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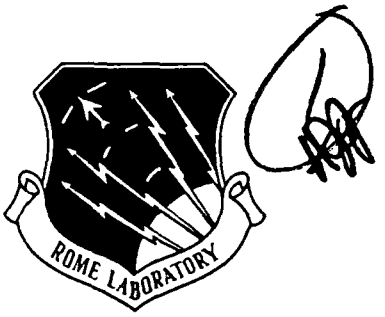

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RELIABILITY ANALYSIS OF SURFACE MOUNT TECHNOLOGY (SMT)

Harris Corporation

Chris A. Myers, Kalyan K. Chakrabarti,
Dr. Donald H. Merlino, Edward G. Palmer,
and Edward F. Pello

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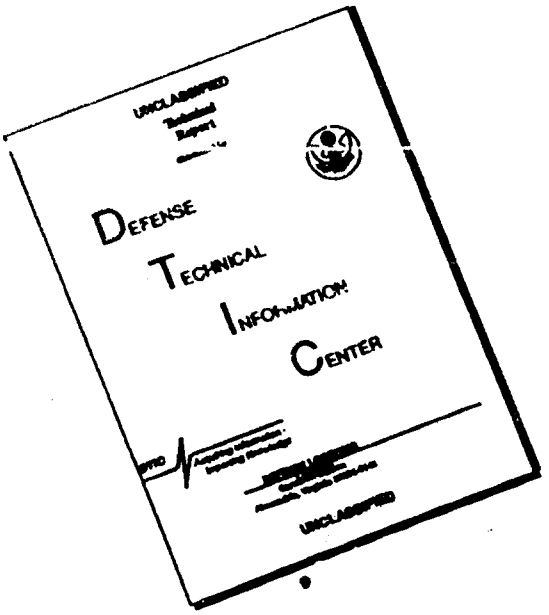

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13. ABSTRACT (Maximum 200 words)

This report indoctrinates the reader with the understanding of what is involved and necessary in designing and assessing the reliability of surface mount products. Deterministic methods were used to identify the primary design and environmental drivers and statistical methods were used to generate a SMT reliability assessment model. Due to the unavailability of field failure data, finite element analyses (FEA) and environmental test data were used to quantify the model parameters. Information obtained during the model development, internal Harris documents, and military and commercial standards were used to generate design, manufacturing and quality guidelines. Finally, reliability testing and its correlation to actual life expectancy is addressed to decide the appropriateness of the of the existing MIL-STD testing requirements and whether these documents need to be modified to correlate to actual life conditions more accurately.

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RELIABILITY ANALYSIS OF SURFACE MOUNT TECHNOLOGY (SMT)

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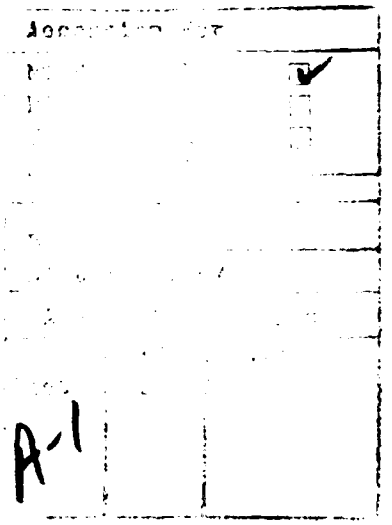

SURFACE MOUNT TECHNOLOGY
RELIABILITY, TESTING AND DESIGN

1.0 EXECUTIVE SUMMARY

The objective of this effort is to develop reliability assessment models, produce a set of design guidelines and evaluate the current testing methods associated with Surface Mount Technology (SMT).

This report indoctrinates the reader with the understanding of what is involved and necessary in designing and assessing the reliability of surface mount product. It also explores areas concerning surface mount solder joint fatigue prediction that have been unanswered, or not fully answered, to provide a reliable means of predicting solder joint life for a given design. Reliability testing and its correlation to actual life expectancy is addressed to decide the appropriateness of the existing MIL-STD testing requirements and whether they need to be modified to correlate to actual life conditions more accurately. The final output of this report is a means of designing surface mount technology assemblies to meet rigorous military conditions and environments.

The following describes the approach taken during the study to ensure an orderly and comprehensive effort, taking advantage of previous efforts and industry literature on similar projects.

1) A literature search was conducted to obtain and quantify reliable test data. The data was examined and statistically analyzed for its applicability for use in the study. There was a significant lack of field data.

2) Finite Element Models (FEM's) with the required flexibility to satisfy the objectives of this project were developed. It was verified that FEM techniques are appropriately useful in determining reliability in the absence of years of field data.

3) Correlation of test data to the Finite Element Analysis (FEA) results was made.

4) An algorithm for MIL-HDBK-217 was developed through reliability modeling, using FEM results and collected data (Appendix B).

5) A Design Guidelines Document was prepared (Appendix A).

6) The test criteria of PR NO. M-9-5510, paragraph 4.1.4 was studied based on solders' material behavior under actual use conditions as compared to test conditions. Recommendations for change were made accordingly.

2.0 INTRODUCTION

Surface mount technology (SMT) involves the placement of electronic components directly onto the surface of a printed wiring board and soldering them into place. The electrical contacts of the component do not penetrate plated-through holes in the board, as do conventional through-hole leaded devices. Surface mount devices (SMD's) are specially designed with terminations on the body, or with leads extending from the body that are designed to support the device mechanically, also providing the electrical interface to the substrate.

Three industry common categories classify surface mount technology: Type I; Type II; and Type III. Type I surface mount assemblies contain solely surface mounted devices on either single or double sided substrates. Type II is referred to as mixed technology, as this type contains both through-hole devices and surface mount devices. The SMD's are typically on top, only, for a Type II SMT assembly. Type III assemblies are through-hole assemblies with small, usually passive devices soldered to the bottom of the board.

There are several categories of surface mounted devices: passive devices which are usually leadless; leaded active devices; leadless active devices; and fine pitch devices. Passive devices are the basic resistors, capacitors and various inductors, coils, and diodes found in

most electronic applications. Active devices, integrated circuits, etc., are multiple I/O devices that require a more complex package. Fine pitch devices are active devices having a lead pitch of 0.025" or less. Twenty five and 20 mil pitch devices are the two primary styles in use, with 15 mil and smaller becoming available. These devices are categorized separately from the standard active devices due to the extra handling and manufacturing requirements necessary to use them.

The benefit of SMT is its capability to reduce size and weight of electronic assemblies by increasing the interconnect density and to provide these benefits at a lower cost. The choices and options in selecting the correct substrate, components and interconnect method are many, and not necessarily obvious. Improper design of a SMT assembly can lead to short lived systems or field failures upsetting critical mission requirements. This document is designed to guide the designer through the selection process to obtain a reliable, manufacturable product. The designer must understand the mechanical interactions between materials chosen, as well as their applicability in the manufacturing processes to be used. This requires complete cooperation and interaction between the electrical, mechanical, components, reliability, test and manufacturing engineers.

2.1 BACKGROUND

In the past ten years, HARRIS has performed a number of reliability studies on Surface Mounted Devices, most specifically on Leadless Chip Carriers. Studies have been performed on Minuteman, MICNS (Observation Drone), OTA (Hubble Telescope), Agusta, and numerous other programs. During early development and use of LCC's, we realized the implications of directly mounting them to unconstrained G-10/FR4 Printed Wiring Boards. A team of design, component and manufacturing engineers developed and patented a compliant lead socket for use with the LCC's until other alternatives were available. This early experience with surface mount technology spurred further interest and concern for the reliability of LCC's and all other surface mounted devices. We have completed a three year HARRIS funded program evaluating the design, manufacturing and reliability of SMT as it applies to the military arena of electronics.

Under the program, tests were conducted to obtain data for analysis of failure trends in surface mount solder joints. The primary purpose of the activity was to develop a significant understanding of the reliability limits of SMT in the military environment. The activity was centered around a substantial test program designed to verify published data and establish new information in areas of specific interest to HARRIS. The study has helped to resolve conflicts in published data.

In the HARRIS study, it was confirmed that LCC's direct mounted to PWB's with significantly different coefficients of thermal expansion (CTE) were a reliability concern. The larger the device, the greater the risk. The risk was markedly reduced when the component and the substrate material CTE more closely matched, particularly the G10/CIC core structure. However, other reliability factors came in to play when the x and y axes were constrained. The greater the constraint of the x-y axes in G10/FR4, the greater the z-axis expansion became, causing plated through hole failures, even on low aspect ratio (2:1) holes. The surest method of increasing the reliability of the SMT assemblies was shown to be the use of compliant leads. This fact was independent of PWB material or the amount of CTE matching attempted on the assembly.

2.2 SCOPE

This effort included the formulation of reliability assessment models for MIL-HDBK-217, "Reliability Prediction of Electronic Equipment." Models were developed for leadless chip carriers (LCC's), leaded (gull-wing) chip carriers (LDCC's), S-lead chip carriers, and J-lead chip carriers (Figure 2.2-1). An algorithm was developed which translates the number of cycles to failure for every component to a failure rate for surface mounted assemblies. The models predict time-to-failure values. These time-to-failure values are transformed into failure rate values which are applicable to MIL-HDBK-217. Each model will be demonstrated using specific design examples (Table 3.12-1).

This effort included the development of a set of design guidelines. These guidelines provide the proper methodology as well as incorrect aspects of SMT design.

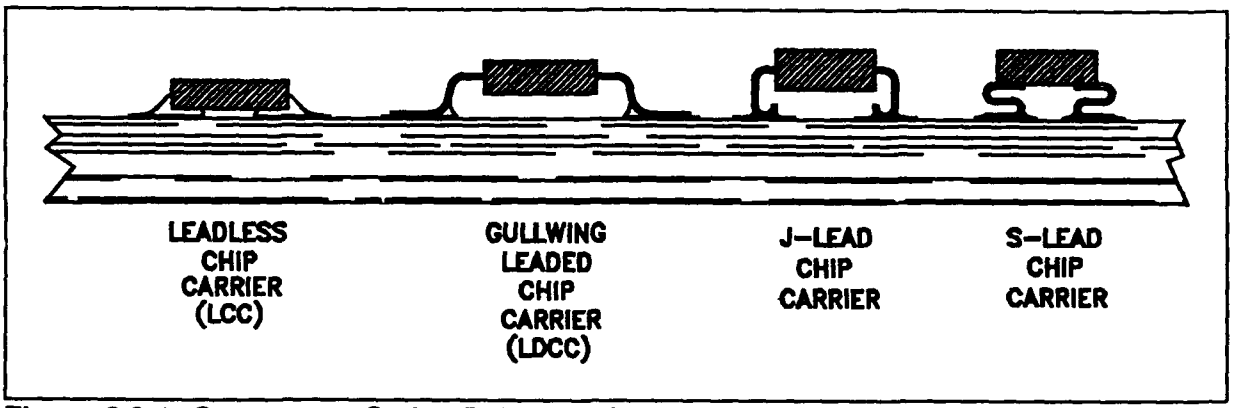

Figure 2.2-1 Component Styles Being Analyzed

Qualification test criteria were evaluated. Only minor modifications to these criteria are recommended. It is the interpretation of the results and extent of there use which should be altered. This is explained in Section 4.0 of this report.

3.0 Reliability Model Development

The following outlines in detail the development of the Surface Mount Technology (SMT) reliability models using MIL-HDBK-217 methodology. A summary of the output from this effort is presented in Appendix B.

3.1 SMT RELIABILITY MODEL BASIS

The development of a failure rate model for solder joints on surface mount devices was approached in a new way. The surface mount model was derived directly from the deterministic physics of the primary failure mode of the solder joint using material properties, design details, expected usage data and finite element analysis. Typical models in the past were based on regression methods using available field data. The availability of field data was too limited to generate any meaningful results.

The underlying assumption in using the model is the superposition model. The superposition model is a modified competing risk model used to combine life failure distributions. The model is not limited to specific types of failure distributions and does not require that the failure distributions be of the same type. This model does require that the failure distributions

be independent of each other. This model can be used to address each failure mode and life event. In general:

P(t) = R(early life) x R(Random) x R(end of life) **(Equation 3.1-1)**

where p(t) is the probability of success at time t
R is the reliability at time t of each phase

- The early life reliability is usually an increasing reliability function. Because it is an increasing function of time the failure rate is decreasing. Early life field failures are the result of manufacturing process defects, design deficiencies and vendor defects (part failures) which are not eliminated by manufacturing screens.

- Random failures are those which occur due to random stress and strength conditions occurring during normal use attributed to the overlap of many distinct time/stress freak distributions each having a discrete physical cause but at the aggregate level appear to happen at a constant time based rate.

- Wear out is the characteristic whereby the solder material exhibits failures due to the accumulation of stress conditions which cause physical breakdown of the solder material. The solder joint data indicated four primary failure modes which result in wear out; fatigue due to thermal and power cycling, creep, tensile stress, and shock/vibration loads.

The approach to the model development concentrated on the types and causes of solder joint failures with each mode considered separately which could then be combined under the superposition concept. The definition of a failure was based on a solder joint fracture which would lead rapidly to an open circuit causing a loss of operating function.

Surface mount solder joints have early life failures due to manufacturing anomalies, random variability of events due to in use periodic stresses exceeding strength of joints or wear out modes primarily caused by the fatigue nature of use stresses and physical properties of the solder formulation and design factors.

To address these separate causes, the modeling addressed each condition individually. It should be noted that the early life failures are minimized and/or eliminated by the use of screening as part of the manufacturing process. Therefore, the failure rate defined by the models are effected by the screening conducted.

In electronic equipment, the failure mode of primary concern is an open circuit. The following table defines the primary causes of SMT open solder joint failures as established in the literature[43,45].

Table 3.1-1 Solder Joint Failure Modes and Causes

Failure Mechanism Driving Factors	Failure Mechanism	Acceleration Relationship
Thermal Cycle	Solder Fatigue - CTE mismatch of PWB and part case materials	T_{max}/T_{min} Rate of Change Dwell
Power Cycle	Induced Solder Fatigue - Power dissipation in part results in solder joint strain due to CTE mismatch as with Thermal Cycling	Thermal Resistance Power Dissipation Power Cycling (On/Off)
Vibration, Fatigue	PWB deflection due to vibration environment causes solder joint tensile stress.	SMT Package Size Vibration Input Level PWB Size
Corrosion	Composition of solder	Humidity (RH%) Temperature

3.2 RELIABILITY MODEL CRITERIA

The failure rate model for SMT application is driven by these primary criteria:

- Must be derived from the Finite Element Analysis (FEA)
- Must reflect the primary design drivers
- Must be similar in structure to MIL-HDBK-217 models in ease of use and must allow

a constant failure rate (i.e., exponential reliability model).

- Must model the predominant failure mechanisms

A secondary objective was for the parameters developed for the equation to be directly related to design controllable variables.

Based on the available literature, the predominant cause of failure[45,71,72,73,75] is thermal cycling induced stress. This mechanism was the primary and only mechanism selected for inclusion in the model. Shock and vibration was not included as the effect is extremely dependent on the application and would make the model too complex to be useful.

3.3 RELIABILITY MODEL

The basic failure rate model derived for SMT is shown in equation 3.3-1. The following paragraphs define the details of each parameter development.

$$\lambda = \frac{[N_u^{\beta-1}]}{(A \cdot B \cdot C \cdot N_f)^{\beta}} \cdot P \cdot (U \times 10^6) \cdot \pi_Q \qquad \text{(Equation 3.3-1)}$$

λ is Failure Rate in failures per 10^6 hours
N_u is Service Life Usage Thermal Cycles in cycles
β is the Distribution Parameter - dimensionless
A is Package Size Factor - dimensionless
B is Standoff Height Factor - dimensionless
C is Coefficient of Thermal Expansion (CTE) Mismatch Factor- dimensionless
N_F is Characteristic Life for Baseline Package = $(K \cdot e^{D-E\Delta T})$ in cycles
P is the Number of Package Pins (=8)
U is Cycle Rate: Cycles/Hour Over Life
π_Q is the Quality Factor

3.4 FINITE ELEMENT ANALYSIS CYCLES TO FAILURE

One of the conditions stipulated was for the model to use deterministic methods. Finite

Element Analysis (FEA) is a recognized method for mechanical analysis. The FEA analysis conducted for this study is described in Appendix D. The output of the FEA is strain values. Solder life strain data was used to define the mean cycles to failure. Since solder has both plastic and elastic strain conditions in use, the FEA considered both in deriving the strain values. A set of package styles, pin counts, and baseline design data provided the data set from which the FEA results were obtained. Temperature ranges were chosen based on previous study work (Mantech, etc.), as well as engineering judgement based on various mission/application possible ranges.

The FEA strain data is converted to mean cycles to failure using the Coffin-Manson equation. The Coffin-Mansion equation is shown in equation 3.4-1. An example of mean-cycles-to-failure calculation can be seen in Appendix D, Pg. 6,7.

$$\frac{\Delta\varepsilon}{2} = \frac{\sigma_f}{E}(2N_f)^b + \varepsilon_f(2N_f)^c \qquad \textbf{(Equation 3.4-1)}$$

Where,

$\Delta\varepsilon/2$	=	Total Strain Amplitude
σ_f	=	Fatigue Strength Coefficient
ε_f	=	Fatigue Ductility Coefficient
b	=	Fatigue Strength Exponent
c	=	Fatigue Ductility Exponent
N_f	=	Mean Number of Cycles-To-Failure
E	=	Young's Modulous of elasticity for solder - psi

The data set derived the cycles to failure for the various package, pins and thermal ranges. The mean number of cycles to Failure (N_f) from the above equation is the mean value of a distribution of values caused by material variability for σ_f and ε_f. Table 3.4-1 summarizes the data sets derived from the FEA which formed the basis of the SMT reliability model.

The calculated number of cycles to failure shown in Table 3.4-1 reveals two important facts. The first is that the data for leaded devices, if plotted on a course scale, trace curves that fall on top of one another, whereas on the same plot, the curve for leadless devices are several orders of magnitude lower than the leaded devices. This highlights the effects of lead compliance on total strain.

Table 3.4-1 FEA Calculated Strain and Cycles to Failure Data Base
(Given as a function of temperature range.)

	Thermal Range						
Package Type	-55°C/ +125°C (180°C Δ)	-55°C/ +105°C (160°C Δ)	-55°C/ +85°C (140°C Δ)	-30°C/ +50°C (80°C Δ)	-55°C/ -15°C (40°C Δ)	+20°C/ +60°C (40°C Δ)	
16-LCC	0.0137 3.5E02	0.0104 6.6E02	0.0068 1.8E03	0.0010 5.8E06	0.0006 6.5E09	0.0022 4.6E04	Strain - in/in Mean cycles to Failure
24-LCC	0.0187 1.8E02	0.0142 3.3E02	0.0092 8.7E02	0.0011 2.0E06	N/A N/A	N/A N/A	
32-LCC	0.0243 1.0E02	0.0182 1.9E02	0.0114 5.3E02	0.0012 1.1E06	0.0007 5.1E08	0.0030 1.7E04	
68-LCC	0.0442 3.0E01	0.0325 5.5E01	0.0189 1.8E02	N/A N/A	N/A N/A	N/A N/A	
16-GULL	0.0023 4.2E04	0.0017 1.4E05	0.0012 1.6E06	0.0005 4.6E11	0.0004 7.2E13	0.0005 4.3E11	
32-GULL	0.0024 3.3E04	0.0018 1.1E05	0.0012 1.1E06	0.0005 4.6E11	0.0004 7.2E13	0.0005 2.7E11	
16-"J"	0.0025 3.0E04	0.0018 1.2E05	0.0012 1.2E06	0.0006 2.3E10	0.0005 2.4E12	0.0006 7.7E10	
16-"S"	0.0021 6.1E04	0.0014 3.3E05	0.0010 7.3E07	0.0006 7.6E09	0.0005 4.1E12	N/A N/A	

The primary output from this effort is N_f, mean cycles to failure.

The second fact is that the last two columns, -55°C/-15°C and +20°C/+60°C, are both 40°C ΔT ranges but result in significantly different cycles to failure. The effects of this on reliability calculations is discussed in 3.5.1.1. The reason for this difference is that the material

properties of solder change significantly as a function of temperature. Specifically, the Modulus of Elasticity increases as temperature decreases. That is, solder can support more load at lower temperatures than at higher temperatures.

Small temperature excursions and lower mean temperatures coupled with high lead compliance yields significantly higher reliability. The consequence of this is that life tests at elevated temperatures are difficult to correlate to actual projected fielded performance. Test data that more closely resembles actual field conditions is required to improve our confidence in predicting reliability.

3.5 REGRESSION EQUATION FOR CYCLES TO FAILURE

The FEA data shows the dependence of solder joint life as primarily a function of the thermal cycle range. Therefore the model would have to reflect this condition. The method selected to translate the model to a usable form was to develop a regression based mean cycles to failure equation with thermal cycle range as the independent variable. This was accomplished by inserting the data into a regression statistical analysis package. The package used was STATGRAPHICS.

The results provided a regression fit equation defined for the mean number of cycles to failure verses the temperature cycling range. A baseline regression equation was derived for each pin configuration; LCC, GULL, J, S. The basic form of the regression equation is:

$$N_f = e^{(D-E\Delta T)} \qquad \textbf{(Equation 3.5-1)}$$

Table 3.5-1 shows the derived equations. The regression equation models fit identified that exponentially based equations provide high correlation coefficients. As with any curve fit equation, there is variability about the exact data points used in the fit. To resolve this variability for the SMT model, the 90% confidence interval was selected for continued model development. The lower interval level was used and the basic curve fit equations were derived for the 90% interval. Figure 3.5-1 shows the 16 pin LCC curve fit and confidence interval. The rest of the curves are provided in Appendix C. A plot of all four regression

equations is shown in Figure 3.5-2.

Table 3.5-1 Regression Equations Parameters **Form = $e^{(D-E\Delta T)}$**

Package	Mean Cycles to Failure		90% C_l Cycles to Failure	
	D	E	D	E
16 Pin LCC	26.3	0.123	23.8	0.123
16 Pin Gull	38.8	0.164	36.7	0.164
16 Pin J	34.1	0.137	33.4	0.137
16 Pin S	33.7	0.125	31.8	0.125

The extent of the FEA assessments and data points available for model development was limited by the number of FEA runs conducted. Therefore to account for all the possible different package size and pin style configurations a modification of the approach of separate models for each package style and size was needed. To accomplish the modeling, it was decided to select a basic set of equations for one package of each pin style. Multipliers would then be used to adjust the baseline cycles to failure for each of the other package sizes. The 16 pin package size was selected as the baseline and the regression equations for these used in further model definition. The basic equations for each of the 16 pin baseline models verses the temperature change is shown in table 3.5-1.

3.5.1 THERMAL TEMPERATURE RANGE

The derived regression equation(s) are based on the thermal temperature range as the independent variable. Therefore, definition of the proper thermal range is needed to generate the correct cycles to failure. The thermal range from the FEA is a single value. In reality the range is a function of three factors:

- Thermal excursion due to ambient environment
- PWB internal thermal rise above ambient
- Thermal rise due to power dissipation of integrated circuit

The algorithm for defining the temperature range with the effects of average joint temperature is shown in equation 3.5.1-1.

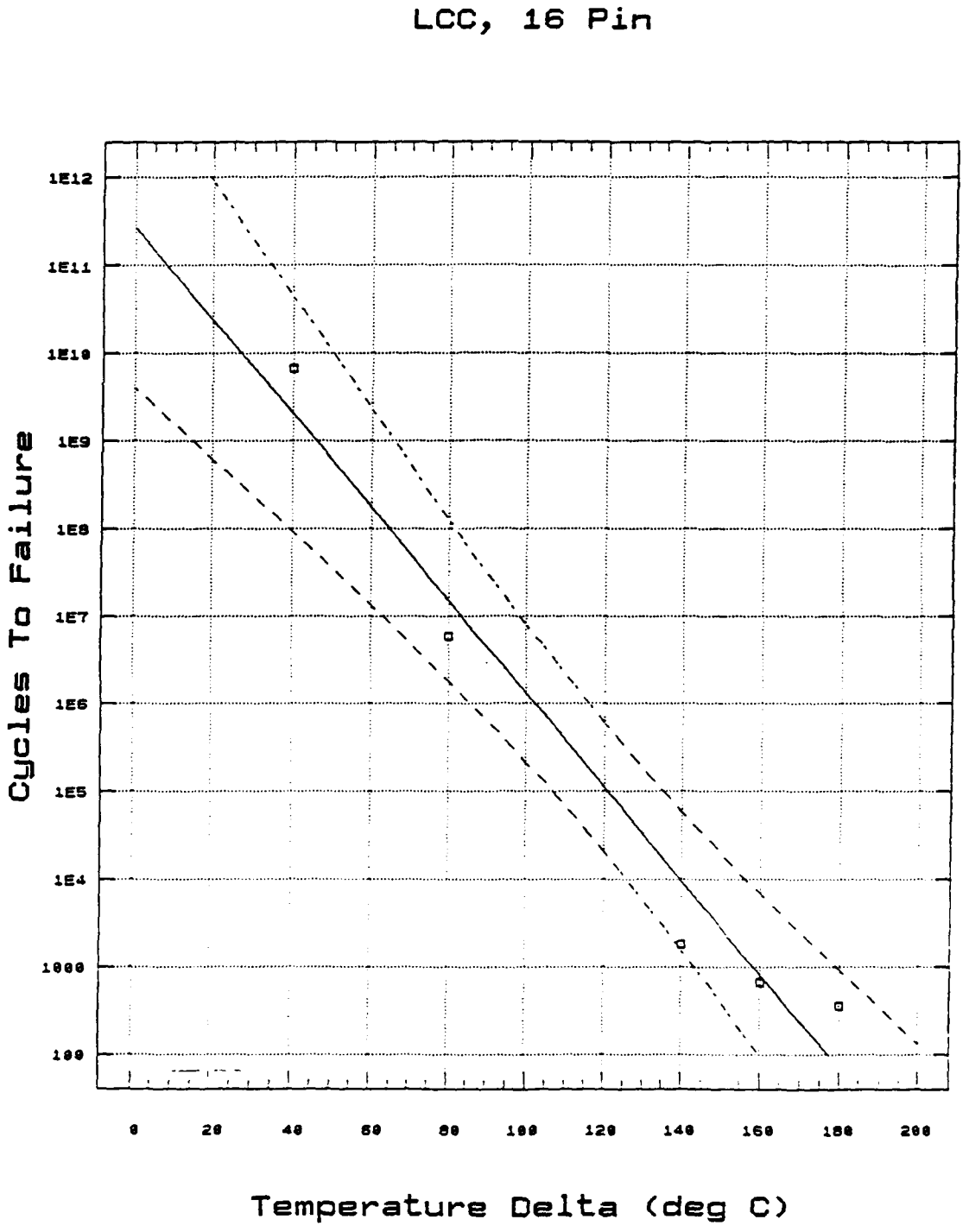

Figure 3.5-1 The Regression Plot of Derived Equation, 16 Pin LCC Package

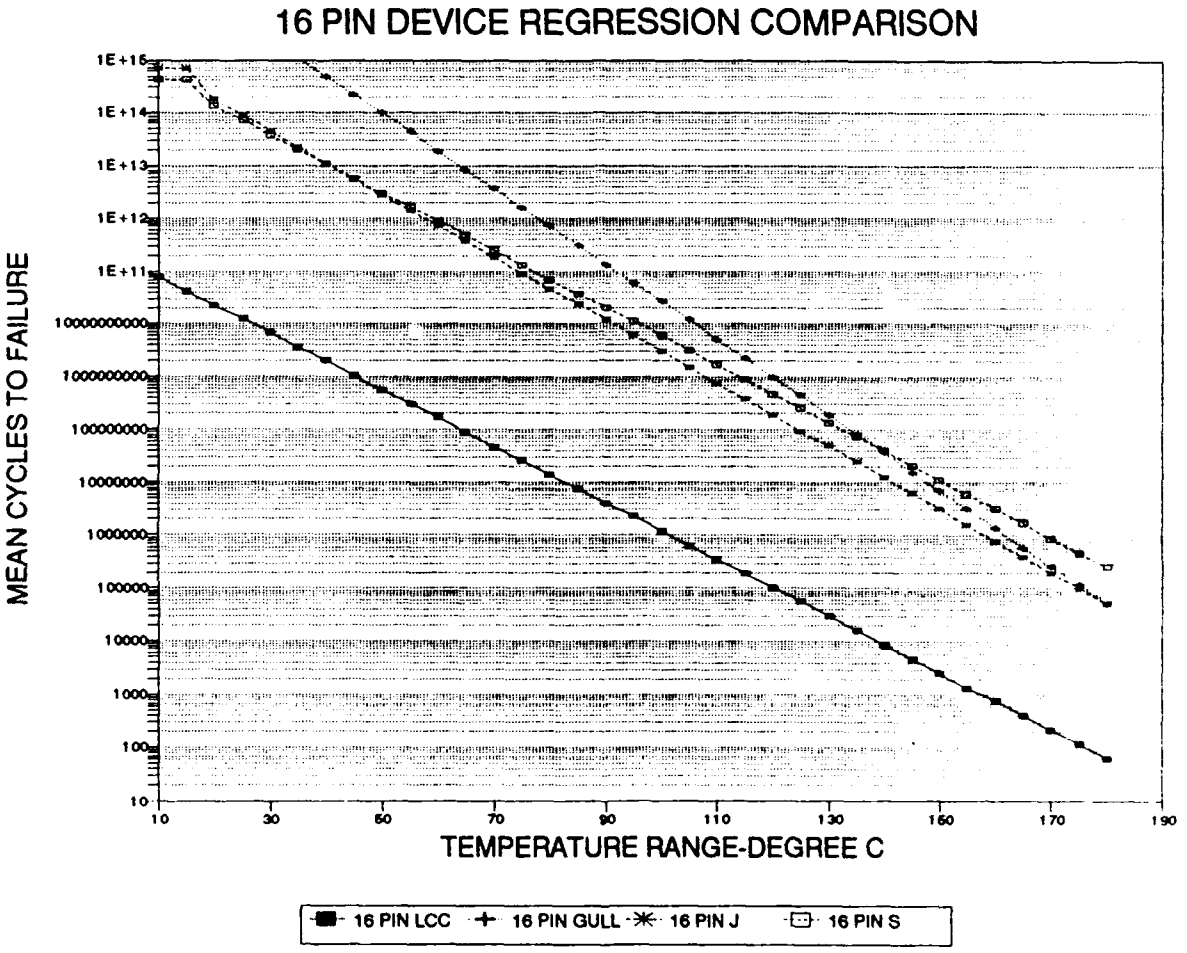

Figure 3.5-2 Regression Curves for the Four Package Styles

$$\Delta T = [(T_{max} - T_{min}) + (\Theta_{CA}\, P_{DIS})] + 3.0[(T_{max} + T_{min})/2 - 25] \quad \text{for } T_{avg} \geq 25°C \qquad \text{(Eq. 3.5.1-1)}$$

Where:

T_{max} is the maximum operating temperature (mission) for the PWB

T_{min} is the minimum operating temperature (mission) for the PWB

Θ_{CA} P_{DIS} defines case temperature of the integrated circuit above the PWB temperature caused by the power dissipation in the component.

$[(T_{max} + T_{min})/2 - 25]$ is the factor for effects of average solder joint temperature above 25°C

Θ_{CA} is the thermal resistance between the part and the PWB in °C/W.

P_{DIS} is the part power dissipation.

For modeling purposes, a typical value is provided for the handbook. This algorithm is provided for users who may have more detailed data available to them (Section 3.6.1.1).

3.5.1.1 Thermal Temperature Range Adjustment Derivation

The FEA results in Table 3.4-1 indicates that the cycles to failure is influenced by the temperature range. The results also show a dependence on the average temperature within the range. For example the data for a 40 degree temperature excursion from -15 to -55 results in a mean cycles to failure of 6.5×10^9. For the same 40 degree excursion from 20 to 60 C the mean cycles to failure is 4.6×10^4. This difference, a factor of 10^5 is significant. This difference is seen for all lead styles. This implies that the cycle life is a function of the average joint temperature as well as the thermal cycle range. This effect was also observed by Engelmaier.[70,74,75]

A correction factor to account for this effect is necessary for joints with average temperatures which differ from a nominal. The approaches available were limited to a empirical approach which provides limited correction for this effect as there was not enough FEA analysis results to address more detailed means. The approach was based providing a single correction factor to the thermal environmental induced excursion and power cycling induced thermal delta temperature used in the calculation. The basis of the mean cycles to failure of the regression equations were material characteristics at 25°C. This became the reference temperature for regression equations in section 3. The average temperatures for the plotted FEA conditions ranged from 10 to 40°C except for the -15 to -55°C condition. The empirical correction factor was applied only to thermal range for average temperature higher

than a 25°C average. This serves to reduce the cycles to failure corresponding to the results of the FEA discussed above:

For example the characteristic cycles for the 40 degree delta with the correction factor applied to the 20-60 degree data results in the regression equation cycles of 6.2E5 verses the FEA result of 4.6E4. *This correction is only applied to average temperatures above the 25 degree level.* No correction is provided for lower temperatures as the present results continue to provide a conservative estimate of cycles to failure without the correction.

3.6 DISTRIBUTION CONSIDERATIONS

The regression models derived in the previous section determines the mean cycles to failure. The mean value is the center of a scatter plot of all possible values. The distribution of cycles to failure about this mean impacts when failures occur. Based on literature reviews, a Weibull failure distribution was found to be descriptive of the variation of solder joint failures based on testing of LCC and leaded devices. This model was therefore selected to define the distributions. Weibull distributions can account for many failure distributions. In addition, Weibull analysis techniques are used in MIL-HDBK-217 motor models.

A second approach was investigated based on probabilistic stress-strain distributions, as exemplified in work by Lambert[49]. This approach, described in Reference 83, utilized distributions of stress and strength, and their variability to define probability of failure. This approach requires more data variability on stress, which was not available from the data sets.

The Weibull model mathematical basis is defined equations ^ 3-1 to 3.6-5 below. The selection of a model was based on design to maintain consistency with MIL-HDBK-217 where a constant failure rate is used for simplicity. Therefore, the model hazard rate should be a constant. The hazard rate of the Weibull distribution is not constant but is time dependent. A simplifying assumption was made to make the hazard rate constant. Mathematically, this can be accomplished by taking an average rate over the total use period. This results in the basic failure rate model with a failure rate which can be treated as constant, consistent with other MIL-HDBK-217 failure rates.

Weibull Model:

$R(t) = e^{-[(t1-t0)/N]\beta}$ Reliability Function **(Equation 3.6-1)**

$F(t) = 1 - e^{-[(t1-t0)/N]\beta}$ Cumulative Failure **(Equation 3.6-2)**

$h(t) = \beta/N \cdot [(t_1-t_0)/N]^{\beta-1}$ Hazard Rate **(Equation 3.6-3)**

t_1 - use time (or N_u use cycles)
t_0 - time to first failure (or N_{u1} cycles to first failure)
N - characteristic life time (or cycles)
β - distribution parameter

Because h(t) is not constant for wear out failure modes, (i.e., exponential model $h(t) = \lambda$ constant) a method is needed to add failure rates to other 217E failure rates. Therefore, the average failure rate over an interval is used based on the following:

$$\lambda(t)_{ave} = 1/(t_2 - t_1) \cdot \int_{t_1}^{t_2} h(t)dt \quad \textbf{(Equation 3.6-4)}$$

Set $t_1 = 0$

$$\lambda(t)_{ave} = H(t) = t^{\beta-1}/N^{\beta} \quad \textbf{(Equation 3.6-5)}$$

The Weibull model provided a second benefit in that a parameter in the model is directly relatable to the mean cycles to failure from the regression results. The Weibull model parameters are discussed below.

3.6.1 USE CYCLES (N_u)

The first parameter is N_u, usage cycles. In this case the number of thermal cycles expected over the service life of the equipment is needed. The usage cycles is dependent on the equipment application which is directly related to the existing environmental factor categories presently in MIL-HDBK-217. Because this data is derived, a table of default usage values was defined based on available literature and mission analysis data.

The Weibull model also has a parameter, (t_o in equations 2.6-1, -2, -3), which is the cycles to first failure. In most instances the values can be assumed to be zero because in the limit, there is always a chance of a failure at or on the initial cycle. This assumption is the most conservative approach and was therefore used in the model. Should data become available in the future, the parameter could be included.

3.6.1.1 THERMAL ENVIRONMENT DEFAULT VALUES

The use and life conditions are not always available to the user. Therefore, to provide ease of use, a compilation of typical specification thermal conditions, temperature ranges and estimated thermal cycle ranges applicable to equipments would allow early use of the model until more detailed data is available.

The approach to defining the typical thermal range is based on existing MIL-Standards and Handbooks and literature surveys. The approach stated with compilation of the major thermal requirements defined in the MIL-standards typically used in equipment design. To maintain similarity to environmental categorization already excising in MIL-HDBK-217, the standards were further classified into the closest MIL-HDBK-217 environment category (π Environment). Table 3.6-1 through 3.6-3 provide the data summary.

The maximum and minimum thermal ranges (Tmax, Tmin) represent the ambient design extremes within the MIL-specifications. This provides the beginning for a maximum possible thermal range (Range). Because an equipment has internal thermal rises to the PWB where a SMT joint is located and an additional thermal rise of the SMT device case above the PWB ambient an additional factor is required to be added. For the purposes of the model development, an internal rise for each of these additional thermal conditions was assumed. A 15°C rise of the PWB over the ambient and a 10°C rise of the SMT device case above board was selected. This was based on typical airborne thermal stress derating requirements which typically limit thermal junctions to 105°C or less at maximum continuous thermal conditions.

The maximum range indicates a cold start and hot start extreme for the equipment. In the majority of uses, the starting temperatures are less than the extremes. It is not realistic for a

unit to experience both extremes in a single mission use therefore an assumption was made that a typical level would usually result in not more than 1/2 of this design range throughout any regime.

An assumption for inhabited environments was that the typical temperatures for operation were 25°C. This applies to airborne inhabited, ground fixed and naval sheltered conditions. This assumption is based on the fact that human operations are limited for operator effectiveness. This condition therefore limits thermal cycling where inhabited conditions exist to a single thermal excursion from the starting point to the 25°C ambient.

To substantiate the assumed rises, MIL-HDBK-781 was reviewed for the thermal levels identified as typical test levels. This document contains simulated mission profiles with hot/cold day starting temperatures used for reliability testing. The test profiles are derived to be representative of mission profiles. The test profile thermal excursions for the mission phase were surveyed. The average of the various profiles was taken as the typical delta temperature. The SMT joint was determined as the typical data plus a 25°C rise to account for thermal rises to the solder joint. The handbook contains test missions for airborne, naval, ground applications. Space and missile uses are not specifically addressed.

For the missile and space environments, no Handbook data was available. The level was assumed the same as the calculated average range. For the Naval use factors similar assumptions were made.

3.6.1.2 Service Life, Use Default Values

The model requires the definition of use cycles, equivalent use times and number of thermal cycles. The approach to developing these parameter is based on surveys of MIL-specifications, and literature surveys.

Use cycles represent the number of thermal cycles the SMT joint will experience in a service lifetime. To develop this an equipments life cycle and mission use profiles are necessary. The life cycle includes all the thermal excursion events. Events in most equipments include

environmental stress screening thermal cycles, non operating daily diurnal thermal cycles resulting from daily temperature changes and storage conditions, maintenance thermal cycling from power cycling the equipment and operational mission thermal cycles.

Diurnal thermal cycling occurs on a daily basis. MIL-STD-210 contains data on the thermal excursion for hot, cold humid environments. This thermal cycling applies to equipments in all applications except ground fixed and benign applications. The typical ranges are categorized into climatic regions. Generally, daily thermal excursions are averaged at 17°C over all categories. With typical equipment life of 20 years at one cycle per day this results in 7300 thermal cycles. Because the regression curves show a significant mean cycles to failure at the low thermal excursion, the effects of this cycling were considered negligible.

Environmental stress screening (ESS) conducted during manufacturing are typically to the extremes of the equipment specifications. ESS is conducted to eliminate defective SMT joints. However, as shown in the regression equations, the mean cycle life is affected by the number and levels of thermal excursions. The number of the cycles is low, but due to the high thermal levels, the impact on life must be considered. For the purposes of this model an assumption was made that the number of thermal cycles in ESS is held to less than 0.1% of the cycle life capability shown in the regression curves and therefore has no negligible effect on the calculation.

The maintenance cycling consists of powering a unit on/off to aid failure diagnosis. The thermal excursions typically limited to the equipment internal thermal rises. The thermal rises assumed above of 25°C while higher than the diurnal cycling, are limited in number. These cycles are therefore negligible.

The mission induced thermal cycles are the predominant source of thermal cycles for the model. The mission includes the powering of the equipment, the use of the equipment with external thermal conditions changing due to power cycling, external environmental changes, and cooling provisions. The equipment service life in terms of mission is typically not specified. However, service life in terms of operating hours is generally specified. Therefore, the approach used was to survey equipment specifications, determine the service life

operating hours, define the typical mission duration using MIL-HDBK-781, calculate a typical mission cycle count by dividing the service life hours by the typical mission length, and evaluate the number of thermal changes occurring during the typical mission from the typical profiles in MIL-HDBK-781. The number of thermal cycles is then the product of the number of missions times the cycles per mission. Table 3.6-4 provides the default factors and derivation basis.

Table 3.6-1 Aerospace Use Factors

Spec.	Tmax °C	Tmin °C	Range (R) Spec	Maximum Range (1) °C	Ave ΔT Range (2)	217E Environment Factor	Mil-Hdbk 781 ΔT (3)	Typical ΔT * (5)
MIL-E-5400 - Electronics Equipment - Airborne, General Specification for								
-1	55	-54	109	134	67	A_I (4)	50	75
-1B	55	-40	95	120	60			
-2	71	-54	125	150	75	A_U	55	80
-3,5	95	-54	149	174	87			
-4	125	-54	179	204	102			
MIL-E-8189 (Inactive for New Designs) Electronics Equipment, Missiles, Boosters, and Allied Vehicles, General Specification for								
-1	55	-54	109	114	67	M_{FF}	N/A	75
-2	71	-54	125	150	75			
-3,5	95	-54	149	174	87			
-4	125	-54	179	204	102			
DOD-E-8983 Electronics Equipment, Aerospace, Extended Space Environment, General Specification for								
	71	-34	105	130	65	S_F	35	55
	61	-24	85	110	55			

(1) Range with 25°C internal rise to SMT joint
(2) Average Temperature = Maximum Range/2
(3) MIL-HDBK-781 related test range, worst case of hot or cold day
(4) Inhabited Ambient at 25°C
(5) Typical ΔT = MIL-HDBK-781 ΔT + 25°C

Table 3.6-2 Naval Use Factors

Spec.	Tmax °C	Tmin °C	Range (R) SPEC	Maximum Range °C (1)	Ave ΔT Range	217E Environment Factor	MIL-HDBK 781 ΔT (3)	Typical ΔT (Est.) (5)
MIL-E-16400 (Superseded by MIL-STD-2036)Electronic Interior Communication and Navigation Equipment, General Specification for								
Unsheltered	65	-54	119	144	72	N_U	55	80
Unsheltered	65	-28	93	118	59			
Unsheltered	50	0	50	75	37.5	N_S	45	70
MIL-STD-2036 - General Requirements for Electronics Equipment Specifications								
Uncontrolled (Full)	65	-28	93	118	59	N_U	55	80
Controlled (Full)	50	0	50	75	37.5	N_S	40	65
Uncontrolled (Minimal)	50	-28	78	103	51.5	N_U	55	80
Controlled	50	10	40	65	32.5	N_S	40	65

(1) Range with 25°C internal rise to SMT joint
(2) Average Temperature = Maximum Range/2
(3) MIL-HDBK-781 related test range, worst case of hot or cold day
(4) Inhabited Ambient at 25°C
(5) Typical ΔT = MIL-HDBK-781 ΔT + 25°C

Table 3.6-3 Ground Use Factors:

Spec.	Tmax °C	Tmin °C	Range (R) Spec	Maximum Range °C (1)	Ave ΔT Range (2)	217E Environment Factor	MIL-HDBK 781 ΔT (3)	Typical ΔT (Est.) (5)
MIL-E-4158 - Electronic Equipment Ground, General Specification for								
	49	-51	100	125	62.5	G_F	55	80
	49	-40	89	114	57			
	71	0	71	91	48			
	82	0	52	77	38.5	G_B	30	45
	68*	-57	125	150		Storage	--	20
MIL-T-28800B - Test Equipment for Use with Electrical and Electronic Equipment, General Specification for								
-1	55	-54	109	134	67	G_M	55	80
-2	55	-40	95	120	60			
-3	55	-15	70	95	47.5			
-4	55	0	55	80	40	G_F	35	60
-5	50	0	50	75	35	G_B	20	45
-6	40	10	30	50	25			
NO	85	-62	147	172		Storage		40
MIL-E-164008 (Superseded)Electronic, Interior Communication and Navigation Equipment, Naval Ship and Shore, General Specification for								
Unsheltered	65	-54	119	144	72	G_M	55	80
Shore	52	-40	92	117	58.5	G_F	35	60
Sheltered	50	0	50	75	37.5			

*Estimated

(1) Range with 25°C internal rise to SMT joint
(2) Average Temperature = Maximum Range/2
(3) MIL-HDBK-781 related test range, worst case of hot or cold day
(4) Inhabited Ambient at 25°C
(5) Typical ΔT = MIL-HDBK-781 ΔT + 25°C
NO = Non-operating

Table 3.6-4 Derived Default Use Factors

MIL-HDBK Environment Category (1)	Typical Delta Temperature °C (2)	Typical Life Hours (3)	Typical Cycles Cycles (4)	Typical Cycle Rate U (5)	Default Life Hours (6)	Default Cycles N_U (7)	Default Cycle Rate U (5)
G_B	45	41600	5200	0.125	45000	7500	0.17
G_F	60	20800	5200	0.25	25000	7500	0.30
G_M	80	10400	10400	1.00	12000	15000	1.25
N_S	65	43680	3640	0.08	45000	8000	0.18
N_U	80	21840	3640	0.17	25000	8000	0.32
A_{IF}	75	7200	4800	0.67	10000	10000	1.00
A_{IC}	75	9600	2400	0.25	15000	5000	0.33
A_{UF}	80	7200	9600	1.33	10000	20000	2.00
A_{UC}	80	9600	3600	0.38	15000	10000	0.67
A_{RW}	75	6000	4000	0.67	10000	8000	0.80
S_F	55	43800	27375	0.63	50000	30000	0.60
M_F	65	1	1	1.00	10	10	1.00
M_L	65	1	1	1.00	10	10	1.00
C_L	65	1	1	1.00	10	10	1.00

G_B - 8 HR/MISSION CYCLE x 5 DAYS/WEEK x 20 YRS	1 THERMAL CYCLE PER MISSION
G_F - 4 HR/MISSION CYCLE x 5 DAYS/WEEK x 20 YRS	1 THERMAL CYCLE PER MISSION
G_M - 2 HR/MISSION CYCLE x 5 DAYS/WEEK x 20 YRS	2 THERMAL CYCLES PER MISSION
N_S - 12 HR/DAY x 7 DAYS/WK x 26 WKS/YEAR x 20 YRS	1 THERMAL CYCLE PER DAY
N_U - 6 HRS/DAY x 7 DAYS/WEEK x 26 WKS/YEAR x 20 YRS	1 THERMAL CYCLE PER DAY
A_{IF} - 35 HRS/MO x 12 MO/YR x 20 YRS, (1.5 HR MISSION)	2 THERMAL CYCLES PER MISSION
A_{IC} - 40 HRS/MO x 12 MO/YR x 20 YRS, (4 HR MISSION)	1 CYCLE PER MISSION
A_{UF} - 35 HRS/MO x 12 MO/YR x 20 YRS	1 THERMAL CYCLE PER MISSION
A_{UC} - 40 HRS/MO x 12 MO/YR x 20 YRS	1.5 THERMAL CYCLES PER MISSION
A_{RW} - 25 HRS/MO x 12 MO/YR x 20 YRS (1.5 HR/MISSION)	1 THERMAL CYCLE PER MISSION
S_F - 5 YR MISSION, CONTINUOUS OPERATION	15 THERMAL CYCLES PER DAY
M_F - 10 HR	2 THERMAL CYCLES PER MISSION
M_L = CL - 1 HR PER MISSION	1 THERMAL CYCLE PER MISSION

A default margin was applied to account for other cycling and maintenance effects.

(1) MIL-HDBK-217"F" proposed environment definitions
(2) Derived delta temperature excursions (Tables 3.6-1, -2, -3)
(3) Engineering estimate based on existing typical specification values - includes all "on" time
(4) Estimated from mission profile usage of various equipments typically used in the environment category.
(5) $U = N_{cycles} / Life\ Hours$ for typical or default parameters
(6) Estimate from typical life plus an estimated margin for uncertainties
(7) Estimate from typical cycles plus an estimated margin for uncertainties

Note: The default life and cycles provides an estimated margin to account for surge usage, wartime expanded usage and unknown contingencies. The default values margin is an estimate above the typical values. The added margin varies from environment to environment.

3.6.2 CHARACTERISTIC LIFE

A required parameter when using the Weibull distribution is the characteristic life value, N_F.

This value represents the point where 63.2 percent of the failures have occurred. The FEA derived median cycle to failure of Equation 3.5-1 is defined as the point where 50 percent of the failures have occurred. To use the regression based cycles in the Weibull model therefore requires the translation of the median cycles (50%) to failure to the characteristic life value (63.2%) within the Weibull model. The relationship between median and characteristic life is defined by the mathematical relationship[42]:

$$N_f = N_F \times (\Gamma(1+1/\beta) \qquad \textbf{(Equation 3.6.2-1)}$$

N_F = the characteristic life (cycles to failure)
Γ = the gamma distribution
N_f = the median cycles to failure, equation 3.5-1

This states that the median life is related to the characteristic life by a Gamma distribution. The value of beta, the distribution parameter of the Weibull model, is described in section 3.6.3 below. Because the model requires the characteristic life and the median life is generated from the FEA regression based models, the median cycles to failure is multiplied by a correction factor (k) using equation 3.6.2-1 and rearranging the equation:

$$N_F = N_f / \Gamma(1+1/\beta) = N_f * k \quad \text{where } k = 1/\Gamma(1+1/\beta) \qquad \textbf{(Equation 3.6.2-2)}$$

k is the correction factor

Tabulated values of the Γ are available in standard mathematical tables. The β parameter is derived as defined in section 3.6.3. This translation is required because the characteristic life is larger than the median life. Without this adjustment, the derived values for failure rate are more pessimistic. Table 3.6.2-1 compares the characteristic life of the four types of solder joint lead attachments evaluated.

3.6.3 DISTRIBUTION PARAMETER

The distribution parameter, Beta (β), is a shape factor which defines the distribution of the failures about the characteristic life. Based on available literature (from test data) the values were tabulated and the minimum value used in the model. The values had essentially the same spread for the leaded style devices. A different value applies to the leadless package. The literature data is shown in table 3.6.3-1.

β - Parametric Estimates:

β = Slope (Distribution) Factor

- Based on Literature/Test Data, Thermal Cycle Tests

Table 3.6.2-1 Baseline Characteristic Life (Cycles to Failure) for Solder Joints, Based on the 16 Pin Regression Equation from the FEA

DELTA T °C	LCC	GULL	J LEAD	S LEAD
5	1.32E+10	4.03E+15	1.7E+14	3.65E+13
10	7.16E+09	1.78E+15	8.6E+13	1.95E+13
15	3.87E+09	7.82E+14	4.3E+13	1.04E+13
20	2.09E+09	3.44E+14	2.2E+13	5.59E+12
25	1.13E+09	1.52E+14	1.1E+13	2.99e+12
30	6.11E+08	6.68E+13	5.5E+12	1.60E+12
35	3.31E+08	2.94E+13	2.8E+12	8.58E+11
40	1.79E+08	1.30E+13	1.4E+12	4.59E+11
45	9.66E+07	5.71E+12	7.1E+11	2.46E+11
50	5.22E+07	2.51E+12	3.6E+11	1.32E+11
55	2.82E+07	1.11E+12	1.8E+11	7.04E+10
60	1.53E+07	4.88E+11	9.1E+10	3.77E+10
65	8.26E+06	2.15E+11	4.6E+10	2.02E+10
70	4.46E+06	9.46E+10	2.3E+10	1.08E+10
75	2.41E+06	4.17E+10	1.2E+10	5.78E+09
80	1.30E+06	1.83E+10	5.9E+09	3.09E+09
85	7.05E+05	8.08E+09	3.0E+09	1.66E+09
90	3.81E+05	3.56E+09	1.5E+09	8.86E+08
95	2.06E+05	1.57E+09	7.5E+08	4.74E+08
100	1.11E+05	6.90E+08	3.8E+08	2.54E+08
105	6.03E+04	3.04E+08	1.9E+08	1.36E+08
110	3.26E+04	1.34E+08	9.6E+07	7.28E+07
115	1.76E+04	5.90E+07	4.9E+07	3.89E+07
120	9.52E+03	2.60E+07	2.4E+07	2.08E+07
125	5.15E+03	1.14E+07	1.2E+07	1.12E+07
130	2.78E+03	5.04E+06	6.2E+06	5.97E+06
135	1.50E+03	2.22E+06	3.1E+06	3.20E+06
140	8.13E+02	9.77E+05	1.6E+06	1.71E+06
145	4.40E+02	4.30E+05	8.0E+05	9.16E+05
150	2.38E+02	1.90E+05	4.0E+05	4.90E+05

GENERAL FORM OF EQUATION: $NF = e^{(D-E\,\Delta T)} \times$ Correction Factor
Correction factor translates median cycles (50%) to Weibull characteristic life (see 3.6.2). Correction factor uses equation 3.6.2-2 and β from table 3.6.3-2. Tabulated values for the Γ function are from CRC Press Standard Mathematical Tables. For LCC, k = 1.129. For Gull, J, and S lead types, k = 1.054.

Table 3.6.3-1 Summary of β Based on Literature Search

Reference	Package Pin Count	Type LCC/Butt(I)/Gull/J	β Value
47	68 P	B (I)	2.2
72	68 P	B (I)	3.2
48	68 P	B (I)	4.0
46	2 C	L	3-6 Mean - 3.68 Min. - 2.2
47	68 P	J	4.6
51	68 P	J	2.58
	68 P	G	3.65
	68 P	J	2.62
	68 P	G	4.44
	68 P	J	1.15
	68 P	G	4.29
7	68 C	J	1.7
	68 C	J	2.7
46	N/A		1.8-3.0
100	68 P	J	6.8
	68 P	G	5.5
	68 P	G	3.3
	44 C	G	1.4
	44 C	G	3.9
	44 P	G	2.5
	44 P	G	5.8

P = Plastic B= Butt or I lead L = LCC J = J Lead
C = Ceramic G = Gullwing F = Flat Pack

Because the β values are greater than 1.0 and have different values for leaded and leadless devices, the value indicates that the distributions are characteristic of a wear out process and that the wear out characteristics of LCC devices are different from that of leaded devices.

Table 3.6.3-2 β Parametric Derivation for the model:

	Leaded	Leadless
Beta Range	1.15-6.8	2.2-4.0
Beta Average	3.42	3.68
Beta (Model)	1.15	2.2

Based on the literature data, the range and average values were developed. To maintain a conservative value for the model, the minimum value within the range was selected. Applying the correction factor to the regression data resulted in the characteristic life values for the baseline 16 pin models shown in Table 3.6.3-1. Additional characteristic life data is provided in Appendix C.

3.7 ADDITIONAL ADJUSTMENT FACTORS

The model basis to this point was derived from a fixed set of conditions which resulted in a defined cycles to failure. Because we wanted the model to address additional design variables, the model has to accommodate this. The predominant effects controllable in design are package size/pin count, lead style, height off the circuit board and different coefficients of thermal expansions due to different printed wiring boards materials. The regression equations are based on the 16 pin models only. Therefore, to account for variations in the design, additional factors are used as multipliers to the characteristic life.

The method to adjust the characteristic life was to be based on ratio's of FEA calculated cycles to failure for various factors varied one at a time. The factors include the coefficient of expansion of different board materials, the effects of various SMT package size (pin counts), the effect of standoff height of a SMT joint.

The FEA analysis effort was not extensive enough to characterize each effect individually. The limited data was used to develop multipliers for package size. Therefore an alternate approach was used based on literature relationships published by Engelmaier.[70,74,75] He developed an equation for cycles to failure based on the parameters described above. The two equations which provided the basis for the model are shown in equation 3.7-1 for leadless SMT packages and equation 3.7-2 for leaded. The exponent of the equation is given in Equation 3.7-3.

$$N_f = 1/2 \left[(F/2\varepsilon'_f) (L_D \Delta\alpha \Delta T/h) \right]^{1/c} \qquad \textbf{(Equation 3.7-1)}$$

$$N_f = 1/2 \left[(F/2\varepsilon'_f) (K/200Ah) (L_D \Delta\alpha \Delta T)^2 \right]^{1/c} \qquad \textbf{(Equation 3.7-2)}$$

Where:

N_f is mean cycles to failure
F is an empirical factor for non-modelable second order failure modes
ε'_f is the fatigue ductility coefficient (approximately 0.325 for SN63 solder)
L_D is the length of the SMT device package
$\Delta\alpha$ is the CTE mismatch of the SMT device and PWB material
ΔT is the temperature delta in °C
h is the standoff height of the solder joint
C is the slope of the strain curve
K is the diagonal lead stiffness constant
A is the joint area

$$C = -0.442 - 6E4\ T_{SJ} + 1.74 \times 10^{\ln(1+360/t)} \qquad \textbf{(Equation 3.7-3)}$$

Where:

T_{SJ} is the average joint temperature
t is the dwell time

These equations are an extension of the Coffin-Mansion equations[55,75]. The slope, C, was found by Engelmaier to vary with the mean solder joint temperature and dwell time but was approximately .5 to .7. A value of .64 was derived from test results.[75] For purposes of the following a value of .65 was selected. The .65 value represents the highest strain to life sensitivity, therefore providing the most conservative cycle life estimates.

3.7.1 PACKAGE SIZE ADJUSTMENT FACTOR, A

The regression equations used to calculate the mean cycles to failure were developed in Section 3 and are based on 16 pin package sizes. A factor is needed to account for large package sizes. The package factor, A, accounts for these different package size and pin counts. This factor can be derived by comparing life predictions for the different package/pin counts for the same lead styles. Base on the physics of strain, the strain value for any package is related to the diagonal distance from the center of the package. As the package size increases so does the strain for a given lead pitch. Therefore, this factor is a multiplier of the FEA baseline diagonal distance. A limited number of FEA results are available to test this concept.

The relationship of package size to cycles to failure can be derived from Equations 3.7-1 and

3.7-2. In these formulas, L_D is the package size. As the package size increases, the strain, which is represented by F, ΔT, $\Delta\alpha$, h, increases and reduces the cycle life in a power law relationship. A limited number of data points from the FEA data was used to ratio the results and to postulate a model. Based on the model baseline of a 16 pin package, larger packages will thus have a multiplicative effect on the cycle life. From Equation 3.7-1 and 3.7-2:

For Leadless Devices: $N_f \alpha 1/L_D^c$

For Leaded Devices: $N_f \alpha 1/(L_D^2)^c$

This factor is shown below. A table of different factor values for leadless, gull wing, J and S type lead styles was derived. The results are shown in table 3.7-1.

For Leadless Devices: **A = (.212/Ld)** **(Equation 3.7.1-1)**

For Leaded Devices: **A = (.424/Ld)** **(Equation 3.7.1-2)**

Where Ld is the diagonal length in inches

Table 3.7.1-1 Package Size Factor A

Adjustment for Package Size Referenced to Pin Count

Number Of Pins	Leadless	Leaded
10	X	
14	X	
16	1.00	1.00
18	0.46	0.91
20	0.43	0.82
24	0.37	0.74
28	0.33	0.65
32	0.30	0.59
44	0.23	0.46
68	0.16	0.31
84	0.13	0.26

A comparison of the model to FEA runs is shown in Table 3.7.1-2 and indicates that the model is conservative. The ratios from the FEA are the ratios of the cycles to failure for the large package size (defined by pin count) to the reference 16 pin FEA results.

Table 3.7.1-2 Comparison of Package Factor A with FEA Results

Number Of Pins	Eq. 3.7.1-1 Leadless	Per FEA Leadless	Eq. 3.7.1-2 Leaded	Per FEA Leaded
16	1.00	1.0	1.00	1.00
24	0.37	0.45	0.74	N/A
32	0.30	0.30	0.59	0.70
68	0.16	0.09	0.31	N/A

3.7.2 STANDOFF HEIGHT FACTOR, B

The standoff height factor, B, provides for the effects of higher standoff height on thermal cycle life. This effect is well established in the literature, especially for leadless devices.[80] The approach used was based on existing relationships. Another approach would have been to conduct a series of FEA assessments addressing different heights, calculating cycle life and developing regression based equations based on the FEA results. Sufficient FEA data was not available to utilize this approach.

The approach used was derived from work by Engelmaier. The relationship of standoff height to cycle life from equation 3.7-1 and 3.7-2 show that the standoff height is directly related to the cycle life. The larger the standoff height, the higher the cycle life. Based on the models use of a reference height of 3 mils for a 16 pin package, higher standoff heights will thus have a multiplicative effect on the cycle life. From 3.7-1 and 3.7-2:

For Leadless Devices: $N_f \alpha h^c$

For Leaded Devices: $N_f \alpha h^c/k$

Where k is the lead compliance. For the model development, k=1.
The results are tabulated in table 3.7.2-1:

For Leadless Devices: $B = (h/0.003)^{1.54}$ **(Equation 3.7.2-1)**

For Leaded Devices: $B = (h/0.003)^{2.37}$ **(Equation 3.7.2-2)**

Where h is the is the height of the solder joint off the PWB in inches.

Table 3.7.2-1 Height Factor, B
Adjustment for Solder Joint Height off the PWB

Height Times 0.001 inches	Leadless Factor	Leaded Factor
3	1.0	1.0
4	1.6	2.0
5	2.2	3.4
6	2.9	5.2
7	3.7	7.4
8	4.5	10.2
9	5.4	13.5
10	6.3	17.3

3.7.3 COEFFICIENT OF EXPANSION MISMATCH FACTOR, C

The coefficient of thermal expansion factor, C, accounts for the effect of the difference in Coefficient of Thermal Expansion (CTE) mismatch between the part and the printed wiring board material. This factor addresses only the more commonly used printed wiring board material CTE values with G-10/FR-4 being the baseline used in the FEA.

The coefficient of expansion is a basic material property. The strain in the solder joint is a function of the degree of mismatch between the board material and the part package material. The standard part package material is alumina, Al_2O_3, with a typical CTE of 6.5 ppm/°C. The board material CTE typical values are shown in Table 3.7.3-1.

The relationship of the CTE to cycle life from Equations 3.7-1 and 3.7-2 show that the CTE is inversely related to the cycle life. The larger the CTE difference, the lower the cycle life. Based on the models use of a reference CTE difference between an FR-4 PWB and ceramic SMT device packages of 10ppm/°C, the lower the CTE mismatch will have a multiplicative effect on the cycle life. From Equations 3.7-1 and 3.7-2:

For Leadless Devices: $N_f \propto 1/(\Delta\alpha)^c$

For Leaded Devices: $N_f \alpha 1/((\Delta\alpha)^2)^c$

The factor form is shown in equations 3.7.3-1. This factor could also be derived from FEA results by conducting analysis with different material CTE mismatch parameters used. The ratio of the calculated life could then be developed. The data for this approach was not available.

For Leadless Devices: $C = (10/\Delta CTE)^{1.54}$ **(Equation 3.7.3-1)**

For Leaded Devices: $C = (10/\Delta CTE)^{2.37}$ **(Equation 3.7.3-2)**

C = Correction factor for CTE mismatch

ΔCTE = the CTE mismatch of the PWB material used to the IC ceramic (Al_2O_3) ppm/°C

10 = the reference mismatch based on FR-4 E/G PWB material

Table 3.7.3-1 CTE Factor, C

Adjustment for CTE mismatch between a device body and the PWB

PWB Material	CTE (ppm/°C)	Δ CTE Mismatch	C Factor Leadless	C Factor Leaded
G-10 or FR-4	16	10	1.0	1.0
Polyimide Kevlar	8	2	11.9	45.3
Epoxy CIC*	6.4	1	34.7	234.0
Epoxy Kevlar	8	2	11.9	45.3

Based on CTE difference between PWB material and Alumina Al_2O_3 - 6.0 ppm/°C

* CIC - Copper/Invar/Copper

3.7.4 QUALITY FACTOR

A factor for Quality is considered necessary to account for life reduction effects due to quality of the processes used to produce the joint. This approach could not provide a fixed factor to account for the quality controls. This factor has to be defined subjectively at this time. The quality factor was originally expected to incorporate effects of different soldering approaches such as vapor phase, Infra Red (IR) or wave soldering and the levels of process control

incorporated. This approach could not be evaluated due to lack of literature on this subject. Therefore, the approach was to utilize a two level factor; one for MIL-quality and one for non-military. The levels for this factor were based on the existing MIL-HDBK-217 quality factors used for solder connections.

Table 3.7.4-1 Quality Factor, Pie Q

Mil Level	Pie Q Factor
Military	1.0
Non-military	2.0

3.8 PACKAGE PINS FACTOR, P

The SMT model derived above is based on the development of a failure rate for a single joint. The joint used in the FEA is the end lead of the SMT package. In a symmetrical package there are eight leads which have the same stress due to the symmetry. The modeling approach also described the distribution aspects of the cycles to failure. Using statistical probability distribution assumptions, a SMT package will fail if any of the joints fail. With eight equally probable places to fail the probability of failure is the product of the probability of each joint failing. Because a constant failure rate assumption is used, the failure rate for a package is therefore the sum of each individual joint failure rate. The model multiplies the single joint failure rate by eight to account for this effect.

While each SMT package has more than eight pins, the stress in lead/joints closer to the center of the device is less than the outer leads/joint. This is shown in the empirical equations developed by Engelmaier (equations 3.7-1 and -2). Therefore, the inner leads on an SMT package are assumed to have no effect on the failure rate.

3.9 TRANSLATION OF CYCLES TO TIME BASE

The SMT solder joint model must also be translated to a time based failure rate for use in MIL-HDBK-217. This translation is necessary as the basic FEA produces a mean cycles to failure number. The Weibull model generates a failures per cycle result. To translate this to

failures per hour, the failures per cycle is multiplied by cycles per hour. This is determined from the expected use cycles and total life use hours which was defined in the environmental definition effort described above. For use in 217, the typical values are related to the environmental categories and are put in the table. A final conversion factor is required to translate the above result to failures per million hours, the standard time used in all 217 failure rates. This is accomplished by multiplying the result by 10^6. This completes the translation factor resulting in a failure rate based on failures per million hours.

U - Cycle Rate:

$$U = N_u/t \ X \ 10^6 \text{ per } 10^6 \text{ hours} \qquad \textbf{(Equation 3.9-1)}$$

Where: U - Cycle Rate in cycles per hour

N_u - Use Cycles (No. of thermal cycles over life use)

t - Use - Operating Life in hours

3.10 MODEL VERIFICATION

Validation of the model developed for the SMT is difficult and has to start with the validation of the Finite Element analysis and Coffin-Manson equation. FEA and the Coffin-Manson relationships have been verified in the literature. Test data to verify the life cycles calculated with these models have generally been through highly accelerated tests above 100°C temperature excursions. The test data used for verification data is therefore non existent for much lower thermal cycle level which are characteristic of the typical ranges predicted by the model. Therefore, the model must be considered a first degree order of magnitude relationship.

Another problem with available test results is the wide diversity in test conditions such as solder type, board material CTE variations, unknown/unquantified characteristics of materials such as CTE temperature dependence. All of these factors result in large differences in published data for seemingly the same general test conditions. Additional complexity arises due to various soldering process techniques.

Field data results on solder joint reliability is likewise non existent to the level of detail needed

to generate the SMT reliability model. The use of large package sizes has been relatively recent which limits any model verification from field data.

The best available validation method for the model is to compare the model mean cycles to failure to the available test data. Test data with all parameters identical to the model is also sketchy. Table 3.10-1 provides a comparison of FEA data to test cycles. This data shows the FEA generally predicts less than the test results. This factor, maintaining a conservative cycle life, was continued in the SMT model. The objective was to maintain a conservative estimate for failure rate.

One additional criteria was used as a check on the relative magnitude of the model derived failure rate. The results of the model calculations were compared to the present model method/results using MIL-HDBK-217F. The results are shown in Table 3.10-2. The comparison shows that the existing MIL-HDBK-217F solder failure rates are of the same relative magnitude for LCC devices at 30 degree ΔT and 16 pin devices only. The MIL-HDBK-217F models are not sensitive to temperature levels, are not sensitive to package size and do not correlate to the leaded device failure rates calculated by the model developed herein.

The verification of the model should be pursued through designed experiments. The author believes that despite the lack of extensive verification, the modeling approach based on deterministic physical laws are adequate for this first generation SMT model.

Table 3.10-1 Comparison of the Number of Cycles to Failure As Predicted by FEA to Test Data
(All data is for LCC's on glass reinforced PWB's)

Pin Count	Test Cycles to Failure Range	Test Cycles to Failure Mean	FEA Cycles to Failure	Temp. Range	Comments:
20	250	250	495	-55°C/+105°C	Only 1 data point available.
20	60-650	355	270	-55°C/+125°C	
28	100-400	250	140	" "	
44	40-225	132	77	" "	

Table 3.10-2 Failure Rate Comparison to Present MIL-HDBK-217F
Failure Rate Per 10^6 Hrs

	16 PIN 40°C ΔT	84 PIN 40°C ΔT	16 PIN 80°C ΔT	84 PIN 80°C ΔT
J LEAD(1)	7.56E-07	3.56E-06	4.13E-04	1.94E-04
S LEAD(1)	2.7E-06	1.29E-05	8.61E-04	4.06E-03
GULL LEAD(1)	5.89E-08	2.26E-07	1.11E-04	5.24E-04
LCC(1)	1.62E-06	1.45E-04	8.15E-02	7.256

MIL-HDBK-217F	Calculated Failure Rates		
Interconnect λ	.01837	.09643	(16 and 84 Pin Packages)
Reflow Connection λ	.00883	.04637	

(1) Failure Rates based on A_{uf}, 20000 cycles, 10000 hr life

3.11 Reliability Model Conclusions

The model proposed provides a traceable methodology for deriving failure rates directly from the results of finite element analysis. The validity of the model is based on the validity of the FEA method which has been shown to be assumption dependent.

The model must be used with an understanding of the basic limitations which include the following:

- The model is derived around the wear out failure mechanism of low cycle fatigue only. The vibration effects (high cycle fatigue) and effects of other environmental factors cannot be addressed per the existing MIL-HDBK-217 environment factor as the use environment is integral to the fatigue life cycle calculation.

- The effect of power cycling of the device on cyclic life is presently assumed to be included within the temperature change factor in the base cycles to failure model.

- The model does not consider corrosion, intermetallic compounds, electro-migration or

leaching type failure mechanisms.

The predicted cycles to failure from the FEA regression models shows a significant cycle life capability for all lead types including LCC style devices at lower thermal cycle range values Figure 3.5-1 and Appendix C). While the cycles to failure over the typical test cycle ranges (-54°C/+125°C) are very small. This could indicate that test conditions are overly severe for determining life use capability.

3.12 Examples Using the Developed Model

Table 3.12-1 shows examples using the method outlined in Section 3. of this report:

Table 3.12-1 Airborne Uninhabited Fighter Failure Rate Computations:

Calculate the failure rate for an Airborne, Uninhabited Application:
The SMT package is an LCC placed on a FR-4 Printed Wiring Board. The mission thermal excursion is 60 degrees (+55 to -5°C), the internal rise is 20 °C.
The LCC standoff height from the PWB is 3 mils.
The design life is 10000 hrs.
The mission use causes 2 thermal cycles per use hour: Life cycles is 20000 cycles.
The data requires use of the detailed model
The Temperature delta is 60 + 20 - 3(((55-5)/2)-25) = 80

	Delta Temp	80	80	80	80	80	80
	LCC Package Size	16	24	32	44	68	84
N_F	Characteristic Life	1.30E+06	1.30E+06	1.30E+06	1.30E+06	1.30E+06	1.30E+06
π_Q	Quality Factor	1	1	1	1	1	1
C	CTE Mismatch Factor	1	1	1	1	1	1
B	Height Factor	1	1	1	1	1	1
A	Package Size Factor	1	1	1	1	1	1
N_u	Use Cycles Over Life	20000	20000	20000	20000	20000	20000
t	Use Hrs Over Life	10000	10000	10000	10000	10000	10000
U	Cycle Rate	2	2	2	2	2	2
P	Pin Factor	8	8	8	8	8	8
Failure Rate Per 10^6 Hrs		0.0815	0.7267	1.1527	2.0681	4.5953	7.2560

3.13 Recommendations for Further Model Development

Some issues have surfaced in the development of this model which affect the results. These are defined here to elaborate on areas for further study.

1. The strain rates are dependent on the thermal cycle defined in the FEA. For the analysis, the cycle is based on a 25°C start, decreased to cold temperature, increased to the maximum temperature and then reduced to 25°C. In use, starting conditions include temperature ranges from 55°C to -40°C. The temperature change direction is also use dependent with aircraft typically seeing temperature decrease due to altitude effects whereas ground and mobile environments will usually see increase temperature. The effects are not known. In addition the prolonged dwell times at low temperature points has an effect on the cycle life capability which is not addressed by the model.

2. The effects of different solder types is not considered. The baseline is Sn63/Pb37 solder. Additional FEA with different solders could improve model resolution. The modeling approach defined herein provides a direct link between physical design parameters and materials to failure rate. This differs significantly from field history statistics regression models used in the past, and provides a methodology for new technology reliability prediction. Further work to develop this approach to other reliability modeling should be investigated.

4.0 TESTING METHODS

Paragraph 4.1.4 of the Statement of Work asks to evaluate specified test methods and criteria of surface mount technology, to determine the appropriateness of the tests and the accuracy of the test conclusions. The tests include: temperature cycling; mechanical shock; vibration; constant acceleration; power cycling; and thermal impedance Θ_{JC} testing. The following paragraphs address all of the factors related to the various test regimes, and how they correlate to actual use conditions. Recommendations for improved testing procedures for SMD screening and qualification are made, as applicable.

4.1. THERMAL CYCLE TESTING

The most controversial test among industry and government SMT experts is the thermal cycle test criteria. The present qualification requirements for SMT are based on MIL-STD-883, Method 1010. This test method is required for individual microelectronic components to meet MIL-M-38510, the microelectronic component specification, and is conducted to determine the resistance of a part to cyclic exposures of high and low temperatures. This testing scenario is carried over to the assembly level for SMT. The test condition within Method 1010 that is specified is Test Condition B, which requires temperature excursions from -55°C to +125°C. The test requirement does not require a soak at either temperature extreme. It states that the chamber shall be at the high or low temperature extreme for at least ten minutes, and the total time shall be sufficient to allow the total mass of each device to reach the specified temperature. Once all devices have reached the specified temperature, the test temperature is reversed. It is the temperature range and the soak time that are of issue.

The temperature range of -55°C to +125°C is used with the assumption that it represents the worst case conditions that a piece of hardware will encounter. The reasoning has been, ". . .if the hardware can withstand these accelerated conditions, then it can withstand any actual use conditions." This may not actually be the case. For standard eutectic and near eutectic Sn/Pb, alloys, the physical properties change dramatically over about 100°C. Once above this temperature, the solder no longer reacts as it would in actual use conditions. Above 100°C, Sn/Pb solders enter a material phase condition that is seldom, if ever encountered in actual field use. Also, the glass transition temperature of most standard PWB materials is about 100°C, causing the substrate to change material characteristics at these temperatures. By using such a high temperature extreme, we may be inducing additional stresses into the solder that causes early failure. Perhaps a lower maximum temperature, below 100°C, would improve the situation.

The Advanced Data/Signal Processing (VHSIC) MANTECH[80] study showed that using a maximum temperature of 95°C caused failures earlier, in one case, than at 125°C. There was no certain explanation as to the reason for this occurrence. It was assumed that the lower temperature would cause less failures in all cases. However, that was not the case.

Statistically, there is little difference between the Mantech results of -55°C/+125°C and -55°C/+95°C testing for the Quatrex/Quartz/CIC assemblies, which causes even more confusion (See Figure 4.1-1). This data shows that solder joint geometry and materials used in the assembly can override the effect of decreasing temperature ranges.

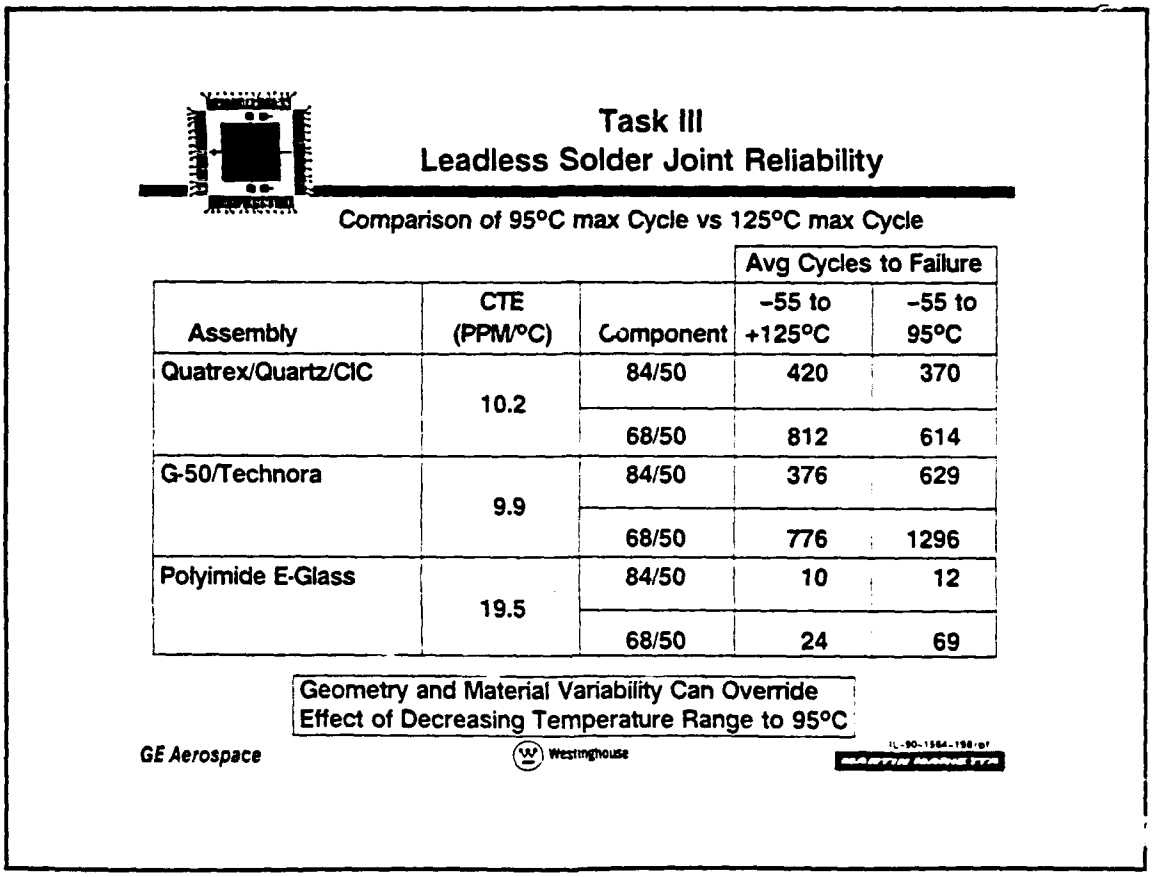

Figure 4.1-1 Mantech[80] Comparison of 95°C Max Cycle to 125°C Max Cycle

The previous paragraph discussed the impact of high temperature extremes on solder joint life. The other concern is the actual delta range of the temperature extremes. It was shown in the MANTECH study that a delta of 180°C (-55°C/+125°C) and a delta 150°C (-55°C/+95°C) temperature range were statistically similar. Modelling performed by HARRIS during the SMT Reliability Study shows a dramatic increase in cycles to failure (CTF) by lowering the delta T to below 100°C. Delta's less than 100°C proved to be significant, with typical cycles to failure predicted to be over 1,000,000 for 16, 24, and 32 pin LCC's on glass/epoxy boards. Further

HARRIS modelling, using different upper and lower temperatures for the same delta range (40°C) proved, again, that the higher temperature ranges induced more damage. This was shown with FEA models using -55°C/-15°C and +20°C/+60°C temperature extremes. The +20°C/+60°C range caused first failures to occur (predicted) at $1.7x10^4$ cycles for a 32 pin LCC. The lower temperature range predicted CTF was $5.1x10^6$ cycles for the same device. This is a significant finding when one considers the probabilities of equipment operating in those temperature ranges. It is believed that the creep phenomena is the primary contributor to this occurrence, as creep becomes the dominating factor above 30-35°C. Although the stated CTF numbers are extremely high, they represent the concern over of the different temperature ranges. It has been perceived that the exact starting temperature for any low delta Temperature range would give equal results. This is not the case, which throws in another factor to be considered in determining a suitable test cycle range and temperature. More FEA studies using constant deltas at various starting temperatures will clear up this issue.

A third aspect of the test criteria that has been evaluated is the dwell time at the extreme temperatures. Again, the criteria is based on a perception of what is happening at the temperature extremes. Past dictum stated that to insure an adequate load is being subjected to the solder joints, the temperature must remain constant for an adequate period of time. Typically, the chamber stayed at temperature to allow all of the devices and materials to reach the test temperature, either -55°C or +125°C. Then the chamber was allowed to dwell to allow as much strain damage as possible to be induced. This was often 10 to 30 minutes, as reported by various industry studies. Thermal analysis using finite element modelling has shown creep to be the primary contributor to solder strain above about +30°C or +35°C. Once the temperature has stabilized at anything above this temperature, strain relaxation takes only seconds to reach a point where further significant strain damage no longer occurs. FEA has also shown in detail, that various durations and temperatures above this range result in the same strain relaxation occurring within the first few minutes of reaching the set temperature. After this time, the curve approaches an asymptote, showing minimal change (Figure 4.1-2).

Therefore, long duration runs are not necessary, as most of the creep strain has occurred within the first few minutes, and any additional time spent at temperature will not change the

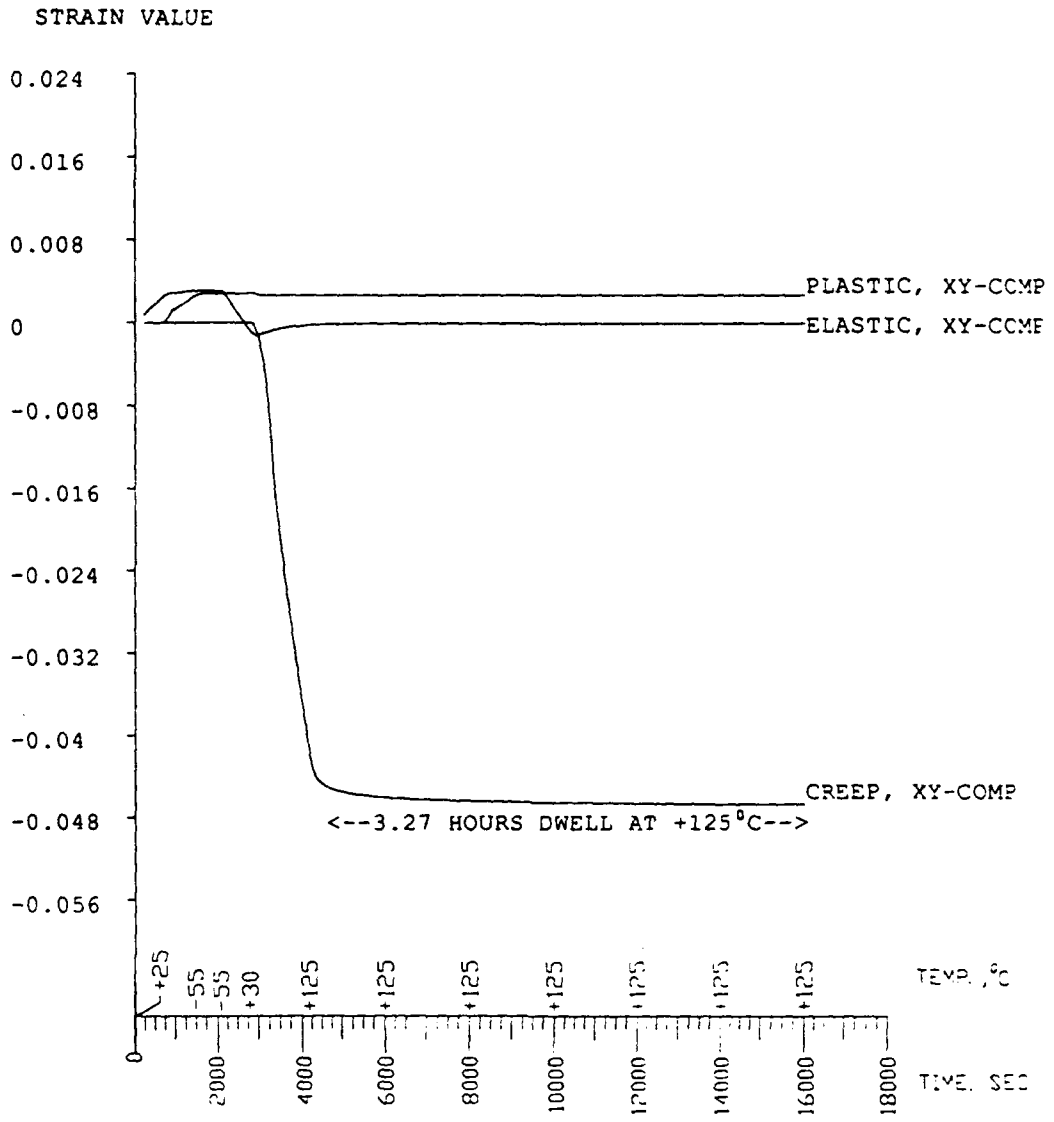

Figure 4.1-2 Strain Diagram Showing Effects of Prolonged Temperature Extreme Dwell Time

data enough to be noticed. Additionally, dwell contributes to creep strain and there is no appreciable creep at low temperatures, there is no need for dwell at low temperatures. Changes in the molecular structure during prolonged (days) dwells at these temperatures may be another factor contributing to the failure of the solder joints, but evaluation of this phenomena is out of the scope of this project.

Finally, one aspect of thermal cycling that came out during the modelling, but requires further study, is the direction taken when starting the thermal cycle. It was theorized that beginning

at room temperature, going to the high temperature extreme initially is more detrimental than first going to the cold temperature extreme. The number of cycles to failure would be higher by a significant factor by going to the lower temperature first. This was noticed in some simple models, but was out of the scope of this project to study further. The theory has been modified to assume that the larger temperature delta from the device ambient (i.e. room temp.), whether it be positive or negative degrees, is the cause for this condition. For example, an excursion from a room temperature of +25°C to +125°C (delta of 100°C), is more severe than from +25°C to -55°C (delta of 80°C). Conversely, an excursion from an ambient of +40°C to -55°C (delta of 95°C) may be more severe than going from +40°C to +100°C (delta of 60°C). This scenario poses interesting questions, but must be further evaluated to clarify what actually happens, if anything. Additional testing or FEA is required.

4.1.1 THERMAL CYCLING SUMMARY

Unfortunately, this discussion has not clarified the thermal cycle testing question of whether the practiced method (MIL-STD 883, Method 1010) is acceptable for simulating actual use conditions. The general industry consensus is that it is not. The most accurate solution is to run actual use conditions with actual use durations. Obviously, this is not a practical solution. The use of the high temperatures, where solder begins to behave differently than in actual use conditions, is also not a desired practice. The solution seems to be in addressing the actual use conditions of a given piece of hardware, and determining the test requirements for that environment. A single test regime blanketing all applications is surely desirable, but not practical for surface mount technology. Conversely, because a particular technology cannot stand up to the test conditions, does not mean that the test is wrong. Perhaps an alternative is not to reach 1000 cycles at -55°C/+125°C, but to reach a certain number of cycles based on the application and end use environment. An LCC that fails at less than 100 cycles of -55°C/+125°C testing may, in fact, survive the entire life of a fielded unit in a ground-based controlled atmosphere environment, and then some. Additional study is needed to correlate actual use conditions to the required test criteria for thermal cycling. Continued monitoring of actual field failure data, too, will add credence to the predicted values for surface mounted devices. Additional field failure data will help to fine tune the curves used to predict expected life.

Limiting the upper temperature to +95°C or +105°C will reduce the possibility of introducing non-related failure modes due to unrealistic solder phase changes or the effects of substrate glass transition effects. Should the upper temperature be +95°C or +105°C? This is subject to much debate as the phase change temperatures vary. It is recommended that the more conservative +95°C temperature be adopted.

It is further suggest that the 1000 cycles be prorated to a lower value per the specific mission/application. Inspection of Table 3.4-1 will aid in determining how much to prorate. More FEA runs at various low temperatures with small delta temperatures would greatly simplify that task.

4.2 TESTING SUMMARY

As mentioned in the opening paragraph of this section, additional test procedures were to be evaluated. Due to the extensive effort required to perform the finite element modelling and correlation of the thermal cycling test data, these tests were not evaluated using FEA. However, from the literature review and in-house experience, it is not apparent that these tests are a significant cause for concern. They are, in most cases, second order effects whereas thermal cycling is the first order effect. The only possible exception to this is shock and vibration.

The mechanical shock and vibration environments conditions are typically easier to predict in accelerated test conditions than thermal cycling. At this time, the principal investigators do not see a need to change any of the test requirements for these mechanical environmental conditions. It should be emphasized, however, that the test criteria utilized should reflect the intended actual use conditions of the particular unit under test and that the use of these standard tests should not be for absolute acceptance. The effects of shock and vibration on a given part is very dependent on the assembly transmissibility and its exact location on a PWB. These factors must be considered in defining any pass/fail qualification test. To summarize, the current qualification tests should be used for a point of departure only. No general specification will work for shock and vibration.

5.0 FIELD FAILURE DATA

Probably the best source of failure data would be data directly from actual use conditions. Actual use failures could be analyzed based on the true number of missions under known conditions. Determination could be made as to whether the cause was component, design or solder joint/process related. This source of this data was not readily known, so, a search was made.

An investigation was made into various Defense Department sources to determine where such data was readily available. Also, results of an Industry/ Government working group (MIL-STD-2000 Industry Working Group) which was performing an actual field study was evaluated as well as a survey of the Defense Technical Information Catalog (DTIC) computerized data base.

5.1 DOD SOURCE INVESTIGATION

From this investigation, it is apparent that no military organization routinely collects maintenance failure data on SMD solder joint reliability. The Air Force has an extensive Maintenance Data Collection (MDC) system administered under Air Force Regulation 66-1. This system is limited to base level and failures are not normally isolated below the printed wiring assembly (PWA) level. PWA's are typically beyond base level maintenance and are generally sent to the cognizant depot repair facilities for repair. At these depots, it is possible, but usually unlikely, for a solder joint to be noted as the cause of the failure for an individual PWA.

At the depot repair lines, faulty PWA's are received from the field for repair. First, the PWA is bench-checked with the appropriate Automated Test Equipment (ATE). The ATE typically fault isolates to an ambiguous group of six or less components. These components are then removed and replaced, usually at random, until the system is operable or, it is determined that the system is beyond repair. The repaired system is returned to stock and to the field as required.

It is an anomaly that nowhere in this process is faulty soldering identified. A faulty solder joint which caused a component to fail or become intermittent may be completely overlooked in the repair technicians effort to trouble shoot a board. The failure is usually assumed to be a faulty component and it is replaced. X-ray, dye penetrant and electrical continuity tests are all available to test solder integrity, if needed, but these tests are not used for routine screening of units pending repair. To test for joint problems, these tests would have to occur before components are removed. Also, the testing problem is exacerbated by the requirement to remove the conformal coating from the connection. If the coating removal process is mechanical, this act alone could affect the analysis and skew the results. In short, solder is not tested because it is difficult, impractical and because no routine failure data collection system demands it.

The following are some of the sources HARRIS personnel interviewed for information on field reliability data:

Mr. Kip Hoffer, Naval Weapons Support Facility, Crane IN.; Mr. Hoffer was unaware of any formal body of collected data at NWSF.

Vernon Jauer, Division Chief, SAALC/MAI, San Antonio Air Logistics Center, Kelly AFB, TX.; no data nor any ongoing method of collecting such data without a special study commissioned.

Warner Robins Air Logistics Center, Robins AFB, GA.; Brent Baumgartner, Reliability Engineer, WRALC/MAIESB, Phil Ramsey, Reliability Engineer, WRALC/MAIESB, Shelbey Jennings, Production Engineer, WRALC/MAIESB, Tom Dills, Maintenance Production, Supervisor, WRALC/MAIP, Jimmy Howell, Maintenance Branch Chief, WRALC/MAIP, Don Hise, Reliability Engineer, WRALC/MAIESB; No standard method currently exists at WRALC to identify and document solder joint failures. WRALC would like to collaborate with Harris in such a study. Mr. Baumgartner has invited us to join him in reviewing the informal data base maintained by their failure analysis section and by their maintenance production lines.

Ogden Air Logistics Center, Hill AFB, UT., Matthew Kalaidis, Maintenance Production Supervisor, OOALC/MAKPI, Robert Whitlock, Reliability and Failure Analysis Center, Supervisor, OOALC/MAKERT; No standard mechanism to identify solder joint failures of incoming PWA's.

George Selenski, Wright Research and Development Center, Aerospace Systems Division, Air Force Systems Command, Wright-Patterson AFB, OH; Mr. Slenski was unaware of any solder reliability studies, but promised to investigate.

Don Hall, Logistics Engineer, DASD(S)CALS, Headquarters, Department of Defense, Deputy for Maintainability, Reliability and Logistics, Washington, D.C.; reply pending.

Mr. Jon Maki, Lead Engineer - Quality, Harris Corp., FL.; Mr. Maki is a former employee of the Electronics Manufacturing Productivity Facility (EMPF) located in China Lake, CA. Mr. Maki was co-chair and co-author of the MIL-STD-2000 Industry Working Group Field Reliability Study.

5.2 MIL-STD-2000 INDUSTRY WORKING GROUP STUDY

While employed at the Navy's Electronic Manufacturing Productivity Facility (EMPF) in China Lake, California, Mr. Jon Maki was involved in the areas of automated inspection and solder joint reliability. He also served as Co-chairman of a Tri-Services study to examine the correlation between workmanship criteria and field failures, primarily on through-hole technology boards.

Mr. Maki states that gathering documentation on solder joints causing failures on military equipment is extremely difficult. Publications periodically occur discussing failure mechanisms, but they usually address only the failure mode, not frequency or time frame of occurrence. He states that, from his observations, most solder joint failures are due to improper design and process control, not visual quality attributes.

The primary problem with obtaining military field failure data, is that failure analysis

documentation only goes to the component level. If a solder joint did cause a failure, it may simply be repaired with no documentation. In general, solder joints are not documented unless it is a blatant problem.

When data on solder joint failures is found, it must be thoroughly scrutinized. Solder joints are frequently blamed for intermittents even though the mechanical and electrical integrity of the solder joint is there. Frequently, technicians call these "cold" solder joints because they are not working "electrically."

Results of the Tri-Services Field Reliability Study, as well as investigations by AFWAL and RADC confirm the problem of a lack of field reliability data on solder joints. Typically, component failure mechanisms during failure analysis are determined by best engineering judgment because detailed failure analysis is costly and rarely performed. Failure analysis typically does not occur unless the failure occurs frequently. Under military requirements, determining the cause of failure is not as critical as getting the equipment operational and back in service.

The AFWAL report, "Latent Defect Life Model and Data", states; "....solder joint failures are rarely recorded. Second, some of the part failures that are recorded are actually caused by solder joint failures. Third, those recorded failed solder joints are rarely associated with the causing defect. With this kind of information, field failure data on solder joints are misleading and of little use for reports that are intended to locate types of defects which cause field failures."

A report by Capt. Thomas Green, RADC, "Getting the Facts from the Field... Real World Failure Data Collection and Analysis", GOMAC, 1987, came to similar conclusions. Capt. Green reiterates that no sufficient data base exists within the DOD or the five major repair depots. Some replacement is performed in the field shops and no data entries are used to identify the component, thus preventing traceability of the part failure. Another concern is that there is no proof of the part actually failing.

We encourage a review of the Tri-Services IWG Field Reliability Study. Although primarily a

workmanship related document, the study touches upon;

- repair practices in the field
- lack of solder joint failure documentation
- solder joint failure mechanisms
- solder joint field failures
- lack of training and background of repair personnel for determining solder joint failures

Also, find attached (Appendix E) a copy of a letter from Jon Maki to Jerry Rosser, Co-Chairman of the Tri-Services Industry Working Group, discussing solder joint reliability.

Other literature obtained during the study:

"F-111 Mark II Avionics SRU Cracked Solder Problem," Ogden, Utah, Meeting Minutes, 9 Aug. 1977.

Failed field units were evaluated for the ability to repair cracked solder joints by reflowing them on a wave solder machine. Of the 64% failed units, 50% were repaired simply by reflowing the solder. Fourteen percent required replacement of components. No indication to the cause of the cracked solder joints was given in the report, but, it is suspected to be a design problem due to the gross amount of failures.

"Analysis of the F/A-18 Hornet Flight Control Computer Field Mean Time Between Failures," P. Griffin, General Electric Binghamton, Proceeding of the 1985 Annual Reliability and Maintainability Symposium, Philadelphia, PA, Jan. 1985.

Distribution of F/A-18 Hornet Flight Control Computer Failures:

38%	PWB/solder joints; smear problem on PWB's
23%	Integrated Circuits
11%	Resistors
10%	Semiconductors other than IC's
6%	Capacitors
2%	Connectors
12%	Other

"Culprits Causing Avionic Equipment Failures," Kam L. Wong, Irving Quart, Jim Kallis, Alan H. Burkhard, 1987 Proceedings, Annual Reliability and Maintainability Symposium, 0149-114x/87/0000-0416.

Distribution of failures: (Composite of 4 programs)

22%	Integrated Circuits
12%	Transistors
10%	Hybrid
10%	Capacitors
10%	Resistors
7%	Diodes
2%	Solder joints
27%	Other

"Report of the Fleet Hardware Assessment Project - A Survey of Soldering Problems Observed in Navy Weapons Systems," Daniel A Fazekas, 11th Annual Electronics Manufacturing Seminar Proceedings, NWC TP 6789, 18-20 Feb. 1987.

Percent of Defects Observed (not failures):

62%	Solder Connection - Moderate Risk
13%	Component and mounting defects - Moderate Risk
9%	Printed Wiring Board Defects
8%	Component and Mounting defects - High Risk
6%	Solder Connection - High Risk
2%	Other Defects

This data indicated that solder joints were not the primary cause of field failures and that, in general, the majority of failures were component or design related.

6.0 FINITE ELEMENT ANALYSIS

In order to define the load steps in the ANSYS finite element analysis the first task was to come up with Time-Temperature profile for thermal cycling of the surface mounted IC device. MIL-STD-883 has guidelines as follows:

Temperature Cycling: -55^{0}C to +125^{0}C (Typically 1000 Cycles) Method 1010.

Thermal Shock: -55^{0}C to +125^{0}C (Typically 15 Cycles), Method 1011.

Mechanical Shock: Minimum 1500g , Method 2002.

Vibration: 60 Hz; 4 hours; X,Y,Z planes with a peak acceleration of 20g, Method 2005.

Constant Acceleration: 5000g minimum, Method 2001.

Power Cycle: Operate device at full rated power while holding substrate at ambient temperature (number of cycles based on system power on/off projection).

Based on in-house thermal cycling test profiles on various programs and also from other industry sources (Westinghouse, Hughes Aircraft etc.), thermal cycling profiles for six temperature ranges -55°C/+125°C, -55°C/+105°C, -55°C/+85°C, -30°C/+50°C, -15°C/-55°C and +20°C/+60°C have been formulated. MIL-STD-883 does not exactly specify any of these temperature cycling profiles. The rationale of selecting these profiles are based on standard industry practice of thermal cycling and actual use conditions. It should be noted, however, that these profiles are for the thermal chamber and not for the components. The dwell time for the thermal chamber ranges from 10 minutes to 30 minutes at the two extreme temperatures of each temperature range. Temperature gradient is usually between 5°C/minute and 10°C/minute. We have selected a dwell time of 10 minutes for the components at the two extreme temperatures.

Appendix D provides the reader with a full understanding of the FEA effort on this project. The results of the FEA are tabulated in Table 3.4-1.

6.1 GEOMETRY

Pad and device geometries were taken from the design guideline, Appendix A. The most sensitive dimension is the LCC standoff height above the PWB. 0.003 inches was used as it is typical of standard solder reflow processes.

6.2 LEADLESS CERAMIC CHIP CARRIER (LCCC)

The package dimensions were taken from Kyocera catalog no. CAT/3.2T8901THA/ 1031E and MIL-M-38510H. Some dimensions have been adjusted to represent a square package. For a square package, there is a 1/8th symmetry and therefore modelling time and the cost is reduced. Ceramic is the only chip carrier material that was considered.

6.3 LEADED SMT DEVICE PACKAGES

Actual package size was based on the corresponding LCC package size. Lead geometry variations were the varying factor.

6.4 POST-PROCESSING IN ANSYS

Before discussing the ANSYS post processing capabilities it will be easier to understand if some ANSYS nomenclature are explained. Solder is modelled as a STIFF 45 element. This element is a 3-D isoparametric solid. It is defined by eight nodal points having three degrees of freedom at each node. Although the ANSYS manual permits prism-shaped element by defining duplicate K and L and duplicate O and P, running the program will display a warning message like "STIFF 45. WEDGES ARE NOT RECOMMENDED."

The following are available in post processing for the STIFF 45 element:

S.I.	STRESS INTENSITY
SIGE	EQUIVALENT STRESS
SIGPR	PRINCIPAL STRESSES -- SIG1, SIG2,SIG3($\sigma1,\sigma2,\sigma3$) WHERE $\sigma1>\sigma2>\sigma3$
SIGE	EQUIVALENT STRESS = $1/\sqrt{2}[(\sigma1-\sigma2)^2+(\sigma2-\sigma3)^2+(\sigma3-\sigma1)^2]^{1/2}$
SIG	STRESS COMPONENTS -- SX,SY,SZ,SXY,SYZ,SXZ
EP	ELASTIC STRAIN COMPONENTS (EPX,EPY,EPZ,EPXY,EPYZ,EPXZ) IN THE ELEMENT COORDINATE SYSTEM.
EPPR	PRINCIPAL ELASTIC STRAINS -- EP1,EP2,EP3
EPPL	AVERAGE PLASTIC STRAINS -- X,Y,Z,XY,YZ,XZ
EPEQ	EQUIVALENT PLASTIC STRAIN
EPCR	AVERAGE CREEP STRAINS -- X,Y,Z,XY,YZ,XZ

Plasticity problems are handled by the incremental procedure which requires an iterative process. After each iteration, the load vector is modified so that the stress calculated in the next iteration approaches the stress which the material can support at that strain. Plasticity convergence occurs whenever the ratio of the plastic strain increment, $\Delta\varepsilon_{pl}$, to the elastic Strain, ε_{el}, is less than or equal to a specified criteria. In our analysis a plasticity ratio of 0.05 has been specified.

6.5 TREATMENT OF HIGH PIN COUNT DEVICES

To minimize the analysis effort for high pin count devices, the following approach would be taken:

1) Take an existing 16 I/O package and convert it to a 32 I/O package using the same body size, but with tighter pitch, reducing it from 50 mil to 25 mil. High pin count devices typically use a finer pitch, therefore this is consistent with existing designs.

2) Compare the strains in the corner leads for both models and develop a correlation.

3) Repeat 1) and 2), above, for different lead configurations.

4) Compare the strains in the corner leads for models with the same I/O count and develop a correlation.

5) Establish a confidence interval limiting extrapolation to larger I/O counts and extrapolate to that limit.

Fine pitch devices were out of the scope of this project and were not modelled, but could have been if required.

7.0 PROPERTIES OF MATERIALS

The material properties used in the FEA work is documented in the Appendix D Supplement. What is presented here are some of the issues surrounding those properties. The reader may also wish to read Section 8.1.1 concerning the fatigue issues in modelling with solder.

7.1 MECHANICAL PROPERTIES

Research was conducted to determine the cyclic stress-strain properties of 63-37 Sn-Pb eutectic solder. Many published technical papers, data books and reports were consulted. While there exists a vast amount of tensile and shear test data in the industry, cyclic test data were difficult to obtain. A Westinghouse report entitled "Hermetic Chip Carrier Compatible

Printed Wiring Board" Report No. AFWAL-TR-85-4082, was selected to obtain solder properties. Table 20, page 83 of the report gives both cyclic and monotonic yield stress and Young's Modulus of 63-37 solder at different temperatures e.g. -55°C, +24°C and +105°C. Values were selected at a strain rate of 0.002in/in/sec. This report, however, did not give plastic Tangent Modulus. This was obtained from "Mantech For Advanced Data/Signal Processing(VHSIC). The Tangent Modulus of 36.8 Kpsi at +24°C seems to be incorrect. This was then calculated from the Westinghouse report.

Data points (stress-strain curves) are available for solder at -55, +24, and +105°C in the literature. These curves clearly show the elastic-plastic regions of the solder, and the Tangent Modulus can easily be calculated from the curves. Appendix D details this development. Data at +125°C is almost non-existent. However, tensile test data at a strain rate of 0.0002mm/mm/sec. was available in a Westinghouse Report entitled "Solder Alloy Development For Electronic Chip Carrier, Report No. AFWAL-TR-88-4215. Other data for +125°C was extrapolated from the previously mentioned two reports. Yield stress and Young's Modulus are available from Ref. 21 (Solder Alloy Development for Electronic Chip Carriers, AFWAL-TR-88-4215, Nov, 1988). Due to the no-linear behavior of solder and lack of stress-strain data in the plastic range, the Tangent Modulus could not be accurately determined. The assumption made in extrapolating the Tangent Modulus is that it is decreasing at the same rate as that from +24 to +105°C. The validity of this assumption can only be established by further testing.

7.2 MECHANICAL PROPERTIES USED IN ANSYS ANALYSIS

The following room temperature (25°C) elastic properties have been used in the analysis:

	CERAMIC	SOLDER 63-37	PWB E/G	KOVAR
Young's Modulus, psi	40E+6	3.6E+6	2.5E+6	30E+6
Poison's Ratio	0.22	0.4	0.12	0.3
Coefficient of Thermal Expansion, inch/inch/°C	7.1E-6	25E-6	18E-6	3E-6
Density, Pound/in^3	0.135	0.308	0.065	0.293

7.2.1 BILINEAR KINEMATIC HARDENING DATA FOR 63-37 SOLDER USED IN ANSYS ANALYSIS

Classical Bilinear Kinematic Hardening assumes the total stress range is equal to twice the yield stress, so that Bauschinger effect is included. It is recommended for materials that obey Von Misses yield criteria (solder may not exactly obey the Von Misses criteria). The material behavior is described by a bilinear stress-strain curve starting at the origin and with positive stress and strain values. The initial slope of the curve is taken as the elastic modulus of the material. At the specified yield stress, the curve continues along the second slope defined by the tangent modulus, E_T (having same unit as elastic modulus). The tangent modulus cannot be less than zero nor greater than the elastic modulus (Appendix D).

BILINEAR KINEMATIC HARDENING DATA

FOR 63-37 SOLDER FOR ANSYS INPUT

REF. HERMETIC CHIP CARRIER COMPATIBLE PWB - Westinghouse Report No. AFWAL-TR-85-4082

All data are at Strain Rate = 0.002 in/in/sec. except as otherwise stated.

	-55° C	+24° C	+105° C	+125° C
YIELD STRESS σ_y, psi	7.3 E3	4.95 E3	2.28 E3	1.51 E3 §
YOUNG'S MOD. E, psi	3.6 E6	3.6 E6	3.48 E6	2.20 E6 §
TANGENT MOD. E_T, psi	98.4 E3 *	36.8 E3	12.3 E3 *	6.30 E6 ¶

* Ref. MANTECH FOR ADVANCED DATA/SIGNAL PROCESSING(VHSIC)

§ Ref. SOLDER ALLOY DEVELOPMENT FOR ELECTRONIC CHIP CARRIER
Report No. AFWAL-TR-88-4215 --By Westinghouse
Strain Rate = 0.0002 mm/mm/sec

¶ Extrapolated

8.0 FAILURE MODES

Based on various references,[43,44,45,46,50,51] the primary discriminating failure mechanism of SMT devices is solder joint fatigue failure caused by stresses induced by thermal cycling, power cycling and mechanical (high cycle vibration) fatigue. The strength of the solder joint is a function of the package lead configuration and geometry, printed wiring board pad geometry, process variables and solder metallurgical properties. These failure modes are not wholly independent of each other and typically interact to cause failures. Another type of failure mode, more common on leaded surface mount devices as well as in through hole devices, is induced tensile stress. This stress is independent of temperature and more so upon time and actual stress levels. Shock and low cycle vibration will have some affect on the solder joints, but the extent and the mode of degradation is vague at this time. These primary failure modes are typically able to be modeled in FEA. However, there are other factors affecting the reliability of the solder joints which are less modelable. These factors are usually process control factors which play an important role in the formation of satisfactory solder joints.

8.1 MODELABLE FAILURE MODES

These result from regular and predictable characteristics such as geometry, fatigue properties and creep properties as opposed to grain size etc.

8.1.1 FATIGUE

Fatigue in solder joints used in electronic packages is caused by thermal and power cycling. The main reason contributing to the fatigue failure of solder joints is the difference in Coefficient of Thermal Expansion (CTE) between the soldered components. Often this is referred to as "Thermal Mismatch". The reliability of electronic packages is largely a function of fatigue, creep, and fatigue-creep interaction in eutectic solder material. Among various mechanical properties of solder, fatigue, by far, has been the single most important subject to be studied and investigated in the industries, universities and research organizations.

Many research publications are available about the mechanism of fatigue failure. Following is

a compilation of published literatures on fatigue mechanism in solder alloy:

A) RESEARCH ON THE MECHANISM OF THERMAL FATIGUE IN NEAR EUTECTIC Pb-Sn SOLDERS --- J.W. Morris,Jr., D. Grivas, D.Tribula, T. Summers and D. Frear, University of California, Berkeley

Brittle intermetallic layers of Cu_3Sn and Cu_6Sn_5 are formed between the copper pad (on PWB) and the solder. The eutectic microstructure consists of parallel lamellae of Pb-rich phase in matrix of Sn. The microstructure is divided into grain-like colonies within each of which the Pb-rich lamellae are nearly parallel. These colonies are not true grains at all, since they contain two distinct phases and many distinct crystallites.

Shear strain is inhomogeneous under cyclic load above room temperature, resulting in rapid coarsening of the eutectic microstructure that concentrates the deformation in well defined bands parallel to the joint surface. Fatigue cracks propagate along the Sn-Sn grain boundaries and join across the Pb-rich region to cause ultimate failure. Failure occurs through the bulk solder unless the joint is so thin that the failure is accelerated by cracking through the intermetallic layer. The coarsening and subsequent failure is influenced more strongly by the number of cycles than the time of exposure to high temperature. Thermal fatigue in tension does not cause well-defined coarsened bands, but often leads to rapid failure through cracking of the brittle intermetallic layer.

B) GRAIN BOUNDARIES AND THE THERMAL FATIGUE OF SURFACE MOUNT SOLDER JOINTS.

--- Donald Stone and Seong-Min Lee (1990 SMART VI Conf.)

Intergranular fatigue failures might be due to oxidation of grain boundaries contacting the atmosphere during sliding. Failure is transgranular at high strain ranges and is governed by the Coffin-Manson equation; failure is intergranular at low strain ranges where Coffin-Manson exponent increases. At high frequencies, failure is transgranular and frequency insensitive. It becomes intergranular at low frequencies, and throughout an intermediate range of frequency fatigue life depends strongly on frequency. The microstructure of the

eutectic alloy is generally globular or lamellar. Lamellae grow in colonies which are distinguished by the orientations of The lamellae. Globular microstructures consists of relatively equiaxed grains of Pb dispersed in a continuous matrix of Sn. The globular microstructure is characteristic of greater supercooling than the lamellar. Fatigue cracks initiate at boundaries between colonies where boundaries intersect the surface.

There are many more excellent papers by the same and other authors on solder fatigue (See Bibliography). In general, microstructure, grain-boundary sliding, dependence on grain size, intermetallic compound, frequency of thermal cycling, stiffness of the whole assembly, amplitude of temperature cycling etc. are factors influencing solder fatigue.

8.1.1.1 FATIGUE LIFE

Our task is to correlate the strain to the number of cycles to failure using Coffin-Manson model or a Modified Coffin-Manson model. At high cyclic frequency, intragranular fatigue dominates and the failure life can be estimated by the Coffin-Manson law. Intergranular failure occurs at low frequencies because grain boundary sliding at low frequencies allow the grain boundaries to become exposed to the atmosphere, which in turn causes oxidation. In the paper titled "The Creep-Fatigue Interaction in Solders and Solder Joints" author Donald Stone proposed a mathematical model to predict the number of cycles to failure. The model is based on crack length, grain size etc. However, in ANSYS analysis we probably cannot use the model. From the combined elasto-plastic and creep analysis by ANSYS we obtain all the X, Y, Z, XY, YZ, and ZX components of plastic strain, creep strain and elastic strain separately. We will also get the principal elastic strains, equivalent plastic strain, equivalent stress etc. From these, we compute a strain range which could be used in the Coffin-Manson law (Appendix D) to get the number of cycles to failure.
The values of σ_f, ε_f, b, and c have been taken from the paper "Predicting Time-To-Failure Using Finite Element Analysis", by Gretchen A. Bivens.

The ANSYS analysis will produce the strain amplitude which could be used in the above equation to obtain the number of cycles to failure for solder joints in leadless chip carrier, gullwing, 'J', and 'S' type leaded devices.

8.1.2 CREEP

Creep in solder joints of electronics devices has been the subject of numerous studies and investigations. Our main interest, however, has been confined to the creep behavior of eutectic solder (63% Sn, 37% Pb).

Creep is the process of strain increment at a constant load. That is to say that under a certain loading condition if the load and temperature are kept constant, the strain will increase with time. Conversely, if the specimen is restrained from straining, there will be a relaxation of stress. How the creep strain is related to temperature and time has been the subject of a bulk of technical papers published by the industries, universities, and research organizations.

8.1.2.1 CREEP MECHANISM

There is no single theory that can define the total creep phenomena for eutectic solder. Besides dependance on time and temperature, creep in solder has been found to be a function of grain size (See Section 8.2.1 for further explanation of grain size and changes). The following observations/results have been compiled from different technical papers about solder creep.

(A) DEFORMATION OF Pb-Sn EUTECTIC ALLOYS AT RELATIVELY HIGH STRAIN RATE --- D. Grivas, K.L. Murty, J.W. Morris, Jr. --- Acta Metallurgica Vol. 27, pp. 731 to 737,1979

Creep occurs simultaneously via two independent mechanisms; a) conventional and b) super-plastic. In conventional high stress deformation regions, creep is independent of phase size. A stress exponent of 7.1±3 and an activation energy of 19.4±0.4 Kcal/mol has been established. The rate controlling step in conventional deformation is believed to be the stress assisted dislocation climb. In the super-plastic deformation mechanism, creep has a dependance on grain size. A stress exponent of 1.96±0.03 and an activation energy of 11.5 Kcal/mol has been established. Creep deformation is in Appendix D.

(B) HIGH TEMPERATURE DEFORMATION OF THE Pb-Sn EUTECTIC

--- M. Cagnon, M. Suery, A. Eberhardt and B. Baudelet -- Acta Metallurgica, Vol. 25, pp. 71-75, 1977

During high temperature deformation, cells formed by dislocating walls are generally observed. The mean size of these cells depends on the applied stress and its value is usually in the range of 1-100 μm. When the grains have a size smaller than that of the cells, the plastic properties of the material may be quite different. Super-plastic behavior appears in the Pb-Sn alloy with small equiaxed grains of about 1 μm in size.

When the tensile axis is parallel to the lamellae planes, no phase boundary sliding occurs and the constitutive law may be written as:

$$\dot{\varepsilon}/dt = K\sigma^{n'} \exp\left[\frac{-(\Delta H_0 - V_0\sigma)}{kT}\right]$$

In this equation units are in M.K.S. units. i.e., σ is in Newton/Meter^2

Where,

$K = 9.0 \times 10^{-18}$ M.K.S.

$n' = 3.4$

$\Delta H_0 = 0.82$ eV
$= 0.82 \times 1.6 \times 10^{-19}$ Joules $= 1.312 \times 10^{-19}$ Joules

k = Boltzman Constant (Assumed) $= 1.38062 \times 10^{-23}$ Joules/^{0}Kelvin
(The paper does not say so specifically)

$V_0 = 10 \times 10^{-28}$ m^3

Creep equations for 63-37 eutectic solder in ANSYS compatible format were difficult to obtain despite the fact that there exists quite a few constitutive equations for creep behavior of solder. Most of these equations are in a stress-relaxation format or in a format which is ANSYS incompatible.

After examining many of the technical papers on solder creep, we have decided to use an equation given in the technical paper "High Temperature Deformation Of The Pb-Sn Eutectic"

by Cagnon et.el.[19] The primary reason for selecting this equation is that the equation is ANSYS compatible (with little modification). The final form of the equation is shown below:

$$d\varepsilon_{cr} = 1.012 \times 10^{-4} \times \sigma^{3.4} \times \exp\left[\frac{-9507}{T}\right] \times dt$$

The analysis of the paper is shown in the following pages. We compared the results with another paper "Deformation of Pb-Sn Eutectic Alloys at Relatively High Strain Rates" by Grivas, Murty, and Morris.[18]

8.1.2.2 CREEP EQUATION

ANSYS COMPATIBLE CREEP EQUATION

HIGH TEMPERATURE DEFORMATION OF THE Pb-Sn EUTECTIC

--- M. Cagnon, M. Suery, A. Eberhardt and B. Baudelet --- Acta Metallurgica, Vol. 25, pp. 71-75, 1977

This technical paper gives the creep equation for eutectic solder in the following form:

$$d\dot{\varepsilon}/dt = K\sigma^{n'}\exp\left[\frac{-(\Delta H_0 - V_0\sigma)}{kT}\right]$$

In this equation all units are in M.K.S. units. i.e. σ is in Newton/Meter^2

Where:

$K = 9.0 \times 10^{-18}$ M.K.S.

$n' = 3.4$

$\Delta H_0 = 0.82$ eV
$= 0.82 \times 1.6 \times 10^{-19}$ Joule $= 1.312 \times 10^{-19}$ Joules

k = Boltzman Constant (Assumed) 1.38062×10^{-23} Joules/^{0}Kelvin
(The paper does not say so specifically)

$V_0 = 10 \times 10^{-28}$ m^3

Therefore,

$$\dot{\varepsilon}/dt = 9.0 \times 10^{-18} \times \sigma^{3.4} \times \exp\left[\frac{-(1.312 \times 10^{-19} - 10 \times 10^{-28}\sigma)}{(1.38 \times 10^{-23}) \times T}\right]$$

or,

$$d\varepsilon/dt = 9.0 \times 10^{-18} \times \sigma^{3.4} \times \exp\left[\frac{-(9507 - 7.246 \times 10^{-5}\sigma)}{T}\right]$$

The term $7.246 \times 10^{-5}\sigma$ in the exponential function is very small and is neglected. So,

$$d\varepsilon = 9.0 \times 10^{-18} \times \sigma^{3.4} \times \exp\left[\frac{-9507}{T}\right] \times dt$$

In our case, σ will always be in psi and has to be converted to Newton/m^2

Conversion factor is ----> 1 psi = 6894.65 N/m^2

Therefore,

$$d\varepsilon = 9.0 \times 10^{-18} \times [(\sigma) \times (6894.65)]^{3.4} \times \exp\left[\frac{-9507}{T}\right] \times dt$$

OR,

$$d\varepsilon = 1.012 \times 10^{-4} \times \sigma^{3.4} \times \exp\left[\frac{-9507}{T}\right] \times dt$$

For a temperature range of -55 to +125°C (i.e. T= 218°K to T = 398°K), the Yield Stress, σ, varies from 7300 psi to 1230 psi respectively:

for -55°C (i.e. T=218°K) and σ =7300 psi

$$d\varepsilon = 1.59 \times 10^{-10} \times dt$$

for +125°C (i.e. T=398°K) and σ =1230 psi

$$d\varepsilon = 1.40 \times 10^{-4} \times dt$$

FINAL FORM OF CREEP EQUATION TO BE USED

$$d\varepsilon = 1.012 \times 10^{-4} \times \sigma^{3.4} \times \exp\left[\frac{-9507}{T}\right] \times dt$$

Another Creep Equation is analyzed here for a comparison:

DEFORMATION OF Pb-Sn EUTECTIC ALLOYS AT RELATIVELY HIGH STRAIN RATES --- D. Grivas, K.L. Murty, J.W. Morris, JR. --- Acta Metallurgica, Vol. 27, pp. 731 to 737,1979

This technical paper gives the creep equation for eutectic solder in the following form:

$$\dot{\gamma}^{\cdot} = [\, 900(\tau^{\cdot})^{1.96}(d^{\cdot})^{-1.8} \exp(-11500/RT) \,]$$

$$+ [\, (1.3\times10^{15})(\tau^{\cdot})^{7.1} \exp(-19400/RT) \,]$$

Where,

- $\dot{\gamma}^{\cdot}$ = $\dot{\gamma}kT/D_0Gb$ (a dimensionless strain rate)
- $\tau^{\cdot}$ = τ/G (a dimensionless shear stress)
- $d^{\cdot}$ = d/b (a dimensionless grain size)
- $\dot{\gamma}$ = Strain Rate
- k = Boltzman's Constant = 1.38×10^{-23} Joule/^{0}K
  = 1.38×10^{-16} erg/^{0}K ; (1 Joule = 10^7 ergs)
- T = Absolute Temperature
- D_0 = Diffusivity for pure Sn (0.08 cm^2/s)
- G = Shear modulus of Pure Sn (2×10^{11} d/cm^2)
- b = Bergers Vector of pure Sn (3.18 A) = 3.18×10^{-8} cm.
- τ = Resolved Shear Stress
- d = Mean Grain Diameter = 5.5μM = 5.5×10^{-4} cm.

Therefore,

$$\dot{\gamma} = [\, D_0Gb/kT \times 900(\tau/G)^{1.96}(d/b)^{-1.8} \exp(-11500/RT) \,] + [\, D_0Gb/kT \times (1.3\times10^{15})(\tau/G)^{7.1} \exp(-19400/RT) \,]$$

$$\dot{\gamma} = \frac{[D_0b^{2.8} \times 900(\tau)^{1.96}(d)^{-1.8} \exp(-11500/RT)]}{kT\,(G)^{0.96}} + \frac{[D_0b \times (1.3\times10^{15})(\tau)^{7.1} \exp(-19400/RT)]}{kT\,(G)^{6.1}}$$

or,

$$d\dot{\gamma}/dt = \frac{[0.08\times(3.18\times10^{-8})^{2.8}\times900(\tau)^{1.96}\times(5.5\times10^{-4})^{-1.8}\exp(-11500/RT)]}{1.38\times10^{-16}\times(2.0\times10^{11})^{0.96}\times T} + \frac{[0.08\times3.18\times10^{-8}\times(1.3\times10^{15})\times(\tau)^{7.1}\exp(-19400/RT)]}{1.38\times10^{-16}\times(2.0\times10^{11})^{6.1}\times T}$$

or,

$$d\dot{\gamma}/dt = \frac{[\,5.53\times10^{-9}(\tau)^{1.96}\exp(-11500/RT)\,]}{T} + \frac{[\,2.775\times10^{-47}\,(\tau)^{7.1}\exp(-19400/RT)\,]}{T}$$

Taking $\sigma = \sqrt{3}\tau$; $\sqrt{3}\varepsilon = \gamma$; and σ in psi = σ x 68930 dynes/cm^2

(σ is in psi in our case and has to be converted to d/cm^2)

$$\sqrt{3}\, d\dot{\varepsilon}/dt = \frac{[\, 5.53 \times 10^{-9} (\sigma x 68930)^{1.96} \exp(-11500/RT)\,]}{(\sqrt{3})^{1.96} \times T} + \frac{[\, 2.775 \times 10^{-47} (\sigma x 68930)^{7.1} \exp(-19400/RT)\,]}{(\sqrt{3})^{7.1} \times T}$$

or,

$$d\varepsilon/dt = \frac{[\, 3.310 \times (\sigma)^{1.96} \exp(-11500/RT)\,]}{T} + \frac{[\, 7.305 \times 10^{-15} (\sigma)^{7.1} \exp(-19400/RT)\,]}{T}$$

i.e.

$$d\varepsilon = \frac{[\, \mathbf{3.31} \times (\sigma)^{1.96} \exp(-11500/RT)\,]}{T} \times dt + \frac{[\, \mathbf{7.305} \times 10^{-15} (\sigma)^{7.1} \exp(-19400/RT)\,]}{T} \times dt$$

For T =218 K, σ =7300 psi,R =2.0, we get $d\varepsilon = 1.99 \times 10^{-6} \times dt$

For T =398 K, σ =1230 psi,R =2.0, we get $d\varepsilon = 5.03 \times 10^{-3} \times dt$

The value of the exponent n has been taken as 1.96. But in the paper the authors stated that

an average value of the slope is n = 1.95 ± 0.23 was obtained (from Table 1 in the paper). Also the tolerance on the constant 900 in the equation has been given as ±110.

Hence, if we take n = 1.95 - 0.23 = 1.72 ;

and the constant = 900-110 =790,

then, at the high temperature, we get

$$d\varepsilon = 8.0 \times 10^{-4}$$

This value is not much different than the high temp creep value obtained in the equation we have decided to use.

8.1.2.3 ANSYS CREEP EQUATION

The ANSYS format of creep equation is shown below:

$$d\varepsilon_{cr} = C1\ \sigma^{C2}\ \varepsilon^{C3}\ \exp\left[\frac{-C4}{T}\right] \times dt$$

Where,

σ = Equivalent Stress
ε = Equivalent strain (based on total strain and previous creep strain)
T = Absolute temperature
t = Time at the end of iteration

The creep equation we have chosen is shown below:

$$d\varepsilon_{cr} = 1.012 \times 10^{-4} \times \sigma^{3.4} \times \exp\left[\frac{-9507}{T}\right] \times dt$$

Where, C1 = 1.012×10^{-4}
C2 = 3.4
C3 = 0.0
C4 = 9507

The constants C1 through C4 are entered into ANSYS input with the "NL" command in PREP7. The C5 field is left blank and a zero (0.0) is entered into the C6 field to invoke the ANSYS creep equation.

8.1.3 INDUCED STRESSES

Stresses other than those attributed to thermal cycling or temperature excursions also play a role in determining the solder joint fatigue life. On leaded surface mount devices (and also on through hole devices, shown by Wild and others), tensile stress can cause failure of the joint. When a lead is deflected to hold it in place during reflow (rework, hot bar) there may be enough stress induced into the solder joint that it will eventually fail from the lead trying to return to its relaxed (pre-soldered) position. This failure is known as a creep rupture failure caused by induced tensile stress due to lead loading or deflection. The amount of stress necessary to cause a creep rupture failure has been shown to be as little as 200 psi.[1] The failure may occur over time with little or no thermal excursions. Creep rupture is less dependent upon temperature than time and stress. As stated earlier, tensile stresses will also accelerate the failure of joints with heavy intermetallics at the joint interface faster than through the bulk solder when normal amounts of intermetallics are present. The tensile stresses are not relieved by creep relaxation as occurs in the bulk solder. During thermal cycling, the stress induced into the solder is reduced as the solder recrystallizes and the strain placed on the solder slows as the system reaches equilibrium. Under tensile load the intermetallic will continue to degrade throughout the cycle.

8.1.4 VIBRATION AND SHOCK

Although the emphasis of this report has focused on the thermal cycling problems of surface mounted devices, there are, yet other factors which may contribute to failure; namely shock and vibration. Less work has been done on these two topics, as they are believed to be less of a contributor to the problem and impossible to predict in general terms. Further FEA should be performed to evaluate the effects of shock and vibration on the strain energy of the solder joint. How much of a contributor to joint degradation is not well known, but it is believed that these simulations will determine the extent.

What is theorized about these conditions is that, once a solder joint, or group of solder joints has begun to crack, any severe amount of shock or vibration will further accelerate the failure of the joint(s). Or, the shock may be so severe as to cause instant failure, due to existing degradation in the solder. This is a serious concern in predicting a "point of failure" for a solder joint. Under thermal cycling only, the life of the solder joint may last another 500 cycles, however, a slight shock may be sufficient for the joint to fracture and become electrically open. To what extent this question can be answered remains to be seen.

8.2 NON-MODELABLE FAILURE MODES

There are many factors which contribute to the reliability of a surface mount solder joint; many of which can be modeled and analyzed with tools such as finite element analysis. However, many of the design and process characteristics of the solder joint cannot be modeled or simulated in determining its reliability. These characteristics include, but are not limited to; grain structure of the solder, intermetallic compounds along mating interfaces, porosity of the solder, contaminant entrapment, conformal coating, solderability and others. These characteristics are responsible for many of the field failures attributed to solder joints in surface mounted devices, and in some cases, through hole devices. Although these conditions cannot readily be modeled, their existence or possibility of occurrence must be accounted for in determining reliability.

8.2.1 GRAIN STRUCTURE

Grain structure plays a significant role in determining the strength of a solder joint. A fine, tight grain structure (Figure 8.2.1-1 and 8.2.1-4), obtained through rapid cooling of solder (soldering iron, forced cooling after reflow, laser reflow) produces a stronger bond material than a loose, coarse grain structure (Figure 8.2.1-3). Coarse grains occur due to the solder cooling at a slow rate, allowing the molecular structure of the solder to change. Domain enlargement and recrystallization occurs, forming large regions of Sn/Pb phase, as well as allowing Pb to precipitate out of phase, producing Pb rich and Sn rich regions.

What occurs during thermal cycling is not unlike slow cooling. During the high temperature excursions, and as stresses (shear) are being applied to the solder, the Sn/Pb phases grow and recrystallize, lessening their mechanical integrity. Grain structure growth is most noticeable along the path of the shear stress, typically between the LCC bottom metallization and the PWB pad region. This grain growth weakens the solder, allowing the formation of cracks which travel through the solder along the grain boundaries and along Pb rich regions[1,2,3] (Figure 8.2.1-8). For this reason, even in solder having the finest grain structure immediately after reflow, recrystallization will occur as heat and shear stresses are applied[2] (Figures 8.2.1-6 and 8.2.1-7). This weakens the originally sound solder joint, allowing cracks to form and eventually cause an open over time. Studies have shown that the increased life of a solder joint with a fine grain structure is not appreciably greater than other solder joints once shear stresses have recrystallized the grain structure along the shear path.[3]

This phenomena of recrystallized grain growth along the shear path also reduces the effectiveness of tall, thick solder joints. Once the change in the solder structure has occurred, the stresses will continue to pass through this region (path of least resistance) no matter how tall the joint profile. The height of the joint does delay this occurrence of recrystallization because of increased compliance, but it is inevitable over time.[1]

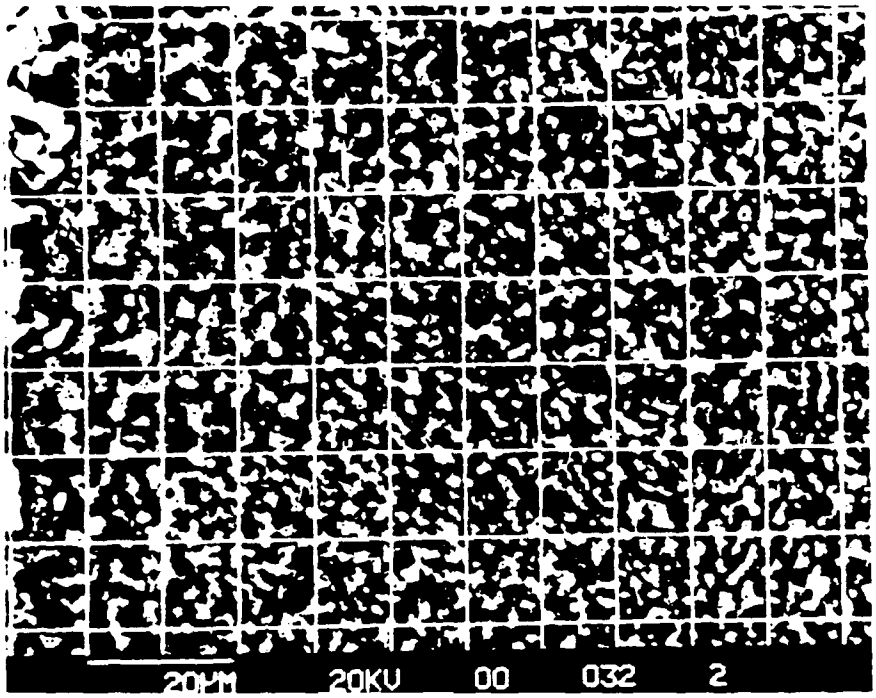

FIG. 8.2.1-1 NORMAL EUTECTIC STRUCTURE OF FAIRLY RAPIDLY COOLED 63/37 Sn/Pb SOLDER

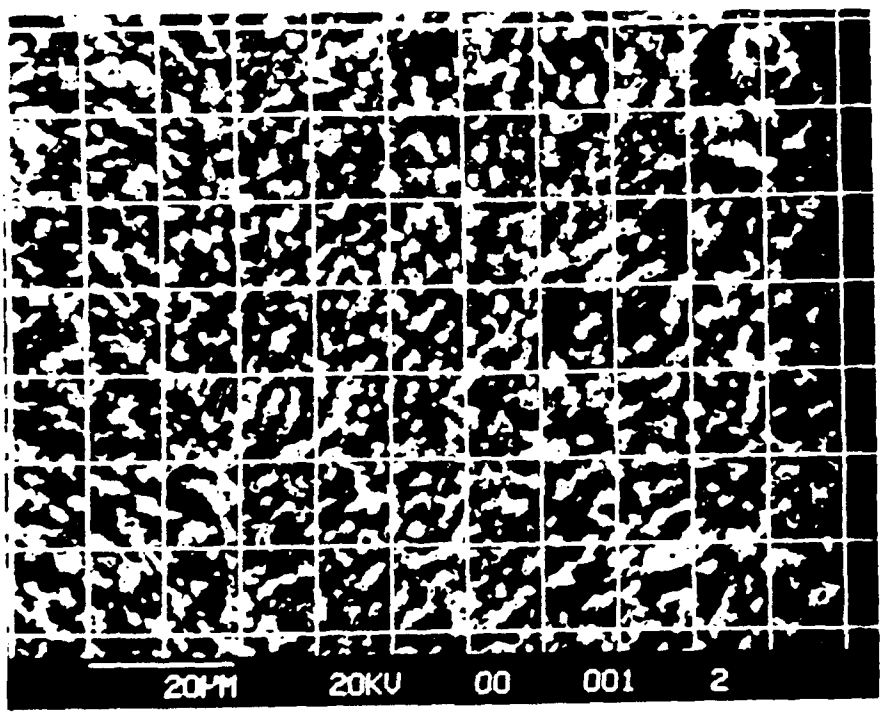

FIG.8.2.1-2 SLOWLY COOLED 63/37 Sn/Pb SOLDER, NOTE COARSE STRUCTURE

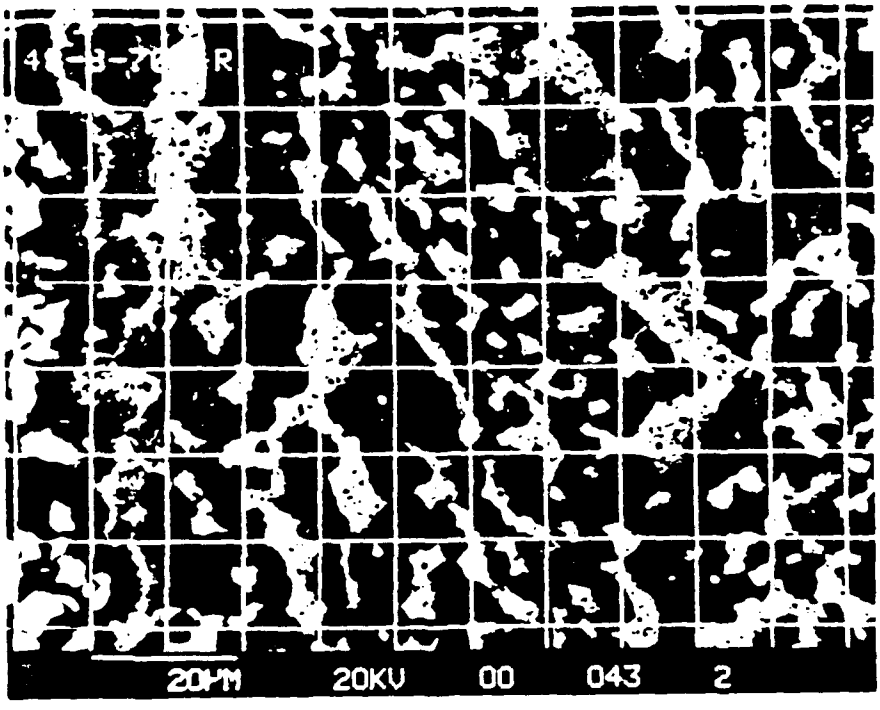

FIG. 8.2.1-3 EFFEECT OF THERMAL CYCLING ON FIG 8.2.1-1 SOLDER. SOLID STATE DIFFUSION/COARSENING

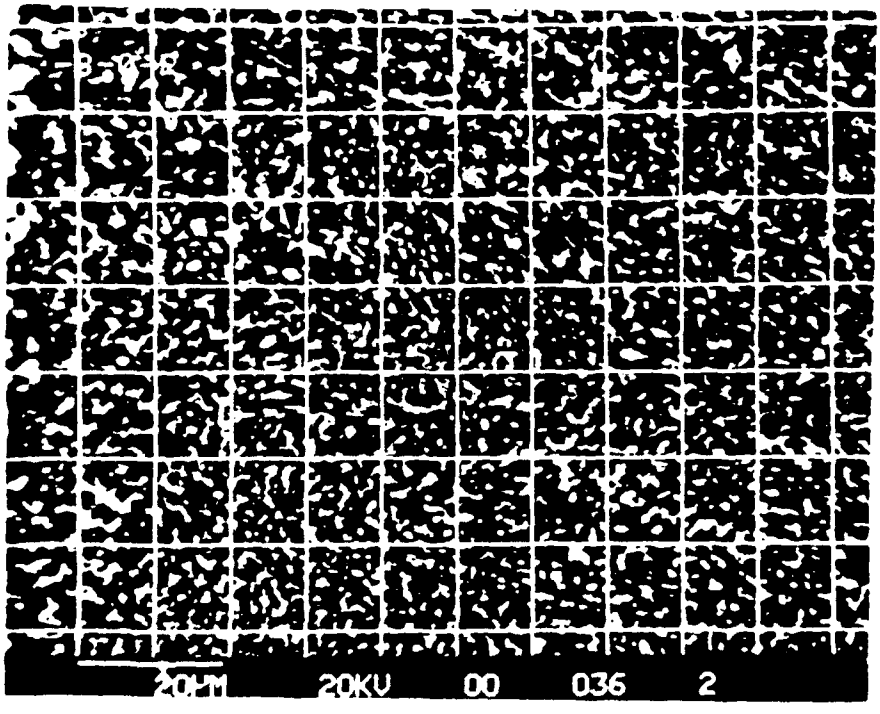

FIG. 8.2.1-4 63/37 Sn/Pb SOLDER RAPIDLY COOLED BY LASER SOLDERING

DeVore/GE (Ref. 9)

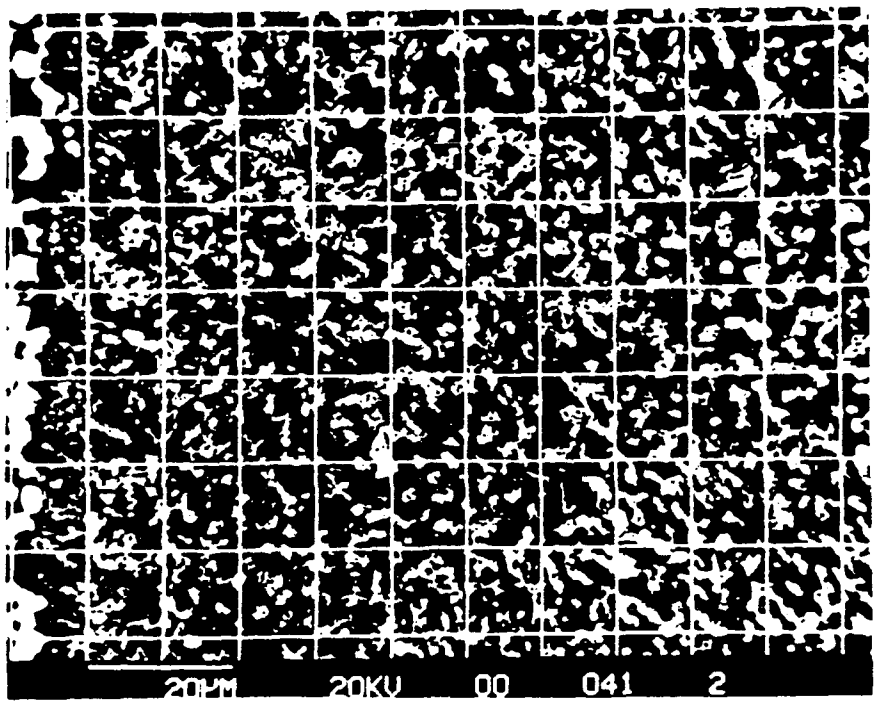

FIG. 8.2.1-5 63/37 Sn/Pb SOLDER VAPOR PHASE REFLOWED

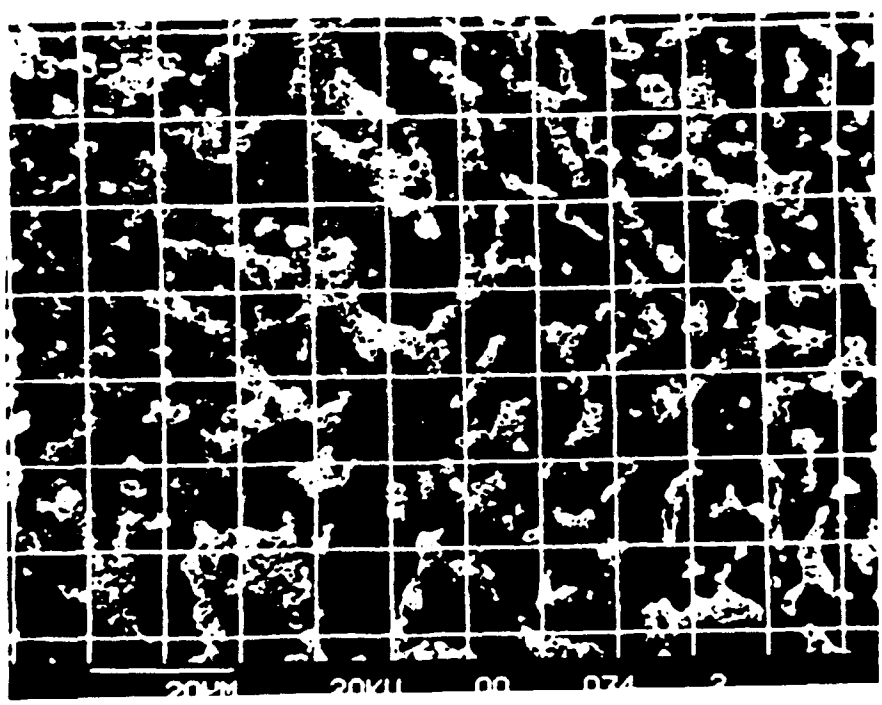

FIG. 8.2.1-6 LASER SOLDER JOINT AFTER 1000 THERMAL CYCLES (-55 TO +125°C)

DeVore/GE (Ref. 9)

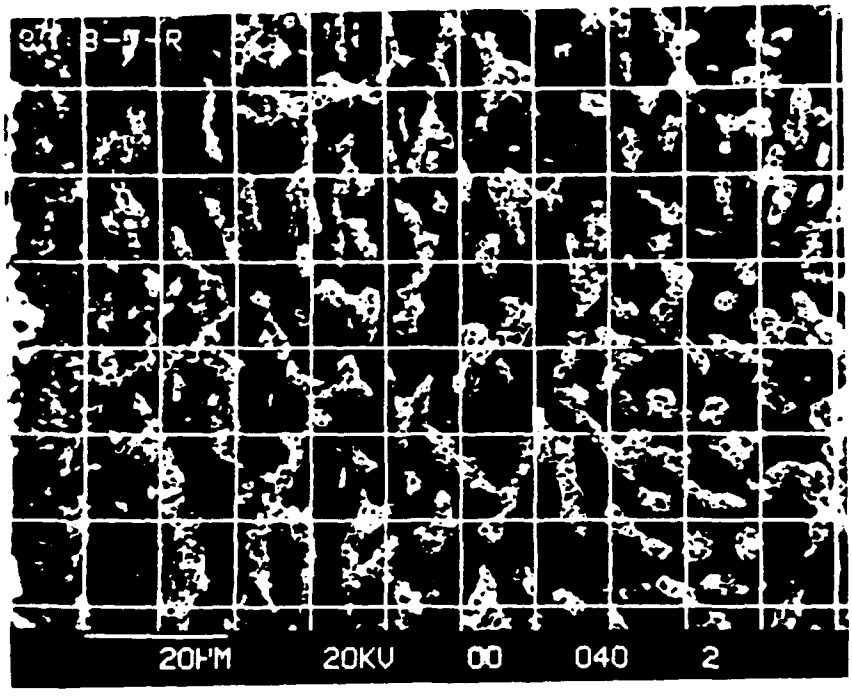

FIG. 8.2.1-7 VAPOR PHASE JOINT AFTER 1000 THERMAL CYCLES (-55 TO +125^{0}C)

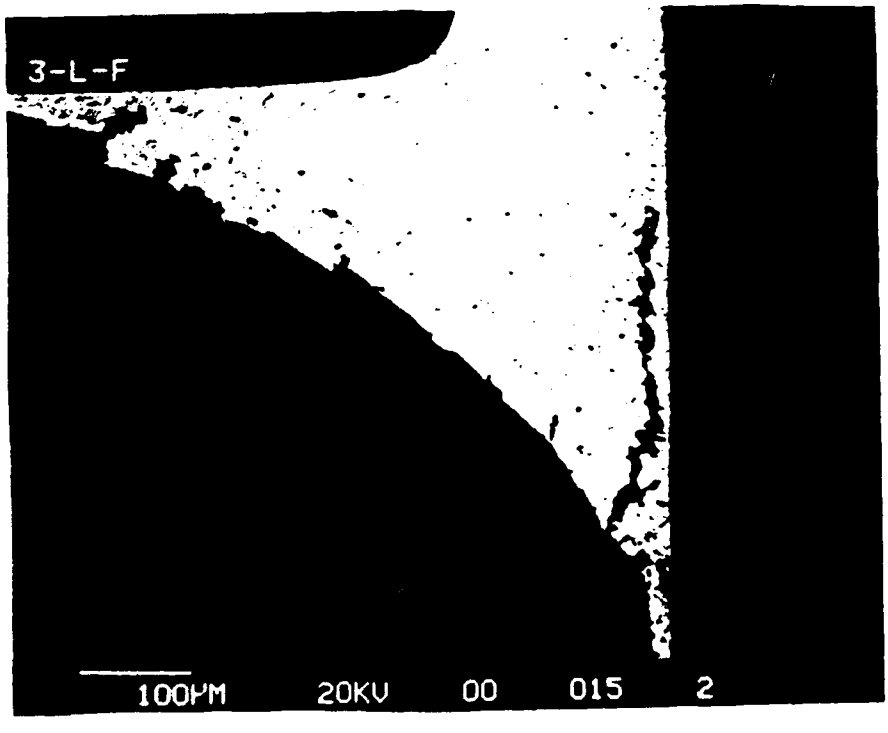

FIG. 8.2.1-8 COARSENING AND RESULTANT CRACKING IN A THROUGH HOLE SOLDER JOINT SUBJECTED TO STRAIN. SIMILAR FAILURE MODE AS A SMD.

DeVore/GE (Ref. 9)

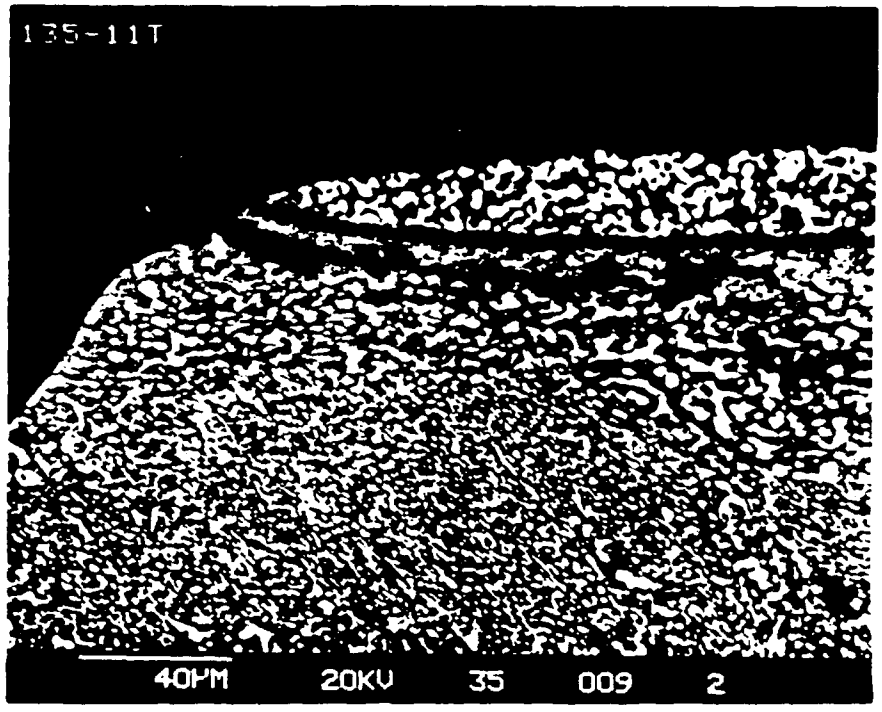

FIG. 8.2.1-9 CRACK PROPAGATION ALONG RECRYSTALLIZED GRAIN PATH

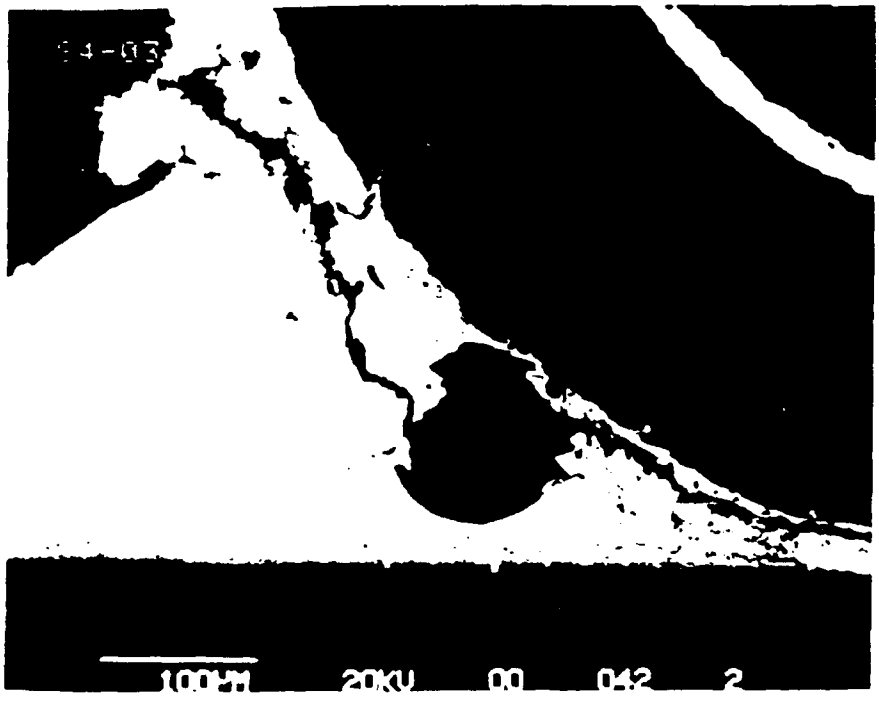

FIG. 8.2.1-10 CRACK PROPAGATION THROUGH A VOID

DeVore/GE (Ref. 9)

8.2.2 INTERMETALLIC COMPOUNDS

Intermetallic compounds and intermetallic growth along material interfaces is another potential reliability concern. During the soldering operation, the molten solder reacts metallurgically with the base metal of the pad, not unlike a chemical reaction, forming an intermetallic compound. This material is an alloying of the solder alloy and the base metal, depending upon the type of materials used. Typically this is a nu-phase Cu/Sn intermetallic (Cu_5Sn_6). Copper being the pad material and Sn from the Sn/Pb solder alloy. A second form of intermetallic compound forms through solid-to-solid diffusion (Cu_3Sn). This v-phase layer forms under the nu-phase at T $\geq$60 °C. It is a more brittle intermetallic and has more influence on the long term reliability of the solder joint[2,4].

Intermetallic growth is a function of time and temperature. The longer the materials are at temperature or maintained in extended stores, the greater the amount of intermetallic formation. Obviously, some intermetallic compounds are essential to a solder joint, for this is what actually makes the mechanical bond. However, when the solder is molten for an extended time period, or maintained at higher temperatures for long durations, intermetallic growth will continue beyond that which is required to form a satisfactory bond. Intermetallics are brittle compared to Sn/Pb compounds or the basis metal which is being soldered.

There are few cases where crack propagation has occurred through the intermetallic growth while under shear loading. This was once a popular theory in leadless surface mount solder joint failure analysis (early Mantech data). In instances where cracks occurred in the intermetallic region, the solder joint thickness was so thin that the intermetallic became a significant contribution to the overall thickness of the joint. The crack propagation was able to branch out of the ductile solder region and into the brittle intermetallic layer, causing a more rapid failure.[2]

Where the concern comes into play on intermetallics (outside of solderability concerns) is when the solder joint is under a tensile load.[2] This situation typically occurs on leaded chip carriers where the lead has some amount of residual stresses remaining after solder solidification due to a forced deflection and hold down of the lead during solder solidification.

Morris' study shows that failure at the intermetallic layer usually occurs more rapidly through tensile stresses than does failure in the bulk solder (8.1.3, Induced Stresses).

8.2.3 POROSITY

Porosity has been shown to have little effect on the resulting solder joint fatigue life when the voiding is less than 25% of the solder joint volume.[1] When the porosity becomes greater than 25% of the joint volume, other problems are usually occurring which should signal a process control problem (i.e. poor solder paste, excessive oxidation on pads or solder spheres, or an inadequate thermal profile). This type of porosity may cause stress risers or easy paths for crack propagation to occur, thus resulting in more rapid solder joint failure. Particularly, voids at the knee of an LCC solder joint (the bottom corner of the castellation) are known to be stress concentration points for cracks to begin.[5]

8.2.4 CONTAMINANT ENTRAPMENT

At this writing, little has been done to evaluate the affects of contaminant entrapment in surface mount solder joints. This is usually a workmanship related topic where contaminants and foreign materials are not allowed in solder joints. Work has been done to evaluate the affects of small amounts of impurity metals (Sb, Al, As, Bi, Cd, Cu, Fe, P, S, and Zn).[6] However, these levels are typically above the specification limits of MIL-SPEC or commercial grade solder and are highly unlikely to occur in the processing of surface mount solder joints. It can be stated that contaminants from processing materials (paste binder, flux residue, etc.) are cause for reliability concern. Ionic residues, commonly found in rosin based fluxes are a known cause of crystalline growth on PWA's, producing current paths between conductors. This phenomenon is exacerbated in high humidity environments which promote the crystalline growth. Shorting or grounding may cause intermittents in the circuit or complete mission failure.

Oxidation on solder balls has not been shown to be a reliability factor, but, it is a processing factor. Excessive oxidation in the paste will cause poor wetting and flow of the solder which in turn may lead to rework of the solder joint. It is the rework that becomes the reliability

concern due to the level (or lack) of process control during the rework operation. The most reliable solder joint is the first solder joint.

8.2.5 CONFORMAL COATINGS

Experiments at IBM[1] (Wild) and others have shown that in some instances, an application of conformal coating can improve the fatigue life of standard processed surface mount solder joints. Wild's experiment showed a 2X increase in thermal cycle life over standard reflowed joints with an application of .001" of Paralene ™. However, he cautions of using this data for all types of conformal coatings. He has shown that an uneven or partial application of coating may be detrimental to LCC solder joint fatigue life due to uneven solder joint stress applications.[1]

8.2.6 SOLDERABILITY

The solderability of the components and the substrate play an important role in establishing the reliability of the solder joint. There are three basic elements of solderability; wetting, non-wetting and dewetting.[7] Wetting is the ability of the base material to form an atomic level bond with the solder alloy. Non-wetting is the inability to form an atomic level bond, usually caused by an incompatibility or a physical barrier between the solder and the base material (oxidation, unsolderable intermetallic compound, wrong flux). Dewetting is defined as all of the gray areas in between wetting and non-wetting.

Solderability plays the most important role in establishing the (desired) intermetallic bond between the substrate and the solder and between the solder and the component. If either one of these mechanisms is faulty (non-wetting, dewetting), then the solder joint is less than optimal. The reliability risk is dependent upon the severity of the wetting problem. Non-wetting problems should be caught at the incoming/receiving inspection solderability tests. With proper storage and shelf life controls, few dewetting problems should be occurring. Unfortunately, this is not always the case and components or PWB's get into the system which have solderability problems.

The primary solderability failure is through dewetting. DeVore states that dewetting is caused by gas evolution during the soldering operation. The source of the gas is the thermal breakdown of organics or the release of water of hydration from inorganics. The water, under high temperature environments of soldering accelerates oxidation of the surface of the molten solder film or of the substrate interface. The area affected is typically the intermetallic surface at the molten solder interface.[7] Dewetting at this interface may form voids large enough or in enough quantity to reduce the effective solder joint area, thus reducing its overall strength, fatigue resistance and electrical conductivity. Voids may act as stress risers and reduce fatigue resistance of the joint as well.

Proper solderability testing and control cannot be over emphasized to insure a strong reliable solder joint. Nothing solders better to solder than solder.

8.2.7 CONCLUSION

It has been shown that there are other factors affecting the fatigue life of surface mounted solder joints besides solder joint size, shape and composition. Grain size, intermetallic compounds, contaminants, coatings and other factors can negatively influence a solder joint. Optimization of process controls, solderability and design play a significant role in ensuring reliable, long lasting surface mount solder joints.

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APPENDIX A

SURFACE MOUNT DESIGN GUIDELINES

SMT DESIGN, MANUFACTURING, AND QUALITY HANDBOOK

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GLOSSARY OF SURFACE MOUNT TERMS

Assembly	– A functionally complete unit made up of parts and/or subassemblies mechanically and/or electrically joined together.
Bare Board Test	– A test of the bare circuit board or substrate before components are attached.
Base Material	– The insulating material upon which the conductor pattern may be formed. The base material may be rigid or flexible. It may be a dielectric sheet or insulated metal sheet.
Board Set	– Is a group of similar type PWB's containing a quantity of similar type components that would make up a data set.
CAD	– Computer-Aided (or Assisted) Design
CAM	– Computer-Aided Manufacturing. Refers to computer-assisted manufacturing tools.
Castellation	– The metalized recess on the side of a chip carrier used to connect conducting planes within the chip carrier as well as provide the interface to an interconnecting structure.
CAT	– Computer-Aided Testing. Refers to computer-based test equipment.
CERDIP	– Ceramic Dual In-Line Package
Chip Carrier	– A low profile rectangular package that protects a semiconductor chip as well as provides the termination interface for the chip (may be leaded or leadless).
CIC	– An abbreviation for Copper/Invar/Copper core material for PWB's.
CIM	– Computer-Integrated Manufacturing. Refers to the linkage of CAD and CAM and CAT together.
Coefficient of Variation	– A measure of dispersion defined as the ratio of the standard deviation to the mean expressed as a percent: $COV = \frac{S}{\bar{x}}(100\%)$
Component	– An electrical, separable part which performs a circuit function (e.g., resistor, capacitor, etc.).
Confidence Level	– The probability that a correct interval estimate is obtained (one that contains the parameter value).
Constraining Core	– A supporting plane internal to an interconnecting structure.
CTE	– Coefficient of Thermal Expansion. The linear thermal expansion per unit change in temperature.
Cure	– The process of placing an SMA in an oven to remove volatiles from a solder paste prior to reflow or setting an adhesive.
Data Point	– The point at which a failure has occurred on a specific component during a particular environmental test on a specific printed wiring board.

Data Set	– A group of data points where all the data points are the same type component on the same type PWB in the same type environmental test.
DIP	– Dual In-Line Package
Dip Solder	– Literally to dip an assembly into a pot of molten solder as a means of soldering.
EMI	– Electro-Magnetic Interference
EMI/RFI	– Electro-Magnetic Interference/Radio Frequency Interference
Error of Estimate (precision)	– The difference between a population parameter and the estimate of that parameter (ex. 1x–1).
Estimator	– A function of observed values from a population used to estimate a parameter (ex. $\bar{x}$ = mean).
Flow Soldering	– A general term referring to either reflow solder or wave solder methods.
FP	– Flat pack
Functional Testing	– A circuit board test method that tests the SMA board at its external connections.
Gate Array	– An IC customized to cluster several logic gates in an array, generally high pin count.
Green Ceramic	– Unfired ceramic with very low liquid content.
IC	– Integrated Circuit
In-Circuit Test	– A circuit board test method using fine probes to test each board component individually.
Interconnecting Structure	– The medium used to interconnect components. Similar unique terms are printed wiring board, substrate, composite board, and packaging and interconnect structure.
JEDEC	– Joint Electronic Devices Engineering Council
"J" Factor	– Product of CTE and Modulus of elasticity.
"J" Lead	– Lead shaped like a J with its hook extending under the package body.
Land	– That portion of a conductive pattern usually, but not exclusively, used for the connection, or attachment, or both of components.
Land Pattern	– A unique grouping of lands used to mount a component and provide interconnecting between components.
LCC	– Leadless Chip Carrier. An SMA package with castellated sides instead of leads, usually ceramic.
LCCC	– Leadless Ceramic Chip Carrier
LSI	– Large Scale Integration Complexity IC. Usually 18–44 leads.
Man Tech	– Manufacturing Technology development activity sponsored by the Air Force.

Mean (or average) – A measure of the center of a distribution defined as:

$$\bar{x} = \frac{x_1 + x_2 + \cdots x_n}{n} = \frac{\sum_i^n x_i}{n}$$

Melf (Metal electrode face) – A term describing tubular SMC's, usually resistors, capacitors, inductors, and diodes (tubular component).

Mini-Pak (1) – A Xerox coined term for any small electronic package.

Mini-Pak (2) – An AWI coined term for a prototype IC chip carrier package made of fiberglass and gold plated copper laminated lands.

MOS – Metal Oxide Semiconductor

MSI – Medium Scale Integration Complexity IC. Usually 16–20 leads.

P&IS – Packaging and Interconnect Structure. Typically a printed wiring board and constraining core assembly.

Parameter – Numerical descriptive measure of a population (ex. μ = mean).

PCC – Plastic Chip Carrier. Common American term for a four-sided gull-wing SMD package. Current sizes range from 18 to over 100 leads.

PLCC – Plastic Leaded Chip Carrier. Typically consisting of "J" leads.

PTH – Plated-Through-Hole

PWB – Printed Wiring Board

PQFP – Plastic Quad Flat Pack. Common designator for a plastic, four-sided gull-wing SMC package. Current sizes range from 20 to over 300 leads.

QFP – Quad Flat Pack. Common American designator for a ceramic four-sided gull-wing SMC package. Current sizes range from 20 to over 300 leads.

RAM – Random Access Memory

Range – A measure of dispersion defined as the difference between the largest and smallest values in a data set.

Reflow Solder – Term used to designate various methods for generating heat to reflow solder pastes used to attach SMD's onto SMA's.

Sample – A collection of observed values from a population.

Signature Analysis – A circuit board test method using fine probes to test sections (component clusters) of the board.

SMA – Surface Mount Assembly. Refers to any electronic assembly containing a majority of surface mount components.

SMC – Surface Mount Component. The term designating any electronic component that mounts on the assembly surface.

SMD – Surface Mount Device. Same as SMC. SMD is a trademark and service mark of N.A. Phillips, though commonly used.

SMT	– Surface Mount Technology. General term to designate the use of SMD's for electronic assembly.
SO	– Small Outline
SOIC	– Small Outline Integrated Circuit. A plastic SMD package. Current pinout standards are 8, 14, 16, 18, 20, 24, and 28 leads.
SOL	– Small Outline, Wide (Large)
SOT	– Small Outline Transistor. A plastic SMD package. Current pinout standards are 8, 14, 16, 18, 20, 24, and 28 leads.
SSIC	– Small Scale Integration Complexity IC. Usually 8–14 leads.
Standard Deviation	– A measure of dispersion or scatter about the mean defined as: $S = \sqrt{\frac{\sum_{i}^{n} (x_i - \bar{x})^2}{n - 1}}$
Surface Mounting	– The electrical connection of components to the land patterns of an interconnecting structure without the use of component lead through-holes.
TCE	– Temperature Coefficient of Expansion
Thick Film	– Conductive and resistive inks that are fired onto a substrate.
Thin Film	– Metal deposition onto a substrate/vacuum deposition.
T_J	– Junction Temperature
Tombstone	– Typically a chip component that has stood up on one end during soldering.
UHIC	– Universal Hybrid Integrated Circuit
VIA	– Passageway through a substrate, plated or solid, to provide continuity.
VHSIC	– Very High Speed Integrated Circuit
VLSIC	– Very Large Scale Integration Complexity IC. Usually 28–200 leads.
1206	– Pseudo-standard size for rectangular chip resistors and chip capacitors. Size is 0.120″ x 0.060″.
Wave Soldering	– A solder method where the assemblies are conveyed over the top of a wave of molten solder.

For other industry standard definitions see IPC-T-50.

1 DESIGN

1.1 Design Considerations

The use of surface mount technology offers a viable way to achieve the low volume and the low weight required by today's electronic systems. It also facilitates the implementation of high-speed circuits when ECL, VLSI, and VHSIC devices are utilized. However, this technology has inherent problems not present in conventional through-hole technology. In addition to the design considerations that are common to both technologies, such as circuit partitioning, thermal management, producibility, testability, reliability, PWB manufacturing allowances, etc., the use of SMT imposes additional considerations when leadless devices or noncompliant leads are used. The main considerations are that of matching the thermal expansion coefficients of the PWB to that of the device and to optimize the design of land patterns for reliable solder joints. Sections of this document discuss design issues and considerations as well as general manufacturing guidelines.

These are not intended to be final specification rules, but merely guidelines to develop a reliable, manufacturable surface mount design. These guidelines are based on the results of this reliability study as well as industry experts' findings and hands-on industry experience. Much of the information has been extracted from standard military specification (MIL-STD-275, MIL-STD-2000A), IPC documents, and other electronic publications and articles. It is up to the designer to ensure that the design meets the particular requirements of his job, based on the mission and environment of the system. However, using a design that is significantly different from these guidelines should be backed-up with testing data to justify the particular deviation. The first priority of the SMT PWB designer is reliability. Reliability cannot be improved in production if it is not optimized in the design.

1.1.1 Component Selection

Component selection is one of the initial phases of the design which must be accomplished before the circuit may be laid out. But, simply stating a component value and size is not enough for a reliable design. Some general guidelines for component selection are as follows:

1. Avoid using metal electrode face (MELF) packages. They are less reliable and more difficult to assemble, requiring special footprints and placement considerations. MELF's are usually used in high volume commercial applications due to their typically lower cost.
2. Avoid nonmechanically supported connectors. The solder joints alone, no matter how many, cannot take the load of mating and unmating. Often, not even once.
3. Use a standard size passive component (chip capacitors and resistors) in the largest size allowable for the design. To ease handling and assembly, however, some consideration must be given to reflow method before selecting final component sizes. See Section 1.5.2.1. The most popular chip component sizes are the 1206 (0.120 inch x 0.060 inch) and the 0805 (0.080 inch x 0.050 inch) and are most readily available.

4. When selecting chip capacitors, avoid using the highest values available in a given chip size. This maximizes the amount of metal in the ceramic, leading to possible failures due to metal and ceramic CTE mismatches. Choose the next largest package size. This is particularly important when the chips are to be wave soldered.
5. Choose between leaded and leadless chip carriers carefully. Leadless chip carriers require less processing and take up slightly less real estate, but require special CTE matching measures to preclude stress cracking. Leaded devices require a preform operation to form the leads to match the footprint, and special handling precautions. However, they absorb CTE mismatch stress better and are easier to inspect and rework.

Other considerations specific to the components to consider are labelling, lead finish (Hot Solder Dipped preferred), Nickel barriers on chips to preclude precious metal leaching and solder coating of gold leads. All of these topics, and more, have been addressed throughout the industry and are available in most of the literature and proceedings which abound in the electronics world.

1.1.2 Printed Wiring Board and Manufacturing Considerations

Once component considerations have been addressed, consider the manufacturing aspects of the design and how they will be influenced by the available production equipment to be used. Some of the items to remember to make the assembly easier are:

1. Limit the size of the PWB or panel to that which can be accommodated by the production equipment. Typically 13 inches by 13 inches is a good maximum guideline.
2. Make the PWB as small as possible to avoid warp and twist problems.
3. Panelize the PWB to provide uniform tooling and ease handling.
4. Consider board edge clearances for fixturing or wave solder conveyor fingers. Components must not interfere.
5. Locate components on a grid to ease programming of automatic dispensing or placement equipment.
6. Remember to make allowances for visual inspection, rework, and ECO changes to the assembly.

1.2 Specifications

This section deals with the use and interpretation of product requirements as specifications. It offers a method for converting general environmental specifications to specific test conditions which can be compared to test data from which a margin of safety can be estimated.

A list of military and commercial specifications and documents that may be of interest to the reader is presented. It is strongly recommended that the reader acquire a copy of the recently issued IPC document IPC-SM-782 (surface mount land patterns, configurations and design rules) and the MIL-STD-2000, Rev A (upon release).

1.2.1 Defining Product Specifications

MIL-STD-810D makes it clear that it is the responsibility of the contractor to determine exactly what the life requirements are for a product and to perform analysis and tests to ensure the product's performance over its life. The first step is to identify the environmental design requirements. Table 1.2.1 is an accumulation of information from various program specifications. These specifications are system level and are not the conditions to which the solder joints will be subjected. Performance evaluation tests are devised from the requirements.

Design of performance evaluation tests is a difficult task and subject to challenge. The EIA/IPC Surface Mount Council states:

"The problem in performance evaluation is that no simple set of tests can be used to predict field life for the different component package types in conjunction with their interconnection product. Also, significant changes in application change the field failure mechanism, and therefore impacts the suitability of the test that will predict the lifetime performance or even allow comparison. The real risk for future electronic equipment is that inappropriate and poorly understood qualification testing can lead to a large amount of product being tested, passed and then becoming a catastrophic field failure."

Due to the difficulties discussed above regarding the determination of a relevant performance test program, many companies have adopted the stringent MIL-STD-883B semiconductor performance testing temperature range of -55 °C to +125 °C. The maximum junction temperature for devices is derated to +125 °C by reliability requirements and typical system designs have a maximum junction temperature of 105 °C. Temperature gradients through the component body and solder joints to the printed wiring board result in roughly a 15–20 °C drop. Depending on other physical system packaging parameters this estimate can be high or low. Consequently,military systems do not experience a maximum temperature value of +125 °C. This implies that a solder joint should not see temperatures above 105 °C if 125 °C junction temperature is used and 85 °C for a 105 °C junction temperature.

It has been said that designing to withstand the MIL-STD-883C temperature test is a conservative approach and that reaching 1000 cycles without solder joint failures will therefore be sufficient to demonstrate the integrity of a selected SMT. This number is strictly arbitrary and has never been correlated back to any real, representative program, thermal environment, or life requirements.

Table 1.2.1. Environmental Specifications for Various Equipment Types

Equipment Type	Storage Temp.	Operating Temp.	Vibration Sine	Vibration Random		Shock
				g rms	Min/ Axis	
Space						
MIL-STD-1540 and DOD-E-8983C		-34 to +71 °C	0.5 in. DA 5–8 Hz, 1.5 g from 8–500 Hz	12.12	5	MIL-STD-810
PDMS	-37 to +71 °C	-20 to +60 °C	Not Specified	16.90	1	Method 516.2 Proc II
OTA	-55 to +85 °C	-40 to +35 °C	5–12 Hz 0.5 in. DA	26	3	Not Specified
S^3	-55 to +85 °C	+5 to +38 °C	12–120 Hz 4 g pk			Not Specified
NSCAT RFS		-30 to +85 °C	120–200 Hz 2 g pk	13.1	3	Pyro
Shuttle	-54 to +65 °C	+2 to +50 °C	Not Specified	11.2	48	20 g pk, 11ms
Airborne						
Jet: Class I (50K ft) Class II (70K ft) Class III (100K ft) Class IV (100K ft)		-54 to +55 °C -54 to +71 °C -54 to +95 °C -54 to +125 °C	10 g pk max 20–2000 Hz 4–30 mW dwells 3 hrs max 7 g pk at 100 Hz	12.4	60	30 g pk, 11ms
Per MIL-E-5400 T PLSS Bomber (B-1)	-62 to +85 °C -62 to +95 °C	-54 to +71 °C -54 to +71 °C		20	5	39 g pk, 10.5 ms
Helicopter (A-129)	-62 to +85 °C	-54 to +55 °C	2 g from 14–33 Hz 5 g from 33–2000 Hz			(18) 1/2 sine pulses of 15 g pk value for 11 ms, 3 shocks each axis: Crash Safety: (12) 1/2 sine pulses of 30 g pk for 11 ms, 2 shocks each axis
Remotely Piloted Vehicle (RPV) (MICNS)	-57 to +71 °C					
Ground						
Unsheltered Uncontrolled	-57 to +68 °C	-51 to +68 °C				
Sheltered Controlled	-57 to +68 °C	0 to +49 °C				
Mobile (Sheltered) Uncontrolled	-57 to +68 °C	-40 to +55 °C				
Shipboard						
Unsheltered Uncontrolled	-57 to +68 °C	-28 to +65 °C	Type of MIL-STD-167-1			Grade A Type A Class I Shock Test, MIL-S-901
Sheltered Controlled	-57 to +68 °C	0 to +50 °C				
Manpak	-40 to +71 °C	-18 to +50 °C	5–500 Hz, 5 g max 30 min/resonance (4 total) per axis			3 ft drop on a steel plate, 1 drop per rate (6 faces)

1.2.2 Applicable Documents

The following list of documents is provided for reference.

1.2.2.1 Department of Defense

Publications are available from Naval Publications and Form Control, 5801 Tabor Road, Philadelphia, PA 19120

MIL-STD-202 Test Methods for Electronic and Electrical Component Parts

MIL-STD-210 Climatic Extremes for Military Equipment

MIL-STD-275 Printed Wiring for Electronic Equipment

MIL-STD-454 Standard General Requirements for Electronic Equipment

MIL-STD-781C Reliability Design Qualification and Production Acceptance Tests

MIL-STD-810D Environmental Test Methods

MIL-STD-883 Test Methods and Procedures for Microelectronics

MIL-STD-2000A Soldering Technology, High Quality/High Reliability

MIL-D-1000 Drawings, Engineering and Associated Lists

MIL-STD-1540B Test Requirements for Space Vehicles

MIL-E-4158E Electrical Equipment, Ground General Requirements for

MIL-E-5400T Electrical Equipment, Airborne, General Specifications for

DOD-E-8983 Electrical Equipment, Aerospace, Extended Space Environments, General Specification for

MIL-E-16400G Electronic, Interior Communication and Navigation Equipment, Naval Ship and Shore: General Specification for

MIL-S-19500 Semiconductor Devices, General Specification

MIL-P-28809 Printed Wiring Boards

MIL-M-38510 Microelectronic Devices, General Specification

MIL-P-50884 Printed Wiring, Flexible and Rigid-Flex

MIL-P-55110 Printed Wiring Boards

MIL-R-55342 Specification, Resistor, Chip

MIL-C-55681 Specification, Capacitor, Chip

MIL-C-83446 Specification, Coil, Chip

1.2.2.2 Institute for Interconnecting and Packaging Electronic Circuits

(IPC) Publications are available from IPC, 7380 N. Lincoln Avenue, Lincolnwood, IL 60646

IPC-T-50 Terms and Definitions

IPC-CM-78 Guidelines for Surface Mounting

IPC-SM-780 Guidelines for Component Packaging and Interconnection with Emphasis on Surface Mounting

IPC-SM-782 Surface Mount Land Patterns Configurations and Design Rules

IPC-S-804 Solderability Test Methods for Printed Wiring Boards

IPC-SM-840 Qualification and Performance of Permanent Polymer Coating for Printed Boards

1.2.2.3 Electronic Industries Association

Publications are available from EIA, 2001 Eye Street, N.W., Washington, DC 20006

JEDEC-95 JEDEC Registered and Standard Outlines for Solid State Products

RS-428 Type Designation System for Microelectronic Devices

RS-481 Tape and Reel Specification

1.2.3 References

Brice, K., "Direct Attachment of Leadless Chip Carrier to Various PWB Material," Heames Motorola Inc. Government Electronics Division

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Lichtenberg, L.R., "Comparison of Environmental Thermal Cycle Tests on Reflow Soldered Assemblies," Motorola Government Electronics Group

Riemer, D.E., "Power Cycling of Ceramic Chip Carriers on Ceramic Substrates (an Analysis of Test Results)," Boeing Aerospace Company Seattle, WA

Waller, D., "Analysis of Surface Mount Thermal and Thermal Stress Performance," Digital Equipment Corporation, Andover, MA

DCD #3834-141 AJ Modem—Environmental Matrix and Component Resonant Frequencies

IPC-CM-78 Surface Mount Considerations

L409C2022 B1 Performance Specification, Harris Corporation

Mantech Report—Some subassembly thermal life testing considerations, IBM

MICNS-FSM LCC Test Report, Harris Corporation

MIL-HDBK-217F Reliability Prediction of Electronic Equipment

PBS-1005 Environmental Requirements, Specification

PDMS Performance Specification, Martin Marietta

Surface Mount Critical Issues and Action Plans, Surface Mount Council, position paper

166863 A129 Helicopter Performance specification, Harris Corporation

1982 LCC/PIP Test Chart, Harris Corporation

1.3 Components

The surface mounted components described in this document are all qualified to military specifications. The majority of the components available to the industry meet vendor specifications only. There is a serious commitment by industry toward standardization. Every unique component considered for use must have its dimensional tolerances reviewed and its land pattern formula verified to ensure reliable solder joints. One should be aware that military standards allow for broad variations which may not be acceptable in your application.

1.3.1 General Requirements

Components must be capable of withstanding the applicable process which will be utilized in the manufacturing facility (i.e., vapor phase, IR reflow, vapor degreasing, etc.). When tape and reels are used, the requirements of EIA RS-481 must be met. Components susceptible to damage by electrostatic discharge shall meet static-sensitive handling procedures.

1.3.2 Passive Component Termination Requirements

Surface mount components are terminated with leads (leaded) and without leads (leadless). Most integrated circuits, multi-element type devices like resistor networks and semiconductor components are available in both configurations. Most discrete components such as resistors, capacitors, inductors and other two terminal type devices are typically leadless devices. Their electrical terminations are an integral part of the component body and they are designed for the part to be planar mounted to a substrate.

The materials used to make component leads for surface mount devices (SMD) are ductile electrically conductive metals. When the lead has to penetrate the component body wall of a ceramic package, Kovar is the material used to make the leads, because of coefficient of thermal expansion (CTE) compatibility to the component body (ceramic) and/or its ability to maintain the seal at the glass interface. The ceramic material is used to house the microchip device. In this configuration, the leads are cofired on the ceramic body, or embedded into a glass medium.

Another form of leaded SMD has the leads brazed onto the outer surface of the component body. These leads are stress relief formed and are compliant with the PWB substrate to which they are soldered. The lead materials used for this type of package do not need to have a matching CTE with the substrate. Therefore, other metals such as copper, beryllium copper, and phosphorus bronze can be used. However, these materials may not be compliant with MIL-M-38510. They must be plated with another metal in order to protect the base material from oxidation and to improve and maintain solderability. Several different platings and/or coatings may be required. Kovar

typically requires a nickel flash, followed by gold plating. Some of the other materials may only require a tin/lead solder coat. Figure 1.3.2 illustrates several standard lead configurations.

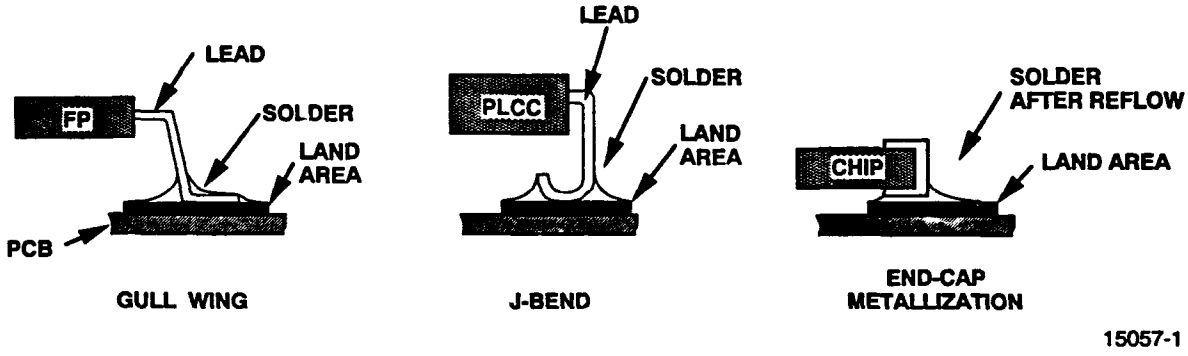

Figure 1.3.2. Lead Configurations

Leadless SMD's are manufactured by a co-firing process. Tungsten (W) metalization is sintered onto the component body connection locations. Nickel is plated on the exposed W electrode, then gold is plated over the nickel.

1.3.3 Discrete Passive Devices

These devices originated in the hybrid industry. A brief explanation of common devices follows:

1.3.3.1 Resistors

Surface mount resistors are grouped into two major categories—chip type devices and metal electrode face-bonded (MELF) devices.

The chip resistors are manufactured by thick or thin film processes. A resistive material is deposited onto a rectangular ceramic substrate with palladium-silver conductive pads

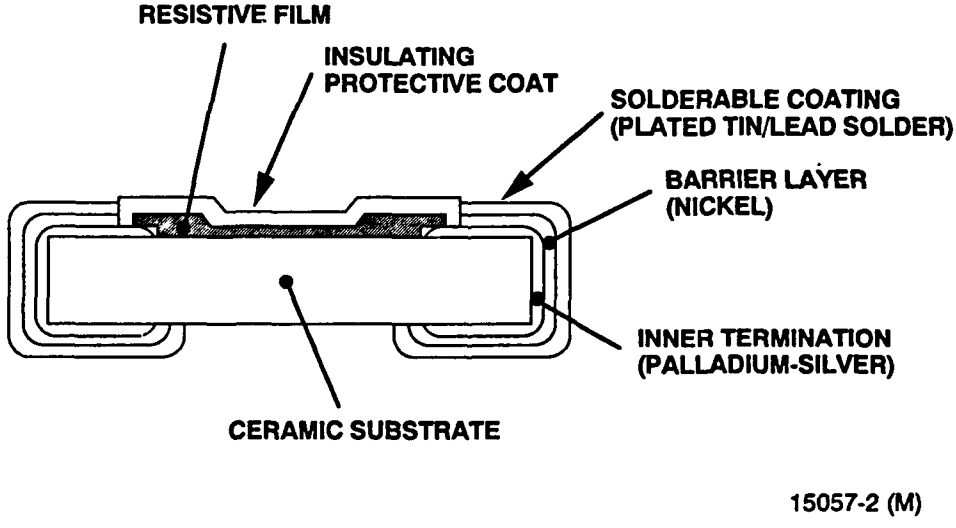

Figure 1.3.3.1-1. Chip Resistor Construction

(terminations). The resistor is trimmed to a desired value and coated with an insulative material. The terminations should be electroplated with nickel and tin/lead solder to prevent silver leaching during reflow.

The MELF type resistors are cylindrical by design, similar to conventional style leaded resistors, except they have no leads. Resistive carbon film or metal film is deposited onto a ceramic core, and caps (metal electrodes) are added to the ends. The resistor is then trimmed to a desired value and sealed with an insulative material. MELF's are not recommended because the cylindrical bodies are not MIL certified and are hard to handle in terms of pick and place equipment.

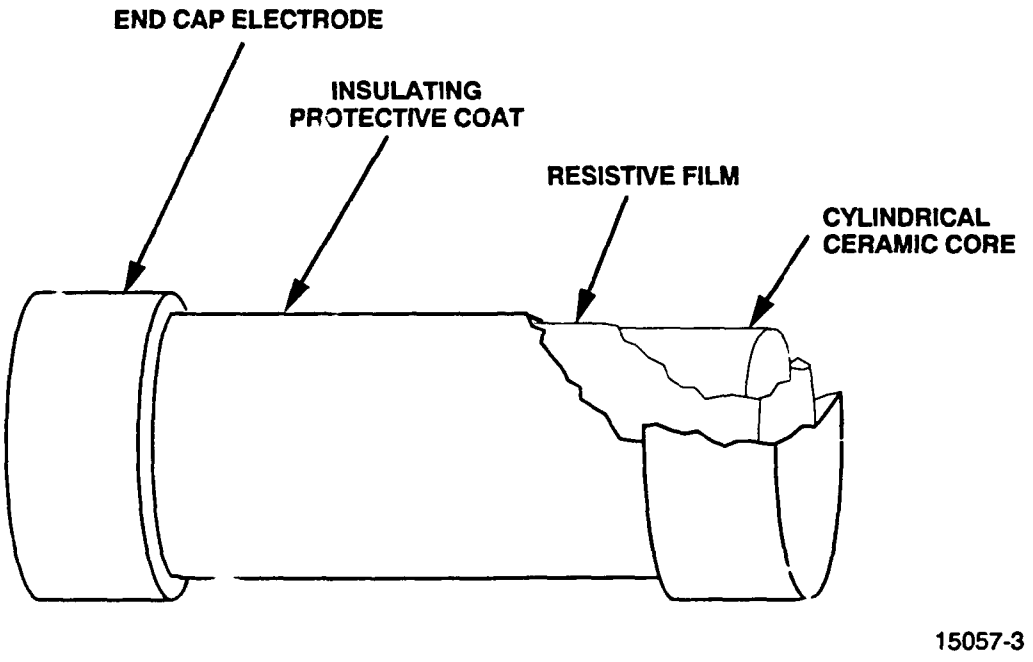

Figure 1.3.3.1-2. Metal Electrode Face Bonding (MELF) Resistor

1.3.3.2 Capacitors

Ceramic (dielectric) chip capacitors are constructed of alternating screened metalized ceramic layers, sintered into one monolithic structure. Typically palladium-silver is the metal screened onto the green ceramic to create the inner electrodes. It is also commonly used for the termination (the outer electrodes), because economically it is one of the least expensive noble metals to work with. These palladium-silver terminations in turn have to be nickel-plated and then tin or tin/lead solder-coated to prevent silver leaching during solder reflow.

Tantalum (electrolytic) chip capacitors are available in a variety of different types and sizes, but they are not being addressed in this study at this time.

1.3.3.3 Inductors

Chip inductors are constructed of a magnet wire wound bobbin epoxied to a ceramic substrate with metalized termination pads (either palladium-silver, silver/nickel barrier/gold, silver/

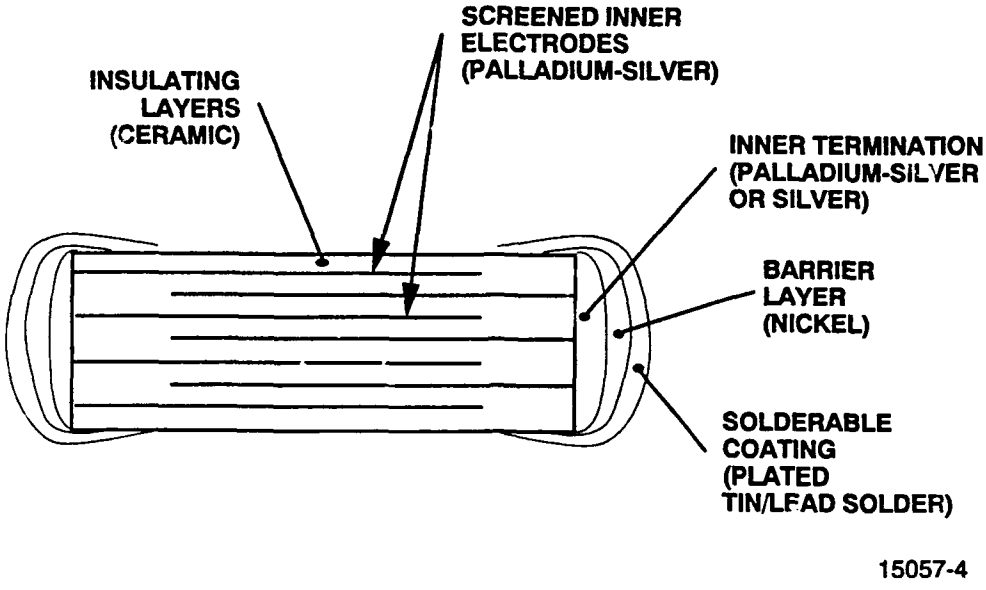

Figure 1.3.3.2. Chip Capacitor (Dielectric)

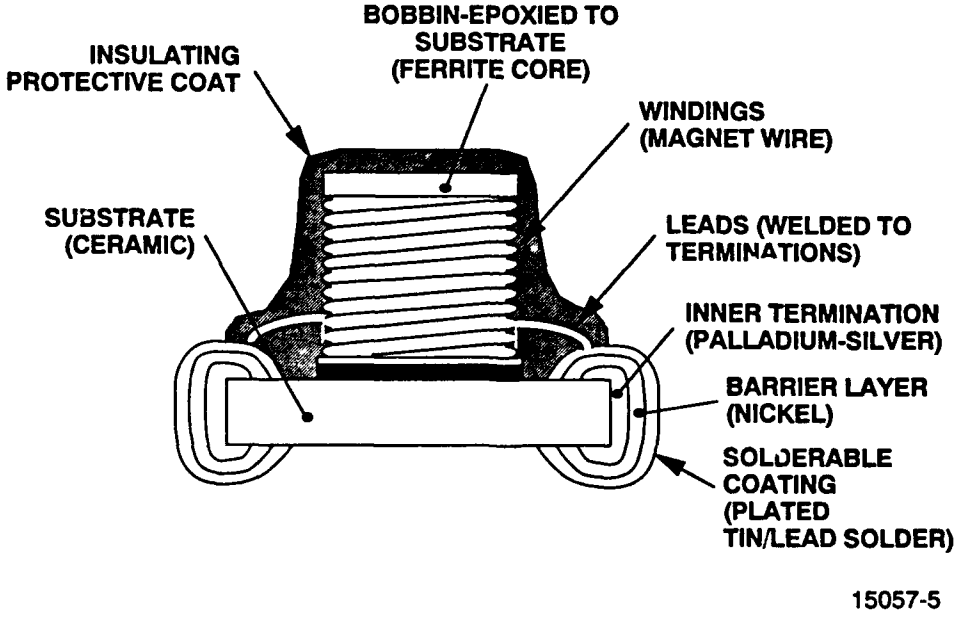

Figure 1.3.3.3. Chip Inductor

nickel barrier/tin lead coat, or silver/nickel barrier/electroplated tin lead). The wire ends are welded to the pads and the completed assembly is conformally coated.

1.3.4 Small Outline Transistors

At the present time there are no qualified military specifications covering small outline transistors. The industry has established two common packages for commercial use. SOT-23 and SOT-89 will be the baseline used to establish a military version surface mount transistor. These devices are plastic and consequently are not hermetically sealed.

1.3.5 Integrated Circuits

Surface mounted integrated circuits can be either a leaded or a leadless device. These devices can also be hermetically (ceramic packages) or nonhermetically (plastic packages) sealed. This study will not address the plastic packages.

There are several types and styles of leaded packages that are defined in MIL-M-38510 that can be considered as surface mount devices. Flatpacks and cer-packs with formed leads, ceramic quad and multilayer ceramic packages with either gull or "J" formed leads, and dual-in-line packages (DIP) when their leads are trimmed to the seating plane and butt soldered to a substrate without aid of plated-through-holes. See Section 1.3.2 for discussion on lead material and plating.

Leadless chip carrier packages (LCC) as defined per MIL-M-38510 can be square or rectangular in shape. The LCC die (microchip) cavity may vary in size, but the body envelope is controlled by MIL-M-38510. Reference Section 1.3.2 for discussion on pad metalization and platings.

1.3.6 Miscellaneous Components and Connectors

There are many styles and vendors available for surface mount connectors. Each usually has its own recommended land pattern and mounting technique defined by its specification.

There are other devices available, notably diodes, which are not covered in this document at this time. Do not limit your consideration to only those covered herein.

1.3.7 Aftermarket Lead Attachment (AMLA)

Various SMT studies have convincingly shown that soldering LCC's (leadless ceramic chip carriers) to unconstrained printed wiring boards falls far short of meeting military requirements. Since many semiconductor vendors supply their product in LCC packages, or, where a design may exist which unsuccessfully utilized LCCs, a means of adding compliant leads to these packages with IC's already mounted and the packages sealed was addressed. Of the several approaches to lead attachment, the present industry direction, thermocompression bonding of copper leads, is recommended. The copper leads, short 14 mil diameter wire, are thermocompression bonded to the metalized castellazations of the package. The leads are then formed by tooling dies to the configuration of choice (Figure 1.3.7) and then solder dipped to complete the process.

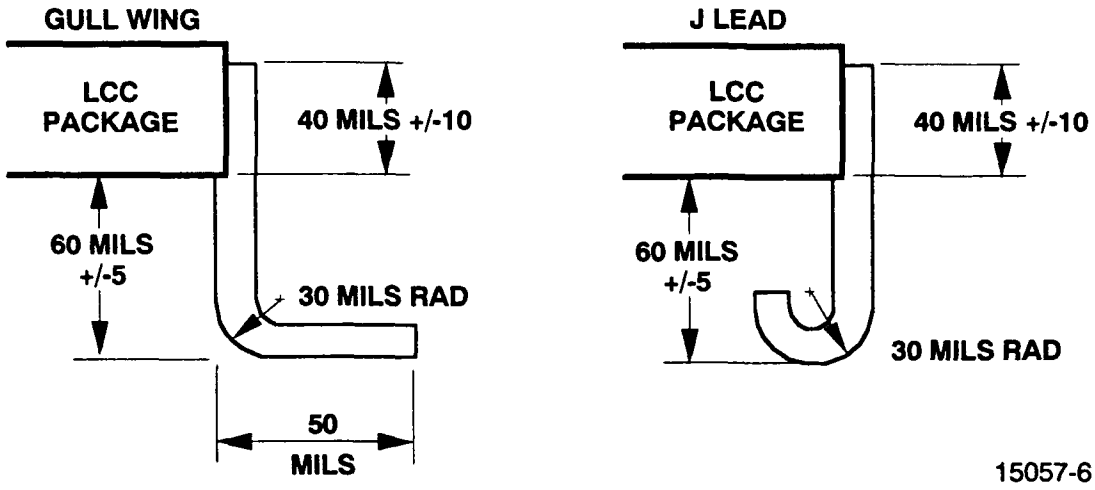

Figure 1.3.7. Typical Lead Detail of AMLA

1.4 P Types and Selection

SMT consists of mounting devices to the surface of a PWB either through short leads or directly to device terminations. In the case of leadless devices, the elimination of leads also eliminates the compliance that these leads provide during thermal cycling of PWB assemblies. For leadless devices there are currently two approaches to the compliance issue; match the CTE of the device to the PWB or increase the compliance of the PWB by effecting its Modules of Elasticity. This section deals with the selection of Packaging and Interconnect Structures (P&IS) for applications requiring controlled expansion of the structure. There are significant cost considerations when chosing a packaging and interconnect structure and ample study should be given to the tradeoff between reliability versus cost.

1.4.1 General Requirements and Design Issues

There are numerous design parameters related to material properties that must be considered when selecting a particular Packaging and Interconnect Structure (P&IS) design (Table 1.4.1). One of the most significant material properties is the coefficient of thermal expansion (CTE). The CTE mismatch between SMD's and the P&IS cause solder joint failures in the form of fatigue cracks. Solder joint fatigue is caused by thermal shock, thermal cycling, and power cycling. Minimizing the CTE differential between the component and the board improves solder joint reliability. Industry data indicates that the board CTE should be 1-2 ppm/°C above that of the ceramic components. This technique should account for the thermal gradient between the part and the board during operation. The lesser the gradient, then the less CTE mismatch present.

When selecting a P&IS on which leadless chip carriers or other non-leaded surface mount parts are used, it is advantageous to understand what the approximate CTE is for the P&IS. This is done by taking into account the individual constituent CTE's and modulus of elasticity in the

X & Y planes. See Examples 1.4.1-1 through 1.4.1-4 in the back of this section for sample stack-ups and CTE calculations. Numerous methods are available. "Maximum" or "average" CTE's can be calculated depending on which equation is used. The "maximum" equation is used for looking at a one-dimension cross-section of the board while the "average" method distributes all materials evenly in volumetric calculations. The two equations are shown below.

METHOD #1, MAXIMUM CTE VALUE:

$$E_c = \%t_1(E_1) + \%t_2) + ...$$

$$\alpha_c = [(\%t_1)(E_1)\alpha_1) + (\%t_2(E_2)\alpha_2) + ...]/E_c$$

Where: E_c = composite modulus of elasticity
E_1 = modulus of elasticity for material 1
E_2 = modulus of elasticity for material 2
α_1 = CTE of material 1
α_2 = CTE of material 2
α_c = CTE of the composite PCB
$\%t_1$ = percentage of material 1 thickness relative to overall composite thickness

METHOD #2, AVERAGE CTE VALUE:

$$\alpha_c = \frac{(\alpha_1 x E_1 x V_1) + (\alpha_2 x E_2 x V_2) + ...}{(E_1 x V_1) + (E_2 x V_2) + ...}$$

Where: E = modulus of elasticity
α = CTE
α_c = CTE of the composite PCB
V = X time Y times thickness

In calculating the CTE's of the composites, the degree of accuracy depends on how much detail is considered. Adding the soldermask and conformal coating can have measurable effect. In the "average" method, subtracting the holes from the volume as well as including the copper plating in the barrel of the hole can result in a more exact number.

1.4.1.1 "J" Factor

Another parameter that may be an indicator of solder joint reliability for leadless components is called the "J" factor. It yields a number that should be proportional to the shear stress generated in the solder joint. A lower "J" number should result in lower stresses and therefore an increase in solder joint life. The equation follows.

EQUATION

Where: J = $\Delta \alpha$ x E
$\Delta\alpha$ = CTE of P&IS - CTE of ceramic LCC (6.4 ppm/°C)
E = Modulus of elasticity of composite board

Examples are presented in Table 1.4.1.1.

Table 1.4.1. Packaging and Interconnect Structure Selection Considerations

DESIGN PARAMETERS	TRANSITION TEMP	COEF OF THERMAL EXPAN	THERMAL CONDUCTIVITY	TENSILE MODULUS	FLEXURAL MODULUS	DIELECTRIC	VOL RESISTIVITY	SURFACE RESISTIVITY	MOISTURE ABSORPTION
TEMP & POWER CYCLING	X	X	X	X					
VIBRATION				X	X				
MECH SHOCK				X	X				
TEMP & HUMIDITY	X	X				X	X	X	X
POWER DENSITY	X		X						
CHIP CARRIER SIZE		X		X					
CIRCUIT DENSITY						X	X	X	
CIRCUIT SPEED						X	X	X	

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Table 1.4.1.1. "J" Factor Calculated Values

COMPOSITE BOARD W/COPPER INCLUDED	E(PSI $x10^6$)	P&IS CTE (PPM/°C)	Δ CTE(PPM/°C)	"J" FACTOR
EPOXY/GLASS	5.1	16.2	9.8	49.98
POLYIMIDE/GLASS	6.1	14.75	8.35	50.90
POLYIMIDE/KEVLAR (7293)	5.5	9.4	3.00	16.50
POLYIMIDE/GLASS W/ CIC	8.3	8.95	2.55	21.16
RO 2800	2.8	16.70	10.30	28.80
RO 28000 W/ CIC	5.2	8.80	2.40	12.48

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1.4.1.2 Other Design Issues

Other design related issues of significance are weight, thermal dissipation characteristics, electrical performance characteristics, and cost. Thermal dissipation needs are greater in SMT designs as parts are smaller and more can be placed per square inch. SMT can also provide enhanced circuit performance (see Section 1.7), over conventional through-hole technology as well as improving the overall system performance and efficiency. Some new board

technologies can cost as much as fifteen times a standard G-10 board, however, the reduction in size and weight imparts a total cost advantage over conventional packaging.

1.4.2 P&IS Types

The packaging and interconnect structure types are classified into three main categories; constrained dielectric, constrained core, and unconstrained. Discussion of each type with examples are provided in the following paragraphs. In addition, Table 1.4.2 provides information on each type of material with advantages and disadvantages identified.

1.4.2.1 Constrained Dielectric

This technique involves the use of a substrate dielectric material that has a natural CTE close or equivalent to that of ceramic chip components or includes a low or negative CTE fiber reinforcement. The following paragraphs explain three common examples.

1.4.2.1.1 Ceramic Substrates

Ceramic has been used in hybrid manufacture and as small PWB's for many years. The major advantage is the CTE match with components. The major disadvantages are size limitations, cost, and its brittle nature. It has been found through industry testing experience and other industry data that solder joints on LCC's mounted to ceramic will crack after thermal cycling although CTE matched. Ceramic boards tested with 84-pin LCC's attached have cracked after 330 cycles of -55 to +125 °C. It can be inferred from this data that matching CTE's (ref. 1.4.6.11) alone does not necessarily provide for high reliability solder joints.

1.4.2.1.2 Kevlar® Composites

Kevlar® is an aramid fiber developed by DuPont which is combined with standard resin systems in varying combinations. The negative CTE of the fiber allows for a CTE match of ceramic when it is mixed with polyimide or epoxy resins. Processing is the same as G-10 or polyimide with the exception of bake cycles and drill types and speeds. The material is more difficult to drill and is also very prone to moisture absorption. Plasma etching must be used after drilling in order to remove the frayed and smeared Kevlar® fibers from the holes prior to plating. Microcracking of the resin occurs and has raised concerns about trace conductor reliability. To date no failures have been tied to this phenomenon. Companies, like Martin Marietta, General Electric, Hughes, and McDonnell Douglas, have developed and used Kevlar® composites with success in military applications. They have accepted the process difficulties and higher costs. Kevlar® composites have a significantly lower "J" rating than most materials.

1.4.2.1.3 Quartz Composites

Quartz fibers are another low CTE material that is combined with polyimide or epoxy to result in a compatible board material that has a CTE in the range of 6–7 ppm/°C. Resin content and copper bring it up to 12–14 ppm/°C. It requires standard PWB processing but drill life is somewhat shorter. The major disadvantage is that it costs fifteen times more than G-10 boards.

Table 1.4.2. Interconnect Structures Comparison

Type	Major Advantages	Major Disadvantages	Comments
Epoxy-fiberglass—unconstrained	Substrate size, weight, rework, dielectric properties, conventional board processing	Thermal conductivity, X & Y CTE	Because of high X & Y CTE, it should be limited to environments and application with small changes in temperature and/or small packages
Polyimide fiberglass—unconstrained	Same as epoxy glass plus high temperature Z axis CTE, substrate size, weight, rework, dielectric	Thermal conductivity X & Y axis CTE, moisture absorption	Same as epoxy fiberglass
Fiberglass/Teflon laminates—unconstrained	Dielectric constant, high temperature	Same as epoxy fiberglass, low temperature stability, thermal conductivity, X & Y axis CTE	Suitable for high speed logic applications, same as epoxy fiberglass
Compliant surface layer—unconstrained	Substrate size, dielectric properties, X & Y axis CTE	Z axis CTE, thermal conductivity	Compliant layer absorbs difference in CTE between ceramic package and substrate
Alumina (ceramic)—constrained dielectric	CTE, thermal conductivity, conventional thick film or thin film processing, integrated resistors	Substrate size, rework limitations, weight, cost, brittleness, dielectric constant	Most widely used for hybrid circuit technology
Epoxy aramid fiber (KEVLAR®)—constrained dielectric	Same as epoxy fiberglass, X & Y axis CTE, substrate size, lightest weight, reworkable, dielectric properties	Thermal conductivity, X & Y axis CTE, resin microcracking, Z axis CTE, water absorption Potential plated through-hole cracking resulting from Z axis CTE	Volume fraction of fiber can be controlled to tailor X & Y CTE, resin selection critical to reducing resin microcracking
Polyimide aramid fiber (KELVAR®)—constrained dielectric	Same as epoxy aramid fiber, substrate size, weight, reworkable, dielectric properties	Thermal conductivity, X & Y axis CTE, resin microcracking, water absorption Potential plated through-hole cracking resulting from Z axis CTE	Same as epoxy aramid fiber
Polyimide quartz (fused silica)—constrained dielectric	Same as polyimide aramid fiber, no surface micro-cracks, substrate size, weight, reworkable, dielectric properties	Thermal conductivity, X & Y axis CTE, water absorption, process solution entrapment, cost Potential plated through-hole cracking resulting from Z axis CTE	Resin microcracks are confined to internal layers and cannot damage external circuitry
Porcelainized C/I/C—constrained	Same as Alumina	Reworkable compatible with thick film materials	Thick film materials are still under development
Polyimide with C/I/C core—constrained	X & Y axis CTE; stiffness, thermal conductivity	Weight, PTH reliability is less, two sides mounting of components Potential plated through-hole cracking resulting from Z axis CTE	Thickness of core can be varied to tailor CTE
Polyimide with graphite fiber core—constrained	Stiffness, thermal conductivity, low weight	Cost Potential plated through-hole cracking resulting from Z axis CTE	Tailoring of CTE
Polyimide with C/I/C distributed plane—constrained	Be used for power and X & Y axis CTE, foil can be used for power and ground	Weight, PTH processing is more difficult Potential plated through-hole cracking resulting from Z axis CTE	Foil layers can be used in varying positions in stackup but must be symmetrical

1.4.2.2 Constrained Core

The constrained approach requires the use of a low CTE metal core or foil to be used with the laminate and resin materials. It is usually laminated during the PWB process, although bonding is sometimes used. The two main variations of this technology are to use a core of metal in the middle of the laminate system or to use distributed planes of thinner material which are utilized for power and ground.

1.4.2.2.1 Restraining Core

This technique appears to be the most popular of the constrained approach. The core materials are usually copper/invar/copper (CIC) and to a lesser extent, copper/molybdenum/copper. The core can be used for grounding as well as CTE control. The dielectric materials are typically G-10 or polyimide. Exotic applications such as porcelain on a core have been found. The core material must be drilled for clearance holes such that plated through-holes (PTH) can be fabricated. The thickness of dielectric must be balanced on either side of the core in order to prevent warpage, even if components are to be mounted on only one side. Figure 1.4.2.2.1 illustrates this design.

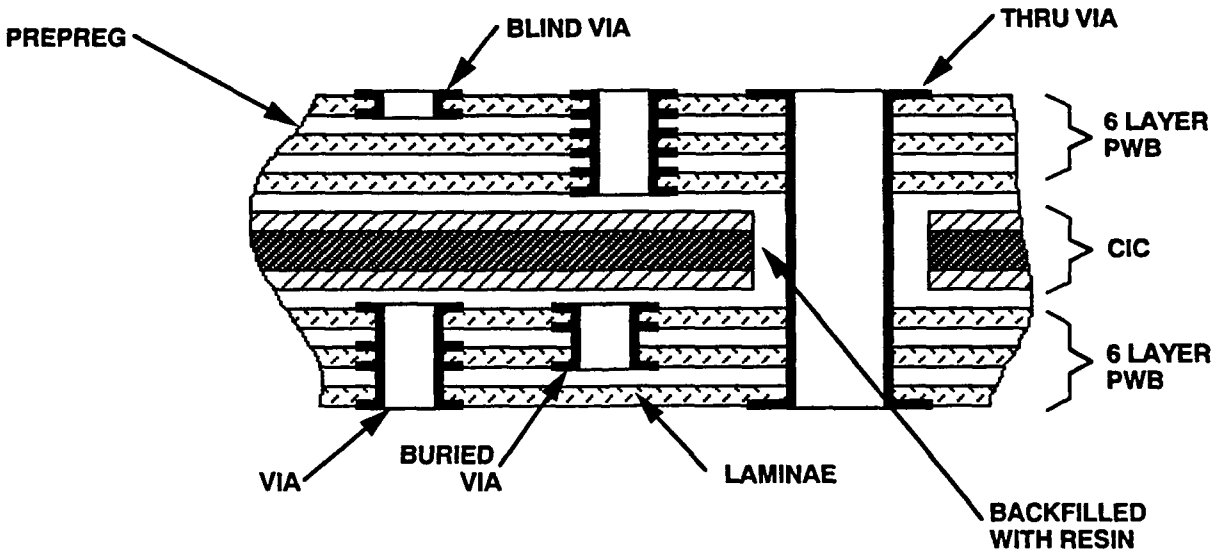

Figure 1.4.2.2.1. Constrained Core Approach

If double-sided component mounting is required, then it becomes possible to assemble the individual boards first and bond the two assemblies together after testing. Process considerations need to be reviewed to determine if component assembly should be done before or after bonding.

1.4.2.2.2 Distributed Planes

This approach utilizes two foil layers of CIC or similar material in the range of 5–10 mils thick. These layers are placed symmetrically in the stack-up to prevent warpage (Figure 1.4.2.2.2). These foils function as power and ground planes. In the case of CIC, this means plating

to the invar to create a via. This is a problem, as Invar does not plate easily. There are numerous processes that enhance the platability of Invar. Preplating the hole with nickel has proven to be successful. According to PWB fabrication houses, there are other proprietary processes that also are effective. Difficulties have been encountered with the bondability of CIC to the PWB laminates. Solutions have been developed to overcome this problem and should be well understood by the PWB vendor before committing to him.

This approach is lightweight and uses standard manufacturing processes as compared to the core method. It is not capable of dissipating as much power. Tradeoffs should be studied prior to implementing a particular constrained approach.

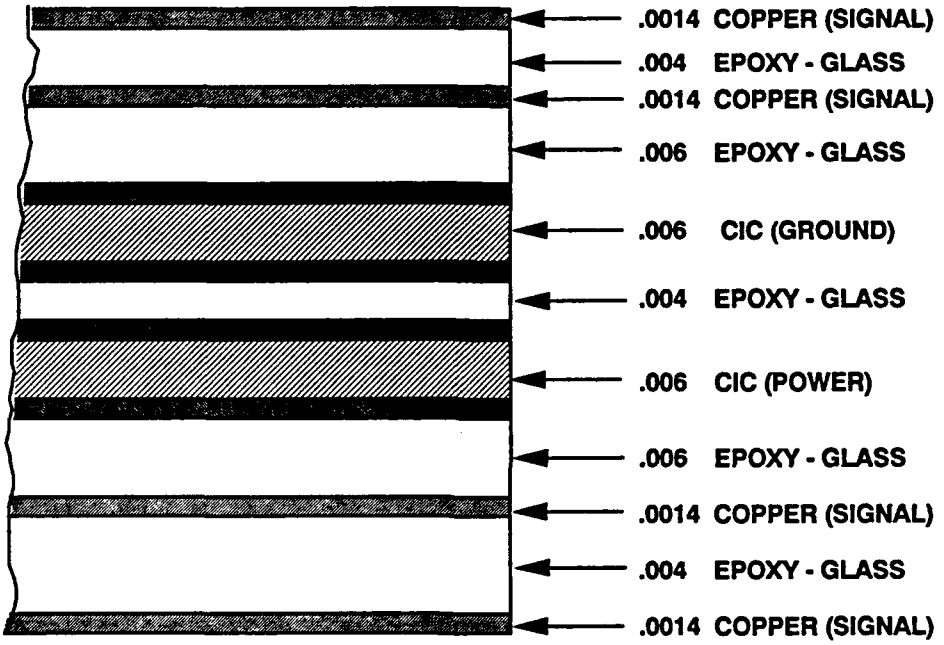

Figure 1.4.2.2.2. Distributed Planes of Atypical CIC Substrate

1.4.2.3 Unconstrained

There are applications where normal printed wiring board materials can be used effectively and reliably in conjunction with surface mount components. Leadless chip carriers can be used with G-10 or polyimide if the pin-out count is small and the thermal cycle range is narrow. A low number of thermal cycles improves the possibilities of using G-10.

Leaded chip carriers and flatpacks have been used successfully in many applications with G-10 PWB's. The compliance of the leads absorbs the majority of the stress rather than the solder joint. The trend with leaded chip carriers is to increase the I/O count within a given area by reducing the lead size and spacing significantly. This trend is driven by the increased I/O count requirements of VHSIC, VLSI, gate array, and application specific integrated circuits (ASIC).

Another method is the use of thick solder joints. This has been done by using copper balls to act as spacers, solder columns as offered by Raychem, or simply supporting the chip carrier

off the board with polyimide or kapton spacers. The solder volume is increased at deposition to compensate for the increased height when using spacers. Manufacturing process considerations must be considered with these techniques and testing perfortmed to determine ultimate relaibility.

One other technique that has been used with some success is to use a highly compliant top surface layer. This compliant layer reduces the stress in the solder joint by not supporting the strain load. A European development called Exacta "Chipstrate" uses a nitrile rubber coating. This technique appears to have promise but is proprietary at this time.

1.4.2.4 New Developments

There are numerous PWB materials and new combinations of materials that are being investigated and evaluated in the industry either privately or through government-funded manufacturing technology development activities. The Mantech program has evaluated a number of Kevlar® composites and Quatrex® materials. The results of their evaluations are available in the Industry Review Proceedings.

Another new material that shows significant promise is a ceramic-filled teflon from Rogers Corporation, named R0-2800. This material has a low dielectric constant and a very low modulus of elasticity. The CTE is approximately the same as G-10. However, if the amount of copper in the board is minimized and a thin core of copper/Invar/copper is added, the CTE becomes significantly lower and the "J" factor lower than Kevlar® results. This is a new material and requires a high temperature press to laminate the boards; equipment that few PWB fabrication vendors possess at this time. The equipment required is a high temperature press used to laminate the boards. The material has potential and may emerge as a high-speed surface mount candidate.

1.4.3 Material Parameters and Characteristics

A list of material properties and parameters are displayed in Table 1.4.3-1. The material properties of the various PWB materials do not include the effect of copper. As an example, the CTE for Polyimide Kevlar is identified as 3.4 to 6.7 depending on the percentage of resin. If copper for ground planes and traces is added, the CTE can go as high as 11 ppm/°C.

Table 1.4.3-2 contains associated material properties that are necessary for working up CTE's on composite boards.

1.4.4 Comments

All of the parameters identified in Tables 1.4.3-1 and 1.4.3-2 should be considered when selecting a P&IS system for a leadless surface mount application. It is difficult to satisfy all of the packaging, environmental, and customer requirements with one material system. As an example, a Polyimide/Kevlar P&IS may be chosen to address the solder joint reliability issue, but at the same time it may not provide the thermal dissipation necessary.

Another consideration is that Z axis expansion affects the reliability of plated through-holes. It has been discovered that materials constrained in the X and Y directions for CTE matching may have significantly different CTE's in the Z direction. Additionally, high I/O part patterns require smaller diameter vias and more interconnect layers, which therefore increases the hole to board

thickness aspect ratio. The higher the ratio is, the lower the PTH reliability becomes. The Z axis expansion issue coupled with the small vias degrades the reliability of the design. It has been shown, that completely filling vias with solder (no voids) improves the life of PTH's, however, the most reliable via is one that has no solder in it at all. None of this is new, but when one no longer has a need to place a lead in a hole, one is tempted to drill as small a hole as possible. SMT does not give us license to violate traditional design guidelines for PTH diameters. Use a 3 to 1 aspect ratio, or less, wherever possible.

For surface mount applications where the CTE of the board is a significant parameter, (i.e., leadless devices), the CTE should be calculated in the design stage and possibly characterized through measurements during the prototype stage. A P&IS will have different CTE values in different areas due to copper distribution. It may be important to have a CTE map of the board to compare with the types of SMD's in each location.

There are numerous techniques for making CTE measurements. Three methods are the Thermo-Mechanical Analyzer (TMA), strain-gauges, and the dilatometer. The TMA is well suited for Z axis measurements as thin samples are its forte. It requires two flat parallel surfaces in which contact is made. The strain-gauge technique is best suited for localized in-plane measurements. These measurements can be made by placing them directly on a PWB in areas of minimum or maximum copper to measure variations. The technique that yields an average CTE in the X, Y plane is the dilatometer. This instrument uses a coupon size of approximately 1/2 x 1". The results are representative of the length dimension. There may be cases where all three techniques are used to characterize the design for a specific application. The importance of the CTE in the X, Y, and Z axis cannot be over- emphasized for the surface mount designs in high reliability applications using leadless components.

Studies have indicated that leaded SMD's have high reliability in thermal cycle, shock, and vibration. Experience with flatpacks backs this up. The path of technology, which has been embraced, has been from chip caps and resistors followed by low pin count LCC's to high pin count VLSI devices. As industry progresses through these technologies, the demands on the P&IS increase.

Table 1.4.3-1. Substrate Materials Properties

Parameter/Factor	Substrate Material				
	Glass Epoxy G10- & FR-4	Ceramic (Alumina)	Polyimide Glass	Polyimide/ KEVLAR® Corlam #7293	Epoxy/ KEVLAR® Corlam #4093
X&Y CTE (ppm/°C)	12.8–16	6.4	11.7–14.2	3.4–6.7 (6.0)	6–7
Z CTE (ppm/°C)	189	6.4	60	83 (5L)	62
Δ CTE from LCC (X&Y) x 10^{-6}	6.4–9.6	0	5.2–7.8	-3 to 0.3	0.4–1
Thermal cond. (W/M/°K)	0.18	20 Btu	0.17	0.12	0.12
XY tensile MOD (PSI x 10^6)	2.5	40	2.8	4.0	4.4
Glass transition temp °C	125	N/A	250	185	135
Density (lb/in^3)	0.065	0.13	0.066	0.06	0.054
Moisture absorption (%)	0.10	–	0.35	1.5	1.5
Dielectric constant (At 1 MHz)	4.8	9.4	4.8	3.33	3.9
Vol. resist (ohms/cm^3)	10^{12}	–	10^{14}	10^{12}	10^{16}
Max. # of layers	30	30	30	15	15
Min. layer thick (mils)	3	4	3	4	–
Max. board thick (mils)	250	100	200	100	–
Smallest line width (mils)	4–6	3–4	4–6	4–6	–
Smallest hole (mils)	8–10	4	8–10	8–10	8-10
Peel strength (lb/in^2)	–	–	–	6 lbs/in^2	7
Max physical size	30" x 30"	6" x 6"	18" x 18"	18" x 18"	18" x 18"
Cost factor FR4 = 1x	1X	6X	1.5X	5–6X	4X
(–) Not available at time of publication or vendor specific					

Table 1.4.3-1. Substrate Materials Properties (Continued)

Parameter/Factor	Substrate Material						
	Polyimide/ Quartz	Teflon Fiberglass	Quatrex 5010/Quartz 525 C/I/C	BT-Epoxy/ KEVLAR® (120) (Bonded)*	Corlam 5010™ (Quatrex 5010/KEVLAR® 108)	Polyimide/ Glass With 6 mil Power and Ground Planes Cu/In/ Cu	RO-2800B
X&Y CTE (ppm/°C)	8.9	20	9–10.5	10.0*	6–7.5	9.5	16
Z CTE (ppm/°C)	36–50	–	65	>80	95	60	24
Δ CTE from LCC (X&Y) x 10^{-6}	2.5	13.6	2.6–4.1	3.6	-0.4–1.5	3.1	9.6
Thermal cond. (W/M/°K)	0.30	0.26 W/M/K	–	–	–	0.17	0.44
XY tensile MOD (PSI x 10^6)	–	0.2	–	–	–	–	0.12
Glass transition temp °C	270	75	–	182	–	250	–
Density (lb/in^3)	–	–	0.079	–	0.047	–	0.072
Moisture absorption (%)	0.4	1.1	0.7	1.2–1.4	2.1	0.35	0.13 max.
Dielectric constant (At 1 MHz)	3.6	2.3	3.8	3.4–3.8	3.8	4.8	2.9 @ 10 GHz
Vol. resist (ohms/cm^3)	10^8	10^{10}	–	–	–	10^{14}	10^{12}
Max. # of layers	15	30	–	–	–	30	10+
Min. layer thick (mils)	4.0 mils	4 mils	6	4	4	3	5
Max. board thick (mils)	100 mils	100 mils	–	–	–	200	100+
Smallest line width (mils)	4–6	4–6	6	6	6	4–6	5
Smallest hole (mils)	8–10	8–10	8	–	–	8–10	–
Peel strength (lb/in^2)	8	–	3.6	4.8–6.0	3.2	–	89.5(5)
Max physical size	18" x 18"	18" x 18"	–	–	–	18"x18"	24 panel
Cost factor FR4 = 1x	15x	–	–	–	–	3.0x	2–3x
(–) Not available at time of publication or vendor specific							

Table 1.4.3-2. General Material Properties

Material, Assume 0.025" THK	CTE (ppm/°C)	Δ of CTE From LCC (ppm/°C)	Thermal Cond (Btu/hr·ft·°F)	Density (lb/in^3)	XY (psi x 10^{+6}) Tensile Modulus	Equiv. Thermal Perf. to Alum.
Aluminum	23.7	17.3	135	0.098	10.0	1.0
Copper	17.6	11.2	226	0.323	17.0	1.7
BEO	5–7	-1.4 to 0.6	120	0.10	39	0.9
Gold	17	11.6	172	0.692		1.3
Silicon	4.2–6	-2.2 to 0.4	85	0.084		0.6
Steel	10	3.6	27	0.283	30	0.2
Molybdenum	5.0	1.4	85	0.396	40	0.63
Titanium	7.9	1.5	10		16	0.074
Alloy 42 (Fe/Ni/Sn)	4.6	-1.8	8.8	0.293	21	0.07
Kovar/(Fe/Ni/Co)	5.8	-0.6	7.7	0.302	20	0.057
Cu/ In/Cu (12.5/75/12.5)	4.6	-1.8	61	0.301	19.6	0.45
CuCLAD Molybdenum	6.0	-0.4	105	0.355	33	0.78
Thermoplastic Resin	25–30	18.6–23.6	–	–	3–4	–
63/67 Solder @ 23 °C	22	15.6	28.9	0.32	2	0.21

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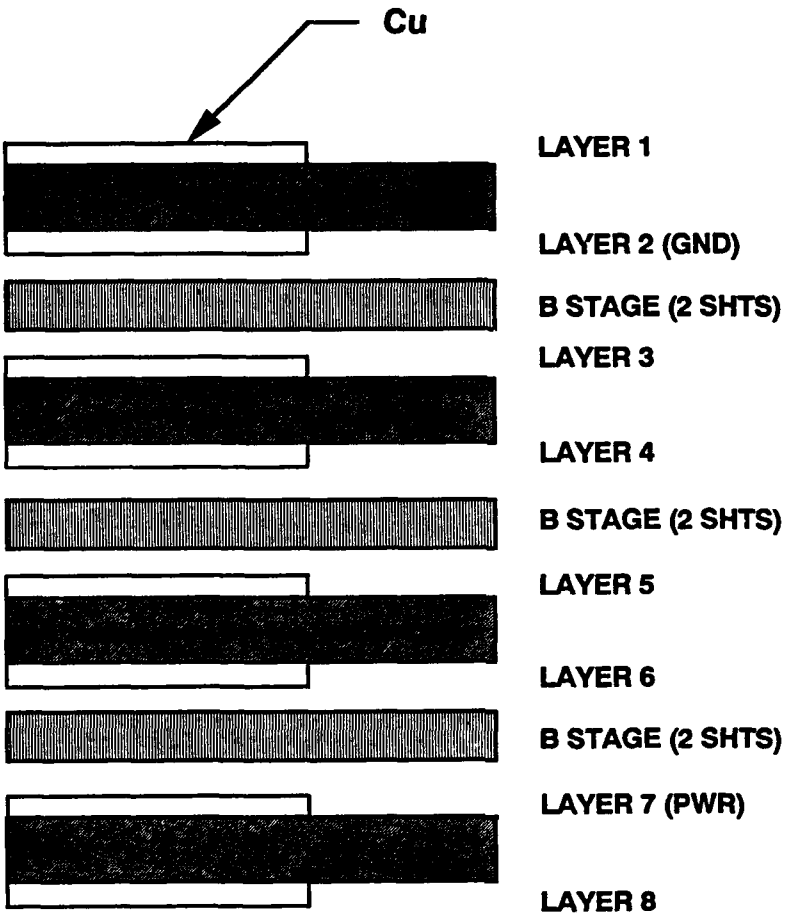


C STAGE: (4 PIECES) x (0.008) = 0.032 INCH
B STAGE: (6 PIECES) x (0.003) = 0.018 INCH
COOPER 1/1: (8 LAYERS) x (0.0014) = 0.011 INCH
0.061

POLYIMIDE:

AVG CTE = 14.7 PPM/°C MAX CTE = 15.4 PPM/°C

G-10

AVG CTE = 16.2 PPM/°C MAX CTE = 16.4 PPM/°C

15057-11 (M)

Example Figure 1.4.1-1. Standard G-10 and Polyimide

CTE Calculations for Epoxy/Glass

		Maximum CTE		CU	Epoxy
C-Stage	: 0.032	E		17.0	2.5
B-Stage	: 0.018	a		16.8	15.8
	0.050	= 82% of Total Thickness			
Copper	: 0.011	= 18% of Total Thickness			
	0.061	Nominal Thickness			

$E_C = 0.18\ (17.0) + 0.82\ (2.5) = 3.06 + 2.05 = 5.11$

$a_c = [3.06\ (16.8) + 2.05\ (15.8)]/5.11 = 16.4$ PPM/°C

Average CTE

Composite : $V_c = 4$ in x 4 in x 0.061 in $= 0.976$ in^3 Assume: 4 in x 4 in Board

Copper : V_1 = (4" x 4") (6 layers) (0.0014) (25% coverage) + (4" x 4") (2 layers) (0.0014) (90% coverage) = 0.074 in^3

G-10 : $V_2 = V_c - V_1 = 0.976 - 0.074 = 0.902$ in^3

$$a_c = \frac{(16.8 \times 17.0 \times 0.074) + (15.8 \times 2.5 \times 0.902)}{(17.0 \times 0.074) + (2.5 \times 9.02)} = 16.2 \text{ PPM/°C}$$

CTE Calculations for Polyimide/Glass

	Maximum CTE		CU	Polyimide
Polyimide	: 0.050 = 82% (same as G-10)	E	17.0	3.7
Copper	: 0.011 = 18% (same as G-10)	a	16.8	14.0

$E_C = 0.18\ (17.0) + 82\ (3.7) = 6.09$

$a_c = [3.06\ (16.8) + 3.03\ (14.0)]/6.09 = 15.4$ PPM/°C

Average CTE

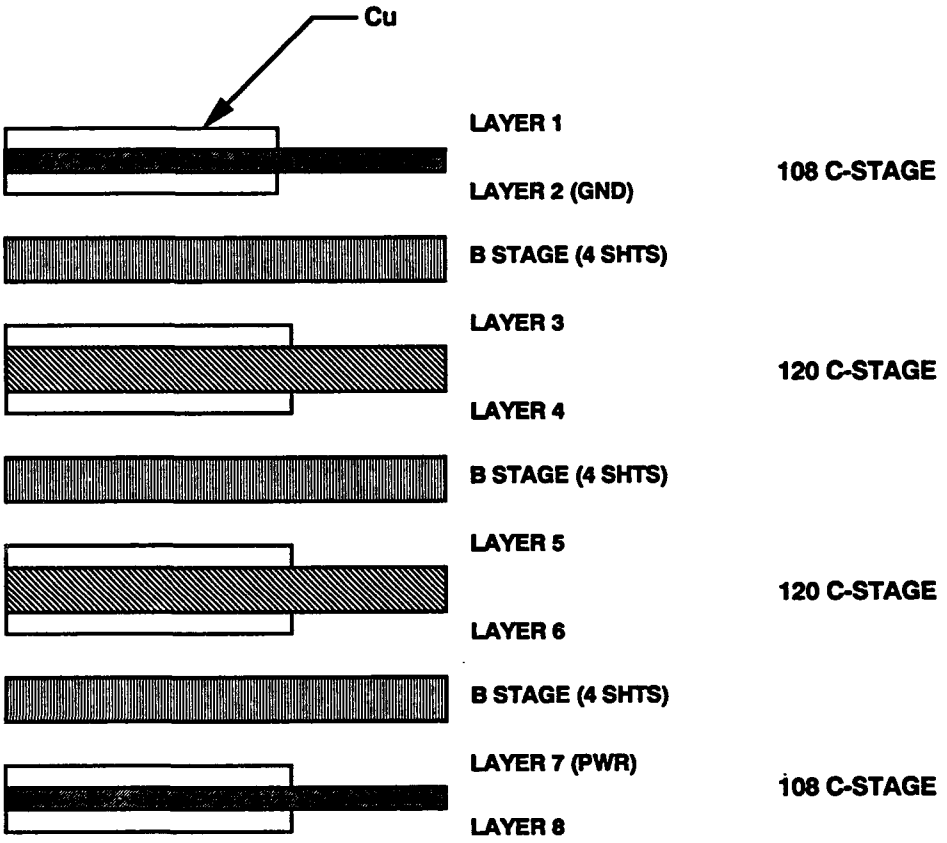
Composite : $V_c = 0.976$ in^3 (same as G-10)

Copper : $V_1 = 0.074$ in^3 (same as G-10)

G-10 : $V_2 = 0.902$ in^3 (same as G-10)

$$a_c = \frac{(16.8 \times 17.0 \times 0.074) + (14.0 \times 3.7 \times 0.902)}{(17.0 \times 0.074) + (3.7 + 0.902)} = 14.75 \text{ PPM/°C}$$

Example 1.4.1-1. CTE Calculations for Epoxy/Glass and Polyimide/Glass



2 PLY STYLE 108 C-STAGE : (2 PIECES) x (0.0045) = 0.009
2 PLY STYLE 120 C-STAGE : (2 PIECES) x (0.0085) = 0.017
STYLE 108 P-STAGE : (12 PIECES) x (0.002) = 0.024
COPPER 1/1 : (8 LAYERS) x (0.0014) = 0.011
0.061

ALL UNITS IN INCHES

AVG CTE = 9.41 PPM/°C MAX CTE = 11.99 PPM/°C

15057-14 (M)

Example Figure 1.4.1-2. Polyimide/Kevlar (Corlam #7293)

CTE Calculations for 7293 Kevlar

Maximum CTE			**CU**	**Kevlar**
#120 C-Stage : 2 Shts x 0.0085	= 0.017	E	17.0	3.0
#108 C-Stage : 2 Shts x 0.0045	= 0.009	a	16.8	6.0
#108 B-Stage : 12 Shts x 0.002	= 0.024			
	0.050 = 82% of Total Thickness			
Copper	0.011 = 18% of Total Thickness			
	0.061 Nominal Thickness			

$E_C = 0.18\ (17.0) + 0.82\ (3.0) = 3.06 + 2.46 = 5.52$

$a_c = [3.06\ (16.8) + 2.46\ (6.0)]/5.52 = 11.99$ PPM/°C

Average CTE

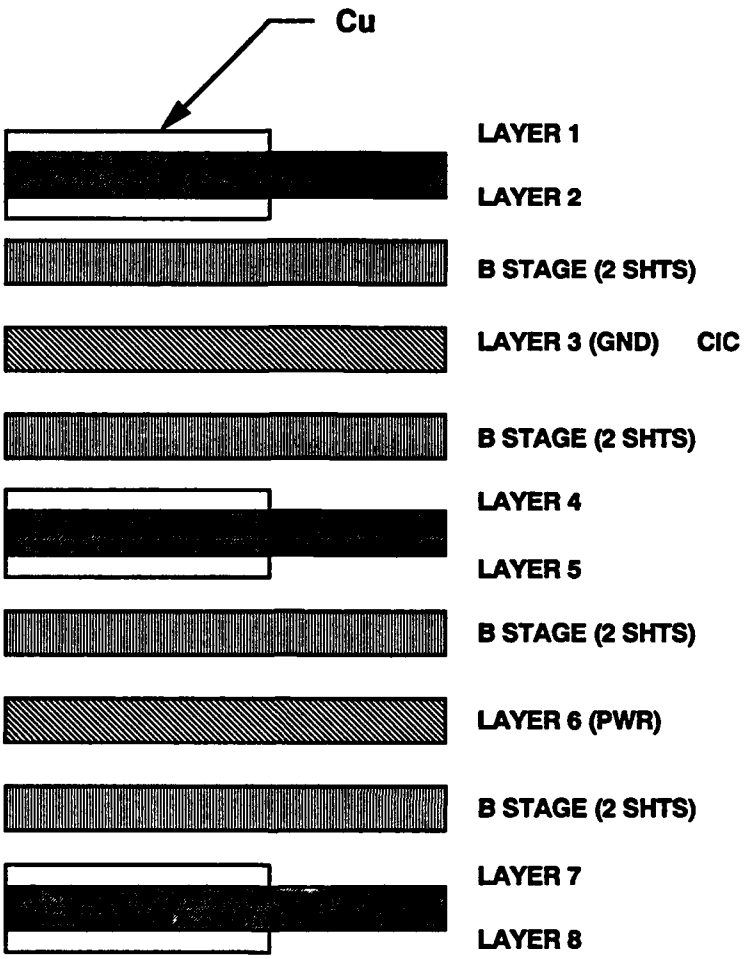
Composite : $V_c = 0.976$ in^3 (same as G-10)

Copper : $V_1 = 0.074$ in^3 (same as G-10)

Kevlar : $V_2 = 0.902$ in^3 (same as G-10)

$$a_c = \frac{(16.8 \times 17.0 \times 0.074) + (6.0 \times 3.0 \times 0.902)}{(17.0 \times 0.074) + (3.0 \times 0.902)} = 9.41 \text{ PPM/°C}$$

Example 1.4.1-2. CTE Calculations for 7293 Kevlar



CIC : (2 PIECES) x (0.006) = 0.012
C-STAGE : (3 PIECES) x (0.006) = 0.018
B-STAGE : (8 PIECES) x (0.003) = 0.024
COPPER 1/1 : (6 LAYERS) x (0.0014) = 0.008

0.062
0.057 PRESSED

AVG CTE = 8.95 PPM/°C MAX CTE = 10.52 PPM/°C

15057-15 (M)

Example Figure 1.4.1-3. CIC Polyimide

CTE Calculations for CIC Polyimide

	Maximum CTE		CU	Polyimide	C/I/C
CIC	: 0.012 = 22.6% of Total Thickness	E	17.0	3.7	18.0
Polyimide	: 0.033 = 62.3% of Total Thickness	a	16.8	14.0	4.6
Copper	: 0.008 = 15.1% of Total Thickness				
	0.053				

$E_C = 0.151\ (17.0) + 0.623\ (3.7) + 0.226\ (18.0) \approx 8.99$

$a_c = [2.57\ (16.8) + 2.30\ (14.0) + 4.07\ (4.6)]/8.99 = 10.47$ PPM/°C

Average CTE

Copper : $V_1 = (4'' \times 4'')\ (0.0014)\ (6) \times (0.25) = 0.034\ in^3$

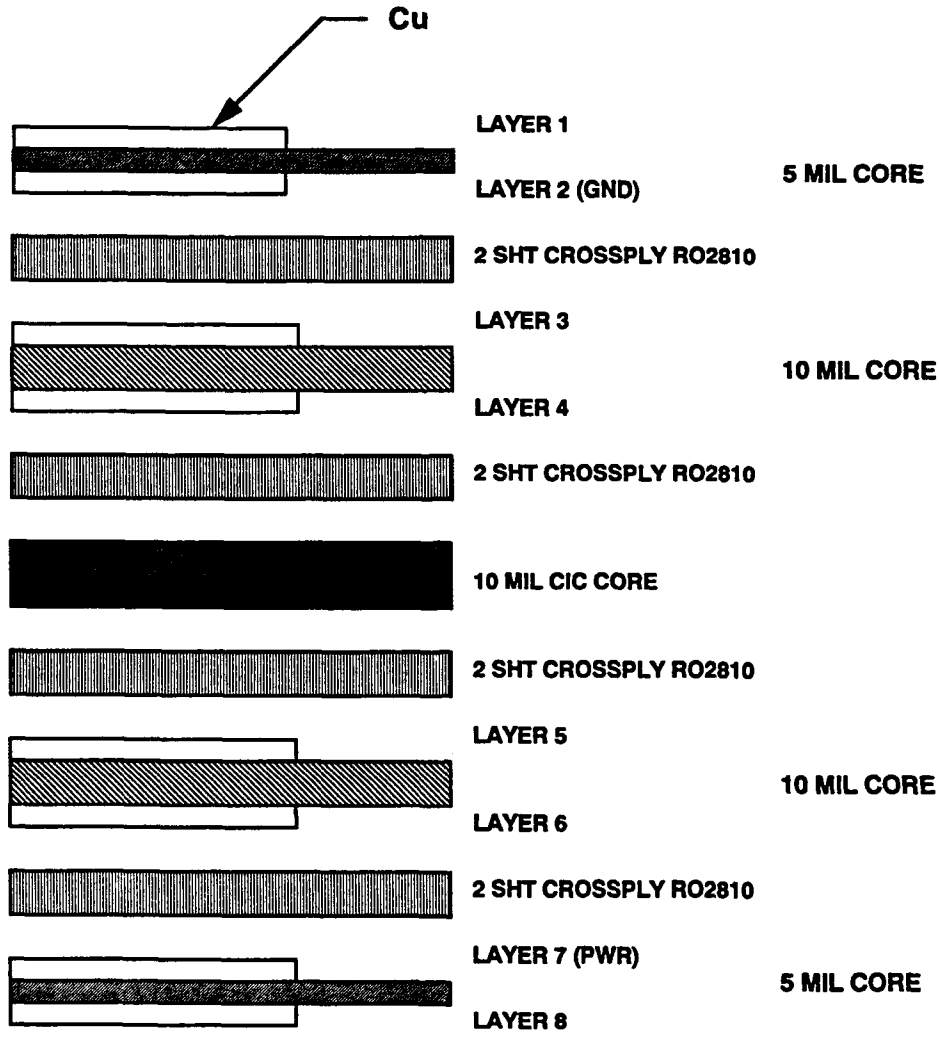
CIC : $V_3 = (4 \times 4)\ (0.006)\ (2) = 0.192\ in^3$

Composite : $V_c = 4 \times 4 \times 0.053 = 0.848\ in^3$

Polyimide : $V_2 = V_c - (V_1 + V_3) = 0.848 - (0.034 + 0.192) = 0.622\ in^3$

$$a_c = \frac{(16.8 \times 17.0 \times 0.034) + (4.6 \times 0.192) + (14.0 \times 3.7 \times 0.622)}{(17.0 \times 0.034) + (18.0 \times 0.192) + (3.7 \times 0.622)} = 9.22 \text{ PPM/°C}$$

Example 1.4.1-3. CTE Calculations for CIC Polyimide



2 SHT CROSSPLY R02810 : (8 PIECES) x (0.0025) = 0.020
LAMINATE RO2800 : (2 PCS X 0.010) + (2 PCS x 0.005) = 0.030
CORE OF CIC : (1 LAYER) x (0.010) = 0.010
COPPER 1/1 : (8 LAYERS) x (0.0014) = 0.011
0.071

ALL UNITS IN INCHES

AVG CTE = 8.8 PPM/°C MAX CTE = 11.2 PPM/°C

15057-16 (M)

Example Figure 1.4.1-4. Rogers R02800 CIC

CTE Calculations for R02800 CIC

	Maximum CTE		CU	R02800	C/I/C
CIC	: 0.010 = 14.1% of Total Thickness	E	17.0	0.06	18.0
R02800	: 0.050 = 70.4% of Total Thickness	a	16.8	16.0	5.2
Copper	: 0.011 = 15.5% of Total Thickness				
	0.071				

$E_C = 0.155\ (17.0) + 0.704\ (0.06) + 0.141\ (18.0) = 5.21$

$a_c = [2.63\ (16.8) + 0.04\ (16.0) + 2.54\ (5.2)]/5.21 = 11.2$ PPM/°C

Average CTE

Composite : $V_c = 4'' \times 4'' \times 0.071 = 1.136\ in^3$

Copper : $V_1 = 0.074\ in^3$(same as in G-10)

CIC : $V_3 = 0.010 \times 4'' \times 4'' = 0.16\ in^3$

R02800 : $V_2 = V_c - (V_1 + V_3) = 1.136 - (0.074 + 0.010) = 1.05\ in^3$

$$a_c = \frac{(16.8 \times 17.0 \times 0.074) + (5.2 \times 18.0 \times 0.16) + (16.0 \times 0.6 \times 1.05)}{(17.0 \times 0.074) + (18.0 \times 0.16) + (0.06 \times 1.05)} = 8.83 \text{ PPM/°C}$$

Example 1.4.1-4. CTE Calculations for R02800 CIC

1.5 PWB Artwork Requirements

The purpose of this section is to define the basic design guidelines for PWB artwork utilizing surface mount technology. An emphasis is placed on establishing standard component land patterns that will provide reliable solder joints. The patterns presented cover those surface mounted devices qualified to military specifications. The formulas used to create these patterns may be modified to create a pattern for any unique surface mounted device. Other important factors that affect layout, such as; thermal and dynamic characteristics, assembly processes (automated insertion, soldering, cleaning, inspection, etc.), and automated testing are also discussed.

1.5.1 General Requirements

To determine the land pattern of the surface mount component there are four main factors to consider:

1. The component dimensions plus tolerances.
2. The positional tolerance of the land pattern with respect to a reference point on the PWB.
3. The positional tolerance of the screened solder paste and solder resist with respect to the same reference point.
4. The placement tolerance of the automated placement equipment.

A worst-case design approach is not realistic considering the relatively large tolerances involved when compared to the small component sizes. The optimum land pattern is one that minimizes the area occupied by a land and maximizes the number of conductors that can be routed between adjacent lands.

IPC-SM-782 (surface mount land patterns, configurations and design rules) was used as an important reference during the creation of the land patterns defined in this section. Although that document emphasizes commercial applications, the ground rules can be readily adapted to military specifications. Note that the patterns specified herein that are different from IPC-SM-782 are preferred over that document based on studies performed during this and other projects. Also, requirements of MIL-STD-2000, Rev. A (proposed) have influenced pad designs contained herein.

1.5.2 Land Patterns

One of the most crucial factors in implementing surface mount technology is the design of the component land pattern. Although solder joint reliability is emphasized, other areas greatly affected are; solder defects, cleaning, inspection, testing, and repair.

The figures in the following sections show only the soldered land patterns. Design of the fan out to vias used to interconnect the patterns will be discussed in general terms in the paragraphs on line and pad size/spacing guidelines. Via patterns for each multileaded device pattern may be established using these guidelines based on the appropriate grid system used. Component spacing guidelines for inspectability are covered in Section 3.2.

1.5.2.1 Passive Devices

Figure 1.5.2.1-1 defines the recommended land patterns for various sizes of standard rectangular components. The minimum and maximum dimensions shown are those found in the military specifications referenced in Section 1.2.2.1. The formulas presented can be used to determine land patterns for any unique rectangular component. The formulas have been written to compensate for the entire tolerance range of the components. This will eliminate the requirement of customizing pad sizes for similar component bodies having dimensions at the opposite ends of the tolerance range. Also, the formulas comply with the proposed MIL-STD-2000, Rev. A, concerning chip component placement and alignment. Figures 1.5.2.1-2 and 1.5.2.1-3 illustrate examples of the tolerance extremes of various chip components with the appropriate land pattern. The solder fillet shown is one half the thickness (optimum). Table 1.5.2.1 lists common components and pad dimensions based on these formulae.

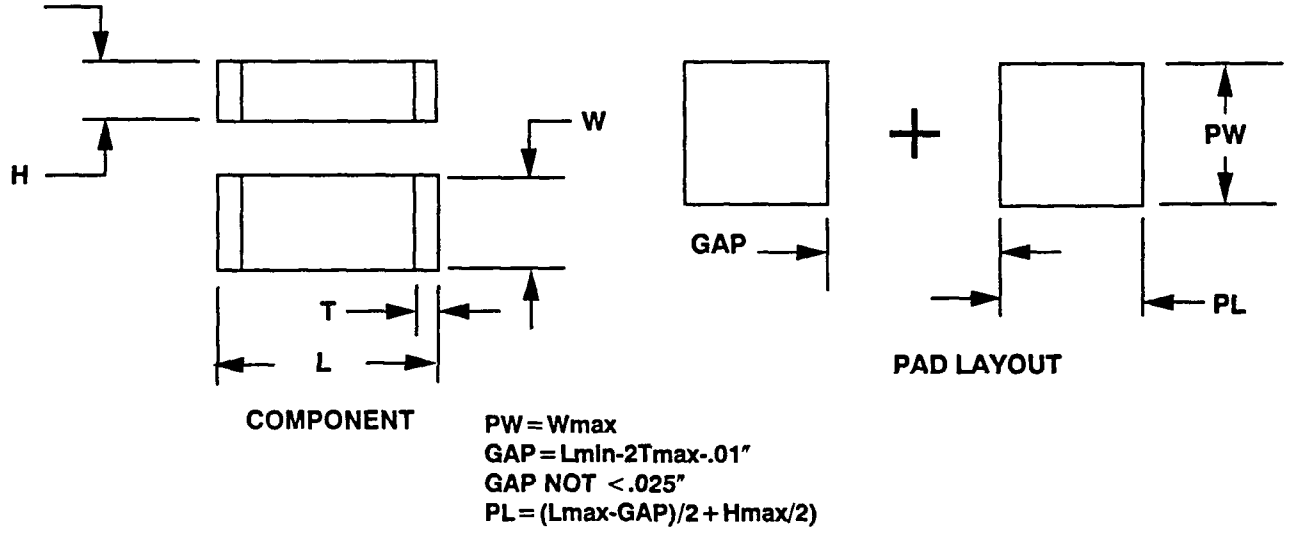
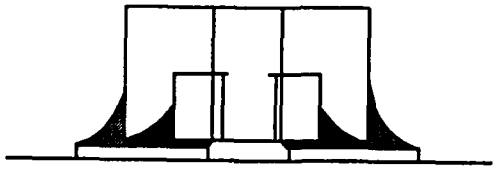


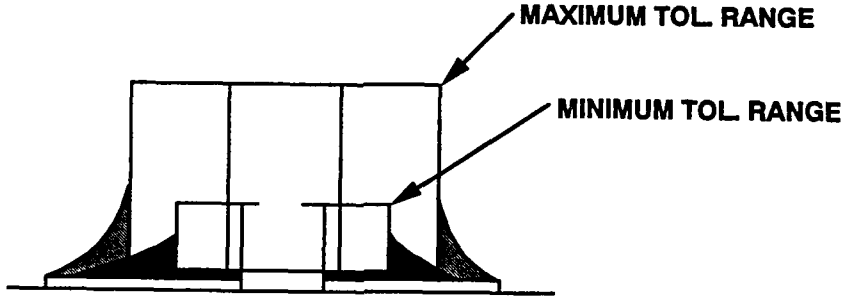
Figure 1.5.2.1-1. Chip Component Pad Dimensioning

Chip components, particularly capacitors, may be susceptible to cracking due to thermal shock during processing. This phenomena is prevalent in wave soldering if the proper preheat profile is not utilized (see Section 2.5.1.3). Factors that may affect cracking include vendor selection, component size and thickness, capacitance value and preheat. Cracking has also been correlated to capacitors containing the maximum value of capacitance available in any package size. It is recommended that the next size component be used in lieu of a capacitor containing the maximum value.

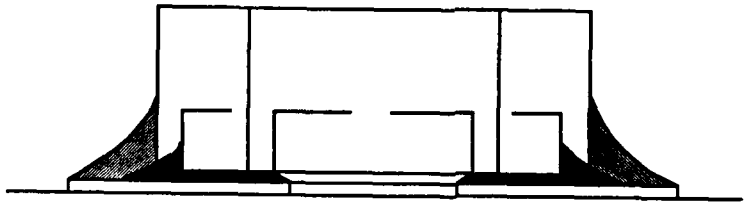
Figure 1.5.2.1-4 illustrates the need to separate common pads. This minimizes the possibility of tombstoning which can occur when solder on one pad reflows before the other and drags the part away from the unreflowed pad. For similar reasons, one should not locate a PTH in or adjacent to a pad. This will cause starvation of the solder joint by causing solder to wick down and fill the PTH. The opposite solder joint, assuming no PTH, will cause the component to raise due to a greater surface tension in the solder. The PTH should be separated from the pad using a necked



0502 AND 0505 CHIP RESISTOR
MIN. AND MAX. TOL. RANGES
(MAX. AND NOMINAL TERMINATION (T) RANGES)



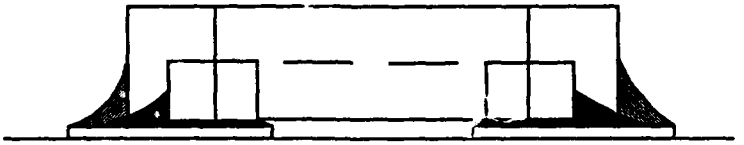
CDR01 (0805) CHIP CAPACITOR
MIN. AND MAX. TOL. RANGES
(MAX. AND NOMINAL TERMINATION (T) LENGTH)



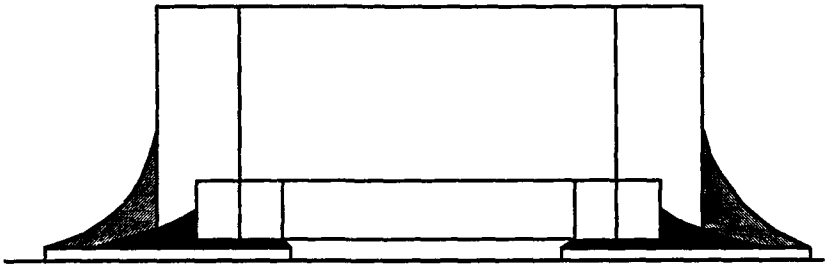
CDR32 (1206) CHIP CAPACITOR
MIN. AND MAX. TOL. RANGES
(MAXIMUM TERMINATION (T) LENGTH)

455-7 (M)

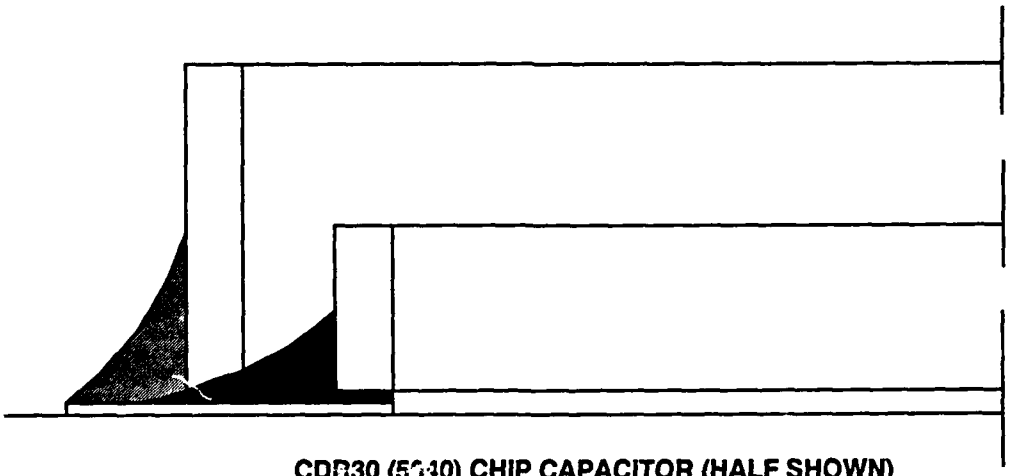
Figure 1.5.2.1-2



1505 CHIP RESISTOR
MIN. AND MAX. TOL. RANGES
(MAXIMUM TERMINATION (T) LENGTH)



CDR04 (1812 CHIP CAPACITOR)
MIN. AND MAX. TOL. RANGES
(MAXIMUM TERMINATION (T) LENGTH)



CDR30 (5040) CHIP CAPACITOR (HALF SHOWN)
MAX. AND MIN. TOL. RANGES
(MAXIMUM TERMINATION (T) LENGTH)

455-6 (M)

Figure 1.5.2.1-3

Table 1.5.2.1.

CHIP COMPONENT PAD CALCULATIONS

Lmax=MAX BODY LENGTH
Lmin=MINIMUM BODY LENGTH
Tmax=MAX TERMINATION LENGTH
Tmin=MIN TERMINATION LENGTH
NOTE: when no Tmin is specified assume Tmin=.010"
Hmax=MAX BODY THICKNESS
Hmin=MIN BODY THICKNESS (.020" IF NOT SPECIFIED)
Wmax= MAX BODY WIDTH
GAP=GAP BETWEEN PADS

PAD LENGTH = (Lmax-GAP)/2 + (Hmax/2)
PAD WIDTH = Wmax
GAP = Lmin-(2xTmax)-.01"
MINIMUM GAP = .025"

COMPONENT DIMENSIONS (inches)

CHIP CAPACITORS

STYLE	MIL-C-	Lmax	Lmin	Tmax	Tmin	Hmax	Hmin	Wmax	PAD WIDTH	PAD LENGTH	GAP
CDR01	55681/1	0.095	0.065	0.030	0.010	0.055	0.020	0.065	0.065	0.063	0.025
CDR02	55681/1	0.195	0.165	0.030	0.010	0.055	0.020	0.065	0.065	0.078	0.095
CDR03	55681/1	0.195	0.165	0.030	0.010	0.080	0.020	0.095	0.095	0.090	0.095
CDR04	55681/1	0.195	0.165	0.030	0.010	0.080	0.020	0.140	0.140	0.090	0.095
CDR05	55681/2	0.200	0.165	0.030	0.010	0.080	0.020	0.270	0.270	0.093	0.095
CDR06	55681/3	0.245	0.205	0.030	0.010	0.080	0.020	0.270	0.270	0.095	0.135
CDR11	55681/4	0.070	0.040	0.015	0.005	0.057	0.028	0.070	0.070	0.051	0.025
CDR12	55681/4	0.080	0.030	0.015	0.005	0.057	0.028	0.070	0.070	0.056	0.025
CDR13	55681/4	0.130	0.090	0.025	0.005	0.102	0.058	0.130	0.130	0.101	0.030
CDR14	55681/4	0.135	0.085	0.025	0.005	0.102	0.058	0.130	0.130	0.106	0.025
CDR22 - CDR25 ------LEADED DEVICES											
CDR26	55681/6	0.165	0.135	0.020	0.010	0.120	0.060	0.165	0.165	0.100	0.085
CDR27	55681/6	0.209	0.171	0.020	0.010	0.120	0.060	0.209	0.209	0.104	0.121
CDR28	55681/6	0.363	0.297	0.020	0.010	0.120	0.060	0.363	0.363	0.118	0.247
CDR29	55681/6	0.440	0.360	0.020	0.010	0.120	0.060	0.440	0.440	0.125	0.310
CDR30	55681/6	0.594	0.486	0.020	0.010	0.120	0.060	0.440	0.440	0.139	0.436
CWR06-A	55681/4	0.115	0.085	0.035	0.010	0.065		0.065	0.065	0.078	0.025
CWR06-B	55681/4	0.165	0.135	0.035	0.010	0.065		0.065	0.065	0.088	0.055
CWR06-C	55681/4	0.215	0.185	0.035	0.010	0.065		0.065	0.065	0.088	0.105
CWR06-D	55681/4	0.165	0.135	0.035	0.010	0.065		0.115	0.115	0.088	0.055
CDW06-E	55681/4	0.215	0.185	0.035	0.010	0.065		0.155	0.155	0.088	0.105
CWR06-F	55681/4	0.235	0.205	0.035	0.010	0.085		0.150	0.150	0.098	0.125
CWR06-G	55681/4	0.280	0.250	0.055	0.010	0.125		0.125	0.125	0.138	0.130
CWR06-H	55681/4	0.300	0.270	0.055	0.010	0.125		0.165	0.165	0.137	0.150
	DOD-C-										
CDR31	55681/7	0.086	0.070	0.033	0.012	0.051	0.020	0.057	0.057	0.056	0.025
CDR32	55681/8	0.133	0.117	0.028	0.012	0.051	0.020	0.070	0.070	0.067	0.051
CDR33	55681/9	0.135	0.115	0.030	0.010	0.059	0.020	0.108	0.108	0.075	0.045
CDR34	55681/10	0.186	0.166	0.030	0.010	0.059	0.020	0.135	0.135	0.075	0.096
CDR35	55681/11	0.188	0.164	0.032	0.008	0.059	0.020	0.280	0.280	0.079	0.090

CHIP RESISTORS

STYLE	MIL-SPEC	Lmax	Lmin	Tmax	Tmin	Hmax	Wmax	PAD WIDTH	PAD LENGTH	GAP
RM0502	55342/1	0.075	0.045	0.027	0.010	0.040	0.035	0.035	0.045	0.025
RM0505	55342/2	0.075	0.045	0.027	0.010	0.040	0.060	0.060	0.045	0.025
RM1005	55342/3	0.125	0.095	0.032	0.010	0.040	0.060	0.060	0.070	0.025
RM1505	55342/4	0.175	0.145	0.032	0.010	0.040	0.060	0.060	0.072	0.071
RM2208	55342/5	0.250	0.220	0.032	0.010	0.040	0.085	0.085	0.072	0.146
RM0705	55342/7	0.100	0.070	0.032	0.010	0.040	0.060	0.060	0.058	0.025

down trace or by depositing solder mask material between the pad and the via. An advantage to the neck down technique is that it reduces the chance of reflowing the solder joint during subsequent wave soldering operations. The heat travelling through a via is sufficient to melt an attached solder joint on the top side when there is no isolation.

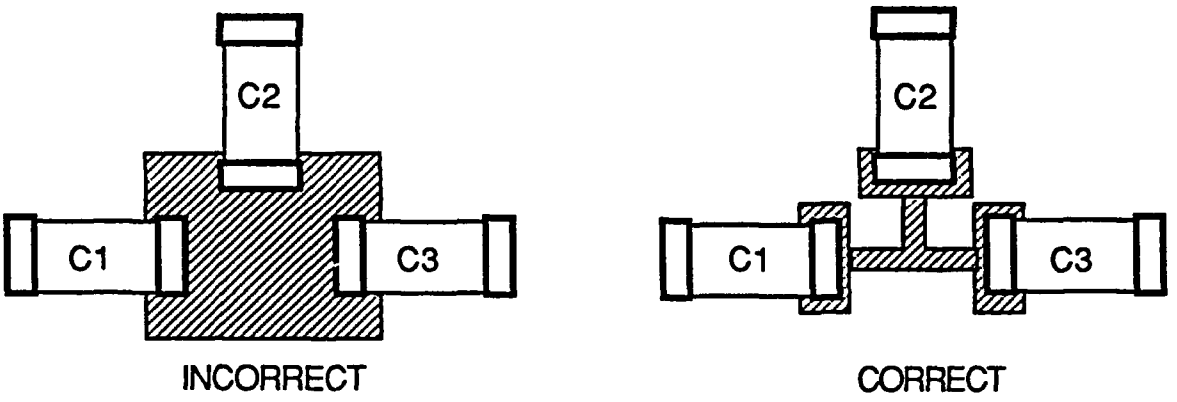


Figure 1.5.2.1-4. Chip Device Pad Configuration

1.5.2.2 Integrated Circuits

MIL-M-38510 is the specification used to define the packaging configurations for flatpacks, dual-in-line packages, quad packs, leaded ceramic chip carriers, and leadless ceramic chip carriers. Data sheets provide for a wide range of body styles and lead count. In addition to defining the current pad dimensions for such components, it is also important to indicate the correct orientation of the package. Indicating Pin one is the standard way of indicating package orientation. Figure 1.5.2.2 shows two methods used to indicate pin one.

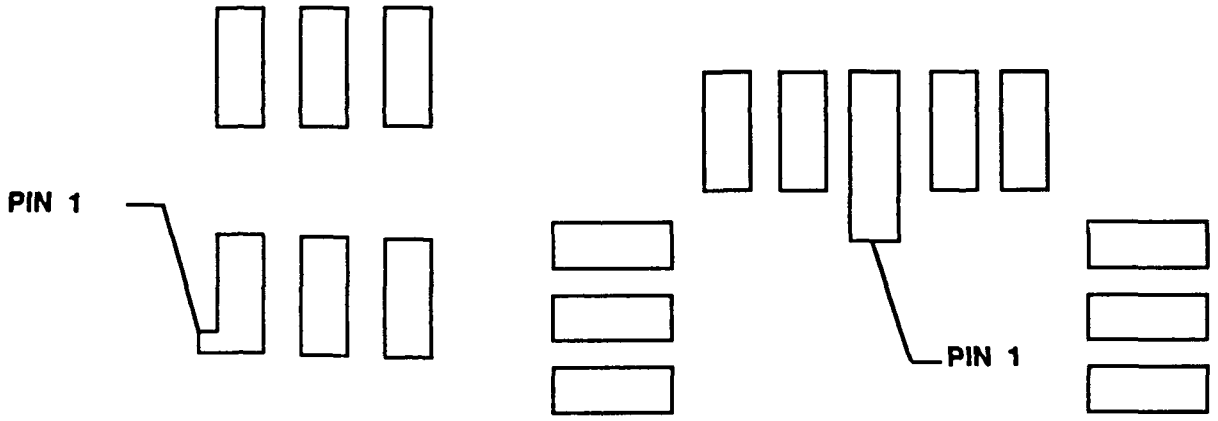


Figure 1.5.2.2. Pin 1 Notation for Flatpacks and LCC's

1.5.2.2.1 Flatpacks

The standard flatpack has seen extensive use in military applications over the years. The basic lead form and footprint requirements have been established with minimal change. To meet the requirements of MIL-STD-2000, Rev. A, the following must be accomplished:

1. The flatpack leads shall be formed in a gull-wing configuration.
2. The first bend must be no closer than 0.015 inch (0.38 mm) to the component body.
3. The lead bends shall be between 45° and 90° (90° preferred) with a bend radius of no less than 1-1/2 times the lead thickness.
4. The foot of the formed lead shall be 1½ times the lead width (or 2 times the diameter).
5. The length of the pad shall be such to allow a heel fillet to be formed between the pad and the lead.

For other workmanship guidelines for gull-wing attachment, see Sections 3.1.8.2 through 3.1.8.4.

1.5.2.2.2 Dual-Inline-Package (DIP)

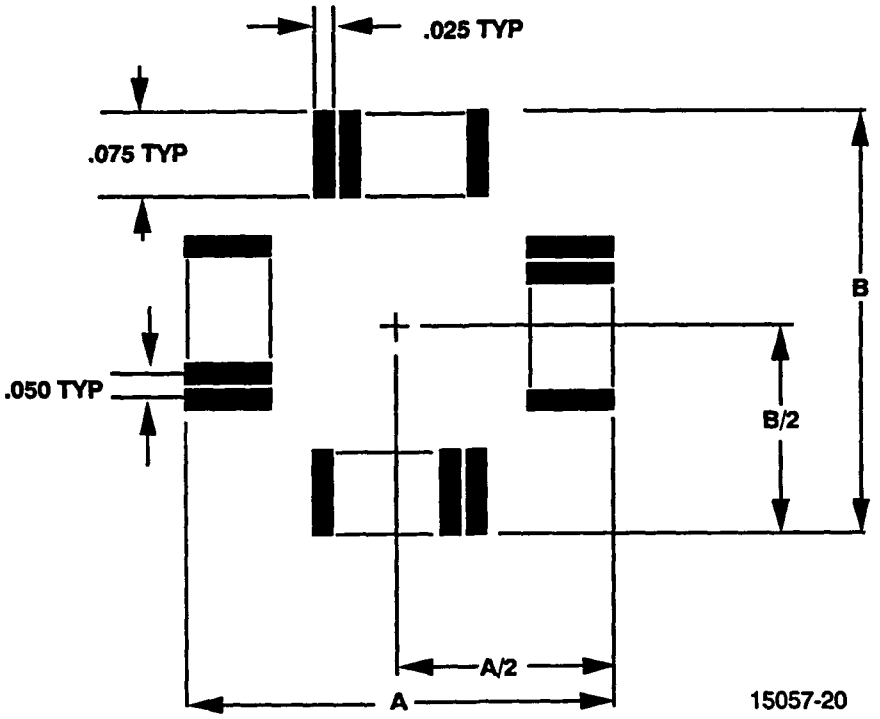
In instances when a component is only available in a DIP style, the component leads are often cropped and mounted in a butt joint configuration. This is fine in many low stress environments, but is not deemed reliable for military applications. When a DIP must be used, the component leads should be bent 90° outward to form a foot approximately 0.60 inch long. This will allow for a standard planar mounting configuration. Use caution as this may be a violation of the applicable MIL-STD.

1.5.2.2.3 Ceramic Quad Packages (Cer-Quads)

Figure 1.5.2.2.3 defines the recommended land patterns for standard size ceramic quad packages as defined in MIL-M-38510. There are two basic body styles with three lead configurations. The body styles are either two-piece ceramic sections with glass seals encapsulating the leads (similar to a cer-DIP), or the leads are brazed to the outside of a solid ceramic body. The leads are either formed in a "J" configuration, a gull-wing configuration, or unformed. The unformed package styles typically are gull-wing formed using the same criteria as the flatpack. The footprints defined herein are based on the following criteria for unformed packages:

- 0.040 inch lead extension from the body to first bend
- 0.050 inch foot length (1½ lead width, minimum)
- 1 lead width minimum inner pad extension
- Approximately 0.010 inch pad extension beyond toe

Actual dimensions may vary based on lead size and particular tooling requirements, but must ultimately meet the requirements of the applicable assembly specification.



MIL-M-38510 Designation*	Package Lead Count	Pattern Dimensions	
		A	B
C-G1	44	0.970	0.970
C-J1	44	0.750	0.750
C-G4	44	0.900	0.900
C-J4	44	0.750	0.750
C-G2	68	1.265	1.265
C-J2	68	1.045	1.045
C-G5	68	1.20	1.20
C-J5	68	1.05	1.05
C-G3	84	1.465	1.465
C-J3	84	1.245	1.245
C-G6	84	1.407	1.407
C-J6	84	1.250	1.250
* All others must be evaluated on a case-by-case basis			

General requirements:

- 1½ width minimum foot
- Sufficient pad length to provide for a heel fillet
- See applicable Workmanship Manual for any specific requirements
- Concurrence of tooling designer (if not preformed) is required

C-G1, G2, and G3 are supplied preformed. Pattern allows for 0.010 inch pad extensions beyond largest allowable dimension.

C-G4, G5, and G6 are not supplied formed. Pattern reflects standard manufacturing tooling design for gull-wing formations. Verify with manufacturing tooling designer for actual requirements.

Figure 1.5.2.2.3. Cer-Quad Patterns

1.5.2.2.4 Leadless Chip Carriers

Figure 1.5.2.2.4 defines the land patterns for standard sizes of leadless chip carriers. Both square and rectangular configurations are defined. These patterns will provide an optimum solder joint provided the CTE of the interconnecting structure and carrier are compatible. The primary requirements are that the pad match the footprint of the LCC's bottom metallization (including pad one) and that sufficient pad extension exists beyond the edge of the component body (0.040 –0.050 inch, typically).

1.5.2.2.5 Fine Pitch Devices (0.025 Inch or Less)

Figure 1.5.2.2.5-1 shows the typical lead forming detail used to establish the land pattern. Figure 1.5.2.2.5-2 defines the land pattern with vias for a 0.020 inch pitch, 264 lead, 1.45 inch square leaded ceramic chip carrier. Figure 1.5.2.2.5-3 shows a typical inner layer conductor routing scheme available with this via pattern. Actual pad lengths may vary due to process tooling requirements. The end item must still meet requirements for planar mounted leads (see Sections 3.1.8.2 through 3.1.8.4).

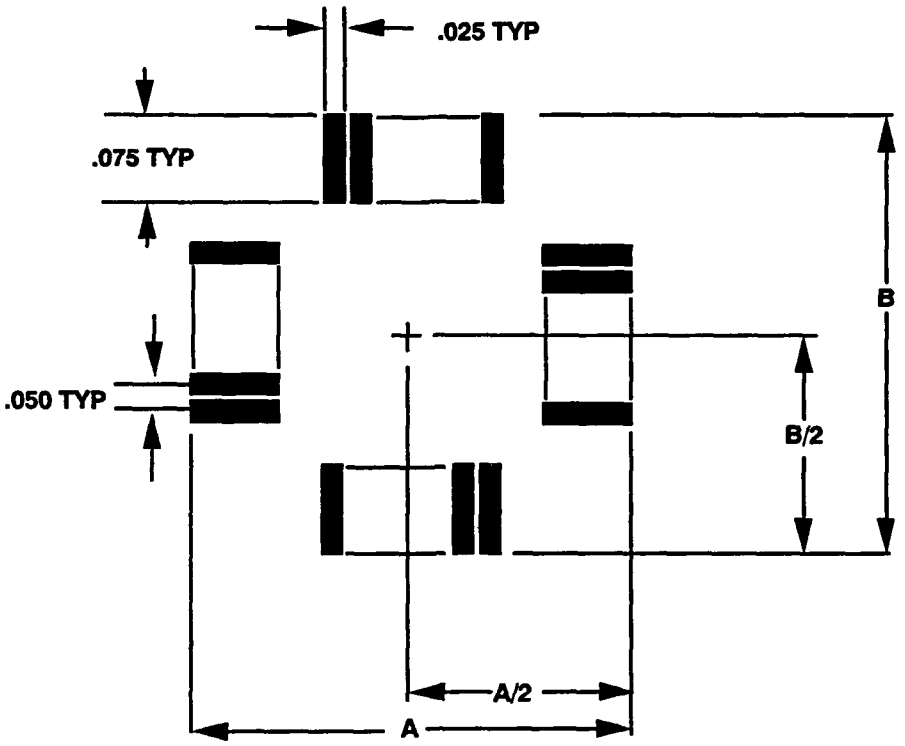
1.5.3 Conductor Width and Spacing

The width of the conductors (and thickness) is determined on the basis of the current carrying capacity required for single-sided and double-sided PWB's. For multilayer PWB's, where a power and ground plane is typically used, the line width and spacing is driven by the PWB density requirements. However, there is a price for higher density; it is lower yield which translates into higher cost per PWB. PWB manufacturers and MIL-STD-275 prefer 0.015 inch wide lines and 0.020 inch wide spaces. The 0.010 inch line and 0.010 inch spacing is considered standard for high yield PWB construction, to a minimum of 0.004 inch wide conductors and 0.005 inch wide spaces with reduced yield or producibility with its corresponding high cost per board. The figures mentioned are based on the subtractive PWB fabrication technology. Smaller lines and spacing can be achieved with the use of semi-additive and/or additive processes. The additive fabrication technology is a very viable substitute for subtractive processing in high-speed circuits for its superior line resolution and the capability to control line widths to close tolerances. Aside from the increased interest in small lines and spaces, SMT PWB conductors are the same as for through-hole PWB's.

1.5.4 Via Size and Spacing

The same standards that define line requirements also define via size and spacing. One important factor for defining via plated through-hole size is the ratio of board thickness to plated hole diameter. A ratio of 3:1 or less is highly preferred and a ratio of 4:1 is acceptable but will increase fabrication costs and reduce reliability in some substrates.

Via locations for multileaded components are usually established as part of and within the envelope of each land pattern. Vias connected to component lands should be located at a distance to prevent solder migration from the component land during solder reflow. The conductor between the land and via should be sufficiently narrow to prevent migration or isolate the land by the use of a solder mask. Figure 1.5.4 shows some typical good design practices.



MIL-M-38510 CASE OUTLINE LETTER	PACKAGE LEAD COUNT	PATTERN DIMENSIONS	
		A	B
C-1	16	.380	.380
C-9	18	.360	.430
C-10	18	.360	.510
C-2	20	.430	.430
C-3	24	.480	.480
C-4	28	.530	.530
C11	28	.430	.630
C12	32	.530	.630
C5	44	.730	.730
C6	52	.830	.830
C7	68	1.030	1.030
C8	84	1.230	1.230

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Figure 1.5.2.2.4. Leadless Chip Carrier Patterns

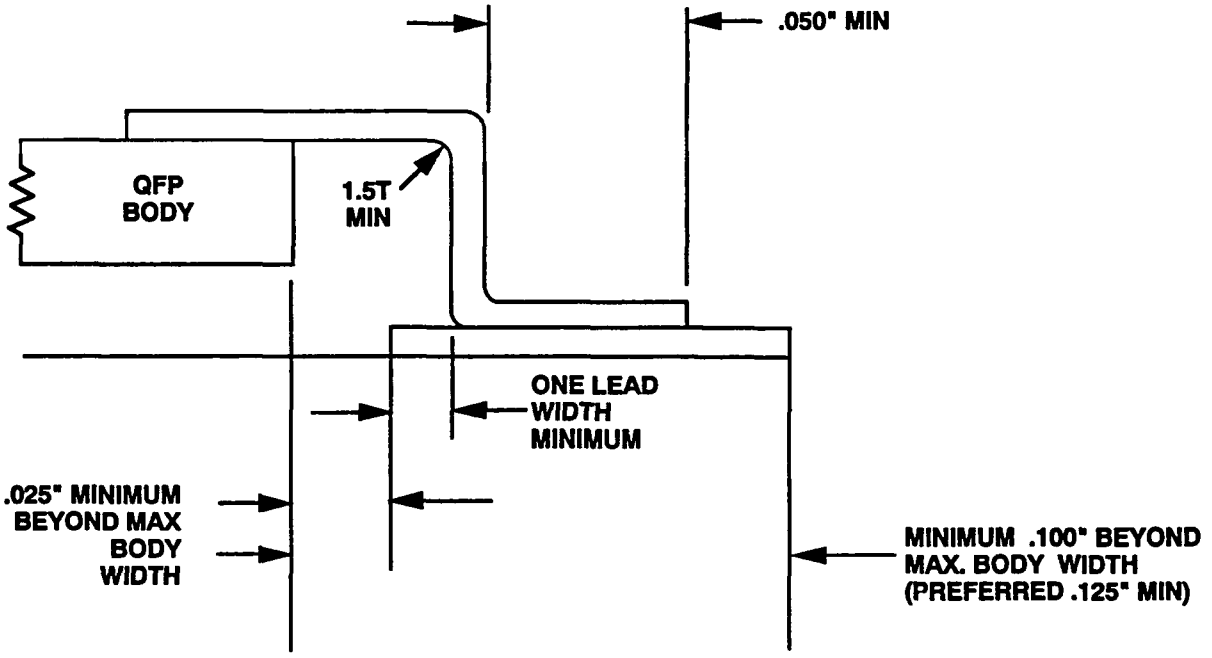


Figure 1.5.2.2.5-1. Fine Pitch Lead Forming Detail

1.5.4.1 Clearance Pad Size for CIC

The film art master pad diameter for a clearance ring to be etched around the barrel of a PTH on copper-invar-copper foil can be calculated once three factors are known. The first factor is the outside diameter of the PTH. Drill holes for plated through-holes are usually drilled 2 mils larger than the stated finish inside plated diameter to allow for the plating build up. The second factor is defining a desired finished clearance annular ring dimension that takes into consideration tolerances and alignment during fabrication. The final factor is an allowance for the under cut which takes place during etching. This is approximately 1 mil of hole diameter for every 1 mil of material thickness to be etched. Figure 1.5.4.1 shows how the clearance hole diameters are calculated.

1.5.5 Layout Guidelines

Designing with surface mount technology requires an understanding of the impact on the design of the following areas:

1. Manufacturability
2. Inspectability
3. Testability
4. Repairability

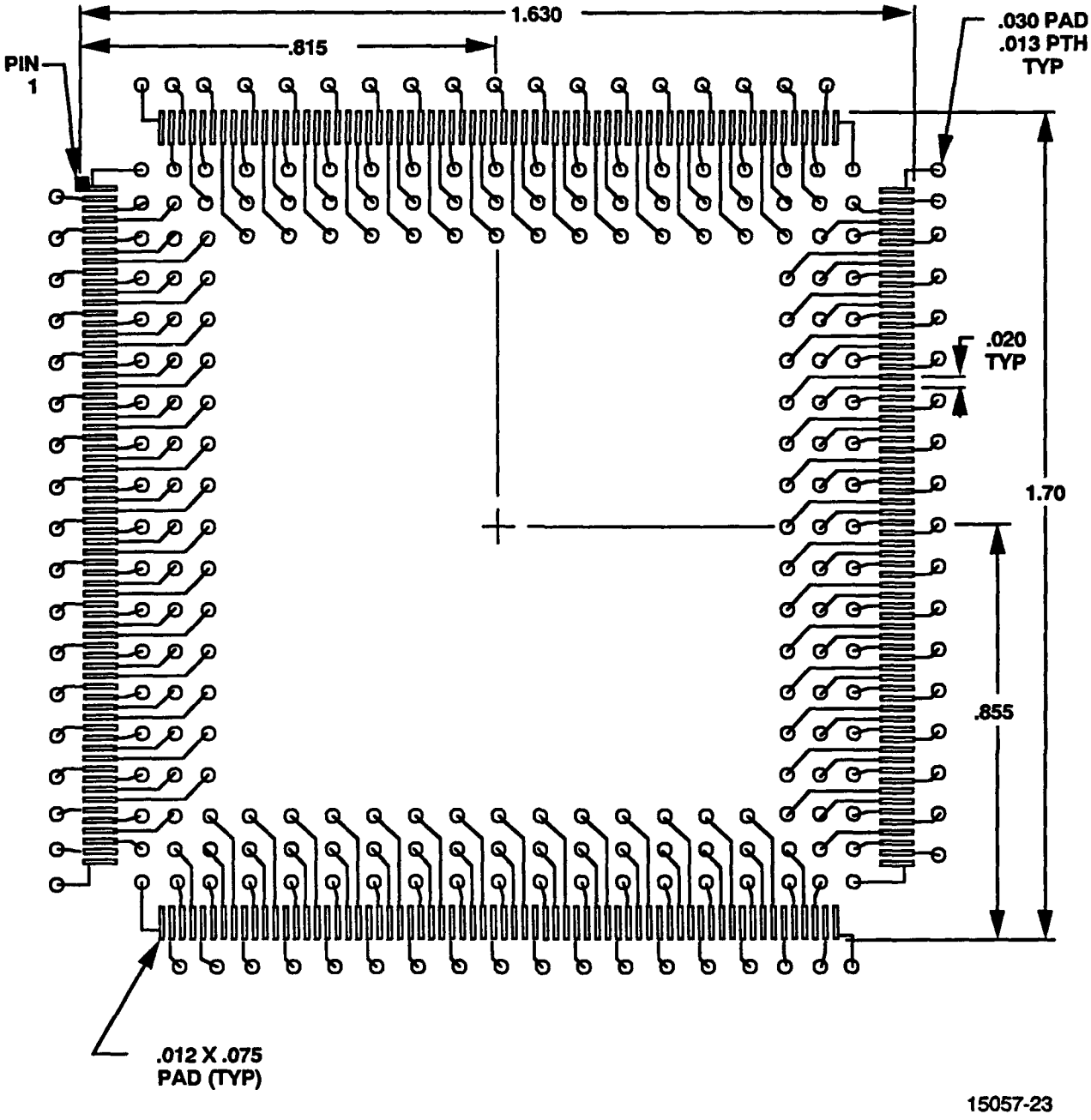


Figure 1.5.2.2.5-2. Land/Via Pattern 264 Lead Device

The equipment to be used in each of these areas must be known during the design phase to determine the limits that they impose. Component placement equipment and required fixturing must be identified to know minimum clearances for each component type. Inspection requirements are often overlooked but are very critical because of the low component profiles and dense packaging associated with surface mounted technology. Automated testing requires an established grid for test point locations and identifying holding fixture clearances. Repairability encompasses rework and modification and implies components must be removed and replaced. Surface mount dictates that all solder joints of a component must be reflowed simultaneously to

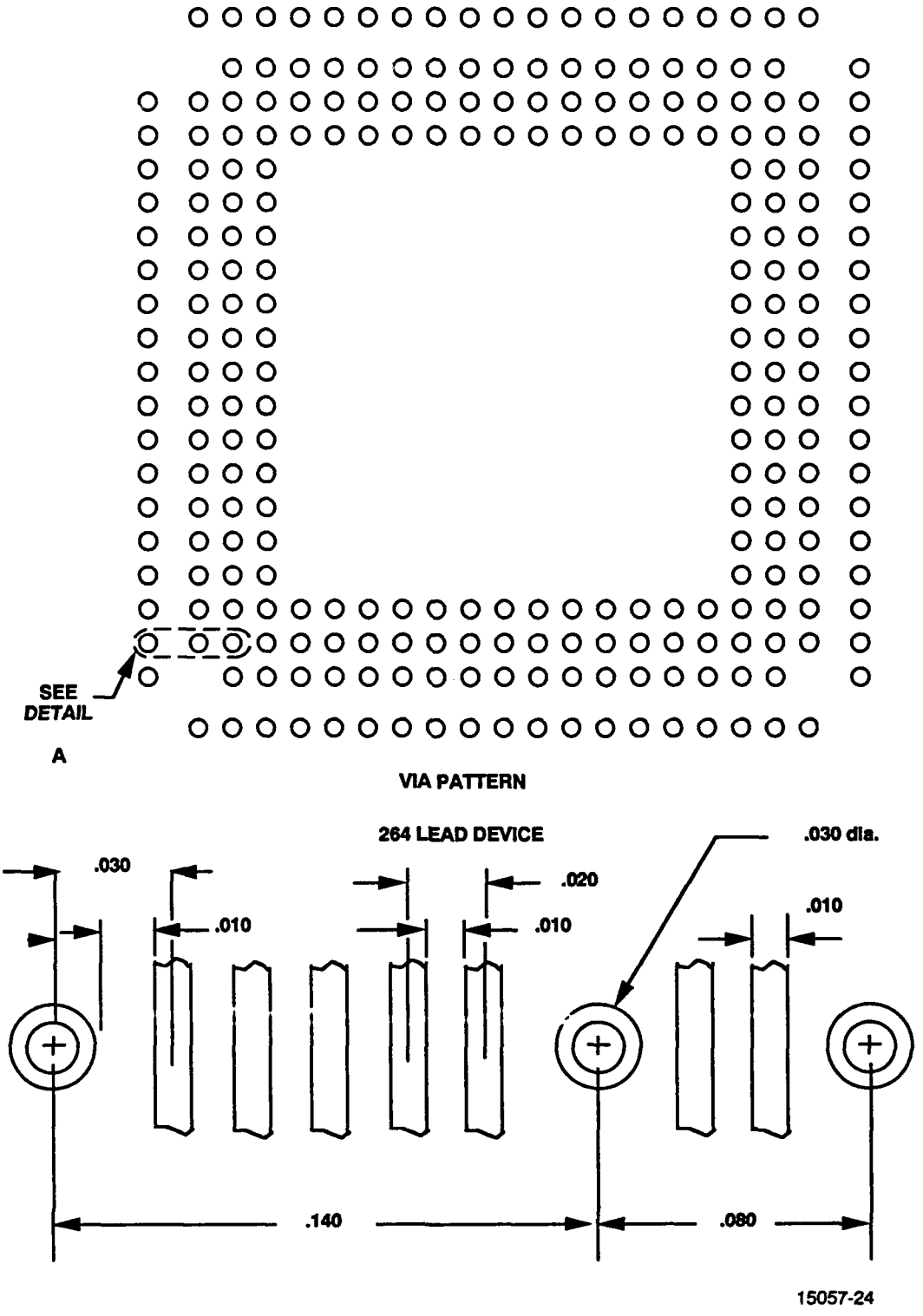


Figure 1.5.2.2.5-3. Internal Trace Routing

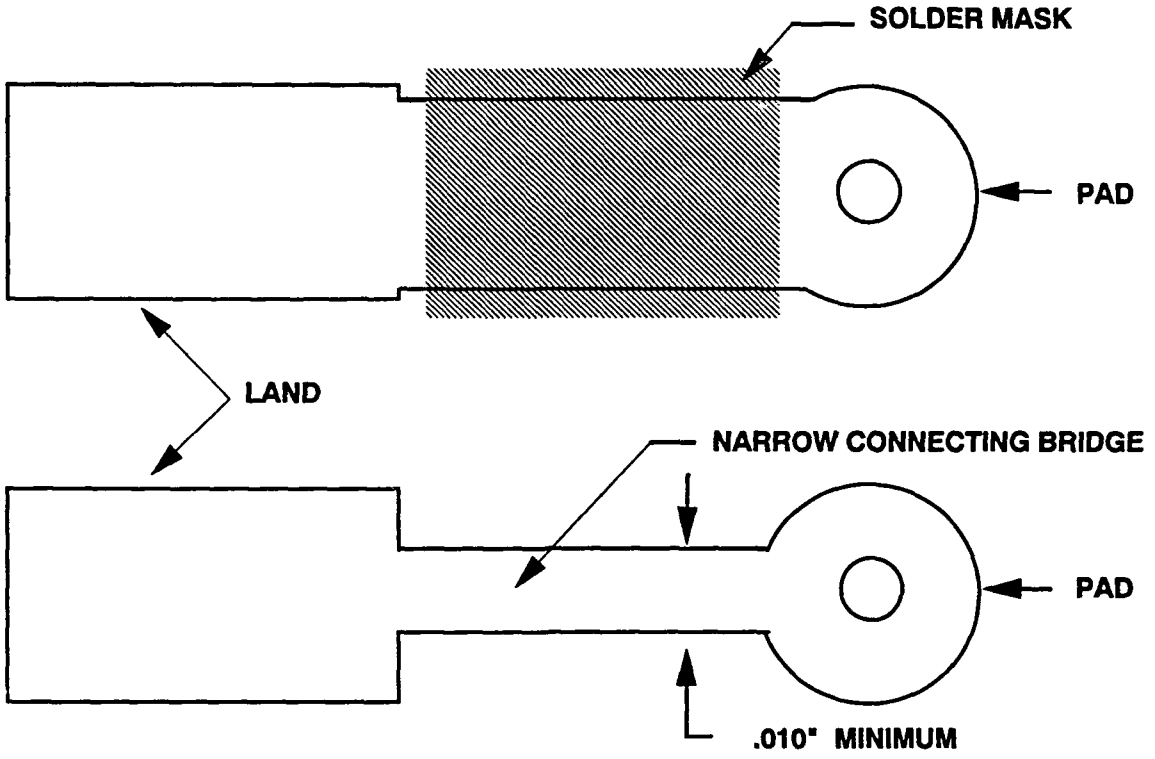


Figure 1.5.4. Solder Migration Prevention During Reflow

remove the part. Solder reflow fixture shapes and sizes vary widely between vendors and must be identified during design layout to establish clearance requirements.

1.5.5.1 Component Spacing

Figure 1.5.5.1-1 shows the recommended land to land clearances that will provide the necessary component spacing to meet the general requirements discussed in paragraph 1.5.5. All possible combinations of component placement are not covered by these guidelines and should be addressed individually during the design layout. Particular attention should be placed on extremes of component heights and the impact on inspection and repair. Also, consideration for wave soldering of chip components is required to preclude shadowing, skipping, and bridging of the solder joints (see Figure 1.5.5.1-2).

1.5.5.2 Tooling Holes

Accurate alignment of the interconnecting structure and assembly fixture is accomplished by providing a minimum of two (preferably three or four) nonplated holes located in the corners of the structure. The hole diameter is typically between 0.100 and 0.150 inch. Specific sizes and locating requirements should be obtained from manufacturing prior to start of layout.

Annular Ring Clearance Diameter = 2 x (F + A + P)
= 2 x (0.005 + 0.005 + 0.005)
= 0.030

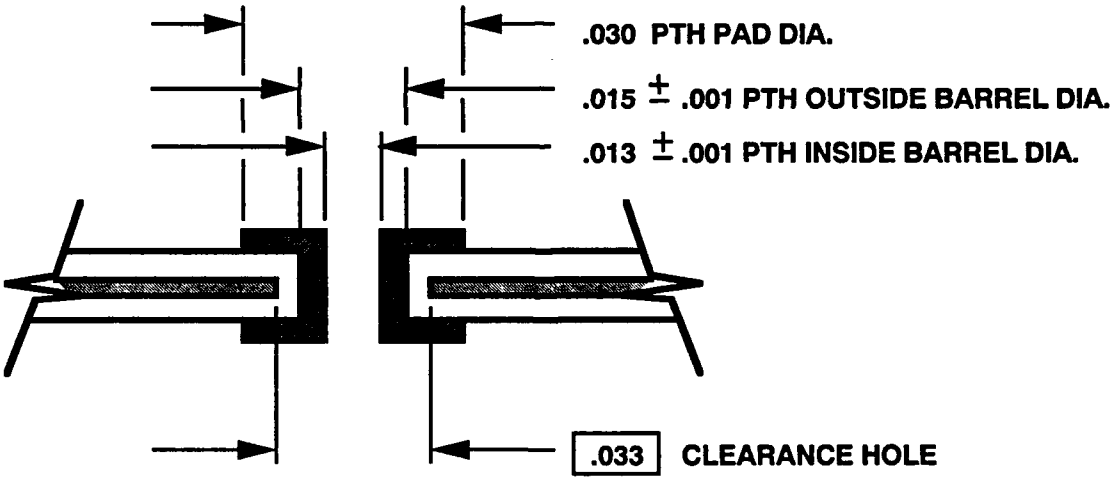
F is Film Error Allowance

A is Alignment Error Allowance

P is Processing Error Allowance

Under Cut Allowance = 2 x C
= 2 x 0.006
= 0.012

C is Core Thickness



+ .015 PTH OUTSIDE BARREL DIA.
+ .030 ANNULAR RING CLEARANCE DIA
- .012 UNDER CUT ALLOWANCE-(ANNULAR RING)

.033 CLEARANCE HOLE

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Figure 1.5.4.1. CIC Clearance Hole Calculation

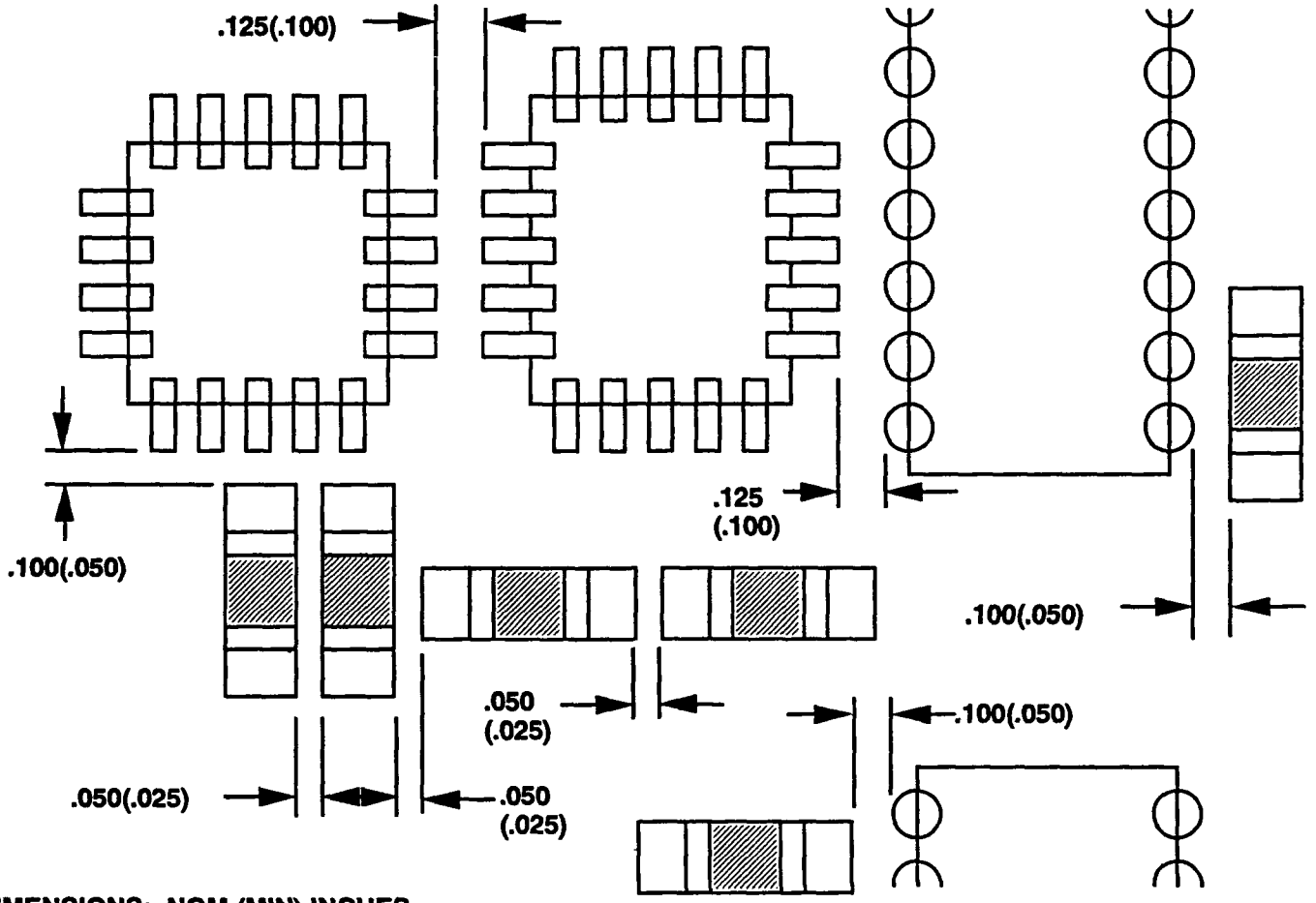

Figure 1.5.5.1-1. Recommended Land to Land Clearances

1.5.5.3 Fiducial Targets

Equipment utilizing optical alignment for improved registration requires targets be placed on the interconnecting structure. The targets or fiducial markes, are usually placed near the tooling holes but should be at least 0.25 inch from the board edge. For structures with the longest dimension 10 inches, two targets minimum are required at diagonal corners. For structures with the longest dimension greater than 10 inches, targets are required at all four corners.

Two targets (minimum) are also required for each high pin count multileaded carrier with leads on 0.020–0.025 inch pitch. The targets should be placed on the diagonal as close to the corners as possible and may lie within the footprint area. Specific target designs (dots, cross hairs, etc.) should be determined by the manufacturing engineer responsible for the vision placement equipment.

1.5.5.4 Automatic Placement

To take full advantage of surface mount technology, automatic placement equipment must be used to the greatest extent possible. Automatic placement affects the layout in two main areas. One is the clearance area required along two or more sides of the structure for handling and

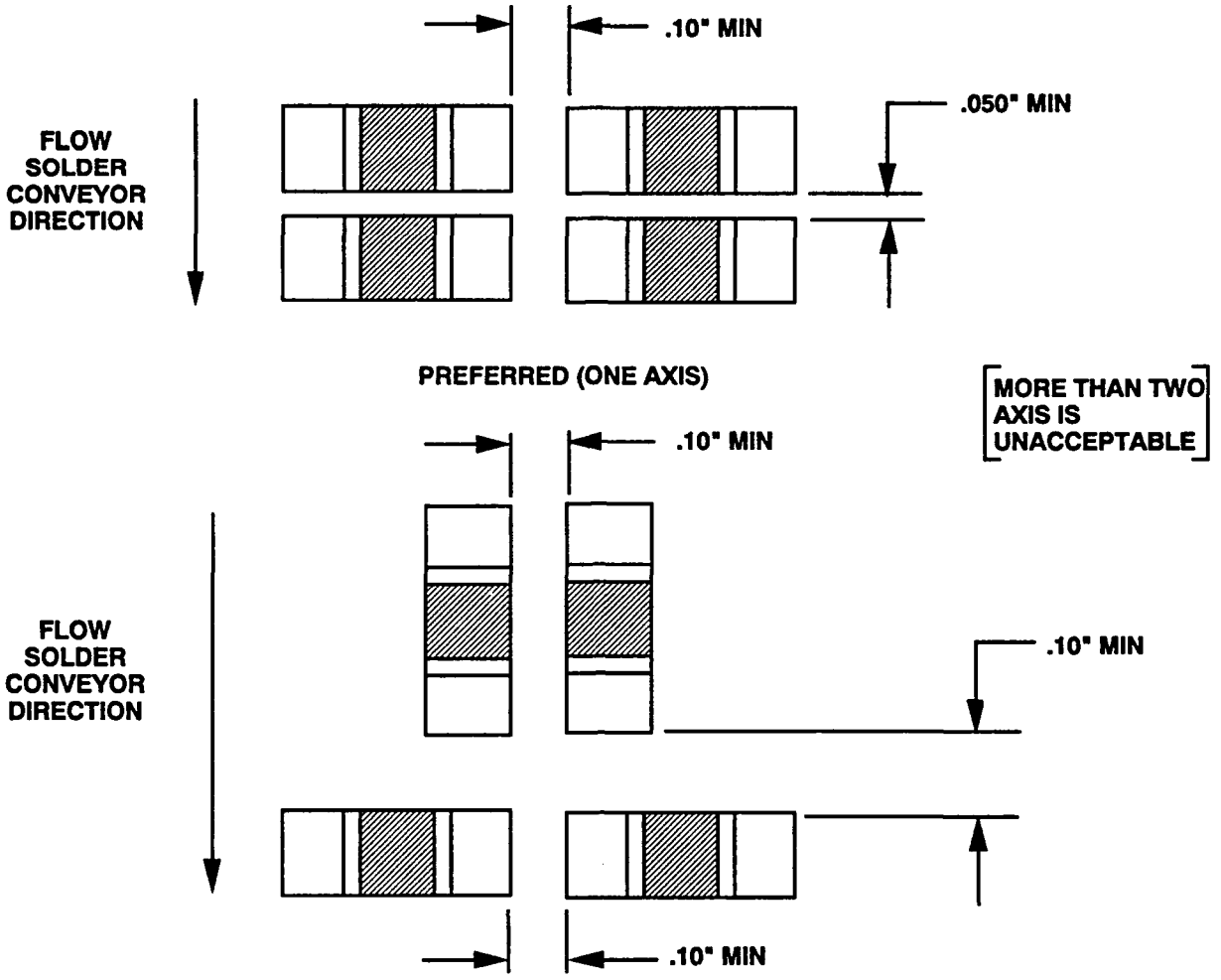

Figure 1.5.5.1-2. Chip Component Mounting for Wave Soldering

fixturing equipment. The other is the clearance area required for various components and the type of pick and place head used. Equipment and fixturing clearance requirements should be obtained from manufacturing prior to start of layout.

1.5.6 Masking Requirements

The design guidelines presented, especially those pertaining to minimum line width and spacing, are based on the assumption that a solder mask is used. Besides providing an insulating dielectric, the mask constrains the solder paste on the land pattern and prevents the solder from flowing to an attached circuit or via. Large areas of copper should be avoided on the outer layers or have reliefs provided to allow contact between the mask and substrate material. The mask should be applied over bare copper prior to tin/lead plating for proper adhesion.

The solder mask must meet the applicable requirements of IPC-SM-840 which defines two types and three classes of solder mask. The two types are wet film and dry film. Wet films

usually have an epoxy base that provides excellent adhesion, although there are two major drawbacks. Larger clearances are needed around solder lands because wet films require increased registration tolerances. Wet films also wick into unplugged vias. It is difficult to maintain a minimum thickness at the interface of the via barrel and structure surface due to this wicking. Dry films are applied by a laminating process and then photoimaged, developed, and cured. Dry film masks provide a uniform tent across via holes, and a more uniform thickness across the board. Dry film solder mask is the preferred mask material. The three classes of solder mask are:

CLASS 1 CONSUMER PRODUCTS
CLASS 2 GENERAL INDUSTRIAL
CLASS 3 HIGH RELIABILITY

A dry film solder mask over base copper meeting the requirements of IPC-SM-840, Type B, Class 3, is recommended for all military applications. Figure 1.5.6 shows typical solder mask guidelines per MIL-STD-2000, Rev. A, Paragraph 5.3.20.3.

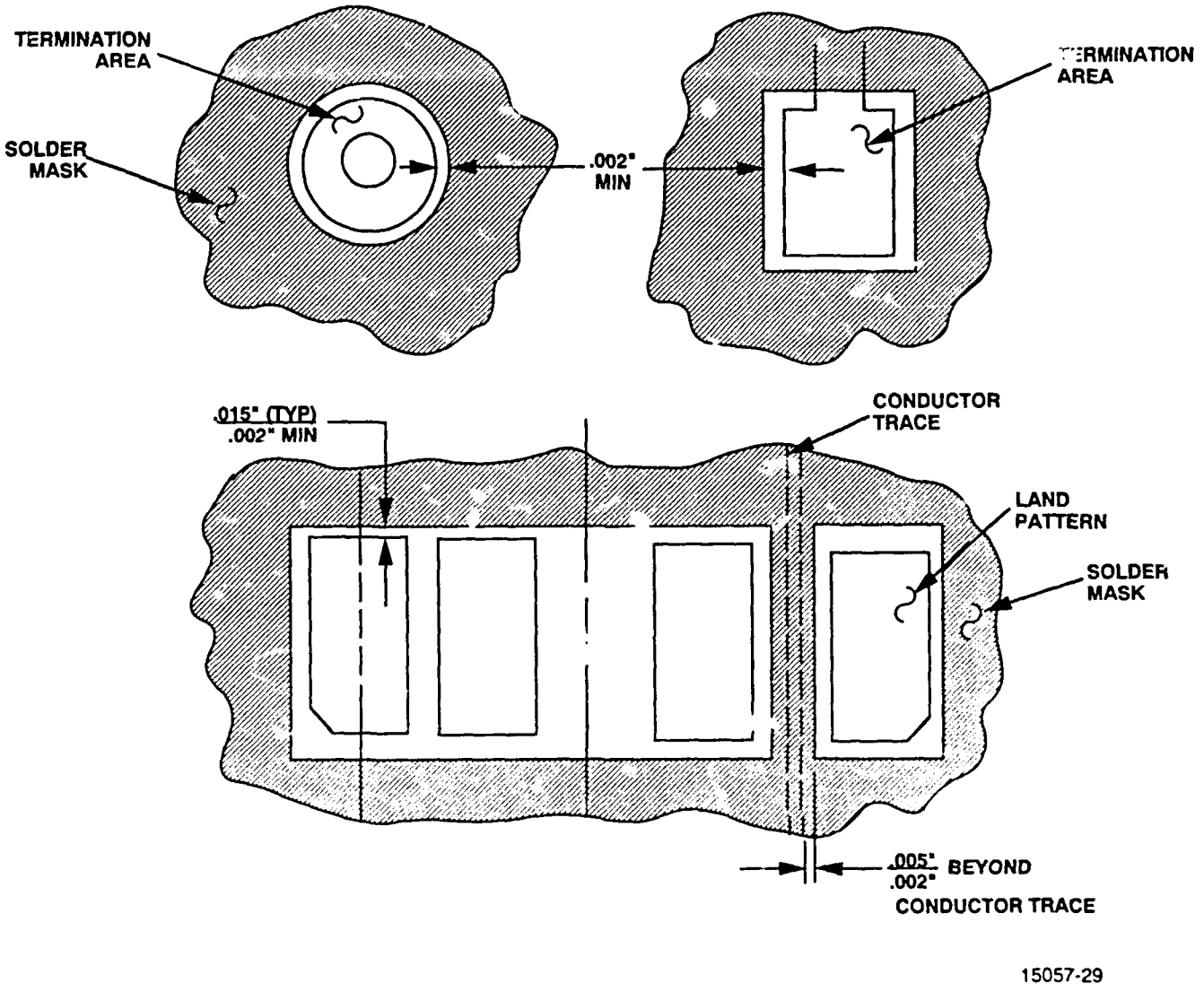

Figure 1.5.6. Polymer Solder Mask Window Size

1.5.7 Testing Requirements

Provisions for appropriate test access pads must be made at the start of layout. Separate pads must be provided for testing purposes. At no time should component solder pads or functional vias be used for probing. If automatic testing is considered, the test equipment to be used should match the standard grid used for layout. A 0.100 inch grid is the most economical and widely used grid. Automatic test equipment that uses a vacuum seal, such as bed of nails, usually require a minimum clearance of 0.100 inch around all edges of the board. Test pads should be isolated from their common solder pad by the use of a solder mask to ensure meeting solder joint requirements. Other test methods might be considered as alternatives to bed of nails testing as the real estate required for test pads often negates the advantage of going to surface mount in the first place.

1.6 Thermal Design Considerations

Due to the size of SMD's, greater thermal density on PWB's is possible versus PTH technology and will continue to be the future trend. This higher thermal density requires more efficient thermal management. Without an effective means of removing heat, junction temperatures will rise above acceptable limits.

1.6.1 Component Limitations

Component manufacturers publish data that show a typical MTBF of approximately 100,000 hours will exist at a T_j of 125 °C (see Figure 1.6.1). The MTBF decreases by a factor of ten at 150 °C. Because of this, many contracts require junction temperature derating to 105 °C. In order to maintain reliable components, special attention should be given to methods of providing an effective means of cooling devices. A graph produced by Gigabit Logic shows the effect of the junction temperature on the MTBF and FIT rate.

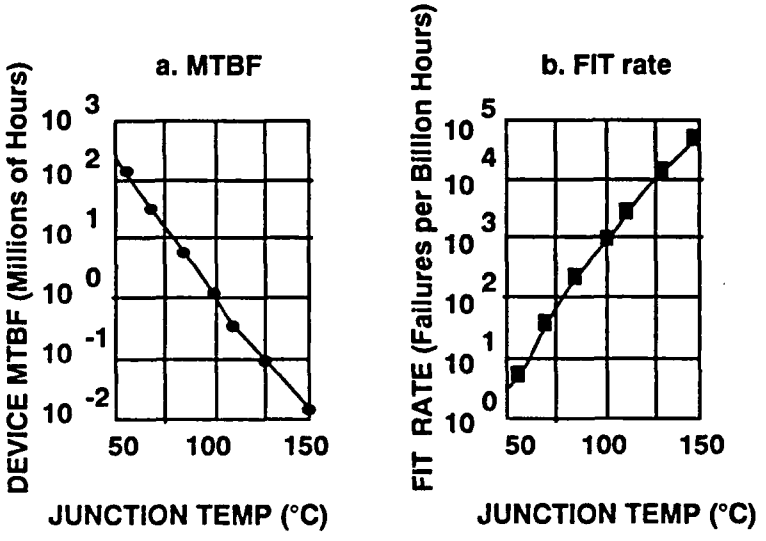

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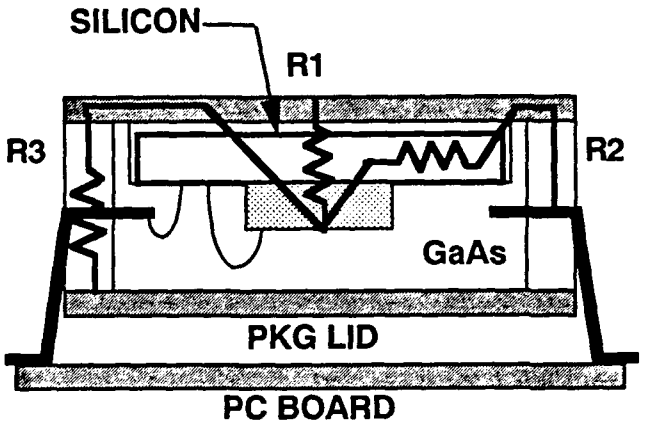
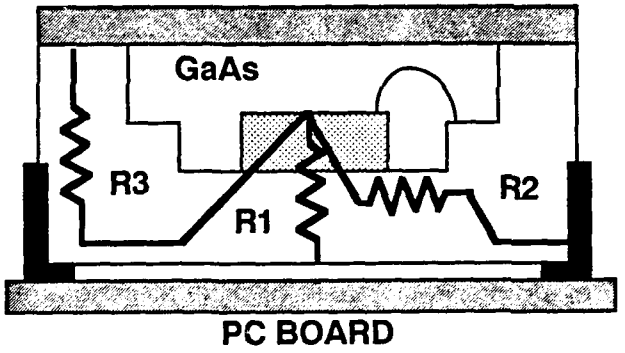
Figure 1.6.1

1.6.2 Thermal Paths

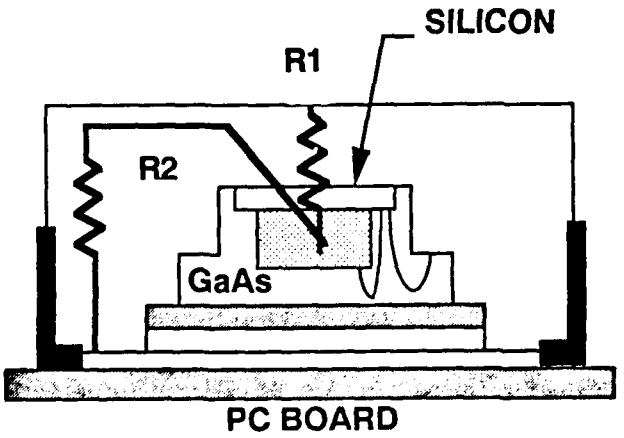
Most packages dissipate heat through a combination of conduction and radiation. Conduction exists between the package, the board, and the chassis. Radiation is more significant at higher temperatures and larger temperature differentials. The conduction path is through the package and then through the leads/solder joints and/or across an air gap. The package thermal resistances are determined by the package style and mounting configuration of the die. Some typical package cross-sectional views are shown in Figure 1.6.2 for various internal thermal paths. A typical leadless package has a thermal resistance (junction to case) of about 30 °C/W. A typical



a. 36 LEAD FLATPACK (F-36)



b. 36 I/O LCC (L-36)



c. 40 I/O LEADED AND LEADLESS CHIP CARRIERS (C-40 AND L-40)

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Figure 1.6.2.

flatpack and dip will have thermal resistances of about 40 and 20 °C/W respectively. Although the DIP has the lowest typical thermal resistance, it also has the largest footprint. When the ratio of the thermal resistance to the footprint area is compared, the leadless package is the best choice.

1.6.3 Heat Removal Techniques

SMT allows for the possibility of increasing packaging density and therefore more heat per unit area must be removed. This section deals with methods for increasing heat removal. Several methods are available to improve the heat dissipation of the package. Thermal shunting is a method of dissipating heat directly from the die through the use of thermal vias. A thermal via is usually in the form of a small metallic slug imbedded in the floor of the package. These thermal vias can then be soldered or attached with an RTV adhesive to the PWB. The ultimate effect is to reduce the junction temperature by shunting the usual package resistances. Figure 1.6.3 shows the bottom view of a 36 I/O LCC and its grouping of thermal vias.

For reducing package thermal resistances, copper leads are a significant improvement over Kovar and should be used wherever practical. Kovar is the standard material for leads, but copper has a thermal conductivity that is over 20 times that of Kovar. The CTE of the copper, however, is much greater than that of ceramic and should be assessed in light of potential CTE incompatibility with ceramic packages. Leadless inverted devices (LID's) are another packaging methodology that can be used to enhance thermal dissipation. In a LID, the die is mounted directly to the floor of the package. Since the package is ceramic and the leads have relatively large cross-sectional areas, the thermal resistance of the package is relatively low.

In a leadless chip carrier, larger solder joints provide a much better heat conduction path to the PWB. The effectiveness of the solder joints at removing heat depends on the consistency of the size of the solder joint. Large solder joints provide better heat transfer due to the larger cross-sectional area.

Certain low boiling point liquids can be used to control package temperatures. Nucleate boiling is a very effective method of removing excess heat. It can ensure the package temperature does not greatly exceed the boiling point of the liquid. Heat pipes work on the principle of nucleate boiling. Weight considerations must be made before using this method.

The Cray supercomputer uses oil to prevent hotspots. The oil is effective in evenly distributing the heat generated by individual components. It has a very high value of specific heat. The key here is to distribute the heat to avoid hot spots.

1.6.3.1 Packaging and Interconnect Structure (P&IS) Level Heatsinking

The P&IS thermal design must be able to dissipate the extra heat that results from the more densely populated boards that result from the use of SMD's. There are a number of board level cooling techniques that can be applied to SMT. One of the most popular methods of cooling a circuit card assembly is the conducting heatsink plate. This is usually an aluminum and/or copper plate that is bolted or bonded to the PWB. The heatsink provides a good heat conduction path to the box-level thermal management system (a thermally controlled mounting surface or a corrugated

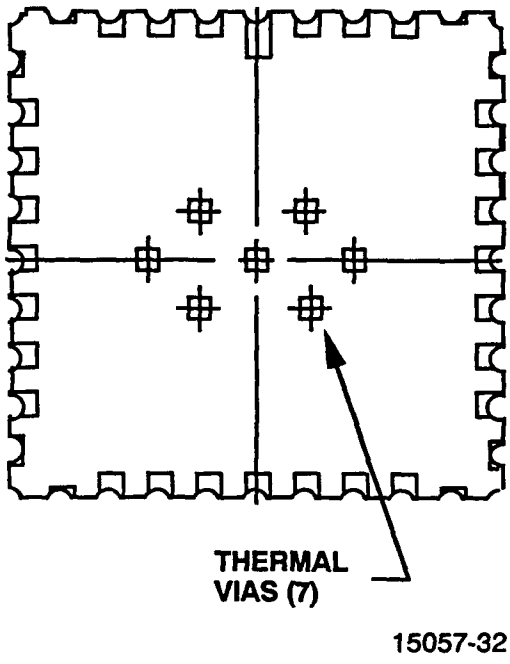


Figure 1.6.3. 36 I/O LCC (L-36)

fin heat exchanger integrated into the chassis side walls). However, due to the previously mentioned importance of CTE compatibility, a simple aluminum or copper heatsink may be inappropriate for some SMT applications.

Instead of the simple aluminum or copper conduction heatsink, a constraining core can be used in the card. There are copper clad invar cores that provide both a heatsink conduction path and mechanical restraint that forces the composite P&IS CTE to more closely match the SMD CTE. In some applications, the low conductivity invar based core may be inadequate for the power density of the card. In these cases, an alternate clad core arrangement can be used. Copper clad molybdenum cores provide the same CTE control as copper clad invar, but with a superior thermal conductivity, especially in the direction perpendicular to the PWB plane.

An even more thermally desirable approach is the hollow-core card design. This method eliminates the heatsink to card edge temperature gradient by placing the coolant flow next to the heat dissipating components. This provides a greatly improved heat dissipation path. The hollow core should be of the familiar corrugated core configuration. In many applications, the core can be made of aluminum or copper. However, as with the conduction heatsinks there may be a number of SMT applications for which this is inappropriate. In these cases, the core can be made of thin sheets of copper clad invar foil or copper clad molybdenum foil. This approach combines the enhanced heat dissipation features with the improved CTE control.

One additional benefit of this approach is improved resistance to vibration and shock. The composite structure formed by the corrugation sandwiched between two plates provides a stiffness-to-weight ratio that far exceeds what is possible with a thin solid core. The resulting P&IS resonant frequencies are higher and the dynamic deflections significantly smaller.

A more exotic method of cooling the circuit card assemblies retains the low thermal impedance characteristics of the hollow core heatsink approach without the need for coolant. Instead of a heat conducting heatsink plate, flat-plate heat pipes can be used. The heat dissipated by the card can be transferred to the side wall of the chassis with about the same temperature rise that would occur between the card and the coolant flow in the hollow core heatsink approach. This approach is desirable when coolant is not available (either avionics or spaceborne applications).

Thermal management can be further enhanced by improving the thermal path that exists between the SMD's and the heatsinks. The most popular method of doing this is to incorporate thermal vias in the PWB design. A fairly easy way to do this is to use filled plated-through holes (PTH). The most common fill material is solder since the vias are easily filled during wave soldering. However, any fill material with a thermal conductivity that exceeds the nonconducting component of the P&IS stack-up is an improvement. The reader should be aware that PTH's that are only partially filled with solder result in a reduction of PTH reliability and that verification of solder fill is impossible without x-ray inspection. For this reason, thermal PTH vias should not be electrically active.

EXAMPLE 1.6.3.1

Purpose:

Determine the thickness and weight of a constraining core assembly for a SEM-E module

Given:

- Two 0.040" thick glass epoxy PWB's bonded to a Copper/Moly/Copper (CMC) core.
- Total module power of 25 watts
- Maximum center line PWB surface temperature of 60 °C
- Rail temperature of 30 °C
- Edge resistance to heat transfer of 0.5 °C/W
- Module dimension of 6.0" x 6.0"
- CTE of assembly required is 7.5 ppm/°C

Properties:

	CTE [ppm/ °C]	E [psi x 10^6]	k [W/in °C]	density [lb/in^3]
G-10 PWB	15.6	2.5	0.044	0.066
Copper	16.8	5.6	10.1	0.32
Molybdenum	5.4	50.0	3.69	0.31

Method:

The total resistance to heat transfer is

$$R_T = \frac{\Delta T}{0.5P} \tag{1}$$

Where ΔT = temperature difference from PWB surface to rail

P = total power

$$R_T = \frac{60-30}{0.5(25)}$$

$$R_T = 2.4\ °C/W$$

The total resistance is also given by

$$R_T = R_{PWB} + R_S + R_e \tag{2}$$

R_{PWB} = printed wiring board resistance

R_S = substrate resistance

R_e = edge resistance

R_{PWB} can be calculated by

$$R_{PWB} = \frac{t_{PWB}}{k_{PWB} LW} \tag{3}$$

$$R_{PWB} = \frac{0.040}{0.044(6)(6)}$$

$R_{PWB} = 0.025$ °C/W

Solving for the substrate resistance in equation (2)

$R_S = R_T - R_{PWB} - R_e$
$= 2.4 - 0.025 - 0.5$

$R_S = 1.875$ °C/W

The substrate resistance can be expressed as

$$R_s = \frac{W}{4k_S t_S L} \tag{4}$$

Equation (4) is derived by assuming uniform power distribution (1).

Solving for $k_s t_s$

$$k_S t_S = \frac{6}{4(1.875)6}$$

$k_s t_s = 0.1333$ W/°C

Parallel resistance is used to determine in-plane heat resistance of two materials.

$$\frac{1}{R_T} = \frac{1}{R_1} + \frac{1}{R_2} \tag{5}$$

Where $R_i = \frac{W}{k_i t_i L}$

Therefore the total substrate conductivity in terms of copper and molydbenum is:

$$k_S t_S = k_{cu} t_{cu} + k_m t_m \tag{6}$$

The thickness of copper and moly are unknown. Another equation is needed to determine t_{cu} and t_m. The CTE of the assembly (CTE_A) is expressed as:

$$CTE_A = \frac{CTE_{PWB} E_{PWB} t_{PWB} + CTE_{cu} E_{cu} t_{cu} + CTE_m E_m t_m}{E_{PWB} t_{PWB} + E_{cu} t_{cu} + E_m t_m} \tag{7}$$

Solving two equations (6) and (7) and two unknowns (t_{cu} and t_m), the following equations can be derived:

$$t_m = \frac{CTE_{PWB} t_{PWB}(CTE_{PWB} - CTE_A) + \frac{E_{cu}}{k_{cu}} k_S t_S (CTE_{cu} - CTE_A)}{\frac{E_{cu}}{k_{cu}} k_m (CTE_{cu} - CTE_A) + E_m (CTE_A - CTE_m)} \tag{8}$$

$$t_{cu} = \frac{k_S t_S - k_m t_m}{k_{cu}} \tag{9}$$

Substituting the values in equations (8) and (9)

$$t_m = \frac{2(2.5)(0.040)(15.6 - 7.5) + 5.6\,(0.1333)(16.8 - 7.5)}{\frac{5.6(3.69)}{10.1}(16.8 - 7.5) + 50\,(7.5 - 5.4)}$$

$$= 0.019 \text{ inch}$$

$$t_{cu} = \frac{0.1333 - 3.69\,(0.019)}{10.1}$$

$$t_{cu} = 0.006 \text{ inch}$$

The total core thickness is

$$t_s = t_{cu} + t_m$$
$$= 0.006 + 0.019$$
$$= 0.025 \text{ inch}$$

A percentage breakdown by volume of the core is

$$\% \text{ Cu} = \frac{0.006}{0.025}(100)$$

$$= 24\%$$

$$\% \text{ Moly} = 76\%$$

Calculating the weight of the core

$$m_c = (6.0)(6.0)[0.31(0.019) + 0.322(0.006)]$$

$$m_c = 0.282 \text{ lbs.}$$

The weight of the assembly is

$$m_A = 0.282 + (6)(6)[2(0.040)](0.066)$$

$$m_A = 0.472 \text{ lbs.}$$

Results:

The heat can be dissipated from the module using a 0.025 inch thick 12/76/12 copper/moly/copper core. The core weight is 0.282 pounds and the assembly (P&IS) weight is 0.472 pounds.

1.7 Circuit Performance

Circuit performance in SMT PWB design involves a number of considerations depending on the type of circuit function, such as digital, analog or RF, and its application environment demanding EMI/RFI control. Other factors such as power dissipation or use environment are also important.

The intent for these guidelines is to be as complete as practical within predicted future SMT usage. Therefore, the initial guides will focus on the most probable areas, namely high speed, high density digital circuit applications with emphasis on EMI control.

1.7.1 High-Speed Digital PWB Design

When frequencies of operation began to exceed 10 MHz and rise times became faster than 20 ns, layout precautions began to become a critical concern. Future projections for SMT applications suggest much higher operational frequencies and correspondingly faster rise times.

To ensure adequate system performance, impedance control, crosstalk minimization, and EMI/RFI control have become important concerns. The following paragraphs deal briefly with these concerns.

The reader is referred to an article by several authors from TI entitled Design Trade-Offs Between Organic Polymer-on-Metal PWBs and Ceramic Thick Film PWBs for High Density Operation Using Leadless Ceramic Chip Carriers for many useful comparisons relative to circuit performance utilizing these types of substrates.

1.7.1.1 Impedance Control

High frequency signals will be reflected due to discontinuities in characteristic impedance. The greater the discontinuity, the greater the reflection. These reflections can cause such anomalies as false gate triggering and signal distortion. Furthermore, the probability of discontinuities usually increases as the packaging density increases.

Since a primary reason for using SMT is to increase packaging density, designers utilizing SMT for high-speed applications must be concerned with minimizing discontinuities. Minimizing discontinuities means controlling impedance.

To control impedance means controlling the ratio of distributed inductance and capacitance over the length of a line. This is accomplished primarily through the use of transmission line technology. By properly employing such technology, one not only controls impedance, but also achieves:

- Controlled capacitance
- Reduced rise time degradation
- Reduced signal distortion
- Reduced crosstalk

Depending on the application, one must choose the optimum transmission line structure and correct relationships of design variables. Table 1.7.1.1 is included as a guide in this selection process.

Table 1.7.1.1. Comparison of Transmission Line Structures

	COPLANAR	MICROSTRIP	STRIPLINE
Construction	Signal and return paths are etched in same plane	Replaces the return trace with a full ground plane	Groundplane is both above and below signal lines
Field Area	Much of the field extends into the air surrounding the circuit, particularly in high impedance circuits	Most is confined between signal conductor and groundplane	Entirely confined between signal conductor and ground place
Practical Impedance Range	45–50 ohms	15–150 ohms	10–100 ohms
Crosstalk	Moderate	Low	Very low
Major Design Variables	Spacing of signal and ground lines Conductor width Cover and base film thickness	Signal conductor width Distance of signal conductor from groundplane	Signal conductor width Distance of signal conductor from both groundplanes
Comments	This relatively inexpensive structure is the simplest and most commonly used transmission line Circuit impedance is sensitive to adjacent metal, metal chassis, etc. Good for low- to medium-speed applications	Better impedance control than coplanar structures Reduced crosstalk Circuit impedance is comparatively insensitive to metal chassis Increased signal line density because no ground lines are in same plane as signal lines Better than coplanar for high-speed applications	Better impedance control and lower crosstalk than microstrip construction Circuit impedance is very insensitive to metal chassis Increased signal line density because no ground lines are in same plane as signal lines Excellent signal transmission characteristics Outstanding suppression and shielding characteristics where EMI/RFI is a concern Best structure for high-speed applications

Equations used in the design calculations for the various structures are relatively standard for PWB's and can be obtained from a number of sources, such as the Fairchild or Motorola ECL Design Handbooks. Software programs such as LineCalc and SPICE are available.

Process control may affect performance. In some instances, fabrication and testing of circuit samples will be necessary to verify process control in order to ensure adequate results.

1.7.1.2 Crosstalk

In many applications, crosstalk minimization is a major concern. Crosstalk is a signal generated in a victim line through inductive and capacitive coupling to a source line. Figure 1.7.1.2-1 illustrates the concept.

Backward, or near end, crosstalk is present in all circuits. Forward, or far end, crosstalk is a problem where the circuit is long in relation to the rise time of the signal. Optimum circuit performance is achieved by eliminating forward crosstalk and minimizing backward crosstalk.

SMD's have shorter, more regular lead lengths internal to the packages in many cases as compared to similar functioning packages not surface mounted. Figure 1.7.1.2-2 illustrates one of the advantages of this configuration.

1.7.1.3 EMI/RFI Control

Some programs demand close attention to EMI/RFI control or the use of inter-connections that are inefficient receivers and radiators of RF signals. Again the application may demand the use of transmission lines, which provide field control, especially microstrip and strip lines. Careful attention must be given to layout features that cause impedance discontinuities such as pads and fan-outs.

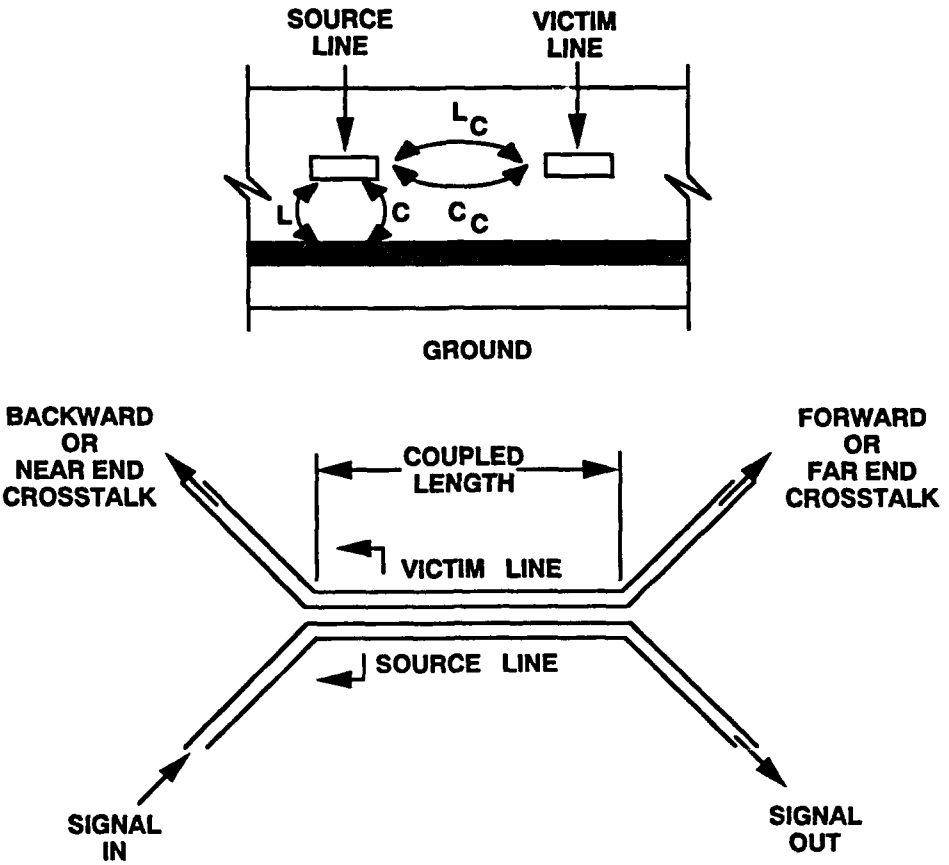
SMT designed PWB's potentially offer better control of EMI/RFI. The improved control is possible primarily because through-holes for leads are not required, thus allowing a more effective use of isolation planes. To ensure adequate control is achieved, however, good design practices must be established (and followed) in the front-end design definition phase of a program. Such practices are usually documented in an EMI/RFI control plan.

An excellent reference source is "EMI Shielding Theory" in Chomerics EMI Shielding Engineering Handbook.

1.7.2 High-Speed CMOS

Since many designs will involve high-speed CMOS, this application section of the circuit performance design guide lines is presented. The following precautions are intended to include both electrical and mechanical designers in an interactive mode.

- Keep V_{cc}-bus routing short. Use strip-line, transmission-line, or ground-plane techniques.
- Keep ground lines short, and as wide as possible. Use separate ground traces to supply high-current devices.



For ideal coupled transmission lines under typical conditions.

$$FXT = \frac{(K_c K_l)\sqrt{\lambda LC}}{2t_r} \quad BXT = (K_c + K_l)/4 \quad K_c = C_c/C \quad K_l = L_l/L_c$$

Where:

FXT = Forward crosstalk as a percentage of the amplitude of the signal in the source line

BXT = Backward crosstalk as a percentage of the amplitude of the signal in the source line

K_c = Capacitive coupling factor

K_l = Inductive coupling factor

*per unit length transmission line

L = Source line inductance with respect to ground*

C = Source line capacitance with respect to ground*

L_c = Coupling inductance*

C = Coupling capacitance*

t_r = Signal rise time

λ = Coupled Length

Figure 1.7.1.2-1. Crosstalk

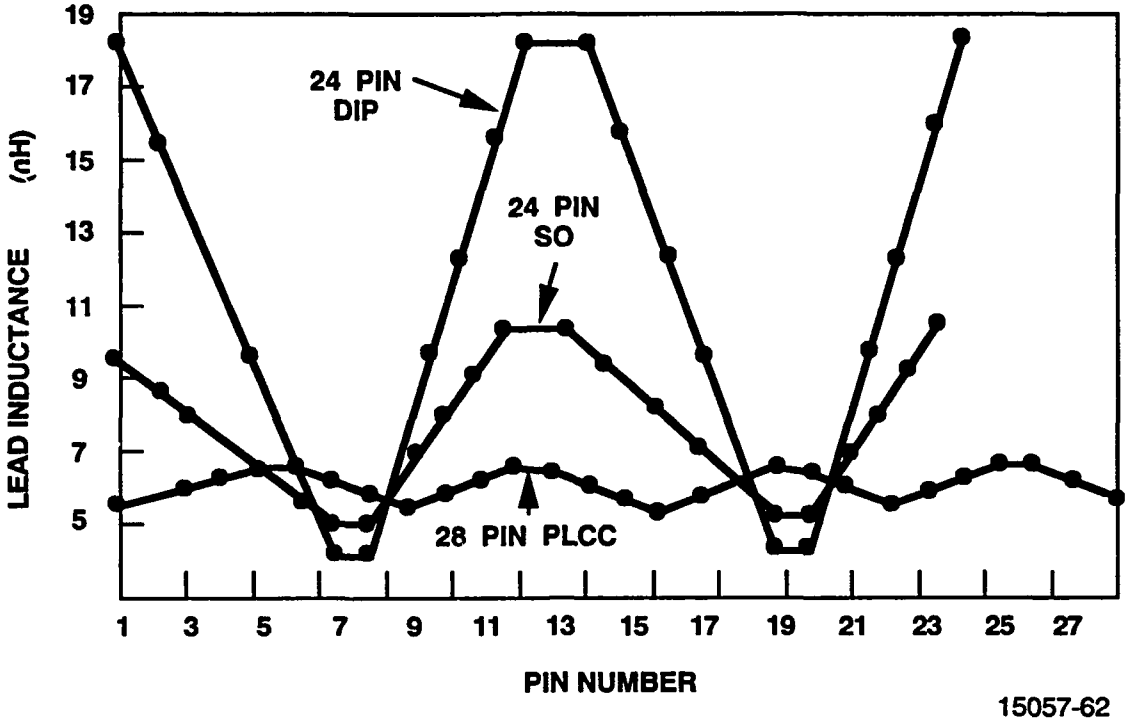


Figure 1.7.1.2-2. Comparison of Lead Inductances of Various Package Configurations

- In systems mixing linear and logic functions and where supply noise is critical to the analog component's performance, provide separate supply buses, or even separate supplies.
- Provide localized decoupling. For random logic, a rule of thumb dictates approximately 10 nF (spaced within 12 cm) for every two to five packages, and 100 nF for every 10 packages.
- For circuits that drive transmission lines or large capacitive loads (μP buses, for example), use a 10 nF ceramic capacitor close to the devices' supply pins.
- Finally, terminate transmission-line grounds near drivers.

1.7.6 References

1. Innovations in Controlled Impedance Interconnections—from a brochure published by Rogers Corp.
2. High Speed-CMOS Designs Address Noise and I/O Levels—EDN April 19, 1984.

1.8 Reliability Testing and Data Evaluation

New test data is constantly being published which propounds new revelations in SMT. This section is intended to arm the reader with the tools required to objectively evaluate data presented to him or her.

Reliability testing of surface mount designs is often required prior to commitment to a program or design. The number of test pieces required may be determined using the theory set forth in this section. Many previous studies have neglected statistical data analysis.

1.8.1 Sample Size Determination for Statistical Significance

The objective of sampling is to estimate unknown population parameters. Here we are interested in estimating the mean cycles to failure of solder joints under various test conditions. The question of how large a sample should the experimenter take in order to estimate the mean is a function of three factors. The first is the amount of variation in the data, generally described by the standard deviation. Second is the amount of precision desired by the experimenter. This is often referred to as the error of estimate. Third, sample size is a function of the confidence desired of the experiment.

One cannot state absolutely that the observed sample estimate is within a specified distance of the true population parameter. Thus, in stating a confidence level of 95 percent, for example, the experimenter is saying there is a 5 in 100 chance that the sample interval (sample value $\pm$ error of estimate) does not contain the true population value.

It is assumed that solder joint wear-out failures follow a normal or lognormal distribution. Based on this assumption, the principles of normal distribution can be used to determine the required sample size based on variation, desired precision, and confidence level. For small samples taken from a normal distribution, the following relationship exists:

$$\frac{(\bar{x} - \mu)}{\frac{\sigma'}{\sqrt{n}}} = t_{\alpha/2,df} \qquad (1)$$

where,

$\bar{x}$ = sample mean

μ = population mean

σ' = sample standard deviation

n = sample size

$t_{\alpha/2,df}$ = value from a t-distribution with $\alpha/2$ area in the right tail and df - degrees of freedom. This defines the 1-α probability area.

Rearranging equation (1) above gives

$$\bar{x} - \mu = t_{\alpha/2,df} \frac{\sigma'}{\sqrt{n}} \qquad (2)$$

In equation (2) the quantity $\bar{x}$-μ defines the error of estimate (the difference between the sample estimate, $\bar{x}$, and the true population parameter, μ). Since μ is unknown, the experimenter defines an upper limit for the quantity $\bar{x}$-μ.

$$(\bar{x} - \mu) \leq B \qquad (3)$$

Thus, substituting B in equation (2) and solving for n gives

$$B = t_{\alpha/2,df} \frac{\sigma'}{\sqrt{n}} \tag{4}$$

$$n = \left(\frac{t_{\alpha/2,df}\, \sigma'}{B}\right)^2 \tag{5}$$

Equation (5) shows that sample size, n, is a function of variation, σ', error of estimate, B, and confidence level $t_{\alpha/2,df}$

Looking again at equation (2) the relationship can be viewed in the following way:

$$\frac{\bar{x} - \mu}{\bar{x}} \times 100 = \frac{t_{\alpha/2,df}}{\sqrt{n}} \left(\frac{\sigma'}{\bar{x}} \times 100\right) \tag{6}$$

Now, $(\bar{x}-\mu/\bar{x}) \times 100$ is the percent error. The value $(\sigma'\mu/\bar{x}) \times 100$ is another method for expressing variation. Here variation is defined as a percent of the mean and is called the coefficient of variation (%COV).

$$\%\text{Error} = \frac{t_{\alpha/2,df}}{\sqrt{n}} \times (\%\text{COV}) \tag{7}$$

or

$$\%\text{COV} = \frac{\sqrt{n}}{t_{\alpha/2,df}} \times (\%\text{Error}) \tag{8}$$

Using equation (8), sample size curves were generated for various confidence levels and percent error. Figures 1.8.1-1 to 1.8.1-3 show sample size curves for 90, 95, and 99 percent confidence levels. To use these charts, the experimenter defines the desired percent error, confidence level, and an estimate of the coefficient of variation, if it is not known.

As an example, it may be desired to estimate the mean life of solder joints within 5 percent of the true mean at a 95 percent confidence level. It is believed that the coefficient of variation is about 12 percent. To determine the required sample size, look at the 5 percent error chart, Figure 1.8.1-2, and locate 12 percent coefficient of variation on the ordinate or vertical axis. From this point, go horizontal to the right until you intersect the 95 percent confidence line. Fromthis point read down on the abscissa or horizontal axis to the sample size. Thus, in order to estimate the mean within 5 percent of the true mean at 95 percent confidence, a minimum sample size of 16 must be taken.

Sometimes, in trying to determine sample size, a prior estimate of variation may not be available. In this case, the experimenter uses his best guess of the variation to determine the sample size. Once the data has been taken, use it to estimate the coefficient of variation. If this value is larger than the initial guess, determine the new required sample size and take additional samples to make up the difference between your initial sample size and the required sample based on the estimate. By taking this approach, one can maintain the desired percent error and confidence level.

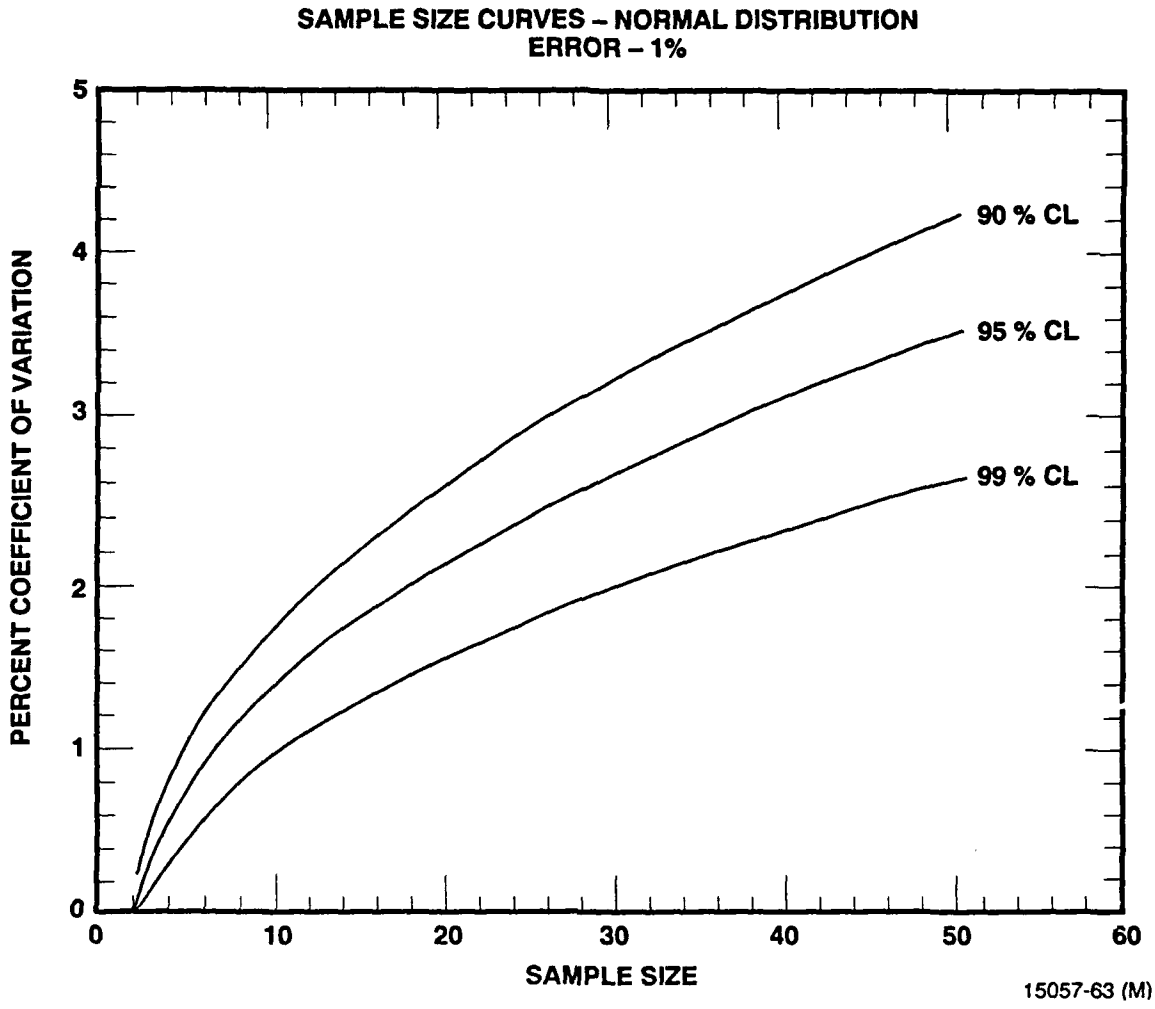


Figure 1.8.1-1. Sample Size Curves – Normal Distribution (Error 1%)

1.8.2 Data Analysis

The following factors must be studied to determine their effect on solder joint reliability or whether a meaningful correlation exists between the factor and solder joint reliability:

Controlled:

- Component
- Board material
- Temperature range

Measured or Monitored:

- Component location on board
- Reworked joints
- When in cycle a failure occurs
- Propagation of solder joint crack

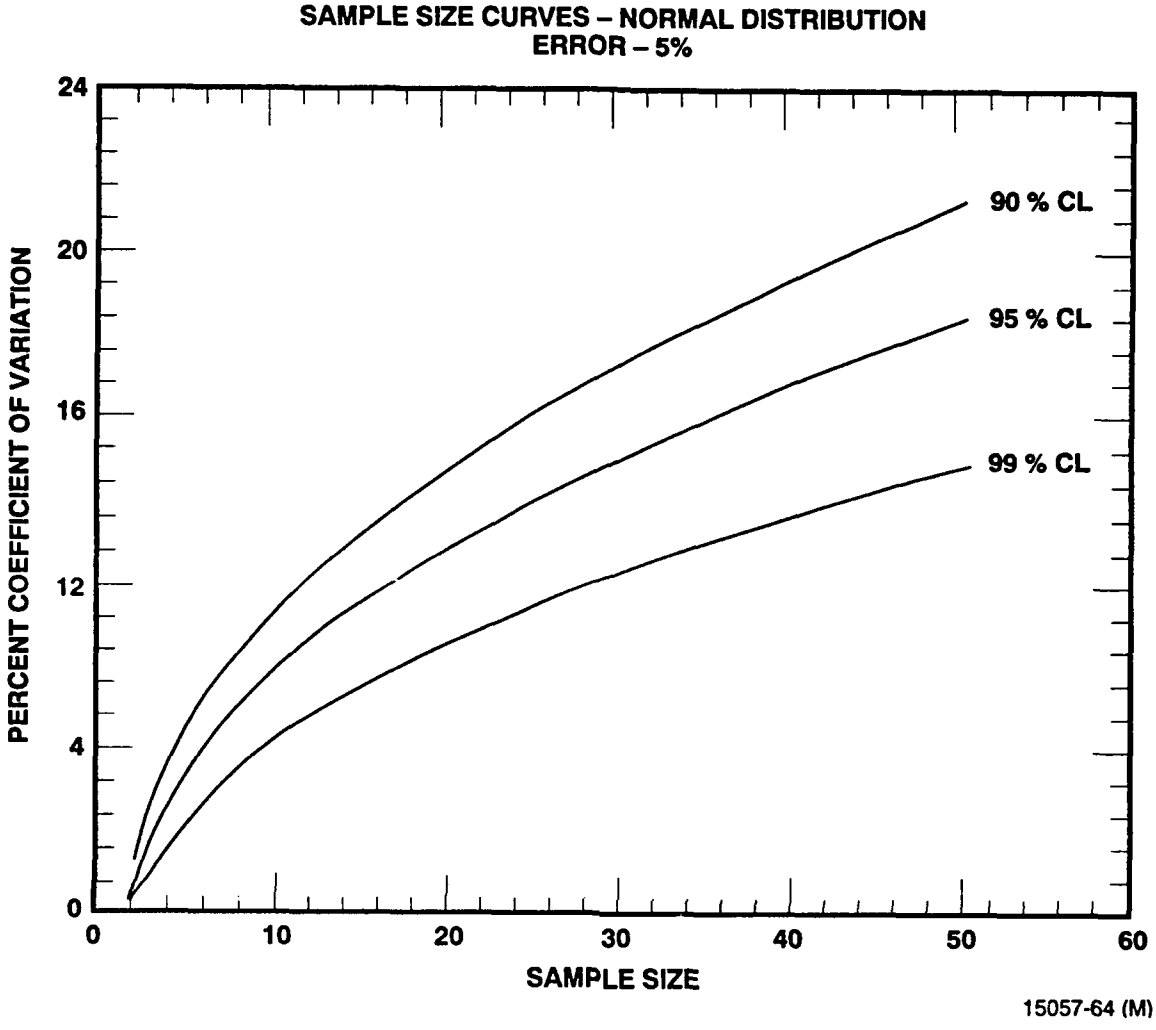


Figure 1.8.1-2. Sample Size Curves – Normal Distribution (Error 5%)

- Measured CTE
- Component size

1.8.3 Factors That Affect Solder Joint Reliability

Fixed Factors:

- Solder type
- Amount of solder
- Solder composition (purity, contaminants, fluxes)
- Solder temperature
- Solder placement method
- Process (temp, profile, handling, cleaning)
- Pad size

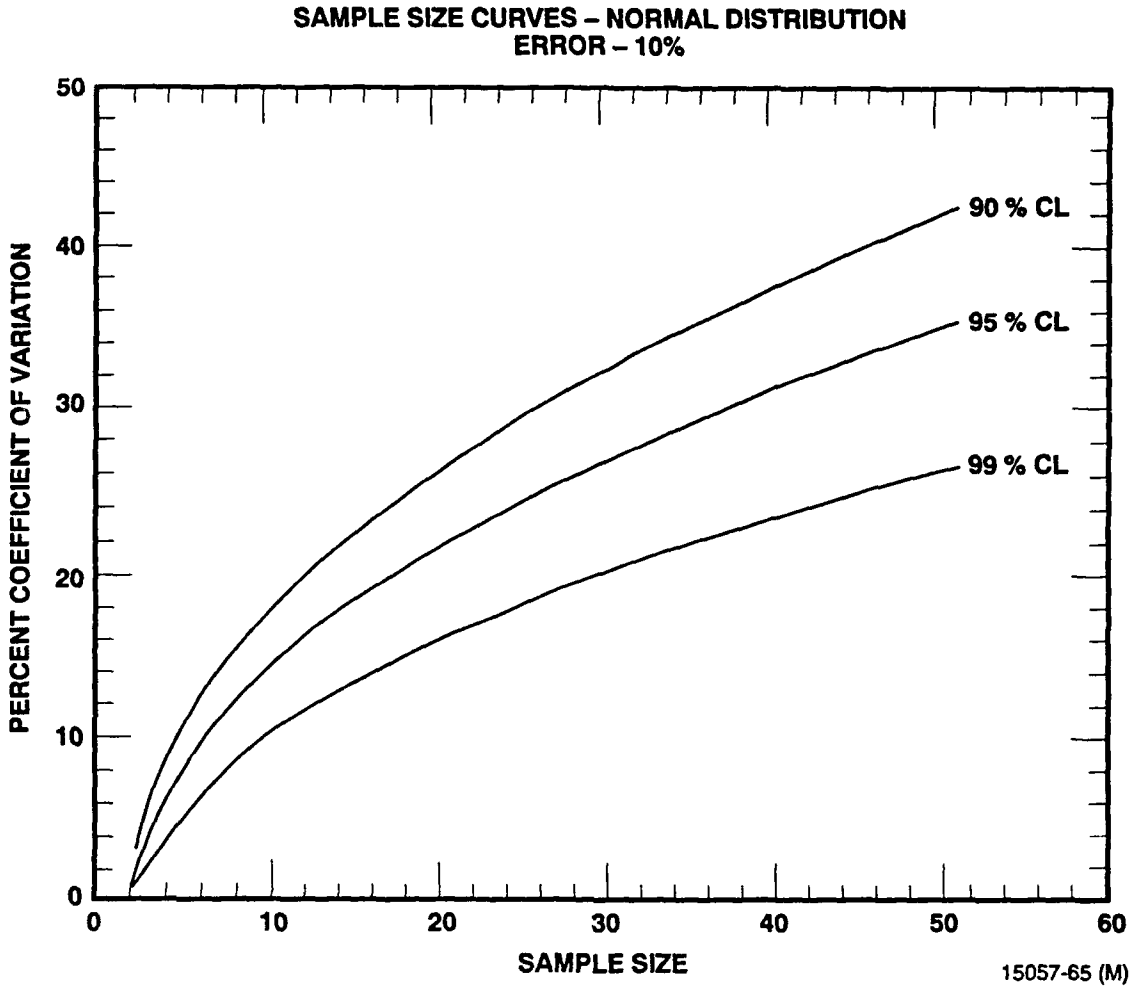


Figure 1.8.1-3. Sample Size Curves – Normal Distribution (Error 10%)

- Termination style
- Termination metal variations
- Fillet shape
- Board stiffness (result of clamp down)
- Location on board
- Cycles per hour
- Stress of test
- Type of components on board
- Number of components on board

1.9 Shock and Vibration Considerations

Mechanical resistance to shock and vibration, like thermal cycling, involves withstanding some number of stress reversal cycles. However, these stress reversals occur much more rapidly for a much larger number of cycles than those induced by thermal cycling. Fortunately, the stresses seen by leads and solder joints during shock and vibration are usually considerably less severe than the stresses resulting from thermal cycling.

The rapid rate of stress reversal during shock and vibration does not allow time for the solder creep to take place. Consequently, shock and vibration, as a typical design, will have high natural frequencies in an effort to lower displacements.

1.9.1 Component Level

At the component level, the same design practices that lead to good thermal fatigue life will also improve resistance to shock and vibration. They are:

1. Greater solder volume
2. More compliant solder geometry
3. Use leaded devices
4. Provide an additional mechanical load path between the SMD package and the board

1.9.2 Board Level

There is nothing new about shock and vibration design for SMT. The same design methods that are applied to through-hole technology also apply to SMT. The basic idea is to improve the stiffness-to-weight ratio of the printed wiring assembly so that higher resonant frequencies result. The higher natural frequencies result in much smaller dynamic board deflections and hence lower stresses imposed on solder joints and/or leads.

The most obvious method of increasing the natural frequency of a circuit card is to apply a low weight stiffening technique. Heatsinks often provide the needed structural support as do stiffening ribs. Hollow core heatsinks offer superior stiffening with the added benefit of superior thermal management.

A less obvious method of increasing the board natural frequency involves the proper selection of edge guides. High clamping force edge guides are preferred. These guides (wedge locks) create a nearly fixed boundary condition at the edge of the card. Simple card retaining clips and slots provide a simply supported edge. If all other factors are the same, the fixed edge usually results in twice the natural frequency achieved with a simply supported edge. thereby greatly reducing the dynamic displacements.

2 MANUFACTURING

The Manufacturing Section of this handbook is designed to indoctrinate the reader as to the general issues pertinent in the present state of manufacturing SMT assemblies. With the amount of new development taking place in process techniques and equipment, this in no way claims to be an all encompassing review. Simply, a general overview of manufacturing methods and concerns. Each contractor will have its own particular opinions as to which process is best or what equipment should be used. It is up to the contractor to develop and ensure that his processes meet the particular MIL-STD's for the contract and that his processes are controlled to provide predictable and repeatable results. Methods such as Statistical Process Control (SPC) are highly recommended and often required by a particular contract. SPC is virtually mandatory in a surface mount process to ensure the quality of the finished product. This is necessary due to the inherent design of surface mount devices and assemblies. The flexibility available in through-hole technology, to obtain a reliable solder joint, simply does not exist for SMT. Surface mount designs and component selection are more process-dependent than PTH technology, and the designer must have an understanding of the particular process methods which will be employed on his design.

2.1 Classification for Surface Mounted Assemblies

TYPE 1 – TOTAL SURFACE MOUNTING

- Only SMD's (no through-hole devices)
- All types of SMD's (including SOIC's and LCC's)
- High density
- Single- and double-sided

TYPE II – MIXED TECHNOLOGY

- SMD's on top, or on top and bottom
- Through-hole devices on top

TYPE III – UNDERSIDE ATTACHMENT

- Small SMD's (resistors, capacitors, and SOT's) mounted on underside of conventional through-hole assemblies

The most common type of surface mount board assembled in military applications is a Type II board with through-hole components and surface mounted components. Type I has become more popular with the increased availability of SMD's.

2.2 PWB Preparation

Prior to assembling any printed wiring board, either surface mount or through-hole, it must first be clean and free of dirt, grease, fingerprints, or other contaminants. It must be free of moisture in the inner layers to preclude measling or delamination. Most importantly, it must be solderable. The solderability of the board must be checked at receiving inspection by testing the accompanying coupon. Once solderability is proven, it must be maintained by proper packaging and

storage. If possible, a separate coupon should be kept with the board in storage to verify solderability has been maintained. Very seldom can a board be rejected at time of manufacturing; therefore, proper storage and shelf life considerations must be observed.

Once the PWB is ready for assembly, it simply needs to be cleaned and baked to remove moisture per the applicable manufacturing process. Further handling must be by the card edges, without contacting solderable surfaces or by wearing protective gloves.

2.3 Solder Selection and Screening

Solder selection will be made for process requirements within the allowances of federal specification QQ-S-571, Solder Tin Alloy: Tin-Lead; and Tin Alloy. Other alloys would require special consideration with technical reasons for variation.

2.3.1 Composition

The composition requirements for normal reflow or wave soldering are Sn63/Pb37. Any other solder composition meeting QQ-S-571 may be used as required for special applications such as when noble metal terminations are used. This is to prevent leaching of the noble metal from the end termination.

When two step soldering is performed, it is desirable to not reflow the first alloy. In this case, a lower temperature alloy should be used on the second reflow operation to prevent the first alloy from melting. However, this procedure requires special processing using two reflow heating ranges.

Examples: First soldering operation using Sn50/Pb50 solder with a reflow temperature of about 250 °C.

Second soldering operation using Sn63/Pb37 solder with a reflow temperature of 215 °C, thus preventing reflow of first alloy.

2.3.1.1 Temperature Requirements

The temperature requirement for eutectic Sn63/Pb37 solder is a liquidous/melting temperature of 361 °F (183 °C). Reflow temperatures should be approximately 50 °F (27 °C) above solder liquidous temperature.

Temperature limits of components must be noted prior to designing them into a surface mounted assembly. The high temperatures may melt or damage some components, especially standard through-hole types modified for surface mount application.

2.3.1.2 Contamination

Contaminants in solder in the form of various metals or compounds not found in the normal processing of solder are prohibited. In addition to meeting the purity requirements of QQ-S-571, virgin solder should meet the following requirements:

- ≦ 0.01% phosphorus
- ≦ 0.001% sulphur

This requirement precludes the use of reclaimed solder.

2.3.1.3 Surface Tension Effects Desired

The desired surface tension effect of the solder is to center any components which may be slightly misaligned from placement and/or handling prior to reflow. This is possible on smaller components, as the weight of larger components tends to overcome the solder surface tension. Caution must be used, for it is surface tension of the solder which also contributes to tombstoning. Avoid using tension properties as a process variable to center components.

2.3.2 Flux Selection

Rosin Mildly Activated (RMA) flux is, and will continue to be, the standard flux selection for Surface Mount soldering of components. This selection is based primarily per MIL-F-14256 covering solder fluxes permissible for military products and partly due to the problems associated with cleaning more highly activated fluxes. MIL-STD-2000, Rev. A is making some allowance for other fluxes, but caution should be used in arbitrarily selecting a more active flux. Flux residue being the prime concern.

2.3.3 Solder Paste Application Method

2.3.3.1 Stenciling

There are a number of requirements associated with using stencils to deposit solder paste. Two important considerations are desired paste thickness and volume considerations. It is recommended to use a stencil when emulsion thicknesses would be greater than 0.010" on a solder screen and when the highest possible volume of solder is required. The stencil allows for paste thicknesses of as much as 0.050" and, with the proper solder paste, provides the greatest volume of solder (barring special processing of screens). Another advantage to stencils is that they are much more durable than screens. Screen emulsions have a tendency to wear faster due to the abrasiveness of the solder paste. Deposit definition can diminish in as little as 50 squeegee passes over a screen emulsion. On-contact printing is required with stencils unless the stencil is mounted using a screen to suspend it. This allows for snap-off, required for off-contact printing. The purpose for using off-contact printing is to reduce solder paste smear problems.

2.3.3.1.1 Aperture Control

Chemical milling is best done from both sides for uniformity of hole size and ease of release of solder cream from the stencil. Thick stencils should have 80 percent of the hole milled from the side facing the circuit (0.015" and up).

The finished pattern hole size is also critical in the milling process. Depending on the vendor, the hole size may be 10–15 percent larger than the artwork positive image. Some vendors compensate for this growth by reducing the image during processing; others recommend reducing the image on the original artwork sent to them. This should be discussed with the stencil vendor prior to ordering.

2.3.3.1.2 Wet Thickness

The wet thickness of the deposit should correspond very closely with that of the stencil. The important factors to consider are the reflowed height of the solder and the volume of actual solder deposited. This is dependent upon the percentage of metal contained in the paste. Obviously, a higher metal content will leave a greater volume of solder. Particle size is also important to consider. If too large of a particle size is used, the entire pattern doesn't get filled and stencil openings may get clogged. Care must be taken when setting up the screen printer with the speed and pressure of the squeegee. Too much pressure may have a scooping effect and pull out solder paste from the stencil, reducing the volume of solder left on the board. If the squeegee speed is too fast insufficient solder may be deposited.

2.3.3.1.3 Viscosity Requirements for Stencil Printing

The viscosity of the solder paste is a measure of the relative thickness of the solder spheres, the flux, and any added thickener present in the paste mixture. The viscosity affects the flow of the solder paste during application as well as its ability to maintain its shape once deposited. Too low of a viscosity and the paste may slump and bridge together or cause solder balls upon reflow from being too spread out. Too thick of a paste may be difficult to dispense or apply with the screen printer. The required viscosity will vary depending upon type of stenciling machine and squeegee hardness. Typically, the recommended range for viscosity when using stencils is between 500,000 and 900,000 centipoise. Viscosity, at the high end of the range, is recommended for fine pitch printing applications.

2.3.3.1.4 Metal Foil Stencils

Advantages:

a. Stencils eliminate the mesh and print consistently without clogging. This includes very small and tightly spaced pads.
b. Stencils are made of metal foil, which is extremely stable and durable. They outlast screens 25:1.
c. Stencils are unaffected by chemicals or long storage periods.
d. Stencils are extremely accurate. Thousands of pads can be precision printed with solder in a single squeegee pass of the printer.
e. Stencils print at twice the speed of an emulsion screen. No flood stroke is necessary.
f. Stencils take half the time that screens take to set up and clean. Squeegees last much longer.
g. Stencils are very cost efficient in production situations.

Disadvantages:

a. Stencils are more complicated. More time is required to produce them.
b. Stencils are initially more costly, due to the additional tooling, material and labor involved in their manufacture. However, it is important to note that, in a production run, stencils far exceed screens in cost efficiency.

Printing With a Stencil

Stencil printing is far less complicated than screen printing. The stencil frame should be selected so that it fits easily to your printer. Select a frame that is sturdy but lightweight.

With the stencil in place and a circuit board on the table, look through the stencil pad openings and adjust the board visually until it aligns with the stencil. Secure the board in place.

Fill the stencil reservoir with paste, set the squeegee for minimum pressure and make a test print. Check for registration and adjust if necessary. If some areas are not printing, increase squeegee pressure. After a few adjustments, the setup is complete.

Mesh support system for the stencil incorporates tensioned polyester or stainless steel mesh around the periphery of the stencil. This provides flatness and flexibility for the stencil. It also makes it possible to run the stencil in the off-contact mode.

Stencil Design

Stencils are usually designed to match an electronic package. These packages have an ever-increasing number of leads or contacts on the bottom face. The stencil places solder paste on the circuit board pads in the same format as the package. Proper pad design is important. This opening, along with the stencil thickness, will determine the amount of solder at each location. Enough solder is needed to make a good mechanical and electrical connection; too much solder may cause bridging and an electrical short will occur.

Selecting the Right Material for the Stencil

There are basically four metals that produce acceptable printing stencils: Stainless Steel, Nickel, Beryllium Copper, and Brass.

The ideal metal should have the following properties:

1. Commercially available in a wide variety of widths and thicknesses
2. Easy to etch
3. Economical
4. Resistant to abrasion and chemical attack
5. Non-toxic

The only metal to fit all of these criteria is brass. Extensive field testing has found brass to be the best all-around metal for electronic stencils. The only exception would be on extremely thin foils—1–3 mils thick. Stainless steel is stronger and more damage resistant. A wide variety of brass foils, from 1 mil to 25 mils in 1 mil increments, are available with varying widths. Nickel plating of brass stencils may help to reduce wear when metal squeegees are utilized.

Stencils for Military and Short Run Applications

Stencils are becoming more and more popular for military and short runs. The logic behind this is simple: stencils can be stored for long periods of time without deterioration or loss of accuracy. When a reorder is received, the stencil can be retrieved from inventory and placed in production immediately. Thus, delays and quality variations are eliminated.

Subjects to be Considered

a. Frame Selection

1. Cast aluminum
   Advantages: Sturdy, rugged
   Disadvantages: Heavy, costly, limited sizes
2. Extruded square or rectangular tubing with welded corners
   Advantages: Sturdy, lightweight, available in a wide selection of cross sections. Can be fabricated to any size.

The frame size can be determined in the following manner:

1. Determine stencil image size—length and width.
2. Additional foil is needed at each end of the stencil in the squeegee direction. This space is a reservoir for the solder paste. Allow at least 2″ at each end.
3. Additional foil is also needed at the edges of the stencils. It is important for the squeegee to travel on the foil and not ride up on the mesh. The amount of extra foil is determined by the squeegee length. Add to this approximately 1″. At this point you have established the outer size of the stencil foil.
4. The stencil is supported around its periphery with mesh. Allow at least 1″ per side on small frames and 2″ per side on large ones. Add this to the foil dimensions and you have the correct minimum I.D. for the stencil frame

b. Stencil Thickness
Stencil thickness is extremely simple. The ratio is approximately 1:1—10 mils of metal foil will print 10 mils of solder. Conditions can be varied slightly by changing squeegee speed and pressure.

c. Artwork
In order to produce a solder stencil, artwork is required. This is usually in the form of a film positive (black image, clear background) and is supplied by the contractor. The quality of this film is most important in producing a quality stencil. The film should have the following information on it:

1. Film should be sharp and dense.
2. Reference center lines should be marked in horizontal and vertical directions.
3. The film should have the customer's or contractor's name, drawing number, and revision number on it.

d. Photo Tooling
Each stencil needs a registered set of film positives that are produced by the vendor. This is called photo tooling. To produce this tooling, a photocopy of your stencil image is required. This copy should appear as it prints on the board or as the stencil is viewed from the squeegee side. It should be marked with the following information:

1. Frame size and model number

2. Stencil thickness
3. Foil size
4. Image orientation and location
5. Critical image dimensions and tolerances
6. Overall image dimensions
7. Mounting mesh—SS or polyester

e. Image Orientation and Position in Frame

It is extremely important that the photocopy show how the stencil image is oriented to the frame. The stencil image is usually centered in both directions in the frame; however, when necessary, an offset in either or both directions is possible. This must be indicated on the photocopy, with reference to the center lines on the film positive.

f. Mounting Mesh

Mesh of SS or polyester is used around the periphery of the stencil. This mesh is necessary to provide tension to the stencil so that it lays flat and true. It also gives flexibility to the stencil so that it can be used in the off-contact mode on the printer, if desired. Polyester mesh provides the greatest flexibility and is the most forgiving. If there is a preference, be sure it appears on the photocopy.

g. Etch Factor

Stencils are produced by a photo etching process. The etchant not only etches through the metal, but sideways, enlarging the images by approximately 50 percent of the stencil thickness. This can be compensated for in the film positive, or modified by the vendor when pad openings are very critical.

h. Pad Size Variations

The pads or images in a stencil can vary widely. When relatively large and small pads are needed in the same stencil, different etch factors may be required.

2.3.3.1.5 Step Solder Deposition With Stencils

In many instances, different amounts of solder are required to be printed onto the PWB. For instance, the amount of solder required for small chip components is less than that required for LCC's. On a single board with a wide variety of component types, step stenciling may be desirable. Step stenciling requires a stencil to be etched to a thinner dimension in the areas required. The component vendor first etches the thickness in the desired areas and then follows with the standard pattern etch. The thickness of the stencil is based on the greatest thickness requirement.

Printer speed, pressure and squeegee durometer (hardness) may all need adjusting based on the amount of step variation on the stencil. Ten to twelve mils is about the maximum step obtainable based on vendor experience. Contact your stencil vendor for specific applications.

2.3.3.2 Screen Printing

Solder screens may be used in any application that does not require excessive paste thicknesses (over 0.006" emulsion) or high volume applications. Solder screens are considerably lower in cost than stencils, may be exposed in-house to increase shelf-life, and are more surface compliant than stencils, which require a small or very flat substrate. There are more manufacturers of screens available then stencil manufacturers and especially flexible mask producers. Thickness accuracy is considered very good and turnaround from vendors is considerably shorter than for stencils/masks.

2.3.3.2.1 Screen Mesh Size

Mesh size is an important factor when using screens to deposit solder paste in order to obtain the proper volume of solder deposited onto a PWB pattern. Generally low mesh counts provide the highest percentage of open area (typically 80 mesh). The range is approximately 60 to 400 strands per inch. Solder particle size is also an important factor in choosing a mesh size. The solder particles must pass through the mesh readily with little clogging. In most cases, with an 80 mesh screen, approximately 50 percent is open area and with every 0.001" increase in emulsion is a 100 percent increase in column open area.

2.3.3.2.2 Emulsion Screens

For many years, emulsion screens have been used, primarily in the hybrid field, to print small amounts of solder paste. Not until surface mounting came along was there a strong need to lay down large amounts of solder paste. Screens are still used today, but for short runs or prototypes only. Screens have severe limitations, as listed below:

a. Solder paste tends to clog screen mesh, producing voids and poor print quality.
b. Screen emulsions tend to wear rapidly, due to the abrasive nature of the solder.
c. Chemicals in the solder paste and cleanup solvent attack the emulsion.
d. Screen mesh blocks 50 percent of the image opening. Erratic print thicknesses are not uncommon.

2.3.3.2.3 Selectively Etched Emulsion Screens

Etched screens are very similar to standard emulsion screens, with one exception. Certain pads are etched to remove the mesh. This permits heavier laydown of paste in this area. However, all of the other disadvantages of emulsion screens still hold true.

2.3.3.2.4 Viscosity Requirements for Screen Printing

Viscosity requirements are about the same as for stencils, between 500,000 and 900,000 centipoise, depending upon application. Fine pitch applications typically require a higher viscosity. Consult solder paste vendors for specific needs.

2.3.3.3 Pneumatic Dispensing

Pneumatic dispensing of solder paste is ideal for dot or strip placing of solder paste. It is an excellent alternative to (relatively) expensive screens or stencils for low volume production or

lab work. It is also applicable for repair work. It is generally a less effective alternative to screening due to the inability to apply a consistent size or shape, although this may be alleviated as the sophistication of the equipment increases. Pneumatic dispensing generally requires a more fluid solder paste than for screen printing and may pose a problem where slump and flow out are important to control.

2.3.3.3.1 Wet Thickness

Typically, the measurement for dispensed solder paste is based upon the needle diameter, which will be about 1.5 times the needle I.D. This must be correlated to desired reflow volume, reflowed height, and percent metal of the solder paste.

2.3.3.3.2 Viscosity Requirements for Pneumatic Dispensing

Viscosity requirements for pneumatic dispensing are generally between 300,000 and 450,000 cps with 500,000 cps as a recommended maximum to ensure even flow of material.

2.3.4 Solder Paste Constituents

2.3.4.1 Alloys

Many more alloys are available and often recommended for reflow soldering because of the limited time that they are in a molten state. This limited time reduces the tendency for dross formation and intermetallic growth between the solder and the base metal (cu). The choice of a certain alloy depends primarily on the intended use. Some typical solder paste alloy applications are as follows:

60Sn/40Pb 63Sn/37Pb	For printed and flexible circuitry
62Sn/35Pb/2Ag	For printed and flexible circuitry where prevention of Ag leaching is reqired. (Chip components with only a Ag/Pd end termination).
10Sn/88Pb/2Ag	For thick-film silver-based conductor, sequential soldering and bumping
96.5Sn/3.5Ag	For lead frame assembly to thick-film circuits which may subsequently be wave soldered onto PWB's
10Sn/90Pb 5Sn/95Pb	For chip bumping, chip carrier elevation and components on bottom side of PWB
Pb/In	To avoid dissolution of gold plating into solder joint
50Sn/50Pb	Typically a plumber's solder, 50Sn/50Pb has shown slight improvements in thermal cycle life over standard alloy solders; its higher melting point, however, makes it less desirable as a standard process

2.3.4.2 Volatiles (Flux and Solvent)

The solder paste flux required to effectively wet most pads, component leads and terminations in surface mount applications can normally be met with an RMA flux. The solvent and viscosity modifiers determine drying time, tackiness, retention of tackiness, and viscosity of the

solder paste. These are usually proprietary constituents and are determined by the requirements of the processes involved in surface mount production.

2.3.4.3 Non-Volatiles (Non-Solder Residuals)

Normally, under proper processing conditions, both at the solder paste manufacturer and the end user, there is little to no residue besides the flux/carrier residue. However, if processing is not carefully controlled at the paste manufacturer, excessive oxidation may occur to the solder particles and may hinder wetting/reflow and leave some residues of oxidation on the surface. If good wetting occurs, some slight oxidation residue is usually harmless.

2.3.4.4 Particle Size

Solder powders are usually produced under stringent processing conditions to ensure uniform, spherical shapes which minimize surface oxidation formation.

There are typically three particle size ranges available:

Size 1or 'C' (Mil Designator)	-100, +200 Mesh approx 75 microns dia., avg. 150 microns dia., max.
Size 2 or 'B' (Mil Designator)	-200, +325 Mesh approx 60 microns dia., avg. 75 microns dia., max.
Size 3 or 'A' (Mil Designator)	-325, +400 Mesh approx 35 microns dia., avg. 45 microns dia., max.

The selection of particle size and shape is particularly important for screen printing or dispensing since large or irregular particles may clog up fine mesh screens or needle orifices. It is believed in some arenas, that a finer particle size is required for printing fine pitch devices, however, that is not a universally held position.

2.4 Placement Method Selection

2.4.1 Manual Placement

Manual placement is used in low volume/development builds using vaccum tweezers and visual (aided) alignment.

Manual placement can be very accurate, but the component size and pad size/ spacing play an important role. Most feel that 0.030" pad spacing is the smallest practical size to place manually. his method can be very reliable and repeatable up to the point of eye and/or mental fatigue. This varies with individual employees and can depend greatly on type of components and quantities involved.

2.4.2 Robotic Placement

2.4.2.1 Pick and Place Machines

There are numerous placement machines available on the market today, from simple, manually assisted machines to large high volume placement machines. Auto placers are used for both low-mix, high volume production as well as high-mix, low volume applications. The difference between the selected machines depends upon the mix and volume requirements, the type of components to be placed, and the accuracy required to place those parts. A machine to simply place large chip devices or large leadless packages does not require the sophistication of a machine required to place high pin count, fine pitched devices. Again, the designer should understand the limitations of the production equipment or the manufacturing capabilities prior to committing to a design.

2.4.2.2 Accuracy

Accuracy is defined as being able to move to a point that the manipulator arm has not been taught and to reach that point with little or no error. There are four basic types of accuracy; absolute, relative, palletizing, and regional.

- Absolute Accuracy—In this type of accuracy the points are addressed by absolute coordinate data; no points are "taught."
- Relative Accuracy—A point and direction (or two points) are taught. The points are addressed by the relative coordinate system.
- Palletizing Accuracy—Three points are taught, usually three corners. Individual points are addressed by fractions of a side.
- Regional Accuracy—This allows accuracy to be programmed within a specific region. Four points and the precise distances between these points are taught. Palletizing/regional accuracy is usually better than or equal to relative accuracy. Most quoted pick and place machines have an accuracy of ± 0.008" even though they quote ± 0.002". The range of quoted accuracies is from ± 0.0002" to ± 0.005". Most of the better articulated arm robots are capable of meeting ± 0.002" accuracy but may be restricted to a certain area within the total range (per foot rms).

2.4.2.3 Repeatability

Repeatability is defined as being able to return to a taught position with little or no error. Most machines are capable of ± 0.002" with some as low as ± 0.0005". Often, the Z-axis has separate and sometimes finer repeatability specifications, depending upon the movement mechanism.

2.4.2.4 Flexibility

Multiple degree of freedom robots are distinguished from other types of automated equipment by use. The use of equipment directed to a single or limited use is called dedicated or

"hard" automation. For example, an automated, dedicated chip inserter may have a manipulator and may also be programmable, but its use is limited to specific component sizes or only placing components.

By contrast, robots are successfully installed in virtually every aspect of printed wiring board production; some units are even used for more than one fabrication step in the same facility. One example applies a silicone solder mask to PWB's on one shift, then the same robot routes soldered boards from their pallet on the next shift. The cost of the robot is justified by its use for two functions. Because robots may be used for different applications, they are considered to offer flexible automation. The user, rather than the equipment vendor, defines the tasks that the equipment performs.

2.4.2.5 Reliability

The equipment should have a quality/performance of 99 percent plus. Downtime should be 1 percent or less due to machine error. Another aspect of the equipment is a 90 percent quality/performance rating. No greater than 10 percent downtime should be due to machine failure, periodic maintenance, etc., combined.

2.4.2.6 Placement Pressure Control

When placing the SMD's in position, the pressure applied is important. Too high a pressure causes bridging, smearing, or movement of the solder paste. Too low a pressure may not ensure good contact between the component and the solder paste, resulting in skewed components. Care must be taken when placing chip devices to prevent cracking. The solder paste acts as an upward force on the ends of the leads as the vacuum tip acts as a ram in the center. Many auto placement systems can control the placement force, which is a function of the component size. See Table 2.4.2.6 for examples of Force Requirements. NOTE: These are guidelines to base process development parameters.

Table 2.4.2.6. Force as Function of I/O for Leadless Chip Carrier Placement

I/O Count	Force (Grams)
Up to 32	75
40–64	100
68–84	125
Over 84	150

Placement pressures for chip components and leaded devices should be determined to preclude damage.

2.5 Solder Reflow Methods and Process Definition

2.5.1 Wave Soldering Chip Components

Wave soldering may be considered if chip components are mounted on the bottom side of an interconnecting structure that consists of a mixture of surface mounted and through-board mounted components. Chip components should be positioned with the longest axis perpendicular to

the direction of the wave solder conveyor whenever possible. The land patterns shown in Figure 1.5.2.1-1 are recommended for reflow soldering and wave soldering applications. See Figure 1.5.5.1-2 for wave solder spacing recommendations and Section 2.5.1.3 for preheating requirements.

2.5.1.1 Single or Dual Wave

Single wave automatic soldering has been the mainstay in industry since its inception over 30 years ago. In that time, several variations have been made to the configuration of the wave to improve the quality and performance, the latest of these being a laminar flow wave. A laminar flow wave is basically a smooth low turbulence wave with the flow of solder primarily in the opposite direction of the PWB travel. This increases the "peelback" effect which helps to produce smoother fillets with less bridging and related defects. It is an excellent system for standard through-hole PWB soldering. One of the reasons for the wave solder's success in through-hole technology was the plated-through-hole itself. Flux, air, and flux vapors are pushed ahead of the solder and out the top, so the solder can fill the hole. There is very little disturbance of the laminar flow of the solder as the PWB passes over the wave.

With the advent of surface mounting technology, new problems arose. No longer was there only a thin short wire lead protruding through the PWB. Surface mounted devices were attached (glued) to the bottom surface of the PWB. Nonmetallic component bodies with metallic surfaces or leads protruding from the side, together with the footprint patterns, drastically disturbed the flow of solder in the laminar flow wave. Surface tension of the solder does not allow it to flow easily into sharp corners between nonmetallic, nonwetting surfaces on its own accord. This is the reason for the "shadow effect"; flux and air entrapment worsen the problems.

The solution to the problem has been the concept of using two solder waves; one turbulent to force solder into the problem areas and a second laminar flow wave to smooth out the large masses of solder. The second wave is necessary because the turbulent wave leaves solder in places where its presence is harmful or the fillet quality is poor.

There are a number of systems available to perform surface mount wave soldering. Most use the same concept in dual wave technology. One new addition to the product line is the use of a single laminar wave with transducers producing a turbulence at the entry portion of the wave, claimed to have the same effect as the separate turbulent wave of the other systems. The vibrations force the solder into the critical spots of SMD's as well as enhancing the flow-through of conventional plated-through-holes.

2.5.1.2 Fluxing Method

Fluxing of the PWB with SMD's in place is primarily the same as conventional through-hole technology processing. Various methods include spray, wave, dip, and the most standard, foam fluxing. In foam fluxing, flux is placed in a container housing an aerator stone, a chimney and brushes to maintain the head of foam at a given height. An air knife or brush wipes off any excess flux.

One consideration to keep in mind is the flux formulation. Through-hole technology often requires a high solids content to ensure adequate coverage and activation. Using a high solids content flux for SMD's can increase the change for solder skips. A low solids flux reduces the change of skips but increases the chance of bridging. The addition of organic activators reduces the bridging problem but doesn't meet MIL-STD's for fluxes. Working closely with a flux manufacturer would be required to obtain the correct formulation. It should also be compatible with through-hole PWB's or mixed technology as required.

2.5.1.3 Preheating

Preheating methods are identical to those of conventional through-hole soldering. The most common types of preheaters include CAL-ROD heaters, infrared bulbs, infrared beds, and heated air. Since most PWB's are still a mix of through-hole and surface mount technologies, the same considerations for board temperature apply. A top side temperature of 180–220 °F is generally recommended with some exceptions (see Paragraph 2.5.1.4). In addition, the components must be prepared (preheated) for their subsequent submersion in molten solder. This reduces the amount of thermal shock and substrate warpage. Components must be preheated to within 100 °C of the soldering temperature at a rate no greater than 2 °C/sec.

2.5.1.4 Time/Temperature Profile

The time/temp profile is probably the most important aspect of wave soldering any type of component. One must have the correct amount of flux, flux activation, top side heat, and time in the wave to obtain optimum solder joints. The major concern of the time/temp profile for surface mount applications is that the top side board temperature does not get too hot in that it reflows and possibly disturbs SMD's that have been previously attached through reflow soldering. Actual time/temp profiling will depend upon nature of design of the substrate and the composition of the flux, and the number of chip components that may be on the bottom side.

2.5.1.5 Air Knife

Air knife technology has been in existence for approximately 10 years. It was first developed to improve the fillet shape, remove solder bridging, and expose nonwettable surface. A hot wind load of about 380 °C at 365 ft/s and 55 SCFM is applied to the underside of the PWB as it exits the solder wave. The solder joints are still molten and the hot air shapes them by removing excess solder. Any bridges and shorts are blown off and any nonwetted surface will be exposed because the solder wetting force is not strong enough to adhere. The solder maintains a strong adherence to wettable surfaces and thus maintains an exceptable solder joint.

This technology has since been incorporated into surface mounting components on the wave solder machine. It serves the same purpose of shaping the fillet and removing bridges. It is also being used (by the same vendor) to aid in reflow of top side fillets in conjunction with I/R lamps.

2.5.1.6 Adhesive Requirements

Adhesives are not new to electronic assembly. They have been used in many areas of assembly for encapsulation, potting, and bonding. The newest use of adhesives is in surface

mounting of components. Unlike through-hole devices which can be clinched to a PWB prior to wave soldering, SMD's cannot. In most cases, the adhesive is only necessary to form a bond until wave soldering can take place. The adhesive must hold the device in the correct orientation upon placement, maintain it during the physical handling before final assembly, and withstand the adverse environments of fluxing plus the high temperatures of the solder wave.

Physical Characteristics Desired:

- Stable one-part system
- Long shelf-life
- Good void filling capability
- Good drop profile (thixotropic)
- Electrically nonconductive
- Noncorrosive
- Sufficient pre-cure tackiness
- Adequate post-cure bond
- Chemically stable
- Distinctive color (aids inspection)

Process Considerations:

- Application Method—pin-transfer, pressure syringe, or screen printing
- Short cure time with low energy cure
- Resistant to high temperatures (wave soldering)
- Repair possibilities—removal of component after cure

Environmental Conditions:

- Nonflammable
- Nontoxic
- Odorless
- Nonvolatile

Types of Adhesive Systems:

- Thermosetting—cured by chemical reaction, cannot be resoftened (epoxy, acrylic, polyester)
- Thermoplastic—no chemical change, can be resoftened repeatedly (nylon, EVA copolymer)
- Elastomeric Adhesives—thermoplastics subset (rubber, silicone, neoprene)
- Toughened Alloy Adhesives—blend of rubbers and resins (epoxy-nylon, phenolic-neoprene)

Curing:

- Heat/time; conventional or IR oven
- Catalytic action
- Ultraviolet (UV) radiation
- Anaerobic—the absence of oxygen

2.5.2 Hot Belt Reflow

Hot belt reflow is perhaps the oldest form of surface mount reflow, primarily used in early hybrid development and still popular today. This method simply passes a special belt material across stationary heating elements. The assembly to be reflowed is placed on the belt and allowed to pass over the hot plates at a predetermined rate. This method provides a simple, efficient reflow process for hybrids, small volume, and development surface mount assemblies. When using hot belt reflow, it is recommended to first, precondition the assembly to drive off any flux volatiles and to preheat the parts and substrate to preclude thermal shock as it crosses the heated surface.

2.5.3 Infrared and Infrared/Convection Reflow

Infrared or IR reflow is a very popular method of reflowing surface mount assemblies. This is also one of the areas of controversy among process engineers as to the proper reflow technique (versus Vapor Phase). IR reflow provides heat to the assembly with the use of infrared lamps along a tunnel. The assemblies pass under the lamps on a conveyor and are gradually heated as they enter each heating zone until the temperature is such that the solder reflows. Because different materials on the assembly have different IR heat absorption properties, as well as the fact that shadowing affects some IR light, the heating is not uniform across an assembly. For this reason, hot and cold spots occur along the board, sometimes affecting the solder joint quality, sometimes damaging the board or components. With a properly profiled oven, these problems can be reduced. This requires extensive process development and profiles for each and every assembly type, no matter how similar. This is okay when large quantities of one assembly type are being produced (i.e., commercial applications), however, when a high mix of different assemblies is being run, process changes can dramatically slow production. These problems have been addressed by many IR oven manufacturers and have been reduced by the combination of direct and diffuse infrared heating elements. A more recent development is the addition of convection heating to the IR oven to help obtain a more even temperature distribution across the assembly.

2.5.3.1 Time/Temperature Profile

The time temperature profile for an IR oven must ensure that:

1. The assembly does not experience thermal shock
2. The solder paste is sufficiently dried out
3. The time at reflow is sufficient to ensure 100 percent reflow of all the solder paste and proper wetting to the terminations
4. The rate of reflow is such that shifting of parts and tombstoning does not occur.

Each individual oven is different and the particular profile will be unique; however, a general profile for proper IR reflow can be seen in Figure 2.5.3.1.

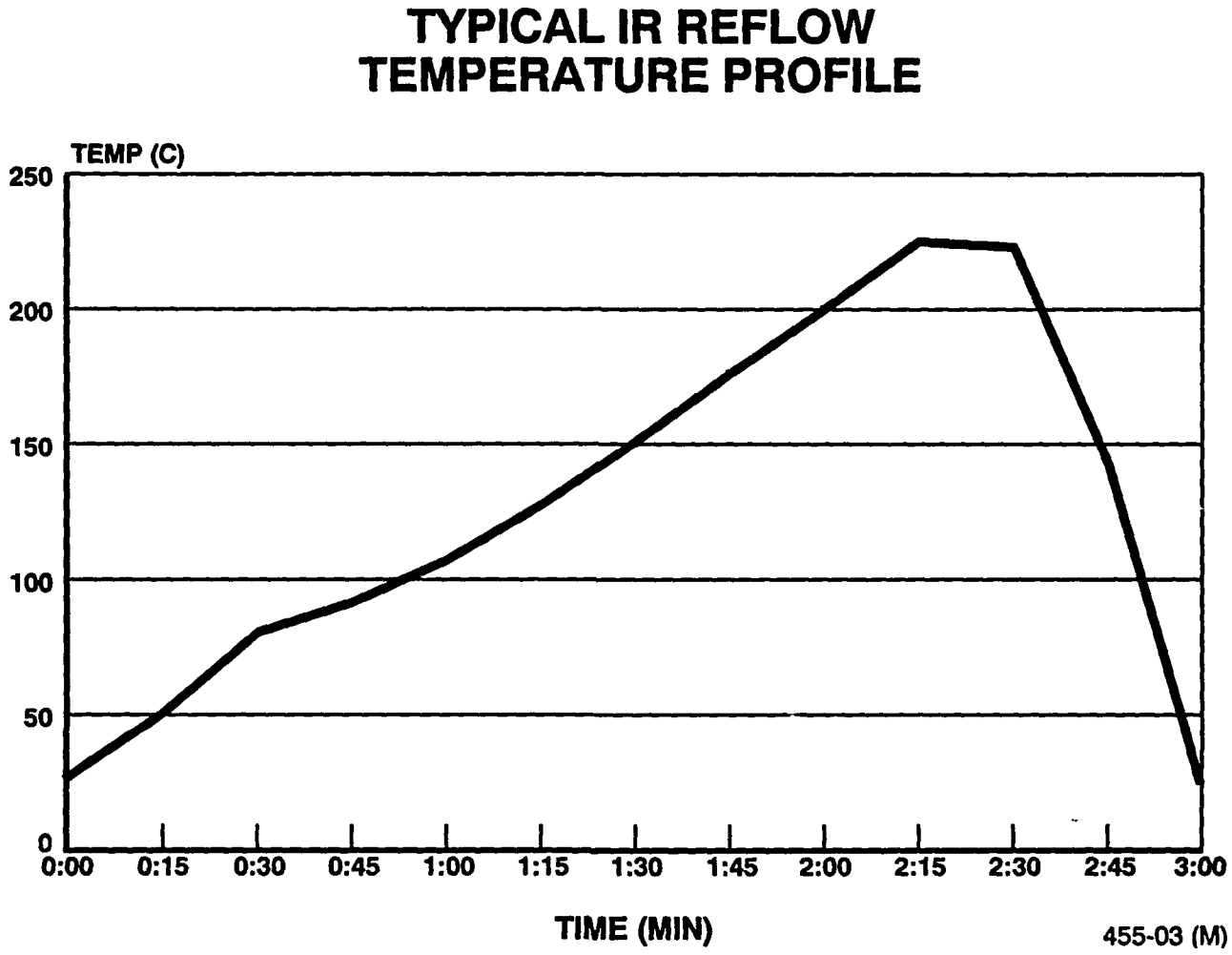


Figure 2.5.3.1.

2.5.4 Vapor Phase

Vapor phase reflow soldering is done by heating a liquid fluorocarbon compound to its boiling point (usually 215 °C) and immersing the substrate in the hot vapors. The vapors condense and transfer heat to the board through the principle of latent heat of condensation. Since the liquid boils at a temperature higher than the solder paste melting point, the solder melts and fuses to the component lead and pads. The controlled temperature of the liquid ensures even heating over the entire PWB/substrate (see Figure 2.5.4).

2.5.4.1 Time/Temperature Profile

The time/temperature profile is also very important in vapor phase soldering as it is in IR reflow. Defects may occur (i.e., solder balls/splatter, insufficient reflow, tombstoning, etc.,) from an improper profile. Also, many batch and in-line vapor phase machines do not have a preheat zone to

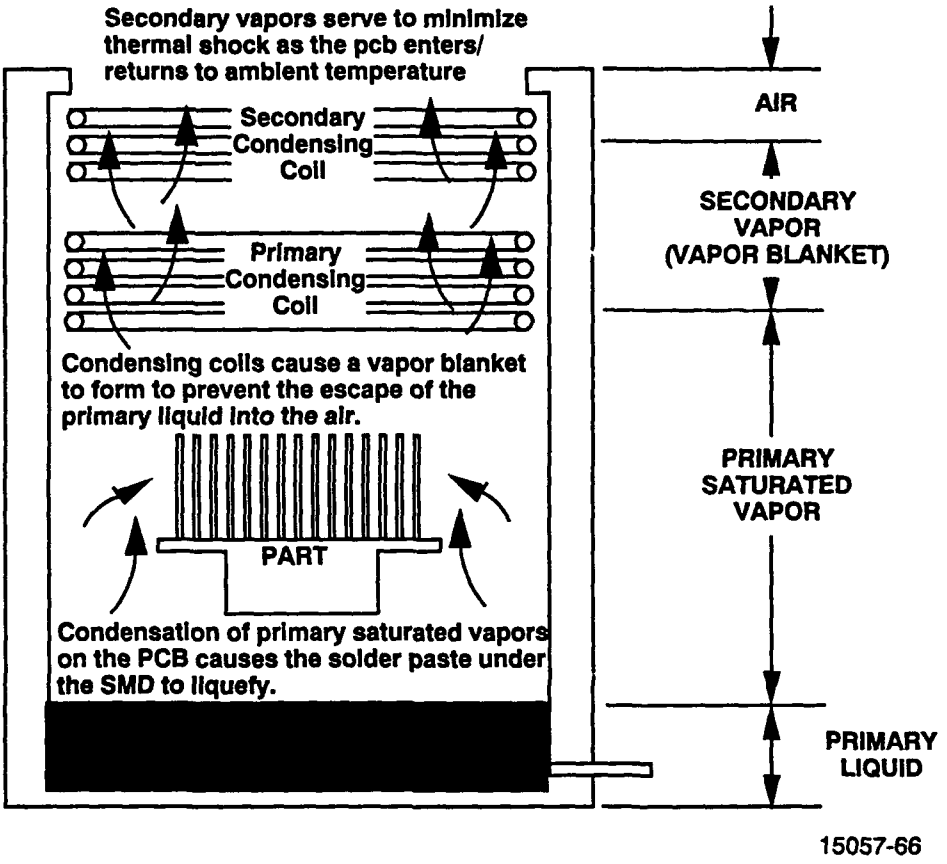


Figure 2.5.4. Vapor Phase Reflow Soldering System

precondition the assembly prior to entering the vapor zone. This was once an area of concern because peope were not preconditioning their boards prior to reflow, causing extensive defects. Proper processes use a preconditioning oven to drive off the flux volatiles and preheat the board and components to preclude thermal shock. Some vapor phase machines now include an IR preheat stage before the vapor zone to ensure a proper preconditioning stage. A typical vapor phase reflow profile is shown in Figure 2.5.4.1.

2.5.5 Components on Both Sides of PWB

There are basically three classifications of surface mount PWB's; Type I, II, and III. Each of these substrate types has the capability of having components mounted on both sides. Type I would have 100 percent SMD's mounted on one or both sides; Type II would have SMD's and through-hole devices on the top side with (usually) small SMD's on the bottom side; Type III substrates would have strictly through-hole components top side with smaller SM devices (chip caps, resistors) on the bottom. There are a number of techniques possible for attaching SMD's to both sides of a substrate, most commonly wave solder and two step reflow.

2.5.5.1 Adhesive/Wave Soldering

To wave solder a PWB, with SMD's on the bottom, it is necessary to first attach the components with an adhesive (see Paragraph 2.5.1.6). This is simply to keep the components in

TYPICAL VAPOR PHASE REFLOW TEMPERATURE PROFILE

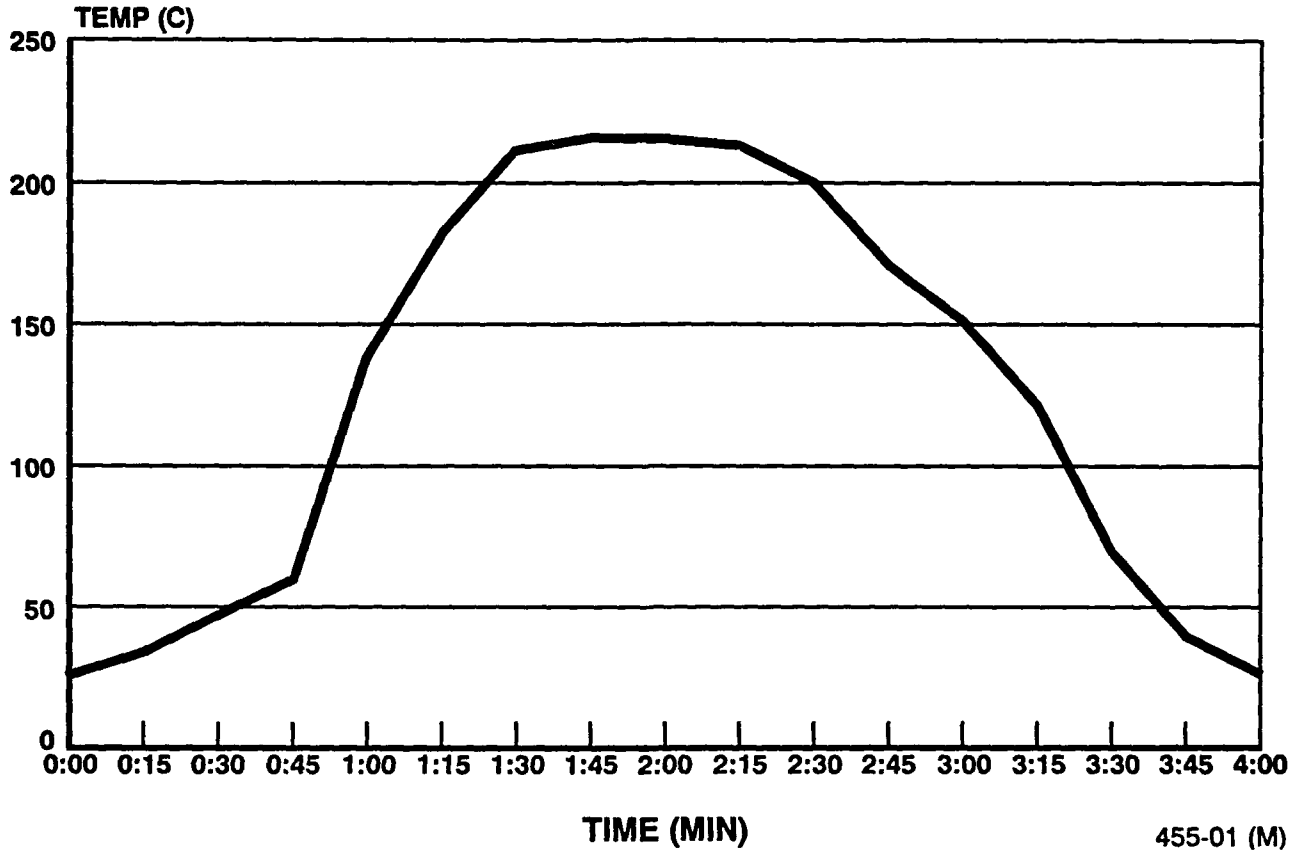


Figure 2.5.4.1.

position. Component orientation is the most critical aspect of wave soldering SMD's. The components must be situated in a manner which will not cause the solder to miss the component lead in any way. Shadowing and skip soldering are the most common defects associated with component orientation. Other considerations for component orientation are excess solder, bridging, and general fillet shape. See Figure 1.5.5.1-2 for recommended component orientation and clearance.

2.5.5.2 Two Temperature Soldering

Two temperature soldering is a simple operation for reflow soldering SMD's on both sides of a substrate. The first side of the substrate is populated using a solder with a higher melting point than that of the solder to be used on the opposite side.

The opposite side is populated and reflowed using the lower temperature solder. This allows the first side to be suspended upside down during the reflow cycle without concern of the components falling off. It also prevents reflow of the first solder joints, possibly causing defects. Another use of high/low temp soldering is for any special heat sensitive components which couldn't withstand the normal reflow temperatures. Reflow methods would be IR, vapor phase, and/or

convection. Specific solder paste alloy depends upon reflow temperatures available (vapor phase fluid restrictive) or desired difference in reflow temperatures. The primary restriction in using this method is the requirement to use two different vapor phase fluids. A single temperature two step reflow can be utilized when the components that would be suspended upside down are relatively small (chip caps/resistors). Surface tension and/or of the solder adhesive would hold them on.

2.5.5.3 One Temperature Double-Sided Soldering

To solder two sides in one operation, the first (bottom) side must be assembled using an adhesive. Once the adhesive has cured, the second (top) side of the board may be assembled and the entire assembly then reflowed at one time. The adhesive will prevent bottom components from falling off. A special fixture must be used to stand the PWB off the surface to prevent damage or movement of the components. This process is very difficult to perform due to solder paste deposition, solder paste curing concerns and difficulty in handling. Two-step soldering or soldering chips with the wave would be the recommendation for a single board assembly. Two boards laminated to a core or heatsink should be processed separately, prior to lamination/bonding whenever possible.

2.6 Repair Methods

There are a number of repair methods available for surface mounted devices depending on the type of component. Some repairs can be made with a conventional soldering iron while some require the use of a special hot gas (air/nitrogen) instrument to reflow all of the solder joints at one time on a given component and use a suction cup device to lift the component off the PWB. This process can be reversed to install a new component.

For removing components which have been placed with adhesives, repair is considerably more difficult. This problem must be faced during the selection of the adhesive. There are adhesives called sycroagalates which are torque breakable adhesives which ease repair. Standard repair procedure must be generated for particular types of repair requiring more than common soldering skills.

2.7 Cleaning Process Selection

The cleaning processes are as varied as the soldering processes available for surface mount assembly. Cleaning systems may be bath, batch or in-line, utilizing either water-based or solvent-based cleaners. The selection of a cleaning system depends upon the application, the contaminates to be removed and the volume of production. For small prototype runs, multiple immersion bath cleaning with manual scrubbing and agitation may be employed. Bath cleaners are not recommended for larger volumes or production due to the problem with contamination level control and throughput. Batch degreasers are popular for low volume production because they are efficient and take up little space. Large volume production usually requires some type of in-line cleaner.

Cleaning materials are also very important to the cleaning process selection. What was once the most common cleaning medium in electronic fabrication, CFC 113, (Freon TF and

similar chlorofluorocarbon (CFC) based solvents, is being phased out and eliminated from use. This is required by the Montreal Protocol which requires the eventual ban on ozone depleting chemicals in industry. A popular alternative to Freon is 1,1,1 Trichloroethane. It has only a fraction of the ozone depletion capabilities as Freon, but is now also on the Montreal Protocol list of chemicals to be banned. This has lead industry to aggressively investigate and develop alternative cleaning solvents for electronic and general industry use. HCFC's (hydrochlorofluorocarbons) have been developed by a number of chemical companies as an alternative to Freon and Trichloroethane and are being accepted as an interim alternative. As they still cause some ozone damage, they too must eventually be phased out, but are seen as an acceptable interim alternative until a total solution can be found. Another medium for electronic cleaning is the use of terpenes. Terpenes are solvents made from the rinds of citrus fruit. These are biodegradable and provide excellent cleaning. However, terpenes are highly volatile and require special cleaning machines equipped with self-contained fire extinguishing equipment. Too, solvent disposal becomes another concern based on treated water disposal regulations.

One solution, which many companies have been using for years, is water. Various cleansers, surficants, and saponifiers have been developed and used over the years to successfully remove flux residues from printed wiring boards. New machines have been developed to tackle the problems associated with cleaning under surface mounted parts, i.e., high pressure impingement sprays and specially angled nozzles. The only concern associated with water cleaning is the disposal issue. The water must be specially treated and handled before it may be dumped into the drain, if that is even permitted at all. The availability of water is also an issue in many areas. In these days of unpredictable drought and availability when even drinking water must be carefully preserved, it is not wise to choose a cleaning method which consumes so much of a precious commodity. Recycling of the water in a closed system may be an answer.

Another alternative to the cleaning issue is noncleaning. This is accomplished by using specially designed fluxes whose residue, if any exists, does not have to be removed from the assembly. They are designed such that the residue is eliminated by the reflow process and requires no further cleaning. This issue is still under contention with the DOD and not likely to be an alternative in high reliability assemblies in the near future. However, as cleaning options decrease, it may yet become an option.

2.7.1 Activity Level Required

The activity level of the cleaning medium must be such that it readily removes any remaining ionic or nonionic contaminants from the reflow process while causing no damage to the PWB or components thereon. The activity level of solvents can be monitored for acid levels, ph, and excessive contamination content. Physical activity of the medium must be such that solvent penetrates under closely spaced components (LCC's, chips, etc.) and removes trapped residues. Surface tension of many liquids prevents this penetration and must be assisted by high pressure sprays. This is also the reason for the minimum spacing requirements found in the components mounting specifications. The use of ultrasonic and subsonic agitation in the cleaning tank can promote additional cleaning, but must be controlled to prevent damage to delicate components.

Government agency investigation (EMPF, China Lake, CA) into ultrasonic cleaning has not yet made this an approved process for cleaning military electronic assemblies.

2.7.2 Susceptibility of Components to Damage by Cleaning Method

Surface mount components meeting military requirements are typically ceramic based. Active components use metal lids welded or soldered in place for hermeticity. In most instances, these components are not readily susceptible to damage during cleaning. They are usually more susceptible to damage during handling (shock and ESD).

2.7.3 Cleanliness Testing

Cleanliness testing is performed on assemblies prior to conformal coating or encapsulation to ensure that detrimental ionic contaminants have been removed. Most of the available machines on the market use a mixture of isopropyl alcohol and deionized water (75 percent/25 percent, respectively) to dissolve any remaining residue and measures the conductivity of the solution. This is then correlated to resistivity over the given surface area under test. This resistivity is converted to mg NaCl/in^2 and compared to the appropriate pass/fail limits set forth for that particular machine (Reference MIL-P-28809).

The difficulty to clean under SMD's also makes it difficult to detect contamination remaining under these devices. For this reason, test equipment manufacturers are equipping their machines with special jets or nozzles to penetrate the close spaced devices and detect all (or most) of the contamination.

Another issue which arises, due to the CFC concern, is the use of nonrosin-based fluxes. Water-based or synthetic fluxes do not have the ionic residues detectable by a typical cleanliness tester. In this case, another set of test criteria would be necessary to ensure that these nonrosin type residues are adequately removed. To date, there is no known system available.

The cleaning process is one that requires sufficient contamination removal with no degradation to the assembly and is environmentally safe. It is not a simple selection and must be a decision based on both system, production, and environmental impact.

3.1 Inspection Criteria

The enclosed inspection criteria are based on the present status of the general requirements of MIL-STD-2000, Rev. A, with modifications or changes based on technical evaluations or reasoning, as noted. As that document has not been officially issued, to date, this information is subject to change in the future. However, this data is based on industry experts from across the nation and is deemed to be the best available for SMT. Without repeating the entire MIL-STD, only the major issues are presented. The numbers in parentheses correspond to the related paragraph of MIL-STD-2000A, dated 14 February 1991.

3.1.1 Inspection (5.3.7.4)

When visual inspection is used, it shall be performed using the magnifiction power specified herein.

Land Width	Inspection	Referee
70.5 mm (0.020 inch)	4X	10X
0.25–0.5 mm (0.010–0.020 inch)	10X	20X
<0.25 mm (0.010 inch)	20X	30X

3.1.2 Solder Coverage (4.20.5)

The solder quantity shall be sufficient to cover all elements of the connection.

3.1.3 Visual Characteristics of Acceptable Solder Connections

3.1.3.1 Wetting and Filleting (4.20.6)

1. Solder shall wet the surface of all connection elements and shall fillet between connection elements over the complete periphery of the connection. The solder shall have a positive contact angle between the surfaces being joined.

Note: There are exceptions based on part configuration (i.e., chip components do not require side fillets).

3.1.3.2 Finish (4.20.1)

1. The appearance of the solder joint surface shall be smooth, with a metallic luster.
2. Solder joints having a gray appearance are not acceptable, except:
   a. The solder connection is made with other than Sn60, Sn62 or Sn63 solder.
   b. The appearance is the result of a slow cooling rate (e.g., high assembly thermal mass after wave or vapor phase soldering).
   c. When one or more of the connection elements are gold or silver plated, or solid silver, the surface may appear slightly porous and gray.

3.1.4 Visual Characteristics of Unacceptable Solder Connections

3.1.4.1 Physical Attributes

1. Poor Wetting
   Nonwetting and dewetting shall be limited to no greater than 5 percent of the solder joint area.
   a. Nonwetting: a surface condition wherein the surface finish of the material is exposed. The surface finish has been in contact with molten solder, but due to contaminants, insufficient flux, oxidation, etc., the solder has failed to form an intermetallic bond (wet) with the material.
   b. Dewetting: a surface condition wherein no surface finish is exposed, but the solder covering the surface has receded into irregularly shaped mounds surrounded by a thin solder film.

2. Voids (4.20.4)
   Voids or blow holes in conjunction with the minimum allowable solder volume are unacceptable.

3. Fractured/Disturbed (4.20.3)
   The solder shall not show evidence of fractures or be disturbed.

   a. Fractured/disturbed: connection will appear frosty and granulated because of movement during solder solidification.

4. Peaks, Protrusions (4.20.2)
   Solder peaks and protrusions are unacceptable.

   a. Peaks, protrusions: an undesired projection from the surface of the solder connection, peaks may be caused by random process variations. Peaks, protrusions may reduce the separation between conductors below the acceptable minimum, may be a cause of arcing or shorting, and shall be cause for rejection.

5. Solder Bridging (4.20.2)
   Solder shall not appear as globules, strings or bridging between adjacent conductors.

6. Contaminated Solder (4.20.2)
   (4.20.2) The solder connection shall be free of contamination.

   a. Contamination: foreign matter inclusions (cotton fibers, dirt embedded in the solder surface, etc.).

7. Flux Residue (4.20.2)
   The solder connection shall be free of flux residue.

8. Solder Splatter
   Solder splatter in the form of solder balls and solder slivers is unacceptable.

   a. Solder splatter: solder balls or slivers clinging to the surface of the laminates or foil. Solder splatter may result in shorting or arcing.

9. Exposed Basis Metal (4.20.2)
   There should be no exposed basis metal in the solder connection, on the top surfaces of conductors and terminal areas of printed wiring or on surfaces of other parts, except when caused by trimming of the lead ends of leaded devices (prior to soldering).

10. Blow Holes (4.20.4)
    Blow holes are unacceptable when in conjunction with minimum allowable solder.

    a. Blow hole: a hole in the solder fillet, caused by gas escaping from within the solder and characterized by jagged, sharp edges around the hole.

11. Insufficient Solder – see specific part type

12. Excessive Solder – see specific part type

3.1.5 Components

3.1.5.1 Body and Seal Condition

1. The lead to body seals of mounted devices shall be undamaged. Body chipouts that extend to or into the glass seal and chipouts that expose a normally encased area of a lead are unacceptable (see Figure 3.1.5.1).
2. Hairline cracks in either the seal or the body are not acceptable.
3. Minor imperfections in the component body due to component manufacturing may be acceptable.
4. Minor cracking or chipping of the meniscus may be acceptable provided that the lead to body seal is undamaged.

3.1.6 Flat Packs

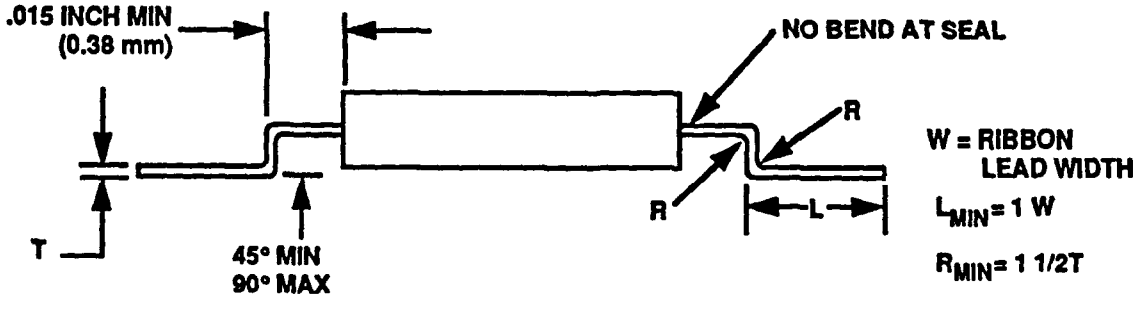
3.1.6.1 Body Seating (40.11.4.2)

New parallelism between the base surface of the component and the PWB shall be minimized.

1. Maximum spacing shall be 0.040 inch (1.0 mm).
2. In no instance shall nonparallelism between the base surface of the mounted component and the surface of the printed wiring board result in nonconformance to maximum spacing requirements.

3.1.6.2 Lead Configuration (4.23.7.1)

1. Leads of planar mounted flat packs shall be configured as shown, except the vertical portion of the lead should be approximately 90° ±5° for better compliance.



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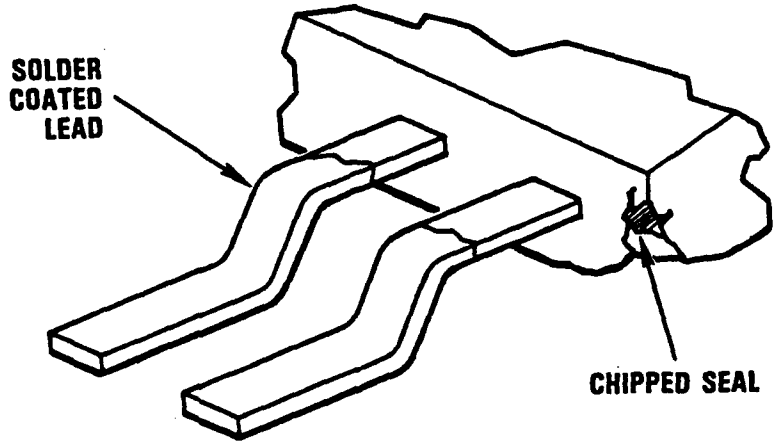

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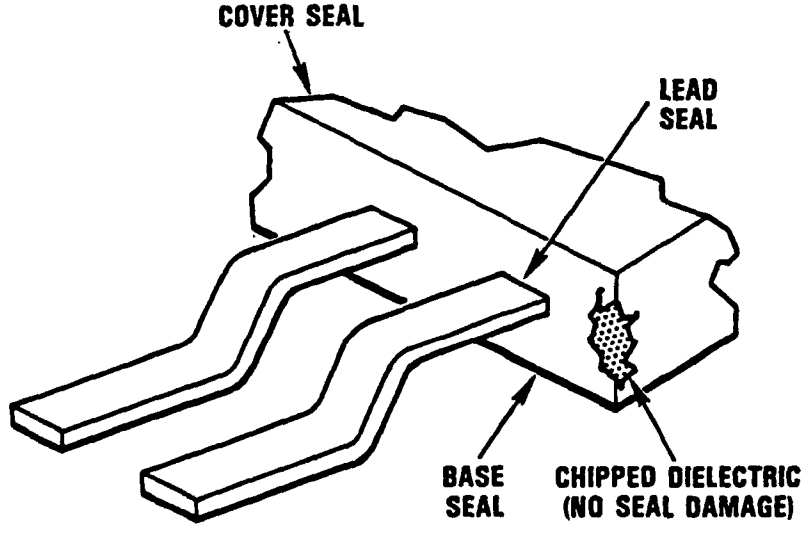

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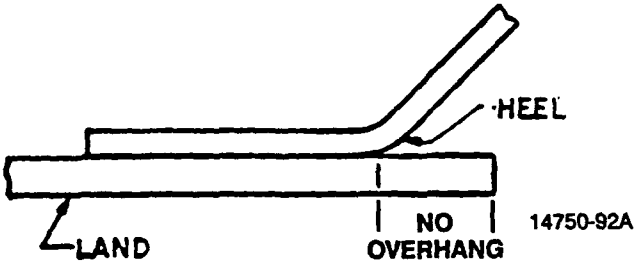
Figure 3.1.5.1.

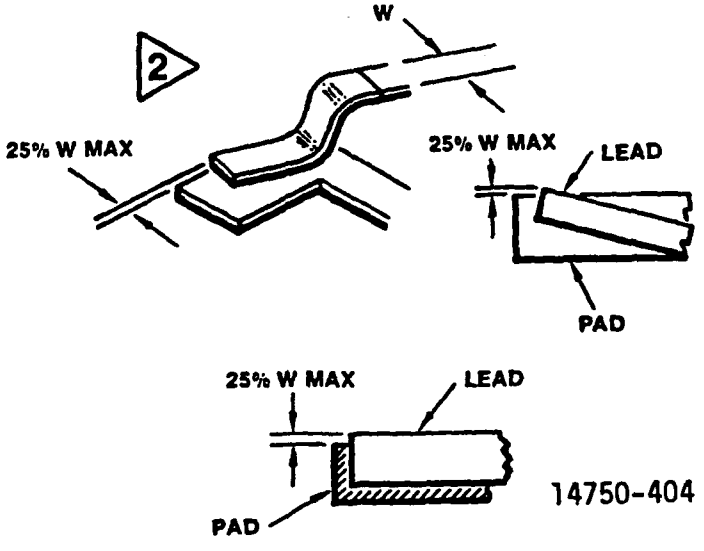
3.1.6.3 Lead Seating (4.23.7.2)

1. Leads shall be seated such that the heel to terminal area relationship will provide for a proper heel fillet (see Paragraph 3.1.6.4).



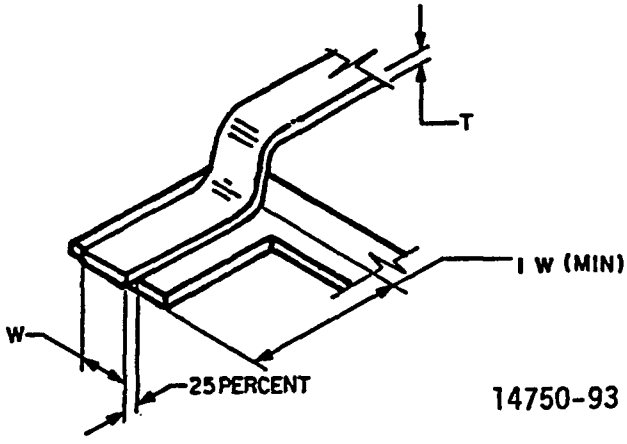
A. FLAT LEAD

2. Side overhang shall be a maximum of 25 percent of the lead width.



3. Toe overhang is acceptable provided that all of the following requirements are met.
   a. Length of lead contact shall be a minimum of 100 percent of the width.
   b. The overhang does not exceed 25 percent of the lead width.

c. Minimum spacing between conductors shall be met.



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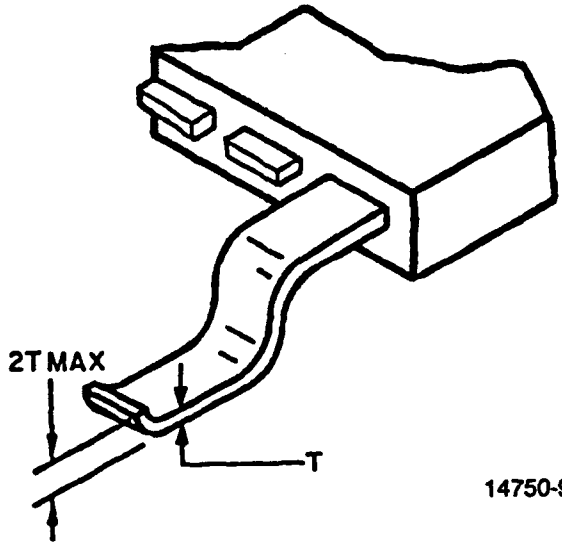
4. Toe curl shall not exceed twice the lead thickness (2T).



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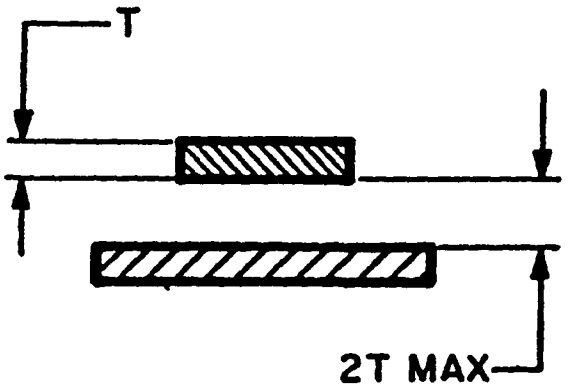
5. Separation between the lead foot and the surface of terminal area shall not exceed twice the lead thickness (2T). (4.16.20)
6. Foot twist shall not result in nonconformance with the 2T maximum spacing requirement.



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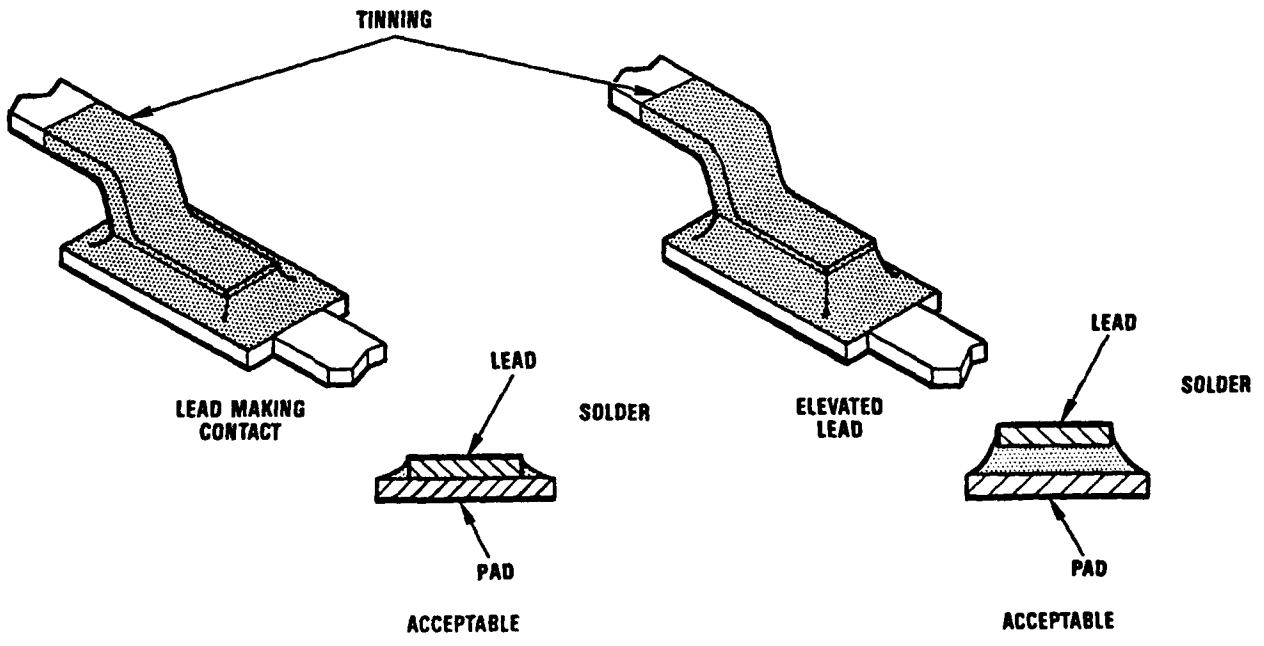
3.1.6.4 Solder Coverage (4.23.7.4, 4.23.7.5)

1. Ribbon leads shall exhibit a visible fillet rising from the pad a minimum of 50% up the side of the lead. The outline of the lead must be discernible in the solder. A thin solder coating due to lead tinning may extend past the upper bend radius to within 0.005 inch of the component body.



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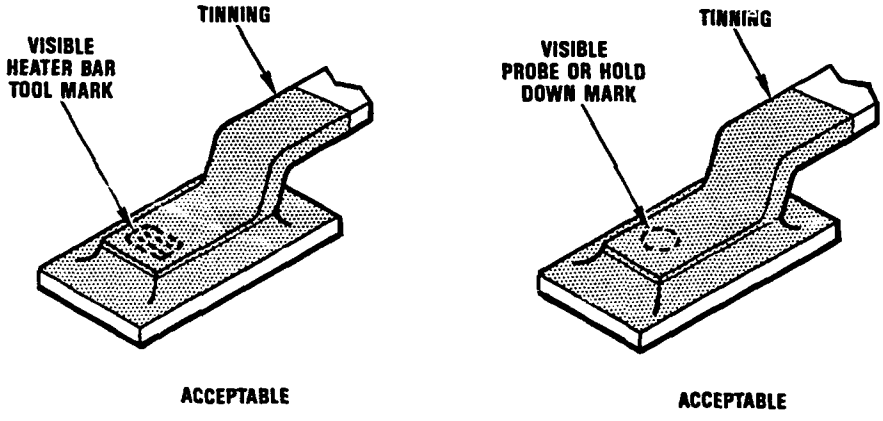
2. Tool marks shall not be cause for rejection. (4.24.12)



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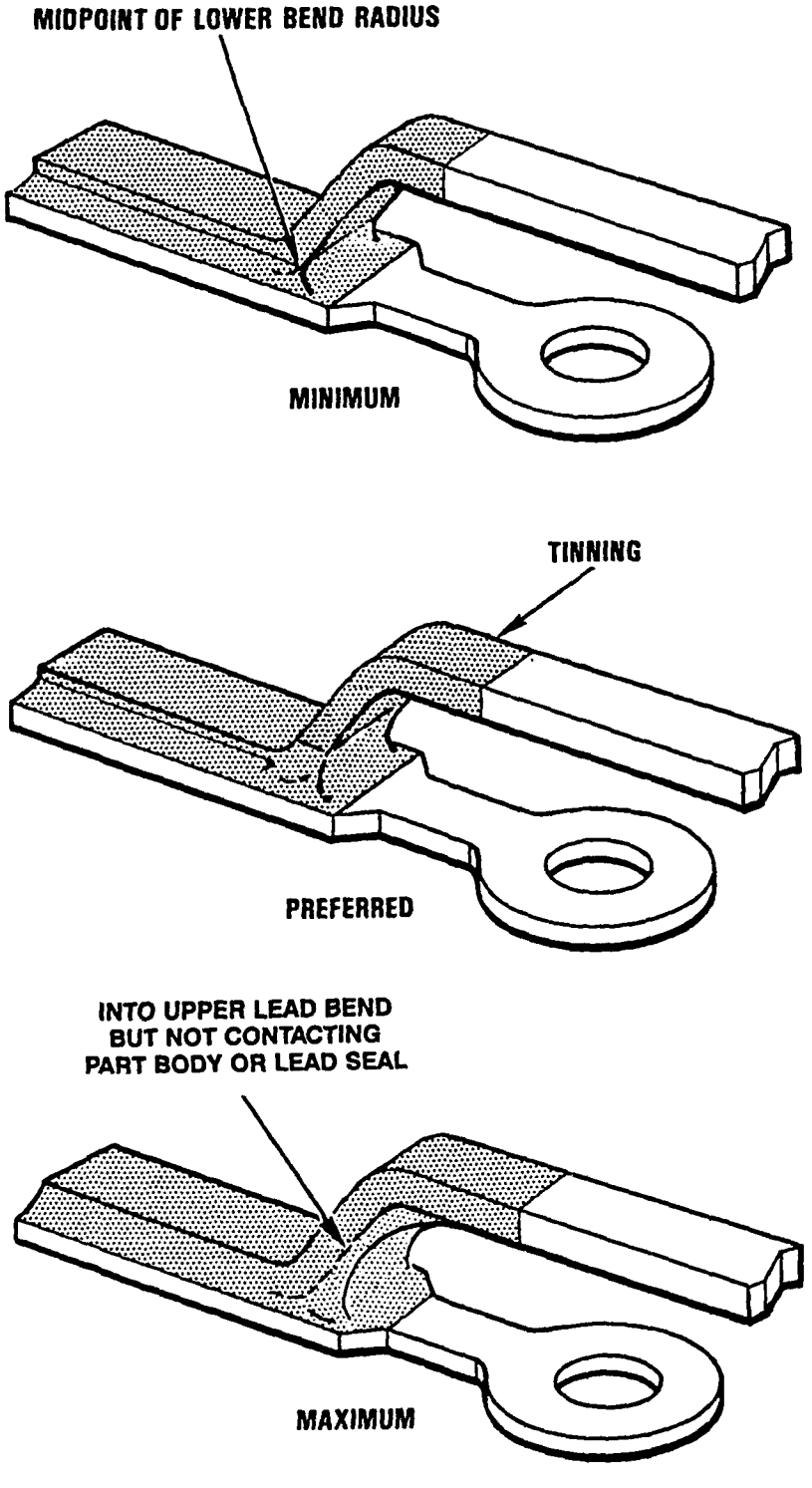
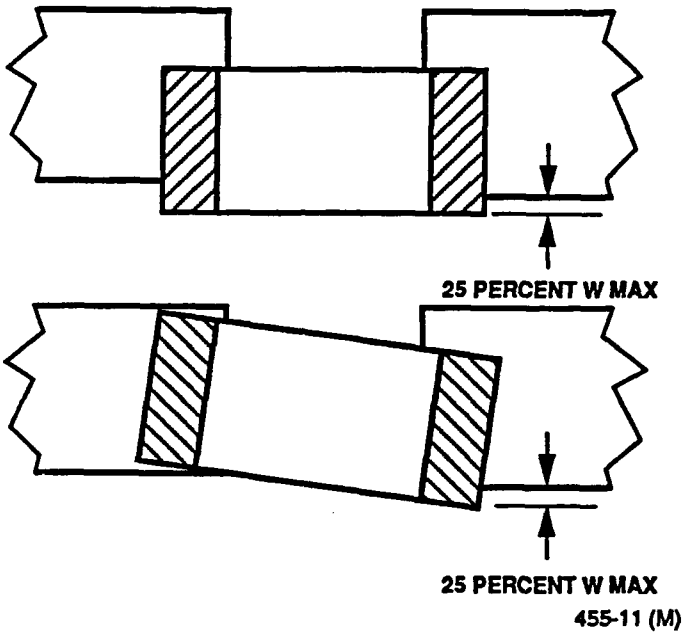
3. As a minimum, the heel fillet shall extend below the midpoint of the lower bend radius.
4. As a maximum, the solder fillet may extend into the upper bend radius, but shall not contact the part body or lead seal.



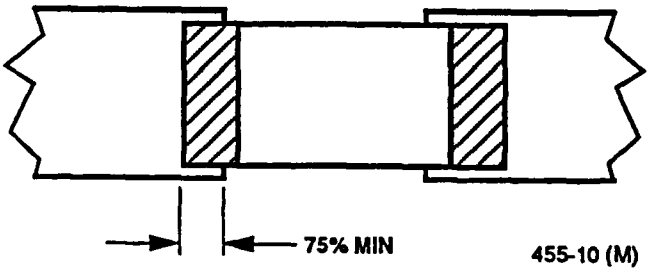
3.1.6.5 Chip Devices (4.23.3)

3.1.6.5.1 Component Positioning

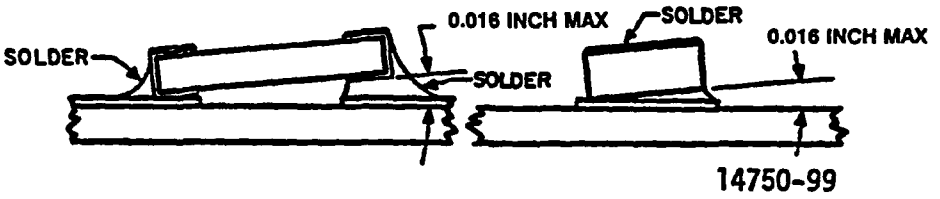
1. Chip devices shall not be stacked or bridge spacing between other parts or components such as terminals or other chip devices. (4.23.3.1)
2. The chip device shall be positioned such that it will not overhang the terminal area more than 25 percent of the device width (w). Minimum conductor spacing shall be maintained. (4.23.3.2)



3. The end cap of the chip device shall extend onto the terminal area a minimum of 75 percent. (4.23.3.2)



4. The space between the body of the soldered-in-place chip device and the terminal areas shall be selected in conjunction with the cleaning jprocess such that contaminants donot remain under the part after cleaning. (4.23.6)
5. The chip device shall be mounted flat and parallel with the surface of the printed wiring board such that the difference between the thickness of the solder under each end is less than 0.016 inch (0.04 mm). (4.23.6)

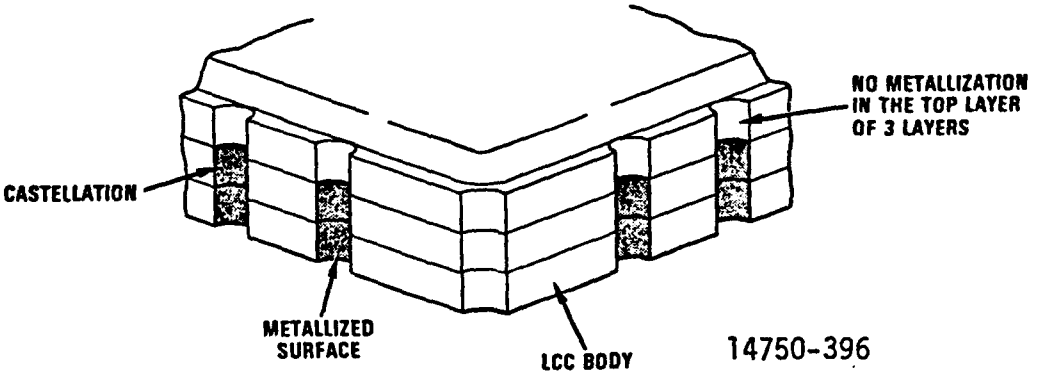


6. Solder shall extend up the end termination a minimum of 0.25 T (0.50 T optimum). (4.23.3.2)
7. Solder may be present on the top of the end cap, provided the end cap is not fully encapsulated. (4.23.3.2)

3.1.6.6 Leadless Chip Carrier, LCC

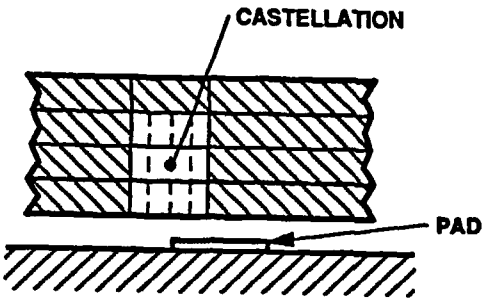
3.1.6.6.1 Castellation

1. Recessed metalized portion of LCC where the connection between the LCC socket lead and the LCC is made.

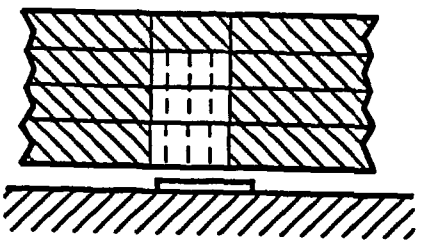


3.1.6.6.2 Visual Inspection Criteria

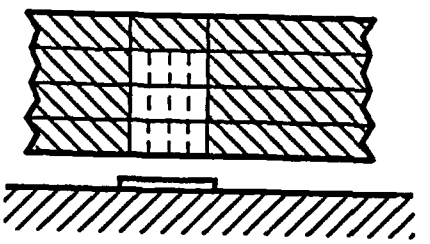
1. Misalignment of LCC to PWB shall not exceed ¾ of the pad width. (4.23.5)



LESS THAN 3/4 OVER PAD
UNACCEPTABLE



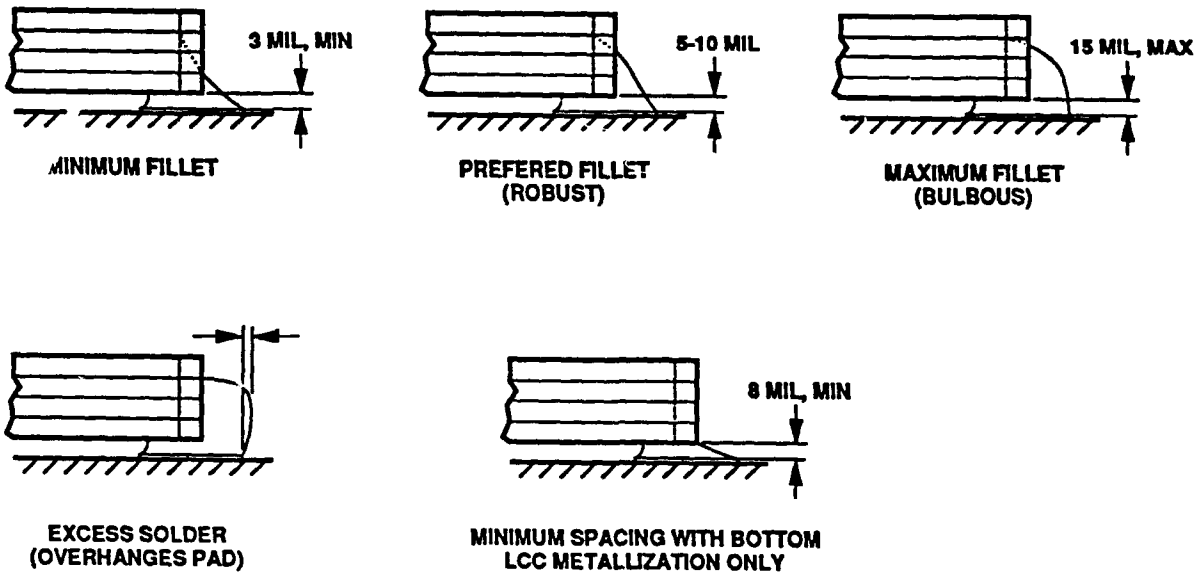
3/4 OVER PAD, MIN
ACCEPTABLE



PREFERRED

455-02 (M)

2. Solder coverage. Presently, the MIL-STD-2000, Rev. A, conflicts with extensive government-funded industry data on the volume and shape of solder fillets for LCC's. A bulbous fillet may be preferred in some cases while a minimum fillet may be unacceptable due to the environment. The following criteria is recommended for general LCC fillet configurations.



3.2 Inspection Methods and Equipment

3.2.1 Inspection of SMD's

Surface mounted devices are a relatively recent development in miniaturization of electronic components. Reducing size gives the advantage of higher functional density in a smaller space but, there are also inherent disadvantages associated with this packaging technology. Closer contact spacings, complex device packages, and many contacts under the devices themselves, make inspection of surface mounted devices most challenging.

In order to truly understand the impact that surface mount technology (SMT) is having, it is important to analyze the differences between this technology and plated through-hole (PTH) technology.

3.2.1.1 Plated Through-Hole (PTH)

With PTH technology, the main physical strength and the mechanical compliance (flexibility, stress relief, or ability to handle dimensional changes from thermal expansion) result from the component lead going through the printed wiring board (PWB). When the lead is not bent between the PWB and component body, the body needs to be separated from the board by a gap to compensate for expansion. If the lead is clinched on the solder side, the connection has even more strength. This is a conservative design with a large inherent safety factor. Therefore, moderate

deviations from the ideal solder fillet (attributes and configuration) are acceptable and may be detected by use of conventional visual inspection techniques.

3.2.1.2 Leaded Surface Mount

For leaded surface mounted components such as flat packs, the solder provides mechanical strength and electrical integrity, but the lead provides mechanical compliance. (Strength may also be provided by adhesives used.) This geometry is very reliable because solder, weak as it is, is strong enough when a proper heel fillet is achieved and stress relief is provided. Voids and insufficient solder are not as tolerable as in a through-hole connection, but available evidence suggests that leaded surface-mount printed wiring assemblies (PWA's) with normal amounts of voids (less than 25 percent volume) from the use of solder paste, have proven to be reliable. However, the location of these voids may be critical if situated in the heel fillet. Another problem is residual tension in the solder if the foot is not allowed to rise while the solder is solidifying. Solder in tension creeps readily and can result in creep rupture (lifted lead). Neither voids or solder in tension are detectable by visual inspection. Photothermal radiometry and x-ray fluoroscopy can detect voids, but no inspection technologies at this time can identify solder in tension. Of course, neither of these anomalies (voids or solder in tension) need occur if the process is designed and controlled to prevent them.

3.2.1.3 Leadless Surface Mount Devices

With leadless chip carriers (LCC's) and chip devices, the solder provides strength and mechanical compliance. Use of an adhesive mount may provide strength, but will also add strain during thermal cycling. The reliability of the solder connection depends not only on the metallurgical qualities of the connection itself, but on thermal expansion characteristics (CTE mismatch) of the PWB and component, uniformity of all solder connections to the component and height of the solder fillet or column. In general, the larger the component, the smaller the safety factor there is for the solder connection which places more importance on metallurgical perfection. Above a certain size, perhaps 44 I/O for a 50-mil pitch LCC, the safety factor (defined in terms of number of thermal cycles) becomes fractional, so that even a package with every connection uniform and structurally perfect is unreliable.

A leadless solder connection cannot be inspected for perfection visually, but a subjective (qualitative) judgement can be made for a deviation that exceeds some limit. Established limits should make the inspection practical; that is, it can't take too long or reject the normal variations associated with a well controlled process since no improvement would be possible. The limitations for visual inspection are:

- Qualitative rather than quantitative
- Relies upon external appearance to determine internal structural integrity (no void detection)
- A large portion of the solder connection is fully or partially hidden under the package

An inspection technique that could detect voids, produce quantifiable data, and inspect underneath the package would be ideal. An inspection system with these capabilities would allow inspection for a smaller deviation which would help to ensure reliability.

3.2.2 Inspection Systems

The current movement in government and the defense electronics industry is a shift from mandating process in MIL-Specs, to specifying product performance and reliability by finding which solder anomalies actually correlate with failures in environmental stress screening (thermal cycling), and eliminating any reference to the rest. These changes will make it easier for a company to embrace automated inspection, but with the so-called "cosmetic" defects eliminated, visual inspection will also be made easier.

The main obstacle to overcome for most defense electronics companies, when transitioning from visual to automated inspection, is the software cost associated with low volume, high mix production. Many of the automated systems that are available today can be dedicated, cost effectively, to a single program with high volume production. Some breakthroughs in application of existing technologies have been made recently, e.g., 3-D x-ray and contour mapping, which may help to solve the recurring cost problem associated with automated inspection.

3.2.2.1 Automated Inspection

The leading approaches to automated inspection are:

Photothermal Radiometry. In this method, patented by Vanzetti Systems Inc., the temperature change of a solder connection is monitored with a chilled infrared detector while (and after) the connection is heated by a yag laser. To oversimplify, connections which get much hotter than the rest are taken to be defective as heat dissipation is reduced due to physical or metallurgical reasons.

X-Ray Fluoroscopy Plus Vision. In this method, the shadow pattern created on a fluorescent screen by x-rays passing through a PWA is analyzed by a machine vision system (TU camera plus image-processing computer), which is able to correlate gray levels with solder thickness. The shape of the fillet (and any voids) is measured, and algorithms are used to identify the nature of each anomaly found. X-ray is the only method capable of inspection underneath LCC's, J-lead packages, and pin grid arrays. Three companies which are leading the way in x-ray plus vision: Four Pi, IRT, and Nicolet.

Diffuse Lighting Plus Vision. Totally diffuse lighting is necessary to prevent bright spots on the solder image, which because of camera limits cause loss of detail. The success of this approach has been demonstrated by consolidated controls. Other vision system companies are now reported to be working on this approach.

Reflectometry. In this approach, a computer calculates the surface topography from the reflection pattern produced by structured light (stripe or moving spot). There are two companies working along these lines: Robotic Vision Systems, Inc. and Photonic Automation Inc.

3.2.2.2 Visual Inspection

Stereo Microscope. Visual inspection may be accomplished using a stereo microscope which will allow the inspector to view the solder connections from different angles and a range of magnification power. This technique is the conventional method employed in most factories today that are assembling and soldering PWA's with PTH and leaded surface mount technologies. This method is less capital intensive, but there are disadvantages. Operator fatigue, operator judgement and the fact that visual inspection is limited to that which is external and not hidden from view are a few. These factors make inspection of leadless surface mount, J-lead, and pin grid arrays very limited or impossible to accomplish as much of the solder connection and surrounding area to be inspected are hidden under the device. Certain microscope attachments and techniques have recently been developed, e.g., image rotators, that give the inspector a 3-D view of the solder connections and an enhanced angle view of the hidden portion. This technique shows promise for leaded surface mount.

3.3 Component Qualifications

3.3.1 Qualifying of electronic components is required to ensure that the components selected for particular applications are suitable for the conditions and environment to which they will be subjected. The specifications for component qualification and selection are listed in Section 1.2, Specifications. In many instances, the government is not completely satisfied with all of the requirements or the lack of certain requirements as they are written to date. To compensate for the lag time in updating these specifications, the government is adding additional requirements to procurement and soldering specifications which require the contractor to impose these requirements on the vendors. One example is the increased requirements on PWB's in the DOD/MIL-STD-2000 series. They call out requirements over and above MIL-P-55110 for use under this document. Increased requirements on components are also proposed in MIL-STD-2000, Rev. A. Engineers, both Design and Components, must be aware of these additional requirements when designing, specifying, and procuring surface mount components.

APPENDIX B

PROPOSED REVISION TO MIL-HDBK-217

Surface Mount Interconnect Failure Rate Model

The failure rate model (refer to equation 3.3-1 of the report):

$$\lambda = \frac{N_u^{\beta-1}}{(A \cdot B \cdot C \cdot N_F)^{\beta}} \cdot 8 \cdot U \cdot 10^6 \cdot \pi_Q$$

Where:

A = Package Size Factor:

Adjustment for Package Size Referenced to Pin Count

Number Of Pins	Leadless	Leaded
10	X	
14	X	
16	1.00	1.00
18	0.46	0.91
20	0.43	0.82
24	0.37	0.74
28	0.33	0.65
32	0.30	0.59
44	0.23	0.46
68	0.16	0.31
84	0.13	0.26

(ref. Table 3.7.1-1)

B = Height Factor:

Adjustment for Solder Joint Height off the PWB

Height Times 0.001 inches	Leadless Factor	Leaded Factor
3	1.0	1.0
4	1.6	2.0
5	2.2	3.4
6	2.9	5.2
7	3.7	7.4
8	4.5	10.2
9	5.4	13.5
10	6.3	17.3

(ref. Table 3.7.2-1)

C = CTE Factor:

Adjustment for CTE mismatch between a device body and the PWB

PWB Material	CTE (ppm/°C)	Leadless Mismatch	C Factor Leadless	C Factor Leaded
G-10 or FR-4	16	10	1.0	1.0
Polyimide Kevlar	8	2	11.9	45.3
Epoxy CIC*	6.4	1	34.0	234.0
Epoxy Kevlar	8	2	11.9	45.3

(ref. Table 3.7.3-1)

π_Q = Quality Factor, Pie Q:

Mil Level	π_Q, Pie Q Factor
Military	1.0
Non-military	2.0

(ref. Table 3.7.4-1)

β = Distribution Parameter:

Lead Type	β
Leaded (J, S, Gull, etc.)	1.15
Leadless (LCC)	2.2

(ref. Table 3.6-3)

N_u,U = Default Usage Factors:

Environ.	Nu Typical Cycles	U Cycle Rate
GB	4000	0.1667
GF	4000	0.1667
GM	6000	0.5
NS	6000	0.3
NU	5000	0.25
AIC	10000	0.6667
AIF	20000	2.0
AUC	10000	0.6667
AUF	20000	2.0
ARW	20000	1.0
SF	15000	0.375
MF	1	0.1
ML	1	1.0
CL	1	1.0

(ref. Table 3.6-4)

N_f = Baseline Characteristic Life (Cycles to Failure) for Solder Joints:

ΔTemp. °C	LCC	Gull	J Lead	S Lead
5	1.32E+10	4.03E+15	1.70E+14	3.65E+13
10	7.16E+09	1.78E+15	8.60E+13	1.95E+13
15	3.87E+09	7.82E+14	4.30E+13	1.04E+13
20	2.09E+09	3.44E+14	2.20E+13	5.59E+12
25	1.13E+09	1.52E+14	1.10E+13	2.99E+12
30	6.11E+08	6.68E+13	5.50E+12	1.60E+12
35	3.31E+08	2.94E+13	2.80E+12	8.58E+11
40	1.79E+08	1.30E+13	1.40E+12	4.59E+11
45	9.66E+07	5.71E+12	7.10E+11	2.46E+11
50	5.22E+07	2.51E+12	3.60E+11	1.32E+11
55	2.82E+07	1.11E+12	1.80E+11	7.04E+10
60	1.53E+07	4.88E+11	9.10E+10	3.77E+10
65	8.26E+06	2.15E+11	4.60E+10	2.02E+10
70	4.46E+06	9.46E+10	2.30E+10	1.08E+10
75	2.41E+06	4.17E+10	1.20E+10	5.78E+09
80	1.30E+06	1.83E+10	5.90E+09	3.09E+09
85	7.05E+05	8.08E+09	3.00E+09	1.66E+09
90	3.81E+05	3.56E+09	1.50E+09	8.86E+08
95	2.06E+05	1.57E+09	7.50E+08	4.74E+08
100	1.11E+05	6.90E+08	3.80E+08	2.54E+08
105	6.03E+04	3.04E+08	1.90E+08	1.36E+08
110	3.26E+04	1.34E+08	9.60E+07	7.28E+07
115	1.76E+04	5.90E+07	4.90E+07	3.89E+07
120	9.52E+03	2.60E+07	2.40E+07	2.08E+07
125	5.15E+03	1.14E+07	1.20E+07	1.12E+07
130	2.78E+03	5.04E+06	6.20E+06	5.97E+06
135	1.50E+03	2.22E+06	3.10E+06	3.20E+06
140	8.13E+02	9.77E+05	1.60E+06	1.71E+06
145	4.40E+02	4.30E+05	8.00E+05	9.16E+05
150	2.38E+02	1.90E+05	4.00E+05	4.90E+05

APPENDIX C

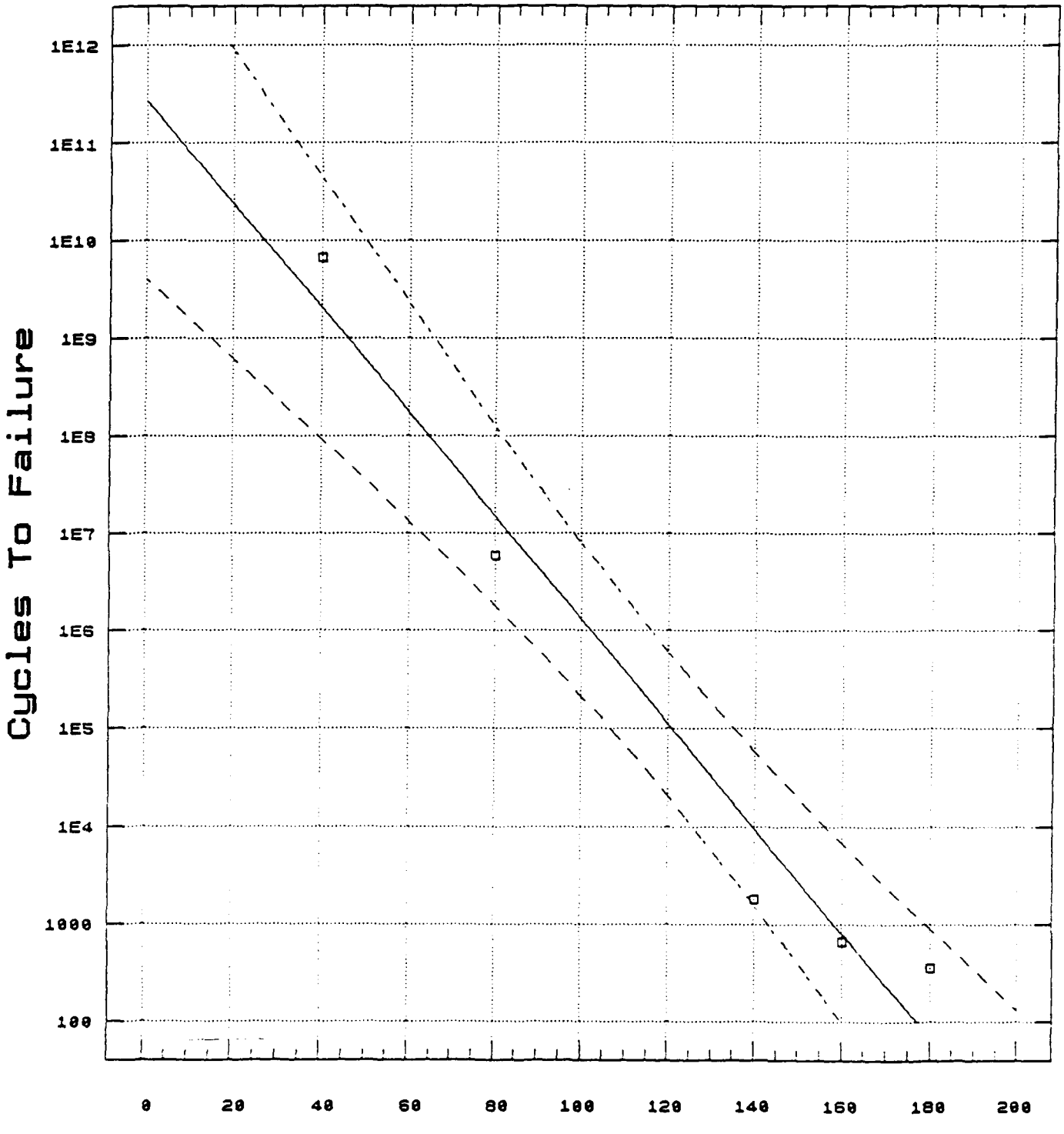
REGRESSION RESULTS

APPENDIX C

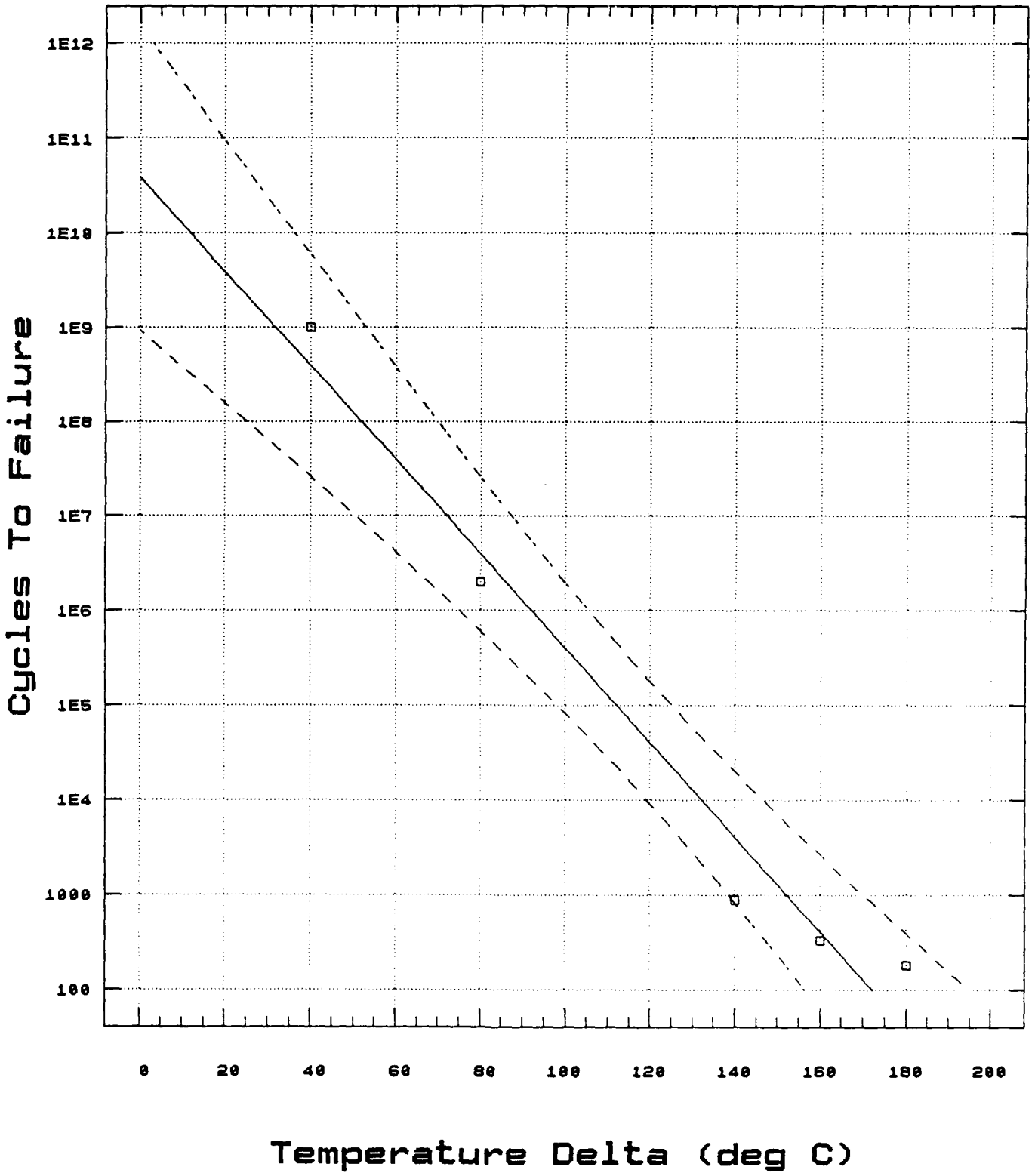
The charts that follow show the regressio plots of the FEA calculated cycles to failure verses temperature cycle range for the 16, 24, and 32 pin leadless and leaded devices. The plots show the fit of the regression equations (dark lines) based on the data. The dashed lines show the calculated 90 % upper and lower confidence interval levels. The plots are generated using STATGRAPHICS™ statistical analysis package on a personal computer.

Additional tables of calculated characteristic life of each package style for all pin counts and temperature cycle ranges are provided. These data reflect the model adjustments for Sections 3.6.2, 3.6.3, and package size adjustments of 3.7.1.

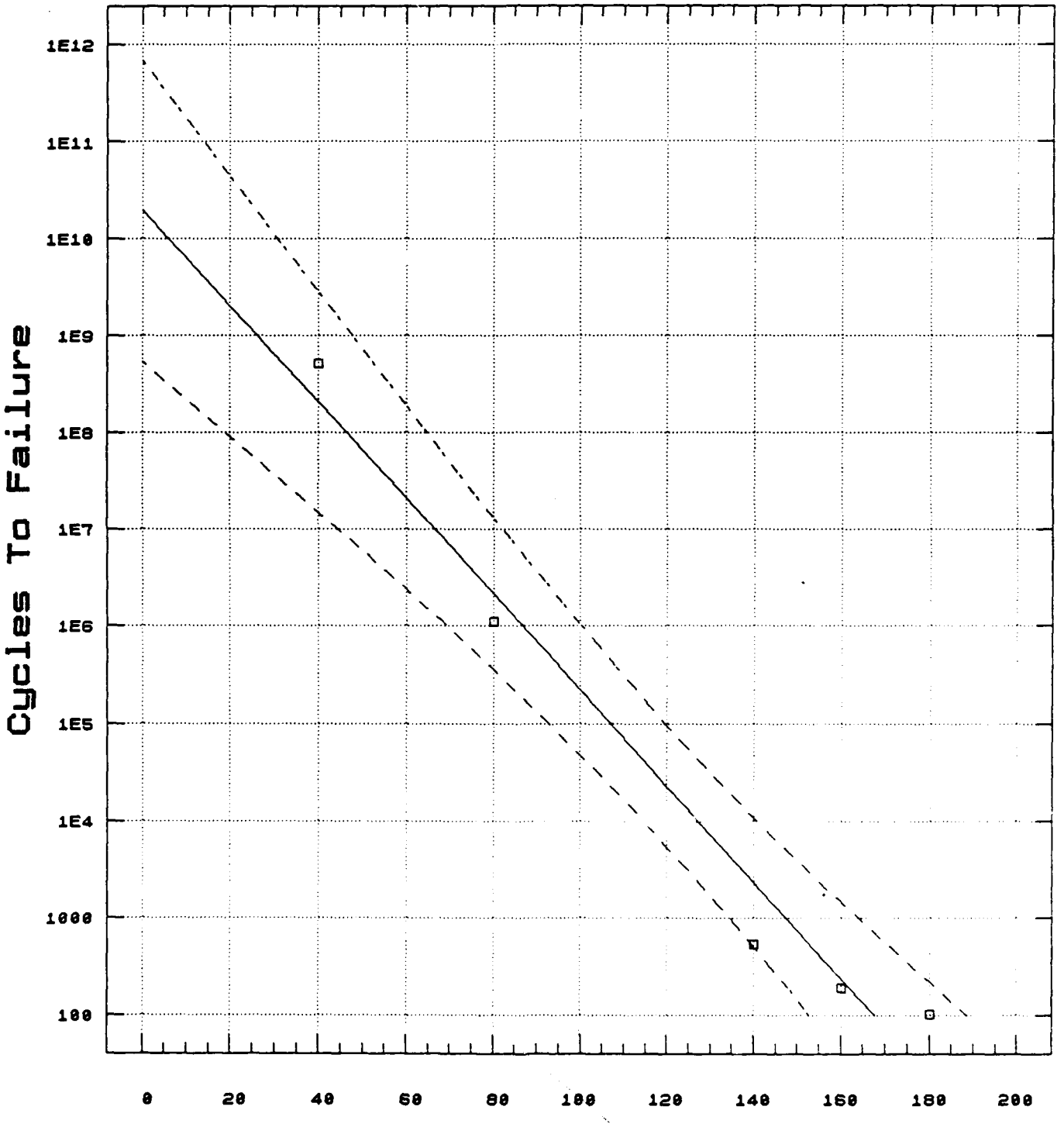
LCC, 16 Pin



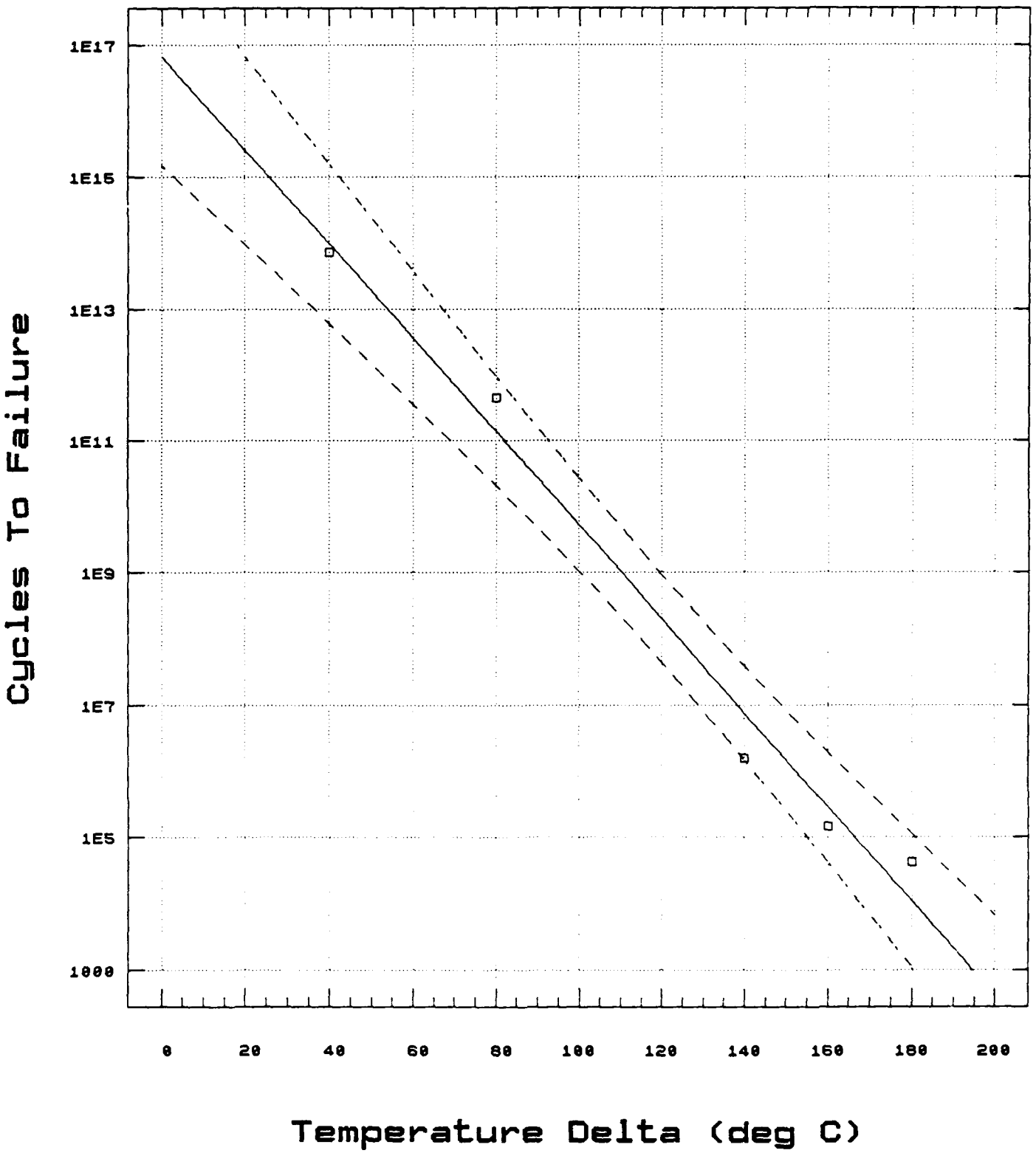
LCC, 24 Pins



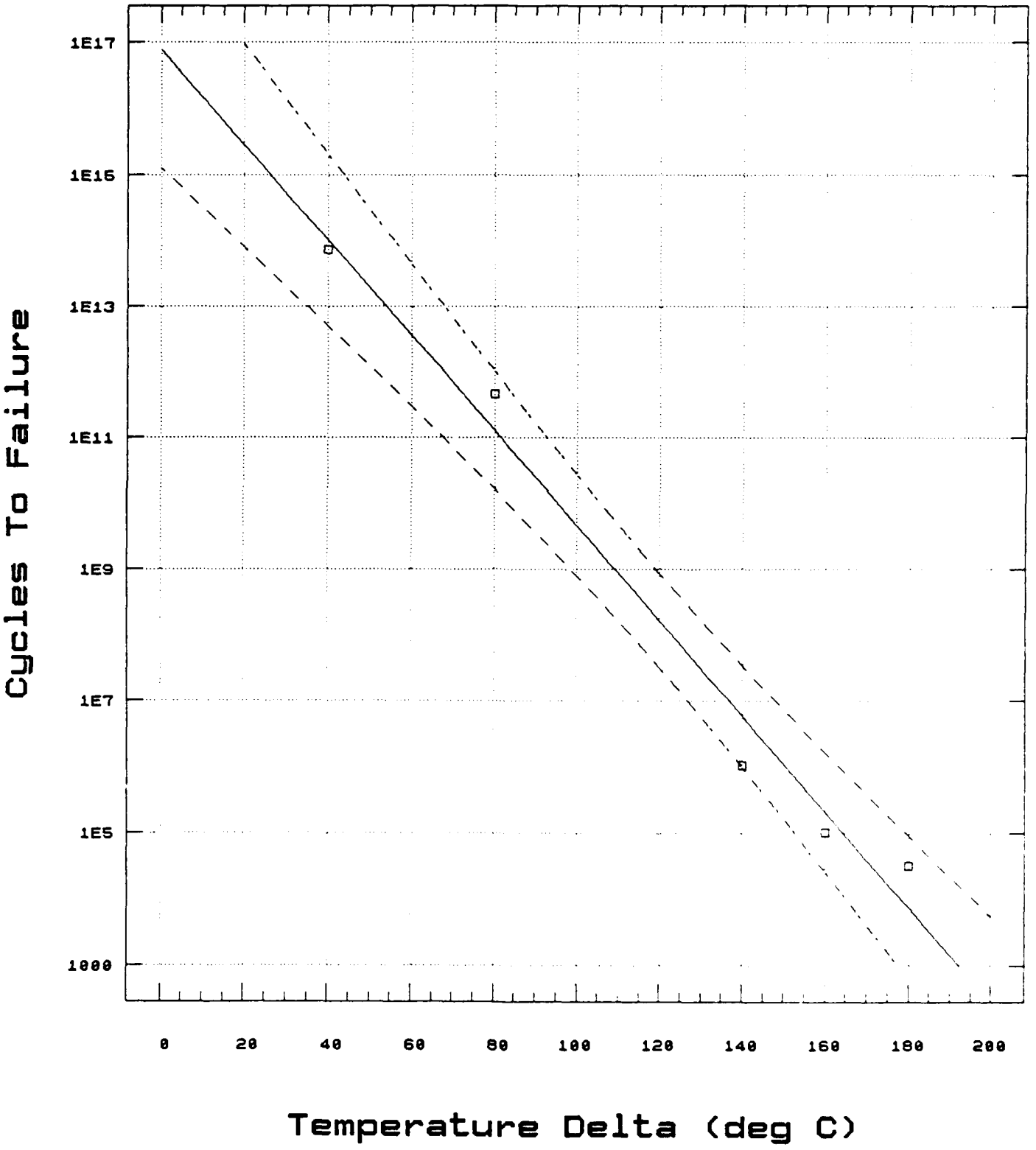
LCC, 32 Pins



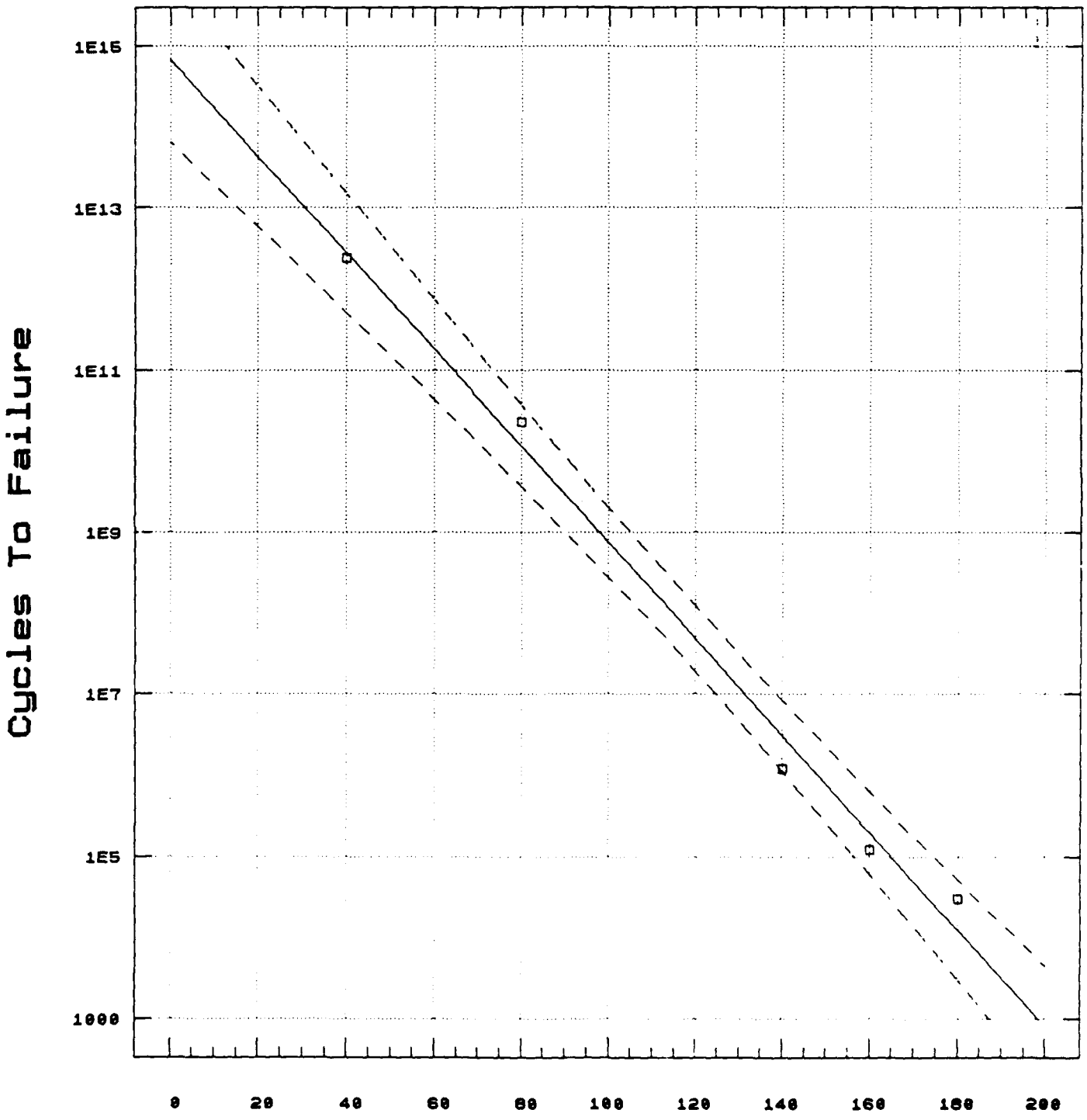
Gull Leads, 16 Pins



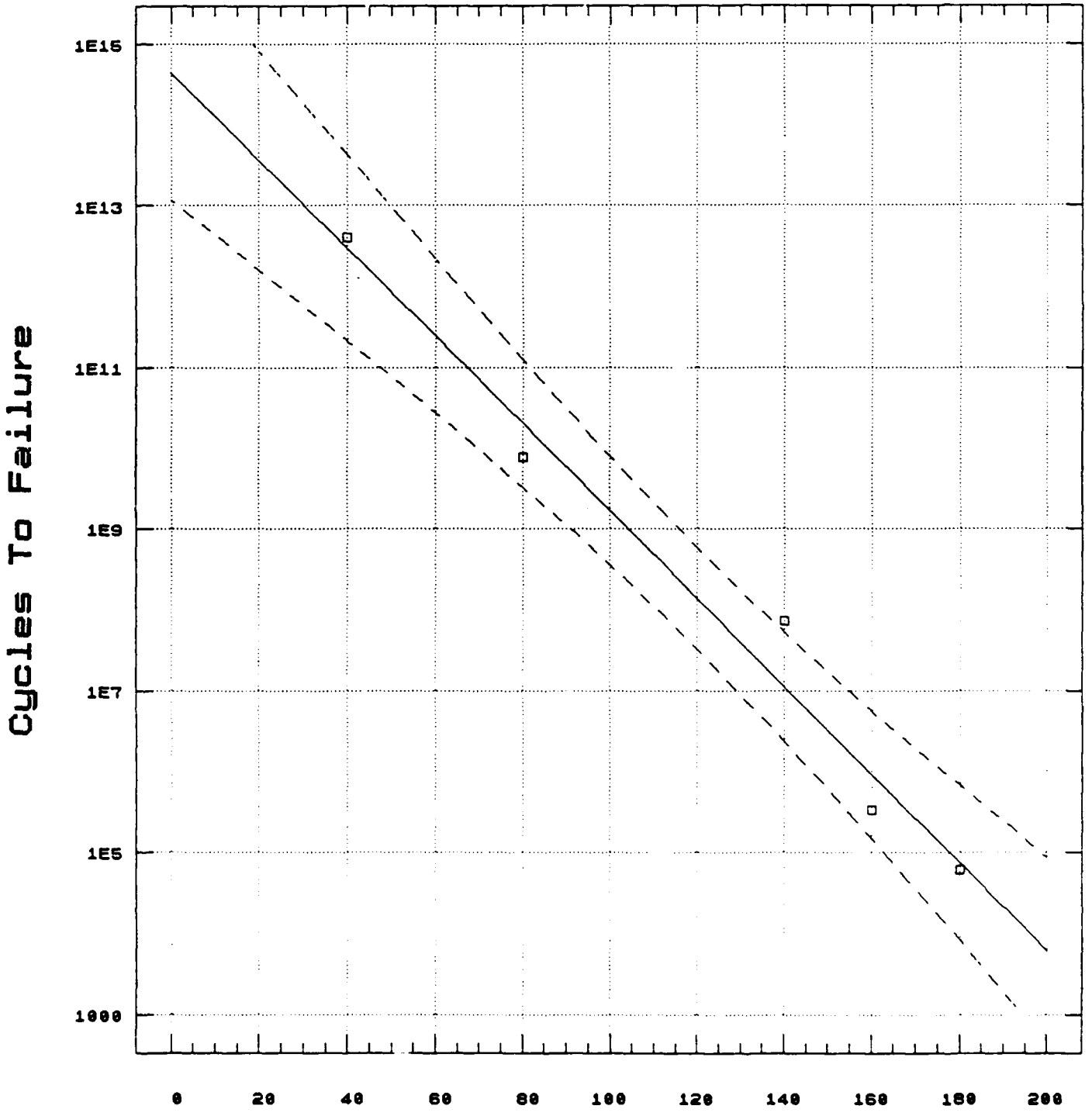
Gull Leads, 32 Pins



'J' Type Leads, 16 Pins



'S' Type Leads, 16 Pins



SMT MODEL

CHARACTERISTIC LIFE LCC CYCLES

PINS	16	24	32	68	84
DELTA T					
10	7.16E+09	2.27E+09	1.62E+09	6.01E+08	4.5E+08
20	2.09E+09	6.63E+08	4.73E+08	1.76E+08	1.3E+08
30	6.11E+08	1.94E+08	1.38E+08	5.14E+07	3.9E+07
40	1.79E+08	5.67E+07	4.04E+07	1.50E+07	1.1E+07
50	5.22E+07	1.66E+07	1.18E+07	4.39E+06	3.3E+06
60	1.53E+07	4.84E+06	3.45E+06	1.28E+06	9.6E+05
70	4.46E+06	1.41E+06	1.01E+06	3.75E+05	2.8E+05
80	1.30E+06	4.14E+05	2.95E+05	1.10E+05	8.2E+04
90	3.81E+05	1.21E+05	8.62E+04	3.20E+04	2.4E+04
100	1.11E+05	3.53E+04	2.52E+04	9.36E+03	7.0E+03
110	3.20E+04	1.03E+04	7.36E+03	2.74E+03	2.1E+03
120	9.52E+03	3.02E+03	2.15E+03	8.00E+02	6.0E+02
130	2.78E+03	8.82E+02	6.29E+02	2.34E+02	1.8E+02
140	8.13E+02	2.58E+02	1.84E+02	6.83E+01	5.1E+01
150	2.38E+02	7.54E+01	5.37E+01	2.00E+01	1.5E+01
160	6.95E+01	2.20E+01	1.57E+01	5.84E+00	4.4E+00
170	2.03E+01	6.44E+00	4.59E+00	1.71E+00	1.3E+00
180	5.94E+00	1.88E+00	1.34E+00	4.99E-01	3.7E-01

Table 1.9

CHARACTERISTIC LIFE GULL LEAD CYCLES

PINS	16	24	32	68	84
DELTA T					
10	1.89E+15	1.24E+15	7.92E+14	2.07E+14	1.5E+14
20	3.66E+14	2.41E+14	1.54E+14	4.02E+13	2.9E+13
30	7.10E+13	4.68E+13	2.98E+13	7.81E+12	5.7E+12
40	1.38E+13	9.09E+12	5.78E+12	1.51E+12	1.1E+12
50	2.67E+12	1.76E+12	1.12E+12	2.94E+11	2.1E+11
60	5.18E+11	3.42E+11	2.18E+11	5.70E+10	4.1E+10
70	1.00E+11	6.63E+10	4.22E+10	1.11E+10	8.0E+09
80	1.95E+10	1.29E+10	8.19E+09	2.14E+09	1.6E+09
90	3.78E+09	2.50E+09	1.59E+09	4.16E+08	3.0E+08
100	7.33E+08	4.84E+08	3.08E+08	8.07E+07	5.9E+07
110	1.42E+08	9.39E+07	5.98E+07	1.57E+07	1.1E+07
120	2.76E+07	1.82E+07	1.16E+07	3.04E+06	2.2E+06
130	5.35E+06	3.53E+06	2.25E+06	5.89E+05	4.3E+05
140	1.04E+06	6.85E+05	4.36E+05	1.14E+05	8.3E+04
150	2.01E+05	1.33E+05	8.46E+04	2.22E+04	1.6E+04
160	3.91E+04	2.58E+04	1.64E+04	4.30E+03	3.1E+03
170	7.58E+03	5.00E+03	3.18E+03	8.34E+02	6.1E+02
180	1.47E+03	9.71E+02	6.18E+02	1.62E+02	1.2E+02

Table 5.4

CHARACTERISTIC LIFE S LEAD CYCLES

PINS	16	24	32	68	84
DELTA T					
10	2.07E+13	1.37E+13	8.71E+12	2.28E+12	1.7E+12
20	5.94E+12	3.92E+12	2.50E+12	6.54E+11	4.8E+11
30	1.70E+12	1.12E+12	7.15E+11	1.87E+11	1.4E+11
40	4.88E+11	3.22E+11	2.05E+11	5.37E+10	3.9E+10
50	1.40E+11	9.23E+10	5.87E+10	1.54E+10	1.1E+10
60	4.00E+10	2.64E+10	1.68E+10	4.41E+09	3.2E+09
70	1.15E+10	7.57E+09	4.82E+09	1.26E+09	9.2E+08
80	3.29E+09	2.17E+09	1.38E+09	3.62E+08	2.6E+08
90	9.42E+08	6.22E+08	3.96E+08	1.04E+08	7.5E+07
100	2.70E+08	1.78E+08	1.13E+08	2.97E+07	2.2E+07
110	7.73E+07	5.10E+07	3.25E+07	8.50E+06	6.2E+06
120	2.21E+07	1.46E+07	9.30E+06	2.44E+06	1.8E+06
130	6.35E+06	4.19E+06	2.67E+06	6.98E+05	5.1E+05
140	1.82E+06	1.20E+06	7.64E+05	2.00E+05	1.5E+05
150	5.21E+05	3.44E+05	2.19E+05	5.73E+04	4.2E+04
160	1.49E+05	9.85E+04	6.27E+04	1.64E+04	1.2E+04
170	4.28E+04	2.82E+04	1.80E+04	4.70E+03	3.4E+03
180	1.23E+04	8.09E+03	5.15E+03	1.35E+03	9.8E+02

Table 5-13

CHARACTERISTIC LIFE J LEAD CYCLES

PINS	16	24	32	68	84
DELTA T					
10	9.11E+13	6.01E+13	3.83E+13	1.00E+13	7.3E+12
20	2.32E+13	1.53E+13	9.73E+12	2.55E+12	1.9E+12
30	5.88E+12	3.88E+12	2.47E+12	6.47E+11	4.7E+11
40	1.50E+12	9.87E+11	6.28E+11	1.64E+11	1.2E+11
50	3.80E+11	2.51E+11	1.60E+11	4.18E+10	3.0E+10
60	9.66E+10	6.37E+10	4.06E+10	1.06E+10	7.7E+09
70	2.45E+10	1.62E+10	1.03E+10	2.70E+09	2.0E+09
80	6.23E+09	4.11E+09	2.62E+09	6.86E+08	5.0E+08
90	1.58E+09	1.05E+09	6.65E+08	1.74E+08	1.3E+08
100	4.03E+08	2.66E+08	1.69E+08	4.43E+07	3.2E+07
110	1.02E+08	6.75E+07	4.30E+07	1.13E+07	8.2E+06
120	2.60E+07	1.72E+07	1.09E+07	2.86E+06	2.1E+06
130	6.60E+06	4.36E+06	2.77E+06	7.27E+05	5.3E+05
140	1.68E+06	1.11E+06	7.05E+05	1.85E+05	1.3E+05
150	4.26E+05	2.81E+05	1.79E+05	4.69E+04	3.4E+04
160	1.08E+05	7.15E+04	4.55E+04	1.19E+04	8.7E+03
170	2.75E+04	1.82E+04	1.16E+04	3.03E+03	2.2E+03
180	7.00E+03	4.62E+03	2.94E+03	7.70E+02	5.6E+02

APPENDIX D

FINITE ELEMENT ANALYSIS MODEL DEVELOPMENT

Appendix Text Excerpted from a Paper Co-authored by

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Submitted to IEEE for Publication

APPENDIX D

FINITE ELEMENT ANALYSIS MODEL DEVELOPMENT

I. INTRODUCTION

SMT is a technology which has been implemented into military and commercial applications for over a decade and yet has very little field data and information available concerning reliability. Consequently, both test and analysis data is required to assess the potential reliability of new, innovative SMT designs. Harris used a Finite Element Analysis (FEA) software program (ANSYS) to generate data relating the package size, lead arrangement and board material to the number of thermal cycles to failure for a SMT device.

Thermal cycle fatigue is the dominating factor in the failure of solder joints despite the fact that vibration, shock and power on/off cycles play a role in the failure mechanism of solder joints. Thermal fatigue failure in solder joints occurs due to the mismatch in the coefficient of thermal expansion (CTE) among the soldered components, i.e. the chip carrier, solder and the printed wiring board (PWB). In an environment where the temperature may vary from -55°C to +125°C, the CTE mismatch causes an appreciable build up of complex stresses in the solder joints, which fail after undergoing a number of thermal cycles. The number of cycles to failure depends on the temperature variation, geometry of both the IC device and the solder joints, amount of CTE mismatch, type of IC device (e.g. leadless and leaded), etc. The temperature variation impacts solder joint failure due to the thermal stresses induced by the materials and geometry, and because of solder's behavior over this temperature range.

In particular, solder undergoes several phase transitions over the -55 to +125°C temperature range. The main concern relating to solder's use is that it begins to transition from the elastic deformation mode to an elastic/plastic deformation mode at around 30 to 35°C. Eutectic solder's melting point is 183°C. It is known that significant creep is observed in metals having homologous temperatures, T/T_{melt} (in °K), above 0.5. The homologous temperature for eutectic solder at room temperature (25°C) is 0.653. This value is confirmed by published test data in literature and correlates with the analysis results. The consequence of solder's phase transition is that stress analysis becomes more complex as the temperature rises. An appropriate creep equation, along with stress/strain curves at different temperature levels, must be utilized in the FEA.

Even though data exists on solder and solder joint failure, most of this data can not be used and/or

compared with other data. This is due to several factors; the primary one being the definition of a joint failure. The determination of the fatigue ductility exponent will be based on the definition of "point of failure" in a SMT solder joint. The "point of failure" is defined as the time to first appearance of a visible crack in the solder joint. The rationale behind this is that once a crack is developed in the joint, it might fracture and become electrically disconnected when subjected to severe amounts of subsequent vibration, shock or other loadings. The solder joint, however, may last additional cycles under thermal cycling alone.

II. FINITE ELEMENT ANALYSIS

As electronic packaging continues to decrease in size, it becomes critical that tentative designs are assessed in the conceptual design stage. One computer analysis technique, Finite Element Analysis (FEA), has become a leader in this field. FEA is a proven technique to predict the thermal and mechanical responses within a structure. The structure is modeled using two parameters: nodes and elements. A node is a grid point located in two or three dimensional space and an element is a geometrical configuration represented by a series of nodes. The geometrical model, materials, loading and boundary conditions are used as input data for the FEA code and a resulting strain distribution obtained. These strain values are then substituted into the Coffin-Manson model to predict the number of thermal cycles to failure. The FEA code ANSYS, developed by Swanson Analysis Systems, was utilized in this study for both the model generation and actual analysis. In the past, the majority of FEAs performed on electronic packages simulated purely elastic strains. Because of solder's complex nature, this study included FEAs that predicted the elastic, plastic and creep strains, which were then combined to obtain an equivalent total strain.

During this study, non-linear finite element analyses were performed on surface mounted solder joints in order to determine the relative magnitude of linear and non-linear strains. The appropriate strain level was then used to estimate solder joint life. Detailed material data over the temperature range of -55°C to +125°C was required for eutectic tin/lead solder. The elastic, plastic and creep strains obtained from the FEA results were combined to obtain an equivalent total strain. The range of this equivalent total strain was then used in the Coffin-Manson model in order to estimate the number of cycles to failure. An alternative method for determining the coefficients and exponents in the Coffin-Manson equation is presented using FEA and test results. Analysis results showed that creep has a substantial effect on total strain. For this reason, FEA reliability modelling of surface mounted designs can not be limited to linear elastic analysis. Instead, analyses must utilize non-linear codes along with detailed material data over a wide temperature range. This results in more complex analyses and a significant increase in computer processing time.

Finite element models (FEMs) were generated for Leadless Chip Carrier (LCC), Gull-wing, "J" lead and "S" lead devices. Figures 1-3 display the geometric information on which three of these models were based. When the structure being modeled is symmetrical, both in geometry and loading conditions, only a section of the structure needs to be modeled. A square package has 1/8 symmetry. Adjusting some of the dimensions to represent a square package reduces complexity, computer processing time and cost. Each FEM generated consisted of a ceramic chip carrier, chip carrier lid, PWB and solder joint. The joints for the leaded packages were represented by a lead with solder and the leadless joint was represented by solder alone. The FEMs are shown in Figures 4-8. The X, Y, and Z directions for Figures 4-8 are shown in Figures 1-3. The ceramic chip carrier and the solder joints were modeled as eight node isoparametric solid elements (STIFF 45 in ANSYS [1]), an example of which is displayed in Figure 9. The PWB (Epoxy-Glass) and the chip carrier lid (Kovar) were modeled as elastic quadrilateral shell elements (STIFF 63 in ANSYS [1]), an example of which is displayed in Figure 10. For the analysis, the thickness was assumed to be 0.05 inch for the PWB and 0.01 inch for the chip carrier lid. A pitch of 50 mil was assumed for all the analyses.

In order to define the load steps in the ANSYS FEA, the time-temperature profile used to thermal cycle surface mounted IC devices had to be identified. Load steps in the form of time versus temperature data points are used as input in ANSYS. Many load steps are required to represent the entire thermal cycle profile. Each load step may again contain many iterations so that the plasticity convergence criteria for the FEA is met. MIL-STD-883 Method 1010 does not specify any particular thermal cycle test criteria for PWB assemblies with surface mounted devices. But the generally accepted thermal cycle test standard in the industry has been test condition B(-55°C to +125°C) for 1000 cycles. Because of the controversy over the correlation between this particular test temperature range and actual use conditions, three temperature profiles were selected, as follows, to evaluate the effects of different temperature ranges: -55°C to +125°C; -55°C to +105°C; and -55°C to +85°C. These temperature profiles consist of a ramp function of 5 to 10°C/minute between the two extreme temperatures and a dwell time of 10 to 30 minutes at both the maximum and minimum values. The profiles used in this study had 10 minute dwell times and the ramp function displayed in Figure 11.

The ANSYS code handles plasticity problems by following incremental steps [2]. After an iteration is performed, ANSYS modifies the load vector to account for the stress that the material can support at the current strain value. Consequently, the stress calculated in the next iteration approaches this value. Plasticity convergence occurs whenever the ratio of the plastic strain increment ($\Delta\varepsilon_{pl}$) to the elastic strain (ε_{el}) is less than or equal to a specified value. In this analysis, a plasticity ratio of 0.05 was chosen based on guidelines provided by the ANSYS users manual.

In order to input the effects of creep into the FEA, the following format was required by the ANSYS software code [2]:

$$d\varepsilon_{cr} = C1\ \sigma^{C2}\ \varepsilon^{C3}\ \exp[-C4/T]\ x\ dt \qquad (A)$$

Where,

ε = Equivalent strain; t = Time at the end of iteration

σ = Equivalent stress; T = Absolute temperature

C1, C2, C3, and C4 are the values of the constants which are used as input data for the ANSYS preprocessor. Other material information required by ANSYS included the stress-strain curve for a bilinear, kinematically hardening material, which is shown in Figure 12. The Young's Modulus E(T) for the elastic portion and the Tangent Modulus E_T for the plastic portion are shown for a particular temperature. A series of such curves can be obtained at other temperatures of interest. Eutectic solder was assumed to be a bilinear, kinematically hardening material for the analysis purpose.

When performing a non-linear FEA, the proper material data must be obtained. A literature search ([3] through [6]) was conducted for this purpose. The elastic properties used in this analysis are given in Table 1. These values were taken at room temperature (25°C). Since the properties of solder vary over the temperature range, the Young's Modulus (Modulus of Elasticity), Tangent Modulus and the Yield Stress are required at selected temperatures. The values used in the FEA are provided in Table 2. The stress/strain profiles accounting for solder's transition throughout the temperature variation are shown in Figures 13, and the corresponding data values are presented in Tables 3 and 4. The Tangent Modulus at 24°C (Table 4) seems to be incorrect and consequently, was discarded. Table 2 shows all the compiled data selected for the analysis.

As mentioned in the previous section, in addition to the data on material property variation with temperature, several parameters are required to simulate the creep effects in the solder. Two papers will be referenced along with the work performed in this area. The first paper is entitled, "High Temperature Deformation of the Pb-Sn Eutectic" [7]. This paper gives the creep equation for eutectic solder in the following form:

$$d\varepsilon/dt = K\sigma^{n'} \exp[-(\Delta H_o - V_o\,\sigma) / kT] \qquad (B)$$

Where,

$K = 9.0 \times 10^{-18}$ M. K. S.

$n' = 3.4$

$\Delta H_o = 0.82$ eV $= 1.313 \times 10^{-19}$ Joules

k = Boltzman Constant $= 1.38062 \times 10^{-23}$ Joules/Kelvin

$V_o = 10 \times 10^{-28}$ m^3

Substituting these values into the creep equation (B) gives,

$$d\varepsilon/dt = 9.0 \times 10^{-18} \times \sigma^{3.4} \times \exp[-(9507 - 7.246 \times 10^{-5}\sigma)/T]$$

Since the term $7.246 \times 10^{-5}\ \sigma$ is very small compared with 9507, it can be neglected, thus giving:

$$d\varepsilon = 9.0 \times 10^{-18} \times \sigma^{3.4} \times \exp[-9507/T] \times dt$$

Converting σ from psi to Newton/m^2; (1 psi = 6894.65 N/m^2), gives:

$$\mathbf{d\varepsilon = 1.012 \times 10^{-4} \times \sigma^{3.4} \times \exp[-9507/T] \times dt} \qquad \mathbf{(C)}$$

The above modified equation (C) was used for the analysis.

A second creep equation was analyzed for comparison. This equation was presented in the paper, "Deformation Of Pb-Sn Eutectic Alloys at Relatively High Strain Rates" [8]. This equation addresses important factors that effect the determination of creep's magnitude and is presented below:

$$\mathbf{\dot{\gamma}^* = [900\ (\tau^*)^{1.96}\ (d^*)^{-1.8}\ \exp(-11500/RT)] + [(1.3 \times 10^{15})\ (\tau^*)^{7.1}\ \exp(-19400/RT)]} \qquad \mathbf{(D)}$$

where,

$\dot{\gamma}^*$ = $\dot{\gamma}kT/D_oGb$ (a dimensionless strain rate)

τ^* = τ/G (a dimensionless shear stress)

d^* = d/b (a dimensionless grain size)

$\dot{\gamma}$ = Strain Rate

k = Boltzman Constant $= 1.38 \times 10^{-23}$ Joules/Kelvin

T = Absolute Temperature

D_o = Diffusivity for pure Sn (0.08 cm^2/s)

G = Shear modulus of pure Sn (2×10^{11} dynes/cm2)

b	=	Bergers Vector of pure Sn (3.18 A)
τ	=	Resolved Shear Stress
d	=	Mean Grain Diameter (5.5 μM to9.9 μM)

Taking $\tau = (\sqrt{3})\tau$; $(\sqrt{3})\varepsilon = \gamma$; τ in psi = τ x 68930 dynes/cm^2 and plugging all the values into equation (D), the value of $d\varepsilon$ (for temperature = +125°C) was found to vary from 5.0 x10^{-3}dt to 8.0x10^{-4}dt. This range was obtained by considering the tolerances of the variables in the creep equation (D). Unfortunately, many simplifications were required in order to convert the second creep equation (D), into a format which was compatible with ANSYS input format, equation (A).

The value of $d\varepsilon$ (for temperature = +125°C) calculated from the creep equation (C) was found to fall within the above range. Equation (C) is compatible with ANSYS input format for creep and was consequently selected for the analysis.

IV. COFFIN-MANSON EQUATION

Elastic, plastic, and creep strain components from the FEA analysis results could be combined to obtain an equivalent strain. This equivalent strain could then be used to estimate the number of cycles to failure by using the Coffin-Manson equation [9]. In order to do so, values of the exponents and the coefficients in the equation need to be determined for solder. The Coffin-Manson equation is given below:

$$\frac{\Delta\varepsilon}{2} = \frac{\sigma_f}{E}(2N_f)^b + \varepsilon_f(2N_f)^c \qquad \text{(E)}$$

Where,

$\Delta\varepsilon/2$	=	Total Strain Amplitude
σ_f	=	Fatigue Strength Coefficient
ε_f	=	Fatigue Ductility Coefficient
b	=	Fatigue Strength Exponent
c	=	Fatigue Ductility Exponent
N_f	=	Number of Cycles-To-Failure

The values of "ε_f" and "c" can be determined from test data and FEA analysis results [10]. As an example, assume that the results of an analysis shows that $\Delta\varepsilon/2$ = 0.024 for 16 I/O LCC and 0.034 for 24 I/O LCC. Taking σ_f = 7300 psi, E = 3.6 x 10^6 psi, and b = -0.05 and substituting this data into the Coffin-Manson

equation (E),

$$0.024 = 0.002 \times (2N_1)^{-0.05} + \varepsilon_f (2N_1)^c \quad \text{(F)}$$

$$0.034 = 0.002 \times (2N_2)^{-0.05} + \varepsilon_f (2N_2)^c \quad \text{(G)}$$

Also assume that from test results, N_1 = 200 cycles for 16-I/O LCC, and N_2 = 100 cycles for a 24-I/O LCC. Substituting these values in equation (F) and (G) gives the following:

$$0.024 = 0.002 \times (400)^{-0.05} + \varepsilon_f (400)^c \quad \text{(H)}$$

$$0.034 = 0.002 \times (200)^{-0.05} + \varepsilon_f (200)^c \quad \text{(J)}$$

Solving equations (H) and (J) gives:

ε_f = 0.532 ; and c = -0.528

A third set of analysis data and test results will enable the value of "b" to be determined using the same procedure.

The above procedure does not address the issue of frequency dependency. However, if enough test data and FEA analysis results are available, relations could easily be established between the frequency and "c", "ε_f", and "b" in the Coffin-Manson equation with suitable curve fitting equations.

V. RESULTS

Elastic, plastic, and creep strains were obtained for all the solder elements in the coordinate directions. The components of the elastic, plastic, and creep strains were added in the X, Y, Z, XY, YZ, and XZ directions. If these strains are denoted by ε_X, ε_Y, ε_Z, ε_{XY}, ε_{YZ} , and ε_{XZ}, then the equivalent total strain $\varepsilon_{eq\text{-}total}$ is given by [11]:

$$\varepsilon_{eq\text{-}total} = \frac{\sqrt{2}}{3}\left[(\varepsilon_X-\varepsilon_Y)^2 + (\varepsilon_Y-\varepsilon_Z)^2 + (\varepsilon_Z-\varepsilon_X)^2 + 6(\varepsilon_{XY}^2 + \varepsilon_{YZ}^2 + \varepsilon_{XZ}^2)\right]^{1/2} \quad \text{(K)}$$

However, instead of tensor shear strain, ANSYS computes the engineering shear strain "γ" as follows [11]:

$\gamma_{XY} = 2\varepsilon_{XY}$; $\gamma_{YZ} = 2\varepsilon_{YZ}$; $\gamma_{XZ} = 2\varepsilon_{XZ}$

ANSYS postprocessing [10] provides ε_X, ε_Y, ε_Z, γ_{XY}, γ_{YZ}, and γ_{XZ}. Therefore, the equation for the equivalent strain becomes,

$$\varepsilon_{eq\text{-}total} = \frac{\sqrt{2}}{3}\left[(\varepsilon_X-\varepsilon_Y)^2 + (\varepsilon_Y-\varepsilon_Z)^2 + (\varepsilon_Z-\varepsilon_X)^2 + (3/2)(\gamma_{XY}^2 + \gamma_{YZ}^2+\gamma_{XZ}^2)\right]^{1/2} \qquad (L)$$

This paper presents the FEA results for the worst case solder joint element. This element was determined based on the value of $\varepsilon_{eq\text{-}total}$. The maximum strained solder element was found to be in the corner joint and located underneath the ceramic chip carrier. This agrees with the test results in which failure of solder joints occurs first in the corner joint. When the first joint failure occurs in an intermediate location, it is found to be due to process control and workmanship.

Three different thermal profiles were simulated. The thermal profiles for the analyses are shown in Figure 11. Each individual strain component was analyzed by comparing the magnitude of its elastic, plastic and creep strains. The X-component of elastic strain, the X-component of plastic strain and the X-component of creep strain are shown in Figure 14. Figures 15-19 show the elastic, plastic, and creep strain components in the Y, Z, XY, YZ, and XZ coordinate directions, respectively. Figures 20-21 show the variations of the equivalent stress (SIGE in ANSYS) and the equivalent total strain ($\varepsilon_{eq\text{-}total}$) respectively. The X-axis (Figures 14-22) represents the linear time scale versus the actual temperature profile. From these curves, it is observed that the creep effect begins to play its dominating role at around 30°C and is the leading contributor to the total strain. The plastic strain, in comparison, stabilizes at almost the same temperature indicating that the yield stress of solder is raised due to plastic deformation while going from +25°C to -55°C and subsequent unloading from -55°C to higher temperature.

The elastic, plastic, and creep strain values were then combined in the respective coordinate directions to provide the total strains, ε_X, ε_Y, ε_Z, γ_{XY}, γ_{YZ}, and γ_{XZ},
where;

$$\varepsilon_X = \varepsilon_{X(elastic)} + \varepsilon_{X(plastic)} + \varepsilon_{X(creep)}$$
$$\varepsilon_Y = \varepsilon_{Y(elastic)} + \varepsilon_{Y(plastic)} + \varepsilon_{Y(creep)}$$
$$\varepsilon_Z = \varepsilon_{Z(elastic)} + \varepsilon_{Z(plastic)} + \varepsilon_{Z(creep)}$$
$$\gamma_{XY} = \gamma_{XY(elastic)} + \gamma_{XY(plastic)} + \gamma_{XY(creep)}$$
$$\gamma_{YZ} = \gamma_{YZ(elastic)} + \gamma_{YZ(plastic)} + \gamma_{YZ(creep)}$$
$$\gamma_{XZ} = \gamma_{XZ(elastic)} + \gamma_{XZ(plastic)} + \gamma_{XZ(creep)}$$

Using equation (L) and the FEA results, total strain amplitude, $\Delta\varepsilon/2$, was determined as follows:

$$\frac{\Delta\varepsilon}{2} = .5[(\varepsilon_{eq\text{-}total})_{max} - (\varepsilon_{eq\text{-}total})_{min}]$$

The total strain amplitudes (for -55°C to +125°C thermal cycle), for the 16 I/O LCC, 32 I/O LCC, and the

68 I/O LCC were found to be 0.0137, 0.0242, and 0.0442 respectively.

Assuming the values of $\varepsilon_f = 0.325$, $\sigma_f = 7300$ psi, $E = 3.6 \times 10^6$ psi, $b = -0.05$, and $c = -0.50$, the number of cycles to failure was found to be 353 cycles, 102 cycles, and 30 cycles for the 16 I/O LCC, 32 I/O LCC, and the 68 I/O LCC respectively. Table 5 shows the complete analysis results for the three different thermal cycling ranges.

To determine the effect of increased dwell time at high temperature, FEA was performed for a 16 I/O LCC. Figure 22 shows the XY component of elastic, plastic and creep strains for a dwell time of 3.27 hours at 125°C. Inspection of Figure 22 shows that no appreciable creep strain occurs at low temperature and that creep strain at high temperature is significant only during the first few minutes of dwell and then approaches an asymptote. It should be noted that microstructural changes that might occur in solder during prolonged dwell at high temperature may have an important effect, but is beyond the scope of this paper.

VI. FEA CONCLUSION

It has become clear that the creep in solder has a substantial effect on the overall strain and thus the solder joint's life. FEAs must incorporate this effect when thermal cycling in order to have validity. This point addresses the controversy of using the -55°C to +125°C thermal profile for accelerated testing. This profile obviously introduces different behavior from the actual field environment. The question arises as to whether this behavior introduces new failure mechanisms or merely accelerates actual ones. If new failure mechanisms are introduced and new improved accelerated tests can not be generated, an alternative would be to perform accurate FEAs on the surface mounted designs under consideration and then perform Environmental Stress Screening (ESS) tests on fielded devices in order to remove defective joints.

This appendix has shown the importance of finite element modelling and its ability to provide much needed data, which was not readily obtainable from the field. In addition to supplying the data needed, the analysis was able to do so with considerable correlation to the available test results. Further reliability model development would have been suspect, if at all possible, without the additional data obtained from the FEA.

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APPENDIX D SUPPLEMENT

MATERIAL PROPERTIES USED IN FINITE ELEMENT ANALYSIS MODEL DEVELOPMENT AND ILLUSTRATIONS OF TYPICAL FEA MODELS

TENSILE TEST DATA FOR PHASE 1 SOLDER ALLOYS

STRAIN RATE = 0.0002 mm/mm/sec

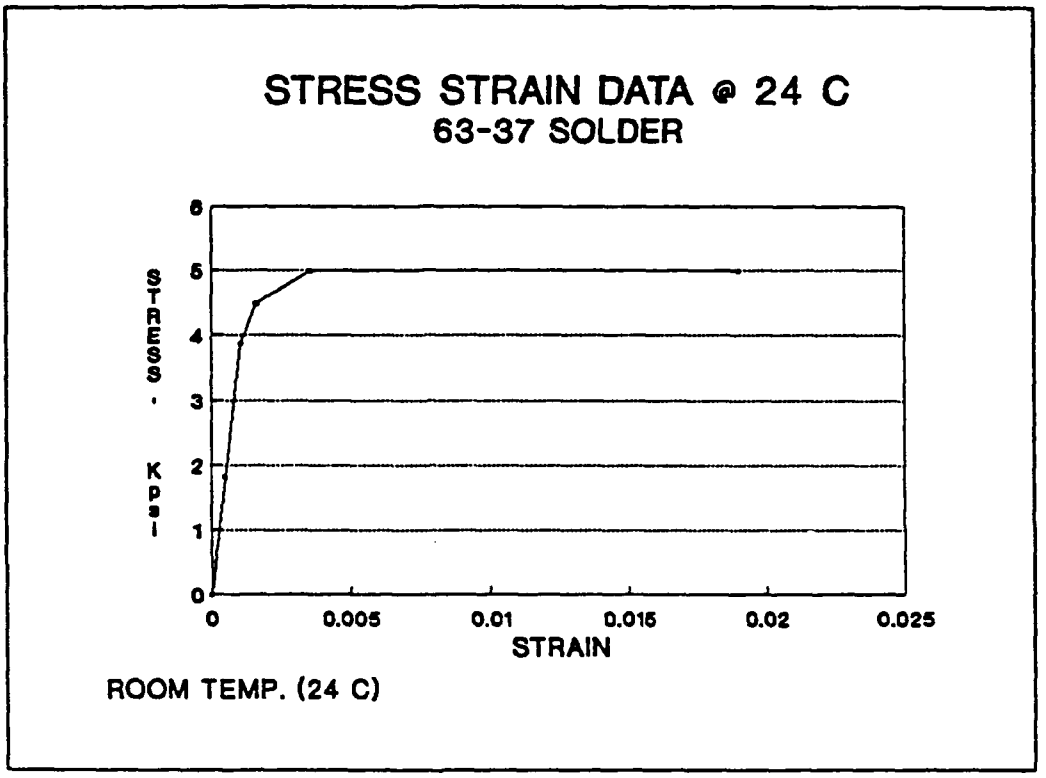
Material Test Temperature (°C)	Yield Stress MPa(psi)	Ultimate Tensile Str. MPa(psi)	Modulus of Elast. MPa(ksi)	Ductility Elongn. %	 Red. Area %
Sn63					
-55	49.64 (7200)	67.36 (9770)	66,050 (9580)	30.6	36.9
+23	20.96 (3040)	22.82 (3310)	29,030 (4210)	37.0	51.1
+125	8.93 (1230)	9.51 (1380)	15,030 (2180)	16.0	91.0
Sn63 Solderlastic					
-55	52.81 (7660)	61.50 (8920)	46,600 (6760)	30.8	44.9
+23	20.20 (2930)	22.27 (3270)	27,580 (4000)	72.5	77.1
+125	10.41 (1510)	11.58 (1680)	15,170 (2200)	15.0	91.0
99.99% 60Sn-40Pb					
-55	93.62 (6820)	74.00(10740)	52,610 (7630)	35.4	42.8
+23	30.20 (4380)	33.99 (4930)	31,580 (4580)	27.5	36.5
+125	13.17 (1920)	14.00 (2030)	20,750 (3010)	12.5	51.4
Ag2.5					
-55	24.13 (3500)	44.54 (6460)	27,860 (4040)	35.2	74.8
+23	19.10 (2770)	32.13 (4660)	20,820 (3310)	37.7	70.6
+125	12.75 (1850)	15.58 (2260)	17,930 (2600)	14.3	64.8
50Pb 50In					
-55	33.09 (4800)	42.34 (6140)	13,580 (1970)	16.8	28.9
+23	21.71 (3150)	31.10 (4510)	8,890 (1290)	34.5	43.9
+125	1.62 (234)	1.64 (238)	2,230 (323)	16.6	99.0

REF: WESTINGHOUSE - "SOLDER ALLOY DEVELOPMENT FOR ELECTRONIC CHIP CARRIER"
AFWAL-TR-88-4215

DS1

STRESS STRAIN DATA FOR 63-37 SOLDER

AT 24^0 C
Monotonic Test Data
Strain Rate = 0.002 in/in/sec.



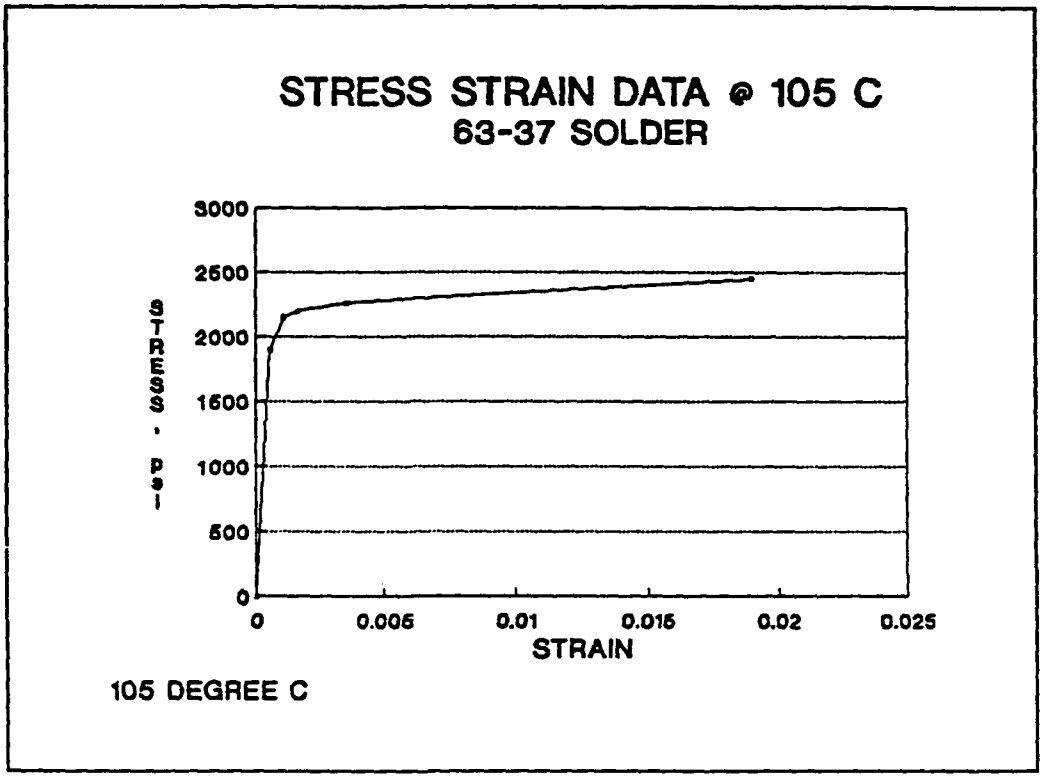
POINTS	STRAIN	STRESS , psi
1	0.5003 E-3	1811
2	0.1070 E-2	3875
3	0.1620 E-2	4490
4	0.3550 E-2	4995
5	0.1900 E-1	5000

YIELD STRESS	σ_y = 3875 psi	
YOUNG'S MODULUS	E = 3.62 E+06	(Elastic Range)
TANGENT MODULUS	E_T = 323.60 psi	(Plastic Range) (Incorrect Data--Not Used)

Ref. : MANTECH FOR ADVANCED DATA/SIGNAL PROCESING (VHSIC)

STRESS STRAIN DATA FOR 63-37 SOLDER

AT 105^0 C
Monotonic Test Data
Strain Rate = 0.002 in/in/sec.



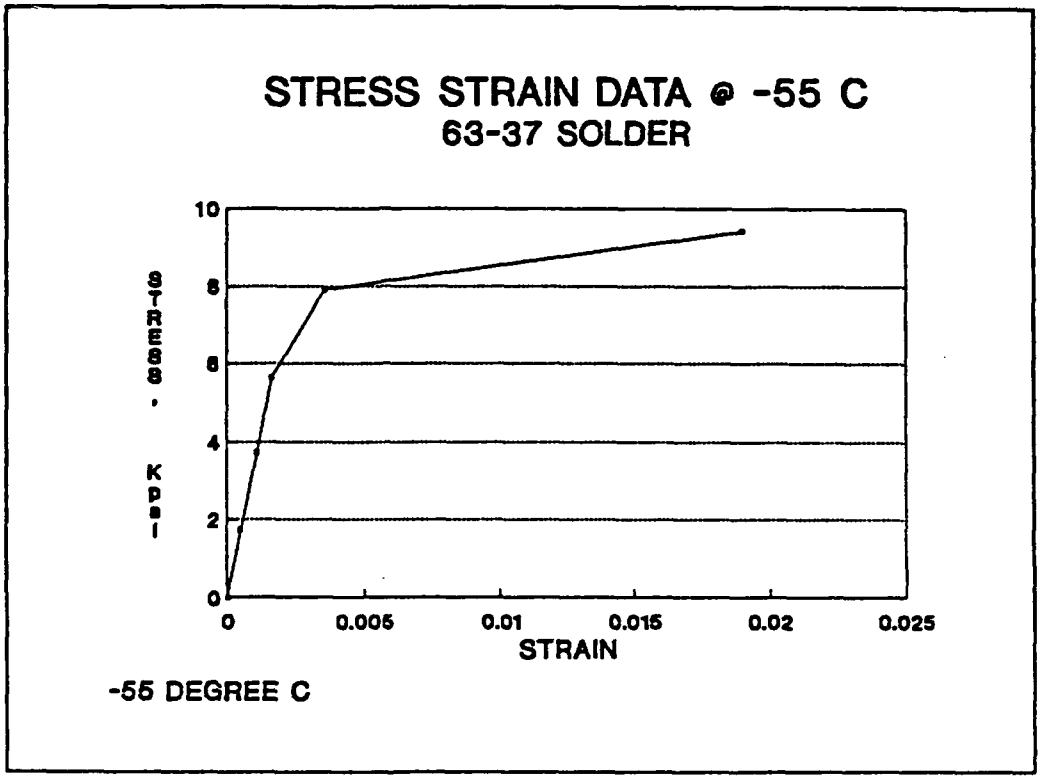
POINTS	STRAIN	STRESS , psi
1	0.5249 E-3	1900
2	0.1070 E-2	2150
3	0.1620 E-2	2200
4	0.3550 E-2	2260
5	0.1900 E-1	2450

YIELD STRESS	σ_y	= 1900 psi		
YOUNG'S MODULUS	E	= 3.62 E+06	psi	(Elastic Range)
TANGENT MODULUS	E_T	= 12297.73	psi	(Plastic Range)

Ref. : MANTECH FOR ADVANCED DATA/SIGNAL PROCESING (VHSIC)

STRESS STRAIN DATA FOR 63-37 SOLDER

AT -55^0 C
Monotonic Test Data
Strain Rate = 0.002 in/in/sec.



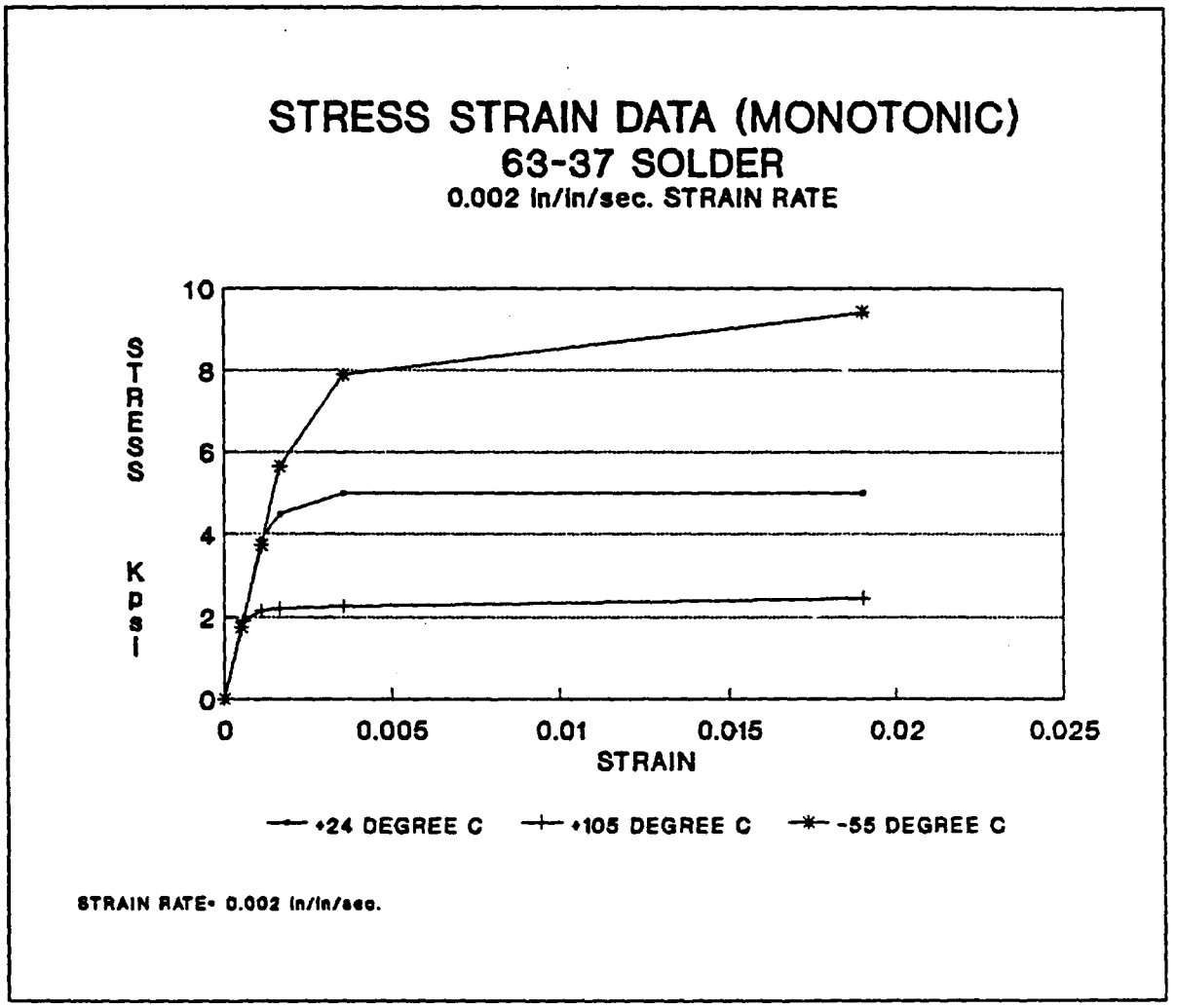
POINTS	STRAIN	STRESS , psi
1	0.4907 E-3	1740
2	0.1070 E-2	3724
3	0.1620 E-2	5638
4	0.3550 E-2	7900
5	0.1900 E-1	9420

YIELD STRESS	σ_y = 5638 psi	
YOUNG'S MODULUS	E = 3.48 E+06 psi	(Elastic Range)
TANGENT MODULUS	E_T = 98381.87 psi	(Plastic Range)

Ref. : MANTECH FOR ADVANCED DATA/SIGNAL PROCESING (VHSIC)

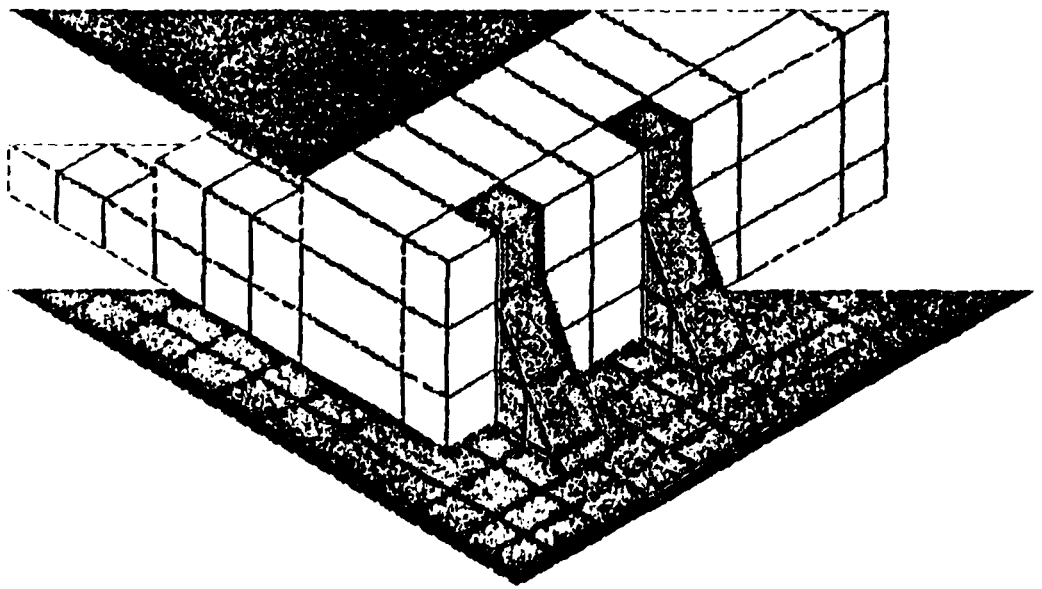
STRESS STRAIN DATA FOR 63-37 SOLDER

Ref. : MANTECH FOR ADVANCED DATA/SIGNAL PROCESSING(VHSIC)



TEMP.	YIELD STRESS σ_y, psi	YOUNG'S MOD. E, psi	TANGENT MODULUS (Plastic) E_T, psi
- 55 ^{0}C	5638	3.48 E+06	98381.87
+ 24 ^{0}C	3875	3.62 E+06	323.60
+ 105^{0}C	1900	3.62 E+06	12297.73

NOTE:
From the table only E_T, the Tangent Modulus, at -55^{0}C and +105^{0}C are used for analysis. E_T at +24^{0}C seems to be wrong and was discarded. Instead, E_T at +24^{0}C as well as σ_y and E at -55^{0}C, +24^{0}C and +105^{0}C are taken from the Westinghouse test data(Ref. Hermetic Chip Carrier Compatible PWB, Report No. AFWAL-TR-85-4082).



16LCC; SMT SOLDER JOINT; 1/8TH MODEL

ANSYS 4.4
APR 26 1990
08:18:01
PREP7 ELEMENTS
TYPE NUM

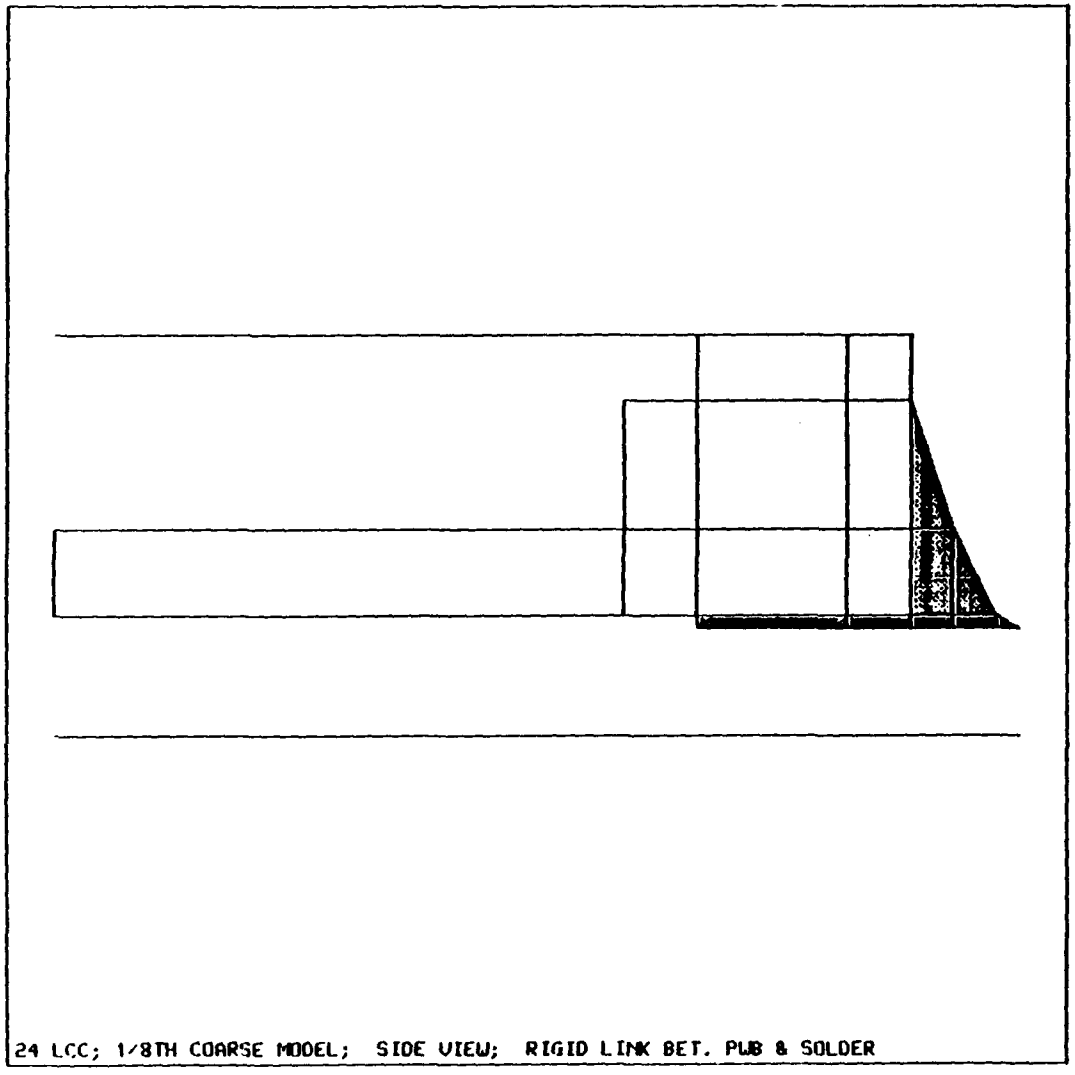
XV =1
YV =1
ZV =1
DIST=0.136118
XF =0.0875
YF =0.0415
ZF =-0.0875
CENTROID HIDDEN

eplot

PRODUCE ELEMENT PLOT IN DSYS = 0
PREP7 -INP=

DS6

DS7

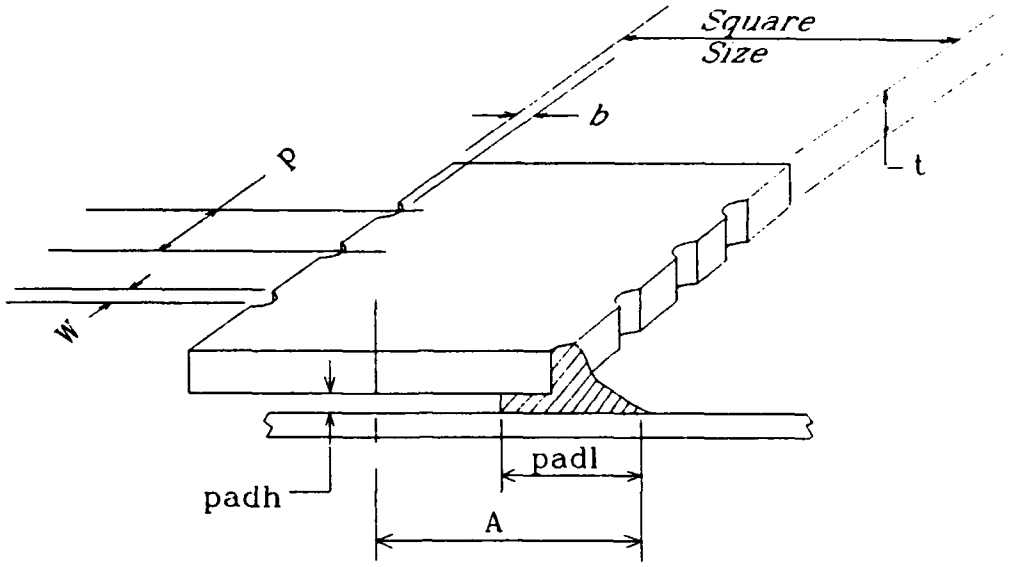


ANSYS 4.4
JAN 16 1990
14:28:55
PREP7 ELEMENTS
TYPE NUM

ZV =1
DIST=0.12375
XF =0.1125
YF =0.0465
ZF =-0.1125
CENTROID HIDDEN

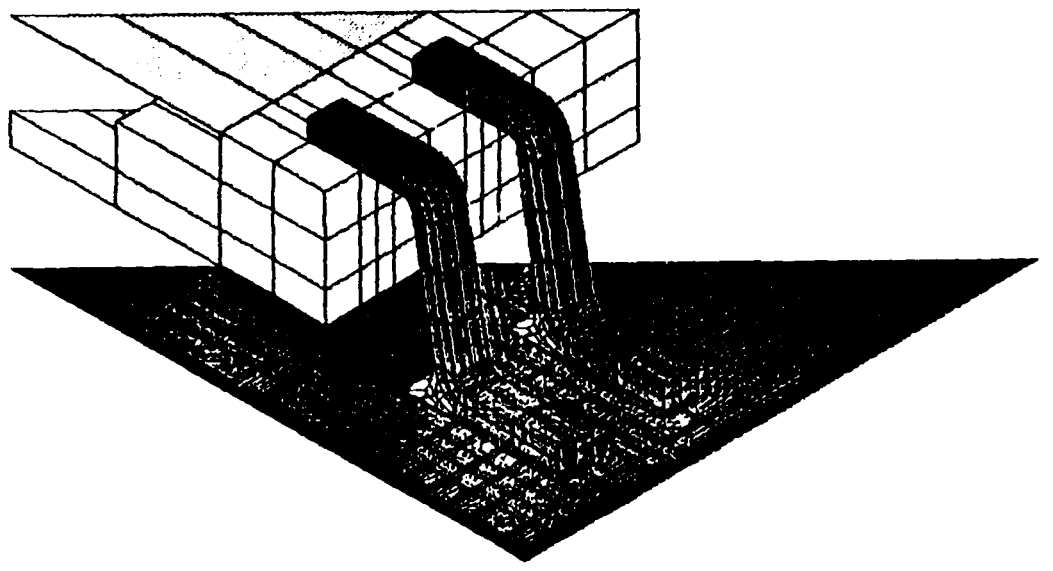
EPLOT

PRODUCE ELEMENT PLOT IN DSYS = 0
PREP7 -INP=



	P	Square Size	A	W	b	t	padl	padh
16 LCC	50 MIL PITCH	0.30	.175	.016	.015	.055	.075	.003
	25 MIL PITCH	0.30	.175	.008	.008	.055	.075	.003
24 LCC	50 MIL PITCH	0.40	.225	.016	.015	.065	.075	.003
	25 MIL PITCH	0.40	.240	.008	.008	.065	.075	.003
32 LCC	50 MIL PITCH	0.50	.275	.016	.015	.065	.075	.003
	25 MIL PITCH	0.50	.275	.008	.008	.065	.075	.003
68 LCC	50 MIL PITCH	950	.515	.016	.015	.065	075	.003
	25 MIL PITCH	.950	.515	.008	.008	.065	.075	.003

PACKAGE DIMENSIONS USED FOR ANSYS ANALYSIS



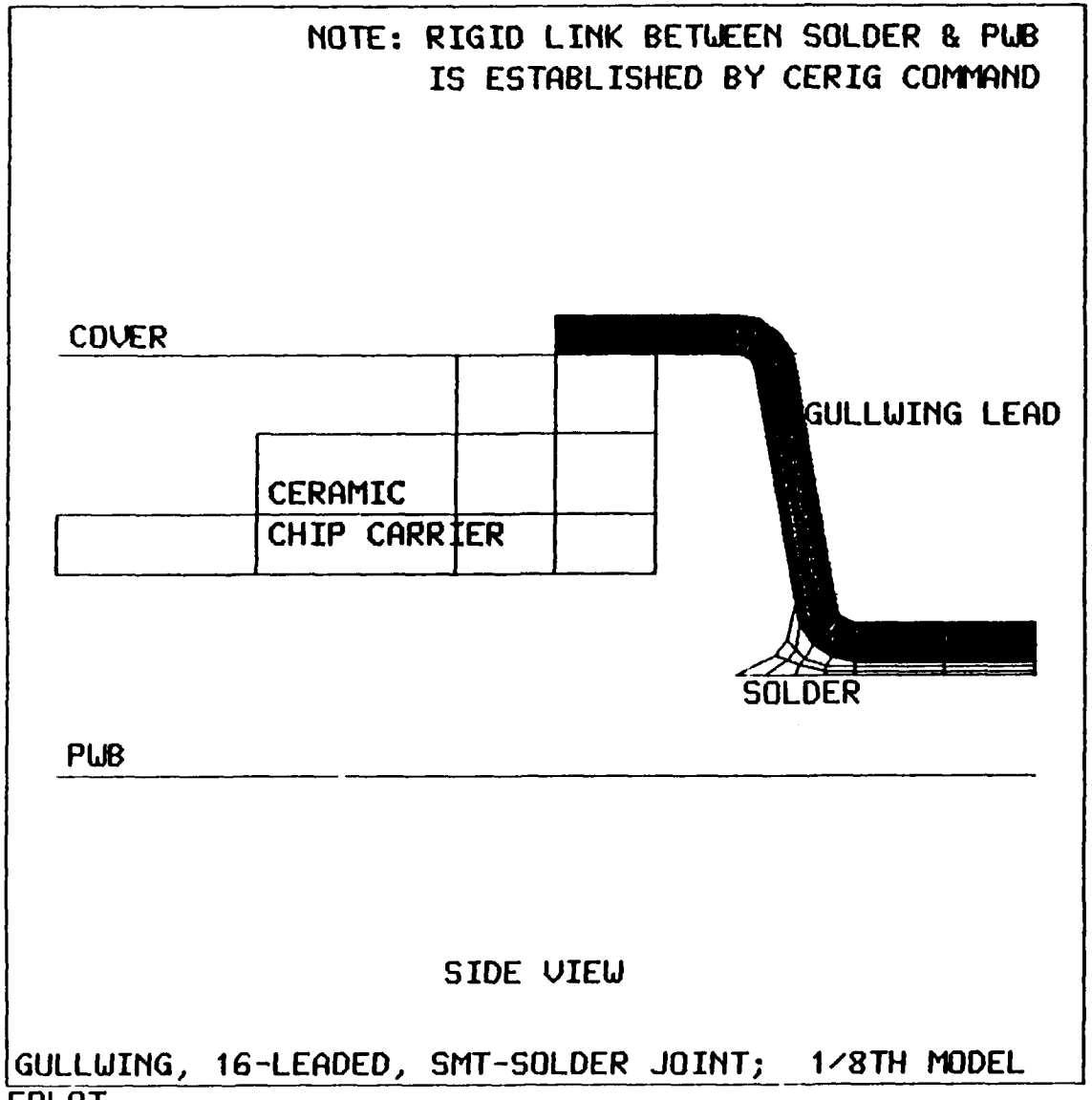
GULLWING, 16-LEADED, SMT-SOLDER JOINT; 1/8TH MODEL

```
 ANSYS  4.4
APR  3 1990
14:53:13
PREP7 ELEMENTS
TYPE NUM

XV  =1
YV  =1
ZV  =1
DIST=0.190565
XF  =0.1225
YF  =0.0575
ZF  =-0.1225
CENTROID HIDDEN
```

```
EPLOT

 PRODUCE ELEMENT PLOT IN DSYS =    0
 PREP7 -INP=
```



ANSYS 4.4
APR 3 1990
14:16:13
PREP7 ELEMENTS
TYPE NUM

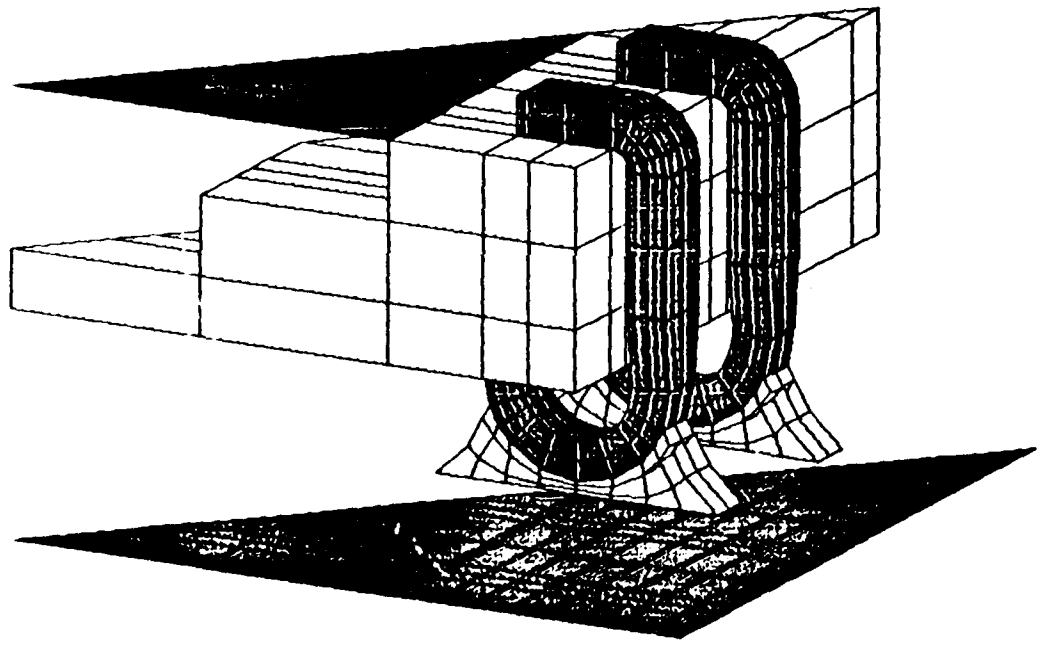
ZV =1
DIST=0.13475
XF =0.1225
YF =0.0575
ZF =-0.1225
CENTROID HIDDEN

EPLOT

PRODUCE ELEMENT PLOT IN DSYS = 0
PREP7 -INP=

DS10

NOTE: RIGID LINK IS ESTABLISHED BETWEEN
PWB & SOLDER BY "CERIG" COMMAND



J-LEAD; 16-LEADED SMT SOLDER JOINT; 1/8TH MODEL

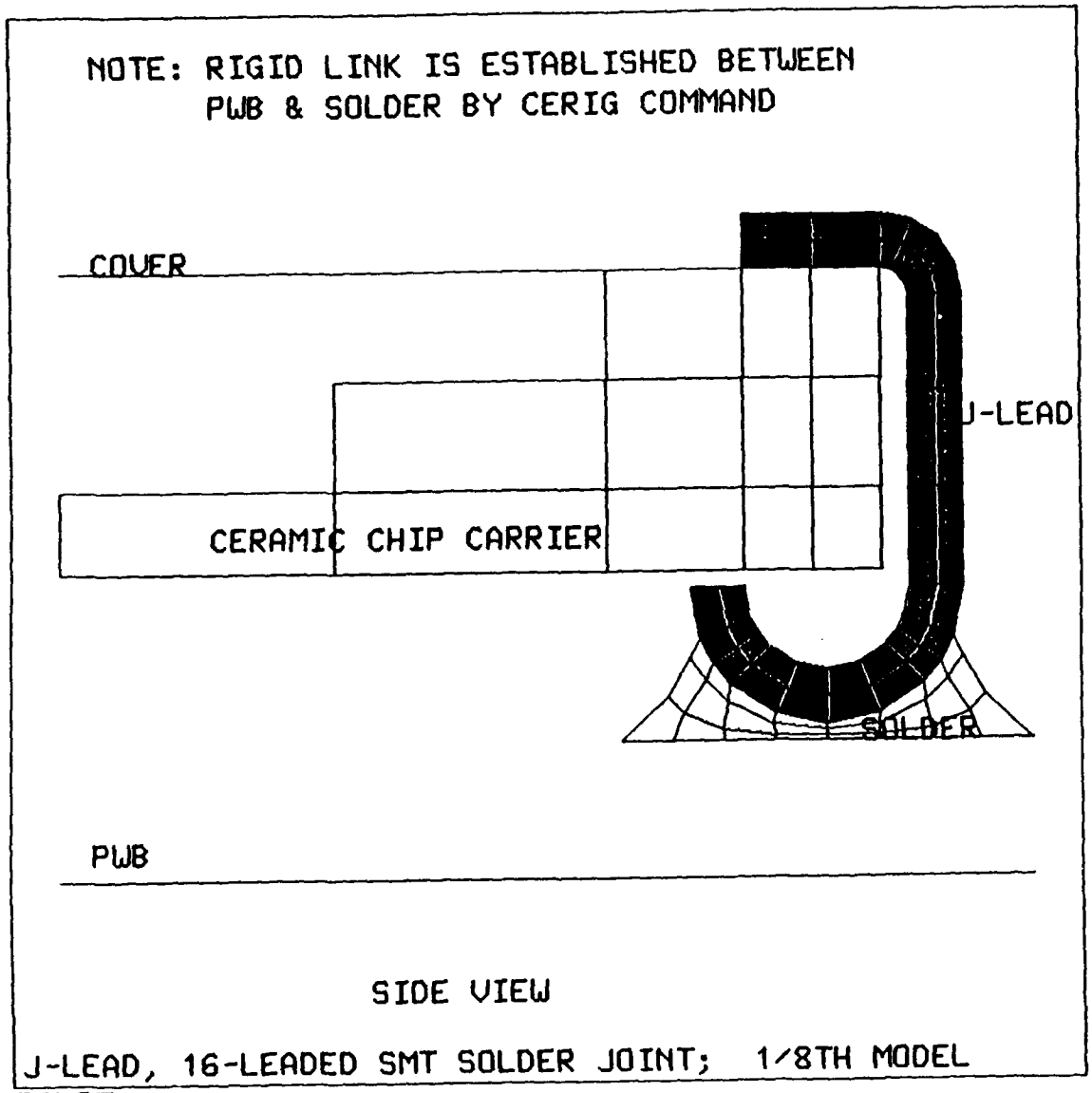
ANSYS 4.4
APR 12 1990
08:43:39
PREP7 ELEMENTS
TYPE NUM

XV =0.8
YV =0.5
ZV =1.5
DIST=0.132081
XF =0.08875
YF =0.0605
ZF =-0.08875
CENTROID HIDDEN

DS11

EPLOT

PRODUCE ELEMENT PLOT IN DSYS = 0
PREP7 -INP=



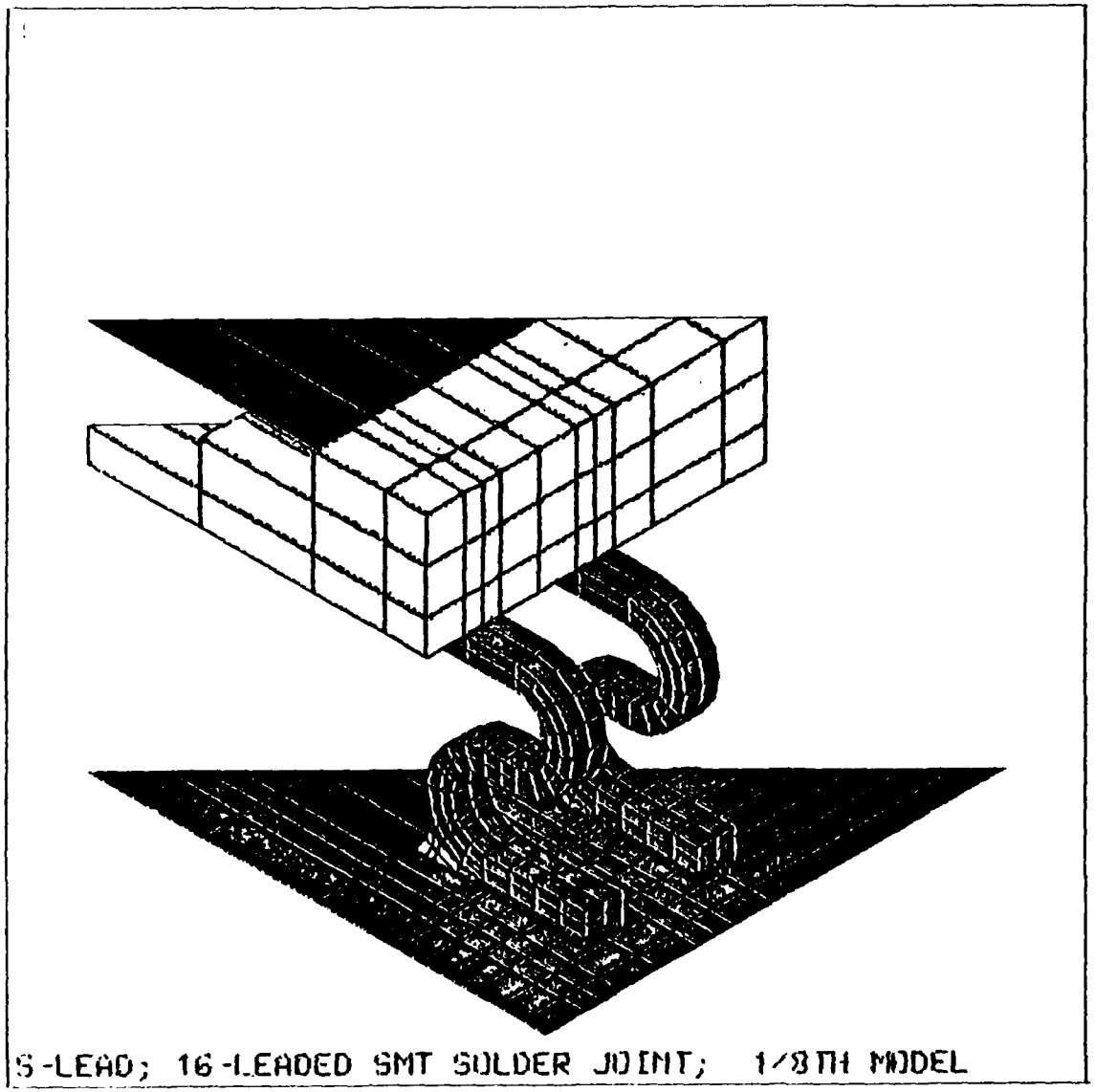
ANSYS 4.4
APR 11 1990
15:34:53
PREP7 ELEMENTS
TYPE NUM

ZV =1
DIST=0.097625
XF =0.08875
YF =0.0605
ZF =-0.08875
CENTROID HIDDEN

EPLOT

PRODUCE ELEMENT PLOT IN DSYS = 0
PREP7 -INP=

DS12



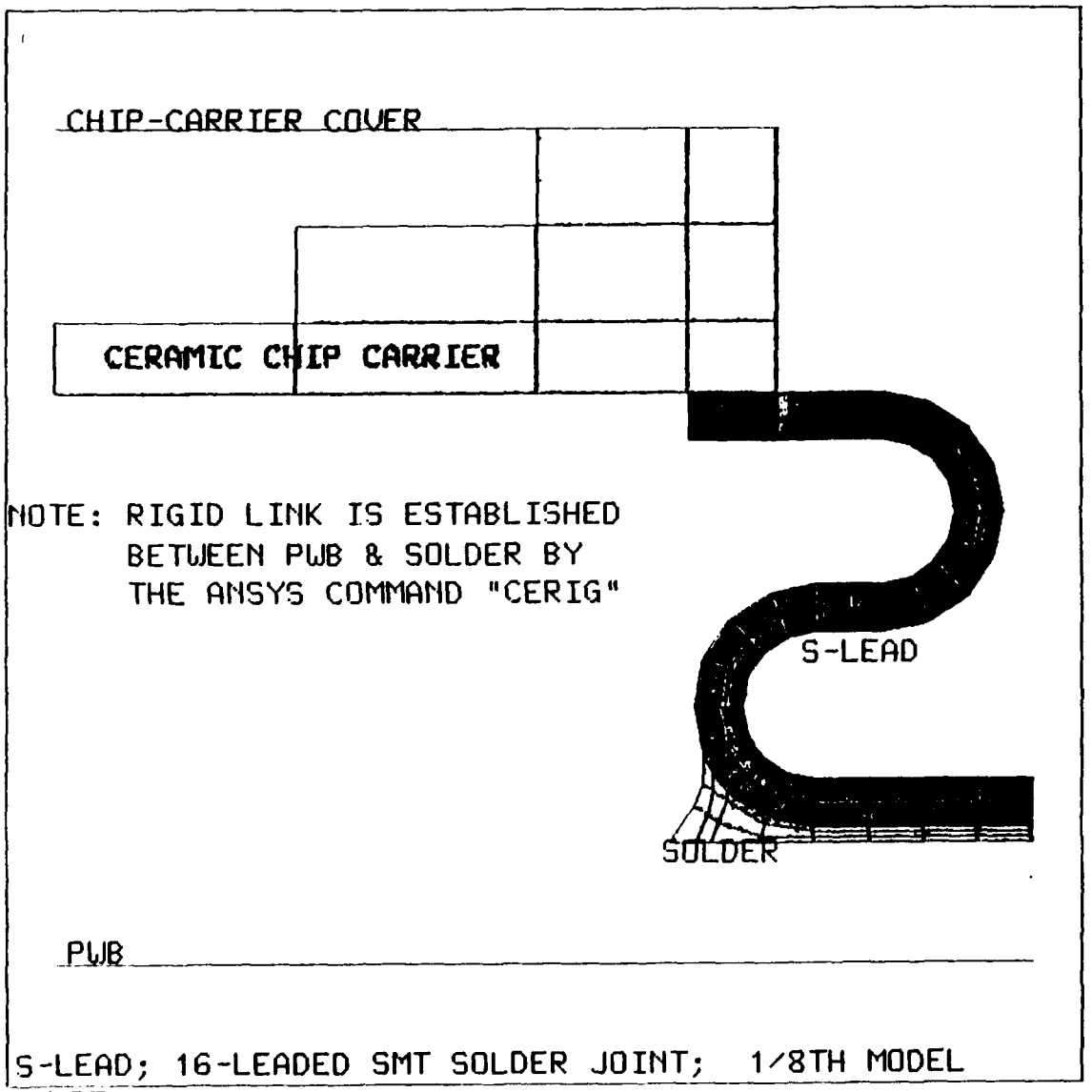
ANSYS 4.4
APR 16 1990
15:18:20
PREP7 ELEMENTS
TYPE NUM

XV =1
YV =1
ZV =1
DIST=0.168627
XF =0.10125
YF =0.0865
ZF =-0.10125
CENTROID HIDDEN

PREP7 -INP=

PREP7 -INP=

DS13



ANSYS 4.4
APR 16 1990
13:56:31
PREP7 ELEMENTS
TYPE NUM

ZV =1
DIST=0.111375
XF =0.10125
YF =0.0865
ZF =-0.10125
CENTROID HIDDEN

DS14

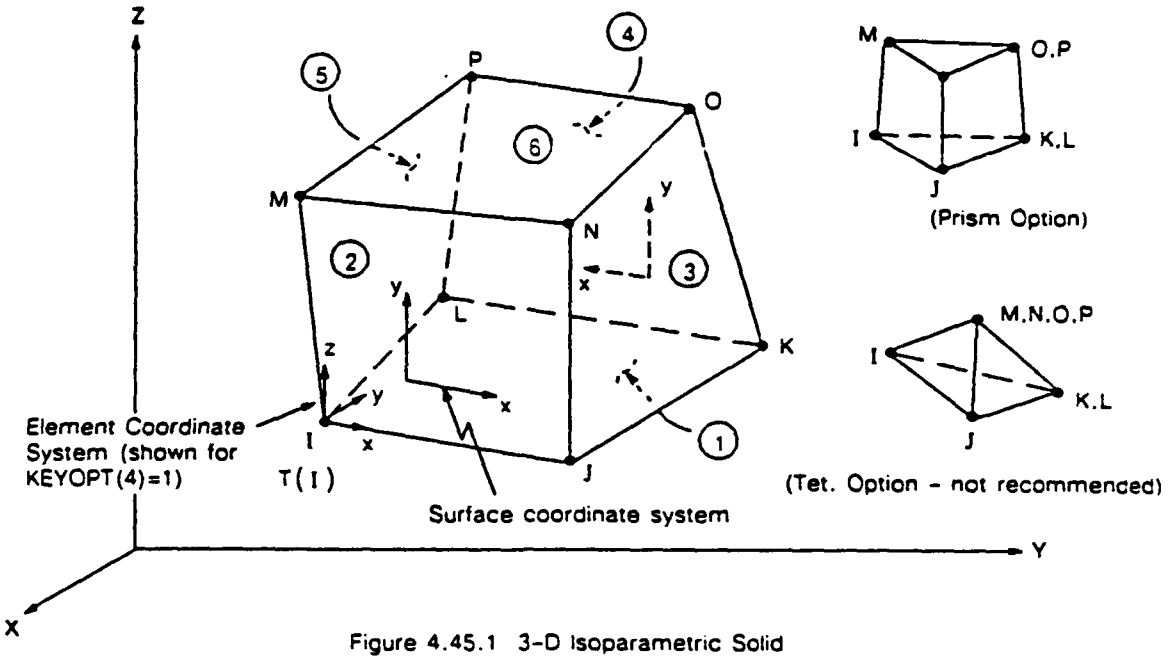
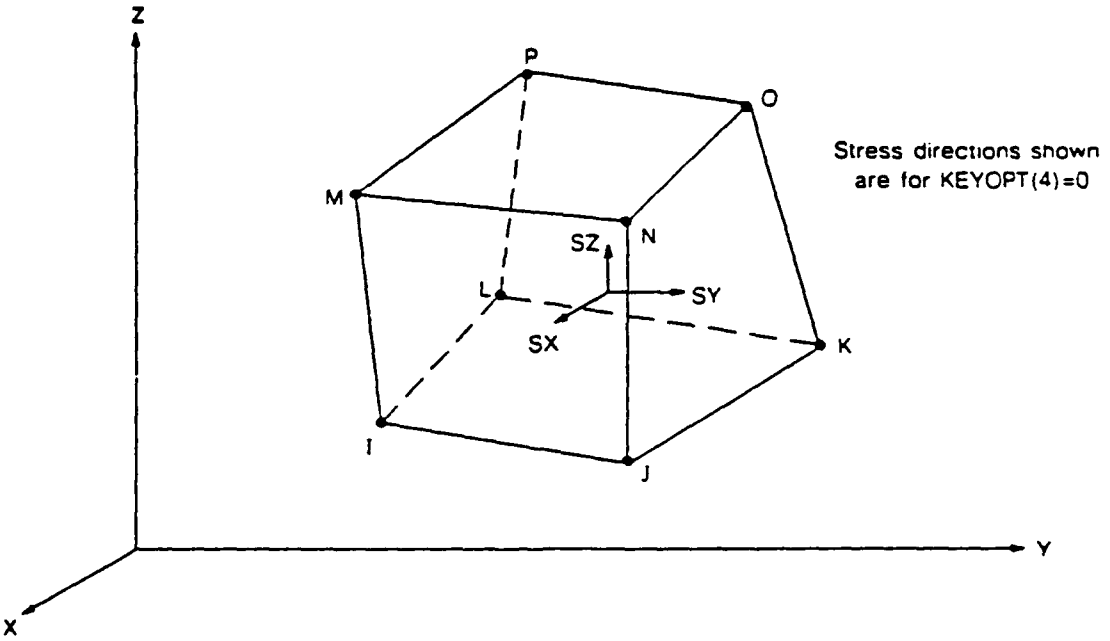
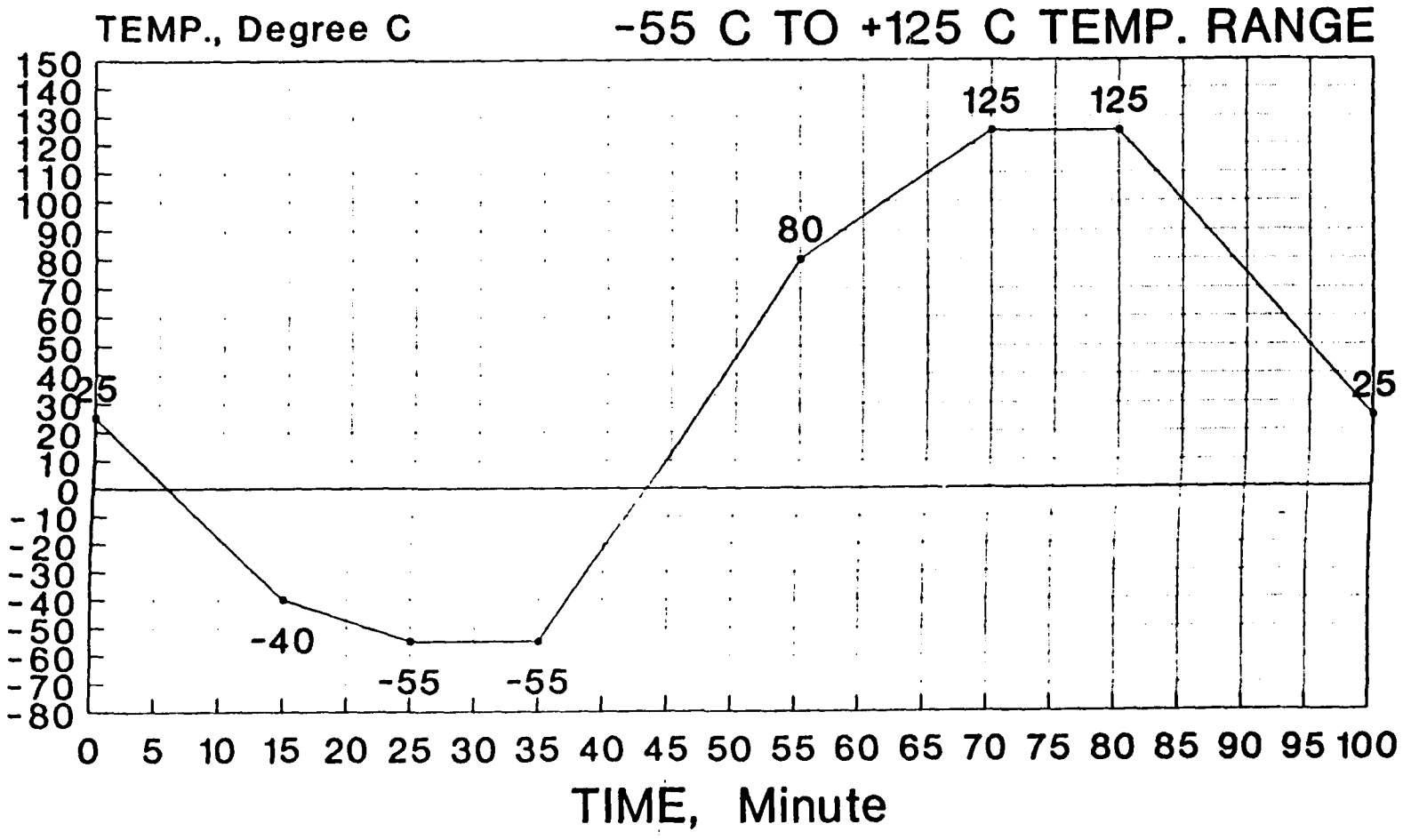


Figure 4.45.1 3-D Isoparametric Solid



3-D Isoparametric Solid Output

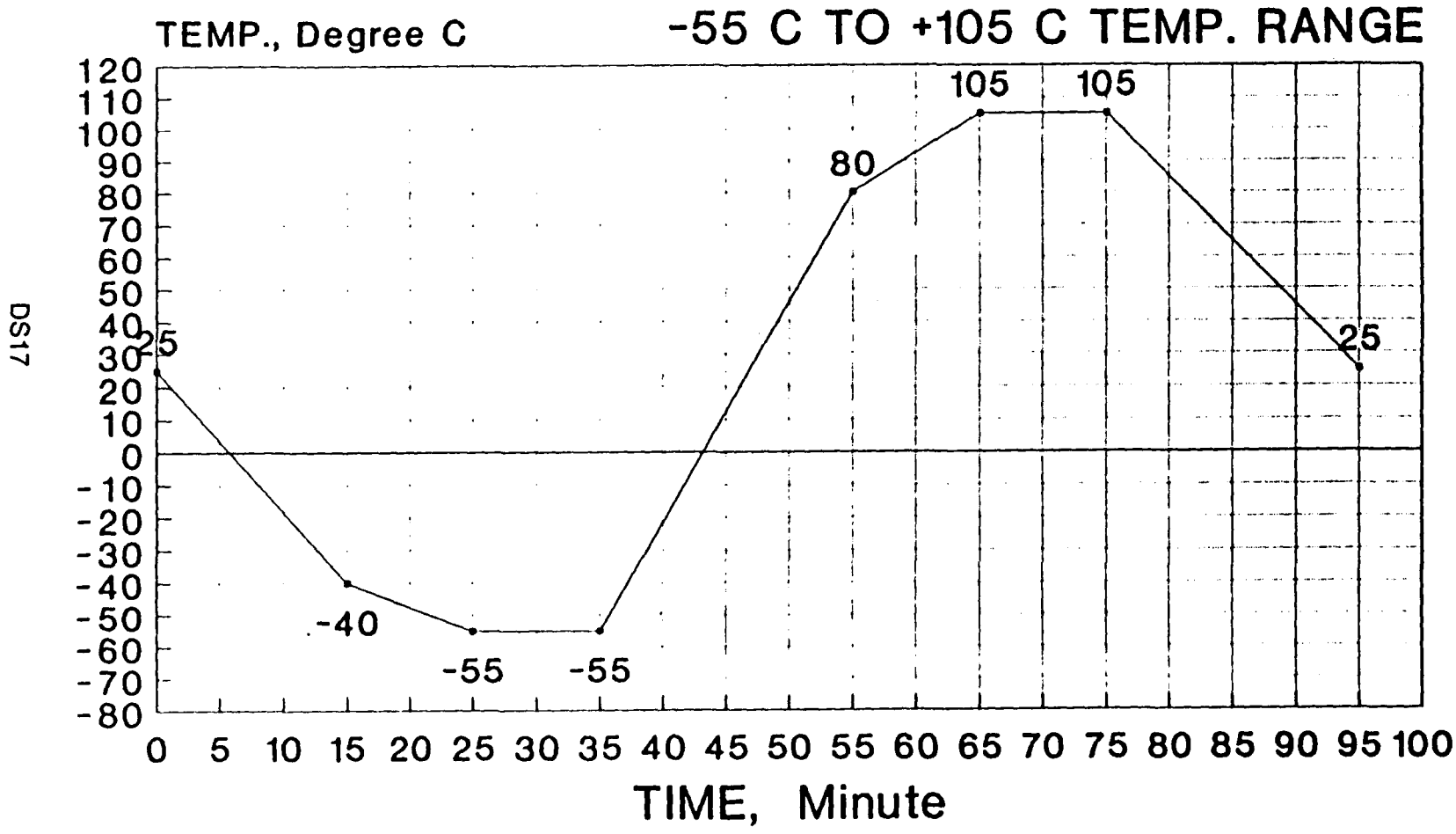
THERMAL CYCLE PROFILE
SOLDER RELIABILITY ANALYSIS



DS16

THIS IS NOT CHAMBER TEMP. PROFILE. THIS IS THE INPUT TO ANSYS ANALYSIS OF SOLDER JOINT OF LEADLESS & LEADED CHIP CARRIERS

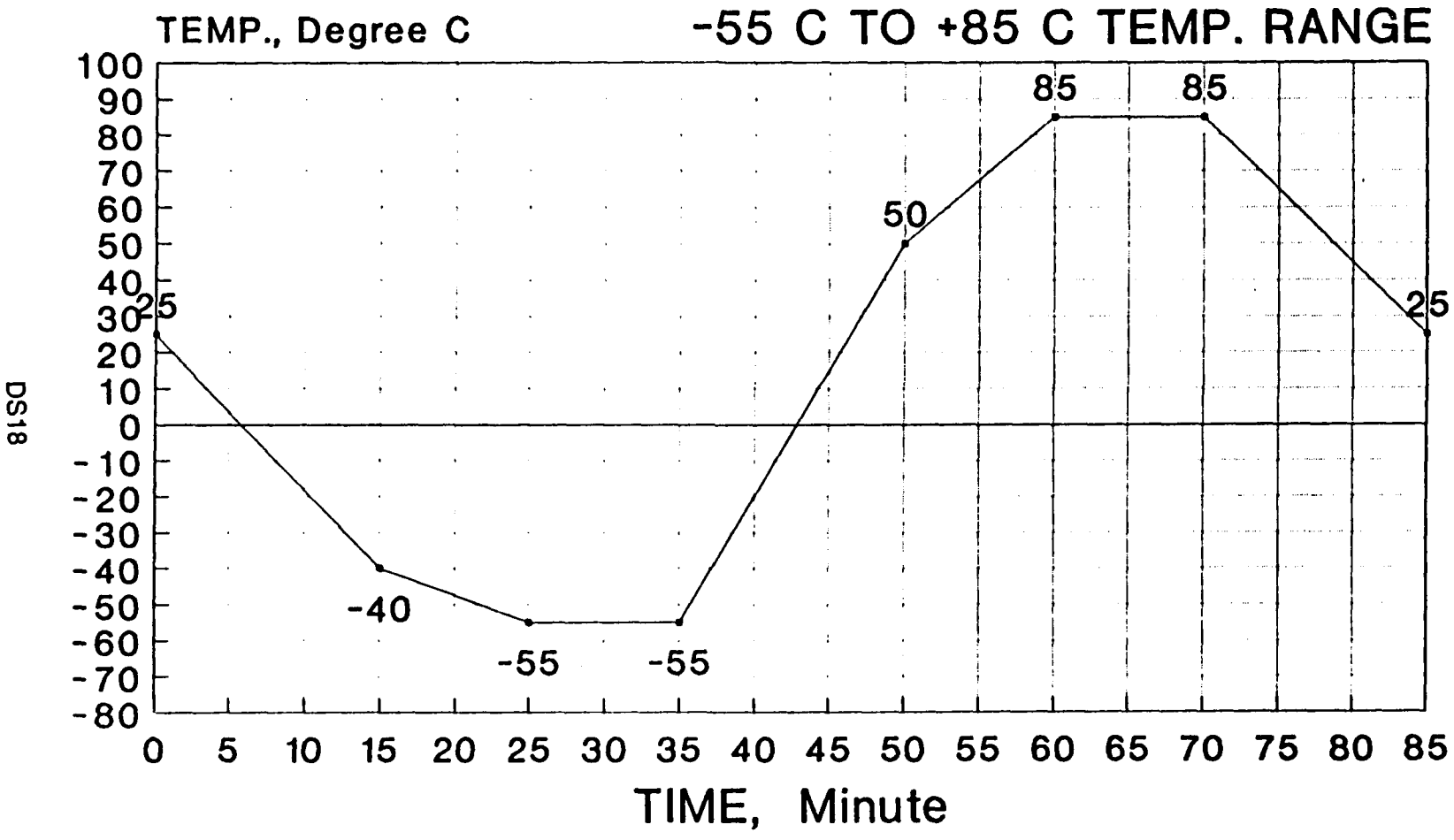
THERMAL CYCLE PROFILE
SOLDER RELIABILITY ANALYSIS



DS17

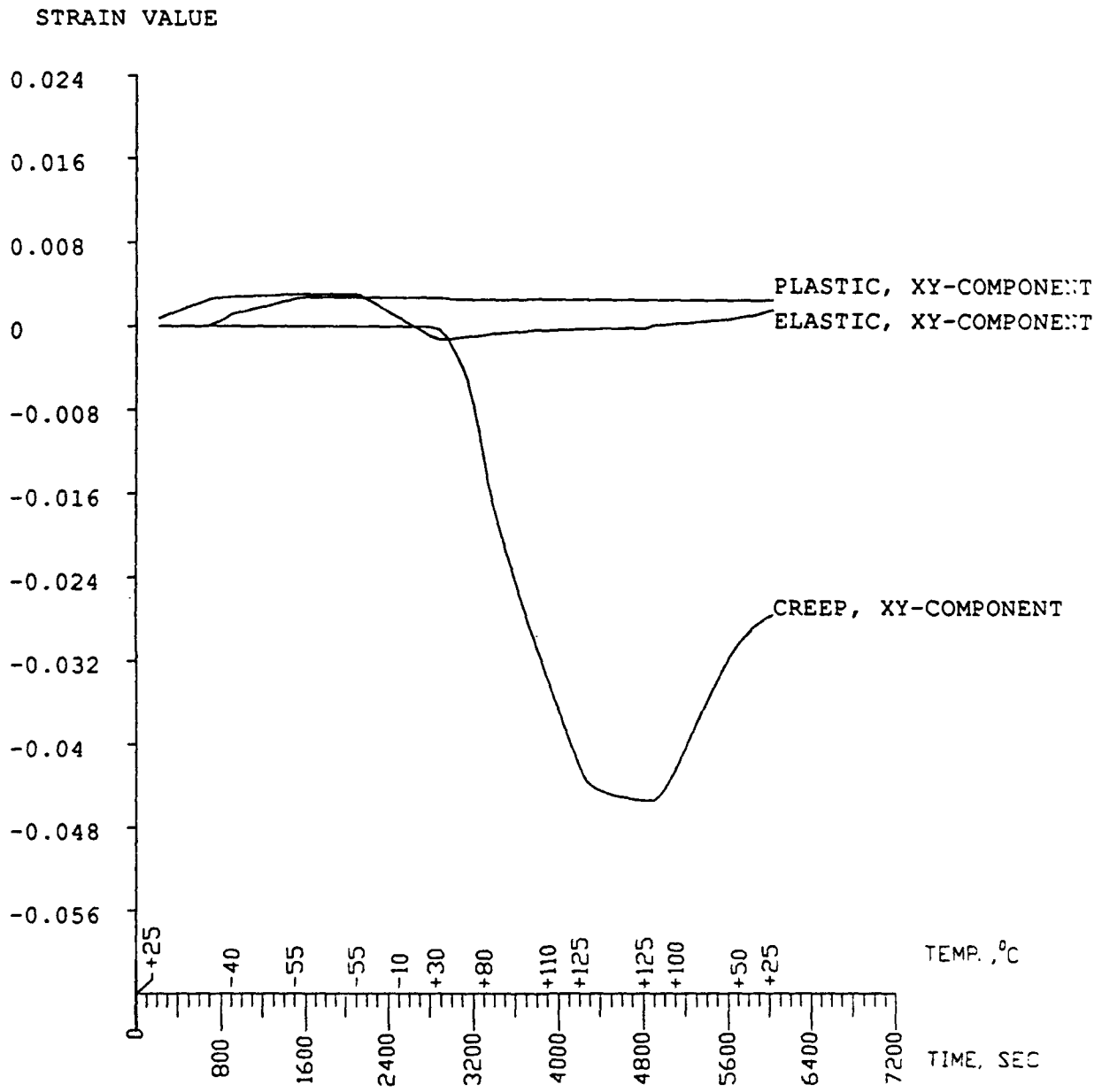
THIS IS NOT CHAMBER TEMP. PROFILE. THIS IS THE INPUT TO ANSYS ANALYSIS OF SOLDER JOINT OF LEADLESS & LEADED CHIP CARRIERS

THERMAL CYCLE PROFILE
SOLDER RELIABILITY ANALYSIS

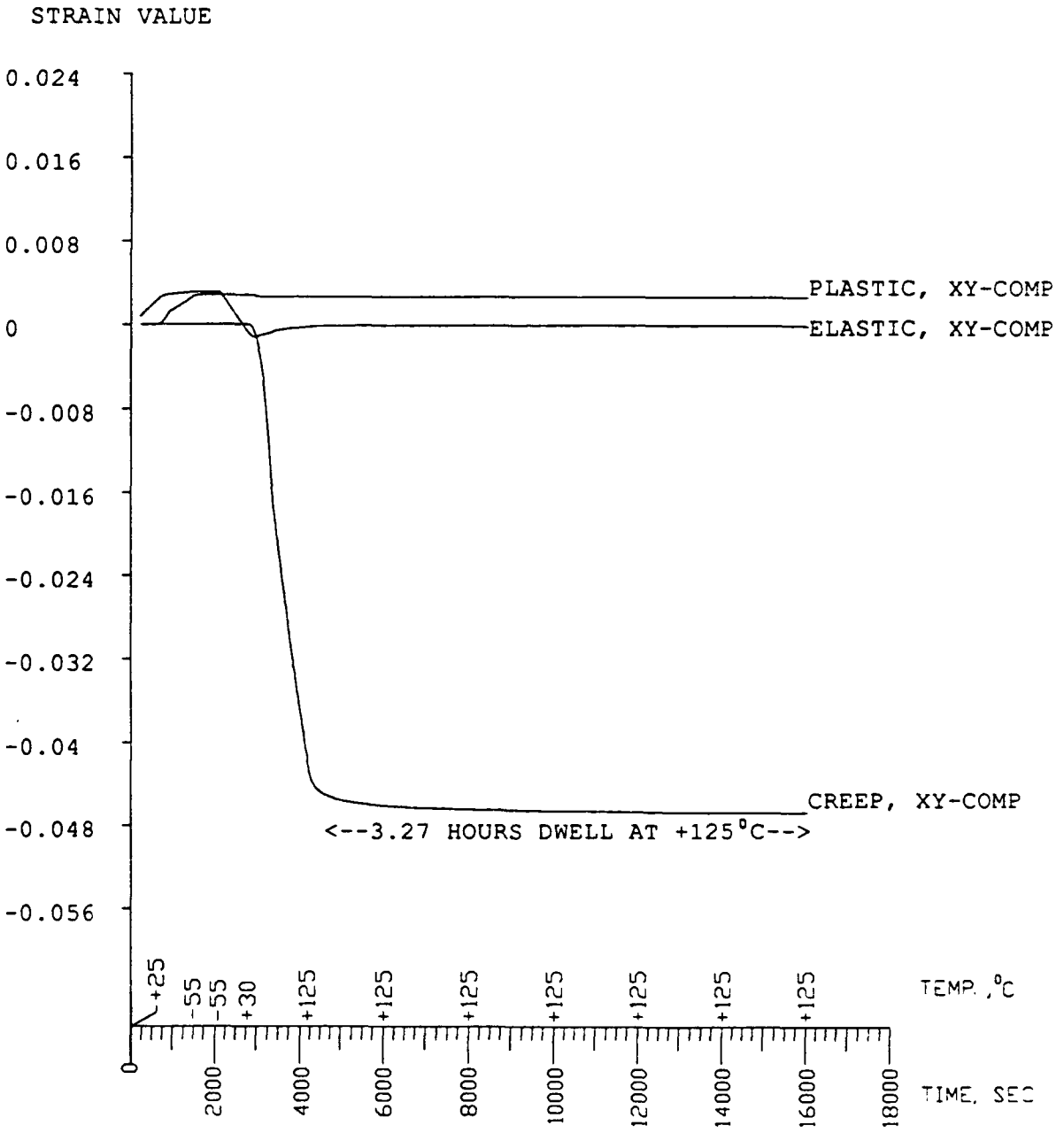


DS18

THIS IS NOT CHAMBER TEMP. PROFILE. THIS IS THE INPUT TO ANSYS ANALYSIS OF SOLDER JOINT OF LEADLESS & LEADED CHIP CARRIERS



A TYPICAL FEA RUN STARTS AT ROOM TEMPERATURE AND RUNS NEGATIVE TO LOW END DWELL OF 10 MINUTES THEN RAMPS UP TO HIGH END DWELL FOR 10 MINUTES AND RETURNS TO ROOM TEMPERATURE.



THIS RUN DUPLICATES THE TYPICAL FEA RUN EXCEPT THAT A PROLONGED HOLD OCCURS AT THE HIGH END. THE SIGNIFICANCE IS THAT THE CREEP STRAIN IN THE PROLONGED HOLD IS NOT SIGNIFICANTLY DIFFERENT FROM A SHORT DWELL.

APPENDIX E

LETTER ON RELIABILITY TO MIL-STD-2000 INDUSTRY WORKING GROUP

HARRIS

April 9, 1990

Hughes Aircraft
P.O. Box 11337
B807C8
Tucson, AZ 85734

ATTENTION: Mr. Jerry Rosser

Jerry,

Per your request, I am sending you information about solder joint reliability. Due to time constraints, I only touched the surface. If you need more information or details, please let me know.

The majority of "verified failures" on military hardware is component failures or EOS. This is supported by various studies.

SOLDER JOINT FAILURES DO OCCUR ON MILITARY HARDWARE. In fact, some electronics have MANY FAILURES due to solder joints. However, these failures are typically design oriented or from improper processes. Solder joint defects capable of causing failure generally need to be very gross. I support the Acceptance Criteria Field Study (FS) conclusions that 2-5% of all failures are probably solder joints. The Naval Fleet Assessment (NFA) had similar data, 6% of the defects that were documented were considered to be high risk solder joints. This is supported by other studies as well. I also feel that 2-5% of the field failures due to solder joints is too high. On one program at Harris, solder joint failures at functional testing was 23 ppm. In the field, the solder joint failure rate is 0.2 ppm.

As the NFA and FS studies show, "PERFECT" solder joints on 100% of the connections do not occur. The inherent noise in visual inspection also allows escapes and variability in our quality assurance efforts. PROPER design allows for these typical manufacturing and quality variances to occur without causing field failures.

I thought it would be of benefit if I identified known problems. I marked them with a "F" if I knew they had caused a failure. The label "P" is for the following:

1. Caused failure in accelerated life testing.
2. Caused crack or a potential future failure mechanism; but did not fail at time of review.
3. Know it has caused problems; however, I'm not sure if it was an actual field failure.

SOLDER JOINT FAILURES

1.	F	Gold - pth; 1950's; excessive Au plating.
2.	F	SMD; - SMD; FS
3.	F	Residual stress in solder (flatpacks); GIDEP, company.
4.	F	Circuitry adhesion; 50-60's, Wild, FS, DeVore.
5.	F	Single-sided SJ - liter.
6.	F	Epoxy conformal coat under glass component - liter.
7.	F	Sn whiskers - military.
8.	F	Plating (organics) on component leads - Wild, DeVore.
9.	P	Gross insufficient - J leads; Engelmaier.
10.	P	Dendritic growth of plating salts through blowholes - Keller.
11.	P/F	Nonwetts.
12.	P	Side-brazed CERDIPS - Wild, company, FS
13.	F	Non-soldered.
14.	P	Heavy unsupported component
15.	F	Mishandling of fine wires by repair tech.
16.	P	SMD voids - f (size, fillet, location, porosity); Millard, DeVore, SRI
17.	F	EOS; liter.
18.	F	ESD; liter.
19.	F	Oxidized/corroded connectors.
20.	P	J-leads butt up against component body.
21.	P	Lead trim on tempered leads; company.
22.	F	Icicles, peaks, holes - "skin effect hardware".
23.	F	Corrosion of part.
24.	P	Vias with high aspect ratios.
25.	P	Component tilt (canting); LCC's; Gull Wing - Millard, DeVore, ManTech, Wild
26.	P	Non-uniformity; LCC.
27.	P	Gross measling - power supplies.
28.	P	DIP lead bent under component body with no top fillet - company.

A concern I have is applying inspection criteria for all board designs and applications. Some defects are more of a concern on special hardware or components. For example,

- Icicles, points, peaks on RF circuitry.
- Measling on power supplies.
- Lead trim on tempered leads.

Also, rarely is the combination of defects considered. A good example of this was addressed in the Field Study - insufficient solder. Accelerated Life Testing (ALT) studies show that insufficient solder can be 25% or less and not affect reliability if completely wetted on pths. However, a combination of 25% solder fill and poor wetting will no longer be a reliable connection. (This is one of the reasons why the field study team choose 75% solder fill on pths)

Basic essentials for solder joint reliability:

1. Proper Design:
   MIL-STD-2000 has come a long way here with SMT. One concern I have is that many accelerated life studies does not include or document typical manufacturing anomolies. New technology requires some type of ALT to ensure proper design.

2. Proper Process:
   Field failures can be attributed to processes but not found by our inspection technique/criteria (plating organics, residual stress in solder, etc). Continued process control is required to prevent these failures.

3. Solder Joint Attributes:
   With proper design and continual process control, only critical defects will affect reliability and need to be reworked. The rest should be identified as process control indicators. I think many of the current Level B process indicators have little use as process indicators. Many of the Level A defects don't affect reliability until they are very gross.

High Risk Attributes:

Non-soldered.
Bridging.
Non-wetting (>90° contact angle)
Fractured/cracked.
DISTURBED (gross).
Solder balls/splatter - loosely adhered on the PCB.
Soluble, ionic flux.
Any conductive element beyond electrical clearance.
Gross insufficient (≐ 50% pth; <25% SMD f(design)).
Partially filled via.
Heavy, unsupported components.
Gold on SMD's.
Lead trim on tempered leads.
Any attribute that affects "current" electrical integri
wrong part, wrong orientation, missing part, etc....
Non-uniformity - SMD leadless.
Canting (excessive) - leadless.

All other variances, should be documented as process indicators. Many more should be included than the curren: I B Table.

Other process indicators should go to dispositioning be determining if they should be not reworked or reworked. For example measling on power supplies.

If I can be of more help, please feel free to contact m 407/727-6329.

Sincerly,

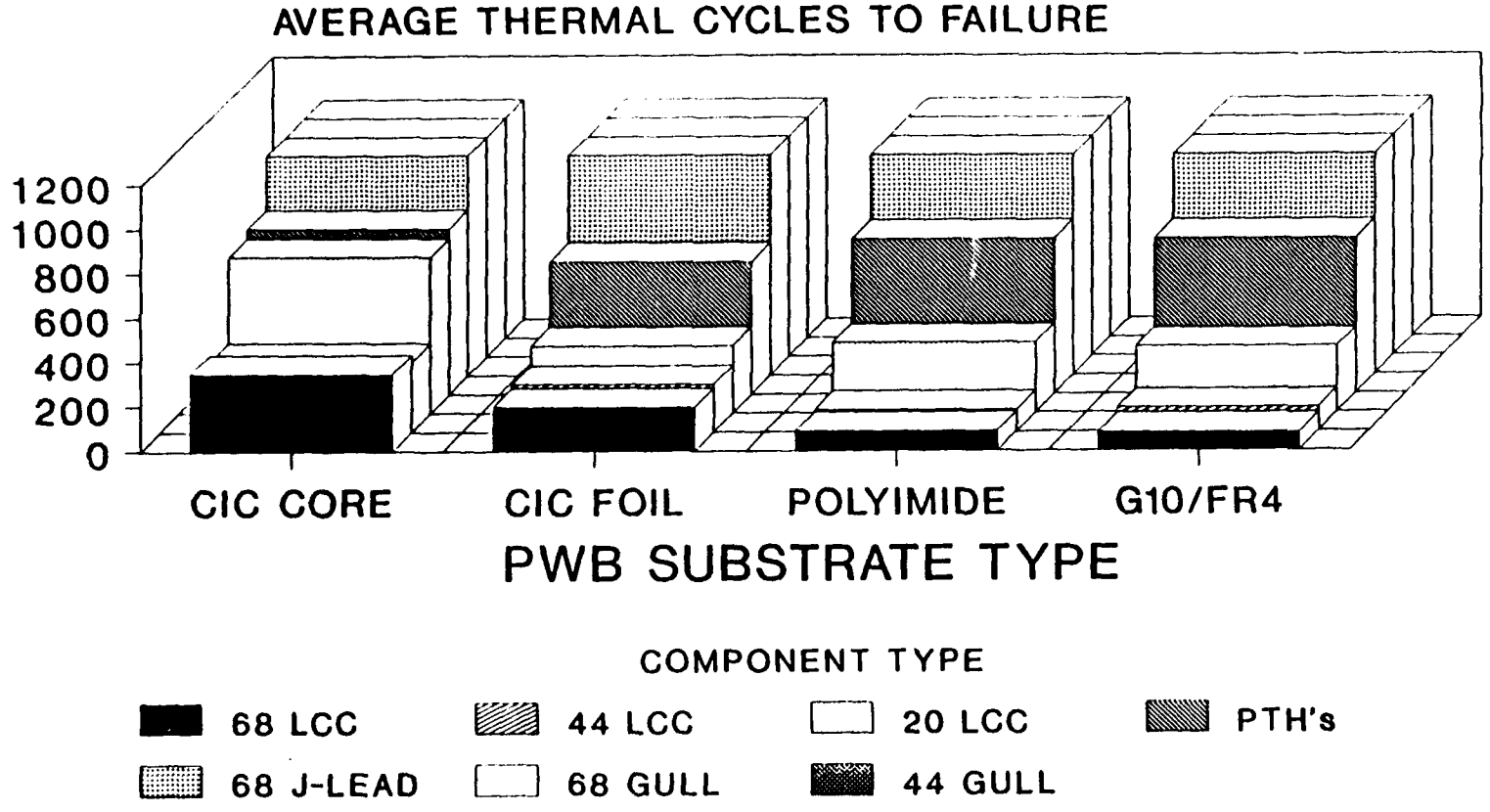
Jon R. Maki
Lead Engineer, AMT

APPENDIX F

TEST DATA

Test data is a key ingredient in developing predictive formulae for solder joint life expectancy. The following Appendix includes data from a HARRIS in-house reliability study and from the industry studies.

HARRIS SMT STUDY
THERMAL CYCLE LIFE DATA



TESTING STOPPED AT 1000 CYCLES.
ONLY HIGH ASPECT RATIO PTH FAILURES
ON G10/FR4 AND POLYIMIDE ASSEMBLIES

5th Interim Technical Report

"SOLDER FILLER METAL DEVELOPMENT FOR ELECTRONIC CHIP CARRIERS"

Contract No. F33615-84-C-5047
Project No. F41457-84-01074

15 FEB, 1987

By--- Westinghouse Defense and electronics center
Development and Operation Center
Baltimore, Maryland

For---Air Force Syst. Command
Wright-Patterson AFB
Ohio, 45433

Failure Criteria : 0.5 milliohm resistance increase(after 14th cycle) @ +125°C

Temp. Range : -55°C to +125°C
Cyclic Rate : 13 Cycles/day

Board Material : Polyimide/Quartz; 0.033" Thick, CTE = 9.4 x 10^6ppm/ °C
Heat Sink : 0.03" thick 430 Stainless Steel

TEST SUMMARY

DEVICES WERE WERE SOLDERED TO ONLY TOP SIDE BOARD(Heat sink betwween boards)

DEVICE TYPE	BOARD MATERIAL	CYCLES /DAY	TEMP. RANGE	NO. OF CYCLES TO FAILURE	NO OF DEVICES
LCC; 84/0.05	Polyimide/quartz	13	-55°C to +125°C	200,275,275	3
LCC; 68/0.05				340,350,360	3
LCC; 44/0.05				350,350	2

DEVICES WERE WERE SOLDERED TO BOTH TOP SIDE BOARD & BOTTOM SIDE BOARD

DEVICE TYPE	BOARD MATERIAL	CYCLES /DAY	TEMP. RANGE	NO. OF CYCLES TO FAILURE	NO OF DEVICES
LCC; 84/0.05	Polyimide/quartz	13	-55°C to +125°C	125,160,160, 170,200,200 ;	6
LCC; 68/0.05				250,250,200, 175,190,190 ;	6
LCC; 44/0.05				225,275, ,275	4

CTE MISMATCH = PWB CTE - CERAMIC CTE
= (9.4 - 6.5)x10^6ppm/°C ; G.E. Ceramics, Inc. (94% Al_2O_3)
= 2.5 x10^6ppm/°C

"A SOLUTION TO SOLDER JOINT FAILURE IN LEADLESS CERAMIC CHIP CARRIERS"

By -- T.A. Krinke and D.K. Pai
Control Date Corporation
Government System Manufacturing
Box 609, 3101 E. 80th Street
Minneapolis, MN 55440

Failure Criteria : Not specified ; Cycles to 1st. crack initiation ?

Temp. Range : $-54^{o}C$ to $+100^{o}C$
Cyclic Rate : 16 Cycles/day

Board Material : Polyimide/Glass, 10 layer; CTE =(11-13)x 10^{6}ppm/ ^{o}C
Heat Sink : Yes

TEST SUMMARY

DEVICE TYPE	BOARD MATERIAL	CYCLES /DAY	TEMP. RANGE	NO. OF CYCLES TO FAILURE	NO. OF DEVICES
LCC; 32/0.05	Polyimide/glass 10 Layers	16	-54 C to +100 C	112; Uncoated	?
LCC; 20/0.05				250; Uncoated	?
LCC; 20/0.05 & 32/0.05				10Z-50Z Higher ; Coated	?
GULL; (172/0.025)	"	"	"	No Failure upto 1000 Cycles.	?
"J" (Top Brazed)	"	"	"	No Failure upto 1000 Cycles.	?
"S" Lead C17410 Cu (Be 0.3Z, Co 0.5Z, rest Cu)	"	"	"	No Failure upto 1000 Cycles for all devices 20/0.05 to 68/0.05	

CTE MISMATCH = PWB CTE - CERAMIC CTE
= (13 - 6.5)x10^{6}ppm/^{o}C ;
= 6.5x10^{6}ppm/^{o}C

"SOME FACTORS AFFECTING LEADLESS CHIP CARRIER SOLDER JOINT FATIGUE LIFE" By------ Wild, R.N. ; IBM

TEST SUMMARY Note: Readings were taken from graphs

DEVICE TYPE	BOARD MATERIAL	CYCLES	TEMP. RANGE from to	NO. OF CYCLES TO FAILURE min.	max.	NO. OF DEVICES
LCC; 20 Pin	EPOXY-GLASS			250	650	8
LCC; 28 Pin	Hard bonded to 0.1" Thick aluminum frame.		-55°C to	100	400	6
LCC; 44 Pin		20		50	225	6
LCC; 68 Pin	CTE(Epoxy-glass) =21 ppm/°C		+125°C	20	50	6
LCC; 84 Pin				10	20	6
LCC; 20 Pin	EPOXY-KEVLAR			1250		8
LCC; 28 Pin	Soft bonded to 0.1" Thick aluminum frame.		-55°C to	750		6
LCC; 44 Pin		20		350	825	6
LCC; 68 Pin	CTE(Epoxy-Kevlr) =10 ppm/°C		+125°C	175	250	6
LCC; 84 Pin				150	200	6
LCC; 20 Pin	EPOXY-KEVLAR			>2000		8
LCC; 28 Pin	Soft bonded to 0.1" Thick aluminum frame.		-55°C to	1500		6
LCC; 44 Pin		12		750	1400	6
LCC; 68 Pin	CTE(Epoxy-Kevlr) =10 ppm/°C		+100°C	350	450	6
LCC; 84 Pin				300	400	6
LCC; 20 Pin	EPOXY-KEVLAR			>2000		6
LCC; 28 Pin	Soft bonded to 0.1" Thick aluminum frame.		-55°C to	>2000		6
LCC; 44 Pin		12		1000	1600	6
LCC; 68 Pin	CTE(Epoxy-Kevlr) =10 ppm/°C		+100°C	650	900	6
LCC; 84 Pin	Silicone confor-mal coating			650	825	6

60/40 solder; standard solder paste screening; Vapor phase reflow;
12 Copper layer board (0.08" thick); No LCC standoff;
Normal standoff height of LCC from board = 0.001" to 0.003"

By--- Hughes Aircraft Company
Ground Systems Group
Fullerton, Ca.

For--- U.S. Army Missile Command
Redstone Arsenal
Alabama 35898

TEST SUMMARY

DEVICE TYPE	BOARD MATERIAL	CYCL /DAY	TEMP. RANGE	NO. OF CYCLES TO FAILURE min.	max.	NO. OF DEVICES
LCC; 20/0.04	POLYIMIDE-GLASS			60	80	50
LCC; 20/0.05	Ablefilm 504 to bond to 0.05" Cu plate.		-65°C to	200	300	50
LCC; 44/0.05	CTE(Poly-Glass)	24		40	60	60
LCC; 84/0.04	=11-13 ppm/°C		+125°C	20	40	40
LCC; 84/0.05	=17.6 for copper			20	40	48
LCC; 84/0.05	POLYIMIDE-GLASS			20; Reinforced corners; No undercoat; Cu sink		6
LCC; 84/0.05	Ablefilm 504 to bond to 0.05" Cu or CIC plate.		-65°C to	200; Reinforced corners; Undercoated; Cu sink		12
LCC; 84/0.05	CTE(Poly-Glass)	24		20; No reinforcement; No undercoat; Cu sink		6
LCC; 84/0.05	=11-13 ppm/°C		+125°C	20; No reinforcement; Undercoated; Cu sink		48
LCC; 84/0.05	=17.6 for copper			Package cracked w/all joints reinforced and undercoated; Cu sink		12
LCC; 84/0.05				20; CIC sink;No undercoat double sided assy.		12
LCC; 84/0.05				20; CIC sink; Undercoat; double sided assy.		12
LCC; 84/0.05				20; CIC sink;No undercoat Single sided assy.		6
LCC; 84/0.05				20; CIC sink; Undercoat; Single sided assy.		6

EPON 828 used for reinforcement.

"PRINTED WIRING BOARDS UTILIZING LEADLESS COMPONENTS"-Final Report, Dec.,1983

Contract DAAH-01-82-C-0482
Project 3263

By--- Hughes Aircraft Company
Ground Systems Group
Fullerton, Ca.

For--- U.S. Army Missile Command
Redstone Arsenal
Alabama 35898

TEST SUMMARY

DEVICE TYPE	BOARD MATERIAL	CYCL /DAY	TEMP. RANGE	NO. OF CYCLES TO FAILURE min. max.	NO. OF DEVICES
LCC; 20/0.04	POLYIMIDE-KEVLAR PWB			600 -700; Undercoated; Cu sink;	50
LCC; 20/0.05	Ablefilm 504 to bond to 0.05" Cu 0.04" CIC. plate.		-65°C to	1000 - 1100; Cu sink	50
LCC; 44/0.05		24		200; Undercoated; Cu sink;	60
LCC; 84/0.04	CTE(Poly-Kevlar) = 6 ppm/°C		+125°C	Package fractured in 20 cycles. Cu sink.	60
LCC; 84/0.05	=17.6 for copper			Package fractured in 20 cycles. Cu sink.	72
LCC; 84/0.05				400 -500; CIC sink; Undercoated.	12
LCC; 84/0.05				300 - 400; CIC sink; No undercoat.	12
LCC; 84/0.05				400 - 500; CIC sink; Novel PWB with Kavlar paper (Hove 743)	24

0.062" PWB thickness; 8-10 mil bondline;

MISSION

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