(2)

RL-TR-92-11
Final Technical Report
February 1992

ADVANCED TECHNOLOGY COMPONENT DERATING

Westinghouse Electronic Systems Group

Timothy A. Jennings

Rome Laboratory
Air Force Systems Command
Griffiss Air Force Base, NY 13441-5700

This report has been reviewed by the Rome Laboratory Public Affairs Office (PA) and is releasable to the National Technical Information Service (NTIS). At NTIS it will be releasable to the general public, including foreign nations.

RL-TR-92-11 has been reviewed and is approved for publication.

APPROVED: Timothy J. Donovan

TIMOTHY J. DONOVAN
Project Engineer

FOR THE COMMANDER: John J. Bart

JOHN J. BART, Chief Scientist
Reliability Sciences

If your address has changed or if you wish to be removed from the Rome Laboratory mailing list, or if the addressee is no longer employed by your organization, please notify RL(ERSR) Griffiss AFB, NY 13441-5700. This will assist us in maintaining a current mailing list.

Do not return copies of this report unless contractual obligations or notices on a specific document require that it be returned.

REPORT DOCUMENTATION PAGE

Form Approved
OMB No. 0704-0188

1. AGENCY USE ONLY (Leave Blank)	2. REPORT DATE	3. REPORT TYPE AND DATES COVERED
	February 1992	Final Jun 89 - Sep 91

4. TITLE AND SUBTITLE
ADVANCED TECHNOLOGY COMPONENT DERATING

5. FUNDING NUMBERS
C - F30602-89-C-0095
PE - 62702F
PR - 2338
TA - 02
WU - 4G

6. AUTHOR(S)
Timothy A. Jennings

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)
Westinghouse Electronic Systems Group
Friendship Site
Box 746
Baltimore MD 21203

8. PERFORMING ORGANIZATION REPORT NUMBER
N/A

9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)
Rome Laboratory (ERSR)
Griffiss AFB NY 13441-5700

10. SPONSORING/MONITORING AGENCY REPORT NUMBER
RL-TR-92-11

11. SUPPLEMENTARY NOTES
Rome Laboratory Project Engineer: Timothy J. Donovan/ERSR/(315) 330-2608

12a. DISTRIBUTION/AVAILABILITY STATEMENT
Approved for public release; distribution unlimited.

12b. DISTRIBUTION CODE

13. ABSTRACT (Maximum 200 words)

This report has been prepared to summarize the technical study performed to determine the derating criteria of advanced technology components. The study covered existing criteria from AFSC Pamphlet 800-27 and the development of new criteria based on data, literature searches and the use of advanced technology prediction methods developed in RADC-TR-90-72. The devices that were investigated were: VHSIC, ASIC, MIMIC, Microprocessor, PROM, Power Transistors, RF Pulse Transistors, RF Multi-Transistor Packages, Photo Diodes, Photo Transistors, Opto-Electronic Couplers, Injection Laser Diodes, LED, Hybrid Deposited Film Resistors, Chip Resistors and Capacitors and SAW devices. The results of the study are additional derating criteria that extend the range of AFSC Pamphlet 800-27. These data will be transitioned from the report to AFSC Pamphlet 800-27 for use by government and contractor personnel in derating electronics systems yielding increased safety margins and improved system reliability.

14. SUBJECT TERMS	15. NUMBER OF PAGES
Reliability, VHSIC, Galium Arsenide (GaAs), Failure Rate, Derating	198
	16. PRICE CODE

17. SECURITY CLASSIFICATION OF REPORT	18. SECURITY CLASSIFICATION OF THIS PAGE	19. SECURITY CLASSIFICATION OF ABSTRACT	20. LIMITATION OF ABSTRACT
UNCLASSIFIED	UNCLASSIFIED	UNCLASSIFIED	UL

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

LIST OF ILLUSTRATIONS (continued)

LIST OF TABLES

LIST OF TABLES (continued)

1.0 EXECUTIVE SUMMARY

1.1 OBJECTIVE

The objective of this effort was to develop and publish new derating criteria so that the reliability of new upcoming and modified designs will be enhanced. Stress derating parameters were needed for advanced components such as VHSIC (very high speed integrated circuits), MIMIC (microwave/millimeter wave monolithic integrated circuits), GaAs FET (gallium arsenide field effect transistor), and photonic devices since the current standards were lacking guidance. The new standards will be used by hardware design contractors and will serve as the basis for an update of AFSC Pamphlet 800-27, "Part Derating Guidelines." The complete parts list for which updated stress derating criteria was to be developed is shown in table 1-1.

Table 1-1 Parts List

VHSIC ASIC MIMIC Microprocessor PROM - ultra-violet erasable - electrically erasable - electrically alterable - avalanche induced migration Power Transistor - silicon - GaAs - MOSFET	RF Pulse Transistor RF Multi-transistor Package Photo Transistor Photo Diode Opto-electronic Coupler Injection Laser Diode LED Hybrid Deposited Film Resistor Chip Resistor Chip Capacitor SAW

1.2 BACKGROUND

Part stress derating has long been established as an important element in enhancing system reliability. Derating is generally defined as the practice of limiting electrical, thermal and mechanical stresses on parts to levels below their specified or proven capabilities in order to provide a safety margin for operation and to improve system reliability. Most contractors have developed their own internal derating practices, but until recently, the DoD (Department of Defense) had no standard practices. RL recognized the need for standardizing this area. This standardization will provide guidance to those contractors without their own policies, indicate a means for invoking contractual derating requirements and create a benchmark against which other derating methods may be evaluated.

In keeping with the cost effective tailoring approach to reliability as defined in MIL-STD-785, "Reliability Programs for Systems and Equipment Development and Production," Boeing Aerospace (Seattle, WA) under contract to RL, divided derating criteria into three different criticality levels. The three level derating approach provides a means of tailoring as a function of mission criticality and severity of the end use environment. RL adapted the results of this study in the publication of AFSC Pamphlet 800-27, "Part Derating Guidelines." Further work on derating was performed by Martin Marietta (Orlando, FL) under contract to RL, which included development of an integrated circuit thermal measurement technique to verify derating. Both of these efforts precluded the development of derating factors for new parts designed since the studies were conducted.

While under contract to RL, Westinghouse recently completed the "Reliability Analysis/Assessment of Advanced Technology" (RA/AAT) study[1] with the intent of updating the microcircuit section of MIL-HDBK-217. With the availability of the stress-failure relationships developed as part of that study, as well as close working relationships with their suppliers and available field failure data, Westinghouse was selected to conduct this "Advanced Technology Component Derating" study.

1.3 APPROACH

Stress derating of advanced technology components is a critical step in the design of electronic systems which employ these components. Only by the increased lifetime advantage offered by stress derating can the system reliability requirement be realized when using advanced technology components in the system designer's intended application.

It was the intent of the authors of the revised AFSC Pamphlet 800-27 to maintain the spirit of the current version of the Pamphlet (hereafter referred to as "the Guidelines") and, at the same time, minimize unnecessary constraints placed on the designers of electronic systems by the derating criteria. These unnecessary constraints result from the application of generalized derating criteria intended to encompass all components within a specific component style in order to keep the guidelines simplified. It was believed that, unless the designer can employ derating criteria in his design with minimum difficulty, he will be reluctant to take the time necessary to apply the derating criteria properly. In this day of Total Quality, process streamlining and high speed design workstations, the designer is motivated to be proactive in all areas affecting his design. Therefore, in the formulation of the new stress derating criteria, a change in the derating criteria format is presented (for microcircuits), with the thought that the designer should, and would, know more about the components with which he was designing, and be more likely to design an optimum, reliable system by applying the appropriate stress derating criteria. The need for the change in the stress derating criteria format was a direct result of the logical approach taken to update the stress derating criteria, and the structure of the reliability models that describe the relationships between applied stresses and component failures.

It is recognized that the stress derating criteria outlined in the Guidelines is, by definition, a description of the maximum allowed stresses that may be applied to a component according to a specified mission

criticality level. It is also recognized that these maximum stresses result in a maximum component failure rate predicted by accepted reliability models. It is noted here that, at the time the current version of the Guidelines was released, the accepted reliability models were included in MIL-HDBK-217D Notice 1. Therefore, the authors of the current version of the Guidelines considered the maximum component failure rates, calculated using the reliability models of MIL-HDBK-217D Notice 1 and the maximum stress derating criteria outlined in the current version of the Guidelines, acceptable for a specified criticality level. A logical approach to updating this stress derating criteria would be to first calculate these acceptable maximum component failure rates at each criticality level. Then, the stress-failure relationships outlined in updated reliability models, such as those included in MIL-HDBK-217E Notice 1 and the RA/AAT study, may be evaluated such that new maximum stresses that result in these same maximum failure rates may be identified. These maximum stresses become the updated stress derating criteria.

This approach to updating the stress derating criteria has (at least) three benefits. First, the stress trade-offs performed to derive the new maximum stresses by evaluating the updated reliability models will identify the "sensitive" derating parameters in the model that, when varied, result in the largest changes in expected failure rate. Second, the approach provides a framework from which derating results can be easily communicated. That is, the concept of how changes in "failure rate" affect design reliability is more commonly understood among system designers and reliability engineers than how changes in "percent of rated value" affect design reliability. Third, the approach provides a basis for evolving the stress derating criteria into a "continuous" function of criticality rather than the currently accepted three levels of criticality. This benefit is expanded upon in a section near the end of this report.

This stress derating approach was applied to several classes of components. The approach was first successfully applied to microcircuits. Having just completed the Reliability Analysis/Assessment of Advanced

Technologies (RA/AAT) study, Westinghouse was intimately aware of those stress factors which directly influence the reliability of advanced technology microcircuits. From a study of the RA/AAT results, it was observed that microcircuit complexity was a "sensitive" derating parameter. Because of the impact that the complexity of the microcircuit has on its failure rate, part of the updated stress derating criteria was generated as simple one variable equations. The variable, of course, was complexity. For example, in the development of the stress derating criteria for MOS Digital ASIC/VHSIC components, the supply voltage derating criteria for criticality level I has the form

Supply Voltage = 129 / (G ** 0.320) volts

where G is the number of gates in the microcircuit. In some instances, the calculated derated stress was virtually independent of complexity. In that case, a constant derating value was substituted for the derating equation. Also, if the calculated derated stress was outside the region of validity of the reliability model, the value of the maximum stress identified in the model was substituted for the derating equation. For example, the maximum junction temperatures allowed for MOS Digital ASIC/VHSIC level III components, although dependent upon complexity, are above the junction temperatures recorded in the reliability data used in the development of the reliability model. Since 125 deg C was the maximum junction temperature identified in the reliability data, the maximum temperature of 125 deg C is substituted for the derating equation.

Other microcircuit derating parameters were not explicitly identified in the reliability models. These parameters, such as fanout and frequency, were considered design and application attributes which influenced the database from which the reliability models were developed. Therefore, the updated stress derating criteria for these parameters were developed from reviews of the literature, supplier information and other pertinent stress derating guidelines.

A similar stress derating method was used for silicon bipolar power transistors. Although the MIL-HDBK-217D Notice 1 reliability model for silicon bipolar power transistors was significantly different from the MIL-HDBK-217E Notice 1 reliability model, the approach used in the development of the microcircuit derating criteria could be applied to silicon bipolar power transistors. The difference between the microcircuit approach and the silicon bipolar power transistor approach was that the derating criteria for the power transistor was developed with equal weight applied to the stresses identified in the reliability model of MIL-HDBK-217E Notice 1. That is, the voltage derating and temperature derating for criticality level I must both be 65% of maximum rating so that the failure rate calculated using MIL-HDBK-217E Notice 1 would equal the failure rate calculated using MIL-HDBK-217D Notice 1 (4 FITS). The temperature derating was then transformed into temperature units with a value of 95 deg C (based on a 150 deg C maximum rating). For further details on this calculation, see section 6.1 on page 102.

Since reliability models for silicon power MOSFETs and GaAs power transistors were not available at the time the current version of the Guidelines were published, different approaches were taken to develop stress derating criteria for these devices.

For power MOSFETs, the stress derating criteria was developed by a thorough review of the literature and supplier surveys, and consensus of both military and industry stress derating guidelines. It was determined that the currently accepted derating policies are adequate in providing the margins of safety and success needed in the intended application.

The stress derating approach for GaAs power transistors was to collect reliability data, develop a stress-failure model and, assuming a maximum failure rate for each criticality level (provided by RL), calculate the maximum stresses allowed. This effort resulted in maximum channel temperatures of 85, 100 and 125 deg C for criticality levels I, II and III, respectively.

With the exception that a reliability model was developed on the RA/AAT study, the stress derating approach for GaAs MIMICs was similar to the approach for GaAs power transistors. The maximum channel temperatures for MIMIC devices were calculated to be 90, 130 and 150 deg C for criticality levels I, II and III, respectively.

It is noted here that, with the exception of the application notes, the silicon and GaAs RF pulse transistors are derated similarly to the silicon and GaAs power transistors since both silicon and GaAs RF pulse transistors must be able to dissipate as much power in pulse mode as the silicon and GaAs power transistors dissipate in continuous mode. GaAs power transistors (power MESFETs) are often used in RF pulse applications

Opto-electronic components presented a different challenge in developing updated stress derating guidelines. The differences between the reliability models of MIL-HDBK-217D Notice 1 and MIL-HDBK-217E Notice 1 resulted in up to several orders of magnitude difference in (improved) predicted failure rates. The quality factor had changed 2400% to 7000%, and the PiT factor of MIL-HDBK-217E Notice 1 utilizes an activation energy of approximately one third of the activation energy used in MIL-HDBK-217D Notice 1. The use of the silicon bipolar power transistor approach to stress derating would have resulted in virtually no stress derating required to meet the failure rates that were considered acceptable at the time the current version of the Guidelines was released. As an alternative approach, the development of updated "acceptable" failure rates for the three criticality levels was considered. The failure rates that can be obtained by applying currently accepted derating guidelines to the reliability models were deemed to be as "acceptable" as any other values chosen. Therefore, without having to do the failure rate calculations and the reverse stress analysis, the currently accepted guidelines become the updated stress derating criteria. A consensus of both military and industry stress derating guidelines was used in the development of this criteria.

There was apparently no change in the reliability models since MIL-HDBK-217D Notice 1 for the passive components evaluated, namely thick and thin film resistors, chip capacitors and SAW devices, and therefore only a consensus of military and industry guidelines was again used in the development of the stress derating criteria for these components.

To check if the expected results of applying stress derating criteria to the components identified in table 1-1 were obtained, a failure rate analysis was performed on available field failure data. The analysis was performed on field failure data provided by failure databases from the AN/APG-66 and AN/APG-68 radar programs and the ALQ-131 radar jammer program during the sorties flown in the 1988 and 1989 time period. It was discovered that the failure rates for PROM devices, power transistors, RF transistors, opto-couplers, LEDs and thin film chip resistors were close to or below the failure rate that would be expected when applying the stress derating criteria outlined in the current version of the Guidelines. Only thick film resistors and ceramic chip capacitors experienced failure rates significantly above expected failure rates. The most likely reason for this discrepancy is that these components often get removed as part of the rework for the suspected failure of another component. Since failure analyses are typically not performed on most of the components removed from systems, it is quite possible that some of the "failed" components are not truly failed. The calculated failure rates in this analysis would therefore be inflated. The results of this verification analysis are, in either case, most encouraging.

At the completion of this study, one concern is still left unresolved. The concern is that the designer is "locked in" to a level of derating criteria based on mission type of the whole system (SF, AUF or GF, for example) rather than the true component or board criticality. This concern prompted the authors of this study to include a section near the end of this report which outlines an alternate approach to implementing stress derating guidelines. The intent of this approach was to justify the reasonableness of imposing criticality level I guidelines on a criticality

level III mission design, and vice versa, depending as much upon system architecture as the safety and success of the mission. The possibility of evolving stress derating criteria into a "continuous" function of criticality is evaluated.

1.4 LIST OF ACRONYMS

The following is a list of the acronyms used in this report.

AFSC - Air Force Systems Command
APD - Avalanche Photo Diode
ASIC - Application Specific Integrated Circuit
ATCD - Advanced Technology Component Derating
CTR - Current Transfer Ratio
EEPROM - Electrically Erasable Programmable Read-Only Memory
EM - Electromigration
ESD - Electrostatic Discharge
eV - Electron Volt
FET - Field Effect Transistor
FMEA - Failure Modes and Effects Analysis
FPMH - Failures Per Million Hours
GaAs - Gallium Arsenide
ILD - Injection Laser Diode
JFET - Junction Field Effect Transistor
LED - Light Emitting Diode
MESFET - Metal Semiconductor Field Effect Transistor
MIL-HDBK - Military Handbook
MIMIC - Microwave/Millimeter Wave Integrated Circuit
MOS - Metal Oxide Semiconductor
MOSFET - Metal Oxide Semiconductor Field Effect Transistor
PROM - Programmable Read-Only Memory
RA/AAT - Reliability Analysis/Assessment of Advanced Technologies
RL - Rome Laboratory
RTOK - Retest Okay
SAW - Surface Acoustic Wave
SOA - Safe Operating Area
TDDB - Time Dependent Dielectric Breakdown
VHSIC - Very High Speed Integrated Circuit
VLSI - Very Large Scale Integration

2.0 REPORT ORGANIZATION

Section 3.0 presents the three approaches taken in the development of the updated stress derating criteria. Each approach is outlined briefly in this section with the details of the approaches provided in the following seven sections. No stress derating criteria is developed in this section.

Section 4.0, 5.0, 6.0, 7.0, 8.0, 9.0 and 10.0 discuss silicon microcircuits, MIMIC devices, power transistors, RF transistors, opto-electronic devices, passive components and SAW devices, respectively. Stress derating criteria and associated application notes are provided in each section for the relevant components in that section.

Section 11.0 presents a summary of the accumulated field failure data for the available component types outlined in table 1-1. A comparison of the predicted failure rate based on Level II criticality derating and the observed failure rate is made to verify the accuracy of the stress derating criteria.

Section 12.0 discusses an alternate approach to stress derating derived from observations made in the development of the updated stress derating criteria for this study.

Section 13.0 summarizes the results of the study and presents conclusions and recommendations for follow-on analysis.

Section 14.0 contains the bibliography of the literature used in part to develop the updated stress derating criteria.

Appendix A provides a comprehensive summary of the updated stress derating criteria and associated application notes.

Appendix B provides sample Fortran programs used in the development of stress derating criteria for microcircuits.

3.0 ADVANCED TECHNOLOGY COMPONENT DERATING

The development of stress derating criteria for advanced technology components requires a fundamentally sound understanding of the relationships between the electrical, thermal and mechanical stresses applied to the components and the resulting life distributions of the component populations. Component reliability models are used to describe these relationships and provide insight into the functional dependence of component life distributions on the applied stresses.

The magnitude of the stress derating determines the amount of expected change in component lifetime or shift in the life distribution of a population of components. In general the more the stress is derated, the longer the life of the component. Therefore, the expected result of derating the stresses applied to a component is to decrease its failure rate. Since most reliability models relate electrical, thermal and mechanical stresses to component lifetime in the form of a failure rate, it is reasonable to use the concept of failure rate as the key link between the reliability model and the stress derating criteria.

The minimum acceptable stress derating depends upon the criticality of the mission. Criticality levels referenced to mission safety and success, as outlined in the current version of the Guidelines, can be established and contrasted in terms of failure rates. The minimum acceptable stress derating for each criticality level sets the maximum failure rate that might be experienced by the component in a mission of specified criticality. It is reasonable to maximize the stress derating, when possible, to provide a greater than minimum margin of safety and success.

The definitions of the criticality levels used in the updated version of the Guidelines are consistent with the current version of the Guidelines. It is noted, however, that the formulation of the updated stress derating criteria is driven by the component failure rates associated with each criticality level and not solely the definitions of criticality.

Criticality Level I (Maximum Derating). Used with equipment whose failure would substantially jeopardize the life of personnel, would seriously jeopardize the operational mission, or would require repairs that are infeasible or economically unjustified, or used when extremely high operational readiness requirements are specified. Level I derating is considered those stress levels below which further reliability gain is small or at which further derating will create design problems that are unacceptable. This level is intended for the most critical applications in which design difficulty can be justified by the reliability requirement.

Criticality Level II. Used with equipment whose failure would degrade the operational mission or would result in unjustifiable repair costs, or used when high operational readiness requirements are specified. Level II derating is considered still in the range in which reliability gains are rapid as stress is decreased. However, achieving designs with these reductions in allowed stress is significantly more difficult than at level III.

Criticality Level III. Used with equipment of lesser criticality than level I or II, namely, equipment whose failure may not jeopardize the operational mission or that can be quickly and economically repaired. Level III derating is that stress level reduction that causes minor design difficulties and yet generates a large incremental reliability gain. The large reliability gain is realized since the effects of stress increase greatly as the absolute maximum rating is approached.

Supplemented by updated stress-failure data provided by three sources, namely, a thorough review of the literature, evaluation of available field data and component supplier surveys, the component reliability models developed on the RL "Reliability Analysis/Assessment of Advanced Technologies" (RA/AAT)[1] and "Reliability Prediction Models for Discrete

Semiconductors"[169] studies provided a starting point for the development of the updated stress derating criteria for several of the component types identified in table 1-1. For those component types not covered by current reliability models, stress derating criteria was developed from either reliability models generated from accumulated life test data or from consensus of current stress derating guidelines available from multiple military and industry sources. These approaches to understanding the stress-failure relationships of advanced technology components, outlined in figure 3-1, were executed on a priority basis in the order listed above. That is, if a current reliability model was available, it was used (approach A). If a reliability model was not available, a reliability model was developed, when possible, from accumulated stress-failure data

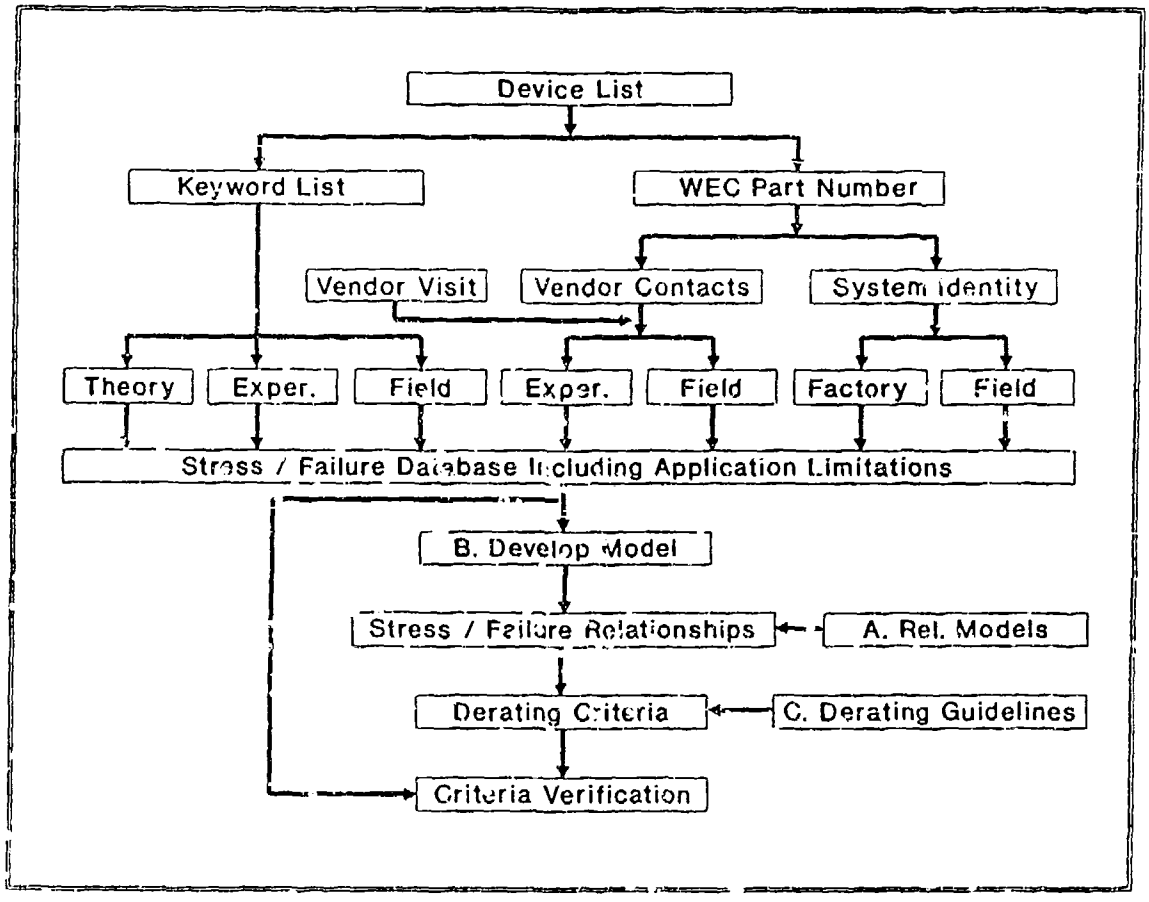


Figure 3-1 Flowchart of Technical Approach

(approach B). If it was not possible to develop a reliability model, then a consensus of available derating guidelines was used to generate the proposed derating criteria (approach C). Table 3-1 identifies the approach used for each component type listed in table 1-1.

In the approach taken to update the stress derating criteria using reliability models, approach A, a methodology was established in which a maximum failure rate was calculated for each criticality level for each component type. The reliability model used to generate these maximum failure rates was MIL-HDBK-217D Notice 1, since this revision of MIL-HDBK-217 was the current Handbook revision (13 June 1983) at the time in which the current version of the Guidelines was released (5 December

Table 3-1 Derating Criteria Approach

Device Type	Approach
ASIC	A,C
VHSIC	A,C
Microprocessor	A,C
PROM	A,C
MIMIC	A,C
Power Transistor	A,B,C
RF Pulse Transistor	C
RF Multi-transistor Package	C
Photo Transistor	C
Photo Diode	C
Opto-electronic Coupler	C
Injection Laser Diode	C
LED	C
Hybrid Deposited Film Resistor	X
Chip Resistor	C
Chip Capacitor	C
SAW	C

KEY: A - Reliability Model Available
B - New Reliability Model Developed
C - Concensus of Available Derating Guidelines
X - Insufficient Information

1983). The reliability models and derating guidelines used to calculate the failure rates are shown in table 3-2 for each component type for which approach A was used. These failure rates, listed in table 3-3, represent the maximum failure rates expected for the given criticality level allowed by the current version of the Guidelines.

The example of how the stress derating criteria was applied in the development of the maximum failure rates for MOS digital ASIC/VHSIC microcircuits is shown in table 3-4. Using the stress derating criteria for MOS microcircuits in the current Guidelines, the maximum values of each factor in the reliability model were determined for each criticality level. The failure rates were calculated to be 0.3402, 3.0593 and 31.640 fpmh for criticality levels I, II and III, respectively (see table 3-3).

Table 3-2 Reliability Models and Derating Guidelines Used In Developing Maximum Failure Rates

Component Type	MIL-HDBK-217D Notice 1	AFSCP 800-27 (1983)
ASIC/VHSIC	Microcircuits:	Microcircuits:
- MOS Digital	- Monolithic MOS Random Logic LSI	- Digital (MOS)
- MOS Linear	- Monolithic MOS Linear	- Linear (MOS)
- Bipolar Digital	- Monolithic Bipolar Ran. Logic LSI	- Digital (Bipolar)
- Bipolar Linear	- Monolithic Bipolar Linear	- Linear (Bipolar)
Microprocessor	Microcircuits:	Microcircuits:
- MOS	- Microprocessor (MOS)	- Digital (MOS)
- Bipolar	- Microprocessor (Bipolar)	- Digital (Bipolar)
PROM	Microcircuits:	Microcircuits:
- MOS	- PROM (MOS)	- Digital (MOS)
- Bipolar	- PROM (Bipolar)	- Digital (Bipolar)
Power Transistors	Transistors:	Transistors:
- Silicon Bipolar	- Group I, Silicon	- Bipolar Silicon
- GaAs	- (Not Listed)	- Field Effect
- MOSFET	- (Not Listed)	- Field Effect

Table 3-3 Maximum Failure Rates for Each Criticality Level

Component Type	Failure Rates (fpmh) for Levels: I	II	III
ASIC/VHSIC			
- MOS Digital	0.3402	3.0593	31.6405
- MOS Linear	0.4932	4.3920	46.0962
- Bipolar Digital	0.3126	1.5862	11.6614
- Bipolar Linear	0.4932	2.7477	24.8862
Microprocessor			
- MOS	0.3402	3.0593	31.6405
- Bipolar	0.3126	1.5862	11.6614
PROM			
- MOS	2.7371	22.7459	264.2236
- Bipolar	0.6322	2.8023	23.6754
Power Transistor			
- Silicon Bipolar	0.0040	1.2917	0.5763

The reliability model parameters and derating values for the microcircuits and power transistors for which approach A was used are shown in abbreviated format in tables 3-5 and 3-6, respectively. The calculated maximum failure rates "bound" the stresses driving the component reliability, described by the updated component reliability models, such that these maximum failure rates could not be exceeded. The values of the stresses, in absolute form or as a percentage of the maximum rated value, became the new derating criteria. Using this methodology, the new derating criteria could remain consistent with the old derating criteria. That is, the updated stress derating criteria will not allow a component to be used in a particular mission with a higher failure rate than was allowed by the current version of the Guidelines. In fact, the derating criteria developed for more complex microcircuits results in a lower failure rate per function for these microcircuits than less complex microcircuits. It

Table 3-4 MOS Digital ASIC Reliability Model Factors at Derated Values

Level	Factor	Value	Stress Derating Attributes
I	PiQ	0.5	S Level
I	PiT	6.9	85 deg C, A = 7532
I	PiV	1.0	5 volts
I	PiE	0.9	SF
I	PiL	1.0	> 4 months production
I	C1	0.0919	20,000 Gates
I	C2	0.0024	20,000 Gates
I	C3	0.048	64 pin DIP, glass seal
II	PiQ	1.0	B Level
II	PiT	16.1	100 deg C, A = 7532
II	PiV	1.76	12-15.5 volts, 85% derating, 100 deg C
II	PiE	9.0	AUF
II	PiL	1.0	> 4 months production
II	C1	0.0919	20,000 Gates
II	C2	0.0024	20,000 Gates
II	C3	0.048	64 pin DIP, glass seal
III	PiQ	6.5	B-2 Level
III	PiT	27.3	110 deg C, A = 7532
III	PiV	1.89	12-15.5 volts, 85% derating, 110 deg C
III	PiE	2.5	GF
III	PiL	1.0	> 4 months production
III	C1	0.0919	20,000 Gates
III	C2	0.0024	20,000 Gates
III	C3	0.048	64 pin DIP, glass seal

is noted here that the environmental factors were chosen for the same reason other constants and parameters were chosen, that is, to give the maximum failure rates. It should be noted, however, that the value of the worst case environmental factor (as well as the other factors) in the development of the maximum failure rate cancels with the worst case environmental factor (as well as the other factors) in the development of the updated stress derating criteria. Again, the intent was not to develop "conservative" results, but results that would be considered commensurate with the results already experienced when using the stress derating criteria outlined by the current version of the Guidelines.

Table 3-5 Reliability Model Factors and Derated Values for ASIC/VHSIC, Microprocessors and PROMs

Description			Factors					
Device Type	Prediction Reference	Crit. Level	Quality (PiQ)	Complexity (C1)	Temperature (PiT)	Voltage (PiV)	Prog. Tech. (PiPT)
Monolithic MOS Random Logic LSI	MIL-217D1	1	0.50	0.0919	6.91	1.00	N/A
		2	1.00	0.0919	16.11	1.76	N/A
		3	6.50	0.0919	27.30	1.89	N/A
Monolithic MOS Linear	MIL-217D1	1	0.50	0.1343	6.91	1.00	N/A
		2	1.00	0.1343	16.11	1.76	N/A
		3	6.50	0.1343	27.30	1.89	N/A
Monolithic Bipolar Random Logic LSI	MIL-217D1	1	0.50	0.2221	2.60	1.00	N/A
		2	1.00	0.2221	4.99	1.00	N/A
		3	6.50	0.2221	7.49	1.00	N/A
Monolithic Bipolar Linear	MIL-217D1	1	0.50	0.1343	6.91	1.00	N/A
		2	1.00	0.1343	16.11	1.00	N/A
		3	6.50	0.1343	27.30	1.00	N/A
Microprocessor (MOS)	MIL-217D1	1	0.50	0.0919	6.91	1.00	N/A
		2	1.00	0.0919	16.11	1.76	N/A
		3	6.50	0.0919	27.30	1.89	N/A
Microprocessor (Bipolar)	MIL-217D1	1	0.50	0.2221	2.60	1.00	N/A
		2	1.00	0.2221	4.99	1.00	N/A
		3	6.50	0.2221	7.48	1.00	N/A
PROM (MOS)	MIL-217D1	1	0.50	0.1340	6.91	1.00	5.8600
		2	1.00	0.1340	16.11	1.76	5.8600
		3	6.50	0.1340	27.30	1.89	5.8600
PROM (Bipolar)	MIL-217D1	1	0.50	0.0650	2.60	1.00	7.2100
		2	1.00	0.0650	5.00	1.00	7.2100
		3	6.50	0.0650	7.50	1.00	7.2100

KEY: N/A - Not Applicable

Table 3-5 Reliability Model Factors and Derated Values for ASIC/VHSIC, Microprocessors and PROMs (continued)

Description			Factors				Failure Rate
Device Type	Prediction Reference	Crit. Level	Complexity (C2)	Complexity (C3)	Environment (PiE)	Learning (PiL)	(Failures / 10^6 Hrs)
Monolithic MOS Random Logic LSI	MIL-217D1	1	0.0024	0.0480	0.90	1.00	0.3402
		2	0.0024	0.0480	9.00	1.00	3.0593
		3	0.0024	0.0480	2.50	1.00	31.6405
Monolithic MOS Linear	MIL-217D1	1	0.0169	0.0480	0.90	1.00	0.4932
		2	0.0169	0.0480	9.00	1.00	4.3920
		3	0.0169	0.0480	2.50	1.00	46.0962
Monolithic Bipolar Random Logic LSI	MIL-217D1	1	0.0051	0.0480	0.90	1.00	0.3126
		2	0.0051	0.0480	9.00	1.00	1.5862
		3	0.0051	0.0480	2.50	1.00	11.6614
Monolithic Bipolar Linear	MIL-217D1	1	0.0169	0.0480	0.90	1.00	0.4932
		2	0.0169	0.0480	9.00	1.00	2.7477
		3	0.0169	0.0480	2.50	1.00	24.8862
Microprocessor (MOS)	MIL-217D1	1	0.0024	0.0480	0.90	1.00	0.3402
		2	0.0024	0.0480	9.00	1.00	3.0593
		3	0.0024	0.0480	2.50	1.00	31.6405
Microprocessor (Bipolar)	MIL-217D1	1	0.0051	0.0480	0.90	1.00	0.3126
		2	0.0051	0.0480	9.00	1.00	1.5862
		3	0.0051	0.0480	2.50	1.00	11.6614
PROM (MOS)	MIL-217D1	1	0.0055	0.0480	0.90	1.00	2.7371
		2	0.0055	0.0480	9.00	1.00	22.7459
		3	0.0055	0.0480	2.50	1.00	264.2236
PROM (Bipolar)	MIL-217D1	1	0.0030	0.0480	0.90	1.00	0.6322
		2	0.0030	0.0480	9.00	1.00	2.8023
		3	0.0030	0.0480	2.50	1.00	23.6754

KEY: N/A - Not Applicable

Table 3-5 Reliability Model Factors and Derated Values for ASIC/VHSIC, Microprocessors and PROMs (continued)

Description			Rationale				
Device Type	Prediction Reference	Crit. Level	Quality (PiQ)	Complexity (C1)	Temperature (PiT)	Voltage (PiV)
Monolithic MOS Random Logic LSI	MIL-217D1	1	S	20K Gates	85 C, A=7532	5V
		2	B	20K Gates	100 C, A=7532	12-15.5V, 85% Der., 100 C
		3	B-2	20K Gates	110 C, A=7532	12-15.5V, 85% Der., 110 C
Monolithic MOS Linear	MIL-217D1	1	S	300 Trans.	85 C, A=7532	5V
		2	B	300 Trans.	100 C, A=7532	12-15.5V, 85% Der., 100 C
		3	B-2	300 Trans.	110 C, A=7532	12-15.5V, 85% Der., 110 C
Monolithic Bipolar Random Logic LSI	MIL-217D1	1	S	20K Gates	85 C, A=5794	(Non-CMOS)
		2	B	20K Gates	100 C, A=5794	(Non-CMOS)
		3	B-2	20K Gates	110 C, A=5794	(Non-CMOS)
Monolithic Bipolar Linear	MIL-217D1	1	S	300 Trans.	85 C, A=7532	(Non-CMOS)
		2	B	300 Trans.	100 C, A=7532	(Non-CMOS)
		3	B-2	300 Trans.	110 C, A=7532	(Non-CMOS)
Microprocessor (MOS)	MIL-217D1	1	S	20K Gates	85 C, A=7532	5V
		2	B	20K Gates	100 C, A=7532	12-15.5V, 85% Der., 100 C
		3	B-2	20K Gates	110 C, A=7532	12-15.5V, 85% Der., 110 C
Microprocessor (Bipolar)	MIL-217D1	1	S	20K Gates	85 C, A=5794	(Non-CMOS)
		2	B	20K Gates	100 C, A=5794	(Non-CMOS)
		3	B-2	20K Gates	110 C, A=5794	(Non-CMOS)
PROM (MOS)	MIL-217D1	1	S	65536 Bits	85 C, A=7532	5V
		2	B	65536 Bits	100 C, A=7532	12-15.5V, 85% Der., 100 C
		3	B-2	65536 Bits	110 C, A=7532	12-15.5V, 85% Der., 110 C
PROM (Bipolar)	MIL-217D1	1	S	65536 Bits	85 C, A=5794	(Non-CMOS)
		2	B	65536 Bits	100 C, A=5794	(Non-CMOS)
		3	B-2	65536 Bits	110 C, A=5794	(Non-CMOS)

KEY: N/A - Not Applicable

Table 3-5 Reliability Model Factors and Derated Values for ASIC/VHSIC, Microprocessors and PROMs (continued)

Description			Rationale					
Device Type	Prediction Reference	Crit. Level	Prog. Tech. (PiPT)	Complexity (C2)	Complexity (C3)	Environment (PiE)	Learning (PiL)
Monolithic MOS Random Logic LSI	MIL-217D1	1	N/A	20K Gates	64P DIP, Glass Seal	SF	> 4 Months
		2	N/A	20K Gates	64P DIP, Glass Seal	AUF	> 4 Months
		3	N/A	20K Gates	64P DIP, Glass Seal	GF	> 4 Months
Monolithic MOS Linear	MIL-217D1	1	N/A	300 Trans.	64P DIP, Glass Seal	SF	> 4 Months
		2	N/A	300 Trans.	64P DIP, Glass Seal	AUF	> 4 Months
		3	N/A	300 Trans.	64P DIP, Glass Seal	GF	> 4 Months
Monolithic Bipolar Random Logic LSI	MIL-217D1	1	N/A	20K Gates	64P DIP, Glass Seal	SF	> 4 Months
		2	N/A	20K Gates	64P DIP, Glass Seal	AUF	> 4 Months
		3	N/A	20K Gates	64P DIP, Glass Seal	GF	> 4 Months
Monolithic Bipolar Linear	MIL-217D1	1	N/A	300 Trans.	64P DIP, Glass Seal	SF	> 4 Months
		2	N/A	300 Trans.	64P DIP, Glass Seal	AUF	> 4 Months
		3	N/A	300 Trans.	64P DIP, Glass Seal	GF	> 4 Months
Microprocessor (MOS)	MIL-217D1	1	N/A	20K Gates	64P DIP, Glass Seal	SF	> 4 Months
		2	N/A	20K Gates	64P DIP, Glass Seal	AUF	> 4 Months
		3	N/A	20K Gates	64P DIP, Glass Seal	GF	> 4 Months
Microprocessor (Bipolar)	MIL-217D1	1	N/A	20K Gates	64P DIP, Glass Seal	SF	> 4 Months
		2	N/A	20K Gates	64P DIP, Glass Seal	AUF	> 4 Months
		3	N/A	20K Gates	64P DIP, Glass Seal	GF	> 4 Months
PROM (MOS)	MIL-217D1	1	65536 Bits	65536 Bits	64P DIP, Glass Seal	SF	> 4 Months
		2	65536 Bits	65536 Bits	64P DIP, Glass Seal	AUF	> 4 Months
		3	65536 Bits	65536 Bits	64P DIP, Glass Seal	GF	> 4 Months
PROM (Bipolar)	MIL-217D1	1	65536 Bits	65536 Bits	64P DIP, Glass Seal	SF	> 4 Months
		2	65536 Bits	65536 Bits	64P DIP, Glass Seal	AUF	> 4 Months
		3	65536 Bits	65536 Bits	64P DIP, Glass Seal	GF	> 4 Months

KEY: N/A - Not Applicable

Table 3-6 Reliability Model Factors and Derated Values for Silicon Bipolar Power Transistors

Description			Factors			
Device Type	Prediction Reference	Crit. Level	Base FR (LambdaB)	Quality (PiQ)	Complexity (C1)	Environment (PiE)
Transistor Group I (Silicon)	MIL-217D1	1 2 3	0.0092 0.0092 0.0092	0.12 0.24 1.20	1.0000 1.0000 1.0000	0.40 65.00 5.80

Description			Factors			Failure Rate
Device Type	Prediction Reference	Crit. Level	Application (PiA)	Power Rating (PiR)	Volt. Stress (PiS)	(Failures / 10^{-6} Hrs)
Transistor Group I (Silicon)	MIL-217D1	1 2 3	1.50 1.50 1.50	5.00 5.00 5.00	1.20 1.20 1.20	0.0040 1.2917 0.5763

Description			Rationale			
Device Type	Prediction Reference	Crit. Level	Base FR (LambdaB)	Quality (PiQ)	Complexity (C1)	Environment (PiE)
Transistor Group I (Silicon)	MIL-217D1	1 2 3	(max) (max) (max)	JANTXV JANTX JAN	Single Trans. Single Trans. Single Trans.	SF AUF GF

Description					
Device Type	Prediction Reference	Crit. Level	Application (PiA)	Power Rating (PiR)	Volt. Stress (PiS)
Transistor Group I (Silicon)	MIL-217D1	1 2 3	Linear Linear Linear	200 Watts 200 Watts 200 Watts	S2 = 70% S2 = 70% S2 = 70%

In the approach to update the stress derating criteria by creating new reliability models, approach B, stress-failure data accumulated from the literature search and supplier surveys was examined, and the reliability model was generated. It is noted here that this approach was used only for the temperature parameter in the reliability model for GaAs power transistors (see Section 6.2).

If approaches A and B were not viable, then a consensus of available derating guidelines was used to update the stress derating criteria, approach C. The fourteen guidelines used in the criteria development are listed in table 3-7. Of these fourteen guidelines, twelve guidelines were from government or military sources and two were from industry sources. The parameters selected for derating by these fourteen sources were not consistent between the sources. Therefore, before the stress derating criteria could be evaluated, it was first necessary to identify the key parameters to be derated. These key parameters were initially limited by the sources that specified derating criteria for three criticality levels (guidelines A through F). The remaining parameters were included as application notes, when appropriate. It is noted here that guidelines A and B were exactly the same, and therefore, guidelines A and B were considered one source in the development of the final updated stress derating criteria. Once these parameters were identified, the consensus of the five guidelines was obtained by calculating the median of the stress derating values for each stress parameter.

In all cases, application notes and design limitations were developed from accumulated component information, obtained in the literature search or supplier surveys, and extrapolated from other derating guidelines. The application notes for each component type are furnished at the end of each primary report sections and in Appendix A. In addition, the adequacy of the stress derating criteria was reviewed using failure rates calculated from accumulated field failure data (see Section 11.0).

Table 3-7 Government/Military/Industry Stress Derating Guideline Titles

Designator	Guideline
A	AFSC Pamphlet 800-27, 5 December 1983
B	ESD-TR-83-197
C	ESD-TR-85-148
D	RADC-TR-84-254
E	RADC-TR-82-177
F	NASC AS-4613
G	GSFC PPL-18 (NASA), October 1986
H	NAVMAT P-4855-1A
J	MIL-STD-2174 (AS), July 1976
K	MIL-STD-975H (NASA), June 1989
L	NAVSEA TE000-AB-GTP-010, September 1985
M	MIL-STD-1547A, December 1987
W	OEM A
X	OEM B

4.0 MICROCIRCUIT DERATING GUIDELINES

For advanced technology silicon microcircuits, the RA/AAT reliability models[1] can be summarized in general form by

$$L(t_o) = PiQ * (C1 * PiT + L_{CYC} + C2 * PiE) * PiL + L_{TDDB}(t_o) + L_{EM}(t_c), \quad (1)$$

where:

$L(t_o)$ is the device failure rate at time to in failures per million hours,

PiQ is the quality factor,

PiT is the temperature acceleration factor, based on technology,

PiE is the application environment factor

PiL is the learning factor,

C1 is the circuit complexity failure rate in failures per million hours,

C2 is the package complexity failure rate in failures per million hours,

L_{CYC} is the EEPROM write cycling induced failure rate in failures per million hours,

$L_{TDDB}(t_o)$ is the time dependent dielectric breakdown (TDDB) failure rate at time to in failures per million hours, and

$L_{EM}(t_o)$ is the electromigration (EM) failure rate at time to in failures per million hours.

A review of the literature[29-100] concerned with microcircuit failure, during the time since the RA/AAT reliability models were generated, resulted in no change to the basic reliability models. However, it was noted that, since failures due to electromigration, having failure rates L_{EM}, are distributed normally with the logarithm of time with very small variances, the effect of L_{EM} on the total failure rate, $L(t_o)$, is either negligible or catastrophic. Therefore, the L_{EM} term was

eliminated from the equation for calculating failure rate and the electromigration effect is presented as an application note. Without this L_{EM} term, the failure rate equation for deriving stress derating criteria simplifies to

$$L(t_o) = PiQ * (C1 * PiT + L_{CYC} + C2 * PiE) * PiL + L_{TDDB}(t_o). \quad (2)$$

The stress parameters and attributes that directly affect the calculated failure rate for a silicon microcircuit are embedded in the Pi, complexity, and wear out failure rate factors of the reliability model. To extract the maximum stresses allowed for each criticality level from the factors in the reliability model, $L(t_o)$ in equation (2) must be set to the maximum failure rate allowed by each criticality level. These maximum failure rates are specified in table 3-3. In the approach to develop stress derating criteria for advanced technology silicon microcircuits, the parameters and attributes of the failure rate model factors were separated into three groups, one group for criticality-specific (CS) attributes, one group for device-specific (DS) attributes and the other group for stress-specific (SS) parameters. Table 4-1 outlines the relationship between the factors in the failure rate equation, the distinction between criticality-specific, device-specific and stress-specific parameters and attributes associated with the factors, and the microcircuit technologies for which these parameters and attributes are applicable.

There were two basic types of device-specific attributes, technology and complexity. The technology attribute was handled by creating stress derating criteria for each technology individually. For example, there are digital and linear, MOS and bipolar ASIC/VHSIC microcircuits. Therefore, four stress derating tables were developed, one for digital MOS ASIC/VHSIC microcircuits, one for digital bipolar ASIC/VHSIC microcircuits, one for linear MOS ASIC/VHSIC microcircuits and one for linear bipolar ASIC/VHSIC microcircuits. The complexity attribute was handled by making the circuit complexity parameter (i.e., number of gates, transistors or bits) a variable in the stress derating criteria. Because of the large number of

Table 4-1 Attributes and Parameters of Microcircuit Model Factors

Factor	Type	Attribute / Parameter	Application to: MOS	Application to: Bipolar
PiQ	CS	Application Environment	Y	Y
PiT	DS	Technology	Y	Y
	SS	Junction Temperature	Y	Y
PiE	CS	Application Environment	Y	Y
PiL	CS	Years In Production	Y	Y
C1	DS	Circuit Technology	Y	Y
	DS	Circuit Complexity	Y	Y
C2	DS	Package Technology	Y	Y
	DS	Package Complexity	Y	Y
L CYC	DS	Circuit Complexity	Y *	N
	SS	Number of Write Cycles	Y *	N
L TDDB	DS	Circuit Complexity	Y	N
	SS	Junction Temperature	Y	N
	SS	Supply Voltage	Y	N

KEY: * - EEPROMs Only

computations required, the C1 factor tables in the RA/AAT final report were transformed to continuous functions. A relationship between circuit complexity and package complexity was developed from literature sources[57] such that the package complexity parameter (i.e., number of pins) could also be handled in terms of the circuit complexity parameter. All other relationships required in the development of the derating criteria were also based on circuit complexity. It is noted here that all relationships based on circuit complexity were always developed in a conservative fashion

such that the resulting stress derating criteria would be valid for all complexities of microcircuits.

The criticality-specific attributes included the application environment attribute and the years-in-production attribute. The application environments for the PiQ factor were always S-Level, B-Level and B-Level for criticality levels I, II and III, respectively. The application environments for the PiE factor were always S_F, A_U and G_F for criticality levels I, II and III, respectively. These application environments were chosen since they were the most closely related to the application environments outlined by the criticality levels in the current version of the Guidelines and resulted in the highest failure rate for the criticality level they represented. The years-in-production attribute for the experience factor, PiL, were always 2 years, 1 year and 0.75 years for criticality levels I, II and III, respectively. These years in production were chosen based upon current experience with component procurement for systems that can be categorized by the definitions given for each criticality level.

The stress-specific parameters, as mentioned previously, are the only ones that, when changed, result in a different failure rate for any given microcircuit. These parameters, temperature, voltage and number of write cycles (EEPROMs only), are the ones that can be traded-off to obtain the same maximum failure rate for a given microcircuit. A consistent approach was taken (with an exception for EEPROMs, see Section 4.3) in developing the bounds for these stress-specific parameters such that the resulting derating criteria would be effective, but not oppressive, in the desired application.

This approach initially ignored the number of write cycles, or L_{CYC}, which was only applicable to EEPROMs. It was then assumed that, if the time dependent dielectric breakdown (TDDB) failure rate was not a factor because wear out was not a concern, then the only stress-specific parameter left was temperature. It is noted here that the defect-related failure

rate (exponential probability density function) is a concern for all microcircuits and cannot be ignored. The independence of the TDDB-driven wear out stresses and temperature is addressed in Section 4.1 in the example of MOS digital ASIC/VHSIC microcircuits. For any microcircuit of a given complexity, the temperature was calculated for which the failure rate did not exceed the maximum failure rate given in table 3-3, dependent upon criticality level. In calculating this maximum temperature, it was noted that the maximum failure rate was not always the limiting factor. Because of the form of the failure rate equation, to solve for temperature imbedded in the PiT factor required the term $L(t_o)/(PiQ*PiL)$ to be greater than C2*PiE. Since $L(t_o)$, PiQ, PiL and PiE are fixed for a given type of microcircuit, C2 controls the validity of the argument. For this reason, only microcircuits of a specified maximum complexity are acceptable in a given criticality level. This complexity limit is included in the stress derating criteria for microcircuits when applicable. If the maximum temperature was calculated to be a value higher than 175 degrees Celsius, then 175 degrees Celsius was chosen as the maximum temperature.

Once the maximum temperature had been calculated for a microcircuit of given complexity, it was noted that any operating temperature below this maximum temperature resulted in a calculated failure rate that was less than the maximum failure rate allowed by the criticality level. This difference in failure rate could then be used to bound the stresses associated with the TDDB wear out mechanism. Table 4-1 shows TDDB failure rates are only applicable to MOS microcircuits, and therefore, this development of the derating criteria for supply current is only applicable to MOS microcircuits.

Time dependent dielectric breakdown is a failure mechanism that results in a component failure distribution that is normal with the logarithm of time. That is, unlike the failure rates currently addressed by MIL-HDBK-217 Revision E Notice 1, the TDDB failure rate is time dependent[1]. There are three factors that affect the rate of failure for TDDB, the electric field across the dielectric, the dielectric film

temperature and the total area taken up by the transistor gates. A relationship was also developed[1] between the latter factor and microcircuit complexity. When dealing with a failure rate model that includes L_{TDDB}, it is assumed that the dielectric film temperature is the same as the junction temperature defining the PiT factor. Therefore, with the film temperature previously defined and the total transistor gate area correlated to microcircuit complexity, the only factor that is not defined is the electric field.

This electric field factor is proportional to the supply voltage according the dielectric thickness which is related to the complexity of the microcircuit. The difference in failure rate between the maximum derated temperature and the operating temperature therefore defines the maximum derating criteria for the supply voltage. That is, with the operating junction temperature less than the maximum junction temperature, the resulting failure rate is less than the maximum failure rate allowed by the criticality level. Therefore, the microcircuit could be operated with a supply voltage higher than the supply voltage allowed when operating at the maximum junction temperature provided the maximum failure rate is not exceeded.

With the device-specific, criticality-specific and stress-specific attributes and parameters defined, the maximum junction temperature and maximum supply voltage (MOS microcircuits only) derating criteria was developed. For convenience in developing this derating criteria, software programs were written in FORTRAN 77 programming language. Appendix B contains an example program written to calculate the temperature and voltage values displayed in the graphs for MOS digital ASIC/VHSIC microcircuits. Once the derating values were calculated, a least squares fit transformed this data into simplified equations dependent upon circuit complexity. The simplified equations become the update stress derating criteria for the junction temperature and supply voltage stress parameters.

It is noted here that, in some instances, the calculated derated stress was virtually independent of complexity. In that case, a constant derating value was substituted for the derating equation. Also, if the calculated derated stress was outside the region of validity of the reliability model, the value of the maximum stress identified in the model was substituted for the derating equation. For microcircuits, it was determined that the applicable reliability models were based on junction temperature data that did not exceed 125 deg C. Therefore, this maximum junction temperature was used in those cases where the calculated derated junction temperature stress was above 125 deg C. It is also noted that the microcircuit reliability models outlined in the RA/AAT study were valid only up to a specified maximum complexity. Although the data graphs generated and the corresponding stress derating equations are continuous past the specified maximum complexity, the stress derating criteria is not considered valid beyond this maximum complexity. Therefore, the derating parameter of "maximum complexity" is included in the list of derating parameters for microcircuits.

Since existing stress derating guidelines, other than those for the stresses explicitly identified in the reliability models, have purposely affected the observed failure rates of components used in applications corresponding to one of the three criticality levels, it was necessary to review the existing stress derating guidelines to determine their relevance in being included in the updated stress derating guidelines, given that the factors being derated were not explicitly included in the current reliability models. It was observed that failure data for components that did not abide by the stress derating criteria was not readily available (typically due to government or military contracts that require some type of derating) and to arbitrarily remove this criteria may be irresponsible. Therefore, the updated stress derating criteria for microcircuits includes both the newly created criteria based upon updated failure rate models as well as the current criteria which was developed for parameters not explicitly included in the updated failure rate models. It is noted here that the only stress derating criteria included by the guideline sources

that outline three criticality levels were included in this proposed revision of the Guidelines.

The application notes for advanced technology microcircuits were developed from a review of applicable literature, supplier surveys and other stress derating guidelines. These application notes may be found at the end of this microcircuit section and in Appendix A.

4.1 ASIC/VHSIC MICROCIRCUITS

Because of differences in technology within the ASIC/VHSIC category, stress derating tables were developed for MOS digital, bipolar digital, MOS linear, and bipolar linear ASIC/VHSIC microcircuits. The differences between the criteria in each table were the results of applying the different device-specific attributes and stress-specific parameters to the failure rate equation. These attributes and parameters included temperature activation energy (PiT), circuit complexity (C1), number of package pins (C2), total transistor gate area (L_{TDDB}) and dielectric thickness (L_{TDDB}). Table 4-2 outlines the values or equations used in evaluating these device/stress-specific attributes.

Table 4-2 ASIC/VHSIC Device/Stress-Specific Attributes

Technology	Attribute	Value / Equation
MOS Digital	Ea	0.35 eV
	C1	0.01 + 0.000427 * GATES ** 0.588
	Pins	11.07 * GATES ** 0.342
	C2	2.8E-4 * PINS ** 1.08
	Transistor Gate Area	1349 * TRANS ** 0.609 (sq um)
	Dielectric Thickness	4.93 / TRANS ** 0.286 (kA)
Bipolar Digital	Ea	0.60 eV
	C1	0.0025 + 0.0000977 * GATES ** 0.601
	Pins	9.16 * GATES ** 0.377
	C2	2.8E-4 * PINS ** 1.08
MOS Linear	Ea	0.65 eV
	C1	0.01 + 0.00150 * TRANS ** 0.488
	Pins	8.69 * GATES ** 0.318
	C2	2.8E-4 * PINS ** 1.08
	Transistor Gate Area	1349 * TRANS ** 0.609 (sq um)
	Dielectric Thickness	4.93 / TRANS ** 0.286 (kA)
Bipolar Linear	Ea	0.65 eV
	C1	0.01 + 0.00150 * TRANS ** 0.488
	Pins	8.69 * GATES ** 0.318
	C2	2.8E-4 * PINS ** 1.08

The temperature activation energies were obtained directly from the tables provided by the RA/AAT final report. The C1 factor equations were derived by fitting the C1 factor data associated with the RA/AAT failure rate models to an appropriate curve. The data and best fit curves are shown in figures 4-1, 4-2 and 4-3 for MOS digital, bipolar digital and MOS and bipolar linear ASIC/VHSIC microcircuits, respectively. The relationships between package pin count and circuit complexity for MOS digital, bipolar digital and MOS and bipolar linear ASIC/VHSIC microcircuits are shown in figures 4-4, 4-5 and 4-6, respectively. The data from which the relationship between total transistor gate area and circuit complexity was derived is shown in figure 4-7 for MOS digital and linear ASIC/VHSIC microcircuits. The dielectric thickness dependence on circuit complexity for MOS digital and linear ASIC/VHSIC microcircuits is shown in figure 4-8.

By applying the approach outlined in section 4.0, maximum junction temperatures and maximum supply voltages were calculated for the four ASIC/VHSIC technologies as a function of circuit complexity. Figures 4-9 and 4-10 show the junction temperature and supply voltage derating curves for MOS digital microcircuits. Figures 4-11 and 4-12 show the junction temperature and supply voltage derating curves for MOS linear microcircuits. Figure 4-11 is also the junction temperature derating curve for bipolar linear microcircuits. Since bipolar ASIC/VHSIC microcircuits do not experience wear out due to TDDB, supply voltage derating curves are not calculated for these technologies. Figure 4-13 shows the junction temperature derating curves for bipolar digital microcircuits. The solid lines on the graphs in each figure represent the best least squares fit to the calculated derating values. These equations of the lines are the new stress derating criteria for each criticality level.

Figure 4-1 C1 Factor for MOS Digital Microcircuits[1]

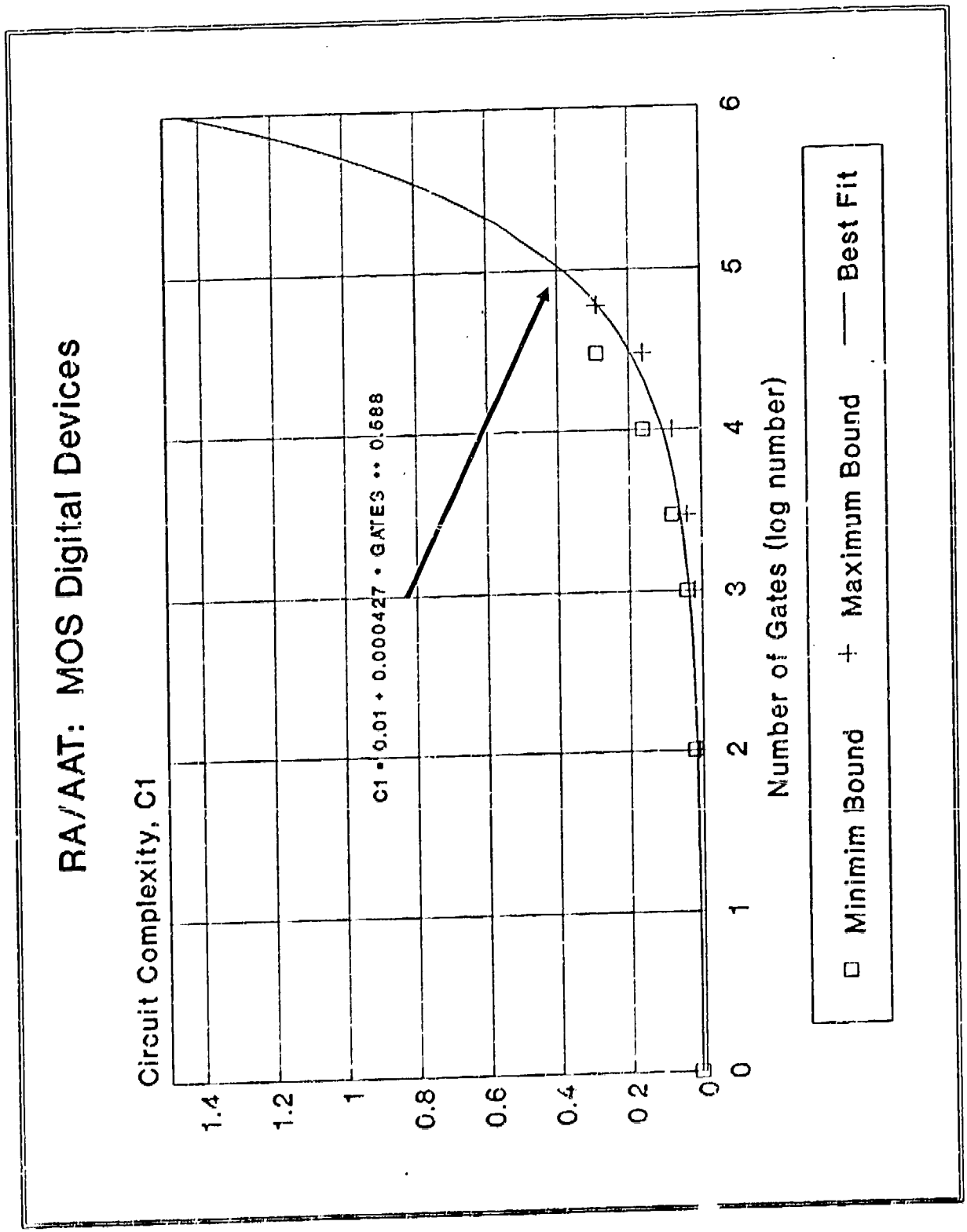


Figure 4-2 C1 Factor for Bipolar Digital Microcircuits[1]

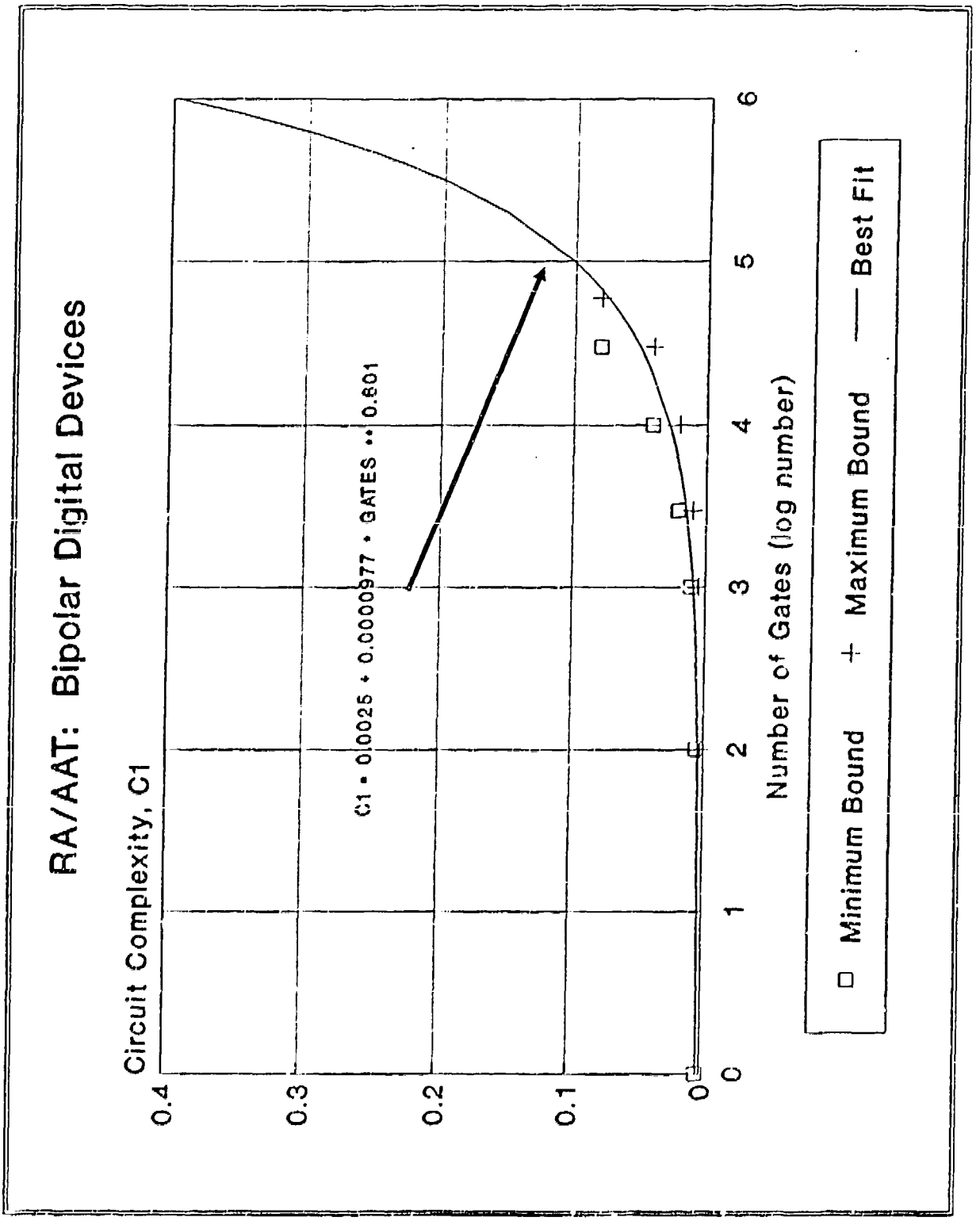


Figure 4-3 C1 Factor for MOS and Bipolar Linear Microcircuits[1]

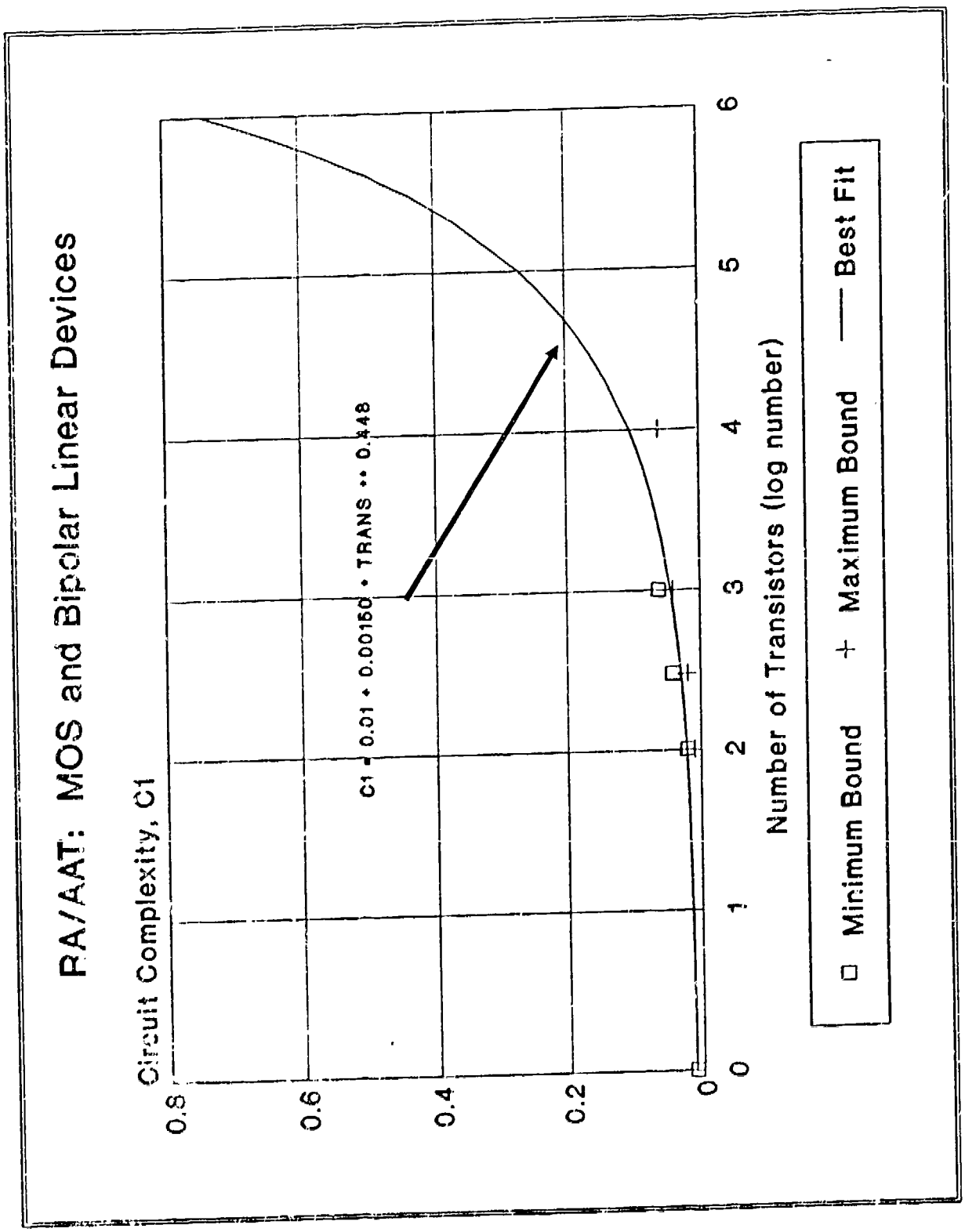


Figure 4-4 Package Pin Count for MOS Digital Microcircuits[57]

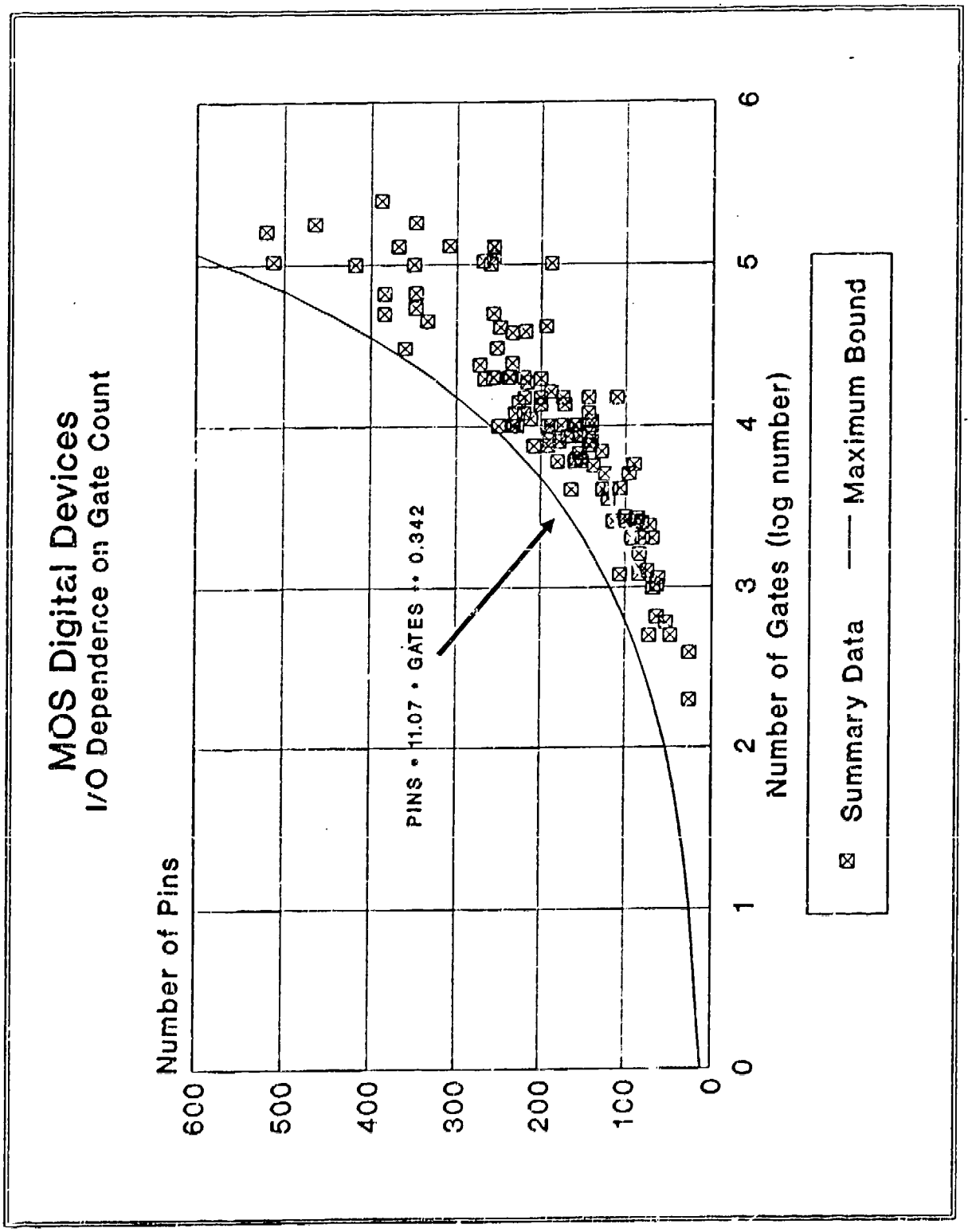


Figure 4-5 Package Pin Count for Bipolar Digital Microcircuits[57]

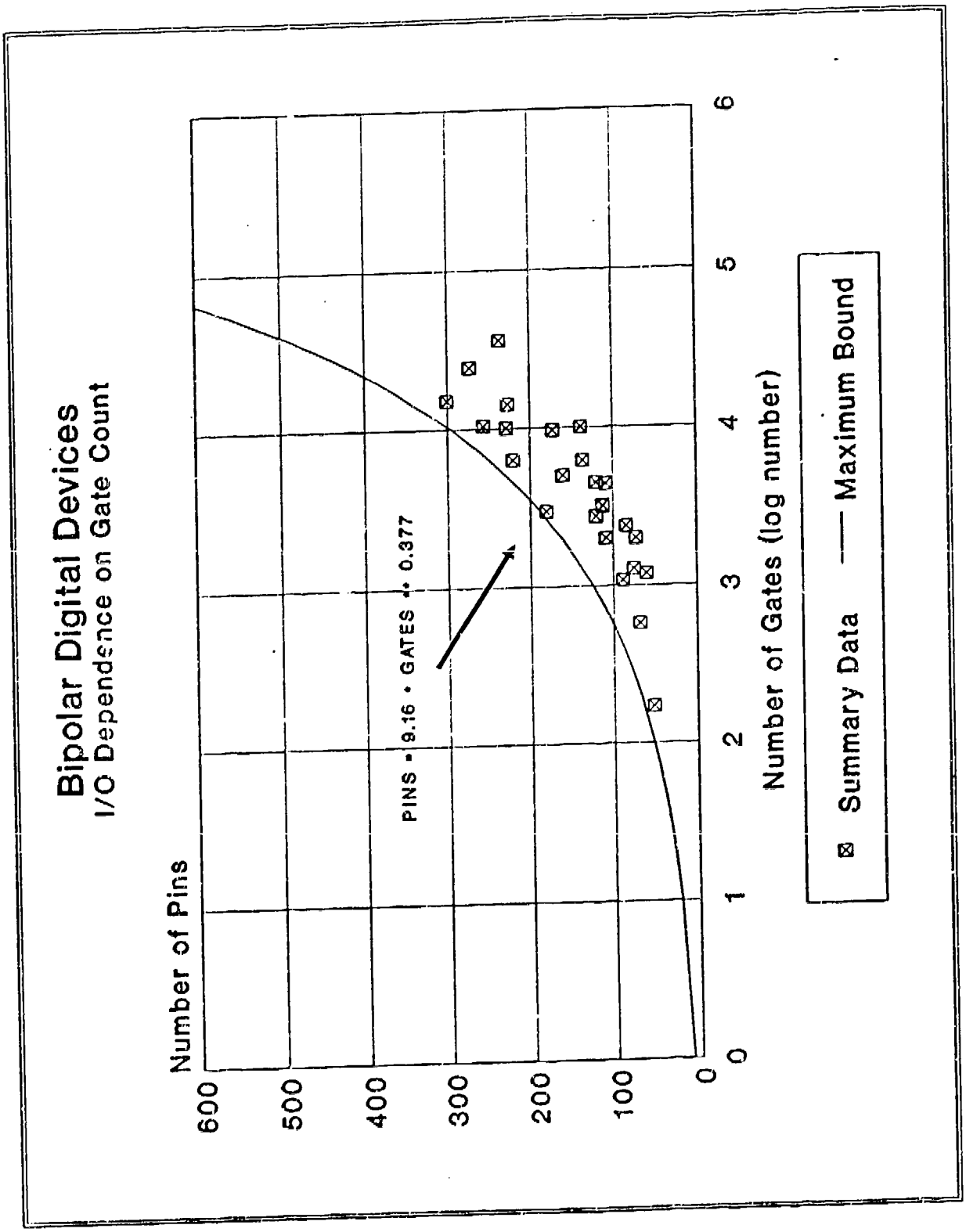


Figure 4-6 Package Pin Count for MOS and Bipolar Linear Microcircuits[57]

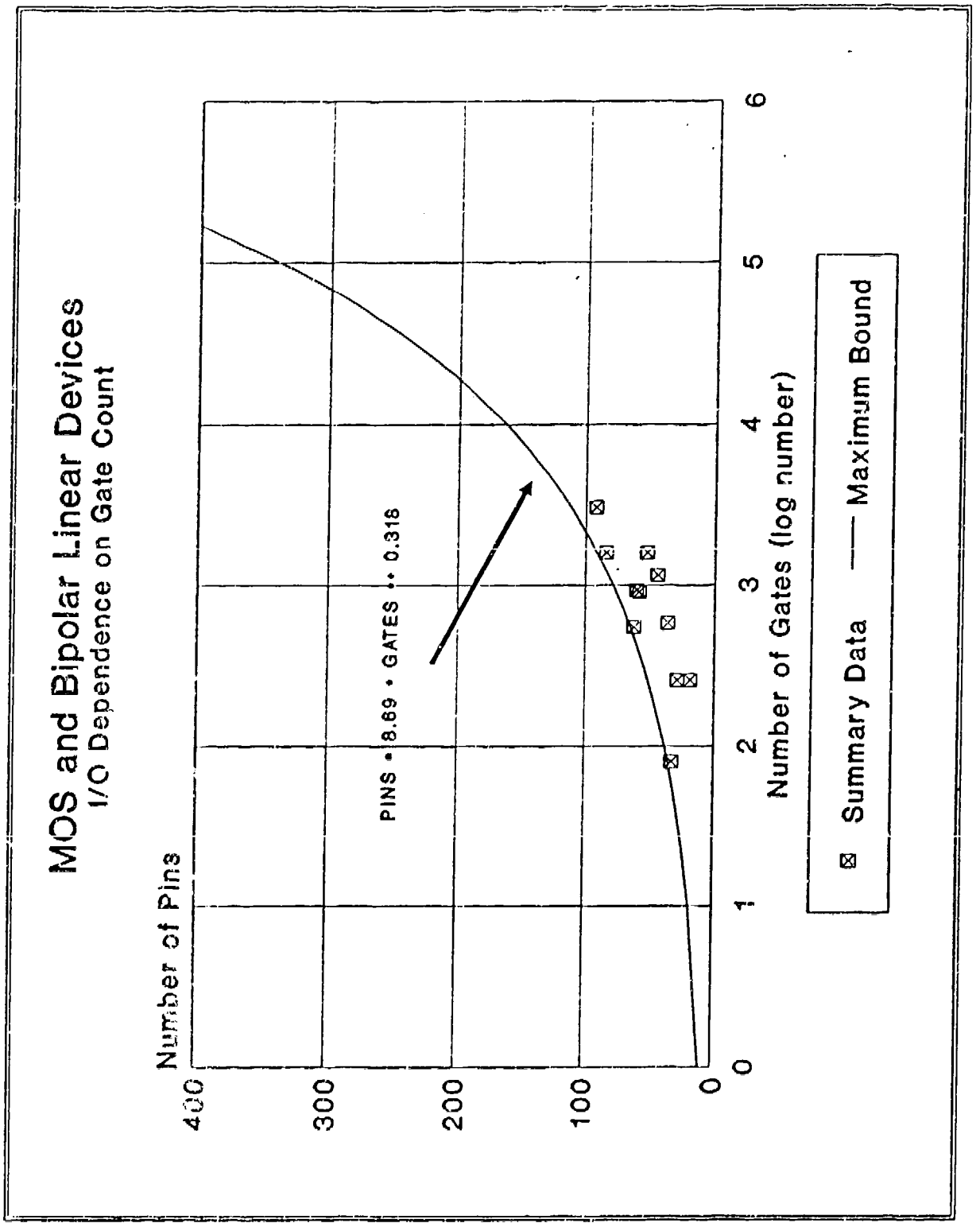


Figure 4-7 Transistor Gate Area for MOS Digital and Linear Microcircuits[1]

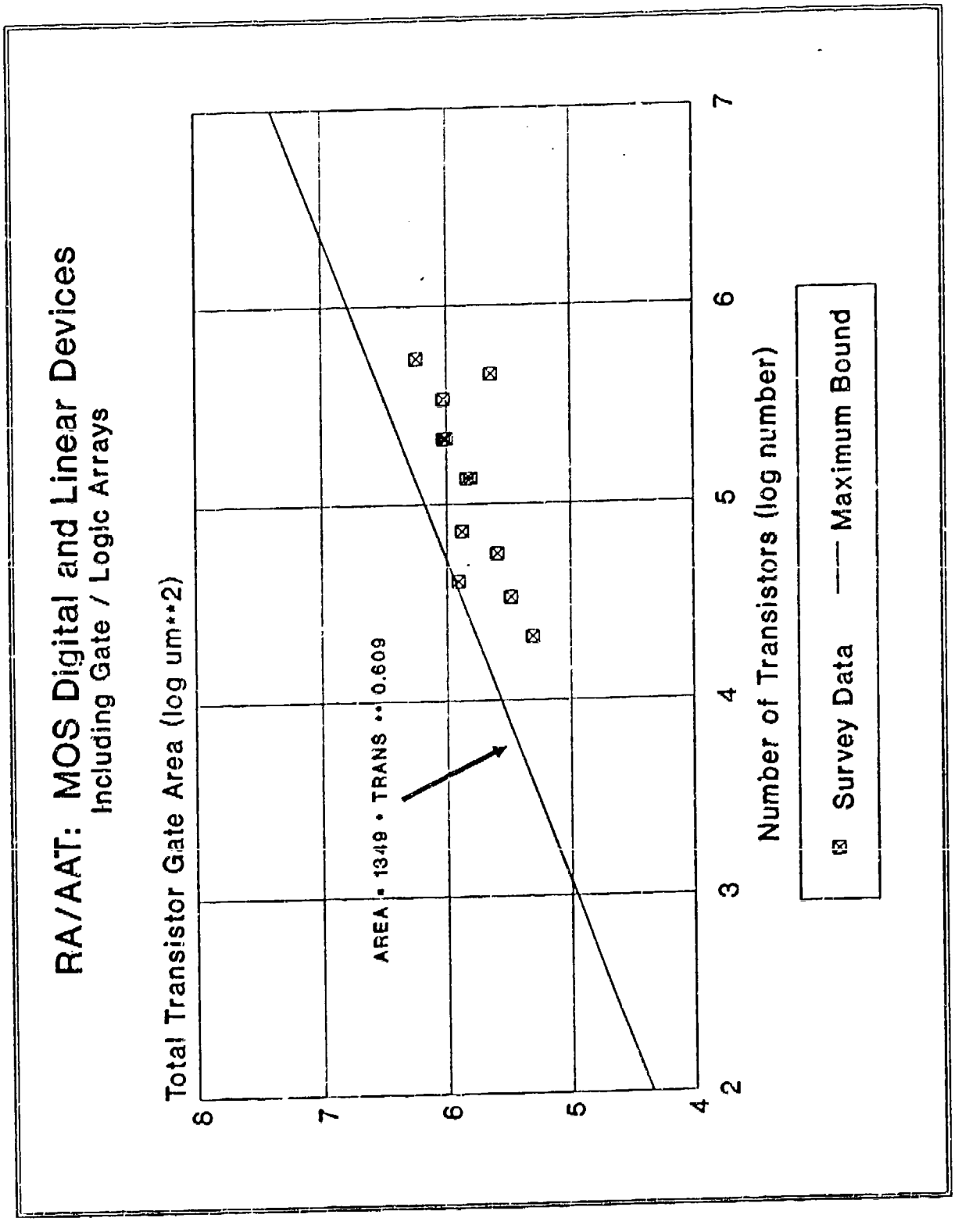


Figure 4-8 Dielectric Thickness for MOS Digital and Linear Microcircuits[1]

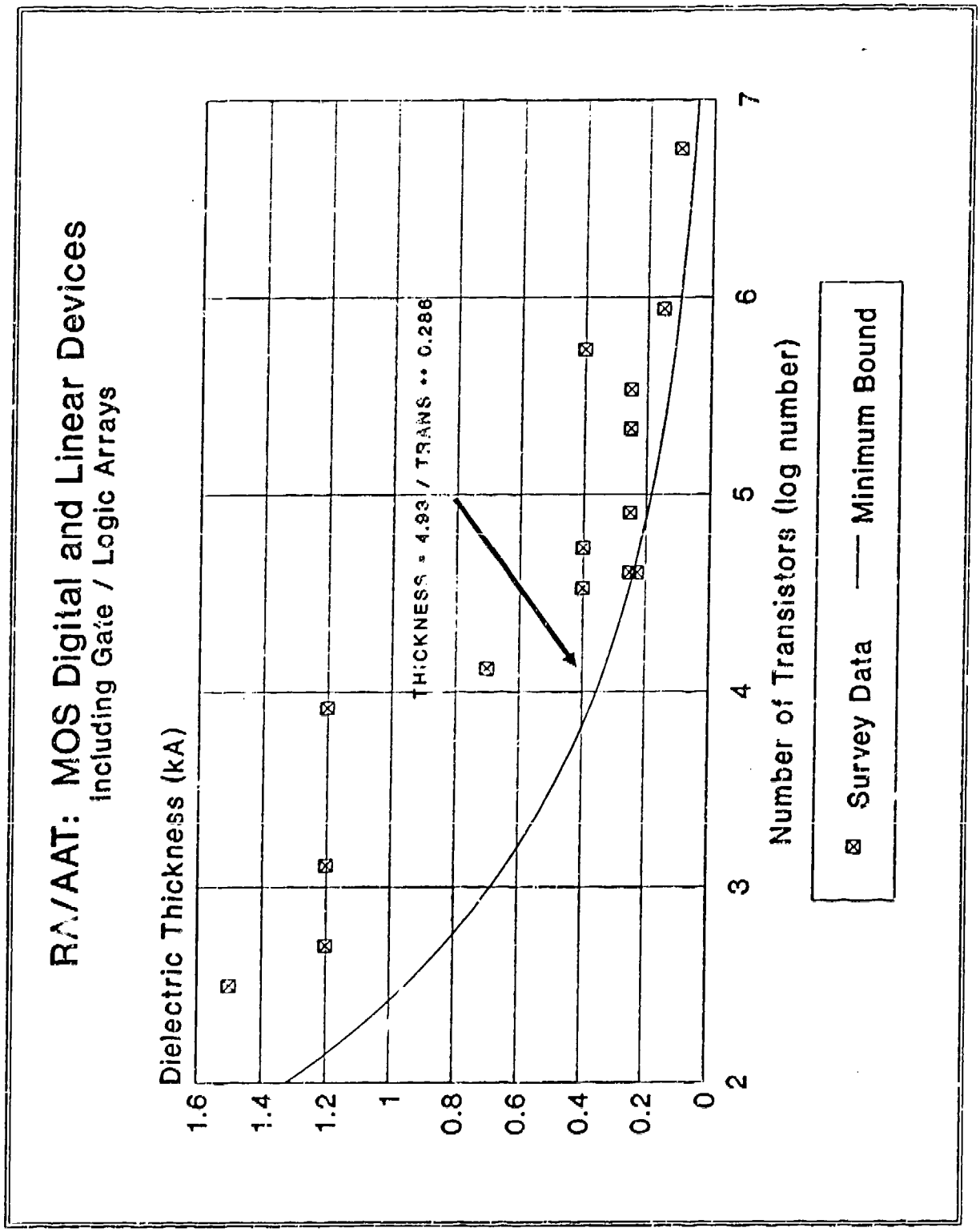


Figure 4-9 Junction Temperature Derating for MOS Digital ASIC/VHSIC

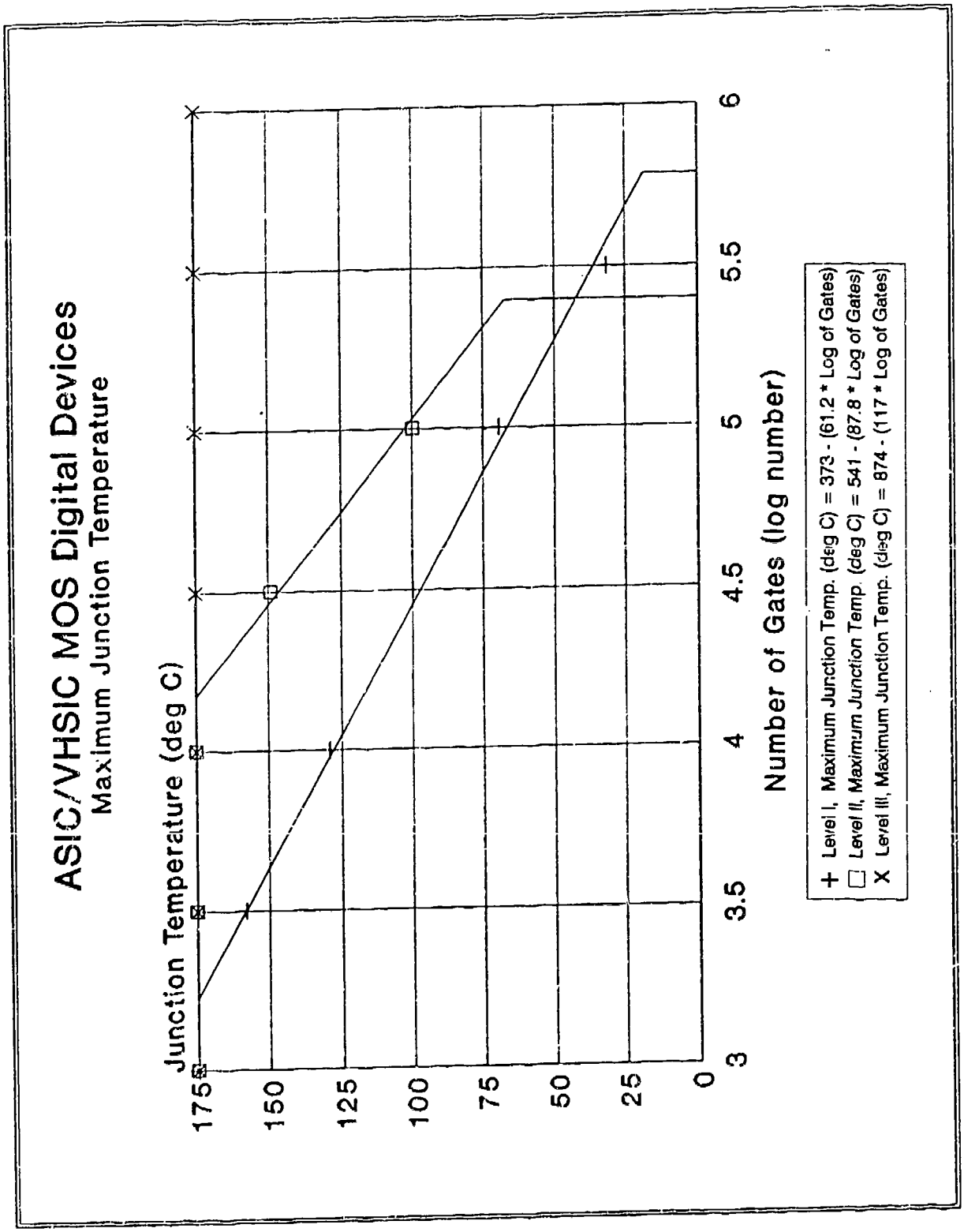


Figure 4-10 Supply Voltage Derating for MOS Digital ASIC/VHSIC

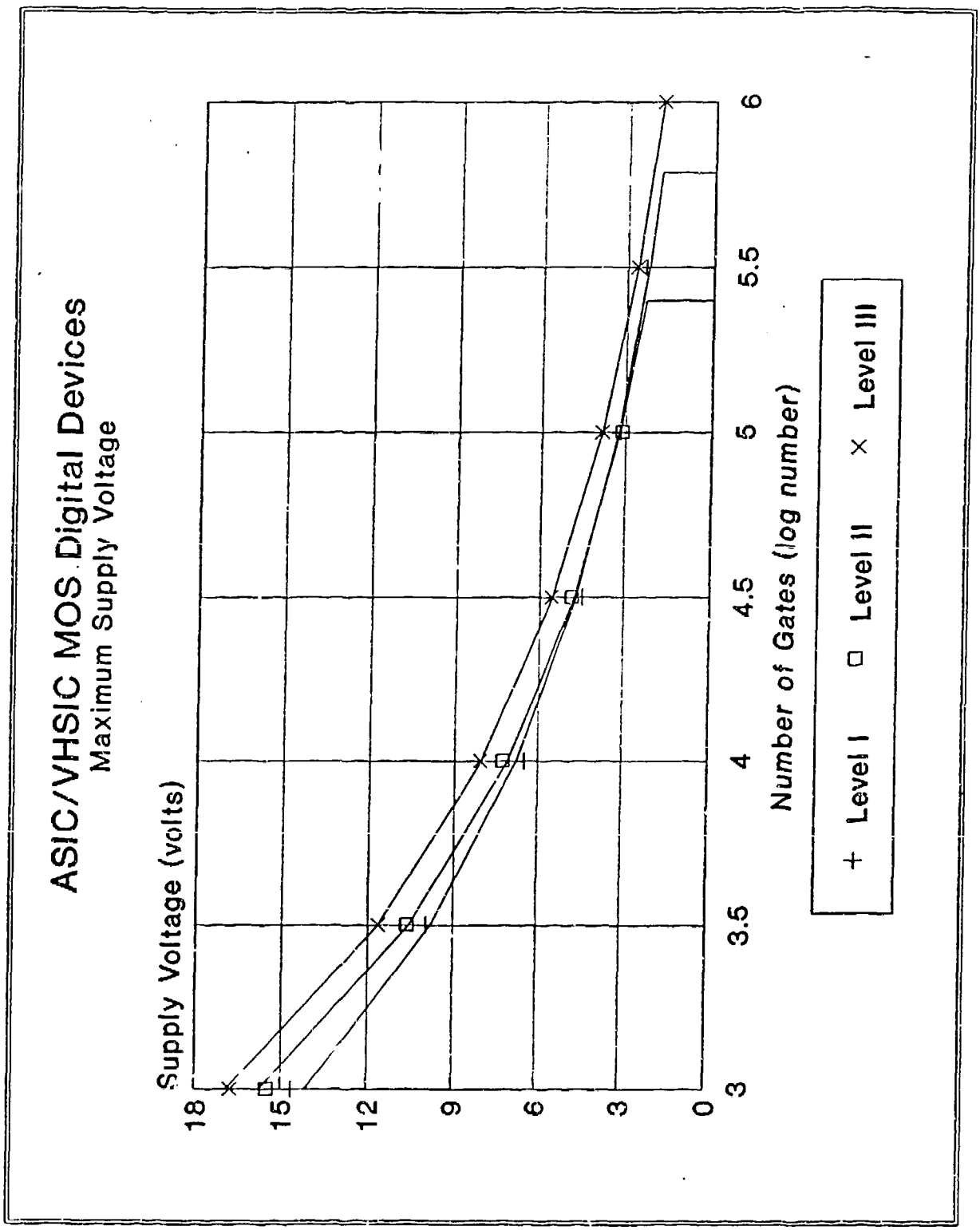


Figure 4-11 Junction Temperature Derating for Bipolar/MOS Linear ASIC/VHSIC

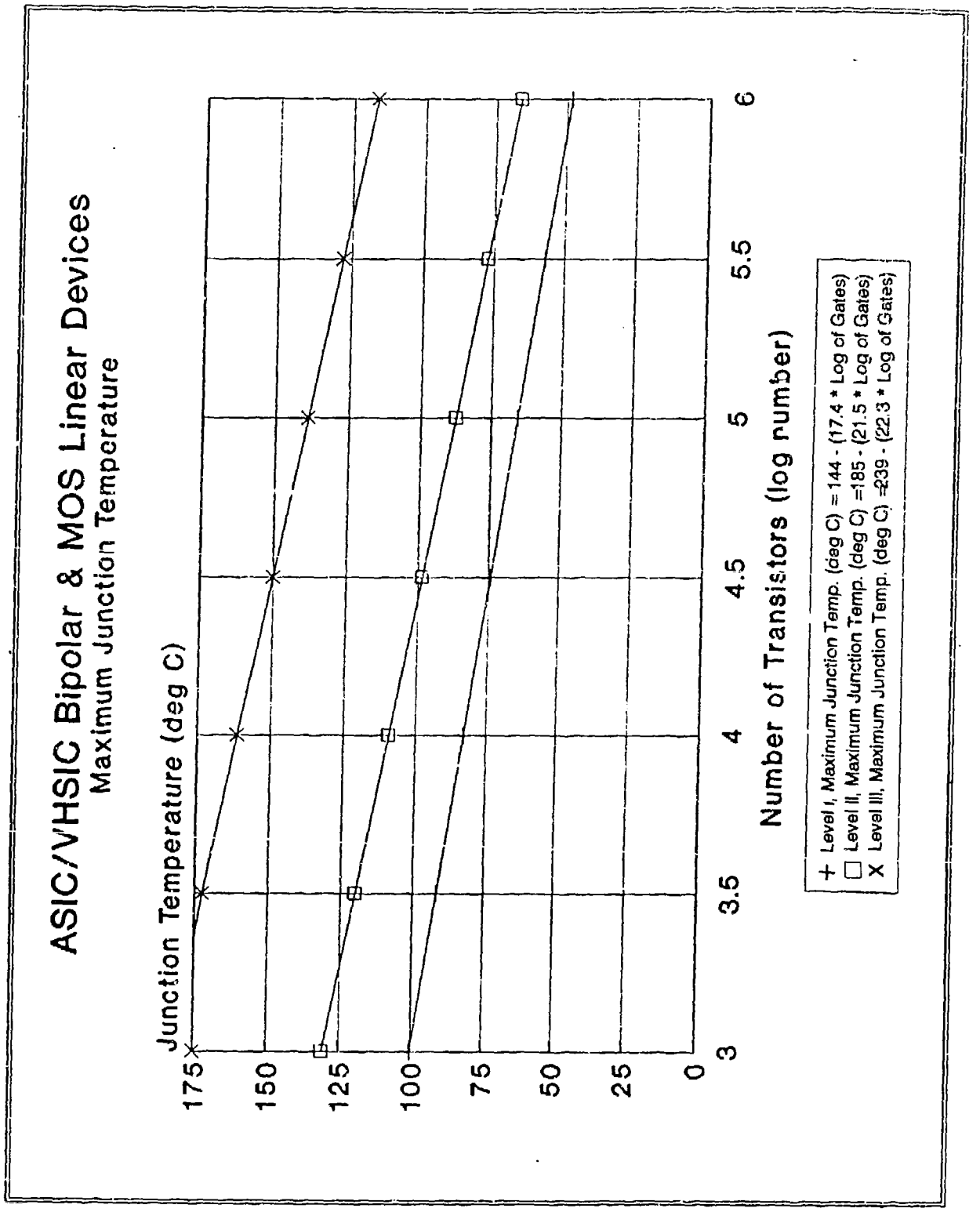


Figure 4-12 Supply Voltage Derating for MOS Linear ASIC/VHSIC

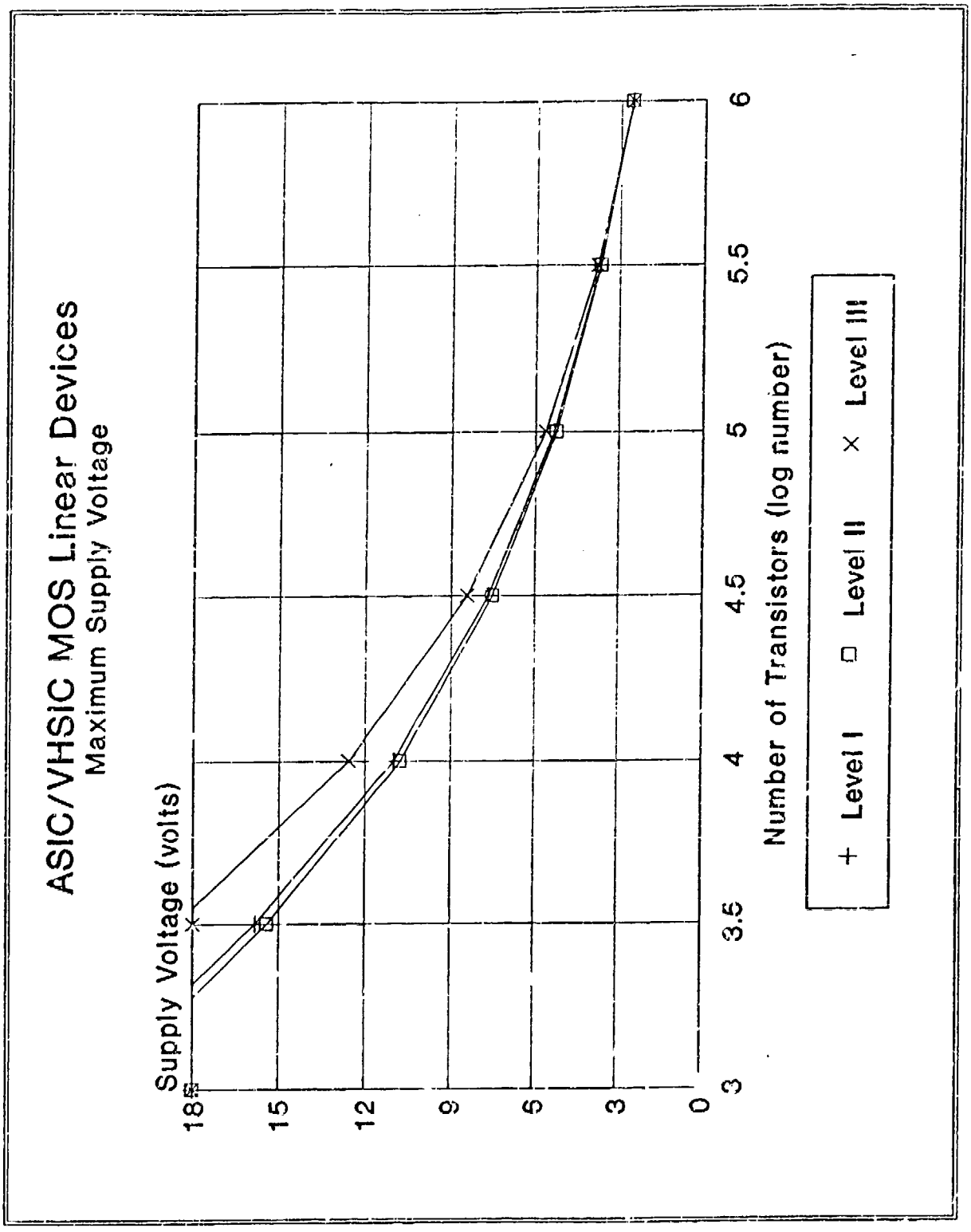
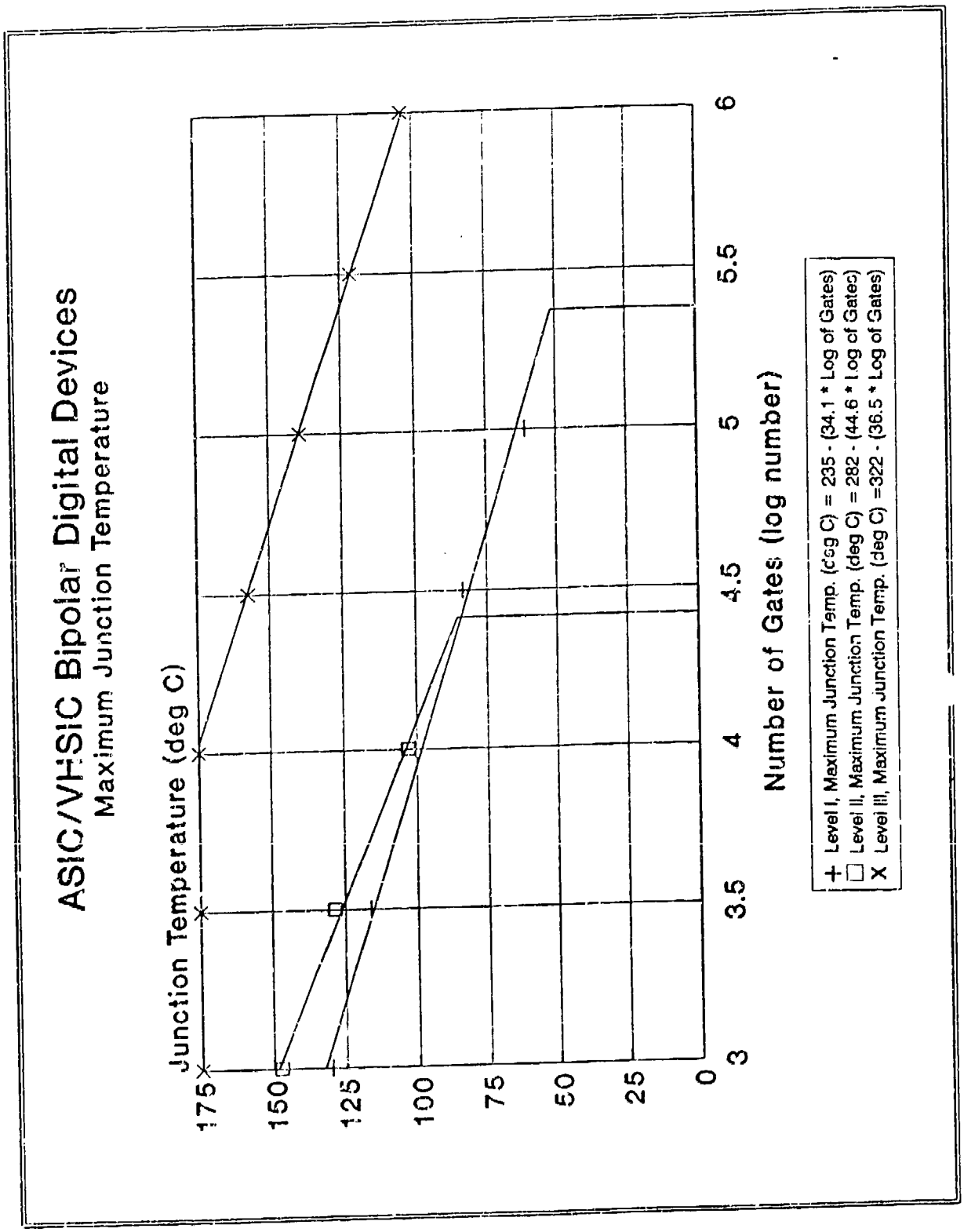


Figure 4-13 Junction Temperature Derating for Bipolar Digital ASIC/VHSIC



Supplementing the junction temperature and supply voltage derating parameters were the stress derating parameters outlined by other derating guideline sources and shown in tables 4-3, 4-4, 4-5 and 4-6 for MOS digital, MOS linear, bipolar digital and bipolar linear microcircuits. In keeping with the general approach outlined in Section 3.0, and because of the uncertainty of criticality assumed with guideline sources not specifying three criticality levels, only those guideline sources supplying derating criteria for three criticality levels were evaluated for inclusion in the updated guidelines. For each parameter specified by these guideline sources, a median value for the parameter was chosen. In the case where the choice was between an even number of values, the average of the two median values was calculated and then rounded up. Priority was given to those guidelines specifying advanced microcircuits, such as VLSI and gate arrays. The remaining guideline sources were used only as a "sanity check" of the updated stress derating criteria. Table 4-7 summarizes the new stress derating criteria for ASIC/VHSIC microcircuits.

As addressed in section 4.0, the complexity of the ASIC/VHSIC device is limited by the criticality level. Although the higher criticality level (Level I, for example) derating criteria allows a more complex device to be used, the allowed stress is typically less than the stress allowed at the lower criticality level (Level II, for example).

For MOS ASIC/VHSIC microcircuits, both maximum junction temperature and maximum supply voltage are a function of circuit complexity. Therefore, these two parameters can be combined to form effective Safe Operating Areas (SOAs) for these microcircuits. Figures 4-14, 4-15 and 4-16 display the SOAs of MOS digital microcircuits for criticality levels I, II and III, respectively. In each graph, the top set of SOAs is for a 1000 gate microcircuit, the middle set of SOAs is for a 10,000 gate microcircuit and the bottom set is for a 100,000 gate microcircuit. Multiple SOAs are displayed as part of each set of SOAs according to the required lifetime of the microcircuit. The "squareness" of the SOA indicates the level of independence of the temperature and voltage factors.

Table 4-3 ASIC/VHSIC MOS Digital Microcircuits Guidelines

CRITICALITY LEVEL	GUIDELINE	DYNAMIC SUPPLY VOLTAGE (PORV)	FREQUENCY (POMS)	OUTPUT CURRENT (FAN OUT) (PORV)	MAXIMUM JUNCTION TEMP. (deg C)	MAXIMUM OPERATING TEMP. (deg C)
I	A&B	70	80	80	85	NL
	C	75 *	80 *	70 (80) *	85 *	NL
	D	75 *	80 *	70 (80) *	85 *	NL
	E	70	80	80	85	NL
	F	100	NL	80	NL	30 C FML
II	A&B	85	80	85	100	NL
	C	80 *	80 *	75 (80) *	100 *	NL
	D	80 *	80 *	75 (80) *	100 *	NL
	E	80	80	90	100	NL
	F	100	NL	90	NL	20 C FML
III	A&B	85	90	90	110	NL
	C	85 *	80 *	80 (90) *	125 *	NL
	D	85 *	80 *	80 (90) *	125 *	NL
	E	80	90	90	110	NL
	F	100	NL	100	NL	20 C FML
NONE SPECIFIED	G	90	90	80	NL	85
	H	(Nominal)	NL	80	110	NL
	J	NL	75	80	110	NL
	K	70 *	80 *	80 *	85 *	NL
	L	(Nominal)	70	80	100	NL
	M	80	NL	80	125	NL
	W	100	50	80	65 PORV	30 C FML
	X	Vcc +/-0.5V	NL	75	125	NL

KEY:
* = Complex Microcircuits
NL = Not Listed
FML = From Maximum Limit
POMS = Percent of Maximum Specified
PORV = Percent of Rated Value

Table 4-4 ASIC/VHSIC Bipolar Digital Microcircuits Guidelines

CRITICALITY LEVEL	GUIDELINE	FIXED SUPPLY VOLTAGE	DYNAMIC SUPPLY VOLTAGE (PORV)	FREQUENCY (POMS)	OUTPUT CURRENT (FAN OUT) (PORV)	MAXIMUM JUNCTION TEMP. (deg C)	MAXIMUM OPERATING TEMP. (deg C)
I	A&B	+/- 3%	NL	80	80	85	NL
	C	+/- 3% *	NL	75 *	70 (70) *	85 *	NL
	D	NL	75 *	75 *	70 (70) *	85 *	NL
	E	+/- 3%	NL	80	80	85	NL
	F	NL	NL	NL	70	NL	30 C FML
II	A&B	+/- 5%	NL	90	85	100	NL
	C	+/- 5% *	NL	80 *	75 (75) *	100 *	NL
	D	NL	80 *	80 *	75 (75) *	100 *	NL
	E	+/- 5%	NL	90	90	100	NL
	F	NL	NL	NL	80	NL	25 C FML
III	A&B	+/- 5%	NL	95	90	110	NL
	C	+/- 5% *	NL	90 *	80 (80) *	125 *	NL
	D	NL	85 *	90 *	80 (80) *	125 *	NL
	E	Per Spec.	NL	95	90	115	NL
	F	NL	NL	NL	90	NL	20 C FML
NONE SPECIFIED	G	+/- 5%	NL (Nominal)	90	80	NL	85
	H	NL	NL	NL	80	110	NL
	J	NL	70 * (Nominal)	75	80	110	NL
	K	NL	NL	80 *	80 *	85 *	NL
	L	NL	NL	70	80	100	NL
	M	10 %	NL	NL	80	125	NL
	W	+/- 5%	NL	50	80	85 POrtV	30 C FML
	X	+/- 0.5V	NL	NL	75	125	NL

KEY:
* = Complex Microcircuits
NL = Not Listed
FML = From Maximum Limit
POMS = Percent of Maximum Specified
PORtV = Percent of Rated Value

Table 4-5 ASIC/VHSIC MOS Linear Microcircuits Guidelines

CRITICALITY LEVEL	GUIDE-LINES	SUPPLY VOLTAGE (PORV)	INPUT VOLTAGE (PORV)	FREQ. (POMS)	OUTPUT CURRENT (FAN OUT) (PORV)	POWER DISSIPATION (PORV)	MAX. JUNCT. TEMP. (deg C)	MAX. OP. TEMP. (deg C)
I	A&B	70	60	NL	70	NL	80	NL
	C	75 *	NL	80 *	70 (80) *	NL	85 *	NL
	D	75 *	NL	80 *	70 (80) *	NL	85 *	NL
	E	70	60	NL	70	NL	80	NL
	F	80	60	NL	NL	55	NL	30 C FML
II	A&B	80	70	NL	75	NL	95	NL
	C	80 *	70 *	NL	75 (80) *	NL	95 *	NL
	D	80 *	NL	80 *	75 (80) *	NL	100 *	NL
	E	80	70	NL	80	NL	95	NL
	F	80	60	NL	NL	80	NL	25 C FML
III	A&B	80	70	NL	80	NL	105	NL
	C	80 *	70 *	NL	80 (90) *	NL	105 *	NL
	D	85 *	NL	80 *	80 (90) *	NL	125 *	NL
	E	80	70	NL	80	NL	105	NL
	F	80	60	NL	NL	90	NL	20 C FML
NONE SPECIFIED	G	90	90	NL	80	75	NL	85
	H	85	80	NL	70	NL	110	NL
	J	70	70	75	75	60	110	NL
	K	80 **	100	NL	80	75 **	100	NL
	L	(Nominal)	75	NL	70	50	NL	125
	M	NL	80	85	85	85	125	NL
	W	80	85	50	75	NL	60 PORV	30 C FML
	X	75	75	NL	NL	NL	125	NL

KEY: * = Complex Microcircuits
** = Worst case; slight variations likely depending on device type

FML = From Maximum Limit
POMS = Percent of Maximum Specified
PORV = Percent of Rated Value
NL = Not Listed

Table 4-6 ASIC/VHSIC Bipolar Linear Microcircuits Guidelines

CRITICALITY LEVEL	GUIDELINE	SUPPLY VOLTAGE (PORV)	INPUT VOLTAGE (PORV)	FREQUENCY (POMB)	OUTPUT CURRENT (FAN OUT) (PORV)	POWER DISSIPATION (PORV)	MAXIMUM JUNCTION TEMP. (deg C)	MAXIMUM OPERATING TEMP. (deg C)
I	A&B	70	60	NL	70	NL	80	NL
	C	+/- 3% *	NL	75 *	70 (70) *	NL	85 *	NL
	D	75 *	NL	75 *	70 (70) *	NL	85 *	NL
	E	70	60	NL	70	NL	80	NL
	F	80	60	NL	NL	55	NL	30 C FML
II	A&B	80	70	NL	75	NL	95	NL
	C	+/- 5% *	70 *	NL	75 (75) *	NL	95 *	NL
	D	80 *	NL	80 *	75 (75) *	NL	100 *	NL
	E	80	70	NL	80	NL	95	NL
	F	80	60	NL	NL	80	NL	25 C FML
III	A&B	80	70	NL	80	NL	105	NL
	C	+/- 5% *	70 *	NL	80 (80) *	NL	105 *	NL
	D	85 *	NL	90 *	80 (80) *	NL	125 *	NL
	E	80	70	NL	80	NL	105	NL
	F	80	60	NL	NL	90	NL	20 C FML
NONE SPECIFIED	G	80	70	NL	80	75	NL	85
	H	75	80	NL	70	NL	110	NL
	J	70	70	75	75	60	110	NL
	K	80 **	100	NL	80	75 **	100	NL
	L	(Nominal)	75	NL	70	50	NL	125
	M	NL	80	85	85	85	125	NL
	W	80	65	50	75	NL	60 PORV	30 C FML
	X	75	75	NL	NL	NL	125	NL

KEY:

* = Complex Microcircuits
NL = Not Listed
FML = From Maximum Limit
POMB = Percent of Maximum Specified
PORV = Percent of Rated Value
** = Worst case; slight variations likely depending on device type

Table 4-7 ASIC/VHSIC Stress Derating Criteria

Classification	Derating Parameter	Level I	Level II	Level III
MOS Digital	(1) Supply Voltage (volts)	129 / (G ** 0.320)	173 / (G ** 0.347)	157 / (G ** 0.323)
	Frequency (PCMS)	90	80	80
	Output Current, Fan Out, (PORV)	70 (80)	75 (80)	80 (90)
Figure 4-9	(2) Maximum Junction Temp. (deg C)	60	121	125
page 44	Circuit Complexity - Maximum Gates	60,000	60,000	60,000
MOS Linear	(1) Supply Voltage (volts)	200 / (TR ** 0.315)	189 / (TR ** 0.311)	210 / (TR ** 0.347)
	Input Voltage (PORV)	60	70	70
	Frequency (PCMS)	80	80	80
	Output Current, Fan Out, (PORV)	70 (80)	75 (80)	80 (90)
Figure 4-11	(2) Maximum Junction Temp. (deg C)	83	109	125
page 46	Circuit Complexity - Maximum Trans.	10,000	10,000	10,000
Bipolar Digital	(1) Supply Voltage (volts)	+/- 3%	+/- 5%	+/- 5%
	Frequency (PCMS)	75	80	90
	Output Current, Fan Out, (PORV)	70 (70)	75 (75)	80 (80)
Figure 4-13	(2) Maximum Junction Temp. (deg C)	72	85	125
page 48	Circuit Complexity - Maximum Gates	60,000	26,000	60,000
Bipolar Linear	(1) Supply Voltage (volts)	+/- 3%	+/- 5%	+/- 5%
	Input Voltage (PORV)	60	70	70
	Frequency (PCMS)	75	80	90
	Output Current, Fan Out, (PORV)	70 (70)	75 (75)	80 (80)
Figure 4-11	(2) Maximum Junction Temp. (deg C)	83	109	125
page 46	Circuit Complexity - Maximum Trans.	10,000	10,000	10,000

KEY: G = Number of Gates
LG = Log (base 10) of TR
TR = Number of Transistors
PORV = Percent of Rated Value
* = Multiplied By

LTR = Log (base 10) of TR
PCMS = Percent of Maximum Specified
** = Taken to the Power of
(1) Not to exceed supplier minimum or maximum rating
(2) Not to exceed 125 deg C or supplier maximum
(whichever is the smaller of the two)

Figure 4-14 Criticality Level I SOA for MOS Digital ASIC/VHSIC

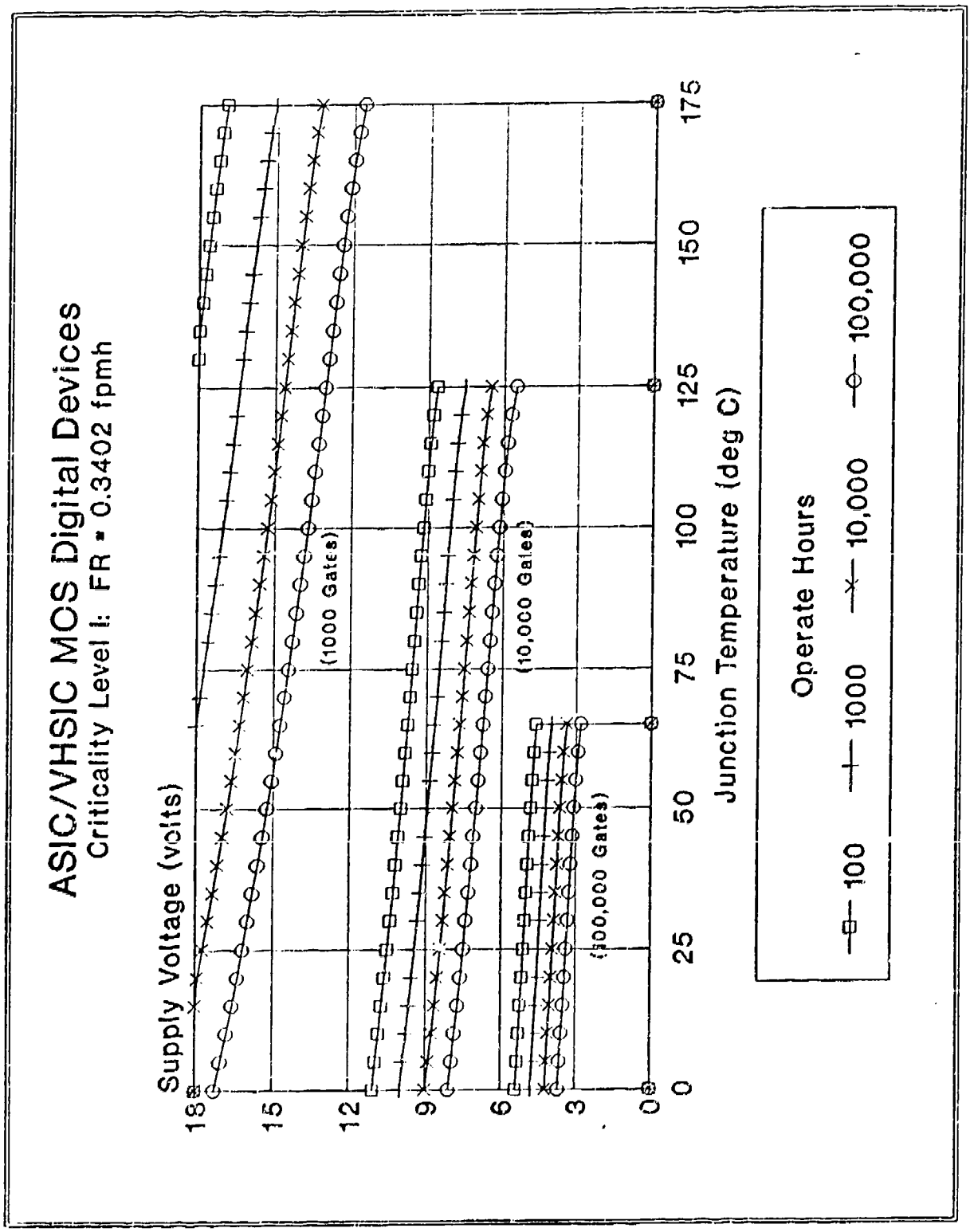


Figure 4-15 Criticality Level II SOA for MOS Digital ASIC/VHSIC

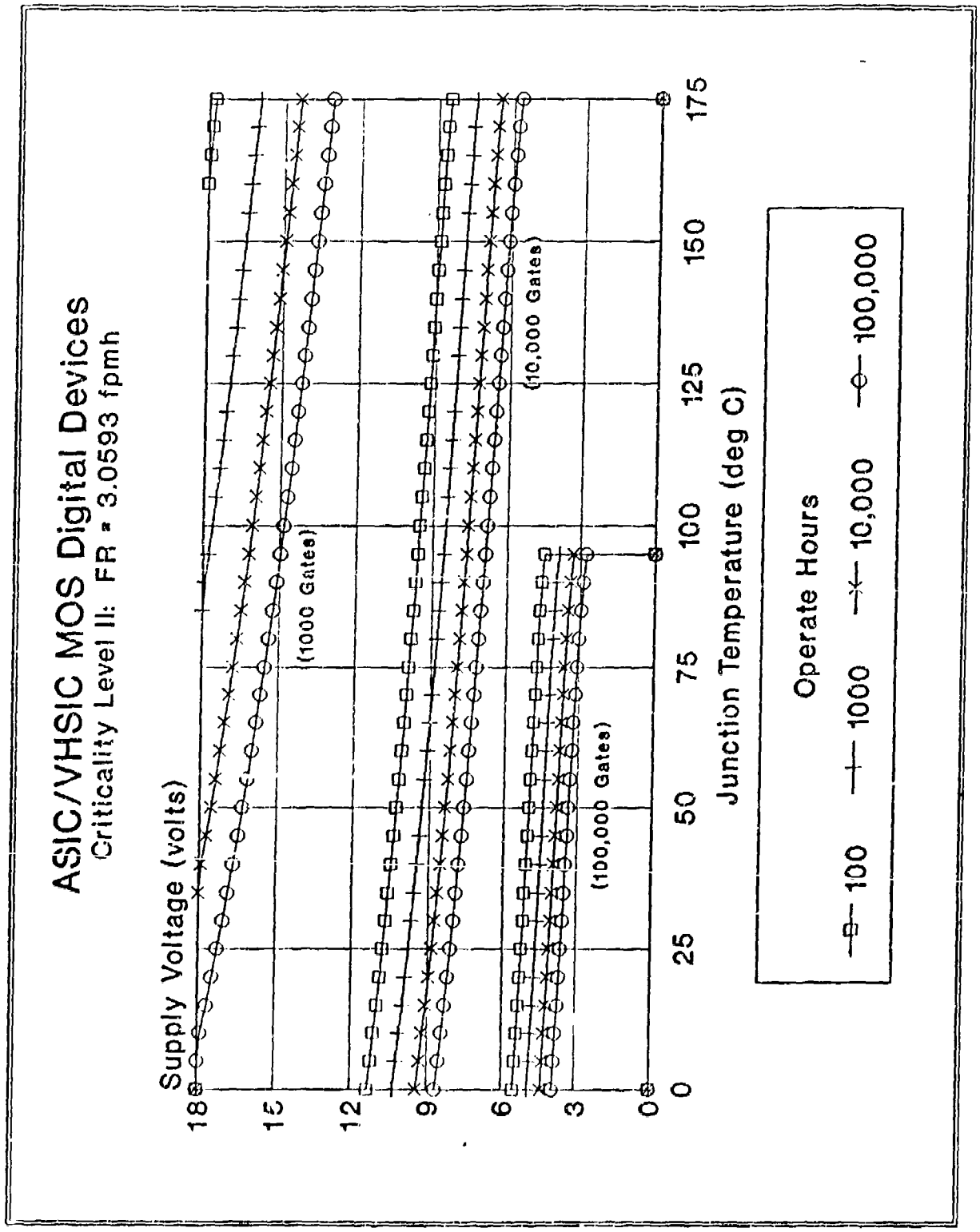
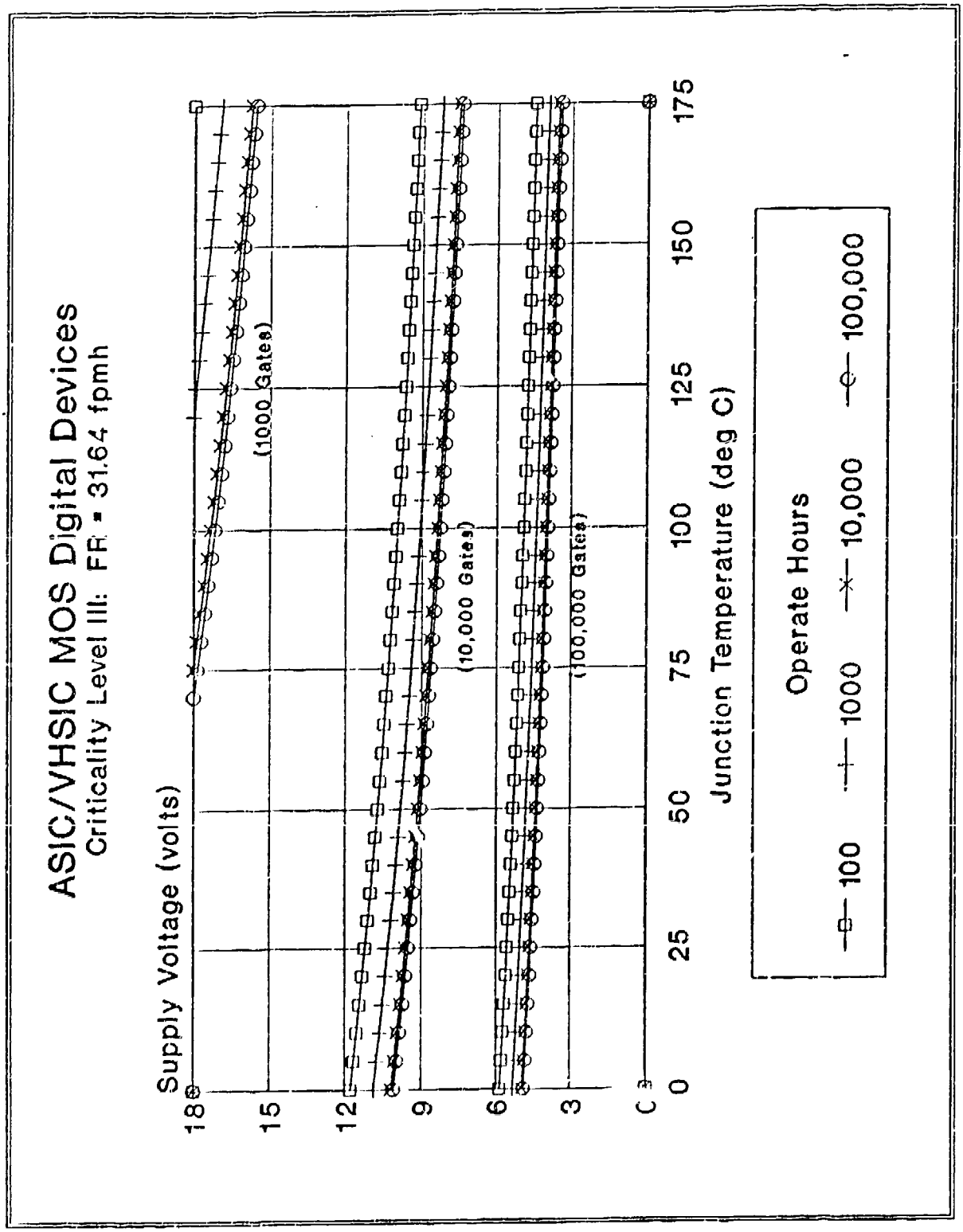


Figure 4-16 Criticality Level III SOA for MOS Digital ASIC/VHSIC



4.2 MICROPROCESSOR MICROCIRCUITS

The stress derating criteria for microprocessors was developed similarly to the ASIC/VHSIC microcircuits, with two exceptions. First, the lack of stress-failure data and reliability models for bipolar or MOS linear microprocessors precluded the development of derating criteria for these technologies. Second, the circuit complexity factor, C1, in the RA/AAT failure rate model was a function of bit count. Therefore, stress derating tables were generated for the three categories of microprocessors, 8-, 16- and 32-bit, for both MOS digital and bipolar digital technologies. The differences between the criteria in each table were the results of applying the different device-specific attributes and stress-specific parameters to the failure rate equation. These attributes and parameters included temperature activation energy (PiT), circuit complexity (C1), number of package pins (C2), total transistor gate area (L_{TDDB}) and dielectric thickness (L_{TDDB}). The values or equations used in evaluating the device/stress-specific attributes are outlined in table 4-8.

Table 4-8 Microprocessor Device/Stress-Specific Attributes

Technology	Attribute	Value / Equation
MOS Digital	Ea	0.35 eV
	C1	0.14
	C1	0.28
	C1	0.56
	Pins	11.07 * GATES ** 0.342
	C2	2.8E-4 * PINS ** 1.08
	Transistor Gate Area	4047 * TRANS ** 0.463 (sq um)
	Dielectric Thickness	28.18 / TRANS ** 0.412 (kA)
Bipolar Digital	Ea	0.60 eV
	C1	0.06
	C1	0.12
	C1	0.24
	Pins	9.16 * GATES ** 0.377
	C2	2.8E-4 * PINS ** 1.08

The temperature activation energies and C1 factor values were obtained directly from the tables provided by the RA/AAT final report. The relationships between pin count and circuit complexity for MOS digital and bipolar digital microprocessors are the same as the relationships associated with MOS digital and bipolar digital ASIC/VHSIC microcircuits, respectively. The circuit complexity dependence of total transistor gate area and dielectric thickness for MOS digital microprocessors are shown in figures 4-17 and 4-18, respectively.

By applying the approach outlined in Section 4.0, maximum junction temperatures and maximum supply voltages (MOS) were calculated for the two microprocessor technologies, three bit counts each, as a function of circuit complexity. Figures 4-19 and 4-20, figures 4-21 and 4-22 and figures 4-23 and 4-24 are the junction temperature and supply voltage derating curves for MOS digital microprocessors of 8-, 16- and 32-bit complexities, respectively. Figures 4-25, 4-26 and 4-27 are the junction temperature derating curves for 8-, 16- and 32-bit bipolar digital microprocessors, respectively. The solid lines on the graphs in each figure represent the best least squares fit to the calculated derating values. These equations of the lines are the new stress derating criteria for each criticality level.

It is noted here that a review of the range of complexities within each category of microprocessor showed the transistor counts varied marginally for 8-bit microprocessors (22,000 to 27,000 transistors) as compared to 16-bit (30,000 to 120,000 transistors) and 32-bit (80,000 to 1,000,000 transistors) microprocessors. Therefore, an approximate worst case 8-bit microprocessor complexity of 10,000 gates was assumed and the stress derating equations for 8-bit microprocessors were changed to the values of those equations at the 10,000 gate complexity.

Supplementing the junction temperature and supply voltage derating parameters were the stress derating parameters outlined by other derating guideline sources as shown in tables 4-9 and 4-10 for MOS digital

microprocessors and bipolar digital microprocessors, respectively. In keeping with the general approach outlined in Section 3.0, and because of the uncertainty of criticality assumed with guideline sources not specifying three criticality levels, the method for evaluating the stress derating criteria for microprocessors was the same as the method used for evaluating the stress derating criteria for ASIC/VHSIC microcircuits. Table 4-11 summarizes the new stress derating criteria for microprocessors.

Figure 4-17 Transistor Gate Area for MOS Digital Microprocessors[1]

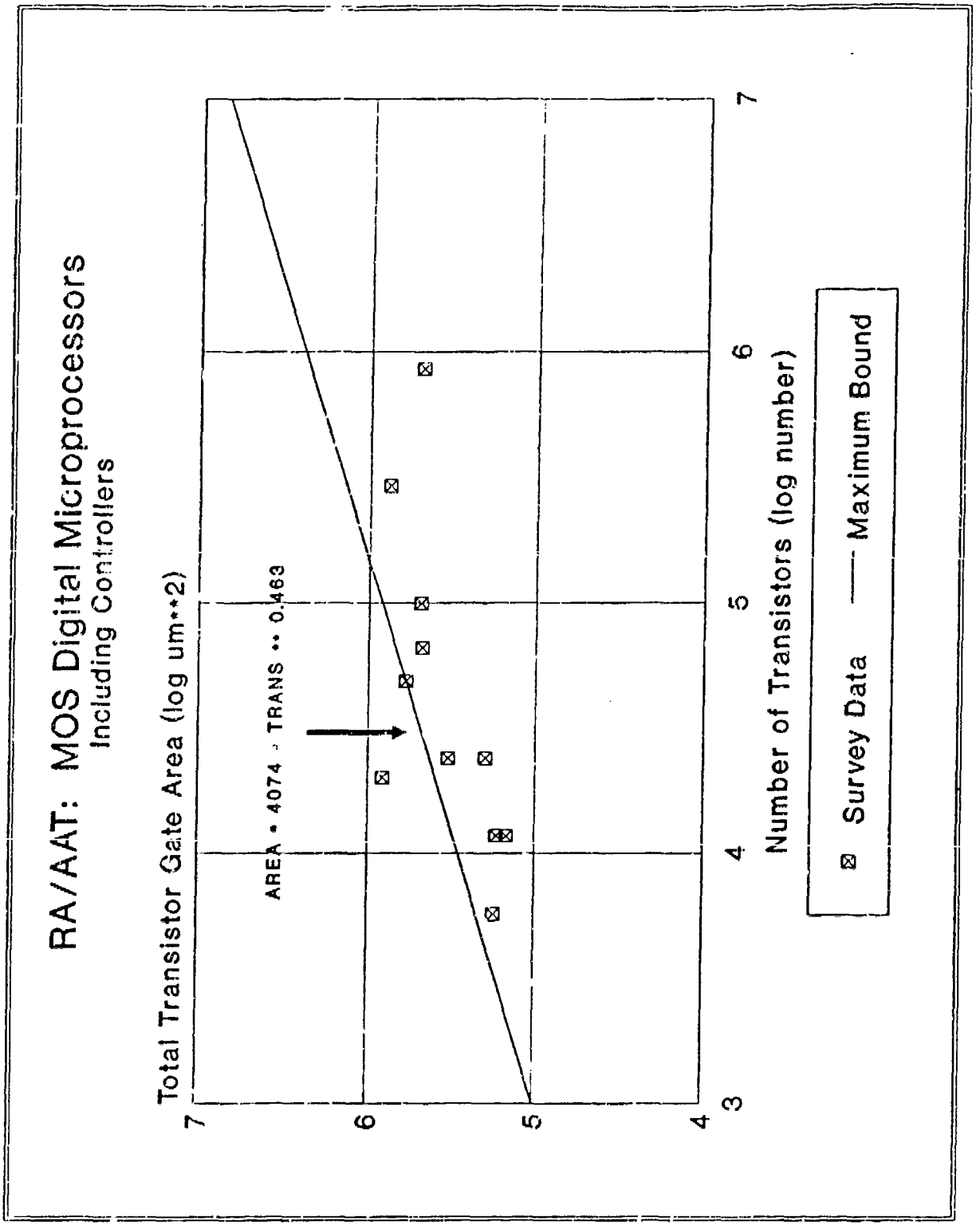


Figure 4-18 Dielectric Thickness for MOS Digital Microprocessors[1]

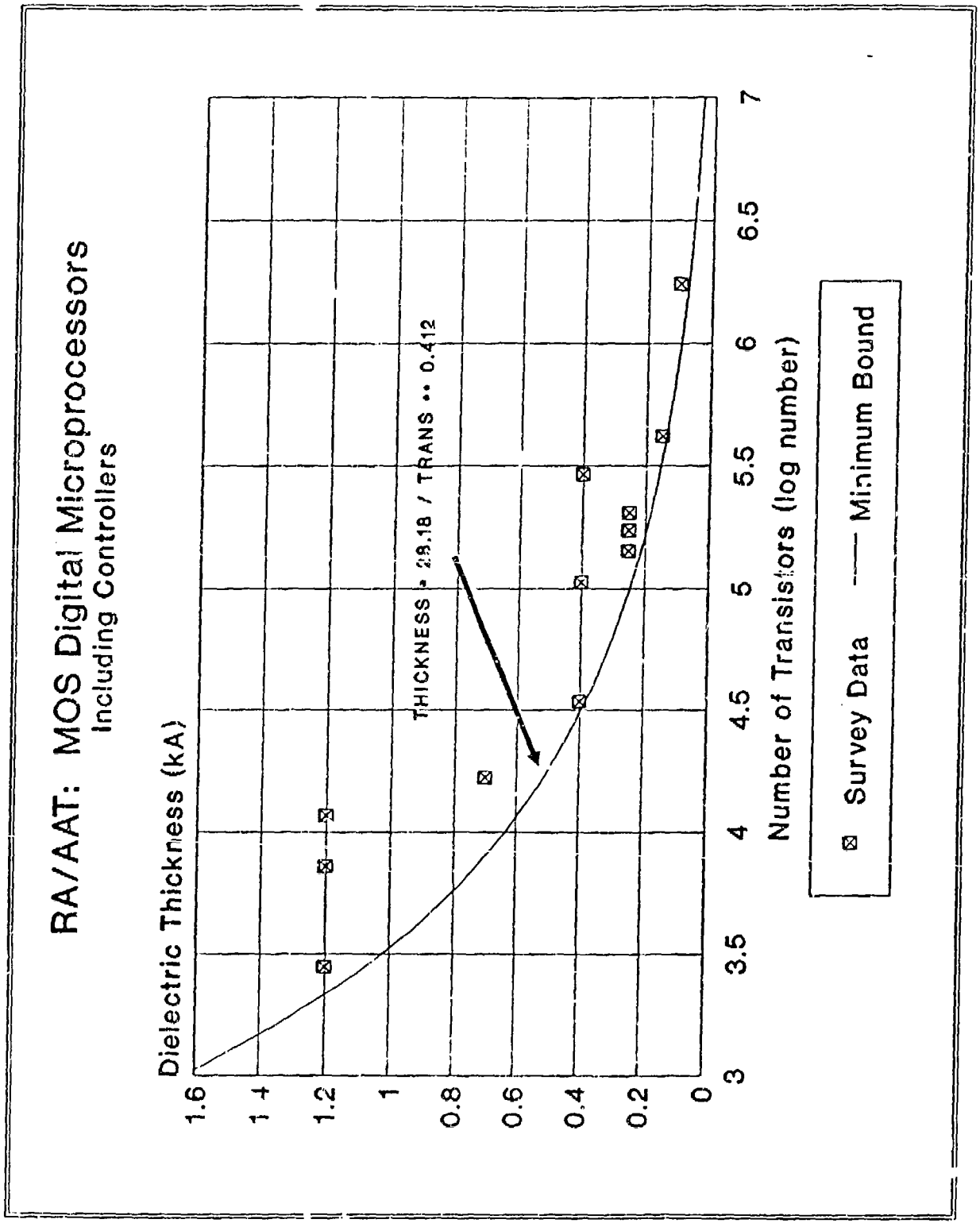


Figure 4-19 Junction Temperature Derating for 8-Bit MOS Digital Microprocessors

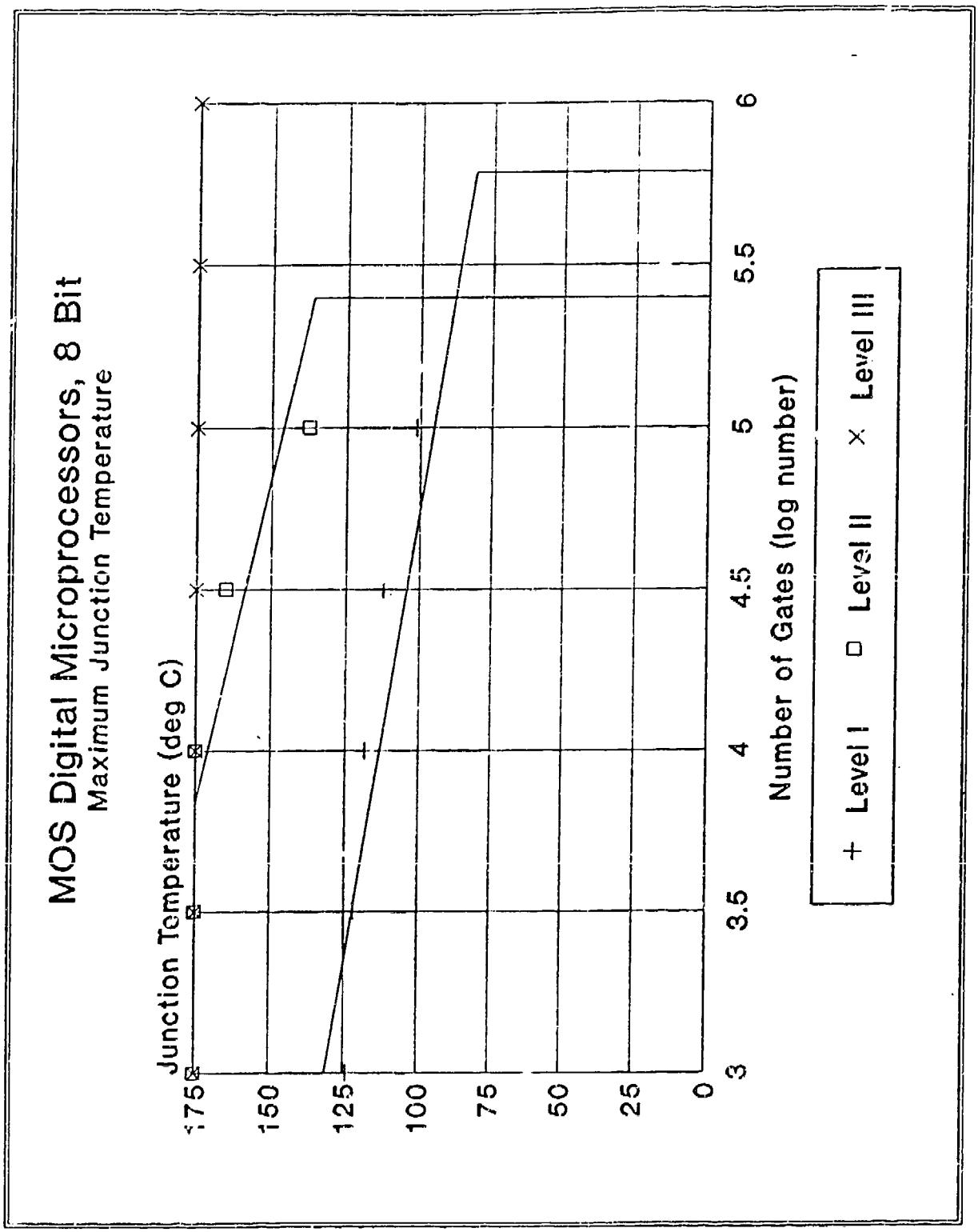


Figure 4-20 Supply Voltage Derating for
8-Bit MOS Digital Microprocessors

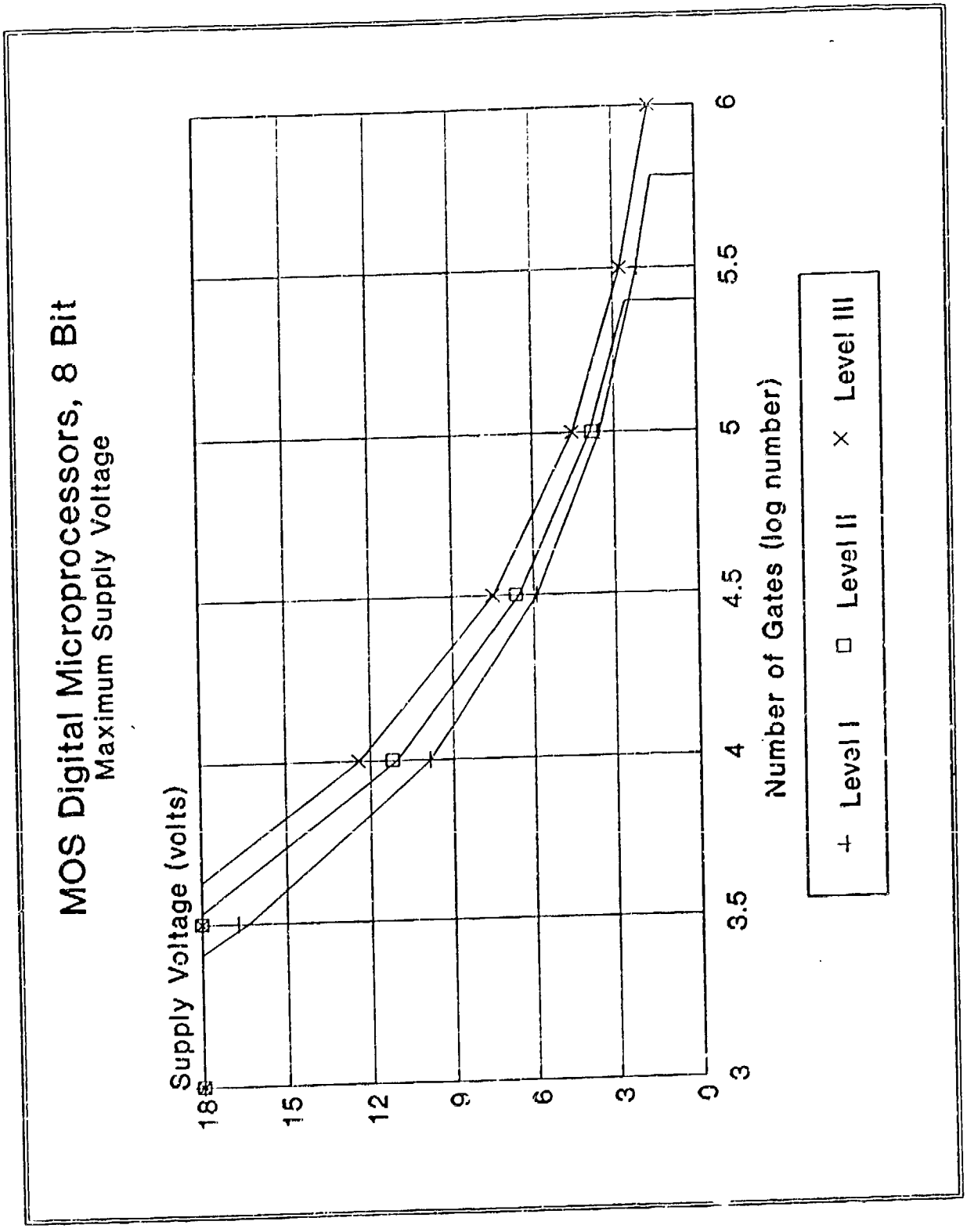


Figure 4-21 Junction Temperature Derating
for 16-Bit MOS Digital Microprocessors

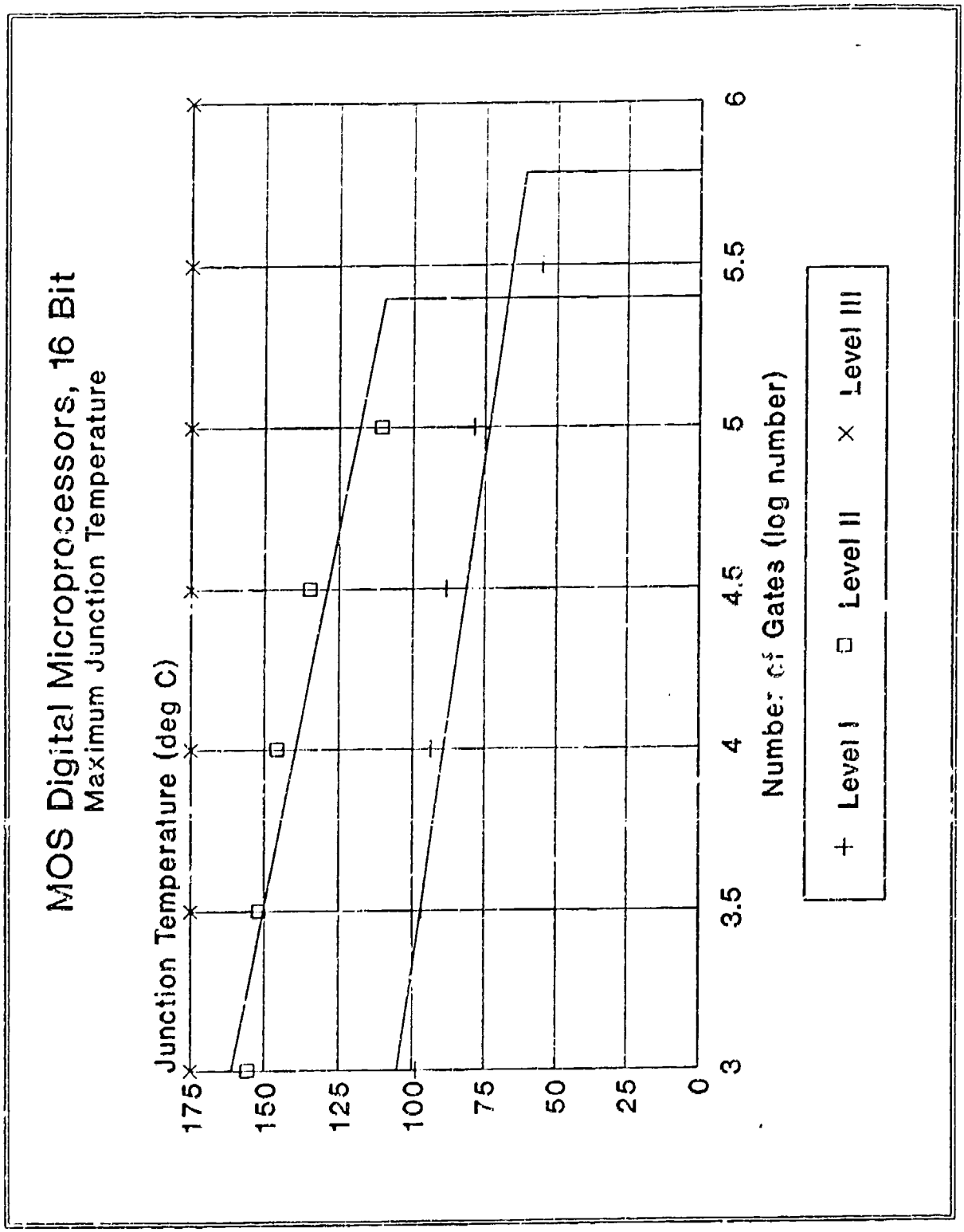


Figure 4-22 Supply Voltage Derating
for 16-Bit MOS Digital Microprocessors

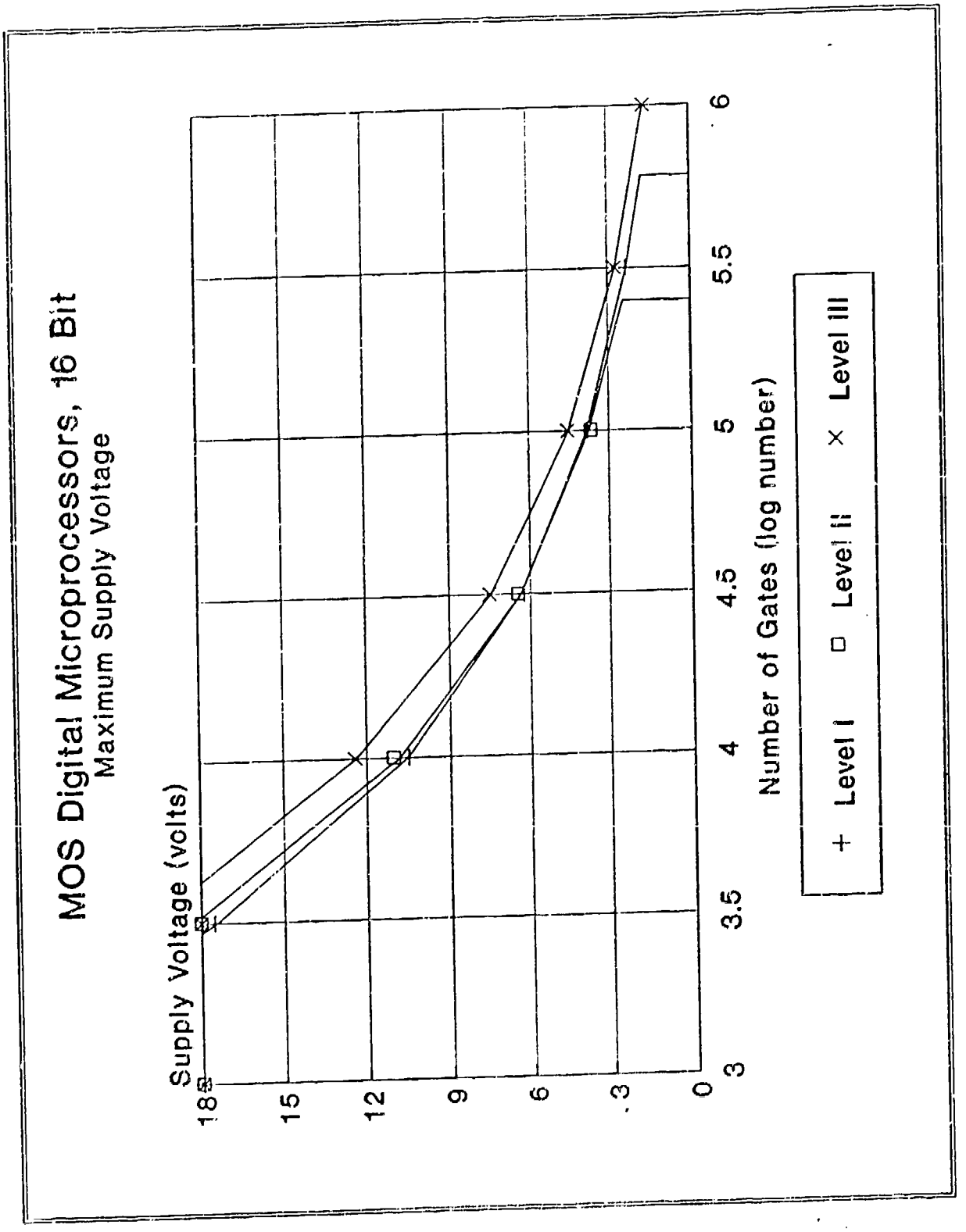


Figure 4-23 Junction Temperature Derating
for 32-Bit MOS Digital Microprocessors

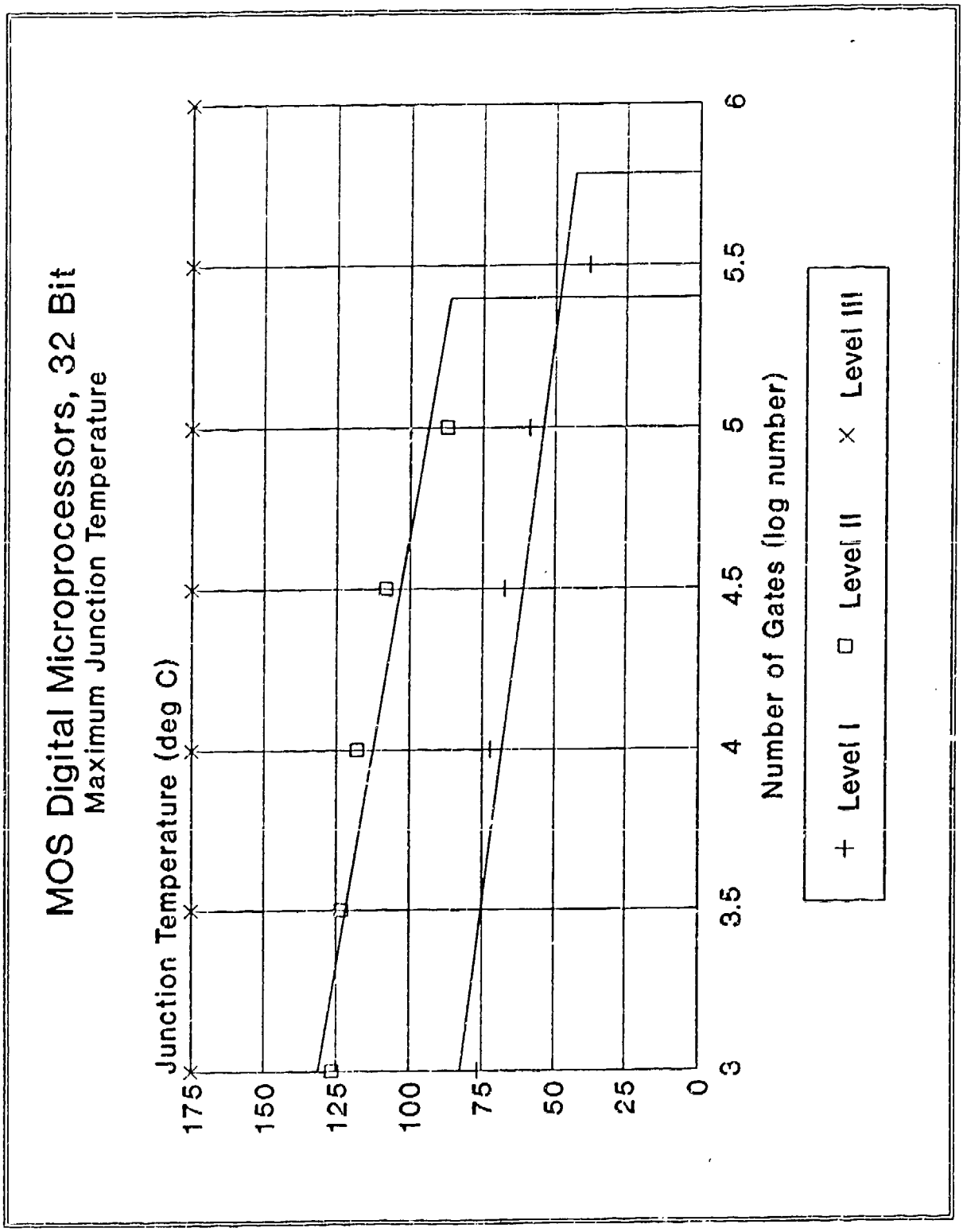


Figure 4-24 Supply Voltage Derating
for 32-Bit MOS Digital Microprocessors

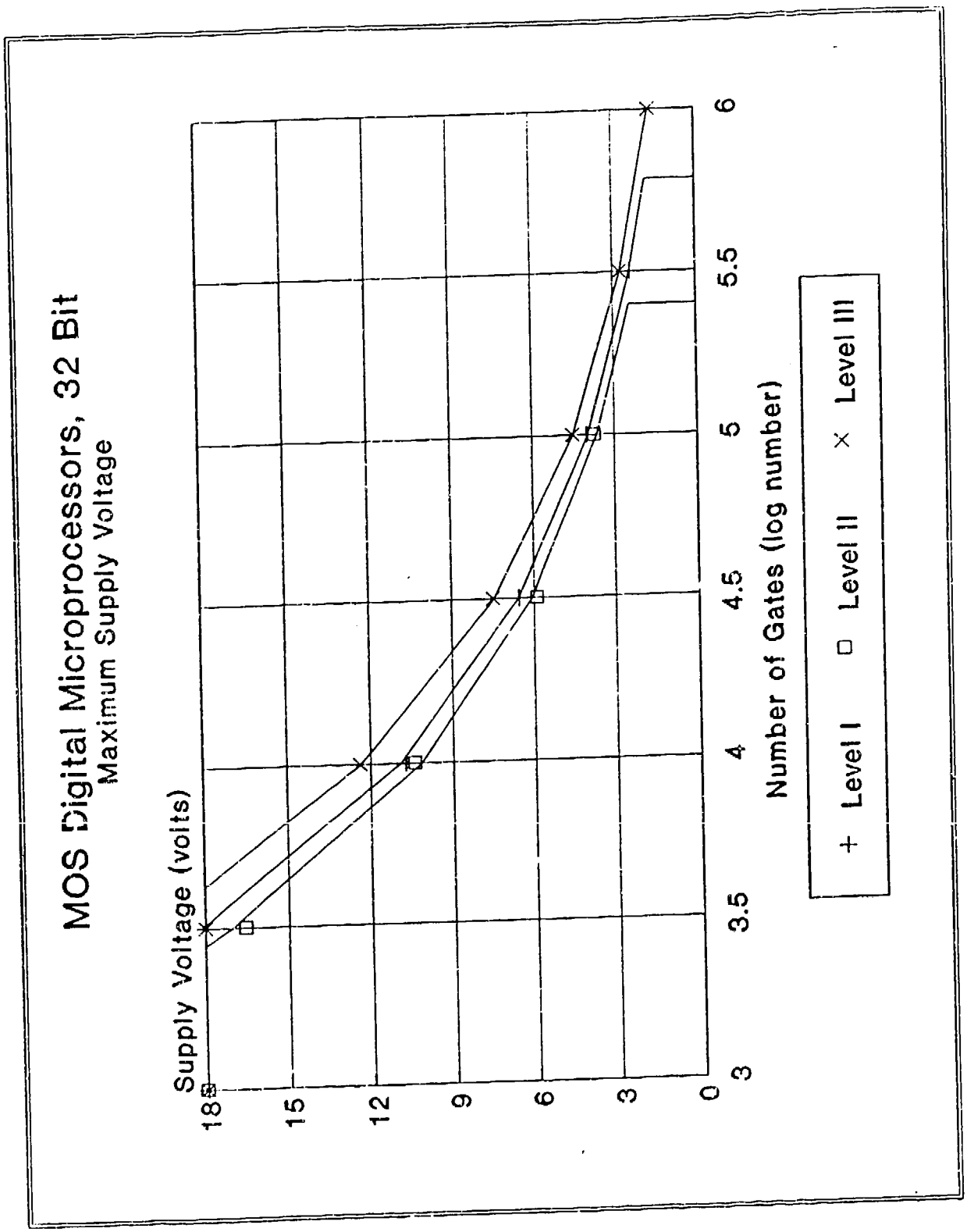


Figure 4-25 Junction Temperature Derating
for 8-Bit Bipolar Digital Microprocessors

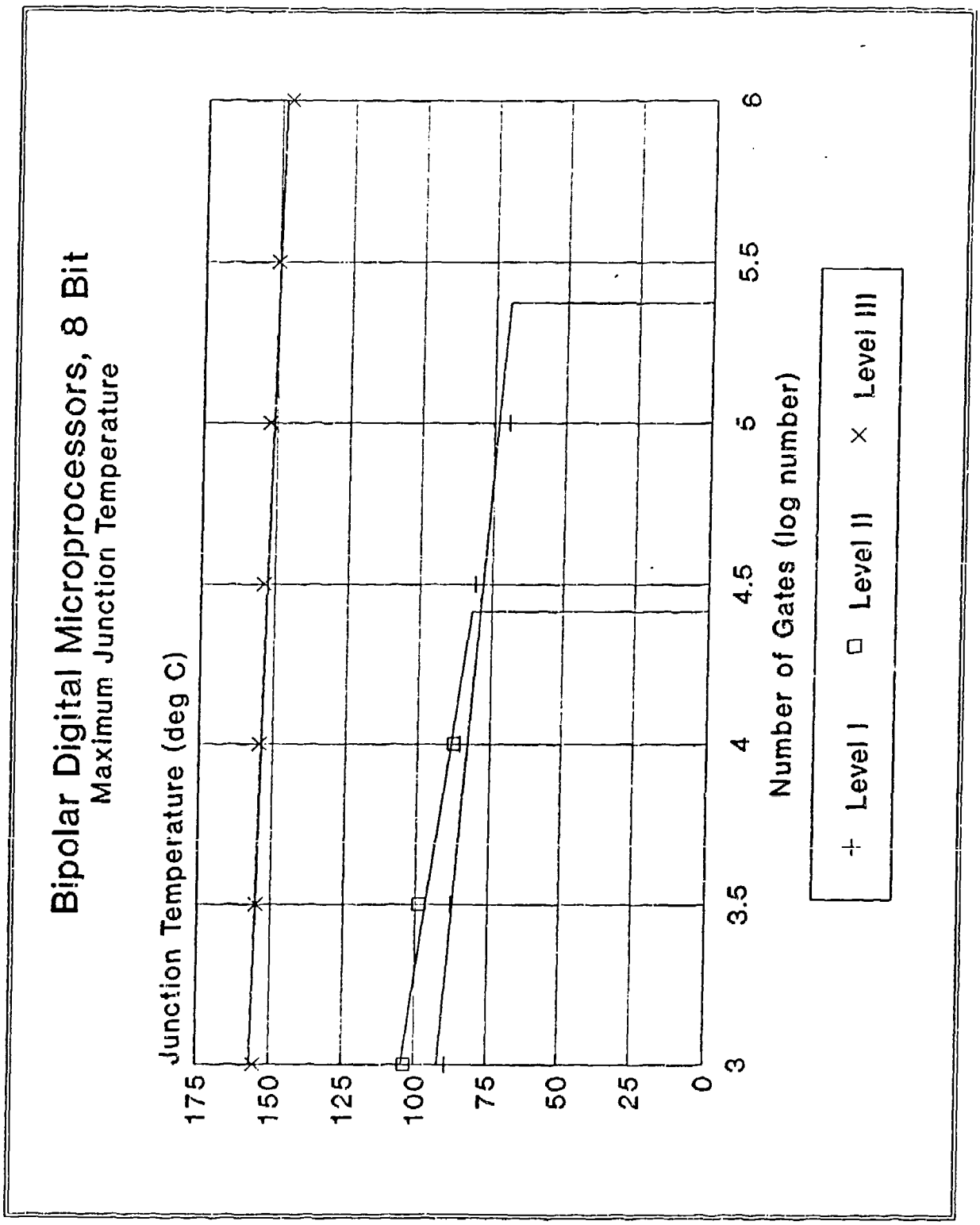


Figure 4-26 Junction Temperature Derating
for 16-Bit Bipolar Digital Microprocessors

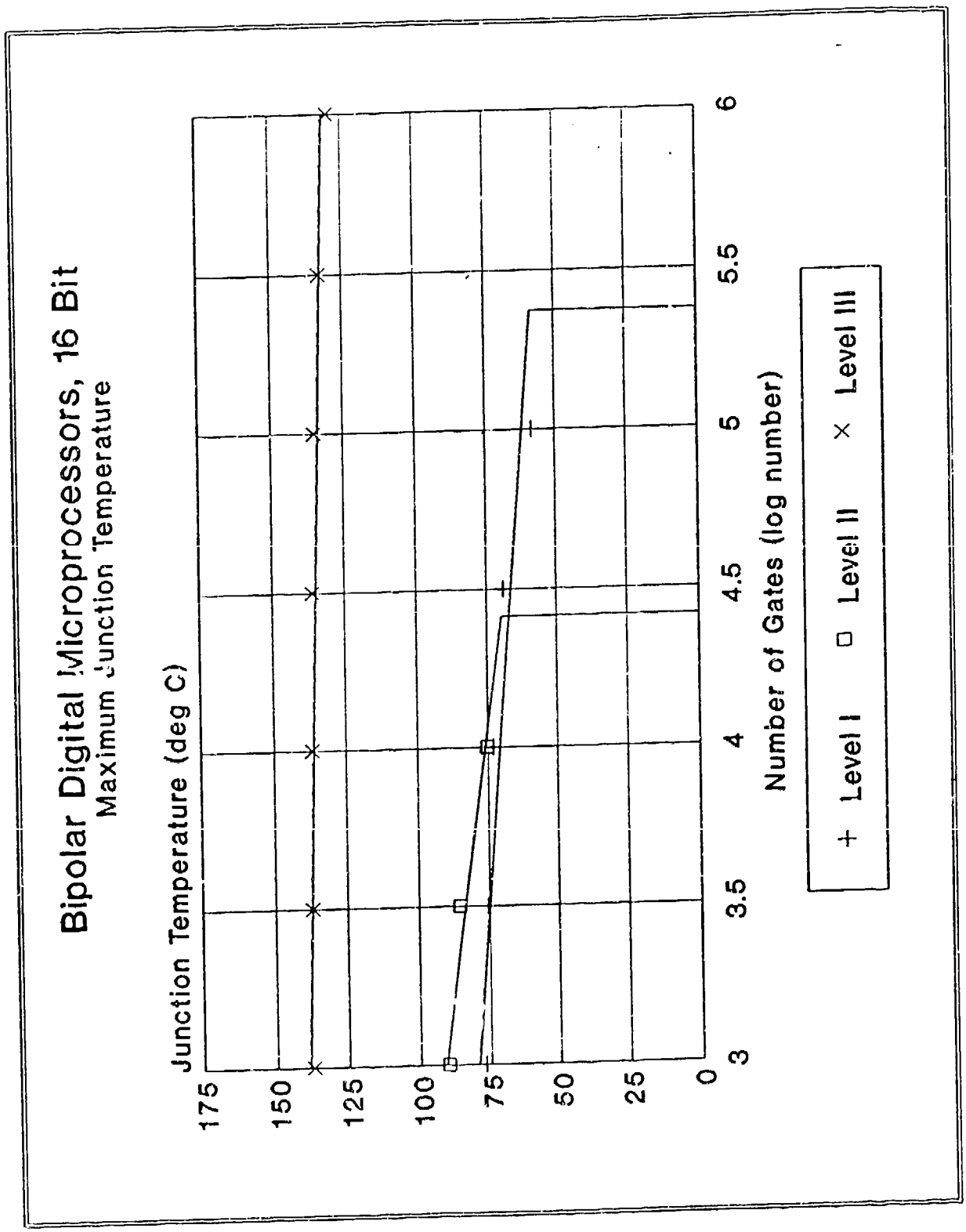


Figure 4-27 Junction Temperature Derating
for 32-Bit Bipolar Digital Microprocessors

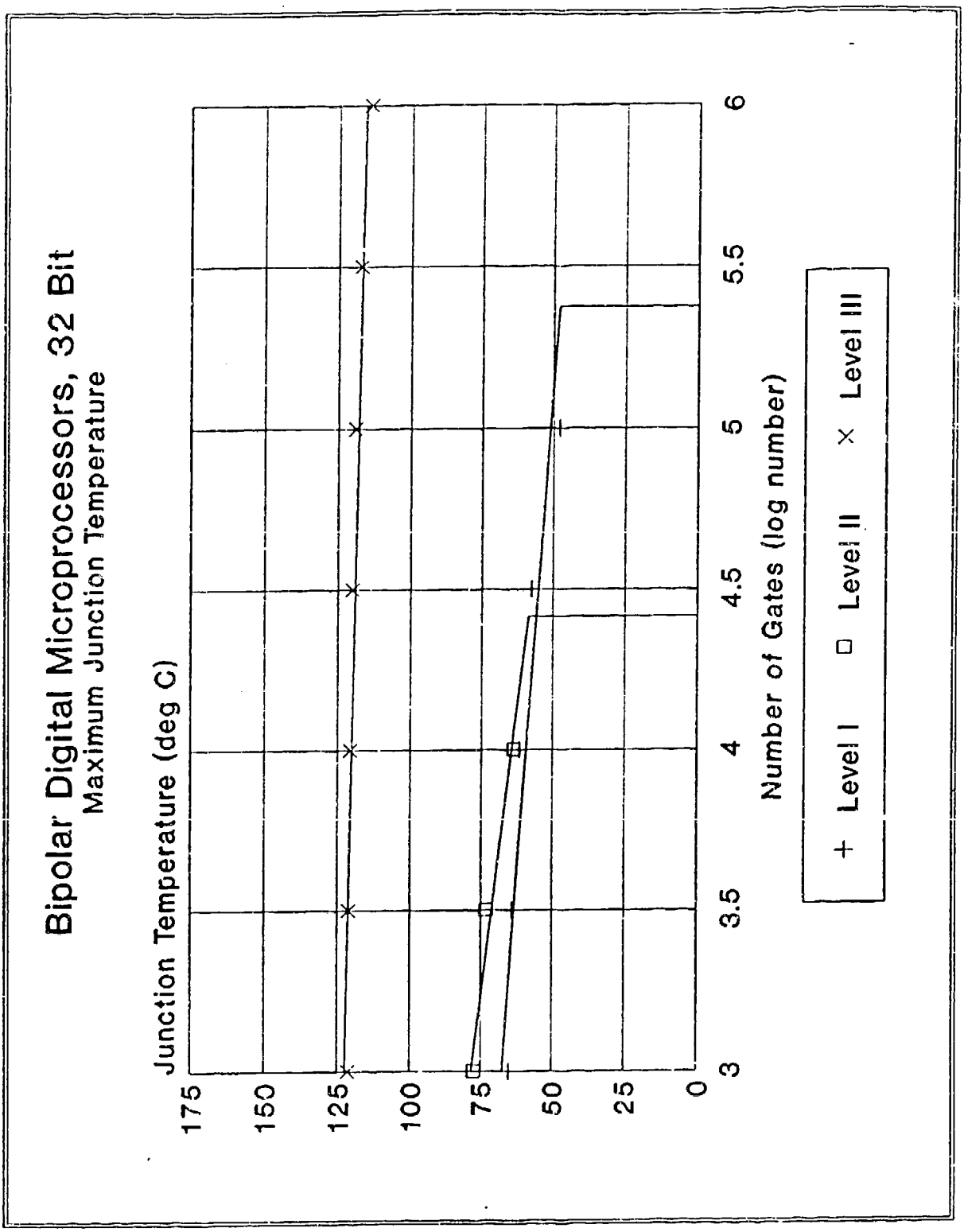


Table 4-9 MOS Microprocessor Guidelines

CRITICALITY LEVEL	GUIDELINE	DYNAMIC SUPPLY VOLTAGE (PORV)	FREQUENCY (POMS)	OUTPUT CURRENT (FAN OUT) (PORV)	MAXIMUM JUNCTION TEMP. (deg C)	MAXIMUM OPERATING TEMP. (deg C)
I	A&B	70	80	80	85	NL
	C	75 *	80 *	70 (80) *	85 *	NL
	D	75 *	80 *	70 (80) *	85 *	NL
	E	70	80	80	85	NL
	F	100	NL	80	NL	30 C FML
II	A&B	85	80	85	100	NL
	C	80 *	80 *	75 (80) *	100 *	NL
	D	80 *	80 *	75 (80) *	100 *	NL
	E	80	80	90	100	NL
	F	100	NL	90	NL	20 C FML
III	A&B	85	90	90	110	NL
	C	85 *	80 *	80 (90) *	125 *	NL
	D	85 *	80 *	80 (90) *	125 *	NL
	E	80	90	90	110	NL
	F	100	NL	100	NL	20 C FML
NONE SPECIFIED	G	NL	90	NL	NL	85
	H	(Nominal)	NL	80	110	NL
	J	NL	75	80	110	NL
	K	70 *	80 *	80 *	85 *	NL
	L	(Nominal)	70	80	100	NL
	M	80	NL	80	125	NL
	W	100	50	80	65 PORV	30 C FML
	X	Vcc +/-0.5V	NL	75	125	NL

KEY:
* = Complex Microcircuits
NL = Not Listed
FML = From Maximum Limit
POMS = Percent of Maximum Specified
PORV = Percent of Rated Value

Table 4-10 Bipolar Microprocessor Guidelines

CRITICALITY LEVEL	GUIDELINE	FIXED SUPPLY VOLTAGE	DYNAMIC SUPPLY VOLTAGE (PORV)	FREQUENCY (POMS)	OUTPUT CURRENT (FAN OUT) (PORV)	MAXIMUM JUNCTION TEMP. (deg C)	MAXIMUM OPERATING TEMP. (deg C)
I	A&B	+/- 3%	NL	80	80	85	NL
	C	+/- 3% *	NL	75 *	70 (70) *	85 *	NL
	D	NL	75 *	75 *	70 (70) *	85 *	NL
	E	+/- 3%	NL	80	80	85	NL
	F	NL	NL	NL	70	NL	30 C FML
II	A&B	+/- 5%	NL	90	85	100	NL
	C	+/- 5% *	NL	80 *	75 (75) *	100 *	NL
	D	NL	80 *	80 *	75 (75) *	100 *	NL
	E	+/- 5%	NL	90	90	100	NL
	F	NL	NL	NL	80	NL	25 C FML
III	A&B	+/- 5%	NL	95	90	110	NL
	C	+/- 5% *	NL	90 *	80 (80) *	125 *	NL
	D	NL	85 *	90 *	80 (80) *	125 *	NL
	E	Per Spec.	NL	95	90	115	NL
	F	NL	NL	NL	90	NL	20 C FML
NONE SPECIFIED	G	+/- 5%	NL	90	NL	NL	85
	H	NL	(Nominal)	NL	80	110	NL
	J	NL	NL	75	80	110	NL
	K	NL	70 *	80 *	80 *	85 *	NL
	L	NL	(Nominal)	70	80	100	NL
	M	10 %	NL	NL	80	125	NL
	W	+/- 5%	NL	50	80	65 PORV	30 C FML
	X	+/- 0.5V	NL	NL	75	125	NL

KEY:
* = Complex Microcircuits
NL = Not Listed
FML = From Maximum Limit
POMS = Percent of Maximum Specified
PORV = Percent of Rated Value

Table 4-11 Microprocessor Stress Derating Criteria

Classification	Derating Parameter	Level I	Level II	Level III
MOS	Supply Voltage (volts), 8-Bit (1)	10	11	13
	Supply Voltage (volts), 16 Bit (1)	606 / (G ** 0.440)	760 / (G ** 0.462)	698 / (G ** 0.438)
	Supply Voltage (volts), 32-Bit (1)	642 / (G ** 0.442)	627 / (G ** 0.448)	696 / (G ** 0.438)
	Frequency (POMS)	80	80	80
	Output Current, Fan Out, (PORV)	70 (80)	75 (80)	80 (90)
	Max. Junc. Temp. (deg C), 8-Bit	120	125	125
	Max. Junct. Temp. (deg C), 16-Bit (2)	90	125	125
	Max. Junct. Temp. (deg C), 32-Bit (2)	60	101	125
	Circuit Complexity - Maximum Gates	N/A	N/A	N/A
Bipolar	Supply Voltage	+/- 3%	+/- 5%	+/- 5%
	Frequency (POMS)	75	80	90
	Output Current, Fan Out, (PORV)	70 (70)	75 (75)	80 (80)
	Max. Junc. Temp. (deg C), 8-Bit (2)	80	85	125
	Max. Junct. Temp. (deg C), 16-Bit (2)	70	70	125
	Max. Junct. Temp. (deg C), 32-Bit (2)	55	56	120
	Circuit Complexity - Maximum Gates	N/A	26,000	N/A

KEY:
G = Number of Gates
LG = Log (base 10) of Gates
N/A = Not Applicable
POMS = Percent of Maximum Specified
PORV = Percent of rated value
* = Multiplied by
** = Taken to the Power of

Notes: (1) Not to exceed supplier minimum or maximum rating
(2) Not to exceed 125 deg C or supplier maximum, which ever is smaller

4.3 PROM MICROCIRCUITS

The stress derating criteria for PROM devices was developed similarly to ASIC/VHSIC microcircuits, with exceptions for EEPROMs. These exceptions centered on the need to include the L_{CYC} term in the failure rate model of equation (2). The differences between the criteria in each table were the results of applying the different device-specific attributes and stress-specific parameters to the failure rate equation. These attributes and parameters included temperature activation energy (PiT), circuit complexity (C1), number of package pins (C2), total transistor gate area (L_{TDDB}) and dielectric thickness (L_{TDDB}). The values or equations used in evaluating the device-specific and stress-specific attributes are outlined in table 4-12.

The temperature activation energies were obtained from the pre-release version of MIL-HDBK-217 Revision F. The C1 factor equations were derived by fitting the C1 factor data associated with the RA/AAT reliability models to an appropriate curve. The C1 data and best fit curves are shown in figures 4-28 and 4-29 for MOS PROMS and bipolar PROMs, respectively. The value for maximum pin count was derived by examination of current supplier

Table 4-12 PROM Device/Stress-Specific Attributes

Technology	Attribute	Value / Equation
MOS	Ea	0.60 eV
	C1	0.00085 + 5.45E-6 * BITS ** 0.515
	Pins	40
	C2	2.8E-4 * PINS ** 1.08
	Transistor Gate Area	1.209E6 (sq um)
	Dielectric Thickness	2.31 / BITS ** 0.175 (kA)
Bipolar	Ea	0.60 eV
	C1	0.0094 + 6.20E-5 * BITS ** 0.514
	Pins	40
	C2	2.8E-4 * PINS ** 1.08

Figure 4-28 C1 Factor for MOS PROMs[1]

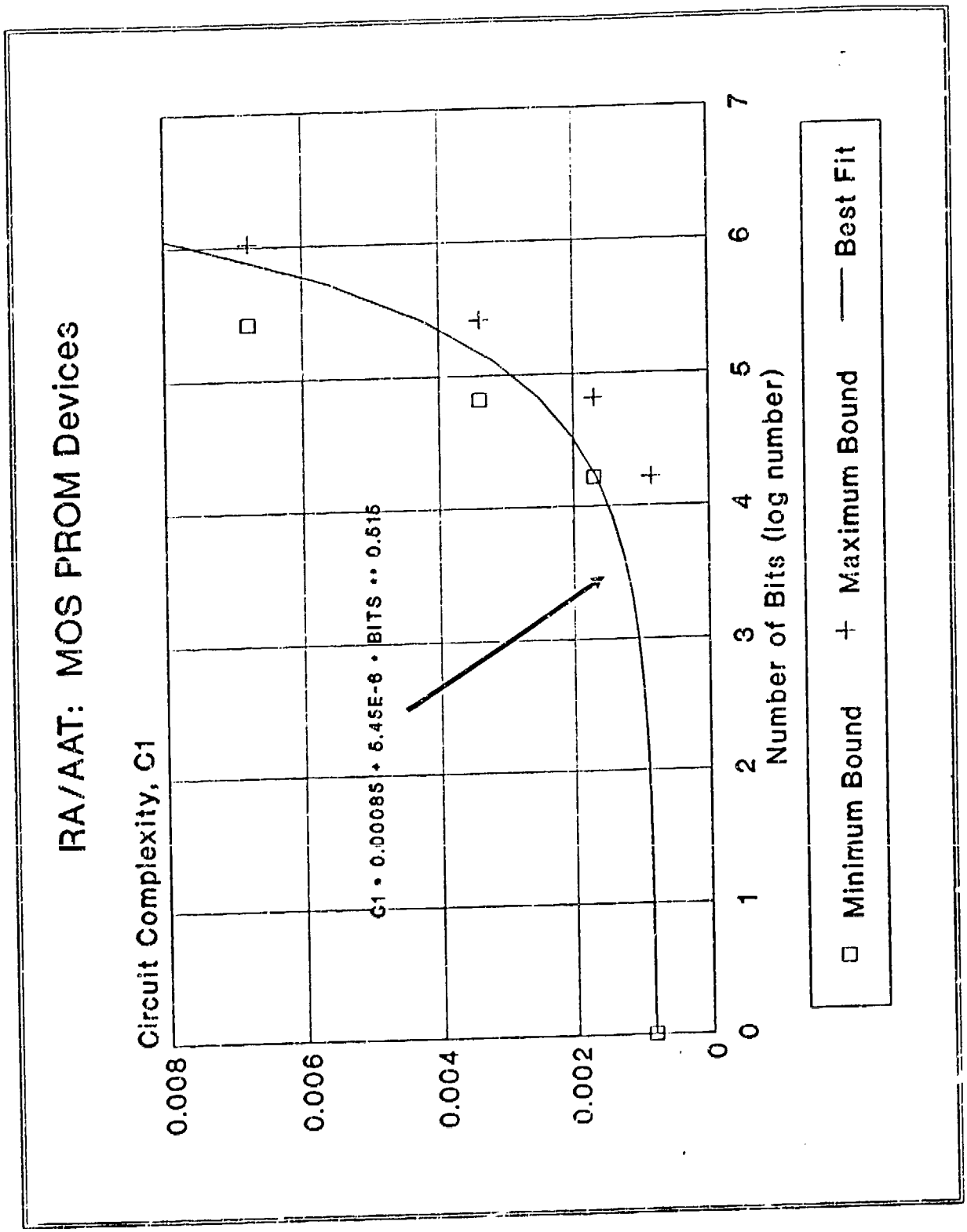
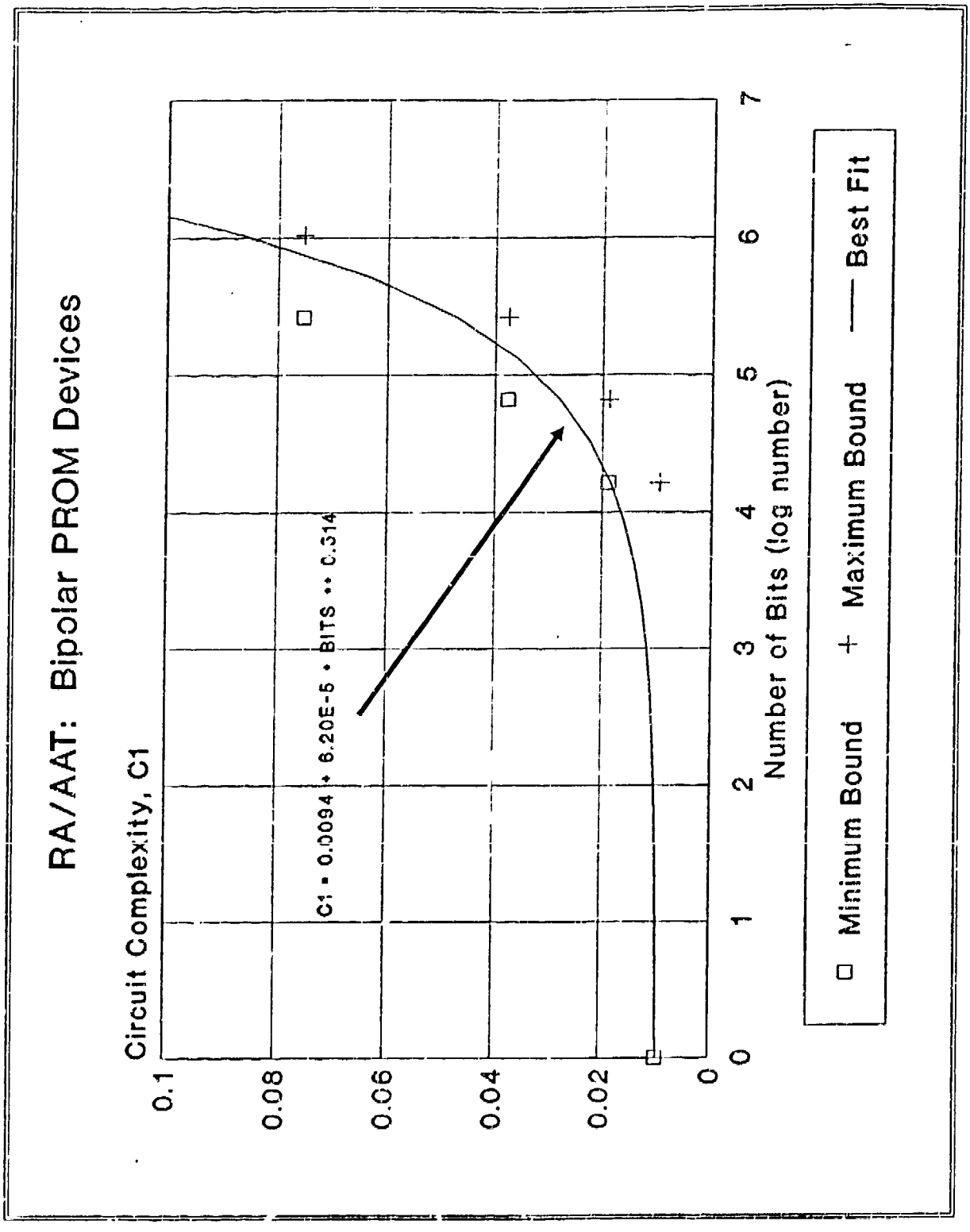


Figure 4-29 C1 Factor for Bipolar PROMs[1]



data books which described memory complexities up to one megabit. The total transistor gate area for MOS PROMs was extracted directly from the RA/AAT final report. The dielectric thickness dependence on memory complexity for MOS PROMs is shown in figure 4-30.

By applying the approach outlined in section 4.0, maximum junction temperatures and maximum supply voltages were calculated for the two PROM technologies as a function of memory complexity. Figures 4-31 and 4-32 show the supply voltage derating curves for MOS PROMs excluding EEPROMs and EEPROMs, respectively. The maximum supply voltage for EEPROMs is lower than the maximum supply voltage for other PROMs because it was traded off with the number of write cycles. It is noted, however, that the difference in supply voltage between EEPROMs and other types of PROMs of similar complexity is at most 0.85 volts. In the trade-off between supply voltage and number of write cycles for EEPROMs, the only guideline used was the requirement was that the supply voltage remain above 5V for all EEPROMs up to 1 Mbit complexity for any criticality level. Figure 4-33 shows the write cycle derating curves generated for EEPROMs. Since bipolar PROMs do not experience wear out due to TDDB, supply voltage derating curves are not calculated for this technology. The solid lines on the graphs in each figure represent the best least squares fit to the calculated derating values.

Supplementing the junction temperature and supply voltage derating parameters were the stress derating parameters outlined by other derating guideline sources as shown in tables 4-13 and 4-14 for MOS PROM devices and bipolar PROM devices, respectively. In keeping with the general approach outlined in Section 3.0, and because of the uncertainty of criticality assumed with guideline sources not specifying three criticality levels, only those guideline sources supplying derating criteria for three criticality levels were evaluated for inclusion in the updated guidelines. For each parameter specified by these guideline sources, a median value for the parameter was chosen. In the case where the choice was between an even

Figure 4-30 Dielectric Thickness for MOS PROMs[1]

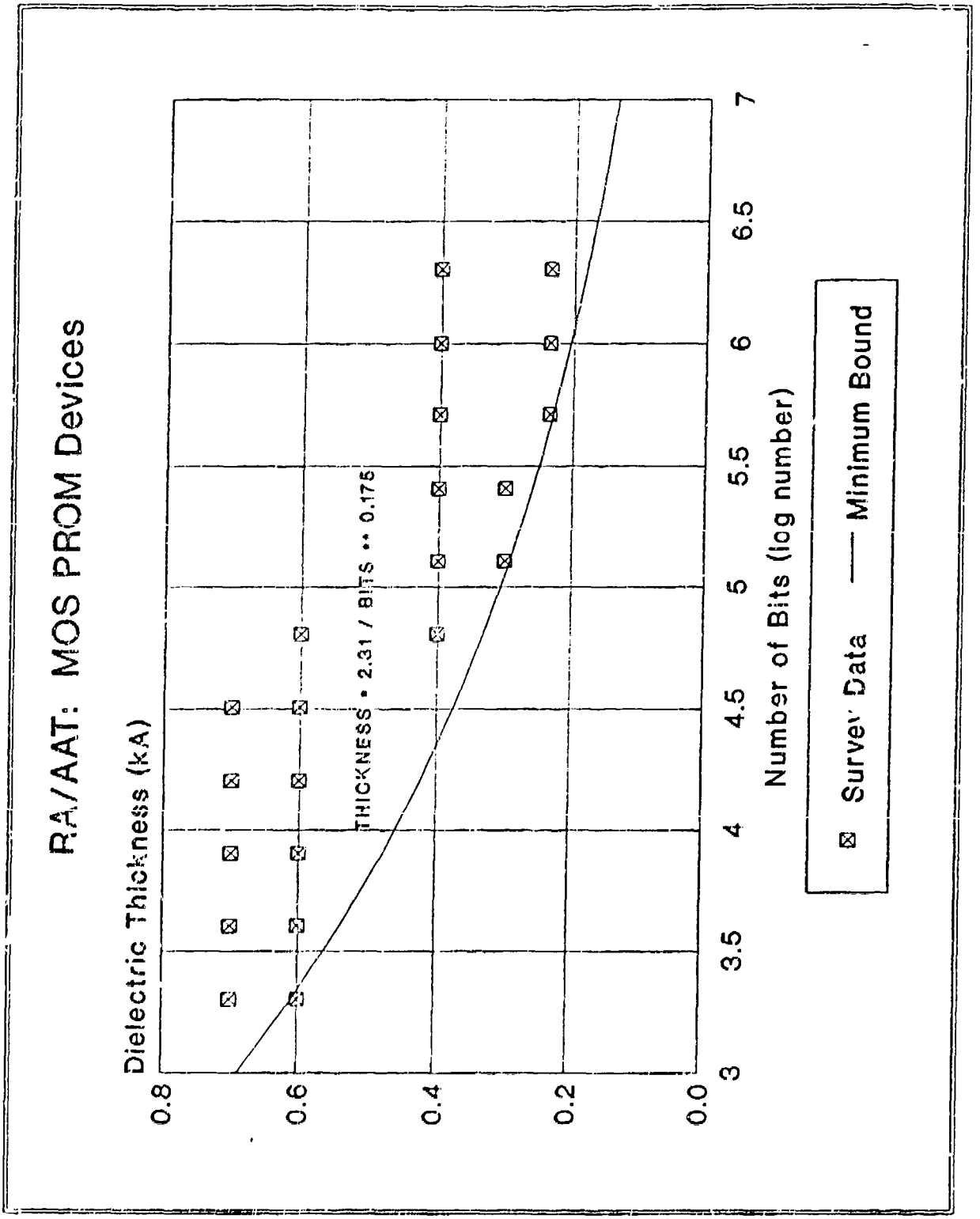


Figure 4-31 Supply Voltage Derating for MOS PROMs Excluding EEPROMs

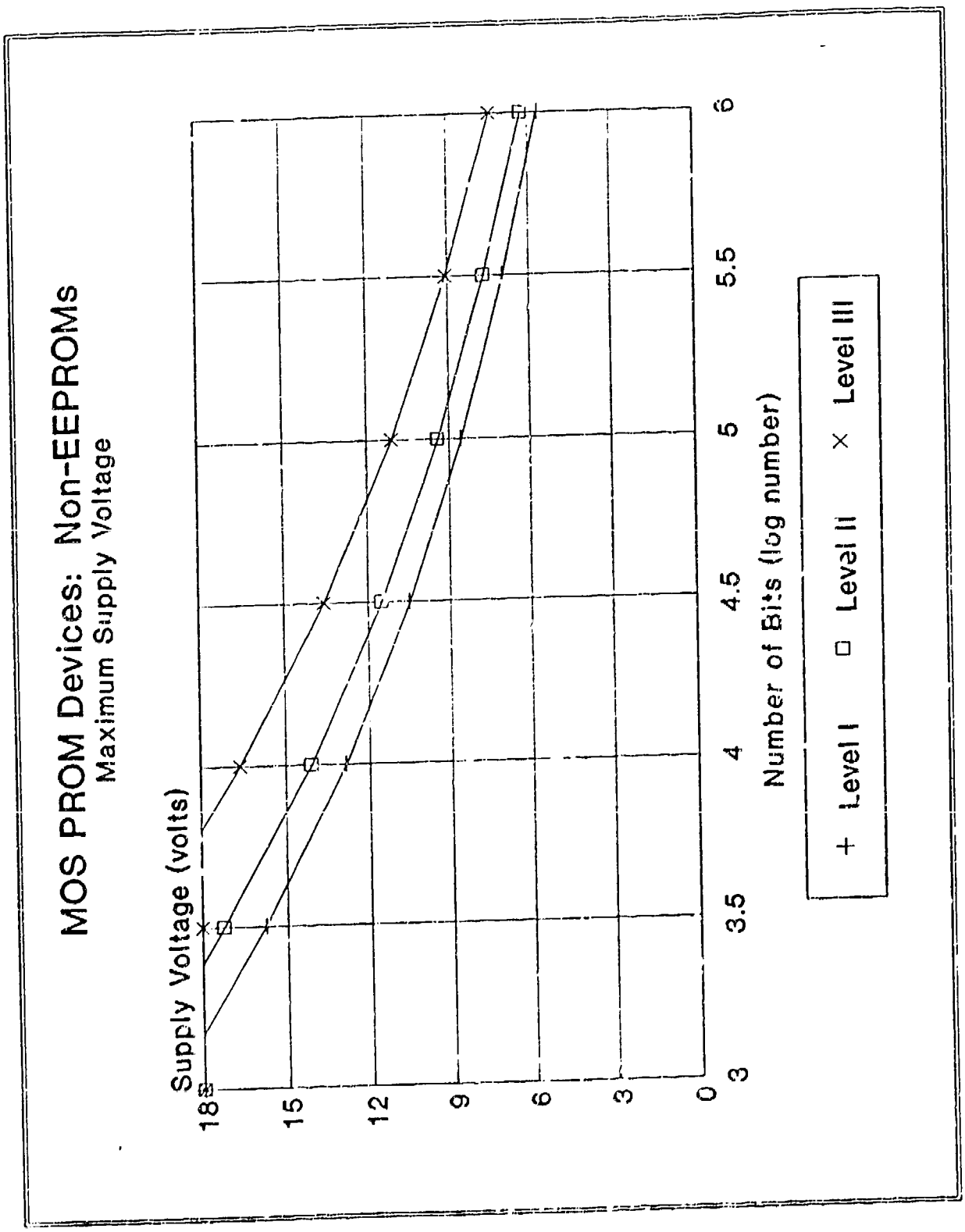


Figure 4-32 Supply Voltage Derating for EEPROMs

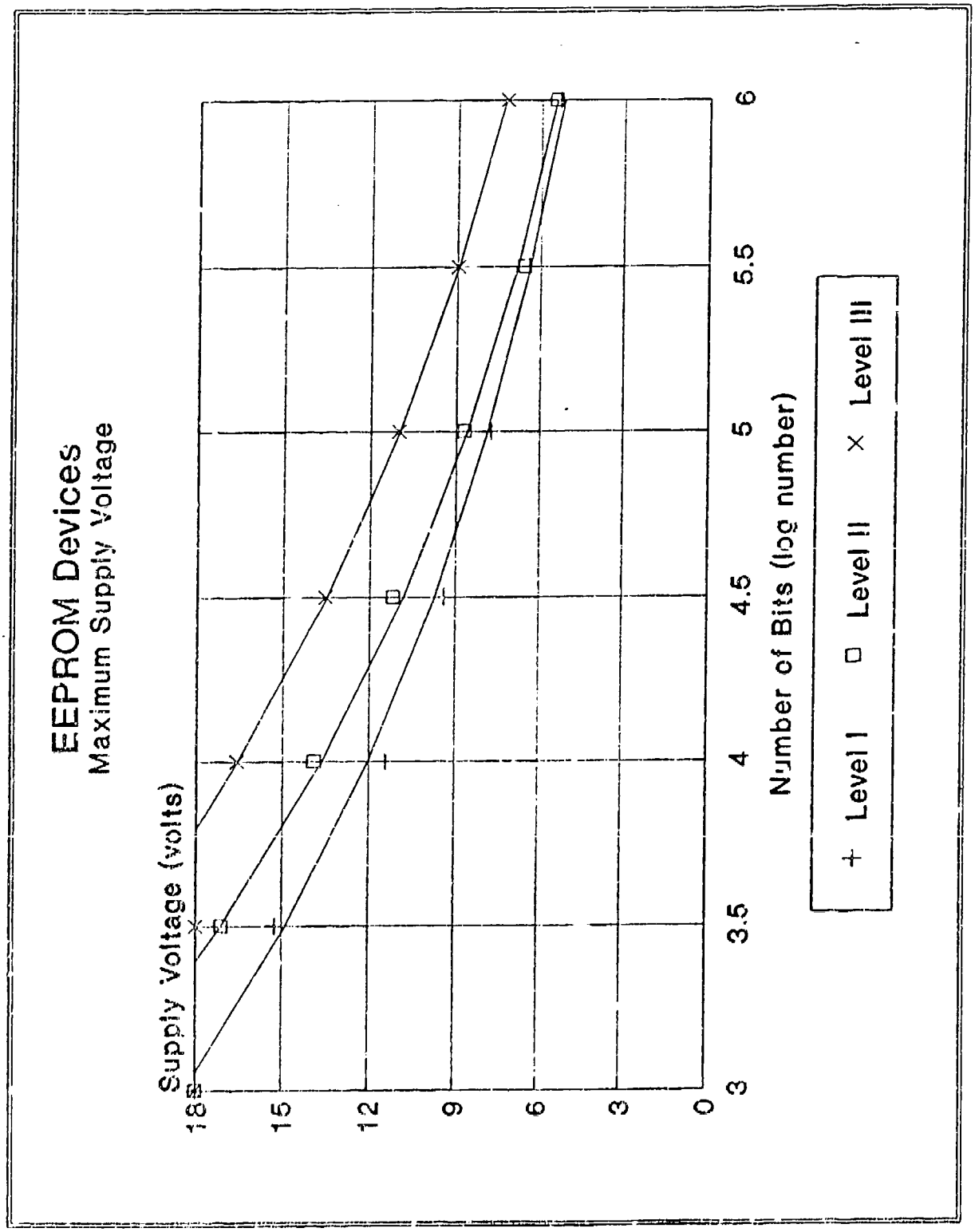


Figure 4-33 Write Cycle Derating for EEPROMs

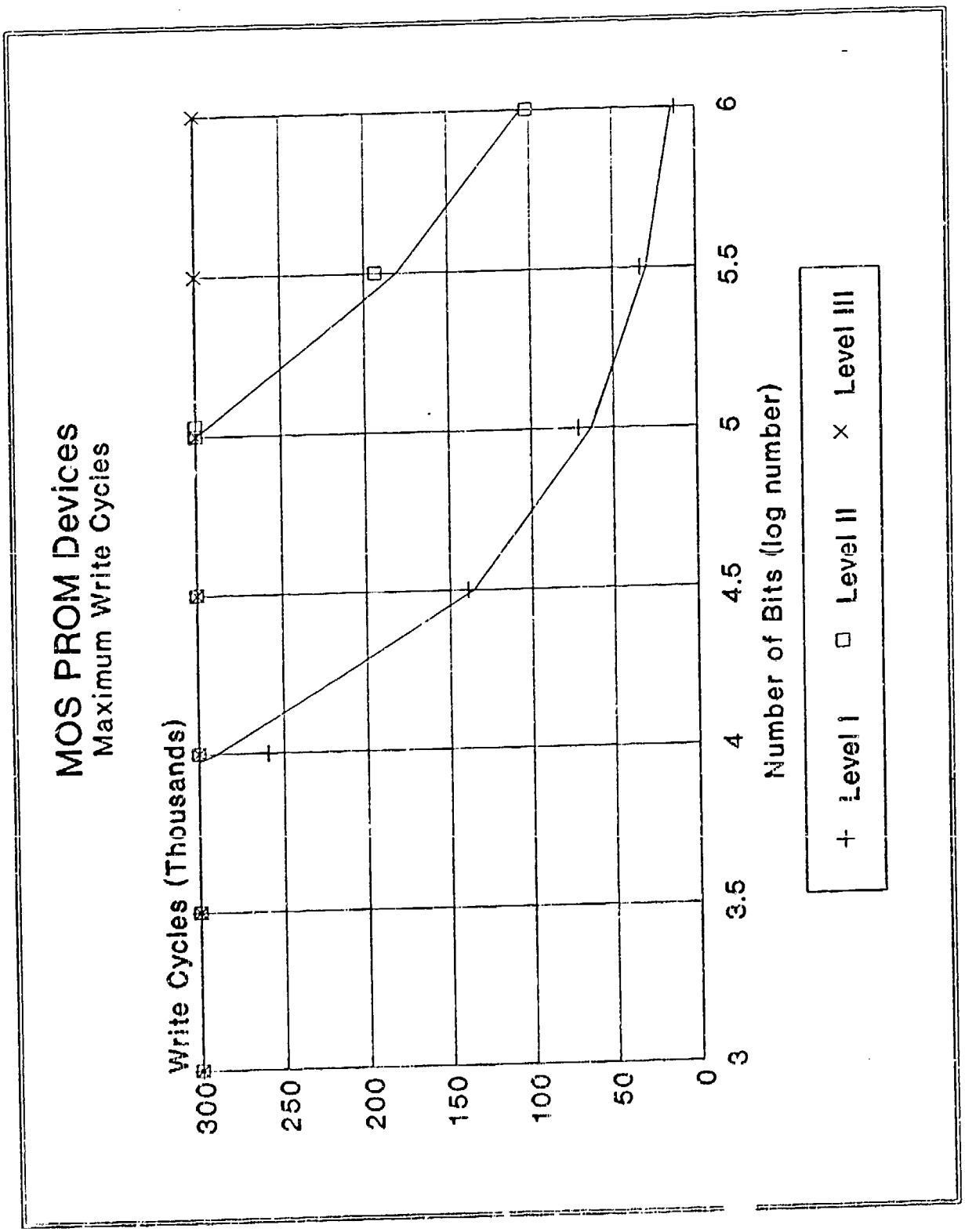


Table 4-13 MOS PROM Guidelines

CRITICALITY LEVEL	GUIDELINE	DYNAMIC SUPPLY VOLTAGE (PORV)	FREQUENCY (POMS)	OUTPUT CURRENT (PORV)	MAXIMUM JUNCTION TEMP. (deg C)	MAXIMUM OPERATING TEMP. (deg C)
I	A&B	70	80	80	85	NL
	C	75 *	NL	70 *	85 *	NL
	D	75 *	NL	70 *	85 *	NL
	E	70	80	80	85	NL
	F	100	NL	80	NL	30 C FML
II	A&B	85	80	85	100	NL
	C	80 *	NL	75 *	100 *	NL
	D	80 *	NL	75 *	100 *	NL
	E	80	80	90	100	NL
	F	100	NL	90	NL	20 C FML
III	A&B	85	90	90	110	NL
	C	85 *	NL	80 *	125 *	NL
	D	85 *	NL	80 *	125 *	NL
	E	80	90	90	110	NL
	F	100	NL	100	NL	20 C FML
NONE SPECIFIED	G	NL	90	NL	NL	85
	H	(Nominal)	NL	80	110	NL
	J	NL	75	80	110	NL
	K	70 *	80 *	80 *	85 *	NL
	L	(Nominal)	70	NL	100	NL
	M	80	NL	80	125	NL
	W	100	50	80	65 PORV	30 C FML
	X	Vcc +/-0.5V	NL	75	125	NL

KEY:
* = Complex Microcircuits
NL = Not Listed
FML = From Maximum Limit
POMS = Percent of Maximum Specified
PORV = Percent of Rated Value

Table 4-14 Bipolar Prom Guidelines

CRITICALITY LEVEL	GUIDELINE	FIXED SUPPLY VOLTAGE	DYNAMIC SUPPLY VOLTAGE (PORV)	FREQUENCY (POMS)	OUTPUT CURRENT (PORV)	MAXIMUM JUNCTION TEMP. (deg C)	MAXIMUM OPERATING TEMP. (deg C)
I	A&B	+/- 3%	NL	80	80	85	NL
	C	+/- 3% *	NL	NL	70 *	85 *	NL
	D	NL	75 *	NL	70 *	85 *	NL
	E	+/- 3%	NL	80	80	85	NL
	F	NL	NL	NL	70	NL	30 C FML
II	A&B	+/- 5%	NL	90	85	100	NL
	C	+/- 5% *	NL	NL	75 *	100 *	NL
	D	NL	80 *	NL	75 *	100 *	NL
	E	+/- 5%	NL	90	90	100	NL
	F	NL	NL	NL	80	NL	25 C FML
III	A&B	+/- 5%	NL	95	90	110	NL
	C	+/- 5% *	NL	NL	80 *	125 *	NL
	D	NL	85 *	NL	80 *	125 *	NL
	E	Per Spec.	NL	95	90	115	NL
	F	NL	NL	NL	80	NL	20 C FML
NONE SPECIFIED	G	+/- 5%	NL	90	NL	NL	85
	H	NL	(Nominal)	NL	80	110	NL
	J	NL	NL	75	80	110	NL
	K	NL	70 *	80 *	80 *	85 *	NL
	L	NL	(Nominal)	70	NL	100	NL
	M	10 %	NL	NL	80	125	NL
	W	+/- 5%	NL	50	80	65 PORV	30 C FML
	X	+/- 0.5V	NL	NL	75	125	NL

KEY:
* = Complex Microcircuits
NL = Not Listed
FML = From Maximum Limit
POMS = Percent of Maximum Specified
PORV = Percent of Rated Value

number of values, the average of the two middle values was calculated. Priority was given to those guidelines specifying advanced microcircuits, such as VLSI and gate arrays. The remaining guideline sources were used as a "sanity check" of the updated stress derating criteria. Table 4-15 summarizes the new stress derating criteria for PROM microcircuits, including the pertinent stress derating criteria from the current version of the Guidelines.

Table 4-15 PROM Stress Derating Criteria

Classification	Derating Parameter	Level I	Level II	Level III
MOS	Supply Voltage * (volts) (1)	65.2 / (B ** 0.183)	85.3 / (B ** 0.199)	85.3 / (B ** 0.178)
	Supply Voltage (volts) (1)	66.0 / (B ** 0.178)	71.1 / (B ** 0.176)	83.3 / (B ** 0.175)
	Frequency (POMS)	80	80	90
	Output Current (PORV)	70	75	80
	Maximum Junction Temp. (deg C) (2)	125	125	125
	Maximum Write Cycles (3)	1.26E8 / (B ** 0.660)	6.94E7 / (B ** 0.470)	300,000
	Circuit Complexity - Maximum Bits	1 Mbit	1 Mbit	1 Mbit
Bipolar	Fixed Supply Voltage	+/- 3%	+/- 5%	+/- 5%
	Frequency (POMS)	80	90	95
	Output Current (PORV)	70	75	80
	Maximum Junction Temp. (deg C) (2)	125	125	125
	Circuit Complexity - Maximum Bits	1 Mbit	1 Mbit	1 Mbit

KEY: B - Number of Bits
LB - Log (base 10) of B
* - Applicable to EEPROMs Only
POMS - Percent of Maximum Specified
PORV - Percent of Rated Voltage
/ - Divided By
** - Taken To The Power Of

Notes: (1) Not to exceed supplier minimum or maximum rating.
(2) Not to exceed 125 deg C or supplier maximum, which ever is smaller.
(3) Applicable to EEPROMs Only. Not to exceed supplier maximum.

4.4 MICROCIRCUIT APPLICATION NOTES

The following application notes for advanced technology microcircuits were developed from a review of applicable literature, supplier surveys and other stress derating guidelines. These application notes may also be found in Appendix A.

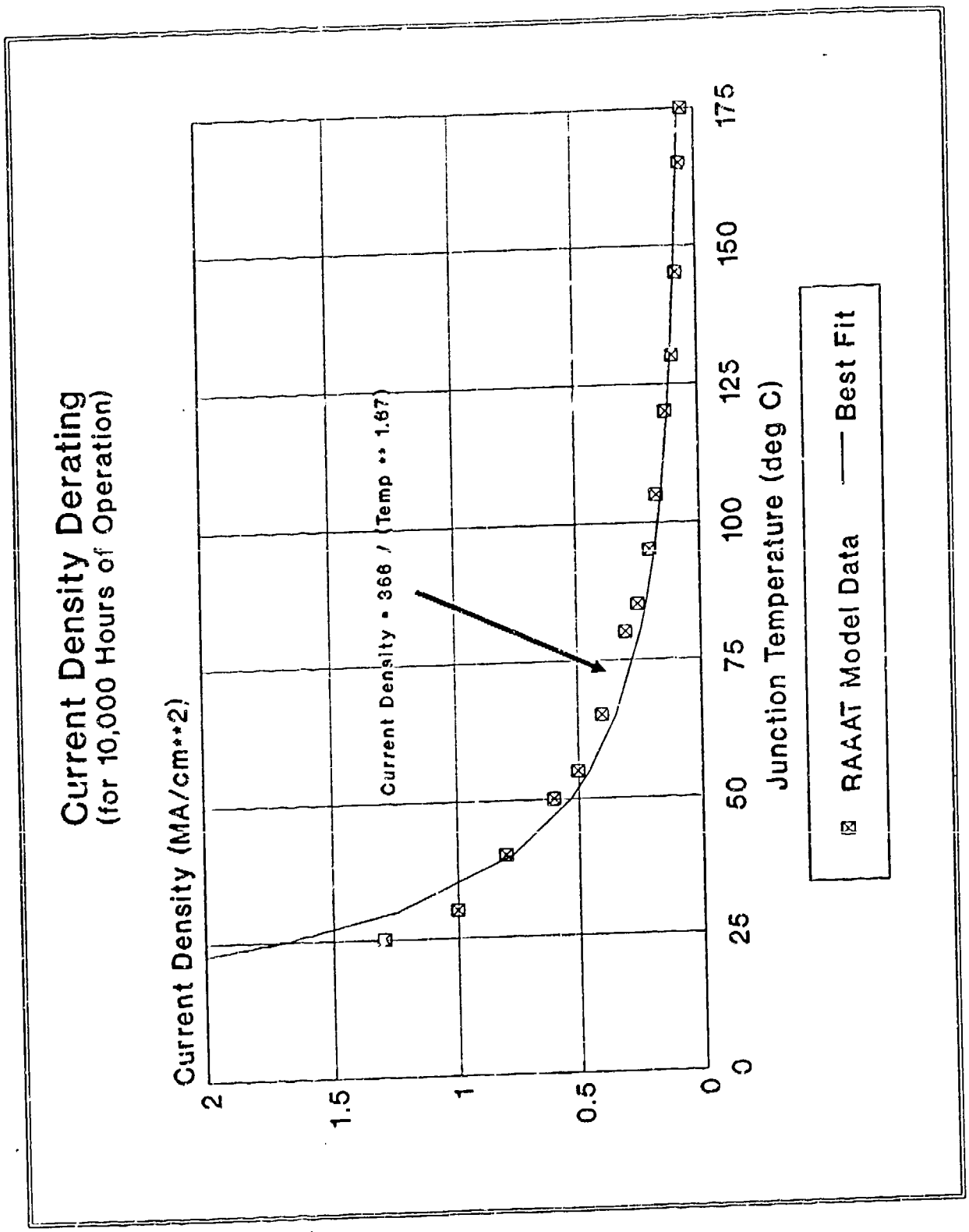
Digital Microcircuits:

1. Advanced technology microcircuits are sensitive to ESD.
2. Unused inputs should be connected to a supply voltage or ground.
3. Supply filtering is required to filter out transients.
4. Heat sinks may be required to maintain derated junction temperatures.
5. Design margins should be used for input leakage (+100%), fanout (-20%) and frequency (-10%).
6. Good engineering judgement should be used to derate other microcircuit characteristics, including hold and propagation delay times, to produce a conservative design.
7. Circuit design must avoid application of reverse voltages on device leads.
8. Do not exceed the current density derating described by the equation
   Current Density = 366 / (Temperature in deg. C ** 1.67)
   or 5E5 A/cm^2, whichever is smaller, for aluminum-based metallized microcircuits for either internal circuit operation or output driver operation (see figure 4-34).
9. (Bipolar) Supply voltage deviations from the specified nominal will shift internal bias points which, when coupled with thermal effects can cause erratic performance.
10. (MOS) Input destruction may occur by shorting leads during assembly.
11. (MOS) High speed transients may result in parasitic bipolar latch-up.

Linear Microcircuits:

1. Each linear device is unique and the designer should have a thorough knowledge of its application requirements to assure that the device is operated within its performance envelope at all times.
2. Heat sinks may be required to maintain derated junction temperatures.
3. Design margins should be used for gain (-20%) and offset voltages and currents (+50%).
4. The circuit design must avoid application of reverse voltage on device leads.
5. Do not exceed the current density derating described by the equation
   Current Density = 366 / (Temperature in deg. C ** 1.67)
   or 5E5 A/cm^2, whichever is smaller, for aluminum-based metallized microcircuits for either internal circuit operation or output driver operation (see figure 4-34).

Figure 4-34 Maximum Current Density for Microcircuits



5.0 MIMIC DERATING GUIDELINES

For advanced technology MIMIC devices, the RA/AAT reliability models[1] can be summarized in general form by

$$I = PiQ * [(C1A * PiTA + C1P * PiTP) * PiA + C2 * PiE) * PiL \quad (3)$$

where:

L is the MIMIC failure rate in failures per million hours,
PiQ is the quality factor,
PiTA is the temperature acceleration factor for active devices,
PiTP is the temperature acceleration factor for passive devices,
PiA is the MIMIC application factor,
PiE is the application environment factor
PiL is the learning factor,
C1A is the circuit complexity failure rate for active devices, in failures per million hours,
C1P is the circuit complexity failure rate for passive devices, in failures per million hours, and
C2 is the package complexity failure rate in failures per million hours.

A review of the literature[101-122] concerned with MIMIC failure, during the time since the RA/AAT failure rate models were generated, resulted in no change to this basic model.

The stress parameters and attributes that directly affect the calculated failure rate for a MIMIC device are embedded in the Pi and complexity failure rate factors of the reliability model. To extract the maximum stresses allowed for each criticality level from the factors in the reliability model, L in equation (3) must be set to the maximum failure rate allowed by each criticality level. Since MIMIC devices were not included in either the current version of the Guidelines or any version of

MIL-HDBK-217, these maximum failure rates are not specified in table 3-3. Therefore, an alternate approach was used to bound the failure rate for each criticality level. It was noted that the maximum failure rates calculated for silicon microcircuits closely approximated the failure rates that would be calculated given probabilities of success of 0.9990, 0.9900 and 0.9000 at 10,000 hours for criticality levels I, II and III, respectively. The actual failure rates associated with these three probabilities of success are 0.1001, 1.0050 and 10.5361, respectively. These three failure rates were used in the approach for developing stress derating criteria in a fashion similar to the approach used for advanced technology silicon microcircuits. The parameters and attributes of the failure rate model factors were separated into three groups, one group for criticality-specific (CS) attributes, one group for device-specific (DS) attributes and the other group for stress-specific (SS) parameters. Table 5-1 outlines the relationship between the factors in the failure rate equation and the distinction between criticality-specific, device specific and stress-specific parameters and attributes associated with the factors.

There were two types of device-specific attributes, technology and complexity. The technology attribute of the C2 factor was handled by noting that the pin count for most MIMICs does not exceed 10 pins. The packaging technology selected was the one that gave the highest failure rate for a 10 pin package according to the RA/AAT final report. Having bound the package complexity, the circuit complexity attribute was handled by noting that the relative difference in values of the C1P factors for MIMIC devices with 11 to 100 passive elements and MIMIC devices with greater than 100 passive elements was less than 10 percent, and that many MIMIC devices had more than 10 passive elements. Therefore, the C1P factor for MIMICs with greater than 100 passive elements was used to represent the C1P factor for MIMICs with 11 to 100 passive elements. Four sets of derating criteria were developed to handle the two C1A and two C1P circuit complexity categories of MIMIC devices.

Table 5-1 Attributes and Parameters of MIMIC Model Factors

Factor	Type	Attribute / Parameter
PiQ	CS	Application Environment
PiTA	SS	Channel Temperature
PiTP	SS	Channel Temperature
PiA	N/A	Application
PiE	CS	Application Environment
PiL	CS	Years In Production
C1A	DS	Circuit Complexity, Active Devices
C1P	DS	Circuit Complexity, Passive Devices
C2	DS	Package Technology
	DS	Package Complexity

The criticality-specific attributes included application environment and years-in-production. The application environments for the PiQ factor were S-Level, B-Level and B-Level for criticality levels I, II and III, respectively. The application environments for the PiE factor were S_F, A_U and G_F for criticality levels I, II and III, respectively. These application environments were chosen since they were the most closely related to the application environments outlined in the current version of the Guidelines. The years-in-production attribute for the experience factor, PiL, were 2 years, 1 year and 0.75 years for criticality levels I, II and III, respectively. These years in production were chosen based upon current experience with component procurement for systems that can be categorized by the definitions given for each criticality level.

The stress-specific parameters, as mentioned previously, are the only ones that, when changed, result in a different failure rate for any given MIMIC. The channel temperature parameter was the only parameter that could be varied to obtain the maximum failure rate for the MIMIC. With the device-specific, criticality-specific and stress-specific attributes and parameters defined, the maximum channel temperature derating criteria was developed.

The criteria in the MIMIC stress derating table was the result of applying the device-specific attributes and stress-specific parameters to the failure rate equation. These attributes and parameters included temperature activation energy (PiTA and PiTP), circuit complexity (C1A and C1P) and number of package pins (C2). Table 5-2 outlines the values used in evaluating these device/stress-specific attributes.

The dependence of failure rate and probability of success at 10,000 hours of operation are shown in figures 5-1 and 5-2, respectively. By applying the approach outlined in sections 3.0 and 4.0, the maximum channel temperature is calculated by setting the MIMIC failure rate of equation (3) to the failure rates of the three criticality levels. The channel temperature derating criteria for MIMIC devices is found in table 5-3.

Table 5-2 MIMIC Device/Stress-Specific Attributes

Technology	Attribute	Value / Equation
GaAs	Ea (Active)	1.50 eV
	Ea (Passive)	0.43 eV
	C1A	7.22
	C1P	2.94
	Pins	10
	C2	2.8E-4 * PINS ** 1.08

Figure 5-1 MIMIC Failure Rate

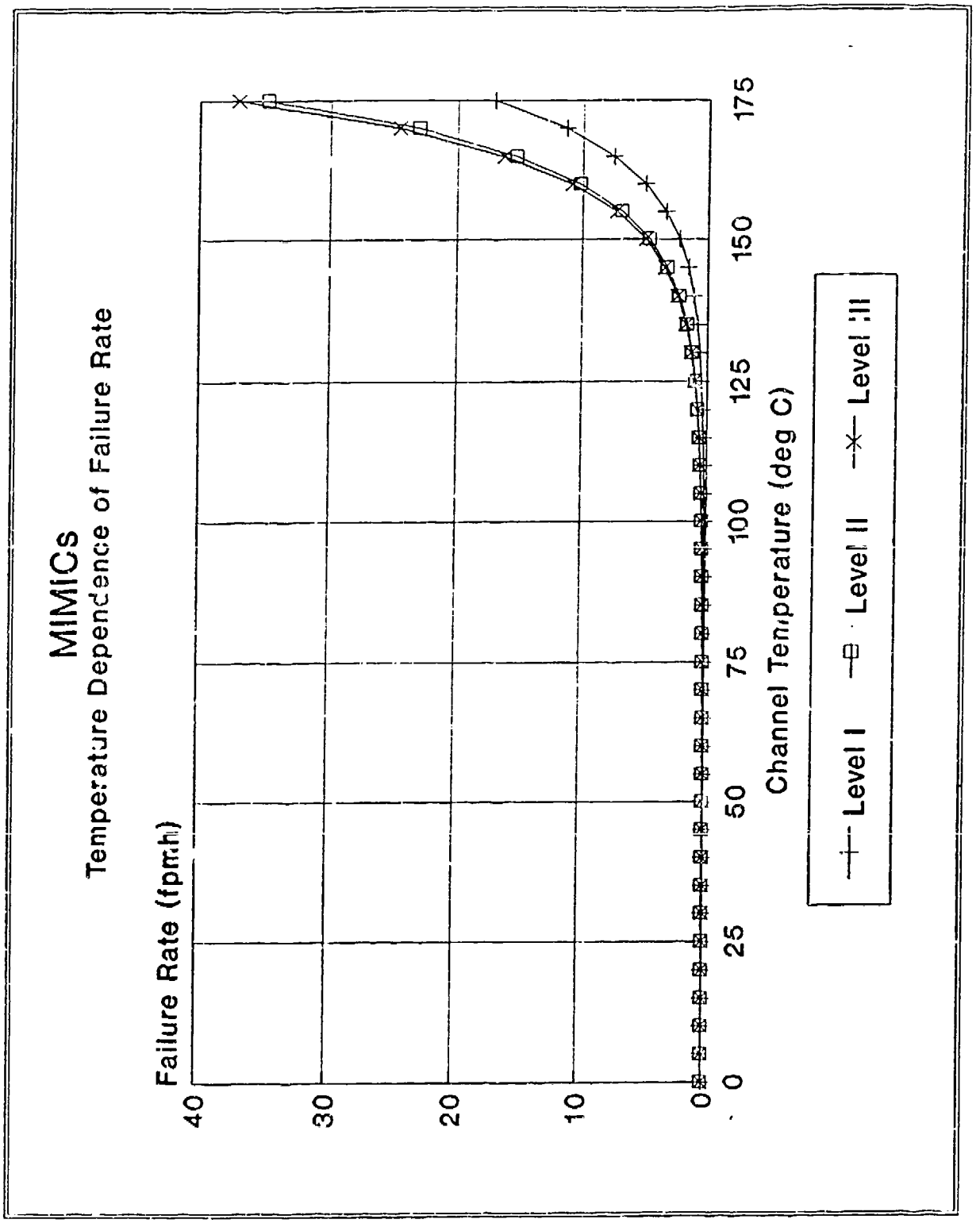


Figure 5-2 MIMIC Probability of Success at 10,000 Hours

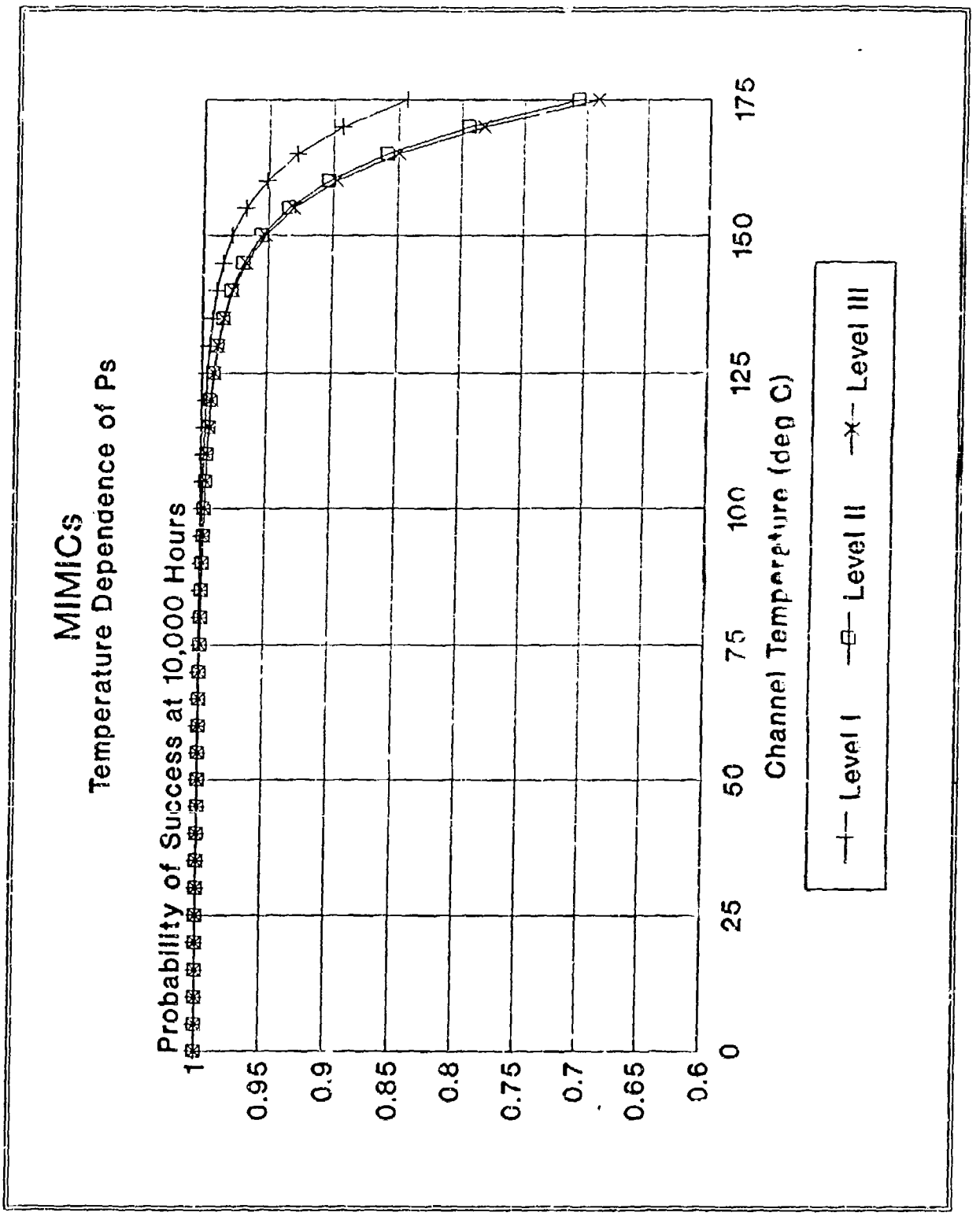


Table 5-3 MIMIC Stress Derating Criteria

Classification	Derating Parameter	Level I	Level II	Level III
GaAs	Maximum Channel Temp. (deg C) (1)			
	For: AE <= 100; PE <= 10	95	130	150
	AE > 100; PE <= 10	95	130	150
	AE <= 100; PE > 10	90	130	150
	AE > 100; PE > 10	90	125	150

KEY: AE - Active Elements
PE - Passive Elements

Notes: (1) Not to exceed supplier maximum.

It is noted here that the calculated derated channel temperature stress for level III mission criticality (approximately 160 to 165 deg C) was above the region of validity of the RA/AAT reliability model. Therefore, the maximum channel temperature for level III criticality was set to the maximum valid channel temperature of 150 deg C.

Since existing stress derating guidelines have purposely affected the observed failure rates of components used in applications corresponding to one of the three criticality levels, it was necessary to review the existing stress derating guidelines to determine their relevance in being included in the updated stress derating guidelines, given that the factors being derated were not explicitly included in the current failure rate models. It was determined that none of the identified fourteen guideline sources provided MIMIC stress derating criteria. Therefore, the updated stress derating criteria for MIMICs is limited to only the newly created criteria based upon the updated RA/AAT reliability models.

MIMIC APPLICATION NOTES

The following application notes for MIMIC devices were developed from a review of applicable literature, supplier surveys and other stress derating guidelines. These application notes may also be found in Appendix A.

1. The environment of the internal package cavity of the MIMIC must be kept inert.
2. Precautions must be observed during electrical test to prevent potential latent failure due to overstress.

6.0 POWER TRANSISTOR DERATING GUIDELINES

Power transistors are designed for power amplification and handling high voltages and large currents. The main concern with power transistors is the high absolute values of power and the limitation of operation imposed by second breakdown.

Stress derating guidelines were generated for three classes of power transistors, silicon bipolar, GaAs and MOSFET. For silicon bipolar power transistors, an approach similar to the microcircuit approach was used to develop the stress derating criteria. For GaAs power MESFETs, adequate data was accumulated which allowed the generation of a temperature dependent failure rate model. For power MOSFETs, it was determined that the currently accepted derating policies were adequate in providing the margins of safety and success needed in the intended applications. Reviews of the literature[123-159], supplier surveys and available stress derating guidelines from government and industry sources were used to evaluate and update the stress derating criteria for these types of power transistors.

The application notes for power transistors were also developed from a review of applicable literature, supplier surveys and other stress derating guidelines. These application notes may be found at the end of this power transistor section and in Appendix A.

6.1 SILICON BIPOLAR POWER TRANSISTORS

The junction temperature, T_j, in a silicon bipolar power transistor increases as the the power increases. The maximum value of T_j is limited by the temperature at which the base region of the transistor becomes intrinsic, that is, the collector is effectively shorted to the emitter and transistor action ceases. The temperature and power handling ability of a transistor can be improved by providing adequate heat sink for efficient thermal dissipation, providing a large enough emitter stripe width to

reduce current density and preferring low voltage, high current application to high voltage, low current applications. The latter condition results in higher temperature rises at the stripe centers. Consequently, both power and junction temperature stresses need to be derated.

The use of power transistors is often limited by a phenomenon called second breakdown, which is marked by an abrupt decrease in device voltage with a simultaneous internal constriction of current. For high power devices, operation must be confined to a safe operating area (SOA) so that permanent damage caused by the second breakdown can be avoided. Figure 6-1 shows a typical SOA for a silicon power transistor operated in the common-emitter configuration. At the upper left (A), collector load lines are limited by current-carrying ability. The DC thermal limit (B) is determined from the thermal resistance R_{th} of the device,

$$R_{th} = (T_j - T_o) / P \qquad (4)$$

where P is the power dissipated. Therefore, the thermal limit defines the maximum allowed junction temperature, where

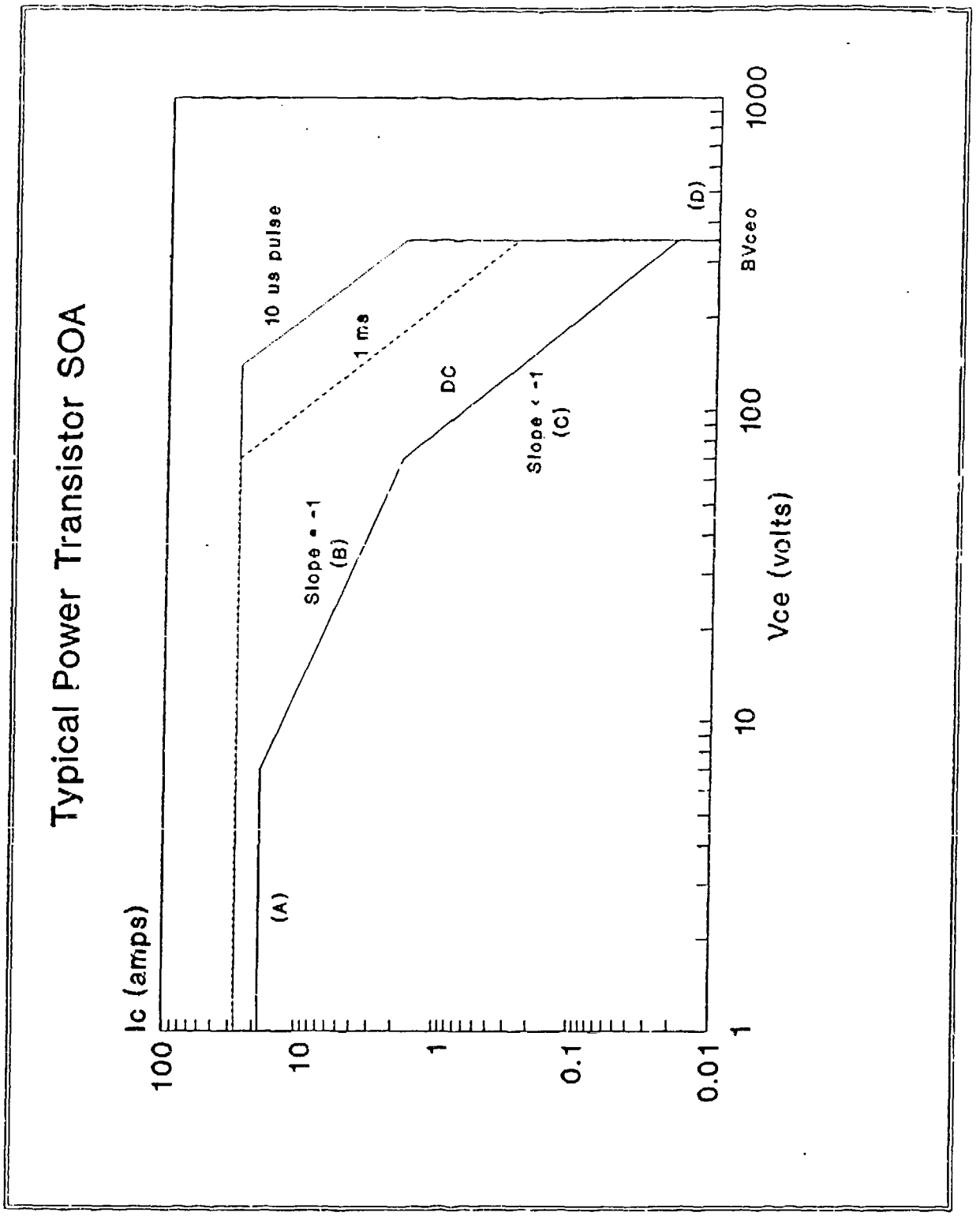
$$R_{th}(peak) = (T_j(max) - T_o) / (I_C \times V_{CE}) \text{ limit} \qquad (5)$$

If $T_j(max)$ and $R_{th}(peak)$ are assumed constant, then

$$(I_C \times V_{CE}) \text{ limit} = (T_j(max) - T_o) / R_{th}(peak) = \text{constant.} \qquad (6)$$

Thus a straight line relationship with slope=1 exists between $Ln(I_C)$ and $Ln(V_{CE})$. At higher voltages and lower currents, the temperature rise at the stripe center is responsible for the second breakdown, and the slope (C) is generally between -1.5 and -2. The device is eventually limited by the first breakdown voltage, or avalanche, in the SOA as indicated by the vertical line (D). For temperatures higher than T_o, the SOA is reduced. All portions of the SOA should be derated to provide margins of safety as needed for application.

Figure 6-1 Typical Power Transistor SOA



For silicon bipolar power transistors, the MIL-HDBK-217E Notice 1 reliability model[169] has the form

$$L = Lb * PiA * PiR * PiS * PiQ * PiE * PiT \quad (7)$$

where:

L is the transistor failure rate in failures per million hours,
Lb is the base failure rate,
PiA is the application factor,
PiR is the power rating factor,
PiS is the voltage stress factor,
PiQ is the quality factor
PiE is the application environment factor, and
PiT is the temperature acceleration factor.

A review of the literature concerned with silicon bipolar power transistor failure, during the time since MIL-HDBK-217E Notice 1 failure rate models were generated, resulted in no change to this basic model.

The stress parameters and attributes that directly affect the calculated failure rate for a silicon bipolar power transistor are embedded in the Pi factors of the reliability model. To extract the maximum stresses allowed for each criticality level from the factors in the reliability model, L in equation (7) must be set to the maximum failure rate allowed by each criticality level. These maximum failure rates are specified in table 3-3. In the approach to develop stress derating criteria for silicon bipolar power transistors, the parameters and attributes of the failure rate model factors were separated into three groups, one group for criticality-specific (CS) attributes, one group for device-specific (DS) attributes and the other group for stress-specific (SS) parameters. Table 6-1 outlines the relationship between the factors in the failure rate equation and the distinction between criticality-specific, device-specific and stress-specific parameters and attributes associated with the factors.

Table 6-1 Attributes and Parameters of Silicon Bipolar Power Transistor Model Factors

Factor	Type	Attribute / Parameter
Ib	N/A	Base Failure Rate (constant)
PiQ	CS	Application Environment
PiT	SS	Junction Temperature
PiE	CS	Application Environment
PiA	N/A	Application (contstant)
PiR	SS	Power Rating
PiS	SS	Voltage Stress

In this power transistor reliability model, there were no device-specific attributes. The only criticality-specific attribute was the application environment attribute. The application environments for the PiQ factor were JANTXV, JANTX and JAN for criticality levels I, II and III, respectively. The application environments for the PiE factor were S_F, A_{UF} and G_F for criticality levels I, II and III, respectively. These application environments were chosen since they were the most closely related to the application environments outlined by the criticality levels in the current version of the Guidelines and resulted in the highest failure rate for the criticality level they represented.

The stress-specific parameters, as mentioned previously, are the only ones that, when changed, result in a different failure rate for the given power transistor. These parameters, junction temperature, breakdown voltage and power rating, are the ones that can be traded-off to obtain a failure rate similar to the maximum failure rate that was calculated using MIL-HDBK-217D Notice 1. As shown in table 6-2, the stress specific attributes include temperature activation energy (PiT) and voltage acceleration (PiS).

Table 6-2 Silicon Bipolar Power Transistor
Stress-Specific Attributes

Technology	Attribute	Value / Equation
Silicon Bipolar	Ea PiS	0.18 eV 0.045 * exp [3.1 * A/R]

The approach taken to develop the bounds for these stress-specific parameters first assumed the power rating was the same as the power rating used to develop the maximum failure rate (200 W). Then, the derating of the remaining stress-specific parameters associated with the other reliability model factors, namely breakdown voltage and junction temperature, were equally weighted in calculating a similar failure rate. The equal weighting of the stress parameters resulted in derating both voltage and temperature to 65%, 85% and 90% of their maximum ratings for criticality levels I, II and III, respectively. Since the conservative maximum rating for silicon bipolar power transistors is 150 deg C, the junction temperature derating for criticality levels I, II and III are 95 deg C, 125 deg C and 135 deg C, respectively.

Supplementing the breakdown voltage and junction temperature derating parameters were the stress derating parameters outlined by other derating guideline sources shown in table 6-3. In keeping with the general approach outlined in Section 3.0, and because of the uncertainty of criticality assumed with guideline sources not specifying three criticality levels, only those guideline sources supplying derating criteria for three criticality levels were evaluated for inclusion in the updated guidelines. The remaining guideline sources were used only as a "sanity check" of the updated stress derating criteria. Table 6-4 summarizes the new stress derating criteria for bipolar silicon power transistors.

Table 6-3 Silicon Bipolar Power Transistor Guidelines

CRITICALITY LEVEL	GUIDELINE	MAXIMUM JUNCTION TEMPERATURE (deg C)	POWER DISSIPATION (PORV)	SAFE OPERATING AREA (PORV), Vce	SAFE OPERATING AREA (PORV), Ic	BREAKDOWN VOLTAGE (PORV)	ON-OFF TEMPERATURE CYCLES
I	A&B	95	50	70 Vce	60 Ic	60	NL
	C	95	50	70 Vce	60 Ic	NL	NL
	D	NL	NL	NL	NL	NL	NL
	E	(55 PORV)	50	70 Vce	60 Ic	60	Fig. 6-4
	F	(55 PORV)	55	55 Vce	55 Ic	60	Fig. 6-4
II	A&B	105	60	70 Vce	60 Ic	70	NL
	C	105	60	70 Vce	60 Ic	NL	NL
	D	NL	NL	NL	NL	NL	NL
	E	(70 PORV)	65	80 Vce	70 Ic	70	Fig. 6-4
	F	(80 PORV)	80	80 Vce	80 Ic	70	Fig. 6-4
III	A&B	125	70	70 Vce	60 Ic	70	NL
	C	125	70	70 Vce	60 Ic	NL	NL
	D	NL	NL	NL	NL	NL	NL
	E	(80 PORV)	75	90 Vce	80 Ic	80	Fig. 6-4
	F	(90 PORV)	90	90 Vce	90 Ic	80	Fig. 6-4
NONE SPECIFIED	G	60	60	75 Vce	75 Ic	NL	NL
	H	110	50	75 Vce	60 Ic	65	NL
	J	110	50	75 Vce	70 Ic	NL	NL
	K	125	50	75 Vce	75 Ic	NL	NL
	L	NL	50	70 Vce	70 Ic	70	NL
	M	125	NL	75 Vce	75 Ic	NL	NL
	W	NL	70	NL	NL	NL	NL
	X	125	NL	100 Vce	100 Ic	NL	NL

KEY: NL = Not Listed
PORV = Percent of Rated Value

Table 6-4 Silicon Bipolar Power Transistor Stress Derating Criteria

Classification	Derating Parameter	Level I	Level II	Level III
Silicon Bipolar	Maximum Junction Temp. (deg C) Power Dissipation (PORV) Safe Operating Area (PORV) Breakdown Voltage (PORV)	95 50 70 Vce 60 Ic 65	125 60 75 Vce 65 Ic 85	135 70 80 Vce 70 Ic 90

KEY: PORV - Percent of Rated Value

6.2 GaAs POWER TRANSISTORS

Although both JFET and MOSFET styles of GaAs transistors exist, the most common style of GaAs power transistor is the MESFET. From reviews of the available literature and supplier surveys, the primary failure mechanism for MESFETs is the interdiffusion of the deposited metal (typically aluminum or gold based) and the GaAs. Typically, the interdiffusion results in a gradual degradation in performance due to increased contact resistance, decreased drain current and reduced channel depth.

The primary stress that accelerates this process is temperature. Table 6-5 summarizes in detail the geometry, materials, ratings and life test bias conditions and results obtained from various literature and supplier sources in which the effects of temperature are well documented. It is observed that the primary failure mode has changed from one that produces catastrophic results, such as gate burn-out, to one that results in gradual degradation, such as a 5% change in I_{DD}. In most cases, an activation energy was calculated, such that a lifetime prediction could be made based on channel temperature. These predictions are shown graphically in figure 6-2. It is noticed that, at high temperatures where the life test was monitored, most of the references showed fairly consistent results. The only exception was reference 154. The mean and standard deviation of the extrapolated lifetimes from the other references enables an approximation of the probability of success to be calculated for a given temperature. The 0.5 (mean), 0.9000, 0.9900 and 0.9990 probabilities of success are shown graphically in figure 6-3. By evaluating each curve at its intersection with the 5 log-hour lifetime line (100,000 hours), and assuming the same relationship between probability of success and criticality level that was assumed for GaAs MIMICs, the maximum junction temperature can be evaluated for each criticality level. The maximum channel temperatures for GaAs power MESFETs are 85, 100 and 125 degrees Celsius for criticality levels I, II and III, respectively.

Table 6-5 GaAs Power MESFET Lifetest Data

REF.	Supplier Information		Geometry			Materials			
	Name	Part Type	Gate Length (um)	Gate Width (mm)	Gate Fingers	Starting Material	Gate Metal	Ohmic Metal	Passivation
138	NL	NL	1.8 - 2.4	6	12	Cr Doped	Al	AuGe-Ag-Au-Ti-Pt-Au	SiO2
138	NL	NL	1.8 - 2.4	6	12	Cr Doped	Al	AuGe-Ag-Au-Ti-Pt-Au	SiO2
138	NL	NL	1.8 - 2.4	6	12	Cr Doped	Al	AuGe-Ag-Au-Ti-Pt-Au	Si3N4
138	NL	NL	1.8 - 2.4	6	12	Cr Doped	Al	AuGe-Ag-Au-Ti-Pt-Au	Si3N4
138	NL	NL	1.8 - 2.4	6	12	Cr Doped	Al	AuGe-Ag-Au-Ti-Pt-Au	SiO2
138	NL	NL	1.8 - 2.4	6	12	Cr Doped	Al	AuGe-Ag-Au-Ti-Pt Au	SiO2
138	NL	NL	1.8 - 2.4	6	12	Cr Doped	Al	AuGe-Ag-Au-Ti-Pt-Au	SiO2
134	NL	NL	2	6	12	Cr Doped	Al	AuGe-Ag-Au-Ti-Pt-Au	Si3N4
134	NL	NL	2	6	12	Cr Doped	Al	AuGe-Ag-Au-Ti-Pt-Au	Si3N4
134	NL	NL	2	6	12	Cr Doped	Al	AuGe-Ag-Au-Ti-Pt-Au	Si3N4
134	NL	NL	2	6	12	Cr Doped	Al	AuGe-Ag-Au-Ti-Pt-Au	Si3N4
134	NL	NL	2	6	12	Cr Doped	Al	AuGe-Ag-Au-Ti-Pt-Au	Si3N4
141	Fujitsu	FLM7785-4C	0.8	10.8	NL	NL	Al	Ti-Pt-Au	NL
141	Fujitsu	FLM7785 4C	0.8	10.8	NL	NL	Al	Ti-Pt-Au	NL
141	Fujitsu	FLM7785-4C	0.8	10.8	NL	NL	Al	Ti-Pt-Au	NL
141	Fujitsu	FLK022WG	0.8	0.6	NL	NL	Al	Ti-Pt-Au	NL
141	Fujitsu	FLK022WG	0.8	0.6	NL	NL	Al	Ti-Pt-Au	NL
141	Fujitsu	FLM7785-4C	0.8	10.8	NL	NL	Al	Ti-Pt-Au	NL
141	Fujitsu	FLM7785-4C	0.8	10.8	NL	NL	Al	Ti-Pt-Au	NL
142	NEC	NL	0.5	3	10	Cr Doped	Al	AuGe-Ni-Ti-Au	SiO2/SiN
142	NEC	NL	0.5	3	10	Cr Doped	Al	AuGe-Ni-Ti-Au	SiO2/SiN
142	NEC	NL	0.5	3	10	Cr Doped	Al	AuGe-Ni-Ti-Au	SiO2/SiN
142	NEC	NL	0.5	3	10	Cr Doped	Ti-Al-Ti	AuGe-Ni-Ti-Au	SiO2/SiN
142	NEC	NL	0.5	3	10	Cr Doped	Ti-Al-Ti	AuGe-Ni-Ti-Au	SiO2/SiN
142	NEC	NL	0.5	3	10	Cr Doped	Ti-Al-Ti	AuGe-Ni-Ti-Au	SiO2/SiN
142	NEC	NL	0.5	3	10	Cr Doped	Ti-Al	AuGe-Ni-Ti-Au	SiO2/SiN
142	NEC	NL	0.5	3	10	Cr Doped	Ti-Al	AuGe-Ni-Ti-Au	SiO2/SiN
158	Raytheon	NL	0.8	0.4	8	NL	Al	NL	SiO2
158	Raytheon	RLK 9027	0.8	0.8	8	NL	Al	NL	SiO2
154	NL	NL	1.0	4.8	24	NL	Ti-W-Au	AuGe-Ni-Ti-Pt-Au	None
154	NL	NL	1.0	4.8	24	NL	Ti-W-Au	AuGe-Ni-Ti-Pt-Au	None
154	NL	NL	1.0	4.8	24	NL	Ti-W-Au	AuGe-Ni-Ti-Pt-Au	None
157	NL	NL	0.6	3	NL	NL	Ti-Al	NL	SiO2
157	NL	NL	0.6	3	NL	NL	Ti-Al	NL	SiO2
157	NL	NL	0.6	3	NL	NL	Al	NL	SiO2
121	Avantek	AT-8140	NL	5	40	NL	NL	NL	SiO2
121	Avantek	AT-8140	NL	5	40	NL	NL	NL	SiO2
121	Avantek	AT-8140	NL	5	40	NL	NL	NL	SiO2

KEY: NL - Not Listed

Table 6-5 GaAs Power MESFET Lifetest Data (continued)

REF.	Ratings				Life Test Data						
	Power (W)	Vp (volts)	Idss (A)	Frequency (GHz)	Bias	Ids (A)	Vds (volts)	Tch (deg C)	Pin (dBm)	Pout (dBm)	Frequency (GHz)
138	NL	NL	NL	NL	DC	0.55	14	260	0	0	0
138	NL	NL	NL	NL	DC	0.5-0.6	14	310	0	0	0
138	NL	NL	NL	NL	DC	0.55	14	270	0	0	0
138	NL	NL	NL	NL	RF	0.55	14	255	28	NL	4
139	NL	NL	NL	NL	DC	0.55	14	160	0	0	0
138	NL	NL	NL	NL	DC	0.55	14	208	0	0	0
138	NL	NL	NL	NL	DC	0.55	14	265	0	0	0
134	5	6.0-7.3	1.34-1.36	4	DC	0.55	14	175	0	0	0
134	5	6.0-7.3	1.34-1.36	4	DC	0.55	14	210	0	0	0
134	5	6.0-7.3	1.34-1.36	4	DC	0.55	14	250	0	0	0
134	5	6.0-7.3	1.34-1.36	4	RF	0.55	14	210	28	NL	4
134	5	6.0-7.3	1.34-1.36	4	RF	0.55	14	250	28	NL	4
141	4	NL	NL	NL	RF	0.5 Idss	10	210	29	NL	8
141	4	NL	NL	NL	RF	0.5 Idss	10	230	29	NL	8
141	4	NL	NL	NL	RF	0.5 Idss	10	250	29	NL	8
141	0.2	NL	NL	NL	RF	0.5 Idss	10	230	13	NL	6.2
141	0.2	NL	NL	NL	RF	0.5 Idss	10	250	13	NL	6.2
141	4	NL	NL	NL	RF	0.5 Idss	10	240	29	NL	8
141	4	NL	NL	NL	RF	0.5-0.7 Idss	10	250	29	NL	8
142	NL	NL	NL	NL	DC	0.3	8	240	0	0	0
142	NL	NL	NL	NL	DC	0.3	8	270	0	0	0
142	NL	NL	NL	NL	DC	0.3	8	300	0	0	0
142	NL	NL	NL	NL	DC	0.3	8	240	0	0	0
142	NL	NL	NL	NL	DC	0.3	8	270	0	0	0
142	NL	NL	NL	NL	DC	0.3	8	300	0	0	0
142	NL	NL	NL	NL	DC	0.3	8	270	0	0	0
142	NL	NL	NL	NL	DC	0.3	8	300	0	0	0
158	0.25	NL	NL	18	RF	NL	10	228	40 mW	100 mW	9.5
153	0.50	NL	NL	18	RF	NL	10	280	55 mW	135 mW	9.5
154	2	(Vds=9V)	0.9-1.6	7.5	RF	0.403-0.755	6.00	150	25.5 dB	30.3-31.3	7.5
154	2	(Vds=9V)	0.9-1.6	7.5	RF	0.375-0.727	6.18	190	25.5 dB	29.3-30.3	7.5
154	2	(Vds=9V)	0.9-1.6	7.5	RF	0.402-0.512	6.32	225	25.5 dB	29.4-31.0	7.5
157	NL	NL	NL	NL	DC	0.3	8	268	0	0	0
157	NL	NL	NL	NL	DC	0.3	8	298	0	0	0
157	NL	NL	NL	NL	DC	0.3	8	268	0	0	0
121	30 dB	-3	1.0	8	DC	NL	NL	225	0	0	0
121	30 dB	-3	1.0	8	DC	NL	NL	250	0	0	0
121	30 dB	-3	1.0	8	DC	NL	NL	275	0	0	0

KEY: NL - Not Listed

Table 6-5 GaAs Power MESFET Lifetest Data (continued)

REF.	Failure Data									
	Failure Mode	Quantity Stressed	Quantity Failed	Duration (hours)	Ea (eV)	Hours	Tch (deg C)	Distribution Type	Mean (log hours)	Sigma (log hours)
138	Burn-out	119	48	2000	NL	NL	NL	log-normal	3.26	1.19
138	Burn-out	60	60	2500	NL	NL	NL	log-normal	2.22	0.59
138	Burn-out	38	10	3000	NL	NL	NL	log-normal	4.35	1.63
138	Burn-out	38	14	3000	NL	NL	NL	log-normal	3.46	0.91
138	Burn-out	64	5	2500	0.86	4.0E5	160	log-normal	5.60	3.31
138	Burn-out	54	7	1000	0.86-1.64	4.0E4	208	log-normal	4.60	3.88
138	Burn-out	94	58	2000	1.64	743	265	log-normal	2.87	1.93
134	5% Idss	139	0	7740	NL	NL	NL	NL	NL	NL
134	5% Idss	56	0	7700	NL	NL	NL	NL	NL	NL
134	5% Idss	16	8	6600	1.8	25[illegible]	250	log-normal	2.40	0.32
134	5% Idss	14	0	3020	1.8	6456	210	log-normal	3.81	0.50
134	5% Idss	16	8	6660	1.8	251	250	log-normal	2.40	0.32
141	5% Idss	8	0	10,000	NL	NL	NL	NL	NL	NL
141	Burn-out	16	9	7250	1.17	6590	230	log-normal	3.82	0.30
141	Burn-out	8	8	2850	1.17	2350	250	log-normal	3.37	0.30
141	Burn-out	16	1	10,000	1.22	12,700	230	log-normal	4.10	0.30
141	Burn-out	8	7	5040	1.22	4330	250	log-normal	3.64	0.30
141	Burn-out	8	5	3210	1.17	3950	240	log-normal	3.60	0.30
141	5% Idss	8	0	5000	NL	NL	NL	NL	NL	NL
142	Migration	8	NL	NL	1.0	1.0E6	130	NL	3.32	NL
142	Migration	8	NL	NL	1.0	1.0E6	130	NL	2.78	NL
142	Migration	8	NL	NL	1.0	1.0E6	130	NL	2.29	NL
142	Vgbd	8	NL	NL	1.0	1.4E6	130	NL	3.46	NL
142	Vgbd	8	NL	NL	1.0	1.4E6	130	NL	2.92	NL
142	Vgbd	8	NL	NL	1.0	1.4E6	130	NL	2.44	NL
142	Vgbd	8	NL	NL	1.0	1.0E7	130	NL	3.78	NL
142	Vgbd	8	NL	NL	1.0	1.0E7	130	NL	3.29	NL
158	5% Idss	7	4	3300	1.0	6.0E6	100	log-normal	3.32	0.78
158	5% Idss	7	7	300	1.0	6.0E6	100	log-normal	2.08	0.46
154	dPo > 1dB	8	8	2638	1.5	65,000	125	NL	3.36	NL
154	dPo > 1dB	12	12	1104	1.5	1.0E7	80	NL	2.14	NL
154	dPo > 1dB	7	7	770	1.5	NL	NL	NL	0.95	NL
157	Burn-out	NL	2	2000	> 0.8	8.8E5	130	log-normal	3.36	0.26
157	Burn-out	NL	3	2000	> 0.8	2.9E6	110	log-normal	3.00	0.26
157	Burn-out	NL	5	1000	NL	NL	NL	log-normal	2.52	0.90
121	Burn-out	NL	NL	NL	1.44	10,400	225	log-normal	3.68	1.40
121	Burn-out	NL	NL	NL	1.44	3000	250	log-normal	3.00	1.40
121	Burn-out	NL	NL	NL	1.44	700	275	log-normal	2.30	1.40

KEY: NL - Not Listed

Figure 6-2 Lifetest Results for GaAs Power MESFETs

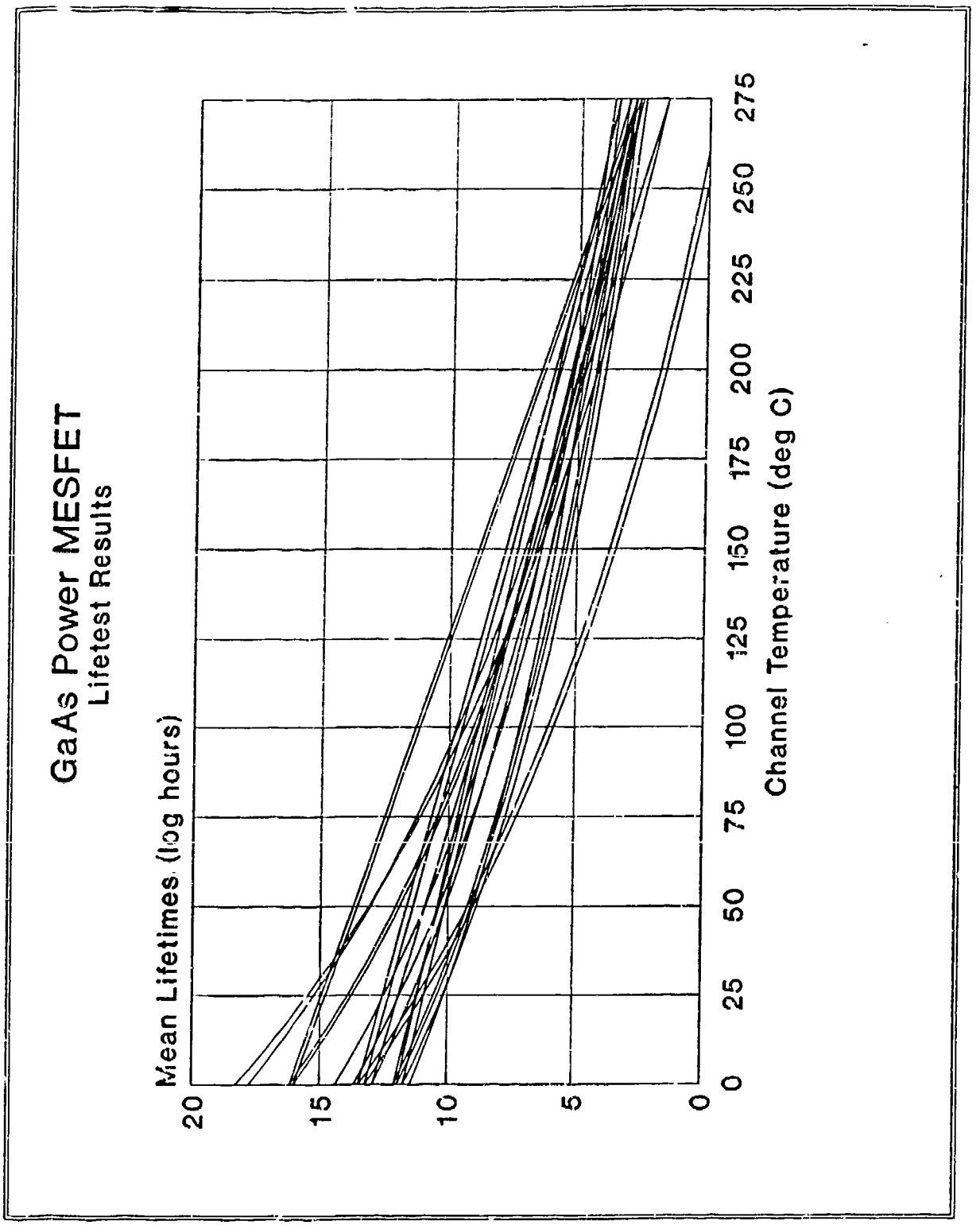
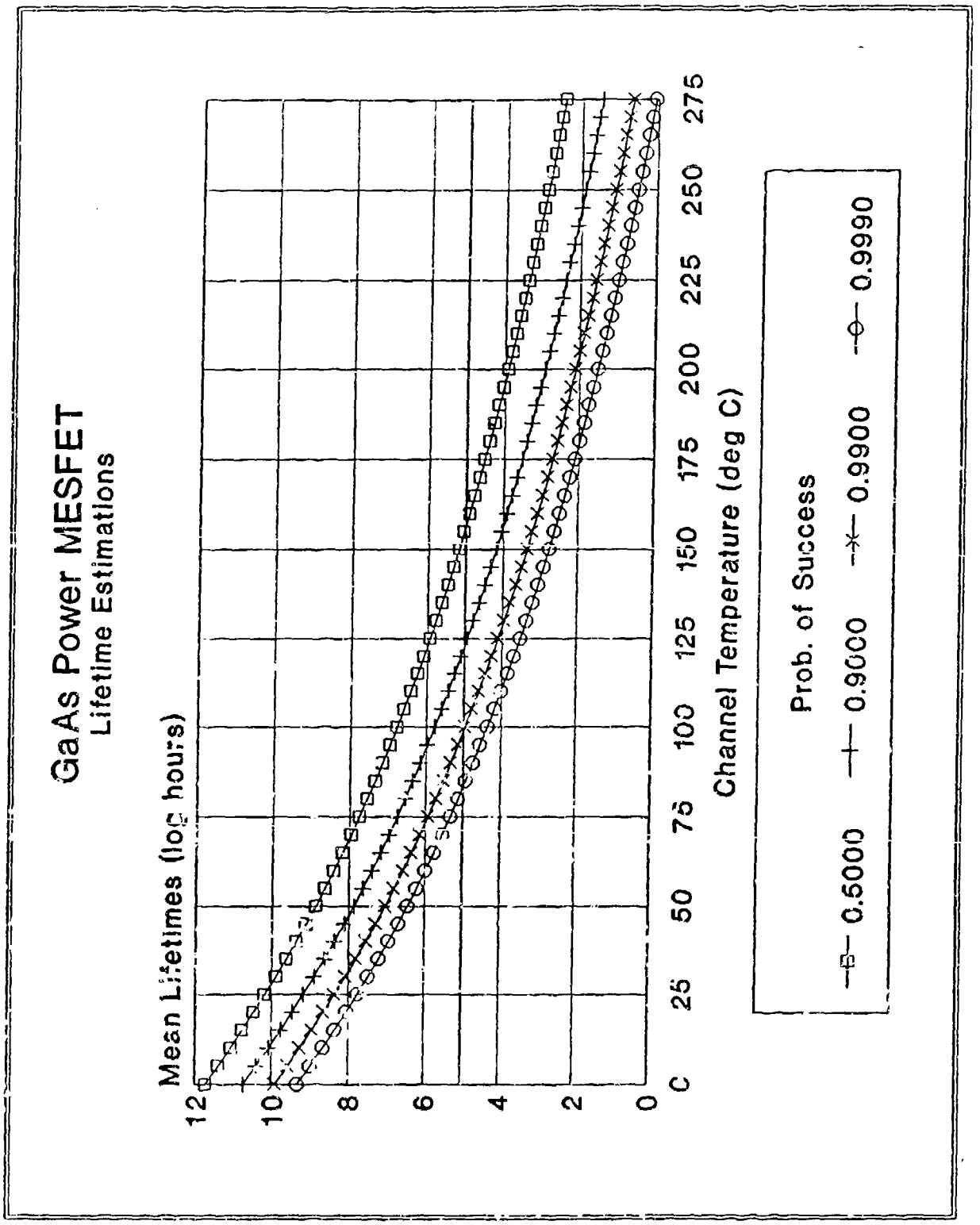


Figure 6-3 GaAs Power MESFET Lifetime Prediction



Supplementing the channel temperature derating parameter was the stress derating parameters outlined by other derating guideline sources as shown in table 6-6. In keeping with the general approach outlined in Section 3.0, and because of the uncertainty of criticality assumed with guideline sources not specifying three criticality levels, only those guideline sources supplying derating criteria for three criticality levels were evaluated for inclusion in the updated guidelines. For each parameter specified by these guideline sources, a median value for the parameter was chosen. In the case where the choice was between an even number of values, the average of the two median values was calculated and then rounded up. The remaining guideline sources were used only as a "sanity check" of the updated stress derating criteria. From a thorough review of the literature, it was determined that currently accepted derating policies are adequate in supplementing the channel temperature derating parameter in providing the margins of safety and success needed for the application. Table 6-7 summarizes the new stress derating criteria for GaAs power transistors.

Table 6-6 GaAs Power Transistor Guidelines

CRITICALITY LEVEL	GUIDELINE	MAXIMUM CHANNEL TEMPERATURE (deg C)	POWER DISSIPATION (PORV)	BREAKDOWN VOLTAGE (PORV)	ON-OFF TEMPERATURE CYCLES
I	A&B	95	50	60	NL
	C	95	50	60	NL
	D	95	50	60	NL
	E	(55 PORV)	50	60	Fig. 6-4
	F	(55 PORV)	55	60	Fig. 6-4
II	A&B	105	60	70	NL
	C	105	60	70	NL
	D	105	60	70	NL
	E	(70 PORV)	65	70	Fig. 6-4
	F	(80 PORV)	80	70	Fig. 6-4
III	A&B	125	70	70	NL
	C	125	70	70	NL
	D	125	70	70	NL
	E	(80 PORV)	80	80	Fig. 6-4
	F	(90 PORV)	90	80	Fig. 6-4
NONE SPECIFIED	G	NL	NL	NL	NL
	H	NL	NL	NL	NL
	J	NL	NL	NL	NL
	K	NL	NL	NL	NL
	L	NL	NL	NL	NL
	M	NL	NL	NL	NL
	W	82 PORV	70	70	NL
	X	125	NL	NL	NL

KEY: NL = Not Listed
PORV = Percent of Rated Value

Table 6-7 GaAs Power Transistor Stress Derating Criteria

Classification	Derating Parameter	Level I	Level II	Level III
GaAs MESFET	Maximum Channel Temp. (deg C)	85	100	125
	Power Dissipation (PORV)	50	60	70
	Breakdown Voltage (PORV)	60	70	70

KEY: PORV - Percent of Rated Value

6.3 POWER MOSFETs

MOSFETs cannot be derated in the same way as bipolar junction transistors because the devices are constructed and operate differently. MOSFETs have considerably higher input impedance than bipolar transistors, which makes them suitable for microwave systems. MOSFETs also have a negative temperature coefficient at high current levels, resulting in the current decreasing with increasing temperature. This characteristic provides for temperature stability and prevents the FET from thermal runaway or second breakdown. Consequently, MOSFETs have found increased acceptance as power devices.

From a thorough review of the literature, it was determined that currently accepted derating policies are adequate in providing those margins of safety and success needed for the application. The stress derating criteria for power MOSFET transistors outlined by other derating guideline sources is shown in table 6-8. In keeping with the general approach outlined in Section 3.0, and because of the uncertainty of criticality assumed with guideline sources not specifying three criticality levels, only those guideline sources supplying derating criteria for three criticality levels were evaluated for inclusion in the updated guidelines. For each parameter specified by these guideline sources, a median value for the parameter was chosen. In the case where the choice was between an even number of values, the average of the two median values was calculated and then rounded up. The remaining guideline sources were used only as a "sanity check" of the updated stress derating criteria. Table 6-9 summarizes the new stress derating criteria for power MOSFET transistors.

Table 6-8 Power MOSFET Transistor Guidelines

CRITICALITY LEVEL	GUIDELINE	MAXIMUM JUNCTION TEMPERATURE (deg C)	POWER DISSIPATION (PORV)	SAFE OPERATING AREA (PORV), Vce	SAFE OPERATING AREA (PORV), Ic	BREAKDOWN VOLTAGE (PORV)	ON-OFF TEMPERATURE CYCLES
I	A&B	95	50	NL	NL	60	NL
	C	95	50	NL	NL	60	NL
	D	NL	NL	NL	NL	NL	NL
	E	(55 PORV)	50	NL	NL	60	Fig. 6-4
	F	(55 PORV)	55	55 Vce	55 Ic	60	Fig. 6-4
II	A&B	105	60	NL	NL	70	NL
	C	105	60	NL	NL	70	NL
	D	NL	NL	NL	NL	NL	NL
	E	(70 PORV)	65	NL	NL	70	Fig. 6-4
	F	(80 PORV)	80	80 Vce	80 Ic	70	Fig. 6-4
III	A&B	125	70	NL	NL	70	NL
	C	125	70	NL	NL	70	NL
	D	NL	NL	NL	NL	NL	NL
	E	(80 PORV)	80	NL	NL	80	Fig. 6-4
	F	(90 PORV)	90	90 Vce	90 Ic	80	Fig. 6-4
NONE SPECIFIED	G	60	60	75 Vce	75 Ic	NL	NL
	H	110	50	75 Vce	60 Ic	65	NL
	J	110	50	75 Vcc	70 Ic	NL	NL
	K	125	50	(75 Vds)	(75 Id)	NL	NL
	L	NL	50	70 Vce	70 Ic	70	NL
	M	125	NL	NL	NL	75	NL
	W	NL	NL	NL	NL	70	NL
	X	125	NL	100 Vcu	100 Ic	NL	NL

KEY NL = Not Listed
PORV = Percent of Rated Value

Table 6-9 Power MOSFET Transistor Stress Derating Criteria

Classification	Derating Parameter	Level I	Level II	Level III
Silicon MOSFET	Maximum Junction Temp. (deg C) Power Dissipation (PDRV) Breakdown Voltage (PDRV)	95 50 60	120 65 70	140 75 75

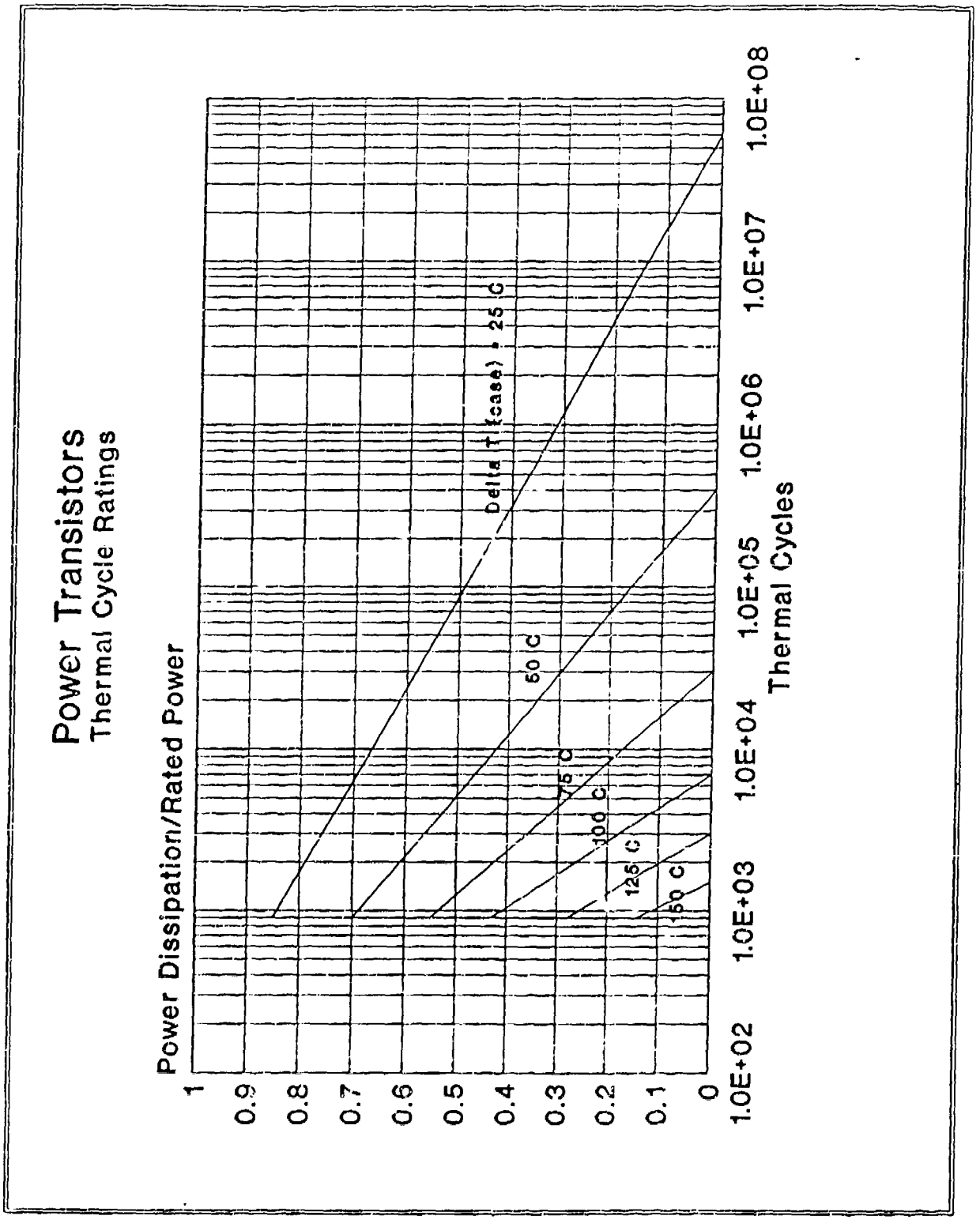
KEY: PDRV - Percent of Rated Value

6.4 POWER TRANSISTOR APPLICATION NOTES

The following application notes for power transistors were developed from a review of applicable literature, supplier surveys and other stress derating guidelines. These application notes may also be found in Appendix A.

1. Power transistors may be sensitive to ESD.
2. Design margins should be used for gain (+/- 10% for screened devices; +/- 20% for unscreened devices), leakage current (+100%), switching times (+ 20%) and saturation voltage (+/- 15%).
3. Heat sinks may be required to maintain derated junction/channel temperatures.
4. SOA curves, adjusted for junction/channel temperature, should not be exceeded under any transient conditions.
5. The number of on-off cycles (temperature cycles) should be limited according the derated power as shown in figure 6-4.

Figure 6-4 On-Off Cycling Limits for Power/Pulse Transistors



7.0 RF TRANSISTOR DERATING GUIDELINES

RF pulse transistors and RF multitransistor packages have typically operated in the low microwave frequency range and have been largely silicon NPN transistors. However, because of the advances in performance and reliability of GaAs transistors, many of the silicon RF pulse transistors are being replaced by GaAs MESFETs.

Some of the critical parameters and construction details for RF pulse and microwave transistors include current gain, switching time, doping level in the base, maximum open circuit voltage (breakdown voltage), off impedance, on impedance, emitter stripe width, base thickness package and wafer parasitics and active area geometry, including interdigitated, overlay and mesh types.

Significant failure mechanisms of RF pulse transistors includes electromigration, corrosion, intermetallic formation on bonds, reverse junction leakage and secondary breakdown. Narrow base widths can result in collector emitter shorts due to temperature accelerated diffusion spikes and pipes if bulk silicon defects such as dislocations and stacking faults are present. Thermal resistance problems can occur on RF transistors and attention to die size, die attach method, package type and application, heat sinks and air flow are important factors relating to the derating criteria. It is noted that the newer device styles are more powerful, more sensitive and cover greater bandwidths, although the basic technologies are the same. Therefore, the updated stress derating criteria for RF pulse transistors and RF multitransistor packages has not changed from the current stress derating criteria, with the exception that perhaps greater attention to detail is required. This attention to detail is highlighted in the following two examples.

In this example, a thermal runaway failure was observed in a microwave multitransistor (NPN) package (see figure 7-1). In this package, two 4-transistor arrays were mounted next to each other. During the failure analysis, it was determined that in the assembly operation, the second array was not mounted properly. The array was sitting on top of the edge of the first array (see figure 7-2). The greatly increased thermal resistance at that end of the array resulted in thermal overstress and eventual catastrophic failure of the multitransistor package.

Other than this analysis, no additional information was accumulated on RF multitransistor packages that indicated a difference between the behavior of RF multitransistor packages and RF single transistor packages. Therefore, it is concluded that the stress derating for these packages should be no different than for RF single transistor packages. It is recommended that the stress derating criteria and associated application notes for RF transistors outlined by the current version of the Guidelines should be followed for RF multitransistor packages.

In a second example, failure analysis performed on 118 RF pulse transistor field failures of SPS-40 transmitters identified 76 of the failures to be related to MOS capacitor overvoltage, high RF voltages due to reflection, transistor mismatch and thermal increases due to reduced die attach. A detailed thermal analysis identified worst case junction temperatures of 87 degree Celsius, well within the required derating. The RF transistors were rated at 50 volts and were not expected to see more than the transistor emitter-base breakdown voltage of 6 volts. However, it was possible to develop RF voltages across the MOS capacitors considerably higher than the emitter-base breakdown voltage when looking at 35 watts of pulsed 450 MHz power. The emitter-base junction breaks down without damage, but the capacitor dielectric breaks down as an irreversible short. Good engineering practices need to supplement any derating policy in order to obtain an acceptable level of safety and success.

Figure 7-1 Catastrophic Damage in an RF Multitransistor Package

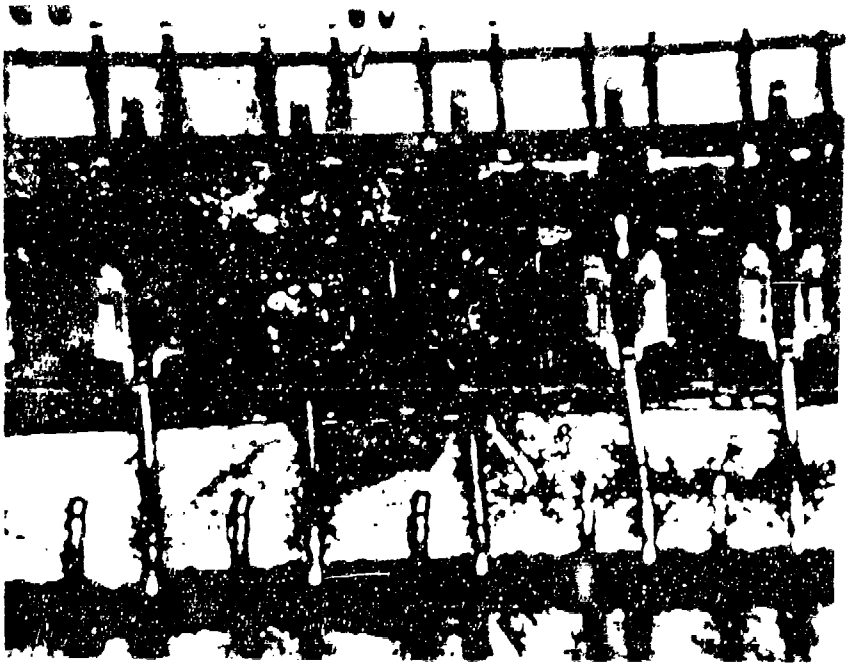
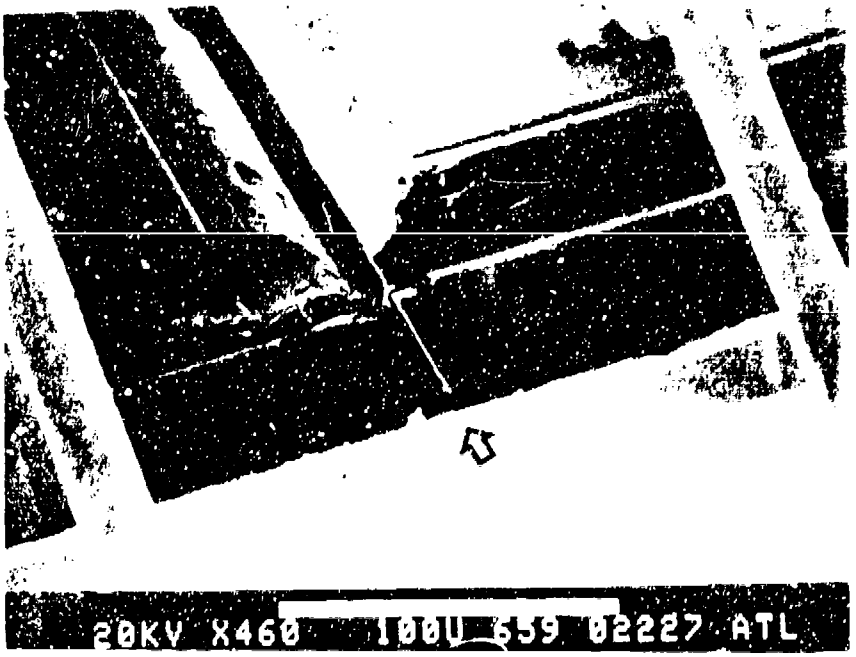


Figure 7-2 Assembly Problem Resulting in Thermal Runaway



Although studies are being performed[160-163] to better understand the effects of peak pulse power per unit gate width, the number of pulses in a pulse train and the duty cycle of the pulse train on the failure rate of RF pulse transistors, the data from these studies does not provide enough insight into modifying current stress derating guidelines for RF pulse transistors.

The stress derating criteria for RF pulse transistors was developed similarly to the stress derating criteria for power transistors. The channel temperature stress derating developed for GaAs power MESFETs is also considered applicable for the GaAs RF pulse transistors. The stress derating criteria for RF pulse transistors outlined by other derating guideline sources is shown in tables 7-1 and 7-2 for silicon bipolar RF pulse transistors and GaAs pulse MESFETs, respectively. In keeping with the general approach outlined in Section 3.0, and because of the uncertainty of criticality assumed with guideline sources not specifying three criticality levels, only those guideline sources supplying derating criteria for three criticality levels were evaluated for inclusion in the updated guidelines. For each parameter specified by these guideline sources, a median value for the parameter was chosen. In the case where the choice was between an even number of values, the average of the two median values was calculated and then rounded up. The remaining guideline sources were used only as a "sanity check" of the updated stress derating criteria. Table 7-3 summarizes the new stress derating criteria for RF pulse transistors.

Table 7-1 Silicon Bipolar RF Pulse Transistor Guidelines

CRITICALITY LEVEL	GUIDELINE	MAXIMUM JUNCTION TEMPERATURE (deg C)	POWER DISSIPATION (PORV)	SAFE OPERATING AREA (PORV), Vce	SAFE OPERATING AREA (PORV), Ic	BREAKDOWN VOLTAGE (PORV)	ON-OFF TEMPERATURE CYCLES
I	A&B	95	50	70 Vce	50 Ic	60	NL
	C	95	50	NL	NL	60	NL
	D	NL	NL	NL	NL	NL	NL
	E	NL	NL	70 Vce	60 Ic	60	Fig. 6-4
	F	(55 PORV)	55	55 Vce	55 Ic	60	Fig. 6-4
II	A&B	105	60	70 Vce	60 Ic	70	NL
	C	105	60	NL	NL	70	NL
	D	NL	NL	NL	NL	NL	NL
	E	(70 PORV)	NL	70 Vce	80 Ic	NL	Fig. 6-4
	F	(80 PORV)	80	80 Vce	80 Ic	70	Fig. 6-4
III	A&B	125	70	70 Vce	60 Ic	70	NL
	C	125	70	NL	NL	70	NL
	D	NL	NL	NL	NL	NL	NL
	E	(80 PORV)	NL	70 Vce	60 Ic	NL	Fig. 6-4
	F	(90 PORV)	90	90 Vce	90 Ic	80	Fig. 6-4
NONE SPECIFIED	G	NL	NL	NL	NL	NL	NL
	H	NL	NL	NL	NL	NL	NL
	J	110	50	75 Vce	70 Ic	NL	NL
	K	NL	NL	NL	NL	NL	NL
	L	NL	50	70 Vce	70 Ic	70	NL
	M	125	NL	75 Vce	75 Ic	NL	NL
	W	NL	70	NL	NL	NL	NL
	X	NL	NL	NL	NL	NL	NL

KEY: NL = Not Listed
PORV = Percent of Rated Value

Table 7-2 GaAs RF Pulse Transistor Guidelines

CRITICALITY LEVEL	GUIDELINE	MAXIMUM CHANNEL TEMPERATURE (deg C)	POWER DISSIPATION (PORV)	BREAKDOWN VOLTAGE (PORV)	ON-OFF TEMPERATURE CYCLES
I	A&B	95	50	60	NL
	C	95	50	60	NL
	D	95	50	60	NL
	E	(55 PORV)	50	60	Fig. 6-4
	F	(55 PORV)	55	60	Fig. 6-4
II	A&B	105	60	70	NL
	C	105	60	70	NL
	D	105	60	70	NL
	E	(70 PORV)	65	70	Fig. 6-4
	F	(80 PORV)	80	70	Fig. 6-4
III	A&B	125	70	70	NL
	C	125	70	70	NL
	D	125	70	70	NL
	E	(80 PORV)	80	80	Fig. 6-4
	F	(90 PORV)	90	80	Fig. 6-4
NONE SPECIFIED	G	NL	NL	NL	NL
	H	NL	NL	NL	NL
	J	NL	NL	NL	NL
	K	NL	NL	NL	NL
	L	NL	NL	NL	NL
	M	NL	NL	NL	NL
	W	82 PORV	70	70	NL
	X	NL	NL	NL	NL

KEY: NL = Not Listed
PORV = Percent of Rated Value

Table 7-3 RF Pulse Transistor Stress Derating Guidelines

Classification	Derating Parameter	Level I	Level II	Level III
Silicon Bipolar	Maximum Junction Temp. (deg C)	95	125	135
	Power Dissipation (PORV)	50	60	70
	Safe Operating Area (PORV)	70 Vce 60 Ic	70 Vce 60 Ic	70 Vce 60 Ic
	Breakdown Voltage (PORV)	65	85	90
GaAs MESFET	Maximum Channel Temp. (deg C)	85	100	125
	Power Dissipation (PORV)	50	60	70
	Breakdown Voltage (PORV)	60	70	70

KEY: PORV - Percent of Rated Value

APPLICATION NOTES

The following application notes for RF pulse transistors were developed from a review of applicable literature, supplier surveys and other stress derating guidelines. These application notes may also be found in Appendix A.

1. RF transistors may be sensitive to ESD.
2. Design margins should be used for gain (+/- 10% for screened devices; +/- 20% for unscreened devices), leakage current (100%), switching times (+ 20%) and saturation voltage (+/- 15%).
3. Heat sinks may be required to maintain derated junction/channel temperatures.
4. The design may require exceeding voltage and power derating limits, but junction/channel temperature limits should be observed at all times.
5. The number of on-off cycles (temperature cycles) should be limited according the derated power as shown in figure 6-4.

8.0 OPTO-ELECTRONIC DEVICE DERATING GUIDELINES

The approach to the development of the stress derating criteria for opto-electronic components was initiated in a fashion similar to the approach used for silicon bipolar power transistors. However, it was realized that the differences between the reliability models of MIL-HDBK-217D Notice 1 and MIL-HDBK-217E Notice 1 resulted in up to several orders of magnitude difference in (improved) predicted failure rates. The quality factor had changed 2400% to 7000%, and the PiT factor of MIL-HDBK-217E Notice 1 utilizes an activation energy of approximately one third of the activation energy used in MIL-HDBK-217D Notice 1. The use of the silicon bipolar power transistor approach to stress derating would have resulted in virtually no stress derating required to meet the failure rates that were considered acceptable at the time the current version of the Guidelines was released. As an alternative approach, the development of updated "acceptable" failure rates for the three criticality levels was considered. The failure rates that can be obtained by applying currently accepted derating guidelines to the reliability models were deemed to be as "acceptable" as any other values chosen. Therefore, without having to do the failure rate calculations and the reverse stress analysis, the currently accepted guidelines become the updated stress derating criteria

The stress derating criteria for opto-electronic devices, including photo transistors, photo diodes, opto-electronic couplers, injection laser diodes and light emitting diodes, was developed by consensus of current stress derating guideline sources, as outlined in section 3.0. The stress derating criteria for opto-electronic devices outlined by other derating guideline sources is shown in table 8-1. In keeping with the general approach outlined in Section 3.0, and because of the uncertainty of criticality assumed with guideline sources not specifying three criticality levels, only those guideline sources supplying derating criteria for three criticality levels were evaluated for inclusion in the updated guidelines. Table 8-2 summarizes the new stress derating criteria for opto-electronic devices.

Crit. Level	Guideline	Derating Parameters for: (See Key Below)								
		Photo-Trans.	APD Diode	PIN Diode		Opto-Coupler	Injection Laser Diode		LED	
		1	1	1	2	1	1	3	1	4
I	A & B	NL	95	95	70	NL	95	50	95	50
	C	NL	95	95	70	NL	95	50	95	50
	D	NL	NL	NL	NL	NL	NL	NL	NL	NL
	E	(55 PORV)	(55 PORV)	(55 PORV)	60	(55 PORV)	NL	50	(55 PORV)	NL
	F	NL	NL	NL	NL	NL	NL	NL	NL	NL
II	A & B	NL	105	105	70	NL	105	60	105	65
	C	NL	105	105	70	NL	105	60	105	65
	D	NL	NL	NL	NL	NL	NL	NL	NL	NL
	E	(70 PORV)	(70 PORV)	(70 PORV)	60	(70 PORV)	NL	50	(70 PORV)	NL
	F	NL	NL	NL	NL	NL	NL	NL	NL	NL
III	A & B	NL	125	125	70	NL	110	70	110	75
	C	NL	125	125	70	NL	110	70	110	75
	D	NL	NL	NL	NL	NL	NL	NL	NL	NL
	E	(80 PORV)	(80 PORV)	(80 PORV)	60	(80 PORV)	NL	50	(80 PORV)	NL
	F	NL	NL	NL	NL	NL	NL	NL	NL	NL
None Specified	G	NL	NL	NL	NL	NL	NL	NL	NL	NL
	H	NL	NL	NL	NL	NL	NL	NL	NL	NL
	J	110	110	110	70	110	110	60	110	65
	K	NL	NL	NL	NL	NL	NL	NL	NL	NL
	L	NL	NL	NL	NL	NL	NL	NL	NL	NL
	M	NL	NL	NL	NL	NL	NL	NL	NL	NL
	W	NL	105	105	70	NL	105	60	105	65
	X	NL	NL	NL	NL	NL	NL	NL	NL	NL

KEY: Derating Parameters
1 - Maximum Junction Temperature (deg C)
2 - Reverse Voltage (PORV)
3 - Power Output (PORV)
4 - Average Forward Current (PORV)

NL - Not Listed
PORV - Percent of Rated Value

Table 8-2 Opto-electronic Device Stress Derating Guidelines

Classification	Derating Parameter	Level I	Level II	Level III
Photo Transistor	Maximum Junction Temp. (PORV)	55	70	80
Photo Diode, APD	Maximum Junction Temp. (PORV)	55	70	80
Photo Diode, PIN	Maximum Junction Temp. (PORV)	55	70	80
	Reverse Voltage (PORV)	70	70	70
Opto-coupler	Maximum Junction Temp. (PORV)	55	70	80
Injection Laser Diode	Maximum Junction Temp. (PORV)	55	70	75
	Power Output (PORV)	50	60	70
LED	Maximum Junction Temp. (PORV)	55	70	75
	Average Forward Current (PORV)	50	65	75

KEY: PORV - Percent of Rated Value

OPTO-ELECTRONIC DEVICE APPLICATION NOTES

The following application notes for opto-electronic devices were developed from a review of supplier surveys and other stress derating guidelines. These application notes may also be found in Appendix A.

Photo Diodes:

1. The gain of APDs should be derated by 3 dB to account for gradual efficiency degradation and shifts in the operating point.

Opto-couplers:

1. External bypassing may be necessary to prevent damaging internal oscillation due to very high gain circuitry within the opto-coupler.
2. Allow for 15% degradation in opto-coupler current transfer ratio (CTR) over the service life of the design. This degradation is especially prevalent at low drive current. The input drive current should be well above the turn-on point.

Light Emitting Diodes (LEDs)

1. Current limiting is required (using a series resistor).
2. Half or full wave rectified AC sine wave is not recommended for LED drive current. If rectified AC is used to drive LEDs, the peak value of the current must never exceed the allowable DC current maximum.

Injection Laser Diodes (ILDs)

1. Power supplies for ILDs must be carefully designed to completely eliminate current pulses which may cause catastrophic facet damage.
2. Output power should be given a 3 dB margin to account for gradual degradation of the device.
3. Mechanical stress, such as thermal or mechanical shock and vibration, cause crystal lattice defects (dark lines) to grow. Stress screening can be used to eliminate devices with these defects.
4. Excess optical power of ILDs will damage facets and will destroy the device. Note that optical power output is strongly temperature dependent and must be monitored and controlled to assure safe operation.
5. For SiO_2 glassivated devices, the integrity of the package hermetic seal must be maintained to prevent moisture absorption which will degrade performance.

9.0 PASSIVE COMPONENT DERATING GUIDELINES

The passive components of interest to this study were hybrid deposited film resistors, chip resistors (RM) and chip capacitors, both ceramic (CDR) and tantalum (CWR). Stress derating guidelines were developed for the chip resistors and chip capacitors only. Because no stress-failure information on hybrid deposited film resistors was identified by the literature search, supplier surveys, other stress derating guideline sources or accumulated field failure data, no stress derating guidelines for hybrid deposited film resistors could be developed.

The stress derating criteria for the chip resistor and chip capacitor was developed from a review of current stress derating guideline sources, as outlined in section 3.0. This approach was taken after finding virtually no information in the literature search[166-167] concerning stress-failure relationships of these passive components, and confirmation by suppliers that these components (virtually) do not fail. The stress derating criteria for these passive devices outlined by other derating guideline sources is shown in table 9-1. It is noted that none of the five guideline sources that typically specify three criticality levels outlined stress derating criteria for chip capacitors. Therefore, the updated stress derating for chip capacitors is based upon best engineering judgement biased by the guideline sources providing only one criticality level criteria. The stress derating criteria for chip resistors was developed in a fashion similar to that for opto-electronic devices. Table 9-2 summarizes the new stress derating criteria for chip resistors and chip capacitors.

Table 9-1 Passive Device Guidelines

Crit. Level	Guideline	Derating Parameters for: (See Key Below)								
		Ceramic Chip Capacitor (CDR)			Tantalum Chip Capacitor (CWR)			Thick / Thin Film Chip Resistor (RM)		
		1	2	3	1	2	3	1	4	5
I	A & B	NL	NL	NL	NL	NL	NL	25 FML	50	NL
	C	NL	NL	NL	NL	NL	NL	25 FML	50	NL
	D	NL	NL	NL	NL	NL	NL	NL	NL	NL
	E	NL	NL	NL	NL	NL	NL	98	50	NL
	F	NL	NL	NL	NL	NL	NL	NL	NL	NL
II	A & B	NL	NL	NL	NL	NL	NL	25 FML	50	NL
	C	NL	NL	NL	NL	NL	NL	25 FML	50	NL
	D	NL	NL	NL	NL	NL	NL	NL	NL	NL
	E	NL	NL	NL	NL	NL	NL	103	60	NL
	F	NL	NL	NL	NL	NL	NL	NL	NL	NL
III	A & B	NL	NL	NL	NL	NL	NL	25 FML	50	NL
	C	NL	NL	NL	NL	NL	NL	25 FML	50	NL
	D	NL	NL	NL	NL	NL	NL	NL	NL	NL
	E	NL	NL	NL	NL	NL	NL	109	70	NL
	F	NL	NL	NL	NL	NL	NL	NL	NL	NL
None Specified	G	85	60	NL	NL	NL	NL	NL	NL	NL
	H	NL	NL	NL	NL	NL	NL	NL	NL	NL
	J	NL	NL	NL	NL	NL	NL	NL	NL	NL
	K	70	60	NL	70	50	NL	NL	NL	NL
	L	NL	NL	NL	NL	NL	NL	100	55	70
	M	NL	NL	NL	85	70	100	NL	NL	NL
	W	85 PORV	60	NL	85 PORV	60	NL	70 PORV	55	75
	X	NL	NL	NL	NL	NL	NL	NL	NL	NL

KEY: Derating Parameters
1 - Maximum Operating Temperature (deg C)
2 - DC Voltage (PORV)
3 - Maximum Surge Voltage (PORV)
4 - Power (PORV)
5 - Voltage (PORV)

NL - Not Listed
FML - From Maximum Limit
PORV - Percent of Rated Value

Table 9-2 Passive Device Stress Derating Criteria

Classification	Derating Parameter	Level I	Level II	Level III
Thick/Thin Film (RM)	Maximum Operating Temp. (PORV) Power (PORV) Voltage (PORV)	80 50 75	80 50 75	80 50 75

KEY: PORV - Percent of Rated Value

Classification	Derating Parameter	Level I	Level II	Level III
Ceramic (CCR)	Maximum Operating Temp. (PORV) DC Voltage (PORV)	85 60	85 60	85 60
Solid Tantalum (CWR)	Maximum Operating Temp. (deg C) DC Voltage (PORV)	85 60	85 60	85 60

KEY: PORV - Percent of Rated Value

PASSIVE DEVICE APPLICATION NOTES

The following application notes for passive devices were developed from a review of supplier surveys and other stress derating guidelines. These application notes may also be found in Appendix A.

Chip Resistors:

1. Chip resistors are sensitive to ESD.
2. The design should tolerate a 2% shift in resistance value.
3. Proper trimming is required to prevent latent failure in low noise applications.
4. Resistor stacking should be avoided.
5. For pulse applications, the average power calculated from pulse magnitude, duration and repetition frequency is used to establish the power derating requirement.
6. Pulse magnitude should be used to establish voltage derating requirement.
7. Film temperatures must stay below 150 degrees Celsius.
8. Voltage stress should stay less than 2 volts/mil.
9. Power density should stay less than 200 W per square inch.
10 The effective resistance value will be reduced when used at frequencies over 200 MHz because of shunt capacitance between the resistive elements and the connecting circuits.

Chip Capacitor:

1. The sum of the peak AC voltage plus any DC bias voltage must not exceed the maximum derated operating voltage.
2. Precautions outlined in MIL-STD-198E should be followed.
3. (Ceramic) A design tolerance of +/- 12% should be allowed.
4. (Tantalum) A design tolerance of +/- 8% should be allowed.

10.0 SAW DERATING GUIDELINES

The stress derating criteria for SAW devices was developed from a review of current stress derating guideline sources, as outlined in section 3.0. This approach was taken after finding virtually no information in the literature search[168] concerning stress-failure relationships of these SAW devices. The stress derating criteria for these SAW devices outlined by other derating guideline sources is shown in table 10-1. It is noted that the four of the five guideline sources that outline stress derating criteria for SAW devices are split between two sets of input power derating. Therefore, the updated stress derating for SAW devices is based upon the most recent update of these guidelines. Table 10-2 summarizes the new stress derating criteria for SAW devices.

SAW DEVICE APPLICATION NOTES

The following application notes for SAW devices were developed from a review of supplier surveys and other stress derating guidelines. These application notes may also be found in Appendix A.

1. SAW devices may be sensitive to ESD.
2. Integrity of the hermetic package must be maintained.
3. The design should not subject the SAW device to the rated maximum of shock, vibration and temperature cycling.

Table 10-1 SAW Device Guidelines

CRITICALITY LEVEL	GUIDELINE	INPUT POWER (<100 MHz) (dBm FML)	INPUT POWER (>100 MHz) (dBm FML)	INPUT POWER (<500 MHz) (dBm FML)	INPUT POWER (>500 Mhz) (dBm FML)	OPERATING TEMPERATURE (deg C)
I	A&B	20	10	NL	NL	NL
	C	NL	NL	18	13	125
	D	NL	NL	18	13	125
	E	20	10	NL	NL	NL
	F	NL	NL	NL	NL	NL
II	A&B	20	10	NL	NL	NL
	C	NL	NL	18	13	125
	D	NL	NL	18	13	125
	E	20	10	NL	NL	NL
	F	NL	NL	NL	NL	NL
III	A&B	20	10	NL	NL	NL
	C	NL	NL	18	13	125
	D	NL	NL	18	13	125
	E	20	10	NL	NL	NL
	F	NL	NL	NL	NL	NL
NONE SPECIFIED	G	NL	NL	NL	NL	NL
	H	NL	NL	NL	NL	NL
	J	NL	NL	NL	NL	NL
	K	NL	NL	NL	NL	NL
	L	NL	NL	NL	NL	NL
	M	NL	NL	NL	NL	NL
	W	20	10	NL	NL	NL
	X	NL	NL	NL	NL	NL

KEY: NL = Not Listed
FML = From Maximum Limit

Table 10-2 SAW Device Stress Derating Criteria

Classification	Derating Parameter	Level I	Level II	Level III
(All)	Input Power (<500 MHz) (FML) Input Power (>500 MHz) (FML) Operating Temperature (deg C)	+18 dBm +13 dBm 125	+18 dBm +13 dBm 125	+18 dBm +13 dBm 125

KEY: FML - From Maximum Limit

11.0 DERATING VERIFICATION

To determine the validity of the stress derating criteria, field failure data was gathered on the component types of interest to this study. Because of the difficulty in verifying space system failures, and the unavailability of consistent ground based system failure data, only avionics system failure data was collected and reduced to observed failure rates. Therefore, the verification of the effectiveness of the stress derating criteria was limited to criticality level II criteria.

The avionics systems in question included the AN/APG-66 and AN/APG-68 radars and the ALQ-131 radar jammer. The field failure data was retrieved for the years of 1988 and 1989, in which over 1500 sorties were flown for each system. In reducing the data it was understood that, although the retest OK (RTOK) failures were not included in this failure summary, not all the remaining failures were verified. This lack of verification may result in observed failure rates that are much higher than actual failure rates. This scenario is typically true for the resistors and capacitors which tend to be removed along with associated suspect failed components as a lower risk option to leaving them in place and risk another rework cycle.

Table 11-1 outlines the component types and the observed failure rates based upon the number of failures observed and the total number of device hours of operation each component type had experienced. It is noted that this observed failure rate is based upon part removals and not necessarily verified failures. Also included in table 11-1 is the predicted failure rate for criticality level II components. These predicted failure rates were generated in the same fashion as the failure rates outlined in table 3-3. Table 11-2 includes the factor values and rationale used to generate the failure rates, based on MIL-HDBK-217D Notice 1 and utilizing the stress derating criteria of the current version of the Guidelines. It is observed that, for the most part, the observed failure rate was comparable to or less than the predicted failure rate of the component. The exceptions included thick film chip resistors and ceramic chip capacitors.

Table 11-1 Stress Derating Assessment for Level II Criticality

Device Type	Observed Failures	Total Device-Hours	Observed Failure Rate	Expected Failure Rate
PROM	32	14,897,252	2.1480 fpmh	22.7459 fpmh (1)
				2.8023 fpmh (2)
Power Transistor	20	7,614,569	2.6265 fpmh	1.2917 fpmh (3)
				2.3400 fpmh (4)
RF Transistor	30	13,863,750	2.1639 fpmh	832.00 fpmh
Opto-coupler	1	361,178	2.7687 fpmh	9.6690 fpmh
LED	0	236,000	<3.3784 fpmh	0.8493 fpmh
Chip Resistor, Thick Film	226	213,201,551	1.0571 fpmh	0.0204 fpmh
Chip Resistor, Thin Film	1	33,821,532	0.0296 fpmh	0.0204 fpmh
Chip Capacitor, Ceramic	7	7,990,390	0.8761 fpmh	0.0971 fpmh

KEY: fpmh - failures per million hours

Notes: (1) MOS PROM
(2) Bipolar PROM
(3) Silicon Bipolar
(4) Silicon MOSFET

Table 11-2 Maximum Failure Rates For Criticality Level II

Device Type	Factors											Failure Rate (Lambda) (Failures /10^6 Hrs)
	Base FR (LambdaB)	Qual. (PiQ)	Com. (C1)	Temp. (PiT)	Env. (PiE)	Appl. (PiA)	P/R (PiR)	Volt. (PiS)	M Net (PiM)	F&POP (PiF)	Cap. (PiCV)	
Bipolar Power Transistor	0.0092	0.24	1.0	N/A	65.0	1.50	5.00	1.20	N/A	N/A	N/A	1.2917
Silicon Power MOSFET	0.1000	0.24	1.0	N/A	65.0	1.50	N/A	N/A	N/A	N/A	N/A	2.3400
RF Transistor	0.1000	2.00	N/A	3.25	8.0	4.00	N/A	N/A	4.0	10.0	N/A	832.00
Opto-coupler	0.0074	0.02	N/A	3843	17.0	N/A	N/A	N/A	N/A	N/A	N/A	9.6690
LED	0.0007	0.02	N/A	3843	17.0	N/A	N/A	N/A	N/A	N/A	N/A	0.8493
Resistor, Fixed Film	0.0034	0.30	N/A	N/A	20.0	N/A	1.00	N/A	N/A	N/A	N/A	0.0204
Capacitor, Ceramic	0.0071	0.30	N/A	N/A	24.0	N/A	N/A	N/A	N/A	N/A	1.90	0.0971

Device Type	Rationale									
	Qual. (PiQ)	Com. (C1)	Temp. (PiT)	Env. (PiE)	Appl. (PiA)	P/R (PiR)	Volt. (PiS)	M Net (PiM)	F&POP (PiF)	Cap. (PiCV)
Bipolar Power Transistor	JANTX	Single	N/A	AUF	Linear	200 Watts	S2=.7	N/A	N/A	N/A
Silicon Power MOSFET	JANTX	Single	N/A	AUF	Linear	N/A	N/A	N/A	N/A	N/A
RF Transistor	JANTX	N/A	105C,R=.7	AUF	Duty>30%	N/A	N/A	No Mat.	.6 P	N/A
Opto-coupler	JANTX	N/A	105 C	ARW	N/A	N/A	N/A	N/A	N/A	N/A
LED	Herm.	N/A	105 C	ARW	N/A	N/A	N/A	N/A	N/A	N/A
Resistor, Fixed Film	P	N/A	N/A	ARW	N/A	<110 Kohm	N/A	N/A	N/A	N/A
Capacitor, Ceramic	P	N/A	N/A	ARW	N/A	N/A	N/A	N/A	N/A	1.1uf

KEY: N/A = Not Applicable

Even if the unverified failure rates of the components are greater than their actual failure rates, then it would be reasonable to assume the system design engineer has been fairly successful utilizing the stress derating criteria. However, with perhaps the exception of the RF transistors which have a two order of magnitude difference between observed and expected failure rates, design engineer may not be guard banding the design more than that required by the derating guidelines. Therefore, either the stress derating guidelines must err on the conservative side or the system design engineer must be more knowledgeable of which stresses are the most critical. In the development of the updated stress derating criteria, increased flexibility was provided in the stress derating criteria such that the system design engineer may be more sensitive to the way stresses affect the reliability of his design.

Based on the data of table 11-1, it is difficult to conclude that the stress derating criteria had completely fulfilled its intent in keeping the component failure rate below a specific level for the given mission criticality. However, it is encouraging that, with the lack of verification of the assumptions concerning the failures, the observed failure rates are close to the expected failure rate target.

It is noted here that not all the device types listed in table 1-1 are included in table 11-1. The failure rate analysis could not be performed on several of the components in question for the following reasons. First, some parts (MIMICs) were not used in these systems. Second, the database structure for part traceability depends on Westinghouse internal part numbers that must be examined to determine component type (i.e., ASIC, PROM, chip capacitor, etc.). To perform this task as stated would be costly and out of scope for this contract. Therefore, an alternate approach was used to collect the failure data.

This approach first identified as many internal part numbers for each component type as possible. Then, these part numbers were compared to the as-designed parts list for each system. If a match existed, the failure

database was searched to identify the number of failures and the total operate time of the component. Unfortunately, if the initial list of component internal part numbers was not complete, it is possible that, although the component type was used in the system, it would appear as though that component type was not used.

12.0 ALTERNATE APPROACH

It is well understood that to determine the influence of each component failure on the criticality of a mission would require a complete failure modes and effects analysis (FMEA). It is also well understood that, depending upon the architecture of a system, it is possible to have the same style of component in two circuits of different criticality. In one circuit, failure of the component may result in total mission failure. In the other circuit, failure of the component may result in only degraded performance. However, because the system mission is of level II criticality, for example, the application stresses applied to both components are derated according to the level II derating criteria. Actually, the mission-critical component might have been better derated according to level I criteria and the other component might have been better derated according to level III criteria. By choosing only level II criteria for both components, the mission is potentially in more jeopardy due to component 1 and the circuit design is overly constrained due to component 2. Unfortunately, this scenario is valid for most system designs, and deciding which criticality level should be used for which component in a given application is futile. An alternate approach to stress derating of components that can address this dilemma is proposed.

It is typical, early in the design phase, to perform a reliability prediction on the system and allocate the reliability requirement to its subsystems. In many cases, these allocations are flowed down to the lowest subsystem level, the component level. At that time, trade-offs in system architecture are made such that the system reliability goal may be achieved. Stress derating guidelines are utilized during this design phase to assure mission safety and success. Since the criticality of each component on the desired system mission is dependent upon its role in performing the desired function, it is reasonable to derate the stress on that component according to the "mission" of the component. The level of stress derating should therefore be dependent upon the acceptable failure rate of the component in its application.

In order to derive stress derating criteria that is flexible enough to be utilized in a domain of continuous failure rates requires the stress derating criteria be based on accurate reliability models. It is noted that the updated stress derating criteria for microcircuits and MIMICs developed as part of this study was based on the updated reliability models of MIL-HDBK-217F (to be published). The only difference between the approach taken to update the current version of the Guidelines and this proposed approach is the replacement of the three levels of criticality based on system mission type with a continuous criticality scale based on component "mission".

The problem with expanding the scope of criticality levels is identifying and providing accurate values for all the variables associated with component failure. This problem is certainly apparent in the example of microcircuits. However, approximations, such as those used to develop the criteria in this study, may be made that simplify and conservatively bound the derating criteria until more accurate information is available.

As described earlier in this report, the variables of the reliability model can be separated into three categories, criticality-specific, device-specific and stress-specific. The criticality-specific parameters included the PiE and PiQ factors. These factors will typically depend upon the system mission and cannot be varied to improve the safety and success of the component mission. The remaining factors involving both device-specific and stress-specific parameters can be varied to improve the safety and success of the component mission.

A problem with evolving component reliability models is the need to incorporate time dependent failure mechanisms into these models. Since the resulting failure rate is no longer constant with time, a failure rate does not adequately describe the number of failures that might be expected, that is, the mean time between failures is no longer constant. Therefore, it may be more reasonable to describe the component reliability in terms of a probability of success after a given number of operating hours.

Given both criticality level definition and time dependent failure rate problems, it is still possible to define the appropriate stress derating criteria for a component mission. However, the format in which the stress derating criteria is to be presented may become tedious when presented in table format. Figures 12-1, 12-2 and 12-3 show graphically the stress derating criteria SOAs for component missions with probabilities of success of 0.9990, 0.9900 and 0.9000, respectively, for ASIC/VHSIC MOS digital microcircuits. It is noted that because a probability of success is used to generate the SOAs the maximum junction temperatures is no longer purely a function of gate count, when compared to figures 4-14 through 4-16 in which a constant failure rate was used to generate the SOAs. Unfortunately, to obtain insight into the SOAs for component reliability other than that for which these graphs were generated requires interpolation between the graphs. Although no suggestions are made at this time concerning an acceptable table format for this data, it may be advantageous for the design/reliability engineer to work from stress derating graphs, such as the one presented in figures 12-1 through 12-3, or better yet, the actual derating algorithms, in order to maintain an understanding of the trade-offs between component complexity, applied stress and component reliability.

The importance in making the stress derating criteria "usable" should not overwhelm the advantages in making the stress derating criteria component or board "mission" critical rather than system mission critical. The method by which system design engineers currently employ stress derating guidelines may have to change from time consuming look-ups in the tables of stress derating guideline books to efficient calculations performed concurrently on the workstation used for producing the system design.

Figure 12-1 P_S = 0.9990 SOAs for MOS Digital ASIC/VHSIC

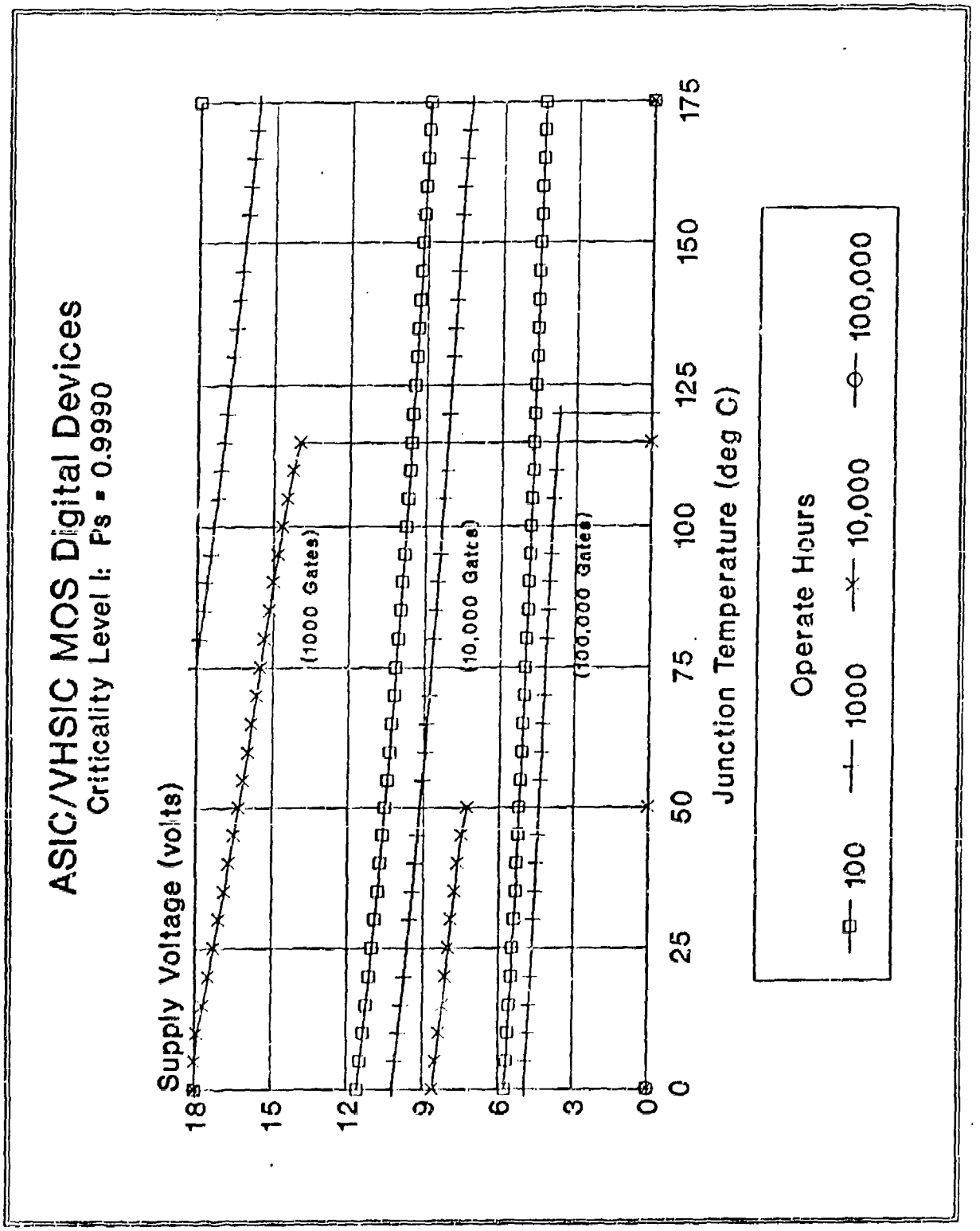


Figure 12-2 P_S = 0.9900 SOAs for MOS Digital ASIC/VHSIC

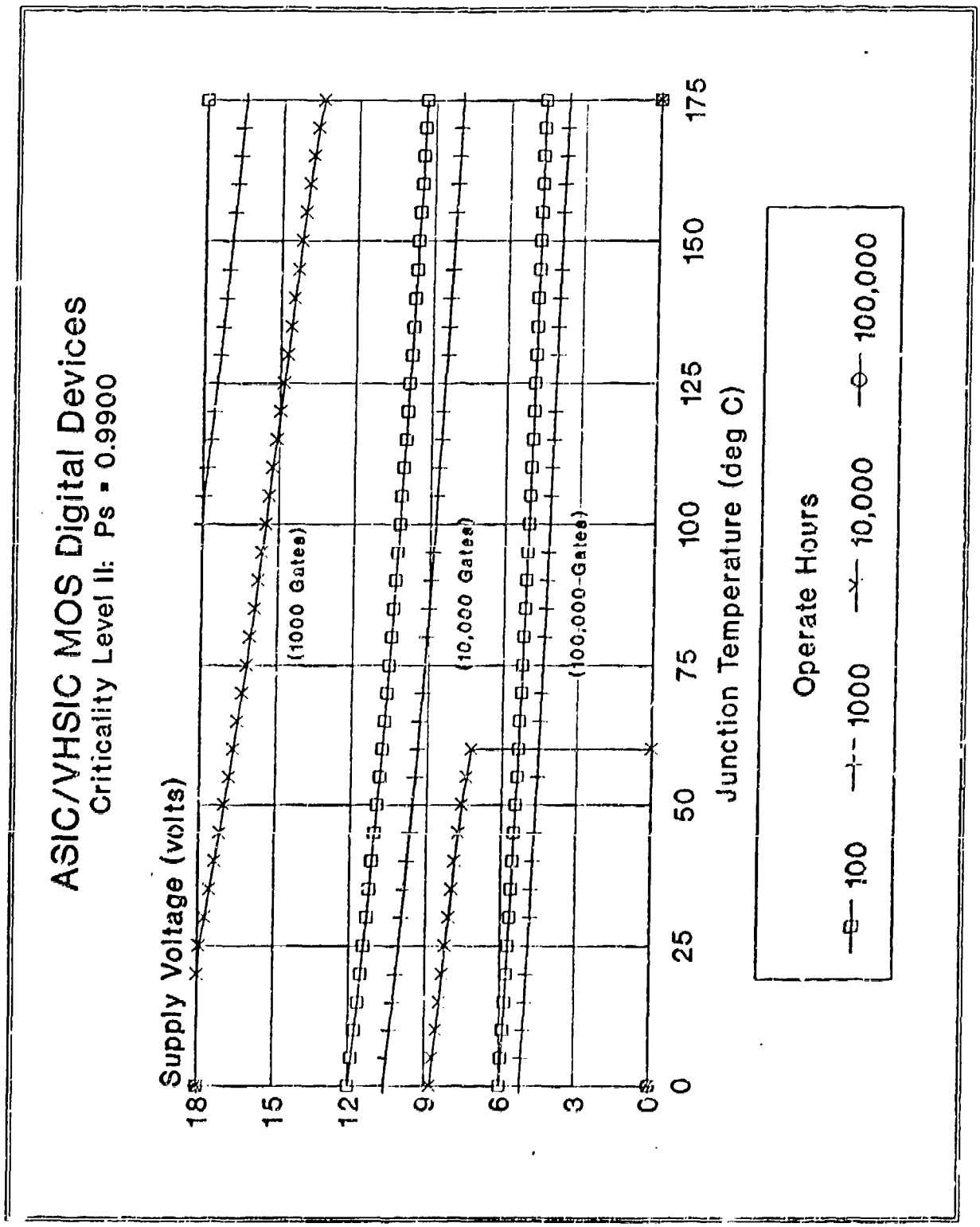
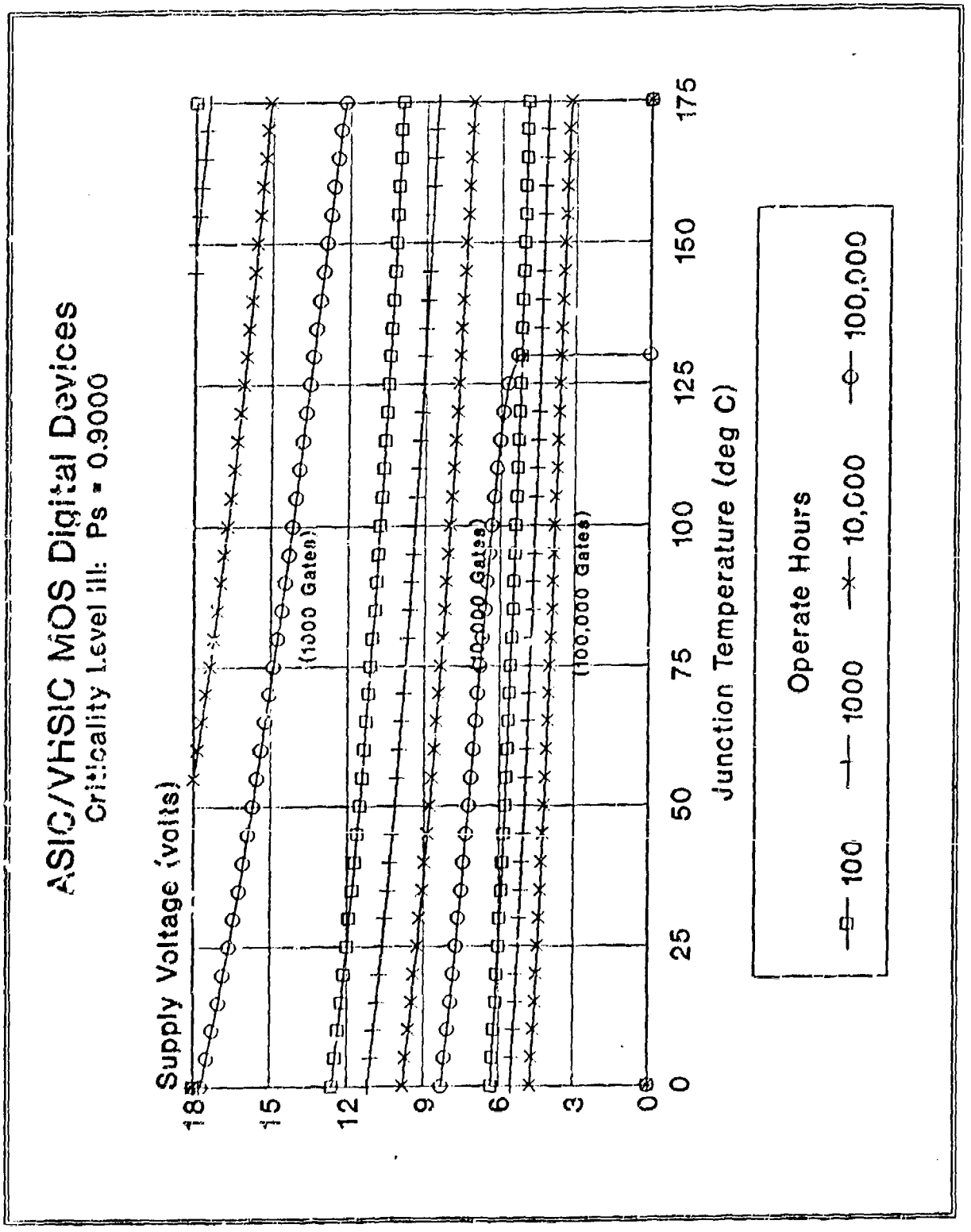


Figure 12-3 P_s = 0.9000 SOAs for MOS Digital ASIC/VHSIC



13.0 SUMMARY

There are multiple methods by which stress derating criteria can be developed. The criteria developed during this study utilized three methods, the use of existing reliability models, the generation of stress-failure relationships based upon accumulated failure data and consensus of stress derating guidelines originating from other military and industrial facilities. Although this latter method utilizes the profound knowledge of others, there may be no accounting for how these criteria were developed, and therefore no insight into how to modify the criteria for changing component technologies and complexities. Even though specific stress-failure relationships may be developed from accumulated failure data, it is not always reasonable to base the development of the stress derating criteria on these relationships since the competing effects of the individual stresses may not being taken into account. The best method (of the three methods used), therefore, is the one in which current reliability models are used to describe the pertinent stress-failure relationships. This method not only allows the insight into the parameters that may be affected by changing component technologies and complexities, but also combines the competing effects of multiple stresses.

Unfortunately, current reliability models were not available for all the component types described in table 1-1, and therefore the other two methods of generating stress derating criteria were used. It is noted, however, that much effort was expended in evaluating and attempting to update the reliability models of the discrete and passive components. The literature searches initially identified over 600 articles of which approximately 240 articles were germane to this study. Of those 240 articles, 160 articles were made available and reviewed. Forty-eight component suppliers of the seventy-two suppliers contacted also provided stress-failure data. Unfortunately most of the data accumulated from these sources could not be used to generate stress derating criteria because key elements of the stress-failure relationships were missing. For example, some sources did not provide the time to failure, while other sources left out stress data,

and still others neglected to provide a reference point along with the temperature activation energy which is needed to describe the failure distribution.

The level of stress derating should be based upon the expected failure rate provided by the reliability model. However, not all the factors that may require derating are currently identified in the reliability model. These factors may include output current or propagation delay times. If changes in these factors result in changes in the observed reliability of the component, then these factors also belong in the reliability model. An evaluation of whether the stress derating parameters identified during this update of the Guidelines should be included in the appropriate reliability model is recommended. In addition, it is recommended that an alternative approach to stress derating, as described in section 12.0, be evaluated to determine the advantages and disadvantages in making the stress derating criteria component or board "mission" critical rather than system mission critical.

14.0 BIBLIOGRAPHY

1. Garry, William, et. al., 'Reliability Analysis/Assessment of Advanced Technologies,' RADC-TR-90-72, 1990
2. Anon, 'Simulation Is The Name Of The Game,' Electron Wireless World
3. Betrano, Frank S., 'Estimating Integrated Circuit Failure Rates From Field Performance,' Proceedings of the Annual Reliability And Maintainability Symposium, 1988
4. Burch, Richard, Najm, Farid, Yang, Ping And Hocevar, Dale, 'Pattern-independent Current Estimation For Reliability Analysis Of CMOS Circuits,' Proceedings of the 25th ACM /IEEE Design Automatic Conference, 1988
5. Chilo, J., And Angenieux, G., 'CAD Formulas For Modeling Of Electrical Interconnections In ICs,' Revue De Physique Applique
6. Conrad, T.R., Mielnik, R.J. and Musolino, L.S., 'Test Methodology To Monitor And Predict Early Life Reliability Failure Mechanisms,' IEEE, 26th Annual Proceedings of the IRPS, 1988
7. Cox, P., Yang, P., Mahant-shetti, S.S. and Chatterjee, P., 'Statistical Modeling For Efficient Parametric Yield Estimation Of MOS VLSI Circuits,' IEEE Journal of Solid State Circuits, 1985
8. Florescu, R.A., 'Comments On "Extension Of The Duane Plotting Technique, By P.S. Peck,"' IEEE Transactions on Reliability, 1986
9. Frost, David F., And Poole, Kelvin F., 'Reliant: A Reliability Analysis Tool For VLSI Interconnects,' IEEE Journal Of Solid State Circuits, Volume 24, April, 1989
10. Hayes, J.P., 'Fault Modeling For Digital MOS Integrated Circuits,' IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 1984
11. Healy, J., 'Modeling IC Failure Rates,' Proceedings Of The Annual Reliability And Maintainability Symposium, 1986
12. Helms, Howard D., 'Various Architectures Of Systems For Measuring Early-life Failure Rates Of Semiconductor Components,' International Testing Conference Proceedings, 1985
13. Hightower, David, Mccusker, Deanna J., And Shinozuka, Kazuya, 'Finding Fault: An Update On Fault Simulation,' VLSI Systems Design, October 1987
14. Holcomb, D.P., North, J.C., 'An Infant Mortality And Long-term Failure Rate Model For Electronic Equipment,' AT&T Technical Journal, 1985
15. Kuo, W., 'Reliability Enhancement Through Optimal Burn-in,' IEEE Transactions on Reliability, 1984
16. Landis, David L., And Muha, Daniel C., 'Evaluation Of System BIST Using Computational Performance Measures,' International Testing Conference Proceedings, 1988
17. Lee, J., Shragowitz, E. and Sahni, S., 'A Hypercube Algorithm For The 0/1 Knapsack Problem,' International Conference On Parallel Processing,
18. Long, D.M., Jaffe, R.C. and Casey, R.H., 'Algorithm For Determining Worst Case Transistor Parameters,' IEEE Transactions on Nuclear Science, 1984
19. McGill, James, 'Predicting Hybrid Microcircuit Reliability: A Primer,' Proceedings Of The 1985 International Symposium On Microelectronics,

20. McLeod, J., 'Simulation: The Last Frontier,' Electronics, 1986
21. Morozowich, Merle, 'A Method To Determine Overload Safe Operating Area,' Conference Proceedings Of The Intelec '85, 7th International Telecommunications
22. Pantic, Dragan, 'Benefits Of Integrated Circuit Burn-in To Obtain High Reliability Parts,' IEEE Transactions On Reliability, 1986
23. Peck, D.S, 'Extension Of The Duane Plotting Technique,' IEEE Transactions on Reliability, 1985
24. Rajsuman, R., Malaiya, Y.K., And Jayasumana, A.P., 'On Accuracy Of Switch-level Modeling Of Bridging Faults In Complex Gates,' Proceedings of the 24th ACM/IEEE Design Automation Conference, 1987
25. Razdan, R. and Strojwas, A.J., 'Statistical Design Rule Developer,' IEEE Transactions On CAD Of Integrated Circuits & Systems, 1986
26. Spencer, J.L., 'Highs And Lows Of Reliability Predictions,' Proceedings of the Annual Reliability And Maintainability Symposium, 1986
27. Tomaine, J.J., 'Predicting Reliability Of ISI Printed Circuit Carriers,' Circuit World, 1986
28. Yacoub, G.Y, Pham, H., Ma, M. and Friedman, E.G., 'System For Critical Path Analysis Based On Back Annotation And Distributed Interconnect Impedance Models,' Microelectron Journal,
29. Seeq Technology, Inc., San Jose, CA, 'Calculation Of EEPROM Board MTBF,' Memory Products Reliability Notes - 1, November 1987
30. Seeq Technology, Inc., San Jose, CA, 'I.C. Scale Definition,'
31. Intel Corp., Santa Clara, CA, 'The Intel Reliability Monitor Program,'
32. Intel Corp., Santa Clara, CA, 'Intel Reliability Monitor Program Data From 1/80 Through 1/87,', March 1987
33. Monolithic Memories, Santa Clara, CA, 'Reliability Report,', November 1983
34. Adams, J.H., 'Radiation Effects In Microelectronics For Space Instruments,' 29th Nuclear Science Symposium and 14th Symposium On Nuclear Power, 1983
35. Andrews, John, 'Detecting CMOS Stuck-open Transistors,' VLSI Systems Design, October 1987
36. Archer, et al, 'A 32b CMOS Microprocessor With On-chip Instruction And ATA Caching And Memory Management,' 1987 IEEE International Solid State Circuits Conference, 1987
37. Banarjee, Biswa, 'Handling The Power Dissipation Of ECL Gate Arrays,' VLSI Systems Design, January 1987
38. Baze, M.P. and Johnston, A.H., 'Testing Considerations For Radiation Induced Latchup,' IEEE Transactions On Nuclear Science, 1987
39. Blott, B.G., 'Gamma-ray Effects On An N-channel MOS Microprocessor (Z8002) In The Zero-bias Condition,' IEEE Transactions on Nuclear Science, October 1983
40. Browning, J.S., Koga, R. and Kolasinski, W.A., 'Single Event Upset Rate Estimates For A 16-k CMOS SRAM,' IEEE Transaction on Nuclear Science, 1985
41. Canali, C., Fantini, F., Soncini, G., Venturi, P. and Zanoni, E., 'Failure Modes Induced In TTL-LS Bipolar Logics By Negative Inputs,' Alta Frequenza, 1982

42. Canali, C., Fantini, F., Gaviraghi, S. and Senin, A., 'Reliability Problems In TTL-LS Devices,' Microelectronics And Reliability, 1981
43. Chao, H.H., Ong, S., Tsai, M.Y., Shih, F.W., Hou, J.C., Lewis and K.W., 'Micro/370: A 32 Bit Single-chip Microprocessor,' IEEE Journal of Solid State Circuits, 1986
44. Chappell, Chappell, Shuster, Segmuller, Allan, Franch and Restl, 'Fast CMOS ECL Receivers With 100-mv Worst-Case Sensitivity,' IEEE Journal Of Solid State Circuits, Volume 23, 1988
45. Clatterbauhe, G.V., Weiner, J.A. and Charles, H.K. Jr., 'Gold-Aluminum Intermetallics: Ball Bond Shear Testing And Thin Film Reaction Couples,' IEEE Transactions on Components and Hybrids Manufacturing Technology, 1984
46. Davies, M.S., Miles, R.E. and Postoyalko, V., 'Two-step Methodology For CMOS VLSI Reliability Improvement: Step One,' Quality and Reliability Engineering International,
47. Denton, Donald L. And Blythe, Donald M., 'The Impact Of Burn-in On IC Reliability,' Journal On Environmental Science, Jan/Feb 1986
48. Doyle, E.A., 'How Parts Fail,' IEEE Spectrum, 1981
49. Dugan, M.P., 'Reliability Characterization Of A 3-8 Micron CMOS/SOS Process,' RCA Review, 1986
50. Edwards, D.G., 'Testing For MOS IC Failure Modes,' IEEE Transactions On Reliability, 1982
51. Enlow, E.W. and Wunsch, D.C., 'Semiconductor Failure Threshold Estimation Problem In Electromagnetic Assessment,' IEEE Transactions on Nuclear Science, Dec 1984
52. Fantini, F. and Marandi, C., 'Failure Modes And Mechanisms For VLSI ICs - A Review,' IEEE Proceedings, Part G, 1985
53. Ferris-Prabhu, Albert V., 'Yield Implications And Scaling Laws For Submicrometer Devices,' IEEE Transactions On Semiconductor Manufacturing, May 1988
54. Filanovsky, Igor M. And Finvers, Ivars G., 'A Simple Nonsaturated CMOS Multivibrator,' IEEE Journal Of Solid State Circuits, Volume 23, 1988
55. Furukawa, M., Hatano, H., and Hanihara, K., 'Precision Measurement Technique Of Integrated MOS Capacitor Mismatching Using A Simple On-chip Circuit,' IEEE Transactions on Electron Devices, 1986
56. Heath, M., Stefanakos, E., Wade, T., Miller, W. and Nicolay, H., 'VLSI Multilevel Metal Defect Characterization System,' Conference Proceedings-IEEE Southeastcon, 1987
57. High Performance Systems, 'Producing Complex ASICs on Tight Schedules,' Semiconductor Design Guide, 1989
58. Hinds, D.J., Stokoe and J.C., 'Optically Induced Latch-up And Other Effects In CMOS UVEPROMs,' Electron Letters, 1985
59. Hinode, K., Owada, N., Nishida, T. And Mukai, K., 'Stress-Induced Grain Boundary Fractures In Al-Si Interconnects,' Journal Of Vacuum Science And Technology, B., 1987
60. Hull, Randy And Jackson, Rick, 'Analysis Of High Voltage ESD Pulse Testing On CMOS Gate Array Technology,' Electrical Overstress And Electrostatic Discharge Symposium Proceedings, 1987
61. Johnston, A.H., 'Models For Total Dose Degradation Of Linear Integrated Circuits,' IEEE Transactions on Nuclear Science, Dec 1987

62. Kacprzak, Tomasz, 'Analysis Of Oscillatory Metastable Operation Of An RS Flip-Flop,' IEEE Journal Of Solid State Circuits, Volume 23, 1988
63. Kacprzak, Tomasz, Albicki, Alexander And Jackson, Todd A., 'Design Of N-well CMOS Flip-Flops With Minimum Failure Rate Due To Metastability,' IEEE International Symposium On Circuits And Systems, 1986
64. Keating, Mike And Meyer, Dennis, 'A New Approach To Dynamic IDD Testing,' International Testing Conference Proceedings, 1987
65. Kemp, K.G. and Poole, K.F., 'Study Of Electromigration In Double Level Metal Systems Using Oxide And Polymer Dielectrics,' Conference Proceedings-iEEE Southeastcon, 1987
66. Kjar, R.A., Lee, S.N., Pancholy, R.K. and Peel, J.L., 'Self-Aligned Radiation And Hard CMOS/SOS,' IEEE Transactions on Nuclear Science, Dec 1976
67. Koga, R. and Kolasinski, W.A., 'Effects Of Heavy Ions On Microcircuits In Space: Recently Investigated Upset Mechanisms,' IEEE Transactions on Nuclear Science, Feb 1987
68. Kumar, M., Fissel, M.G., Pourrezaei, K., Lee, K. And Dougla, 'Growth And Properties Of Tin And Tioxny Diffusion Barriers In Silicon On Sapphire Integrated Circuits,' Thin Solid Films, 1987
69. Lee, Chen, Holland, Fong And Hu, 'Oxide Defect Density, Failure Rate And Screen Yield,' 1986 Symposium On VLSI Technology
70. Lee, J.C., Chen, In-chin and Hu, Chenming, 'Modeling And Characterization Of Gate Oxide Reliability,' IEEE Transactions on Electron Devices
71. Mangir, T.E., 'Sources Of Failures And Yield Improvement For VLSI And Restructurable Interconnects For RVLSI And WSI,' Proceedings of the IEEE, 1984
72. Mckirdy, Ray and Lea, Mike, 'WSI: A Technology For Reliability,' Yield Modeling And Defect Tolerance In VLSI
73. Meredith, John W., 'Microelectronics Reliability,' IEEE Region 5 Conference, 1988
74. Miller, Jeffrey, Hecht, Herbert, And Morris, Seymour, 'Accounting For Soft Errors In Memory Reliability Prediction,' Annual Reliability And Maintainability Symposium, 1989
75. Myers, D.K., 'Ionizing Radiation Effects On Various Commercial NMOS Microprocessors,' IEEE Transactions on Nuclear Science, Dec 1977
76. Olivo, Piero, Nguyen, Thao N., And Ricco, Bruno, 'High-field-induced Degradation In Ultra-thin Sio2 Films,' IEEE Transactions On Electron Devices, 1988
77. Olsen, D.R., and James, K.L., 'Effects Of Ambient Atmosphere On Aluminum-copper Wirebond Reliability,' IEEE Transactions on Components and Hybrids Manufacturing Technology, 1984
78. Padmanabhan, R., 'Corrosion Failure Modes In A Tab200 Test Vehicle,' IEEE Transactions on Components and Hybrids Manufacturing Technology, 1986
79. Pantic, D.M., 'Maturity Factors In Predicting Failure Rate For Linear Integrated Circuits,' IEEE Transactions on Reliability, 1984
80. Patterson, J.M., And David, R.F., 'An Investigation Of The Effect Of Electric Field Equivalency (EFE) Dice Screening On Hybrid Yield,' International Symposium For Testing And Failure Analysis

81. Pease, R.L., Turfler, R.M., Platteter, D., Emily, D. and Slice, R, 'Total Dose Effects In Recessed Oxide Digital Bipolar Microcircuits,' IEEE Transactions on Nuclear Science, 1983
82. Pecht, M., Palmer, M., Schenke, W. and Porter, R., 'Investigation Into PWB Component-Placement Trade-offs,' IEEE Transactions on Reliability
83. Pesic, B., Dimitrijev, S. and Stojadinovic, N., 'Sudden Failures Associated With The Gate Oxide Of CMOS Transistors,' Microelectronics Reliability
84. Radojcic, R., 'Generic Qualification Of Semi-custom IC Product Families,' Microelectronics And Reliability, 1986
85. Schroeder, J.E., Gingerich, B.L. and Bechtel, G.R., 'Total Dose and Dose Rate Radiation Characterization of a Hardened EPI-CMOS Gate Array,' IEEE Transactions on Nuclear Science, 1984
86. Shirley, C.G. and Blish, R.C., 'Thin-film Cracking and Wire Ball Shear In plastic Dips Due to Temperature Cycle and Thermal Shock,' Proceedings of the 25th Annual IRPS, 1987
87. Simonaitis, D.F., 'IC Failure Rate Estimates from Field Data,' IEEE Transactions on Components and Hybrid Manufacturing Technology, 1983
88. Smith, William, Jr. and Khory, Noshir, 'Does the Burn-in of Integrated Circuits Continue to be a Meaningful Course to Pursue,' Proceedings of the 38th Electronics Components Conference, 1988
89. Soucair, F.S., 'High-temperature Latchup Characteristics In VLSI CMOS Circuits,' IEEE Transactions On Electron Devices, 1988
90. Stroehle, D., 'Influence Of The Chip Temperature On The Moisture-induced Failure Rate Of Plastic-encapsulated Devices,' IEEE Transactions on Components and Hybrids Manufacturing Technology, 1983
91. Sweetman, Dave, And Haifley, Tim, 'Reliability Enhancements - Million Cycle EEPROMs,' Annual Reliability And Maintainability Symposium, 1987
92. Towner, J.M., 'Electromigration Testing Of Thin Films At The Wafer Level,' Solid State Technology, 1984
93. Veloric, H., Dugan, M.P., Morris, W., Denning, R. and Schnable, G., 'Reliability Of CMOS/SOS Integrated Circuits,' RCA Review, 1984
94. Winokur, P.S., Sexton, F.W. Hash, G.L. and Turpin, D.C., 'Total-dose Failure Mechanisms Of Integrated Circuits In Laboratory And Space Environments,' IEEE Transactions on Nuclear Science, Dec 1987
95. Winokur, Sexton, Schwank, Fleetwood, Dressendorfer and Wrobel, 'Total-dose Radiation And Annealing Studies: Implications For Hardness Assurance Testing ,' IEEE Transactions Of Nuclear Science, 1986
96. Wittlinger, Hal, And Salerno, Carmine, 'New BiMOS Process Improves Analog Applications: Fast, Low-power Quad Op Amp Benefits From Enhancements To High-speed CMOS,' Technological Horizons
97. Wong, K.L., Quart, I., Kallis, J.M., and Burkhard, A.H., 'Culprits Causing Avionic Equipment Failures,' Proceedings of the Annual Reliability And Maintainability Symposium, 1987
98. Woodhall, Barnes W., Newman, B. Dale, And Sammuli, Avrid G., 'Empirical Results On Undetected CMOS Stuck-open Failures,' Proceedings of the International Testing Conference, 1987
99. Yue, H., Davison, D., Jennings, R.F., Lothongkam, P. and Rinerson, D., 'Radiation Response Of High Speed CMOS Integrated Circuits,' IEEE Transactions On Nuclear Science, 1987

100. Zietlow, T.C., Morse, T.C., Urquhart, K.C., Wilson, K.T. and Aukerman, L., 'Correlation Of Total Dose Damage In Capacitors And Transistors To 1.25 Micron Integrated Circuits,' IEEE Transactions on Nuclear Science, Dec 1987
101. Bellem, R.D. and Jenkins, W.C., 'Radiation Effects On GaAs Charge Coupled Devices With High Resistivity Gate Structures,' IEEE Transactions On Nuclear Science, 1986
102. Bill Roesch, 'GaAs Failure Mechanisms,' Tri-quint
103. Christou, A. And Anand, Y., 'GaAs Mixer Diode Burnout Mechanisms At 36-94 GHz,' IEEE, 1980
104. Christou, Tseng, Peckerar, Anderson, McCarthy, Buot, and Campbel, 'Failure Mechanism Study Of GaAs MODFET Devices And Integrated Circuits,' IEEE, 1985
105. Fourrier, J.Y. and Pestie, J.P., 'Very High Reliability Fast Bipolar IC Technology For Use In Undersea Optical Fiber Links,' Journal of Lightwave Technology, 1984
106. Fraser, Arthur, And Ogbonnah, Dominic, 'Reliability Investigation Of GaAs IC Components,' GaAs IC Symposium, Nov 11-14, 1985
107. Gagnon, Michael P., 'Analog GaAs ICs Show Steady Improvement,' Electronic Products, June 15, 1988
108. Ho, Pang, Andrade, Tom, And Johnson, Ed, 'GaAs MMIC Reliability Analysis And Its Impact On Microwave Systems, Part I,' MSM & CT, Aug/Sept 1987
109. Larson, Lawrence E., 'High-speed Analog-to-digital Conversion With GaAs Technology: Prospects, Trends, And Obstacles,' IEEE International Symposium On Circuits And Systems, 1988
110. Michael Chester, 'At The Forefront,' Electronic Products, October 15, 1987
111. Peters, Michael, Roesch, William J., And Rubalcava, Anthony, 'Studying Lifetimes And Failure Rates Of GaAs MMICs,' Microelectronics And Radiofrequency, July, 1988
112. Roche, J., Sasonoff, J., And Wallace, R., 'Reliable MMICs: Status And Prospects,' Raytheon Presentation, October 21, 1988
113. Roesch, William J., 'Thermo-reliability Relationships Of GaAs ICs,' Gallium Arsenide IC Symposium, November, 1988
114. Roesch, William J., And Stunkard, Douglas, 'Proving GaAs Reliability With IC Element Testing,' Triquint Semiconductor, 1986
115. Schappacher, Jerry, 'The Blossoming Of Digital GaAs ICs,' Electronic Products, June 15, 1988
116. Snodgrass, M.L. and Klirman, R., 'High Reliability High Sensitivity Lightwave Receiver For The S1 Undersea Lightwave System,' Journal of Lightwave Technology, 1984
117. Spadaro, Joseph J., Associate Editor, 'The Future Is Now For GaAs ICs,' Electronic Products, June 15, 1988
118. Spector, M. and Dodson, G.A., 'Reliability Evaluation Of GaAs IC Pre-amplifier HIC,' Technical Digest, 1987
119. Tomasetta, Louis R., 'Processing Advances Push GaAs ICs To Higher VLSI Levels,' EDN, June 9, 1988
120. Topham, P.J., Hayes, R.C., Goodridge, I.H., Tombling, C. and Benn, D., 'Heterojunction Bipolar Digital ICs Using MOCVD Material,' IEEE Gallium Arsenide Integrated Circuit Symposium, 1986

121. Wilhems n, Finn, Yee, Russell, Zee, Terry And Oskrink, Nort, 'Temperature s. Reliability In Power GaAs FETs And MIC GaAs FET Power Amplifiers,' Microwave Journal, May 1984
122. Wirfl, J., And Hartnagel H.L., 'Field And Temperature Dependent Life-time Limiting Effects Of Metal-GaAs Interfaces Of Device Structures Studied By XPS And E,' IEEE, 1986
123. Blackburn, D.L., 'Power MOSFET Failure Revisited,' 19th Annual IEEE Power Electronics Specialists Conference, 19th, Japan, 1988
124. Blackburn, D.L. Berning, D.W., Benedetto, J.M. and Galloway, K.F., 'Ionizing Radiation Effects On Power MOSFETs During High Speed Switching,' 19th Annual Conference On Nuclear And Space Radiation Effects, Las Vegas, 1982
125. Canali, C. Fancini, F., Umena, L. and Zanoni, E., 'Degradation Mechanisms Induced By Temperature In Power MESFETs,' Electronics Letters, 1985
126. Canali, Castaldo, Fantini, Ogliari, Umena, And Zanoni, 'Gate Metallization "Sinking" Into The Active Channel In Ti/W/Au Metallized Power MESFETs,' IEEE Electron Devices Letters, 1986
127. Carpenter, Grant, Lee, Fred, C., And Chen, Dan Y., 'A 1800V, 300A Non-destructive RBSOA Tester For Bipolar Transistors,' 19th Annual IEEE Power Electronics Specialists Conference, April 1988
128. Chung, H.R. Baliga, B.J. Kretchmer, J.W. and Piacente, P.A., 'Insulated Gate Bipolar Transistor (IGBT) With A Trench Gate Structure,' Technical Digest, 1987
129. Chang, M., Yilmaz, H., Gauffreau, G., Hshien, I. and Hodgins, R., 'Advanced 50-V High-side Switch Technology,' IEEE Transactions on Electron Devices
130. Dumas, J.M., Kervarrec, G., Bresse, J.F. Boulaire, J.Y. and Gauneau, M., 'Investigation On Interelectrode Metallic 'paths' Affecting The Operation Of IC MESFETs,' Technical Digest, 1987
131. Ferla, Musumeci, Busatto, Spirito, And Vitale, 'Switching Characteristic Of A High Voltage BMFET,' Extended Abstracts Of The 18th Conference On Solid State Devices And Materials, 1986
132. Fischer, T.A., 'Heavy-ion-induced, Gate-rupture In Power MOSFETs,' IEEE Transactions on Nuclear Science, Dec 1987
133. Fukui, H., Wemple, S.H., Irvin, J.C., Hwang, J.C. and Cox, H.M., 'Reliability Of Power GaAs Field-effect Transistors,' IEEE Transactions On Electron Devices, 1982
134. Fukui, Wemple, Irvin, Niehau, Hwang, Cox, Schlosser, And Dil, 'Reliability Of Improved Power GaAs Field-effect Transistors,' IEEE, 18th Proceedings Of The IRPS, 1980
135. Gauen, Kim, And Schultz, Warren, 'Proper Testing Can Maximize Performance In MOSFETs,' EDN, May 14, 1987
136. Hayat, S.A. and Jones, B.K., 'Low Process Yield Of Some PNP Power Transistors,' Microelectronics Reliability
137. Hu, C. and Chi, M., 'Second Breakdown Of Vertical Power MOSFETs,' IEEE Transactions On Electron Devices, 1982
138. Jordar, A.S., Irvin, J.C., And Schlosser, W.O., 'A Large Scale Reliability Study Of Burnout Failure In GaAs Power FETs,' IEEE, 1980

139. Jovanovic, Milan M., And Lee, Fred C., 'Design Considerations For Paralleling Bipolar Transistors,' IEEE Transactions For Power Electronics, 1987
140. Kanamori, S., and Matsumoto, T., 'High-reliability Microwave Silicon Power Transistor With Stepped Electrode Structure And Tin Diffusion Barrier,' IEEE Transactions On Electron Devices, 1986
141. Kashiwagi, S., Takase, S., Usui, T. And Ohono, T., 'Reliability Of High Frequency High Power GaAs MESFETs,' IEEE, 25nd Annual Proceedings Of The IRPS, 1987
142. Katsukawa, K., Kose, Y., Kanamori, M. And Sando, S., 'Reliability Of Gate Metallization In Power GaAs MESFETs,' IEEE, 22nd Annual Proceedings Of The IRPS, 1984
143. Korman, C.S., Love, R.P., Temple, V.A.K., And Walden, J.P., 'A Low On-resistance MOSFET For High Efficiency Switching Power Supplies,' 2nd International Conference On Power Electronics And Variable-speed Drives
144. Koyanagi, Lewis, Martin, Huang, And Chen, 'Increased Degradation Of Half-micron PMOSFETs Due To Swapped Pulse Stressing,' International Electron Devices Meeting (IEDM), 1987
145. Millea, Michael F., 'Gradual Degradation Of GaAs FETs Under Normal Operation,' 24th Annual Proceedings of the IRPS, 1987
146. Morgan, A.N., 'Improved Power Transistor Performance By Hollow Emitter Construction - Switching Power Supply Applications,' 2nd International Conference On Power Electronics And Variable-speed Drives
147. Nakagawa, Akio, 'Numerical Experiment For 2500V Double Gate Bipolar-mode MOSFETs (DGIGBT) And Analysis For Large Safe Operating Area (SOA),' Pesc 1988 Record, 19th Annual IEEE Power Electronics Specialists Conference, April 1988
148. Nakagawa, Akio, Yamaguchi, Yoshihiro, And Kiminori, Watanabe, 'Improved Bipolar-mode MOSFETs (IGBT) With Self-aligning Technique And Wafer Bonding (SDB) - Why Is The Bipolar-mode MOSFET SOA,' Extended Abstracts Of The 19th Conference
149. Nakagawa, Yamaguchi, Watanabe, And Ohashi, 'Safe Operating Area For 1200-V Nonlatchup Bipolar-mode MOSFETs,' IEEE Transactions On Electron Devices, 1987
150. Nakatani, Y, 'Ultra-high-voltage High-speed Switching Power Transistor With New Fine Emitter Structure,' Electron Commun Jpn, 1983
151. Ogbonmah, Dominic, And Fraser, Arthur, 'Reliability Investigation Of 1 Micron Depletion Mode IC MESFETs,' 24th Annual Proceedings of the IRPS, 1986
152. Omori, Masa, And Wholey, James N., Gibbons, James F., 'Accelerated Active Life Test Of GaAs FET And A New Failure Mode,' IEEE, 1980
153. Poole, Walter, And Walshak, Louis, 'Five-year Quest To Prove Power Transistor Reliability,' Microwaves & Rf, July 1984
154. Russell, K.J, And Dhiman, J.K., 'Power GaAs FET Rf Life Test Using Temperature-compensated Electrical Stressing,' IEEE, 24th Annual Proceedings Of The IRPS, 1986
155. Schlangenotto, H. And Neubrand, H., 'Dynamical Avalanche During Turn-off Of GTO-thyristors And IGBTs,' Archiv Fir Electrotechnik, 1989

156. Schmid, Horst, 'Switching Losses Of The New Siret - A Comparison To Other Medium-power Devices,' Conference Record Of The 1988 IEEE Industry Applications Society Annual Meeting, 1988
157. Wada, Y., 'Electromigration Properties Of Titanium/Aluminum Metallization And A Failure Mechanism For Titanium/Aluminum Gate GaAs MESFET,' Journal of the Electrochemical Society, 1986
158. White, P.M., Rogers, C.G. and Hewitt, B.S., 'Reliability of Ku-Band GaAs Power FETs Under Highly Stressed RF Operation, IEEE, 21st Annual Proceedings of the IRPS, 1983
159. Yilmaz, Benjamin, Owyang, Chang, And Van Dell, 'Recent Advances In Insulated Gate Bipolar Transistor (IGBT) Technology,' Conference Record Of The 1986 IEEE Industry Applications Society Annual Meeting, 1986
160. Anderson, W.T., Christou, A. And Wilkins, B.R., 'GaAs FET High Power Pulse Reliability,' IEEE, 21st Annual Proceeding Of The IRPS, 1983
161. Anderson, W.T., Buot, F.A., And Christou, A., 'High Power Pulse Reliability Of GaAs Power FETs,' IEEE, 1986
162. James, D.S. and Dormer, L., 'A Study Of High Power Pulsed Characteristics Of Low-noise GaAs MESFETs,' IEEE Transactions On Microwave Theory And Techniques, 1981
163. Yoshida, Y., Mohri, K., Yoshino, K. and Nakano, M., 'Switching Characteristics And Applications Of Amorphous Ct Core Pulse Triggered Power Transistors (PTPT),' IEEE Translation Journal On Magnetics In Japan, 1985
164. Dixon, R.W., 'Current Directions in GaAs Laser Device Development,' The Bell System Technical Journal, May-June 1980
165. Spectra Diodes Labs, '100mW CW GaAlAs Laser Diode,' Data Sheet, 1989
166. Munikoti, Ramchandra, And Dhar, Pulak, 'Highly Accelerated Life Testing (HALT) For Multilayer Ceramic Capacitor Qualification,' IEEE Transactions On Components, Hybrids, And Manufacturing Technology, 1988
167. Rawal, B.S. Ladew, R. and Garcia, R., 'Factors Responsible For Thermal Shock Behavior Of Chip Capacitors,' Proceedings of the 37th Electronic Components Conference, 1987
168. Vale, C.R., 'Long Term Stability of SAW Decoders,' IEEE Ultrasonics Symposium, 1986
169. Colt, D.W. and Priore, M.G., 'Reliability Prediction Models For Discrete Semiconductor Devices,' RADC-TR-88-97, July 1988

Appendix A

ASIC/VHSIC Derating Criteria

Classification	Derating Parameter	Level I	Level II	Level III
MOS Digital Figure 4-9 page 44	(1) Supply Voltage (volts) Frequency (POMS) Output Current, Fan Out, (PORV) (2) Maximum Junction Temp. (deg C) Circuit Complexity - Maximum Gates	129 / (G ** 0.320) 80 70 (80) 80 60,000	173 / (G ** 0.347) 80 75 (80) 121 60,000	157 / (G ** 0.323) 80 80 (90) 125 60,000
MOS Linear Figure 4-11 page 46	(1) Supply Voltage (volts) Input Voltage (PORV) Frequency (POMS) Output Current, Fan Out, (PORV) (2) Maximum Junction Temp. (deg C) Circuit Complexity - Maximum Trans.	200 / (TR ** 0.315) 60 80 70 (80) 53 10,000	189 / (TR ** 0.311) 70 80 75 (80) 109 10,000	210 / (TR ** 0.347) 70 80 80 (90) 125 60,000
Bipolar Digital Figure 4-13 page 48	(1) Supply Voltage (volts) Frequency (POMS) Output Current, Fan Out, (PORV) (2) Maximum Junction Temp. (deg C) Circuit Complexity - Maximum Gates	+/- 3% 75 70 (70) 72 60,000	+/- 5% 80 75 (75) 85 26,000	+/- 5% 90 80 (80) 125 60,000
Bipolar Linear Figure 4-11 page 46	(1) Supply Voltage (volts) Input Voltage (PORV) Frequency (POMS) Output Current, Fan Out, (PORV) (2) Maximum Junction Temp. (deg C) Circuit Complexity - Maximum Trans.	+/- 3% 60 75 70 (70) 83 10,000	+/- 5% 70 80 75 (75) 109 10,000	+/- 5% 70 90 80 (80) 125 10,000

KEY: G = Number of Gates
LG = Log (base 10) of TR
TR = Number of Transistors
PORV = Percent of Rated Value
* = Multiplied By
LTR = Log (base 10) of TR
POMS = Percent of Maximum Specified
** = Taken to the Power of
(1) Not to exceed supplier minimum or maximum rating
(2) Not to exceed 125 deg C or supplier maximum
(whichever is the smaller of the two)

Microprocessor Stress Derating Criteria

Classification	Derating Parameter	Level I	Level II	Level III
MOS	Supply Voltage (volts), 8-Bit (1)	10	11	13
	Supply Voltage (volts), 16 Bit (1)	606 / (G ** 0.440)	760 / (G ** 0.462)	698 / (G ** 0.438)
	Supply Voltage (volts), 32-Bit (1)	642 / (G ** 0.442)	627 / (G ** 0.448)	696 / (G ** 0.438)
	Frequency (POMS)	80	80	80
	Output Current, Fan Out, (PORV)	70 (80)	75 (80)	80 (90)
	Max. Junc. Temp. (deg C), 8-Bit	120	125	125
	Max. Junct. Temp. (deg C), 16-Bit (2)	90	125	125
	Max. Junct. Temp. (deg C), 32-Bit (2)	60	101	125
	Circuit Complexity - Maximum Gates	N/A	N/A	N/A
Bipolar	Supply Voltage	+/- 3%	+/- 5%	+/- 5%
	Frequency (POMS)	75	80	90
	Output Current, Fan Out, (PORV)	70 (70)	75 (75)	80 (80)
	Max. Junc. Temp. (deg C), 8-Bit (2)	80	85	125
	Max. Junct. Temp. (deg C), 16-Bit (2)	70	70	125
	Max. Junct. Temp. (deg C), 32-Bit (2)	55	56	120
	Circuit Complexity - Maximum Gates	N/A	26,000	N/A

KEY:
G = Number of Gates
LG = Log (base 10) of Gates
N/A = Not Applicable
POMS = Percent of Maximum Specified
PORV = Percent of rated value
* = Multiplied by
** = Taken to the Power of

Notes: (1) Not to exceed supplier minimum or maximum rating
(2) Not to exceed 125 deg C or supplier maximum, which ever is smaller

PROM Stress Derating Criteria

Classification	Derating Parameter		Level I	Level II	Level III
MOS	Supply Voltage * (volts)	(1)	65.2 / (B ** 0.183)	85.3 / (B ** 0.199)	85.3 / (B ** 0.178)
	Supply Voltage (volts)	(1)	66.0 / (B ** 0.178)	71.1 / (B ** 0.176)	83.3 / (B ** 0.175)
	Frequency (POMS)		80	80	90
	Output Current (PORV)		70	75	80
	Maximum Junction Temp. (deg C)	(2)	125	125	125
	Maximum Write Cycles	(3)	1.26E8 / (B ** 0.660)	6.94E7 / (B ** 0.470)	300,000
	Circuit Complexity - Maximum Bits		1 Mbit	1 Mbit	1 Mbit
Bipolar	Fixed Supply Voltage		+/- 3%	+/- 5%	+/- 5%
	Frequency (POMS)		80	90	95
	Output Current (PORV)		70	75	80
	Maximum Junction Temp. (deg C)	(2)	125	125	125
	Circuit Complexity - Maximum Bits		1 Mbit	1 Mbit	1 Mbit

KEY: B - Number of Bits
LB - Log (base 10) of B
* - Applicable to EEPROMs Only
POMS - Percent of Maximum Specified
PORV - Percent of Rated Voltage
/ - Divided By
** - Taken To The Power Of

Notes: (1) Not to exceed supplier minimum or maximum rating.
(2) Not to exceed 125 deg C or supplier maximum, which ever is smaller.
(3) Applicable to EEPROMs Only. Not to exceed supplier maximum.

MICROCIRCUIT APPLICATION NOTES:

1. (Digital) Advanced technology microcircuits are sensitive to ESD
2. (Digital) Unused inputs should be connected to a supply voltage or ground.
3. (Digital) Supply filtering is required to filter out transients.
4. (Digital) Design margins should be used for input leakage (+100%), fanout (-20%) and frequency (-10%).
5. (Digital) Good engineering judgement should be used to derate other microcircuit characteristics, including hold and propagation delay time to produce a conservative design.
6. (Digital, MOS) Input destruction may occur by shorting leads during assembly.
7. (Digital, MOS) High speed transients may result in parasitic bipolar latch-up.
8. (Digital, Bipolar) Supply voltage deviations from the specified nominal will shift internal bias points which, when coupled with thermal effects can cause erratic performance.
9. (Digital & Linear) Heat sinks may be required to maintain derated junction temperature.
10. (Digital & Linear) Circuit design must avoid application of reverse voltage on device leads.
11. (Digital & Linear) Do not exceed the current density derating described by the equation:

    Current Density = 366 / (Temperature in deg. C ** 1.67)

    or 5E5 A/sq-cm, whichever is smaller for aluminum-based metallized microcircuits for either internal circuit operation or output driver operation.
12. (Linear) Each linear device is unique and the designer should have a thorough knowledge of its application requirements to assure that the device is operated within its performance envelope at all times.
13. (Linear) Design margins should be used for gain (-20%) and offset voltages and currents (+50%).

MIMIC Stress Derating Criteria

Classification	Derating Parameter	Level I	Level II	Level III
GaAs	Maximum Channel Temp. (deg C) (1)			
	For: AE <= 100; PE <= 10	95	130	150
	AE > 100; PE <= 10	95	130	150
	AE <= 100; PE > 10	90	130	150
	AE > 100; PE > 10	90	125	150

KEY: AE - Active Elements
PE - Passive Elements

Notes: (1) Not to exceed supplier maximum.

MIMIC APPLICATION NOTES:

1. The environment of the internal package cavity of the MIMIC must be kept inert.
2. Precautions must be observed during electrical test to prevent potential latent failure due to overstress.

Power Transistor Stress Derating Criteria

Classification	Derating Parameter	Level I	Level II	Level III
Silicon Bipolar	Maximum Junction Temp. (deg C)	95	125	135
	Power Dissipation (PORV)	50	60	70
	Safe Operating Area (PORV)	70 Vce 60 Ic	75 Vce 65 Ic	80 Vce 70 Ic
	Breakdown Voltage (PORV)	65	85	90
GaAs MESFET	Maximum Channel Temp. (deg C)	85	100	125
	Power Dissipation (PORV)	50	60	70
	Breakdown Voltage (PORV)	60	70	70
Silicon MOSFET	Maximum Junction Temp. (deg C)	95	120	140
	Power Dissipation (PORV)	50	65	75
	Breakdown Voltage (PORV)	60	70	75

KEY: PORV - Percent of Rated Value

POWER TRANSISTOR APPLICATION NOTES:

1. Power transistors may be sensitive to ESD.
2. Design margins should be used for gain (+/-10% for screened devices; +/-20% for unscreened devices), leakage current (+100%), switching times (+20%) and saturation voltage (+/-15%).
3. Heat sinks may be required to maintain derated junciton/channel temperatures.
4. SOA curves, adjusted for junction temperature, should not be exceeded under any transient conditions.
5. The number of on-off cycles (temperature cycles) should be limited according to the derated power as shown in figure A-1.

RF Pulse Transistor Stress Derating Criteria

Classification	Derating Parameter	Level I	Level II	Level III
Silicon Bipolar	Maximum Junction Temp. (deg C)	95	125	135
	Power Dissipation (PORV)	50	60	70
	Safe Operating Area (PORV)	70 Vce	70 Vce	70 Vce
		60 Ic	60 Ic	60 Ic
	Breakdown Voltage (PORV)	65	85	90
GaAs MESFET	Maximum Channel Temp. (deg C)	85	100	125
	Power Dissipation (PORV)	50	60	70
	Breakdown Voltage (PORV)	60	70	70

KEY: PORV - Percent of Rated Value

RF TRANSISTOR APPLICATION NOTES:

1. RF transistors may be sensitive to ESD.
2. Design margins should be used for gain (+/-10% for screened devices; +/-20% for unscreened deviced), leakage current (+100%), switching times (+20%) and saturation voltage (+/-15%).
3. Heat sinks may be required to maintain derated junciton/channel temperatures.
4. The design may require exceeding voltage and power derating limits, but junction/channel temperature limits should be observed at all times.
5. The number of on-off cycles (temperature cycles) should be limited according to the derated power as shown in figure A-1.

Optoelectronic Device Stress Derating Criteria

Classification	Derating Parameter	Level I	Level II	Level III
Photo Transistor	Maximum Junction Temp. (PORV)	55	70	80
Photo Diode, APD	Maximum Junction Temp. (PORV)	55	70	80
Photo Diode, PIN	Maximum Junction Temp. (PORV) Reverse Voltgae (PORV)	55 70	70 70	80 70
Opto-coupler	Maximum Junction Temp. (PORV)	55	70	80
Injection Laser Diode	Maximum Junction Temp. (PORV) Power Output (PORV)	55 50	70 60	75 70
LED	Maximum Junction Temp. (PORV) Average Forward Current (PORV)	55 50	70 65	75 75

KEY: PORV - Percent of Rated Value

OPTO-ELECTRONIC DEVICE APPLICATION NOTES:

Photo Diodes:

1. The gain of APDs should be derated by 3 dB to account for gradual efficiency degradation and shifts in the operating point.

Opto-couplers:

1. External bypassing may be necessary to prevent damaging internal oscillations due to very high gain circuitry within the opto-coupler.
2. Allow for 15% degradation in opto-coupler current transfer ratio (CTR) over the sevice life of the design. This degradation is especially prevalent at low drive current. The input drive current should be well above the turn-on point.

Light Emitting Diodes (LEDs):

1. Current limiting is requred (using a series resistor).
2. Half or full wave rectified AC sine wave is not recommended for LED drive current. If rectified AC is used to drive LEDs, the peak value of the current must never exceed the allowable DC current maximum.

Injection Laser Diodes (ILDs):

1. Power supplies for ILDs must be carefully designed to completely elminiate current pulses which may cause catastrophic facet damage.
2. Output power should be given a 3 dB margin to account for gradual degradation of the device.
3. Mechanical stress, such as thermal or mechanical shock and vibration, cause crystal lattice defects (dark lines) to grow. Stress screening can be used to eliminate devices with these defects.
4. Excess optical power of ILDs will damage facets and will destroy the device. Note that optical power output is strongly temperature dependent and must be monitored and controlled to assure safe operation.
5. For SiO2 glassivated devices, the integrity of the package hermetic seal must be maintained to prevent moisture

Chip Capacitor Stress Derating Criteria

Classification	Derating Parameter	Level I	Level II	Level III
Ceramic (CDR)	Maximum Operating Temp. (PORV) DC Voltage (PORV)	85 60	85 60	85 60
Solid Tantalum (CWR)	Maximum Operating Temp. (deg C) DC Voltage (PORV)	85 60	85 60	85 60

KEY: PORV - Percent of Rated Value

CHIP CAPACITOR APPLICATION NOTES:

1. The sum of the peak AC voltage plus any DC bias voltage must not exceed the maximum derated operating voltage.
2. Precautions outlined in MIL-STD-198E should be followed.
3. (Ceramic) A design tolerance of +/- 12% should be allowed.
4. (Tantalum) A design tolerance of +/- 8% should be allowed.

Chip Resistor Stress Derating Criteria

Classification	Derating Parameter	Level I	Level II	Level III
Thick/Thin Film (RM)	Maximum Operating Temp. (PORV) Power (PORV) Voltage (PORV)	80 50 75	80 50 75	80 50 75

KEY: PORV - Percent of Rated Value

CHIP RESISTOR APPLICATION NOTES:

1. Chip resistors are sensitive to ESD.
2. The design should tolerate a 2% shift in resistance value.
3. Proper trimming is required to prevent latent failure in low noise applications.
4. Resistor stacking should be avoided.
5. For pulse applications, the average power calculated from pulse magnitude, duration and repetition frequency is used to establish the power derating requirement.
6. Pulse magnitude should be used to establish the voltage derating requirement.
7. Film temperatures must stay below 150 degrees Celsius.
8. Voltage stress should stay less than 2 volts per mil.
9. Power density should stay less than 200 watts per square inch.
10. The effective resistence value will be reduced when used at frequencies over 200 MHz beceuse of shunt capacitance between the resistive elements and the connecting circuits.

SAW Device Stress Derating Criteria

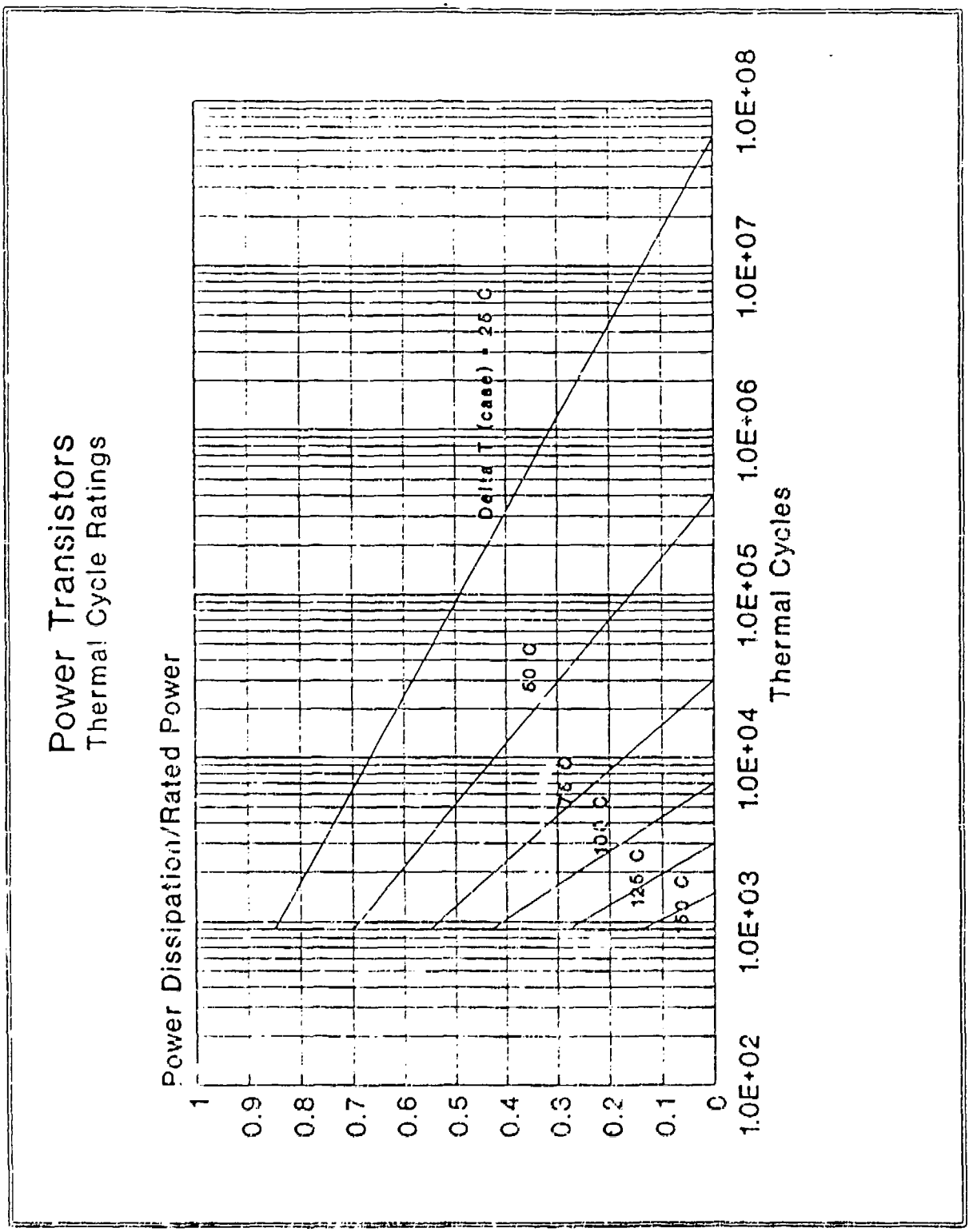
Classification	Derating Parameter	Level I	Level II	Level III
(All)	Input Power (<500 MHz) (FML) Input Power (>500 MHz) (FML) Operating Temperature (deg C)	+18 dBm +13 dBm 125	+18 dBm +13 dBm 125	+18 dBm +13 dBm 125

KEY: FML - From Maximum Limit

SAW DEVICE APPLICATION NOTES:

1. SAW devices are sensitive to ESD.
2. Integrity of the hermetic package must be maintained.
3. The design should not subject the SAW device to the rated maximum of shock, vibration and temperature cycling.

Figure A-1 On-Off Cycling Limits for Power/RF Pulse Transistors



Appendix B

```
C
C*****************************************************************
C
C       PROGRAM DERASIC1.FOR
C
C       PURPOSE:
C
C          Compute derating curves for ASIC - MOS Digital and Linear
C          devices given a constant probability of success or a
C          constant failure rate (with time).  Revision 1
C
C*****************************************************************
C
        IMPLICIT REAL*8(A-H,O-Z), INTEGER*4(I-N)
        CHARACTER*80 HEADER
        DIMENSION VDATA(7,177),NEXT(7)
C
C       Open Input and Output Data Files
C
        OPEN (5,FILE='INPUT.DAT',STATUS='OLD')
        OPEN (6,FILE='TEMP.DAT',STATUS='NEW')
        OPEN (10,FILE=' ',STATUS='NEW')
C
C       TDDB Constants
C
        UO = 8.4D0
        SO = 0.4D0
        AO = 1.7816D5
        TO = 22.D0
        Ea = 0.3D0
        EO = 2.222D0
        BETA = 4.5D0
C
C       Input Required Data
C
        READ (5,*,END=500)
5       CONTINUE
        READ (5,2000,END=500) ITYPE,DUMMY,A,PiQ,PiL,PiE,MINLG,MAXLG,
     *     MINLH,MAXLH,MINTP,MAXTP,INCTP
        WRITE (*,2000) ITYPE,DUMMY,A,PiQ,PiL,PiE,MINLG,MAXLG,MINLH,
     *     MAXLH,MINTP,MAXTP,INCTP
C
C       Begin Number of Gates Increment Loop
C
        DO 400 K = 0,6
C
C       Initialize Data Array
C
           DO 20 I = 1,7
              DO 10 J = 1,177
                 VDATA(I,J) = 0.D0
```

```
10          CONTINUE
            NEXT(I) = 0
20       CONTINUE
C
         GATES = 10.D0**(DBLE(K)/2.D0) * 1000.D0
C
C     Calculate # of Transistors and # of Pins
C
         TR = GATES * 4.D0
         PINS = 11.07D0 * GATES ** 0.342D0
C
C     Calculate TOX, AS, Area Acceleration, C1 and C2
C
         TOX = 4.93D0 / TR ** 0.286D0
         AS = 1349.D0 * TR ** 0.309D0
         CALL AA(AO,AS,UO,ACCAA)
C
         C1 = 0.01D0 + 0.000427D0 * GATES**0.588D0
         C2 = 2.8D-4 * PINS**1.08D0
C
C     Begin Time Increment Loop
C
         DO 200 J = MAXLH,MAXLH
            STIME = DBLE(J)
            TIME = 10.D0**J
            IF (ITYPE) 30,30,40
30          CONTINUE
            Psmax = DUMMY
            Elmax = -1.D6 * DLOG(Psmax) / TIME
            GOTO 50
40          CONTINUE
            Elmax = DUMMY
            Psmax = DEXP(-1.D-6 * Elmax * TIME)
50          CONTINUE
C
C     Calculate  Max Temp From Lambda 217F For Number of Gates and Pins
C        After Checking For Out Of Range Condition
C
            ARG = Elmax/(PiQ*PiL) - C2 * PiE
            IF (ARG.LE.0.D0) GOTO 150
            TEMP = 1.D0/298.D0-DLOG(10.D0*ARG/C1)/A
            TEMP = 1.D0 / TEMP - 273.D0
            MAXIMP = DINT(DMIN1(DBLE(MAXTP),TEMP))
C
C     Output Status
C
            WRITE (*,*) 'TEMP = ',TEMP,'      Elmax = ',Elmax
            WRITE (6,*) 'TEMP = ',TEMP,'      Elmax = ',Elmax
C
C     Begin Temperature Increment Loop
C
```

```
                NEXT(J+1) = 0
                DO 100 I = MAXIMP,MAXIMP,INCTP
                   TS = DBLE(I)
                   CALL AT(TO,TS,Ea,ACCAT)
C
C       Calculate Failure Rate for New Temperature Using MIL-HDBK-217F
C
                   PiT = 0.1D0*DEXP(-A*(1.D0/(TS+273.D0)-1.D0/298.D0))
                   EL = PiQ * PiL * (C1 * PiT + C2 * PiE)
                   IF (EL.GE.ELmax) GOTO 100
                   Psac = DEXP(-1.D-6 * EL * TIME)
                   Fcc = 1.D0 - (Psmax / Psac)
                   CALL ZVAL(Fcc,Z)
                   U = STIME - SO * Z
                   ACCAEF = (10.D0**(UO - U/ACCAA)) / ACCAT
                   ES = DLOG(ACCAEF) / BETA + EO
                   V = ES * TOX * 10.D0
                   IF (V.GT.18.D0) V = 18.D0
                   NEXT(J+1) = NEXT(J+1) + 1
                   VDATA(J+1,NEXT(J+1)) = V
                   VDATA(1,NEXT(J+1)) = TS
100             CONTINUE
                MAXI = MAX(NEXT(J),NEXT(J+1))
                GOTO 200
150             CONTINUE
                WRITE (*,*) 'ARGUMENT OUT OF RANGE'
                WRITE (10,*) 'ARGUMENT OUT OF RANGE'
200          CONTINUE
C
C       Output Data
C
             WRITE (*,*) DUMMY,A,PiQ,PiL,PiE
             WRITE (10,*) DUMMY,A,PiQ,PiL,PiE
             DO 300 I=1,MAXI+1
                WRITE (10,1000) VDATA(1,I),(VDATA(J+1,I),J=MAXLH,MAXLH)
300          CONTINUE
400       CONTINUE
          GOTO 5
500       STOP
C
C       Format Statements
C
1000      FORMAT (1X,7F10.2)
2000      FORMAT (I2,G9.4,4G8.2,7I5)
          END
```

```
      SUBROUTINE AA(AO,AS,UO,ACC)
C
C*****************************************************************************
C
C     SUBROUTINE AA
C
C     PURPOSE:
C
C        Calculate the acceleration factor due to dielectric area
C         relative to a reference area.
C
C     USAGE:
C
C        CALL AA (AO,AS,UO,ACC)
C
C     DESCRIPTION OF PARAMETERS:
C
C        AO  - reference area (square microns)
C        AS  - operating area (square microns)
C           UO   - log of median time of reference distribution (hours)
C        ACC - acceleration factor
C
C     SUBROUTINES AND FUNCTION SUBPROGRAMS REQUIRED:
C
C        ZVAL - calculates number of sigmas from the mean
C
C*****************************************************************************
C
      IMPLICIT REAL*8 (A-H,O-Z), INTEGER*4 (I-N)
      F = AO / (AO + AS)
      CALL ZVAL(F,Z)
      ACC = 1.D0 + (Z / UO)
      RETURN
      END
```

```
      SUBROUTINE AT(TO,TS,Ea,ACC)
C
C*************************************************************************
C
C       SUBROUTINE AT
C
C       PURPOSE:
C
C           Calculate the acceleration factor due to temperature stress
C           relative to a reference temperature
C
C       USAGE:
C
C          CALL AT (TO,TS,Ea,ACC)
C
C       DESCRIPTION OF PARAMETERS:
C
C          TO  - reference temperature
C          TS  - operating temperature
C          Ea  - activation energy (eV/deg K)
C          ACC - acceleration factor
C
C       SUBROUTINES AND FUNCTION SUBPROGRAMS REQUIRED:
C
C          NONE
C
C*************************************************************************
C
       IMPLICIT REAL*8 (A-H,O-Z), INTEGER*4 (I-N)
       B = 8.617D-5
       ACC = DEXP((Ea/B)*(1.D0/(TO+273.D0) - 1.D0/(TS+273.D0)))
       RETURN
       END
```

```
      SUBROUTINE ZVAL(F,Z)
C
C*****************************************************************************
C
C     SUBROUTINE ZVAL
C
C     PURPOSE:
C
C        Calculates the number of sigmas away from the mean of a
C        normal distribution for a given probability of failure
C        (cumulative percent failure in decimal).  This subroutine
C        uses the Newton-Raphson method of finding roots.
C
C     USAGE:
C
C        CALL ZVAL(F,Z)
C
C     DESCRIPTION OF PARAMETERS:
C
C        F - probability of failure (cumulative percent failure in
C            decimal)
C        Z - number of sigmas from the mean of the normal distribution
C
C     SUBROUTINES AND FUNCTION SUBPROGRAMS REQUIRED:
C
C        CNDA - cumulative normal distribution approximation
C
C*****************************************************************************
C
      IMPLICIT REAL*8 (A-H,O-Z), INTEGER*4 (I-N)
C
      IF (F.LE.0.5D0) ZNEW = -0.5D0
      IF (F.GT.0.5D0) ZNEW = 0.5D0
      Z = ZNEW
C
      DO 5 N=1,100
         CALL CNDA(Z,FNEW,IFLAG)
         IF (IFLAG.EQ.-1) FNEW = 0.D0
         IF (IFLAG.EQ.1) FNEW = 1.D0
         PHI = FNEW - F
         PHIPRI = 1.D0/(DSQRT(2.D0*3.141592653589793)*DEXP(.5D0*Z**2))
         ZNEW = Z
         Z = Z - PHI / PHIPRI
         IF (DABS(Z-ZNEW)/DABS(Z).LT.0.0000001D0) RETURN
5     CONTINUE
      RETURN
      END
```

```
      SUBROUTINE CNDA(Z,F,IFLAG)
C
C*************************************************************************
C
C     SUBROUTINE CNDA
C
C     PURPOSE:
C
C        Calculates the value of the cumulative normal distribution at
C        a given number of sigmas away from the mean.  This subroutine
C        uses a series expansion of the normal distribution to perform
C        the integration.
C
C     USAGE:
C
C        CALL CNDA (Z,F,IFLAG)
C
C     DESCRIPTION OF PARAMETERS:
C
C        Z     - number of sigmas from the mean = (x - u) / s
C        F     - area under the normal distribution at Z
C        IFLAG - error flag =  0  OK
C                           = -1  Z is less than -5.5
C                           =  1  Z is greater than 5.5
C
C     SUBROUTINES AND SUBPROGRAMS REQUIRED:
C
C        NONE
C
C*************************************************************************
C
      IMPLICIT REAL*8 (A-H,O-Z), INTEGER*4 (I-N)
      N = 0
      F = 0.D0
C
      IFLAG = 0
      IF (Z.GT.5.5D0) IFLAG = 1
      IF (Z.LT.-5.5D0) IFLAG = -1
      IF (IFLAG.NE.0) RETURN
C
1     FACT = 1.D0
      DO 3 N=0,135
           RN = N
           IF (N.EQ.0) GO TO 2
           FACT = FACT * RN
2          SUMN = (-1.D0)**N * Z**(2*N+1)
           SUMD = (2.D0*RN+1.D0) * 2.D0**N * FACT
           SUM = SUMN / SUMD
           F = F + SUM
3     CONTINUE
      F = F / DSQRT(2.D0 * 3.141592653589793) + 0.5D0
      RETURN
      END
```

MISSION

OF

ROME LABORATORY

Rome Laboratory plans and executes an interdisciplinary program in research, development, test, and technology transition in support of Air Force Command, Control, Communications and Intelligence (C^3I) activities for all Air Force platforms. It also executes selected acquisition programs in several areas of expertise. Technical and engineering support within areas of competence is provided to ESD Program Offices (POs) and other ESD elements to perform effective acquisition of C^3I systems. In addition, Rome Laboratory's technology supports other AFSC Product Divisions, the Air Force user community, and other DOD and non-DOD agencies. Rome Laboratory maintains technical competence and research programs in areas including, but not limited to, communications, command and control, battle management, intelligence information processing, computational sciences and software producibility, wide area surveillance/sensors, signal processing, solid state sciences, photonics, electromagnetic technology, superconductivity, and electronic reliability/maintainability and testability.