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RELIABILITY ASSESSMENT OF SURFACE MOUNT TECHNOLOGY (SMT)

Gretchen A. Bivens

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This report documents an in-house study that was conducted in order to assess the current reliability problems associated with surface mount technology (SMT). Specific areas investigated included failure modes, design guidelines, reliability prediction techniques and reliability evaluation test methods associated with SMT. A literature search was conducted and many IR&D programs were reviewed. The results showed a considerable amount of research in the area of SMT failure modes and in the development of SMT design guidelines. The two areas that were deficient were the development of a reliability prediction technique for SMT and the appropriateness of current reliability evaluation test methods.

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0.0 INTRODUCTION

As military systems become more complex, the chances of failures increase because more parts of the system can fail. Reliability assessment also becomes more difficult. No longer are failures caused by a single failure mechanism. Now they are caused by a combination of mechanisms. When these combinations are not considered, early failures occur. Failures can also occur early due to unknown environmental conditions. For example, back in 1963, the submarine, THRESHER, was destroyed and 129 lives were lost. This loss might have been avoided had engineers known about the deep ocean currents and disturbances. Now, through research and testing, engineers have a much better knowledge of the deep water environment and this information is used in their designs. A similar situation occurs with aircraft and spacecraft. Some information is known about these environments, but there is much more yet to be learned. For now, design engineers must utilize what they know and do their best to predict fielded response.

Traditionally, data has been collected from fielded systems, analyzed and formulated into reliability prediction models. Currently, however, several emerging technologies have little or no field data and are too complex to consider single failure mechanisms for each failure mode. The reliability of these systems must still be assessed in order to ensure reliable systems. Surface Mount Technology (SMT) is one such emerging technology. Because of the lack of field data, reliability assessment is currently being performed by testing preliminary boards to see if the boards can survive specific environments. This can be costly and time consuming when the designs must be modified several times before the assembly meets the test standards.

1.0 SUMMARY

The need to assess the reliability of SMT became apparent as more and more military systems began to use this technology. Rome Air Development Center (RADC) initiated this study to investigate the failure modes, design guidelines, reliability prediction techniques and reliability

evaluation test methods associated with SMT. Once the status of these areas is understood, steps can be taken to improve any deficiencies.

A literature search was conducted. The results showed many articles, papers, independent research and development (IR&D) program reports that documented a considerable amount of research in the area of SMT failure modes. Focal points for the IR&D programs were contacted and additional information obtained. Many military contractors visited RADC and gave briefings outlining their research.

Only two problems were encountered in this investigation. The first was the difficulty of obtaining field data. There are not many fielded systems using SMT. For the few systems already deployed, reliability data is almost nonexistent. Secondly, even though a significant amount of test data exists, many of the testing parameters in the data varied from contractor to contractor, thus making it difficult to compare the results.

The results of this study show that the failure modes driving the reliability of SMT are the failure of the solder connection and the failure of the plated-thru-hole (PTH). The main factor affecting these modes involved the Coefficient of Thermal Expansion (CTE) of the device, board, solder and PTH materials. Other factors include the solder connection designs, package size, assembly techniques, temperature distribution, operating temperature and the quality of the materials. Preliminary guidelines have been written and should be carefully considered for each one of these areas of concern.

SMT is a new technology whose long term reliability has yet to be determined. The best possible way to ensure reliable military systems is to follow design and manufacture guidelines that are currently available. The guidelines include a Navy report on boards using leadless chip carriers and documents published through industry organizations; e.g., the Institute for Interconnecting and Packaging Electronic Circuits (IPC) and the Institute of Electrical and Electronic Engineers (IEEE).

The main failure mode, the open or intermittent failure of the solder connection, results from solder fatigue and creep. Most electronic failures occur at a constant failure rate, but this solder connection failure occurs at an increasing rate. Therefore, new reliability prediction techniques are needed for SMT. The technique used must consider the material stress caused by environment and the strength in the solder. Failure occurs once the stress exceeds the solder's strength. Information used in the formulation of a prediction or assessment model should include data from fielded systems (if available) and laboratory testing.

The current method being used to evaluate the final reliability of a surface mounted assembly (SMA) is to environmentally test the SMA before entering the production phase. It is important that these tests give an accurate measure of reliability. Therefore, an evaluation must be made of the current environmental testing in particular, the thermal tests used to ensure reliable assemblies. Specific concerns of the thermal cycling tests involve the cycle frequencies and temperature extremes. These concerns stem from the effects of temperature on creep phenomena in the solder. The number of temperature cycles to failure are decreased by increased maximum temperature and by increased frequency, i.e., increasing the dwell time at the maximum temperature.

2.0 CURRENT ACTIVITIES

Currently, the military is using SMT in many of its systems. A list of military systems was reported by Robert Reynolds in his article entitled "Surface-Mount Electronics Meet the Military's High Reliability Needs" in the August 1985 issue of Defense Electronics. This list is displayed in Table 1 and includes 7 programs in the production phase, 15 programs in the pre-production phase, and 52 in the development phase. These figures indicate that the military is already committed to the use of surface mount devices (SMDs) and, therefore, must ensure their reliability.

At present, there is a DoD Ad Hoc Committee on SMT which is looking at the problems associated with surface mounting. The DoD Ad Hoc Committee consists of both DoD and industry representatives and is addressing the

TABLE 1: PROGRAMS COMMITTED TO SURFACE MOUNT TECHNOLOGY (AS OF AUGUST 1985) (Ref. 1)

Development Phase

Small ICBM (SICBM)
F-20 Radar
Agusta Helicopter
Navstar Global Positioning System
Fire Support Team (FIST) Digital Message Device
Advanced Capability EA-6B EW Aircraft
Milstar Ground Support Equipment
Low-Altitude Navigation Targeting Infrared System for Night (LANTIRN)
Target Acquisition FLIR
Scanned Image Display
Miniaturized Receiver Terminal
Marine Air Traffic Control & Landing System (MATCALS)
Modular Anti-Jam Integrated Communications (MAJIC) 5
Light Airborne Multipurpose System(LAMPS)Radar
ALQ-149 (Countermeasures)
Malfunction Detection, Analysis & Recording (MADAR)
Digital Scan Converters for
P-3 Orion Aircraft
Commander's Independent Thermal Viewer
Ground Target Control System
Defense Satellite Communications System
Platoon Early Warning System
Integrated Communications, Navigation, Identification Avionics System (ICNIA)
Integrated Electronic Warfare System (INEWS) (active & passive countermeasures)
Infrared Search and Track (IST)
Passive/Active Location System (PALS)
Medium-Lift Aircraft
PAVEWAY IV Laser-Guided Bomb
Harpoon Missile
AAWS Tank Breaker
Interactive Display Terminal (JTIDS)
Light Helicopter, Experimental (LHX) Radar
JVX Low-Cost Tracker
Solid State Phased Array (SSPA) Radar
Mast-Mounted Fire Control System (MMFCS) Digitally (VHSIC insertion)
Multi-Information Distribution System (MIDS)
Digital Message Device
ALR-69
Advanced Narrowband Digital Voice Terminal(ANDVT)
Consolidated Very Low Frequency(CVLF)Radio
ALQ-99 (Countermeasures)
ALQ-131 (Jammer) (VHSIC insertion)
Advanced Inertial Navigation System (AINS)
VCP-VHSIC Communications Processor
VAX Militarized Computer
Data Accumulation & Distribution System (DADS)
Airborne Optical Adjunct (AOA)
F-14 and A-6 Retrofit
High Speed Anti-Radar Missile (HARM) (VHSIC insertion)
Seawolf (British Aerospace Shipboard Anti Missile System)
Aquila RPV
AYK-4 Airborne Computer
F-18 Flight Maneuver Control System

Preproduction Phase

Advanced Fighter Technology Integration (AFTI)
Advanced Medium-Range Air-to-Air Missile (AMRAAM)
Extremely Low Frequency (ELF) Submarine Communications
Sidewinder AAM
ALQ-135 (Countermeasures)
A-7 Digital Scan Converter
Enhanced Modular Signal Processor (EMSP) (AN/UYS-2)
Joint Tactical Information Distribution System (JTIDS) - F-15 Information System
Submarine Advanced Combat System (SUBACS)
Submarine Active Detection Sonar (SADS)
Trident II Fire Control
Single-Channel Ground Air Radio System (SINCGARS)
Consolidated Very Low Frequency (CVLF) Communication
F-16 Survivable Flight Data Recorder
EF-111A Raven EW Jamming Aircraft

Production Phase

UYK-44 Military Computer
B-1B Defensive Electronics
Bradley Fighting Vehicle Systems (BFVS)
Nighthawk Search and Rescue Helicopter
Standard Electronic Module (SEM)
F-16 Radar Module
ARC-182 Radio

concerns associated with the implementation of SMT. Some of these concerns are reliability assessment, environmental characterization, failure definition, solder/solder paste characterization, accept/reject criteria, critical assembly process factors, rework and repair, design, package standardization, coordination/consolidation of multiple efforts and an interim policy. The Committee has suggested that certification of the manufacturing process occur in the design phase of the program. This will ensure good quality control throughout the production phase.

There are also several non-government organizations and committees that are addressing the problems involved in SMT and are publishing documents which outline guidelines for design, manufacture and testing of SMAs. Committees and conferences held by the Electronic Industries Association (EIA), Institute for Interconnecting and Packaging Electronic Circuits (IPC), Institute of Electrical and Electronic Engineers (IEEE), Surface Mount Technology Association (SMTA), and others have given industry the opportunity to gain knowledge in this critical technology. In addition, IPC has provided several IPC documents and papers that give guidance on the many facets of SMT. Members from these societies and organizations and industry have formed the Surface Mount Council which is addressing industry's concerns over the implementation of SMDs.

The Surface Mount Council has proposed a five-year "plan" to expedite the implementation of SMT. This "plan" addresses the areas of component availability, component standardization, hermetic sealing, solderability, computer-aided design, thermal modeling tools, interconnection tools, bare board and assembly testing, cleaning, pick and place, and soldering. Some future goals of the Council include the evaluation of different package configurations and test criteria, the publication of solder joint integrity requirements, and the standardization of tab formats and assembly criteria.

A DoD organization that is investigating the problems associated with SMT is the Materials Laboratory at Wright-Patterson AFB. Many contracts addressing the problems of SMT are included in the Manufacturing Technology (Man Tech) program. This program is concerned with industry's ability

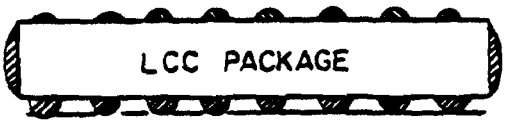
to apply VHSIC technology to military systems. VHSIC technology requires developing new packaging designs which can handle the high level of interconnection density. Two contracts in this program have made significant contributions to the development of SMT. The first was the contract "High Reliability Packaging Using Hermetic Chip Carriers (HCC) on Compatible Printed Wiring Boards (PWBs)" held by the coalition of Texas Instruments, IBM and Boeing, May 1983 through March 1989. The second is the contract "Advanced Digital Signal Processing" held by the coalition of General Electric, Westinghouse and Martin Marietta (March 1986 through December 1989).

The Navy and the Army have also made significant contributions to SMT by publishing documents, each addressing specific areas and applications. The Navy has a document (P-3651) written by Raytheon which was released in late 1987. This document addresses specific applications of leadless components on ceramic boards. The Army has a Technical Report, "Printed Wiring Boards Utilizing Leadless Components", that was published in December of 1983, and was written by Hughes Aircraft Co. Both of these documents address designs, material selection, thermal considerations, processes and testing requirements.

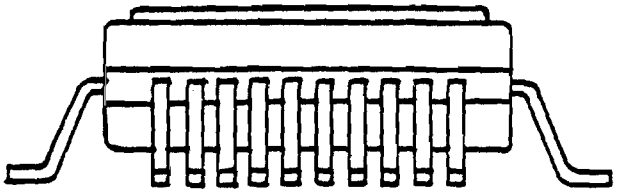
3.0 SMT DESCRIPTION

When manufacturing SMAs, solder footprints are deposited onto the surface of a board and surface mountable components are aligned with this footprint and then the components are soldered to the footprint. SMDs can have leads which are soldered to the footprint or can be leadless, in which case the castellation at the edge of the component is soldered directly to the board. This process differs from the manufacturing of thru-hole assemblies which consist of inserting a lead wire from a component through a hole drilled into the circuit board and soldering the lead into the board. There are several advantages to using the SMDs. The most commonly cited ones are the decrease in board size (up to 60 percent decrease), the increase in signal transfer speed, and the decrease in crosstalk.

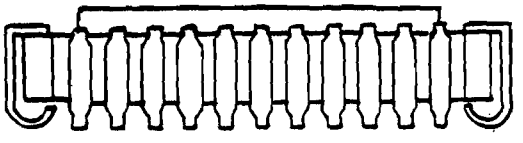
FIGURE 1: PACKAGE DESIGNS (REF. 6)



LEADLESS CHIP CARRIER



"GULL-WING" LEADED CHIP CARRIER



"J" LEADED CHIP CARRIER

The solder connections in surface mounting mate the outer edge of the device package to the top surface of the board. These connections do not penetrate the board surface. The packages used in surface mounting have three general designs: leadless chip carriers (LCCs), leaded chip carriers (LDCCs), and flat packs. The two most common designs for LDCCs are referred to as gull-wing and J-leaded. Pictures of these designs are shown in Figure 1. Leaded solder connections have more flexibility than the leadless connections; however, the leads are difficult to manufacture, handle and rework. The leaded connections do not have as great an ability to transfer heat as the leadless connections have.

Strains develop in the solder connection when the CTEs of the board and device material are not compatible. The CTE of the board material must closely match the CTE of the packaged device in order to minimize the occurrence of failures due to expansion differences. Some manufacturers have eliminated this mismatch of materials by using ceramic for the board material to match the ceramic devices most often used in military systems. Ceramic, however, is costly, heavy and brittle. An alternative is to substitute Kevlar fibers for the E-glass presently used as the support fabric in organic PWBs. Kevlar has the advantage of being lightweight, but also has the disadvantage of having poor thermal conductivity, high moisture absorption and high cost. Some manufacturers are constructing compatible boards by layering copper and invar material. As the ratio of the copper thickness to the invar thickness increases the thermal conductivity rate increases, but the weight of the board also increases.

4.0 SMT MANUFACTURE

The mounting of SMDs onto printed circuit boards (PCBs) has introduced reliability concerns due to the potential damage to the devices. Traditional thru-hole mounted printed wiring boards (PWBs) were assembled by wave-soldering the bottom of the boards. Since the devices were on the top of the PWBs, they were not directly exposed to liquid solder temperatures during the wave-soldering. For SMDs, which have the devices and the solder connections on the same side of the board, the devices will be

heated to liquid solder temperatures, regardless of the assembly method used. This high temperature exposure can degrade the SMDs.

There are many reflow soldering techniques associated with SMT. The well known reflow soldering methods include modified wave soldering, vapor phase, and infrared. Other methods include oven, hot gas and laser. These reflow soldering methods involve the screening of a solder paste onto the board, placing the device on the board and heating the board until the solder reflows around the solder connections of the device. Solder reflow methods can reduce potential component damage due to excessive temperature exposure. For example, when the operating temperature of these reflow systems is lower than 260^{o}C and there is a warm-up period, damage due to thermal stress and thermal shock is minimized.

Wave soldering is the conventional method that is used in soldering thru-hole devices. This method has been modified for SMA and now includes two soldering waves and a hot air knife. The second solder wave assures that any connection skipped over in the first wave will be subsequently soldered. The hot air knife reduces bridging between connections. These modifications have reduced voiding, bridging and shading. The problem with wave soldering is that most wave soldering machines operate at an average temperature of 260^{o}C. Soldering at these high temperatures can leave residual stresses in the solder connections.

Vapor phase reflow soldering involves passing SMAs through a saturated vapor at 215^{o}C. When the vapor condenses on the solder joint, the heat released melts the solder which redistributes itself to form a solder connnection. Some advantages of the vapor-phase process are uniform heating of all components, no overheating of components, very little oxidation and very easy flux removal. The disadvantages are high cost, and contamination of the vapor and prolonged exposure of packaged devices to high temperatures. Board sizes that can be handled by this technique range from 5.5 x 5.5 inch boards to 24 x 18 inch boards.

The infrared (IR) reflow soldering method heats the components through the absorption of radiant energy. This method attempts to control

the maximum temperature at approximately 215°C but cannot assure uniform heating due to the different emmissivities of the board and device materials. Flux is more difficult to clean after IR soldering as compared to vapor-phase soldering. Since IR converts 90 percent of all input energy into processing energy, it economizes on power consumption.

A reliability concern associated with production is the manufacturing of mixed boards. Mixed boards are boards that have both surface-mounted and thru-hole mounted components. Problems occur because these boards must go through the soldering process twice, once for the SMDs and once for the thru-hole components. Several contractors who want to take advantage of the SMD's decrease in board space and who find specific SMDs unavailable, manufacture mixed boards. As SMDs become increasingly available, the extent of mixed board manufacturing may decrease. Until such time, however, mixed boards will most likely continue to exist.

5.0 FAILURE MODES

The two main failure mechanisms in SMAs, the failure of the solder connection and the failure of the PTH, are due to the thermal expansion rates in the SMA. Failures occur because as the devices and the underlying board expand unevenly in the plane of the board (x-y plane), the solder connnections between these two mediums are strained. To reduce the occurrence of solder connection failures, the board's x-y plane expansion must be controlled. As the board and the via hole material expand unevenly in the direction perpendicular to the plane of the board (z-axis), strain develops in the via hole until a break occurs. To reduce the occurrence of via hole failures, the board z-axis expansion must also be controlled. Unfortunately, decreasing the expansion in one plane causes an increase in expansion in the other plane. The best board material is not one with the lowest horizontal expansion rate or the lowest vertical expansion rate, but rather, the material that minimizes expansion in both the x-y plane and z-axis. Other factors affecting the reliability of the assemblies include: bending of the solder connections on leaded devices, unsolderable boards, misalignment, lifting of the solder pad off of the board, and warping of the board. Since these failure mechanisms are associated with

the assemblies, the methods used to test for these failures are those listed in Table 2. This list was developed by Eugene Blackburn of RADC/RBRE.

5.1 FAILURE MODE 1: THE SOLDER CONNECTION FAILURES

The solder connection has become a critical factor in the reliability of SMAs. The solder connections between the device (IC package, resistor, capacitor, etc) and the board must provide an electrical transfer point and must also provide the mechanical connection. Becoming a mechanical support for the packages exposes the connections to significant amounts of stress and strain. This strain, along with temperature changes, can alter the material's state. Significant changes in the material's state can induce changes in the electrical parameters, produce excess fatigue and cause cracking of the solder connections. Each of these mechanisms leads to a breakdown in the transfer of electrical signals, thus degrading the component performance.

The actual failure of the solder connection is caused by fatigue and creep in the solder. Solder is a material whose mechanical properties are temperature and time dependent. The grain structure of solder is affected by the temperature vs time history for each sample and this structure affects the solder's mechanical strength. Solder with a small grain structure has greater strength than solder with a large grain structure. A larger grain structure occurs when solder is cooled at a slow rate and when solder is maintained at a constant, high temperature. This has been demonstrated by the failure data from thermal cycling tests. When the cycling rate is decreased or the dwell time at maximum temperature is increased, the number of temperature cycles to failure decreased.

When operating SMAs at high temperatures, solder creep becomes an important factor in the life expectancy of the part. "Creep can be defined as the slow and progressive deformation of a material with time under a constant stress." Metals usually begin to exhibit creep when heated to 40 percent of the melting temperature. The softening to melting temperature for common tin/lead solders is between 182 and 240^{o}C. When solder is

exposed to high temperature values (e.g., above 95°C) for long periods of time, creep causes solder deformation that leads to solder connection failures. Temperatures must be kept below creep levels in order to reduce the occurrence of these failures.

TABLE 2: QUALIFICATION TEST REQUIREMENTS FOR SURFACE MOUNTED DEVICES

Temperature Cycling:	-55°C to +125°C (typically 1000 cycles) per MIL-STD-883, Method 1010.
Thermal Shock:	-55°C to +125°C (typically 15 cycles) per MIL-STD-883, Method 1011.
Moisture Resistance:	Temperature cycle over 25°C to 65°C in 90 to 100 percent relative humidity (typically 10 cycles) per MIL-STD-883, Method 1004.
Mechanical Shock:	Minimum 1500 g level (or as dictated by system requirements when greater) per MIL-STD-883, Method 2002.
Vibration:	60 Hz; 4 hours; x, y, z planes with a peak acceleration of 20 g per MIL-STD-883, Method 2005.
Constant Acceleration:	5000 g level minimum per MIL-STD-883, Method 2001.
Salt Atmosphere:	24 hours at 35°C in a fog yielding a deposition rate between 10000 and 50000 mg per sq meter per MIL-STD-883, Method 1009.
Power Cycle:	Operate device at full rated power while holding substrate at ambient temperature (number of cycles based on system power up/down projection).
Thermal Impedence θ_{JC} Testing	

Factors affecting the fatigue life of the solder joint include the difference in CTE between the board and the substrate, the temperature distribution in the board and substrate, the soldering process, preproduction testing, and soldering materials. The difference in thermal expansion rates between the substrate and the board must be kept at a minimum or the solder joint will crack open. The picture in Figure 2 indicates the direction of the thermal expansion. Two common ways of minimizing this expansion difference are mounting a device onto a board that has a similar

or equal CTE and allowing for a flexibility in the solder connection or in the top layer of the substrate. The temperature distribution in these materials must also be controlled in order to keep the expansion differences between the top and the bottom of the solder connection at a minimum. Many of the parameters in the soldering process affect the reliability of the solder joint. Some examples are the soldering temperature, the uniformity of the heat distribution, the quality of the materials used, the accuracy of the placement techniques, the ability of the process to minimize oxidation and contamination, etc. Preproduction testing, such as testing the PCB for solderability before plating, can increase the reliability of the soldered PCB by removing improper and unclean materials. The soldering materials also affect the solder joint reliability. When choosing a solder paste, the flux content, the type of flux, the particle size and shape, and the oxidation resistance must all be considered. The best solder depends on the type of soldering process used. The manufacturer must consider the strengths and weaknesses of each type of paste and choose which one will assure the most reliable connection for each application.

5.2 FAILURE MODE 2: VIA HOLE

Another critical failure mechanism in the SMA is the PTH connection referred to as a via hole. There are three types of vias; blind via, buried via and through via. A typical via crack in multi-layer board is shown in Figure 3. This breakage is caused by the z-axis expansion. One of the problems resulting from constraining the expansion in the x-y plane has been the increase in expansion rates along the z-axis. Consequently, the z-axis expansion in the substrate is causing copper vias to break under tension.

The fatigue life of the vias is affected by the board materials, the via cross-sectional area and the quality of the copper material. The expansion of the board in the vertical direction must be controlled by using boards that have a low CTE in this direction. The Ad Hoc Committee on SMT has proposed requiring an analytical proof of proper design for designs using a via hole height to hole diameter ratio greater than 4:1.

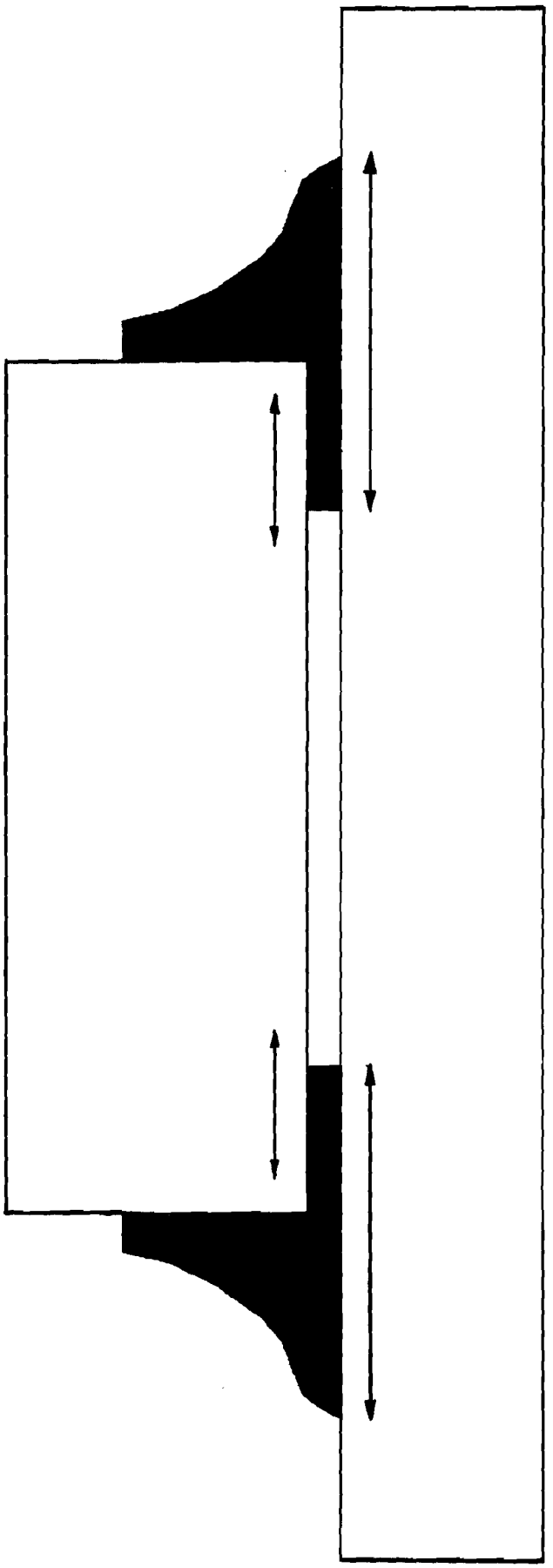
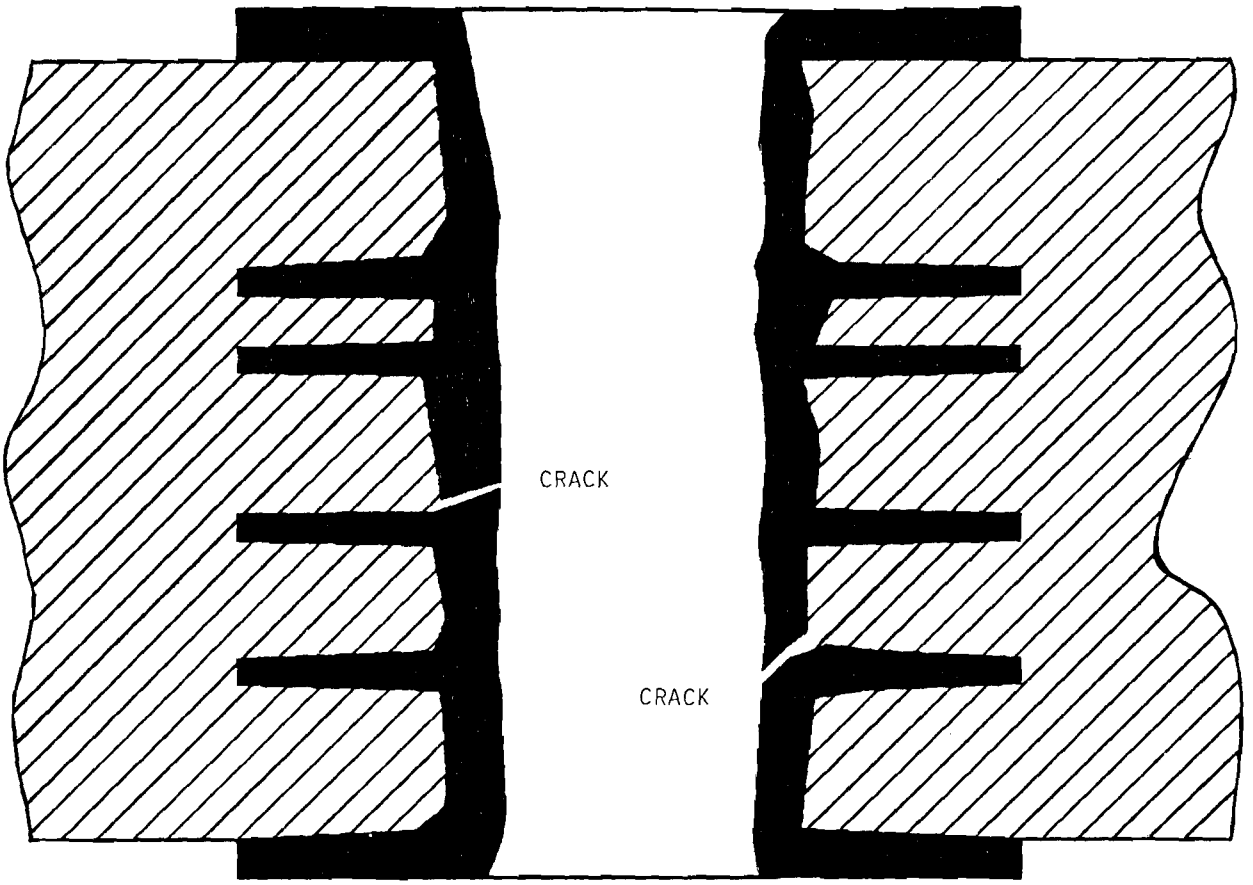


FIGURE 2: DIRECTION OF THERMAL EXPANSION

FIGURE 3: TYPICAL VIA CRACK IN A MULTI-LAYER BOARD



The quality of the copper material is being researched by many private companies. It is believed that minor changes in the via's material content and structure have significant affect on the ability of via's to undergo thermal cycling.

6.0 FINITE ELEMENT ANALYSIS

Finite element simulations of electronic devices can predict some of the failure modes of an SMA as a function of the physical and environmental factors. RADC is currently using finite element simulations for this purpose. Finite element methods are computer aided simulation techniques that are used to predict the response of structures. This technique is being used at RADC to predict the response of microelectronic devices to environmental conditions. Data obtained from these finite element analyses should be used to form reliability prediction models for certain types of failures. SMT is an area which could utilize this concept. For example, several finite element simulations have been made by RADC to determine the affects of the physical factors on the stress values in the solder (Ref #14). These physical factors include: the shape of the solder fillet; the spacing height between the package and the board; the package size; and the package and board materials. The results of these analyses can be used with statistical methods to predict a time to failure.

An example of a statistical method which can be used for this purpose is the interference method. The interference method designates the probability of a failure as the probability that the stress exceeds the strength. In the case of SMT, these factors are the thermal environment, package dimensions, solder joint designs and material properties. The interference is specified as the occurrence where the stress exceeds the strength and is determined through the use of analytical, field and test data. The reliability of the solder joint is then the probability of no interference. Further information on applying this method can be found in the following reports by Charles Lipson: RADC-TR-66-710 (March, 1967), RADC-TR-68-403 (December, 1968).

7.0 RELIABILITY PREDICTION TECHNIQUES

When designing electronic equipment, an analysis must be performed in order to determine whether the equipment will meet its reliability requirements. The current reliability prediction models used by the military are formulated using historical part failure data which creates difficulties in new technology areas such as SMT where there is a lack of field data. Current attempts in developing SMT prediction models are grouped into two main procedures; the modification of current prediction models, and the formulation of new models by using analytical simulation results, and test data and test results. Regardless of the procedure used to develop a prediction model, the following criteria must be satisfied: the model must have verified accuracy, have easily obtainable information and be a flexible expression which can easily be modified.

The Reliability Analysis Center (RAC) published a state-of-the-art report entitled "Surface Mount Technology: Reliability Reviews" (Ref. 11). This report presented reliability prediction models for PWBs, microcircuit packages and solder connections. A preliminary model for the PWB, displayed in Figure 4, looked at the various factors involved including complexity, quality and environmental factors. There was insufficient data for the model to go into detail, but the foundation for a future model was set.

The RAC reviewed the existing MIL-HDBK-217 microcircuit package model, Figure 5, and identified which factors were inappropriate for SMT. These factors were the temperature factor, π_T, and the complexity factor C_2. The temperature factor is based on heat dissipation and will vary for the SMD. A suggestion was made that the temperature factor be based on the thermal resistance, θ_{JC}. The table in MIL-HDBK-217 must be updated to include θ_{JC}'s for SMD's. The complexity factor does not consider the impact of varying lead designs (leadless, J-lead, gull-wing, etc.). The following formula was derived by the RAC and was based on RAC failure rate data.

$$C_2 = 8.28 \times 10^{-5} (Np)^{1.82}$$

where Np represents the number of connections.

A different modeling approach is being used to represent the solder connection failure mode because this failure mode is based on the fatigue of the solder material and has a Weibull distribution, which can have a failure free period. Most component failure modes in electronic equipment have a random occurrence and, therefore, have an exponential time-to-failure distribution (i.e., a constant failure rate). The solder connection failure is based on the stress and the strength in the solder. As time progresses, the stress in the solder increases and the strength decreases. Eventually, after a certain period of failure free time, the stress in the solder will exceed its strength and the solder will crack. The failure rate then increases exponentially once this failure free period has ended. Therefore, a modeling approach based on an increasing failure rate must be considered for Leadless Chip Carrier SMDs.

The RAC presented a preliminary solder connection model, Figure 6, which was based on the Coffin-Manson model. The Coffin-Manson model, Figure 7, relates the number-of-cycles-to-failure to the plastic strain range that occurs in the solder during use. The RAC then modified this model to consider the thermal and power-related temperature cycling as well as take into account the substrate material, the stand-off height, the chip carrier size, and the environmental conditions.

The RAC used Bell Lab's work, done by Werner Engelmaier, as a basis for the solder connection prediction model. Bell Labs formulated a model for shear strain by assuming a uniform strain distribution and neglecting the secondary effects of cyclic warpage and transient strain. The shear strain was then multiplied by a "non-ideal" factor to account for secondary effects. Experimental tests were then performed and the results of these tests were compared to the predicted strain. The results showed only a 12 to 27 percent difference between the test data and the original ideal configuration. This difference is accounted for by the "non-ideal" factor. This model, Figure 8, assumes the solder composition to be 60/40 Tin/Lead. This model can use the output stresses/strains from a finite element simulation to predict the number-of-cycles to failure.

FIGURE 4: PRELIMINARY PRINTED WIRING BOARD MODEL (Ref. 11)

$$\lambda_p = (\lambda_1 N_1 + \lambda_2 N_2 + \lambda_3 N_3)\ \Pi_C \Pi_Q \Pi_E$$

λ_p = PWB failure rate (failures/10^6 hours)
λ_1 = via PTH base failure rate
λ_2 = loaded PTH base failure rate
λ_3 = SMT proportionality constant
N_1 = number of via PTHs
N_2 = number of loaded PTHs
N_3 = number of surface mount connections
Π_C = complexity factor (based on the number of circuit planes)
Π_Q = quality factor
Π_E = environmental factor

$\Pi_C = .65(L)^{.63}$
L = number of circuit planes

FIGURE 5: MIL-HDBK-217 DEVICE PACKAGE MODEL (Ref. 11)

Existing series of MIL-HDBK-217

$$\lambda_p = \Pi_Q \left[C_1 \Pi_T \Pi_V + (C_2)\Pi_E\right] \Pi_L$$

λ_p = device failure rate (failures/10^6 hours)
Π_Q = quality factor
C_1 = circuit complexity factors
C_2 = package complexity factor
Π_T = temperature factor
Π_E = environmental factor
Π_V = voltage derating factor
Π_L = device learning factor

$C_2 = 8.28 \times 10^{-5} (N_p)^{1.82*}$

*New lead factor for SMD

FIGURE 6: PRELIMINARY SOLDER CONNECTION MODEL (Ref. 11)

$$MTTF = \Pi_b \Pi_n \Pi_{CCS} \Pi_E \left[\frac{1}{aN_1 + bN_2} \right]$$

MTTF = solder connection mean-time-to-failure (hours)

Π_b = base time to failure (based on substrate material)

= 3.3, epoxy/glass

= 440, copper clad invar

= 730, ceramic

Π_n = solder dimension factor

= $(h)^{2.4}$ where h = stand-off height (mils)

Π_{CCS} = chip carrier size factor

= $.69(L)^{-2.29}$ where L = chip carrier edge size (inches)

Π_E = environmental factor

N_1 = number of power cycles per hour

N_2 = number of environment-related temperature cycles per hour

a = power constant, based on TCE tailoring

b = environmental constant, based on ΔT

$$b = (\Delta T/25)^{-2.0}$$

FIGURE 7: UNMODIFIED COFFIN-MANSON MODEL (Ref. 11)

$$\Delta E_p = C\ (N_f)^{-\beta}$$

ΔE_p = plastic strain range

N_f = number of cycles to failure

C, β = constants

FIGURE 8: BELL LAB'S MODEL (Ref. 12)

$$N_f = \frac{1}{2} F\left[\frac{(CSR)}{2E_f^{1}}\right]^{1/C}$$

N_f: number of cycles to failure
CSR: cyclic strain range
$2E_f^{1}$: .65 (40/60 Tin/Lead)
F: "non-ideal" factor ($1.12 \leq F \leq 1.27$)
C: $-(0.442) - (6 \times 10^{-4})\ \bar{T}_s + (1.74 \times 10^{-2})\ \mathrm{Ln}\ (1+f)$
$\bar{T}_s$: mean cyclic solder joint temperature
f: cyclic frequency ($1 \leq f \leq 1000$ cycles/day)

In order to formulate reliability prediction models for SMDs, the existing PTH models can be compared with failure test data and the appropriate modifications made. This, however, is not the most accurate approach since the driving failure mode for SMDs is not the same as for PTH, thus, SMT is not properly represented. An alternative method is to generate new prediction models by using analytical results, test data, and physics-of-failure relationships. This model would give a time-to-failure value and is applicable in this area since the driving failure mechanism, the failure of the solder connection, is based on mechanical wear out of the solder.

8.0 DESIGN AND MANUFACTURE GUIDELINES

Traditionally thru-hole mounting was the primary method used to manufacture PCBs. SMT has introduced many reflow processes including modified wave soldering, vapor phase and infrared. Consequently, the manufacturing process has become an important consideration in the design of SMA. When establishing guidelines, equal consideration must be given to the design and manufacture stages. The Navy, Army and Air Force have produced guidelines which are discussed throughout this section.

One of the major reliability considerations in SMA production is the lead design of the package. The section on the solder connection failure

mechanism discusses the different design and manufacturing factors that must be considered. Other considerations in the design stage include the quality of the materials used, the physical size of the devices, the number of I/O connections, the heat dissipation method used, the material properties and the thermal resistance values.

The Navy document, "Leadless Components on Ceramic Circuit Boards," addresses the guidelines for LCC on ceramic boards. The ceramic boards were chosen because the CTE of these boards matches the CTE of the LCC and the LCCs were chosen because the LCCs have good thermal contact and are easy to handle. This documents problems associated with the manufacturing of these boards and outlines several of these problems and ways to prevent these problems from occurring. The guidelines cover computer-aided design (CAD), trace metals, physical layout guidelines, thermal coatings, soldering materials, cleaning methods, component placement and assembly inspection. The Navy states that following these guidelines will ensure a high reliability system for ceramic boards.

The designer of an assembly must consider the physical design layout, the intended use environment, the characteristics of manufacturing materials and the heat dissipation method. The Navy document has a section on the design practices for these SMAs. In particular, there is a section that outlines the recommended general procedure for the CAD of multilayer boards. This CAD outline covers the electrical, mechanical and layout considerations in the design stage. It suggests that the preliminary design review should cover the power dissipation calculations, initial thermal analysis, preliminary device layout, logic diagram, and the parts list. The critical design review should cover the performance specifications, preliminary thermal and reliability analysis results, logic diagram, and product documentation.

The Navy document gives designer guidelines on the size and spacing of the traces on the board. The minimum trace allowances for copper lines are listed below:

DIMENSION	MINIMUM	TYPICAL
Line width	0.005	0.010
Line-to-line spacing	0.005	0.010
Via size (square)	0.005	0.015
Via-to-via spacing	0.007	0.010
Line-to-via spacing	0.007	0.011
Conductor to ceramic blank edge	0.015	
Conductor to dielectric edge	0.0075	0.030
Via to dielectric edge	0.010	
Pad to dielectric edge	0.005	

The Navy document lists the following advantages when considering whether to use a copper or noble metal trace. The copper is preferable in the areas of cost, line resistivity, rework capability, and adhesion to dielectric surfaces. The noble metal is a much lower risk when working in high humidity environments and can tolerate wider lines than listed in the table for copper traces, but must also have a leach-resistant material on the top layer of the board. Since noble metal boards use the air-fired process and the copper use the nitrogen-fired process, the incompatibility of these systems must also be considered. Table 3 was taken from the NAVSO document and lists thick film incompatibilities.

When using ceramic boards, the Navy recommends some layout guidelines. First, when using ceramic blanks up to 5" x 5", the minimum thickness should be 25 mils for boards with one to five layers, and 40 mils for boards with six to eight layers. When determining the layout position of the thermal heat sinks, the high powered and high failure rate components should be located as close to the heat sinks as possible. In addition, metal or ceramic packages using eutectic die bonding will aid in forming a good thermal contact. To protect against contaminants, a conformal coating should be applied to protect the modules. Table 4 lists the properties of the four most common coating materials for ceramic boards.

TABLE 3: THICK FILM SYSTEM INCOMPATIBILITY (Ref. 4)

SUBJECT MATERIAL	INCOMPATIBLE WITH WHAT OTHER MATERIALS	REASON FOR INCOMPATIBILITY
NITROGEN-FIRED MATERIALS		
Substrate	Interlayer conductor	Adhesion, caused by organic contamination
	Interlayer dielectric	Bow, caused by mismatch in dielectric TCE
Interlayer conductor	Interlayer dielectric	Blistering or delamination, caused by trapped carbon or oxidized copper
Surface conductor	Interlayer dielectric	Adhesion, caused by low mechanical strength of dielectric
	Surface dielectric	Wicking, inherent in the two materials
		Cracking, caused by mismatch in TCE
	Solder	Solderability inhibited, caused by oxidation of copper
AIR-FIRED MATERIALS		
Substrate	Interlayer conductor	Adhesion, caused by organic contamination
	Interlayer dielectric	Bow, caused by mismatch in dielectric TCE
Interlayer conductor	Interlayer dielectric	Adhesion, caused by frit content in conductor
Surface conductor	Interlayer dielectric	Adhesion, caused by frit content in conductor
	Surface dielectric	Adhesion, caused by frit content in conductor
		Cracking, caused by mismatch in TCE
	Solder	Solderability inhibited, caused by glass-rich conductor surface

The quality of the materials has a significant affect on the integrity of the assembly. The Navy states that for a reliable ceramic board, there must be consistent raw materials and a stable manufacturing process. The solder paste selection is critical. If the contractor is having the paste supplied by another manufacturer, the Navy suggests that the following information be specified: the review and inspection of the data and identification sheets, the methods and equipment used to measure pastes, the nature of the circuit and processing conditions, and an agreement on what documentation will be supplied. Preproduction testing is a good way to assure quality materials. Suggested tests to be performed on ceramic board coupons include tests for conductor adhesion, conductor resistance, pad solderability, conductor integrity, dielectric leakage, insulation resistance, biased humidity, and the quality of fired print. The user should also check the printability, the oxide and solder ball formation, the tackiness, working life and residue removal.

When preparing the ceramic boards and components for production, proper cleaning must occur. If the boards and/or components are not adequately solderable, the solder connection between the component and the board will not form even with a considerable amount of manual rework. A solvent aqueous cleaning solution is used on ceramic boards and ceramic LCCs. The boards and LCCs are then visually inspected for wetting damage, excess solder, solder shorts, flux residue and leaching. Table 5 lists a cleaning summary on the different solutions, processes, and inspection criteria. There is also a special precaution for ultrasonic cleaning. This method of cleaning is not allowed by the Navy since it can cause damage to sensitive microelectronic parts.

Automatic placement is preferred over manual placement in the production of SMAs. If manual placement is used, there should be 100 percent operator verification of compliance with the placement, orientation, alignment, damage and mounting position. When reworking the assembly the methods in Table 6 are suggested.

TABLE 4: MODULE COATING MATERIALS - COMPARISON OF PROPERTIES (Ref. 4)

	PARYLENE	ACRYLIC	SILICONE	POLYURETHANE
REPAIRABILITY				
Method of coating removal for repair				
Solder-through	Fair	Good	Poor	Good
Solvent removal	No	Yes	No (but can be sofened by solvent)	No
Mechanical cutting	No	No	Yes	Yes (with hot knife)
Abrasive blasting	Yes	Yes	No	Yes
THERMAL PROPERTIES				
Resistance to continuous heat (^{o}C)	150	120	200	120
Linear coefficient expansion (microin/in/^{o}C)	35-70	50-90	200-290	100-200
Thermal conductivity (10^{4}cal/sec/ca^{2})	3	4-5	3.5-8	4-5
CHEMICAL RESISTANCE				
Effect of organic solvents	None	Softened & dissolved by common solvents	Softened by hydrocarbons	In general resistant
Effect of weak acids	None	None	Light	Light
Effect of weak bases (alkalides)	None	None	Light	Light
ELECTRICAL PROPERTIES				
Dielectric strength (v/mil), short time 23^{o}C, at 1.0 mil	5500-7000	2500	2000	3500
Volume resistivity (ohm-cm) 23^{o}C, 50% RH	10^{16}-10^{17}	10^{15}	10^{15}	10^{14}
Surface resistivity at 23^{o}C, 80 Hz	2.65-3.15	3.0-4.0	2.7-3.1	5.3-7.8
80 KHz	2.65-3.10	2.5-3.5	2.6-2.7	5.4-7.6
80 MHz	2.65-2.95	2.2-3.2	2.5-2.7	4.2-5.2
Dissipation factor 23^{o}C, 80 Hz	0.0002-0.020	0.20-0.04	0.001-0.007	0.015-0.05
80 KHz	0.0002-0.019	0.02-0.04	0.001-0.005	0.04-0.060
80 MHz	0.0006-0.013		0.001-0.002	0.005-0.070

TABLE 5: CLEANING SUMMARY (Ref. 4)

CLEANING SOLUTIONS	
Organic	For non-ionic contaminants Clorinated or flourinated solvents with addition of alcohol
Aqueous	For ionic contaminants Deionized water with or without a detergent
CLEANING PROCESSES	
General	Aqueous after solvent cleaning Minimize time between reflow and flux removal Thin out flux to facilitate cleaning Ensure component markings are not removed Adapt cleaning process to any change in solder and flux
Automated in-line (preferred)	Immersion followed by spray
Manual	Immersion followed by spray Slow, operator dependent
INSPECTION	
Visual	
Solvent extract	Ionograph
Destructive	Removal of component
SPECIAL PRECAUTIONS	
	No ultrasonic cleaning Attention to any change in solder paste Attention to code markings

TABLE 6: REWORK AND CIRCUIT MODIFICATION (Ref. 4)

Solder Joint Touchup The assembly is preheated (100°C), the defective solder joint is lightly fluxed, and the solder is reflowed with a temperature-controlled iron set at about 400°C.
LCC Replacement The assembly is preheated (100°C) and the defective device joints solder-reflowed by directing a stream of hot gas to the localized area. When reflow occurs, the defective device is removed. The device sites are then redressed, a new part is aligned, and the solder is reflowed by directing a stream of hot gas to the site.
Discrete Device Replacement The assembly is preheated to approximately 100°C. The lead joints of the defective device are then solder-reflowed with either a temperature-controlled soldering iron or a hot gas system. It can be lifted off the multilayer interconnect boards and after redressing, a replacement device can be soldered in.

The final inspection and test should include a visual inspection of the assembly, 100 percent electrical testing on each lot of boards and environmental screening tests. The inspection after solder reflow should review the component standoff height, component alignment after soldering and the cross-sectioning of solder joints. The Navy document suggested that the assembly be environmentally screened by thermal cycling the assembly 3-20 times from -55°C to +95°C. Other tests include salt fog, shock and vibration. Table 7 lists the general guidelines for final visual inspection.

The Army's technical report on leadless components outlines the materials used for the thermal mounting plate (TMP). For optimum reliability, the TCEs of the PCB and TMP materials should match. The best combination of materials was cited as Kelvar reinforced polyimide boards with a copper clad invar TMP. Table 8 lists other TMP materials along with the advantages and disadvantages of each. This report also outlines the following list of characteristics for TMP adhesive: ease of application and removal, high thermal conductivity, electrical insulation, good adhesion in adverse environments, thin compliant bondline, close CTE match to PCB material, low modulus of rigidity, and a low glass transition temperature.

The major Air Force work on SMT use guidelines is being done in the Man Tech program. The contract "High Reliability Packaging Using Hermetic Chip Carriers (HCC) on Compatible Printed Wiring Boards (PWBs)," part of the Man Tech program, concluded that Kevlar is currently the best support fabric to use to control both the solder connection and via hole failures. A current contract under the Man Tech program, "Advanced Digital Signal Processing," is using these Kevlar constrained boards to determine how materials and processes can affect the solder joint properties. General Electric is heading the task III group: Solder Process Controls. This group is looking at the component stability controls, the soldering materials, and the processes and controls. The following component solderability controls have been identified: minimize CTE difference, increase solder joint height underneath the chip carriers, increase the solder fillet size and have uniform joint geometry. The overall contract is researching six soldering processes: laser, infrared, belt reflow, vapor phase, inverted wave and conduction reflow. Inverted wave soldering is a modification of the wave soldering technique. There will be a set of assemblies manufactured for each of the six soldering processes. Each set of assemblies will then be subjected to thirteen different tests. The thirteen tests will vary the testing parameters in order to indicate how relatively small changes in test conditions affect the test results. The affects that heat up cycles, reflow temperatures and cool down rates have on the quality of the solder joint will be investigated. Since the boards used in these tests are Kevlar constrained boards, the data obtained from these tests can be used to formulate reliability prediction models and a set of guidelines for Kevlar boards only.

TABLE 7: GENERAL GUIDELINES FOR FINAL VISUAL INSPECTION (Ref. 4)

MATERIALS	
Chipouts of Ceramic	Extending into perimeter of designed thick film
	Extending under the designed thick film and reducing supporting ceramic
Cracks in Ceramics	Extending into perimeter of designed thick film
	Visible from top view and bottom view
Dielectric	Uniform coverage free from voids, pinholes, and cracks which expose underlying metallization
Metallization	Free from delamination
	Location and size of pads is design-specific
	Voids and blisters which decrease external solderable surface below requirement
	Bridging or reduced spacing
	Corrosion
	Surface irregularities when not associated with underlying features or internal touchup
Overglaze (as applicable)	Cracks detrimental to intended hermetic application
	Peeling, lifting, blistering, bubbles not entirely within the glassy film(s)
	Pinholes exposing dielectric or metallization
	Bleeding onto external solderable surface exceeding percent of solderable surface required
WORKMANSHIP	
Foreign Material	Bridging or reduced spacing or in any way interfering with component mounting
	Corrosive
Cleanliness	For tinned MIBs: resistivity testing to ohm-cm minimum
Registration	Metallization to ceramic edge, dielectric to ceramic edge per customer specifications

TABLE 8: THERMAL MOUNTING PLATE MATERIALS (Ref. 5)

Aluminum	o Significant thermal advantage. o Unsuitable because its high TCE will increase the TCE of any PCB material interconnected.
Copper	o Lower TCE than aluminum. o Must be plated with nickel to protect against corrosion.
Copper Clad Molybdenum	o Good thermal conductivity. o Good fabrication characteristics. o Poor availability. o High cost.
Molybdenum	o Acceptable TCE value. o Extremely high cost. o Fabrication problems.
Kovar	o Good TCE match o Restricted usage.
Copper Clad Invar	o High modulus of elasticity. o Dominates TCE of composite assembly. o Low cost. o Available. o Heavy (used when weight is not a factor).

9.0 MAINTENANCE CONSIDERATIONS

The maintainability of SMA is an issue that needs a significant amount of consideration. There are currently many repair/replacement equipments available. The most common and effective repair and replacement of SMDs utilizes the hot gas method. In this method, a hot gas is applied directly to the solder connection. Once the solder is reflowed, the chip carrier is removed, the surface cleaned, and the chip carrier replaced. It is important to keep the amount of heat affecting areas other than the solder joint at a minimum. This aspect should be considered in the designing stage. Components must have adequate spacing between each other and the placement of heat sinks should be carefully considered. Heat sinks placed improperly can drain the heat applied during removal, thus impeding the process. Other methods of removal and replacement include soldering irons, hot plates and infrared equipment. No matter which method is used, preheating the assembly close to solder's melting temperature before removal helps prevent thermal damage.

An article published in Electronic Packaging and Production entitled "The Removal and Replacement of SMCs" suggested the following criteria for the removal and replacement of SMD: there should be no damage to adjacent components and to the PCB; it should be a non-hazardous operation; it should require minimum skill; there should be minimum time to effect rework; the system should be capable of both removal and replacement; and it should be at a low cost. The criteria affecting the reliability is the damage to the devices and the boards. The criteria affecting the maintainability are the minimum time and the skill required. If the same piece of equipment is able to perform both the removal and replacement of a device, the reliability of the PCB will improve due to minimizing thermal damage and the maintainability will improve due to decreased time to repair.

The lead design on an SMD affects the accuracy of the replacement. One of the arguments for using the LCC versus the LDCC is the difficulty of replacing an LDCC. On high pin count LDCCs, where the lead spacing is less than 100 mils and in some cases as small as 20 mils, the replacement equipment must be very precise and the technician operating the equipment must be highly skilled. These factors increase the overall cost of incorporating LDCCs as well as LCCs into military programs.

10.0 EVALUATION OF TEST METHODS

Because of the unique behavior of solder, specifically the time and temperature dependent stress relaxation (creep), there are concerns with the current testing methods. Werner Engelmaier of Bell Labs listed some of these concerns as: cyclic stress levels too high, test frequencies too high, test temperature extremes too high or too low, inappropriate test methods and inappropriate conclusions from tests. In addition, the failure criteria must accurately identify the reliability of the device/system being tested. "Continuous continuity monitoring" during cyclic testing produces the most accurate test results. The best test method for representing the accurate service conditions is the powered functional cycling. Unfortunately, this testing procedure is also the most difficult and the most expensive.

Thermal cycling from -55°C to +125°C is being used as an accelerated test to compare the reliability of SMDs among the many different manufacturers of SMDs. It is assumed that the larger the number of cycles to failure, the more reliable the assembly. This might not be the case because of the changes in solder's mechanical properties over this temperature range. Important materials to investigate are the solder, where one of the main failure modes occurs, and the via/PCB material, where the other main failure mode occurs. An evaluation must also be made of the affect cycling frequency has on solder's properties since the solder connection failure mode is already known to be accelerated by slow thermal cycling. All of these factors must be considered in order to have appropriate test methods and to be able to make appropriate conclusions from the results.

11.0 CONCLUSIONS

This report documents an in-house study that was conducted in order to assess the current reliability problems associated with Surface Mount Technology (SMT). The results showed that a considerable amount of research has been completed in the areas of SMT failure modes and in the development of SMT design guidelines. Additional research, however, is needed in other areas of reliability concern. One area that needs further investigation is the development of a reliability prediction technique for SMT. The current method being researched to formulate reliability prediction techniques for SMT uses finite element prediction methods, environmental test data and statistical methods which relate the number of cycles to failure to the physical response in the solder. The second area that needs further investigation involves current reliability acceleration test methods. Because of the unique behavior of solder, there are concerns with the accuracy of using higher test cyclic frequencies and higher temperature extremes than what is actually experienced in the field. These acceleration tests might be misrepresenting the actual field failure mechanisms.

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