Reliability Design Handbook

No. RDH 376

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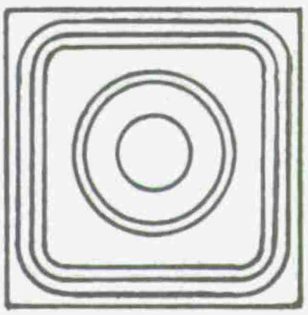

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RELIABILITY ANALYSIS CENTER

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RELIABILITY DESIGN HANDBOOK

March 1976

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Under Contract to:

Rome Air Development Center
Griffiss Air Force Base, NY 13441

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PREFACE

This Reliability Design Handbook is intended to serve as a tool for designers of military equipment and, in particular, for designers of equipment items that would typically make up avionics systems. The handbook provides guidelines for use by design engineers to assure the achievement of a reliable end product. From the standpoint of design, it is consistent with, and extends, basic concepts and reliability improvement techniques described in MIL-HDBK-217B. Specifically, the handbook provides design information, factors, and parameters, and other engineering data affecting reliability. In addition, the handbook describes the approach to reliable design, includes theoretical and cost considerations and describes methods covering such considerations as part control, derating, environmental resistance, redundancy and design evaluation.

The foresight of Air Force Systems Command and Rome Air Development Center in recognizing the need for a comprehensive guidance document to aid electronic design engineers in achieving design reliability goals provided the impetus for preparation of this handbook.

The cooperation and technical direction of Thomas Dellacave, RADC Project Engineer, in bringing this handbook to fruition is gratefully acknowledged. IIT Research Institute is indebted to the many RADC and contractor personnel who provided much of the reference material and who contributed guidance and constructive criticism during the research effort.

This handbook was prepared by IIT Research Institute (IITRI), Chicago, Illinois, under contract to RADC. The work was directed by R. T. Anderson, Manager of Reliability, with technical contributions by many IITRI staff members.

IIT Research Institute

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SECTION 1

INTRODUCTION

SECTION 1

INTRODUCTION

1.1 Purpose and Scope of the Handbook

This handbook has been prepared to serve as a tool for designers of military equipment and systems. The purpose of the handbook is to provide information and direction to the designer which will help him engineer reliability into an equipment during its basic design stage. To this end, it provides design data and guidelines for those safety, mission, maintenance and cost factors which together form the working elements of reliability engineering, system engineering and cost effectiveness.

This handbook is primarily intended for use in the design of new equipment(s) or systems which are largely composed of electronic parts and components. However, it can also be used for the design of systems which encompass both nonelectronic and electronic parts, as well as for the modification of existing systems.

This handbook embodies a preventive approach to reliability. From the standpoint of design, it extends basic concepts and reliability improvement parameters which are described in MIL-HDBK-217B, "Reliability Prediction of Electronic Equipment". In addition to complementing this document, the attendant handbook describes the overall approach to reliable design, including theoretical, practical and cost considerations. It describes methods for considering such areas as component selection, derating, thermal and environmental design evaluation, redundancy, part improvement and part screening techniques.

The following pages (Section 1.2 and its subsections) provide an introductory overview of reliability engineering techniques, establish the theme for the remainder of the handbook and, in general, identify broad measures which can be taken to implement reliability during design.

1.2 Introduction to Reliability Engineering

An effective reliability engineering program begins with the recognition that the achievement of a high level of actual use reliability is a function of design as well as all life cycle activities. Design establishes the inherent reliability potential of a system, and the transition from the paper design to hardware results in an actual system reliability below this inherent level. Accordingly, its assessment must be approached first via its design characteristics (which establish an upper limit of reliability), and then in conjunction with a series of modifying factors that account for production, operation and maintenance degradation.

Therefore, deliberate and positive measures must be taken during design and development which enhance inherent reliability by forcing the design to be iterated, and minimize degradation by eliminating potential failures and manufacturing flaws prior to production and operational use. Such measures demand that all reliability activities be effectively managed during the entirety of system development. Reliability efforts start with design--selecting the best parts, applying part derating concepts, incorporating screening techniques and/or designing redundancy into the system. It includes both purchasing practices and specifications which insure the procurement of reliable components. It ranges from adequate test methods and assembly processes to effective formal systems for accurately reporting, analyzing and correcting failures which occur during use. Many times, only a little additional effort is needed to assure acceptable field reliability. In contrast, the consequences of unreliability in the field are severe--high cost and excessive maintenance downtime.

1.2.1 Reliability and Life Characteristics

Reliability has been described as "quality in the time dimension". It is classically defined as the probability that an item will perform satisfactorily for a specified period of time under a stated set of use conditions. From a functional point of view, in order for an item to be reliable, it must do more than meet an initial factory performance or quality specification--it must also operate satisfactorily for an acceptable period of time in the field application for which it is intended.

The classical definition of reliability, stated above, stresses four elements, namely: probability, performance requirements, time and use conditions. Probability is that quantitative term which expresses the likelihood of an event's occurrence (or nonoccurrence) as a value between 0 and 1. Performance requirements are those criteria which clearly describe or define what is considered to be satisfactory operation. Time is the measure of that period during which one can expect satisfactory performance. Use conditions are the environmental conditions under which one expects an item to function.

Determining reliability, therefore, involves the understanding of several concepts which relate to these four definitional elements. Among such concepts is that of a failure rate which can vary as a function of age. A failure rate is a measurement of the number of malfunctions occurring per unit of time. In order to show the variation in failure rate, separate consideration is given to three (3) discrete periods when viewing the failure characteristics of a product or item over its life span (and then considering a large sample of its population). These periods are shown in Figure 1-1 and are described below.

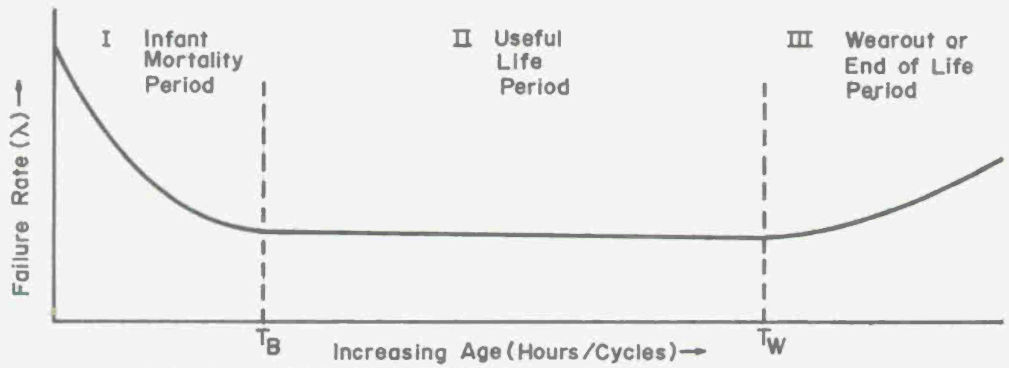

Fig 1-1 LIFE CHARACTERISTIC CURVE (Ref. 1)

I Infant Mortality Period

Initially, the item population exhibits a high failure rate. This failure rate decreases rapidly during this first period (often called the "infant mortality", "burn-in" or debugging period), and stabilizes at an approximate value (at time T_B) when the weak units have died out. It may be caused by a number of things: gross built-in flaws due to faulty workmanship (manufacturing deviations from the design intent),

transportation damage or installation errors. This initial failure rate is unusually pronounced in new equipment. Many manufacturers provide a "burn-in" period for their product, prior to delivery, which helps to eliminate a high portion of the initial failures and assists in establishing a high level of operational reliability. Examples of early failures are:

- Poor welds or seals
- Poor solder joints
- Poor connections
- Dirt or contamination on surfaces or in materials
- Chemical impurities in metal or insulation
- Voids, cracks, thin spots in insulation or protective coatings
- Incorrect positioning of parts

Many of these early failures can be prevented by improving the control over the manufacturing process. Sometimes, improvements in design or materials are required to increase the tolerance for these manufacturing deviations, but fundamentally these failures reflect the "manufacturability" of the component or product and the control of the manufacturing process. Consequently, these early failures would show up during:

- In-process and final tests
- Process audits
- Life tests
- Environmental tests

II Useful Life Period

The item population, after having been burned-in, reaches its lowest failure rate level, which is normally characterized by a relatively constant failure rate, accompanied by negligible or very gradual changes due to wear. This second period (between T_B and T_W as seen in Figure 1-1) is called the useful life period, and is characterized mainly by the occurrence of stress related failures. The exponential failure distribution is widely used as a mathematical model to approximate this time period. This period varies among hardware types, is the interval usually given most weight in design reliability action, and is the most significant period for reliability prediction and assessment activities.

Figure 1-2 shows the interaction of stress and strength relative to the time periods identified in Figure 1-1. Figure 1-2(A) illustrates the distribution of a typical stress/strength density curve for an item having low reliability and/or inadequate design margin. The shaded area indicates that stress exceeds strength a certain percentage of the time, with resultant failure. Note that for items having an inadequate design margin, instantaneous stress frequently exceeds the average strength. This is shown in Figure 1-2(C).

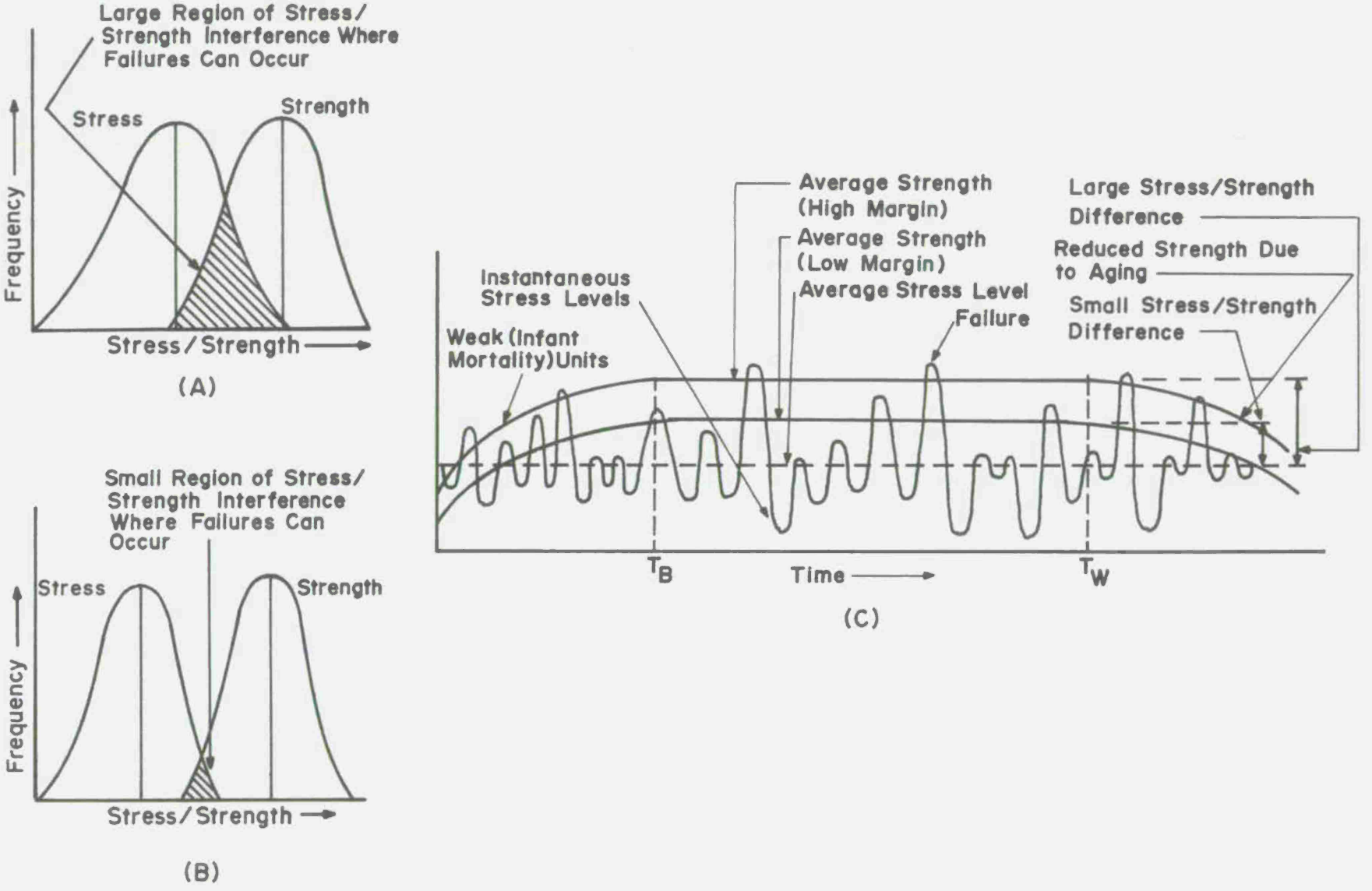

Fig 1-2 STRESS VERSUS STRENGTH DISTRIBUTIONS (Ref 1)

In contrast, Figure 1-2(B) shows the separation of the stress/strength distribution indicative of a high design safety factor (adequate design margin) and high reliability. Occasionally, random increases in the level of a stress or a combination of stresses causes a device to fail. This is also shown in Figure 1-2(C). For electronic devices and components, experience has shown that excessive temperature and voltage levels, either steady state, transient or changing at rapid rates, are the two most destructive stresses. Humidity, vibration, shock and altitude also contribute to the failure of design strength devices.

III Wearout Period

The third and final life period occurs when the item population reaches the point where the failure rate starts to increase noticeably (T_W). This point is identified as the end of useful life or the start of wearout. Beyond this point on the time axis, the failure rate increases rapidly. When the hardware failure rate due to wearout becomes unacceptably high, replacement or repair of the item should be made. Replacement schedules (of critical short-life components) are based on the recognition of this failure rate.

Wearout failures, as shown in Figure 1-1 and 1-2, are due primarily to deterioration of the design strength of the device as a consequence of operation and exposure to environmental fluctuations. Deterioration results from a number of familiar chemical and physical phenomena:

- Corrosion or oxidation
- Insulation breakdown or leakage
- Ionic migration of metals in vacuum or on surfaces
- Frictional wear or fatigue
- Shrinkage and cracking in plastics.

Optimizing reliability involves the consideration of each and all of these three life periods. Early failures must be eliminated by systematic procedures of controlled screening and burn-in tests. Stress related failures must be minimized by providing adequate design margin. Wearout must be eliminated by timely preventive replacement or short-life component parts. Thus, all major factors which influence (and degrade) a system's operational reliability must be addressed during design (using appropriate techniques described later) to optimize and control system reliability.

In order to introduce several additional concepts, consider for the moment that portion of Figure 1-1 denoted as the useful life period. During this time period, reliability is described by means of the single parameter exponential distribution:

$$R(t) = e^{-\lambda t}$$

where:

R(t) is the probability that the item will operate without failure for the time period, t (usually expressed in hours), under stated operating conditions;

e is the base of the natural logarithms, equal to 2.7182...;

λ is the item failure rate (usually expressed in failures per hour), and is a constant for any given set of stress, temperature and quality level conditions. It is determined for parts and components from large scale data collection and/or test programs.

When appropriate values of λ and t are inserted into the above expression, the probability of success (i.e., reliability) is obtained for that time period.

The reciprocal of the failure rate is defined as the mean time between failures (MTBF)

$$MTBF = 1/\lambda$$

The MTBF is primarily a figure of merit by which one hardware item can be compared to another. It is a measure of the failure rate (λ) during the useful life period. The document used to establish failure rates (λ) for the constituent electronic parts (resistors, semiconductors, etc.) used in systems and equipment is MIL-HDBK-217B[2]. A more definitive discussion of MIL-HDBK-217B is given in Section 2.1.3.

Reliability estimates prepared in accordance with MIL-HDBK-217B techniques reflect the inherent (or potential) reliability of a system as defined by its engineering documentation, its stress and safety factors and gross environmental application, manufacturing and quality factors. These estimates are indicative of the upper limit or reliability potential as depicted by the useful life period in Figure 1-1. However, these estimates do not reflect the expected system performance after initial manufacturing and many times do not reflect expected performance when operated and maintained in its actual field environment.

The sections which follow discuss how degradation in reliability can occur during the periods which encompass production and operation of the equipment or system, and how reliability can grow from a degraded level back up to that which approaches the inherent or potential value of the system.

1.2.2 Reliability Degradation

The results of numerous data collection efforts have shown that the reliability of fielded equipment and systems is degraded from three to ten times the potential predicted during design[3]. The transition from a paper design to production to field operations introduces degradation factors which constrain the expected reliability. This section provides a brief discussion of these factors which can be broadly divided into manufacturing and production factors, system operation and maintenance activities.

In order to assess the magnitude of the reliability degradation due to manufacturing, the impact of manufacturing processes (i.e., the process induced defects, the efficiency of conventional manufacturing and quality control inspection, and the effectiveness of reliability screening techniques) must be evaluated. In addition to the latent defects attributable to purchased parts and materials, assembly errors can account for substantial degradation. Assembly errors can be brought about by operator learning, motivational or fatigue factors. Manufacturing and quality control inspections and tests are provided to minimize degradation from these sources and to weed out the more obvious defects. No inspection process can remove all defects which inhabit an item presented for inspection. A certain number of defective items will escape the process, be accepted and be placed in field operation. More importantly, these gross defects are overshadowed by unknown numbers of latent defects, the results of weakened parts, which can fail under the proper conditions of stress--usually during field operation. Factory screening tests are designed to apply a stress of given magnitude over a specified duration to remove these kinds of defects. As is the case with conventional inspection processes, screening tests are not 100% effective.

From the preceding discussion, it is evident that the assessment of reliability degradation due to production involves estimating the number of defects induced during fabrication and assembly processes minus the number removed by conventional quality control tests and inspections. Section 4.2.1 of this handbook provides further details concerning reliability degradation resulting from production processes.

Degradation in reliability also occurs as a result of system operation. Wearout, with aging as the dominant failure mechanism, can shorten or reduce the useful life. Situations also occur in which a military system may be called upon to operate beyond its design capabilities because of an unusual mission requirement or to avoid a ground threat. These situations could cause ill effects to its constituent parts. Operational abuses due to rough handling, extended duty cycles or neglected maintenance can contribute materially to reliability degradation, which eventually results in failure. The degradation can be a result of the interaction of man, machine and environment. The translation of the factors which influence operational reliability degradation into corrective procedures requires a complete analysis of functions performed by man and machine, plus fatigue and/or stress conditions which could degrade operator performance.

Degradation in inherent reliability can also occur as a result of maintenance activities. Studies[3] have shown that excessive handling brought about by frequent preventive maintenance or poorly executed corrective maintenance (e.g., installation errors) have degraded system reliability. Several trends in system design have reduced the need to perform adjustments or make continual measurements to verify peak performance. Extensive replacement of analog with digital circuitry, inclusion of more built-in test equipment and use of fault tolerant circuitry are indicative of these trends. These factors, along with greater awareness of the cost of maintenance, have brought changes for ease of maintenance whose by-product has been increased system reliability. In spite of these trends, the maintenance technician remains a primary cause of reliability degradation. The effects of poorly trained, poorly supported or poorly motivated maintenance technicians on reliability degradation require careful assessment and quantification.

1.2.3 Reliability Growth

Reliability growth represents the resultant action taken to hasten a hardware item toward its reliability potential either during development or during subsequent manufacturing or operation. During early development, the achieved reliability of a newly fabricated item, or an off-the-board prototype, is much lower than its predicted reliability. This is due to initial design and engineering deficiencies as well as manufacturing flaws. The reliability growth process, when formalized and applied as an engineering discipline, allows management to exercise control, allocate resources and maintain visibility into activities designed to achieve a mature system prior to full production or field use.

The basic concepts associated with a reliability growth process and its application to newly fabricated hardware involve consideration of hardware test, failure, correction and retest activities. Specifically, reliability growth is usually an iterative test-fail-correct process. There are three essential elements involved in achieving reliability growth, namely:

(1) Detection and analysis of hardware failures,

(2) Feedback and redesign of problem areas,

(3) Implementation of corrective action and retest.

The rate at which hardware reliability grows is dependent on how rapidly these three elements can be accomplished and, more importantly, how well the corrective action solves the problem identified. During early development and test activities, the achieved reliability (or MTBF) is well below that predicted on the basis of design analyses and analytical predictions. As development and test efforts progress and problem areas become resolved, measured reliability values approach the inherent (design based) value. Figure 1-3 depicts this process.

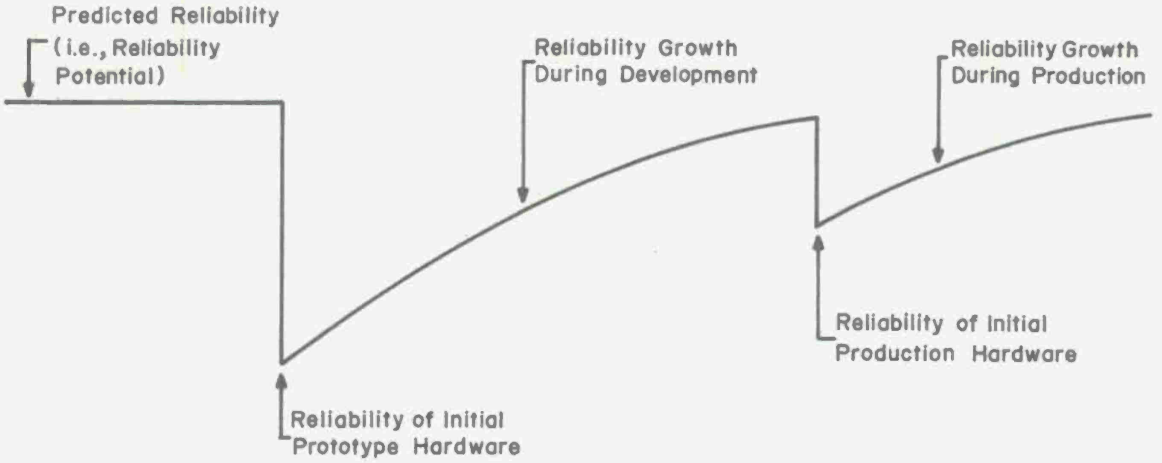

Fig 1-3 RELIABILITY GROWTH PROCESS DURING DESIGN AND DEVELOPMENT

Figure 1-3 also shows that a decrease in reliability occurs at the onset of production. This is primarily due to workmanship errors resulting from unfamiliar operations, process discrepancies and quality oversights which drive reliability below expected levels. As production continues and skill increases, measured reliability again approaches the inherent value. Later sections of this handbook will describe techniques by which reliability growth can be modeled and applied to the development of Air Force Systems.

1.3 Organization of the Handbook

The handbook is comprised of three (3) major sections containing introductory material, background information and guidelines for reliable design. Definitions and an annotated bibliography are also included. The following summarizes its contents:

Reliability Theory and Application (Section 2)

Provides the designer with an overview of the more significant reliability concepts, formulae and evaluation techniques used by reliability engineers in assuring that reliability is designed into the system.

Airborne Systems (Section 3)

Identifies the typical avionics systems and describes specific equipment classes, their complexity and their approximate reliability levels. The intent is to show, in general, the relationship between performance, complexity and reliability.

Reliability Design Data (Section 4)

Comprises the main body of this handbook and provides guidelines for reliable design covering component selection, derating, design simplification, environmental resistance, redundancy, and tolerance evaluation. In addition, basic design approaches to help minimize reliability degradation due to production and maintenance are also covered. Design-to-cost guidelines are provided in this section.

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2. Military Standardization Handbook 217B (DoD), "Reliability Prediction of Electronic Equipment," 20 September 1974.

3. Research Study of Radar Reliability and Its Impact on Life Cycle Costs for the APQ-113, -114, -120 and -144 Radar Systems, General Electric Company, Aerospace Electronic Systems Department, Utica, New York, August 1972.

SECTION 2

RELIABILITY THEORY AND APPLICATION

SECTION 2

RELIABILITY THEORY AND APPLICATION

2.1 Basic Reliability Theory

The previous section of this handbook introduced fundamental reliability engineering concepts. This section expands upon those concepts to provide a more detailed understanding of how design activities can influence hardware reliability. The subsections which follow treat basic reliability theory, management for reliability and reliability evaluation tools used during system development.

2.1.1 Exponential Failure Model

The life characteristic curve shown in Section 1 (Figure 1-1) can be further defined by three failure components which predominate during the three periods of an item's life. Figure 2-1 illustrates these components in terms of an equipment hazard rate, z(t). The hazard rate can be simply stated as the conditional probability of failure and will be defined later. The failure components shown in Figure 2-1 include:

(1) Early Failure--due to design and quality-related manufacturing flaws and which have a decreasing hazard rate.

(2) Stress Related Failure--due to application stresses and which have a constant hazard rate.

(3) Wearout Failures--due to aging and/or deterioration and which have an increasing hazard rate.

Examination of Figure 2-1 indicates that:

(1) The infant mortality period is characterized by a high but rapidly decreasing hazard rate that is comprised of:

  (a) a high quality failure component
  (b) a constant stress related failure component
  (c) a low wearout failure component.

(2) The useful life period is characterized by a constant hazard rate that is comprised of:

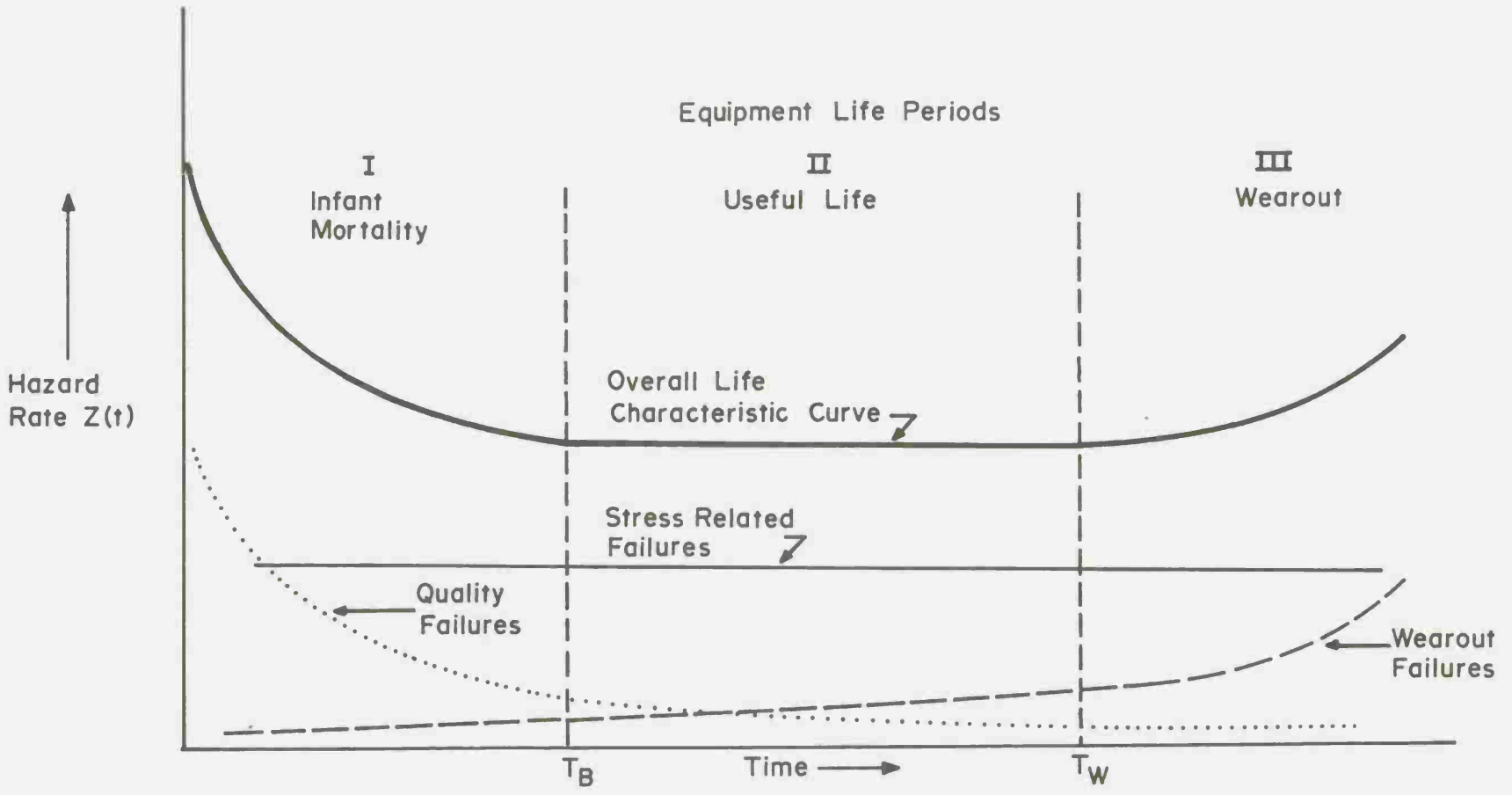


Fig 2-1 COMPONENTS OF FAILURE

(a) a low (and decreasing) quality failure component
(b) a constant stress related failure component
(c) a low (but increasing) wearout failure component.

Note: The combination of all three components results in a constant hazard rate because the decreasing quality failures and increasing wearout failures tend to offset each other, and because the stress related failures exhibit a relatively large amplitude.

(3) The wearout period is characterized by an increasing hazard rate that is comprised of:

(a) a negligible quality failure component
(b) a constant stress related failure component
(c) an initially low but rapidly increasing wearout failure component.

The general approach to reliability for electronic systems is to minimize early failures by emphasizing factory test and inspection and preventing wearout failures by replacing short life parts. Consequently, the useful life period characterized by stress related failures is the most important period, and the one to which design action is primarily addressed.

Figure 2-1 illustrates that during the useful life period the hazard rate is constant. A constant hazard (or failure) rate is described by the exponential failure distribution. Thus, the exponential failure model reflects the fact that the item must represent a mature design whose failure rate, in general, is primarily comprised of stress related failures. This means that early failures have been minimized, and wear-out is not noticeable or is beyond the period of concern. The magnitude of this failure rate is directly related to the stress/strength ratio of the item.

The exponential model can be derived from the basic notions of probability[1]. When a fixed number, N_o, of components are repeatedly tested, there will be, after a time t, N_s components which survive the test and N_f components which fail. The reliability or probability of survival is at any time t during the test:

$$R(t) = \frac{N_s}{N_o} = \frac{N_s}{(N_s+N_f)}$$

Since $N_s = N_o - N_f$; reliability can be written:

$$R(t) = \frac{N_o-N_f}{N_o} = 1 - \frac{N_f}{N_o} = 1 - F(t)$$

and

$$\frac{dR}{dt} = \frac{-1}{N_o}\frac{dN_f}{dt} = -f(t)_i$$

where

$f(t)_i$ = the failure density function, i.e., the probability that a failure will occur in the next time increment dt.

The hazard rate z(t) is defined as the ratio of the fractional failure rate to the fractional surviving quantity, that is, number of the original population still operating at time t, or simply the conditional probability of failure[2].

$$z(t) = \frac{f(t)}{R(t)} = \frac{f(t)}{1-F(t)}$$

$$= \frac{f(t)}{1 - \int_0^t f(t)dt}$$

for the exponential distribution

$$f(t) = \lambda\, e^{-\lambda t}$$

$$z(t) = \lambda$$

In general, it can be assumed that the hazard rate of electronic elements and systems remains constant over practical intervals of time, and that $z(t)_i = \lambda_i$. Hence, λ_i, a constant, represents the expected number of random failures per unit of operating time of the i^{th} element, i.e., the failure rate. Thus, when a constant failure rate can be assumed:

$$z(t)_i = \lambda_i = \frac{f(t)_i}{R(t)_i} = \frac{\frac{-dR(t)_i}{dt}}{R(t)_i}$$

Solving this differential equation for $R(t)_i$ gives the exponential distribution function commonly used in reliability prediction:

$$R(t)_i = e^{-\lambda_i t}$$

Also, the mean time to failure can be determined by:

$$MTBF = \int_0^\infty R(t)dt,$$

so that, when a constant failure rate λ_i can be assumed:

$$MTBF_i = \int_0^\infty e^{-\lambda_i t} dt = \frac{1}{\lambda_i}$$

The above expressions for $R(t)_i$ and $MTBF_i$ are the basic mathematical relationships used in reliability prediction. It must be emphasized, however, that these expressions were derived based on the fundamental assumption that the failure rate of the item under consideration is a constant.

The emphasis on the exponential distribution in reliability work makes it worthwhile to discuss the use of this function as a failure-probability model. The mechanism underlying the exponential reliability function is that the hazard rate (or the conditional probability of failure in an interval given survival at the beginning of the interval) is independent of the accumulated life.

The use of this type of "failure law" for complex systems is judged applicable because of the many forces that can act upon the item and produce failure. As stated previously, the stress/strength relationship and varying environmental conditions result in effectively random failures.

Another factor for assuming the exponential distribution in long-life complex systems is the so-called "approach to a stable state," wherein the system hazard rate is effectively constant regardless of the failure pattern of individual parts. This state results from the mixing of part ages when failed elements in the system are replaced or repaired. Over a period of time, the system hazard rate oscillates, but this cyclic movement diminishes in time and approaches a stable state with a constant hazard rate.

A third argument for assuming the exponential distribution is that the exponential can be used as an approximation of some other function over a particular interval of time for which the true hazard rate is essentially constant.

Subsequent paragraphs in Section 2.1 which describe system and part failure models used for predicting R are based on the assumption that the constant hazard rate is applicable and that the item is operating within the flat portion of its characteristic curve.

2.1.2 System Modeling Concepts

To evaluate the reliability of systems and equipment, a method is needed to reflect the reliability connectivity of the many part types having different stress-determined failure rates that would normally make up a complex equipment. This is accomplished by establishing a relationship between equipment reliability and individual part/item failure rates.

Prior to discussing these relationships, it would be useful to discuss system reliability objectives first. For military systems, reliability must be evaluated from the following three separate, but related, standpoints:

(1) Reliability as it impacts personnel safety.

(2) Reliability as it impacts mission success.

(3) Reliability as it impacts unscheduled maintenance or logistic factors.

Each of these basic reliability considerations bears a relationship to the failure modes and mechanisms which impact safety, mission success and unscheduled maintenance. Figures 2-2a and 2-2b provide an example

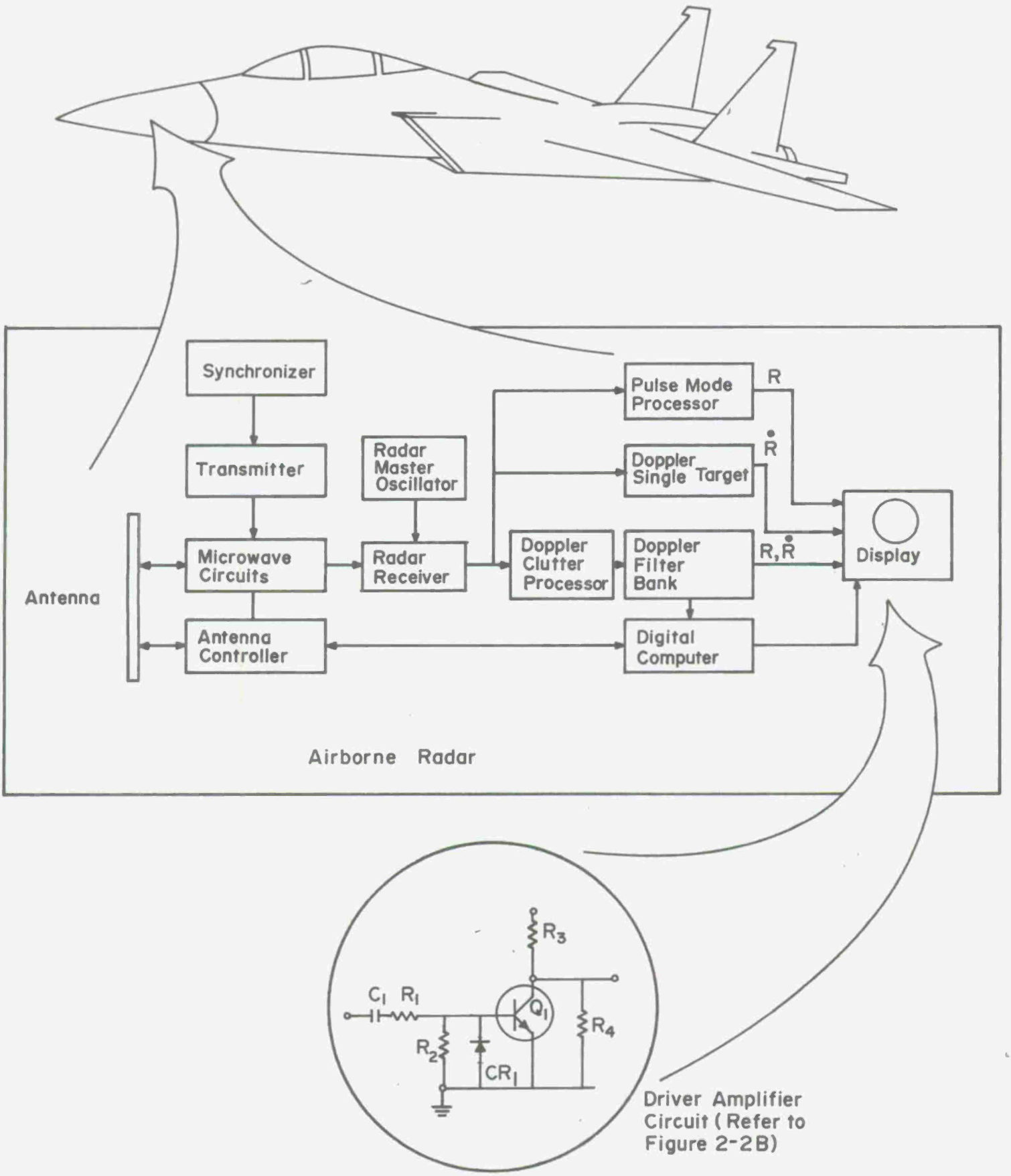
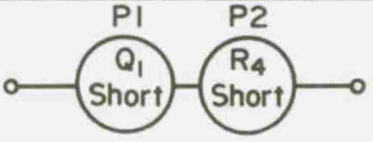


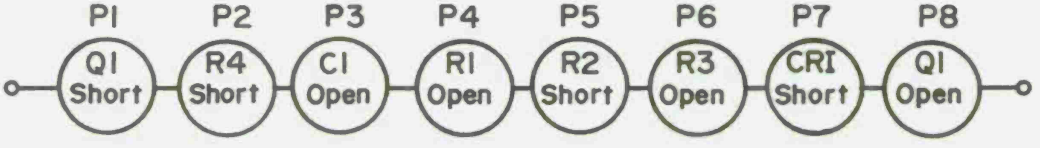
Fig 2-2A RELATIONSHIP BETWEEN MISSION ACCOMPLISHMENT EQUIPMENT PERFORMANCE AND CIRCUIT RELIABILITY

Part	Failure Mode	Failure Mode Impact		
		Safety	Mission	Unscheduled Maintenance
Q1	Short	X	X	X
R4	Short	X	X	X
C1	Open		X	X
R1	Open		X	X
R2	Short		X	X
R3	Open		X	X
CR1	Short		X	X
Q1	Open		X	X
C1	Short			X
R1	Short			X
R2	Open			X
R3	Short			X
R4	Open			X
CR1	Open			X

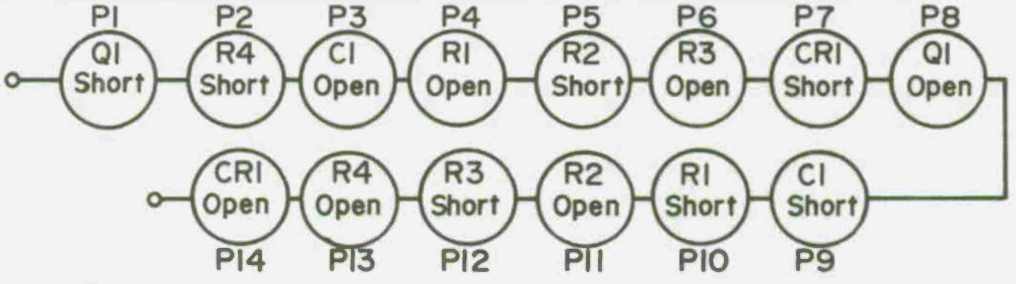
Failure Mode Matrix



Failure Modes Whose Probability of Occurrence Impacts Safety - $R = 1-(P1)(P2)$



Failure Modes Whose Probability of Occurrence Impacts Mission Success - $R_M = 1-(P1).....(P8)$



Failure Modes Whose Probability of Occurence Impacts Unscheduled Maintenance - $R_U = 1-(P1).....(P14)$

Safety, Mission, & Unscheduled Maintenance Reliability

Fig 2-2B RELATIONSHIP BETWEEN MISSION ACCOMPLISHMENT, PERFORMANCE, & CIRCUIT RELIABILITY (CONT.)

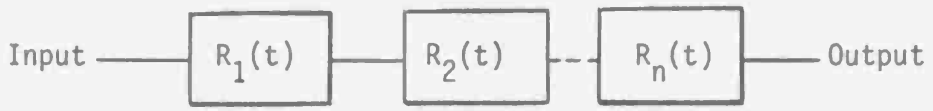
of how these concepts apply even at the circuit level of complexity. Figure 2-2a shows a typical driver circuit within the system architecture of a typical airborne radar. Figure 2-2b indicates the reliability implications of various failure modes in this circuit.

Figure 2-2b identifies those parts whose specific failure modes would result in a safety hazard. Similarly, the functioning of those parts whose failure modes would cause mission abort are indicated. Finally, it is indicated that unscheduled maintenance depends on the proper functioning of all elements. For critical military systems, these considerations are defined in contractual documents and are usually specified quantitatively in terms of probability of success (reliability) or mean-time-between-failure (MTBF), as applicable.

Regardless of which of the particular safety, mission or unscheduled maintenance considerations are being addressed, the rules for reliability connectivity are applicable. These rules imply that failures are stress related and the exponential failure distribution is applicable.

Each of the diagrams shown in Figure 2-2b represents a serial reliability configuration. Failure of any one part in the series would result in failure of the equipment. Further, it may be assumed that failure of any part would occur independently of the operation of other components.

In general, the serial equipment configuration may be represented by the following block diagram:



Reliability of the series configuration is the product of the reliabilities of the individual blocks:

$$R_s(t) = R_1(t) \cdot R_2(t) \cdots R_i(t) \cdots R_n(t)$$

where

$R_s(t)$ is the series reliability, and $R_i(t)$ is the reliability of the "i^{th}" block for the time "t".

The concept of constant failure rate allows the computation of system reliability as a function of the reliability of parts and components to be accomplished in the following manner:

$$R(t) = \prod_{i=1}^{n} e^{-\lambda_i t} = e^{-\lambda_i t} \cdot e^{-\lambda_2 t} \cdots e^{-\lambda_n t}$$

This can be simplified:

$$R(t) = e^{-(\lambda_1 t + \lambda_2 t + \ldots + \lambda_n t)} = e^{-(\lambda_1 + \lambda_2 + \ldots + \lambda_n)t}$$

The general form of this expression can be written:

$$R(t) = \exp\left[-t \sum_{i=1}^{n} \lambda_i\right]$$

Another important relationship is obtained by considering the j^{th} subsystem failure rate (λ_j) to be equal to the sum of the individual failure rates of n independent elements of the subsystems such that:

$$\lambda_j = \sum_{i=1}^{n} \lambda_i$$

Revising the MTBF formulas to refer to the system rather than an individual element gives the mean-time-between-failures of the system as:

$$MTBF = \frac{1}{\lambda_j} = \frac{1}{\sum_{i=1}^{n} \lambda_i}$$

Successive estimates of the j^{th} subsystem failure rate can be made by combining lower level failure rates using

$$\lambda_j = \sum_{i=1}^{n} \lambda_{ij} \qquad (j = 1, \ldots m)$$

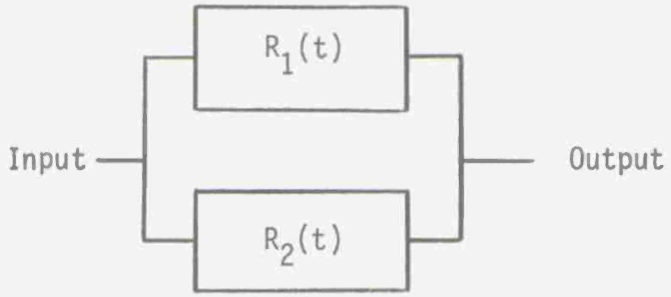
where

λ_{ij} = the failure rate of the i^{th} component in the j^{th} level subsystem

λ_j = failure rate of j^{th} level subsystem.

Equipment reliability is therefore a combination of the failure rates of the parts from which the equipment is built. As previously stated, these part failure rates can combine in series so that if any part fails, the equipment fails. They can also combine in parallel so that when a part fails there is another part to perform the same function.

The more complex configuration would consist of equipment items or parts operating both in series and parallel combinations--together with the various permutations. A parallel configuration accounts for the fact that alternate part or item configurations can be designed to insure equipment success. A two element parallel reliability configuration is represented by the following block diagram:



In order to evaluate the reliability of parallel configurations, consider, for the moment, that a reliability value (for any configuration) is synonomous with probability (i.e., probability of successful operation) and can take on values ranging between 0 and 1. If we represent the reliability by the symbol $\underline{R}$ and its complement (i.e., unreliability) by the symbol Q, then from the fundamental notion of probability,

$$R + Q = 1$$

$$R = 1 - Q$$

From the above, it can be seen that a probability can be associated with successful operation (reliability) as well as with failure (unreliability). For a single block (on the block diagram), the above relationship is valid. However, for the two element parallel reliability configuration shown, two paths for successful operation exist and the above relationship becomes:

$$(R_1 + Q_1)(R_2 + Q_2) = 1$$

Assuming that $R_1 = R_2$ and $Q_1 = Q_2$ (i.e., the blocks are identical), this can be rewritten as

$$(R + Q)^2 = 1$$

Upon expansion, this becomes

$$R^2 + 2RQ + Q^2 = 1$$

Recall that reliability represents the probability of successful operation. This condition is represented by the first two terms of the above expression. Thus, the reliability of the parallel configuration can be represented by:

$$R_p = R^2 + 2RQ$$

Note that either both branches are operating successfully (the R^2 term), or one has failed while the other operates successfully (the 2RQ term).

Substituting the value of $R = 1 - Q$ into the above expression, we obtain

$$R_p = (1-Q)^2 + 2(1-Q)Q$$

$$= 1 - 2Q + Q^2 + 2Q - 2Q^2$$

$$R_p = 1 - Q^2$$

To obtain an expression in terms of reliability only, the substitution $Q = 1 - R$ can be made which yields:

$$R_p = 1 - (1-R)(1-R)$$

Returning to the more general case where $R_1 \neq R_2$, this may be expressed:

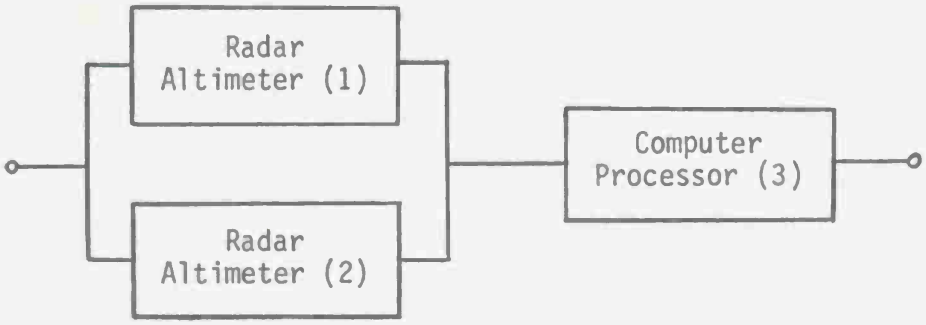
$$R_p = 1 - (1-R_1)(1-R_2)$$

By similar reasoning, it can be shown that, for n blocks connected in a parallel reliability configuration, the reliability of the configuration can be expressed by:

$$R_p(t) = 1 - (1-R_1)(1-R_2) \ldots (1-R_n)$$

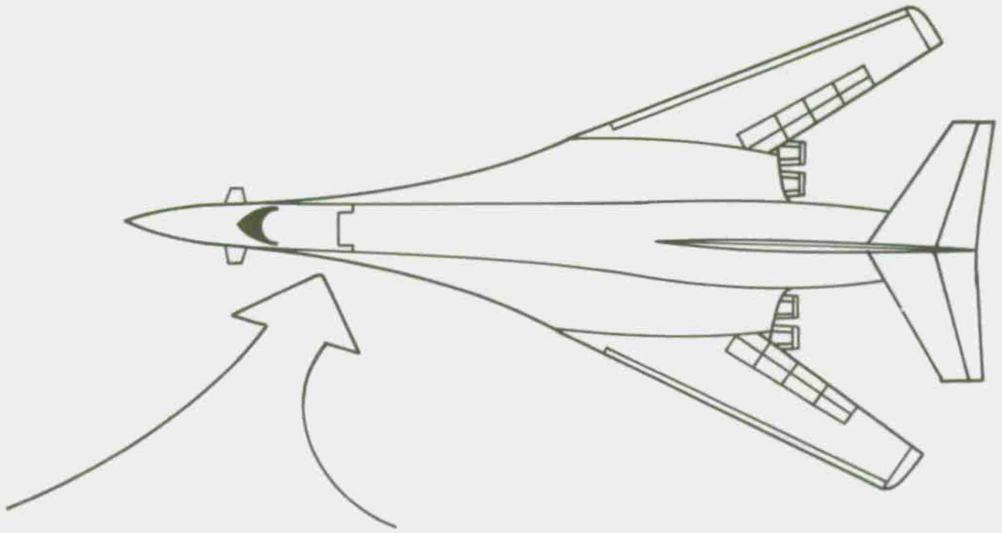
The series and parallel reliability configurations (and combinations of these), as described above, represent the basic concepts involved in estimating the reliability of complex equipment. A further elaboration of parallel reliability configurations (redundancy techniques) is given in Section 4.1.4 of this handbook.

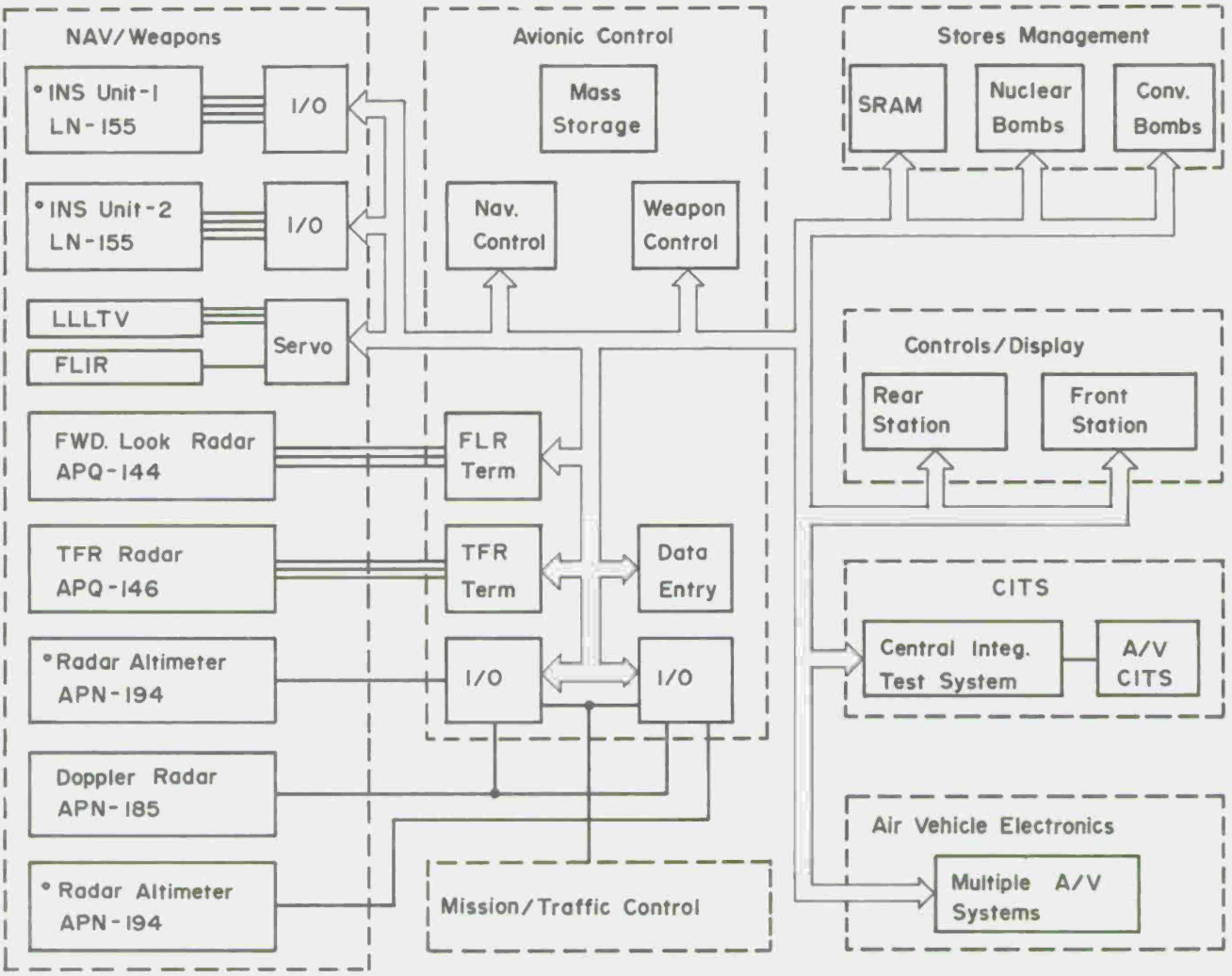
The serial and parallel reliability concepts presented in the preceding paragraphs establish the mathematical framework for the reliability connectivity of various elements. Their application can be illustrated to show both the benefits and penalties of redundancy when considering safety, mission and unscheduled maintenance reliability. For example, a simplified equipment composed of three functional elements (as shown below) can be used to illustrate the technique.



Elements 1 and 2 are identical and represent one form of functional redundancy operating in series with Element 3. A practical example of this configuration can be taken from the B-1 avionics suite. Referring to Figure 2-3, it can be seen that redundant Inertial Navigation Systems (INS) and/or Radar Altimeters are associated with Elements 1 and 2. Element 3 represents the computer processor, which uses the output of each element to arrive at a substantially more accurate position fix or altitude profile control.

Reliability block diagrams can be defined corresponding to non-redundant serial, safety, mission and unscheduled maintenance reliability. As described initially in this section, the reliability block diagrams depict only those functional elements which must operate properly to meet that particular reliability requirement. Figure 2-4 depicts the





• Note Presence Of Redundant Internal Navigation and Radar Altimeter Systems

Fig 2-3 BLOCK DIAGRAM OF B-1 INTEGRATED OFFENSIVE AVIONIC SYSTEMS UNDER COMPUTER CONTROL

$R_{Serial} = R_1 \cdot R_2 \cdots R_n$

where

$R_n = e^{-\lambda t}$

$MTBF = \frac{1}{\lambda}$

$R_{Parallel} = 1 - (1-R)(1-R)$

$= 2R - R^2$

$R_1 = 0.85$

$R_2 = 0.85$

$R_3 = 0.99$

$t = 100$ hours

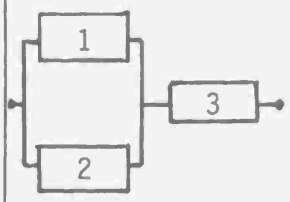
Reliability Requirement	Reliability Block Diagram	Calculated Values
1. Serial (Nonredundant) Reliability		$R = R_1 R_3 = 0.84$ MTBF = 575 hrs
2. Safety (or Mission) Reliability		$R = 2\left[R_1 - R_1^2\right] R_3$ $= 0.97$ Equivalent MTBF = 3030 hrs
3. Unscheduled Maintenance Reliability		$R = R_1 R_2 R_3 = 0.72$ MTBF = 298 hrs

Fig. 2-4 CALCULATIONS FOR SYSTEM RELIABILITY

various block diagrams, reliability formulas and typical values corresponding to these requirements. Figure 2-4 indicates that the use of redundancy provides a significant increase in safety and mission reliability numerics above that of a serial or nonredundant configuration; however, it imposes a penalty by adding an additional serial element in the unscheduled maintenance chain.

2.1.3 Part Failure Modeling

As indicated previously, prediction is an integral task of reliability development programs. The basic concept which underlies reliability prediction and the calculation of reliability numerics is that system failure is a reflection of part failure. Therefore, a method for estimating part failure rates is needed. The most direct approach to estimating part failure rates involves the use of large scale data collection efforts to obtain the relationships (i.e., models) between engineering and reliability variables. This approach utilizes controlled test data to:

(a) derive relationships between design and generic reliability factors, and

(b) develop factors for adjusting the reliability to estimate field reliability when considering application conditions.

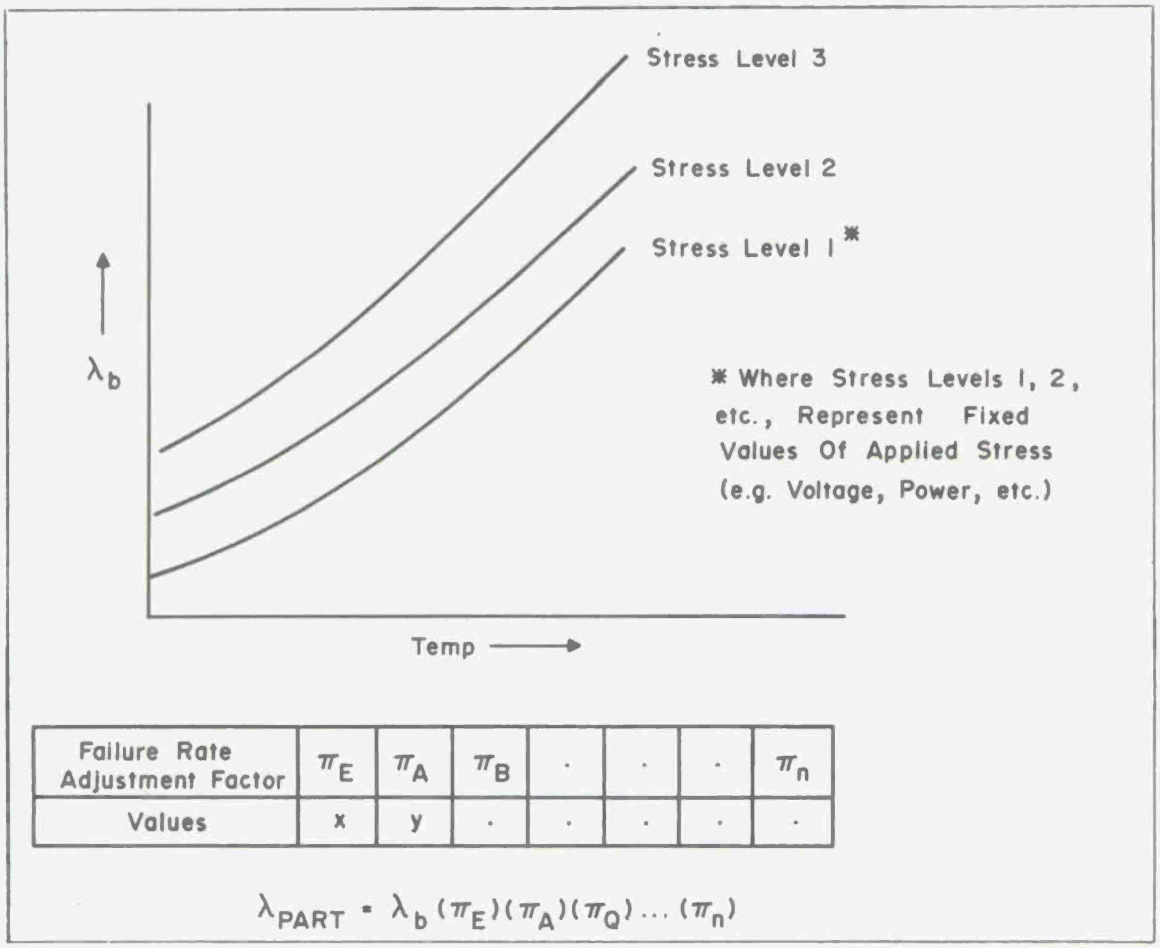
These data have been reduced through physics-of-failure techniques and are included in MIL-HDBK-217B[3] in a form suitable for estimating stress-related failure rates. MIL-HDBK-217B provides guidance during design and allows individual part failure rates to be combined within a suitable system reliability model (see Section 2.1.2) to arrive at an estimate of system reliability.

Part failure models (see Figure 2-5) vary with different part types: however, their general form is:

$$\lambda_{part} = (\lambda_b)(\pi_E)(\pi_A)(\pi_Q) \ldots (\pi_n)$$

where:

λ_{part} is the total part failure rate.



Failure Rate Adjustment Factor	π_E	π_A	π_B	.	.	.	π_n
Values	x	y	.	.	.	.	.

$$\lambda_{PART} = \lambda_b (\pi_E)(\pi_A)(\pi_Q) \ldots (\pi_n)$$

Fig 2-5 PART FAILURE MODEL (Conceptual)

λ_b is the base failure rate. The value is obtained from reduced part test data for each generic part category, where the data is generally presented in the form of failure rate versus normalized stress and temperature factors. The part's primary load stress factor and its factor of safety are reflected in this basic failure rate value. As shown in Figure 2-5, the value of λ_b is generally determined by the anticipated stress level (e.g., power and voltage) at the expected operating temperature. These values of applied stress (relative to the part's rated stress) represent the variables over which design control can be exercised and which influence the item's ultimate reliability.

π_E is the environmental adjustment factor which accounts for the influences of environments other than temperature, and is related to the military operating condition (vibration, humidity, etc.) under which the item must perform. These environmental classes have been defined in MIL-HDBK-217B. Table 2-1 defines each class in terms of its nominal environmental conditions.[3] Depending upon the specific part type and style, the value of π_E may vary from 0.2 up to 120. The missile launch environment is usually the most severe and generally dictates the highest value of π_E. Values of π_E for microelectronic devices have been added to Table 2-1 to characterize this range for a particular part type.

π_A is the application adjustment factor. This factor depends on the application of the part, and takes into account secondary stress and application factors that are considered to be "reliability-significant".

π_Q is the quality adjustment factor used to account for the degree of manufacturing control with which the part was fabricated and tested prior to its shipment to the user. Many parts are covered by specifications which have several quality levels. Table 2-2 identifies parts with multilevel quality specifications.[3] Table 2-3 shows actual values of π_Q for the various quality levels for microelectronics and discrete transistors.[3]

π_n is the symbol for a number of additional adjustment factors which account for cyclic effects, construction class and other factors that modify failure rate.

The data used as the basis to develop MIL-HDBK-217B consisted of both controlled test data and field data. The controller test data directly related stress/strength variables on a wide variety of parts and was suitable to establish the base failure rates (λ_b).

Base failure rates, in general, have been established from tests conducted under accelerated stress conditions which speed up the aging process. Stress levels were defined, time to failure data was recorded and all failure modes were identified. Part failure rates derived under accelerated stress conditions were then converted to normal operating

Table 2-1 ENVIRONMENTAL SYMBOL IDENTIFICATION AND DESCRIPTION

Environment	π_E Symbol	Nominal Environmental Conditions	π_E * Value
Ground, Benign	G_B	Nearly zero environmental stress with optimum engineering operation and maintenance.	0.2
Space, Flight	S_F	Earth orbital. Approaches Ground, Benign conditions without access for maintenance. Vehicle neither under powered flight nor in atmospheric re-entry.	0.2
Ground, Fixed	G_F	Conditions less than ideal to include installation in permanent racks with adequate cooling air, maintenance by military personnel and possible installation in unheated buildings.	1.0
Ground, Mobile (and Portable)	G_M	Conditions more severe than those for G_F; mostly for vibration and shock. Cooling air supply may also be more limited, and maintenance less uniform.	4.0
Naval, Sheltered	N_S	Surface ship conditions similar to G_F but subject to occasional high shock and vibration.	4.0
Naval, Unsheltered	N_U	Nominal surface shipborne conditions but with repetitive high levels of shock and vibration.	5.0
Airborne, Inhabited	A_I	Typical cockpit conditions without environmental extremes of pressure, temperature, shock and vibration.	4.0
Airborne, Uninhabited	A_U	Bomb-bay, tail, or wing installations where extreme pressure, temperature and vibration cycling may be aggravated by contamination from oil, hybraulic fluid, and engine exhaust. Classes I and Ia equipment of MIL-E-5400 should not be used in this environment.	6.0
Missile, Launch	M_L	Severe conditions of noise, vibration, and other environments related to missile, launch and space vehicle boost into orbit, vehicle re-entry and landing by parachute. Conditions may also apply to installation near main rocket engines during launch operations.	10.0

*Values for monolithic microelectronic devices.

Table 2-2 PARTS WITH MULTI-LEVEL QUALITY SPECIFICATIONS

Part	Quality Designators
Microelectronics	A,B,B-1,B-2,C
Discrete Semiconductors	JANTXV,JANTX,JAN
Capacitors, Established Reliability (ER)	L,M,P,R,S
Resistors, Established Reliability (ER)	M,P,R,S

Table 2-3 π_Q - QUALITY FACTORS

Microelectronic Quality Factors		
Quality Level or Screen Class	Description	π_Q
A	MIL-M-38510, Class A (JAN)	1
B	MIL-M-35810, Class B (JAN)	2
B-1	MIL-STD-883, Method 5004, Class B	5
B-2	Vendor Equivalent of MIL-STD-883, Method 5004, Class B	10
C	MIL-M-38510, Class C (JAN)	16
D	Commercial (or non-MIL STD) part, with no screening beyond the manufacturer's regular quality assurance practices. The indicated π_Q value represents an average for all grades of commercial parts.	150
Transistor Quality Factors		
JANTXV	Values of π_Q shown are applicable to MIL-S-19500 transistor covering linear, logic switching and high frequency applications.	0.2
JANTX		0.4
JAN		2.0
LOWER		10.0

conditions through knowledge of the test acceleration factors. Acceleration factors were determined through detailed analyses of accelerated test failures involving physics-of-failure studies to determine mechanisms of failure.

The aging process has been characterized via rate process models, attributed to Arrhenius and Eyring,[4] that are a result of both empirical data and theoretical considerations. These rate process models form the basis of physics-of-failure and accelerated test techniques and provide a relationship between stress (electrical and thermal), time and failure rate. The Arrhenius model takes the following general form.

$$\lambda_b = K_1 e^{-c_1/T}$$

K = a constant

c = a constant depending on the activation energy of the individual part type failure mechanism

T = absolute temperature in ^{o}K.

The Eyring model includes an additional temperature factor (T):

$$\lambda_b = K_2 T e^{-c_2/T}$$

The individual constants are, of course, different in value from those of the Arrhenius model.

Neither of these relationships have been proven to be exact models of the time-stress combination with respect to failure rates. They are merely approximations, useful in conjunction with a certain set of conditions.

Although laboratory controlled test data provide value information as to the upper limit or potential reliability of parts, application factors and the use environment prevent realization of this potential. Field data collection and analysis efforts have indicated part failure rates well above those determined from laboratory testing. To account for the adverse influence of the application environment and to align the base failure rate (λ_b) with field experience, a series of π factors, as previously defined, have been developed to account for specific

production, operation and maintenance and application environment stress factors.

MIL-HDBK-217B completely describes failure rate models, failure rate data and adjustment factors to be used in estimating the failure rate for the individual generic part types. Table 2-4 presents a tabulation of several models, their base failure rates (λ_b), associated π factors and failure rate values for several representative part types. The specific procedures for deriving the failure rates differ according to part class and type.

Table 2-4 REPRESENTATIVE PART FAILURE RATE CALCULATIONS

Factors / Model	Values									
	λ_b	π_E	π_Q	π_L	π_{T2}	C_1	C_2	π_R	π_{cv}	λ_p ($\times 10^{-6}$)
Monolithic Bipolar Microelectronic Device $\lambda_p = (\pi_L)(\pi_Q)(C_1\pi_T + C_2\pi_E)$		6.0	5.0	1.0	1.9	0.006	0.002			0.115
Fixed Resistor $\lambda_p = \lambda_b(\pi_E)(\pi_R)(\pi_Q)$	0.0015	8.0	5.0					1.6		0.096
Fixed Capacitor $\lambda_p = \lambda_b(\pi_E)(\pi_{cv})(\pi_Q)$	0.003	24.0	1.0						2.0	0.144

2.2 Managing for Reliability

Studies have shown that for complex avionics systems, the attainment of reliability goals during the development phase has not guaranteed achievement of the same reliability level in the field. Typically, reliability has been found to be degraded by a factor ranging from 3 to 10 during operation and maintenance phases following production. This is due to many factors among which are:

(a) Lack of an effective R&M program

Depth, time and sophistication of R&M efforts during equipment development will significantly impact the reliability achieved in the field.

(b) Imperfect maintenance

Generally, all maintenance actions are reported; hence, actions due to false alarms, secondary failures, maintenance induced failures and adjustments are reflected in the field reliability numeric.

(c) Inaccurate accounting of operating time

Field reliability reflects the ratio of total operating hours to number of maintenance actions. Many times operating time estimates are based on "on-line" operating time only. If based on total operating time (i.e., check out time and operating time), the field reliability will much more closely approximate the reliability demonstrated during development.

As indicated in Section 1.2, achievement of high field reliability is the result of good management. A reliability program must be planned and implemented during development. A control system must be established that includes provisions for:

(a) Accurately predicting and analyzing reliability by developing and applying a reliability model that accounts for design, production and field application factors.

(b) Forcing out defects through a strong aggressive reliability growth program.

(c) Simulating field conditions in R&M performance and demonstration tests.

In general, management and control of system reliability must be based on a recognition of the system's life cycle beginning at concept, extending through design and production and ending at removal of the system from the inventory. The ultimate objective of the management effort is to achieve acceptable field reliability. Thus, the achievement of an acceptable field reliability for any given system involves numerous tasks which must occur prior to field use. Figure 2-6 depicts

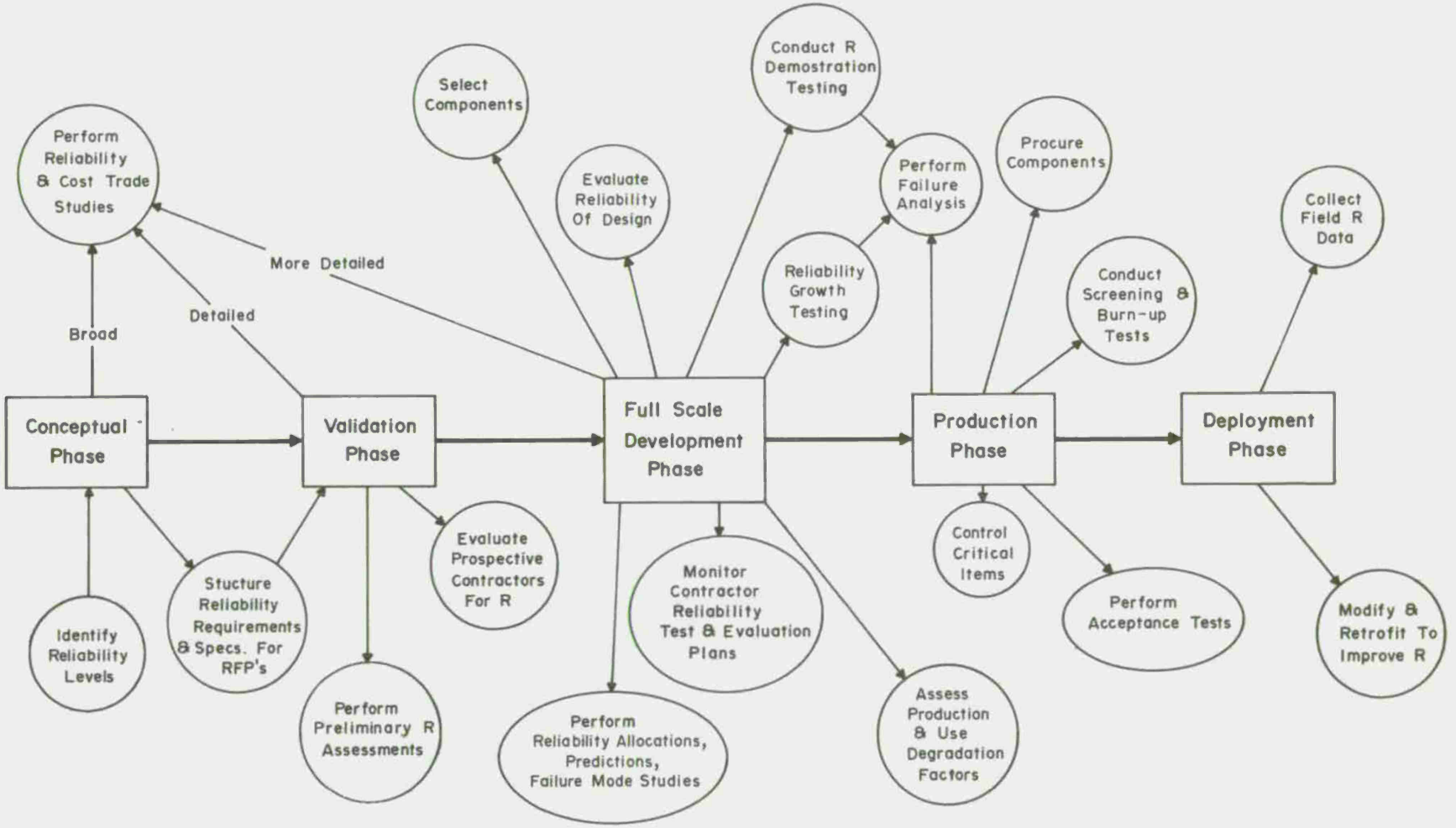


Fig. 2-6 RELIABILITY LIFE CYCLE ACTIVITIES

some of the activities which must be structured, scheduled and implemented in order that field reliability objectives are met, and which are keyed to hardware development milestones. They represent an approach to a well rounded reliability engineering program. Shown are both government and contractor efforts to:

(1) Initiate reliability activities in the conceptual phase and early validation phases of development.

(2) Perform system analysis involving tradeoff decisions beginning during the later conceptual phase and continuing through the development phase.

(3) Structure RFP requirements which cover reliability, its growth and demonstration test requirements.

(4) Evaluate and select contractor(s).

(5) Monitor contractor performance during development.

(6) Perform reliability allocations, predictions and failure mode and effects analyses.

(7) Conduct growth and demonstration tests.

(8) Select and procure component parts.

(9) Assess degradation factors for production and field use.

(10) Collect field data to measure actual field reliability.

Of particular interest to the design engineer is the set of reliability activities which must occur during system development. Standard reliability program provisions are fully defined in AFSCP-800-XX, "Reliability and Maintainability (R&M) Management Guide". The document explains how to insure appropriate levels of reliability and maintainability over the life cycle of systems and equipment through effective management actions by staff, program office and contractor personnel.

Figure 2-7, taken from AFSCP-800-XX, lists the elements of a hardware reliability program and shows the importance of each element during the life cycle phases of development. This list generally follows the outline of MIL-STD-785A, "Reliability Program for Systems and Equipment Development and Production".[5] MIL-STD-785A is the basic standard for

Element	Life Cycle Phase				
	Conceptual	Validation	Full Scale Development	Production	Deployment
Requirements Definition	xxxxxxxxxx	xxxxxxxAAAAAA	A.....		
Reliability Model	xxxxx	xxxxxxxxxxxxxx	xxxxx.....		
Reliability Prediction	xxxxx	xxxxxxxxxxxxxx	xxxxx.....		
Reliability Apportionment	ooooo	ooooooooooooooo	ooooo.....		
Failure Modes Analysis	ooooo	ooooooooooooooo	xxxxx.....		
Design for Reliability	ooooo	xxxxxxxxxxxxxxx	xxxxxxxxxxx	.....	
Parts Selection	ooooo	xxxxxxxxxxxxx	AAAAAA.....	.....	
Design Review	ooooo	xxxxxxxxxxxxxx	xxxxx.....		
Design Specifications	xxxxxxx	xxxxxxxxxxxxx	x.....		
Acceptance Specifications	xxx	xxxxxxxxxAAAAA	.....		
Reliability Evaluation Tests	----	xxxxxxxxxxxxxx	xxxxx		
Failure Analysis	----	xxxxxxxxxxxxxx	xxxxxxxxxxxx	ooooooooooo	ooooooooooo
Data System	----	xxxxxxxxxxxxxx	xxxxxxxxxxxx	ooooooooooo	ooooooooooo
Quality Control		ooooooooooo	xxxxxxxxxxxxx	xxxxxxxxxxx	ooooooooooo
Environmental Tests		xxxxx	.....AAAAAAA	.....	
Reliability Acceptance Tests		xx	.....AAAAA	ooooooooo	

First contract

KEY

------	Desirable activity (for highest success probability)
oooooo	Necessary activity (errors seldom disastrous)
xxxxxx	Very important activity (errors often disastrous)
AAAAAA	Critical activity (errors usually disastrous)
.....	Low key activity (to update previous results)

Figure 2-7 RELIABILITY PROGRAM ELEMENTS[10]

planning reliability programs for Department of Defense development and production contracts.

2.3 Reliability Evaluation Tools During Development

Reliability evaluation techniques can be classified into the categories shown in Figure 2-8.[6] The figure indicates that various models are used to apportion reliability requirements to various levels of hardware within the total system, and to predict the design's inherent reliability. The estimates become benchmarks for subsequent reliability assessment efforts. Other reliability efforts are concerned with trading and measuring the growth of reliability during the development effort, and with assuring that reliability is not degraded during production or during operation and maintenance activities. Although several methods and techniques are employed during the development effort to evaluate reliability, they all rely on prediction techniques to provide a quantitative measure of reliability.

Reliability prediction, failure modes and effects analysis (FMEA) and reliability growth techniques represent those prediction and design evaluation methods that provide a quantitative measure of how reliably the design will perform. Additionally, these techniques help determine where the design can be improved. Since specified reliability goals have become common contractual requirements which must be met along with functional performance requirements, it is evident that these quantitative evaluations need to be applied during the design stage to guarantee that the equipment will function as specified for a given duration under the operational and environmental conditions of intended use. These reliability evaluation tasks are described in the subsections which follow.

2.3.1 Prediction Techniques

Reliability prediction is the process of quantitatively assessing the reliability of a system or equipment during its development--prior to large scale fabrication and field operation. During design and development, predictions serve as quantitative guides by which design alternatives can be judged for reliability. Reliability predictions also provide criteria for reliability growth and demonstration testing, logistics cost studies and various other development efforts.

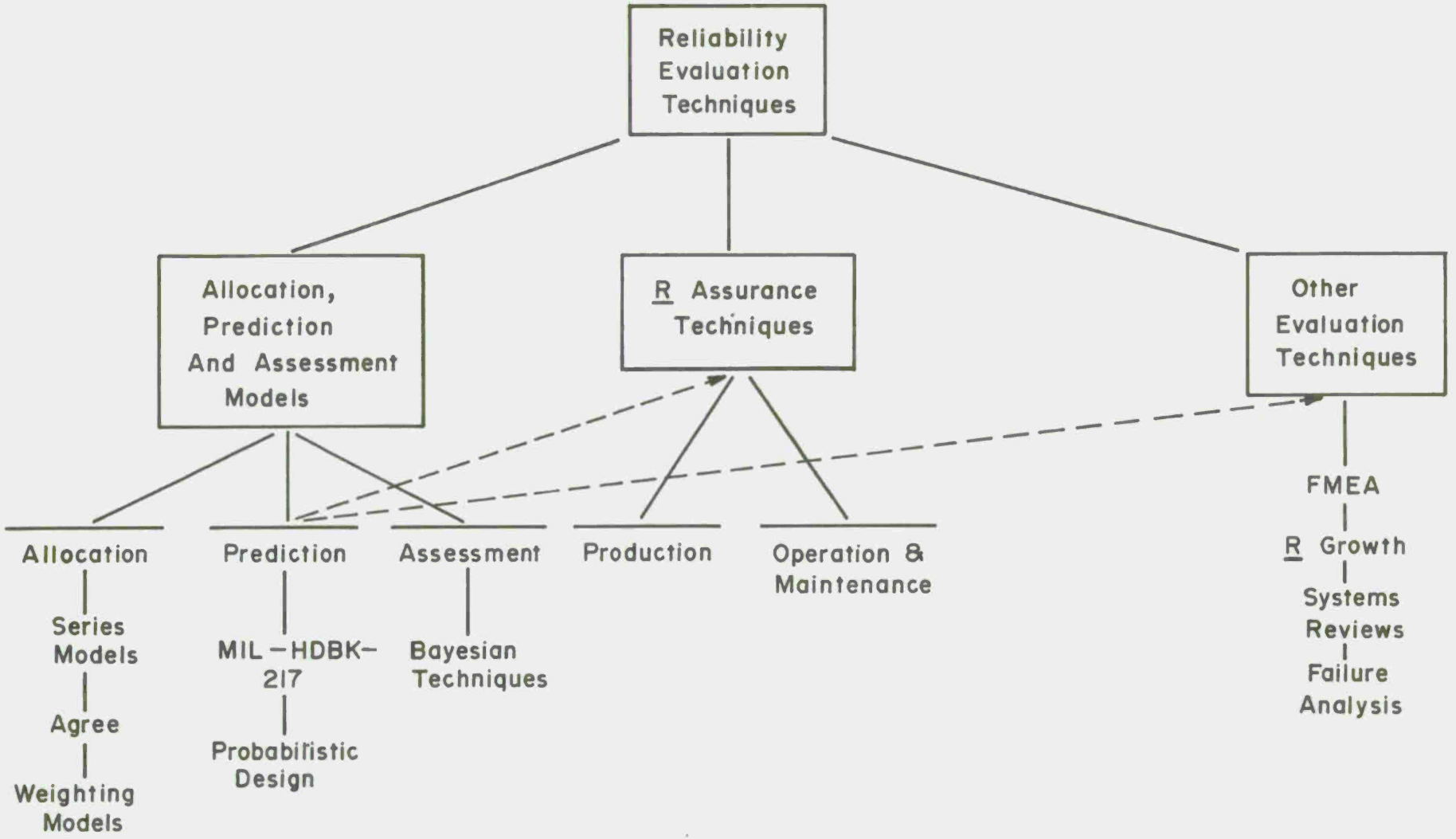


Fig 2-8 CLASSIFICATION OF RELIABILITY EVALUATION TECHNIQUES (Ref. 6)

Thus, reliability prediction is a key to system development and allows reliability to become an integral part of the design process. To be effective, the prediction technique must relate engineering variables (the language of the designer) to reliability variables (the language of the reliability engineer).

A prediction of reliability is obtained by determining the reliability of the lowest system level item and proceeding through intermediate levels until an estimate of system reliability is obtained. The prediction methodology is dependent on the availability of: (1) accurate evaluation models that reflect the reliability connectivity of the lower level items and (2) substantial failure data that has been analyzed and reduced to a form suitable for application to the low level items.

There are various formal prediction procedures, based on theoretical and statistical concepts that differ in the level of data on which the prediction is based. The specific steps for implementing these procedures are described in detail in reliability handbooks. Among the procedures available are parts count methods and stress analysis techniques. Failure rate data for both methods are available in MIL-HDBK-217B.[3]

The parts count method provides an estimate of reliability based on a count by part type (resistor, capacitor, integrated circuit, transistor, etc.). This method is applicable during proposal and early design studies where the degree of design detail is limited. It involves counting the number of parts of each type, multiplying this number by a generic failure rate for each part type and summing up the products to obtain the failure rate of each functional circuit, subassembly, assembly and/or block depicted in the system block diagram. The advantage of this method is that it allows rapid estimates of reliability in order to quickly determine the feasibility (from the reliability standpoint) of a given design approach. The technique uses information derived from available engineering information and does not require detailed part-by-part stress and design data.

The stress analysis technique involves the same basic steps as the part count technique. However, the stress analysis technique requires the use of detailed part models (as shown in Section 2.1.3) plus calculation of circuit stress values for each part prior to determining its

failure rate. Each part is evaluated in its electrical circuit and mechanical assembly application based on an electrical and thermal stress analysis. Once part failure rates are established, a combined failure rate for each functional block in the reliability diagram can be determined. To facilitate calculation of part failure rates, worksheets based on part failure rate models are normally prepared to aid in the evaluation. Figure 2-9 depicts a worksheet patterned after information derived from MIL-HDBK-217B. These worksheets are prepared for each functional circuit in the system. When completed, these sheets provide a tabulation of circuit part data including: part description, electrical stress factors, thermal stress factors, basic failure rates, the various multiplying or additive environmental and quality adjustment factors, and the final combined part failure rates. The variation in part stress factors (both electrical and environmental) resulting from changes in circuitry and packaging is the means by which reliability is controlled during design. Considerations for and effects of reduced stress levels (derating) which result in lower failure rates are treated in Section 4.1.3.

Both the parts count and the stress analysis methods of predicting reliability rely on part failure rate data obtained from MIL-HDBK-217B. However, not all parts used in electronic system design are included in MIL-HDBK-217B. For those parts not covered by 217B, where little supporting data is available, care must be exercised in estimating their failure rates. In general, estimating failure rates for parts having limited failure data involves comparative evaluations or special tests and studies.

Comparative evaluations involve the extrapolation of failure data from well documented parts to parts having little or no failure data provided similarity exists. Similarity refers to those performance, type, class, construction, material or rating parameters by which the comparison can be made. To remain valid, extrapolation must account for the differences between the parts compared as well as their similarities and must be supported by detailed rationale.

Evaluations must include modes of failure, production history and other factors bearing on reliable operations.

STRESS ANALYSIS – RELIABILITY PREDICTION WORKSHEET

ENGINEERING DATA													RELIABILITY ANALYSIS												
1	2	3	4			5			6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
LINE	REF. DES.	PART DESCRIPTION	LOAD, VOLTAGE, DISSIPATION						Stress Ratio Or Tj	Appl Or Hot Spot Value Or Cap Freq. & Wave F'M	Const. Or Wire Or Cmplxty (Note 1)	Cycles Or Service Grade	Contact Qty Or Form Or Z CKT	λ_b $\times 10^{-6}$ Hrs.	Π_V Π_{S2} Π_L	Π_R Π_{RW} Π_{SR} Π_{CV}	Π_E Π_{EG}	Σ_E	Π_{ER}	Π_Q OR Π_A	Π_{CS} Π_F Π_G Π_P Π_t	Π_C	Π_N Π_{TAP} Π_P (PIN)	N Σ CYC	Π CYC	λ PART $\times 10^{-6}$
			ACTUAL			RATED																				
			I	V	W	I	V	W																		
1																										
2																										
3																										
4																										
5																										
6																										
7																										
8																										
9																										
10																										

ENG _____ NAME _____ DATE

REL _____ NAME _____ DATE

_____ PROJECT / UNIT

_____ ASSEMBLY / ASSEMBLY PART NO.

_____ ENVIRONMENT / ASSEMBLY FPMH

NOTES: LIST CONNECTOR BODY MATERIAL HERE

SUM

Fig. 2-9 STRESS ANALYSIS – RELIABILITY PREDICTION WORKSHEET

Part test efforts usually require extended time periods and/or large quantities of parts before statistically confident failure rates can be established. Costs associated with large scale part testing may be difficult to justify for low usage parts.

In another direction, efforts to relate reliability to system function and performance level, as exemplified by the "Reliability Prediction Techniques for Conceptual Phases of Development"[7], have produced interesting results. Strong correlations have been found between radar performance variables (such as peak power, pulse width, antenna gain, etc.) and MTBF characteristics. These techniques, based on the analysis of system failure data, provide a means for relating predictions to actual system use history and through mathematical methods such as regression analysis, to major performance parameters.

In addition, newer techniques[8] are currently available which allow estimates to be made of the time requirements needed to bring a newly developed system to reliability maturity (RPM). At lower levels of assembly, the concepts related to the forced defect approach to subassembly testing are applicable. These techniques allow for quantitative estimation of the reliability growth process which heretofore, for the most part, was ignored in the design and production process. Reliability growth techniques are discussed in Section 2.3.3.

The actual prediction techniques used for any given system vary depending on the phase of system development. Consequently, each prediction effort is evaluated in view of the development phase which it represents. For example, a gross reliability prediction (based on rough parts count or based on function/performance levels) may be completely adequate during the preliminary design and definition phase. It would serve as the basis to determine if the inherent reliability of the design is feasible and is within the "design to" requirements established by cost of ownership studies, and consequently can be used as the basis (from a reliability standpoint) to proceed to the detailed design stage. As further information becomes available, a gross prediction would not be adequate. At this time, possibly, a part-by-part reliability prediction, based on stress analysis techniques, would be required.

Figure 2-10 is a partial list of a radar system hierarchy. The life cycle phases of a radar development program are also listed. The figure shows that, as the program progresses from conceptual to detailed design, hardware is defined at a lower level of the assembly. Reliability prediction, allocation and assessment is required to predict reliability and should be continually updated to reflect the greater level of hardware definition. Also listed in Figure 2-10 are reliability prediction techniques appropriate to the level of design definition.

2.3.2 Failure Mode Analysis Techniques

Under the heading of failure mode analysis, two techniques are generally used, namely, (1) failure mode, effects and criticality analysis, and (2) fault tree analysis. Failure mode, effects and criticality analysis represents a "bottom-up" approach while fault tree analysis represents a "top-down" approach. Both represent analytical approaches for assessing the consequences of failure.

Failure mode and effects analysis is an iterative documented process of a systematic nature performed to identify basic faults at the part level and determine their effects at higher levels of assembly. The failure mode and effects analysis can be performed utilizing either actual failure modes from field data or hypothesized failure modes derived from design analyses, reliability prediction activities and experiences relative to the manner in which parts fail. In their most complete form, failure modes are identified at the part level, which is usually the lowest level of direct concern to the equipment designer. In addition to providing insight into failure cause and effect relationships, the failure mode and effects analysis provides the disciplined method for proceeding part-by-part through the system to assess failure consequences (see Figure 2-2B). Failure modes are analytically induced into each component, and failure effects are evaluated and noted, including severity and frequency (or probability) of occurrence. As the first mode is listed, the corresponding effect on performance at the next higher level of assembly is determined. The resulting failure effect becomes, in essence, the failure mode that impacts the next higher level. Iteration of this process results in establishing the ultimate effect at the system level. Once the analysis has been performed for all failure modes, it is usually the

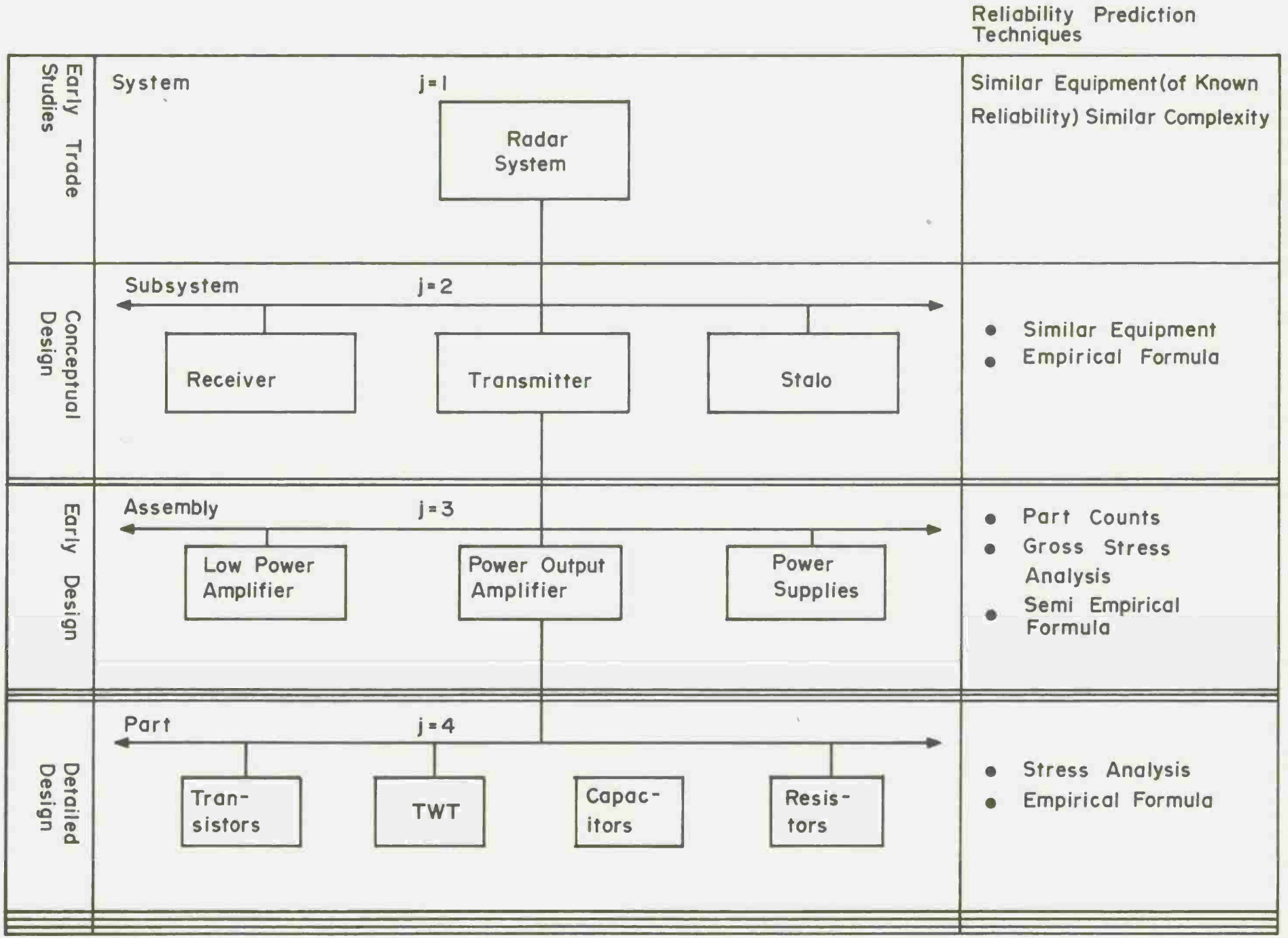


Fig 2-10 RADAR SYSTEM HIERARCHY(PARTIAL LISTING)

case that each effect or symptom at the system level is caused by several different failure modes at the lowest level. This relationship to the end effect provides the basis for grouping the lower level failure modes.

Using this approach, probabilities for the occurrence of the system effect can be calculated, based on the probability of occurrence of the lower level failure modes (i.e., modal failure rate times time). Based on these probabilities, and a severity factor assigned to the various system effects, a criticality number can be calculated. Criticality numerics provide a method of ranking the system level effects derived previously. Criticality numerics also provide the basis for corrective action priorities, engineering change proposals or field retrofit actions. Figure 2-11 depicts a convenient format for documenting the information generated during failure mode, effects and criticality analyses.

FAILURE MODE, EFFECTS AND CRITICALITY ANALYSIS Page of

System _____ LRU _____ Circuit _____ Date _____

Eng'r _____

Part	Failure Mode	Part Effect	Circuit Effect	System Effect	Failure Frequency	Criticality

Figure 2-11 FMECA WORKSHEET

Fault tree analysis (FTA) is a tool that lends itself well to analyzing failure modes found during design, factory test or field data returns. The fault tree analysis procedure can be characterized as an iterative documented process of a systematic nature performed to identify basic faults, determine their causes and effects, and establish their probabilities of occurrence. The approach involves several steps, among which is the structuring of a highly detailed logic diagram which depicts

basic faults and events that can lead to system failure and/or safety hazards. Next is collecting basic fault data and failure probabilities for use in computation. The next step is using computational techniques to analyze the basic faults, determine failure mode probabilities, and establish criticalities. The final step involves formulating corrective suggestions which, when implemented, would eliminate (or minimize) those faults considered critical. The steps involved, the diagrammatic elements and symbols, and methods of calculation are shown in Figure 2-12.

This procedure can be applied at any time during a system's life cycle. However, it is considered most effective when applied:

(a) during preliminary design, on the basis of design information and a laboratory or engineering test model, and

(b) after final design, prior to full scale production, on the basis of manufacturing drawings and an initial production model.

The first of these is performed to identify failure modes and formulate general corrective suggestions (primarily in the design area). The second is performed to show that the system, as manufactured, is acceptable with respect to reliability and safety. Corrective actions or measures, if any, resulting from the second analysis would emphasize controls and procedural actions that can be implemented with respect to the "as manufactured" design configuration.

The outputs of the analysis include:

(a) A detailed logic diagram that depicts all basic faults and conditions that must occur to result in the hazardous condition(s) under study.

(b) A probability of occurrence numeric for each hazardous condition under study.

(c) A detailed fault matrix that provides a tabulation of all basic faults, their occurrence probabilities and criticalities, and the suggested change or corrective measures involving circuit design, component part selection, inspection, quality control, etc., which, if implemented, would eliminate or minimize the hazardous effect of each basic fault.

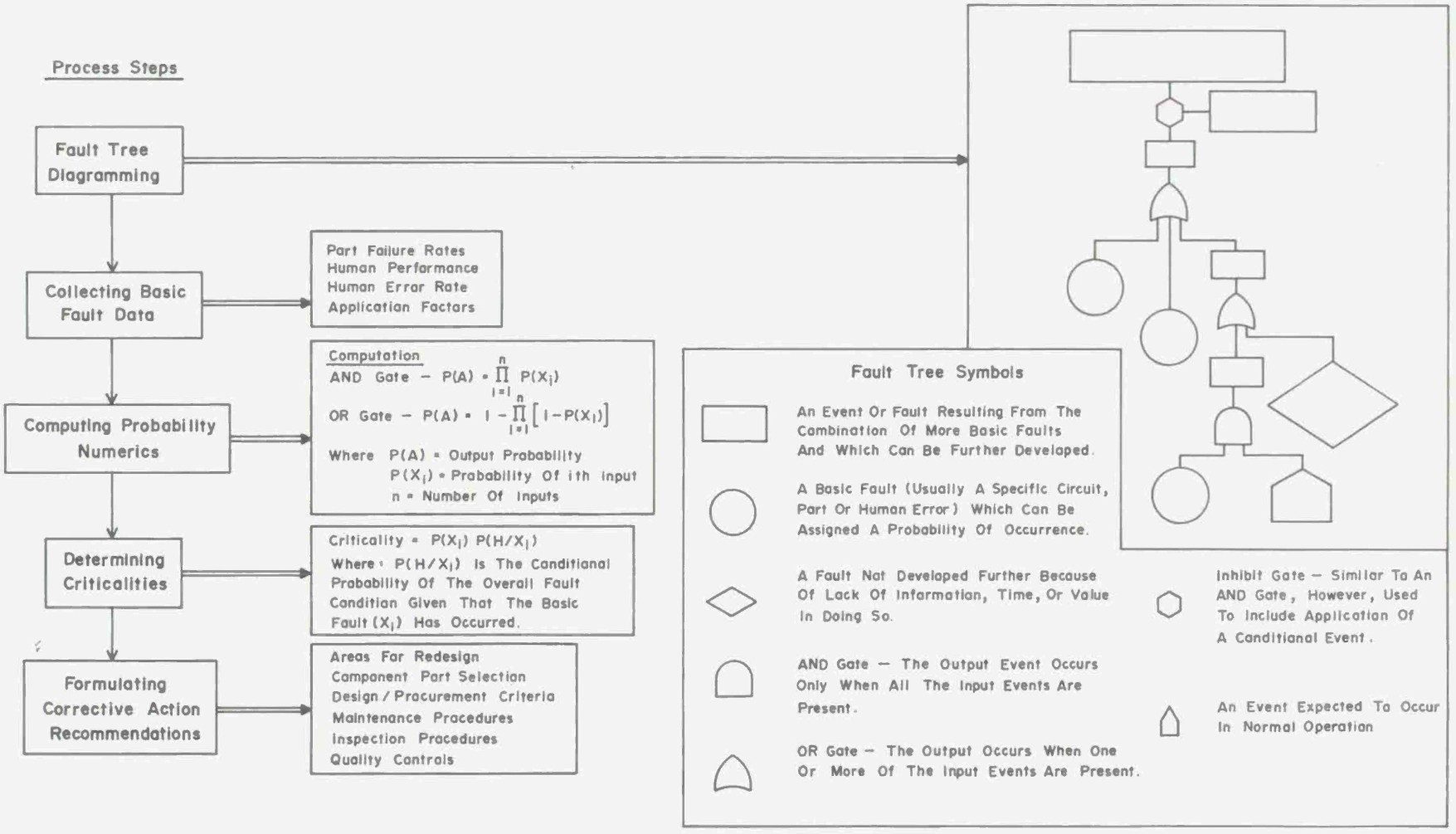


Fig. 2-12 FAULT TREE ANALYSIS

2.3.3 Reliability Testing

Reliability testing during system development can be divided into two major classifications:

(1) Reliability Growth

(2) Reliability Demonstration.

Reliability growth tests are for the purpose of detecting reliability problems. Reliability demonstration tests are for the purpose of proving reliability. Basic concepts associated with each of these test classes are discussed in this subsection.

Reliability growth can be generally defined as the improvement process during which hardware reliability increases to an acceptable level. As indicated in Section 1.2.3, the measured reliability of newly fabricated hardware is much less than the potential reliability estimated during design, using standard handbook techniques. This definition encompasses not only the technique used to graph increases in reliability (i.e., "growth plots") but also the management/resource allocation process which causes hardware reliability to increase.[8] Both are discussed here.

The purpose of a growth process, especially a reliability growth test, is to achieve acceptable reliability in field use. Achievement of acceptable reliability is dependent on the extent to which testing and other improvement techniques have been used during development to "force-out" design and fabrication flaws, and on the rigor with which these flaws are analyzed and corrected. A primary objective of growth testing is to provide methods by which hardware reliability development can be dimensioned, disciplined and managed as an integral part of overall development. Reliability growth testing also provides a technique for extrapolating the current reliability status (at any point during the test) to some future result. In addition, it provides methods to assess the magnitude of the test-fix-retest effort prior to the start of development, thus allowing trade-off decisions.

Many of the models for reliability growth represent the reliability of the system as it progresses during the overall development program. Also, it is commonly assumed that these curves are nondecreasing, that is, once the system's reliability has reached a certain level, it will not drop below this level during the remainder of the development program. It is important to note that this assumes that any design or engineering changes made during the development program do not decrease the system's reliability.

If, before the development program has begun, the exact shape of the reliability growth curve is known for a certain combination of system design and development effort, then the model is a deterministic one. In this case, the amount of development effort needed to meet the reliability requirement could be determined, and the sufficiency of the design would also be known.

In most situations encountered in practice, the exact shape of the reliability growth curve will not be known before the development program begins. One may, however, be willing to assume that the curve belongs to some particular class of parametric reliability growth curves. The analysis then reduces to a statistical problem of estimating the unknown parameters from the experimental data. These estimates may be revised as more data are obtained during the progress of the development program. Using these estimates, the program manager can monitor and project the reliability of the system and make necessary decisions accordingly.

For complex electronic/electromechanical avionic systems, the model used most often for reliability growth processes, and in particular reliability growth testing, is one originally published by J. T. Duane.[8,9] Essentially, this model provides a deterministic approach to reliability growth such that the system MTBF versus operating hours falls along a straight line when plotted on log-log paper. That is, the change in MTBF during development is proportioned to T^{α} where T is the cumulative operating time and α is the rate of growth corresponding to the rapidity with which faults are found and changes made to permanently eliminate the basic causes of the faults observed.

In order to structure a growth test program (based on the Duane model) for a newly designed system, a detailed test plan is necessary. This plan must describe the test-fix-retest concept and show how it will be applied to the system hardware under development. The plan must incorporate the following:

(a) Values for specified and predicted (inherent) reliabilities. Methods for predicting reliability (model, data base, etc.) must also be described.

(b) Criteria for reliability starting points, i.e., criteria for estimating the reliability of initially fabricated hardware, must be determined. For avionics systems, the initial reliability for newly fabricated systems has been found to vary between 10 and 30% of their predicted (inherent) values.

(c) Reliability growth rate (or rates) must be defined. To support the selected growth rate, the rigor with which the test-fix-retest conditions are structured must be completely defined.

(d) Calendar time efficiency factors, which define the relationship of test time, corrective action time and repair time to calendar time, must be determined.

Note that each of the factors listed above impacts the total time (or resources) which must be scheduled to grow reliability to the specified value. Figure 2-13 illustrates the concepts described above.

In addition, Figure 2-13 graphically depicts the four elements needed to structure and plan a growth test program described above. These four elements are further described as follows:

(1) Inherent reliability--represents the value of design reliability estimated during prediction studies, and may correspond to the value above that specified in procurement documents. Ordinarily, the contract specified value of reliability is somewhat less than the inherent value. The relationship of the inherent (or specified) reliability to the starting point greatly influences the total test time.

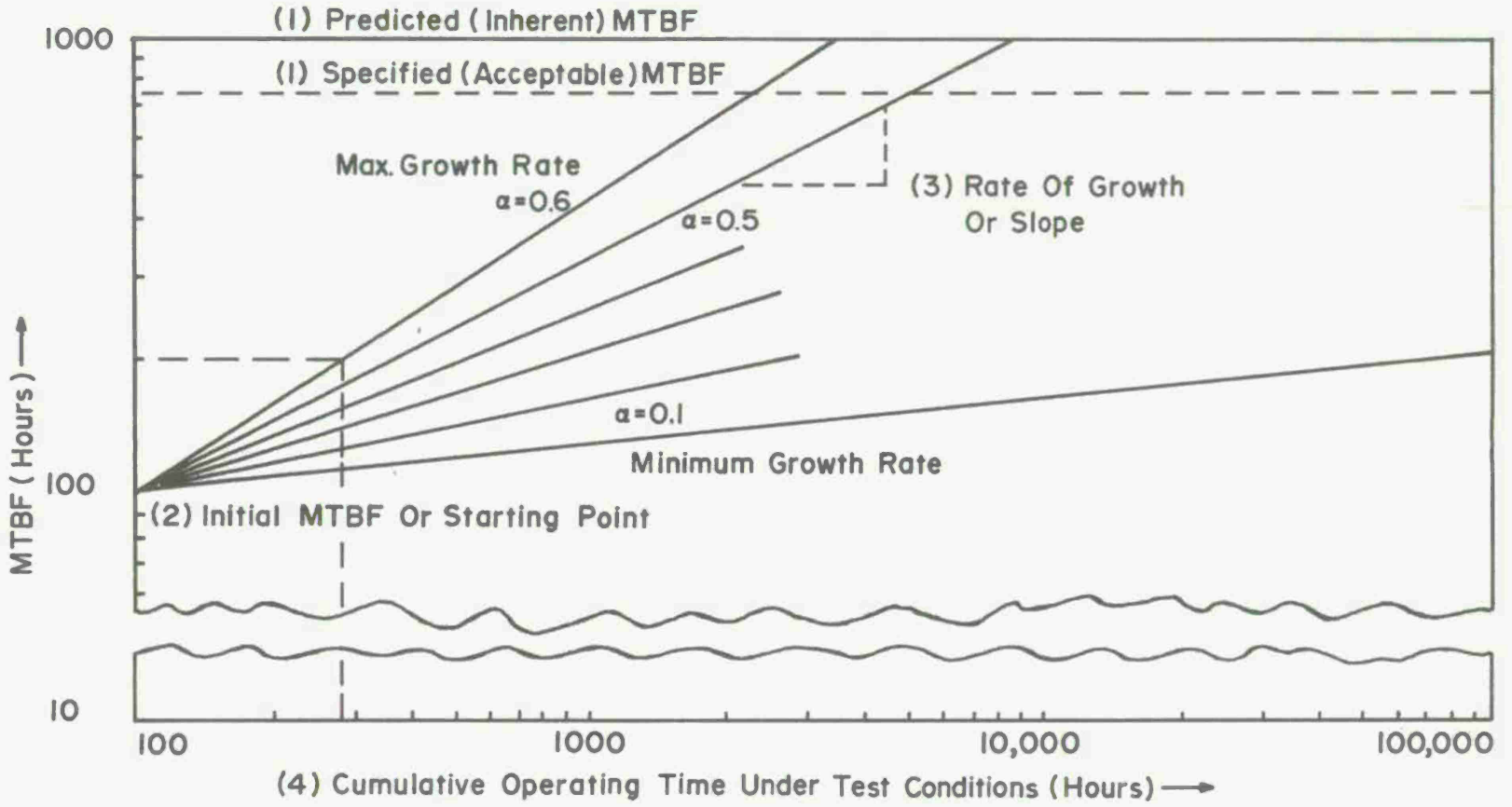


Fig 2-13 RELIABILITY GROWTH PLOT

(2) Starting point--represents an initial value of reliability for the newly manufactured hardware usually falling within the range of 10-30% of the inherent or predicted reliability. Estimates of the starting point can be derived from prior experience or are based on percentages of the estimated inherent reliability. Starting points must take into account the amount of reliability control exercised during the design program and the relationship of the system under development to the state-of-the-art. Higher starting points minimize test time.

(3) Rate of growth--depicted by the slope of the growth curve which is, in turn, governed by the amount of control, rigor and efficiency by which failures are discovered, analyzed and corrected through design and quality action. Rigorous test programs which foster the discovery of failures, coupled with management-supported analysis and timely corrective action, will result in a faster growth rate and consequently less total test time.

(4) Calendar time/test time--represents the efficiency factors associated with the growth test program. Efficiency factors include repair time and operating/nonoperating time as they relate to calendar time. Lengthy delays for failure analysis, subsequent design changes, implementation of corrective action or short operating periods will extend the growth test period.

Figure 2-13 shows that the value of the parameter α can vary between 0.1 and 0.6. A growth rate of 0.1 can be expected in those programs where no specific consideration is given to reliability. In those cases, growth is largely due to solution of problems impacting production and from corrective action taken as a result of user experience. A growth rate of 0.6 can be realized if an aggressive, hardhitting reliability program with management support is implemented. This latter type program must include a formal stress oriented test program designed to aggravate and force defects and vigorous corrective action.

Figure 2-13 shows the requisite hours of operating and/or test time and continuous effort required for reliability growth. It shows the dramatic effect that the rate of growth (α) has on the cumulative operating time required to achieve a predetermined reliability level. For example, Figure 2-13 shows, for a product whose MTBF potential is 1000 hr, that 100,000 hr of cumulative operating time is required to achieve an MTBF of 200 hr when the growth rate is 0.1. And, as previously stated, a 0.1 rate is expected when no specific attention is given to reliability growth. However, if the growth rate can be accelerated to 0.6 (by growth testing and formal failure analysis activities), then only 300 hr of cumulative operating time is required to achieve an MTBF of 200 hr.

Reliability demonstration tests are designed for the purpose of proving, with statistical confidence, a specific reliability requirement; not specifically to detect problems, or to grow reliability. The test takes place after the design is frozen and its configuration is not allowed to change. However, in practice, some reliability growth may occur because of the deferred correction of failures observed during the test.

Reliability demonstration is specified in most military system procurement contracts and involves, in many instances, formal testing conducted per MIL-STD-781B. This standard defined test plans, environmental exposure levels, cycle times and documentation required to demonstrate formally that the specified MTBF requirements of the equipment have been achieved. Demonstration tests are normally conducted <u>after</u> development has been completed but before high rate production has been initiated. Demonstration tests are normally conducted after growth tests in the development cycle using initial production hardware.

As previously indicated, reliability demonstration testing, conducted per MIL-STD-781B, carries with it a certain statistical confidence level--and the more demonstration testing, the more confidence. The more reliability growth testing that is performed, the higher the actual reliability. Depending on program funding and other constraints, system testing may follow one of two options. The first option maximizes growth testing and minimizes demonstration testing resulting in a high MTBF at a low confidence. Option two minimizes reliability growth testing with a resultant lower MTBF at higher confidence. These concepts are shown graphically in Figure 2-14.

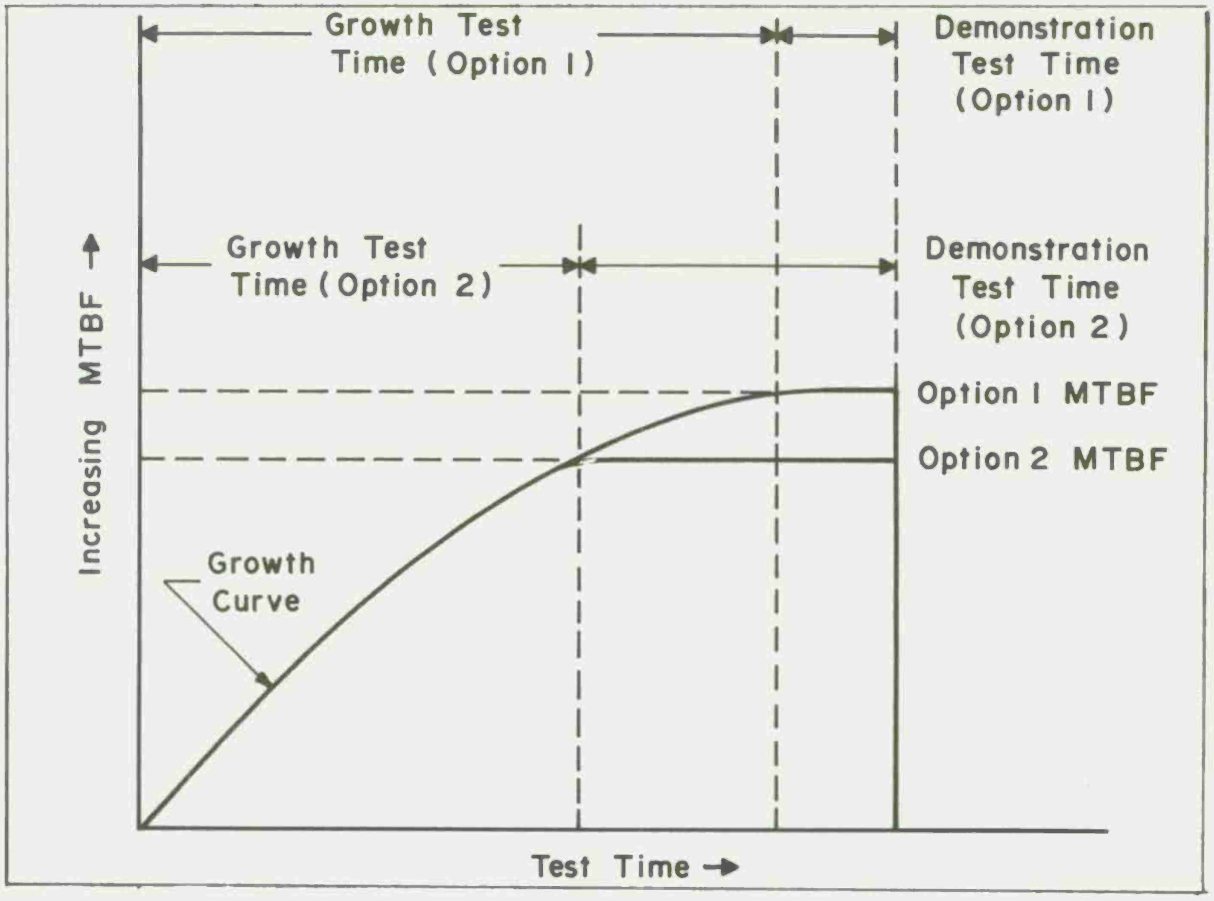


Fig. 2-14 RELIABILITY TESTING OPTIONS

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SECTION 3

MILITARY AIRBORNE SYSTEMS

SECTION 3

MILITARY AIRBORNE SYSTEMS

The objective of this section is to provide a general overview of military electronic system design trends and the reliability design issues and circumstances that surround them. Airborne electronics are emphasized because they are most challenging to the designer. Constraints in size, weight, volume and operational environment are generally much more restrictive for airborne systems than they are for ground based equipments. The factors are discussed relative to trends that are evident today in avionics, the avionics environment over which reliability must be provided, and an engineering judgment of current equipment reliability state-of-the-art.

3.1 Trends in Avionics*

Over the last decade, the use of integrated circuits has increased dramatically across all portions of the RF spectrum in the areas of low to medium power level. The situation is approximately as shown in Figure 3-1, and has impacted favorably on the general question of reliability, maintainability, and cost effectiveness of avionic systems.

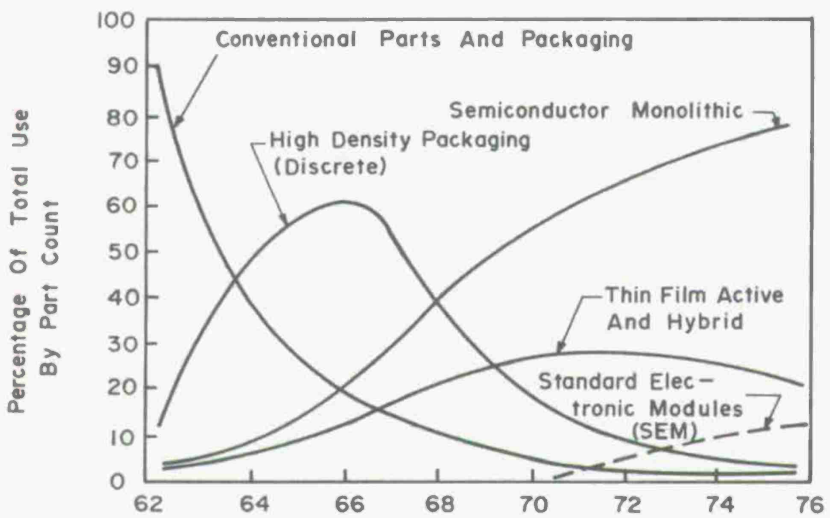


Fig. 3-1 ESTIMATION OF USAGE

*The material in Sections 3.1 and 3.4 is based on the references numbered 1 through 5 at the end of this chapter.

Table 3-1 is illustrative of avionics equipment trends in modern day military aircraft. The avionics suite typically includes navigation, communication, radar, penaids, IFF, internal control, display and information systems. A sampling of different types of aircaft is given for comparison. Figure 3-2 and Table 3-2 exemplify the system complexity of a typical multimode radar. System complexity has a strong bearing on reliability and is considered further in Section 3.3.

Table 3-1 AVIONICS MATRIX

		A-10 (Basic)	A-10 (Night)	A-10 (Adv)	F-15	F-16	RF-4C (Adv)	F-106 (Adv)	B-1
NAVIGATION	NAVSET			•					
	OMEGA								
	LORAN		•				•		
	INERTIAL			•	•	•	•		•
	DOPPLER			•					•
	AIR DATA	•	•	•	•	•	•	•	•
	TACAN	•	•	•	•	•	•	•	•
	ILS/MLS		•	•	•		•	•	•
	RADAR ALTIMETER						•	•	•
	RADAR (AIR/GROUND)						•		•
	RADAR (TA/TF)						•		•
	AHRS	•	•		•				
	UHF ADF	•	•	•	•	•			•
FLIGHT CONTROL	SAS AVAIDS	•	•						•
	AFCS AVAIDS		•		•				•
	SAS DIGITAL			•		•	•	•	
	AFCS DIGITAL			•		•	•	•	
COMMUNICATIONS	UHF	•	•		•	•	•	•	•
	HF		•	•			•		•
	VHF	•	•						
	IFF TRANS	•	•	•	•	•	•	•	•
	IFF INTER				•	•		•	•
	DIGITAL LINK			•	•	•		•	
	DOWN LINK						•		
	INTERCOM	•	•				•	•	•
EW	RHAW/ECM	•	•	•	•	•		•	•
	ELINT/ECM						•		
CONTROLS/ DISPLAYS	INSTRUMENTS	•	•	•	•	•	•	•	•
	CONTROLS	•	•	•	•	•	•	•	•
	HUD		•	•	•	•		•	
	HSD				•		•	•	
	VSD				•		•	•	
	MFD						•	•	
MISSION FIRE CONTROL	RADAR (A/A)			•	•	•		•	
	MISSILE SUPPORT	•	•	•	•	•			
	AIR GND (CCJP)		•	•					
	AIR GND FIXREF	•							•
	AIR AIR (HLGS)					•			
	STORES MGMNT	•	•	•		•			•
	LASER SEEKER	•	•	•					
	LASER RANGER		•	•					
MISSION SENSORS	EO		•	•			•		•
	CAMERA						•		
	SLAR						•		
	VIR						•		•
	DATA ANNOTATION						•		
AIRCRAFT	PROPULSION CONTROL							•	
	FUEL MANAGEMENT					•		•	•
	FLIGHT HISTORY			•			•	•	•
	FLIGHT ENVELOPE CNTRL	•	•	•		•	•	•	•

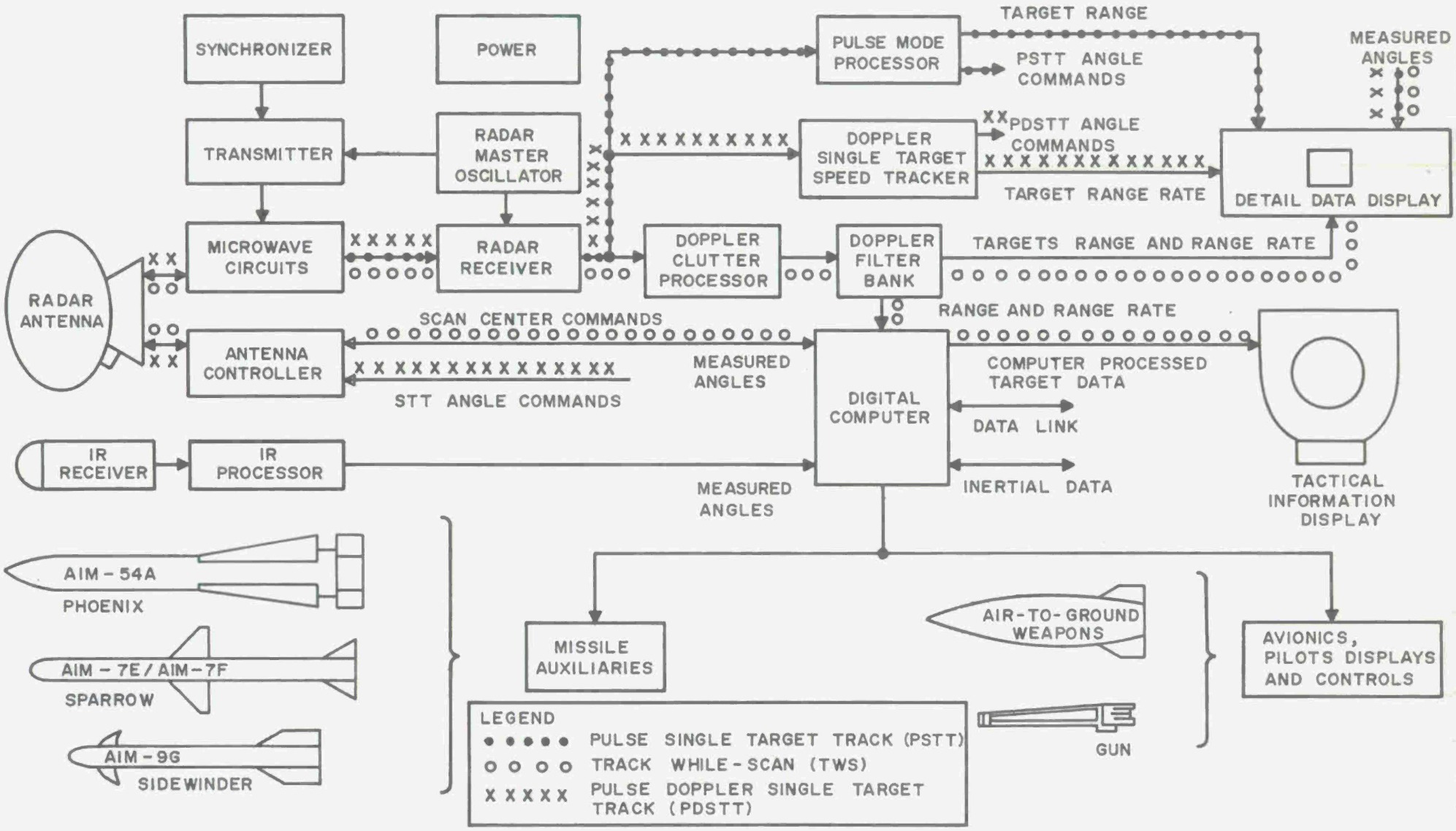


Fig. 3-2 AWG-9 RADAR SYSTEM

Table 3-2 AWG-9 RADAR SYSTEM

		Analog Functional Complexity (Estimate of Equivalent Series Active Elements)	Estimated Reliability MTBF (KHr) (Sec. 33)
1. Radar	Radar functioning as pulse Doppler sensor for long and intermediate ranges or as conventional pulse radar for long and especially short ranges	200-400	0.08-0.16
2. Antenna	Broadband, slotted planar array	1-5	20-100
Antenna Controller		10-20	3-6
Microwave Circuits		1-5	20-100
3. Transmitter	1) Uses gridded pulse TWT for pulse Doppler mode and Phoenix guidance 2) Uses separate CW TWT for Sparrow target illumination	50-100	0.04-0.8
Synchronizer		5-10	6-12
Master Oscillator		5-10	6-12
4. Receiver		25-50	0.9-1.8
Doppler Clutter Processor		10-20	3-6
Doppler Filter Bank		10-20	3-6
Doppler Single Target Speed Processor	Used for Sparrow target illumination mode	5-10	6-12
Pulse Mode Processor		5-10	6-12
5. Detail Data Display	Storage tube	5-10	6-12
Tactical Information Display	10" diameter CRT	5-10	6-12
6. Digital Computer	(Equivalent Analog Complexity)	25-50	0.9-1.8
7. Data Link System	(Equivalent Analog Complexity)	25-50	0.9-1.8
8. Inertial Information System		50-100	0.4-0.8
9. IR Receiver		50-100	0.4-0.8
IR Processor		25-50	0.9-1.8
10. Power System		50-100	0.4-0.8
11. Missile Auxiliaries			
AIM-54A Phoenix		50-100	0.4-0.8
AIM-7E/F Sparrow		50-100	0.4-0.8
AIM-9G Sidewinder		50-100	0.4-0.8

A most significant trend, from the point of view of system architecture, is the trend toward digital electronics. This is indicated by the use of digital fly-by-wire to replace mechanical linkages and hydraulic systems, the use of digital multiplexing to replace extensive bundles of individual cables, and the use of computers to oversee and control the various avionics systems.

The old situation, indicated in Figure 3-3a, shows the avionics structure of the F-4E and indicates that each avionics function along with its attendant controls, displays, and computer, represented essentially a separate individual entity. The new concept, indicated in Figure 3-3B, shows the tendency toward a general commonality that extends from a control computer to a common avionics bus and integrated displays. A wide range of potential advantages appears to favor this digital avionics concept. This includes the following:

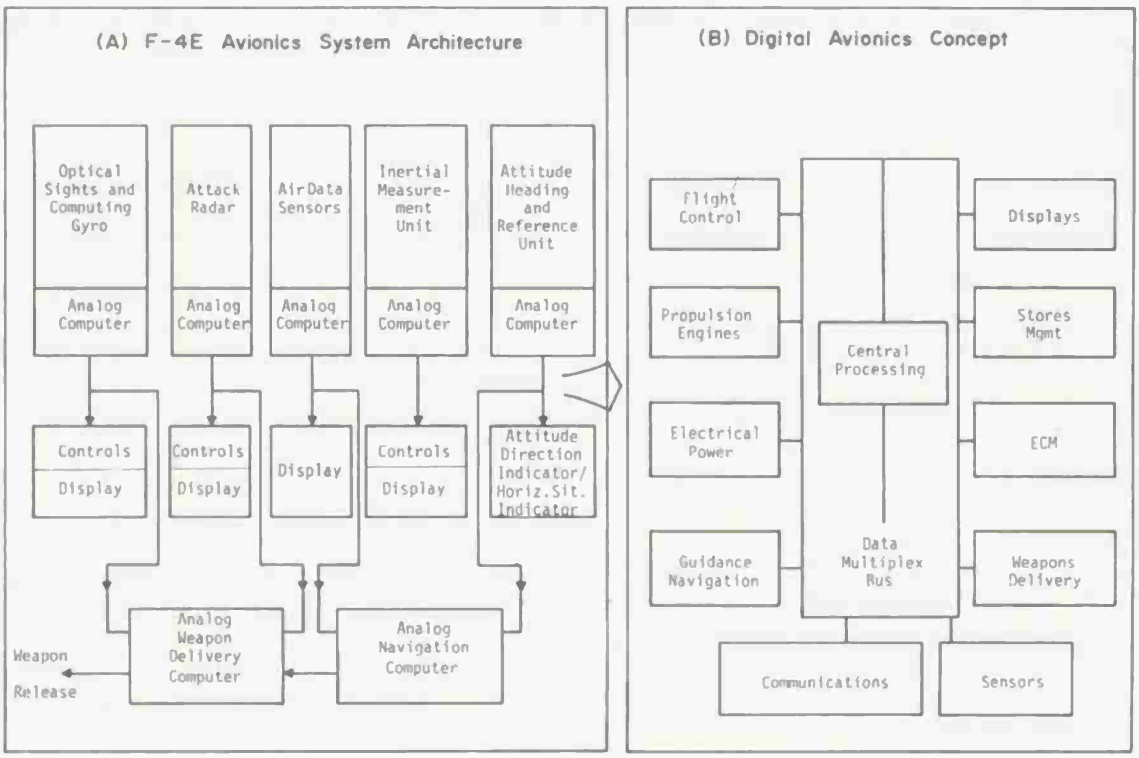


Fig. 3-3 DIGITAL AVIONICS TREND

- Digital information can generally be transmitted and processed faster and more flexibly than analog information.
- Large scale integrated-circuit (LSI) computers can provide much higher data processing capacities at a fraction of the cost and size of preceding generation equipment.
- Digital avionics holds out the promise of significant system reliability improvement and system cost reduction. Improved system reliability stems from the fact that digital avionics offers commonality, and hence widespread use, of a limited number of modular subsystems among different aircraft. Furthermore, the resultant modularity tends to improve maintainability and provide ready potential for future growth. Modifications and future expansions of avionics packages would tend to be readily achieved by plugging different modules into the basic core system.

The following sections consider the avionics environment over which reliability must be provided and the impact of equipment complexity on the MTBF potential.

3.2 The Avionics Environment

The avionics environment can impose relatively severe operating conditions on equipment with regard to conditions of temperature, altitude, shock, vibration, humidity, sand and dust, etc. The general military specification defining these service boundaries (primarily for operation in manned aircraft) is MIL-E-5400. In this specification, four classes of equipment are delineated according to the following temperature-altitude regime:

Class 1 -- Equipment designed for 50,000 ft altitude and continuous sea level operation over the temperature range of -54^{o} to $+55^{o}$C.

Class 1A -- Equipment designed for 30,000 ft altitude and continuous sea level operation over the temperature range of -54^{o} to $+55^{o}$C.

Class 2 -- Equipment designed for 70,000 ft altitude and continuous sea level operation over the temperature range of -54^{o} to $+71^{o}$C.

Class 3 -- Equipment designed for 100,000 ft altitude and continuous sea level operation over the temperature range of -54^{o} to $+95^{o}$C.

Class 4 -- Equipment designed for 100,000 ft altitude and continuous sea level operation over the temperature range of -54^{o} to $+125^{o}$C.

The operating boundaries for these classes of equipment are indicated in Table 3-3, and in Figures 3-4 and 3-5. The operating requirements are as follows:

(1) Each class of equipment is to be exposed to the temperature conditions shown in Table 3-3. The ambient temperature within the specified temperature ranges may remain constant for long periods or may vary at a rate as high as 1^{o} per second.

(2) Each class of equipment must operate under the conditions and within the ranges listed in column I, II, III and VII of Table 3-3.

(3) The equipment in a nonoperating condition must withstand long periods of exposure to the temperature extremes and thermal shock as listed in Table 3-3.

(4) Each class of equipment must meet the altitude conditions listed in column VIII of Table 3-3, both for continuous operation and exposure in a nonoperating condition. The altitude may remain constant for long periods or vary at a rate as high as 0.5 in. of mercury per second.

(5) The equipment is required to operate under the applicable temperature-altitude combinations shown in Figure 3-4.

(6) The equipment is required to withstand the effects of humidities up to 100 percent, including conditions wherein condensation takes place in and on the equipment. The equipment shall withstand the above conditions during operating and nonoperating conditions.

(7) When normally mounted (with vibration isolators in place, if any), the equipment shall operate satisfactorily when subjected

Table 3-3 ENVIRONMENTAL CONDITIONS

Equipment Operating								Equipment Operating and Nonoperating	Equipment Nonoperating	
Temperature extremes for the chamber (without external cooling provisions)				Combined Temperature Altitude			Temperature Shock	Altitude	Temperature Extremes	Temperature Shock
Equipment Class	I Continuous	II Intermittent	III Short-Time	IV	V	VI	VII	VIII	IX	X
Class 1	-54 °C to +55 °C	30 min +71 °C	---	Curve A	Curve B	---	-54 °C to +71 °C	Sea Level to 50,000 ft	-62 °C to +85 °C	-62 °C to +85 °C
Class 1A	-54 °C to +55 °C	30 min +71 °C	---	Curve A	Curve B	---	-54 °C to +71 °C	Sea Level to 30,000 ft	-62 °C to +85 °C	-62 °C to +85 °C
Class 2	-54 °C to +71 °C	30 min +95 °C	---	Curve A	Curve B	---	-54 °C to +95 °C	Sea Level to 70,000 ft	-62 °C to +95 °C	-62 °C to +95 °C
Class 3	-54 °C to +95 °C	30 min +125 °C	10 min +150 °C	Curve A	Curve B	Curve C	-54 °C to +125 °C	Sea Level to 100,000 ft	-62 °C to +125 °C	-62 °C to +125 °C
Class 4	-54 °C to +125 °C	30 min +150 °C	10 min +260 °C	Curve A	Curve B	Curve C	-54 °C to +150 °C	Sea Level to 100,000 ft	-62 °C to +150 °C	-62 °C to +150 °C

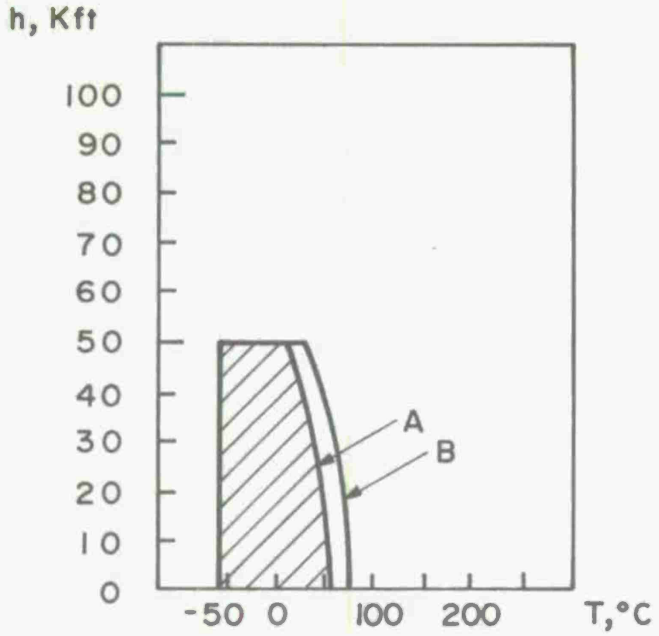


Fig.(A) Class I Equipment

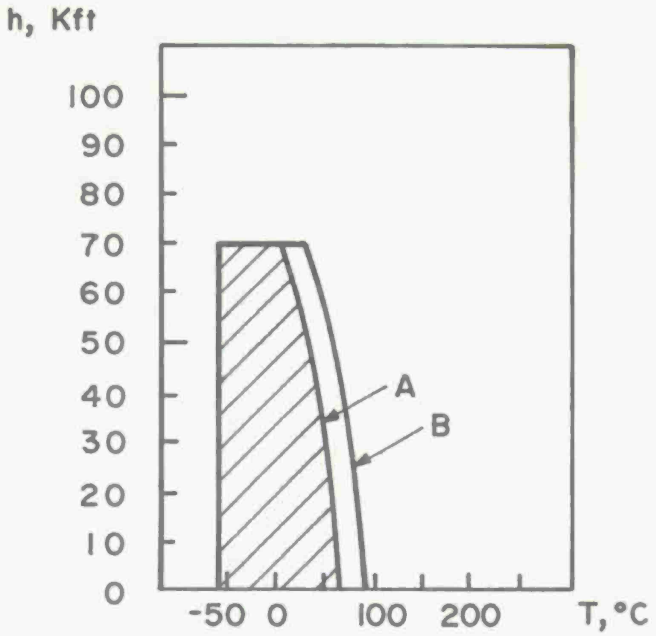


Fig.(B) Class 2 Equipment

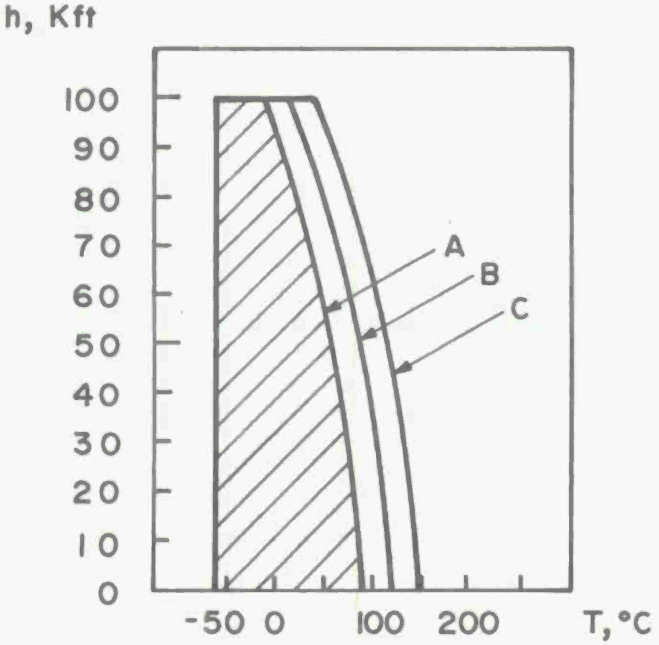


Fig.(C) Class 3 Equipment

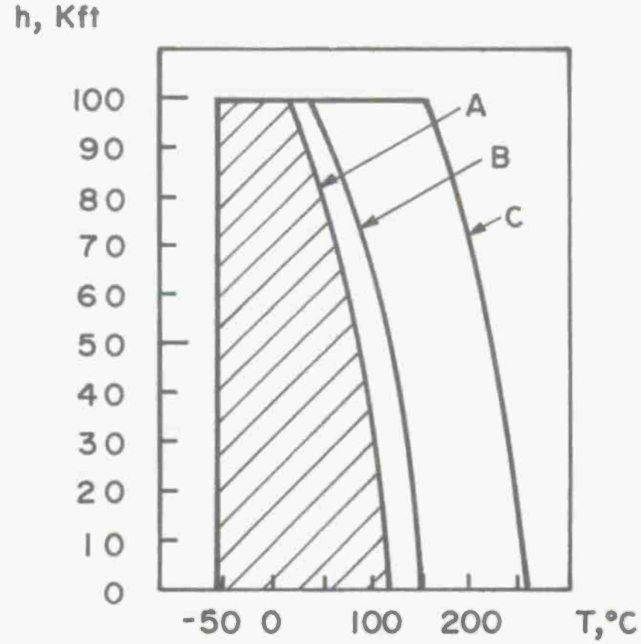
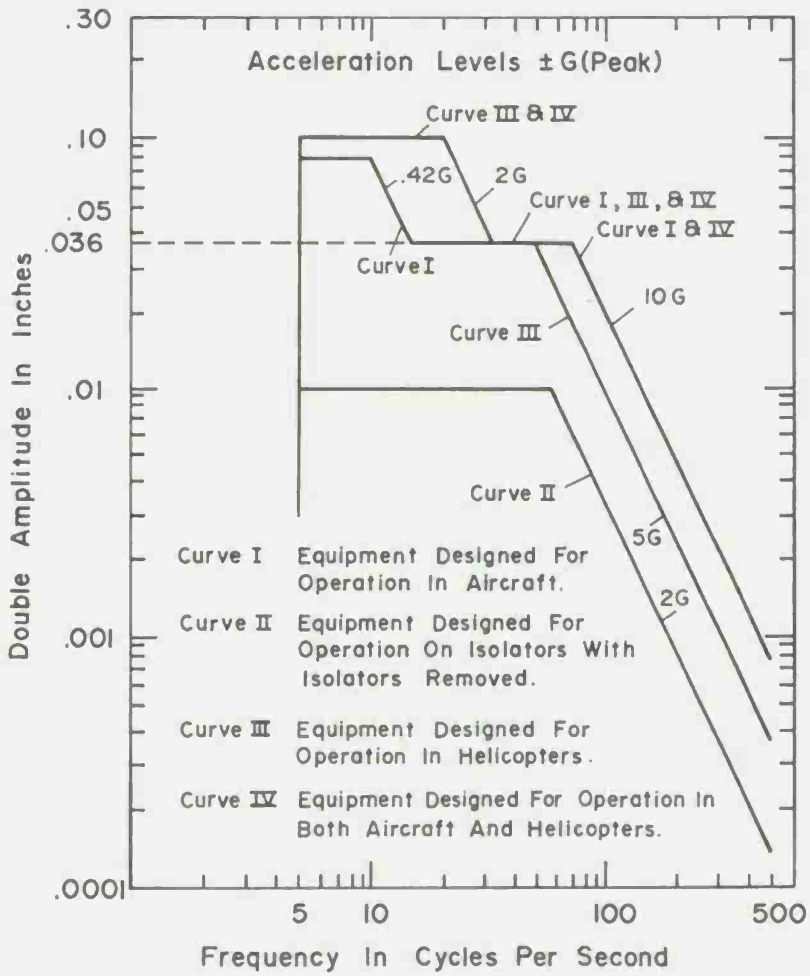


Fig.(D) Class 4 Equipment

Note: Refer To Table 3-3 For Use Of A,B,C

Fig. 3-4 TEMPERATURE ALTITUDE PROFILES FOR AVIONIC EQUIPMENT



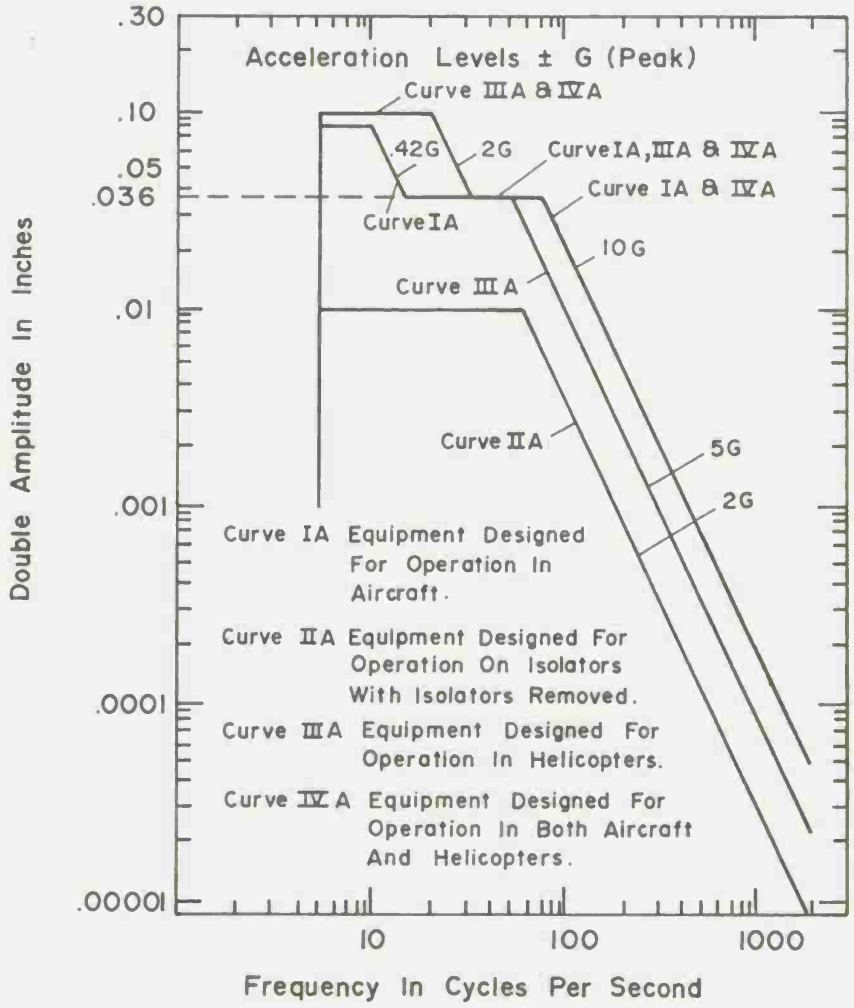


Fig. 3-5 VIBRATION REQUIREMENTS FOR AVIONIC EQUIPMENT

to vibration within the frequency range and amplitude as shown on Figure 3-5 and specified in the detail equipment specification.

(8) Equipment normally mounted on isolators must operate satisfactorily with isolators removed when subjected to vibration within the frequency range and amplitude as shown on curve II or IIA of Figure 3-5.

(9) Console controls located in the cockpit area shall conform to curve I or IA, except that the amplitude shall not exceed 5 g.

(10) Equipment (with vibration isolators in place, if any) should not suffer damage or subsequently fail to provide the performance specified in the detail equipment specification when subjected to 18 impact shocks of 15 g, consisting of three shocks in opposite directions along each of three mutually perpendicular axes, each shock impulse having a time duration of 11 ± 1 milliseconds. The maximum "g" shall occur at approximately 5½ milliseconds.

(11) With excursion stops or bumpers in place and with maximum rated load applied in a normal manner, the mounting base, individual isolators, or other attaching devices must be capable of withstanding at least 12 impact shocks of 30 g, consisting of two shocks in opposite directions along each of three mutually perpendicular axes. Each shock impulse shall have a time duration of 11 ± 1 milliseconds. The "g" value is to be within ± 10 percent. Maximum "g" value shall occur at approximately 5½ milliseconds. Bending and distortion are permitted; however, there shall be no failure to the attaching joints and the equipment of dummy load shall remain in place.

(12) The equipment shall withstand, in both an operating and non-operating condition, exposure to sand and dust particles as encountered in operational areas of the world.

(13) The equipment must withstand, in both an operating and non-operating condition, exposure to fungus growth as encountered in tropical climates. Overall spraying of the equipment must not be necessary to meet this requirement.

(14) The equipment must withstand, in both an operating and non-operating condition, exposure to salt-sea atmosphere.

(15) The equipment must not cause ignition of an ambient-explosive-gaseous mixture with air when operating in such an atmosphere.

This, in brief, is a representative overview of the avionics environment, and the severe operational conditions under which airborne electronic equipment must perform reliably and consistently over its operational life.

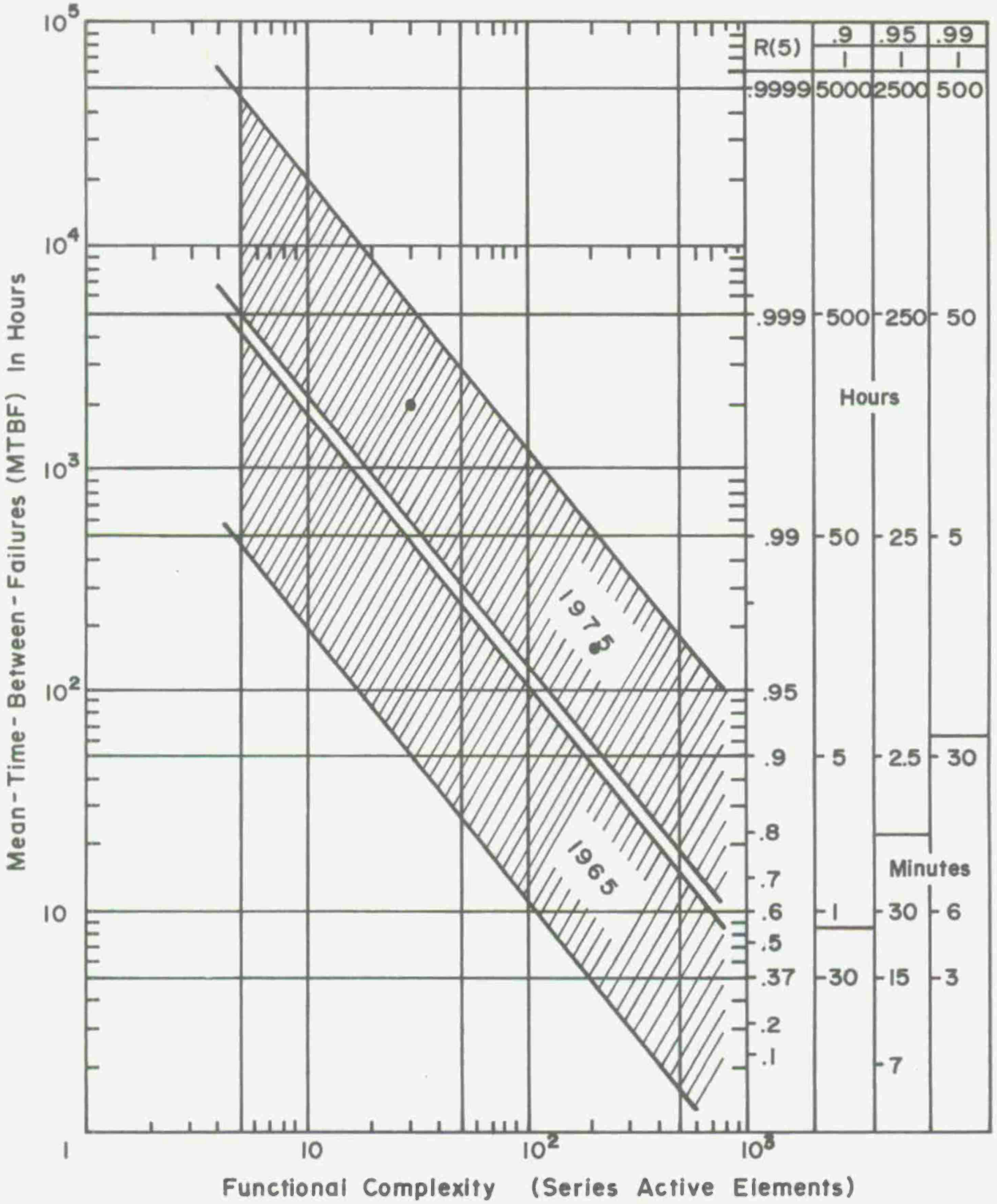
3.3 Equipment Reliability State-of-the-Art

Figure 3-6 is abstracted from the familiar chart of MIL-STD-756. The graphical portrayal of the reliability situation around 1965 gives the MTBF of a number of different analog type avionic equipments. The MTBF data was obtained from operator and pilot observations.

It is interesting to make a comparison of the then prevailing vacuum tube technology operational in the early 1960's, relative to the predominantly solid state technology available today. The comparison indicates that, in the area of low to medium power signal level application, the 1975 technology has undergone approximately an order of magnitude improvement in inherent reliability.

A bold extrapolation based on this situation thus suggests that the equipment reliability curve for 1975 be shifted up by one order of magnitude as shown in Figure 3-6.

As rough reference points to describe functional complexity, the following series active element counts would be representative of avionic equipments at opposite ends of this spectrum:



Note: An Active Element Is Defined As A Device Which Controls Or Converts Energy. A Typical Example Would Be A Transistor And Associated Circuitry.

Fig. 3-6 AVIONICS EQUIPMENT RELIABILITY (ANALOG)

	Functional Complexity (Series Active) Elements	Predicted MTBF (Hrs)
Multimode Radar	200	160
VHF Trans/Rcvr	30	2000

These two points are plotted on the equipment reliability trendline for 1975.

3.4 Summary and Conclusion: 1975 Avionics Trends

The dialogue of this section has been conducted within the context of trends. An attempt to predict the exact makeup of future generation avionics suites has been avoided. The justification for this position is clear if one considers that the designers of the 1950's could not have visualized many of the avionic developments that evolved in the 1960's, for example, the Wild Weasel electronic warfare system, or the laser seeker trackers and smart bombs which began appearing at the end of that decade. What has been highlighted here, then, are trends--trends which are examplified by the current avionics on the F-15, F-16, B-1, et al. The immediate overview and its near-term projection is approximately as shown in Table 3-1.

Technology today has evolved along the line from vacuum tube to transistor, and from discrete to integrated circuitry. Ramifications of this evolution are most evident in the digital area which has seen the rapid development and widespread use of full size integrated circuit digital computers and microprocessors. From the point of view of avionics, these devices appear to have arrived in time to handle the resultant complexity caused by the drive for ever increasing avionic systems performance. It is a major fact, that has been witnessed by avionics system evolution over the past two decades, that the ever-increasing drive for performance has negatively impacted on the issues of complexity, reliability and cost. The trade-off between the first two factors is indicated in Figure 3-6. More will be said about the last factor below. The following paragraphs comment first on the ability of digital computers and microprocessors to handle the resultant complexity. The next two paragraphs then deal with the ability of the new integrated-circuit technology to address the issues of reliability and cost.

Relative to the issue of complexity, the question that is being raised today is whether new aircraft integrated avionics systems should use a centralized multiprocessor to perform all or most of the individual subsystem computer functions, or whether there should be distributed computation facilities with a central executive computer to direct the operations. A point that may decide this issue, and one that is becoming increasingly more important today, is the problem of computer software. Ideally, avionics mission software should be easy to structure and document, inexpensive to modify and independent of the specific computer or sensor hardware being used. In this regard, system development trends could be adversely affected if avionics software proves to be cost-prohibitive and unmanageable.

Relative to the issue of reliability and cost, a question that is currently under review is whether future avionics equipment should be constructed from a family of standard electronic modules (SEM). Potential benefits of adopting standard modules are indicated by the Navy experience with the standard hardware program (SHP).

In this program, standard modules today appear to be showing failure rates of only 0.1 to 0.01 per million operating hours, and 80% of the present catalog of standard modules sell for under $60. However, there are also other points to consider here. One of the more basic ones has to do with the increased weight/volume penalty that modularization will impose (which may thus place a limit on performance growth) and bears on the question of whether the electronics technology has reached a sufficient level of maturity to be ready for standardization (digital type functions). It is easy to recall that in the early 1950's the subminiature vacuum tube was the smallest active-element electronic device. Soon thereafter, the transistor began making its appearance in military electronics, and by the late 1950's, a micromodule program would have been based on transistor technology. Subsequently, in the early 1960's, a transistor micromodule program would in turn have been made obsolete by the emerging microcircuit development. A decade since then has seen a 100:1 increase in the number of active elements that can be fabricated on a single semiconductor chip. It is not clear whether this trend is to continue into the next decade.

In the final analysis, however, the overriding factor may turn out to be what is increasingly becoming recognized as a way of life. It is that the driving force today can no longer be determined solely by the need for increased performance. Rather, it is becoming more responsive to the economic pressure to reduce acquisition and life-cycle costs. In this regard, it might be possible to greatly improve reliability and control and reduce costs by going to a standard module philosophy. It might work as follows. The widespread use and availability of SEM's would tend to result in low module costs. Widespread availability of SEM's would, in turn, tend to reduce the time required to design and build prototypes of new avionics systems and speed the transition into production. Availability of low cost SEM's in the field might then make it economically sensible to discard rather than to fault isolate and repair. In turn, a discard-on-failure maintenance concept would tend to reduce the training and skill levels required for maintenance. It would also ease the perennial logistics problem of obtaining replacements for devices no longer being manufactured. The SEM's in use would be functionally equivalent even though they might represent different generations of technology.

This then seems to be a fair representation of some of the major issues and circumstances that surround the state of avionics today.

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Section 4

RELIABILITY DESIGN DATA

4.1 Design to Maximize Inherent Reliability

4.2 Design to Minimize Reliability Degradation During Production and Use

4.3 Design to Cost

SECTION 4

RELIABILITY DESIGN DATA

During a period of high cost and rapid inflation, the key to an effective military system is the achievement of a balance between performance, reliability and other system factors at a minimum cost. The key to achieving this balance hinges on the realization that total cost of ownership is driven by system attributes apart from strict performance requirements. Reliability is one such attribute. Poor reliability (and the factors which cause it) result in high field-support cost and, consequently, high cost of ownership. The interrelationship among the system parameters which give rise to design balance are depicted in Figure 4-1. The figure shows that the various parameters for performance, R, M, and cost are trade-off variables to arrive at "design to" target goals which represent a balanced design.

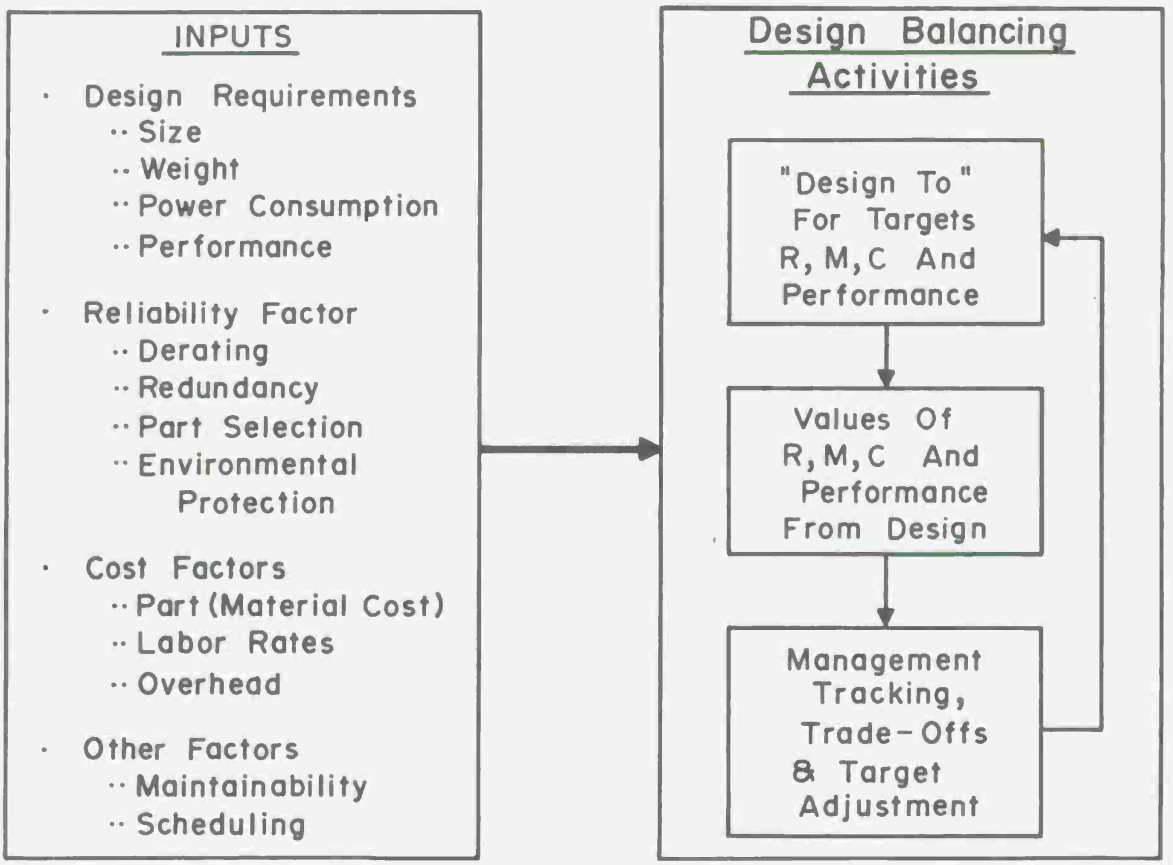


Fig. 4-1 DESIGN BALANCING ACTIVITIES

This section of the handbook emphasizes the "design to" philosophy in terms of specific reliability and cost guidelines which can be applied during design. Included are three major subsections:

(1) "Design to" Maximum Inherent Reliability, paragraph 4.1.

(2) "Design to" Minimize Reliability Degradation During Production and Use, paragraph 4.2

(3) "Design to" Cost, paragraph 4.3.

Section 4.1

DESIGN TO MAXIMIZE INHERENT RELIABILITY

4.1 Design to Maximize Inherent Reliability

4.1.1 Part Selection and Control

A diversified complement of electronic parts is available to structure modern military electronic systems. These parts constitute the building blocks from which systems are fashioned and, as such, greatly impact hardware reliability. Since the reliability of the end item is dependent upon these building blocks, the importance of selecting and applying the most effective parts cannot be overemphasized.

The task of selecting, specifying, assuring proper design application and, in general, controlling parts used in complex electronic systems is a major engineering task. Part selection and control is a multidisciplinary undertaking involving the best efforts of component engineers, failure analysts and reliability engineers as well as design engineers. Numerous controls, guidelines and requirements must be formulated, reviewed and implemented during the development effort. Table 4-1 presents a simplified list of the ground rules and activities needed to assure that this task is adequately considered. The subsections which follow provide detailed information, data and specific guidelines for the general ground rules listed in Table 4-1. Subsection 4.1.1.1 covers part control; subsection 4.1.1.2 provides specific part selection data and guidelines as they apply to each generic part classification and subsection 4.1.1.3 covers part screening.

4.1.1.1 Part Control

Part control activities comprise a large segment of the total effort for part selection, application and procurement. The effort encompasses tasks for standardization, approval, qualification and specification of parts which meet performance, reliability and other requirements of the evolving design. This subsection of the handbook provides further details with regard to these control tasks, indicates their importance within the part selection process and provides appropriate design guidance. Electronic parts that comprise any electronic equipment constructed for military purposes are under the cognizance of the Military Parts Control Advisory Group, located in the Directorate of Engineering Standardization at the Defense Electronics Supply Center (DESC). This group

Table 4-1 GROUND RULES FOR PART SELECTION AND CONTROL

a) Determine part type needed to perform the required function and the environment in which it is expected to operate.

b) Determine part criticality.

- Does part perform critical functions (i.e., safety or mission critical)?
- Does part have limited life?
- Does part have long procurement lead time?
- Is the part reliability sensitive?
- Is the part a high cost item or does it require formal qualification testing?

c) Determine part availability.

- Is part on a Preferred Part List?
- Is part a Standard MIL item available from a qualified vendor?
- What is normal delivery cycle?
- Will part continue to be available throughout the life of the equipment?
- Is there an acceptable in-house procurement document on the part?
- Are there multiple sources available?

d) Estimate expected part stress in its circuit application.

e) Determine reliability level required for the part, in its application.

f) Determine the efficiency of burn-in or other screening methods in improving the part's failure rate (as required).

g) Prepare an accurate and explicit part procurement specification, where necessary. Specifications should include specific screening provisions, as necessary to assure adequate reliability.

h) Determine actual stress level of the part in its intended circuit application. Include failure rate calculations per MIL-HDBK-217B.

i) Employ appropriate derating factors consistent with reliability prediction studies.

j) Determine need for nonstandard part and prepare a request for approval as outlined in MIL-STD-749 or MIL-STD-891.

promotes standardization in part selection and application. By using standard parts in new equipment design and development programs, much time and effort can be saved while obtaining better equipment performance in addition to simpler and better logistics support.

DESC promotes usage of standard parts and manages standardization problems for parts which are initially characterized as nonstandard but whose repetitive usage makes their standardization necessary.

DESC, as DoD's standardization manager, works closely with the military services and industry in developing an effective standardization program for new systems.

Therefore, the general rule for part selection is that wherever possible, standard devices should be used. Standard devices may be defined as those which by virtue of systematic testing programs and a history of successful use in equipment have demonstrated their ability to consistently function within certain specific electrical, mechanical and environmental limits and, as a result, have become the subject of military (MIL) specifications. MIL specifications which thoroughly delineate a part's substance, form and operating characteristics exist, or are in preparation, for practically every known type of electronic component. Military Standards exist which cover the subject of testing methods applicable to MIL-specified components. For example:

MIL-STD-202, Test Methods for Electronic Parts
MIL-STD-750, Test Methods for Semiconductor Devices
MIL-STD-883, Test Methods for Microelectronic Devices.

In addition, Military Standards exist which list by MIL designation those parts or devices which are preferred for use in military equipment. For example:

MIL-STD-1562, List of Standard Microcircuits
MIL-STD-701, List of Standard Semiconductors
MIL-STD-199, Selection and Use of Resistors
MIL-STD-198, Selection and Use of Capacitors.

Brief descriptions of these standards are given in the bibliography section of this handbook (Appendix B).

In conjunction with part standardization, nonstandard part approval must be considered. Nonstandard part approval is comprised of activities to document and secure authorization to use the part in the system. Military-STD-891 outlines the functions of a Part Advisory Group or a Part Control Board operating under both government and contractor cognizance and which provides the necessary mechanism for securing approval of nonstandard parts.

The qualification of nonstandard parts should include detailed and formal submittal of data to support approval request. This data must be: (1) statistical test data, (2) analytical data for components that are similar to a standard part, or (3) a combination of statistical and analytical data. (Note: Those components that require formal statistical test data for qualification should be identified as critical items.)

The selection process should include design evaluation, reliability history review, construction analysis, failure mode and effects analysis and cost effectiveness studies as necessary. The control effort should include the development of meaningful procurement specifications which, when completed, reflect a balance between design requirements, QA and reliability needs consistent with apportionment studies and vendor capabilities, and which cover:

lot acceptance testing,
QA provisions (including incoming inspection),
qualification testing, if required.

A well controlled part program involves establishing a vendor control program, audits of vendor processes, the establishment of source inspection, where applicable, and the preparation of associated documentation. The part control effort includes identifying all critical parts, equipment/components, and other items considered critical from any of the following standpoints:

- mission and safety sensitive (failure impacts mission success and flight safety, i.e., flight safety critical),
- reliability sensitive (from early R studies, apportionments, etc.),
- have limited life,
- are high cost items,

- have long procurement lead times,
- require formal statistical qualification testing.

Planning for critical item control must include controls for special handling, the identification of critical item characteristics to be inspected or measured during incoming inspection, material review procedures, traceability criteria and periodic audits. All items considered flight safety critical must be coded. Detailed documentation must be prepared that describes procedures, tests, test results, and efforts to reduce the degree of criticality of each item.

4.1.1.2 Part Selection Guidelines

This subsection presents reliability information to aid in the selection of electronic parts for a specific design application. Included are guidelines for:

(a) Microcircuits (paragraph 4.1.1.2.1)
(b) Semiconductors (paragraph 4.1.1.2.2)
(c) Resistors (paragraph 4.1.1.2.3)
(d) Capacitors (paragraph 4.1.1.2.4)
(e) Other Parts (paragraph 4.1.1.2.5)

4.1.1.2.1 Microcircuits

In general, there are two major classes of microcircuits:

Monolithic
Hybrid.

A monolithic microcircuit is characterized by a single silicon chip, suitably packaged and performing well-defined functions. This characterization encompasses varying degrees of complexity up to and including LSI and may include purely digital functions or linear applications. Monolithic microcircuits cover most forms of current technology, e.g., TTL, MOS, CMOS, etc.

In contrast, hybrid microcircuits result from combining various electronic, component, material and manufacturing technologies into miniature electronic interconnections and packaging. Normally, film circuits are combined with chip and discrete components on a substrate.

Integrated and complex monolithic circuits can be included within a hybrid.

Before deciding which class of microcircuit best meets the needs of a particular application, careful consideration should be given to construction, parameters, size, cost and reliability constraints as they relate to the specific design. Trade-off studies should be performed covering such factors as:

- Comparison of total costs. This includes development costs for each type plus cost of fabrication and testing.
- Comparison of circuit parameter requirements such as resistance tolerances, tracking, temperature coefficient, speed, voltage levels, and electrical isolation with the parameter limitations of monolithic and hybrid circuits.
- Comparison of package size requirements to the space available.
- Evaluation of circuit power dissipation and the thermal resistances of the packaged circuit to insure acceptable temperatures on the substrate.

For monolithic IC's, numerous standard devices (listed in MIL-STD-1562) are available from which selections can be made (see Appendix C). Because hybrids are essentially custom-made devices, a similar standardizing document does not currently exist. In recognition of the increasing usage of hybrid devices, the approach to reliable hybrids has been via test and inspection techniques. Military STD-883A (Test Methods for Microelectronic Devices) includes a section for internal visual inspection of hybrid devices (Method 2017 of MIL-STD-883A). Revisions to this standard which would establish additional test methods for hybrids are contemplated.

The selection of a specific microcircuit type is governed by the guidelines depicted in Table 4-2. As previously indicated, the expected reliability level of parts and of microcircuits in particular must be incorporated into the selection process. Appendix C contains a listing of integrated circuits taken from MIL-STD-1562 and represents devices which are considered to be standard and acceptable for use in military equipment.

Table 4-2 MICROCIRCUIT SELECTION GUIDELINES

1. MIL-STD-1562, List of Standard Microcircuits.
2. MIL-M-38510, Microcircuits, General Specifications For. This document defines screening per MIL-STD-883, "Test Methods and Procedures for Microelectronics".
3. Historical test data (similar application) or other engineering information and/or data that provides assurance that the device is sufficiently rugged and reliable for the application (e.g., previous use in Air Force equipment, comparable application, or GFE).
4. MIL-HDBK-175, "Microelectronic Device Data Handbook" (Application data).

NOTE: When a desired device is not covered by MIL-M-38510, a new specification or drawing should be prepared and coordinated with potential manufacturers of the device. To assist the contractor in these actions, the Department of Defense Reliability Analysis Center located at RADC, Griffiss AFB, Rome, New York, maintains a comprehensive up-to-date data base on environmental operating capabilities failure rates, failure modes and mechanisms, and fabrication techniques covering hybrid and monolithic microcircuits.

The failure rates included in Appendix C are only intended to be used as comparative guides to designers in the selection and application of microcircuits. These failure rates were calculated according to MIL-HDBK-217B prediction methods using generalized design and application assumptions.

In addition, Table 4-3 provides failure mode and rate information for digital and linear microcircuits. The information included in this table is intended to be used for comparing the reliability aspects of microcircuits and to aid in selecting the optimum device for a given

Table 4-3 APPLICATION NOTES FOR IC'S

Microcircuit Type	Application Notes	Failure information*	Failure rate Range ($F/10^6$ hrs)
DIGITAL		Failure indicators: mechanical anomaly (VIS) - 1% Opens (pin to pin) - 20% Shorts (pin to pin) - 22% Operation degradation - 57%	0.032-0.344
TTL	Standard: Intended for use in implementing logic functions where speed and power requirements are not critical. This family offers a full spectrum of logic functions in various packages. Typical gate power dissipation is 10 mW with a typical propagation delay time of 10 ns. These devices exhibit a fanout of 10 when driving other standard TTL devices usually used to perform general purpose switching and logic functions. Low Power: Employed in logic design where low power dissipation is the primary concern. These devices have a typical gate power dissipation of 1 mW with a typical propagation delay time of 30 ns. Typically, these devices will drive only one standard TTL device but exhibit a fanout of 10 when loaded by other low power devices. Low power generates less heat and therefore allows for greater board densities. Lower current levels also introduce less noise and reduce constraints on power supplies. High Speed: Used to implement high speed logic functions in digital systems. These devices employ a Darlington output configuration to achieve a typical propagation delay time of 6 ns. The typical gate power dissipation is 23 mW. These devices can drive up to 12 standard TTL devices and exhibit a fanout of 10 when driving other high speed devices. Commonly used in high speed memories and central processor units. Schottky: Used when ultra-high speeds are desired. These devices employ shallow diffusions and smaller geometries which lower internal capacitance to reduce delay time and sensitivity to temperature variation. Typical delay time is 3 ns and power dissipation is 19 mW. However, this power dissipation increases with frequency. These devices can drive 12 standard TTL devices and up to 10 Schottky devices. Noise immunity is reduced due to the nonsaturated switching operation. A ground plane is recommended for interconnections over 6 in. long and twisted-pair lines for distances over 10 in.	Constituent failure modes: Surface defects - 6% Oxide defects - 4% Diffusion defects - 2% Metallization defects - 50% Bond/wire defects - 13% Die attach bond - 11% Cracked die - 1% Package - 13%	0.032-0.180
CMOS	Used where low power is extremely desirable and high speeds are not essential. The typical power dissipation is 10 mW (at 10 kHz) and increases with frequency. Typical delay time is 50 ns. A typical fanout for CMOS loads is 50, while only 1 for standard TTL loads. Noise immunity is typically 1.5 V for CMOS compared to 0.4 V for standard TTL devices. This makes these devices useful in high noise environments. Handling precautions should be given consideration due to susceptibility to overstress from electrostatic discharge. Most commonly employed in medical electronics, calculators, watches, clocks and automotive systems. These devices are highly tolerant of power supply voltage variation and will operate anywhere in the range of 3 to 15 volts.	Constituent failure modes: Surface defects - 27% Oxide defects - 16% Diffusion defects - 9% Metallization defects - 25% Bond/wire defects - 15% Package - 8%	0.044-0.344

Table 4-3 APPLICATION NOTES FOR IC'S (Continued)

Microcircuit type	Application notes	Failure information*	Failure rate range ($F/10^6$ hrs)
ECL	Intended for use in digital systems requiring high switching speeds and moderate power dissipation. Typical propagation delay time is 2 ns and typical power dissipation is 25 mW. Operation requires a -5.2 V supply and properly terminated lines or control impedance circuit boards. The logic levels (-0.9 V and -1.7 V) are not as easily detected as those of TTL devices. Intended for use in high speed systems such as central processors, memory controllers, peripheral equipment, instrumentation and digital communications. A typical fanout is 15 when driving ECL devices.	Prevalent failure modes: Bond die attach Metallization defect Bond/wire defects (Failure percentages not available)	0.056-0.088
Programmable ROM	Used in systems having nonvolatile memory requirements. Nichrome fusible links allow for custom field programming to aid system prototyping. Programming procedures must be closely regulated to prevent fuse "Grow-Back". Useful in implementing hardware algorithms and microprogramming.	Learning factor ("L) is especially applicable due to additional step required for programming. Prevalent failure modes: Metallization defect Surface/oxide defect Package defects (Failure percentages not available)	0.280
LINEAR	Intended for use in signal amplification detection and transmission, and voltage regulation. Large power dissipation limits packaging density and requires consideration of thermal design parameters. Extensively used in communications, controls, instrumentation and information systems.	Failure indicators: mechanical anomaly (VIS) - 1% Opens (pin to pin) - 9% Shorts (pin to pin) - 7% Operational degradation - 83% Constituent failure modes: Surface defects - 54% Oxide defects - 2% Diffusion defects - 2% Metallization defects - 18% Bond/wire defects - 8% Die attach bond - 9% Cracked die - 1% Package - 6%	0.096-0.208

*Failure indicators are device failure modes which identify the failure condition by visual, electrical or mechanical measurements without performing any destructive analyses. For the purpose of accumulating statistics, pin-to-pin testing should be performed on failures first, to establish an open or short and verify the failure, which then is classified as an operational degradation. Mechanical anomaly occurs when a visual or mechanical defect exists and electrical performance is still within specifications.

The operational degradation failure indicator subclassifications are as follows:

Digital:
- Stuck High
- Stuck Low
- Output Unstable/Erratic
- No Output Signal (only refers to cases where the failure cannot be classified as stuck high or low and there is no output response to an input signal)
- Parameter out of tolerance

Linear:
- Hardover Positive (latched/saturated)
- Hardover Negative (latched/saturated)
- Output Unstable/Fluctuates/Erratic
- Output Clipped
- Latched/Saturated (other than at extremes)
- No Output Signal (refers only to cases where the failure cannot be classified in any of the above categories and there is no output response to an input signal)
- Parameter out of tolerance

Constituent failure modes identify the constituent of the microcircuit and its defective condition which resulted in the failure indicator.

The relative occurrence data presented was derived from malfunction reports collected industry-wide by the Reliability Analysis Center. The qualification and screening tests of MIL-M-38510 for JAN parts may shift these distributions to those modes not easily detected. For example, the high incidence of metallization defects in TTL may be reduced by appropriate emphasis on pre-cap visual inspection and metallization process control.

design application. The table lists the device class and type, application notes, failure information and failure rate range. The information presented in Table 4-3, when modified to eliminate the effects of packaging, is applicable to IC chips used within hybrid microcircuits. The range of failure rates listed for each type was computed from MIL-HDBK-217B using values for adjustment factors ranging from worst case to optimum application conditions.

4.1.1.2.2 Semiconductor Devices

Expanding technology, widespread use and the economics of large volume production have resulted in a proliferation of discrete semiconductor devices. There exists a wide variety of functional classifications based upon electrical characteristics, such as low or high power, switching time, internal capacitance, and forward current, available to the designer. In addition, there are several categories relating to semiconductor device material and its physical configuration. In total, there are thirty-five officially recognized functional and constructional classifications of semiconductor device types. These types can be found in MIL-STD-701.

The selection of a specific semiconductor device is governed by the guidelines depicted in Table 4-4. As shown in this table, the governing specification for discrete semiconductor devices is MIL-S-19500. This basic document and its appended detailed specification sheets establish the general and specific requirements including definitions, abbreviations and symbols, electrical characteristics, electrical, mechanical and environmental requirements, styles, test methods, quality assurance provisions, and qualification and inspection procedures for all semiconductor devices.

MIL-STD-701 provides a listing of those MIL-S-19500 devices which are considered to be standard or are preferred for use in DoD equipments. Failure rates for these devices can be calculated in accordance with MIL-HDBK-217B.

Table 4-5 provides additional information for discrete semiconductor devices. Included in this table are typical applications for the type of semiconductor listed, a cross referencing of standard types derived from MIL-STD-701 and a list of failure rates against each semiconductor type.

Table 4-4 SEMICONDUCTOR SELECTION GUIDELINES

1. MIL-STD-701, "Lists of Standard Semiconductor Devices".
2. MIL-S-19500E, "Semiconductor Devices, General Specification For" ("JANTXV" or "JANTX" devices).
3. Historical Test data (similar application) or other engineering information and/or data that provides assurance that the device is sufficiently rugged and reliable for the application (e.g., previous use in military equipment).

NOTE: In selecting semiconductor devices it is important to remember that in MIL-S-19500 the values specified for "ratings", "maximum ratings", or "absolute maximum ratings" are based on the "absolute system" and are not to be exceeded under any service or test conditions. These ratings are limiting values beyond which the serviceability of any individual semiconductor device may be impaired. It follows that a combination of all the absolute maximum ratings cannot normally be attained simultaneously. Combinations of certain ratings may be obtained only if no other single maximum rating is exceeded. Unless otherwise specified, the voltage, current and power ratings are based on continuous dc power conditions at free air ambient temperature of $25^{o} \pm 3^{o}C$. For pulsed or other conditions of operation of similar nature, the current, voltage and power dissipation ratings are a function of time and duty cycle.

Table 4-5 APPLICATION AND SELECTION GUIDELINES FOR SEMICONDUCTORS

Semiconductor type	Application	MIL-STD-701 Table No.	Failure rate $F/10^6$ hrs
Diodes, silicon general purpose	Low power rectifiers	I	0.68
	Axial lead power rectifiers	II	0.68
	Power diodes	III	0.68
	High voltage rectifier assemblies	IV	0.68
	Switching diodes	V	0.68
	Multiple diode arrays	VI	0.68
Diodes, silicon voltage reference	Voltage reference diodes	VII	0.85
	Low level forward-voltage reference diodes	VIII	0.85
	Voltage regulator diodes	IX	0.85
	Current regulator diodes	XIV	0.85
Rectifiers, silicon controlled	Thyristors	XIX	0.90
		XX	0.90
Diodes, silicon microwave detector microwave mixer	Fast recovery	XI	8.1
	Detector	X	12.0
	Mixer	X	16.0
Diodes, germanium microwave detector	Tunnel diodes	XII	1.7
	Detector	X	35.0
	Mixer	X	61.0
Diode, varactor	Voltage variable capacitor	XIII	8.1
Transistor, silicon NPN	Low power and switching	XXI	0.98
	High power > 5 w	XXIII	0.98
	Radio frequency	XXV	0.98
	Darlington	XXVIII	0.98
	Dual transistor, differential amplifier	XXVI	1.96
	Low power chopper	XXXII	0.98
	Low power dual emitter chopper	XXXIII	0.98
Transistor, silicon PNP	Low power and switching	XXII	1.6
	High power > 5 w	XXIV	1.6
	Radio frequency	XXV	1.6
	Dual transistor, differential amplifier	XXVI	3.2
	Low power chopper	XXXII	1.6
Transistor, silicon, dual	Complimentary NPN/PNP	XXVII	2.58
Transistor, silicon, FET	Field effect N channel	XXX	2.7
	Field effect P channel	XXX	2.7
	Field effect, dual unitized N channel	XXXI	5.4

Because of the proliferation of device types, proven technology and device standardization, semiconductor failure modes are well established and can be effectively controlled during processing. Consequently, failures usually occur on a random basis during normal operation within the useful life of the device. Table 4-5 includes failure rate information for each semiconductor type. The failure rates shown were taken from Section 3.0 of MIL-HDBK-217B under the airborne inhabited environment.

4.1.1.2.3 Resistors

As a generic class of electronic devices, resistors have been well documented by MIL specifications and standards. Consequently, a selection from among a variety of available standard types and styles can be made. For economic reasons, standard resistors are normally produced in large productions runs, making the selection of standard devices even more attractive. Note, however, that there are exceptions. Extremely tight-tolerance fixed resistors and certain precision type variable resistors, which require a unique output voltage curve, taps or stacking configuration, may be difficult or expensive to procure or possess questionable reliability. Resistor selection is governed by the guidelines given in Table 4-6.

Table 4-6 RESISTOR SELECTION GUIDELINES

1. MIL-STD-199, "Resistors, Selection and Use of"
2. The 39000 series of Established Reliability Military Specifications.
3. Historical test data (similar application) or other engineering information and/or data that provides assurance that the device is sufficiently rugged and reliable for the application (e.g., previous use in military equipment, comparable application or GFE).

NOTE: For selecting particular resistors for specific applications, the qualified product list should be consulted for a list of qualified sources prior to procurement commitments.

In addition to these selection criteria, Table 4-7 presents further considerations to be employed when selecting resistors. The resistor types shown, together with their appropriate MIL specification style designations and applicability to new design, reflect the provisions of MIL-STD-199.

The generic failure rates given in the table are taken from MIL-HDBK-217B and are provided for purposes of comparison. The failure rates reflect an airborne inhabited environment and an M quality level.

4.1.1.2.4 Capacitors

Similar to resistors, capacitors have been thoroughly investigated for operational characteristics, identified for form, function and applicable ratings, and documented for procurement, test, qualification approval, quality control and standardization within MIL specifications and standards. Like resistors, they are normally produced in large production runs which tends to keep unit pieces low priced and promotes standardization. Capacitor selection is governed by the guidelines given in Table 4-8.

Table 4-8 CAPACITOR SELECTION GUIDELINES

1. MIL-STD-198, "Capacitors, Selection and Use of".
2. The 39000 series of Established Reliability Military Specifications.
3. Historical test data (from similar application) or other engineering information and/or data that provides assurance that the device is sufficiently rugged and reliable for the application (e.g., previous use in military equipment, comparable application, or GFE).

NOTE: In selecting particular capacitors for specific applications, the qualified product list should be consulted for a list of qualified sources prior to procurement commitments.

Table 4-7 APPLICATION AND SELECTION GUIDELINES FOR RESISTORS

Military specifications	Type	Styles	Application notes	Failure Modes	Failure rate ($F/10^6$ hrs)
MIL-R-11	Composition insulated	Inactive for new design. Use MIL-R-39008			
MIL-R-26	Wire-wound (power type)	RW29 RW37 RW31 RW38 RW33 RW47 RW35 RW57	See data on MIL-R-39007		0.33
MIL-R-93	Wire-wound (accurate)	Inactive for new design. Use MIL-R-39005			
MIL-R-10509	Film (high stability)	RN75	See data on MIL-R-55182		0.023
MIL-R-11804	Film (power type)	RD60 RD65 RD70	Use where power dissipation equivalent to MIL-R-39007 are required and where ac performance must be considered. RD60, RD65, and RD70 are considered uninsulated.	SHORTS--Humidity or salt air can cause shunt paths on surface of resistor and shorting between spirals. OPENS--Can be caused by mechanical damage. Operation at RF above 100 MHz may produce inductive effects on spiralled units.	1.3
MIL-R-18546	Wire-wound power type (chassis mounted)	RE77 RE80	See data on MIL-R-39009		0.65
MIL-R-22684	Film (insulated)	Inactive for new design. Use MIL-R-39017			
MIL-R-39005	Wire-wound (accurate) established reliability	RBR52 RBR56 RBR53 RBR57 RBR54 RBR71 RBR55 RBR72	Styles RBR52, 53, 54, 55, 55, and 71 are preferred for new design. Preferred resistance tolerances are ± 0.1% and ± 1.0%.	SHORTS--Application of over-voltage can cause insulation breakdown between windings. OPENS--Resistors employ plastic or ceramic bobbins which are subject to mechanical damage, resulting in open windings. Operation over 50 kHz can produce inductive and intra-winding capacitive effects.	0.15
MIL-R-39007	Wire-wound (power type) established reliability	RWR74 RWR81 RWR78 RWR84 RWR80 RWR89	Use for large power dissipation where ac performance is not vital (e.g., as voltage dividers, or bleeders in power supplies). Satisfactory for use at frequencies up to 20 kHz even though the ac characteristics are controlled. The use of tapped resistors should be avoided; the insertion of taps weakens the resistor mechanically and lowers the effective power rating. Resistors are not suitable for use above 50 kHz.	SHORTS--Rarely occur, but can happen due to intrawinding insulation breakdown. OPENS--Usually occur due to mechanical damage suffered by the resistor or from winding burnout due to the wattage rating or the rated continuous working voltage being exceeded.	0.066

Table 4-7 APPLICATION AND SELECTION GUIDELINES FOR RESISTORS (Page 2)

Military Specifications	Type	Styles	Application Notes	Failure Modes	Failure rate ($F/10^6$ hrs)
MIL-R-39008	Composition (insulated)	RCR05 RCR07 RCR20 RCR32 RCR42	Use for general applications where initial tolerance needs to be no tighter than ± 5% and long term stability under fully rated operating conditions needs to be no better than ± 15%. Resistance increases up to 20% during storage in humidity. Operation of the resistor at rated load will drive out the noisture and bring the resistor value back to within tolerance.	Both shorts and opens very rarely occur unless resistor is so over-loaded or overheated as to cause the phenolic case or thermo-setting binder material to carbonize. In high impedance circuits, the failure mode is generally a short; in low impedance circuits, the failure mode is open. High "JOHNSON" noise levels are present in resistor values above 1.0 megohm. DRIFT--RF will produce capacitive effects end-to-end. Operation at VHF or higher frequency reduces effective resistance due to dielectric losses (the "Boello" effect).	0.0048
MIL-R-39009	Wire-wound (power type) established reliability	RER40 RER60 RER45 RER65 RER50 RER70 RER55 RER75	Use where a lower tolerance and a greater power dissipation is required for a given unit size than is provided by MIL-R-39007 resistors, and where ac performance is not critical. The power dissipating capacity of these resistors is dependent upon the area of heat sink upon which is it mounted.	SHORTS--May occasionally occur due to intra-winding insulation breakdown. OPENS--May occasionally occur due to damage to the winding, poor winding to terminal connection, etc., suffered during fabrication.	0.13
MIL-R-39017	Film (insulated) established reliability	RLR05 RLR07 RLR20 RLR32 RLR42	Resistors have semi-precision characteristics and small sizes. The sizes and wattage ratings are comparable to MIL-R-39008 units and stability lies between MIL-R-39008 and MIL-R-55182. Full power operating temperature should not exceed 70°C. Resistance-temperature characteristic is ± 200 PPM/°C.	SHORTS or OPENS may occur if resistor is poorly fabricated or over-loaded in application. Operation at RF above 100 MHz may produce inductive effects on spiral-cut types.	0.02
MIL-R-55182	Film established reliability	RNR50 RNR55 RNR60 RNR65 RNR70	Use where high stability, long life, reliable operation and accuracy are required. Resistors are particularly suited for high frequency applications. Application examples include: high-frequency, tuned circuit loaders, television side-band filters, rhombic antenna terminators, radar pulse equipment, and metering circuits.	SHORTS--May occasionally occur because of protuberances on adjacent resistance spirals. OPENS--May occasionally occur due to non-uniform spirals resulting in a too-thin resistance path. Operation at 400 MHz and above will result in resistance decrease due to shunt capacitance effects.	0.023

Table 4-7 APPLICATION AND SELECTION GUIDELINES FOR RESISTORS (Page 3)

Military Specifications	Type	Styles	Application notes	Failure modes	Failure rate ($F/10^6$ hrs)
VARIABLE RESISTORS					
MIL-R-19	Wire-wound (low operating temperature)	RA20 RA30	Use for noncritical, low power, low frequency applications where the characteristics of wirewound devices are more desirable than those of composition. Common applications are bias controls and voltage dividers. Wattage rating depends upon the size and type of heat sink unit is mounted on. Resistors have high inductance between windings.	Variable resistors as a class of components share many common failure modes: 1. Wire-wound units are inductive, winding-to-winding, causing resistance drift and affecting circuitry accuracy. 2. Wire-wound units suffer shorts between winding loops due to insulation breakdown or contaminants which bridge the insulation. 3. Windings will rupture with sufficient wear by the wiper arm, resulting in an open circuit. 4. All variable resistors can suffer movement of the wiper on the resistance element as the result of shock or vibration. In critical applications, the resultant change of the output voltage can constitute a "failure" of the resistor. 5. Non-wire-wound units become noisier with wear life, and will suffer resistance change due to humidity. 6. Power ratings for all variable resistors are based upon the engagement of the maximum resistance by the wiper. Excessive currents can be drawn when less-than-maximum resistance is engaged, resulting in a burn-out of the resistance element.	6.4
MIL-R-22	Wire-wound (power type)	RP05 RP06 RP10 RP15 RP20 RP25 RP30	Use in such applications as motor speed controls; lamp dimming; heater and oven controls; potentiometric uses; applications where voltage or current variation is required, such as voltage-divider or bleeder circuits.		6.0
MIL-R-94	Composition (insulated)	RV4 RV6	Rate for full-load operation at 70°C, otherwise SEE DATA ON MIL-R-23285.		20.0
MIL-R-12934	Wire-wound precision	RR0900 RR1000 RR1100 RR1300 RR1400 RR2000 RR2100 RR3000	Use in applications requiring close conformity of the electrical output (in terms of applied voltage) to the angular position of the wiper arm on the resistance element. This functional conformity (whether producing a linear or nonlinear output curve with shaft rotation) is available in tolerances ranging from 0.025% through 1.0%. Power rating is dependent on the size and type of heat sink upon which resistor is mounted.		5.8
MIL-R-23285	Non-wire-wound	RVC5 RVC6	Use where initial setting stability is not critical and long term stability needs to be no better than ± 20%. Rated for full load operation at 125°C.		6.7

Table 4-7 APPLICATION AND SELECTION GUIDELINES FOR RESISTORS (Page 4)

Military specifications	Type	Styles	Application notes	Failure modes	Failure rate ($F/10^6$ hrs)
MIL-R-22097	Non-wire-wound (lead-screw actuated)	RJ12 RJ24 RJ22 RJ26 RJ50	See data on MIL-R-39035	Variable resistors as a class of components share many common failure modes. (see preceding page.)	9.5
MIL-R-27208	Wire-wound (lead-screw actuated)	RT26	See data on MIL-R-39015		0.70
MIL-R-39002	Wire-wound semi-precision	RK09	Use where the precision needed is better than that supplied by MIL-R-19 units and less than that supplied by MIL-R-12934 units. Power rating is dependent on size and type of heat sink upon which resistor is mounted.		6.4
MIL-R-39015	Wire-wound (lead-screw actuated) established reliability	RTR12 RTR22 RTR24	Use for matching, balancing, and adjusting circuit variables in critical applications. For extremely critical applications, use in conjunction with a fixed resistor, so that change in wiper setting due to shock or vibration limits output voltage change to a negligible minimum.		0.14
MIL-R-39035	Non-wire-wound (lead-screw actuated) established reliability	RJR12 RJR14	Same as MIL-R-39015		7.96

Table 4-9 presents additional considerations to be employed when selecting capacitors. The capacitor types shown, together with their appropriate MIL specification style designations and applicability to new design, reflect the provisions of MIL-STD-198.

The failure rates given in Table 4-9 have been provided for the sole purpose of demonstrating comparative reliability levels of the various capacitor types. These are generic failure rates taken from MIL-HDBK-217B.

4.1.1.2.5 Other Parts

The selection of the following devices are governed by the guidelines depicted in Tables 4-10 through 4-20 and Figure 4-2.

Electron Tubes (Table 4-10)

Inductive Devices (Table 4-11)

Relays (Table 4-12, 4-13 and 4-14)

Switches (Table 4-15, 4-16 and Figure 4-2)

Connectors (Table 4-17)

Microwave Devices (Table 4-18 and 4-19)

Cables (Table 4-20).

4.1.1.3 Part Screening

As discussed in Section 1 of this handbook, virtually all manufactured devices exhibit a life characteristic which may best be represented by the bathtub curve shown in Figure 1-1. This section deals with the first segment of the curve, namely, the "infant mortality" or the "early failure" period of the equipment's life. Experience shows that a newly constructed equipment fails more often during its early life (i.e., during assembly and testing) than later during use in the field.

This indicates that piece parts received from the supplier contain a certain number of weak devices which tend to fail during initial testing of subassemblies or complete equipments.

In order to eliminate the incipient failures from the manufacturing process, quality and screening tests can be employed. The quality tests

Table 4-9 APPLICATION AND SELECTION GUIDELINES FOR CAPACITORS

Military specification	Type	Styles	Application notes	Failure modes	Failure rate ($F/10^6$ hrs)
FIXED, GLASS AND MICA					
MIL-C-5	Mica dielectric	CM05 CM07 CM06 CM08	Inactive for new design. See MIL-C-39001		
		CM15 CM35 CM20 CM45 CM30 CM50	Use in circuits requiring precise, high-frequency filtering, bypassing and coupling. Use where close impedance limits are essential with respect to temperature, frequency and aging--such as in tuned circuits which control frequency, reactance, or phase. Use as padders in tuned circuits, as secondary capacitance standards, and for tuning of high frequencies. Capacitors have good stability and reliability.	Shorts can occur due to moisture absorption, or due to internal solder flow resulting from excessive heat generated during external lead-soldering. Opens usually result from rupture of weak internal connections due to vibration or shock.	0.06
MIL-C-10950	Mica dielectric	CB50 CB61 CB55 CB62 CB56 CB65 CB57 CB66 CB60 CB67	Intended for use at frequencies up to 500 MHz. Use in tuned circuits, and in coupling and bypassing applications in VHF and UHF circuits. Units have high reliability if properly protected from high ambient temperature and humidity conditions.	Capacitors are very susceptible to silver-ion migration, resulting in shorts. Migrations can occur in a few hours when capacitors are simultaneously exposed to dc voltage stress, humidity and high temperature.	0.93
MIL-C-23269	Glass dielectric	Inactive for new design. See MIL-C-23269.			
MIL-C-23269	Glass dielectric established reliability (FR: 1 to 0.001)	CYR10 CYR13 CYR15 CYR17 CYR20 CYR22 CYR30 CYR32	Capacitors should be used as substitutes for mica units in applications requiring known reliability and where the differences in temperature coefficient and dielectric loss are taken into account. They are stable in extreme environmental conditions, have long life (30,000 hrs and more) and are very satisfactory for use in missile-borne and space equipment. These physically-small units are resistant to high G loads, but are susceptible to damage from mild mechanical shocks. Therefore, they should be handled carefully. They exhibit a much higher Q over a wider capacitance range than mica dielectric units.	Degradation of dielectric crystalline structure can occur as the result of storage below $45^{\circ}C$. The capacitance will decrease with the decrease in dielectric constant and the unit will drift out of tolerance. Opens are frequently due to poor connections of leads to the plates or mechanical damage to the capacitor. Over-heating during external soldering can result in internal solder flow (shorts) or rupture of internal solder connection (opens).	0.021

Table 4-9 APPLICATION AND SELECTION GUIDELINES FOR CAPACITORS (Page 2)

Military specification	Type	Styles	Application notes	Failure modes	Failure rate ($F/10^6$ hrs)
MIL-C-39001	Mica dielectric established reliability (FR: 1 to 0.001)	CMR04 CMR05 CMR06 CMR07 CMR08	Intended for use where known orders of reliability are required. Failure rate depends almost exclosively on unit's application; e.g., (1) with constant temperature, capacitor life is inversely proportional to the 8th power of the applied dc voltage, or (2) with constant dc voltage, life decreases approximately 50% per each $10^{o}C$ rise in temperature. Life expectancy at rated conditions is 50,000 hrs, minimum. (Failure rate shown in last column is taken from MIL-STD-198C.)	Same comments as given for MIL-C-5.	0.006
FIXED, ELECTROLYTIC					
MIL-C-62	Electrolytic (dry electrolyte aluminum)	Not applicable for airborne equipment use.			
MIL-C-3965	Electrolytic (non-solid electrolyte) tantalum	Inactive for new design. See MIL-C-29006.			
MIL-C-39003	Tantalum (solid electrolyte) established reliability (FR: 2 to 0.001)	CSR13	Intended for use where a known order of reliability is required. These capacitors are the most stable, reliable and long-lived electrolytics available. These units are not temperature sensitive. Limitations are relatively high leakage current, small voltage range (6-120 V) and a maximum allowable reverse current of 5% of rated dc voltage at $+25^{o}C$ to 1.0% at $+125^{o}C$. Capacitors are used where low-frequency, pulsating dc components are to be bypassed or filtered-out and for uses requiring large capacitances, small size and the ability to withstand significant shock and vibration levels. Use for filtering, bypass, coupling, blocking, energy storage and other low voltage dc applications. Capacitors are available only in polarized form; use only in dc circuits with the polarity observed.	Shorts can occur due to solder-balls created by internal solder flow resulting from heat generated during the external soldering of leads. Shorts due to dielectric breakdown are rare due to self-healing effect of high leakage current on the MnO_2, provided current is limited by use of a 3 ohm/volt line resistance in series with the capacitor. Opens occur mainly due to poor solder or weld internal connections which rupture during vibration or shock.	0.052

Table 4-9 APPLICATION AND SELECTION GUIDELINES FOR CAPACITORS (Page 3)

Military specification	Type	Styles	Application notes	Failure modes	Failure rate ($F/10^6$ hrs)
MIL-C-39006	Electrolytic (non-solid electrolyte) tantalum reliability established	CLR25 CLR27 CLR35 CLR37 CLR65	Polarized foil capacitors (styles CLR25 and CLR35) should be used where large capacitance values are required and wide tolerances are acceptable. Use for bypassing or filtering-out low frequency pulsating dc components. When used for low frequency coupling in vacuum tube and transistor circuits, allow for leakage current. Units should be used only in dc circuits with polarity properly observed. If ac components are present, the sum of the peak ac voltage plus the applied dc voltage must not exceed the dc rated voltage. Also, peak ac voltage shall not exceed the applied dc voltage. Nonpolarized foil capacitors (styles CLR27 and CLR37) are suitable for use in ac applications where dc voltage reversals occur. Examples: tuned, low frequency circuits; phasing low-voltage ac motors; computer circuits, in which dc voltage-reversal occurs; servo systems. Sintered-slugs (style CLR65) are used primarily in low voltage power supply filtering circuits. Use in dc applications only; no reverse voltage can be tolerated.	Capacitors are subject to failure (shorts) due to leakage of the electrolyte which can be caused by wide-range temperature cycling, vibration or agencies which damage the seal. The application of reverse voltage will also result in shorts. Opens are usually associated with faults in external lead welds.	0.11
MIL-C-39018	Electrolytic (aluminum oxide electrolyte)	CU13 CU15 CU17	Use in filter, coupling, and bypass applications in which large capacitances are needed and capacitance excesses over the nominal value can be tolerated. For polarized units (styles CU13 and CU17) the applied ac peak voltage should never exceed the applied dc voltage. The sum of the applied ac peak and dc voltages should never exceed the dc rated weaking voltage. Use where low-frequency, pulsating dc signal components are to be filtered out, such as in B power supplies up to 250 dc working volts; at plate and screen connections to B+; and as cathode bypass units in self-biasing circuits.	Capacitance loss (drift) will occur as the result of the aluminum oxide dielectric electric electrochemically combining with the electrolyte. Opens can occur by the dissolution in the electrolyte of the lead between an electrode and the aluminum. Seal degradation can result from use of any type of halogenated solvent wash. Application of voltage in reverse polarity will burn-out (open) these units.	1.6

Table 4-9 APPLICATION AND SELECTION GUIDELINES FOR CAPACITORS (Page 4)

Military specification	Type	Styles	Application notes	Failure modes	Failure rate ($F/10^6$ hrs)
FIXED, PAPER AND PLASTIC					
MIL-C-25	Paper (or paper-plastic dielectric)	Inactive for new design. See MIL-C-19978.			
MIL-C-11693	Feed through radio-interference reduction; ac and dc	CZ23 CZ33 CZ42	Use in applications where it is necessary to pass low-frequency currents through a chassis or from point-to-point in an equipment and to pass the RF currents (which can cause interference) to ground by the shortest possible path. Typical equipment for the above applications are: (a) rotating machinery (b) ignition systems (c) electromechanical voltage regulators, vibrators, and switches (d) electronic devices (transmitters, radar modulators, thyratrons, etc.).	Same comments as given for MIL-C-19978.	0.01
MIL-C-12889	Bypass radio-interference reduction paper dielectric, ac and dc	CA32 CA36 CA47	Use for general purpose applications where suppression of broadband radio interference is needed. These capacitors are useful in limiting electrical disturbances of the conducted type only. Where maximum insertion loss from a bypass capacitor above 1 MHz is desired, the feed-through type covered by MIL-C-11693 will provide attenuation over the useful frequency range.	Principal failure modes are shorts due to entrance of moisture or contaminants if hermetic seal is ruptured. Opens are due to poor internal connections which can rupture due to shock or vibration.	0.02
MIL-C-14157	Plastic (paper-plastic) or plastic dielectric, dc, hermetically-sealed in metal cases, established reliability (FR: 1 to 0.001)	Inactive for new design. See MIL-C-19978.			

Table 4-9 APPLICATION AND SELECTION GUIDELINES FOR CAPACITORS (Page 5)

Military specification	Type	Styles	Application notes	Failure modes	Failure rate ($F/10^6$ hrs)
MIL-C-18312	Metallized paper (or polyester film) dielectric	Inactive for new design. See MIL-C-39022.			
MIL-C-19978	Plastic (or paper -plastic) dielectric	CQR07 CQR09 CQR12 CQR13 CQR29 CQR32 CQR33	Capacitors are intended for use in applications which require high insulation resistance, low dielectric absorption, or low loss factor over wide temperature ranges, and where the ac components of the impressed voltage is small compared to the dc voltage rating. If ac components are present, the sum of the dc peak voltage and the ac peak voltage shall never exceed the rated dc voltage, nor shall the peak ac voltage exceed 20% of the dc voltage rating at 60 Hz, 15% at 120 Hz, or 1.0% at 10,000 Hz. For Air Force equipment applications, do not use these capacitors above 85°C ambient temperature.	Principal failure modes are open, due to poor internal connections and use at rated voltage levels in high temperatures. Shorts can occur due to internal solder flow caused by excessive heat being applied to the terminals during external soldering. Shorts also occur due to contaminants in the dielectric causing momentary breakdown which can result in a carbonization of the plastic, which, if extensive enough, will result in a permanent short.	0.0012
MIL-C-39022	Metallized dielectric, dc (hermatically sealed in metal cases), established reliability	CHR09 CHR19	Intended for use in applications where the ac voltage component is small compared to the dc voltage rating and where occasional periods of low insulation resistance and momentary breakdown can be tolerated. If ac component is present, the sum of the applied dc and the peak ac voltage shall not exceed the rated dc voltage, and the ac voltage shall not exceed 20% of the dc voltage rating.	Opens occur due to poor internal connections, which under strong electrical or mechanical stress, will rupture. Shorts can occur due to internal solder flow as the result of over-heating the leads during external soldering. Momentary shorts occur very frequency because the dielectric is so thin, but will heal themselves, losing a small amount of capacitance in the process.	0.0012
FIXED, CERAMIC					
MIL-C-11015	Ceramic dielectric (general purpose)	CK60 CK67 CK62 CK68 CK63 CK69 CK65 CK70 CK66 CK71	Intended for use where small size, comparatively large capacitance and high insulation resistance are required. Capacitors are suitable for use as bypass, filter and noncritical coupling elements in high-frequency circuits where applicable capacitance change caused by temperature variations can be tolerated. (Continued)	Shorts--can occur due to silver ion migration caused by high humidities coupled with the application of high dc voltage. Opens-generally result from damage done to the capacitor by handling or by the application of excessive heat during soldering which ruptures internal connections.	0.44

Table 4-9 APPLICATION AND SELECTION GUIDELINES FOR CAPACITORS (Page 6)

Military specification	Type	Styles	Application notes	Failure modes	Failure rate ($F/10^6$ hrs)
MIL-C-11015	(continued)		Typical cases include resistive-capacitive coupling for audio and radio frequency, RF and IF cathode bypass, etc. Use where dissipation factor is not critical and moderate changes due to temperature, voltage and frequency variations, do not affect proper circuit function.	Shorts can also occur by internal solder reflow due to excessive heat applied to leads during external soldering without use of a proper heat sink procedure.	
MIL-C-39011	Not applicable, specification cancelled.				
MIL-C-39014	Ceramic dielectric, established reliability (FT: 1 to 0.001)	CK05 CK06 CK64 CK72	Use in applications where the required reliability level is known. Otherwise application notes are the same as given for MIL-C-11015.	Same as MIL-C-11015.	0.044
VARIABLE					
MIL-C-81	Ceramic dielectric	CV11 CV21 CV31	Capacitors are intended for use where fine tuning adjustments are periodically required. They are frequently used in RF, IR, oscillator, phase shifter, and discriminator stages. Capacitance and adjustment are relatively linear. Capacitance change with temperature change in nonlinear; also the temperature sensitivity over the capacitance range is nonlinear. Do not use these units for temperature compensation. These are small-size trimmers which are relatively stable under shock and vibration. Where greater stability is required, air trimmers should be used.	Same comments as given for MIL-C-11015.	2.4
MIL-C-92	Air dielectric (trimmer)	CT04 CT12 CT16	Same applications as given for MIL-C-81 units, except that these units are more stable with temperature. Voltage ratings for these units range from 50 VDC (CT04) through 700 VDC (CT12).	Shorts can occur due to presence of contamination within the capacitor. Contaminants frequently are due to threat wear or to gold plating shaken loose by vibration. Opens result from cold internal solder connections rupturing during external soldering operations.	1.0

Table 4-10 ELECTRON TUBE SELECTION CRITERIA

1. MIL-STD-200, "Electron Tubes, Selection of".

2. MIL-E-1, "Electron Tubes, General Specification for".

3. MIL-STD-454C, "Standard General Requirements for Electronic Equipment", Requirement No. 29.

   Appendix D presents a listing of electron tubes which have been excerpted from MIL-STD-200. Tube types listed in MIL-STD-200 are those devices which meet the following criteria:

   a) The tube shall be considered by representatives of the military departments the best available type for current application.

   b) The tube shall have been in production, and continued availability shall be reasonably certain.

   c) The tube shall have an approved military specification.

   Appendix D provides a list of failure rates for tubes taken from MIL-HDBK-217B. These failure rates are from one to three orders of magnitude greater than semiconductor devices currently in use. These failure rates are provided mainly for comparison and should be used only when no semiconductor device can be found to cover the specific design situation. In the case of high power/high frequency tubes, careful coordination with the tube manufacturers is recommended. Note that tubes, in general, possess much shorter useful life periods than semiconductor devices.

4. Historical test data (similar applications) or other engineering information and/or data that provides assurance that the device is sufficiently rugged and reliable for the application (e.g., previous use in military equipment, comparable application or GFE).

Table 4-11 SELECTION CRITERIA FOR TRANSFORMERS AND INDUCTORS

1. MIL-STD-1286, "Transformers, Inductors and Coils, Selection and Use of".

2. Established Reliability Specifications:

   MIL-T-39013, "Transformers and Inductors, Audio and Power"

   MIL-T-39026, "Transformers, Pulse, Low Power"

3. In accordance with MIL specifications:

   MIL-T-27, "Transformers and Inductors"

   MIL-C-15305, "Coils, RF and Transformers, RF & IF"

   MIL-T-21038, "Transformers, Pulse"

4. Historical test data (from similar applications or other engineering information and/or data that provides assurance that the device is sufficiently rugged and reliable for the application (e.g., previous use in military equipment, comparable application or GFE).

A list of failure rates for generic types of transformers and inductors is given in Table 4-14. This list, derived from MIL-HDBK-217B, provides comparative values for various inductive devices.

Table 4-12 RELAY SELECTION CRITERIA

1. MIL-STD-1346, "Relays, Selection and Use of" (Applicable military specifications are listed in Table 4-13.)
2. MIL-STD-454C, "Standard General Requirements for Electronic Equipment", Requirement No. 57.
3. MIL-R-39016, "Relays, Electromagnetic, Established Reliability, General Specification for".
4. Historical test data (from similar applications or other engineering information and/or data that provides assurance that the device is sufficiently rugged and reliable for the application (e.g., previous use in military equipment, comparable application or GFE).

Where use of a nonstandard device is necessary, request for approval of this device shall be made to military agencies according to the requirements and procedures of MIL-STD-749.

A list of failure rates for generic types of relays is given in Table 4-14. This list, derived from MIL-HDBK-217B, provides comparative values for various relay types.

Table 4-13 APPLICABLE MIL SPECIFICATIONS FOR RELAYS

a) Low current relays (up to 10 amps). Low current relays up to 10 amperes shall conform to MIL-R-5757. However, relay applications requiring high in-rush current capabilities (i.e., motor and controller functions) may be in accord with MIL-R-6106, as applicable.

b) High current relays. Relays used in high current applications shall conform to MIL-R-6106.

c) Time delay relays. Thermal time delay relays shall conform to MIL-R-19648. Electronic, including solid state, time delay relays shall conform to MIL-R-83726.

d) Solid state telegraph relay assemblies. Solid state passive telegraph relays shall conform to MIL-R-27777.

e) Established reliability relays. Established reliability relays shall conform to MIL-R-39016.

f) Reed relays. Reed relays shall conform to MIL-R-5757.

g) Relay sockets. When relay sockets are required, they shall conform to MIL-S-12883.

Table 4-14 GENERIC FAILURE RATES (x 10^{-6}) FOR RELAYS AND INDUCTIVE DEVICES (Derived from MIL-HDBK-217B)

Part Type	Use Environment—Increasing Severity——→								
	Ground Benign	Space Flight	Ground Fixed	Airborne Inhabited	Naval Sheltered	Ground Mobile	Airborne Uninhabited	Naval Uninhabited	Missile Launch
RELAYS									
1. General Purpose	0.13	0.13	0.30	1.3	1.6	2.6	2.6	3.2	16.0
2. Contactor, High Current	0.43	0.43	1.0	4.5	5.5	5.6	8.8	11.0	36.0
3. Latching	0.12	0.12	0.29	1.3	1.6	1.6	2.5	3.1	16.0
4. Reed	0.11	0.11	0.26	1.1	1.4	1.4	2.2	2.7	14.0
5. Meter Movement and Bi-Metal	2.4	2.4	5.7	25.0	30.0	31.0	49.0	61.0	310.0
INDUCTIVE DEVICES									
1. Pulse Transformer	0.0012	0.0012	0.0027	0.0075	0.0083	0.0045	0.014	0.011	0.015
2. Audio Transformer	0.0025	0.0025	0.0066	0.018	0.02	0.011	0.034	0.027	0.036
3. Power Transformers and Filters	0.0075	0.0075	0.021	0.056	0.064	0.034	0.12	0.096	0.11
4. RF Transformers and Coils	0.0096	0.0096	0.022	0.06	0.066	0.036	0.11	0.084	0.12

Table 4-15 SELECTION CRITERIA FOR SWITCHES

1. MIL-STD-1132, "Switches and Associated Hardware, Selection and Use of".

2. Requirements 58 of MIL-STD-454C, "Standard General Requirements for Electronic Equipment". MIL-STD-454C, Requirement 58 requires that:

   a) Switches and associated hardware shall be selected from MIL-STD-1132 and shall conform to the applicable specifications listed therein.

   b) Switches other than those listed in MIL-STD-1132 shall conform to one of the following specifications:

      MIL-S-12285, Switch, Thermostatic

      MIL-S-15743, Switches, Rotary, Enclosed

      MIL-S-18396, Switches, Meter and Control, Naval Shipyard

      MIL-S-21604, Switches, Rotary, Multipole and Selector Type

      MIL-S-28705, Switch, Leaf Spring, (Pile-up Contacts; Lever, Push, Turn; Illuminated and Nonilluminated) General Specification for.

3. Historical test data (from similar applications) or other engineering information and/or data that provides assurance that the device is sufficiently rugged and reliable for the application (e.g., previous use in military equipment, comparable application or GFE).

A list of failure rates for generic switch types is given in Table 4-16. The relationship between contact life versus load characteristics is shown in Figure 4-2.

Table 4-16 FAILURE RATES FOR GENERIC SWITCH TYPES (x 10^{-6})

Switch Type	Use Environment								
	Ground Benign	Space Flight	Ground Fixed	Airborne Inhabited	Naval Sheltered	Ground Mobile	Airborne Uninhabited	Naval Uninhabited	Missile Launch
1. Toggle	0.17	0.17	0.57	6.8	0.68	2.9	8.6	4.0	114.0
2. Pushbutton	0.11	0.11	0.38	4.6	0.46	1.9	5.7	2.7	76.0
3. Sensitive	0.27	0.27	0.90	11.0	1.1	4.5	14.0	6.3	180.0
4. Rotary	0.42	0.42	1.4	17.0	1.7	6.9	21.0	9.7	280.0

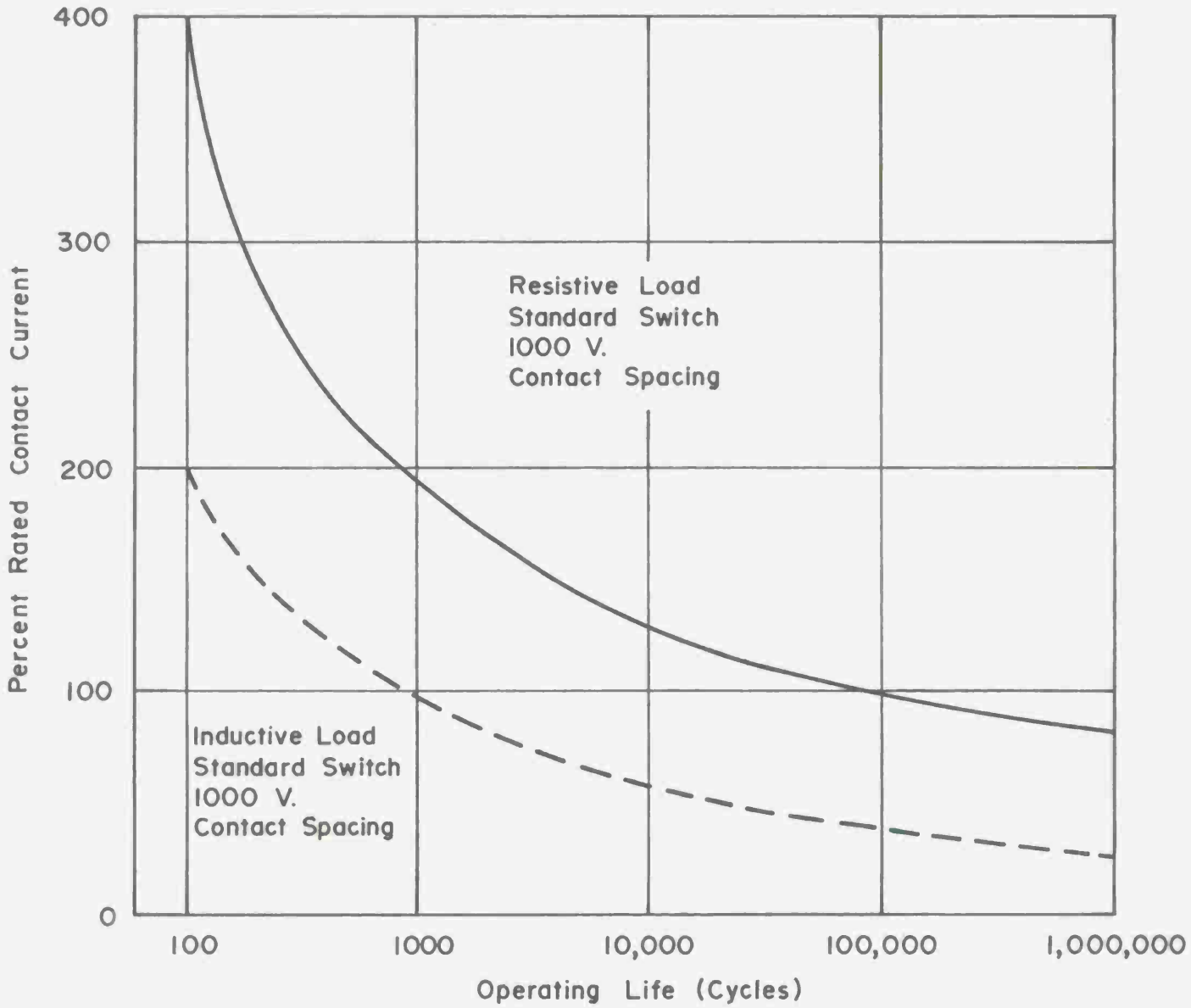


Fig. 4-2 EFFECT OF CURRENT ON OPERATING LIFE (TYPICAL CHARACTERISTIC)

Table 4-17 CONNECTOR SELECTION CRITERIA

1. Approved style of Military Specification.
2. MIL-STD-454C, "Standard General Requirements for Electronic Equipment", Requirement No. 10, Notice 3, 1 May 1972.
3. MIL-P-11268(EL), "Parts, Materials and Processes Used in Electronic Equipment".
4. Historical test data (from similar applications) or other engineering information and/or data that provides assurance that the device is sufficiently rugged and reliable for the application (e.g., previous use in military equipment, comparable application or GFE).

Table 4-18 SELECTION CRITERIA FOR WAVEGUIDES AND RELATED EQUIPMENT

1. MIL-STD-1327, "Flanges, Coaxial and Waveguides; and Coupling Assemblies, Selection of".
2. MIL-STD-1328, "Couplers, Directional (Coaxial Line, Waveguide and Printed Circuit), Selection of".
3. MIL-STD-1329, "Switches, RF Coaxial, Selection of".
4. MIL-STD-454C, "Standard General Requirements for Electronic Equipment", Requirement No. 53.

Table I of MIL-STD-454 relates specific types of waveguide equipment to the applicable MIL specification.

Listings of waveguides, directional couplers, flanges, coupling assemblies and RF switches are given in Military Standards 1327, 1328 and 1329, respectively. Microwave equipments listed in MIL-STD-1327, 1328 and 1329 are those which meet the following criteria:

a) The microwave equipment shall be considered by government representatives the best available type for the current application.

b) The microwave equipment shall have been in production, and continued availability shall be reasonably certain.

c) The microwave equipment shall have an approved military specification.

Table 4-19 which follows provides additional guidelines for application of waveguides and related equipment.

Table 4-19 APPLICATION AND USE OF WAVEGUIDES AND RELATED EQUIPMENT

The following requirements of MIL-STD-1327, 1328 and 1329 apply to the use, in military equipment, of waveguides and related equipment:

a) Military equipment and assemblies shall comply with their performance specification requirements when using listed flanges and coupling assemblies which are from manufactured lots possessing acceptable material and physical characteristics.

b) Directional couplers used in military equipment shall be from lots possessing acceptable material and physical and electrical characteristics and shall in no manner degrade the operational characteristics of the equipments in which used.

c) Coaxial switches used in military applications shall be representative of manufactured lots possessing acceptable material and physical and electrical characteristics and shall in no manner degrade the operational characteristics of the equipment in which used.

d) Request for use of waveguide and related equipment not listed in these standards. When a contractor has determined that a flange or coupling assembly not listed in these standards is required, a written request for use of a nonstandard part shall be made in accordance with MIL-STD-749.

General Design Considerations

a) Materials. When selecting parts, consideration shall be given to corrosion resistance of materials and the proper protection of dissimilar metal combinations.

b) Fabrication or rigid assemblies. MIL-HDBK-660 shall be used as a guide in the fabrication of rigid assemblies

Table 4-20 SELECTION CRITERIA FOR CABLES

1. MIL-STD-454C, "Standard General Requirements for Electronic Equipment", Requirement No. 66.
2. An approved Military Specification style.
3. Historical data (similar application) test data or other engineering information that provides assurance that the cable is sufficiently rugged and reliable for the application (e.g., previous use in military equipment, comparable application or GFE). Note: When the use of a nonstandard cable is considered necessary, request for approval for its use shall be submitted to the military according to the procedures of MIL-STD-749.

The following requirements of MIL-STD-454C apply to the selection of cables:

Solid or stranded--Either solid or stranded conductors may be used--within the restrictions of the particular wire or cable specification--except that (a) only stranded wire shall be used in aerospace applications, and (b) for other applications, stranded wire shall be used when so indicated by the equipment specification. Specifically, stranded wire shall be used for wires and cables which are normally flexed in use and servicing of the equipment, such as cables attached to the movable half of detachable connectors.

Size--Conductors shall be of such cross-section, temper, and flexibility as to provide ample and safe current-carrying capacity and strength. In general, wire shall not be smaller than size 22. Smaller wire may be used when benefits can be obtained with no loss in performance. Specifically, smaller wire may be used in cables having larger numbers of wires and adequate support against vibration. Smaller size wire may be used when necessary for welding of electronic interconnections.

are those that reduce the number of defective devices from production lines by means of inspection and conventional testing. The screens are those which remove inferior devices and reduce the hazard rate by methods of stress application.

The purpose of reliability screening is to compress the early failure period and reduce the failure rate to acceptable levels as quickly as possible. Figure 4-3 illustrates the application of a time stress at the part level and shows, comparatively, how reliability screening can improve the part failure rate. It also shows that, by applying a higher temperature stress of 125°C instead of 100°C, comparable failure rate levels can be achieved in 100 hours instead of 240 hours.

The term "screening" can be said to mean the application to an electronic device of a stress test, or tests, which will reveal inherent weaknesses (and thus incipient failures) of the devices without destroying the integrity of the device. This procedure, when applied equally to a group of similar devices manufactured by the same processes, is used to identify sub-par members of the group without impairing the structure or functional capability of the "good" members of the group.

The rationale for such action is that the inferior devices will fail and the superior devices will pass, provided the tests and stress levels are properly selected. If the failed units are removed from the group, the remaining devices are those which have demonstrated the ability to withstand stress and their reliability under normal rated operating conditions can therefore be assumed.

Screening can be done (a) by the part manufacturer, (b) by the user in his own facilities, or (c) by an independent testing laboratory. No matter which agency is employed to do the screen tests, the user should first acquaint himself with the efficacy of the screening tests used by the vendor in normal production. If such screens exist, and are effective, screens can be designed to supplement the vendor's tests; if the vendor's tests are unsatisfactory, the screening program will have to be a comprehensive one.

When particular failure modes or mechanisms are known or suspected to be present (as indicated in subsection 4.1.1.2), a specific screen should be selected to detect these unreliable elements.

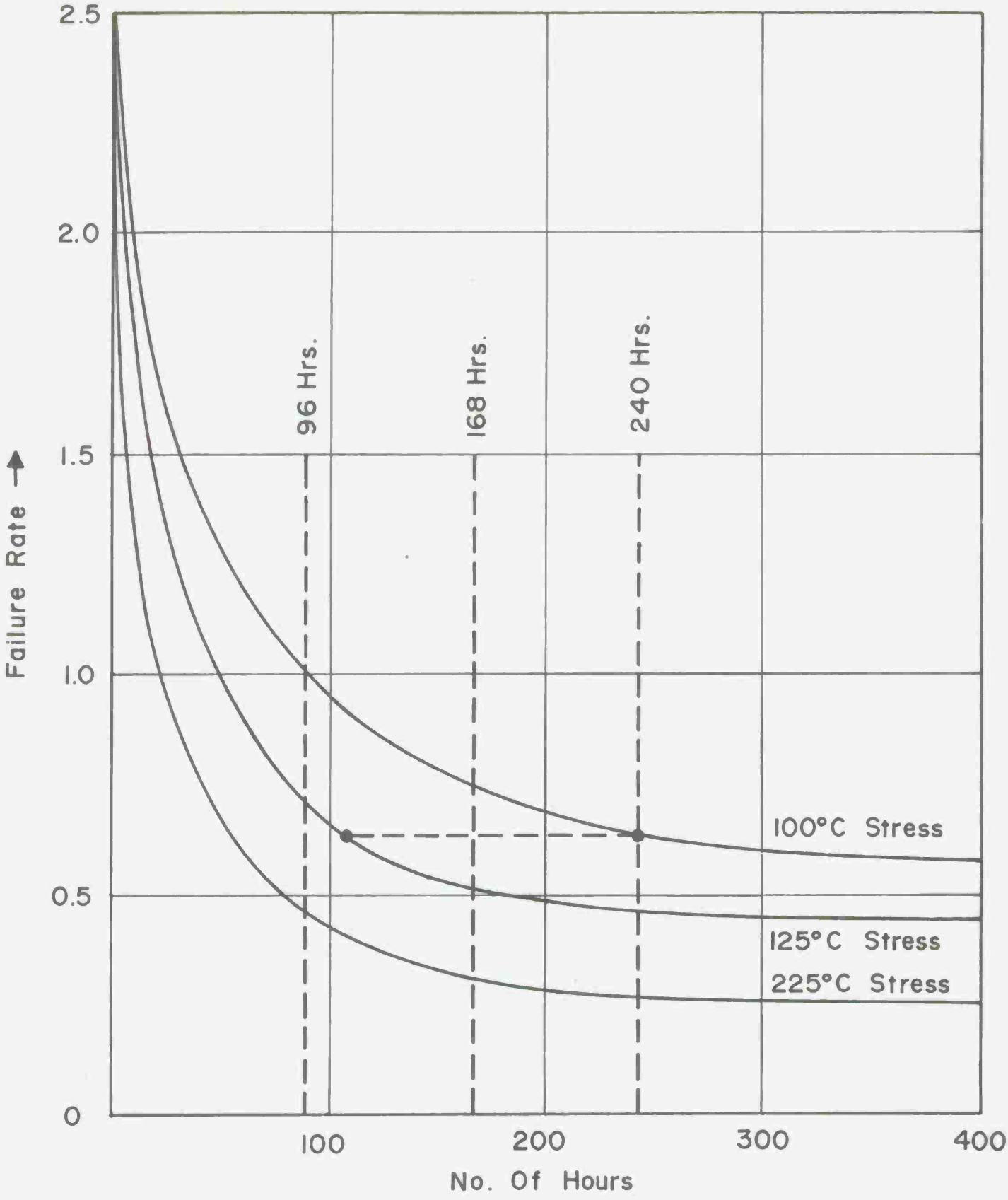


Fig. 4-3 RELIABILITY SCREENS

Table 4-21 shows the failure mode distribution for standard silicon transistors and integrated circuits: SSI, MSI, LSI (TI data), and integrated circuits technologies, TTL, CMOS (RAC data).

A detailed understanding of the device characteristics, materials, packaging and fabrication techniques relative to the failure mode distribution shown in Table 4-21 is essential in selecting a meaningful screen at reasonable cost. Devices that perform the same function may be fabricated with different materials (e.g., aluminum leads instead of gold on an integrated circuit). The effectiveness of a screen is material-dependent. For example, the stress level that is effective for gold may be ineffective for aluminum because of the difference in mass. The x-ray screen is effective for gold, but aluminum and silicon are transparent to x-rays. Some screens are effective for p-n-isolated integrated circuits but ineffective for dielectrically isolated devices. Only a thorough knowledge of the device to be screened and the effectiveness and limitations of the various tests can produce a useful and reliable screening procedure.

Screening tests are particularly well suited to discrete semiconductor and microelectronic devices due to their material/process dependency. MIL-STD-883A forms the basis for selecting meaningful screening tests for microelectronic devices. Note that TX semiconductors are screened and burned-in in a manner comparable to MIL-STD-883.

Tables 4-22 and 4-23, reproduced from MIL-HDBK-175, provide a listing of microcircuit defects/screens and a comparison of screening methods, respectively.

The criticality of the component part application and the required level of reliability has an important bearing on the stress levels and number of tests that should be included in the overall part screening procedure. The part screen procedure must also be cost effective and must meet time and funding constraints.

Figure 4-4 shows relative cost estimates for various part classes. It can be seen that the most cost effective screen is class B of MIL-STD-883.

Table 4-21 FAILURE MODE DISTRIBUTION FOR TRANSISTORS AND INTEGRATED CIRCUITS

Failure Mode	TI Data in %*					RAC Data in %**	
	Transistor	SSI	MSI	LSI	MOS/LSI	TTL	CMOS
Metallization	6	10	18	26	7	50	25
Diffusion	10	8	12	25	13	2	9
Foreign Material		5	11	13	1	6	7
Miscellaneous	6	5	12	13	21		
Oxide	31	18	20	13	33	4	16
Bonding	38	14	7	4	5	13	15
Die Attach Packaging	9	5	3	2	5	25	8
Misapplication		35	17	4	15		
	100	100	100	100	100	100	100

*Data published in the Proceedings of the IEEE, February 1974 (C.G. Peattie, et al.; Elements of Device Reliability).

**Data supplied by Reliability Analysis Center, RADC.

Table 4-22 MICROCIRCUIT DEFECTS/SCREENS

Point at Which a Reliability-Influencing Variable is Introduced	Failure Mechanism	Failure Mode	Failure Detection Method
Slice Preparation	Dislocations and stacking faults	Degradation of junction characteristics	Initial electrical test; operational-life tests
	Nonuniform resistivity	Unpredictable component values	Initial electrical test;
	Irregular surface	Improper electrical performance and/or shorts, opens, etc.	Initial electrical test; operational-life tests
	Cracks, chips, scratches (general handling damage)	Opens, possible shorts in subsequent metallization	Initial electrical test; visual (pre-cap); thermal cycling
	Contamination	Degradation of junction characteristics	Visual (pre-cap); thermal cycling; high-temperature storage; reverse bias
Passivation	Cracks and pin holes	Electrical breakdown in oxide layer between metallization and substrate; shorts caused by faulty oxide diffusion mask	High-temperature storage; thermal cycling; high-voltage test; operating-life test; visual (pre-cap)
	Nonuniform thickness	Low breakdown and increased leakage in the oxide layer	High-temperature storage; thermal cycling; high-voltage test; operating-life test; visual (pre-cap)
Masking	Scratches, nicks, blemishes in the photo mask	Opens and/or shorts	Visual (pre-cap); initial electrical test
	Misalignment	Opens and/or shorts	Visual (pre-cap); initial electrical test
	Irregularities in photoresist patterns (line widths, spaces, pinholes)	Performance degradation caused by parameter drift, opens, or shorts	Visual (pre-cap); initial electrical test
Etching	Improper removal of oxide	Opens and/or shorts or intermittents	Visual (pre-cap); initial electrical test; operational-life test
	Undercutting	Shorts and/or opens in metallization	Visual (pre-cap); initial electrical test
	Spotting (etch splash)	Potential shorts	Visual (pre-cap); thermal cycling; high-temperature storage; operational-life test
	Contamination (photoresist, chemical residue	Low breakdown; increased leakage	Visual (pre-cap); initial electrical test; thermal cycling; high-temperature storage; operational-life test; reverse bias
Diffusions	Improper control of doping profiles	Performance degradation resulting from unstable and faulty passive and active components	High-temperature storage; thermal cycling; operational-life test; initial electrical test

Table 4-22 MICROCIRCUIT DEFECTS/SCREENS (Page 2)

Point at Which a Reliability-Influencing Variable is Introduced	Failure Mechanism	Failure Mode	Failure Detection Method
Metallization	Scratched or smeared metallization (handling damage)	Opens, near opens, shorts, near shorts	Visual (pre-cap; thermal cycling; operational-life test
	Thin metallization to insufficient deposition or oxide steps	Opens and/or high-resistance intraconnections	Initial electrical test; operational-life test; thermal cycling
	Oxide contamination-material incompatibility	Open metallization to poor adhesion	High-temperature storage; thermal cycling; operational-life test
	Corrosion (chemical residue)	Opens in metallization	Visual (pre-cap); high-temperature storage; thermal cycling; operational life test
	Misalignment and contaminated contact areas	High contact resistance or opens	Visual (pre-cap); initial electrical test; high-temperature storage; thermal cycling; operational-life test
	Improper alloying temperature or time	Open metallization, poor adhesion, or shorts	Initial electrical test; high-temperature storage; thermal cycling; operational-life tests
Die Separation	Improper die separation resulting in cracked or chipped dice	Opens and potential opens	Visual (pre-cap); thermal cycling; vibration; mechanical shock; thermal shock
Die Bonding	Voids between header and die	Performance degradation caused by overheating	X-ray; operational-life; acceleration, mechanical shock; vibration
	Overspreading and/or loose particles of eutectic solder	Shorts or intermittent shorts	Visual (pre-cap); X-ray; monitored vibration; monitored shock
	Poor die-to-header bond	Cracked or lifted die	Visual (pre-cap); acceleration; shock, vibration
	Material mismatch	Lifted or cracked die	Thermal cycling; high-temperature storage; acceleration
Wire Bonding	Overbonding and underbonding	Wire weakened and breaks or is intermittent; lifted bond; open	Acceleration; shock; vibration
	Material incompatibility or contaminated bonding pad	Lifted lead bond	Thermal cycling; high-temperature storage; acceleration, shock, vibration
	Plague formation	Open bonds	High-temperature storage; thermal cycling; acceleration, shock, vibration
	Insufficient bonding pad area or spacings	Opens or shorted bonds	Operational-life test; acceleration, shock, vibration; visual (pre-cap)

Table 4-22 MICROCIRCUIT DEFECTS/SCREENS (Page 3)

Point at Which a Reliability-Influencing Variable is Introduced	Failure Mechanism	Failure Mode	Failure Detection Method
Wire Bonding (continued)	Improper bonding procedure or control	Opens, shorts, or intermittent operation	Visual (pre-cap); initial electrical test; acceleration, shock, vibration
	Improper bond alignment	Open and/or shorts	Visual (pre-cap); initial electrical test
	Cracked or chipped die	Open	Visual (pre-cap); high-temperature storage; thermal cycling; acceleration, shock, vibration
	Excessive loops, sags, or lead length	Shorts to case, substrate, or other leads	Visual (pre-cap); X-ray; acceleration, shock, vibration
	Nicks, cuts, and abrasions on leads	Broken leads causing opens or shorts	Visual (pre-cap); acceleration, shock, vibration
	Unremoved pigtails	Shorts or intermittent shorts	Visual (pre-cap); acceleration, shock, vibration, X-ray
Final Seal	Poor hermetic seal	Performance degradation; shorts or opens caused by chemical corrosion or moisture	Leak tests
	Incorrect atmosphere sealed in package	Performance degradation caused by inversion and channeling	Operational-life test; reverse bias; high-temperature storage, thermal cycling
	Broken or bent external leads	Open circuit	Visual; lead fatigue tests
	Cracks, voids in kovar-to-glass seals	Shorts and/or opens in the metallization caused by a leak	Leak test; electrical test; high-temperature storage; thermal cycling; high-voltage test
	Electrolytic growth of metals or metallic compounds across glass seals between leads and metal case	Intermittent shorts	Low-voltage test
	Loose conducting particles in package	Intermittent shorts	Acceleration; monitored vibration; X-ray; monitored shock
	Improper marking	Completely inoperative	Electrical test

Table 4-23 COMPARISON OF SCREENING METHODS

Screen	Defects	Effectiveness	Cost	Comments
Interval visual inspection	Lead dress Metallization Oxide Particle Die bond Wire bond Contamination Corrosion Substrate		Inexpensive to moderate	This is a mandatory screen for high-reliability devices. Cost will depend upon the depth of the visual inspection.
Infrared	Design (thermal)	Very good	Expensive	For use in design evaluation only.
X-Ray	Die bond Lead dress (gold) Particle Manufacturing (gross errors) Seal Package Contamination	Excellent Good Good Good Good Good Good	Moderate	The advantage of this screen is that the die-to-header bond can be examined and some inspection can be performed after encapsulation. However, some materials are transparent to X-rays (i.e., Al and Si) and the cost may be as high as six times that of visual inspection, depending upon the complexity of the test system.
High temperature storage	Electrical (stability) Metallization Bulk silicon Corrosion	Good	Very inexpensive	This is a highly desirable screen.
Temperature cycling	Package Seal Die bond Wire bond Cracked substrate Thermal mismatch	Good	Very inexpensive	This screen may be one of the most effective for aluminum lead systems.
Thermal shock	Package Seal Die bond Wire bond Cracked substrate Thermal mismatch	Good	Inexpensive	This screen is similar to temperature cycling but induces higher stress levels. As a screen it is probably no better than temperature cycling.
Constant acceleration	Lead dress Die bond Wire bond Cracked substrate	Good	Moderate	At 20,000-G stress levels, the effectiveness of this screen for aluminum is questionable.
Shock (unmonitored)	Lead dress	Poor	Moderate	The drop-shock test is considered inferior to constant acceleration. However, the pneupactor shock test may be more effective. Shock tests may be destructive.
Shock (monitored)	Particles Intermittent short Intermittent open	Poor Fair Fair	Expensive	Visual or X-ray inspection is preferred for particle detection.
Vibration fatigue	Lead dress Package Die bond Wire bond Cracked substrate	Poor	Expensive	This test may be destructive. Except for work hardening, it is without merit.
Vibration variable frequency (unmonitored)	Package Die bond Wire bond Substrate	Fair	Expensive	
Vibration variable frequency (monitored)	Particles Lead dress Intermittent open	Fair Good Good	Very expensive	The effectiveness of this screen for detecting particles is part-dependent.

Table 4-23 COMPARISON OF SCREENING METHODS (Continued)

Screen	Defects	Effectiveness	Cost	Comments
Random vibration (unmonitored)	Package Die bond Wire bond Substrate	Good	Expensive	This is a better screen than VVF (unmonitored) especially for space-launch equipment, but it is more expensive.
Random vibration (monitored)	Particles Lead dress Intermittent open	Fair Good Good	Very expensive	This is one of the most expensive screens; when combined with only fair effectiveness for particle detection, it is not recommended except in very special situations.
Helium leak test	Package Seals	Good	Moderate	This screen is effective for detecting leaks in the range of 10^{-8} to 10^{-10} Attm cc/sec.
Radiflo leak test	Package Seals	Good	Moderate	This screen is effective for leaks in the range of 10^{-8} to 10^{-12} Attm cc/sec.
Nitrogen bomb test	Package Seals	Good	Inexpensive	This test is effective for detecting leaks between the gross-and-fine-leak-detection ranges.
Gross-leak test	Package Seals	Good	Inexpensive	Effectiveness is volume-dependent. Detects leaks greater than 10 Attm cc/sec.
High-voltage test	Oxide	Good	Inexpensive	Effectiveness is fabrication dependent.
Isolation resistance	Lead dress Metallization Contamination	Fair	Inexpensive	
Intermittent operation life	Metallization Bulk silicon Oxide Inversion/ channeling Design Parameter drift Contamination	Good	Expensive	Probably no better than ac operating life.
Ac operating life	Metallization Bulk silicon Oxide Inversion/ channeling Design Parameter Contamination	Very good	Expensive	
Dc operating life	Essentially the same as intermittent life.	Good	Expensive	No mechanisms are activated that could not be better activated by ac life tests.
High-temperature ac operating life	Same as ac operating life	Excellent	Very expensive	Temperature acts to accelerate failure mechanisms. This is probably the most expensive screen and one of the most effective.
High-temperature reverse bias	Inversion/ channeling	Poor	Expensive	

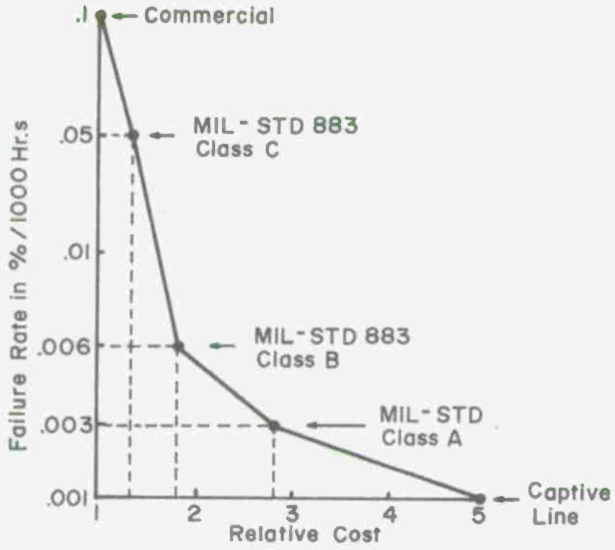


Fig. 4-4 SCREENING EFFECTIVENESS

Table 4-24 lists all the required screens for classes A, B and C of MIL-STD-883, Method 5004. (Note that a burn-in test is required for classes A and B only.) The effectiveness of these screens is shown in Table 4-25. Finally, the cost ranges of screening tests for class B devices are listed in Table 4-26.

Table 4-24 SCREENING SEQUENCE - METHOD 5004 - MIL-STD-883

Screen	Reliability Classes		
	A	B	C
Internal Visual	Condition A	Condition B	Condition B
Stabilization Bake	24 h	24 h	24 h
Thermal Shock	15 cycles and	15 cycles or	15 cycles or
Temperature Cycle	10 cycles	10 cycles	10 cycles
Mechanical Shock	20,000 g	no	no
Centrifuge	30,000 g	30,000 g	30,000 g
Hermeticity	yes	yes	yes
Critical Electrical Parameters	yes	no	no
Burn-in	168 + 72 h	168 h	no
Final Electrical	yes	yes	yes
X-Ray Radiograph	yes	no	no
External Visual	yes	yes	yes

Table 4-25 FALLOUT FROM MIL-STD-883 TESTS[21]

Screen	Average % Fallout	Range (%)
Precap Visual	15	2.0-45
Hermeticity	5	0.1-10
Burn-in	3	0.1-20
Electrical Testing	5	1.3-12
External Visual	4	0.1- 8

Table 4-26 SCREENING TEST COSTS FOR CLASS B DEVICES[21]

MIL-STD-883 Method	Min.	Typical ($)	Max.
1) Precap Visual Inspection Condition B	0.15	0.25	3.00
2) High-Temperature Storage	0.01	0.05	0.10
3) Temperature Cycling	0.05	0.10	0.10
4) Constant Acceleration	0.05	0.10	0.25
5) Fine Leak	0.05	0.10	0.25
6) Gross Leak	0.05	0.10	0.20
7) Burn-in	0.25	0.50	5.00
8) Final Electrical	0.25	0.50	2.00
Total Class B	0.86	1.70	10.90

Note that Table 4-26 covering screening costs is provided for comparative purposes only. Its intent is to illustrate relative cost differences (up to 20 to 1) for screening tests on devices of varying complexity. For a simple integrated circuit logic gate, screening tests will be lower. For LSI devices, the cost will approach the maximum indicated.

4.1.2 Derating

The guidelines in the preceding section on parts selection and control assume that the parts are inherently reliable and capable of withstanding the stresses to which they will be submitted.

Additional improvement in part and, ultimately, equipment reliability can be realized by applying the techniques of derating. Derating can be defined as the operation of a part at less severe stresses than those for which it is rated. In practice, derating can be accomplished by either reducing stresses or by increasing the strength of the part. Selecting a part of greater strength is usually the most practical approach.

Derating is effective because the failure rate of most parts tends to decrease as the applied stress levels are decreased below the rated value. The reverse is also true: the failure rate increases when a part is subjected to higher stresses and temperature. The failure rate model of most parts is stress and temperature dependent. This dependence is discussed more fully in the subsection following (4.1.2.1). Specific derating criteria are given in subsection 4.1.2.2.

4.1.2.1 Temperature-Stress Factors

The temperature-stress effect can best be observed by studying MIL-HDBK-217B failure rate models. The parts failure rate model (discussed in Section 2.1.3) for discrete semiconductors is expressed as follows:

$$\lambda_p = \lambda_b(\pi_E \times \pi_A \times \pi_{S2} \times \pi_C \times \pi_Q)$$

where

λ_p is the part failure rate

λ_b is the base failure rate

π_E Environment--accounts for influence of environmental factors other than temperature. (See Table 2-1, Section 2.1.3.)

π_Q Quality--accounts for effects of different quality levels

π_A Application--accounts for effect of application in terms of circuit function

π_C Complexity--accounts for effect of multiple devices in a single package

π_{S2} Voltage Stress--adjusts model for a second electrical stress (application voltage) in addition to wattage included within λ_b).

The equation for the base failure rate, λ_b, is:

$$\lambda_b = A \exp \frac{N_T}{273 + T + (\Delta T)S} \quad \exp \frac{273 + T + (\Delta T)S}{T_M}^{P}$$

where

A is a failure rate scaling factor.

N_T, T_M and P are shaping parameters.

T is the operating temperature in degrees C, ambient or case, as applicable.

ΔT is the difference between maximum allowable temperature with no junction current or power (total derating) and the maximum allowable temperature with full rated junction current or power.

S is the stress ratio of operating electrical stress to rated electrical stress.

The values for the shaping parameters and constraints are shown in Table 4-27 (taken from MIL-HDBK-217B). The resulting base failure rate (λ_b) for a SI, NPN transistor is shown in Table 4-28 also taken from MIL-HDBK-217B. Figure 4-5 is derived from Table 4-28. It is evident that the only variables of the equation for the base failure rate (λ_b) are T; the operating temperature, ΔT, the difference between maximum temperatures in de-energized and energized state and S, the electrical stress ratio.

Table 4-28 and Figure 4-5 show how λ_b varies with temperature and stress. The data presented is based on the typical maximum junction temperature of 175°C (fully derated) and 25°C for the maximum temperature at which full rated operation is permitted.

Table 4-27 DISCRETE SEMICONDUCTOR BASE FAILURE RATE PARAMETERS

Group	Part Type	λ_b Constants				
		A	N_T	T_M	P	T
Transistors	Si, NPN	0.13	-1052	448	10.5	150
	Si, PNP	0.45	-1324	448	14.2	150
I	Ge, PNP	6.5	-2142	373	20.8	75
	Ge, NPN	21.0	-2221	373	19.0	75
II	FET	0.52	-1162	448	13.8	150
III	Unijunction	3.12	-1779	448	13.8	150
Diodes	Si, Gen. Purpose	0.9	-2138	448	17.7	150
IV	Ge, Gen. Purpose	126	-3568	373	22.5	75
V	Zener/Avalanche	0.04	- 800	448	14	150
VI	Thyristors	0.82	-2050	448	9.5	150
VII	Microwave					
	Ge, Detectors	0.33	- 477	343	15.6	45
	Si, Detectors	0.14	- 392	423	16.6	125
	Ge, Mixers	0.56	- 477	343	15.6	45
	Si, Mixers	0.19	- 394	423	15.6	125
VIII	Varactor, Step Recovery & Tunnel	0.93	-1162	448	13.8	150

Table 4-28 BASE FAILURE RATES FOR GROUP I TRANSISTORS (SILICON, NPN)

T (°C)	S 0.1	0.2	0.3	0.4	0.5	0.6	0.7	0.8	0.9	1.0
0	0.0034	0.0041	0.0048	0.0057	0.0067	0.0079	0.0095	0.011	0.014	0.018
10	0.0038	0.0046	0.0054	0.0064	0.0075	0.0089	0.010	0.013	0.017	0.023
20	0.0043	0.0051	0.0060	0.0071	0.0084	0.010	0.012	0.015	0.020	0.029
25	0.0046	0.0054	0.0064	0.0075	0.0089	0.010	0.013	0.017	0.023	0.033
30	0.0040	0.0057	0.0067	0.0079	0.0095	0.011	0.014	0.018	0.025	
40	0.0054	0.0064	0.0075	0.0009	0.010	0.013	0.017	0.023	0.033	
50	0.0060	0.0071	0.0084	0.010	0.012	0.015	0.020	0.029		
55	0.0064	0.0075	0.0089	0.010	0.013	0.017	0.023	0.033		
60	0.0067	0.0079	0.0095	0.011	0.014	0.018	0.025			
65	0.0071	0.0084	0.010	0.012	0.015	0.020	0.029			
70	0.0075	0.0089	0.010	0.018	0.017	0.023	0.033			
75	0.0079	0.0095	0.011	0.014	0.018	0.025				
80	0.0084	0.010	0.012	0.015	0.020	0.029				
85	0.0089	0.010	0.013	0.017	0.023	0.033				
90	0.0095	0.011	0.014	0.018	0.025					
95	0.010	0.012	0.015	0.020	0.029					
100	0.010	0.013	0.017	0.023	0.033					
105	0.011	0.016	0.018	0.025						
110	0.012	0.013	0.020	0.029						
115	0.013	0.017	0.023	0.033						
120	0.014	0.010	0.025							
125	0.015	0.020	0.029							
130	0.017	0.023	0.033							
135	0.018	0.025								
140	0.020	0.029								
145	0.023	0.033								
150	0.025									
155	0.029									
160	0.033									

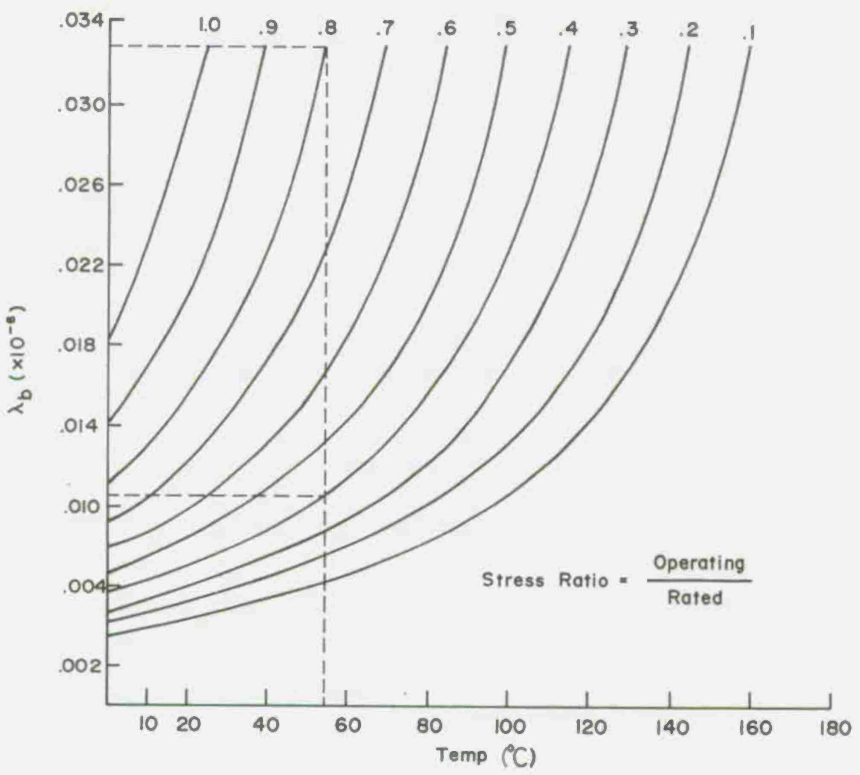


Fig. 4-5 Stress/Temperature Plot For Group I Transistor (Silicon, NPN)

The data show that at higher temperatures (100°C) and at electrical stress higher than 40% (even at lower temperatures) the slopes of the curves (and the failure rate) increase drastically.

Since semiconductors as well as most electronic parts are sensitive to temperature, the thermal analysis of any design should accurately provide the ambient temperatures needed for proper application of the part. Of course, lower temperatures produce better reliability but can also produce increased penalities in terms of added loads (or constraints) on controlling the system's environment. The thermal analysis should be part of the design process and included in all the trade-off studies covering equipment performance, reliability, weight, volume, environmental control requirements, and above all, cost.

Derating procedures vary with different types of parts and their application. Resistors are derated by decreasing the ratio of operating power to rated power. Capacitors are derated by maintaining the applied voltage at a lower value than the voltage for which the part is rated. Semiconductors are derated by keeping the power dissipation below the rated level.

The first step in the procedure for derating electronic parts involves the use of derating curves, which usually relate derating levels to some critical environmental or physical factor. Such curves are typically included in the part specification. A typical derating curve for semiconductors is shown in Figure 4-6.

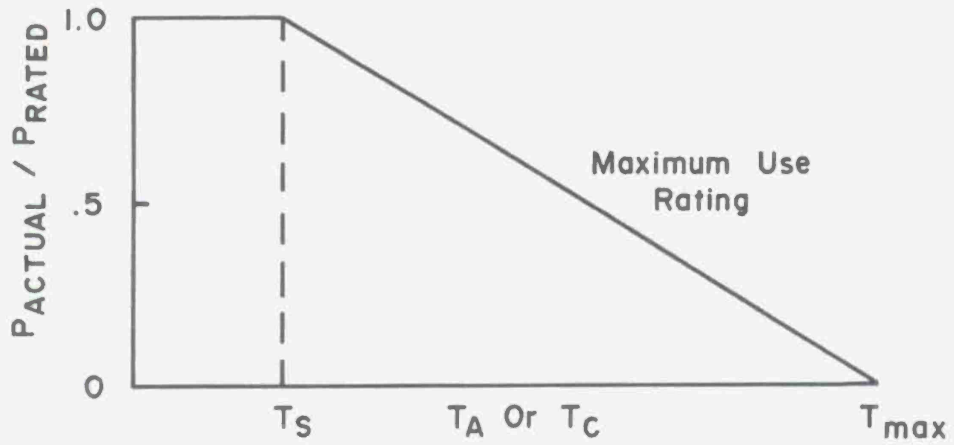


Fig. 4-6 TYPICAL DERATING GRAPH

In Figure 4-6,

T_S is the temperature derating point (usually 25°C)

T_{MAX} is the maximum junction temperature

T_A is the ambient temperature

T_C is the case temperature.

Maximum junction temperature (T_{MAX}) is normally 175°C for silicon and 100°C for germanium devices. Although usually 25°C, T_S can be other values of temperature.

This conventional derating approach makes the approximate assumption that the thermal resistance, θ, from ambient or case to junction is a constant, and that the junction temperature is:

$$T_J = T_A + \theta_{JA} P_J$$

or

$$T_J = T_C + \theta_{JC} P_J$$

where

T_J is junction temperature

T_A is ambient temperature

T_C is case temperature

θ_{JA} is thermal resistance (ambient to junction, °C per watt)

θ_{JC} is thermal resistance (case to junction, °C per watt)

P_J is power (watts) dissipated at junction.

These equations indicate that operation anywhere along the derating line between T_S and T_{MAX} will result in a junction temperature equal to T_{MAX} and that the thermal resistance (θ) is constant at a value:

$$\theta = \frac{T_{MAX} - T_S}{P_{(rating)}} \ ^oC/watt$$

where

$P_{(rating)}$ is power rating (watts) at temperature T_S.

This assumption of constant thermal resistance is approximate. For many common transistors, the assumption is close and conservative because their actual thermal resistance has only a slightly negative slope as a function of the temperature of the bulk semiconductor material. An actual curve of constant junction temperature for these devices resembles Figure 4-7.

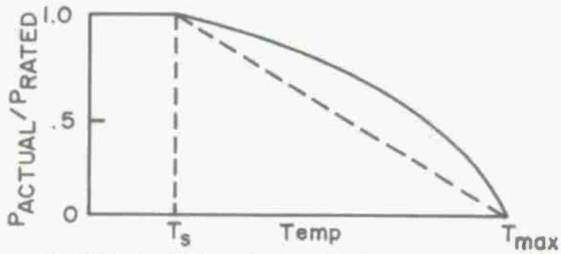


Fig. 4-7 ACTUAL CONSTANT JUNCTION TEMPERATURE CURVE

As shown in Figure 4-7, if the curvature of $T_J = T_{MAX}$ curve is large, then the assumption of the dotted straight line can lead to appreciable error. The fact that the curvature of $T_J = T_{MAX}$ can be different for the two cases of referencing θ_{JA} or θ_{JC} is one reason why differences may be obtained in using these two ratings in prediction computations.

This assumption error may be very large for some devices. This is recognized by suppliers who specify a multipoint derating curve to approximate, more closely, the extreme curvature in the constant $T_J = T_{MAX}$ curve. An example is the derating curve for the 1N3263 power diode, Figure 4-8, where the three rating points are 160 amps at 125°C, 120 amps at 150°C, 0 amps at 175°C. As shown in Figure 4-8, the two point linear derating assumption from 160 amps at 125°C would have resulted in an 80 amps rating at 150°C instead of the actual rating of 120 amps. This would have caused a third or more of the device capability to be wasted at 150°C.

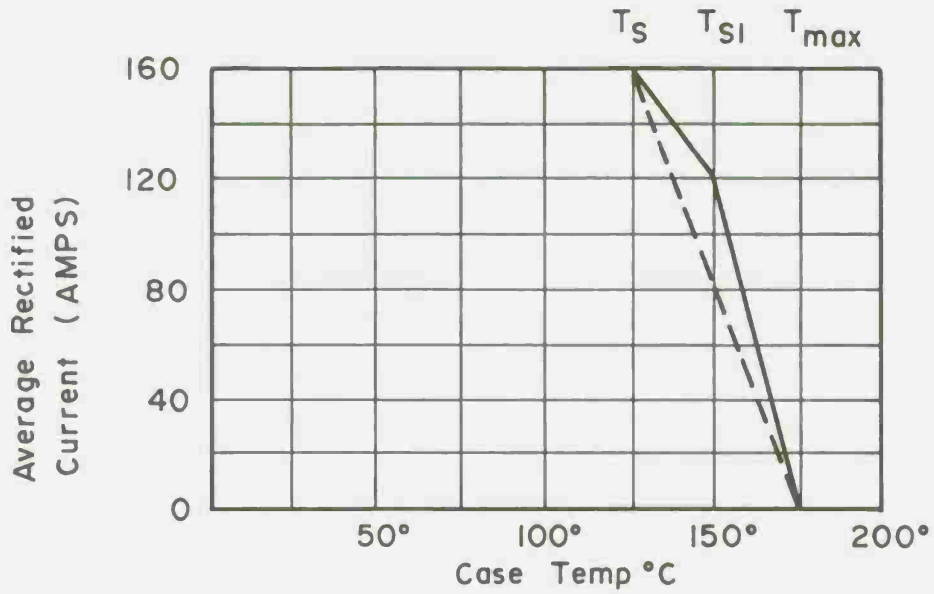


Fig. 4-8 MULTIPOINT DERATING CURVE FOR IN3263 POWER DIODE

Occasionally in the Military Specifications, the derating instructions are presented as notes relative to the maximum ratings. The slash sheets appended to MIL-S-19500 contain numerous examples of derating instructions for discrete semiconductor devices.

4.1.2.2 Specific Derating Guidelines

This subsection provides specific guidelines for derating component parts used in electronic equipment. In general, guidelines and graphic presentation of acceptable part operation are given for the environmental classes covering ground, airborne and space applications.

These guidelines represent a composite summary of derating policies employed presently by firms within the electronic industry who specialize in military applications. The derating criteria for resistors, capacitors and semiconductors are presented in graphic format and include parametric restrictions for both stress ratios and case temperatures. The derating criteria for microcircuits, inductive devices, relays and connectors are presented in tabular format. The graphs show three basic derating regions which are defined as follows:

A Acceptable--the most reliability/cost effective region providing the optimum margin of safety. Usage of parts in this region is recommended. No reliability degradation is expected.

Q Questionable--the region in which the devices are operated within their ratings but are not optimum with respect to reliability. Long term reliability can be degraded. The designer should consult with the reliability or component engineer regarding part application.

R Restricted--the region in which the device ratings are exceeded. Do not use; part overstressed.

In addition to providing an adequate margin of safety, Region A reflects cost/effectiveness precepts. As a general rule, the specific derating guidelines (Region A) should not be conservative to the point where costs rise excessively (e.g., higher than necessary part ratings are selected). Neither should the derating criteria be so loose as to render reliable part application ineffective. Optimum derating occurs at or below the point on the stress/temperature curve where a rapid increase in failure rate is noted for a small increase in temperature or stress. This may be visualized by referring to Figure 4-5 (when considering a silicon NPN transistor) presented in the preceding subsection.

Consider that the transistor is used at $55^{o}C$ ambient temperature rated for 500 mW at $25^{o}C$ and used at two different stress levels 400 mW = 80% and 200 mW = 40%. Referring to Figure 4-5, at a stress of 80% and a temperature of $55^{o}C$, the failure rate λ_b is 0.33×10^{-6}. It can also be seen that 80% stress or 400 mW is the maximum allowable power dissipation at $55^{o}C$ for this transistor. If, however, the transistor is stressed only 40% at $55^{o}C$, the failure rate λ_b decreases drastically to 0.010×10^{-6}. A considerable reliability improvement of 3.3 to 1 has been achieved.

Table 4-29 and Figures 4-9 through 4-11 present the derating guidelines for microcircuits. Figures 4-12 through 4-16 give the derating guidelines for semiconductors. Figure 4-17 through 4-20 show the derating guidelines for resistors. Figure 4-21 through 4-30 show the derating

Table 4-29 MICROELECTRONIC DEVICE DERATING CHART

Power Supply Voltage(s) - Use power supply voltage at parameter guarantee level which is derated from absolute maximum ratings.

Output Current (Load, Fan-Out) - Derate to 80% of maximum allowable.

Input Voltage - Logic - Derate to same voltage level as noted above for supply voltage(s).

Input Voltage - Linear - Derate to 70% of absolute maximum rating.

$$T_J = T_A + \theta_{JA}(P_D)$$

$$T_C = T_J - \theta_{JC}(P_D)$$

For: Digital Logic Device Application

$$P_D = \frac{I_{PDL} + I_{PDH}}{2} \times V_{cc} + (I_{OL} \times V_{OL})$$

where

P_D is the actual power dissipated in the circuit application and is the product of the actual measured calculated voltage and current.

I_{PDL} is the actual supply current drain with inputs in logic "0" state.

I_{PDH} is the actual supply current drain with inputs in logic "1" state.

V_{cc} is the actual power supply voltage.

I_{OL} is the actual output logic "0" state sink currents.

V_{OL} is the actual logic state "0" output voltage.

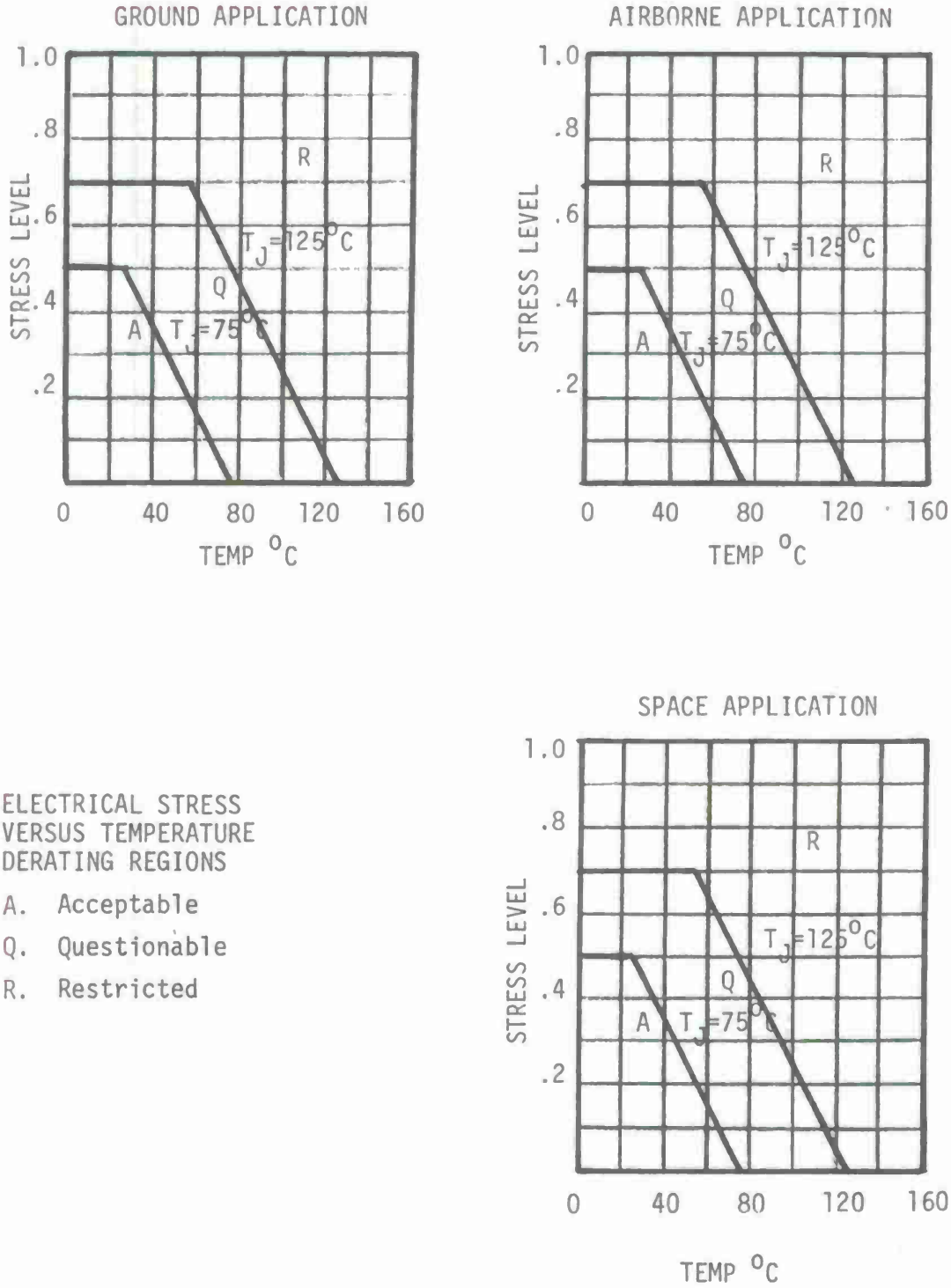
For: Linear Device Application

$$P_D = V_s^+ \times I_{ss}^+ + V_s^- \times I_{ss}^-$$

where

V_s is the actual supply voltage ($\pm$)

I_{ss} is the actual supply current ($\pm$).



ELECTRICAL STRESS
VERSUS TEMPERATURE
DERATING REGIONS

A. Acceptable

Q. Questionable

R. Restricted

Figure 4-9 MICROCIRCUIT, MAX OPERATING JUNCTION TEMP, 125°C

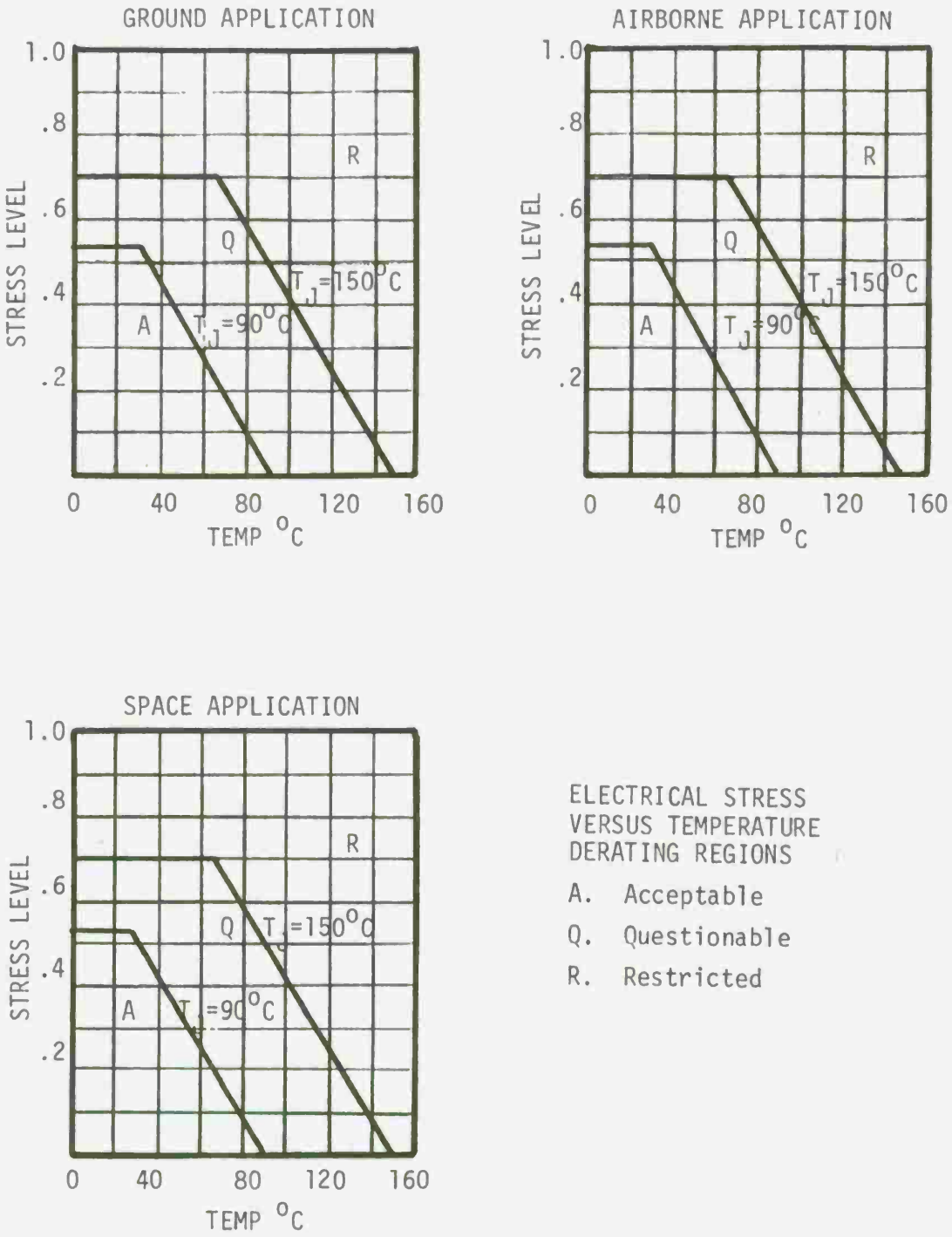
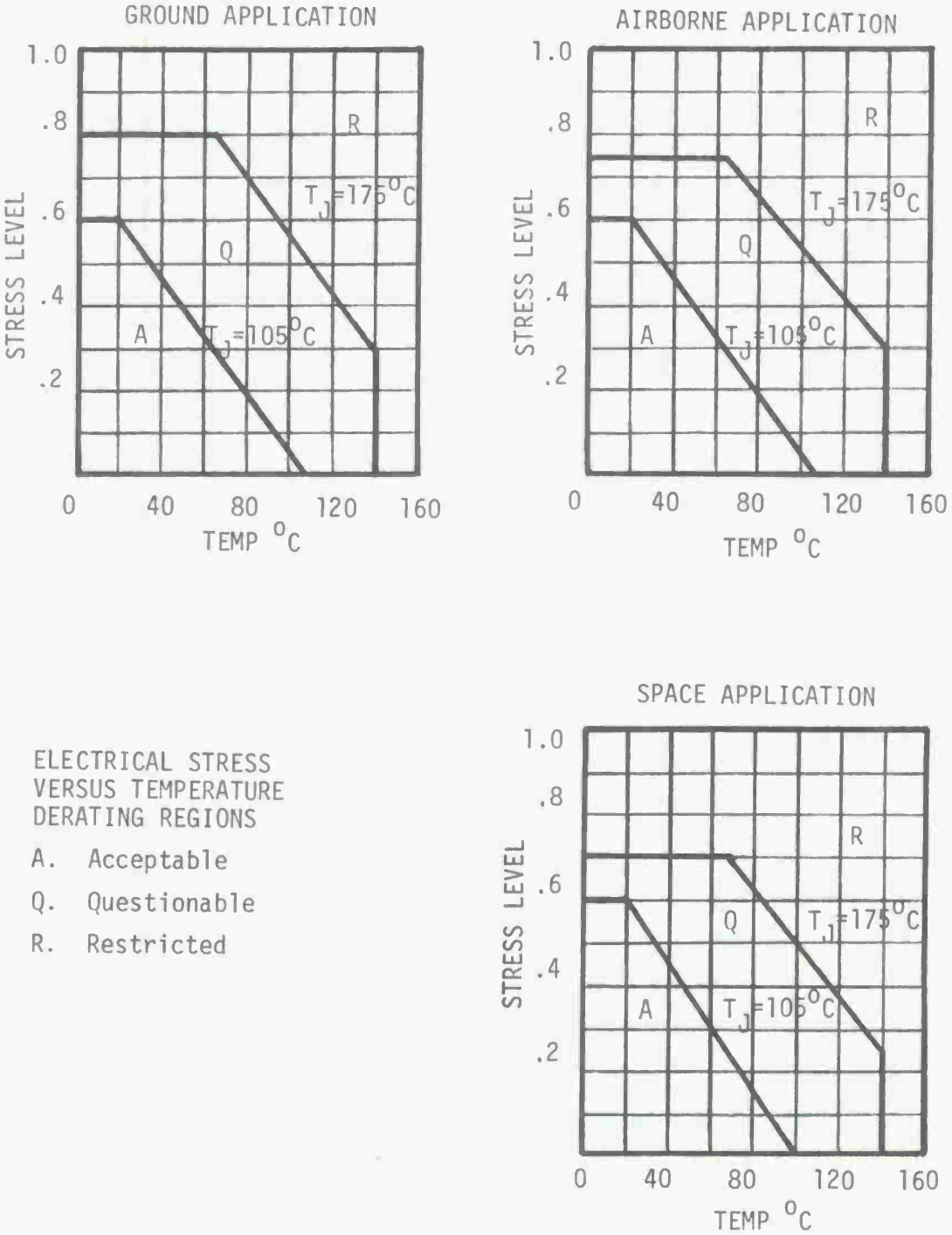


Figure 4-10 MICROCIRCUIT, MAX OPERATING JUNCTION TEMP, 150°C



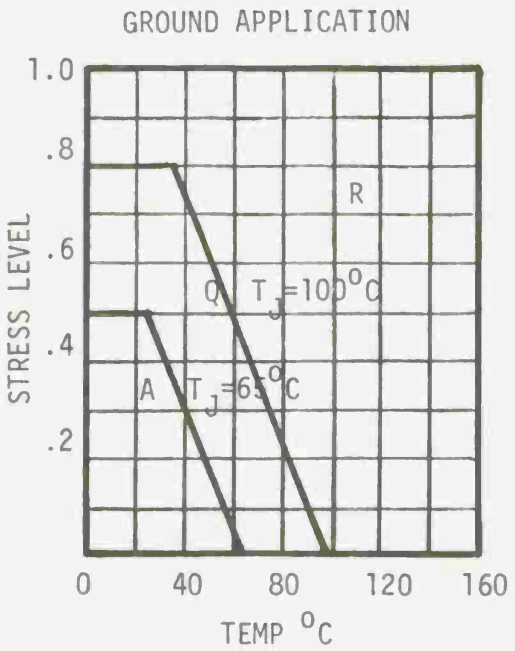
ELECTRICAL STRESS
VERSUS TEMPERATURE
DERATING REGIONS

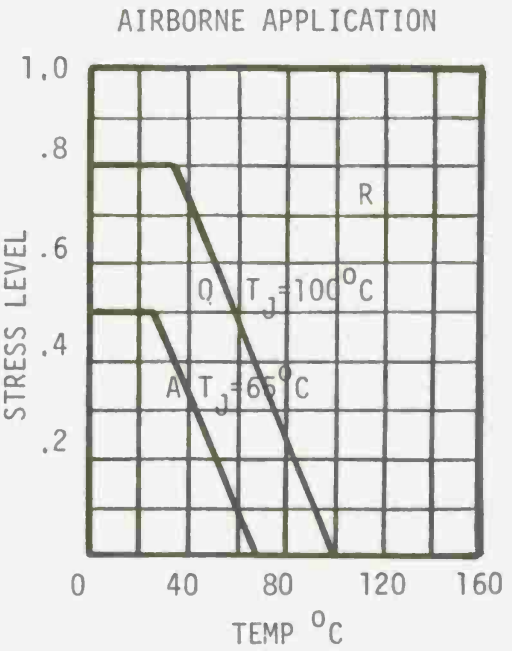
A. Acceptable

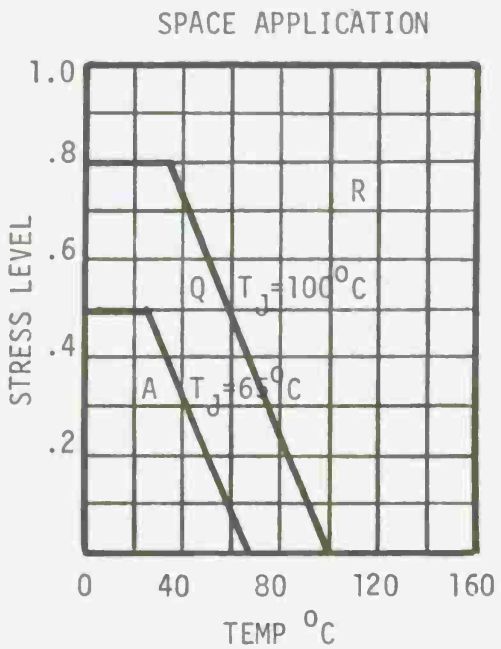
Q. Questionable

R. Restricted

Figure 4-11 MICROCIRCUIT, MAX OPERATING JUNCTION TEMP, 175°C







ELECTRICAL STRESS VERSUS TEMPERATURE DERATING

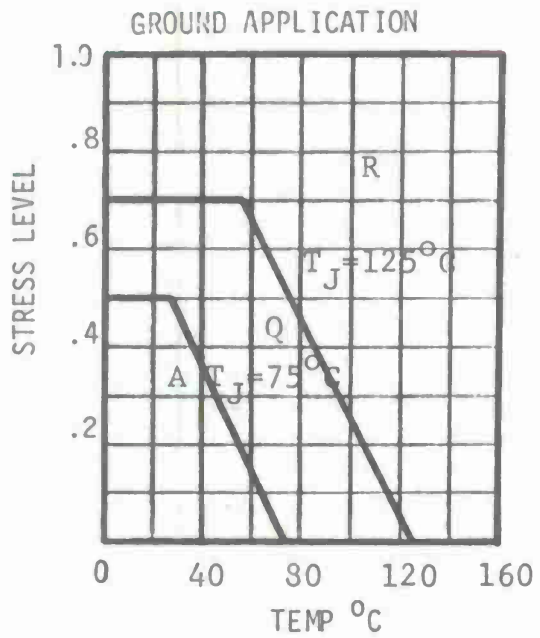
A. Acceptable

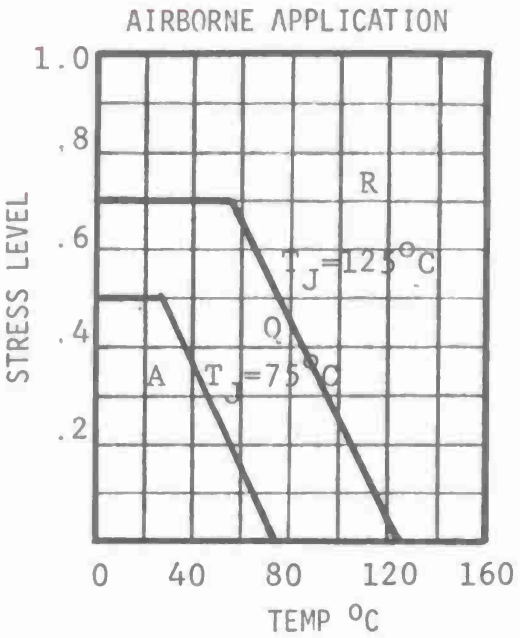
Q. Questionable

R. Restricted

NOTES:
- Diodes
  $I_f \leq 75\%$
  PIV $\leq$ 80%
- Transistors
  $I_c \leq 80\%$
- Any Voltage
  $\leq 90\%$

Figure 4-12 SEMICONDUCTOR, MAX OPERATING JUNCTION TEMP, 100°C





ELECTRICAL STRESS
VERSUS TEMPERATURE
DERATING REGIONS

A. Acceptable

Q. Questionable

R. Restricted

NOTES:
- Diodes
  $I_f \leq 75\%$
  PIV $\leq 80\%$
- Transistors
  $I_c \leq 80\%$
- Any Voltage
  $\leq 90\%$

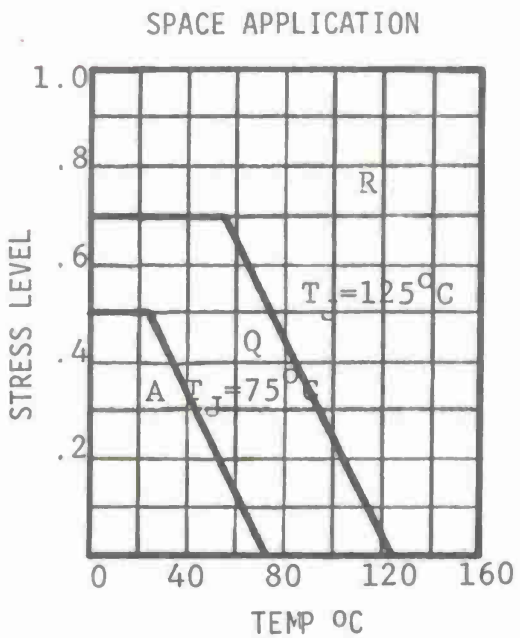
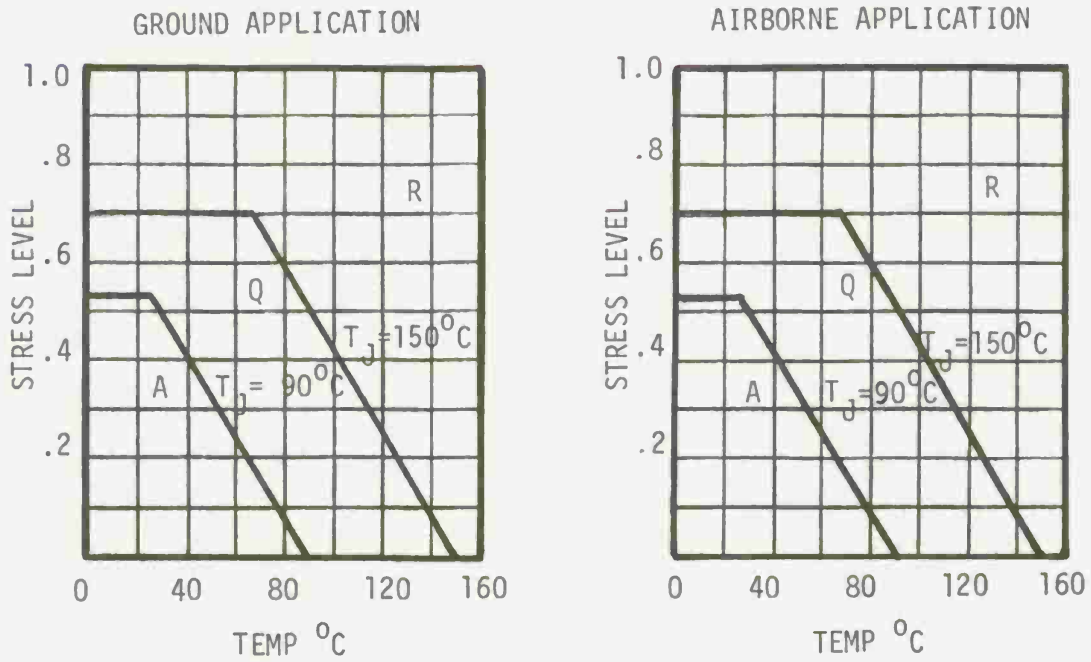
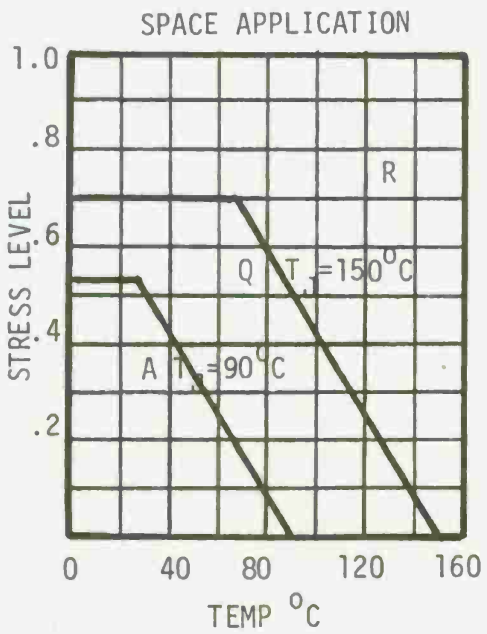


Figure 4-13 SEMICONDUCTOR, MAX OPERATING JUNCTION TEMP, 125°C





ELECTRICAL STRESS
VERSUS TEMPERATURE
DERATING REGIONS

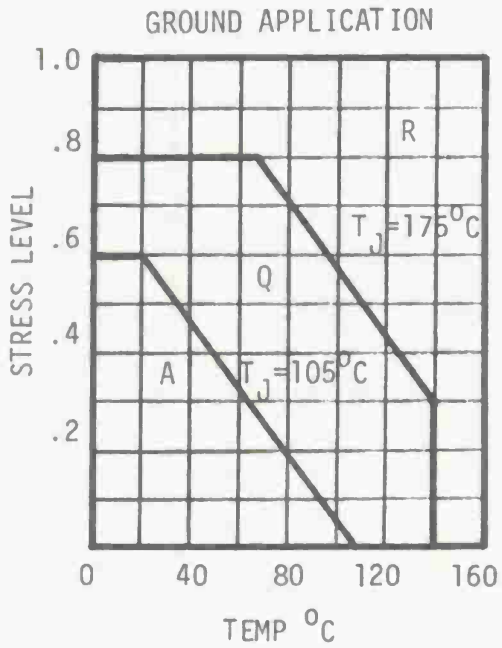
A. Acceptable

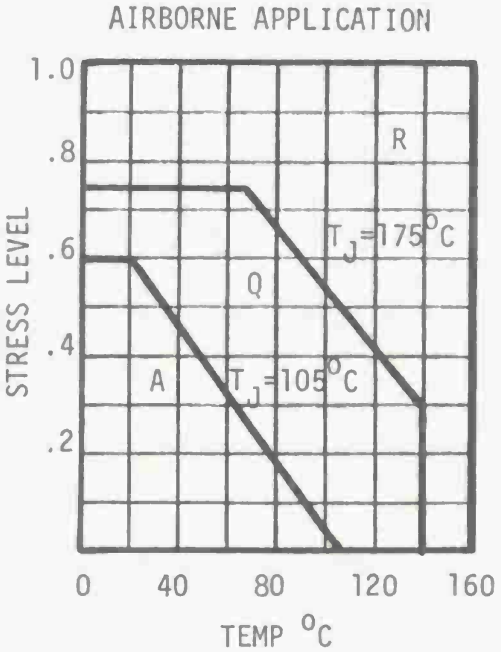
Q. Questionable

R. Restricted

NOTES:
- Diodes
  $I_f \leq 75\%$
  PIV $\leq 80\%$
- Transistors
  $I_c \leq 80\%$
- Any Voltage
  $\leq 90\%$

Figure 4-14 SEMICONDUCTOR, MAX OPERATING JUNCTION TEMP, 150°C





ELECTRICAL STRESS
VERSUS TEMPERATURE
DERATING REGIONS

A. Acceptable

Q. Questionable

R. Restricted

NOTES:
- Diodes
  $I_f \leq 75\%$
  $PIV \leq 80\%$
- Transistors
  $I_C \leq 80\%$
- Any Voltage
  $\leq 90\%$

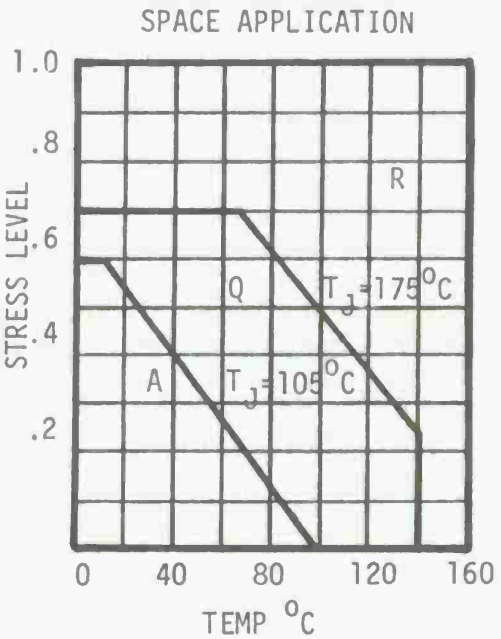
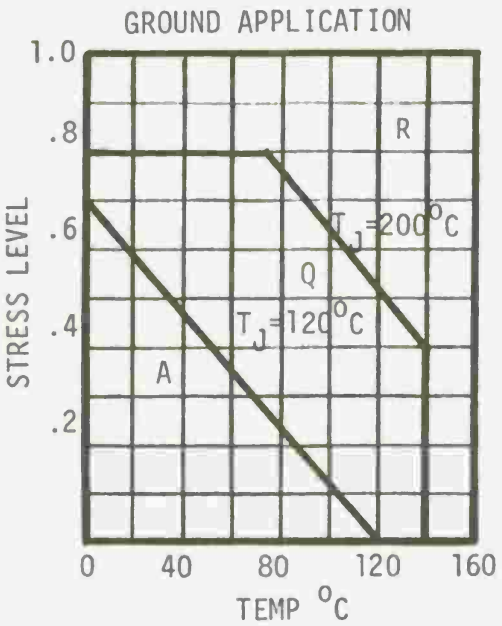
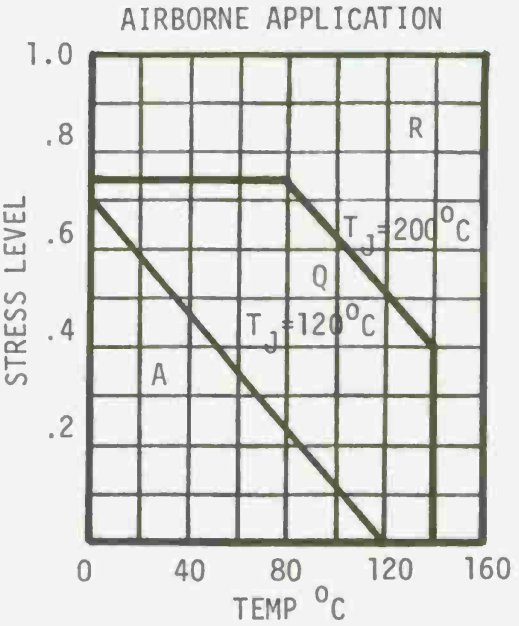
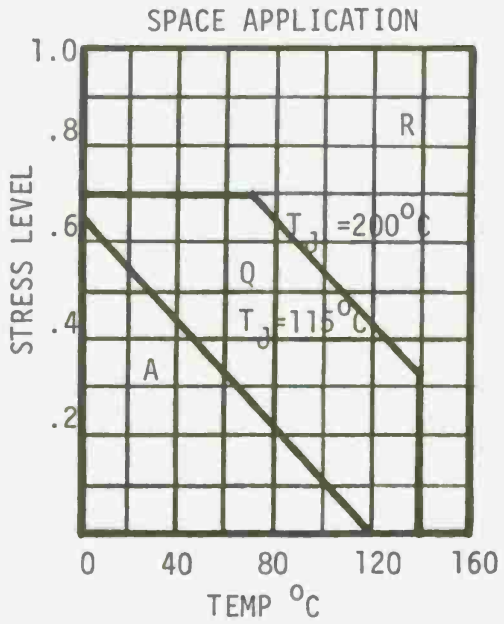


Figure 4-15 SEMICONDUCTOR, MAX OPERATING JUNCTION TEMP, 175°C







ELECTRICAL STRESS
VERSUS TEMPERATURE
DERATING REGIONS

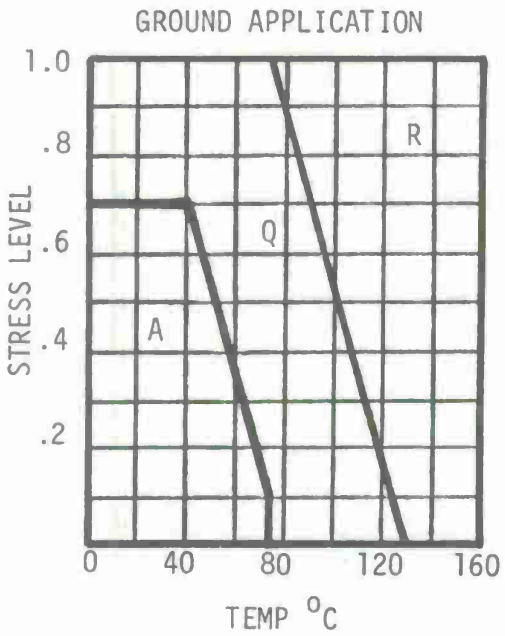
A. Acceptable

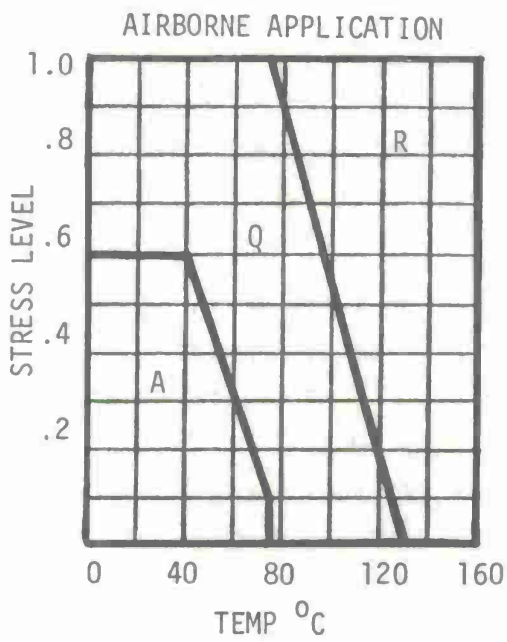
Q. Questionable

R. Restricted

NOTES:
- Diodes
  $I_f \leq 75\%$
  PIV $\leq$ 80%
- Transistors
  $I_c \leq 80\%$
- Any Voltage
  $\leq$ 90%

Figure 4-16 SEMICONDUCTOR, MAX OPERATING JUNCTION TEMP, 200°C





ELECTRICAL STRESS
VERSUS TEMPERATURE
DERATING REGIONS

A. Acceptable

Q. Questionable

R. Restricted

NOTE: Peak Voltage and Current Shall Not Exceed 75% of Rated Values

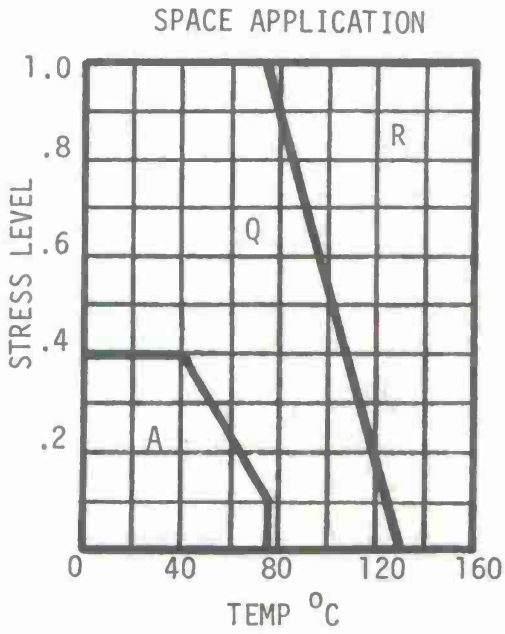
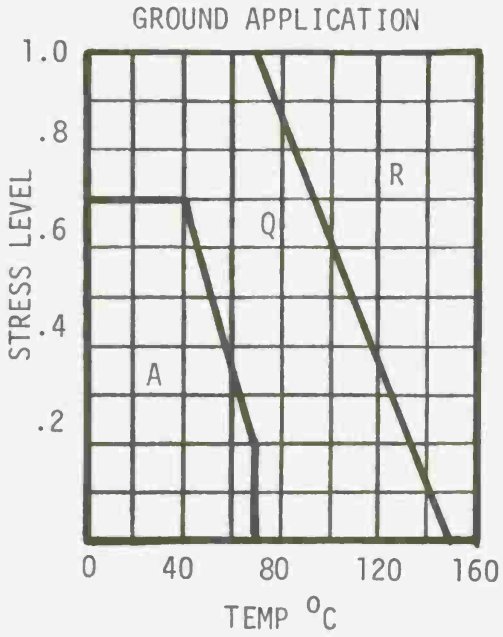
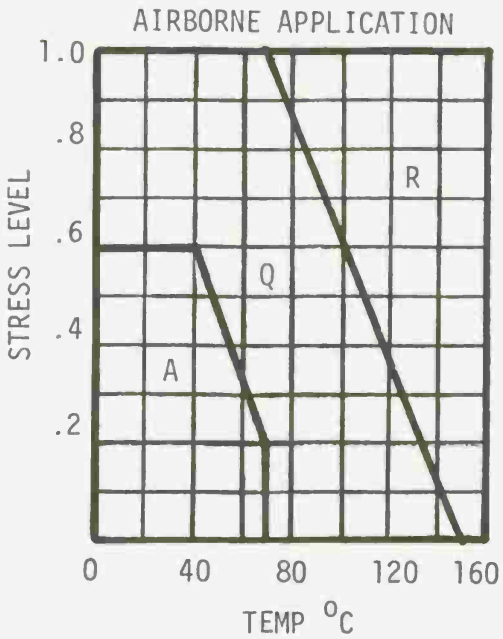
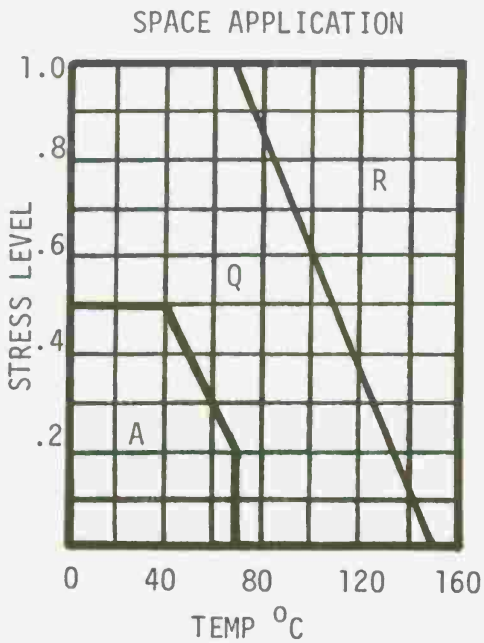


Figure 4-17 RESISTOR, FIXED, CARBON COMPOSITION (RCR)







ELECTRICAL STRESS VERSUS TEMPERATURE DERATING REGIONS

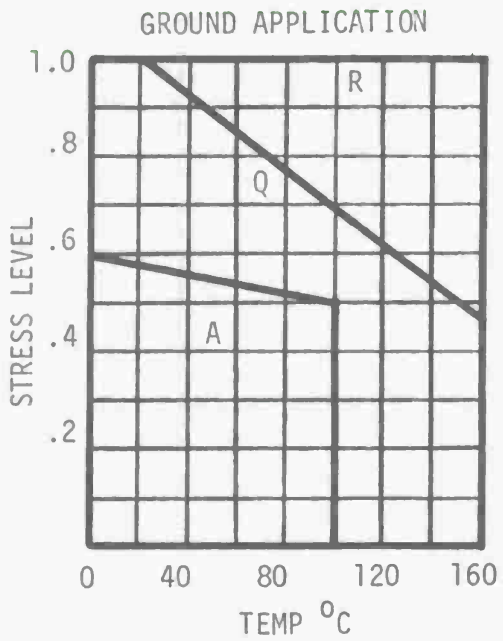
A. Acceptable

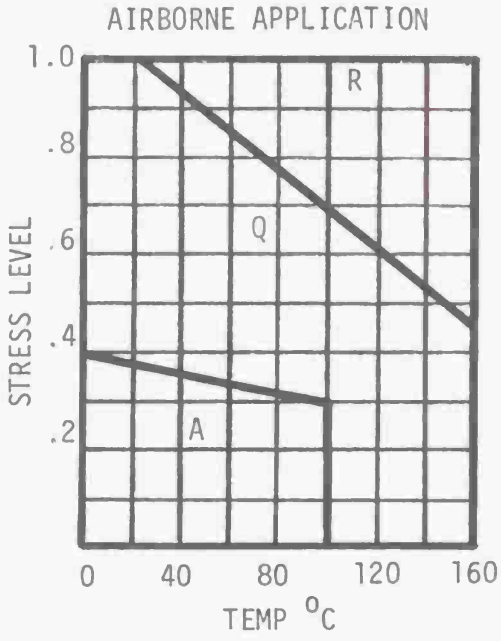
Q. Questionable

R. Restricted

NOTES:
- Peak Power Not to Exceed Rated Power
- Applied Voltage Not to Exceed 75% of Rating

Figure 4-18 RESISTOR, FIXED, METALFILM (RLR, RNR)





ELECTRICAL STRESS
VERSUS TEMPERATURE
DERATING REGIONS

A. Acceptable

Q. Questionable

R. Restricted

NOTES:
- Peak Power Not to Exceed Rated Power
- Applied Voltage Not to Exceed 75% of Rating

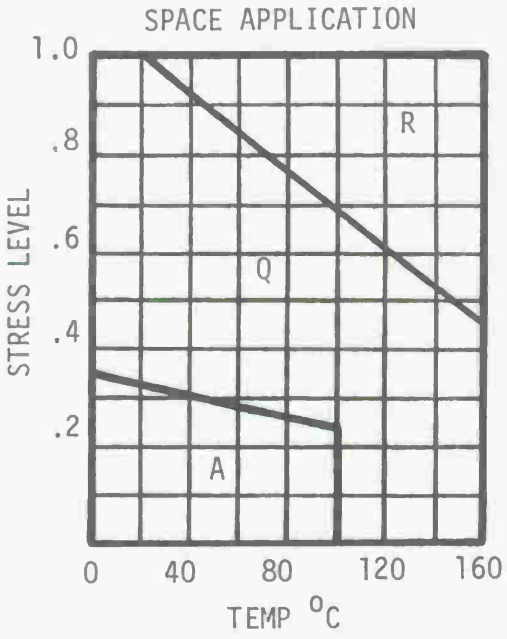
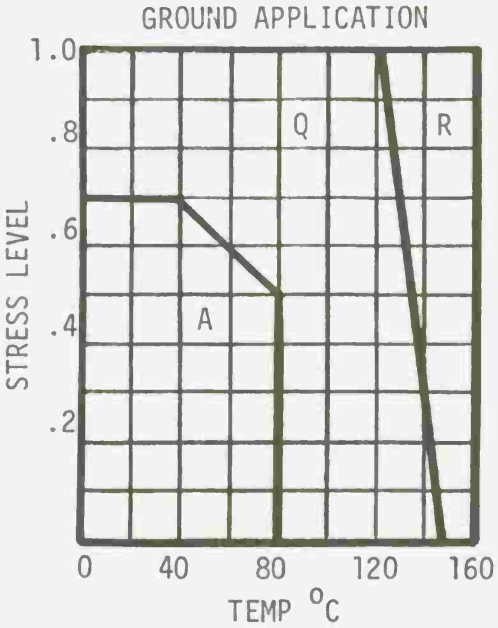
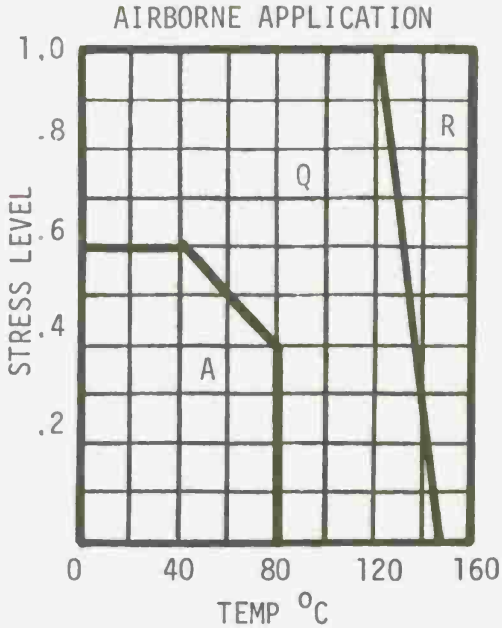
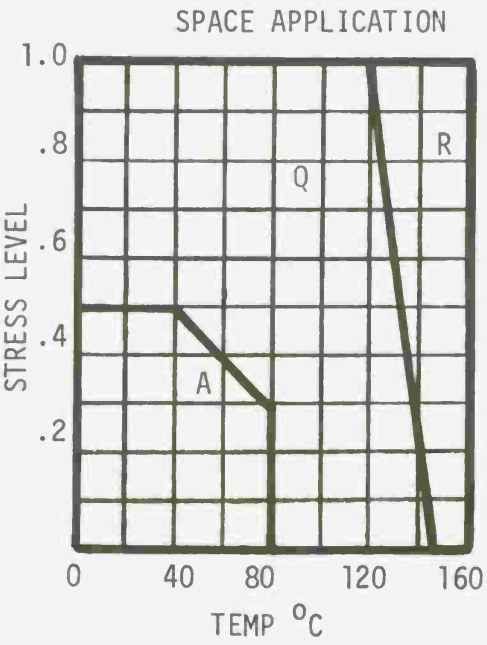


Figure 4-19 RESISTOR, POWER, WIREWOUND (RER, RWR)







ELECTRICAL STRESS VERSUS TEMPERATURE DERATING REGIONS

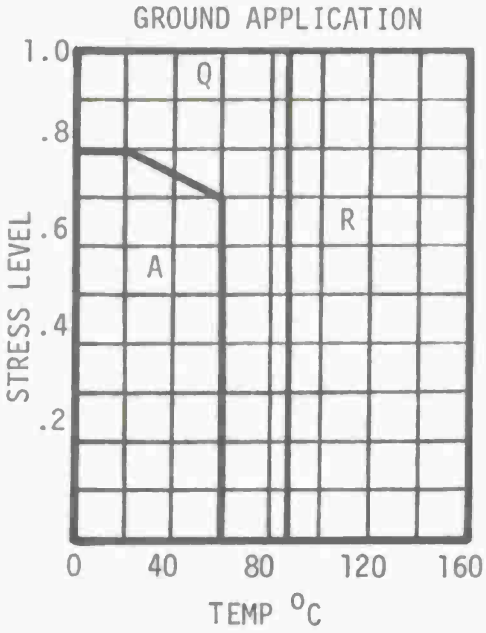
A. Acceptable

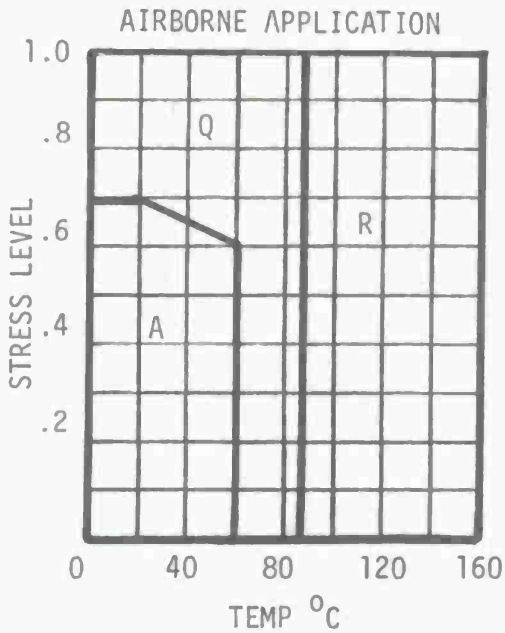
Q. Questionable

R. Restricted

NOTES:
- Peak Power Not to Exceed Rated Power
- Applied Voltage Not to Exceed 75% of Rating

Figure 4-20 RESISTOR, PRECISION, WIREBOUND (RBR)





ELECTRICAL STRESS
VERSUS TEMPERATURE
DERATING REGIONS

A. Acceptable

Q. Questionable

R. Restricted

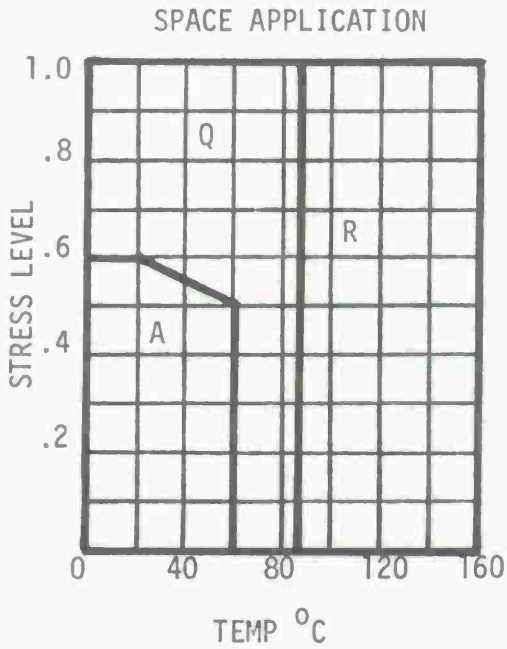


Figure 4-21 CAPACITOR, MICA (CM)

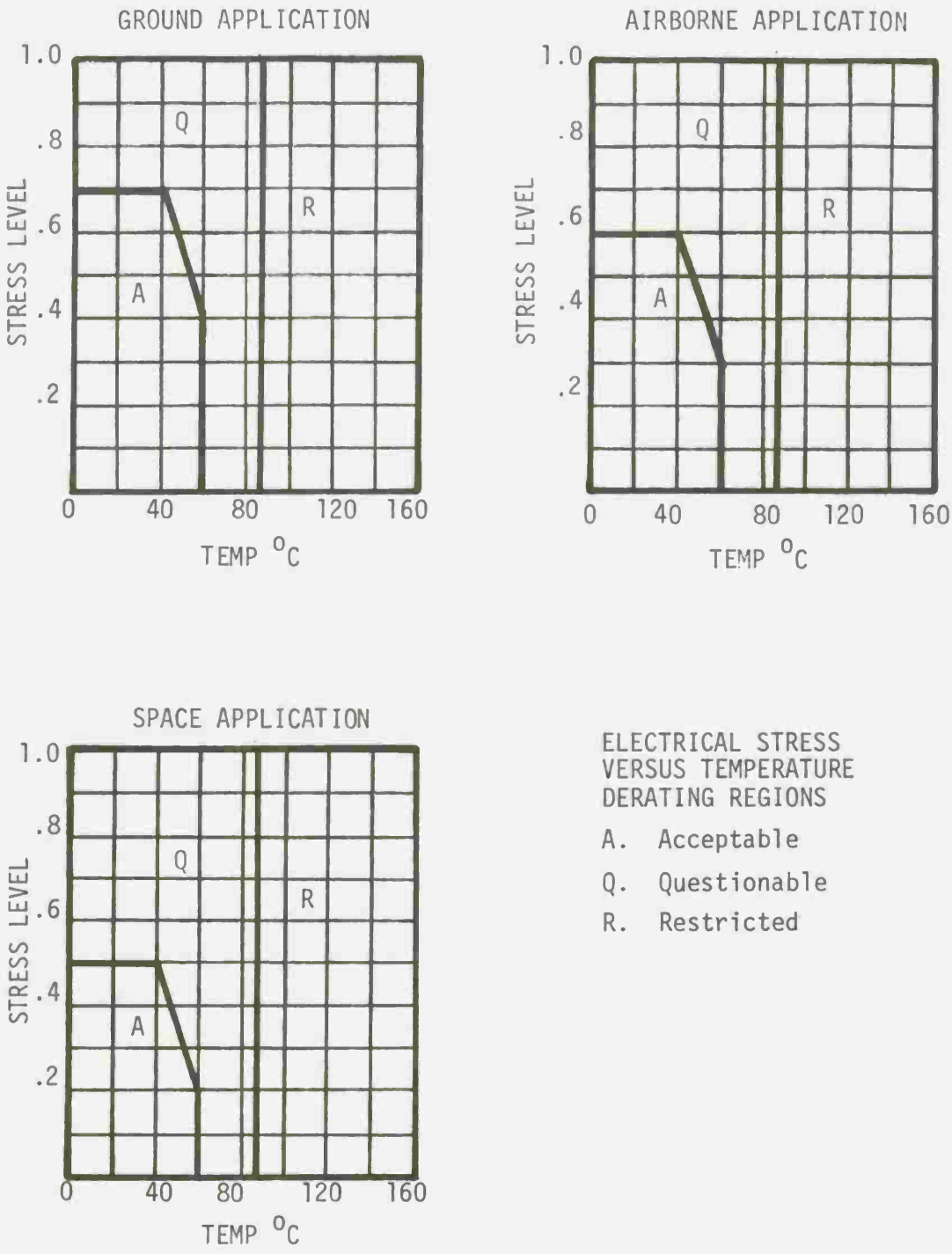
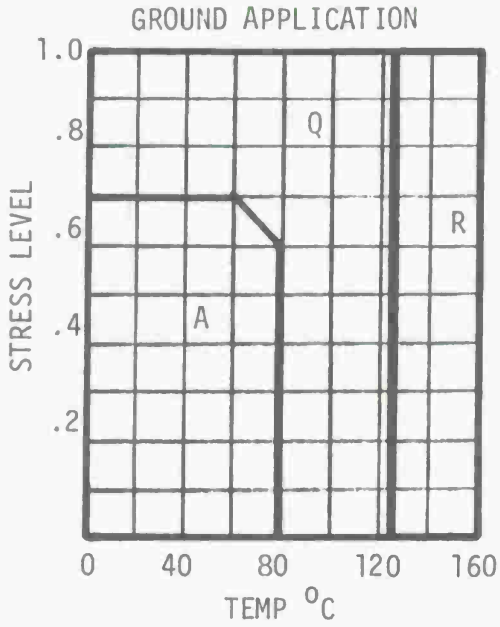
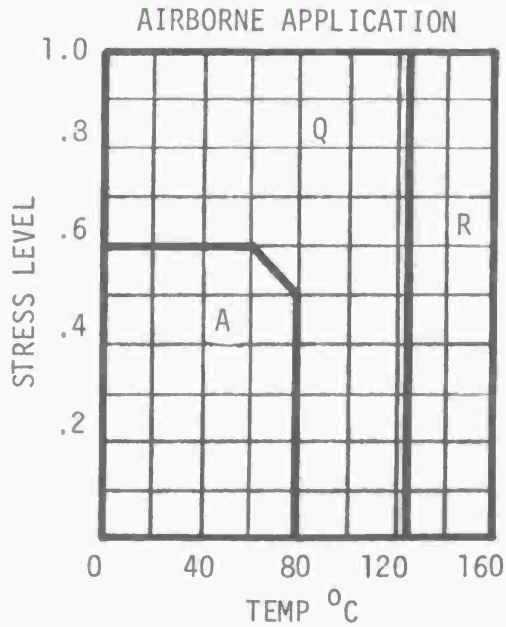


Figure 4-22 CAPACITOR, CERAMIC, TEMP COMPENSATING





ELECTRICAL STRESS
VERSUS TEMPERATURE
DERATING REGIONS

A. Acceptable

Q. Questionable

R. Restricted

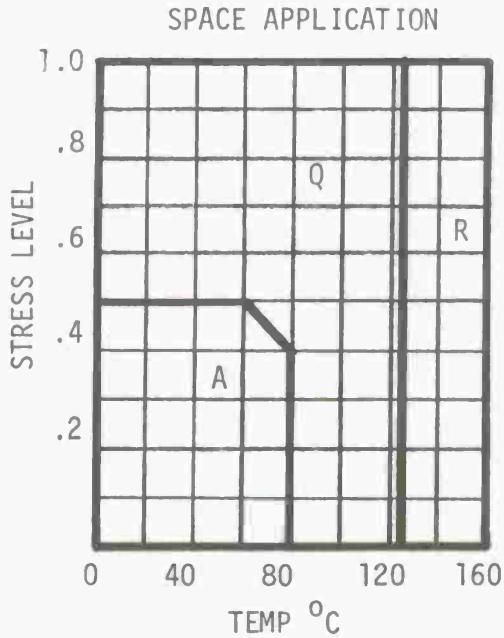
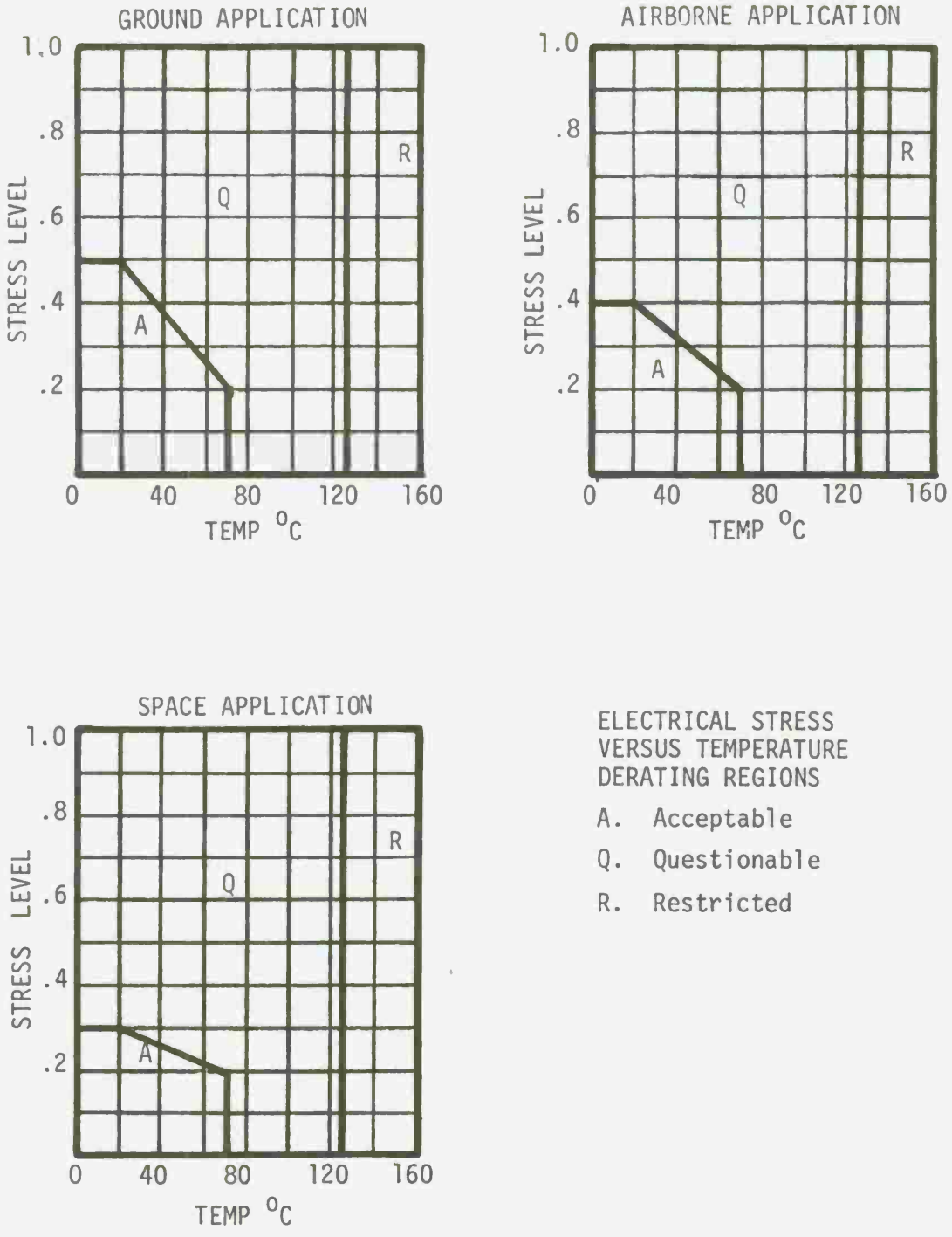


Figure 4-23 CAPACITOR, PAPER-PLASTIC OR METALLIZED (CPV, CH) MAX TEMP, 125°C



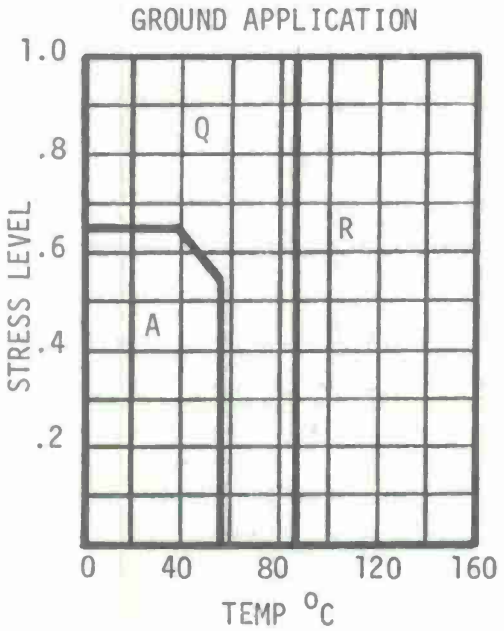
ELECTRICAL STRESS
VERSUS TEMPERATURE
DERATING REGIONS

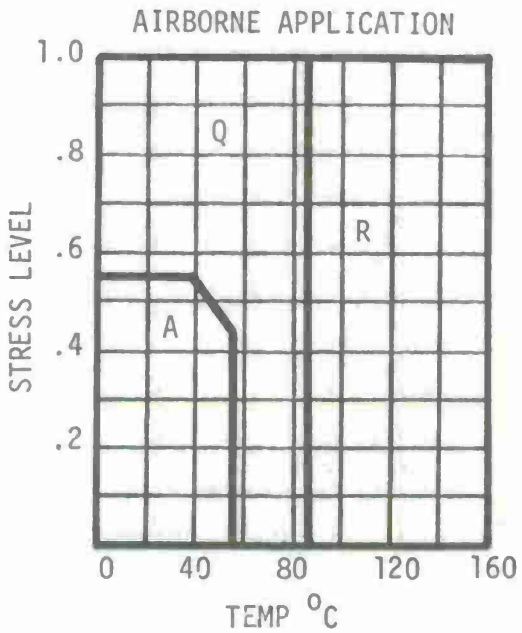
A. Acceptable

Q. Questionable

R. Restricted

Figure 4-24 CAPACITOR, AIR TRIMMER





ELECTRICAL STRESS
VERSUS TEMPERATURE
DERATING REGIONS

A. Acceptable

Q. Questionable

R. Restricted

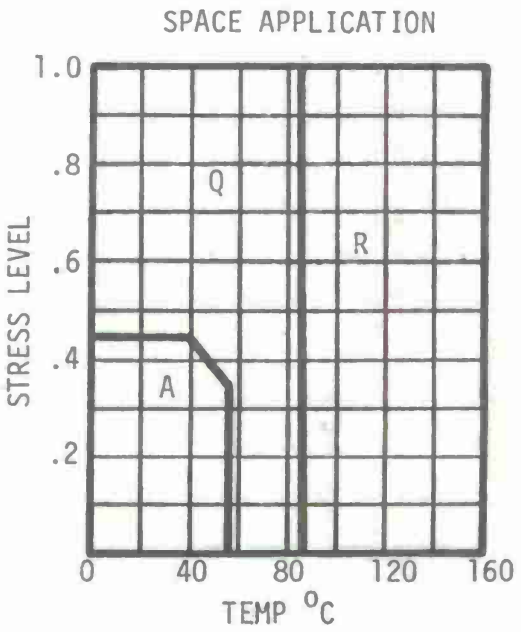


Figure 4-25 CAPACITOR, CERAMIC, GP, MAX TEMP, 85°C

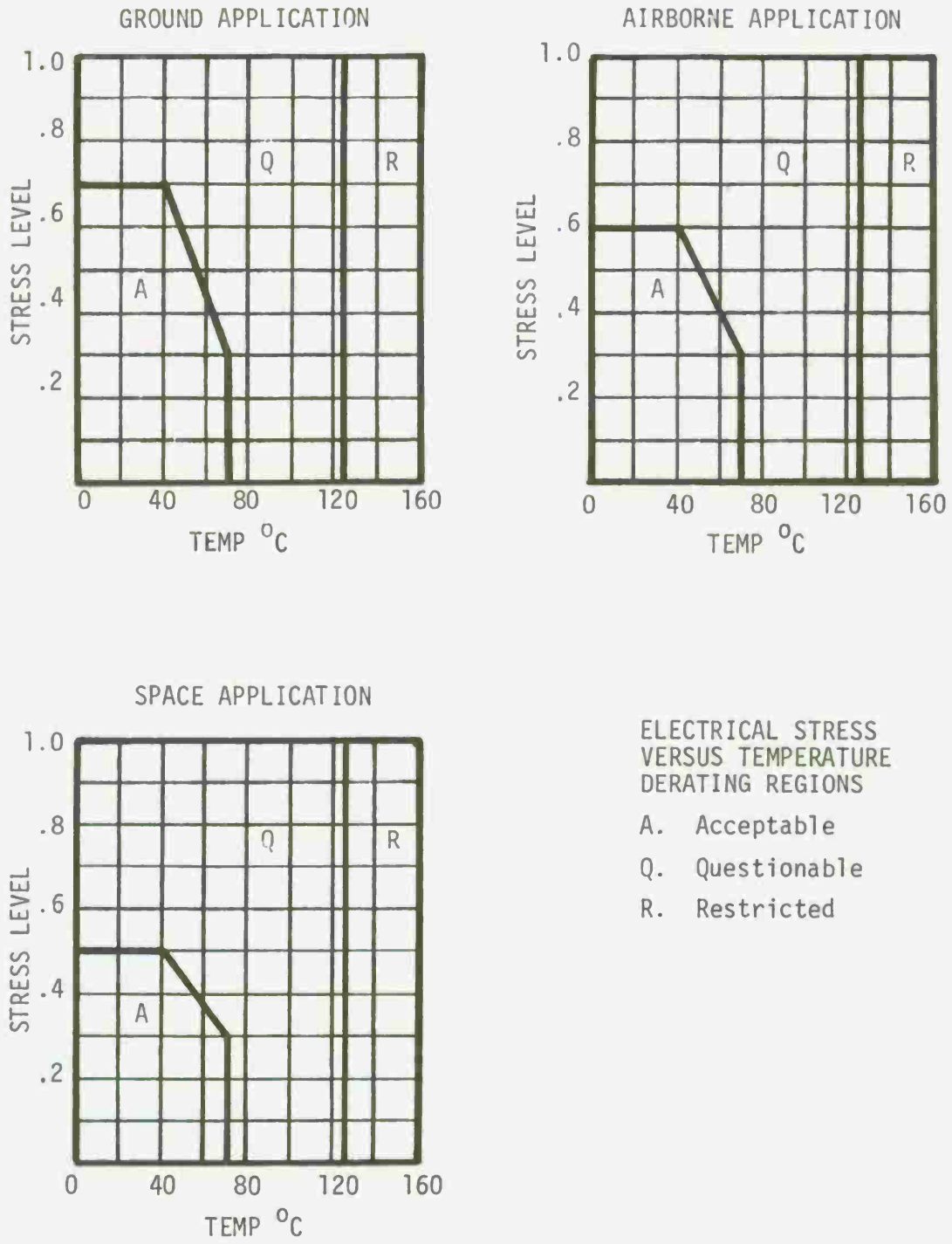
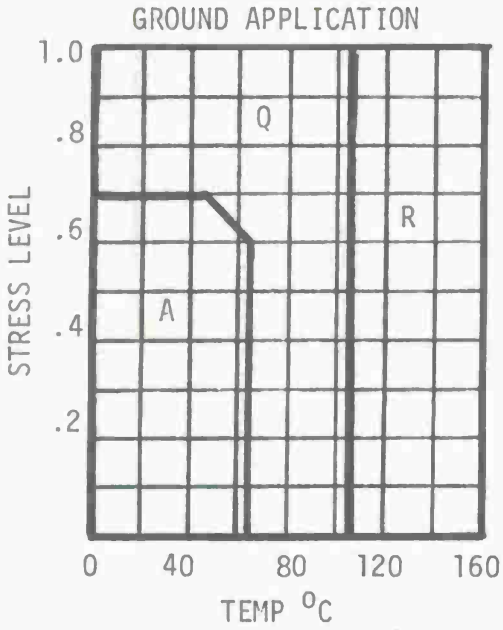
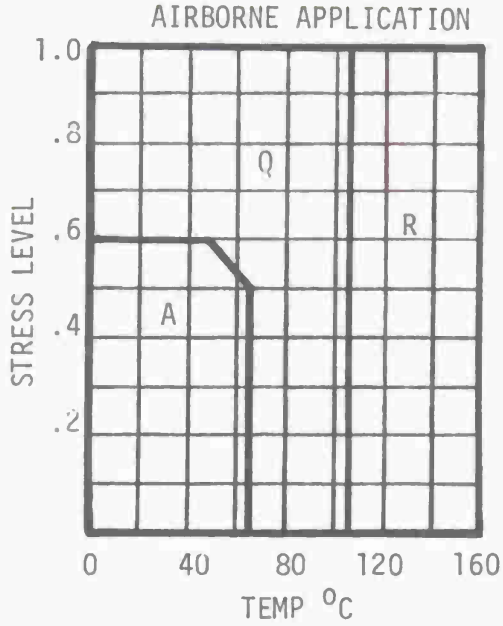


Figure 4-26 CAPACITOR, CERAMIC, GP, MAX TEMP, 125°C





ELECTRICAL STRESS
VERSUS TEMPERATURE
DERATING REGIONS

A. Acceptable

Q. Questionable

R. Restricted

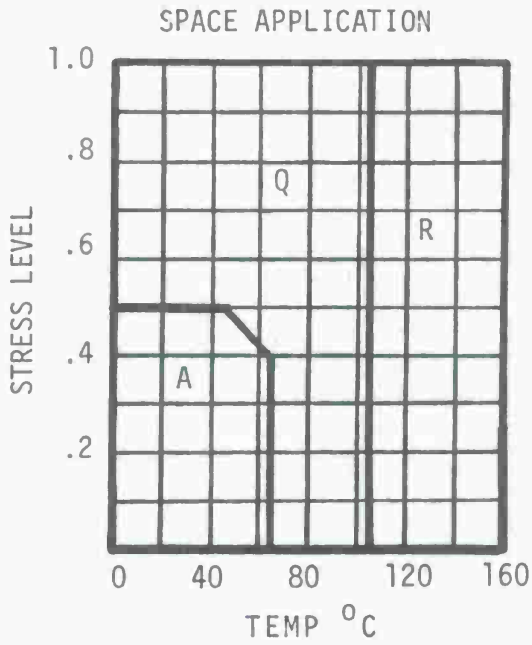
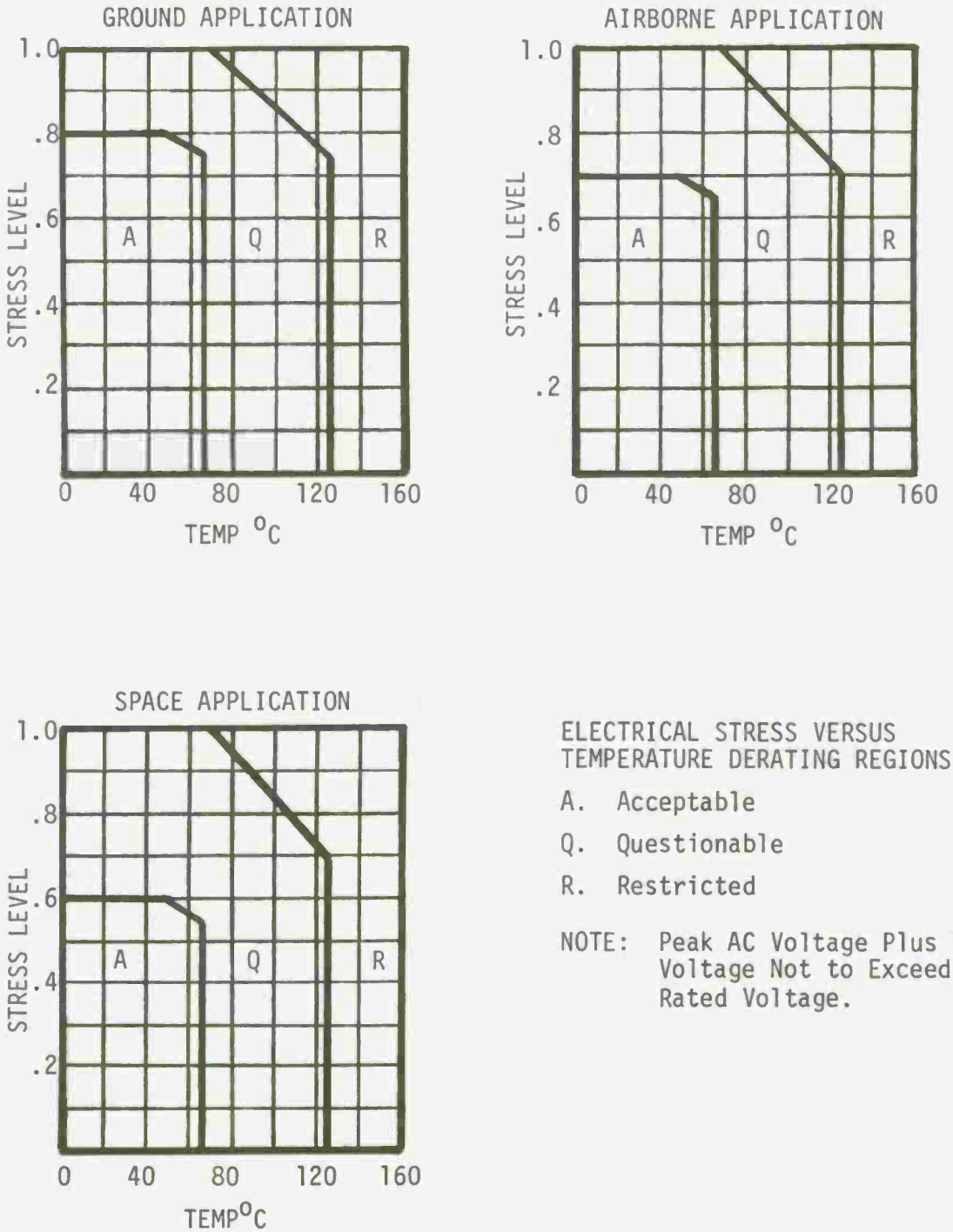


Figure 4-27 CAPACITOR, PAPER-PLASTIC OR METALLIZED (CPV, CH)



ELECTRICAL STRESS VERSUS TEMPERATURE DERATING REGIONS

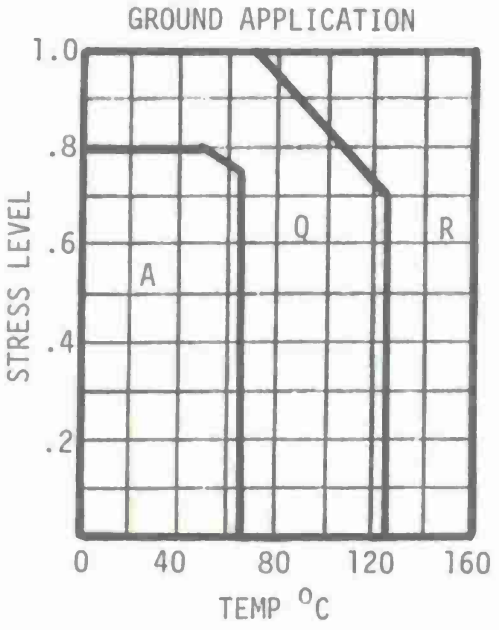
A. Acceptable

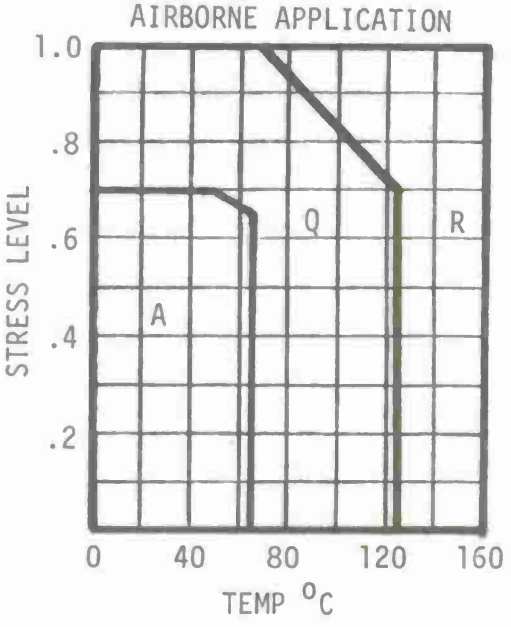
Q. Questionable

R. Restricted

NOTE: Peak AC Voltage Plus DC Voltage Not to Exceed Rated Voltage.

Figure 4-28 CAPACITOR, TANTALUM, WET ELECTROLYTE (CLR)





ELECTRICAL STRESS VERSUS TEMPERATURE DERATING REGIONS

A. Acceptable

Q. Questionable

R. Restricted

NOTES:

- Provide Series Circuit Impedance $\geq$ 3 ohms
- Max Reverse DC Voltage

  25°C - 5%
  85°C - 1.5%
  125°C - 0.5%

- No Reverse Ripple Permitted

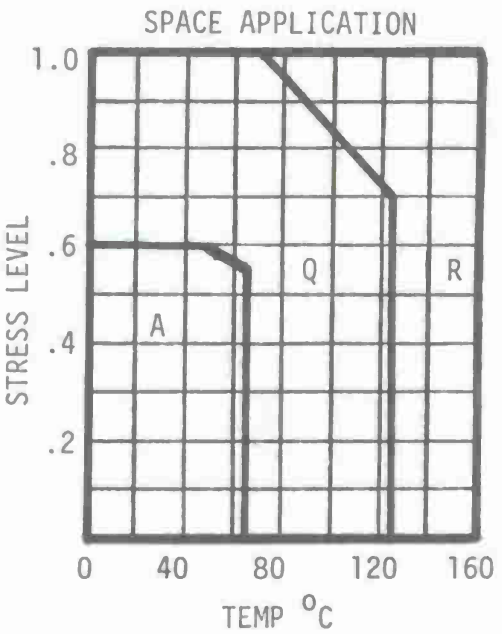
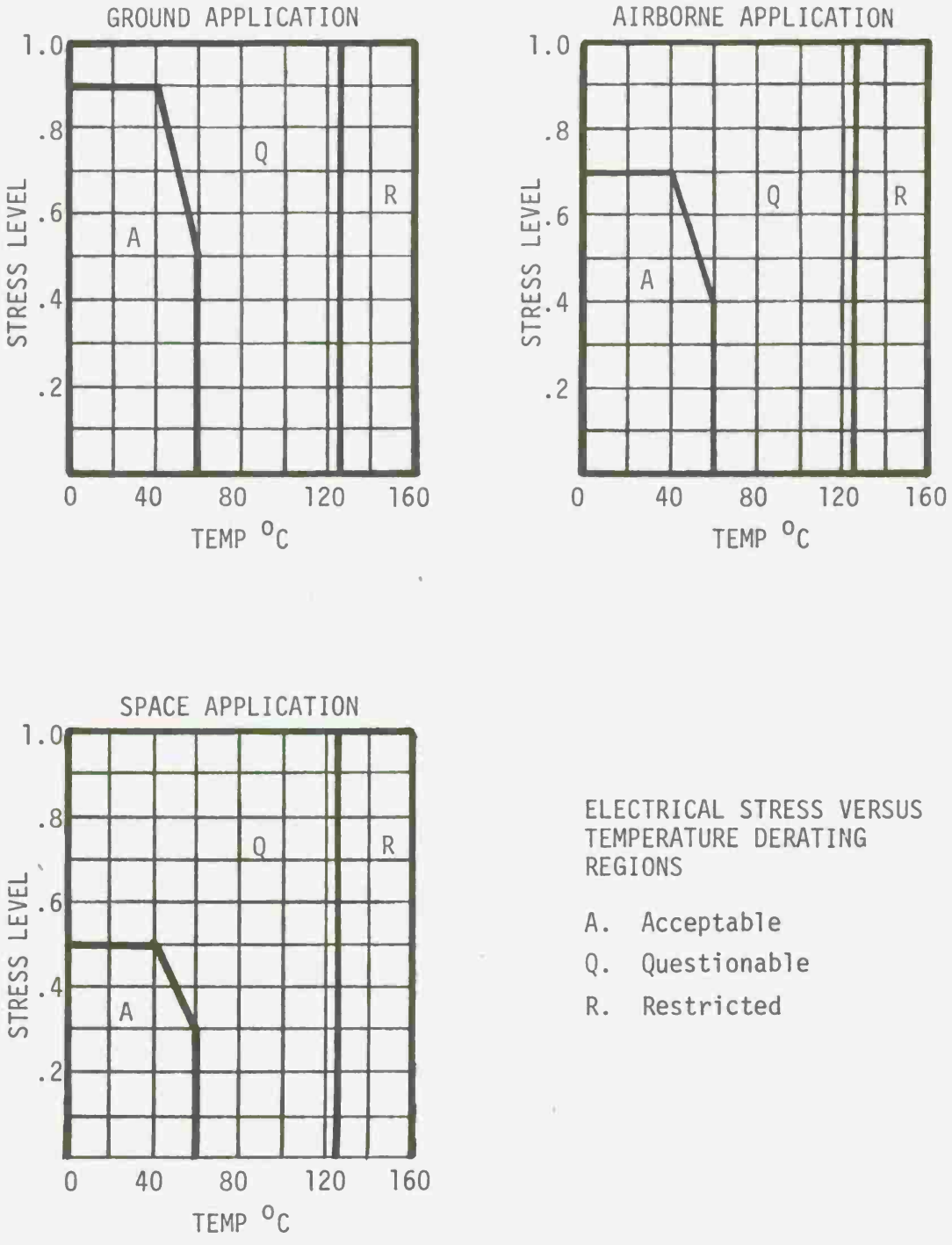


Figure 4-29 CAPACITOR, TANTALUM, SOLID (CSR)



ELECTRICAL STRESS VERSUS TEMPERATURE DERATING REGIONS

A. Acceptable

Q. Questionable

R. Restricted

Figure 4-30 CAPACITOR, GLASS (CY)

guidelines for capacitors. Tables 4-30 through 4-32 provide guidelines for other parts. Where derating information is graphically presented, the figures show three basic regions of part operation which impact reliability.

Table 4-30 DERATING FOR COILS, CHOKES AND TRANSFORMERS

Inductor Type	Maximum Permissible % of Manufacturer's Rating		
		Voltage	
	Current Operating	Maximum Applied	Transient (maximum)
Coil, Inductor Saturable Reactor	60%	60%	90%
Coil, Radio Frequency Fixed	70%	60%	90%
Inductor General	70%	60%	90%
Transformer, Audio	70%	60%	90%
Transformer Pulse, Low Power	60%	60%	70%
Transformer, Power	70%	60%	90%
Transformer, Radio Frequency	60%	60%	90%
Transformer, Saturable Core	60%	60%	90%

Table 4-31 RELAY DERATING CHART

Part Type	Stress Parameter	% Stress (Allowed)	Remarks
Relay	Rated Contact Current	50%	The rated contact current for each contact set shall be derated by 50%. Each active contact set must be calculated separately. a. Active means actually wired to serve a circuit function. b. Each circuit path through the relay constitutes a contact set.

NOTE:

1. Consideration must be given to the type of load to be switched, i.e., inductive, capacitive, lamp resistive, or motor when computing operating current.
2. Rated current means the maximum current for a given type of load which the relay will make, carry and break for its rated life.
3. Adequate contact protection must be provided where applicable.
4. Exercise care in the area of power switching with grounded case relays.

Table 4-32 CONNECTOR DERATING CHART

Connector Type	Stress Parameter	% Stress (Allowed)
R-f Coaxial	Current	50
Multipin	Current	50
Cable	Current	50
All types	Voltage	See Table Below for Nonpressured Systems

Min Air Space	Voltage at Sea Level		
	Rated V (rms)	Working V	
		DC	AC (rms)
< 0.031	600	280	200
0.031	1000	490	350
0.045	1500	700	500
0.062	1800	840	600
0.076	2250	1050	750
	Voltage at 50,000 ft altitude		
< 0.031	225	100	75
0.031	375	190	125
0.045	525	210	175
0.062	675	315	225
0.076	790	360	360
	Voltage at 70,000 ft altitude		
< 0.031	150	70	50
0.031	300	125	90
0.045	375	175	125
0.062	450	210	150
0.076	500	230	165

4.1.3 Environmental Resistance

In order to realize fully the benefits of a reliability oriented design, consideration must be given early in the design process to the required environmental resistance of the equipment being designed. The environmental resistance, both intrinsic and that provided by specifically directed design features, will singularly determine the ability of the equipment to withstand the deleterious stresses imposed by the environment in which the equipment will be operated. The initial requirement for determining the required environmental resistance is the identification and detailed description of the environments in which the equipment must operate. The next step is then the determination of the performance of the components and materials that comprise the equipment when exposed to the degrading stresses of the environments so identified. When such performance is inadequate or marginal with regard to the equipment reliability goals, corrective measures such as derating, redundancy, protection from adverse environments, or selection of more resistant materials and components are necessary to fulfill the reliability requirements of the equipment.

4.1.3.1 Environmental Factors

Since reliability is strongly dependent upon the operating conditions that are encountered during the entire life of the equipment, it is important that such conditions are accurately identified at the beginning of the design process. Environmental factors which exert a strong influence on equipment reliability are listed in Table 4-33 and discussed on the following pages.

High temperatures impose a particularly severe stress on most electronic components since they can cause not only catastrophic failure such as melting of solder joints and burn out of solid state devices, but also slow progressive deterioration of component performance levels due primarily to chemical degradation effects. It is often stated that excessive temperature is the primary cause of poor reliability in military electronic equipment.

Table 4-33 ENVIRONMENTAL STRESSES, EFFECTS AND RELIABILITY IMPROVEMENT TECHNIQUES IN ELECTRONIC EQUIPMENT

Environmental Stress	Effects	Reliability Improvement Techniques
High Temperature	Parameters of resistance, inductance, capacitance, power factor, dielectric constant, etc. will vary; insulation may soften; moving parts may jam due to expansion; finishes may blister; devices suffer thermal aging; oxidation and other chemical reactions are enhanced; viscosity reduction and evaporation of lubricants are problems; structural overloads may occur due to physical expansions.	Heat dissipation devices, cooling systems, thermal insulation, heat-withstanding materials.
Low Temperature	Plastics and rubber lose flexibility and become brittle; electrical constants vary; ice formation occurs when moisture is present; lubricants gel and increase viscosity; high heat losses; finishes may crack; structures may be overloaded due to physical contraction.	Heating devices, thermal insulation, cold-withstanding materials.
Thermal Shock	Materials may be instantaneously overstressed causing cracks and mechanical failure; electrical properties may be permanently altered. Crazing, delamination, ruptured seals.	Combination of techniques for high and low temperatures.
Shock	Mechanical structures may be overloaded causing weakening or collapse; items may be ripped from their mounts; mechanical functions may be impaired.	Strengthened members, reduced inertia and moments, shock absorbing mounts.
Vibration	Mechanical strength may deteriorate due to fatigue or overstress; electrical signals may be mechanically and erroneously modulated; materials and structures may be cracked, displaced, or shaken loose from mounts; mechanical functions may be impaired; finishes may be scoured by other surfaces; wear may be increased.	Stiffening, control of resonance.

Table 4-33 ENVIRONMENTAL STRESSES, EFFECTS AND RELIABILITY IMPROVEMENT TECHNIQUES IN ELECTRONIC EQUIPMENT (Continued)

Environmental Stress	Effects	Reliability Improvement Techniques
Humidity	Penetrates porous substances and causes leakage paths between electrical conductors; causes oxidation which leads to corrosion; moisture causes swelling in materials such as gaskets; excessive loss of humidity causes embrittlement and granulation.	Hermetic sealing, moisture-resistant material, dehumidifiers, protective coatings.
Salt Atmosphere and Spray	Salt combined with water is a good conductor which can lower insulation resistance; causes galvanic corrosion of metals; chemical corrosion of metals is accelerated.	Nonmetal protective covers, reduced use of dissimilar metals in contact, hermetic sealing, dehumidifiers.
Electromagnetic Radiation	Causes spurious and erroneous signals from electrical and electronic equipment and components; may cause complete disruption of normal electrical and electronic equipment such as communication and measuring systems.	Shielding, material selection, part type selection.
Nuclear/Cosmic Radiation	Causes heating and thermal aging; can alter chemical, physical and electrical properties of materials; can produce gases and secondary radiation; can cause oxidation and discoloration of surfaces; damages electrical and electronic components especially semiconductors.	Shielding, component selection, nuclear hardening.
Sand and Dust	Finely finished surfaces are scratched and abraded; friction between surfaces may be increased; lubricants can be contaminated; clogging of orifices, etc.; materials may be worn, cracked, or chipped; abrasion, contaminates insulations, corona paths.	Air-filtering, hermetic sealing.
Low Pressure (High Altitude)	Structures such as containers, tanks, etc. are overstressed and can be exploded or fractured; seals may leak; air bubbles in materials may explode causing damage; internal heating may increase due to lack of cooling medium; insulations may suffer arcing and breakdown; ozone may be formed; outgasing is more likely.	Increased mechanical strength of containers, pressurization, alternate liquids (low volatility), improved insulation, improved heat transfer methods.

In present day electronic systems design, great emphasis is placed on small size and high component part densities. This generally requires a cooling system to provide a path of low thermal resistance from heat-producing elements to an ultimate heat sink of reasonably low temperature.

Solid state components are generally rated in terms of maximum junction temperatures, and the thermal resistances from this point to either the case or to free air are usually specified. The specification of maximum ambient temperature for which a component is suitable is generally not a sufficient method for component selection with densely packaged parts since the surface temperatures of a particular component can be greatly influenced by heat radiation or heat conduction effects from other nearby parts. These effects can lead to overheating above specific maximum safe temperatures even though the ambient temperature rating appears not to be exceeded. It is preferable, therefore, to specify thermal environment ratings such as equipment surface temperatures, thermal resistance paths associated with conduction, convection and radiation effects, and cooling provisions such as air temperature, pressure and velocity. In this manner, the true thermal state of the temperature-sensitive internal elements can be determined.

Low temperatures experienced by electronic equipment can also cause reliability problems. These problems are usually associated with mechanical elements of the system and include mechanical stresses produced by differences in the coefficients of expansion (contraction) of metallic and nonmetallic materials, embrittlement of nonmetallic components, mechanical forces caused by freezing of entrapped moisture, stiffening of liquid constituents, etc. Typical examples include cracking of seams, binding of mechanical linkages, and excessive viscosity of lubricants.

Additional stresses are produced when electronic equipment is exposed to sudden changes of temperature or rapidly changing temperature cycling conditions. These conditions generate large internal mechanical stresses in structural elements particularly when dissimilar materials are involved. Effects of the thermal shock induced stresses include cracking of seams, delamination, loss of hermeticity, leakage of fill gases, separation of encapsulating components from components and enclosure surface leading to the creation of voids, and distortion of support members.

A thermal shock test is generally specified to determine the integrity of solder joints since such a test creates large internal forces due to differential expansion effects. Such a test has also been found to be instrumental in creating segregation effects in solder alloys leading to the formulation of lead-rich zones which are susceptible to cracking effects.

Electronic equipment is often subjected to environmental shock and vibration both during normal use and testing. Such environments can cause physical damage to components and structural members when deflections produced cause mechanical stresses which exceed the allowable working stress of the constituent parts.

The natural frequencies of subsystems comprising the equipment are important parameters which must be considered in the design process since a resonant condition can be produced if a natural frequency is within the vibration frequency range. The resonance condition will greatly amplify the deflection of the subsystem and may increase stresses beyond the safe limit.

The vibration environment can be particularly severe for electrical connectors since it may cause relative motion between members of the connector. This motion in combination with other environment stresses can produce fret corrosion which generates wear debris and causes large variations in contact resistance.

Humidity and salt air environments can cause degradation of equipment performance since they promote corrosion effects in metallic components and can foster the creation of galvanic cells particularly when dissimilar metals are in contact. Another deleterious effect of humidity and salt air atmospheres is the formation of surface films on nonmetallic parts which cause leakage paths and degrade the insulation and dielectric properties of these materials. Absorption of moisture by insulating materials can also cause a significant increase in volume conductivity and dissipation factor of materials so affected.

Electromagnetic and nuclear radiation can cause disruption of performance levels and, in some cases, permanent damage to exposed equipment. It is important, therefore, that such effects be considered in

determining the required environmental resistance for electronic equipment that must achieve a specified reliability goal.

Electromagnetic radiation often produces interference and noise effects within electronic circuitry which can impair the functional performance of the system. Sources of these effects include corona discharges, lightning discharges, sparking and arcing phenomena. These may be associated with high voltage transmission lines, ignition systems, brush-type motors, and even the equipment itself. Generally, the reduction of interference effects requires incorporation of filtering and shielding features or the specification of less susceptible components and circuitry.

Nuclear radiation can cause permanent damage by alteration of the atomic or molecular structure of dielectric and semiconductor materials. High energy radiation can also cause ionization effects which degrade the insulation levels of dielectric materials. The mitigation of nuclear radiation effects typically involves the use of materials and components possessing a higher degree of intrinsic radiation resistance and the incorporation of shielding and hardening techniques.

In addition to the aforementioned stress factors, other environmental factors may require consideration in the design process to assure that adequate environmental resistance is incorporated into the equipment design. These additional factors include:

- Sand and dust
- Fungus
- Acoustic noise
- Electric fields
- Magnetic fields
- Presence of reactive liquids and gases

Each of these stress factors, if present, requires determination of its impact on the operational and reliability characteristics of the materials and components comprising the equipment being designed, and the identification of material, component and packaging techniques that afford the necessary protection against such degrading factors.

In the environmental stress identification process that precedes the selection of environmental resistance techniques, it is essential that stresses associated with all life intervals of the equipment be considered. This includes not only the operational and maintenance environments but also the preoperational environments when stresses imposed on the parts during manufacturing assembly, inspection, testing, shipping and installation may have significant impact on the eventual reliability of the equipment. Stresses imposed during the preoperational phase are often overlooked, but they may represent a particularly harsh environment which the equipment must withstand. Often the shock and humidity environments to which commercial and military systems are exposed during shipping and installation are more severe than those it will encounter under normal operating conditions. It is also probable that some of the environmental resistance features that are contained in a system design pertain to conditions that are encountered in the preoperational phase, and not in conditions that the equipment experiences after being put into operation.

4.1.3.2 Environmental Resistance Provisions

After identification of all environmental stress factors that will be encountered by a particular electronic system, a determination is made of components and elements of the system which will be adversely affected and the effects of this degradation on the apportioned reliability goals. Generally, such a determination will not only identify elements of the proposed design that are totally unsuitable, but equally important, will identify trade-off situations where incorporation of specific protective features will significantly enhance the achievable reliability.

In these cases, the solution is the specification of components having greater inherent resistance to the identified environmental stresses and the selection of particular protection techniques for reducing these stresses to levels that produce more favorable reliability characteristics.

Thermal Protection

Since excessive temperature is a primary cause of operational and reliability degradation, each proposed system design must be evaluated to establish that its thermal performance is consistent with the required equipment reliability. The preferred method for evaluating the thermal performance of electronic equipment (with respect to reliability) is a parts stress analysis method (per Section 2.3.1) which determines the maximum safe temperatures for constituent parts. A reduction in the operating temperature of components is a primary method for achieving improved reliability levels. This is generally possible by provision of a thermal design which reduces heat input to minimally achievable levels and provides low thermal resistance paths from heat-producing elements to an ultimate heat sink of reasonably low temperature. The thermal design is often as important as the circuit design in obtaining the necessary performance and reliability characteristics of electronic equipment.

The failure rates of electronic system components vary significantly with temperature. Table 4-34 illustrates the reliability improvement potential that is associated with the operation of circuit elements at reduced temperatures. A consideration of life cycle costs will generally indicate that the cost of designing and implementing adequate thermal performance into equipment is fully recovered by savings in maintenance costs early in the operational life of the equipment. A suitable thermal design will also minimize temperature excursions of components when environmental temperatures or power dissipation vary, resulting in further reliability benefits.

The part stress analysis method for evaluating system thermal performance is based on a determination of the maximum allowable temperature for each component which is consistent with the equipment reliability and the failure rate allocated to that component. Once these maximum allowable temperatures are assigned and the power dissipated by each component is ascertained, a heat flow network can be established from each component to available heat sinks or coolants for analysis of the system thermal performance. In situations where surface temperatures must be related to maximum allowable internal temperatures, such as

Table 4-34 RELIABILITY IMPROVEMENT POTENTIAL AT REDUCED TEMPERATURES

Part Description	Base Failure Rates* (per 10^6 hrs)		Δt ^oC	Decrease in Failure Rate Due to Low T
	Reduced Temp-^oC	High Temp-^oC		
PNP Silicon Transistors	0.008 at 40^o	0.063 at 160^o	120	8:1
NPN Silicon Transistors	0.0054 at 40^o	0.033 at 160^o	120	6:1
Glass and Porcelain Capacitors	0.0009 at 40^o	0.029 at 125^o	85	32:1
Transformers and Coils	0.001 at 90^o	0.0267 at 85^o	45	27:1
Resistors, Comp. Carb.	0.0002 at 40^o	0.0063 at 90^o	50	31:1

*Taken from MIL-HDBK-217B at a 10% stress level.

junction temperatures of semiconductor devices, a knowledge of the internal thermal resistance of these components is required to calculate the corresponding surface temperatures for the particular operating conditions of the component.

A step by step procedure for evaluating thermal performance of proposed designs includes the following activities:

- Establish the maximum and minimum environmental temperatures of anticipated heat sinks and coolants.
- Characterize the available cooling techniques such as forced air convection, liquid or vaporization cooling.
- Develop a heat flow network using electrical analog techniques for the conditions of maximum allowable component temperatures and maximum environmental heat sink or coolant temperatures; determine the thermal resistance requirements from parts to heat sinks.

- Select packaging approaches and component placements that will fulfill the thermal resistance requirements in terms of the available and permissible cooling techniques.
- Determine the suitability of simple cooling techniques such as free or forced air cooling for satisfying the heat concentration and thermal resistance requirements of the proposed design. If insufficient, proceed to higher level cooling techniques until an optimum cooling method is identified.
- Evaluate the penalties associated with the selected cooling method and perform trade-off analyses to identify alternative approaches and refinements if possible.

Further specifics of the parts stress thermal anslysis and design techniques are described in Navelex Publication No. 0967-437-7010, July 1973, and other references described in this publication.

Although each proposed system design requires a thermal performance analysis based on its specific characteristics, there are a number of general rule-of-thumb approaches associated with specific components that are beneficial for obtaining suitable thermal performance. Guidelines to achieve reliable design through temperature reduction of specific components are itemized in Table 4-35.

Mechanical Protection

Protection against mechanical abuse environments is generally achievable by use of suitable packaging, mounting and structural techniques. The reliability impact of mechanical protection techniques is generally singular in that these measures do or do not afford the required protection against the identified mechanical abuse stresses. In most cases, trade-off situations between the level of protection and reliability improvements are not as pronounced as in the case of thermal protection. The one exception may be the case of fatigue damage where the level of protection would have a significant impact on reliability if in fact fatigue was a primary failure mechanism in the normal life of the equipment.

Table 4-35 DESIGN GUIDELINES TO REDUCE COMPONENT OVERHEATING

Semiconductor Devices

a) Minimize thermal contact resistance between device and its mounting by using large area, smooth contacting surfaces and specifying thermal gaskets or compounds as required.

b) Locate remote from high temperature parts.

c) Use heat sinks with fins positioned vertically and in direction of air or coolant flow. Use painted or coated surfaces to improve radiation characteristics.

Capacitors

a) Locate remote from heat sources.

b) Insulate thermally from other heat sources.

Resistors

a) Locate for favorable convection.

b) Provide mechanical clamping or encapsulating material for improved heat transfer to heat sinks.

c) Use short leads whenever possible.

Transformers and Inductors

a) Provide heat conduction paths for transfer of heat from these devices.

b) Locate favorably for convection cooling.

c) Provide cooling fins where appropriate.

Printed Wiring Boards

a) Specify larger area conductors where practicable.

b) Segregate heat producing elements from heat sensitive components.

c) Use intermediate metal core layers in multi-layer systems and provide good conduction paths from these layers to support members and intermediate heat sinks.

d) Use protective coatings and encapsulants for improving heat transfer to lower temperature supports and heat sinks.

Shock and Vibration Protection

The environmental resistance required to protect against specified shock and vibration stresses is generally determined by an analysis which evaluates the deflections and mechanical stresses produced by these environmental factors. This generally involves the determination of natural frequencies and evaluation of the mechanical stresses within components and materials produced by the shock and vibration environment. If the mechanical stresses so produced are below the allowable safe working stress of the materials involved, no direct protection methods are required. If, on the other hand, the stresses exceed the safe levels, corrective measures such as stiffening, reduction of inertia and bending moment effects, and incorporation of further support members are indicated. If such approaches do not reduce the stresses below the safe levels, further reduction is usually possible by the use of shock absorbing mounts.

Humidity, Salt Air, Sand and Dust Protection

It is often mandatory to provide protection of the system elements against dust, dirt, contamination, humidity, salt spray and other mechanical abuse environments of this type. Although trade-off situations generally do not exist in terms of potential reliability improvements, this protection does significantly impact the operational and reliability levels of the equipment.

Possible protection methods against this class of environmental stresses include hermetic sealing, desiccants, and protective coatings. Hermetic sealing is often required when components such as solid state devices must be operated in a controlled atmosphere. The technical considerations involved in the selection of the hermetic seal system are its effects on the thermal performance of the system and its resistance to cracking during thermal shock conditions.

There are many insulating compounds that can be applied as coatings on electronic component assemblies. Among these are epoxies, silicones, polyurethanes, polystyrenes and varnishes. Generally, these are selected in accordance with MIL-I-46058 for military applications. Technical considerations for selection of suitable protective coatings are insulation

resistance under the expected humidity and temperature conditions, dissipation factor, dielectric constant, mechanical flexibility, resistance to cracking during thermal shock, removal ease for repair work, ease of application, and its ability to prevent the migration of corrosion products.

Radiation Protection

Radiation protection generally must be specifically designed for the noise and interference fields against which protection is required. This usually involves the specification of shielding and filtering that are effective in the frequency range of concern.

Nuclear radiation protection generally consists of the use of specific components having an intrinsic hardness and the incorporation of shielding features that impact the required level of hardness to the system. Again, the provision of nuclear protection schemes is usually a go/no-go proposition since few trade-off situations are apparent.

4.1.3.3 General Packaging Considerations

The selection of a suitable packaging method for electronic equipment requires consideration of many trade-off factors in addition to the environmental protection factors described above. Characteristics that influence the choice of a packaging method include cost, size, producibility, maintainability, repairability and reliability. In many cases, the system requirements are conflicting, and the selection process becomes one of identifying a packaging approach offering the best compromise of the many divergent requirements.

In military electronic systems, size, weight and reliability are prime considerations, and the choice of packaging methods must reflect the priority of these factors. System packaging approaches are generally concentrated on microelectronic packaging systems because of the size reduction and reliability benefits associated with semiconductor integrated circuit devices. Semiconductor integrated circuits not only offer reliability improvements because of their inherent properties but also because of the reduced number of interconnections that are needed. Further improvements result from the highly controlled fabrication processes and techniques utilized in the manufacture of such devices.

Table 4-36 illustrates a general ranking of trade-offs associated with electronic packaging techniques. For particular systems, these ranking factors will vary depending upon the specific requirements of the system. However, the general order of ranking is believed to be appropriate for a large population of systems, although large variations will occur.

Table 4-36 PACKAGING TRADE-OFFS

Type of Packaging	Characteristics					
	Size	Cost	Throw Away Cost	Relia-bility	Main-tenance Repair	Logistics/ Spares
Soldered Modules on Boards	P	F	G	P	F	F
Welded Modules on Boards	P	P	F	P	F	F
Hybrid Modules (with integrated circuits)	F	P	F	F	F	F
Hybrid Compartmentalized	F	P	F	F	F	F
Etched Circuits	F	P	F	F	F	F
Pluggable Flat-Pack Modules	F	F	G	P	G	F
Flat-Pack Integrated Circuits Printed Wiring Board	G	G	G	F	G	G
Welded Flat-Pack IC Stack	G	P	P	F	P	F
Thin-Film Circuits	G	G	F	F	P	F
IC Chips	G	G	P	G	P	P
Large-Scale Integration (LSI)	G	G	P	G	P	P
MOS Devices	G	G	P	G	P	P

G = Good
F = Fair
P = Poor

4.1.4 Redundancy

The reliability of a system can be significantly enhanced through the use of redundancy. Redundancy involves designing one or more alternate signal paths into the system through addition of parallel elements.

Redundancy has been extensively applied in airborne systems. For example, the electronic multiplexing system for the B-1 bomber[27] currently uses a redundant design. In this system, redundant computers control the main switching buses. Normally, one of the two computers is active and feeds the two main buses which control all switching functions while the other continuously performs the same function and compares its output with the active computer. If the active computer malfunctions, the standby automatically takes over.

Another example of a redundant configuration is provided by the AWG-9 weapon control system as used aboard the Grumman F-14 fighter[28]. In this system, two major sensors are used to achieve the same goal.

- Pulse Doppler search, track, acquisition and guidance radar
- Gimbal-mounted infrared search/acquisition sensor.

The infrared system provides a backup to the radar if the latter is inoperable due to malfunctions or jamming. Additionally, it may operate in a dual mode to augment the radar search volume.

This subsection of the handbook presents data and guidelines for the application and evaluation of redundancy. The categorization of techniques, their advantages and disadvantages and specific design examples are included. This treatment of redundancy is not meant to be exhaustive, but to point out concepts of redundancy important to electronic equipment design applications and to caution the designer that applications of redundancy are not without drawbacks. For a more detailed discussion of redundancy, the reader is referred to the reference sources.

4.1.4.1 General Concepts

As indicated in Section 2.1.2, safety and mission reliability can be increased through redundancy at the cost of decreasing unscheduled maintenance (or serial) reliability. Note, however, that the unscheduled maintenance reliability reduction accompanying redundancy may be offset

by also improving reliability through use of component improvement techniques--such as part screening, derating and design simplification--as discussed elsewhere in this guide.

Depending on the specific applications, a number of approaches are available to improve reliability through redundant design. These design approaches can be classified on the basis of how the redundant elements are introduced into the circuit to provide a parallel signal path. In general, there are two (2) major classes of redundancy:

(1) Active redundancy--External components are not required to perform the function of detection, decision and switching when an element or path in the structure fails.

(2) Standby redundancy--External elements are required to detect, make a decision and switch to another element or path as a replacement for a failed element or path.

Techniques related to each of these two classes are depicted in the simplified tree-structure shown in Figure 4-31.

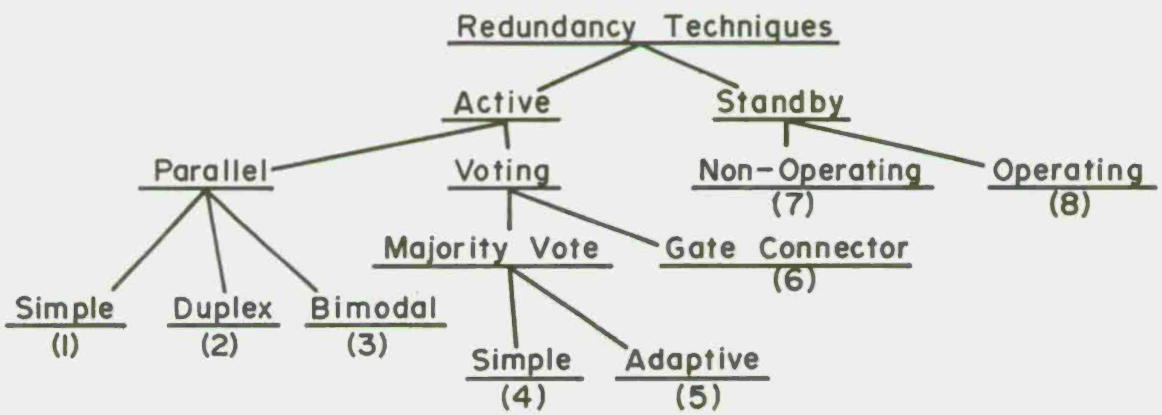


Fig. 4-31 REDUNDANCY TECHNIQUES

Table 4-37 further defines each of the eight techniques shown in Figure 4-31.

Although not readily apparent, redundancy does not lend itself to categorization exclusively by element complexity. Although certain of the configurations described in Table 4-37 are more applicable at the

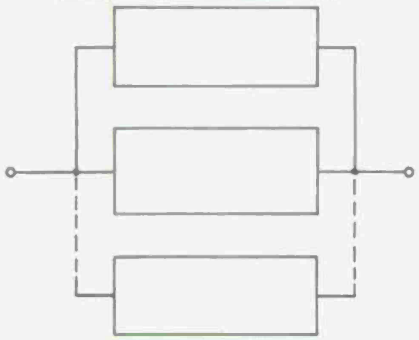
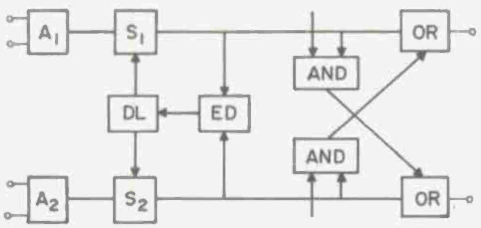
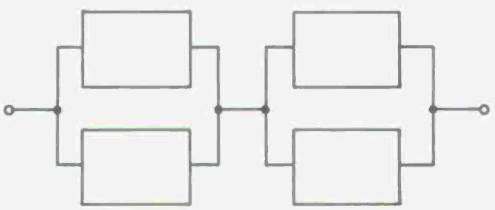
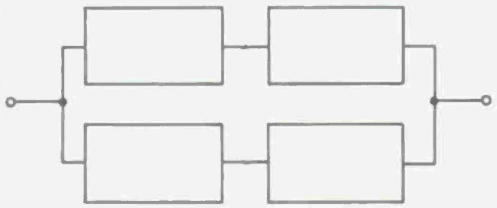
Simple Parallel Redundancy 	In its simplest form, redundancy consists of a simple parallel combination of elements. If any element fails open, identical paths exist through parallel redundant elements.
Duplex Redundancy 	This technique is applied to redundant logic sections, such as A1 and A2 operating in parallel. It is primarily used in computer applications where A1 and A2 can be used in duplex or active redundant modes or as a separate element. An error detector at the output of each logic section detects noncoincident outputs and starts a diagnostic routine to determine and disable the faulty element.
(a) Bimodal Parallel/ Series Redundancy 	A series connection of parallel redundant elements provides protection against shorts and opens. Direct short across the network due to a single element shorting is prevented by a redundant element in series. An open across the network is prevented by the parallel element. Network (a) is useful when the primary element failure mode is open. Network (b) is useful when the primary element failure mode is short.
(b) Bimodal Series/ Parallel Redundancy 	

TABLE 4-37 REDUNDANCY TECHNIQUES

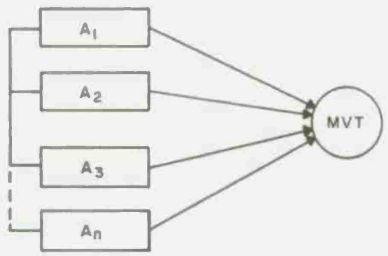
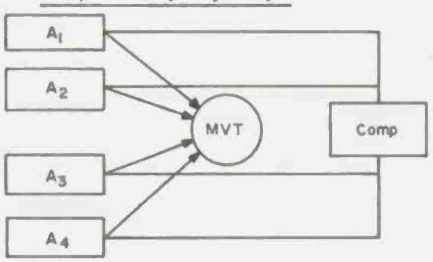
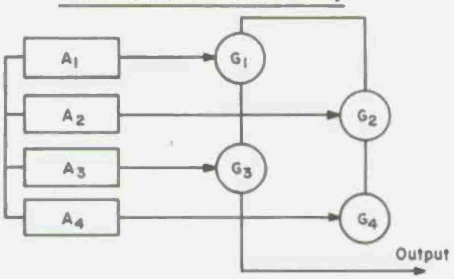
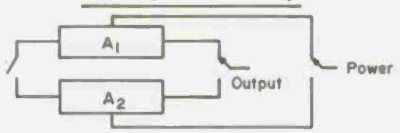
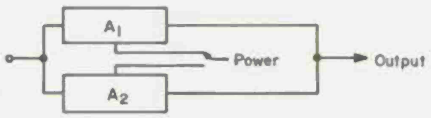
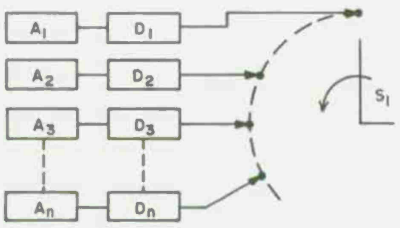
Majority Voting Redundancy 	Decision can be built into the basic parallel redundant model by inputting signals from parallel elements into a voter to compare each signal with remaining signals. Valid decisions are made only if the number of useful elements exceeds the failed elements.
Adaptive Majority Logic 	This technique exemplifies the majority logic configuration discussed previously with a comparator and switching network to switch out or inhibit failed redundant elements.
Gate Connector Redundancy 	Similar to majority voting. Redundant elements are generally binary circuits. Outputs of the binary elements are fed to switch-like gates which perform the voting function. The gates contain no components whose failure would cause the redundant circuit to fail. Any failures in the gate connector act as though the binary element were at fault.
Standby Redundancy  	A particular redundant element of a parallel configuration can be switched into an active circuit by connecting outputs of each element to switch poles. Two switching configurations are possible. 1) The element may be isolated by the switch until switching is completed and power applied to the element in the switching operation. 2) All redundant elements are continuously connected to the circuit and a single redundant element activated by switching power to it.
Operating Redundancy 	In this application, all redundant units operate simultaneously. A sensor on each unit detects failures. When a unit fails, a switch at the output transfers to the next unit and remains there until failure.

TABLE 4-37 REDUNDANCY TECHNIQUES (Cont.)

part or circuit level as opposed to the equipment level, this is not due to inherent limitations of the particular configuration but rather to supporting factors such as cost, weight and complexity.

In addition to the two major classes and related techniques, another form of redundancy can exist within normal nonredundant design configurations. Parallel paths within a network often are capable of carrying an added load when elements fail. This can result in a degraded but tolerable output. In other words, an element failure in a parallel path does not always cause complete equipment failure but, instead, degrades equipment performance. The allowable degree of degradation depends on the number of alternate paths available. Where a mission can still be accomplished using an equipment whose output is degraded, the definition of failure can be relaxed to accommodate degradation. Naturally, limiting values of degradation must be built into the new definition of failure. This slow approach to failure, having been termed "graceful degradation", is exemplified by an array of elements configured into an antenna or an array of detectors configured into a receiver. In either case, individual elements may fail, reducing resolution, but if a minimum number operate, resolution remains great enough to identify a target.

The decision to use redundant design techniques must be based on a careful analysis of the trade-offs involved. Redundancy may prove the only available method when other techniques of improving reliability have been exhausted or when methods of part improvement are shown to be more costly than duplications. Its use may offer an advantage when preventive maintenance is planned. The existence of a redundant equipment can allow for repair with no system downtime. Occasionally, situations exist in which equipments cannot be maintained (e.g., spacecraft). In such cases, redundant elements may prolong operating time significantly.

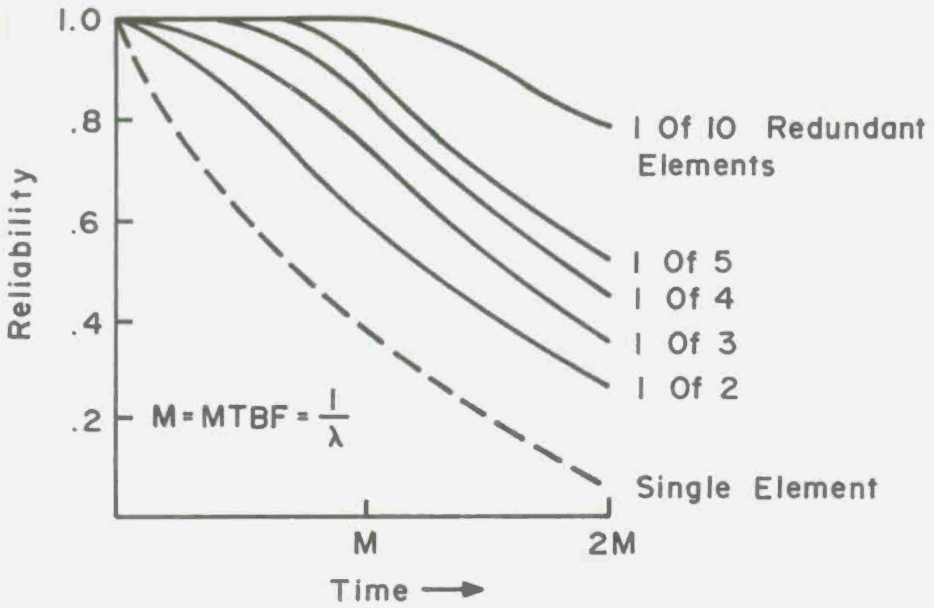
But the application of redundancy is not without penalties. It will increase weight, space, complexity, cost and time to design. As previously described, the increase in complexity results in a decrease of unscheduled maintenance reliability--safety and mission reliability is gained at the expense of serial mean-time-between-failure (MTBF).

In general, the reliability gain for additional redundant elements decreases rapidly for additions beyond a few parallel elements. As illustrated by Figure 4-32 for simple parallel redundancy, there is a diminishing gain in reliability and MTBF as the number of redundant elements is increased. As shown for the simple parallel case, the greatest gain achieved through addition of the first redundant element is equivalent to a 50% increase in the system MTBF. In addition to maintenance cost increases due to repair of the additional elements, reliability of certain redundant configurations may actually be less. This is due to the serial reliability of switching or other peripheral devices needed to implement the particular redundancy configuration (see Table 4-37).

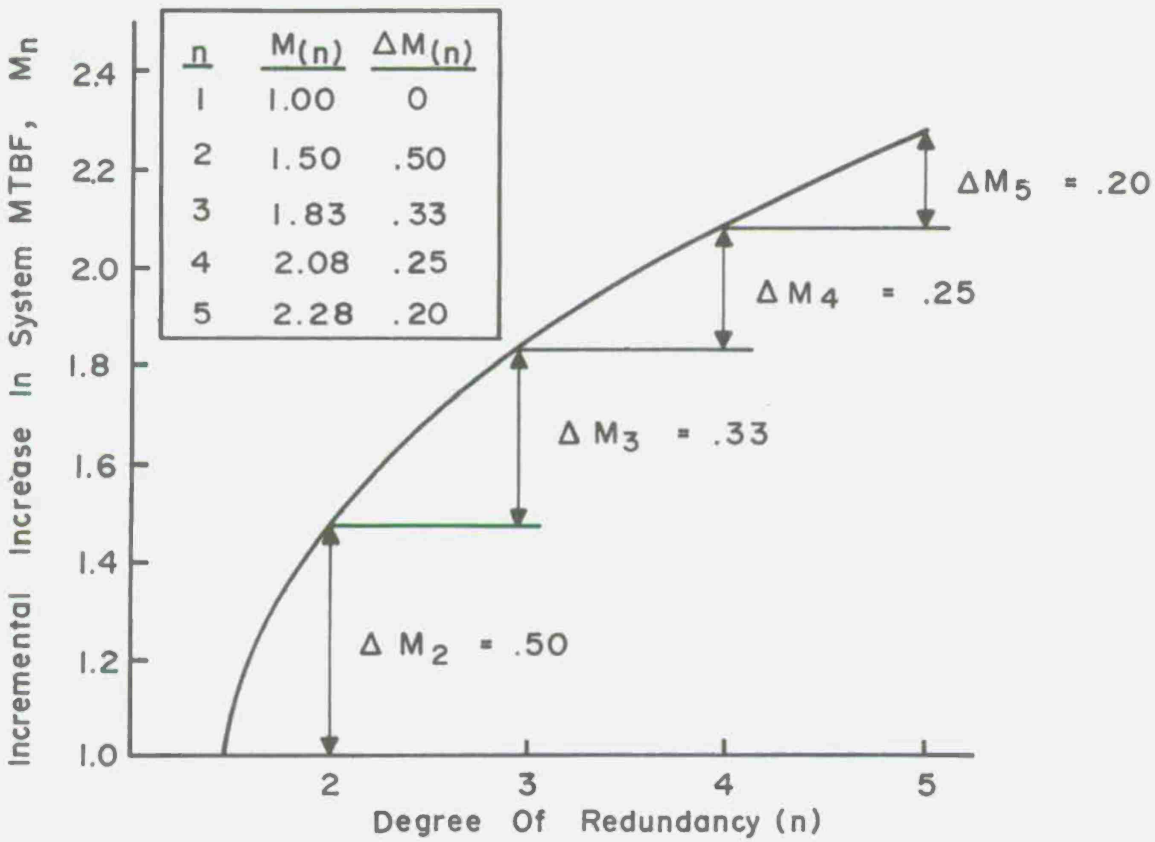
The effectiveness of certain redundancy techniques (especially standby) can be enhanced by repair. Standby redundancy allows repair of the failed unit (while operation of the good unit continues uninterrupted) by virtue of the switching function built into the standby redundant configuration. The switchover function can readily provide an indication that failure has occurred and operation is continuing on the alternate channel. With a positive failure indication, delays in repair are minimized. A further advantage of switching is related to built-in test (BIT) objectives. Built-in test can be readily incorporated into a sensing and switchover network for ease of maintenance purposes.

An illustration of the enhancement of redundancy with repair is shown in Figure 4-33. The achievement of increased reliability brought about by incorporation of redundancy is dependent on effective isolation of redundant elements. Isolation is necessary to prevent failure effects from adversely affecting other parts of the redundant network. The susceptibility of a particular redundant design to failure propagation may be assessed by application of failure mode effects analysis as discussed in Section 2.3.2. The particular techniques addressed there offer an effective method of identifying likely fault propagation paths.

Interdependency is most successfully achieved through standby redundancy, as represented by configurations classified as decision with switching, where the redundant element is disconnected until a failure is sensed. Design based on such techniques must provide protection



(a) Simple Active Redundancy For One Of n Element Required



(b) Incremental Increase In System MTBF For n Active Elements

Fig. 4-32 DECREASING GAIN IN RELIABILITY AS NUMBER OF ACTIVE ELEMENTS INCREASES

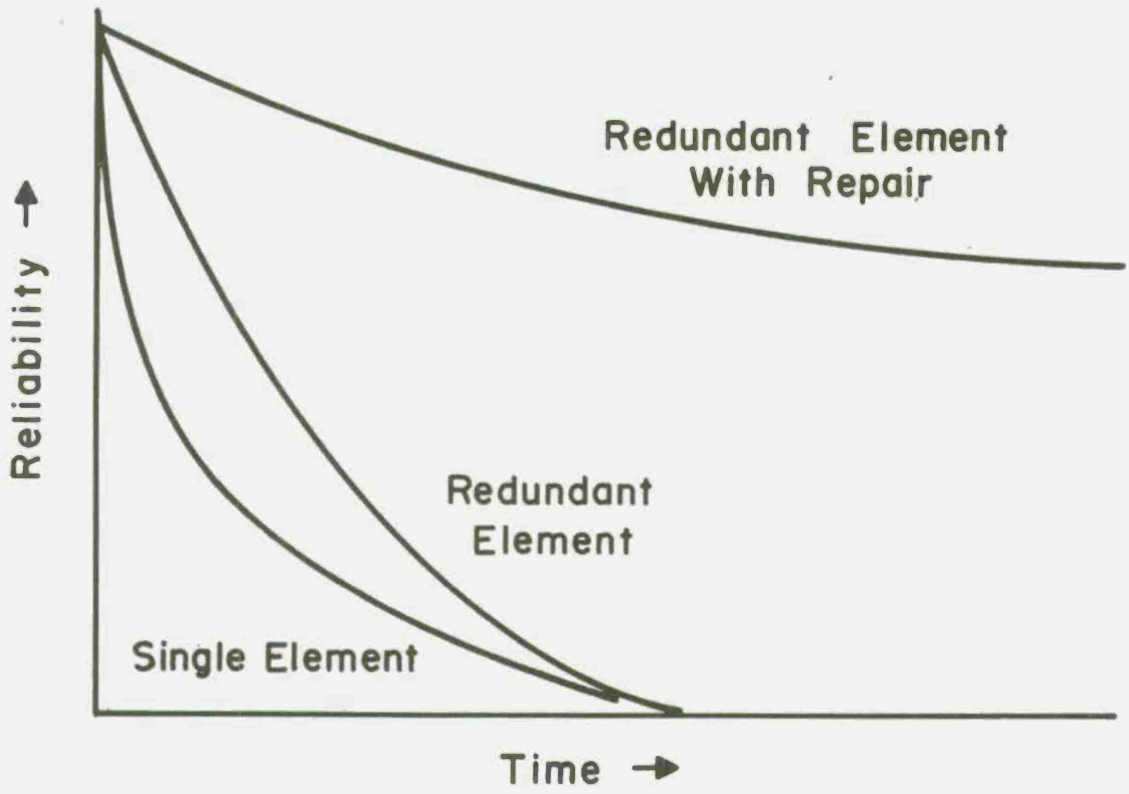


Fig.4-33 RELIABILITY GAIN FOR REPAIR OF SIMPLY PARALLEL REDUNDANT ELEMENT AT FAILURE

against switching transients and consider effects of switching interruptions on system performance.

Furthermore, care must be exercised to assure reliability gains from redundancy are not offset by increased failure rates due to switching devices, error detectors and other peripheral devices needed to implement the redundancy configurations.

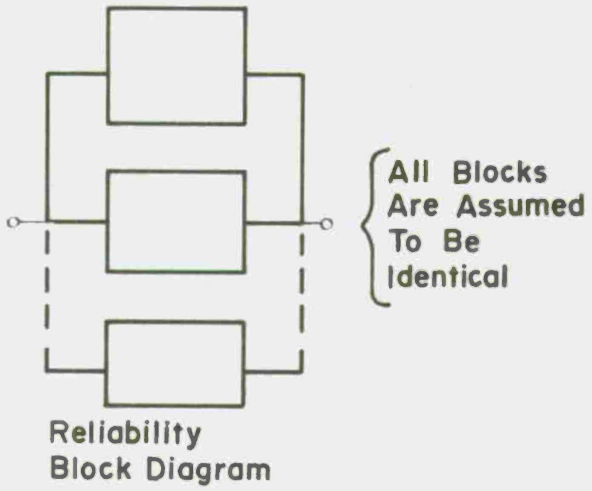
4.1.4.2 Redundancy Techniques

This section provides further information on the redundancy techniques itemized in Figure 4-31 and further described in Table 4-37. Figures 4-34 through 4-38 present block diagrams, mathematical models, a plot of the reliability function, applications, and advantages and disadvantages for those techniques defined in Table 4-37. As shown in Figure 4-31, active and standby redundancy are major categories or redundancy techniques. Several different techniques of parallel redundancy are given, since it is the most widely used type. Examples of voting and standby redundancy are also included. Due to the similarity between several of the techniques shown in Table 4-37, several are combined into one figure. In particular, gate connector redundancy and adaptive majority logic have been included as a modification of majority voting; standby redundancy has been considered to be a modification of operating redundancy as implemented by a different switching arrangement. More detailed information regarding models and applications of these specialized techniques is to be found in references 27, 28, 29, 30, 31 at the end of Section 4. Applications of these specific redundancy techniques to design examples may be found in Section 4.1.4.3.

4.1.4.3 Design Examples

This section presents examples of current applications of redundancy to avionics equipment. The particular examples discussed are listed below:

- Simple parallel redundant precision voltage supply
- Quad-redundant computer building block
- Majority voter redundant ÷ 8 counter
- Standby redundant channels in an RF receiver.



Reliability
Block Diagram

APPLICATION

Provides protection against irreversible hardware failures for continuously operating equipments.

MATHEMATICAL MODEL

$$R = 1-(1-e^{-\lambda t})n$$

SIMPLIFIED MODEL

$$R = 1-(\lambda t)^n$$

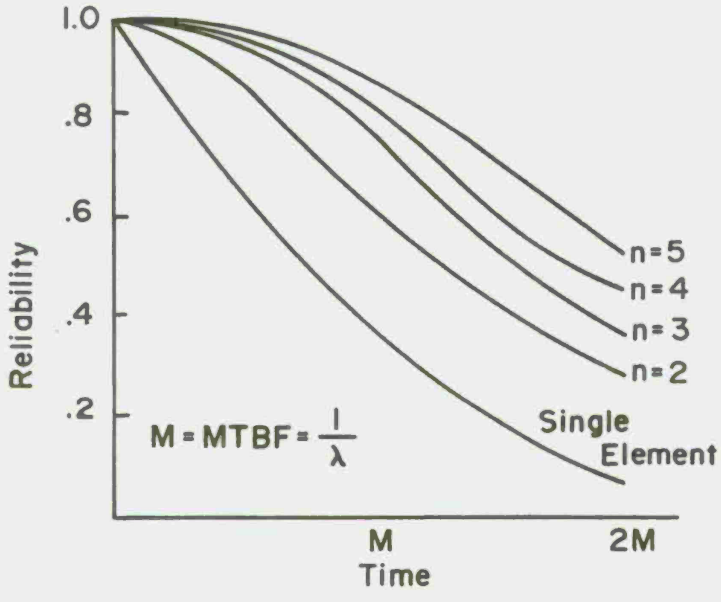
for small λt

where

n = number of parallel elements

λ = failure rate

R = reliability



RELIABILITY FUNCTION FOR SIMPLE PARALLEL RELIABILITY

ADVANTAGES

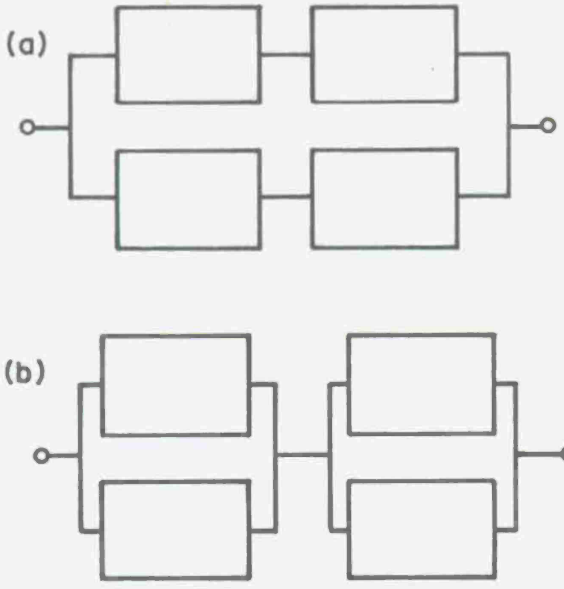
- Simplicity
- Significant gain in Reliability from nonredundant element
- Applicable to both analog and digital circuitry

DISADVANTAGES

- Load sharing must be considered
- Sensitive to voltage division across the elements
- Difficult to prevent failure propagation
- May present circuit design problems

Fig. 4-34 SIMPLE PARALLEL REDUNDANCY

Reliability Block Diagram



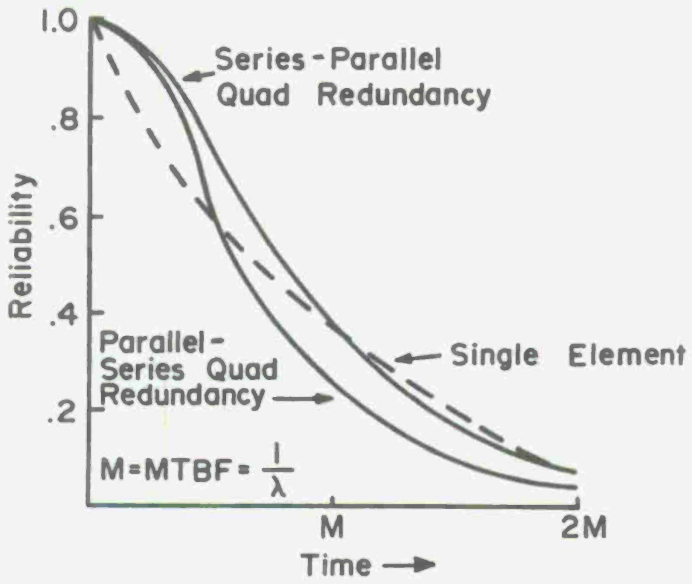
All Elements Shown In The Block Diagram Are Assumed Identical

APPLICATION

Applicable primarily at the part level where short and open protection is required.

a) Protects primarily against the short failure mode.

b) Protects primarily against the open failure mode.



RELIABILITY FUNCTION FOR BIMODAL CONFIGURATIONS

MATHEMATICAL MODEL

a) $R = 2e^{-2\lambda t} - e^{-4\lambda t}$

b) $R = 4e^{-2\lambda t} - 4e^{-3\lambda t} + e^{-4\lambda t}$

ADVANTAGES

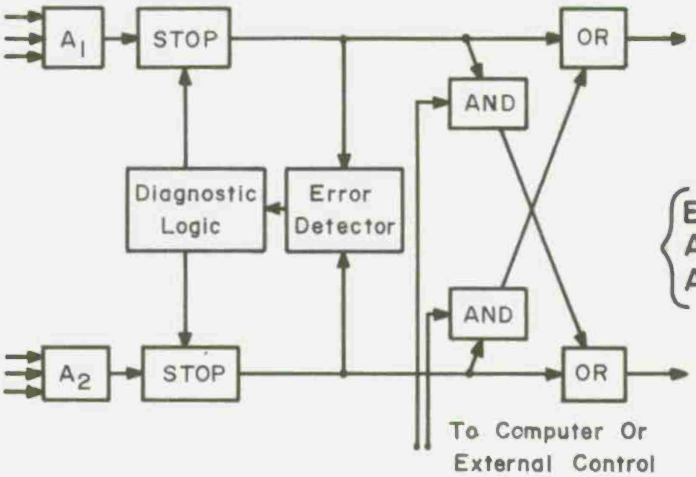
- Provides significant gain in reliability at the part or stage level for short mission times.

DISADVANTAGES

- Difficult to design.
- Restricted to part and/or stage applications.

Fig. 4-35 BIMODAL REDUNDANCY

Reliability Block Diagram



Elements A_1 & A_2 Are Identical

APPLICATION

This technique is applicable to digital computer circuits with the objective of preventing incorrect logic elements from upsetting other circuits.

MATHEMATICAL MODEL

$$R = P_{ED}P_{DL}((2P_AP_{SW}-(P_AP_{SW})^2 \cdot (2P_3-P_3^2)$$

where

$$P_3 = P_{GO1}+P_{GO2}P_{GA}-P_{GO1}P_{GO2}P_{GA}$$

where

P_{ED} = error detector reliability

P_{DL} = diagnostic logic reliability

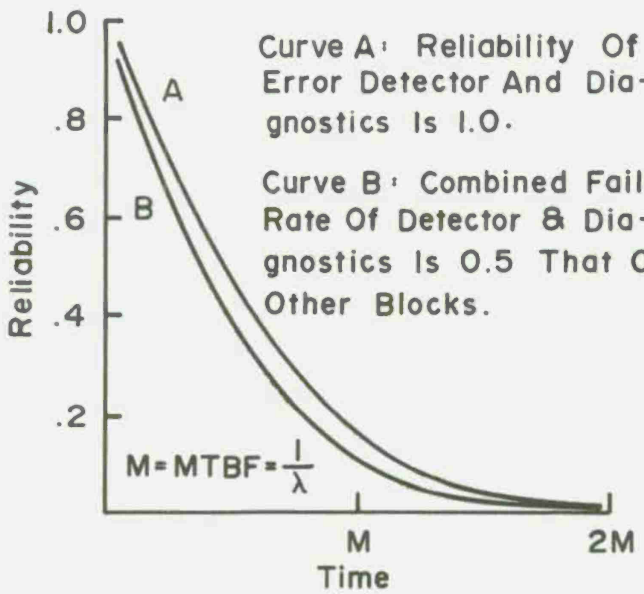
P_A = element reliability

P_{SW} = stop switch reliability

P_{GO1} = probability first input to OR gate gets through

P_{GO2} = probability second input to OR gate gets through

P_{GA} = reliability of AND gate



Curve A: Reliability Of Error Detector And Diagnostics Is 1.0.

Curve B: Combined Failure Rate Of Detector & Diagnostics Is 0.5 That Of Other Blocks.

RELIABILITY FUNCTION FOR DUPLEX REDUNDANCY

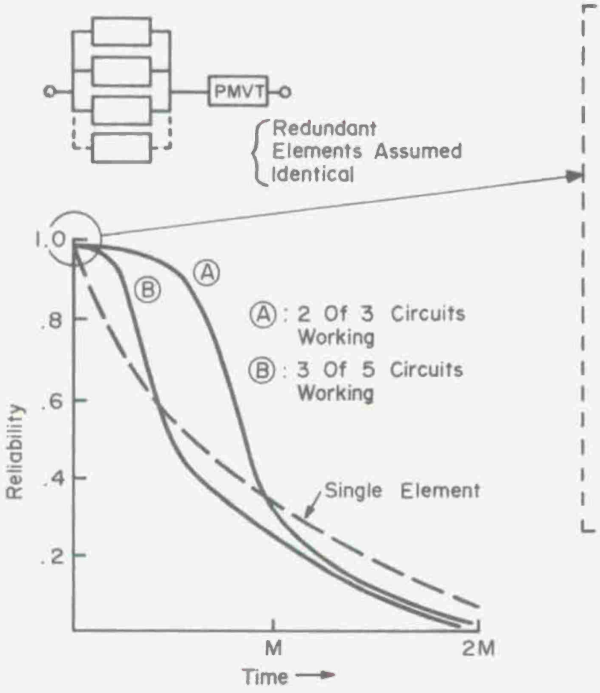
ADVANTAGES

- Applicable to duplex, active redundant modes or separate elements
- Maintains function for n-1 failures
- Protects against open and short failure modes and errors
- Faulty units can be repaired without disrupting the computer

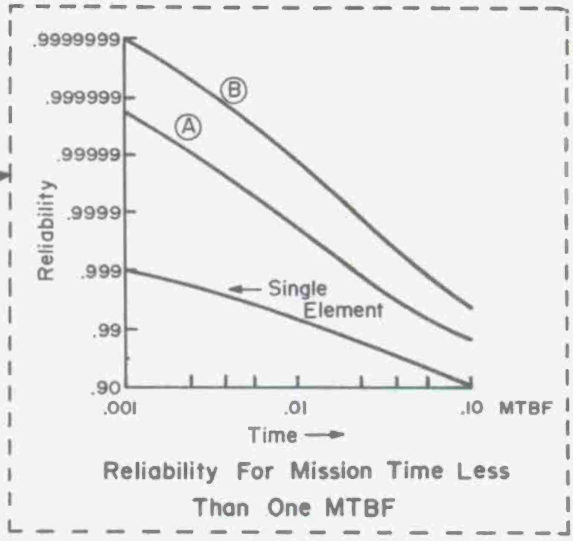
DISADVANTAGES

- May require diagnostic program
- Increased complexity due to sensing and switching
- Storage capacity requirements may increase due to redundant data requirements

Fig. 4-36 DUPLEX REDUNDANCY



Reliability Function For Majority Voting Redundancy



Reliability For Mission Time Less Than One MTBF

APPLICATION

Generally used with logic circuitry for either continuous or intermittent operation. This technique with minor modification, may be put in the form of adaptive majority logic or gate connector redundancy.

ADVANTAGES

- Can be implemented to provide indication of defective elements
- Can provide a significant gain in reliability for short mission times (less than one MTBF)

DISADVANTAGES

- Requires voter reliability significantly better than element reliability
- Lower reliability for long mission time (greater than one MTBF)

MATHEMATICAL MODEL

$$R = \left[\sum_{i=0}^{n} \binom{2n+1}{i} (1-e^{-\lambda t}) \cdot e^{-\lambda t(2n+1-i)} \right] e^{-\lambda_m t}$$

SIMPLIFIED MODEL

$$R = e^{\lambda_m t} - \binom{2n+1}{n+1} (\lambda t)^{n+1}$$

for small λt

where

n = number of redundant elements minus minimum number of elements required

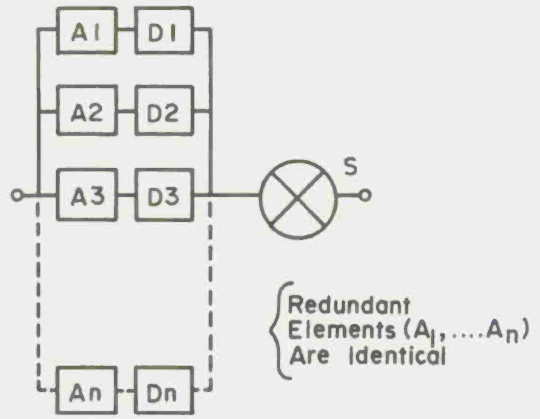
λ = failure rate

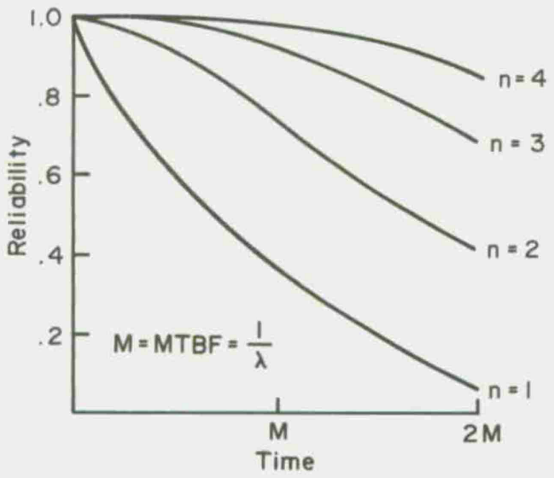
R = reliability

λ_m = failure rate of MVT

Fig. 4-37 MAJORITY VOTING REDUNDANCY

Reliability Block Diagram





RELIABILITY FUNCTION FOR OPERATING REDUNDANCY WITH UNIT SELECTION

APPLICATION

This configuration uses single mode redundancy with a sensor (Dn) on each unit possessing switching capability when a failure is detected. It is used when long starting time must be avoided and only single output can be tolerated. This technique may be reconfigured to a standby redundancy technique by altering the switching arrangement to activate the elements as they are switched into the circuit.

MATHEMATICAL MODEL

(Operating Redundancy)

$$R = e^{-\lambda t}\left[\sum_{r=0}^{n-1} \frac{(\lambda t)^r}{r!}\right]$$

Assuming error detector and switching reliability is 1.0.

where

n = number of parallel elements

λ = failure rate $(A_n + D_n)$

R = reliability

MATHEMATICAL MODEL

(Standby Redundancy)

$$R = e^{-\lambda t}\left[1 + \frac{\lambda}{\lambda_s}(1 - e^{-\lambda_s t})\right]$$

where

λ = element failure rate

λ_s = failure rate of switching function

R = reliability

ADVANTAGES

- Applicable to analog and digital circuitry
- Effective for intermittent failure modes

DISADVANTAGES

- Delay due to sensing and switching
- Redundancy gains are limited by failure modes of sensing and switching devices
- Increased complexity due to sensing and switching

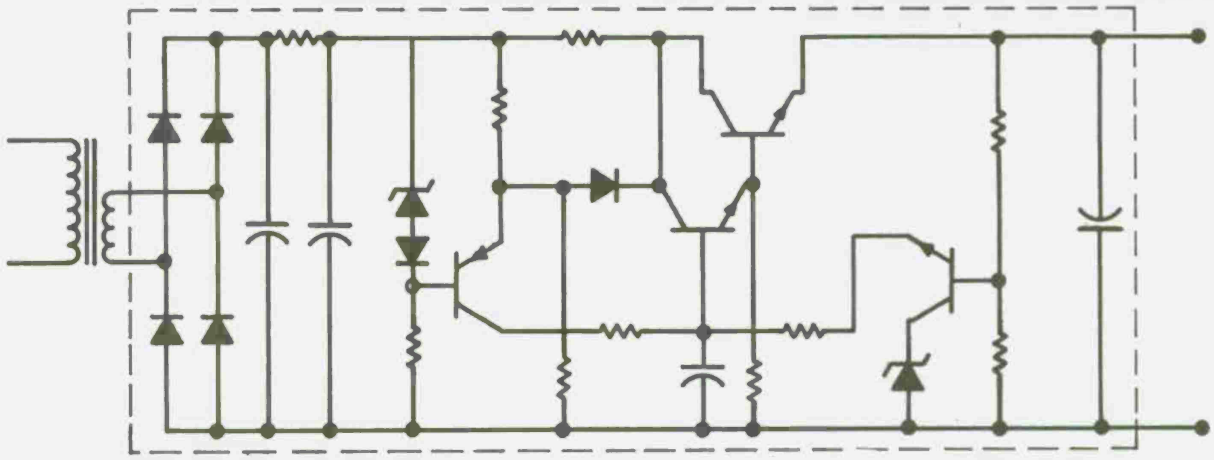
Fig. 4-38 STANDBY REDUNDANCY

In the following fourteen pages, a circuit diagram is given for each example and the specific reliability model is provides. A graphic comparison is provided for each example which illustrates the reliability for both redundant and nonredundant configurations.

EXAMPLE 1

SIMPLE PARALLEL REDUNDANCY

This example considers application of simple parallel redundancy at the circuit level centered around a precision regulated voltage supply. The circuit diagram for the basic nonredundant configuration plus part failure rates are shown in Figure 4-39.



Part	n	Failure Rate $\lambda(\times 10^{-6})$	$n\lambda$
Resistor, carbon composition	10	0.002	0.020
Capacitor, solid tantalum	4	0.038	0.152
Transformer, power	1	0.056	0.056
Transistor, silicon PNP	1	1.6	1.600
Transistor, silicon NPN	3	0.98	0.294
Diode, general purpose	6	0.68	0.408
Diode, zener	2	0.85	1.700
		Total	4.230

Figure 4-39 PRECISION REGULATED VOLTAGE SUPPLY

For the nonredundant circuit, the total failure rate is given by:

$$\lambda_{Total} = \Sigma \lambda_{parts} = 4.23 \times 10^{-6} \text{ failures/hour}$$

Using an operating time of 2000 hours, the reliability for the nonredundant configuration is:

$$R = e^{-\lambda_{total} t} = e^{-(4.23 \times 10^{-6})(2 \times 10^{3})}$$

$$R = 0.992$$

Figure 4-40 shows the configuration for the redundant supply. The basic circuit is shown within the dotted lines in Figure 4-39.

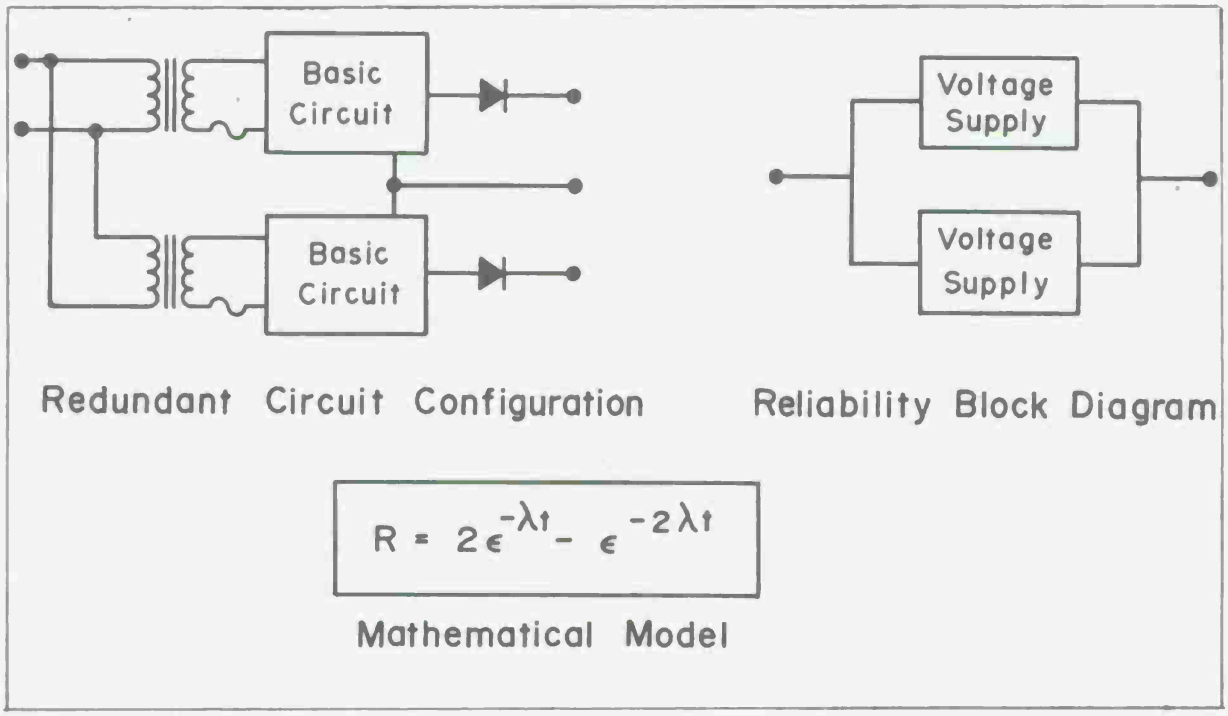


Fig. 4-40 REDUNDANT REGULATED VOLTAGE SUPPLY

Using the mathematical model given in Figure 4-40, the reliability of the redundant configuration is:

$$R = 1 - (1-e^{-\lambda t})^2$$

$$R = 0.99993$$

As indicated previously, the time period used is 2000 hours. A side-by-side comparison of reliability versus time for both configurations is given in Figure 4-41 for mission times above 2000 hours. Figure 4-41 uses an expanded time axis plus a log scale on the time axis to provide greater resolution between the two curves.

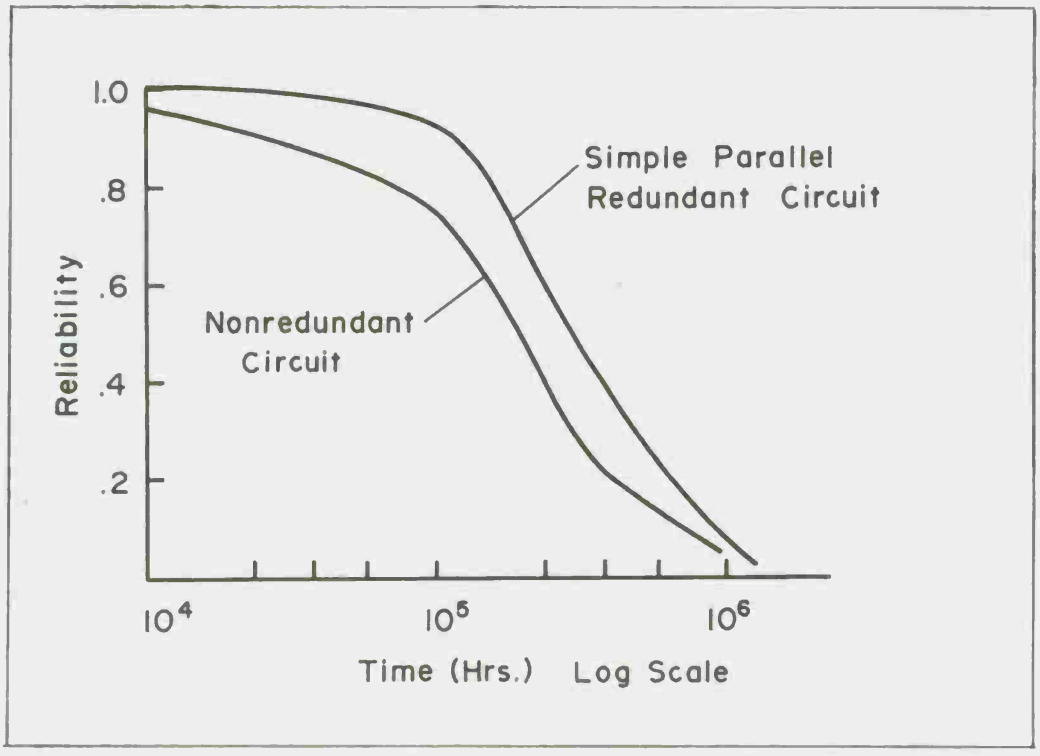
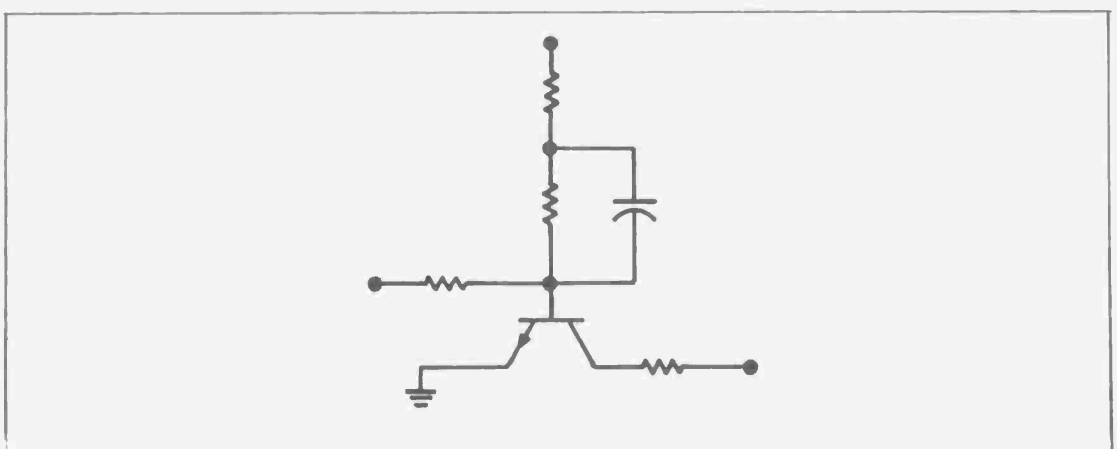


Fig. 4-41 RELIABILITY COMPARISON OF SIMPLE REDUNDANT AND NONREDUNDANT VOLTAGE SUPPLIES

EXAMPLE 2

BIMODAL REDUNDANCY--QUAD CONFIGURATION

This example examines redundancy at the part level. The example chosen depicts application of a quad-redundant configuration centered around a transistor and its associated biasing network. The advantage of the quad configuration is that, at the part level, it protects against both open and short failure modes. A circuit diagram and a list of failure rates is given in Figure 4-42 for the nonredundant circuit.



Part	n	Failure Rate $\lambda(\times 10^{-6})$	$n\lambda$
Resistor, carbon composition	4	0.002	0.008
Capacitor, ceramic	1	0.033	0.033
Transistor, NPN silicon	1	0.98	0.980
			1.021×10^{-6}

Figure 4-42 BASIC TRANSISTOR CIRCUIT

For the circuit shown in Figure 4-42, the total failure rate is:

$$\lambda_{Total} = \Sigma \lambda_{parts} = 1.021 \times 10^{-6} \text{ failures/hour}$$

Using an operating time of 2000 hours, the reliability of the circuit is:

$$R = e^{-\lambda_{total} t} = e^{-(1.021 \times 10^{-6})(2 \times 10^{3})}$$

$$R = 0.9980$$

This circuit finds wide application in computers and other digital equipment. If 25 such circuits were to be used within an equipment and all were required to operate successfully for 2000 hours, the reliability could be expressed by

$$R = (0.9980)^{25}$$

$$R = 0.9512$$

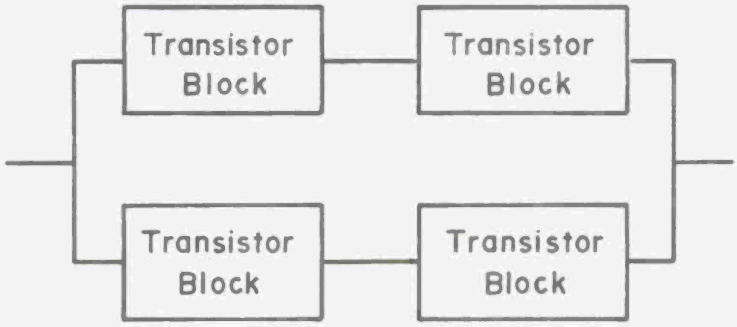
Figure 4-43 shows the circuit diagram for the redundant quad configuration. The reliability block diagram and mathematical model are also included. Since the quad-redundant circuit is used to protect against short and open failure modes, their probability of occurrence must appear in the mathematical model. However, for purposes of this example, both shorts and opens will be assumed equally likely to occur. Thus, the mathematical model used here (see Figure 4-43) is greatly simplified in contrast to a model which includes different modal probabilities.

Design of the quad circuit includes the selection of three parallel resistors in the collector circuit as shown in Figure 4-43. If it is assumed that the predominant failure mode of these resistors is open, the failure of any one resistor will have a minimal effect on the power supply voltage. For simplicity of calculation, the reliability of these three resistors has been considered as part of the basic configuration rather than separate parallel redundant elements.

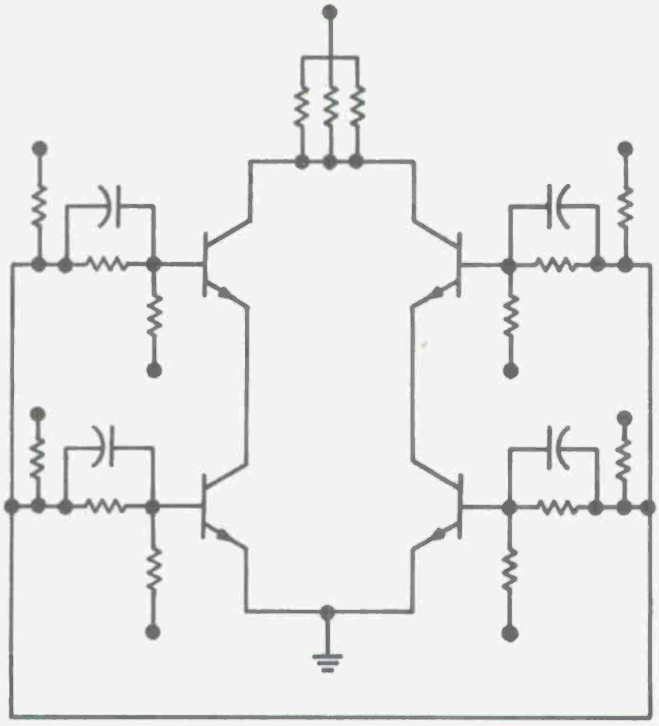
Using the mathematical model given in Figure 4-43, the reliability of the quad-redundant configuration is:

$$R = 2e^{-\lambda t} - e^{-4\lambda t}$$

$$R = 0.99998$$



Reliability Block Diagram



Quad Redundant Building Block

$$R = 2e^{-\lambda t} - e^{-4\lambda t}$$

Mathematical Model

Fig.4-43 QUAD REDUNDANT TRANSISTOR CIRCUIT

If 25 such circuits are used, the reliability of the aggregate is given by

$$R = (0.99998)^{25}$$

$$R = 0.99959$$

A graphical comparison of these results for a single quad circuit plus the aggregate of 25 quad circuits is shown in Figure 4-44. As described in the previous example, the time scale has been expanded to show results for operating times greater than 2000 hours. A log scale is used to provide resolution between the two curves.

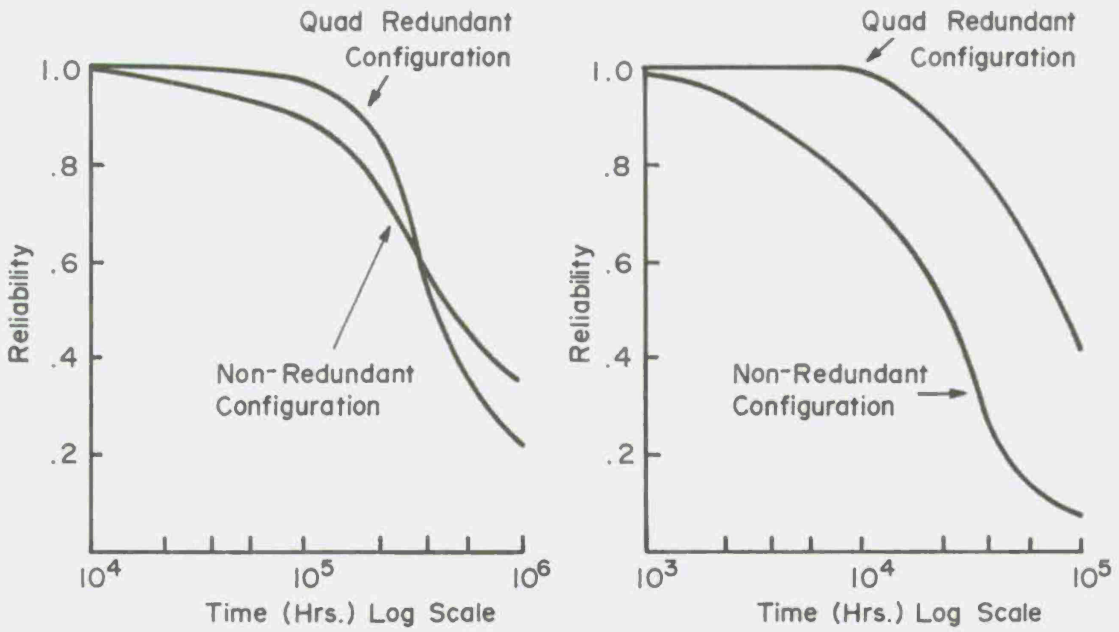


Fig. 4-44 COMPARISON OF RELIABILITY FOR QUAD REDUNDANT AND NON-REDUNDANT TRANSISTOR CIRCUIT

EXAMPLE 3

MAJORITY VOTE REDUNDANCY

This example presents an application of majority voting redundancy. It uses a divider logic circuit as the vehicle to show the application of redundancy. Divider circuits are frequently used in timing applications for computers and space systems. Both the divider and voter circuit are assumed to be packaged within separate integrated circuits. Figure 4-45 presents the logic diagram for a ÷ 8 counter circuit.

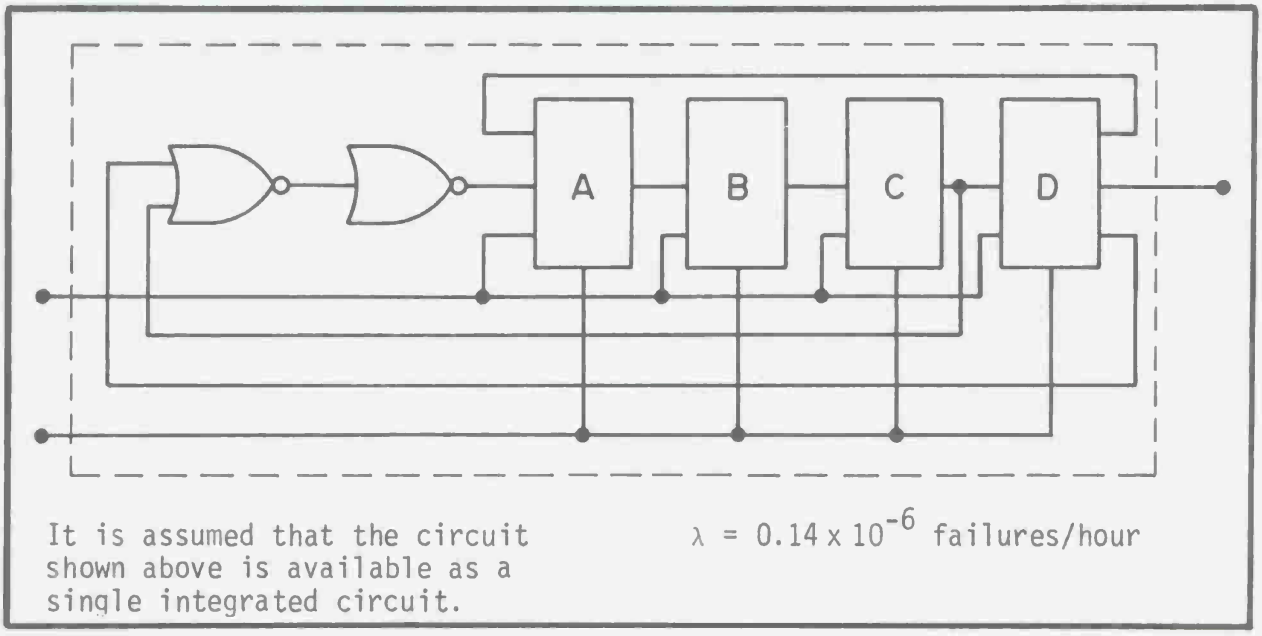


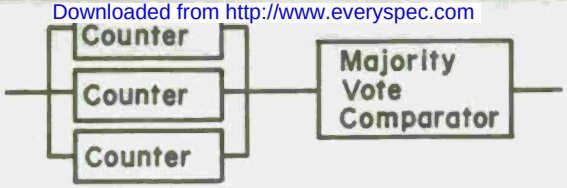
Figure 4-45 ÷ 8 COUNTER CIRCUIT

For an application within an orbiting satellite having a mission life of 4500 hours (approximately six months), the reliability for the nonredundant ÷ 8 counter is given by:

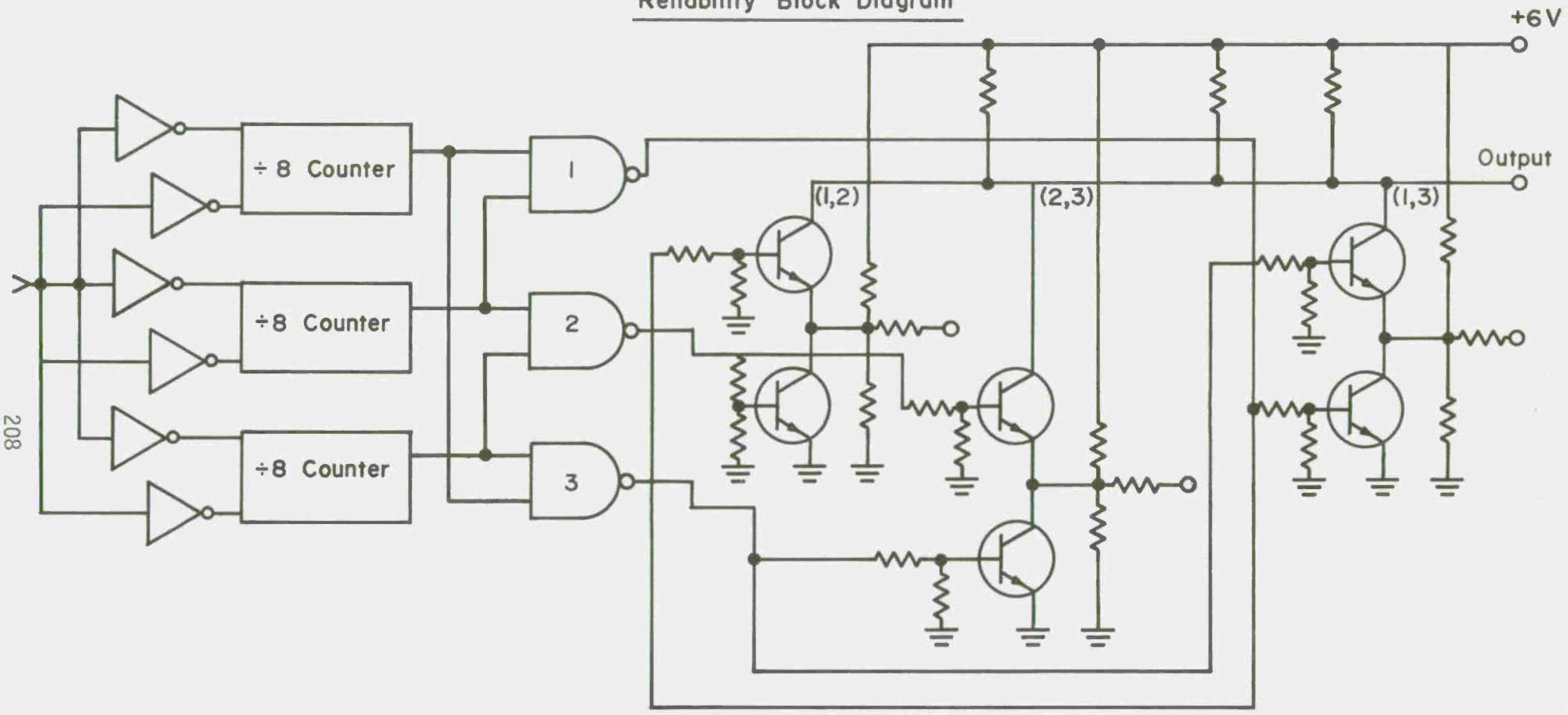
$$R = e^{-\lambda t} = e^{-(0.14 \times 10^{-6})(4.5 \times 10^{3})}$$

$$R = 0.994$$

Figure 4-46 shows the circuit diagram, reliability block diagram and mathematical model for the redundant majority voting configuration for the ÷ 8 counter. A two-out-of-three majority voting circuit possesses the advantage of output selection. This means that any two



Reliability Block Diagram



Redundant Circuit Schematic

$$R = (e^{-\lambda_m t})\left[e^{-3\lambda_p t} + 3e^{-2\lambda_p t}(1 - e^{-\lambda_p t})\right]$$

Mathmatical Model

Where λ_p = Failure Rate Of A Single Counter

λ_m = Failure Rate Of The Comparator Network

Fig. 4-46 TWO OUT OF THREE MAJORITY VOTE REDUNDANT ÷8 COUNTER

of the three ÷ 8 counters need operate correctly for a proper output. The resistor/transistor networks provide for comparison of ÷ 8 counter outputs. Should the output of any ÷ 8 counter fail to match that of the remaining, its output would be inhibited.

Using the mathematical model shown in the figure, the reliability for the majority voting redundant circuit is given by:

$$R = e^{-\lambda_m t}\left[e^{-3\lambda_p t} + 3\, e^{-2\lambda_p t}(1 - e^{-\lambda_p t})\right]$$

where λ_p is the total failure rate of the majority vote/integrated circuit comparator and is equal to 0.007×10^{-6} failures/hour.

For an operating time of 4500 hours,

$R = 0.9999$

A graphical comparison of these results is shown in Figure 4-47 for mission times above 4500 hours. Note also that the time axis has been expanded and a log scale used to provide resolution between the two curves.

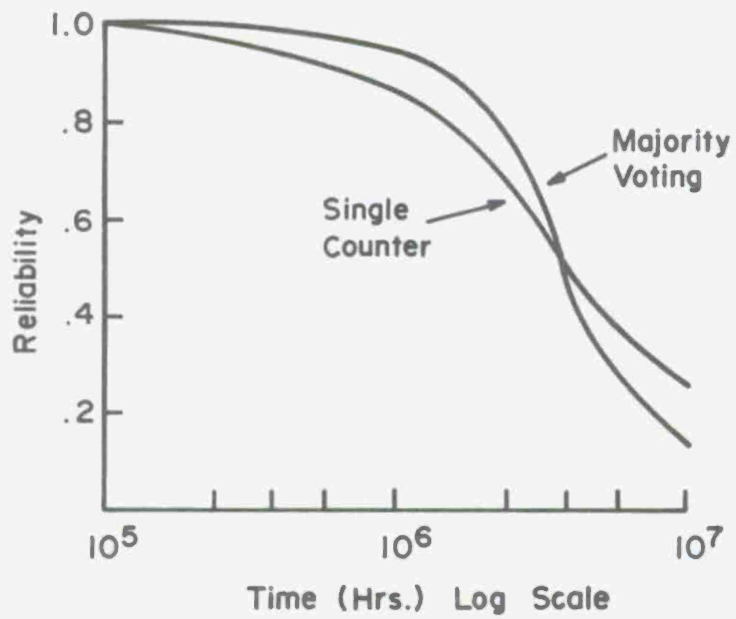


Fig. 4-47 RELIABILITY COMPARISON FOR REDUNDANCY & NON-REDUNDANT ÷ 8 COUNTER CONFIGURATION

EXAMPLE 4

STANDBY REDUNDANCY

This example shows an application of standby redundancy involving switching. This example utilizes functional R-F channels as the vehicle by which redundancy is applied. In this particular application, the redundant channels are isolated at the power input and at both the signal input and output. Switching is accomplished by MOSFET's driven by shift register stages of an address/decode circuit using high voltage amplifiers.[30] Each channel within the redundant configuration consists of:

- R-F and associated circuitry
- Oscillator mixer and associated circuitry
- IF and associated circuitry
- Detector and associated circuitry
- High voltage amplifier
- Shift register
- MOSFET's

Figure 4-48 presents a diagram for a single (nonredundant) R-F receiver channel plus failure rates for the various functional circuits. The total failure rate for the single channel is:

$$\lambda_{Channel} = \Sigma \lambda_{circuits}$$

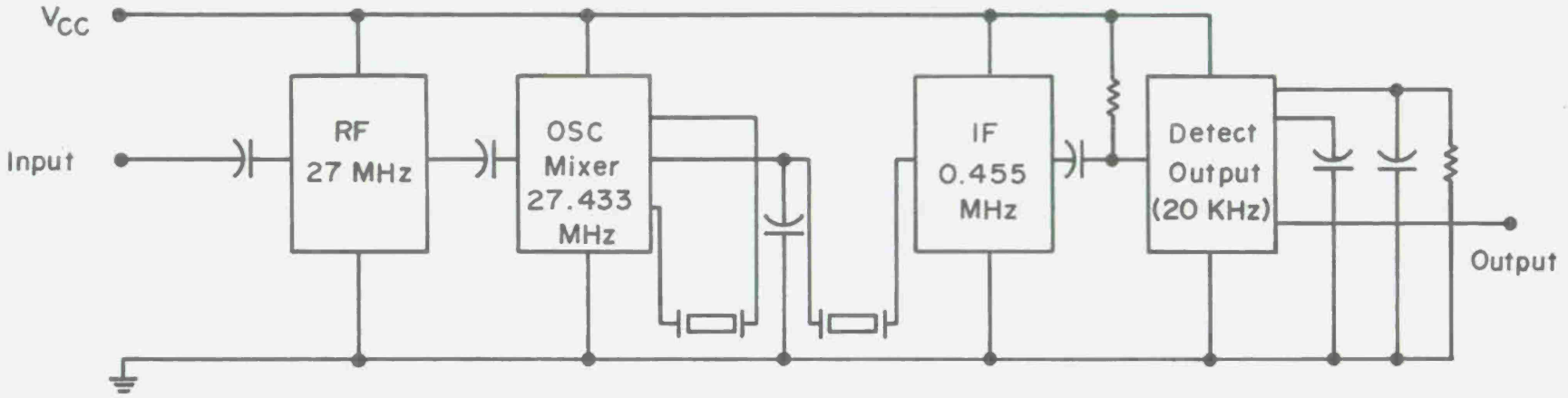
$$= 52.0 \times 10^{-6} \text{ failures/hour}$$

For a 2000 hour operating time, the reliability is:

$$R = e^{-\lambda_{ch} t} = e^{-(52.0 \times 10^{-6})(2000)}$$

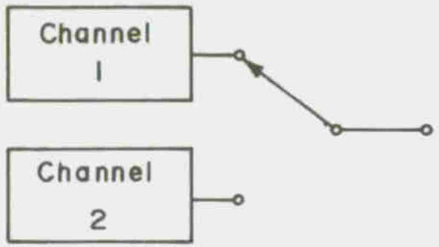
$$R = 0.901$$

Figure 4-49 shows the circuit diagram, reliability block diagram and mathematical model for the two channel redundant configuration. The additional circuitry needed to implement the switching function and isolation between channels are listed below. Circuit failure rates are also given:

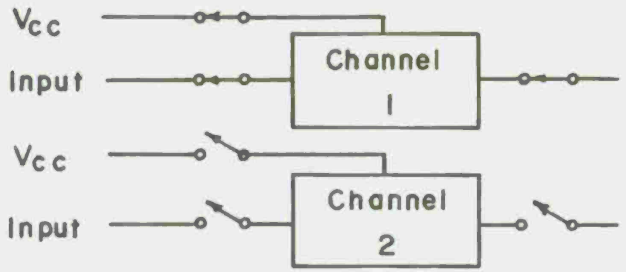


Circuit	Failure Rate ($\times 10^{-6}$)
RF Amplifier And Associated Circuitry	20.5
Oscillator / Mixer And Associated Circuitry	8.4
IF Amplifier And Associated Circuitry	16.2
Detector And Associated Circuitry	6.9
	52.0

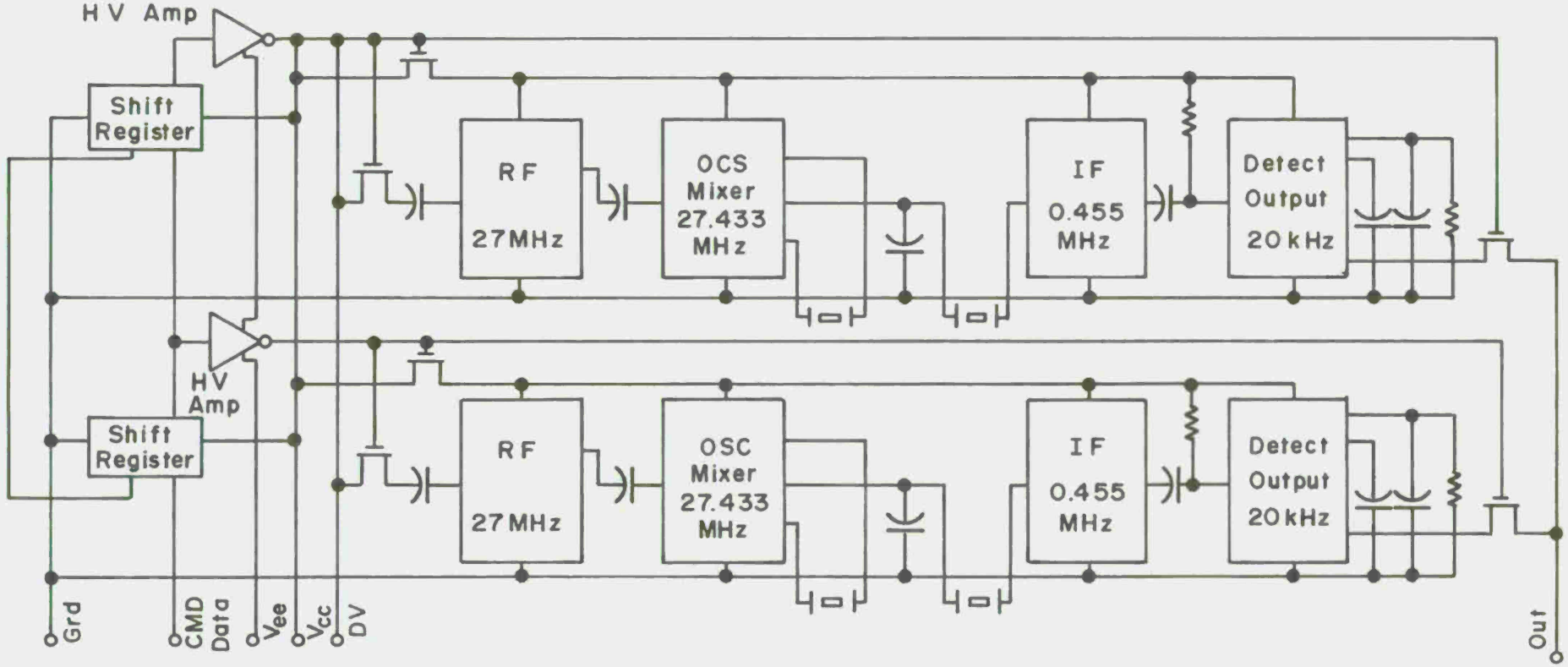
Fig. 4-48 NON-REDUNDANT RF AMPLIFIER CHANNEL



Reliability Block Diagram



Simplified Circuit Block Diagram



Redundant Circuit Block Diagram

$$R = e^{-\lambda CH f}\left[1 + \frac{\lambda CH}{\lambda_s}\left(1 - e^{-\lambda_s f}\right)\right]$$

Mathematical Model

Fig. 4-49 STANDBY REDUNDANT TWO CHANNEL RF RECEIVER

Circuit	n	Failure Rate $\lambda(\times 10^{-6})$	$n\lambda$
Shift register	1	0.23	0.23
High voltage amplifier	1	0.15	0.15
MOSFET output isolators	3	2.70	8.10
		Total	8.48 $(\times 10^{-6})$

Using the mathematical model shown in Figure 4-49, the reliability for the standby redundant R-F receiver is:

$$R = e^{-\lambda_{ch} t}\left[1 + \frac{\lambda_{ch}}{\lambda_s}\left(1 - e^{-\lambda_s t}\right)\right]$$

$$R = 0.9949$$

The results of both redundant and nonredundant configurations are compared in Figure 4-50.

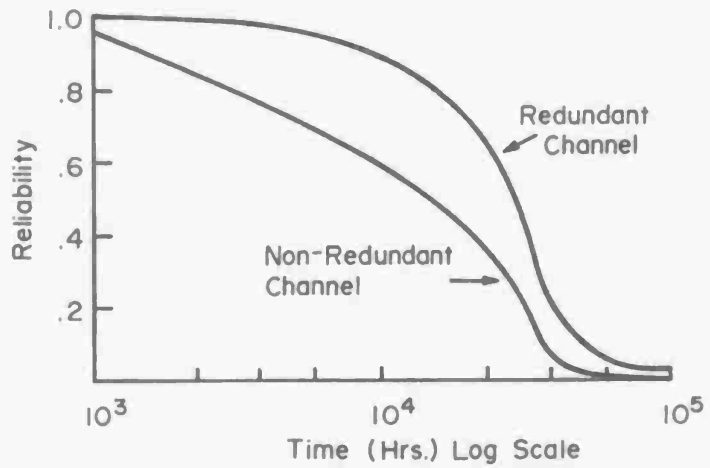


Fig. 4-50 RELIABILITY COMPARISON OF REDUNDANT & NON-REDUNDANT RF RECEIVER CHANNELS

4.1.5 Design Simplification and Analysis

Achieving high reliability in systems and equipment involves the application of specific efforts and analyses to simplify the design to account for transients and to minimize component aging characteristics. In general, simplification without the compromise of performance will enhance reliability. Transient pickup and component aging will cause unreliable operation and malfunction and, when carried to the extreme, lead to overstress and failure. Aging manifests itself by a draft in component values, accompanied by a spread in tolerance limits. These failure characteristics (as described in Section 2 and depicted in Figure 2-1) must be taken into account during design and, in particular, when attempting to improve reliability and extend the useful life portion of the equipment.

The subsections which follow provide detailed information and specific guidelines on these subjects. Subsection 4.1.5.1 covers Design Simplification, 4.1.5.2 covers Degradation Analysis and 4.1.5.3 covers Overstress and Transient Analysis.

4.1.5.1 Design Simplification[32]

Many complex electronic systems have subsystems or assemblies that operate serially. Many of their parts and circuits are in series similar to links of a chain such that only one link need fail to stop the system. This characteristic, along with the increasing trend of complexity in new designs, tends to add more and more links to the chain, thus greatly increasing the statistical probability of failure.

Therefore, one of the steps in achieving reliability is to simplify the system and its circuits as much as possible without sacrificing performance. However, it should be noted that because of the general tendency to increase the loads on the components that remain, there will be a limiting point to circuit simplification. This limit is the value of electrical stress that should not be exceeded for a given type of electrical component. Limit values can be established for various types of components as determined by their failure rates. In addition, it should also be clear that the simplified circuit must meet performance criteria under application conditions (e.g., "worst case") as described

later in this subsection (paragraph 4.1.5.3). During design reviews, special attention should be given to determine if all the circuitry is required in order to perform the intended function.

Design simplification and substitution involves several techniques: (1) the use of proven circuits with known reliability, (2) the substitution of highly reliable digital circuitry (where feasible), (3) the use of high reliability integrated circuits to replace discrete lumped constant circuitry, (4) the use of highly reliable components wherever individual discrete components must be used, and (5) the use of those designs which minimize the effects of catastrophic failure modes.

The most obvious way to eliminate failure modes and mechanisms of a part is to eliminate the part itself. Although design simplification is, in general, practiced, deliberate attempts to remove parts from established designs may not be.

For instance, digital design can have extraneous logic elements incorporated within it. However, minimization techniques, such as by Boolean reduction, are well established and can be powerful tools for incorporating reliability into a design through simplification. For example, consider the application of Boolean reduction to a logic design containing superfluous elements, as shown in Figure 4-51. The original logic diagram is represented by this figure and the corresponding Boolean expression is

$$D = \overline{C} \cap (A \cup \overline{B}) \cup \overline{A} \cap (\overline{B} \cup C) \cup B \cap (A \cup C) \quad (1)$$

Two equivalent reductions are found for this equation. The sum-of-products form

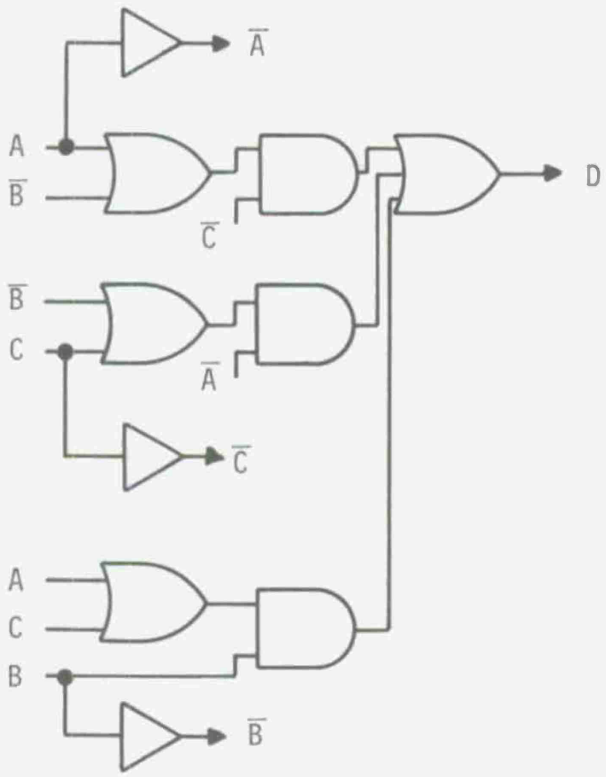
$$D = (\overline{A} \cap \overline{B}) \cup (A \cap \overline{C}) \cup (B \cap C) \quad (2)$$

is the basis for Figure 4-51b, which is simpler than that of Figure 4-51a. Still simpler is the product-of-sums form of reduction

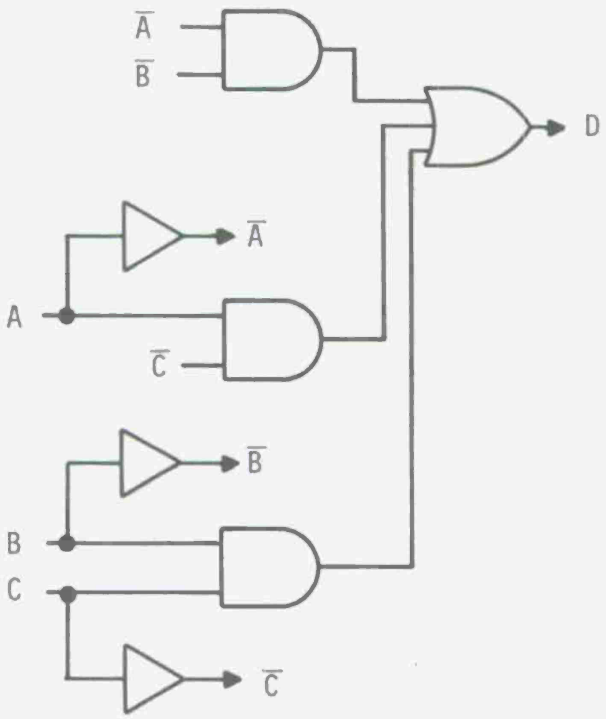
$$D = (A \cup \overline{B} \cup C) \cap (\overline{A} \cup B \cup \overline{C}) \quad (3)$$

which is shown in Figure 4-51c. Simplification can also include the determination and removal of items that have no functional significance.

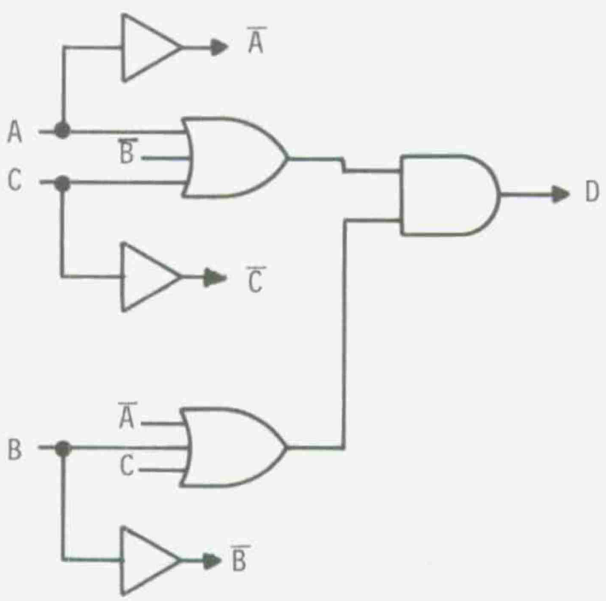
(a) LOGIC DIAGRAM FOR EQUATION 1



(b) LOGIC DIAGRAM FOR EQUATION 2



(c) LOGIC DIAGRAM FOR EQUATION 3



LEGEND

= "AND" Logical Gate

= "OR" Logical Gate

= Logical Inverter

A, B, C = Inputs

$\overline{A}$, $\overline{B}$, $\overline{C}$ = Inversions of Inputs

D = Output

Fig. 4-51 BOOLEAN REDUCTION OF LOGIC ELEMENTS

The optimization by simplicity can permit a high degree of reliability by making success dependent upon fewer items. Thus, the number of potential failures is reduced. Inasmuch as functioning is now dependent upon fewer items, care is necessary to insure that unusual performance is not required of these items. Any simplification wherein the operation of the remaining parts is not adversely altered will yield a reliability improvement.

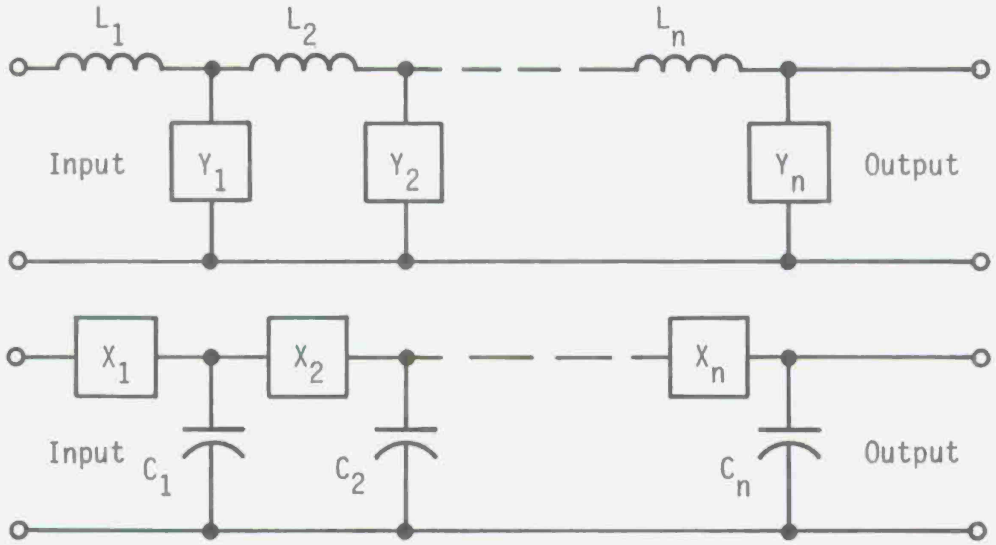
In addition, efforts should also be directed toward the reduction of the critical effects of component failures. The aim here is to reduce catastrophic failures to, at most, a degradation in performance. As an example, consider Figure 4-52, which illustrates the design of filter circuits. A low-pass design, as shown in Figure 4-52a, can involve either series inductances or shunt capacitances. The latter is to be avoided if shorting is the predominant failure mode peculiar to the applicable capacitor types (e.g., solid tantalum), since a catastrophic failure of the filter could result. Similarly, in the high-pass filter of Figure 4-52b, the use of a shunt inductor is superior to the use of a series ceramic capacitor, for which an open is the expected failure mode. Here, the solid tantalum capacitor, if applicable to the electrical design, could be a better reliability risk, since its failure would only result in noise and an incorrect frequency, instead of a complete loss of signal.

4.1.5.2 Degradation Analysis[33]

The failure rate data which appears in this handbook (and in MIL-HDBK-217B) is not based on part changes due to aging. Component parts such as resistors and capacitors are, however, known to change with age and stress so that degradation due to aging can represent a significant failure mode in a complex, long life system (see Figure 2-1, Section 2).

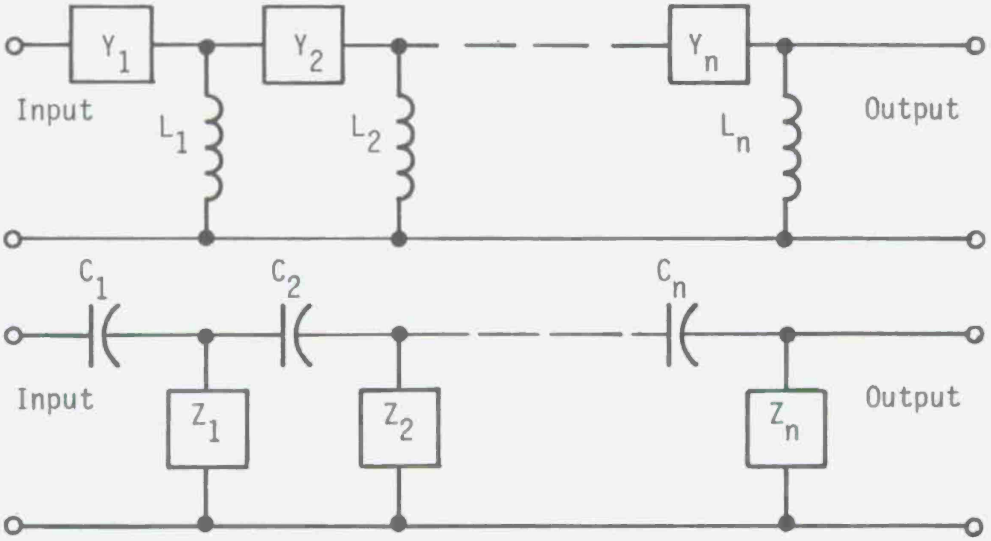
Two examples of part parameter change due to aging are shown in Figure 4-53a through 4-53d. These figures show the average change from initial value versus time and the standard deviation of change from initial value versus time for resistance of a resistor type and the capacitance of a capacitor type. The resistor data is plotted for two stress levels while the capacitor data is plotted at rated voltage. The

(a) LOW-PASS FILTER



LEGEND: T_i, for i = 1,2,...,n: Limited to R and C elements in various acceptable combinations.

(b) HIGH-PASS FILTER



LEGEND: I_i, for i = 1,2,...,n: Limited to R and L elements in various acceptable combinations.

Fig. 4-52 ALTERNATIVE FILTER DESIGNS

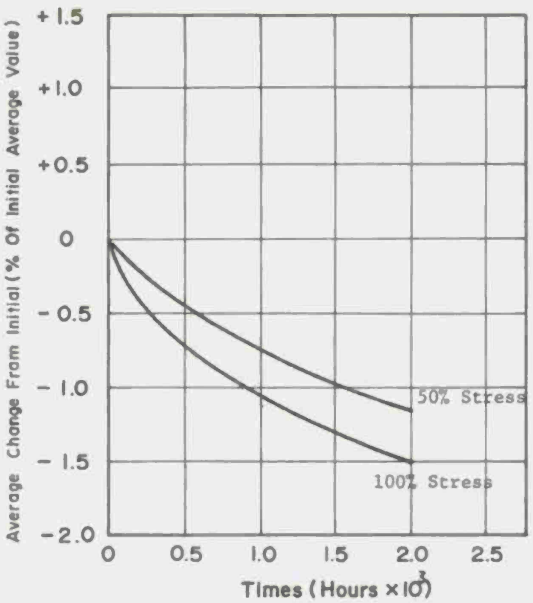


Fig A Average Change From Initial Resistance For MIL-R-11 Carbon Composition Resistors At 70°C Ambient And Various Electrical Stresses.

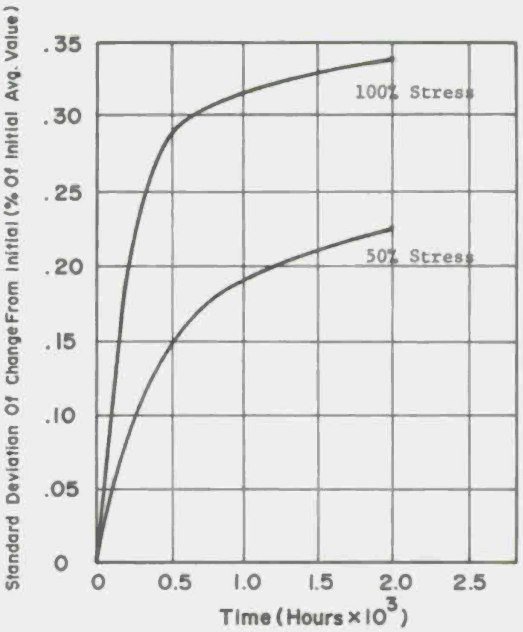


Fig B Standard Deviation Of Change From Initial Resistance For MIL-R-11 Carbon Composition Resistors At 70°C Ambient And Various Electrical Stresses.

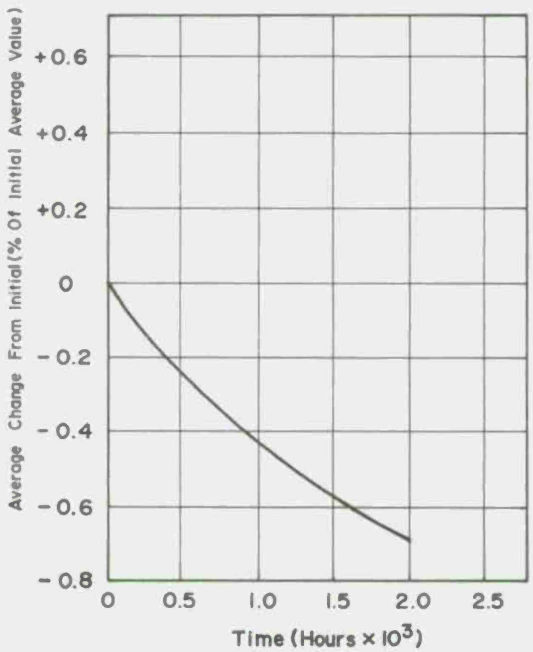


Fig C Average Change From Initial Capacitance For MIL-C-20 Temperature Compensating Ceramic Capacitors At Rated Voltage And 85°C Ambient.

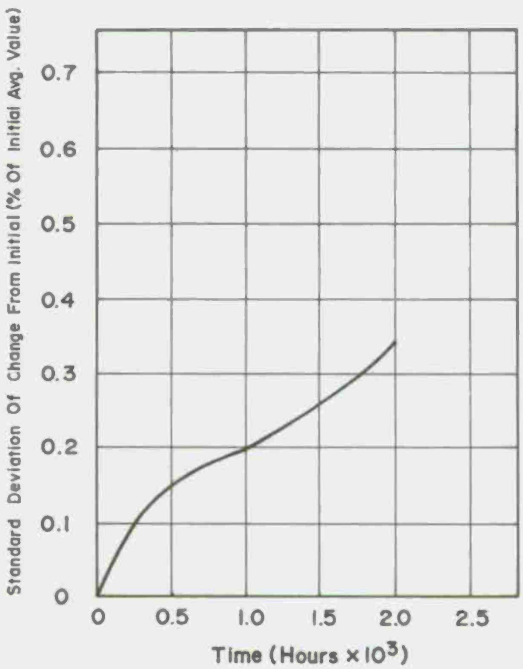


Fig D Standard Deviation Of Change From Initial Capacitance For MIL-C-20 Temperature Compensating Ceramic Capacitors At Rated Voltage And 85° Ambient.

Fig. 4-53 DEGRADATION CHARACTERISTICS DUE TO AGING

resistor data was determined from life test data representing a total of 1520 tested parts from three manufacturers, while the capacitor data came from life test data representing a total of 340 tested parts from two manufacturers. Another type of resistor presentation (Figure 4-54) shows the initial tolerance and nominal value for a parameter, and plots the change in these parameters under one specified stress and temperature condition for a period of time.

There are basically two approaches to reduce part variation due to aging. These are:

(1) Control of device changes to hold them within limits for a specified time under stipulated conditions.

(2) The use of tolerant circuit design to accommodate drifts and degradation in time.

In the first category, as described in Subsection 4.1.1, the technique that is basically used is to precondition the component (burn-in) so that it undergoes significant change early in life but then levels off and becomes relatively constant for the remainder of life. In addition, there is detailed testing and control of the materials going into the part, along with strict control of processes.

In the second category, the attempt is made to design circuitry which is inherently tolerant to part parameter change. Two different techniques that are practiced here are: (1) the use of feedback to electrically compensate for parameter variation and thus provide for performance stability, and (2) the design of circuitry that provides the minimum required performance, even though the performance may vary somewhat due to aging. The latter approach makes use of analyses procedures such as

- worst case analysis
- parameter variation
- statistical design
- transient design
- stability analysis.

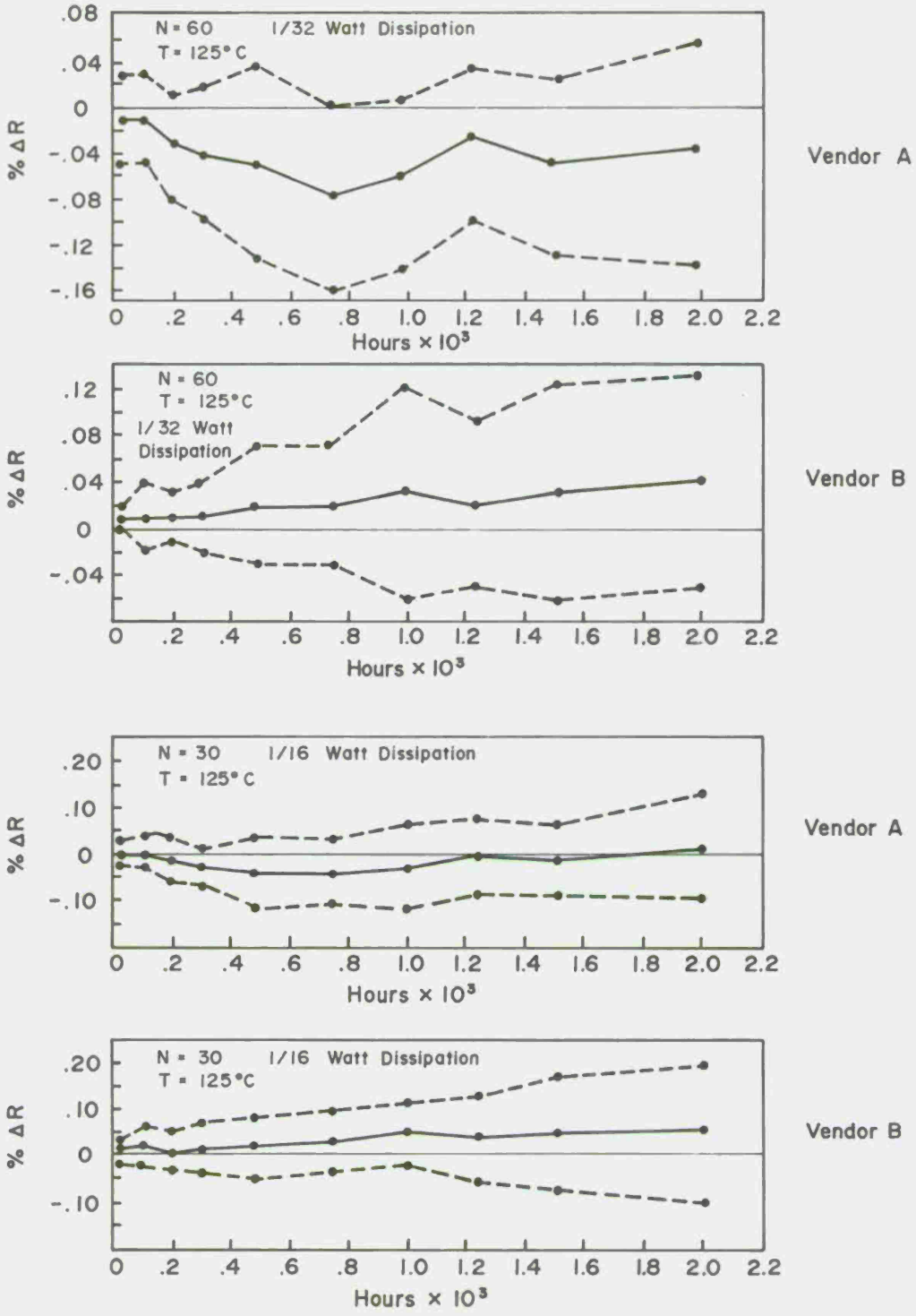


Fig. 4-54 RESISTANCE CHANGE OF 1/8 WATT, FIXED METAL FILM RESISTORS DURING 2000 HOURS OF OPERATION (PERCENTAGE CHANGE IN RESISTANCE)

There are alternate ways to proceed. One way is to view the overall circuit specification as a fixed requirement and to then determine the allowable limits of each part parameter variation. Each part is then selected accordingly. The other way is to examine the amount of parameter variation expected in each part (including the input) and then to determine the output under worst case combination, or other type of combination. The result can then be appraised with regard to determining the probability of surviving degradation for some specified period of time. Many of these analysis methods and their associated mathematical models have been computerized and are available to perform specific analyses of the type mentioned. Table 4-38, taken from MIL-HDBK-217A, indicates the features of some of these computer models.

In worst case analysis, direct physical dependence should be taken into account. For example, if a voltage bus feeds several different points, the voltages at each of the several points would not be treated as variables independent from each other. Likewise, if temperature coefficients are taken into account, one part of the system should not be presumed to be at the hot limit and the other at the cold limit at the same time--unless of course it is physically reasonable that it be so. In the following discussion, it is assumed that these correlations are taken into account wherever possible. A very general boundary condition for the analysis is that the circuit or system should be constructed according to its specifications and that the analysis proceeds from there. Consider now the absolute worst case analysis. In the absolute worst case analysis, the limits for each independent parameter are set without regard to other parameters or to its importance in the system. The position of the limits is usually set by engineering judgment. In some cases, the engineer may perform several analyses with different limits for each case to assess the result prior to fixing the limits.

There can also be modified worst case analyses developed because of the pessimism of the absolute worst case analysis. It is not worthwhile to go into all of these, but a typical one uses the following method for setting the limits: Critical items are given limits as in absolute worst case analysis and the rest of the items are given limits of their purchase tolerance.

Table 4-38 TYPICAL CIRCUIT ANALYSIS TECHNIQUES

Analysis Technique	Type of Analysis	Mathematical Model Necessary	Parts' Data Necessary	Output Information Received	Type of Circuits Suitable
MANDEX Worst-Case Method	Steady state ac and dc worst-case	Circuit's simultaneous equations or matrix equation	Nominal value and end-of-life limits	Worst-case value of output variable compared with allowable value	Class A amplifiers, power supplies, all biasing (dc) circuits, logic circuits, etc.
Moment Method	Statistical	Circuit's simultaneous equation or matrix equation	Mean (or nominal) value and standard deviation or variance of each input parameter and correlation coefficients when they exist	The mean and variance of the distribution of each output parameter	Any circuit for which a mathematical model can be derived
Monte Carlo Method	Statistical; predicts output variable distribution at any time; steady state ac or dc (transient may be performed if formula is available)	Circuit's simultaneous equation, matrix equation, transfer function (any mathematical representation including input parameter	Complete distribution of each input parameter at a time	20 cell histogram for each output variable	Any circuit for which a mathematical model can be derived
VINIL Method	VINIL Method	Piece-wise linear equivalent circuits	Application curves over operating and environmental ranges along with drift data	Input characteristics (maximum and minimum), transfer characteristics (max. and min.), output characteristics (max. and min.)	Digital; linear analog
Parameter Variation Method	General, determines allowable parameter variation before design fails to function. Considers both one and two-at-a-time parameter variation	Circuit's simultaneous equation or matrix equation	A nominal value for each parameter and a range (in per cent)	Failure points for one and two-at-a-time parameter variation Schmoo plot determines safe operating envelope for design	Any steady state ac or dc circuit
SPARC (AEM-1, AEM-2, AEM-3) System of Programs	DC analysis, ac analysis; transient analysis	Equivalent circuits, equations, or matrices	Nominal (mean); Minimum (-3σ); Maximum ($+3\sigma$)	Solution of unknown in floating point fixed decimal output	All types, dc, bias, switching, nonlinear effects, ac response and distributed parameter circuit servo loops and feedback systems
SCAN DC Method	Linear static, nonlinear static	Linear or nonlinear equations in appropriate matrix form with reasonable estimates of values of the unknowns affects by nonlinear equations	Nominal (mean); Minimum (-3σ); Maximum ($+3\sigma$)	Nominal solutions, partial derivatives of unknowns with respect to knowns, worst case values, and the probability of the unknowns being outside of specified limits	All circuits that can be described by linear and nonlinear equations
SCAN AC Method	Linear sinusoidal dynamic analysis	Simultaneous complex variable equations with the real and the imaginary parts of the equations separated	Nominal (mean); Minimum (-3σ); Maximum ($+3\sigma$)	Families of frequency response curves; statistical variation of unknowns at any selected frequency; $+3\sigma$, -3σ and mean of unknowns vs frequency (assumed)	Any linear circuit that contains frequency-dependent devices and which is driven or is significantly analyzed with sinusoidal driving functions
SCAN Transient Method	Linear and nonlinear transient analysis; differential equation solution	Simultaneous differential equations	Nominal parts data; alternate sets of parts' data; parts' data for the switched states	Time response of linear or nonlinear systems	All circuits for which the transient determining effects can be modeled

In any worst case analysis, the values of the parameters are adjusted (within the limits) so that circuit performance is as high as possible, then readjusted so it is as low as possible. The values of the parameters are not necessarily set at the limits--the criterion for their value is to make the circuit performance an extreme. The probability of this occurring in practice depends on the limits which were set by the engineer at the beginning, on the probability functions of the parameters, and on the complexity of the system being considered.

One argument in favor of absolute worst case analysis (as opposed to a statistical analysis) is that many digital electronic systems have many similar parts, each of which must have such a high probability of working properly, that a statistical analysis will, for practical purposes, turn out to be an absolute worst case analysis, and the absolute worst case analysis is much simpler and depends on fewer assumptions.

Computer routines are available for performing these analyses on electronic circuits. Generally speaking, the curve of circuit performance versus each independent parameter is assumed to be monotonic and a numerical differentiation is performed at the nominal values to see in which direction the parameter should be moved to make the circuit performance high or low. It is also presumed that this direction is independent of the values of any of the other parameters as long as they are within their limits. If these assumptions are not true, a much more detailed analysis of the equations is necessary before worst case can be performed. Essentially, this involves generation of a response surface for the circuit performance which accounts for all circuit parameters.

4.1.5.3 Overstress and Transient Analysis

Semiconductor circuit malfunctions can arise from two general sources: transient circuit disturbances and component burnout. Generally, transient upsets are the controlling factor, because they can occur at much lower energy levels.

Transients in circuits can prove troublesome in many ways. Flip-flops and Schmitt triggers can be inadvertently triggered, counters can change count, memory can be altered due to driving current or direct magnetic field effect, one-shot multivibrators can pulse, the transient

can be amplified and interpreted as a control signal, switches can change state, semiconductors can latch-up in undesired conducting states that require reset, etc. The effect can be caused by transients at the input terminals, output terminals, on the supply terminals, or on combinations of these. Transient upset effects can be generally characterized as follows:

- Circuit threshold regions for upset are very narrow. That is, there is a very small amount of voltage amplitude difference between the largest signals which have no probability of causing upset and the smallest signals which will certainly cause upset.
- The dc threshold for response to a very slow input swing is calculable from the basic circuit schematic. This can establish an accurate bound for transients that exceed the dc threshold for times longer than the circuit propagation delay (a manufacturer's specification).
- Transient upsets are remarkably independent of the exact wave-shape, and depend largely on the peak value of the transient and the time duration over which the transient exceeds the dc threshold. This waveform independence allows relatively easy experimental determination of circuit behavior with simple wave-forms (square pulse).
- The input leads (or signal reference leads) are generally the ones most susceptible to transient upset.

It can further be noted that standard circuit handbook data can often be used to gauge transient upset susceptibility. For example, square pulse triggering voltage is sometimes given as a function of pulse duration. A typical plot for a low level integrated circuit is shown in Figure 4-55.

As indicated above, it is possible for semiconductors to latch up in undesired conducting states that require reset (power removal). There are various ways in which this can happen. One common way is shown in Figure 4-56. This shows an open-base transistor circuit with collector current as a function of collector-emitter voltage. The load line for a particular collector resistance is shown. The collector current

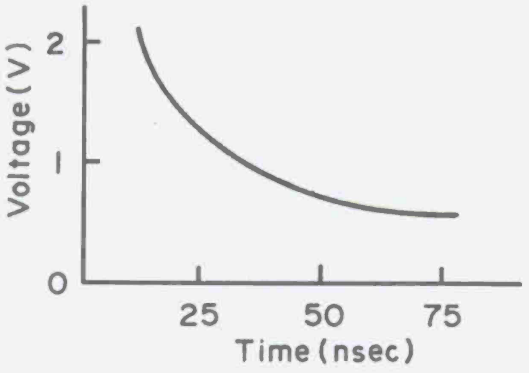


Fig. 4-55 SQUARE PULSE TRIGGERING VOLTAGE FOR TYPICAL LOW LEVEL INTEGRATED CIRCUIT.

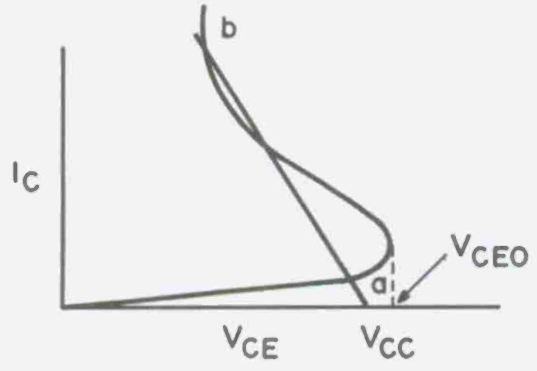


Fig. 4-56 LATCH UP RESPONSE

is normally low (operating point a). However, a transient can move the operating level to point b, where the circuit becomes latched up at a high current level. The signal required to cause this event can be determined by noting that the collector-emitter voltage must be driven above the V_{CEO} (collector-emitter breakdown) voltage.

Another mode of latch-up can occur when a transistor is grown in a semiconductor substrate, for example, an n-p-n transistor in a doped p-substrate. Under unusual voltage or gamma radiation stress, the device can act like an n-p-n-p or SCR device, latching into conduction.

(For this reason, integrated circuits in missile and aircraft systems usually have dielectric isolation rather than junction isolation.)

Overstress

Although various system components are susceptible to damage, the most sensitive of these tend to be semiconductor components. This data will be emphasized first and will then be followed by data on resistors and capacitors. Also, the transistor data given below are immediately followed by suggestions for transient suppression.

Transistor Overstress

In a vulnerability study, conducted by Braddock, Dunn and McDonald (BDM)[34], a considerable amount of data on semiconductor failure from overstress was compiled. The test procedure was approximately as follows. The BDM studies used square pulse testing with pulse durations from 100 nsec to 20 μsec. In the course of the studies, it was determined that reverse diode current and reverse base-emitter current had the lowest failure thresholds, so these were studied rather extensively. For simplicity, the collector was left open during transistor testing. This restriction did not grossly affect the results, since collector current is a second-order effect. BDM found that failure was almost always due to junction hot spots, although metallization and bond damage could sometimes also occur. The criterion for failure was a 15% decrease in β or zener voltage, although this was not crucial since the difference between the level where slight degradation occurred and complete failure occurred was only about a half an order of magnitude. The 2N2222 was then extensively tested for statistical analysis. After testing approximately 700 of these devices, it was found that the average power failure level was

$$P \simeq 0.1\, t^{-0.48}$$

where P is the power (W) and t is the time (sec). These data were spread over about one order of magnitude as indicated in Figure 4-57. There appeared to be no significant variation due to different manufacturers or different geometries. Data for other types of transistors are shown in Figure 4-58.

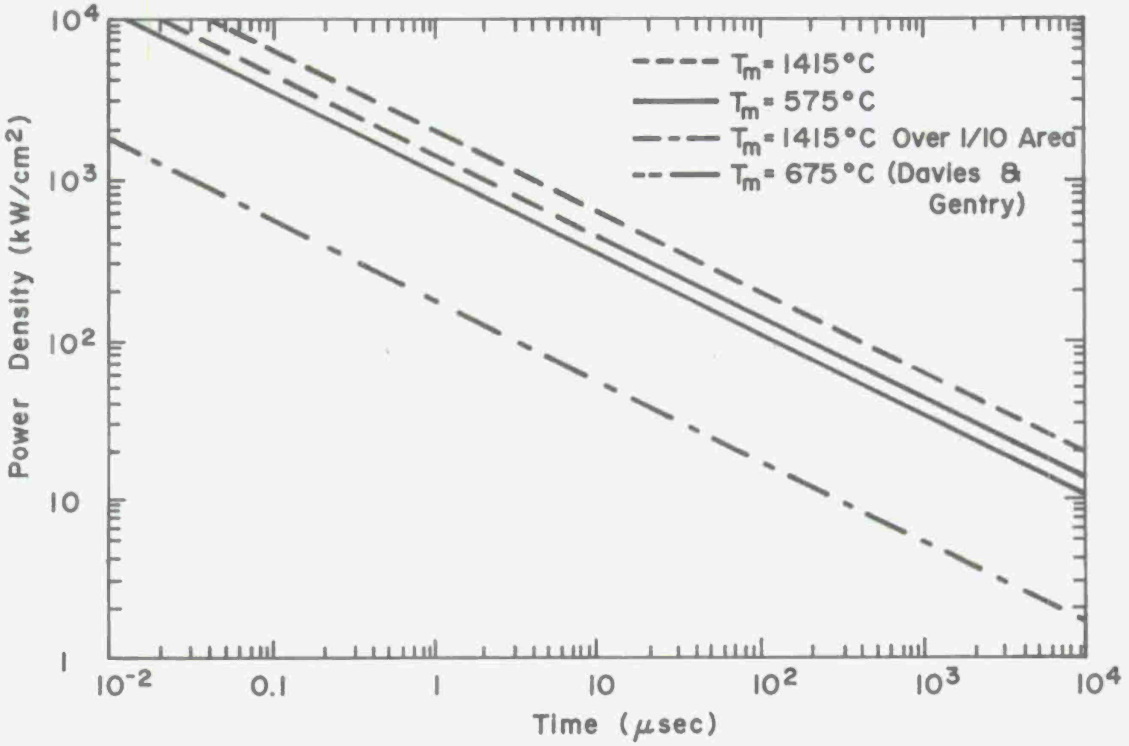


Fig. 4-57 2N2222 OVERSTRESS FAILURE DATA

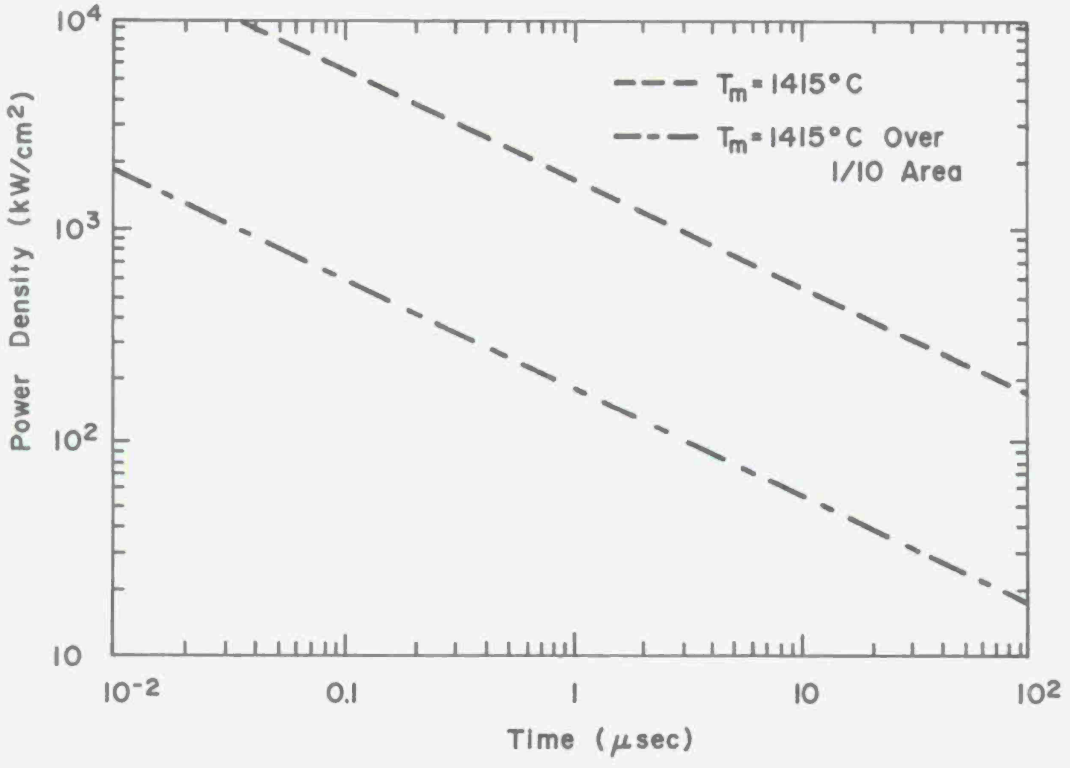


Fig. 4-58 OVERSTRESS FAILURE DATA FOR EIGHT TRANSISTORS

Transient Suppression for Semiconductors

There are many techniques available for transient suppression. Some of these are illustrated in Figure 4-59 through 4-64, and apply in the following areas:

- Transistors
- SCR's
- CMOS
- TTL Protection
- Diode Protection

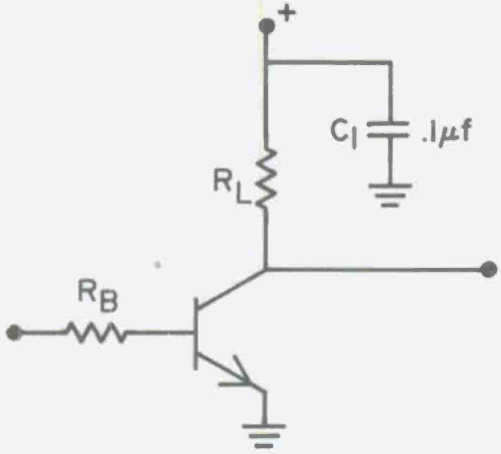
These techniques are representative of generally applicable methods and are not intended as an exhaustive list.

Resistor Overstress

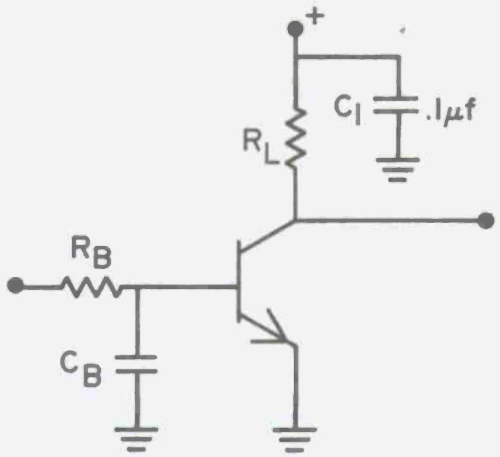
Sandia Laboratories[35] has performed pulse testing on a limited quantity of carbon composition, metal film and wire wound resistors. The test results are indicative of the transient vulnerability of these particular devices. The tests indicated that these three types of resistors were able to withstand pulse powers far in excess of their dc power rating. (The power ratings of the resistors ran from ¼ watt carbons to 10 watt wire wound.) Wire wound resistors withstood pulse power of more than 5000 times their dc rating, metal film resistors more than 1000 times, and carbon composition resistors more than 500 times (pulse widths $\leq$ 20 μsec).

The test conditions were approximately as follows. High voltage pulses were supplied directly across the resistor and an electronic counter was used to count the number of pulses applied. The average power of the pulse was equal to or less than the average power rating of the resistors. The duty cycle was less than one percent. The pulse waveform was rectangular, as shown in Figure 4-65. (Pulse waveform was not altered in any noticeable way during tests.) Test results are shown in Figures 4-66 through 4-68.

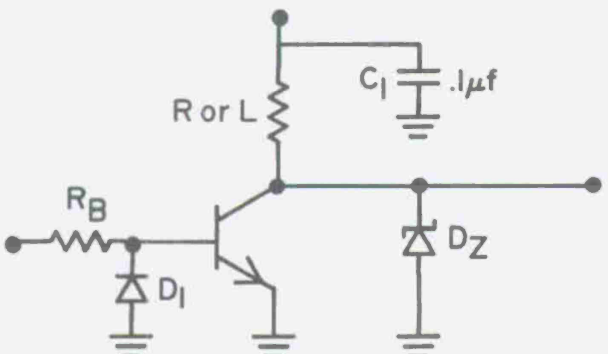
The maximum safe voltage (E_p) given therein represents the voltage at which the resistor did not change in value during a minimum of 100 pulses. The following examples demonstrate possible uses of these results.



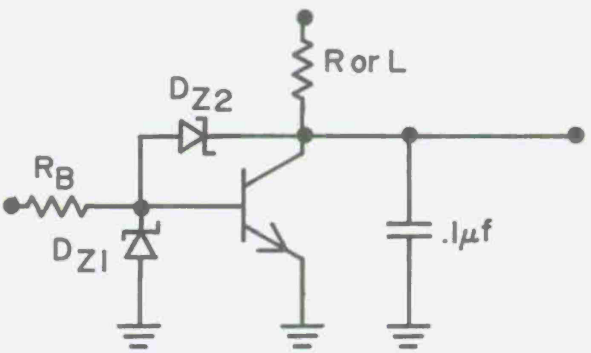
(A) Current Limiting Resistor (R_B) And Transient Suppression Capacitor (C_1)



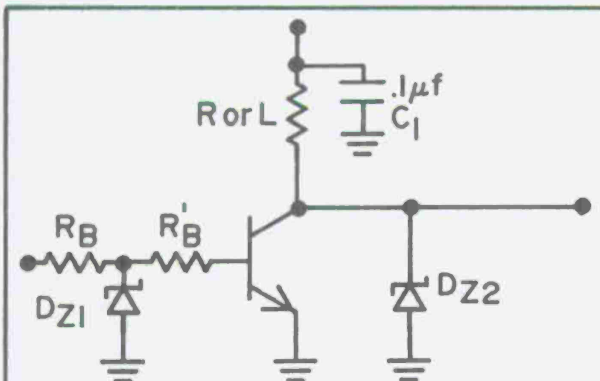
(B) Low Gain Filter (R_B, C_B) And Transient Suppression Capacitor (C_1)



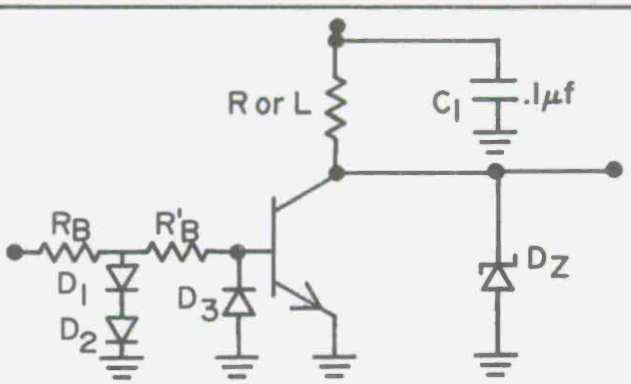
(C) Transient Limiter (R_B, D_1, D_Z) And Transient Suppression Capacitor (C_1)



(D) Transient Suppression For Base And Collector (R_B, D_{Z1}, D_{Z2})

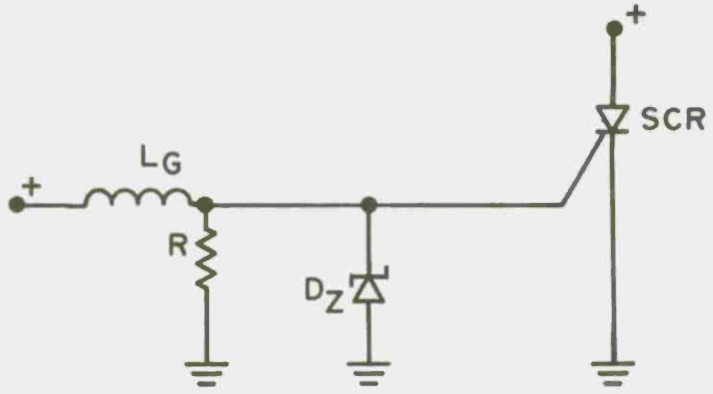


(E) Reverse And Forward Transient Limiter (R_B, D_{Z1}, D_{Z2}) And Transient Capacitor

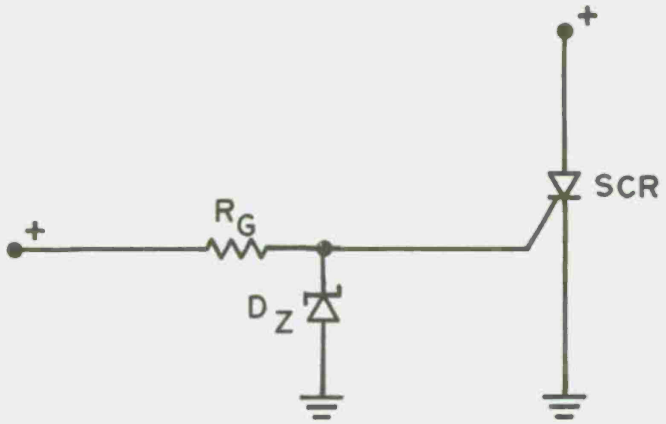


(F) Complete Transient Protection (R_B, D_1, D_2, D_Z, C_1)

Fig. 4-59 TRANSISTOR PROTECTION

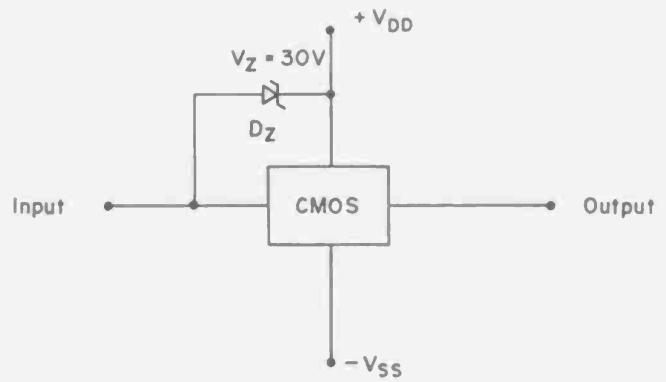


(A) Integrator (Lg, R) Serves To Limit The Initial Surge Current When The Gate Is Turned On. Diode Dz Protects Against Voltage Transients. The PIV of the SCR Should Be Chosen To Provide Sufficient Anode To Cathode Protection.

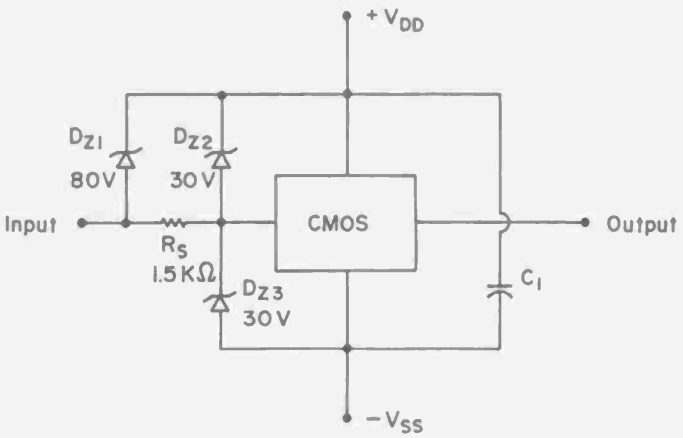


(B) Resistor R_G Limits The Gate Current Of The SCR and Diode Dz Protects The Gate Against Voltage Transients

Fig. 4-60 SCR PROTECTION



a) Single Diode Clamps Positive Input Voltage To V_{DD} And Negative Input Voltages To V_{DD} − 30 Volts Thus Preventing Gate Breakdown.



b) Diode D_{Z2} And D_{Z3} Clamps Positive Input To V_{DD} And Negative Input To V_{SS}. Diode D_{Z1} And R_S Provide Time Delay And Current Limit Action. Capacitor C_1 Prevents High Frequency Transient From Entering The Device Through The Power Supply.

Fig. 4-61 CMOS PROTECTION

a) Store Unused Devices In Conductive Foam Or Use Any Method That Shorts All Leads Together.

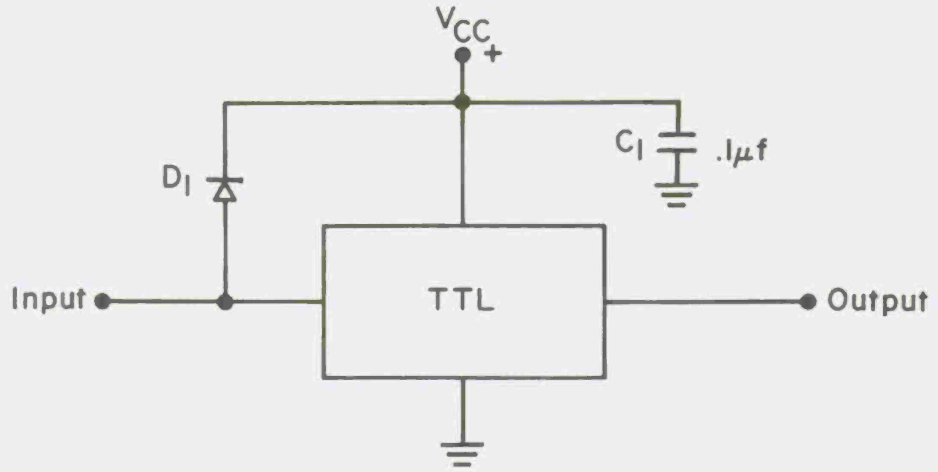
b) Use Grounded Soldering Iron.

c) Ground All Test Equipment.

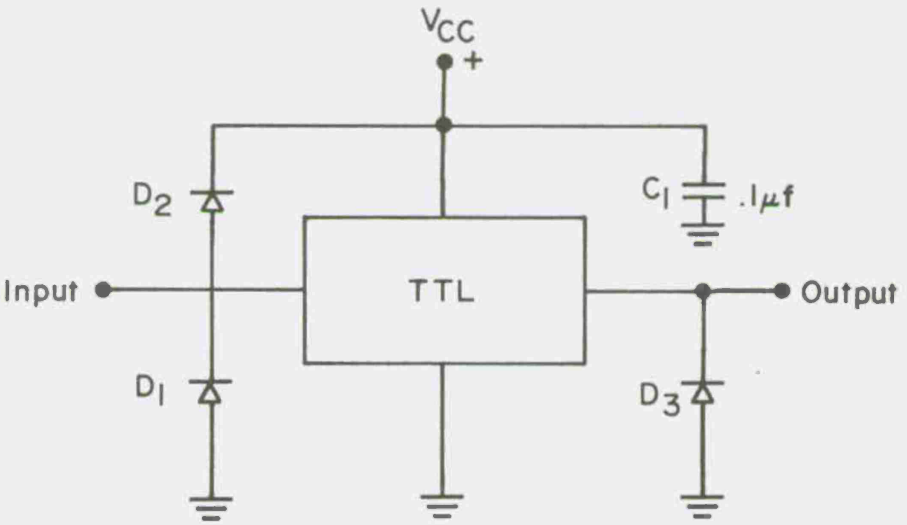
d) All Unused Device Inputs Should Be Connected To V_{DD} Or V_{SS}.

e) All Low Impedance Equipment Should Be Disconnected From Device Inputs Before DC Power Supplies Are Turned Off.

Fig. 4-62 CMOS HANDLING PRECAUTIONS

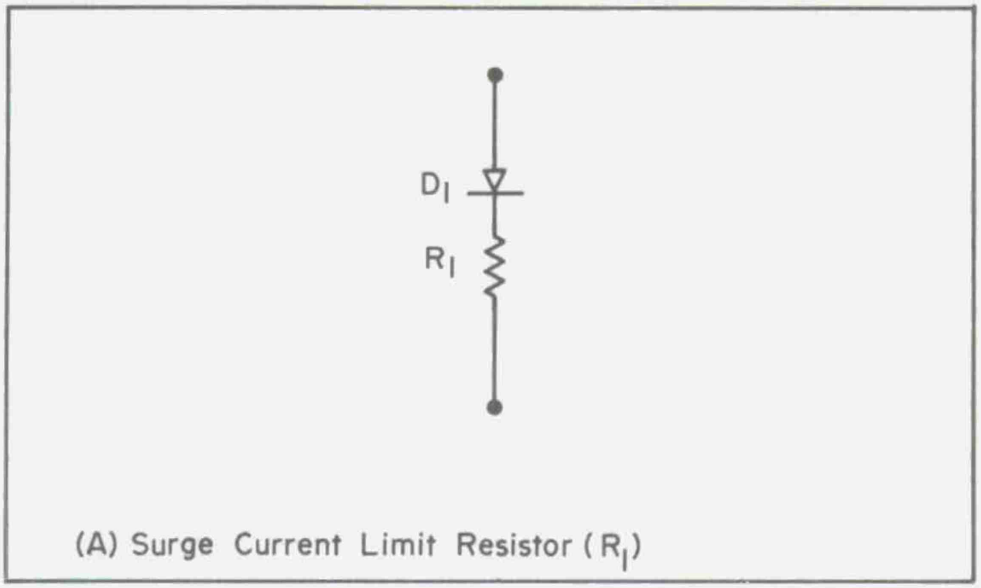


(A) Diode D_1 Presents Input From Becoming Greater Than V_{CC} And Capacitor C_1 Absorbs High Frequency Transients On The Power Supply Line

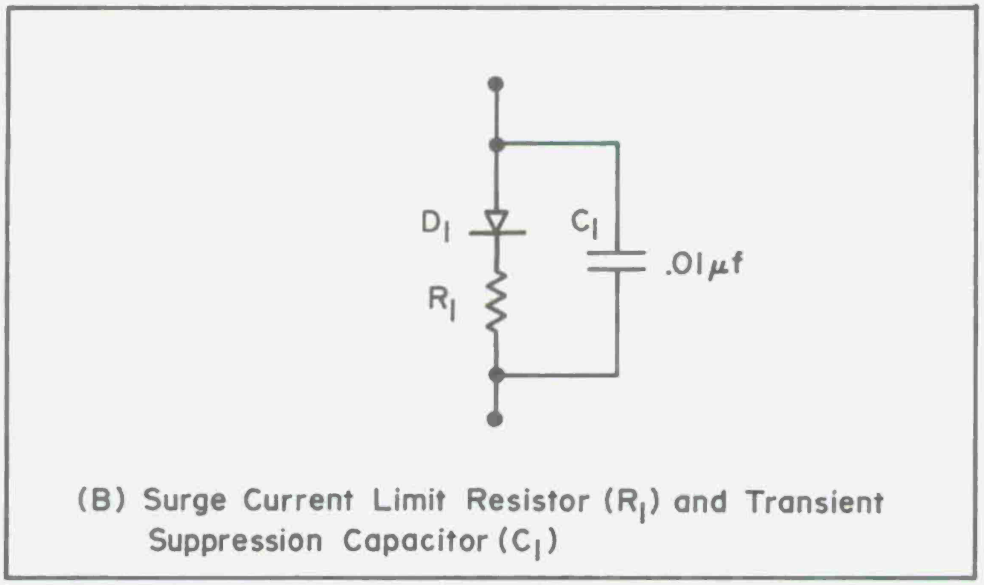


(B) Diodes D_1 And D_2 Clamp The Positive Input To V_{CC} And The Negative Input To Ground. Diode D Prevents The Output From Going Below Ground C_1 Absorbs High Frequency Transients On The Power Supply Line.

Fig 4-63 TTL PROTECTION



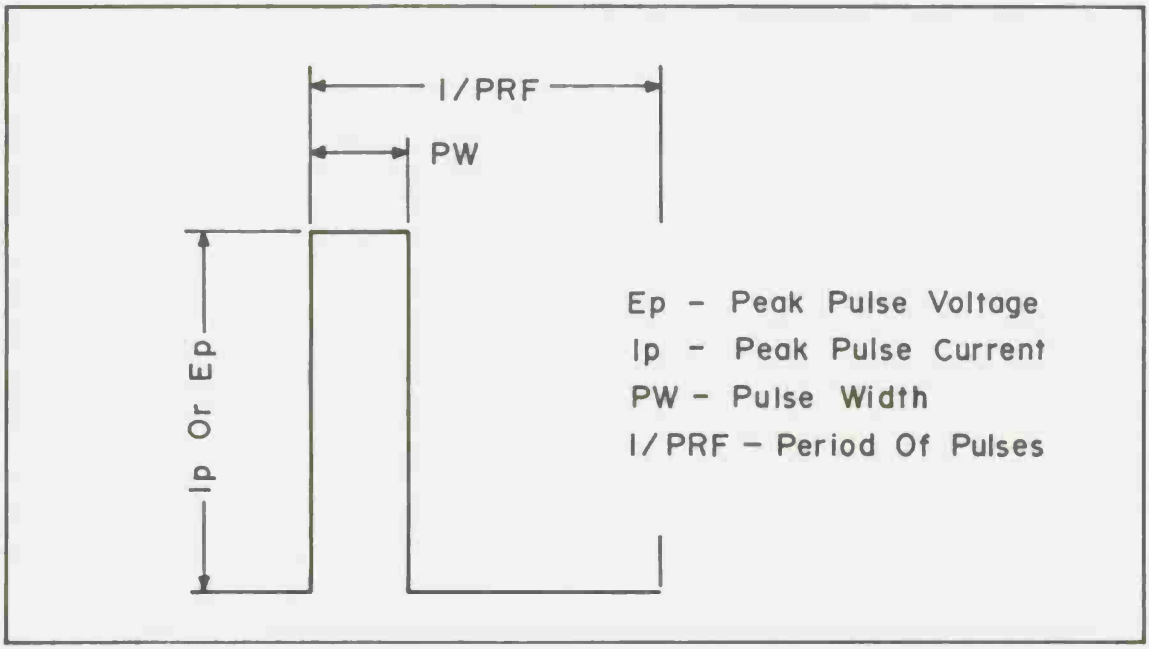
(A) Surge Current Limit Resistor (R_I)



(B) Surge Current Limit Resistor (R_I) and Transient Suppression Capacitor (C_I)

Note: The Best Protection For A Diode Is Sufficient Overrating Of The Reverse Breakdown Voltage (PIV), Forward Surge Current (I_S) And Power Disipation Capability (P)

Fig. 4-64 DIODE PROTECTION



Power Of The Pulse : $P_{pulse} = (Ip) \times (Ep)$ Or $P_{pulse} = (Ep)^2/R$

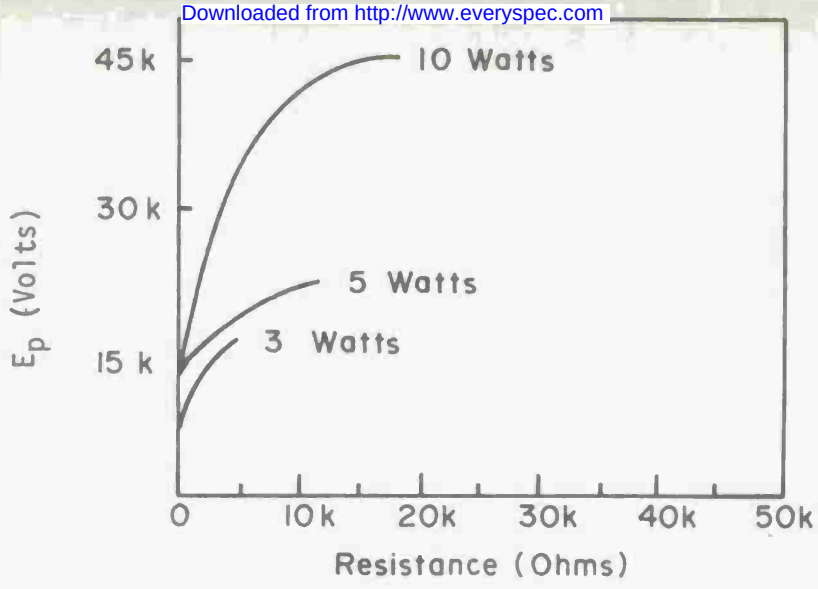
Energy Of The Pulse : $E_{pulse} = (P_{pulse}) \times (PW)$

Average Power Of The Pulse : $P_{avg.} = (P_{pulse}) \times (PW)/(1/PRF)$

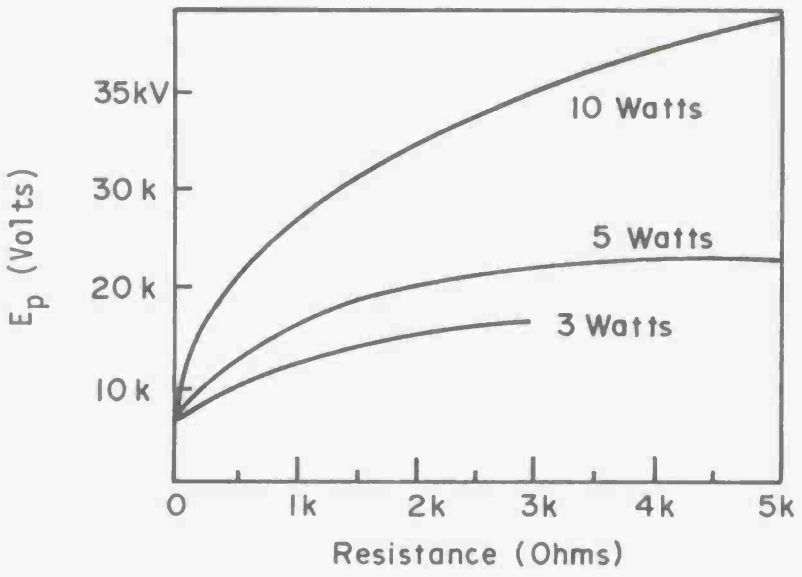
Duty Factor Of The Pulse : $DF = PW/(1/PRF)$

Fig. 4-65 PULSE WAVEFORM

(a)



(b)



(c)

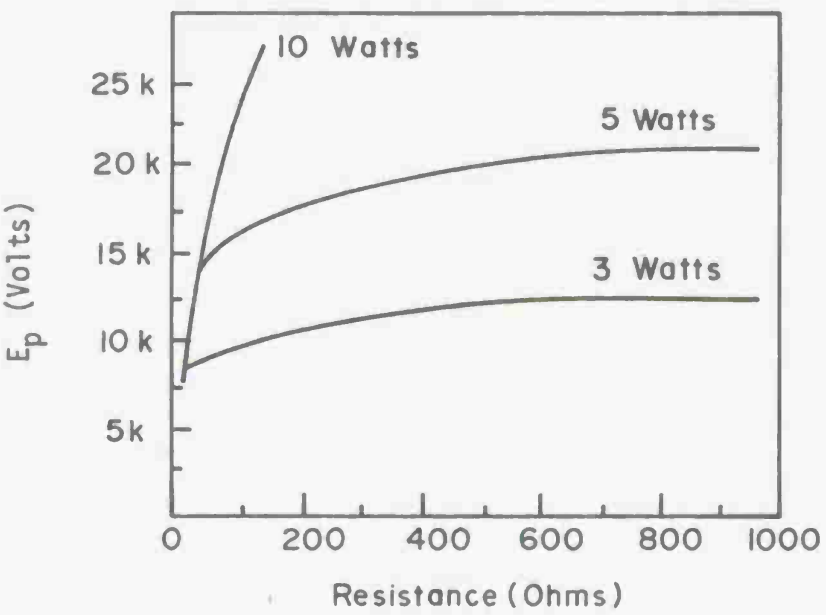
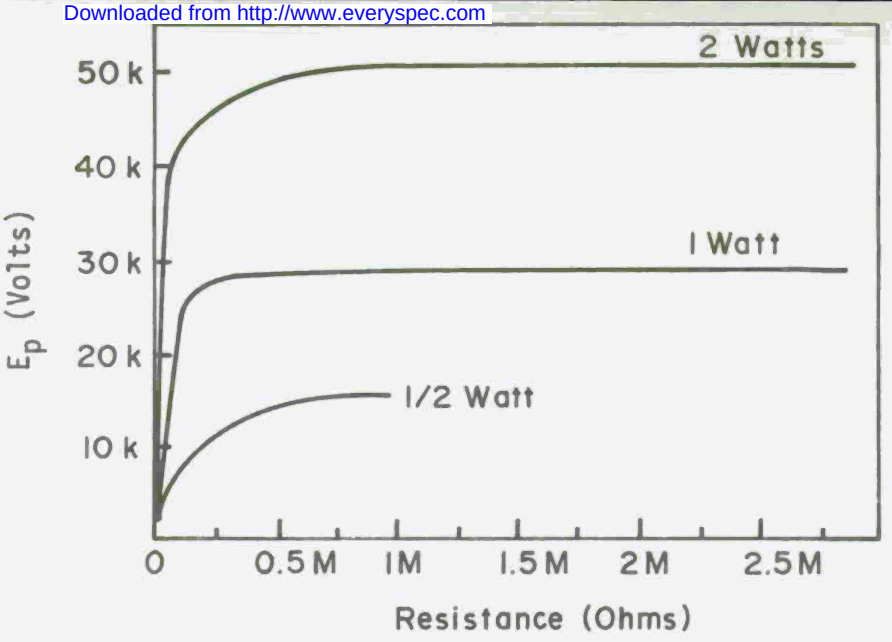
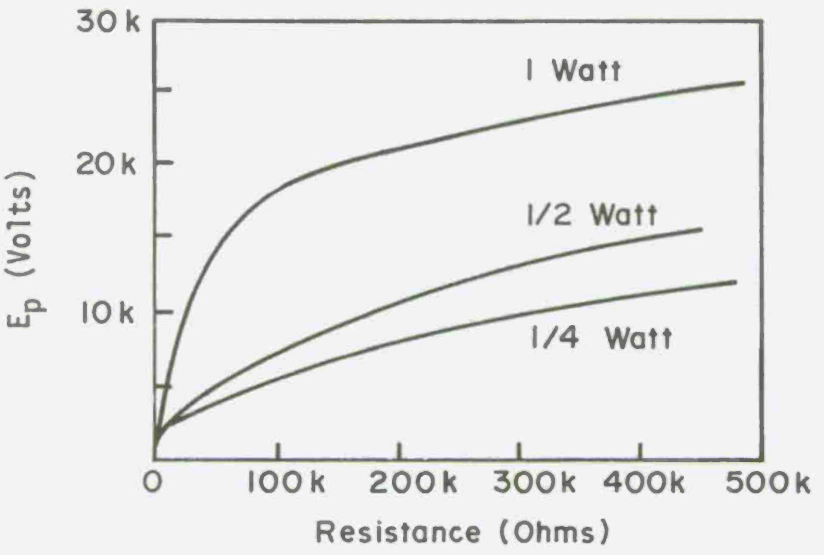


Fig 4-66 WIRE-WOUND RESISTORS

(a)



(b)



(c)

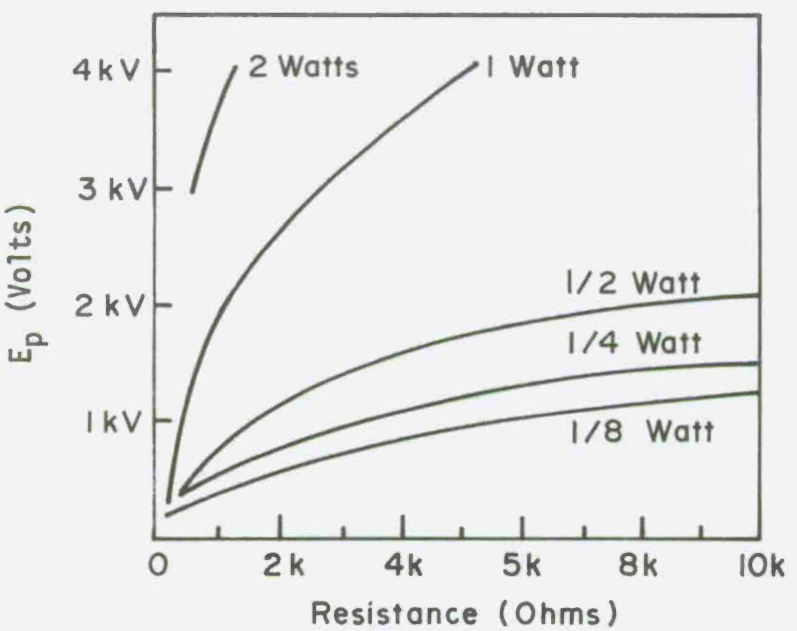
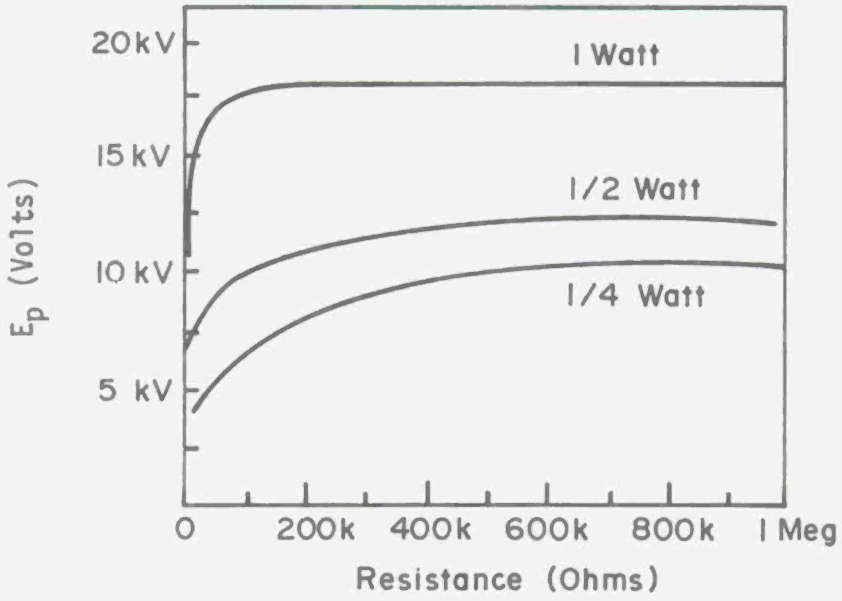


Fig. 4-67 METAL FILM RESISTORS

(a)



(b)

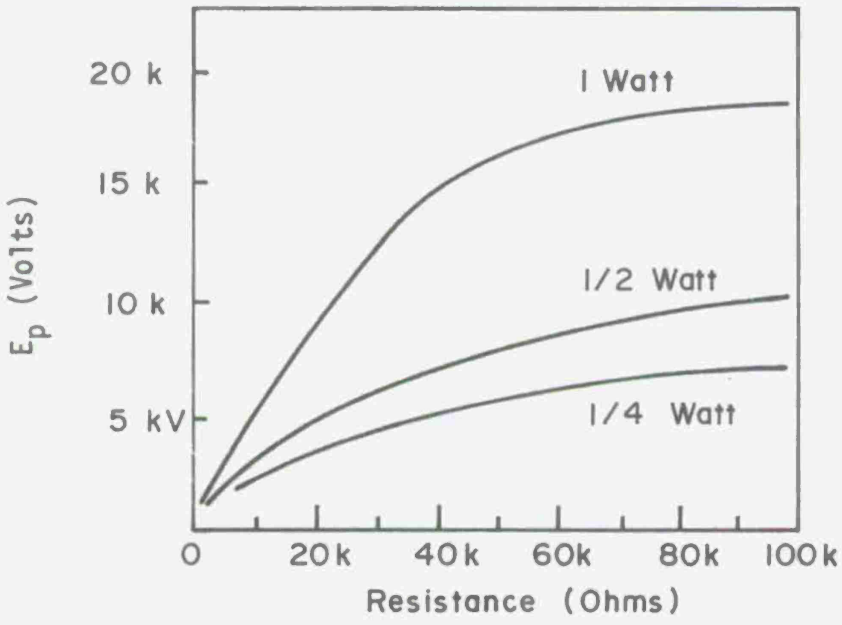


Fig 4-68 CARBON-COMPOSITION RESISTORS

Example 1

Consider an application that requires a resistor to withstand a pulse of 2 kV at a pulse width of 20 μsec with a resistance value of 2.0 KΩ. From Figures 4-66 through 4-68, it is seen that the following resistors meet this requirement.

- wire wound, 3 W or larger
- metal film, 1 W or larger
- carbon composition, 1 W or larger.

Example 2

Consider an application that requires a resistor to withstand a pulse of 10 kV at a pulse width of 20 μsec with a resistance value of 1.0 KΩ. From Figures 4-66 through 4-68, it is seen that the following resistors meet this requirement.

- wire wound, 3 W or larger
- metal film, 1 W or larger
- carbon composition, 1 W or larger.

Note that if the pulse width is narrower than 20 μsec, the recommended maximum pulse voltage may be exceeded. If, however, the pulse width is wider than 20 μsec, then the pulse voltage must be reduced. Figure 4-69 shows how the pulse width affects the maximum pulse voltage for one particular case.

Further, it is interesting to note the relationship between resistor survival and pulse width. From Figure 4-69, it is seen that the narrower the pulse, the longer the life of the resistor. For example, a pulse of 800 V can open the resistor in less than 10 pulses at a pulse width of 10 μsec; on the other hand, the resistor remains undamaged at the end of 100 pulses for a pulse width of 1 μsec.

Capacitor Overstress

Although semiconductor devices, such as diodes and transistors, generally tend to be the ones most susceptible to failure from transient overstress, the overstress mechanism can also be responsible for failure to other devices. The transient voltage tolerance and failure level of two types of low power low voltage capacitors are discussed in this

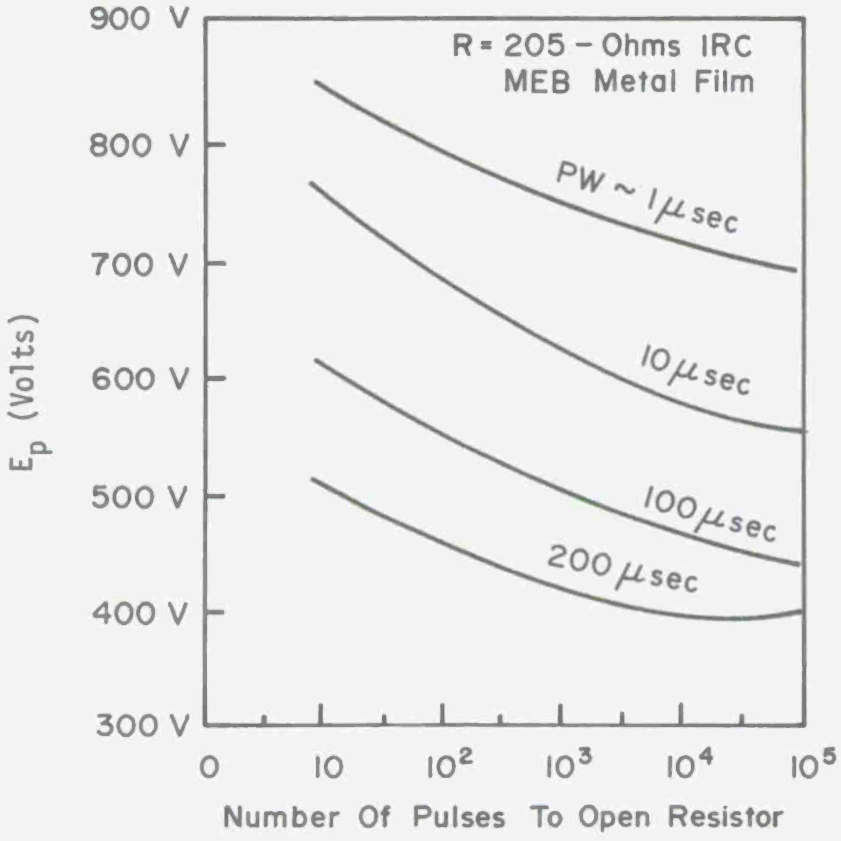


Fig.4-69 PULSE WIDTH VS. MAXIMUM PULSE VOLTAGE

section. The damage failure levels of these devices are compared to other typical electronic components, as indicated in Table 4-39.

The data shown here are based on tests of two types of common low voltage capacitors, and were conducted by Harry Diamond Laboratories.[36] The devices under test were ceramic disc capacitors and solid tantalum electrolytic capacitors. The test procedure was approximately as follows. The capacitors were single pulse tested and the capacitance, dissipation factor, and leakage resistance was measured before and after each pulse application in order to correlate the parameter change. The open circuit test pulse was varied in width from 1 to 30 μsec, with the amplitude varying from the 50 V no-fail pulse in the case of the tantalums in reverse polarity, to the 10 kV pulse needed to break down the ceramics. The rectangular pulse was applied through both a low impedance (1 Ω) and a moderate impedance (100 Ω) network in order to evaluate the effect of

Table 4-39 DAMAGE ENERGIES*

Component	Energy (μJ)
Point Contact Diodes 1N82A-2N69A	0.7 - 12
Integrated Circuits μA709	10
Low Power Transistors 2N930-2N1116A	20 - 1000
High Power Transistors 2N1039 (Ger)	1000 and up
Switching Diodes 1N914-1N933J	70 - 100
Zener Diodes 1N702A	1000 and up
Rectifiers 1N537	500
Solid Tantalum Capacitors	61 and up

*Typical energy failure levels of semiconductors compared to the energy required to damage low voltage tantalum capacitors. Based on a 1 μsec square damaging pulse.

current limiting. The effects of charge rate were also examined by the use of ramp testing. (In ramp testing, the capacitor only partially charges during the duration of the pulse.) The ramp voltage pulse method gave more consistent, though essentially the same, failure levels, as indicated in Table 4-40.

The test matrices for the ceramic and the solid tantalum capacitors are shown in Tables 4-40 and 4-41, respectively. Figure 4-70 is a plot of the reverse polarity breakdown energies for two different values of solid tantalum capacitors.

Table 4-40 CERAMIC CAPACITORS

Capacitance	WVDC	Wave Shape	Mean Breakdown Voltage	Standard Deviation in Breakdown Voltage	Minimum Breakdown Voltage
50 pf	1000	rectangular	9679.9	1698.0	7300.0
		ramped	10287.5	1619.9	7300.0
		both	9998.9	1664.6	7300.0
1000 pf	1000	rectangular	6097.2	538.9	5472
		ramped	5891.0	541.2	4900
		both	5971.6	546.8	4900

Table 4-41 SOLID TANTALUM CAPACITORS

Breakdown Voltage							
Polarity	Capacitance	WVDC	Mean	Standard Deviation	Minimum	Pulse Width	Number of Tested Devices
Forward	0.0047 µf	35	154.5	43.1	90.0	2.6 & 4 µs	19
Forward	2.2 µf	35	154.5	43.1	90.0	4.8 & 30 µs	24
Forward	2.2 µf	15	142.6	48.7	68.0	3.0 & 30 µs	17
Reverse	0.0047 µf	35	106.0	19.7	65.0	1.0 & 10 µs	15
Reverse	2.2 µf	35	106.0	19.7	65.0	3.0 & 30 µs	15
Reverse	2.2 µf	15	53.7	6.5	43.0	30 µs	6

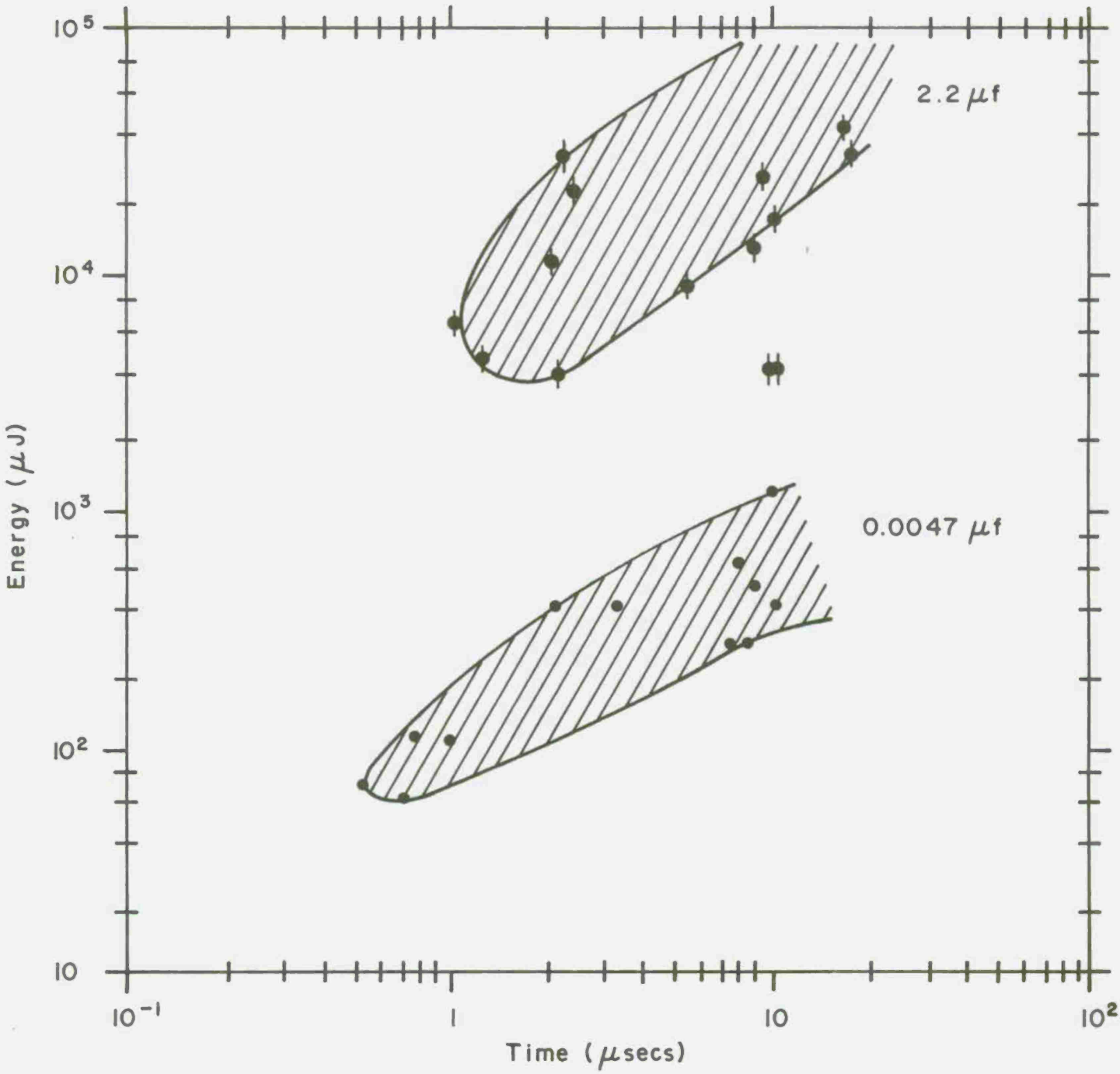
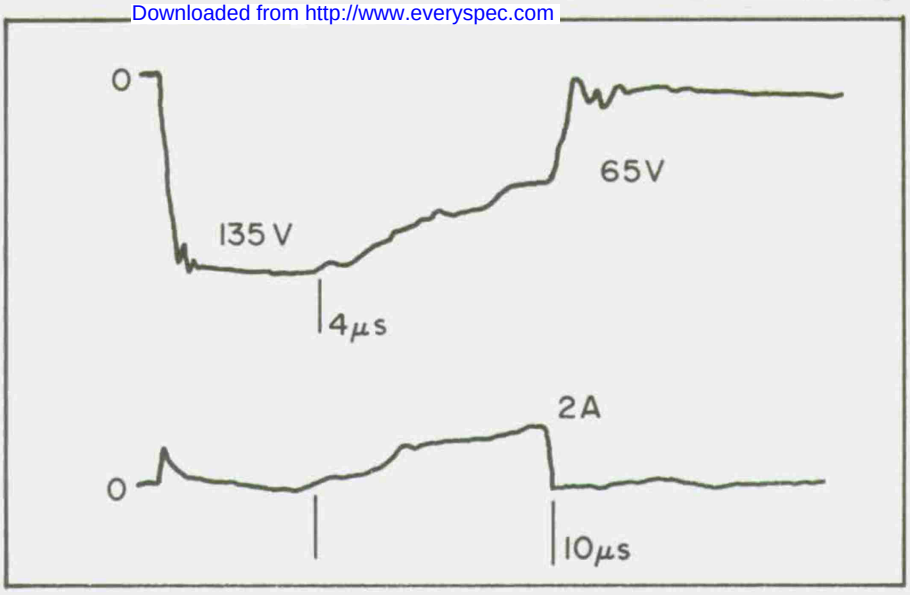


Fig 4-70 PLOT OF REVERSE ENERGY FOR FAILURE FOR THE 35 WVDC SOLID TANTALUM DEVICES

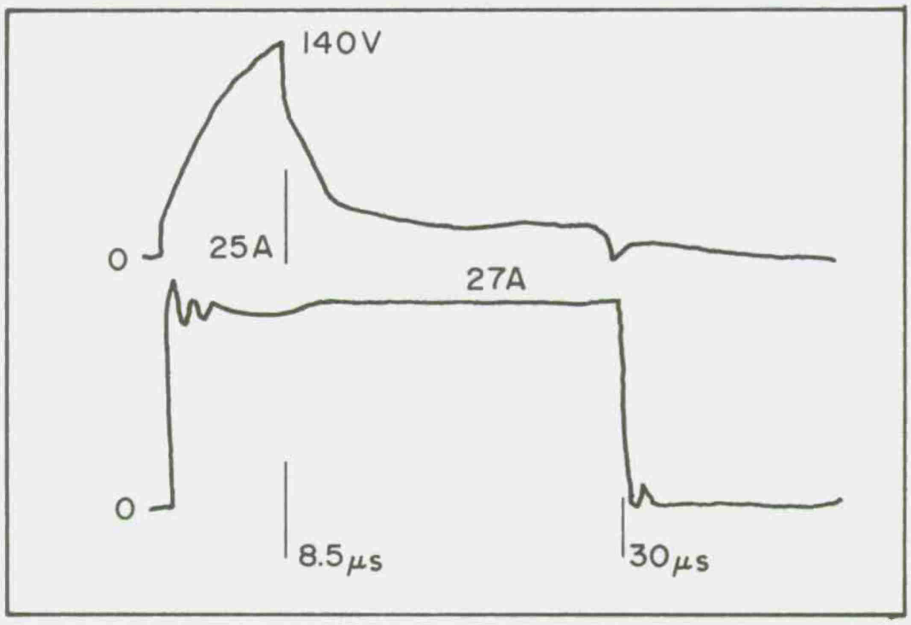
In general, the nonpolar dielectric capacitors exhibited voltage breakdown at four to six times their dc rated voltage level when subjected to pulse excitation in the microsecond time region. Normal charging characteristics were seen prior to the point of breakdown. At breakdown, the voltage dropped rapidly, while the current showed a corresponding increase. Arcs were often seen. The result of such breakdown is to reduce the capacitor's leakage resistance and subsequently the breakdown voltage level, presumably by creating tracking paths in the material or in the encapsulation. The extent of the damage depends on the amount of energy dissipated after the breakdown and on the location of the breakdown site. In some instances, a capacitance change was noted, as well as a device fracture.

The electrolytic capacitors exhibited a broad range of vulnerability which appears to vary with capacitor value, voltage rating, and the particular construction. The results on solid tantalum capacitors showed relatively low damage levels. The levels are comparable to those for semiconductor devices. Refer to Table 4-39 for comparison. The rectangular pulse response of the tantalum devices varied with the circuit loading. Generally, after the voltage reached some critical value as shown in Figure 4-71, increased conduction through the device was seen. (Normal charging characteristics were seen prior to this point.) The current then increased with time, and correspondingly the voltage across the capacitor decreased with time, until a sharp drop was seen in the voltage, which was then accompanied by a sharp rise in the current. When this behavior was evident in the response, the device could also be expected to suffer a decrease in leakage resistance. When the circuit loading was of low impedance, the response appeared similar to the "second breakdown" effect seen in reversed semiconductor junctions. In these cases, the device goes into an avalanche mode, and, after a given amount of energy is dissipated in the device junction, it then switches to a second breakdown state. Failure occurs rapidly in this second breakdown state. Models have been formulated for predicting the time at which a device would enter this second breakdown at given power levels. These models are based on localized heating of portions of the device junction. When a critical temperature is reached, second breakdown occurs. The

(A) .0047μf, 35 WVDC
Normal Polarity



(B) 2.2μf, 35 WVDC
Reverse Polarity



(C) 2.2μf, 15 WVDC
Normal Polarity

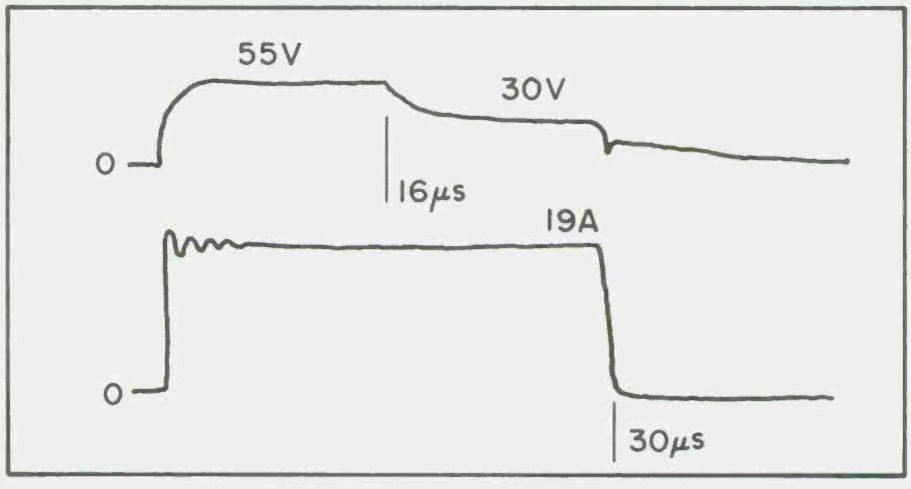


Fig 4-71 CAPACITOR PULSE RESPONSE

relationship generally employed for second breakdown prediction is of the form

$$P = A_1 T^{-\frac{1}{2}}$$

or correspondingly

$$E = A_2 T^{\frac{1}{2}}$$

where P and E are the power and energy, respectively, required for failure at a given rectangular pulse width, T. "A" represents a constant usually determined by measurement. Test data indicate a gross dependence between the square root of pulse width and the energy required for the initiation of the high current low voltage state. The reverse polarity tends to appear slightly more sensitive than the forward. The general response, both forward and reverse, appears similar in character for the tantalum capacitors.

Overall results of the ceramic and the solid tantalum tests, as well as other capacitor types, are shown in Table 4-42.

Table 4-42 FAILURE LEVELS OF COMMON CAPACITORS

Capacitor/Description	Voltage* Mean/Min (volts)	Minimum Pulse Width (μsec)	Energy Max/Min (μJ)	Failure
0.5 μf, 100 Vdc etched tantalum foil	F-250 R-250	0.1 0.1	> 1300 > 1300	No No
0.56 μf, 35 Vdc solid tantalum	F-80 R-80	0.1 0.1	> 490 > 490	No No
5.0 μf, 50 Vdc wet tantalum slug	F-32 R-32	0.1 0.1	> 190 > 190	No No
50 pf, 1000 Vdc ceramic	10000/7300	---	---	Yes
1000 pf, 1000 Vdc ceramic	6000/4900	---	---	Yes
0.0047 μf, 35 Vdc solid tantalum	F-150/90 R-110/65	0.25 0.7	1,000/86 1,100/61	Yes Yes
2.2 μf, 35 Vdc solid tantalum	F-150/90 R-110/65	5.5 1.2	50,000/3500 40,000/3300	Yes Yes
2.2 μf, 15 Vdc solid tantalum	F-140/68 R-54/73	0.1 2.0	30,000/1100 20,000/1200	Yes Yes
10 pf	1000	8.0		No (10 pulses)
4700 pf, 500 Vdc	1000	8.0		No (10 pulses)
1 μf, 200 Vdc	1000	8.0		No (10 pulses)
0.022 μf, 600 Vdc	1000	8.0		No (10 pulses)
100 μf, 75 Vdc	R-2250	2.0		No (13 pulses)
400 μf, 15 Vdc	R-2250	2.0		No (3 pulses)

*F: Forward
R: Reverse

SECTION 4.2

DESIGN TO MINIMIZE RELIABILITY DEGRADATION DURING PRODUCTION AND USE

4.2.1 Contributions to Reliability Degradation

4.2.2 Design for Ease of Inspection and Maintenance

- 4.2.2.1 Hardware Partitioning
- 4.2.2.2 Fault Diagnosis
- 4.2.2.3 Prediction of Incipient Failures

4.2 Design to Minimize Reliability Degradation During Production and Use

As discussed in Section 1.2, a reliability (i.e., MTBF) estimate computed using MIL-HDBK-217B prediction techniques will reflect the reliability potential of a system or component item during its useful life period. This estimate depicts the inherent (or potential) reliability of the design as defined by its engineering documentation, basic stress/strength design factors and gross application factors. However, the estimate does not represent operational reliability unless design failures have been eliminated, manufacturing and quality defects have been minimized and operating and maintenance procedures have been optimized. Therefore, to insure high field reliability, special efforts, designed specifically for the purpose of minimizing reliability degradation, must be applied during system design and development, production, operation and maintenance. Lack of effort in these areas can result in a system reliability as low as 10% of its inherent reliability (see Subsection 2.2). Furthermore, experience has indicated that the degree of degradation is directly related to the level of inspectability and maintainability built into the system. The purpose of this subsection is to provide information and guidelines to design for ease of inspection and maintenance, thus providing the means to minimize production and use degradation. Subsection 4.2.1 discusses those factors that contribute to unreliability and which can be controlled during production and use. Subsection 4.2.2 provides design for ease of inspection and maintenance information and guidelines.

4.2.1 Contributions to Reliability Degradation

The specific objectives of this subsection are to:

(a) Provide insight into basic fabrication and manufacturing processes which can be planned and traded off during design to minimize degradation effects.

(b) Establish the conceptual framework for viewing field maintenance procedures as contributors to operational unreliability.

(c) Estimate the advantage of additional process controls, tests or better inspection.

The key to minimizing and controlling reliability degradation is to estimate the defects introduced by production and maintenance. Two types of defects must be considered--quality defects and reliability defects. Quality defects are defined as those defects which can be located by conventional inspection. Reliability defects are those defects which require some stress applied over a time interval to develop into a detectable defect.

As an example of the two types of defects, consider a resistor with the leads bent close to its body. If the stress imposed during bending caused the body to chip, this is a quality defect. However, had the stress been inadequate to chip the body, the defect would go unnoticed by conventional inspection. When the body is cycled through a temperature range, small cracks can develop in the body. This would allow moisture and other gases to contaminate the resistive element causing resistance changes. This is a reliability defect, R(t). This defect is also a design defect if the design specifications require a tight bend to fit the component properly in a board. If the improper bend is due to poor workmanship, the defect is classified as an induced defect.

Table 4-43 shows some of the processes involved in the manufacturing of an electronic assembly, and identifies some of the associated defects and resultant failure modes.

The operation and maintenance of equipment in normal field usage also induce defects. It has been shown that operators in the field will stress systems beyond the predicted levels either through neglect, unfamiliarity with the equipment, carelessness, or mission constraints. Also, maintenance, scheduled and unscheduled, degrades reliability. During unscheduled maintenance, good parts are replaced in an effort to locate the faulty parts. In many cases, the good parts are written up as defective instead of being reinstalled. These parts often are returned to depot for repair or discarded, resulting in a failure rate that is higher than is actually occurring. Scheduled maintenance can also introduce defects into satisfactory assemblies. These defects are due to:

- Foreign objects left in an assembly
- Bolts not tightened sufficiently or overtightened
- Dirt injection

Table 4-43 PRODUCTION PROCESS AND ASSOCIATED DEFECTS

General Process	Induced Defects	Failure Mode				
		Intermittent	Short Circuit	Open Circuit	Value Change	Noise
Wire Stripping	Nicked Lead			X		
	Broken Strands		X			
	Short Leads	X		X		X
	Long Leads		X			
Soldering	Excessive Heat			X	X	X
	Insufficient Heat	X		X		X
	Excessive Solder		X			X
	Insufficient Solder	X		X		X
Lead Cutting	Dull Tools (Shock)	X		X	X	X
Crimping	Wrong Tool	X		X	X	X
	Wrong Terminal		X			
	Low Force			X		
	Excessive Force	X		X		
Wire Wrapping	Broken Wire			X		
	Loose Connection	X		X		X
Lead Bending	Stress on Case	X	X		X	X
Wire Dress	Vibration Sensitivity	X	X	X		X
	Residual Stress	X	X	X		X

- Parts replaced improperly
- Improper lubricant installed.

These induced defects and operational stresses, along with the influence of the environment, are factors that must be controlled and accounted for in the analysis of reliability. In general, the environmental factor considered in handbook prediction techniques accounts for the added stress provided by operation within that environment. However, the environmental stresses imposed during maintenance may be other than what was anticipated during prediction. For instance, a subassembly removed for repair in a desert area may be placed in direct sunlight while awaiting transfer. Component temperatures may exceed those experienced during normal operation for extended periods, thus reducing their life expectancy. Mechanical stresses imposed on components during removal, repair and reinsertion may exceed that designed for a given environment. Therefore, all maintenance procedures should be evaluated and controlled to minimize maintenance induced defects.

Reliability degradation control involves concepts related to inspection--frequency of, type, location and efficiency. A key facet of reliability degradation control is the determination of the efficiency of inspections--incoming, production, final and field inspections. It should be recognized that no inspection procedure is perfect. The possibility or the probability of an error in an inspection procedure is a function of a number of factors, some of which are:

(a) Probability that all component functions are exercised by the test performed.

(b) Reliability and calibration of test fixture and equipment.

(c) Probability of inspector error.

(d) Complexity of item inspected.

(e) Inspection instructions, criteria, etc.

The efficiency of an inspection can be expressed as a probability of detecting a defect and will have a numerical value between 0 and 1. A perfect or error-free inspection would have an associated numeric value of 1. The inspection efficiency may also be expressed as a percentage.

The factors which influence inspection efficiency can be expressed as probabilities which are the tools for calculating the detection of a defect. As an example, assume there are four (4) independent factors which influence a particular inspection. Further assume that the probability of each factor is (0.9). Then the probability of inspection (i.e., inspecting efficiency) is $(0.9)^4$ or about (0.66). Thus, even though the probability of each factor is relatively high, the collective probability or the inspection efficiency is relatively low. This illustrates the difficulty of obtaining a perfect inspection.

As previously discussed, conventional inspections are designed to remove quality defects; however, since inspections are not perfect, all quality defects will not be removed. Figure 4-72 is an example of how inspections can be used to reduce the number of quality defects in a component.

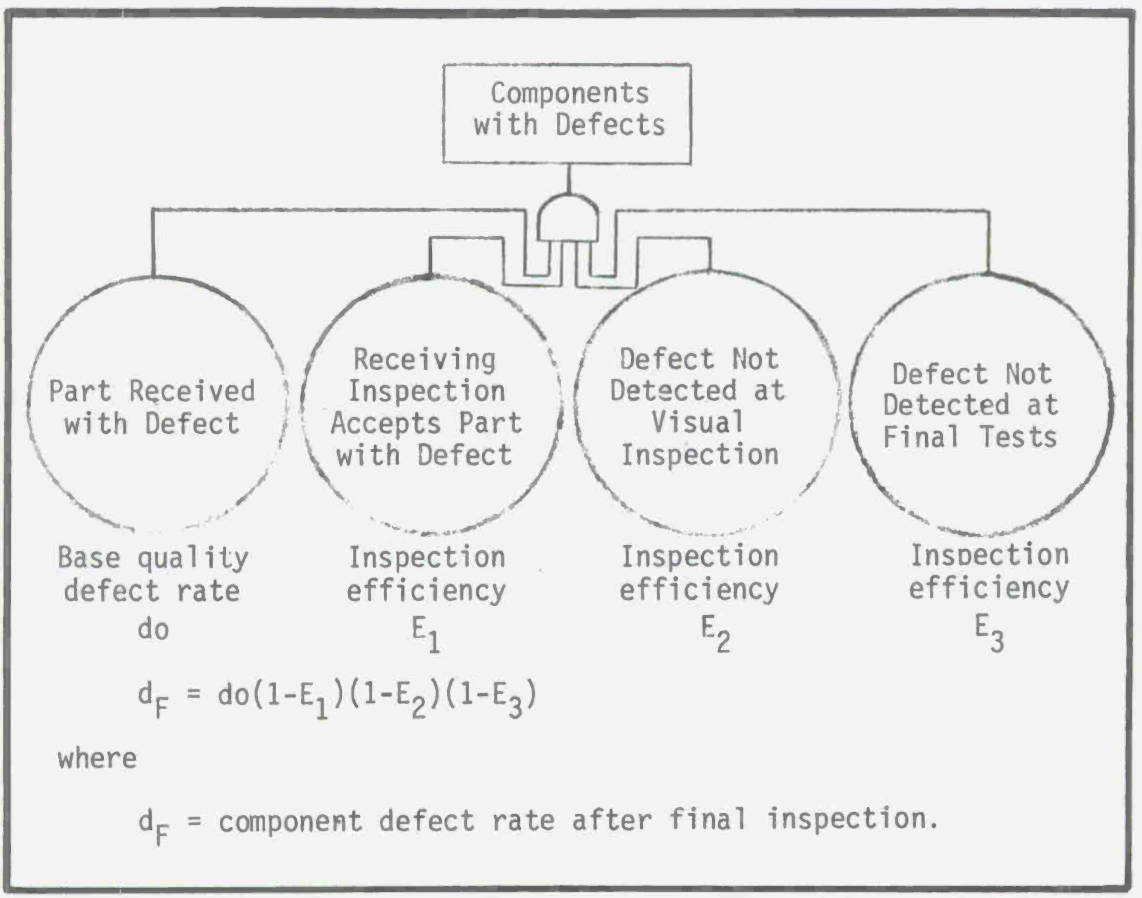


Figure 4-72 FAULT TREE DIAGRAM FOR QUALITY DEFECTS

Even though an individual inspection is not perfect, a sequence of inspections can insure a small number of outgoing defects. This can be seen from the above fault tree diagram which shows that for an outgoing component to contain a defect, the occurrence of all four of the following events are required.

(a) Part received with a defect

(b) Receiving inspection accepts part with a defect

(c) Defect not detected at in-process inspection

(d) Defect not detected at final test station.

It should also be noted that if any of the inspections of the example were perfect ($E_n = 1$), there would be no outgoing components with defects.

A burn-in or screen test is included in the inspection of many electronic equipments. This type of test is designed to convert reliability defects which will cause premature failures in the field into failures in the assembly plant. This results in a lowered infant mortality rate of the system immediately after production. The screen efficiency, S, is the probabiliy of converting a reliability defect into an observable failure. The number of reliability defects converted and detected is the product of the number of incoming reliability defects, the screen efficiency, and the inspection efficiency. If the screen efficiency is (0.9) and the inspection is (0.9), then the probability of converting and detecting a reliability defect is (0.81). Thus, even with the use of a screen, all of the induced reliability defects will not be detected and removed.

To assess and control the reliability of a system as it leaves production or a field maintenance activity, values for inherent quality and reliability defect rates, induced quality and reliability defect rates, and inspection/screening efficiencies must be determined by a process and inspection analysis.

The process and inspection analysis involves: (1) a determination of the induced defects (quality and latent reliability) associated with each of the more significant steps required in the fabrication of the system as planned--based on an analysis of planned inspection criteria

and historical rejection rates derived from similar processes; (2) an assessment of the total outgoing (from production) defect rate based on the derived process-induced defects and supplied inspection reject rates; and (3) a calculation, based on the ratio of the inherent reliability to the outgoing reliability.

Values for process or maintenance induced defect rates can be derived from an evaluation of reject statistics, determined from an evaluation of stresses applied by the manufacturing processes, or can be based on experience factors with similar systems and processes. The values derived or obtained for reject rates, induced defect rates, and inspection and screen efficiencies can be combined in a process and inspection analysis flow chart which is used to derive a final outgoing defect rate. The total defect rate or outgoing reliability numeric stemming from a process analysis can then be used to determine manufacturing reliability degradation factors.

4.2.2 Design for Ease of Inspection and Maintenance

As previously indicated, achieving high reliability is directly related to the degree of effectiveness of the special features designed and built into a system which would make it easy to produce (i.e., assemble and test) and maintain. These features must be designed with the objective of aiding the production inspector or maintenance technician in recognizing and diagnosing failures or weak areas and making a repair as early and as rapidly as possible. Furthermore, the incorporation of these special features into a system, in addition to improving reliability, producibility and maintainability, will result in a reduction of manufacturing and field support cost.

In order to effectively design for ease of inspection and maintenance, the designer must be completely aware of basic problems and marginal or difficult areas related to assembly and maintenance. He must be aware of possible equipment failure modes connected with these problem areas, and he must be completely familiar with the production and maintenance environment. The designer must recognize that production problems are potential maintenance problems, e.g., if assembly is difficult under factory conditions, it would be virtually impossible under field conditions.

Achieving ease of inspection and maintenance requires designing special means into the system for: (1) identifying failure and/or potential (or marginal) failures, and (2) facilitating fault diagnosis (e.g., access to failed units and removal and replacement of failed units). Table 4-44 presents a simplified list of activities and development guidelines that will aid in assuring implementation of these features.

Although implementing these features involves essentially all aspects of equipment development, concepts relative to hardware partitioning (i.e., packaging, modularity, etc.), fault diagnosis and detection of incipient failures are considered key elements. The following subsection provides information about and guidelines for these three elements.

4.2.2.1 Hardware Partitioning

Hardware partitioning is the process of dividing the system into physically and functionally distinct units to facilitate fault isolation, removal and replacement. Partitioning enables equipment units, assemblies and subassemblies to be designed as discrete items or modules.

Modularization affects both maintainability and producibility as indicated in Figure 4-73.

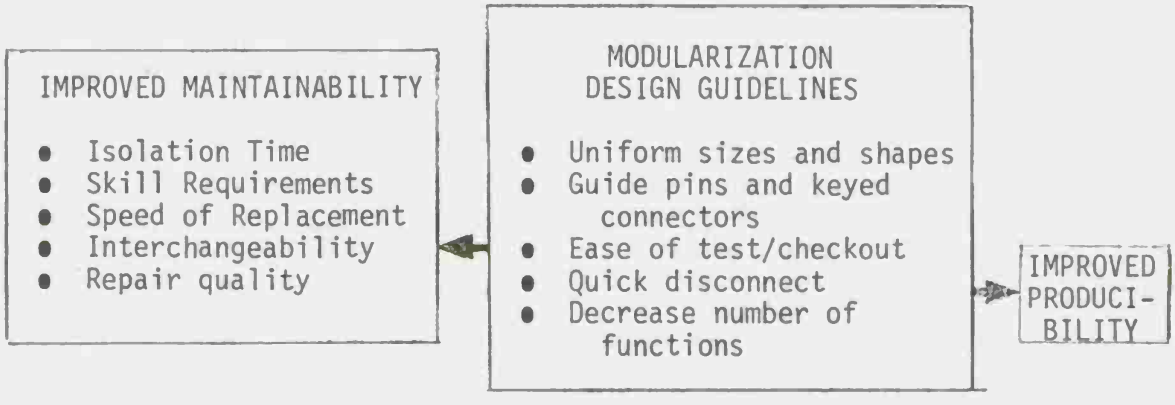


Figure 4-73 MODULARIZATION DESIGN

Table 4-44 EASE OF MAINTENANCE GUIDELINES

Failure diagnosis, identification and replacement are facilitated by:

- Using modular design techniques
- Use of special built-in circuits for fault detection, error warning lights, etc.
- Designing for replacement at higher levels
- Using increased skill level technicians
- Increasing depth of penetration of localization features
- Utilizing test indications which are less time consuming and/or less difficult to interpret
- Designing for minimum diagnostic strategies
- Making accessible and obvious both the purpose of the test points and their relationship to the item tested
- Improving quality of technical manuals or maintenance aids
- Designing access for ease of entry
- Reducing number of access barriers
- Reducing need for isolation access by bringing test point, controls and displays out to accessible locations
- Reducing number of interconnections per replaceable item
- Using plug-in elements
- Reducing requirements for special tools.

Modularization is achieved through functional design which encompasses the packaging of components and subassemblies performing similar functions in self-contained units, thus facilitating testing and maintenance.

The application of modular design allows the isolation of faults to a unit which may be removed from the equipment for on-site repair, shipment to a repair depot or throwaway. The equipment may be immediately put back into operation by replacement of a spare modules, minimizing on-line maintenance action. Localization of components into modules eliminates long paths and crossovers, as illustrated in Figure 4-74.[40] This further enhances ease of maintenance by simplifying the tracing of signal paths when locating and isolating a failure.

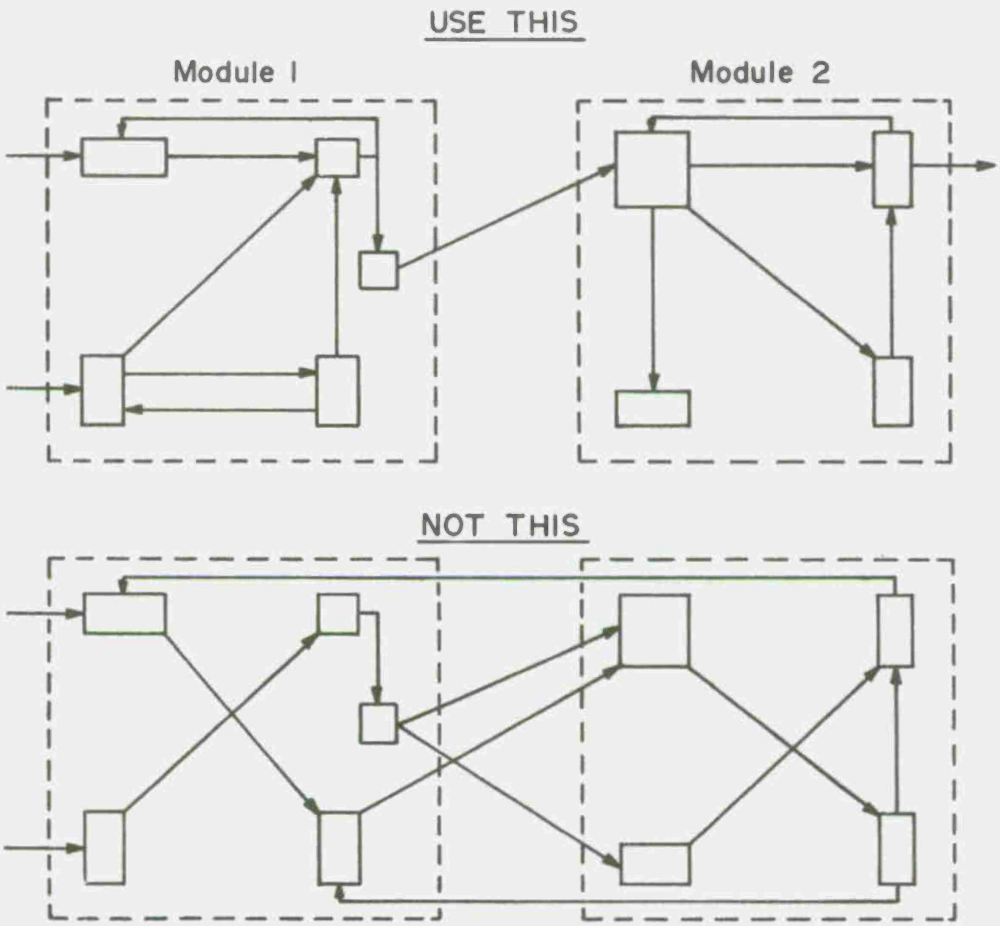


Fig. 4-74 DESIGN FOR FUNCTIONAL MODULARIZATION

An example of modularization currently used in airborne systems design is the line replaceable unit (LRU). The LRU concept allows the rapid removal and replacement of large equipment modules or subsystems on the flight line for maintenance at a repair station. The application of this concept allows reduction of fault isolation time, reduction of on-line maintenance personnel skill requirements and provides for consistent quality of repair.

If the module is inexpensive and not used in great numbers, there is a strong likelihood of adopting a throwaway maintenance concept for the module. This is a logical conclusion of a cost of ownership analysis (COO) (see Section 4.3) indicating that repair costs are greater than the cost of a new unit. The logistics of module replacement are directly related to the initial design decisions on size and complexity of modules. Repair of equipment can be accomplished by replacement of a module after fault isolation is accomplished by some portable test equipment or built-in test, but the repair of a module generally requires jigs, fixtures, power supplies, etc.

This equipment is ordinarily found at the production plant to enable rework of these modules. However, it is generally too expensive for field application. Along with the training and technical orders required for field repair of a module, there are the cost factors which must be considered. Further details on the logistical aspects can be obtained from the APLCM/AFSCM 800-4 manual on Optimum Repair Level Analysis (ORLA).

Based on costs and logistics, a design trade-off must be made, in the concept formulation stage, to design small inexpensive modules which will be designated throwaway or to design larger modules for a possible economy of equipment repair. It is crucial that these decisions be made early in the concept phase where changes least affect program costs.

An equipment which implements the throwaway concept of modular design possesses several advantages. Throwaway modules allow savings in repair time, tools, facilities and manpower. They also allow improved standardization and interchangeability of modules and assemblies. Throwaway modules also impose several penalties. They increase supply burdens because modules must always be on hand. Similarly, redesign or retrofit of manufactured units becomes difficult since modules cannot be readily modified.

If a module can be cost effectively thrown away, the trouble shooting and repair aids in the module can be eliminated, providing the module can still be readily isolated. In this case, it should be remembered that an expensive part should not be discarded with an inexpensive but failure prone part. In the case of an inexpensive module containing an expensive part (30% of module cost), a plug-in connection allowing salvage of the expensive part may be considered.

4.2.2.2 Fault Diagnosis

It must be emphasized that a system's ease of maintenance depends on those design features which impact the ability to diagnose failure rapidly and accurately. Repair cannot begin until the failure is identified, located and isolated. Consideration of fault diagnostics during equipment design can significantly increase ease of maintenance by reducing diagnostic time and, therefore, equipment downtime. Design factors contributing to rapid fault diagnosis are:

- Built-in Test Provisions
- Maintenance Support

Special provisions must be designed into the system that will provide the means to assess the condition of internal LRU's, assemblies, or modules, for the prupose of locating failures. Such provisions can have a wide range of complexity, depending on the needs and constraints of the specific system. Some systems may simply provide test points to interface with external support equipment. Other systems may incorporate Built-in-Test-Equipment (BITE) or sophisticated Built-in-Test (BIT) which operate under computer control and provide complete indication of failure.

Built-in test provisions obviously influence inspection and maintenance cost. From the maintenance viewpoint, maximizing fault isolation is the most desirable approach. However, a number of difficulties arise. Built-in test provisions add cost to the equipment's development. Thus, the extent of the provisions must be determined through trade-off studies concerning maintenance needs and total cost of ownership. The trade-off between acquisition costs and potential maintenance savings must be evaluated to determine the impact. Other factors may influence the decision, such as: short downtime requirement, criticality of the item, or personnel requirements.

Incorporating test points into the system involves considering number, type, location and arrangement. The physical location of the test points has a marked effect on the quality of inspection and maintenance. Generally, test points should be located near the signal source, since the nature of a signal may be such that it does not travel well without being altered in the process of transmission. This consideration is particularly pertinent in those cases where the waveshape of the signal is critical and will tend to change in transmission to a test point. The designer should keep in mind that the technician needs only an indication that reflects an out-of-tolerance condition of the true signal. If these indications are documented during engineering tests, they will provide adequate malfunction indicators for field use.

Particular care should be taken to make test points accessible. Ideally, internal test points should be clustered around the portion of the unit that will be most accessible when installed. There should be only one adjustment control associated with each test point and it should be easily and reliably operated.

Test points should be grouped or arrayed on a central panel to facilitate checking and troubleshooting. The test points should be grouped in an orderly fashion which is convenient for sequential checking. The specific test points to be employed in an electronic system depend on the operational and tactical demand placed on the system design, and the special needs of a particular service. The number and type of test points should be compatible with test instrumentation (built-in or otherwise) that is available at the place of system use, or at the maintenance or repair activity.

The functional location of test points should be fixed by determining from the manufacturing inspection requirements and the maintenance procedures during what signals must be available to the technician and at what points they must be available. Test points should make available those signals that the procedures indicate the technician must have in order to inspect and maintain the system. Their location must be planned into the system for maximum effectiveness.

A test point (which may be nothing more than a bare wire) should be provided at the input and output for each line replaceable unit. One convenient way to provide these test points is to mount components on one side of a board and wiring on the other side with electrical connection through the board. The advantage of having test points alone on a flat surface rather than in among the parts is that full identifying information for each test point can be stamped on the surface without being obscured by the parts.

It should not be necessary to remove any assembly from a major component to inspect or troubleshoot that assembly. This may require special test points on the major components or assemblies. But test equipment and bench mockup access to the outputs and inputs of each line replaceable unit should be provided through the normal interconnecting plugs wherever possible. Design guidelines for test points in electronic equipment are listed in Table 4-45.

The decision to include BITE/BIT must be based on a trade-off between basic maintenance factors and other system parameters and constraints. Built-in test capabilities have three uses at field level:

- Warning that subsystem has become inoperative
- Generating failure signals to reconfigure system
- Fault isolation to a replaceable element.

The difficulties of applying BITE/BIT are:

- Changes in hardware (modifications or additions to the system) require BIT hardware/software modifications.
- Information transfer between systems with BIT is greater than without BIT.
- Systems BIT is normally designed by system integrators who are not as familiar with the system as the original designers.
- Centralized BIT requires increased data input and more elaborate logic.

Table 4-45 DESIGN GUIDELINES FOR TEST POINTS

1. Test points should be provided for the input and output of each line replaceable or repairable assembly, circuit, item or unit; these points should be immediately available.
2. Ground points should be provided as necessary, particularly when a painted surface would otherwise prevent good electrical contact.
3. Voltage dividers should be incorporated at test points for voltage in excess of 300 volts.
4. Test points and their associated labels and controls should face the technician for best visibility, consider use of color coded test points for each of location.
5. Combine test points, where feasible, into clusters for multipronged connectors, particularly where similar clusters occur frequently.
6. Arrange test points in a test panel or other surfaces according to the following criteria, listed in order of priority:
   a) The type of test equipment to be employed at each point
   b) The type of connector used and the clearance it requires
   c) The function to which each point is related
   d) The test routines in which each point will be used
   e) The order in which each will be used.
7. Label each test point with the tolerance limits of the signal, and a number, letter or other symbol keyed to the maintenance instructions.
8. Locate routine test points so that they can be used without removal of cabinet cover or chassis.
9. Label each test point with the in-tolerance signal.

In general, built-in tests perform fault isolation by applying a signal to a circuit and measuring its response by primary measurements such as voltage levels, distortion, noise, etc. Meters or go/no-go test equipment are built into the circuit so that a minimum of external test equipment need be connected to test the circuit performance. Checkout is normally performed manually by applying stimulus and observing the response of the circuit by BITE. The output can be fed to a computer which determines if all measured parameters are within limits. The computer can also generate the necessary test signals. BITE, in addition to reducing the mean time to repair a failure (MTTR), also lowers the skill level needed to maintain equipment because fault isolation is performed by a computer and the technician need only replace the component identified by the computer.

To determine BITE sophistication, it is necessary to define the requirements for MTTR, number of parameters tested, criticality of malfunction, and level of maintenance personnel. For instance, aircraft operating in battle conditions pose severe restraints on the time permitted for a system check. In a combat situation, aircraft are recycled as rapidly as possible because of the limited time between missions and shortened preflight checkout. Therefore, the MTTR should be minimal, e.g., one hour or less. Due to the complexity of the avionics equipment, many parameters need to be tested to insure mission success. Even with skilled technicians, the time required to remove panels to get at test points is prohibitive. Therefore, some form of BITE is necessary, and the more complete the testing performed, the higher the likelihood of finding critical malfunctions. If the aircraft were to have a computer on board, the computer could cycle the avionics through a complete test while returning from a mission when the computer burden is low. All necessary parameters could either be printed out for a semiskilled technician to evaluate for conformance to specification, or the computer could perform this function as well as identify any defective avionics modules.

An example with opposing requirements is a central communication network having redundant equipment. In this case, a few voltage current and/or power meters located at the output of large subassemblies in the network BITE would allow an operator to isolate a malfunctioning

subassembly quickly. The backup unit would be switched on and, once the defective subassembly is disconnected, the defective component can be identified and repaired at a less demanding pace. The degree of BITE used in this example would depend upon the skill level of the technician.

A very important consideration when implementing BITE is the manner in which it affects the circuit. Ideally, it should look like an open circuit at all times under all failure modes in the control circuit. In this way, the built-in test provision will not decrease the circuit reliability. Since this is not always possible or practical, its loading effects should be evaluated in the operation of a circuit. Circuit operation should be studied to determine if there is another location in the circuit where a similar measurement might provide as much and possibly more information with less loading. A failure mode and effect study should be performed on the BITE to determine the impact of various failures on the operation of the circuit under test. Those failure modes causing lowered performance of the circuit under test should be eliminated by a different test technique or by improving reliability using techniques described in Section 4.1 of this handbook.

The system to be maintained should be fully described by the designer. Schematic diagrams of new or unusual circuits should be provided. Equipments to be tested should be broken down into functional block diagrams, and engineering sketches and diagrams should be provided to identify modules and test points. Modules and test points should be labeled or coded to facilitate identification from documentation. The testing procedure should be documented in a clear, concise manner and expected signal levels and waveforms adequately indicated.

The designer should also prepare a technical description of proposed test or support equipment which must be available to maintain the equipment. If the test or support equipment is government furnished, the nomenclature of the equipment should be identified. However, if the test or support equipment for maintaining the equipment is commercial, the designer should list the name of the supplier and catalog number of the commercially available equipment. A statement should be furnished, and preferred and alternate devices should be indicated if there is more than one suitable test or support equipment available. It should be stated whether the proposed test is built into the equipment.

4.2.2.3 Prediction of Incipient Failure

Often, components require many hours of operation before they degrade to the point that the circuit in which they are installed ceases to operate adequately. For the components degrading at a slow rate, life prognosis, or failure prediction, allows scheduling of preventive maintenance in a timely manner for most efficient use of maintenance personnel, increased MTBF, and maximum equipment availability. However, the penalty that must be paid for these advantages is more frequent status measurements involving detailed data on the signal levels present throughout a circuit. This data is compared with predetermined data limits to validate circuit failure or proper operation. Data taken for life prognosis must be stored for comparison to future data. By comparing data from several such groups, data degradation trends can be identified, the degraded part located, and the expected lifetime predicted. The classic way of obtaining data, i.e., a technician taking data at many locations in the circuit, is expensive and prohibitively time consuming. The current approach, which expedites data collection, is to use Built-in-Test Equipment, BITE, which simplifies data taking or Built-in-Tests, BIT, which can obtain these data under computer control. Another approach that can be useful is to measure secondary effects, such as component temperature and electric and magnetic field gradients, around a circuit board or subassembly.

Secondary effects are defined as those effects which are not produced solely from the signal processing. Examples of such effects are: the heating of a component due to current flow rectification, or mixing of an ac signal(s) at the junction of a bipolar transistor due to its nonlinear characteristics, and odor emitted from a component due to current flow. A broad background in physical effects associated with component operation physics, as well as state-of-the-art detection techniques, are needed in order to fully exploit secondary effects. This section will provide only an insight into this subject since a complete discussion is beyond the scope of this handbook. Some references for both mechanical and electrical systems are provided at the conclusion.

Secondary effects can be subdivided into passive or active categories. Passive effects were used as examples in the preceding paragraph, i.e., a sensor monitors the effects of the operating system without

providing any stimulus other than what is normally present. The second example could also be an active technique if an external RF field were imposed on a bipolar transistor. The nonlinear conductivity would cause a signal to be reradiated from the transistor with an AM component proportional to the signal being processed by the transistor. An active effect is, therefore, one utilizing external stimulus. Secondary effects can be further categorized into chemical, mechanical and electromagnetic. The fields covered in each of these categories are presented in Table 4-46.

The feasibility of sensing secondary effects has been demonstrated and is applied with varying degrees of success through the industry. Secondary effects sensing has not been widely accepted because the signals obtained from them are complex and difficult to interpret. In general, the secondary effect created by a component is not uniquely characterized by a single response in the electromagnetic, mechanical or chemical domain and, therefore, requires the use of different types of sensors for any inspection.

The secondary effects may best be described as "signatures". This signature may be characterized in the time domain, the frequency domain, or in the case of chemical signatures, the molecular weight, partition coefficients, or size distribution. The environment must also be considered as having a signature characterized in terms of a particular sensory system.

Normal signatures as well as signatures of an incipient or actual failure may vary slightly from equipment to equipment because of nominal differences in components and assembly. Failure signatures may, in some cases, tend to be masked by variations in the environmental signatures. There are several possible ways that the environmental factors may be negated. The unit under test can be placed in a controlled environment or otherwise shielded from its effects. Improved sensors can, with spatial resolution, improve the signal to environment ratio by cancelling the environmental signature. The improvements in data processors (minicomputers, digital fast Fourier transform, etc.) make it possible to subtract steady-state environmental contributions if they remain constant or change slowly.

Table 4-46 CAUSE AND EFFECT OF SECONDARY EFFECTS

Secondary Effect Sensed	Source of Effect
Electrical	
Infrared	Power Dissipation
	Transistor heating
	Resistor heating
	Display heating
	Capacitor heating
	Connector heating
Microwave	Poor connector
	Noisy transistors
	Transistor nonlinearity
High Frequency	Oscillating current in coils
	Poor connection
	Insufficient by-pass cap
Electric Field	AC and DC voltage gradients
Magnetic Field	AC and DC currents
Mechanical	
Noise	Conductor vibration
	Poor electrical connection (arcing)
	Loose component
Heat	Power dissipation components
	Poor connection
	Friction
Chemical	
Odors	Overheating Arcing
Particles	Overheating Arcing

Secondary effect monitoring meets the ideal criteria for BITE/BIT sensors because they do not load the circuit under test, and, if they should fail, the operation of the circuit is unaffected. The sensors are, in general, more expensive than BITE/BIT but they can supply supplemental diagnostic data which might otherwise be difficult to obtain by conventional BITE techniques.

SECTION 4.3

DESIGN TO COST

4.3 Design to Cost

Currently, design to cost goals are used in contracts to seek the best balance between performance and acquisition cost in most defense systems programs. The decision to emphasize cost goals was made in the light of the hard realities of likely future levels of DoD budgets and the ever increasing unit acquisition, manpower and support cost.[48] Although design to cost is not a unique concept, it does represent a constraint to add to the task of designing equipment which will meet performance, reliability, maintainability, and now, cost goals. Of course, the true objective of the design effort is to achieve a balanced design that will meet all requirements. In this section of the handbook, we will treat the seemingly simple task of achieving the "balanced" design. Specifically, we will discuss:

(a) The "design-to-cost" philosophy,

(b) Procedures for allocating broad contractual goals to the subsystem and component level, and

(c) Techniques which can be used to meet cost goals.

4.3.1 Design to Cost Overview

An understanding of the rationale and background for the design to cost philosophy will aid in the application of these principles. Design to cost evolved after studies of past program cost trends revealed that the military would not be able to replace equipment at the same rate at which present equipment was becoming obsolete. A clearer understanding of the dilemma is possible by reviewing the DoD resource allocation process.

DoD Resource Allocation Process

DoD planners did not see a real growth in the portion of the federal budget allocated for military needs. A fixed inflow of funds is shown in Figure 4-75. Due to the increased complexity of today's equipment, a larger portion of the budget was projected to be allocated to: 1) operating and maintenance needs, and 2) manpower requirements. The procurement budget for new replacement equipment was expected to remain constant, at best. It was obvious that steps would have to be taken to restrict cost (in most cases, unit production cost) to past levels of

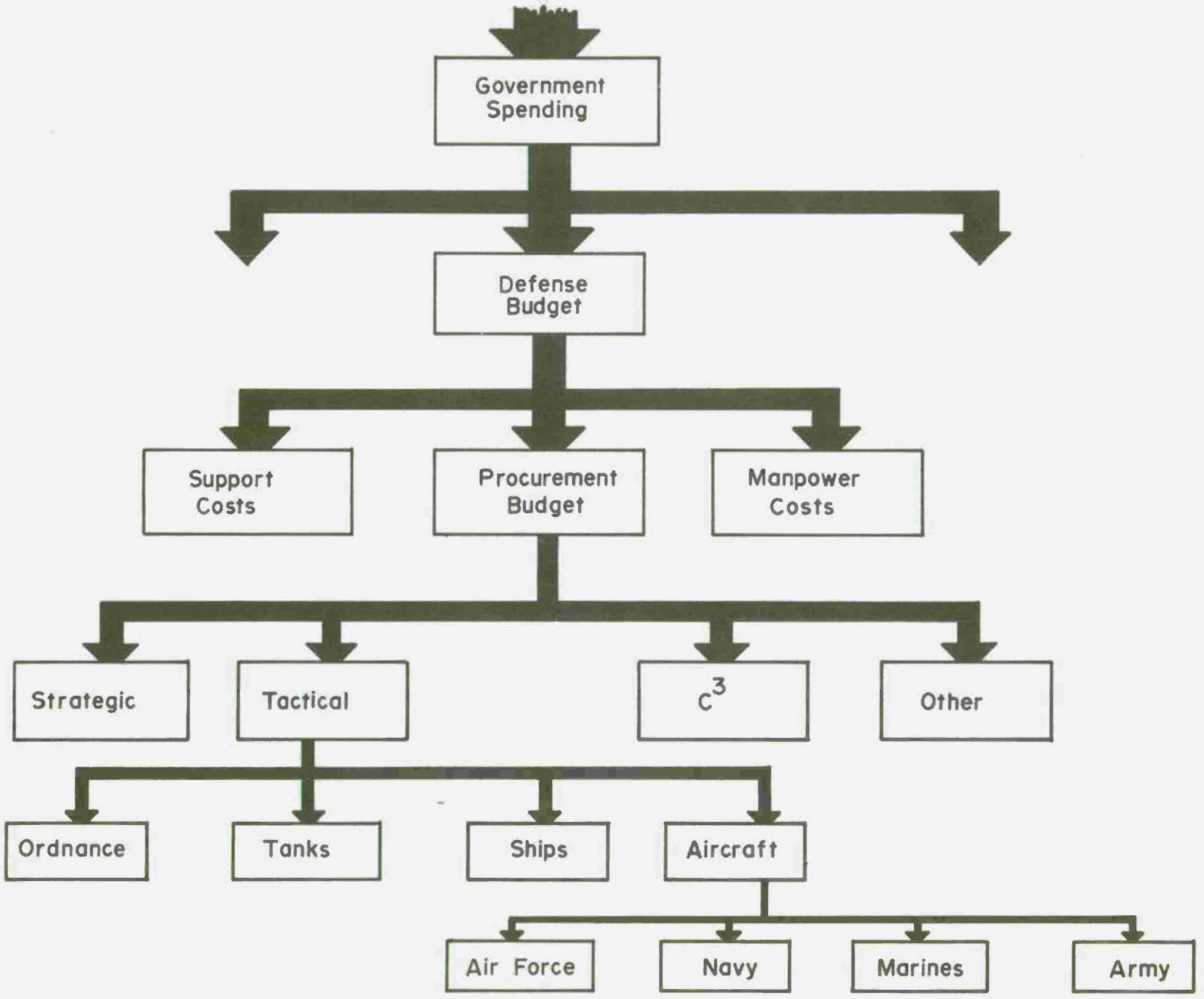


Fig. 4-75 THE DOD RESOURCE ALLOCATION PROCESS

equipment unit cost in order to provide equivalent force structures. Design to cost was instituted precisely to achieve this end. It was also intended to slow the trend toward increased performance without regard to cost, reliability and complexity of the new equipment.

Design to cost could take different emphases dependent on the type of development program. Four programs[44] with varying design to cost emphasis are defined in Table 4-47. As seen in the table, "Design-to-Unit-Production-Cost" (DTUPC) is emphasized in most major military programs. DTUPC can determine the number of aircraft or equipment the military could "afford".

Table 4-47 TYPES OF DESIGN-TO-COST PROGRAMS

Design to Cost Programs	Program Characteristics	Program Examples
Production Unit Price	Large Quantity Procurements	• Close Support Aircraft A-10 • Lightweight Fighter
Total Program Costs	• Complex Equipment • Small Buys • High Development Cost	• AWACS • Advanced Airborne Command Post
Production Unit Cost and Installation Cost	• Large Quantity Procurement of Subsystems	• Airborne Radar • Avionics Equipment • TACAN • Gyroscope
Development and Operating Costs	Facilities and Construction Programs	• Ground Radar Installations

Despite the emphasis on unit production cost in contractual requirements, the overriding objective is to minimize the life cycle costs--design to unit production cost is only an aid in the process. A major component of life cycle cost is support cost. A quick review of Figure 4-75 illustrates the importance of minimizing support cost. If support

costs are compromised when meeting DTUPC goals, future funds for equipment procurement are further reduced.

What this means is that during design one must strive for a balanced design which will:

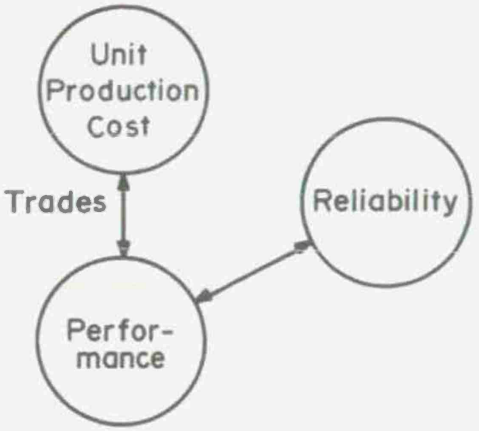
(a) Maximize performance within unit cost goals, and
(b) Minimize support cost, to minimize life cycle costs.

A design that minimizes support cost involves the application of reliability disciplines during the design phase. The practitioner who embraces reliability fundamentals in equipment design is actually incorporating sound economic principles which will lead to the lowest cost to the owner.

Figure 4-76 illustrates the relationship between objectives of a design program. In the past, the emphasis on performance would often become overriding, to the detriment of reliability and cost considerations. Design engineers must now balance performance, reliability and unit production goals equally against the overall objective of minimizing life cycle costs.

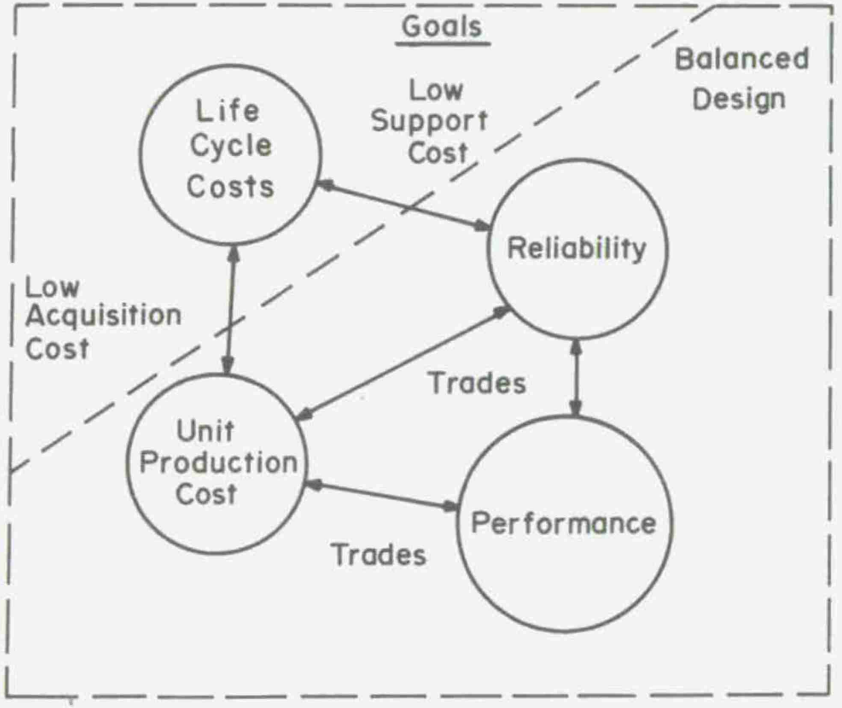
To meet this need, attention is focused on structuring a balanced design approach derived from a life cycle cost model that is composed of, and governed by, submodels which calculate R&M and cost variables. Figure 4-77 presents an overview of the methodology within this framework. The figure shows the life cycle cost model as the vehicle by which estimates for operation, performance, R, M, and cost are traded off to obtain "design to" target goals which collectively represent a balanced design. This life cycle cost model includes submodels which are representative of acquisition costs and logistics support costs, subject to the constraints of functional objectives and minimal performance requirements.

Life cycle cost represents all costs incurred from the point at which the decision is made to acquire a system, through operational life and eventual disposal of the system. A variety of analytical approaches can be used as inputs to the establishment of an optimum life cycle cost model. The total life cycle cost model is thus composed of subsets of cost models which are then exercised during trade-off studies. These



- Low Reliability
- Better Performance

Old



New

Fig. 4-76 TRADE RELATIONS BETWEEN PROGRAM OBJECTIVES (BALANCED DESIGN)

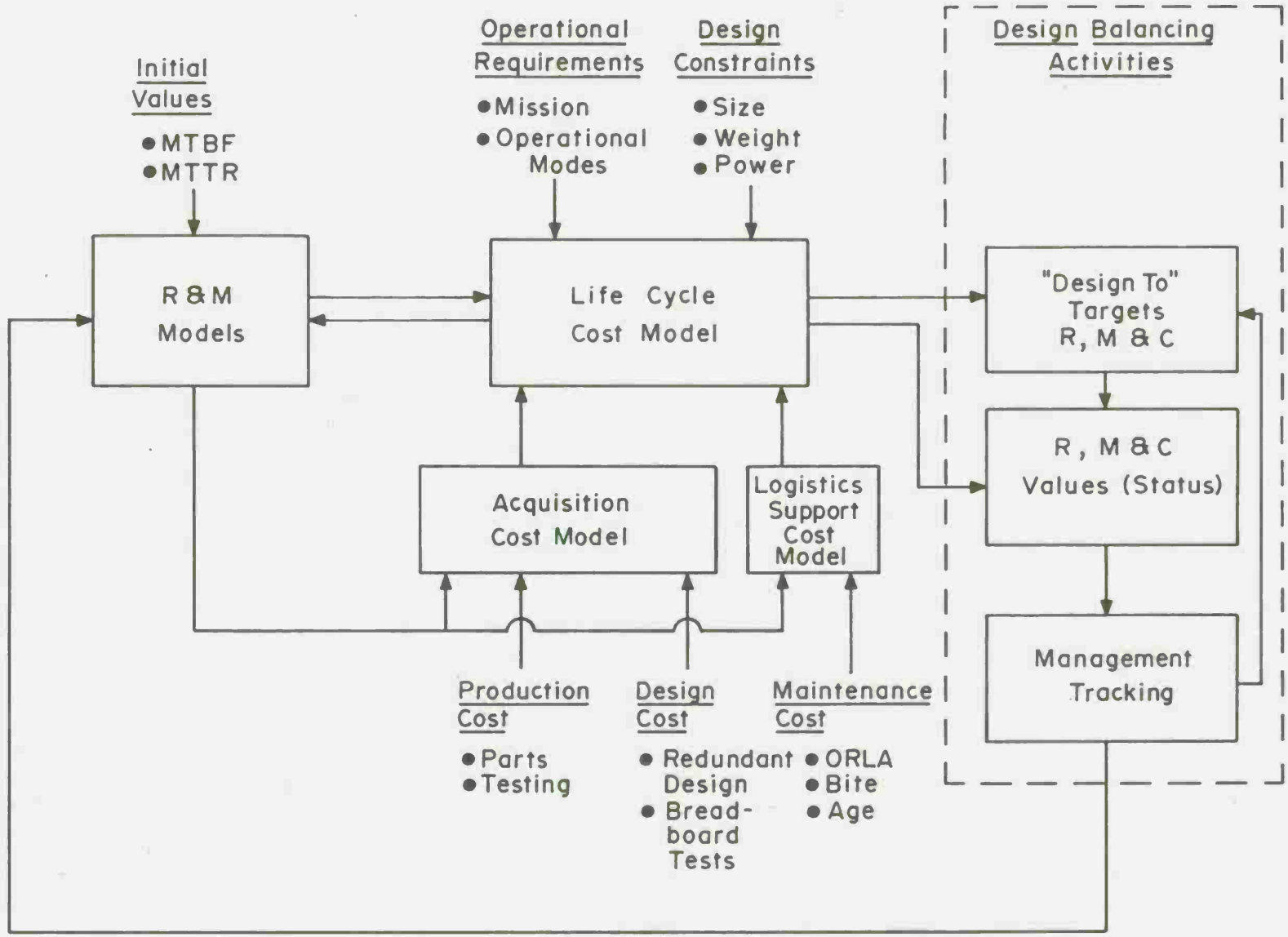


Fig. 4-77 R&M AND COST METHODS

cost models and cost estimating relationships range from simple informal relationships to complex mathematical statements derived from empirical data.

A total life cycle cost (LCC) is represented by costs collected in two areas: (1) system acquisition costs, and (2) logistics and support costs. In simple mathematical terms, the above can be stated by:

LCC = AC + LSC

where

LCC = life cycle cost

AC = acquisition cost

LSC = logistic support cost

Some of the major elements comprising these cost categories are shown below:

Acquisition (AC)

Design and development

- Basic engineering
- Test and evaluation
- Experimental tooling
- System management

Manufacturing and quality engineering

Fabrication

Production tooling

Quality control

Test equipment

Facilities

Initial spares

Training

Logistics and Support (LSC)

- Spares
- Personnel and training
- Overhaul and lower echelon maintenance facilities
- Aerospace ground equipment (AGE)
- Logistics factors

LCC models have been formulated which establish relationships to controllable AC and LSC characteristics. To obtain AC cost estimates for design and development, detailed engineering costs as well as statistical cost relationships (parametric sensitivity analyses) should be compiled and/or established. Obtaining this information necessitates a firm understanding of the equipment, its development and production processes, and a historical data base on similar type equipment. A few specific approaches which should be undertaken are: relating costs to measurements of technology over a given period of time, and using trend line parameters developed from the historical data base of similar equipments. The technological advance sought through the new equipment and the allotted development time can be used for gross estimating purposes.

In further estimating AC costs, production cost information is required. Production costs, in general, include material, labor, G&A, overhead, profit, capitalization for production, handling and transportation. Specific factors that comprise production costs are:

Recurring Production Costs

- Fabrication
- Assembly
- Test
- Manufacturing support
- Quality control
- Engineering support

Nonrecurring Costs

- Manufacturing engineering
- System integration
- Engineering changes
- Quality assurance

First article tests
Test equipment
Tooling
Facilities
Documentation

Program Management

Planning
Administration
Control

It should be noted that R&M can have a significant impact on production costs. Redundant systems can add to both system weight and cost. Use of established reliability components (per appropriate MIL-SPECS) and stringent quality control during production (e.g., equipment screening tests plus extensive subassembly testing) can also increase production cost. High quality parts which increase the design safety factors may be costly to procure and may also increase inspection costs. The cost factors associated with production test failures can be minimized if failure modes are eliminated during design, and if reliability defects are uncovered early in the production cycle. The factors that would reduce production costs, as reliability requirements are increased, include rework, material review board action (MRB), scrap rate and QC inspection.

The most complex cost estimating relationships are found in the logistics support cost area (LSC). For example, a logistics support cost model developed by the Air Force defines this factor in terms of eight equations as follows:

(1) Initial and pipeline spares cost
(2) Replacement spares cost
(3) On-equipment maintenance cost
(4) Off-equipment maintenance cost
(5) Inventory entry and supply management cost
(6) Support equipment cost
(7) Cost of personnel training and training equipment
(8) Cost of management and technical data.

The factors, elements and terms of these equations identify an incurred cost, time or expended resource in military field operations. The initial and pipeline spares cost illustrates the complexity and detail of the model.

This cost factor is defined in terms of (a) number of Line Replaceable or Repairable Units (LRU's) in the subsystem, (b) expected peak force flying hour/month, (c) fraction of maintenance actions for which the LRU or SRU (Small Replaceable Unit) can be repaired in place, (d) mean flying time between maintenance actions, (e) average base repair time, (f) fraction of removals returned to depot for repair, (g) expected total force flying hours over life cycle, (h) expected unit cost at the time of initial provisioning, (i) fraction of removals expected to be scrapped. Similar relationships exist for the other logistic cost factors.

A review of logistics support cost factors indicate that they are driven by system R&M characteristics. For example, when considering maintenance costs, the reliability of the system and its components, in terms of unscheduled maintenance frequencies and MTBF, directly impacts the frequency of repair and/or overhaul of failed components. Also, the higher the reliability, the lower the number of field modifications required and the lower the cost, including retrofit. Significant R&M expenditures during the development phase can be cost justified if improved field R&M performance and lower operating and maintenance will result from the R&M efforts.

In the Air Force LSC model, the functional modules of a system are called LRU's and the submodules are called SRU's. While the definitions of the LRU and SRU may differ somewhat, the definition as functional modules and submodules can be consistently applied.

The model provides costs per LRU and SRU and subtotals by equation, as well as totals and percentages by cost equation. It also lists the logistic support costs for each AGE item required to support the system. In addition, it separates fixed logistic support costs from costs sensitive to maintenance frequency. Thus, the model can determine the anticipated support costs of a given system configuration.

The model can determine the cost area which has the greatest impact on the overall cost. It can be used as a tool to optimize system cost--evaluating potential alternatives that meet design requirements. It can be used for parametric sensitivity analysis, determining the effects of varying parameter values on the cost of an LRU, SRU and total system, and aiding the identification and evaluation of risk and uncertainty factors. It can be used as a means of evaluating cost and performance target goals and as a vehicle to budget total cost of ownership by categories of costs on a continuing basis. Finally, it can be used to establish the discipline data bases that can be used for cost evaluation of other design configurations, as well as tracking the sensitive discipline parameters during the design to cost and balanced design phases.

4.3.2 Defining Cost and Reliability Targets

A full design to cost effort begins with the "requirements" process and continues through production. The application of design to cost goals in DoD contracts becomes firmer as the project approaches its production phase. Table 4-48 lists contract cost factors in a design to cost effort during the program phases.[44]

4.3.2.1 Concept and Validation Phase

During the conceptual phase, production costs, key support cost factors and equipment quantity relationships are derived and compared with "available" resources. These factors are iterated as primary parameters during the formulation of numerous essential performance requirements for the new system.

Resulting from this process are performance and reliability bands and a target unit production cost. The established cost goals can be validated and refined for use as primary design parameters, equal to performance in priority during full scale development.

The trade-off process during the concept and validation phases includes:

unit cost versus reliability
unit cost versus performance
reliability versus performance.

Table 4-48 HYPOTHETICAL DESIGN TO COST PROGRAM

Program Phase/ Cost Governing Factor	Concept and Validation	Full Scale Development	Production
1. Specification and Request for Proposal	Limited number of critical characteristics. Additional goals or features in terms of priorities.	Minimum performance features; no "how to" specifications.	Minimum use of military specifications.
2. Cost Goal	Variable (but defined) budgetary estimate.	Increasingly firm cost. Possible production price option.	Firm cost.
3. Cost Goal (support)	Life cycle cost or approximation (reliability or maintainability). Life cycle cost may be source selection criterion.	Same as concept or validation, but firmer base.	Perhaps warranty.
4. Contract	Cost type.	Cost type with possible production options.	Fixed price.
5. Incentives	Performance, reliability, maintainability, life cycle cost and, in some cases, production unit cost.	Production unit cost, life cycle cost.	Profit. Production unit cost goal. Possible maintenance warranty. Value engineering.

Issues of primary consideration during the trade-off process are: off-the-shelf requirements versus performance; complexity versus reliability; redundancy versus weight and volume penalties; and many others.

The "design to" concept has, as a fundamental philosophy, the notion that trade-offs can be made within the balanced design framework of the design to cost structure. Defining the limits for trade-off of R&M parameters is of a critical importance. The unit production price limits the cost of spares, the amount of built-in test equipment (BITE), and the level of functional reliability that can be designed into the system to meet the operational availability requirement. The operational scenario, along with unit level reliability, defines the expected number of system faults which will have to be serviced within the defined ownership costs. Required system availability further constrains reliability and establishes the maintenance and supply considerations that will have to be designed into the system. All these factors, and more, enter into the initial design trades if affordable systems are to be acquired. By setting a unit production price and designing to it, the BITE, redundancy, and maintenance concepts that can be utilized are automatically limited. The offsetting factors must be spares and manpower or availability.

Although only limited data is available in the early phases of the life cycle, the design to cost goal, as well as the minimal acceptable performance requirements, should be estimated as early as possible in the conceptual phase (through LCC studies as previously described). These estimates will have the primary purpose of providing visibility to management so that the design configuration may be adjusted to provide the most cost effective minimum within the constraints imposed and the balancing objectives for performance, reliability, etc.

As was mentioned previously, trade-offs would have to be made over the life cycle of the system. The cost trade-offs during the conceptual and early development phases will be made at a gross parametric level and will depend primarily on the contractor's historical support data. During these phases, operating and support costs, and research and development costs should be verified to support system design. However, this cannot be a true validation but only a verification of the cost driving parameters. For the most part, the significant factors will be reliability, modularization, fault isolation, sparing and manning.

Updated data banks must be used for estimating such parameters as unscheduled and scheduled maintenance manhours, AGE utilization and adequacy, technical manual adequacy, spare parts utilization, and diagnostic testing and training. During the development phase, submodule alternatives are still being considered and many of the required data elements are only estimates. That point at which a prototype is designed is the first point at which accurate module/submodule logistic and support cost estimates can be made. Trade-offs which should be made during this phase include test equipment versus maintenance manhours, reliability growth program costs versus spares requirements, maintenance manhours versus transportation and inventory cost to maintain spares pipelines. Cost targeting must be expanded to include requirements on the number of operating and maintenance personnel permitted, support equipment costs, the number of line items permitted to be entered into inventory, and on-equipment fault detection and isolation.

Throughout the entire life cycle in which the design to cost methodology is employed, the following two questions must be addressed:

(1) Is the latest design iteration meeting the performance and cost goals?

(2) Do alternative designs exist which further minimize the cost of ownership and enhance the performance characteristics?

Once a design has been chosen, trade-off analyses would then be very detailed and limited to such things as changes in part quality, redundancy, reliability goals for particular components and producibility methods. Thus, it is imperative that the initial analyses focus attention on high cost areas and develop alternatives to reduce the cost.

Figures 4-78 and 4-79 illustrate the relationship between reliability, maintainability and cost. Figure 4-78 shows that as a system is made more reliable, everything else being equal, the operation costs will decrease since there are fewer failures. At the same time, acquisition costs (both development and production) must be increased to attain the increased reliability. At some point, each acquisition dollar spent on increasing reliability will result in exactly a dollar saved in operating costs. This point represents the reliability for which total costs are minimum. Note that there are steps in attaining reliability which are of

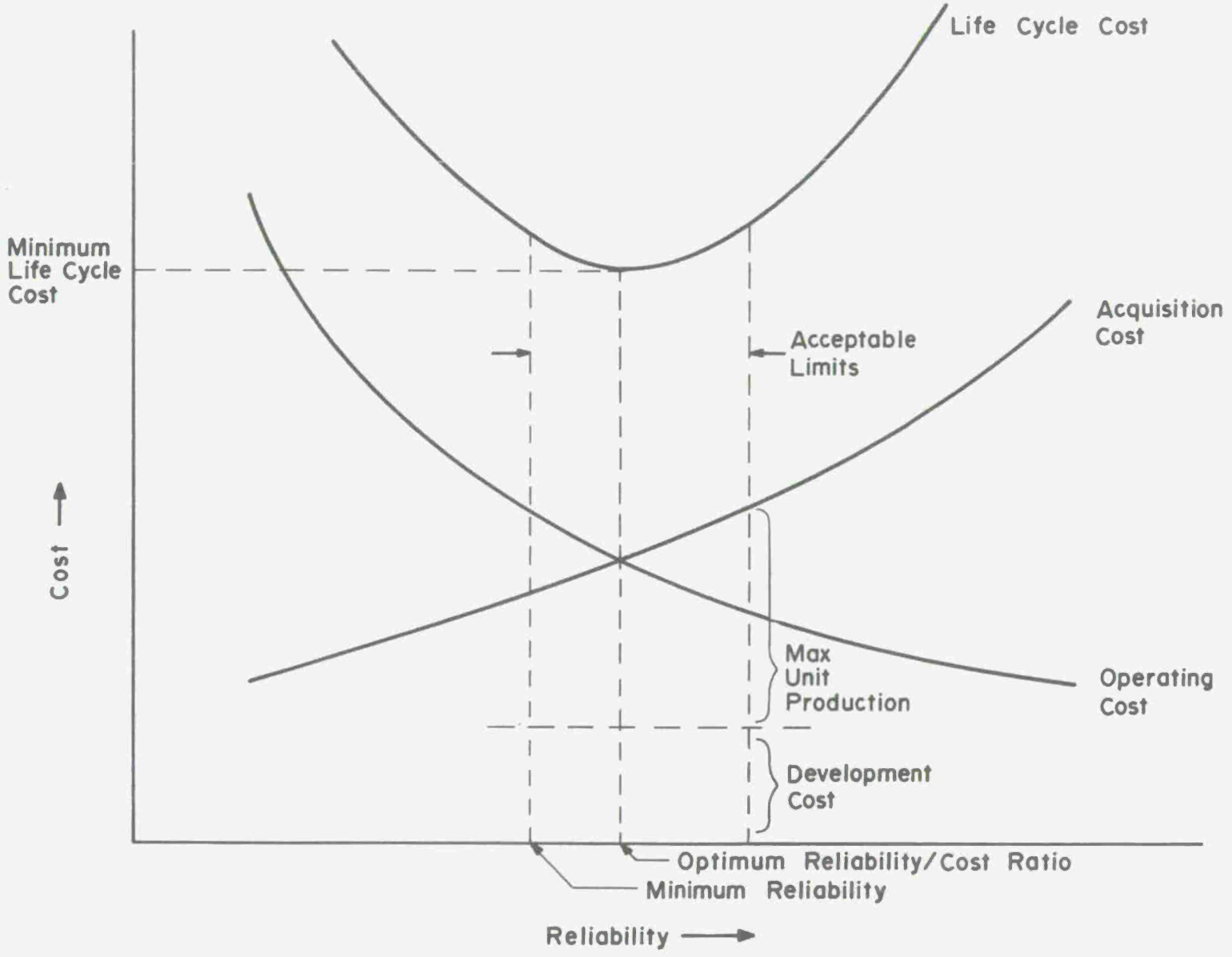


Fig. 4-78 COST VERSUS RELIABILITY

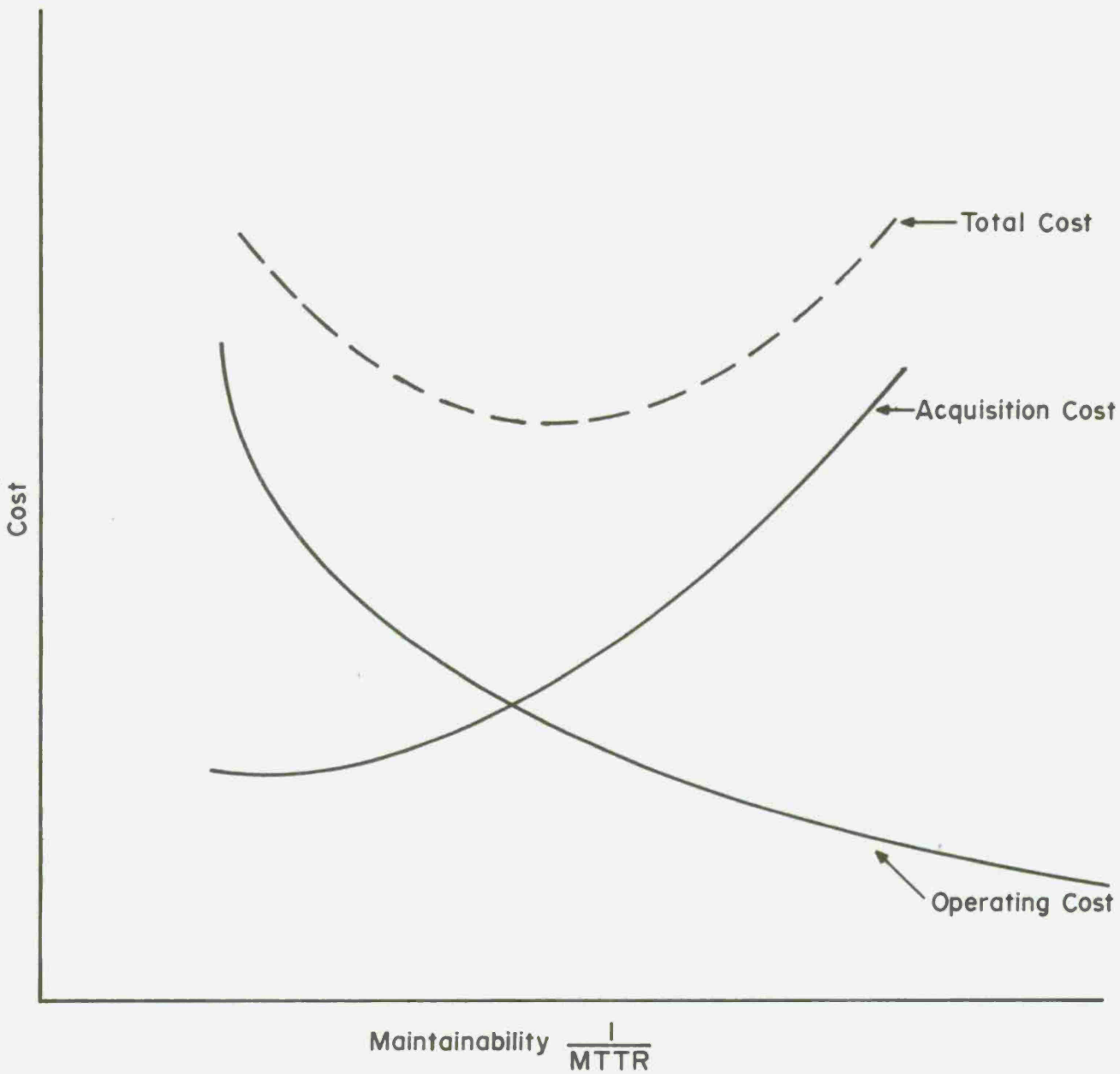


Fig. 4-79 COST VERSUS MAINTAINABILITY

varying difficulty and cost. The cheapest increase in reliability would be taken first and the most expensive last. Therefore, the cost of reliability must be an upward increasing slope.

Essential to effective trade-off studies is the definition of each step and the development of accurate reliability/cost curves for equipment that shows the sensitivity and breakpoints of critical reliability factors. It is the objective of early trade studies to define a band of acceptable performance and cost goals. Figure 4-78 illustrates a method of defining the minimum reliability and the maximum unit production cost based on the minimum ownership cost principles. We assume development cost is fixed over a limited range of MTBF. The right side of the acceptable bound shown in the figure is constrained by the maximum unit production cost, and also results in a new optimum total cost. The left side bound defines minimum reliability levels. The maximum unit production cost should be based on true affordability considerations, and traded and verified during the development and production phases of the program.

Like reliability, increasing maintainability causes increased acquisition costs and reduced operating costs. Maintainability is generally measured in Mean-Time-To-Repair (MTTR); the less time required to repair an item (the smaller MTTR), the more maintainable the item. If one takes the reciprocal of MTTR to obtain a variable which increases with maintainability and with cost of attainment of acquisition, exactly the same type of curves are obtained as for reliability (Figure 4-79).

Relationships can be derived to determine cost variations with equipment performance assuming various technologies and reliability and maintainability approaches. Relationships can also be derived defining how reliability and maintainability vary with performance (or with complexity, which is in turn dependent on performance) with cost held constant. The resultant reliability and maintainability for any given performance can be referred to as the baseline reliability and baseline maintainability.

The concept of availability is of value, in this context, for R&M trade-off studies. Availability is the ability of an item, under the combined aspects of its reliability and maintenance, to perform its required function at a stated instant in time.

Availability involves the application of both reliability and maintainability, ie.., MTBF and MTTR, and is expressed mathematically as

$$A = \frac{MTBF}{MTBF + MTTR}$$

An availability assessment provides a measure of total equipment performance. Equipment can be designed and built to have a high MTBF with respect to MTTR, or ease of maintenance can be designed into the equipment that would result in short maintenance time elements and a low MTTR with respect to MTBF. Frequently, the most practical way to achieve a high probability of equipment performance is to supplement the design for reliability with a design for efficient and rapid repair and a high degree of maintainability. Quantifying these R&M factors in terms of availability provides an insight into the effectiveness of the equipment and demonstrates numerically the impact of significant system R&M elements. Included in this insight is the effectiveness of the R&M design and support factors.

The trade-offs between reliability and maintainability must also be considered. For this purpose, additional relationships are derived which state how relative cost changes as reliability or maintainability is varied from the baseline. Figure 4-80 provides an example of the reliability/maintainability trade-off process using the availability concept described previously. This figure can be interpreted as a resultant cost allocation approach for optimizing MTBF and MTTR. The isocost and isoavailability curves shown here define the appropriate mix of MTBF and MTTR to optimize cost. Note that the optimum R&M approach occurs at the point of contact between the isoavailability and isocost curves. The actual isocurves for specific equipment can be generated using computerized calculation procedures in conjunction with the reliability, maintainability, cost and availability models previous described.

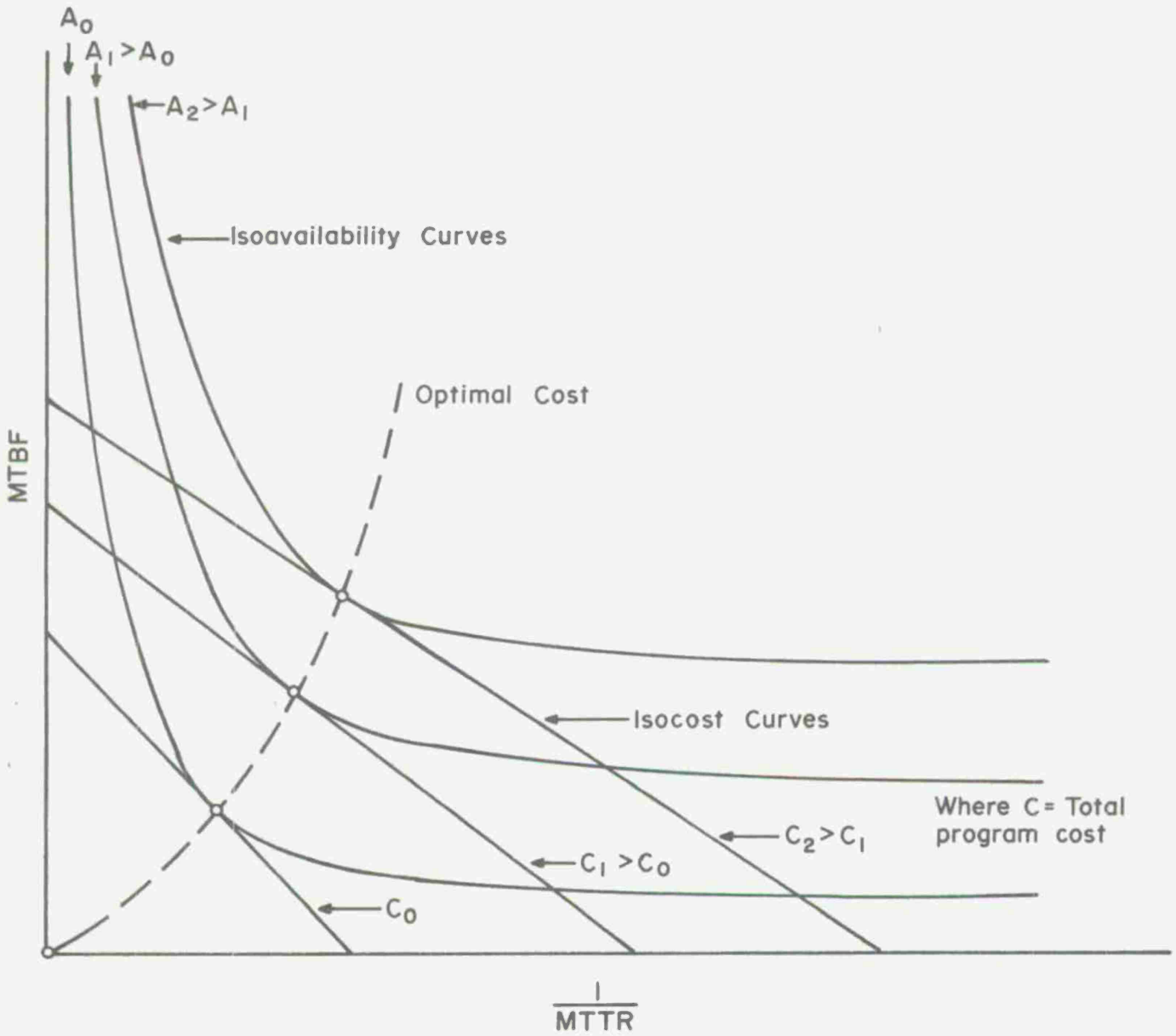


Fig. 4-80 OPTIMUM COST ALLOCATION APPROACH

4.3.2.2 Development and Production Phase

As the program progresses through advanced and full scale development, some cost (production and support) and performance trade-off flexibility is needed to permit the development of acceptable systems within the cost constraints. For this purpose, design to cost programs feature these characteristics:

(a) End-item minimum performance goals or specifications (to allow trade-off flexibility) are used rather than detail design specifications for systems, subsystems and components.

(b) Trade-off decision thresholds for program managers are established to clarify their authority to make trade-offs within the overall cost, schedule and performance requirements of the program, and

(c) Sufficient development time and resources are allocated to iterate designs to reduce future costs.

The iterative design process is an essential ingredient of effective design to cost program implementation. Figure 4-81 illustrates[46] several phases in a design program with the emphasis on: 1) allocation of cost goals to the subsystem and component level, 2) estimates of subsystem costs with comparison to target figures, and 3) reallocation or redesign to achieve total target cost goals. The process continues throughout the program's life cycle, including the preproduction and production phase.

The initial cost goal allocation is developed by Program Management. The objective of the allocation process is to develop cost goals that are under the designer's control. This means that nonrecurring costs, such as G&A, fee and development cost, must be segregated from the essential remaining costs that are within the designer's control. The principal recurring costs (material, direct labor and support labor) are shown in Figure 4-82. These costs are further categorized by functions or subsystems to establish a cost matrix that can be used as a Design UPC worksheet. An example of a preliminary Design UPC worksheet is shown in Table 4-49. The initial allocation of system cost is based on an estimate of the relative complexity of each individual subsystem. Note

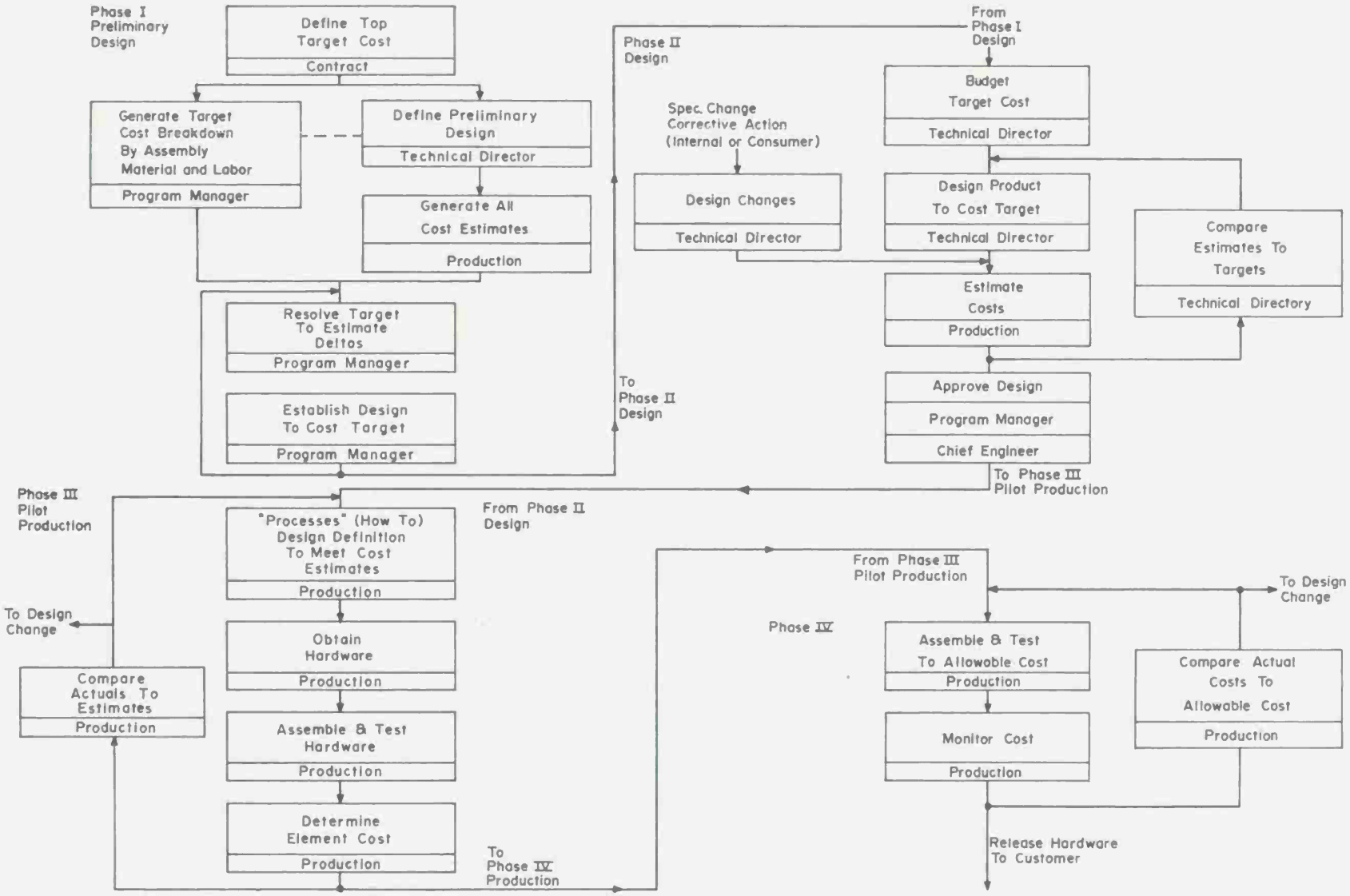


Fig. 4-81 DESIGN TO COST PROGRAM PHASES (Ref 46)

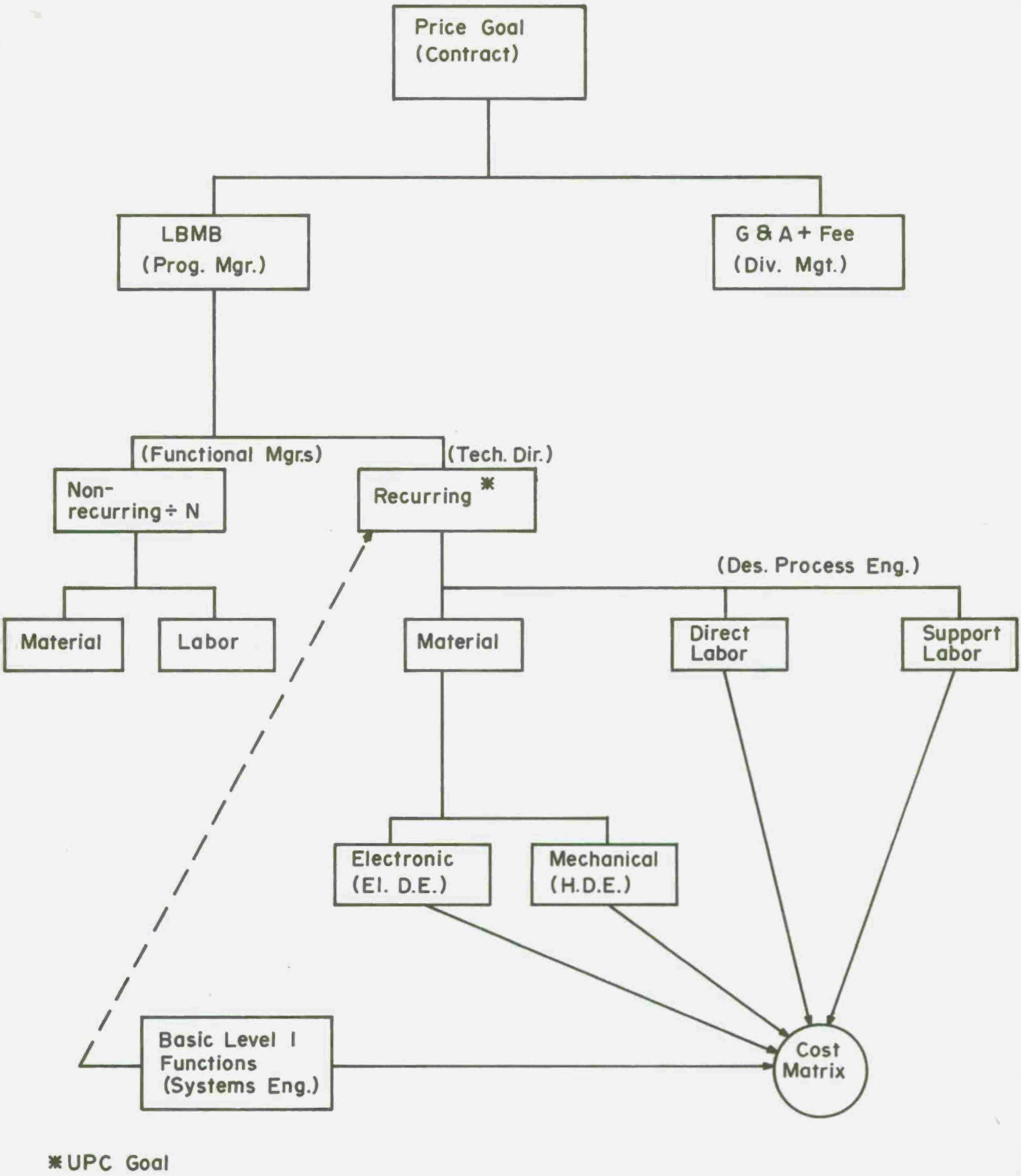


Fig. 4-82 DESIGN TO TARGET COST MODEL

Table 4-49 PRELIMINARY DESIGN UPC WORKSHEET--PHASE 1[46]

Device Computer
Labor Rates June 1975
Quantity 40
Date December 1, 1974

Production Rate 3/Month
Top Target $40,000
Lot Quantity 3

Function	Percent Complexity	60% Material Tar.	Est.	30% Direct Labor Tar.	Est.	10% Support Labor Tar.	Est.	100% Total Tar.	Est.
Memory	22%	4.5		3.2		1.1		8.8	
CPU	25%	7.4		1.9		0.7		10.0	
Chassis	20%	3.6		3.3		1.1		8.0	
Power Supply	4%	4.0		0.4		0.2		1.6	
Final Assembly	3%	---		0.9		0.3		1.2	
Unit Test	14%	---		4.1		1.5		5.6	
I/O	12%	3.9		0.7		0.2		4.8	
Total	100%	20.4		14.5		5.1		40.0	
"SHOULD COST"									

that the estimate is based on a known total:

production quantity,
production rate, and
cost related to a specified base year.

Historical data is used to make an initial estimate of the distribution of cost between material, direct and support labor. After preliminary design data is generated, production cost estimates are generated and the data compared with target values. Table 4-50 compares the estimates with target costs and shows adjusted target cost where deviation against the target would not be reduced by further design change. To meet total contract cost goals, it was decided (in this example) to reduce nonrecurring product design costs.

The subsystem can now be further defined by the components, chassis, connectors and cables that make up these subsystems. In the same manner as described above, target costs can be allocated to the component level and firm costs can be estimated and compared with the target values. The costs are shown in the Work Breakdown Structure (WBS) in Figure 4-83. The WBS is a useful method of allocating both cost goals and task assignments to individual designers. Table 4-51 lists target values for subassemblies; the procedure for allocating, estimating and resolving deviation from target cost is the same as previously discussed. At this point, it is possible to improve the accuracy of the estimates and set standard hours for assembly and test of the individual subsystems. Standard hours can be estimated by production personnel, given the production rate and total quantities.

It should be noted that trade-offs can be made between support cost and component types, as well as assembly time, to achieve the overall target cost goal. Methods for estimating and selecting the lowest cost solution is the subject of Section 4.3.3.

In the previous example, it was simple to relate the subassembly's performance function to its cost. In many cases, it is difficult to separate cost and function, since a particular performance function is shared by several assemblies. Since cost and reliability estimates can be more easily estimated against subassemblies (using reliability worksheets as described in Section 4.1), it is useful to employ a function

Table 4-50 PRELIMINARY DESIGN UPC WORKSHEET (COMPLETED)--PHASE 1[46]

Device Computer
Labor Rate June, 1975
Quantity 40
Date December 1, 1974

Production Rate 3/Month
Top Target $40,000
Lot Quantity 3

Function	Percent Complexity	60% Material Tar.	60% Material Est.	30% Direct Labor Tar.	30% Direct Labor Est.	10% Support Labor Tar.	10% Support Labor Est.	100% Total Tar.	100% Total Est.	Adjusted Target
Memory	22%	4.5	5.0	3.2	4.0	1.1	1.4	8.8	10.4	9.0
CPU	25%	7.4	7.3	1.9	2.3	0.7	1.0	10.0	10.6	10.6
Chassis	20%	3.6	4.2	3.3	3.6	1.1	1.3	8.0	9.1	8.9
Power Supply	4%	1.0	1.3	0.4	0.9	0.2	0.9	1.6	3.1	2.6
Final Assembly	3%	---	---	0.9	1.4	0.3	0.6	1.2	2.0	2.0
Unit Test	14%	---	---	4.1	3.6	1.5	1.0	5.6	4.6	4.6
I/O	12%	3.9	3.8	0.7	1.2	0.2	0.6	4.8	5.6	5.6
Total	100%	20.4	21.6	14.5	17.0	5.1	6.8	40.0	45.4	43.3

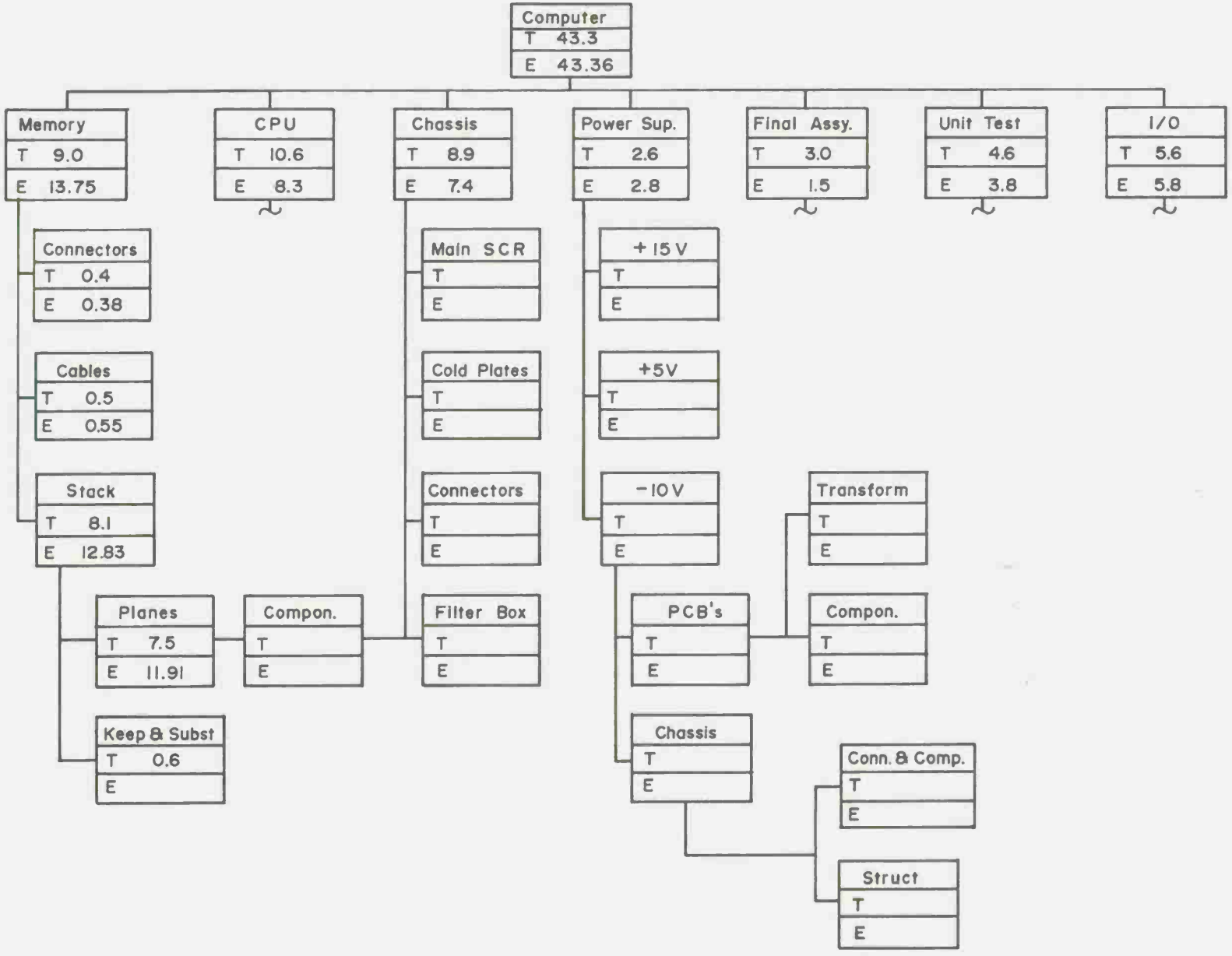


Fig. 4-83 WORK BREAKDOWN STRUCTURE (Ref 46)

Table 4-51 UNIT PRODUCT COST MATRIX[46]

Product Line Computer
Device
Cum. Ave. Quantity
Lot Size

UPCT(LBMB) $9.0K
Production Rate
Date
Rev. No.

Page ___ of ___

Subsystem	Standard Hours		Material $K		Direct Labor $K		Support Labor $K		Total $K	
1.0 Memory	Tar.	Est.	Tar.	Est.	Tar.	Est.	Tar.	Est.	Tar.	Est.
1.1 Stack	91.0	243.0	4.3	4.8	2.53	6.76	1.27	1.27	8.1	12.83
1.2 Cables	4.4	4.6	0.30	0.33	0.12	0.14	0.08	0.08	0.50	0.55
1.3 Connectors	5.1	5.4	0.20	0.17	0.14	9.15	0.06	0.06	0.40	0.38
Total	100.0	253.0	4.8	5.30	2.79	7.05	1.41	1.41	9.0	13.76

versus subassembly worksheet of the type shown in Table 4-52. Estimates of the fraction of the subassembly that performs a specific function are determined by the designer. Using known part counts for the subassembly, it is possible to estimate the number of components required to perform a particular function. Both labor and material cost to perform the function can now be estimated as shown in Figure 4-84. The reliability or failure rate associated with the performance of the function can also be estimated using part count or reliability stress worksheets. The need for the performance function can then be scrutinized in light of the knowledge of the cost of the function and unreliability associated with the design. Trade-offs can be made with full knowledge of the cost to include a specific function in the system.

4.3.2.3 Balanced Design Management

As previously indicated, an effective military system must seek a balance between performance, R&M and cost. The balancing must be done on a tentative basis, such that the bounds for all parameters can change. A balanced design management technique must be structured which provides visibility into system costs and shows how they relate to performance and R&M requirements. The management technique must provide a means of ascertaining whether the design configuration can be established within the "design to" goals and, if not, to give warning of this in time to permit corrective action. In addition, the balanced design methodology must maintain a historical record of all parameters associated with the design configurations.

A concept presently being used in the design stage of ongoing programs involves the formation of a balanced design team, composed of representatives from the military program office and contractors. This team participates in reviewing ongoing designs and planned production processes in order to provide information and alternatives that would enhance performance and/or reduce cost. During early system development, conceptual cost of ownership studies were used to derive target "design to" goals covering the balancing parameters, and were assigned to each equipment item. These target goals were then used as the basis for balancing each design parameter.

Table. 4-52 FUNCTION - SUBASSEMBLY MATRIX

Labor Back-up / Board No. / Spec. Reqt. & Para.	8091-1	-2	-3	-4	-5	-6	-7	-8	-9	-10	-11	-12	-13	-14	-15	-16	-17	-18	-19	3401B242/43/46/43	EG 8091 A1	SK 97979-8091-1	Manufacturer	Parts/Function
20.14.1 RJDF																								
a,e) Interpret & Validate Input Com.			0.5										1.0											451
b) Command RS Thrust							0.5		1.0	1.0														273
c) Command / SO Valve Closure	1.0		0.5		0.5						1.0	1.0												963
d) Monitor Thrust Pressure & Denote Fail					0.5	1.0																		279
f) Bite		0.5		1.0			0.5	0.5																209
#1 Convert & Reg. Cir. Volt (P/S)														1.0	1.0	1.0	1.0	1.0	1.0	1.0				496
#2 Maintain Min. Sol. Volt. (BUS)		0.5						0.5																76
#3 Interface Circuit (Mother)																								
#4																								80
#5 Enclose LRU (Chassis Misc. Hdwr.)																								
#6																								
Elec. Piece Part Count Per System	323	67	606	61	273	142	144	84	158	43	30	170	148	284	4	6	12	88	76	20				

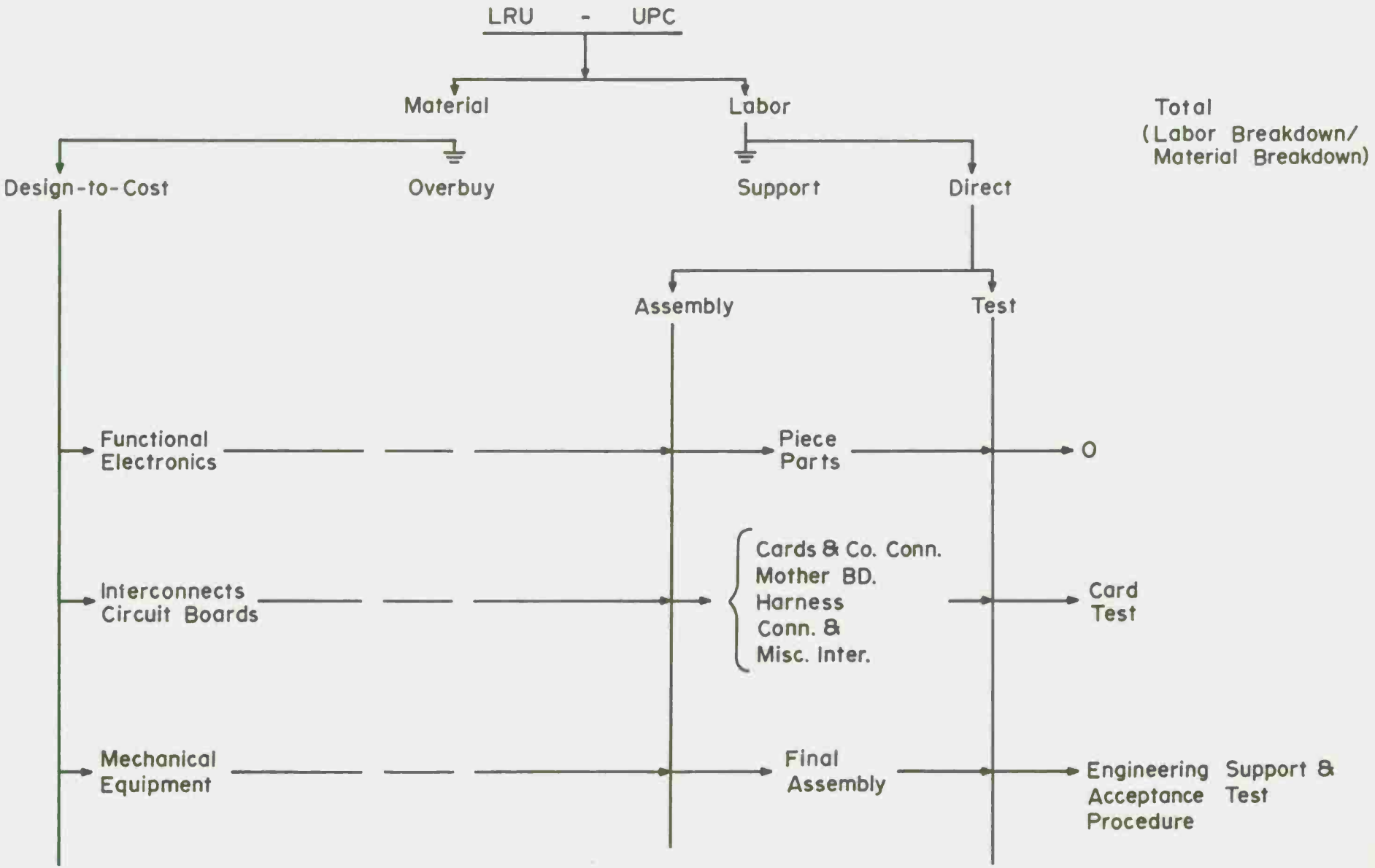


Fig 4 - 84 LRU-UNIT PRODUCTION COST

To assure that the team has the proper data, in the proper format at the proper time, a management information system (MIS) containing each discipline's data banks (e.g., R, M, etc.) can be developed as part of the program.

The MIS serves as a record keeper and processor for all data related to balancing a system design. It serves as a vehicle for providing effective technical interface, as well as pertinent reports, to military personnel concerned with balancing design parameters. Therefore, the primary purpose of the MIS is to facilitate proper balance of pertinent system parameters, such as cost, performance, reliability, maintainability and producibility. The actual balanced design is accomplished through an iterative process which results in a continuous update of the estimated value of each system parameter. Thus, a higher degree of confidence can be given to the acquisition cost, logistics support cost, and cost of ownership as the system is developed. In addition, it provides visibility to all the "design to" goals. Outputs of the MIS are available at each significant milestone (e.g., design reviews). Thus, the MIS allows the "balanced design" team to flag areas that may require further design effort to reduce costs or enhance reliability, performance, etc.

Figure 4-85 contains a conceptual diagram of the MIS record form. Each data element in the structure is representative of a functional unit of the system (i.e., SRU) and is related to its succeeding level (i.e., LRU). This type of arrangement provides a comparison of target values to estimated values.

A tolerance band is displayed in terms of "greater than" or "less than" goals. These tolerances indicate the maximum band of acceptable fluctuations of the system parameter values. Examples of the balancing parameters and the data elements to be stored in the MIS are: cost (material, acquisition, LSC), reliability (MTBF, parts count), maintainability (fault detection, on-line and off-line, BITE, MTTR, AGE), producibility (percent subcontracted, percent LSI, discrete circuits, etc.), configuration (weight, power, volume), and survivability (EMP, nuclear hardening).

Fig 4-85 MIS RECORD FORMAT

Although the comparisons to be made within the balanced design are relatively few and simple, great quantities of data must be processed and disseminated. The MIS is both economically and technically suited for computer processing. A computerized version allows for a greater degree of flexibility and responsiveness.

Because of continual iteration of the design during system development, many computer runs are performed to evaluate and revise the balancing parameters. Preformatted keypunch cards and MACROS (open subroutines which allow the programmer to alter input parameters and have several executions during a single computer run) assure rapid computer processing.

The MIS was structured such that parameters outside of the target goal tolerance band are flagged. These flagged values are used by the "balanced design" teams for analyses/trade-offs. These values are used with the previous data to derive new targets, new design configurations, etc. The general flow of information related to the function of the MIS through the balanced design process is depicted in Figure 4-86.

The MIS, therefore, facilitates the balancing of the system parameters (cost, reliability, maintainability, survivability, design configuration, performance and producibility). The balancing is accomplished through an iterative process where the various parameters are continuously monitored and updated. Hence, the MIS provides the vehicle for both collecting and disseminating parameter values at each iteration. Thus, a historical record of the design process for an LRU, SRU or any parameter is retrievable at any point in time.

4.3.3 Meeting Cost and Reliability Targets

The previous section described methods of defining, allocating, and managing cost and reliability goals. The handbook would not be complete if it did not provide guidance to enable a designer to meet the defined cost and reliability targets. Meeting cost constraints is the subject of this section and will be treated at two levels: 1) the broad system trades made during the early concept and validation phase, and 2) detailed cost trade-off involving component selection.

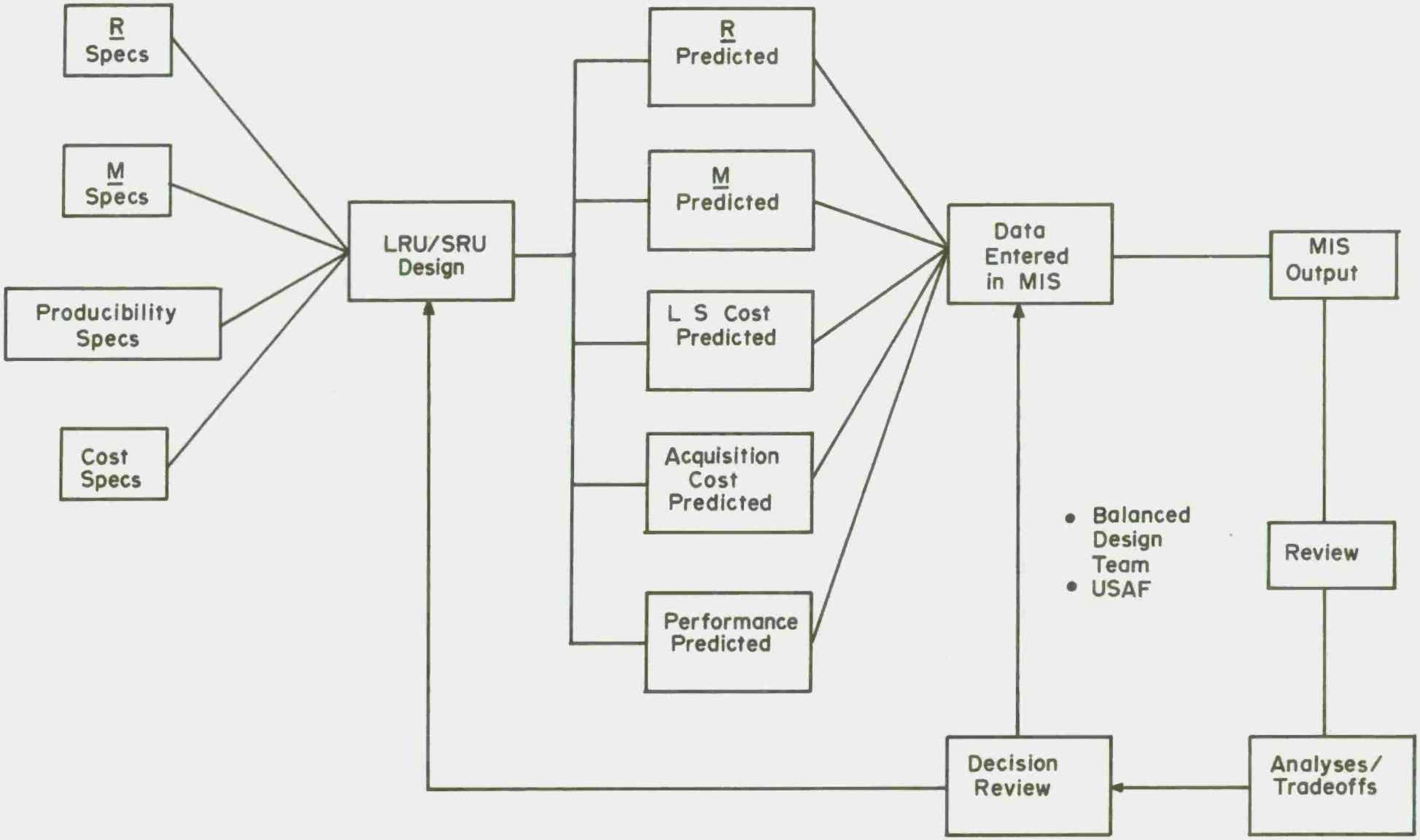


Fig 4 - 86 MIS INFORMATION FLOW

Concept and Validation Phase

The B-1 offers an excellent example of the application of design-to-cost principles. As originally conceived, the electronics for this aircraft would cost $10-12 million per aircraft, weigh about six tons and would consume 100 kW of power. Although it was acknowledged that B-1 mission needs are complex, it was felt that the requirements could be met at lower cost, by applying "design-to-cost" principles. The end result of the cost cutting effort was to remove three tons of electronic equipment and an expectation of improvement of the field reliability.[45] For example, the B-1 will now have two good inertial navigators on board for less than the price of one more precise navigator and the radar will cost less than half of that originally proposed. The "design-to-cost" principles used to achieve these results from the B-1 can be generalized for most other aircraft programs. They are:[45]

(1) Review of all requirements for avionics against both the specific designs needed and against the cost of the design.

(2) When stated requirements drive costs unduly, other means should be sought to satisfy the requirements.

(3) Equipment of proven and reliable performance should be selected in preference to starting completely new designs, even if the older equipment needs modification to adapt and fit.

(4) Apply standardization principles whenever possible.

(5) Balance, and if necessary change, operational procedures if simpler, less costly equipment can be found to do the job.

(6) Allocate and define cost goals for individual subsystems of the avionics complements.

(7) Eliminate, or put into a phase of intensive advance development, high risk equipment to prove and reduce cost.

(8) Segregate equipment by function (e.g., offensive and defensive subsystems) to reduce complexity and to increase flexibility of the computer software.

(9) Use standard (off-the-shelf) equipment where possible. Hold industrial competition to select equipment.

The above list is by no means complete and only outlines a common-sense approach to equipment selection in the early phase of the design. The role of the designer during this phase is to provide cost and reliability data using limited detail design information. One of his efforts is to identify costly processes or high skill levels and manpower cost associated with alternative design requirements. The designer must be aware of the limits of available technology and be experienced enough to relate past problem areas to the proposed design requirements. As the design is iterated and better defined, the cost reliability trade-offs can be more mechanized and better defined.

The next section describes the procedures necessary to perform detailed trade-off at the component and system level.

Development and Production Phase

The cost of unreliability is usually measured in terms of the added repair and replacement cost accrued in the field resulting from a failure of a component. This cost can be compared with the incremental unit cost of a component of higher reliability. If the added component cost is less than the savings resulting from reduced field failures, the high reliability component should be selected. Reliability parameters can be used to estimate the expected cost of field failures. Although application of the principles outlined above should yield a design which minimizes ownership costs, the resultant design may not meet the program "design-to-cost" goals. In addition, component costs are not the only contribution to unit production cost. High reliability requirements can often add to the labor cost by requiring higher labor skill levels. On the other hand, low reliability components can increase unit production cost by requiring added quality support labor, increase system test time and scrap rate, and increase the probability of higher cost platform and/or other verification test failures.[47] The added costs will eventually be charged through variance and overhead accounts to unit production cost.

The decision to select alternative high reliability equipment can be based on the following equality. If the change in component cost and labor

requirements are less than the added support costs, expected test failure costs and expected field failure costs,

$$\Delta \text{ Component Cost} + \Delta \text{ Labor Cost} < \Delta \text{ Inspection Cost} + \Delta \text{ Expected in Process Failure Test Cost} + \Delta \text{ Expected Field Failure Cost}$$

then select the high reliability equipment.

The general formula to be used for the selection of individual components or a complete system is more formally given below:

$$CQ < Q \sum_{i=1}^{n} (\Delta P(f)_i \times C_i) + Q \times \Delta P(f) \times C_f$$

where

ΔC = average added cost of a high reliability part over a standard part (both parts and labor)

Q = quantity of parts per system

$\Delta P(f)_i$ = added failure probability of low reliability failure over a standard part during the i^{th} test phase

n = number of test phases

C_i = cost of failure during the i^{th} test phase

$\Delta P(f)$ = probability of failure in the field $\Delta P(f)_m \Delta\lambda T$

C_f = cost of field failures.

Selection of equipment that satisfies the inequality will result in the lowest ownership cost. If the second term on the right of the equation is disregarded (i.e., expected field failure costs) and the inequality is satisfied, lowest unit production cost will be attained.

Field Cost Versus Component Cost

The simplest comparison that a designer can make is between unit component cost and field failure costs. The underlying assumption in this approach is that the added fabrication labor costs incurred by selecting the high reliability design is offset by the saving resulting from a reduction of test related failures. With the understanding of the assumptions, the rule is applied as follows:

(a) Estimate the (inherent) failure rate (λ) of each alternative design (use stress derating tables and formulas as described in MIL-HDBK-217B--see Section 2).

(b) Estimate the useful life of the system (T).

(c) Estimate the cost (C) to service each failure in the field.

The expected cost of field failures is:

$$E(Cost) = \lambda \cdot T \cdot C$$

Table 4-53 lists the parameters and costs of three alternate transistor designs.[48] The failure rate (λ) was estimated using the following formula:

$$\lambda = \lambda_b(\pi_E \pi_Q \pi_A \pi_{S2})$$

where λ_b is the base failure rate adjustment factor shown in the table. Adjustment factors are listed in Table 4-53. Values were obtained from MIL-HDBK-217B using available design data. Note the change in total cost of the transistors as the equipment's life increases.

The effect of adding a component to a circuit can also be evaluated using the approach. The procedure and input data are used to compute the failure rates (Table 4-54) so that two total reliability costs are computed with and without clamping diodes in the circuit. The estimated cost in these illustrations does not represent total field failure cost, but represents only those factors over which the designer has direct control.

Standardization--Costs and Savings

Component standardization can reduce the unit production cost of the system as well as development cost. Standardization allows quantity discounts in the purchase of components and can significantly reduce documentation cost during development.

A reliability study[47] of two radar systems (APQ-120 and APQ-113) found the program which emphasized standardization (APQ-113) utilized one-third fewer piece part drawings and 2800 fewer piece parts to achieve basically the same functions that the APQ-120 provides. Comparisons of part standardization are shown by part type in Figure 4-87. This chart

Table 4-53 SELECTING THE OPTIMUM TRANSISTOR[48]

Computations	Transistor #1 Without Heat Sink	Transistor #1 With Heat Sink	Transistor #2 Without Heat Sink
π_E Environmental Factor (A_I)	25	25	25
π_Q Quality Factor	0.4	0.4	0.4
π_A Application Factor	1.5	1.5	1.5
π_{S2} Voltage Stress	0.75	0.75	0.48
λ_b Base Failure Rate ($\times 10^{-6}$ hrs)	0.063	0.016	0.010
λ Failures per 10^6 hrs	0.709	0.18	0.11
MTBF (Mean Time Between Failures)	1,410,437	5,555,555	9,090,909
Percent Failures/Year	1.22%	0.31%	0.19%
Field Cost/1 Year	30.8¢	7.9¢	5.0¢
Field Cost/2 Years	61.6¢	15.8¢	9.0¢
Standard Cost/Year	25.0¢	33.0¢	40.0¢
Total Cost/Year	55.8¢	40.9¢	45.0¢
Total Cost/2 Years	86.6¢	48.8¢	49.0¢

Table 4-54 COMPARISON FOR DESIGN TO ADD A DIODE[48]

Computation	Without Diode	With Diode
π_E Environmental Factor (A_E)	25	25
π_Q Quality Factor	0.4	0.4
π_A Application Factor	0.5	0.5
π_{S2} Voltage Stress Factor	0.75	0.48
λ_b Base Failure Rate ($\times 10^{-6}$ hrs)	0.063	0.063
λ (Failures per 10^6 hrs)	0.709	0.454
MTBF (Mean Time Between Failure)	1,410,437	2,202,643
Percent Failures/Year	0.468%	0.30%
Initial Part Cost	40.5¢	45.0¢
Warranty Cost/Year	11.9¢	7.6¢
Standard Cost/Year	40.0¢	45.0¢
Total Cost/Year	51.9¢	52.6¢

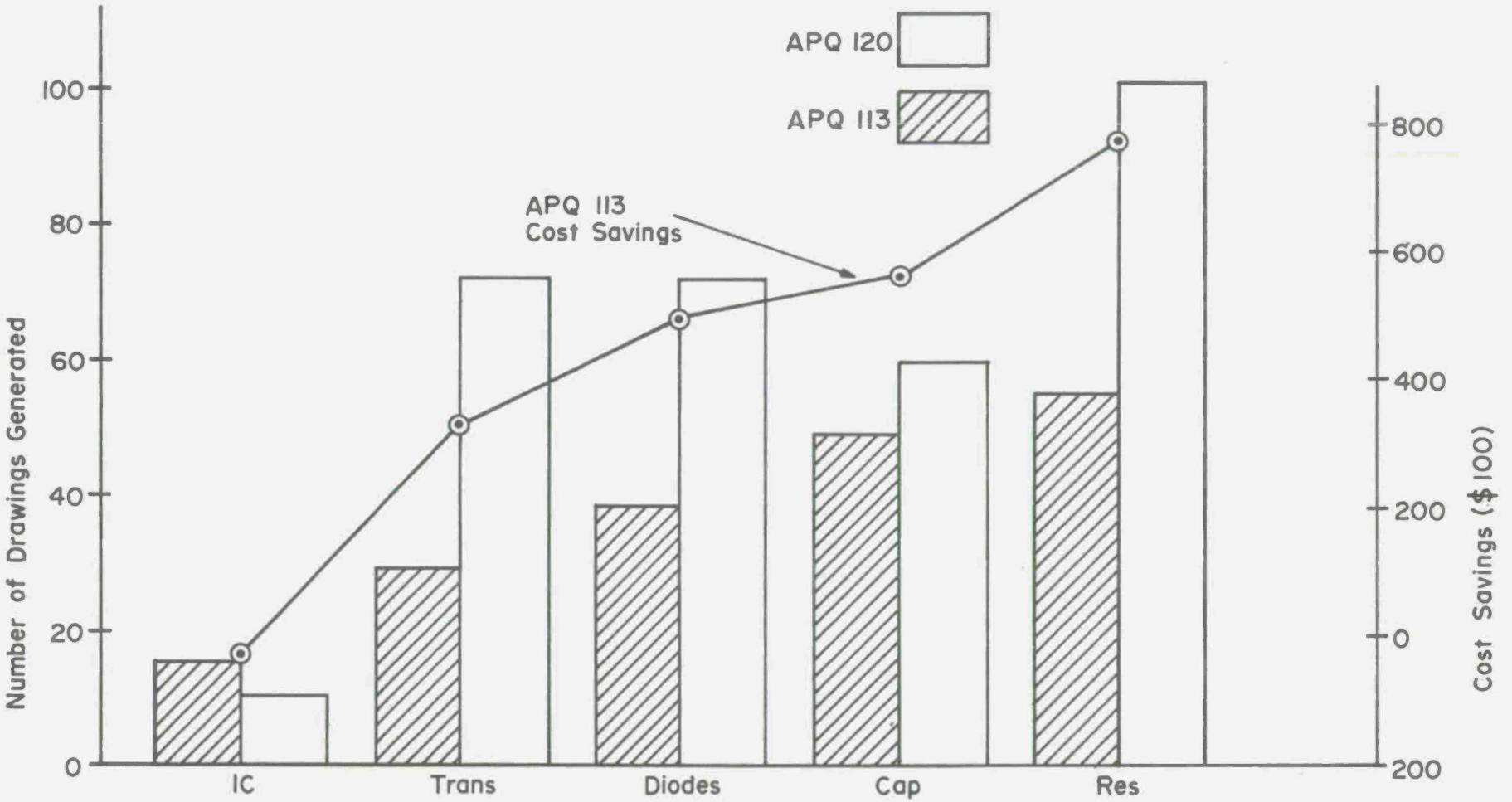


Fig. 4-87 PART STANDARDIZATION - COST SAVINGS (Ref 47)

shows the percent of total part population of a generic part type as a function of the number of different part drawings utilized. Figure 4-88 shows an estimate of initial potential cost savings available through parts standardization based on a cost of $5000 to make and release a part drawing. The savings available through pooled-buy purchase agreements would provide additional cost savings and results in reduced unit production cost.

Standardization is applied through the use of a Preferred Parts List (PPL) distributed to the designer. Although the PPL should be compiled with preference given to components of high known reliability, standardization can lead to a compromise of reliability. Listed in Table 4-55 is the MTTF of five vacuum tube designs at five different vibration levels.

Table 4-55 MTTF OF ALTERNATIVE TUBE DESIGNS[49]

Probabilities	0.10	0.20	0.40	0.10	0.20	% of Tubes Used
	Vibration Level					Expected
States of Nature	N_1	N_2	N_3	N_4	N_5	Value (EV)
S_1 Present Design	200	200	200	200	200	200
S_2 Design 2	180	180	260	180	180	212 (Single Best)
S_3 Design 3	240	220	200	180	180	202
S_4 Design 4	180	200	200	210	240	207
S_5 Design 5	185	175	165	155	145	Dominated

The highest reliability can be achieved by selecting the tube that performs best at the specified vibration level. Since only one tube can be produced economically, tube design 2 should be selected and will produce the highest level of reliability at all vibration levels. The table illustrates the application of principles of decision theory to product design. Reference 49 offers a more complete discussion of decision theory.

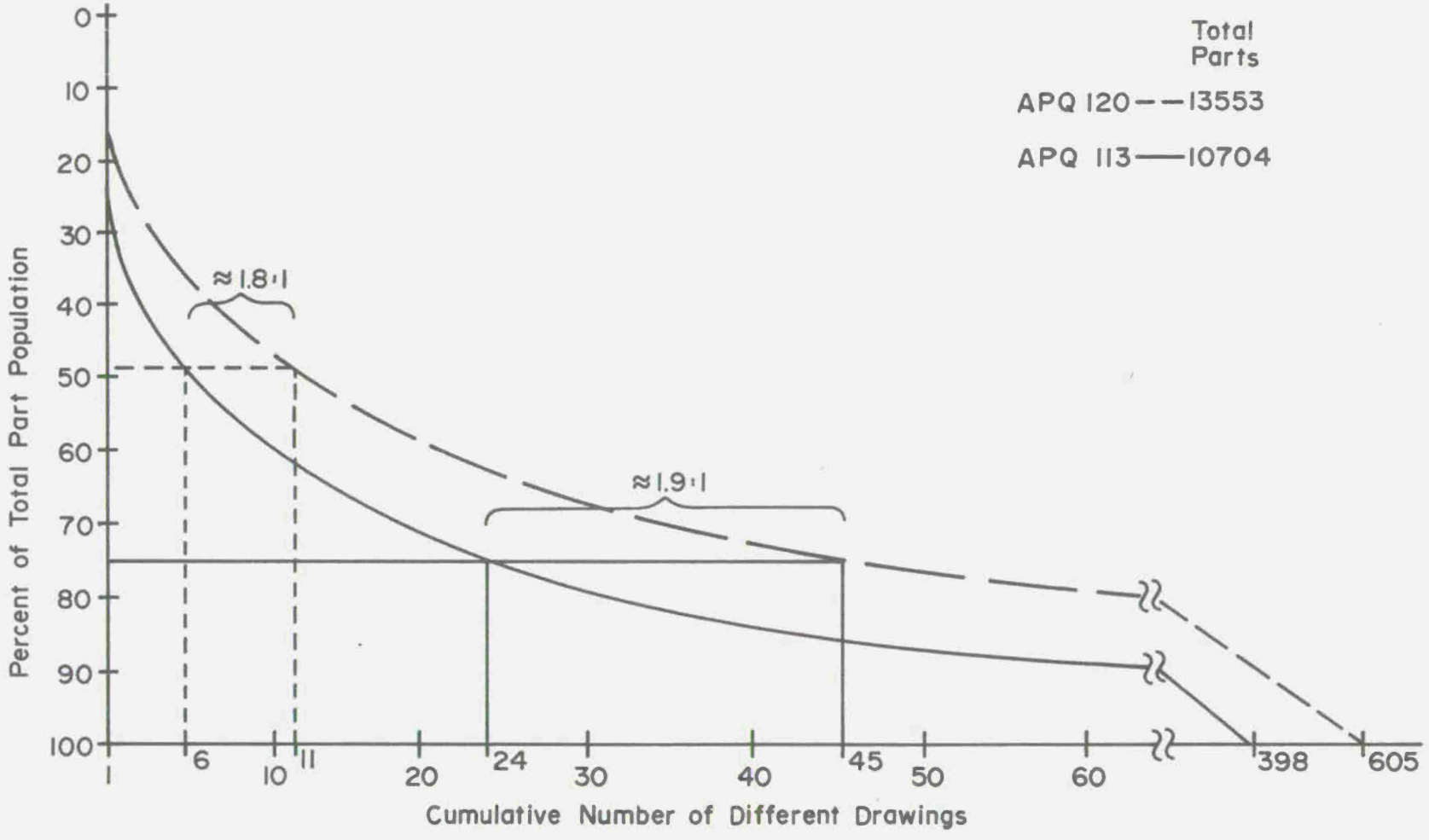


Fig. 4-88 DRAWING STANDARDIZATION COMPARISON
COMPOSITE OF ALL DRAWINGS (Ref 47)

Component Cost Versus Expected Cost of Failure During System Test

A system will be subjected to several phases of test during its production. These can include:

Incoming Test
In-Process Test
Reliability Acceptance Test (RAT)
Platform Test

The cost of failure during test increases as the system progresses to a higher assembly level. Table 4-56 lists estimated failure probabilities for both high and low reliability components, based on the APQ-113 system development experience.[47] To decide whether the added cost of the high reliability components is paid for during the system test phase, the following inequality is tested.

$$\Delta C \cdot Q < Q \sum_{i=1}^{n} \Delta P_i(f) \cdot C_i$$

where

ΔC = the average additional cost per component = \$1.00
Q = Quantity of Parts/System = 10,700

Therefore,

$\Delta C \cdot Q$ = \$10,700

ΔP_i and C_i are given in Table 4-56.

$$Q\Big[(P_1(HR)-P_1(S))\cdot C_1 + (P_2(HR)-P_2(S))\cdot C_2 + 0.30(P_3(HR)-P_3(S))\cdot C_3 + (P_4(HR)-P_4(S))\cdot C_4\Big]$$

$$= 10{,}700(\$0.384 + \$0.48 + \$0.015 + \$0.50)$$

$$= \$14{,}758$$

The added expected cost of test failure is greater than the increased cost of the component; therefore, the high reliability components will result in the lowest unit production cost.

Table 4-56 APQ-113 PRODUCTION TEST FAILURE EXPERIENCE[47]

Test Phase	$P_i(S)$ % Failures Std. Parts	$P_i(HR)$ % Failures High Rel. Parts	C_i Cost of Failure
Incoming	3.0 %	0.6 %	$ 16
In-Process	0.4 %	0.08%	$ 150
RAT*	0.02%	0.003%	$ 300
Platform	0.03%	0.01%	$2,500

*30% of systems presented to RAT.

Estimates of both failure probabilities and cost of failure will vary with the type of system being developed, and the manufacturer must develop data from his test experience. If the costs of test failure are correctly accounted for, high reliability parts can be justified and result in lower production cost in many system production programs.

The failure probabilities in Table 4-56 include both inherent reliability failures and infant mortality type failures. If a screening program is introduced into the production program, the cost of burn-in can be directly compared to reductions in other product and QC costs.[50] Figure 4-89 illustrates the impact of a burn-in program on production and QC costs.

A cost evaluation of product environmental screening of the APQ-113 Radar was performed in Reference 47. Typical burn-in costs were compared with the cost of platform failure. To quote from the study, "The product environmental screening investment would have been completely amortized if only 24 percent of the factory burn-in precipitated failures had escaped to fail at the field platform level. Actually, it was found that 40 to 80 percent of the LRU's tested, failed burn-in, most occurring during the first temperature cycle." Without burn-in tests, the majority of these failures would have been detected during platform testing.

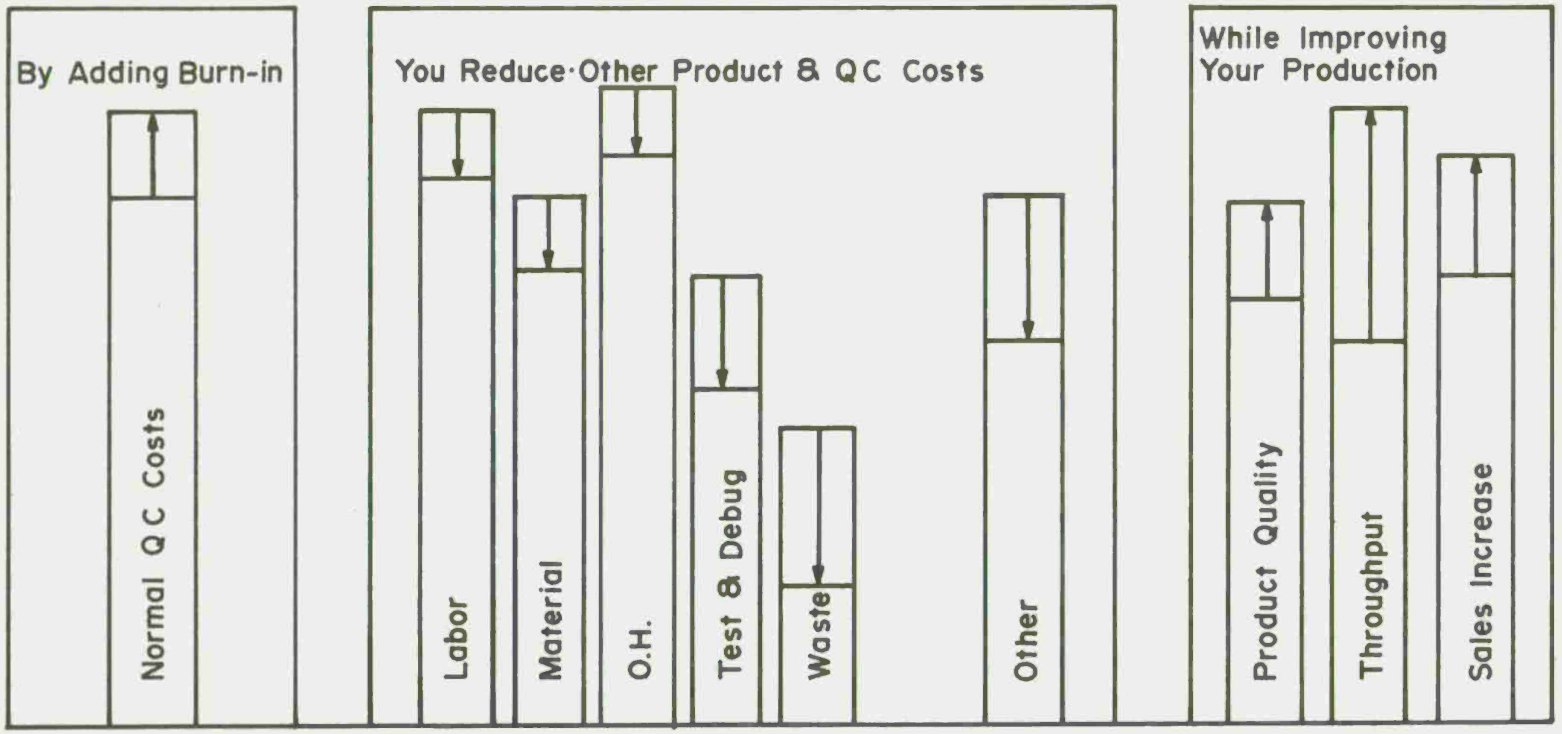


Fig. 4-89 PRODUCTION IMPACT OF A BURN-IN PROGRAM (Ref 50)

Balanced Design--Meeting System Requirements

A methodology has been established to evaluate the reliability of a design in terms of

(a) System Field Failure Costs, and
(b) Total Unit Production Costs.

A strong case has been established that high reliability components and reliability provisioning can reduce production costs. It is also conceded that, often, reliability and unit cost goals can be in conflict and a designer must balance his design to meet both of the contractual requirements. To achieve a total balanced system design, a cost versus reliability trade-off must be performed. The example and methodology presented were originally described in Reference 51.

Three component groups are defined, each having three levels of reliability. Table 4-57 lists both costs and failure rates for each group and reliability level for equipment under consideration for a Missile Interface Unit, proposed for use in a manned bomber.

The component groups categorized by the various degrees of reliability yield 18 combinations shown in Table 4-58. For example, point 4 is computed in the following manner:

$$\text{MTBF} = \frac{10^6}{29.0 + 3.5 + 0.18 + 33.0}$$

MTBF = 15,225 hours

Cost = 11,650 + 1,560 ($0.54)

Cost = $12,984

All computed points can be displayed in a scatter plot as shown in Figure 4-90.

A reliability requirement of 19,000 hours is shown as a horizontal line in the figure. Using point #1 as a reference, equipment reliability must be increased to one of the alternate configurations. A line to point 9, or condition (2,2,1), exhibits a 19,493 hour MTBF at the lowest cost of $12,776 per unit.

Table 4-57 COST/RELIABILITY WORKING DATA[48]

Component Group	Quantity (Q)	MIL-STD Failure Rate (Per 10^6 hrs)	Med. Rel. Failure Rate	Cost of Med. Rel. (Per Comp)	High Rel. Failure Rate	Cost of High Rel. (Per Comp)
1. Integrated Circuits	525	29.0	14.5	$0.54	3.63	$3.00
2. Semiconductors	1560	7.1	3.5	0.54	0.89	2.50
3. Resistors	280	0.3	---	---	0.18	1.75
4. Other Part Types	---	33.0	---	---	----	----

Total Failure Rate = 69.4
Equivalent MTBF = 14,409
Total Cost Based on MIL-STD parts = $11,650

Table 4-58 COSTS AND MTBF FOR ALL COMBINATIONS OF RELIABILITY SCREENS[51]

Point Number	Reliability Level (see Legend)			Total Cost (Dollars)	MTBF (Hours)	Slope (from Pt. #1)
	Integrated Circuits	Semi-Conductors	Resistors			
1	1	1	1	11650	14409	0.0508
2	1	1	3	12142	14434	0.0508
3	1	2	1	12492	15197	0.9358
4	1	2	3	12984	15225	0.6117
5	1	3	1	12550	15825	0.3631
6	1	3	3	16042	15855	0.3293
7	2	1	1	11934	18214	13.4240
8	2	1	3	12425	18254	4.9605
9	2	2	1	12776	19493	4.5155
10	2	2	3	13268	19538	3.1711
11	2	3	1	15834	20588	1.4650
12	2	3	3	16325	20388	1.3217
13	3	1	1	13225	22711	5.2715
14	3	1	3	13717	22773	4.0472
15	3	2	1	14067	24734	4.2711
16	3	2	3	14559	24807	3.5744
17	3	3	1	17125	28441	2.1976
18	3	3	3	17617	26525	2.0306

LEGEND

1 - Military
2 - Screened MIL-STD's
3 - High Reliability

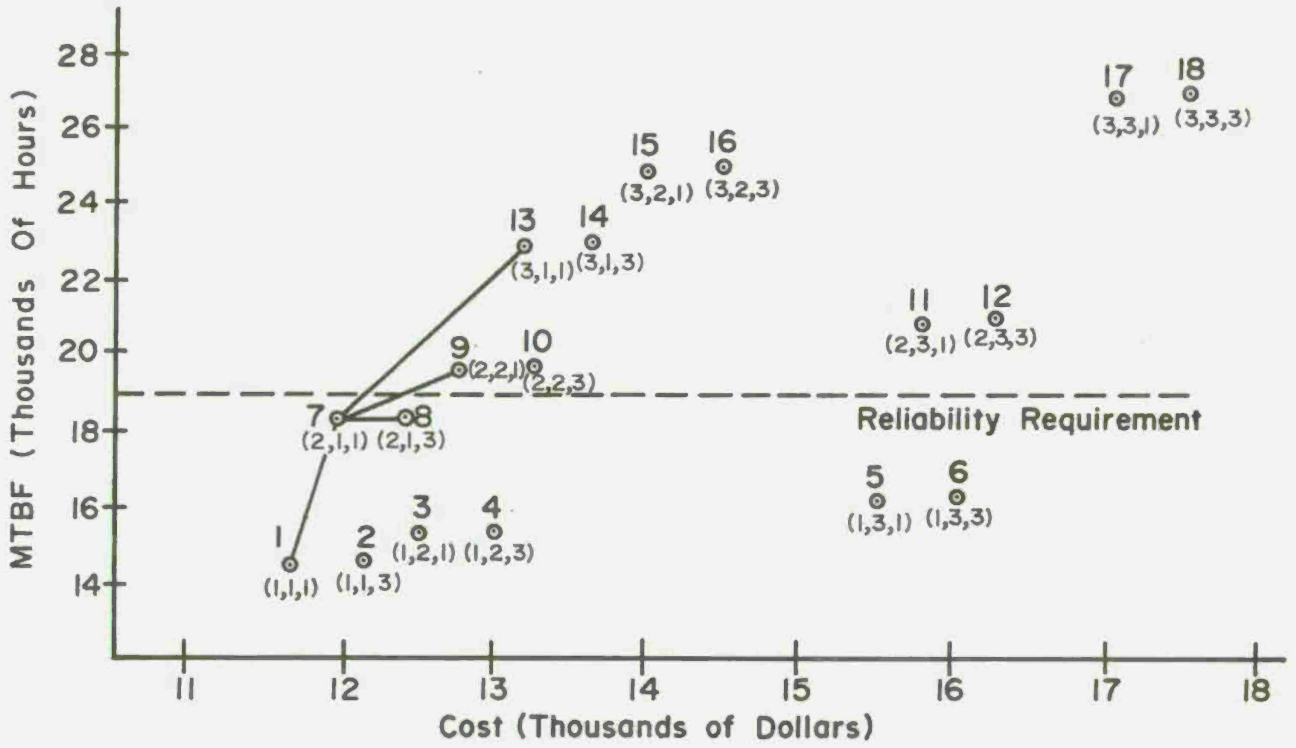


Fig. 4-90 PREDICTED MTBF VS. COST (Ref. 51)

In making cost-reliability trade-offs, all possible combinations of screening techniques on all component part types should be considered. There may be parts not yet computed which exceed the requirements at less cost.

The scatter plot is an excellent method of visualizing possible combinations of part and screen types. If the analysis indicates that no combination of screens will meet both cost and reliability criteria, redesign may be necessary. The design will be iterated and reevaluated as described in Section 4.3.2.

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APPENDIX A

DEFINITIONS, ABBREVIATIONS AND SYMBOLS

DEFINITIONS

Acceptable Quality Level (AQL)

The quality standard associated with a given producer's risk which is prescribed by the customer or quality engineer for the products on order. It is usually expressed in terms of percent defective per hundred units.

Availability

The ability of an item, under the combined aspects of its reliability and maintenance, to perform its required function at a stated instant in time.

Burn-In

The operation of items prior to their ultimate application intended to stabilize their characteristics and to identify early failures.

Characteristic, Operating

The curve which describes the probability of acceptance of a lot for various values of process average.

Defect

A characteristic which does not conform to applicable specification requirements and which adversely affects or potentially affects the quality of a device.

Degradation

A gradual deterioration in performance as a function of time.

Demonstrated

That which has been proven by the use of concrete evidence gathered under specified conditions.

Derating

The intentional reduction of stress/strength ratio in the application of an item, usually for the purpose of reducing the occurrence of stress related failures.

Downtime

The period of time during which an item is not in a condition to perform its intended function.

Effectiveness

The capability of the system or device to perform its function.

Engineering, Human

The science of studying the man-machine relationships in order to minimize the effects of human error and fatigue and thereby provide a more reliable operating system.

Engineering Quality

The science of establishing quality acceptance and evaluation criteria such as acceptance sampling plans, control charts, classification of defects, and tests.

Engineering, Reliability

The science of including those factors in the basic design which will assure the required degree of reliability.

Failure

The termination of the ability of an item to perform its required function.

Failure Analysis

The logical, systematic examination of an item or its diagrams(s) to identify and analyze the probability, causes, and consequences of potential and real failures.

Failure, Catastrophic

Failures that are both sudden and complete.

Failure, Random

Any failure whose cause and/or mechanism make its time of occurrence unpredictable, but which is predictable only in a probabilistic or statistical sense.

Failure, Wearout

A failure that occurs as a result of deterioration processes or mechanical wear and whose probability of occurrence increases with time.

Failure Law, Exponential

The exponential failure law states that the probability of survival P_S of an equipment operating for a time T is a function of the mean life, m, or of failure rate λ, as expressed by the following formulas:

$$P_S = e^{-T/M} \qquad P_S = e^{-\lambda T}$$

Failure Rate (λ)

The number of failures of an item per unit measure of life (cycles, time, etc.). During the useful life period, the failure rate, λ, is considered constant.

Fault

An attribute which adversely affects the reliability of a device.

Forced Defect

See TEST-TO-FAILURE

Freedom, Degrees Of

The number of observations that are free to vary at random, regardless of the restrictions imposed by the statistics describing the distribution.

Hazard Rate (Z(t))

At a particular time, the rate of change of the number of items that have failed divided by the number of items surviving.

Item

Item denotes any level of hardware assembly; i.e., system, subsystem, equipment, components, part, etc.

Human Factors

A body of scientific facts about human characteristics. The term covers biomedical and psychosocial considerations in the areas of human engineering, personnel selection, training, life support, job performance aid. and human performance evaluation.

Maintainability

A characteristic of design and installation which is expressed as the probability that an item will be retained in or restored to a specified condition within a given period of time, when the maintenance is performed in accordance with prescribed procedures and resources.

Maintenance

All actions necessary for retaining an item in or restoring it to a specified condition.

Maintenance, Corrective

The actions performed, as a result of failure, to restore an item to a specified condition.

Maintenance, Preventive

The actions performed in an attempt to retain an item in a specified condition by providing systematic inspection, detection and prevention of incipient failure.

Man-Function

The function allocated to the human component of a system.

Mean-Maintenance-Time

The total preventive and corrective maintenance time divided by the number of preventive and corrective maintenance actions during a specified period of time.

Mean-Time-Between-Failures (MTBF)

For a particular interval, the total functioning life of a population of an item divided by the total number of failures within the population during the measurement involved.

Mean-Time-Between-Maintenance (MTBM)

The mean of the distribution of the time intervals between maintenance actions (either preventive, corrective, or both).

Mean-Time-To-Repair

The total corrective maintenance time divided by the total number of corrective maintenance actions during a given period of time.

Quality

A measure of the degree to which a device conforms to applicable specification and workmanship standards.

Quality, Average Outgoing

The ultimate average quality of products shipped to the customer which are the result of the composite techniques of sampling and screening.

Randomness

The occurrence of an event in accordance with the laws of chance.

Redundancy

In an item, the existence of more than one means of performing its function.

Redundancy, Active

That redundancy wherein all redundant items are operating simultaneously rather than being switched on when needed.

Redundancy, Standby

That redundancy wherein the alternative means of performing the function is inoperative until needed, and is switched on upon failure of the primary means of performing the function.

Reliability

The characteristic of an item expressed by the probability that it will peform a required function under stated condition for a stated period of time.

R Growth Testing

The improvement process during which hardware reliability increases to an acceptable level.

Reliability, Inherent

The potential reliability of an item present in its design.

Reliability, Intrinsic

The probability that a device will perform its specified function, determined on the basis of a statistical analysis of the failure rates and other characteristics of the parts and components which comprise the device.

Repair

See MAINTENANCE, CORRECTIVE

Replaceability

A measure of the degree to which replacement of an item will be accomplished within a given time under specified conditions.

Risk

The probability of rendering the wrong decision based on pessimistic data or analysis.

Safety

The conservation of human life and its effectiveness, and the prevention of damage to items, consistent with mission requirements.

Screening

The process of performing 100 percent inspection on product lots and removing the defective units from the lots.

Screening Test

A test or combination of tests, intended to remove unsatisfactory items or those likely to exhibit early failures.

Step Stress Test

A test consisting of several stress levels applied sequentially for periods of equal duration to a sample. During each period, a stated stress level is applied and the stress level is increased from one step to the next.

Storage Life (Shelf Life)

The length of time an item can be stored under specified conditions and still meet specified requirements.

Stress, Component

The stresses on component parts during testing or usage which affect the failure rate and hence, the reliability of the parts. Voltage, power, temperature, and thermal environmental stress are included.

Survivability

The measure of the degree to which an item will withstand hostile man-made environment and not suffer abortive impairment of its ability to accomplish its designated mission.

System Effectiveness

A measure of the degree to which an item can be expected to achieve a set of specific mission requirements, and which may be expressed as a function of availability, dependability and capability.

Test-To-Failure

The practice of inducing increased electrical and mechanical stresses in order to determine the maximum capability of a device so that conservative usage in subsequent applications will thereby increase its life through the derating determined by these tests.

Time, Mission

That element of Uptime during which the item is performing its designated mission.

Time, Up (Uptime)

That element of active time during which an item is either alert, reacting or performing a mission.

Time, Down (Downtime)

That element of time during which the item is not in condition to perform its intended function.

Uptime Ratio

The quotient of uptime divided by Uptime plus Downtime.

Wearout

The process of attrition which results in an crease of hazard rate with increasing age (cycles, time, miles, events, etc., as applicable for the item).

ABBREVIATIONS AND SYMBOLS

AC	Acquisition Cost
AFCM	Air Force Logistics Command Manual
AFSCM	Air Force Systems Command Manual
AGE	Aerospace Ground Equipment
AQL	Acceptable Quality Level
AWACS	Airborne Warning and Control System
BIT	Built-In-Test
BITE	Built-In-Test Equipment
CMOS	Complimentary Metal Oxide Semiconductor
COO	Cost of Ownership
DTUPC	Design to Unit Production Cost
EAR	Electronically Agile Radar
ECAP	Electronic Circuit Analysis Program
EOM	Ease of Maintenance
FMEA	Failure Mode and Effects Analysis
FTA	Fault Tree Analysis
G & A	General and Administrative
LCC	Life Cycle Cost
LRU	Line Replaceable Unit
LSI	Large Scale Integration
LSC	Logistic Support Cost
MIS	Management Information System
MOS	Metal Oxide Semiconductor
MRB	Material Review Board
MTBF	Mean-Time-Between-Failures

MTBMA	Mean-Time-Between-Maintenance Actions
MTTF	Mean-Time-To-Failure
MTTR	Mean-Time-To-Repair
ORLA	Optimum Repair Level Analysis
PPL	Preferred Parts List
PPM	Parts Per Million
QC	Quality Control
RAC	Reliability Analysis Center
RADC	Rome Air Development Center
RFP	Request for Proposal
ROM	Read Only Memory
RPM	Reliability Planning and Management
SRU	Small Replaceable Unit
T_B	Burn-In-Time
TTL	Transistor-Transistor Logic
T_W	Wearout Time
TWT	Traveling Wave Tube
UPC	Unit Production Cost
WBS	Work Breakdown Strucutre
Z(t)	Hazard Rate
λ	Failure Rate

APPENDIX B

BIBLIOGRAPHY (ANNOTATED)

Reference Documents: The following documents provide additional or supporting information. A synopsis of each document is presented as it appears in the text. (NOTE: The latest issue of a document should be used when seeking reference information.)

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   The objective of this book is to develop reliability concepts and methods in a logical way, from simple components to complex systems, to give the reader a thorough understanding of the subject, and to show him how to solve reliability problems by analysis, design, and testing. There is an abundance of useful reliability formulas in the book which will help the reader predict system reliability, establish reliability goals, and determine the procedures necessary to achieve them. Also included is a quantitative treatment of system maintainability, availability, and safety and outlined methods which have to be followed.

2. Military Standardization Handbook 217B, Reliability Prediction of Electronic Equipment, Sept. 1974.

   This document, which is a revision of MIL-HDBK-217, provides two methods of reliability prediction: a) Parts Stress Analysis, and b) Parts Count. The part failure rate models have been brought up to date and models added for newer parts. Mathematical expressions for part failure rates are provided for use in computer programming. Tables, rather than curves, are used for base failure rates to improve ease of manual application of the prediction methods. These prediction methods will be continually up-dated as new information becomes available. This Handbook includes information relating to Part Stress Analysis Prediction in the areas of: a) Microelectronic Devices, b) Discrete Semiconductors, c) Tubes, Electronic Vacuum, d) Lasers, e) Resistors, f) Inductive Devices, h) Rotating Devices, i) Relays, j) Switches, k) Connectors, l) Wire and Printed Wiring Boards, and m) Miscellaneous Parts. Also covered is Parts Count Reliability Prediction. Appendices dealing with System Reliability Modeling and Approximation for Reliability Calculation, and a comprehensive bibliography are also included.

   This Handbook is oriented toward reliability prediction of military electronic equipment; it provides a common basis for predicting and comparing predictions on military contracts and proposals. It is not a complete guide to reliability engineering.

3. Myers, R., Wong, K., and Gordy, H., Reliability Engineering for for Electronic Systems, John Wiley and Sons, New York, 1964.

   This book represents an introductory treatment of reliability engineering as applied to electronic systems. Suitable for use as a text book for students or research workers, the subject matter covers fundamental concepts drawn from probability and statistics and applies them to reliability engineering. Simple problems and references are provided at the end of each chapter.

4. Vaccaro, J., and Gorton, H. (RADC and Battelle Memorial Institute), Reliability Physics Notebook, RADC-TR-65-330, AD 624-769, October, 1965.

The purpose of this Notebook is to make available to the electronics reliability engineer current state-of-the-art information relating to what may be termed the reliability physics of solid state electronic parts. It explains techniques and procedures for obtaining pertinent data on specific part types and methods of utilizing the data in accelerated testing, screening, and reliability prediction programs. Consideration is largely limited to degradation and failure mechanisms which remain after gross mechanical and quality defects have been screened out. A brief section on silicon integrated circuits is included.

5. Military Standard 785A, Reliability Program for Systems and Equipment Development and Production, March, 1969.

Establishes uniform criteria for reliability programs and provides guidelines for the preparation of reliability program plans. Lists detailed requirements as Program Elements including: (a) Reliability Management (Reliability Organization, Management and Control, Subcontractor and Supplier Reliability Program, Program Review, (b) Reliability Design and Evaluation (Design Techniques. Reliability Analysis, Parts Reliability, Failure Mode and Effect Analysis, Reliability, Critical Items, Effects of Storage, Design Reviews) (c) Reliability Testing and Demonstration (Reliability Test Plans, Development Testing, Reliability Demonstration) (d) Failure Data (Failure Data Collection Analysis and Corrective Action, Failure Summaries), (e) Production Reliability (Transition from Development, Reprocurement), (f) Status Reports.

6. Anderson, R., Kos, D., and Schiller, J., (IITRI) Reliability and Maintainability Planning Guide for Army Aviation Systems and Components, R & M Division, Directorate for Product Assurance, U.S. Army Aviation Systems Command, St. Louis, Missouri, July 1974.

This guidebook serves as a management tool to use in planning, managing and monitoring R&M programs for aviation systems. It provides specific guidelines for structuring work efforts, allocating resources and evaluating all life cycle R&M activities.

7. Study of Reliability Prediction Techniques for Conceptual Phases of Development, Final Report, Rome Air Development Center, RADC-TR-74-235, October 1974.

This report presents the results of a study to develop a reliability prediction technique to estimate system complexity for application during the early conceptual phases of system development. The prediction technique is based on system performance data derived from design specifications, detailed parts summaries, and detailed handbook predictions using MIL-HDBK-217A on existing systems.

8. Selby, J. and Miller, S., (General Electric), "Reliability Planning and Management - RPM", Symposium for Reliability and Maintainability Technology for Mechanical Systems, Washington, AOA, April, 1972.

This paper presents a new approach to the reliability planning and management of complex weapon systems. RPM is essentially a management tool for briding the gap between stated reliability requirements and implementation planning. The RPM methodology, equally usable by buyer and contractor, is applicable to establishing plans projecting effort. evaluating proposals and monitoring contract performance.

9. Research Study of Radar Reliability and Its Impact on Life Cycle Costs for the APQ-113,-114,-120, and -144 Radar Systems, General Electric Company, Aerospace Electronic Systems Department, Utica, New York, August, 1972.

The purpose of this study was to provide insight into Reliability Worth through quantifying the relative values of reliability activities and their impact on life-cycle-costs. The study is based on data obtained and analyzed for the APQ-120 and the APQ-113,-114, and -144 Radar Systems. In-service reliability performance data was gathered and analyzed for both radar families, the objective being to correlate differences in performance with the equipment reliability requirements and programs structured. The reliability disciplines and methodologies applied to these radar programs were analyzed with emphasis placed on providing measurable quantified analysis and conclusions. Recommendations are provided, based on conclusions derived from study findings, relative to reliability contracting practices, prerelease disciplines and testing programs.

10. Reliability and Maintainability Management Guide, Air Force Systems Command, AFSCP 800 Series, 1974.

This pamphlet explains how to insure appropriate levels of reliability and maintainability (R&M) over the life cycle of systems and equipments through effective management actions by staff, program office and contractor personnel.

11. Military-Standard-781B, Reliability Tests: Exponential Distribution, 1967.

Outlines test levels and test plans for reliability qualification (demonstration), reliability production acceptance (sampling) tests, and for longevity tests. (The test plans are based upon the exponential, or Poisson distribution, and are intended for the testing of equipment.) Provides uniformity in R testing by: (a) Facilitating the preparation of Military Specs and Standards through the establishment of standard test levels and test plans; (b) restricting the variety of reliability tests so that those conducting tests can establish facilities; (c) Facilitating the determination of more realistic correlation factors between test and operational reliability; and (d) facilitating the direct comparison of MTBF test results through the establishment of uniform test levels and plans. Includes graphic examples and examples of records and reports.

12. Kilpatrick, P.S., Mitchell, P.D., Scales, E.A., Aircraft Avionics Trade-off Study, Vol. II, Final Report, AD 915-881L, September, 1973.

The objective of this study was to define and evaluate modular avionics concepts and to provide data for an orderly time-phased transition to these concepts. This document presents the results from the avionics requirements definition task. The general objectives of this task were to define future avionics requirements and trends across a spectrum of Air Force operations so that the subsequent trade-offs would have a meaningful basis.

13. Miller, B., "AWG-9 Provides Multi-Target Capability", Aviation Week and Space Technology, March 12, 1973.

Presents capabilities of the AWG-9 weapon control system and how it will aid the Navy in maintaining the rigid quantitative reliability requirements on the Navy's Grumman F-14 fighter.

14. Ulsamer, E., "How Computers Will Fly Tommorrow's Airplanes," Air Force Magazine, July, 1972.

This article discusses the Air Force's concept of the "digital airplane," and presents the advantages of such a system.

15. Klass, P.J., "USAF Weighing Standardized Modules, "Aviation Week and Space Technology, September 16, 1974.

Discusses the success of the Navy's attempt at circuit-module standardization through their Standard Hardware Program (SHP), and how it might affect the USAF to consider a similar program for future airborne avionics.

16. MIL-STD-749B, Preparation and Submission of Data for Approval of Nonstanda rd Parts, August, 1969.

This standard establishes uniform procedures for the preparation and submission of data for approval of nonstandard parts prior to use in military equipment.

17. MIL-STD-891B, Contractor Parts Control and Standardization Program, April, 1974.

This standard establishes the criteria and guidelines for the preparation and implementation of a planned contractor parts control and standardization program. Includes (a) Reference Documents; (b) Definitions; (c) General Requirements; (d) Detail Requirements; (e) Equipment Performance; (f) Data and graphics designating parts selected for proposed and additional program preferred parts lists.

18. MIL-STD-1562, Lists of Standard Microcircuits, November, 1974.

The purpose of this standard is to provide equipment designers and manufacturers with lists of microcircuits considered to be most acceptable for military applications and to control and minimize the variety of microcircuits used by military activities in order to facilitate effective logistic support of equipment in the field; to maximize economic support of and to concentrate improvement on, production of the microcircuits listed in this standard.

19. MIL-STD-701J, Lists of Standard Semiconductor Devices, January, 1974.

This standard provides device characteristics, ratings and other parameters of standard semiconductors. It is intended to guide designers in the selection process for non-critical applications where an established device can be used.

20. MIL-STD-199B, Resistors, Selection and Use Of, June, 1974.

The purpose of this standard is to provide the equipment designer with a selection of standard resistors for use in most military applications; to control and minimize the variety of resistors used in military equipment in order to facilitate logistic support of the equipment in the field; and to outline criteria pertaining to the use, choice, and application of resistors in military equipment.

21. MIL-STD-198C, Capacitors, Selection and Use of, December, 1971.

This standard provides the equipment designer with a selection of standard capacitors for use in most military applicactions; controls and minimizes the variety of capacitors used in military equipment in order to facilitate logistic support of the equipment in the field; and outlines criteria pertaining to the use, choice, and application of capacitors in military equipment.

22. MIL-STD-202E, Test Methods for Electronic and Electrical Component Parts, April, 1973.

This standard establishes uniform methods for testing electronic and electrical component parts, including basic environmental tests to determine resistance to deleterious effects of natural elements and conditions surrounding military operations, and physical and electrical tests. This standard is intended to apply only to small parts, such as transformers and inductors, weighing up to 300 pounds or having a root-mean-square test voltage up to 50,000 volts unless otherwise specifically invoked.

23. MIL-STD-750, Test Methods for Semiconductor Devices, February, 1970

This standard is intended to apply only to semiconductor devices (i.e., transistors, Diodes, voltage regulators, rectifiers and tunnell diodes). The test methods described have been prepared to serve several purposes including control of laboratory conditions, control uniform methods and format of results.

24. MIL-M-38510, Microcircuits, General Specification For, October, 1973.

This specification and its supplementary slash sheets provide data and selection guidelines for microcircuits. It is intended to aid designers in selection and application of standard monolithic IC types.

25. MIL-HDBK-175, Microelectronic Device Data Handbook, May 1968

This handbook is intended as a quick-reference document for use by design engineers, technicians, parts specialists, and by contractors. The text is addressed to readers with little or no experience in microelectronics. It is intended to provide general guidance for employing the technology. Solutions to the specific problems of equipment design must be considered in the context of cost, schedule, environments, and the other constraints of a particular application and are therefore beyond the scope of this handbook. The handbook does provide general information that will be of substantial assistance in the solution of specific problems.

26. MIL-S-19500E, Semiconductor Devices, General Specification For, March, 1974.

This specification covers the general requirements for semiconductor devices used in military equipment. Specific requirements for a particular type of semiconductor device are listed in the applicable detail specificaction, which is included within the specification as slash sheets.

27. MIL-STD-1286, Transformers, Inductors and Coils, Selection and Use Of, June, 1970.

This standard provides guidelines for selection and application of inductive devices. Data and information covering classes of insulators, power ratings, etc. is provided to aid designers in selecting suitable devices.

28. MIL-STD-1346, Relays, Selection and Application Of, June, 1969.

This standard provides guidelines for the selection and application of relays. Included is information on types, styles, contact ratings and other data for reliable relay application.

29. MIL-STD-1132, Switches and Associated Hardware, Selection and Use Of, June, 1968.

Similar to MIL-STD-1346, this standard provides data and information relative to switches. Application guidelines, data and notes are provided to aid designers in proper selection.

30. MIL-STD-883, Test Methods and Procedures for Microelectronics, May, 1968.

The purpose of this standard is to establish uniform methods and procedures for testing microelectronic devices, including basic environmental tests to determine resistance to deleterious effects of natural elements and conditions surrounding military and space operations, and physical and electrical tests. For the purpose of this standard, the term "devices" includes such items as monolithic, multi-chips, film, and hybrid microcircuits, microcircuit arrays, and the elements from which the circuits and arrays are formed. This standard is intended to apply only to microelectronic devices.

This document includes a) referenced documents, b) abbreviations, symbols and definitions, c) general requirements, d) detail requirements, and test methods relating to: Environmental Tests, Mechanical Tests, Electrical Tests (digital), Electrical Tests (linear), and Test Procedures.

31. MIL-I-46058, Insulating Compound, Electrical (for coating printed circuit assemblies), February 1974.

This specification lists the properties, characteristics and qualities of insulating compounds and materials used to seal printed circuit boards from moisture entrapment, corrosion or other harmful environmental effects.

32. Klass, P.J., "Multiplex Systems to be Tested on B-1," Aviation Week and Space Technology, March 5, 1973, p. 38.

Presents the Electrical (function) Multiplexing System (E Mux), which performs electrical functions of the on/off switching type.

33. Fasano, R.M., Lemack, A.G., "A Quad Configuration--Reliability and Design Aspects," Proceedings of the 8th National Symposium on Reliability and Quality Control, January 1962.

Primarily discusses the reliability design aspects and limitations of electronic circuits in which a particular type of component redundancy called QUADing is used. Proposes that a nonredundant and a QUAD redundant circuit are analyzed to establish the magnitude of the increased reliability, effects on loading, power, terminal supplies, transient aspects, etc.

34. Barrett, L.S., Reliability Design and Application Considerations for Classical and Current Redundancy Schemes, Lockheed Missiles and Space Company, Inc., Sunnyvale, California, September 30, 1973.

This report presents a summarization of the reliability, application, and design aspects of both classical and state-of-the-art redundancy methodology and, in addition, some of the more attractive redundancy techniques currently being investigated or developed.

35. Anderson, J.E. and Macri, F.J., "Multiple Redundancy, Applications in a Computer,"

This paper presents a computer design in which the selected form of redundancy was a result of various tradeoff studies performed to yield the optimum overall design. The units are the Launch Vehicle Digital Computer and Data Adapter (LVDC/LVDA).

36. Chamow, M.F. and Smith, W.M., "Some Precepts of Reliable Electronic Design," Proceedings of 1966 Reliability and Maintainability Symposium, pp. 269-275.

Presents precepts for reliable design. The guidelines given are practical and are derived from actual experience.

37. MIL-HDBK-217A Reliability Stress and Failure Rate Data for Electronic Equipment, December 1, 1965, pp. 9-1 to 9-10.

This handbook provides essential failure rate data for electronic parts and indicates how MIL-STD-756 may be implemented using this data. The handbook was designed to improve prediction accuracy. Application K factors are included to account for the severity of the use environment.

38. Electromagnetic Pulse Handbook for Missiles and Aircraft in Flight, SC-M-71-0346, Sandia Laboratories, Albuquerque, September, 1972, pp. 311-316.

The objective of this handbook is to provide for analysis by breaking down the EMP response of an in-flight missile or aircraft, and also to provide available quantitative data (both experimentally and theoretically derived) on each of the constituent parts of the response.

39. C.R. Lennox, Experimental Results of Testing Resistors Under Pulse Conditions, Sandia Laboratories, Albuquerque, 1967.

Presents results of tests performed on three types of resistors; those being wire-wound, metal film and carbon composition; also describes testing equipment.

40. C. Case and J. Miletta, Capacitor Failure Due to High Level Electrical Transients, Harry Diamond Laboratories, Technical Note circa 1974.

This report preserts the results of tests conducted on solid tantalum capacitors of low dc voltage rating which have demonstrated failure energy levels for those type of capacitors comparable to the failure levels of low power discrete semiconductor devices and small-scale integrated circuits, and describes the failure characteristics of the solid tantalum devices and other typical capacitor types. These capacitor failure levels are compared to typical failure levels of semiconductor devices.

41. Standard Workmanship Manual, OAM001, Singer Aerospace & Marine Systems, June 1971.

This manual serves as a compilation of acceptable Workmanship methods, procedures, practices and aids for use in the manufacture of electronic products.

42. Standard Printed Wiring Practices, ESP18, The Singer Company Kearfoot Division, October, 1971.

The purpose of this document is to insure that all printed wiring designs represent the highest quality consistent with current economically sound manufacturing procedures.

43. Engineering Design Handbook, Maintainability Guide for Design, Army Materiel Command, October, 1972 AD754-202.

The objective of this hardbook is to influence design so that equipment can be (1) serviced efficiently and effectively if servicing is required, and repaired efficiently and effectively if it should fail, (2) operable for the period of intended life without failing and without servicing, if possible. This handbook embraces information on the extent and nature of the Maintainance Problems as it exists today and the principles and techniques that, if included in future design, will reduce this problem.

44. Maintainability Principles and Practices, B.S. Blanchard and E. E. Lowery, McGraw-Hill Book Company, New York, 1969.

This book is an introduction to maintainability engineering. Its focus throughout is on the principles and practices of organization, planning, actuation, and control of a company maintainability program. This book is primarily designed for use in courses at either the undergraduate or graduate level.

45. Investigation of Secondary Effects for the Checkout of Nonelectronic Systems, Air Force Aero Propulsion Laboratories Research and Technology Division, AFAPL-TR-65-57, August, 1965.

The main objectives of this investigation was to demonstrate the feasibility of sensing secondary phenomena of nonelectronic system operation and to obtain information concerning the status of the system or its components. The primary emphasis has been on secondary effects not requiring the physical dismantling of the system under test and not currently employed in existing checkout operations.

46. Secondary Effect Technique Study, U.S. Army Armament Command, FCF-13-74, June, 1974.

The object of this program was to identify and develop secondary effect detection technique concepts for use with the MAID-TECH Program. The purpose of these techniques is to simplify checkout procedures and to provide information that cannot be easily obtained through primary measurements.

47. Gansler, J.S. and Sutherland, G.W. (DoD), A Design to Cost Overview Defense Management Journal, September, 1974.

This article presents a philosophy of design-to-cost, applicable to the DoD. The need for principles, commercial practice, life cycle cost considerations, characteristic features, application, and the relationship to DoD decision process are covered, as well as the challenge to DoD and the defense industry. Also presented is a hypothetical design to cost program.

48. McColl, D.R.S. (Deputy for Advanced Technology-SAFRD), Remarks Before the Windy City Old Crows Assn., Chicago, Illinois, September 19, 1974.

This paper presents the matter of increasing complexity of weapons and their higher costs, and the effect this has on purchasing equipment. Pointed out is the design to cost approaches taken by the Air Force to alleviate this major problem.

49. Unit Product Cost System, Honeywell Aerospace Division, St. Petersburg, Florida,

This pamphlet provides informative data related to a Unit Product Cost System. The design is broken down into four phases, those being: Phase I - Preliminary Design, Phase II-Design, Phase III-Pilot Production, and Phase IV-Production. The data is presented in the form of diagrams, flow charts and work sheets.

50. Deger, E. and Jobe, T., (RCA Corporation, Consumer Electronics, Indianapolis, IN.), "For the Real Cost of a Design, Factor in Reliability", Electronics, August 30, 1973.

Presents a method of figuring total reliability costs into design tradeoffs. Includes information on the economics of reliability, reliability data sources, a guide to transistor reliability, adding components for lower total cost, guidelines in actual practice, reliability compared to modular design, and presently used reliability data.

51. Starr, M.K. (Graduate School of Business, Columbia University), Product Design and Decision Theory, Prentice-Hall, Inc., Englewood Cliffs, N.J., 1963.

This book attempts to explain the nature of decision theory and how it can be utilized to improve design decisions. Many different kinds of design situations are presented, but the surface of possibilities has only been scratched. Extensive detail has been avoided in presenting the examples for lack of space. This book has been planned so that, all members of the design team as well as students of engineering, production, marketing, and management can obtain a different point of view about the product design problem.

52. Jones, E.R. (Wakefield Eng. Inc.), A Guide to Component Burn-in Technology, Wakefield Engineering, Inc., 1972.

The purpose of this booklet is to help explain why and how reduction in failures is accomplished and how this accomplishment relates to test time, costs and certain procedural considerations.

53. "Cost Versus Reliability Trade-Off", Proceedings of the 1967 Annual Symposium on Reliability, Washington, D.C., January 1967.

Presents a technique for achieving a higher required reliability at minimum possible cost.

APPENDIX C

COMPARATIVE FAILURE RATES FOR MONOLITHIC MICROCIRCUITS

(Standard Types from MIL-STD-1562)

Each device type is defined in the appropriate slash sheets of MIL-M-38510)

TTL and NAND Gates, Inverters and Buffers

Commercial or Generic Number	Specification MIL-M-38510/	Device Type	Circuit Description	$F/10^6$ hrs
5400	1	04	Quad, 2-input NAND gate	0.060*
54H00	23	04	Quad, 2-input (high speed) NAND gate	0.064
54L00	20	04	Quad, 2-input (low power) NAND gate	0.068
54S00	70	01	Quad, 2-input (Schottky) NAND gate	0.064
5401	1	07	Quad, 2-input NAND gate (open collector output)	0.056
54L01	20	06	Quad, 2-input NAND gate (open collector output)(low power)	0.052
54H01	23	06	Quad, 2-input NAND gate (open collector output)(high speed)	0.052
5403	1	09	Quad, 2-input, open collector NAND gate	0.056
54L03	20	06	Quad, 2-input, open collector (low power) NAND gate	0.052
54S03	70	02	Quad, 2-input, open collector (Schottky) NAND gate	0.056
5404	1	05	Hex inverter	0.072
54H04	23	05	Hex inverter (high speed)	0.076
54L04	20	05	Hex inverter (low power)	0.072
54S04	70	03	Hex inverter (Schottky)	0.076
5405	1	08	Hex inverter, open collector	0.064
54S05	70	04	Hex inverter, open collector (Schottky)	0.064
5406	8	01	Inverter/buffer driver, 30-volt output	0.072
5407	8	03	Buffer driver, 30-volt output	0.064
5408	16	01	Quad, 2-input AND gate	0.064
5409	16	02	Quad, 2-input, open collector AND gate	0.060

*Assumption, stress levels and other ground rules used to calculate the failure rates are given at the end of this appendix.

TTL and NAND Gates, Inverters and Buffers (Cont'd)

Commercial or Generic Number	Specification MIL-M-38510/	Device Type	Circuit Description	F/10^6 hrs
5410	1	03	Triple, 3-input NAND gate	0.056
54H10	23	03	Triple, 3-input (high speed) NAND gate	0.060
54L10	20	03	Triple, 3-input (low power) NAND gate	0.056
54S10	70	05	Triple, 3-input (Schottky) NAND gate	0.060
5412	1	06	Triple, 3-input, open collector NAND gate	0.052
5420	1	02	Dual, 4-input NAND gate	0.052
54H20	23	02	Dual, 4-input (high speed) NAND gate	0.052
54L20	20	02	Dual, 4-input (low power) NAND gate	0.052
54S20	70	06	Dual, 4-input (Schottky) NAND gate	0.052
54H22	23	07	Dual, 4-input NAND gate (open collector output)(high speed)	0.044
54S22	70	07	Dual, 4-input NAND gate (open collector output)(Schottky)	0.044
5430	1	01	Single, 8-input NAND gate	0.032
43H30	23	01	Single, 8-input (high speed) NAND gate	0.044
54L30	20	01	Single, 8-input (low power) NAND gate	0.032
54S30	70	03	Single, 8-input (Schottky) NAND gate	0.044
5437	3	02	Quad, 2-input NAND buffer	0.060
5438	3	03	Quad, 2-input (open collector) NAND buffer	0.052
5440	3	01	Dual, 4-input NAND buffer	0.060
54H40	24	01	Dual, 4-input (high speed) NAND buffer	0.052
54S40	72	01	Dual, 4-input (Schottky) NAND buffer	0.052

TTL or NOR Gates

Commercial or Generic Number	Specification MIL-M-38510/	Device Type	Circuit Description	$F/10^6$ hrs
5402	4	01	Quad, 2-input NOR gate	0.064
54L02	27	01	Quad, 2-input NOR gate (low power)	0.068
54S02	73	01	Quad, 2-input NOR gate (Schottky)	0.072
5423	4	02	Dual, 4-input with strobe and expandable input NOR gate	0.060
5425	4	03	Dual, 4-input NOR gate with strobe	0.060
5427	4	04	Triple, 3-input NOR gate	0.064
5450	5	01	Expandable, dual 2-wide, 2-input AND-OR invert gate	0.052
54H50	40	01	Expandable, dual 2-wide, 2-input AND-OR invert gate (hi-spd)	0.056
5451	5	02	Dual, 2-wide, 2-input AND-OR invert gate	0.052
54L51	41	01	Dual, 2-wide, 2-input AND-OR invert gate (low power)	0.052
54H51	40	02	Dual, 2-wide, 2-input AND-OR invert gate (high speed)	0.052
54S51	74	01	Dual, 2-wide, 2-input AND-OR invert gate (Schottky)	0.056
5453	5	03	Expandable, 4-wide, 2-input AND-OR invert gate	0.052
54H53	40	03	Expandable, 4-wide, 2-input AND-OR invert gate (high speed)	0.052
5454	5	04	4-wide, 2-input AND-OR invert gate	0.052
54H54	40	04	4-wide, 2-input AND-OR invert gate (high speed)	0.052
54L54	41	02	4-wide, 2-input AND-OR invert gate (low power)	0.052
54H55	40	05	Expandable, 2-wide, 4-input AND-OR invert gate (high speed)	0.044
54L55	41	03	Expandable, 2-wide, 4-input AND-OR invert gate (low power)	0.044
54S64	74	02	4-2-3-2 input AND-OR invert gate	0.052

TTL or NOR Gates (Cont'd)

Commercial or Generic Number	Specification MIL-M-38510/	Device Type	Circuit Description	$F/10^6$ hrs
54S65	74	03	4-2-3-2 input, open collector AND-OR invert gate (Schottky)	0.052
5486	7	01	Quad, 2-input, exclusive-OR gate	0.084
54L86	26	01	Quad, 2-input, exclusive-OR gate (low power)	0.044

TTL Adders

5482	6	01	2-bit, full adder	0.044
5483	6	02	4-bit, full adder	0.112
9304	6	03	Dual, full adder	0.092

TTL ALU

9341	11	01	ALU/function generator	0.180
9342	11	02	Lookahead carry generator	0.092
54181	11	01	ALU/function generator	0.180
54182	11	02	Lookahead carry generator	0.092

TTL Flip-Flops, Multivibrators and Latches

Commercial or Generic Number	Specification MIL-M-38510/	Device Type	Circuit Description	$F/10^6$ hrs
5470	2	06	Single, edge-triggered J-K flip-flop	0.068
5472	2	01	Single, J-K master slave flip-flop	0.064
54H72	22	01	Single, J-K master slave flip-flop (high speed)	0.060
54L72	21	02	Single, J-K master slave flip-flop (low power)	0.064
5473	2	02	Dual, J-K master slave, no preset flip-flop	0.084
54H73	22	02	Dual, J-K master slave, no preset flip-flop (high speed)	0.084
54L73	21	03	Dual, J-K master slave, no preset flip-flop (low power)	0.084
5474	2	05	Dual, D-type, edge triggered flip-flop	0.072
54H74	22	03	Dual, D-type, edge triggered flip-flop (high speed)	0.088
54L74	21	05	Dual, D-type, edge triggered flip-flop (low power)	0.076
54S74	71	01	Dual, D-type, edge triggered flip-flop (Schottky)	0.084
5475	15	01	4-bit, bistable latch, complementary outputs	0.092
5476	2	04	Dual, J-K, master-slave flip-flop	0.084
54H76	22	04	Dual, J-K, master slave flip-flop (high speed)	0.076
5477	15	02	4-bit latch	0.084
54L78	21	04	Dual, J-K, master slave flip-flop (low power)	0.084
5479	2	07	Dual, D-type, edge triggered, buffered output flip-flop	0.084
54H101	22	05	Single, edge triggered, J-K flip-flop (high speed)	0.072
54H103	22	06	Dual, J-K edge triggered flip-flop (high speed)	0.092
54S112	71	02	Dual, J-K edge triggered flip-flop (Schottky)	0.084

TTL Flip-Flops, Multivibrators and Latches (Cont'd)

Commercial or Generic Number	Specification MIL-M-38510/	Device Type	Circuit Description	$F/10^6$ hrs
54S113	71	03	Dual, J-K edge triggered flip-flop (Schottky	0.084
54S114	71	04	Dual, J-K edge triggered flip-flop (Schottky)	0.084
54116	15	03	Dual, 4-bit latch	0.092
54121	12	01	Single monostable multivibrator	0.068
54122	12	02	Single, retriggerable with clear monostable multivibrator	0.068
54123	12	03	Dual, retriggerable with clear monostable multivibrator	0.092
54174	17	01	Hex, D-type, positive-edge flip-flop triggered with clear and single outputs	0.152
54S174	71	05	Hex, D-type, positive-edge flip-flop triggered with clear and single outputs (Schottky)	0.152
54175	17	02	Quad, D-type, positive-edge flip-flop triggered with clear and complementary outputs	0.120
54S175	71	06	Quad, D-type, positive-edge flip-flop triggered with clear and complementary outputs (Schottky)	0.112
9308	15	03	Dual, 4-bit latch	0.092
9314	15	04	4-bit, master reset latch	0.100

TTL Shift Registers

Commercial or Generic Number	Specification MIL-M-38510/	Device Type	Circuit Description	$F/10^6$ hrs
5495	9	01	4-bit, right shift, left shift	0.100
54L95	28	01	4-bit, right shift, left shift (low power)	0.100
5496	9	02	5-bit	0.108
54164	9	03	8-bit, parallel-out, serial	0.112
54L164	28	02	8-bit, parallel-out, serial (low power)	0.112
54165	9	04	8-bit, parallel load	0.120
54194	9	05	4-bit, bidirectional	0.120
54195	9	06	4-bit, parallel access	0.112
76L70	28	05	8-bit, parallel-out, serial (low power)	0.120
93L00	28	04	4-bit (low power)	0.100
93L28	28	03	Dual, 8-bit (low power)	0.092

TTL Decoders

5442	10	01	BCD to decimal	0.100
54L42	29	01	BCD to decimal (low power)	0.100
5443	10	02	Excess-3 to decimal	0.100
54L43	29	02	Excess-3 to decimal (low power)	0.100
5444	10	03	Excess-3 gray-to-decimal	0.100
54L14	29	03	Excess-3 gray-to-decimal (low power)	0.100
5445	10	04	BCD to decimal decoder/driver (open collector)	0.100
5446	10	06	BCD to 7-segment decoder/driver (open collector)	0.100
54L46	29	04	BCD to 7-segment decoder/driver (open collector)(low power)	0.100
5448	10	08	BCD to 7-segment decoder/driver	0.100
5449	10	09	BCD to 7-segment decoder/driver (open collector)	0.092

TTL Counters

Commercial or Generic Number	Specification MIL-M-38510/	Device Type	Circuit Description	$F/10^6$ hrs
5490	13	07	High speed	0.100
54L90	25	01	High speed decade (low power)	0.120
5492	13	01	Divide-by-12	0.088
5493	13	02	4-bit binary	0.092
54L93	25	02	4-bit binary (low power)	0.088
54162	13	05	Synchronous 4-bit decade (synchronous clear)	0.120
54163	13	04	Synchronous 4-bit binary (synchronous clear)	0.120
54192	13	08	Synchronous 4-bit up/down decade	0.152
54193	13	09	Synchronous 4-bit up/down binary	0.140

TTL Data Selectors/Multiplexers

54150	14	01	16-input with enable	0.108
54153	14	03	Dual, 4-input with enable	0.100
9309	14	04	Dual, 4-input without enable	0.068
9312	14	02	8-input with enable	0.084
9322	14	05	Quad, 2-input with enable	0.084

CMOS NAND Gates, Buffers, Inverters, and AND-OR Select Gates

4007A	53	01	Dual, complementary pair plus inverter	0.044
4011A	50	01	Quad, 2-input NAND gate	0.056
4012A	50	02	Dual, 4-input NAND gate	0.056
4019A	53	02	Quad, AND-OR select gate	0.072
4023A	50	03	Triple, 3-input NAND gate	0.064
4049A	55	03	Inverting hex buffer	0.052
4050A	55	04	Non-inverting hex buffer	0.068

CMOS Flip-Flops

Commercial or Generic Number	Specification MIL-M-38510/	Device Type	Circuit Description	$F/10^6$ hrs
4013A	51	01	Dual, D-type, edge triggered	0.104
4027A	51	02	Dual, J-K, master slave	0.112

CMOS NOR Gates

4000A	52	01	Dual, 3-input plus inverter	0.056
4001A	52	02	Quad, 2-input	0.056
4002A	52	03	Dual, 4-input	0.056
4025A	52	04	Triple, 3-input	0.064

CMOS Adders

4008A	54	01	4-bit full adder	0.152

CMOS Counters/Dividers

4017A	56	01	Decade counter/divider	0.232
4018A	56	02	Presettable divide-by-N counter	0.256
4020A	56	03	14-stage ripple-carry binary counter/divider	0.344
4022A	56	04	Divide-by-S counter/divider	0.200
4024A	56	05	7-stage binary counter	0.200

CMOS Static Shift Registers

Commercial or Generic Number	Specification MIL-M038510	Device Type	Circuit Description	$F/10^6$ hrs
4006A	57	01	Dual, 4-stage/dual 5-stage	0.320
4014A	57	02	8-stage synchronous parallel or serial input/serial output	0.256
4015A	57	03	Dual, 4-stage serial input/parallel output	0.256
4021A	57	04	8-stage asynchronous parallel input/serial output	0.256
4031A	57	05	64-stage	0.232

Programmable ROM

HYPROM 512	201	01	512-bit	0.280

Bipolar Operational Amplifiers

741	101	01	Single, internally compensated	0.144
747	101	02	Dual, internally compensated	0.136
LM101A	101	03	Single, externally compensated	0.120
LM10SA	101	04	Single, externally compensated	0.152
LM102	106	01	Voltage follower	0.112
LM110	106	02	Voltage follower, high speed	0.112

Bipolar Voltage Regulators

723	102	01	Precision	0.112
LM109	107	01	5-volt	0.112

Bipolar Voltage Comparators

Commercial or Generic Number	Specification MIL-M-38510/	Device Type	Circuit Description	$F/10^6$ hrs
710	103	01	Single, differential	0.120
711	103	02	Dual channel, differential	0.112
LM106	103	03	Single, comparator/buffer	0.096
LM111	103	04	Precision, comparator/buffer	0.120

Bipolar Line Drivers and Receivers

55107	104	01	Dual, line receiver	0.144
55108	104	02	Dual, line receiver, open collector output	0.136
55113	104	05	Dual, differential line driver (3-state output)	0.184
55114	104	03	Dual, differential line driver (2-state output)	0.208
55115	104	04	Dual, differential line receiver	0.176
9614	104	03	Dual, differential line driver (2-state output)	0.208
9615	104	04	Dual, differential line receiver	0.176

ECL NOR Gates

10501	60	01	Quad, OT/NOR with strobe	0.080
10502	60	02	Triple, NOR, single OR/NOR	0.080
10505	60	03	Triple, 2-3-2 OR/NOR	0.080
10506	60	04	Triple, 3-4-3 NOR	0.076
10507	60	05	Triple, exclusive OR/NOR	0.088
10509	60	06	Dual, 4-5 OR/NOR	0.072

CMOS

Generic Number	Military Number	Table	Circuit Description	$F/10^6$
4000A	/05201	II-B	Dual, 3-input plus inverter NOR gates	0.056
4001A	/05202	II-B	Quad, 2-input NOR gates	0.056
4002A	/05203	II-B	Dual, 4-input NOR gates	0.056
4006A	/05701	II-E	Dual, 4-stage/dual 5-stage static shift register	0.320
4007A	/05301	II	Dual, complementary pair plus inverter	0.044
4008A	/05401	II-C	4-bit full adder	0.152
4011A	/05001	II	Quad, 2-input NAND gate	0.056
4012A	/05002	II	Dual, 4-input NAND gate	0.056
4013A	/05101	II-A	Dual, D-type, edge triggered flip-flop	0.104
4014A	/05702	II-E	8-stage, synchronous parallel or serial input/serial output static shift register	0.256
4015A	/05703	II-E	Dual, 4-stage serial input/parallel output static shift register	0.256
4017A	/05601	II-D	Decade counter/divider	0.232
4018A	/05602	II-D	Presettable divide-by-N counter	0.256
4019A	/05302	II	Quad, AND-OR select gate	0.072
4020A	/05603	II-D	14-stage ripple-carry binary counter/divider	0.344
4021A	/05704	II-E	8-stage asynchronous parallel input/serial output static shift register	0.256
4022A	/05604	II-D	Divide-by-S counter/divider	0.200
4023A	/05003	II	Triple, 3-input NAND gate	0.064

CMOS (Cont'd)

Generic Number	Military Number	Table	Circuit Description	$F/10^6$
4024A	/05605	II-D	7-stage binary counter	0.200
4024A	/05204	II-B	Triple, 3-input NOR gates	0.064
4027A	/05102	II-A	Dual, J-K, master-slave flip-flop	0.112
4031A	/05705	II-E	64-stage static shift register	0.232
4019A	/05503	II	Inverting hex buffer	0.052
4050A	/05501	II	Non-inverting hex buffer	0.068

ECL

10501	/06001	V	Quad, OR/NOR with strobe	0.080
10502	/06002	V	Triple, NOR, single OR/NOR, single OT/NOR gate	0.080
10505	/06003	V	Triple, 2-3-2 OR/NOR gate	0.080
10506	/06004	V	Triple, 3-4-3 NOR gate	0.076
10507	/06005	V	Triple, exclusive OR/NOR gate	0.088
10509	/06006	V	Dual, 4-5 OR/NOR gate	0.072

Linear Devices

Generic Number	Military Number	Table	Circuit Description	$F/10^6$
710	/10301	IV-B	Single, differential voltage comparator	0.120
711	/10302	IV-B	Dual channel, differential voltage comparator	0.112
723	/10201	IV-A	Precision voltage regulator	0.112
741	/10101	IV	Single, internally compensated operational amplifier	0.144
747	/10102	IV	Dual, internally compensated operational amplifier	0.124
55107	/10401	IV-C	Dual, line receiver	0.144
55108	/10402	IV-C	Dual, line receiver, open collector output	0.144
55113	/10405	IV-C	Dual, differential line driver	0.184
55114	/10403	IV-C	Dual, differential line driver (2-state output)	0.208
55115	/10404	IV-C	Dual, differential line receiver	0.176
9614	/10403	IV-C	Dual, differential line driver	0.208
9615	/10404	IV-C	Dual, differential line receiver	0.176
LM101A	/10103	IV	Single, externally compensated operational amplifier	0.120
LM102	/10601	IV	Voltage follower operational amplifier	0.112
LM106	/10303	IV-B	Single, comparator/buffer voltage	0.096
LM108A	/10104	IV	Single, externally compensated operational amplifier	0.152
LM109A	/10701	IV-A	5-volt voltage regulator	0.112
LM110	/10602	IV	Voltage follower, high speed operational amplifier	0.112
LM111	/10304	IV-B	Precision, comparator/buffer voltage comparator	0.120

TTL Medium Speed/Power	TTL Low Power	TTL High Speed	TTL Schottky	Circuit Description	$F/10^6$
5400 /00104 I	54L00 /02004 I	54H00 /02304 I	54S00 /07001 I	Quad, 2-input NAND gate	0.060
5401 /00107 I	54L01 /02006 I	54H01 /02306 I		Quad, 2-input NAND gate (open collector output)	0.56
5402 /00401 I-B	54L02 /02701 I-B		54S02 /07301 I-B	Quad, 2-input NOR gate	0.064
5403 /00109 I	54L03 /02006 I		54S03 /07002 I	Quad, 2-input, open collector NAND gate	0.056
5401 /00105 I	54L04 /02305 I	54H04 /07005 I	54S04 /07003 I	Hex inverter	0.072
5405 /00108 I			54S05 /07004 I	Hex inverter, open collector	0.064
5406 /00501 I				Inverter/buffer driver, 30 volt output	0.072
5407 /00803 I				Buffer driver, 30-volt output	0.064
5408 /01601 I				Quad, 2-input AND gate	0.064

TTL Medium Speed/Power	TTL Low Power	TTL High Speed	TTL Schottky	Circuit Description	F/10^6
5409 /01602 I				Quad, 2-input, open collector AND gate	0.060
5410 /00103 I	54L10 /02003 I	54H10 /02303 I	54S10 /07005 I	Triple, 3-input NAND gate	0.056
5412 /00106 I				Triple, 3-input, open collector NAND gate	0.052
5420 /00102 I	54L20 /02002 I	54H20 /02302 I	54S20 /07006 I	Dual, 4-input NAND gate	0.052
		54H22 /02307 I	54S22 /07007 I	Dual, 4-input NAND gate (open collector output)	0.044
5423 /00402 I-B				Dual, 4-input with strobe and expandable input NOR gate	0.060
5425 /00403 I-B				Dual, 4-input NOR gate with strobe	0.060
5427 /00404 I-B				Triple, 3-input NOR gate	0.064
5430 /00101 I	54L30 /02001 I	54H30 /02301 I	54S30 /07008 I	Single, 8-input NAND gate	0.032

TTL Medium Speed/Power	TTL Low Power	TTL High Speed	TTL Schottky	Circuit Description	$F/10^6$
5437 /00302 I				Quad, 2-input NAND buffer	0.060
5438 /00303 I				Quad, 2-input (open collector) NAND buffer	0.052
5440 /00301 I		54H40 /02401 I	54S40 /07201 I	Dual, 4-input NAND buffer	0.060
5442 /01001 I-F	54L42 /02901 I-F			BCD to decimal decoder	0.100
5443 /01002 I-F	54L43 /02902 I-F			Excess -3 to decimal decoder	0.100
5444 /01003 I-F	54L44 /02903 I-F			Excess -3 gray-to-decimal decoder	0.100
5445 /01004 I-F				BCD to decimal decoder/driver (open collector)	0.100
5446 /01006 I-F	54L46 /02904 I-F			BCD to 7 segment decoder/driver (open collector)	0.100
5448 /01008 I-F				BCD to 7 segment decoder/driver	0.100

TTL Medium Speed/Power	TTL Low Power	TTL High Speed	TTL Schottky	Circuit Description	F/10^6
5449 /01009 I-F				BCD to 7 segment decoder/driver (open collector)	0.092
5450 /00501 I-B		54H50 /04001 I-B		Expandable, dual 2-wide, 2-input AND-OR invert gate	0.052
5451 /00502 I-B	54L51 /04101 I-B	54H51 /04002 I-B	54S51 /07401 I-B	Dual, 2-wide, 2-input AND-OR invert gate	0.052
5453 /00503 I-B		54H53 /04003 I-B		Expandable, 4-wide, 2-input AND-OR invert gate	0.052
5454 /00504 I-B	54L54 /04102 I-B	54H54 /04004 I-B		4-wide, 2-input AND-OR invert gate	0.052
	54L55 /04103 I-B	54H55 /04005 I-B		Expandable, 2-wide, 4-input AND/OR invert gate	0.044
			54S64 /07402 I-B	4-2-3-2 input AND-OR invert gate	0.052
			54S65 /07403 I-B	4-2-3-2 input, open collector AND-OR invert gate	0.052
5470 /00206 I-A				Single, edge-triggered J-K flip-flop	0.068

TTL (Cont'd)

TTL Medium Speed/Power	TTL Low Power	TTL High Speed	TTL Schottky	Circuit Description	$F/10^6$
5472 /00201 I-A	54L72 /02102 I-A	54H72 /02201 I-A		Single, J-K master-slave flip-flop	0.064
5473 /00202 I-A	54L73 /02103 I-A	54H73 /02202 I-A		Dual, J-K, master-slave, no preset flip-flop	0.084
5474 /00205 I-A	54L74 /02105 I-A	54H74 /02203 I-A	54S74 /07101 I-A	Dual, D-type, edge-triggered flip-flop	0.072
5475 /01501 I-A				4-bit, bistable latch, complementary outputs	0.092
5476 /00204 I-A		54H76 /02204 I-A		Dual, J-K, master-slave flip-flop	0.084
5477 /01502 I-A				4-bit latch	0.084
	54L78 /02104 I-A			Dual, J-K, master-slave flip-flop	0.084
5479 /00207 I-A				Dual, D-type, edge triggered buffered output flip-flop	0.084
5482 /00601 I-C				2-bit, full adder	0.044

TTL (Cont'd)

TTL Medium Speed/Power	TTL Low Power	TTL High Speed	TTL Schottky	Circuit Description	$F/10^6$
5483 /00602 I-C				4-bit, full adder	0.112
5486 /00701 I-B	54L86 /02601 I-B			Quad, 2-input, exclusive-OR gate	0.084
5490 /01307 I-G	54L90 /02501 I-G			High-speed decade counter	0.100
5492 /01301 I-G				Divide-by-12 counter	0.088
5493 /01302 I-G	54L93 /02502 I-G			4-bit binary counter	0.092
5495 /00901 I-E	54L95 /02801 I-E			4-bit, right shift, left shift register	0.100
5496 /00902 I-E				5-bit shift register	0.108
		54H101 /02205 I-A		Single, edge-triggered J-K flip-flop	0.084
		54H103 /02206 I-A		Dual, J-K edge-triggered flip-flop	0.072

TTL (Cont'd)

TTL Medium Speed/Power	TTL Low Power	TTL High Speed	TTL Schottky	Circuit Description	$F/10^6$
			54S112 /07102 I-A	Dual, J-K edge-triggered flip-flop	0.084
			54S113 /07103 I-A	Dual, J-K edge-triggered flip-flop	0.084
			54S114 /07104 I-A	Dual, J-K edge-triggered flip-flop	0.084
54116 /01503 I-A				Dual, 4-bit latch	0.092
54121 /01201 I-A				Single, monostable multivibrator	0.068
54122 /01202 I-A				Single, retriggerable with clear monostable multivibrator	0.068
54123 /01203 I-A				Dual, retriggerable with clear monostable multivibrator	0.092
54150 /01401 I-H				16-input with enable data selector/ multiplexer	0.108
54153 /01403 I-H				Dual, 4-input with enable data selector/ multiplexer	0.100

TTL (Cont'd)

TTL Medium Speed/Power	TTL Low Power	TTL High Speed	TTL Schottky	Circuit Description	F/10^6
54162 /01305 I-G				Synchronous 4-bit decade (synchronous clear) counter	0.120
54163 /01304 I-G				Synchronous 4-bit binary (synchronous clear) counter	0.120
54164 /00903 I-E	54L64 /02802 I-E			8-bit, parallel-out, serial shift register	0.112
54165 /00904 I-E				8-bit, parallel load shift register	0.120
54174 /01701 I-A			54S174 /07105 I-A	Hex, D-type, positive-edge flip-flop triggered with clear and single outputs	0.120
54175 /01702 I-A			54S175 /07106 I-A	Quad, D-type, positive-edge flip-flop triggered with clear and complementary outputs	0.120
54181 /01101 I-D				ALU/function generator	0.180
54182 /01102 I-D				Lookahead carry generator	0.092
54192 /01308 I-G				Synchronous 4-bit up/down decade counter	0.152

TTL Medium Speed/Power	TTL Low Power	TTL High Speed	TTL Schottky	Circuit Description	F/10^6
54193 /01309 I-G				Synchronous 4-bit up/down binary counter	0.140
54194 /00905 I-E				4-bit, bidirectional shift register	0.120
54195 /00906 I-E				4-bit, parallel access shift register	0.112
	76L70 /02805 I-E			8-bit, parallel-out, serial shift register	0.120
	93L00 /02804 I-E			4-bit shift register	0.100
9304 /00603 I-C				Dual, full adder	0.092
9308 /01503 I-A				Dual, 4-bit latch	0.092
9309 /01404 I-H				Dual, 4-input without enable data selector/multiplexer	0.068
9312 /01402 I-H				8-input with enable data selector/ multiplexer	0.084

TTL (Cont'd)

TTL Medium Speed/Power	TTL Low Power	TTL High Speed	TTL Schottky	Circuit Description	F/10^6
9314 /01504 I-A				4-bit, master reset latch	0.100
9322 /01405 I-H				Quad, 2-input with enable data selector/multiplexer	0.084
	93L28 /02803 I-E			Dual, 8-bit shift register	0.092
9341 /01101 I-D				ALU/function generator	0.180
9342 /01102 I-D				Lookahead carry generator	0.092

Memory Devices

Generic Number	Military Number	Table	Circuit Description	F/10^6
HYPROM.512	/20101	III	512-bit PROM	0.280

Assumption for Failure Rate Calculations

The following assumptions were made in failure rate computations.

1. $\pi_Q = 2$, $\pi_E^* = 4$, $\pi_L = 1$, $T_A = 25^oC$

2. Where the number of transistors (NT) < 120, $T_J = 10^oC + T_A$; and where $N_T > 120$, $T_J = 25^oC + T_A$. Hence, π_T values are $\pi_{T_1} = 0.17$ and 0.35; $\pi_{T_2} = 0.24$ and 0.82, respectively.

3. Where more than one circuit configuration exists, worst case complexity was used.

*π_E = Airborne Inhabited Environment

APPENDIX D

CHARACTERISTICS AND FAILURE RATES OF STANDARD ELECTRON TUBES

Table I TUBES APPROVED FOR USE IN MILITARY EQUIPMENT

Cathode Ray-Electrostatic Deflection and Focus

Type No.	Ip mA mAdc* Maximum	Maximum Anode Voltage Eb1 Vdc	Maximum g1 Cutoff V	MIL-E-1/ Specification Sheet No.	$F/10^6$ hrs
1DP7	220*	300	95	1204	15
1DP11	220*	300	95	1204	15
3ACP1A	660	1500	- 75	311	15
3ACP7A	660	1500	- 75	311	15
3ADP2	660*	1100	- 87	974	15
3ADP7	660*	1100	- 87	974	15
3ADP11	660*	1100	- 87	974	15
3SP1	660	1100	-101	502	15
3WP1	660	1100	- 75	267	15
4MP1	660*	1100	- 87	1296	15
5ADP1	660	1100	- 56	689	15
5ADP7	660	1100	- 75	689	15
5AFP1	660	1750	- 75	1048	15
5AFP7	660	1750	- 75	1048	15
5AQP7	660	1650	- 79	1133	15
5BFP7	660	1550	- 65	1205	15
5BHP2A	660	880	- 80	1395	15
6DP7	1980	1550	-124	1079	15
7AEP7	660	1375	- 75	949	15
7AGP19	660	3500	-175	1178	15
7AKP25	660	2750	-120	1219	15
7BSP7	310	1650	- 72	1455	15
7YP2	660	1650	- 90	422	15
12AKP7	660	3300	-240	1122	15
12ATP28	1980	2000	- 86	1400	15

Cathode Ray-Magnetic Deflection, Electrostatic and Magnetic Focus

Type No.	Focus Type	If mA Max	Maximum Anode Voltage Eb1 Vdc	Maximum Grid Cutoff Ec1 Vdc	MIL-E-1/ Specification Sheet No.	$F/10^6$ hrs
5AHP7A	Elec	660	1100	-77	972	15
5FP7A	Mag	660	8800	-70	1392	15
5FP14A	Mag	660	8800	-70	1392	15
7ABP7A	Elec	660	1100	-77	866	15
7MP7	Mag	660	8800	-63	67	15
10KP7A	Mag	660	11000	-63	1162	15
10WP7	Elec	660	900	-77	1005	15
12ABP7A	Elec	660	1100	---	1261	15
22CP7A	Mag	660	18000	-77	1072	15
22CP25A	Mag	660	18000	-77	1072	15

Image Converters

Type No.	Eb Vdc Max	ib Adc Max	Ib Adc Max	Altitude ft	MIL-E-1/ Specification Sheet No.	$F/10^6$ hrs
6914	16,000	3.5	0.35	10,000	1049	20
6929	12,000	3.5	0.35	10,000	1583	20

Traveling Wave

Type No.	Frequency Range GHz	Function	Power Output	MIL-E-1/ Specification Sheet No.	$F/10^6$ hrs
8175	2.9 to 3.1	Amplifier	1 kW	1623	30
8362	5.4 to 5.9	Amplifier	50 W	1653	30
8364	5.4 to 5.9	Amplifier	200 mW	1654	30

Planar and Pencil

Type No.	Design	Function	Pp W	Fl MHz	MIL-E-1/ Specification Sheet No.	$F/10^6$ hrs
6299	Planar triode ceramic-metal		2.0	3,000	484	100
7554	Pencil triode ceramic-metal	Class C amplifier	2.5	550	1325	100
6442	Planar triode ceramic-metal	Oscillator or amplifier	8.0	2,500	1055	100
7815	Planar triode ceramic-metal	Anode, grid pulsed oscillator or amplifier	10	3,000	1429	100
7289	Planar triode	CW oscillator	100	2,500	1120	100

Pulse Modulators (gas)

Type No.	epx kV	ib a	Ib Adc	Pb_9 x10^9	MIL-E-1/ Specification Sheet No.	$F/10^6$ hrs
7621	8	90	0.100	2.7	1428	10
7782	12	350	0.2	4.0	1636	10
7665	16	350	0.50	5.0	1485	10
7620	20	500	0.5	10	1612	10
8354	25	1,000	2.2	25	1361	10
7390	33	2,000	4.0	30	1361	10

Vidicons

Type No.	Cutoff Vdc max	Center Resolution (lines) min	MIL-E-1/ Specification Sheet No.	$F/10^6$ hrs
7038	-95	650	1534	20
7263A	-95	650	1294	20
7735A	-95	650	1410	20

Klystrons

Type No.	Center Frequency MHz	Power Output W	Frequency Range MHz	Duty		MIL-E-1/ Spec. Sheet No.	$F/10^6$ hrs
				CW	Pulse		
Amplifiers							
8493	1088	25 K	960 to 1215		X	1112	200
8237	3040	6720	2980 to 3100		X	1589	200
8196	3500	3.5 M	3400 to 3600		X	1520	200
8315	5642	300	5385 to 5900		X	1290	200
8361	5650	3 M	5400 to 5900		X	1228	200
8404	5657	2	5385 to 5930	X		1289	200
Oscillator							
5837	1800	0.05	785 to 2820	X	X	602	30
6BM6A	2175	0.05	550 to 3800	X		746	30
6133	2613	0.095	1500 to 3750	X	X	200	30
2K22	4575	0.100	4240 to 4910	X		1638	30
7471	5650	0.03	5500 to 5800	X		1283	30
VA-220B	7275	1.0	7125 to 7425	X		1631	30
2K48	7500	0.02	4000 to 11000	X		374	30
6390	8882	0.045	6700 to 11065	X	X	840	30
6940	9080	0.02	8500 to 9660	X		1229	30
6781	9275	0.040	8500 to 10000	X		1180	30
7511	9500	0.020	8500 to 10500	X		1119	30
8230	13300	15	13295 to 13305	X		1340	30
8407	13450	0.140	12400 to 14500	X		1571	30
8182	69750	0.015	68750 to 70750	X		1425	30

Power Triodes

Type No.	Function	Pp W	F1 MHz	MIL-E-1/ Specification Sheet No.	$F/10^6$ hrs
8161	C Telegraphy	4,000	110	1619	75

Power Tetrodes

Type No.	Function	Pp W	Fl MHz	MIL-E-1/ Specification Sheet No.	$F/10^6$ hrs
6816	C Telegraphy	115	1,212	1239	100
6884	C Telegraphy	115	1,215	1239	100
7580W	Class AB1	250	30	1385	100
8621	Class AB1	250		1580	100
8245/ 4CX250K	C Pulsed	250	1,500	1506	100
8167	Class AB1	300	500	1313	100
8321	Class AB1	350		1634	100
8322	Class AB1	350		1634	100
8651 4CX300Y	C Telegraphy	400	110	1541	100
6283	C Telegraphy	480	900	1314	100
8500	C Telegraphy	480	900	1314	100
7650	Linear RF Power Amplifier	600	1,215	1552	100
7651	Pulsed RF Amplifier	600	1,215	1553	100
8168/ 4CX1000A	Class AB1 or AB	1,000	110	1569	100
8660 4CX1500B	Class B or AB	1,500	30	1648	100
8170W	C Telegraphy	5,000	100	1427	100
6952	Anode Pulsed Amplifier; Class B	8,000	550	1106	100
6166A/ 7007	C Telegraphy	12,000	220	1543	100
2041	Screen and Grid Pulsed Amplifier; Class B	20,000	575	1383	100

Graphic Indicators

Type No.	Ionization Voltage Vdc	Cathode Current (Individual) mA	Character Display	MIL-E-1/ Specification Sheet No.	$F/10^6$ hrs
6844A	170	4.0	Numeral	1266	15
7009	170	2.0	Numeral	1500	15
7977	170	2.0	Numeral	1497	15
8421	170	3.5	Numeral	1454	15
8422	170	3.5	Numeral	1519	15
8423	170	4.5	Numeral	1518	15

Receiving Triodes

Type No.	Ef V Max	If mA Max	Mu Max	1b mAdc Max	MIL-E-1/ Specification Sheet No.	$F/10^6$ hrs
6C4WA	6.9	160	18.5	14.5	857	5
12AT7WC	13.9	158	70.0	14.0	1097	5
5670W	6.9	370	44.0	10.5	5	5
5703WB	6.9	210	28.5	11.5	1070	5
5718	6.6	160	31.0	11.0	172	5
5719	6.6	160	80.0	0.9	173	5
5744WB	6.9	210	80.0	5.2	1073	5
5751	13.8	190	85.0	1.8	10	5
5814A	13.8	190	18.5	14.5	12	5
6012W	6.6	320	40.0	8.5	188	5
6111WA	6.6	320	23.0	11.0	1270	5
6112	6.6	320	80.0	1.10	190	5
6533WA	6.9	210	60.0	1.25	1104	5
7077	6.6	258	115.0	8.8	1203	5
7586	6.9	145	42.0	12.5	1397	5
8085	6.9	145	100.0	12.0	1491	5
8532W	6.3	425	65.0	18.0	1527	5

Receiving Tetrodes and Pentodes

Type No.	Cutoff	Ef V Max	If Amps Max	Ib mAdc Max	MIL-E-1/ Specification Sheet No.	$F/10^6$ hrs
6A110WA	Sharp	6.9	0.480	12.5	1130	5
6AU6WC	Sharp	6.9	0.325	13.5	952	5
5054W	Sharp	6.9	0.190	11.0	4	5
5702WB	Sharp	6.9	0.210	9.5	1069	5
5749W	Remote	6.9	0.325	13.5	8	5
5840W	Sharp	6.6	0.160	9.5	1656	5
5894	-----	13.8	2.0	2 x 110	152	5
5899	Semi-Remote	6.6	0.160	9.2	97	5
7587	Sharp	6.9	0.160	11.8	1434	5

Receiving Mixers and Converters

Type No.	Ef V Max	If mA Max	Ib mAdc Max	MIL-E-1/ Specification Sheet No.	$F/10^6$ hrs
5636	6.6	160	6.9	168	10
5725W	6.9	190	9.0	6	10
5750	6.9	325	3.5	9	10
5784WB	6.9	210	7.1	1096	10

Receiving Power Output Triodes

Type No.	Ef V Max	If mA Max	Mu Max	Ib mAdc Max	MIL-E-1/ Specification Sheet No.	$F/10^6$ hrs
5687WB	13.2	470	21.0	45	779	5
6080WC	6.6	2650	2.5	150	1655	5

Receiving Power Output Pentodes

Type No.	Amplifier Description	Ef V Max	If mA Max	Ib mAdc Max	MIL-E-1/ Specification Sheet No.	$F/10^6$ hrs
6AN5WA	Video	6.9	480	43	839	5
6L6WGB	Beam Power	6.9	960	80	197	5
5639	Video RF	6.6	480	28	159	5
5686	Beam Power	6.9	380	44	171	5
5902	Beam Power	6.6	480	37	175	5
6005W	Beam Power	6.9	480	57	13	5
6094	Beam Power	6.6	640	57	821	5
6146W	Beam Power	10%	1325	140	1502	5
6384	Beam Power	6.9	1260	88	1022	5