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RELIABILITY DERATING PROCEDURES

Martin Marietta Aerospace

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The objectives of this study were the establishment of derating parameters and levels for electronic parts, development of thermal models, creation of temperature verification methods, and the development of the framework leading to the creation of a military standard for derating of parts. The results of the study revealed that derating data on complex devices are difficult to obtain so an alternate approach was used involving failure rate data from MIL-HDBK-217 and specific failure mode information. Thermal models, both internal and nodal, were developed for six package types and temperature test results for one of these types were compared to the theoretical value. The comparison was extremely favorable.

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FOREWORD

This final study contract technical report was prepared by Martin Marietta Orlando Aerospace as a part of the engineering services to the Rome Air Development Center (RADC), Griffiss AFB, New York, under contract F30602-83-C-0006, CDRL A003. The RADC technical monitor for this program is Mr. Bruce Dudley.

CONTENTS

ILLUSTRATIONS

ILLUSTRATIONS

ILLUSTRATIONS

TABLES

TABLES

1.0 EXECUTIVE SUMMARY

The objective of the Reliability Derating Procedures program was to develop the framework leading to the creation of a military standard for the derating of electronic and electromechanical devices for Air Force application. Primary areas of investigation were: 1) relationship of case temperatures to junction temperatures, 2) methods of verifying that derating has been accomplished, 3) relationship of reliability to cost, 4) derating standards for complex devices, 5) creation and verification of thermal models, and 6) temperature derating verification techniques through data collection and testing.

The specific devices identified for investigation under this program were hybrids, complex integrated circuits, memory devices, microwave devices, and surface acoustic wave (SAW) devices. The overall approach divided the program into five specific tasks: 1) a literature search and survey data, 2) parts derating standards and application guidelines, 3) case temperature derating and measurement, 4) reliability versus cost, and 5) development of a military standard framework.

The literature search and survey data task, while being highly successful in obtaining industry response, did not produce a meaningful quantity of data. Task 1 results did highlight industry's need and desire for consistent and standard guidance for new or advanced technology derating and junction temperatures.

The parts derating standards and application guidelines task was planned to use survey guidance from task 1. As task 1 progressed, it was evident that an alternative approach was needed, due to the lack of firm data. The approach established was to investigate MIL-HDBK-217D data and algorithms to determine what factors might be considered for derating, task 2.

Each MIL-HDBK-217D factor, such as environment, package size, complexity, temperature, voltage, etc., was investigated in detail to determine its impact on the subject device. The output of the investigation resulted in specific derating criteria for each of the devices. The derating criteria specified the parameters to be derated and the amount of derating in relation to the three-level derating philosophy. The balance of the task was identification and guidance in relation to the failure modes and mechanisms. The approach for this later portion was to first identify the failure mode origins, then group the modes, and finally to identify the point of elimination or control of specific failure modes.

The case temperature derating and measurement task 3 was to develop and verify models for junction temperature derating to case temperature derating. This task was also to provide a cost-effective technique for actual measurement of selected integrated circuit and semiconductor case temperatures related to the junction temperatures. The task was accomplished with the creation of two specific types of models. The first model was an internal one predominately used for new devices to approximate the thermal impedance from the chip junction to the case bottom (θjc). The second model was an external one for specific package types (axial studs, ceramic chip carriers, cerdip, flatpack, hybrid, and side-brazed). Each of the

specific package types identified a temperature measurement point on the specific package. In conjunction with curves derived from model runs, the actual junction temperature of the chip were estimated. Two of the six package models have been verified for accuracy, through actual test measurement data (with side-brazed and ceramic chip carriers). These models were determined to be within 4 degrees centigrade (°C) of the measured value.

Each package model required measurement of the board temperature and junction temperature in order to determine the temperature value at the specified device measurement point. Two additional variables, ambient air and radiation sink temperatures, were considered by providing tolerance bands on each curve. The final portion of the task identified measurement equipment available, with it's respective advantages, disadvantages, and accuracies to determine which characteristics could be used to make the temperature measurements in a system. It needs to be highlighted, to prevent misapplication of the models, that the external models presented are not universally applicable to all package sizes, mountings, chip sizes, etc.

The reliability versus cost task (4) addressed the components which drive the cost of reliability. The primary drivers addressed are the contract requirements, funding level, temperature requirements, quality level, and device cost.

The final task (5) was to develop a military standard framework which would be used for the creation of the standard for the derating of electronics and electromechanical devices for Air Force application.

2.0 DEVICE DERATING GUIDELINES

2.1 Derating Definitions

2.1.1 Derating Levels

The range of derating is generally defined as a point between the minimum derating point and the point of over-derating. The optimum derating, therefore, should occur at or below the point of stress (i.e., voltage, temperature) where a rapid increase in failure rate occurs for a small increase in stress. Three derating levels are selected on the basis of the criticality of the application.

Derating Level I (Maximum Derating)

This level pertains to equipment failure that would substantially jeopardize the life of personnel, or seriously jeopardize the operational mission. Repairs are considered unfeasible or economically unjustified at this level.

Level I derating is also considered to be those stress levels below which further reliability derating gain is negligible, or where further derating will create difficult design problems. This derating is intended for the most critical applications, or where the associated design difficulty can be justified by the reliability requirement.

Derating Level II

This derating level refers to failure that would degrade the operational mission or would result in unjustifiable repair costs. Level II derating is considered to be still in the range where reliability gains are rapid as stress is decreased. However, achieving designs with these reductions in allowed stress is significantly more difficult than at Level III.

Derating Level III

This derating level pertains to equipment that is considered less critical than Level I or II equipment. Level III failure does not jeopardize the operational mission, or can be quickly and economically repaired.

Level III derating is also that stress level reduction which creates minor design difficulties, while generating the largest environmental reliability gain. This gain is realized because the effect of stress increases dramatically as the absolute maximum rating is approached.

2.1.2 Part Quality Levels

Derating cannot be used to compensate for using parts of a lower quality than necessary to meet usage reliability requirements. The quality level of a part has a direct effect on the predicted failure rate.

Electrical testing of all parts in a lot is not guaranteed for commercial or JAN level military parts. For high reliability applications, only fully tested and screened parts (including burn-in) should be used, in addition to applying the appropriate derating levels. Section 6.0, Table 39, shows the part quality levels and the screening requirements as specified in MIL-HDBK-217D.

2.1.3 Environments

Equipment environments are commonly associated with derating criticality levels. The various operational environments, as defined in MIL-HDBK-217D, can be assigned to these levels, as shown below.

Environment	Level
Ground	III
Flight	II
Space	I

These environmental conditions are broad categories to give some guidance in selecting the proper part derating requirements. In the ground environment, equipment required to be mobile or mission critical in most cases should be rated in accordance with level II. Flight or airborne equipment that may be crew-hazardous should be derated to level I.

The equipment environments versus derating levels in the table are guidelines only; operational environment, program goals, operational objectives, and life cycle cost may modify or dictate the derating level selection.

2.2 Hybrid Devices

Hybrid devices are composed of elements such as integrated circuits, transistors, capacitors, and/or resistor chips mounted on a common substrate. This technology combines elements into a high density package to decrease volume and sometimes power. The hybrid may use thick film or thin films as interconnections and resistive elements. The primary failure modes are failures of active components, integrated circuits or transistor chips, and interconnection faults.

Application

In hybrids, a deviation from the nominal supply voltage will shift internal bias points. This deviation, coupled with thermal effects, can result in the device performing erratically. Some hybrid circuits are also susceptible to electrostatic discharge. Since hybrids are affected by these parameters, design precautions to control supply voltage and electrostatic discharge handling precautions, such as grounding, should be taken. However, the primary driver for derating is the junction temperature.

Derating

These derating criteria for hybrids are summarized in Table 1. Individual elements or devices contained in the hybrid package should be derated individually, in accordance with the guidelines of AFSC Pamphlet 800-27.

TABLE 1. DERATING FOR HYBRID DEVICES

	Level I	Level II	Level III
Maximum Junction Temperature (°C)	85	100	110
Thick Film Power Density	<50 watts/in^2	<50 watts/in^2	<50 watts/in^2
Thin Film Power Density	<40 watts/in^2	<40 watts/in^2	<40 watts/in^2

Note: For every degree C above 100°C case temperature, derate the power density 1 watt per square inch below the values shown.

2.3 Complex Integrated Circuits

The complex integrated circuits defined for derating guidelines include four specific groups: 1) large-scale integration (LSI) and custom LSI, 2) very high speed integrated circuits (VHSIC), 3) very large scale integrated circuits (VLSI), and 4) microprocessors.

Among the different technologies used for fabricating the complex arrays are: 1) bipolar, 2) p-channel metal oxide semiconductor (MOS), and 3) complementary metal oxide semiconductor (CMOS). The bipolar and p-channel MOS techniques require load resistors and by the nature of their design have higher static power dissipation than CMOS. The CMOS technology uses both p- and n-type transistors in series. The signal that turns the n-type transistor on, turns the p-type transistor off, and vice versa. There is never a path to ground for the current, except through an external load. This lack of a path results in a saving of operation power, and in turn reduces overall device temperature. Howeve , as CMOS is operated at higher frequencies, power dissipation increases significantly resulting in the same effect as p-channel and bipolar.

Application

MOS/CMOS devices tend to be highly sensitive to damage due to electrostatic discharge. This discharge is due to excessive noise on signal lines. The performance of bipolar devices is affected by supply voltage deviations from the specified nominal, due to shifting bias points when coupled with thermal effects. Increased bipolar action in CMOS devices in particular can lead to latch-up. Design precautions need to be taken to ensure maximum operability of these complex devices by minimizing or eliminating noise on signal lines and control of supply voltage deviations.

Derating

These derating criteria for complex integrated circuits, LSI, VHSIC, VLSI, and microprocessors, are summarized in Table 2.

TABLE 2. DERATING CRITERIA FOR COMPLEX INTEGRATED CIRCUITS (LSI, VHSIC, LSI, MICROPROCESSORS)

	Level I	Level II	Level III
Maximum Junction Temperature (°C)	85	100	125
Supply Voltage (of Rated Value)	0.75*	0.80	0.85
Output Current (of Rated Value)	0.70	0.75	0.80
Fan Out (Digital) (of Maximum Specified)			
Bipolar	0.70	0.75	0.80
MOS	0.80	0.80	0.90
Operating Frequency (Digital) (of Maximum Specified)			
Bipolar	0.75	0.80	0.90
MOS	0.80	0.80	0.80

*Note: Designing below 75 percent of the supply voltage may run the device below the recommended operating voltage.

2.4 Memory Devices

The memory devices defined for derating guidelines include three specific technologies. They are 1) bipolar, 2) MOS, and 3) bubble. In the bipolar and MOS technology, the memory group can be broken up into random access memories (RAM) and read only memories (ROM).

The RAMs, in turn, can be categorized as static and dynamic. These two RAMs differ in how they store data. Static RAMs are easier to use, while dynamic RAMs are cheaper and use less power. However, dynamic RAMs must be refreshed and recycled.

Although the bubble device and material technology is significantly different from silicon devices, this technology is also based on a batch manufacturing process. As a device, bubble memory is very well suited to serial data storage. It is slower than silicon devices, but it is non-volatile, and will allow data to be stored and retrieved efficiently. Bubble memories are light, compact, and low-power devices.

Application

The performance of MOS devices is a function of the operating voltages, and their ability to handle high operating voltage decreases very rapidly with reduced device sizes. Bipolar memory circuits do not suffer from this limitation. However, they are restricted, based on current drain and power dissipation limits. Bubble memory operation is dependent upon the ability of the external support microelectronic devices to function properly within their specified limits. Design precautions should be taken to ensure that the proper tolerances are set for the particular device application in accordance with the device specifications.

Derating

These derating criteria for memory devices (RAM and ROM) are specified in Table 3. Table 4 represents the derating criteria selected for bubble memories. Bubble memory derating will also involve the use of the guidelines specified within for the individual microelectronic devices. These devices make up the external support required for bubble memory operation.

TABLE 3. DERATING CRITERIA FOR MEMORY DEVICES (RAM AND ROM)

	Level I	Level II	Level III
Maximum Junction Temperature (°C)	85	100	125
Supply Voltage (of Rated Value)	0.75	0.80	0.85
Output Current (of Rated Value)	0.70	0.75	0.80

TABLE 4. DERATING CRITERIA FOR MEMORY DEVICES (BUBBLES)

	Level I	Level II	Level III
Maximum Ambient Operating Temperature (°C)	85	85	85

2.5 Microwave Devices

The microwave devices addressed in this section are 1) GaAs FET, 2) detectors and mixers, 3) varactor diodes, 4) step recovery diodes, 5) PIN diodes, 6) tunnel diodes, 7) IMPATT diodes, 8) Gunn diodes, and 9) transistors.

The microwave devices are categorized, based on the amount of electrical stress characteristic to a normal operating environment. There are low and high electrical stressed devices, which are separated into four groups for derating purposes. These groups are:

High electrical stressed devices:

Group I - GaAs FET
Group II - Transistors/IMPATT/Gunn Diodes

Low electrical stressed devices:

Group III - Varactor/Step Recovery/PIN/Tunnel
Group IV - Detectors/Mixers

- Silicon
- Germanium

The derating parameters selected for these devices are junction temperature, voltage, and power. The selection was based on the predominant failure modes occurring in application. These modes are metal migration caused by voltage and power stresses, junction shorts, and hermeticity problems, all of which are predominately temperature-related failures.

2.5.1 GaAs FET Devices

Application

The field-effect transistor is a voltage-controlled device which has a high input impedance and can perform the switching or amplification function. GaAs FETs are often used in amplifiers, but are also used in microwave oscillators and mixers. GaAs FETs are subject to damage caused by switching transients and static discharge.

Derating

These derating criteria for GaAs FETs are listed in Table 5.

TABLE 5. GaAs FET DEVICE DERATING

	Level I	Level II	Level III
Junction Temperature (°C)	95	105	125
Power Dissipation (percent)	50	60	70
Breakdown voltage (percent)	60	70	70

2.5.2 Transistors/IMPATT and Gunn Diodes

Application

Microwave transistors, IMPATT Diodes, and Gunn diodes are all classified as high electrically stressed devices. In fact, IMPATT diodes are characterized by their ability to dissipate maximum power per unit volume, while Gunn diodes and microwave transistors operate most efficiently at power levels just below the maximum specified. The voltage applied to these devices is a major concern for correct operation. Design precautions need to be exercised to ensure that recommended specificaiton voltage levels are not surpassed.

Derating

These derating criteria for microwave transistors, IMPATT diodes, and Gunn diodes are in Table 6.

TABLE 6. TRANSISTOR/IMPATT/GUNN DERATING

	Level I	Level II	Level III
Junction Temperature (°C)	95	105	125
Power Dissipated (percent)	50	60	70
Breakdown voltage (percent)	60	70	70

2.5.3 Varactor/Step Recovery/PIN/Tunnel Diodes

Application

Varactor, step recovery, PIN, and tunnel diodes are described as being low electrically stressed devices. They are low power handling devices and should not be subjected to unusually large power stresses. High junction temperature is a very destructive stress which should be limited.

Derating

These derating criteria for varactor, step recover, PIN, and tunnel diodes are summarized in Table 7.

2.5.4 Silicon and Germanium Detectors and Mixers (Schottky)

Application

These minimally stressed devices typically operate at low power levels and low noise figures. They are particularly sensitive to circuit transients and electrostatic discharges, which result in diode burnout. Precautions should be taken to safeguard against this.

TABLE 7. VARACTOR/ STEP RECOVERY/PIN/ TUNNEL DERATING

	Level I	Level II	Level III
Junction Temperature (°C)	95	105	125
Power Dissipation (percent)	50	60	70
Breakdown voltage (percent)	70	70	70

Silicon detectors and mixers are widely used and are highly accepted. However, germanium devices are not recommended for use.

Derating

These derating criteria for silicon detectors and mixers (Schottky) are summarized in Table 8. Derating for germanium detectors and mixers has been developed in spite of the negative recommendation. This group's derating appears in Table 9.

TABLE 8. SILICON DETECTORS/MIXERS (SCHOTTKY) DERATING

	Level I	Level II	Level III
Junction Temperature (°C)	95	105	125
Power Dissipated (percent)	50	60	70
Breakdown voltage (percent)	70	70	70

TABLE 9. GERMANIUM DETECTORS/MIXERS DERATING

	Level I	Level II	Level III
Junction Temperature (°C)	75	90	105
Power Dissipated (percent)	50	60	70
Breakdown voltage (percent)	70	70	70

2.6 Surface Acoustic Wave (SAW) Devices

Surface acoustic wave (SAW) devices are currently being used as delay lines, oscillators, resonators, and filters. They are tailored to the particular frequency and response desired for each application, with a frequency range from 50 megahertz to about 2 gigahertz. Interest in SAW devices has evolved primarily because of two characteristics inherent to the waves themselves. The first characteristic is the short wavelength and related slow propagation velocity of the acoustic wave, as compared to the electromagnetic wave. This characteristic allows signal delay and filtering.

The second characteristic is the propagation of the acoustic waves along the surface of the solid. This characteristic enables the energy at a depth of one wavelength or less to be sensed and manipulated by the SAW elements. A SAW device usually consists of the SAW element on its piezoelectric substrate plus any auxiliary elements, such as an amplifier or matching elements, and the packaging of the complete device. The most commonly used substrate material is quartz due to its demonstrated temperature stability over a wide range. The input and output electronic interface is achieved through interdigital transducers. Those transducers create a strain on the substrate surface, with applied voltage causing the generation of a physical wave.

Application

SAW devices are passive. They operate at a low power level and are low heat generators. Since heat generation is minimal, the environment determines the SAW operating temperature. The devices surrounding the SAW device become a major concern when environmental temperatures rise. Precautions should be taken to ensure that the surrounding devices do not create an unstable operating environment. The frequency stability demonstrated by the SAW device is a design requirement which can cause part degradation if it is not controlled. These devices have also exhibited sensitivity to electrostatic discharge. Design attention is required to minimize this stress.

Derating

The derating level breakdown (I, II, and III) will not be applicable to SAW devices, due to their passive operative nature. In most cases, derating is inappropriate for SAW devices. However, input power and operating temperature are two parameters that require limiting. These derating criteria for SAW devices are summarized in Table 10.

TABLE 10. SAW DEVICE DERATING

	Center Frequency (MHz)	
	$\geq$ 500	< 500
Input Power (dB)	13	18
Temperature (°C) (Operating Maximum)	125	125

3.0 BASIS FOR DEVICE DERATING

3.1 Rationale of Device Derating

This section provides support and rationale for the derating criteria specified for the particular device types under investigation. A literature search, along with a survey of the industry via letters and telephone contacts (see Appendix 3), was implemented as a means of obtaining derating criteria for the specified devices.

The derating information received did not address the more complex device types. Therefore, MIL-HDBK-217D was used as the primary basis for derating for the hybrid devices, complex integrated circuits, memory devices, and the microwave devices. A survey was conducted within Martin Marietta to supplement the MIL-HDBK-217D approach. The information received tended to support the guidelines established using MIL-HDBK-217D. Due to the lack of information published on SAW devices, the derating criteria was based on discussions held with those device manufacturers knowledgeable with the basic device design and applications. Each of these device types will be discussed in their respective sections, with derating rationale and supporting charts provided.

Using MIL-HDBK-217D, there are many factors which have to be considered due to their impact on the failure rate of each device type. The failure rate drivers and factors investigated were quality level, environment, failure rate, interconnections, package size, density, complexity, temperature, voltage, frequency, power, and application.

The failure rate of each device involves the combination of different factors. The effect of the factors that are common to all the devices will be discussed in this section, while the remaining factors will be discussed as they apply.

The quality factor used in the computation of the failure rate is the same for all the microelectronic and microwave devices. The exception is SAW devices, since they are not discussed in MIL-HDBK-217D.

Figure 1 shows a plot of the component quality level impact on failure rate. The plot shows that the quality level impact increases significantly at the levels going from B-2 to B-1 (vendor equivalent to 883 Class B). The quality level is a direct multiplier in the failure rate calculation, but is solely dependent on testing and inspection criteria.

The component environmental application factors of MIL-HDBK-217D have a direct bearing on the individual failure rates. The following discussion will assess the impact of the environment as related to the component level failure rate. Figure 2 shows a plot of all the application environmental factors for microelectronic devices as presented in MIL-HDBK-217D, Table 5.1.2.5-3. This table shows that the Cannon Launch (CL) environment overshadows all the other environmental factors. For that reason, the CL environment was removed and the plot was regenerated in Figure 3. This figure shows that the level III ground environments are all in the lower third of the curve.

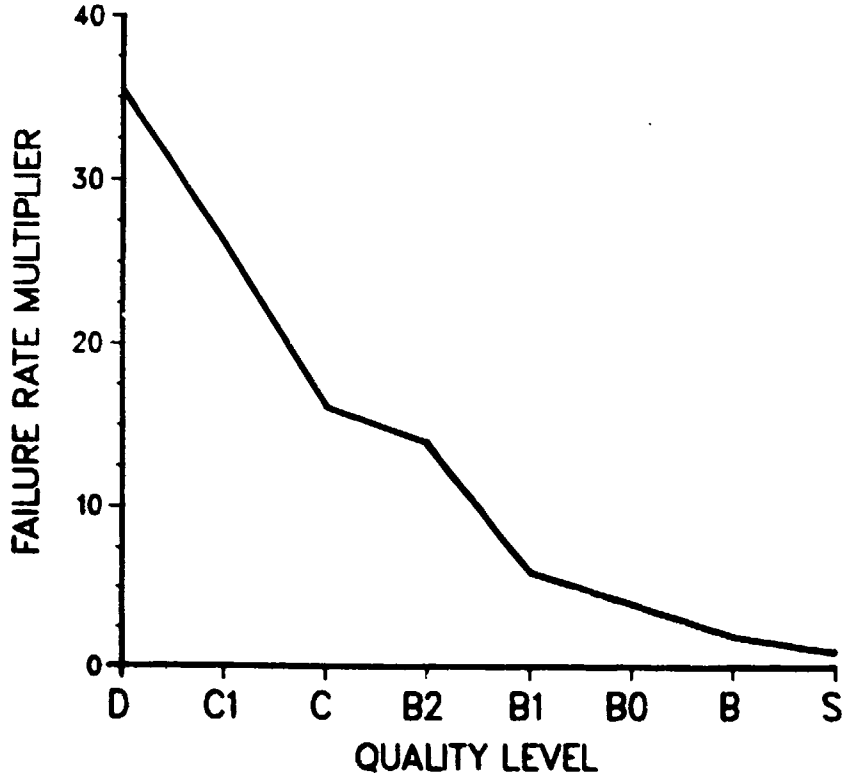


Figure 1. Quality Level Impact on Failure Rate

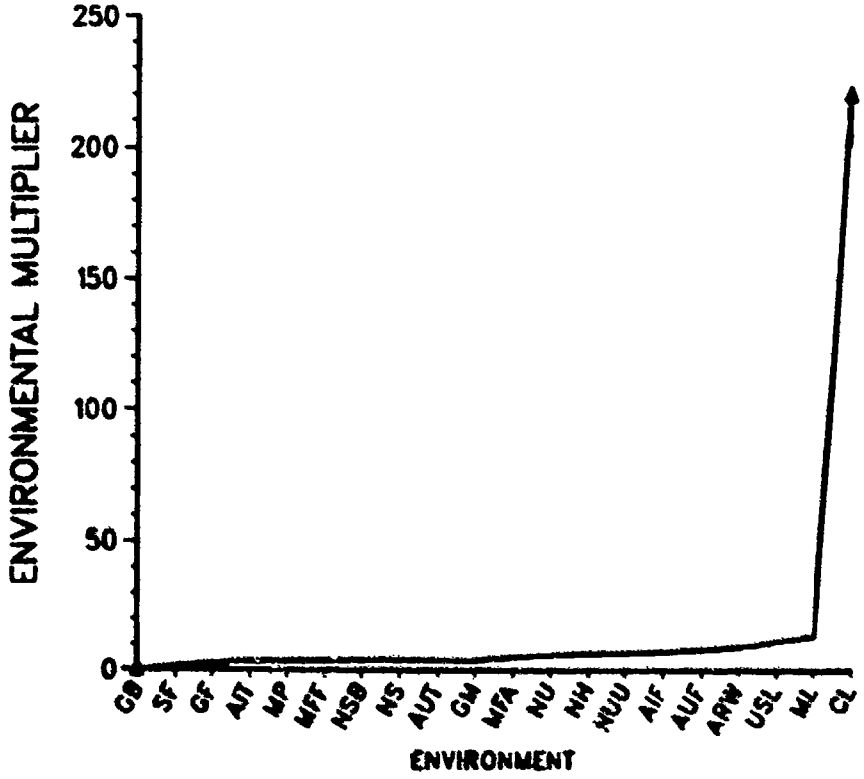


Figure 2. Environmental Impact on Failure Rate

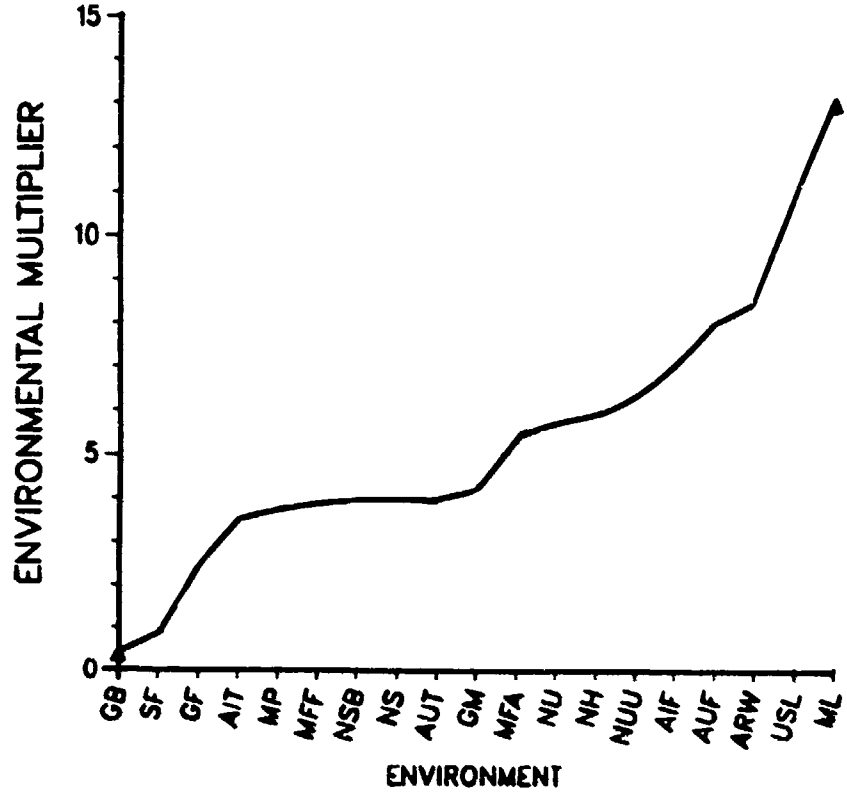


Figure 3. Environmental Impact on Failure Rate

The next step was to select a typical LSI integrated circuit and perform a MIL-HDBK-217D prediction on the typical integrated circuit across the temperature range of 0 to 200°C for each environmental application factor. The circuit selected was a MIL-M-38510 quality level B component, part number M38510/47001 (Generic 1802). The results of the iterative prediction were plotted in two ways. The first was to establish a failure rate factor (multiplier) based on the particular environment using 0°C as its base, and the second was to plot the actual failure rates predicted. The two sets of curves are shown in Figures 4 and 5, respectively. The factor plot (Figure 4) shows the driver of failure rate to be the temperature. For all the environments, the failure rate begins to show significant increase as the component temperatures increase above 100°C. The largest failure rate multiplying factor across the temperature range was found to be in the ground benign environment. This factor is calculated to be 30891. In order to investigate and highlight the slopes of the lines, the temperature range was reduced to 25 to 175°C. The regenerated plot is shown in Figure 6. The reduced temperature range did not reveal any additional information.

The failure rate plot in Figure 5 confirmed that the ambient temperature is the controlling factor for failure rate. All the environments except for the CL override one another. The CL environment appears to approach the rest of the environments at approximately 200°C. The temperature range was again reduced and the curves regenerated (Figure 7). The expanded curves do not add any additional information.

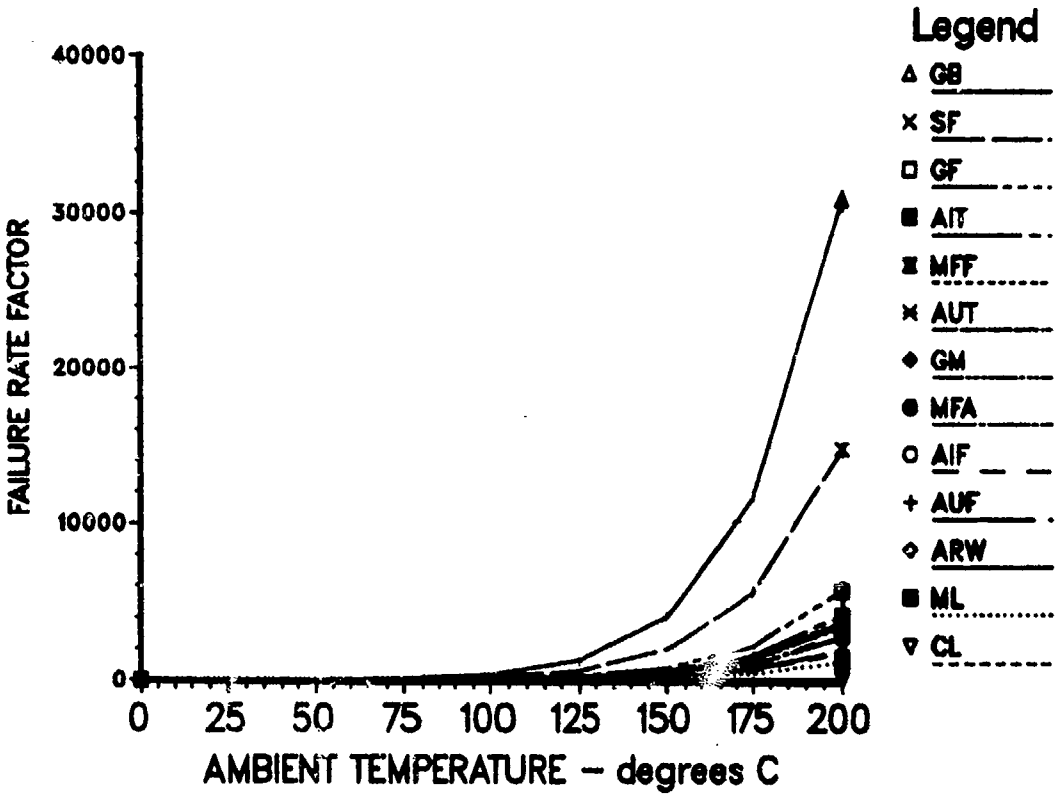


Figure 4. Environmental Impact on Failure Rate

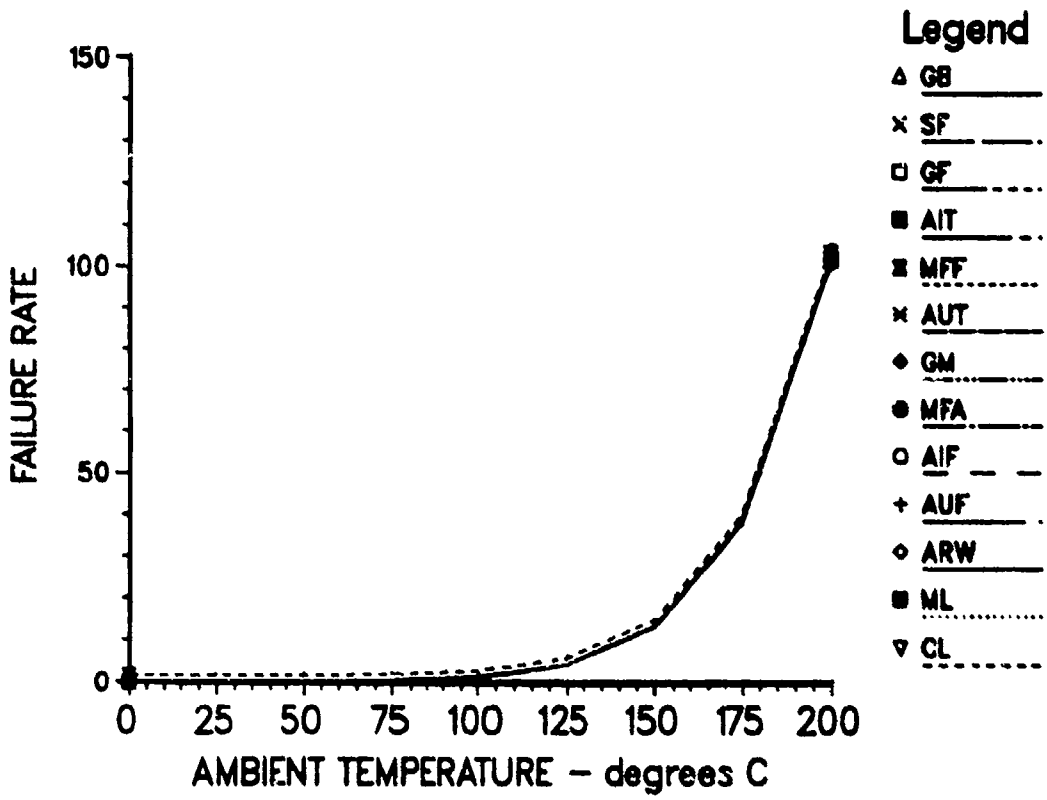


Figure 5. Environmental Impact on Failure Rate

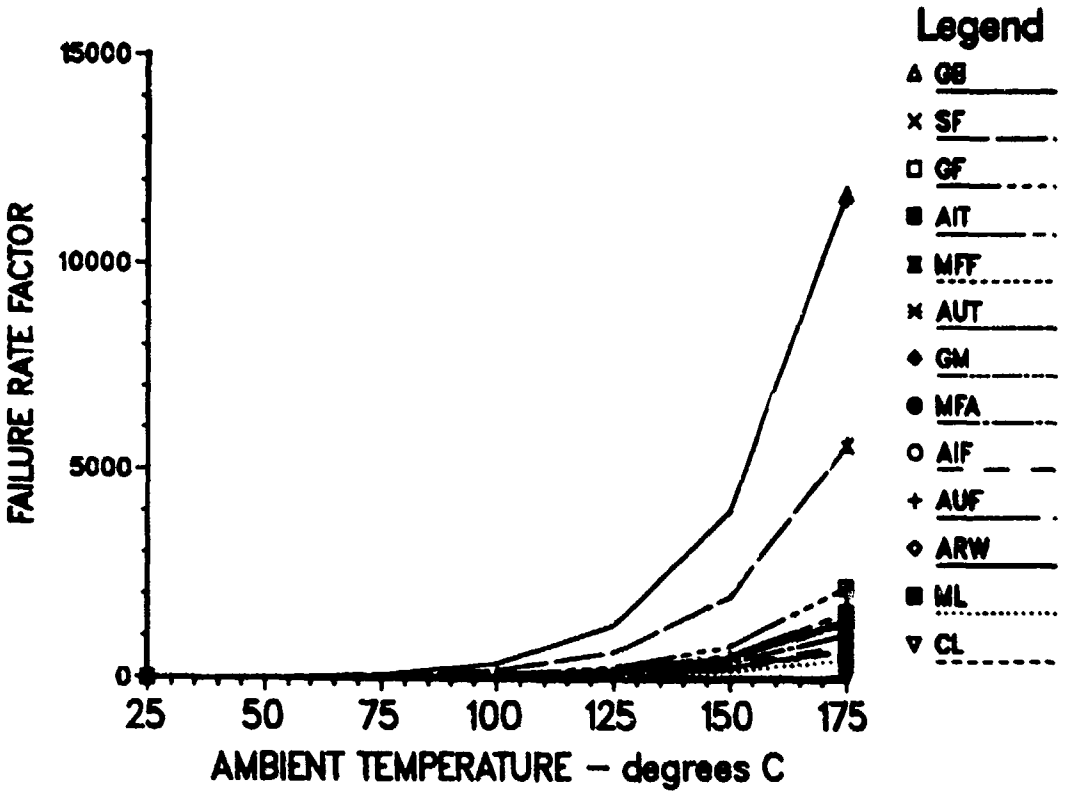


Figure 6. Environmental Impact on Failure Rate

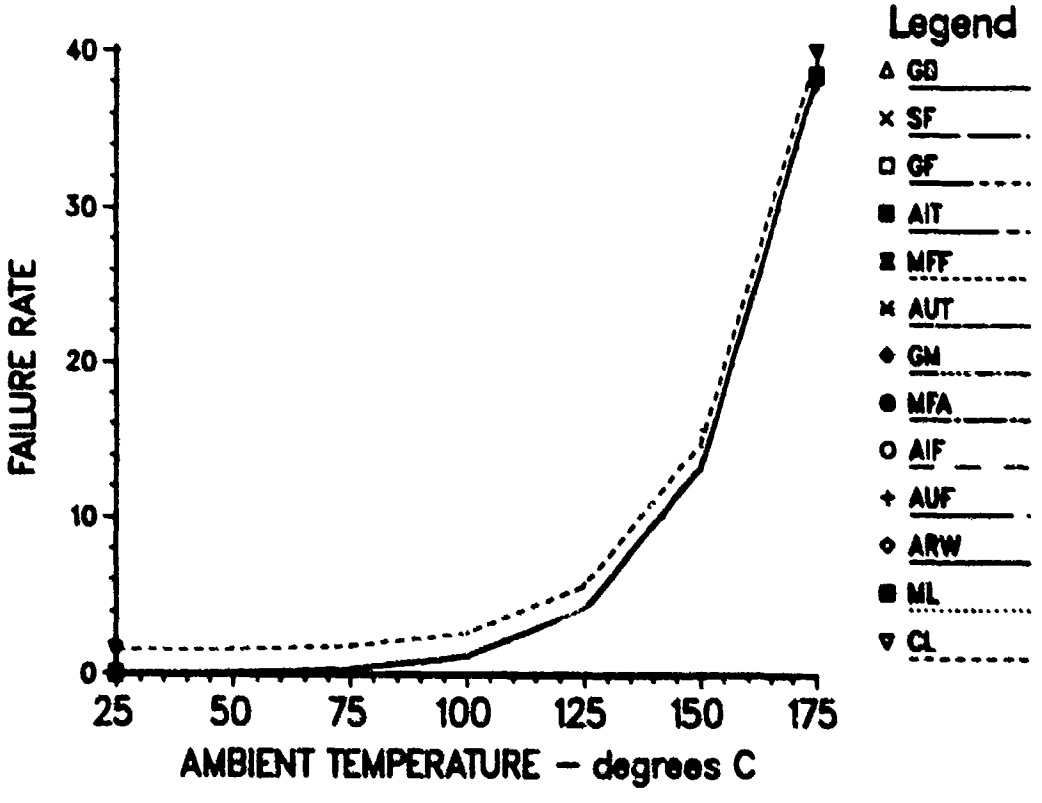


Figure 7. Environmental Impact on Failure Rate

The result of the investigation of the environmental factors specified in MIL-HDBK-217D indicates that they do not change the slope of the failure rate and are not failure rate drivers. The environmental factors are only multipliers to adjust the magnitude of the failure rate and should not be the primary drivers for derating. This rationale can be applied to the environmental factors for the microwave devices. If the curves were replotted for the microwave devices, the new curves would look identical, with the exception of an upward shift due to factor variations.

3.2 Basis for Hybrid Derating

Establishment of hybrid device derating criteria is not a commonly addressed area. This is pointed out in the survey derating summary in appendix 3. Only 4 responses out of 32 addressed hybrids for derating. Those 4 responses were concerned with junction temperature. The junction temperature deratings specifically mentioned were 110°C and 105°C. Another approach reported was to use 75 percent of the specified temperature rating. The lack of response from the survey led to the derivation of derating based on the data of MIL-HDBK-217D and knowledge of failure rate drivers from Task 3 (Section 4) thermal models.

In order to arrive at a reasonable derating criteria, each major driver in the hybrid failure rate must be investigated. The junction temperature of the integrated circuit elements can be investigated through the use of the failure rate temperature acceleration factors for monolithic microelectronics. Figure 8 shows the junction temperature impact on the temperature acceleration factor for each technology addressed in MIL-HDBK217D. The figure shows that there is no significant acceleration factor where junction temperature is limited between 80°C to 90°C (less than 10) for all technologies. When the junction temperature rises to approximately 100°C, the factor for CMOS and linear acceleration rises to approximately 16. At a junction temperature of approximately 110°C for CMOS and linear acceleration, the temperature acceleration factor begins to increase rapidly to approximately a value of 27. This analysis would tend to indicate significant breakpoints for hybrid derating criteria.

A second driver to hybrid device failure rate is the quantity and type of interconnections. Figure 9 shows bimetal and single metal bond interconnections. The figure shows the factor based on a single interconnect. When the prediction is accomplished in accordance with MIL-HDBK-217D, the interconnection failure rate contribution factor (λ_1) is multiplied by the total number of interconnections. Applying the junction temperatures in Figure 8 to the package temperature of Figure 9 minimizes the impact of interconnections. Based on the most severe curve in Figure 9, bimetal bonds, the 85°C temperature factor is approximately 14. The factor at 100°C is approximately 30 and at 110°C the factor rises rapidly to approximately 44. The curves of Figure 9 tend to support the breakpoints selected from the previous curves in Figure 8. (Figure 10 intentionally deleted).

The third driver peculiar to hybrids is the package size impact on temperature. Figure 11 shows the impact of the seal perimeter (directly related to package size) on failure rate as the package temperature increases. An analysis showed that an increase in seal perimeter does not change the shape of the curve, that is, the package failure rate factor is

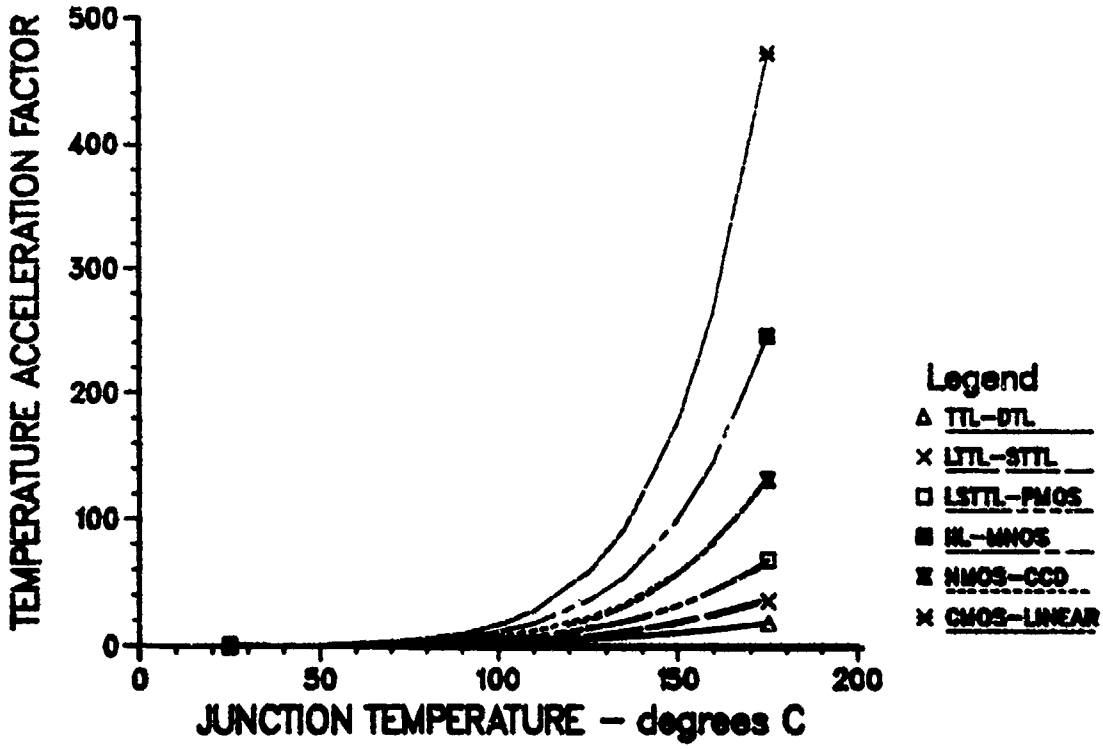


Figure 8. Microelectronics: Junction Temperature versus Failure Rate

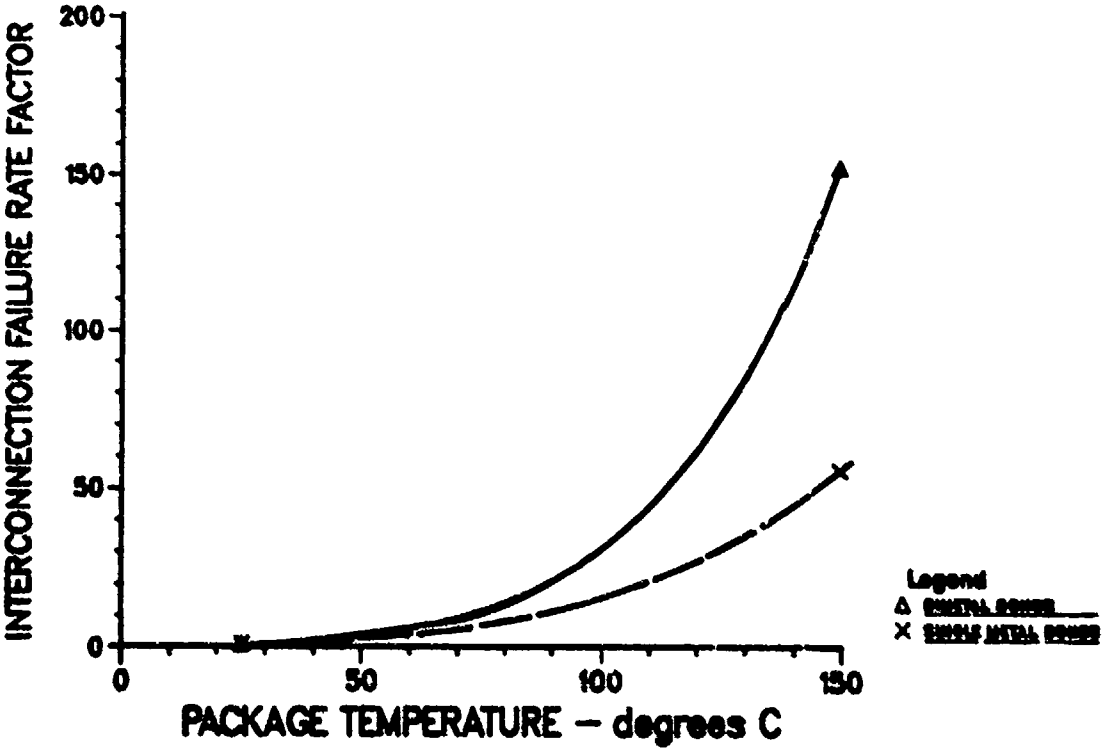


Figure 9. Hybrid: Package Temperature versus Interconnections

the same at a specific temperature regardless of the perimeter value. Therefore, the figure is calculated on a seal perimeter of two inches. As with the previous figure, the base temperature of 25°C is used and again the factors (multipliers) are compared to the same breakpoints of 85, 100, and 110°C. The factors associated with the three breakpoints are approximately 15, 33, and 48 respectively. This analysis (figure) again supports the derating breakpoints established from the junction temperature and interconnect analysis.

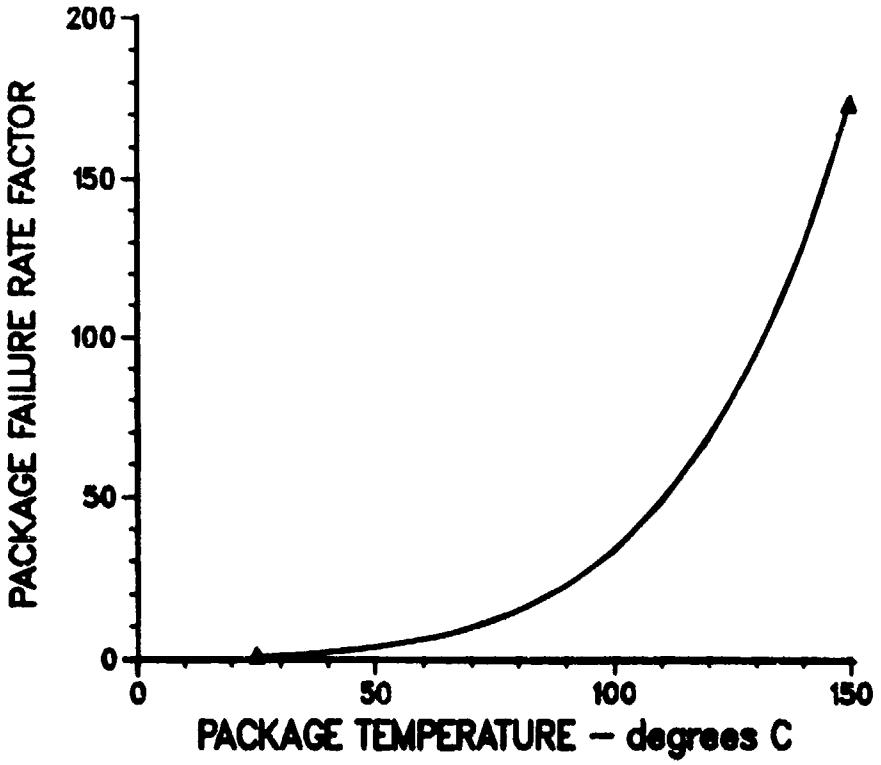


Figure 11. Hybrid: Package Temperature versus Package Size (2-inch Perimeter Seal)

The final factor investigated for impact on the hybrid was the density factor as defined in MIL-HDBK-217D. MIL-HDBK-217D defines density as a measure of the mechanical complexity as a whole. The density formula is: $\text{Density} = \frac{\text{number of interconnections}}{(\text{As} + 1.0)}$ where As = area of the substrate in square inches.

This factor is based solely on mechanical complexity and is not related directly to the common derating of power density. Figure 12 shows the density impact on the hybrid failure rate. Inspection of the curve shows no obvious breakpoints to drive the derating criteria. A relationship does exist however, with earlier figures (8 and 9). Both figures are based on interconnections and in turn can be related to temperature. As the density and temperature increase, the factor or multiplier will increase dramatically.

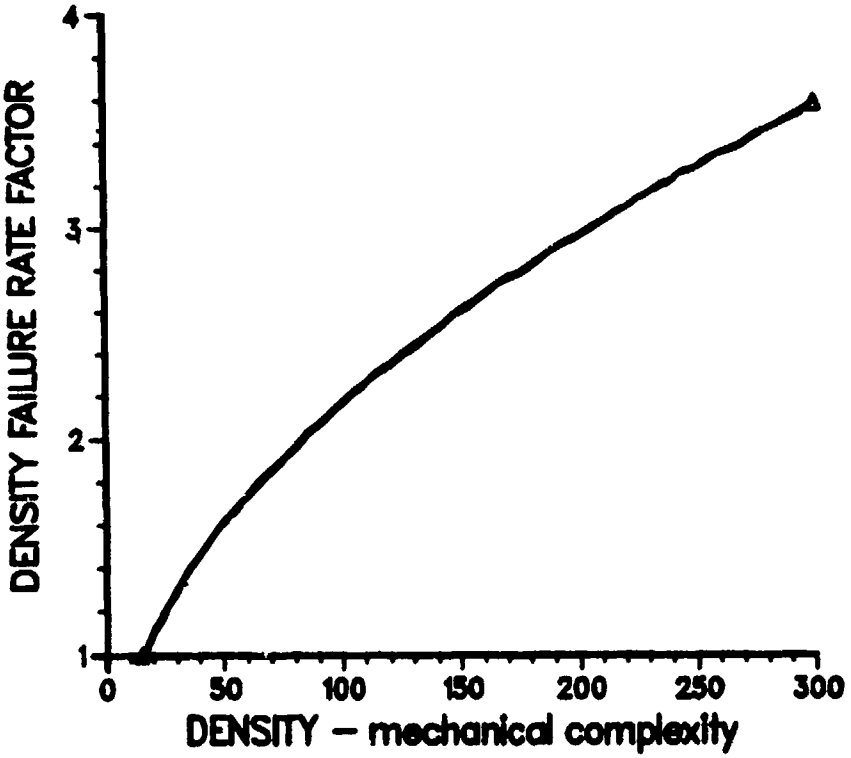


Figure 12. Hybrid: Density Impact on Failure Rate

The thick/thin film trimming required to obtain a particular parameter greatly affects the power density. As the device is trimmed, the power density increases. MIL-STD-883B restricts trimming to a maximum of 50 percent of the original size, thus creating the need for power density derating. In establishing the derating requirements for power density, the individual design limits have to be taken into consideration to allow for design changes. The power density derating chosen supports the established one. Based on this rationale, the derating criteria specified in section 2.2 (Table 1) was selected.

3.3 Basis for Complex Integrated Circuit Derating

The results of the survey (appendix 3) revealed no specific data related to integrated circuits. The lack of industry response to integrated circuitry has required investigation of derating criteria to be developed through MIL-HDBK-217D. The majority of the documents that address integrated circuitry technology, including MIL-HDBK-217D, consider two factors, circuit complexity and circuit function. Complex integrated circuit devices begin with the criteria of greater than 100 equivalent gate logic elements. The different technologies, bipolar, MOS, and CMOS each define the number of gate equivalents differently, according to MIL-HDBK-217D. Here is the MIL-HDBK-217D definition of the gate equivalents:

1 Bipolar: Gate equivalents = $\frac{\text{number of transistors}}{2.5}$

2 CMOS: Gate equivalents = $\frac{\text{number of transistors}}{3.75}$

3 MOS: Gate equivalents = $\frac{\text{number of transistors}}{3.0}$.

Each element of MIL-HDBK-217D impacting the failure rate was investigated to determine breakpoints. The impact of the quality and environmental factors on the failure rate have previously been discussed in section 3.1.

The temperature acceleration factor for complex integrated circuits is the same factor used for all the microcircuit devices. Figure 1 previously addressed in section 3.2, Basis for Hybrid Derating, shows the temperature acceleration factor impact in relation to junction temperature for all the technologies. Analysis of the breakpoints of the curves in Figure 1 concluded that the junction temperature was to be 85, 100, and 110°C for levels I, II, and III, respectively. For the present time, we will assume these points are still valid. They may be modified upon investigation of other failure rate drivers.

The voltage derating stress factor as presented in MIL-HDBK-217D is applied only to CMOS technology. It is based upon the recommended specification supply voltage and the operating supply voltage in actual application. There are two CMOS ranges in which the application voltage affects the failure rate, a value other than 1.0. These two ranges will be investigated separately. In both cases the numerical value is related to junction temperature. Figure 13 shows a plot of junction temperature versus the voltage stress multiplier. The multiplier is based on the minimum value for each voltage range. For example, the minimum value in the 12 to 15.5 volt CMOS range would be 0.11. This is derived by the applicable formula:

$$\pi v = 0.110e^{x}$$

where

$$x = \frac{0.168Vs(Tj + 273)}{298}$$

Vs = operating voltage in actual operating

Tj = device junction temperature (°C).

When the value of x goes to zero, the value of $v = 0.110$.

Using the same approach for the 18 to 20 volt recommended specification supply voltage, when x goes to zero in equation $\pi v = 0.068e^{x}$, the minimum is $\pi v = 0.068$.

Only one obvious breakpoint is highlighted in the curves in Figure 13. The breakpoint is associated with the 3 and 8 volt curves. The subject breakpoints are associated with a junction temperature of approximately

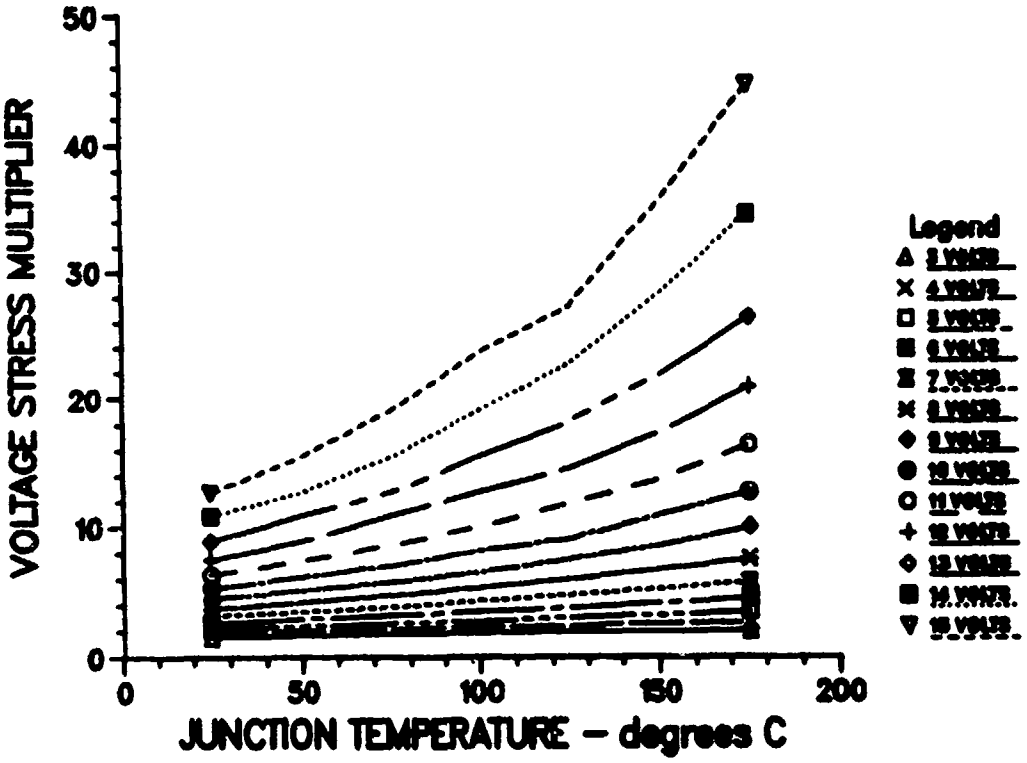


Figure 13. Complex IC: Junction Temperature versus Voltage Stress

125°C. The voltage stress multiplier at this specific point is approximately 27. Using the 125°C and 27 multiplier would tend to fix the level III derating and translate to an approximate percent of supply voltage derating of 0.85 across the application voltage range.

The CMOS recommended specification supply voltage in the 18- to 20-volt range is plotted in Figure 14. These curves show several breakpoints. They are at a junction temperature of 125°C with 16 and 18 volts, 100°C with 18 and 19 volts, and approximately 80°C with 20 volts. The voltage stress multipliers range from approximately 17 to 25. These three junction temperature breakpoints would tend to suggest temperature derating of 85, 100, and 125°C for Level I, II, and III, respectively. The respective derating associated with the supply voltage is approximately 80 percent.

The last term investigated is the circuit complexity factor. This term is solely dependent on the number of gates for the technology. MIL-HDBK-217D differentiates complexity factors for bipolar and MOS, while there is no separate complexity factor for CMOS technology. Figures 15 through 18 show the gate count impact on the failure rate for the bipolar and MOS devices. Each technology, bipolar and MOS, has two complexity components, C1 and C2. The results of complexity factor investigation for both bipolar and MOS produced no outstanding results. The curves (Figure 15-18) show that as the number of gates increase the impact on the failure rate also increased. The general slope of each curve is similar and the comparable factors (C1 and C2) of MOS technology are less impacted by increasing gate count than bipolar technology. An example of this impact

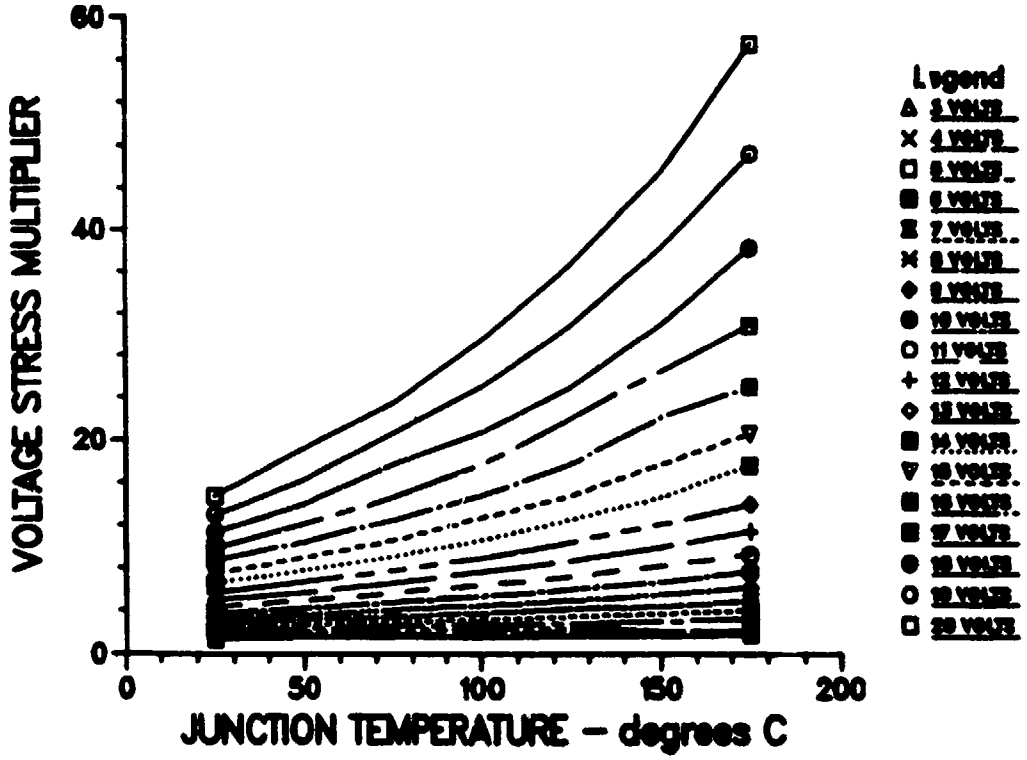


Figure 14. Complex IC: Junction Temperature versus Voltage Stress

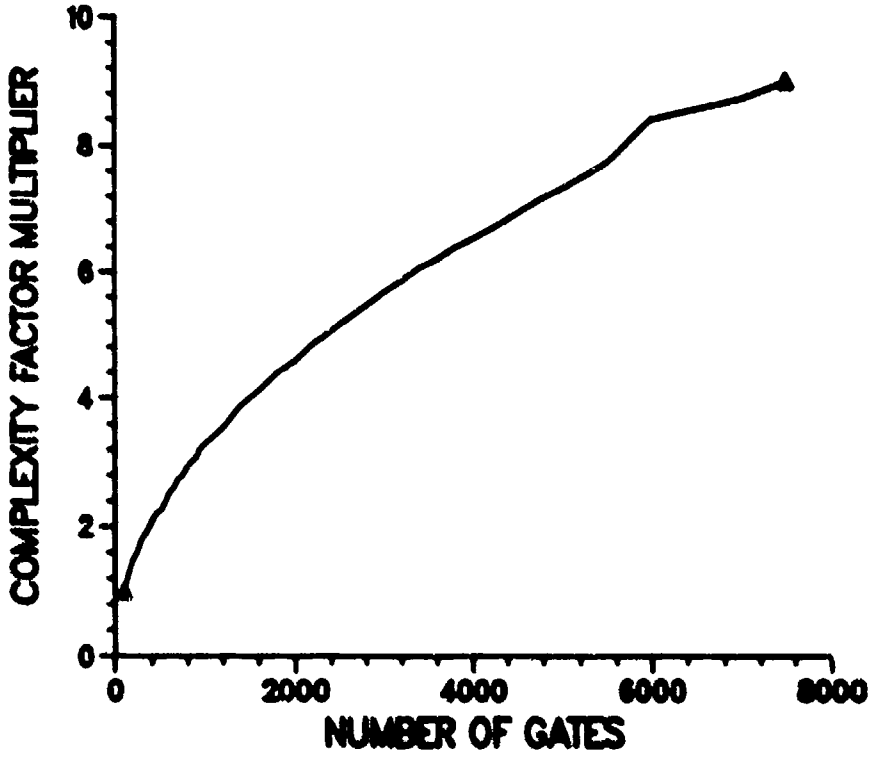


Figure 15. Gate Count Impact on Failure Rate of Bipolar Devices (C1 Complexity)

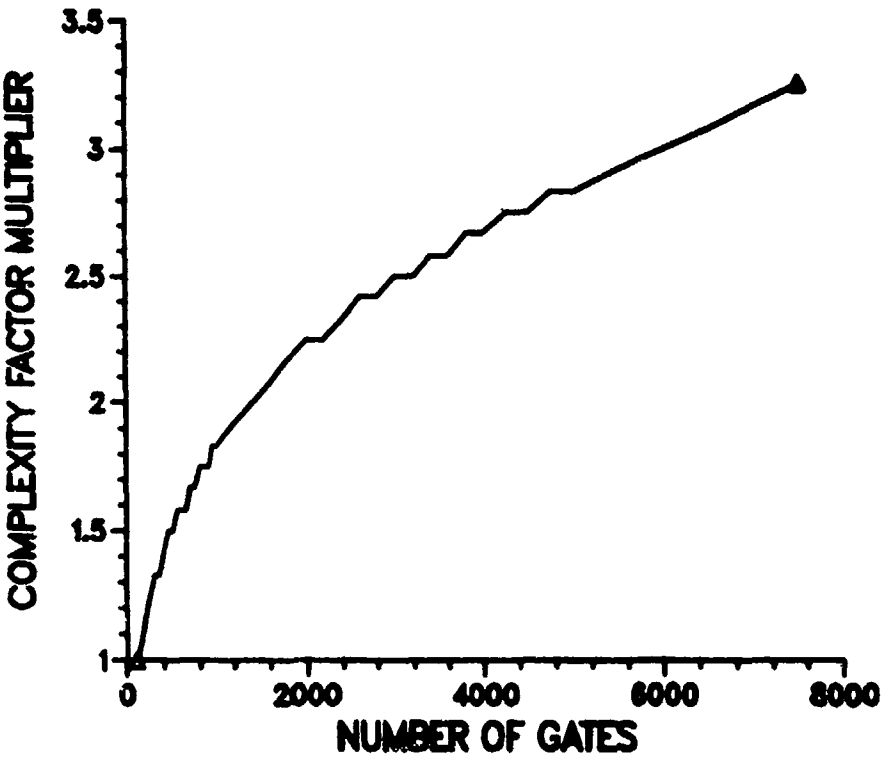


Figure 16. Gate Count Impact on Failure Rate of Bipolar Devices (C2 Complexity)

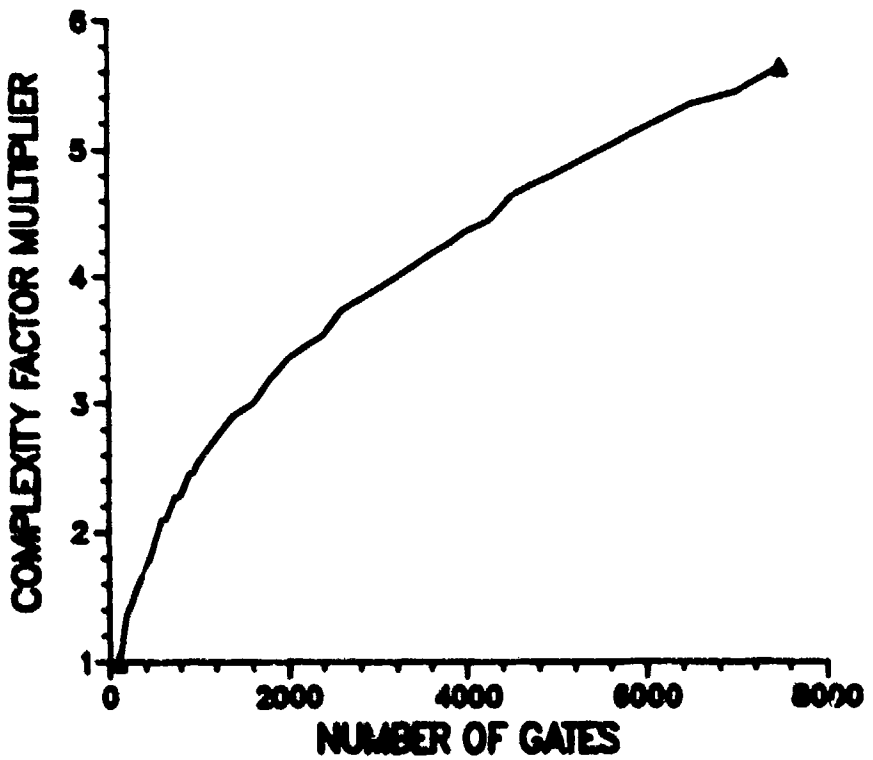


Figure 17. Gate Count Impact on Failure Rate of MOS Devices (C1 Complexity)

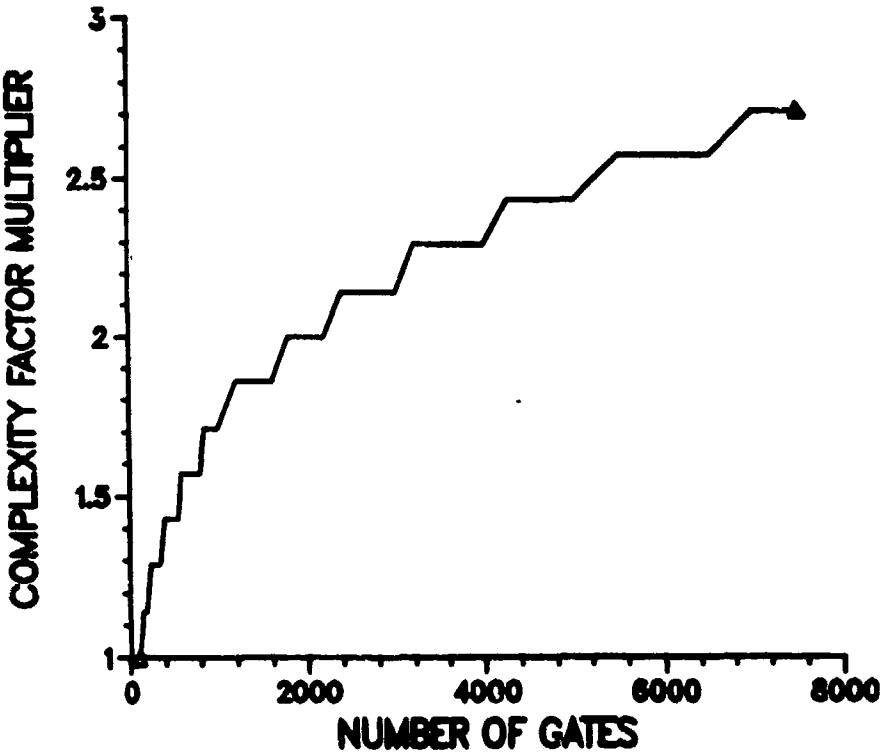


Figure 18. Gate Count Impact on Failure Rate of MOS Devices (C2 Complexity)

is the C1 factor of bipolar for 7500 gates (Figure 15) is greater than the C1 factor of MOS (Figure 17) for the same number of gates (9.0 versus 5.6). The same impact can be observed in Figures 16 and 18 for the C2 factors. observed in Figures 16 and 18 for the C2 factors.

These derating criteria for complex integrated circuits, LSI, VHSIC, VLSI, and microprocessors, are summarized in Table 1, section 2.3. The selection of the specific derating levels was based on the information and analysis conducted within Martin Marietta and the survey response from industry. The analysis presented herein tends to support the industry response; that is, it generally correlates with the most often selected parameter.

3.4 Basis for Memory Device Derating

The industry survey did not produce any information regarding memory devices. Also, the derating criteria received from other companies did not cover memory devices. Because of the unavailability of external data and derating for these devices, Martin Marietta must again resort to internally available data, analysis, and MIL-HDBK-217D.

The memory devices defined for derating guidelines include three specific technologies. They are: 1) bipolar, 2) MOS, and 3) bubble. In the bipolar and MOS technologies, the memory group can be divided into RAM and ROM memories. The RAMs, in turn, can be categorized as static and dynamic.

The basic difference between dynamic and static RAMs is in the way they store data. The static RAM uses a flip-flop to store a bit, while the dynamic RAM uses a capacitor. The static RAM is easier to use because refresh logic is not required. In addition, static RAM control signals tend to be easier to generate because cycling is usually unnecessary. The dynamic RAM draws less power. The static RAM draws power continuously to sustain its flip-flops, while the dynamic RAM draws minimal power between cycles. The dynamic RAM die size tends to be smaller than the static RAM die size. The size is due to the difference in cell designs, and the die size of the dynamic RAM is often at least 20 percent smaller than that of a comparable static RAM from the same manufacturer.

The ROM is a random access memory in which the stored information is fixed and non-volatile. A semiconductor ROM is a circuit whose stored information is fixed by a masking operation during wafer processing. Bipolar ROMs offer access times in the 25 to 50 nanosecond range for transistor, transistor logic (TTL) and 15 to 20 nanoseconds for (ECL), which represent an order of magnitude improvement over equivalent MOS circuits. Historically, MOS ROMs have offered greater bit densities than have bipolar circuits. Most recently, however, technological advances have narrowed the gap in bit densities.

Perhaps the most important characteristics of a memory chip are the number of bits, speed capability, and power dissipation. The supply voltage and current play a major role in controlling the power distribution. Again, since no data collected shed light on memory derating and failure rate impact, MIL-HDBK-217D was used to derive the memory derating criteria. The same factors affect memory failure rate as affect integrated circuits as a whole, with the addition of a number of bits factor. The temperature acceleration factor (Figure 9), quality level factor (Figure 1), and voltage stress factor for CMOS technology (Figures 13 and 14) previously investigated will be applicable to this memory discussion.

The derating parameters developed for the complex integrated circuits based on the effect of these factors (section 3.3) will also be applicable to the memory device (RAM or ROM) derating. These parameters include the supply voltage and junction temperature. Due to the similarities with the complex integrated circuit analysis and the importance of the current to the operation of the device, the same derating will be specified for the output current.

The analysis conducted on memory devices did not discover any substantial information on the operating frequency. Therefore, a conclusion could not be drawn as to the effect of derating this parameter.

The C1 and C2 factors previously discussed for complex integrated circuits were based on gate count. They were replaced with C1 and C2 factors based on a device number of bits complexity for memory devices. Figures 19 through 21 show a plot of the impact of bit count on failure rate of various memory types. The curves are interesting, and at several points appear to have a breakpoint or change of slope, but it is not customary or practical to derate a memory device based on a percentage of bits.

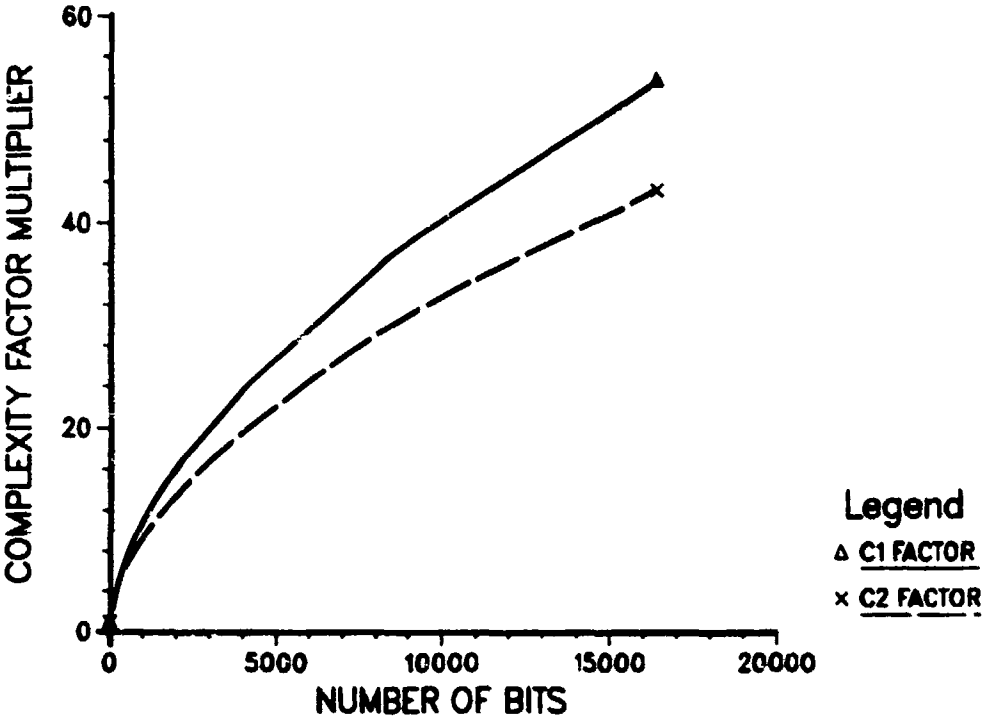


Figure 19. Bit Count Impact on Failure Rate of Bipolar RAM Devices

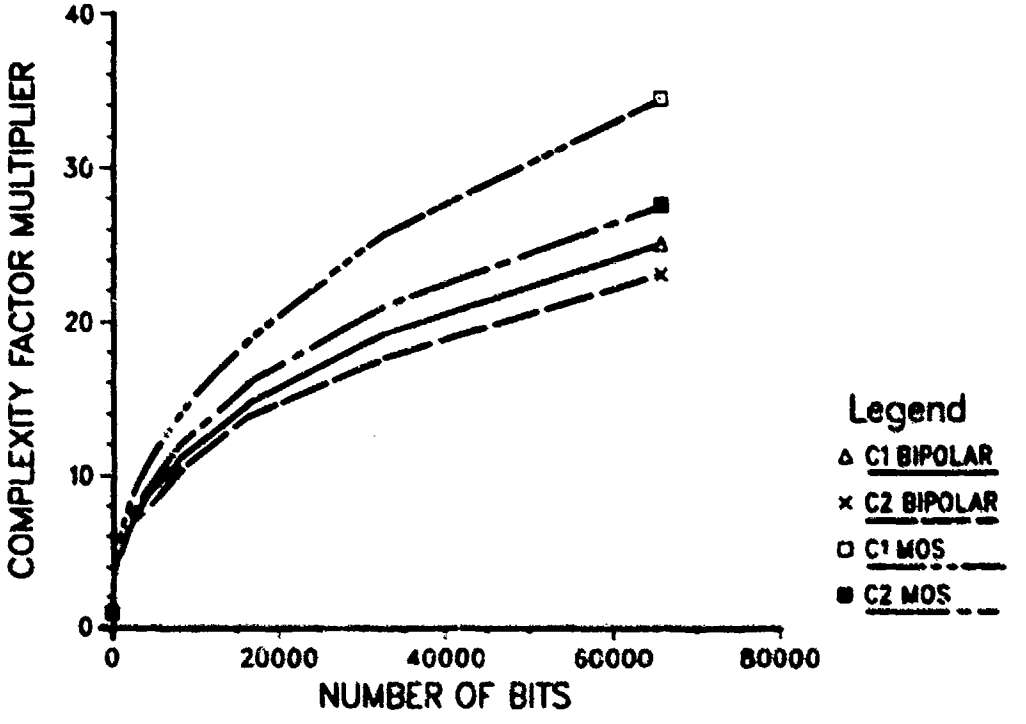


Figure 20. Bit Count Impact on Failure Rate of ROM and PROM Devices

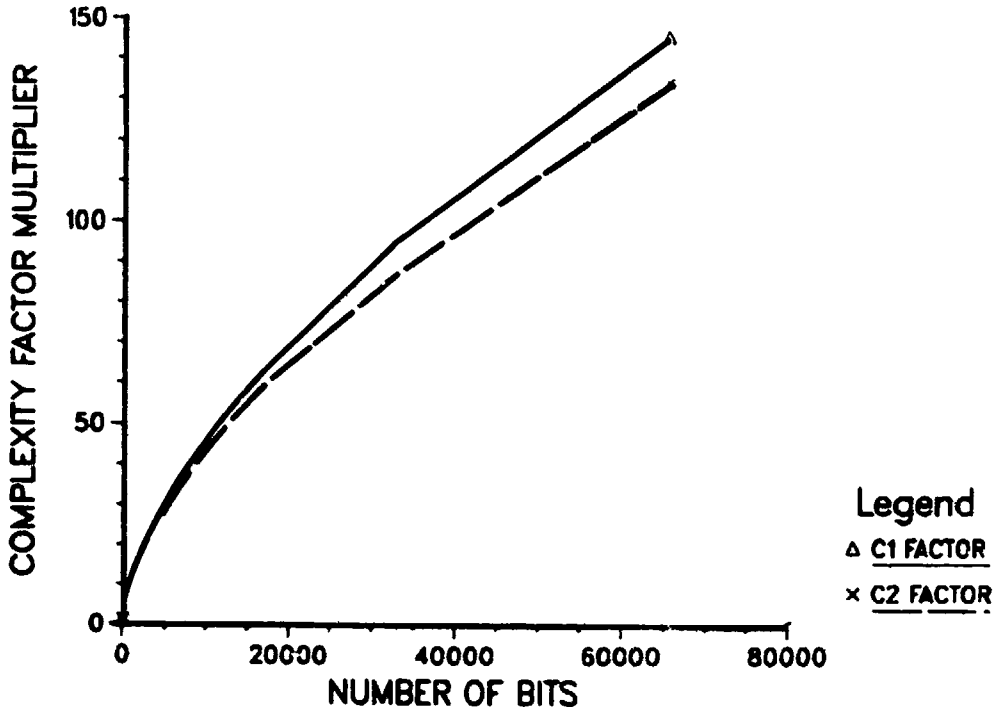


Figure 21. Memory Devices: Bit Count Impact on Failure Rate of MOS RAM Devices

Based on this analysis, these derating criteria for RAM or ROM devices, as it appears in Table 2, was selected.

Bubble memory technology (both device and material) is significantly different from silicon integrated circuitry. However, they are both based on a batch manufacturing process, with the cost of a function very strongly dependent on the functional density per batch and manufacturing yields. From this point of view, bubble technology has some very major disadvantages, coupled with some potential long-term benefits.

First of all, as a device it is very well suited to serial storage of data. Although it is slower than any silicon integrated circuit based storage circuit, it is non-volatile (or at least it can be designed to be). Secondly, it can also be used to perform very simple logic functions which allow data to be stored and retrieved efficiently. Thirdly, it can be used to preamplify the otherwise very small signal magnetically, so it can be used to design a reasonably self-contained memory chip.

The bubble memory has major disadvantages, which are:

1 Very high material cost, caused by both very high initial substrate cost and a very expensive, difficult, and low productivity liquid phase epitaxy deposition process. Material cost is approximately 30 to 50 times higher than silicon.

2 A very high packaging cost, since every circuit has to have an individually adjusted bias field and a rotating magnetic field limit into the package.

3 Limited operational temperature range.

Potential long-term benefits that stimulate bubble memory development are:

1 A processing method that typically requires only three masking steps, only one of which is critical, compared to the six and more for silicon.

2 There is much room for improvement in bit density, since bubble memory is based on a relatively simple design.

3 Because it has only one critical masking step and no critical alignment requirements, it is a technology best positioned to take advantage of improvements in pattern definition techniques.

Due to the dearth of information received on bubble memory devices, MIL-HDBK-217D was used in the determination of the derating criteria for those memory devices. The approach taken by MIL-HDBK-217D is to divide the overall bubble memory operating failure rate into two parts. They are: (1 control and detection structure, and 2) memory storage area. Each of these parts has an associated failure rate that is accumulative in order to produce the overall device failure rate. The factors affecting the failure rates of both the control and detection structure, along with the memory storage area, were then investigated. The analysis performed in section 3.1 (Figures 1 through 6) on the effect of the quality and environmental factors on failure rate also applies to bubble memories.

The device complexity factors, C_{11} and C_{21} for the control and detection element, and C_{12} and C_{22} for the memory storage area, were investigated and their effect plotted in Figures 22 and 23, respectively. These complexity factors are based on the number of bubble chips per device and therefore do not represent a practical derating parameter.

The next factors reviewed were the duty cycle and the write duty cycle of the control and detection structure. The duty cycle factor is application dependent, since it is a function of the usage the bubble device experiences.

The impact of the duty cycle factor on failure rate is plotted in Figure 24. The result is a straight line, indicating that this factor has a linear relationship with failure rate. It is not practical or customary to derate a device based on its usage. The write duty cycle is also based on the usage of the bubble device, and was not used for derating. A plot was generated showing the impact of the write duty cycle on the failure rate. It is shown in Figure 25.

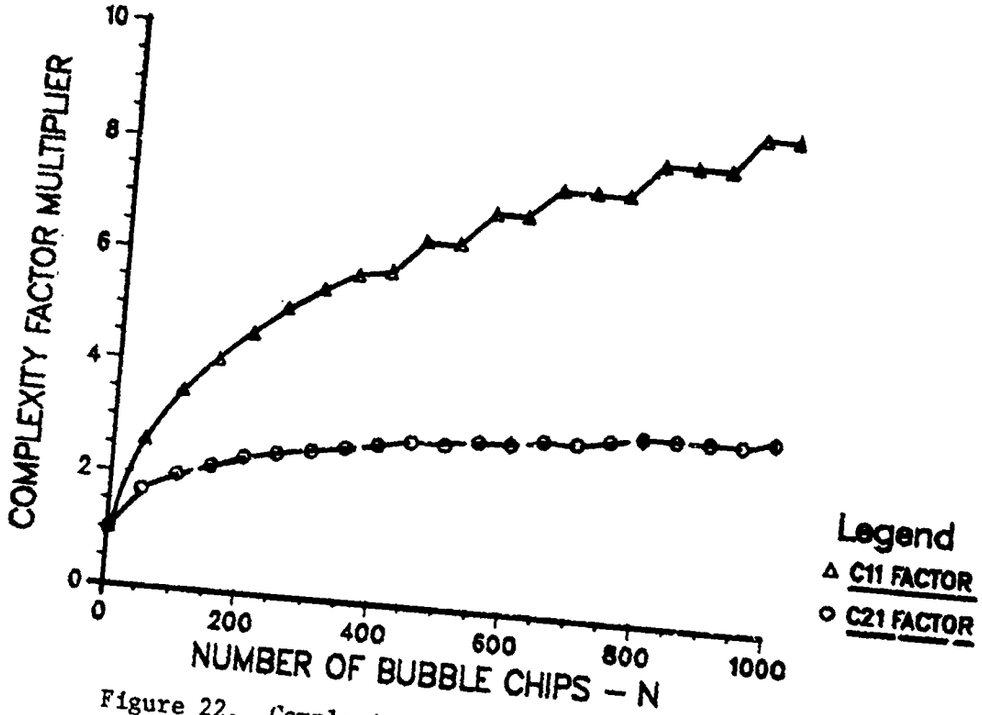


Figure 22. Complexity Factor Impact on Failure Rate of Bubble Memories

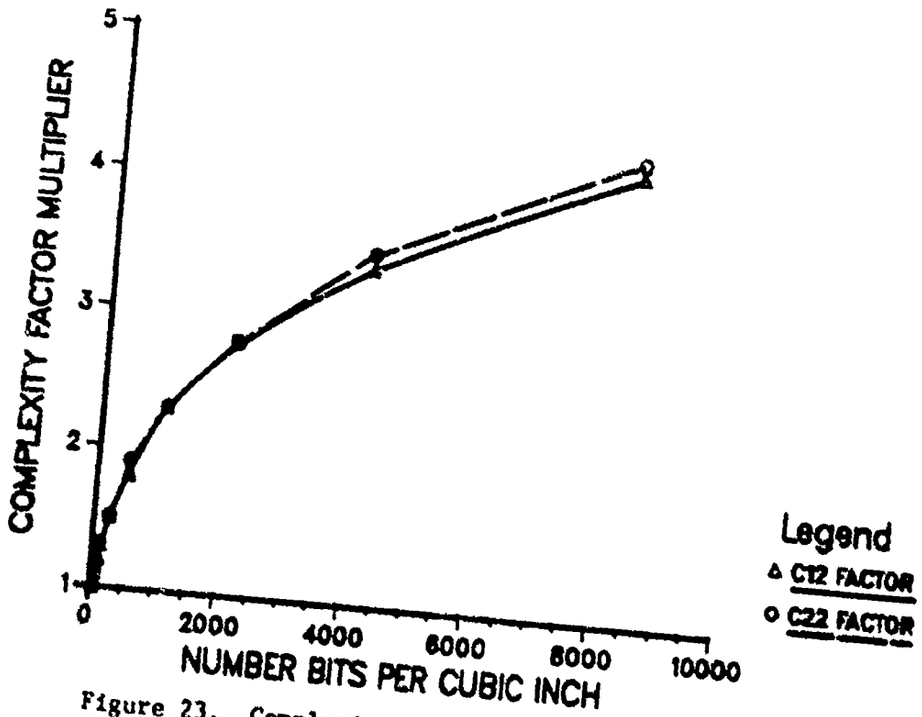


Figure 23. Complexity Factor Impact on Failure Rate of Bubble Memories

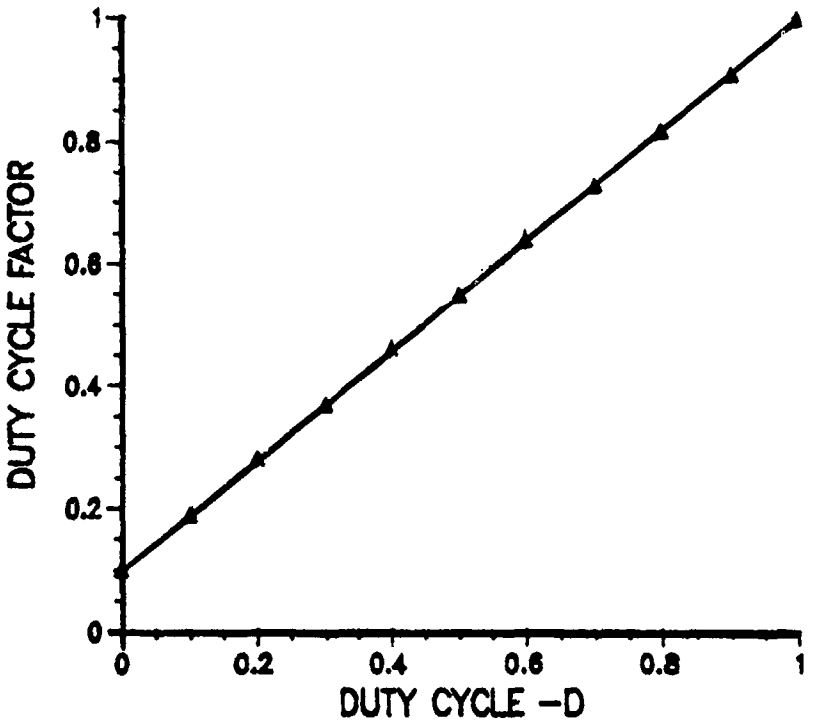


Figure 24. Duty Cycle Factor Impact on Bubble Memory Failure Rate

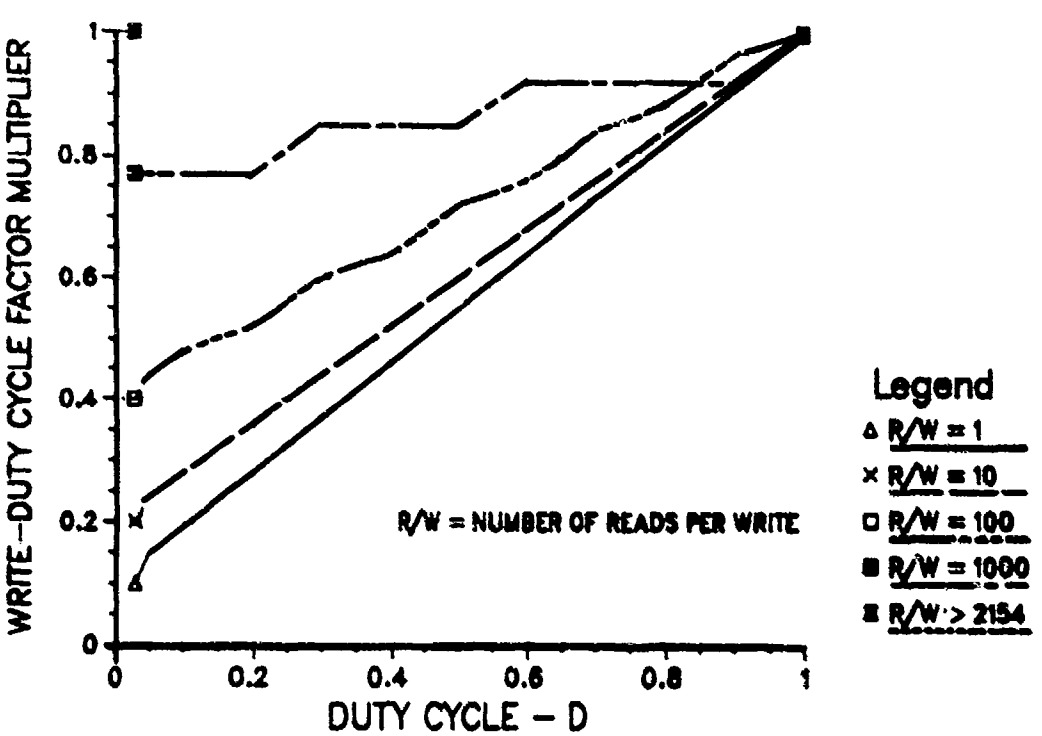


Figure 25. Write-Duty Cycle Factor Impact on Failure Rate of Bubble Memory

Based on this analysis of bubble memory devices, it was concluded that the maximum ambient operating temperature would be the only parameter specified for derating. Other required derating will be applicable to those microelectronic devices that compose the external support required for proper bubble memory operation. The criteria for derating bubble memories was summarized in Table 4, section 2.4.

3.5 Basis for Microwave Device Derating

The microwave device derating section covers the following device types:

1 GaAs FETs

2 Transistors (microwave)

3 IMPATT diodes

4 Gunn diodes

5 Varactor diodes

6 Step recovery diodes

7 PIN diodes

8 Tunnel diodes

9 Silicon detectors or mixers

10 Germanium detectors or mixers.

The industry survey did not reveal any data or information on microwave devices. Limited information received from the Martin Marietta survey, and MIL-HDBK-217D, were used as the basis for microwave device derating.

The results of the Martin Marietta survey are summarized in Figure 47 in Appendix 3. The information received via the survey served as a means of grouping the device types and establishing derating parameters. Actual derating values were not received, with the exception of a recommended junction temperature of less than 100°C or 110°C for all microwave devices.

After grouping the devices as specified in section 2.5, Microwave Device Derating, MIL-HDBK-217D was used for the actual development of the derating criteria. The device grouping, based on the amount of electrical stress typically present during operation, is supported by MIL-HDBK-217D. The part operating failure rates and the factors that impact them were investigated for each device grouping in order to determine the derating criteria. In general, the factors investigated were:

1 Quality level

2 Environment

3 Application

4 Frequency

5 Power

6 Temperature.

These factors are not all applicable to each group of devices. Also, the discussion in section 3.1 on the effect of the quality level and environment on the failure rate applies directly to the microwave devices.

3.5.1 GaAs FETs

MIL-HDBK-217D indicates that the GaAs FET failure rate is primarily dependent upon power and temperature stresses. The impact of case or ambient temperature and the power stress ratio on the GaAs FET failure rate is plotted in Figure 26. It appears that a break in the curve emerges at a stress ratio of 0.60 and a temperature of 85°C. This indicates a sharp rise in the failure rate due to overstressing. The objective of derating is to minimize failures and to maintain a minimum failure rate, so it would be appropriate to select a failure rate factor that would accomplish this objective. Three is the approximate designated factor. Above this value, the rise in failure rate is considerably more dynamic. The failure rate factor associated with the 0.60 stress ratio is 3.34. This was established as the Level II power dissipation derating value. Level I and Level III values were 0.50 and 0.70, respectively.

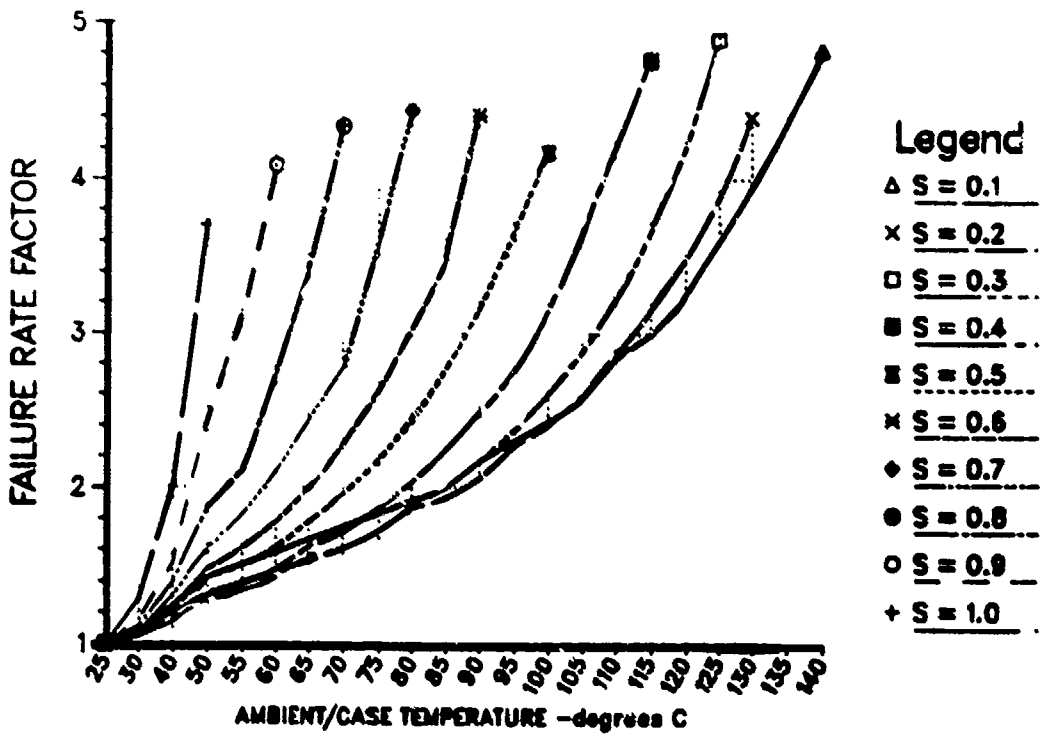


Figure 26. Temperature Impact on Failure Rate of GaAs FET

The relationship between the ambient temperature, junction temperature, and power dissipation is represented by the following equation

$$T_j = T_A + \theta_{JA}P_d.$$

The junction temperature can be controlled by derating the power. Power derating also assures a low failure rate factor. Junction temperature derating levels were established by utilizing vendor specifications for GaAs FETs. A range of θ_{jA} of 200 to 260 degrees centigrade per watt was used as an input into the equation, along with their respective power dissipation values. The power was derated and the resulting junction temperature computed for the two endpoints of the θ_{jA} range.

Here is a summary of the outcome of this work:

P_d = 50 percent yields T_j midpoint = 87.5°C
P_d = 60 percent yields T_j midpoint = 100°C
P_d = 70 percent yields T_j midpoint = 112.5°C.

Based on these calculations, the junction temperature derating for levels I, II, and III were established as 95, 105, and 125°C, respectively.

Breakdown voltage was another electrical characteristic suggested for derating. Based on the assumption that the power dissipation and junction temperature values were as stated here, conservative and perhaps standard breakdown voltage derating levels were established. They were:

Level I = 0.60
Level II = 0.70
Level III = 0.70.

The remaining factors affecting the GaAs FET failure rate are of no consequence, since the application factor is power related and the assumed complexity factor is one.

3.5.2 Transistor/IMPATT/Gunn Diodes

IMPATT and Gunn diodes were grouped with microwave transistors. A suggestion received in the Martin Marietta survey pointed out that since they are all high electrically stressed devices, diodes and transistors should be in the same group. Using the failure rate model for microwave transistors in MIL-HDBK-217D, the factors which were investigated due to their impact on failure rate were operating power and frequency, and temperature.

Several observations were made by plotting the impact of failure rate of the operating power and frequency (Figure 27). First, as the power level increases, the failure rate factor increases more rapidly at lower frequencies. Second, as the frequency increases, the failure rate factor rises sharply to above thirty for all power settings. Accordingly, the failure rate factor was limited to ten.

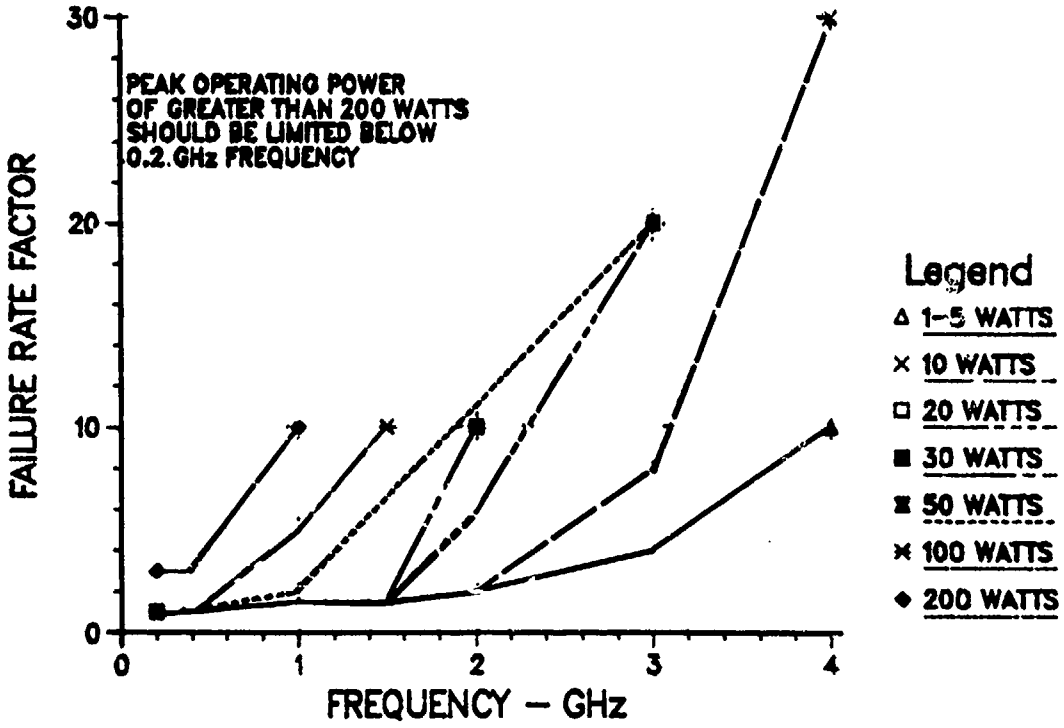


Figure 27. Operating Power and Frequency Impact on Failure Rate of Microwave Transistors

The junction temperature impact on failure rate based on voltage stress was plotted in Figures 28 and 29, respectively, for aluminum and gold transistor material. In both figures, a junction temperature of 100°C represents a sharp, drastic rise in the failure rate factor. The plot for the aluminum material (Figure 28) attains a failure rate factor of ten at a junction temperature of approximately 127°C. For the gold material (Figure 29), a failure rate factor of two was achieved at a junction temperature of approximately 130°C. Based on the initial rise in the failure rate factor at T_j = 100°C, Level I and II derating criteria were set at 95°C and 105°C, respectively. Level III was set to 125°C.

Figures 28 and 29 show that the maximum operating junction temperature of 200°C cannot be attained at voltage stress ratios of above 0.60. Therefore, voltage breakdown derating levels I, II, and III were set at 0.60, 0.70, and 0.70, respectively.

Based on conventional practice, the power dissipation derating levels were set as specified in Table 6, Transistor/IMPATT/Gunn Derating.

3.5.3 Varactor/Step Recovery/PIN/Tunnel

These devices are categorized together, since they are all low electrically stressed devices. They are also addressed in this grouping in MIL-HDBK-217D. Figure 30 represents the ambient or case temperature impact on failure rate based on the power stress ratio. At an ambient or case temperature of 85°C and a power stress ratio of 0.50, a break in the curve

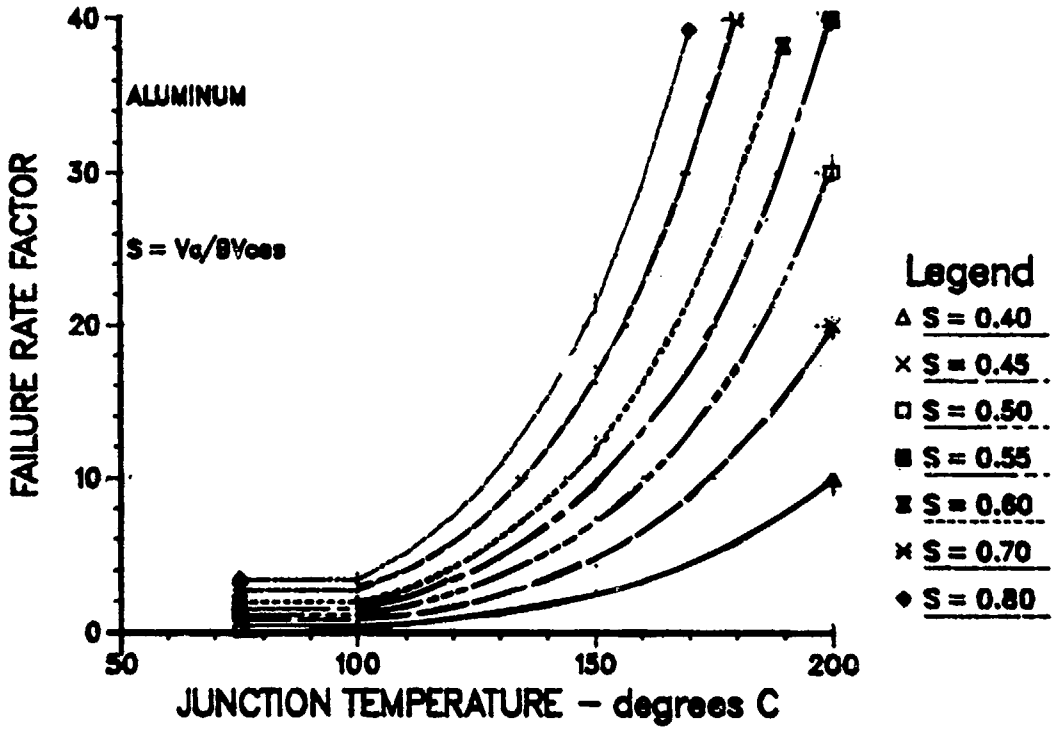


Figure 28. Junction Temperature Impact on Failure Rate of Microwave Transistors

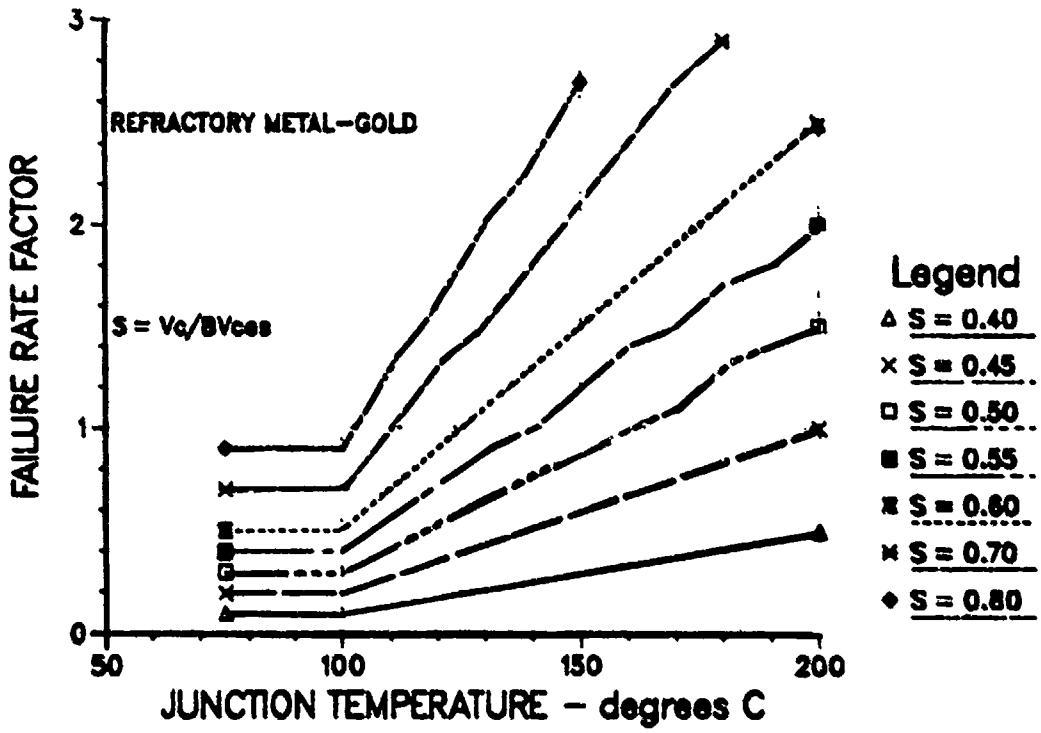


Figure 29. Function Temperature Impact on Failure Rate of Microwave Transistors

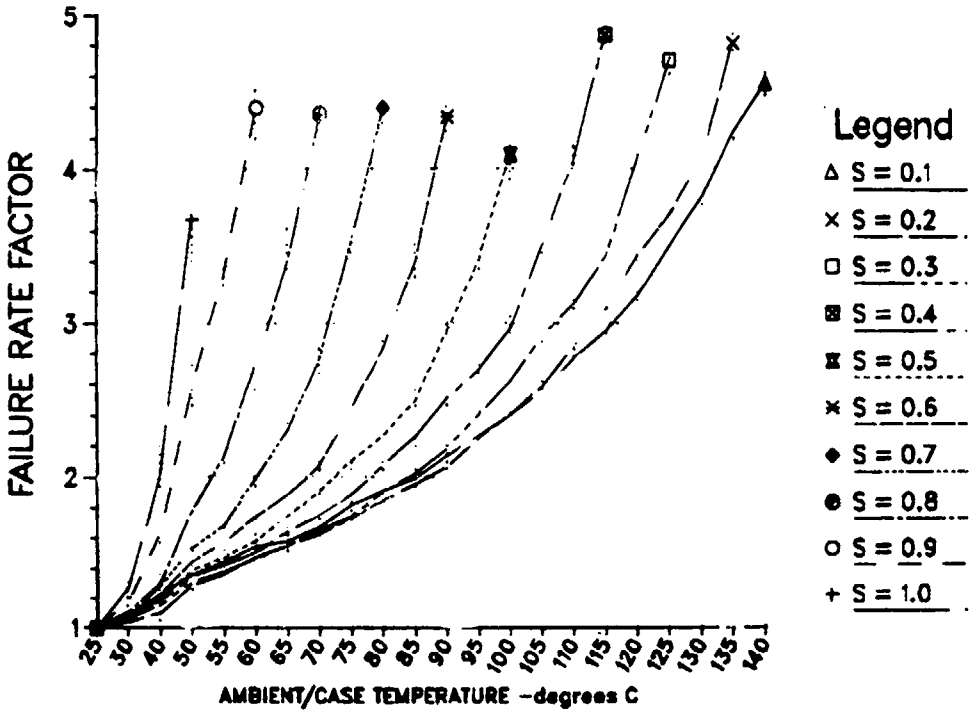


Figure 30. Temperature Impact on Failure Rate of Varactor, Step, Recovery, PIN and Tunnel Diodes

appears which is below the reasonable (in our judgement) failure rate factor of three. At temperatures above 85°C, the failure rate begins to rise much more rapidly at the 0.50 stress level. Based on this and conventional practice, the power dissipation levels (I, II, III) were set at 0.50, 0.60, and 0.70, respectively.

The derating criteria for the junction temperature was set at 95, 105, and 125°C for Level I, II, and III respectively to be consistent with the derating already established. There was no information received to disprove these values. The reverse voltage was derated to 0.70 across the three levels based primarily on convention for these type of devices.

3.5.4 Silicon and Germanium Detectors/Mixers

Detectors and mixers are classified as low electrically stressed devices. The base failure rate is the main factor affecting the operating failure rate of these devices. The base rate is driven by the power stress ratio and the ambient or case temperature. The detectors and mixers are divided into categories based on their material. The silicon devices have a much wider temperature range than the germanium. The germanium devices are not recommended for new design. However, the germanium devices were researched and derating criteria established.

The failure rate factors for each stress ratio, as they changed with respect to the ambient or case temperature, were plotted in Figures 31 through 35 for the following devices:

1 Silicon mixers

2 Germanium mixers

3 Silicon detectors

4 Silicon Schottky detectors

5 Germanium detectors.

The failure rate should be held below three, since a factor above that results in a rapid increase in the failure rate, due to overstressing. The curves for both silicon and germanium devices indicate that a power stress ratio of at least 0.50 will hold the failure rate factor below three and still provide a sufficient, nonrestrictive derating requirement. It was established that Level I, II, and III power dissipation derating criteria would be set at 0.50, 0.60, and 0.70, respectively.

The reverse voltage was set at 0.70 across all three levels for both the silicon and germanium devices. The voltage rate was based on the nature of the devices and their low stress applications.

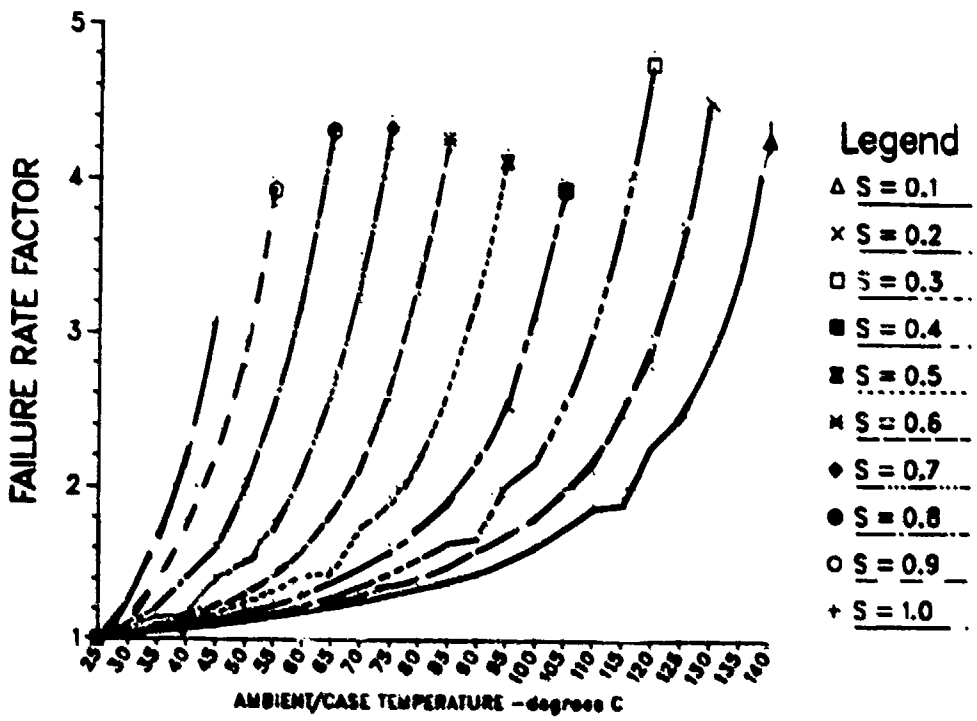


Figure 31. Temperature Impact on Failure Rate of Silicon Microwave Mixers

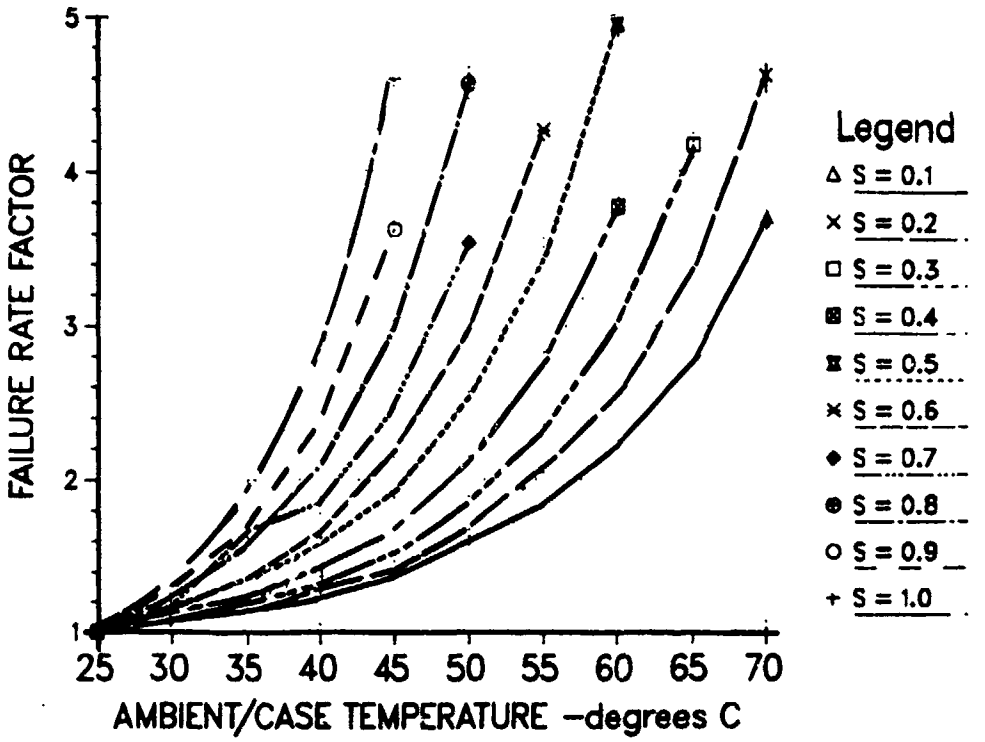


Figure 32. Temperature Impact on Failure Rate of Germanium Microwave Mixers

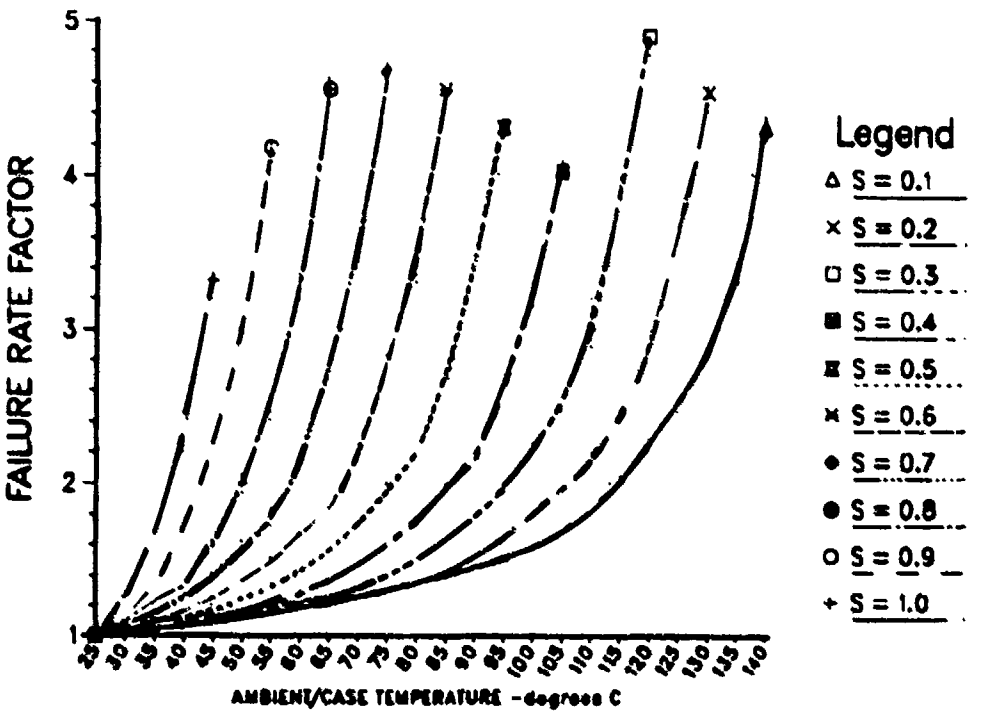


Figure 33. Temperature Impact on Failure Rate of Silicon Microwave Detectors

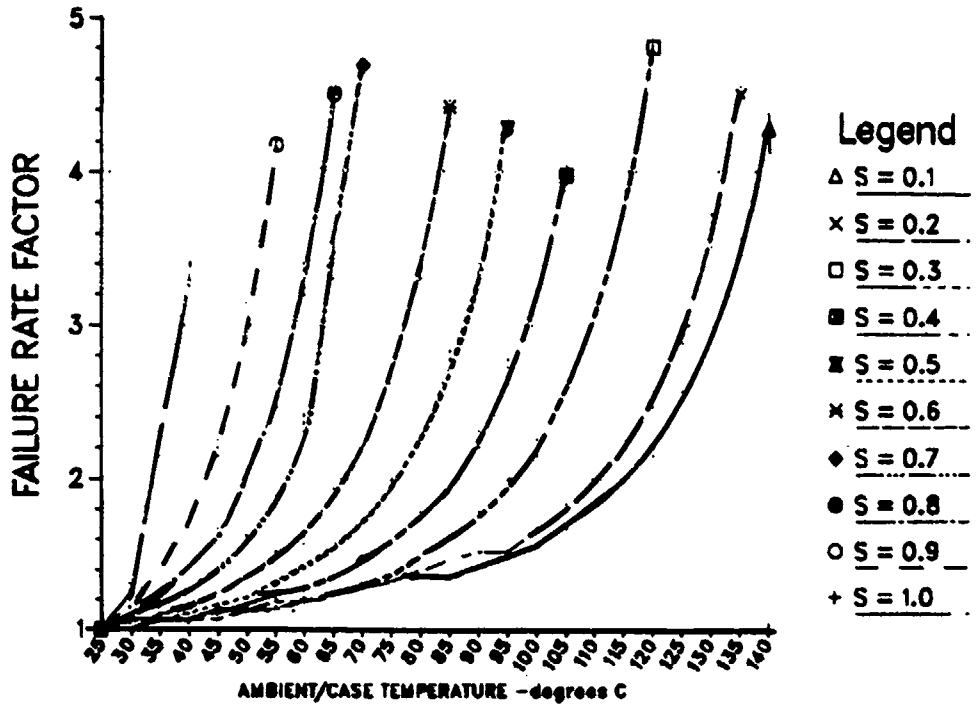


Figure 34. Temperature Impact on Failure Rate of Silicon Schottky Diode Detector

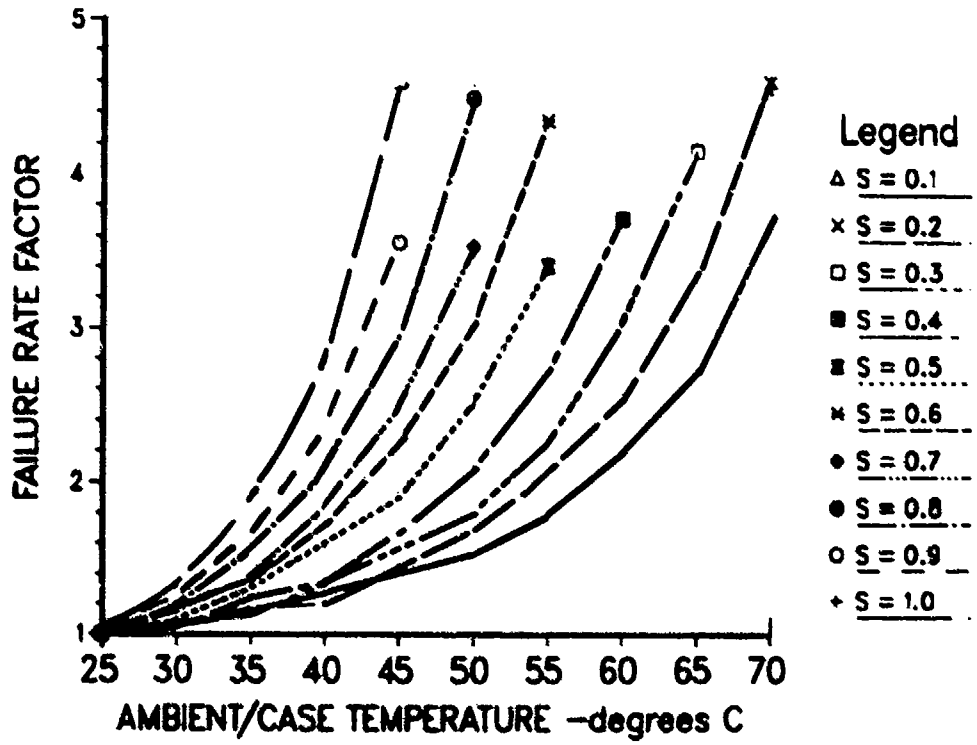


Figure 35. Temperature Impact on Failure Rate of Germanium Microwave Detector

The junction temperature does vary with material used. Junction temperatures of 95, 105, and 125°C for the silicon devices at Levels I, II, and III, respectively, were selected for consistency. The temperatures were also selected to conform with the recommendation of limiting T_j to 110°C. Junction temperatures of 75, 90, and 105°C for the germanium devices were selected at levels I, II, and III, respectively. Temperatures selected were based on the one industry survey response on germanium devices.

3.6 Basis for SAW Device Derating

Surface Acoustic Wave (SAW) devices were specified as one of the newest technologies requiring derating guidelines and applications. Because of the absence of published information on SAW devices, the industry survey was used. The survey revealed that two companies are primarily involved in the development of these devices. General information about SAW devices (i.e., design processes, fabrication, etc.) was obtained, but published derating guidelines were not available, due to the recent technology development and the design of the device. Therefore, the suggested derating parameters and values must be based on discussions held with those knowledgeable in the area and the basic device design and applications.

There are two important characteristics about SAW devices which solicit interest in terms of their usefulness: 1) the wavelength and the directly related propagation velocity, and 2) surface propagation. Traits which make SAW devices attractive are actually features inherent to the waves themselves.

The wavelength of an acoustic wave of a given frequency is about 10^5 times shorter than that of an electromagnetic wave of the same frequency. Similarly, the propagation velocity is 10^5 times slower. This suggests that a one or two centimeter long SAW device is equivalent to several thousand electromagnetic wavelengths. Many kinds of signal manipulations involve devices measured in wavelengths, thus creating an interest in SAW device application.

Surface propagation is the other characteristic that makes SAW devices useful. Acoustic waves propagate along the surface of a solid in a preferred direction. These acoustic waves, for all practical purposes, do not extend more than two wavelengths below the surface, with most of the energy at a depth of one wavelength or less. Therefore, energy can be sensed and manipulated by metallic elements applied to the surface of the piezoelectric substrate.

A SAW device usually consists of the SAW element on its substrate plus any auxiliary elements, such as an amplifier or matching elements, and the packaging of the complete device. The electrodes in actual SAW devices are composed of fingers extending from a common bus, forming a comb-like appearance. Two combs are placed so that their fingers overlap from opposite sides, with the voltage between the two opposite electrodes creating a strain on the substrate surface. As this strain varies with a changing voltage, a physical wave is generated at the surface. This wave has a frequency corresponding to the finger spacing.

This particular SAW layout or design is called an interdigital transducer. Most SAW devices have two transducers - one input and one output. The fingers in the transducers are spaced a quarter wavelength apart. The finger width is a quarter wavelength of the desired frequency. Interdigital transducers normally consists of dozens or hundreds of finger pairs. This principle is illustrated in Figure 36.

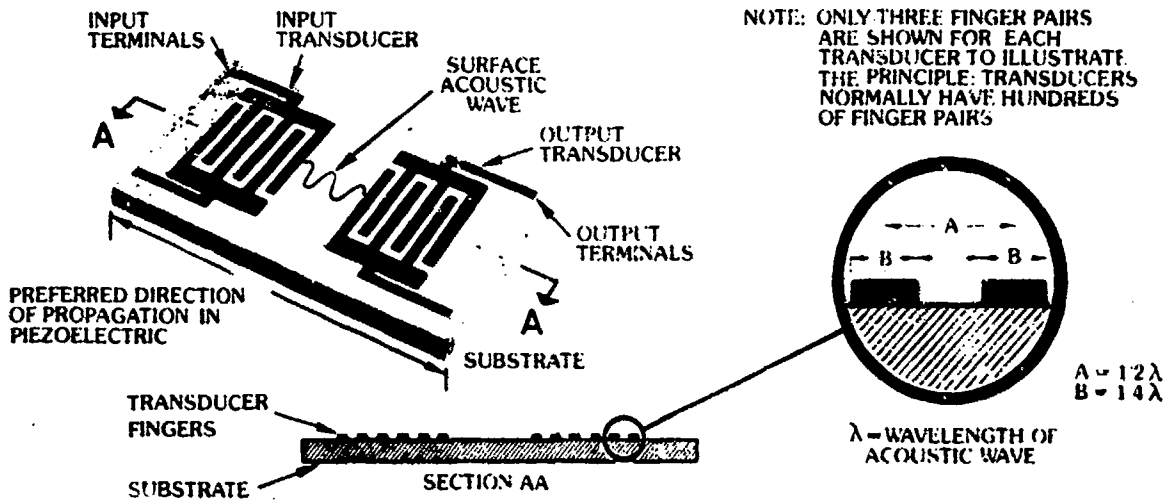


Figure 36. SAW Transducer

Four major applications of SAW devices are currently being used both commercially and by the military: They are:

1 Delay lines

2 Oscillators

3 Resonators

4 Filters.

A finite travel time for signals between the input and output transducers is inherent to the design of SAW devices. Due to this finite time, a SAW device can function as a delay line. The great advantage of a SAW delay line is the significant amount of delay that can be obtained in a very small device. A SAW device can also function as an oscillator by placing an amplifier in the loop between input and output transducers. The amplifier adjusts for the losses in the delay line, while the spacing of the fingers makes the transducers respond only to the selected wavelengths for which they were designed.

A SAW resonator consists of either one or two transducers, with a grating extending in both directions of wave propagation. The surface acoustic wave is launched in both directions from the input transducer and is reflected back and forth by the adjacent gratings. This creates a standing wave at the designed frequency which is determined by the finger

width and spacing. Since the finger width and spacing are chosen to resonate only at a desired wavelength, the resonator performs effectively as a filter.

SAW devices are tailored to the particular frequency and response desired for each application with a frequency range from 50 megahertz to about 2 gigahertz. There are a number of basic design variables (Table 11) which can be employed to obtain a design which complies with a specific set of requirements. The requirements are generally of the type listed:

1 Frequency

2 Bandwidth

3 Response

4 Insertion loss

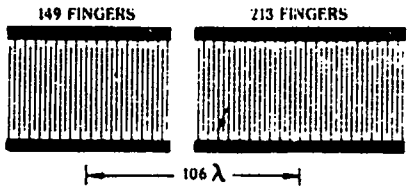
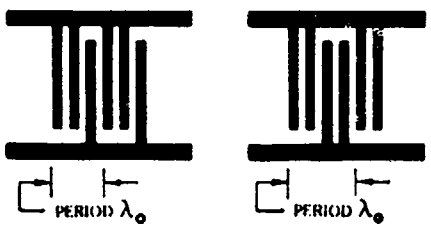
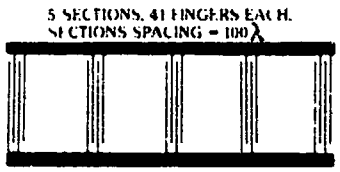
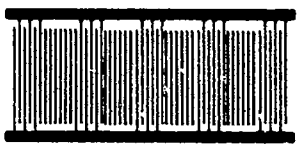
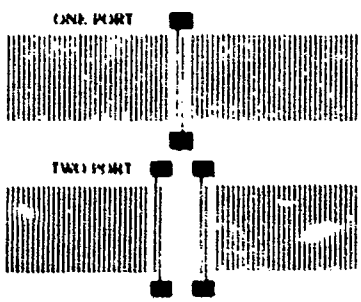
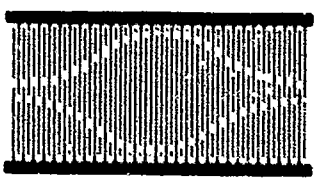
5 Frequency stability.

The frequency of a SAW device is determined by the width and spacing of the fingers. Finger spacing and width also generate the surface acoustic waves. The accuracy to which the desired center frequency is attained is dependent upon the precision of the mask making and fabrication steps. If a very exact frequency is required, the center frequency can be adjusted over a very small range by two techniques. One is to vary the mass of the fingers. Increasing the finger mass lowers the frequency very slightly. Another is to rotate the whole pattern very slightly from exact alignment along the principle axis of propagation. This allows the frequency to be tuned over a small range by phase shifting.

The acoustic waves generated at the surface of the substrate are affected by the presence of the fingers. The fingers cause the waves to be reflected back and forth between the fingers and the input and output transducers. This effect is caused by a discontinuity in the impedance of the substrate (represented by each finger). The discontinuity causes the waves to peak and be reflected. These reflections can be reduced by using the appropriate techniques listed in Table 11. The bandwidth of a SAW device is determined by the number of finger pairs in the transducers (delay lines) or the number of lines in the gratings (resonator). Adding to the number of finger pairs reduces the bandwidth.

Once the desired bandwidth is established, the next requirement is usually to reduce the responses outside this bandwidth to the lowest values possible (at least below some specified level). A narrow bandwidth is obtained by having a large number of finger pairs, but having numerous fingers results in reflected waves. To compensate for this, the thinned electrode transducer design variable is applied (Table 11). This involves eliminating groups of finger pairs until the transducer consists of multiple sets of a few finger pairs separated by space, while still maintaining the same finger width and spacing. The same frequency and bandwidth will result. To prevent waves from being reflected across the open spaces between finger sections dummy fingers are placed in the open sections.

TABLE 11. DESIGN VARIABLES

NUMBERS OF FINGERS AND TRANSDUCER SEPARATION		Number of fingers is related to bandwidth by the expression $\Delta f/fc=1/n$ where n is the number of finger pairs. Transducer separation determines delay.
NUMBER OF FINGERS PER PERIOD (WAVELENGTH). MAY BE TWO PER PERIOD (AS ABOVE) OR 3 OR 4 (AS SHOWN HERE)		Multiple fingers produce stronger harmonics. Three fingers per period provides stronger fundamental, 2nd and 4th harmonics, plus (decreasingly) seven additional harmonics. Four fingers per period provides stronger fundamental, 3rd, 9th and 11th harmonics.
THINNED TRANSDUCER (ALSO CALLED OPEN STRUCTURE)		Either or both transducers can be thinned. Removing groups of fingers while maintaining overall transducer length cuts down on second-order effects resulting from internal reflections.
DUMMY FINGERS		Dummy fingers (not connected to either electrode) can be inserted to absorb waves reflected across open spaces between finger sections.
ONE OR TWO PORTS (FOR RESONATORS ONLY)		One port resonator behaves exactly like a bulk crystal resonator and simplifies circuit design. Has high Q and low loss. Two port devices may have variable Q and are easier to build to given requirements.
APODIZATION		Changing the overlap of the fingers from opposite electrodes in a determined pattern results in weighting the frequency response of the transducer. Normally one of the transducers in a delay line is apodized. Note that the shortened fingers are continued (after a gap) by dummy fingers. These suppress multiple reflections across the open spaces and the associated second-order effects in the response curve.

Insertion loss is a major consideration in many SAW device applications. It is defined as the proportion of the input energy that does not appear at the output. There are two main causes of insertion loss:

1 Waves traveling away from transducer

2 Coupling coefficient.

The waves that are excited by the tranducer travel in both directions away from the transducer. In a delay line, only those waves that travel toward the output transducer are used; the other half are dissipated or absorbed. Half of the waves, or a quarter of the acoustic energy, that reach the output transducer will travel past it and be absorbed or dissipated. This translates into a minimum six decibel loss of the acoustic energy. Resonators, however, are able to utilize both sets of waves due to the gratings on both sides of the transducer. Delay lines typically exhibit a high insertion loss, whereas resonators are associated with a low insertion loss.

The insertion loss which results from the electromechanical coupling coefficient of the substrate material is a characteristic of the material itself. There is no way to change it. All commonly used substrate materials have low coupling coefficients, but some are much lower than others. Table 12 lists the coupling coefficients of commonly used substrate materials for SAW devices along with their temperature coefficients (how much the frequency of the device changes with each degree change in temperature). There is clearly a trade-off to be made between increased coupling coefficient and increased temperature stability depending on the device application. As the table indicates, the coupling coefficient of lithium niobate is much better than that of quartz, but its temperature coefficient is very poor and that of quartz is nearly perfect.

SAW devices, in most cases, are used in the very low power level of circuits. Therefore, even a 15 dB loss is translated into only a few milliwatts or less in absolute terms. However, the loss is undesirable since

TABLE 12. COUPLING COEFFICIENTS OF COMMONLY USED SUBSTRATE MATERIALS FOR SAW DEVICES

	Wave Velocity Meters per sec	Coupling Coefficient in Percent	Temperature Coefficient per Degree Centigrade
Lithium Niobate (Y,Z cut)	3488	4.82	94
Lithium Tantalate (Y,Z cut)	3230	0.66	35
Quartz (ST cut)	3158	0.116	Negligible

the amplification needed to compensate for it may introduce instability, phase distortion, or other types of noise in the signal. The coupling coefficient has to be considered in combination with the closely related frequency stability.

The frequency stability of SAW devices has to be considered on three different time scales, with each affected by different parameters:

1 Short term (less than a second)

2 Medium term (hours)

3 Long term (months).

The short term stability depends on the efficiency of the device, while medium term stability is largely determined by the temperature coefficient of the substrate material. Long term stability is a problem when frequency stability is required over periods of many months, as in the case of frequency sources. Experience indicates that with present technology the frequency drift demonstrated by SAW devices is not as desirable as that shown by crystal oscillators. The aging effect of SAW devices is at least one or two parts per million per month while the best crystal oscillator achieves a drift of about one part per million per year.

SAW devices are passive; they typically operate at a low power level and are low heat generators. Due to these operating characteristics, derating, in most cases, is inappropriate. The level I, II, and III derating breakdown does not apply because of the operative nature of these devices (passive) and their low population in systems. There has also been no information received from industry to support derating levels for SAW devices.

The frequency stability demonstrated by the SAW device is a design requirement which can cause part degradation if it is not controlled. Life tests that have been conducted on SAW filters suggest that the best frequency stability exhibited by these devices is at low power, while maintaining constant temperature range. The results of the tests with input power of 13 dBs and 18 dBs and a center frequency of 500 megahertz are illustrated in the plot of frequency change versus time of Figures 37 and 38. Figure 38 (18 dBs) shows that frequency stability is forfeited at increased input power. The power ratio of the 18 dB samples is three times that of the 13 dB samples. This situation creates an effect on aging which is four times greater. It can be concluded that minimum aging and increased frequency stability occur at low input power. Therefore, input power is the primary derating factor for SAW devices.

The temperature dependence of SAW devices is driven by the substrate material. Each substrate material has an associated temperature coefficient (see Table 12) which determines how the frequency of the device changes with each degree change in temperature. The frequency stability is determined by the temperature coefficient of the substrate specified as a design consideration. Since SAW devices are low heat generators, their environment determines the operating temperature. The devices surrounding the SAW

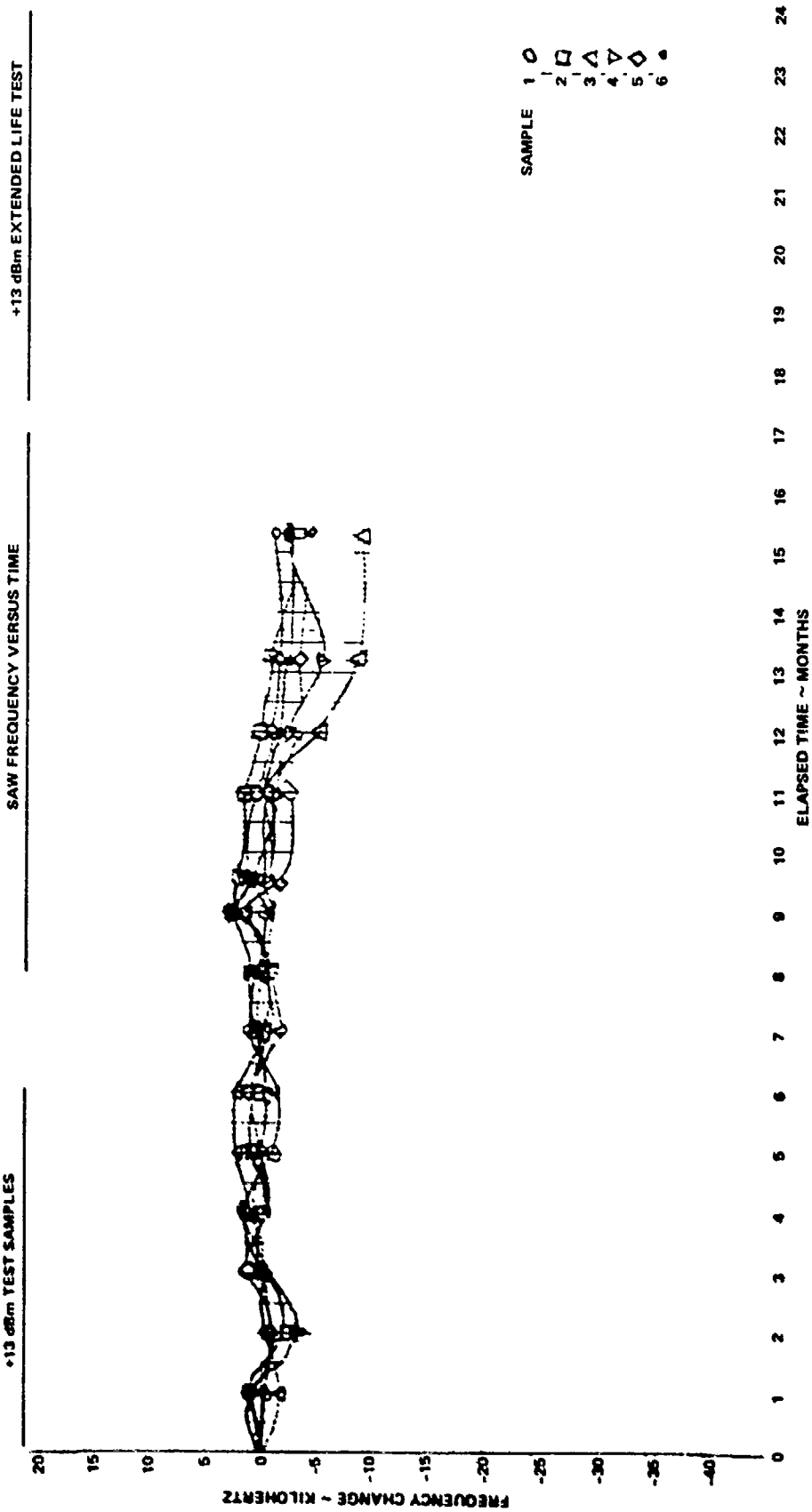


Figure 37. SAW Frequency versus Time

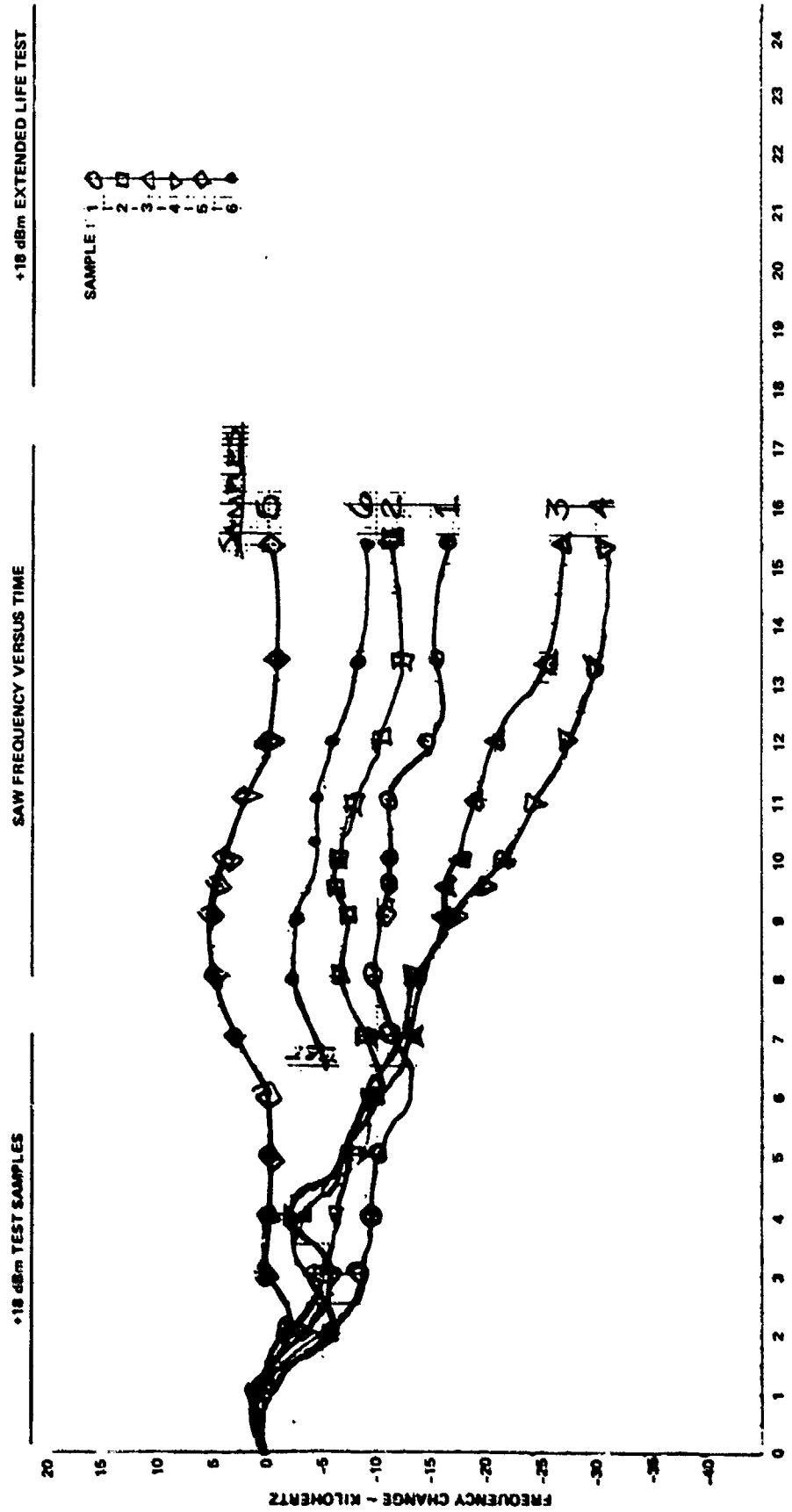


Figure 38. SAW Frequency versus Time

device are a major concern because of their heat potential. With such an environment, industry indicates that the SAW operating temperature is not to exceed 125°C.

Industry has determined through work with SAW devices that they are not particularly sensitive to shock and vibration. However, SAWs are somewhat sensitive to electro-static discharge. Design attention is required to minimize this stress.

Based on this discussion, the derating criteria for SAW devices outlined in Table 10, section 2.6, was selected.

4.0 FAILURE MODES/MECHANISMS

4.1 General

Failure modes are a primary concern of reliability when considering semiconductors and their failure rate. The origin of failure modes can occur at many different points. The failure mode can be a result of inherent design weaknesses (actual or potential), a manufacturing process, materials used, or human error.

Generally, failure modes are initially identified through accumulated experience or device physics analysis. Some failure modes can be eliminated or controlled, while others are inherent in a particular device type. The modes which can be eliminated or controlled are related somewhat in the quality levels discussed in section 3.1.

The controlled modes can be translated to concerns in the overall semiconductor, the die fabrication process, and the assembly process. Figures 39 through 41 show the major reliability concern in each area, respectively. The control method or constraint for the concern is also shown. Some of the concerns can only be controlled at the semiconductor manufacturer's facility, while others can be controlled at the contractor's facility or an independent testing laboratory. Figure 40 shows an example of a semiconductor manufacturer control using internal visual inspection. Such inspection controls such modes as glassivation, metalization, and bonding pads. Electrical performance in which the control can take the form of burn-in, baselining, or rescreening is an example of contractor's facility control modes.

4.2 Application Guidelines

Specific failure mode information is not readily available for the components under investigation, due to their recent entry into the market. The Martin Marietta survey (Appendix 3) revealed some failure mode data with associated failure mechanisms.

VLSI and VHSIC devices are relatively new technologies. The failure mechanism list is tentative in nature, since much of what needs to be known will not be discovered until development is further along. The VLSI and VHSIC devices, along with hybrids, have typically exhibited failures in the form of shorts, opens, leakage, and latch-up. According to sources at Martin Marietta, the mechanisms associated with these failures are primarily due to manufacturer's techniques and design applications. Both of these mechanisms are controllable. Inadequate manufacturing techniques have resulted in insufficient substrate contacts, lack of guard bars, and lack of protection at the input/output point. The designer should implement safeguards into his design and create a system that would be tolerant to such failures. The application of the design should also be specifically stated so as no discrepancies exist.

Since these devices represent a new technology still in a development phase, failure mode/mechanism data has not been completely established. However, many of the possible areas of concern can be identified through

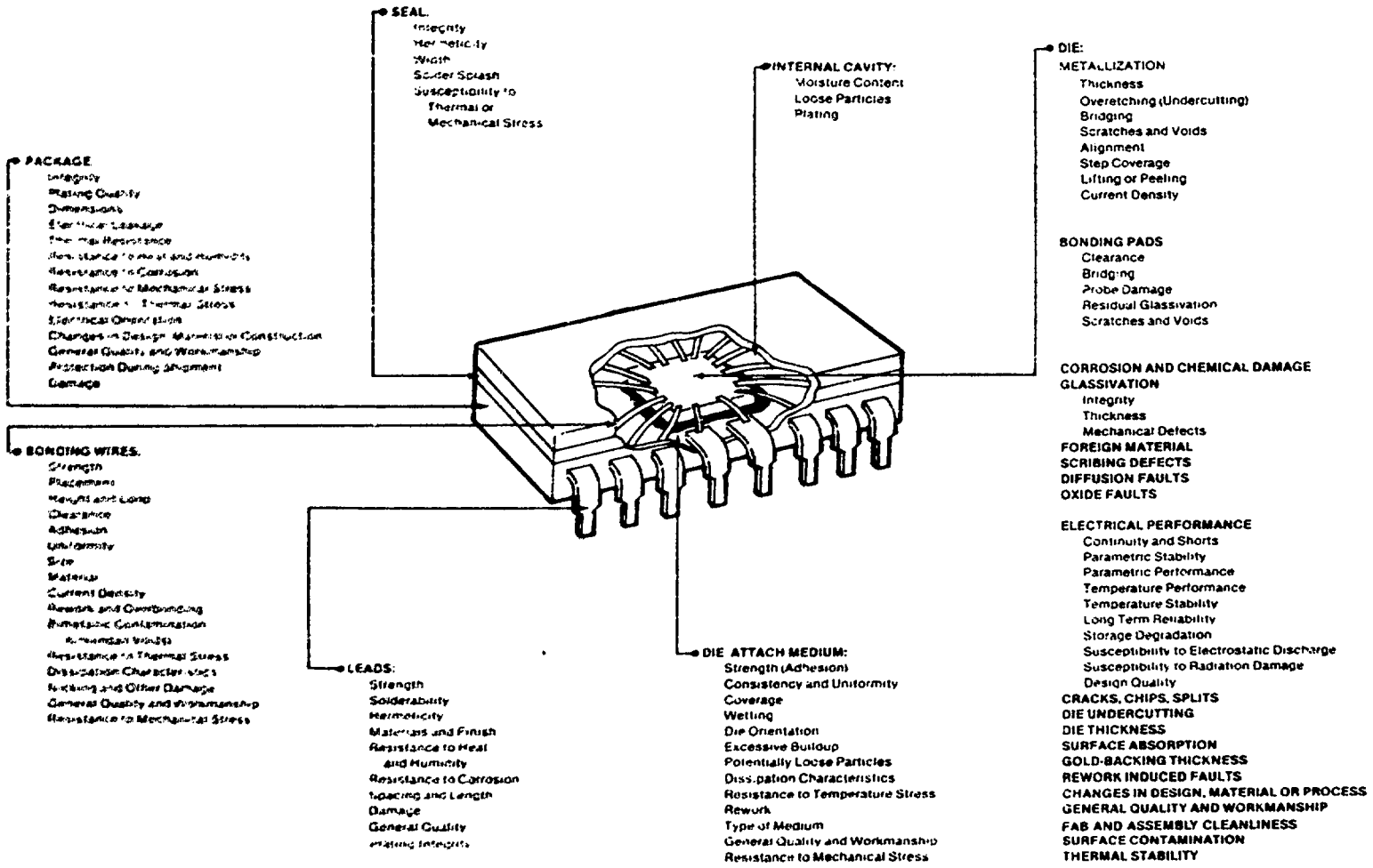


Figure 39. The Primary Concerns of Semiconductor Reliability

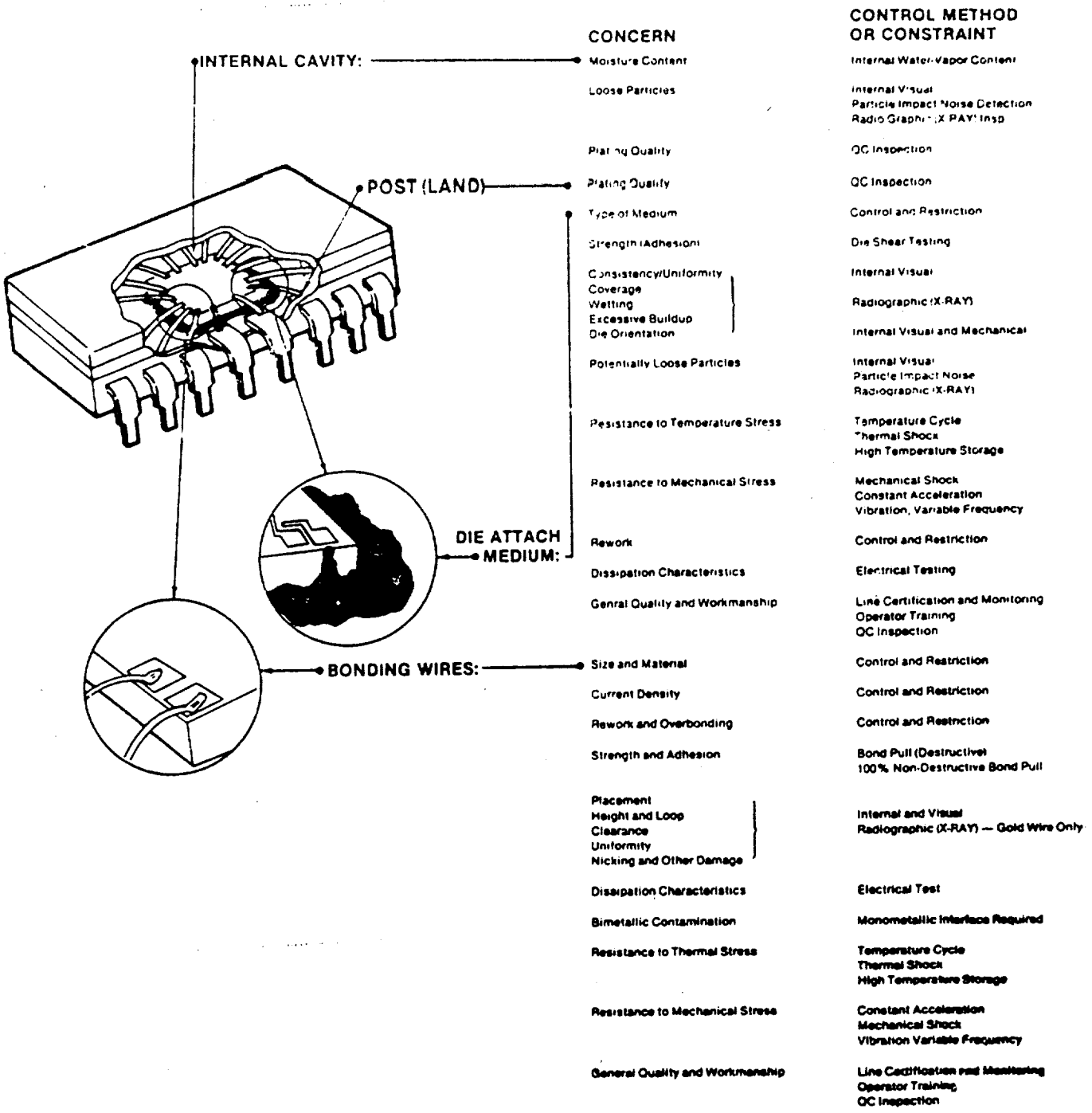


Figure 40. Reliability Concerns: The Die Fabrication Process

the extrapolation from what is known regarding existing technologies. Other areas have been highlighted in the course of analysis over the last few years. It is possible to focus upon several specific portions of the manufacturing process to the extent that process changes might impact reliability, some physical parameters (such as threshold voltage and surface mobility) that affect various failure mechanisms, and such specific failure mechanisms as radiation sensitivity and multiple layer interconnects.

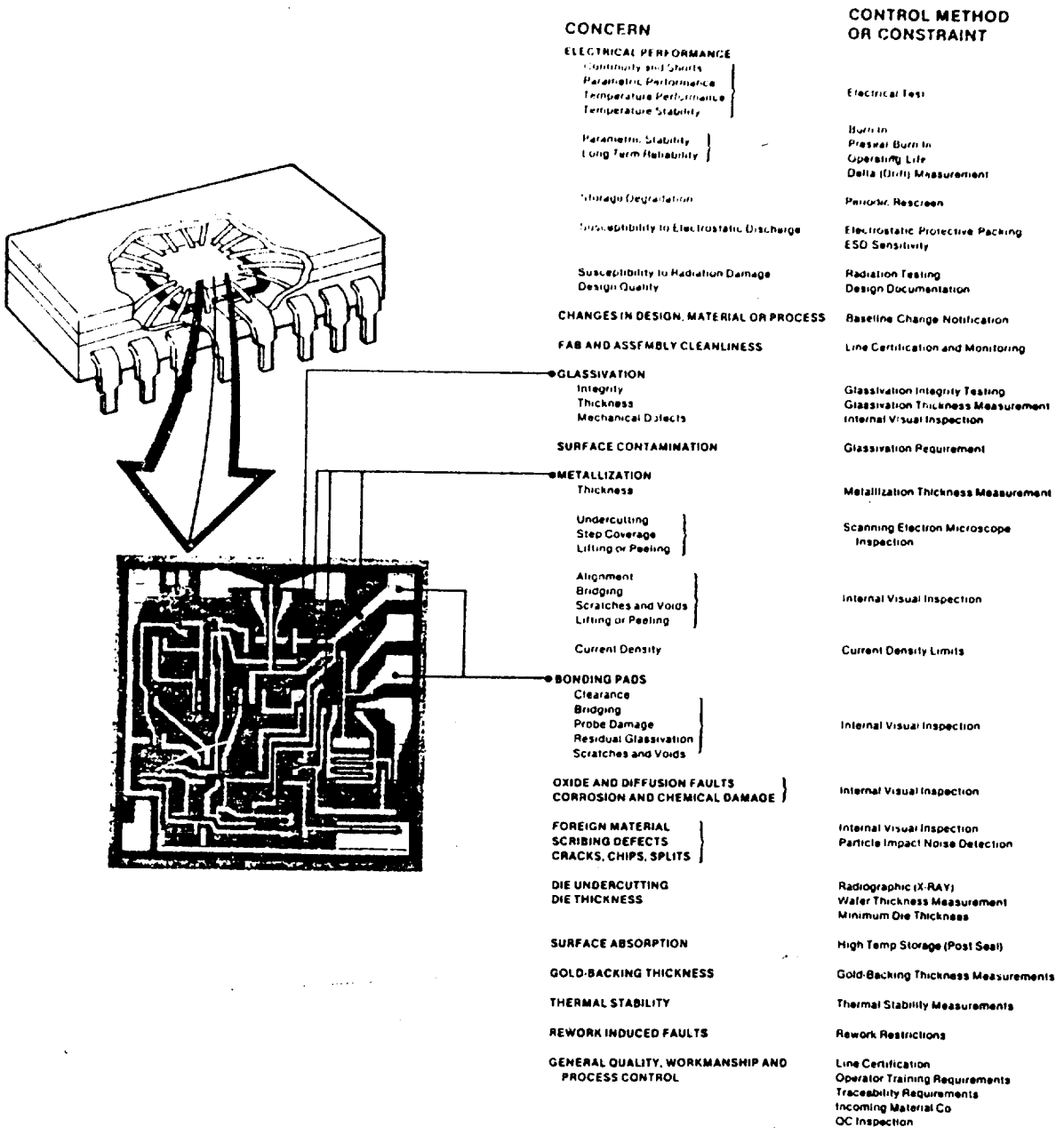


Figure 41. Reliability Concerns: The Assembly Process

The main causes of failure of microelectronic parts, as stated by P.D.T. O'Connor in his paper "Microelectronic System Reliability Prediction," are summarized in Table 12b with typical percentage contributions. These percentage contributions can vary, based on technology, production techniques, quality control, screening methods, circuit design, system maturity, maintenance, and use. However, they do represent "typical" percentage points. An additional failure mode not covered in the table is an out-of-spec overload condition which refers to failures not due to part properties but due to system design.

TABLE 12b. FAILURE MODES OF MICROELECTRONIC DEVICES

Failure Mode	Typical Failure Percent
Bulk Silicon, Surface Related	50
Foreign Materials/Particles	5
Bonds	25
Hermeticity	10
Other	10

As shown in Table 12b, the major causes of microelectronic part failure (applicable also to LSI devices) are usually defects introduced during the wafer fabrication process. Failures due to this type of defect can occur when cross-sectional areas are reduced to the extent that physical processes such as electromigration or localized overheating can change the part characteristics within the operating lifetime. Normally, geometrics are such that these processes would not affect electrical characteristics in the typical lifetime of a good part. However, imperfections due to nonuniformity of diffusion, oxidation or metalization, crystal flows, etc., can lead to reduced cross-sections in parts which otherwise pass initial visual, electrical, and burn-in tests. Subsequent deterioration due to these processes can then result in failure. The probability of the existence of failure-inducing imperfections is likely to be higher with increasing complexity and packing density, other things being equal. However, this aspect tends to be offset by improvements in fabrication technology.

The other two main internal failure modes shown in Table 12b, bond failure and hermeticity, are package related and time dependent. Temperature is unlikely to be the prime failure factor in a purely mechanical process, such as some bond failures, but is a factor intermetallic processes. Temperature effects also affect the time to failure caused by a leaky package. The relationship between temperature and time is unlikely to be simple, since temperature cycling and the nature of impurities introduced are likely to dominate.

Package related failure modes are not as highly correlated with chip complexity as are failures due to chip imperfections. The rate of occurrence depends upon quality control during part fabrication and test.

Microwave devices suffer from yet another set of failure modes. According to the article, "Reliability Life Tests on an Encapsulated Millimeter Wave DDR IMPATT Diode," the primary failure mode appearing in their accelerated life test was a junction short. Such shorts are caused by gold in the ohmic metalization diffusing into the silicon layer through the platinum barrier. This diffusion creates a current path. According to Martin Marietta sources, the diffusion is commonly referred to as migration. It is typically a result of inadequate design application related to

temperature stresses. Hermeticity problems in microwave devices have also emerged due to design applications.

Microwave devices are another relatively new technology with limited information available on typical failure modes. To gain insight into possible failure modes, it would be beneficial to examine data on diodes in general.

The diode will generally fail either open or short. The following information taken from the Martin Marietta book, Reliability for the Engineer (Book 7), is a summary of the percentage of the time that the general purpose germanium, silicon, and surge limiting/logic diode will fail either open or short. The short percent of failures for the germanium diodes is 65 percent, for the silicon diodes is 65 percent, and for the surge limiting/logic diodes is 45 percent. The open percent of failures for the germanium diodes is 35 percent, for the silicon diodes is 35 percent, and for the surge limiting/logic diodes is 55 percent.

Table 13 shows the most common causes of PIN diode failures and design features used to eliminate these failures, as reported by Unitrode in their book PIN Diode Designer's Handbook and Catalog. This information can be directly used by designers of microwave devices (diodes in general) to possibly prevent these failures from occurring.

Failure mode data was not available for memory devices. However, some design considerations were pinpointed in a memory applications handbook for memory subsystems. These designs will maximize RAM board yields during manufacturing.

Some memory board designs are easy to manufacture. Others, while functionally identical, have low manufacturing yields due to many bad chips. The difference between the two is usually the amount of margin designed into the system. Power supply and timing margins are both critical.

As margins go up to zero or negative, the amount of soft errors increases. Soft errors are those that occur intermittently. Soft errors usually occur during a memory cycle where some system parameter has gone out of specification. The solution to soft errors is a careful system design and board layout.

There are three things the system designer can do to maximize RAM board yield during manufacturing:

1 Design proper power supply decoupling

2 Design as much margin as possible in all control signal timing

3 Never allow spurious, shortened memory cycles to occur.

These suggestions are applicable to a design with tolerance for faults built in.

TABLE 13. COMMON DIODE FAILURES WITH DESIGN FEATURES TO ELIMINATE FAILURES

Diode Failures	Design Features
Whisker or ribbon-to-post connection failure. Whiskers or ribbon-to-die bond failure. Broken whiskers or ribbon. Insufficient whisker pressure.	No whisker, ribbons, or posts necessary. *Terminal pins are bonded to the die at approximately 1000°C.*
Mechanical failure of the die bond.	A uniform, true metallurgical bond takes place along both sides of the die. A fused glass seal extending beyond both sides of the die-to-pin bond gives added strength.
Lead fatigue.	Lead brazed directly to pin. Lead does not extend into the glass-to-metal seal; hence, no glass edge to cut into the lead. Lead bonding does not stress glass seal. Statistical quality-control sampling is performed to assure uniformity of braze.
Impurities in protective coating, movement and change in characteristics of coating (such as hardening or cracking), pin holes in coating.	*Glass is one of the most stable materials known.* A thick glass seal fused directly to the silicon surface eliminates the need for other protective coating.
Incomplete weld resulting in imperfect seal.	No weld is used for hermetic seal. Glass sleeve is remelted and fused around the silicon die to permanently seal and passivate the surface.
Lack of hermeticity in plastic devices.	Fused-in-glass construction.
Corrosion of diode components.	All components are inherently corrosion resistant Material content is verified by certifications and by regular independent laboratory analyses.
Instability of paint used for light shields.	All paint cured during bakeout at 200°C.
Mismatch of thermal coefficient of expansion resulting in thermal fatigue failures.	Terminal pins, silicon and glass seal are matched for temperature coefficient of expansion. Material content verified by certifications and regular independent laboratory analyses.
Melting of eutectic compounds at temperatures that exceed diode ratings.	*Lowest melting combinations of elements is 200°C above maximum rated temperatures.*
Entrapped flakes of copper oxide, silver paste and gold, plus glass chips or other conductive or non-conductive particles.	No copper, silver paste, or gold used in device. In addition, there is absolutely no void in which particles may become entrapped. The metallurgical bond between die faces and both the terminal pins and overall fused glass seal make *Unitrode diodes void free.*
Weld splash residue contaminates junction.	No welding performed inside hermetic glass seal.
Voltage-activated ionic and molecular migrations, including electromigration of contact metals.	Migrations are restricted by virtue of the glass adhering directly to the silicon. Power-stress screening eliminates the remaining extremely small percentages of devices in which such changes occur.

5.0 TEMPERATURE MODELING AND VERIFICATION

5.1 Objective

The need has been established for a method of verifying the junction temperature of a device to ensure that derating has been implemented. Since the junction temperature of a device cannot be measured directly, a point on the case where easy access for measurement can be obtained had to be identified. The objective was to find a practical, reliable, and easy to use method of establishing the derated junction temperature from the thermally related case temperature (measurement point).

5.2 Approach

To accomplish the objective, analytical thermal models were developed and verified that generate a practical method of computing or graphically determining the derated temperatures. Two specific types of models were developed and verified with test data for this purpose. The first model was an internal thermal model approximating the thermal resistance from the chip junction to the case bottom (θ_{JC}). This model was predominately used for new designs as a ball park predictor, or quick look method of deriving an initial thermal resistance (θ_{JC}). The second was an external thermal model designed for specific package types to relate the measured case temperature with the junction temperature. This model was used for already existing devices that are housed in one of six package types. Both of these models can be modified for the specific applications of the user. The computer programs for the internal model, and the conduction calculations for the external model, are provided in appendices 5 and 6 respectively, so that modifications can be made to model specific designs and assumptions.

Test measurements were performed on a 40-pin, side-brazed ceramic package. Measurement data was acquired on the ceramic chip carrier package for the purpose of verifying two of the external models. Since a high correlation between the models and the measurement data was obtained, it was assumed that the models for the other package types were accurate. All models were based on the same assumptions and ground rules.

Upon verification, the external models were used to provide a graphic representation of the relationship between the junction temperature and the identified measurement point for each of the package types, based on specified assumptions. The implementation of derating was determined. In the internal model, thermal resistance tables were generated for each level of device construction. These tables were used in the computation of the thermal resistance from the chip junction to the case bottom (θ_{JC}). This established the ball park prediction of θ_{JC} for new designs.

As in the case of the external model, the thermal resistance tables produced by the internal model were based on certain assumptions. Each of these models (internal and external) will be addressed in the following sections, along with their assumptions, specific applications, and results.

5.3 Internal Model

Discrete devices can be modeled using approximations for heat spreading effects at each level of construction. These models are particularly useful for devices of new design when a ball park prediction of θ_{JC} is required. Computer programs that model the internal thermal characteristics of these discrete devices were developed for square, rectangular, and circular surfaces. These models are dependent on critical assumptions, and are operable over specific parameters, in order for them to be useful to the average device user who is not familiar with the internal construction of the device. The assumptions and parameters incorporated in these programs are:

1. 50-percent thermal dissipation area (100 percent for circular surfaces)
2. 100-percent attachment coverage
3. Specified material conductivity
4. Surface shape
5. Spreading angle at each level of construction (variable input)
6. Thickness variability as chip dimensions vary at chip level.

The impact of the other thermal parameters such as cooling, internal radiation, and secondary flow paths are discussed in the external model (Section 5.4) since the thermal resistance calculated by the internal model is independent of these parameters.

The applicability of these programs is dependent upon the user knowing the material of each level of the device; the material conductivity (section 5.4, Table 30); and the spreading angle (appendix 5.4). The programs are written so that the computer will cue the user when specific inputs are required. For example, at the chip level, the program asks for the chip material, the material conductivity, and the desired spreading angle. At the attachment level, the program first provides the user with a list of attachment materials and then asks for the choice to be entered. The material conductivity and the spreading angle are then requested. The internal heat spreading angle has a significant impact on thermal resistance, from the chip junction to the case bottom (θ_{JC}). The internal model employs the spreading angle in the computation of the thermal resistance at each level of device construction by allowing the model user to specify the angle desired. There are many variables, such as attachment voids, chip size, dissipation area, material type, and thickness, all which affect the heat spreading function. This creates difficulty in specifying one angle that typically represents the heat spread. Based on analysis (Appendix 5.4), it was concluded that the correct spreading angle could not be determined. The spreading function is an important factor that needs consideration when developing models. However, further investigation was not possible, due to program limitations. All the programs follow the same user-friendly format.

The programs, which are presented in appendix 5, allow for the modification of these terms and others so that more specific cases can be instituted. They are written in the BASIC programming language and are well documented with comments and section headings so that modifications can be accomplished.

The programs that model the previously mentioned surface types consider the heat flow at each level of construction beginning with the chip (device) itself. The thermal dissipation area is accounted for at this level, with the thermal resistance being computed for these dimensions. The next level dimensions are calculated, based on the thickness of the device and the desired spreading angle. The calculation is represented by the following equation for the square and rectangular surfaces. The next level dimension calculation for circular devices is discussed in the respective section.

$$L2 = L+2*T*TAN(A)$$

where

L2 = new length
L = present length
T = thickness of present level
A = spreading angle.

Units are in mils.

It should be noted that if the spread exceeds the dimensions of that level of construction, then the point at which the spread touches the edge becomes the dimensions for the next level.

The programs for the other levels follow the same format, with the variable values changing in order to account for the varying materials, spreading, and dimensions. The attachment materials and the intermediate materials have both been limited to the ones most widely used in industry. However, this can be modified to incorporate any material used. The attachment materials assumed are eutectics, silver, gold, and nonconductive epoxies. The intermediate materials assumed are a gold header, beryllia, alumina, molytab, and nickeltab.

The result of the program's computation is a table comprised of thermal resistance values for a variety of dimensions. By adding the thermal resistance values for each level of construction, a thermal resistance value from the junction to the case can be calculated. The resulting tables for each device level of the three different surface types are presented in their respective sections which immediately follow. The tables have all been generated assuming a 45-degree spreading angle. For a more detailed analysis of the spreading angle, see appendix 5.4.

5.3.1 Square Model

LSI and VLSI devices are frequently square or nearly square. Since the package features of these devices may also have a square format, such as hermetic chip carriers, a square model is attractive. The programs

that model the square devices employ the following equation for the computation of the thermal resistance at each level of the device construction:

$$R1 = T/(K*W*(W+2*T*TAN(A)))$$

where

R1 = thermal resistance (°C per watt)
T = thickness (mils)
W = width (mils)
K = material conductivity (watts per inch °C)
A = spreading angle (degrees).

The value for K must be divided by 1000 in order to have agreement among measurement units.

Calculations have been performed for typical materials in the primary heat flow path using various spreading angles. As expected, the thermal resistance (θ_{JC}) increases as the spreading angle decreases, with the greatest impact occurring at the outermost packaging level. An increased area is inversely proportional to the calculated thermal resistance. Similar comparisons can also be made to estimate the effects of chip hot spots and voids in the chip attachment which concentrate the thermal flow.

A sample calculation shown in Table 14 illustrates the use of the tables generated by the square model. This particular example has four levels of construction and assumes a 45-degree spread. Using Tables 15 through 18, the values for the thermal resistance and the next level dimensions can be obtained for all the levels of construction. The dimensions used to enter the tables subsequent to the device level are calculated in the previous level's table and carried over. Interpolation may be required. The thermal resistance values for each level are then summed and multiplied by the power dissipated to obtain the junction to case temperature change.

TABLE 14. SQUARE DEVICE SAMPLE CALCULATION

Device: Square Surface Material: Silicon Conductivity: 2.13 watts per inch-degrees centigrade Thickness: 12 mils	Header: Material: Gold Conductivity: 7.54 watts per inch - degrees centigrade Thickness: 0.2 mils
Attachment: Material: Eutectic Conductivity: 4.5 watts per inch-degrees centigrade) Thickness: 0.5 mils	Package: Material: Alumina Conductivity: 0.478 watts per inch - degrees centigrade Thickness: 46 mils
50 Percent Dissipation 45 degrees Spreading	P_D = 1.6125 Watts

Level	Length Times Width (in inches)	Thermal Resistance (degrees centigrade (per watt)	Length(*) Times Width(*) (inches)
Device	250 x 250	0.22473	212.75 x 212.75
Attachment	212.75 x 212.75	0.00253	213.6 x 213.6
Header	213.6 x 213.6	0.00060	213.94 x 213.94
Package	213.94 x 213.94	1.33113	
θ_{JC} = 1.60 degrees centigrade per watt			
$\Delta T_{JC} = \theta_{JC} P_D$ = 2.58°C			

TABLE 15. SQUARE SURFACE DEVICE - 50% DISSIPATION

MATERIAL: SILICON
CONDUCTIVITY: 2.13 (W/IN.*C)
SPREADING ANGLE: 45 DEGREES

LENGTH * WIDTH	THERMAL RESISTANCE	Linc * Winc
2 X 2	148.51285	2.00 X 2.00
4 X 4	67.17533	4.00 X 4.00
6 X 6	40.88483	6.00 X 6.00
8 X 8	28.20787	8.00 X 8.00
10 X 10	23.02732	10.00 X 10.00
15 X 15	13.31180	15.00 X 15.00
20 X 20	8.81288	20.00 X 20.00
25 X 25	7.64834	25.00 X 25.00
30 X 30	5.87526	30.00 X 30.00
35 X 35	4.67073	35.00 X 35.00
40 X 40	3.81055	40.00 X 40.00
45 X 45	3.17263	45.00 X 45.00
50 X 50	3.04843	50.00 X 50.00
60 X 60	2.29236	60.00 X 60.00
70 X 70	1.79013	70.00 X 70.00
80 X 80	1.43842	80.00 X 80.00
90 X 90	1.18205	90.00 X 90.00
100 X 100	1.12024	100.00 X 100.00
110 X 110	0.95512	110.00 X 110.00
120 X 120	0.82430	120.00 X 120.00
130 X 130	0.71884	127.91 X 127.91
140 X 140	0.63253	134.98 X 134.98
150 X 150	0.56098	142.05 X 142.05
160 X 160	0.50098	149.12 X 149.12
170 X 170	0.45017	156.19 X 156.19
180 X 180	0.40675	163.26 X 163.26
190 X 190	0.36935	170.33 X 170.33
200 X 200	0.33689	177.40 X 177.40
250 X 250	0.22473	212.75 X 212.75
300 X 300	0.16059	248.10 X 248.10
350 X 350	0.12049	283.45 X 283.45
400 X 400	0.09373	318.80 X 318.80
450 X 450	0.07500	354.15 X 354.15
500 X 500	0.06138	389.50 X 389.50

TABLE 16. SQUARE SURFACE ATTACHMENT

MATERIAL: EUTECTIC
CONDUCTIVITY: 4.5 (W/IN.*C)
SPREADING ANGLE: 45 (DEGREES)

LENGTH * WIDTH	THERMAL RESISTANCE	Linc * Winc
2 X 2	18.51852	2.00 X 2.00
4 X 4	5.55556	4.00 X 4.00
6 X 6	2.64551	6.00 X 6.00
8 X 8	1.54321	8.00 X 8.00
10 X 10	1.01010	10.00 X 10.00
15 X 15	0.46297	15.00 X 15.00
20 X 20	0.26455	20.00 X 20.00
25 X 25	0.17094	25.00 X 25.00
30 X 30	0.11948	30.00 X 30.00
35 X 35	0.08818	35.00 X 35.00
40 X 40	0.06775	40.00 X 40.00
45 X 45	0.05368	45.00 X 45.00
50 X 50	0.04357	50.00 X 50.00
60 X 60	0.03036	60.00 X 60.00
70 X 70	0.02236	70.00 X 70.00
80 X 80	0.01715	80.00 X 80.00
90 X 90	0.01357	90.00 X 90.00
100 X 100	0.01100	100.00 X 100.00
110 X 110	0.00910	110.00 X 110.00
120 X 120	0.00765	120.00 X 120.00
130 X 130	0.00652	131.00 X 131.00
140 X 140	0.00563	141.00 X 141.00
150 X 150	0.00491	151.00 X 151.00
160 X 160	0.00431	161.00 X 161.00
170 X 170	0.00382	171.00 X 171.00
180 X 180	0.00341	181.00 X 181.00
190 X 190	0.00306	191.00 X 191.00
200 X 200	0.00276	201.00 X 201.00
250 X 250	0.00177	251.00 X 251.00
300 X 300	0.00123	301.00 X 301.00
350 X 350	0.00090	351.00 X 351.00
400 X 400	0.00069	401.00 X 401.00
450 X 450	0.00055	451.00 X 451.00
500 X 500	0.00044	501.00 X 501.00

TABLE 17. SQUARE SURFACE - INTERMEDIATE MATERIAL

MATERIAL: GOLD HEADER
CONDUCTIVITY: 7.54 (W/IN.*C)
SPREADING ANGLE: 45 (DEGREES)

LENGTH * WIDTH	THERMAL RESISTANCE	Linc * Winc
2 X 2	5.52609	2.40 X 2.40
4 X 4	1.50712	4.40 X 4.40
6 X 6	0.69077	6.40 X 6.40
8 X 8	0.39472	8.40 X 8.40
10 X 10	0.25505	10.40 X 10.40
15 X 15	0.11483	15.40 X 15.40
20 X 20	0.06501	20.40 X 20.40
25 X 25	0.04177	25.40 X 25.40
30 X 30	0.02908	30.40 X 30.40
35 X 35	0.02141	35.40 X 35.40
40 X 40	0.01641	40.40 X 40.40
45 X 45	0.01298	45.40 X 45.40
50 X 50	0.01053	50.40 X 50.40
60 X 60	0.00732	60.40 X 60.40
70 X 70	0.00538	70.40 X 70.40
80 X 80	0.00412	80.40 X 80.40
90 X 90	0.00326	90.40 X 90.40
100 X 100	0.00264	100.40 X 100.40
110 X 110	0.00218	110.40 X 110.40
120 X 120	0.00184	120.40 X 120.40
130 X 130	0.00156	130.40 X 130.40
140 X 140	0.00135	140.40 X 140.40
150 X 150	0.00118	150.40 X 150.40
160 X 160	0.00103	160.40 X 160.40
170 X 170	0.00092	170.40 X 170.40
180 X 180	0.00082	180.40 X 180.40
190 X 190	0.00073	190.40 X 190.40
200 X 200	0.00066	200.40 X 200.40
250 X 250	0.00042	250.40 X 250.40
300 X 300	0.00029	300.40 X 300.40
350 X 350	0.00022	350.40 X 350.40
400 X 400	0.00017	400.40 X 400.40
450 X 450	0.00013	450.40 X 450.40
500 X 500	0.00011	500.40 X 500.40

TABLE 18. 40-PIN CERAMIC SIDE BRAZED PACKAGE

MATERIAL: ALUMINA
CONDUCTIVITY: .478 (W/IN.*C)
SPREADING ANGLE: 45 (DEGREES)
ATTACHMENT MATERIAL: EUTECTIC
INTERMEDIATE MATERIAL: GOLD HEADER

LENGTH * WIDTH	THERMAL RESISTANCE	Linc * Winc
2 X 2	513.14441	106.00 X 106.00
4 X 4	251.82081	108.00 X 108.00
6 X 6	164.82819	110.00 X 110.00
8 X 8	121.41362	112.00 X 112.00
10 X 10	94.91708	108.00 X 108.00
15 X 15	60.47814	113.00 X 113.00
20 X 20	42.96175	112.00 X 112.00
25 X 25	32.90063	117.00 X 117.00
30 X 30	26.29352	122.00 X 122.00
35 X 35	21.65001	127.00 X 127.00
40 X 40	17.71495	124.00 X 124.00
45 X 45	15.13628	129.00 X 129.00
50 X 50	13.11434	134.00 X 134.00
60 X 60	10.16969	144.00 X 144.00
70 X 70	8.15084	154.00 X 154.00
80 X 80	6.53766	160.00 X 160.00
90 X 90	5.46942	170.00 X 170.00
100 X 100	4.64901	180.00 X 180.00
110 X 110	4.00392	190.00 X 190.00
120 X 120	3.48675	200.00 X 200.00
130 X 130	3.06528	210.00 X 210.00
140 X 140	2.71695	220.00 X 220.00
150 X 150	2.42557	230.00 X 230.00
160 X 160	2.17922	240.00 X 240.00
170 X 170	1.96900	250.00 X 250.00
180 X 180	1.78808	260.00 X 260.00
190 X 190	1.63123	270.00 X 270.00
200 X 200	1.49433	280.00 X 280.00
250 X 250	1.01433	330.00 X 330.00
300 X 300	0.73406	380.00 X 380.00
350 X 350	0.55603	430.00 X 430.00
400 X 400	0.43585	480.00 X 480.00
450 X 450	0.35087	530.00 X 530.00
500 X 500	0.28856	580.00 X 580.00

5.3.2 Rectangular Model

The rectangular model is particularly applicable to chips which have concentrated power dissipation, such as output drivers along one side in a rectangular region, as well as chips with high aspect ratios. The following equation is used to model the thermal resistance of devices of this type:

$$R = \frac{1}{(L-W)\ (2\ K\ TAN(A))} \cdot \ln\left(\frac{L}{W}\ \frac{2\ T\ TAN(A) + W}{2\ T\ TAN(A) + L}\right)$$

where

R = thermal resistance (°C per watt)
L = length (mils)
W = width (mils)
K = material conductivity (watts per inch °C)
T = thickness (mils)
A = spreading angle (degrees).

The value for K must be divided by 1000 in order to have agreement among the units of measurement.

The rectangular model is very similar to the square model, except square dimensions cannot be modeled by the rectangular programs. If square dimensions were applied to the thermal resistance equation above, the result would be division by zero. However, using the concept of limits, dimensions up to the perfect square can be modeled correctly by the rectangular programs.

A sample calculation that employs Tables 19 through 22 is illustrated in Table 23. The steps involved in this calculation are identical to those in the square model. It should be noted that the shape or behavior of the chip determines which model to use and which tables to employ. Using values from both the square and rectangular tables interchangeably can result in erroneous answers.

TABLE 19. RECTANGULAR SURFACE DEVICE - 50% DISSIPATION

MATERIAL: SILICON
CONDUCTIVITY: 2.13 (W/IN.*C)
SPREADING ANGLE: 45 (DEGREES)

LENGTH * WIDTH	THERMAL RESISTANCE	Linc * Winc
2 X 4	98.43361	2.00 X 4.00
2 X 6	75.31256	2.00 X 6.00
4 X 6	52.19135	4.00 X 6.00
4 X 8	43.04614	4.00 X 8.00
4 X 10	36.78247	4.00 X 10.00
4 X 12	32.18511	4.00 X 12.00

TABLE 19. (CONTINUED)

6	X	8	33.90086	6.00	X	8.00
6	X	10	29.07790	6.00	X	10.00
6	X	12	25.51632	6.00	X	12.00
6	X	14	22.76464	6.00	X	14.00
6	X	16	20.56767	6.00	X	16.00
6	X	18	18.76930	6.00	X	18.00
8	X	10	24.25487	8.00	X	10.00
8	X	12	21.32400	8.00	X	12.00
8	X	14	19.05248	8.00	X	14.00
8	X	16	17.23435	8.00	X	16.00
8	X	18	15.74303	8.00	X	18.00
8	X	20	14.49566	8.00	X	20.00
8	X	22	13.43587	8.00	X	22.00
8	X	24	12.52351	8.00	X	24.00
10	X	15	17.45786	10.00	X	15.00
10	X	20	14.13854	10.00	X	20.00
10	X	25	11.91016	10.00	X	25.00
10	X	30	10.30220	10.00	X	30.00
15	X	20	10.81927	15.00	X	20.00
15	X	25	9.13631	15.00	X	25.00
15	X	30	7.91702	15.00	X	30.00
15	X	35	6.99019	15.00	X	35.00
15	X	40	6.26062	15.00	X	40.00
15	X	45	5.67069	15.00	X	45.00
20	X	25	7.45344	20.00	X	25.00
20	X	30	6.46590	20.00	X	30.00
20	X	35	5.71385	20.00	X	35.00
20	X	40	5.12094	20.00	X	40.00
20	X	45	4.64097	20.00	X	45.00
20	X	50	4.24416	20.00	X	50.00
20	X	55	3.91045	20.00	X	54.89
20	X	60	3.62578	20.00	X	58.42
25	X	30	6.70063	25.00	X	30.00
25	X	35	5.96889	25.00	X	35.00
25	X	40	5.38526	25.00	X	40.00
25	X	45	4.90808	25.00	X	45.00
25	X	50	4.51019	25.00	X	50.00
25	X	55	4.17302	25.00	X	55.00
25	X	60	3.88349	25.00	X	60.00
25	X	65	3.63204	25.00	X	65.00
25	X	70	3.41155	25.00	X	70.00
25	X	75	3.21656	25.00	X	75.00
30	X	35	5.23710	30.00	X	35.00
30	X	40	4.72759	30.00	X	40.00
30	X	45	4.31059	30.00	X	45.00
30	X	50	3.96260	30.00	X	50.00
30	X	55	3.66751	30.00	X	55.00
30	X	60	3.41396	30.00	X	60.00
30	X	65	3.19367	30.00	X	65.00
30	X	70	3.00041	30.00	X	70.00
30	X	75	2.82945	30.00	X	75.00

TABLE 19. (CONTINUED)

30	X	80	2.67709	30.00	X	80.00
30	X	85	2.54045	30.00	X	84.10
30	X	90	2.41719	30.00	X	87.63
35	X	40	4.21806	35.00	X	40.00
35	X	45	3.84734	35.00	X	45.00
35	X	50	3.53776	35.00	X	50.00
35	X	55	3.27510	35.00	X	55.00
35	X	60	3.04934	35.00	X	60.00
35	X	65	2.85310	35.00	X	65.00
35	X	70	2.68088	35.00	X	70.00
35	X	75	2.52848	35.00	X	75.00
35	X	80	2.39264	35.00	X	80.00
35	X	85	2.27078	35.00	X	84.10
35	X	90	2.16083	35.00	X	87.63
35	X	95	2.06110	35.00	X	91.17
35	X	100	1.97025	35.00	X	94.70
35	X	105	1.88711	35.00	X	98.24
40	X	45	3.47660	40.00	X	45.00
40	X	50	3.19759	40.00	X	50.00
40	X	55	2.96080	40.00	X	55.00
40	X	60	2.75716	40.00	X	60.00
40	X	65	2.58011	40.00	X	65.00
40	X	70	2.42468	40.00	X	70.00
40	X	75	2.28711	40.00	X	75.00
40	X	80	2.16446	40.00	X	80.00
40	X	85	2.05442	40.00	X	84.10
40	X	90	1.95511	40.00	X	87.63
40	X	95	1.86502	40.00	X	91.17
40	X	100	1.78293	40.00	X	94.70
40	X	105	1.70780	40.00	X	98.24
40	X	110	1.63879	40.00	X	101.77
40	X	115	1.57516	40.00	X	105.31
40	X	120	1.51631	40.00	X	108.84
45	X	50	2.91856	45.00	X	50.00
45	X	55	2.70289	45.00	X	55.00
45	X	60	2.51735	45.00	X	60.00
45	X	65	2.35598	45.00	X	65.00
45	X	70	2.21430	45.00	X	70.00
45	X	75	2.08887	45.00	X	75.00
45	X	80	1.97703	45.00	X	80.00
45	X	85	1.87665	45.00	X	84.10
45	X	90	1.78605	45.00	X	87.63
45	X	95	1.70387	45.00	X	91.17
45	X	100	1.62896	45.00	X	94.70
45	X	105	1.56040	45.00	X	98.24
45	X	110	1.49741	45.00	X	101.77
45	X	115	1.43934	45.00	X	105.31
45	X	120	1.38562	45.00	X	108.84
45	X	125	1.33579	45.00	X	112.38
45	X	130	1.28943	45.00	X	115.91
45	X	135	1.24620	45.00	X	119.44

TABLE 19. (CONTINUED)

50	X	60	2.64284	50.00	X	60.00
50	X	70	2.33412	50.00	X	70.00
50	X	80	2.09091	50.00	X	80.00
50	X	90	1.89416	50.00	X	90.00
50	X	100	1.73158	50.00	X	100.00
50	X	110	1.59492	50.00	X	107.77
50	X	120	1.47840	50.00	X	114.84
50	X	130	1.37785	50.00	X	121.91
50	X	140	1.29018	50.00	X	128.98
50	X	150	1.21305	50.00	X	136.05
60	X	70	2.02544	60.00	X	70.00
60	X	80	1.81497	60.00	X	80.00
60	X	90	1.64460	60.00	X	90.00
60	X	100	1.50377	60.00	X	100.00
60	X	110	1.38534	60.00	X	107.77
60	X	120	1.28433	60.00	X	114.84
60	X	130	1.19714	60.00	X	121.91
60	X	140	1.12110	60.00	X	128.98
60	X	150	1.05418	60.00	X	136.05
60	X	160	0.99485	60.00	X	143.12
60	X	170	0.94186	60.00	X	150.19
60	X	180	0.89425	60.00	X	157.26
70	X	80	1.60452	70.00	X	80.00
70	X	90	1.45419	70.00	X	90.00
70	X	100	1.32989	70.00	X	100.00
70	X	110	1.22532	70.00	X	107.77
70	X	120	1.13612	70.00	X	114.84
70	X	130	1.05909	70.00	X	121.91
70	X	140	0.99192	70.00	X	128.98
70	X	150	0.93279	70.00	X	136.05
70	X	160	0.88034	70.00	X	143.12
70	X	170	0.83350	70.00	X	150.19
70	X	180	0.79141	70.00	X	157.26
70	X	190	0.75338	70.00	X	164.33
70	X	200	0.71885	70.00	X	171.40
70	X	210	0.68735	70.00	X	178.47
80	X	90	1.30388	80.00	X	90.00
80	X	100	1.19258	80.00	X	100.00
80	X	110	1.09892	80.00	X	107.77
80	X	120	1.01902	80.00	X	114.84
80	X	130	0.95001	80.00	X	121.91
80	X	140	0.88981	80.00	X	128.98
80	X	150	0.83683	80.00	X	136.05
80	X	160	0.78982	80.00	X	143.12
80	X	170	0.74783	80.00	X	150.19
80	X	180	0.71010	80.00	X	157.26
80	X	190	0.67600	80.00	X	164.33
80	X	200	0.64504	80.00	X	171.40
80	X	210	0.61680	80.00	X	178.47
80	X	220	0.59093	80.00	X	185.54
80	X	230	0.56715	80.00	X	192.61
80	X	240	0.54522	80.00	X	199.68

TABLE 19. (CONTINUED)

90	X	100	1.08127	90.00	X	100.00
90	X	110	0.99645	90.00	X	107.77
90	X	120	0.92407	90.00	X	114.84
90	X	130	0.86155	90.00	X	121.91
90	X	140	0.80700	90.00	X	128.98
90	X	150	0.75899	90.00	X	136.05
90	X	160	0.71638	90.00	X	143.12
90	X	170	0.67833	90.00	X	150.19
90	X	180	0.64412	90.00	X	157.26
90	X	190	0.61322	90.00	X	164.33
90	X	200	0.58515	90.00	X	171.40
90	X	210	0.55955	90.00	X	178.47
90	X	220	0.53609	90.00	X	185.54
90	X	230	0.51453	90.00	X	192.61
90	X	240	0.49464	90.00	X	199.68
90	X	250	0.47624	90.00	X	206.75
90	X	260	0.45915	90.00	X	213.82
90	X	270	0.44325	90.00	X	220.89
100	X	110	1.03435	100.00	X	110.00
100	X	120	0.96082	100.00	X	120.00
100	X	130	0.89713	100.00	X	127.91
100	X	140	0.84142	100.00	X	134.98
100	X	150	0.79227	100.00	X	142.05
110	X	120	0.88729	110.00	X	120.00
110	X	130	0.82853	110.00	X	127.91
110	X	140	0.77711	110.00	X	134.98
110	X	150	0.73176	110.00	X	142.05
110	X	160	0.69142	110.00	X	149.12
120	X	130	0.76975	120.00	X	127.91
120	X	140	0.72202	120.00	X	134.98
120	X	150	0.67990	120.00	X	142.05
120	X	160	0.64246	120.00	X	149.12
120	X	170	0.60895	120.00	X	156.19
120	X	180	0.57877	120.00	X	163.26
130	X	140	0.67430	127.91	X	134.98
130	X	150	0.63498	127.91	X	142.05
130	X	160	0.60003	127.91	X	149.12
130	X	170	0.56875	127.91	X	156.19
130	X	180	0.54058	127.91	X	163.26
130	X	190	0.51508	127.91	X	170.33
140	X	150	0.59567	134.98	X	142.05
140	X	160	0.56290	134.98	X	149.12
140	X	170	0.53357	134.98	X	156.19
140	X	180	0.50715	134.98	X	163.26
140	X	190	0.48324	134.98	X	170.33
140	X	200	0.46149	134.98	X	177.40
140	X	210	0.44162	134.98	X	184.47
150	X	160	0.53015	142.05	X	149.12
150	X	170	0.50251	142.05	X	156.19
150	X	180	0.47765	142.05	X	163.26
150	X	190	0.45513	142.05	X	170.33

TABLE 19. (CONTINUED)

150	X	200	0.43465	142.05	X	177.40
150	X	210	0.41595	142.05	X	184.47
150	X	220	0.39879	142.05	X	191.54
160	X	170	0.47490	149.12	X	156.19
160	X	180	0.45140	149.12	X	163.26
160	X	190	0.43013	149.12	X	170.33
160	X	200	0.41079	149.12	X	177.40
160	X	210	0.39311	149.12	X	184.47
160	X	220	0.37690	149.12	X	191.54
160	X	230	0.36198	149.12	X	198.61
160	X	240	0.34820	149.12	X	205.68
170	X	180	0.42794	156.19	X	163.26
170	X	190	0.40777	156.19	X	170.33
170	X	200	0.38943	156.19	X	177.40
170	X	210	0.37267	156.19	X	184.47
170	X	220	0.35730	156.19	X	191.54
170	X	230	0.34316	156.19	X	198.61
170	X	240	0.33009	156.19	X	205.68
170	X	250	0.31799	156.19	X	212.75
180	X	190	0.38761	163.26	X	170.33
180	X	200	0.37017	163.26	X	177.40
180	X	210	0.35426	163.26	X	184.47
180	X	220	0.33960	163.26	X	191.54
180	X	230	0.32621	163.26	X	198.61
180	X	240	0.31379	163.26	X	205.68
180	X	250	0.30229	163.26	X	212.75
180	X	260	0.29160	163.26	X	219.82
180	X	270	0.28165	163.26	X	226.89
190	X	200	0.35279	170.33	X	177.40
190	X	210	0.33758	170.33	X	184.47
190	X	220	0.32367	170.33	X	191.54
190	X	230	0.31086	170.33	X	198.61
190	X	240	0.29903	170.33	X	205.68
190	X	250	0.28808	170.33	X	212.75
190	X	260	0.27789	170.33	X	219.82
190	X	270	0.26841	170.33	X	226.89
190	X	280	0.25955	170.33	X	233.96
200	X	250	0.27514	177.40	X	212.75
200	X	300	0.23255	177.40	X	248.10
250	X	300	0.18997	212.75	X	248.10
250	X	350	0.16454	212.75	X	283.45
300	X	350	0.13910	248.10	X	283.45
300	X	400	0.12268	248.10	X	318.80
300	X	450	0.10971	248.10	X	354.15
350	X	400	0.10628	283.45	X	318.80
350	X	450	0.09506	283.45	X	354.15
350	X	500	0.08599	283.45	X	389.50
400	X	450	0.08385	318.80	X	354.15
400	X	500	0.07585	318.80	X	389.50
400	X	550	0.06924	318.80	X	424.85
400	X	600	0.06370	318.80	X	460.20

TABLE 19. (CONTINUED)

450	X	500	0.06785	354.15	X	389.50
450	X	550	0.06194	354.15	X	424.85
450	X	600	0.05698	354.15	X	460.20
450	X	650	0.05276	354.15	X	495.55
500	X	550	0.05604	389.50	X	424.85

TABLE 20. RECTANGULAR SURFACE ATTACHMENT - ABLEBOND 36-2 EPOXY

MATERIAL: EPOXY
CONDUCTIVITY: 5.10000E-02 (W/IN.*C)
SPREADING ANGLE: 45 (DEGREES)

LENGTH	*	WIDTH	THERMAL RESISTANCE	Linc	*	Winc
2	X	4	1987.57227	2.00	X	4.00
2	X	6	1440.65479	2.00	X	6.00
4	X	6	893 [illegible]3402	4.00	X	6.00
4	X	8	70[illegible] [illegible]66	4.00	X	8.00
4	X	10	582.80274	4.00	X	10.00
4	X	12	496.89356	4.00	X	12.00
6	X	8	516.47193	6.00	X	8.00
6	X	10	427.33716	6.00	X	10.00
6	X	12	364.61359	6.00	X	12.00
6	X	14	318.02881	6.00	X	14.00
6	X	16	282.04108	6.00	X	16.00
6	X	18	253.39508	6.00	X	18.00
8	X	10	338.20270	8.00	X	10.00
8	X	12	288.68433	8.00	X	12.00
8	X	14	251.88123	8.00	X	14.00
8	X	16	223.43351	8.00	X	16.00
8	X	18	200.77891	8.00	X	18.00
8	X	20	182.30698	8.00	X	20.00
8	X	22	166.95457	8.00	X	22.00
8	X	24	153.99201	8.00	X	24.00
10	X	15	196.24143	10.00	X	15.00
10	X	20	151.12875	10.00	X	20.00
10	X	25	122.91018	10.00	X	25.00
10	X	30	103.58320	10.00	X	30.00
15	X	20	106.01372	15.00	X	20.00
15	X	25	86.24472	15.00	X	25.00
15	X	30	72.69678	15.00	X	30.00
15	X	35	62.83164	15.00	X	35.00
15	X	40	55.32501	15.00	X	40.00
15	X	45	49.42216	15.00	X	45.00
20	X	25	66.47504	20.00	X	25.00
20	X	30	56.03871	20.00	X	30.00
20	X	35	48.43681	20.00	X	35.00
20	X	40	42.65257	20.00	X	40.00
20	X	45	38.10360	20.00	X	45.00

TABLE 20. (CONTINUED)

20	X	50	34.43162	20.00	X	50.00
20	X	55	31.40551	20.00	X	55.16
20	X	60	28.86845	20.00	X	62.23
25	X	30	45.60268	25.00	X	30.00
25	X	35	39.41858	25.00	X	35.00
25	X	40	34.71226	25.00	X	40.00
25	X	45	31.01099	25.00	X	45.00
25	X	50	28.02312	25.00	X	50.00
25	X	55	25.56090	25.00	X	55.00
25	X	60	23.49645	25.00	X	60.00
25	X	65	21.74045	25.00	X	65.00
25	X	70	20.22895	25.00	X	70.00
25	X	75	18.91378	25.00	X	75.00
30	X	35	33.23519	30.00	X	35.00
30	X	40	29.26775	30.00	X	40.00
30	X	45	26.14769	30.00	X	45.00
30	X	50	23.62925	30.00	X	50.00
30	X	55	21.55268	30.00	X	55.00
30	X	60	19.81197	30.00	X	60.00
30	X	65	18.33175	30.00	X	65.00
30	X	70	17.05732	30.00	X	70.00
30	X	75	15.94860	30.00	X	75.00
30	X	80	14.97512	30.00	X	80.00
30	X	85	14.11381	30.00	X	86.28
30	X	90	13.34618	30.00	X	93.35
35	X	40	25.30200	35.00	X	40.00
35	X	45	22.60357	35.00	X	45.00
35	X	50	20.42669	35.00	X	50.00
35	X	55	18.63230	35.00	X	55.00
35	X	60	17.12779	35.00	X	60.00
35	X	65	15.84805	35.00	X	65.00
35	X	70	14.74621	35.00	X	70.00
35	X	75	13.78779	35.00	X	75.00
35	X	80	12.94625	35.00	X	80.00
35	X	85	12.20177	35.00	X	86.28
35	X	90	11.53818	35.00	X	93.35
35	X	95	10.94301	35.00	X	99.00
35	X	100	10.40616	35.00	X	104.00
35	X	105	9.91967	35.00	X	109.00
40	X	45	19.90781	40.00	X	45.00
40	X	50	17.98995	40.00	X	50.00
40	X	55	16.40941	40.00	X	55.00
40	X	60	15.08420	40.00	X	60.00
40	X	65	13.95751	40.00	X	65.00
40	X	70	12.98720	40.00	X	70.00
40	X	75	12.14314	40.00	X	75.00
40	X	80	11.40204	40.00	X	80.00
40	X	85	10.74633	40.00	X	86.28
40	X	90	10.16190	40.00	X	93.35
40	X	95	9.63770	40.00	X	99.00
40	X	100	9.16496	40.00	X	104.00

TABLE 20. (CONTINUED)

40	X	105	8.73656	40.00	X	109.00
40	X	110	8.34621	40.00	X	114.00
40	X	115	7.98937	40.00	X	119.00
40	X	120	7.66186	40.00	X	124.00
45	X	50	16.07307	45.00	X	50.00
45	X	55	14.66086	45.00	X	55.00
45	X	60	13.47674	45.00	X	60.00
45	X	65	12.47029	45.00	X	65.00
45	X	70	11.60305	45.00	X	70.00
45	X	75	10.84917	45.00	X	75.00
45	X	80	10.18705	45.00	X	80.00
45	X	85	9.60119	45.00	X	86.28
45	X	90	9.07909	45.00	X	93.35
45	X	95	8.61078	45.00	X	99.00
45	X	100	8.18848	45.00	X	104.00
45	X	105	7.80569	45.00	X	109.00
45	X	110	7.45705	45.00	X	114.00
45	X	115	7.13822	45.00	X	119.00
45	X	120	6.84549	45.00	X	124.00
45	X	125	6.57590	45.00	X	129.00
45	X	130	6.32674	45.00	X	134.00
45	X	135	6.09574	45.00	X	139.00
50	X	60	12.17997	50.00	X	60.00
50	X	70	10.48584	50.00	X	70.00
50	X	80	9.20624	50.00	X	80.00
50	X	90	8.20500	50.00	X	90.00
50	X	100	7.40007	50.00	X	100.00
50	X	110	6.73903	50.00	X	113.15
50	X	120	6.18649	50.00	X	124.00
50	X	130	5.71766	50.00	X	134.00
50	X	140	5.31489	50.00	X	144.00
50	X	150	4.96515	50.00	X	154.00
60	X	70	8.79319	60.00	X	70.00
60	X	80	7.71982	60.00	X	80.00
60	X	90	6.88041	60.00	X	90.00
60	X	100	6.20536	60.00	X	100.00
60	X	110	5.65109	60.00	X	113.15
60	X	120	5.18769	60.00	X	124.00
60	X	130	4.79459	60.00	X	134.00
60	X	140	4.45689	60.00	X	144.00
60	X	150	4.16356	60.00	X	154.00
60	X	160	3.90647	60.00	X	164.00
60	X	170	3.67934	60.00	X	174.00
60	X	180	3.47712	60.00	X	184.00
70	X	80	6.64699	70.00	X	80.00
70	X	90	5.92417	70.00	X	90.00
70	X	100	5.34297	70.00	X	100.00
70	X	110	4.86575	70.00	X	113.15
70	X	120	4.46680	70.00	X	124.00
70	X	130	4.12831	70.00	X	134.00
70	X	140	3.83744	70.00	X	144.00

TABLE 20. (CONTINUED)

70	X	150	3.58487	70.00	X	154.00
70	X	160	3.36355	70.00	X	164.00
70	X	170	3.16802	70.00	X	174.00
70	X	180	2.99394	70.00	X	184.00
70	X	190	2.83796	70.00	X	194.00
70	X	200	2.69741	70.00	X	204.00
70	X	210	2.57014	70.00	X	214.00
80	X	90	5.20131	80.00	X	90.00
80	X	100	4.69134	80.00	X	100.00
80	X	110	4.27195	80.00	X	113.15
80	X	120	3.92183	80.00	X	124.00
80	X	130	3.62458	80.00	X	134.00
80	X	140	3.36919	80.00	X	144.00
80	X	150	3.14747	80.00	X	154.00
80	X	160	2.95316	80.00	X	164.00
80	X	170	2.78150	80.00	X	174.00
80	X	180	2.62859	80.00	X	184.00
80	X	190	2.49172	80.00	X	194.00
80	X	200	2.36833	80.00	X	204.00
80	X	210	2.25656	80.00	X	214.00
80	X	220	2.15489	80.00	X	224.00
80	X	230	2.06196	80.00	X	234.00
80	X	240	1.97680	80.00	X	244.00
90	X	100	4.18093	90.00	X	100.00
90	X	110	3.80748	90.00	X	113.15
90	X	120	3.49529	90.00	X	124.00
90	X	130	3.23061	90.00	X	134.00
90	X	140	3.00284	90.00	X	144.00
90	X	150	2.80526	90.00	X	154.00
90	X	160	2.63206	90.00	X	164.00
90	X	170	2.47907	90.00	X	174.00
90	X	180	2.34274	90.00	X	184.00
90	X	190	2.22070	90.00	X	194.00
90	X	200	2.11075	90.00	X	204.00
90	X	210	2.01121	90.00	X	214.00
90	X	220	1.92062	90.00	X	224.00
90	X	230	1.83780	90.00	X	234.00
90	X	240	1.76183	90.00	X	244.00
90	X	250	1.69193	90.00	X	254.00
90	X	260	1.62735	90.00	X	264.00
90	X	270	1.56753	90.00	X	274.00
100	X	110	3.43444	100.00	X	110.00
100	X	120	3.15268	100.00	X	120.00
100	X	130	2.91371	100.00	X	132.96
100	X	140	2.70845	100.00	X	144.00
100	X	150	2.53030	100.00	X	154.00
110	X	120	2.87157	110.00	X	120.00
110	X	130	2.65361	110.00	X	132.96
110	X	140	2.46645	110.00	X	144.00
110	X	150	2.30434	110.00	X	154.00
110	X	160	2.16194	110.00	X	164.00

TABLE 20. (CONTINUED)

120	X	130	2.43644	120.00	X	132.96
120	X	140	2.26459	120.00	X	144.00
120	X	150	2.11551	120.00	X	154.00
120	X	160	1.98463	120.00	X	164.00
120	X	170	1.86930	120.00	X	174.00
120	X	180	1.76664	120.00	X	184.00
130	X	140	2.09358	132.96	X	144.00
130	X	150	1.95524	132.96	X	154.00
130	X	160	1.83437	132.96	X	164.00
130	X	170	1.72769	132.96	X	174.00
130	X	180	1.63276	132.96	X	184.00
130	X	190	1.54766	132.96	X	194.00
140	X	150	1.81716	144.00	X	154.00
140	X	160	1.70516	144.00	X	164.00
140	X	170	1.60592	144.00	X	174.00
140	X	180	1.51785	144.00	X	184.00
140	X	190	1.43858	144.00	X	194.00
140	X	200	1.36751	144.00	X	204.00
140	X	210	1.30291	144.00	X	214.00
150	X	160	1.59354	154.00	X	164.00
150	X	170	1.50064	154.00	X	174.00
150	X	180	1.41796	154.00	X	184.00
150	X	190	1.34399	154.00	X	194.00
150	X	200	1.27742	154.00	X	204.00
150	X	210	1.21724	154.00	X	214.00
150	X	220	1.16231	154.00	X	224.00
160	X	170	1.40840	164.00	X	174.00
160	X	180	1.33052	164.00	X	184.00
160	X	190	1.26113	164.00	X	194.00
160	X	200	1.19865	164.00	X	204.00
160	X	210	1.14199	164.00	X	214.00
160	X	220	1.09056	164.00	X	224.00
160	X	230	1.04358	164.00	X	234.00
160	X	240	1.00040	164.00	X	244.00
170	X	180	1.25374	174.00	X	184.00
170	X	190	1.18778	174.00	X	194.00
170	X	200	1.12922	174.00	X	204.00
170	X	210	1.07579	174.00	X	214.00
170	X	220	1.02718	174.00	X	224.00
170	X	230	0.98293	174.00	X	234.00
170	X	240	0.94230	174.00	X	244.00
170	X	250	0.90488	174.00	X	254.00
180	X	190	1.12298	184.00	X	194.00
180	X	200	1.06699	184.00	X	204.00
180	X	210	1.01666	184.00	X	214.00
180	X	220	0.97086	184.00	X	224.00
180	X	230	0.92884	184.00	X	234.00
180	X	240	0.89049	184.00	X	244.00
180	X	250	0.85517	184.00	X	254.00
180	X	260	0.82259	184.00	X	264.00
180	X	270	0.79224	184.00	X	274.00

TABLE 20. (CONTINUED)

190	X	200	1.01189	194.00	X	204.00
190	X	210	0.96381	194.00	X	214.00
190	X	220	0.92054	194.00	X	224.00
190	X	230	0.88057	194.00	X	234.00
190	X	240	0.84405	194.00	X	244.00
190	X	250	0.81071	194.00	X	254.00
190	X	260	0.77972	194.00	X	264.00
190	X	270	0.75099	194.00	X	274.00
190	X	280	0.72439	194.00	X	284.00
200	X	250	0.77052	204.00	X	254.00
200	X	300	0.64288	204.00	X	304.00
250	X	300	0.51533	254.00	X	304.00
250	X	350	0.44216	254.00	X	354.00
300	X	350	0.36912	304.00	X	354.00
300	X	400	0.32308	304.00	X	404.00
300	X	450	0.28730	304.00	X	454.00
350	X	400	0.27723	354.00	X	404.00
350	X	450	0.24652	354.00	X	454.00
350	X	500	0.22197	354.00	X	504.00
400	X	450	0.21591	404.00	X	454.00
400	X	500	0.19440	404.00	X	504.00
400	X	550	0.17673	404.00	X	554.00
400	X	600	0.16208	404.00	X	604.00
450	X	500	0.17289	454.00	X	504.00
450	X	550	0.15722	454.00	X	554.00
450	X	600	0.14415	454.00	X	604.00
450	X	650	0.13309	454.00	X	654.00
500	X	550	0.14165	504.00	X	554.00

TABLE 21. RECTANGULAR SURFACE HEADER - GOLD PLATE

MATERIAL: GOLD
CONDUCTIVITY: 7.54 (W/IN.*C)
SPREADING ANGLE: 45 (DEGREES)

LENGTH	*	WIDTH	THERMAL RESISTANCE	Linc	*	Winc
2	X	4	2.88499	2.40	X	4.40
2	X	6	1.95265	2.40	X	6.40
4	X	6	1.02028	4.40	X	6.40
4	X	8	0.77123	4.40	X	8.40
4	X	10	0.61992	4.40	X	10.40
4	X	12	0.51825	4.40	X	12.40
6	X	8	0.52217	6.40	X	8.40
6	X	10	0.41973	6.40	X	10.40
6	X	12	0.35089	6.40	X	12.40
6	X	14	0.30147	6.40	X	14.40
6	X	16	0.26423	6.40	X	16.40
6	X	18	0.23519	6.40	X	18.40

TABLE 21. (CONTINUED)

8	X	10	0.31732	8.40	X	10.40
8	X	12	0.26527	8.40	X	12.40
8	X	14	0.22789	8.40	X	14.40
8	X	16	0.19975	8.40	X	16.40
8	X	18	0.17780	8.40	X	18.40
8	X	20	0.16019	8.40	X	20.40
8	X	22	0.14576	8.40	X	22.40
8	X	24	0.13371	8.40	X	24.40
10	X	15	0.17115	10.40	X	15.40
10	X	20	0.12877	10.40	X	20.40
10	X	25	0.10322	10.40	X	25.40
10	X	30	0.08613	10.40	X	30.40
15	X	20	0.08640	15.40	X	20.40
15	X	25	0.06926	15.40	X	25.40
15	X	30	0.05779	15.40	X	30.40
15	X	35	0.04958	15.40	X	35.40
15	X	40	0.04341	15.40	X	40.40
15	X	45	0.03861	15.40	X	45.40
20	X	25	0.05212	20.40	X	25.40
20	X	30	0.04348	20.40	X	30.40
20	X	35	0.03731	20.40	X	35.40
20	X	40	0.03267	20.40	X	40.40
20	X	45	0.02905	20.40	X	45.40
20	X	50	0.02616	20.40	X	50.40
20	X	55	0.02379	20.40	X	55.40
20	X	60	0.02182	20.40	X	60.40
25	X	30	0.03486	25.40	X	30.40
25	X	35	0.02991	25.40	X	35.40
25	X	40	0.02618	25.40	X	40.40
25	X	45	0.02329	25.40	X	45.40
25	X	50	0.02097	25.40	X	50.40
25	X	55	0.01907	25.40	X	55.40
25	X	60	0.01749	25.40	X	60.40
25	X	65	0.01615	25.40	X	65.40
25	X	70	0.01500	25.40	X	70.40
25	X	75	0.01400	25.40	X	75.40
30	X	35	0.02497	30.40	X	35.40
30	X	40	0.02185	30.40	X	40.40
30	X	45	0.01943	30.40	X	45.40
30	X	50	0.01750	30.40	X	50.40
30	X	55	0.01592	30.40	X	55.40
30	X	60	0.01459	30.40	X	60.40
30	X	65	0.01347	30.40	X	65.40
30	X	70	0.01251	30.40	X	70.40
30	X	75	0.01168	30.40	X	75.40
30	X	80	0.01095	30.40	X	80.40
30	X	85	0.01031	30.40	X	85.40
30	X	90	0.00974	30.40	X	90.40
35	X	40	0.01875	35.40	X	40.40
35	X	45	0.01667	35.40	X	45.40
35	X	50	0.01501	35.40	X	50.40

TABLE 21. (CONTINUED)

35	X	55	0.01365	35.40	X	55.40
35	X	60	0.01252	35.40	X	60.40
35	X	65	0.01156	35.40	X	65.40
35	X	70	0.01074	35.40	X	70.40
35	X	75	0.01002	35.40	X	75.40
35	X	80	0.00940	35.40	X	80.40
35	X	85	0.00885	35.40	X	85.40
35	X	90	0.00836	35.40	X	90.40
35	X	95	0.00792	35.40	X	95.40
35	X	100	0.00752	35.40	X	100.40
35	X	105	0.00716	35.40	X	105.40
40	X	45	0.01460	40.40	X	45.40
40	X	50	0.01315	40.40	X	50.40
40	X	55	0.01195	40.40	X	55.40
40	X	60	0.01096	40.40	X	60.40
40	X	65	0.01012	40.40	X	65.40
40	X	70	0.00940	40.40	X	70.40
40	X	75	0.00878	40.40	X	75.40
40	X	80	0.00823	40.40	X	80.40
40	X	85	0.00775	40.40	X	85.40
40	X	90	0.00732	40.40	X	90.40
40	X	95	0.00693	40.40	X	95.40
40	X	100	0.00659	40.40	X	100.40
40	X	105	0.00627	40.40	X	105.40
40	X	110	0.00599	40.40	X	110.40
40	X	115	0.00573	40.40	X	115.40
40	X	120	0.00549	40.40	X	120.40
45	X	50	0.01169	45.40	X	50.40
45	X	55	0.01064	45.40	X	55.40
45	X	60	0.00975	45.40	X	60.40
45	X	65	0.00900	45.40	X	65.40
45	X	70	0.00836	45.40	X	70.40
45	X	75	0.00780	45.40	X	75.40
45	X	80	0.00732	45.40	X	80.40
45	X	85	0.00689	45.40	X	85.40
45	X	90	0.00651	45.40	X	90.40
45	X	95	0.00617	45.40	X	95.40
45	X	100	0.00586	45.40	X	100.40
45	X	105	0.00558	45.40	X	105.40
45	X	110	0.00533	45.40	X	110.40
45	X	115	0.00509	45.40	X	115.40
45	X	120	0.00488	45.40	X	120.40
45	X	125	0.00469	45.40	X	125.40
45	X	130	0.00451	45.40	X	130.40
45	X	135	0.00434	45.40	X	135.40
50	X	60	0.00879	50.40	X	60.40
50	X	70	0.00753	50.40	X	70.40
50	X	80	0.00659	50.40	X	80.40
50	X	90	0.00586	50.40	X	90.40
50	X	100	0.00527	50.40	X	100.40
50	X	110	0.00479	50.40	X	110.40

TABLE 21. (CONTINUED)

50	X	120	0.00440	50.40	X	120.40
50	X	130	0.00406	50.40	X	130.40
50	X	140	0.00377	50.40	X	140.40
50	X	150	0.00352	50.40	X	150.40
60	X	70	0.00628	60.40	X	70.40
60	X	80	0.00549	60.40	X	80.40
60	X	90	0.00489	60.40	X	90.40
60	X	100	0.00440	60.40	X	100.40
60	X	110	0.00400	60.40	X	110.40
60	X	120	0.00367	60.40	X	120.40
60	X	130	0.00338	60.40	X	130.40
60	X	140	0.00314	60.40	X	140.40
60	X	150	0.00293	60.40	X	150.40
60	X	160	0.00275	60.40	X	160.40
60	X	170	0.00259	60.40	X	170.40
60	X	180	0.00245	60.40	X	180.40
70	X	80	0.00471	70.40	X	80.40
70	X	90	0.00419	70.40	X	90.40
70	X	100	0.00377	70.40	X	100.40
70	X	110	0.00343	70.40	X	110.40
70	X	120	0.00314	70.40	X	120.40
70	X	130	0.00290	70.40	X	130.40
70	X	140	0.00270	70.40	X	140.40
70	X	150	0.00252	70.40	X	150.40
70	X	160	0.00236	70.40	X	160.40
70	X	170	0.00222	70.40	X	170.40
70	X	180	0.00210	70.40	X	180.40
70	X	190	0.00199	70.40	X	190.40
70	X	200	0.00189	70.40	X	200.40
70	X	210	0.00180	70.40	X	210.40
80	X	90	0.00367	80.40	X	90.40
80	X	100	0.00330	80.40	X	100.40
80	X	110	0.00300	80.40	X	110.40
80	X	120	0.00275	80.40	X	120.40
80	X	130	0.00254	80.40	X	130.40
80	X	140	0.00236	80.40	X	140.40
80	X	150	0.00220	80.40	X	150.40
80	X	160	0.00206	80.40	X	160.40
80	X	170	0.00194	80.40	X	170.40
80	X	180	0.00184	80.40	X	180.40
80	X	190	0.00174	80.40	X	190.40
80	X	200	0.00165	80.40	X	200.40
80	X	210	0.00157	80.40	X	210.40
80	X	220	0.00150	80.40	X	220.40
80	X	230	0.00144	80.40	X	230.40
80	X	240	0.00138	80.40	X	240.40
90	X	100	0.00294	90.40	X	100.40
90	X	110	0.00267	90.40	X	110.40
90	X	120	0.00245	90.40	X	120.40
90	X	130	0.00226	90.40	X	130.40
90	X	140	0.00210	90.40	X	140.40

TABLE 21. (CONTINUED)

90	X	150	0.00196	90.40	X	150.40
90	X	160	0.00184	90.40	X	160.40
90	X	170	0.00173	90.40	X	170.40
90	X	180	0.00163	90.40	X	180.40
90	X	190	0.00155	90.40	X	190.40
90	X	200	0.00147	90.40	X	200.40
90	X	210	0.00140	90.40	X	210.40
90	X	220	0.00134	90.40	X	220.40
90	X	230	0.00128	90.40	X	230.40
90	X	240	0.00122	90.40	X	240.40
90	X	250	0.00118	90.40	X	250.40
90	X	260	0.00113	90.40	X	260.40
90	X	270	0.00109	90.40	X	270.40
100	X	110	0.00240	100.40	X	110.40
100	X	120	0.00221	100.40	X	120.40
100	X	130	0.00204	100.40	X	130.40
100	X	140	0.00189	100.40	X	140.40
100	X	150	0.00176	100.40	X	150.40
110	X	120	0.00200	110.40	X	120.40
110	X	130	0.00185	110.40	X	130.40
110	X	140	0.00172	110.40	X	140.40
110	X	150	0.00160	110.40	X	150.40
110	X	160	0.00150	110.40	X	160.40
120	X	130	0.00170	120.40	X	130.40
120	X	140	0.00158	120.40	X	140.40
120	X	150	0.00147	120.40	X	150.40
120	X	160	0.00138	120.40	X	160.40
120	X	170	0.00130	120.40	X	170.40
120	X	180	0.00123	120.40	X	180.40
130	X	140	0.00146	130.40	X	140.40
130	X	150	0.00136	130.40	X	150.40
130	X	160	0.00127	130.40	X	160.40
130	X	170	0.00120	130.40	X	170.40
130	X	180	0.00113	130.40	X	180.40
130	X	190	0.00107	130.40	X	190.40
140	X	150	0.00127	140.40	X	150.40
140	X	160	0.00118	140.40	X	160.40
140	X	170	0.00111	140.40	X	170.40
140	X	180	0.00105	140.40	X	180.40
140	X	190	0.00100	140.40	X	190.40
140	X	200	0.00095	140.40	X	200.40
140	X	210	0.00090	140.40	X	210.40
150	X	160	0.00110	150.40	X	160.40
150	X	170	0.00104	150.40	X	170.40
150	X	180	0.00098	150.40	X	180.40
150	X	190	0.00093	150.40	X	190.40
150	X	200	0.00088	150.40	X	200.40
150	X	210	0.00084	150.40	X	210.40
150	X	220	0.00080	150.40	X	220.40
160	X	170	0.00098	160.40	X	170.40
160	X	180	0.00092	160.40	X	180.40

TABLE 21. (CONTINUED)

160	X	190	0.00087	160.40	X	190.40
160	X	200	0.00083	160.40	X	200.40
160	X	210	0.00079	160.40	X	210.40
160	X	220	0.00075	160.40	X	220.40
160	X	230	0.00072	160.40	X	230.40
160	X	240	0.00069	160.40	X	240.40
170	X	180	0.00087	170.40	X	180.40
170	X	190	0.00082	170.40	X	190.40
170	X	200	0.00078	170.40	X	200.40
170	X	210	0.00074	170.40	X	210.40
170	X	220	0.00071	170.40	X	220.40
170	X	230	0.00068	170.40	X	230.40
170	X	240	0.00065	170.40	X	240.40
170	X	250	0.00062	170.40	X	250.40
180	X	190	0.00078	180.40	X	190.40
180	X	200	0.00074	180.40	X	200.40
180	X	210	0.00070	180.40	X	210.40
180	X	220	0.00067	180.40	X	220.40
180	X	230	0.00064	180.40	X	230.40
180	X	240	0.00061	180.40	X	240.40
180	X	250	0.00059	180.40	X	250.40
180	X	260	0.00057	180.40	X	260.40
180	X	270	0.00055	180.40	X	270.40
190	X	200	0.00070	190.40	X	200.40
190	X	210	0.00067	190.40	X	210.40
190	X	220	0.00064	190.40	X	220.40
190	X	230	0.00061	190.40	X	230.40
190	X	240	0.00058	190.40	X	240.40
190	X	250	0.00056	190.40	X	250.40
190	X	260	0.00054	190.40	X	260.40
190	X	270	0.00052	190.40	X	270.40
190	X	280	0.00050	190.40	X	280.40
200	X	250	0.00053	200.40	X	250.40
200	X	300	0.00044	200.40	X	300.40
250	X	300	0.00035	250.40	X	300.40
250	X	350	0.00030	250.40	X	350.40
300	X	350	0.00025	300.40	X	350.40
300	X	400	0.00022	300.40	X	400.40
300	X	450	0.00020	300.40	X	450.40
350	X	400	0.00019	350.40	X	400.40
350	X	450	0.00017	350.40	X	450.40
350	X	500	0.00015	350.40	X	500.40
400	X	450	0.00015	400.40	X	450.40
400	X	500	0.00013	400.40	X	500.40
400	X	550	0.00012	400.40	X	550.40
400	X	600	0.00011	400.40	X	600.40
450	X	500	0.00012	450.40	X	500.40
450	X	550	0.00011	450.40	X	550.40
450	X	600	0.00010	450.40	X	600.40
450	X	650	0.00009	450.40	X	650.40
500	X	550	0.00010	500.40	X	550.40

TABLE 22. RECTANGULAR - 40 PIN CERAMIC SIDE BRAZED PACKAGE

MATERIAL: ALUMINA
CONDUCTIVITY: .478 (W/IN.*C)
SPREADING ANGLE: 45 (DEGREES)
ATTACHMENT MATERIAL: NON-CONDUCTIVE EPOXY
INTERMEDIATE MATERIAL: GOLD HEADER

LENGTH * WIDTH	THERMAL RESISTANCE	Linc * Winc
2 X 4	352.74793	106.00 X 108.00
2 X 6	277.60706	106.00 X 110.00
4 X 6	202.46662	108.00 X 110.00
4 X 8	171.75175	108.00 X 112.00
4 X 10	150.31781	108.00 X 114.00
4 X 12	134.30350	108.00 X 116.00
6 X 8	141.03760	110.00 X 112.00
6 X 10	124.24382	110.00 X 114.00
6 X 12	111.58256	110.00 X 116.00
6 X 14	101.60744	110.00 X 118.00
6 X 16	93.49555	110.00 X 120.00
6 X 18	86.73919	110.00 X 122.00
8 X 10	107.45017	112.00 X 114.00
8 X 12	96.85520	112.00 X 116.00
8 X 14	88.46430	112.00 X 118.00
8 X 16	81.61023	112.00 X 120.00
8 X 18	75.87959	112.00 X 122.00
8 X 20	70.99969	112.00 X 124.00
8 X 22	66.78260	112.00 X 126.00
8 X 24	63.09367	112.00 X 128.00
10 X 15	75.84531	114.00 X 119.00
10 X 20	63.70966	114.00 X 124.00
10 X 25	55.27736	114.00 X 129.00
10 X 30	49.00475	114.00 X 134.00
15 X 20	51.12657	113.00 X 118.00
15 X 25	44.56381	113.00 X 123.00
15 X 30	39.64470	113.00 X 128.00
15 X 35	35.79169	113.00 X 133.00
15 X 40	32.67627	113.00 X 138.00
15 X 45	30.09610	113.00 X 143.00
20 X 25	38.00090	118.00 X 123.00
20 X 30	33.90371	118.00 X 128.00
20 X 35	30.68004	118.00 X 133.00
20 X 40	28.06371	118.00 X 138.00
20 X 45	25.88998	118.00 X 143.00
20 X 50	24.05033	118.00 X 148.00
20 X 55	22.47003	118.00 X 153.00
20 X 60	21.09578	118.00 X 158.00
25 X 30	29.80668	123.00 X 128.00
25 X 35	27.01967	123.00 X 133.00
25 X 40	24.75137	123.00 X 138.00

TABLE 22. (CONTINUED)

25	X	45	22.86230	123.00	X	143.00
25	X	50	21.26022	123.00	X	148.00
25	X	55	19.88157	123.00	X	153.00
25	X	60	18.68075	123.00	X	158.00
25	X	65	17.62410	123.00	X	163.00
25	X	70	16.68619	123.00	X	168.00
25	X	75	15.84737	123.00	X	173.00
30	X	35	23.84629	122.00	X	127.00
30	X	40	21.85158	122.00	X	132.00
30	X	45	20.18866	122.00	X	137.00
30	X	50	18.77723	122.00	X	142.00
30	X	55	17.56167	122.00	X	147.00
30	X	60	16.50237	122.00	X	152.00
30	X	65	15.56980	122.00	X	157.00
30	X	70	14.74172	122.00	X	162.00
30	X	75	14.00089	122.00	X	167.00
30	X	80	13.33380	122.00	X	172.00
30	X	85	12.72966	122.00	X	177.00
30	X	90	12.17968	122.00	X	182.00
35	X	40	19.85714	127.00	X	132.00
35	X	45	18.35989	127.00	X	137.00
35	X	50	17.08759	127.00	X	142.00
35	X	55	15.99057	127.00	X	147.00
35	X	60	15.03362	127.00	X	152.00
35	X	65	14.19039	127.00	X	157.00
35	X	70	13.44105	127.00	X	162.00
35	X	75	12.77024	127.00	X	167.00
35	X	80	12.16578	127.00	X	172.00
35	X	85	11.61802	127.00	X	177.00
35	X	90	11.11909	127.00	X	182.00
35	X	95	10.66261	127.00	X	187.00
35	X	100	10.24324	127.00	X	192.00
35	X	105	9.85647	127.00	X	197.00
40	X	45	16.86292	132.00	X	137.00
40	X	50	15.70282	132.00	X	142.00
40	X	55	14.70178	132.00	X	147.00
40	X	60	13.82777	132.00	X	152.00
40	X	65	13.05707	132.00	X	157.00
40	X	70	12.37174	132.00	X	162.00
40	X	75	11.75785	132.00	X	167.00
40	X	80	11.20437	132.00	X	172.00
40	X	85	10.70258	132.00	X	177.00
40	X	90	10.24530	132.00	X	182.00
40	X	95	9.82679	132.00	X	187.00
40	X	100	9.44208	132.00	X	192.00
40	X	105	9.08721	132.00	X	197.00
40	X	110	8.75875	132.00	X	202.00
40	X	115	8.45377	132.00	X	207.00
40	X	120	8.16982	132.00	X	212.00
45	X	50	14.54283	137.00	X	142.00
45	X	55	13.62134	137.00	X	147.00

TABLE 22. (CONTINUED)

45	X	60	12.81612	137.00	X	152.00
45	X	65	12.10567	137.00	X	157.00
45	X	70	11.47355	137.00	X	162.00
45	X	75	10.90704	137.00	X	167.00
45	X	80	10.39601	137.00	X	172.00
45	X	85	9.93257	137.00	X	177.00
45	X	90	9.51003	137.00	X	182.00
45	X	95	9.12316	137.00	X	187.00
45	X	100	8.76747	137.00	X	192.00
45	X	105	8.43926	137.00	X	197.00
45	X	110	8.13535	137.00	X	202.00
45	X	115	7.85315	137.00	X	207.00
45	X	120	7.59029	137.00	X	212.00
45	X	125	7.34487	137.00	X	217.00
45	X	130	7.11514	137.00	X	222.00
45	X	135	6.89963	137.00	X	227.00
50	X	60	11.95280	142.00	X	152.00
50	X	70	10.70626	142.00	X	162.00
50	X	80	9.70491	142.00	X	172.00
50	X	90	8.88094	142.00	X	182.00
50	X	100	8.18993	142.00	X	192.00
50	X	110	7.60141	142.00	X	202.00
50	X	120	7.09369	142.00	X	212.00
50	X	130	6.65093	142.00	X	222.00
50	X	140	6.26115	142.00	X	232.00
50	X	150	5.91530	142.00	X	242.00
60	X	70	9.10169	144.00	X	154.00
60	X	80	8.24422	144.00	X	164.00
60	X	90	7.53918	144.00	X	174.00
60	X	100	6.94832	144.00	X	184.00
60	X	110	6.44543	144.00	X	194.00
60	X	120	6.01186	144.00	X	204.00
60	X	130	5.63401	144.00	X	214.00
60	X	140	5.30159	144.00	X	224.00
60	X	150	5.00678	144.00	X	234.00
60	X	160	4.74346	144.00	X	244.00
60	X	170	4.50679	144.00	X	254.00
60	X	180	4.29286	144.00	X	264.00
70	X	80	7.38682	154.00	X	164.00
70	X	90	6.75794	154.00	X	174.00
70	X	100	6.23056	154.00	X	184.00
70	X	110	5.78139	154.00	X	194.00
70	X	120	5.39393	154.00	X	204.00
70	X	130	5.05608	154.00	X	214.00
70	X	140	4.75872	154.00	X	224.00
70	X	150	4.49493	154.00	X	234.00
70	X	160	4.25922	154.00	X	244.00
70	X	170	4.04730	154.00	X	254.00
70	X	180	3.85571	154.00	X	264.00
70	X	190	3.68162	154.00	X	274.00
70	X	200	3.52270	154.00	X	284.00

TABLE 22. (CONTINUED)

70	X	210	3.37706	154.00	X	294.00
80	X	90	6.12909	164.00	X	174.00
80	X	100	5.65244	164.00	X	184.00
80	X	110	5.24625	164.00	X	194.00
80	X	120	4.89571	164.00	X	204.00
80	X	130	4.58995	164.00	X	214.00
80	X	140	4.32072	164.00	X	224.00
80	X	150	4.08180	164.00	X	234.00
80	X	160	3.86827	164.00	X	244.00
80	X	170	3.67626	164.00	X	254.00
80	X	180	3.50260	164.00	X	264.00
80	X	190	3.34477	164.00	X	274.00
80	X	200	3.20070	164.00	X	284.00
80	X	210	3.06862	164.00	X	294.00
80	X	220	2.94710	164.00	X	304.00
80	X	230	2.83492	164.00	X	314.00
80	X	240	2.73102	164.00	X	324.00
90	X	100	5.17581	174.00	X	184.00
90	X	110	4.80434	174.00	X	194.00
90	X	120	4.48458	174.00	X	204.00
90	X	130	4.20513	174.00	X	214.00
90	X	140	3.95904	174.00	X	224.00
90	X	150	3.74058	174.00	X	234.00
90	X	160	3.54531	174.00	X	244.00
90	X	170	3.36965	174.00	X	254.00
90	X	180	3.21076	174.00	X	264.00
90	X	190	3.06634	174.00	X	274.00
90	X	200	2.93448	174.00	X	284.00
90	X	210	2.81358	174.00	X	294.00
90	X	220	2.70234	174.00	X	304.00
90	X	230	2.59962	174.00	X	314.00
90	X	240	2.50447	174.00	X	324.00
90	X	250	2.41610	174.00	X	334.00
90	X	260	2.33378	174.00	X	344.00
90	X	270	2.25692	174.00	X	354.00
100	X	110	4.43392	184.00	X	194.00
100	X	120	4.13904	184.00	X	204.00
100	X	130	3.88161	184.00	X	214.00
100	X	140	3.65490	184.00	X	224.00
100	X	150	3.45356	184.00	X	234.00
110	X	120	3.73625	190.00	X	200.00
110	X	130	3.50270	190.00	X	210.00
110	X	140	3.29704	190.00	X	220.00
110	X	150	3.11455	190.00	X	230.00
110	X	160	2.95145	190.00	X	240.00
120	X	130	3.26911	200.00	X	210.00
120	X	140	3.07746	200.00	X	220.00
120	X	150	2.90734	200.00	X	230.00
120	X	160	2.75524	200.00	X	240.00
120	X	170	2.61849	200.00	X	250.00
120	X	180	2.49480	200.00	X	260.00

TABLE 22. (CONTINUED)

130	X	140	2.88578	210.00	X	220.00
130	X	150	2.72646	210.00	X	230.00
130	X	160	2.58399	210.00	X	240.00
130	X	170	2.45585	210.00	X	250.00
130	X	180	2.33994	210.00	X	260.00
130	X	190	2.23459	210.00	X	270.00
140	X	150	2.56716	220.00	X	230.00
140	X	160	2.43307	220.00	X	240.00
140	X	170	2.31253	220.00	X	250.00
140	X	180	2.20348	220.00	X	260.00
140	X	190	2.10436	220.00	X	270.00
140	X	200	2.01383	220.00	X	280.00
140	X	210	1.93085	220.00	X	290.00
150	X	160	2.29905	230.00	X	240.00
150	X	170	2.18527	230.00	X	250.00
150	X	180	2.08226	230.00	X	260.00
150	X	190	1.98867	230.00	X	270.00
150	X	200	1.90319	230.00	X	280.00
150	X	210	1.82482	230.00	X	290.00
150	X	220	1.75269	230.00	X	300.00
160	X	170	2.07145	240.00	X	250.00
160	X	180	1.97390	240.00	X	260.00
160	X	190	1.88521	240.00	X	270.00
160	X	200	1.80423	240.00	X	280.00
160	X	210	1.72997	240.00	X	290.00
160	X	220	1.66162	240.00	X	300.00
160	X	230	1.59352	240.00	X	310.00
160	X	240	1.54006	240.00	X	320.00
170	X	180	1.87639	250.00	X	260.00
170	X	190	1.79211	250.00	X	270.00
170	X	200	1.71518	250.00	X	280.00
170	X	210	1.64460	250.00	X	290.00
170	X	220	1.57969	250.00	X	300.00
170	X	230	1.51970	250.00	X	310.00
170	X	240	1.46416	250.00	X	320.00
170	X	250	1.41254	250.00	X	330.00
180	X	190	1.70793	260.00	X	270.00
180	X	200	1.63457	260.00	X	280.00
180	X	210	1.56737	260.00	X	290.00
180	X	220	1.50551	260.00	X	300.00
180	X	230	1.44838	260.00	X	310.00
180	X	240	1.39545	260.00	X	320.00
180	X	250	1.34629	260.00	X	330.00
180	X	260	1.30049	260.00	X	340.00
180	X	270	1.25771	260.00	X	350.00
190	X	200	1.56132	270.00	X	280.00
190	X	210	1.49713	270.00	X	290.00
190	X	220	1.43806	270.00	X	300.00
190	X	230	1.38351	270.00	X	310.00
190	X	240	1.33298	270.00	X	320.00
190	X	250	1.28603	270.00	X	330.00

TABLE 22. (CONTINUED)

190	X	260	1.24230	270.00	X	340.00
190	X	270	1.20146	270.00	X	350.00
190	X	280	1.16322	270.00	X	360.00
200	X	250	1.23098	280.00	X	330.00
200	X	300	1.04690	280.00	X	380.00
250	X	300	0.86284	330.00	X	380.00
250	X	350	0.75084	330.00	X	430.00
300	X	350	0.63886	380.00	X	430.00
300	X	400	0.56556	380.00	X	480.00
300	X	450	0.50739	380.00	X	530.00
350	X	400	0.49228	430.00	X	480.00
350	X	450	0.44167	430.00	X	530.00
350	X	500	0.40051	430.00	X	580.00
400	X	450	0.39107	480.00	X	530.00
400	X	500	0.35463	480.00	X	580.00
400	X	550	0.32441	480.00	X	630.00
400	X	600	0.29895	480.00	X	680.00
450	X	500	0.31819	530.00	X	580.00
450	X	550	0.29109	530.00	X	630.00
450	X	600	0.26825	530.00	X	680.00
450	X	650	0.24874	530.00	X	730.00
500	X	550	0.26399	580.00	X	630.00

TABLE 23. RECTANGULAR DEVICE AMPLE CALCULATION

Given:

Device: Material: Silicon (2.13 watts per inch-degrees centigrade 50 percent dissipation
Dimension: 120 x 140
Thickness: 18 Mils

Epoxy Type: Ablebond 36-2 (0.051 watts per inch-degrees centigrade)
Thickness: 2 Mils

Header Type: Gold Plate (7.54 watts per inch - degrees centigrade)
Thickness: 0.2 Mils

Package Type: Ceramic (0.478 watt per inch - degrees centigrade)
Thickness: 40 Mils

P_D: 1 Watt

Level	Material	Dimension (inches)	Thermal Resistance (degrees centigrade (per watt)	Next Level DIM
Device	Silicon	120 x 140	0.72202	120.00 x 134.98
Epoxy	Ablebond	120 x 134.98	2.35068	120.00 x 138.56
Header	Gold	120 x 138.56	0.00160	120.40 x 138.96
Package	Ceramic	120.4 x 138.96	3.10490	---
			6.179	

$\Delta T_{JC} = P_D * \theta_{JC}$
$= 1 * 6.179$
$= 6.179°C$

-Thermal resistance values are interpolated

5.3.3 Circular Model

Specific constructions, such as mesa devices, that are required to dissipate high power, are readily evaluated by a circular model. Actual temperature gradients could be more accurately described by a hemispherical model, but the added complexity is not warranted, due to the thin sections involved up to the point of the heat sink. The circular model can be represented by the following equation:

$$R1 = \frac{1}{K \cdot \pi \cdot TAN(A)} \cdot \frac{\frac{1}{R-1}}{R + T \cdot TAN(A)}$$

where

R1 = thermal resistance (degrees centigrade per watt)
K = material conductivity (watts per inch - degrees centigrade)
A = spreading angle (degrees)
R = radius (mils)
T = thickness (mils).

The value for K must be divided by 1000 in order to have agreement among measurement units.

Table 24 illustrates the use of the circular model tables. These tables are generated by the model programs for each level of construction. Tables 25 through 29 are of the same format as the ones that represent the square and rectangular surfaces. However, the diameter and radius are used in place of the length and width. When entering these data tables, it should be noted that the diameter is used as the entering dimension for the first level of construction. All subsequent levels use the radius.

Next level dimension computation for circular devices is based on the thickness of that particular level of construction and the radius of the dissipation area. The equation which represents this computation follows:

$$R^2 = R+T*TAN(A)$$

where

R^2 = new radius (mils)
R = present radius (mils)
T = present thickness (mils)
A = spreading angle (degrees).

The heat dissipated is assumed to be over 100 percent of the area, since circular devices have junctions over the entire surface.

TABLE 24. CIRCULAR SAMPLE

Given:

Device: Material - Silicon
Diameter - 10 mils
Conductivity - 2.13 watts per inch - degrees centigrade

Heat Sink: Material - Copper
Conductivity - 10 watts per inch - degrees centigrade

OHMIC
Metallization: Platinum (1.8 watts per inch - degrees centigrade) 45 degree spread
Titanium (0.45 watt per inch - degrees centigrade) 100 percent dissipation
Gold Header (7.54 watts per inch - degrees centigrade) Pd = 1 Watt

Level	Material	Radius Dimension (inches)	Thermal Resistance (degrees centigrade per watt)	Next Level DIM
Device	Silicon	5.0	3.52	5.67
OHMIC metallization	Platinum	5.67	0.045	5.68
OHMIC metallization	Titanium	5.68	2.19	5.78
OHMIC metallization	Gold	5.78	0.1002	5.86
Heat Sink	Copper	5.86	1.64	--
			θ_{JC} = 7.5	

ΔT_{JC} = 7.5°C

TABLE 25. CIRCULAR SURFACE DEVICE

MATERIAL: SILICON
CONDUCTIVITY: 2.13 (W/IN.*C)
SPREADING ANGLE: 45 (DEGREES)

DIAMETER	THERMAL RESISTANCE	RADIUS(inc)
1	35.1627	0.57
2	17.5813	1.13
3	11.7209	1.70
4	8.7907	2.27
5	7.0325	2.83
6	5.8604	3.40
7	5.0232	3.97
8	4.3953	4.53
9	3.9070	5.10
10	3.5163	5.67
12	2.9302	6.80
14	2.5116	7.93
16	2.1977	9.07
18	1.9535	10.20
20	1.7581	11.33
22	1.5983	12.47
24	1.4651	13.60
26	1.3524	14.73
28	1.2558	15.87
30	1.1721	17.00
32	1.0988	18.13
34	1.0342	19.27
36	0.9767	20.40
38	0.9253	21.53
40	0.8791	22.67
42	0.8372	23.80
44	0.7991	24.93
46	0.7644	26.07
48	0.7326	27.20
50	0.7033	28.33

TABLE 26. CIRCULAR SURFACE METALLIZATION - PLATINUM

MATERIAL: PLATINUM
CONDUCTIVITY: 1.8 (W/IN.*C)
SPREADING ANGLE: 45 (DEGREES)

RADIUS	THERMAL RESISTANCE	RADIUS(inc)
1	1.4035	1.01
2	0.3523	2.01
3	0.1568	3.01
4	0.0882	4.01
5	0.0565	5.01
6	0.0393	6.01
7	0.0288	7.01
8	0.0221	8.01
9	0.0174	9.01
10	0.0141	10.01
12	0.0098	12.01
14	0.0072	14.01
16	0.0055	16.01
18	0.0044	18.01
20	0.0035	20.01
22	0.0029	22.01
24	0.0025	24.01
26	0.0021	26.01
28	0.0018	28.01
30	0.0016	30.01
32	0.0014	32.01
34	0.0012	34.01
36	0.0011	36.01
38	0.0010	38.01
40	0.0009	40.01
42	0.0008	42.01
44	0.0007	44.01
46	0.0007	46.01
48	0.0006	48.01
50	0.0006	50.01

TABLE 27. CIRCULAR SURFACE METALLIZATION - TITANIUM

MATERIAL: TITANIUM
CONDUCTIVITY: .45 (W/IN.*C)
SPREADING ANGLE: 45 (DEGREES)

RADIUS	THERMAL RESISTANCE	RADIUS(inc)
1	63.7199	1.10
2	16.6813	2.10
3	7.5323	3.10
4	4.2711	4.10
5	2.7467	5.10
6	1.9137	6.10
7	1.4092	7.10
8	1.0808	8.10
9	0.8551	9.10
10	0.6934	10.10
12	0.4823	12.10
14	0.3548	14.10
16	0.2719	16.10
18	0.2150	18.10
20	0.1742	20.10
22	0.1440	22.10
24	0.1211	24.10
26	0.1032	26.10
28	0.0890	28.10
30	0.0775	30.10
32	0.0682	32.10
34	0.0604	34.10
36	0.0539	36.10
38	0.0484	38.10
40	0.0437	40.10
42	0.0396	42.10
44	0.0361	44.10
46	0.0330	46.10
48	0.0303	48.10
50	0.0280	50.10

TABLE 28. CIRCULAR SURFACE - GOLD PLATE

MATERIAL: GOLD
CONDUCTIVITY: 7.54 (W/IN.*C)
SPREADING ANGLE: 45 (DEGREES)

RADIUS	THERMAL RESISTANCE	RADIUS(inc)
1	3.0909	1.08
2	0.8021	2.08
3	0.3611	3.08
4	0.2044	4.08
5	0.1313	5.08
6	0.0914	6.08
7	0.0673	7.08
8	0.0516	8.08
9	0.0408	9.08
10	0.0331	10.08
12	0.0230	12.08
14	0.0169	14.08
16	0.0130	16.08
18	0.0102	18.08
20	0.0083	20.08
22	0.0069	22.08
24	0.0058	24.08
26	0.0049	26.08
28	0.0042	28.08
30	0.0037	30.08
32	0.0032	32.08
34	0.0029	34.08
36	0.0026	36.08
38	0.0023	38.08
40	0.0021	40.08
42	0.0019	42.08
44	0.0017	44.08
46	0.0016	46.08
48	0.0014	48.08
50	0.0013	50.08

TABLE 29. CIRCULAR SURFACE HEAT SINK - COPPER

MATERIAL: COPPER
CONDUCTIVITY: 10 (W/IN.*C)
SPREADING ANGLE: 45 (DEGREES)
HEAT SINK THICKNESS: 2.5 (MIL IN.)

RADIUS	THERMAL RESISTANCE	RADIUS(INC)
1	22.7364	3.50
2	8.8419	4.50
3	4.8229	5.50
4	3.0607	6.50
5	2.1221	7.50
6	1.5603	8.50
7	1.1967	9.50
8	0.9474	10.50
9	0.7689	11.50
10	0.6366	12.50
12	0.4573	14.50
14	0.3445	16.50
16	0.2688	18.50
18	0.2157	20.50
20	0.1768	22.50
22	0.1476	24.50
24	0.1251	26.50
26	0.1074	28.50
28	0.0932	30.50
30	0.0816	32.50
32	0.0721	34.50
34	0.0641	36.50
36	0.0574	38.50
38	0.0517	40.50
40	0.0468	42.50
42	0.0426	44.50
44	0.0389	46.50
46	0.0357	48.50
48	0.0328	50.50
50	0.0303	52.50

5.3.4 Hybrid Model

Thermal considerations for hybrid microcircuits have become more important with the advent of high power devices and the increased density of devices on a hybrid substrate. The hybrid model is the concept that lead to the derivation of the square, rectangular, and circular models. The hybrid model provides a rapid and relatively simple approach to predict the maximum temperatures reached in various devices on the hybrid substrate. This model considers the effect of the heat transfer between all device/device and resistor/device combinations, with modifications to allow for both chip resistors and devices on heat spreaders. The model program will not be presented, but the following commentary on the hybrid model provides sufficient information for its derivation and implementation.

The hybrid circuit usually consists of a metal casing or package, which consists of a header and cover. The substrate is attached to the header, and the hybrid circuitry is fabricated on the upper surface of the substrate. The circuitry can consist of thick and thin film resistors, capacitors, inductors, conduction paths, and assorted semiconductor devices.

Most semiconductor devices on the substrate have a defined heat generating region. This region is normally considered to be about 50 percent of the devices' total upper surface area. Resistors also have a heat generating region, but this region is a function of the way they are trimmed (i.e., L shaped, laser or abrasive trimming). Various trimmings are shown in Figure 42. Heat flows through the device or resistor, and substrate and header, to the external header surface. When there is more than one heat dissipating device or resistor on the substrate, there is often a thermal coupling developed between them. When this coupling occurs, the junction temperature of a device rises to a higher temperature than that produced by the device itself. Figure 43 shows a basic thermal resistance model for a device

where

T_J = junction temperature of the device
θ_d = thermal resistance from the device to the center of the substrate
T_S = midsubstrate temperature under the device
T_{CP} = the portion of the substrate temperature due to other devices and resistors
θ_{CS} = the midsubstrate to header thermal resistance
T_C = the header lower surface temperature (ambient)

The temperature source T_{CP} is given by

$$T_{CP}\ 1i = \sum_{\substack{j=1 \\ j \neq i}}^{N} \theta_{ij} P_j \qquad (1)$$

where

θ_{ij} = the coupling thermal resistance from device j to device or resistor i
N = total number of heat dissipating elements on a substrate
P_j = the power dissipation of device j.

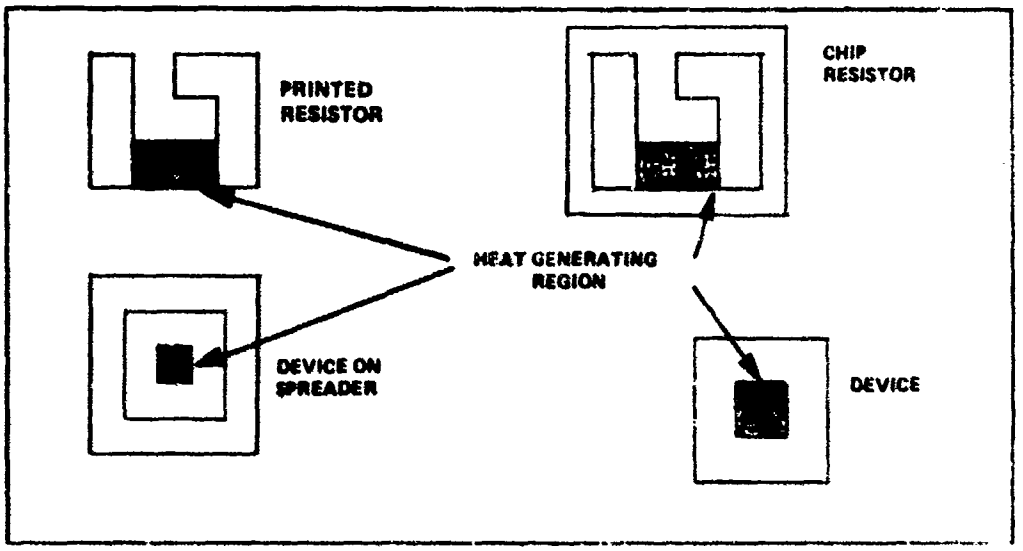


Figure 42. Hybrid Model Heat Generating Regions

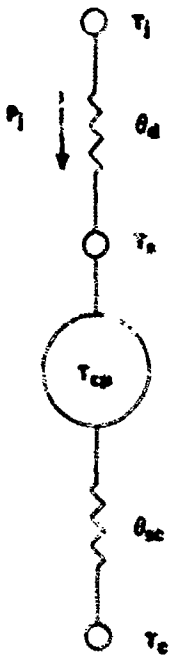


Figure 43. Device

The heat generating temperature, T_{ji}, of device i is given as

$$T_{ji} = Tepli + P_i(\theta_{di} + \theta_{Sci}) + Tc. \quad (2)$$

Two assumptions must be made to be able to derive a closed form solution of the temperature distribution. The first assumption is that rectangular-shaped heat dissipation can be modeled as a circular device with the same base area. The second assumption is that the substrate itself is circular, with a radius R_o that is equal to the distance from the center of the device to the nearest substrate edge. Figure 44 illustrates both assumptions.

The radius of the assumed circular device is given by

$$r_{oi}\sqrt{\frac{Aibi}{\pi}} \quad (3)$$

where ai and bi are the rectangular dimensions. This assumption is valid unless a_i exceeds b_i more than three times. It should be noted that the assumption of a circular substrate with an area less than that of the rectangular substrate will give a conservative answer.

Using the circular models, the temperature distribution is given by the following ordinary differential equations:

$$\frac{d^2T}{dr} \quad \frac{1}{r}\frac{dT}{dr} - \lambda^2 T = 0 \quad (4)$$

where

$$\lambda = \frac{1}{K_s S\left(\frac{S}{2K_s} + \frac{E}{K_E} + \frac{H}{K_H}\right)} \quad (5)$$

where

S = substrate thickness
K_S = substrate conductivity
E = epoxy (under substrate) thickness
K_E = epoxy (under substrate) thermal conductivity
H = header thickness
K = header thermal conductivity.

The equation applies for $r_o \leq r \leq R_o$, with boundary conditions

$T = T_s$ at $r = r_o$

$\frac{dT}{dr} = 0$ at $r \geq R_o$.

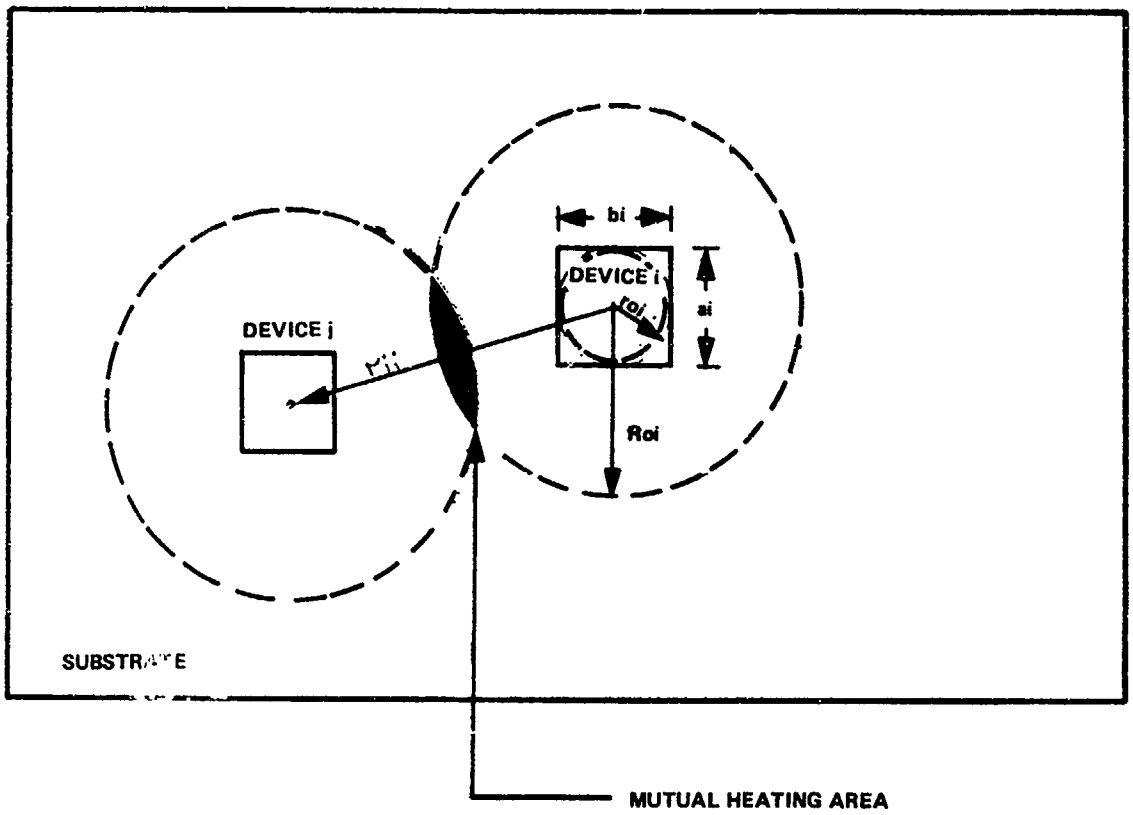


Figure 44. Single/Multiple Device(s)

The solution of equation 4 is

$$T = C_1 I_o(\lambda r) + C_2 K_o(\lambda r). \qquad (6)$$

Evaluating C_1 and C_2 by applying the boundry conditions gives

$$T = \frac{K_1(\lambda R_o) I_o(\lambda_F) + I_1(\lambda R_o) K_o(\lambda_r)}{K_1(R_o) I_o(r_o) + I_1(R_o) K_o(r_o)} \times T_S \qquad (7)$$

where I_o, I_1, K_o, and K_1 are modified Bessels of the 0th and first order. Thus, the midsubstrate temperature is given by equation 7 for $r_o \leq r \leq R_o$ and by T_s for $0 \leq r \leq r_o$.

The heat power for P is given by

$$P = K_s S \lambda^2 \int_{\phi=o}^{2\pi} \int_{r=o}^{R_o} Tr dr d\phi \qquad (8)$$

When integrated, the temperature T, (for $r_o \leq r \leq R_o$) is arrived at in terms of the power dissipation P of the device.

$$= \frac{A(K_1(\lambda R_o)I_o(\lambda r) + I_1(\lambda R_o)K_o(\lambda r))}{K_1(\lambda R_o)\frac{r_o}{2} I_o(\lambda r_o) - \frac{1}{\lambda} I_1(\lambda R_o)\frac{r_o}{2} K_o(\lambda r_o) + \frac{1}{\lambda} K_1(\lambda r_o)} \qquad (9)$$

where

$$A = \frac{1}{2\pi K_s S \lambda^2 r_o}$$

θ_{sc} is calculated by setting $r = r_o$ in equation 9. This is calculated the same way for all devices and resistors on the substrate.

θ_d is calculated by adding the device thermal resistance to the thermal resistance through half the substrates.

$$\theta_d = \theta_{dr} + \frac{S}{2K_s ab} + \frac{V}{K_v ab} + \frac{G}{K_g ab} \qquad (10)$$

where

θ_{dr} = device thermal resistance
V = device epoxy thickness
K_v = conductivity
G = conductor thickness
K_g = conductor conductivity.

The device thermal resistance is calculated by a simple and conservative spreading resistance model. If rectangular heat dissipation region:

$$\theta_{dr} = \frac{1}{2K_d(c-d)} \ln \frac{c}{d} \frac{d+2t}{c+2t} \qquad (11)$$

where

t = thickness of device
c,d = rectangular dimensions of heat generation region
K_d = device thermal conductivity.

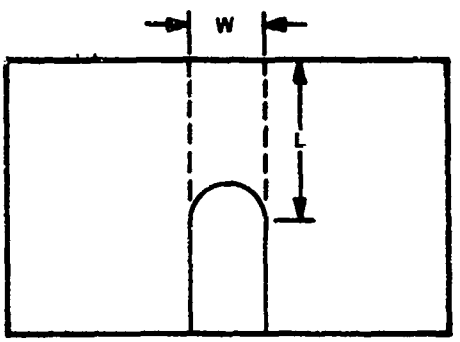
If c = d (square)

$$\theta_{dr} = \frac{t}{(K_d C^2)(1 + \frac{2T}{C})} \qquad (12)$$

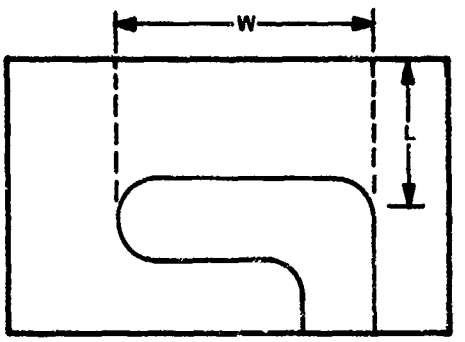
If circular dissipation area, $r = \sqrt{\frac{cd}{\pi}}$

$$\theta_{dr} = \frac{t}{Kdr(r+t)} \cdot \qquad (13)$$

Trimmed resistors experience rather high surface temperatures. The majority of this temperature is dissipated across the length of the cut and the remaining width of the resistor.



LASER OR ABRASIVE



L SHAPE

If the resistor is a chip resistor, (typically a resistor printed on a small rectangular substrate material), the dissipation area should be calculated. Then the chip can be treated as a device for all other purposes. The thermal resistance to midsubstrate now would be

$$\theta_d = \theta_{chip} + 1/2\theta_{substrate} + \theta_{epoxy} + \theta_{conductor} \qquad (14)$$

If printed directly on the substrate, $\theta_{chip} = \theta_{epoxy} = 0$.

To account for a heat spreader, the heat generating region of the device is projected to the top of the spreader using the appropriate spreading resistance model. Figure 45 shows this principle.

The spreader is then treated as a device with the projected heat generating region. Its thermal resistance to midsubstrate is

$$\theta_d = \theta_{dr} + \theta_{spreader} + 1/2\theta_{substrate} + \theta_{epoxy} + \theta_{conductor}. \qquad (15)$$

If the chip is not eutectically bonded to the spreader, an additional epoxy must be added.

5.4 External Model

Analytical external thermal models have been designed for the six selected packages (side-brazed dip, ceramic chip carrier, cerdip, flatpack, hybrid, axial stud). The models were designed to relate the case temperature measurement (selected measurement point) with the junction temperature for verification. These models are represented as nodal thermal equations, with each model considering the measurement point, the type of cooling, and the external environments.

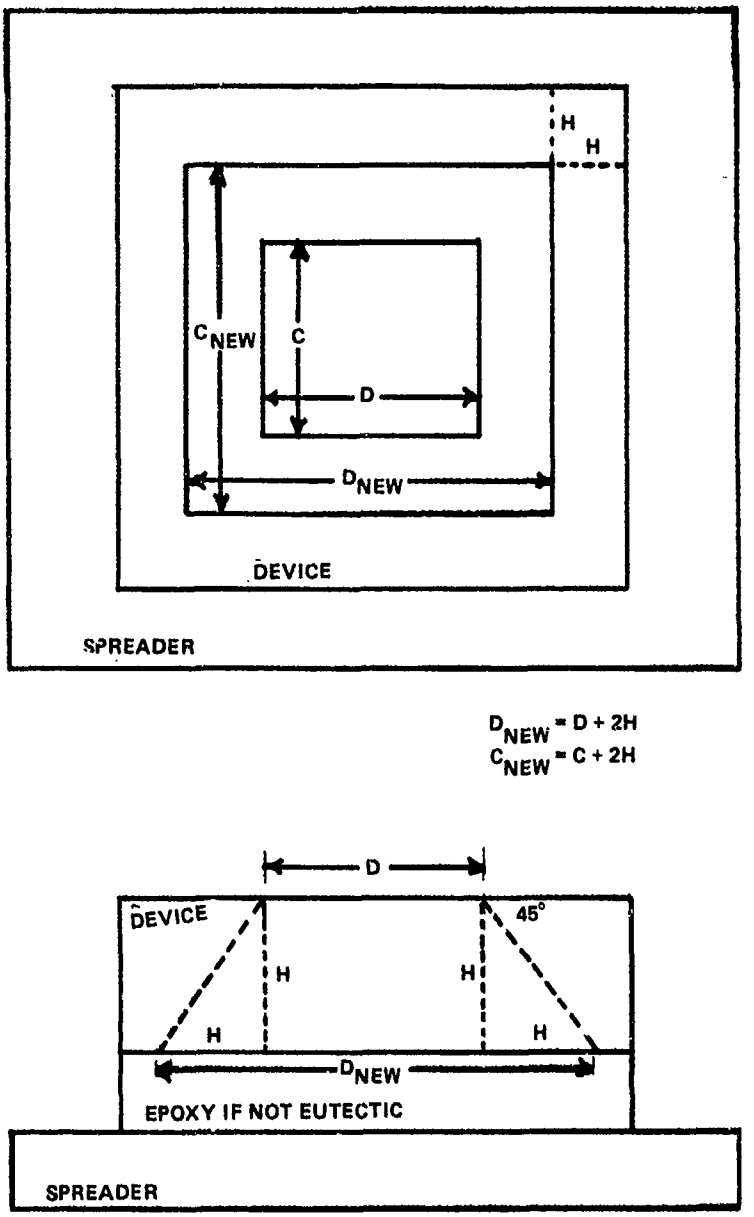


Figure 45.

The major consideration in model design is the identification of a measurement point that is accessible and thermally related to the junction temperature. The measurement point location has been defined as the geometric center of the device for all packages where the center is an accessible point.

The selection of the geometric top center was based on several major considerations. The center of the top may not be the peak temperature point of the device top, but access to the top is generally the most convenient and very easily definable. From an engineering standpoint, the conductivity of the lid is extremely high compared to the rest of the package. The thermal drop across the lid is small in relation to the total thermal resistance from junction to the measurement point (lid center).

The geometric top center of the device is not an accessible measurement point for microwave devices because they are predominately stud mounted inside a cavity. This positioning presents many complications in measuring microwave devices directly. However, before the device is mounted into an operating system, a thermocouple can be attached to the ceramic ring near the bottom of the heat source. There is a much better conduction path through the bottom than through the top. For these reasons, the bottom has been selected as the measurement point for axial studded packages.

There are three predominant types of cooling to be considered for the external model. They are 1) conduction, 2) convection, and 3) radiation. Each cooling method is addressed in the following paragraphs.

Conduction

The basic approach to conduction heat transfer is the use of the standard heat transfer equation

$$Q_k = \theta_k \ \Delta T$$

where

Q_k = heat flow rate; degrees centigrade per watt
$\theta_k = \frac{L}{K\,A}$ = conductive thermal resistance
L = length of flow path
K = material thermal conductivity
A = heat flow area
ΔT = temperature difference.

The values for thermal conductivity (k) to be used are shown in Table 30. These values are shown at a particular temperature, since thermal conductivity varies with temperature.

Convection

The basic approach to convection heat transfer is the use of the standard heat transfer equation

$$Q_h = \theta_h \ (T_S - T_F)$$

where

Q_h = heat flow rate; degrees centigrade per watt
$\theta_h = \frac{1}{L\ A}$ = convection thermal resistance
θ_h = heat transfer coefficient
T_S = surface temperature
T_F = temperature of surrounding fluid, such as ambient air
L = length of flow path
A = heat flow area.

The heat transfer coefficients (θ_h) to be used are shown in Table 31.

TABLE 30. THERMAL CONDUCTIVITY OF TYPICAL MATERIALS

Materials	Thermal Conductivity (watts per inch - degrees centigrade)
Air	0.00066
Alumina (96 percent)	0.478
(90 percent)	0.339
Aluminum	5.52
Beryllia	4.1
Copper	9.66
Diamond	9.0
Epoxy (conductive)	0.051
(non-conductive)	
Ablefilm-550-1	0.0079
Ablebond-450	0.0091
Eutectic (gold-silicon)	4.5
Fiberglass	0.00122
Galium Arsenide	
Glass (CV-111)	0.025
(7583)	0.029
(KC-1)	0.034
Gold	7.54
Gold (Glass Dieattach)	0.255
Kovar	0.419
Molybdenum	3.7084
Molytab	3.9
Plastic (polystrene)	0.00381
Plastic foam	0.0043 - 0.0035
Platinum	1.77
Silicon	2.13
Silver	10.61
Stainless Steel	0.4318
Steel	1.2192
Tin	0.44604
Titanium	0.45
Water	0.0153

TABLE 31. CONVECTION HEAT TRANSFER COEFFICIENT

Cooling Technique	Heat Transfer Coefficient θ_h (watts per square inch-degrees-centigrade)
Free Convection (Horizontal Surface)	0.00181 - 0.00368
High altitudes [21,336 meters (70,000 feet)]	0.00181
Sea level	0.00368
Forced air (20 CFM)	0.0109 - 0.0181
Forced convection	
Air over plain fins	0.0219 - 0.10967
Air over interrupted fins	3 to 5 times higher than plain fins
Liquid Cooling	
Dielectric liquid	0.36774 - 1.4645
Water	1.8064 - 36.774

Radiation

Radiation heat transfer is the most complex method to be investigated. The same basic approach is used with the standard heat transfer equation

$$Q_R = \sigma f_R F_{ES} A (T_E^4 - T_S^4)$$

where

Q_R = heat flow rate; degrees centigrade per watt
σ = Stefan-Boltzmann constant (air = 0.37 pounds of force-feet cubed per pounds of mass-square inches-degrees Rankin)
f_R = relative emissivity between the surface and the surroundings approximately equal to the product of both emissivities
F_{ES} = view factor between the part and the surroundings
A = radiating area
T_E = absolute temperature of radiating surface
T_S = absolute temperature of surroundings.

The view factor is the measure of how well the emitter sees the absorber. It is a value between 0 and 1. Typical values are given in Table 32. The emissivity also varies between 0 and 1. A perfect black body has an emissivity equal to 1, while a perfectly shiny body has an emissivity of 0. The emissivity of typical metals and non-metallic materials is given in Table 33.

TABLE 32. VIEW FACTORS FOR VARIOUS CONFIGURATIONS

Configuration	View Factor
Infinite parallel planes	1.0
Body completely enclosed by another body; internal body cannot see any part of itself	1.0
Two squares in perpendicular planes with a common side	0.20
Two equal, parallel squares separated by distance equal to side	0.19
Two equal, parallel circular disks separated by distance equal to diameter	0.18

TABLE 33. EMISSIVITY OF TYPICAL SURFACES

Surface	Emissivity (ϵ)
Silver	0.02
Aluminum (buffed)	0.03
Aluminum foil (dull)	0.03
Gold (plated)	0.03
Gold (vacuum deposited)	0.03
Aluminum foil (shiny)	0.04
Aluminum (polished)	0.05
Stainless steel (polished)	0.05
Chrome	0.08
Tantalum	0.08
Beryllium (polished)	0.09
Beryllium (milled)	0.11
Rene 41	0.11
Nickel	0.18
Titanium	0.20
Aluminum (sandblasted)	0.40
White silicone paint (gloss)	0.75
Black silicone paint (flat)	0.81
Black vinyl phenolic (dull)	0.84
Lamp black	0.95
Magnesia	0.95
Grey silicon paint	0.96
Silicon	0.64
Alumina (Al_2O_3)	0.30

External Environments

The considerations for external environments are shown in Figure 46. The package represented in Figure 46 is the cofired side-brazed package, D5, for which measurements have been made. The package measured data is discussed in appendix 7. The external environments have already been addressed in the type of cooling discussion. The environments are conduction, convection, and radiation. For the external area, cooling must be applied and considered with forced air, still air (free air), heat sinks, insulators, pins, and printed circuit boards.

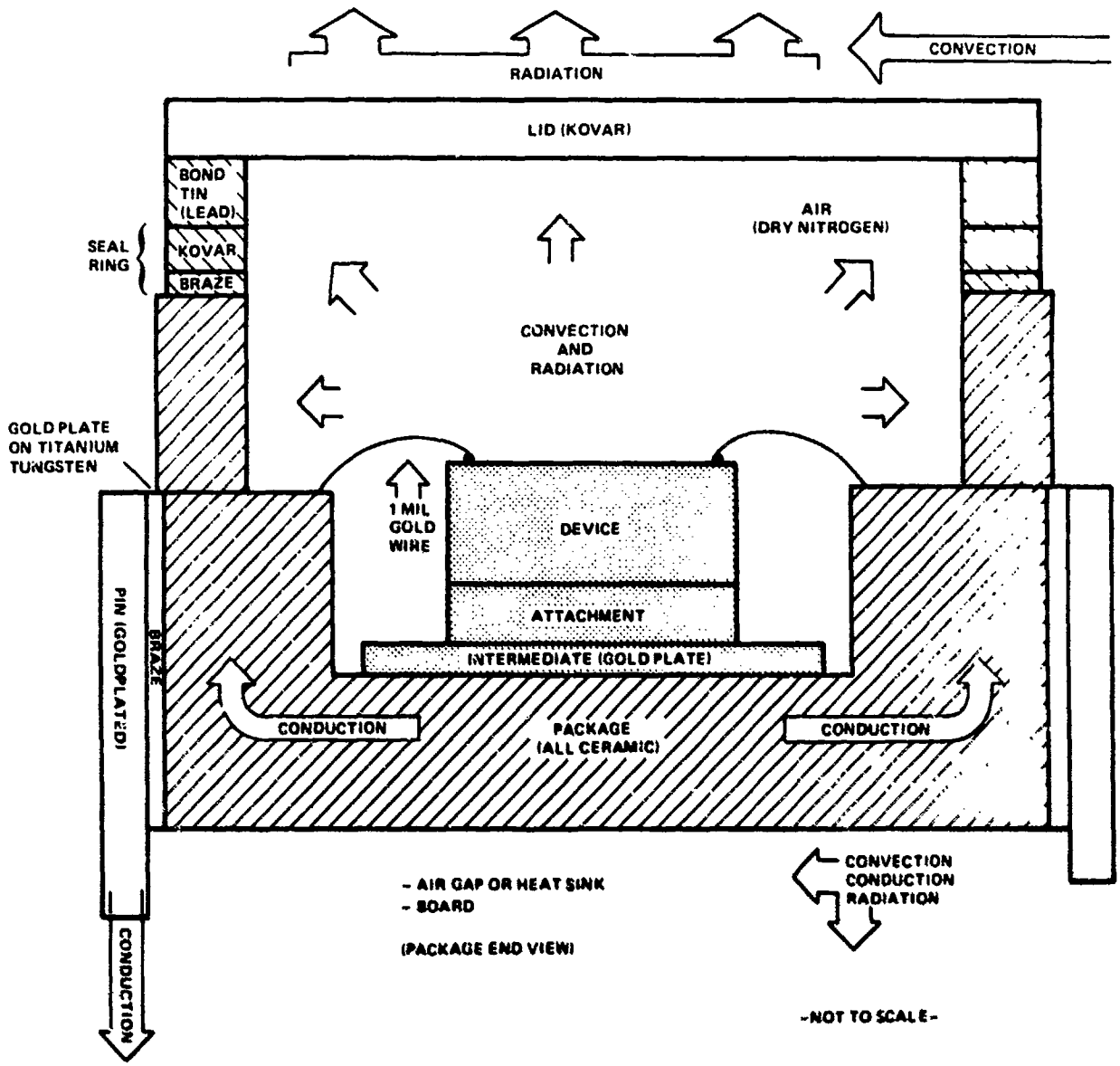


Figure 46.

5.4.1 Nodal Programs

Nodal programs that model all six of the specified package types have been developed. Their purpose was to establish a relationship between the junction temperature and the measurement point. These programs solve a network analysis in a way similar to that of the SINDA computer program. The nodal programs also are based on the same modeling techniques as the SINDA computer program. The techniques used to model these packages involved separating them into integral parts and then establishing the applicable dimensions and nodes.

The external model is nodal, which solved a network analysis. The number of nodal regions in the packages are divided in a range from nine to sixteen. Four of the nodes were designated as boundary or source conditions, while one was designated as the selected measurement point. The number of nodes were kept to a minimum in order to keep the costs of the analysis within the program constraints.

Several inputs were required to use the model. The inputs were referred to as the boundary or source conditions. The specific boundaries required were the ambient air, radiation sink, circuit board, and junction temperatures. Supplying all these condition in degrees centigrade resulted in the nodal model predicting the temperatures of the other nodal regions.

The nodal model can also be used to predict the junction temperature by supplying the first three boundary conditions (ambient air, radiation sink, and circuit board temperatures), and the source (amount of power applied) of the junction temperature in watts.

Table 34 illustrates the inputs (boundaries and source) required for the nodal model conditions. Using the model in these two formats results in output data that is highly comparable. This comparability will be discussed in the next section, external model correlation.

The materials used in the packaging were considered in the modeling process, since the flow of heat depends on the conductivity of these materials. Taking these factors (node location dimensions, and material conductivity) into consideration, conduction calculations were developed and the nodal programs implemented. The nodal programs will not be provided, however. The conduction calculations, package diagrams, and node descriptions presented in appendix 6 can directly be used in the derivation of nodal programs.

The side-brazed model was exercised considerably to assess the impact of the boundary conditions on the temperature of the various nodes of interest. As indicated by Figures 47 and 48, the ambient air and the radiation sink do not appear to have a significant impact on the temperatures of the other nodes when the board temperature was kept constant. Maintaining the board temperature constant created, in effect, an ultimate heat sink. There is a temperature delta of only 2 to 5°C as the variable temperature changes from 25 to 130°C for all except board temperature. The main temperature driver was found to be the circuit board, based on the

TABLE 34. EXTERNAL MODEL INPUTS

Model Conditions	Boundaries (Temperature)				Source (Power)
	Ambient Air	Radiation Sink	Board	Junction	Junction
Predicted Junction Predicted Measurement Point	X	X	X		X
Measured Junction Predicted Measurement Point	X	X	X	X	

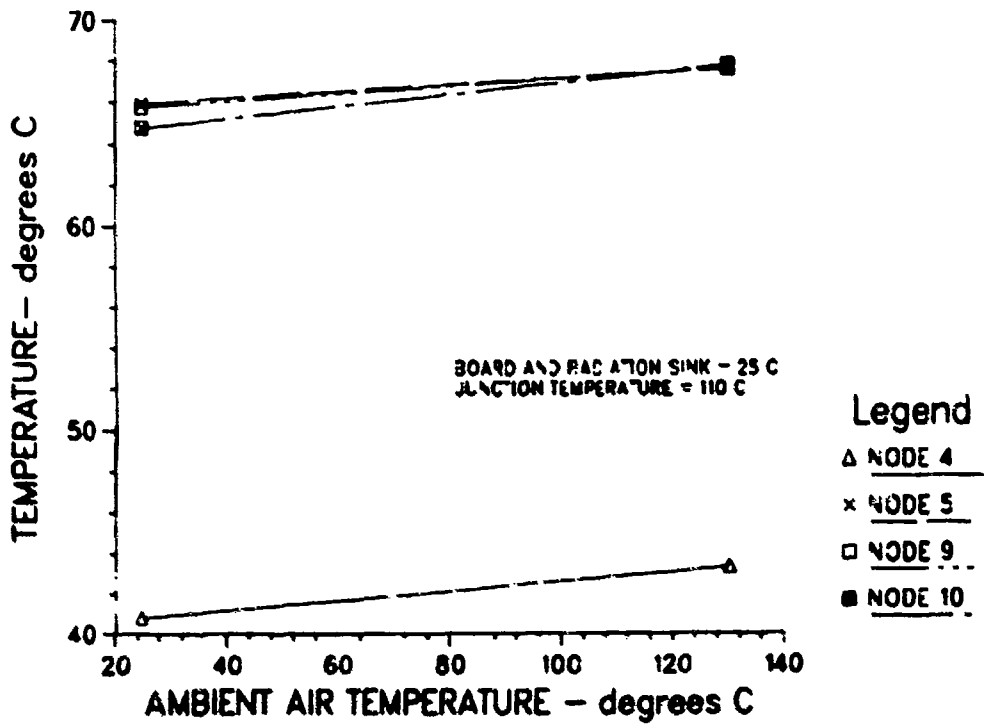


Figure 47. Ambient Air Impact on Package Nodes

evidence presented in Figure 49. As the temperature of the board increases, the node temperatures increase linearly with an approximate temperature delta of 42°C as the board temperature varies from 25 to 130°C.

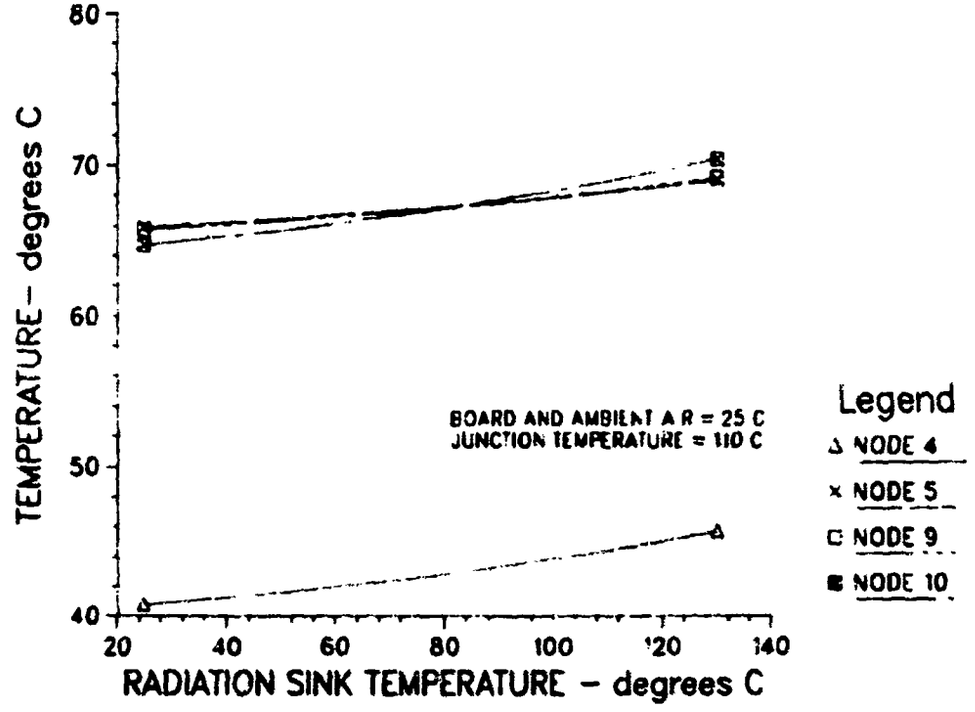


Figure 48. Radiation Sink Temperature on Package Nodes

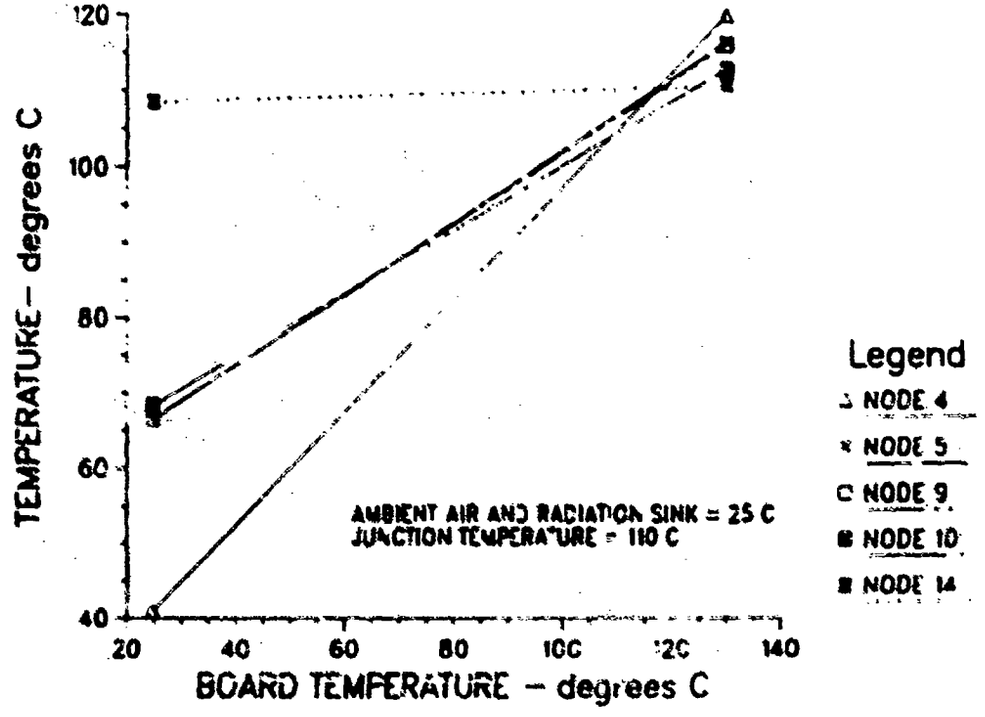


Figure 49. Figure 49. Board Temperature Impact on Package Nodes

The primary objective in developing the external models was to relate the measurement point temperature back to the junction temperature, in a format that allows a quick and easy verification that derating has occurred. This has been accomplished through a graphic representation of the relationship between the junction temperature and the measurement point temperature for each of the six package types. These package curves, discussed in section 5.4.3, Package Derating Curves, are applicable only under certain conditions. These conditions are defined in appendix 6 under the respective package types. The limiting conditions of appendix 6 for the packages are: package size, pin quantity, materials, and dimensions. These conditions, if not acceptable for a specific set of requirements, may be modified by making changes to the conduction calculations (appendix 6).

5.4.2 External Model Correlation

Correlation of the external model was necessary to substantiate study results. Test measurements were performed on a group of seven 40-pin side-brazed ceramic packages, with power transistors connected as the active chips. There were temperature measurement points on the package: lid (center), center lead, and end lead. The base resistor of each sample was adjusted so that all packages were dissipating about the same power. The main supply collection voltage was then adjusted to vary the power of all the test packages. Both free air and circuit board environments were measured at varying power levels. The results, conditions, test set-ups, etc. of the correlation tests are in appendix 7.1.

In addition to the measurements made on the side-brazed package, data extracted from the Martin Marietta Ceramic Chip Carrier Test Report was used for verifying the ceramic chip carrier external model. The test was conducted with two 48-pad carriers at four power levels. The test module description, procedures, measurements, layout, and thermocouple location are shown for the Ceramic Chip Carrier Test in Appendix 7.2. Nodal programs were developed to model the conditions set forth in both the side-brazed and ceramic chip carrier data so a direct correlation could be made.

The correlation of the side-brazed package nodal model, with the actual measured data for the junction, lid, and center lead temperatures, is illustrated in Figure 50. The predicted and measured temperatures in this figure represent average values. Each computer iteration involved specifying an ambient air and radiation sink temperature of 25°C, the measured board temperature, and the measured power level. It was observed that the predicted temperatures were higher in all cases, indicating that the model represents worse case results. The largest temperature differences observed between the predicted and measured values for the junction, lid, and center lead were 3.62, 4.25, and 5.34°C, respectively. The models' prediction of the lid temperature was better than that for the center lead by approximately 1°C. Based on these observations, it was concluded that the model's prediction of the values for the junction, lid, and center lead correlated with the measured results at equivalent power dissipation levels.

To show the effect of power on the measurement point in both the side brazed-package model and the actual measurements, Figures 51 and 52 were

plotted, using both the lid and center lead as possible requirement points. In these curves, both the predicted and measured temperatures represent average values. The model tracks closely with the measured values. Once again, the predicted values were higher (in most cases) than the measured values, resulting in a worst case prediction. The largest variation between the predicted and measured values occurred while using the lid as the measurement point (Figure 51). The variation occurred at 2 watts, and was 2.19°C. The resulting slope of the predicted line is 5.52 degrees, per watt, indicating that the power does have an impact on the lid as a measurement point.

Figure 52 employs the center lead as the measurement point, resulting in data comparable to that in Figure 51. The predicted temperature tracked closely with the measured temperature, with the largest delta (2.47°C) occurring at 2 watts. The power also impacts the center lead as a measurement point, as indicated by the slope of the predicted line (7.36 degrees).

Several conclusions can be made, based on data in Figures 51 and 52. First of all, the power does have an effect on the measurement point in both the model and the measurement data. This conclusion is illustrated by the positively increasing slopes in the figures. Secondly, the power impact is much less on the lid than on the center lead. This conclusion is based on the comparison of the two slope values for the lid and center lead. The slope for the lid is the smallest of the two. The model prediction tracks more closely with the measured results using the lid, as opposed to the center lead, as the measurement point.

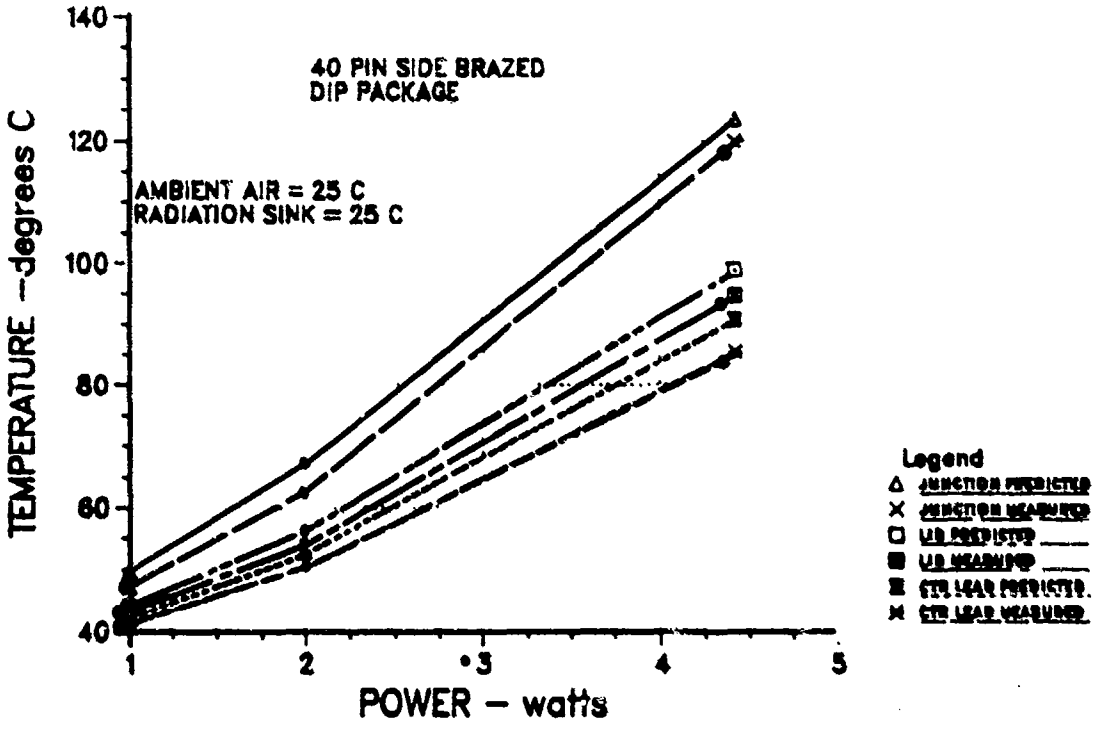


Figure 50. External Model Correlation with Board Measurement Test (• Measurement Point)

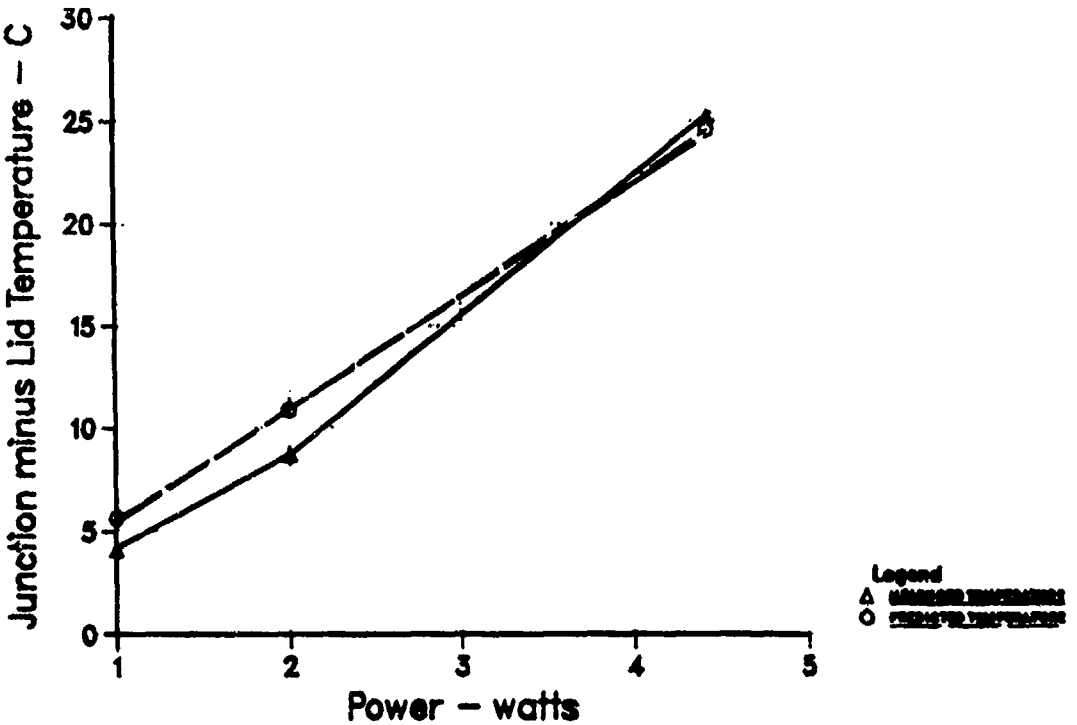


Figure 51. Junction minus Lid Temperature versus Power

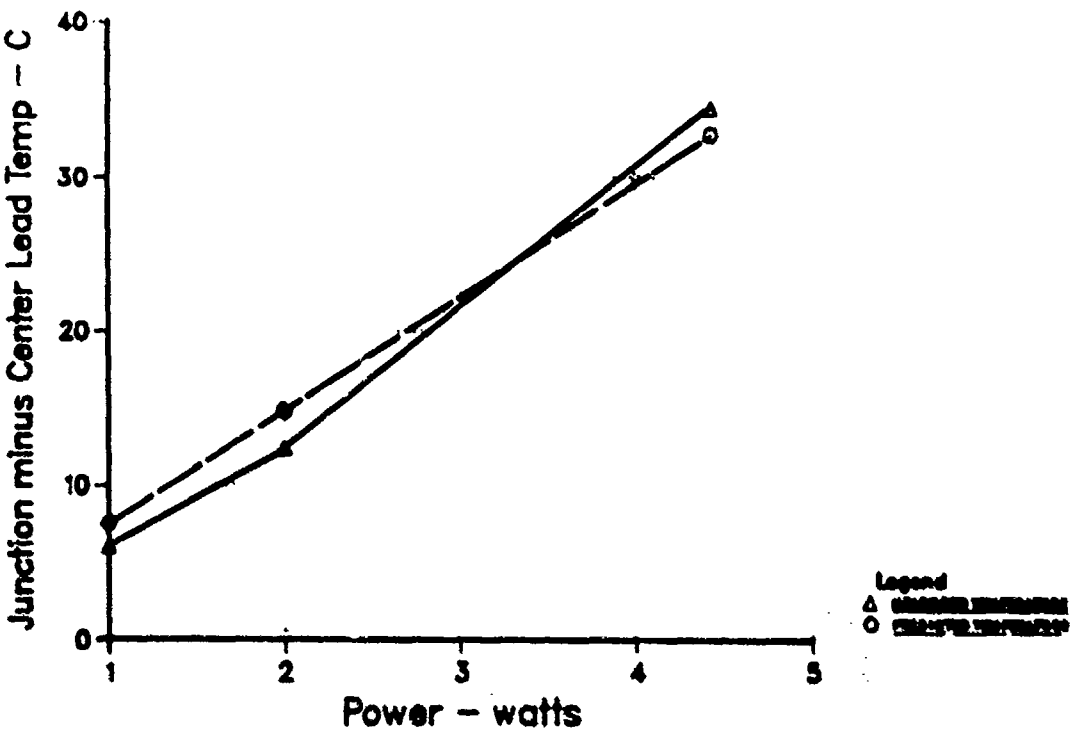


Figure 52. Junction minus Center Lead Temperature versus Power - Measured and Predicted 40 Pin Side Brazed Package

Since the above dissertation concluded that the power has an impact on the measurement point, the two methods of using the model were investigated as to their impact on the resulting derating curves. Figures 53 and 54 show the effect of using the model with four boundaries or three boundaries. Four boundaries involved supplying the ambient air, radiation sink, circuit board and junction temperatures. Three boundaries involved supplying the ambient air, radiation sink, and circuit board temperatures, along with the power supplied in watts.

The legend in the two figures identifies measured and predicted temperatures. That is, the four boundry conditions were inputted to the model for the measured juntion temperature curve, and three boundry conditions were inputted to the model for the predicted curve. For the predicted curve the power was also inputted and the model computes the junction temperature. Figure 53 plots the lid versus junction temperature, and illustrates an excellent correlation between the two model variations, with the predicted values representing worst case results.

Figure 54 plots the center lead versus junction temperature, and illustrates a larger distinction between the two model variations. However, the model does track closely with the measured temperatures. It was concluded that by inputting the power directly to the model, there is minimal impact on the resulting derating curves. It was also decided that the model can be used in both capacities, regardless of power, for the determination of junction temperature derating.

The ceramic chip carrier nodal model was designed based on a 48-pad carrier. In order to correlate the model results with the ceramic chip carrier test report, the data on the 48-pad carrier was extracted from the report and summarized in Table 35. As indicated in the table, two chips were subjected to four power levels, ranging from 0.27 watt to 1.1 watts. Measurements were taken at three locations (base, solder pads, and lid) and theta values computed.

According to the carrier test report, the ambient air and radiation were 90°C. The board temperature was assumed to be the solder pad temperature. This data, along with the power, was used as input into the ceramic chip carrier model.

The results were then compared to the test data illustrated in Table 36. The predicted lid temperature (on the average) was within one-half degree centigrade of the measured temperature. The predicted junction temperature (on the average) was within two degrees centigrade of the measured temperature. Based on these results, it was concluded that an excellent correlation between the model and the test data exists for the ceramic chip carrier.

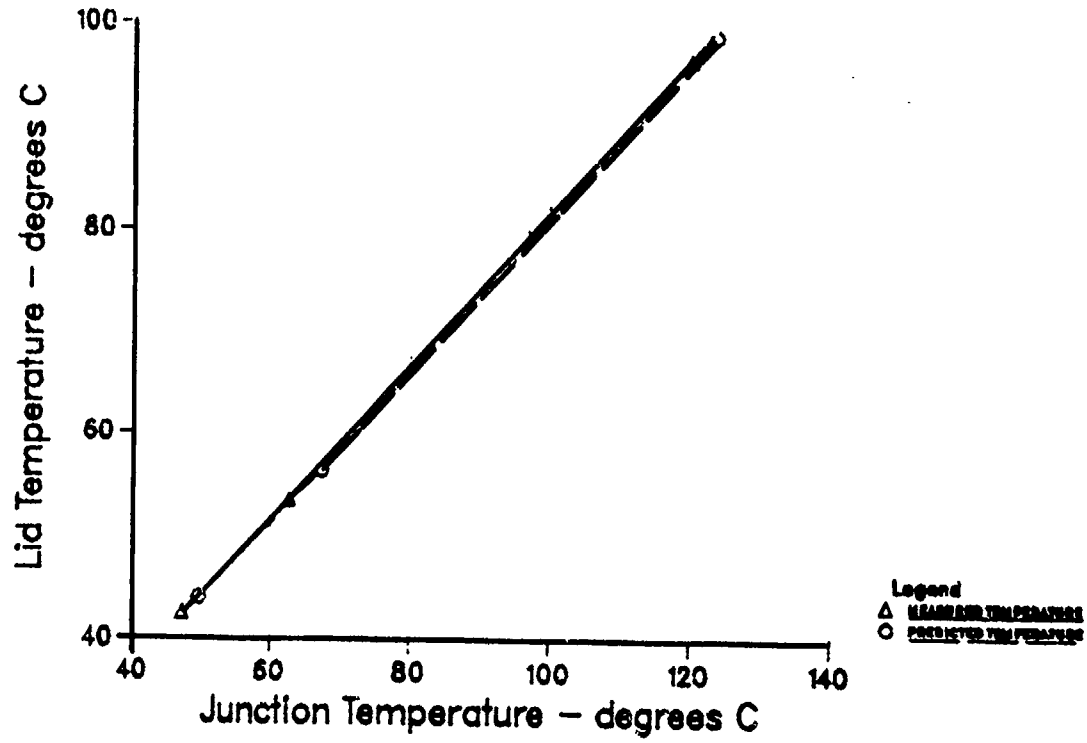


Figure 53. Predicted Junction and Lid Comparison to Measured Junction and Predicted Lid Temperature
40 Pin Side Brazed Package

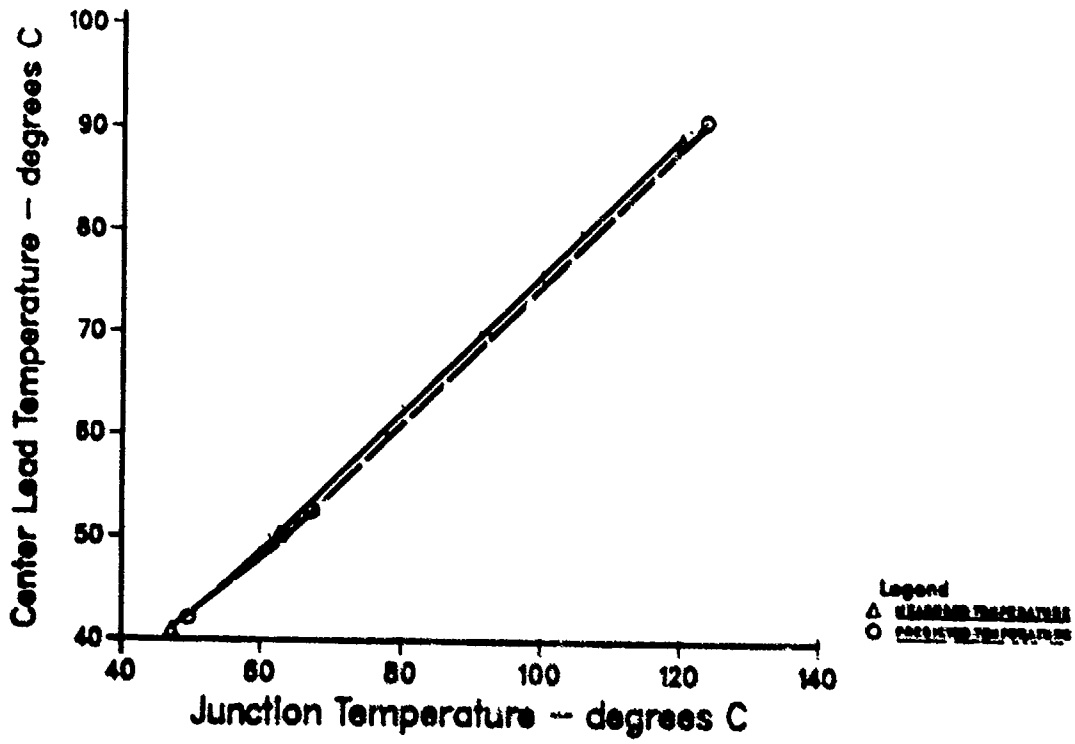


Figure 54. Junction and Center Lead Predicted Temperature Comparison to Measured Junction and Predicted Center Lead Temperature – 40 Pin Side Brazed Package
40 Pin Side

TABLE 35. CERAMIC CHIP CARRIER TEST REPORT AND 48-PAD TEST DATA SUMMARY

Test	Sample	*Power	Package Base			Solder Pads			Package Lid		
			TJ	Base Temperature	Theta	TJ	Pad Temperature	Theta	TJ	Lid Temperature	Theta
1	2	0.27	94.00	92.40	5.984						
	1	0.27				94.31	89.60	16.495			
	2	0.27				94.00	90.10	14.586			
	1	0.27							94.31	92.60	6.396
	2	0.27							94.00	89.10	18.326
2	1	0.54	103.68	92.90	20.044						
	2	0.54	103.27	100.40	5.336						
	1	0.54				103.68	95.80	14.652			
	2	0.54				103.27	96.00	13.516			
	1	0.54							103.68	100.10	6.657
	2	0.54							103.27	93.30	18.535
3	1	0.8	114.27	98.40	19.757						
	2	0.8	113.59	108.60	6.235						
	1	0.8				114.27	102.60	14.529			
	2	0.8				113.59	102.90	13.357			
	1	0.8							114.27	108.10	7.681
	2	0.8							113.59	98.60	18.730
4	1	1.1	127.17	106.30	19.574						
	2	1.1	126.26	119.90	5.968						
	1	1.1				127.17	117.70	14.509			
	2	1.1				126.26	112.20	13.194			
	1	1.1							127.17	119.60	7.100
	2	1.1							126.26	107.00	18.074

*Inputs Into the C^3 Model

TABLE 36. CERAMIC CHIP CARRIER TEST DATA VERSUS MODEL

	Temperature (Degrees Centigrade)					
	Sample Number	Power (watts)	T_j	Solder Pads*	Package Lid	Package Base
Test Data	1	0.27	94.31	89.90	92.6	-
	2	0.27	94.00	90.10	89.10	92.4
	1	0.54	103.68	95.80	100.10	92.9
	2	0.54	103.27	96.00	93.30	100.40
	1	0.8	114.27	102.60	108.10	98.40
	2	0.8	113.59	102.90	98.60	108.60
	1	1.1	127.17	117.70	119.60	106.30
	2	1.1	126.26	112.20	107.00	119.90
Model Output	1	0.27	92.94	89.90	90.08	92.45
	2	0.27	93.14	90.10	90.28	92.65
	1	0.54	101.89	95.80	96.18	100.90
	2	0.54	102.09	96.00	96.38	101.10
	1	0.8	111.62	102.60	103.17	110.16
	2	0.8	111.92	102.90	103.47	110.46
	1	1.1	124.10	117.70	112.48	112.09
	2	1.1	124.60	112.20	112.98	112.59

*Solder pad temperatures used as an input into the model
o Individual test data points were input into the C^3 model
- Ambient air and radiation sink = 80 degrees centigrade
- Measured solder pad temperatures
- Measured power

5.4.3 Package Derating Curves

The derating curves developed for the six package types (side-brazed, ceramic chip carrier, cerdip, flatpack, hybrid and axial stud) are the end result of the external nodal models. They show the relationship between the junction temperature and the selected measurement point. The curves are to be used in verifying junction temperature derating for existing devices, based on the temperature of the measurement point. For new technology devices that will be housed in the same package types, curves were generated to show the relationship between the base temperature and the measurement point temperature. It should be noted, however, that the packages have been modeled assuming specific chip sizes. These chip sizes are discussed in respective sections in appendix 6. Any other curves generated will vary, based on the size of the chip. Additional limiting assumptions of appendix 6 for the packages, are: single package size, pin quantity, materials, one cooling environment, and single heat output.

Three curves were generated for each package type based on board temperatures of 25, 55, and 85°C. A tolerance band was created for these curves by changing the ambient air and radiation sink from 25 to 85°C. This was done to account for the model's boundary conditions. The desired temperatures should fall within the tolerance band, permitting the verification of derating. Interpolation can be performed due to the linear relationship in the band.

The accuracy of two of the models (side-brazed and ceramic chip carrier) was proven by the correlation of the model output with measured test data. The assumptions, rationale, and design used in developing these two models were used in the development of the other models. Therefore the same accuracy is expected, but cannot be verified, due to the lack of test

data for these package types. The exception to the accuracy expectations will be the hybrid model. The large quantity of variables and the complexities in hybrid design would render the unverified hybrid model a best estimate.

5.4.3.1 Side-Brazed Package

The derating curves generated for the side-brazed package can be used if the ambient air, radiation sink, board, and lid temperatures are known. To obtain the board temperature, a measurement must be taken on the bottom side of the board directly under the device. Figure 55 can be used to determine the related junction temperature, and establish whether derating has been implemented. The curves are applicable only when used in conjunction with the specifications and assumptions described in appendix 6.1, Side-Brazed Package. The assumptions are based on the package being a 40 pin side brazed package with specific package, attachment, and chip (device) dimensions. The nodal conduction equations are written for these specific dimensions and materials. The assumptions can be changed to apply to certain specifications by modifying the conduction calculations (also in appendix 6.1).

Figure 56 should be used for new technology devices to establish the proper relationship between the base and lid temperatures. The curves in Figure 56 represent a typical 40-pin package with all internal leads connected.

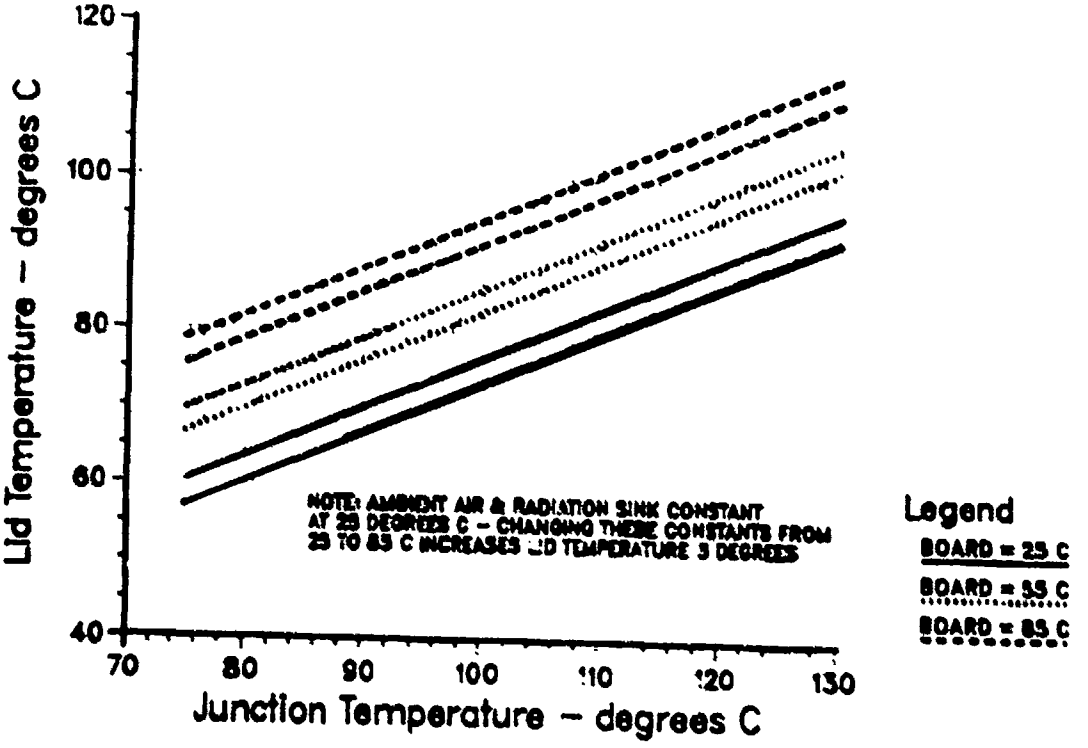


Figure 55. Junction Versus Lid Temperature - Predicted 40 Pin Sized Braxed Package

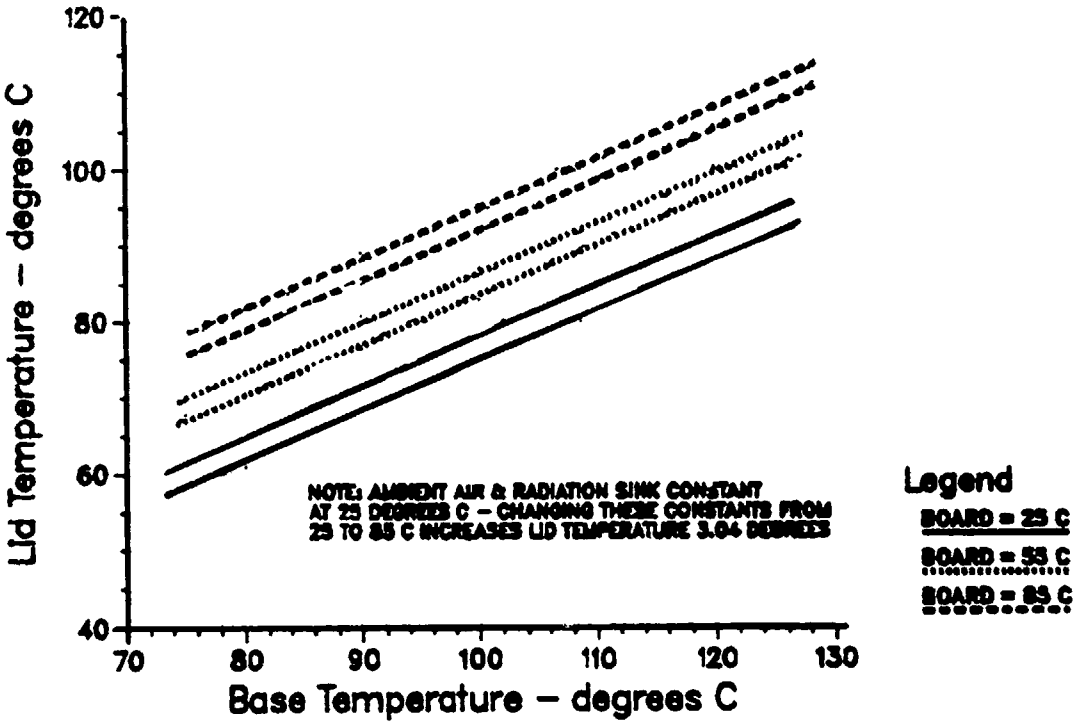


Figure 56. Lid versus Base Temperature - Predicted 40 Pin Side Brazed Package

5.4.3.2 Ceramic Chip Carrier

The derating curves for the ceramic chip carrier are shown in Figures 57 and 58. The junction versus lid temperature curves (Figure 57) are to be used for existing devices. The base versus lid temperature curves (Figure 58) are to be used for new technology devices, or where this relationship needs to be established. The assumptions and specifications made when developing this model are presented in appendix 6.2, Ceramic Chip Carrier, and can be modified according to need. The nodal conduction equations are based on specific material and package and device dimensions. It should be noted that the solder pad temperature is substituted for the board temperature in this model. This assumption was made based on the fact that there are no leads going through the board, and that the thermal gradients (if any) through the board are ignored.

5.4.3.3 Cerdip Package

Figures 59 and 60 represent the derating curves for the cerdip package. The assumptions and specifications used in modeling this package are in appendix 6.3. Applicability of the curves in Figures 59 and 60 are dependent upon these assumptions, along with knowledge of the ambient air, radiation sink, board, and lid temperatures. The nodal conduction equations are based on specific materials and package and device dimensions. The board temperature measurement location is specified as being on the bottom side of the board directly under the device.

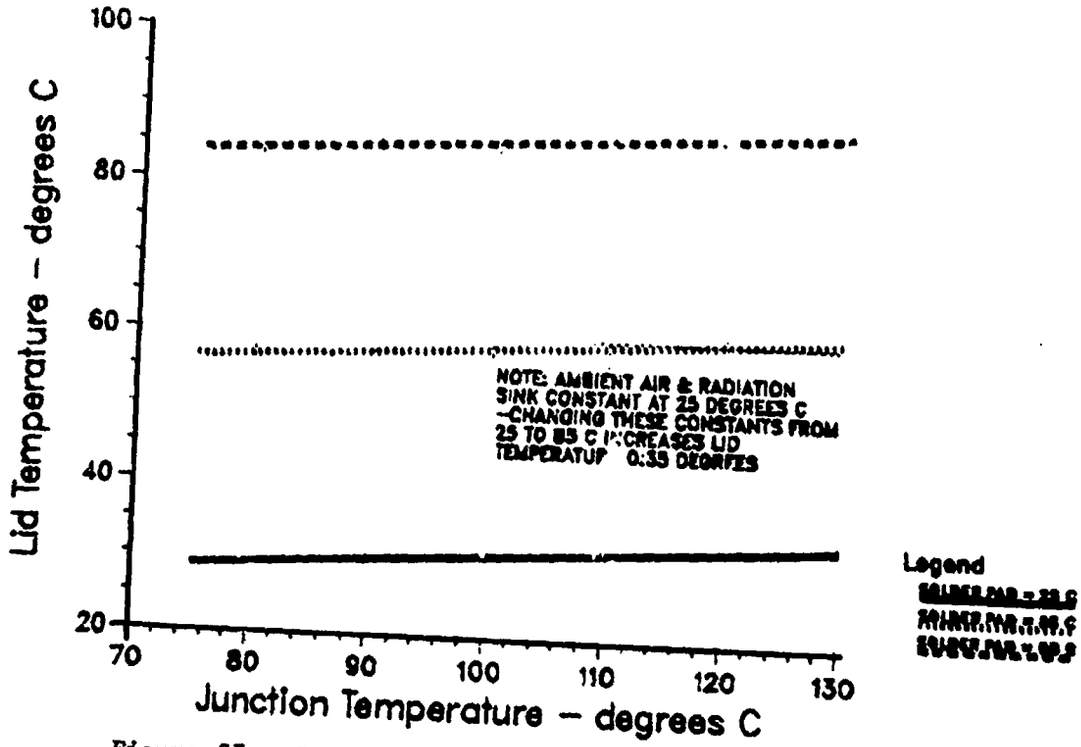


Figure 57. Junction Versus Lid Temperature - Predicted Ceramic Chip Carrier Package

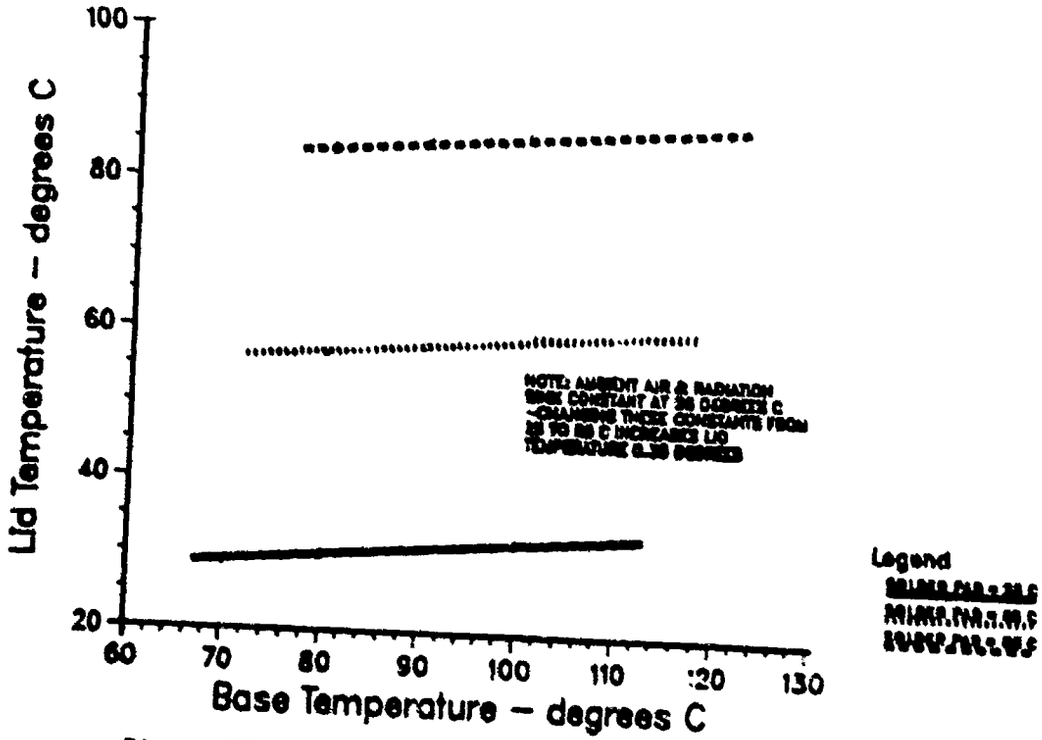


Figure 58. Lid versus Base Temperature - Predicted Ceramic Chip Carrier Package

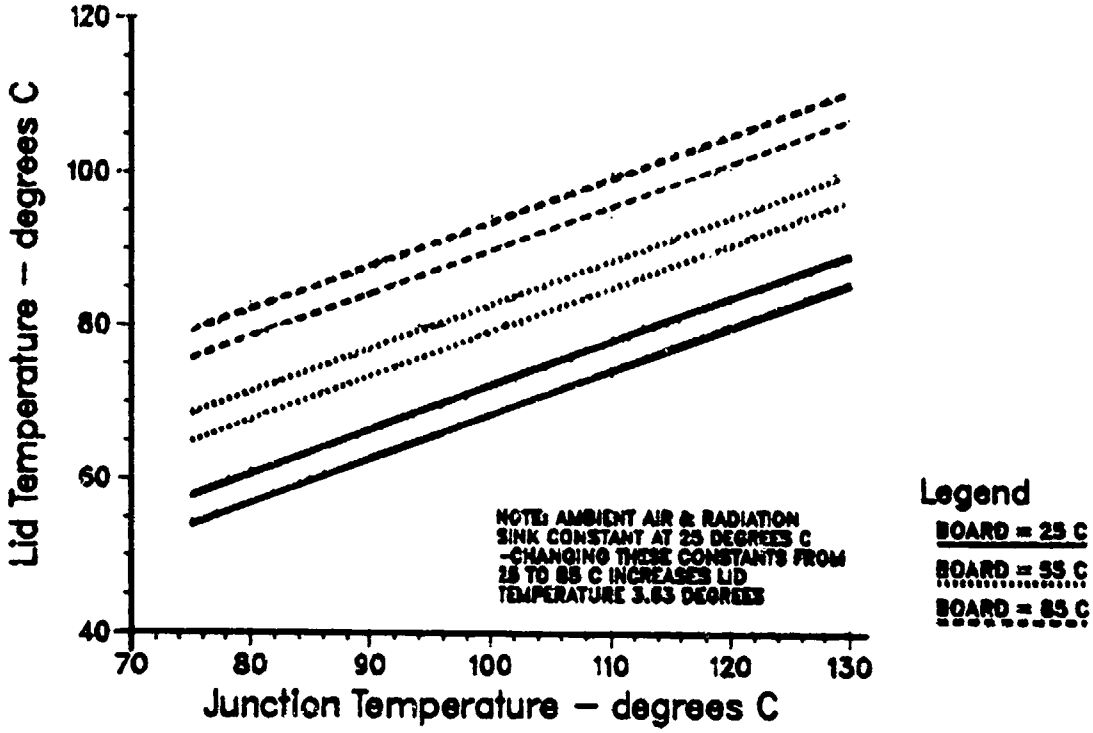


Figure 59. Junction versus Lid Temperature - Predicted Cerdip Package

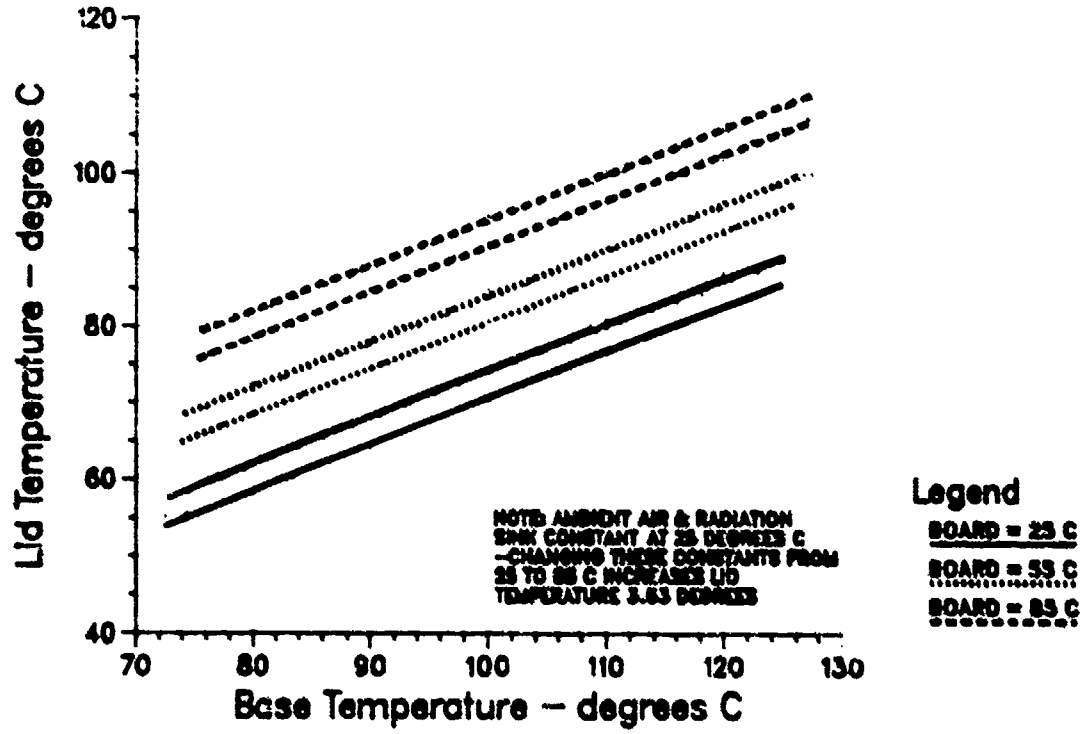


Figure 60. Lid versus Base Temperature - Predicted Cerdip Package

5.4.3.4 Flatpack Package

The derating curves for the flatpack package are presented in Figures 61 and 62. The flatpack modeling techniques (assumptions and specifications) are addressed in full detail in appendix 6.4. The same conditions hold for using these curves. The correct assumptions must be identified, and the ambient air, radiation sink, board, and lid temperatures must be known. The nodal conduction equations are based on specific package and material type and dimensions. The measurement location for the board temperature is specified as being on the bottom side of the board, directly under the device.

5.4.3.5 Hybrid Package

The derating curves for the hybrid package are specified in Figures 63 through 68. In Figures 63 and 67, the derating tolerance bands for the different board temperatures overlap one another. Therefore, the band for each board was plotted separately in Figures 64 through 66, and Figures 68 through 70.

The hybrid package presents a special group of problems. Once the hybrid is sealed, there is no way to tell what is inside. Therefore, it is necessary to know what elements make up the hybrid device prior to sealing. Because of the quantity and variety of elements composing a hybrid, the modeling of this package involved averaging the area as one single heat source. The information required in the other package types (ambient air, radiation sink, board, and lid temperatures) is also required for the

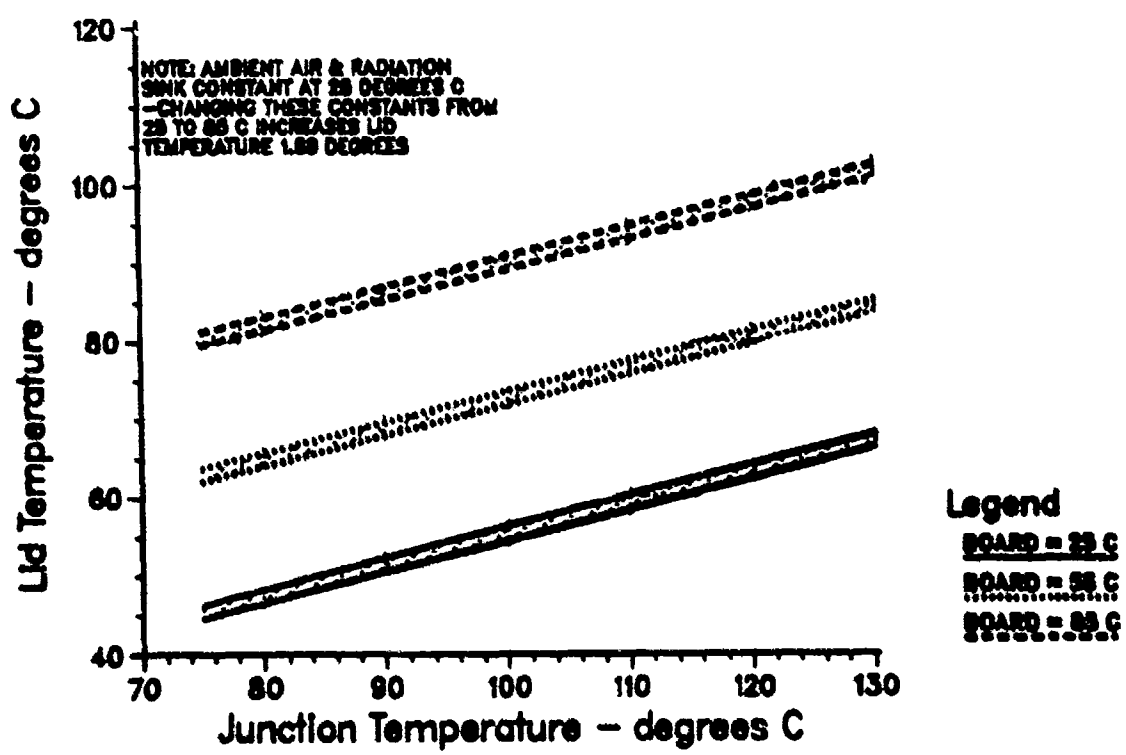


Figure 61. Junction versus Lid Temperature - Predicted Flatpack Package

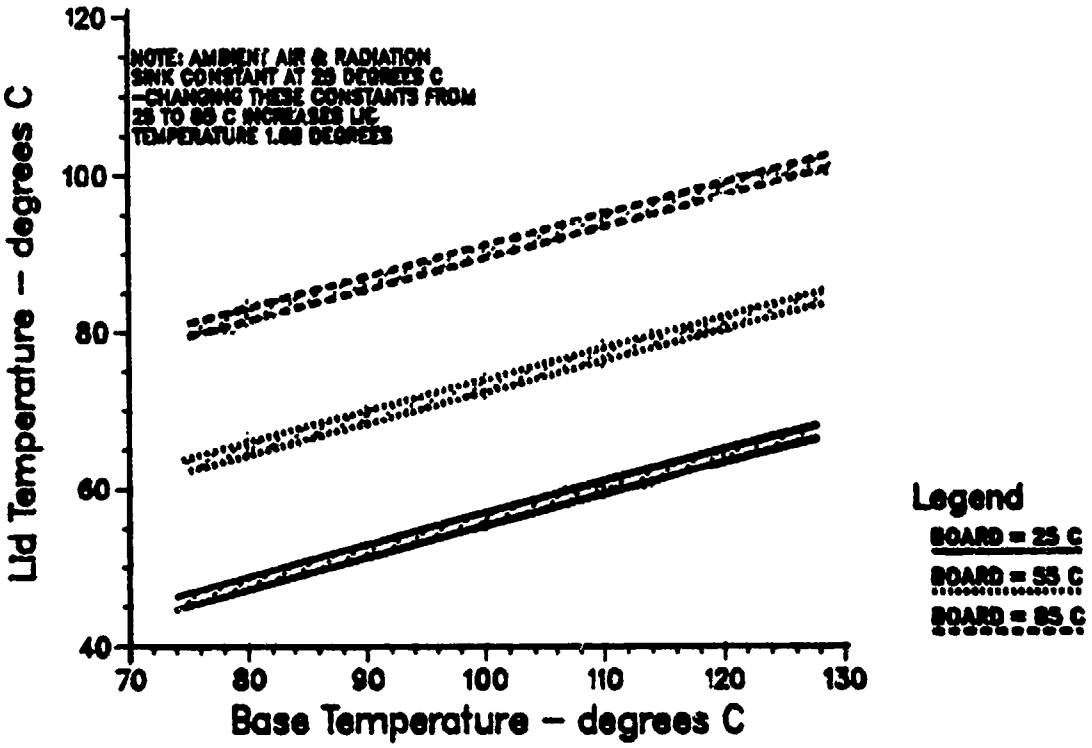


Figure 62. Lid versus Base Temperature - Predicted Flatpack Package

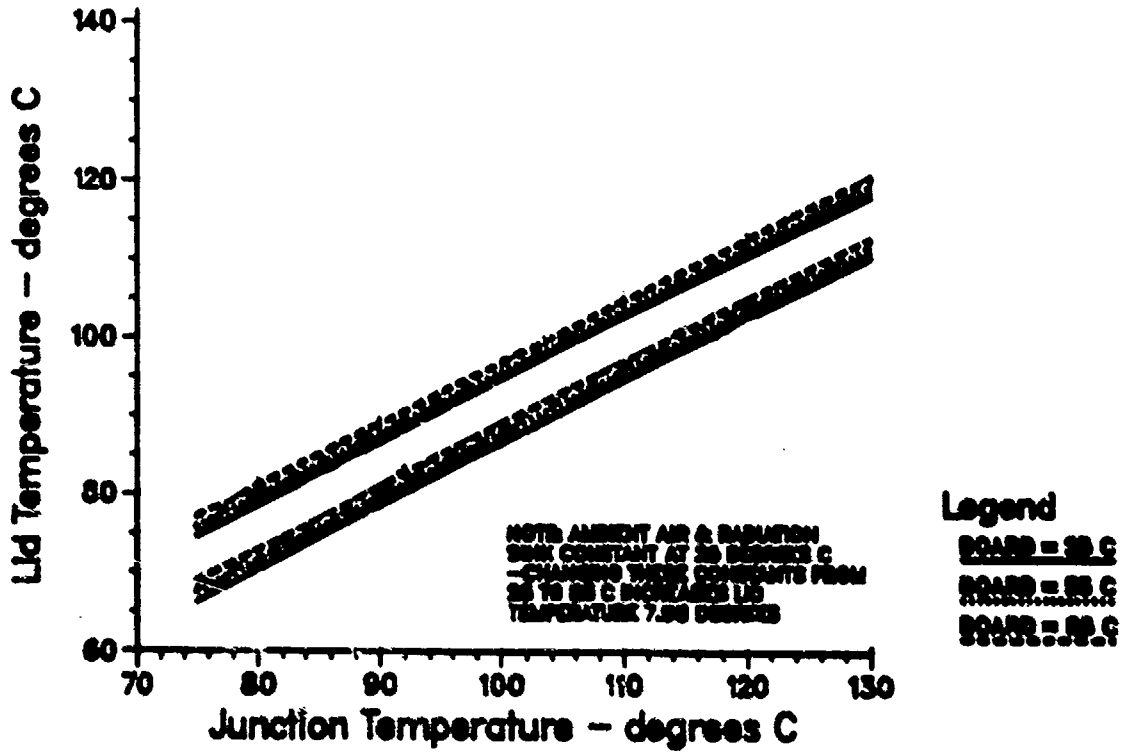


Figure 63. Junction versus Lid Temperature - Predicted Hybrid Package

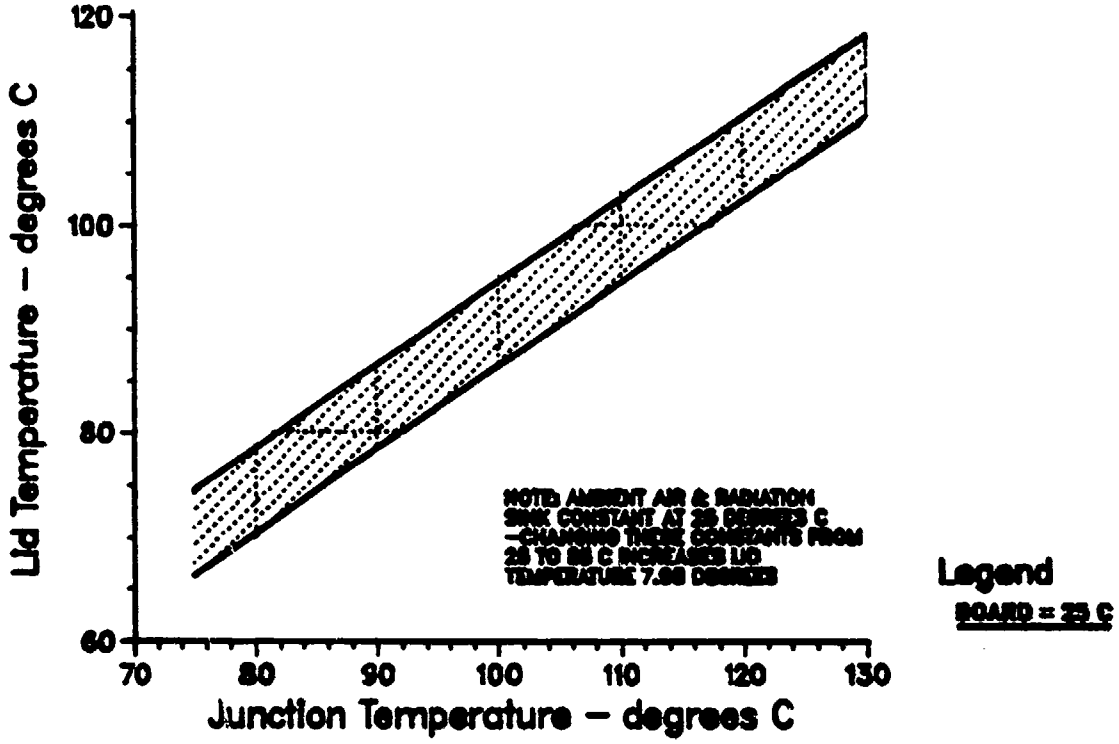


Figure 64. Junction versus Lid Temperature - Predicted Hybrid Package

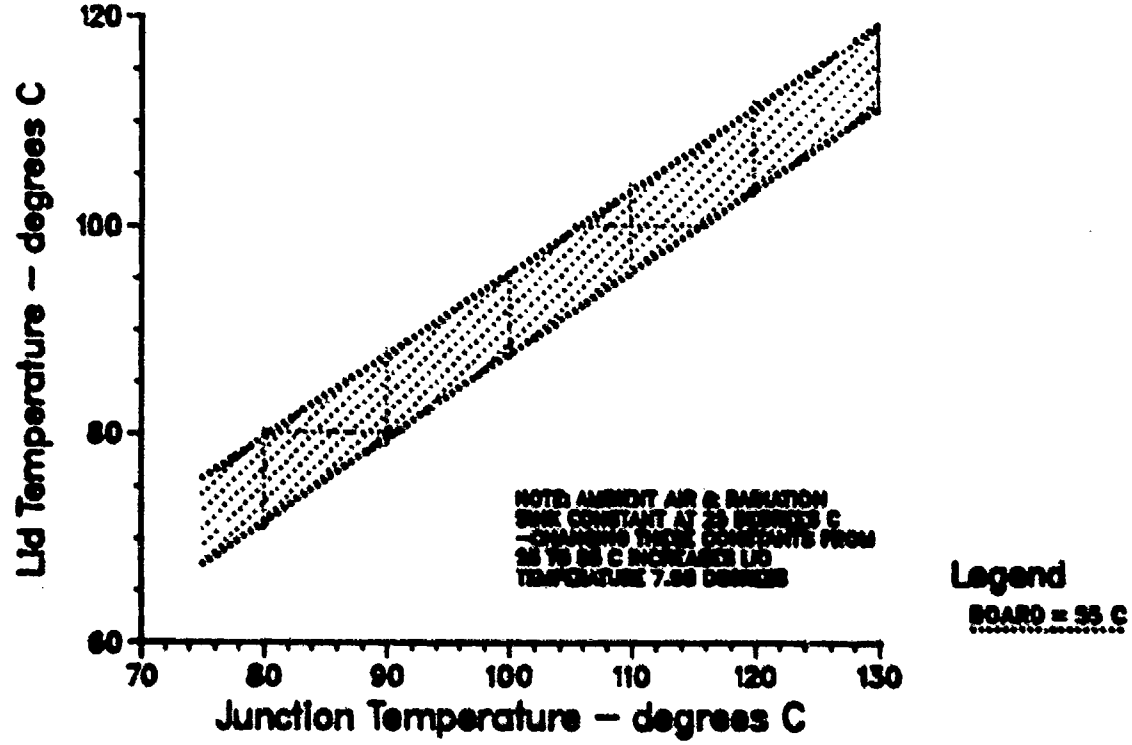


Figure 65. Junction versus Lid Temperature - Predicted Hybrid Package

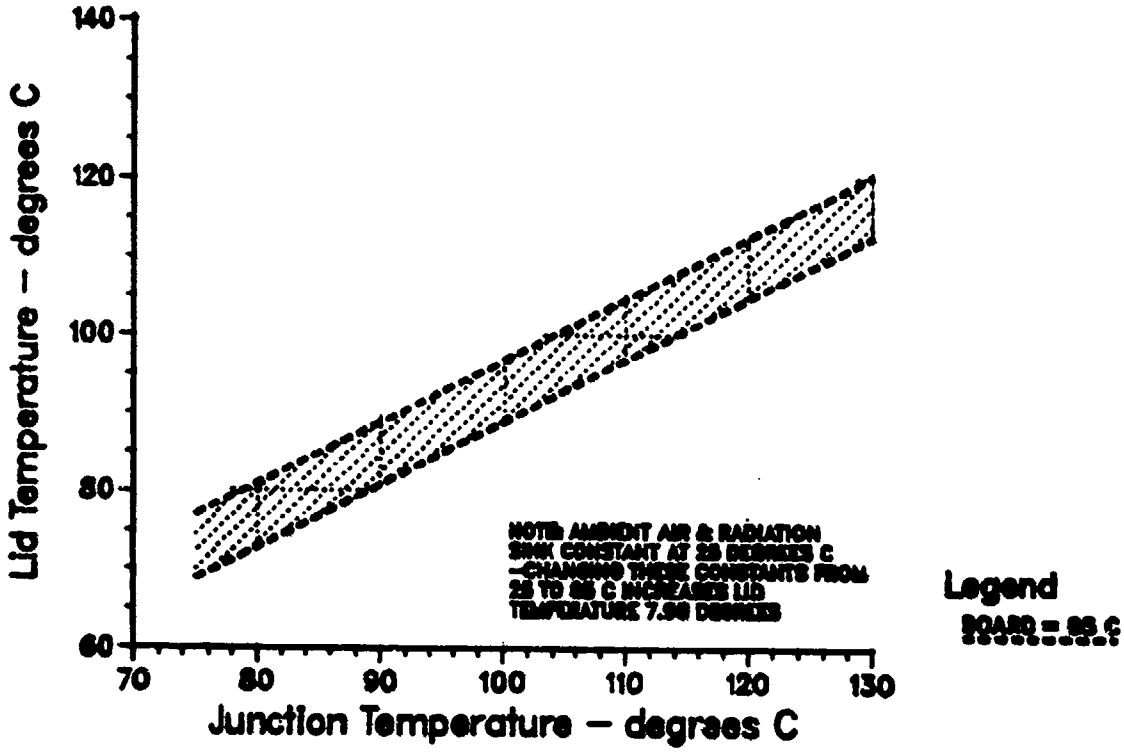


Figure 66. Junction versus Lid Temperature - Predicted Hybrid Package

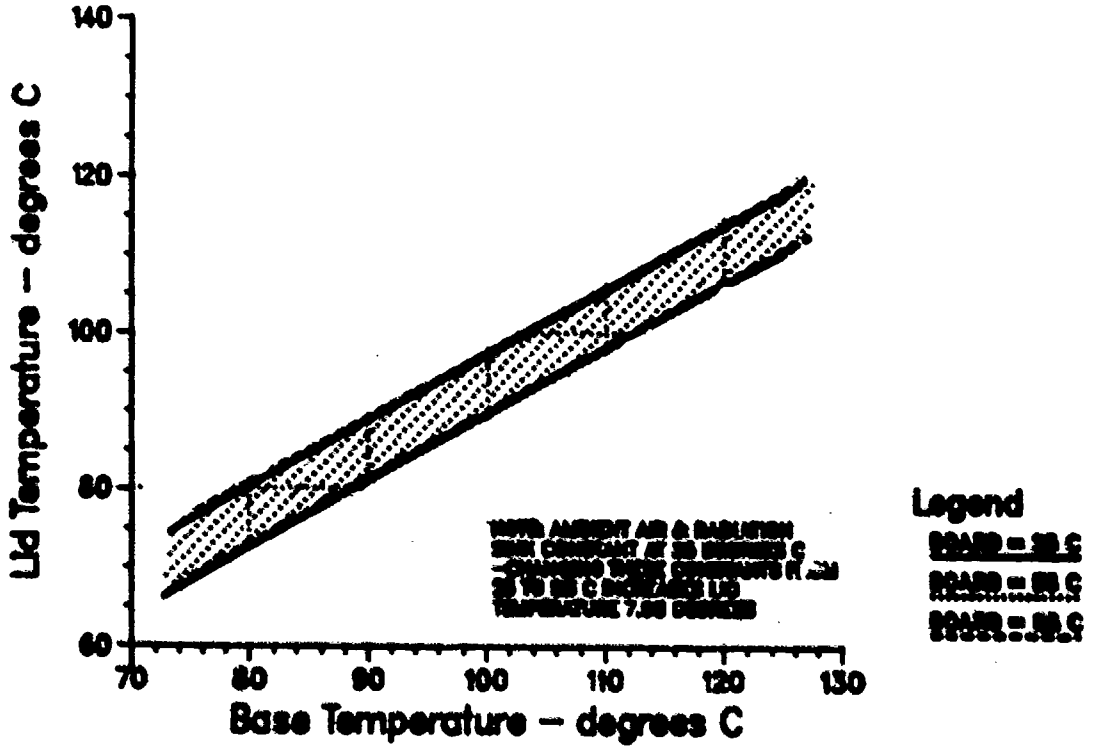


Figure 67. Lid versus Base Temperature - Predicted Hybrid Package

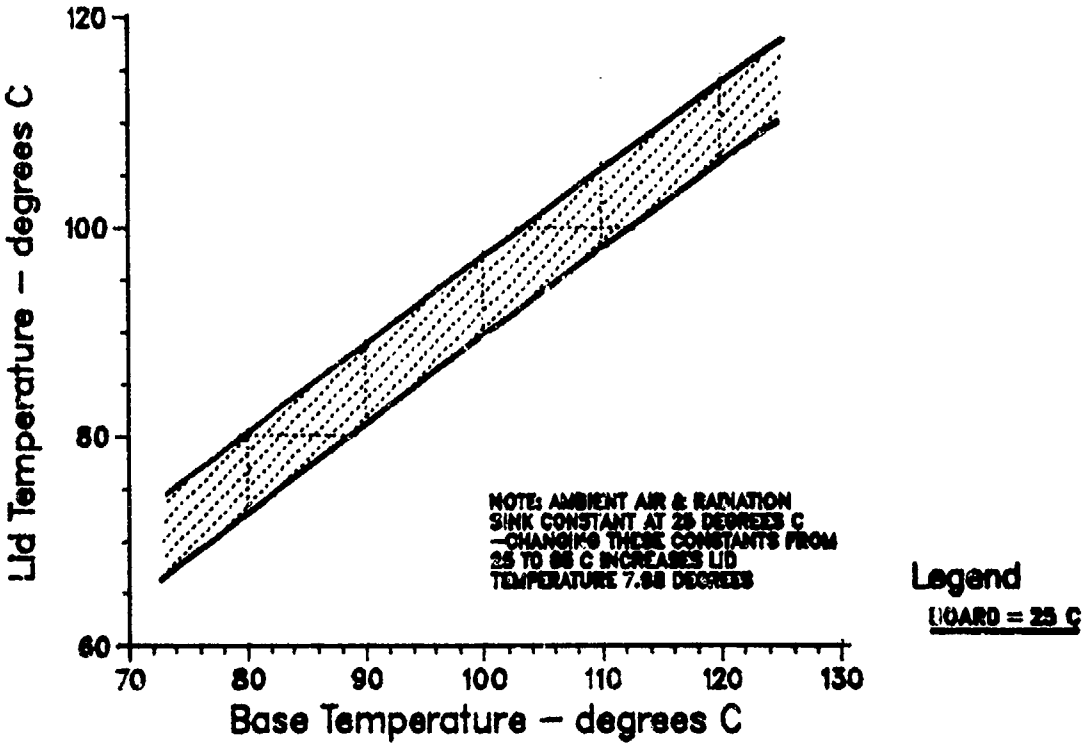


Figure 68. Lid versus Base Temperature - Predicted Hybrid Package

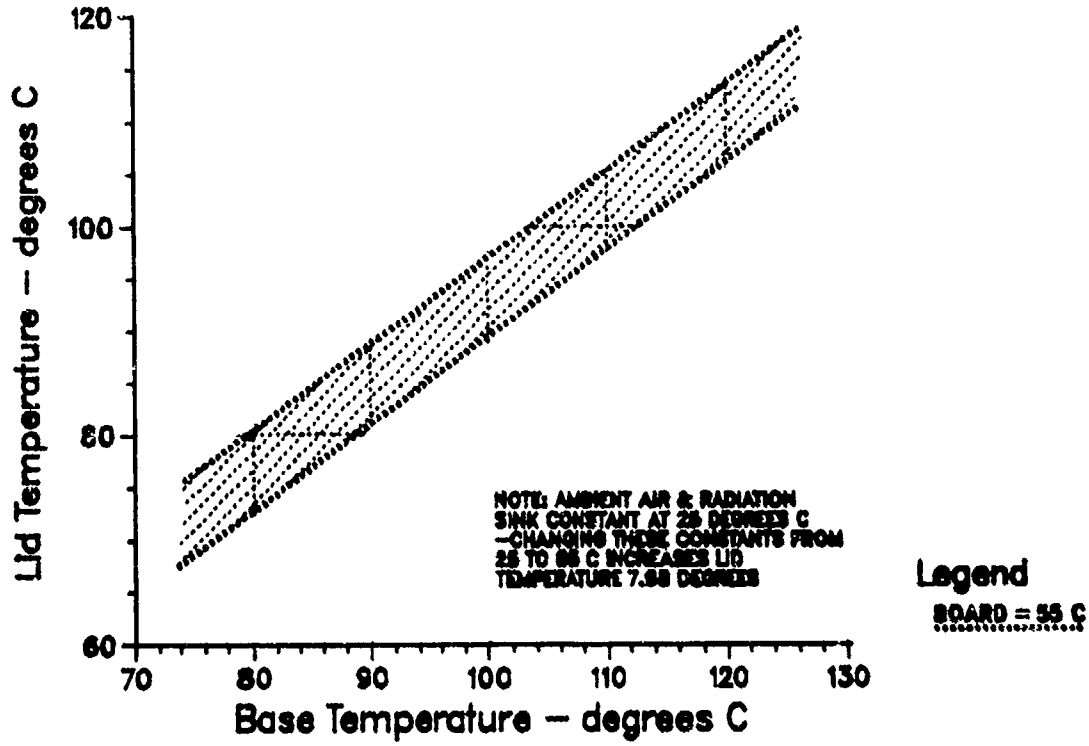


Figure 69. Lid versus Base Temperature - Predicted Hybrid Package

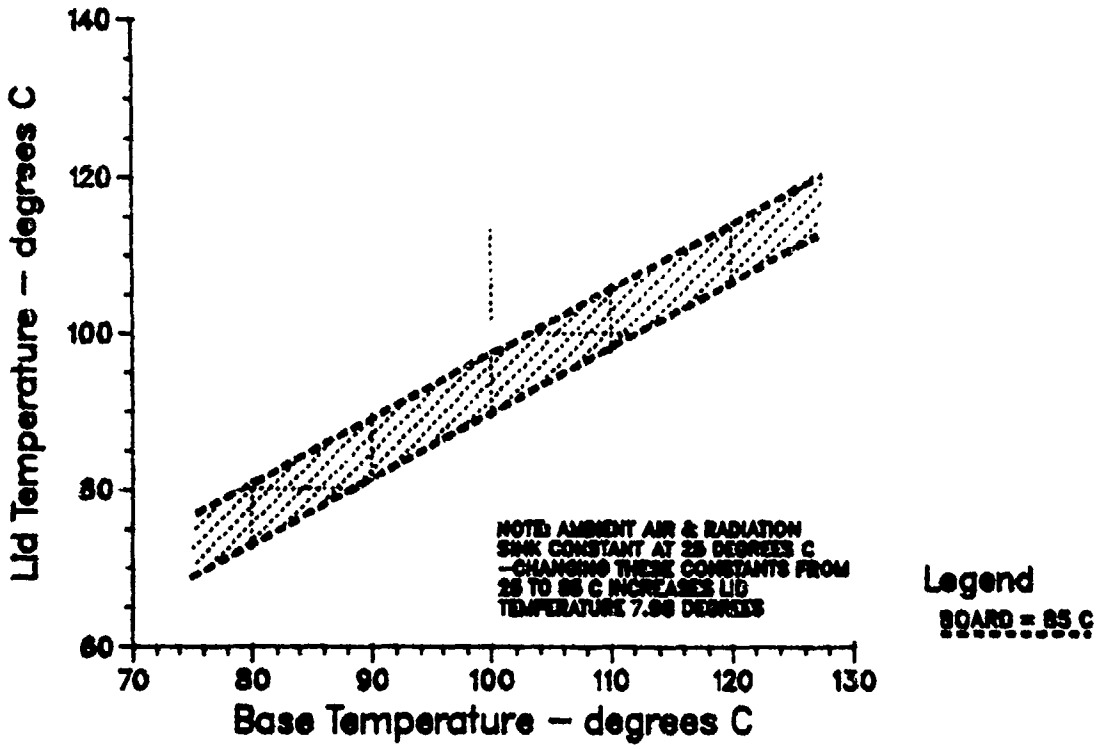


Figure 70. Lid versus Base Temperature - Predicted Hybrid Package

hybrid. The board measurement location is the same. The basic assumptions made in the modeling process are in appendix 6.5. Since hybrid packages are very complex and are usually custom designed, a detail internal thermal analysis should be required to be performed by the vendor.

5.4.3.6 Axial Stud Package

The axial stud package is a special case, since the devices are generally not accessible for measurement. In most cases, these devices are mounted inside a cavity or heatsink. This creates a difficulty in making measurements. The derating curves for the axial stud package type were generated, based on certain assumptions and specifications which are presented in appendix 6.6. The actual curves for axial stud package models are in Figures 71 and 72. The board temperature is replaced by the heatsink temperature in these figures, with the measurement location being adjacent to the ceramic ring. The measurement point identified for the purpose of relating back to the junction temperature is a point on the ceramic ring near the bottom of the device. This point is only measurable before the device is mounted into an operating system.

5.5 Measurement Equipment

The accuracy of the measured device temperatures is directly dependent upon the device or method used to obtain the measurement. There are numerous measurement devices available. The simplest method is the use of thermocouples. If a thermocouple is used for measurement, the best accuracy one could expect would be in the 1 to 2°C range, due to the limitations

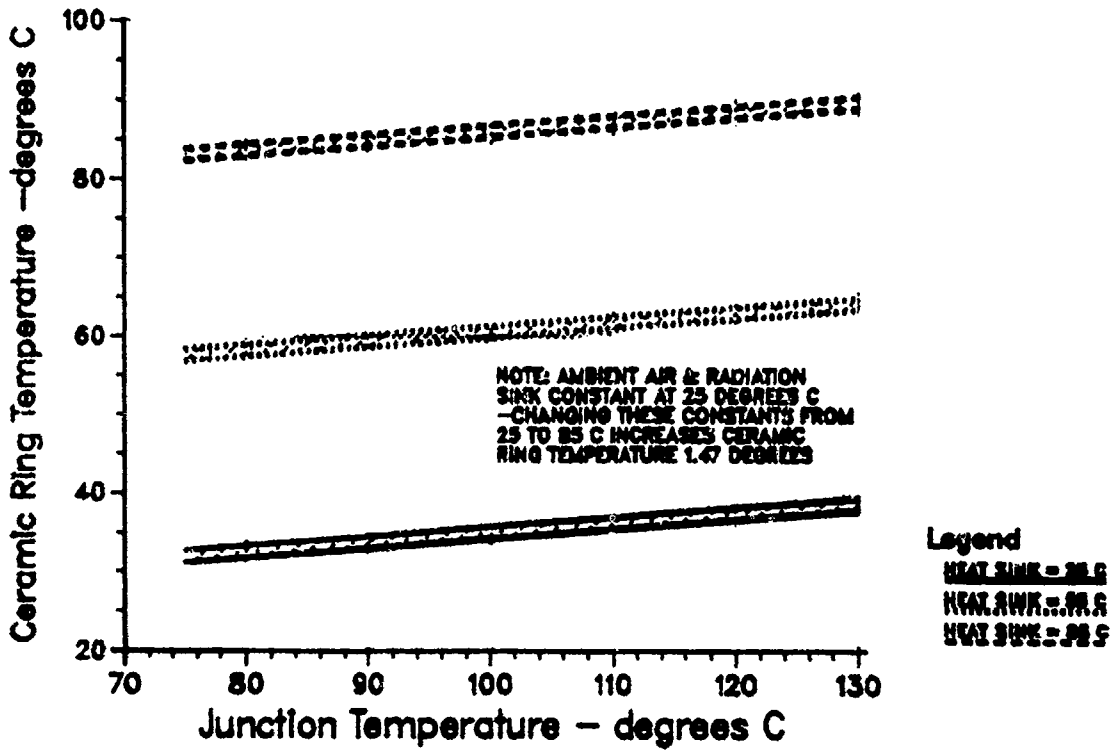


Figure 71. Junction versus Ceramic Ring Temperature - Predicted Axial Stud Package

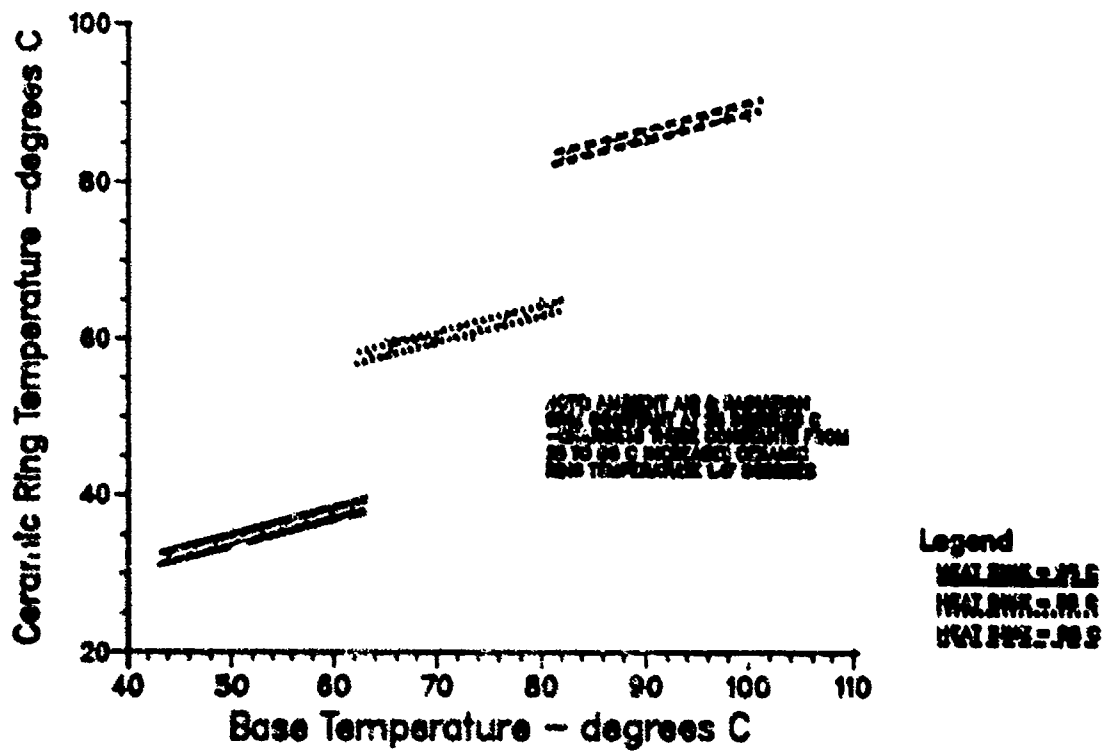


Figure 72. Ceramic Ring versus Base Temperature - Predicted Axial Stud Package

of the thermocouple itself. The cost involved in using thermocouples is associated with the recorder. The recorder allows for approximately six to twenty simultaneous thermocouple readings, and costs about $2000.

A second simple, but less versatile, method is the use of temperature labels. The label method can only be used where there is sufficient space to apply the label. The sizes generally available range from three-sixteenths of an inch to approximately five-sixteenths inch in diameter spots and rectangular labels approximately 3/4 by 1/4 of an inch. The rectangular labels could be applied to a variety of dual-in-line packages, and the spots to TO-5, TO-91, TO-99, TO-100, TO-3, and TO-66 packages. The labels adhere to the surface of the object to monitor its temperature. As each heat sensitive spot is exposed to temperature, the dot changes temperature in approximately one second, with a plus or minus one percent accuracy. The temperatures available are generally in 10°C increments. The dot can can only be used once.

A more modern and sophisticated method is the use of infrared (IR) temperature probes. These devices can be found in a wide range, from hand-held, portable, self-contained to fixed-mounted instruments, with a broad family of indicators and controllers. The instruments available can result in much more accurate and repeatable temperature measurements. Table 37 shows the specifications available for such instruments. The cost of these instruments, depending on the specification requirements, ranges from approximately $350 to more than $2000. The IR technique is not the least expensive way of measurement. Instead, it is an order of magnitude greater than other methods. The IR technique also allows for only one measurement at a time. Testing problems emerge with using the IR temperature probes, when access to the printed circuit board is not permitted in the system configuration. In this case, the IR method would not be recommended, and thermocouples would have to be used.

TABLE 37. INFRARED TEMPERATURE PROBES SPECIFICATIONS AVAILABLE

Specification	Range (Typical)
Accuracy	± 0.5 percent of reading or scale
Repeatability	± 1°C or 1°F; ± 0.5 percent
Temperature ranges (selection)	-30°C to 1100°C -30°F to 2000°F
Power requirements	ac or dc
Display	analog or digital
Target spot size	Factory set and/or varies with operation distance
Operations distance	2 centimeters to infinity

6.0 COST VERSUS RELIABILITY

The cost of reliability is a very complex and controversial subject. The complexity is due to several factors which interact and drive both the cost and reliability. The controversy is a result of the reliability funding level versus contract reliability analysis and component requirements on a particular program.

The first factor to be considered is component temperature. As the temperature of a component, specifically microelectronic devices, increases, the failure rate also increases. Figure 73 shows a curve plotting junction temperature versus failure rate multiplier. This curve is based on a relatively simple class B digital low power Schottky TTL quad 2-input nand gate (generic 54LS00). This simple, yet common, gate was selected so other impacting parameters can be assessed against the same device. The failure rates used to derive the multipliers are shown in Table 38. The computer program that derived the failure rates did so in accordance with MIL-HDBK-217D. To derive the multipliers, the quality level B line was followed across the temperature range from 15 to 120°C. Since a class B component was used to produce the curve, a check was made to see if the multipliers hold true for any quality level. The largest error found was approximately 0.05 percent at 120°C for a class S component.

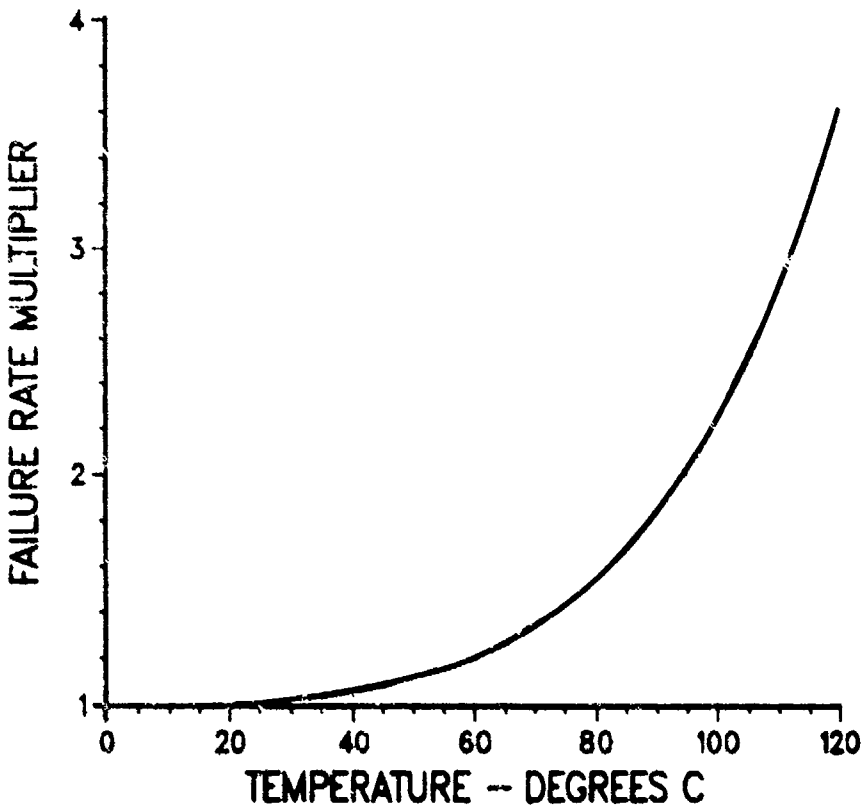


Figure 73. Temperature Impact on Failure Rate

TABLE 38. FAILURE RATES USED TO DERIVE MULTIPLIERS

ITEM	MIL-HDBK-217D QUAL	...STRESS... PWR	VLT	CUR	QTY	FAILURE RATE GF-OF TEMP = 15	GF-OF TEMP = 20	GF-OF TEMP = 25	GF-OF TEMP = 30	GF-OF TEMP = 35
IC DIG	S	CPLX=4			1	.0066	.0067	.0067	.0068	.0069
IC DIG	B	CPLX=4			1	.0133	.0134	.0135	.0136	.0138
IC DIG	B0	CPLX=4			1	.0265	.0267	.0270	.0273	.0277
IC DIG	B1	CPLX=4			1	.0398	.0401	.0404	.0409	.0415
IC DIG	B2	CPLX=4			1	.0862	.0868	.0876	.0887	.0900
IC DIG	C	CPLX=4			1	.1061	.1069	.1078	.1091	.1108
IC DIG	C1	CPLX=4			1	.1725	.1737	.1752	.1773	.1800
IC DIG	D	CPLX=4			1	.2322	.2338	.2359	.2387	.2423
IC DIG	D1	CPLX=4			1	.4643	.4676	.4718	.4774	.4846

ITEM	MIL-HDBK-217D QUAL	...STRESS... PWR	VLT	CUR	QTY	FAILURE RATE GF-OF TEMP = 40	GF-OF TEMP = 45	GF-OF TEMP = 50	GF-OF TEMP = 55	GF-OF TEMP = 60
IC DIG	S	CPLX=4			1	.0071	.0072	.0074	.0077	.0080
IC DIG	B	CPLX=4			1	.0141	.0144	.0149	.0154	.0160
IC DIG	B0	CPLX=4			1	.0282	.0289	.0297	.0308	.0321
IC DIG	B1	CPLX=4			1	.0423	.0433	.0446	.0462	.0481
IC DIG	B2	CPLX=4			1	.0917	.0939	.0966	.1000	.1042
IC DIG	C	CPLX=4			1	.1129	.1155	.1189	.1231	.1283
IC DIG	C1	CPLX=4			1	.1834	.1877	.1932	.2000	.2085
IC DIG	D	CPLX=4			1	.2469	.2527	.2600	.2692	.2806
IC DIG	D1	CPLX=4			1	.4937	.5054	.5201	.5385	.5613

ITEM	MIL-HDBK-217D QUAL	...STRESS... PWR	VLT	CUR	QTY	FAILURE RATE GF-OF TEMP = 65	GF-OF TEMP = 70	GF-OF TEMP = 75	GF-OF TEMP = 80	GF-OF TEMP = 85
IC DIG	S	CPLX=4			1	.0084	.0089	.0095	.0102	.0111
IC DIG	B	CPLX=4			1	.0168	.0178	.0190	.0205	.0222
IC DIG	B0	CPLX=4			1	.0337	.0357	.0381	.0410	.0445
IC DIG	B1	CPLX=4			1	.0505	.0535	.0571	.0615	.0667
IC DIG	B2	CPLX=4			1	.1095	.1159	.1237	.1332	.1446
IC DIG	C	CPLX=4			1	.1347	.1426	.1523	.1639	.1780
IC DIG	C1	CPLX=4			1	.2189	.2318	.2474	.2664	.2892
IC DIG	D	CPLX=4			1	.2947	.3120	.3330	.3586	.3893
IC DIG	D1	CPLX=4			1	.5894	.6240	.6661	.7171	.7786

TABLE 38. (CONTINUED)

MIL-HDBK-217D

ITEM	QUAL	PWR	VLT	CUR	N1	N2	CUM	1	2	3	4	5	6	7	8	9	10
IC DIG	S	CFLX=4			1		.0121	.0133	.0145	.0188	.0240						
IC DIG	B	CFLX=4			1		.0264	.0289	.0298	.0478	.0589						
IC DIG	B0	CFLX=4			1		.0481	.0537	.0593	.0783	.0969						
IC DIG	B1	CFLX=4			1		.0731	.0806	.0880	.1141	.1401						
IC DIG	B2	CFLX=4			1		.1083	.1196	.1308	.1688	.2068						
IC DIG	C	CFLX=4			1		.1681	.1849	.2017	.2593	.3169						
IC DIG	C1	CFLX=4			1		.3165	.3493	.3820	.4902	.5984						
IC DIG	D	CFLX=4			1		.4262	.4702	.5142	.6589	.8035						
IC DIG	D1	CFLX=4			1		.8524	.9403	1.0282	1.3040	1.5798						

The next factor to be considered is the relation of component quality level and its impact on the failure rate. Figure 74 graphically shows this relationship. The same digital low power Schottky TTL quad 2-input nand gate was used to derive the multipliers. Again, the failure rates are shown in Table 38. Table 39 is a copy of MIL-HDBK-217D quality factors for microelectronic devices. The table gives the description of each quality level addressed.

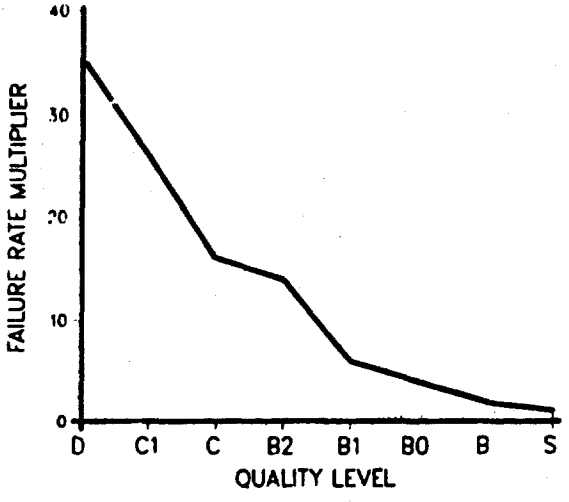


Figure 74. Quality Level Impact on Failure Rate

TABLE 39. π_Q, QUALITY FACTORS

Quality Level	Description	π_Q
S	Procured in full accordance with MIL-M-38510, Class S requirements.	0.5
B	Procured in full accordance with MIL-M-38510, Class B requirements.	1.0
B-0	Procured in full accordance with MIL-M-38510, Class B requirements except that device is not listed on Qualified Products List (QPL). The device shall be tested to all the electrical requirements (parameters, conditions and limits) of the applicable MIL-M-38510 slash sheet. No waivers are allowed except current and valid generic data** may be substituted for Groups C and D.	2.0
B-1	Procured to all the screening requirements of MIL-STD-883, Method 5004, Class B and in accordance with with electrical requirements of MIL-M-38510, DESC drawings, or vendor/contractor electrical parameters. the device shall be tested to all the quality conformance requirements of MIL-STD-883, Method 5005, Class B. No waivers are allowed except current and valid generic data** may be substituted for Groups C and D. This category applies to DESC drawings and contractor prepared specification control drawings (SCD's) containing the above B-1 screening and quality conformance requirements.	3.0
B-2	Procured to vendor's equivalent of the screening requirements of MIL-STD-883, Method 5004, Class B, and in accordance with the vendor's electrical parameters and vendor's equivalent quality conformance requirements of MIL-STD-883, Method 5005, Class B. Applies to contractor prepared SCD's containing the above B-2 screening and quality conformance requirements.	6.5
C	Procured in full accordance with MIL-M-38510, Class C requirements.	8.0
C-1	Procured to screening requirements of MIL-STD-883, Method 5004, Class C and the qualification requirements of Method 5005, Class C. Generic data may be substituted for Groups C&D	13.0
D	Hermetically sealed part with no screening beyond the manufacturer's regular quality assurance practices; parts encapsulated with organic material.*	17.5
D-1	Commercial (or non-mil standard) part, encapsulated or sealed with organic materials (e.g., epoxy, silicone or phenolic).	35.0

Finally, the cost of the same device is assessed against the quality levels previously discussed. The cost data against the subject device was provided by the Martin Marietta component engineering group. This data was based on an average cost from two large semiconductor manufacturers for the specific quality level. The average cost was then converted to a multiplier using the D1 quality level as a base (1.0). A D1 quality level is a commercial or non-military standard component. Figure 75 shows the quality level impact on component cost by plotting the cost multiplier against the quality level. The points on the figure marked by a triangle (Δ) indicate actual data points obtained. The curve is then plotted across all the quality levels.

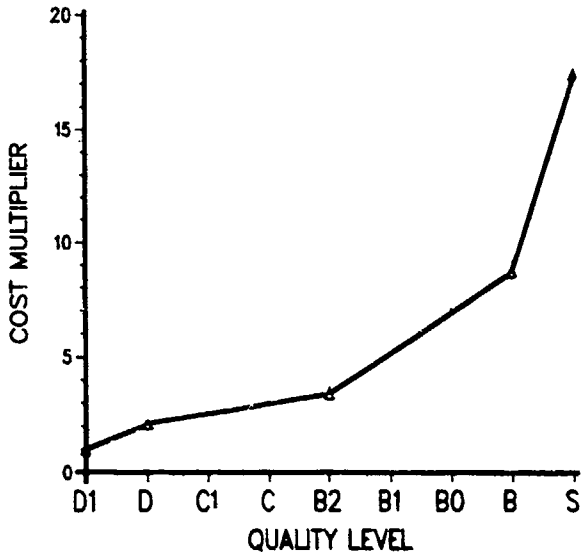


Figure 75. Quality Level Impact on Cost

Additional cost factors which impact reliability are contained in the design process. The design process, in relation to derating criteria, encompasses the type of cooling necessary and addition of heat sinks to reduce the component temperature. The degree of reliability in design then is part of the quantity and quality of analysis. Both are from the design and reliability group. The driver becomes the requirement imposed by the product specification, or the importance and visibility of reliability by the contractor. An example of in-depth analysis of the microelectronics may include investigation of all parameters that vary with temperature. Figure 76 shows the variation of silicon conductivity with temperature. This figure, coupled with the failure rate multiplier figures previously discussed, could be used to determine the method of cooling and necessity of heat sinks. A less thorough analysis may be the accomplishment of a reliability prediction using average temperatures and stress levels.

The specification driver is defined through the imposition of MIL-STD-785B or MIL-STD-1543, notice 2. Through the imposing of specific tasks or paragraphs of the military standards, a minimum level of reliability is established. According to data collected in RADC-TR-83-13, "Missile and Space Systems Reliability vs Cost Trade-off Study," the average cost in

man-months per year, varies slightly across program phase. The reliability program cost can be estimated as a percent of engineering labor per year for the three major program phases. The FSED program phase averages 4.3 percent of total engineering labor for the reliability program. The production and validation program phases average 4.4 and 5.0 percent respectively.

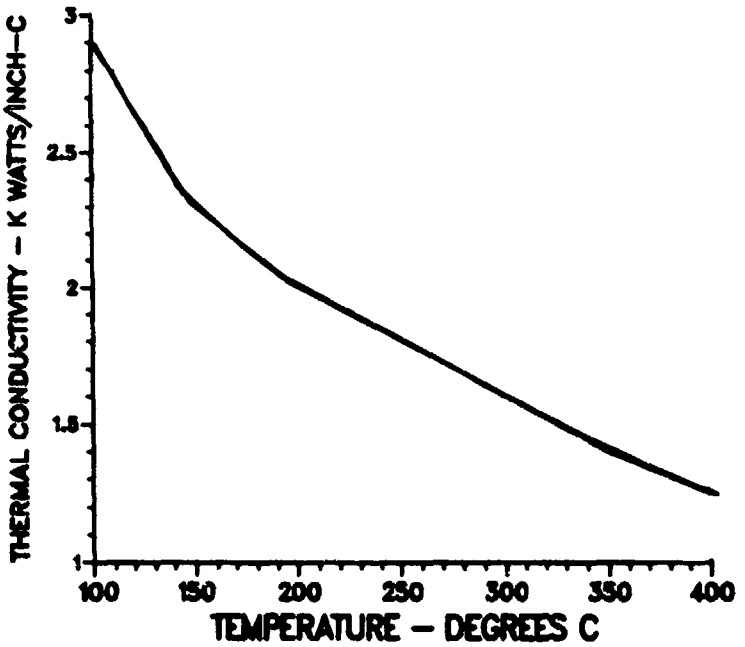


Figure 76. Silicon Thermal Conductivity versus Temperature

The major cost drivers, according tc RADC-TR-83-13, within the reliability program related to MIL-STD-785B, are:

1	Parts program	28.3 percent
2	FRACAS/FRB	11.3 percent
3	Engineering support	14.0 percent
4	FMECA	4.7 percent
5	Testing	6.0 percent
6	Analysis	8.7 percent

These average cost driver percentages are based on the average across FSED, production, and validation phases of a program. At this point, none of the referenced funding levels for reliability include engineering support from engineering to reliability, or any engineering performed analyses.

In order to reduce program costs, part quality level reduction is often considered. The reduction of part quality level, from mil to commercial, has impacts on failure rate and cost. The failure rate impact has been shown previously in figure 74 and related cost impact in figure 75. Derating cannot be used to compensate for using parts of a lower quality level. The derating levels specified (I, II or III) are not based on part quality. The levels are based on mission criticality assuming the proper quality part has been selected. Component derating can in no way account for or make up for poor quality.

The subject of cost versus reliability can be summarized as a complex relationship. It is not solely controlled by the contractor or customer, design engineer, or reliability engineer. The basic tools are available to produce a good reliable piece of hardware. Without the proper time span and funding, however, something less is often accepted. Depending upon the program phase, the commitment assumes different emphasis, i.e., analytical, test, etc. But each phase commitment is reduced to two basic constraining factors, cost and schedule. In spite of the restrictive cost and schedule and schedule constraints, the reliability function must be introduced at the early phase of the program. Continuity must be maintained. The reliability tasks, as a minimum for each program phase, are specified in MIL-STD-785B appendix A, Table A-I. These tasks should be strictly adhered to.

7.0 MILITARY STANDARD FRAMEWORK

The final specific task identified in the program approach was to develop a military standard framework. The framework is intended to be used for the creation of the standard for the derating of electronics and electromechanical devices for Air Force application. Figure 76A shows the outline for the military standard.

Figure 76A

OUTLINE OF MILITARY STANDARD

1.0	SCOPE
1.1	Purpose
1.2	Application of Standard
1.2.1	Content of Standard
1.2.2	Tailoring
2.0	REFERENCE DOCUMENTS
2.1	General
3.0	DEFINITIONS
4.0	GENERAL REQUIREMENTS
4.1	Equipment Derating Levels
4.2	Equipment Environments
5.0	DETAILED REQUIREMENTS
5.1	Microcircuits
5.2	Transistors
5.3	Diodes
5.4	Resistors
5.5	Capacitors
5.6	Surface Acoustical Wave Devices
6.0	APPENDICES
	(Examples of Parts Derating)

8.0 CONCLUSIONS AND RECOMMENDATIONS

8.1 Conclusion

The primary objective of the Reliability Derating Procedures program was to develop the framework for the creation of a military standard. This standard is to be for the derating of electronic and electromechanical devices for Air Force application. This was accomplished through the investigation of specific areas, such as the relationship of case temperatures to junction temperatures, the development of derating standards for selected advance technology devices, the creation of thermal models, the derating thermal model verification through data collection and testing, and the relationship of reliability to cost. Based on this investigation, several conclusions were drawn which led to the accomplishment of the program's overall objectives. These conclusions are:

1. Standardized derating criteria is greatly desired by industry, since industry does not have such criteria available at the present time.

2. The development of derating standards for the advanced technology devices did not produce any astonishing results.

3. The internal model is particularly useful when a ball park prediction of the thermal resistance from the chip junction to the case bottom (θ_{JC}) is desired for devices of new design.

4. The heat spreading angle involved in the internal model calculation has a significant impact on the θ_{JC}. However, correlation of this angle could not be ascertained, due to program limitations.

5. There are many variables involved in thermal modeling. The number of variables necessitates the modeling of specific package types, as opposed to general ones.

6. The external model is applicable only to specific package types or configurations.

7. Both models (internal and external) can be easily modified to change variable conditions to meet particular needs.

8. Two external models were verified through test data, resulting in an accuracy of approximately 4°C.

9. The remaining external models were developed with the same assumptions and ground rules as the two that demonstrated such a high correlation with test measurements. It can be expected that these remaining models are accurate (except hybrid external model).

10. The hybrid package presents a special group of problems. Since hybrid packages are very complex and are usually custom designed, a detailed internal thermal analysis should be required to be performed by the vendor.

11 The methodology for verifying junction temperature derating requires the identification of a case measurement point. The point chosen for all packages, except the axial study package, is the geometric top center of the lid. The axial stud measurement point is on the ceramic ring close to the heat source.

12 The lid category was investigated as a possible measurement point. It was determined that the lid temperature tracks more closely with the junction temperature.

13 In terms of reliability versus cost, it was determined that the reliability function must be introduced at the early phases of a program. Also, continuity must be maintained, in spite of the restrictive cost and scheduling constraints.

8.2 Recommendations

All the objectives set forth for this program were achieved. However, during the course of the program, areas deserving further investigation were identified. Those areas could not be investigated in this study due to program limitations. Instead, a series of recommendations have been developed for possible implementation into future work in this subject area:

1 Additional package types or configurations should be modeled in order to extend the data verification base.

2 Additional data from test measurements should be obtained to further validate the models presented in this study. Any additional models required should be created.

3 Additional investigation of the heat spreading angle is warranted, due to its impact on the resulting thermal resistance.

4 In an effort to ascertain industry acceptance and possibly create the surfacing of additional data, the Air Force should disseminate the results of this study to all those concerned.

APPENDIX 1.0

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APPENDIX 2.0

POTENTIAL DATA SOURCES

Advanced Micro Devices Inc., Sunnyvale, CA
Aerojet Electrosystems, Azusa, CA
*Aerospace Corporation, Los Angeles, CA
Aertech Industries, Sunnyvale, CA
*Airesearch, Torrance, CA
AM General Corp., Detroit, MI
AMBAC Industries, Ft. Washington, PA
*AMEX Systems, Hawthorne, CA
American Microsystems, Santa Clara, CA
Anderson Labs, Inc., Bloomfield, CT
Applied Devices, Kissimmee, FL
Applied Physics Lab, Laurel, MD
ARINC Research Corp., Annapolis, MD
Arma Division (AMBAC), Garden City, NY
Automation Industries (Vitro), Silver Springs, MD
*Ball Aerospace, Boulder, CO
Bechtel Power, Ann Arbor, MI
Bechtel Power, Norwalk, CA
Beckman Instruments, Fullerton, CA
Bell Aerospace, Buffalo, NY
Bell Helicopter, Ft. Worth, TX
Bendix-Oceanics, Sylmar, CA
Bendix-Guidance, Mishawaka, IN
*Bendix-Communications, Baltimore, MD
Bendix-Aerospace, Towson, MD
*Bendix-Guidance, Teterboro, NJ
Boeing-Aerospace, Seattle, WA
Bulova Watch, Valley Stream, NY
Bunker-Ramo, Thousand Oakes, CA
*Burroughs, Paoli, PA

NOTE: Asterisk (*) denotes useful responses.

*Chandler Evans, W. Hartford, CT
Charles Stark Draper Lab, Cambridge, MA
Cincinnati Electronics, Cincinnati, OH
Comsat Labs, Clarksburg, MD
CONRAC Corp., Duarte, CA
Crystal Technology, Inc., Palo Alto, CA
*CUBIC Corp., San Diego, CA
Dalmo-Victor, Belmont, CA
*Douglas Aircraft, Long Beach, CA
Dynalectron-Aerospace, Ft. Worth, TX
EM & M - Sesco, Chatsworth, CA
*E-Systems, St. Petersburg, FL
*E-Systems, Monteck Division, Salt Lake City, UT
*E-Systems, Falls Church, VA
Eaton Corp., Long Island, NY
EDO Corp., College Point, NY
Efratom Systems, Irvine, CA
Electrodynamics (Talley), Rolling Meadows, IL
*Electrospace Systems, Richardson, TX
*Emerson Electric, St. Louis, MO
Fairchild Republic, Farmingdale, NY
Fairchild, Space & Electronics, Germantown, MD
Fairchild Stratos, Manhattan Beach, CA
Fairchild Test Systems, Latham, NY
Fairchild-Weston, Syossett, NY
*FMC-Northern Ordnance, Minneapolis, MN
FMC-Ordnance, San Jose, CA
Ford-Aeronutronic, Newport Beach, CA
*Ford Aerospace, Palo Alto, CA
General Dynamics - Pomona, Pomona, CA
*General Dynamics - Convair, San Diego, CA
General Dynamics - Electronics, San Diego, CA

NOTE: Asterisk (*) denotes useful responses.

General Dynamics - Land Systems, Warren, MI
General Dynamics, Ft. Worth, TX
General Electric, Daytona Beach, FL
*General Electric, Pittsfield, MA
General Electric, Schenectady, NY
General Electric, Syracuse, NY
General Electric, Utica, NY
*General Electric, Philadelphia, PA
General Electric, Burlington, VT
General Instrument, Hicksville, NY
*Goodyear Aerospace, Akron, OH
Goodyear Aerospace, Litchfield Park, AZ
*Gould Inc., El Monte, CA
Gould Inc., Glen Burnie, MD
Gould, Inc., Cleveland, OH
*Grumman Aerospace, Bethpage, NY
GTE Systems, Mountain View, CA
*Hamilton 57D, Windsor Locks, CT
Harris Corp., Melbourne, FL
Harris Corp., Rochester, NY
*Harris Corp., Syosset, NY
*Hartman Systems, Huntington Station, NY
Hazeltine Corp., Braintree, MA
*Hazeltine Corp., Greenlawn, NY
Hewlett Packard, Palo Alto, CA
Hewlett Packard, Loveland, CO
Hi-Rel Labs, Monrovia, CA
*Honeywell Inc., West Covina, CA
Honeywell Inc., Clearwater, FL
*Honeywell Inc., Tampa, FL
*Honeywell Inc., Lexington, MA
Honeywell Inc., Bloomington, MN

NOTE: Asterisk (*) denotes useful responses.

*Honeywell Inc., Hopkins, MN
*Honeywell Inc., St. Louis Park, MN
Honeywell Inc., Seattle, WA
Hughes Aircraft, El Segundo, CA
*Hughes Aircraft, Fullerton, CA
Hughes Aircraft, Los Angeles, CA
Hughes Aircraft, Torrance, CA
Hughes Helicopters, Culver City, CA
IBM Corp., Gaithersburg, MD
IBM Corp., Poughkeepsie, NY
IBM Corp., Owego, NY
IBM Corp., Hopewell Junction, NY
IBM Federal Systems Division, Owego Tioga County, NY
*Ingalls Shipbuilding, Pascagoula, MS
Integrated Circuit Engineering, Scottsdale, AZ
International Engineering, San Francisco, CA
International Laser Systems, Orlando, FL
*Interstate Electronics, Anaheim, CA
Intel Corp., Chandler, AZ
Intel Corp., Santa Clara, CA
ITT Avionics, Clifton, NJ
ITT Aerospace, Ft. Wayne, IN
ITT Electro-Optical, Roanoke, VA
ITT Federal Electric, Paramus, NJ
*ITT Gilfillan, Van Nuys, CA
Joy Manufacturing, New Philadelphia, OH
*Kaiser Electronics, San Jose, CA
Kaman Sciences Corp., Colorado Springs, CO
Keltec Florida, Ft. Walton Beach, FL
Ketron Inc., Warminster, PA
*Kyocera International Inc., San Diego, CA
Lawrence Livermore Lab, Livermore, CA

NOTE: Asterisk (*) denotes useful responses.

Lear Siegler, Grand Rapids, MI
Litton Data Systems, Van Nuys, CA
Litton Systems Inc., Woodland Hills, CA
*Lockheed - California, Burbank, CA
Lockheed Electronics, Plainfield, NJ
Lockheed - Georgia, Marietta, GA
Lockheed Missile Systems, Sunnyvale, CA
*LSI Products, LaJolla, CA
Loral Electronic Systems, Yonkers, NY
*Magnavox Government & Industrial, Ft. Wayne, IN
*Magnavox, Torrance, CA
*Magnavox, Mahwah, NJ
*Martin Marietta, Denver, CO
*Martin Marietta, Orlando, FL
McDonnell Douglas, Huntington Beach, CA
*McDonnell Douglas, St. Louis, MO
Memorex, Santa Clara, CA
*Microsonics, Weymouth, MA
Microwave Associates, Burlington, MA
Motorola, Shaumburg, IL
*Motorola, Scottsdale, AZ
Motorola, Ft. Worth, TX
National Waterlift, Kalamazoo, MI
Norden Systems, Norwalk, CA
Northrup Corp., Anaheim, CA
Northrup Corp., Hawthorne, CA
*Northrop Corp., Newbury Park, CA
Northrop Corp., Rolling Meadows, IL
Novatronics Inc., Pompano Beach, CA
Perkin-Elmer, Pomona, CA
Plessey Dynamics, Hillside, NJ
*Plessey Optoelectronics, Irvine, CA

NOTE: Asterisk (*) denotes useful responses.

QED Systems, Virginia Beach, VA
*Exxon Office Systems, Lionville, PA
*RCA, Princeton, NY
*RCA, Burlington, MA
RCA Solid State Tech Center, Somerville, NJ
RCA, Camden, NJ
*RCA, Moorestown, NJ
Raytheon, Portsmouth, RI
*Raytheon, Goleta, CA
*Raytheon, Bedford, MA
Raytheon, Northborough, MA
Raytheon, Sudbury, MA
Raytheon, W. Andover, MA
Raytheon, Wayland, MA
*Reflectone, Tampa, FL
REL Inc., Boynton Beach, FL
Reliance Electric, Cleveland, OH
*RMI Inc., National City, CA
Rockwell International, Thousand Oaks, CA
Rockwell, Anaheim, CA
Rockwell, Downey, CA
*Rockwell, Los Angeles, CA
*Rockwell-Collins, Cedar Rapids, LA
*Rockwell, Columbus, OH
*Rockwell-Collins, Richardson, TX
*Rosemount Inc., Eden Prairie, MN
Sanders Associates, Nashua, NH
*Sandia Laboratories, Albuquerque, NM
*Sawtek Inc., Orlando, FL
*Science Applications, Palo Alto, CA
*Sedco Systems, Melville, NY
Semcor Inc., Moorestown, NY

NOTE: Asterisk (*) denotes useful responses.

*Signetics, Sacramento, CA
Siemens-Allis Inc., Atlanta, GA
*Sierra Research Corp., Buffalo, NY
*Singer-Kearfott, Wayne, NJ
*Singer-Librascope, Glendale, CA
*Singer-Kearfott, Littlefalls, NJ
Smith Industries, Clearwater, FL
*Sperry-Flight Systems, Phoenix, AZ
*Sperry Gyroscope, Clearwater, FL
*Sperry Marine, Charlottesville, VA
Sperry Systems, Benicia, CA
Sperry Systems, Great Neck, NY
*Sperry Univac, St. Paul, MN
SPIRE Corp., Bedford, MA
SRI International, Menlo Park, CA
*Stromberg Carlson, Longwood, FL
Sunstrand, Rockford, IL
Sylvania Systems, Needham Heights, MA
Syscom Corp., Sunnyvale, CA
Tektronix, Beaverton, OR
Teledyne-Brown, Huntsville, AL
Teledyne Electronics, Newbury Park, CA
Teledyne MEC, Palo Alto, CA
Teledyne-Ryan, San Diego, CA
Teledyne Systems, Northridge, CA
Texas Instruments, Austin, TX
Texas Instruments, Dallas, TX
*Tracor Inc., Austin, TX
*TRW Defense & Space, Redondo Beach, CA
TRW Electronics, Colorado Springs, CO
TRW Equipment, Cleveland, OH
TRW LSI Products, LaJolla, CA

NOTE: Asterisk (*) denotes useful responses.

TRW Semiconductors, Lawndale, CA
Tylan Corp., Torrance, CA
*Unidynamics/Phoenix, Phoenix, AZ
Unidynamics/St. Louis, St. Louis, MO
United Technologies, Windsor Locks, CT
United Technologies, Melville, NY
*Varian, Palo Alto, CA
*VLSI Technology Inc., San Jose, CA
Vought Corp., Dallas, TX
Weitek, Santa Clara, CA
Westinghouse Electric, Sunnyvale, CA
*Westinghouse Electric, Baltimore, MD
Westinghouse Electric, Hunt Valley, MD
Westinghouse Electric, Buffalo, NY
Westinghouse Electric, Pittsburgh, PA
Weston Controls, Archibald, PA
Xerox-Electro Optical, Pasadena, CA
*Zilog Inc., Cambell, CA

NOTE: Asterisk (*) denotes useful responses.

APPENDIX 3.0

LITERATURE SEARCH AND DATA SURVEY

Martin Marietta was required to complete an in-depth, computer assisted literature search, coupled with telephone calls and personal visits to potentially key data sources. The object was to obtain, review and analyze equipment and system manufacturer(s) derating policies, company internal part derating documentation not released for general publication, periodical articles, technical reports, military specifications, and vendor documentation. This data has been published on integrated circuits, semiconductors and advanced technology devices (i.e., VLSI, VHSIC, memory). However, there was little to be found in these particular areas of interest.

The computerized search and library reviews were then supported by a letter survey, a telephone survey, and visits to the most promising data sources to find more information on the vital subjects. The response to these activities exceeded historical experience on similar data surveys (see Table 40). However, it was more an expression of mutual interest than a contribution of useful information. The information received as a result of these efforts has been analyzed and is discussed in the Published Guidelines Analysis of this appendix. Because of the limited information received from industry on derating guidelines and failure mode data for advanced technology devices, an internal letter survey was used. The responses to this survey are summarized in the Martin Marietta Survey portions of this appendix.

TABLE 40. HISTORICAL VERSUS ACTUAL RESULTS OF DATA SURVEYS

Type of Survey	Time Span (Weeks)		Response (Percent)*		Yield (Percent)	
	Historical	Actual	Historical	Actual	Historical	Actual
Letter	12	10	5 - 50	55	2 - 10	35
Telephone	1	1	100	100	20	65
Literature	2 - 12	12	N/A	N/A	25	25
Visits	8	2	100	100	75	72

*Results are based upon experience observed over seven years on six reliability data survey programs conducted at Martin Marietta Orlando Aerospace. The normal response range in letter surveys is 5 to 50 percent.

Literature Search

The literature search was implemented by the Martin Marietta Orlando Aerospace Technical Information Center (TIC). The Center has access to virtually all technical information published during the past ten years. It maintains on-line computer access to more than 100 data bases. In addition to our own files, special emphasis was directed to the files of the

Defense Technical Information Center (DTIC). Because of the relative newness of application of the devices of interest, the search was generally limited to material published in the four years ending December 1982. More recent publications were tracked on a day-to-day basis.

The electronic devices researched as key words are listed in column 1 of Table 40. Additional key words used are listed in Table 41. The computerized search yielded 1037 abstracts, which were reviewed. Only 151 abstracts appeared to be relevant. After review, only 35 of the titles had sufficient merit to be retained. These are included in the bibliography (Appendix 1).

TABLE 41. KEY WORDS

DEVICES	OTHER KEY WORDS
Hybrid	Derating
Transistor	Reliability Derating
Capacitors	Thermal Tests
Resistor Chips	Thermal Testing
Integrated Circuits	Thermal Resistance
LSI/Custom LSI	Junction Temperature
VHSIC	Junction Temperature Measurement
VLSI	Case Temperature
Microprocessors	Case Temperature Measurement
Memory	Temperature
Bipolar	Thermal
MOS	Application Notes
Bubble	Application Guidelines
Microwave	Failure Modes
Silicon Detectors	Failure Mechanisms
Germanium Detectors	
Silicon Schottky Detectors	
Silicon Mixers	
Germanium Mixers	
IMPATT Diodes	
GUNN Diodes	
Varactor Diodes	
PIN Diodes	
Step Recovery Diodes	
Tunnel Diodes	
Transistor	
GaAs FET	
SAW	

Letter Survey

A letter and two-part questionnaire was mailed to 257 addresses at 240 corporate locations, with a return date of 30 May 1983. The mailing list was compiled from the Electronic Industries Association JC-13 technical committee rosters, the Government-Industry Data Exchange Program (GIDEP)

roster, and prospective respondents known by the Rome Air Development Center (RADC) or Martin Marietta to have a vested interest in the subject. The addresses are listed in appendix 2.

There were 90 returns. Eighty-four, or 93 percent of the returns provided useful information. The response to five general survey questions is summarized here.

1 Does your company/division use standard electronics component derating? 71 Yes 19 No

2 Are the component derating guidelines documented? 68 Yes 22 No

3 Does your company/division have standard application guidelines and tolerance factors? 55 Yes 35 No
Documented? 53 Yes 37 No

4 During forthcoming inspection, subsystem, and/or system level testing, are failed parts subject to analysis to determine failure modes and/or mechanisms? 30 Yes 14 No 46 Sometimes

5 Has your company/division performed any thermal tests to verify derating parameters? 44 Yes 46 No

The second page of the survey questionnaire asked the question:

> "Have you conducted, within the past 5 years, any testing (life, screening, demonstrations, etc.) which measured any of the following parameters on the following devices (please check appropriate boxes)."

The number of addressees who responded to this question is summarized in Table 42.

An analysis of the results of the literature search and the letter survey lead to the following conclusions:

1 Of the 10 companies most common in the literature who were queried, only seven responded. Only four of these seven reported conducting testing which measure case or junction temperatures.

2 Only one respondent, Sandia National Laboratories, reported an accumulation of relevant failure rate data.

3 There is very little temperature measurement data available, and most of it resides in five companies. The companies are:

Sperry - Clearwater, Florida
Magnavox - Ft. Wayne, Indiana
Stromberg Carlson - Longwood, Florida
Sierra Research - Buffalo, New York
Hughes Aircraft - Fullerton, California

TABLE 42. TEST MEASUREMENT RESPONSE

DEVICE	TEMPERATURE		FAILURE RATE
	JUNCTION	CASE	
Hybrid	8	18	
Transistors			
Capacitors			
Resistor Chips			
Integrated Circuits			
LSI/Custom LSI	6	13	1
VHSIC	1	3	
VLSI	4	8	
Microprocessors	6	12	1
Memory			
Bipolar	6	12	
MOS	4	12	1
Bubble	1	1	
Microwave			
Silicon Detectors	2	3	
Germanium Detectors	1	1	
Silicon Schottky Detectors	1	3	
Silicon Mixers	1	3	1
Germanium Mixers	1	1	
IMPATT Diodes	2	2	
GUNN Diodes	1	2	1
Varactor Diodes	2	4	1
PIN Diodes	1	5	1
Step Recovery Diodes	1	3	
Tunnel Diodes	1	1	
Transistor	3	4	
GaAs FET	4	6	
SAW	1	2	

Telephone Survey

A telephone survey was used as a follow-up to the letter survey for the purpose of obtaining useful data or information by mail. There were a total of 52 telephone calls. The calls led to the receipt of 33 copies of corporate derating guidelines, and the basis for seven personal visits. Less data was available after contacting the most promising respondents. The telephone survey was terminated after 50 percent of the sources had been contacted.

On-Site Visits

With proper preparation and response, on-site visits are the best source of data. Such visits provided clearer communication and less bias, since fewer misunderstandings in terminology, meanings, or questions can occur. The on-site visit offers the respondent an opportunity to clarify points of doubt, since he has ready access to his organization's data base. Last, but not least, the personal visit tends to assure the respondent's cooperation and his company's approval for the release of data.

Seven visits were made because of a dearth of promised data and practical judgements with respect to fiscal limitations on travel. The results of these trips to Motorola (6/20), Hughes Aircraft (6/21), AIRESEARCH (6/22), Douglas Aircraft (6/21), TRW (6/22), Sierra Research (8/24), and SAWTEC (9/20) were documented in trip reports and sent to RADC by Martin Marietta letters. Four of these sources provided information that was useful in completing Task 3 of the study contract, an assessment of case temperature derating and measurement.

Due to conflicts in data availability and usefulness, the planned and tentatively scheduled trips to additional respondents were cancelled. This was a topic of discussion with RADC, and was documented in the appropriate monthly status reports and the first interim review.

The literature search and data survey provided some very interesting results. The results obtained did not further the progress of the program, but highlighted the point that most everyone contacted was interested. In general, the respondents had little useful information, but wanted some form of consistent or standardized guidance in the field of derating and junction temperatures. Each individual visited or contacted by telephone had their own opinion of how it should be handled, but each was open to a standard requirement in the form of a military specification.

Published Guidelines Analysis

Industry derating guidelines and information were obtained primarily as a result of telephone calls following up the response to the survey letter. Final document sources are listed in Table 43. This is an updated version of the document source listing provided to RADC by the Martin Marietta Orlando Aerospace Interim Report OR 17328 on 15 August 1983.

A total of thirty-three documents were received. Of these, thirty-two had useful derating criteria for semiconductors and integrated circuits. Very few companies had published guidelines for the more advanced technology devices (i.e., LSI, VLSI, VHSIC, etc.) These guidelines were included in the analysis when they were available. The data collected from the derating standards of these companies was analyzed by first grouping the data by part type. Within the part type, the analysis focused on the parameters derated and the amount of derating applied. The derating criteria received from about 90 percent of the respondents was not based on derating levels or operating environments. Therefore, these two elements were not evaluated in the analysis.

TABLE 43. INDUSTRY DERATING GUIDELINES

Bendix-Guidance, Teterboro, New Jersey
Cubic Defense Systems, San Diego, California
Delco Electronics, Goleta, California
Douglas Aircraft, Long Beach, California
E Systems, Falls Church, Virginia
Electrospace Systems, Richardson, Texas
Exxon Corporation, Lionville, Pennsylvania
Ford Aerospace, Palo Alto, California
General Electric Company, Schenectady, New York
Goodyear Aerospace, Akron, Ohio
Gould Incorporated, Glen Burnie, Maryland
Hamilton Standard, Windsor Locks, Connecticut
Harris Corporation, Melbourne, Florida
Hartman Systems, Huntington Station, New York
Honeywell, St. Louis Park, Minnesota
Honeywell, Hopkins, Minnesota
Hughes Aircraft, Fullerton, California
Interstate Electronics, Anaheim, California
Kaiser Electronics, San Jose, California
Lockheed Aircraft, Burbank, California
Lockheed Missile, Sunnyvale, California
Martin Marietta Aerospace, Baltimore, Maryland
Martin Marietta Aerospace, Orlando, Florida
Northrop Corporation, Newbury Park, California
Raytheon Corporation, Bedford, Massachusetts
Raytheon Corporation, Goleta, California
Sierra Research Corporation, Buffalo, New York
Signetics Corporation, Sacramento, California
Sperry Marine, Charlottesville, Virginia
Sperry Flight Systems, Phoenix, Arizona
Texas Instruments, Dallas, Texas
TRW Corporation, Redondo Beach, California
VLSI Technology Corporation, San Jose, California

Tables 44 through 46 represent the tabulated results of the analysis on derating standards for diodes, integrated circuits, and transistors, respectively. On the left hand side of each table are the part types which are derated, along with the number of sources that referenced that part type enclosed in parentheses. The stress parameters are across the top of the tables. These parameters are derated by the majority of the respondents. The value enclosed in parentheses for these parameters indicates the percentage of respondents who derated that parameter for the specific part type. The range of values to which the part is derated, and the percentage of respondents who derate to that value, is presented in descending percentage order. This derating information can be reduced further for the purpose of comparing the industry derating standards and those listed in the "Reliability Part Derating Guidelines Report" (RADC-TR-82-177).

TABLE 44. SURVEY GUIDELINE SUMMARY

DIODES

TYPE	JUNCTION TEMP.	REVERSE VOLTAGE	FORWARD CURRENT	POWER	PEAK SURGE CURR.	VOLTAGE	VOLTAGE TRANSIENT
	(87%)	(81%)	(71%)	(48%)	(48%)		
GENERAL PURPOSE SIGNAL RECTIFIERS SWITCHING (31)	110°C-33% 125°C-26% <100°C-19% 100°C-15% >125°C- 4% 120°C- 3%	.50-44% .70-20% >.70-16% .65-12% .60- 8%	.50-41% .50<x<.75-27% .75-18% .40- 9% .80- 5%	.30-40% .50-40% >.50-20%	.50-47% .75-27% >.75-20% .70- 6%		
	(96%)		(48%)	(64%)			
REGULATORS ZENERS (25)	110°C-33% <110°C-21% 100°C-17% >125°C-17% 125°C- 4% <20°C- 4% 105°C- 4%		.50-25% .50<x<.70-25% .70-25%	.50-69% >.50-19% <.50-12%			
	(88%)	(88%)	(75%)	(63%)	(63%)		
SILICON CONTROLLED RECTIFIER (SCR) (8)	110°C-43% <110°C-43% >110°C-14%	.50-71% >.50-29%	.50-50% .65-33% .60-17%	.50-40% .30-40% .60-20%	>.50-60% .50-40%		
STEP RECOVERY (1)	110°C		.75	.50		.75	.80
SCHOTTKY (1)	110°C			.50		.75	.80
TUNNEL GERMANIUM (1)	75°C			.50		.70	.80

TABLE 45. SURVEY GUIDELINE SUMMARY

MICROCIRCUITS

TYPE	JUNCTION TEMP.	SUPPLY VOLTAGE	OUTPUT CURRENT	INPUT COMMON VOLTAGE	INPUT DIFF VOLTAGE	FAN OUT	OPERATING FREQ	INPUT VOLTAGE
LINEAR (30)	(80%) 110°C-38% 125°C-21% <100°C-21% 100°C-16% 130°C- 4%	(83%) .80-36% .90-20% .85-16% .75-16% .70-12%	(60%) .75-44% .80-28% .70-17% <.70-11%	(43%) .70-46% .80-23% >.80-15% .75- 8% .60- 8%	(38%) .90-38% .85-25% <.85-37%			
DIGITAL (26)	(88%) 110°C-35% 125°C-22% 100°C-17% <100°C-17% 130°C-4.5% TMAX-30°C-4.5%	(58%) BIPOLAR .80-20% ±10%-20% .75-13% ±.5-13% >.80-13% .70- 7% ±5% - 7% 3.5V- 7% MOS .70-50% .85-50%	(23%) BIPOLAR .80-67% .90-33% MOS .70-100%			(54%) BIPOLAR .80-64% .70-21% .75-15% MOS .90-50% .80-50%	(27%) BIPOLAR .75-86% .90-14% MOS .80-100%	
VOLTAGE REGULATOR (14)	(79%) 110°C-45% <110°C-36% >110°C-19%		(79%) .75-45% .80-36% <.75-19%					(93%) .80-77% <.80-15% .85- 8%
HYBRID (4)	(100%) 105°C-50% 110°C-25% .75-25%							

TABLE 46. SURVEY GUIDELINE SUMMARY

TRANSISTORS

TYPE	JUNCTION TEMP	VOLTAGE	CURRENT	POWER
GENERAL PURPOSE (30)	(83%) 110°C-32% 125°C-28% <100°C-20% 100°C-16% >125°C- 4%	(83%) .75-52% .80-16% .70-16% <.70-16%	(70%) .75-52% .50-24% .70-9.5% .80-9.5% .90-5%	(67%) .50-65% >.50-15% .30-15% .40- 5% Power Transistor .30-87% .75-13%
FIELD EFFECT TRANSISTOR (9)	(33%) 110°C-67% 125°C-33%	(89%) .75-38% .60-25% .70-13% .80-12% .50-12%	(70%) .75-50% .65-25% .50-25%	(44%) .65-25% .50-25% .30-25% .20-25%
Ga As FET (2)	(100%) 100°C 125°C	(100%) .75 .70	(50%) .90	(100%) .50 .65

The survey results were condensed to show a single derating value for each part type and stress parameter. The highest percentage of respondents derating by a specific intensity established this single value. Tables 47 through 49 present these values, along with the applicable RADC report derating standards (Levels I, II, and III, respectively) in a tabular format to facilitate a direct comparison.

Further review and analysis of the derating source documentation received has lead to the following conclusions:

1 There is a body of general guidelines on transistors, diodes, resistors, and capacitors that is comparable with the Level I/II guidelines identified by RADC. These guidelines are referenced in Tables 47 through 49.

2 There were some published guidelines for ICs, but none of them addressed VHSIC or VLSI devices.

3 Derating for hybrid microcircuits was scarcely mentioned. As Table 45 indicates, only four companies address it in their guidelines, and then only to derate junction temperature.

TABLE 47. DERATING GUIDELINES COMPARISON SURVEY VERSUS RADC-TR-82-177 DIODES

DIODES

PART TYPE	JUNCTION TEMP.		REVERSE VOLT.		FORWARD CURR.		POWER DISS.		PEAK SURGE CURR.		VOLTAGE		VOLTAGE	
	SURVEY	RADC	SURVEY	RADC	SURVEY	RADC	SURVEY	RADC	SURVEY	RADC	SURVEY	RADC	SURVEY	RADC
GENERAL PURPOSE: SIGNAL SWITCHING	110	95 110 125	50	10 70 70	50	50 65 75	50	50 60 70	50	N/A				
RECTIFIERS	110	95 110 125	50	70 70 70	50	50 65 75	50	N/A	50	N/A				
SCR's	110	95 110 125	50	N/A	50	50 70 70	50	N/A	50	N/A				
REGULATORS ZENERS	110	95 110 125			50	N/A	50	50 60 70						
SCHOTTKY	110	95 110 125					50	50 60 70			75	N/A	80	N/A
STEP RECOVERY VARACTOR	110	N/A			75	N/A	50	N/A			75	N/A	80	N/A
TUNNEL GERMANIUM	110	N/A					50	N/A			75	N/A	80	N/A

NOTE: JUNCTION TEMPERATURE IS EXPRESSED IN °C.

THE OTHER STRESS PARAMETERS ARE EXPRESSED AS THE PERCENT OF THE RATED VALUE.

TABLE 48. DERATING GUIDELINES COMPARISON SURVEY VERSUS RADC-TR-82-177 MICROCIRCUITS

MICROCIRCUITS

PART TYPE	JUNCTION TEMP		SUPPLY VOLT		OUTPUT CURR.		INPUT COMM VOL.		INPUT DIFF VOLT.		FAN OUT		OPERATING FREQ		INPUT VOLT.	
	SURVEY	RADC	SURVEY	RADC	SURVEY	RADC	SURVEY	RADC	SURVEY	RADC	SURVEY	RADC	SURVEY	RADC	SURVEY	RADC
LINEAR	110	80 95 105	80	70 80 80	75	70 80 80	70	N/A	90	N/A					N/A	60 70 70
DIGITAL	110	85 100 110	BIPOLAR ±10%	± 5% ± 5% ± 5%	80	80 90 90					BIPOLAR 80	N/A	BIPOLAR 75	80 90 95		
			MOS 85	70 85 85							MOS 80	N/A	MOS 80	80 80 90		
VOLTAGE REGULATOR	110	80 95 105			75	70 75 80									80	70 80 80
HYBRID	105	85 100 110														

NOTE: JUNCTION TEMPERATURE IS EXPRESSED IN °C

THE OTHER STRESS PARAMETERS ARE EXPRESSED AS THE PERCENT OF THE RATED VALUE.

TABLE 49. DERATING GUIDELINES COMPARISON SURVEY VERSUS RADC-TR-82-177 TRANSISTORS

TRANSISTORS

PART TYPE	JUNCTION TEMP		VOLTAGE		CURRENT		POWER	
	SURVEY	RADC	SURVEY	RADC	SURVEY	RADC	SURVEY	RADC
GENERAL PURPOSE	110	95 110 125	75	60 70 70	75	N/A	50	50 60 70
FET	110	95 110 125	75	60 70 70	75	N/A	50 65	50 60 70
GaAs FET	100 125	95 110 125	70 75	60 70 70	90	N/A	50 65	50 60 70

NOTE: JUNCTION TEMPERATURE IS EXPRESSED IN °C.

THE OTHER STRESS PARAMETERS ARE EXPRESSED AS THE PERCENT OF THE RATED VALUE.

4 Derating for memory devices was not mentioned. There was no derating information for bubble memories in particular.

5 Only silicon devices get any attention of any of the microwave devices listed in the contract statement of work. No one seems to use germanium devices, and they are not selected or recommended for new design. Stress parameters for tunnel germanium diodes were mentioned by only one respondant, with germanium devices in general not being addressed by other sources. Martin Marietta followed the format for derating established by the one respondent.

6 SAW devices were recognized only by the device manufacturers. These devices are relatively new technology and little information is available. However, derating information was received from a device manufacturer.

7 Application guidelines in terms of mission criticality or the MIL-HDBK-217D environments were virtually non-existant in the industrial data.

8 Present derating criteria, i.e. RADC-TR-82-177, appears to be more complete and inclusive than what is used by the industry in general.

9 Structured collection of field data and design analyses performed on existing programs would substantiate or revise present derating criteria.

Martin Marietta Survey

A survey of Martin Marietta electronics experts was conducted to supplement the information received from industry. The objective was to obtain failure mode data and derating guidelines for the specific advanced technology devices this contract addresses (i.e., VLSI, VHSIC, etc.). There was a total of eleven letters and questionnaires mailed, with four responses. Authors of the outstanding surveys were identified and contacted by telephone.

The surveys that were returned did not reveal any additional facts. They confirmed or reinforced what has been previously published on failure modes and derating for ICs, hybrids, and memory devices. As one respondent indicated, specific information on microwave devices was limited, due to the fact that data needed for the creation of derating standards does not exist for these devices. The survey questions and results are summarized in Figures 77 and 78.

Reliability Derating Procedures
Survey

Please complete the following questionnaire by recording the response to the following questions in the chart on the next page. Feel free to make any additional comments/remarks that you consider pertinent or helpful to this task.

1. What would, in your opinion, be the major parameters for derating?

2. What derating value would you suggest for these parameters?

3. What is the predominant failure mode?

4. This failure mode is the result of:

   a. Manufacturing techniques

   b. Device physics

   c. Design application

Figure 77. Martin Marietta survey.

DERATING				
DEVICE	PARAMETER	VALUE	FAILURE MODE	CAUSE (A,B,C)*
HYBRID TRANSISTORS CAPACITORS	SAME AS DISCRETES-DERATING DEPENDS ON APPLI. BREAK-DOWN VOLTAGE JUNCTION TEMP.	20% (TR), 50% (C) 150 C (MAX)	SHORTS	A, C
RESISTOR CHIPS	POWER DISSIPATION	50%	OPENS, R VALUE CHANGE. RARE TO HAVE FAILURE	C
INTEGRATED CIRCUITS LSI/CUSTOM LSI VHSIC VLSI MICROPROCESSORS MEMORY BIPOLAR MOS BUBBLE	JUNCTION TEMP OPER. VOLTAGE TOLERANCE FAN OUT	150 °C (MAX)	SHORTS OPENS LEAKAGE LATCH-UP (SCR)	A, C ATOMIC RADIATION NOISE SPIKES, LACK OF GUARD BARS, INSUFFICIENT SUBSTRATE CONTACTS, LACK OF PROTECTION @ I/O
MICROWAVE SILICON DETECTORS GERM DETECTORS SILICON SCHOTTKY DETECTORS SILICON MIXERS GERM MIXERS	JUNCTION TEMP. POWER	VARIES PER MATERIALS USED, PROCESS TECHNOLOGIES, & THE VENDOR OPERATING SPECS.	METAL MIGRATION SHORTS HERMITICITY PROBLEMS	C TEMP. RELATED
IMPATT DIODES GUNN DIODES VARACTOR DIODES PIN DIODES STEP RECOVERY DIODES TUNNEL DIODES TRANSISTOR GAAS FET	JUNCTION TEMP. VOLTAGE POWER			

SAW

COMMENTS/REMARKS:

*KEY	CAUSE OF FAILURES
A	MANUFACTURING TECHNIQUES
B	DEVICE PHYSICS
C	DESIGN APPLICATION

Figure 77a. Martin Marietta survey results.

APPENDIX 4.0

DATA GROUPING

Data grouping is a significant step in the case temperature derating and measurement task. It consists of two forms, the device grouping versus packaging, and measured or collected temperature data grouping. The device grouping versus packaging types is shown in Table 50.

TABLE 50. DATA GROUPING

Device Group	Studs	Metal Cans	Ceramic Chip Carriers	Cerdip/ Flatpack	Hybrid
Transistors	X	X			
Diodes	X	X			
Integrated circuits		X	X	X	
Microwave	X	X			X
Hybrid		X			X

The device grouping plan versus the package type encompasses the most widely used military devices. Plastic encapsulated package types were not addressed or considered, since they are not approved for miltary equipment. The axial package was not addressed or considered for two basic reasons. First, there is limited future usage of axial packages, according to device manufacture general data. Second, axial packages do not appear to be a particular area of temperature problems, according to survey respondents queried.

The second data grouping considered was the measured or collected data. The data received has been grouped by package type. The generally considered package types are listed against the case outline letter designations shown in Table 51. This listing was extracted from Appendix C of MIL-M-38510E.

TABLE 51. CASE OUTLINE LETTER DESIGNATIONS

Letter 1/	Appendix C Designation	Description 2/
A	F-1	14-lead FP (1/4" x 1/4")
B	F-3	14-lead FP (3/16" x 1/4")
C	D-1	14-lead DIP (1/4" x 3/4")
D	F-2	14-lead FP (1/4" x 3/8")
E	D-2	16-lead DIP (1/4" x 7/8")
F	F-5	16-lead FP (1/4" x 3/8")
G	A-1	8-lead can
H	F-4	10-lead FP (1/4" x 1/4")
I	A-2	10-lead can
J	D-3	24-lead DIP (1/2" x 1-1/4")
K	F-6	24-lead FP (3/8" x 5/8")
M	A-3	12-lead can
P	D-4	8-lead DIP (1/4" x 3/8")
Q	D-5	40-lead DIP (9/16" x 2-1/16")
R	D-8	20-lead DIP (1/4" x 1-1/16")
S	F-9	20-lead FP (1/4" x 1/2")
V	D-6	18-lead DIP (1/4" x 16/16")
W	D-7	22-lead DIP (3/8" x 1-1/8")
	F-8	24-lead FP (1/4" x 3/8")
	C-1	16-terminal SQ, CCP (.300" x .300")
	C-2	20-terminal SQ, CCP (.350" x .350")
	C-3	24-terminal SQ, CCP (.400" x .400")
	C-4	28-terminal SQ, CCP (.450" x .450")
	C-5	44-terminal SQ, CCP (.650" x .650")
	C-6	52-terminal SQ, CCP (.750" x .750")
	C-7	68-terminal SQ, CCP (.950" x .950")
	C-8	84-terminal SQ, CCP (1.150" x 1.150")
	C-9	18-terminal RECT, CCP (.285" x .350")
	C-10	28-terminal RECT, CCP (.285" x .425")
	C-11	28-terminal RECT, CCP (.350" x .550")
	C-12	32-terminal RECT, CCP (.450" x .550")

APPENDIX 5. INTERNAL MODEL

APPENDIX 5.1. Square Surface Program

This appendix contains the computer program for the square surface device. This program is referenced in section 5.3.1.

SQUARE SURFACE DEVICE - 50% DISSIPATION

```
00005 OPEN "LP:" FOR WRITE AS FILE #1
00010 REM              ASSUMPTIONS AND VARIABLE NAMES
00011 REM UNITS FOR LENGTH, WIDTH, & THICKNESS ARE IN MIL INCHES
00012 REM DISSIPATION AREA IS 50%
00014 REM SPREADING ANGLE VARIES PER EXTERNAL ENVIRONMENTS
00020 REM          L=Length W=Width T=Thickness K=Thermal Conductivity
00021 REM          A=Spreading Angle(radians) S=Spreading Angle(degrees)
00022 REM          L1(W1)=Adjusted length(width) for dissipation area
00023 REM          L2(W2)=Length(width) for next level
00024 REM          R1,R2=Thermal Resistance  I=Increment
00025 REM SUBROUTINE VARIABLES: W=Width of field  D=# decimal digits
00026 REM          Q$=formatted output  J,F,O=tab settings
00039 REM                              INPUTS
00040 L=W=T=0
00050 INPUT "ENTER THE MATERIAL TYPE  ";F$
00060 INPUT "ENTER THE THERMAL CONDUCTIVITY IN W/INCH*CENTIGRADE  ";K
00061 INPUT "ENTER THE SPREADING ANGLE IN DEGREES  ";S
00069 REM                            TABLE TITLES
00070 PRINT #1, TAB(21);"SQUARE SURFACE DEVICE-50% DISSIPATION"
00075 PRINT #1, " "
00076 PRINT #1, " "
00077 PRINT #1, " "
00080 PRINT #1, TAB(28);"MATERIAL: ";F$
00081 PRINT #1, TAB(28);"CONDUCTIVITY: ";K;"(W/IN.*C)"
00082 PRINT #1, TAB(28);"SPREADING ANGLE: ";S;"DEGREES"
00083 PRINT #1, " "
00085 PRINT #1, " "
00090 PRINT #1, TAB(12);"  LENGTH * WIDTH     THERMAL RESISTANCE ";
00092 PRINT #1, "   Linc     *     Winc"
00095 PRINT #1, TAB(12);"  ---------------     ------------------ ";
00096 PRINT #1, "   ------------------"
00099 REM                              INCREMENTING
00100 L=2
00105 W=2
00110 IF L<10 THEN I=2
00120 IF (L<50) AND (L>=10) THEN I=5
00121 IF (L<200) AND (L>=50) THEN I=10
00122 IF (L<500) AND (L>=200) THEN I=50
00129 REM                           THICKNESS VARIATION
00130 IF (L<10) OR (W<10) THEN T=6
00140 IF (L<25) AND (L>=10) THEN T=8
00150 IF (L<50) AND (L>=25) THEN T=12
00151 IF (L<100) AND (L>=50) THEN T=15
00152 IF L>=100 THEN T=18
00160 REM                              50% DISSIPATION
00161 L1=.707*L
00162 W1=.707*W
00168 REM                             THERMAL RESISTANCE
00169 A=3.1415927/180*S
00170 R1=T/(L*W1*(W1+2*T*TAN(A)))
00171 R2=R1*1000
00191 REM                    NEXT LEVEL DIMENSIONS (SPREADING)
00192 L2=L1+2*T*TAN(A)
```

SQUARE SURFACE DEVICE - 50% DISSIPATION (CONTINUED)

```
00194 IF L2>L THEN L2=L
00200 GOSUB 800
00205 IF L=500 THEN 420
00370 L=L+I
00380 W=L
00390 GOTO 110
00420 CLOSE #1
00440 END
00490 REM                                   SUBROUTINES
00500 REM                                     OUTPUT
00800 W=5: D=0
00810 V=L: GOSUB 1000: PRINT #1, TAB(14);Q$;TAB(20);"X";TAB(22);Q$;
00820 W=13: D=5: V=R2: GOSUB 1000: PRINT #1, TAB(J);Q$;
00830 W=7:D=2:V=L2:GOSUB 1000:PRINT #1, TAB(F);Q$;TAB(62);"X";TAB(O);Q$
00840 RETURN
00900 REM                                     TABLE FORMAT
01000 IF D=0 THEN 1050
01003 Q=INT(V+.5/(10^D))
01005 C=LEN(STR$(Q))
01010 GOSUB 4000
01011 Q$=LEFT$(STR$(Q),C-1)+"."
01015 Q=INT((V-Q)*(10^D)+.5)
01020 P$=STR$(Q)
01030 M=LEN(P$)
01033 M1=M-1
01035 Q$=Q$+RIGHT$("00000000"+RIGHT$(P$,M1),D+1)
01040 RETURN
01050 Q=INT(V+.5)
01060 Q$=RIGHT$(S$+STR$(Q),W)
01070 RETURN
01080 REM                                TAB SETTINGS FOR TABLE
04000 X=C-2
04010 IF X=1 THEN 4050
04015 IF X=2 THEN 4055
04020 IF X=3 THEN 4060
04025 IF X=4 THEN 4065
04030 IF X=5 THEN 4070
04050 J=37: F=55: O=65: RETURN
04055 J=36: F=54: O=64: RETURN
04060 J=35: F=53: O=63: RETURN
04065 J=34: F=53: O=63: RETURN
04070 J=33: F=53: O=63: RETURN
```

SQUARE SURFACE ATTACHMENT

```
00005 OPEN "LP:" FOR WRITE AS FILE #1
00010 REM                ASSUMPTIONS AND VARIABLE NAMES
00011 REM UNITS FOR LENGTH,WIDTH,& THICKNESS ARE MIL INCHES
00012 REM 100% COVERAGE
00013 REM SPREADING ANGLE VARIES PER EXTERNAL ENVIRONMENTS
00020 REM          L=Length W=Width T=Thickness K=Thermal Conductivity
00021 REM          A=Spreading Angle(radians) S=Spreading Angle(degrees)
00022 REM          L2(W2)=Length(width) for next level   I=Increment
00023 REM          R1,R2= Thermal Resistance
00024 REM SUBROUTINE VARISBLES:W=Width of field  D=# decimal digits
00025 REM          Q$=formatted output  J,F,O=tab settings  Z(L3)=device length
00026 REM          T2=device thickness
00030 REM                              INPUTS
```

SQUARE SURFACE ATTACHMENT (CONTINUED)

```
00040 L=W=T=0
00045 S$="                "
00046 PRINT "ATTACHMENT MATERIAL CHOICES: EUTECTIC, SILVER EPOXY, "
00047 PRINT "GOLD EPOXY, NON-CONDUCTIVE EPOXY, CONDUCTIVE EPOXY, "
00048 PRINT "AND NONE"
00050 INPUT "ENTER THE MATERIAL TYPE:  ";F$
00060 INPUT "ENTER THE THERMAL CONDUCTIVITY IN W/INCH*CENTIGRADE:  ";K
00061 INPUT "ENTER THE SPREADING ANGLE IN DEGREES:  ";S
00069 REM                          TABLE TITLES
00070 PRINT #1, TAB(26);"SQUARE SURFACE ATTACHMENT"
00075 PRINT #1, " "
00076 PRINT #1, " "
00077 PRINT #1, " "
00080 PRINT #1, TAB(26);"MATERIAL : ";F$
00081 PRINT #1, TAB(26);"CONDUCTIVITY: ";K;"(W/IN.*C)"
00082 PRINT #1, TAB(26);"SPREADING ANGLE: ";S;"(DEGREES)"
00083 PRINT #1, " "
00085 PRINT #1, " "
00090 PRINT #1, TAB(12);"  LENGTH * WIDTH     THERMAL RESISTANCE ";
00092 PRINT #1, "   Linc     *     Winc"
00095 PRINT #1, TAB(12);"  ---------------     ------------------ ";
00096 PRINT #1, "   -----------------"
00098 REM                            INCREMENTING
00100 L=2
00105 W=2
00106 Z=2
00110 IF L<10 THEN I=2
00120 IF (L<50) AND (L>=10) THEN I=5
00123 IF (L<200) AND (L>=50) THEN I=10
00125 IF (L<500) AND (L>=200) THEN I=50
00130 GOTO 400
00160 REM                            THERMAL RESISTANCE
00165 A=3.1415927/180*S
00170 R1=T/(K*W*(W+2*T*TAN(A)))
00171 R2=R1*1000
00191 REM                      NEXT LEVEL DIMENSIONS(SPREADING)
00192 L2=L+2*T*TAN(A)
00195 GOSUB 2000
00196 Z=Z+I
00197 GOSUB 800
00205 IF L>=500 THEN 700
00370 L=L+I
00380 W=L
00390 GOTO 110
00400 REM                          ATTACHMENT THICKNESSES
00401 IF F$="EUTECTIC" THEN T=.5
00410 IF F$="SILVER EPOXY" THEN T=.5
00420 IF F$="GOLD EPOXY" THEN T=.5
00430 IF F$="NON-CONDUCTIVE EPOXY" THEN T=2
00440 IF F$="CONDUCTIVE EPOXY" THEN T=1
00450 IF F$="NONE" THEN T=0
00460 GOTO 160
00700 CLOSE #1
00720 END
00750 REM                                SUBROUTINES
00760 REM                                  OUTPUT
00800 W=5: D=0
00810 V=L: GOSUB 1000: PRINT #1, TAB(14);Q$;TAB(20);"X";TAB(22);Q$;
00820 W=13: D=5: V=R2: GOSUB 1000: PRINT #1, TAB(J);Q$;
00830 W=7:D=2:V=L2:GOSUB 1000:PRINT #1, TAB(F);Q$;TAB(62);"X";TAB(O);Q$
00840 RETURN
00900 REM                                TABLE FORMAT
```

SQUARE SURFACE ATTACHMENT (CONTINUED)

```
01000 IF D=0 THEN 1050
01003 Q=INT(V+.5/(10^D))
01005 C=LEN(STR$(Q))
01010 GOSUB 4000
01011 Q$=LEFT$(STR$(Q),C-1)+"."
01015 Q=INT((V-Q)*(10^D)+.5)
01020 P$=STR$(Q)
01030 M=LEN(P$)
01033 M1=M-1
01035 Q$=Q$+RIGHT$("00000000"+RIGHT$(P$,M1),D+1)
01040 RETURN
01050 Q=INT(V+.5)
01060 Q$=RIGHT$(S$+STR$(Q),W)
01070 RETURN
01090 REM                              DEVICE THICKNESS
02000 A=3.1415927/180*S
02010 IF Z<10 THEN T2=6
02020 IF (Z<25) AND (Z>=10) THEN T2=8
02030 IF (Z<50) AND (Z>=25) THEN T2=12
02040 IF (Z<100) AND (Z>=50) THEN T2=15
02050 IF Z>=100 THEN T2=18
02070 Z1=Z*.707: Z2=Z1+2*T2*TAN(A)
02080 IF Z2>Z THEN Z2=Z
02085 Z3=Z-Z2
02087 IF Z3=0 THEN 2095
02088 L3=(Z-2*T2*TAN(A))/.707
02089 Z4=Z: Z=L3: GOSUB 5000: L4=(Z4-2*T3*TAN(A))/.707
02090 IF L2>L4 THEN L2=L4
02092 Z=Z4
02091 RETURN
02095 L2=Z: RETURN
02098 REM                          TAB SETTINGS FOR TABLE
04000 X=C-2
04010 IF X=1 THEN 4050
04015 IF X=2 THEN 4055
04020 IF X=3 THEN 4060
04025 IF X=4 THEN 4065
04030 IF X=5 THEN 4070
04050 J=37: F=55: O=65: RETURN
04055 J=36: F=54: O=64: RETURN
04060 J=35: F=53: O=63: RETURN
04065 J=34: F=53: O=63: RETURN
04070 J=33: F=53: O=63: RETURN
05000 IF Z<10 THEN T3=6
05010 IF (Z<25) AND (Z>=10) THEN T3=8
05020 IF (Z<50) AND (Z>=25) THEN T3=12
05030 IF (Z<100) AND (Z>=50) THEN T3=15
05040 IF Z>=100 THEN T3=18
05050 RETURN
```

SQUARE SURFACE - INTERMEDIATE MATERIAL

```
00005 OPEN "LP:" FOR WRITE AS FILE #1
00010 REM                ASSUMPTIONS AND VARIABLE NAMES
00011 REM UNITS FOR LENGTH, WIDTH, & THICKNESS ARE IN MIL INCHES
00012 REM 100% COVERAGE
00013 REM SPREADING ANGLE VARIES PER EXTERNAL ENVIRONMENTS
00020 REM          L=Length W=Width T=Thickness K=Thermal Conductivity
00021 REM          A=Spreading Angle(radians) S=Spreading Angle(degrees)
00022 REM          L2(W2)=Length(width) for next level    I=Increment
00023 REM          R1,R2=Thermal Resistance
00024 REM SUBROUTINE VARIABLES: W=width of field  D=# decimal digits
00025 REM          Q$=formatted output  J,F,O=tab settings
00030 REM                              INPUTS
00040 L=W=T=0
00041 PRINT "INTERMEDIATE MATERIAL CHOICES: GOLD HEADER, BERYLLIA, "
00042 PRINT "ALUMINA, MOLYTAB, NICKELTAB, AND NONE"
00050 INPUT "ENTER THE MATERIAL TYPE:  ";F$
00060 INPUT "ENTER THE THERMAL CONDUCTIVITY IN W/INCH*CENTIGRADE:  ";K
00061 INPUT "ENTER THE SPREADING ANGLE IN DEGREES:  ";S
00069 REM                            TABLE TITLES
00070 PRINT #1, TAB(23);"SQUARE SURFACE-INTERMEDIATE MATERIAL"
00071 PRINT #1, " "
00072 PRINT #1, " "
00075 PRINT #1, " "
00080 PRINT #1, TAB(27);"MATERIAL: ";F$
00081 PRINT #1, TAB(27);"CONDUCTIVITY: ";K;"(W/IN.*C)"
00082 PRINT #1, TAB(27);"SPREADING ANGLE: ";S;"(DEGREES)"
00085 PRINT #1, " "
00086 PRINT #1, " "
00090 PRINT #1, TAB(12);"  LENGTH * WIDTH     THERMAL RESISTANCE ";
00092 PRINT #1, "   Linc     *    Winc"
00095 PRINT #1, TAB(12);"  ---------------    ------------------ ";
00096 PRINT #1, "   -----------------"
00099 REM                              INCREMENTING
00100 L=2
00105 W=2
00110 IF L<10 THEN I=2
00120 IF (L<50) AND (L>=10) THEN I=5
00121 IF (L<200) AND (L>=50) THEN I=10
00125 IF (L<500) AND (L>=200) THEN I=50
00130 GOTO 400
00165 REM                             THERMAL RESISTANCE
00168 A=3.1415927/180*S
00170 R1=T/(K*W*(W+2*T*TAN(A)))
00172 R2=R1*1000
00191 REM                      NEXT LEVEL DIMENSIONS(SPREADING)
00192 L2=L+2*T*TAN(A)
00193 W2=W+2*T*TAN(A)
00195 GOSUB 800
00205 IF L=500 THEN 420
00370 L=L+I
00380 W=L
00390 GOTO 110
00400 REM                                    THICKNESSES
00401 IF F$="GOLD HEADER" THEN T=.2
00402 IF F$="BERYLLIA" THEN T=0
00403 IF F$="ALUMINA" THEN T=0
00404 IF F$="MOLYTAB" THEN T=0
00405 IF F$="NICKELTAB" THEN T=0
00406 IF F$="NONE" THEN T=0
00407 GOTO 165
```

SQUARE SURFACE - INTERMEDIATE MATERIAL (CONTINUED)

```
00420 CLOSE #1
00440 END
00699 REM                                SUBROUTINES
00700 REM                                  OUTPUT
00800 W=5: D=0
00810 V=L: GOSUB 1000: PRINT #1, TAB(14);Q$;TAB(20);"X";TAB(22);Q$;
00820 W=13: D=5: V=R2: GOSUB 1000: PRINT #1, TAB(J);Q$;
00830 W=7:D=2:V=L2:GOSUB 1000:PRINT #1, TAB(F);Q$;TAB(62);"X";TAB(O);Q$
00840 RETURN
00850 REM                                TABLE FORMAT
01000 IF D=0 THEN 1050
01003 Q=INT(V+.5/(10^D))
01005 C=LEN(STR$(Q))
01010 GOSUB 4000
01011 Q$=LEFT$(STR$(Q),C-1)+"."
01015 Q=INT((V-Q)*(10^D)+.5)
01020 P$=STR$(Q)
01030 M=LEN(P$)
01033 M1=M-1
01035 Q$=Q$+RIGHT$("00000000"+RIGHT$(P$,M1),D+1)
01040 RETURN
01050 Q=INT(V+.5)
01060 Q$=RIGHT$(S$+STR$(Q),W)
01070 RETURN
03999 REM                          TAB SETTINGS FOR TABLE
04000 X=C-2
04010 IF X=1 THEN 4050
04013 IF X=2 THEN 4055
04020 IF X=3 THEN 4060
04025 IF X=4 THEN 4065
04030 IF X=5 THEN 4070
04050 J=37: F=55: O=65: RETURN
04055 J=36: F=54: O=64: RETURN
04060 J=35: F=53: O=63: RETURN
04065 J=34: F=53: O=63: RETURN
04070 J=33: F=53: O=63: RETURN
```

40 PIN CERAMIC SIDE BRAZED PACKAGE

```
00005 OPEN "LP:" FOR WRITE AS FILE #1
00010 REM                    ASSUMPTIONS AND VARIABLE NAMES
00011 REM UNITS FOR LENGTH, WIDTH, & THICKNESS ARE IN MIL INCHES
00012 REM 100% COVERAGE
00013 REM SPREADING ANGLE VARIES PER EXTERNAL ENVIRONMENTS
00020 REM     L=Length W=Width T=Thickness K=Thermal Conductivity
00021 REM     A=Spreading Angle(radians) S=Spreading Angle(degrees)
00022 REM     L2(W2)=length(width) for next level    I=Increment
00023 REM     R1,R2=Thermal Resistance
00024 REM     T1,T2,T4=Thickness for attachment, header,and package respectively
00025 REM SUBROUTINE VARIABLES: W=width of field  D=# decimal digits
00026 REM     Q$=formatted output  J,F,O=tab settings  Z(L1)=device length
00027 REM     T=device thickness
00030 REM                                  INPUTS
00040 L=W=T4=0
00050 INPUT "ENTER THE MATERIAL TYPE:  ";F$
00059 INPUT "ENTER THE THERMAL CONDUCTIVITY IN W/INCH*CENTIGRADE:  ";K
```

40 PIN CERAMIC SIDE BRAZED PACKAGE (CONTINUED)

```
00060 INPUT "ENTER THE SPREADING ANGLE IN DEGREES:  ";S
00061 PRINT " "
00062 PRINT "ATTACHMENT MATERIAL CHOICES: EUTECTIC, SILVER ";
00063 PRINT "EPOXY, GOLD EPOXY,"
00064 PRINT "NON-CONDUCTIVE EPOXY, CONDUCTIVE EPOXY, AND NONE"
00065 INPUT "ENTER THE ATTACHMENT MATERIAL  ";A$
00066 PRINT " "
00067 PRINT "INTERMEDIATE MATERIAL CHOICES: GOLD HEADER,BERYLLIA,ALUMINA,"
00068 PRINT "MOLYTAB,NICKLETAB AND NONE"
00070 INPUT "ENTER THE INTERMEDIATE MATERIAL  ";H$
00073 REM                              TABLE TITLES
00074 PRINT #1, TAB(21);"40-PIN CERAMIC SIDE BRAZED PACKAGE"
00075 PRINT #1, " "
00076 PRINT #1, " "
00077 PRINT #1, " "
00080 PRINT #1, TAB(28);"MATERIAL: ";F$
00081 PRINT #1, TAB(28);"CONDUCTIVITY: ";K;"(W/IN.*C)"
00082 PRINT #1, TAB(28);"SPREADING ANGLE: ";S;"(DEGREES)"
00083 PRINT #1, TAB(28);"ATTACHMENT MATERIAL: ";A$
00084 PRINT #1, TAB(28);"INTERMEDIATE MATERIAL: ";H$
00085 PRINT #1, " "
00087 PRINT #1, " "
00090 PRINT #1, TAB(12);"  LENGTH * WIDTH     THERMAL RESISTANCE ";
00092 PRINT #1, "   Linc     *     Winc"
00095 PRINT #1, TAB(12);"  ---------------     ------------------- ";
00096 PRINT #1, "   ------------------"
00098 REM                                INCREMENTING
00099 Z=2
00100 L=2
00105 W=2
00110 IF L<10 THEN I=2
00120 IF (L<50) AND (L>=10) THEN I=5
00121 IF (L<200) AND (L>=50) THEN I=10
00122 IF (L<500) AND (L>=200) THEN I=50
00125 REM                               THICKNESS VARIATION
00129 GOTO 402
00130 IF (L1<10) OR (W1<10) THEN T4=52
00140 IF (L1<25) AND (L1>=10) THEN T4=49
00150 IF (L1<50) AND (L1>=25) THEN T4=46
00151 IF (L1<100) AND (L1>=50) THEN T4=42
00152 IF L1>=100 THEN T4=40
00167 REM                               THERMAL RESISTANCE
00168 A=3.1415927/180*S
00170 R1=T4/(K*W*(W+2*T4*TAN(A)))
00171 R2=R1*1000
00191 REM                        NEXT LEVEL DIMENSIONS(SPREADING)
00192 L2=L+2*T4*TAN(A)
00193 W2=W+2*T4*TAN(A)
00199 GOSUB 800
00205 IF L=500 THEN 429
00370 L=L+I
00380 W=L
00390 GOTO 110
00400 REM                          THICKNESS OF PREVIOUS LEVELS
00402 IF H$="GOLD HEADER" THEN T2=.2
00403 IF H$="BERYLLIA" THEN T2=0
00404 IF H$="ALUMINA" THEN T2=0
00405 IF H$="MOLYTAB" THEN T2=0
00406 IF H$="NICKLETAB" THEN T2=0
00407 IF H$="NONE" THEN T2=0
00408 IF A$="EUTECTIC" THEN T1=.5
00409 IF A$="SILVER EPOXY" THEN T1=.5
00410 IF A$="GOLD EPOXY" THEN T1=.5
```

40 PIN CERAMIC SIDE BRAZED PACKAGE (CONTINUED)

```
00411 IF A$="NON-CONDUCTIVE EPOXY" THEN T1=2
00412 IF A$="CONDUCTIVE EPOXY" THEN T1=1
00413 IF A$="NONE" THEN T1=0
00415 GOSUB 2000
00416 Z=Z+I
00417 GOTO 130
00429 CLOSE #1
00440 END
00500 REM                                   SUBROUTINES
00550 REM                                     OUTPUT
00800 W=5: D=0
00810 V=L: GOSUB 1000: PRINT #1, TAB(14);Q$;TAB(20);"X";TAB(22);Q$;
00820 W=13: D=5:V=R2: GOSUB 1000: PRINT #1, TAB(J);Q$;
00830 W=7:D=2:V=L2:GOSUB 1000:PRINT #1, TAB(F);Q$;TAB(62);"X";TAB(O);Q$
00840 RETURN
00900 REM                                   TABLE FORMAT
01000 IF D=0 THEN 1050
01003 Q=INT(V+.5/(10^D))
01005 C=LEN(STR$(Q))
01010 GOSUB 4000
01011 Q$=LEFT$(STR$(Q),C-1)+"."
01015 Q=INT((V-Q)*(10^D)+.5)
01020 P$=STR$(Q)
01030 M=LEN(P$)
01033 M1=M-1
01035 Q$=Q$+RIGHT$("00000000"+RIGHT$(P$,M1),D+1)
01040 RETURN
01050 Q=INT(V+.5)
01060 Q$=RIGHT$(S$+STR$(Q),W)
01070 RETURN
01999 REM                                 DEVICE THICKNESS
02000 A=3.1415927/180*S: IF Z<10 THEN T=6
02005 IF (Z<25) AND (Z>=10) THEN T=8
02010 IF (Z<50) AND (Z>=25) THEN T=12
02015 IF (Z<100) AND (Z>=50) THEN T=15
02020 IF Z>=100 THEN T=18
02025 Z1=Z*.707: Z2=Z1+2*T*TAN(A): IF Z2>Z THEN 2095
02030 L1=(Z-(2*(T1+T2+T)*TAN(A)))/.707: RETURN
02095 L1=(Z-(2*(T1+T2)*TAN(A)))/.707: RETURN
02098 REM                              TAB SETTINGS FOR TABLES
04000 X=C-2
04010 IF X=1 THEN 4050
04015 IF X=2 THEN 4055
04020 IF X=3 THEN 4060
04025 IF X=4 THEN 4065
04030 IF X=5 THEN 4070
04050 J=37: F=55: O=65: RETURN
04055 J=36: F=54: O=64: RETURN
04060 J=35: F=53: O=63: RETURN
04065 J=34: F=53: O=63: RETURN
04070 J=33: F=53: O=63: RETURN
```

APPENDIX 5.2. Rectangular Surface Programs

This appendix contains the computer program for the square surface device. This program is referenced in section 5.3.2.

RECTANGULAR SURFACE DEVICE - 50% DISSIPATION

```
00005 OPEN "LP:" FOR WRITE AS FILE #1
00010 REM                    ASSUMPTIONS AND VARIABLE NAMES
00011 REM UNITS FOR LENGTH, WIDTH,& THICKNESS ARE IN MIL INCHES
00012 REM SPREADING ANGLE VARIES PER EXTERNAL ENVIRONMENTS
00013 REM DISSIPATION AREA IS 50%
00020 REM       L=Length W=Width T=Thickness K=Thermal Conductivity
00021 REM       A=Spreading Angle(radians)  S=Spreading Angle(degrees)
00022 REM       L1(W1)=Adjusted length(width) for dissipation area
00023 REM       L2(W2)=Length(width) for next level  I=Increment
00024 REM       R1,R2,R3,R4=Thermal Resistance
00025 REM SUBROUTINE VARIABLES: W5=Width of field  D=# of decimal digits
00026 REM       V=Function  Q$=formatted output  J,F,O=tab settings
00039 REM                                  INPUTS
00040 L=W=T=0
00050 INPUT "ENTER THE MATERIAL TYPE  ";F$
00060 INPUT "ENTER THE THERMAL CONDUCTIVITY IN W/INCH*CENTIGRADE  ";K
00061 INPUT "ENTER THE SPREADING ANGLE IN DEGREES  ";S
00069 REM                                TABLE TITLES
00070 PRINT #1, TAB(18);"RECTANGULAR SURFACE DEVICE-50% DISSIPATION"
00071 PRINT #1, " "
00072 PRINT #1, " "
00075 PRINT #1, " "
00080 PRINT #1, TAB(28);"MATERIAL: ";F$
00081 PRINT #1, TAB(28);"CONDUCTIVITY: ";K;"(W/IN.*C)"
00082 PRINT #1, TAB(28);"SPREADING ANGLE: ";S;"(DEGREES)"
00085 PRINT #1, " "
00087 PRINT #1, " "
00090 PRINT #1, TAB(12);"  LENGTH * WIDTH     THERMAL RESISTANCE ";
00092 PRINT #1, "   Linc     *     Winc"
00095 PRINT #1, TAB(12);"  ---------------     ------------------- ";
00096 PRINT #1, "   ------------------"
00099 REM                                INCREMENTING
00100 L=2
00105 W=2
00110 IF L<10 THEN I=2
00120 IF (L<50) AND (L>=10) THEN I=5
00121 IF (L<200) AND (L>=50) THEN I=10
00123 IF (L<500) AND (L>=200) THEN I=50
00129 REM                              THICKNESS VARIATION
00130 IF (L<10) OR (W<10) THEN T=6
00140 IF (L<25) AND (L>=10) THEN T=8
00150 IF (L<50) AND (L>=25) THEN T=12
00151 IF (L<100) AND (L>=50) THEN T=15
00152 IF L>=100 THEN T=18
00159 W=W+I
00160 REM                                50% DISSIPATION
00161 L1=.707*L
00162 W1=.707*W
00168 REM                              THERMAL RESISTANCE
00169 A=3.1415927/180*S
00170 R1=1/(2*K*TAN(A)*(L1-W1))
00180 R2=(L1/W1)*((2*T*TAN(A)+W1)/(2*T*TAN(A)+L1))
00190 R3=LOG(R2)
00191 R4=R1*R3*1000
00193 REM                      NEXT LEVEL DIMENSIONS(SPREADING)
```

RECTANGULAR SURFACE DEVICE - 50% DISSIPATION (CONTINUED)

```
00194 L2=L1+2*T*TAN(A)
00195 W2=W1+2*T*TAN(A)
00196 IF L2>L THEN L2=L
00197 IF W2>W THEN W2=W
00198 GOSUB 800
00199 REM                                   TABLE INCREMENTING
00205 IF L=500 THEN 420
00206 IF L>=100 THEN 400
00330 IF (L<100) AND (W+I>L*3) THEN 370
00340 GOTO 110
00370 L=L+I
00380 W=L
00390 GOTO 110
00400 IF (L>=100) AND (W+I>L*1.5) THEN 370
00410 GOTO 110
00420 CLOSE #1
00440 END
00500 REM                                SUBROUTINES
00600 REM                                  OUTPUT
00800 W5=5: D=0
00810 V=L: GOSUB 1000: PRINT #1, TAB(14);Q$;TAB(20);"X";
00815 V=W: GOSUB 1000: PRINT #1, TAB(22);Q$;
00820 W5=13: D=5: V=R4: GOSUB 1000: PRINT #1, TAB(J);Q$;
00830 W5=7: D=2: V=L2: GOSUB 1000: PRINT #1, TAB(F);Q$; TAB(62): "X";
00835 V=W2: GOSUB 1000: PRINT #1, TAB(O);Q$
00840 RETURN
00900 REM                                TABLE FORMAT
01000 IF D=0 THEN 1050
01003 Q=INT(V+.5/(10^D))
01005 C=LEN(STR$(Q))
01010 GOSUB 4000
01011 Q$=LEFT$(STR$(Q),C-1)+"."
01015 Q=INT((V-Q)*(10^D)+.5)
01020 P$=STR$(Q)
01030 M1=LEN(P$)-1
01035 Q$=Q$+RIGHT$("00000000"+RIGHT$(P$,M1),D+1)
01040 RETURN
01050 Q=INT(V+.5)
01060 Q$=RIGHT$(S$+STR$(Q),W5)
01070 RETURN
01080 REM                          TAB SETTINGS FOR TABLES
04000 X=C-2
04010 IF X=1 THEN 4050
04015 IF X=2 THEN 4055
04020 IF X=3 THEN 4060
04025 IF X=4 THEN 4065
04030 IF X=5 THEN 4070
04050 J=37: F=55: O=65: RETURN
04055 J=36: F=54: O=64: RETURN
04060 J=35: F=53: O=63: RETURN
04065 J=34: F=53: O=63: RETURN
04070 J=33: F=53: O=63: RETURN
```

RECTANGULAR SURFACE ATTACHMENT

```
00005 OPEN "LP:" FOR WRITE AS FILE #1
00010 REM                    ASSUMPTIONS AND VARIABLE NAMES
00011 REM UNITS FOR LENGTH, WIDTH, AND THICKNESS ARE IN MIL INCHES
00012 REM 100% COVERAGE
00013 REM SPREADING ANGLE VARIES WITH EXTERNAL ENVIRONMENTS
00020 REM           L=Length W=Width T=Thickness K=Thermal Conductivity
00021 REM           A=Spreading Angle(radians)  S=Spreading Angle(degrees)
00022 REM           L2(W2)=Length(width) for next level   I=Increment
00023 REM           R1,R2,R3,R4=Thermal Resistance
00024 REM SUBROUTINE VARIABLES:W5=Width of field  D=# of decimal digits
00025 REM           V=function  Q$=formatted output  F,J,O=tab settings
00026 REM           Z=device length  T2=device thickness
00039 REM                              INPUT
00040 L=W=T=0
00045 S$="             "
00046 PRINT "ATTACHMENT MATERIAL CHOICES: EUTECTIC, SILVER EPOXY, "
00047 PRINT "GOLD EPOXY, NON-CONDUCTIVE EPOXY, CONDUCTIVE EPOXY, "
00048 PRINT "AND NONE"
00050 INPUT "ENTER THE MATERIAL TYPE  ";F$
00060 INPUT "ENTER THE THERMAL CONDUCTIVITY IN W/INCH*CENTIGRADE  ";K
00065 INPUT "ENTER THE SPREADING ANGLE IN DEGREES  ";S
00069 REM                           TABLE TITLES
00070 PRINT #1, TAB(24);"RECTANGULAR SURFACE ATTACHMENT"
00075 PRINT #1, " "
00076 PRINT #1, " "
00077 PRINT #1, " "
00080 PRINT #1, TAB(28);"MATERIAL: ";F$
00081 PRINT #1, TAB(28);"CONDUCTIVITY: ";K;"(W/IN.*C)"
00082 PRINT #1, TAB(28);"SPREADING ANGLE: ";S;"(DEGREES)"
00085 PRINT #1, " "
00087 PRINT #1, " "
00090 PRINT #1, TAB(12);"  LENGTH * WIDTH     THERMAL RESISTANCE ";
00092 PRINT #1, "   Linc     *    Winc"
00095 PRINT #1, TAB(12);"  ---------------     ------------------ ";
00096 PRINT #1, "   ------------------"
00099 REM                              INCREMENTING
00100 L=2
00105 W=2
00106 Z=2: Y=2
00110 IF L<10 THEN I=2
00120 IF (L<50) AND (L>=10) THEN I=5
00121 IF (L<200) AND (L>=50) THEN I=10
00123 IF (L<500) AND (L>=200) THEN I=50
00130 GOTO 500
00160 W=W+I
00168 REM                           THERMAL RESISTANCE
00169 A=3.1415927/180*S
00170 R1=1/(2*K*TAN(A)*(L-W))
00180 R2=(L/W)*((2*T*TAN(A)+W)/(2*T*TAN(A)+L))
00190 R3=LOG(R2)
00191 R4=R1*R3*1000
00192 REM                      NEXT LEVEL DIMENSIONS(SPREADING)
00193 L2=L+2*T*TAN(A)
00194 W2=W+2*T*TAN(A)
00195 GOSUB 2000
00196 IF Z>=100 THEN 199
00197 IF (Z<100) AND (Y+I>Z*3) THEN 201
00198 GOTO 202
00199 IF (Z>=100) AND (Y+I>Z*1.5) THEN 201
00200 GOTO 202
```

RECTANGULAR SURFACE ATTACHMENT (CONTINUED)

```
00201 Z=Z+I: Y=Z
00202 GOSUB 800
00204 REM                                   TABLE INCREMENTING
00205 IF L=500 THEN 700
00206 IF L>=100 THEN 400
00330 IF (L<100) AND (W+I>L*3) THEN 370
00340 GOTO 110
00370 L=L+I
00380 W=L
00390 GOTO 110
00400 IF (L>=100) AND (W+I>L*1.5) THEN 370
00410 GOTO 110
00490 REM                                 ATTACHMENT THICKNESSES
00500 IF F$="EUTECTIC" THEN T=.5
00510 IF F$="SILVER EPOXY" THEN T=.5
00520 IF F$="GOLD EPOXY" THEN T=.5
00530 IF F$="NON-CONDUCTIVE EPOXY" THEN T=2
00540 IF F$="CONDUCTIVE EPOXY" THEN T=1
00550 IF F$="NONE" THEN T=0
00560 GOTO 160
00700 CLOSE #1
00720 END
00740 REM                                       SUBROUTINES
00750 REM                                         OUTPUT
00800 W5=5: D=0
00810 V=L: GOSUB 1000: PRINT #1, TAB(14);Q$;TAB(20);"X";
00815 V=W: GOSUB 1000: PRINT #1, TAB(22);Q$;
00820 W5=13: D=5: V=R4: GOSUB 1000: PRINT #1, TAB(J);Q$;
00830 W5=7: D=2: V=L2: GOSUB 1000: PRINT #1, TAB(F);Q$;TAB(62); "X";
00835 V=W2: GOSUB 1000: PRINT #1, TAB(O);Q$
00840 RETURN
00900 REM                                       TABLE FORMAT
01000 IF D=0 THEN 1050
01003 Q=INT(V+.5/(10^D))
01005 C=LEN(STR$(Q))
01010 GOSUB 4000
01011 Q$=LEFT$(STR$(Q),C-1)+"."
01015 Q=INT((V-Q)*(10^D)+.5)
01020 P$=STR$(Q)
01030 M1=LEN(P$)-1
01035 Q$=Q$+RIGHT$("00000000"+RIGHT$(P$,M1),D+1)
01040 RETURN
01050 Q=INT(V+.5)
01060 Q$=RIGHT$(S$+STR$(Q),W5)
01070 RETURN
01090 REM                                     DEVICE THICKNESS
02000 A=3.1415927/180*S
02010 IF Z<10 THEN T2=6
02020 IF (Z<25) AND (Z>=10) THEN T2=8
02030 IF (Z<50) AND (Z>=25) THEN T2=12
02040 IF (Z<100) AND (Z>=50) THEN T2=15
02050 IF Z>=100 THEN T2=18
02055 Y=Y+I
02060 Z1=Z*.707: Y1=Y*.707: Z2=Z1+2*T2*TAN(A): Y2=Y1+2*T2*TAN(A)
02065 IF Z2>Z THEN Z2=Z
02066 IF Y2>Y THEN Y2=Y
02068 Z3=Z-Z2: Y3=Y-Y2
02070 IF Z3=0 THEN 2095
02072 L3=(Z-2*T2*TAN(A))/.707
02074 Z4=Z: Z=L3: GOSUB 3000: L4=(Z4-2*T3*TAN(A))/.707
```

RECTANGULAR SURFACE ATTACHMENT (CONTINUED)

```
02076 IF L2>L4 THEN L2=L4
02078 Z=Z4
02080 IF Y3=0 THEN 2096
02082 W3=(Y-2*T2*TAN(A))/.707
02084 IF W2>W3 THEN W2=W3
02086 RETURN
02095 L2=Z: GOTO 2080
02096 W2=Y: RETURN
03000 IF Z<10 THEN T3=6
03010 IF (Z<25) AND (Z>=10) THEN T3=8
03020 IF (Z<50) AND (Z>=25) THEN T3=12
03030 IF (Z<100) AND (Z>=50) THEN T3=15
03040 IF Z>=100 THEN T3=18
03050 RETURN
03999 REM                                   TAB SETTINGS FOR TABLE
04000 X=C-2
04010 IF X=1 THEN 4050
04015 IF X=2 THEN 4055
04020 IF X=3 THEN 4060
04025 IF X=4 THEN 4065
04030 IF X=5 THEN 4070
04050 J=37: F=55: O=65: RETURN
04055 J=36: F=54: O=64: RETURN
04060 J=35: F=53: O=63: RETURN
04065 J=34: F=53: O=63: RETURN
04070 J=33: F=53: O=63: RETURN
```

RECTANGULAR SURFACE - INTERMEDIATE MATERIAL

```
00005 OPEN "LP:" FOR WRITE AS FILE #1
00010 REM                   ASSUMPTIONS AND VARIABLE NAMES
00011 REM UNITS FOR LENGTH, WIDTH, AND THICKNESS ARE IN MIL INCHES
00012 REM SPREADING ANGLE VARIES PER EXTERNAL ENVIRONMENT
00013 REM 100% COVERAGE
00020 REM            L=Length W=Width T=Thickness K=Thermal Conductivity
00021 REM            A=Spreading Angle(radians)  S=Spreading Angle(degrees)
00022 REM            L2(W2)= Length(width) for next level  I=Increment
00023 REM            R1,R2,R3,R4,=Thermal Resistance
00024 REM SUBROUTINE VARIABLES:W5=Width of field  D=# of decimal digits
00025 REM            V=function  O$=formatted output  J,F,O=tab settings
00030 REM                              INPUTS
00040 L=W=T=0
00045 PRINT "INTERMEDIATE MATERIAL CHOICES: GOLD HEADER, BERYLLIA, "
00046 PRINT "ALUMINA, MOLYTAB, NICKELTAB, AND NONE"
00050 INPUT "ENTER THE MATERIAL TYPE  ";F$
00060 INPUT "ENTER THE THERMAL CONDUCTIVITY IN W/INCH*CENTIGRADE  ";K
00065 INPUT "ENTER THE SPREADING ANGLE IN DEGREES  ";S
00069 REM                           TABLE TITLES
00070 PRINT #1, TAB(19);"RECTANGULAR SURFACE-INTERMEDIATE MATERIAL"
00072 PRINT #1, " "
00073 PRINT #1, " "
00075 PRINT #1, " "
00080 PRINT #1, TAB(28);"MATERIAL: ";F$
00081 PRINT #1, TAB(28);"CONDUCTIVITY: ";K;"(W/IN,*C)"
00082 PRINT #1, TAB(28);"SPREADING ANGLE: ";S;"(DEGREES)"
00085 PRINT #1, " "
00087 PRINT #1, " "
00090 PRINT #1, TAB(12);"  LENGTH * WIDTH     THERMAL RESISTANCE ";
00092 PRINT #1, "   Linc     *     Winc"
00095 PRINT #1, TAB(12);"  ---------------     ------------------ ";
```

RECTANGULAR SURFACE - INTERMEDIATE MATERIAL (CONTINUED)

```
00096 PRINT #1, "   -----------------"
00099 REM                                  INCREMENTING
00100 L=2
00105 W=2
00110 IF L<10 THEN I=2
00120 IF (L<50) AND (L>=10) THEN I=5
00121 IF (L<200) AND (L>=50) THEN I=10
00123 IF (L<500) AND (L>=200) THEN I=50
00130 GOTO 411
00160 W=W+I
00161 REM                                THERMAL RESISTANCE
00162 A=3.1415927/180*S
00170 R1=1/(2*K*TAN(A)*(L-W))
00180 R2=(L/W)*((2*T*TAN(A)+W)/(2*T*TAN(A)+L))
00190 R3=LOG(R2)
00191 R4=R1*R3*1000
00192 REM                          NEXT LEVEL DIMENSIONS(SPREADING)
00193 L2=L+2*T*TAN(A)
00194 W2=W+2*T*TAN(A)
00195 GOSUB 800
00204 REM                                  TABLE INCREMENTING
00205 IF L=500 THEN 420
00206 IF L>=100 THEN 400
00330 IF (L<100) AND (W+I>L*3) THEN 370
00340 GOTO 110
00370 L=L+I
00380 W=L
00390 GOTO 110
00400 IF (L>=100) AND (W+I>L*1.5) THEN 370
00409 GOTO 110
00410 REM                                    THICKNESSES
00411 IF F$="GOLD HEADER" THEN T=.2
00412 IF F$="BERYLLIA" THEN T=0
00413 IF F$="ALUMINA" THEN T=0
00414 IF F$="MOLYTAB" THEN T=0
00415 IF F$="NICKELTAB" THEN T=0
00416 IF F$="NONE" THEN T=0
00417 GOTO 160
00420 CLOSE #1
00440 END
00500 REM                                    SUBROUTINES
00550 REM                                      OUTPUT
00800 W5=5: D=0
00810 V=L: GOSUB 1000: PRINT #1, TAB(14);Q$;TAB(20);"X";
00815 V=W: GOSUB 1000: PRINT #1, TAB(22);Q$;
00820 W5=13: D=5: V=R4: GOSUB 1000: PRINT #1, TAB(J);Q$;
00830 W5=7: D=2: V=L2: GOSUB 1000: PRINT #1, TAB(F);Q$;TAB(62);"X";
00835 V=W2: GOSUB 1000: PRINT #1, TAB(O);Q$
00840 RETURN
00950 REM                                    TABLE FORMAT
01000 IF D=0 THEN 1050
01003 Q=INT(V+.5/(10^D))
01005 C=LEN(STR$(Q))
01010 GOSUB 4000
01011 Q$=LEFT$(STR$(Q),C-1)+"."
01015 Q=INT((V-Q)*(10^D)+.5)
01020 P$=STR$(Q)
01030 M1=LEN(P$)-1
01035 Q$=Q$+RIGHT$("00000000"+RIGHT$(P$,M1),D+1)
01040 RETURN
01050 Q=INT(V+.5)
01060 Q$=RIGHT$(S$+STR$(Q),W5)
01070 RETURN
```

RECTANGULAR SURFACE - INTERMEDIATE MATERIAL (CONTINUED)

```
03999 REM                                TAB SETTINGS FOR TABLES
04000 X=C-2
04010 IF X=1 THEN 4050
04015 IF X=2 THEN 4055
04020 IF X=3 THEN 4060
04025 IF X=4 THEN 4065
04030 IF X=5 THEN 4070
04050 J=37: F=55: 0=65: RETURN
04055 J=36: F=54: 0=64: RETURN
04060 J=35: F=53: 0=63: RETURN
04065 J=34: F=53: 0=63: RETURN
04070 J=33: F=53: 0=63: RETURN
```

RECTANGULAR - 40 PIN CERAMIC SIDE BRAZED PACKAGE

```
00005 OPEN "LP:" FOR WRITE AS FILE #1
00010 REM                    ASSUMPTIONS AND VARIABLE NAMES
00011 REM UNITS FOR LENGTH, WIDTH, AND THICKNESSS ARE IN MIL INCHES
00012 REM SPREADING ANGLE VARIES PER EXTERNAL ENVIRONMENT
00020 REM       L=Length W=Width T=Thickness K=Thermal Conductivity
00021 REM       A=Spreading Angle(radians)  S=Spreading Angle(degrees)
00022 REM       L2(W2)=Length(width) for next level  I=Increment
00023 REM       R1,R2,R3,R4=Thermal Resistance
00024 REM       T1,T2,T4=Thickness for attachment,header,and package respectively
00025 REM SUBROUTINE VARIABLES:W5= Width of field  D=# of decimal digits
00026 REM       V=function  Q$=formatted output  Z(L1)=device length
00027 REM       T=device thickness
00030 REM                                INPUTS
00040 L=W=T4=0
00045 INPUT "ENTER THE MATERIAL TYPE  ";F$
00050 INPUT "ENTER THE THERMAL CONDUCTIVITY IN W/INCH*CENTIGRADE  ";K
00055 INPUT "ENTER THE SPREADING ANGLE IN DEGREES  ";S
00060 PRINT " "
00061 PRINT "ATTACHMENT MATERIAL CHOICES: EUTECTIC, SILVER "
00062 PRINT "EPOXY, GOLD EPOXY, NON-CONDUCTIVE EPOXY, "
00063 PRINT "CONDUCTIVE EPOXY, AND NONE"
00064 INPUT "ENTER THE ATTACHMENT MATERIAL:  ";A$
00065 PRINT " "
00066 PRINT "INTERMEDIATE MATERIAL CHOICES: GOLD HEADER, BERYLLIA, "
00067 PRINT "ALUMINA, MOLYTAB, NICKELTAB, AND NONE"
00068 INPUT "ENTER THE INTERMEDIATE MATERIAL:  ";H$
00069 REM                            TABLE TITLES
00070 PRINT #1, TAB(16);"RECTANGULAR-40 PIN CERAMIC SIDE BRAZED PACKAGE"
00071 PRINT #1, " "
00072 PRINT #1, " "
00075 PRINT #1, " "
00080 PRINT #1, TAB(28);"MATERIAL: ";F$
00081 PRINT #1, TAB(28);"CONDUCTIVITY: ";K;"(W/IN.*C)"
00082 PRINT #1, TAB(28);"SPREADING ANGLE: ";S;"(DEGREES)"
00083 PRINT #1, TAB(28);"ATTACHMENT MATERIAL: ";A$
00084 PRINT #1, TAB(28);"INTERMEDIATE MATERIAL: ";H$
00085 PRINT #1, " "
00087 PRINT #1, " "
00090 PRINT #1, TAB(12);"  LENGTH * WIDTH     THERMAL RESISTANCE ";
00092 PRINT #1, "   Linc     *     Winc"
00095 PRINT #1, TAB(12);"  ---------------     ------------------ ";
00098 PRINT #1, "   ------------------"
00099 REM                            INCREMENTING
00100 L=2
00105 W=2
```

RECTANGULAR - 40 PIN CERAMIC SIDE BRAZED PACKAGE (CONTINUED)

```
00106 Z=2
00110 IF L<10 THEN I=2
00120 IF (L<50) AND (L>=10) THEN I=5
00121 IF (L<200) AND (L>=50) THEN I=10
00123 IF (L<500) AND (L>=200) THEN I=50
00125 REM                              THICKNESS VARIATION
00129 GOTO 411
00130 IF (L1<10) OR (W1<10) THEN T4=52
00140 IF (L1<25) AND (L1>=10) THEN T4=49
00150 IF (L1<50) AND (L1>=25) THEN T4=46
00151 IF (L1<100) AND (L1>=50) THEN T4=42
00152 IF L1>=100 THEN T4=40
00160 W=W+I
00162 REM                                THERMAL RESISTANCE
00165 A=3.1415927/180*S
00170 R1=1/(2*K*TAN(A)*(L-W))
00180 R2=(L/W)*((2*T4*TAN(A)+W)/(2*T4*TAN(A)+L))
00190 R3=LOG(R2)
00191 R4=C1*R3*1000
00192 REM                          NEXT LEVEL DIMENSIONS(SPREADING)
00193 L2=L+2*T4*TAN(A)
00194 W2=W+2*T4*TAN(A)
00199 GOSUB 800
00200 REM                                  TABLE INCREMENTING
00205 IF L=500 THEN 435
00206 IF L>=100 THEN 400
00330 IF (L<100) AND (W+I>L*3) THEN 370
00340 GOTO 110
00370 L=L+I
00380 W=L
00385 Z=Z+I
00390 GOTO 110
00400 IF (L>=100) AND (W+I>L*1.5) THEN 370
00410 GOTO 110
00411 REM                              THICKNESS OF PREVIOUS LEVELS
00412 IF H$="GOLD HEADER" THEN T2=.2
00413 IF H$="BERYLLIA" THEN T2=0
00414 IF H$="ALUMINA" THEN T2=0
00415 IF H$="MOLYTAB" THEN T2=0
00416 IF H$="NICKELTAB" THEN T2=0
00417 IF H$="NONE" THEN T2=0
00420 IF A$="EUTECTIC" THEN T1=.5
00421 IF A$="SILVER EPOXY" THEN T1=.5
00422 IF A$="GOLD EPOXY" THEN T1=.5
00423 IF A$="NON-CONDUCTIVE EPOXY" THEN T1=2
00424 IF A$="CONDUCTIVE EPOXY" THEN T1=1
00425 IF A$="NONE" THEN T1=0
00430 GOSUB 2000
00433 GOTO 130
00435 CLOSE #1
00440 END
00500 REM                                    SUBROUTINES
00550 REM                                      OUTPUT
00800 W5=5: D=0
00810 V=L: GOSUB 1000: PRINT #1, TAB(14);Q$;TAB(20);"X";
00815 V=W: GOSUB 1000: PRINT #1, TAB(22);Q$;
00820 W5=13: D=5: V=R4: GOSUB 1000: PRINT #1, TAB(J);Q$;
00830 W5=7: D=2: V=L2: GOSUB 1000: PRINT #1, TAB(F);Q$;TAB(62);"X";
00835 V=W2: GOSUB 1000: PRINT #1, TAB(O);Q$
00840 RETURN
00900 REM                                    TABLE FORMAT
01000 IF D=0 THEN 1050
```

RECTANGULAR - 40 PIN CERAMIC SIDE BRAZED PACKAGE (CONTINUED)

```
01003 Q=INT(V+.5/(10^D)) .
01005 C=LEN(STR$(Q))
01010 GOSUB 4000
01011 Q$=LEFT$(STR$(Q),C-1)+"."
01015 Q=INT((V-Q)*(10^D)+.5)
01020 P$=STR$(Q)
01030 M1=LEN(P$)-1
01035 Q$=Q$+RIGHT$("00000000"+RIGHT$(P$,M1),D+1)
01040 RETURN
01050 Q=INT(V+.5)
01060 Q$=RIGHT$(S$+STR$(Q),W5)
01070 RETURN
01999 REM                                   DEVICE THICKNESS
02000 A=3.1415927/180*S: IF Z<10 THEN T=6
02005 IF (Z<25) AND (Z>=10) THEN T=8
02010 IF (Z<50) AND (Z>=25) THEN T=12
02015 IF (Z<100) AND (Z>=50) THEN T=15
02020 IF Z>=100 THEN T=18
02025 Z1=Z*.707: Z2=Z1+2*T*TAN(A): IF Z2>Z THEN 2095
02030 L1=(Z-(2*(T1+T2+T)*TAN(A)))/.707: RETURN
02095 L1=Z-2*T2*TAN(A): RETURN
02098 REM                                TAB SETTINGS FOR TABLES
04000 X=C-2
04010 IF X=1 THEN 4050
04015 IF X=2 THEN 4055
04020 IF X=3 THEN 4060
04025 IF X=4 THEN 4065
04030 IF X=5 THEN 4070
04050 J=37: F=55: O=65: RETURN
04055 J=36: F=54: O=64: RETURN
04060 J=35: F=53: O=63: RETURN
04065 J=34: F=53: O=63: RETURN
04070 J=33: F=53: O=63: RETURN
```

APPENDIX 5.3. Circular Surface Programs

This appendix contains the computer program for the circular surface device. This program is referenced in section 5.3.3.

CIRCULAR SURFACE DEVICE

```
00005 OPEN "LP:" FOR WRITE AS FILE #1
00010 REM                    ASSUMPTIONS AND VARIABLE NAMES
00011 REM    UNITS FOR DIAMETER, THICKNESS, AND RADIUS ARE IN MIL INCHES
00012 REM    DISSIPATION AREA IS: 100%
00013 REM    SPREADING ANGLE VARIES PER EXTERNAL ENVIRONMENT
00020 REM         D=DIAMETER T=THICKNESS K=THERMAL CONDUCTIVITY
00021 REM         A=SPREADING ANGLE(RADIANS)  S= SPREADING ANGLE(DEGREES)
00022 REM         I=INCREMENTS  R=RADIUS  R2,R3=THERMAL RESISTANCE
00023 REM         R4=NEXT LEVEL DIMENSIONS DUE TO SPREADING
00024 REM    SUBROUTINE VARIABLES: W=WIDTH OF FIELD  D=# DECIMAL DIGITS
00025 REM         Q$=FORMATTED OUTPUT  J,F,O=TAB SETTINGS
00030 REM                              INPUTS
00040 D=T=0
00050 INPUT "ENTER THE MATERIAL TYPE:  ";F$
00060 INPUT "ENTER THE THERMAL CONDUCTIVITY IN W/INCH*CENTIGRADE:  ";K
00065 INPUT "ENTER THE SPREADING ANGLE IN DEGREES:  ";S
00066 REM                            TABLE TITLES
00070 PRINT #1, TAB(28);"CIRCULAR SURFACE DEVICE"
00075 PRINT #1, " "
00076 PRINT #1, " "
00077 PRINT #1, " "
00080 PRINT #1, TAB(26);"MATERIAL: ";F$
00081 PRINT #1, TAB(26);"CONDUCTIVITY: ";K;"(W/IN.*C)"
00082 PRINT #1, TAB(26);"SPREADING ANGLE: ";S;"(DEGREES)"
00083 PRINT #1, " "
00085 PRINT #1, " "
00090 PRINT #1, TAB(14);"  DIAMETER    THERMAL RESISTANCE    RADIUS(inc)  "
00095 PRINT #1, TAB(14);"  --------    ------------------    -----------  "
00099 REM                           INCREMENTING
00100 D=1
00110 IF D<10 THEN I=1
00120 IF (D<50) AND (D>=10) THEN I=2
00125 REM                             THICKNESS
00130 T=D/15
00155 REM                           THERMAL RESISTANCE
00156 A=3.1415927/180*S
00160 R=D/2
00170 R2=(1/(K*3.1415927*TAN(A)))*(1/R-1/(R+T*TAN(A)))
00172 R3=R2*1000
00175 REM                    NEXT LEVEL DIMENSIONS(SPREADING)
00180 R4=R+T*TAN(A)
00190 IF R4>D THEN R4=D
00200 GOSUB 800: REM PRINT #1,TAB(18);D;TAB(32);R3;TAB(51);R4
00202 REM                             TABLE FORMAT
00205 IF D=50 THEN 225
00210 D=D+I
00220 GOTO 110
00225 CLOSE #1
00230 END
00500 REM                          SUBROUTINES
00550 REM                            OUTPUT
00800 W=4: D3=0
00810 V=D: GOSUB 1000: PRINT #1, TAB(18);Q$;
00820 W=11: D3=4: V=R3: GOSUB 1000: PRINT #1, TAB(J);Q$;
00830 W=6: D3=2: V=R4: GOSUB 1000: PRINT #1, TAB(F);Q$
```

CIRCULAR SURFACE DEVICE (CONTINUED)

```
00840 RETURN
00900 REM                              TABLE FORMAT
01000 IF D3=0 THEN 1050
01003 Q=INT(V+.5/(10^D3))
01005 C=LEN(STR$(Q))
01010 GOSUB 4000
01011 Q$=LEFT$(STR$(Q),C-1)+"."
01015 Q=INT((V-Q)*(10^D3)+.5)
01020 P$=STR$(Q)
01030 M1=LEN(P$)-1
01035 Q$=Q$+RIGHT$("00000000"+RIGHT$(P$,M1),D3+1)
01040 RETURN
01050 Q=INT(V+.5)
01060 Q$=RIGHT$(S$+STR$(Q),W)
01070 RETURN
01080 REM                          TAB SETTINGS FOR TABLE
04000 X=C-2
04010 IF X=1 THEN 4050
04015 IF X=2 THEN 4055
04020 IF X=3 THEN 4060
04025 IF X=4 THEN 4065
04050 J=34: F=53: RETURN
04055 J=33: F=52: RETURN
04060 J=32: F=51: RETURN
04065 J=31: F=50: RETURN
```

CIRCULAR SURFACE METALLIZATION - PLATINUM

```
00005 OPEN "LP:" FOR WRITE AS FILE #1
00010 REM                      ASSUMPTIONS AND VARIABLE NAMES
00011 REM    UNITS FOR RADIUS AND THICKNESS ARE IN MIL INCHES
00012 REM    100% COVERAGE
00013 REM    SPREADING ANGLE VARIES WITH THE EXTERNAL ENVIRONMENT
00020 REM           R=RADIUS T=THICKNESS K=THERMAL CONDUCTIVITY
00021 REM           A=SPREADING ANGLE(RADIANS)  S=SPREADING ANGLE(DEGREES)
00022 REM           I=INCREMENTS  R2,R3=THERMAL RESISTANCE
00023 REM           R4=RADIUS FOR NEXT LEVEL
00024 REM    SUBROUTINE VARIABLES: W=WIDTH OF FIELD   D=# DECIMAL DIGITS
00025 REM           Q$=FORMATTED OUTPUT  J,F,Q=TAB SETTINGS
00035 REM                                INPUTS
00040 R=T=0
00050 INPUT "ENTER THE MATERIAL TYPE:  "iF$
00060 INPUT "ENTER THE THERMAL CONDUCTIVITY IN W/INCH*C[illegible]/GRADE:  "iK
00065 INPUT "ENTER THE SPREADING ANGLE IN DEGREES:  "iS
00067 REM                              TABLE TITLES
00070 PRINT #1, TAB(20)i"CIRCULAR SURFACE METALLIZATION-PLATINUM"
00071 PRINT #1, " "
00072 PRINT #1, " "
00075 PRINT #1, " "
00080 PRINT #1, TAB(26)i"MATERIAL: "iF$
00081 PRINT #1, TAB(26)i"CONDUCTIVITY: "iKi"(W/IN.*C)"
00082 PRINT #1, TAB(26)i"SPREADING ANGLE: "iSi"(DEGREES)"
00084 PRINT #1, " "
00085 PRINT #1, " "
00090 PRINT #1, TAB(14)i"  RADIUS      THERMAL RESISTANCE      RADIUS(inc)  "
00095 PRINT #1, TAB(14)i"  ------      ------------------      -----------  "
00099 REM                            INCREMENTING
00100 R=1
00110 IF R<10 THEN I=1
00120 IF (R<50) AND (R>=10) THEN I=2
00125 REM                              THICKNESS
```

CIRCULAR SURFACE METALLIZATION - PLATINUM (CONTINUED)

```
00130 T=.008
00135 REM                                THERMAL RESISTANCE
00165 A=3.1415927/180*S
00170 R2=(1/(K*3.1415927*TAN(A)))*(1/R-1/(R+T*TAN(A)))
00175 R3=R2*1000
00177 REM                          NEXT LEVEL DIMENSIONS(SPREADING)
00180 R4=R+T*TAN(A)
00199 REM                                    OUTPUT
00200 GOSUB 800
00202 REM                                  TABLE FORMAT
00205 IF R=50 THEN 225
00210 R=R+I
00220 GOTO 110
00225 CLOSE #1
00230 END
00500 REM                                  SUBROUTINES
00550 REM                                    OUTPUT
00800 W=4: D=0
00810 V=R: GOSUB 1000: PRINT #1, TAB(18);Q$;
00820 W=11: D=4: V=R3: GOSUB 1000: PRINT #1, TAB(J);Q$;
00830 W=6: D=2: V=R4: GOSUB 1000: PRINT #1, TAB(F);Q$
00840 RETURN
00900 REM                                  TABLE FORMAT
01000 IF D=0 THEN 1050
01003 Q=INT(V+.5/(10^D))
01005 C=LEN(STR$(Q))
01010 GOSUB 4000
01011 Q$=LEFT$(STR$(Q),C-1)+"."
01015 Q=INT((V-Q)*(10^D)+.5)
01020 P$=STR$(Q)
01030 M1=LEN(P$)-1
01035 Q$=Q$+RIGHT$("00000000"+RIGHT$(P$,M1),D+1)
01040 RETURN
01050 Q=INT(V+.5)
01060 Q$=RIGHT$(S$+STR$(Q),W)
01070 RETURN
01080 REM                          TAB SETTINGS FOR TABLE
04000 X=C-2
04010 IF X=1 THEN 4050
04015 IF X=2 THEN 4055
04020 IF X=3 THEN 4060
04035 IF X=4 THEN 4065
04050 J=34: F=53: RETURN
04055 J=33: F=52: RETURN
04060 J=32: F=51: RETURN
04065 J=31: F=50: RETURN
```

CIRCULAR SURFACE METALLIZATION - TITANIUM

```
00005 OPEN "LP:" FOR WRITE AS FILE #1
00010 REM                    ASSUMPTIONS AND VARIABLE NAMES
00011 REM     UNITS FOR RADIUS AND THICKNESS ARE IN MIL INCHES
00012 REM     100% COVERAGE
00013 REM     SPREADING ANGLE VARIES PER EXTERNAL ENVIRONMENT
00020 REM          R=RADIUS T=THICKNESS K=THERMAL CONDUCTIVITY
00021 REM          A=SPREADING ANGLE(RADIANS)  S=SPREADING ANGLE(DEGREES)
00022 REM          I=INCREMENTS  R2,R3=THERMAL RESISTANCE
00023 REM          R4=RADIUS FOR NEXT LEVEL
00024 REM     SUBROUTINE VARIABLES: W=WIDTH OF FIELD  D=# DECIMAL DIGITS
00025 REM          Q$=FORMATTED OUTPUT  J,F,O=TAB SETTINGS
00035 REM                              INPUTS
00040 R=T=0
00050 INPUT "ENTER THE MATERIAL TYPE:  ";F$
00060 INPUT "ENTER THE THERMAL CONDUCTIVITY IN W/INCH*CENTIGRADE:  ";K
00065 INPUT "ENTER THE SPREADING ANGLE:  ";S
00067 REM                            TABLE TITLES
00070 PRINT #1, TAB(20);"CIRCULAR SURFACE METALLIZATION-TITANIUM"
00071 PRINT #1, " "
00072 PRINT #1, " "
00075 PRINT #1, " "
00080 PRINT #1, TAB(28);"MATERIAL: ";F$
00081 PRINT #1, TAB(28);"CONDUCTIVITY: ";K;"(W/IN.*C)"
00082 PRINT #1, TAB(28);"SPREADING ANGLE: ";S;"(DEGREES)"
00083 PRINT #1, " "
00085 PRINT #1, " "
00090 PRINT #1, TAB(14);"  RADIUS      THERMAL RESISTANCE      RADIUS(inc)  "
00095 PRINT #1, TAB(14);"  ------      ------------------      -----------  "
00099 REM                               INCREMENTING
00100 R=1
00110 IF R<10 THEN I=1
00120 IF (R<50) AND (R>=10) THEN I=2
00125 REM                                 THICKNESS
00130 T=.009
00135 REM                              THERMAL RESISTANCE
00165 A=3.1415927/180*S
00170 R2=(1/(K*3.1415927*TAN(A)))*(1/R-1/(R+T*TAN(A)))
00175 R3=R2*1000
00180 R4=R+T*TAN(A)                 NEXT LEVEL DIMENSIONS(SPREADING)
00190 REM                                  OUTPUT
00200 GOSUB 800
00202 REM                                TABLE TITLES
00205 IF R=50 THEN 225
00210 R=R+I
00220 GOTO 110
00225 CLOSE #1
00230 END
00500 REM                            SUBROUTINES
00550 REM                              OUTPUT
00800 W=4: D=0
00810 V=R: GOSUB 1000: PRINT #1, TAB(18);Q$;
00820 W=11: D=4: V=R3: GOSUB 1000: PRINT #1, TAB(J);Q$;
00830 W=6: D=2: V=R4: GOSUB 1000: PRINT #1, TAB(F); Q$
00840 RETURN
00900 REM                            TABLE FORMAT
01000 IF D=0 THEN 1050
01002 O=INT(V+.5/(10 D))
01005 C=LEN(STR$(O))
01010 GOSUB 4000
```

CIRCULAR SURFACE METALLIZATION - TITANIUM (CONTINUED)

```
01011 Q$=LEFT$(STR$(Q),C-1)+"."
01015 Q=INT((V-Q)*(10^D)+.5)
01020 P$=STR$(Q)
01030 M1=LEN(P$)-1
01035 Q$=Q$+RIGHT$("00000000"+RIGHT$(P$,M1),D+1)
01040 RETURN
01050 Q=INT(V+.5)
01060 Q$=RIGHT$(S$+STR$(Q),W)
01070 RETURN
01080 REM                          TAB SETTINGS FOR TABLES
04000 X=C-2
04010 IF X=1 THEN 4050
04015 IF X=2 THEN 4055
04020 IF X=3 THEN 4060
04025 IF X=4 THEN 4065
04050 J=34: F=53: RETURN
04055 J=33: F=52: RETURN
04060 J=32: F=51: RETURN
04065 J=31: F=50: RETURN
```

CIRCULAR SURFACE - GOLD PLATE

```
00005 OPEN "LP:" FOR WRITE AS FILE #1
00010 REM                    ASSUMPTIONS AND VARIABLE NAMES
00011 REM    UNITS FOR RADIUS AND THICKNESS ARE IN MIL INCHES
00012 REM    100% COVERAGE
00013 REM    SPREADING ANGLE VARIES WITH THE EXTERNAL ENVIRONMENT
00020 REM          R=RADIUS T=THICKNESS K=THERMAL CONDUCTIVITY
00021 REM          A=SPREADING ANGLE(RADIANS)  S=SPREADING ANGLE(DEGREES)
00022 REM          I=INCREMENTS  R2,R3=THERMAL RESISTANCE
00023 REM          R4=RADIUS FOR NEXT LEVEL
00024 REM    SUBROUTINE VARIABLES: W=WIDTH OF FIELD  D=# DECIMAL DIGITS
00025 REM          Q$=FORMATTED OUTPUT  J,F,O=TAB SETTINGS
00030 REM                              INPUTS
00040 R=T=0
00050 INPUT "ENTER THE MATERIAL TYPE:  ";F$
00060 INPUT "ENTER THE THERMAL CONDUCTIVITY IN W/INCH*CENTIGRADE:  ";K
00065 INPUT "ENTER THE SPREADING ANGLE IN DEGREES:  ";S
00069 REM                             TABLE TITLES
00070 PRINT #1, TAB(26);"CIRCULAR SURFACE-GOLD PLATE"
00071 PRINT #1, " "
00072 PRINT #1, " "
00075 PRINT #1, " "
00080 PRINT #1, TAB(28);"MATERIAL: ";F$
00081 PRINT #1, TAB(28);"CONDUCTIVITY: ";K;"(W/IN.*C)"
00082 PRINT #1, TAB(28);"SPREADING ANGLE: ";S;"(DEGREES)"
00083 PRINT #1, " "
00085 PRINT #1, " "
00090 PRINT #1, TAB(14);"  RADIUS      THERMAL RESISTANCE      RADIUS(inc)  "
00095 PRINT #1, TAB(14);"  ------      ------------------      -----------  "
00099 REM                            INCREMENTING
00100 R=1
00110 IF R<10 THEN I=1
00120 IF (R<50) AND (R>=10) THEN I=2
00125 REM                              THICKNESS
00130 T=.079
00160 REM                           THERMAL RESISTANCE
00165 A=3.1415927/180*S
00170 R2=(1/(K*3.1415927*TAN(A)))*(1/R-1/(R+T*TAN(A)))
```

CIRCULAR SURFACE - GOLD PLATE (CONTINUED)

```
00175 R3=R2*1000
00177 REM                          NEXT LEVEL DIMENSIONS(SPREADING)
00180 R4=R+T*TAN(A)
00190 REM                                    OUTPUT
00200 GOSUB 800
00203 REM                                 TABLE FORMAT
00205 IF R=50 THEN 225
00210 R=R+I
00220 GOTO 110
00225 CLOSE #1
00230 END
00500 REM                              SUBROUTINES
00550 REM                                OUTPUT
00800 W=4: D=0
00810 V=R: GOSUB 1000: PRINT #1, TAB(18);Q$;
00820 W=11: D=4: V=R3: GOSUB 1000: PRINT #1, TAB(J);Q$;
00830 W=6: D=2: V=R4: GOSUB 1000: PRINT #1, TAB(F);Q$
00840 RETURN
00900 REM                              TABLE FORMAT
01000 IF D=0 THEN 1050
01003 Q=INT(V+.5/(10^D))
01005 C=LEN(STR$(Q))
01010 GOSUB 4000
01011 Q$=LEFT$(STR$(Q),C-1)+"."
01015 Q=INT((V-Q)*(10^D)+.5)
01020 P$=STR$(Q)
01030 M1=LEN(P$)-1
01035 Q$=Q$+RIGHT$("00000000"+RIGHT$(P$,M1),D+1)
01040 RETURN
01050 Q=INT(V+.5)
01060 Q$=RIGHT$(SPACE$+STR$(Q),W)
01070 RETURN
01080 REM                        TAB SETTINGS FOR TABLE
04000 X=C-2
04010 IF X=1 THEN 4050
04015 IF X=2 THEN 4055
04020 IF X=3 THEN 4060
04025 IF X=4 THEN 4065
04050 J=34: F=53: RETURN
04055 J=33: F=52: RETURN
04060 J=32: F=51: RETURN
04065 J=31: F=50: RETURN
```

CIRCULAR SURFACE HEAT SINK - COPPER

```
00005 OPEN "LP:" FOR WRITE AS FILE #1
00010 REM                    ASSUMPTIONS AND VARIABLE NAMES
00011 REM     UNITS FOR RADIUS AND THICKNESS ARE IN MIL INCHES
00012 REM     100% COVERAGE
00013 REM     SPREADING ANGLE VARIES PER EXTERNAL ENVIRONMENT
00020 REM          R=RADIUS T=THICKNESS K=THERMAL CONDUCTIVITY
00021 REM          A=SPREADING ANGLE(RADIANS)  S=SPREADING ANGLE(DEGREES)
00023 REM          I=INCREMENTS  R2,R3=THERMAL RESISTANCE
00024 REM          R4=RADIUS FOR NEXT LEVEL
00025 REM     SUBROUTINE VARIABLES: W=WIDTH OF FIELD  D=# DECIMAL DIGITS
00026 REM          Q$=FORMATTED OUTPUT  J,F,O=TAB SETTINGS
00030 REM                                  INPUTS
00040 D=T=0
00050 INPUT "ENTER THE MATERIAL TYPE  ";F$
00060 INPUT "ENTER THE THERMAL CONDUCTIVITY IN W/INCH*CENTIGRADE  ";K
00065 INPUT "ENTER THE SPREADING ANGLE IN DEGREES  ";S
00066 INPUT "ENTER THE HEAT SINK THICKNESS IN MIL INCHES";T
00069 REM                                TABLE TITLES
00070 PRINT #1, TAB(23);"CIRCULAR SURFACE HEAT SINK-COPPER"
00075 PRINT #1, " "
00076 PRINT #1, " "
00077 PRINT #1, " "
00080 PRINT #1, TAB(28);"MATERIAL: ";F$
00081 PRINT #1, TAB(28);"CONDUCTIVITY: ";K;"(W/IN.*C)"
00082 PRINT #1, TAB(28);"SPREADING ANGLE: ";S;"(DEGREES)"
00083 PRINT #1, TAB(28);"HEAT SINK THICKNESS: ";T;"(MIL IN.)"
00088 PRINT #1, " "
00089 PRINT #1, " "
00090 PRINT #1, TAB(14);"  RADIUS      THERMAL RESISTANCE      RADIUS(INC)  "
00095 PRINT #1, TAB(14);"  ------      ------------------      -----------  "
00099 REM                                  INCREMENTING
00100 R=1
00110 IF R<10 THEN I=1
00120 IF (R<50) AND (R>=10) THEN I=2
00130 REM                                THERMAL RESISTANCE
00135 A=3.1415927/180*S
00170 R2=(1/(K*3.1415927*TAN(A)))*(1/R-1/(R+T*TAN(A)))
00175 R3=R2*1000
00177 REM                          NEXT LEVEL DIMENSIONS(SPREADING)
00180 R4=R+T*TAN(A)
00190 REM                                  OUTPUT
00200 GOSUB 900
00202 REM                                TABLE FORMAT
00205 IF R=50 THEN 225
00210 R=R+I
00220 GOTO 110
00225 CLOSE #1
00230 END
00500 REM                          SUBROUTINES
00510 REM                            OUTPUT
00800 W=6: D=0
00810 V=R: GOSUB 1000: PRINT #1, TAB(10);Q$;
00820 W=11: D=4: V=R3: GOSUB 1000: PRINT #1, TAB(J);Q$;
00830 W=6: D=2: V=R4: GOSUB 1000: PRINT #1, TAB(F);Q$
00840 RETURN
00900 REM                          TABLE FORMAT
01000 IF D=0 THEN 1050
01002 O=INT(V+.5/(10^D))
01005 Q$=LEFT$(STR$(O),
01010 GOSUB 4000
```

CIRCULAR SURFACE HEAT SINK - COPPER (CONTINUED)

```
01011 Q$=LEFT$(STR$(Q),C-1)+"."
01015 Q=INT((V-Q)*(10^D)+.5)
01020 P$=STR$(Q)
01030 M1=LEN(P$)-1
01035 Q$=Q$+RIGHT$("00000000"+RIGHT$(P$,M1),D+1)
01040 RETURN
01050 Q=INT(V+.5)
01060 Q$=RIGHT$(S$+STR$(Q),W)
01070 RETURN
01080 REM                          TAB SETTINGS FOR TABLES
04000 X=C-2
04010 IF X=1 THEN 4050
04015 IF X=2 THEN 4055
04020 IF X=3 THEN 4060
04025 IF X=4 THEN 4065
04050 J=34: F=53: RETURN
04055 J=33: F=52: RETURN
04060 J=32: F=51: RETURN
04065 J=31: F=50: RETURN
```

APPENDIX 5.4

Spreading Angle Analysis

The internal heat spreading angle has a significant impact on thermal resistance, from the chip junction to the case bottom (θ_{JC}). The internal model employs the spreading angle in the computation of the thermal resistance at each level of device construction by allowing the model user to specify the angle desired. There are many variables, such as attachment voids, chip size, dissipation area, material type and thickness, all which affect the heat spreading function. This creates difficulty in specifying one angle that typically represents the heat spread.

An analysis based on the comparison of the internal model, the external node, and the measurement data was conducted. The purpose of the analysis was to determine the spreading angle for a specific chip. The device modeled for this analysis was the one involved in the circuit board test with an ambient air of 25°C and a lower level of 1 watt. Several iterations of the internal model were made to determine the predicted thermal resistance, from junction to case, for a range of spreading angles range of 0 to 89.9 degrees. The results are represented in Figure 78. As expected, an inverse relationship exists between the spreading angle and θ_{JC}. As the spreading angle increases, θ_{JC} decreases. These predicted values were then compared to the measured θ_{JC} values recorded for the seven devices mounted on the circuit board (ambient air = 25°C and power = 1 watt). This comparison is summarized in Table 52. The table shows evidence that the measured θ_{JC} values fall above the values in the predicted range. Using the side-brazed external nodal model, the predicted θ_{JC} value for the specified measurement conditions is 0.31 degrees centigrade per watt. This value falls within the internal model prediction. However, it does not compare with the measured values.

Based on this analysis, it was concluded that the correct spreading angle could not be determined. The spreading function is an important factor that needs consideration when developing models. However, further investigation was not possible, due to program limitations.

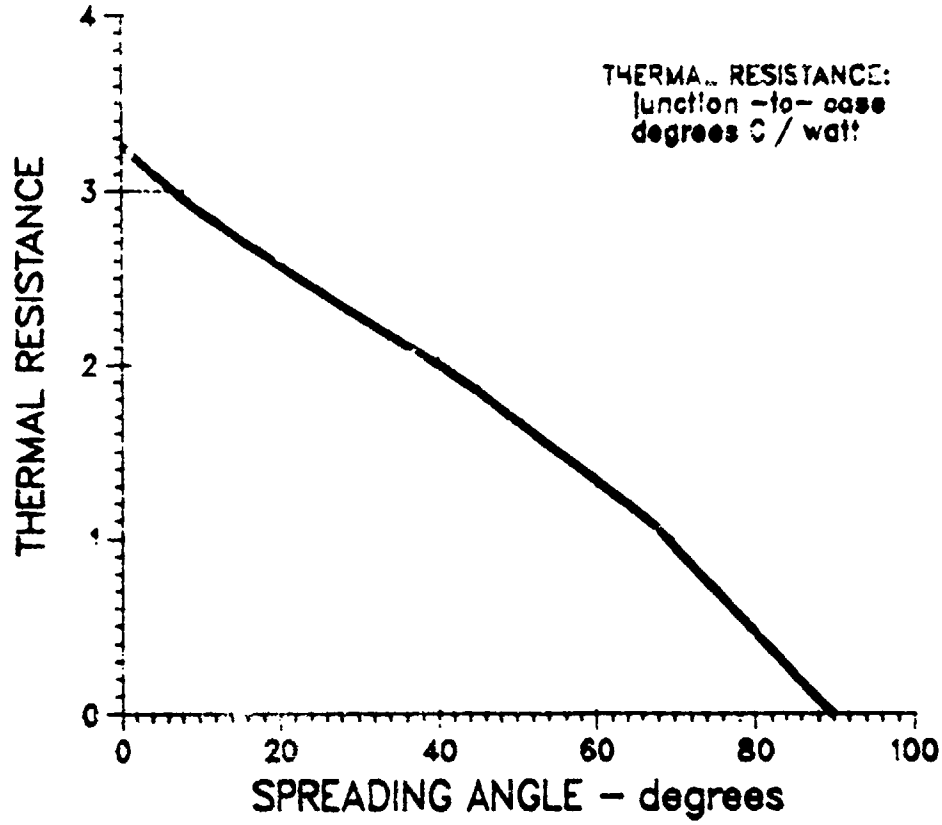


Figure 78. Internal Model Predicted Thermal Resistance Spreading Angle versus Thermal Resistance 40 Pin Side Brazed Dip Package

TABLE 52. INTERNAL MODEL PREDICTION VERSUS CIRCUIT BOARD MEASUREMENT DATA

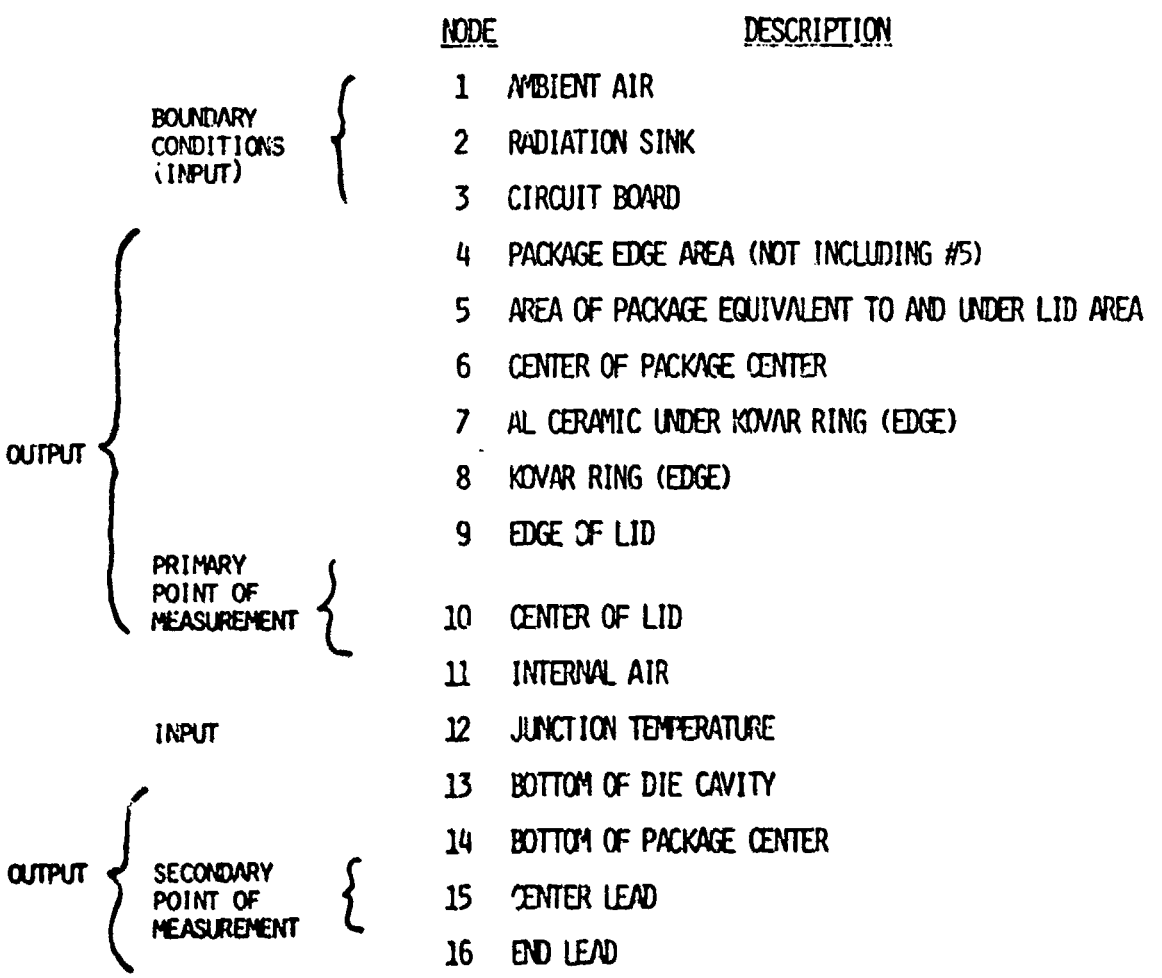
Predicted θ_{JC} for Spreading Angle Variations		Measured θ_{JC} of Seven Devices
Spreading Angle (degrees)	Predicted θ_{JC} (degrees centigrade per watt)	θ_{JC} Measured (degrees centigrade per watt)
0	3.25	9.33
8	2.96	8.82
12.5	2.81	10.58
22	2.52	9.50
40	2.00	11.87
45	1.85	7.25
67	1.10	6.32
89.9	0.002	Average θ_{JC} = 9.10

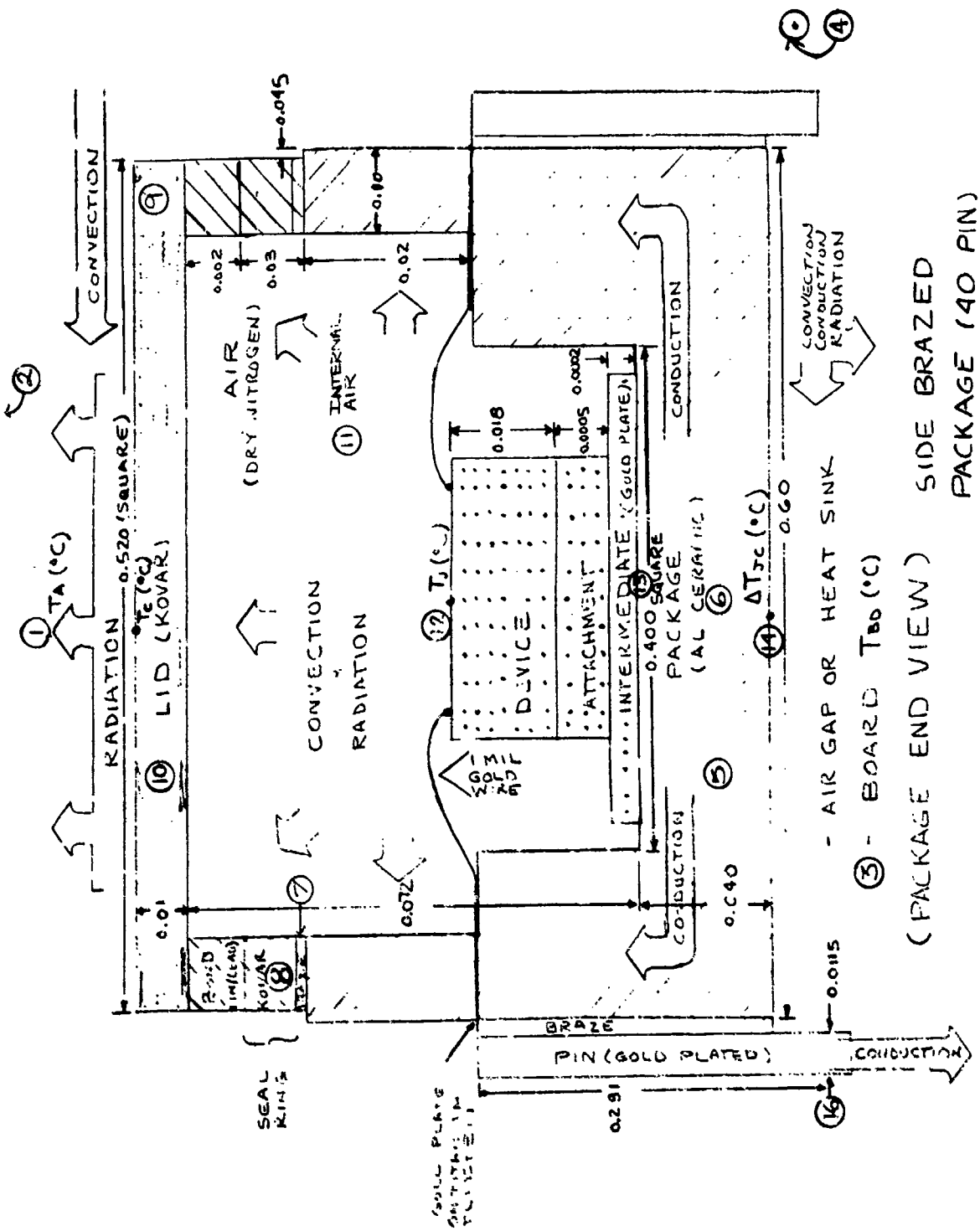
APPENDIX 6. EXTERNAL MODEL

Appendix 6.1. Side-Brazed Package

The figures in this appendix are intended to supplement the text in section 5.4.3.1.

SIDE BRAZED PACKAGE NODAL DESCRIPTION





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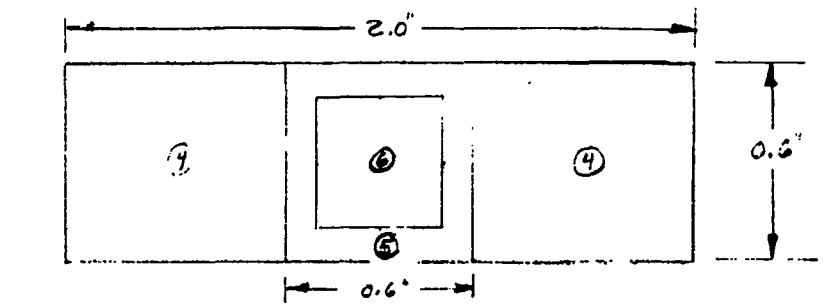
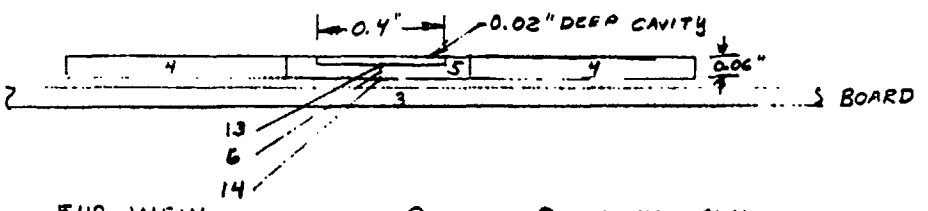
Form D-3061 April 1978

PROJECT	MARTIN MARIETTA AEROSPACE ORLANDO DIVISION	PAGE	TEMP.	PERM.
MICROELECTRONICS		1		
MODEL SIDE BRAZED PACK		REPORT		

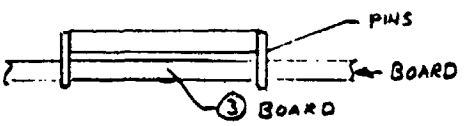
PACKAGE MODEL





END VIEW

① AIR ② RADIATION SINK



BOUNDARY NODES

1 AIR
2 RADIATION SINK
3 CIRCUIT BOARD

CONDUCTORS

1, 4, A
1, 5, B (SIDES ONLY) TOP COVERED
3, 4, C AIR GAP
3, 5, D AIR GAP
4, 5, E
5, 6, F SQ-SQ SIDE
3, 4, CP PINS
3, 5, DP PINS
13, 6, E1
6, 14, E1
3, 14, D1 AIR GAP

RADIATION COND

2, 4, G
2, 5, H (SIDES ONLY)
3, 4, I AIR GAP
3, 5, J AIR GAP
14, 3,

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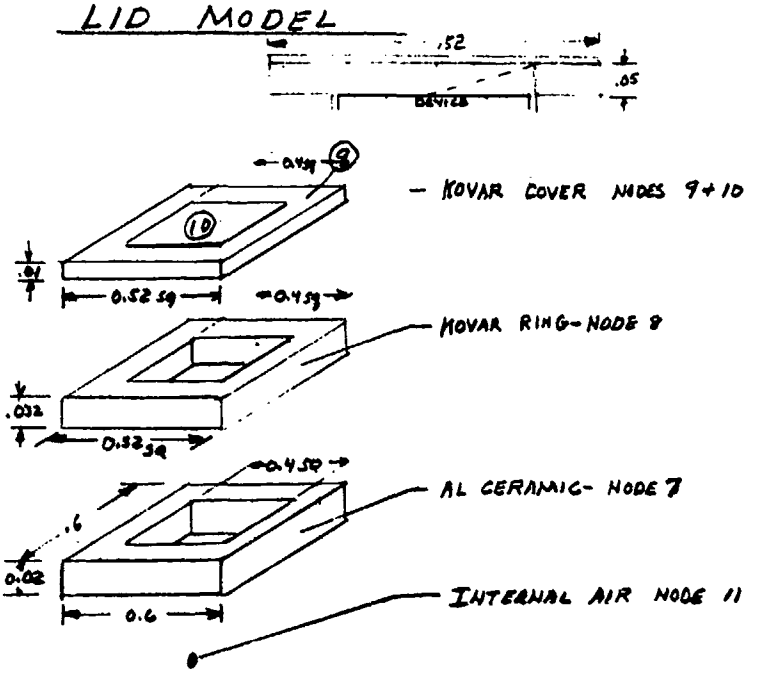
PROJECT	MARTIN MARIETTA AEROSPACE ORLANDO DIVISION	PAGE	TEMP.	PERM.
MICROELECTRONICS		2		
MODEL		REPORT		
SIDE BRAZED PACK				

LID MODEL



CONDUCTORS

5, 7,	K		
7, 8,	L		
8, 9,	M		
9, 10,	N	SQ-SQ SHAPE FACTOR	
7, 1,	O		
8, 1,	P	EXTERNAL CONVECTION	
9, 1,	Q		
10, 1,	R		
7, 11,	S		
8, 11,	T	INTERNAL CONVECTION	
9, 11,	U		
10, 11,	V		

RADIATION CONDUCTORS

AC	7, 2
AD	8, 2
AE	9, 2
AF	10, 2

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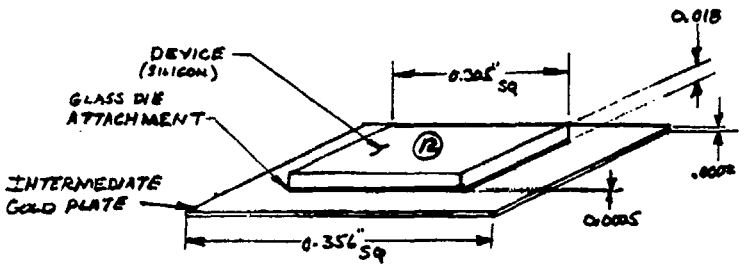
PROJECT	MARTIN MARIETTA AEROSPACE ORLANDO DIVISION	PAGE	TEMP.	PERM.
MICROELECTRONICS		3		
MODEL		REPORT		
SIDE BRAZED PACK				

DEVICE MODEL



CONDUCTORS

12, 13, W
12, 11, X CONNECTION
12, 5, AD AIR GAP

RADIATION CONDUCTORS

12, 10, Y LID TOP
12, 5, Z CARRIER
12, 7, AA LID SIDES
12, 8, AB LID SEAL

GOLD WIRES
12, 5 AH (NOT IN MODEL

3/21/84 { Σ AD + AH = .00072 + .00090 = .00162 change 12, 5 To .00162 (4 wires)
OR 40 WIRES .00072 + .0089 = .00962 R/HR-A

GOLD WIRES from (5) TO PINS .0013 DIA (per Carolyn McCandless 3-12-84)

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BJ 12-6-83		

MARTIN MARIETTA

Form D-3061 April 1978

PROJECT	MARTIN MARIETTA AEROSPACE ORLANDO DIVISION	PAGE	TEMP.	PERM.
MICROELECTRONICS		4		
MODEL		REPORT		
SIDE BRAZED PACK				

CONDUCTOR CALCULATIONS

EXTERNAL CONVECTION $h = 0.7\ ^{B}/_{HR\text{-}FT^2\text{-}°F} = 0.0026\ ^{W}/_{in^2\text{-}°C}$

$K_{air} = .0173\ ^{B}/_{HR\text{-}FT\text{-}°F} = 0.00076\ ^{W}/_{IN\text{-}°C}$

		(B/HR,F)
A	$hA = (.0026)(1.08) = .0028\ ^{W}/_{°C}$ =	.0053
B	$hA = (.0026)(.072) = .0002\ ^{W}/_{°C}$ =	.0004
C	$KA/L = (.00076)(0.84)/.002 = .0103\ ^{W}/_{°C}$ =	.0195
D	$KA/L = (.00076)(0.20)/.062 = .0025\ ^{W}/_{°C}$ =	.0046
E	$KA/L = (2)(.339)(.6)(.06)/0.4 = .0610\ ^{W}/_{°C}$	.1157
F	$KS = (.339)\left(\frac{4(.04)(.2)}{.15} + (4)(.54)(.04)\right) = .1016\ ^{W}/_{°C}$	.1927
CP	$KA/L = (28\ pins)(.419)(.00046)/.002 = .087\ ^{W}/_{°C}$	.1650
DP	$KA/L = (12\ pins)(.419)(.00046)/.062 = .0373\ ^{W}/_{°C}$	.0707
K	$KA/L = (.339)(.24)/.04 = 2.034\ ^{W}/_{°C}$	3.856
L	$1/\left(\frac{L}{KA_7} + \frac{L}{KA_6}\right) = 1/\left(\frac{.01}{(.339)(.24)} + \frac{.015}{(.419)(.1104)}\right) = 2.236\ ^{W}/_{°C}$	4.239
M	$1/\left(\frac{L}{KA_8} + \frac{L}{KA_4}\right) = 1/\left(\frac{.017}{(.419)(.1104)} + \frac{.005}{(.419)(.1104)}\right) = 2.3129\ ^{W}/_{°C}$	4.385
N	$KS = (.419)\left(\frac{4(.2)(.01)}{3} + 4(.54)(.01)\right) = .0343\ ^{W}/_{°C}$	.0650
O	$hA = (.0026)(2.4)(.02) = 1.25E\text{-}4\ ^{W}/_{°C}$	2.37E-4
P	$hA = (.0026)(2.08)(.032) = 1.73E\text{-}4\ ^{W}/_{°C}$	3.28E-4
Q	$hA = (.0026)(.13) = 3.41E\text{-}4\ ^{W}/_{°C}$	6.47E-4
R	$hA = (.0026)(.16) = 4.16E\text{-}4\ ^{W}/_{°C}$	7.89E-4
S	$KA/L = (.0007)(.034)/.2 = .0001\ ^{W}/_{°C}$	1.90E-4
T	$KA/L = (.0007)(.0512)/.2 = .0002\ ^{W}/_{°C}$	3.79E-4
DI	$hA = (.00076)(.16)/.062 = .002\ ^{W}/_{°C}$	.0037

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Form D-3061 April 1978

PROJECT	MARTIN MARIETTA AEROSPACE ORLANDO DIVISION	PAGE	TEMP.	PERM.
MICROELECTRONICS		5		
MODEL		REPORT		
SIDE BRAZED PACK				

CONDUCTORS CONTINUED

		(B/HR,°F)
V	$KA/L = (.0007)(.16)/.035 = .0448$ W/°C	.0849
W	$1/(\frac{L}{KA}_{12} + \frac{L}{KA}_{alum} + \frac{L}{KA}_{gold}) = 1/(\frac{.018}{(2.13)(.093)} + \frac{.0005}{(255)(.093)} + \frac{.0002}{(7.54)(.093)})$ = 8.91 W/°C	16.89
X	$KA/L = (.0007)(.093)/.035 = .0026$ W/°C	.0049
AD = MS	$= (.00076)\left(\frac{(4)(.035)(.093)}{.0475} + (4)(.54)(.018)\right) = .00038$ W/°C	7.22E-4
EI	$K/L = (.339)(.16)/.02 = 2.712$ W/°C	5.142

Radiation Conductors

		(ft²)
G	$FEA = (1)(.8)(1.08) = 0.864$ in²	0060
H	$FEA = (1)(.8)(.072) = 0.0576$ in²	.0004
I	$FEA = (1)_{(.8,.8)}(.6667)(.84) = 0.5609$ in²	.0039
J	$FEA = (1)_{(.8,.8)}(.6667)(.20) = 0.1333$ in²	.000926
Y	$FEA = (.7?)_{(.35,.5)}(.2593)(.093) = .01761$ in²	.00012
Z	$FEA = (1)_{(.5,.7)}(.411)(02196) = .00903$ in²	.00006
AA	$FEA = (.05)_{.5,.7}(.411)(.093)^{.0378} = .00191$ in²	.00001
AB	$FEA = (.05)_{.5,.35}(.2593)(.0558) = .00072$ in²	.00001
AC	$FEA = (1)(.8)(.04) = .032$	.00022
AD	$FEA = (1)(.8)(.0666) = .0533$	.00037
AE	$FEA = (1)(.3)(.13) = .104$	.00072
AP	$FEA = (1)(.8)(.16) = .125$	.00089
AG	$FEA = (1)(.6667)(.16) = .1067$ in²	.000741
GOLD WIRES CONNECTION	AH $(4)\frac{KA}{L} = (4)(7.54\frac{W}{in°C})(\frac{7.854E-7}{.035}) = .00047$	.00090

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BJ 12-9-83		

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Form D-3081 April 1978

PROJECT	MARTIN MARIETTA AEROSPACE ORLANDO DIVISION	PAGE	TEMP.	PER.
MICROELECTRONICS		6		
MODEL		REPORT		
SIDE BRAZED PACK				

DATA FILE

# NODES	# BOUNDARIES	ENERGY BAL	INITIAL TEMP	OCCI/OF=0
12	4	.001	80	1

BOUNDARY NODE #, TEMP

1, 80., 2, 80., 3, 80, 12, 110.

# of CONDUCTORS

25

CONDUCTORS

1,4, .0053, 1,5, .0004, 3,4, .0303, 3,5, .0129

4,5, .1157, 5,6, .1426, 3,4, .1650, 3,5, .07[illegible]

5,7, 3.856, 7,8, 4.239, 8,9, 4.385, 9,10, .0660

7,1, .000237, 8,1, .000328, 9,1, .000647, 10,1, .000789

7,11, .000190, 8,11, .000379, 10,11, .0849

12,13, 16.51, 12,11, .0049, 12,5, .000379
13,6, 5.142, 6,14, 5.142, 14,3, .0037

RADIATORS

12

RADIATORS

2,4, .006, 2,5, .0004, 3,4, .0039, 3,5, .0017

12,10, .00012, 12,5, .00006, 12,7, .00001, 12,8, .00001

7,2, .00022, 8,2, .00037, 9,2, .00072, 10,2, .00089

RAD TO SPACE

0

SOURCES

0

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BZ 12-7-[illegible]		

[redacted]
Form D-3081 April 1978

PROJECT	MARTIN MARIETTA AEROSPACE ORLANDO DIVISION	PAGE	TEMP.	PERM.
MICROELECTRONICS		8		
MODEL		REPORT		
SIDE BRAZED PACK				

MODEL CHANGES FOR COMPONENT

NOT MOUNTED ON BOARD

RADIATION + CONVECTION TO BOARD GO TO FREE AIR
LEAD CONDUCTION TO BOARD ~~BECOMES~~ CONVECTION TO FREE AIR

CONDUCTORS 4,3 → 4,1 RAD 4,3 → 4,2
5,3 → 5,1 5,3 → 5,2
14,3 → 14,1 14,3 → 14,2

4,3 (PINS) 4,1 (PINS) 4,2 (PINS)
5,3 (PINS) 5,1 (PINS) 5,2 (PINS)

				(B/HR,F)
bottom	4,1	from bottom of 4	$= hA = (.0026)(0.84) = .0022$ W/C	.0041
To	5,1	" " " 5	$= hA = (.0026)(0.20) = .0005$	.0010
AIR	14,1	" " " 14	$= hA = (.0026)(0.16) = .0004$	.0008

PINS To AIR

4,1 $= hA = (.0026)(0.237)_{(\text{CPINS})} = .000175$ W/C .004124

5,1 $= hA = (.0026)(0.359)_{(14\ \text{PINS})} = .000932$ W/C .001768

5 PIN SURFACE AREA $\{[(.04)(.062)+(.02)(.175)](2) + [(.0115)(.062+.175)](2)\}(40) + 4[(2)(.062)+(.0115)(.062)] = 1.195$

Σ CONDUCTION

	BOTTOM	(PINS)	TOP+SIDES	
4,1 =	(.0041)	+ (.004124)	+ (.0053)	= .0135
5,1 =	(.0010)	+ (.001768)	+ (.0004)	= .0032
14,1 =			.00080	

PREPARED BY	CHECKED BY	REVISED BY
BZ 1-4-84		

MODEL CHANGES FOR COMPONENT NIT MOUNTED ON BOARD (CONTINUED)

RADIATION

4,2 FEA = (1)(.8)(0.84) = .672in² .004667A²
5,2 FEA = (1)(.8)(0.20) = .160in² .001111 A²
14,2 FEA = (1)(.8)(0.16) = .128in² .000889A²

Σ RADIATION

4,2. = (.006) + (.004667) = .0107
5,2 = (.0004) + (.00111) = .0015
14,2 = .000889

PREPARED BY	CHECKED BY	REVISED BY
B²/1-4-84		

Form D-3081 April 1978

PROJECT	MARTIN MARIETTA AEROSPACE ORLANDO DIVISION	PAGE 12	TEMP.	PERM.
MICROELECTRONICS				
MODEL SIDE BRAZED PACK		REPORT		

Model Changes for gold wires

connecting chip cavity to pins

gold wires are .0013 in dia (per Carolyn McLaughlin 3-12-58)

ADD 2 NEW NODES AT PIN braze JOINTS

15 at JOINT WITH NODE 5
16 at JOINT WITH NODE 4

Node 5 to pins (15)

$G_{ambient} = K\frac{A}{L} = (.339)(.6)(.06)/.1 = .12204$

$G_{wires} = K\frac{A}{L}(\text{number}) = (7.54)\left(\frac{\pi}{4}\right)(.0013^2)/.1\,(12) = .00120$

$G_{Total} = G_1 + G_2 = .12324$ w/c (.23363 Btu/hr-F)

Node 4 to Pins (16)

$G = K\frac{A}{L} = (.339)(1.4)(.04)/.15 = 0.18984$ w/c (.35996) Btu/hr-F

G_{wires} (Node 5 to pins (16)) $= (7.54)\left(\frac{\pi}{4}\right)(.0013^2)/.4\,(28)$

$= .00070$ w/c

(

Pins To Board

15, 3 (DP) .0373 w/c
16, 3 (CP) .0871 w/c

Near Conductance

5, 15, .23368
4, 16, .35996
5, 16, .00133
15, 3, .0707
16, 3, .1165

PREPARED BY	CHECKED BY	REVISED BY
B 3-17-84		

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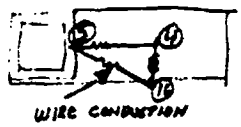
PROJECT	MARTIN MARIETTA AEROSPACE ORLANDO DIVISION	PAGE 13	TEMP.	PERM.
MODEL SIDE BRAZED PACK		REPORT		

Modification to Gold Wire Changes

WAS



NOW

	WAS	NOW
5,4	.1157 + .0015	= .1172
4,16	.3599 + .0035	= .3635
5,16	- delete	

Term G .0839 .0886 down 0.3%

However, wire heat flow is now influenced by temperature of Ag_2O_3 package. Increased heat flow from 5 to 4 can be dissipated also by convection to air and conduction in board

Results - Minimal change mode 4 rose 0.01 °C
mode 16 dropped 0.01 °C
mode 10 rose 0.01 °C
all others - no change

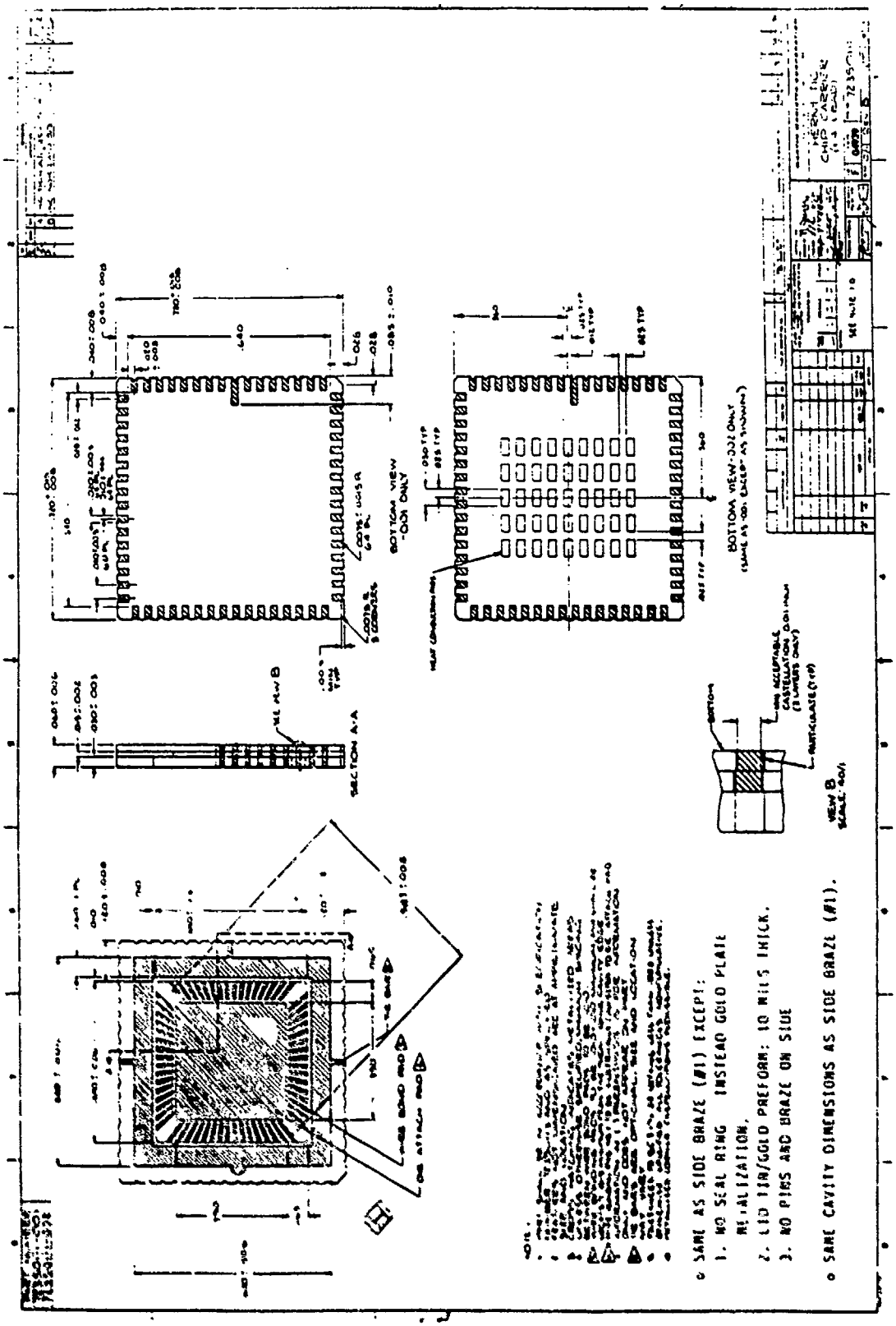
Comparison of Results with measured data

		1.04 W Measured	1.04 W Predicted	1.99 W M	1.99 W P	4.34 W M	4.34 W P
Junction	°C	47.2	49.6	62.7	67.4	119.7	122.3
Lid	°C	43.1	43.2	54.0	56.5	91.7	98.1
Center Lead	°C	41.1	42.1	50.9	52.6	85.5	90.1
End Lead	°C	36.1	37.6	39.7	43.9	61.9	71.3
Ambient Air			25	25		25	
Radiation Shield			25	25		25	
Board Temperature			35.3	37.0		61.3	
Power Dissipation			1.01 W	1.99		4.34	
Θ_{JC}	°C/W	11.8	14.1	11.95			

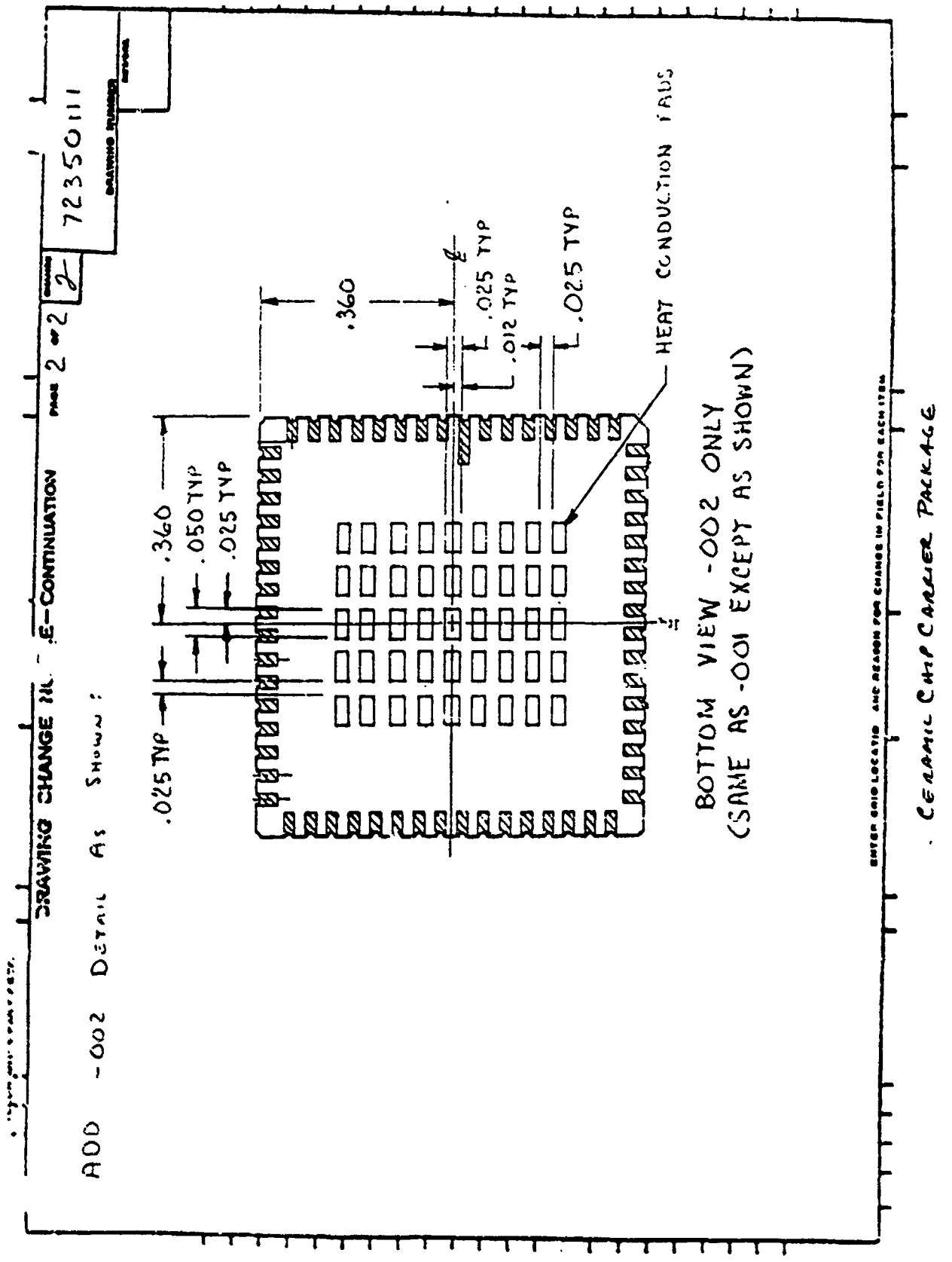
PREPARED BY	CHECKED BY	REVISED BY
BJ 3-15-84		

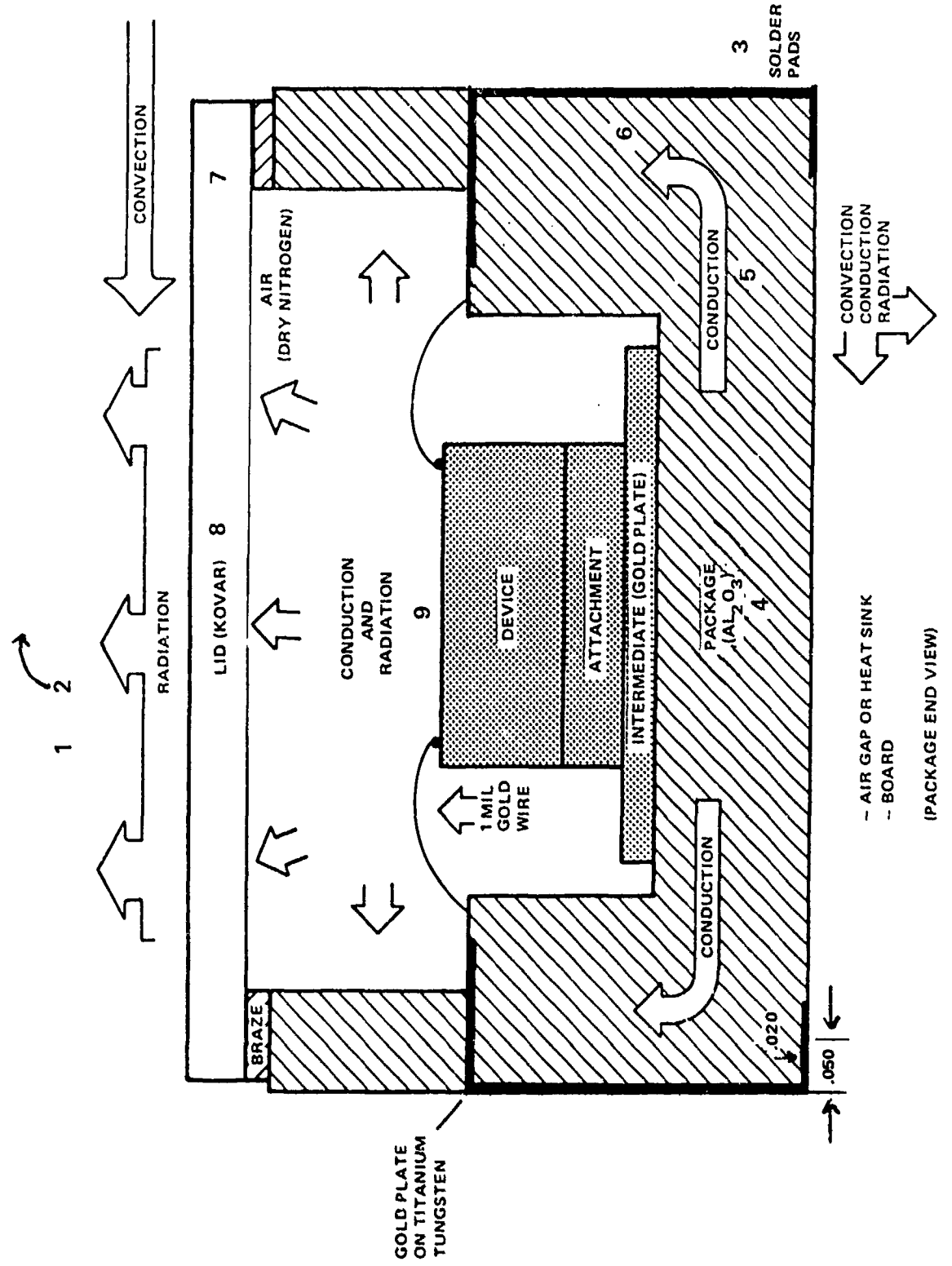
Appendix 6.2. Ceramic Chip Carrier

The figures in this appendix are referred to in section 5.4.3.2. They also supplement the work described in that section.



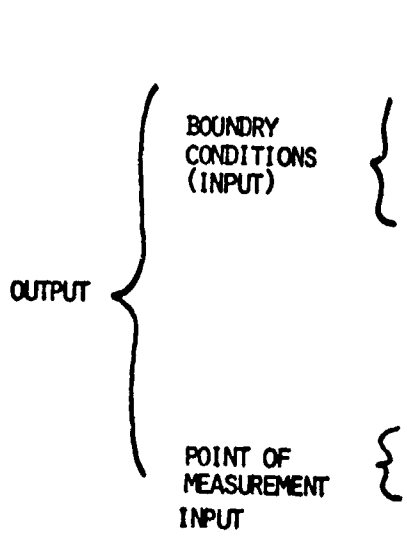
CERAMIC CHIP CARRIER PACKAGE





CERAMIC CHIP CARRIER PACKAGE

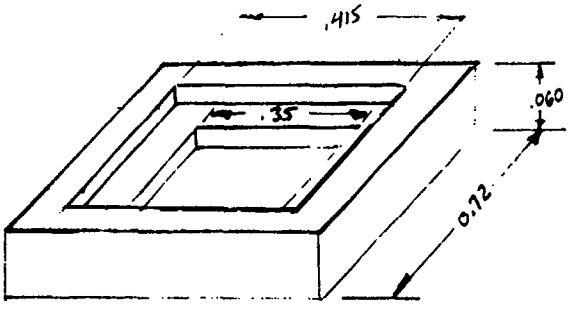
CERAMIC CHIP CARRIER NODAL DESCRIPTION

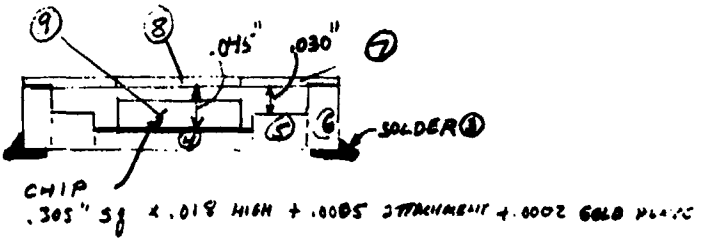


NODE	
1	AMBIENT AIR
2	RADIATION SINK
3	SOLDER PADS
4	BASE CENTER
5	BASE
6	PACKAGE EDGE
7	LID EDGE
8	LID CENTER
9	JUNCTION

Form D-3061 April 1978

PROJECT	MARTIN MARIETTA AEROSPACE ORLANDO DIVISION	PAGE	TEMP.	PERM.
MICROELECTRONICS		/		
MODEL C3		REPORT		





BOUNDARY NODES

1. AIR
2. RADIATION SINK
3. BOARD

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2-22-84		

MARTIN MARIETTA
Form D-3061 April 1978

PROJECT MICROELECTRONICS	MARTIN MARIETTA AEROSPACE ORLANDO DIVISION	PAGE 2	TEMP.	PERM.
MODEL C^3		REPORT		

C^3 MODEL CALCULATIONS

	From Node / To Node			B/HR °F
EXTERNAL CONVECTION	1, 8	$G = hA = (.0026)(.305)(.305)$	$= 2.42E-4$ W/°C	4.6E-4
	1, 7	$G = hA = (.0026)(0.4254)$	$= 0.00111$ "	.00210
	1, 6	$G = hA = (.0026)(.1728)$	$= 4.5E-4$ "	8.5E-4
	4, 3	$G = K\frac{A}{L} = (.00076)(.35)(.35)/.01$	$= .00931$ "	.01765
	5, 3	$G = K((W_2L_2)-(W_1L_1))/T$		
		$=(.00076)[(.415^2)-(.35^2)]/.01$	$= .00378$ W/°C	.00717
EXTERNAL CONDUCTION	6, 3	$G = K(.72^2-.415^2)/.03)$	$= 3.9118$ W/°C	
		$=(.00076)(.72^2-.415^2)/.02$	$= 7.6759$ W/°C	
		$G = 1/(1/3.9118+1/7.6759) = 2.5844$		4.900Z
INTERNAL CONDUCTION	5,6	$G_1 = (4)(.339)(.54*.06+.06*.415/.07625 = .48675$ W/°C		
		$G_2 = (4)(.339)(.54*.03+.03*.3825/.01625 = .47951$ W/°C		
		$G_T = 1/(1/.48675+1/.47951) = .32516$ W/°C		0.61654
	4,5	$G_1 = (4*.339)(.54*.015+.015*.305/.0225) = .28670$ W/°C		
		$G_2 = (4*.339)(.54*.03+.03*.35/.01625) = .89815$ W/°C		
		$G_T = 1/(1/.28670+1/.89815) = .21733$ W/°C		0.41208
	6,7	$G = (.339)(.72^2-.415^2)/.03 = 3.9118$ W/°C		7.4171
	7,8	$G = (.446)(4)(.54*.01+.01*.305/.13125) = .05109$		0.09687
	9,4	$G_1 = (2.13)(.35)(.35)/.018 = 11.008$		
		$G_2 = (.339)(.35)(.35)/.075 = 0.5837$		
		$G_T = 1/(1/11.008+1/0.5837) = 0.52716$ W/°C		0.99959
INTERNAL CONVECTION	9,5	$G_1 = (.00076)(4*.305*.015)/.05 = 2.8E-04$ W/°C		
		$G_2 = (7.54)(48)(\pi(.001^2)/4)/.05 = .00569$ W/°C		
		$G = 2.8E-04+.00569 = .00596$ W/°C		0.01131
	9,8	$G = (.00076)(.305)(.305)/.027 = .00262$ W/°C		0.00496
	5,7	$G = (.00076)((.415^2)-(.35^2))/.03 = .00126$ W/°C		0.00239
INTERNAL RADIATION	9,8	$A_1 = .305^2 = .09303$ in^2 ; $A_2 = A_1$		Ft^2
		$KR = .09303/(1/.85+(1/.5-1)+(A_1/A_2)(1/.02-1)) = .00182$ in^2		1.3E-5 A
	9,7	$KR = (.305^2)/[1/.09+(1/.5-1)+.305^2/(.415^2-.305^2)(1/.02-1))$		
		$= .00134$ in^2		9.3E-6
	9,6	$KR = (.305^2)/((1/.06+(1/.5-1)+(.305^2/(4*.415*.03))(1/.7-1)$		
		$= .00504$		3.5E-5
	9,5	$A_1 = (.018)(.305)(4) = .02196$; $A_2 = (4)(.35)(.015) = .021$ in^2		
		$KR = .02196/(1/.35+(1/.5-1)+(.02196/.021)(1/.7-1) = .00510$ in^2		3.5E-5
	5,7	$A_1 = (.415^2)-(.305^2) = .0792$ in^2 ; $A_2 = A_1$		
		$KR = .0792/(1/.4+(1/.7-1)+(1/.02-1) = .00153$ in^2		1.1E-5

PREPARED BY	CHECKED BY	REVISED BY
B 3-[illegible]-84		

C^3 MODEL CALCULATIONS (CONTINUED)

From Node / To Node		ft^2
8,2	$A_1 = .305^2 = .09303\ in^2$ $A_2 = 100\ in^2$ $KR = .09303/(1/1 + (1/.02 - 1) + (.09303/100)(1/.1 - 1)) = .00186\ in^2$	1.3E-5
7,2	$A_1 = .72^2 - .305^2 = .42538$; $A_2 = 100$ $KR = .42538/(1 + (1/.02 - 1) + (\frac{.42538}{100})(1/.1 - 1)) = .00851\ in^2$	5.9E-5
6,2	$A_1 = (4)(.06)(.72) = .1728\ in^2$; $A_2 = 100\ in^2$ $KR = (.1728)/(1/.5 + (1/.1 - 1) + (\frac{.1728}{100})(1/.1 - 1)) = .01115\ in^2$	4.9E-4
6,3	$A_1 = (4)(.06)(.72) = .1728\ in^2$; $A_2 = 100\ in^2$ $KR = (.1728)/[1/.5 + (1/.1 - 1) + (\frac{.1728}{100})(1/.8 - 1)) = .01114\ in^2$	4.9E-4
5,3	$A_1 = .415^2 - .35^2 = .04973\ in^2$; $A_2 = A_1$ $KR = .04973/(1/.7 + (1/.7 - 1) + (1/.8 - 1)) = .02360\ in^2$	1.6E-4
4,3	$A_1 = .305^2 = .09303\ in^2$; $A_2 = A_1$ $KR = .09303/(1/.7 + (1/.7 - 1) + (1/.8 - 1)) = .05198\ in^2$	3.6E-4

RADIATION CONSTANTS ARE of the FORM

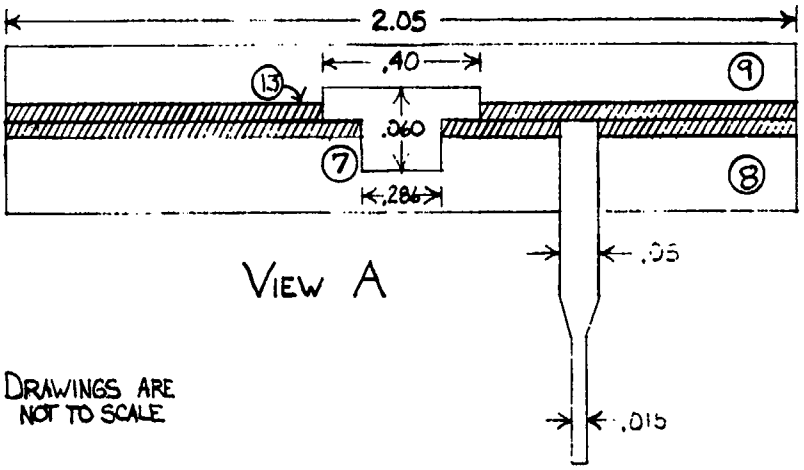
$$KR = \frac{A_1}{\frac{1}{F_{12}} + \left(\frac{1}{\epsilon_1} - 1\right) + \frac{A_1}{A_2}\left(\frac{1}{\epsilon_2} - 1\right)}$$

Where A_1 = AREA of surface 1
A_2 = AREA of surface 2
ϵ_1 = EMISSIVITY of surface 1
ϵ_1 = EMISSIVITY of surface 2
F_{12} = BLACK BODY SHAPE FACTOR from Surface 1 to surface 2

Appendix 6.3. Cerdip Package

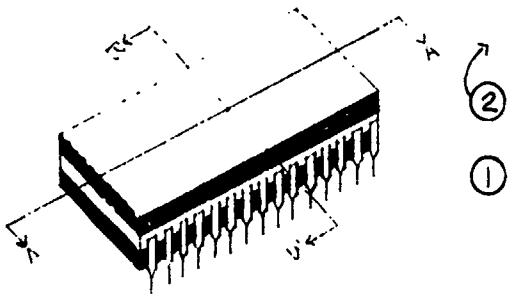
The figures in this appendix are referred to in section 5.4.3.3. They also supplement the work described in that section.

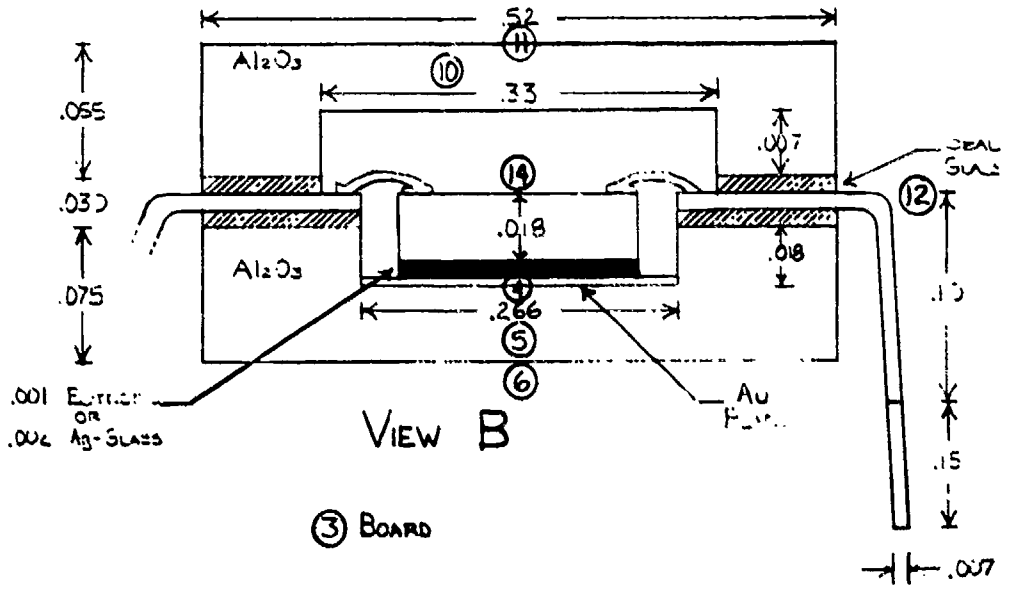
CERDIP



VIEW A

DRAWINGS ARE NOT TO SCALE





VIEW B

3 BOARD

CERDIP NODAL DESCRIPTION

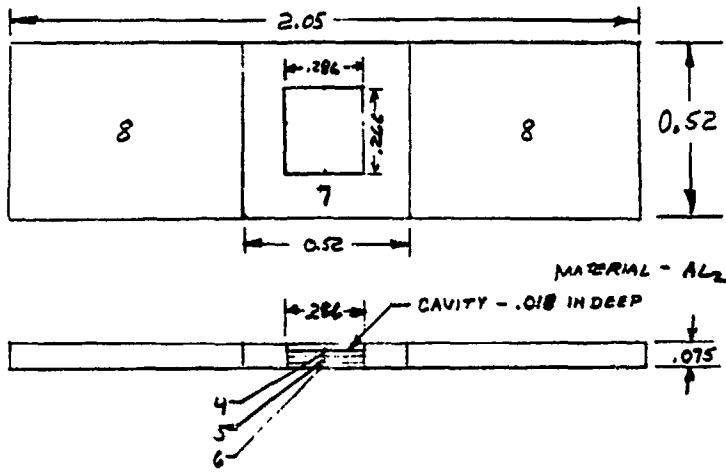
	NODE	DESCRIPTION
BOUNDRY CONDITIONS (INPUT)	1	AMBIENT AIR
	2	RADIATION SINK
	3	CIRCUIT BOARD
OUTPUT	4	CAVITY BOTTOM
	5	BASE CENTER (UNDER CAVITY)
	6	BASE BOTTOM (UNDER CAVITY)
	7	AREA OF PACKAGE BASE EQUIVALENT TO CAVITY
	8	PACKAGE BASE EDGES
	9	PACKAGE LID EDGES
POINT OF MEASUREMENT	10	AREA OF PACKAGE LID EQUIVALENT TO CAVITY
	11	LID CENTER
	12	GLASS SEAL EDGES (PIN LEADS AVG. IN)
	13	EQUIVALENT TO NODE 10, BUT GLASS SEAL PORTION (PIN LEADS AVG. IN)
INPUT	14	JUNCTION

MARTIN MARIETTA

Form D-3061 April 1978

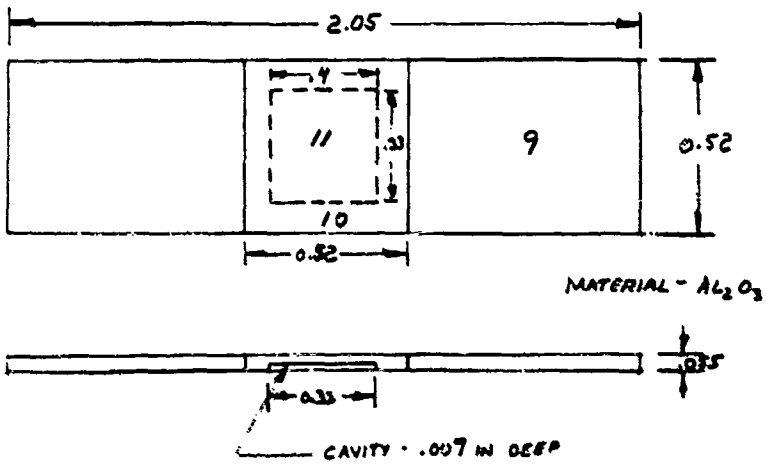
PROJECT	MARTIN MARIETTA AEROSPACE ORLANDO DIVISION	PAGE	TEMP.	PERM.
MICROELECTRONICS		1		
MODEL CERDIP		REPORT		

PACKAGE BASE



glass INTERFACE .030" between pins
.023" at pins

PACKAGE LID



PREPARED BY	CHECKED BY	REVISED BY
BZ 1-18-84		

Form D-3081 April 1978

PROJECT	MARTIN MARIETTA AEROSPACE ORLANDO DIVISION	PAGE 2	TEMP.	PERM.
MODEL CERDIP		REPORT		

GLASS SEAL AND PIN LEADS

OVERALL DIMENSIONS (LESS CAVITY)

THICKNESS = .030"
LENGTH = 2.05"
WIDTH = .52"

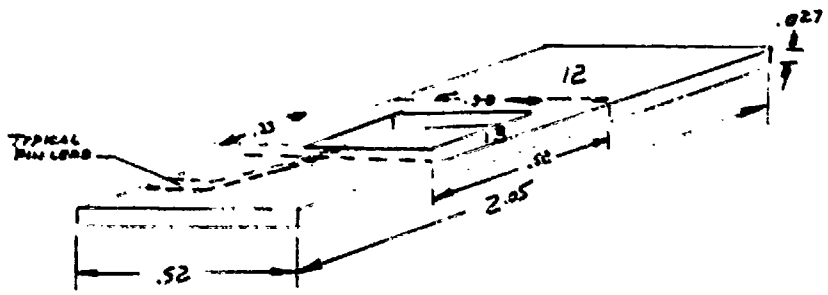
NOTE PIN LEADS OCCUPY ≈50% OF TOTAL AREA

THICKNESS AT PINS .23" ≈50% TOTAL AREA
THICKNESS BETWEEN PINS .30" ≈50% TOTAL AREA

USE AVERAGE THICKNESS $(.23+.30)/2 = 0.27$ IN

ASSUMES TEMPERATURE GRADIENT THRU PINS IN DIRECTION NORMAL TO PLANE OF SEAL IS NEGLIGIBLE.

USE AVERAGE PIN/LEAD CONDUCTANCE IN PLANE OF SEAL



NODE 12 REPRESENTS THE AVERAGE PIN LEAD TEMP

PIN LEAD PATTERN

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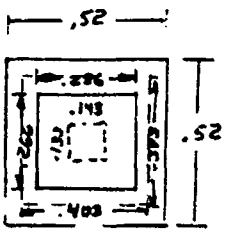
RB 2-15-84		

Form D-3061 April 1978

PROJECT MICROELECTRONICS	MARTIN MARIETTA AEROSPACE ORLANDO DIVISION	PAGE 3	TEMP.	PERM.
MODEL CERDIP		REPORT		

BASE + CAP SPREADING CONDUCTANCE

BASE



$W_1 = .019$
$L_1 = .154$
$T_1 = (.296 - .158)/2 = .059$

$W_2 = .025$
$L_2 = .276$
$T_2 = (.398 - .276)/2 = .061$

$$G = KS = K\left[(4)(.54)(W) + (2)\frac{L_1 W}{T_1} + (2)\frac{L_2 W}{T_2}\right] + 2\frac{W}{T}(L_1 + L_2)$$

Ref: Jacob & Hawkins Pg 38

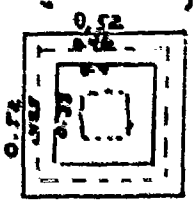
$L_{AVG} = \frac{L_1 + L_2}{2}$ Substituting $+ 2\frac{W}{T}(2L_{AVG})$

$$G = K\left[(4)(.54)(W) + (4)\frac{W}{T}L_{AVG}\right]$$

$$G = 4K\left[.54W + WL_{AVG}/T\right]$$

When $W = .019$, $L_{AVG} = 0.138$, $T = 0.13$

CAP



$W = .048$
$L_{AVG} = .1825$
$T_{AVG} = .013$

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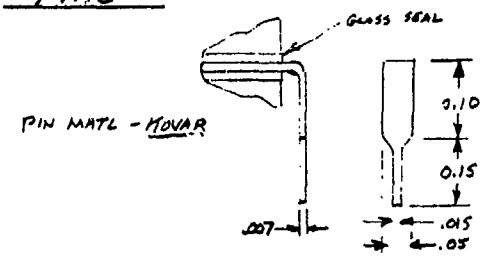
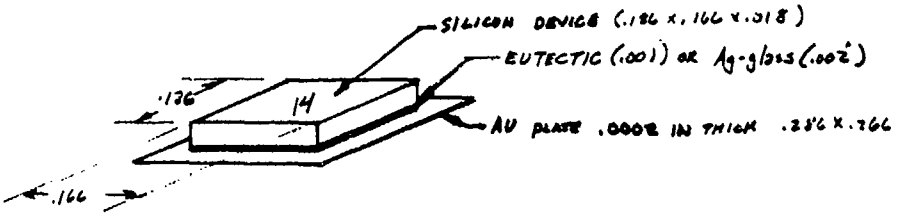
BE 2-17-89		

PINS



12-3 28 pins .05 wide (.007 thick) 28 x .05 = 1.4
13-3 12 pins .05 " " " 12 x .05 =

DEVICE



BOUNDARY NODES

NODE	
1	AIR
2	RADIATION SINK
3	CIRCUIT BOARD

Form D-3081 April 1978

PROJECT MICROELECTRONICS	MARTIN MARIETTA AEROSPACE ORLANDO DIVISION	PAGE 5	TEMP.	PERM.
MODEL CERDIP		REPORT		

CERDIP PACKAGE CALCULATIONS

EXTERNAL CONDUCTORS

	From Node/ To Node		W/C	B/HR °F
CONVECTION	1, 9	$G_1 = (.0026)(.52)(1.53) =$	.00207	
		$G_2 = (.0026)(.053)(4.1) =$	5.9E-4	
		$G_T = .0027 + 5.9E-4 =$	.00265	.00913
	1, 10	$G_1 = (.0026)(.19)(1.7) =$	8.4E-4	
		$G_2 = (.0026)(.055)(1.04) =$	1.5E-4	
		$G_T = 8.4E-4 + 1.5E-4 =$	9.9E-4	.00187
	1, 11	$G = (.0026)(.33)(.33)$	2.8E-4	5.4E-4
	1, 12	$G = (.0026)(.03)(4.1)$	3.2E-4	6.1E-4
	1, 13	$G = (.0026)(.03)(1.04)$	8.1E-5	1.5E-4
	1, 7	$G = (.0026)(.075)(2.57)$	5.04E-4	9.5E-4
	1, 8	$G = (.0026)(.075)(1.52)$	1.04E-4	1.9E-4
CONDUCTION	3, 6	$G = (.00076)(.266)(.286)/.01$	.00578	.01096
	3, 7	$G = (.00076)(.52)(.52)/.01$	.01477	.02800
	3, 8	$G = (.00076)(.52)(1.53)/.01$	.06047	.11465
RADIATION	2, 9	$KR = (1)(.8)(.52)(1.53)$	.63648 IN²	.00442 ft²
	2, 10	$KR = (1)(.8)(.19)(1.7)$	.2584 IN²	.00179 ft²
	2, 11	$KR = (1)(.8)(.33)(.35)$	.0924 IN²	6.4E-4
	2, 12	$KR = (1)(.8)(.03)(4.1)$	.0984 IN²	6.8E-4
	2, 13	$KR = (1)(.8)(.03)(1.04)$	.02496 IN²	1.7E-4
	2, 7	$KR = (.25)(.8)(.015)(4.1)$	.0615	4.3E-4
	2, 8	$KR = (.25)(.8)(.075)(1.04)$	.0156	1.1E-4

INTERNAL CONDUCTORS - BASE

		W/C	B/HR. °F
4, 5	$G = (.339)(.266)(.286)/.019$	1.3574	2.5737
4, 6	$G = (.339)(.266)(.286)/.019$	1.3574	2.5737
4, 7	$G_1 = (.339)(4)(.54 * .019 + .019 * .158/.054)$	.08271	
	$G_2 = (.339)(4)(.54 * .025 + .025 * .276/.061)$	.17167	
	$G_T = 1.896/(1/.08271 + 1/.17167)$		.12660
5, 7	$G_1 = (4)(.339)(.54 * .019 + .019 * .158/.054)$	.08271	
	$G_2 = (4)(.339)(.54 * .025 + .025 * .276/.061)$	.17167	
	$G_T = 1.896/(1/.08271 + 1/.17167)$		.12660

PREPARED BY BZ 3-22-84	CHECKED BY	REVISED BY

Form D-3081 April 1978

PROJECT MICROELECTRONICS	MARTIN MARIETTA AEROSPACE ORLANDO DIVISION	PAGE 6	TEMP.	PERM.
MODEL CERDIP		REPORT		

CERDIP PACKAGE CALCULATIONS - CONTINUED

From Node To Node		W/°C	B/HR, °F
6, 7	$G_1 = 4(.337)(.54*.019+.019*.158/.059)$	.08291	
	$G_2 = 4(.337)(.54*.025+.025*.276/.061)$	.17169	
	$B_T = 1.896/(1/.08291 + 1/.17169)$		.10600
7, 8	$G = (.337)(.015)(1.04)/.441$	.05976	.11369
	INTERNAL CONDUCTORS - CAP		
10, 9	$G = (.339)(.055)(1.04)/(.4125)$	.04701	.08913
10, 11	$G = (.337)(.048)(.1825)/.13$	.12052	.23796
	INTERNAL CONDUCTORS - GLASS SEAL & PIN LEADS		
12, 13	$G_1 = (.419)(.007)(.52)/(.441)$	.00346	.00656
	$G_2 = (.025)(.27)(.52)/.441)$	.00796	.01509
	$G_T = .00346 + .00796$	.01142	.02165
9, 12	$G_1 = (.025)(.52)(1.53)/.0135$	1.4733	
	$G_2 = (.339)(.52)(1.53)/.0275$	9.8076	
	$G_T = 1/(1/1.4733 + 1/9.8076)$	1.2809	2.4287
8, 12	$G_1 = (.025)(.52)(1.53)/.0135$	1.4733	
	$G_2 = (.339)(.52)(1.53)/.0375$	7.1922	
	$G_T = 1/(1/1.4733 + 1/7.1922)$	1.2228	2.3186
7, 13	$G = (.025)(.52)(.3737)/.0135$	.35486	.68233
10, 3	$G = (.025)(.52)(.2622)/.0135$	.25249	.47874
13, 3	$G = (.419)(.007)(.6)/.2$	.00880	.01668
12, 3	$G = (.419)(.007)(1.4)/.2305$	.01781	.03378
	INTERNAL CONDUCTORS - SILICON CHIP		
14, 4	$G_1 = (2.13)(.166)(.186)/.018$	3.6537	6.9277
	$G_2 = (.339)(.266)(.286)/.0095$	2.7147	
	$G_T = 1/(1/3.6537 + 1/2.7147)$	1.5575	2.9531
14, 11	$G = (.00076)(.166)(.186)/.04$	5.9E-4	.00111
14, 7	$G = (.00076)(.018)(.704)/.05$	1.9E-4	3.7E-4

PREPARED BY BJ 3-27-84	CHECKED BY	REVISED BY

Form D-3061 April 1978

PROJECT	MARTIN MARIETTA AEROSPACE ORLANDO DIVISION	PAGE	TEMP.	PERM.
MICROELECTRONICS		7		
MODEL CERDIP		REPORT		

CERDIP PACKAGE CALCULATIONS -CONTINUED

INTERNAL RADIATION

From Node To Node		in^2	ft^2
14, 11	$HR = (1)(.5)(.166)(.186)$	.01544	1.1 E-4
14, 7	$HR = (1)(.5)(.018)(.704)$	.00634	4.4 E-5

INTERNAL CONDUCTORS -GOLD JUMP WIRES

14, 13	$G = (7.54)\ \pi\ (.001)^2 (40)/4$	2.4 E-4	1.6 E-6

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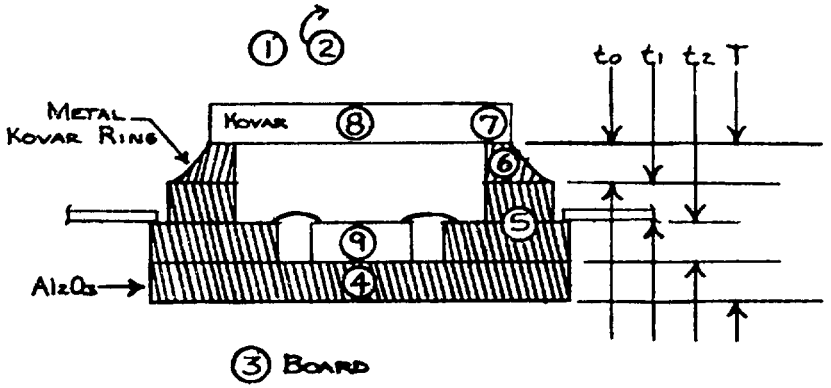
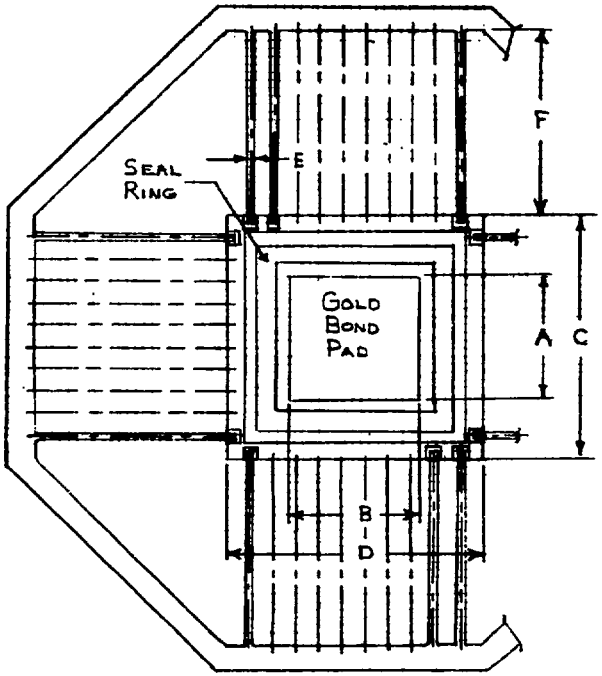
BZ 3-27-84		

Appendix 6.4. Flatpack Package

The figures in this appendix are referred to in section 5.4.3.4. They also supplement the work described in that section.





NOTES:

METAL RING: KOVAR
LID: .010" THICK; KOVAR
AC_2O_3: 96% @ 100°C
LEAD COUNT: 80
TOP BRAZE

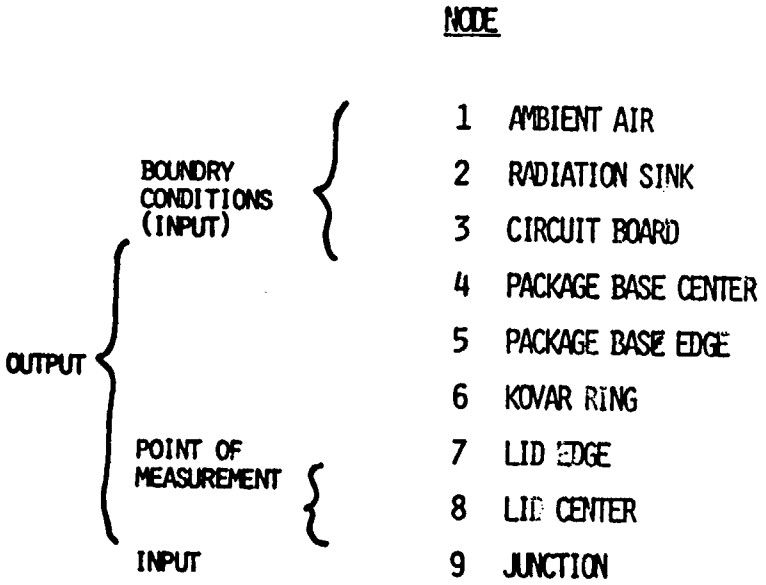
DIMENSIONS:

D/A CAVITY: AXB: .366 X .366
LAYER THICKNESS: $t_o/t_1/t_2/T$: -/.020/.031/.071

OVERALL SIZE: CXD: 1.114 X 1.114
LEAD SPACING: .050
LEAD DIMENSIONS: EXF: .018 X .4335

FLATPACK PACKAGE

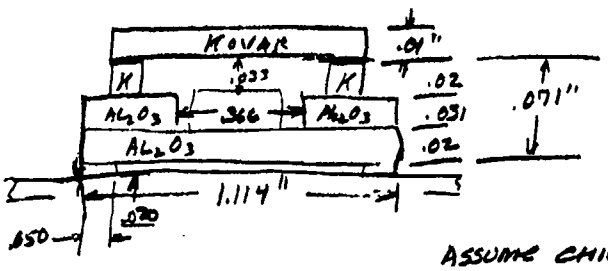
FLATPACK NODAL DESCRIPTION



MARTIN MARIETTA

Form D-3061 April 1978

PROJECT	MARTIN MARIETTA AEROSPACE ORLANDO DIVISION	PAGE	TEMP.	PERM.
MICROELECTRONICS		1		
MODEL FLATPACK		REPORT		



AL_2O_3 (96% @ 100°C)
K = .339 W/IN, C

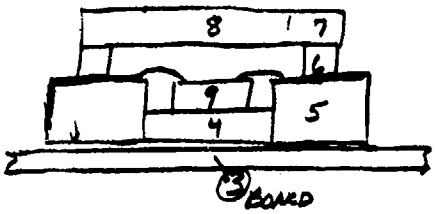
KOVAR
K = .419 W/IN.C

ASSUME CHIP .305 x .305 x .018
SILICON
K = 2.13 W/IN °C

K_{air} = .0173 B/HR FT °F
= .00076 W/IN °C

① AIR ② RADIATION SINK

h_{CONV} = 0.7 B/HR FT² °F
= .0026 W/IN² °C



1 AIR
2 RAD SINK
3 BOARD

PREPARED BY	CHECKED BY	REVISED BY
B. 3-15-84		

MARTIN MARIETTA
Form D-3061 April 1978

PROJECT MICROELECTRONICS	MARTIN MARIETTA·AEROSPACE ORLANDO DIVISION	PAGE 2	TEMP.	PERM.
MODEL FLATPACK		REPORT		

CONDUCTORS - INTERNAL

4, 5 SPREADING 90% chipsize (.305 = .9) = .2745

$G_1 = 4K\left(\frac{(.54)(.02) + (.02)(.2745)}{.0455}\right) = .1772$

$G_2 = 4K\left[\frac{(.54)(.051) + (.051)(.366)}{.187}\right) = .1727$

$G_{TOTAL} = 1/R_G + 1/R_C = .0875\ W/C$ (.1658) B/HR,F

5, 6 $K\frac{A}{L}$

$(.339)(.414^2 - .366^2)/.0255 = 16.5\ W/C$

$(.419)(.7^2 - .5^2)/.101 = 10.1\ W/C$

$G_{TOTAL} = 1/(1/16 + 1/6) = 6.2\ W/C$ (11.76) B/HR,F

6, 7

$G_1 = 10.1$ (from 5, 6) $= 10.1\ W/C$

$G_2 = (.419)(.7^2 - .5^2)/.105 = 20.1\ W/C$

$G_{TOTAL} = 1/(1/6 + 1/6) = 6.7\ W/C$ (12.74)

7, 8 $G = 4K\left(\frac{.54(.01) + (.01)(.3)}{.15}\right) = .0426\ W/C$ (.0807)

9, 4 $G_1 = K\frac{A}{L} = (2.13)(.305^2)/.018 = 11.0\ W/C$

$G_2 = K\frac{A}{L} = (.339)(.366^2)/.01 = 3.83\ W/C$

$G_T = 1/(\frac{1}{11} + \frac{1}{3.83}) = 2.84$ (5.38)

9, 8 $G = K\frac{A}{L} = (.00076)(.305^2)/.033 = .0021\ W/C$ (.0041)

9, 5 G = SPREAD = $4K(.54(.018) + (.305)(.018)/.0305) = .0006$

K_{AL} (GOLD WIRE) $(80)(754)(.001^2)\frac{\pi}{4}/.31 = .0015$

$.0015 + .0021 = .0040$ (.0040)

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3-18-54		

CONDUCTORS EXTERNAL

			G Min =
8, 1	$hA = (.0026)(.3^2) = .0002$ W/C		(.0004)
7, 1	$hA = (.0026)(.7^2 - .3^2) = .001$ W/C		(.002)
6, 1	$hA = (.0026)(4)(.7)(.02) = .0001$ W/C		(.0003)
5, 1	$hA = (.0026)[(4)(1.114)(.051) + (1.114^2 - .7^2)] = .0025$ W/C		(.0048)
4, 3	$KA/L = (.00076)(.366)^2/.02 = .0051$ W/C		(.0097)
5, 3	$KA/L = (.00076)(1.114^2 - .366^2)/.02 = .0285$ W/C		
G2	$(.339)(1.114^2 - .366^2)/.01 = 25.5$ W/C		
G3	TOTAL = $1/(1/\quad + 1/\quad)$	.0285	
G4	Leads $(80)(.45)(.018)(.02)/.43$	$= .1206$	
		$G_T = G_3 + G_4 = .1491$	(.2826)

RADIATION — INTERNAL

9, 8 $F = .8$, $\epsilon_1 = .5$, $\epsilon_2 = .35$, $A_1 = .305^2 = .093$, $A_2 = .3^2 = .09$

$G = A_1 / \left[\frac{1}{F} + \left(\frac{1}{\epsilon_1} - 1\right) + \frac{A_1}{A_2}\left(\frac{1}{\epsilon_2} - 1\right)\right]$

$G = (.24)(.093) = .0223$ in^2 = .0002 ft^2

9, 7 $F = .2$, $\epsilon_1 = .5$, $\epsilon_2 = .35$, $A_1 = (.305^2) = .093$, $A_2 = (.6^2 - .3^2) = .27$

$G = (.15)(.093) = .0140$ in^2 = .0001 ft^2

9, 5 $F = .8$, $\epsilon_1 = .5$, $\epsilon_2 = .7$, $A_1 = (.018)(4)(.305) = .0220$ in^2, $A_2 = (.031)(4)(.366) = .0454$ in^2

$G = (.21)(.022) = .0046$ in^2 = .000032 ft^2

RADIATION - EXTERNAL

8, 2 $G = FEA = (1)(.35)(.3^2) = .0315\ in^2 = .00022\ ft^2$

7, 2 $G = FEA = (1)(.35)(.6^2 - .3^2) = .0945\ in^2 = .00066\ ft^2$

6, 2 $G = FEA = (.5)(.35)(4)(.02)(.7) = .0098\ in^2 = .00007\ ft^2$

6, 3 $G = FEA = (.2)(.35)(4)(.02)(.7) = .0039\ in^2 = .00003\ ft^2$ (.5-.3)

5, 2 $G = FEA = (.5)(.7)(4)(.051)(1.114) = .0795 = .00055\ ft^2$

5, 3 $G = FEA =$ same $= .0795$

$G = F = .9$
$\varepsilon_1 = .7$
$\varepsilon_2 = .8$
$A_1 = 1.107$
$A_2 = 1.107$

$G = (.559)(1.107) = 0.618\ in^2$

$\Sigma G = .0795 + .618 = .698\ in^2 = .00485\ ft^2$

4, 3 $F = .9$
$\varepsilon_1 = .7$
$\varepsilon_2 = .8$
$A_1 = A_2 = .134\ in^2$

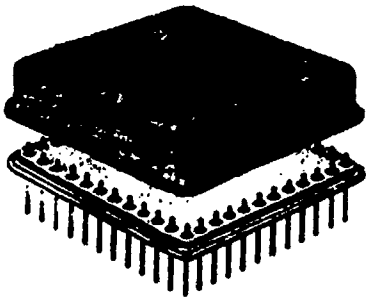
$G = (.559)(.134) = .0749\ in^2 = .00052\ ft^2$

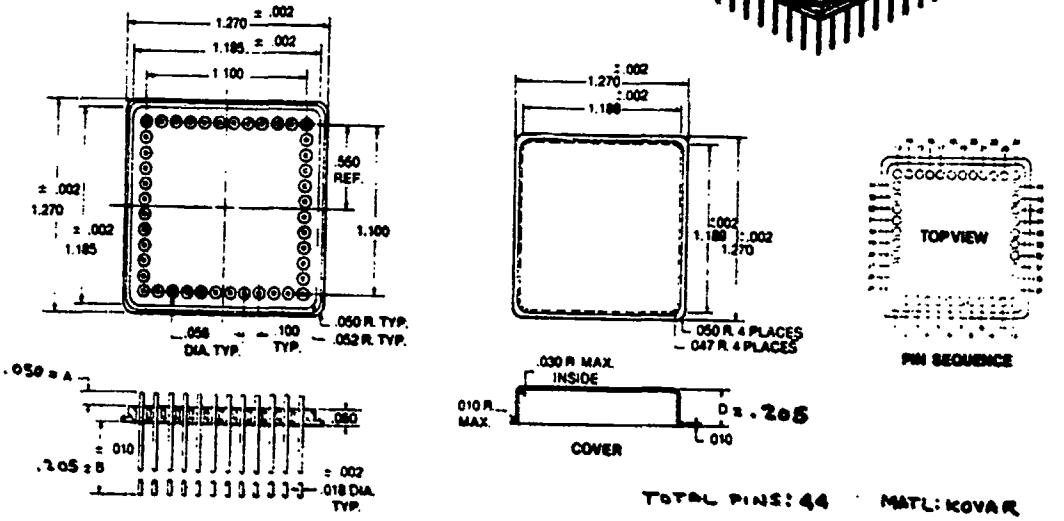
PREPARED BY	CHECKED BY	REVISED BY
BJ 3-19-84		

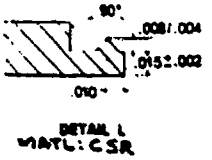
L-27

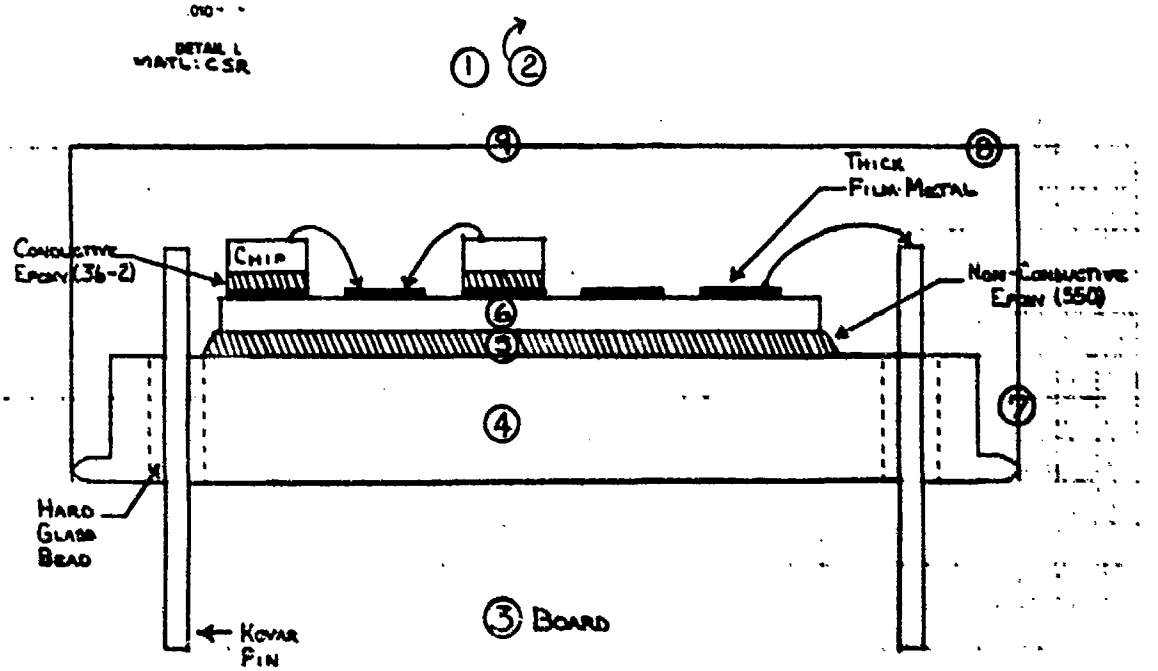
Appendix 6.5. Hybrid Package

The figures in this appendix are referred to in section 5.4.3.5. They also supplement the work described in that section.









HYBRID PACKAGE

6-39

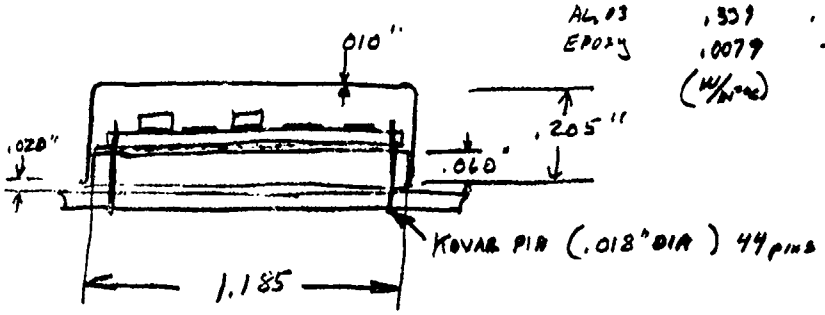
HYBRID NODAL DESCRIPTION

		NODE	
BOUNDRY CONDITIONS (INPUT)		1	AMBIENT AIR
		2	RADIATION SINK
		3	CIRCUIT BOARD
OUTPUT		4	BASE MIDDLE
		5	NON-CONDUCTIVE EPOXY (MIDDLE)
INPUT		6	TOP OF CHIP CARRIER BOARD (CENTER)
OUTPUT		7	BASE COVER
		8	LID EDGE
	POINT OF MEASUREMENT	9	LID CENTER

Form D-3061 April 1978

PROJECT	MARTIN MARIETTA AEROSPACE ORLANDO DIVISION	PAGE	TEMP.	PERM.
MICROELECTRONICS		1		
MODEL HYBRID		REPORT		

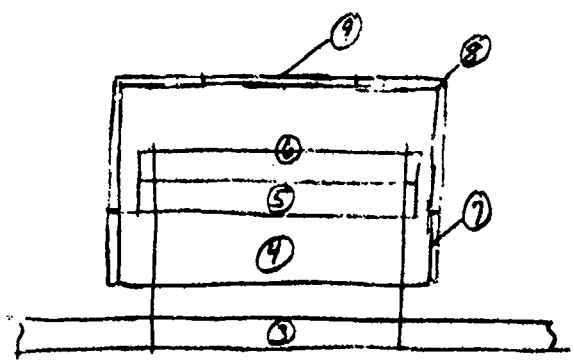
	K	ε
KOVAR	.419	.35
Al_2O_3	.339	.7
EPOXY	.0079	—
	(W/IN°C)	



- ASSUME CIRCUIT BOARD .020" Al_2O_3
- " NON-CONDUCTIVE EPOXY .005" THICK
- " KOVAR BASE

$K_{air} = .0173 \frac{B}{HR\ FT\ °F}$
$= .0076 \frac{W}{IN\ °C}$

$h_c = 0.7 \frac{B}{HR\ FT^2\ °F}$
$= .0026 \frac{W}{IN^2\ °C}$



NODE

1 - ambient air
2 - Radiation sink
3 - Board

PREPARED BY	CHECKED BY	REVISED BY
B 3-19-84		

CONDUCTOR CALCULATIONS

		W/°C	B/hr °F
6,5	$B_1 = KA/L = (.339)(1.15)(1.15)/.02 =$	22.416	
	$G_2 = (.0079)(1.15)(1.15)/.0025 =$	4.179	
	$G_{TOTAL} = 1/(\frac{1}{B}+\frac{1}{G}) =$	3.522	(6.679)
5,4	$G_1 = KA/L = (.0079)(1.15)(1.15)/.0025 =$	4.179	
	$G_2 = KA/L = (.419)(1.185)(1.185)/.03 =$	19.612	
	$G_T = 1/[\frac{1}{G}+\frac{1}{G}] =$	3.445	(6.532)
4,3	$G_1 = KA/L\ (.419)(1.185)(1.185)/.03 =$	19.612	
	$G_2 = (.00076)(1.270)(1.270)/.02 =$	0.061	
	$G_T = 1/[\frac{1}{G}+\frac{1}{G}] =$	0.061	(0.116)
4,7	G = SPREADING W = 0.1060" L = 1.067" T = 0.0593 K = 0.419	G = .9598 W/°C	(1.8198 B/hr °F)
7,8	$G = K\frac{A}{L} = (419)(4)(1.185)(.01)/.175 =$	0.113	(0.215)
8,9	G SPREADING W = .01 L = .6 T = .293 K = 0.419	G = 0.0434	(0.0822)
6,9	$G = K\frac{A}{L} = (.00076)(.6^2)/.011 =$	.0025	(.0047)
6,8	$G = K\frac{A}{L} = (.00076)(1.185^2 - .6^2)/.11 =$	.0072	(.0137)

PREPARED BY	CHECKED BY	REVISED BY
BZ 3-20-84		

EXTERNAL CONVECTION

		W/°C	B/HR °F
9, 1	$G = hA = (.0026)(.6^2) = .00094$		(.00177)
8, 1	$G = hA = (.0026)(1.185^2 - .6^2 + 4)(1.185)(.145) = .0045$		(.00854)
7, 1	$G = hA = (.0026)(4)(1.185)(.06) = .00074$		(.00140)
4, 3	$G = K\frac{A}{L} = (.00076)(1.185^2)/.02 = .05336$		(.10118)

RADIATION - INTERNAL

6, 9

$F = 0.7$
$\varepsilon_1 = 0.7$
$\varepsilon_2 = 0.35$
$A_1 = (1.15)^2$
$A_2 = (0.6)^2$

$F_{1-2} = \frac{1}{\left[\frac{1}{F_{12}} + \left(\frac{1}{\varepsilon_1} - 1\right) + \frac{A_1}{A_2}\left(\frac{1}{\varepsilon_2} - 1\right)\right]} = .11521$

$G = F_{12} A_1 = .15237 \text{ in}^2$ (.00106 A²)

6, 8

$F = 0.3$
$\varepsilon_1 = 0.7$
$\varepsilon_2 = 0.35$
$A_1 = (1.15^2) = 1.3225 \text{ in}^2$
$A_2 = (1.165^2 - .6^2 + 4)(1.165)(.145) = 1.673$
w/ side area included $A_1 = 1.4575$

$F_{12} = .19121$
$G = .25287 \text{ in}^2 = .00176 \text{ ft}^2$

$F_{12} = .18665$
$G = .26831 \text{ in}^2 = .00186 \text{ ft}^2$ (.00186 A²)

PROJECT	MARTIN MARIETTA AEROSPACE ORLANDO DIVISION	PAGE	TEMP.	PERM.
MICROELECTRONICS		4		
MODEL HYBRID		REPORT		

RADIATION - EXTERNAL

	F	ϵ_1	ϵ_2	A_1	A_2	$\frac{in^2}{FA}$	$\left(\frac{ft^2}{FA}\right)$
9, 2	1	.7	1	.36	∞	.252	.00175
8, 2	.75	.7	1	1.73	∞	.982	.00682
8, 3	.5	.7	.8	.69	∞	.284	.00197
7, 2	.5	.7	1	.28	∞	.115	.00080
7, 3	.5	.7	.8	.28	∞	.115	.00080

4, 3

$F_{12} = .95$
$\epsilon_1 = .7$
$\epsilon_2 = .8$
$A_1 = 1.404$
$A_2 = 1.404$

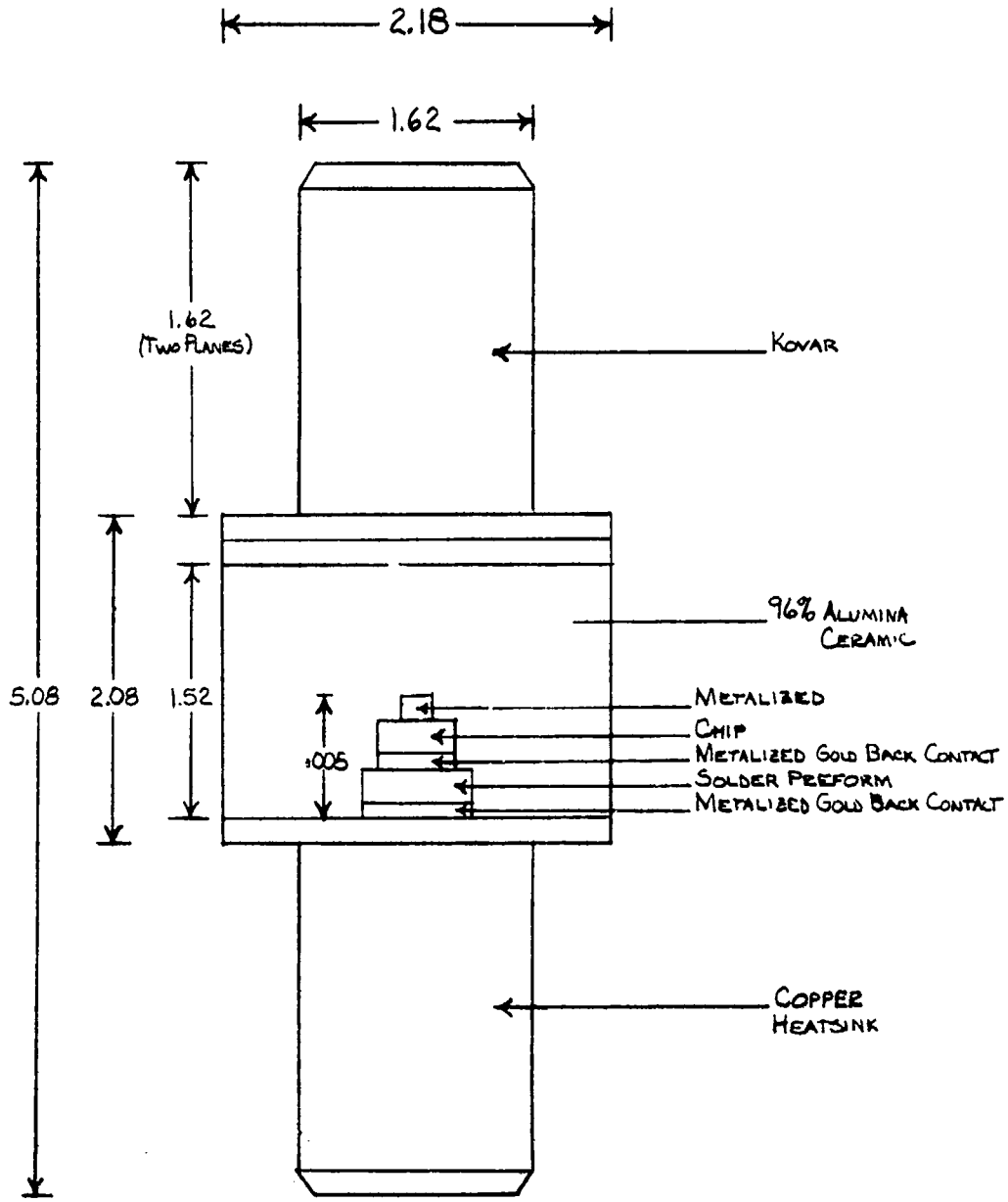
$F = .578$

$FA = 0.811\ in^2 = (.00563\ ft^2)$

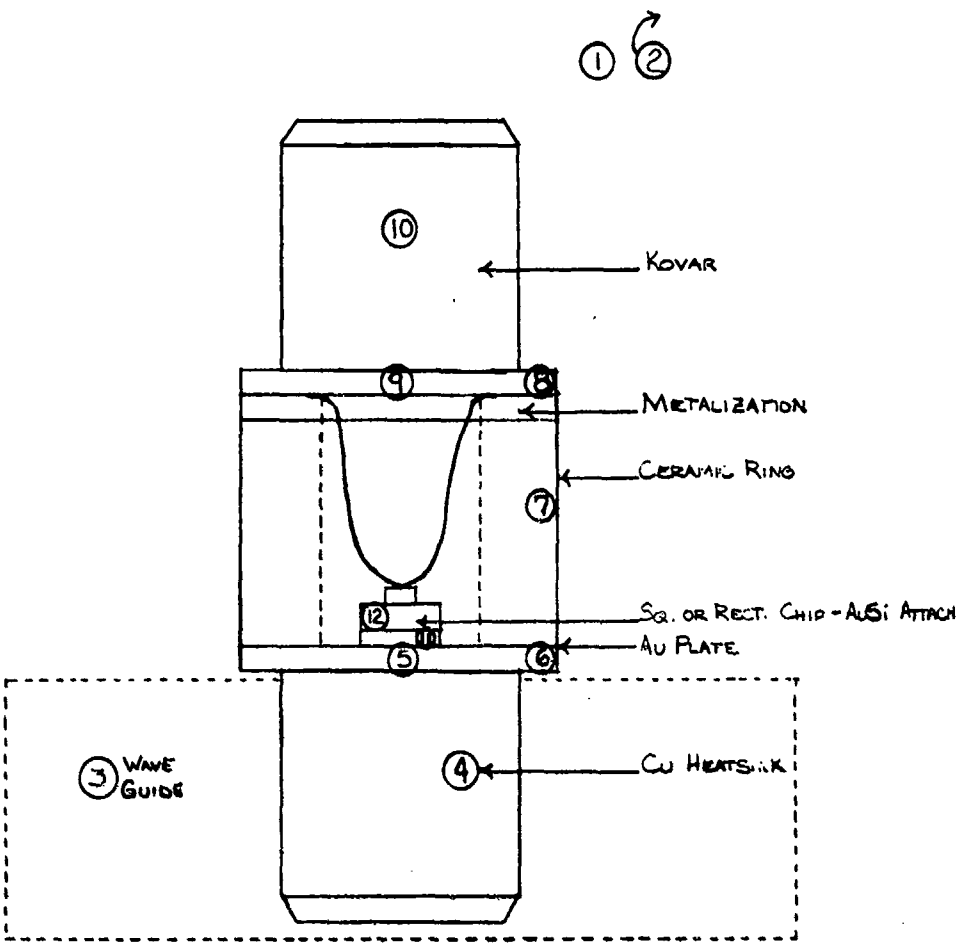
PREPARED BY	CHECKED BY	REVISED BY
B 3-22-84		

Appendix 6.6. Axial Stud Package

The figures in this appendix are referred to in section 5.4.3.6. They also supplement the work described in that section.



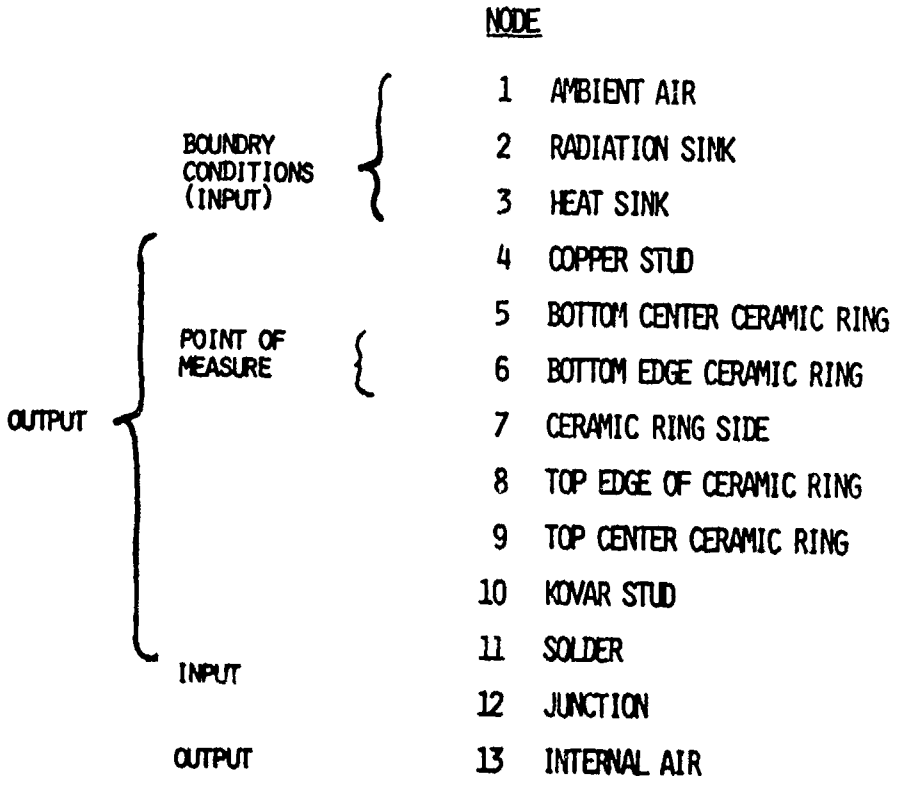
Axial Stud Package



WIRE: GOLD RIBBON: 2 MILS WIDE X .5 MILS THICK

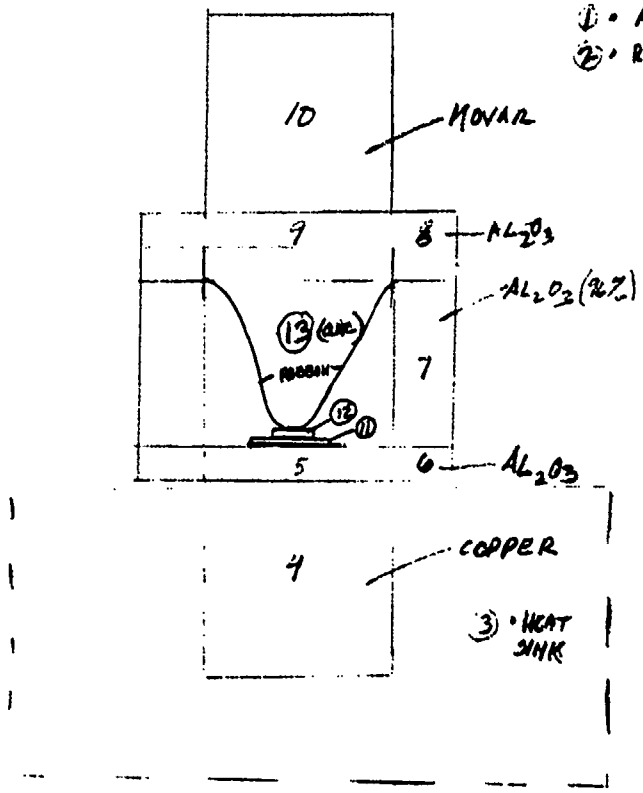
AXIAL STUD PACKAGE

AXIAL STUD PACKAGE NODAL DESCRIPTION



Form D-3061 April 1978

PROJECT MICROELECTRONICS	MARTIN MARIETTA AEROSPACE ORLANDO DIVISION	PAGE 1	TEMP.	PERM.
MODEL STUD		REPORT		



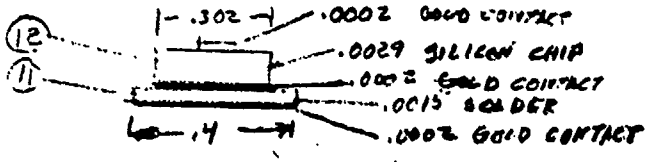
① · NR
② · RADIATION SINK

MATERIAL CONDUCTIVITY W/in°C

AL_2O_3	0.473
SILICON	2.13
GOLD	7.54
SOLDER	1.3
KOVAR	0.419
COPPER	9.66
AIR	.00076

h_c = 0.7 BTU/HR FT² °F
= .0026 W/IN² °C

PACKAGE



ASSUMED CHIP .305" square

PREPARED BY	CHECKED BY	REVISED BY

CONDUCTORS EXTERNAL

		W/°C	B/HR °F
1, 10	$hA = (.0026)[(\pi 1.62)(1.62) + \pi(.81^2)] =$	.02680	.05081
1, 8	$hA = (.0026)\pi[(3.18)(.28) + (1.09^2 - .81^2)] =$	.00933	.01769
1, 7	$hA = (.0026)(\pi)(3.18)(1.52) =$	.02707	.05132
1, 6	$hA = (.0026)(\pi)(2.18)(.28) =$	.00499	.00945
6, 3	$hA = (4.965)(\pi)(1.09^2 - .81^2) =$	2.448	4.643
4, 3	$hA = (7.3)(\pi)(1.62)(1.62) = 60.187$		
	$2\pi K \frac{L}{\ln \frac{r_2}{r_1}} = (7.66)(1.62) / \ln \frac{.81}{.4} = 139.36$		
	$G = \frac{1}{G_1} + \frac{1}{G_2} =$	42.03	79.70

CONDUCTORS INTERNAL

4, 5	$K\frac{A}{L}$ $(9.66)(\pi)(.81^2)/.81 = 24.58$		
	$(0.478)(\pi)(.81^2)/.14 = 7.04$		
	$G = \frac{1}{G_1} + \frac{1}{G_2} = 5.477$	= 5.471	10.37
5, 6	$G\frac{2\pi KL}{\ln \frac{r_2}{r_1}} = \frac{(2\pi)(.478)(.25)}{\ln .95/.5} =$	= 1.310	2.484
6, 7	$K\frac{A}{L} = (.478)(\pi)(1.09^2 - .81^2)/.90$	= 0.8876	1.6831
7, 8	SAME as 6, 7		1.6831
8, 9	same as 5, 6		4.20
9, 10	$K\frac{A}{L}$ $(.478)(\pi)(.81^2)/.14 = 7.04$		
	$(.419)(\pi)(.51^2)/.81 = 1.067$		
	$G = \frac{1}{G_1} + \frac{1}{G_2}$	0.926	1.756
12, 8	(RIBBON) $A = (.002)(.0005) = 1E\text{-}6\ in^2$		
	$L = \approx 1.6$ IN		
	$G = K\frac{A}{L} = (7.54)(1.2E\text{-}6)/1.6 =$	.00001	.00002

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Form D-3081 April 1978

PROJECT	MARTIN MARIETTA AEROSPACE ORLANDO DIVISION	PAGE	TEMP.	PERM.
MICROELECTRONICS		3		
MODEL STUD		REPORT		

CONDUCTION. CHIP + CASE

				W/°C	B/HR°F
12, 11	kA/L	(.13)(.305²)/.002	= 47.07		
		(9.66)(.305²)/.0002	= 44193.1		
		(1.3)(.4²)/.00075	= 2773.		
		G = 1/Σ 1/R	=	71.82	136.19
11, 5	kA/L	(1.3)(.4²)/.00075	= 2771.		
		(.715)(1²)/.14	= 3.414		
		G = 1/Σ 1/R	= 3.373	3.373	6.395

INTERNAL CONVECTION

h = 0.4 B/HRFT²°F = .00146 W/CM²°C

12, 13	hA	(.00146)[(.305²+.002²)(π)(1)]	= .00044	.00021	
13, 5	hA	(.00146)[(π)(.51²)−.4²]	= .00384	.00185	
13, 7		(.00146)(π)(1.62)(1.52)	= .01129	.02142	
13, 9		(.00146)(π)(.51²)	= .00301	.00571	
13, 11		(.00146)[.4²−.305²+(4)(1)(.002)]	= .00010	.00019	

Radiation. EXTERNAL

				m²	ft²
10, 2		FCA = (.5)(.35)(π)(1.62)(1.62)		1.443	
		(1)(.35)(π)(.81²)		.7214	
8, 2		(.5)(.7)(π)[1.09²−.81²]	= .58496	2.1643	.01583
		= (.5)(.7)(π)(2.18)(.26)	= .31116		
			= 1.23612	1.2561	.00872
7, 2		FCA = (.5)(.7)(π)(2.18)(1.52)	=	3.6913	
6, 2		FCA = (.5)(.7)(2.18)(.26)(π)	=	.6112	

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Form D-3081 April 1978

PROJECT MICROELECTRONICS	MARTIN MARIETTA AEROSPACE ORLANDO DIVISION	PAGE 4	TEMP.	PERM.
MODEL STUD		REPORT		

RADIATION - EXTERNAL (CONTINUED)

8,10	F_{11} [illegible]	F_{12} = .35651		
	F_2 [illegible]			
	F_1 .7			
	F_2 = .35	FA = .59573	.5957	.00414
	A_1 1.611			
	A_2 2.215			
10,5	FFA (.3218)(.35)([illegible])		.9285	.00645
8,3	FFA (.5)(.7)(2.215)([illegible])		.21364	.00148
7,3	FFA = [illegible]		3.643	.0253
6,3	FFA = (.5)(.7)(2.215)(.035)(π)		.6712	.00466

RADIATION - INTERNAL

12,9	F_{11} = .888	F_{12} = .1712		
	F_1 .5			
	F_2 .7			
	A_1 .0785	FA = .112	.04412	.00031
	A_2 2.061			
12,7	F .855	F_{12} .07516		
	[illegible]			
	[illegible]	FA = .00705	.00705	.00005
	A [illegible]			

11,9 + 11,7 - [illegible]

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B.J. 3-26-84		

Form 0-3001 April 1970

PROJECT MICROELECTRONICS	MARTIN MARIETTA AEROSPACE ORLANDO DIVISION	PAGE 5	TEMP.	PERM.
MODEL STUD		REPORT		

RADIATION - INTERNAL (CONTINUED)

5,9 F_{12} .433 $\quad$ $\sqrt{2.115^2 + 1.62^2} = 1.315$

C_1 .7

C_2 .7

A_1 1.968

A_2 2.061

$F_{12} = \frac{1}{1.62}(2.115 + 1.315) = .433$

F_{12} 0.3177 $\quad$ IN²

$FA = 0.625$ $\quad$ .625 $\quad$ .1351

5,7 F_{12} .567

C_1 .7

C_2 .7

A_1 1.965

A_2 7.136

$FA = 0.8635$ $\quad$ IN² $\quad$ .563 $\quad$ .1216

Summary

13 NODES (2 BOUNDARY)

20 CONDUCTORS

13 RADIATORS

1 SOURCE (12)

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APPENDIX 7.0

MEASUREMENT TESTS

7.1 Temperature Measurement Tests

- o Open Air Test
- o Printed Wiring Board Mounting

7.2 Hermetic Chip Carrier Thermal Test

APPENDIX 7.1

TEMPERATURE MEASUREMENT TESTS

Test Objectives

The basic objective of this task was to generate actual thermal gradient data for a standard package. This data can be used to verify thermal models for the generation of derating curves.

Test objectives were to:

1 Develop capabilities to measure junction and test point temperatures

2 Control and determine package power output for the test package

3 Calculate junction to test point resistance

4 Determine the best measurement point to externally establish junction temperature derating.

Test Result Summary

It appears that the best measuring points for determining the junction temperature are the lid and the center lead of the package. Both had a high correlation factor with the junction to power.

Test Hardware and Procedure

A standard 40-lead side-brazed package was chosen as the test package because of its popularity in the industry. The package had an NPN 2NC5337 transistor mounted in the die cavity for power dissipation. A transistor was used instead of a resistor because the junction temperature of the transistor is directly proportional to the reverse bias resistance of the base-emitter junctions. Attached to the package on the lid, center lead, and end lead of the package were three mil chromel - constantan thermocouples, used to measure the gradient across the package when power is applied to the transistor. The small thermocouples were chosen because of the small amount of heat they would draw off. The packages were configured in two fashions: one was unmounted (open air), while the other was mounted to a printed wiring board (PWB). For more information, see the section on test configuration conditions and power levels.

Power Dissipation Measurement

To generate heat, the transistors were dc biased, using a load and base resistor, as shown in Figure 79. The power dissipated was calculated in watts by measuring the voltage drop across the collector-emitter of the package, multiplied by the voltage drop across the load resistor, and divided by the load resistor's resistance. The base resistor was adjusted so that all the packages were dissipating about the same power. The main supply collection voltage was then adjusted to vary the power of all the test packages.

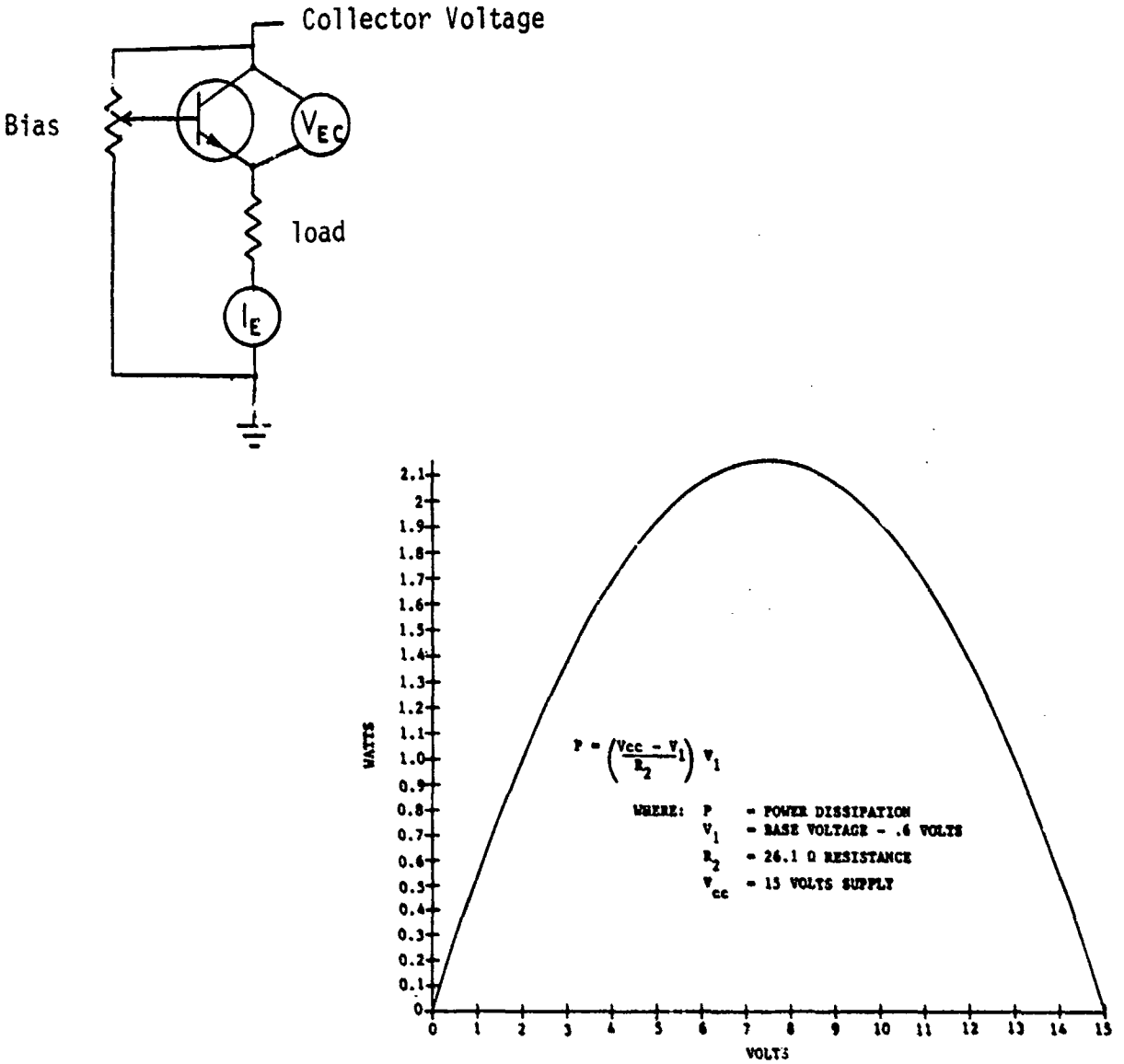


Figure 79. Power Dissipation Circuit

Junction Temperature Measurements

The relationship of the voltage drop across the emitter-base junctions, when biased by a constant power supply and temperature, is shown in Figure 80. The relationship mentioned is linear over the test temperature (25 to 130 degrees C.). Therefore, the package's voltage drop was expressed by the linear equation $y = Mx + B$, where y equals junction temperature, x equals voltage drop, and M and B are constants. The constants were found by measuring the voltage drop at known temperatures and fitting the data in the equation by the least squares method described in the section on calibration.

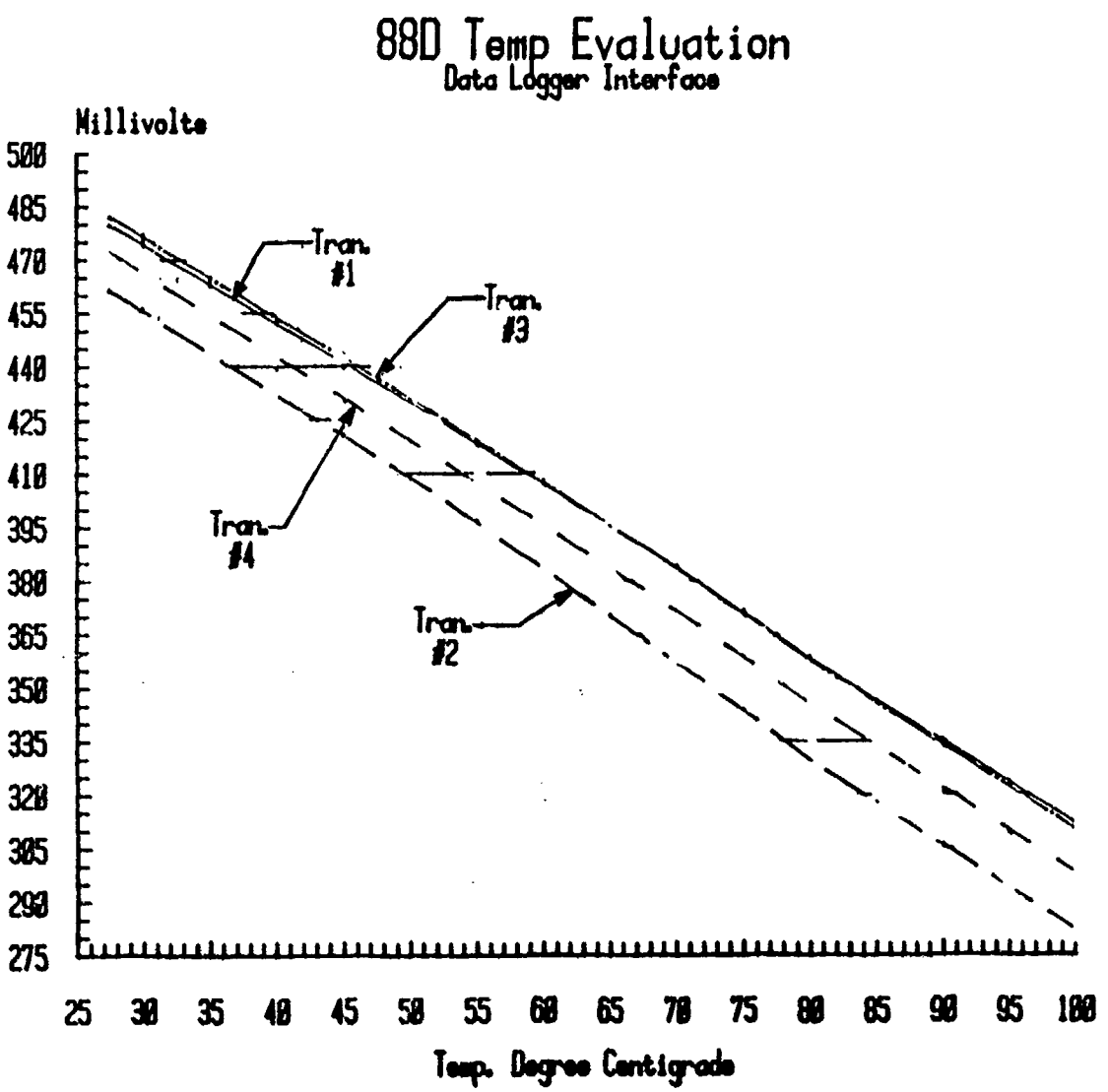


Figure 80. Transistor Calibration Curve (Typical)

The package's junction temperature was determined by switching the power dissipation circuit off and by switching the reverse bias circuit into place. The final circuit that was used is shown in Figure 81. The relay was activated, isolating the emitter and base junctions. Then the voltage drop across the reversed biased emitter-base junctions was measured. The total off-time of the powering circuit was about 30 milliseconds. This short off-time did not allow the junction to cool off significantly. The Fluke datalogger then converted this voltage to the junction temperature.

Thermal Resistance Calculation

To determine the thermal resistance from the device junction to the test points, it was necessary to measure the power dissipation, junction temperature, and test points with the Fluke 2240C datalogger. The junction

temperature was determined by the technique mentioned earlier and was recorded by the datalogger. The power was determined by measuring the various voltages and using the equation previously mentioned in the power dissipation section. The Hewlett-Packard 9836 computer was used to calculate and record the wattage. The test point temperatures were measured by the thermocouples and the datalogger, and recorded by the computer. The accuracy of the datalogger is as follows.

Worst case resolution	0.1 degree
NBS conformity	0.11 degree
System accuracy	0.7 degree

The temperature delta was then calculated by taking the difference of the two test points, (the lid and the package junction), and dividing it by the power dissipated. This gives an answer in degrees centigrade per watt (°C/W).

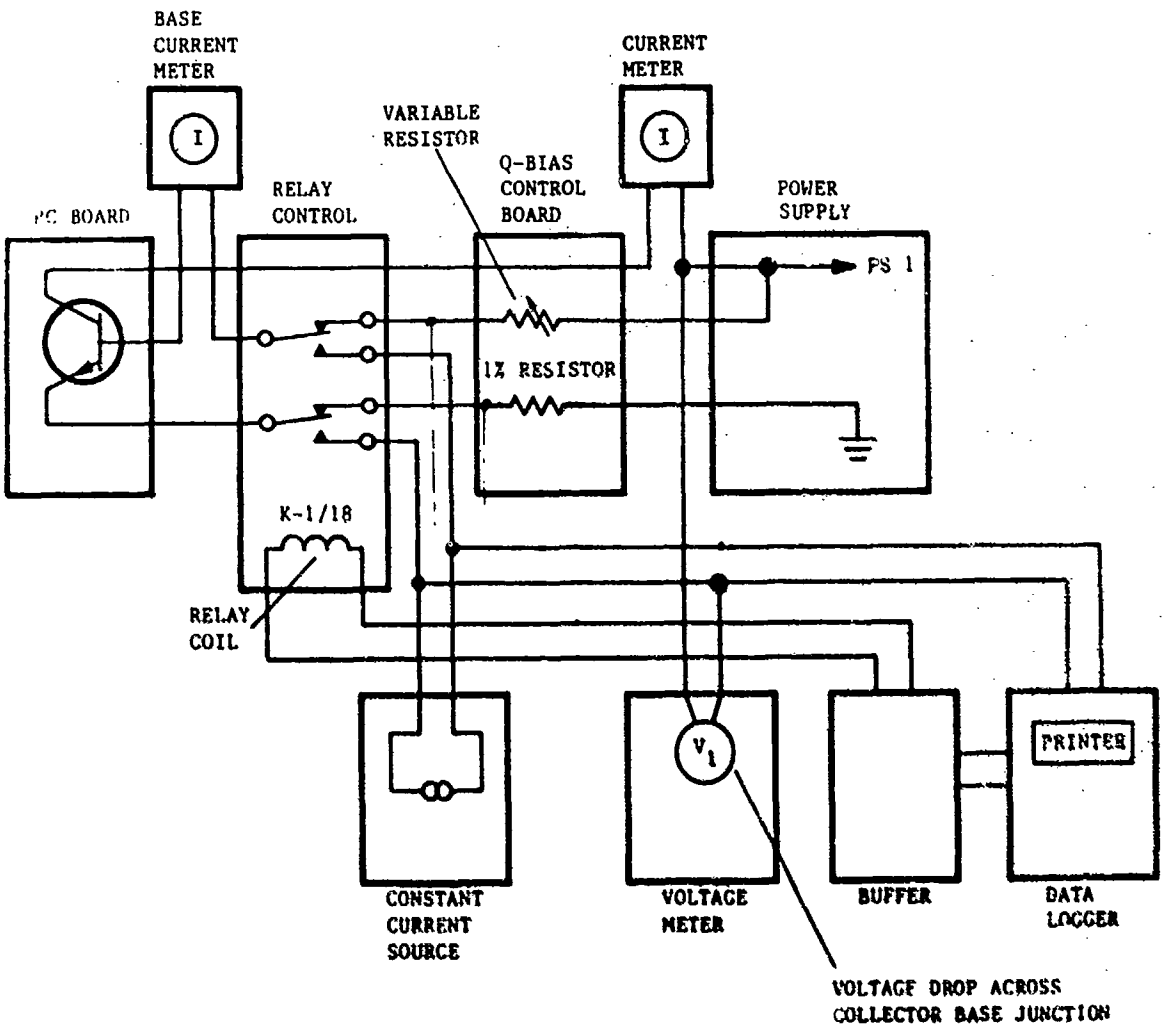


Figure 81. System Block Diagram

Calibration

The junctions were all calibrated by measuring the voltage drop of the reverse biased E - B junction with respect to temperature. This was done at 15 steps over the temperature range of -10 to 130 degrees Centigrade. This data was fitted to a curve, as shown in Figure 82, to produce a linear equation for each transistor. Figure 83 also shows the amount of error typically encountered by this method over the temperature range. This was done prior to each test to increase the accuracy.

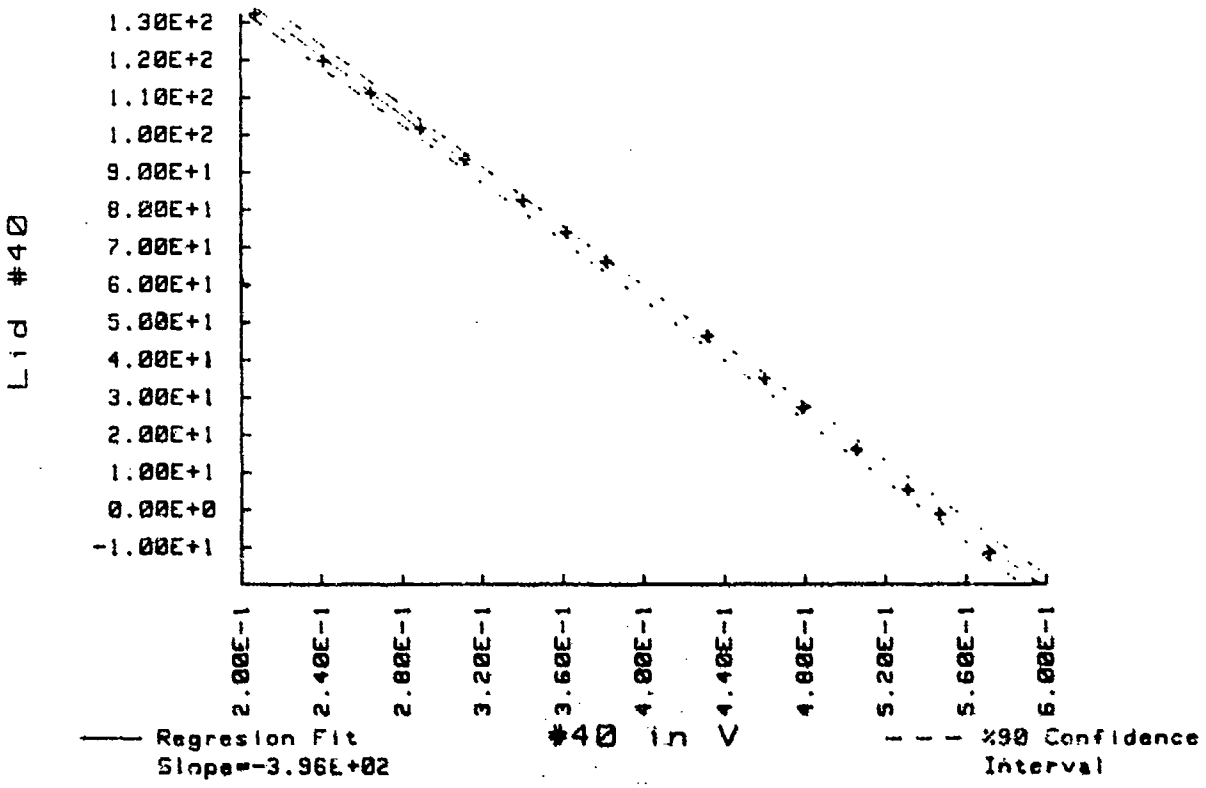


Figure 82. Transistor Calibration Test 2/1/84

Test Configuration, Conditions, and Power Setting

Two different test configurations were chosen. The first was an open air test where the package was not mounted. The second was a PWB test, which consisted of mounting the packages to a polyimide PWB.

Open Air Test

The packages in this test were not mounted. The test points measured were the lid, center lead, end lead, junction, and the case under the package. This test was chosen to give data to the thermal model on the effects of radiation and air convection. The test was performed inside a temperature oven to prevent any air currents from coming in contact with the packages. The ambient chamber air was 25 degrees centigrade. The wattage was

****

POLYNOMIAL REGRESSION ON DATA SET:

Transistor Calabration Test 3/4/84

****

--where: Dependent variable = (5)Lid #41
Independent variable = (39)#41 in V

VARIABLE	N	MEAN	VARIANCE	STANDARD DEVIATION	COEFF. OF VARIATION
#41 in V	15	.40314	.01342	.11583	28.73265
Lid #41	15	58.99333	2135.88924	46.21579	78.34070

CORRELATION = -.99986

SELECTED DEGREE OF REGRESSION = 1
R-SQUARED = .99972
STANDARD ERROR OF ESTIMATE = .800607086159

ANALYSIS OF VARIANCE TABLE

SOURCE	DF	SUM OF SQUARES	MEAN SQUARE	F-VALUE
TOTAL	14	29902.50933		
REGRESSION	1	29894.25670	29894.25670	46638.96
X^1	1	29894.25670	29894.25670	46638.96
RESIDUAL	13	8.33263	.64097	

VARIABLE	REGRESSION COEFFICIENTS STD. FORMAT	E-FORMAT	STANDARD ERROR REG. COEFFICIENT	T-VALUE
'CONSTANT'	219.81857	.219818574050E+03	.77286	284.43
X^1	-398.93149	-.398931490598E+03	1.84724	-215.96

	COEFFICIENT	90 % CONFIDENCE INTERVAL LOWER LIMIT	UPPER LIMIT
'CONSTANT'	219.81857	218.44057	221.18758
X^1	-398.93149	-402.20362	-395.65936

TABLE OF RESIDUALS

OBS#	OBSERVED Y	PREDICTED Y	RESIDUAL	STANDARDIZED RESIDUAL	SIGNIF.
1	-12.50000	-11.32233	-1.17767	-1.47097	
2	-1.00000	-.31182	-.68818	-.85957	
3	5.50000	6.03119	-.53119	-.66348	
4	15.80000	15.84490	-.04490	-.05609	
5	27.10000	26.61605	.48395	.60447	
6	34.60000	33.95639	.64361	.80390	
7	45.70000	44.92701	.77299	.96551	
8	65.20000	64.35497	.84503	1.05548	
9	72.30000	72.01446	.78554	.98118	
10	81.30000	80.55159	.74841	.93480	
11	92.20000	91.64189	.35811	.44730	
12	100.30000	100.13913	.16087	.20094	
13	109.60000	109.75338	-.15338	-.19157	
14	118.10000	118.72933	-.62933	-.78607	
15	130.40000	131.97386	-1.57386	-1.96583	

Durbin-Watson Statistic: .268989728107

Figure 83. Transistor Calibration Test

adjusted so that the junction temperature did not exceed the maximum operating temperature of around 135 degrees centigrade. The desired power was around 2 watts.

Printed Wiring Board Test

In this test, all seven packages were mounted to a single piece of 0.047-inch standard double-sided polyimide fiberglass, with 1 ounce copper on the underside (Figure 84). The 1 ounce copper underside simulates the thermal spreading effect of circuitry normally found in actual hardware. The leads that are connected to the transistors were isolated from the copper ground plane. The PWB was not mounted to a heat sink. The test was performed in a thermal oven that was turned off. This test was performed at three different power levels: 1, 2, and 4 watts at 25 degrees centigrade ambient conditions, and at 55 and 85 degrees centigrade ambient conditions. A 2 watt power level was employed.

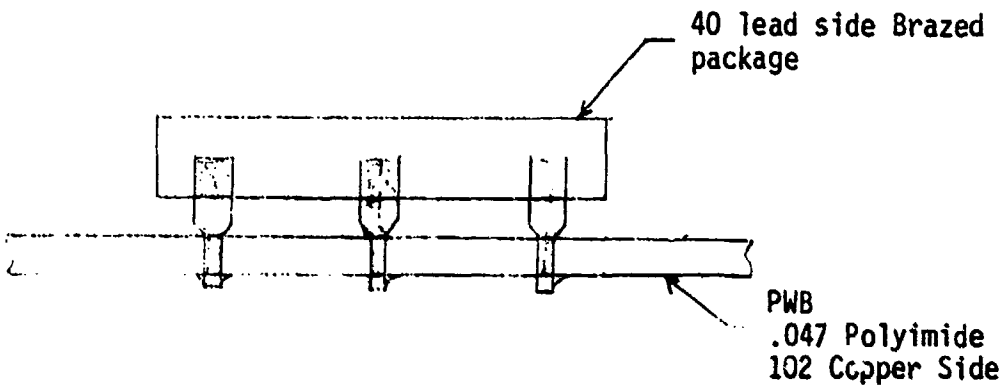


Figure 84. PWB Configuration

Transistor Thermal Test (Open Air)

Thermal Readings (Deg. C)

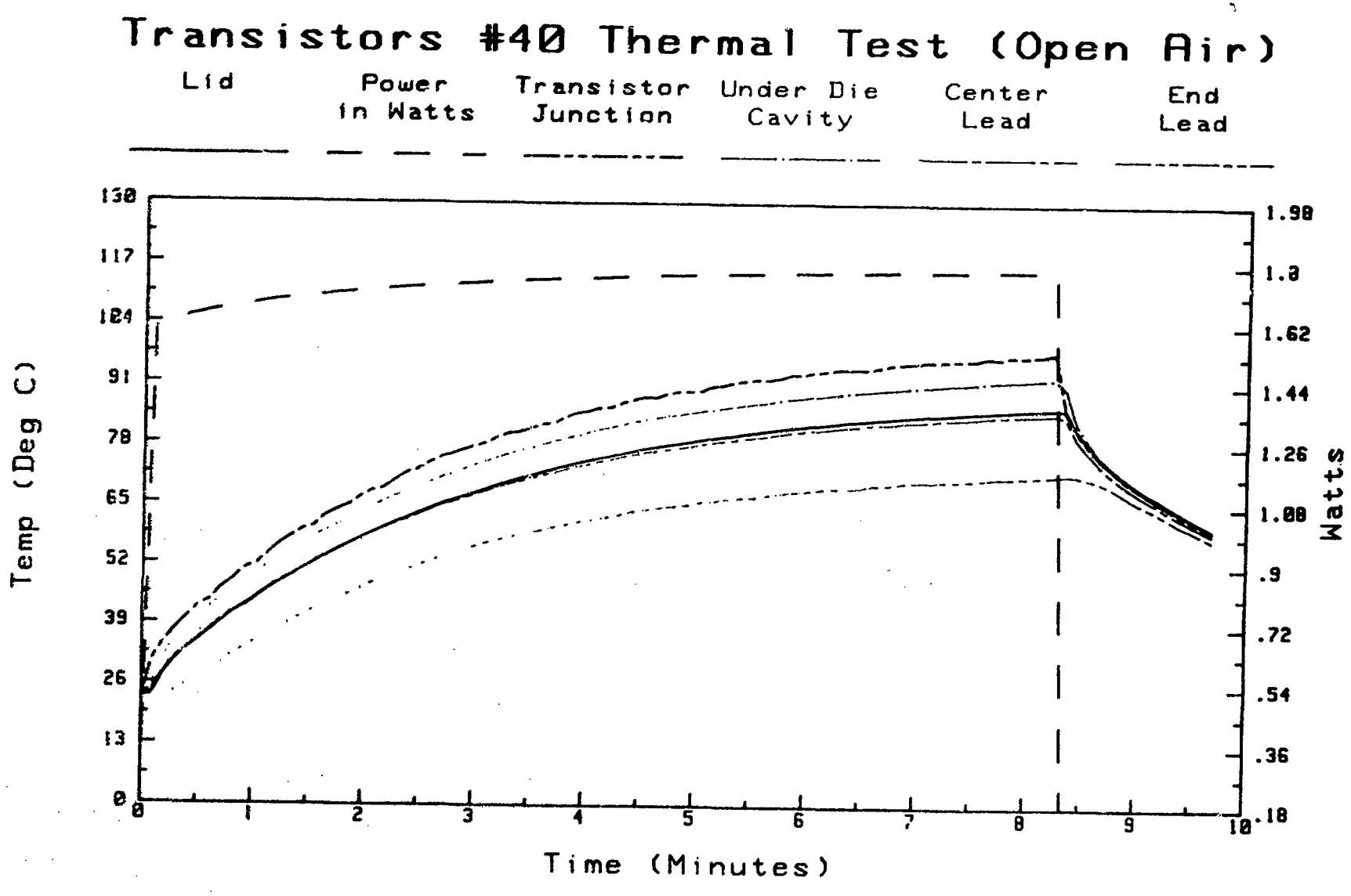
TRANS #	J	L	W	B	C	E
40	98.2	86.2	1.77	92.6	85.0	71.9
41	99.0	87.6	1.79	95.9	84.3	64.0
43	101.7	85.4	1.78	91.9	79.2	72.2
44	102.1	89.3	1.81	94.4	85.9	75.0
45	85.9	75.4	1.40	50.0	74.8	62.9
46	100.3	87.6	1.77	97.3	86.4	73.3
47	97.5	85.7	1.74	95.1	85.8	71.1

Theta Values (C/W)

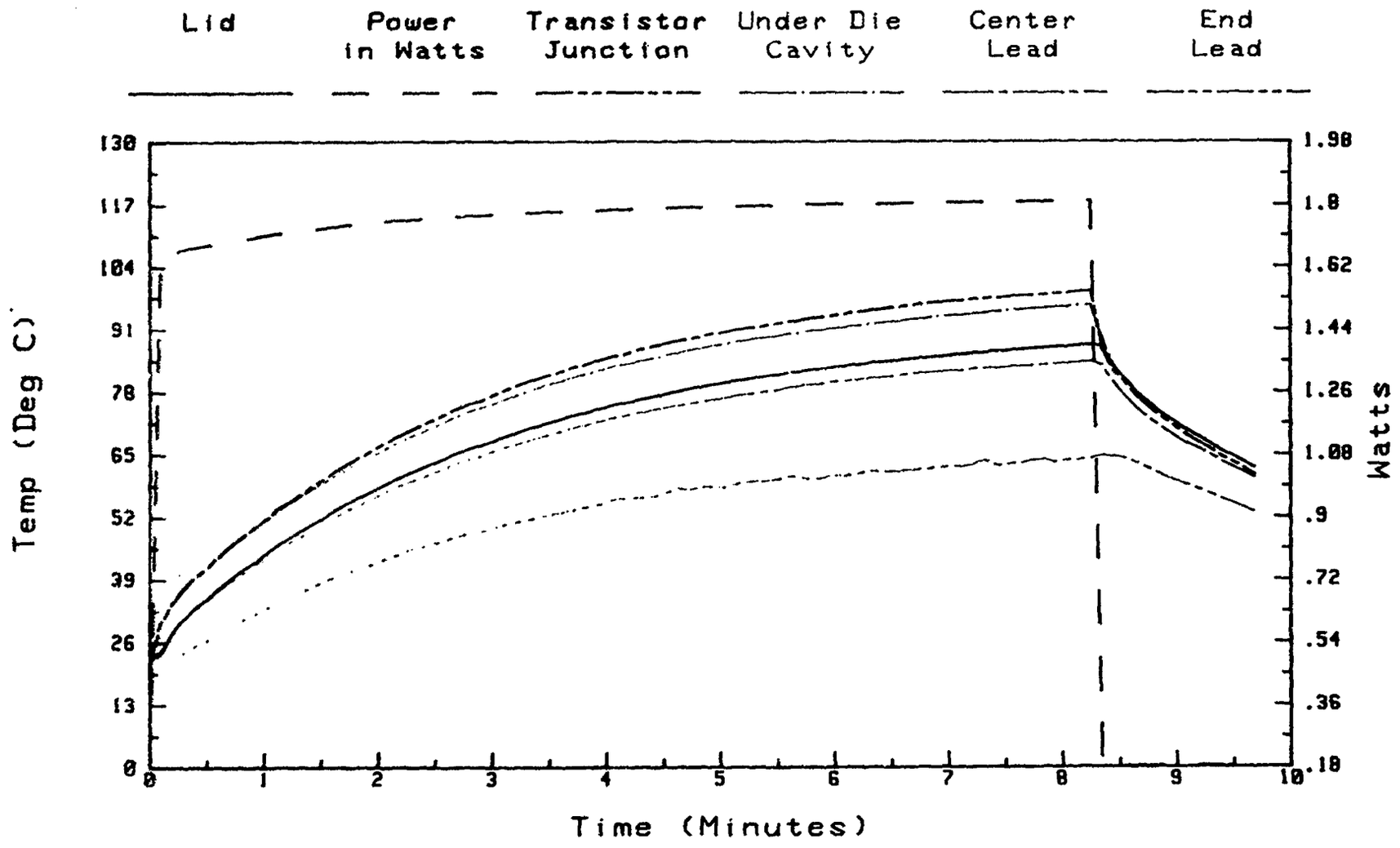
TRANS #	J/L	J/B	J/C	J/E	L/B	L/C	L/E
40	6.80	3.18	7.48	14.90	-3.63	.68	8.10
41	6.33	1.70	8.17	19.50	-5.41	1.06	12.38
43	9.17	5.51	12.66	16.60	-3.21	3.94	7.88
44	7.05	4.23	8.94	14.97	-4.54	.17	6.20
45	7.49	25.63	7.92	16.42	25.85	8.14	16.64
46	7.17	1.69	7.85	15.26	-6.28	-.11	7.29
47	6.78	1.37	6.72	15.18	-5.12	.23	8.69

J=TRANSISTOR'S JUNCTION
L=PACKAGE'S LID
B=UNDER DIE CAVITY (CASE TEMP)
C=PACKAGE'S CENTER LEAD
E=PACKAGE'S END LEAD
W=POWER (WATTS)

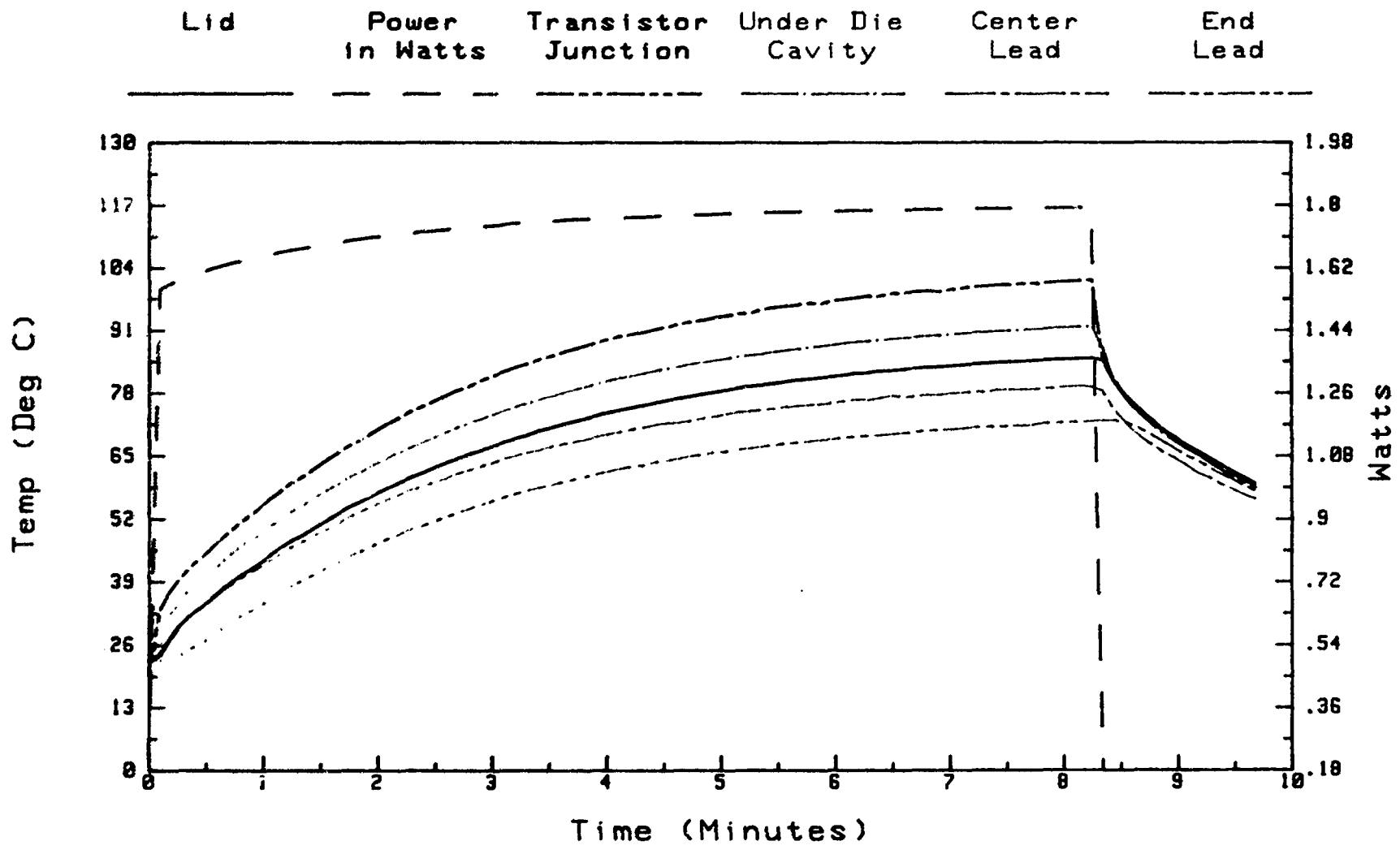
J/L=JUNCTION - LID
J/B=JUNCTION - BASE
J/C=JUNCTION - CENTER LEAD
J/E=JUNCTION - END LEAD
L/B=LID - BASE
L/C=LID - CENTER LEAD
L/E=LID - END LEAD



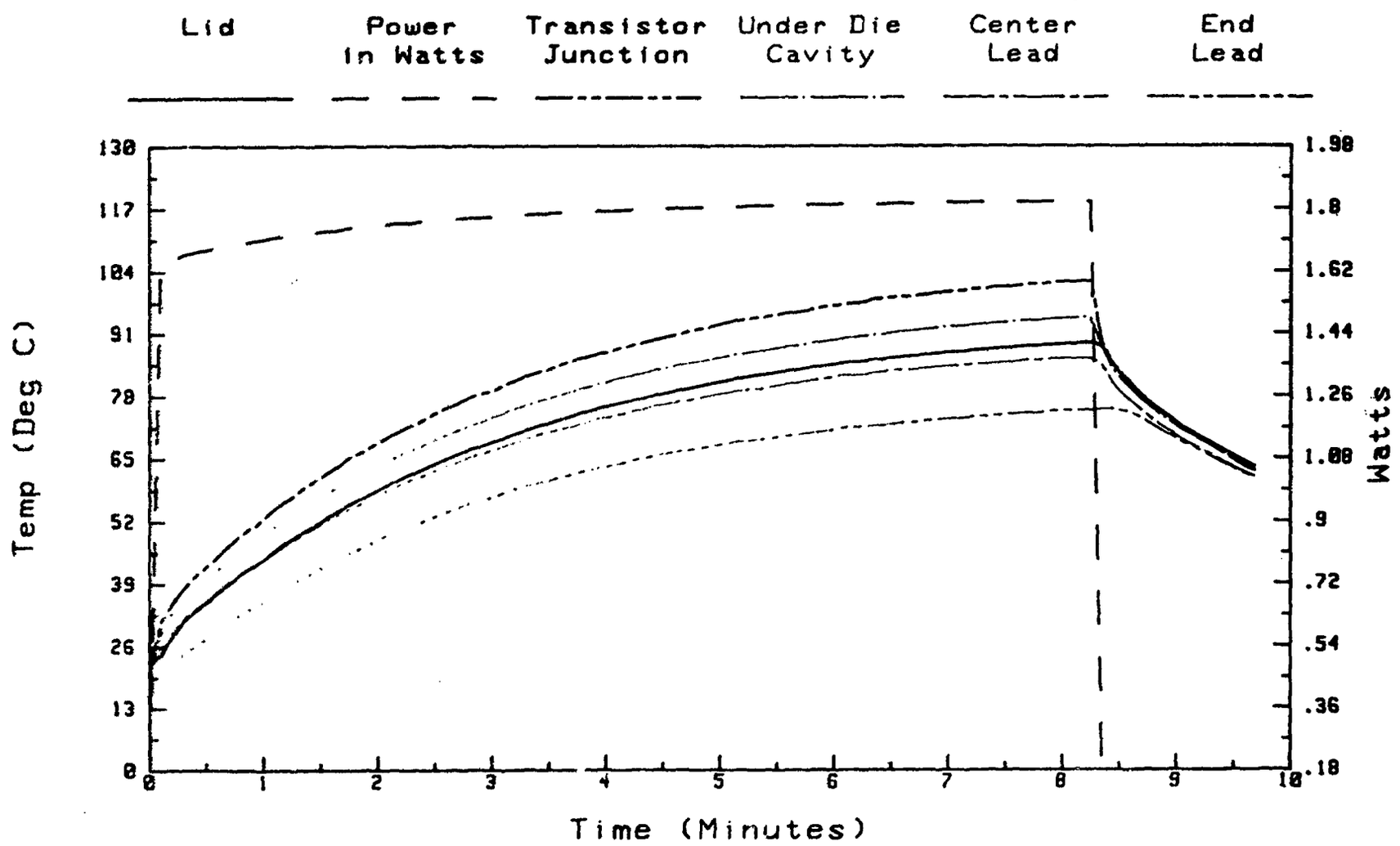
Transistors #41 Thermal Test (Open Air)



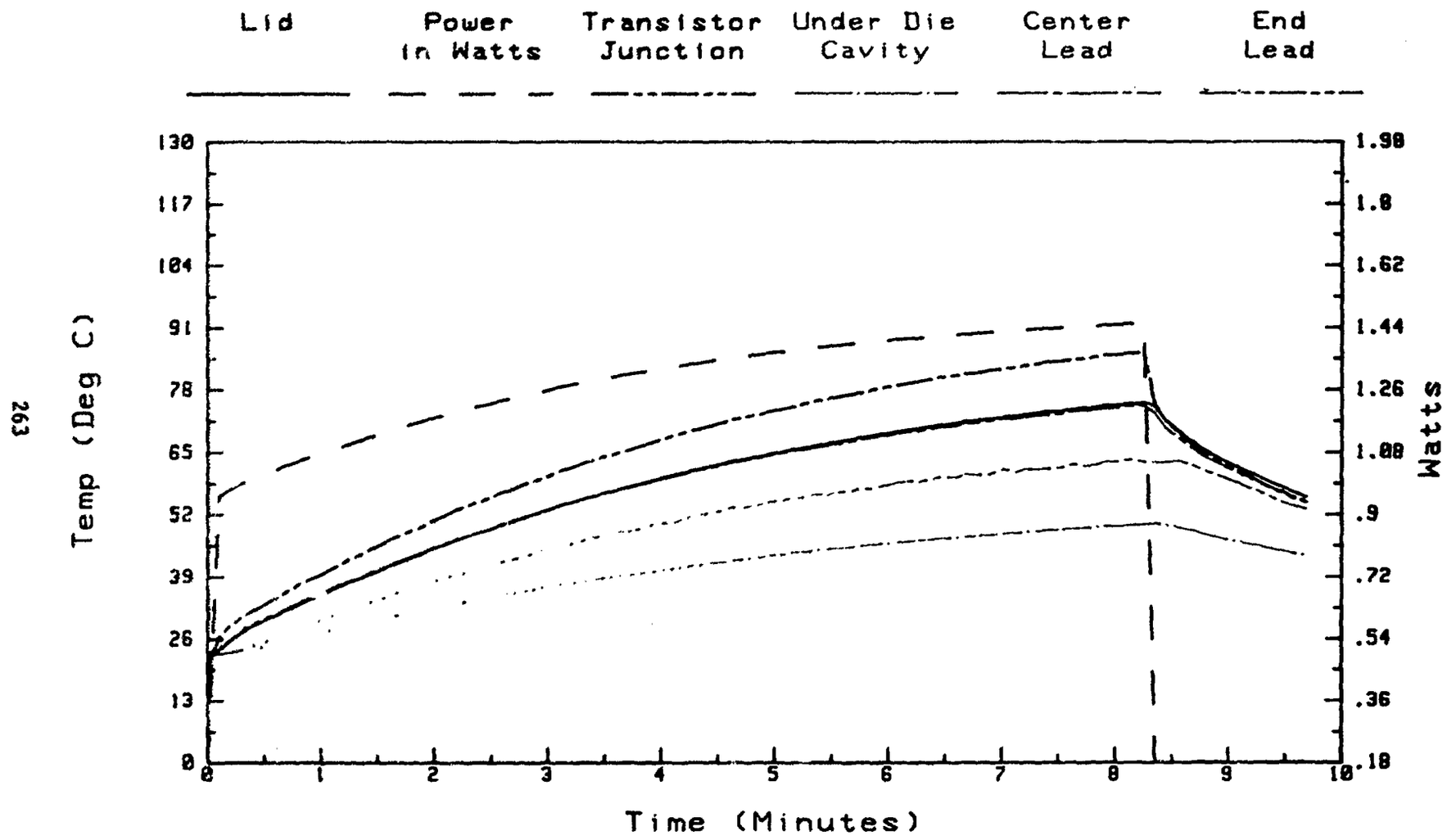
Transistors #43 Thermal Test (Open Air)



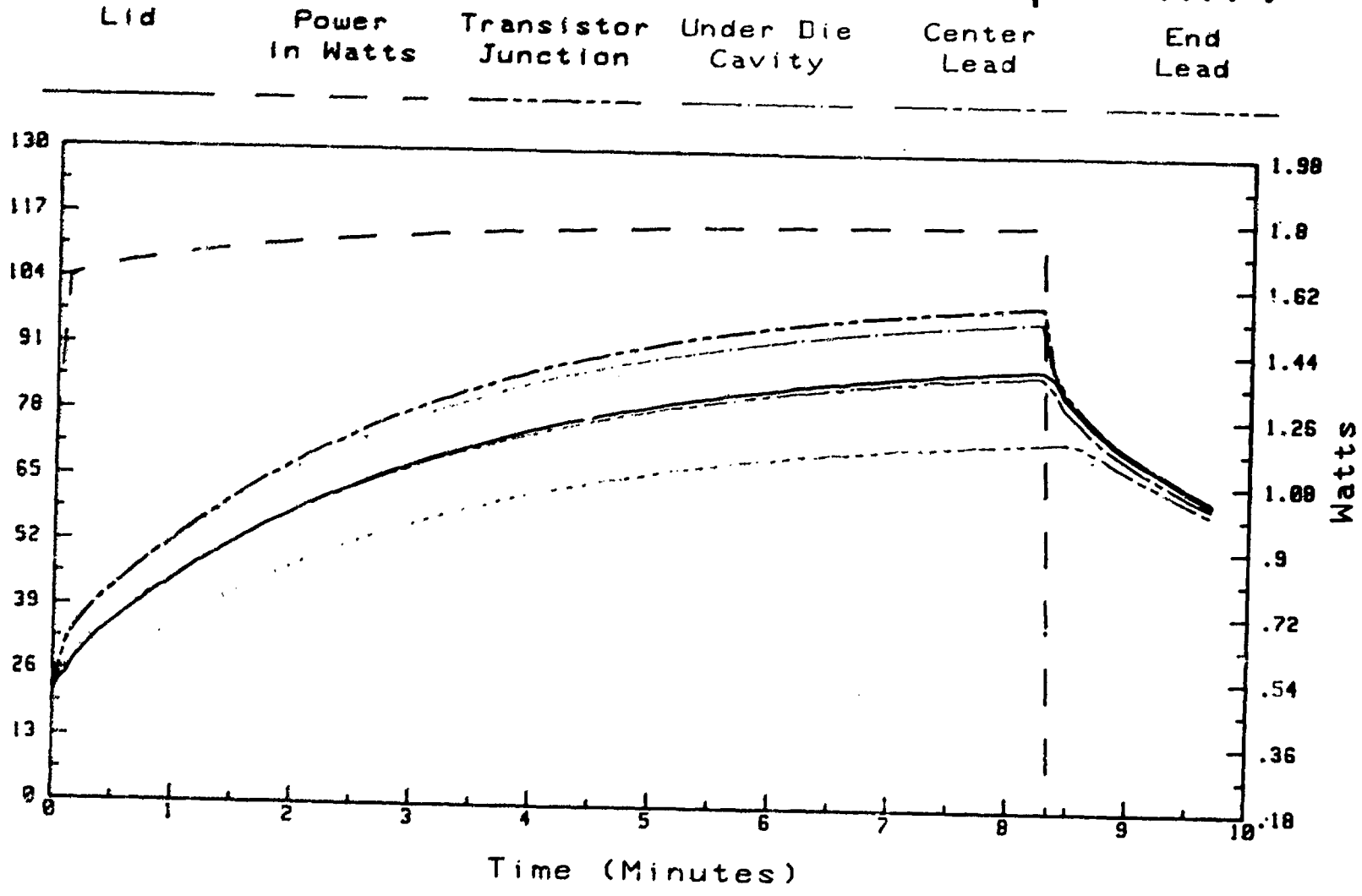
Transistors #44 Thermal Test (Open Air)



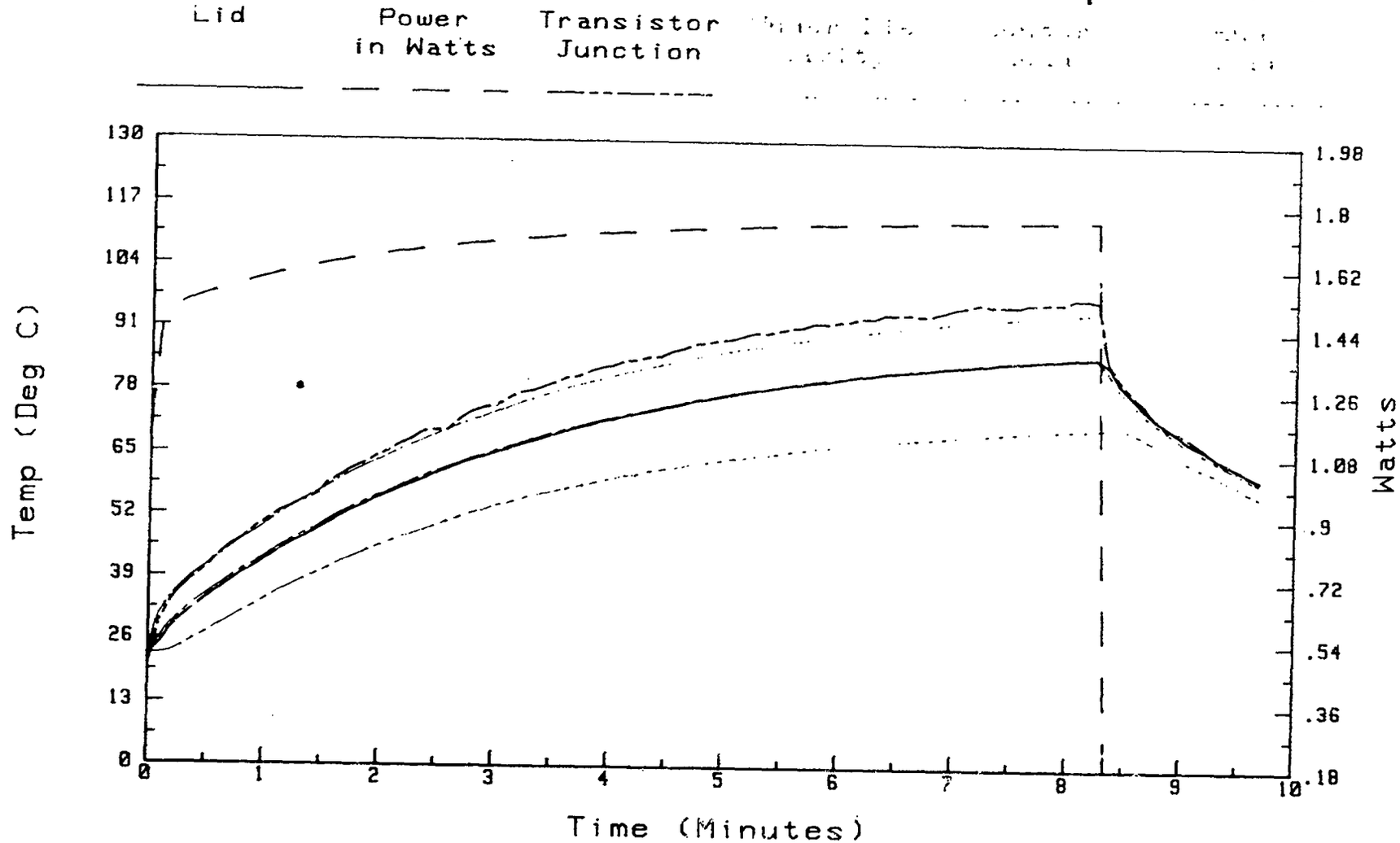
Transistors #45 Thermal Test (Open Air)



Transistors #46 Thermal Test (Open Air)



Transistors #47 Thermal Test (Open Air)



Transistor Thermal Test (PWB 1W 25C)

Thermal Readings (Deg. C)

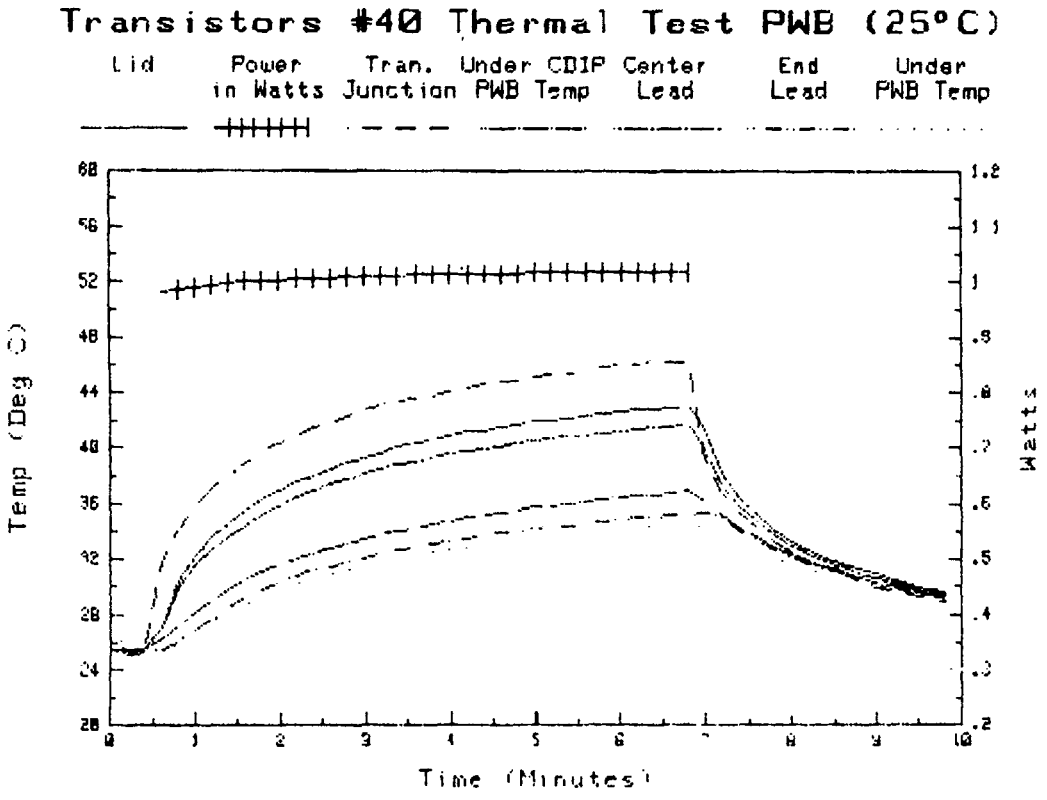
TRANS #	J	L	W	B	P	C	E
40	46.2	42.9	1.02	36.7	34.5	41.5	35.1
41	45.2	41.8	1.03	36.1	34.3	37.9	34.9
43	49.9	44.7	1.01	39.2	36.0	42.7	37.7
44	47.5	43.8	1.03	37.7	36.1	42.0	37.7
45	48.1	42.4	.99	36.4	34.9	41.0	35.1
46	47.0	43.1	1.01	39.7	35.7	41.0	36.4
47	46.5	43.0	1.00	40.2	35.6	42.0	35.7

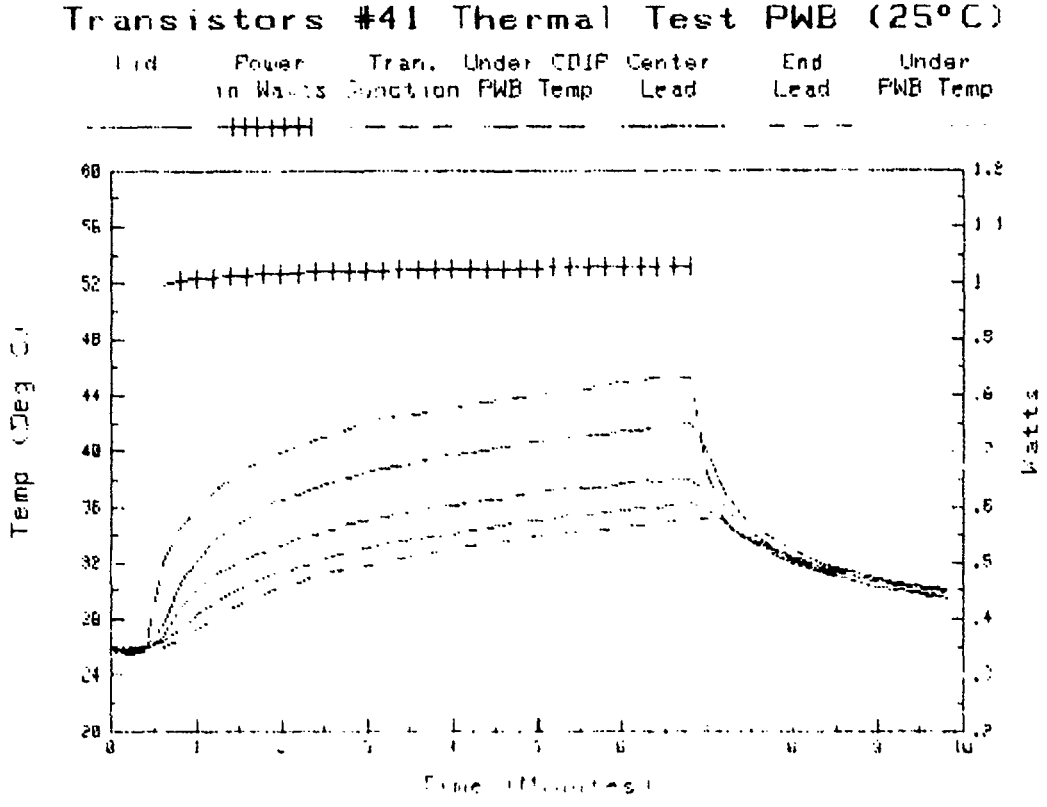
Theta Values (C/W)

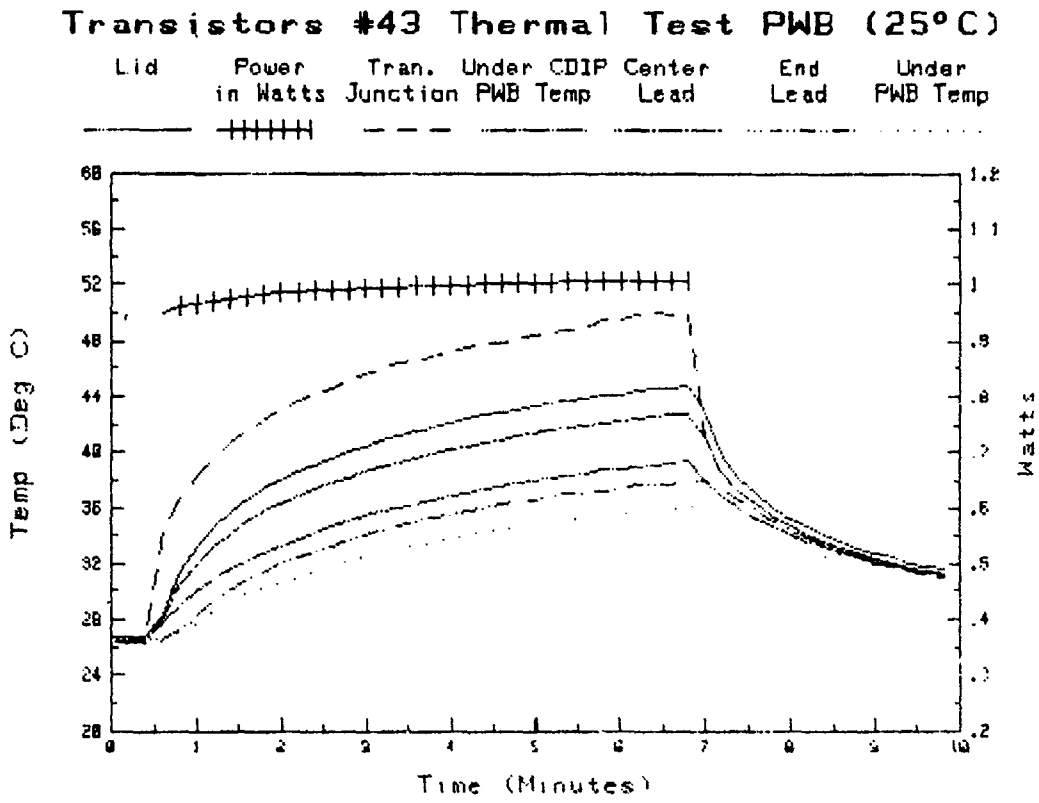
TRANS #	J/L	J/B	J/P	J/C	J/E	L/B	L/P	L/C	L/E
40	3.24	9.33	11.49	4.62	10.90	6.09	8.25	1.38	7.66
41	3.28	8.82	10.57	7.07	9.98	5.54	7.28	3.79	6.70
43	5.12	10.58	13.76	7.11	12.07	5.46	8.64	1.99	6.95
44	3.57	9.50	11.05	5.32	9.50	5.93	7.48	1.75	5.93
45	5.78	11.87	13.39	7.20	13.19	6.09	7.61	1.42	7.41
46	3.87	7.25	11.23	5.96	10.53	3.38	7.36	2.09	6.66
47	3.51	6.32	10.92	4.51	10.82	2.80	7.41	1.00	7.31

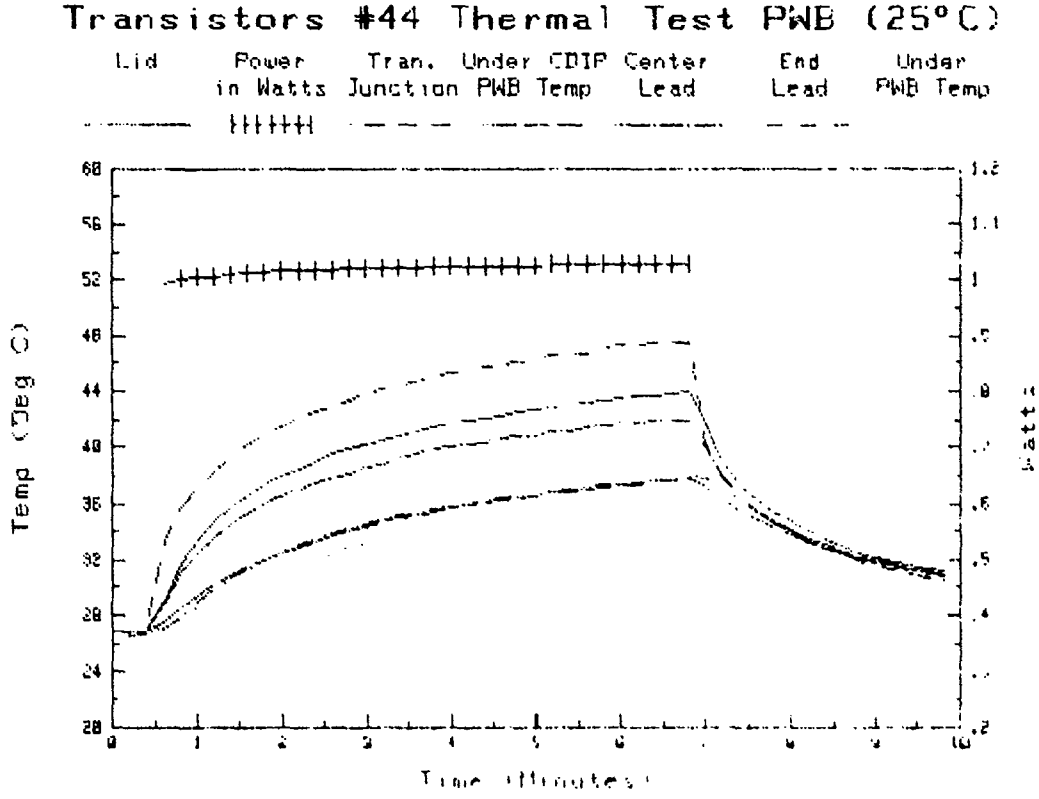
J=Transistor's Junction
L=Package's Lid
B=Under CDIP (PWB Temp)
P=Other Side of PWB from B
C=Package's Center Lead
E=Package's End Lead

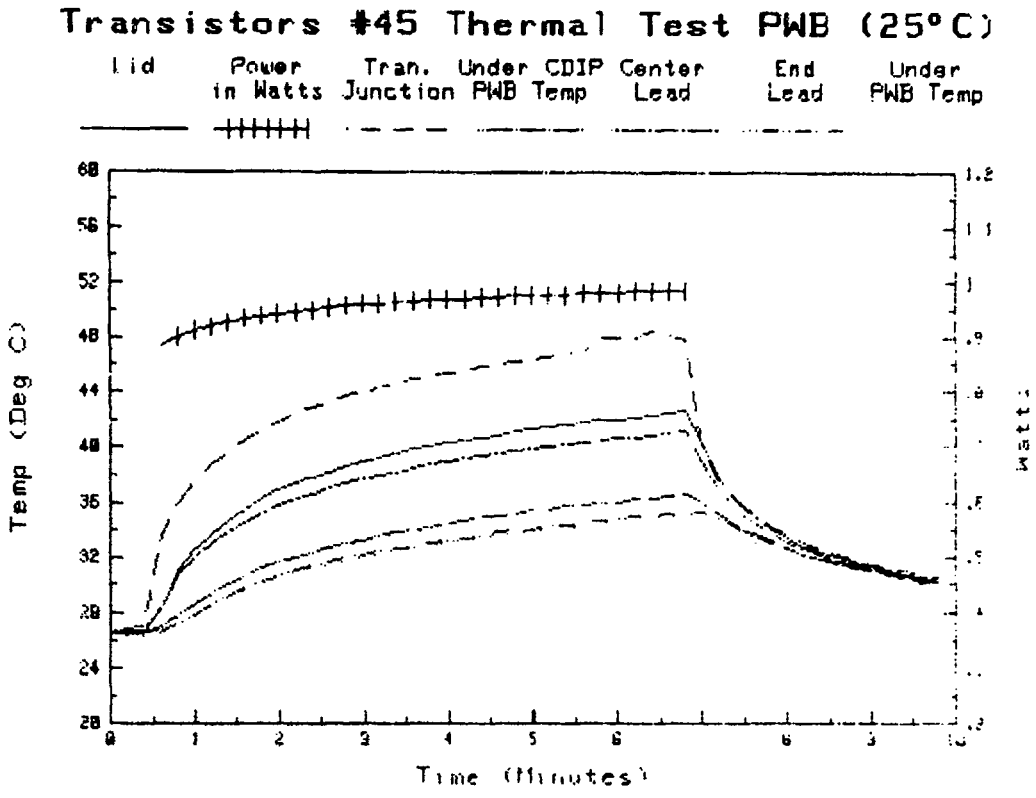
Printed Wiring Board
Ambient Air = 25°C
Power Dissipated = 1 watt

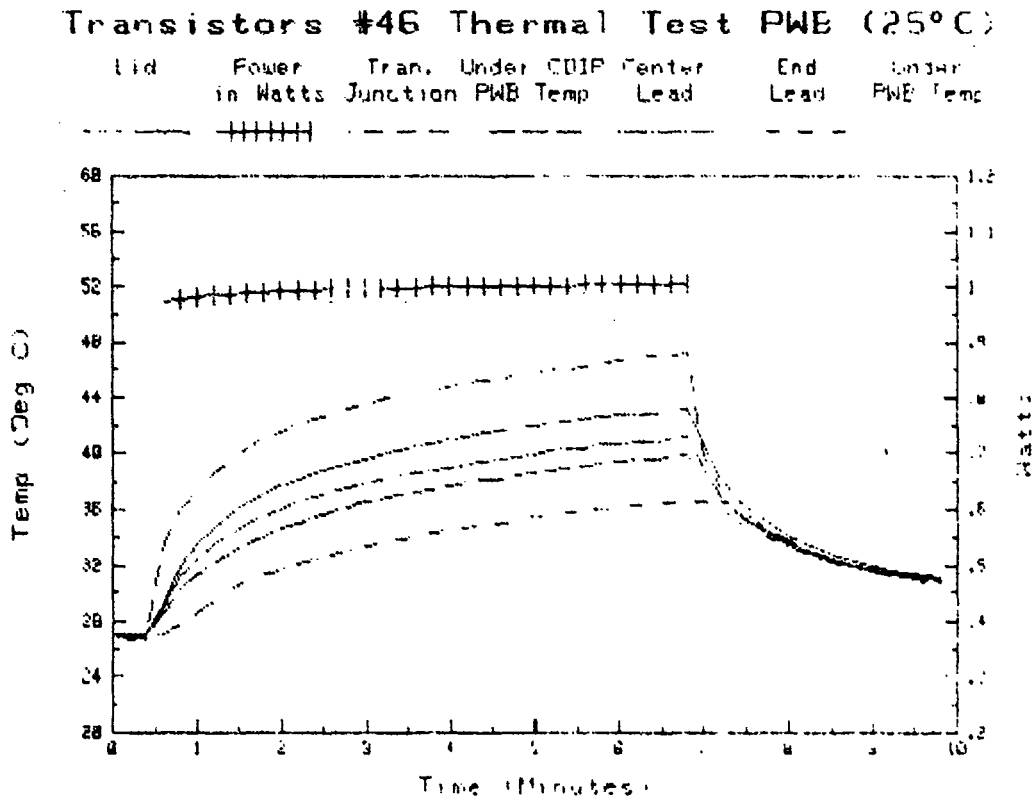


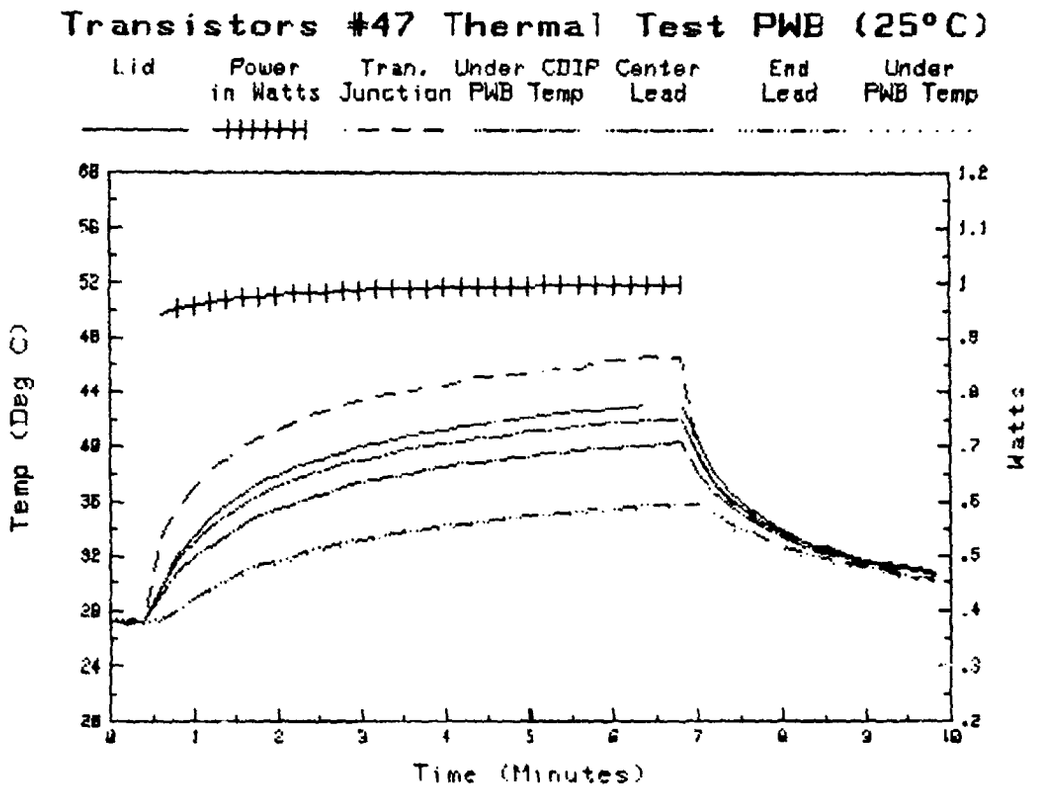












Transistor Thermal Test (PWB 2W 25C)

Thermal Readings (Deg C)

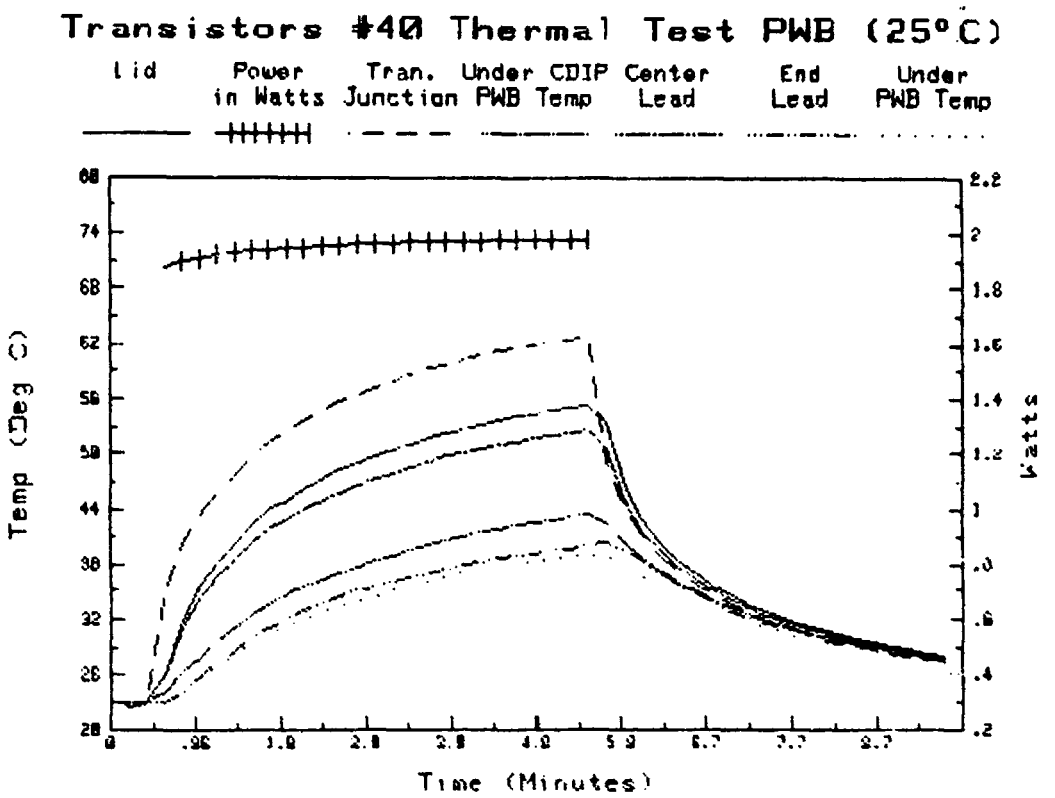
TRANS #	J	L	W	B	P	C	E
40	62.5	55.0	1.98	43.1	38.8	52.3	39.7
41	59.8	52.4	1.98	41.5	38.2	45.6	38.7
43	67.8	56.5	1.99	46.2	39.7	52.7	42.4
44	62.1	54.2	1.98	42.4	39.6	50.8	42.5
45	65.7	54.9	2.08	42.1	39.1	51.7	38.6
46	60.8	52.5	1.93	46.5	38.7	49.0	39.3
47	60.3	52.7	1.96	47.4	38.6	50.6	38.2

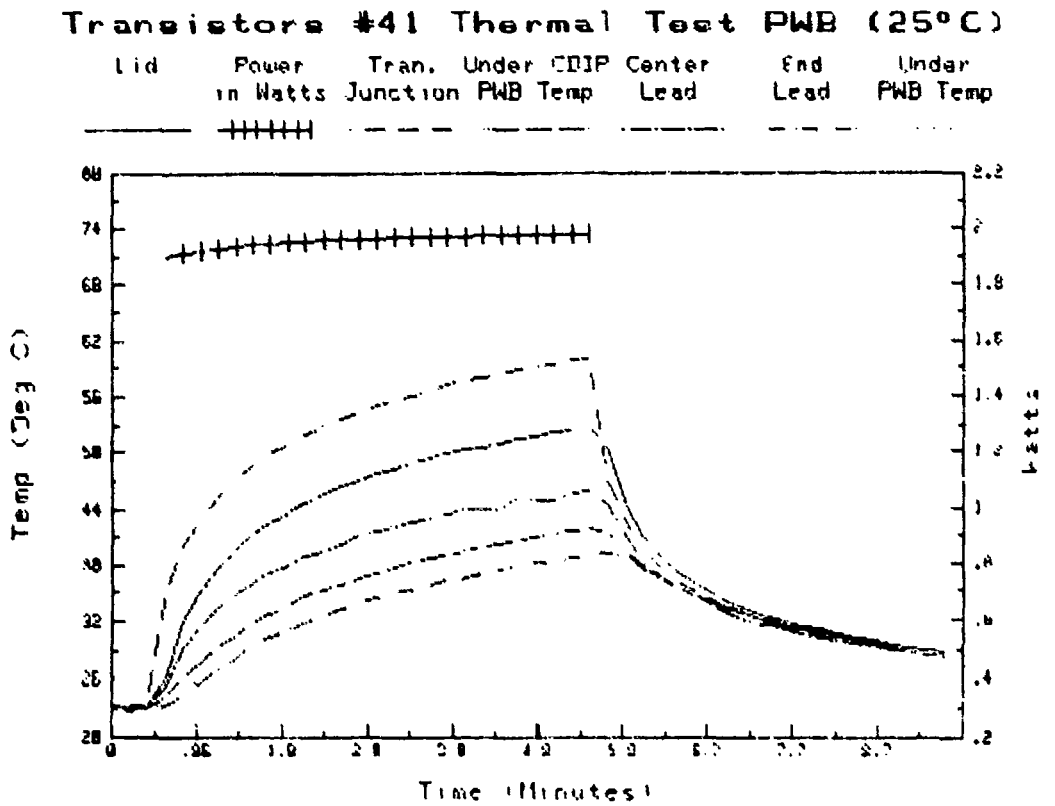
Theta Values (C/W)

TRANS #	J/L	J/B	J/P	J/C	J/E	L/B	L/P	L/C	L/E
40	3.80	9.81	11.99	5.16	11.53	6.01	8.19	1.36	7.73
41	3.71	9.22	10.89	7.15	10.63	5.51	7.17	3.43	6.92
43	5.70	10.89	14.16	7.61	12.80	5.19	8.46	1.91	7.10
44	4.00	9.97	11.39	5.72	9.92	5.97	7.39	1.72	5.92
45	5.18	11.34	12.79	6.72	13.03	6.16	7.61	1.54	7.85
46	4.30	7.40	11.43	6.11	11.12	3.10	7.14	1.81	6.83
47	3.85	6.55	11.03	4.92	11.23	2.70	7.18	1.07	7.38

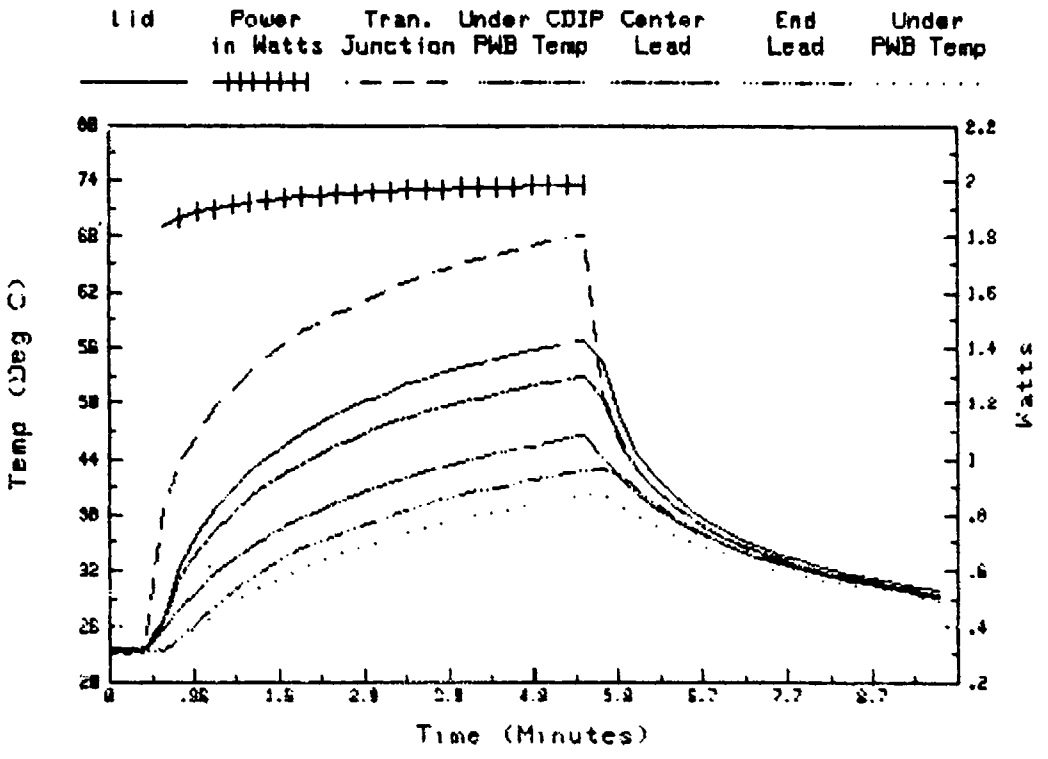
J=Transistor's Junction
L=Package's Lid
B=Under CDIP (PWB Temp)
P=Other Side of PWB from B
C=Package's Center Lead
E=Package's End Lead

Printed Wiring Board
Ambient Air = 25°C
Power Dissipated = 2 watts

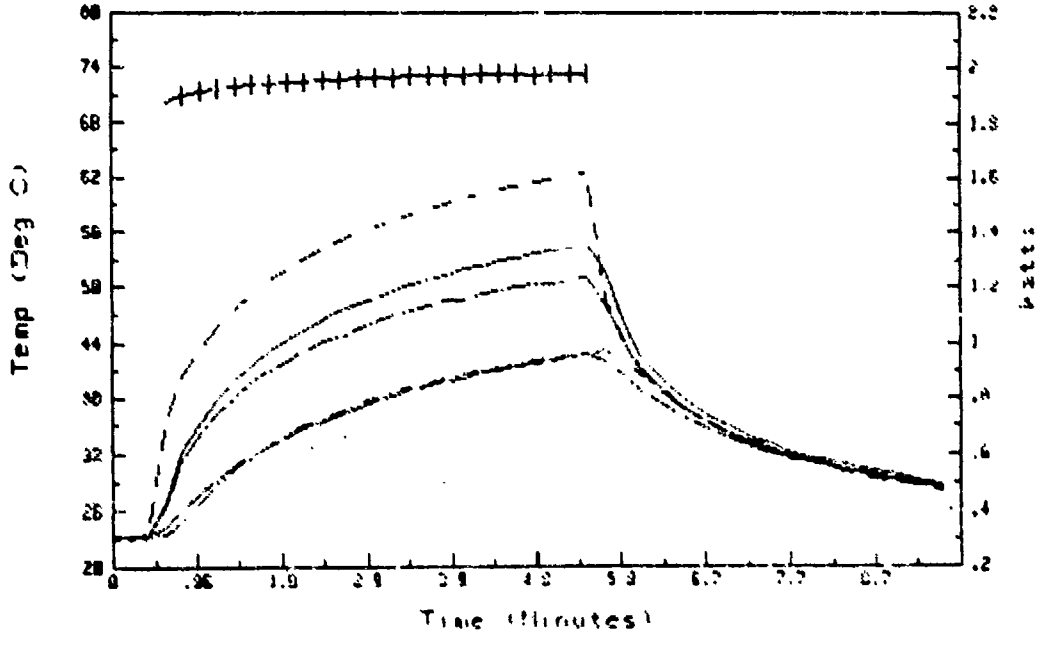




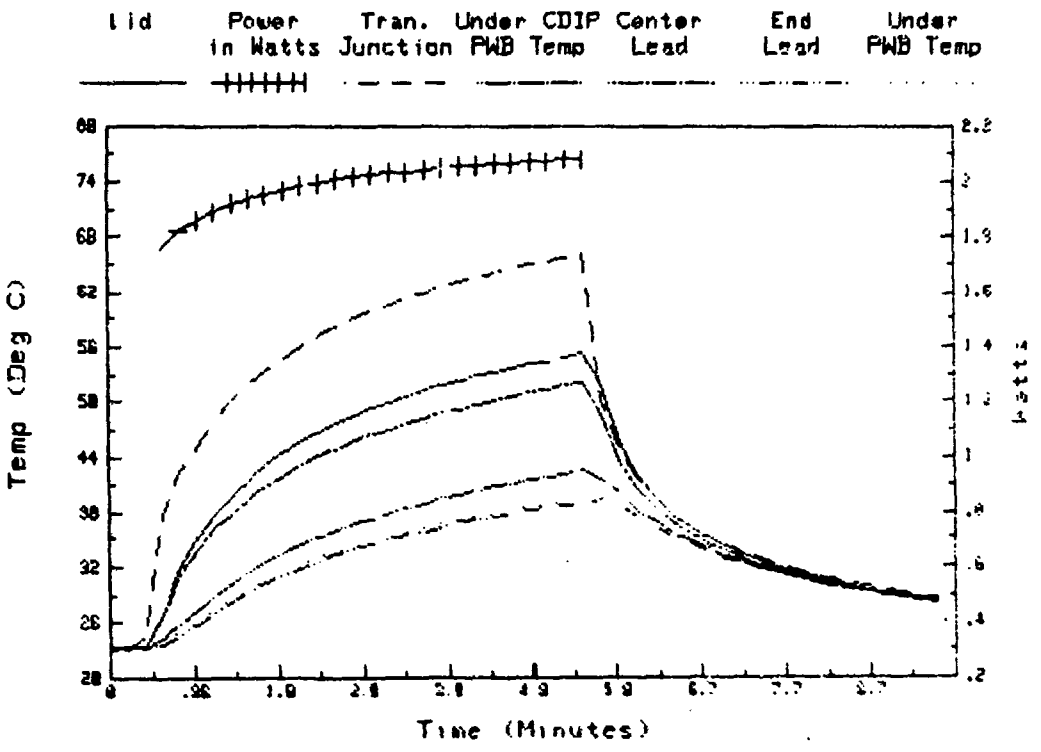
Transistors #43 Thermal Test PWB (25°C)



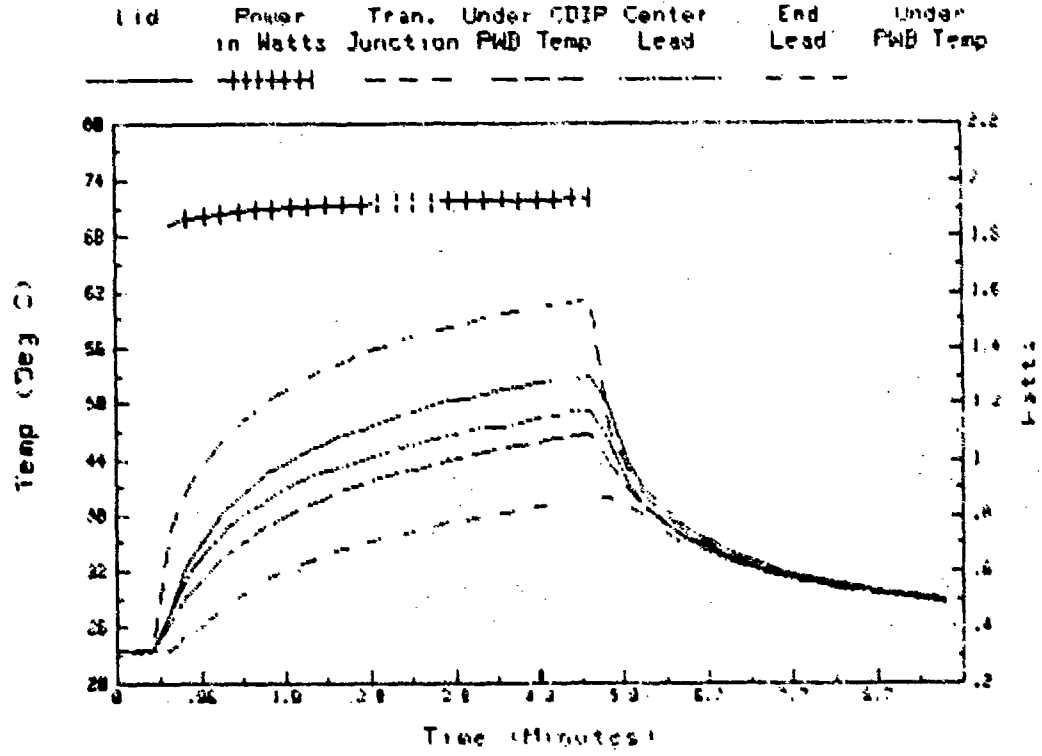
Transistors #44 Thermal Test PWB (25°C)

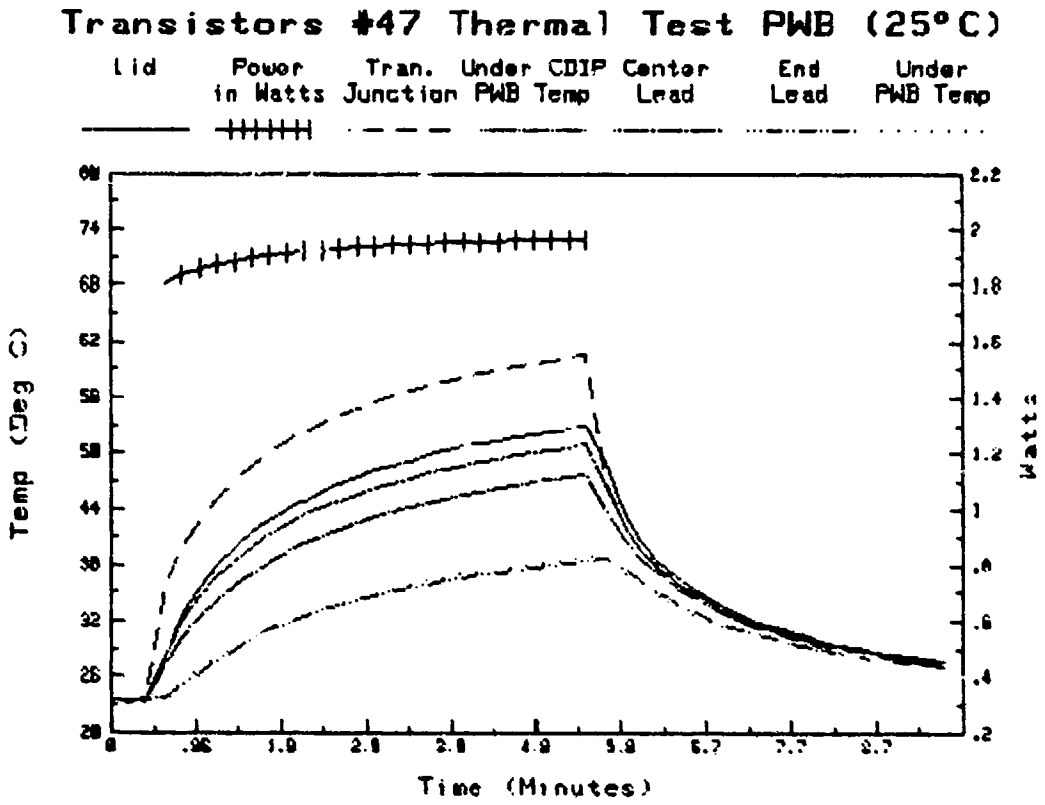


Transistors #45 Thermal Test PWB (25°C)



Transistors #46 Thermal Test PWB (25°C)





Transistor Thermal Test (PWB 2W 55C)

Thermal Readings (Deg. C)

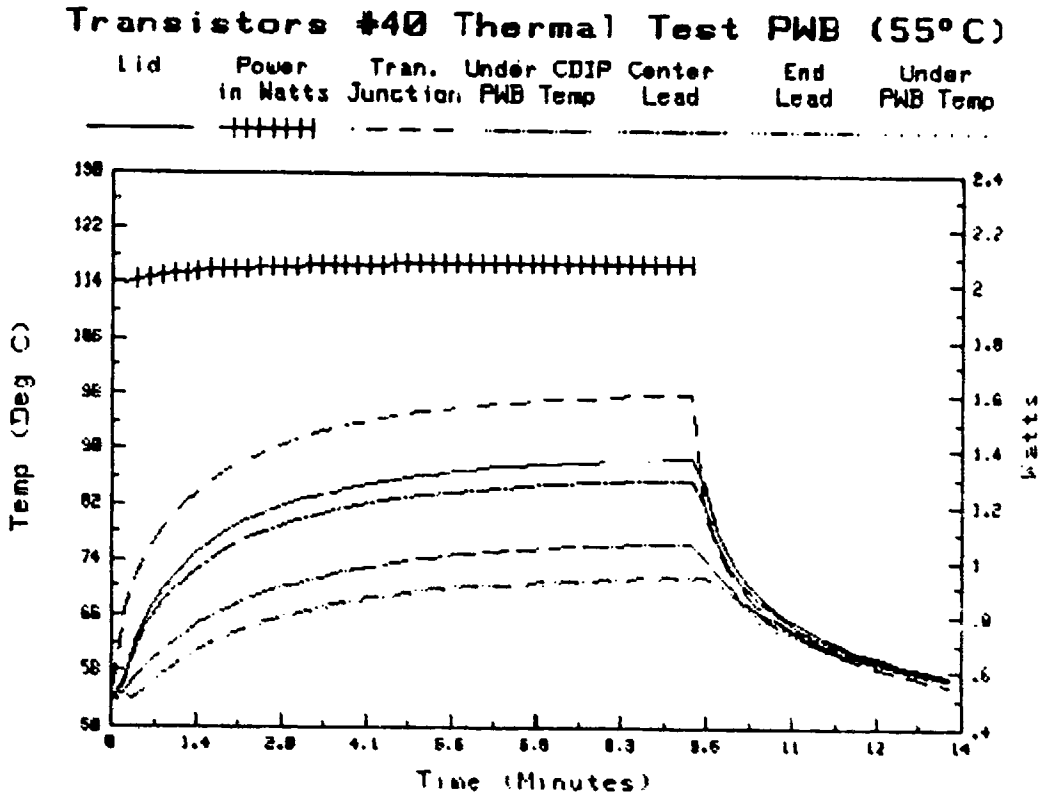
TRANS #	J	L	W	B	P	C	E
40	98.0	88.7	2.08	76.6	71.4	85.6	71.7
41	95.1	86.0	2.07	74.8	70.9	78.1	70.8
43	104.7	90.3	2.10	80.2	72.5	86.1	74.4
44	96.6	86.6	2.07	74.3	70.8	82.6	72.7
45	103.3	89.6	2.30	75.7	71.9	85.9	71.0
46	95.7	85.7	2.03	79.9	71.0	81.1	70.7
47	94.9	85.0	2.10	79.9	69.5	82.7	68.5

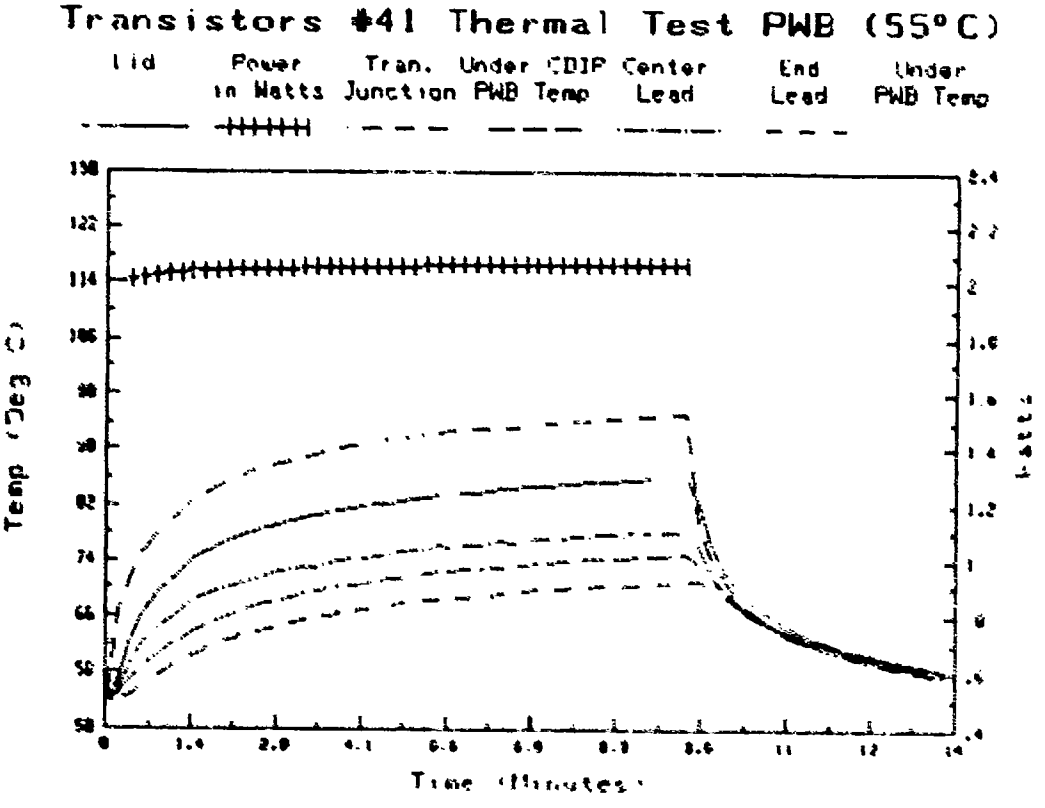
Theta Values (C/W)

TRANS #	J/L	J/B	J/P	J/C	J/E	L/B	L/P	L/C	L/E
40	4.48	10.31	12.81	5.97	12.67	5.83	8.33	1.49	8.19
41	4.38	9.79	11.68	8.20	11.73	5.41	7.30	3.82	7.35
43	6.85	11.65	15.31	8.85	14.41	4.80	8.47	2.00	7.56
44	4.82	10.76	12.45	6.75	11.53	5.94	7.63	1.93	6.71
45	5.95	11.99	13.65	7.56	14.04	6.04	7.70	1.61	8.09
46	4.95	7.81	12.20	7.22	12.35	2.86	7.25	2.27	7.40
47	4 70	7.12	12.06	5.79	12.54	2.42	7.37	1.09	7.84

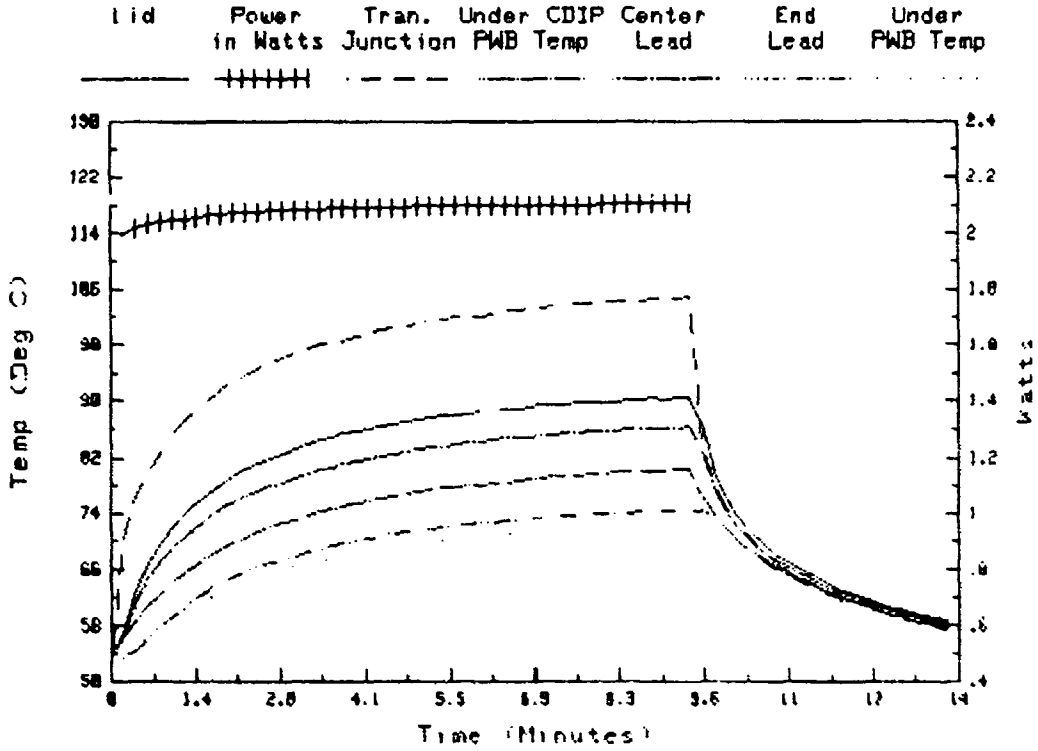
J=Transistor's Junction
L=Package's Lid
B=Under CDIP (PWB Temp)
P=Other Side of PWB from B
C=Package's Center Lead
E=Package's End Lead

Printed Wiring Board
Ambient Air = 55°C
Power Dissipated = 2 watts

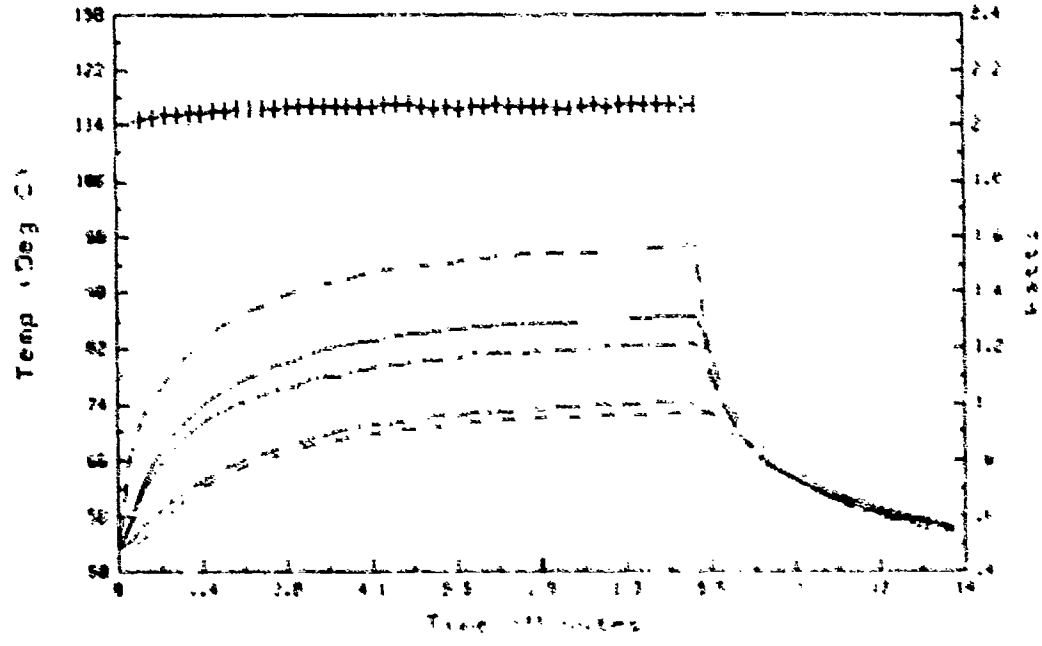


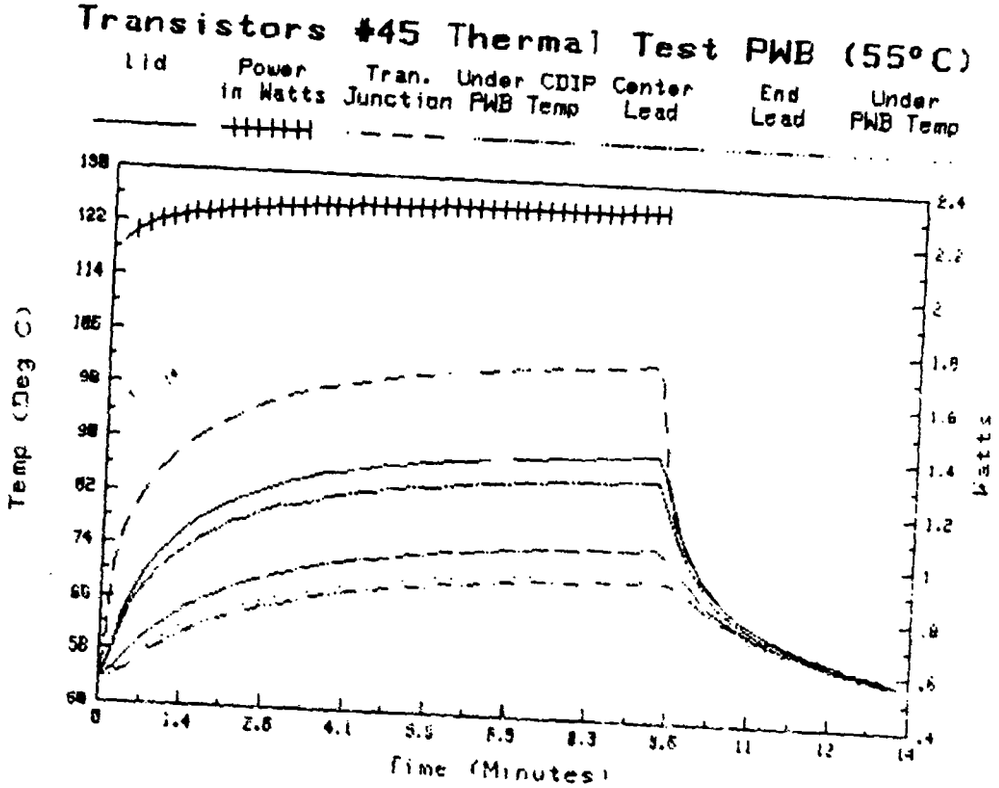


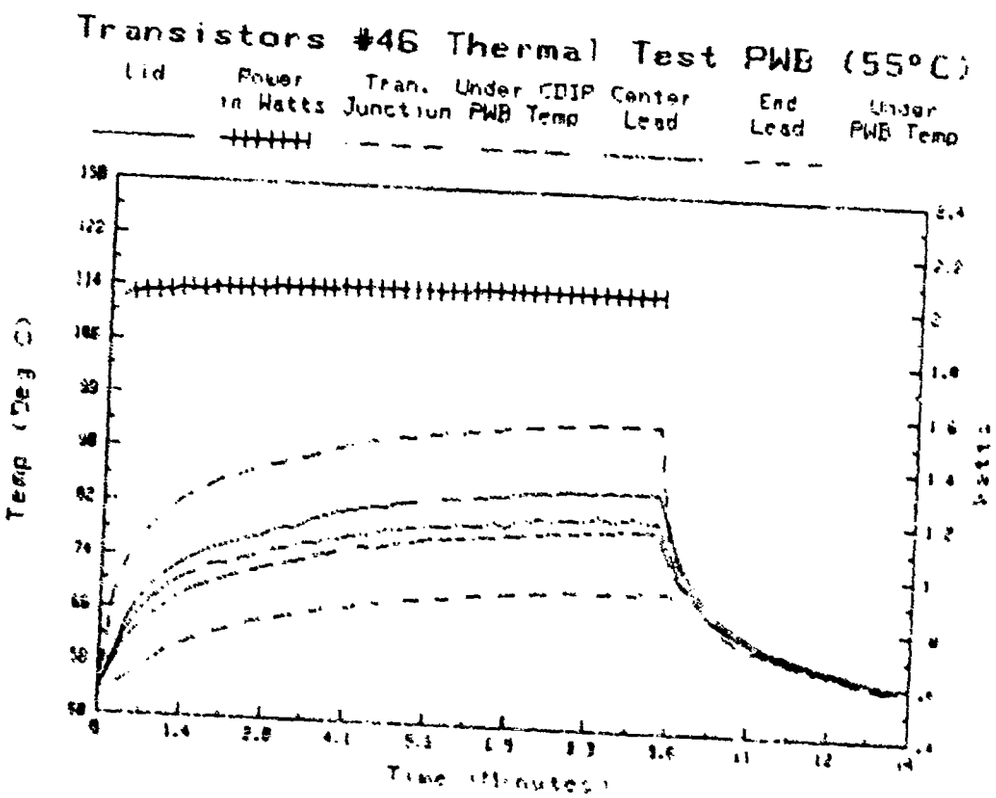
Transistors #43 Thermal Test PWB (55°C)

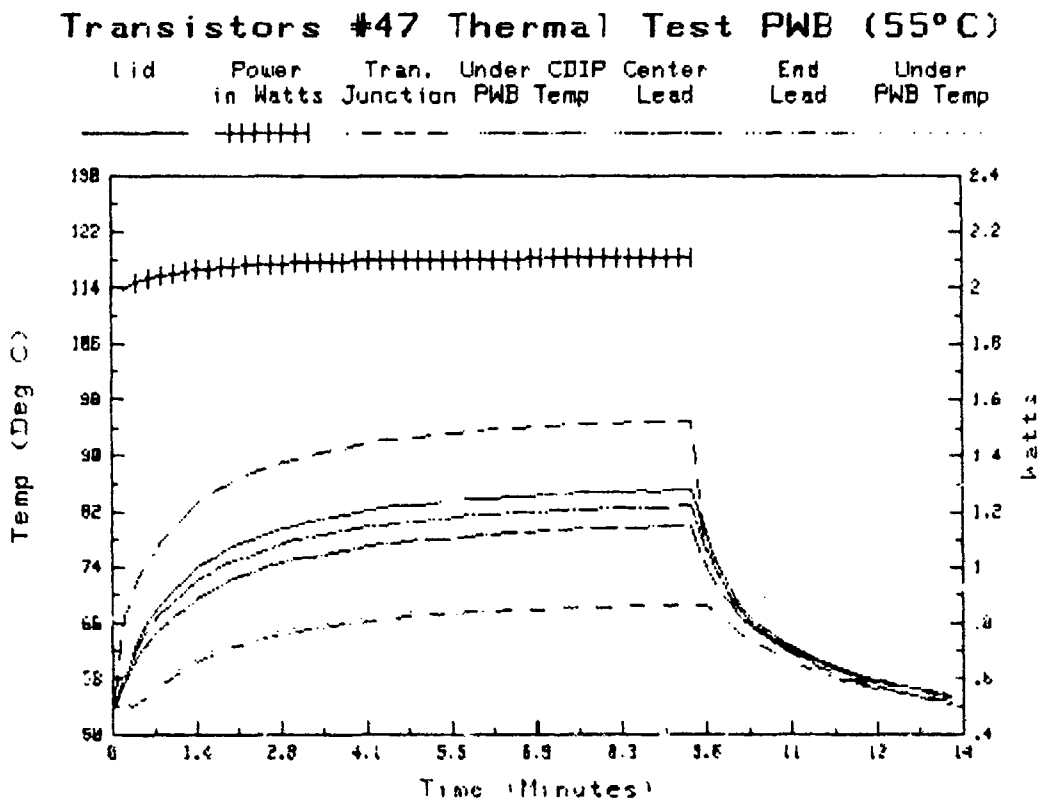


Transistors #44 Thermal Test PWB (55°C)









Transistor Thermal Test (PWB 2W 85C)

Thermal Readings (Deg. C)

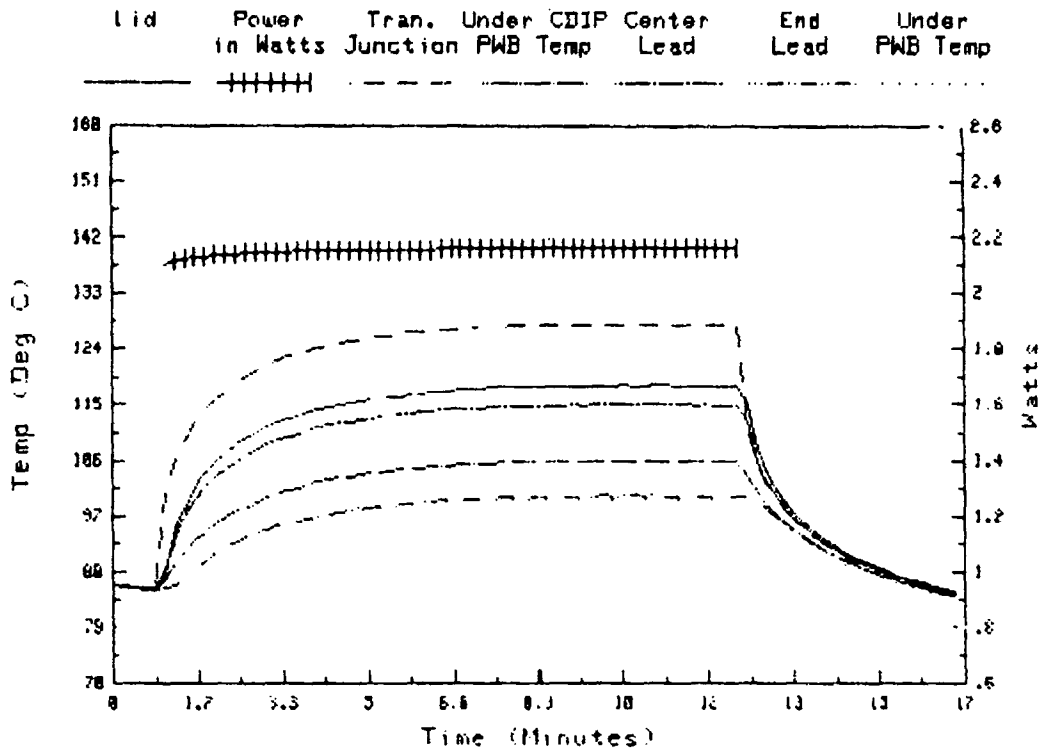
TRANS #	J	L	W	B	P	C	E
40	127.9	118.0	2.16	105.8	99.8	114.9	100.2
41	127.1	116.6	2.14	105.5	101.0	109.7	100.8
43	137.2	121.2	2.19	111.4	102.9	116.8	104.0
44	129.8	118.4	2.14	106.1	102.3	115.2	104.4
45	132.8	118.5	2.40	104.3	100.1	114.8	98.3
46	127.0	115.6	2.10	110.2	100.6	111.9	100.2
47	125.7	114.0	2.20	97.5	98.5	111.7	96.0

Theta Values (C/W)

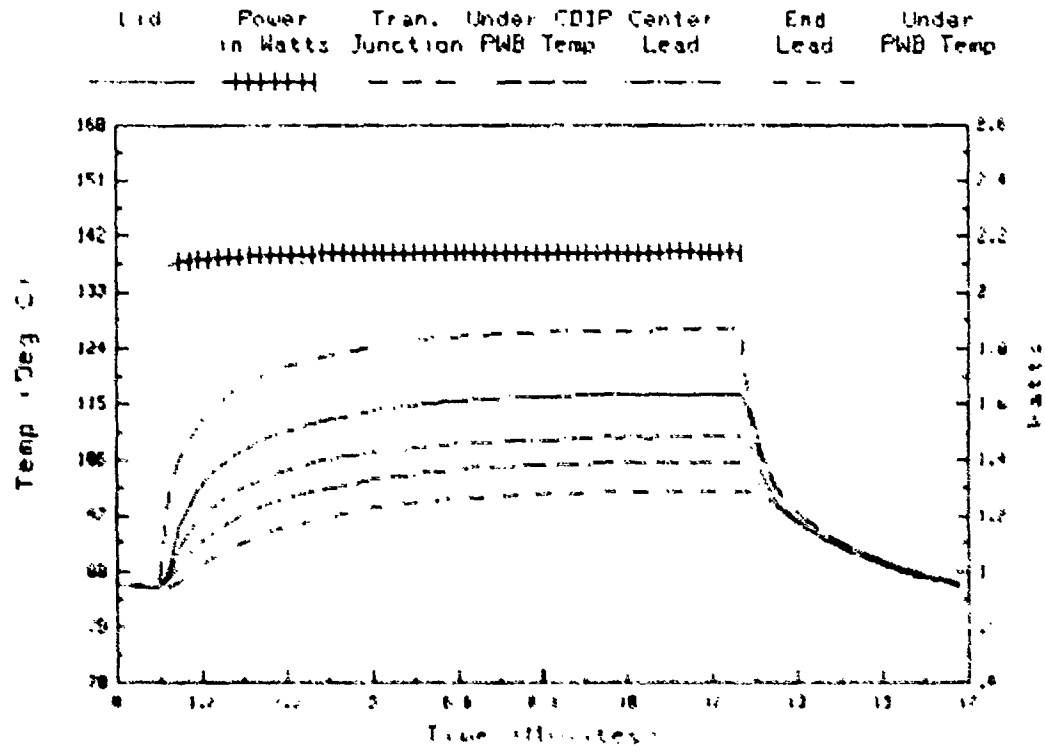
TRANS #	J/L	J/B	J/P	J/C	J/E	L/B	L/P	L/C	L/E
40	4.57	10.22	12.99	6.01	12.81	5.64	8.42	1.43	8.24
41	4.89	10.07	12.17	8.11	12.26	5.18	7.28	3.22	7.37
43	7.31	11.78	15.67	9.32	15.16	4.48	8.36	2.01	7.86
44	5.33	11.07	12.85	6.83	11.87	5.74	7.51	1.49	6.53
45	5.96	11.87	13.62	7.50	14.37	5.92	7.67	1.54	8.42
46	5.44	8.01	12.57	7.20	12.76	2.57	7.13	1.76	7.32
47	5.30	12.80	12.35	6.35	13.49	7.50	7.05	1.05	8.18

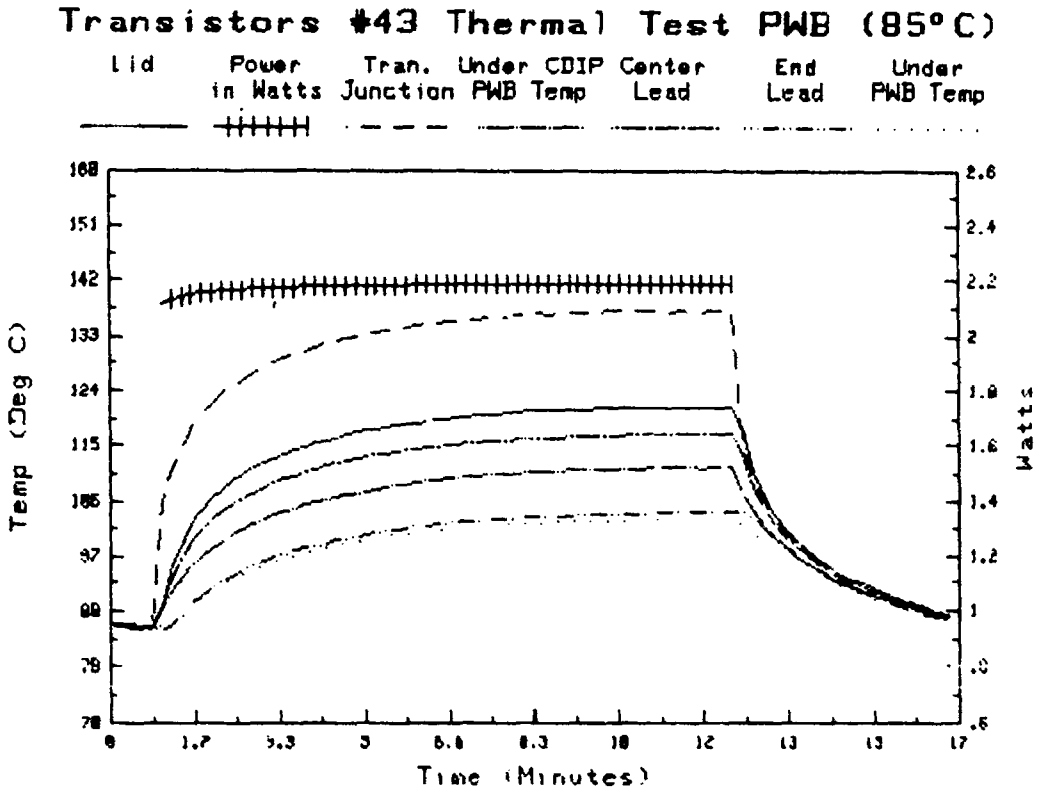
J=Transistor's Junction
L=Package's Lid
B=Under CDIP (PWB Temp)
P=Other Side of PWB from B
C=Package's Center Lead
E=Package's End Lead

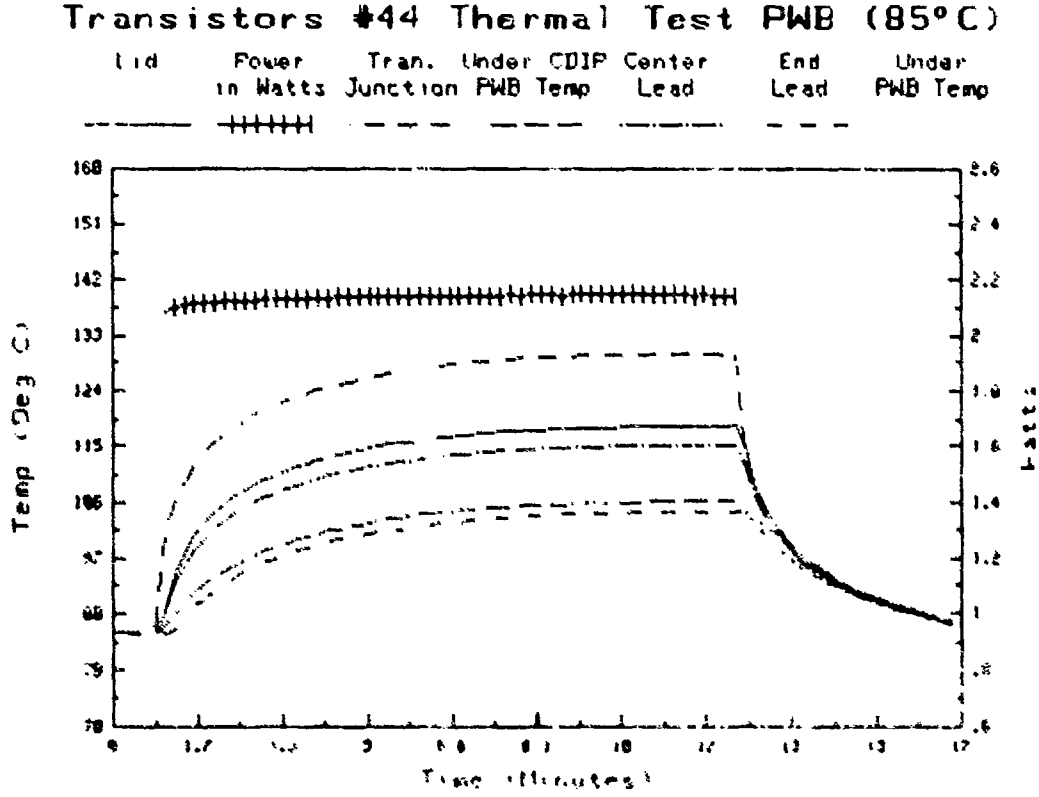
Transistors #40 Thermal Test PWB (85°C)

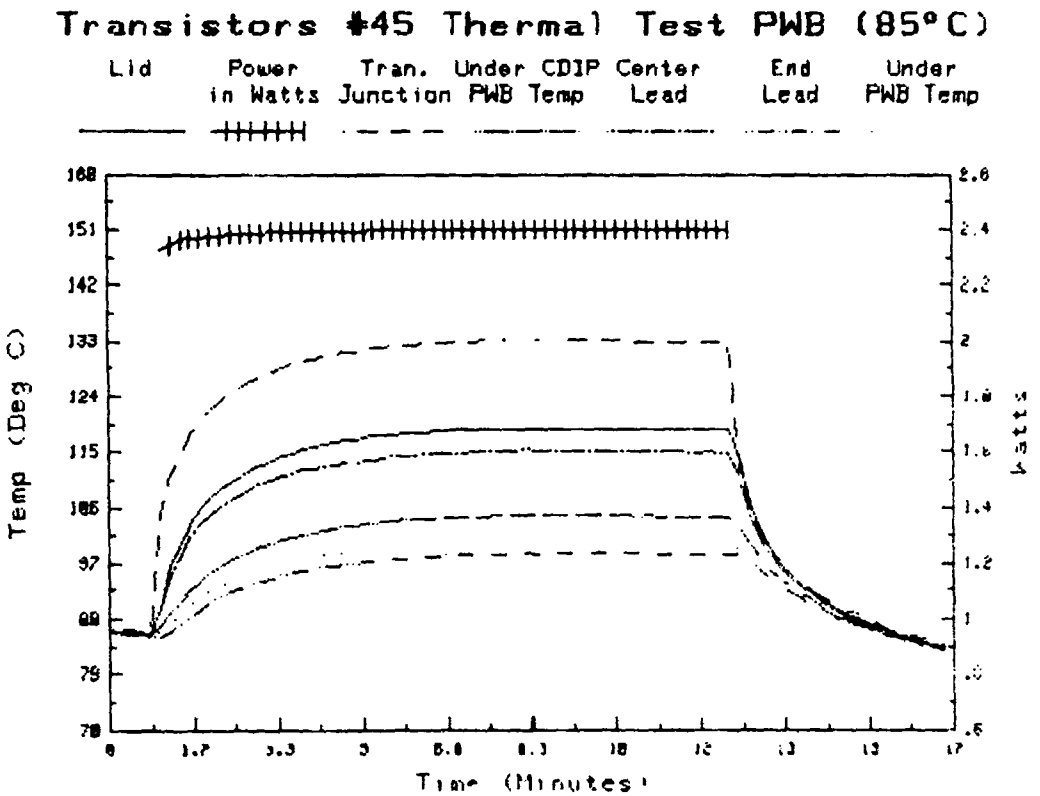


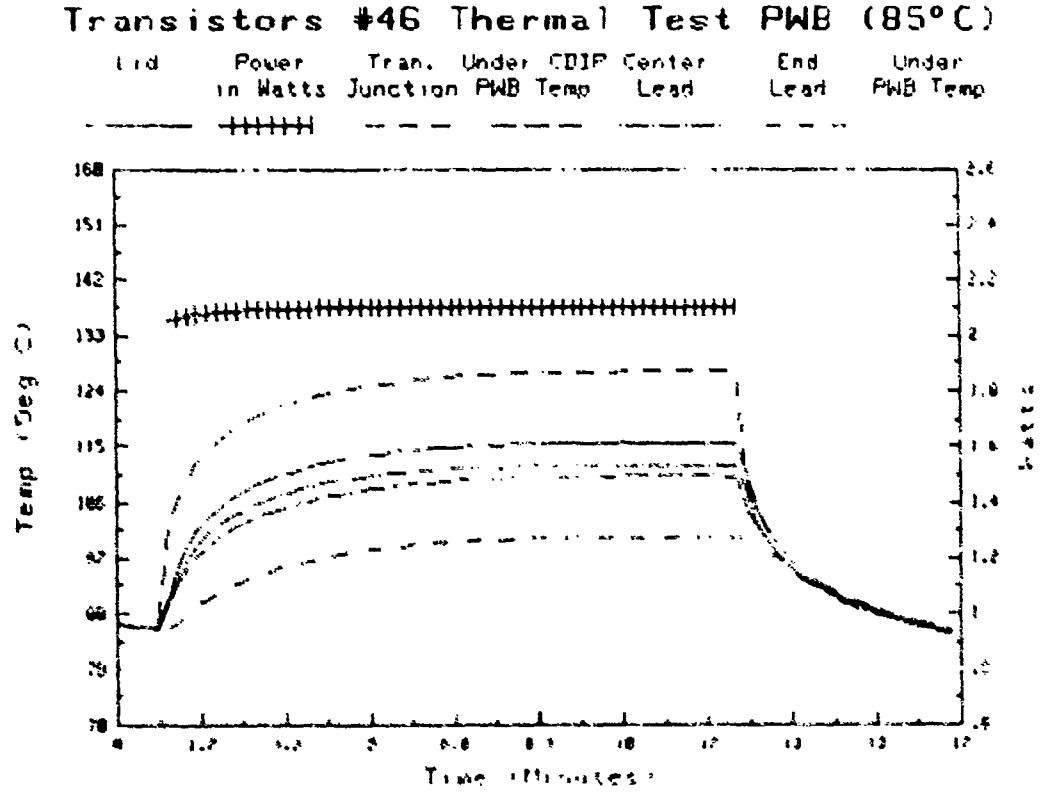
Transistors #41 Thermal Test PWB (85°C)

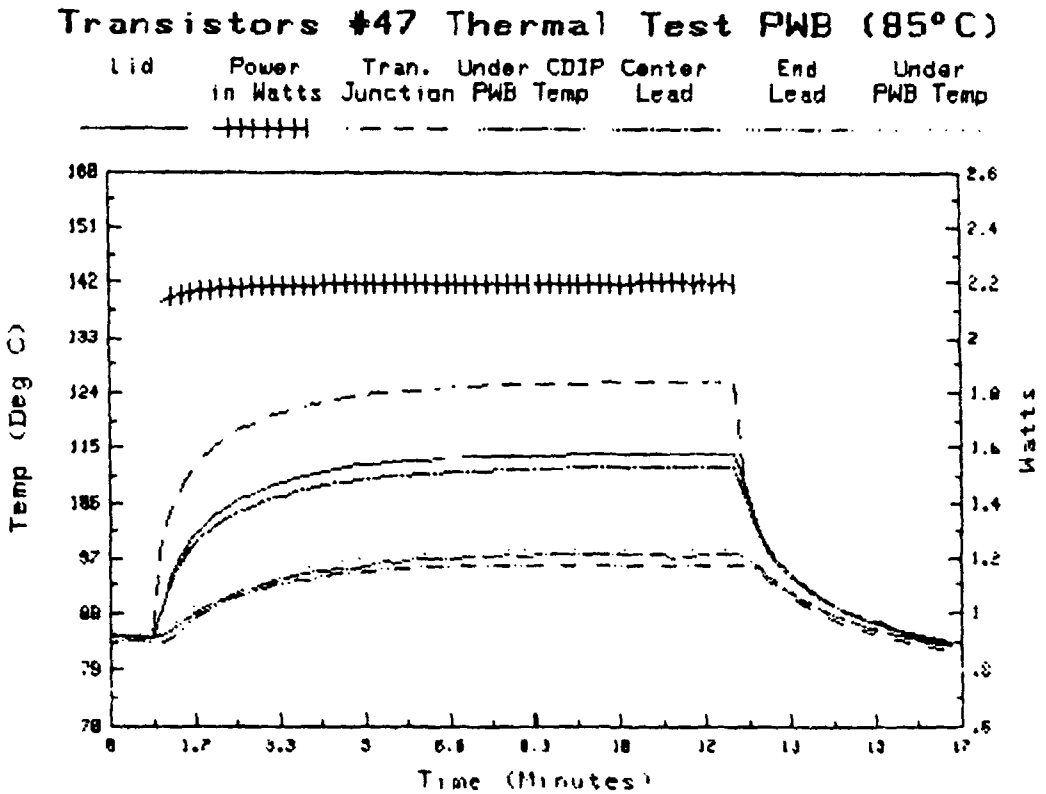












Transistor Thermal Test (PWB 5W 25C)

Thermal Readings (Deg. C)

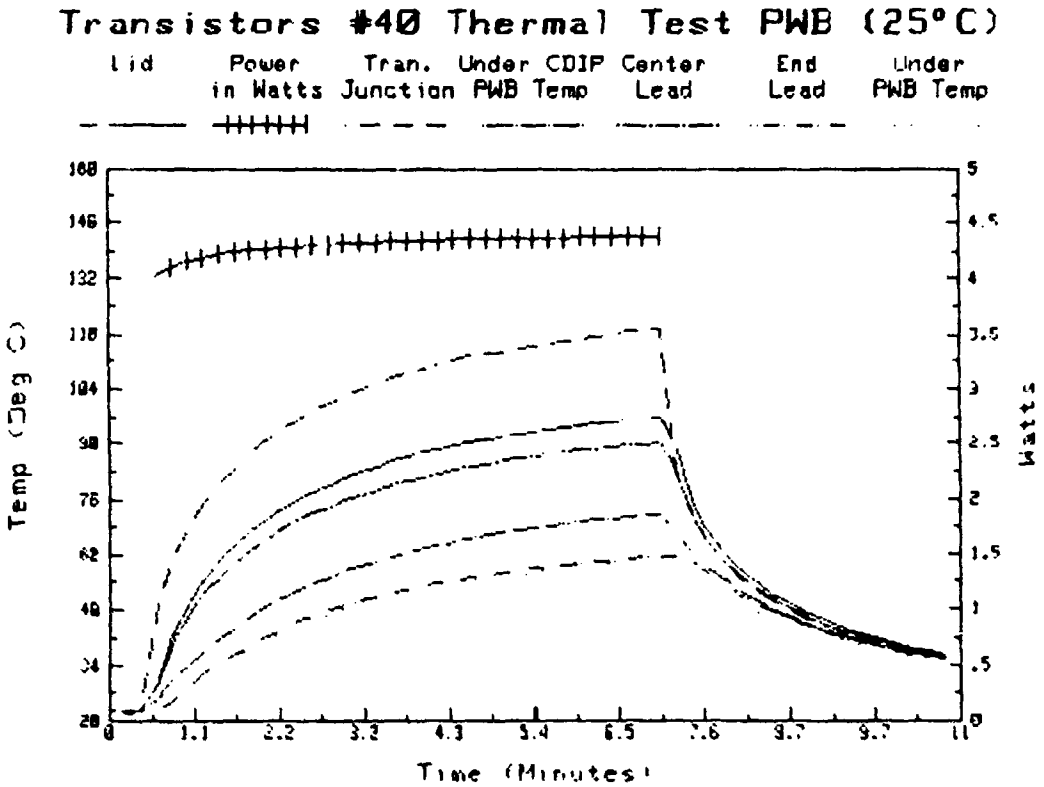
TRANS #	J	L	W	B	P	C	E
40	119.0	96.3	4.38	71.8	60.4	89.8	61.1
41	110.0	89.1	4.31	66.6	58.6	72.3	58.4
43	134.1	100.6	4.45	80.5	63.8	91.2	67.1
44	117.4	93.9	4.34	69.2	62.0	84.5	65.8
45	129.2	99.6	4.87	71.2	62.8	91.4	60.6
46	113.7	91.0	4.24	79.5	60.8	81.5	61.3
47	116.2	92.7	4.44	82.9	61.0	87.6	59.1

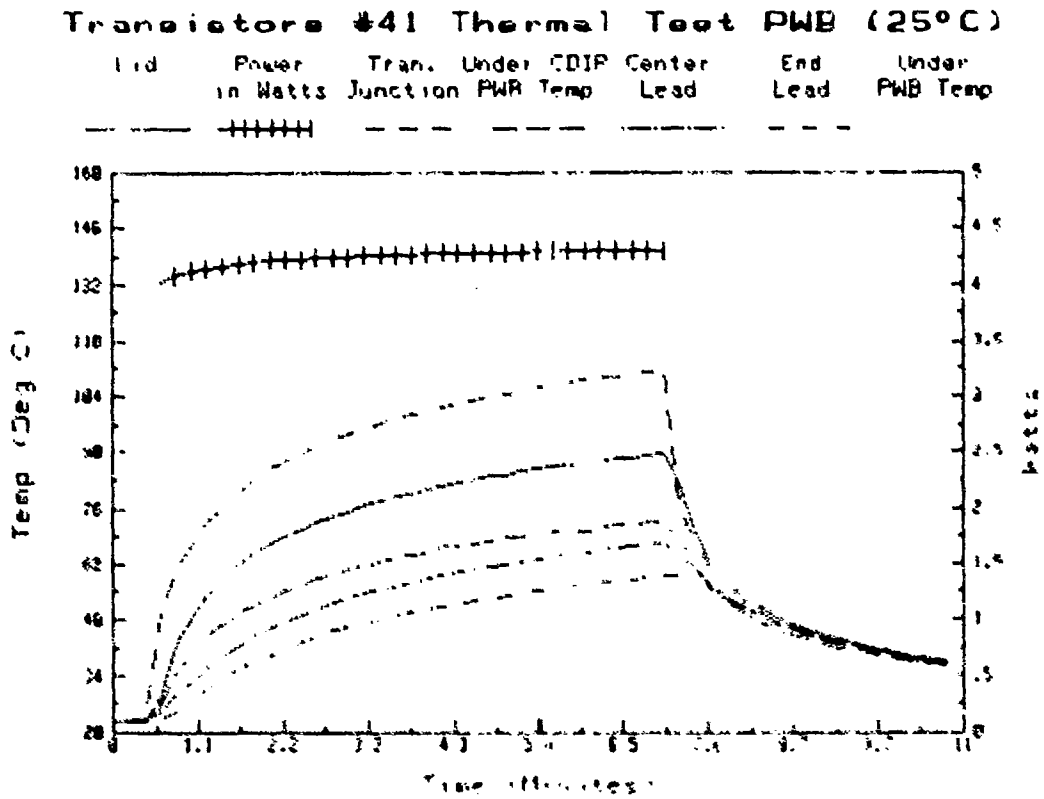
Theta Values (C/W)

TRANS #	J/L	J/B	J/P	J/C	J/E	L/B	L/P	L/C	L/E
40	5.17	10.76	13.36	6.66	13.20	5.59	8.19	1.48	8.03
41	4.84	10.06	11.92	8.74	11.96	5.22	7.08	3.90	7.12
43	7.52	12.04	15.79	9.64	15.05	4.51	8.27	2.11	7.52
44	5.42	11.10	12.76	7.58	11.89	5.69	7.35	2.16	6.47
45	6.08	11.91	13.63	7.76	14.08	5.83	7.55	1.68	8.01
46	5.35	8.06	12.47	7.59	12.35	2.71	7.12	2.24	7.00
47	5.29	7.50	12.43	6.44	12.86	2.21	7.14	1.15	7.57

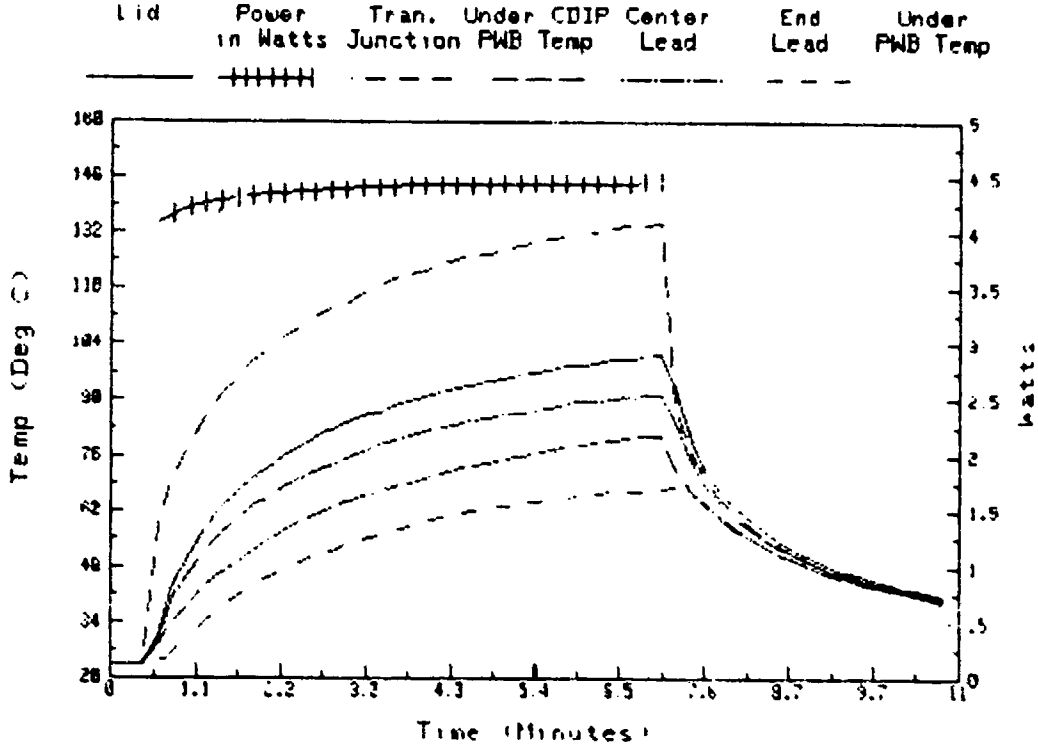
J=Transistor's Junction
L=Package's Lid
B=Under CDIP (PWB Temp)
P=Other Side of PWB from B
C=Package's Center Lead
E=Package's End Lead

Printed Wiring Board
Ambient Air = 25°C
Power Dissipated = 5 watts

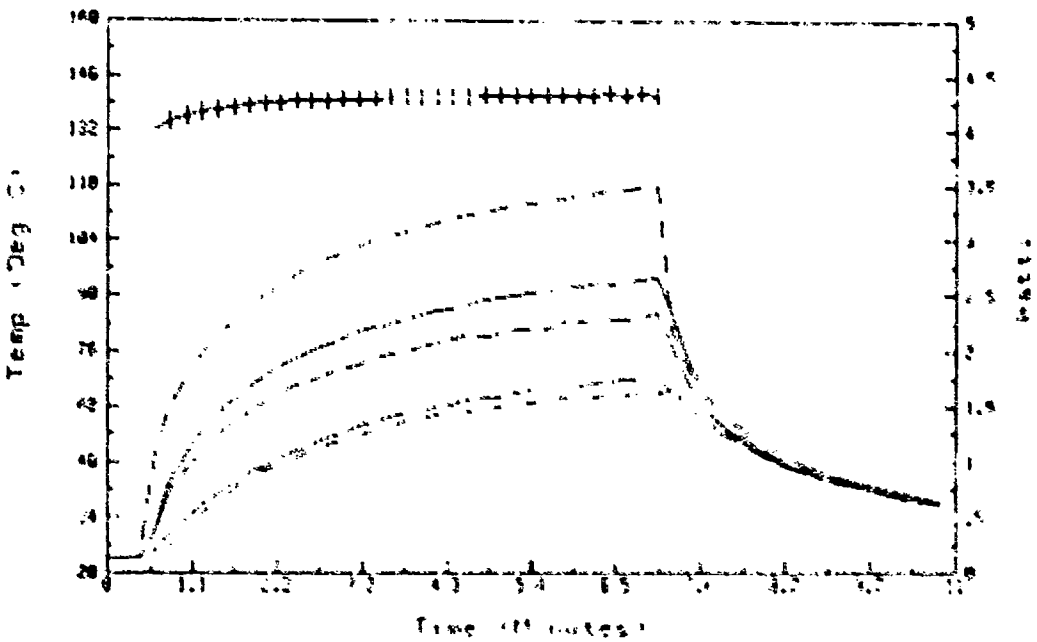




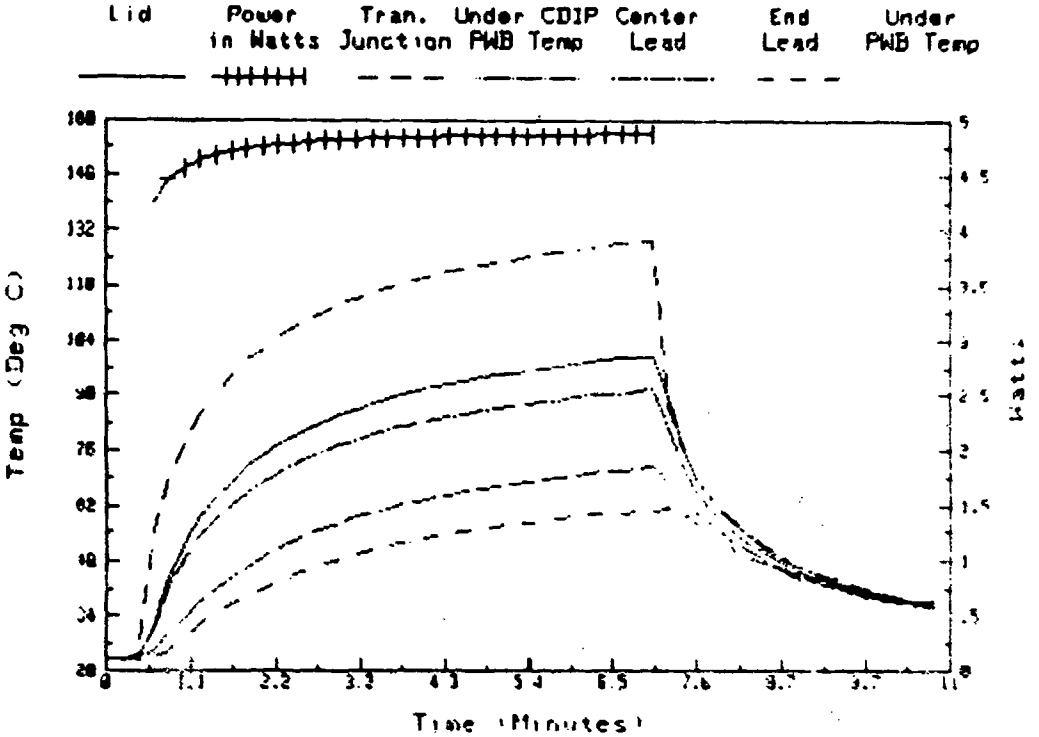
Transistors #43 Thermal Test PWB (25°C)



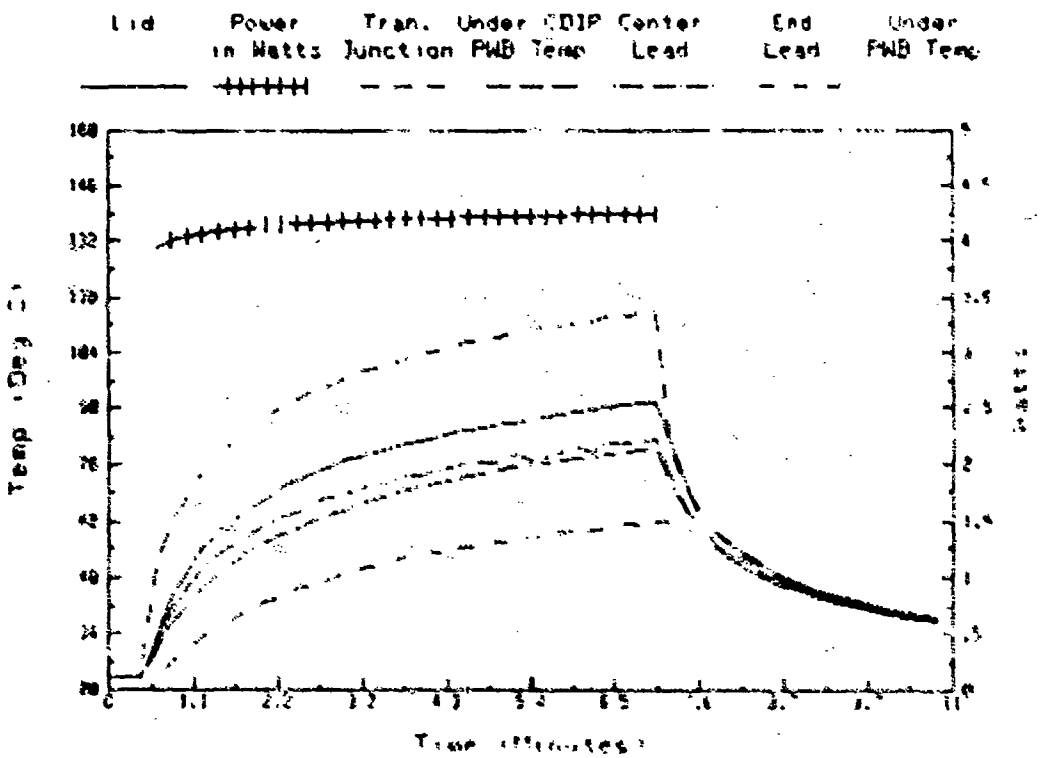
Transistors #44 Thermal Test PWB (25°C)

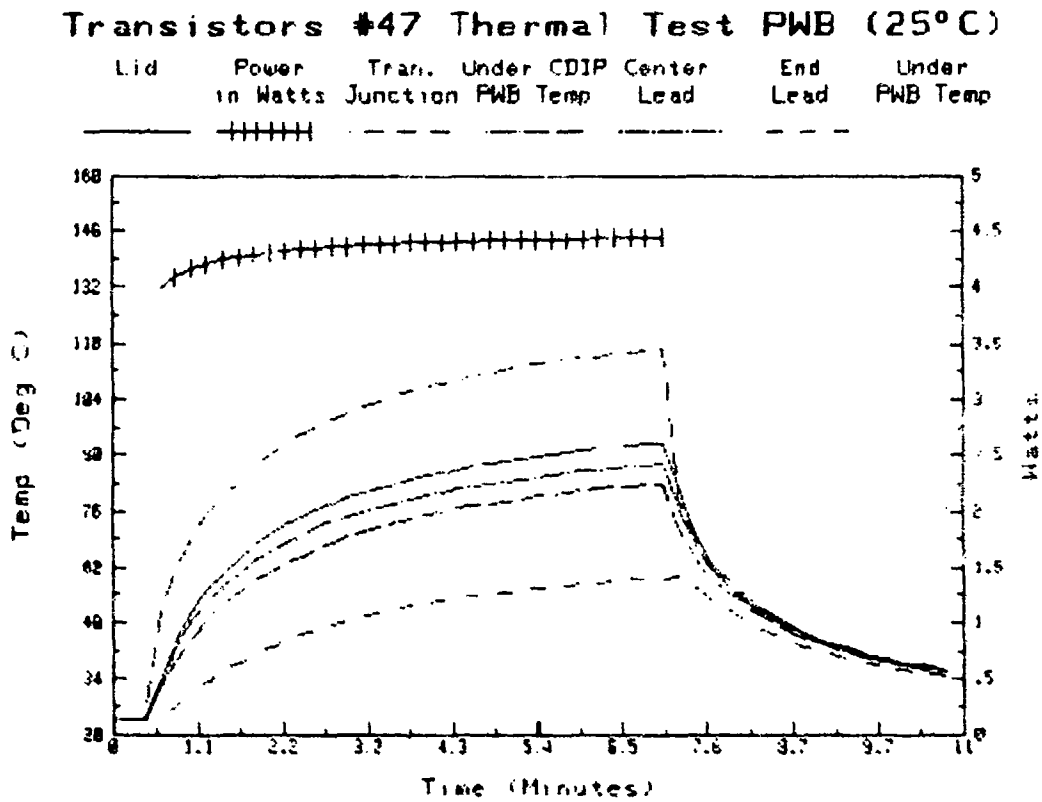


Transistors #45 Thermal Test PWB (25°C)



Transistors #46 Thermal Test PWB (25°C)





APPENDIX 7.2

Hermetic Chip Carrier Thermal Test

Test Module Description:

Four multilayer polyimide fiberglass printed wiring board assemblies were fabricated and assembled. Each circuit board contained four metallization layers as illustrated in Figure 2.0. The following HCC components were installed on each circuit board assembly; 5-64 terminal, 2-48 terminal, 2-40 terminal, 3-32 terminal and 10-24 terminal size devices. All carriers, with the exception of nine 24 terminal carriers contained power transistors. To accommodate the various size HCC chip cavities two different dies were used, a 2NC5337 transistor and a 2N6274 transistor were eutectically mounted to the HCC cavities. Figure 4 illustrates the component and thermocouple locations for each printed wiring board.

The printed wiring board assemblies were bonded to two different support plate materials. One each A and B circuit board assemblies were bonded to an .090 thick aluminum support plate using RTV-88 silicon adhesive (.010 max thickness). The remaining A&B boards were hard bonded to a .030 thick Cu clad Invar support plate using ablefilm 506 (.006 thickness). The Cu clad thickness on each side of the invar was .0048 inch or 16% of the total thickness.

4.2 Thermal Resistance & Temperature Measurement Procedures:

NPN power chip transistors were installed in each carrier to simulate actual device die and provide a mens for directly measuring the junction temperature. In addition to the transistors, small diameter (3-mil) Chromel - Constantan thermocouples were added to measure the base temperature, solder joint temperature and lid temperature for various HCC's as shown in Figure 4.

4.2.1 Power Dissipation Measurements

The power dissipated was determined by measuring the voltage drop across the emitter-collector (V_{EC}) of the transistor and multiplying the voltage by the current (I_C).

$$P = V_{EC} \times I_C$$

where:

P = power dissipation of device, in watts
V_{EC} = voltae drop across emitter - collector, in volts
I_C = collector current, current in amps

The power dissipated by the transistor (0 to 2 watts max.) was adjusted by a change in the base voltage and current resulting from varying the resistance.

Junction Temperature Measurements

All power transistors were calibrated to determine the individual forward bias of the base-emitter voltage versus temperature characteristics. The relationship of the voltage drop across the emitter-base and temperature is linear over the test temperature range. Therefore, the transistor's forward voltage drop can be expressed by the equation $y = Mx + b$, where y equals temperature, x = voltage drop, and M and b are constants. The constants can be found by measuring the voltage drop at known temperatures and fitting the data in the equation by using the least squares method. Using this equation the temperature of the transistor junction can be determined by measuring the forward voltage drop across the emitter base.

Thermal Resistance Calculation

To determine the thermal resistance from the device junction to case, it was necessary to measure the power dissipation, junction temperature, and case temperature. The junction temperature and case temperature were measured using a Fluke 2240C data logger. The voltage drop across the emitter and base of the transistor is then measured. Using the transistor calibration curve relationship, the data logger converts the measured voltage to temperature. Knowing the device junction temperature, case temperature and power dissipation, the thermal resistance ($\theta j\text{-}c$) was calculated using the following relationship:

$$\theta j\text{-}c \qquad \frac{Tj - Tc}{Pwr}$$

where:

$\theta j\text{-}c$ = junction to case thermal resistance (°C/w)
Tj = junction temperature (°C)
Tc = HCC case temperature at the solder joint (°C)
Pwr = device power dissipation (w)

Calibration and Pre-Test Configuration

Both module assemblies were installed in a pair of ATLIS cold wall plates with sufficient air baffles to minimize temperature chamber air current effects on the component temperature measurements. The temperature chamber was initially set at 90°C where the transistors were adjusted such that they were dissipating zero power. The voltage drop across the emitter base was then measured. Several temperature step increases were made in increments of 10°C until 130°C was reached. For each temperature the boards were allowed to stabilize before the voltage drop across the emitter base was recorded. These measurements with the temperature reading were then curve fitted to each transistor using the least squares method. The calibration test was performed on the test modules in these test configurations to minimize errors generated by test set up variations.

Test Configuration Conditions & Power Setting Test Levels

To obtain the test data under typical operating conditions the modules were installed in a chamber set to 80°C. Each transistor was initially set to dissipate 1/4 watt. After chamber stabilization the function and thermocouple measurements were recorded. Power levels were re-adjusted to 1/2, 3/4 and 1 watt. After stabilization, junction and thermocouple readings were again recorded for all power level settings.

Junction to Case Thermal Resistance

The junction to case thermal resistance values obtained from the test results are summarized in Table I for various size HCCs. Case temperature measurements for $\theta j\text{-}c$ were taken from the HCC solder joint locations. Test results indicate that the junction to case thermal resistance remains fairly constant for the various power levels tested. $\theta j\text{-}c$ values for the copper clad invar module compared well with the aluminum supported module.

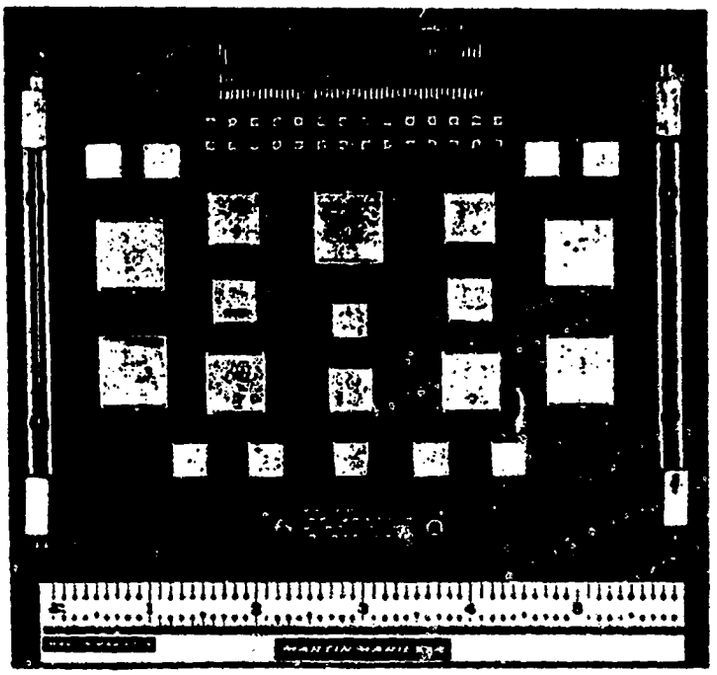


Figure 2. Functional Multilayer Test Module

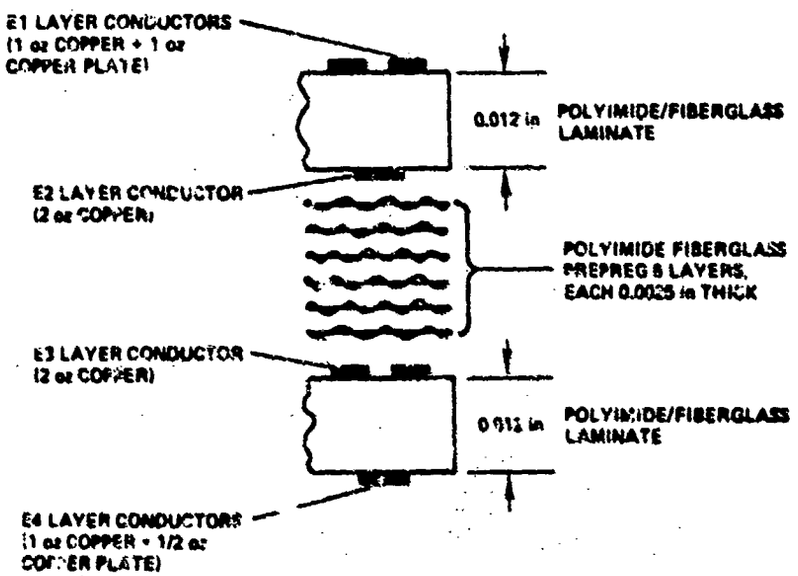
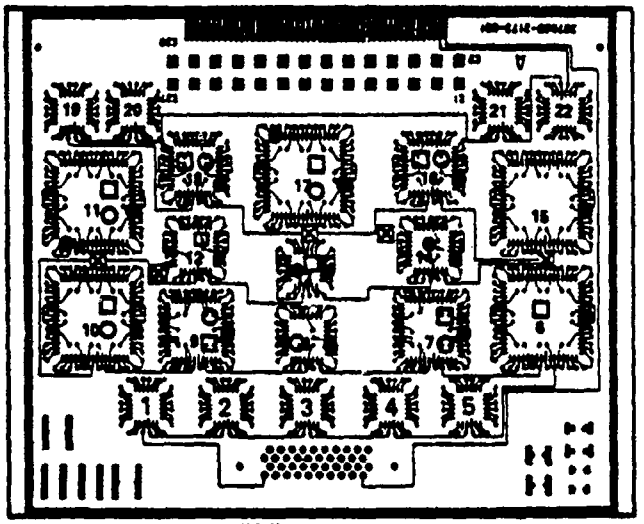
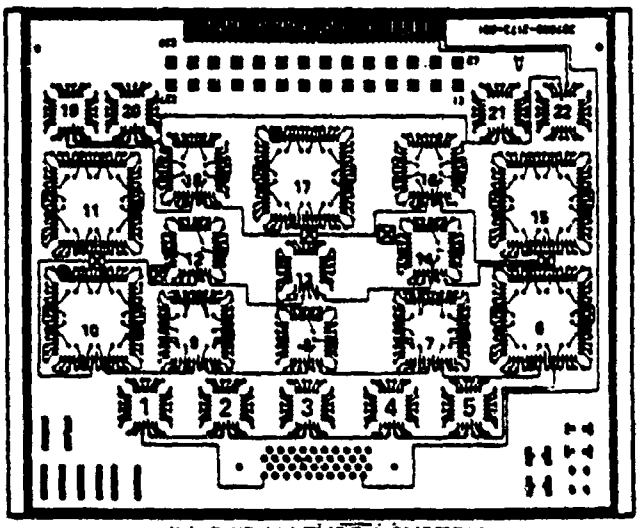


Figure 2. Standard Polyimide PWB Lay-Up



(a) PWB "B" TYPE 3 SYSTEM



(b) PWB 'A' TYPE 1 SYSTEM

LEGEND:

●	THERMOCOUPLE IN SOLDER JOINT	28
□	THERMOCOUPLE MOUNTED UNDER HCC	10
○	THERMOCOUPLE MOUNTED ON LID OF HCC	10
×	THERMOCOUPLE MOUNTED ON METAL PLATE	10

Figure 4. Thermocouple Locations on Test Hardware

TABLE 1

θj-c for 5 HCC Sizes at 4 Pwr Settings

Component Location	HCC Part Size	Al θj-c °C/w 1/4w	1/2w	3/4w	1w	Copper Clad Invar θj-c °C/w 1/4w	1/2w	3/4w	1w	Mean for all data (w)stand dev. M + 3σ
6	64	-	17.26	17.13	16.99	18.51	19.4	19.91	19.92	Mean = 12.37
10	64	11.26	11.56	11.35	11.71	12.55	12.39	12.34	9.04	σ = 3.8
11	64	9.97	9.92	10.23	10.28	11.26	11.51	10.96	11.52	M+3σ = 23.7
15	64	12.87	12.46	12.54	12.42	4.76	5.45	6.12	6.67	
17	64	14.35	12.46	12.79	12.85	-	-	-	-	
7	48	16.49	14.65	14.53	14.51	-	-	-	-	Mean = 14.35
9	48	14.58	13.52	13.36	13.19	-	-	-	-	σ = 1.1
										M+3σ = 17.65
16	40	6.92	8.41	8.61	8.68	8.55	8.91	7.52	11.05	Mean = 9.38
18	40	10.15	10.54	10.59	10.65	8.69	9.58	9.76	9.50	σ = 1.08
										M+3σ = 12.62
8	32	14.32	12.92	13.05	13.88	14.97	14.99	16.79	17.43	Mean = 13.52
12	32	11.82	10.78	10.80	11.16	13.15	12.95	13.99	14.78	σ = 1.80
14	32	12.62	11.45	12.14	12.72	12.82	13.96	15.04	16.00	M+3σ = 18.92
13	24	10.20	10.81	11.53	11.86	-	-	-	-	Mean = 11.1
										σ = .75
										3σ+M = 13.35