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PRINTED WIRING ASSEMBLY AND INTERCONNECTION RELIABILITY

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This report presents reliability prediction models for printed wiring assemblies, solderless wrap assemblies, wrapped and soldered assemblies, and discrete wiring assemblies w/electroless deposited PTH for inclusion in MIL-HDBK-217. Collected field failure rate data were utilized to develop and evaluate the factors. The reliability prediction models are presented in a form compatible with MIL-HDBK-217D, proposed.

This report has been reviewed by the RADC Public Affairs Office (PA) and is releasable to the National Technical Information Service (NTIS). At NTIS it will be releasable to the general public, including foreign nations.

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PREFACE

This final report was prepared by IIT Research Institute, Chicago, Illinois, for the Rome Air Development Center, Griffiss AFB, New York, under Contract F30202-80-C-0078. The RADC technical monitor for this program was Mr. John McCormick (RBRE). This report covers the work performed from February 1980 to August 1981.

The principal investigator for this project was Mr. D.W. Coit with valuable assistance provided by Mr. D.W. Fulton, Mr. J.J. Steinkirchner, Mr. R.G. Arno and Mr. E.R. Bangs. Data collection efforts for this program were coordinated by Mr. I.L. Krulac.

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1. INTRODUCTION

1.1 Purpose. The primary objective of this study was to develop a failure rate prediction methodology which could be employed in the reliability assessment of printed wiring assemblies and alternative types of interconnection assemblies currently used in the electronics industry. Different types of interconnection assemblies considered include double-sided and multilayer printed wiring, solderless wrap, wrapped and soldered, clip termination and discrete wiring with electroless deposited plated through holes.

Previously documented field experience has indicated that the current prediction methodology for printed wiring boards and connections as presented in MIL-HDBK-217C, Reliability Prediction of Electronic Equipment, is inaccurate. The current methodology has also proved insufficient in regard to the full spectrum of available technologies. This study involved the development of an interconnection assembly failure rate prediction models which replace the current printed wiring board and connection prediction models, increases prediction accuracy and expands prediction capabilities to previously unexplored areas.

1.2 Background. Advances in the electronics industry dictate that printed wiring assemblies and alternate types of interconnection assemblies be compatible with highly dense circuit designs. Therefore, the use of multilayer printed wiring boards is becoming more and more desirable. However, there is a relatively lengthy time between design submittal and finished product for multilayer printed wiring boards. This is one of the primary reasons for the emergence of alternate types of interconnection assemblies. The alternate interconnection assemblies, most notably discrete wiring boards can also provide other distinct advantages depending on the users particular needs. The choice of which method of interconnection is most suitable for a particular application must be decided after considering many different factors.

In most applications, any advantages offered by a particular type of interconnection assembly are of little or no consequence unless it can also provide reliable service over the expected life of the system. Therefore, there is a need for an accurate reliability prediction methodology capable of considering the full spectrum of available interconnection assemblies. It is particularly essential to accurately predict printed wiring assembly failure rate because that is the most predominately used interconnection technology.

Failure rate and mean time between failure (MTBF) prediction capabilities are necessary in the development and maintenance of reliable electronic equipment. Predictions performed during the design phase yield early estimates of the anticipated equipment reliability and provide a quantitative basis for performing design trade-off analyses, reliability growth monitoring, maintenance action and spares allocation requirements, and life cycle cost studies.

A useful interconnection assembly failure rate prediction methodology should afford the optimal consideration of those qualities common to practical reliability assessment techniques including:

- a relatively uncomplicated approach which is easy to use and does not require intimate knowledge of device characteristics beyond readily available information

- the appropriate discrimination against device design and usage attributes which contribute to known failure mechanisms

- a dynamic, flexible expression, which, through simple modification, allows for the evaluation of newly emerging technologies

- reasonable accuracy over the total range of all parameters considered in the technique.

This report describes the approach, results and conclusions of the study and includes the proposed interconnection assembly reliability prediction models to replace Section 5.1.13 of MIL-HDBK-217D.

2. THEORETICAL ANALYSIS

2.1 Literature Review. A comprehensive literature review was performed to identify all published information which is relevant to the reliability of printed wiring boards, solder connections, discrete wiring boards and alternate types of connections and interconnection boards. Literature sources searched include the Reliability Analysis Center automated library information retrieval system, the National Technical Information Service (NTIS), the Defense Technical Information System (DTIS), and the Government Industry Data Exchange Program (GIDEP). Additionally, manufacturers and users of printed wiring and other interconnection assemblies have supplied useful information and test results.

The primary objective of the literature review was to locate references whose content could be used to supplement the data analysis process and to provide the reliability models with a sound theoretical foundation. An effort was undertaken to investigate the fundamental physical and electrical characteristics of each type of interconnection assembly in order to identify the respective failure mechanisms and the parameters having a significant impact on reliability. Once identified, the failure mechanisms were further studied to determine which combinations of the significant parameters would minimize and maximize their frequency of occurance.

Additionally, for types of interconnection assemblies which have been developed more recently and for which there exists limited field data, conclusions obtained through the literature review were merged with the available data to develop a useful prediction model.

2.2 Theoretical Discussions.

2.2.1 Plated Through Holes (PTH). The PTH multilayer printed wiring board consists of a number of layers of thin circuit boards which are stacked one above the other and laminated into one monolithic assembly. At the points of proposed interconnection, holes are drilled which pass through the pads on the conductors of the inner layers which are larger than the drilled hole. Drilling exposes a rim of copper around the entire circumference of the hole. The copper on the individual layers in the plated through hole is connected by copper plating. Plated through holes are also used for interconnection on discrete wiring w/PTH assemblies. The discrete wiring boards are plated in an electroless copper bath where copper is deposited to form the component holes and make connections to the discrete wires.

It is not uncommon to encounter manufacturing difficulties which result in PTHs which are subject to the formation of barrel cracks. This tendency to form barrel cracks is generally due either to imperfections in the PTH barrel wall which greatly amplify the level of axial strains, very poor effective ductility of the copper plating, or a combination of these two factors. Poor drilling or excessive acid etching during the hole wall cleaning process can lead to rough barrel walls. A level but thin plating on the rough barrel wall may then result in localized stress concentrations and large plastic strains. For certain copper electro-plating systems, the rough hole wall may also have a detrimental influence on grain growth and may produce locally weakened intergranular boundries which are easily fractured. Even if the PTH walls are smooth, variable electroplating processes may yield copper of very low conductivity.

A primary cause of printed wiring board failures is the mismatch of thermal coefficients of expansion in the plated through hole. The thermal coefficients of expansion for the copper plated through hole and the epoxy glass substrate are not compatible. When exposed to thermal cycling, the copper and the epoxy glass expand and contract at different rates creating

stresses in the plated through hole which can surpass the ultimate strength of the copper plating. Under laboratory conditions, 98% of all multilayer printed wiring board open circuits were found to be from 360° PTH barrel fractures.[1] A possible solution to this problem is the use of polyimide as a board material. Manufacturing difficulties have arisen, however, when printed wiring boards have been made with polyimide and its widespread use has not been observed.

PTH barrel stresses have been observed to be significantly higher in the central portion of the PTH. Approximately 30 times as many PTH failures were observed in the central 50% of the PTH in the laboratory.[2] The tested multilayer printed wiring boards were composed of eight circuit planes. Internal circuit planes inhibiting free expansion and additive loading on PTH lands were considered to be the principal reason for higher centralized stresses. As the number of internal circuit planes increase on a printed wiring board, the stresses in the central plated through hole region become larger.

Surface and internal land fractures were concentrated at the surfaces of the printed wiring board. The larger stresses were observed at the surfaces because those land areas have larger deflection than the internal lands; therefore, a dramatic increase in land fractures is not expected to correspond to an increase in circuit plane quantity. The stresss on the internal lands are less than the stresses on the surface, but the sum total of surface and internal land failures would be expected to increase as the quantity of circuit planes increases.

1,2. Harley, Strong and Young, Reliability Investigation of Thermal Stress/Fatigue Failure in Multilayer Interconnection Boards, RADC-TR-70-192.

Additionally, the thickness of the plating presents an important parameter effecting failure rate. Excessively thin plating in the PTH may result in more observed fractures. Thicker internal lands cause higher barrel stress by subjecting the PTH barrel to repetitive bending stresses during thermal cycling. A precise matching of surface and internal land thickness and barrel plating thickness is required to insure the highest quality PTH.

2.2.2 Solder Connections. There has been considerable work done on failure mechanisms in solder connections by Manko, Beal and Bangs, Ehuwaites, Zakrayck and others. This section briefly discusses several of the solder connection failure mechanisms. More detailed analyses are identified in the bibliography.

Solder connections that contain copper-tin-intermetallics or gold-tin intermetallics have relatively poor reliability characteristics. Test results have shown that solder connection failures are accelerated by pressure on the crack susceptible intermetallic compounds.

It has been shown in tests by Beal and Bangs that low frequency thermal cycling of solder connections promotes cracking in 63 Sn - 37 Pb alloy when cycled in the -65°C to 150°C range. The influence of thermal cycling is a primary cause of solder connection failure.

The plating process employed in the coating of leads prior to soldering has frequently been found to be a source for defects that contribute to solder connection failures. In most plating systems, organic polymers form and bath maintenance by carbon treatment is required to eliminate or minimize the presence of organic impurities which can co-deposit. Some of these polymers have extremely large molecules with lengths of up to one-half to one micron. These materials usually are readily absorbed by activated carbon and can be removed from the system.

The remaining polymer materials can be co-deposited, which can lead to stresses or faults in the deposit, giving rise to corrosion sites.

Bath cleaniless is essential. If a bath is properly maintained, there should be no problems with the electroplated deposit itself. An interesting fact is that only 5% of the problems arising in corrosion testing are due to plating systems that were not properly maintained, or kept in a clean conditon. Experience has demonstrated that the substrate being plated causes 95% of the subsequent failures. Take as an example a typical screw machine or stamped part. These parts normally have a surface finish of approximately 1um. Couple this with the fact that most metals today are being improperly recycled, thereby causing inclusions of foreign material (foreign metals and oxides of these metals). Accordingly, one must consider not only the surface preparation that is necessary, but also compensate for inclusions within the bulk, and also at the surface of the part.

In wave soldering, the solder is pumped out of a narrow slot to produce a wave or series of waves. The conveyor can be at a small angle to the horizontal to assist drainage of the solder, and double waves or special wave forms may also be used for this purpose. In cascade soldering, the solder flows down a trough by gravity and is returned by pump to the upper reservoir. These wave solder systems are excellent in that a virtually oxide-free solder surface is presented to the part, and removal of flux and vapors is also promoted by the flow of the solder.

Integrated wave soldering systems for printed wiring assemblies provide units that can apply the flux, dry and preheat the board, solder components, and clean the completed assembly. Some of the systems have special features where the flux is applied by passing through a wave, by spraying, by rolling, or by dipping. Several systems employ oil mixed with the solder to aid in the elimination of icicles and bridging between

conductor paths. Another system features dual waves flowing the opposite direction to the board travel.

The principal fluxes used for printed wiring assembly soldering are nonactivated, mildly activated and activated rosin. The choice of flux presents several reliability concerns which are considered briefly.

Noncorrosive fluxes all have rosin as a common ingredient. Rosin has unique physical and chemical properties which make it ideal as a flux. It melts at 127°C (260°F) and remains active in the molten state up to 315°C (600°F). The active constituent of rosin (abietic acid) is inert in the solid state, active when molten, and returns to an inactive state when cooled. Thus it is widely used in the electrical and electronics industries because the flux residue is noncorrosive and non-conductive.

Nonactivated rosin consists of rosin plasticized with an inert plasticizer for core solder or dissolved in an inert solvent as a liquid flux. No additives for the purpose of increasing flux activity are used. This is the mildest of the rosin fluxes, and only extremely clean and solderable metals can be soldered reliably with nonactivated rosin.

Because of the slow fluxing action of nonactivated rosin, mildly activated rosin is also used. It contains additives which improve the fluxing action of the rosin but leave residues which are noncorrosive and nonconducting. Mildly activated rosin is used in high reliability electronic assemblies, and removal of the flux residue is optional. Mildly activated rosin can be plasticized for core solder or dissolved in an organic solvent to provide a liquid flux.

The activated rosin fluxes are the most active of all and depend on the addition of small amounts of complex organic compounds for their increased activity. Hydrohalides of amines such as hydrazine hydrohalide,

glutamic acid hydrochlorides, cetyl pyridinium bromide, aniline hydrochloride and organic acids such as benzois and succinic have been disclosed in patent literature as additives for activated rosin fluxes to be used in liquid form or as a core material. Additive amounts varying from 0.2 to 5% have been used.

The use of activated rosin as a noncorrosive flux is based on the theory that the activator is decomposed by heat and that the residue is not electrically conductive and corrosive. High production-line speeds have demanded more highly active fluxes, but the question of harmful flux residues is still a matter of debate in critical applications where corrosion resistance is the foremost consideration.

If rosin residues must be removed, alcohol or chlorinated hydrocarbons may be used. Certain rosin activators are soluble in water but not in organic solvents. These flux residues require removal by organic solvents, followed by a water rinse.

2.2.3 Printed Wiring Boards (PWBs). Processing factors such as chemistry, lamination parameters, etc., have an influence on moisture content within the board material, although no single dominant factor has been identified. Likewise, the effect of assembly processing (baking, fluxing, soldering, cleaning, etc.) have been shown to influence printed wiring board failure rate.

A materials/process related problem of considerable importance is the following: if in raw material manufacture, or multilayer board lamination, contamination from foreign fibers occurs, PWB reliability may suffer. As an inclusion in the dielectric composite, foreign fibers may contact an anodically biased conductor and even bridge to a nearby cathode. Filament growth has often been observed to occur rapidly at accelerated test conditions. Hence, preventing this type of contamination is extremely important.

Other factors relative to PWB configuration should be mentioned here. For example, when conformal coatings are applied to the finished PWB, an intensification of the foreign fiber failure mechanism is often observed, together with a shortening of PWB life. An apparently related observation is that failures in multilayer boards tend to occur first on the most deeply buried innerlayers, and later on the layers closest to the board surfaces. The reasons for this behavior are not yet fully understood.

Another factor which influences failure rate is the spacing between conductor traces on the printed wiring board. It has been shown that as conductor trace spacing drops below approximately 4 mils, the failure rate is adversely effected.[3] Above 4 mils spacing, there appears to be no significant effect on failure rate. Most of the current high density printed wiring boards range between 5 to 10 mils spacing and trace width and spacing are not important failure rate influencing variables.

It is emphasized that this section addressed printed wiring board reliability characteristics not associated with plated through holes. Plated through hole failures account for up to 98% of all printed wiring assembly failures (Section 2.2.1).

2.2.4 Solderless Wrap Assembies. The solderless wrap process consists of wrapping a solid conductor around a post with sharp corners. The wire is wrapped while under tension, causing deformation of the wire at the sharp corners of the post. The post is also deformed under the wire. The resulting joint provides a gas tight interface between the wire and the post. Two types of wrap are used. One type has all bare wire wrapped on the post, while the other has an insulated turn (last turn) wrapped on the post. Under dynamic conditions, the deformed wire acts as a stress

3 Lanti, Delaney and Hines, The Characteristic Wearout Process in Epoxy-Glass Printed Wiring Circuits for High Density Electronic Packaging, Bell Laboratories.

concentration notch which may result in low fatigue life. The insulated turn prevents deformation of the wire at the last turn, thereby eliminating the stress concentration notch.

The solderless wrap technique is limited to round solid wire since the properties of solid wire are needed to assure the intimate and uniform contact which assures continuity. Control of material properties of the wire, terminals and coatings of these material is necessary to assure reliable solderless wrap connections.

The wire generally used is round soft copper that is plated with tin, tin-lead alloy, silver or gold. Special tools for wrapping are commercially available. Failure mechanisms for solderless wrap assemblies include insufficient tension in the wire and lack of required hardness in the copper wire. These failure mechanisms will cause a voltage drop across the wire and post interface.

2.2.5 Wrapped and Soldered Assemblies. The wrapped and soldered process consists of wrapping an insulated wire around a post with sharp corners. The wrapping process has several physical similarities to the solderless wrap process. But instead of forming a gas tight, tension induced connection, solder is applied to the wraps to form the permanent connection. Controls of material properties of the wire, terminal posts and wire insulation is necessary to assure reliable wrapped and soldered connections. Additionally, tool calibration and surface solderability are important reliability characteristics concerning wrapped and soldered assemblies.

Test information concerning wrapped and soldered assemblies is not available. Possible failure mechanisms concern incomplete removal of insulation or residual carbonized products resulting in a weaker wrapped and soldered connection.

2.2.6 Clip Termination Assemblies. Clip termination assemblies are designed to provide reliable electrical and mechanical terminations for use as an interconnection assembly. The clip termination process briefly consists of a length of wire, automatically stripped, compressed, wiped along the terminal post during the termination process and held in place by a metal clip. The process is accomplished by either hand tool application or by automatic point to point wiring machines. Control of material properties of the wire, the clip and the terminal post is necessary to assure reliable clip termination assemblies.

Results of reliability tests subjecting the clip termination assemblies to vibration, thermal shock, salt spray and humidity do not reveal any inherent weaknesses in the clip termination technology. Potential failure mechanisms for clip termination assemblies include variable gas tight clip characteristics, relaxation of spring tension and dimensional variability (clip vs. wire vs. terminal post).

2.2.7 Discrete Wiring Assembly w/Electroless Deposited PTH. A study by R.J. Clarke[4] provided the following theoretical discussions concerning manufacturing processes and failure mechanisms. A discrete wiring assembly with electroless deposited plated through holes is basically a pattern of insulated wires laid down on an adhesive coated substrate by a numerically controlled machine. The wire used is NEMA 34-gauge polyimide insulated wire, equivalent to a .024 inch flat printed circuit conductor of one ounce copper foil. A thin (0.0004 inch) low-flow epoxy-glass pre-peg is laminated to the surfaces of the panel, over the wires, to give added protection to the finished board. The adhesive and pre-peg are then cured by an oven bake to encapsulate the wire. A temporary mask is applied to both surfaces of the board for protection

4 Clark, R.J. (General Electric Company), High Speed Logic Packaging Using Multiwire Interconnection Technology, Presented at the 1976 Wescon Professional Program.

during subsequent chemical cleaning operations. Holes are drilled in the board using conventional printed circuit NC drilling equipment. After drilling, most of the holes have one or two wire cross sections exposed at the wall of the hole.

A cleaning cycle removes epoxy or adhesive smears and etches the polyimide insulation about 0.002 inches to expose a wire stub at the wall of the hole. After cleaning, the drilled boards are plated in an electroless copper bath where copper is deposited to form the component PTH's and electrically connect the PTH to the wires. Typically, 0.0015 inches of copper is plated in the holes, but thicker deposits are possible. After copper plating, the temporary mask is removed and a protective finish is applied to the copper to prevent oxidation and ensure good solderability. The components are then assembled by either a hand soldering or wave soldering operation.

Two failure mode areas in discrete wiring assemblies w/PTH are the wire crossovers and wire ends to PTH interface. The wire crossover potentially can be a source of failure. When one wire crosses another, there is typically 0.0012 inch of polyimide insulation between them. The typical breakdown voltage at a single crossover is 1,500 - 2,000 volts. Photomicrographics of a wire crossover show some deformation of the upper wire due to the motion of the pressure foot at ultrasonic frequencies. The wire is ordinarilly tested by the manufacturer to determine its ability to maintain insulation integrity under extreme conditions. Environmental testing at several testing laboratories has shown no degradation of the insulation resistance between crossovers after thermal shock, thermal cycling, shock vibration, humidity cycling and exposure to salt spray.

Test data accumulated to date indicates that the connection of the wire end to the copper plating in the PTH is very reliable. The cleaning cycle removes the insulation from the wire and exposes about 0.002 inch of the wire. The drilling operation slightly deforms the wire end resulting

in a "nailhead" condition. When electroless copper is deposited in the hole, there is not only the connection formed by the interlocking grain structures of the frontal cross sectional area of the wire and plated copper, but also a mechanical condition formed by the circumferential deposition of copper around the area of the wire end where the insulation was removed.

3. DATA COLLECTION AND PRELIMINARY ANALYSIS

3.1 Data Collection and Reduction. The modification of current failure rate prediction models or the development of new prediction methodologies should be derived from field failure rate data obtained from closely monitered systems. Modeling activities require extensive data resources because failure rate prediction models derived using limited data will reflect the characteristics of only that information. This section presents the data collection procedure followed and the preliminary analysis used to develop a useful interconnection assembly data base.

One of the advantages offered by a printed wiring "assembly" level prediction model was the ability to acquire a more extensive data base. Exhaustive failure analysis is required to differentiate between a plated through hole failure and a solder connection failure. Both types of failures can appear in maintenance reports as a connection open circuit. Most of the available data sources do not perform extensive analysis. But because the intention of the study was to develop a printed wiring "assembly" failure rate prediction model, data sources without failure analysis were included in the data base. This is because failures which could not be classified as either printed wiring board or solder connection failures would still be correctly regarded as an "assembly" failure.

The Reliability Analysis Center operated by the IIT Research Institute at Griffiss Air Force Base was solicited to aid in the data collection process. The Reliability Analysis Center regularly pursues the collection of nonelectronic parts reliability data including printed wiring

boards, solder connections and other pertinent interconnection methods. Data resources which had been collected and summarized prior to the initiation of this study were availabile for analysis. However, the requirements for extensive data resources necessitated additional data collection activities to supplement the existing information.

A survey of commercial, industrial and goverment organizations was conducted shortly after the beginning of the study. Organizations contacted either manufactured, used or were similarly connected with one or more of the interconnection technologies. Information requested included field experience data, pre-production and production equipment tests, failure analysis reports and physical construction details. A sum total of over 400 organizations were contacted. Approximately 10% of all organizations contacted during the data collection effort submitted information pertaining to printed wiring or alternative types of interconnection assemblies. Additionally, a GIDEP (Government Industry Data Exchange Program), Urgent Data Request was submitted and circulated. However, no significant results came of this action. A primary concern of the majority of contributors was the proprietary nature of the information and the desire to remain anonymous. For this reason, none of the data contributors in this study will be identified.

A prerequisite to the summarization of data was the identification of all parameters and factors influencing the reliabilty of interconnection assemblies. A task was defined at the beginning of the program whose goal was a reliability evaluation based solely on theoretical considerations. These theoretical studies served to identify the important parameters which were then further investigated using data analysis. Identification of construction details and process controls which were theoretically believed to have an effect on reliability were pursued for each source of data.

All data items received during the data collection efforts were reviewed for completeness of deta and examined for any inherent biases. Any data submittal which displayed obvious biases was not considered in this study. Those reports lacking sufficient detail were not considered until the necessary additional information was acquired.

A summary of the collected and reduced data is given in Table 3.1. Table 3.1 presents assembly operating hours, connection operating hours and recorded failures for each type of interconnection technology. It is emphasized that the recorded failures for printed wiring assemblies include both printed wiring board and solder connection failures. The number of connection operating hours is obtained simply by multiplying the number of connections on the assembly by the operating hours.

TABLE 3.1: DATA SUMMARY BY TECHNOLOGY

Technology	Assy. Hrs. ($\times 10^6$)	Connection Hrs. ($\times 10^6$)	Failures
Wave Soldered Printed Wiring	950.876	348,502.940	81
Reflow Soldered Printed Wiring	*	48,445.115	4
Solderless Wrap	*	328,956.105	4
Wrapped and Soldered	*	3,056.630	0
Clip Termination	16.530	1,670.368	0
Discrete Wiring w/Electroless Deposited PTH	0.546	477.204	1

*Precise values for assembly operating hours not available

3.2 Failure Rate Distribution Considerations. The interconnection assembly data base contains no time-to-failure data. As a result, only the exponential failure rate distribution with its underlying constant failure rate could have been considered to model the predicted failure rate. The exponential distribution provides many advantages in regard to reliability modeling. Use of the exponential distribution is consistent with existing MIL-HDBK-217C failure rate prediction models, provides for maximum data utilization and offers a simple calculation for mean time to failure (MTTF). However, accelerated testing has demonstrated that nonelectronic parts including interconnection assemblies follow an increasing, time dependent failure rate. This section provides a discussion considering whether the exponential distribution can adequately describe the failure rate of printed wiring assemblies.

The test conditions which printed wiring assemblies are often exposed to consist of thermal cycling in the range of roughly -50°C to 100°C. Each thermal cycle creates stress in the copper plated through hole which can exceed the elastic region of the copper stress-strain curve. When the elastic region of the stress-strain curve is exceeded, the plated through hole remains slightly deformed even after the applied stress is eliminated. The continuous cycling induces fatigue type failures resulting from the accumulated effect of each successive thermal cycle. These failures are clearly time dependent. The yield point on the stress-strain curve represents the division between the elastic and plastic ranges. The yield point is estimated at between 20,000 psi to 65,000 psi for the copper plating.

Initially consideration was given to printed wiring assemblies operating in relatively benign conditions. The temperature differences observed in the benign environments do not approach the levels tested in the laboratory. The induced stress in the copper plated through hole does not approach the yield point of the stress-strain curve and fatigue induced failures are not observed. Failures observed in the relatively benign environments generally relate to poor quality copper plating or random

(time independent) high stress levels which exceed the ultimate strength of the plated through holes or the solder connections. While acknowledging that wearout failures will still occur, the conclusion is that the failure rate for printed wiring assemblies operating in benign environments closely follows an exponential distribution over the intended life of the equipment. The environment classifications which are considered relatively benign are ground benign, ground fixed, naval submarine, space flight and naval sheltered.

In the case of application environments which do include severe thermal cycling, time dependent fatigue type failures would be expected to occur. If a fixed population of plated through hole printed wiring assemblies were allowed to complete a life history, an increasing failure rate distribution could be estimated. However, since the state of the art in the electronics industry changes at a rapid rate, electrical equipment that is designed today will be obsolete in roughly ten years. In 1970, the current widespread use of multilayer technology was not observed and with the advent of higher density VLSI circuitry and chip carriers, the present printed wiring boards already face certain unavoidable changes. In ten years of continuous operating time, a single plated through hole would not come close to recording sufficient operating hours to expect even one failure in the harshest avionic environment. Ten years is a relatively short time compared to MTBF for printed wiring assemblies. The conclusion was made that the failure rate for printed wiring assemblies does not become dominated by wearout failures until a long time after the intended use of the equipment. Additionally it was concluded that the failures observed during this study effort were primarily random occurrences of high stress levels and that the exponential distribution can approximate the failure rate of printed wiring assemblies operating in any environment over the intended lifetime of the equipment. Occurrences of random high stress levels which may exceed the ultimate strength of the plated through holes or solder connections would not be unusual in a stressful environment classification such as airborne, uninhabited fighter.

For the purposes of this study, it was concluded that utilization of the exponential distribution for each application provides accurate failure rate predictions.

4. FAILURE RATE PREDICTION MODEL DEVELOPMENT

4.1 Printed Wiring Assemblies.

4.1.1 Proposed Failure Rate Prediction Model. This section presents the proposed failure rate prediction model for printed wiring assemblies. This recommended addition to the existing MIL-HDBK-217C models is the result of analyses performed on the data base compiled during the study. The failure rate prediction model for printed wiring assemblies is:

$$\lambda_p = \lambda_b \pi_Q \pi_E \Sigma [N_i (\pi_C + \pi_{Si})]$$

where

λ_b = base failure rate = .000041 failures/10^6 hrs.

π_Q = quality factor, Table 4.1-3

π_E = environmental factor, Table 4.1-4

N_1 = quantity of wave soldered plated through holes

N_2 = quantity of hand soldered plated through holes

π_C = complexity factor, Table 4.1-1

π_{Si} = solder application factors, Table 4.1-2

The remaining sections pertaining to printed wiring assembly failure rate prediction model development give the detailed procedures which resulted in the above failure rate prediction model and the numerical values given in Tables 4.1-1 through 4.1-4.

TABLE 4.1-1
COMPLEXITY FACTOR

# of circuit planes	π_C
≤ 2	1
3	1.3
4	1.5
5	1.8
6	2.0
7	2.2
8	2.4
9	2.6
10	2.7
11	2.9
12	3.1
13	3.2
14	3.4
15	3.5
16	3.7

for greater than 16 circuit planes

$\pi_C = 0.65\ \ell^{.63}$

ℓ = quantity of circuit planes

TABLE 4.1-2
SOLDER APPLICATION FACTOR

Process	Rework Percentage	π_S
Wave Solder	0 - 5	0
	6 - 10	0.2
	11 - 15	0.9
	16 - 20	1.5
	21 - 25	2.2
	26 - 30	2.9
	31 - 35	3.6
	36 - 40	4.3
	over 40	6.1
	Unknown	6.1
Hand Solder	Not applicable	13

TABLE 4.1-3
QUALITY FACTOR

Quality Grade	π_Q
Manufactured to MIL-SPEC or equivalent IPC standards	1
Lower quality grade	10

TABLE 4.1-4

ENVIRONMENTAL FACTOR

Environment	π_E
G_B	1
S_F	1
G_F	2.3
N_{SB}	4.1
N_S	5.3
A_{IT}	3.8
M_P	6.9
M_{FF}	8.7
M_{FA}	12
G_M	7.7
N_H	13
N_{UU}	14
A_{UT}	8.2
N_U	12
A_{IF}	7.7
A_{RW}	19
U_{SL}	26
A_{UF}	16
M_L	29
C_L	500

4.1.2 Preliminary Assumptions and Methodology. The methodology necessary to extract an accurate and useful failure rate prediction model from the vast number of variables affecting printed wiring assembly reliability is included in this section. Assumptions based on theoretical discussions and/or data analysis are noted as they occur in the prediction model development process.

Variables considered to effect printed wiring assembly failure rate are given in Table 4.1-5. These variables are divided into two major categories: (1) Construction details and process controls, and (2) Environmental stresses. The assumption is made that the printed wiring assembly failure rate (λ_p) can be expressed as a function of construction details and process controls multiplied by a function of environmental stresses. A series of environmental factors (π_E) was used to define the function of environmental stresses. They were normalized to a value of one corresponding to printed wiring assemblies operating in the ground, benign environment. In equation form:

$$\lambda_p = f(\text{construction details, process controls})\ \pi_E$$

where

$\lambda_p \equiv$ printed wiring assembly failure rate

$\pi_E \equiv$ environmental factor

This is consistent with existing MIL-HDBK-217C failure rate prediction models. This is also a necessary assumption because environment conditions such as temperature cycling vary within an environment classification, and that specific information would not be available during the design stage of equipment when failure rate predictions prove most beneficial.

TABLE 4.1-5

FACTORS INFLUENCING PRINTED WIRING ASSEMBLY FAILURE RATE

- Construction Details and Process Controls
  - Number of plated through holes (PTH)
  - Number of circuit planes
  - Foil weight
  - PTH plating thickness
  - PTH diameter
  - Number of solder connections
  - Method of solder application
  - Amount of rework necessary on solder connections
  - Solderability of component leads
  - Type of conformal coating, if any
- Environmental Stresses
  - Effect of temperature cycling
  - Effect of thermal shock
  - Effect of humidity
  - Effect of random vibration
  - Effect of sine vibration
  - Effect of mechanical shock

The function of construction details and process controls was assumed equal to the sum of the failure rate contribution of the plated through hole, the failure rate contribution of the solder connections and the combined other failure rate contributions. In equation form:

$$\lambda_p = [\lambda_{p,pth} + \lambda_{p,ws} + \lambda_{p,other}] \pi_E$$

where

$\lambda_{p,pth}$ = failure rate contribution of the plated through holes

$\lambda_{p,ws}$ = failure rate contribution of the solder connections

$\lambda_{p,other}$ = combined other failure rate contributions

This assumption considers the three subcomponents of the failure rate equation to be independent. This is a reasonable assumption and will be discussed later in this section.

The three subcomponents which define the function of construction details and process controls were initially considered separately. The plated through hole (PTH) failure rate contribution includes not only plated through hole failures, but PTH associated failures such as open circuits resulting from fractures between the PTH and an internal land.

Both theoretical discussions and data analysis revealed that the two dominant variables affecting PTH failure rate contribution are the total number of PTH's and the total number of circuit planes on the considered printed wiring assembly.

The assumption was made that the failure rate contribution for an individual PTH is independent of the total number of PTH's and is constant for a particular number of circuit planes. The failure rate contribution of the PTHs is given by the following equation:

$$\lambda_{p,pth} = \lambda_{pth}(\ell)\, N$$

where

$\lambda_{pth}(\ell)$ = individual PTH failure rate as a function of ℓ

ℓ = number of circuit planes

N = quantity of PTHs

It is noted that the notation used, $\lambda_{pth}(\ell)$, represents failure rate as a function of circuit plane quantity and should not be confused with the use of parenthesis to denote multiplication. This term, $\lambda_{pth}(\ell)$, will be the only term which uses this notation.

Next, the failure rate contribution of wave solder connections was considered. The wave solder failure rate contribution is highly variable, depending on the total number of solder connections, the solderability of the component leads, the amount of rework necessary after the printed wiring assembly passes through the solder wave, the printed wiring assembly design and other factors. The assumption was made that the total number of solder connections and the amount of rework are the two dominant variables affecting the failure rate contribution of wave solder connections. Factors such as solderability of component leads and printed wiring assembly design are not included directly in the model. However, the amount of necessary rework gives an indication of solderability and design, and therefore, the influence of these factors was not neglected. Additionally, the amount of rework is important because the reworked solder connection will inherently have a higher failure rate due to the variability of direct human involvement.

The net failure rate contribution of solder connections was assumed proportional to the total number of solder connections. Additionally, the

average failure rate of an individual solder connection was assumed independent of the total number of solder connections. In equation form:

$$\lambda_{p,ws} = \lambda_{ws} n$$

where

λ_{ws} = average solder connection failure rate

n = quantity of solder connections

Since the average solder connection failure rate (λ_{ws}) is a variable depending on rework percentage, it was desirable to define several special cases. Notation listed below is for λ_{ws} when (1) there is zero necessary rework, (2) there is total or 100% rework and (3) there is an average rework percentage. Additionally, the rework percentage will be denoted as x.

λ_0 = λ_{ws}, ($x = 0$, zero rework)

λ_{rw} = λ_{ws}, ($x = 1$, total rework)

$\lambda_{\overline{x}}$ = λ_{ws}, ($x = \overline{x}$, average rework)

x = rework percentage ($0 \leq x \leq 1$)

$\overline{x}$ = average rework percentage

$\overline{x}$ represents a constant value of rework and therefore $\lambda_{\overline{x}}$ is a constant value. Similarly, λ_0 and λ_{rw} are constant values for the remainder of the model development process.

Average solder connection failure rates for the three special cases have the following relation:

$$\lambda_{rw} > \lambda_{\bar{x}} > \lambda_o$$

It should be intuitively clear that this relation is correct. The relation simply states that failure rate is an increasing function of rework percentage. The inequality is also informative because the zero rework and total rework cases represent the minimum and maximum possible values for average solder connection failure rate (λ_{ws}). Failure rates for rework percentages not at zero, total or average values were defined as a linear function between the two extremes.

$$\lambda_{ws} = \lambda_o (1 - x) + \lambda_{rw} x$$

where all variables have been previously defined

It is noticed that the above equation collapses to the correct values when $x = 0$, or $x = 1$, is used. The above relation is shown graphically in Figure 4.1-1.

Although the equation for λ_{ws} is in a simple form, it is desirable to transform the equation in order to simplify the process of adding the failure rate contribution of the plated through holes to the failure rate contribution of the solder connections. The transformed equation is:

$$\lambda_{ws} = \lambda_{\bar{x}} + D$$

where

$\lambda_{\bar{x}}$ = λ_{ws} when rework percentage is at an average value

D = deviation from $\lambda_{\bar{x}}$ to complete equality

D must be a function of rework percentage for the given equality. $\lambda_{\bar{x}}$ can be solved for by using the equation:

$$\lambda_{ws} = \lambda_o (1 - x) + \lambda_{rw}\bar{x}$$

$$\lambda_{\bar{x}} = \lambda_o (1 - \bar{x}) + \lambda_{rw}\bar{x}$$

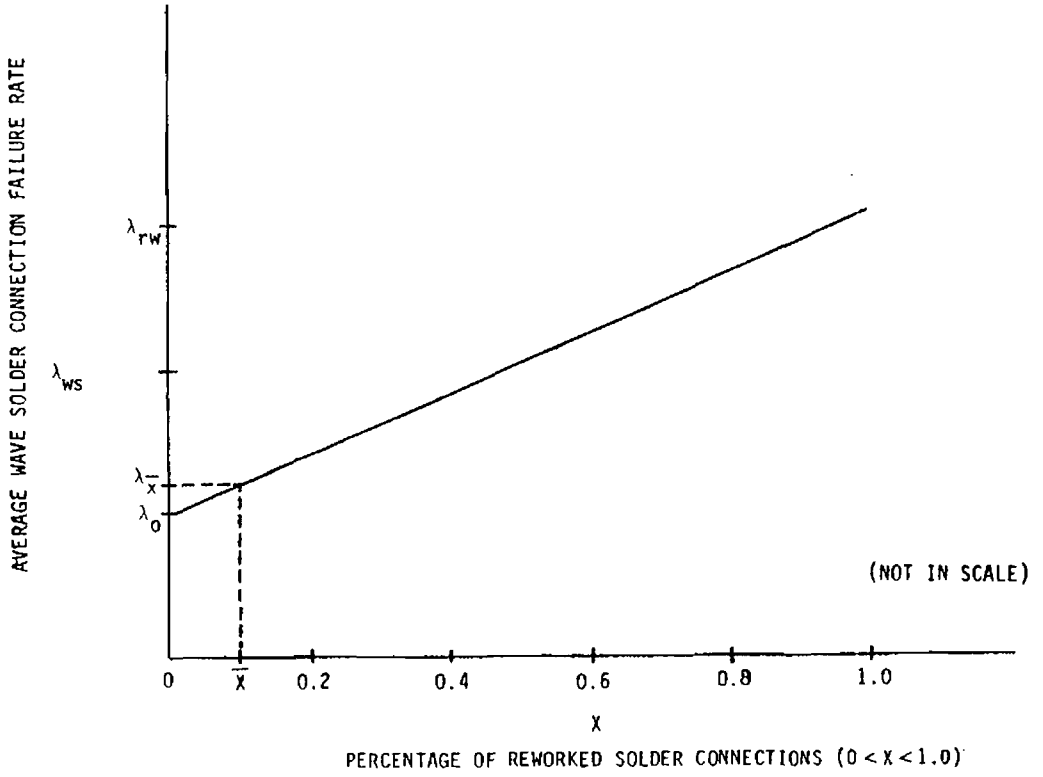


FIGURE 4.1-1 AVERAGE WAVE SOLDER CONNECTION FAILURE RATE VS. REWORK PERCENTAGE

This relation can be used to solve for D by the following steps:

$$\lambda_{ws} = \lambda_{\bar{x}} + D$$

$$\lambda_o (1 - x) + \lambda_{rw} x = \lambda_o (1 - \bar{x}) + \lambda_{rw} \bar{x} + D$$

$$\lambda_o + (\lambda_{rw} - \lambda_o) x = \lambda_o + (\lambda_{rw} - \lambda_o) \bar{x} + D$$

$$(\lambda_{rw} - \lambda_o) x = (\lambda_{rw} - \lambda_o) \bar{x} + D$$

$$D = (\lambda_{rw} - \lambda_o) (x - \bar{x})$$

Substituting this relation for D into the equation for average solder connection failure rate results in:

$$\lambda_{ws} = \lambda_{\bar{x}} + (\lambda_{rw} - \lambda_o) (x - \bar{x})$$

which is mathematically identical to the original equation for λ_{ws} and is also shown graphically by Figure 4.1-1.

Sustituting into the equation for net failure rate contribution of solder connections, the result is:

$$\lambda_{p,ws} = [\lambda_{\bar{x}} + (\lambda_{rw} - \lambda_o) (x - \bar{x})] n$$

Since it was the objective of this study to formulate a single printed wiring assembly failure rate prediction model, the feasibility of adding the solder connection failure rate contribution term to the relation developed for plated through hole failure rate contribution was considered. Therefore, it was necessary to investigate the ratio of the quantity of solder connections to the quantity of plated through holes (n/N ratio). In many cases this ratio is equal to unity. However, many other examples of printed wiring assemblies exist which have "via" holes or

unloaded plated through holes. The presence of the "via" holes result in the n/N ratio taking a value sightly less than unity. The increment which the n/N ratio differs from unity has been found generally to be of such a small magnitude that assuming the ratio is equal to one for all printed wiring assemblies does not introduce significant errors. Applying this assumption to the equation for failure rate contribution of solder connections resulted in:

$$\lambda_{p,ws} = [\lambda_{\overline{x}} + (\lambda_{rw} - \lambda_o)(x - \overline{x})]n$$

$$\lambda_{p,ws} = \frac{n}{N}[\lambda_{\overline{x}} + (\lambda_{rw} = \lambda_o)(x - \overline{x})]N$$

$$\lambda_{p,ws} = [\lambda_{\overline{x}} + (\lambda_{rw} - \lambda_o)(x - \overline{x})]N$$

This equation is now in a form that is most compatible with the PTH failure rate contribution equation.

Finally, all additional failure mechanisms which contribute to printed wiring assembly failure rate are lumped into the category of $\lambda_{p,other}$. Where extensive failure analysis has been available, it has been found that:

$$(\lambda_{p,pth} + \lambda_{p,ws}) >> \lambda_{p,other}$$

From theoretical discussions, the assumption was made that $\lambda_{p,other}$ is an increasing function of the number of plated through holes. A practical example is that as the number of PTH's increase, the number of trace paths and thus the sum length of the trace paths would increase. This would result in an increase in the probability of a trace-to-trace short, therby raising failure rate. Other factors which were thought to influence $\lambda_{p,other}$ such as conformal coating were investigated using data analysis and no significant effect was detected. Since the quality of data

corresponding to $\lambda_{p,other}$ was too limited to develop a more exact relation, the assumption was made that $\lambda_{p,other}$ is a linear function of N (PTH count), and no other variables.

$$\lambda_{p,other} = \lambda_{other} N$$

where

$\lambda_{p,other}$ = combined other failure rate contributions
λ_{other} = estimated constant value
N = quantity of plated through holes

Any inaccuracies introduced by this assumption are negligible due to the previously stated inequality.

The three subcomponents of the printed wiring assembly failure rate prediction model were summed to derive the following equation:

$$\lambda_p = [\lambda_{pth}(\ell) + \lambda_{\overline{x}} + (\lambda_{rw} - \lambda_o)(x - \overline{x}) + \lambda_{other}] N \pi_E$$

rearranging,

$$\lambda_p = [(\lambda_{pth}(\ell) + \lambda_{\overline{x}} + \lambda_{other}) + (\lambda_{rw} - \lambda_o)(x - \overline{x})] N \pi_E$$

The first part of this equation $\{\lambda_{pth}(\ell) + \lambda_{\overline{x}} + \lambda_{other}\}$ varies only with the quantity of circuit planes and was analyzed using the data base. Data analysis including the utilization of curve-fitting techniques and correlation coefficients resulted in the following optimal relation:

$$\lambda_{pth}(\ell) + \lambda_{\overline{x}} + \lambda_{other} = \lambda_b \left(\frac{\ell}{\ell_o}\right)^a , \ell > o$$

where

λ_b = base failure rate
ℓ_o = a constant number of circuit planes
a = constant

As was mentioned before in this section, the three subcomponents of the printed wiring assembly failure rate prediction model were assumed to be independent. If small inaccuracies were introduced in that assumption, then they would be eliminated in the above step because λ_b was determined from the data and therefore included any differentials caused by an inaccurate assumption of independence.

In the above equation, ℓ_o is a chosen constant number of circuit planes and λ_b and a are constants obtained through data analysis. The ℓ_o term was set equal to two circuit planes (a double sided printed wiring board) which is the minimum number of circuit planes included in the data base.

Sustituting into the printed wiring assembly failure rate prediction model, the result was:

$$\lambda_p = \left[\lambda_b \left(\frac{\ell}{\ell_o} \right)^a + (\lambda_{rw} - \lambda_o) (x - \bar{x}) \right] N \pi_E$$

Complexity factor and solder application factor were defined as:

$$\pi_C = \left(\ell / \ell_o \right)^a$$

$\pi_C \equiv$ Complexity factor

$$\pi_S = \frac{1}{\lambda_b} \left[(\lambda_{rw} - \lambda_o) (x - \bar{x}) \right]$$

$\pi_S \equiv$ Solder application factor

Substituting the above defined relations for complexity factor and solder application factor, the equation for λ_p becomes:

$$\lambda_p = \lambda_b N (\pi_C + \pi_S) \pi_E$$

Additionally, a quality factor (π_Q) was introduced as a means of assigning a higher predicted failure rate to printed wiring assemblies not manufactured to specifications similar to those considered in this reliability study. The quality factor is multiplicative and its inclusion results in the following printed wiring assembly failure rate prediction model:

$$\lambda_p = \lambda_b N (\pi_C + \pi_S) \pi_Q \pi_E$$

This failure rate prediction model for printed wiring assemblies applied only to wave soldered assemblies. Many cases exist where hand soldered assemblies are manufactured. A solder application factor for hand soldered printed wiring assemblies was also developed. The hand soldered, solder application factor is:

$$\pi_S = \frac{1}{\lambda_b} (\lambda_{hs} - \lambda_{\overline{x}})$$

where

λ_b = base failure rate

λ_{hs} = hand solder connection failure rate

$\lambda_{\overline{x}}$ = average wave solder connection failure rate for a constant, average rework percentage

This equation assumes a constant failure rate for hand solder connections.

Printed wiring assemblies which utilize heat sensitive or open devices often require both wave soldering and hand soldering operations. The failure rates for the hand soldered and wave soldered plated through holes were considered individually and then summed. This could be done

because plated through hole quantity is proportional to failure rate. The printed wiring assembly failure rate for assemblies requiring hand and wave soldering is:

$$\lambda_p = \lambda_b N_1 (\pi_C + \pi_{S_1}) \pi_Q \pi_E + \lambda_b N_2 (\pi_C + \pi_{S_2}) \pi_Q \pi_E$$

where

N_1 = quantity of wave soldered PTHs

π_{S_1} = wave solder, solder application factor (a function of rework percentage)

N_2 = quantity of hand soldered PTHs

π_{S_2} = hand solder, solder application factor

all other parameters have been previously defined

This rather cumbersome equation was simplified to form the final printed wiring assembly failure rate prediction model:

$$\lambda_p = \lambda_b \pi_Q \pi_E \sum [N_i (\pi_C + \pi_{Si})]$$

where

λ_b = base failure rate
π_Q = quality factor
π_E = environmental factor
N_1 = quantity of wave soldered PTHs
N_2 = quantity of hand soldered PTHs
π_C = complexity factor
π_{Si} = solder application factors

4.1.3 Environmental Factor. The printed wiring assembly failure rate prediction model as proposed in this study would replace the existing printed wiring board (PWB) and connection models. A result is the absence of an existing series of environmental factors for the proposed model. This would not create any problems if printed wiring assembly failure rate data was plentiful in all environments, but this was not the case. Data has been collected and summarized in nine different user environments. This data must be used cautiously, however, because data within an environment classification based on limited data sources may contain potential biases. Therefore, the summarized data together with the existing environmental factors for PWB's and connections as presented in RADC-TR-80-299, Revision of Environmental Factors for MIL-HDBK-217B, was used to generate the optimal environmental factors presented in this section.

There are several necessary assumptions which must be made prior to data analysis. The first assumption is that the existing environmental factors accurately define the effect of environmental stress on PWB's and connections, respectively. The technical study (RADC-TR-80-299) which derived the two series of environmental factors is dated September 1980, and should represent current information. These environmental factor values are given in Table 4.1-6. The second assumption is that a printed wiring assembly environmental factor (π_E) would fall somewhere in between the values derived for printed wiring boards ($\pi_{E,PWB}$) and connections ($\pi_{E,C}$). This assumption follows from the first assumption and should be intuitively obvious. The next assumption is that printed wiring assembly environmental factors can be expressed as a linear combination of PWB and connection environmental factors or:

$$\pi_E = A\ \pi_{E,C} + B\ \pi_{E,PWB}$$

$$A + B = 1$$

where

π_E = printed wiring assembly environmental factor

$\pi_{E,C}$ = existing connection environmental factor

$\pi_{E,PWB}$ = existing PWB environmental factor

A and B = unknown constants ($0 < A < 1$, $0 < B < 1$)

Using data analysis to obtain best fit values for A and B minimized the effect of biases contained in individual environment classifications and was used to obtain environmental factors where no data exists.

TABLE 4.1-6 ENVIRONMENTAL FACTORS FOR PRINTED WIRING BOARDS AND CONNECTIONS

ENVIRONMENT	CONNECTIONS $\pi_{E,C}$	PWB $\pi_{E,PWB}$
GB	1	1
SF	1	1
GF	2.1	2.4
NSB	3.5	4.4
NS	4.4	5.7
AIT	3.0	4.2
MP	7.3	6.7
MFF	7.3	9.3
MFA	10	13
GM	7.3	7.8
NH	11	14
NUU	12	15
AUT	4	10
NU	9.9	13
AIF	6	8.4
ARW	16	20
USL	22	27
AUF	8	20
ML	25	31
CL	420	530

The procedure followed was to assume a series of environmental factors from the equation:

$$\pi_E = A\,\pi_{E,C} + B\,\pi_{E,PWB}$$

where the constants were initially set at (A = 0, B = 1.0) then investigated at (A = 0.1, B = 0.9), (A = 0.2, B = 0.8),..., (A = 0.9, B = 0.1) and (A = 1.0, B = 0). At each point, the assumed series of environmental factors were compared to the observed series of environment factors which were obtained by:

$$\pi_E = \frac{\lambda_p}{N}\,\frac{1}{\lambda_b \pi_C}$$

This equation is very similar to the wave soldered printed wiring assembly failure rate prediction model transformed into an equation for environmental factor. Differences will be discussed later in this section. λ_p, the printed wiring assembly failure rate and N, the number of plated through holes in the above equation were easily obtained from the data base. Complexity factor (π_C) was defined in the previous section as a power function of , the number of circuit planes. The complexity factor function was solved for by using the assumed series of environmental factors to normalize the data to ground, benign conditions and then applying regression analysis for best fit of the data. Because of the normalization of the data, the complexity factor function varies with the assumed environmental factors. Complexity factors given as a function of assumed environmental factors are listed in Table 4.1-7. Base failure rate (λ_b) was temporarily obtained by using the data accumulated in the ground, benign environment ($\pi_E = 1$), normalized for complexity to a base failure rate corresponding to 2 circuit planes ($\ell = 2$, $\pi_C = 1$). Thus every unknown in the above equation was found with reasonable confidence and a series of observed (or calculated) environmental factors were generated. The summarized data used for environmental factor development is given in Table 4.1-8.

TABLE 4.1-7 COMPLEXITY FACTORS VS. ASSUMED ENVIRONMENTAL FACTORS

$\pi_E = A\ \pi_{E,C} + B\ \pi_{E,PWB}$		$\pi_C = (\ell/2)^a$
A	B	a
0	1.0	0.510
0.1	0.9	0.546
0.2	0.8	0.585
0.3	0.7	0.627
0.4	0.6	0.674
0.5	0.5	0.726
0.6	0.4	0.783
0.7	0.3	0.848
0.8	0.2	0.921
0.9	0.1	1.006
1.0	0	1.104

TABLE 4.1-8 SUMMARIZED DATA FOR ENVIRONMENTAL FACTOR DEVELOPMENT

ENVIRONMENT	PWB hrs. x 10^6	$\overline{N}$	pth hrs. x 10^6	$\overline{\ell}$	FAILURES
GB	11.985	928	11,119.474	6.0	1
GF	809.821	347	281,063.865	3.1	22
NSB	3.851	341	1,312.689	3.1	0
GM	30.420	142	4,309.500	2.0	1
AIT	2.481	222	550.725	6.0	0
AIF	3.223	222	715.561	6.0	0
AUT	43.614	555	24,192.196	6.2	23
AUF	40.761	555	22,609.550	6.2	33
ARW	1.221	555	677.306	6.2	1

Differences in the equation for observed environmental factor and the proposed printed wiring assembly failure rate prediction model are the absence of the quality factor and the solder application factor. Quality factor would be assigned a valve of one for all data collected for this study because of the stringent manufacturing specifications considered. Therefore its inclusion would not affect the equation in any form. For the environmental factor discussions, it was desirable to assign a value of zero to solder application factor in all cases. A solder application factor of zero corresponds to a printed wiring assembly with a constant, average percent of rework. If the rework percentages are distributed similarly around the average value for each environment classification, then this assumption will have no adverse effects but will serve to simplify the data analysis process. Because the printed wiring assemblies are wave soldered and reworked before being exposed to a particular environment, it was believed that rework percentages are similar for each environment classification and that this assumption is an accurate one.

To compare assumed and observed environment factors, a goodness of fit test similar in form to the chi-squared test will be employed. The format of the test is:

$$gf = \Sigma \frac{w\,(\pi_{E,obs} - \pi_{E,pre})^2}{\pi_{E,pre}}$$

where

gf = goodness of fit coefficient ($gf = 0$ is a perfect fit)

w = weighting factor, see Appendix 2

$\pi_{E,obs}$ = observed environmental factors

$\pi_{E,pre}$ = assumed environmental factors

The point at which the goodness of fit coefficient is a minimum was used to quantify the optimal environment factors. The results are given in Figure 4.1-2. The optimal environmental factors occur at (A = 0.3, B = 0.7) and as a result the environmental factors can be represented by:

$$\pi_E = .3\ \pi_{E,C} + .7\ \pi_{E,PWB}$$

and are given in Table 4.1-4.

The relation described by the above equation was applied to a recently completed study which expanded the number of avionic environment categories (Avionic Environmental Factor for MIL-HDBK-217C, Contract F30602-80-C-0193). The environmental factor table given in Appendix 1, Table 5.1.13.1-4, includes environmental factors for the additional environment categories.

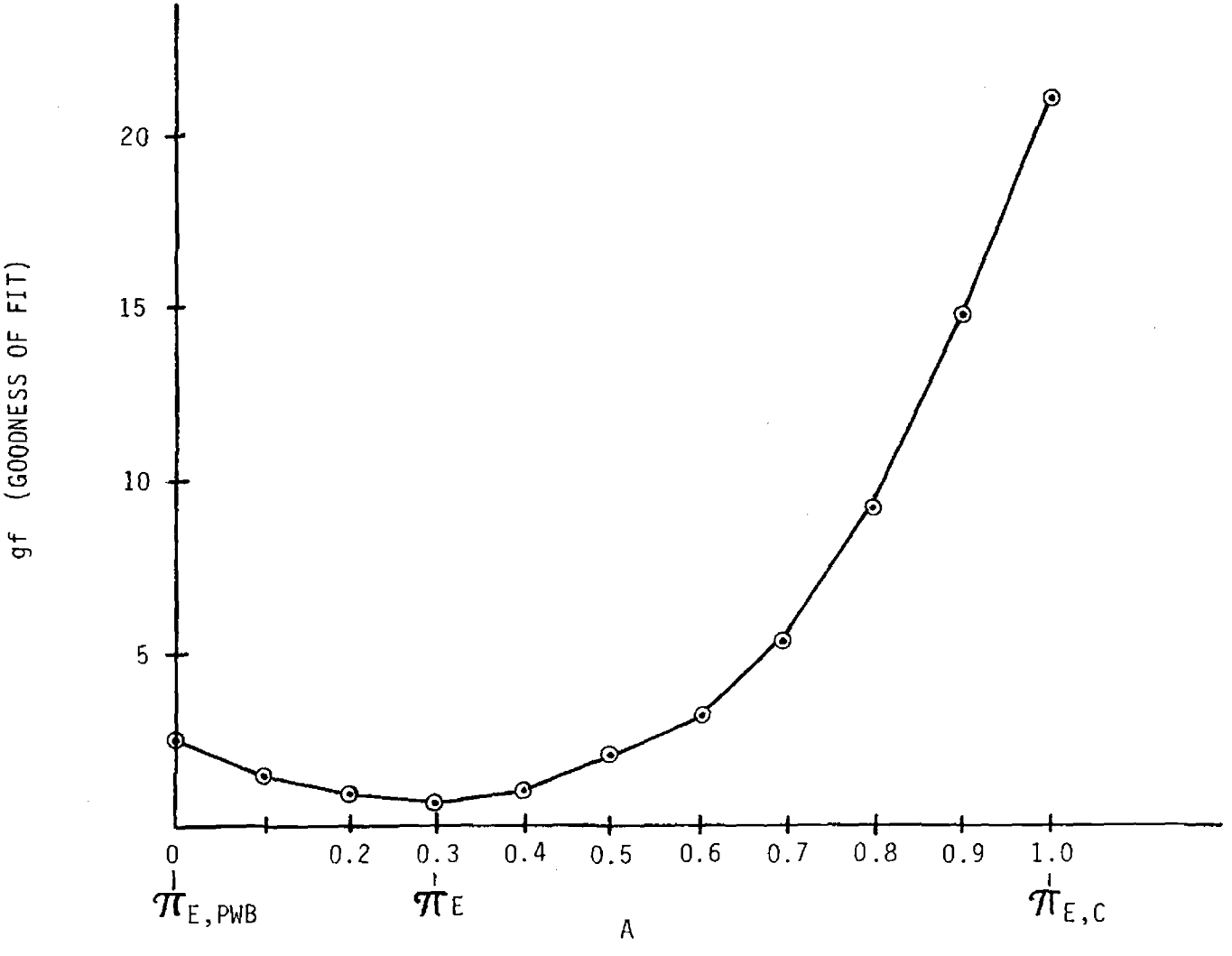
4.1.4 Complexity Factor. During the environmental factor development process, different series of environmental factors were assumed correct and then analyzed using the data base to determine goodness-of-fit. For each series of environmental factors, a unique complexity factor was derived to normalize the data. In this section, the previously derived complexity factor function corresponding to the optimal series of environmental factors is presented. Additionally, a more detailed explanation of the process used to obtain complexity factors is included.

The equation which defines complexity factor is given by:

$$\pi_C = \left(\ell/2\right)^{.63}$$

where ℓ = quantity of circuit planes.

FIGURE 4.1-2: GOODNESS OF FIT VS. ASSUMED ENVIRONMENTAL FACTORS



This equation was derived from data with complexity factor characteristics ranging from two to eight circuit planes. The data were normalized using the environmental factors given in Table 4.1-4. The assumption was made that the complexity factor remains valid for printed wiring assemblies above the range of data found in this study. This is an accurate assumption because the range of data found in this study was sufficient to determine significant trends. The results of the complexity factor development process is given in Table 4.1-1.

It is noted here that there are many parameters which pertain to printed wiring assembly complexity. The use of the term "complexity factor" to describe the effect which an increase in the number of circuit planes has on failure rate is simply a convenient notation and does not intend to imply that this is the only parameter which increases the complexity of printed wiring assemblies.

The first step towards developing a complexity factor, as defined in this study, was to determine the relation between failure rate and number of circuit planes. As a result of theoretical discussions, the conclusion can be made that failure rate is an increasing function of number of circuit planes or:

$$\lambda_p \alpha f(\ell)$$

As a prerequisite to further data analysis, the data was separated into groups, each with a unique number of circuit planes. Because the distribution of data among different environment categories is not similar for each "unique circuit plane quantity" group, all data was normalized to a uniform set of environment conditions. The data was also normalized for plated through hole quantity. An average rework percentage was assumed for each group. Applying properties of the exponential failure rate distribution, the data was normalized and consolidated by:

$$\lambda = \frac{\Sigma f}{\Sigma(TN\pi_E)}$$

where λ = normalized failure rate

Σf = total of failures in "unique circuit plane quantity" group

T = printed wiring assembly operating hours

N = quantity of plated through holes

π_E = environmental factor

TN = plated through hole operating hours

$TN\pi_E$ = TN normalized to ground, benign conditions

A normalized failure rate was calculated for each unique number of circuit planes. The data was then in a form suitable for utilization of curve fitting techniques. Different proposed functions of the number of circuit planes were attempted to fit the data. Correlation coefficients were calculated such that results of fitting different curves could be compared. Examples of several different attempts to fit curves to the data are:

$$\lambda = A\ell^B$$

$$\lambda = Ae^{B\ell}$$

$$\lambda = A\ell + B$$

where A and B = unknown constants

e = natural logrithim

Regardless of the choice of environmental factors, the optimal relation was found to be:

$$\lambda = A\ell^B$$

These curve fitting techniques result in the assumption in Section 4.1.2 that the complexity factor will take the form:

$$\pi_C = \left(\ell/2\right)^a$$

where the denominator in the above fraction is a chosen constant equal to the smallest quantity of circuit planes found in the data base.

Multiple regression analysis was performed to obtain exact values for the unknown constants (A and B) in the complexity factor equation. Because the equation is not in the form which is usually associated with regression analysis, a log transformation must be applied. The result is:

$$\lambda = A\ell^B$$
$$\ln\lambda = \ln A + B \ln\ell$$

The equation is now in a form compatible with the preliminary model for regression analysis given in Appendix 2, Applicable Statistical Techniques. To further clarify the analysis, the following substitutions were made:

$$Y = b_0 + b_1 x_1$$

where

$$Y = \ln\lambda$$
$$b_0 = \ln A$$
$$b_1 = B$$
$$x_1 = \ln\ell$$

The composition of the complexity factor is such that the unknown constant, B (or b_1), is of primary interest. This constant is equal to the exponent in the complexity factor function. The value which the A (or b_0) constant assumes is simply a normalization constant and is not essential to the complexity factor development process.

The results of the multiple regression analysis were:

$$A = .0000274$$
$$B = .627$$

The result corresponds to the complexity factor given at the beginning of this section.

Because the values for normalized failure rate depend on the choice of environmental factors, it should be clear why complexity factor also varied in the environmental factor development process. Additionally, it should be clear that environmental factor and complexity factor had to be developed simultaneously. Although they are presented in separate sections, the environmental factor and complexity factor could not have been developed independent of one another.

4.1.5 Base Failure Rate. It is the objective of this section to develop an accurate base failure rate which can be applied to all printed wiring assembly options. In Section 4.1.3, data collected in the ground, benign environment was used to estimate base failure rate. Now that an optimal series of environmental factors was derived, all data resources collected for this study were utilized to determine a more precise value for base failure rate.

In the section concerning environmental factor development, it was desirable to use the data collected in gound, benign environment for estimating a base failure rate. This was because that particular environment will assume an environmental factor of one, regardless of conclusions from the development process. A result of quantifying the optimal environmental factors was that base failure rate estimates can be obtained from any of the environment categories simply by dividing the normalized failure rate by the environmental factor. This is due to the multiplicative nature of the environmental factor. Then to obtain a base failure rate which best fits the total data resources, base failure rates calculated from each environment category were considered and an intermediate value proposed.

The previously described process begins with the general equation for wave soldered printed wiring assembly failure rate:

$$\lambda_p = \lambda_b N (\pi_C + \pi_S) \pi_Q \pi_E$$

where all parameters have been previously defined, and rearranging to solve for base failure rate (λ_b):

$$\lambda_b = \frac{1}{\pi_E} \left[\frac{\lambda_p}{N \pi_Q} \frac{1}{\pi_C + \pi_S} \right]$$

Quality factor (π_Q) and solder application factor (π_S) are again allowed to assume values of one and zero respectively without introducing biases. The base failure rate can, therefore, be expressed as:

$$\lambda_b = \frac{1}{\pi_E} \left[\frac{\lambda_p}{N \pi_C} \right]$$

Base failure rates calculated from the data are given in Table 4.1-9. Single-sided 60% confidence limits are used to approximate base failure rate point estimates in cases where no failures were observed. These points are marked with an asterisk.

TABLE 4.1-9 BASE FAILURE RATES VS. ENVIRONMENT

ENVIRONMENT	$\lambda_{b,.05}$	$\hat{\lambda}_b$	$\lambda_{b,.95}$
GB	.000002	.000045	.000214
GF	.000017	.000026	.000037
MSB	---	.000129*	.000425
GM	.000002	.000030	.000142
AIT	---	.000219*	.000716
AIF	---	.000083*	.000271
AUT	.000036	.000053	.000075
AUF	.000033	.000045	.000060
ARW	.000002	.000038	.000180

* Zero failure case, upper 60% confidence limit used to approximate point estimate.

Large deviations from an average value are only observed in zero failure cases and are not meaningful deviations.

A weighted average of the values given in Table 4.1-9 was used to derive a final numerical quantity for base failure rate. The values were weighted such that environments with relatively more observed failures receive greater influence. The quantity of recorded failures is the best indication of precision in failure rate point estimates. Environments with no recorded failures were not included in the calculations for base failure rate because a 60% upper confidence limit value is only meaningful if it provides a relatively lower failure rate and this was not the case. A discussion of the weighting factor which was used is included in Appendix 2.

The calculated optimal base failure rate is:

λ_b = 0.00041 failures/10^6 hrs.

This value isn't significantly different than the base failure rate value obtained using just ground, benign data. Therefore, no inaccuracies were introduced in the previous section when ground, benign environment data was used solely to estimate base failure rate.

4.1.6 Solder Application Factor. For wave soldered printed wiring assemblies, the solder application factor has been defined as an increasing linear function. The factor will increase with the percentage of connections reworked after wave soldering. The rework percentage is an important parameter because it provides an indication of several solder related problems. A high rework percentage can represent poor solderability of component leads or a poorly designed circuit. Perhaps more important, a reworked solder connection will inherently have a higher failure rate due to the variability of direct human involvement. This section will present the proposed solder application factors and the corresponding procedure followed for wave soldered and hand soldered printed wiring assemblies.

The solder application factor for wave soldered assemblies was derived by transforming the failure rate prediction model to solve for solder application factor,

$$\pi_S = \frac{\lambda_p}{N} \frac{1}{\lambda_b \pi_Q \pi_E} - \pi_C$$

Using data sources which contain at least one failure, the observed (or calculated) solder application factors are listed in increasing order in Table 4.1-10 and presented in histogram form in Figure 4.1-3. Zero failure cases were not included because of the questionable precision in calculating failure rates without observed failures. It was desirable to locate the minimum and maximum observed solder application factor, but first the validity of each point was considered. The negative values correspond to printed wiring assemblies where the rework percentage is less than the constant, average value. This can be confirmed by returning to the definition of solder application factor in Section 4.1.2. There was concern, however, about the two largest values for solder application factor. These two values appear to be divergent from all remaining values.

TABLE 4.1-10 OBSERVED SOLDER APPLICATION FACTORS

NUMBER	π_S
1	-0.8
2	-0.3
3	-0.2
4	0.1
5	0.2
6	0.5
7	1.0
8	1.2
9	1.4
10	1.4
11	2.2
12	5.4
13	23.5

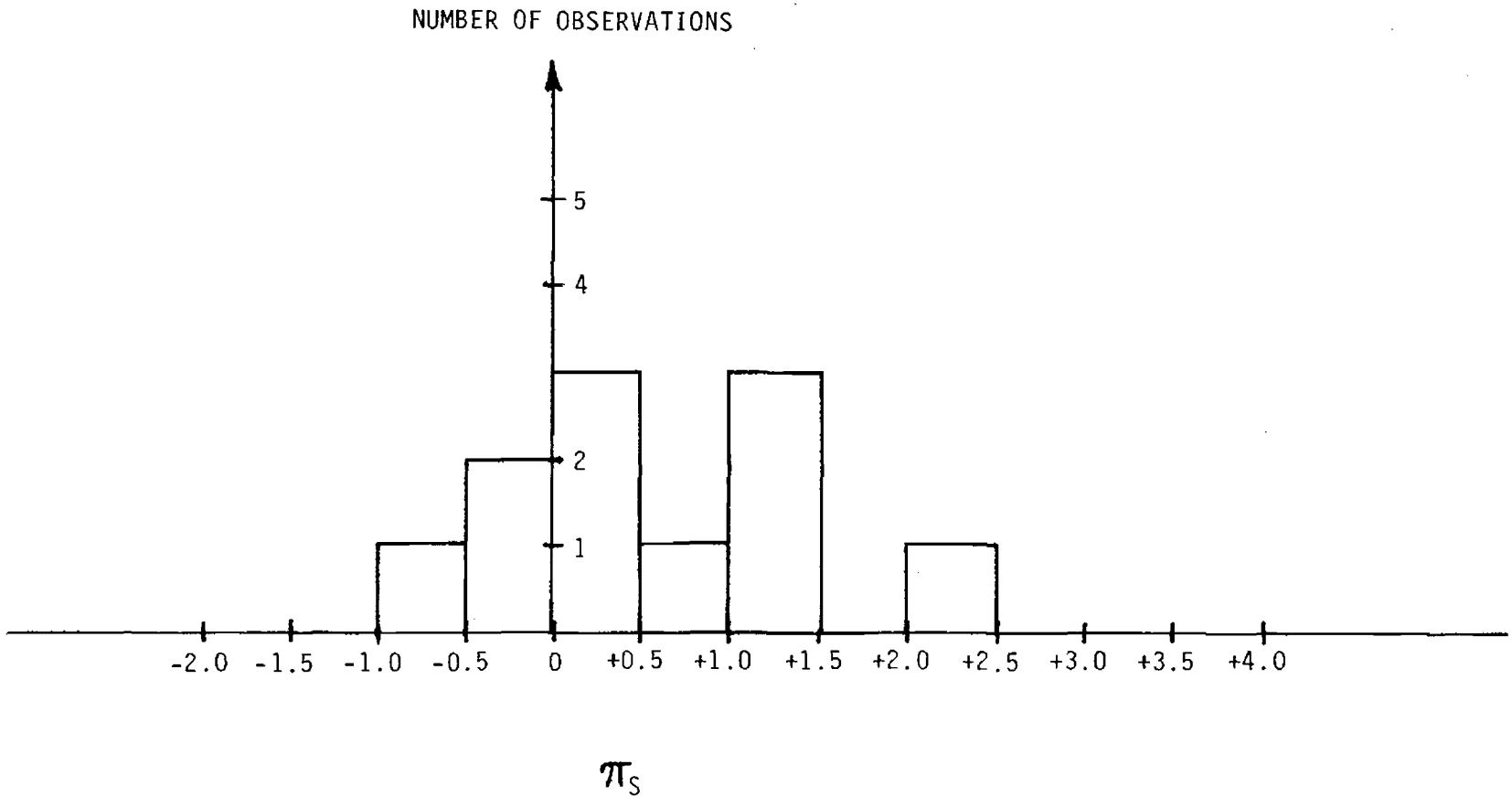


FIGURE 4.1-3: SOLDER APPLICATION FACTOR DENSITY HISTOGRAM

The Dixon Criterion was utilized to consider whether these two data points were outliers. Results of the test imply that both points are indeed significantly divergent from the remainder. A brief explanation of the Dixon Criterion is included in Appendix 2. The conclusion is that these two points are either natural outliers, or the result of poor data recording practices or they represent the inability of the environmental factor to represent all possible missions within an environment classification. Therefore, these two points were not included in further development and the minimum and maximum was considered to be -0.8 and 2.2, respectively.

The solder application factor and each parameter was defined as:

$$\pi_S = \frac{1}{\lambda_b}\left[(\lambda_{rw} - \lambda_o)(x - \bar{x})\right]$$

in Section 4.1.2.

Every term in the solder application factor equation is a constant except for x, the rework percentage. The equation was arranged to the more familiar linear form:

$$\pi_S = \left[\frac{1}{\lambda_b}(\lambda_{rw} - \lambda_o)\right] x - \left[\frac{1}{\lambda_b}(\lambda_{rw} - \lambda_o)\,\bar{x}\right]$$

$$\pi_S = Ax - B$$

If each constant in the solder application factor expression were known or if the rework percentages corresponding to each observed solder application factor were available, then best fit values for A and B could have been found and the solder application factor development process concluded. Unfortunately, neither condition existed and an alternate procedure was developed.

To compensate for the shortcomings in the data base, a solder rework survey was conducted. Participants in the survey were manufacturers of military or similar quality, commercial equipment. The manufacturers were

asked to supply a typical value (not average value) of solder rework percentage for their wave soldered printed wiring assemblies. The results are shown graphically on a Weibull probability plot in Figure 4.1-4. Each data point represents a survey participants rework percentage reply. The best fit line through the data points corresponds to a cumulative distribution function as follows:

$$F(x) = 1 - \exp\left\{-(x/.085)^{1.24}\right\}$$

where

x = rework precentage

To insure that the resulting function represents the data points adequately, the Kolmogorov-Smirnov goodness of fit test was performed. Results from the test revealed that deviations from predicted values were not significant and therefore the fit is adequate. It was noted, however, that the largest deviations occur at the lower tail of the curve (rework percentages less than 3%). This is not considered unusual for Weibull plots. For further clarification of the results of the survey, the cumulative distribution function and the density function are presented graphically using a linear scale in Figures 4.1-5 and 4.1-6, respectively.

The rationale behind the solder rework survey and subsequent analysis was that expected maximum and minimum values for rework percentages could be found for the number of data sources in the data base. The assumption was made that the manufacturers of the printed wiring assemblies represented in the data base and the participants in the solder rework survey have similar distributions of rework percentage. Thus, the maximum and minimum values for rework percentage could be aligned with the maximum and minimum values for solder application factor and the unknown constants in the expression for wave soldered, solder application factor were determined.

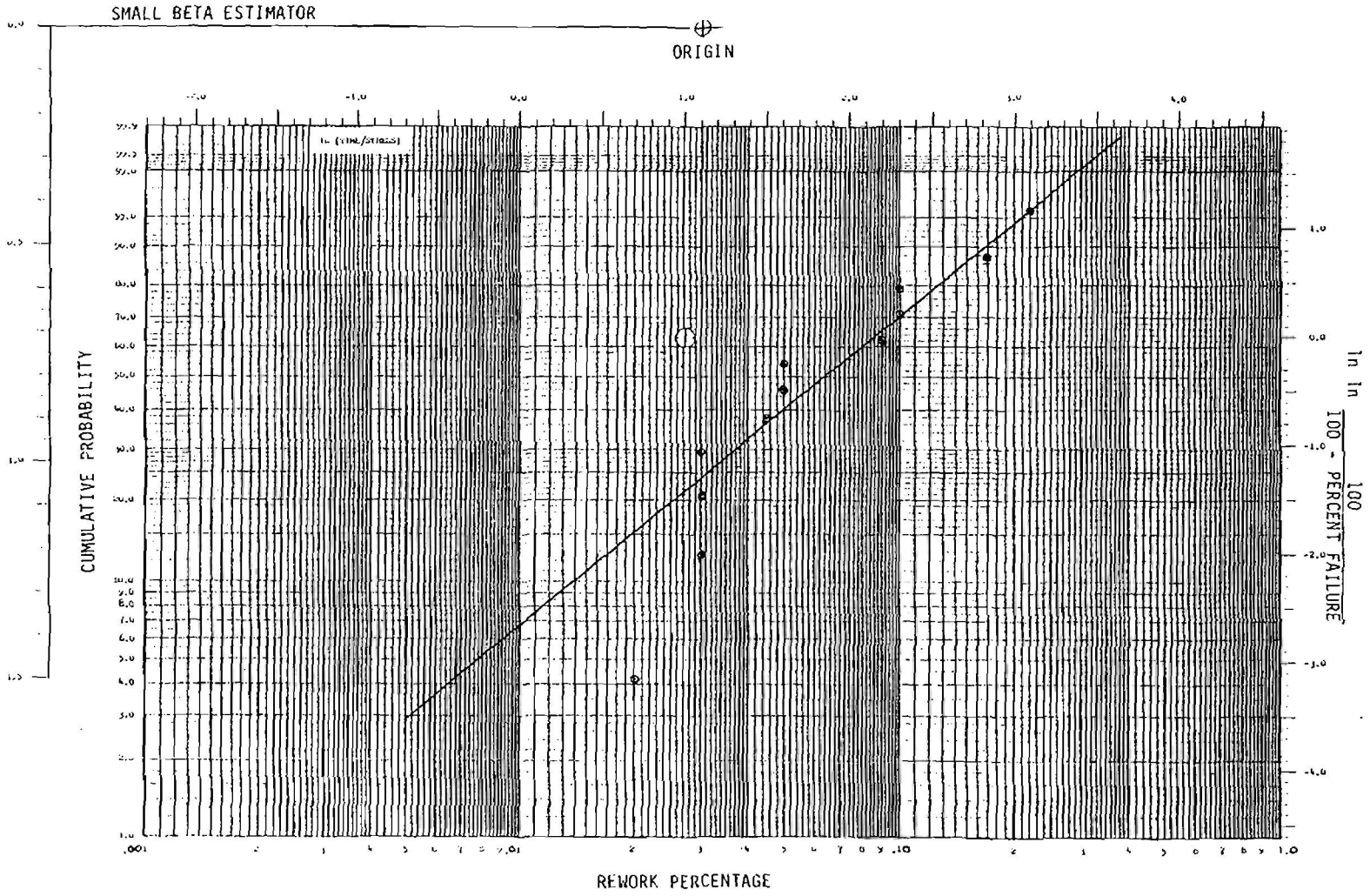


FIGURE 4.1-4: WEIBULL CUMULATIVE DISTRIBUTION FUNCTION FOR SOLDER REWORK PERCENTAGES

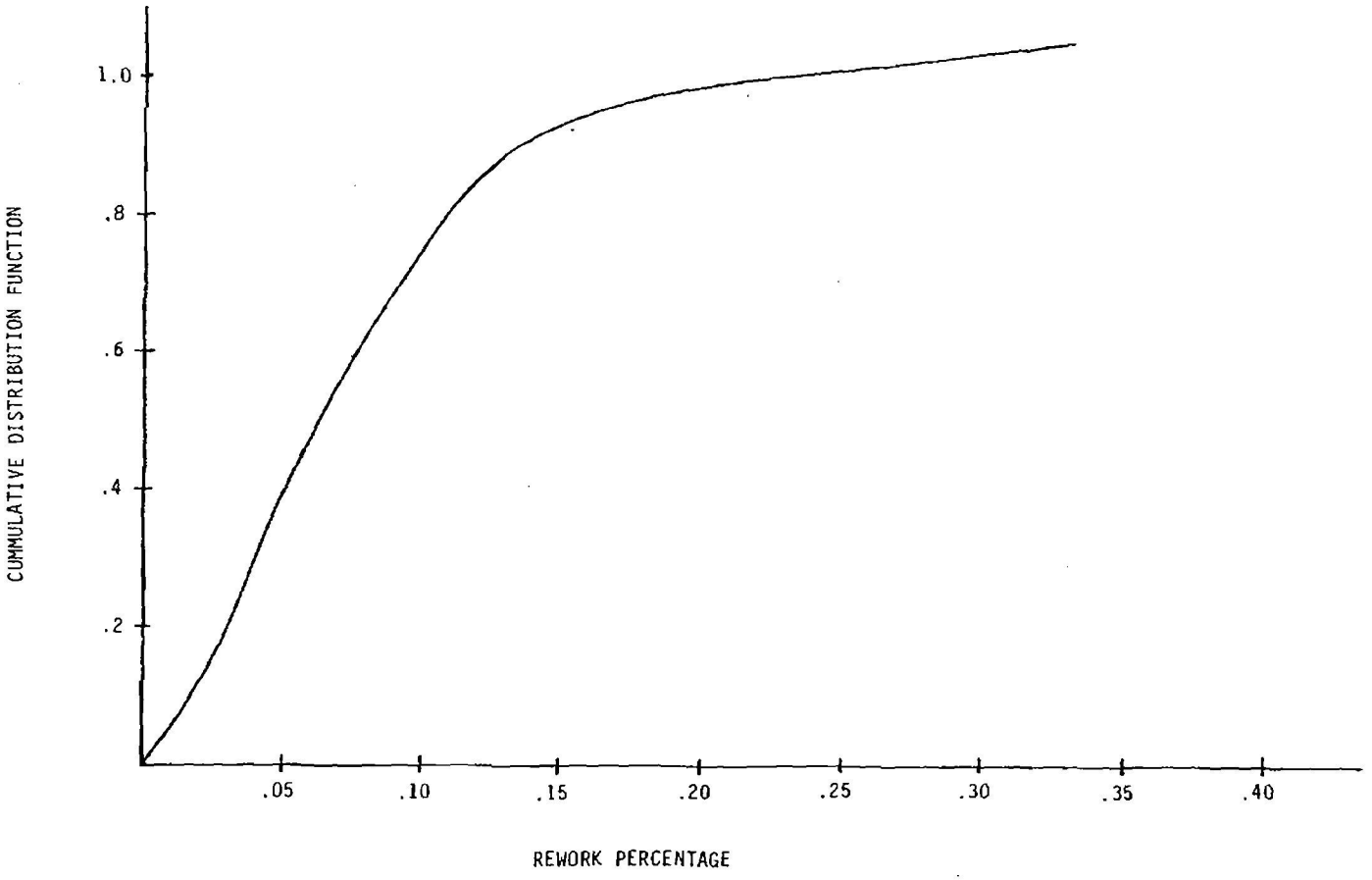


FIGURE 4.1-5: REWORK PERCENTAGE CUMMULATIVE DISTRIBUTION FUNCTION

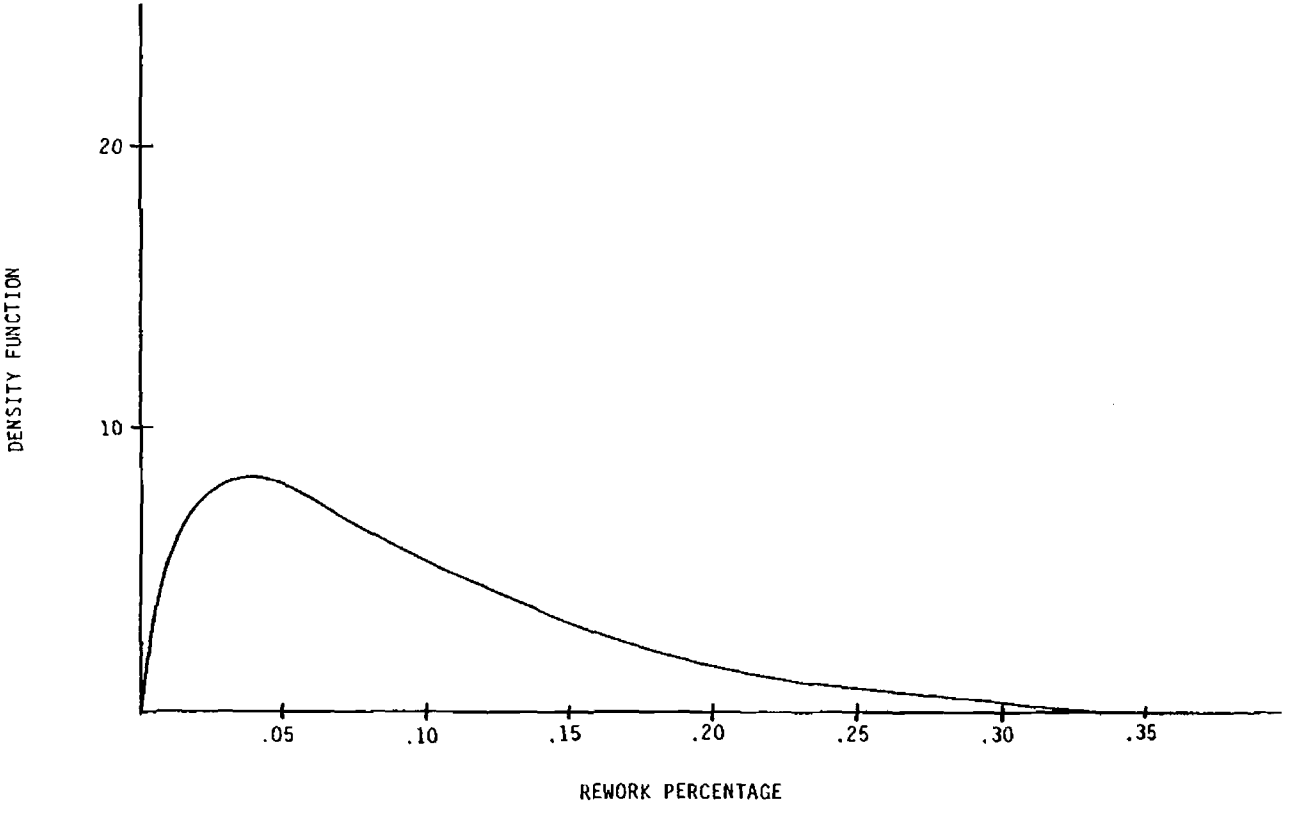


FIGURE 4.1-6: REWORK PERCENTAGE DENSITY FUNCTION

The cumulative distribution function was reexamined to find the expected minimum and maximum values for rework percentage corresponding to the number of sources (thirteen) in the data base. The expected cumulative distribution value can be found for any point by the equation:

$$F(x) = \frac{i - \frac{1}{2}}{n}$$

where i = rank of interested data point ($1 \leq i \leq n$)

n = total quantity of data points

Because the minimum and maximum points are of primary interest, values for $i = 1$ and 13 were entered into the above equation. The variable n assumed a value of 13 for each case. The results are:

$$F_1(x) = 0.038$$
$$F_{13}(x) = 0.962$$

The cumulative distribution function was transformed into an equation for x and the values for $F_1(x)$ and $F_{13}(x)$ substituted to obtain the minimum and maximum rework percentages. The equation for x is:

$$x = .085 \left[(-\ln (1 - F(x)))^{\frac{1}{1.24}} \right]$$

and the results were:

$$x_{min} = .006 \text{ reworks/connection}$$
$$x_{max} = .220 \text{ reworks/connection}$$

These results were aligned with the minimum and maximum solder application factor values (-0.8, 2.2) to solve for the unknowns in the solder application factor equation. This was done by:

$$\pi_S = Ax - B$$

where

$$A = \left(\frac{2.2 + 0.8}{.220 - .006} \right) = 14.0$$

$$B = (14.0)\ (.220) - 2.2 = 0.88$$

and

$$\pi_S = 14.0x - 0.88$$

There was concern that the poorest fit in Figure 4.1-4 was at the lower tail of the curve. The small rework percentages at the lower tail of the curve would result in the lowest failure rate predictions. Therefore, in order to be slightly conservative while still maintaining prediction accuracy, the proposed solder application factor takes the following form for wave soldering:

$$\pi_S = 0, \qquad x \leq 0.06$$

$$\pi_S = 14.0x - 0.88, \quad x > 0.06$$

The cutoff point of 0.06 for rework percentage corresponded to the point where solder application factor equals zero. This is the optimal form for wave soldered, solder application factor and is presented in Section 4.1.1, Table 4.1-2.

The hand soldering operation is essential to printed wiring assembly manufacturing. Printed wiring assemblies can be 100% hand soldered. There are also heat sensitive and open parts (switches, relays, etc.) that are not mounted on the printed wiring assembly during the automatic soldering process. The PTHs for these devices are masked during the soldering operation and the parts are hand soldered in later. Therefore, a solder application factor for hand soldering was developed.

Efforts to obtain data on hand soldered printed wiring assemblies proved futile. In general, hand soldered printed wiring assemblies are manufactured in low quantities and therefore sufficient operating hours could not be accumulated. One option available was to consider the existing base failure rate for hand solder connections (.0026 failures/10^6 hours). This option was rejected, however, because the hand soldered connection base failure rate is primarily intended for wire-to-wire or wire-to-terminal post connections and not for a plated through hole, hand soldered connection. Additionally, the base failure rate for hand soldered connections is not an intuitively satisfactory value. Therefore, an alternate plan was devised.

The alternate plan was based on the variability in hand soldering caused by human involvement at every connection. The variability of human involvement in the hand soldering operation is identical to a wave soldered printed wiring assembly that is totally (100%) reworked. Therefore the assumption made was that the hand soldered, solder application factor can be approximated by the equation developed for wave soldering with a solder rework value of 1 (100%). It is emphasized that reworked wave soldered connections and hand soldered connections are different. But because of the identical variability introduced by the complete human involvement and lack of supporting data, this is the best available methodology. If data corresponding to hand soldered plated through hole connections becomes available, the derived value can be checked for validity. Substituting a value of one into the equation for wave soldered, solder application factor, the result was:

$$\pi_S = 14.0 - 0.88 = 13.1$$

This is the proposed value presented in Table 4.1-2.

4.1.7 Quality Factor. Based on theoretical discussions and analysis of manufacturing specifications, it was strongly felt that the failure rate of printed wiring assemblies would depend on the quality standards followed by the manufacturers. This section presents the proposed quality factors and the corresponding methodology used. The quality factor is multiplicative in form and is given in Table 4.1-3.

Theoretical analysis revealed that many different manufacturing options have an effect on reliability. Several examples are (1) the use of a preheat stage before wave soldering to prevent excessive plated through hole degradation, (2) different available cleaning techniques to remove flux residues, and (3) controls imposed upon both drilling and etching operations to insure plating quality. These examples are provided merely as a sampling of the many manufacturing variables which are believed to have an impact on reliability. Manufacturers decide on particular specifications for various reasons. Equipments with lower intended lifetimes or equipments where printed wiring assembly failures are not considered critical may be manufactured to less stringent specifications. These differences will be manifested in the failure rates and should be considered in printed wiring assembly prediction models.

An initial attempt was made to divide the data into two unique groups: (1) printed wiring assemblies manufacturered to MIL-SPEC and (2) printed wiring assemblies not manufacturered to MIL-SPEC. Base failure rates were calculated for each unique group of data. Results are presented in Table 4.1-11. Point estimates, along with upper and lower 90% confidence limits are given in the table. Analysis of the results reveal that no significant conclusions can be made from the data and that a quality factor based on this type of reasoning would not appear to have any significance.

TABLE 4.1-11: BASE FAILURE RATES VS. QUALITY GRADE

Quality Grade	$\lambda_{b,.05}$	$\hat{\lambda}_b$	$\lambda_{b,.95}$
MIL-SPEC	.000034	.000041	.000049
Commercial	.000006	.000036	.000113

The assumption that failure rate depends on quality standards was reanalyzed. Analysis revealed that the commercial grade printed wiring assemblies which were included in the data base were manufactured to high industrial standards, comparable to MIL-SPEC standards. Therefore, for the remainder of the quality factor development process, MIL-SPEC and comparable industrial standards were considered equivalent. Further analysis revealed that printed wiring assemblies manufactured to relatively lower standards of quality, such as those found in portable tape recorders, copy machines and electronic games were not closely monitored to determine operating hours or particular failed components. Therefore, data for these types of assemblies could not be obtained.

Because the type of data desired to determine a precise quality factor was unavailable, the assumption that quality standards influence failure rate could not be rejected and was still considered valid. Previous reliability studies were investigated to obtain optimal values for quality factor. A quality factor of one was assigned to printed wiring assemblies manufacturered to MIL-SPEC or comparable industrial (IPC) standards. Based on previous reliability studies such as RADC-TR-78-15, Crimp Connection Reliability, a value of ten was assigned to any printed wiring assemblies manufactured to less than MIL-SPEC or comparable industrial (IPC) standards.

4.2 Reflow Soldered Assemblies.

4.2.1 Proposed Failure Rate Prediction Model. This section presents the proposed failure rate prediction model for reflow soldered printed wiring assemblies. The model represents the results of analysis performed on the data base developed for this study. The proposed failure rate prediction model for reflow soldered assemblies is:

$$\lambda_{rsa} = .000069\ N\ \pi_E \text{ failures}/10^6 \text{ hrs.}$$

where

N = quantity of reflow soldered connections

π_E = environmental factor, Table 4.2-1

TABLE 4.2-1: ENVIRONMENTAL FACTOR

ENVIRONMENT	π_E	ENVIRONMENT	π_E
G_B	1	A_{IA}	7.5
G_F	2.1	A_{IF}	5
G_M	7.3	A_{UC}	2
M_P	7.3	A_{UT}	7.5
		A_{UB}	6
N_{SB}	3.5	A_{UA}	9.5
N_S	4.4	A_{UF}	7
N_U	9.9		
N_H	11	S_F	1
N_{UU}	12	M_{FF}	7.3
		M_{FA}	10
A_{RW}	16	U_{SL}	22
A_{IC}	1.5	M_L	25
A_{IT}	5.5	C_L	420
A_{IB}	4.5		

4.2.2 Model Development Procedure. The procedure followed to obtain the proposed failure rate prediction model for reflow soldered assemblies is included in this section. Assumptions based on theoretical discussions and/or data analysis are noted as they occur in the prediction model development process.

Reflow soldered assemblies generally consist of a single or double sided printed wiring board with reflow soldered connections to the leads of flatpack packaged components. Several reliability related advantages are

offered by this type of interconnection assembly, most notably the absence of plated through holes. Variables which do, however, effect the reliability of reflow soldered assemblies are given in Table 4.2-2.

TABLE 4.2-2: FACTORS INFLUENCING REFLOW SOLDERED ASSEMBLY FAILURE RATE

- o Construction Details and Process Controls
  - Number of solder connections
  - Presence of gold-tin-lead intermetallics
  - Human induced variance in time-temperature-pressure profile
  - Solderability of surfaces
  - Conformal coating, if any
  - Moisture content of printed wiring boards
  - Foil weight
- o Environmental Stresses
  - Effect of temperature cycling
  - Effect of thermal shock
  - Effect of humidity
  - Effect of random vibration
  - Effect of sine vibration
  - Effect of mechanical shock

Based on theoretical discussions, the dominant failure mechanisms for reflow soldered assemblies are associated with the interface between the solder and the printed wiring board and the interface between the solder and the component lead. Another area where potential failure mechanisms exist is the interface between the copper pad and the epoxy glass substrate. In each case, potential failures are concentrated at an individual connection. Therefore it follows that the reflow soldered assembly failure rate is proportional to the total quantity of solder connections.

It was also evident from the theoretical analysis, that the frequency of reflow soldered assembly failure mechanisms increases when exposed to thermal cycling or thermal shock. Therefore, an appropriate series of environmental factors were designated to represent the net effect on failure rate of the combined environmental stresses. The reflow soldered assembly data collected in support of this study effort came from equipments operating in either the satellite or ground, fixed environments. This is not unusual because the use of reflow soldered technology is primarily concentrated in satellite applications. As a result, no empirical means of developing environmental factors was available. The existing environmental factors as presented in RADC-TR-80-229, Revision of Environmental Factors for MIL-HDBK-217B, were assumed correct.

The assumptions discussed in the several preceding paragraphs were used to develop the following reflow soldered assembly failure rate prediction model:

$$\lambda_{rsa} = \lambda_b N \pi_E$$

where

λ_b = base failure rate
N = quantity of solder connections
π_E = environmental factor, Table 4.2-1

The base failure rate represents the sum of failure rate contributions from each failure mechanism for an individual connection.

A numerical quantity for base failure rate was obtained from the data base. Table 4.2-3 presents the reduced data for reflow soldered assemblies. The table lists connection hours and failures for each environment classification. The data was collected in connection hours because of the assumption that assembly failure rate is proportional to the total number of connections.

TABLE 4.2-3: REFLOW SOLDERED ASSEMBLY DATA

ENVIRONMENT	CONNECTIONS HRS. (x 10^6)	FAILURES
SAT	39,610.000	0
GF	8,835.115	4

The base failure rate was derived from the data by:

$$\lambda_b = \frac{\Sigma f}{\Sigma(T_{rf}{}^N \pi_E)}$$

where

Σf = total of observed failures

$T_{rf}{}^N$ = reflow soldered connection operating hours

π_E = environmental factor, Table 4.2-1

Substituting values from the data base

$$\lambda_b = \frac{4 \text{ failures}}{58{,}163.742 \times 10^6 \text{ hrs.}}$$

$$= .000069 \text{ failures}/10^6 \text{ hrs.}$$

This value is not significantly different from the existing base failure rate for reflow soldered connections (.00008 failures/10^6 hrs). However, the calculated base failure rate is proposed to replace the existing value because the proposed base failure rate was obtained by observing reflow soldered assemblies in operating conditions. The previous base failure rate was derived using accelerated testing techniques. Therefore, the reflow soldered assembly failure rate prediction model becomes:

$$\lambda_p = .000069\ N\ \pi_E \text{ failures}/10^6 \text{ hrs.}$$

This model was transformed into a more general form, such that a single prediction model can be used for several manufacturing technologies. The more general form is:

$$\lambda_p = \pi_E \sum (\lambda_{bi} N_i)$$

where one value for λ_{bi} corresponds to reflow soldered technology. This general format will also account for reflow soldered assemblies which might also utilize alternate interconnection technologies.

4.3 Solderless Wrap Assemblies

4.3.1 Proposed Failure Rate Prediction Model. This section presents the proposed prediction model for solderless wrap assemblies. This recommended addition to the existing MIL-HDBK-217C models is the result of the analysis performed on the data base compiled during this study. The failure rate prediction model for solderless wrap assemblies is:

$$\lambda_{wwa} = (.0000035N_1 + .000069N_2)\ \pi_E \text{ failures}/10^6 \text{ hours}$$

where

N_1 = quantity of wraps

N_2 = quantity of reflow soldered connections

π_E = environmental factor, Table 4.2-1

4.3.2 Model Development Procedure. The methodology used to extract an accurate and useful failure rate prediction model pertaining to solderless wrap assemblies is included in this section. Assumptions based on theoretical discussions and/or data analysis are noted as they occur in the prediction model development process.

A theoretical investigation was performed to study the reliability characteristics of solderless wrap assemblies. Variables believed to effect reliability are presented in Table 4.3-1.

TABLE 4.3-1: FACTORS INFLUENCING SOLDERLESS WRAP ASSEMBLY FAILURE RATE

- o Construction Details and Process Controls
  - Number of wraps
  - Relaxation of spring constant
  - Hardness of copper
  - Tool calibration
  - Cold flow properties of insulation
  - Wire gauge
  - Insulation stripping controls
- o Environmental Stresses
  - Effect of temperature cycling
  - Effect of thermal shock
  - Effect of humidity
  - Effect of random vibration
  - Effect of sine vibration
  - Effect of mechanical shock

It was assumed that the only failure mechanisms pertaining to solderless wrap assemblies which significantly effect failure rate are those which are associated with the wraps and the solder connections. Solder connections are used in solderless wrap assemblies to electrically connect circuits to power and ground planes. If the solderless wrap assembly construction doesn't include power and ground planes, then the wraps were assumed the only significant contributor to assembly failure rate.

Similar to the argument concerning printed wiring assemblies, it was assumed that a multiplicative environmental factor (π_E) can be used to express the failure rate contribution resulting from all environmental stresses. Solderless wraps and solder connections are both currently classified in MIL-HDBK-217C as "connections". It was necessary to assume that the existing connection environmental factors are accurate because there was insufficient data to develop updated environmental factors or to provide a true verification of the existing environmental factors. There is however, failure rate data in four different environments which do not reveal any inadequacies in the existing factors.

It was assumed that failure rate contributions of the wraps and the solder connections are independent of one another. Additionally, it was assumed that each individual wrap has an equal failure rate for a given environment. Similarly, each solder connection has an equal failure rate. If the assumptions discussed above are applied, the solderless wrap assembly failure rate prediction model takes the following form:

$$\lambda_{wwa} = (\lambda_{ww} N_1 + \lambda_{SC} N_2)\ \pi_E$$

λ_{ww} = individual wrap failure rate

N_1 = quantity of wraps

λ_{SC} = solder connection failure rate

N_2 = quantity of solder connections

π_E = environmental factor

According to properties of the exponential failure rate distribution, the observed failure rate for individual wraps can be obtained from the data by:

$$\lambda_{ww} = \frac{\Sigma f}{\Sigma(T_{ww}\pi_E)}$$

where

Σf = total number of observed failures
T_{ww} = wrap operating hours
$T_{ww}\pi_E$ = normalized wrap operating hours

The summarized data for solderless wrap assemblies is given in Table 4.3-2. Operating environment, connection operating hours and observed failures are presented in the table.

TABLE 4.3-2: SOLDERLESS WRAP ASSEMBLY DATA

ENVIRONMENT	CONNECTIONS HRS. (x 10^6)	FAILURES
GF	3,500.000	0
NSB	325,000.000	4
AIT	7.965	0
AUT	448.140	0

Substituting values from the data base in the equation for individual wrap failure rate results in:

$$\lambda_{ww} = \frac{4 \text{ failures}}{1.14 \times 10^{12} \text{ ww hrs}}$$

$$_{ww} = .0000035 \text{ failures}/10^6 \text{ hours}$$

Due to the proximity of this value to the existing solderless wrap base failure rate of .0000025 failures/10^6 hrs., there is no significant difference between the two values. However, the calculated solderless wrap

assembly base failure rate will be proposed to replace the existing solderless wrap failure rate because the data used in this study represents relatively more current data sources.

The base failure rate for solder connections as used in solderless wrap assemblies was assumed equal to the base failure rate developed for reflow solder connections in Section 4.2. The base failure rate for reflow solder connections is .000069 failure/10^6 hrs.

Substituting the base failure rates for wraps and solder connections into the general solderless wrap assembly failure rate prediction model, the model takes the following form:

$$\lambda_{wwa} = (.0000035N_1 + .000069N_2)\ \pi_E \text{ failures}/10^6 \text{ hrs.}$$

where all parameters have been previously defined.

The model was transformed into a more general form such that a single failure rate prediction model could be used for several different interconnection assemblies. Additionally, the general form of the model accounts for designs which consist of a combination of technologies. The general form is:

$$\lambda_p = \pi_E \sum (\lambda_{bi} N_i)$$

where parameter choices for λ_{bi} are equal to solderless wrap and reflow soldered base failure rates.

4.4 Wrapped and Soldered Assemblies.

4.4.1 Proposed Failure Rate Prediction Model. This section presents the proposed failure rate prediction model for wrapped and soldered assemblies. This model represents the conclusions made from the data

analysis process. The failure rate prediction model for wrapped and soldered assemblies is:

$$\lambda_{wsa} = (.00014\ N_1 + .000069\ N_2)\ \pi_E \text{ failures}/10^6 \text{ hrs.}$$

where

N_1 = quantity of wraps

N_2 = quantity of reflow soldered connections

π_E = environmental factor, Table 4.2-1

4.4.2 Model Development Procedure. A methodology to develop an accurate and useful failure rate prediction model for wrapped and soldered assemblies was derived. The detailed procedure followed is presented in this section.

A theoretical investigation was performed to study reliability characteristics of wrapped and soldered assemblies. Variables believed to effect reliability are presented in Table 4.4-1.

The manufacturing process involved in wrapped and soldered assemblies is comparatively recent and extensive field failure rate data resources have not yet been accumulated. The optimal form for a wrapped and soldered assembly failure rate prediction model could not be determined from the limited data base. Therefore, physical similarities between wrapped and soldered, and solderless wrap were analyzed and used to supplement the available data.

The use of wrap as an interconnection method is a common denominator between wrapped and soldered, and solderless wrap assemblies. For each technology, the quantity of wraps is of primary importance in determining reliability. The general relation between failure rate and quantity of

TABLE 4.4-1: FACTORS INFLUENCING WRAPPED AND SOLDERED ASSEMBLY FAILURE RATE

- o Construction Details and Process Controls
  - Number of wraps
  - Tool calibration
  - Solderability of surfaces
  - Incomplete removal of insulation at connection
  - Wire gauge
  - Insulation material
- o Environmental Stresses
  - Effect of temperature cycling
  - Effect of thermal shock
  - Effect of humidity
  - Effect of random vibration
  - Effect of sine vibration
  - Effect of mechanical shock

wraps was assumed the same for wrapped and soldered, and solderless wrap assemblies. This served to simplify the model development process by lessening the dependence on an incomplete data base. This assumption, together with a wrapped and soldered base failure rate derived from the available data formed the basis for the wrapped and soldered failure rate prediction model.

The proposed general equation for wrapped and soldered assemblies is:

$$\lambda_{wsa} = (\lambda_{ws} N_1 + \lambda_{sc} N_2) \pi_E \text{ failures}/10^6 \text{ hrs.}$$

where

λ_{WS} = individual wrap failure rate

N_1 = quantity of wraps

λ_{SC} = reflow soldered connection failure rate
= .000069 failures/10^6 hrs., from Section 4.2

N_2 = quantity of solder connections

π_E = environmental factor, Table 4.2-1

This model for wrapped and soldered assemblies is intuitively correct. Based on analysis of construction details, any solder connections utilized on a wrapped and soldered assembly to electrically connect to power or ground planes, are independent of the wraps and should be represented in the failure rate prediction model accordingly. Additionally, the same series of environmental factors accurately predict the effects of environmental stress on solder connections and solderless wrap connections. Therefore, the same series of environmental factors theoretically would apply to wrapped and soldered assemblies.

To determine the wrapped and soldered base failure rate, the collected data was analyzed. All collected and summarized data was from systems operating in the ground, fixed environment. Table 4.4-2 presents the collected data.

TABLE 4.4-2: WRAPPED AND SOLDERED ASSEMBLY DATA

ENVIRONMENT	CONNECTION HRS. (x 10^6)	FAILURES
GF	3,056.630	0

To develop a base failure rate where no observed failures have been recorded, a one sided 60% confidence limit value was used to approximate the base failure rate. The actual method to derive the best estimate for base failure rate is:

$$\lambda_{ws} = \frac{.916}{\Sigma(T_{ws}\pi_E)}$$

where

$.916 = \frac{1}{2}\ \chi^2\ (.40,2)$, see Appendix 2

T_{ws} = quantity of wrap operating hours

π_E = environmental factor, Table 4.2-1

Substituting values from the data base

$$\lambda_{ws} = \frac{.916}{6418.923} = .00014 \text{ failures}/10^6 \text{ hrs.}$$

Substitution of this value into the proposed equation for wrapped and soldered assembly failure rate model gives:

$$\lambda_{wsa} = (.00014\ N_1 + .000069\ N_2)\ \pi_E \text{ failures}/10^6 \text{ hrs.}$$

The model was, however, transformed into a more general form such that a single prediction model could be used for several interconnection assemblies. Additionally, the general form of the model can account for designs which consist of a combination of interconnection technologies.

The general form is:

$$\lambda_p = \pi_E\ \Sigma\ (\lambda_{bi}N_i)$$

where choices for λ_{bj} are equal to wrapped and soldered, and reflow soldered base failure rate.

4.5 Clip Termination Assemblies.

4.5.1 Proposed Failure Rate Prediction Model. This section presents the proposed prediction model for clip termination assemblies. This recommended addition to the existing MIL-HDBK-217C models is the result of the analysis performed on the data base. The failure rate prediction model for clip termination assemblies is:

$$\lambda_{cta} = .00012\ N\ \pi_E \text{ failures}/10^6 \text{ hrs.}$$

where

N = quantity of connections

π_E = environmental factor, Table 4.2-1

4.5.2 Model Development Procedure. The methodology used to derive an accurate and useful failure rate prediction model pertaining to clip termination assemblies is included in this section. Assumptions based on theoretical discussions and/or data analysis are noted as they occur in the prediction model development process.

Similar to arguments concerning other technologies, it was assumed that a multiplicative environmental factor can be used to express the failure rate contribution resulting from all environmental stresses. Data for clip termination assemblies were available solely from equipments operating in the naval, sheltered environment. As a result, no empirical means of developing environmental factors was available. Because clip termination assemblies utilize a pressure contact connection analogous to

crimp connections, the assumption was made that one series of environmental factors represents the effects of environmental stress for both cases. The environmental factors for crimp connections are given in Table 4.2-1.

A theoretical investigation was performed to study the reliability characteristics of clip termination assemblies. Variables believed to effect reliability are presented in Table 4.5-1.

TABLE 4.5-1: FACTORS INFLUENCING CLIP TERMINATION ASSEMBLY FAILURE RATE

- o Construction Details and Process Controls
  - Number of connections
  - Dimensional variability
  - Relaxation of spring tension
  - Installation controls
  - Variable gas tight characteristics
- o Environmental Stresses
  - Effect of temperature cycling
  - Effect of thermal shock
  - Effect of humidity
  - Effect of random vibration
  - Effect of sine vibration
  - Effect of mechanical shock
  - Effect of atmosphere pollutants

The dominant failure mechanisms associated with clip termination assemblies relate to the actual clip termination connections. The failure rates of individual clip termination connections were assumed independent

of each other. Therefore the clip termination assembly failure rate is the sum of the individual connection failure rates. Applying this assumption and utilizing the crimp connection environmental factors results in the following equation for clip termination assembly failure rate:

$$\lambda_{cta} = \lambda_{ct}{}^{N}\pi_E$$

where

λ_{ct} = clip termination failure rate
N = quantity of connections
π_E = environmental factor, Table 4.2-1

TABLE 4.5-2: CLIP TERMINATION ASSEMBLY DATA

ENVIRONMENT	ASSY. HRS. x (10^6)	CONNECTION HRS. (x 10^6)	FAILURES
NS	16.530	1,670.368	0

The collected data was analyzed to determine the clip termination failure rate. Table 4.5-2 presents the summarized data. To develop a failure rate where no observed failures have been recorded, a one sided 60% confidence level value was utilized. The best estimate for clip termination base failure rate was derived by:

$$\lambda_{ct} = \frac{.916}{\Sigma(T_{ct}\pi_E)}$$

where

.916 = $\frac{1}{2}\ \chi^2\ (.40, 2)$, see Appendix 2

T_{ct} = clip termination operating hours

$$\lambda_{ct} = \frac{.916}{7349.619} = .00012 \text{ failures}/10^6 \text{ hrs.}$$

Therefore the clip termination assembly failure rate prediction model is:

$$\lambda_{cta} = .00012\ N\ \pi_E \text{ failures}/10^6 \text{ hrs.}$$

The model was transformed into the general form such that one prediction model can be used for several interconnection possibilities. The more general form is:

$$\lambda_p = \pi_E \sum (\lambda_{bi} N_i)$$

where for clip termination assemblies:

$$\lambda_{bi} = .00012 \text{ failures}/10^6 \text{ hrs.}$$

N_i = quantity of clip terminations

4.6 Discrete Wiring Assembly w/Electroless Deposited PTH

4.6.1 Proposed Failure Rate Prediction Model. This section presents the proposed failure rate prediction model for discrete wiring assemblies with electroless deposited plated through holes (PTH). This recommended addition to the existing MIL-HDBK-217C models is the result of analysis performed on the data base. The proposed failure rate prediction model is:

$$\lambda_{dwa} = \lambda_b \pi_E \sum [N_i (1 + \pi_{Si})]$$

where

λ_b = base failure rate = .00026 failures/10^6 hours

π_E = environmental factor, Table 4.1-4

N_1 = quantity of wave soldered plated through holes

N_2 = quantity of hand soldered plated through holes

π_{Si} = solder application factors, Table 4.1-2

4.6.2 Model Development Procedure. A methodology to develop an accurate and useful failure rate prediction model was derived for discrete wiring assemblies with electroless deposited plated through holes. The procedure included a theoretical investigation of reliability characteristics. Variables believed to effect reliability of discrete wiring assemblies w/electroless deposited PTH are presented in Table 4.6-1.

TABLE 4.6-1: FACTORS INFLUENCING DISCRETE WIRING ASSEMBLY w/ELECTROLESS DEPOSITED PTH FAILURE RATE

- o Construction Details and Process Controls
  - Number of plated through holes
  - PTH diameter
  - PTH plating thickness
  - Number of wire crossovers
  - Number of levels of circuitry
  - Homogeneity of plating at interface of wire and PTH
  - Insulation material
  - Method of solder application
  - Rework percentage after wave soldering
  - Solderability of surfaces
- o Environmental Stresses
  - Effect of temperature cycling
  - Effect of thermal shock
  - Effect of humidity
  - Effect of random vibration
  - Effect of sine vibration
  - Effect of mechanical shock

The manufacturing process involved in discrete wiring w/electroless deposited PTH is comparatively recent and extensive field failure rate data resources have not yet accumulated. The optimal form for a discrete wiring assembly w/electroless deposited PTH failure rate prediction model could not be determined from the limited data base. Therefore, physical similarities between discrete wiring w/electroless deposited PTH and printed wiring were analyzed and used to supplement the available data.

Both discrete wiring assemblies w/PTH and printed wiring assemblies have plated through holes used for interconnection purposes. Each technology utilizes a different unique plating process, but the failure rate dependence on plated through hole quantity is similar. Additionally, each technology is faced with the problem caused by the mismatch of thermal coefficients of expansion in the plated through hole. As was discussed in Section 2.2.1, stresses are caused in plated through hole assemblies when exposed to temperature extremes or temperature cycling. This is because the thermal coefficients of expansion for epoxy glass and copper are not compatible. Using this as criteria, the same series of environmental factors were used to represent the effects of environmental stress. There was not sufficient data to derive a unique series of environmental factors for discrete wiring assemblies w/electroless deposited PTH.

Another similarity between discrete wiring assemblies w/PTH and printed wiring assemblies is the available soldering options. Either type of assembly can be hand soldered or wave soldered. The solder connections on the two types of interconnection assemblies are sufficiently similar so that the solder application factor derived for printed wiring assemblies was applied to both discrete wiring w/PTH and printed wiring assemblies. The solder application factor is given in Table 4.1-2.

In general, the discrete wiring assemblies w/PTH contain one or two levels of circuitry. However, the manufacturers of plated through hole discrete wiring boards are capable of producing boards with greater than two levels of circuitry. An increase in quantity of circuitry levels would

relate to an increase in failure rate. Sufficient data to derive numerical quantities to represent this increase were not available. Therefore the proposed model is limited to predicting the failure rate of assemblies with two or less levels of circuitry. Discrete wiring assemblies w/PTH are capable of crossing circuit paths (wire crossovers) on an individual level. The need for additional levels of circuitry is not as crucial as in printed wiring assemblies where circuit paths cannot cross. Therefore, this limitation does not severely effect prediction capabilities.

The assumptions discussed in the preceding paragraphs were used to develop the following discrete wiring assembly with electroless deposited PTH failure rate prediction model:

$$\lambda_{dwa} = \lambda_b \pi_E \sum [N_i (1 + \pi_{S_i})]$$

where

λ_b = base failure rate, (failures/10^6 hrs)

π_E = environmental factor, Table 4.1-4

N_1 = quantity of wave soldered PTHs

N_2 = quantity of hand soldered PTHs

π_{S_i} = solder application factors, Table 4.1-2

A numerical quantity for base failure rate was obtained from the data base. Table 4.6-2 presents the reduced data for discrete wiring assemblies w/electroless deposited PTH. The table lists assembly hours, connection hours and observed failures per environmental classification. All collected data came from equipment operating in airborne, uninhabited transport environment. All assemblies were wave soldered.

TABLE 4.6-2: DISCRETE WIRING ASSEMBLIES w/ELECTROLESS DEPOSITED PTH DATA

ENVIRONMENT	ASSY. HRS ($\times 10^6$)	PTH HRS ($\times 10^6$)	FAILURES
A_{UT}	0.546	477.204	1

The base failure rate was derived from the data by:

$$\lambda_b = \frac{\Sigma f}{\Sigma(T_{dw}{}^N \pi_E)}$$

where

Σf = sum of observed failures

T_{dw} = assembly operating hours

$T_{dw}{}^N$ = plated through hole operating hours

π_E = environmental factor, Table 4.1-4

Substituting values from the data base:

$$\lambda_b = \frac{1 \text{ failure}}{3{,}913.073 \times 10^6 \text{ hrs.}}$$

$$= .00026 \text{ failures}/10^6 \text{ hours}$$

Substitution of this value into the proposed equation for discrete wiring assemblies w/electroless deposited PTH failure rate model gives:

$$\lambda_{dwa} = .00026\ \pi_E\ \Sigma\ [N_i(1 + \pi_{S_i})] \text{ failures}/10^6 \text{ hours}$$

where all parameters have been previously defined.

The model was, however, transformed into a more general form such that one prediction model could be used for discrete wiring assemblies w/electroless deposited PTH and printed wiring assemblies. The general form is:

$$\lambda_p = \lambda_b \pi_Q \pi_E \sum [N_i(\pi_C + \pi_{S_i})]$$

where λ_b is the base failure rate for discrete wiring w/electroless deposited PTH. Quality factor, π_Q, and complexity factor, π_C, assume a value of one for discrete wiring assemblies w/electroless deposited PTH.

5. MODEL EVALUATION

Data from several sources were received too late to be included in the model development process for printed wiring assemblies. These data were used for evaluation or validation of the proposed printed wiring assembly failure rate prediction models. Model validation demonstrates that the proposed failure rate prediction models are accurate for data points other than those used to derive the model. Since failure experience data for all technologies other than plated through hole printed wiring boards were severely limited, all the data were utilized in the model development process and no model evaluations using field data were performed.

Data from three different sources were included in the model validation process. Table 5.1 presents the validation data. Included in the table are printed wiring assembly operating hours, observed failures, failure rate point estimates, 90% confidence interval values and predicted failure rates calculated using both the proposed model and the current MIL-HDBK-217C methodology. For data entry number three; a single sided 60% confidence limit value was used to approximate the point estimate. In addition to the tabulated data, the correlation between predicted failure rate and observed failure rate for both the proposed models and the current MIL-HDBK-217C models are presented graphically in Figures 5.1 and 5.2.

TABLE 5.1: PRINTED WIRING ASSEMBLY MODEL VALIDATION DATA

Entry Number	Assy. Hrs ($\times 10^6$)	Failures	$\lambda_{.05}$	$\hat{\lambda}$	$\lambda_{.95}$	λ_p proposed models	λ_p MIL-HDBK-217C
1	96.838	9	.049	.09	.16	.06	.15
2	39.169	4	.035	.10	.23	.12	.72
3	18.480	0	--	.05*	.16	.04	.50

*Upper 60% confidence value used to approximate point estimate

Although three data sources are not sufficient to provide extensive model validation, several interesting points are introduced. Each of the three data points suggest that the proposed failure rate prediction models accurately predict the observed failure rate. Also, data entry number two consisted of multilayer printed wiring assemblies with eight to ten circuit planes. The complexity factor characteristics of this data entry exceed those included in the model development process. Therefore, the close proximity between the observed failure rate and the proposed failure rate prediction can be used as additional verification that the derived complexity factor remains accurate beyond the range included in the model development process.

All collected data pertaining to solderless wrap assemblies was included in the model development process. However, an observed solderless wrap failure rate is given in RADC-TR-69-458, RADC Nonelectronic Notebook, Index and Revision to Section 2. Since thie value was derived apart from this study, it serves certain model evaluation purposes. The observed failure rate was derived from ground environment failure rate data. In order to compare this value to the proposed solderless wrap base failure rate, it was normalized to ground, benign conditions. The normalization was done by dividing the observed failure rate by the ground, fixed environmental factor. The normalized failure rate point estimate is

NOT REPRODUCIBLE

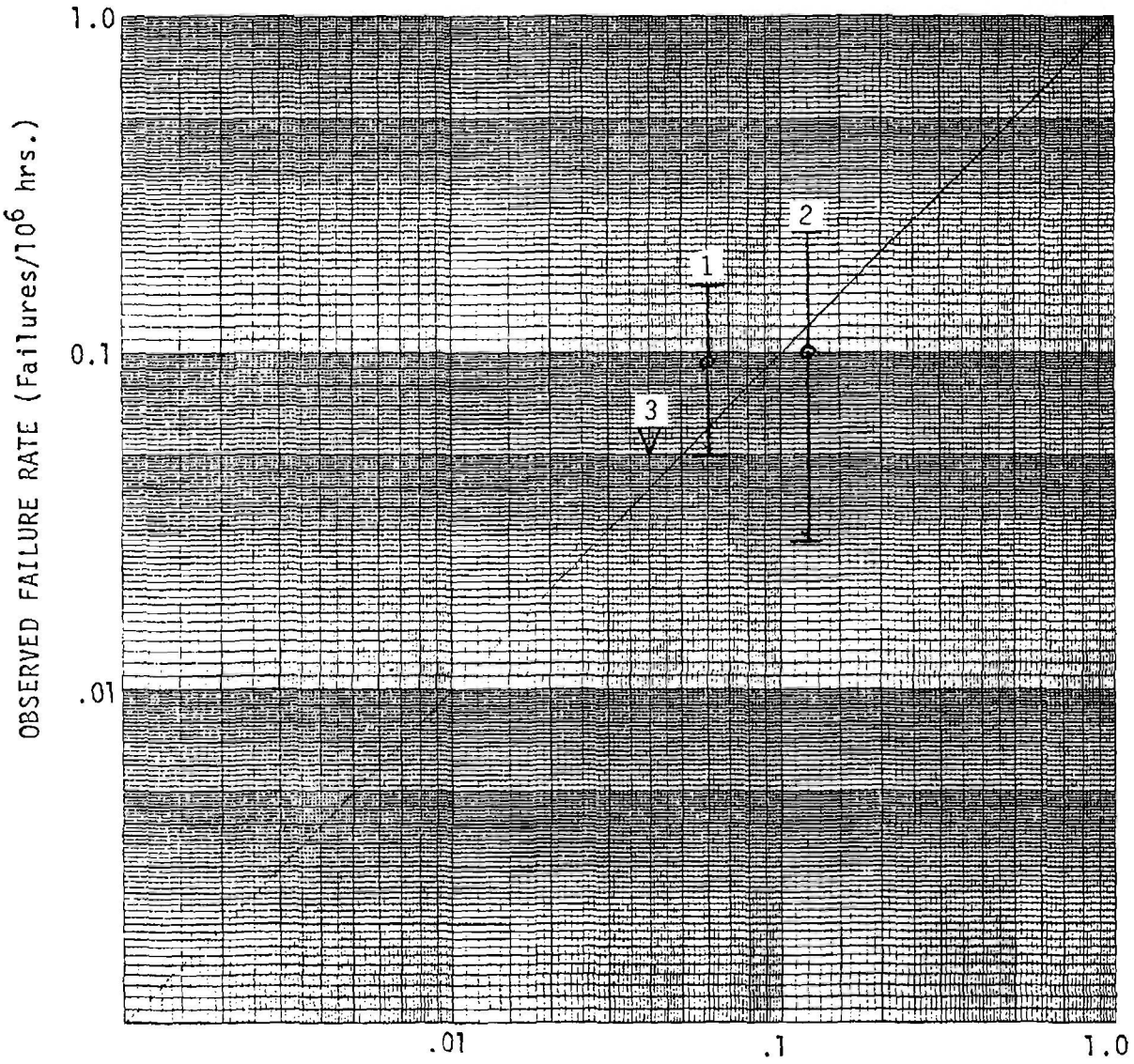


FIGURE 5.1: PRINTED WIRING ASSEMBLY OBSERVED FAILURE RATES VS. PROPOSED MODEL PREDICTED FAILURE RATES

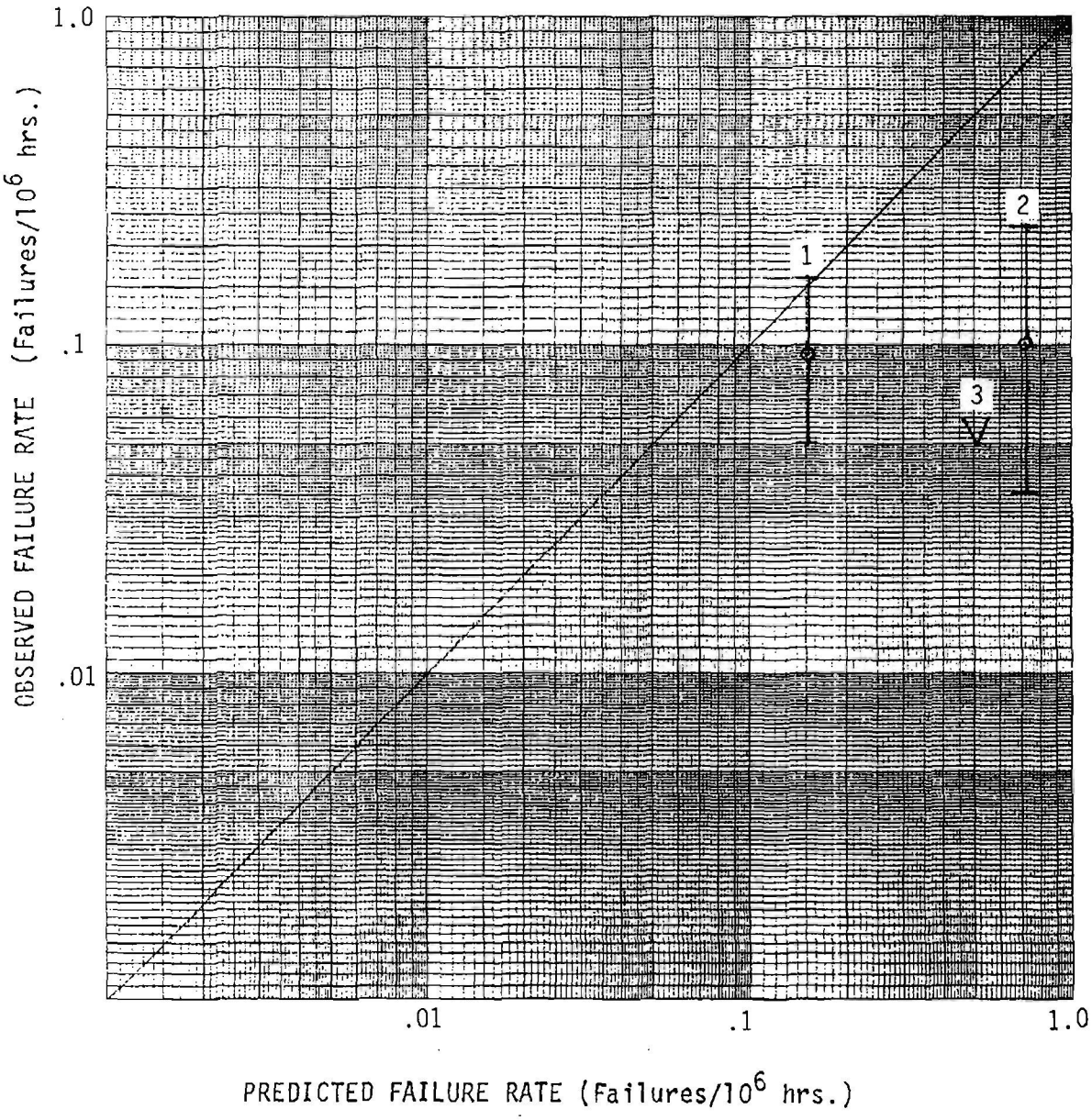


FIGURE 5.2: PRINTED WIRING ASSEMBLY OBSERVED FAILURE RATES VS. MIL-HDBK-217C PREDICTED FAILURE RATES

.0000067 failures/10^6 hours. With 90% confidence, there is no statistically significant difference between this value and the proposed base failure rate for solderless wrap assemblies.

6. CONCLUSIONS

The failure rate prediction mathematical models developed for interconnection assemblies greatly improve upon current failure rate prediction capabilities. Over 9.6 x 10^8 assembly operating hours and 7.3 x 10^{11} connection operating hours were collected and analyzed in support of this study effort. The following advantages are offered by the proposed failure rate prediction methodology:

- o greater sensitivity
- o increased accuracy
- o expanded prediction capabilities
- o assembly level prediction model

These advantages offered by the proposed models are discussed in the following paragraphs.

The proposed failure rate prediction model for printed wiring assemblies provides greater sensitivity in regard to predicting multilayer printed wiring assembly failure rate. The proposed model offers a complexity factor which modifies the predicted failure rate with a particular numerical value corresponding to each unique number of circuit planes. Additionally the proposed model offers greater sensitivity in regard to wave soldered connections. The printed wiring assembly failure rate is modified by a solder application factor which varies according to the rework percentage after wave soldering. The proposed prediction model also considers hand soldered printed wiring assemblies and printed wiring assemblies which may require both wave and hand soldered connections.

The proposed failure rate prediction models offer increased prediction accuracy. Since the initial printed wiring board failure rate prediction model began being used, many technological advances have been made concerning interconnection methods. The data used to derive the proposed prediction models is from the most current available data sources and therefore represents applicable technological advances. Similarly, collected data pertaining to other types of interconnection assemblies were from the most recent available data sources.

Another advantage offered by the proposed failure rate prediction models is that the quantity of considered technologies has been expanded. Interconnection asemblies included in this study which have not been previously considered are wrapped and soldered assemblies, clip termination assemblies and discrete wiring with electroless deposited PTH assemblies.

The proposed failure rate prediction methodology consists of interconnection "assembly" level models. The assembly level printed wiring model replaces the existing printed wiring board and connection models. This offers several advantages. First, field failure rate data was much more accessible at the "assembly" level. This was crucial because large quantities of data were required to develop precise failure rate prediction models. Secondly, the assembly level models provide for a relatively easier prediction methodology by requiring one less mathematical model for system level reliability predictions.

7. RECOMMENDATIONS

Although the proposed interconnection assembly failure rate prediction models greatly improve prediction capabilities, several recommendations are necessary in light of all available information. Several of the proposed models were based on limited data resources and should be further investigated. Additionally, there are emerging

technologies which are identified in this section but not considered in the study. Every possible attempt should be made in the future to collect field failure rate data so that failure rate prediction methodologies can be developed for these technologies.

The failure rate prediction models for wrapped and soldered, and clip termination assemblies were derived using a single sided 60% confidence value to estimate the base failure rate. While this technique provided intuitively reasonable results, it cannot replace the precision offered from data analysis utilizing observed field failures. Additionally, the solder application factor for hand soldered printed wiring assemblies was derived using an extension of the relation developed for wave soldered printed wiring assemblies. Therefore, the proposed wrapped and soldered, clip termination and hand soldered printed wiring assembly prediction models should be reevaluated when sufficient data sources become available.

Perhaps the emerging technology which is most widely used in the electronics industry is flexible circuitry. The use of flexible circuit boards is being introduced into military equipments. As a result, there will be an increase in potential data sources and perhaps sufficient data to derive a failure rate prediction methodology in the near future.

Manufacturers are able to produce polyimide substrate printed wiring boards. The z-axis thermal coefficient of expansion for polyimide is much more compatible with the copper plated through hole than regular epoxy glass. Theoretically, the plated through hole failure rate on polyimide substrate printed wiring boards is significantly lower, particularly at high temperature applications. However, cost and manufacturing difficulties inhibit wide spread usage of polyimide. Future high reliability or high temperature applications may require polyimide because of the superior high temperature characteristics. Therefore, it is recommended that efforts are made to collect data for polyimide printed wiring assemblies.

The chip carrier is an emerging technology with potential to have a great effect on the electronics industry. The dual-in-line package (DIP) cannot meet the physical and electrical requirements of LSI and VLSI circuitry. Chip carriers provide relief but are not compliant with existing epoxy glass substrates. Chip carriers require a more rigid board material. A chip carrier assembly mounted on an epoxy glass board when exposed to vibration stress could severly strain the interconnections. Therefore, the use of ceramic boards, which offer a more rigid substrate, may accompany the growth of chip carriers. It is recommended that a failure rate prediction methodology for ceramic boards and chip carriers be considered.

Another technology which is relatively recent is porcelainized-steel substrates. The porcelainized steel substrates offer far superior heat transfer characteristics as compared to epoxy glass substrates. As interconnection density increases with the advent of LSI and VLSI devices, heat transfer characteristics will become crucial. Heat sensitive devices such as high power transistors can be mounted on porcelainized steel with much less difficulty. The reliability of porcelainized-steel substrates should be studied if they begin to be utilized more often.

A technological advancement concerning soldering technology is vapor formed reflow soldered connections. The solder connection is made by introducing a freon vapor into an enclosure with the unsoldered assembly. The evaporation temperature of liquid freon is variable, depending on the particular composition. Therefore, the uniform temperature within the enclosure can be controlled to best suit the users particular needs. This technique virtually eliminates the variability introduced by human involvement. The resulting solder connections would potentially have very low failure rates. A reliability study concerning vapor formed solder connections would require large magnitudes of collected data and any proposed study should be initiated at the earliest possible opportunity.

APPENDIX 1

MIL-HDBK-217C REVISION PAGES

5.1.13 INTERCONNECTION ASSEMBLIES

5.1.13.1 Plated Through Hole Assemblies

The failure rate model for plated through hole (PTH) assemblies is:

$$\lambda_p = \lambda_b \pi_Q \pi_E \Sigma \left[N_i (\pi_C + \pi_{S_i}) \right]$$

where

λ_b = base failure rate, Table 5.1.13.1-1

π_Q = quality factor, Table 5.1.13.1-2

π_E = environmental factor, Table 5.1.1 3.1-4

N_1 = quantity of wave soldered PTHs

N_2 = quantity of hand soldered PTHs

π_C = complexity factor, Table 5.1.13.1-5

π_{S_i} = solder application factors, Table 5.1.13.1-3

TABLE 5.1.13.1-1
λ_b, BASE FAILURE RATE

TECHNOLOGY	λ_b (failures/10^6 hrs.)
Printed Wiring Assemblies	.000041
Discrete Wiring w/Electroless Deposited PTH*	.00026

*applies to two or less levels of circuitry

TABLE 5.1.13.1-2
π_Q, QUALITY FACTOR

QUALITY GRADE	π_Q
Manufactured to MIL-SPEC or comparable IPC Standards	1
Lower Quality	10

TABLE 5.1.13.1-3
π_S, SOLDER APPLICATION FACTOR

PROCESS	REWORK PERCENTAGE	π_S
Wave Solder	0 - 5	0
	6 - 10	0.2
	11 - 15	0.9
	16 - 20	1.5
	21 - 25	2.2
	26 - 30	2.9
	31 - 35	3.6
	36 - 40	4.3
	over 40	6.1
	unknown	6.1
Hand Solder	Not Applicable	.13

TABLE 5.1.13.1-5
π_C, COMPLEXITY FACTOR

Number of Circuit Planes	π_C
≤2	1
3	1.3
4	1.5
5	1.8
6	2.0
7	2.2
8	2.4
9	2.6
10	2.7
11	2.9
12	3.1
13	3.2
14	3.4
15	3.5
16	3.7
Discrete Wiring w/PTH	1

For greater than 16 circuit planes,
$\pi_C = .65\ \lambda^{.63}$,
λ = quantity of circuit planes

TABLE 5.1.13.1-4
ENVIRONMENTAL MODE FACTORS

ENVIRONMENT	π_E
G_B	1
G_F	2.3
G_M	7.7
M_P	6.9
N_{SB}	4.1
N_S	5.3
N_U	12
N_H	13
N_{UU}	14
A_{RW}	19
A_{IC}	2.0
A_{IT}	5.5
A_{IB}	8.5
A_{IA}	5.5
A_{IF}	7.0
A_{UC}	6.0
A_{UT}	15
A_{UB}	25
A_{UA}	15
A_{UF}	20
S_F	1
M_{FF}	8.7
M_{FA}	12
U_{SL}	26
M_L	29
C_L	500

5.1.13.2 Non Plated Through Hole Assemblies

The failure rate model for non plated through hole assemblies is:

$$\lambda_p = \pi_E \Sigma (\lambda_{bi} N_i)$$

where π_E = environmental factor, Table 5.1.13.2-2

$\Sigma(\lambda_{bi} N_i)$ = sum total of base failure rates for all the connections on the assembly

λ_{bi} = base failure rates, Table 5.1.13.2-1

N_i = quantity of connections

TABLE 5.1.13.2-1
λ_b, BASE FAILURE RATE

TECHNOLOGY	λ_{bi} (failures/10^6 hrs)
Solderless Wrap	.0000035
Wrapped and Soldered	.00014
Clip Termination	.00012
Reflow Solder	.000069
Hand Soldered	.0026
Weld	.0013

TABLE 5.1.13.2-2
π_E, ENVIRONMENTAL MODE FACTORS

ENVIRONMENT	π_E
G_B	1
G_F	2.1
G_M	7.3
M_P	7.3
N_{SB}	3.5
N_S	4.4
N_U	9.3
N_H	11
N_{UU}	12
A_{RW}	16
A_{IC}	1.5
A_{IT}	3.5
A_{IB}	4.5
A_{IA}	7.5
A_{IF}	5
A_{UC}	2
A_{UT}	7.5
A_{UB}	5
A_{UA}	9.5
A_{UF}	7
S_F	1
M_{FF}	7.3
M_{FA}	10
U_{SL}	22
M_L	25
C_L	420

5.1.13.3 EXAMPLE FAILURE RATE CALCULATIONS

Example 1

Given: A plated through hole printed wiring assembly having 6 circuit planes and 700 PTHs is to be used in an uninhabited trainer airborne environment. 560 of the PTHs are filled by wave soldering and 140 by hand soldering. 8 percent of the wave solder connections require rework. All elements of the assembly are in accordance with military specifications.

Step 1 - The general failure rate expression (See Section 5.1.13.1) is:

$$\lambda_p = \lambda_b \pi_Q \pi_E [N_1(\pi_C + \pi_{S_1}) + N_2(\pi_C + \pi_{S_2})].$$

Step 2 - From Table 5.1.13.1-1 the base failure rate for printed wiring assemblies is:

$$\lambda_b = .000041 \text{ failures}/10^6 \text{ hr.}$$

Step 3 - From Tables 5.1.13.1-2 and 5.1.13.1-4:

$$\pi_Q = 1$$

$$\pi_E = 15 \text{ for } A_{UT}.$$

Step 4 - From Table 5.1.13.1-5 for 6 circuit planes:

$$\pi_C = 2.$$

Step 5 - From Table 5.1.13.1-3 the application factor for wave solder with 8% rework is:

$$\pi_{S_1} = 0.2$$

and the application factor for hand solder is:

$\pi_{S_2} = 13.$

Step 6 - From the example statement:

$N_1 = 560$
$N_2 = 140.$

Step 7 - Obtain the failure rate by substituting values into the model:

$\lambda_p = .00041\ (1)\ (15)\ [560(2 + 0.2) + 140(2 + 13)]$
$= 2.049$ failures/10^6 hours.

Example 2

Given: A discrete wiring with electroless deposited PTHs assembly having 2 levels of circuitry and 600 PTHs is to be used in a fixed ground environment. All PTHs are filled by wave soldering, 18 percent of which require rework. All elements of the assembly are in accordance with IPC specifications.

Step 1 - The general failure rate expression, all connections formed by wave solder (See Section 5.1.13.1) is:

$\lambda_p = \lambda_b\ \pi_Q\ \pi_E\ [N(\pi_C + \pi_S)].$

Step 2 - From Tables 5.1.13.1-1, 5.1.13.1-2, and 5.1.13.1-4:

$\lambda_b = .00026$ failures/10^6 hours
$\pi_Q = 1$
$\pi_E = 2.3$ for G_F.

Step 3 - From Tables 5.1.13.1-3 and 5.1.13.1-5:

π_S = 1.5 (18% rework)
π_C = 1.

Step 4 - Given in the example statement:

N = 600.

Step 5 - Obtain the failure rate by substituting the values into the model:

λ_p = .00026 (1) (2.3) (600) (1 + 1.5)
= .897 failures/10^6 hours.

Example 3

Given: A solderless wrap wiring assembly is to be used in an inhabited cargo airborne environment. The assembly consists of 1560 wraps and 156 of the posts are connected to either the ground or voltage planes with reflow solder. All elements of the assembly are in accordance with military specifications.

Step 1 - The general failure rate expression (See Section 5.1.13.2) is:

$$\lambda_p = \pi_E (\lambda_{b_1} N_1 + \lambda_{b_2} N_2)$$

where:

λ_{b_1} = solderless wrap base failure rate
N_1 = quantity of solderless wraps
λ_{b_2} = reflow soldered base failure rate
N_2 = quantity of solder connections.

Step 2 - From Tables 5.1.13.2-2 and 5.1.13.2-1:

π_E = 1.5 for A_{IC}
λ_{b1} = .0000035 failures/10^6 hours
λ_{b2} = .000069 failures/10^6 hours.

Step 3 - Obtain the failure rate by substituting values into the model:

λ_p = 1.5 (.0000035) (1560) + (.000069) (156)
= .024 failures/10^6 hours.

Example 4

Given: A wrapped and soldered wiring assembly is to be used in a fixed ground environment. The assembly consists of 4000 wrapped and soldered connections.

Step 1 - The general failure rate expression (See Section 5.1.13.2) is:

$\lambda_p = \pi_E \lambda_b N.$

Step 2 - From Tables 5.1.13.2-2 and 5.1.13.2-1:

π_E = 2.1 for fixed ground
λ_b = .00014 failures/10^6 hours.

Step 3 - Given in the example statement:

N = 4000.

Step 4 - Obtain the failure rate by substituting the values into the model:

$$\lambda_p = 2.1\ (.00014)\ (4000)$$
$$= 1.176 \text{ failures}/10^6 \text{ hours.}$$

Example 5

Given: A clip termination wiring assembly is to be used in a sheltered naval environment. The assembly consists of 2400 clip terminations and 100 of the posts are connected to either the ground or voltage planes by reflow solder connections. All elements of the assembly are in accordance with military specifications.

Step 1 - The general failure rate expression (See Section 5.1.13.2) is:

$$\lambda_p = \pi_E\ (\lambda_{b1}\ N_1 + \lambda_{b2}\ N_2),$$

where:

λ_{b1} = clip termination base failure rate
N_1 = quantity of clip terminations
λ_{b2} = reflow solder base failure rate
N_2 = quantity of reflow solder connections.

Step 2 - From Tables 5.1.13.2-2 and 5.1.13.2-1:

π_E = 4.4 for N_S
λ_{b1} = .00012 failures/10^6 hours
λ_{b2} = .000069 failures/10^6 hours.

Step 3 - Given in the example statement:

$N_1 = 2400$
$N_2 = 100.$

Step 4 - Obtain the failure rate by substituting values into the model:

$\lambda_p = 4.4\ [(.00012)\ (2400) + (.00069)\ (100)]$
$= 1.298$ failures/10^6 hours.

Example 6

Given: A reflow solder printed wiring assembly (no PTHs) is to be used in a space flight environment. The assembly consists of the printed wiring board and 300 reflow solder connections. All elements of the assembly are in accordance with military specificaitons.

Step 1 - The general failure rate expression (See Section 5.1.13.2) is:

$\lambda_p = \pi_E\ \lambda_b\ N.$

Step 2 - From Tables 5.1.13.2-2 and 5.1.13.2-1:

$\pi_E = 1$ for S_F
$\lambda_b = .000069$ failures/10^6 hours.

Step 3 - Given in the example statement

$N = 300.$

Step 4 - Obtain the failure rate by substituting the values into the model:

$$\lambda_p = 1\ (.000069)\ (300)$$
$$= .021 \text{ failures}/10^6 \text{ hours.}$$

5.1.14 Connections. The part operating failure rate model (λ_p) is:

$$\lambda_p = \lambda_b (\Pi_E \times \Pi_T \times \Pi_Q)$$

where:

λ_b = base failure rate (Table 5.1.14-1)

Π_E = environmental factor (Table 5.1.14-2)

Π_T = tool type factor (Table 5.1.14-3 for crimp type)
= 1 or all types except crimp

Π_Q = quality factor (Table 5.1.14-4 for crimp type)
= 1 or all types except crimp

TABLE 5.1.14-1

λ_b, BASE FAILURE RATE

CONNECTION TYPE	λ_b (F/10^6 hrs)
Hand Solder	.0026
Crimp	.00026
Weld	.0013

TABLE 5.1.14-2
ENVIRONMENTAL MODE FACTORS

ENVIRONMENT	π_E
G_B	1
G_F	2.1
G_M	7.3
M_P	7.3
N_{SB}	3.5
N_S	4.4
N_U	9.9
N_H	11
N_{UU}	12
A_{RW}	16
A_{IC}	1.5
A_{IT}	5.5
A_{IB}	4.5
A_{IA}	7.5
A_{IF}	5
A_{UC}	2
A_{UT}	7.5
A_{UB}	6
A_{UA}	9.5
A_{UF}	7
S_F	1
M_{FF}	7.3
M_{FA}	10
U_{SL}	22
M_L	25
C_L	420

TABLE 5.1.14-3: TOOL TYPE FACTORS (π_T)
FOR CRIMP CONNECTIONS

TOOL TYPE	π_T
Automated	1
Manual	2

Notes: 1 Automated encompasses all powered tools not handheld.

2 Manual includes all hand-held tools.

TABLE 5.1.14-4: QUALITY FACTORS (π_Q)
FOR CRIMP CONNECTIONS

QUALITY GRADE	π_Q	COMMENTS
Automated Tools	1.0	Daily pull tests recommended.
Manual Tools:		
Upper	0.5	Only MIL-SPEC or approved equivalent tools and terminals, pull test at beginning and end of each shift, color coded tools and terminations.
Standard	1.0	Only MIL-SPEC tools, pull test at beginning of each shift.
Lower	10.0	Anything less than standard criteria.

APPENDIX 2

APPLICABLE STATISTICAL TECHNIQUES

APPENDIX 2
APPLICABLE STATISTICAL TECHNIQUES

In order to identify and evaluate the relationships between the various reliability considerations which are defined by the data, various statistical analysis techniques were employed. The techniques which were applicable to the derivation of the reliability prediction models are briefly reviewed in the following paragraphs.

Stepwise Multiple Linear Regression Analysis. The stepwise multiple linear regression analysis routine assumes a preliminary model of the form:

$$Y' = b_0 + b_1X_1 + b_2X_2 + \ldots b_iX_i$$

where Y' is the resultant dependent variable; X_1, $X_2 \ldots X_i$ are the independent variables which are thought to influence the value of Y'; and b_1, $b_2 \ldots b_i$ are the coefficients which will be found by the regression.

To perform a regression, a number of data points, each consisting of a known Y and its corresponding X variables, are required. A proper regression also requires that the X variables be nearly independent and that there are many more data points than X variables.

The regression technique first computes a correlation matrix comparing all the X variables to one another as well as to the observed Y. This matrix serves to identify any nonindependent X variables (except those which are a function of two or more other X variables) and is also used to compute the relative correlation of the Y variable to each of the X variables.

The analysis orders the X variables according to their relative correlation with the Y variables. Considering the first X variable and the

Y variable, b_0 and b_1 are computed such that the sum of the squares of (Y-Y') will be a minimum. The second X variable is then considered in the computation of b_0, b_1 and b_2 such that the sum of the squares of (Y-Y') will again be minimum.

If the improvement in the estimate afforded by the inclusion of this second variable is significant with respect to a given confidence level, the variable is accepted as part of the model and regression continues by considering a third variable.

If considering the second variable does not result in a significant improvement, the model remains

$$Y = b_0 + b_1X_1$$

Whenever a new variable is included in the fitted model, all previously included variables are retested for significance, given that the new variable is in the model.

The regression continues until all of the signficant X variables have been identified and their corresponding b coefficients have been calculated.

Curve Fit Analysis Technique. A series of curve fit programs are available for establishing the mathematical relationship between dependent and independent variable pairs in a given data set. These techniques provide a least squares curve fit of the data points to various types of expressions, including linear, exponential, power, and hyperbolic functions. The output of these programs express the dependent variable (Y) in terms of the independent variable (X) and two coefficients (A,B). In addition to the values of the coefficeints A and B, the output provides an index of determination for each function which represents the "goodness-of-fit" of the expression to the data points.

R^2 - Multiple Correlation Coefficient. The R^2 value is the ratio of the sum of the squares of the variance explained by the regression to the sum of the squares of the variance in the observed data. An R^2 value of 100% is the ideal result.

Chi-Square Goodness of Fit Test. The chi-square goodness of fit test compares observed data to expected values by:

$$\chi^2 = \Sigma \frac{(o-e)^2}{e}$$

where

χ^2 = chi-square values
o = observed value
e = predicted value

The resulting chi-square value decides whether or not the observed events differ from the predicted at a set level of significance for given degrees of freedom. Chi-square tables are given in Experimental Statistics, National Bureau of Standards, Handbook 91 authored by Mary Gibbons Natrella.

Chi-square Confidence Intervals. The chi-square statistic is used to identify a confidence internal around the point estimate failure rate. The 90% confidence internal is comprised of the lower 5% confidence and upper 95% confidence levels. A 90% confidence interval is the range of values around the point estimate that would, with a 90% probability, include the mean of an infinite sample of similar devices. These values are calculated as follows:

$$\text{Lower - 5\% confidence level} = \frac{\chi^2 (.95, 2r)}{2T}$$

$$\text{Point estimate} = \frac{r}{T}$$

$$\text{Upper - 95\% confidence level} = \frac{\chi^2 (.05, 2r + 2)}{2T}$$

where

r = number of degrees of freedom equal to the number of observed failures

T = total operating hours

$\chi^2(\alpha)$ = Chi-sqaure value for the particular confidence level based on the number of degrees of freedom (obtained from Chi-sqaure tables)

Additionally, data records where no failures were recorded utilized a single sided upper 60% confidence value to approximate point estimate. This value was calculated similar to the upper 95% confidence level given above.

Kolmogorov - Smirnov Goodness of Fit Test. This test analyzes the maximum difference between observed and expected value for a theoretical cumulative distribution. If the maximum difference is larger than the critical value for a set level of significance, then the observed events would not appear to follow the assumed theoretical distribution. A more thorough description and critical value tables are given in Non-parametric Statistics for the Behavioral Sciences, McGraw-Hill, 1956, authored by Sidney Siegel.

Dixon Criterion. The Dixon Criterion is used to identify outliers. It is given by a formula dependent on sample size. A full description and tables of the critical values are given in Experimental Statistics, National Bureau of Standards Handbook 91, authored by Mary Gibbons Natrella.

Weighting Factor. It often happens in reliability studies that some of the data points used in a regression analysis or statistical calculation are less precise than others. Ideally, the reciprical of the variance would provide a suitable weighting factor. If there is not sufficient information to calculate the variance, the reciprical of the chi-sqaure 90% confidence interval size can be considered. This type of weighting factor contains biases at high and low failure rates. The optimal weighting factor for data bases where no variance can be computed is the reciprical of the difference between the log values for the 95% confidence level and the 5% confidence level:

$$wf = \frac{1}{\ln \lambda_{.95} - \ln \lambda_{.05}}$$

where

$\lambda_{.95}$ = upper - 95% confidence level

$\lambda_{.05}$ = lower - 5% confidence level.

This provides a weighting factor whose influence increases with the number of observed failures, but contains no biases at high or low failure rates. This method is empirical rather than strictly theoretical.

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