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RELIABILITY PREDICTION MODELING OF NEW DEVICES

Arthur D. Little, Inc.

Roger G. Long
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ROME AIR DEVELOPMENT CENTER
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This report presents reliability prediction models for high density microcircuits including magnetic bubble and charge-coupled device memories for inclusion in MIL-HDBK-217C, "Reliability Prediction of Electronic Equipment". The approach in this investigation was unique in that the models were developed utilizing only early device life cycle data, since there was only limited field data available. Two separate models were developed. An additive hybrid type failure rate → next page

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prediction model was formulated for Magnetic Bubble Memories and for the Charge-Coupled Memory devices it was found that the NMOS Dynamic RAM model currently in MIL-HDBK-217C, Notice 1 was applicable. Both models are presented in the standard MIL-HDBK-217C format, are relatively simple to use, and allow for refinements based on field and life test data as it becomes available. Finally the models exhibit reasonable correlation with existing field data.

Evaluation

The objective of this effort was to develop failure rate prediction models for Magnetic Bubble Memory (MBM) and Charge-Coupled Device (CCD) Memory circuits regardless of their complexity or density. The approach taken was unique in that the models were developed from data obtained during the early stages of the devices' life cycle.

The general form of the failure rate prediction technique for MBM's was found to be an additive hybrid type model consisting of the summation of the failure rates of four individual sectors; control sense and driving sector, memory sector, interconnect and substrate sector, and the inductive sector. The following are some of the more important findings:

a. The complexity factors for the control sector are based on the number of major and minor loops and for the memory sector on the number of bits per loop. The existing complexity tables in MIL-HDBK-217C-"Reliability Prediction of Electronic Equipment", are used for these values.

b. Multipliers based on the number of major and minor loops are used to modify the memory sector complexity factors.

c. A magnetic bias margin multiplier factor which corresponds to the voltage derating factor was developed for the memory sector.

d. A derating multiplier based on bubble size was developed for the memory sector temperature acceleration factor.

In addition the model retains the normal MIL-HDBK-217C adjustment factors such as quality, package, environment, and device learning factor. The remaining contributions to the total failure rate are obtained by using the appropriate sections of MIL-HDBK-217C such as for the printed wiring structures.

For CCD's it was found that the present NMOS Dynamic RAM model in MIL-HDBK-217C was capable of predicting the failure rates to acceptable accuracy.

To assess the accuracy of the models, comparisons are presented between the predicted failure rates and actual field data. These comparisons along with sample calculations demonstrate reasonable confidence in the developed models. The feasibility of the approach to develop failure rate prediction models based on early life cycle data will be assessed and refinements incorporated based on additional field data as it becomes available.

The prediction models presented in this report are for information purposes only at this time, and are not intended to be used without approval of the appropriate contract office. The new models will be submitted for early DOD and industry co-ordination and inclusion in MIL-HDBK-217C.

RADC wishes to thank Mr. Fred Sakate and the Federal Aviation Administration (FAA) for contributions in the partial funding of this effort.

Peter F. Manno

PETER F. MANNO

Project Engineer

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PREFACE

This report was prepared by Arthur D. Little, Inc., of Cambridge, Massachusetts, under U. S. Air Force Contract No. F30602-78-C-0296. The contract was initiated by AFSC Rome Air Development Center of Griffis AFB, NY, 13441. It was administered under the technical direction of Mr. Peter Manno, RADC/RBRM, acting as the technical project officer. Captain D. G. Arnold, U. S. Air Force, was the contract administrator for the USAF.

This report is a summary of the work completed under this contract during the period from September 1978 through November 1979.

SUMMARY

PURPOSE AND SCOPE

The current guidelines of Military Standardization Handbook MIL-HDBK-217, Reliability Prediction of Electronic Equipment, may not be applicable to certain classes of large-scale semiconductor memory devices. Therefore, in this study, two examples of new semiconductor memory technologies -- i.e., Magnetic Bubble Memory devices and Charge-Coupled Memory devices -- were examined to develop models for calculating their reliability.

Magnetic Bubble Memory devices are being used in increasingly larger quantities and research is continuing in the development of devices in the 10^6-bit range. On the other hand, Charge-Coupled Memory devices have not been as widely accepted in the marketplace. Since competing technologies have proven to be more versatile, many manufacturers have discontinued their efforts in this area. Therefore, most of the effort in this study was concentrated on the Magnetic Bubble Memory devices because of their greater potential for being typical of future large-scale semiconductor memory systems.

FINDINGS

The methods of MIL-HDBK-217C (Proposed Notice 1) model for predicting the reliability of an N-MOS large-scale memory are suitable for the technology and chip architecture of the new Charge-Coupled Memory devices; therefore, we developed a model for the latter devices based on the applicable guidelines approach. To increase our confidence in the validity of this approach, theoretical

calculations of device failure rates were compared to the limited field data that were available. The correlation of the figures was within an acceptable range.

The Magnetic Bubble Memory uses thin-film technology for the memory structure and is a nondissipative array of magnetic elements. The data read and write elements are dissipative current loops deposited close to the permalloy memory elements of the same chip. The surrounding mechanical interface and magnetic elements that make up the remainder of the memory device were accounted for as discrete segments of the additive hybrid failure rate prediction model.

The Magnetic Bubble Memory devices are being used in some developmental systems, and in final product areas for evaluation purposes. Data have been developed on factors that affect the fabrication yield, but because of the limited field exposure to date little data have been developed on failure modes and failure rates of these devices. The high-capacity capability of these devices -- 10^5 or 10^6 bits poses some unique problems of "soft" error reliability not directly related to the class of failure normally considered in the guidelines of MIL-HDBK-217. The "hard" errors such as those normally related to catastrophic defects such as permanent physical defects in the structure, shorts, voids or other intrinsic flaws are the prime consideration in this study. The second class of defect is the "soft" error such as random, nonrecurring bit errors not associated with any physical defect. The "soft" errors may be due to system noise, pattern sensitivity or external effects such as alpha radiation. The failure rate model developed for the Magnetic Bubble Memory devices is based on catastrophic or drift-related failures and does not include the "soft" errors.

MODELS DEVELOPED

The failure rate model for Charge-Coupled Memory devices developed from Section 2.1.4-1 of MIL-HDBK-217C (Proposed Notice 1) is:

$$\lambda p = \pi_Q[C_1 \pi_T \pi_V + (C_2 + C_3)\pi_E]\pi_L$$

As calculated with this model, typical failure rates of two to ten failures per 10^6 hours at 40°C compare favorably with the limited field experience.

The failure rate prediction model developed for the Magnetic Bubble Memory devices is based on a hybrid structure where the total failure rate is the summation of the individual failure rates, i.e.:

$$\lambda p = \lambda_1 + \lambda_2 + \lambda_3 + \lambda_4$$

where:

λp = failure rate of the Magnetic Bubble Memory
λ_1 = failure rate of the sense elements
λ_2 = failure rate of the memory elements
λ_3 = failure rate of the interconnect structure
λ_4 = failure rate of the inductive elements

RECOMMENDATIONS

Because of the declining interest in charge-coupled devices, we recommend that no further study be devoted to their reliability prediction modeling.

The Magnetic Bubble Memory system is a very active area for the next generation of large-scale semiconductor memories. Consistent field data of failure rates and failure modes are needed for further verification of the reliability prediction model we have developed. In the interim, this model is satisfactory for comparative reliability analysis and as a guide for the accumulation of field data.

I. INTRODUCTION

A. BACKGROUND

Large-scale memory devices with capacity for storage in the order of 10^5 or 10^6 bits are rapidly emerging as realizable memory systems. Because the recommendations of the Military Standardization Handbook for the Reliability Prediction of Electronic Equipment MIL-HDBK-217 may not be adequate for this class of device, this study was initiated to evaluate the state-of-the-art of some of the new semiconductor memory devices in this category and develop a model for the prediction of failure rates for large-scale microcircuits.

The two devices selected as probably typical of the new state-of-the-art large-scale memory products are the Charge-Coupled Memory devices and the Magnetic Bubble Memory devices. As this study progressed it became evident that the development of Charge-Coupled Memory devices was declining and many of the manufacturers had withdrawn from the fabrication of this class of product. Therefore, it was decided that Charge-Coupled Memory products would not warrant the detailed evaluation required of the more dominant Magnetic Bubble Memories.

B. PURPOSE

The objective of this study was the development and validation of a reliability prediction technique for new state-of-the-art microcircuits, specifically high-density complex microcircuits such as Magnetic Bubble Memory and Charge-Coupled Memory circuits. The work was based on guidelines established in MIL-HDBK-217, "Reliability Prediction of Electronic Equipment."

The materials, process technology and fabrication techniques used in Magnetic Bubble Memory devices were evaluated. Established semiconductor reliability techniques were examined where applicable and data extrapolated to be used in the development of the proposed failure rate prediction model.

C. METHOD

Background information was developed by an extensive literature search of technical publications, manufacturers' data, and previous studies. A series of interviews was conducted with research personnel, manufacturers, probable device users, and various government and private installations involved in the design, development, manufacture or application of these two devices. The data were analyzed and a series of models was tested to develop a unique approach to a recommended prediction technique.

II. MAGNETIC BUBBLE MEMORY DEVICE OPERATION

A. TYPICAL OPERATING CHARACTERISTICS

Bell Laboratories and Western Electric have been fabricating Magnetic Bubble Memory devices for several years. The majority of these devices has been for telephone-related applications. IBM has been conducting research and applications development on Magnetic Bubble Memory systems for computer applications. Although various companies are fabricating memory systems encompassing a wide range of characteristics (Table 1), the principal U.S. manufacturers and suppliers of the Magnetic Bubble Memory Devices for general use are Texas Instruments, Rockwell International, and Intel Magnetics.

B. GENERAL DESCRIPTION

Magnetic Bubble Memory devices are a hybrid mass-memory that features nonvolatility, low-power operation, and high-density storage. The basic memory is an epitaxial film of magnetic material on a nonmagnetic garnet crystal substrate with a surrounding magnetic bias field mechanism to complete the basic hybrid module. With the present state-of-the-art, 10^5-bit systems are being evaluated in the field and 10^6-bit systems are feasible.

Much of the early work on Magnetic Bubble Memory structures was done by Bell Laboratories starting in the late 1960's. In addition to Bell Laboratories (and Western Electric) at least three U.S. manufacturers now offer memory devices for commerical use, and a few non-U.S. manufacturers are entering the marketplace.

TABLE 1

KEY CHARACTERISTICS OF CURRENT MAGNETIC BUBBLE MEMORY DEVICES AND COMPARABLE SEMICONDUCTOR MEMORY DEVICES***

CHARACTERISTIC	TEXAS INSTRUMENTS TIB0203	TIB0303	ROCKWELL RBM256	INTEL MAGNETICS 7110	2118*	NATIONAL MM5290*	FAIRCHILD F16K*	SIGNETICS 2690*	TEXAS INSTRUMENTS TMS4164*	TMS4116**	AMI S4028**
Storage Capacity (K Bits)	92	254	256	1000	16	16	16	16	65	16	16
Typical Access Time	4 ms	7.3 ms	4 ms	41ms	80 ns	150 ns	150 ns	150 ns	100 ns	150 ns	200 ns
Maximum Data Rate (KBPS)	50	100	150	100	--	--	--	--	--	--	--
Power Dissipation (W)	0.7	0.9	0.82	6	0.16	0.5	0.375	0.46	0.25	0.5	--
Operating Temperature Range (°C)	0 to 50	0 to 50	-10 to +70	0 to 70	0 to 70	0 to 70	0 to 70	0 to 70	0 to 70	0 to 70	0 to 70
Dip Configuration (No. of Pins)	14	20	18	20	16	16	16	16	16	16	24
Technology	MBM	MBM	MBM	MBM	NMOS	NMOS	NMOS	NMOS	NMOS	NMOS	VMOS

*Dynamic Ram
**Static Ram
***The data is from published data sheets.

The magnetic bubble device is fabricated using technology similar to semiconductor processes. The magnetic domain centers are formed in a magnetic epitaxial film of garnet crystal on a nonmagnetic garnet substrate, and the magnetic domains tend to form or orient themselves in fields perpendicular to the surface. An external field, developed by a permanent magnet structure modulated by two orthogonal electromagnetic coils supported around the garnet substrate, is used to control the bubble formation, location and polarity.

The most widely used basic substrate is a high-purity gadolinium garnet. The thin-film magnetic layer is of the same crystal class with a compatible coefficient of expansion to maintain adhesion strength. Discrete bubble location and pattern is determined by an organization of permalloy elements deposited on the epitaxial surface with an intervening silicon dioxide (SiO_2) insulating layer.

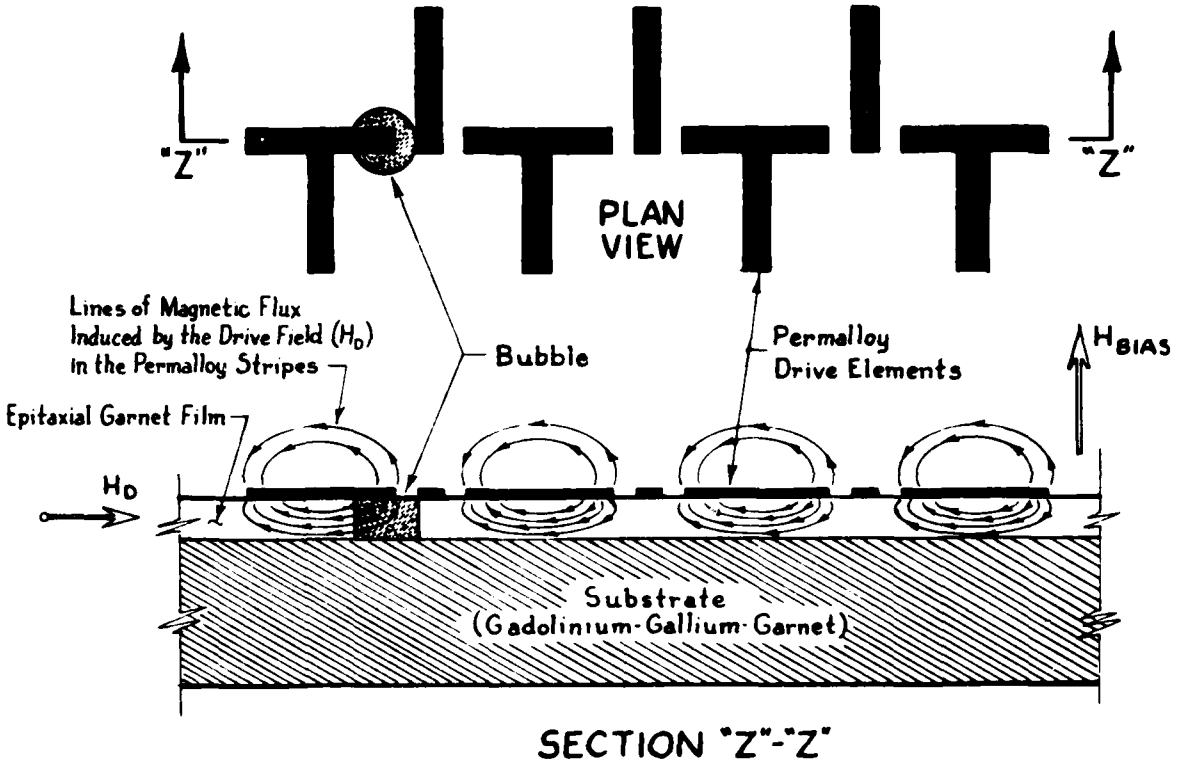
The basic principle of operation of a Magnetic Bubble Memory is the controllable ability to develop small cylindrical magnetic domains in the magnetic film normal to the film by application of an external magnetic field. The magnetic domains are cylinders normal to the epi film, and the circular cross-section area on the film surface takes on the shape of a bubble when viewed under a polarized light, giving the technology the term "bubble." Over a finite range of the external magnetic bias field these bubble domains remain intact. At higher magnetic fields than the "bias range," the bubbles decrease in size and reverse the polarity of their magnetism to that of the surrounding material and cease to exist. When the field is reduced below the bias margin limit, the "bubble" or cylindrical domain deforms into an elongated area and loses its identity as a defined site. The finite useable bias range is unique to a particular bubble structure and is a unique property of the individual design. Individual magnetic domains are considered as "logical ones" and the absence of a domain at a site is a "logical zero."

Strips of magnetic material such as permalloy are located on the epi film by a photolithographic process. A rotating external magnetic field will shift the polarity of these permalloy strips and, in effect, move the magnetic domain along. This apparent movement is actually an orderly rotation of the individual magnetic vectors accomplished by a local reversal of the field to enhance the attraction of the bubble domain to a nearby magnetic area. The permalloy strips form a corridor to guide the bubble propagation and create a data stream of "ones" or "zeros."

At a juncture point of the permalloy pattern, the presence of a bubble can be detected by a change in the magneto-resistance of the permalloy. A bridge arrangement adjacent to the permalloy is used to develop a signal of the presence or absence of a magnetic domain. One leg of the bridge is a reference pattern away from the permalloy and a second leg of the bridge is a conductive pattern under the permalloy site. A change in the resistivity will occur in the presence of a magentic domain.

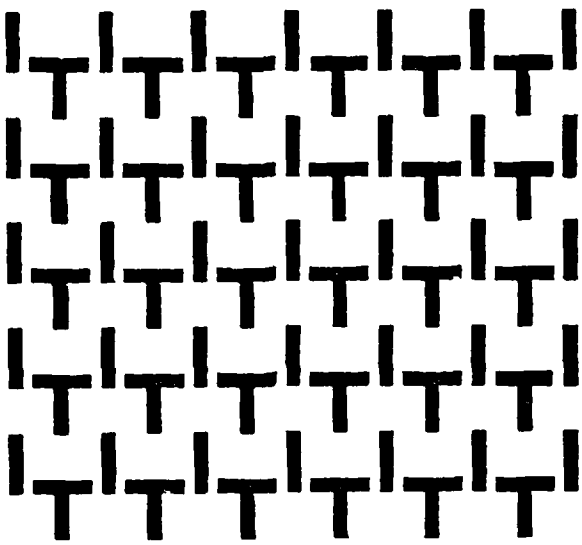
A nondestructive read, or "replicate" function, is accomplished by temporarily elongating a bubble by a field developed by the conductor loop current. The bubble is split into two sites by the injection of a current pulse at the midpoint of the bubble to cause the stretched bubble to collapse into two parts. One site rejoins the circulating data stream, and the second is read out as a "one" or "zero" by a sensor loop.

To write in data, a current loop is used to locally magnetize a data site in the data chain of a specific polarity to produce the desired "one" or "zero" state. Passing a pulse of current through a loop of current conductors located under a permalloy strip will alter the bias field of the permalloy element. The direction of the localized field, the direction of the horizontal field during the pulse and the configuration of the permalloy element determine the effect on the bubble.

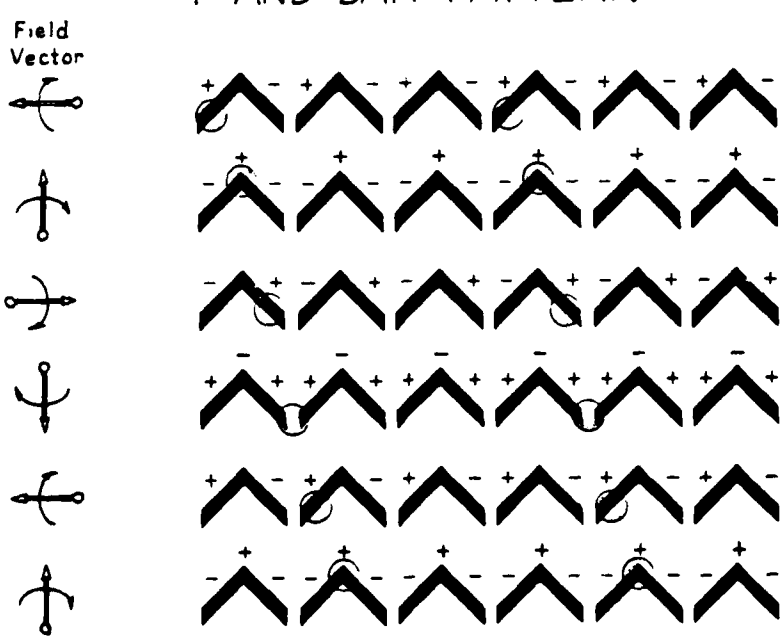


TYPICAL MAGNETIC DOMAIN PROPAGATION

Figure 1



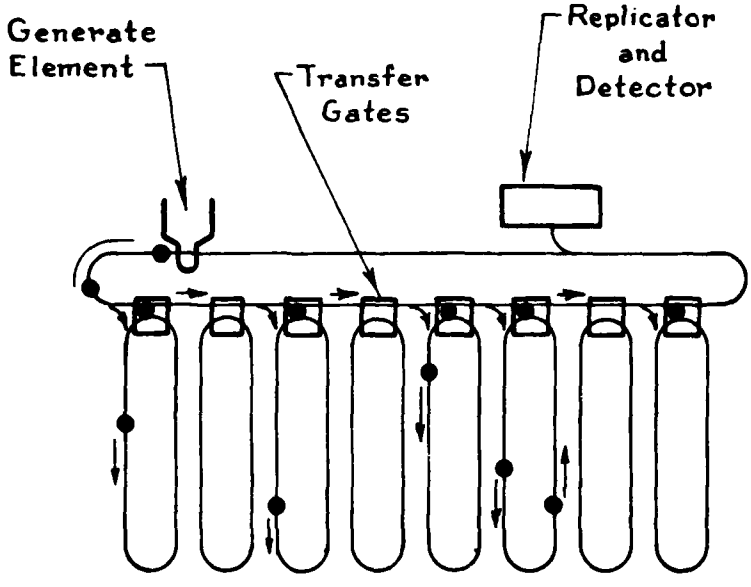
T AND BAR PATTERN



CHEVRON PATTERN

(Bubble Position Versus Magnetic Field Vector)

Figure 2



LOOP ORGANIZATION

Figure 3

The generate function inverts the bias field to allow the formation of a new bubble. The annihilate function is the collapse of a bubble when the immediate field is intensified, and the transfer function is the movement of a bubble from an element on one track to an element on another track.

The data are circulated in a series of minor loops or tracks, each independent of the other. The data are transferred to a major loop on command, thus developing a selective serial read-out or read-in system. The read and write functions are normally accomplished on the major loop or loops and transferred to the desired minor memory loop as selected by the logic.

The chip architecture is a series of minor loops that make up the body of the memory, one or more major loops to transfer data, generate circuitry, replicate circuitry, state sensors.

For the current state-of-the-art, the minimum practical bubble diameter is in the order of 2μm (micrometer) to 3μm (micrometer). Experimental devices are being fabricated with bubble diamteters of less than 1μm. For a nominal chip size of 0.4 x 0.4 inch where from 70% to 80% of the area is available for minor loops, a memory capacity of 256K bits is practical with a bubble size of 3μm. With bubbles 2μm or smaller in diameter, it may be possible to develop a capacity of 10^6 bits in a 0.4-inch square chip. This increased capacity per unit area results in a greater memory density. The required sensing, write or control elements do not increase in direct proportion with the added bit capacity; therefore, with a slightly more efficient bit size and a small increase in chip size, the memory capacity can increase without a major increase in substrate or chip area.

The rotating external magnetic field is supplied by two orthogonal coil sets. These are placed around the chip to develop a uniform and efficient field coupling. Connection from the coils to the coil-driving contact areas is via an intervening substrate, usually a printed circuit card. The total assembly is enclosed in a magnetic shield to reduce interference from external fields. The assembly is encapsulated in a Dual In-Line Package (DIP) format, nonhermetic hybrid package of 18 to 38 leads.

The generation of the magnetic domains in the epitaxial film depends upon the purity of the film and the underlying crystalline substrate. Individual defects can cause malfunctions, errors, or failures in a specific area of a data stream. A memory is typically made up of many minor loops and the individual defect will only affect the loop using that area. By external software organization the affected loop can be deleted from use and the remainder of the memory operated with no ill effect. The total available memory is less than the theoretical maximum, but a practical yield can be achieved by this mechanism.

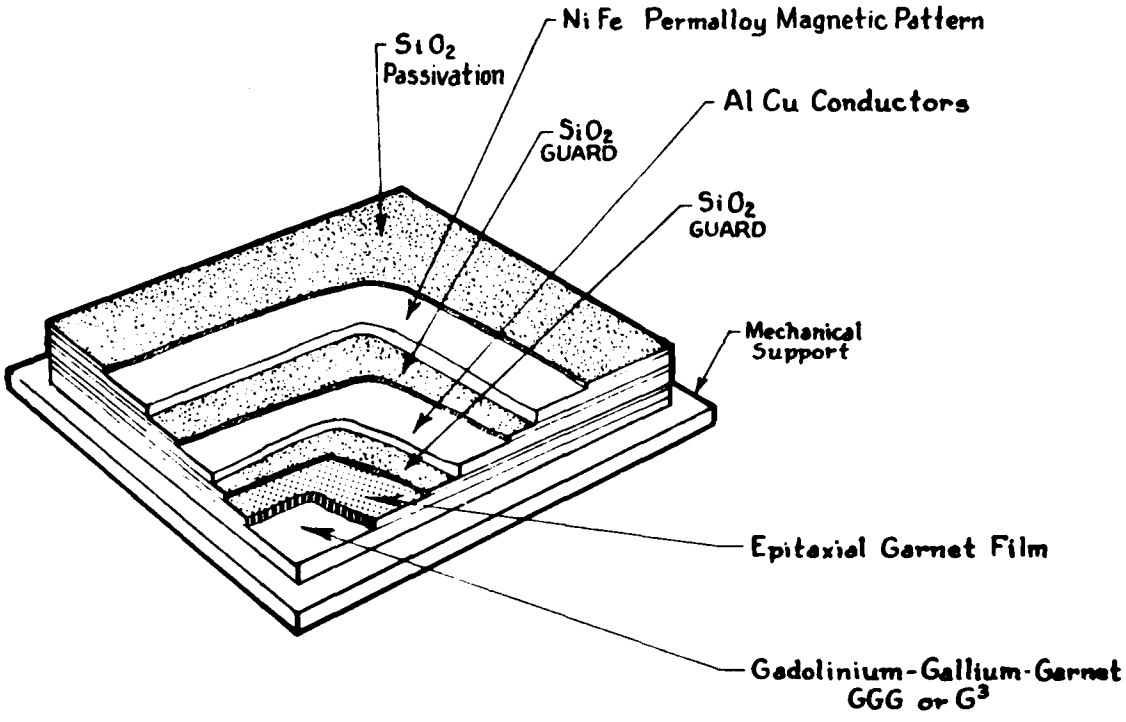
Although each manufacturer's construction is unique, in general, the basic constructions are similar to each other. Most of the individual manufacturer's uniqueness lies in the specifics of the process steps and in the chip and total memory architecture. Choices of coding to select minor loops, organizational grouping of minor and major loops, and read/write functions are the variable parameters of the memory architecture.

As shown in Figures 4 through 8, a Gadolinium-Gallium Garnet (G^3) substrate is coated with an epitaxial film of iron garnet in a lattice structure followed by a silicon dioxide (SiO_2) protective layer. Contact areas of Aluminum-Copper (AlCu) are deposited by a photolithographic process, and then a protective insulating layer of SiO_2 is added. The permalloy Chevron, the I-, or the Tee-structure is applied by photolithography and a final passivating layer of SiO_2 added. Contact areas to the pads are etched out and the total structure annealed prior to chip scribing and separation.

The chips are mounted on a substrate that in many cases is a printed circuit (PC) board. The chip contact areas are wire bonded to the PC contact areas. The orthogonal coil assembly is mounted around the chip/PC board assembly and bonds carried from the coils to the PC board as in Figure 9. A lead frame is attached prior to the assembly of the permanent magnet structure bias field and a magnetic shield. The magnets are adjusted for optimum bias field via access holes and the completed assembly is encapsulated. (See Figures 10 through 13.)

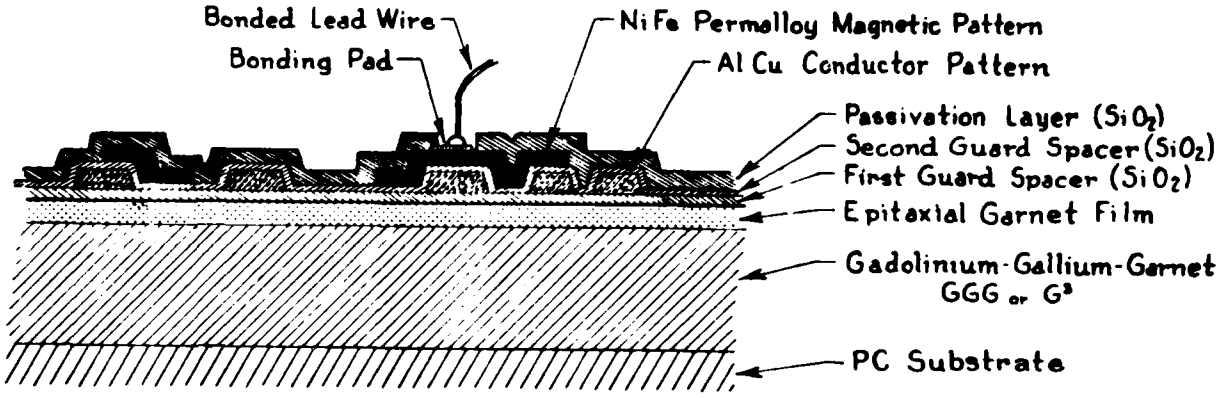
C. MAJOR/MINOR LOOP

The individual data bits are stored in circulating minor loops. Depending upon the organization of the individual manufacturer's chip architecture, these loops can store on the order of 256 to 1,000 bits of data each. To enter data, or to retrieve data from a selected minor loop the data are temporarily transferred, in a nonvolatile and nondestruct transfer, to a major loop. Read and write functions are performed on the circulating major loop and the data transferred back to the appropriate minor loop.



MATERIAL LAYERS
OF MAGNETIC BUBBLE MEMORY CHIP

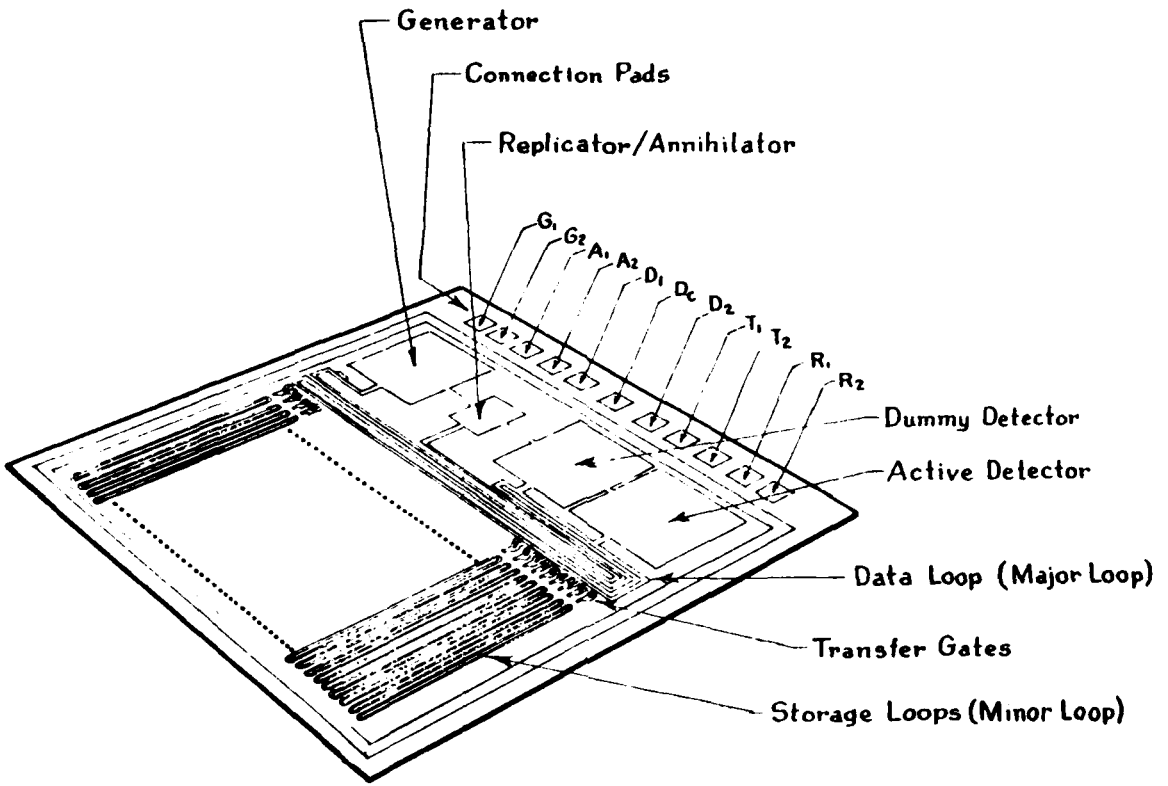
Figure 4



CROSS-SECTIONAL VIEW

OF MAGNETIC BUBBLE MEMORY CHIP

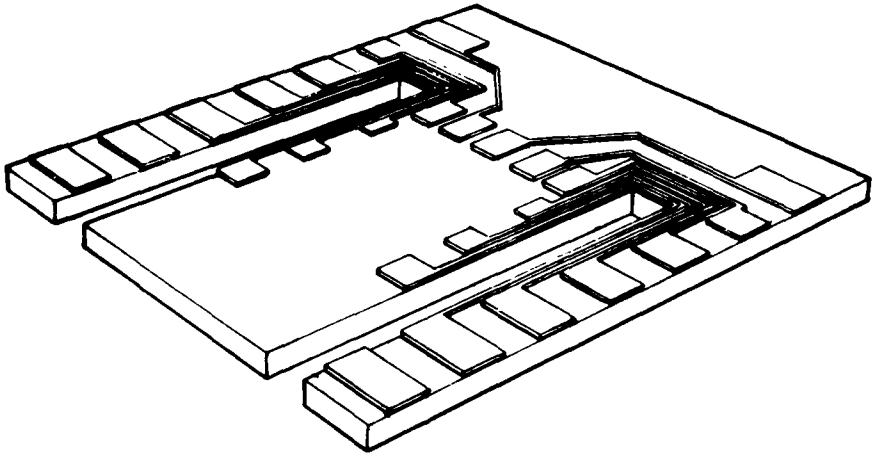
Figure 5



LAYOUT OF ELEMENTS

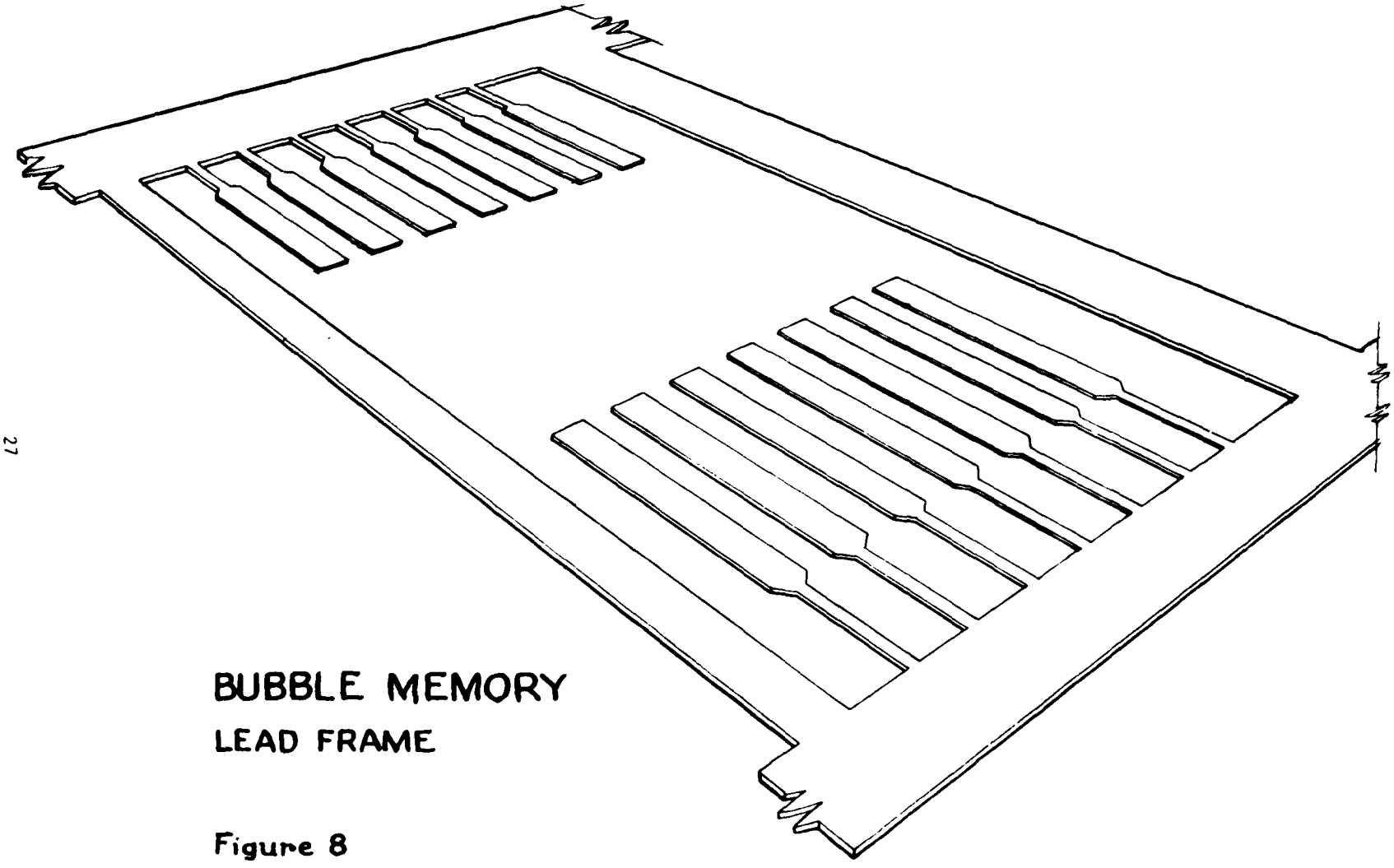
MAGNETIC BUBBLE MEMORY CHIP

Figure 6



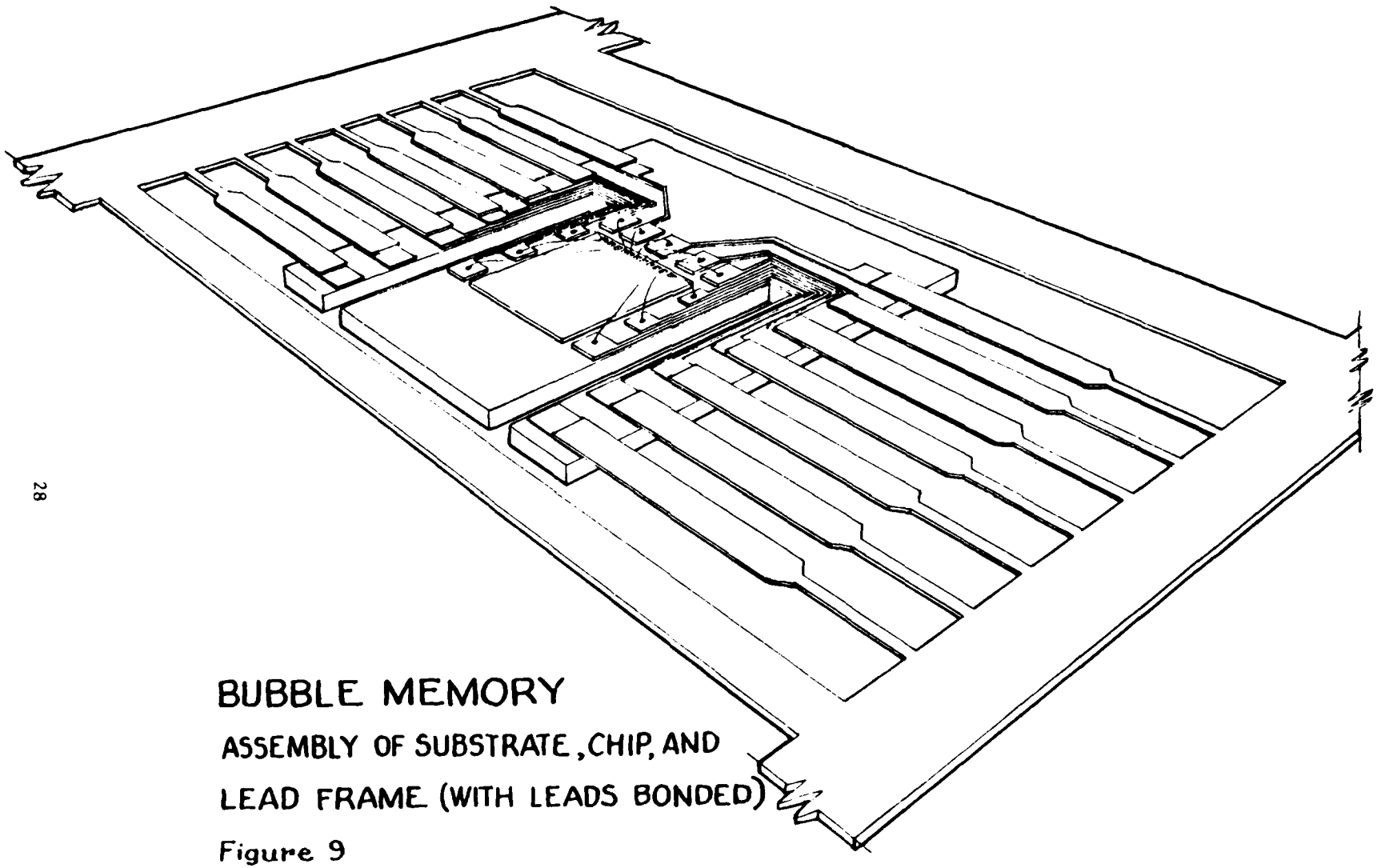
BUBBLE MEMORY
PRINTED CIRCUIT SUBSTRATE

Figure 7



BUBBLE MEMORY
LEAD FRAME

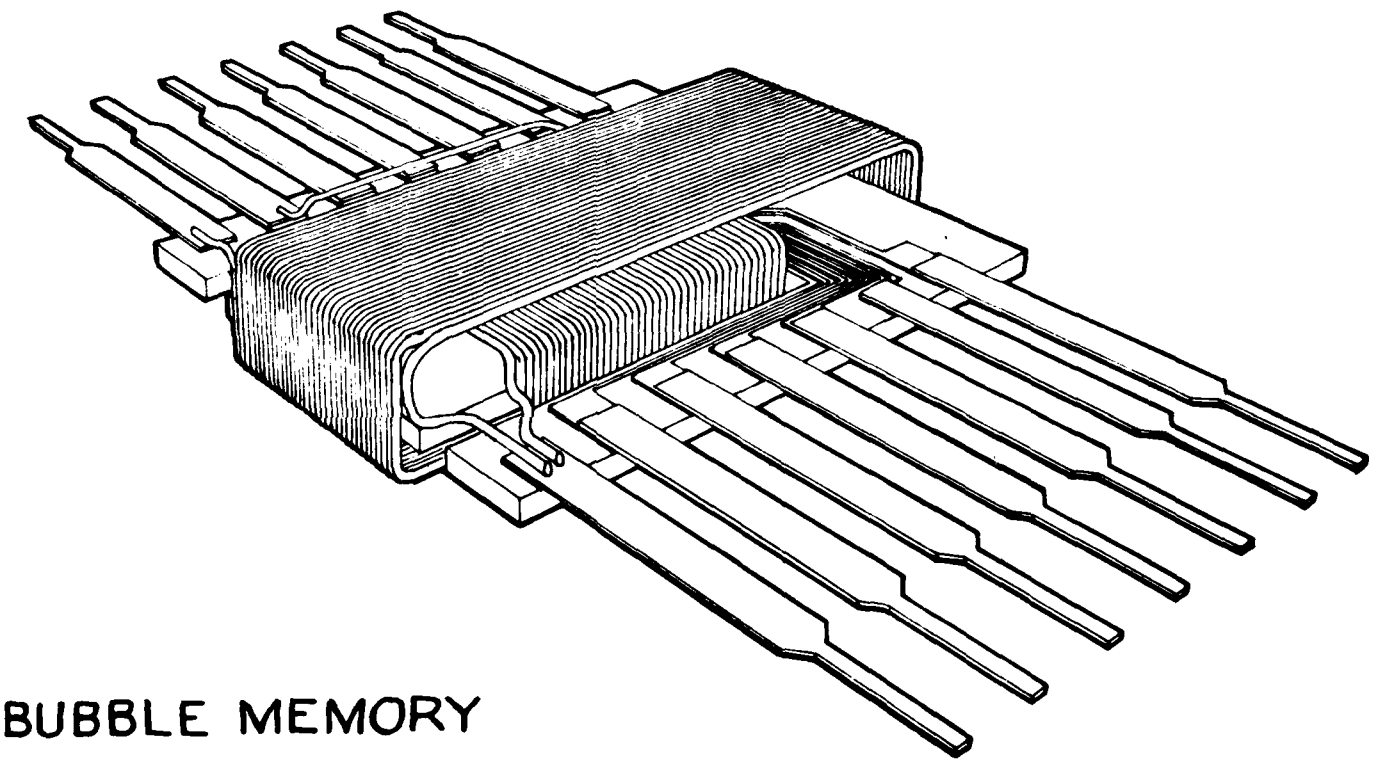
Figure 8



BUBBLE MEMORY

ASSEMBLY OF SUBSTRATE, CHIP, AND LEAD FRAME (WITH LEADS BONDED)

Figure 9

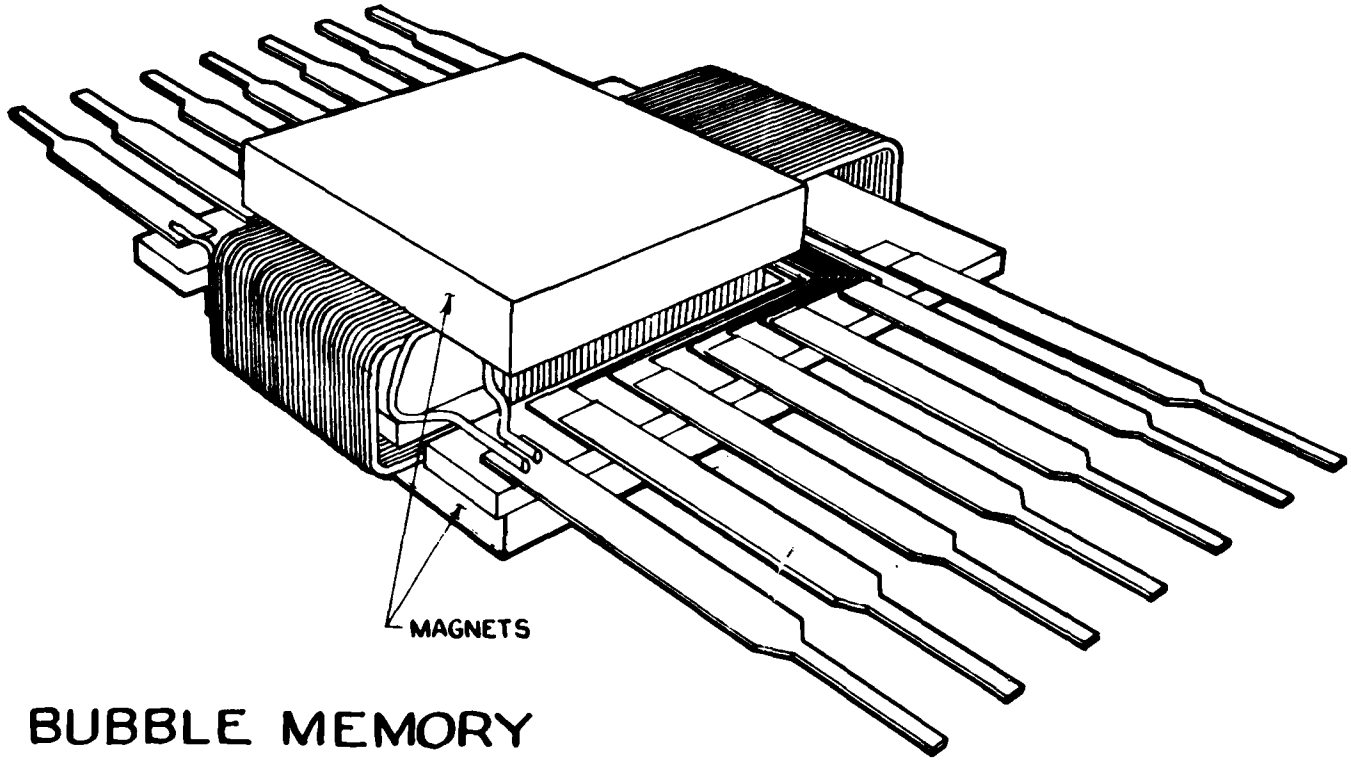


BUBBLE MEMORY

LEAD FRAME TRIMMED AND

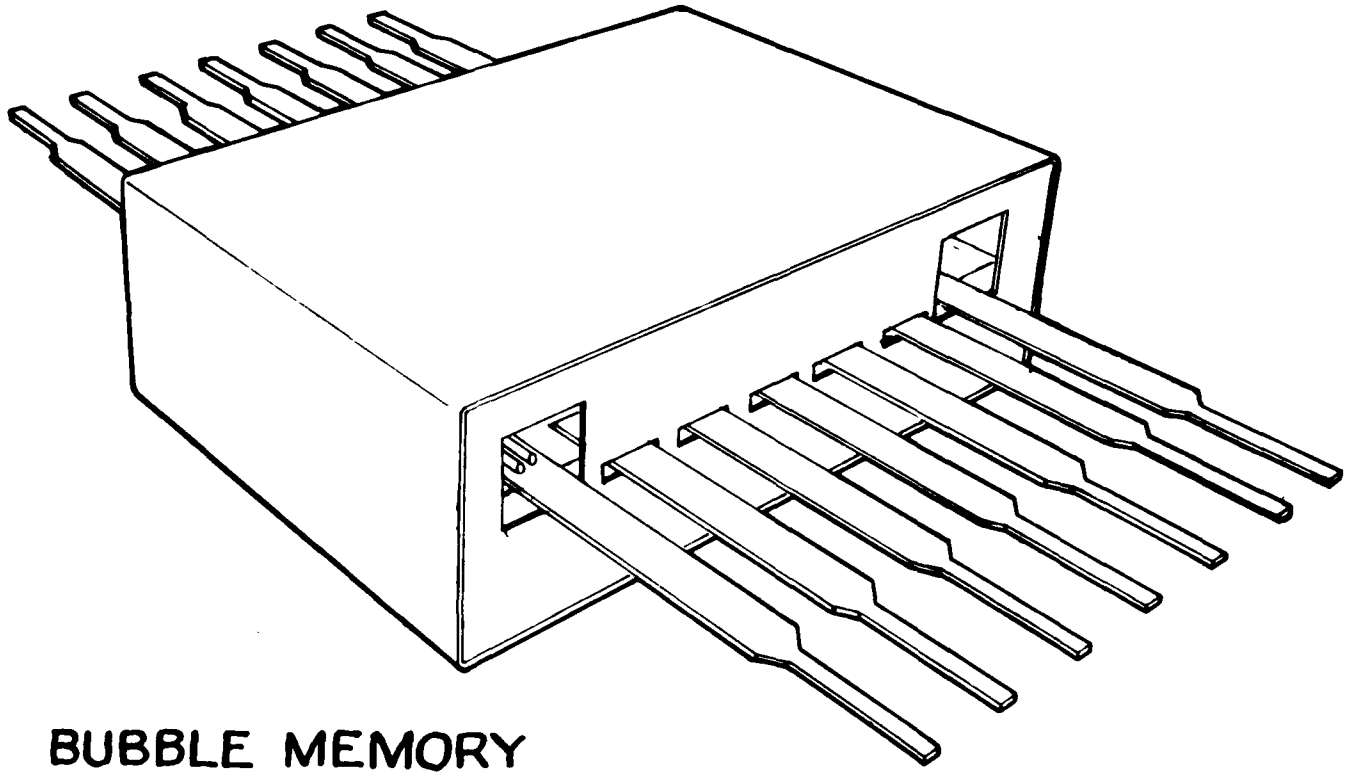
ORTHAGONAL COILS INSTALLED

Figure 10



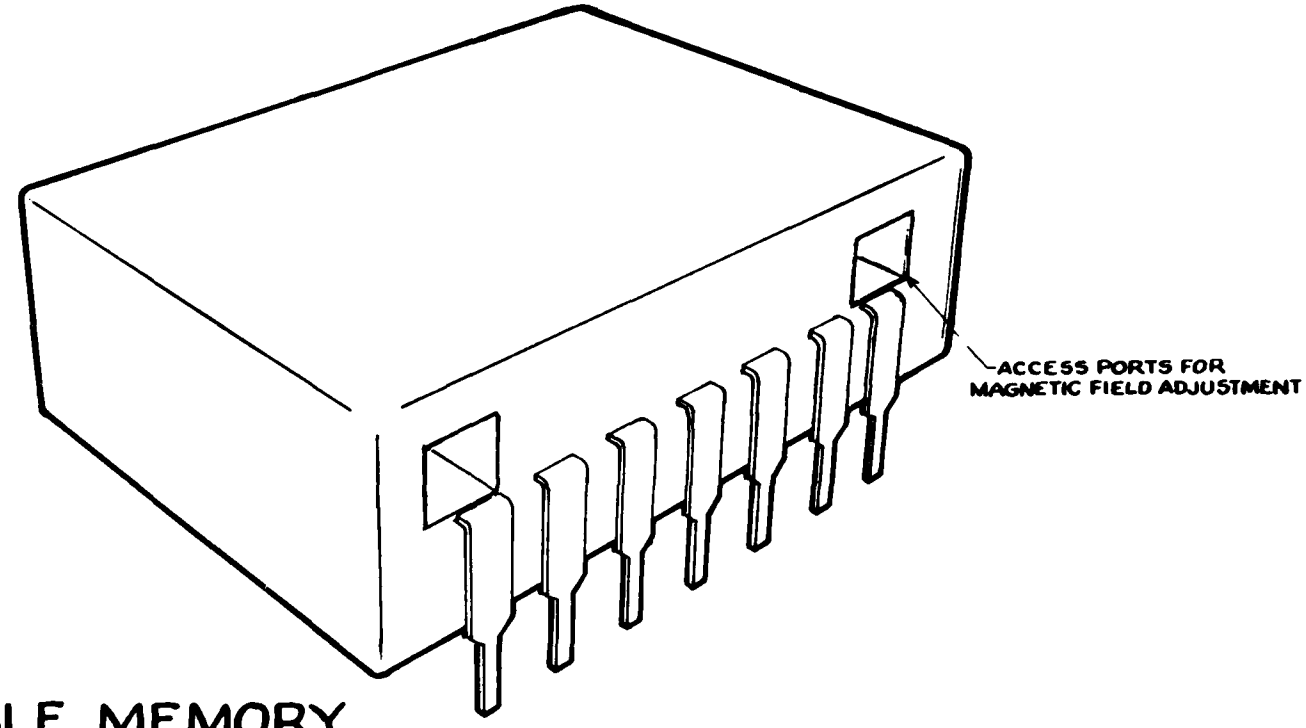
BUBBLE MEMORY
MAGNETS INSTALLED

Figure 11



BUBBLE MEMORY
MAGNETIC SHIELDS
INSTALLED

Figure 12



BUBBLE MEMORY
ENCAPSULATED
AND LEADS FORMED

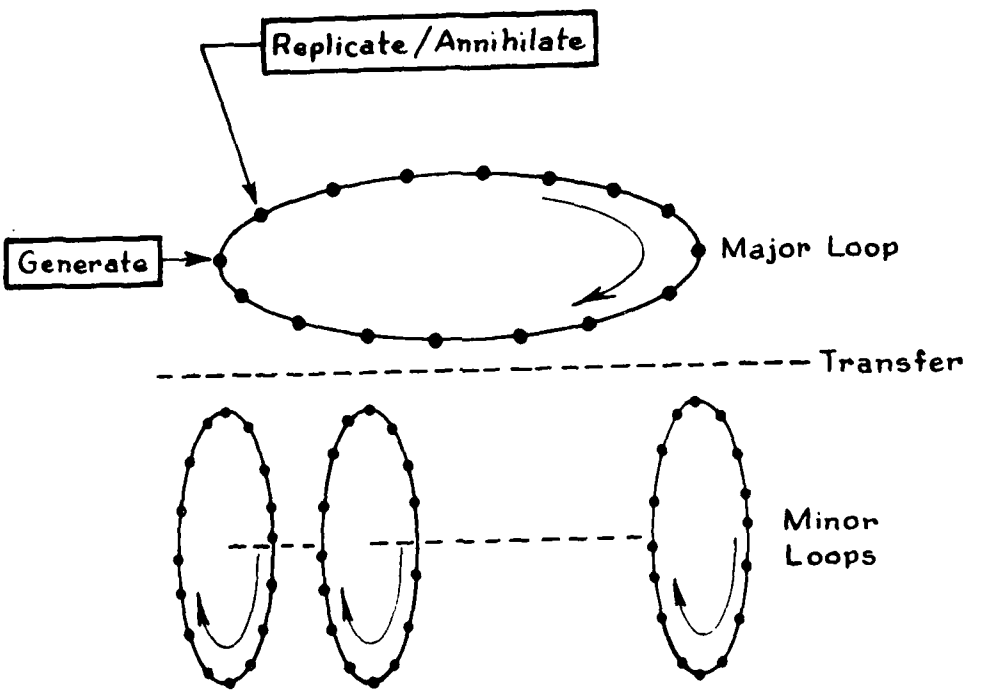
Figure 13

The process of transferring from minor to major loop in some popular chip architectures can be described as a serial-parallel-serial organization of minor serial shift registers. Data are generated serially into a major loop shifted into position over a reference area of the minor loops. The data are then transferred in parallel to the minor loop for storage. The procedure is reversed for data read out. The data are transferred to the major loop in parallel and are clocked serially through a detector (Figure 14).

The general approach allows a reasonably fast access time to data at any location. Access times on the order of 5 milliseconds (ms) to 10ms and data rates of 100 kilobits per second (kbps) are nominal. Of greater importance is the capability to map the semiconductor chip to identify defect areas and delete them from the memory organization at a nominal loss of storage capacity, but at a major increase in yield. The wafer chip size and density is such that only by the mapping mechanism is a useable yield practical in everyday production.

D. MAGNETIC FIELD OPERATION

The magnetic bubble domains are formed in the magnetic epitaxial film in a plane perpendicular to the nonmagnetic substrate. These domains are formed by an orderly arrangement of magnetic fields. The external field provides a "bias" energy level to develop the bubble domains. Specific location and movement of these domains is accomplished by a local alteration of the bias field. A polarized magnetic domain, or bubble, is shifted or moved along a race track route of magnetic segments. When modulated by an external alternating magnetic field, the magnetic bit polarity of the segments is inverted with each cycle. The effect of this alternating magnetic polarity is that of data movement along the path defined by the magnetic segments.



MAJOR / MINOR LOOP OPERATION

Figure 14

Bubble generation, bubble size and bubble stability are dependent upon characteristics of the material, photolithography of the magnetic pattern, and the strength of the bias field. The optimum bubble size for a particular material and pattern is approximately equal to twice the thickness and equal to the ratio of energy per unit area of the domain wall to the saturation magnetism ($d \simeq 2h = \frac{2\sigma}{\P M_s^2}$ where d = diameter of bubble, h = thickness, σ is the energy per unit area and $4\P M_s$ is the saturation magnetism). The external field required to sustain a stable bubble is the bias. In general, a higher bias level is required for the smaller bubble diameters, but stability of the bias field is about 10% to 12% of the nominal level. The saturation magnetism is influenced by temperature, and the allowable margin of bias limits is a function of the temperature range of operation. Over a range of 70°C bias margin limits of 10% to 12% are generally realizable, but over a wider temperature range such as the 110°C often specified for Military applications the allowable bias margin shrinks.

Original chip design data and recommended operating limits should take into account these required control parameters. If a device is operated within some margin limit of about 80% of the combination of all control limits, then reliable operation is attainable.

III. MAGNETIC BUBBLE MEMORY FAILURE RATE MODEL

A. DEVICE TEST DATA

A Magnetic Bubble Memory system is relatively new, and there is little field data at this time which we can use as a basis for describing or predicting probable operating reliability. Some of the data that have been reported have been for a total system and not the basic memory device. Device operating reliability statistics have been difficult to obtain, and much of the data have been more qualitative than quanitative. Because of the large scale of memory capacity much of the reliability reporting has been in the error rate of memory retention and read-out.

In a test of a 2 Megabit (Mbit) Magnetic Bubble Memory* structure with thirty-two 64 Kilobit (Kbit) chips, an analysis was made of a probable failure rate. Bias margins were varied over a range that was calculated to simulate more than 20 years' operation and cycled over the temperature range from -10°C to 50°C to stress the magnetic parameters. The read-error rate was less than 9×10^{-12} /read.

Another classification of performance or reliability is the soft error rate, a phenomenon which is not as easily classified, measured or compared, but one which is a practical problem of the management of large-capacity memories. Soft errors may be defined as random, non-recurring single-bit errors, some of which may be accounted for by software manipulation. Soft errors may be caused by a combination of noise, data pattern sensitivity, and/or marginal operating conditions.

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*2-Mbit Magnetic Bubble Memory
Tsuboya, et al., IEEE Transactions on Magnetics, Sept. 1977.

A manufacturer* tested more than 200 Magnetic Bubble Memories over a wide range of environmental conditions. These acceletated tests were in accordance with MIL-STD-883A, as applicable. The devices tested were 93-Kbit memories and the criteria for failure were of two classes. A catastrophic failure was defined as a continuity failure such as an open or shorted element. Function failures were defined as repeatable 1-bit or more-than-1-bit errors out of 10^6 bits, or a failure to retain stored data. Soft errors were not classed as errors for this series of accelerated tests.

Of the more than 200 devices tested, for a total of over 100K unit hours, only two devices failed catastrophically: one wire bond separated from a pad; and at extreme low temperatures (-40°C), one unit had a shift of the magnet structure during the test of data retention. Five devices had a repeatable functional error during the test series. From the test results it was estimated, with a 60% confidence level, that in an application of 6.8×10^7 bits per year, the failure rate is approximately 0.001 part per 10^6 hours at 50°C.

The data in a magnetic bubble memory are the predictable presence or absence of a magnetic domain or "bubble" in a location, at a particular instant in time. Much concern has been expressed that the materials may have a wear-out characteristic. A series of tests** has shown that error-free operation of long-time exercising of the order of 10^{15} bubble steps is realizable. At data rates up to 100KHz the bias field may decrease, but can be controlled to allow error rates as low as 10^{-20} per step.

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*Texas Instruments Reliability Report T1B0203, June 1979.

**"Long-Term Propagation Studies in Magnetic Bubble Devices," P.W. Shumate, et al., Bell Laboratories, Murray Hill, NJ 07974.

"Lifetime Characterization of Propagated Bubble Data Streams," P.W. Shumate, et al., Bell Laboratories, Murray Hill, NJ 07974.

The results of an extensive testing* of more than 800 68-Kbit magnetic bubble memory chips configured into 200 memory systems indicate that the device may have a high degree of reliability. In general, the majority of Magnetic Bubble Memory devices are in non-hermetic packages. In the end-use system, it is common practice to put two or more of these packages in a single hermetic package. Even then, there are the familiar problems of integrated circuit reliability. Losses are largely attributed to mechanical faults such as loss of a bond, or weakening of a conductor track accelerated by a package leak. The major problems of the bias-margin limits are to a large extent compensated for by early characterization of the device limits and control of the bias margin over the expected operating range. This is practical for individual systems where only a few chips are used, and where the extra care and engineering attention is warranted. For large-scale reproducible general-purpose applications, this may not be feasible.

From this study, for this particular design, a bias margin of ±12 Oersteds (Oe) was required for acceptable reliability. Of the units 10% failed this criterion; 11% of the units were outside the limits of a nominal 40 Oe drive field; and the remaining 75% to 80% of the units were packaged for field use. Of this group, another 35% failed final qualification tests.

A two-year test** of a 0.5-Mbit capacity Magnetic Bubble Memory system demonstrated a capability to operate reliably with a read-failure rate of 1.9×10^{-12}/read. This test was performed in a somewhat benign environment which simulated a real-use condition

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*"Magnetic Bubble Testing," F. B. Hagedorn, et al., IEEE Transactions on Magnetics, Sept. 1978.

**"Tests for Magnetic Bubble Memory," N. Yamaguchi. IEEE Transactions on Magnetics, Sept. 1978.

rather than the usual accelerated stress functions. No significant changes were noted in the bias field or magnetic structure during the test period, of which approximately one-half was operating time for the memory device. A variety of special test programs and environmental conditions were imposed on the devices. Operating bias margin limits were verified several times during the test and no significant changes were noted.

Typical of current production units are those reported by a manufacturer in 1979.* A life-testing program has been completed on a 1-Mbit Magnetic Bubble Memory. This unit is a series parallel unit with 320 parallel data loops, 48 of which are reserved for manufacturing defects, and 16 are used for error correction codes. The system has a capacity of 128 Kbytes (1 byte = 8 bits) or 1,048,576 bits. A read error rate of 10^{-9}/read is predicted. This equipment points up one of the typical problems confronting an analysis of the Magnetic Bubble Memory system. At these bit densities and capacity, on the order of 10^{6} bits, only a few units are fabricated and testing is of the product-acceptance rather than stress-level type. Only infant mortality-type data are available; the remainder are projections.

B. PERMALLOY CORROSION AND ELECTROMIGRATION

Use of permalloy iron-nickel alloy elements in Magnetic Bubble Memory devices is widespread, but there is some concern that corrosion of the thin (~ 0.45 μm) elements may lead to premature failure. The likelihood of this may be assessed in an examination of the behavior of such devices, or their thin-film components in a corrosive atmosphere, and what might be predicted from work published on the alloy in bulk.

A useful published work on corrosion of thin films of permalloy is that of Gangulee et al.* In this work, 0.02- μm permalloy films were heated to 250°C with and without the presence of air, and were shown to oxidize to the point of magnetic failure in 100-200 hours if air was present. However, coatings of 0.5 μm Silicon Oxide (SiO), Silicon Nitride (Si_3N_4) or Aluminum Oxide (Al_2O_3) all protected the devices from degradation for the entire test period of 500 hours. While some concern was voiced that SiO or Al_2O_3 might be water-permeable under extreme moisture conditions, some samples coated with 0.5- μm Al_2O_3 survived more than 1-1/2 years at 250°C, while passing a current equivalent to 10^7 amperes per square centimeter (A/cm^2). Other test specimens coated with Si_3N_4 and SiO were boiled in water for 50 hours without ill effects from this rather extreme treatment.

"Bulk" iron-nickel alloys have been reported by Pettibone to exhibit corrosion resistance better than that of pure nickel.** Thinning of specimens of 80% nickel, 20% iron, indicate loss through smooth corrosions with no pitting of only about 10 μm in ten years of exposure to an industrial atmosphere. If this is presumed to be a linear function with time, then it supports qualitatively the work of Gangulee on thinner films. Pettibone also refers to earlier work suggesting that if the sample is kept in a benign environment or coated lightly, corrosion "may be entirely absent."

From these references, one may anticipate the following:

- 0.45- μm permalloy films exposed to air at 250°C may fail within one year.
- 0.45- μm permalloy films exposed to an "industrial atmosphere" may fail within one year.

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*"Long-Term Stability of Magnetoresistive Bubble Detectors," A. Gangulee, et al., IEEE Transactions, April 1974.

**"Nickel Iron Alloys," J.S. Pettibone. Corrosion Resistance of Metals and Alloys, Reinhold Publishing Corp., New York.

- 0.45- μm permalloy films protected with 0.5- μm Al_2O_3 should tolerate exposure to an industrial atmosphere for several years unless extreme temperature and humidity conditions prevail.
- 0.45- μm permalloy films protected with SiO or Si_3N_4 should be free from corrosion under the most severe conditions imaginable for many years.
- Other easily applied coatings such as plastic films and protective housings may also give added protection.

The conductor film layer for read/write control current loops and magneto resistive bridge elements is deposited between the epitaxial film and the permalloy strips. Insulating layers of SiO_2 separate the conductor pattern from the permalloy and the epitaxial layer. The current requirements of the loop may be in excess of 10^7 A/cm^2. A potential failure mode may now exist from electromigration effects. The aluminum conductor layer usually contains 4% copper to reduce the probability of migration, but the high current density level may be a problem.

J. E. Davies of Intel Magnetics has completed a study* on the electro migration in Magnetic Bubble Memory structures and has concluded that because of the low duty factor of less than 1% and the use of 4% copper in the aluminum conductor material that an MTTF in excess of 100 years is reasonable even operating at 70°C.

In this same study the question of intermetallic interdiffusion and chemical reaction was evaluated in the case of gold bond wires on Cu-Al conductors. No measureable decrease in bond strength was noted after aging of 240 hours at 200°C. At an activation energy

*"The 7110, a one Megabit Magnetic Bubble Memory Reliability Report RR-22; J.E. Davies, Intel Magnetics, Santa Clara, CA 95051 Sept. 1979.

level of 0.8 eV the aging time of 240 hours at 200°C extrapolates to 30 years at 70°C chip temperature. The validity of the exact activation level and the errors possible in long lifetime extrapolations may be a question, but the general trend is comparable to other banding techniques to a degree as to give rise to some optimism that with adequate care and control this is a viable interconnect technique.

Current densities of $10^7 A/cm^2$ applied to small geometry thin film aluminum conductor patterns can cause early failures because of the inability of the conductor to dissipate this level of energy. Intermittent application of high density currents of this order of magnitude may reduce the problems of gross heat dissipation, but may introduce new problems of local hot spot degradation and fatigue or metallic degradation induced by repetitive temperature excursions. The indications by several studies* are that the time to failure may increase rapidly with current densities greater than 2×10^7 A/cm^2 as a function of duty cycle and repetition rate. At pulse widths of 0.1 μs, repetition rates of 100 KH_z and current densities of $2.8 \times 10^7/cm^2$ failures start to occur. A small reduction of the current density towards 10^7 A/cm^2 reduces the local heating to a level as not to be a major detriment to long-term reliability.

*Failure of Small Thin film Conductors due to High Current Density pulses. E. Kensbrou et al. Bell Laboratories 1978.

C. CALCULATED RELIABILITY OF SEMICONDUCTOR MEMORY DEVICES

The reliability handbook MIL-HDBK-217C (Proposed Notice 1) provides guidelines for estimating the reliability of memory devices. These guidelines were developed and verified from field data on relatively low-density devices. Not much field data have been available on the large-scale integrated circuits and the calculations for these devices are still unproven. This is a similar problem that is being investigated for Magnetic Bubble Memory Devices.

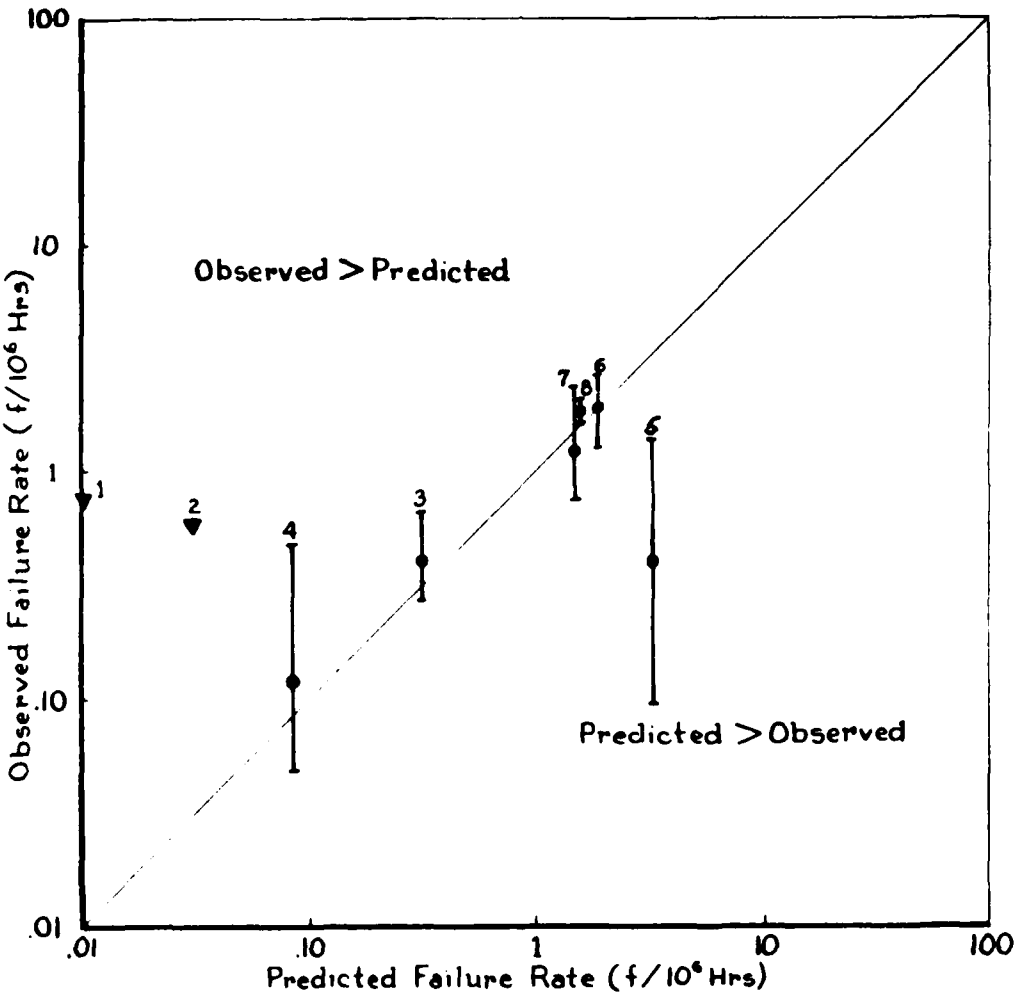
The leverage and sensitivity of certain of the parameters of the calculations become more significant with the increase of bit capacity as well as the increase of bit density. The basic reference philosophy for the categories and characterization of many of the parameters is that the devices being evaluated are part of a large population and that the devices are produced and procured within specific guidelines. These assumptions set bounds on the data developed rather than to restrict the design or acquisition of the devices. General experience has shown that deviations from these prescribed conditions cloud the data and reduce the confidence level of the accuracy of prediction. These deviations are not necessarily a cause of reduced reliability, but because of the lack of control it is assumed that -- in general -- for a wide sampling, a major decrease in reliability could be expected, particularly if the wide range of environmental conditions is expected. It is rational to expect that for a narrow sample, and for restricted environmental or applications conditions, modifications to the base parameters may be justifiable. This concept is a major consideration in the rationale for the judicious use of the MIL-HDBK-217C (Proposed Notice 1) guidelines in large-scale integrated circuit memory devices and, until more definitive data are available, will also be applicable to some of the recommendations for Magnetic Bubble Memory calculations.

In a report by the ITTRI Reliability Analysis Center* in 1979, a comparison was made between actual field data and calculated values of predicted failure rates for memory devices. (See Figures 15 and 16 and Tables 2 and 3.)

To illustrate the effect of certain of the basic parameters on a predicted reliability, the results of a few sample calculations are listed in Table 4. From a general statistical viewpoint the impact of memory density on reliability is a controversial subject. Semiconductor defects are random; even with the utmost care in the process, some defect density will exist. With an increase in the number of IC elements there is the increased possibility that one of these defects will interfere with an active element. The general experience of large-scale integration is that as the bit quantity increases, the trend is to increase the bit density to control substrate area growth. Conversely, as the density increases because of reduced element size and improved layout efficiency, smaller defects in the substrate can cause catastrophic failures.

Calculations of memory device reliability with the guidelines of MIL-HDBK-217C (Proposed Notice 1) correlate to available field data at memory sizes up to about 4096 bits. This is illustrated in Figures 15 and 16. For memory capacity up to 65,536 bits additional calculations have been made as listed in Table 4. This data is presented to establish a reference for comparison of the reliability calculations of a Magnetic Bubble Memory or Charge-Coupled Device memory from the models recommended in this report.

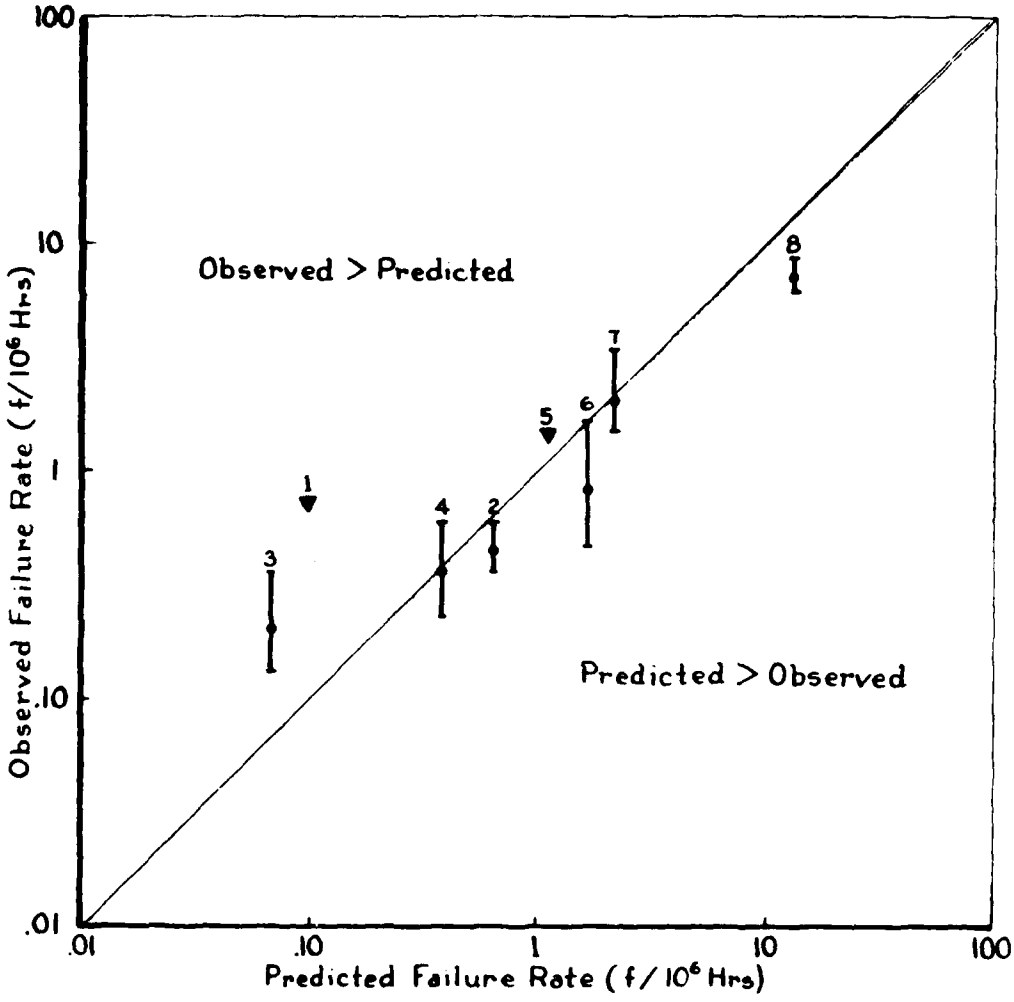
*LIS/Microprocessor Reliability Prediction Model Development RADC-TR-79-97



Source:
RAC
RADC - TR-79-97

MOS DYNAMIC RAM AND SHIFT REGISTER OBSERVED FAILURE RATES VS PROPOSED MODEL PREDICTED FAILURE RATES

Figure 15



Source:
RAC
RADC-TR-79-97

MOS STATIC RAM AND SHIFT REGISTER OBSERVED FAILURE RATES VS PROPOSED MODEL PREDICTED FAILURE RATES

Figure 16

TABLE 2

MOS DYNAMIC RAM AND SHIFT REGISTER DATA

Device Description					Application Description					Failure Rates ($\lambda/10^6$ Hours)				
Entry No.	Technology	Bit Complexity	Package	No. Pins	T_j(°C)	Screen Class	Application Env.	Device Hours (10^6)	No. Failures	Observed 20% C.L.	Observed Point Estimate	Observed 80% C.L.	Predicted* MIL-HDBK-217B	Predicted RAC Model
1	PMOS	50	CAN	10	35	S	SF	1.963	0	--	--	0.82	0.01	0.01
2	PMOS	128	CAN	8	35	B-1	GF	2.761	0	--	--	0.58	0.06	0.03
3	PMOS	320	CM-DIP	16	60	D	GB	16.486	7	0.29	0.42	0.62	8.97	0.34
4	PMOS	1024	CAN	8	50	B-1	NS	16.354	2	0.05	0.12	0.26	0.75	0.09
5	NMOS	2048	PL-DIP	16	55	D-1	GB	2.290	1	0.10	0.44	1.31	37.92	3.40
6	PMOS	2048	C-DIP	14	65	D	AIF	4.851	9	1.33	1.86	2.58	59.93	1.82
7	NMOS	4096	CM-DIP	16	60	D	GB	3.110	4	0.74	1.29	2.16	42.27	1.50
8	NMOS	4096	CM-DIP	22	60	D	GB	100.000	174	1.63	1.74	1.87	42.27	1.54

*Predictions Using Notice II Dated 17 March 1978.

TABLE 3

MOS STATIC RAM AND SHIFT REGISTER DATA

Device Description					Application Description					Failure Rates ($\lambda/10^6$ Hours)				
Entry No.	Technology	Bit Complexity	Package	No. Pins	T_J(°C)	Screen Class	Application Env.	Device Hours (10^6)	No. Failures	Observed 20% C.L.	Observed Point Estimate	Observed 80% C.L.	Predicted* MIL-HDBK-217B	Predicted RAC Model
1	PMOS	256	CM-DIP	16	45	B-1	NS	2.600	0	--	--	0.62	0.28	0.10
2	PMOS	320	C-DIP	16	55	D	GF	114.011	52	0.40	0.46	0.53	7.41	0.58
3	NMOS	1024	C-DIP	16	40	B-1	GB	29.670	6	0.13	0.20	0.31	0.14	0.07
4	NMOS	1024	C-DIP	16	40	D	GB	61.510	26	0.35	0.42	0.51	4.33	0.42
5	NMOS	1024	S-DIP	16	40	D	GB	1.168	0	--	--	1.38	8.66	1.17
6	NMOS	1024	S-DIP	16	40	D	GF	4.480	4	0.51	0.89	1.50	14.42	1.64
7	PMOS	2048	C-DIP	18	65	C-1	AIF	3.850	8	1.45	2.08	2.96	35.96	2.16
8	NMOS	4096	E-DIP	22	60	D	GB	85.440	594	6.71	6.95	7.20	82.29	13.00

*Predictions Using Notice II Dated 17 March 1978.

A 1024-bit memory screened to a vendor equivalent of MIL-STD-883, Class B, as defined by MIL-HDBK-217 (Class B-2) may have a predicted failure rate of 0.19 parts per 10^6 hours. A 65,536-bit memory under the same conditions would have a predicted failure rate of 1.95 parts per 10^6 hours. For a capacity increase of 64 times the predicted failure rate is increased 10 times. This is to emphasize that although the probability of failure will increase with greater bit capacity or element count the relationship is not linear.

D. CALCULATION OF SEMICONDUCTOR MEMORY FAILURE RATE

$$\lambda p = \pi_Q[C_1\pi_T\pi_V + (C_2 + C_3)\pi_E]\pi_L*$$

Where:

π_Q = A quality factor based on the process handling, production screening and adherence to the Military procurement guides of MIL-M-38510. For a fully screened and qualified part the multiplier is 0.5. High-reliability hermetic commercial vendor equivalent components have a multiplier of 6.5 and nonhermetic parts have a multiplier of 35.

$C_1 + C_2$ = Circuit complexity factors that take into account a scaling for bit or element density.

π_T = A temperature acceleration factor based on technology. This is a very critical factor and careful consideration must be given to these calculations. Large-scale devices with high bit density may tend to have high junction temperatures and a detrimental effect on reliability.

*MIL-HDBK-217C, Notice 1 Section 2.1.4

π_V = A voltage derating stress factor based on general industry experience. In the case of the Magnetic Bubble Memory this factor has no precedence or experience so a comparative judgement will be necessary.

C_3 = A package complexity factor to take into account the probability of interconnection failures.

π_E = The application environment factor. In general, most of large-scale memory devices are in the ground benign category except for a grouping of specific airborne or space applications for memory.

π_L = The device learning factor where the experience curve of large-scale production is taken into account. Many of the extreme-high-capacity memory devices are made in short lots or under special or custom conditions. It is difficult to judge the comparative quality of a well developed production process versus a hand crafted small lot of devices by highly skilled workers. In between are the more loosely controlled units being fabricated while process controls, limits, and experience are being developed.

TABLE 4

CALCULATED FAILURE RATES OF SEMICONDUCTOR MEMORY DEVICES

Memory Size (bits)	Screening Level	Calculated Failure Rate λp* (Parts per 10^6 Hours)
1,024	S	0.014
	B-1	0.087
	B-2	0.19
	C-1	0.38
	D-1	1.02
16,384	S	0.07
	B-1	0.40
	B-2	0.86
	C-1	1.72
	D-1	4.62
65,536	S	0.15
	B-1	0.9
	B-2	1.95
	C-1	3.9
	D-1	10.5

*MIL-HDBK-217C,(Proposed Notice 1) Section 2.1.4

E. FAILURE RATE MODEL DEVELOPMENT

The Magnetic Bubble Memory device in its present form is an assembly of two major structural segments: (1) a basic memory and control structure consisting of thin-film elements on a crystalline substrate, and (2) a magnetic structure to provide a controlled magnetic field, consisting of a magnet, magnetic coils and a housing. These two major structural segments of the hybrid are interconnected by a mechanical substrate and lead frame. The interconnect substrate in present technology is normally a printed circuit board.

It is quite evident that in the reliability analysis of the total device the general form of a hybrid model must be considered. This general form is then expanded to take into account the unique trends of each of the component parts when subjected to the time, temperature, and environmental stresses of the application.

The basic form as used in the reliability handbook MIL-STD-217 for semiconductor devices is:

$$\lambda_p = \lambda\pi$$

where:

λ_p = The device failure rate as a constant over time. Failures are catastrophic or drift in nature.

λ = Device-related failure parameters.

π = Environmental and use factors relating to the application, process, and design.

For a hybrid structure the failure rate is a summation of the reliability of the individual segments of the hybrid. Field experience is available for correlation with the theoretical calculations for some of the segments of the Magnetic Bubble Memory. For others, some interpolation and judgment based on a comparable process or condition must be used until more definitive data becomes available.

The general form of the overall Magnetic Bubble Memory device is as follows:

$$\lambda_p = \lambda_1 + \lambda_2 + \lambda_3 + \lambda_4$$

where:

λ_p = Failure rate of a Magnetic Bubble Memory in parts per 10^6 hours.

λ_1 = Failure rate of the control sense and driving sector.

λ_2 = Failure rate of the memory sector.

λ_3 = Failure rate of the interconnect substrate and structure.

λ_4 = Failure rate of the inductive structure.

1. Thin Film Structure

From the concepts of the reliability handbook MIL-HDBK-217 a monolithic device, failure rate is of the additive form:

$$\lambda_p = \lambda_T + \lambda_M$$

where:

λ_p = Overall monolithic device failure rate in parts per 10^6 hours.

λ_T = Failure rate due to time, temperature stress and electrical bias related degradation.

λ_M = Failure rate due to environmental stress effects and from mechanical or fabrication processes.

The thin-film structure of a Magnetic Bubble Memory device is in two parts: (1) the memory sector is a pattern of magnetic elements arranged in data loops and deposited over an epitaxial film layer; and (2) the control, sense, and driving sector is a cluster of conductive elements deposited on the same substrate. This combination of thin-film structures has some similarity to the general form of a semiconductor memory device in that the number of elements and the "packing density" are directly related to the memory capacity. However, there is a significant difference between the two structures. In a general form of semiconductor memory all of the elements, including the memory bits, are active elements. The reliability of these elements is subject to the limitations of junction temperature stress degradation. The number of active elements affected by this class of failure degradation is a direct function of the memory capacity, and so the device failure rate is influenced in a significant manner by the bit capacity scaling of this device. The exact relationship of the capacity scaling to failure rate may be argued, but the trend of an increase in the predicted failure rate with an increase in semiconductor memory capacity is generally accepted as discussed in the previous chapter on semiconductor memory devices and as calculated by the recommendations of MIL-HDBK-217C (Proposed Notice 1).

The Magnetic Bubble Memory device memory elements are not active semiconductor current-dissipating junctions, but are passive magnetic domains whose state is controlled by an external field. In this respect the Magnetic Bubble Memory structure is freed from the limitations of time/temperature degradation related to increases in memory capacity.

a. Conductive Thin Film Elements

The drive and sense circuitry elements of the Magnetic Bubble Memory are current-controlling circuitry and their projected reliability is heavily influenced by the time and temperature stress relationship. The structure is a pattern of read/write control current loops and magneto-resistive bridge elements deposited as Cu-Al conductors between the epitaxial layer and the magnetic permalloy strips. Insulating layers of SiO_2 separate the current handling conductors from the permalloy and epitaxial layers. The reliability of these control functions can be determined by the relationships recommended in MIL-HDBK-217C (Proposed Notice 1) section 2.1.1 to 2.1.6. The general form is:

$$\lambda_p = \pi_Q[C_1\pi_T\pi_V + (C_2 + C_3)\pi_E]\pi_L$$

where:

λ_p = The control element's failure rate in $F/10^6$ hours.

π_Q = Quality factor (Table 2.1.5-1).

π_T = Temperature acceleration factor based on technology (Table 2.1.5-4 through 2.1.5-13).

π_V = Voltage derating stress factor (Table 2.1.5-14).

π_E = The application environment factor (Table 2.1.5-3).

$C_1 + C_2$ = Circuit complexity factor (control devices) based on gate count (Tables 2.1.5-15 to 2.1.5-21.

C_3 = Package complexity (Table 2.1.5-24, values ÷ 2); the chip may only involve 1/2 of the interconnect and not include the overall package. The connection to the lead frame may be via an intervening printed circuit structure and the remaining interconnect mechanism is accounted for in this structure. This is illustrated in Figure 9.

π_L = Device learning factor (Table 2.1.5-2).

b. Memory Elements Structure

The memory segment is a series of repetitive patterns of magnetic elements aligned over the epitaxial film. No direct connections are made to the current or voltage conductors. The energy involved is the changing magnetic fields and the rotating magnetic strip polarity. As in any multilayer thin-film structure, the delineation of a complex fine line pattern is subject to photolithographic defects. The number of screening levels for Magnetic Bubble Memory devices is far less than the multiplicity of steps required for active semiconductor elements and there are essentially no multilayer registration requirements.

The general form of the failure rate model for this part of the memory structure follows the general format of semiconductor devices as recommended in the guidelines of the reliability handbook MIL-HDBK-217. Specific numerical designations for some of the factors cannot be quantified at this time because of the lack of sufficient field data. The nondissipative structure and the reduction of multilayer registration of the Magnetic Bubble Memory structure make it obvious that the numerical designations, such as for the junction temperature stress factor, should be substantially lower than those experienced in active semiconductor memories. With a lack of definitive information on the level of differences that exists, some engineering judgement is applicable. For a minimum derating it is not unreasonable to think of a two-to-one comparison and a maximum may be an order of magnitude value. On this basis we propose a range of 0.5 to 0.1 for a derating factor. An optimistic reliability prediction would use the 0.1 derating; a pessimistic view, the 0.5 derating. In the present state-of-the-art the guideline for derating factor may be related to the bubble size. For bubble sizes of 3 μm or larger the optimistic derating of 0.1 may be applicable and for bubble diameters of less than 3 μm, then a derating of 0.5 may be used. Until more experience and detailed field data is available or developed, this range is recommended. On this basis, the reliability or failure rate calculation for the magnetic memory sector of the thin-film structure is:

$$\lambda_p = \pi_Q[N_1(C_1\pi_T\pi_M + C_2\pi_E) + N_2(C_1\pi_T\pi_M + C_2\pi_E)]\pi_L$$

where:

λ_p = Failure rate of the magnetic memory structure in parts per 10^6 hours.

π_Q = Quality factor (Table 2.1.5-1).

$C_1 + C_2$ = Circuit complexity factor for a dynamic memory such as a single Magnetic Bubble Memory loop either major or minor loop as applicable from Table 2.1.5-21.

N_1 = Number of major loops (a multiplier for the C_1 and C_2 factors for the major loops).

N_2 = Number of active minor loops (a multiplier for the C_1 and C_2 factors for the active minor loops).

π_T = Temperature acceleration factor based on technology and bubble size. There is no junction dissipation and the only temperature factor is the case temperature. The effect of a non-hermetic packaging on the nondissipative permalloy elements is minimal. The π_T tables of 2.1.5-12 are applicable to this sector of the device. To take into account the variations due to bubble size, a modifier of the optimistic 0.1 derating factor is used for bubble sizes of 3μm or larger. For the more critical sizes (less than 3μm in diameter), the pessimistic multiplier of a 0.5 derating factor is used.

π_M = Magnetic bias margin factor. This is in the same class of modifier as the voltage derating factor of active semiconductor devices as defined in Table 2.1.5-14. With no additional information available from field data to more accurately define this parameter, a factor of 1 is used within the restricted use conditions of an operating

bias margin of 80% of the vendor rated bias margin requirements of the lowest case temperature of the application.

π_E = Application environment factor (Table 2.1.5-3).

π_L = Device learning factor (Table 2.1.5).

2. Magnetic Structure

The three functional parts of the magnetic structure are: (1) the magnets, (2) the orthogonal coil structure, and (3) the shield. The magnetic shield protects the total device from outside magnetic influence and contains the magnetic field within the device. This component is quite inert and has no significant contribution to the device failure rate. The static magnetic field source is a permanent magnet and once set to a nominal energy level, determined by the mounting considerations of the design, is stable throughout the general temperature range of interest. There may be a mechanical movement that could result in a catastrophic failure, but this is accounted for in the overall learning factor and environmental factor multipliers for the total device.

The magnetic coils are inductive devices and the failure rate prediction recommendations are applicable to the conditions of MIL-HDBK-217C.

The general form for inductive devices from MIL-HDBK-217C is:

$$\lambda_p = \lambda_b (\pi_E \pi_Q \pi_c)$$

where:

λ_p = Failure rate of the inductive devices in parts per 10^6 hours.

λ_b = A base failure rate of the form:

Ae^x in which $x = \left(\frac{T_{HS} + 273}{N_T}\right)^G$

and T_{HS} = Hot spot temperature in degrees C

N_T = Temperature constant*

G = Acceleration constant*

A = Insulation factor*

π_E = Environmental factor Table 2.7.1-3.

π_Q = Quality factor Table 2.7.1-2.

3. Interconnect Substrate Structure

The recommendations of the reliability Handbook MIL-HDBK-217C for printed wiring board and interconnection failure rates are applicable. The basic form of calculation of the failure rates of a printed wiring board as defined in paragraph 2.12 of MIL-HDBK-217C is:

$$\lambda_p = \lambda_b N \pi_E$$

*These constants are listed in Tables 2.7.1-1 through 2.7.1-14.

The contribution of the printed circuit wiring board to the overall failure rate of a Magnetic Bubble Memory is inconsequential and could be deleted with no impact on the overall calculation. It is identified here for the sake of completeness.

Where:

λ_p = Failure rate of the printed wiring board in parts per 10^6 hours.

$\lambda_b = 6 \times 10^{-6}$ (worse case).

N = Number of connections. (Number of connections to the lead frame plus three for the magnetic structure if no other information is available).

π_E = Application factor of table 2.12.

4. General Form of Failure Rate Model of a Magnetic Bubble Memory Device

The basic premise is that the failure rate of a hybrid structure such as a Magnetic Bubble Memory device is the summation of the failure rates of the individual structures. In this specific case the MBM failure rate is:

$$\lambda_p = \Sigma(\lambda_1 + \lambda_2 + \lambda_3 + \lambda_4)$$

where:

λ_1 = Failure rate of control segments.
λ_2 = Failure rate of memory sector.
λ_3 = Failure rate of magnetic structure.
λ_4 = Failure rate of printed circuit structure and interconnections.

Expanded this will be:

$$\lambda_p = \pi_Q [C_1\pi_T\pi_V + (C_2 + C_3)\pi_E] + [N_1(C_1\pi_T\pi_M + C_2\pi_E) + N_2(C_1\pi_T\pi_M + C_2\pi_E)] \pi_L + \lambda_b(\pi_E\pi_Q) + \lambda_b N\pi_E$$

F. SAMPLE CALCULATIONS OF PREDICTED RELIABILITY OF A MAGNETIC BUBBLE MEMORY DEVICE

A series of sample calculations have been made of several combinations of probable Magnetic Bubble Memory device parameters to illustrate the leverage of each sector on the overall predicted failure rate. Several cases are defined and the calculations made are based on these assumptions. A learning factor of 10 should be used for calculations of new product introductions for the current state of the art. If a justification of a more optimistic learning can be determined, then the calculated reliability projections can be decreased by reduction of the learning factor to 1.

Case No. 1: 92K bit Magnetic Bubble Memory, 40°C ambient, ground benign environment. 14 pin DIP enclosure, 1 major loop and 3 dissipative control elements (Generate, replicate and detector bridge) plus 144 current transfer gates for the 144 memory minor loops. Bubble size 3 μm dia. Screening B-2 level.

Case No. 2: Same as Case No. 1, except Class D screening.

Case No. 3: Same as Case No. 1, except Class D-1 screening.

Case No. 4: 1 Megabit Magnetic Bubble Memory device. 40°C ambient, ground benign environment, 20 pin DIP enclosure. 256 minor loops and 2 major loops. 12 dissipative control gates plus 512 transfer gates for the memory loops. Bubble size 2 μm dia. and B-2 screening level.

Case No. 1 Sample Calculations

$$\lambda_p \text{ (Control Elements)} = \pi_Q[C_1\pi_T\pi_V + (C_2 + C_3)\pi_E]\pi_L$$

$$= 6.5\ [(0.013)(0.49)(1) + (0.0008 + 0.0017)1]1$$

$$= 0.0577 = 0.06/10^6 \text{ hours}$$

Note: $\pi_Q = 6.5$, class B-2; $\pi_E = 1$; $\pi_L = 1$ (in production quantity);

$C_1 = 0.013$, Table 2.1.5-21, 144 transfer + 4 control elements;

$C_2 = 0.0008$; $\pi_T = 0.49$, Table 2.1.5-12 @ 40°C ambient (+ 1 1/2°C rise);
C is based on 10 functional pins;
$\pi_V = 1$, Table 2.1.5-14.

$$\lambda_p \text{ (Memory Elements)} = \pi_Q[N_1(C_1\pi_T\pi_M + C_2\pi_E) + N_2(C_1\pi_T\pi_M + C_2\pi_E)]\pi_L$$

$$= 6.5\ [1(0.026)(0.28)(0.1) + (0.0013\ )(1) + 144\ (....)]1$$

$$= 1.91/10^6 \text{ hours}$$

Note: $\pi_Q = 6.5$; $\pi_E = 1$; $\pi_L = 1$; $N_1 = 1$; $N_2 = 144$ @ 641 bits;

$C_1 = 0.026$, Table 2.1.5-23, 641 bit dynamic ram*;

$C_2 = 0.0013$, Table 2.1.5-23; $\pi_M = 1.0$;

$\pi_T = 0.28$ (Table 2.1.5-8, No Power Dissipation.) x 0.1 for bubble dia. = 3 um.

*641 bits/major loop and 641 bits/minor loop.

λ_p (Magnetic Sector) = λ_b ($\pi_E \pi_Q \pi_c$) x 2 for 2 coils.

= 0.0005 (1 x 1 x 1) x 2

= $0.001/10^6$ hours

Note: Section 2.7.2

λ_p (Interconnect Structure) = $\lambda_b N \pi_E$

= 6×10^{-6} x 28 x 1

= 168×10^{-6} = $0.00017/10^6$ hours

Note: Section 2.12; 28 connections not including the chip.

λ_p (Magnetic Bubble Memory) = 0.06 + 1.91 + 0.001 + 0.00017

= $1.97/10^6$ hours

Case No. 2 Sample Calculations

λ_p (Magnetic Bubble Memory) = 92K bit class D

= 0.16 + 5.14 + 0.001 + 0.00017)

= $5.3/10^6$ hours

Case No. 3 Sample Calculations

λ_p (Magnetic Bubble Memory) = 92K bit class D-1

$= 0.32 + 10.285 + .001 + .00024$

$= 10.61/10^6$ hours

Case No. 4 Sample Calculations (1,048,576 bit, M.B.M. class B-2)

λ_p (Control Elements) $= \pi_Q [C_1\pi_T\pi_V + C_2 + C_3)\pi_E]\pi_L$ *

$= 6.5 [((0.021)(0.49)(1)$
$+ (0.001 + 0.0026))(1)]1$

$= 0.09$

λ_p (Memory Elements) $= \pi_Q [N_1(C_1\pi_T\pi_M + C_2\pi_E)$
$+ N_2(C_1\pi_T\pi_M + C_2\pi_E)]\pi_L$

$= 6.5 [2(0.34 \times 0.28 \times 0.5 + 0.0017 \times 1)$
$+256 (0.08 \times 0.28 \times 0.5 + 0.0039 \times 1)] 1$

$= 25.21$

Note: 1024 bits/major loop and 4096 bits/minor loop.

λ_p (Magnetic Bubble Memory) $= 0.09 + 25.21 = 25.3/10^6$ hours

*NOTE: C_3 is based on 15 functional pins.

Correlation of Data:

A comparison can be made of the calculated reliability of semiconductor memory devices and the Magnetic Bubble Memory of a similar class of screening. In this comparison we see some justification for the projected levels of reliability, but in a more detailed examination of the elements of the Magnetic Bubble Memory calculations it is noted that an extreme leverage is assigned to the number of memory elements. As field data on actual operating systems is developed, this area should be examined closely to ascertain the appropriate leverage this factor should have in the comparative reliability projections for this class of device.

TABLE 5

Projected Reliability of a Range of Semiconductor Memory Devices with Class B-2 Screening

	NMOS DYNAMIC MEMORY			Magnetic Bubble Memory		
Complexity	1K	16K	64K		92K	1Meg
				Control Elements	0.06	0.09
				Memory Elements	1.91	25.2
Projected Reliability $F/10^6$ Hrs.	0.19	0.86	1.95	TOTAL	1.97	25.3

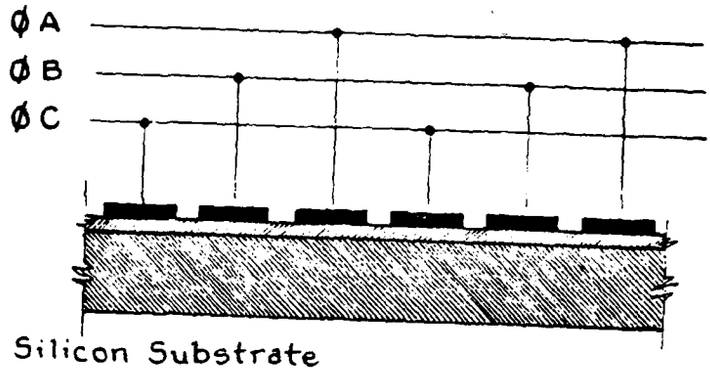
IV. CHARGE-COUPLED DEVICE MEMORY

A. DESCRIPTION

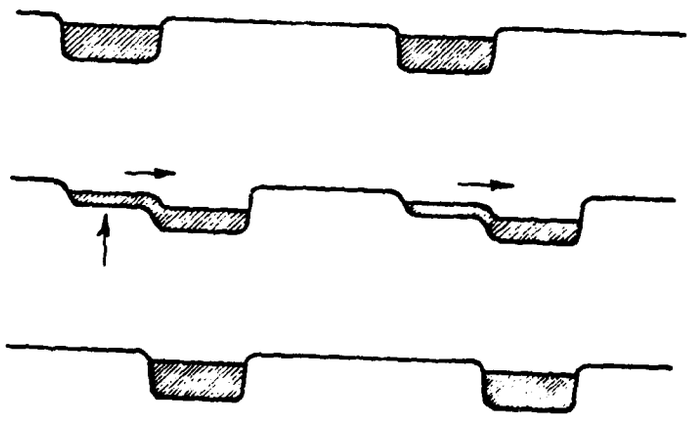
A charge-coupled device (CCD) is essentially an analog shift register. The analog variable is the amount of charge held in a metal-oxide-silicon (MOS) capacitor. The charge can be moved along from capacitor to capacitor by cycling the voltages applied to the conductors of the MOS structure. The basic structure of a CCD and the action of a three-phase clock for shifting the charge are shown in Figure 17.

When a positive voltage is applied to a capacitor electrode or gate, a depletion region is produced in the silicon below the gate, and a potential well results at the silicon-silicon dioxide interface. The stored charge then flows from the adjacent storage site into the newly formed potential well. Clearly a three- or four-phase clock drive can establish the direction of transfer and move the stored charge smoothly along the shift register. Two-phase clock drive systems can also be used, but the gate electrode structure must be asymmetrical in order to determine the direction in which the charge will move.

An important parameter of CCD's is the charge transfer efficiency, η, the fraction of the total charge moved to the next storage site in each cycle. The fractional loss, ε, which is equal to $1 - \eta$, is also used in discussing this effect. Starting with an initial charge, Q, after n transfer cycles, the remaining charge Q_r, is equal to $Q_o \eta^n$, ($Q_o \{1 - n\varepsilon\}$). It is clearly advantageous to have high transfer efficiency in order to preserve the signal through many transfer cycles.



STRUCTURE



MOVEMENT OF CHARGE

BASIC CHARGE TRANSFER SHIFT REGISTER

Figure 17

In spite of its simplicity, the CCD is a surprisingly versatile device. As a shift register, the CCD has been used in many analog signal processing schemes. Charge can be injected photoelectrically into linear or rectangular charge-coupled arrays. The resultant CCD's are line scan and photo imaging devices, respectively.

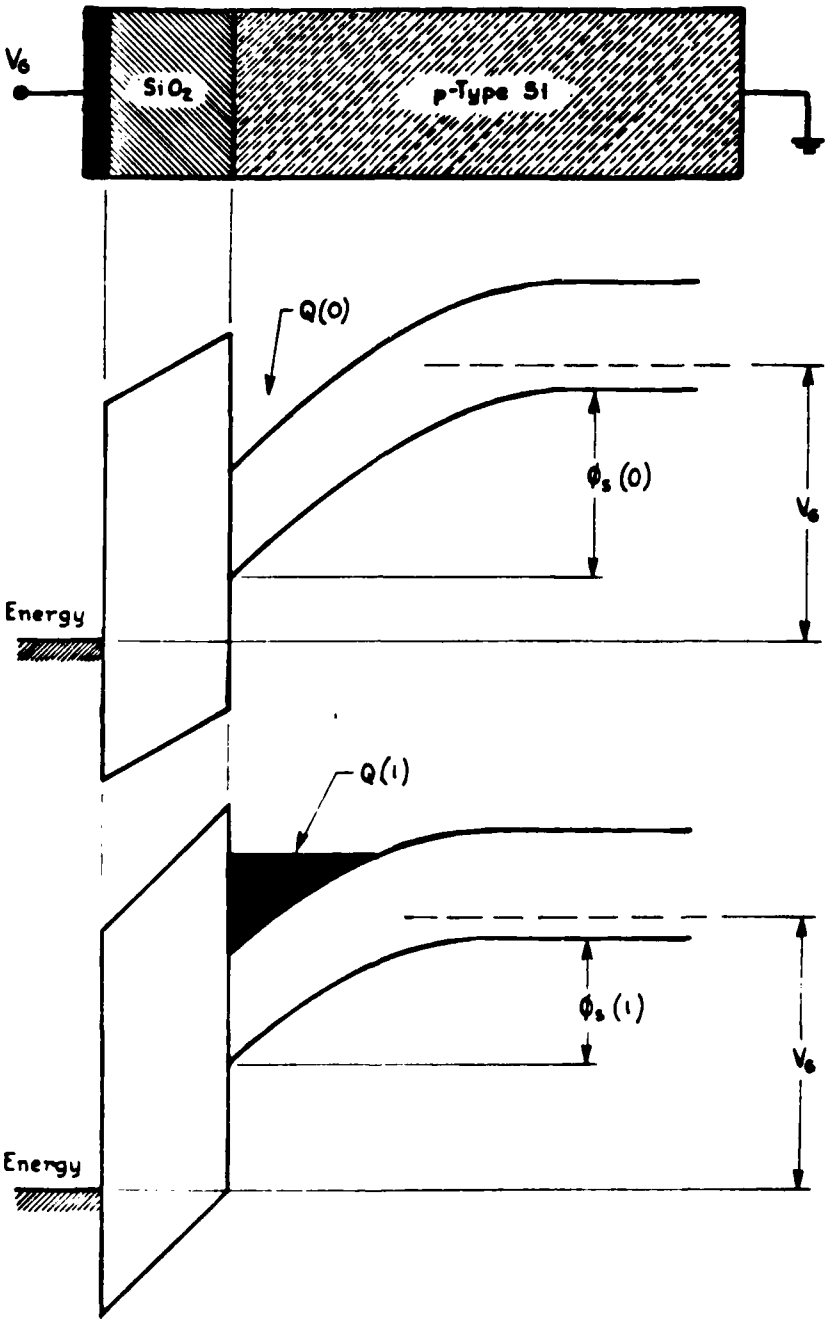
If the stored charge is quantized at two levels, the CCD becomes a binary digital storage device, or memory.

B. CHIP ARCHITECTURE

There are two types of charge-coupled devices based on the location of the stored charge. The surface channel CCD (SCCD) stores the charge on the surface of the silicon, under the insulating silicon dioxide layer (Figure 18). The buried channel CCD (BCCD) stores the charge in a thin layer of silicon, doped to a conductivity opposite that of the silicon substrate (Figure 19).

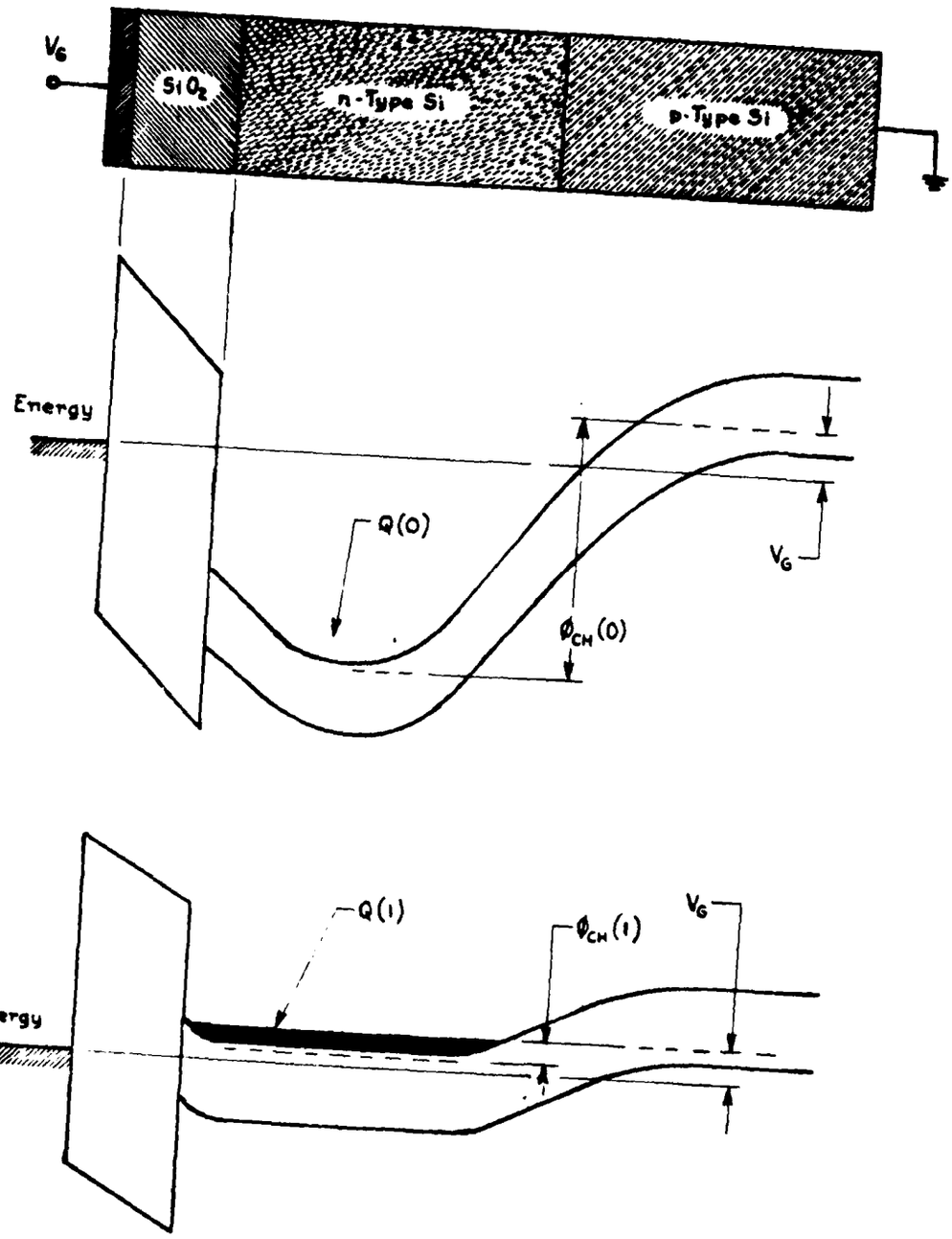
The BCCD has certain advantages over the SCCD. It needs no bias charge* to obtain a high transfer efficiency (η>.9999), does not have noise caused by surface states, and has a faster response for its physical size than the SCCD. However, the BCCD stores about one-half the charge of an SCCD, has higher leakage currents and is more difficult to fabricate.

*Memory CCD's often store appreciable amounts of charge to represent a "zero," sometimes as much as half the charge used to represent a "one." This is called "fat zero" operation as opposed to "real zero" operation, where no charge represents a "zero." Small amounts of bias charge, less than one-tenth the "one" state charge, are sometimes called "slim zero" operation.



CHARGE STORAGE IN SURFACE CHANNEL CCD

Figure 18



CHARGE STORAGE IN BARRIER CHANNEL CCD

Figure 19

Some of the more important CCD structures are shown in Figure 20. The single metal structure, a, used in early CCD's is degraded by the instability of the exposed channel oxide. The doped polysilicon structure, b, protects the channel oxide with high-resistivity undoped polysilicon between the gates. Other more complex structures, c, d, and e, use two or three levels of polysilicon and/or aluminum.

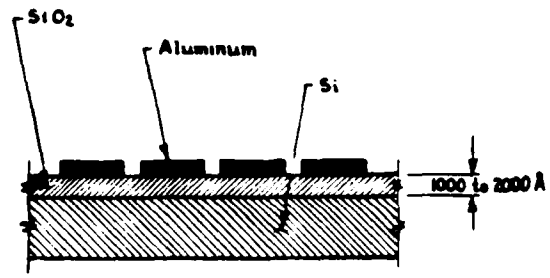
C. MEMORY ORGANIZATION

The simplest CCD memory organization is a single loop (Figure 21a). Because some small fraction of the stored charge is lost in each transfer, the signal must be periodically regenerated, in this case at the corners of the zigzags. Average access time is comparatively long in a single-loop memory. A more complicated single-loop organization, with parallel transfer through much of the loop (Figure 21b), has a shorter access time.

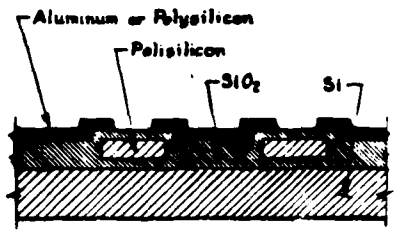
Multiple-loop memories may have linear organizations (Figure 21c), or if the number of loops is large enough, two-dimensional organizations (Figure 21d).

D. MANUFACTURERS

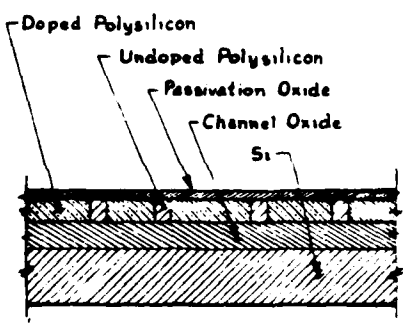
Early in the development of CCD technology (ca 1970), the potential of the device for high-density digital storage was recognized. Densities greater than one million bits per square inch were forecast. It was believed that these high densities would lower the cost per bit and make CCD memory systems highly competitive with alternative semiconductor digital storage techniques such as the MOS random access memory (MOS RAM). Many firms took an active part in CCD memory development (Table 6). Of these thirteen, only three firms (Intel, Fairchild, and Texas Instruments)



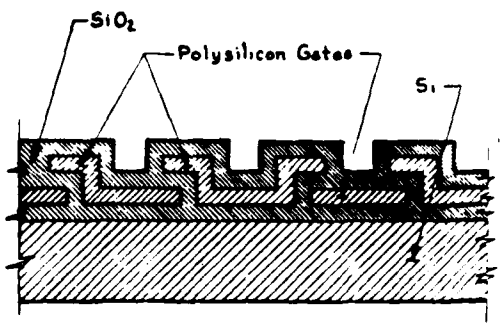
(a) SINGLE METAL CCD



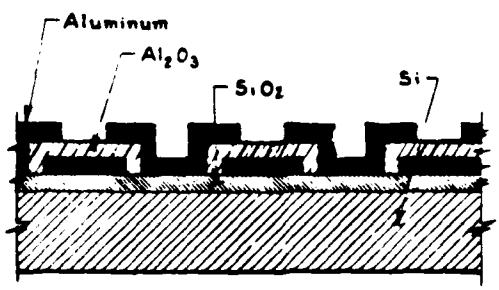
(c) POLYSILICON-ALUMINUM or TWO LEVELS OF POLYSILICON GATES



(b) DOPED POLYSILICON GATES



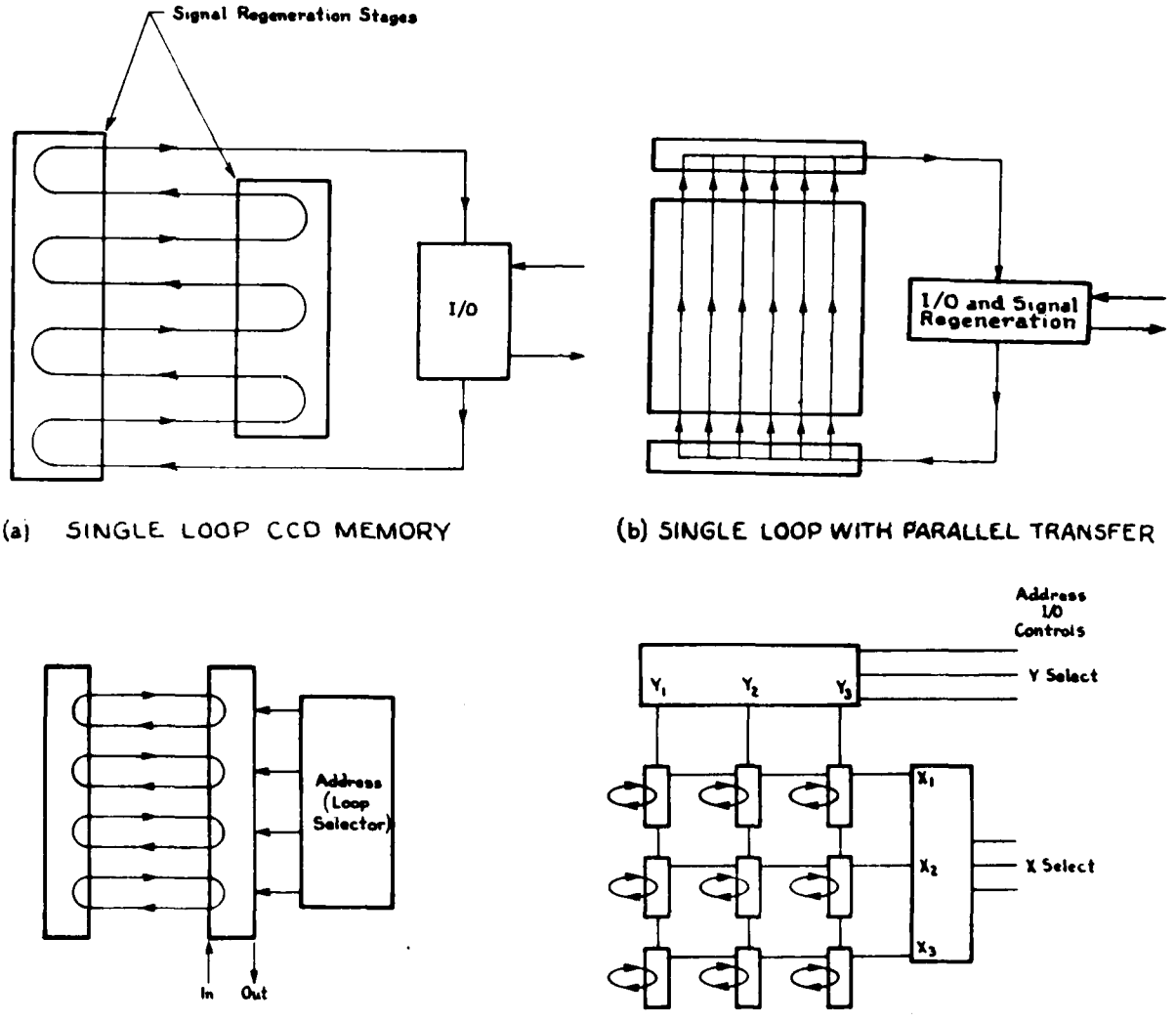
(d) THREE LEVELS OF POLYSILICON



(e) ANODIZED ALUMINUM CCD

CHARGE COUPLED DEVICE STRUCTURES

Figure 20



(a) SINGLE LOOP CCD MEMORY

(b) SINGLE LOOP WITH PARALLEL TRANSFER

(c) ONE DIMENSIONAL MULTILOOP ORGANIZATION

(d) TWO DIMENSIONAL MULTILOOP ORGANIZATION

CCD MEMORY ORGANIZATION

Figure 21

TABLE 6

FIRMS WHICH HAVE BEEN ACTIVE IN THE DEVELOPMENT OF CCD MEMORIES

Bell Northern
*Fairchild
General Electric Company, Ltd. (England)
General Electric
IBM
*Intel
Motorola
Plessey
RCA
Rockwell International
Siemens
Signetics
*Texas Instruments

*Firms which marketed devices.

eventually marketed a commercial product. As CCD memories were developed, progress was also made in the development of MOS RAM's, and a clearcut economic advantage for CCD's failed to materialize. As larger CCD memory arrays were developed, the MOS RAM's also increased in size. Intel no longer makes a CCD memory; Texas Instruments makes a CCD memory device, but is not actively seeking customers; and Fairchild remains the only serious producer of CCD memories.

E. FAILURE RATE MODEL DEVELOPMENT

The general form of a failure rate model for an electronic component is:

$$\lambda = \pi_a \pi_b \pi_c [C_1 f_1(T) + C_2 f_2(V) + C_3 f_3(E) + \ldots]$$

where:

λ = Failure rate.

$\pi_a, \pi_b \ldots$ = Multiplicative factors representing device quality, state of the manufacturer's learning curve, etc.

$C_n f_n(x)$ = Additive terms representing stress (voltage, temperature, environment) complexity (number of bits or gates), or some special effect or parameter.

To develop a reliability model for CCD memories, the NMOS dynamic RAM model was taken as a prototype, because MOS RAMS are close to CCD memories in structure, use and complexity. The NMOS dynamic RAM reliability model given in paragraph 2.1-4.1 of MIL-HDBK-217C (Proposed Notice 1) is:

$$\lambda_p = \pi_Q[C_1\pi_T\pi_V + (C_2 + C_3)\pi_E]\pi_L$$

where:

λ_p = Failure rate in failures/10^6 hours.

π_Q = A quality factor.

π_T = A temperature stress factor.

π_V = A voltage stress factor.

π_E = An environmental stress factor.

C_1 and C_2 = Device complexity (bit count) failure rates.

C_3 = Package complexity failure rate.

π_L = A learning curve factor.

Two questions must be answered in order to fit the NMOS RAM prototype model to CCD devices:

(1) Should the specific form of the model be changed by adding or deleting some terms or coefficients?

(2) What numerical values should be used for the parameters and coefficients in the model?

In seeking an answer to the first question, only one effect, the soft error rate, was identified as a potential candidate for inclusion in the CCD reliability model. Further analysis showed that the soft error rate does not belong in a reliability model that, by definition accounts only for catastrophic or drift-related errors. The specific form of the prototype was retained unchanged.

Soft errors are random, nonrecurring errors resulting from the loss of bits, or the upset of stored data without any accompanying physical damage. Bursts of noise exceeding the noise margins of a device would be a source of soft errors. A major cause of soft errors in CCD memories and dynamic RAM's is ionizing radiation, alpha particles, passing through the memory array area. The source of alpha particles is the decay of radioactive contaminants in packaging materials of the memory device. Uranium and thorium are present at parts-per-million levels in the sealing glasses, alumina ceramic packages, zirconia and quartz fillers, and even in plated gold. These are all sources of alpha particles with energies of about eight to nine million electron volts (Mev). At this energy, the alpha particles will penetrate silicon to a depth of about 50 microns (0.002 inch) and will generate one electron-hole pair for each 3.6 electron volts of energy. Up to 2.5 million electron hole pairs are produced for each alpha particle, and this is enough charge to fill a potential well and alter a stored bit.

The soft error rate is a parameter of a memory device. Should the rate rise above a specified level, the device is no longer useful and has failed. For this reason the soft error phenomenon was considered for inclusion in the CCD memory reliability model. But the alpha emission rate and, hence the soft error rate, are independent of temperature, pressure, voltage, and time.* Therefore, the soft error rate is a quality control problem and not a reliability problem, and does not belong in the reliability model. Note too, that alpha particle-induced soft errors are not peculiar to CCD's but also occur in dynamic RAM's.

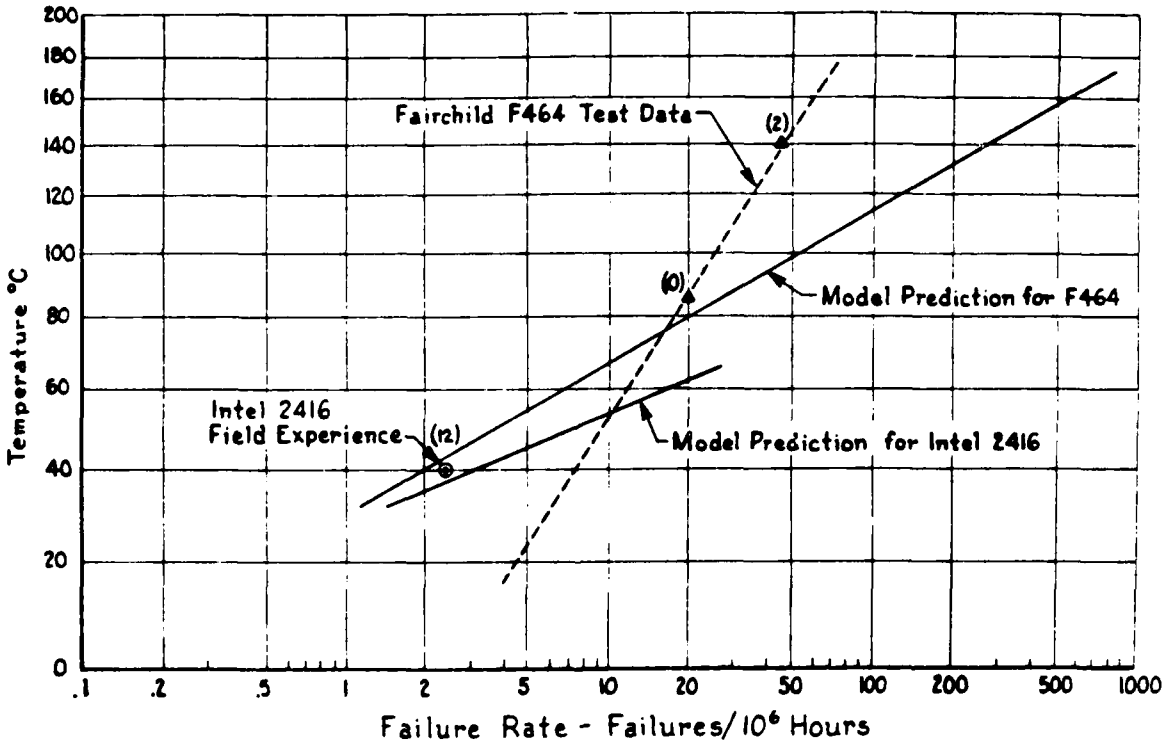
*Actually the alpha emission rate will decrease slowly as the radioactive contaminants are "used up."

Two sources of inputs can be used to answer the second question. The structure and operation of the NMOS RAM and the CCD memory can be compared to see if there is some physical reason for changing the value of some parameter or coefficient in the model. This comparison has been made and no basis for change has been found. The integrated circuit technologies for both devices are quite similar, and there is no difference in structural complexity sufficient to justify change.

The other input which might determine values for the parameters and coefficients in the reliability model is actual reliability data, either from field experience or from reliability testing. Very little data of this type is available because, to date, there has been no large-scale production and use of CCD memories. Therefore, reliability experience cannot be used to modify the numerical values of the model. Furthermore, the reliability data which could be found fit the MIL-HDBK-217C NMOS dynamic RAM reliability model to an acceptable degree of accuracy.

F. FAILURE RATE MODEL VALIDATION

We found reliability data for two CCD memories: the Intel 2416 and the Fairchild F464. The Intel field experience, the Fairchild test results, and the predictions from the NMOS dynamic RAM model are plotted in Figure 22. The number of failures for each datum is shown in parentheses. The agreement of the model with the Intel field experience is excellent. The agreement of the model with the Fairchild test data is much poorer, but the accuracy of the test data is also poor because of the small numbers of failures and total unit hours.



COMPARISON OF N-MOS DYNAMIC RAM MODEL WITH CCD RELIABILITY DATA

Figure 22

1. Intel 2416 Data

The Intel 2416 data was obtained from the field experience of Azurdata, Inc., which had 3,000 units in use for an estimated 5.2×10^6 unit hours. On the basis of 12 reported failures, the best estimate failure rate is 2.4 failures per 10^6 hours.

The Intel 2416 is a 16K serial memory, 64 loops of 256 bits each. It is contained in an 18-pin plastic dual inline package. The maximum supply voltage is 12 volts. The parameters used in the reliability model are:

$\pi_Q = 35$

$C_1 = .186$

$\pi_T = 0.44 (T_j = 40°C)$*

$\pi_V = 1.0$

$C_2 = 0.0088$

$C_3 = 0.007$

$\pi_E = 1$

$\pi_L = 1$

λ_p(computed) = 3.42 failures per 10^6 hours

2. Fairchild F464 Data

The Fairchild F464 data comes from a Fairchild LSI reliability report dated October 1978. Two sample lots of 18 and 16 units were operated for 2,400 hours and 1,000 hours, respectively, at an ambient temperature of 125°C. Two reported failures, one in each

*The junction temperatures are assumed to be 15° above ambient for these computations.

lot, were attributed to ionic contamination. Two more sample lots of 18 and 17 units were operated for 1,000 hours each at an ambient temperature of 70°C. There were no failures.

The best-estimate failure rate for two failures in 59,200 unit hours is 45 failures per 10^6 hours, at 125°C ambient. The best estimate failure rate for no failures in 35,000 unit hours is 20 failures per 10^6.*

The Fairchild F464 is a 64K serial memory (65,536 bits in one loop), contained in a dual inline hermetic package with 22 pins.

The parameters used in the reliability model are:

$\pi_Q = 17.5$
$C_1 = 0.434$
$\pi_T = 38 \ (T_j = 140°C)$
$= 3.6 \ (T_j = 85°C)$
$C_2 = 0.02$
$C_3 = 0.008$
$\pi_E = 1$
$\pi_L = 1$

λ_p(computed) = 290 failures per 10^6 hours at T_m = 140°C
λp(computed) = 28 failures per 10^6 hours at T_m = 85°C

---

*Lower limit of the confidence interval for MTBF for confidence level $1-\alpha$ and τ failures in total unit hours T is:

$$MTBF = \frac{2T}{\chi^2 \ (\alpha, \ 2r + 2)}$$

Reference; Reliability Engineering, Wm. H. vonAlven, Prentice-Hall, Inc. 1965.

APPENDIX A

BIBLIOGRAPHY OF MAGNETIC BUBBLE MEMORY

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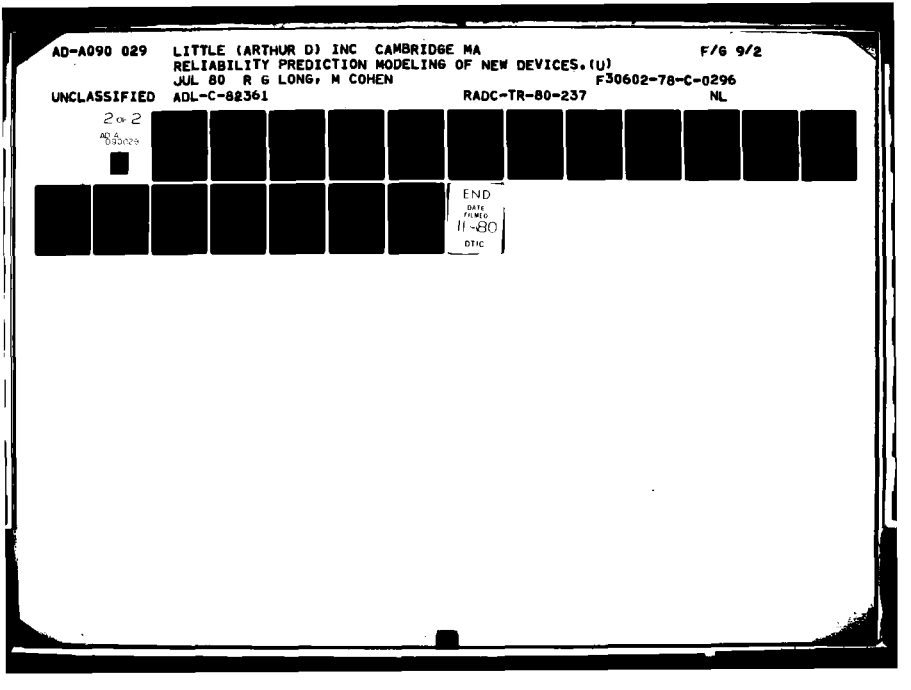

APPENDIX B

BIBLIOGRAPHY OF CHARGE-COUPLED DEVICE TECHNOLOGY

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