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George C. Marshall Space Flight Center
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QD01

MULTIPROGRAM/PROJECT COMMON-USE DOCUMENT

WORKMANSHIP STANDARD FOR PRINTED WIRING BOARDS

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DOCUMENT HISTORY LOG

Status (Baseline/ Revision/ Canceled)	Document Revision	Effective Date	Description
Baseline		02/05/99	Initial release
Revision	A	06/21/06	Updated document per NASA Headquarters Rules Review. Reformatted document to new template, and renumbering all paragraphs accordingly. Updated the "APPLICABLE DOCUMENT" section to remove canceled, or add replacement documents. Replaced MIL-P-81728 with SAE-AMS-P-81728, which supersedes MIL-P-81728. Replaced QQ-N-290 with SAE-AMS-QQ-N-290, which supersedes QQ-N-290. Replaced "ASTM B488-95" with "ASTM B488-01". Added "J-STD-003" titled Solderability Tests for Printed Boards to the APPLICABLE DOCUMENTS section. Revised the second sentence of paragraph 4.2 as follows: ".....data is available for review and approved by the procuring organization." In the second sentence of paragraph 4.5.1, replaced "Tables 5 and 6 of IPC-4101" with "Tables 3-1 and 3-2 of IPC-4101". In paragraph 4.5.5, replaced "99.5" with "99.75" and "ASTM E53-86a" with "ASTM E53-02". In paragraph 4.5.6, replaced "MIL-P-81728" with "SAE-AMS-P-81728". In paragraph 4.5.8, replaced "ASTM B488-95" with "ASTM B488-01". In paragraph 4.5.9, replaced "QQ-N-290" with "SAE-AMS-QQ-N-290". Updated paragraph 5.14.6 titled "Layer-to-Layer Registration", and revised Figure 6. Updated paragraph 5.14.8 titled "Hole Solderability" with the following: "After stress testing as specified in 5.14.7, the printed wiring board test specimen shall meet the requirements per J-STD-003, Test Method C (Solder Float Test) for Class 3." In the second sentence of paragraph 5.15.1, replaced "it's" with "its". Revised Tables III and IV to correlate with the updated paragraph numbering. Added the wording "(zero defects)" in the title of Table V.

FOREWORD

This standard sets forth requirements for rigid printed wiring boards (PWB's). The parts in conformance with this standard are intended for use in aircraft, spacecraft, launch vehicles, and mission-essential support equipment. These requirements shall be invoked by drawings and specifications for flight hardware and critical support equipment.

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1.0 SCOPE

This publication sets forth requirements for rigid printed wiring boards (PWB's). The parts in conformance with this standard are intended for use in aircraft, spacecraft, launch vehicles, and mission-essential support equipment.

Special requirements may exist which are not covered by or are not in conformance with the requirements of this publication. *Design documentation shall contain the detail for such requirements, and they shall take precedence over conflicting portions of this publication when the Marshall Space Flight Center (MSFC) has approved them in writing.*

This standard is intended for use by MSFC and its contractors. The term supplier refers to the fabricator of PWB's. The terms procuring organization and customer refer to MSFC when MSFC is the direct purchaser or to the MSFC contractor when they are the direct purchasers.

2.0 APPLICABLE DOCUMENTS

Unless otherwise specified, the issue in effect on the date of invitation for bids or request for proposal applies.

2.1 Military Standards

Document Number	Title
MIL-PRF-31032	Printed Circuit Wiring Board, General Specification for

2.2 Society of Automotive Engineers

Document Number	Title
SAE-AMS-QQ-N-290	Nickel Plating (Electrodeposited)
SAE-AMS-P-81728	Plating, Tin-Lead (Electrodeposited)

2.3 Other Standards

Document Number	Title
A-A-56032	Commercial Item Description, Ink, Marking, Epoxy Base
ANSI/ASQC Q9001-1994	American National Standard, Quality Systems-Model for Quality Assurance in Design, Development, Production, Installation, and Servicing
ANSI/ASQC 9002-1994	Quality Systems-Model for Quality Assurance in Production, Installation, and Servicing

ASTM B488-01	Standard Specification for Electrodeposited Coatings of Gold for Engineering Uses
ASTM E53-02	Determination of Copper in Unalloyed Copper by Gravimetry
IPC-T-50	Terms and Definitions for Interconnecting and Packaging Electronic Circuits
IPC-TM-650	Test Methods Manual
IPC-SM-840	Qualification and Performance of Permanent Polymer Coating (Solder Mask) for Printed Circuit Boards
IPC-2221	Generic Standard on Printed Board Design
IPC-4101	Materials Standard for Printed Boards
IPC-6012	Qualification and Performance Specification for Rigid Printed Boards
J-STD-003	Solderability Tests for Printed Boards
J-STD-006	Requirements for Electronic Grade Solder Alloys and Fluxed and Non Fluxed Solid Solders for Electronic Soldering Applications

3.0 DEFINITIONS

Acronyms used in this standard. The acronyms used in this standard are defined as follows:

AMS	Aerospace Material Specification
ANSI	American National Standards Institute
ASQC	American Society for Quality Committee
ASTM	America Society for Testing and Materials
C	Acceptance Number
CAD/CAM	Computer-Aided Design/Computer-Aided Manufacturing
ESD	Electrostatic Discharge
FREQ	Frequency
MSFC	Marshall Space Flight Center
N/A	Not Applicable
PTH	Plate-Thru-Hole

PWB Printed Wiring Board

QMS Quality Management System

SAE Society of Automotive Engineers

SPEC Specimen

TM Test Method

Printed wiring board definitions that form a part of this standard are contained in IPC-T-50. Additional definitions are given below:

a. **Thermal-Shock Test.** The thermal-shock test is used to determine the ability of a printed wiring board to withstand repeated rapid temperature excursions without losing electrical continuity and current-carrying capacity, and without degradation of the materials.

b. **Thermal-Stress Test.** The thermal-stress test is a test used to determine the ability of a printed wiring board to withstand the soldering operation without fracturing the plated-through holes or other conductors and without degradation of the materials. It consists of floating the specimens on molten solder followed by microsectioning the plated-through holes and visually examining the board and the microsectioned holes.

4.0 GENERAL REQUIREMENTS

4.1 Classification. Printed wiring boards shall be of the types specified as follows:

a. Type 1 -single-sided board.

b. Type 2 -double-sided board.

c. Type 3 -multilayer board.

4.2 Qualification. Qualification shall consist of the following:

a. on-site audit of supplier's quality system and manufacturing processes.

b. review of qualification test data from an independent laboratory.

Qualification testing shall be in accordance with the test/inspections specified in Table III. Current and active qualification to other printed wiring board standards MIL-PRF-31032 or IPC-

6012 shall be accepted in lieu of additional testing provided the data is available for review and approved by the procuring organization. Qualification status shall be maintained by continued acceptance of microsectioned coupons provided with the purchased product and periodic on-site audits.

4.3 Deviation and Waiver Requests. The supplier shall be responsible for assuring that any departures from this publication are evaluated, coordinated with, and submitted to the procuring organization for approval prior to use or implementation. Rework shall be permissible unless excluded by other provisions of the contract. All rework shall meet the requirements of this publication. Rework is not repair. Repair shall be made only in compliance with applicable contractual requirements.

4.4 Quality Management System (QMS). Unless otherwise specified by procurement documentation, the supplier shall have a QMS in compliance with ANSI/ASQC Q9001 or Q9002 as applicable. The PWB supplier shall require laminate/prepreg suppliers to have a QMS that complies with ANSI/ASQC Q9002.

4.5 Materials

Materials used in low pressure or vacuum compartments shall have low emittance of condensables and noxious or toxic gases. Materials used shall be subject to MSFC approval.

4.5.1 Metal-Clad Laminates. Metal-clad laminates shall be in accordance with IPC-4101. The PWB supplier shall require that the laminate/prepreg supplier's material be qualified and that conformance testing be performed in accordance with Tables 3-1 and 3-2 of IPC-4101. The type, copper thickness, surface condition, and material thickness shall be specified on the approved engineering drawing. Base material for Type 3 individual layers shall be .002 inch (.05 mm) minimum thickness per sheet plus sufficient prepreg (see 4.5.2) to meet the minimum dielectric requirements of 5.14.5.

4.5.2 Bonding Layer (Prepreg). The bonding layers for Type 3 boards shall be preimpregnated (B-Stage) glass cloth conforming to IPC-4101 and of the same type as the metal-clad plastic sheet.

4.5.3 Plating or Solder Coating. Unless otherwise specified in the approved engineering drawing, printed wiring boards shall be solder coated or tin-lead plated and fused. When other platings are used on the same printed wiring board in conjunction with solder coating or fused tin-lead plating, there shall be no tin-lead between the other plating and the copper. When polymer mask coatings are applied over bare or black-oxide copper, exposed circuit areas shall be solder-coated or tin-lead plated and fused. Unless otherwise specified, plating thickness shall meet the requirements of 5.13.1. This does not apply to vertical conductor edges when fused tin-lead plating is used.

4.5.4 Electroless Copper Plating. An electroless copper deposition system shall be used as a preliminary process for providing the conductive layer over nonconductive material for subsequent electrodeposition of plated-through holes.

4.5.5 Electrolytic Copper Plating. All electrolytic copper plating shall have a minimum purity of 99.75 percent as determined by American Society of Testing and Materials (ASTM) E53-02. The minimum thickness shall meet the requirements of 5.14.3. The type of copper deposit may be specified by the procuring organization.

4.5.6 Tin-Lead Plating. Tin-lead plating shall be in accordance with SAE-AMS-P-81728. Fusing shall be required on all tin-lead plated surfaces. The fused tin-lead shall meet the thickness requirements of 5.14.3, shall be homogeneous, and shall completely cover the conductors. This is not intended to apply to vertical conductor edges.

4.5.7 Solder Coating. Solder coating shall be in accordance with composition Sn60, Sn62, or Sn63 of J-STD-006. The solder coating thickness shall meet the thickness requirements of 5.14.3, shall be homogeneous, and shall completely cover the conductors.

4.5.8 Gold Plating. All electrolytic gold plating shall be in accordance with ASTM B488-01. The thickness shall be as specified in 5.14.3. A low-stress nickel plating (see 4.5.9) shall be used between gold overplating and copper. The class and type shall be as specified on the approved engineering drawing.

4.5.9 Nickel Plating. All electrolytic nickel plating shall be low stress and conform to SAE-AMS-QQ-N-290, Class 2 except the minimum thickness shall be as specified in 5.14.3.

4.5.10 Solder Mask. Polymer mask coating materials shall meet the requirements Class 3 and shall be specified on the approved engineering drawing.

4.5.11 Marking Ink. Marking ink shall be an epoxy-base ink conforming to A-A-56032.

4.5.12 Solvents. Solvents shall be nonconductive and noncorrosive, and shall not degrade the quality of the material. Solvents shall be properly labeled and maintained in a clean and uncontaminated condition. Those showing evidence of contamination or decomposition shall not be used.

4.6 Quality Conformance Test Circuitry

4.6.1 Type 1 and Type 2. Unless otherwise specified in the engineering documentation, test coupons are not required to be submitted to the procuring organization for Type 1 and 2.

4.6.2 Type 3. Quality conformance test coupons in accordance with IPC-2221 or as provided by engineering documentation shall be included at least once on the panel. The coupon

shall incorporate a pad at each layer and shall represent the worse design case. When solder mask is specified for the production board then it shall be incorporated into the test coupon.

5.0 DETAILED REQUIREMENTS

5.1 Dimensions.

5.1.1 Hole Pattern. The accuracy of the hole pattern shall be as specified on the approved engineering drawing.

5.1.2 Overall. Finished printed wiring boards shall meet the dimensional requirements specified herein and on the approved engineering drawing.

5.2 Conductor Width and Spacing. Unless otherwise specified on the approved engineering drawing, isolated reductions of 20 percent or less of any conductor width or spacing caused by any combinations of edge roughness, nicks, pinholes or scratches shall be acceptable. The conductor width or spacing remaining at the point of reduction shall be 80 percent of the remaining conductor width or spacing specified on the approved engineering drawing. Under no circumstances shall the edges of the conductors have a roughness that exceeds .005 inch (.13 mm) or 20 percent of the line width, whichever is less, from peak to valley as measured over any .5 inch (13 mm) length (see Figure 1).

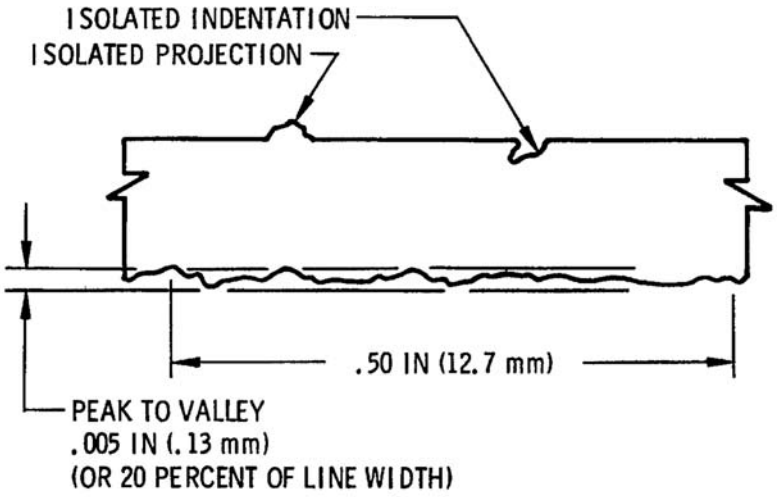

Figure 1. Edge Roughness

5.3 Measling and Crazing. Measling, crazing, or white spots below the board surface shall be acceptable if the total area affected does not exceed 1 percent of the board area and there is no more than 25 percent reduction in space between electrically uncommon conductors. The edge of the printed wiring board may show evidence of crazing, haloing, or chipping, provided it

does not extend into the board closer to the nearest conductor than the established minimum electrical spacing, or .060 inch (1.52 mm), whichever is less.

5.4 Delamination. There shall be no delamination of the individual layers or plies of the board.

5.5 Undercutting. Undercutting at each edge of the conductors shall not exceed the total thickness of clad and plated copper.

5.6 Conductor Outgrowth. There shall be no outgrowth on conductor edges finished with fused tin-lead plating or solder coating. The maximum permissible outgrowth on conductors plated with other than the above metals shall be .001 inch (.025 mm).

5.7 Bow and Twist. The maximum allowable bow and twist shall be 1.5 percent for that use through-hole devices exclusively and 0.75 percent for PWB's that use surface mounted components unless otherwise specified on the approved engineering drawing. Bow and twist shall be determined in accordance with IPC-TM-650, Method 2.4.22.

5.8 Plating Adhesion. When tested as specified in IPC-TM-650, Method 2.4.1, there shall be no evidence of the plating or coating being removed as shown by particles adhering to the tape or by separation of the plating or coating from the circuit pattern. If the metal outgrowth breaks off (slivers) and/or adheres to the tape, this is evidence of outgrowth but not plating adhesion failure.

5.9 Dielectric Withstanding Voltage (DWV). Test applicable coupons in accordance with IPC-TM-650, Method 2.5.7, at a voltage of 500 Vdc (+15, -0). Adjust the voltage to 250 Vdc (+15, -0) when the spacing is less than 0.003 inch. The dielectric withstanding voltage shall be applied between all common portions of each test pattern and all adjacent common portions of each test pattern. The voltage shall be applied between conductor patterns of each layer and the electrically isolated pattern of each adjacent layer. There shall be no dielectric breakdown of circuits or flashover.

5.10 Cleanliness. When tested in accordance with IPC-TM-650, Method 2.3.25, uncoated printed wiring boards shall be free of ionic and other contaminants such as dirt, oil, corrosion, corrosive products, salts, smut, grease, fingerprints, mold release agents, foreign matter or flux residue. The contamination level shall not exceed an equivalent of 1.17 $\mu g/cm^2$ of sodium chloride.

5.11 Marking. Unless otherwise specified, each individual board and each set of quality conformance test coupons shall be marked in accordance with the approved engineering drawing, with the date and manufacturer's code (Federal Supply Code for Manufacturers). For traceability, the quality conformance test coupon shall be identified with the corresponding production boards produced on the panel of that coupon. The marking shall be produced by the

same process used in producing the conductor pattern, by the use of marking ink or by the use of an electric pencil on a copper pad provided for marking purposes. Etched marking shall not reduce the spacing requirements specified on the master drawing. All marking shall be compatible with materials and parts, legible after all tests and in no case shall affect board performance.

5.12 Solder Mask. Cured solder mask coatings shall meet the requirements of IPC-SM-840, class H. Prior to coating, boards shall meet the cleanliness requirements of 5.10. For the purposes of qualification, solder mask when used in the design shall be considered part of the qualification requirements of the PWB supplier. Quality conformance inspection of solder mask shall be through testing of attributes in accordance with IPC-SM-840, Table 9.

5.13 Specific Requirements (Types 1 and 2 without plated-through holes). In addition to the requirements detailed above, Type 1 and Type 2 boards without plated-through holes shall meet the following:

5.13.1 Plating or Coating Thickness. Plating or coating thickness shall conform to the requirements specified in Table I unless otherwise specified on the approved engineering drawing.

5.13.2. Annular Ring. The minimum ring shall be .015 inch (.38 mm) when measured from the edge of the drilled hole to the outer edge of the annular ring. See Figure 2.

Table I. Plating or Coating Thickness

Plating or Coating Material	Minimum Surface Thickness Inches (mm)
Gold	.00005 inch min (.0013 mm)
Nickel	.0002 inch min (.005 mm)
Tin-lead, fused[1]	.0003 inch min (.008 mm)
Solder coat[1]	.0003 inch min. (008 mm)

Note 1. Thickness shall be measured at the crest of the conductor.

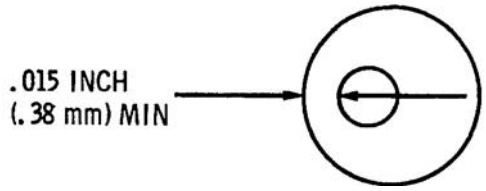

Figure 2. Minimum Annular Ring (Unsupported Hole)

5.14 Specific Requirements (Type 2 with plated-through hole and Type 3). Plated-through holes of Type 2 and 3 shall be formed by a combination of electroless copper plating and electrolytic copper plating, and shall be overplated with either tin-lead plating or solder coating. Type 2 boards with plated-through holes and Type 3 boards shall meet the following:

5.14.1 Plated-through hole. Plated-through holes shall be microsectioned in the vertical plane at the center of the hole and examined for quality of plating at a magnification of 100X±5 percent. Plating thickness shall be measured at a magnification of 200X minimum. Each side of the hole shall be viewed independently. A minimum of one microsection containing at least three holes shall be made for each sample tested. Examination shall be made both before and after the specimen is etched. They shall be free of the following defect (see Figures 3 and 4):

a. Layer-to-layer misregistration exceeding limits specified in 5.14.6.

b. Cracks in the plated copper or internal foils.

c. Resin smear in Type 3 printed wiring boards.

d. Separation at conductor interfaces (Type 3).

e. Separation between plated layers (Types 2 and 3).

f. Nailheading of internal interfaces exceeding 50 percent of the thickness of the copper foil (Type 3).

g. Plating thickness less than the minimum requirements of 5.14.3.

h. Plating voids in the plated-through hole.

i. Etchback (when specified) in excess of .003 inch (.08 mm) or less than .0002 inch (.005 mm).

j. Delamination.

k. Resin recession with a maximum depth in excess of .003 inch (.08 mm) or along the side of the plated-through hole for a distance in excess of 40 percent of the cumulative base material thickness (sum of the layer thicknesses being evaluated) on the side of the plated-through hole being evaluated.

l. Laminate voids away from the plated barrel more than .003 inches (.08 mm) in diameter.

m. Nodules that reduce the hole diameter below minimum drawing requirements.

n. Glass fiber protrusion reducing the plating thickness below the minimum specified on the approved engineering drawing.

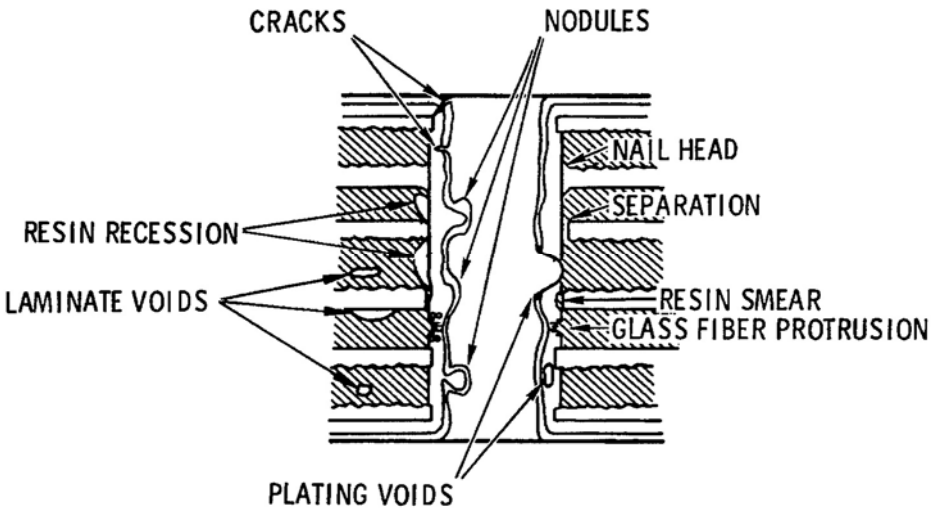

Figure 3. Defects in Multilayer Printed Wiring Board

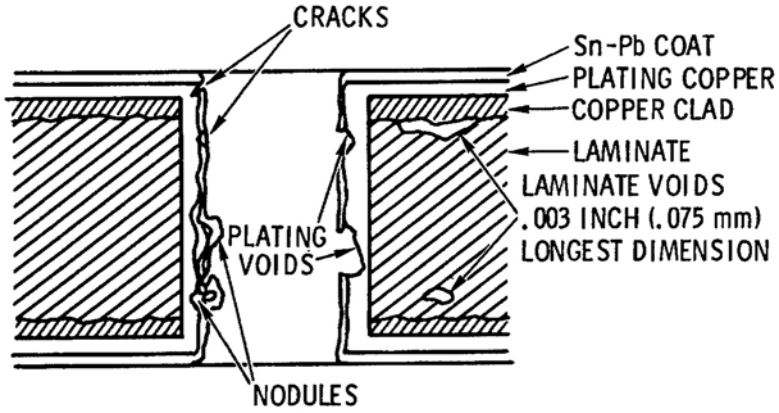

Figure 4. Cracks, Nodules, and Voids in Double-Sided PWB's

5.14.2 Hole Cleaning and Etchback (Type 3 only). Holes shall be processed to remove all traces of resin smear and contaminants from the surfaces of the exposed internal copper rings. When etchback is specified on the approved engineering drawing, it shall be .0002 inch (.005 mm) minimum and .003 inch (.08 mm) maximum when measured at the internal copper contact area protrusion with a preferred depth of .0005 inch (.013 mm) (see Figure 5). Wicking may extend an additional .003 inch (.08 mm). The etchback shall be effective on at least the top or bottom surface of each internal conductor (see Figure 5).

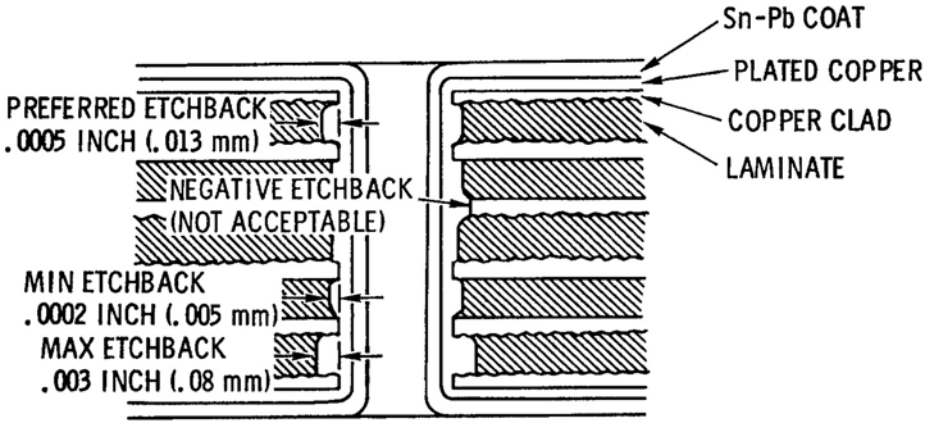

Figure 5. Multilayer Printed Wiring Board

5.14.3 Plating or Coating Thickness. Plating or coating thickness shall conform to the requirements specified in Table II unless otherwise specified on the approved engineering drawing.

5.14.4 Annular Ring. The minimum annular ring for plated-through holes shall be as follows:

External - .005inch (.13 mm)

Internal (Type 3 only) - .002 inch (.05 mm).

The measurement of the annular ring on external layers shall be from the inside surface (within the hole) of the plated hole to the outer edge of the annular ring on the surface of the board. On internal layers, the annular ring shall be measured from the edge of the drilled hole to the outer edge of the annular ring.

5.14.5 Dielectric Layer Thickness (Type 3). Finished Type 3 boards shall have a minimum of .0035 inch (.09 mm) of dielectric material between the consecutive conductor layers, when cured. The dielectric material shall be comprised of laminate, and laminate, or

multiple layers of prepreg. There shall be no less than two sheets of prepreg used between each pair of adjacent conductor layers.

5.14.6 Layer-to-Layer Registration. Unless otherwise specified on the approved engineering drawing, the layer-to-layer registration shall not reduce the minimum internal annular ring below the limit per paragraph 5.14.4. The internal registration shall be evaluated by vertical microsectioning and inspected at 50 to 100 magnifications. After laminating and drilling, multilayer boards may be X-ray examined to assure that the drilled holes pass through the pads on each layer leaving sufficient copper around the holes to meet the requirement of 5.14.4. In event of conflict between X-ray and microsection, the microsection shall govern.

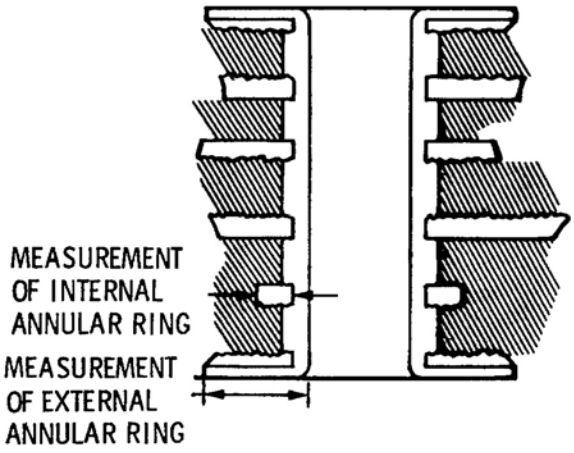

Figure 6. Annular Ring Measurements

Table II. Plating or Coating Thickness (Plated-Through Holes)

Plating or Coating Material	Minimum Surface and Through-Hole Plating of Coating Thickness, Inches (mm)
Electroless copper	Sufficient for subsequent electrodeposition
Electrolytic copper[1]	.001 in. min (0.25 mm)
Gold	.00005 in. min (.0013 mm)
Nickel	.0002 in. min (.005 mm)
Tin-lead, fused[2]	.0003 in. min (.0076 mm)
Solder coat[2]	.0003 in. min (.0076 mm)

Notes:

1. Thinnest point shall be .001 inch (0.25 mm) or greater.
2. Thickness shall be measured at the crest of the conductor or at the crest in the hole, as applicable. A plating of .0001 inch min (.002 mm) in the hole is acceptable.

5.14.7 Thermal Stress. When tested as specified in IPC-TM-650, Method 2.6.8, the specimen shall exhibit no cracking, separation of plating and conductors, blistering or delamination. Measling, crazing or white spots below the board surface are acceptable if the total area affected does not exceed 2 percent of the board area and there is no more than 50 percent reduction in space between electrically uncommon conductors. The specimen shall be microsectioned. Resin recession at the interface of the hole wall and plated through hole barrel shall be permitted provided the maximum depth as measured from the barrel wall does not exceed .003 inch (.08 mm) and the resin recession on any side of the plated-through hole does not exceed 40 percent of the cumulative base material thickness (sum of the layer thicknesses being evaluated) on the side of the plated-through hole being evaluated. (See Figure 3.)

5.14.8 Hole Solderability. After thermal stress testing as specified in 5.14.7, the printed wiring board test specimen shall meet the requirements per J-STD-003, Test Method C (Solder Float test) for Class 3.

5.14.9 Rework Solderability. Three holes per coupon shall be tested in accordance with IPC-TM-650, Method 2.4.36. The cross section of the plated-through holes shall meet the requirement of 5.14.7 and 5.14.8.

5.14.10 Circuitry (Type 3 Only).

a. *Circuit Shorts (Insulation Resistance).* A test voltage shall be applied between all common portions of each conductor pattern and all adjacent common portions of each conductor pattern. The voltage shall be applied between conductor patterns of each layer and the electrically isolated pattern of each adjacent layer. The minimum applied breakdown test voltage shall be 60 volts dc unless otherwise specified on the approved engineering drawing. The insulation resistance between mutually insulated conductors shall be greater than 100 megohms.

b. *Circuit Continuity.* A current shall be passed through each conductor or group of interconnected conductors by applying electrodes on the terminals at each end of the conductor or group of conductors. The current passed through the conductors shall not exceed that specified on the master drawing for the smallest conductor in the circuit. There shall be no open circuits in the specimen.

5.14.11 Thermal Shock. When tested in accordance with IPC-TM-650 Method 2.6.7.2, the specimen shall meet the circuitry requirement (see 5.14.10) and shall exhibit no measling or crazing in excess of that allowed in 5.14.7, and no cracking, separation of the plating and conductors, blistering, or delamination.

5.15 Quality Assurance Provisions

5.15.1 Responsibility for Inspection

Unless otherwise specified, the supplier shall be responsible for the performance of all inspection requirements as specified herein. The supplier may use its own or any other facility, subject to customer approval. MSFC and the procuring organization reserves the right to perform any of the inspections set forth in the specification, where such inspections are deemed necessary to assure that supplies and services conform to prescribed requirements.

5.15.2 Test Equipment and Inspection Facilities

The supplier shall provide and maintain test and measurement equipment and inspection facilities sufficient to perform the required inspections. Accuracy of the measuring and test equipment shall be assured by means of a calibration system as required in 4.4.

5.15.3 Classification of Inspection

The inspections specified herein are classified as follows:

a. Materials inspection (see 5.15.4).

b. Supplier qualification inspection (see 5.15.5).

c. Quality conformance inspection (see 5.15.6).

5.15.4 Materials Inspection

Materials inspection shall consist of certification, supported by verifying data based on statistical sampling that all materials that become a part of the finished product are in accordance with the specified requirements.

5.15.5 Supplier Qualification Inspection

When required, qualification inspection shall be performed at a laboratory acceptable to the procuring organization, on the test specimens produced with material, equipment, and procedures that will be used in subsequent production. The qualification test specimens shall consist of two test boards of an actual production configuration together with the associated test coupons that meet the requirements of IPC-2221. Separate qualification will be required for each resin system employed. Qualification inspection shall consist of the examinations and tests specified in Table III. One failure shall be sufficient cause for refusal to grant qualification approval.

5.15.6 Quality Conformance Inspection

Quality conformance inspection shall consist of material verification per 5.15.4 and examinations or tests on the production boards and the quality conformance test coupons as shown in Table IV. Features of the boards shall be measured at 3X magnification. Referee magnification for board features shall be as required. Each Type 3 production board or panel of boards shall incorporate the quality conformance test coupons as specified herein or on the approved engineering drawing. Two coupons (one thermally stressed and one as manufactured) shall be microsectioned, inspected by the supplier, and provided to the procuring organization along with the remaining coupons in the strip. The supplier shall retain the remainder of unused quality conformance test coupons for one year unless otherwise specified. Metallographic preparation shall be performed in accordance with IPC-TM-650, Method 2.1.1, except plating thickness shall not be determined by averaging and magnification for plated-through hole quality and plating thickness shall be conducted at 200X minimum with upward adjustment allowable to resolve suspected discrepancies.

5.15.7 Inspection Lot

An inspection lot shall consist of all boards fabricated from the same materials, using the same processing procedures, produced under the same conditions in one tank load in a batch plating operation or in one shift's production in an automated line, and offered for inspection at one time.

5.15.8 Sampling Plan

All Type 3 (multilayer) boards shall be inspected 100 percent. Sampling for Types 1 and 2 shall be by the C=O sampling plan specified in Table V. The Index Values at the top of each sample size column associates to the A.Q.L. level. For a lot to be accepted, all samples shall conform to the requirements. A lot is withheld if one or more samples are non-conforming. A withheld lot is not considered rejected until a review by the supplier and customer is completed to assess the extent and seriousness of the non-conformance.

Table III. Qualification Inspection

EXAMINATION OR TEST	REQUIREMEMT AND METHOD PARAGRAPH	QUAL TEST SPECIMEN NUMBER	TEST COUPON BY BOARD TYPE			ENTIRE TEST BOARD
			1	2	3	
Visual and dimensional						
Dimensions	5.1	1, 2	–	–	–	X
Conductor width & spacing	5.2	1, 2	–	–	–	X
Measling & crazing	5.3	1, 2	–	–	–	X
Delamination	5.4	1, 2	–	–	–	X
Conductor outgrowth	5.6	2	–	–	–	X
Bow & twist	5.7	1, 2	–	–	–	X
External annular ring	5.13.2 5.14.4	1, 2 2	–	–	–	X
Marking	5.11	1, 2	–	–	–	X
PTH microsection						
PTH	5.14.1	2	–	Coupon[1]	Coupon	–
Plating thickness	5.14.3	2	–	Coupon	Coupon	–
Etchback	5.14.2	2	–	Coupon	Coupon	–
Undercutting	5.5	2	–	Coupon	Coupon	
Dielectric thickness	5.14.5	2	–	Coupon	Coupon	–
Layer to layer registration	5.14.6	2	–		Coupon	–
Internal annular ring	5.14.4	2	–	–	Coupon	–
Plating adhesion	5.8	1, 2	Coupon	Coupon	Coupon	–
Thermal stress	5.14.7	1	–	Coupon	Coupon	–
Hole solderability	5.14.8	1	–	Coupon	Coupon	–
Rework solderability	5.14.9	1	–	Coupon	Coupon	–
Dielectric Withstanding Voltage (DWV)	5.9	1	Coupon	Coupon	Coupon	–
Circuitry	5.14.10	2	–	–	Coupon	–
Thermal shock	5.14.11	2	–	–	Coupon	–
Solder mask	5.12					

Note 1. Coupon selected by supplier unless otherwise specified in engineering documentation. Coupons must meet specimen requirements of this standard and of IPC-2221.

Table IV. Quality Conformance Inspection

EXAMINATION OR TEST	REQUIREMENT & METHOD PARAGRAPH	UNPLATED TYPE 1 AND 2		PLATED TYPE 2		TYPE 3	
		SPEC	FREQ	SPEC	FREQ	SPEC	FREQ
Visual and dimensional							
Dimensions	5.1	Board	Sample	Board	Sample	Board	100%
Conductor width & spacing	5.2	Board	Sample	Board	Sample	Board	100%
Measling & crazing	5.3	Board	Sample	Board	Sample	Board	100%
Delamination	5.4	Board	Sample	Board	Sample	Board	100%
Conductor outgrowth	5.6	Board	Sample	Board	Sample	Board	100%
Bow & twist	5.7	Board	Sample	Board	Sample	Board	100%
External annular ring	5.13.2 5.14.4	Board Board	Sample Sample	Board Board	Sample Sample	Board Board	100% 100%
Marking	5.11	Board	Sample	Board	Sample	Board	100%
PTH microsection							
PTH	5.14.1	N/A	N/A	Coupon[2]	Sample	Coupon	Note 1
Plating thickness	5.14.3	N/A	N/A	Coupon	Sample	Coupon	Note 1
Etchback	5.14.2	N/A	N/A	Coupon	Sample	Coupon	Note 1
Undercutting	5.5	N/A	N/A	Coupon	Sample	Coupon	Note 1
Dielectric thickness	5.14.5	N/A	N/A	Coupon	Sample	Coupon	Note 1
Layer to layer registration	5.14.6	N/A	N/A	Coupon	Sample	Coupon	Note 1
Internal annular ring	5.14.4	N/A	N/A	Coupon	Sample	Coupon	Note 1
Plating adhesion	5.8	Board	Sample	Board	Sample	Board	100%
Thermal stress	5.14.7	N/A	N/A	Coupon	Sample	Coupon	Note 1
Hole solderability	5.14.8	N/A	N/A	Coupon	Sample	Coupon	Note 1
Circuitry	5.14.10	N/A	N/A	N/A	N/A	Board	100%
Solder mask	5.12						

Note 1. Two coupons per panel (one thermally stressed and one as manufactured) shall be tested and microsectioned for Type 3 boards.
Note 2. Coupon selected by supplier unless otherwise specified in engineering documentation. Coupons must meet specimen requirements of this standard and of IPC-2221.

Table V. C=O (zero defects) Sampling Plans

	Index Value			
Lot Size	**0.10**	**1.0**	**2.5**	**4.0**
1–8	All	All	5	3
9–15	All	13	5	3
16–25	All	13	5	3
26–50	All	13	5	5
51–90	All	13	7	6
91–150	125	13	11	7
151–280	125	20	13	10
281–500	125	29	16	11

6.0 NOTES

This document replaces MSFC-STD-2907 dated February 5, 1999.

PACKAGE NO. 10443R

DOCUMENTATION RELEASE LIST
GEORGE C. MARSHALL SPACE FLIGHT CENTER

MSFC CODE IDENT 14981/339B2
ISSUE DATE FEB 22 2007

C H	DOCUMENT NUMBER	DRL DSH	DRL REV	TITLE	CCBD NO.	PCN	PC	EFFECTIVITY
*	MSFC-STD-2907	202 -		WORKMANSHIP STANDARD FOR PRINTED WIRING BOARDS	000-00-0000	0000000	ZA	NONE

CHG NO.	CHG REV	CHG NOTICE	RESPONSIBLE ENGINEER	RESPONSIBLE ORGANIZATION	ACTION DATE	DESCRIPTION
			MARK STRICKLAND	CR30	02/12/99	BASELINE RELEASE
*	1	DCN000	EUGENA GOGGANS	EO03	02/22/07	DOCUMENT RELEASED THRU PDS. NO LONGER TRACKED IN ICMS.

CHECKER

N/A
02/15/07

(FINAL)

PACKAGE NO: 10443R

PROGRAM/PROJECT: MULTI LAST UPDATED: 02/22/07

NOMENCLATURE: MSFC-STD- GOING TO NONE EFFECTIVITY

ECR NO:	PCN:	CCBD NO:	DATE PREPARED:
E003-0000	0000000	000-00-0000	02/22/07
		SB3-00-0000	

DWG SIZE	DRAWING NUMBER	DWG REV	EPL/DRL/DDS NUMBER	DWG REV	EPL DSH	EPL REV	EO DASH NUMBER	EO REV	PART NUMBER
			MSFC-HDBK-1453		202	-			
			MSFC-HDBK-1674		202	-			
			MSFC-HDBK-2221		203	-			
			MSFC-HDBK-505		202	-			
			MSFC-HDBK-670		202	-			
			MSFC-MNL-1951		209	-			
			MSFC-PROC-1301		202	-			
			MSFC-PROC-1721		202	-			
			MSFC-PROC-1831		202	-			
			MSFC-PROC-1832		202	-			
			MSFC-PROC-404		202	-			
			MSFC-PROC-547		202	-			
			MSFC-QPL-1918		204	-			
			MSFC-RQMT-1282		202	-			
			MSFC-SPEC-1198		202	-			
			MSFC-SPEC-1238		202	-			
			MSFC-SPEC-1443		202	-			
			MSFC-SPEC-164		202	-			
			MSFC-SPEC-1870		202	-			
			MSFC-SPEC-1918		203	-			
			MSFC-SPEC-1919		206	-			
			MSFC-SPEC-2083		202	-			
			MSFC-SPEC-2223		202	-			
			MSFC-SPEC-2489		206	-			
			MSFC-SPEC-2490		205	-			
			MSFC-SPEC-2491		203	-			
			MSFC-SPEC-2492		203	-			
			MSFC-SPEC-2497		211	-			
			MSFC-SPEC-250		202	-			
			MSFC-SPEC-445		202	-			
			MSFC-SPEC-504		202	-			
			MSFC-SPEC-521		202	-			
			MSFC-SPEC-548		202	-			
			MSFC-SPEC-560		202	-			
			MSFC-SPEC-626		202	-			
			MSFC-SPEC-684		202	-			
			MSFC-SPEC-708		202	-			
			MSFC-SPEC-766		202	-			
			MSFC-STD-1249		202	-			
			MSFC-STD-1800		202	-			
			MSFC-STD-246		202	-			
			MSFC-STD-2594		203	-			

PACKAGE NO: 10443R

DWG SIZE	DRAWING NUMBER	DWG REV	EPL/DRL/DDS NUMBER	DWG REV	EPL DSH	EPL REV	EO DASH NUMBER	EO REV	PART NUMBER
			MSFC-STD-2903		202	-			
			MSFC-STD-2904		202	-			
			MSFC-STD-2905		202	-			
			MSFC-STD-2906		202	-			
			MSFC-STD-2907		202	-			
			MSFC-STD-366		202	-			
			MSFC-STD-383		202	-			
			MSFC-STD-486		202	-			
			MSFC-STD-506		203	-			
			MSFC-STD-531		202	-			
			MSFC-STD-557		202	-			
			MSFC-STD-561		203	-			
			MSFC-STD-781		202	-			

SUBMITTED BY ENGINEERING AREA:	BASIC CHANGE	PARTIAL	COMPLETE	CLOSES ACTION
EO03	X		X	EO03

PREPARED BY:
EUGENA GOGGANS
12/19/06

SUBMITTED BY:

CONCURRENCE:

TRANSMITTAL DATES
TO RELEASE DESK 02/22/07 10:00
TO MSFC DOC REP 02/22/07 00:00

REMARKS: