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JPL D-8208, Rev. I

Spacecraft Design and
Fabrication Requirements for

Electronic Packaging and Cabling

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This document contains:

January 14, 2002

JPL
Jet Propulsion Laboratory
California Institute of Technology

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Change Incorporation Log

Change Letter	Release		Authority	Pages Affected	Date	Engineering Approval	
	Initials	Section				Initials	Section
A	JWA	648		Init. Rel.	10/1/91	DLW	358
B	JWA	644		All	8/1/94	CJB	349
C	GSR	644	Process Identification #P03.05.09.00	All	3/15/97	CJB	349
D	CD	349		All	8/15/98	CJP	349
E	CD	349	ISO	Added ISO requirements to Section 3.2, Section 3.12 needed additional crimp tool tables.	3/26/99	CJB	349
F	CD	349	ISO	Added new section 3.10, Radio Frequency.	7/26/99	CJB	349
G	CJB	349	ISO	Removed Table 3.3-4; rewrote Sections 3.6 and 3.7; corrections to paragraphs 2.1 and 4.2 and equations 7.2.4 and 7.2.6.3 in Section 3.10; corrections to Figure 3.12-1 and Table 3.12-10; and corrected Applicable Documents section as necessary	9/25/00	CJB	349
H	CJB	349	ISO	Changes to Section 3.6: Added paragraphs 4.8.2.3 and 5.3.8.4; deleted paragraph 4.8.10.2; and made corrections to drawings in Figures 3.6-2 and 3.6-9. Changes to Section 3.7: Replaced paragraphs 1.3 and 3.1.1.3 with corresponding paragraphs from Section 3.6; added paragraphs 4.8.2.3 and 5.3.8.4; deleted paragraph 4.8.9.2; and made corrections to drawing in Figure 3.7-2 Changes to Section 3.12: Added Table 3.12-13, paragraph 2.5.13.4 and paragraphs 2.5.11 thru 2.5.11.4	10/26/00	CJB	349

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Change Letter	Release		Authority	Pages Affected	Date	Engineering Approval	
	Initials	Section				Initials	Section
I	CJB	349	ISO	Changes to Section 2: Modified paragraph 2.7; made additions to paragraph 4. Changes to Section 3.2: Added paragraph 1.13.6; modified paragraph 1.13.8.1 (1.13.7.1 in Rev. H). Changes to Section 3.5: Modified paragraph 1; altered paragraph 1.1; modified paragraphs 2 and 2.1 and changed paragraph numbering as a consequence; corrected paragraph 2.1.3.5 (2.2.3.5 in Rev. H). Extensive changes made to Section 3.6: much of it has been rewritten. Several new tables were added-Tables 3.6-1, 3.6-9, 3.6-10; Tables 3.6-2, 3.6-3, 3.6-5, and 3.6-7 were modified; paragraph 3.1.1.1 was totally rewritten with Table 3.6-1 added; paragraph 3.1.1.2 was largely rewritten; much of paragraphs 4.4.1, 4.4.1.1, 4.4.2, 4.4.2.1, 4.4.2.2, and 4.4.3 were rewritten. Added new Figures 3.6-4, 3.6-5, 3.6-8, and 3.6-9; paragraphs 4.8.13, 4.8.13.1, 4.8.13.2, 4.8.13.3, 4.8.13.4, 4.8.14, 4.8.15, 4.8.15.1, 4.8.15.2, 4.8.15.3, and 6.1.4 have been added; paragraphs 4.9.1, 4.9.1.1, and 4.10 have been extensively revised.	1/7/02	JKB	349

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Change Letter	Release		Authority	Pages Affected	Date	Engineering Approval	
	Initials	Section				Initials	Section
I	CJB	349	ISO	Changes in Section 3.7: Extensive changes made to this section; much of it has been rewritten. New tables 3.7-1, 3.7-9, and 3.7-10 were added; tables 3.7-2, 3.7-3, 3.7-5, and 3.7-7 were modified; paragraph 3.1.1.1 was totally rewritten with table 3.7-1 added; paragraph 3.1.1.2 was largely rewritten; much of paragraphs 4.4.1, 4.4.1.1, 4.4.2, 4.4.2.1, 4.4.2.2, and 4.4.3 were rewritten. Added new Figures 3.7-4, 3.7-5, 3.7-8, and 3.76-9; paragraphs 4.8.13, 4.8.13.1, 4.8.13.2, 4.8.13.3, 4.8.13.4, 4.8.14, 4.8.15, 4.8.15.1, 4.8.15.2, 4.8.15.3, and 6.1.4 have been added; paragraphs 4.9.1, 4.9.1.1, and 4.10 have been extensively revised. Extensive changes were made to Section 3.12: Modified paragraph 1.4.1.1; modified paragraph 1.5.4.7; modified paragraph 2.5.10.14; added paragraph 2.6; added Table 3.12-14; added paragraphs 3.3.5, 3.3.5.1, 3.3.5.2, 3.3.5.3, 3.4, 3.4.1, 3.4.2, 3.4.3, 6.1.1. Several other new paragraphs were added and minor modifications were made. Changes to Section 3.13: This entire section has been totally rewritten. Changes to Section 3.14: Modified paragraph 1; modified paragraph 1.1; paragraph 1.1.1.2 added; Figures 3.14-3 and 3.14-10 revised; added Figures 3.14-18 and 3.14-19; paragraphs 1.2.3.8 and 1.2.3.9 added; corrected paragraph 2.2.1.3 c. (2.2.2.1 c. in Rev. H); modified paragraph 3.1. Changes to Section 3.15: Modified paragraph 2.2.1; modified paragraph 2.2.2; modified paragraph 3.1.	1/7/02	JKB	349

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Change Letter	Release		Authority	Pages Affected	Date	Engineering Approval	
	Initials	Section				Initials	Section
I	CJB	349	ISO	Changes to Section 3.16: Modified Table 3.16-1; modified paragraph 4.5.1 and 4.5.1.1 (combined the contents of 4.5.1.1 into 4.5.1); several new paragraphs added such as 4.5.2; modified 4.5.3.1 (4.5.2.1 in Rev. H); modified some of the other paragraphs in 4.5; Table 3.16-3 changed considerably. Changes to Section 3.17: Modified paragraph 1.8.3.	1/7/02	JKB	349

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Foreword

This standard is not intended to be self-imposing, but recommends preferred engineering practices for programs, projects, and tasks. It may be cited in contracts and program documents as a technical requirement or as a reference for guidance. Determining the suitability of this standard and its provision is the responsibility of the performing organization. Individual provisions of this standard may be tailored (i.e., modified or deleted) by contract or program specifications to meet specific program/project/task needs and constraints.

1 PURPOSE

The requirements included here have been qualified for use on JPL flight hardware systems by a combination of formal qualification testing and flight application. The applicability of this document is defined in JPL D-12872, "*JPL Process for Tailoring Mission Assurance to Specific Projects*."

For contracted tasks it is often desirable to rely, to the maximum extent possible, on the project assurance practices of the vendor/contractor. Requests for proposal should state that the contractor should meet the intent of D-8208; any significant differences between their packaging standards and those of D-8208 should be clearly identified. Vendor survey, documentation review, and negotiation should establish the applicable contractor documentation to incorporate into the contract and, if necessary, include modification/additions necessary to the contractors documentation/processes.

This document should be used from a concurrent engineering point of view. There are a number of critical issues to be addressed at the design/packaging design stage that cannot be taken up after the fact without either seriously compromising the project goals or costing more than was anticipated. All relevant disciplines, engineering and otherwise, should be brought into play, preferably by forming a work team at the conceptual design stage and before any of the critical design decisions have been made.

This document is also to be used in accord with ISO 9001 registration and periodic registration reassessments for the continued maintenance and improvement of the product delivery system . The chief ISO elements affecting this document are:

- Design Control, especially Design Input, Design Output, and Design Changes (Design Requirement)

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- Process Control (Fabrication Requirement)
- Control of Inspection, Measuring, and Test Equipment (Fabrication Requirement)
- Inpection and Test Status (Fabrication Requirement)
- Control of Nonconforming Product (Fabrication Requirement)
- Corrective and Preventive Action (Fabrication Requirement)
- Handling, Storage, Packaging, Preservation and Delivery (General Requirement)

2 STRUCTURE

This document is structured such that each section contains the design, fabrication, and quality assurance requirements. It is written in specification format with single “shall” statements; making it easier to identify the individual requirements as an aid to generating lists of specific items to be incorporated into design drawings, notes, and correspondence. Commercial specifications have been included wherever possible, and new technologies will be added as they become qualified for flight.

Cross references internal to each Section are shown in red, and cross references to other Sections are blue. Each one is “linked” to the actual object; clicking on it will take you to the item referenced.

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Applicable Documents

1 JET PROPULSION LABORATORY

The documents listed in this section form a part of this standard to the extent specified herein. These documents are available on-line at **http://dmie.jpl.nasa.gov**, **http://standards.pl.nasa.gov**, or in Section 349's central documentation area.

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1.1 Specifications

Title	Document Number	Rev.	Official Date	Process/ Subprocess
Safety Requirements for Spacecraft Mechanical Support Equipment	ES501492	F	02/21/98	-
Preparation and Application of Epoxy-Polymer Adhesive, Detail Specification for	FS502752	C	10/27/98	Polymerics
Torque Requirements, Fasteners, Structural	ES504255	I	02/09/99	-
Preparation of Surfaces for Adhesive Bonding, Detail Specification for	FS504508	S	10/27/98	Polymerics
Installation and Removal of Key-Locked Threaded Inserts, Detail Specification for	FS505925	D	08/15/83	Mechanical
Vacuum Outgassing of Polymers (Micro-VCM Technique), Test Specification for	TS507035	B	05/05/88	-
Lead Forming and Trimming for Integrated Circuits, Detail Procedure for	EP513209	B	08/11/88	Component Mounting
Assembly and Wiring of Electronic Equipment and Assemblies, Manufacturing Processes and Procedures for	FP513414	G	09/25/00	Electronic Packaging and Cabling
Footprint Requirements for Printed Wiring Boards, Detail Specification for	CS515520	A	-	Component Mounting

1.2 Drawings

Title	Document Number	Rev.	Official Date	Process/ Subprocess
Socket Force Retention Tool	10090277-1	A	02/15/86	-
Wire-wrap Retainer	10117788	A	02/15/86	-
Tubing, Insulation, Heat Shrinkable Polyolefin	ST10017	G	05/09/96	-
Clip, Rectangular Connector, Lock	ST10043	D	01/14/92	-
Screw, Rectangular Connector, Lock, Cres	ST10044	E	12/16/91	-
Stud, Rectangular Connector, Lock, Cres	ST10046	A	03/28/67	-
Nut, Captive Washer, Self-Locking, Cres	ST10049	D	01/06/92	-
Nut, Hexagon, Self-Locking, Cres	ST10060	D	07/05/94	-

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Title	Document Number	Rev.	Official Date	Process/ Subprocess
Screw, Panhead, “Hi-Torque,” Recess Locking	ST10073	E	12/21/98	-
Connector, Elec., Hermetic Rec., Jam-Nut, Mounting	ST10078	M	03/05/80	-
Connector, RF, Twinax Receptacle	ST10196	F	09/21/00	-
Connector, RF, Twinax Plug	ST10197	F	09/21/00	-
Magnet Wire, 150 C Insulation	ST10219	G	11/14/91	-
Terminal, Electrical, Slotted, Swage Mount	ST10591	A	11/14/91	-
Magnet Wire, Class 105, Bondeze, Self Adhesive Ins.	ST10865	A	08/11/67	-
Wire, Magnet, Copper, 130°C, Insulation, Type UN2	ST10866	A	10/07/81	-
Magnet Wire, 200 C Insulation	ST11027	C	10/07/81	-
Terminal, Electrical, Bifurcated, Swage Mount	ST11076	G	11/14/91	-
Terminal, Electrical, Bifurcated, Swage Mount	ST11204	G	11/14/91	-
Terminal, Electrical, Bifurcated, Swage Mount	ST11205	F	11/14/91	-
Terminal, Electrical, Bifurcated, Swage Mount	ST11299	F	11/14/91	-
Insert, Threaded, Miniature, CRES Non-locking	ST11326	G	03/23/94	-
Connector, Elec., Hermetic Rec., Jam-Nut Mounting	ST11376	F	02/05/76	-
Connector, Saver, Elec., Rectangular, Non-magnetic	ST11488	G	02/13/81	-
Form, Radiation Barrier, Flat Package	ST11913	B	01/27/76	-
Cover, Radiation Barrier, Flat Package	ST11914	D	12/02/80	-
Stud, Rectangular Connector Saver, Mounting	ST11940	C	12/02/99	-
Connector, Elec., Female Contact, Crimp Type, Rect.	ST11956	C	01/12/79	-
Connector, Elec., Mail Contact, Crimp Type, Rect.	ST11957	C	01/12/79	-
Clip Connector, Micro D	ST11976	B	01/14/92	-
Screw, Connector, Micro D, Locking	ST11977	C	12/16/91	-

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Title	Document Number	Rev.	Official Date	Process/ Subprocess
Studlock, Connector, Micro D	ST11978-2	B	03/15/90	-
Form, IC Shield	ST11994	A	12/02/80	-
Cover, IC Shield	ST11995	D	08/25/81	-
Base, IC Shield	ST11996	B	09/28/82	-
Shield, IC	ST11997	D	08/25/81	-
Connector Saver, Elec., Repairable, Non-mag.	ST11998	C	01/14/92	-
Cover, Radiation Barrier, Flat Pkg., (Harris Series)	ST11999	B	09/09/82	-
Screw, Rectangular Connector, Lock, Cres, Special	ST12009	D	12/16/91	
Connector, Elec., High-density, Male, Crimp Type	ST12023	A	01/01/89	-
Connector, Elec., High-density, Female, Crimp Type	ST12024	A	02/01/89	-
Terminal, Elec., Rounded, Swage Mount, High-Voltage	ST12047	B	11/14/91	-
Terminal, Elec., Rounded, Swage Mount, High-Voltage	ST12048	B	11/14/91	-
Terminal, Elec., Rounded, Swage Mount, High-Voltage	ST12049	B	11/14/91	-
Terminal, Elec., Rounded, Swage Mount, High-Voltage	ST12050	B	11/14/91	-
Wire, Magnet 155°C , Insulation, Type Spun	ST12281	A	04/29/94	-

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1.3 Standards

Title	Document Number	Rev.	Official Date	Process/ Subprocess
JPL Standard for System Safety (601/40)	D-560	B	06/93	-
Electrostatic Control for Assembly and Test Areas for Flight Projects	D-1348	D	09/17/99	-
JPL Process for Tailoring Mission Assurance to Specific Projects	D-12872	-	01/97	-
Electronic Parts Program Requirements for Flight Equipment	D-5357	-	11/21/90	-
Electrostatic Discharge Control Products Standards Handbook	D-6970	-	03/90	-
Drafting Manual	STD00001	C	11/09/98	-
Flight Materials, Processes, Fasteners, Packaging and Cabling Hardware Selection Guide	STD00009	B	04/01/93	-

1.4 Miscellaneous

Title	Document Number	Rev.	Official Date	Process/ Subprocess
Surface Mount Workmanship Standards	IOM 3490-94-230	A	05/12/94	-

2 COMMERCIAL

2.1 AMS

Title	Document Number	Rev.	Official Date	Process/ Subprocess
Foam, Flexible, Polyurethane Foam, Open Cell, Medium Flexibility	AMS-3570	-	-	-

2.2 ANSI

Title	Document Number	Rev.	Official Date	Process/ Subprocess
Dimensioning and Tolerances	ANSI Y14.5	M	1994	-
Requirements for Soldered Electrical and Electronic Assemblies	ANSI/J-STD-001	B	10/96	-

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Title	Document Number	Rev.	Official Date	Process/ Subprocess
Requirements for Soldering Fluxes	ANSI/J-STD-004	-	01/95	-
Requirements for Soldering Pastes	ANSI/J-STD-005	-	01/95	-
Requirements for Electronic Grade Solder Alloys and Fluxes and Non-fluxes Solid Solders for Electronic Soldering Applications	ANSI/J-STD-006	-	01/95	-

2.3 ANSI/IEEE

Title	Document Number	Rev.	Official Date	Process/ Subprocess
Versatile Backplane Bus VME, Section 7	ANSI/IEEE 1014	-	3/87	-

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2.4 ANSI/IPC

Title	Document Number	Rev.	Official Date	Process/ Subprocess
Acceptability of Printed Boards	ANSI/IPC-A-610	E		
Qualification and Performance of Electrical Insulating Compound for Printed Board Assemblies	ANSI/IPC-CC-830	-	04/90	-
Guidelines for Cleaning Printed Boards and Assemblies	ANSI/IPC-CH-65	-	12/90	-
Guidelines for Printed Board Component Mounting	ANSI/IPC-CM-770	D	01/96	-
Specification for Single- and Double-sided Flexible Printed Wiring	ANSI/IPC-D-250	A	09/86	-
Design Standards for Rigid Printed Boards and Rigid Printed Board Assemblies	ANSI/IPC-D-275	-	09/91	-
Suggested Guidelines for Modification, Rework, and Repair of Printed Boards and Assemblies	ANSI/IPC-R-700	C	01/88	-
Post Solder Solvent Cleaning Handbook	ANSI/IPC-SC-60	-	04/87	-
Pre and Post Solder Mask Application Cleaning Guidelines	ANSI/IPC-SM-839	-	04/90	-

2.5 ASTM

Title	Document Number	Rev.	Official Date	Process/ Subprocess
Specification for Methyl Ethyl Ketone	ASTM D740-94	-	94	-
Standard Test Method for Oxidation Stability of Mineral Insulating Oil	ASTM D2440	-	93	-

2.6 IEEE

Title	Document Number	Rev.	Official Date	Process/ Subprocess
Mechanical Core Specification for Conduction-Cooled Eurocards	IEEE 1101.2	-	92	-

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2.7 IPC

Title	Document Number	Rev.	Official Date	Process/ Subprocess
Generic Performance Specification for Printed Boards	IPC-6011	-	1996	PWB Fab
Qualification and Performance Specification for Rigid Printed Boards	IPC-6012	A	10/99	PWB Fab
Qualification and Performance Specification for Flexible Printed Board	IPC-6013	-	11/98	PWB Fab
Manufacturer's Qualification Profile (MQP)	IPC-1710	A	12/97	PWB Vendor Selection
Generic Standard on Printed Board Design Amendment	IPC-2221	-	7/99	PWB Layout
Sectional Design Standard for Rigid Organic Printed Boards	IPC-2222	-	7/99	PWB Layout
Sectional Design Standard for Flexible Printed Boards	IPC-2223	-	7/99	PWB Layout
Specification for Base Materials for Rigid and Multilayer Printed Boards	IPC-4101	-	5/99	PWB Fab
Acceptability of Printed Boards	IPC-A-600	E	11/99	PWB Fab
Acceptability of Electronic Assemblies	IPC-A-610	C	2000	PWB Assy
Post Solder Aqueous Cleaning Handbook	IPC-AC-62	A	12/86	Cleaning
Metal Foil for Printed Wiring Applications	IPC-CF-150	F	08/92	-
Guidelines for Printed Board Component Mounting	IPC-CM-770	D	01/96	-
Flexible Bare Dielectric for Use in Flexible Printed Wiring	IPC-FC-231	C	04/92	-
Specification for Adhesive Coated Dielectric Films for Use as Cover Sheet for Flexible Printed Wiring	IPC-FC-232	C	04/92	-
Flexible Adhesive Bonding Films (Note: This document is actually part of IPC-FC-232.)	IPC-FC-233	-	-	-
Metal-Clad Flexible Dielectric for Use in Fabrication of Flexible Printed Wiring	IPC-FC-241	C	04/92	-

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Title	Document Number	Rev.	Official Date	Process/ Subprocess
Design Standard for Flexible One- and Two-Sided Printed Boards	IPC-D-249	-	01/87	-
Specification for Single- and Double-Sided Flexible Printed Wiring	IPC-FC-250	-	09/86	-
Design Guide for High Density Interconnects (HDI) and Microvias	IPC/JPCA-2315	-	06/00	
Performance Specification for Rigid-Flex Printed Boards	IPC-RF-245	O	04/87	-
Post Solder Semiaqueous Cleaning Handbook	IPC-SA-61	-	04/94	-
Surface Mount Design and Land Pattern Standard	IPC-SM-782	A	08/93	-
Qualification and Performance of Permanent Solder Mask	IPC-SM-840	C	01/96	-
Terms and Definitions for Interconnecting and Packaging Electronic Circuits	IPC-T-50	E/F	07/96	-
Cleaning and Cleanliness Test Program Phase 1 Test Results	IPC-TR-580	-	10/89	-

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2.8 Miscellaneous

Title	Document Number	Rev.	Official Date	Process/ Subprocess
Isopropyl Alcohol	TT-I-735	A	11/05/91	-
Naphtha, Aliphatic	TT-N-95	B	11/05/91	-
Toluene, Technical	TT-T-548	F	11/05/91	-

3 MILITARY

3.1 Specifications

Title	Document Number	Rev.	Official Date	Process/ Subprocess
Anodic Coatings, for Aluminum and Aluminum Alloys	MIL-A-8625	F	09/10/93	-
Copper Plating, Electrodeposited	MIL-C-14550	B	03/20/87	-
Chemical Conversion Coatings on Aluminum and Aluminum Alloys	MIL-C-5541	E	11/30/90	-
Desiccants, Activated, Bagged, Packaging Use and Static Dehumidification	MIL-D-3464	E	04/21/87	-
Crimping Tool, Hand or Power Actuated, Wire Termination, Tool Kit, General Specification for	MIL-DTL-22520	G	09/12/97	-
Flux, Soldering, Liquid (Rosin Base)	MIL-F-14256	F	06/15/95	-
Gold Plating, Electrodeposited	MIL-G-45204	C	06/09/93	-
Glass Beads: For Cleaning and Peening	MIL-G-9954	A	04/25/96	-
Hybrid Custom Microcircuits, General Specification for	MIL-H-38534	-	-	-
Insulating, Plastic, Laminated, Thermosetting, Glass Cloth Epoxy Resin, GEE-F	MIL-I-24768/2	-	12/08/92	-
Microcircuits, General Specification for	MIL-M-38510	J	08/27/93	-
Plastic Sheet, Laminated, Metal Clad (for Printed Wiring Boards), General Specification for	MIL-P-13949	-	-	-

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Title	Document Number	Rev.	Official Date	Process/ Subprocess
Plastic Sheet, Laminated, Thermosetting, Glass Faber Base, Eposy-Resin	MIL-P-18177	C	01/25/92	-
Printed Wiring Board, Flexible And Rigid-flex, General Specification For	MIL-P-50884	H	-	
Printed Wiring Boards	MIL-P-55110	H	-	-
Plating, Tin-Lead, Electrodeposited	MIL-P-81728	A	03/28/80	-
Quality Program Requirements	MIL-Q-9858	A	10/01/96	-
Screw Threads, Standards, Optimum Selected Series, General Specification for	MIL-S-7742	D	09/02/92	-
Transformers and Inductors (Audio, Power, and High Power Pulse), General Specification for	MIL-PRF-27	F	06/06/94	-
Terminal Lugs, Splices of Conductors, Crimp Style, Copper, General Specification for	MIL-T-7928	G	12/19/80	-
1,1,1-Trichloroethane Methyl Chloroform) Inhibited, Vapor Degreasing	MIL-T-81533	A	10/29/01	-
Wiring, Aerospace Vehicle	MIL-W-5088	L	12/10/92	-
Wire, Electrical, Solderless Wrap, Insulated and Uninsulated, General Specification for	MIL-W-81822	A	03/15/94	-

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3.2 Standards

Title	Document Number	Rev.	Official Date	Process/ Subprocess
Engineering Drawing Practices	MIL-STD-100	F	09/09/96	-
Standard General Requirements for Electronic Equipment	MIL-STD-454	N	05/04/95	-
Reliability Program for System and Equipment Development and Production	MIL-STD-785	B	08/05/88	-
Test Methods and Procedures for Microelectronics	MIL-STD-883	E	12/31/96	-
Test Methods and Procedures for Microcircuit Line Certification	MIL-STD-977	-	11/15/94	-
Electrostatic Discharge Control Program for Protection of Electrical and Electronic Parts, Assemblies and Equipment (Excluding)	MIL-STD-1686	C	10/25/95	-
Product Assurance Provisions for Custom Hybrid Microcircuits Line Certification of Fabrication Processes	MIL-STD-1772	B	02/20/96	-
Military Standards for Flexible and Rigid Flexible Printed Wiring for Electronic Assemblies, Requirements for	MIL-STD-2118	-	05/12/86	-
Calibration System Requirements	MIL-STD-45662	-	04/28/95	-

3.3 Department of Defense

Title	Document Number	Rev.	Official Date	Process/ Subprocess
Electrostatic Discharge Control Handbook for Protection of Electrical and Electronic Parts, Assembly and Equipment (Excluding Electrically Initiated Explosive Devices)	DoD HDBK-263	-	-	-

3.4 Miscellaneous

Title	Document Number	Rev.	Official Date	Process/ Subprocess
Acetone, Technical	O-A-51	H	07/22/96	-
Ethyl Alcohol (Ethanol) Denatured Alcohol and Proprietary Solvent	O-E-760	D	09/09/93	-

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Title	Document Number	Rev.	Official Date	Process/ Subprocess
Methanol, Technical (Methyl Alcohol)	O-M-232	J	11/19/90	-
1,1,1 Trichloroethane, Technical Inhibited (Methyl Chloroform)	O-T-620	C	01/04/93	-
Trichloroethylene, Technical	O-T-634	C	04/06/93	-
Qualified Manufacturers List of Custom Hybrid Microcircuits	QML-38534	-	04/03/95	-
Qualified Manufacturers List of Microcircuits Manufacturers	QML-38535	-	-	-

4 NASA

Title	Document Number	Rev.	Official Date	Process/ Subprocess
Material Selection List for Space Hardware Systems	MSFC HDBK-527	-	-	-
Flammability, Odor and Offgassing Requirements and Test Procedures for Materials in Environments that Support Combustion	NHB 8060.1B	-	-	-
Workmanship Standard for Staking and Conformal Coating of Printed Wiring Boards and Electronic Assemblies	NASA-STD-8739.1	-	08/06/99	Polymeric Applications
Workmanship Standard for Surface Mount Technology	NASA-STD-8739.2	-	08/31/99	Surface Mount Technology
Soldered Electrical Connections	NASA-STD-8739.3 w/ Change 2	-	12/15/97	Component Mounting/ Soldering
Crimping, Interconnecting Cables, Harnesses, and Wiring	NASA-STD-8739.4	-	02/09/98	Cabling and Wiring
Fiber Optic Terminations, Cable Assemblies, and Installation	NASA-STD-8739.5	-	02/09/98	Fiber Optics

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5 FEDERAL

Title	Document Number	Rev.	Official Date	Process/ Subprocess
Airborn Particulate Cleanliness Classes in Clean Rooms and Clean Zones	FED-STD-209	E	09/11/92	-
Federal Thread Standard Handbook	H-28	-	-	-
1989 Industrial Laminated Thermal Setting Products	NEMA LI-1	-	-	-
Nickel Plating, Electrodeposited	QQ-N-290	A	11/12/71	-
Solder; Tin-Alloy; Lead-Tin Alloy; and Lead Alloy	QQ-S-571	F	06/15/95	-

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Document Structure

This document is structured such that each section contains a specific fabrication "discipline": soldering, adhesives, cleaning, etc. It is written in specification format with single "shall" statements; making it easier to identify the individual requirements as an aid to designer in generating lists of specific items to be incorporated into design drawings and notes. Commercial specifications have been included wherever possible, and new technologies will be added as they become qualified for flight.

- Definitions and Terms
- Mechanical Requirements
- Thermal Requirements
- Surface Mount Technology
- Printed Wiring Boards
- Flexible Printed Wiring
- Wire Wrap
- High Voltage Packaging
- Radio Frequency
- Hybrids and Multichip Modules
- Cabling and Wiring
- Magnetics
- Manual Component Mounting
- Repair
- Cleaning
- Polymerics
- Shipping and Handling

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Definitions, Terms, and Acronyms

1 TERMS

The terms used throughout this document are as defined in IPC T-50E with the following exclusions, exceptions, additions, and clarifications.

1.1 Exclusions

The definitions for the following terms and acronyms are omitted from the IPC T-50E:

Term
antistatic material
glassivation
insulative material
production master
ultimate heat sink

Acronym
JCIMRB
PAL
V_{CC}
V_{EE}
VSO
V_{TT}

1.2 Exceptions

Use the following definitions instead of those provided by IPC T-50E:

Term	Definition
antistatic material	ESD-protective material having a surface resistivity greater than 10^9 but not greater than 10^{12} ohms per square.
blow hole	A solder connection with a small hole penetrating from the surface of the solder to a void of indeterminate size within the solder connection. Also called pin hole.

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Term	Definition
conformal coating	A coating applied over electronic components and electrical conductors to provide electrical insulation, support, moisture protection and environmental isolation.
embedment	The complete encasement of a component or module in a resin using molds that separate from the component or module after the resin has cured.

1.3 Additions

The following definitions are used in addition to the IPC T-50E:

Term	Definition
creepage	A condition, usually of an increasing current, through or over the surface of a medium between different electrical potentials, resulting in a lower path of resistance.
concurrent engineering	The integration of all the various activities, both engineering and otherwise (e.g., purchasing, facilities, etc.) in parallel fashion and with open communication during the product design, development, and build cycle to ensure minimal cost, faster time-to-market, and a product which the customer wants and feels satisfied with.
control of inspection, measuring and test equipment	The use of various equipments to perform inspection, measuring, and testing ensuring the conformance of product to specified requirements must be controlled, maintained, and calibrated when necessary. The measurement uncertainty must be determined and documented and consistent with the required measurement capability. Proper documentation must be maintained.
control of nonconforming product	The required steps ensuring that nonconforming product (see below) is kept segregated from conforming product such that there is no confounding of the two. Proper documentation must be maintained.
corrective and preventive action	The required steps ensuring that the product delivery system is maintained in proper working order and deviations are understood and eliminated in a systematic and rational fashion. Proper documentation must be maintained.

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Term	Definition
design input	All inputs entering the process of designing a product.
design output	All outputs of the design process. Typically these will consist of a set of engineering drawings.
design changes	Changes made to the design output after the initial design has been completed. Normally these are executed as engineering change orders (ECOs).
electronic component	An electronic part such as a resistor, capacitor, diode, integrated circuit or transistor.
electronic hardware and equipment	Electronic assemblies, electronic circuit card assemblies, surface mount assemblies, hybrid assemblies (including MCMs), cable and harness assemblies (including connector mating faces, insulation, fastening devices and associated brackets and hardware forming the assembly), subassemblies, and completed electronic boxes.
engineering change order	An order calling out a change to the design output.
eutectic	A mixture or alloy with a melting point lower than that of the individual components.
handling, storage, packaging, preservation and delivery	All the operations involved in handling the product from incoming parts (e.g., piece parts, PWBs, etc.), storage of work-in-progress (WIP), steps taken to ensure the preservation of the product during fabrication and assembly, packaging the product to avoid damage and contamination, and delivery of the product to the customer in a satisfactory state. Proper documentation must be maintained.
inspection and test status	The exact status of a product in the product delivery system regarding its conformance or nonconformance to the specified requirements. Proper documentation must be maintained.
ISO 9000	An international set of quality management system standards.
ISO 9001	An international standard for a quality management system comprising design, manufacturing, and testing. ISO 9001 is composed of twenty (20) elements, nineteen (19) of which apply to the JPL PDS.

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Term	Definition
manufactured article	An article of hardware manufactured using acceptable fabrication and assembly procedures. Such articles may consist of printed wiring boards, printed wiring board assemblies, cable assemblies, hybrid assembles, etc.
measling	Add from D-8208: An internal condition in laminated base material in which the glass fibers are separated from the resin at the weave intersection. This condition manifests itself in the form of discrete white spots or “crosses” below the surface of the base material, and is usually related to thermally induced stresses.
multilayer	Replace from D-8208: A stacked array of etched printed layers laminated together.
nonconforming product	Product deviating from specified requirements to the extent that it can no longer be considered in a state useful to and/or desired by the customer.
quality management system	The total system involving all inputs, resources, and constraints to produce an output (produce/service) to a customer which the customer wants and feels satisfied with.
process control	All of the steps required to ensure that the fabrication and assembly operations are maintained in a fashion consistent with the reduction of variation, pin-pointing the cause(s) of deviation when it occurs, taking the appropriate steps to bring the system back into control (corrective action), and maintaining the system once the cause(s) of deviation have been eliminated (preventive action). Proper documentation must be maintained.
product delivery system	At JPL this term is preferred to “quality management system.

1.4 Clarifications

Insert the following words and phrases to complete the IPC T-50E definition:

Term	Definition
annular ring	Add “completely” in front of “surrounding...”
land	Also called pad.

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Term	Definition
nonpolar fluids	Add “the example fluids for each type of solvent as listed in D-8208.”
pad	Also known as land.
planar	Also known as coplanar.
plug	Also known as plug connector.
pot life	Also known as working time.
receptacle	Also known as receptacle connector.
trace	Also known as conductor.

2 ACRONYMS

The following acronyms are used throughout this document. In the case where an acronym has multiple meanings, the definition will include information regarding the context (application) in which each is used.

Acronym	Definition
AC	Aqueous Cleaning
AE	Alcohol, Ethyl, Reagent (AE) O-E-760, Type II
AQL	Acceptance Quality Level
ar	Annular ring
AR	Aspect ratio
ATP	Assembly Test Plan or Acceptance Test Procedure
BGA	Ball Grid Array
BPN	Blind Plate Nut
CAD	Computer Aided Design
CDR	Critical Design Review
CIP	Circuit Interrupt Pad
CLCC	Ceramic Leaded Chip Carrier
CMA	Circular Mil Area

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Acronym	Definition
CMOS	Complementary Metal Oxide Semiconductor
CPI	Continuous Process Improvement
CSP	Chip Scale Package
CTE	Coefficient of Thermal Expansion (generally given in PPM/°C); same as TCE
CE	Concurrent Engineering
DFC	Design For Cleanability
DFE	Design For Environment
DFI	Design For Inspectability
DFM	Design For Manufacturability
DFR	Design For Reliability
DFT	Design For Testability
DIP	Dual In-line Package
DSP	Dual Shear Plate
ECI	Engineering Change Instruction
ECL	Emitter Collector Logic
ECO	Engineering Change Order
EED	Electroexplosive Devices
EMI	Electromagnetic Interference
ESD	Electrostatic Discharge
ESDS	Electrostatic Discharge Sensitive
FEA	Finite Element Analysis
FEM	Finite Element Modeling
FHS	Finished hole size
HAT	Hybrid Assembly Traveler
HDI	High density interconnect
HSM	Hermetically Sealed Microcircuit
IC	Integrated Circuit

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Acronym	Definition
ICD	Interface Control Drawing/Document
I/L	Inner layer
I/O	Input/Output
IR	Inspection Report
JCI	JPL Critical Instruments
LCC	Leaded Chip Carrier
LLCC	Leadless Ceramic Chip Carrier
LSI	Large Scale Integrated Circuit
LTPD	Lot Tolerance Percent Defective
MCM	Multichip Module
MELF	Metal Electrode Face Bonding (Cylindrical)
MRB	Material Review Board
MS	Margin of Safety
MSDS	Material Safety Data Sheet
O/L	Outer layer
PAL	Programmable Array Logic
pbw	Parts By Weight
PCB	Printed Circuit Board
PDA	Percent Defect Allowable
PDS	Product Delivery System
PEM	Plastic Encapsulated Microcircuit
PLCC	Plastic Leaded Chip Carrier
PPM/°C	Parts Per Million/° Centigrade
PTH	Plated Through-Hole
PWB	Printed Wiring Board
QA	Quality Assurance
QML	Qualified Manufacturers List

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Acronym	Definition
QMS	Quality Management System
RFI	Radio Frequency Interference
SAC	Semiaqueous Cleaning
SC	Solvent Cleaning
SF	Safety Factor
SIP	Single In-line Package
SJ	Solder Joint
SJLPM	Solder Joint Life Prediction Model, e.g., Coffin-Manson-based model
SMC	Surface Mount Component
SMD	Surface Mount Device
SMT	Surface Mount Technology
SO	Small Outline
SOD	Small Outline VHF Switching Diode Small Outline Transistor/Diode/LED
SOIC	Small Outline Integrated Circuit Gull Wing Lead
SOJ	SOIC Package with J Leads
SOLIC	Small Outline Integrated Circuit Gull Wing Lead Wide Body
TAB	Tape Automated Bonding
TCC	Temperature Coefficient of Capacitance
TCE	Thermal Coefficient of Expansion; same as CTE
TCR	Temperature Coefficient of Resistance
T_g	Glass Transition Temperature, e.g., of a resin or an organic substrate material such as FR-4
TTL	Transistor Transistor Logic
V_{CC}	Positive reference voltage
V_{EE}	Negative reference voltage
VLSI	Very Large Scale Integrated Circuit

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Acronym	Definition
VSO	Very Small Outline
V_{TT}	Bias reference voltage
WIP	work-in-progress

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General Requirements

1 MINIMUM REQUIREMENTS

The mechanical hardware packaging design shall meet the minimum requirements of the environmental conditions of the spacecraft mission. Special emphasis shall be placed on limiting the junction temperature of all active electronic components and the deflection of printed wiring boards, within safe boundaries, to enhance the reliability of all semiconductors and protect all soldered connections.

1.1 Conflicting Requirements

In the event of any conflict between the approved drawing set, which incorporates the special technical and quality requirements of the Jet Propulsion Laboratory, and the requirements of this standard, the approved drawing set shall take precedence.

1.2 Redundant Requirements

Redundant conductor requirements and other specific reliability measures shall conform to applicable project documents.

1.3 Drawing Instructions

1.3.1 Drawing Conformance. All drawings shall conform to JPL STD00001 and ANSI Y14.5 for reproducibility.

1.4 Documentation

1.4.1 Deliverable Package. A deliverable documentation package shall be maintained for each deliverable item that includes an approved fabrication instruction, inspection data, deviation reports, and all Material Review Board (MRB) evaluations.

1.4.2 Manufacturing and Inspection Records. All manufacturing and inspection checks shall be recorded on approved fabrication instruction accompanying each manufactured article to keep an accurate history of that part.

1.4.2.1 Materials Certification. Manufacturers of the materials shall supply certification of conformance to the required and applicable specifications.

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1.4.3 Traceability. Traceability shall be maintained throughout the process from receiving or source inspection to final tests.

1.4.3.1 Reverse Traceability. The information content of each document shall be sufficient to provide reverse-traceability.

1.5 Design Control

1.5.1 Design Input. All design-input requirements relating to the product, including applicable statutory and regulatory requirements, shall be identified, documented, and their selection reviewed for adequacy. Incomplete, ambiguous, or conflicting requirements shall be resolved with those responsible for imposing the requirements.

1.5.2 Design Output. All design outputs shall be documented and expressed in terms that can be verified against design-input requirements.

1.5.2.1 Design-Input Requirements. The design output shall meet the design-input requirements.

1.5.2.2 Acceptance Criteria. The design output shall contain or make refeence to acceptance criteria.

1.5.2.3 Crucial Design Characteristics. The design output shall identify those characteristics of the design which are crucial to the safe and proper functioning of the product, including operating, storage, handling, maintenance, and if applicable, proper disposal requirements.

1.5.2.4 Review of Design-Output Documents. All design-output documents shall be reviewed prior to being released.

1.5.3 Design Changes. All design changes and modifications shall be identified, documented, reviewed, and approved by authorized personnel before their implimentation.

1.6 Materials Requirements/Material Selection

All parts and materials shall be selected from the latest revision of JPL STD00009, Engineering Standard: Flight Materials, Processes, Fasteners, Packaging and Cabling Hardware Selection Guide. In the event that a part and/or material is desired to be used, but is not found in JPL STD00009, the cognizant electronic packaging and fabrication engineers shall be consulted as to what choice(s) is (are) to be made and a permanent record kept of such change(s).

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1.7 Design for X

All electronic hardware and equipment shall be designed to allow for X, where X signifies:

- Cleanability
- Environment
- Inspectability
- Manufacturability
- Reliability
- Testability

1.7.1 Design For Cleanability (DFC). All electronic hardware and equipment shall be designed to allow cleaning after fabrication and testing have been completed.

1.7.2 Design For Environment (DFE). All electronic hardware and equipment shall be designed to allow for minimal environmental impact when retired or disposed of (applies to ground support equipment). The use of environmental conscious materials and processes during the manufacturing cycle is strongly encouraged.

1.7.3 Design For Inspectability (DFI). All electronic hardware and equipment shall be designed to allow ease of being inspected, either visually where appropriate, or by appropriately designated testing procedures.

1.7.4 Design For Manufacturability (DFM). All electronic hardware and equipment shall be designed to allow ease of fabrication and assembly with minimal impact on manufacturting operations.

1.7.5 Design For Reliability (DFR). All electronic hardware and equipment shall be designed to withstand the environment defined by the applicable document and also all the rogors of physical handling during transportation, handling, and removal.

1.7.6 Design For Testability (DFT). All electronic hardware and equipment shall be designed to allow ease of being tested by appropriately designated testing procedures.

1.8 Fatigue Life

Electronic packaging systems shall be qualified by test to a fatigue life margin of three (3).

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1.9 General Thermal Requirements

Electronic packaging and cabling systems shall incorporate thermal design requirements into electronic circuit designs and subassemblies to assure the production of high-reliability, space-qualified electronics.

1.10 Structural Requirements

The components mounted on the printed wiring board shall be designed to withstand the stress, dynamics and shock requirements specified in the mission requirements.

1.11 General Handling, Storage, Packaging, Preservation, and Delivery Requirements

A suitable system shall be in-place to ensure the following:

- Handling incoming parts (e.g., piece parts, PWBs, etc.) to avoid damage
- Storage of work-in-progress (WIP) to avoid damage and to preserve the product from contamination, damage, and deterioration
- Protection and suitable preservation of the product during fabrication and assembly
- Packaging the product to avoid damage and contamination
- Delivery of the product to the customer in a satisfactory state and free of contamination, damage, and deterioration
- Proper documentation must be maintained.

1.12 Environmental Conditions

1.12.1 PWA Requirements. The printed-wiring board assembly, when packaged on a subchassis, in an enclosure, or spacecraft bay, shall meet all the environmental conditions specified by the mission requirements.

1.13 General Fabrication Requirements

1.13.1 Manufacturers. The following shall apply to all manufacturers producing articles for JPL.

1.13.1.1 Manufacturer Approval. All manufactured articles (e.g., PWBs, hybrids, harness assemblies, etc.) for JPL flight electronics shall be fabricated by a JPL-approved source.

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1.13.1.2 JPL Survey. JPL flight-approved manufacturers must have passed a survey performed by a JPL technical team.

1.13.1.3 Technical Team. The technical team shall consist of a minimum of an Electronic Packaging Engineer or an Electronic Process Engineer, and a Quality Assurance Representative.

1.13.1.4 Yearly Review. Qualified sources shall be reviewed on a yearly basis for continuation of their qualified status, unless they have provided quality products within the last quarter.

1.13.1.5 Key Personnel. Loss of key personnel vital to a reliable operation, transfer of operations to another facility which has not been approved, or deterioration of processes or controls beyond the point of immediate corrective action shall revoke qualification and require requalification and technical survey.

1.13.1.6 Requalification. Loss of qualified status for any reason shall require a requalification and a JPL technical survey team approval.

1.13.2 Facilities. All fabrication and assembly of electronic hardware and equipment shall be conducted in a facility suitable for the production of such hardware, including good housekeeping.

1.13.3 Requirements Meeting the Demands of ISO 9001. The following fabrication requirements shall be met for ISO 9001:

- Process Control
- Control of Inspection, Measuring and Test Equipment
- Inpection and Test Status
- Control of Nonconforming Product
- Corrective and Preventive Action

1.13.3.1 Process Control. A suitable system shall be in-place to ensure the following:

- Fabrication and assembly operations are maintained in a fashion consistent with the reduction of variation
- The cause(s) of deviation are pin-pointed when it occurs
- Appropriate steps are taken to bring the system back into control (corrective action)

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- Appropriate steps are taken to maintain the system once the cause(s) of deviation have been eliminated (preventive action)
- Proper documentation must be maintained.

1.13.3.2 Control of Inspection, Measuring and Test Equipment. A suitable system shall be in-place to ensure the following:

- Control of the various equipments to perform the conformance of product to specified requirements
- The proper maintenance and calibration of such equipment
- Determination of the measurement uncertainty and consistency with the required measurement capability
- Proper documentation must be maintained.

1.13.3.3 Inpection and Test Status. A suitable system shall be in-place to ensure the following:

- Determination of the exact status of a product in the product delivery system regarding its conformance or nonconformance to the specified requirements
- Proper documentation must be maintained.

1.13.3.4 Control of Nonconforming Product. A suitable system shall be in-place to ensure the following:

- Segregation of the nonconforming product from conforming product such that there is no confounding of the two
- Proper documentation must be maintained.

1.13.3.5 Corrective and Preventive Action. A suitable system shall be in-place to ensure the following:

- Maintenance of the product delivery system in proper working order
- Assurance that deviations are understood and eliminated in a systematic and rational fashion
- Proper documentation must be maintained.

1.13.4 Component Attachment. All component leads shall be mounted to their respective land patterns. The assembly drawing shall specify where this attachment consists of surface mount components and where it consists of plated through hole (PTH) mounting. The

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positioning of the leads or parts onto the land patterns may significantly impact the solder joint and must therefore be given careful consideration prior to mounting the leads to surface land patterns.

1.13.5 Electrostatic Discharge Requirements. Special care shall be taken in accordance with JPL D-1348 for handling active electronic components or assemblies to prevent damage from electrostatic discharge.

1.13.6 Prohibition on the Use of Tin. Tinplating, or tin coating, shall not be allowed on any item forming an electronic component of a printed wiring board assembly (PWBA). This includes, but is not limited to, such items as bare printed wiring boards (PWBs), component leads, screws, etc. However, it shall be allowed that the PWB manufacturer can use tin plate as an etch resist, provided that it is removed entirely prior to shipping the PWBs to JPL.

1.13.7 Marking Requirements. Completed assemblies shall be identified with part numbers, serial numbers, project identifiers and titles in accordance with project requirements and/or assembly drawings.

1.13.8 Outgassing. Flight-rated parts and material shall be tested in accordance with JPL TS507035.

1.13.8.1 Outgassing Limit. Outgassing shall be limited to a maximum total mass loss (TML) of 1.0% and maximum collected volatile condensable materials (CVCM) of 0.1%. For certain polymenic materials, if the water vapor regained (WVR) is also measured, the outgassing criteria shall be a maximum TML-WVR of 1.0% and maximum CVCM of 0.1%.

1.14 General Inspection Criteria Requirements

1.14.1 Visual Inspection. Each application of any polymeric shall be inspected with the unaided eye and microscope, at a maximum magnification of 12X with the exception of hybrids and microcircuits (see below). A record shall be kept of such inspection.

1.14.1.1 Visual Inspection of Hybrids and Microcircuits. Each application of any polymeric shall be inspected with the unaided eye and microscope, at a magnification greater than 30X. A record shall be kept of such inspection.

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Mechanical Requirements

1 DESIGN REQUIREMENTS

1.1 Environmental Conditions

1.1.1 Conformance. A spacecraft chassis and its electronic subassemblies shall be designed to meet the requirements of JPL D-8208 and the environmental conditions encountered by that mission.

1.1.2 Analysis. Analysis shall be provided with all analytical backups to indicate that the equipment will survive the electromechanical and thermal stresses of launch and the environment of space.

1.2 Structural Considerations

1.2.1 Margin of Safety. Electronic equipment shall be designed to ensure structural integrity by providing a yield margin of safety greater than 0.4 or an ultimate margin of safety greater than one (1).

1.2.2 Margin Calculation. The Margin of Safety (MS) shall be calculated as follows:

$$MS = SF - 1$$

where

$$SF_{yield} = \frac{\sigma_{yield}}{\sigma_c} \quad \textbf{or} \quad SF_{ultimate} = \frac{\sigma_{ult}}{\sigma_c}$$

MS: Margin of Safety
SF: Safety Factor
σ_{yield}: Yield stress of material
σ_{ult}: Ultimate stress of material
σ_c: Calculated stress

1.2.3 Stress and Dynamics Considerations. All chassis assemblies shall be designed to meet the specified stress and dynamics requirements of the mission.

1.2.3.1 Analysis Requirements. Analytical studies of the vibration and shock levels shall be provided to indicate that deflections and radius of curvature of the PWBs will not damage sensitive electronic components, crack solder joints or break the structural elements.

1.2.3.2 Analysis by Similarity. Analytical evaluation indicating similarity with comparable equipment that was analyzed, tested and successfully flown in a spacecraft shall be allowed to prove that the chassis assembly meets required stress and dynamic considerations.

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1.2.3.3 Subchassis Structural Performance Parameters. DSP subchassis shall be designed so that all axes of the fundamental resonant frequency and peak response, installed in the intended spacecraft application, fall within the conservative or adequate design region depicted in Figure 3.3-1.

1.2.3.4 Decoupling Factor. The fundamental resonance shall be decoupled from other structural resonances by a factor of at least 1.4.

1.2.4 Structural Fasteners. For structural fasteners, see JPL Specification ES504255.

1.3 Mechanical Design Layout

1.3.1 Accuracy.The layout drawing shall provide information regarding the chassis and all the electromechanical parts, assemblies, subassemblies, and mechanical hardware that comprise the chassis physical assembly to allow a tolerance analysis within a ±0.005 inch accuracy.

1.3.2 DSP Subchassis. Subchassis design shall consist of an aluminum honeycomb section with aluminum closeouts on the two long edges.

1.3.3 Versa Module European (VME) Subchassis.Versa Module European subchassis (thermal plates) shall be designed per the requirements of IEEE Std 1101.2-1992 and ANSI/IEEE Std. 1014, Section 7. The pitch can be varied to meet particular project requirements, but should contain provision for mounting in a commercial chassis.

1.3.4 Microwave and Radio-Frequency Chassis. Microwave and RF chassis shall be brazed, dip brazed, or machined from a block of aluminum, providing cavities to mount PWB assemblies or other electronic parts, and include a cover with provisions for installing gaskets for EMI and noise shielding, when required by the design.

1.3.5 Venting.

1.3.5.1 Direct Venting.Chassis which are not hermetically sealed shall be vented directly to the ambient of space.

1.3.5.2 Vent Area.The total area of vent opening shall allow the pressure in the enclosed volume to bleed down to 3×10^{-3} torr in 60 seconds or less, when the pressure, both residual air and outgassing, is reduced from ambient sea level to 10^{-5} torr in 6 seconds or less.

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Design Frequency Hz vs. Peak Response 'G's At The Electronic Part/Component Level

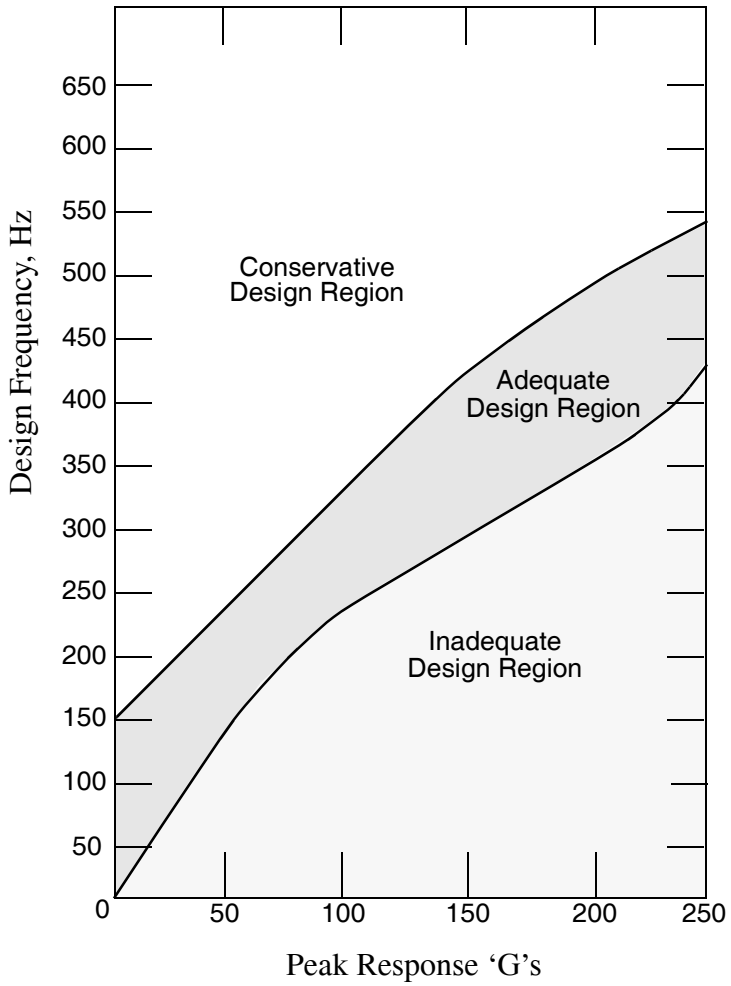

Figure 3.3-1 DSP Dynamic Design Criteria

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1.3.5.3 Hermetic Enclosures.Flight equipment installed in hermetically sealed chassis shall be exempt from the requirements of this section if the product of the measured leak rate and the mission time is such that the resultant pressure in the enclosure at the end of the mission is greater than 50 torr.

1.3.6 Thermal Considerations. Thermal analyses of heat dissipation, semiconductor junction temperature control and the elimination of hot spots, during the design phase shall be provided to assure proper thermal design as defined in JPL D-8208, Section 3.3.

1.3.7 Detail Chassis Design.The detail drawing shall include the parts and materials list, welding requirements, mechanical, electrical and other environmental tests, marking, electrostatic discharge protection and traceability requirements of the detailed designs of the chassis assembly and components.

1.4 Materials

1.4.1 Surface Finishes. Close fitting surfaces between electronic assemblies, subassemblies and associated hardware shall be protected against corrosion and galvanic action using materials listed in Table 3.3-1.

1.4.1.1 Secondary Electrical Path. To assure protection against corrosion, fasteners and grounding straps shall provide secondary electrical paths when anodic surfaces are employed.

1.4.1.2 Polished Surfaces. Aluminum parts requiring a polished surface shall be fabricated from aluminum alloys that do not require surface treatment for corrosion protection.

1.4.1.3 Surface Finishes. Finishes for electronic equipment hardware shall have a high emittance to promote heat transfer.

1.4.1.4 Special Surface Finishes.Spacecraft or instrument loads to be inserted into low earth orbit shall have a thermal control finish that is designed to withstand erosion from an atomic oxygen environment.

1.5 Fasteners

1.5.1 Fastener Selection. Fasteners for electronic equipment shall be from Table 3.3-2.

1.5.2 Threaded Fasteners. All threaded fasteners without inherent locking capability shall be spot bonded to prevent loosening.

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Table 3.3-1 Finishes

Description*	Thermal Control	Corrosion Resistant	Remarks
Enamel APA-2474	●		
Gold Electroplating	●		
Polished Surfaces	●		
Cat-A-Lac Gloss White Paint 443-1-500 /Catalyst-CA-33	●		
AKZO 463-3-8	●		
Cat-A-Lac Black	●		
Hincom/NS43G	●		
Aeroglaze Z307	●		
Chemglaze Z004	●		
Anodizing of Aluminum Parts Per MIL-A-8625, Type II, Class I		●	Nonconductive
Anodizing of Magnesium Parts		●	Dow 17 process Electrically nonconductive
Chemical conversion of Aluminum Parts, MIL-C-5541, Class III		●	Electrically conductive
Conversion Coating Magnesium Parts for Electrical Conductivity		●	Dow 7 Process
Touch-up Magnesium Parts for Electrical Conductivity		●	Dow 19 Process
Conversion Coating Aluminum Parts per MIL-C-5541, Class IA		●	Painted or not for corrosion protection

* Refer to JPL ST00009 for information regarding materials and application specifications.

1.5.2.1 Self Locking. Self-locking screws shall be identifiable by suitable head markings after the locking device is installed.

1.5.2.2 Thread Form. Thread form and class shall conform to MIL-S-7742.

1.5.2.3 Flat Washers. Flat washers shall be used under bolt heads and nuts to distribute stresses over a larger area as required by the structural analysis.

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1.5.2.4 Lock Washers. The use of lock washers of any type, such as star or split, shall be prohibited in all electronic equipment.

1.5.3 Screw in a Blind Hole. Fastener combinations for blind-hole applications shall be either a locking thin-wall insert with a Long-Lock CRES screw, a nonlocking Keensert witha pellet lock fastener, or a nonlocking pressnut with Nylock CRES screw.

1.5.4 Screw and Nut Combination. Fasteners shall be a CRES screw and a self-locking nut for all through-hole applications.

1.5.5 Screw Length. Screw length shall be chosen such that, when seated, the minimum thread engagement is the same as the diameter of the screw.

1.5.5.1 Nylock Screws. Nylock screws shall require full engagement of the locking device in the mating thread area.

1.5.5.2 Thread Exposure. Screw and nut combination shall require a minimum of 1-1/2 threads exposed above the nut.

1.5.6 Alternate Locking Methods. Spot bonding or an integral locking method shall be used on fasteners not bearing structural loads.

1.5.7 Latent Debris Control. Captive nuts or capped inserts shall be used on parts requiring threaded fasteners or where numerous screw removals take place for assembly or calibration.

1.5.8 Fasteners in Electrical Circuits. Fasteners within subassemblies as part of an active electrical circuit other than a ground point shall be prohibited.

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Table 3.3-2 Fastener Diameter and Pitch Combinations

Diameter	Pitch	Requirements
0-80	UNF	Use Federal Thread Standard Handbook H-28 for Threads Larger than 5/16-24 UNF
2-56	UNC	
4-40	UNC	
6-32	UNC	
8-32	UNC	
10-32	UNF	
1/4-28	UNF	
5/16-24	UNF	

1.5.9 Rivets. Rivets shall be selected from Table 3.3-3 for use in electronic equipment and hardware as long as structural and thermal integrity are not sacrificed.

1.5.10 Inserts.

1.5.10.1 Threaded Inserts. The center of the thin-wall, threaded insert shall be a minimum of 1.5 times the major diameter of the insert internal thread from the edge of the mounting material.

1.5.10.2 Nonlocking Inserts. The preparation of holes and dimensions for nonlocking inserts shall be per Table 3.3-4 and installed per JPL Spec FP513414.

1.5.10.3 Impact Installation. Inserts requiring impact installation shall be installed before the electronic components have been mounted and installed per JPL Spec FP513414.

1.5.10.4 Molded-in Inserts. Blind and through-hole, molded-in inserts for use in honeycomb panels shall be selected from Table 3.3-5 and installed using material from JPL D-8208, Section 3.17, per JPL Spec FP513414.

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Table 3.3-3 Rivet Maximum Projection Before Driving (Inches)

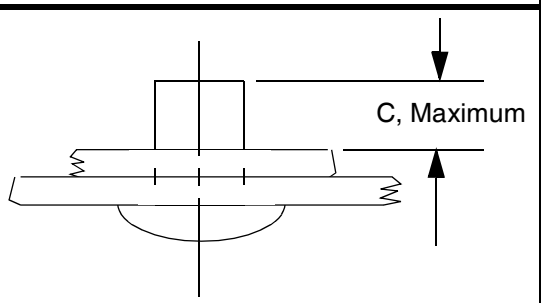
Rivet Diameter	Dimension C	
1/16	0.094	
3/32	0.141	
1/8	0.188	
5/32	0.234	
3/16	0.281	
1/4	0.375	
5/16	0.469	
3/8	0.562	

Table 3.3-4 Nonlocking Insert Hole Dimensions-ST11326 (Inches)

Internal Threads	External Threads	A Tap Drill Depth (Minimum)	B +.010/-.000
0-80	6-40	0.175	0.140
2-56	6-40	0.175	0.140
2-56	8-32	0.215	0.166
4-40	10-32	0.265	0.194
6-32	12-28	0.275	0.220
8-32	1/4-28*	0.325	0.255
* Modified minor diameter.			

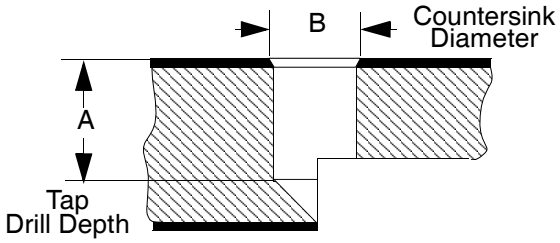


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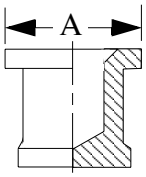
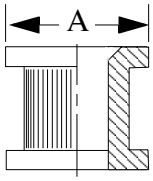
Table 3.3-5 Molded-in Inserts

C-Number*	A-Diameter Maximum	Installation Hole Size (Diameter)
04	0.310	0.311 - 0.317
06	0.310	0.311 - 0.317
08	0.341	0.342 - 0.348
3	0.390	0.392 - 0.398

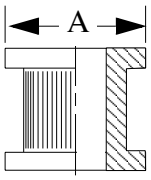
Blind Threaded
Series SL6061C*



Thru Threaded
Series SL6096C-XXX**



Clearance Hole
Series SL6089 A or C-XXX**



*Screws threaded into P/N SL6061 inserts are critical with respect to length.
** Indicates panel thickness

1.5.11 Blind Plate Nut. The blind-plate nut (BPN) detailed in Table 3.3-6 shall be used in DSP subchassis applications.

1.5.11.1 BPN Preparation. Preparation of holes and dimensions of BPNs shall conform to the requirements of Table 3.3-6.

1.6 Rectangular Connectors

1.6.1 Connector Savers. Front-mounted and back-mounted rectangular connector schemes utilizing connector savers shall be configured as shown in Figures 3.3-2 and 3.3-3, respectively.

1.6.1.1 Connector Saver Clips. Except on 50- and 78-pin connectors, clip number ST10043-1 shall be used for all front- and back-mount connector configurations; 50- and 78-pin connectors require clip number ST10043-2.

1.6.2 Front Mounted "D" Subminiature Connectors. Front-mounted "D" subminiature connectors as shown in Figure 3.3-4 and through-hole mounted as shown in Figure 3.3-5, shall be mounted using the connector cutout, mounting hole dimensions, and the assembly hardware shown in Figure 3.3-6.

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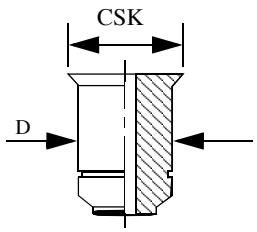
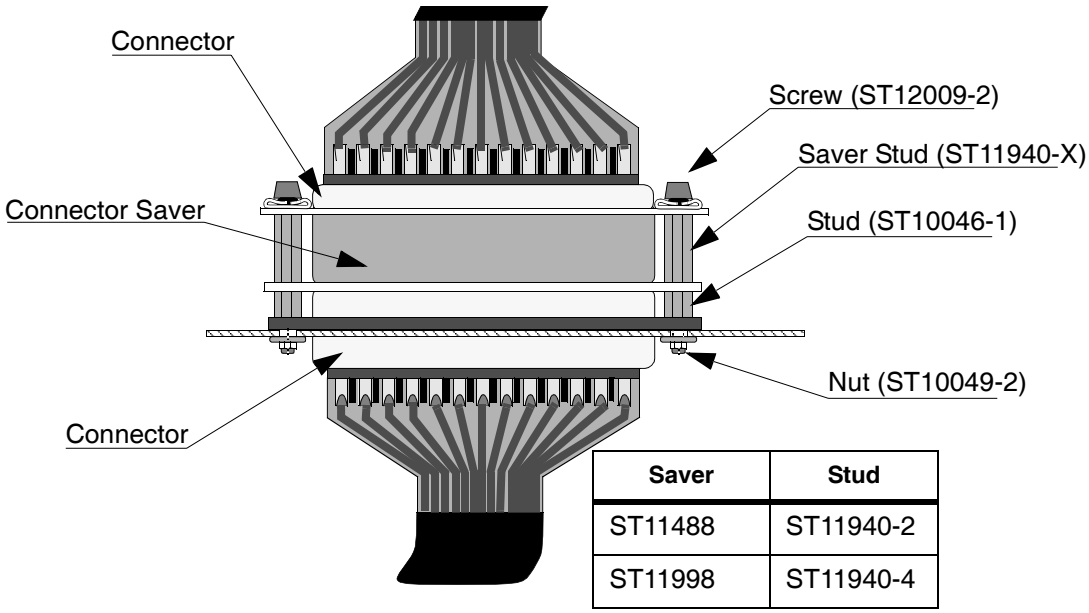
Table 3.3-6 BPN and Hole Dimensions

Part Number	Thread Size	D Diameter	CSK Diameter	Installation Hole Diameter
VN 1906BB0-1Y 	4-40	0.185-0.187	0.242-0.247	0.1875-0.1890



Saver	Stud
ST11488	ST11940-2
ST11998	ST11940-4

Figure 3.3-2 Front-Mounted Rectangular Connector with Connector Saver

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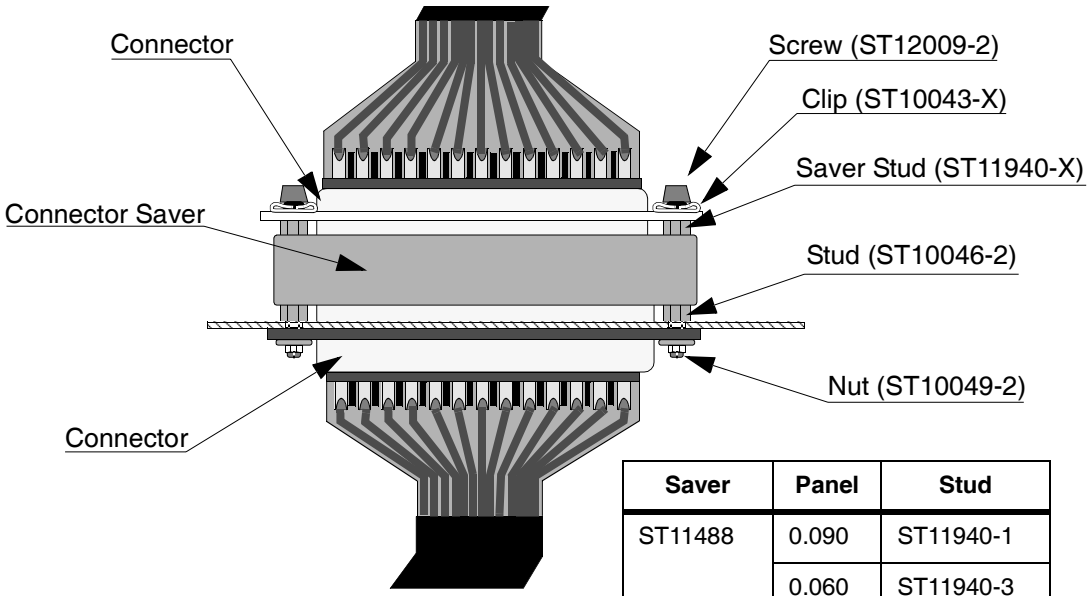

Saver	Panel	Stud
ST11488	0.090	ST11940-1
	0.060	ST11940-3
ST11998	0.060	ST11940-5

Figure 3.3-3 Back-Mounted Rectangular Connector with Connector Saver

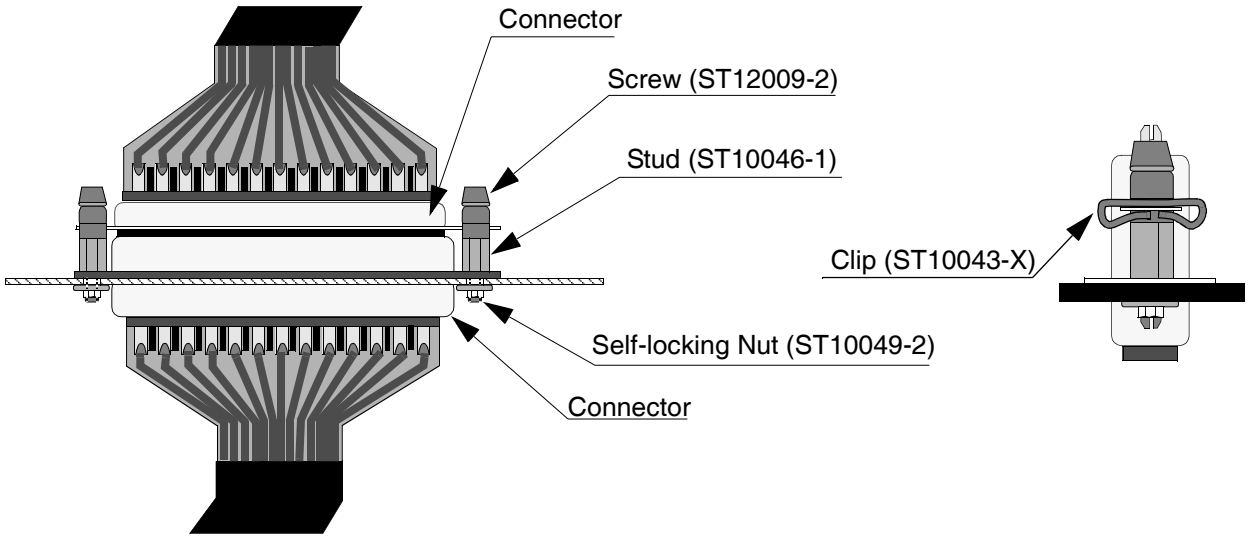

Figure 3.3-4 "D" Subminiature, Front-Mounted Connector

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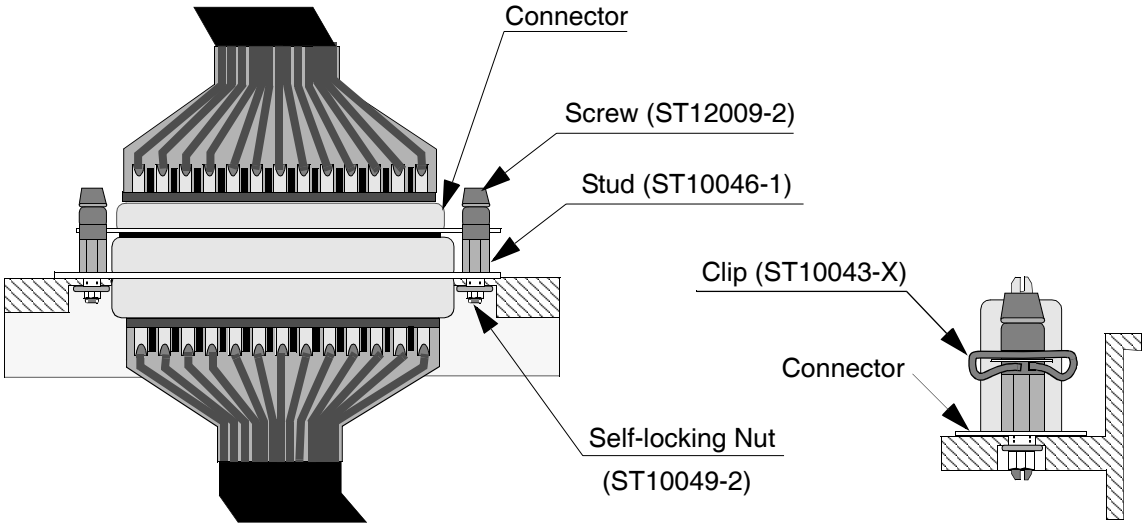

Figure 3.3-5 "D" Subminiature, Through-Hole Mounted Connector

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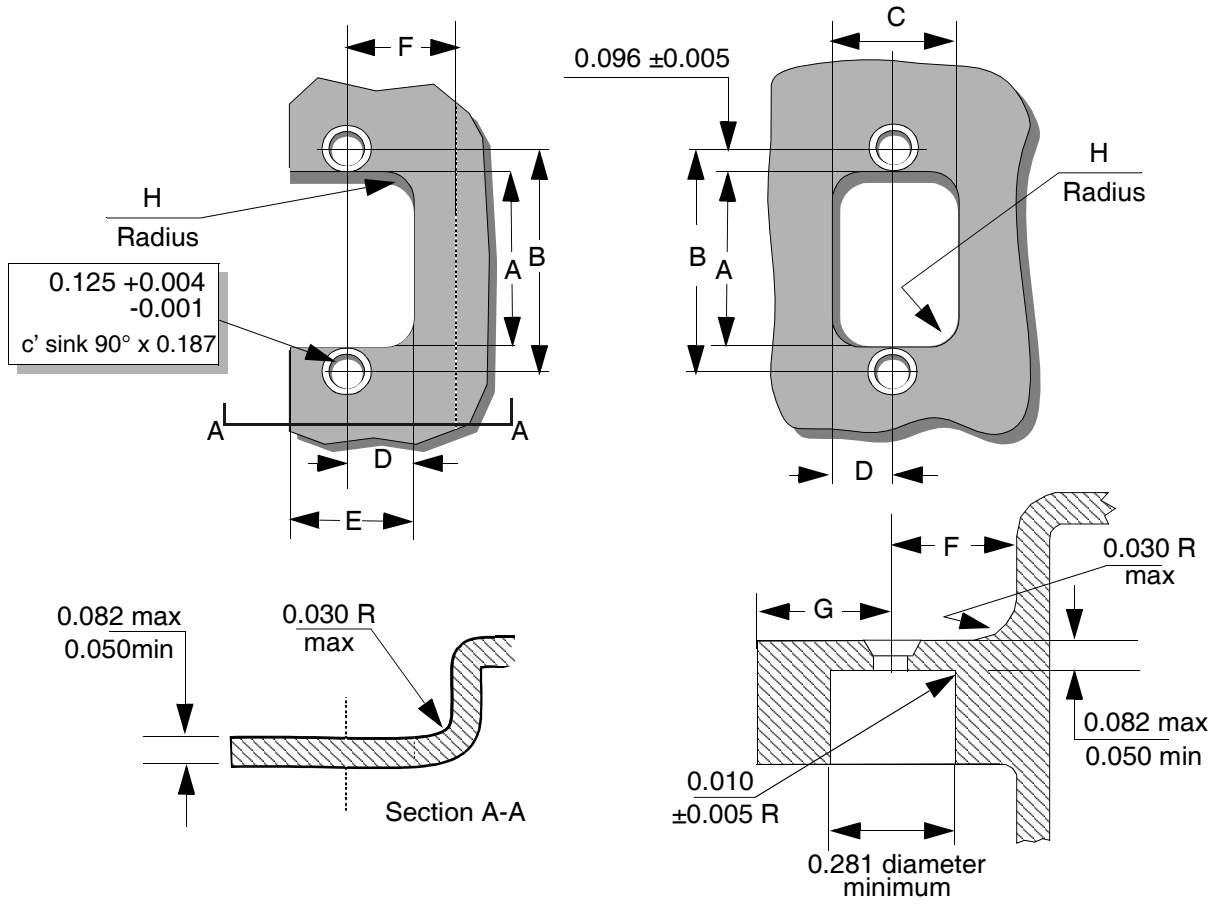

Front-Mount/Through-Hole Installation

Pins	A ±.005	B ±.005	C	D ±.005	E	F	G	H Radius
9	0.792	0.984	0.468	0.234	0.534	0.310	0.300	0.125
15	1.120	1.312	0.468	0.234	0.534	0.310	0.300	0.125
25	1.660	1.852	0.468	0.234	0.534	.3100	0.300	0.125
37	2.308	2.500	0.468	0.234	0.534	0.310	0.300	0.125
50/78	2.214	2.406	0.568	0.284	.6340	0.369	0.355	0.090

Figure 3.3-6 "D" Subminiature Connector Cutout and Mounting Hole

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1.6.3 Micro “D” Connectors. Micro “D” connectors, front mounted as shown in Figure 3.3-7 and through-hole mounted as shown in Figure 3.3-8, shall be mounted using the connector cutout and mounting hole dimensions with the assembly hardware shown in Figure 3.3-9.

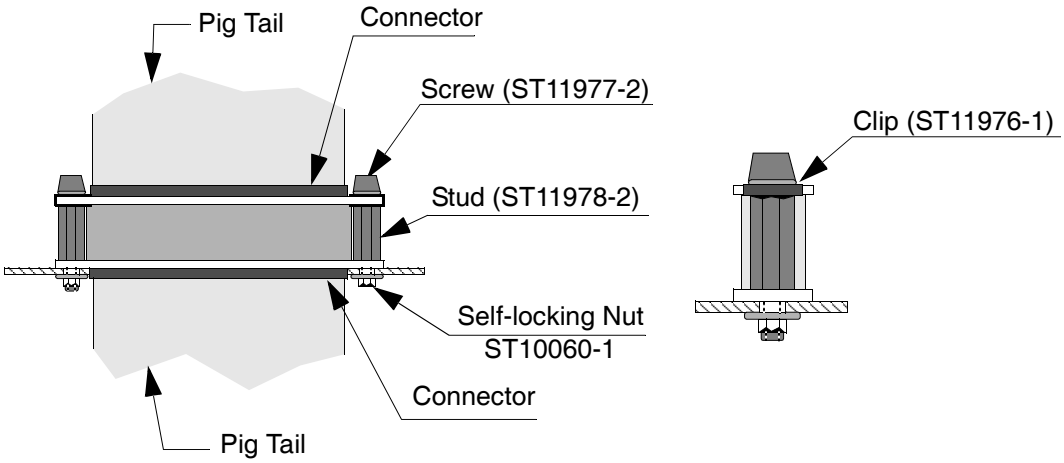

Figure 3.3-7 Micro “D” Front-Mounted Connector

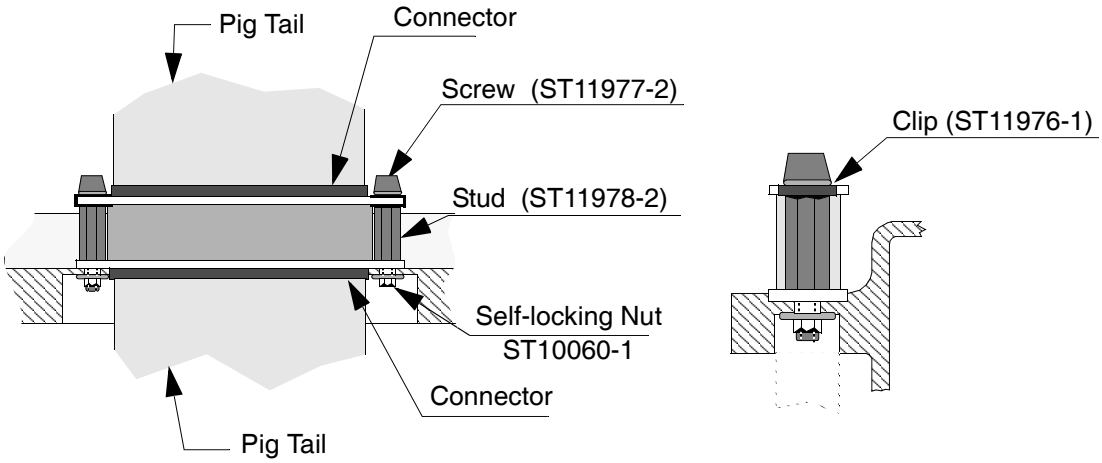

Figure 3.3-8 Micro “D” Through-Hole Mounted Connector

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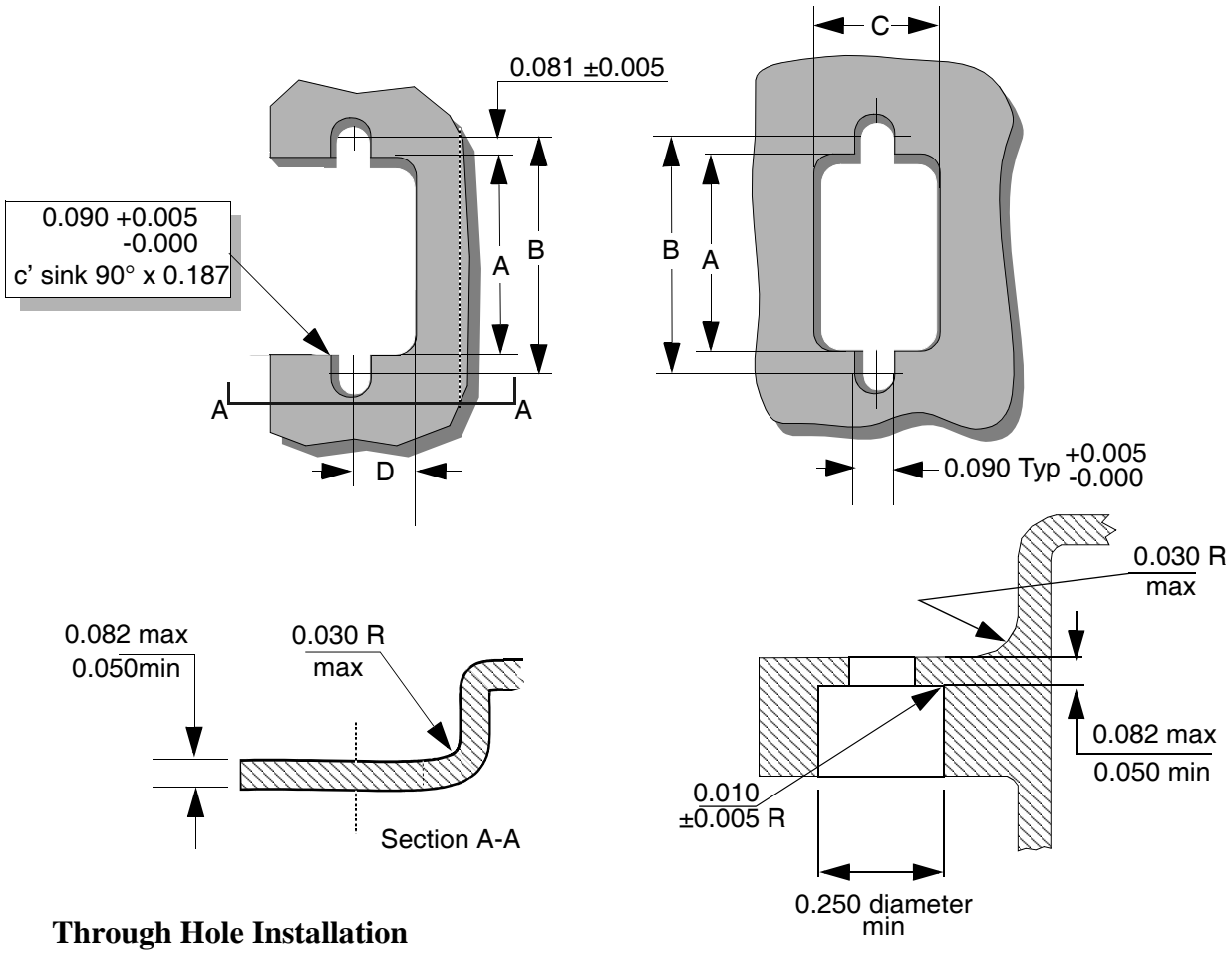

Through Hole Installation

Pins	A +0.004 -0.000	B +0.005 -0.000	C +0.010 -0.000	D +0.005 -0.000
9	0.408	0.570	0.308	0.154
15	0.558	0.720	0.308	0.154
21	0.708	0.870	0.308	0.154
25	0.808	0.970	0.308	0.154
31	0.958	1.120	0.308	0.154
37	1.108	1.270	0.308	0.154
51	1.058	1.220	0.348	0.174

Figure 3.3-9 Micro "D" Connector Cutout and Mounting Holes

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1.6.4 Back Mounted "D" Subminiature Connectors. D" Subminiature connectors, back mounted as shown in Figure 3.3-10 shall be mounted using the connector cutout and mounting hole dimensions and the assembly hardware shown in Figure 3.3-11.

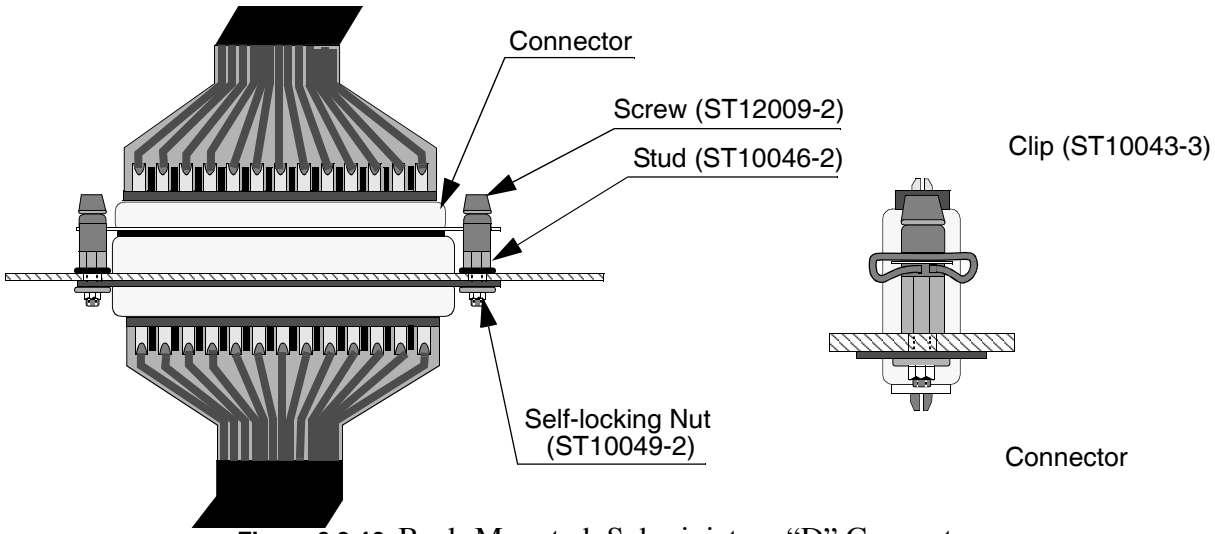

Figure 3.3-10 Back-Mounted, Subminiature "D" Connector

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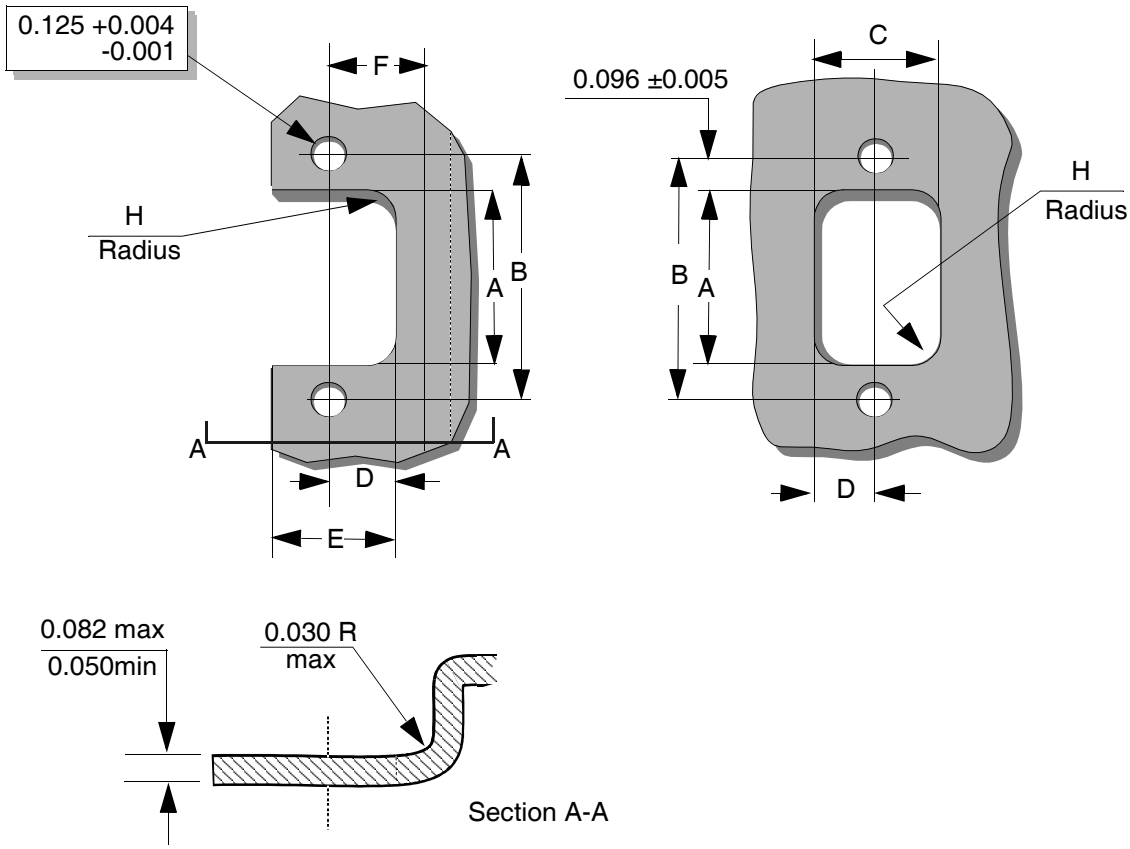

Through-Hole Installation

Pins	A ±.005	B ±.005	C	D ±.005	E	F	H Radius
9	0.792	0.984	0.468	0.234	0.534	0.310	0.125
15	1.120	1.312	0.468	0.234	0.534	0.310	0.125
25	1.660	1.852	0.468	0.234	0.534	0.310	0.125
37	2.308	2.500	0.468	0.234	0.534	0.310	0.125
50	2.214	2.406	0.568	0.284	0.634	0.369	0.090

Figure 3.3-11 "D" Subminiature Back-Mount Connectors

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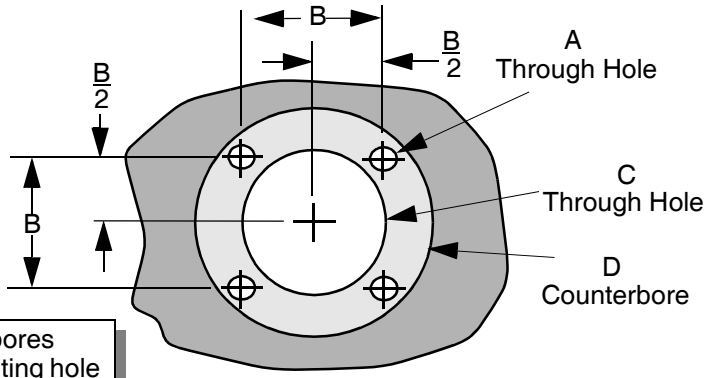
1.7 Circular Connectors

1.7.1 Wall Mounted. Circular connectors, wall mounted as shown in Figures 3.3-13 and 3.3-14 shall be mounted using the connector cutout and mounting hole dimensions with the assembly hardware shown in Table 3.3-7 and Figure 3.3-12.

Table 3.3-7 Circular Connector Mounting Hole Dimensions

Shell Size	A Diameter +0.004/-0.001	B ±0.005	B/2 ±0.010	C Diameter +0.005/-0.001	D Diameter ±0.010	Hardware Mounting
8	0.125	0.594	0.297	0.562	1.125	#4 Pan-head Screw
10	0.125	0.719	0.360	0.688	1.312	"
12	0.125	0.812	0.406	0.875	1.438	"
14	0.125	0.906	0.453	1.000	1.562	"
16	0.125	0.969	0.484	1.125	1.656	"
18	0.125	1.062	0.531	1.250	1.781	"
20	0.125	1.156	0.578	1.375	1.906	"
22	0.125	1.250	0.625	1.500	2.156	"
24	0.149	1.378	0.687	1.625	2.225	#6 Pan-head Screw



NOTE: Individual counterbores may be used around mounting hole and screw hole in lieu of the counterbore pattern shown above.

(Used in conjunction with Table 3.3-7.)

Figure 3.3-12 Circular Connector Cutout

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Table 3.3-8 Mounting Surface Thickness (See Figure 3.3-13.)

Shell Size	Standard Density Solder Type	Standard Density Crimp Type	High Density Crimp Type
8	0.040	0.040	0.147
10	0.040	0.040	0.152
12	0.040	0.040	0.152
14	0.040	0.040	0.152
16	0.040	0.040	0.152
18	0.040	0.040	0.152
20	0.060	0.187	0.179
22	0.060	0.187	0.179
24	0.060	0.187	0.179

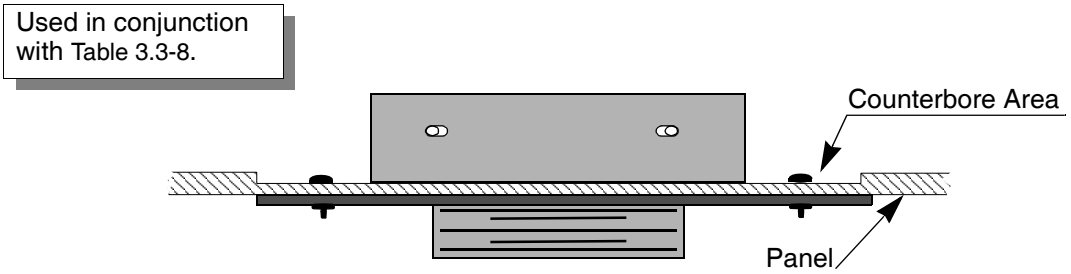

Figure 3.3-13 Thick Panel Counterbores

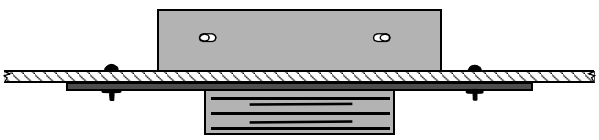

Figure 3.3-14 Typical Circular Connector Installation

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1.8 Other Connectors

1.8.1 Connector Mounting.Other connectors shall be mounted using the connector cutout and the assembly hardware specified by the connector manufacturer.

1.9 Fasteners for Other Connectors

1.9.1 Integral Locking. The fasteners or coupling nuts for these connectors shall be secured by an integral locking device or be spot bonded per JPL D-8208, Section 3.17.

1.10 Interconnections Cabling

1.10.1 Cabling Conformance. Cabling interconnection shall comply with JPL D-8208, Section 3.12.

1.11 Radiation Shielding

1.11.1 Shielding Conformance. Radiation shielding shall comply with JPL D-8208, Section 3.14.

1.12 Chassis Marking

The chassis shall be identified with part number, serial number, and project identifier in accordance with Table 3.3-9.

2 FABRICATION REQUIREMENTS

2.1 Documentation

2.1.1 Completed Package.A deliverable documentation package shall be maintained for each deliverable item that includes an approved fabrication instruction, inspection data, deviation reports, and all MRB evaluations.

2.1.2 Manufacturing and Inspection Records. All manufacturing and inspection checks shall be recorded on shop travelers accompanying each piece of hardware to keep an accurate history of each deliverable.

2.1.3 Materials Certification. Manufacturers of the all materials shall supply certification of conformance to the required and applicable specifications.

2.1.4 Traceability. Traceability shall be maintained throughout the process from receiving or source inspection to final tests.

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2.2 Assemblies Intrawiring

2.2.1 Cabling Compliance. All cabling and wiring shall be assembled as specified in JPL D-8208, Section 3.12.

Table 3.3-9 Marking Processes for Material and Equipment

Material	Surface Processing	Bag and Tag	Rubber Stamping	Silk Screening	Stenciling	Printing	Engraving	Vibration Etching	Photo-Etched Copper	Electrolytic Etching	Name Plates	Vinyl Labels	Metal Labels	Metal Stamping	Forging, Casting, & Molding	Polyester-Base Labels	Hot Stamping	Polyimide Film Labels
Aluminum and Aluminum Alloys	Before	●					●	●		●				●	●			
	After	●	●	●	●	●												●
Magnesium and Magnesium Alloys	Before	●					●	●		●				●	●			
	After	●	●	●	●	●												●
Stainless Steel	Before	●					●	●		●				●	●			
	After	●	●	●	●	●												●
Titanium and Titanium Alloys	Before	●					●	●		●				●	●			
	After	●	●	●	●	●												●
Beryllium	N/A	●	●	●	●	●	●	●		●				●	●			
Copper and Copper Alloys	Before	●					●	●		●								
	After	●	●	●	●	●												●
Metallic Materials	N/A	●	●	●	●	●	●	●		●				●	●			
Printed Wiring Boards	N/A	●	●	●	●	●			●									●
Connectors	N/A	●	●	●	●	●	●										●	●
Electronic Components and Modules	N/A	●	●	●	●	●										●		●
Plastic Parts	N/A	●	●	●	●	●									●		●	●
Ground Equipment	N/A	●	●	●	●	●	●	●		●	●	●	●	●	●	●	●	●
Shipping and Handling Equipment	N/A	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●		

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2.3 Threaded Fastener Torque Requirements

2.3.1 Torque Compliance. All non-structural threaded fasteners shall be tightened to the approved torque requirements provided in the following paragraphs.

2.3.2 Locking Method. Spot bonding shall not be used for fasteners bearing structural loads.

2.3.3 Thread Engagement. A minimum of one (1) nominal diameter engagement shall be required for all applications.

2.3.4 Torque Values. The torque values are specified for the material combinations shown, and shall apply to self-locking and nonlocking threaded fasteners.

2.3.4.1 Torque Limits. Electronic packaging torque values shall be as shown in Table 3.3-10 and Table 3.3-11 except for self-locking fasteners.

2.3.4.2 Self-locking Fasteners. The value of running torque upon installation shall be added to the applicable torque value from Table 3.3-10 and Table 3.3-11 to obtain the final installation torque.

2.3.4.3 Self-locking Fastener Replacement Criteria. The running torque value of each screw shall conform to the minimum values listed in Table 3.3-12 or be replaced with a new screw.

2.3.4.4 Final Installation. The fastening procedure for final installation of fastener systems to specified torque values shall be accomplished by installing the fastener to a torque value within the specified tolerances.

2.3.4.5 Exceeding Torque Limits. If a torque value greater than +10% of the specified value is inadvertently applied, the fastener shall be completely loosened. The fastener shall be considered for replacement or reinstalled to the proper value at the discretion of the Cognizant Engineer.

2.3.4.6 Fracture-Critical Fasteners. No fracture-critical fasteners shall be reinstalled if a torque value greater than specified is inadvertently applied during installation.

2.3.4.7 Other Torque Values. To obtain torque values for other material combinations not contained in this document, contact the Fastener Specialist in Section 352.

2.3.4.8 Bolt and Nut Combinations. During the installation of bolt and nut combinations, torque shall be applied to the nut whenever possible.

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Table 3.3-10 A286 (Ftu >160 ksi) Fastener Torque Limits**

Torque Application	Size	2	4	6
	Threads	**56**	**40**	**32**
	Lubrication	**Torque +1 -10% (inch-pounds)**		
Tapped hole in Ti, Steel, Invar, Al 7075, Insert in Al or Magnesium	No Lube	5	11	20
	Thread	4	9	16
	Thread+ Head*	3	6	10
Tapped Hole in Al 2024 and Al 6061	No Lube	5	11	20
	Thread	4	9	16
	Thread + Head*	3	6	10

*Applies to lubricated nuts when the torque is applied to the nut.
** For #8 and #10, refer to JPL specification ES504255, Structural Fasteners.

Table 3.3-11 300 CRES (Ftu >80 ksi) Fastener Torque Limits**

Torque Application	Size	2	4	6
	Threads	**56**	**40**	**32**
	Lubrication	**Torque +1 -10% (inch-pounds)**		
Tapped hole in Ti, Steel, Invar, Al 7075, Insert in Al or Magnesium	No Lube	3	5	10
	Thread	2	4	8
	Thread+ Head*	1.4	3	5

*Applies to lubricated nuts when the torque is applied to the nut.
** For #8 and #10, refer to JPL specification ES504255, Structural Fasteners.

Table 3.3-12 Fastener Minimum Running Torques

Screw Size	Minimum Running Torque (inch-pounds)
2-56	0.5
4-40	1.0
6-32	1.5
8-32	2.0

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2.3.4.9 Through-hole Application. Through-hole applications shall use capped inserts, if possible, or capped nuts to trap any debris generated from the installation and removal of the externally threaded fastener.

2.3.4.10 Capped Inserts, Nuts, or Blind Holes. The depth of the capped insert, nut, or blind hole shall be measured prior to installation of the screw to verify a minimum of 0.050 inch clearance of screw to cap or bottom of hole.

2.3.4.11 Lubrication. No lubrication shall be applied to threaded fasteners at the time of installation, except for fasteners supplied with lubricant, as specified on their applicable standard drawing.

2.3.4.12 Minimum Running Torque. For values not provided in these tables, a minimum running torque of 10% of the required torque value or 1/2 inch-pound, whichever is less, shall exist before addition to required torque.

2.3.4.13 Marking Self-Locking Screws. Six dots on the head of the screw and/or an “L” in the part number shall identify self-locking screws.

2.3.4.14 SMA Connectors. Mating SMA connectors shall be torqued to 7-10 in.lbs. and spot bonded per JPL D-8208, Section 3.17.

2.3.4.15 TNC Connectors. Mating TNC connectors shall be torqued to 12-15 in.lbs. and spot bonded per JPL D-8208, Section 3.17.

2.3.5 Exposed Threads.

2.3.5.1 Screw and Nut Combinations. Screw and nut combinations, torqued to the requirements of this specification, shall have a minimum of $1\ ^{1}/_{2}$ screw threads extending through the nut.

2.3.5.2 Flush. Certain electronic packaging applications shall permit the screw threads to be a minimum of flush with the top of the nut.

2.3.5.3 Spot Bonding. If the screw and nut are to be spot bonded, the $1\ ^{1}/_{2}$ screw threads minimum shall apply.

2.4 Microwave and RF Chassis Assembly

2.4.1 Internal Cavities. PWBs, electronic components, interconnecting cables and connectors shall be inserted into internal cavities of the chassis to form the assemblies.

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2.5 Rectangular Connector Mounting

2.5.1 Front-Mounted and Through-Hole "D" Subminiature Connectors. Front-mounted and through-hole connectors shall be oriented in accordance with the applicable drawing(s) and secured per Table 3.3-13.

2.5.2 Front-Mounted and Through-Hole Micro-D Connectors. Front-mounted and through-hole Micro-D connectors shall be oriented in accordance with the applicable drawing(s) and secured per Table 3.3-14.

2.5.3 Back-Mounted "D" Subminiature Connectors. Back-mounted "D" subminiature connectors shall be oriented in accordance with the applicable drawing(s) and secured per Table 3.3-13.

2.5.4 Micro-D Connectors. Micro-D connectors shall be oriented in accordance with the applicable drawing(s) and secured per Table 3.3-14.

Table 3.3-13 "D" Subminiature Connector Installation Procedures

Installation Method	Parts Required	Torque Requirements
Stud bearing surface on chassis or mounting plate (back-mount)	ST10046-2 Stud (0.188 head ht) with ST10049-2	Apply 8-9 in-lb torque to stud while restraining nut.*
Stud bearing surface on connector flange (front-mount)	ST10046-1 Stud (0.250 head ht.) with ST10049-2	Apply 8-9 in-lb torque to stud while restraining nut.*
Mating of connector	ST10043 locking clip and ST10044 screw Assembly	Apply 3.5 to 4.5 in-lb torque to screw.
*Do NOT add running torque to these values.		

Table 3.3-14 Micro-D Connectors

Application	Part No.	Torque
Nut (#2 small pattern nut) Stud Clip Assembly	ST10060-1 ST11978-2 ST11976-1	Apply 3.5 to 4.0 in-lb torque (1.5 in-lb running torque plus 2.0 to 2.5 seating torque)
Screw	ST11977-2	Apply 2.0 to 2.5 in-lb torque (0.5 in-lb running torque plus 1.5 to 2.0 in-lb seating torque)

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2.6 Circular Connector Mounting

2.6.1 Hermetic Connector Jam Nut Torque. ST10078-XX and ST11376-XX hermetic connectors shall be mounted using the torque values listed in Table 3.3-15.

2.6.2 Connector Backshell Torque. Connector backshells and backshell hardware shall be torqued per the values provided in Table 3.3-16.

2.6.3 Twinax Connectors.Twinax connectors shall be torqued per the values provided in Table 3.3-17.

2.6.4 RF Connectors.RF connectors shall be torqued per the values provided in Table 3.3-18.

2.7 Radiation Shields

2.7.1 Mounting Compliance. Radiation shields shall be installed per JPL D-8208, Section 3.14.

2.8 Marking

2.8.1 Marking Compliance. The chassis shall be marked with the part number or identifier using the materials and processes listed in Table 3.3-9.

2.9 Self-clinching Studs, Blind Nuts, and Nylon Fasteners

2.9.1 Aluminum Shear Plates. Hardware mounted to self-clinching studs installed in aluminum shear plates shall use ST10049 self-locking nuts torqued per Table 3.3-19.

2.9.2 Blind Nuts. A286 fasteners into blind nut BN372-440-1 in aluminum shall be torqued at 12 inch-pounds. For non-A286 fasteners, torque to 6 inch-pounds.

2.9.3 Nylon Fasteners. Nylon fasteners shall be torqued per Table 3.3-20 when mated with a nylon nut.

2.10 Transformers and Inductors

2.10.1 Bonded Transformers and Inductors. Re-torquing after curing of bonding material shall not be required.

2.10.2 Installation Torque Values. The torque values given in Table 3.3-21 shall pertain to installation only.

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2.10.3 Metal Fastener Tubes. Inductors using metal fastener tubes shall be controlled by Table 3.3-11.

Table 3.3-15 Connector Jam Nut Connectors

Thread Size	Torque Values			
	Inch Pounds		Foot Pounds	
	Minimum	Maximum	Minimum	Maximum
0.5625	80	85		
0.6875	100	110	8	9
0.8750	140	150	11	12
1.0000	160	170	13	14
1.1250	210	230	18	19
1.2500	260	280	21	23
1.3750	300	320	24	25
1.5000	325	350	28	30
1.6250	350	375	28	30

Table 3.3-16 Connector Backshell Torque Values

Thread Size	Torque Values			
	Inch Pounds		Foot Pounds	
	Minimum	Maximum	Minimum	Maximum
0.3125	20	26		
0.3750	20	26		
0.4375	20	26		
0.5000	20	26		
0.5625	25	32		
0.6250	25	32		
0.6875	30	36		
0.7500	34	40		
0.8125	40	46		

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Table 3.3-16 Connector Backshell Torque Values (Continued)

Thread Size	Torque Values			
	Inch Pounds		Foot Pounds	
	Minimum	Maximum	Minimum	Maximum
0.8750	46	50		
0.9375	50	55		
1.0000	55	60		
1.0625	60	65		
1.1250	70	75		
1.1875	75	80		
1.2500	80	85		
1.3125	85	90		
1.3750	90	95		
1.4375	100	110	8	9
1.5000	100	110	8	9
1.6250	110	120	9	10
1.7500	120	130	10	11
1.8750	140	150	11	12
2.0000	150	160	12	13
2.0625	160	170	13	14
2.1250	170	180	14	15
2.2500	170	180	14	15
2.3125	180	190	15	16
2.3750	190	200	16	17
2.5000	200	210	17	18
2.5250	210	220	18	19
2.7500	220	230	18	19
2.8750	230	240	19	20
3.0000	240	250	20	21

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Table 3.3-17 Twinax Connector Recommended Torque Values

Connector Type	Torque (inch-pounds)
Plug coupling nut (ST10197-1)	8.0 to 10.0
Jack jam nut (ST10196-1)	25.0 to 30.0

1. Notes:
1. 1. Mounting hole for Jack shall be prepared as specified in ST10196.
1. 2. It is not recommended to use the O-ring gasket on Jack.

Table 3.3-18 RF Connector Recommended Torque Values

Connector Type	Torque (inch-pounds)
SMA Plug	7.0 to 10.0
Jam Nut - SMA Blkhd Feedthrough	12.0 to 15.0
TNC Plug	12.0 to 15.0
Jam Nut - TNC Blkhd Feedthrough	12.0 to 15.0

Table 3.3-19 Self-clinching Studs

Basic Part Number	Size	4	6	8
	Threads	40	32	32
	Mating Nut	Torque +0 -10% (inch-pounds)		
FHS-440	ST10049-2	6		
FHS-632	ST10049-3		12	
FHS-832	ST10049-4			18

*Do not add running torque to these values.

Table 3.3-20 Nylon Screw and Nut Torque Values

Screw Size	Torque Value
4-40	8 +0 -1 inch-ounce
6-32	16 +0 -1 inch-ounce
8-32	27 +0 -1 inch-ounce

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Table 3.3-21 Transformer and Inductor Torque Values

Screw	Fastener System	Torque Values (inch-pounds)
4-40	Screw and ST10049 Nut (Integral Washer)	4
4-40	Screw and Hex Nut (Spot Bond as Locking Feature)	6
6-32	Screw and ST10049 Nut (Integral Washer)	10
6-32	Screw and Hex Nut (Spot Bond as Locking Feature)	12

2.11 Cast Module Inserts

2.11.1 Torque Values. Torque values for cast module inserts shall conform to Table 3.3-22.

2.11.2 Bonded Cast Modules. Re-torquing after curing of bonding material shall not be required.

2.12 Cable Clamps

2.12.1 Metal Cable Clamps. The torque values from Table 3.3-11 shall be used for metal cable clamps.

2.12.2 Nylon Cable Clamps. An applicable metal “D” washer and the torque values from Table 3.3-11 shall be used for plastic (nylon) clamps.

2.13 Transistors and Diodes

2.13.1 Stud Mounted. Stud mounted transistors and diodes shall be torqued per Table 3.3-23.

2.13.2 Other Stud Mounted Components. Stud mounted electronic components with thread sizes not listed or with fragile components shall be torqued per the manufacturer’s recommendations.

2.14 Aluminum Honeycomb Inserts

2.14.1 Insert Selection. Fasteners mounting electronic hardware into molded-in inserts in aluminum honeycomb structure (DSP subchassis) shall be torqued to the requirements of Table 3.3-24.

2.14.2 Hole Tolerance.The holes for inserts shall be machined into the honeycomb sandwich in accordance with the applicable engineering drawing and Table 3.3-24.

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Table 3.3-22 Cast Module Insert Torque Values

Screw	Torque Value (inch-pounds)	Tolerance (inch-pounds)
2-56	3	+0 -1
4-40	7	+0 -1
6-32	12	+0 -1

Table 3.3-23 Stud Mounted Transistor and Diode Torque Values

Stud Size	Torque (inch-pounds)
10-32	11 +0 - 10%
1/4-28	23 +0 - 10%
5/16-24	36 +0 - 10%

Table 3.3-24 Inserts Molded in Aluminum Honeycomb

Basic Part Number	Material	Configuration	Mating Screw	Size/Number of Threads* (inch-pounds +0 -10%)			
				4-40	6-32	8-32	10-32
SL6061	CRES	Blind Thread	DS132(L)	12	18	35	50
SL6089	Aluminum	Through Hole	DS132	11	17	30	45
SL6096	CRES	Threaded Through Hole	DS132(L)	12	18	35	50
*Do NOT add running torque to these values.							

2.14.2.1 Hole Roundness. Holes shall be round to within 0.002 inch of true position.

2.14.3 Blind Plate Nuts. Shear plate screws (ST10073) mounting into blind plate nuts in aluminum DSP subchassis (VN1906BB0-1Y) closeouts shall be torqued at 12 inch-pounds +0/-10%.

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3 QUALITY ASSURANCE

3.1 Verification Methods

The following methods shall be used to verify the requirements of this document.

3.1.1 Inspection. Verification by inspection is accomplished by comparing the requirements specified in Section 2 with the appropriate characteristics of an item. Inspection includes evaluation of mechanical functionality and accuracy as described in corroborating documentation.

3.1.1.1 Qualification. All threaded fasteners torqued to the requirements of this specification shall be 100% inspected for proper torque prior to TA and FA testing and final assembly.

3.1.1.2 Running Torque. Running torque shall be verified for all fasteners.

3.1.1.3 Inspection. Screw and nut combinations shall be inspected for conformance to the requirements of paragraph 2.3.4.13 herein.

3.1.2 Test. Verification by testing is accomplished by subjecting an item to a set of conditions under the control of approved plans, procedures, and test equipment which will provide a measurable response. The results of the test are compared with the expected results as specified in Section 2.

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Thermal Requirements

1 DESIGN REQUIREMENTS

1.1 Environmental Conditions

1.1.1 Spacecraft Chassis. Spacecraft chassis and its electronic subassemblies shall be designed to meet the environmental conditions as defined by mission parameters.

1.1.2 Analysis and Certification. A thermal analysis and certification testing shall be performed to demonstrate that the equipment will survive the electromechanical and thermal stresses of ground test, launch, and the environment of space as defined by the mission parameters.

1.1.2.1 Thermal Analysis Review. An independent review of the thermal analysis shall be completed by a reliability engineer (or person with sufficient training to function as reliability engineer) prior to assembly to verify that the board and components will survive the thermal stresses of launch and the environment of space.

1.1.3 Junction Temperature Reduction. Special emphasis shall be put on reducing the junction temperatures of semiconductors to levels below the maximums specified in the project requirement documents.

1.2 Packaging/Layout Design

1.2.1 Component Positioning. The packaging design shall optimally locate or position electronic components on the boards to meet the thermal requirements, as well as mechanical, structural, EMI/RFI, and electrical requirements.

1.2.2 Subassembly Fasteners. Each subassembly shall be fastened to the chassis with a sufficient number of fasteners to satisfy both thermal and structural requirements.

1.2.3 Thermally Conductive Mounting Methods. To maintain their derated temperature range as determined by the thermal analysis, electronic components that require a higher thermal conductance or a shortened or augmented thermal path to the metal chassis shall be mounted with thermally conductive material per JPL D-8208, Section 3.14.

1.2.3.1 Thermally Conductive Bonding Methods. Electronic components requiring thermally conductive bonding shall meet the requirements of JPL D-8208, Section 3.17.

1.2.3.2 Thermal Window. A thermal window in the PWB shall be provided for axial leaded components, radial-leaded components, and TO-type metal can devices requiring heat dissipation as determined by the thermal analysis.

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1.2.4 Thermal Cooling Straps and Braids.Straps or braids shall be used for dual inlines or other packaged types to provide cooling where no polymeric or shim is allowed under the part, as illustrated in Figure 3.4-1.

1.2.4.1 Strap/Braid Analysis. All thermal straps shall be analyzed for heat conduction properties and resistance to vibration fatigue failure to meet the mission requirements.

1.2.5 High-Power Parts.

1.2.5.1 Analog Parts. The designer shall avoid the selection or use of high-power analog devices unless specified by the project documents.

1.2.5.2 Screw or Stud Mount Devices. The designer shall select screw-mount or stud-mount devices whenever possible to meet both thermal and structural requirements.

1.2.5.3 Axial Lead Component. High-power, axial-lead components shall be located in the coolest section of the board with lead geometries selected to meet all thermal and structural requirements.

1.3 Thermal Performance Parameters

It is recommended that high-power parts be selected from items that list low Θjc parameters, or divided into segments to allow selection of two or more lower power parts to handle the load when a low Θjc part is not available.

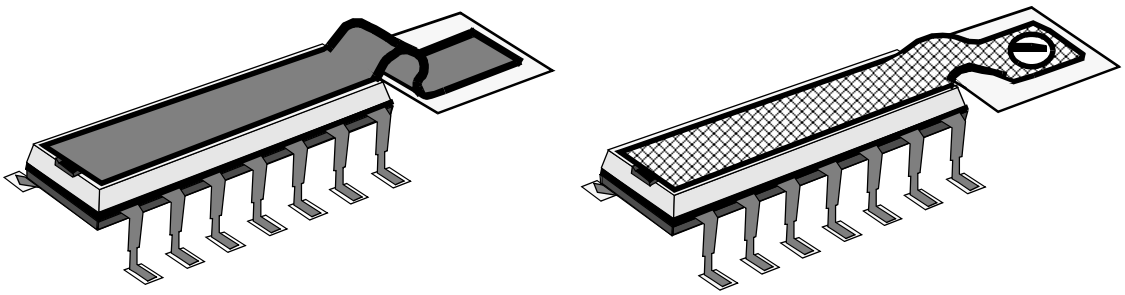

Figure 3.4-1 Thermal Cooling Strap or Braid

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1.3.1 Dual Shear Plate. The thermal design for the electronic boards mounted onto subchassis shall provide the heat flow path toward the outboard shear plate of the bay.

1.3.1.1 Heat Flow. The heat flow path shall be a direct path to the outer shear plate as shown in Figure 3.4-2.

1.4 Materials

1.4.1 Material Selection. Materials selected for their special thermal properties shall take into consideration all aspects of electronics packaging.

1.4.2 Surface Finishes. Surface finish shall be selected to provide low resistance thermal paths through interfaces.

1.4.2.1 Heat Transfer Surfaces. Finishes selected for electronic equipment shall provide adequate surfaces to meet heat transfer requirements.

1.4.2.2 Thermal Control Finishes. The thermal control finishes shall be one of the following:

a. Anodizing
b. Chromate Finish
c. Hard Anodize
d. Thermal Paint

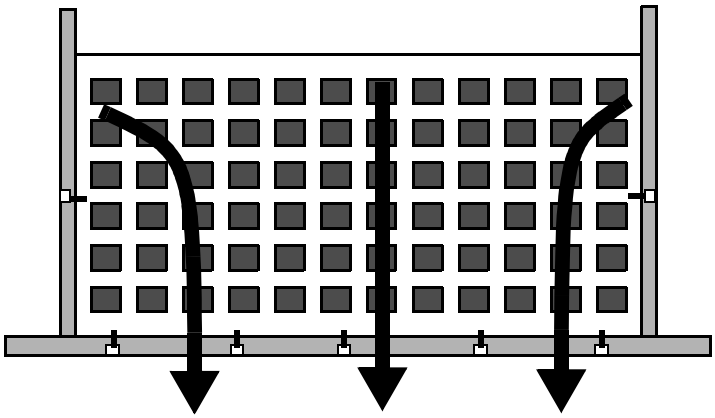

Figure 3.4-2 Thermal Design Path for DSP Modules

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1.4.3 Flame Retardant Materials. Flame retardant materials shall be used in all designs.

1.4.4 Polymerics. Applications requiring thermal conductance shall use bonding material as specified in JPL D-8208, Section 3.17.

1.4.4.1 Conductive Materials. Conductive heat transfer materials shall be used to keep electronic components within their operating limits.

1.4.5 Ceramics. Selection of ceramics shall consider thermal conductivity, thermal mismatch, EMI, surface finish, and bonding.

1.5 Fastener Requirements

1.5.1 Threaded Fasteners. The number of fasteners as a function of temperature difference can be determined from the joint resistance values for fasteners identified in Table 3.4-1.

1.5.2 Fastener Torque. Fasteners shall be torqued to the requirements of JPL D-8208, Section 3.3.

1.5.3 Inserts. Inserts shall be used when mounting high-power, stud-mount devices to aluminum.

1.6 Thermal Design Options

1.6.1 Baseline Options. The following thermal design options can be used to improve the thermal coupling of the piece parts to the heat sink in order to meet junction temperature requirements compared to thermal analysis results. The list is in order of decreasing thermal resistance. All designs shall employ the baseline option as a minimum.

Table 3.4-1 Threaded Fastener Joint Resistance Value

#4 Fastener	#6 Fastener	#8 Fastener	#10 Fastener
2.2°C or 4°F per Watt	1.7°C or 3°F per Watt	1.1°C or 2°F per Watt	0.7°C or 1°F per Watt

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1.6.2 PWB Design Options.

a. Baseline is 1 oz/in^2 copper internal layers and power/ground plane on layers 3/4

b. Heavy Copper, 2 oz/in^2, for all internal layers

c. 1 oz/in^2 copper for internal layers with power/ground plane moved to layers 2/3

d. Large pads, square, on back side of board

e. Large pads + extra vias under part

1.6.3 Part Mounting Options.

a. Baseline uses leads only for heat transfer from part to board.

b. Polymeric material between part and board

c. Shim under part bonding part to PWB

d. Strap or braid between part case and closeout edge

e. Top and bottom straps or braid to closeout edge

f. Shim plus top strap or braid to closeout edge

g. Board cutouts to chassis

h. Controlled torque stud mounting

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Surface Mount Technology

1 DESIGN REQUIREMENTS

For design rules, the following documents shall apply:

- ANSI/IPC-D-275 (September 1991), *"Design Standards for Rigid Printed Boards and Rigid Printed Board Assemblies."*
- NASA-STD-8739.2 (August 1999), *"Workmanship Standard for Surface Mount Technology."*
- IPC-SM-782, Rev. A (August 1993), "*Surface Mount Design and Land Pattern Standard*."
- ANSI/IPC-SM-839 (April 1990), "*Pre and Post Solder Mask Application Cleaning Guidelines*."

1.1 Producibility Level

The producibility level shall be either Level A (General Design Complexity) or Level B (Moderate Design Complexity) as defined in ANSI/IPC-D-275.

1.2 Design Rule Exceptions

1.2.1 General Exceptions.

1.2.1.1 Wave Soldering. Wave soldering shall be allowed for bottom side reflow, as appropriate.

1.2.1.2 Component Restrictions. The only types of SMCs that shall be placed on the bottom side (solder side) of a wave solderable PWB are SMC chip resistors, MELFs (resistors, diodes), and discrete SOTs.

1.2.2 Electronic Parts.

1.2.2.1 Plastic Encapsulated Microcircuits. PEMs for spacecraft flight applications shall be first qualified for the specific, intended application with approval from the procuring NASA agency.

1.2.2.2 Ceramic Resistors. Ceramic resistors with a minimum of three-side terminations shall be used; five-sided terminations are preferred.

1.2.2.3 Barrier Underplating. There shall be a barrier underplating of nickel between the external solderable layer of the end-cap termination and the internal silver-palladium layer to prevent silver being leached into the solder joint.

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1.2.2.4 Solderable Surface. Ceramic chip component terminations shall have a solder coating that meets the following requirements:

a. The solderable layer shall be a tin-lead alloy containing between 58 to 68% tin.

b. Plated from solution and fused using a post-plating reflow process.

c. The external solderable layer shall not have been produced by dipping.

d. The external solderable layer of the termination shall be 0.0003 inch minimum.

1.2.2.5 Mounting Configurations. I-lead or butt-mounted components shall be prohibited in flight hardware.

1.2.2.6 Flat Leads. The use of leads without stress relief shall be authorized by the NASA procuring agency on a case-by-case basis.

1.2.2.7 Leadless Chip Carriers. LCCs for spacecraft flight applications shall be first qualified for the specific, intended application with approval from the procuring NASA agency.

1.2.2.8 Lead Forming. Unless dictated otherwise by custom tooling, lead forming of flat-packs and quad flat-packs shall meet the requirements of Figure 3.5-1.

Note: Deviations require approval by the procuring NASA agency.

1.2.3 Component-to-Board Spacing. The distance between the component body and the surface of the PWB shall comply with the following:

a. Flat-pack and axial leaded devices—0.010" to 0.020"

b. Dual-inline Packages—0.060" minimum

c. TO-Cans (TO-5, TO-99, etc.)—0.030" minimum

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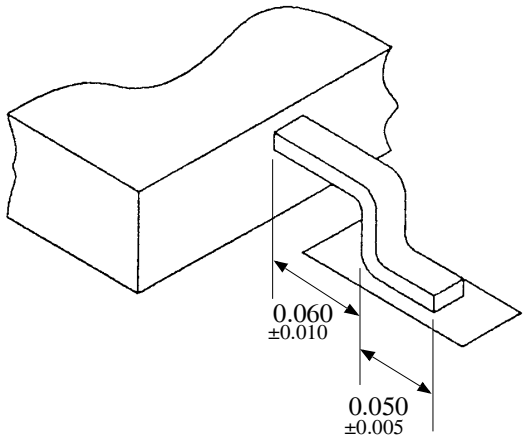

Figure 3.5-1 Typical Lead Form Dimensions for CFP and CQFP

1.2.4 Land Pattern Standards. Land patterns shall, at a minimum, meet the following requirements.

1.2.4.1 Chip Components. Land patterns for chip capacitors, chip resistors with five-sided terminations, and chip inductors shall meet the requirements of Figure 3.5-2.

1.2.4.2 Chip Resistors. Land patterns for chip resistors with three-sided terminations shall meet the requirements of Figure 3.5-5.

1.2.4.3 Tantalum Chip Capacitors. Land patterns for tantalum chip capacitors with fold-under ribbon leads shall meet the requirements of Figure 3.5-6.

1.2.4.4 MELF Devices. Land patterns for MELF devices shall meet the requirements of Figure 3.5-4.

1.2.4.5 Flat-pack and Quad Flat-pack. Land patterns for flat-packs and quad flat-packs shall meet the requirements of Figure 3.5-6.

1.2.4.6 Local Fiducials. A minimum of two local fiducials shall be placed on all footprints with 84 leads or more and footprints with lead pitch equal to or less than 0.025 inch.

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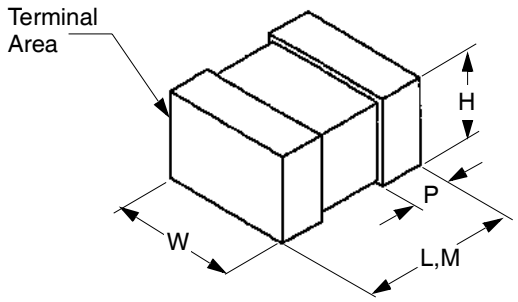
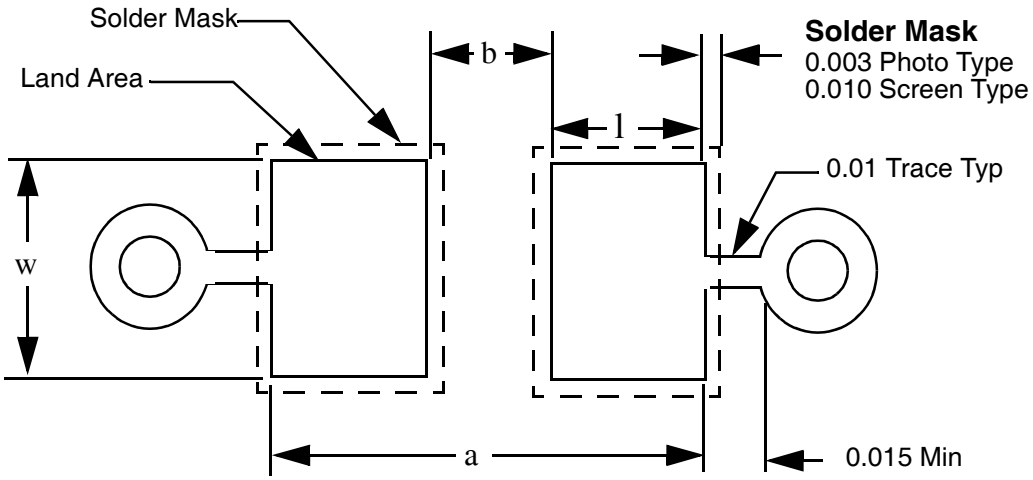
Chip Devices





Dimension*	Tolerance
W	Max
L	Max
M	Min
H	Max
P	Max

* Dimensions not including solder coat.

Formula

$a = L + {}^{H}/_{2} + 0.010$

$b = M - 2P - 0.010$

$b_{min} = 0.020$

$w = W + 0.020$

$l = \frac{a-b}{2}$

Figure 3.5-2 Chip Component Land/Pad Pattern Design

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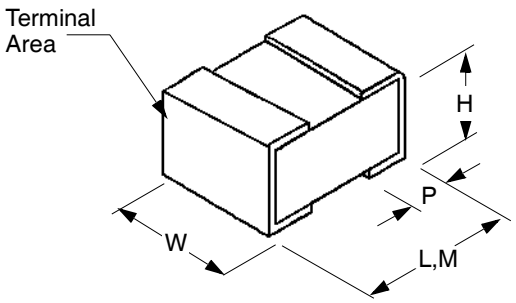
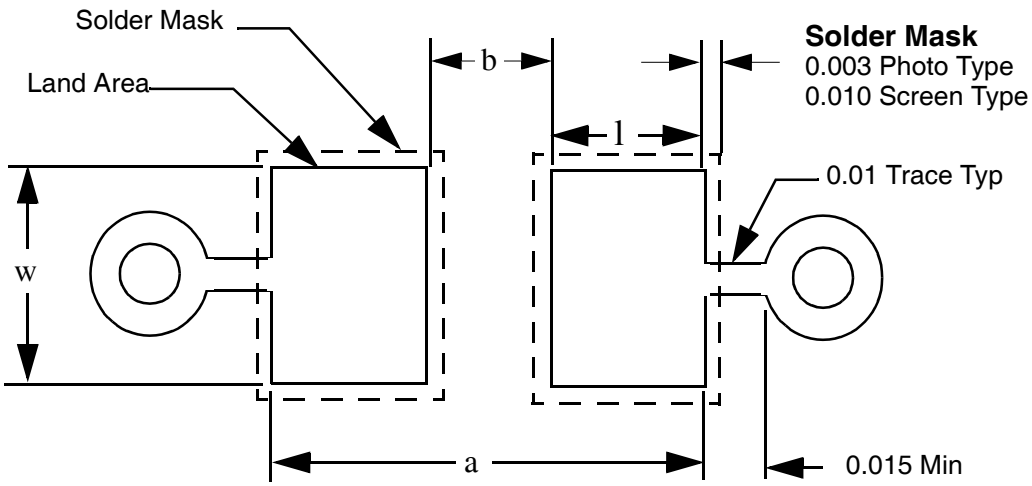
Chip Resistors
with Three-sided Terminations





Dimension*	Tolerance
W	Max
L	Max
M	Min
H	Max
P	Max

* Dimensions not including solder coat.

Formula

$a = L + {}^{H}/_{2} + 0.010$

$b = M - 2P - 0.010$

$b_{min} = 0.020$

$w = W + 0.005$

$l = \frac{a-b}{2}$

Figure 3.5-3 Chip Resistor Land/Pad Pattern Design

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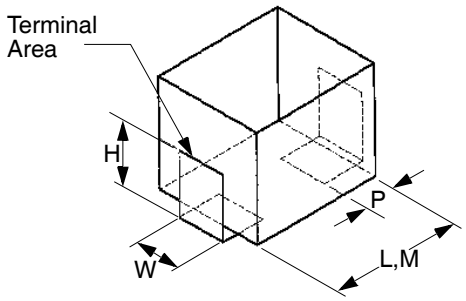
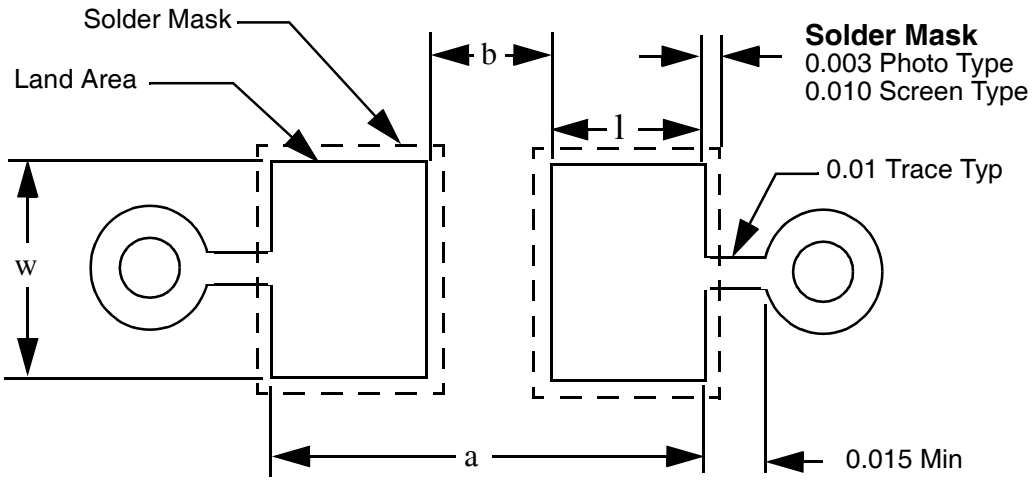
Tantalum Chip Capacitors
with Fold-Under Ribbon Leads





Dimension*	Tolerance
W	Max
L	Max
M	Min
H	Max
P	Max

* Dimensions not including solder coat.

Formula

$a = L + {}^{H}/_{2} + 0.010$

$b = M - 2P - 0.010$

$b_{min} = 0.020$

$w = W + 0.0120$

$l = \frac{a-b}{2}$

Figure 3.5-4 Tantalum Chip Capacitor Land/Pad Pattern Design

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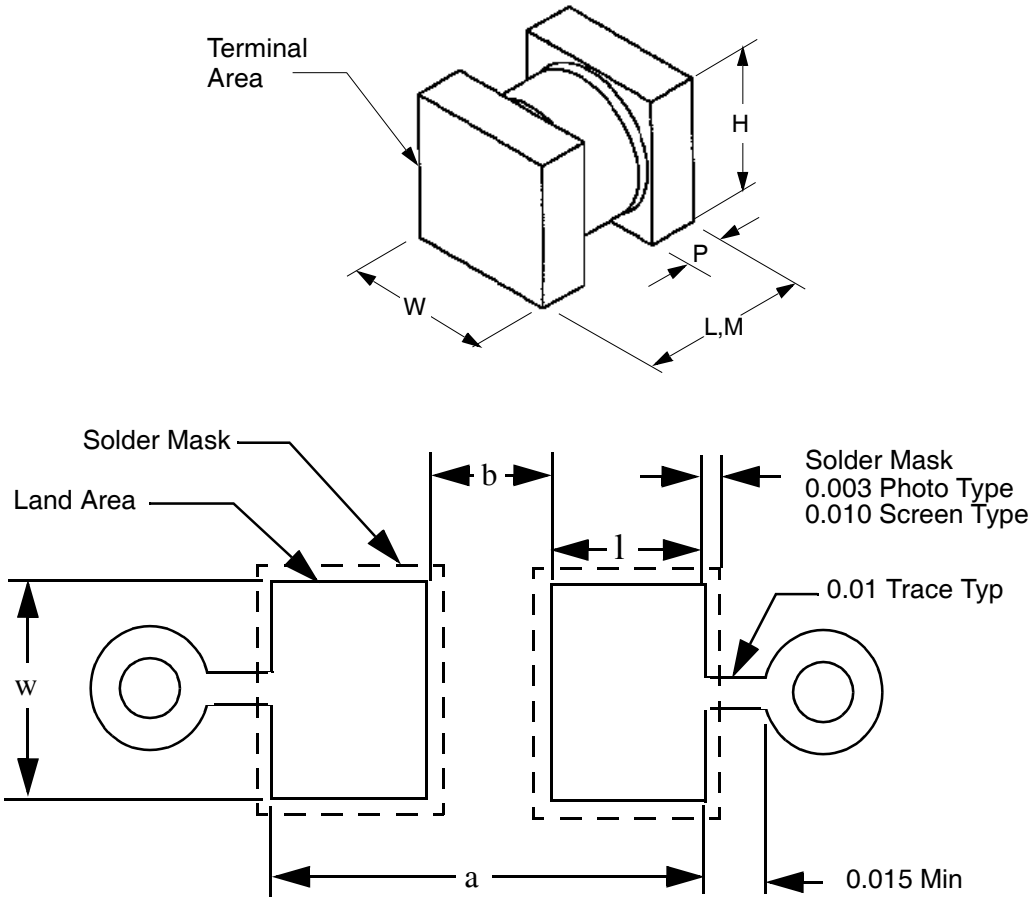
MELF Devices



Dimension*	Tolerance
W	Max
L	Max
M	Min
H	Max
P	Max

* Dimensions not including solder coat.

Formula

$a = L + {}^{H}/_{2} + 0.010$

$b = M - 2P - 0.010$

$b_{min} = 0.020$

$w = W + {}^{H}/_{2} + 0.005$

$l = \frac{a-b}{2}$

Figure 3.5-5 MELF Component Land/Pad Pattern Design

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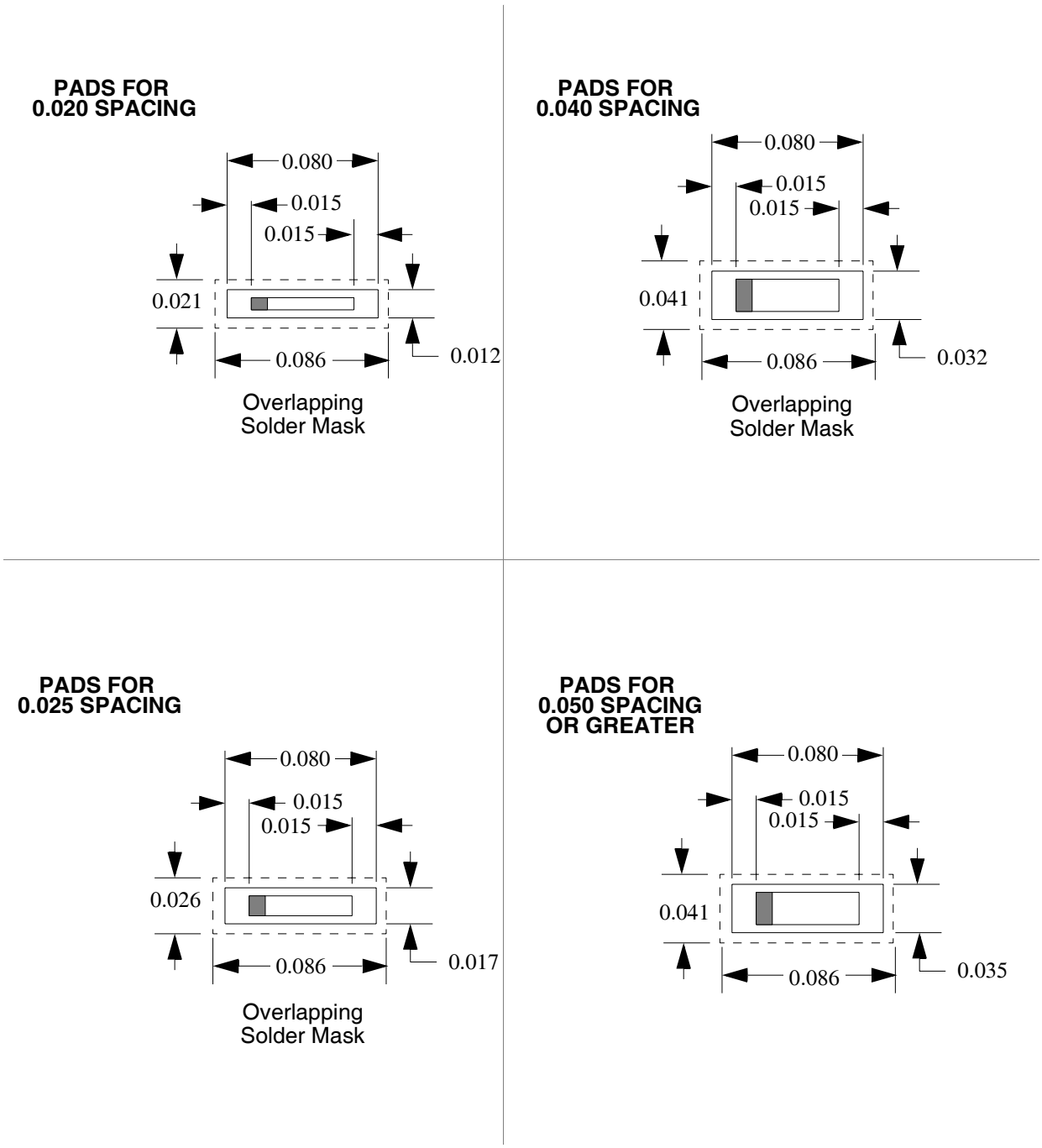

Figure 3.5-6 Typical Pads and Solder Mask Keepouts for CFP and CQFP

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2 ASSEMBLY REQUIREMENTS

Assembly requirements specific to surface mount technology processing shall be per NASA-STD 8739.2 (August 1999) *"Workmanship Standard for Surface Mount Technology."*

2.1 Assembly Rule Exceptions

2.1.1 Materials.

2.1.1.1 Type of Solder. All solder used shall be either eutectic (63%tin/37% lead, by weight); or tin/lead/silver (62% tin/36% lead/2%silver, by weight); or near-eutectic (60% tin/40% lead, by weight), eutectic solder is preferred.

2.1.1.2 Type of Flux/Paste. The only type of flux/paste that shall be allowed is rosin mildly activated (RMA).

2.1.2 Testing Requirements. The following testing requiremnts shall pertain.

2.1.2.1 Determination of Contamination Level in Solder. Every six months, the solder used shall be tested using appropriate instrumentation to determine the contamination levels of the solder. The results shall be documented in a manner suitable for inclusion as part of the documentation package delivered to JPL with the finished PWA.

2.1.2.2 Performance of Solderability Test for Solder Paste. Prior to the actual soldering operation, a test to determine the solderability of the solder paste shall be performed on a setup board.

2.1.2.3 Performance of Solderability Test for PWB/SMCs. Prior to the actual soldering operation, a test to determine the solderability of the PWB and SMCs shall be performed on a setup board.

2.1.2.4 Determination of Solder Paste Volume. Solder paste volume shall be verified by suitable methods and the results documented in a manner suitable for inclusion as part of the documentation package delivered to JPL with the finished PWA.

2.1.3 Lead Forming.

2.1.3.1 Flat-packs and Quad Flat-packs. Flat-pack and quad flat-pack leads shall be formed by machine and/or die in compliance with Figure 3.5-1 on page 3.5-3.

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2.1.3.2 Coined (Flattened) Leads. The procedure for coining leads shall be approved by the procuring NASA agency.

2.1.3.3 Base Material Exposure. Nicks, cracks, and other deformations which expose base material are prohibited.

2.1.3.4 Toe-up/Toe-down. Toe-up/toe-down shall be less than 0.004 (0.1 mm).

2.1.3.5 Hermeticity Testing. After forming and trimming, hermetically sealed integrated circuits with lead egress directly from the package cavity and DIPs shall be tested for leaks per MIL-STD-883, Method 1014.10, fine and gross.

2.1.4 Terminal Mounting.

2.1.4.1 PTH Mounting. When the use of terminals mounted in PTHs has been approved by the procuring NASA agency, they shall be installed using a flared flange swage.

2.1.4.2 Part Installation. Installation of parts on terminals shall be per JPL D-8208, Section 3.16.

2.1.5 Tinning. Component leads shall be tinned and comply with the following requirements prior to installation:

a. All soldered surfaces are smooth and completely wetted with solder.

b. There are no projections, bridges, fractures, inclusions, or porosity.

c. No flux residue remains after the cleaning process.

d. All devices with a pitch 0.020 inch or less shall be robotically tinned by an acceptable automated robotic tinning machine.

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2.1.5.1 Gold-plated Leads or Terminations. Gold shall be removed form component leads and terminations by immersion in a dedicated solder bath prior to tinning in compliance with the following:

a. The lead shall be immersed in a dynamic bath, or with slow movement through a static bath for 2-5 seconds.

b. Gold contamination in the first solder bath shall be less than 4%.

2.1.6 Alignment Requirements.

2.1.6.1 Lead Side Overhang. For surface mounted parts with lead pitch 0.050 inches and greater, including chip components, the lead side overhang is prohibited (e.g., leads are coincident with the side of the pad).

2.1.6.2 Lead Toe Overhang. For gull wing leads (i.e., lap joints), lead toe overhang shall be less than or equal to 0.005 inches, or 10% of the lap joint length, whichever is less, while not decreasing the conductor-to-conductor spacing greater than 20%.

2.1.7 Reflow Requirements.

2.1.7.1 PEM Storage. PEMs shall be stored in an inert atmosphere to prevent moisture ingression prior to assembly.

2.1.7.2 PEM Bakeout. Within one hour before assembly, the PEMs shall be baked to remove moisture.

2.1.7.3 Time/Temperature Profile. A time/temperature profile shall be established and documented for each reflow process.

2.1.7.4 Dual Vapor/Batch Vapor Phase Reflow Prohibition. The use of dual vapor/batch vapor phase reflow systems shall be prohibited.

2.1.7.5 Hot Bar Soldering Prohibition. The use of hot bar soldering shall be prohibited.

2.1.8 Cleaning after Soldering. Cleaning after soldering shall be performed within 30 ±5 minutes after the soldering operation.

2.1.8.1 Time Window for Performing Cleaning. Prior to application of conformal coating, PWAs shall be cleaned within 30 ±5 minutes after the soldering operation or stored in a drybox until processing can resume.

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2.1.8.2 Ozone Depleting Chemicals. No ozone-depleting chemical shall be used to clean PWAs.

2.1.8.3 Ionic Contamination Testing Prior to Conformal Coating. After cleaning, but prior to applying any type of conformal coating, ionic contamination testing shall be performed and documented for each PWB with the following restrictions:

a. Contamination Level. The ionic contamination level shall not exceed 10 micrograms per square inch.

b. Component Area. The approximate area of the components shall be accounted for in computing the board area.

c. Recleaning. If any PWA shows an ionic contamination level equal to or greater than 10 micrograms per square inch, it shall be recleaned until it shows a less than 10 micrograms per square inch.

d. Documentation Package. The ionic contamination information shall be part of the document package delivered to JPL with the finished PWA.

2.1.9 Solder Connections.

2.1.9.1 Fillet Geometry. A concave fillet of solder shall exist between the conductor and the termination.

2.1.9.2 Contact Angle. Solder conditions shall indicate wetting and adherence where the solder blends to the soldered surface by forming a contact angle of 45° or less, except when the configuration and quantity of solder results in a contour which extends over the edge of the land.

2.1.9.3 PWB Damage. Blistering or delamination bridging 50% of the distance between PTHs or between subsurface conductors, or which extends 50% of the distance under surface/subsurface conductors and other subsurface conductors shall be cause for rejection.

2.1.9.4 Component Damage. Damage to components beyond the allowance of the procurement specification is prohibited.

2.1.9.5 Stressed Solder Joints. Stress lines in solder joints shall be cause for rejection.

2.1.10 Lap Joints (Gull-wing Leads).

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2.1.10.1 Minimum Fillet. Lap joints, both flat and round lead, shall have a complete fillet for a minimum of three sides or 75% of the joint periphery.

2.1.10.2 Heel Fillet. Lap joints shall have a complete heel fillet.

2.1.10.3 Maximum Fillet. Lap joint solder fillets shall not extend into the top bend and have a maximum heel fillet of one-half the lead bend height as shown in Figure 3.5-7.

2.1.11 Rework and Repair. Rework and repair shall be in accordance with JPL D-8208, Section 3.15.

2.1.12 Deliverables. All PWAs shall be hand delivered with a certificate of compliance to NASA-STD 8739.2 accompanying the documentation package.

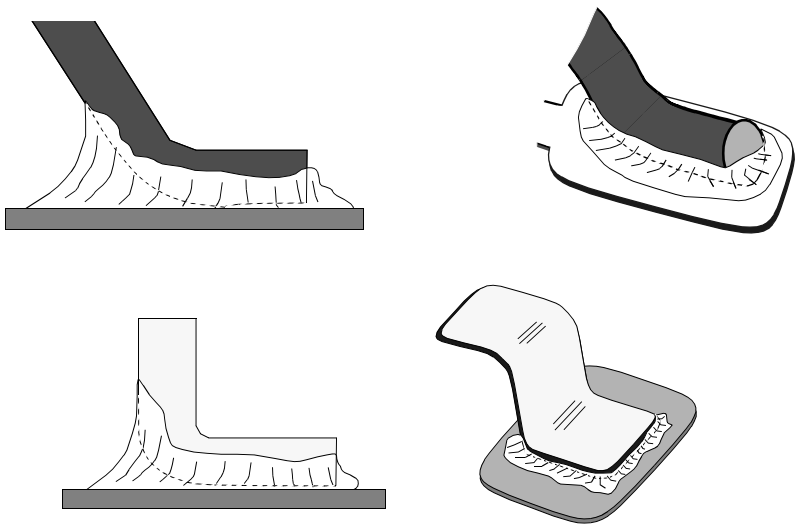

Figure 3.5-7 Round and Flat Lap Joints

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3 QUALITY ASSURANCE

3.1 Acceptance Criteria

NASA-STD 8739.2 shall be used as acceptance criteria.

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Printed Wiring Boards

1 SCOPE

This specification sets forth the requirements for the design and fabrication of flight rigid electronic printed wiring boards (PWBs) to meet the stringent demands of JPL. In general, the IPC documents (both for design and performance) cited in paragraphs 4, 4.7, and 5 are sufficient. Where these documents do not suffice, requirements more rigorous or far-reaching than the IPC documents are called out below.

1.1 Purpose

This specification provides the requirements and quality assurance provisions for rigid PWBs procured for use in spacecraft and scientific instruments for space applications and other high reliability uses.

1.2 Applicability

This specification is applicable to all NASA Jet Propulsion Laboratory (JPL) programs and contracts using PWBs for space flight applications and critical ground support equipment. It shall be invoked on all procurements for flight and critical ground support equipment PWBs. It shall apply to all in-house design efforts, all direct outside vendor procurements, and also to sub-tier vendor-manufactured PWBs for JPL programs and/or contracts.

1.3 PWB Types

The boards include the following types:

- Type 1 - Single-sided PWB;
- Type 2 - Double-sided PWB;
- Type 3 - Multilayer PWB (MLB) without blind or buried vias;
- Type 4 - Multilayer PWB (MLB) with blind or buried vias.

1.4 Assembly Methods

The two assembly methods in common use are manual assembly and automated SMT assembly. Assembly refers to the mounting and subsequent soldering of components to

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the PWB surface. In manual assembly the components are hand mounted and hand soldered. If automated assembly is used, the components are mounted by the use (or partial use) of a piece of equipment dedicated to mounting components on the PWB. Such a machine is commonly referred to as a pick-and-place machine. The soldering techniques used are mass soldering techniques such as vapor phase reflow. The soldering operation creates a sturdy metallurgical bond (interconnect) between the components' I/Os, or leads, and the PWB.

For manual assembly, refer to JPL D-8208, Section 3.14, Component Mounting/Soldering; for automated SMT assembly refer to JPL D-8208, Section 3.5, Surface Mount Technology. Some assemblies may be assembled using a combination of the two. It is necessary to mention these assembly methods in this section since certain requirements at the PWB level are directly affected by the assembly method used to populate the PWB. In this document, PWBs that will be assembled using the Automated SMT method are referred to as "SMT PWBs." Some of the requirements in this section apply strictly to SMT PWBs, e.g., fiducials. See paragraph 4.8.5 on page 3.6-24.

2 GENERAL INFORMATION

2.1 Role of Electronic Packaging and Fabrication

As part of the DBAT process, all flight and engineering model (EM) PWBs should be procured through Section 349, Electronic Packaging and Fabrication. The term PWB encompasses rigid boards, rigid-flex boards, and flex boards. In addition to flight and EM boards, all other PWBs should also be procured through Section 349. Section 349 maintains a controlled Approved Vendor List (AVL) for the explicit purpose of facilitating the procurement of PWBs of all quality levels from flight to breadboard. Section 349 can quickly facilitate the procurement of PWBs since it maintains close contact with the PWB vendor base and periodically assesses the vendors' capabilities.

2.2 Waivers and Deviations

The requirements set forth in this document have been developed to ensure that the PWBs procured using this procedure meet or exceed expectations and to maintain the attendant risk at an acceptable level. Any or all of these requirements may be waived. However, the cognizant engineer must be aware that as requirements are waived, the risk of failure increases. The cognizant engineer, in conjunction with the program manager, must decide if this risk is worth waiving the requirements. All waivers to the

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requirements shall be obtained from the DBAT Process Owner in written form. See *Category A Waiver Request/Approval* on DMIE.

2.3 Vendor Selection and Qualification

2.3.1 Vendor Selection. A recommendation may be made to add a particular vendor to the AVL based on either prior experience with the vendor or due to the vendor's outstanding reputation and/or unique capabilities. In this case, a JPL vendor survey team will perform a survey of the vendor's facility.

2.3.2 Vendor Capability. When assessing a vendor regarding his/her capability to build PWBs, the following items shall be reviewed and ascertained:

- Capability to build state-of-the-art rigid polyimide PWBs and rigid FR-4 PWBs;
- Capability to build specialty PWBs such as flex, rigidflex, PTFE (e.g., Duroid) boards, Thermount boards, etc.;
- Capability to build a particular category of PWB, e.g., a vendor that specializes in quick turnaround, prototype PWBs may not be the optimal choice for building flight PWBs;
- A proven track record for providing high reliability PWBs;
- For rigid PWBs, certification to MIL-P-55110 (the current version) shall be required;
- For flex and rigidflex PWBs, being able to fabricate to MIL-P-50884 (the current version) shall be required;
- For PWB acceptability, use of IPC-A-600 (the current version) shall be required;
- Although not required, it is desirable that the PWB vendor be certified to ISO 9002, or be actively seeking certification, or at a minimum be ISO compliant;
- Successful compliance to the JPL Vendor Survey shall be required.

2.3.3 Survey Team. To determine a particular vendor's capability, a JPL survey team shall visit the vendor at his facility. Prior to being surveyed, a potential vendor shall be sent a letter informing them that a JPL Survey Team will be visiting their facility. At the same

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time as the letter is sent, the vendor will also be sent a survey questionnaire entitled *PWB Vendor Information Questionnaire* (D-21523). This questionnaire shall be completed before or at the time of the survey, preferably before. It is the responsibility of Section 349 to keep the questions of this survey updated in a timely fashion. The survey questionnaire shall be employed to assess the particular vendor's capability.

The survey team shall consist of at least one representative from Section 349 (Electronic Packaging and Fabrication) and at least one representative from Section 512 (Quality Assurance). The team may also include a representative from Procurement. QAP 30.42, "*Quality Assurance Survey of Printed Wiring Board Suppliers*," shall be used as the governing document for the survey process.

2.3.4 Vendor Qualification. During or shortly after the survey, an informal profile of the vendor may be completed to conveniently summarize vendor information. It is also highly recommended that the vendor have completed IPC-1710 (12/97), "*Manufacturer's Qualification Profile (MQP)*," and have it available upon request. If the particular PWB facility is approved, the facility with an appropriate contact is added to the AVL (see section 2.3.5). The vendor shall be notified either via telephone or email or both that he/she has been qualified.

2.3.5 Approved Vendor List. A list of suitable PWB vendors qualified for fabricating PWBs for JPL shall be kept. This list of suitable vendors shall constitute an Approved Vendor List (AVL); this AVL shall be maintained by Section 349 in a suitable format by the PWB Process Engineer. It is to be shared only on a valid as-needed basis.

2.3.6 Vendor Disqualification and Requalification. A vendor may be disqualified due to poor quality and/or untimely delivery. In the event that a particular vendor is disqualified, they shall be sent a letter specifying in exact detail why they are being disqualified and what steps are recommended in order to obtain requalification. This letter shall be written by QA and Section 349. In the event that disqualification is felt warranted, the vendor's name will be removed from the JPL AVL. If it is thought worthwhile to requalify the vendor based on corrective actions taken by the vendor to remedy the disapproval, a JPL Vendor Survey Team shall again perform a survey and follow the procedure stated above for new vendors.

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3 ENGINEERING AND LAYOUT CONSIDERATIONS

3.1 Design For X

There are a number of important considerations that the designer should take into account to produce a high quality PWB. The following are set forth for heuristic consideration. These are:

- Design For Producibility.
- Design For Assembly.
- Design For Inspectability.
- Design For Testability.

It is the designer's responsibility to take into account all of the above in exercising the design function. Failure to take the above into consideration can result in an unsatisfactory product, that is, one that does not perform as intended in its service environment over the time period for which it was intended.

Designing for X is a nontrivial issue since if performed correctly, it results in a significant cost savings and generally a superior product. Costs escalate as the product passes out of the design stage through board fabrication and assembly and into final system test and integration. If a faulty product is not detected at that stage, it may result in a mission that is seriously compromised or that fails.

3.1.1 Design For Producibility (DFP). The aspects of DFP are:

- Do not needlessly design a PWB to a producibility level that makes it difficult to build the board.
- Adhere to recognized design rules.
- Plan ahead so that the PWB doesn't have to be fabricated under rushed conditions.

3.1.1.1 Producibility Level. The IPC documentation no longer supports a definition of producibility level. However, as an aid to the PWB Layout Designer, the following is set forth to define a heuristic probability level based on several pertinent board factors.

The following factors are used to define a producibility level. The parameters are:

- Trace width/trace spacing;

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- Number of layers;
- X-Y dimensions;
- Number of plated holes;
- Aspect ratio;
- Blind/buried vias;
- Controlled impedance.

Each factor is assigned a particular value of its Producibility Number in one of the corresponding tables. Then, given the parameters for a given PWB, find its corresponding Overall Producibility Number by adding the Producibility Numbers for the individual factors. A careful review of the various producibility numbers of each factor will also give the PWB Layout Designer a better feel for the impact of each factor. For example, trace width/trace spacing has a greater affect on overall producibility than the number of plated holes.

The Overall Producibility Number so calculated should be used strictly as an heuristic aid to the PWB Layout Designer so that he can arrive at a sense of how producible his PWB is. If he has any questions regarding the producibility of any PWB, he should consult with the appropriate PWB Process Engineer.

(1) Trace width/trace spacing

Trace width/ trace spacing	10 mil/10 mil to 8 mil/8 mil	7 or 6 mil/7 or 6 mil	5 mil/5 mil	Less than 5 mil/5 mil
Producibility number	2	5	10	20

(2) Number of layers

Number of layers	4 but less than 8	8 but less than 14	14 but less than 18	18 or greater
Producibility number	2	8	14	20

Note: Single-sided and double-sided PWBs have a Producibility Number of 0 for this parameter.

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(3) X-Y dimensions

X-Y Dimensions	L ≤ 4" and/or W ≤ 4"	L ≤ 12" and/or W ≤ 12"	L < 18" and/or W < 18"	L ≥ 22" and/or W ≥ 22"
Producibility number	2	8	14	20

(4) Number of plated holes

Number of plated holes	Less than 500	500–999	1000–3,000	Greater than 3,000
Producibility number	2	4	7	10

(5) Aspect ratio

Aspect Ratio	Less than or equal to 6:1	Greater than 6:1 and less than/equal to 8:1	Greater than 8:1 and less than/equal to 10:1	Greater than 10:1
Producibility number	2	5	10	15

Note: The aspect ration (AR) of a PWB is the board thickness to the minimum drilled hole diameter. For example, if the minimum drilled hole diameter is 0.016 inch and the board thickness is 0.125 inch, the AR = 0.125:0.016 = 8:1 (app.).

(6) Blind and/or buried vias

Blind and/or buried vias	Yes
Producibility number	20

(7) Controlled impedance

Controlled impedance	±10% tolerance	Less than ±10% tolerance
Producibility number	7	15

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Table 3.6-1 Producibility Level of a PWB

Overall Producibility Number	Level of Difficulty	Producibility Level
90-120	Extremely hard	4+
70-89	Very Hard	4
55-69	Hard	3
40-54	Average	2
20-39	Easy	1
Less than 20	Very easy	1

Examples of producibility levels calculated using the tables above.

Example 1: A PWB has trace width/spacings of 0.007 inch/0.007 inch. The board is 12 layers. The board dimensions are 10.00 inch × 6.000 inch. it has 350 plated-through-holes. The board thickness is 0.062 inch and the minimum drilled hole diameter is 0.016 inch. Therefore, AR = 3:1 (app.). There are no blind/buried vias. No controlled impedance

Overall Producibility Number = (1) 5 + (2) 8 + (3) 8 + (4) 2 + (5) 2 + (6) 0 + (7) 0 = 25
Conclusion: Easy to produce
Producibility Level: 1

Example 2: A PWB has trace width/spacings of 0.005 inch/0.005 inch. The board is 14 layers. The board dimensions are 14.000 inch × 9.500 inch. It has 1,200 plated-through-holes. The board thickness is 0.062 inch and the minimum drilled hole diameter is 0.013 inch. Therefore, AR = 5:1 (app.). There are no blind/buried vias. No controlled impedance.

Overall Producibility Number = (1) 10 + (2) 14 + (3) 14 + (4) 7 + (5) 2 + (6) 0 (7) 0 = 47
Conclusion: Average producibility
Producibility Level: 2

Example 3: A PWB has trace width/spacings of 0.005 inch/0.005 inch. The board is 14 layers. The board dimensions are 18.000 inch × 12.000 inch. It has 2,900 plated-through-holes. The board thickness is 0.125 inch and the minimum drilled hole diameter is 0.013 inch. Therefore, AR = 10: 1 (app.). There are no blind/buried vias. No controlled impedance.

Overall Producibility Number = (1) 10 + (2) 14 + (3) 14 + (4) 7 + (5) 10 + (6) 0 (7) 0 = 55
Conclusion: Hard to produce
Producibility Level: 3

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Example 4: A PWB has trace width/spacings of 0.005 inch/0.005 inch. The board is 14 layers. The board dimensions are 18.000 inch × 12.000 inch. It has 2,900 plated-through-holes. The board thickness is 0.125 inch and the minimum drilled hole diameter is 0.013 inch. Therefore, AR = 10:1 (app.). There are blind vias in the top two and bottom two layers. No controlled impedance.

Overall Producibility Number = (1) 10 + (2) 14 + (3) 14 + (4) 7 + (5) 10 + (6) 20 (7) 0 = 75
Conclusion: Very hard to produce
Producibility Level: 4

Example 5: A PWB has trace width/spacings of 0.005 inch/0.005 inch. The board is 14 layers. The board dimensions are 18.000 inch × 12.000 inch. It has 2,900 plated-through-holes. The board thickness is 0.125 inch and the minimum drilled hole diameter is 0.013 inch. Therefore, AR = 10:1 (app.). There are blind vias in the top two and bottom two layers. Controlled impedance ± 10%.

Overall Producibility Number = (1) 10 + (2) 14 + (3) 14 + (4) 7 + (5) 10 + (6) 20 (7) 7 = 82
Conclusion: Very hard to produce
Producibility Level: 4

Example 6: A PWB has trace width/spacings of 0.004 inch/0.004 inch. The board is 14 layers. The board dimensions are 18.000 inch × 12.000 inch. It has 3,500 plated-through-holes. The board thickness is 0.125 inch and the minimum drilled hole diameter is 0.013 inch. Therefore, AR = 10:1 (app.). There are blind vias in the top two and bottom two layers. Controlled impedance ± 5%.

Overall Producibility Number = (1) 20 + (2) 14 + (3) 14 + (4) 10 + (5) 10 + (6) 20 (7) 15 = 103
Conclusion: Extremely hard to produce
Producibility Level: 4+

3.1.1.2 Design Rules. The designer shall follow recognized design rules for designing the PWB, and shall exercise sound judgment in ensuring that the board shall not deviate too greatly from recognized designs. The following are particularly sensitive to DFP:

- Make sure that the aspect ratio (AR) is no greater than 8:1. An AR of 6:1 or less is preferred.
- Trace width/trace spacing should be no less than 0.005 inch.
- If the board is a multilayer, make sure that the construction is symmetrical.

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- Pad size for plated holes. The formula for calculating minimum pad size is:

  $$PAD_{min} = FHS_{nom} + 2ar + FA$$

  where FHS_{nom} = nominal finished hole size
  ar = minimum annular ring allowed
  FA = fabrication allowance (varies from one PWB facility to another).

  Bear in mind that the PWB vendor must control both the layer-to-layer registration and the hole-to-pad registration when producing a multilayer PWB.

Example: When designing pad sizes, bear in mind this chart:

PAD SIZE	**EASE OF FABRICATION**
FHS_{nom} + 0.024 inch	PREFERRED
FHS_{nom} + 0.018 inch	STANDARD
FHS_{nom} + 0.014 inch	ADVANCED
FHS_{nom} + 0.012 inch	VERY ADVANCED (some PWB facilities may not be able to do this)

Also remember that if the finished hole size is specified as 0.018 ± 0.003 inch, then the calculated FHS_{nom} will be 0.018 inch. However, if the finished hole size is specified as 0.018 + 0.003-0.001 inch, then the calculated FHS_{nom} will be 0.019 inch, not 0.018 inch.

Based on this, one can arrive at various pad sizes for a FHS_{nom} = 0.018 inch

PAD_{min} = 0.042 inch	PREFERRED
PAD_{min} = 0.036 inch	STANDARD
PAD_{min} = 0.032 inch	ADVANCED
PAD_{min} = 0.030 inch	VERY ADVANCED

3.1.1.3 Planning. In addition to following good design rules, both the designer and the project engineer should plan effectively to avoid a situation in which the PWB vendor must hastily fabricate the PWB. It is important to remember that the more complex the PWB, the more lead time should be allowed for its fabrication. Compressing the lead time is not recommended. A rule-of-thumb table is given below to guide the designer and project engineer. See Table 3.6-2.

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Table 3.6-2 Fabrication Allowance Time

Type of PWB	Recommended time allowable for fabrication after placement of the PO*
Single-sided PWB	3 days
Double-sided PWB	3-5 days
4-6 lyr MLB (multilayer board)	2-3 wks.
8 lyr and > 8 lyr MLB	3-4 wks.
Blind and/or buried vias MLB	4-5 wks.
Line widths/line spaces < 0.005"	3-4 wks.
Controlled impedance board	4-5 wks.

*. PO = purchase order. Placement is defined as that date in which the vendor receives the PO documentation.

4 DESIGN REQUIREMENTS

Design rules for printed wiring boards (PWBs) shall be per the documentation hierarchy set forth in IPC-2221 (1998), *"Generic Standard on Printed Board Design."* Regarding rigid printed wiring boards, the chief document, in addition to IPC-2221 (1998), is IPC-2222, *"Sectional Design Standard for Rigid Organic Printed Boards."* Exceptions to these two documents are detailed in this section. In addition, the designer is strongly encouraged to peruse the Section 349 (Electronic Packaging and Fabrication) procedure, *Printed Wiring Products Acquisition*, which can be viewed by going to http://section349.jpl.nasa.gov and clicking "MCDL."

4.1 Preferred Units

The preferred units are English (inch or mil where 1 mil = 0.001 inch) rather than metric (millimeters [abb. mm]). The units shall be given in English with hard metric units in parentheses. Note that the above IPC standards utilize metric units (mm) in all tables. If conversion is necessary, use the following conversion factor:

$$X(\text{in mm}) \times 0.03937 = Y \text{ inch.}$$

4.2 Performance Class

The performance class shall be IPC Class 3, High Reliability Electronic Products.

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4.3 Dimensioning and Tolerancing

All dimensions and tolerances shall be per ANSI Y14.5.

4.4 Electrical Testing

There are two aspects to electrical testing. There is electrical verification testing at the PWB facility, and in addition, for flight PWBs, an Integri-Test is performed in Section 349.

4.4.1 Electrical Verification Testing at the PWB Vendor. Electrical verification testing shall be conducted at the vendor's facility, and the vendor shall ensure that this test is performed. If the vendor subcontracts the work to a test facility, the vendor shall inform JPL that this is being done prior to the test being performed. JPL shall have a say if the subcontracted testing facility is adequate.

All electrical testing shall be conducted at 200 Vdc minimum. Unless otherwise specified on the drawing, electrical verification testing shall consist of netlist testing using suitable test instrumentation. The PWB vendor shall be supplied with an IPC-D-356A file supplied along with the Gerber files in the ZIP file (see 4.10 below) for the purpose of electrical testing. See paragraph 4.4.2.2 below. The results of such a test shall constitute one of the deliverables to JPL. See paragraph 6.2 below.

4.4.1.1 Netlist Comparison between the Design Database Netlist File and the Gerber Extracted Netlist File. In addition, the vendor shall perform a netlist comparison between the IPC-D-356A file generated directly from the design database (schematic netlist) and the extracted netlist file from the Gerber data (extracted netlist). In this way, electrical continuity and isolation errors can be detected at the time the front-end engineering (FEE) is performed at the PWB vendor's facility rather than at electrical test when the PWBs have already been manufactured. In the event that discrepancies are found, the PWB vendor shall inform the JPL PWB Coordinator and/or the JPL PWB Process Engineer, preferably by email. The PWB Coordinator shall inform the PWB vendor to put the job on hold, by email, until all discrepancy issues are resolved. When all discrepancies have been resolved, the PWB Coordinator shall inform the PWB vendor to resume the PWB build, by email.

4.4.2 Integri-Test. Flight PWBs shall have complete netlist testing by Section 349 prior to assembly. In addition, engineering model (EM) PWBs should be considered as potentially flight PWBs, and they too shall have complete netlist testing prior to

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assembly. Both double-sided (DS) PWBs and multi-layer boards (MLBs) shall have netlist testing.

At a minimum, at least one flight PWB per lot shall have netlist testing performed on the Integri-Test testing machine. The name of the netlist testing machine used by section 349 is the Integri-Test® testing machine. At the same time, if the PWB is a surface mount technology (SMT) board, at least one flight PWB per lot shall also be tested for adequate solderability. The Planning Engineer[1] shall indicate on the Service Order (SO) that the Integri-Test shall be part of the procurement of all flight PWBs. There are two separate conditions relating to the generation of an appropriate file for the Integri-Test so that it may be conducted.

4.4.2.1 Integri-Test (IT) Service Process for PWBs. The IT service process originates through the SO request process at the time of the original request to buy PWBs from a vendor is executed. After the PWB order has been delivered and inspected (with an accompanying Inspection Report, i.e., IR), a single PWB is selected to be IT processed. The selection is normally done from the highest serial number available; it could however be the one board that has the most superficial flaws discernible by unaided visual check.

The PWB Coordinator delivers the procured hardware package to the Planning and Control Planner. The Planning and Control Planner logs the task into the Production Planning and Control system and then make arrangements with the IT File Engineer (ITFE) to produce a compatible file for execution in the Integri-Test computer. At the same time, the Planning and Control Planner solicits an AIDS from the appropriate Fabrication Engineer for test execution. The Planning and Control Planner is also responsible for the appropriate QA signatures on the AIDS prior to start of test. This AIDS will include both the IT service and the SERA solderability test service. The file and AIDS, along with the original package, is handed to the IT Coordinator for testing.

Upon completion of both tests, QA does a buyoff by generating an IT IR. Copies of the IR and data package, along with the original materials and PWB, are returned to the Planning and Control Planner for final disposition. The Planning and Control Planner then places the tested PWB back into the Production Planning and Control system.

1. The Planning Engineer is generally the person responsible for generating the Service Order (SO).

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4.4.2.2 Files Placed on DocuShare. Thus, there will normally be three separate files placed in DocuShare by the Planning Engineer. These are:

(1) The output file from the design database (either an IPC-D-356A file or a Neutral file);

(2) The IPC-D-356A file generated by the IT File Engineer or another designated party if a Neutral file is supplied;

(3) The IPC-D-356A file converted to an ASCII file by the Integri-Test technician.

4.4.3 Alternative Procedure for Creating an IPC-D-356A File. If an E-CAD system not capable of generating either an IPC-D-356A file or a Neutral file, it shall then be the responsibility of the PWB designer (or a designated third party) to ensure that a file is directly generated from the design database that can be converted into an IPC-D-356A file. It is the responsibility of the designer to ensure that the final output is an IPC-D-356A file. If the designer cannot ensure this, he/she should negotiate with the cognizant engineer to arrange to have this done.

4.5 PWB Identification

The designer shall follow the recommendations in this paragraph to the extent that it is practical and design rules are not violated. The designer shall ensure that the PWB artwork shall have both a FAB (PWB fabrication) number and an ASSY (PWA = printed wiring assembly) number on the top side of the PWB so that these numbers are etched in the PWB along with the traces, vias, etc. The FAB number and the ASSY number shall agree with the drawing numbers. In addition, the word REV. and S/N (serial number) shall also be etched in the PWB. For ease of identification, the FAB number shall be indented. However, the fields after REV. and S/N shall be left blank.

ASSY 101XXXXX REV. S/N

FAB 101XXXXY REV. S/N

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If the above is not feasible due to space limitations on the board, the designer should have the first row on the top side of the PWB

ASSY 101XXXXX REV. S/N

and the second row on the bottom side.

FAB 101XXXXY REV. S/N

If convenient, the designer shall have the artwork contain the acronym of the project so that it too is etched into the board. If the PWB has a backing board that will be bonded to the bottom side, then the designer should revert to placing both on the top side.

Note: By definition the top side of the PWB is the side appearing by looking down on the PWB from above. This is also often designated the component side. However, some boards today have components on both sides of the board.

The PWB vendor shall have the responsibility of filling in the REV. field and the S/N field of the bare PWB either with the silk screen or by a suitable marking technique. These numbers shall be clearly legible. If possible, the PWB vendor should modify the artwork so that the S/N numbers are etched into the PWB. When the PWBs are received back from the PWB vendor, the identification fields should appear as such.

PWB #1

ASSY 101XXXXX REV. S/N
FAB 101XXXXY REV. X S/N 001

PWB #2

ASSY 101XXXXX REV. S/N
FAB 101XXXXY REV. X S/N 002

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In addition, a Lot Date Code shall be marked on the board by the PWB vendor using a suitable technique to ensure that the code is legible. If there is room at the top of the board, the company shall give their name, e.g., Golden Era Circuits. Otherwise, the name shall appear on the bottom of the board. Panel location numbers shall not be acceptable as S/N numbers.

4.5.1 Serialization in the Case of PWB Rebuild. If delivery of the PWBs is made, the PWBs are accepted by JPL, and the PWB manufacturer has occasion to rebuild the boards, the S/N numbers shall be increased by 100. Given the case illustrated above, the new S/N numbers in this instance would be 101, 102, etc. Make sure that the PWB vendor is informed and understands that the PWBs in question are being rebuilt.

4.6 Coupons

The use of coupons shall constitute one of the primary ways for establishing the quality of PWBs. The coupon set called out in Table 3.6-3 shall be adhered to, both by type and number. The smallest applicable board hole size shall be used for the A and B coupons, that is, the coupon set shall reflect the specific finished PWB characteristics. It will be noted that some of the coupons are for Group B testing (C, E, M, and P) and some are for internal process control at the PWB facility (A, B, G, and M). Of all the coupons, the ones most useful for evaluating the quality of the PWB are the A and B coupons.

Note: The PWB manufacturer supplies the artwork for the coupons at the time that the Gerber files are photoplotted at the vendor's facility.

4.6.1 A and B Coupons. The principal coupons used by JPL QA for evaluating PWB quality are the A and B coupons. These coupons contain plated-through-holes (PTHs), and they are processed along with the PWBs on the panel as it experiences the various manufacturing processes. The PTHs in these coupons shall be representative of the actual PTHs found in the PWBs themselves. At a minimum, three microsections ("buttons") shall be prepared for JPL QA inspection at the PWB vendor's facility. These are:

(1) B (X-Direction) As-Received;

(2) A (X-Direction) Thermal Stress;

(3) B (Y-Direction) Thermal Stress.

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The holes of the coupons that are to be thermal stressed shall not be filled with any hole fill material, regardless of whether such material is used to fill the vias of the PWBs proper.

These microsections shall constitute one of the deliverable items to JPL. See paragraph 6.2 on page 3.6-54. The vendor shall also submit the results of the coupon evaluations and these shall also constitute one of the deliverable items.

Table 3.6-3 Coupon Type, Identification, and Frequency and Position on Panel

Purpose of Coupon	Identification Letter	Frequency and Position on Panel
Hole solderability	A	Three per panel (two from diagonally opposite corners)
Thermal stress*, plating thickness, and bond strength	B	Two per panel (from diagonally opposite corners)
Plating adhesion and surface solderability (This is for Group B testing)	C	One per panel, position optional, pattern defined by artwork
Moisture and insulation resistance (This is for Group B testing)	E	Two per panel opposite corners
Solder mask adhesion (Done by the PWB vendor for PC purposes)**	G	One per panel with solder mask, location optional
Surface mount solderability (SMT boards only) (Done by the PWB vendor for PC purposes)	M	One per panel, position optional, pattern defined by artwork
Surface mount bond strength (SMT boards only) (Not always run; not necessary if misrun)	N	One per panel, position optional, pattern defined by artwork
Copper peel strength (This is for Group B testing)	P	One per panel, position optional, pattern defined by artwork

* The microsectioning after thermal stress shall be conducted following IPC-A-600, Rev. E, Acceptability of Printed Boards, Internally Observable Characteristics

** PC = process control.

Note: As a double check, it is recommended that microsectioning be performed on a periodic basis at JPL (the Failure Analysis Laboratory at JPL can perform this function) to validate the results of the PWB manufacturer's microsectioning results.

Note: If the lot size is sufficient (lot size ≥ 5), the sacrifice of an actual PWB to determine the above characteristics would be highly advantageous.

4.7 Material Identification and Specification

For material identification and material designations, IPC-4101 (1997), *"Specification for Base Materials for Rigid and Multilayer Printed Boards,"* shall be followed. Since

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this document employs metric units, English units shall be given in brackets following the metric units. For example, a polyimide copper clad core 0.008" (0.2 mm) having 1 oz./ft^2 copper on the top side and 1/2 oz./ft^2 copper on the bottom side is to be designated using the following convention: L 41 0200 [0.008"] C1/CH B B. Consult IPC-4101 for further details.

Note: As of February, 1998, Mil-S-13949, *"Sheet, Printed Wiring Board, General Specification for,"* has been discontinued and is no longer supported.

4.7.1 Abbreviations. The following abbreviations are pertinent to the above specification.

L = laminate;

P = prepreg;

B (1st B) = thickness tolerance class (can be A or B; use B unless a more stringent requirement is needed);

B (2nd B) = surface quality class (can be A or B; use B unless a more stringent requirement is needed).

4.7.2 Examples of Common Material Callouts. The following give several common callouts that the designer may desire in specifying materials. For further details, consult IPC-4101.

- L 24 = sheet 24 in IPC-4101, which is standard FR-4 epoxy laminate reinforced with woven E-glass and having a T_g between 150°C to 200°C.
- P 24 = sheet 24 in IPC-4101, which is standard FR-4 epoxy prepreg reinforced with woven E-glass and having a T_g between 150°C to 200°C.
- L 40 = sheet 40 in IPC-4101, which is standard polyimide laminate reinforced with woven E-glass and having a minimum T_g of 200°C.
- P 40 = sheet 40 in IPC-4101, which is standard polyimide prepreg reinforced with woven E-glass and having a minimum T_g of 200°C.
- L 41 = sheet 41 in IPC-4101, which is standard polyimide laminate reinforced with woven E-glass and having a minimum T_g of 250°C.
- P 41 = sheet 41 in IPC-4101, which is standard polyimide prepreg reinforced with woven E-glass and having a minimum T_g of 250°C.

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- L 42 = sheet 42 in IPC-4101, which is standard polyimide laminate reinforced with woven E-glass and having a T_g of 200°C-250°C.
- P 42 = sheet 42 in IPC-4101, which is standard polyimide prepreg reinforced with woven E-glass and having a T_g of 200°C-250°C.
- L 50 = sheet 50 in IPC-4101, which is modified epoxy laminate reinforced with woven Aramid fibers (Thermount) and having a minimum T_g of 135-190°C.
- P 50 = sheet 50 in IPC-4101, which is modified epoxy prepreg reinforced with woven Aramid fibers (Thermount) and having a minimum T_g of 135-190°C.
- L 53 = sheet 53 in IPC-4101, which is standard polyimide laminate reinforced with non-woven Aramid fibers (Thermount) and having a minimum T_g of 220°C.
- P 53 = sheet 53 in IPC-4101, which is standard polyimide prepreg reinforced with non-woven Aramid fibers (Thermount) and having a minimum T_g of 220°C.

4.7.3 Laminate/Prepreg Material Choice. The laminate/prepreg material choice for all flight PWBs, EM PWBs, and critical ground support equipment PWBs shall be polyimide reinforced E-glass copper clad laminate and polyimide reinforced E-glass prepreg for all single-sided, double-sided, and multilayer PWBs. Epoxy reinforced E-glass (FR-4) copper clad laminate and epoxy reinforced E-glass (FR-4) prepreg is suitable for test boards and standard ground support equipment. Polyimide has superior properties to FR-4 material, particularly because it has a higher T_g and a reduced CTE-Z. These properties afford it to better withstand thermal excursions, both during service operating temperatures and assembly rework to avoid lifted lands. See Table 3.6-4.

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Table 3.6-4 Tg and CTE-Z of Three Resin Systems

Resin System	T_g °C	CTE-Z 10^{-6} in/in/°C (ppm)	Er*	WA %†
Polyimide	200-250	50	4.1	0.43
FR-4 (difunctional)	125	85	4.4	0.14
FR-4 (multifunctional)	170	70	4.4	0.13

* Er = dielectric constant relative to vacuum.

† WA = water absorption as a percent.

Note: The T_g (glass transition temperature) and the CTE-Z (coefficient of thermal expansion-Z axis) are two of the most critical properties of the PWB resin system. The T_g is that temperature at which the resin system making up the PWB loses its rigidity and becomes more rubber-like; its electrical and mechanical properties are also seriously degraded. Resin systems with higher T_gs are favored. See Table 3.6-4.

Note: The CTE-Z refers to the expansion of the resin system in the unrestrained direction due to thermal excursion. Resin systems with lower CTE-Zs are favored. See Table 3.6-4.

Note: Polyimide tends to absorb more water than epoxy. For this reason, it must be baked prior to certain processes to rid it of moisture.

4.8 Design Rules

4.8.1 Materials. Specific material issues:

- Constraining core material;
- Prohibition of Copper-Invar-Copper (CIC) or Copper-Molybdenum-Copper (CMC);
- Backing board.

4.8.1.1 Constraining Core Material. If a constraining core material is used, it shall be of a symmetrical construction with the constraining material in the center.

4.8.1.2 Copper-Invar-Copper and Copper-Molybdenum-Copper Prohibition. The use of Copper-Invar-Copper (CIC) or Copper-Molybdenum-Copper (CMC) is prohibited on all PWBs.

4.8.1.3 Backing Board. A backing board is also known as an insulation board. If a backing board is used, it shall be called out on the fabrication drawing. Regarding the installation of a backing board, there are two different installation procedures that must be distinguished on the drawing: (1) If backing board has no terminals to be installed, the PWB manufacturer normally installs the backing board. (2) If the backing board is to

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have terminals installed, JPL personnel will install both the backing board and the terminals.

The designer shall specify on the fabrication drawing which of the two procedures is to be followed. If case (1) is to be followed, the drawing number stands as is. If case (2) is to be followed, the drawing number must make use of a hyphenated number indicating that the PWB manufacturer is not responsible for the fabrication of everything on the drawing. For example, the drawing number could be 101XXXXX-501. Refer to JPL-STD-00001, *"Drafting Manual,"* Rev. C.

4.8.1.4 Backing Board Installed by the PWB Manufacturer. If the PWB manufacturer installs the backing board, the backing board material shall be of the same type as the PWB, e.g., if the PWB is polyimide reinforced E-glass, the backing board shall also be polyimide reinforced E-glass. Generally a double-sided copper clad 0.008 inch core is used. The PWB manufacturer etches off the copper and laminates the resulting bare core to the PWB using prepreg of the same resin type as the PWB and backing board.

4.8.1.5 Backing Board Installed at JPL. If the backing board is installed at JPL, the terminals are swaged into place. The bottom of the terminal holes are filled with Eccobond 55/9, and in addition, any counterbored holes are filled with Eccobond 55/9. The backing board is also bonded to the PWB using Eccobond 55/9.

4.8.2 PTHs and Vias. There are several important considerations regarding plated through holes (PTHs) and vias: pad size, clearance from ground and voltage planes, copper plating, unused pads, PTH-via fill, tented vias (not allowed), etchback, buried and blind vias, PTH connection restriction in the case of terminals.

4.8.2.1 Pad Size. The formula for calculating minimum pad size is:

$$PAD_{min} = FHS_{nom} + 2ar + FA$$

where:

FHS_{nom} = nominal finished hole size
ar = minimum annular ring allowed
FA = fabrication allowance.

See paragraph 3.1.1.2, "Design Rules" on page 3.6-9 above for an example.

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Note: Different PWB facilities will have different FAs. It would be a good idea to consult with the PWB Process Engineer if there are any questions regarding the FA to be used.

4.8.2.2 Pad Shape. If feasible, the pad shape on the inner layers shall be that of a teardrop. This helps improve the reliability of the PTH.

4.8.2.3 Hole Size Tolerance. The size specified for a hole shall be for the finished hole. Unless otherwise specified on the fabrication drawing, the hole size tolerance shall be ± 0.003 inch.

4.8.2.4 Clearance from Ground and Voltage Planes. Plated through holes shall have a minimum of 0.009 inch (0.23 mm) clearance from all ground and voltage planes.

4.8.2.5 Annular Ring. IPC-2221 for Class 3 PWBs shall be allowed for PTH vias (see 9.1.2 and Table 9.2 in IPC-2221).

4.8.2.5.1 *Annular Ring for PTHs Used for Component Leads.* For PTHs used for component through-holes (e.g., connectors) the external annular ring shall be a minimum of 0.005 inches (0.128 mm) and the internal annular ring shall be a minimum of 0.002 inch (0.051 mm). PTHs to be used as component through-holes shall be clearly called out in the drawing hole schedule.

4.8.2.6 Copper Plating. Copper plating on the walls of plated through holes and plated vias shall be 0.0015 inch (0.038 mm) nominal with no single reading less than 0.001 inch (0.025 mm). See Figure 3.6-8.

4.8.2.7 Unused Pads. There shall be no electrically and/or mechanically unused pads on any of the internal layers. Isolated pads used for mechanical support should not be removed, but the drawing should indicate that such pads are present.

4.8.2.8 PTH-Via Fill. PWBs that will be mounted to a backing board shall have all empty PTH vias filled with one of the materials designated in Table 3.6-5. If the PTH vias are unobstructed and can easily be cleaned during the assembly cleaning process, via hole fill is optional. If a via hole fill material is used on the PWBs to fill vias, it shall not be used to fill the holes of the coupons that are to be thermal stressed. See paragraph 4.6.1 above.

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Table 3.6-5 Acceptable Via Hole-Fill Material

Hole-fill Material	Manufacturer	Distributor or Supplier
Hysol 1C (2-part epoxy)	Dexter Corp. Seabrook, NH (800) 767-8786	K.R. Anderson Santa Ana, CA (714) 549-1343
Armstrong C7/W (2-part epoxy)	Resin Technology South Easton, MA (508) 230-8070	Ellsworth Adhesive Systems Tustin, CA (800) 888-0698
Eccobond 285 (2-part epoxy)	Emerson & Cuming Billerica, MA (978) 436-9700	Ablestik Laboratories Rancho Dominguez, CA (310) 764-4800
Peters SD 2361 (1-part epoxy)	Lackwerke Peters D-47882 Kempen Germany	Electrochemicals Inc. Maple Plain, MN 55359 (800) 321-9050
Peters PP 2795 (1-part epoxy) white	Lackwerke Peters D-47882 Kempen Germany	Electrochemicals Inc. Maple Plain, MN 55359 (800) 321-9050
Peters PP 2795-SD (1-part epoxy) grey	Lackwerke Peters D-47882 Kempen Germany	Electrochemicals Inc. Maple Plain, MN 55359 (800) 321-9050
B-stage resin of approximately the same composition as that of the board. If this does not completely fill the holes, one of the above two materials shall be used to finish the fill.	N/A	N/A

4.8.2.9 Tented Vias. Tented vias shall not be allowed. All blind and/or buried vias shall be filled with one of the materials designated in Table 3.6-5.

4.8.2.10 Etchback. There shall be etchback between 0.0002-0.001 inch (0.005-0.026 mm); 0.0005 (0.013 mm) inch is preferred. Figure 3.6-8 on page 3.6-45 displays a plated through hole showing acceptable etchback and perfect layer-to-layer registration. However, regardless of the amount of etchback achieved, there shall be no separation between the inner layer copper and the plated through hole copper after thermal stress. Appropriate microsections shall be examined to ensure that this is the case.

Note: Polyimide is difficult to ecthback.

Note: Etchback is defined as the controlled removal of all components of the base material (glass and resin) by a suitable process, e.g., plasma, on the side walls of the holes prior to plating to expose additional conductor areas.

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Note: Negative etchback is defined as the process in which inner conductor material is recessed relative to the surrounding base material.

4.8.2.11 Negative Etchback. Negative etchback of the copper shall be prohibited.

4.8.2.12 Buried and Blind Vias. PWBs with buried and blind vias shall be designed such that buried and blind vias shall be produced by sequential lamination techniques. See paragraph 4.8.2.9 above.

4.8.2.13 Through Hole Connection Restriction. Through holes (unplated) used for terminal mounting shall not have internal PWB connections.

4.8.3 Non-Plated Through Holes. Non-plated through holes shall have 0.015 inch (0.038 mm) clearance from conductors and all other conductor elements, including PTHs. Non-plated through holes shall be kept at 0.050 inch (1.26 mm) minimum from the edges of the board.

4.8.4 Antipads in the Plane Layers. To ensure sufficient isolation of the internal plane layers, when designing antipads in the plane layers, bear in mind this chart:

ANTIPAD SIZE	**EASE OF FABRICATION**
FHS_{nom} + 0.030 inch	PREFERRED
FHS_{nom} + 0.026 inch	STANDARD
FHS_{nom} + 0.022 inch	ADVANCED
FHS_{nom} + 0.014 inch	VERY ADVANCED (some PWB facilities may not be able to do this)

Note: An antipad is also referred to as a clearance from the plated through hole to the internal plane.

Also remember that if the finished hole size is specified as 0.018 ± 0.003 inch, then the calculated FHS_{nom} will be 0.018 inch. However, if the finished hole size is specified as 0.018 + 0.003-0.001 inch, then the calculated FHS_{nom} will be 0.019 inch, not 0.018 inch.

4.8.5 Fiducials for SMT PWBs. All SMT PWBs shall have fiducials on the PWB surface to aid in the placement of components during the SMT assembly process. All fiducials (and tooling holes) shall be placed on an appropriate grid. If the SMT PWB has components on both sides of the board, fiducials shall be placed on both sides of the board.

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Note: A fiducial is a fixed location point on a PWB surface used by a placement machine's vision system to orient itself for accurate component placement. Global fiducials are associated with the PWB surface as a whole. Local fiducials are associated with particular components. See Figure 3.6-1.

4.8.5.1 Global Fiducials. All SMT PWBs shall have three global fiducials on the PWB to ensure accurate placement of components on the PWB surface prior to the solder reflow operation. These three fiducials shall be placed in three of the corners, and each fiducial shall be a 0.040 inch diameter pad (no hole) having a 0.050 inch clearance around it. All global fiducials shall be a minimum of 0.200 inch from the PWB edge.

4.8.5.2 Local Fiducials. For each leaded component on the board surface having a pitch of 0.025 inch or less, there shall be two local fiducials at opposite corners of the component footprint for proper component placement. These local fiducials shall have exactly the same dimensions as the global fiducials.

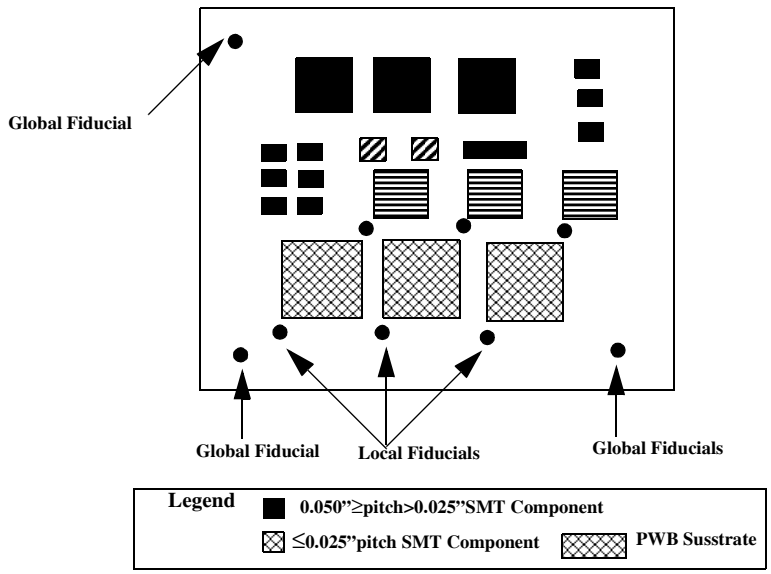

Figure 3.6-1 Global and Local Fiducials Depicted on a Surface Mount PWB

4.8.6 Footprint Patterns. The designer shall consult JPL D-8208, Section 3.5, Surface Mount Technology, as applicable for either SMT or manual assembly. It may also be applicable for the designer to consult JPL D-8208, Section 3.14, Component Mounting/Soldering. In addition, the designer may wish to consult EP517060, *"Design Requirements for*

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Surface Mount Component Footprints on Printed Wiring Boards, Detail Specification for," and CS515520, *"Footprint Requirements for Printed Wiring Boards, Detail Specification for."* The latter document must be used cautiously since portions of it are out of date. Footprint patterns can also be obtained from the various packaging manufacturers' guidelines. Many of these guidelines can be accessed over the Internet or are free from the manufacturer.

4.8.7 Distance of Features to Board Edges and to Mounting Holes. The following pertain to conductive feature spacing to the board edges and to mounting holes.

4.8.7.1 Distance of Features to Edges of Board. All conductors, such as pads, traces, and including ground and power planes, shall be no nearer than 0.030 inch (0.76 mm) to the edges of the board.

4.8.7.2 Distance of Features to Mounting Holes. All conductors, including planes, shall be a minimum of 0.030 inch (0.76 mm) clearance from fastener heads or washers as shown in Figure 3.6-2. All conductors, including ground and power planes, shall be a minimum of 0.030 inch (0.76 mm) from mounting holes.

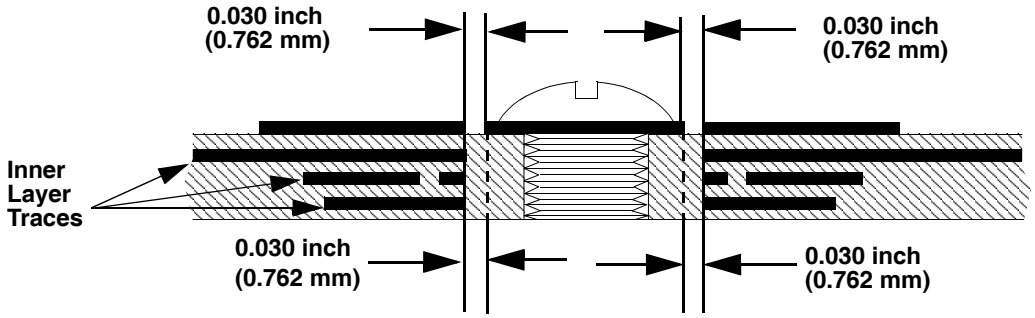

Figure 3.6-2 Mounting Hole Size

4.8.8 Terminals. Nonplated through-holes shall be designed and installed per the requirements given herein. See paragraph 4.8.2.12, "Buried and Blind Vias" on page 3.6-24. for additional information regarding connection restrictions.

4.8.8.1 Terminal Pad Size. Pads for terminals shall be a minimum diameter of 0.015 inch (0.38 mm) larger than the terminal base.

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4.8.8.2 Terminal Soldering. Terminals shall be soldered to the terminal pad.

4.8.8.3 Hole Size. Holes for mounting terminals shall be 0.004 inch (0.102 mm) larger than the nominal diameter of the terminal shank, with a difference between the minimum and maximum diameter (unilateral tolerance) as provided in Table 3.6-6.

Table 3.6-6 Terminal Hole Unilateral Tolerance

Hole Diameter (inch)	Difference (inch)	Hole Diameter (millimeter; mm)	Difference (millimeter; mm)
Up to 0.032	0.002	Up to 0.81	0.05
0.033 to 0.063	0.003	0.82 to 1.60	0.08
0.064 to 0.188	0.004	1.61 to 4.78	0.10

4.8.8.4 Counterbored Holes. When used to facilitate terminal installation, counterbored holes shall be located a minimum distance of 0.0125 inch (0.32 mm) from all conductive elements, including board edges, plated holes, fasteners, and metal identifiers.

4.8.8.5 Keepout Zones. All counterbored holes shall have a concentric, cylindrical keepout zone 0.025 inch (0.64 mm) greater in diameter than the counterbore, with no encroachment of inner layers or conductors. See Figure 3.6-3.

4.8.8.6 Orientation Tolerance. Terminals shall be oriented within ±10° of the specified orientation.

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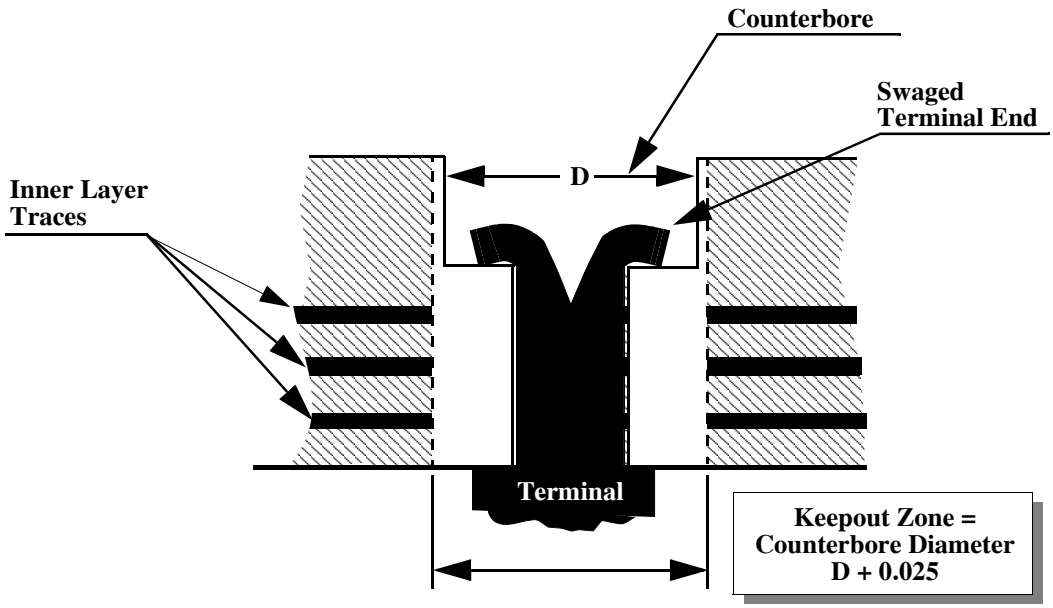

Figure 3.6-3 Keepout Zone

4.8.9 Surface Finish. Hot air solder leveling (HASL) shall be the preferred method.

4.8.9.1 Surface Finish for Soldering. Immersion or electroless tin, nickel, or gold shall not be used as a surface finish for soldering.

4.8.9.2 Surface Finish. The method of surface finish on SMT pads or PTHs shall be specified on the drawing.

4.8.9.3 Tin-lead Plate and Fuse. Tin-lead plate and fuse is not recommended. It is prohibited for all surface mount boards, and if used, shall be used in conjunction with trace widths/spacings greater than 0.010 inch and components having a pitch equal to or greater than 0.050 inch. If tin-lead plate and fuse is used, the plating thickness of the tin-lead shall be 0.0003-0.001 inch prior to fusing.

4.8.9.4 Solder Coat and Hot Air Leveling. Solder coating and hot air leveling (HASL) shall be applied after the application of solder mask over bare copper (SMOBC).

4.8.9.5 Final Solder Finish. Solder applied via HASL shall meet IPC Class 3 final finish per IPC-6012, Table 3-2.

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4.8.9.6 Hydrosqueegee Prohibition. The hydrosqueegee coating or leveling process shall not be used for flight PWBs.

4.8.10 Solder Mask. There are several important considerations regarding solder mask:

- Solder mask materials;
- Solder mask artwork;
- Solder mask/feature locations;
- Cleaning prior to solder mask application;
- Prohibition against tin-lead under the solder mask.

4.8.10.1 Solder Mask Materials. Solder mask materials shall be selected with one of the materials designated in Table 3.6-7. However, bear in mind that a particular application, e.g., the proximity of the electronic box to S/C optics, may make one choice of solder mask more acceptable. If there is a question, consult with the PWB Process Engineer.

4.8.10.2 Solder Mask/Feature Location. Solder mask shall be no nearer than 0.002 inch (0.050 mm) to any feature.

4.8.10.3 Cleaning Prior to Solder Mask Application. All PWBs shall be cleaned prior to solder mask application. The document governing this activity shall be ANSI/IPC-SM-839, *Pre and Post Solder Mask Application Cleaning Guidelines*.

4.8.10.4 Prohibition of Tin-Lead under Solder Mask. There shall be no tin-lead under the solder mask.

4.8.10.5 Solder Mask Dams between Mounting Lands. If a solder mask dam between SMT component mounting pads is desired to prevent solder bridging, a minimum of 0.004 inch of solder mask + 0.003 inch clearance on each side must be allowed. See Figure 3.6-4. For round BGA mounting pads, only 0.003 of solder mask + 0.003 inch on each side must be allowed. See Figure 3.6-4.

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Table 3.6-7 Acceptable Solder Mask Materials

Material	Manufacturer	Distributor or Supplier
SR1000 (1-part epoxy) Screenable SM	Polyclad/Enthone (Cookson) Londonderry, NH (800) 366-1185	K.R. Anderson Santa Ana, CA (714) 549-1343
SR2020 (2-part epoxy) Screenable SM	Polyclad/Enthone (Cookson) Londonderry, NH (800) 366-1185	K.R. Anderson Santa Ana, CA (714) 549-1343
Dynamask KM (formerly DynaChem KM) (epoxy-acrylic) Dry film SM	Shipley Ronal Tustin, CA (714) 730-4200	Call Shipley-Ronal Order Entry (714) 730-4200
Vacrel 8140 Dry film SM	DuPont iTechnologies Research Triangle Park, NC (800) 243-2143	Circuit Image Systems Orange, CA (800) 640-2184
Probimer 52 LPI SM	Vantico Inc. Los Angeles, CA (818) 265-7160	Vantico Inc. Customer Service (818) 265-7193
Carapace EMP110 LPI SM (UV bump required)	Electra Polymers Roughway Mill TN11 9SG England UK	Electra Polymers 2914 East Katella Ave. Suite 208 Orange, CA (714) 744-8394
PSR-4000 series LPI SM	Taiyo America, Inc. Carson City, NV (775) 885-9959	Same as manufacturer

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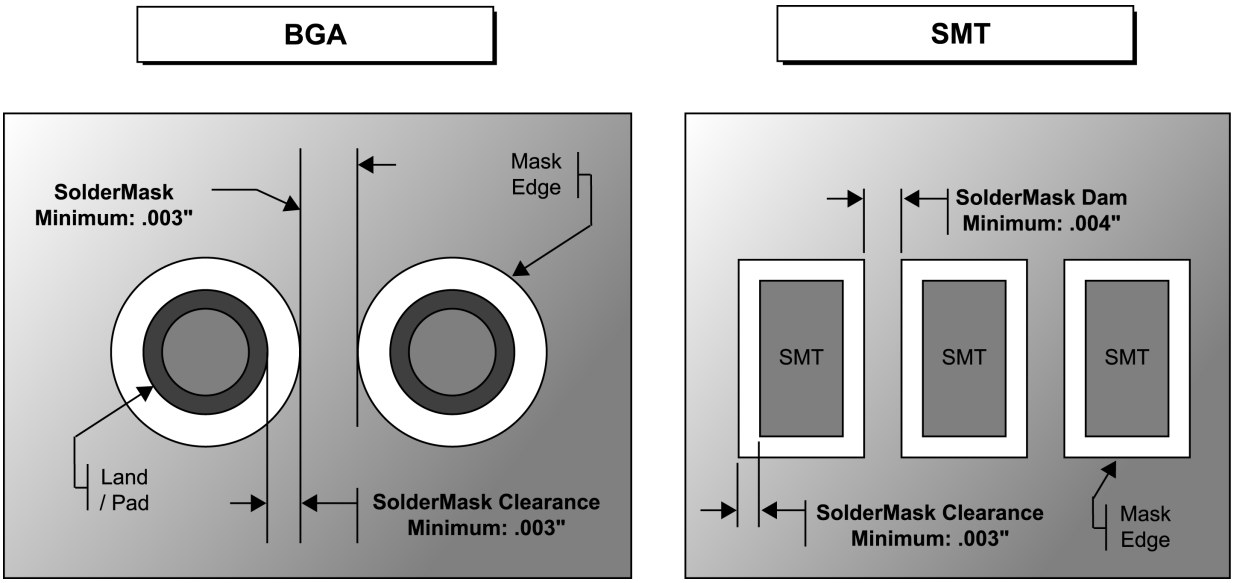

Figure 3.6-4 Solder Mask

4.8.11 Legend Marking Materials. Legend marking (silk screen nomenclature) materials are designated in Table 3.6-8. The required color shall be white unless specified differently on the fabrication drawing.

Table 3.6-8 Acceptable Legend Marking Material

Material	Manufacturer	Distributor or Supplier
Hysol M-Series/Catalyst 20/A Color: white (M-9-N) (2-part epoxy permanent marking ink) (Formerly Wornowink)	Polyclad/Enthone (Cookson) Londonderry, NH (800) 366-1185	K.R. Anderson Santa Ana, CA (714) 549-1343

4.8.11.1 Legend Marking/Feature Location. Legend marking shall be no nearer than 0.007 inch (0.178 mm) to any feature.

4.8.12 Dielectric Separation between Adjacent Conductive Layers. Separation between conductors on adjacent layers shall be 0.0035 inch minimum and consist of a minimum of two plies of prepreg.

4.8.13 Multilayer Board Construction. If the printed wiring board is a multilayer construction, the following rules shall pertain.

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4.8.13.1 Foil Construction versus Core Construction. Two different constructions are used to manufacturing a multilayer board (MLB). These are:

(1) Foil construction;

(2) Core construction.

See Figure 3.6-5 below which illustrates both construction types for an 8-layer MLB. There are advantages and disadvantages of each construction although generally registration control is better with the foil construction.

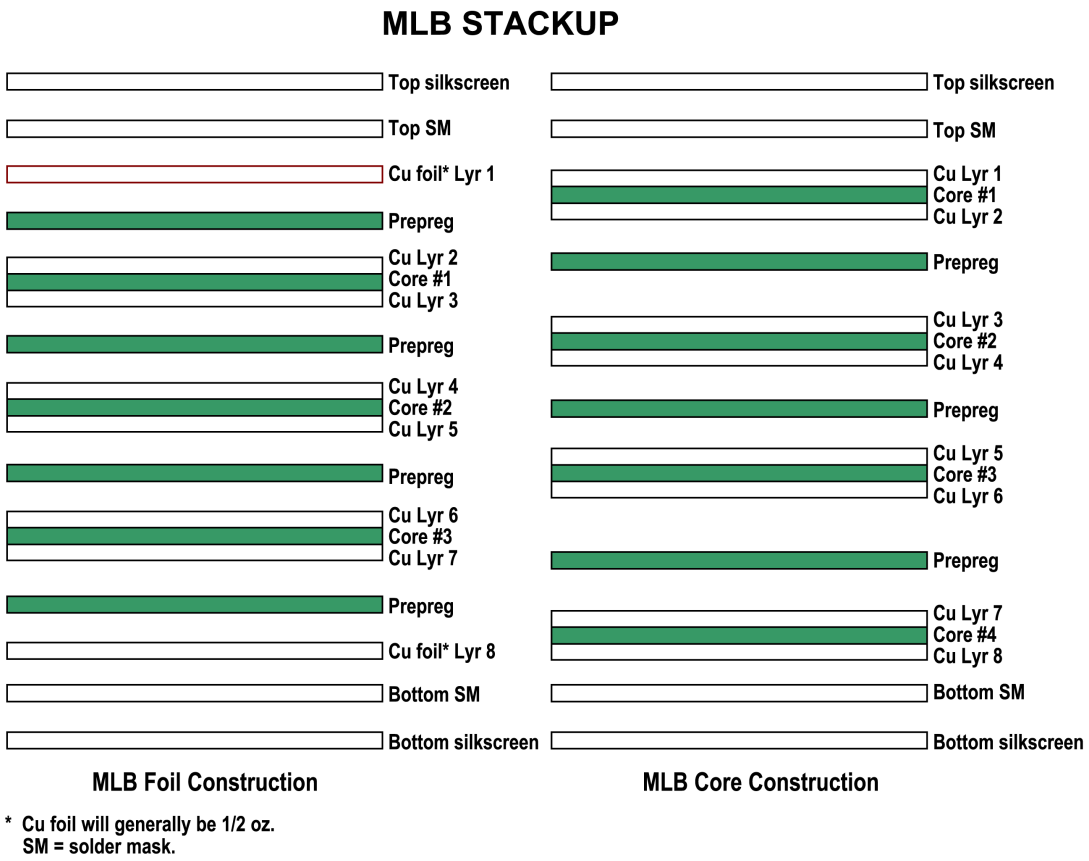

Figure 3.6-5 Foil Construction versus Core Construction.

Figure 3.6-8 on page 3.6-45 shows a plated through hole in an 8-layer MLB having perfect layer-to-layer registration. It also shows etchback (see 4.8.2.10) and copper

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plating (see 4.8.2.6) that exhibits the normal pattern of heavier plating at the two ends of the hole and less heavy plating in the middle. Figure 3.6-9 on page 3.6-46 shows a plated through hole showing layer-to-layer misregistration.

4.8.13.2 Multilayer Board Thickness. To estimate the thickness of a MLB, the following heuristic guidelines can be given.

Assume each dielectric layer to be 0.005 inch. This includes both core and prepreg dielectric. The following copper thicknesses can be used for estimation purposes:

- 1/2 oz. Cu = 0.0007 inch;
- 1 oz. Cu = 0.0014 inch;
- 2 oz. Cu = 0.0028 inch.

Plating on the top and bottom layers will add an extra 0.005 inch roughly. Solder mask on the top and bottom layers will add an extra 0.002 inch roughly. Therefore, for the MLB depicted in Figure 3.6-5 above, assuming that the top and bottom copper layers are 1/2 oz. copper and all other copper layers are 1 oz. copper, the thickness as calculated from the above rules is:

Thickness = 0.002 (SM) + 0.005 (plating) + 7 (dielectrics) x 0.005 +
6 (1 oz. Cu) x 0.0014 + 2(1/2 oz. Cu) x 0.0007 = 0.052 inch

If a tighter thickness is needed, discuss with the PWB Process Engineer if the dielectric layer can be taken to be 0.004 inch rather than 0.005 inch.

4.8.13.3 Multilayer Board Thickness Tolerance. The overall thickness tolerance should be +/-10% and shall be expressed in inch on the drawing. For the MLB illustrated above, the fabrication drawing shall read 0.052 +/-0.005.

4.8.13.4 Symmetrical Stackup. When designing the stackup, the designer should be cognizant that the materials utilized in MLB constructions are subject to shrinkages and material distortions as the copper is etched off the layers. The more copper that is removed from a layer, the more material shrinkage is experienced due to the relief of stresses pent up within the copper clad laminate material. Therefore, a core that has signal-signal (S-S) will shrink much more (relatively speaking) that a core that has plane-plane (P-P).

As an example, assume the stackup is as follows for a 10-layer MLB (assuming foil construction):

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S (lyr 1 = outer layer)

prepreg

S-S (lyrs 2-3 = inner layer)

prepreg

S-S (lyrs 4-5 = inner layer)

prepreg

S-S (lyrs 6-7 = inner layer)

prepreg

P-P (lyrs 8-9 = inner layer)

prepreg

S (lyr 10 = outer layer)

Of the four inner layers, the three S-S layers will shrink at pretty much the same rate; whereas the P-P layer will shrink much less due to there being much more copper on this inner layer. Hence, it will subsequently be harder to hold adequate registration during the drilling and lamination processes.

A much more symmetrical construction would be the following:

S (lyr 1 = outer layer)

prepreg

P-S (lyrs 2-3 = inner layer)

prepreg

S-S (lyrs 4-5 = inner layer)

prepreg

S-S (lyrs 6-7 = inner layer)

prepreg

S-P (lyrs 8-9 = inner layer)

prepreg

S (lyr 10 = outer layer)

Consult with the PWB Process Engineer if there is a question.

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4.8.14 Controlled Emissions. The following points are made regarding controlling the RF emissions from signal and power and ground layers. See Figure 3.6-6.

- The most effective way of controlling emissions from the signal traces is to locate them as closely as possible to their reference planes.
- The most effective way of controlling emissions from the reference planes is to locate them as closely as possible to each other.

Since both of these recommendations cannot always be realized simultaneously, the first takes precedence over the second. Controlling emissions from the reference planes, if they cannot be located as close as possible, can be accomplished by using by-pass capacitors.

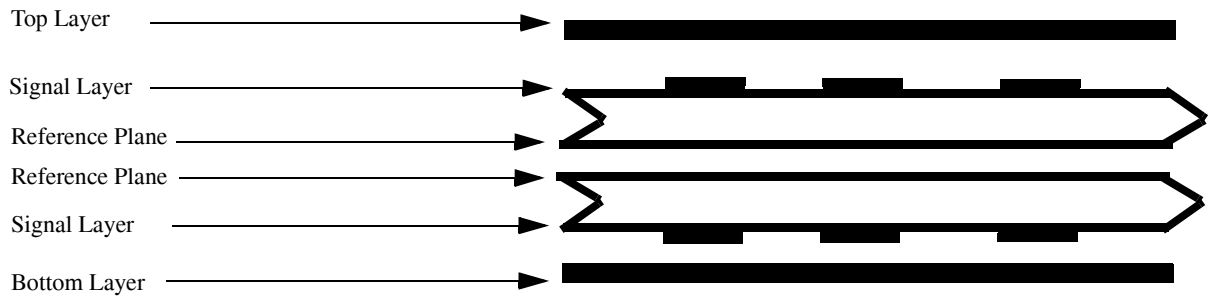

Figure 3.6-6 MLB Showing Signal Layers and Reference Planes

4.8.15 Controlled Impedance MLB Construction. As frequencies increase, traces increasingly take on the properties of transmission lines. Under these circumstances, it is important to understand the properties of controlled impedance (Z_o).

4.8.15.1 Controlled Impedance PWBs-Design. The four types of controlled impedance boards are microstrip, embedded microstrip, stripline, and dual stripline. For design information, refer to Section 6.4, pp. 40-43, of IPC-2221, *"Generic Standard on Printed Board Design,"* for further details.

4.8.15.2 Controlled Impedance PWBs-Fabrication. There are several important considerations to keep in mind regarding the successful fabrication of controlled impedance MLBs. Below are four parameters that are critical and must be carefully controlled (also see Figure 3.6-7 below):

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- Dielectric constant (Er, εr or DK). This is a function of the choice of material used. Some materials, such as polytetrafluoroethylene (PTFE: Teflon, Duroid, etc.) have low Ers. For example, PTFE has a dielectric constant somewhere in the range of 2.5. The Er of polyimide is about 4.0. However, PTFE is not the easiest material to process. This parameter is based on the choice of materials. Unless specified otherwise on the drawing, polymide is the material to be used for flight-controlled impedance MLBs.
- The width of the trace, w. This is a critical feature of a controlled impedance board. The etching process is critical in keeping the side walls of the trace as straight as possible. A precision spray etching machine is critical. The etch factor that the fabricator can achieve is more controllable during the etch process if a lighter weight copper is used, e.g., 1/2 oz., 1/4 oz., etc. This parameter is subject to control by the PWB fabricator.
- The thickness of the trace, t. It is also important to control the thickness. If the weight of copper is too thin, in the inner layers it may become buried by the prepreg material. This parameter is subject to control by the PWB fabricator.
- The distance of the bottom of the trace to the reference plane, h. To control h, make sure that the signal trace and its corresponding reference plane are located on the same piece of core material. This parameter is subject to control by the PWB fabricator.

Given what was said above about the four critical parameters, the following can be said about each one's affect on the controlled impedance:

- Increase the dielectric constant, Er (or DK), will decrease the controlled impedance;
- Increase the trace width, w, will decrease the controlled impedance;
- Increase the trace thickness, t, will decrease the controlled impedance;
- Decrease the distance of the bottom of the trace to the reference plane, h, will decrease the controlled impedance.

In general, the nominal dielectric constant, Er, of the material is used for the value of Er in making controlled impedance calculations. See Table 3.6-4 as a reference. For the

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value of w, as a first pass, use the value that is given in the drawing. The trace thickness, t, depends on the copper weight used. However, remove 0.0002 inch due to processing.

- 1/2 oz. Cu = 0.0007 - 0.0002 = 0.0005 inch;
- 1 oz. Cu = 0.0014 - 0.0002 = 0.0012 inch;
- 2 oz. Cu = 0.0028 - 0.0002 = 0.0026 inch.

The designer should bear in mind, however, that the formulas for calculating the controlled impedance (Z_o) are complicated, so a good software program for calculating controlled impedance should be used.

4.8.15.3 Controlled Impedance PWBs-Testing. Make sure that the fabricator has time domain reflectometry (TDR) testing capabilities to test the achieved impedance. This will help in adjusting the process parameters to achieve the desired controlled impedance. A suitable coupon for controlled impedance shall be used when the PWB is a controlled impedance PWB. The PWB vendor shall supply this coupon and position it on a suitable place on the panel during PWB manufacture.

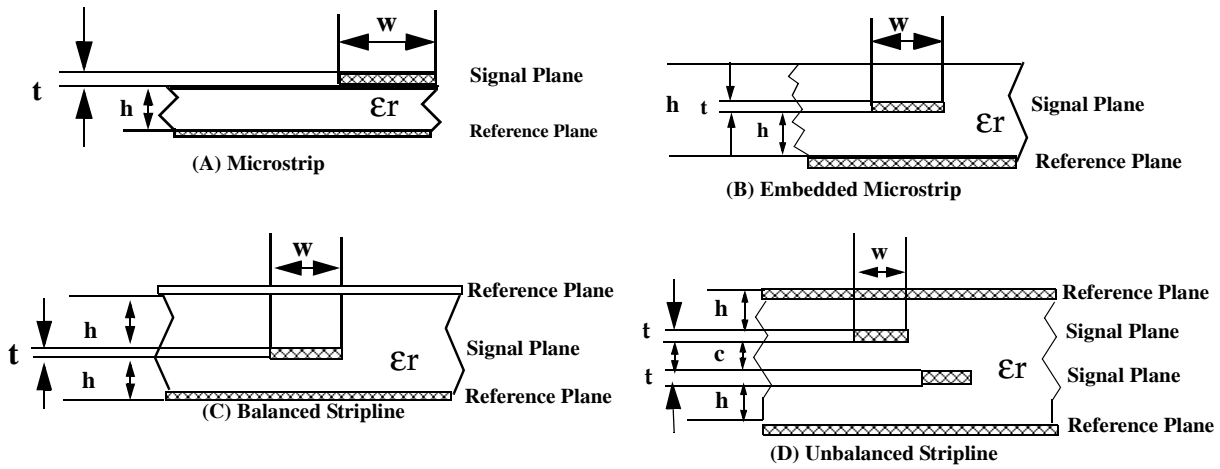

Figure 3.6-7 Transmission Line Printed Board Constructions: w, t, and h

4.9 Fabrication Drawing

4.9.1 Fabrication Drawing. The following items shall be found on the fabrication drawing.

- Fabrication drawing notes (see paragraph 4.9.1.1 below).

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- The hole block, including all plated and unplated holes. The hole block should also give tolerances for all holes. The sizes specified shall be for the finished hole. The hole chart shall also specify which holes are to be filled, if any. The hole block shall also clearly specifiy what holes are blind holes and what holes are buried holes, if there are such holes in the PWB in question.
- A drawing depicting the board dimensions, including the overall thickness and thickness tolerance. All dimensions and tolerances shall be per ANSI Y14.5.
- If an MLB, a layer-by-layer stackup drawing shall be depicted, including an insulation board (if any). The stackup shall also depict the solder mask layer(s) and the silkscreen layer(s). A symmetrical layer build-up is highly preferred. See Figure 3.6-5 and paragraph 4.8.13.4.
- The fabrication drawing shall have the file extensions associated with each layer, including silkscreen and solder mask, used as labels for the stackup layers along with the layer names.
- The fabrication drawing shall locate the origin of the coordinate system and be consistent with the netlist. The coordinate system shall be shown on the drawing.
- Any other special features.

4.9.1.1 Fabrication Drawing Notes. At minimum, the fabrication drawing notes shall contain the following:

- The type of PWB shall be called out on the fabrication drawing. See 1.3 above.
- PWB laminate material, including both cores and prepregs. The weight of copper shall be specified for all core materials called out. See paragraph 4.7 above.
- Minimum trace width/spacings (given for quotation purposes).
- Surface finish. If any surface finish other than HASL is to be used, it shall be called out on the drawing. See paragraph 4.8.9.
- Solder mask callout. See paragraph 4.8.10 above. If solder mask is used, no solder shall be permitted under the solder mask.

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- Legend ink. See paragraph 4.8.11 above.
- Hole fill. See paragraph 4.8.2.8 above.
- PWB identification. Identify all boards per paragraph 4.5 above.
- Maximum bow and twist shall not exceed 0.75% for SMT boards and 1.0% for all other boards.
- Just prior to the application of solder mask, one board per lot shall be cleaned and tested for cleanliness using a suitable ionic contamination tester and the result documented. The ionic contamination level shall not exceed 10 micrograms per square inch (10 µg/in^2). Each side of the board contributes to the total area in square inches. If the board fails, the entire lot shall be recleaned, and the test repeated until the board passes the test. See paragraph 4.8.10.3 above and paragraphs 5.3.10 and 5.3.10.1 below.
- All boards shall be packaged for shipment following paragraph 5.3.19 below.

See Table 3.6-9 for an example of fabrication drawing notes. These notes are for guidance only. The particular PWB under consideration may require a different set of notes.

Table 3.6-9 Example of Fabrication Drawing Notes

NOTES: UNLESS OTHERWISE SPECIFIED	Applicable Paragraph Number(s) in Section 3.6
1. ALL SECTIONS AND SUBSECTIONS REFERRED TO IN THIS DOCUMENT ARE PER JPL SPECIFICATION D-8208.	N/A
2. THIS DOCUMENT AND RELATED ARTWORK ARE COMPUTER GENERATED. CHANGES ARE TO BE PERFORMED ON THE ORIGINAL DATABASE ON FILE IN SECTION 349.	N/A
3. FABRICATE PRINTED WIRING BOARD PER SECTION 3.6.	1.2
4. FOIL CONSTRUCTION SHALL BE EMPLOYED FOR MULTILAYER CONSTRUCTION.	5.3.6
5. COPPER PLATING IN HOLES SHALL BE 0.0015 INCH NOMINAL THICKNESS WITH NO SINGLE READING LESS THAN 0.001 INCH.	4.8.2.6; 5.3.9.1
6. NEGATIVE ETCHBACK SHALL BE PROHIBITED.	4.8.2.11; 5.3.9.3
7. POSITIVE ETCHBACK SHALL BE 0.0002-0.002 INCH; 0.0005 INCH IS PREFERRED. PLASMA DESMEAR/ETCHBACK IS THE PREFERRED METHOD.	4.8.2.10; 5.3.9.2
8. LAYER-TO-LAYER REGISTRATION SHALL NOT EXCEED 0.010 INCH ON MULTILAYER PWBs 10 LAYERS OR LESS, AND IT SHALL NOT EXCEED 0.010 INCH + 0.001 INCH FOR EACH ADDITIONAL LAYER OVER 10. FOR EXAMPLE, IT SHALL NOT EXCEED 0.014 INCH FOR A 14 LAYER MULTILAYER PWB.	5.3.6.2

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Table 3.6-9 Example of Fabrication Drawing Notes (Continued)

NOTES: UNLESS OTHERWISE SPECIFIED	Applicable Paragraph Number(s) in Section 3.6
9. THE EXTERNAL ANNULAR RING SHALL BE AT LEAST 0.002 INCH, AND THE INTERNAL ANNULAR RING SHALL BE AT LEAST 0.001 INCH.	4.8.2.5; 5.3.9.4
10. IONIC CONTAMINATION SHALL BE MEASURED ON ONE BOARD PER LOT* DIRECTLY PRIOR TO THE APPLICATION OF SOLDER MASK AND SHALL NOT EXCEED 10 MICROGRAMS PER SQUARE INCHES. TEST DOCUMENTATION SHALL BE DELIVERED WITH THE BOARD. THE BOARD USED FOR IONIC CONTAMINATION TESTING SHALL BE BAKED AT 125 F FOR 20 MINUTES PRIOR TO APPLICATION OF SOLDER MASK	5.3.10.1
11. APPLY ITEM X† SOLDER MASK TO TOP AND BOTTOM OVER BARE COPPER, COMPONENT PADS TO BE FREE FROM BLEEDING OR MISREGISTRATION.	4.8.10.1; 5.3.11
12. AFTER APPLICATION OF SOLDER MASK, APPLY SOLDER COAT OVER BARE COPPER USING HOT AIR LEVELING (HASL). SOLDER THICKNESS AT CREST TO BE 0.00015 TO 0.002 INCH. THERE SHALL BE NO SOLDER UNDERNEATH SOLDER MASK.	4.8.9; 4.8.10.4; 5.3.11; 5.3.12
13. SEPARATION BETWEEN CONDUCTORS ON ADJACENT LAYERS SHALL BE 0.0035 INCHES MINIMUM AND CONSIST OF A MINIMUM TWO PLIES OF PREPREG.	4.8.12; 5.3.6.1
14. LEGEND OVER SOLDER MASK ON BOTH SIDES OF PWB USING HYSOL M-SERIES/CATALYST 20/A WHITE EPOXY INK. LEGEND MARKING SHALL BE NO NEARER THAN 0.005 INCH TO ANY SOLDER PAD. INK STAMP REVISION LETTER AND SERIAL NUMBER USING HYSOL M-SERIES/CATALYST 20/A WHITE EPOXY INK. CHARACTER HEIGHT SHALL BE 0.050 INCH (MINIMUM).	4.8.11; 4.8.11.1; 5.3.13
15. CONTINUITY AND SHORTS TESTING USING A SUITABLE NETLIST TESTING DEVICE SHALL BE PERFORMED ON EACH PWB, AND THE DOCUMENTATION DELIVERED WITH THE FINISHED PWB. SHORTS TESTING SHALL BE AT A MINIMUM OF 200 VOLTS D.C.	4.4; 4.4.1; 5.3.15
16. THERE SHALL BE A MINIMUM OF TWO COUPON STRIPS FOR EACH PANEL PRODUCED. EACH STRIP SHALL AT A MINIMUM CONSIST OF A AND B COUPONS, AND EACH STRIP SHALL BE PLACED AT ONE OF THE CORNERS DIAGONALLY ACROSS FROM THE OTHER STRIP AND AT RIGHT ANGLES FROM THE OTHER STRIP AND BE LOCATED NO MORE THAN 0.250 INCH FROM A BOARD ON THE PANEL.	4.6; 4.6.1; 5.3.2
17. BOW AND TWIST SHALL NOT EXCEED 0.75%.	5.3.17
18. MATERIALS USED SHALL BE TRACEABLE TO THE MANUFACTURER'S LOT. CERTIFICATION SHALL BE SUPPLIED WITH ALL TEST DATA.	6.2

* PWB LOT = A lot consists of those PWBs processed at the same time and under the same conditions. The lot may consist of one panel or several panels.

† ITEM X = One of the acceptable solder mask materials. See Table 3.6-7.

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4.9.1.2 Released Drawing. Prior to the initiation of the PWBs, the master fabrication drawing (often called simply the fab drawing) shall be released. See paragraph 4.10 below.

4.10 Design Output

The following items shall normally constitute the output from the PWB design effort. All electronic files should be zipped together into one ZIP file for convenience of handling and for electronic transmission. This ZIP file shall be placed in the Product Data Management System (PDMS) for all flight hardware.

Note: PDMS is replacing the vellum file service for all new projects. Most older drawings are also being converted into the PDMS.

- A complete set of Gerber files containing a Gerber file for each layer of the PWB. It is the responsibility of the designer to ensure that the file extension outputs of his/her CAD system are used to label the different layers of the stackup on the fabrication drawing. See paragraph 4.9.1.
- Gerber file(s) for the legend to identify reference designators, etc. Legending is also known as silk screening, so these are generally referred to as the silk screen Gerber files. Two are required if the board has legends on both the top side and the bottom side.
- It is preferred that the Gerber files be on the same 0,0 as the IPC-D-356A file.
- Gerber file(s) for solder mask. Two are required if the board is to have solder mask on both the top side and the bottom side.
- If the board is an SMT PWB, Gerber file(s) for the stencil. These are generally referred to as the solder paste Gerber files. Two are required if the board is to have surface mount components on both the top side and the bottom side.
- If hole fill is being done and the holes to be filled are not indicated clearly and unambiguously on the hole chart, then the designer shall supply a fill file.
- It is preferred that a route file be provided. The center of the line shall be used as the board edge. All cutouts and slots should also be part of the route file.

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- An aperture file containing the aperture list. If an extended Gerber RS-274X file is employed in which the aperture shapes are already embedded, this file is then superfluous. It is highly preferred that a Gerber RS-274X file be supplied.
- A drill file containing the drill program. It is preferred that an Excellon 2 Format plus M48 Header file be supplied. There should be a separate drill file for all holes in the PWB. There should be a drill file for all plated through holes, a drill file for non-plated through holes, a drill file for each set of buried vias (if the PWB has these), a drill file for each set of blind vias (if the PWB has these), etc.
- An electronic version of the fabrication drawing in pdf format. For flight hardware, this drawing shall be a reference copy of the released drawing.
- An electronic version of the assembly drawing in pdf format. For flight hardware, this drawing shall be a reference copy of the released drawing.
- A PDMS version of the fabrication drawing shall be available. For flight hardware, this drawing shall be a released drawing. The hardcopy version shall be generated from the computer database.
- A PDMS version of the assembly drawing shall be available. For flight hardware, this drawing shall be a released drawing. The hardcopy version shall be generated from the computer database.
- IPC-D-356A file of the netlist generated directly from the design database. It is the responsibility of the designer to ensure the creation of the IPC-D-356A file. If his/her system does not create this as a normal output, the designer should negotiate with the cognizant engineer to arrange to have this done. See paragraph 4.4.3. Once the IPC-D-356A file has been generated from the design database, it shall not be modified.
- A Read-Me file containing the following:
    - Name of all files with a brief verbal description of each file.
    - Any other pertinent information required to plot the artwork and manufacture the board, including such items as:
        - List of intentional shorts;
        - Special layers identified, such as hole fill layers;

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- Identification of special pads and symbols;
- Comment out test points left open in mask;
- Special grounding situations;
- All exceptions to D-8208.

It shall be the responsibility of the designer to perform design rule checks (DRCs) on the design package before it is released and to perform a final quality check on the design.

5 FABRICATION REQUIREMENTS

The fabrication requirements for all JPL printed wiring boards (PWBs) shall be per the IPC-6011 (1999), "*Generic Performance Specification for Printed Boards.*" Regarding the fabrication requirements for rigid printed wiring boards, the chief document, in addition to IPC-6011, is IPC-6012 (1999), *"Qualification and Performance Specification for Rigid Printed Boards."* Exceptions to these two documents for flight PWBs are detailed in this section.

5.1 Order of Precedence

In the event of a conflict between the procurement document(s), this specification, the fabrication drawing, and/or any other documentation, the following order of precedence shall pertain:

- Purchase Order (P.O.) or Contract with the vendor;
- Master fabrication drawing;
- This specification;
- IPC-6012, *"Qualification and Performance for Rigid Printed Boards;"*
- IPC-6011, *"Generic Performance Specification for Printed Boards."*

5.2 Performance Class

The performance class shall be IPC Class 3, High-Reliability Electronic Products.

5.2.1 Pre-Fabrication Inspection. Travelers may be reviewed and submitted to JPL prior to starting the PWB fabrication. If necessary, plotted artwork films may also be reviewed. The JPL PWB Process Engineer and/or JPL QA will decide if this is necessary.

5.2.2 Board Type. Board Types 1 through 4 shall be acceptable for JPL use. See 1.3 above. The type of PWB and the use will be called out on the fabrication drawing.

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5.3 Fabrication Requirements—Flight PWBs

5.3.1 Acceptance Criteria. ANSI/IPC-A-600E, "Acceptability of Printed Wiring Boards," shall be used as acceptance criteria using Class 3 acceptability level.

5.3.2 Coupons. The necessary coupons shall be plotted on all artworks as appropriate. See 4.6 above. If the PWB is a controlled impedance PWB, the vendor shall supply this coupon and position it on a suitable place on the panel during PWB manufacture. See 4.8.15.3.

5.3.3 Artworks to be Sent to JPL. After the vendor has performed the front-end engineering activities on the Gerber files and the Gerber files have been photoplotted, the artwork inspected, and the production phototools produced, the vendor shall send duplicate top layer artwork film and the top silk screen (legend) artwork film to the PWB Process Engineer at JPL at MS 103-106. If the PWB is an SMT PWB, the vendor shall also include the solder paste artwork film for the top layer and the bottom layer (if applicable). Diazo phototools are acceptable. If the board has components on the bottom side, the vendor shall also send the bottom layer artwork film and the bottom silk screen (legend) artwork film to the PWB Process Engineer at JPL. These artwork films will be used by assembly engineers as an aid in planning the PWB assembly operation.

5.3.4 Panelization. The most expeditious panel size shall be used to build JPL PWBs. The panel size shall take into account the dimensional stability of the material and layer-to-layer registration.

5.3.5 Inner Layer Inspection of MLBs. All inner layers shall be 100% inspected using AO1 prior to the lamination process. This requirement may be waived at the discretion of the PWB Process Engineer and JPL QA. The wainver shall be in written form to the PWB vendor. It is highly preferred that the AO1 machine be CAD-driven. All defective inner layers shall be discarded.

5.3.6 MLB Lamination. Unless otherwise specified on the fabrication drawing, foil constructions shall be allowed. All MLBs shall be symmetrical. For buried and/or blind vias, the MLB shall be built using sequential lamination techniques.

5.3.6.1 Dielectric Separation Between Conductor Layers. Dielectric separation between conductor layers shall be a minimum of 0.0035 inch (0.089 mm) and shall be attained by the use of a minimum of two plies of prepreg.

5.3.6.2 Layer-to-Layer Registration. Layer-to-layer registration shall not exceed 0.010 inch in multilayer PWBs (MLBs) 10 layers or less, and it shall not exceed 0.010 + 0.001 inch for

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each additional layer greater than 10. For example, it shall not exceed 0.014 inch for a 14-layer MLB. This requirement is to be used in conjunction with that of annular ring. See paragraph 5.3.9.4 below. See Figures 3.6-8 and 3.6-9 for examples of layer-to-layer perfect registration and misregistration.

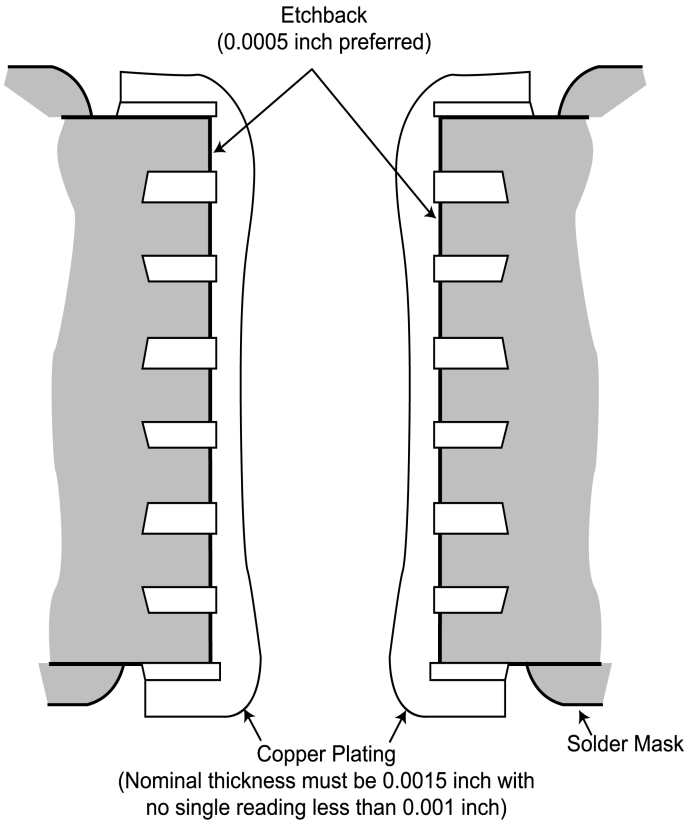

Figure 3.6-8 8-Layer MLB Showing Perfect Layer-to-Layer Registration

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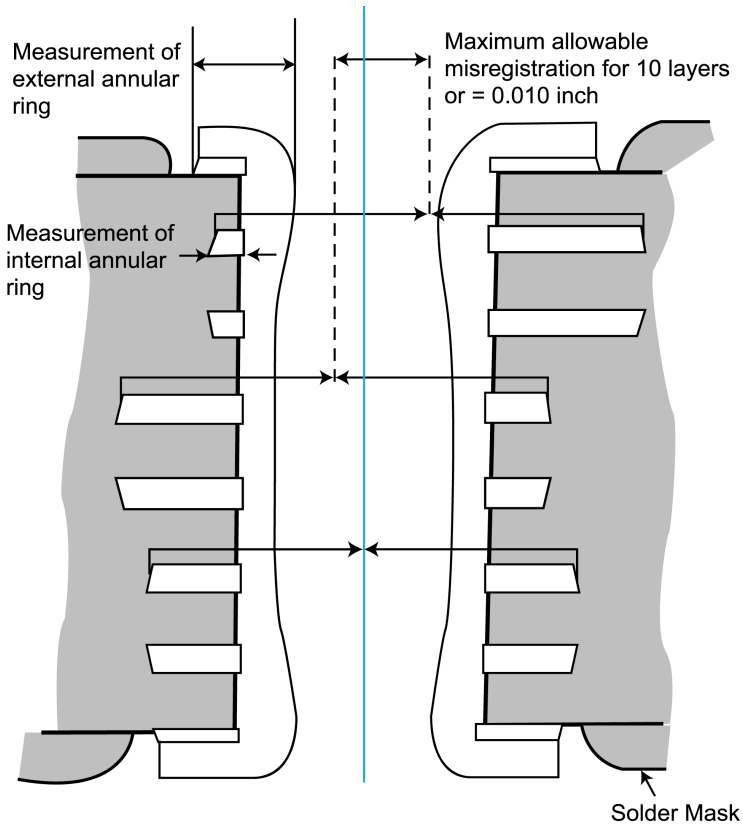

Figure 3.6-9 8-Layer MLB Showing Layer-to-Layer Misregistration and Measurement of Annular Ring (External and Internal)

5.3.7 Drilling. A suitable entry and backup material shall be used for drilling PWBs. Only one PWB shall be used per drill stack-up. A maximum of 500 hits is allowed per drill bit; after that the bit must be replaced. Resharpened drill bits shall not be allowed. A drill first article shall be used for each lot.

5.3.8 MLB Registration. An adequate tooling system shall be employed to ensure proper MLB registration. In addition, it is highly recommended that the PWB vendor employ a real-time X-ray system for viewing layer stackups to ensure good registration of the MLB.

5.3.9 PTHs and Vias. The following pertain to plated-through-holes and plated vias.

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5.3.9.1 Copper Plating. Copper plating on the wall of the plated through hole (PTH) and plated vias shall be 0.0015 inch (0.038 mm) nominal with no single reading less than 0.001 inch (0.025 mm). See Figure 3.6-8.

5.3.9.2 Etchback. There shall be etchback between 0.0002-0.001 inch (0.005-0.026 mm); 0.0005 (0.013 mm) inch is preferred. Plasma desmear/etchback is the preferred method. See paragraph 4.8.2.10 above.

5.3.9.3 Negative Etchback. Negative etchback of the copper shall be prohibited.

5.3.9.4 Annular Ring. IPC-6012 for Class 3 PWBs shall be followed for PTH vias (see Table 3.5 in IPC-6012). For PTHs used for component through-holes (e.g., connectors) the external annular ring shall be a minimum of 0.005 inches (0.128 mm) and the internal annular ring shall be a minimum of 0.002 inches (0.051 mm). All such PTHs used as component through-holes shall be clearly identified on the drawing. If not so identified, the PWB manufacturer shall follow IPC-6012, Class 3 PWBs regarding annular ring. For measurement of annular ring see Figure 3.6-9.

5.3.9.5 Buried and Blind Vias. PWBs with buried and blind vias shall be produced by sequential lamination techniques.

5.3.9.6 Via Fill. If required (see paragraphs 4.8.2.8 and 4.8.2.9 above), all empty vias shall be filled with an acceptable hole fill material. See Table 3.6-5 above.

5.3.10 Cleaning Prior to Solder Mask Application. All PWBs shall be cleaned prior to solder mask application. The document governing this activity shall be ANSI/IPC-SM-839, *"Pre and Post Solder Mask Application Cleaning Guidelines."*

5.3.10.1 Ionic Contamination Testing. Just prior to the application of solder mask, one board per lot shall be cleaned and tested for cleanliness using a suitable ionic contamination tester and the result documented. The ionic contamination level shall not exceed 10 micrograms per square inch (10 $\mu g/in^2$). Each side of the board contributes to the total area in square inches. If the board fails, the entire lot shall be recleaned, and the test repeated until the board passes the test.

5.3.11 Solder Mask. The solder mask to be used shall be one of the mask materials designated in 4.8.10 above.

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5.3.12 Surface Finish. The method of surface finish on surface mount pads or PTHs shall be specified on the drawing, and the PWB vendor shall consult the drawing. If the method of surface finish is not called out in the drawing, the method used shall be HASL.

5.3.13 Legend Ink. The legend ink to be used shall be that designated in 4.8.11 above.

5.3.14 Insulation Board. If an insulation board is called for on the drawing, it shall be of the same material as the PWB itself.

5.3.15 Electrical Test. Electrical test shall be performed on all PWBs per 4.4.1 above. In addition, a netlist comparison test shall be performed between the IPC-D-356A file generated from the design database and the Gerber extracted netlist file. See 4.4.1.1 above.

5.3.16 Rework. Minor rework, such as the use of an Exacto knife to rework shorts, shall be allowed. Repair of PWBs, such as the use of resistance welding to repair opens, shall not be allowed.

5.3.17 Maximum Bow and Twist. Maximum bow and twist shall not exceed 0.75% for SMT boards and 1.0% for all other boards.

5.3.18 Serialization and Board Identification. Each individual PWB shall be given a unique serial number following paragraph 4.5. Normally, the serial number (S/N) will begin at 001, 002, 003, etc. unless specific directions indicate otherwise. The serial numbers shall be legible and easy to read. In addition, the PWB vendor shall place his company name somewhere on each PWB to easily identify the company that manufactured the PWBs.

5.3.19 Handling & Packaging/Shipping. All completed PWBs shall be handled by their edges to avoid contamination and damage. All completed PWBs shall be bagged in ESD Barrier Bags; one PWB per bag. Then the PWBs in their respective ESD Barrier Bags are to be suitably packaged in padded envelopes to avoid damage.

5.3.19.1 Pickup at the Vendor. If convenient, the completed PWBs will be picked up at the PWB facility by either the PWB Coordinator or the QA Representative and hand carried back to JPL.

5.3.19.2 Shipping to JPL. If it is not feasible due to time and/or distance constraints to pick up the completed PWBs, they shall be shipped by a carrier that ensures overnight delivery so that they can be received by JPL the following day.

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5.3.20 Chief Fabrication Requirements.The chief fabrication requirements for JPL flight PWBs are summarized in Table 3.6-10. In the case of test PWBs, the following requirements shall still pertain:

- Electrical test of 200 Vdc;
- Desmear and etchback;
- ESD bag individually;
- Unique serial number required.

Note: If the CogE knows that the test PWB will lead into a flight PWB, he/she should consider whether some or all of the fabrication requirements for flight PWBs should be invoked.

In certain cases, to ensure adherence to the agreed-upon build schedule and to understand why slippages occur, more stringent management techniques such as a Status Tracking Matrix may be required of the PWB vendor. If necessary, consult with the PWB Process Engineer.

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Table 3.6-10 Chief Fabrication Requirements for JPL Flight PWBs

Fabrication Requirements	Yes	No	Comments
Electrical test, netlist, 200 Vdc	X		Must be netlist tested from an IPC-D-356A file generated directly from the design database, and this netlist shall be compared to the extracted netlist*
Desmear required	X		Plasma preferred method
Etchback	X		0.0002-0.001 inch; 0.0005 inch preferred
MLB lamination	X		Foil construction preferred unless otherwise specified
Dielectric separation between adjacent conductive layers	X		A minimum of 0.0035 inch attainable by the use of a minimum of two plies of prepreg
Annular ring	X		IPC-6012, Class 3
Standard surface finish	X		HASL unless otherwise specified
Copper plating in PTHs/vias	X		0.0015 inch nominal; no single reading < 0.001inch
Ionic contamination testing	X		One PWB per lot directly prior to SM application; reading must be < 10 µg/in^2
Approved solder mask (SM) material	X		See Table 3.6-7
Via fill (only required for PWBs with a backing board or blind/buried vias unless called out on the fabrication drawing)	X		See Table 3.6-5
JPL I/L and final source	X		Must be done at vendor's facility
ESD bag individually	X		ESD Barrier Bag
Unique Serial Number Required	X		For example, 001, 002, etc. On top of the PWB if room permits
Coupons Required	X		See Table 3.6-3
Microsections to be shipped with order	X		A and B microsections

*. The IPC-D-356A file shall be supplied to the PWB vendor along with the Gerber files and other appropriate files, such as the drill file, etc., in the ZIP file.

5.3.21 JPL QA Source Inspections. All flight PWBs shall have the following JPL QA source inspections:

- Inner layer (I/L);
- Final.

See paragraph 6.1.4 below.

JPL QA shall be notified, at a minimum 24 hours in advance, that the boards are ready for source. To perform this function, the PWB vendor shall email the following individuals at JPL:

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- QA Lead person in Electronic Packaging and Fabrication or his/her designated representative;
- QA Inspector normally involved with PWB source inspection;
- PWB Coordinator;
- PWB Process Engineer.

The prime point-of-contact at each PWB facility approved to build flight PWB hardware for JPL shall be given the names, email addresses, and phone numbers of the above individuals. If the list changes in any way, the point-of-contact shall receive an updated list.

Once the email is sent to the above individuals at JPL, the QA Inspector normally involved with PWB source inspection shall call the PWB vendor to verify that he/she will be there for source at the designated time. If the QA Inspector normally involved with PWB source inspection fails to call the PWB vendor within four (4) hours of the expected source, then the PWB vendor shall call either the PWB Coordinator or the PWB Process Engineer and inform them of this fact.

5.4 Fabrication Requirements-Terminal Boards

5.4.1 Terminals. Terminal installation into plated through-holes shall be per the requirements of ANSI/IPC-J-STD-001B and nonplated through-holes per the following requirements.

5.4.1.1 Physical Defects. Any of the following physical defects shall be cause for rejection:

- Split or bent tines;
- Split or cracked terminal holes;
- Delaminated base material;
- Altered spacing between bifurcations.

5.4.1.2 Orientation Tolerance. Terminals shall be oriented within ±10° of the specified orientation.

5.4.1.3 Perpendicular Tolerance. Terminal shall be perpendicular to the plane of the board within ±5°, measuring at the bottom of the tines and/or the terminal center.

5.4.1.4 Seating Tolerance. The entire base of the terminal shall rest against the wiring board, etched conductor, or terminal pad.

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5.4.1.5 Tightness. After swaging prior to soldering, terminals shall be tight enough that they cannot be rotated by hand.

5.4.1.6 Concentricity. The swaged flange shall be concentric to within 0.010 inch (0.25 mm) of the terminal centerline.

5.4.1.7 Swaging. Any of the following swage defects shall be cause for rejection. See Figure 3.6-10.

- Terminal swage more than 0.012 inch (0.030 mm) above the plane of the board;
- Funnel-type swage;
- More than two cracks in the terminal flange;
- Radial splits or cracks extending into the shank;
- More than two radial splits or cracks or two cracks less than 90° apart;
- Hairline cracks extending through the thickness of the flange;
- Roll-over edge more than 0.004 inch above board surface.

5.4.1.8 Measling or Crazing. Measling or crazing caused by terminal installation shall be acceptable provided they do not form a continuous path between conductors or a continuous area or path extending more than 0.060 inch from the terminal.

5.4.1.9 Terminal Soldering. Terminals swaged into circuit interconnection conductors shall be soldered. See Figure 3.6-11.

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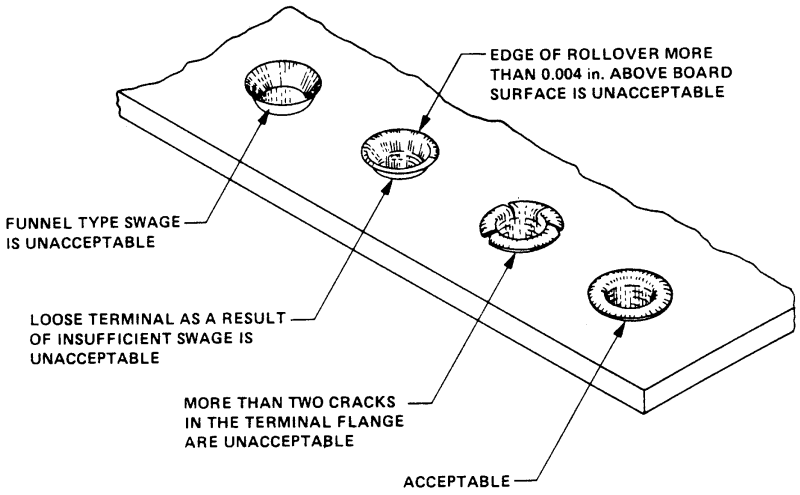

Figure 3.6-10 Terminal Swaging

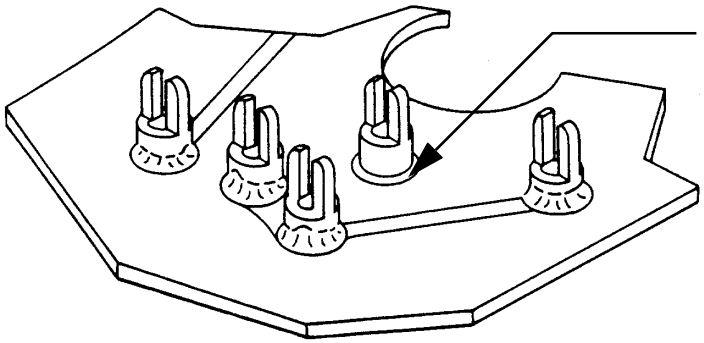

Figure 3.6-11 Terminal Soldering

6 QUALITY ASSURANCE

6.1 JPL Approval and Reviews

JPL shall reserve the right to review critical items both prior to and during the PWB fabrication process.

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6.1.1 QA Governing Documents. The documents governing the inspection of printed wiring boards by JPL QA personnel shall be QAI 10.1.2, *"Inspection of Printed Wiring Boards and Flexible or Rigid Flex Circuits"* and QAWS 100.40, *"Inspection Requirements for Fabrication of Printed Wiring and Terminal Boards."* The PWB manufacturer shall use ANSI/IPC-A-600E, *"Acceptability of Printed Boards,"* as the acceptance criteria using Class 3 acceptability level.

6.1.2 Survey of Vendor's Site. JPL reserves the right to survey the PWB fabricator's site at any time to assess its suitability for fabricating PWBs to JPL's specifications. See paragraph 2.3, Vendor Selection and Qualification, on page 3.6-3.

6.1.3 Pre-fabrication Approvals. JPL reserves the right to review all vendor artwork films and travelers prior to starting the PWB fabrication.

6.1.4 Source Inspections. The following JPL source inspections to a released drawing shall be mandatory:

- Inner layer (prior to lamination);
- Final inspection;
- Microsections–PTH coupons must show positive etchback and minimum annular ring.

Normally both inner layer source and final source shall be performed at the vendor's site by JPL QA. In the event that the vendor has established that he can perform and deliver high quality PWBs in a timely manner as expected, the requirement of inner layer inspection may be waived by the JPL PWB Process Engineer and QA.

6.1.4.1 Inner Layer Inspection. JPL inspection of inner layer details shall be 100% of the manufactured lot.

6.1.4.2 Final Inspection. JPL inspection of the finished (routed, tested, and inspected by the vendor's final inspection process) PWBs shall be 100% of the manufactured lot. JPL QA shall also examine preselected microsections of both A and B coupons. Both As-Received and Thermal Stress microsections shall be examined.

6.2 Data Package-Deliverables to JPL

The following items shall be delivered to JPL at the end of the PWB build:

- Completed PWBs.

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- Results of all electrical verification testing performed at 200 Vdc.
- All material certifications.
- Traceability - The material used shall be traceable to the manufacturer's lot number through date code and serial number.
- Certificate of Material - Certificates of material shall be part of the delivered documentation package for each PWB.
- Copies of all inspection reports, traceability data, deviations, and MRB actions shall accompany each delivered PWB.
- Coupons (microsections) + results of microsection evaluation. See paragraph 6.1.4.2 above.
- Results of ionic contamination testing.

7 GUIDELINES AND RECOMMENDATIONS

The following points are guidelines only and do not constitute official requirements.

7.1 Purpose

Because PWB technology is rapidly changing, it is felt that the use of guidelines and recommendations is a way to ensure that the design engineers keep abreast of the latest developments without unduly hampering them with hard-and-fast requirements. The points covered in these guidelines are:

- PWBs with microvias.

7.1.1 Microvia PWBs. To achieve interconnection densities higher than those achievable through such conventional techniques as through-holes and standard multilayer technology, the use of microvias is recommended. For both high density substrates and microBGA/CSP substrates, microvias should prove of value, and their use is increasing. Any assembly having over 120 attachment pads per square inch and array components of less than 0.040 inch (1.0 mm) would benefit from microvia technology. The designer may want to consult IPC/JPCA-2315, *"Design Guide for High Density Interconnects (HDI) and Microvias."*

Microvias are used in conjunction with PTHs and blind and/or buried vias to achieve very high interconnect densities (HDI). Such PWBs are known as HDI PWBs. These densities are being driven by microBGAs and chip scale packages having small pitches

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and a large number of I/Os. By definition, a microvia is a hole 0.006 inch or less used to interconnect two adjacent layers of circuitry.

7.1.1.1 Construction of a Microvia PWB (HDI PWB). There are several recognized methods for producing microvia PWBs: photoimageable dieletric formation, laser formation, and plasma formation. For high production applications, photoimageable formation of microvias seems the most promising. For high reliability applications, laser formation and plasma formation are the most promising, with laser formation being favored because of several process advantages.

7.1.1.2 Use of RCC. Using the laser formation of microvias, one of the most common materials now in use for the production of microvias is resin foil, also known as resin coated copper (RCC). This is copper foil to which is attached first C-stage (fully cured) resin followed by B-stage (partially cured) resin. This material is used as the cap in multilayer constructions, and it is the layer in which the microvias are produced. It can be used as a cap for both the top and bottom of the board (microvias on both the top and bottom). It can be applied on both the top and bottom a second time to produce a second layer of microvias. Below is one method by which microvias on both the top and bottom of a board could be produced in a PWB facility:

(1) Build a conventional Type 3 or Type 4 MLB.

(2) Make sure that the top and bottom artwork, in addition to any circuitry and other features, has target pads for the microvias. See Figure 3.6-12.

(3) Process the outer layers of the MLB like any conventional MLB but instead of applying solder mask and a surface finish, process to Step 4.

(4) Laminate RCC (the cap layers) to the MLB. The lamination can be both top and bottom if microvias are desired on both top and bottom.

(5) Use conventional artwork and photoresist to define the circuitry on the top and bottom layers. The cap layers should also contain the microvia capture pads. See Figure 3.6-12.

(6) Develop the photoresist, exposing the copper pattern.

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(7) Etch away the copper using a conventional etching technique. During the etching process, the copper to form the actual microvias is also etched away.

Note: If a UV-YAG laser is used, removing the copper to form the actual microvias is not necessary since the UV-YAG laser can ablate copper as well as resin.

(8) Ablate the exposed resin with a CO_2 laser, which will ablate the resin material but will not penetrate the copper of the capture pad.

(9) Clean the microvia hole of debris from the laser process.

(10) Plate the microvias.

(11) Finish off board.

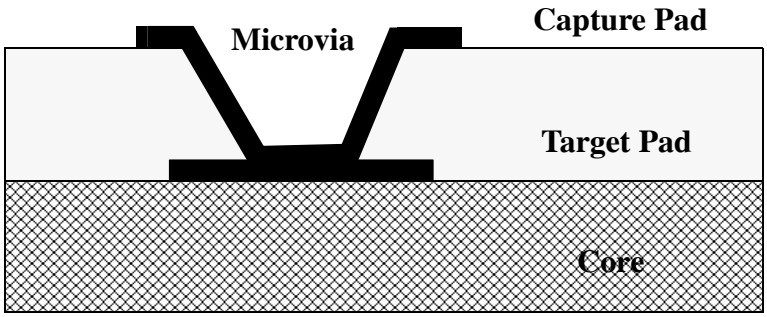

Figure 3.6-12 Microvia Structure Showing Core, Target Pads and Capture Pads

7.1.1.3 IPC Design Guidelines for Microvia PWBs. Design guidelines for microvia printed wiring boards can be found in IPC/JPCA-2315, *"Design Guide for High Density Interconnect Structures and Microvias."* Microvias are a rapidly emerging technology, and not all the details have been worked out yet regarding their construction. This is still an area under investigation and subject to rapid change.

7.1.1.4 Internal Guidelines for Microvia PWBs. The manufacturer should have the capability of producing 0.004 inch diameter microvias; however, 0.003 inch diameter is preferred. Along with the ability to produce microvias, the manufacturer should also have in-house

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capabilities to produce fine lines and spacings. Trace width/spacing capability should be 0.004/0.004; however, 0.003/0.003 is strongly preferred. Four categories of design guidelines are set forth below for use by JPL designers (see Table 3.6-11):

- Category A: This is the least demanding category of HDI processes. It should have the highest yield and the lowest cost. For HDI PWBs, this category corresponds to Level 1 producibility.
- Category B: This is the conventional HDI process category. For HDI PWBs, this category corresponds to Level 2 producibility.
- Category C: This is the high end HDI process category. For HDI PWBs, this category corresponds to Level 3 producibility.
- Category D: This is the extreme HDI process category. For HDI PWBs, this category corresponds to Level 4 producibility. It will have the lowest yield and the highest cost.

Refer to Table 3.6-11 for the specific guidelines. The parameters defined in Figure 3.6-13 are for reference to Table 3.6-11.

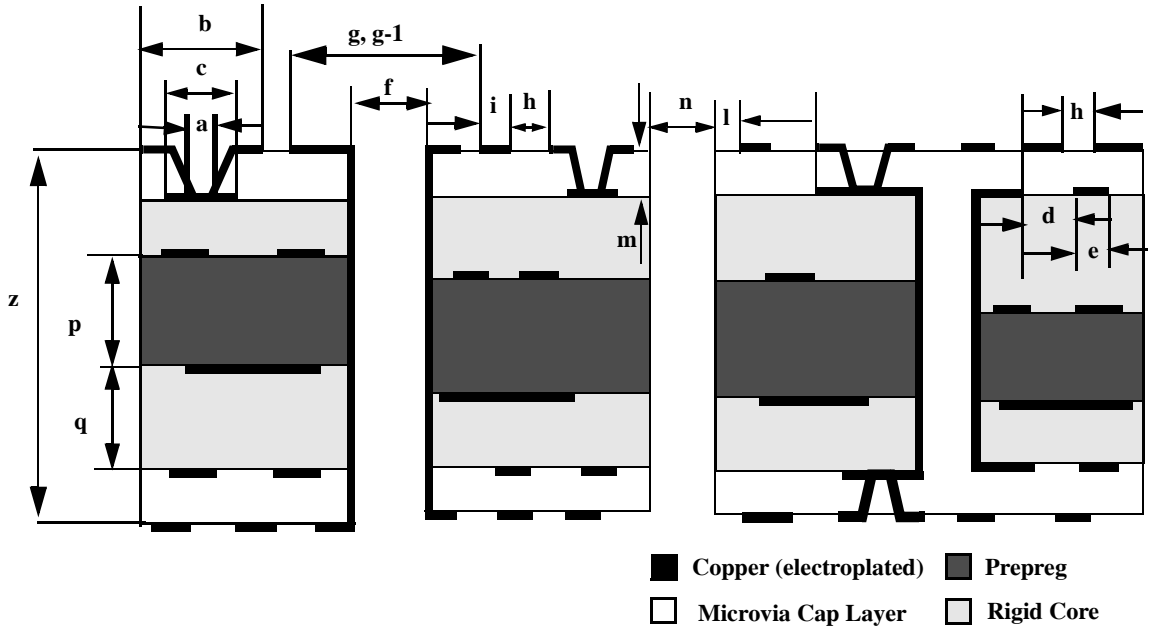

Figure 3.6-13 Parameter Identification for Table 3.6-11

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Table 3.6-11 Design Guidelines for Microvia Boards (HDI PWBs)

Symbol	Feature	Category A (µm/mil)	Category B (µm/mil)	Category C (µm/mil)	Category D (µm/mil)
a	Minimum microvia hole dia. (as imaged)	150/6	100/4	75/3	35/1.5
b	Surface via capture pad dia.	350/14	300/12	250/10	150/6
b-1	Via in SMT pad width	300/12	250/10	250/10	130/5
c	Target pad dia.	350/14	300/12	250/10	150/6
d	Conductor/pad spacing on rigid I/L	125/5	100/4	75/3	50/2
e	Trace width on core layer	125/5	100/4	75/3	50/2
f	Min. FHS (PTH)	250/10	200/8	150/6	50/2
g	Surface PTH via pad (FHS + ar x 2)	FHS + 350/14	FHS + 300/12	FHS + 250/10	FHS + 100/4
g -1	Min. through hole pad dia.	600/24	500/20	400/16	150/6
h	Trace spacing on O/L	125/5	100/4	75/3	50/2
i	Trace width on O/L	125/5	100/4	75/3	50/2
l	Surface conductor to unplated hole	250/10	200/8	200/8	200/8
m	Min. HDI (µvia layer) dielectric thickness	75/3	62.5/2.5	50/2	25/1
n	Min. unplated hole dia.	350/14	300/12	300/12	300/12
p	Min. prepreg thickness	100/4	75/3	50/2	50/2
q	Min. core thickness	100/4	75/3	50/2	50/2
z	Min. board thickness	725/29	600/24	500/20	200/16
	Min. plated thickness	25/1	20/0.8	15/06	15/0.6
	Min. AR (m/a)	< 1.0	1.0	1.5	1.3 (min. 50 µm dia.)

Abbreviations:

HDI - High density interconnect
SMT - Surface mount technology
I/L - Inner layer
O/L - Outer layer
FHS - Finished hole size
PTH - Plated through hole
ar - Annular ring
AR - Aspect ratio

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Flexible and Rigid-Flexible Printed Wiring

1 SCOPE

This specification sets forth the requirements for the design and fabrication of flight flexible (a.k.a. flex) and rigid flexible (a.k.a. rigid flex) electronic printed wiring boards (PWBs) to meet the stringent demands of JPL. In general, the IPC documents (both for design and performance) cited in paragraphs 4, 4.7, and 5 below are sufficient. Where these documents do not suffice, requirements more rigorous or far-reaching than the IPC documents are called out below.

1.1 Purpose

This specification provides the requirements and quality assurance provisions for flexible and rigid flexible PWBs procured for use in spacecraft and scientific instruments for space applications and other high reliability uses. Since the rigid portion of a rigid flexible printed wiring board is built in exactly the same fashion as a rigid PWB (see JPL D-8208, Section 3.6), this section will concentrate chiefly on the flexible portion of the PWB.

1.2 Applicability

This specification is applicable to all NASA Jet Propulsion Laboratory (JPL) programs and contracts using PWBs for space flight applications and critical ground support equipment. It shall be invoked on all procurements for flight and critical ground support equipment PWBs. It shall apply to all in-house design efforts, all direct outside vendor procurements, and also to sub-tier vendor-manufactured PWBs for JPL programs and/or contracts.

1.3 PWB Types

The boards include the following types:

- Type 1 - Single-sided flexible PWB, with or without stiffeners;
- Type 2 - Double-sided flexible PWB, with or without stiffeners;
- Type 3 - Multilayer flexible PWB (MLB) with plated-through-holes, with or without stiffeners;

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- Type 4 - Multilayer rigid flexible PWB (MLB) with plated-through-holes;
- Type 5 - Multilayer rigid flexible PWB (MLB) without plated-through-holes.

There are three use categories:

Use A - Capable of withstanding flex during installation (flex-to-install);

Use B - Capable of withstanding continuous flexing for the number of cycles as specified on the master drawing (dynamic flex);

Use C - Capable of withstanding a high temperature environment (105°C or greater).

1.4 Assembly Methods

The two assembly methods in common use are manual assembly and automated SMT assembly. Assembly refers to the mounting and subsequent soldering of components to the PWB surface. In manual assembly the components are hand mounted and hand soldered. If automated assembly is used, the components are mounted by the use (or partial use) of a piece of equipment dedicated to mounting components on the PWB. Such a machine is commonly referred to as a pick-and-place machine. The soldering techniques used are mass soldering techniques such as vapor phase reflow. The soldering operation creates a sturdy metallurgical bond (interconnect) between the components' I/Os, or leads, and the PWB.

For manual assembly, refer to JPL D-8208, Section 3.14, Component Mounting/Soldering; for automated SMT assembly refer to JPL D-8208, Section 3.5, Surface Mount Technology. Some assemblies may be assembled using a combination of the two. It is necessary to mention these assembly methods in this section since certain requirements at the PWB level are directly affected by the assembly method used to populate the PWB. In this document, PWBs that will be assembled using the Automated SMT method are referred to as "SMT PWBs." Some of the requirements in this section apply strictly to SMT PWBs, e.g., fiducials. See paragraph 4.8.5 on page 3.7-25.

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2 GENERAL INFORMATION

2.1 Role of Electronic Packaging and Fabrication

As part of the DBAT process, all flight and engineering model (EM) PWBs should be procured through Section 349, Electronic Packaging and Fabrication. The term PWB encompasses rigid boards, rigid-flex boards, and flex boards. In addition to flight and EM boards, all other PWBs should also be procured through Section 349. Section 349 maintains a controlled Approved Vendor List (AVL) for the explicit purpose of facilitating the procurement of PWBs of all quality levels from flight to breadboard. Section 349 can quickly facilitate the procurement of PWBs since it maintains close contact with the PWB vendor base and periodically assesses the vendors' capabilities.

2.2 Waivers and Deviations

The requirements set forth in this document have been developed to ensure that the PWBs procured using this procedure meet or exceed expectations and to maintain the attendant risk at an acceptable level. Any or all of these requirements may be waived. However, the cognizant engineer must be aware that as requirements are waived, the risk of failure increases. The cognizant engineer, in conjunction with the program manager, must decide if this risk is worth waiving the requirements. All waivers to the requirements shall be obtained from the DBAT Process Owner in written form. See *Category A Waiver Request/Approval* on DMIE.

2.3 Vendor Selection and Qualification

2.3.1 Vendor Selection. A recommendation may be made to add a particular vendor to the AVL based on either prior experience with the vendor or due to the vendor's outstanding reputation and/or unique capabilities. In this case, a JPL vendor survey team will perform a survey of the vendor's facility.

2.3.2 Vendor Capability. When assessing a vendor regarding his/her capability to build PWBs, the following items shall be reviewed and ascertained:

- Capability to build state-of-the-art rigid polyimide PWBs and rigid FR-4 PWBs;
- Capability to build specialty PWBs such as flex, rigidflex, PTFE (e.g., Duroid) boards, Thermount boards, etc.;

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- Capability to build a particular category of PWB, e.g., a vendor that specializes in quick turnaround, prototype PWBs may not be the optimal choice for building flight PWBs;
- A proven track record for providing high reliability PWBs;
- For rigid PWBs, certification to MIL-P-55110 (the current version) shall be required;
- For flex and rigidflex PWBs, being able to fabricate to MIL-P-50884 (the current version) shall be required;
- For PWB acceptability, use of IPC-A-600 (the current version) shall be required;
- Although not required, it is desirable that the PWB vendor be certified to ISO 9002, or be actively seeking certification, or at a minimum be ISO compliant;
- Successful compliance to the JPL Vendor Survey shall be required.

2.3.3 Survey Team. To determine a particular vendor's capability, a JPL survey team shall visit the vendor at his facility. Prior to being surveyed, a potential vendor shall be sent a letter informing them that a JPL Survey Team will be visiting their facility. At the same time as the letter is sent, the vendor will also be sent a survey questionnaire entitled *PWB Vendor Information Questionnaire* (D-21523). This questionnaire shall be completed before or at the time of the survey, preferably before. It is the responsibility of Section 349 to keep the questions of this survey updated in a timely fashion. The survey questionnaire shall be employed to assess the particular vendor's capability.

The survey team shall consist of at least one representative from Section 349 (Electronic Packaging and Fabrication) and at least one representative from Section 512 (Quality Assurance). The team may also include a representative from Procurement. QAP 30.42, "*Quality Assurance Survey of Printed Wiring Board Suppliers*," shall be used as the governing document for the survey process.

2.3.4 Vendor Qualification. During or shortly after the survey, an informal profile of the vendor may be completed to conveniently summarize vendor information. It is also highly recommended that the vendor have completed IPC-1710 (12/97), "*Manufacturer's Qualification Profile (MQP)*," and have it available upon request. If the particular PWB facility is approved, the facility with an appropriate contact is added to

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the AVL (see section 2.3.5). The vendor shall be notified either via telephone or email or both that he/she has been qualified.

2.3.5 Approved Vendor List. A list of suitable PWB vendors qualified for fabricating PWBs for JPL shall be kept. This list of suitable vendors shall constitute an Approved Vendor List (AVL); this AVL shall be maintained by Section 349 in a suitable format by the PWB Process Engineer. It is to be shared only on a valid as-needed basis.

2.3.6 Vendor Disqualification and Requalification. A vendor may be disqualified due to poor quality and/or untimely delivery. In the event that a particular vendor is disqualified, they shall be sent a letter specifying in exact detail why they are being disqualified and what steps are recommended in order to obtain requalification. This letter shall be written by QA and Section 349. In the event that disqualification is felt warranted, the vendor's name will be removed from the JPL AVL. If it is thought worthwhile to requalify the vendor based on corrective actions taken by the vendor to remedy the disapproval, a JPL Vendor Survey Team shall again perform a survey and follow the procedure stated above for new vendors.

3 ENGINEERING AND LAYOUT CONSIDERATIONS

3.1 Design For X

There are a number of important considerations that the designer should take into account to produce a high quality PWB. The following are set forth for heuristic consideration. These are:

- Design For Producibility.
- Design For Assembly.
- Design For Inspectability.
- Design For Testability.

It is the designer's responsibility to take into account all of the above in exercising the design function. Failure to take the above into consideration can result in an unsatisfactory product, that is, one that does not perform as intended in its service environment over the time period for which it was intended.

Designing for X is a nontrivial issue since if performed correctly, it results in a significant cost savings and generally a superior product. Costs escalate as the product passes out of the design stage through board fabrication and assembly and into final

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system test and integration. If a faulty product is not detected at that stage, it may result in a mission that is seriously compromised or that fails.

3.1.1 Design For Producibility (DFP). The aspects of DFP are:

- Do not needlessly design a PWB to a producibility level that makes it difficult to build the board.
- Adhere to recognized design rules.
- Plan ahead so that the PWB doesn't have to be fabricated under rushed conditions.

3.1.1.1 Producibility Level. The IPC documentation no longer supports a definition of producibility level. However, as an aid to the PWB Layout Designer, the following is set forth to define a heuristic probability level based on several pertinent board factors.

The following factors are used to define a producibility level. The parameters are:

- Trace width/trace spacing;
- Number of layers;
- X-Y dimensions;
- Number of plated holes;
- Aspect ratio;
- Blind/buried vias;
- Controlled impedance.

Each factor is assigned a particular value of its Producibility Number in one of the corresponding tables. Then, given the parameters for a given PWB, find its corresponding Overall Producibility Number by adding the Producibility Numbers for the individual factors. A careful review of the various producibility numbers of each factor will also give the PWB Layout Designer a better feel for the impact of each factor. For example, trace width/trace spacing has a greater affect on overall producibility than the number of plated holes.

The Overall Producibility Number so calculated should be used strictly as an heuristic aid to the PWB Layout Designer so that he can arrive at a sense of how producible his

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PWB is. If he has any questions regarding the producibility of any PWB, he should consult with the appropriate PWB Process Engineer.

(1) Trace width/trace spacing

Trace width/ trace spacing	10 mil/10 mil to 8 mil/8 mil	7 or 6 mil/7 or 6 mil	5 mil/5 mil	Less than 5 mil/5 mil
Producibility number	2	5	10	20

(2) Number of layers

Number of layers	4 but less than 8	8 but less than 14	14 but less than 18	18 or greater
Producibility number	2	8	14	20

Note: Single-sided and double-sided PWBs have a Producibility Number of 0 for this parameter.

(3) X-Y dimensions

X-Y Dimensions	$L \leq 4"$ and/or $W \leq 4"$	$L \leq 12"$ and/or $W \leq 12"$	$L < 18"$ and/or $W < 18"$	$L \geq 22"$ and/or $W \geq 22"$
Producibility number	2	8	14	20

(4) Number of plated holes

Number of plated holes	Less than 500	500–999	1000–3,000	Greater than 3,000
Producibility number	2	4	7	10

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(5) Aspect ratio

Aspect Ratio	Less than or equal to 6:1	Greater than 6:1 and less than/equal to 8:1	Greater than 8:1 and less than/equal to 10:1	Greater than 10:1
Producibility number	2	5	10	15

Note: The aspect ration (AR) of a PWB is the board thickness to the minimum drilled hole diameter. For example, if the minimum drilled hole diameter is 0.016 inch and the board thickness is 0.125 inch, the AR = 0.125:0.016 = 8:1 (app.).

(6) Blind and/or buried vias

Blind and/or buried vias	Yes
Producibility number	20

(7) Controlled impedance

Controlled impedance	±10% tolerance	Less than ±10% tolerance
Producibility number	7	15

Table 3.7-1 Producibility Level of a PWB

Overall Producibility Number	Level of Difficulty	Producibility Level
90-120	Extremely hard	4+
70-89	Very Hard	4
55-69	Hard	3
40-54	Average	2
20-39	Easy	1
Less than 20	Very easy	1

Examples of producibility levels calculated using the tables above.

Example 1: A PWB has trace width/spacings of 0.007 inch/0.007 inch. The board is 12 layers. The board dimensions are 10.00 inch × 6.000 inch. it has 350 plated-through-holes. The board thickness is 0.062 inch and the minimum drilled hole diameter is 0.016

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inch. Therefore, AR = 3:1 (app.). There are no blind/buried vias. No controlled impedance

Overall Producibility Number = (1) 5 + (2) 8 + (3) 8 + (4) 2 + (5) 2 + (6) 0 + (7) 0 = 25
Conclusion: Easy to produce
Producibility Level: 1

Example 2: A PWB has trace width/spacings of 0.005 inch/0.005 inch. The board is 14 layers. The board dimensions are 14.000 inch × 9.500 inch. It has 1,200 plated-through-holes. The board thickness is 0.062 inch and the minimum drilled hole diameter is 0.013 inch. Therefore, AR = 5:l (app.). There are no blind/buried vias. No controlled impedance.

Overall Producibility Number = (1) 10 + (2) 14 + (3) 14 + (4) 7 + (5) 2 + (6) 0 (7) 0 = 47
Conclusion: Average producibility
Producibility Level: 2

Example 3: A PWB has trace width/spacings of 0.005 inch/0.005 inch. The board is 14 layers. The board dimensions are 18.000 inch × 12.000 inch. It has 2,900 plated-through-holes. The board thickness is 0.125 inch and the minimum drilled hole diameter is 0.013 inch. Therefore, AR = 10: 1 (app.). There are no blind/buried vias. No controlled impedance.

Overall Producibility Number = (1) 10 + (2) 14 + (3) 14 + (4) 7 + (5) 10 + (6) 0 (7) 0 = 55
Conclusion: Hard to produce
Producibility Level: 3

Example 4: A PWB has trace width/spacings of 0.005 inch/0.005 inch. The board is 14 layers. The board dimensions are 18.000 inch × 12.000 inch. It has 2,900 plated-through-holes. The board thickness is 0.125 inch and the minimum drilled hole diameter is 0.013 inch. Therefore, AR = 10:l (app.). There are blind vias in the top two and bottom two layers. No controlled impedance.

Overall Producibility Number = (1) 10 + (2) 14 + (3) 14 + (4) 7 + (5) 10 + (6) 20 (7) 0 = 75
Conclusion: Very hard to produce
Producibility Level: 4

Example 5: A PWB has trace width/spacings of 0.005 inch/0.005 inch. The board is 14 layers. The board dimensions are 18.000 inch × 12.000 inch. It has 2,900 plated-through-holes. The board thickness is 0.125 inch and the minimum drilled hole

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diameter is 0.013 inch. Therefore, AR = 10:l (app.). There are blind vias in the top two and bottom two layers. Controlled impedance ± 10%.

Overall Producibility Number = (1) 10 + (2) 14 + (3) 14 + (4) 7 + (5) 10 + (6) 20 (7) 7 = 82
Conclusion: Very hard to produce
Producibility Level: 4

Example 6: A PWB has trace width/spacings of 0.004 inch/0.004 inch. The board is 14 layers. The board dimensions are 18.000 inch × 12.000 inch. It has 3,500 plated-through-holes. The board thickness is 0.125 inch and the minimum drilled hole diameter is 0.013 inch. Therefore, AR = 10:l (app.). There are blind vias in the top two and bottom two layers. Controlled impedance ± 5%.

Overall Producibility Number = (1) 20 + (2) 14 + (3) 14 + (4) 10 + (5) 10 + (6) 20 (7) 15 = 103
Conclusion: Extremely hard to produce
Producibility Level: 4+

3.1.1.2 Design Rules. The designer shall follow recognized design rules for designing the PWB, and shall exercise sound judgment in ensuring that the board shall not deviate too greatly from recognized designs. The following are particularly sensitive to DFP:

- Make sure that the aspect ratio (AR) is no greater than 8:1. An AR of 6:1 or less is preferred.
- Trace width/trace spacing should be no less than 0.005 inch.
- If the board is a multilayer, make sure that the construction is symmetrical.
- Pad size for plated holes. The formula for calculating minimum pad size is:

$$PAD_{min} = FHS_{nom} + 2ar + FA$$

where FHS_{nom} = nominal finished hole size
ar = minimum annular ring allowed
FA = fabrication allowance (varies from one PWB facility to another).

Bear in mind that the PWB vendor must control both the layer-to-layer registration and the hole-to-pad registration when producing a multilayer PWB.

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Example: When designing pad sizes, bear in mind this chart:

PAD SIZE	**EASE OF FABRICATION**
FHS_{nom} + 0.024 inch	PREFERRED
FHS_{nom} + 0.018 inch	STANDARD
FHS_{nom} + 0.014 inch	ADVANCED
FHS_{nom} + 0.012 inch	VERY ADVANCED (some PWB facilities may not be able to do this)

Also remember that if the finished hole size is specified as 0.018 ± 0.003 inch, then the calculated FHS_{nom} will be 0.018 inch. However, if the finished hole size is specified as 0.018 + 0.003-0.001 inch, then the calculated FHS_{nom} will be 0.019 inch, not 0.018 inch.

Based on this, one can arrive at various pad sizes for a FHS_{nom} = 0.018 inch

PAD_{min} = 0.042 inch PREFERRED

PAD_{min} = 0.036 inch STANDARD

PAD_{min} = 0.032 inch ADVANCED

PAD_{min} = 0.030 inch VERY ADVANCED

3.1.1.3 Planning. In addition to following good design rules, both the designer and the project engineer should plan effectively to avoid a situation in which the PWB vendor must hastily fabricate the PWB. It is important to remember that the more complex the PWB, the more lead time should be allowed for its fabrication. Compressing the lead time is not recommended. A rule-of-thumb table is given below to guide the designer and project engineer. See Table 3.7-2.

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Table 3.7-2 Fabrication Allowance Time

Type of PWB	Recommended time allowable for fabrication after placement of the PO*
Single-sided PWB	7 days
Double-sided PWB	7–10 days
4-6 lyr MLB (multilayer board)	3–4 wks.
8 lyr and > 8 lyr MLB	4–5 wks.
Blind and/or buried vias MLB	5–6 wks.
Line widths/line spaces < 0.005"	5–6 wks.
Controlled impedance board	5–6 wks.

* PO = purchase order. Placement is defined as that date in which the vendor receives the PO documentation.

4 DESIGN REQUIREMENTS

Design rules for printed wiring boards (PWBs) shall be per the documentation hierarchy set forth in IPC-2221 (1998), *"Generic Standard on Printed Board Design."* Regarding flexible printed wiring boards, the chief document, in addition to IPC-2221 (1998), is IPC-2223, *"Sectional Design Standard for Flexible Printed Boards."* Exceptions to these two documents are detailed in this section. In addition, the designer is strongly encouraged to peruse the Section 349 (Electronic Packaging and Fabrication) procedure, *Printed Wiring Products Acquisition*, which can be viewed by going to http://section349.jpl.nasa.gov and clicking "MCDL."

4.1 Preferred Units

The preferred units are English (inch or mil where 1 mil = 0.001 inch) rather than metric (millimeters [abb. mm]). The units shall be given in English with hard metric units in parentheses. Note that the above IPC standards utilize metric units (mm) in all tables. If conversion is necessary, use the following conversion factor:

$$X(\text{in mm}) \times 0.03937 = Y \text{ inch.}$$

4.2 Performance Class

The performance class shall be IPC Class 3, High Reliability Electronic Products.

4.3 Dimensioning and Tolerancing

All dimensions and tolerances shall be per ANSI Y14.5.

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4.4 Electrical Testing

There are two aspects to electrical testing. There is electrical verification testing at the PWB facility, and in addition, for flight PWBs, an Integri-Test is performed in Section 349.

4.4.1 Electrical Verification Testing at the PWB Vendor. Electrical verification testing shall be conducted at the vendor's facility, and the vendor shall ensure that this test is performed. If the vendor subcontracts the work to a test facility, the vendor shall inform JPL that this is being done prior to the test being performed. JPL shall have a say if the subcontracted testing facility is adequate.

All electrical testing shall be conducted at 200 Vdc minimum. Unless otherwise specified on the drawing, electrical verification testing shall consist of netlist testing using suitable test instrumentation. The PWB vendor shall be supplied with an IPC-D-356A file supplied along with the Gerber files in the ZIP file (see 4.10 below) for the purpose of electrical testing. See paragraph 4.4.2.2 below. The results of such a test shall constitute one of the deliverables to JPL. See paragraph 6.2 below.

4.4.1.1 Netlist Comparison between the Design Database Netlist File and the Gerber Extracted Netlist File. In addition, the vendor shall perform a netlist comparison between the IPC-D-356A file generated directly from the design database (schematic netlist) and the extracted netlist file from the Gerber data (extracted netlist). In this way, electrical continuity and isolation errors can be detected at the time the front-end engineering (FEE) is performed at the PWB vendor's facility rather than at electrical test when the PWBs have already been manufactured. In the event that discrepancies are found, the PWB vendor shall inform the JPL PWB Coordinator and/or the JPL PWB Process Engineer, preferably by email. The PWB Coordinator shall inform the PWB vendor to put the job on hold, by email, until all discrepancy issues are resolved. When all discrepancies have been resolved, the PWB Coordinator shall inform the PWB vendor to resume the PWB build, by email.

4.4.2 Integri-Test. Flight PWBs shall have complete netlist testing by Section 349 prior to assembly. In addition, engineering model (EM) PWBs should be considered as potentially flight PWBs, and they too shall have complete netlist testing prior to assembly. Both double-sided (DS) PWBs and multi-layer boards (MLBs) shall have netlist testing.

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At a minimum, at least one flight PWB per lot shall have netlist testing performed on the Integri-Test testing machine. The name of the netlist testing machine used by section 349 is the Integri-Test® testing machine. At the same time, if the PWB is a surface mount technology (SMT) board, at least one flight PWB per lot shall also be tested for adequate solderability. The Planning Engineer[1] shall indicate on the Service Order (SO) that the Integri-Test shall be part of the procurement of all flight PWBs. There are two separate conditions relating to the generation of an appropriate file for the Integri-Test so that it may be conducted.

4.4.2.1 Integri-Test (IT) Service Process for PWBs. The IT service process originates through the SO request process at the time of the original request to buy PWBs from a vendor is executed. After the PWB order has been delivered and inspected (with an accompanying Inspection Report, i.e., IR), a single PWB is selected to be IT processed. The selection is normally done from the highest serial number available; it could however be the one board that has the most superficial flaws discernible by unaided visual check.

The PWB Coordinator delivers the procured hardware package to the Planning and Control Planner. The Planning and Control Planner logs the task into the Production Planning and Control system and then make arrangements with the IT File Engineer (ITFE) to produce a compatible file for execution in the Integri-Test computer. At the same time, the Planning and Control Planner solicits an AIDS from the appropriate Fabrication Engineer for test execution. The Planning and Control Planner is also responsible for the appropriate QA signatures on the AIDS prior to start of test. This AIDS will include both the IT service and the SERA solderability test service. The file and AIDS, along with the original package, is handed to the IT Coordinator for testing.

Upon completion of both tests, QA does a buyoff by generating an IT IR. Copies of the IR and data package, along with the original materials and PWB, are returned to the Planning and Control Planner for final disposition. The Planning and Control Planner then places the tested PWB back into the Production Planning and Control system.

4.4.2.2 Files Placed on DocuShare. Thus, there will normally be three separate files placed in DocuShare by the Planning Engineer. These are:

(1) The output file from the design database (either an IPC-D-356A file or a Neutral file);

1. The Planning Engineer is generally the person responsible for generating the Service Order (SO).

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(2) The IPC-D-356A file generated by the IT File Engineer or another designated party if a Neutral file is supplied;

(3) The IPC-D-356A file converted to an ASCII file by the Integri-Test technician.

4.4.3 Alternative Procedure for Creating an IPC-D-356A File. If an E-CAD system not capable of generating either an IPC-D-356A file or a Neutral file, it shall then be the responsibility of the PWB designer (or a designated third party) to ensure that a file is directly generated from the design database that can be converted into an IPC-D-356A file. It is the responsibility of the designer to ensure that the final output is an IPC-D-356A file. If the designer cannot ensure this, he/she should negotiate with the cognizant engineer to arrange to have this done.

4.5 PWB Identification

The designer shall follow the recommendations in this paragraph to the extent that it is practical and design rules are not violated. The designer shall ensure that the PWB artwork shall have both a FAB (PWB fabrication) number and an ASSY (PWA = printed wiring assembly) number on the top side of the PWB so that these numbers are etched in the PWB along with the traces, vias, etc. The FAB number and the ASSY number shall agree with the drawing numbers. In addition, the word REV. and S/N (serial number) shall also be etched in the PWB. For ease of identification, the FAB number shall be indented. However, the fields after REV. and S/N shall be left blank.

ASSY 101XXXXX REV. S/N

FAB 101XXXXY REV. S/N

If the above is not feasible due to space limitations on the board, the designer should have the first row on the top side of the PWB

ASSY 101XXXXX REV. S/N

and the second row on the bottom side.

FAB 101XXXXY REV. S/N

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If convenient, the designer shall have the artwork contain the acronym of the project so that it too is etched into the board. If the PWB has a backing board that will be bonded to the bottom side, then the designer should revert to placing both on the top side.

Note: By definition the top side of the PWB is the side appearing by looking down on the PWB from above. This is also often designated the component side. However, some boards today have components on both sides of the board.

The PWB vendor shall have the responsibility of filling in the REV. field and the S/N field of the bare PWB either with the silk screen or by a suitable marking technique. These numbers shall be clearly legible. If possible, the PWB vendor should modify the artwork so that the S/N numbers are etched into the PWB. When the PWBs are received back from the PWB vendor, the identification fields should appear as such.

PWB #1

ASSY	101XXXXX	REV.	S/N
FAB	101XXXXY	REV. X	S/N 001

PWB #2

ASSY	101XXXXX	REV.	S/N
FAB	101XXXXY	REV. X	S/N 002

In addition, a Lot Date Code shall be marked on the board by the PWB vendor using a suitable technique to ensure that the code is legible. If there is room at the top of the board, the company shall give their name, e.g., Golden Era Circuits. Otherwise, the name shall appear on the bottom of the board. Panel location numbers shall not be acceptable as S/N numbers.

4.5.1 Serialization in the Case of PWB Rebuild. If delivery of the PWBs is made, the PWBs are accepted by JPL, and the PWB manufacturer has occasion to rebuild the boards, the S/N numbers shall be increased by 100. Given the case illustrated above, the new S/N numbers in this instance would be 101, 102, etc. Make sure that the PWB vendor is informed and understands that the PWBs in question are being rebuilt.

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4.6 Coupons

The use of coupons shall constitute one of the primary ways for establishing the quality of PWBs. The coupon set called out in Table 3.7-3 shall be adhered to, both by type and number. The smallest applicable board hole size shall be used for the A and B coupons, that is, the coupon set shall reflect the specific finished PWB characteristics. It will be noted that some of the coupons are for Group B testing (C, E, M, and P) and some are for internal process control at the PWB facility (A, B, G, and M). Of all the coupons, the ones most useful for evaluating the quality of the PWB are the A and B coupons.

Note: The PWB manufacturer supplies the artwork for the coupons at the time that the Gerber files are photoplotted at the vendor's facility.

4.6.1 A and B Coupons. The principal coupons used by JPL QA for evaluating PWB quality are the A and B coupons. These coupons contain plated-through-holes (PTHs), and they are processed along with the PWBs on the panel as it experiences the various manufacturing processes. The PTHs in these coupons shall be representative of the actual PTHs found in the PWBs themselves. At a minimum, three microsections ("buttons") shall be prepared for JPL QA inspection at the PWB vendor's facility. These are:

(1) B (X-Direction) As-Received;

(2) A (X-Direction) Thermal Stress;

(3) B (Y-Direction) Thermal Stress.

The holes of the coupons that are to be thermal stressed shall not be filled with any hole fill material, regardless of whether such material is used to fill the vias of the PWBs proper.

These microsections shall constitute one of the deliverable items to JPL. See paragraph 6.2 on page 3.7-56. The vendor shall also submit the results of the coupon evaluations and these shall also constitute one of the deliverable items.

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Table 3.7-3 Coupon Type, Identification, and Frequency and Position on Panel

Purpose of Coupon	Identification Letter	Frequency and Position on Panel
Hole solderability	A	Three per panel (two from diagonally opposite corners)
Thermal stress*, plating thickness, and bond strength	B	Two per panel (from diagonally opposite corners)
Plating adhesion and surface solderability (This is for Group B testing)	C	One per panel, position optional, pattern defined by artwork
Moisture and insulation resistance (This is for Group B testing)	E	Two per panel opposite corners
Solder mask adhesion (Done by the PWB vendor for PC purposes)**	G	One per panel with solder mask, location optional
Surface mount solderability (SMT boards only) (Done by the PWB vendor for PC purposes)	M	One per panel, position optional, pattern defined by artwork
Surface mount bond strength (SMT boards only) (Not always run; not necessary if misrun)	N	One per panel, position optional, pattern defined by artwork
Copper peel strength (This is for Group B testing)	P	One per panel, position optional, pattern defined by artwork

* The microsectioning after thermal stress shall be conducted following IPC-A-600, Rev. E, Acceptability of Printed Boards, Internally Observable Characteristics

** PC = process control.

Note: As a double check, it is recommended that microsectioning be performed on a periodic basis at JPL (the Failure Analysis Laboratory at JPL can perform this function) to validate the results of the PWB manufacturer's microsectioning results.

Note: If the lot size is sufficient (lot size ≥ 5), the sacrifice of an actual PWB to determine the above characteristics would be highly advantageous.

4.7 Material Identification and Specification

For material identification and material designations, the following IPC documents shall be followed:

IPC-MF-150, *Metal Foil for Printed Wiring Applications*;

IPC-FC-232, *Adhesive Coated Dielectric Films for Use as Cover Sheets for Flexible Printed Wiring and Flexible Bonding Films*;

IPC-FC-241, *Metal Clad Flexible Dielectrics for Use in Fabrication of Flexible Printed Wiring*;

IPC-4101, *Specification for Base Materials for Rigid and Multilayer Printed Boards.*

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Since these documents employ metric units, English units shall be given in brackets following the metric units.

4.7.1 Abbreviations. The following abbreviations are pertinent to the above specification.

L = laminate;

P = prepreg;

B (1^{st} B) = thickness tolerance class (can be A or B; use B unless a more stringent requirement is needed);

B (2^{nd} B) = surface quality class (can be A or B; use B unless a more stringent requirement is needed).

4.7.2 Examples of Common Material Callouts. The following give several common callouts that the designer may desire in specifying materials. For further details, consult IPC-4101.

- L 24 = sheet 24 in IPC-4101, which is standard FR-4 epoxy laminate reinforced with woven E-glass and having a T_g between 150°C to 200°C.
- P 24 = sheet 24 in IPC-4101, which is standard FR-4 epoxy prepreg reinforced with woven E-glass and having a T_g between 150°C to 200°C.
- L 40 = sheet 40 in IPC-4101, which is standard polyimide laminate reinforced with woven E-glass and having a minimum T_g of 200°C.
- P 40 = sheet 40 in IPC-4101, which is standard polyimide prepreg reinforced with woven E-glass and having a minimum T_g of 200°C.
- L 41 = sheet 41 in IPC-4101, which is standard polyimide laminate reinforced with woven E-glass and having a minimum T_g of 250°C.
- P 41 = sheet 41 in IPC-4101, which is standard polyimide prepreg reinforced with woven E-glass and having a minimum T_g of 250°C.
- L 42 = sheet 42 in IPC-4101, which is standard polyimide laminate reinforced with woven E-glass and having a T_g of 200°C–250°C.
- P 42 = sheet 42 in IPC-4101, which is standard polyimide prepreg reinforced with woven E-glass and having a T_g of 200°C–250°C.

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- L 50 = sheet 50 in IPC-4101, which is modified epoxy laminate reinforced with woven Aramid fibers (Thermount) and having a minimum T_g of 135–190°C.
- P 50 = sheet 50 in IPC-4101, which is modified epoxy prepreg reinforced with woven Aramid fibers (Thermount) and having a minimum T_g of 135–190°C.
- L 53 = sheet 53 in IPC-4101, which is standard polyimide laminate reinforced with non-woven Aramid fibers (Thermount) and having a minimum T_g of 220°C.
- P 53 = sheet 53 in IPC-4101, which is standard polyimide prepreg reinforced with non-woven Aramid fibers (Thermount) and having a minimum T_g of 220°C.

4.7.3 Laminate/Prepreg Material Choice. The laminate/prepreg material choice for all flight PWBs, EM PWBs, and critical ground support equipment PWBs shall be polyimide reinforced E-glass copper clad laminate and polyimide reinforced E-glass prepreg for all single-sided, double-sided, and multilayer PWBs. Epoxy reinforced E-glass (FR-4) copper clad laminate and epoxy reinforced E-glass (FR-4) prepreg is suitable for test boards and standard ground support equipment. Polyimide has superior properties to FR-4 material, particularly because it has a higher T_g and a reduced CTE-Z. These properties afford it to better withstand thermal excursions, both during service operating temperatures and assembly rework to avoid lifted lands. See Table 3.7-4.

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Table 3.7-4 Tg and CTE-Z of Three Resin Systems

Resin System	T_g °C	CTE-Z 10^{-6} in/in/°C (ppm)	Er*	WA %†
Polyimide	200-250	50	4.1	0.43
FR-4 (difunctional)	125	85	4.4	0.14
FR-4 (multifunctional)	170	70	4.4	0.13

* Er = dielectric constant relative to vacuum.

† WA = water absorption as a percent.

Note: The T_g (glass transition temperature) and the CTE-Z (coefficient of thermal expansion-Z axis) are two of the most critical properties of the PWB resin system. The T_g is that temperature at which the resin system making up the PWB loses its rigidity and becomes more rubber-like; its electrical and mechanical properties are also seriously degraded. Resin systems with higher T_gs are favored. See Table 3.7-4.

Note: The CTE-Z refers to the expansion of the resin system in the unrestrained direction due to thermal excursion. Resin systems with lower CTE-Zs are favored. See Table 3.7-4.

Note: Polyimide tends to absorb more water than epoxy. For this reason, it must be baked prior to certain processes to rid it of moisture.

4.8 Design Rules

4.8.1 Materials. Specific material issues:

- Constraining core material;
- Prohibition of Copper-Invar-Copper (CIC) or Copper-Molybdenum-Copper (CMC);
- Backing board.

4.8.1.1 Eyelet Prohibition. Eyelets shall be prohibited on flex and rigid flex PWBs.

4.8.1.2 Backing Board. A backing board is also known as an insulation board. If a backing board is used, as in the case of rigid flex PWBs, it shall be called out on the fabrication drawing. Regarding the installation of a backing board, there are two different installation procedures that must be distinguished on the drawing: (1) If backing board has no terminals to be installed, the PWB manufacturer normally installs the backing board. (2) If the backing board is to have terminals installed, JPL personnel will install both the backing board and the terminals.

The designer shall specify on the fabrication drawing which of the two procedures is to be followed. If case (1) is to be followed, the drawing number stands as is. If case (2) is to be followed, the drawing number must make use of a hyphenated number indicating

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that the PWB manufacturer is not responsible for the fabrication of everything on the drawing. For example, the drawing number could be 101XXXXX-501. Refer to JPL-STD-00001, *"Drafting Manual,"* Rev. C.

4.8.1.3 Backing Board Installed by the PWB Manufacturer. If the PWB manufacturer installs the backing board, the backing board material shall be of the same type as the PWB, e.g., if the PWB is polyimide reinforced E-glass, the backing board shall also be polyimide reinforced E-glass. Generally a double-sided copper clad 0.008 inch core is used. The PWB manufacturer etches off the copper and laminates the resulting bare core to the PWB using prepreg of the same resin type as the PWB and backing board.

4.8.1.4 Backing Board Installed at JPL. If the backing board is installed at JPL, the terminals are swaged into place. The bottom of the terminal holes are filled with Eccobond 55/9, and in addition, any counterbored holes are filled with Eccobond 55/9. The backing board is also bonded to the PWB using Eccobond 55/9.

4.8.2 PTHs and Vias. There are several important considerations regarding plated through holes (PTHs) and vias: pad size, clearance from ground and voltage planes, copper plating, unused pads, PTH-via fill, tented vias (not allowed), etchback, buried and blind vias, PTH connection restriction in the case of terminals.

4.8.2.1 Pad Size. The formula for calculating minimum pad size is:

$$PAD_{min} = FHS_{nom} + 2ar + FA$$

where:

FHS_{nom} = nominal finished hole size
ar = minimum annular ring allowed
FA = fabrication allowance.

See paragraph 3.1.1.2, "Design Rules" on page 3.7-10 above for an example.

Note: Different PWB facilities will have different FAs. It would be a good idea to consult with the PWB Process Engineer if there are any questions regarding the FA to be used.

4.8.2.2 Pad Shape. If feasible, the pad shape on the inner layers shall be that of a teardrop. This helps improve the reliability of the PTH.

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4.8.2.3 Hole Size Tolerance. The size specified for a hole shall be for the finished hole. Unless otherwise specified on the fabrication drawing, the hole size tolerance shall be ± 0.003 inch.

4.8.2.4 Clearance from Ground and Voltage Planes. Plated through holes shall have a minimum of 0.009 inch (0.23 mm) clearance from all ground and voltage planes.

4.8.2.5 Annular Ring. IPC-2221 for Class 3 PWBs shall be allowed for PTH vias (see 9.1.2 and Table 9.2 in IPC-2221).

4.8.2.5.1 *Annular Ring for PTHs Used for Component Leads.* For PTHs used for component through-holes (e.g., connectors) the external annular ring shall be a minimum of 0.005 inches (0.128 mm) and the internal annular ring shall be a minimum of 0.002 inch (0.051 mm). PTHs to be used as component through-holes shall be clearly called out in the drawing hole schedule.

4.8.2.6 Copper Plating. Copper plating on the walls of plated through holes and plated vias shall be 0.0015 inch (0.038 mm) nominal with no single reading less than 0.001 inch (0.025 mm). See Figure 3.7-8

4.8.2.7 Unused Pads. There shall be no electrically and/or mechanically unused pads on any of the internal layers. Isolated pads used for mechanical support, and in the case of flex PWBs—surface topography, shall not be removed, but the drawing should indicate that such pads are present.

4.8.2.8 PTH-Via Fill. PWBs that will be mounted to a backing board shall have all empty PTH vias filled with one of the materials designated in Table 3.7-5. If the PTH vias are unobstructed and can easily be cleaned during the assembly cleaning process, via hole fill is optional. If a via hole fill material is used on the PWBs to fill vias, it shall not be used to fill the holes of the coupons that are to be thermal stressed. See paragraph 4.6.1 above.

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Table 3.7-5 Acceptable Via Hole-Fill Material

Hole-fill Material	Manufacturer	Distributor or Supplier
Hysol 1C (2-part epoxy)	Dexter Corp. Seabrook, NH (800) 767-8786	K.R. Anderson Santa Ana, CA (714) 549-1343
Armstrong C7/W (2-part epoxy)	Resin Technology South Easton, MA (508) 230-8070	Ellsworth Adhesive Systems Tustin, CA (800) 888-0698
Eccobond 285 (2-part epoxy)	Emerson & Cuming Billerica, MA (978) 436-9700	Ablestik Laboratories Rancho Dominguez, CA (310) 764-4800
Peters SD 2361 (1-part epoxy)	Lackwerke Peters D-47882 Kempen Germany	Electrochemicals Inc. Maple Plain, MN 55359 (800) 321-9050
Peters PP 2795 (1-part epoxy) white	Lackwerke Peters D-47882 Kempen Germany	Electrochemicals Inc. Maple Plain, MN 55359 (800) 321-9050
Peters PP 2795-SD (1-part epoxy) grey	Lackwerke Peters D-47882 Kempen Germany	Electrochemicals Inc. Maple Plain, MN 55359 (800) 321-9050
B-stage resin of approximately the same composition as that of the board. If this does not completely fill the holes, one of the above two materials shall be used to finish the fill.	N/A	N/A

4.8.2.9 Tented Vias. Tented vias shall not be allowed. All blind and/or buried vias shall be filled with one of the materials designated in Table 3.7-5.

4.8.2.10 Etchback. There shall be etchback between 0.0002-0.002 inch (0.005-0.050 mm); 0.0005 (0.013 mm) inch is preferred. Figure 3.7-8 on page 3.7-46 displays a plated through hole showing acceptable etchback and perfect layer-to-layer registration. However, regardless of the amount of etchback achieved, there shall be no separation between the inner layer copper and the plated through hole copper after thermal stress. Appropriate microsections shall be examined to ensure that this is the case.

Note: Polyimide is difficult to ecthback.

Note: Etchback is defined as the controlled removal of all components of the base material (glass and resin) by a suitable process, e.g., plasma, on the side walls of the holes prior to plating to expose additional conductor areas.

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Note: Negative etchback is defined as the process in which inner conductor material is recessed relative to the surrounding base material.

4.8.2.11 Negative Etchback. Negative etchback of the copper shall be prohibited.

4.8.2.12 Buried and Blind Vias. PWBs with buried and blind vias shall be designed such that buried and blind vias shall be produced by sequential lamination techniques. See paragraph 4.8.2.9 above.

4.8.2.13 Through Hole Connection Restriction. Through holes (unplated) used for terminal mounting shall not have internal PWB connections.

4.8.3 Non-Plated Through Holes. Non-plated through holes shall have 0.015 inch (0.038 mm) clearance from conductors and all other conductor elements, including PTHs. Non-plated through holes shall be kept at 0.050 inch (1.26 mm) minimum from the edges of the board.

4.8.4 Antipads in the Plane Layers. To ensure sufficient isolation of the internal plane layers, when designing antipads in the plane layers, bear in mind this chart:

ANTIPAD SIZE	**EASE OF FABRICATION**
FHS_{nom} + 0.030 inch	PREFERRED
FHS_{nom} + 0.026 inch	STANDARD
FHS_{nom} + 0.022 inch	ADVANCED
FHS_{nom} + 0.014 inch	VERY ADVANCED (some PWB facilities may not be able to do this)

Note: An antipad is also referred to as a clearance from the plated through hole to the internal plane.

Also remember that if the finished hole size is specified as 0.018 ± 0.003 inch, then the calculated FHS_{nom} will be 0.018 inch. However, if the finished hole size is specified as 0.018 + 0.003-0.001 inch, then the calculated FHS_{nom} will be 0.019 inch, not 0.018 inch.

4.8.5 Fiducials for SMT PWBs. All SMT PWBs shall have fiducials on the PWB surface to aid in the placement of components during the SMT assembly process. All fiducials (and tooling holes) shall be placed on an appropriate grid. If the SMT PWB has components on both sides of the board, fiducials shall be placed on both sides of the board.

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Note: A fiducial is a fixed location point on a PWB surface used by a placement machine's vision system to orient itself for accurate component placement. Global fiducials are associated with the PWB surface as a whole. Local fiducials are associated with particular components. See Figure 3.7-1.

4.8.5.1 Global Fiducials. All SMT PWBs shall have three global fiducials on the PWB to ensure accurate placement of components on the PWB surface prior to the solder reflow operation. These three fiducials shall be placed in three of the corners, and each fiducial shall be a 0.040 inch diameter pad (no hole) having a 0.050 inch clearance around it. All global fiducials shall be a minimum of 0.200 inch from the PWB edge.

4.8.5.2 Local Fiducials. For each leaded component on the board surface having a pitch of 0.025 inch or less, there shall be two local fiducials at opposite corners of the component footprint for proper component placement. These local fiducials shall have exactly the same dimensions as the global fiducials.

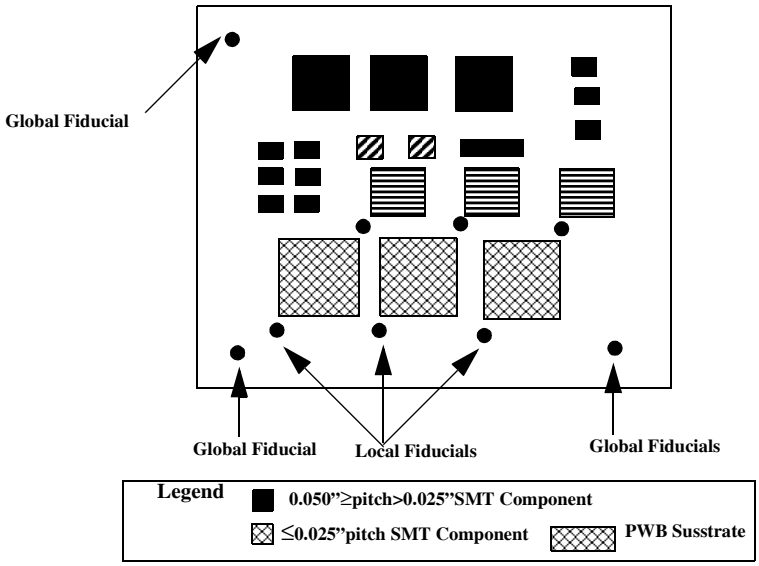

Figure 3.7-1 Global and Local Fiducials Depicted on a Surface Mount PWB

4.8.6 Footprint Patterns. The designer shall consult JPL D-8208, Section 3.5, Surface Mount Technology, as applicable for either SMT or manual assembly. It may also be applicable for the designer to consult JPL D-8208, Section 3.14, Component Mounting/Soldering. In addition, the designer may wish to consult EP517060, *"Design Requirements for*

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Surface Mount Component Footprints on Printed Wiring Boards, Detail Specification for," and CS515520, *"Footprint Requirements for Printed Wiring Boards, Detail Specification for."* The latter document must be used cautiously since portions of it are out of date. Footprint patterns can also be obtained from the various packaging manufacturers' guidelines. Many of these guidelines can be accessed over the Internet or are free from the manufacturer.

4.8.7 Distance of Features to Board Edges and to Mounting Holes. The following pertain to conductive feature spacing to the board edges and to mounting holes.

4.8.7.1 Distance of Features to Edges of Board. All conductors, such as pads, traces, and including ground and power planes, shall be no nearer than 0.030 inch (0.76 mm) to the edges of the board.

4.8.7.2 Distance of Features to Mounting Holes. All conductors, including planes, shall be a minimum of 0.030 inch (0.76 mm) clearance from fastener heads or washers as shown in Figure 3.7-2. All conductors, including ground and power planes, shall be a minimum of 0.030 inch (0.76 mm) from mounting holes.

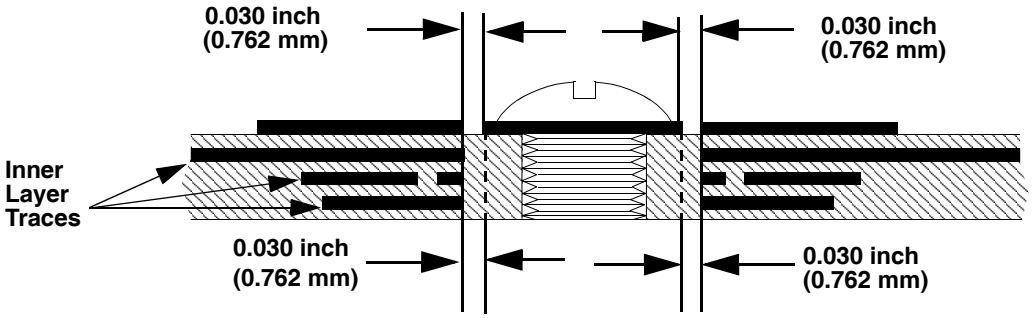

Figure 3.7-2 Mounting Hole Size

4.8.8 Terminals. Nonplated through-holes shall be designed and installed per the requirements given herein. See paragraph 4.8.2.12, "Buried and Blind Vias." on page 3.7-25. for additional information regarding connection restrictions.

4.8.8.1 Terminal Pad Size. Pads for terminals shall be a minimum diameter of 0.015 inch (0.38 mm) larger than the terminal base.

4.8.8.2 Terminal Soldering. Terminals shall be soldered to the terminal pad.

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4.8.8.3 Hole Size. Holes for mounting terminals shall be 0.004 inch (0.102 mm) larger than the nominal diameter of the terminal shank, with a difference between the minimum and maximum diameter (unilateral tolerance) as provided in Table 3.7-6.

Table 3.7-6 Terminal Hole Unilateral Tolerance

Hole Diameter (inch)	Difference (inch)	Hole Diameter (millimeter; mm)	Difference (millimeter; mm)
Up to 0.032	0.002	Up to 0.81	0.05
0.033 to 0.063	0.003	0.82 to 1.60	0.08
0.064 to 0.188	0.004	1.61 to 4.78	0.10

4.8.8.4 Counterbored Holes. When used to facilitate terminal installation, counterbored holes shall be located a minimum distance of 0.0125 inch (0.32 mm) from all conductive elements, including board edges, plated holes, fasteners, and metal identifiers.

4.8.8.5 Keepout Zones. All counterbored holes shall have a concentric, cylindrical keepout zone 0.025 inch (0.64 mm) greater in diameter than the counterbore, with no encroachment of inner layers or conductors. See Figure 3.7-3.

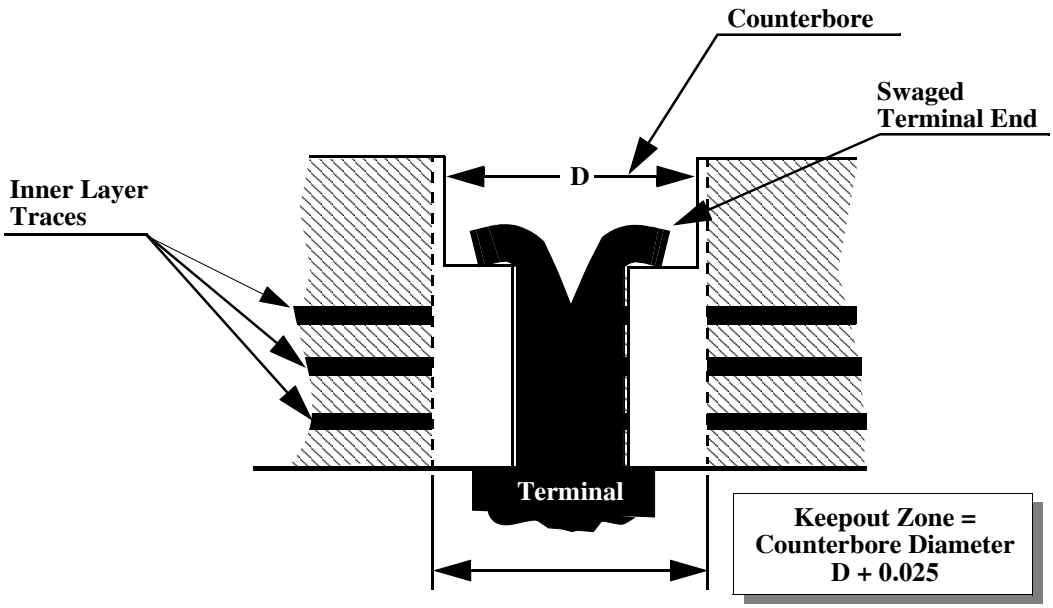

Figure 3.7-3 Keepout Zone

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4.8.8.6 Orientation Tolerance. Terminals shall be oriented within ±10° of the specified orientation.

4.8.8.7 Terminal Restiction. Terminals shall not be installed into PWBs in areas containing acrylic adhesives in the laminate.

4.8.9 Surface Finish. Hot air solder leveling (HASL) shall be the preferred method.

4.8.9.1 Surface Finish for Soldering. Immersion or electroless tin, nickel, or gold shall not be used as a surface finish for soldering.

4.8.9.2 Surface Finish. The method of surface finish on SMT pads or PTHs shall be specified on the drawing.

4.8.9.3 Tin-lead Plate and Fuse. Tin-lead plate and fuse is not recommended. It is prohibited for all surface mount boards, and if used, shall be used in conjunction with trace widths/spacings greater than 0.010 inch and components having a pitch equal to or greater than 0.050 inch. If tin-lead plate and fuse is used, the plating thickness of the tin-lead shall be 0.0003-0.001 inch prior to fusing.

4.8.9.4 Solder Coat and Hot Air Leveling. Solder coating and hot air leveling (HASL) shall be applied after the application of solder mask over bare copper (SMOBC).

4.8.9.5 Final Solder Finish. Solder applied via HASL shall meet IPC Class 3 final finish per IPC-6012, Table 3-2.

4.8.9.6 Hydrosqueegee Prohibition. The hydrosqueegee coating or leveling process shall not be used for flight PWBs.

4.8.10 Solder Mask. There are several important considerations regarding solder mask:

- Solder mask materials;
- Solder mask artwork;
- Solder mask/feature locations;
- Cleaning prior to solder mask application;
- Prohibition against tin-lead under the solder mask.

4.8.10.1 Solder Mask Materials. Solder mask materials shall be selected with one of the materials designated in Table 3.7-7. However, bear in mind that a particular application,

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e.g., the proximity of the electronic box to S/C optics, may make one choice of solder mask more acceptable. If there is a question, consult with the PWB Process Engineer.

Table 3.7-7 Acceptable Solder Mask Materials

Material	Manufacturer	Distributor or Supplier
SR1000 (1-part epoxy) Screenable SM	Polyclad/Enthone (Cookson) Londonderry, NH (800) 366-1185	K.R. Anderson Santa Ana, CA (714) 549-1343
SR2020 (2-part epoxy) Screenable SM	Polyclad/Enthone (Cookson) Londonderry, NH (800) 366-1185	K.R. Anderson Santa Ana, CA (714) 549-1343
Dynamask KM (formerly DynaChem KM) (epoxy-acrylic) Dry film SM	Shipley Ronal Tustin, CA (714) 730-4200	Call Shipley-Ronal Order Entry (714) 730-4200
Vacrel 8140 Dry film SM	DuPont iTechnologies Research Triangle Park, NC (800) 243-2143	Circuit Image Systems Orange, CA (800) 640-2184
Probimer 52 LPI SM	Vantico Inc. Los Angeles, CA (818) 265-7160	Vantico Inc. Customer Service (818) 265-7193
Carapace EMP110 LPI SM (UV bump required)	Electra Polymers Roughway Mill TN11 9SG England UK	Electra Polymers 2914 East Katella Ave. Suite 208 Orange, CA (714) 744-8394
PSR-4000 series LPI SM	Taiyo America, Inc. Carson City, NV (775) 885-9959	Same as manufacturer

4.8.10.2 Solder Mask/Feature Location. Solder mask shall be no nearer than 0.002 inch (0.050 mm) to any feature.

4.8.10.3 Cleaning Prior to Solder Mask Application. All PWBs shall be cleaned prior to solder mask application. The document governing this activity shall be ANSI/IPC-SM-839, *Pre and Post Solder Mask Application Cleaning Guidelines*.

4.8.10.4 Prohibition of Tin-Lead under Solder Mask. There shall be no tin-lead under the solder mask.

4.8.10.5 Solder Mask Dams between Mounting Lands. If a solder mask dam between SMT component mounting pads is desired to prevent solder bridging, a minimum of 0.004

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inch of solder mask + 0.003 inch clearance on each side must be allowed. See Figure 3.7-4. For round BGA mounting pads, only 0.003 of solder mask + 0.003 inch on each side must be allowed. See Figure 3.7-4.

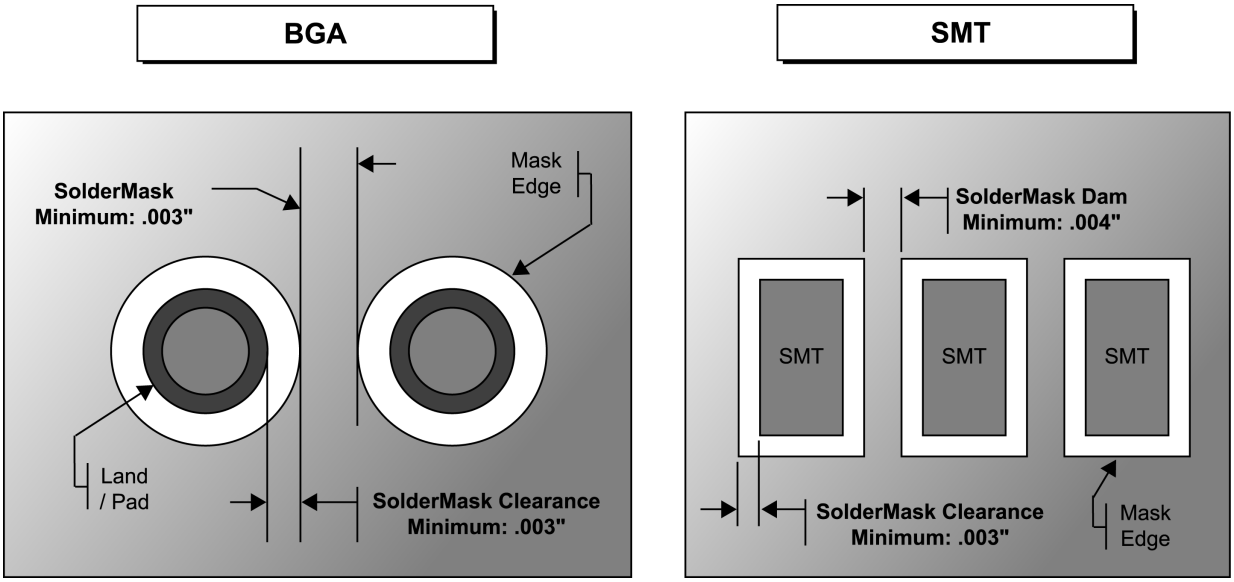

Figure 3.7-4 Solder Mask

4.8.11 Legend Marking Materials. Legend marking (silk screen nomenclature) materials are designated in Table 3.7-8. The required color shall be white unless specified differently on the fabrication drawing.

Table 3.7-8 Acceptable Legend Marking Material

Material	Manufacturer	Distributor or Supplier
Hysol M-Series/Catalyst 20/A Color: white (M-9-N) (2-part epoxy permanent marking ink) (Formerly Wornowink)	Polyclad/Enthone (Cookson) Londonderry, NH (800) 366-1185	K.R. Anderson Santa Ana, CA (714) 549-1343

4.8.11.1 Legend Marking/Feature Location. Legend marking shall be no nearer than 0.007 inch (0.178 mm) to any feature.

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4.8.12 Dielectric Separation between Adjacent Conductive Layers. Separation between conductors on adjacent layers shall be 0.0035 inch minimum and consist of a minimum of two plies of prepreg.

4.8.13 Multilayer Board Construction. If the printed wiring board is a multilayer construction, the following rules shall pertain.

4.8.13.1 Foil Construction versus Core Construction. Two different constructions are used to manufacturing a multilayer board (MLB). These are:

(1) Foil construction;

(2) Core construction.

See Figure 3.7-5 below which illustrates both construction types for an 8-layer MLB. There are advantages and disadvantages of each construction although generally registration control is better with the foil construction.

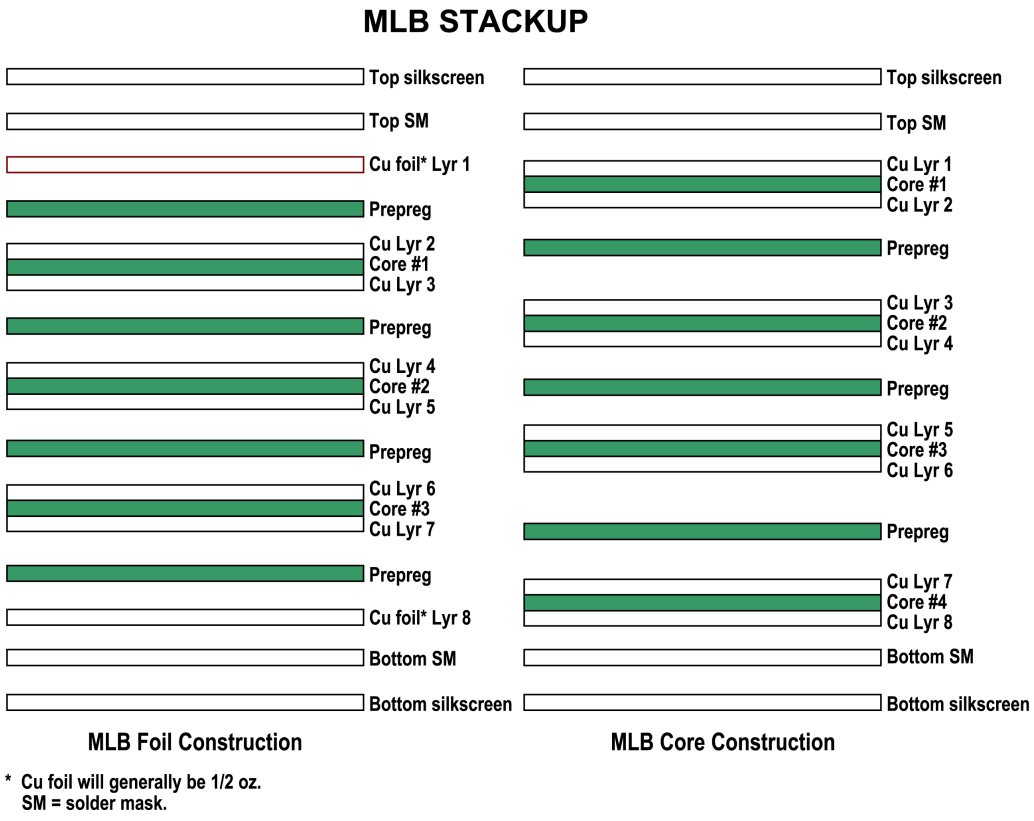

Figure 3.7-5 Foil Construction versus Core Construction.

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Figure 3.7-8 on page 3.7-46 shows a plated through hole in an 8-layer MLB having perfect layer-to-layer registration. It also shows etchback (see 4.8.2.10) and copper plating (see 4.8.2.6) that exhibits the normal pattern of heavier plating at the two ends of the hole and less heavy plating in the middle. Figure 3.7-9 on page 3.7-47 shows a plated through hole showing layer-to-layer misregistration.

4.8.13.2 Multilayer Board Thickness. To estimate the thickness of a MLB, the following heuristic guidelines can be given.

Assume each dielectric layer to be 0.005 inch. This includes both core and prepreg dielectric. The following copper thicknesses can be used for estimation purposes:

- 1/2 oz. Cu = 0.0007 inch;
- 1 oz. Cu = 0.0014 inch;
- 2 oz. Cu = 0.0028 inch.

Plating on the top and bottom layers will add an extra 0.005 inch roughly. Solder mask on the top and bottom layers will add an extra 0.002 inch roughly. Therefore, for the MLB depicted in Figure 3.7-5 above, assuming that the top and bottom copper layers are 1/2 oz. copper and all other copper layers are 1 oz. copper, the thickness as calculated from the above rules is:

$$\text{Thickness} = 0.002\ (\text{SM}) + 0.005\ (\text{plating}) + 7\ (\text{dielectrics}) \times 0.005 + 6\ (1\text{ oz. Cu}) \times 0.0014 + 2(1/2\text{ oz. Cu}) \times 0.0007 = 0.052\text{ inch}$$

If a tighter thickness is needed, discuss with the PWB Process Engineer if the dielectric layer can be taken to be 0.004 inch rather than 0.005 inch.

4.8.13.3 Multilayer Board Thickness Tolerance. The overall thickness tolerance should be +/-10% and shall be expressed in inch on the drawing. For the MLB illustrated above, the fabrication drawing shall read 0.052 +/-0.005.

4.8.13.4 Symmetrical Stackup. When designing the stackup, the designer should be cognizant that the materials utilized in MLB constructions are subject to shrinkages and material distortions as the copper is etched off the layers. The more copper that is removed from a layer, the more material shrinkage is experienced due to the relief of stresses pent up within the copper clad laminate material. Therefore, a core that has signal-signal (S-S) will shrink much more (relatively speaking) that a core that has plane-plane (P-P).

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As an example, assume the stackup is as follows for a 10-layer MLB (assuming foil construction):

S (lyr 1 = outer layer)

prepreg

S-S (lyrs 2-3 = inner layer)

prepreg

S-S (lyrs 4-5 = inner layer)

prepreg

S-S (lyrs 6-7 = inner layer)

prepreg

P-P (lyrs 8-9 = inner layer)

prepreg

S (lyr 10 = outer layer)

Of the four inner layers, the three S-S layers will shrink at pretty much the same rate; whereas the P-P layer will shrink much less due to there being much more copper on this inner layer. Hence, it will subsequently be harder to hold adequate registration during the drilling and lamination processes.

A much more symmetrical construction would be the following:

S (lyr 1 = outer layer)

prepreg

P-S (lyrs 2-3 = inner layer)

prepreg

S-S (lyrs 4-5 = inner layer)

prepreg

S-S (lyrs 6-7 = inner layer)

prepreg

S-P (lyrs 8-9 = inner layer)

prepreg

S (lyr 10 = outer layer)

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Consult with the PWB Process Engineer if there is a question.

4.8.14 Controlled Emissions. The following points are made regarding controlling the RF emissions from signal and power and ground layers. See Figure 3.7-6.

- The most effective way of controlling emissions from the signal traces is to locate them as closely as possible to their reference planes.
- The most effective way of controlling emissions from the reference planes is to locate them as closely as possible to each other.

Since both of these recommendations cannot always be realized simultaneously, the first takes precedence over the second. Controlling emissions from the reference planes, if they cannot be located as close as possible, can be accomplished by using by-pass capacitors.

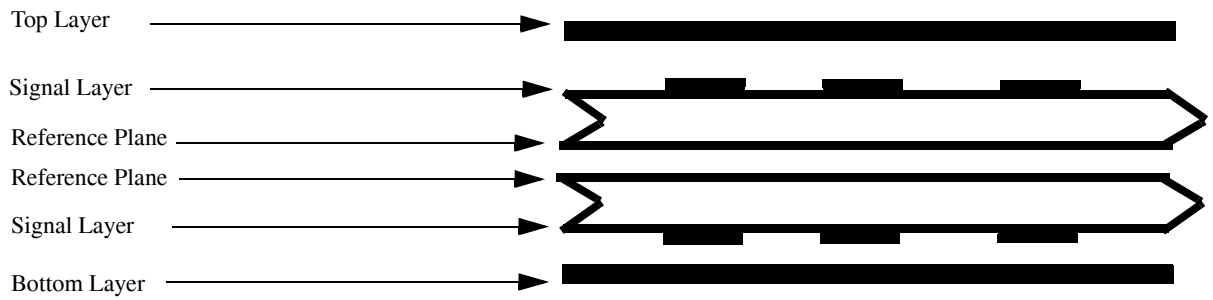

Figure 3.7-6 MLB Showing Signal Layers and Reference Planes

4.8.15 Controlled Impedance MLB Construction. As frequencies increase, traces increasingly take on the properties of transmission lines. Under these circumstances, it is important to understand the properties of controlled impedance (Z_o).

4.8.15.1 Controlled Impedance PWBs-Design. The four types of controlled impedance boards are microstrip, embedded microstrip, stripline, and dual stripline. For design information, refer to Section 6.4, pp. 40-43, of IPC-2221, *"Generic Standard on Printed Board Design,"* for further details.

4.8.15.2 Controlled Impedance PWBs-Fabrication. There are several important considerations to keep in mind regarding the successful fabrication of controlled impedance MLBs.

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Below are four parameters that are critical and must be carefully controlled (also see Figure 3.7-7 below):

- Dielectric constant (Er, εr or DK). This is a function of the choice of material used. Some materials, such as polytetrafluoroethylene (PTFE: Teflon, Duroid, etc.) have low Ers. For example, PTFE has a dielectric constant somewhere in the range of 2.5. The Er of polyimide is about 4.0. However, PTFE is not the easiest material to process. This parameter is based on the choice of materials. Unless specified otherwise on the drawing, polymide is the material to be used for flight-controlled impedance MLBs.
- The width of the trace, w. This is a critical feature of a controlled impedance board. The etching process is critical in keeping the side walls of the trace as straight as possible. A precision spray etching machine is critical. The etch factor that the fabricator can achieve is more controllable during the etch process if a lighter weight copper is used, e.g., 1/2 oz., 1/4 oz., etc. This parameter is subject to control by the PWB fabricator.
- The thickness of the trace, t. It is also important to control the thickness. If the weight of copper is too thin, in the inner layers it may become buried by the prepreg material. This parameter is subject to control by the PWB fabricator.
- The distance of the bottom of the trace to the reference plane, h. To control h, make sure that the signal trace and its corresponding reference plane are located on the same piece of core material. This parameter is subject to control by the PWB fabricator.

Given what was said above about the four critical parameters, the following can be said about each one's affect on the controlled impedance:

- Increase the dielectric constant, Er (or DK), will decrease the controlled impedance;
- Increase the trace width, w, will decrease the controlled impedance;
- Increase the trace thickness, t, will decrease the controlled impedance;
- Decrease the distance of the bottom of the trace to the reference plane, h, will decrease the controlled impedance.

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In general, the nominal dielectric constant, Er, of the material is used for the value of Er in making controlled impedance calculations. See Table 3.7-4 as a reference. For the value of w, as a first pass, use the value that is given in the drawing. The trace thickness, t, depends on the copper weight used. However, remove 0.0002 inch due to processing.

- 1/2 oz. Cu = 0.0007 - 0.0002 = 0.0005 inch;
- 1 oz. Cu = 0.0014 - 0.0002 = 0.0012 inch;
- 2 oz. Cu = 0.0028 - 0.0002 = 0.0026 inch.

The designer should bear in mind, however, that the formulas for calculating the controlled impedance (Z_o) are complicated, so a good software program for calculating controlled impedance should be used.

4.8.15.3 Controlled Impedance PWBs-Testing. Make sure that the fabricator has time domain reflectometry (TDR) testing capabilities to test the achieved impedance. This will help in adjusting the process parameters to achieve the desired controlled impedance. A suitable coupon for controlled impedance shall be used when the PWB is a controlled impedance PWB. The PWB vendor shall supply this coupon and position it on a suitable place on the panel during PWB manufacture.

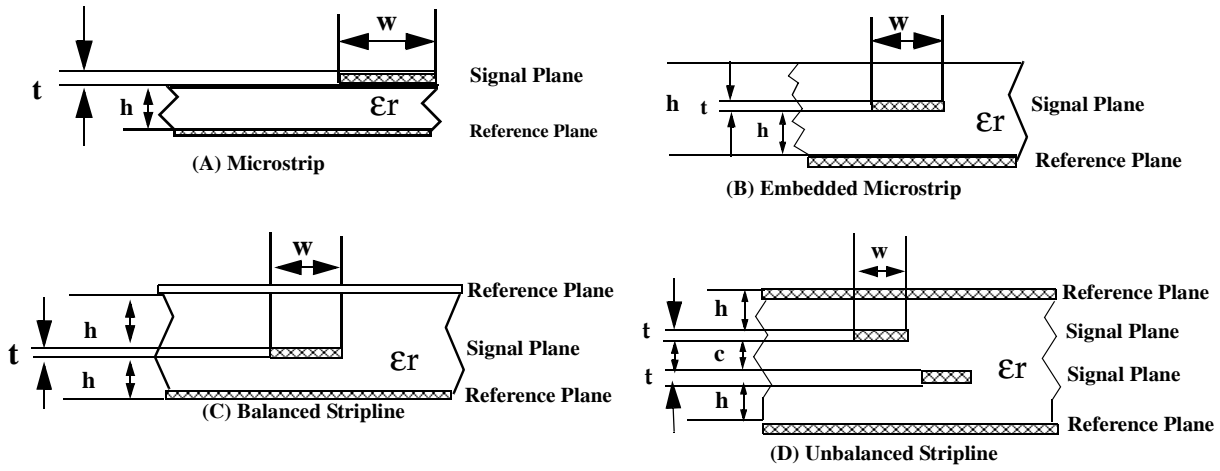

Figure 3.7-7 Transmission Line Printed Board Constructions: w, t, and h

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4.9 Fabrication Drawing

4.9.1 Fabrication Drawing. The following items shall be found on the fabrication drawing.

- Fabrication drawing notes (see paragraph 4.9.1.1 below).
- The hole block, including all plated and unplated holes. The hole block should also give tolerances for all holes. The sizes specified shall be for the finished hole. The hole chart shall also specify which holes are to be filled, if any. The hole block shall also clearly specifiy what holes are blind holes and what holes are buried holes, if there are such holes in the PWB in question.
- A drawing depicting the board dimensions, including the overall thickness and thickness tolerance. All dimensions and tolerances shall be per ANSI Y14.5.
- If an MLB, a layer-by-layer stackup drawing shall be depicted, including an insulation board (if any). The stackup shall also depict the solder mask layer(s) and the silkscreen layer(s). A symmetrical layer build-up is highly preferred. See Figure 3.7-5 and paragraph 4.8.13.4.
- The fabrication drawing shall have the file extensions associated with each layer, including silkscreen and solder mask, used as labels for the stackup layers along with the layer names.
- The fabrication drawing shall locate the origin of the coordinate system and be consistent with the netlist. The coordinate system shall be shown on the drawing.
- Any other special features.

4.9.1.1 Fabrication Drawing Notes. At minimum, the fabrication drawing notes shall contain the following:

- The type of PWB shall be called out on the fabrication drawing. See 1.3 above.
- PWB laminate material, including both cores and prepregs. The weight of copper shall be specified for all core materials called out. See paragraph 4.7 above.
- Minimum trace width/spacings (given for quotation purposes).

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- Surface finish. If any surface finish other than HASL is to be used, it shall be called out on the drawing. See paragraph 4.8.9
- Solder mask callout. See paragraph 4.8.10 above. If solder mask is used, no solder shall be permitted under the solder mask.
- Legend ink. See paragraph 4.8.11 above.
- Hole fill. See paragraph 4.8.2.8 above.
- PWB identification. Identify all boards per paragraph 4.5 above.
- Maximum bow and twist shall not exceed 0.75% for SMT boards and 1.0% for all other boards.
- Just prior to the application of solder mask, one board per lot shall be cleaned and tested for cleanliness using a suitable ionic contamination tester and the result documented. The ionic contamination level shall not exceed 10 micrograms per square inch (10 $\mu g/in^2$). Each side of the board contributes to the total area in square inches. If the board fails, the entire lot shall be recleaned, and the test repeated until the board passes the test. See paragraph 4.8.10.3 above and paragraphs 5.3.10 and 5.3.10.1 below.
- All boards shall be packaged for shipment following paragraph 5.3.19 below.

See Table 3.7-9 for an example of fabrication drawing notes. These notes are for guidance only. The particular PWB under consideration may require a different set of notes.

Table 3.7-9 Example of Fabrication Drawing Notes

NOTES: UNLESS OTHERWISE SPECIFIED	Applicable Paragraph Number(s) in Section 3.6
19. ALL SECTIONS AND SUBSECTIONS REFERRED TO IN THIS DOCUMENT ARE PER JPL SPECIFICATION D-8208.	N/A
20. THIS DOCUMENT AND RELATED ARTWORK ARE COMPUTER GENERATED. CHANGES ARE TO BE PERFORMED ON THE ORIGINAL DATABASE ON FILE IN SECTION 349.	N/A
21. FABRICATE PRINTED WIRING BOARD PER SECTION 3.6.	1.4
22. FOIL CONSTRUCTION SHALL BE EMPLOYED FOR MULTILAYER CONSTRUCTION.	5.3.6

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Table 3.7-9 Example of Fabrication Drawing Notes (Continued)

NOTES: UNLESS OTHERWISE SPECIFIED	Applicable Paragraph Number(s) in Section 3.6
23. COPPER PLATING IN HOLES SHALL BE 0.0015 INCH NOMINAL THICKNESS WITH NO SINGLE READING LESS THAN 0.001 INCH.	4.8.2.4; 5.3.9.1
24. NEGATIVE ETCHBACK SHALL BE PROHIBITED.	4.8.2.9; 5.3.9.3
25. POSITIVE ETCHBACK SHALL BE 0.0002-0.002 INCH; 0.0005 INCH IS PREFERRED. PLASMA DESMEAR/ETCHBACK IS THE PREFERRED METHOD.	4.8.2.8; 5.3.2.9
26. LAYER-TO-LAYER REGISTRATION SHALL NOT EXCEED 0.010 INCH ON MULTILAYER PWBs 10 LAYERS OR LESS, AND IT SHALL NOT EXCEED 0.010 INCH + 0.001 INCH FOR EACH ADDITIONAL LAYER OVER 10. FOR EXAMPLE, IT SHALL NOT EXCEED 0.014 INCH FOR A 14 LAYER MULTILAYER PWB.	5.3.6.2
27. THE EXTERNAL ANNULAR RING SHALL BE AT LEAST 0.002 INCH, AND THE INTERNAL ANNULAR RING SHALL BE AT LEAST 0.001 INCH.	4.8.2.3; 5.3.9.4
28. IONIC CONTAMINATION SHALL BE MEASURED ON ONE BOARD PER LOT* DIRECTLY PRIOR TO THE APPLICATION OF SOLDER MASK AND SHALL NOT EXCEED 10 MICROGRAMS PER SQUARE INCHES. TEST DOCUMENTATION SHALL BE DELIVERED WITH THE BOARD. THE BOARD USED FOR IONIC CONTAMINATION TESTING SHALL BE BAKED AT 125 F FOR 20 MINUTES PRIOR TO APPLICATION OF SOLDER MASK	5.3.10.1
29. APPLY ITEM X† SOLDER MASK TO TOP AND BOTTOM OVER BARE COPPER, COMPONENT PADS TO BE FREE FROM BLEEDING OR MISREGISTRATION.	4.8.10.1; 5.3.11
30. AFTER APPLICATION OF SOLDER MASK, APPLY SOLDER COAT OVER BARE COPPER USING HOT AIR LEVELING (HASL). SOLDER THICKNESS AT CREST TO BE 0.00015 TO 0.002 INCH. THERE SHALL BE NO SOLDER UNDERNEATH SOLDER MASK.	4.8.9; 4.8.10.4; 5.3.11; 5.3.12
31. SEPARATION BETWEEN CONDUCTORS ON ADJACENT LAYERS SHALL BE 0.0035 INCHES MINIMUM AND CONSIST OF A MINIMUM TWO PLIES OF PREPREG.	4.8.13; 5.3.6.1
32. LEGEND OVER SOLDER MASK ON BOTH SIDES OF PWB USING HYSOL M-SERIES/CATALYST 20/A WHITE EPOXY INK. LEGEND MARKING SHALL BE NO NEARER THAN 0.005 INCH TO ANY SOLDER PAD OR VIA HOLE. INK STAMP REVISION LETTER AND SERIAL NUMBER USING HYSOL M-SERIES/CATALYST 20/A WHITE EPOXY INK. CHARACTER HEIGHT SHALL BE 0.050 INCH (MINIMUM).	4.8.11; 4.8.11.1; 5.3.13
33. CONTINUITY AND SHORTS TESTING USING A SUITABLE NETLIST TESTING DEVICE SHALL BE PERFORMED ON EACH PWB, AND THE DOCUMENTATION DELIVERED WITH THE FINISHED PWB. SHORTS TESTING SHALL BE AT A MINIMUM OF 200 VOLTS D.C.	4.4.1; 5.3.15

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Table 3.7-9 Example of Fabrication Drawing Notes (Continued)

NOTES: UNLESS OTHERWISE SPECIFIED	Applicable Paragraph Number(s) in Section 3.6
34. THERE SHALL BE A MINIMUM OF TWO COUPON STRIPS FOR EACH PANEL PRODUCED. EACH STRIP SHALL AT A MINIMUM CONSIST OF A AND B COUPONS, AND EACH STRIP SHALL BE PLACED AT ONE OF THE CORNERS DIAGONALLY ACROSS FROM THE OTHER STRIP AND AT RIGHT ANGLES FROM THE OTHER STRIP AND BE LOCATED NO MORE THAN 0.250 INCH FROM A BOARD ON THE PANEL.	4.6; 4.6.1; 5.3.2
35. BOW AND TWIST SHALL NOT EXCEED 0.75%.	5.3.17
36. MATERIALS USED SHALL BE TRACEABLE TO THE MANUFACTURER'S LOT. CERTIFICATION SHALL BE SUPPLIED WITH ALL TEST DATA.	6.2

* PWB LOT = A lot consists of those PWBs processed at the same time and under the same conditions. The lot may consist of one panel or several panels.

† ITEM X = One of the acceptable solder mask materials. See Table 3.7-7.

4.9.1.2 Released Drawing. Prior to the initiation of the PWBs, the master fabrication drawing (often called simply the fab drawing) shall be released. See 4.10 below.

4.10 Design Output

The following items shall normally constitute the output from the PWB design effort. All electronic files should be zipped together into one ZIP file for convenience of handling and for electronic transmission. This ZIP file shall be placed in the Product Data Management System (PDMS) for all flight hardware.

Note: PDMS is replacing the vellum file service for all new projects. Most older drawings are also being converted into the PDMS.

- A complete set of Gerber files containing a Gerber file for each layer of the PWB. It is the responsibility of the designer to ensure that the file extension outputs of his/her CAD system are used to label the different layers of the stackup on the fabrication drawing. See 4.9.1.
- Gerber file(s) for the legend to identify reference designators, etc. Legending is also known as silk screening, so these are generally referred to as the silk screen Gerber files. Two are required if the board has legends on both the top side and the bottom side.
- It is preferred that the Gerber files be on the same 0,0 as the IPC-D-356A file.

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- Gerber file(s) for solder mask. Two are required if the board is to have solder mask on both the top side and the bottom side.
- If the board is an SMT PWB, Gerber file(s) for the stencil. These are generally referred to as the solder paste Gerber files. Two are required if the board is to have surface mount components on both the top side and the bottom side.
- If hole fill is being done and the holes to be filled are not indicated clearly and unambiguously on the hole chart, then the designer shall supply a fill file.
- It is preferred that a route file be provided. The center of the line shall be used as the board edge. All cutouts and slots should also be part of the route file.
- An aperture file containing the aperture list. If an extended Gerber RS-274X file is employed in which the aperture shapes are already embedded, this file is then superfluous. It is highly preferred that a Gerber RS-274X file be supplied.
- A drill file containing the drill program. It is preferred that an Excellon 2 Format plus M48 Header file be supplied. There should be a separate drill file for all holes in the PWB. There should be a drill file for all plated through holes, a drill file for non-plated through holes, a drill file for each set of buried vias (if the PWB has these), a drill file for each set of blind vias (if the PWB has these), etc.
- An electronic version of the fabrication drawing in pdf format. For flight hardware, this drawing shall be a reference copy of the released drawing.
- An electronic version of the assembly drawing in pdf format. For flight hardware, this drawing shall be a reference copy of the released drawing.
- A PDMS version of the fabrication drawing shall be available. For flight hardware, this drawing shall be a released drawing. The hardcopy version shall be generated from the computer database.
- A PDMS version of the assembly drawing shall be available. For flight hardware, this drawing shall be a released drawing. The hardcopy version shall be generated from the computer database.

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- IPC-D-356A file of the netlist generated directly from the design database. It is the responsibility of the designer to ensure the creation of the IPC-D-356A file. If his/her system does not create this as a normal output, the designer should negotiate with the cognizant engineer to arrange to have this done. See paragraph 4.4.3. Once the IPC-D-356A file has been generated from the design database, it shall not be modified.
- A Read-Me file containing the following:
  - Name of all files with a brief verbal description of each file.
  - Any other pertinent information required to plot the artwork and manufacture the board, including such items as:
    - List of intentional shorts;
    - Special layers identified, such as hole fill layers;
    - Identification of special pads and symbols;
    - Comment out test points left open in mask;
    - Special grounding situations;
    - All exceptions to D-8208.

It shall be the responsibility of the designer to perform design rule checks (DRCs) on the design package before it is released and to perform a final quality check on the design.

5 FABRICATION REQUIREMENTS

The fabrication requirements for all JPL printed wiring boards (PWBs) shall be per the IPC-6011 (1999), *"Generic Performance Specification for Printed Boards."* Regarding the fabrication requirements for the rigid portion of rigid flex printed wiring boards, the chief document, in addition to IPC-6011, is IPC-6012 (1999), *"Qualification and Performance Specification for Rigid Printed Boards."* Regarding the fabrication requirements for the flex portion of rigid flex printed wiring boards and flex printed wiring boards, the chief document, in addition to IPC-6011, is IPC-6013 (1999), *"Qualification and Performance Specification for Flexible Printed Boards."* Exceptions to these two documents for flight PWBs are detailed in this section.

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5.1 Order of Precedence

In the event of a conflict between the procurement document(s), this specification, the fabrication drawing, and/or any other documentation, the following order of precedence shall pertain:

- Purchase Order (P.O.) or Contract with the vendor;
- Master fabrication drawing;
- This specification;
- IPC-6012, *"Qualification and Performance for Rigid Printed Boards;"*
- IPC-6011, *"Generic Performance Specification for Printed Boards."*

5.2 Performance Class

The performance class shall be IPC Class 3, High-Reliability Electronic Products.

5.2.1 Pre-Fabrication Inspection. Travelers may be reviewed and submitted to JPL prior to starting the PWB fabrication. If necessary, plotted artwork films may also be reviewed. The JPL PWB Process Engineer and/or JPL QA will decide if this is necessary.

5.2.2 Board Type. Board Types 1 through 4 shall be acceptable for JPL use. See 1.3 above. The type of PWB and the use will be called out on the fabrication drawing.

5.3 Fabrication Requirements—Flight PWBs

5.3.1 Acceptance Criteria. ANSI/IPC-A-600E, "Acceptability of Printed Wiring Boards," shall be used as acceptance criteria using Class 3 acceptability level.

5.3.2 Coupons. The necessary coupons shall be plotted on all artworks as appropriate. See 4.6 above. If the PWB is a controlled impedance PWB, the vendor shall supply this coupon and position it on a suitable place on the panel during PWB manufacture. See 4.8.15.3.

5.3.3 Artworks to be Sent to JPL. After the vendor has performed the front-end engineering activities on the Gerber files and the Gerber files have been photoplotted, the artwork inspected, and the production phototools produced, the vendor shall send duplicate top layer artwork film and the top silk screen (legend) artwork film to the PWB Process Engineer at JPL at MS 103-106. If the PWB is an SMT PWB, the vendor shall also include the solder paste artwork film for the top layer and the bottom layer (if applicable). Diazo phototools are acceptable. If the board has components on the bottom side, the vendor shall also send the bottom layer artwork film and the bottom silk screen

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(legend) artwork film to the PWB Process Engineer at JPL. These artwork films will be used by assembly engineers as an aid in planning the PWB assembly operation.

5.3.4 Panelization. The most expeditious panel size shall be used to build JPL PWBs. The panel size shall take into account the dimensional stability of the material and layer-to-layer registration.

5.3.5 Inner Layer Inspection of MLBs. All inner layers shall be 100% inspected using AO1 prior to the lamination process. This requirement may be waived at the discretion of the PWB Process Engineer and JPL QA. The wainver shall be in written form to the PWB vendor. It is highly preferred that the AO1 machine be CAD-driven. All defective inner layers shall be discarded.

5.3.6 MLB Lamination. Unless otherwise specified on the fabrication drawing, foil constructions shall be allowed. All MLBs shall be symmetrical. For buried and/or blind vias, the MLB shall be built using sequential lamination techniques.

5.3.6.1 Dielectric Separation Between Conductor Layers. Dielectric separation between conductor layers shall be a minimum of 0.0035 inch (0.089 mm) and shall be attained by the use of a minimum of two plies of prepreg.

5.3.6.2 Layer-to-Layer Registration. Layer-to-layer registration shall not exceed 0.010 inch in multilayer PWBs (MLBs) 10 layers or less, and it shall not exceed 0.010 + 0.001 inch for each additional layer greater than 10. For example, it shall not exceed 0.014 inch for a 14-layer MLB. This requirement is to be used in conjunction with that of annular ring. See paragraph 5.3.9.4 below. See Figures 3.7-8 and 3.7-9 for examples of layer-to-layer perfect registration and misregistration.

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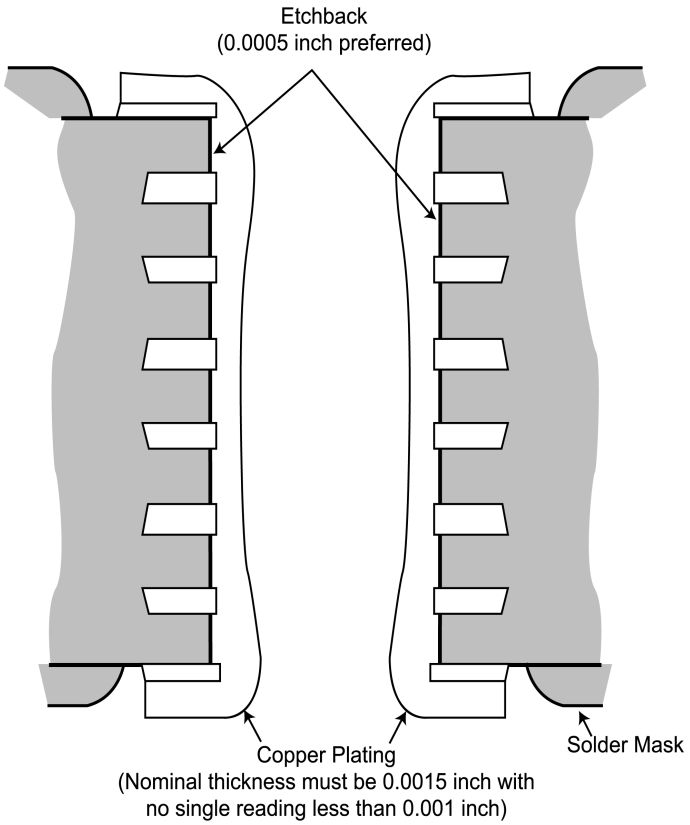

Figure 3.7-8 8-Layer MLB Showing Perfect Layer-to-Layer Registration

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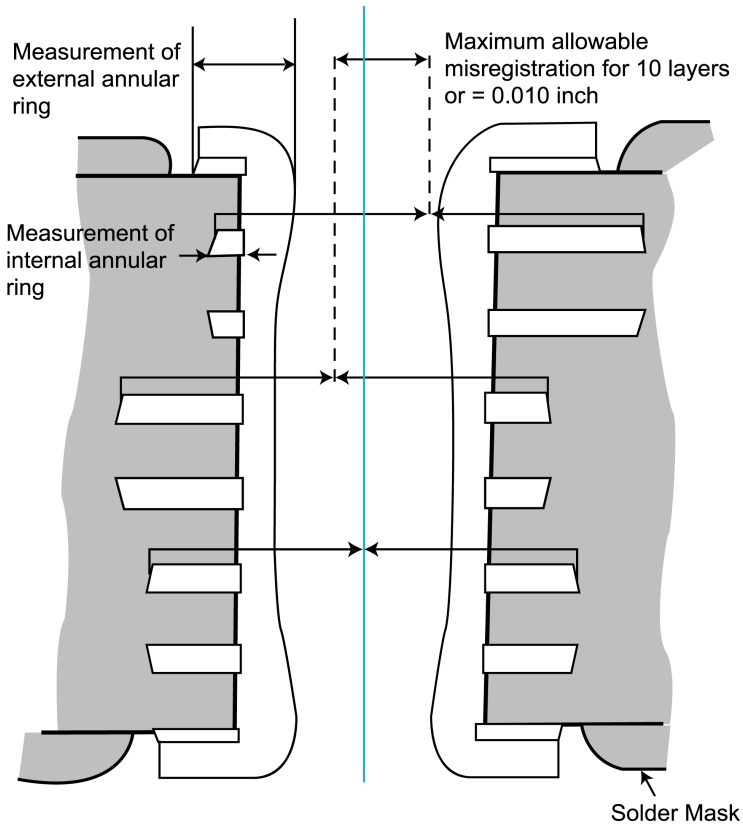

Figure 3.7-9 8-Layer MLB Showing Layer-to-Layer Misregistration and Measurement of Annular Ring (External and Internal)

5.3.6.3 Tooling System for Dimensional Stability. For the flex portion of rigid flex PWBs or for flex PWBs, the vendor shall demonstate that he/she has an adequate tooling system in place to assume proper dimensional stablity.

5.3.7 Drilling. A suitable entry and backup material shall be used for drilling PWBs. Only one PWB shall be used per drill stack-up. A maximum of 500 hits is allowed per drill bit; after that the bit must be replaced. Resharpened drill bits shall not be allowed. A drill first article shall be used for each lot.

5.3.8 MLB Registration. An adequate tooling system shall be employed to ensure proper MLB registration. In addition, it is highly recommended that the PWB vendor employ a

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real-time X-ray system for viewing layer stackups to ensure good registration of the MLB.

5.3.9 PTHs and Vias. The following pertain to plated-through-holes and plated vias.

5.3.9.1 Copper Plating. Copper plating on the wall of the plated through hole (PTH) and plated vias shall be 0.0015 inch (0.038 mm) nominal with no single reading less than 0.001 inch (0.025 mm). See Figure 3.7-8.

5.3.9.2 Etchback. There shall be etchback between 0.0002-0.001 inch (0.005-0.026 mm); 0.0005 (0.013 mm) inch is preferred. Plasma desmear/etchback is the preferred method. See paragraph 4.8.2.10 above.

5.3.9.3 Negative Etchback. Negative etchback of the copper shall be prohibited.

5.3.9.4 Annular Ring. IPC-6012 for Class 3 PWBs shall be followed for PTH vias (see Table 3.5 in IPC-6012). For PTHs used for component through-holes (e.g., connectors) the external annular ring shall be a minimum of 0.005 inches (0.128 mm) and the internal annular ring shall be a minimum of 0.002 inches (0.051 mm). All such PTHs used as component through-holes shall be clearly identified on the drawing. If not so identified, the PWB manufacturer shall follow IPC-6012, Class 3 PWBs regarding annular ring. For measurement of annular ring see Figure 3.7-9.

5.3.9.5 Buried and Blind Vias. PWBs with buried and blind vias shall be produced by sequential lamination techniques.

5.3.9.6 Via Fill. If required (see paragraphs 4.8.2.8 and 4.8.2.9 above), all empty vias shall be filled with an acceptable hole fill material. See Table 3.7-5 above.

5.3.10 Cleaning Prior to Solder Mask Application. All PWBs shall be cleaned prior to solder mask application. The document governing this activity shall be ANSI/IPC-SM-839, *"Pre and Post Solder Mask Application Cleaning Guidelines."*

5.3.10.1 Ionic Contamination Testing. Just prior to the application of solder mask, one board per lot shall be cleaned and tested for cleanliness using a suitable ionic contamination tester and the result documented. The ionic contamination level shall not exceed 10 micrograms per square inch (10 $\mu g/in^2$). Each side of the board contributes to the total area in square inches. If the board fails, the entire lot shall be recleaned, and the test repeated until the board passes the test.

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5.3.11 Solder Mask. The solder mask to be used shall be one of the mask materials designated in 4.8.10 above.

5.3.12 Surface Finish. The method of surface finish on surface mount pads or PTHs shall be specified on the drawing, and the PWB vendor shall consult the drawing. If the method of surface finish is not called out in the drawing, the method used shall be HASL.

5.3.13 Legend Ink. The legend ink to be used shall be that designated in 4.8.11 above.

5.3.14 Insulation Board. If an insulation board is called for on the drawing, it shall be of the same material as the PWB itself.

5.3.15 Electrical Test. Electrical test shall be performed on all PWBs per 4.4.1 above. In addition, a netlist comparison test shall be performed between the IPC-D-356A file generated from the design database and the Gerber extracted netlist file. See 4.4.1.1 above.

5.3.16 Rework. Minor rework, such as the use of an Exacto knife to rework shorts, shall be allowed. Repair of PWBs, such as the use of resistance welding to repair opens, shall not be allowed.

5.3.17 Maximum Bow and Twist. Maximum bow and twist shall not exceed 0.75% for SMT boards and 1.0% for all other boards.

5.3.18 Serialization and Board Identification. Each individual PWB shall be given a unique serial number following paragraph 4.5. Normally, the serial number (S/N) will begin at 001, 002, 003, etc. unless specific directions indicate otherwise. The serial numbers shall be legible and easy to read. In addition, the PWB vendor shall place his company name somewhere on each PWB to easily identify the company that manufactured the PWBs.

5.3.19 Handling & Packaging/Shipping. All completed PWBs shall be handled by their edges to avoid contamination and damage. All completed PWBs shall be bagged in ESD Barrier Bags; one PWB per bag. Then the PWBs in their respective ESD Barrier Bags are to be suitably packaged in padded envelopes to avoid damage.

5.3.19.1 Pickup at the Vendor. If convenient, the completed PWBs will be picked up at the PWB facility by either the PWB Coordinator or the QA Representative and hand carried back to JPL.

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5.3.19.2 Shipping to JPL. If it is not feasible due to time and/or distance constraints to pick up the completed PWBs, they shall be shipped by a carrier that ensures overnight delivery so that they can be received by JPL the following day.

5.3.20 Chief Fabrication Requirements. The chief fabrication requirements for JPL flight PWBs are summarized in Table 3.7-10. In the case of test PWBs, the following requirements shall still pertain:

- Electrical test of 200 Vdc;
- Desmear and etchback;
- ESD bag individually;
- Unique serial number required.

Note: If the CogE knows that the test PWB will lead into a flight PWB, he/she should consider whether some or all of the fabrication requirements for flight PWBs should be invoked.

In certain cases, to ensure adherence to the agreed-upon build schedule and to understand why slippages occur, more stringent management techniques such as a Status Tracking Matrix may be required of the PWB vendor. If necessary, consult with the PWB Process Engineer.

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Table 3.7-10 Chief Fabrication Requirements for JPL Flight PWBs

Fabrication Requirements	Yes	No	Comments
Electrical test, netlist, 200 Vdc	X		Must be netlist tested from an IPC-D-356A file generated directly from the design database, and this netlist shall be compared to the extracted netlist*
Desmear required	X		Plasma preferred method
Etchback	X		0.0002-0.001 inch; 0.0005 inch preferred
MLB lamination	X		Foil construction preferred unless otherwise specified
Dielectric separation between adjacent conductive layers	X		A minimum of 0.0035 inch attainable by the use of a minimum of two plies of prepreg
Annular ring	X		IPC-6012, Class 3
Standard surface finish	X		HASL unless otherwise specified
Copper plating in PTHs/vias	X		0.0015 inch nominal; no single reading < 0.001inch
Ionic contamination testing	X		One PWB per lot directly prior to SM application; reading must be < 10 µg/in^2
Approved solder mask (SM) material	X		See Table 3.7-7
Via fill (only required for PWBs with a backing board or blind/buried vias unless called out on the fabrication drawing)	X		See Table 3.7-5
JPL I/L and final source	X		Must be done at vendor's facility
ESD bag individually	X		ESD Barrier Bag
Unique Serial Number Required	X		For example, 001, 002, etc. On top of the PWB if room permits
Coupons Required	X		See Table 3.7-3
Microsections to be shipped with order	X		A and B microsections

*. The IPC-D-356A file shall be supplied to the PWB vendor along with the Gerber files and other appropriate files, such as the drill file, etc., in the ZIP file.

5.3.21 JPL QA Source Inspections. All flight PWBs shall have the following JPL QA source inspections:

- Inner layer (I/L);
- Final.

See paragraph 6.1.4 below.

JPL QA shall be notified, at a minimum twenty-four hours in advance, that the boards are ready for source. To perform this function, the PWB vendor shall email the following individuals at JPL:

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- QA Lead person in Electronic Packaging and Fabrication or his/her designated representative;
- QA Inspector normally involved with PWB source inspection;
- PWB Coordinator;
- PWB Process Engineer.

The prime point-of-contact at each PWB facility approved to build flight PWB hardware for JPL shall be given the names, email addresses, and phone numbers of the above individuals. If the list changes in any way, the point-of-contact shall receive an updated list.

Once the email is sent to the above individuals at JPL, the QA Inspector normally involved with PWB source inspection shall call the PWB vendor to verify that he/she will be there for source at the designated time. If the QA Inspector normally involved with PWB source inspection fails to call the PWB vendor within four (4) hours of the expected source, then the PWB vendor shall call either the PWB Coordinator or the PWB Process Engineer and inform them of this fact.

5.4 Fabrication Requirements-Terminal Boards

5.4.1 Terminals. Terminal installation into plated through-holes shall be per the requirements of ANSI/IPC-J-STD-001B and nonplated through-holes per the following requirements.

5.4.1.1 Physical Defects. Any of the following physical defects shall be cause for rejection:

- Split or bent tines;
- Split or cracked terminal holes;
- Delaminated base material;
- Altered spacing between bifurcations.

5.4.1.2 Orientation Tolerance. Terminals shall be oriented within ±10° of the specified orientation.

5.4.1.3 Perpendicular Tolerance. Terminal shall be perpendicular to the plane of the board within ±5°, measuring at the bottom of the tines and/or the terminal center.

5.4.1.4 Seating Tolerance. The entire base of the terminal shall rest against the wiring board, etched conductor, or terminal pad.

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5.4.1.5 Tightness. After swaging prior to soldering, terminals shall be tight enough that they cannot be rotated by hand.

5.4.1.6 Concentricity. The swaged flange shall be concentric to within 0.010 inch (0.25 mm) of the terminal centerline.

5.4.1.7 Swaging. Any of the following swage defects shall be cause for rejection. See Figure 3.7-10.

- Terminal swage more than 0.012 inch (0.030 mm) above the plane of the board;
- Funnel-type swage;
- More than two cracks in the terminal flange;
- Radial splits or cracks extending into the shank;
- More than two radial splits or cracks or two cracks less than 90° apart;
- Hairline cracks extending through the thickness of the flange;
- Roll-over edge more than 0.004 inch above board surface.

5.4.1.8 Measling or Crazing. Measling or crazing caused by terminal installation shall be acceptable provided they do not form a continuous path between conductors or a continuous area or path extending more than 0.060 inch from the terminal.

5.4.1.9 Terminal Soldering. Terminals swaged into circuit interconnection conductors shall be soldered. See Figure 3.7-11.

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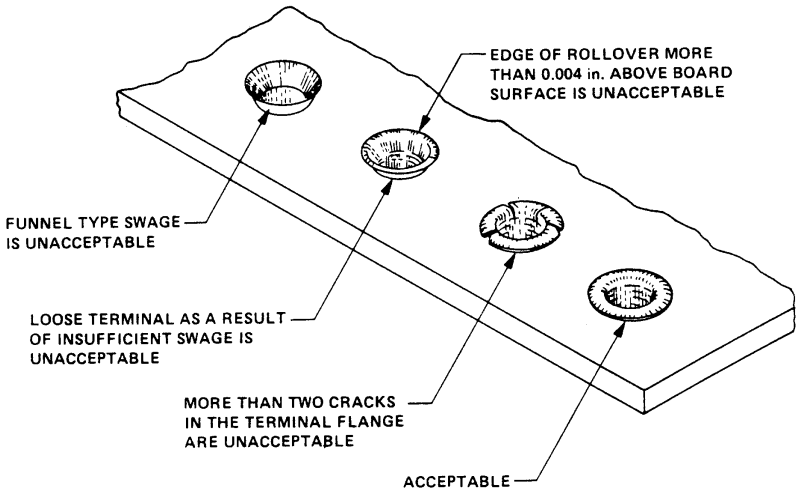

Figure 3.7-10 Terminal Swaging

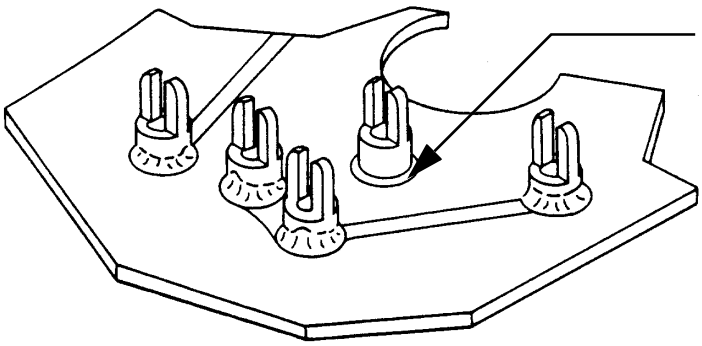

Figure 3.7-11 Terminal Soldering

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6 QUALITY ASSURANCE

6.1 JPL Approval and Reviews

JPL shall reserve the right to review critical items both prior to and during the PWB fabrication process.

6.1.1 QA Governing Documents. The documents governing the inspection of printed wiring boards by JPL QA personnel shall be QAI 10.1.2, *"Inspection of Printed Wiring Boards and Flexible or Rigid Flex Circuits"* and QAWS 100.40, *"Inspection Requirements for Fabrication of Printed Wiring and Terminal Boards."* The PWB manufacturer shall use ANSI/IPC-A-600E, *"Acceptability of Printed Boards,"* as the acceptance criteria using Class 3 acceptability level.

6.1.2 Survey of Vendor's Site. JPL reserves the right to survey the PWB fabricator's site at any time to assess its suitability for fabricating PWBs to JPL's specifications. See paragraph 2.3, Vendor Selection and Qualification, on page 3.7-3

6.1.3 Pre-fabrication Approvals. JPL reserves the right to review all vendor artwork films and travelers prior to starting the PWB fabrication.

6.1.4 Source Inspections. The following JPL source inspections to a released drawing shall be mandatory:

- Inner layer (prior to lamination);
- Final inspection;
- Microsections–PTH coupons must show positive etchback and minimum annular ring.

Normally both inner layer source and final source shall be performed at the vendor's site by JPL QA. In the event that the vendor has established that he can perform and deliver high quality PWBs in a timely manner as expected, the requirement of inner layer inspection may be waived by the JPL PWB Process Engineer and QA.

6.1.4.1 Inner Layer Inspection. JPL inspection of inner layer details shall be 100% of the manufactured lot.

6.1.4.2 Final Inspection. JPL inspection of the finished (routed, tested, and inspected by the vendor's final inspection process) PWBs shall be 100% of the manufactured lot. JPL QA shall also examine preselected microsections of both A and B coupons. Both

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As-Received and Thermal Stress microsections shall be examined. Both A and B microsections of the rigid portion of a PWB (in the case of a rigid flex PWB) and the flex portion shall be examined.

6.2 Data Package-Deliverables to JPL

The following items shall be delivered to JPL at the end of the PWB build:

- Completed PWBs.
- Results of all electrical verification testing performed at 200 Vdc.
- All material certifications.
- Traceability - The material used shall be traceable to the manufacturer's lot number through date code and serial number.
- Certificate of Material - Certificates of material shall be part of the delivered documentation package for each PWB.
- Copies of all inspection reports, traceability data, deviations, and MRB actions shall accompany each delivered PWB.
- Coupons (microsections) + results of microsection evaluation. See paragraph 6.1.4.2 above.
- Results of ionic contamination testing.

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Wire Wrap

1 DESIGN REQUIREMENTS

1.1 Documentation

1.1.1 Complete Package. Documentation shall contain all information necessary to design, fabricate, and inspect JPL flight-rated electronic equipment: physical, electrical, environmental, and process criteria.

1.1.2 Assembly Drawing. The assembly drawing shall provide the detailed information required to:

a. Define the wire wrap pins and ground pins in a to/from format,

b. Define V_{CC}, V_{EE}, and V_{TT} pin identification, and

c. Meet all requirements defined in JPL D-8208, Section 3.6.

1.1.3 Wire List. The wire list shall be available prior to wrapping and shall:

a. Identify the printed wiring board number,

b. Define the wire connections in a point-to-point format, and

c. Define wire level lists.

1.1.4 Manufacturing Data. Manufacturing and inspection data shall be required for each assembly.

1.1.4.1 Parts and Material Certification. Certificate of conformance shall be required for all parts and materials used in the fabrication of flight-rated electronics.

1.2 Wire

1.2.1 Wire Specification. All wire shall meet the requirements of MIL-W-81822: Kynar and Teflon TFE are rated in Table 3.8-1.

1.2.2 Conductor. The conductor shall be solid, round, soft copper or copper-alloy wire.

1.2.3 Conductor Finish. The wire shall have a continuous and unbroken coating of tin, nickel or silver plating, as specified on the fabrication drawing.

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1.2.4 Elastic Properties of 30 AWG Wire. The copper or copper alloy shall have a minimum elongation of 12 inches per each 10 inch sample of 30 AWG wire (0.0100 inch OD).

Table 3.8-1 Typical Insulated Wire for Wrap Applications

Property	Teflon TFE	PDVF (Kynar)
Temperature Rating, Degrees C	200	135
Oxidation Resistance	O	O
Flame Resistance	O	E
Abrasion Resistance	G	E
Cut-Through Resistance	F	E
Dielectric Strength	E	G-E
Dielectric Constant (1 kHz)	2.10	4.72
Dielectric Constant vs. Frequency	E	P
Resistance to dissolving in:		
Gasoline, Kerosene	E	E
Toluene	E	E
1, 1, 1 Trichloroethane	O	O
Ethyl Alcohol	O	O
Vertrel© XMS	O	O
AK 225T	O	O
Legend: O = Outstanding, E = Excellent, G = Good, P = Poor, F = Fair		

1.2.5 Elastic Properties of 28 AWG Wire. The copper or copper alloy shall have a minimum elongation of 15 inches per each 10 inch sample of 28 AWG wire (0.0126 inch OD).

1.2.6 Wire Softness. The wire shall be of sufficient softness to take approximately 95 percent (95%) of the indentation due to the solderless wrapped connection on the wrap post.

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1.3 Insulation

1.3.1 Basic Properties. The wire insulation shall:

a. Be able to withstand temperatures up to 130°C (266°F).

b. Possess good oxidation resistance.

c. Be flame resistant.

d. Possess good cut-through resistance.

e. Possess good dielectric strength.

1.3.2 Wire Stripping. The insulation shall be readily strippable from the wire without changing the wire or the wire insulation characteristics.

1.3.3 Insulation Thickness. The insulation thickness shall be a minimum of 40% of the conductor diameter.

1.4 Board Design

1.4.1 Plane Requirements. The double-sided printed circuit board shall be designed with a V_{CC} plane on the bottom of the board and a ground plane on the top with the following exceptions:

a. Schottky Transistor Transistor Logic (TTL) boards shall have a minimum of 2 ground planes with a V_{CC} plane sandwiched between. This is also required for high-speed Complementary Metal Oxide Semiconductor (CMOS) logic.

b. Boards with Mixed Emitter Collector Logic (ECL) and TTLs require 4 planes: V_{CC}(+5v), V_{EE}(-5v), ground plane, V_{TT}(-2v); and spaces for Single In-line Package (SIP) termination resistors.

c. ECL boards require a V_{TT} plane.

1.4.2 Dielectric Materials. Dielectric materials shall meet the requirements of MIL-P-13949, Type GFN or Polyamide Specification.

1.4.3 Copper Clad and Plating. Copper clad and plating thickness for the PWB shall meet the requirements of JPL D-8208, Section 3.6, Printed Wiring Boards.

1.4.4 Flame Retardant Materials. Flame retardant materials shall meet the requirements of FR-4 (general purpose) or FR-5 (heat resistant) on NEMA LI 1 1983.

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1.4.5 Installation Hole Size. The holes for wrap posts shall be 0.055 ±0.001 inch in diameter and unplated.

1.5 Wrap Post

1.5.1 Post Dimensions. The post shall be 0.025 inch square on each side prior to first time wrap.

1.5.2 Wrap Post Materials. Wrap posts shall be made of copper-base alloys as specified on the part detail drawings.

1.5.3 Surface Plating. Wrap posts shall be gold plated as specified on the part detail drawings.

1.5.4 Minimum Plating. The minimum plating thickness shall be 0.000050 inch.

1.5.5 Edge Radius. The edge radius of the wrap post shall be 0.002 inch or less.

1.5.6 Edge Burrs. Edge burrs shall be no greater than 0.0015 inch.

1.5.7 Post Length. The length of the post shall be determined by the level of individual wire-wrapped connections required.

1.5.8 Apex Configuration. The apex, or tip, of the wrap post should be finished with a radius or pointed to facilitate insertion into a wrapping tool.

1.5.9 Parallelism. The wrap post shall be straight and all sides parallel within 0.005 inch per inch.

1.5.10 Wrap Post Spacing. All installed wrap posts shall be spaced 0.100 inch center-to-center or as otherwise specified in the assembly drawing.

1.5.11 Wrap Post Insulation. Wrap posts spaced closer than 0.100 inch shall be insulated with an approved insulation material per engineering drawing.

1.5.12 Minimum Torque. Installed pins shall have the capability to withstand up to 2.0 inch-ounce torque without spinning in their mounting holes or breaking.

1.5.13 Contact Spring Orientation. Posts shall be installed so that the orientation of the contact springs is parallel to the sides of the IC leads and conforms to Figure 3.8-1.

1.5.14 Socket/Post Orientation. The individual posts shall be positioned with the socket axis perpendicular to the board axis as shown in Figure 3.8-1.

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1.5.15 Wrap Post Installation. All wrap posts shall be pressed into the fiberglass board with an approved pressing machine to provide uniformity and obtain the maximum shear without damage between the socket and epoxy glass, and conform to Figure 3.8-2.

1.5.16 Socket/Post Orientation. The individual posts shall be positioned with the socket axis perpendicular to the board axis as shown in Figure 3.8-2.

1.6 Socket Design

1.6.1 Hole Diameter. The pilot hole in the socket shall be 0.060 inch in diameter and 100° countersunk to avoid possible integrated circuit (IC) lead damage upon insertion into the sockets.

1.6.2 Socket Material. The material selected shall provide high mechanical and electrical reliability and maintain good spring characteristics of the socket.

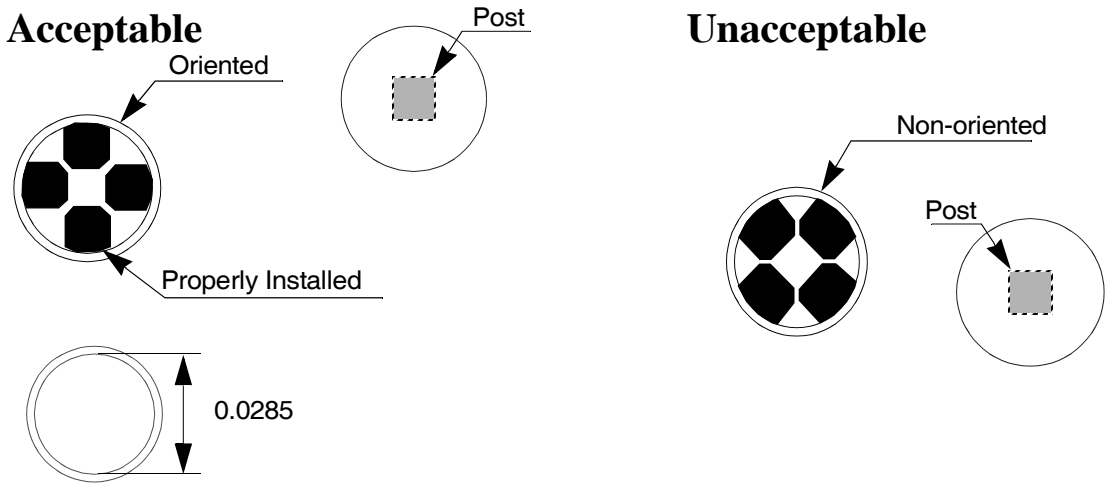

Figure 3.8-1 Wrap Post Internal Contact Spring Orientation

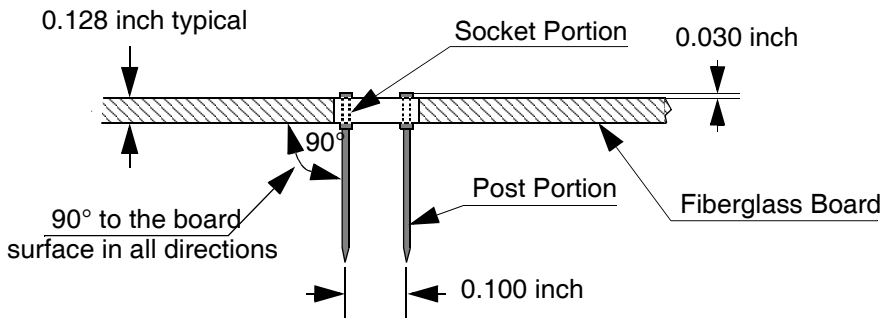

Figure 3.8-2 Wrap Post Installation

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1.6.3 Contact Spring. The contact spring in each socket shall be designed for high mechanical and electrical reliability.

1.6.4 Type of Contact. A multiple contact consisting of at least four fingers with smooth edges shall be required to avoid possible IC lead damage resulting from IC insertion or removal.

1.6.5 Plating. Contact plating shall meet the requirements specified in MIL-G-45204 and QQ-N-290.

1.6.6 Orientation. The socket pins shall be inserted so that the springs in the sockets are flat with respect to the lead to be inserted as shown in Figure 3.8-1.

1.7 Wire Wrap Connection

1.7.1 Routing. The wire wrap interconnect shall be installed running from pin to pin on the same wrap level unless otherwise specified in the "to/from" connection files.

2 FABRICATION REQUIREMENTS

2.1 Equipment

2.1.1 Certified Tooling. Wire-wrap tooling shall be certified for calibration per paragraph 3.3.1.1.

2.2 Wire

2.2.1 Continuous Insulation. Installed wires shall provide continuous and undamaged wire insulation from terminal to terminal and be free from tears, cuts, kinks, burns or frays.

2.2.2 Rewrapping. No portion of a wire previously wrapped on a wrap post shall be reused.

2.2.3 Damage Avoidance. Wires shall be routed so they are not tight against the sharp edges of other posts, terminals, or abrasive objects on an assembly.

2.2.4 Excessive Wire.The wire routing shall be selected to preclude excessive lengths and wire protruding above the apex of any wrap post.

2.3 Board

2.3.1 Electrical Testing. Each wire wrapped board shall be checked for opens and shorts between all interconnect circuit nets, including shorts and opens of and between the power and ground planes.

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2.4 Wrap Post

2.4.1 Bent Wrap Post. Wrap posts shall not be bent or damaged during the wire wrap installation but may appear polished.

2.4.2 Wrap Post Plating. The wrap post plating shall be smooth without nicks or gouges.

2.4.3 Post Rewrap. The wrap post shall be acceptable for rewrap providing it contains no nicks, gouges, or other physical defects.

2.5 Wrap Post Socket

2.5.1 Minimum Retention. All wrap post sockets shall exhibit a minimum retention force of 0.5 ounce.

2.5.2 Retention Force of Contact. The insertion and separation force test shall meet the following requirements:

a. Insertion force shall not exceed 1.5 oz. per individual pin socket contact.

b. Withdrawal force shall not be less than 0.5 oz., nor exceed 1.5 oz. per individual pin socket contact.

2.6 Wrap Connection

2.6.1 Minimum Turns of Wire. There shall be at least seven (7) turns of bare wire and one-half turn of insulated wire for AWG 28 and AWG 30 on a 0.025 inch post.

2.6.2 Proper Wire-Wrap Construction. Wrapped connections and wire routing will be in accordance with Figure 3.8-3.

2.6.3 End Tail. The end tail of any wire wrap shall only be allowed to extend less than one uninsulated wire diameter from the post.

2.6.4 Adjacent Turn Spacing. Spacing between adjacent turns on a post shall be less than one-half the diameter of uninsulated wire.

2.6.5 Smooth Connection. The finished wire wrap connection shall be smooth with no overlapped turns of uninsulated wire.

2.6.6 Overlap. All wire wrap configurations shall conform to the wrap specification depicted in Figure 3.8-3.

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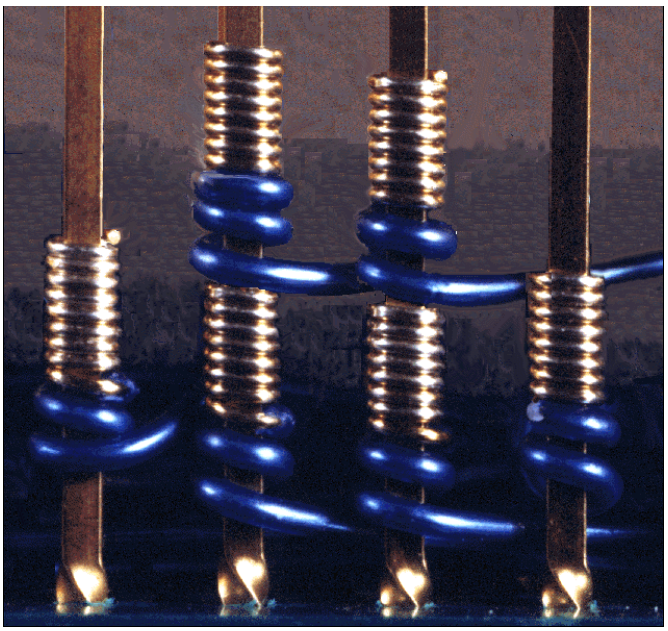

Figure 3.8-3 Wire-Wrapped Connections

2.6.7 Overwrapping. Only the insulated portion of secondary wraps shall be allowed to overwrap the last turn uninsulated wire of previous wrap.

2.6.8 Taut Routing.Routing of the insulated wire leads from each post connection shall not cause the wire to unwrap, loosen or short to adjacent wires or terminals.

2.6.9 Wire Retainer. A wire-wrap retainer, JPL Dwg #10117788, shall be used where the wire run is longer than 2 inches and the number of wraps per post is the same.

2.6.10 Spot Ties. Spot ties shall be used where the wire run is longer than 2 inches and the number of wraps per post are uneven.

2.6.11 Gas-tight Wrap Connection. The solderless wrapped connection, except for the first and last turn, shall, for each turn, exhibit a gas-tight area on at least 75% of the corners in contact with uninsulated wire.

2.6.12 Strip Force Test. The results of the strip force test shall conform to Table 3.8-2.

Table 3.8-2 Strip Force Test Results

Wire Size (AWG)	Post Size (Inches)	Minimum Force (Pounds)
28	0.025	3.0
30	0.025	2.0

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3 QUALITY ASSURANCE

3.1 Verification Methods

The following methods shall be used to verify the requirements of this document.

3.1.1 Inspection. Verification by inspection is accomplished by comparing the requirements specified in Section 2 with the appropriate characteristics of an item. Inspection includes evaluation of mechanical functionality and accuracy as described in corroborating documentation.

3.1.2 Test. Verification by testing is accomplished by subjecting an item to a set of conditions under the control of approved plans, procedures, and test equipment which will provide a measurable response. The results of the test are compared with the expected results as specified in Subsection 2.

3.2 Inspection Methods

Any item displaying the defects shown in Figure 3.8-4 shall be returned for disposition by the packaging engineer.

a. Nicked and bent wrap post, identified as Item 1.

b. Overlapping bare wire, identified as Item 2.

c. Improper spacing of wire wraps, identified as Item 3.

d. Wire not wrapped at an angle parallel to board, identified as Item 4.

e. Nicked wire insulation, identified as Item 5.

f. Insufficient turns of insulated wire, identified as Item 6.

g. Bare wire protruding away from wrap post, identified as Item 7.

h. Insulated wire overlapping bare wire of more than the first wrap, identified as Item 8.

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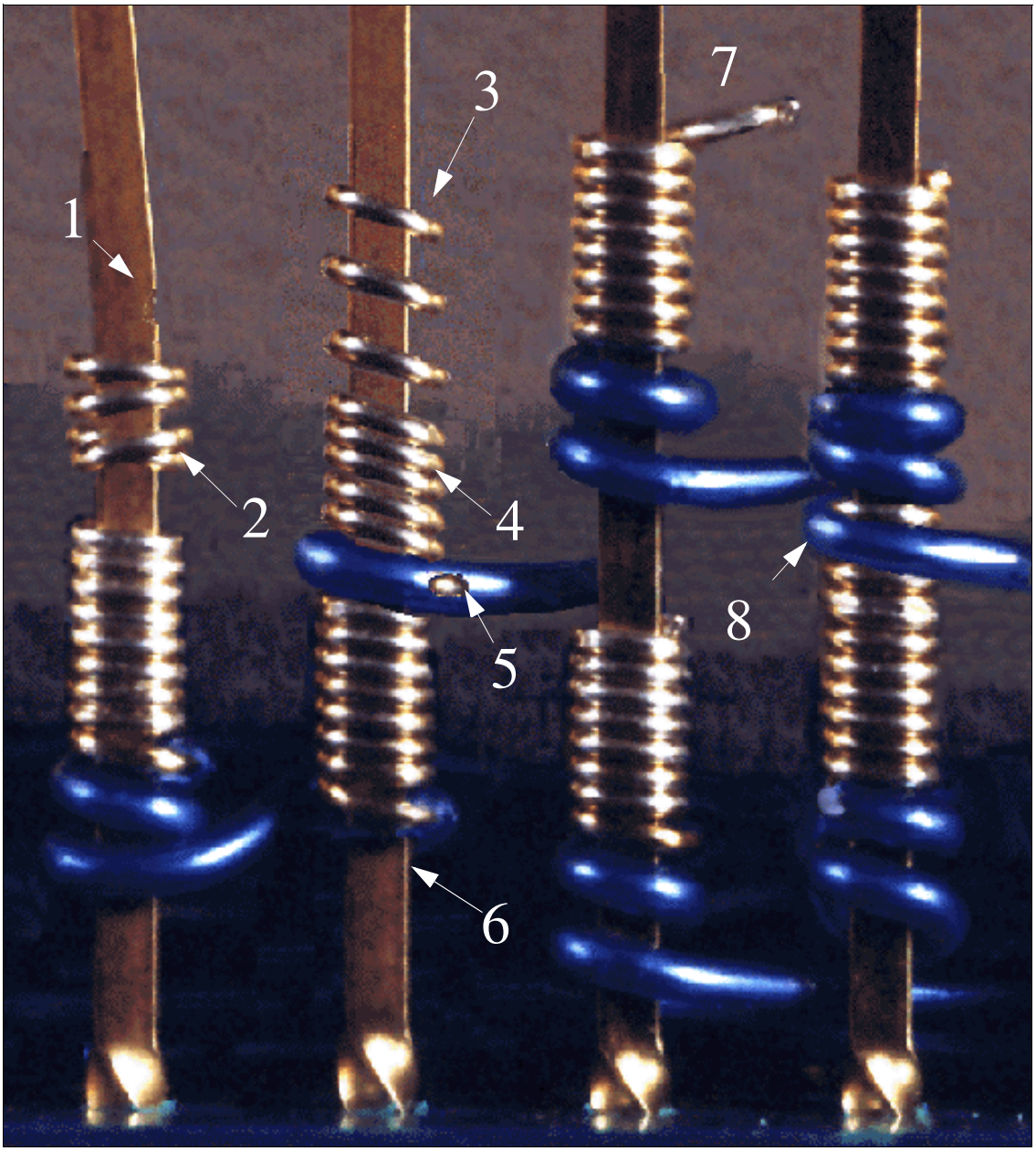

Figure 3.8-4 Wire Wrap Defects

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3.2.1 Magnification. The requirements shall be verified by a visual check using 12X power magnification.

3.3 Test Methods

Procedures for specific tests are detailed in JPL FP513414. Any test that does not meet the specified requirements shall be repeated using recalibrated equipment, to ensure that the production wire-wrap connections are fully reliable. All tests and results shall be performed per, and results recorded on, an approved shop traveller.

3.3.1 Tool Calibration.

3.3.1.1 Wrapping Tool. The capability of the wrapping tools to provide acceptable solderless wrapped electrical connections shall be established for each combination of wrap post (based on cross-sectional geometry), wire gage, conductor material, and wrapping bit-and-sleeve configuration.

3.3.1.2 Socket Force Retention Tool. The socket force retention tools shall be calibrated in the inspection and calibration laboratory.

3.3.1.3 Gas-tight Test. A gas-tight test shall be conducted on new equipment and/or once a year to verify tool condition.

3.3.1.4 Tool Verification. All other tools shall be checked every day before use, and every 4 hours thereafter, to determine that they are working properly.

3.3.1.5 Wire Size. The same size wire and post being used on the hardware shall be used to perform the tool verification tests.

3.3.2 Wire.

3.3.2.1 Test Current. The current passed through the wires shall not exceed that specified on the master drawing for the smallest wire in the circuit.

3.3.2.2 Unwrap Test. The unwrap test shall certify that the unwrapped wire, when pulled straight, does not break, nick, gouge, or bend the post.

3.3.2.3 Strip Force Test. The strip force test shall be performed using the rate of travel of 1/2 to 6.0 inches per minute, and the minimum acceptable strip force values using a 0.025" pin shall be 3.0 pounds for size 28 AWG wire and 2.0 pounds for size 30 AWG wire.

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3.3.3 Board.

3.3.3.1 Continuity Check. For boards with no flight parts installed, a current shall be passed through each wire or group of interconnected wires by applying electrodes on the wire wrap pins at each end of the wire or group of wires.

3.3.4 Socket Contact Retention Force Test. The testing of the sockets shall be conducted using the Socket Force Retention Tool, JPL tool #10090277-1A or equivalent as approved by JPL engineering.

3.3.4.1 Test Quantities. Test samples shall be five percent or 100 samples per lot, whichever is less.

3.3.4.2 Retention Force. The acceptable retention force measurements for flight contacts shall be a maximum insertion of 1.5 oz., a maximum withdrawal of 1.5 oz., and a minimum withdrawal of 0.5 oz.

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High-Voltage Requirements

1 DESIGN REQUIREMENTS

Design of high-voltage equipment must consider the following categories:

a. Flux density

b. Voltage gradients

c. Critical pressure and venting

d. Materials and components

e. Isolation or separation of high-voltage circuits

f. Testing

1.1 Flux Density

Flux lines should be spread as evenly as possible to minimize any high local flux density and not allow the flux lines to concentrate, as is the case at sharp points and with irregular geometries. To control flux densities, the following items shall be addressed:

1.1.1 Terminals. Terminals for high-voltage circuits shall be JPL Standard ST12047 through ST12050, Terminal, Electrical, Rounded, Swage Mount, High-Voltage, or ST 10591, ST11204, ST11076, ST11205, ST11020, and ST11299 using JPL high-voltage soldering processes defined in FP513414.

1.1.2 Flush Leads. The ends of component leads shall be flush with the edge of the terminal.

1.1.3 Minimal Terminals. The use of terminals shall be kept to a minimum in high-voltage circuits.

1.1.4 Sharp Points. Circuit conductors, electronic and mechanical parts that are subjected to high-voltage stress shall be designed or laid out in a manner that avoids sharp points, sharp corners, sharp edges, and abrupt changes in dimensions.

1.1.5 Smooth Conductors. Smooth curves, rather than sharp corners, shall be used for changes in direction of all conductors.

1.2 Voltage Gradients in High-Voltage Equipment

Voltage gradients should be as low as possible. Attempt to spread the applied voltage linearly to minimize the unit voltage gradient over or within the total available insulating media. When possible, increase the insulating distances, utilize media with a greater dielectric strength, or both.

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a. High-Voltage Limits. The requirements of this section shall be mandatory for space electronic equipment having voltages in excess of 250 volts AC peak or DC peak. This limit is applicable to frequencies from DC to 60 Hz, and shall be reduced in accordance with Figure 3.9-1 for frequencies above 60 Hz. Even at lower voltages, the conductive plasmas generated by a corona or arc, or other mechanism such as passage of the spacecraft vehicle through low pressure gaseous environments, can drift across conductors carrying much lower voltages (e.g. 24 volts), initiating arcing in these circuits. At frequencies above 1 GHz, breakdowns can occur in cavities or wave guides in vacuum due to secondary emissions (multipacting). Protection against multipaction is not addressed in this document.

b. The theoretical minimum breakdown voltage of 270 volts peak is for air; other gases, especially the noble ones, even in trace quantities, can cause breakdown to occur at much lower voltages.

1.2.1 Determination of Voltage Gradient. The distance or thickness between high-voltage conductors shall be measured in a straight line from the points of closest approach, including worst tolerance buildup. The voltage gradient shall then be calculated by dividing the peak voltage by the insulating distance or thickness in mils.

1.2.2 Voltage Gradient Limits. If the geometry is such that the maximum gradient cannot be calculated, the thickness of insulation provided as a function of the voltage shall be 40 volts/mil or 10% of the actual breakdown voltage for the thickness of insulation used in the design, whichever voltage gradient is less.

1.2.3 Maximum Gradient.If the geometry is one in which calculation of the maximum gradient is possible, the maximum gradient allowable shall be 100 volts/mil, or 25% of the actual breakdown voltage for the same thickness of insulation, whichever is less.

1.2.4 Conductor Spacing. The minimum interface separation of conductors carrying high voltages on the same side of printed wiring or terminal boards shall be as calculated by:

$$d = 0.250\sqrt{kV\ peak}$$

d is the separation in inches.
kV (kilovolts) is the maximum peak voltage difference between the conductors.

Methods used to increase the interface separation, such as holes in the terminal board that are filled with high voltage encapsulant, should be part of the calculation.

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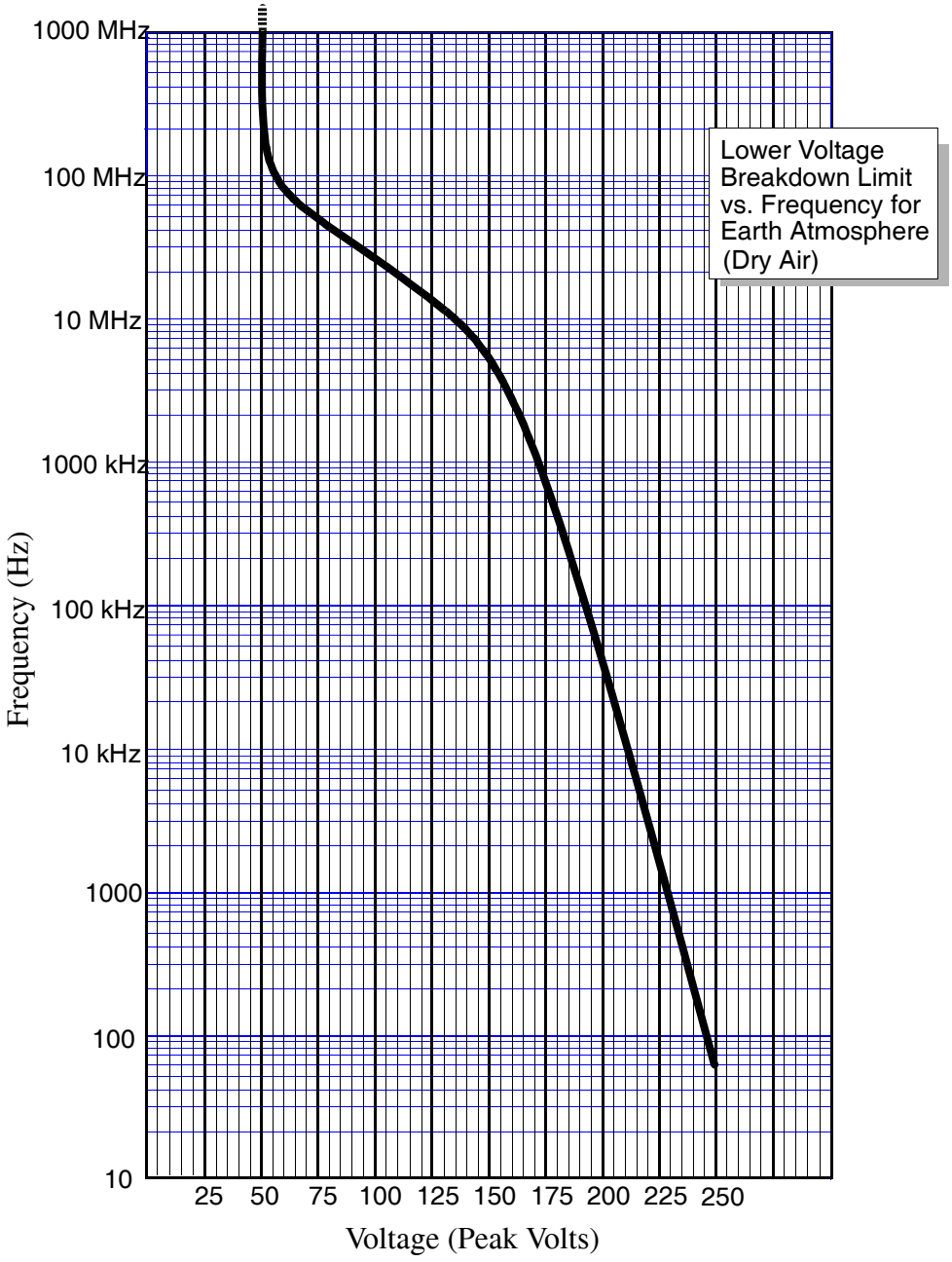

Figure 3.9-1 Lower Voltage Breakdown Limit

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1.2.5 Conductor Order. Layout of the high-voltage circuitry shall provide for gradient reduction by placing conductors in the order of decreasing voltages, as long as such placement does not cause adverse effects on the performance of the circuit.

1.2.6 Spacing from Edge. The minimum distance of the conductors from the edge of the printed wiring or terminal board shall be 1.5 times the value obtained from the equation in paragraph 1.2.4, unless the module design provides solid insulation beyond the edge of the board which satisfies the requirements of 1.2.2 or 1.2.3.

1.3 Critical Pressure and Venting

When possible, do not operate high-voltage circuits within the critical pressure region (50 torr to $5x10^{-4}$ torr). If high-voltage operation is required within the critical pressure region, the basic parameters in this section must be carefully addressed. Venting is also a design subject which must be addressed and will be covered in paragraph 1.3.2. Electromagnetic interference versus venting design parameters will not be found in this section.

1.3.1 Critical Pressure Region. The range of pressures through which the dielectric strength of the air reduces to 20 percent or less of the dielectric strength at 20°C and sea level pressure, shall be the critical pressure region for the purpose of this section. Limits of the critical pressure region in dry air are 50 torr (60,000 feet altitude) to $5x10^{-4}$ torr (310,000 feet altitude).

1.3.1.1 High-Voltage Circuits. Experience has shown that any high-voltage circuit contained in an enclosure may operate at the lower end of the critical pressure region (10^{-3} to 5×10^{-4} torr); therefore, no circuits shall be degraded by such operation. Suitable analysis or tests shall be performed to demonstrate compliance.

1.3.2 Venting.

1.3.2.1 Direct Venting. Enclosures which are not hermetically sealed shall be vented directly to the ambience of space.

1.3.2.2 Vent Area. The total area of vent opening shall allow the pressure in the enclosed volume to bleed down to 3×10^{-3} torr in 60 seconds or less, when the pressure is reduced from ambient sea level to 10^{-5} torr in 6 minutes or less.

1.3.2.3 Hermetic Enclosures. Flight equipment installed in hermetically sealed enclosure shall be exempt from the requirements of this section if the product of the measured leak rate and the mission time is such that the resultant pressure in the enclosure at the end of the mission is greater than 50 torr.

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1.4 Materials and Components

1.4.1 Dielectric Parameters.

1.4.1.1 High Dielectric Strength Rating. Insulating materials having the higher dielectric strength shall be used in high-voltage applications when other properties or characteristics pertinent to the application are similar.

1.4.1.2 Low Dielectric Strength Rating. Materials with dielectric strength of less than 300 volts/mil at the thickness required shall be avoided, unless necessary because of electrical requirements.

1.4.1.3 Dielectric Constant. Insulating materials with low dielectric constants shall be selected for insulating high voltages whenever possible.

1.4.1.4 Dielectric Constant Matching. Where two different insulating materials are in contact, they shall be selected so that the difference in their dielectric constant is minimal. This is important because the field intensities are inversely proportional to their dielectric constants (i.e., $\frac{E_1}{E_2} = \frac{k_2}{k_1}$)

1.4.1.5 High Dielectric Constant. Materials with a dielectric constant greater than five shall be avoided; unless the higher dielectric constant is required, and the voltage gradients are shown to be acceptable.

1.4.2 High Frequency Applications.Insulation materials selected for use at high frequency, nominally above 1.0 MHz applications, shall have the dielectric constants and dielectric losses low enough so that blistering, delamination, or other internal damage caused by internal heating will not occur during normal operation.

1.4.3 Insulating Material Section.

1.4.3.1 Air Dielectric Strength. For purposes of equipment design in accordance with this section, air shall be assumed to have a zero dielectric strength in the critical pressure region.

1.4.3.2 Low Arc Resistant Materials. Organic insulating materials, which have a tendency to sustain arcing under any pressure condition, or which deteriorate or outgas under arcing conditions, shall avoid contact with bare conductors emerging from the insulating material and exposed to the ambient pressure. High arc resistant materials such as inorganics shall be used as shown in Figure 3.9-2.

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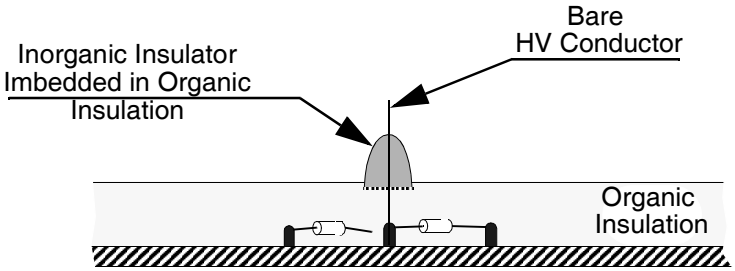

Figure 3.9-2 Inorganic Insulation

1.4.3.3 Filled Materials. Insulation, which employs fillers or discrete materials mixed throughout its volume, shall be considered to have the dielectric strength of the lowest dielectric strength material in the mixture.

1.4.3.4 Insulation Coatings and Embedments. All exposed conductors carrying high-voltages shall be insulated or embedded in an electrically insulating material in conformance with this document. Conductors which must be exposed to the ambient pressure for proper functioning (e.g., spark gaps), shall be exempt from this requirement.

1.4.3.5 Foams. Expanded or syntactic foam materials, or materials that are porous, shall be avoided in high-voltage insulation applications.

1.4.3.6 Adhesion of Polymeric Materials. Selection of polymeric insulation materials and preparation of solid surfaces in contact with such materials shall assure proper adhesion of the polymeric materials to eliminate electrical creepage paths between conductors.

1.4.3.7 Removal of Absorbed Gas. Prior to polymerization, encapsulation and impregnation materials shall be exposed to a vacuum sufficient to remove absorbed gas. Pouring of insulation material into mold while both items are under vacuum prevents air entrapment.

1.4.4 High-Voltage Transformers and Inductors.Transformers and inductors shall meet the requirements of this document, JPL D-8208, Section 3.13, as well as the requirements of this high-voltage section.

1.4.4.1 Maximum Voltage Stress. The thickness of the wire insulation and the winding technique shall be such that the maximum possible voltage between any two adjacent

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wires in a winding is in no case larger than 40 volts peak. The overall configuration shall comply with the voltage gradient limit requirements of this document for high-voltage equipment.

1.4.4.2 Additional Insulation. Bonded interfaces separating connections internal to the magnetics shall comply with paragraph 1.2.4 of this document.

1.4.4.3 Pulse Transformers. In high-voltage pulse transformers with pulse widths of 10 µsec or less, the allowable voltage limit between wires shall be 200 volts peak.

1.4.4.4 Core Connection. If there is no internal connection between a winding and the core, electrically conductive cores which are electrically insulated from the mounting base of the transformer or inductor shall have an auxiliary lead brought out to facilitate hipot tests between the core and the windings to test core insulation integrity.

1.4.4.5 Plastic-Encased Cores. Cores fabricated from high permeability magnetic materials and encased in plastic shall be exempt from requirement 1.4.4.4 of this section, provided that the plastic material is in accordance with all the paragraphs under 1.4, and is sufficiently transparent to allow measurement of the minimum thickness of insulation separating the core from the winding.

1.4.4.6 Metallic-Encased Cores. Cores encased with metallic covers and covered with insulation material also shall be exempt provided the insulating material is in accordance with paragraph 1.4.3 of this section and the low-voltage winding (primary) is between the high-voltage windings and the core.

1.4.4.7 Winding Embedment. Windings shall be impregnated and then encapsulated or embedded with suitable materials and techniques to meet the requirements of 1.2, so that all wires are securely anchored and no pockets or voids occur.

1.4.4.8 Bonding. The insulation or embedment material shall be compatible with the lead wire insulation and achieve a thorough bond so that electrical creepage paths from the conductor to the outside of the transformer or inductor will not occur.

1.4.4.9 Bond Length. The length of the bond path from the conductor to the outside of an encapsulated or embedded module shall be 0.25 inch, or in accordance with paragraph 1.2.6 of this section, whichever is greater.

1.4.4.10 Wire Anchors. Provisions shall be made to anchor the wire as it emerges from the encapsulant or embedment.

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1.4.5 Connectors.Connectors shall not be used as high-voltage interfaces in equipment unless compliance of such connectors with the requirements of this section is demonstrated by suitable tests.

1.4.5.1 Insulation Materials. Insulation materials used in connectors shall be selected per the high-voltage requirements in paragraph 1.4.3 of this section.

1.4.6 Electronic Components.Only electronic components that have demonstrated, by test, the ability to operate under the design maximum voltage shall be selected for high-voltage applications.

1.4.7 Selection of Terminal Board Hardware.For high-voltage circuitry at or above 1000 volts peak, swaged terminals, discrete components and solid bus wire for interconnections shall be used.

1.4.7.1 Terminal Pads. Terminal pads shall not be used under swaged terminals in circuits with voltages above 1000 volts peak.

1.4.7.2 Printed Wiring. Printed wiring conductors (etched circuits) shall not be used above 1000V peak, unless special precautions are taken to reduce voltage gradients along the conductor edges.

1.4.7.3 Swaged Terminals. Swaged terminals should not be used for circuits operating above 10 kV, unless the peak stresses induced by the terminals are reduced.

1.5 Isolation of High- and Low-Voltage Circuits

When possible, isolate or otherwise separate or shield high-voltage circuits to decrease the possibility that the high-voltage circuits will affect the low-voltage circuit.

1.5.1 Separation of High-Voltage Circuits.Circuits employing high-voltage shall be physically separated from low-voltage circuits with a minimum length common boundary when located on the same printed wiring or terminal board as shown in Figure 3.9-3.

1.5.1.1 Low-Voltage Circuit Protection. A ground bus shall be located between high- and low-voltage circuitry to prevent possible high-voltage creepage currents or arcs causing interference with, or damage to, the low-voltage circuits, as shown in Figure 3.9-3.

1.5.1.2 Superimposed Ground Bus. Where the same high-voltage exists on both sides of the printed wiring or terminal board, the ground bus shall be on both sides, superimposed one above the other as shown on Figure 3.9-4.

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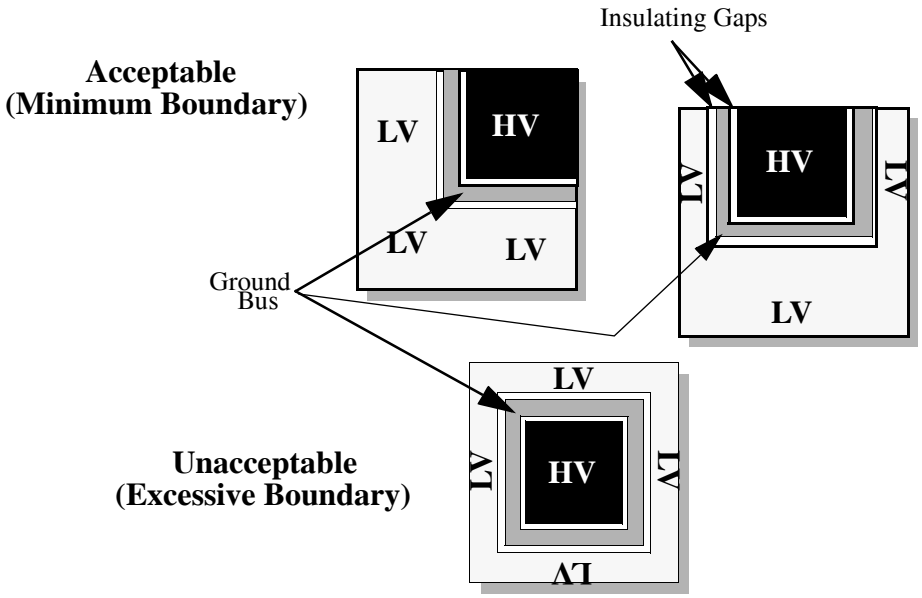

Figure 3.9-3 Required Separation of High-Voltage and Low-Voltage Parts

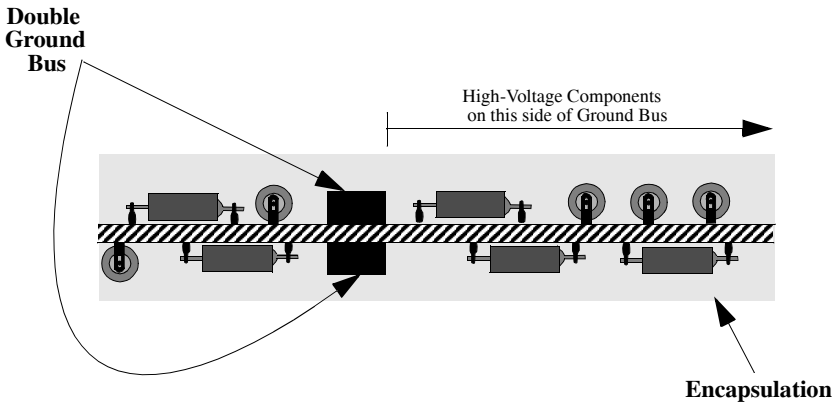

Figure 3.9-4 Common Boundary, HV and LV Circuits

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1.5.1.3 Wider Ground Bus. When possible, consider making the ground bus wider than regular conductors to provide a lower impedance return path for an arc.

1.5.1.4 Independent Ground Bus. The purpose of the ground bus is to handle arcs; therefore, it shall be independent of any other grounds except the high-voltage circuit ground.

1.5.1.5 Shielding. Shielding shall be required as a means to isolate high-voltage from other circuitry when it cannot be demonstrated that the high-voltage circuitry will operate without corona or arcing while at the minimum dielectric strength in the critical pressure region.

1.5.1.6 Gaseous Environment Shielding. Shielding shall be required if the equipment is intended to function in a low dielectric strength gaseous environment.

1.6 Testing

Whenever possible, the high-voltage design shall include features to facilitate corona and voltage breakdown evaluation.

2 FABRICATION REQUIREMENTS

2.1 General Fabrication Requirements

The ST12047 through ST12050 terminals have been designed to eliminate the need to round-off the top of a terminal solder joint when used in high-voltage applications. These particular terminals are actually ST11204 bifurcated terminals which have been modified to have rounded-off tops rather than sharp pointed tines. Now that these rounded-top high-voltage terminals are available, the soldering process is no longer unique to high-voltage and the regular flight soldering requirements and procedures of JPL D-8208, Section 3.14, now apply to high-voltage terminals also. If terminals other than ST12047 through ST12050 are used, the solder ball procedure provided in FP513414 shall be used to make the connections.

Other fabrication requirements and processes for standard flight equipment are also applicable to high-voltage equipment. Consult the appropriate Sections of this document (e.g., Cleaning, Flux Removal, Soldering, Embedding, Impregnating and Marking) in support of the fabrication of high-voltage equipment.

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2.2 Specific High-Voltage Fabrication Requirements

During fabrication procedures, routing, layout and assembly techniques shall not cause the following conditions to exist in high-voltage equipment:

a. Kinks in wires or insulation

b. Sharp points

c. Splayed wire strands

d. Wires protruding past terminal shoulders

e. Dirty or otherwise contaminated areas

f. Unapproved materials or component substitutions

g. Voids in the encapsulant material

3 QUALITY ASSURANCE

3.1 Verification Methods

The following methods shall be used to verify the fabrication requirements of Section 2 of this document.

3.1.1 Inspection. Verification by inspection is accomplished by comparing the requirements specified in Section 2 with the appropriate characteristics of an item. Inspection includes evaluation of mechanical functionality and accuracy as described in corroborating documentation.

3.1.2 Test. Verification by testing is accomplished by subjecting an item to a set of conditions under the control of approved plans, procedures, and test equipment which will provide a measurable response. The results of the test are compared with the expected results as specified in Section 2.

3.2 Visual Inspection

In addition to the subjects delineated in the various associated processes in this document (e.g., cleaning, soldering, embedding, impregnating and marking), the following items shall be cause for rejection during inspection:

a. Sharp bends in wires or cables

b. Sharp points

c. Kinks in wires

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d. Creases in insulations

e. Broken wires or strands

f. Splayed wires

g. Disturbed wire lay

h. Unapproved component substitutions

i. Unapproved materials usage

j. Damage to components, chassis, PWBs or terminal boards

k. Contamination or foreign materials

3.3 Documentation Package

Assure the existence and completion of a set of manufacturing documents which includes materials certifications, inspection reports, travellers, engineering drawings, ECOs, ECIs, any MRB actions and responses and all other pertinent data which will prove the equipment pedigree and status.

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Radio Frequency

1 SCOPE

This section details requirements for the design of radio frequency, (RF), circuits. The following documents are applicable to the extent herein stated:

- FP513414 (JPL), “Assembly and Wiring of Electronic Equipment and Assemblies, Manufacturing Processes and Procedures for.”
- EIA Stardard RS-199A
- EIA Standard RD-200
- EIA Standard RD-261
- EIA Standard RS-166, “Miniature Waveguide Flanges, Unpressurized Contact Type.”
- IPC-2141, “Controlled Impedance Circuit Boards and High-Speed Logic Design.”
- IPC-6018, “Microwave End Product Board Inspection and Test.”
- IPC-C-406, “Design and Application Guidelines for Surface Mount Connectors.”
- IPC-D-275, “Design Standard for Rigid Printed Boards and Rigid Printed Board Assemblies.”
- IPC-D-316, “Design Guide for Microwave Circuit Boards Utilizing Soft Substrates.”
- IPC-D-317A, “Design Guidelines for Electronic Packaging Utilizing High-Speed Techniques.”
- MIL-F-3922B
- MIL-STD-461C
- MIL-STD-462
- MIL-STD-1250 (MI)

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2 TRANSMISSION LINES

When transferring RF signals from one location to another, source to load impedance matching is extremely important. If mismatched impedances exist in the signal path, maximum power will not be transferred because some of the signal will establish standing waves as it is reflected back towards its source and the remaining signal will become distorted. Transmission lines provide a constant impedance path between like impedances at different locations or impedance transformations that match the output impedance of the source to the input impedance of the load.

2.1 Cables

Cables are designed to provide constant impedance between their input and output. Input sources and output loads should be designed to match the characteristic impedance of the cable. The specification for cables is the EIA standard “Solid and Semi-Solid Dielectric Transmission Lines” RS-199A

2.1.1 Coaxial Cables. Coaxial cables are excellent for use at frequencies from 20 kHz to 5 GHz. They provide a shield to help isolate the signal from stray capacitance and magnetic fields. They also reduce the amount of signal coupling into other circuits. Coaxial cables will not prevent strong signals from interfering with low-level signals. The shielding effect is compromised in that the shield carries the signal return current, thus making it part of the signal path.

A coaxial cable, (“coax”), is a shielded cable with an insulator that separates the center conductor and shield while providing the capacitance necessary to form a transmission line. Each increment of the cable inductance is neutralized by an increment of capacitance, thus establishing a constant impedance for the propagating signal. The shield is used as a return path for the signal carried by the center conductor. The coax shield provides good electrostatic protection in that the RF signal return is connected to the RF circuits ground plane. Electrostatic noise is capacitively coupled to the shield, which attenuates the noise by reflecting most of it away from the shield because of the impedance mismatch. The capacitive coupling generally occurs when the coax comes in contact with another signal carrying wire. Any coupled signal voltage that is introduced between the ends of the shield affects the signal. If the shield is connected to RF ground at both ends, any voltage between the two ground locations will appear as a signal voltage. Low frequency signals (20 kHz to 6 MHz) are particularly susceptible to interference from ground loops and common mode noise. When electrostatic noise is the

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problem and the noise between the source and load ground locations is low, best performance is obtained by grounding the shield at the source and at the load.

High frequency current generates a magnetic field, which couples noise into near-by conductors. The conductors act as receiving antennas or secondary windings of a transformer. Electromagnetic shields attenuate magnetic fields by making use of the fact that electromagnetic radiation must simultaneously contain a constant ratio of electric and magnetic fields to propagate through space. The shields are designated to attenuate the electric field and thereby reduce the magnetic field component of the electromagnetic wave. The outer conductor of the coax cable must therefore provide a low impedance path to ground to be effective against electromagnetic interference. When the coax is used to reduce noise interference produced by its strong radiation fields, the shield may require grounding at intermediate points along the cable. The radiated interference should be removed as soon as possible by multiple ground points for maximum effectiveness.

If the shielding application requires effectiveness against large radiated fields and the region is subjected to ground loops, the coax may require replacement with a triaxial or a balanced-pair cable. The triaxial and balanced pair cables are also effective against crosstalk between transmission lines. Cross talk between coaxial cables occurs when the signal current in the shield of one coax couples a signal into the shield of an adjacent coax.

2.1.2 Triaxial Cables. Triaxial cables are coaxial cables with an additional isolated outer braid that protects, encloses, and acts as a true shield for the enclosed coaxial conductors. This added braid is connected to ground. It isolates the signal carrying coaxial conductors from capacitance fields, ground loop currents and magnetic radiation. The shield wire that provides the return path for the signal is no longer tied to ground and remains isolated from the added outside shield.

If a triaxial cable is used for high frequency low impedance applications, the distributed capacitance and impedance of the coaxial line can be reduced. The outer braid, (shield), of the triaxial cable functions as the signal return. One end of that braid is connected to the source return and the other to the load return. Only the source return end of that braid is connected to ground. The inter-coaxial braid is connected to its inter-conductor at the source output and its load end is floated above ground. In this configuration, the inter-coaxial braid forms a Faraday shield between the inter-conductor and the braided outer shield. This provides a low impedance, (approximately 12Ω), low-loss

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transmission line to carry high current pulses to a low impedance load. Isolating triaxial connectors are available for this application.

2.1.3 Twin-Coaxial Cables.A twin-coaxial cable is a two-conductor twisted balanced wire pair with a shielding braid around the pair of wires. The twisting of the two balanced-signal carrying wires cancel any random induced noise voltage pick-up and provides protection against any low frequency magnetic noise that passes through the braided shield. Above approximately 15 MHz the cable becomes useless because the transmission losses are unacceptable.

When this type of cable is used, the signal carrying twisted pair of conductors are isolated from ground. The shielding braid is grounded at both ends (source and load). The twin-coaxial cables minimize the pick-up of magnetic interference, because each conductor of the twisted pair generates approximately the same voltage when they are both subjected to the same magnetic field changes. Use of this cable in RF application is limited to low frequencies as mentioned earlier.

2.1.4 Breakdown of Cable Type Transmission Lines.Breakdown can occur because of excessive heat, excessive voltages, ionization or multipaction. These problems are addressed in the following subsections.

2.1.4.1 Cable Heating. Cable dielectric, (insulating), material has a limited operating temperature range. Its surrounding temperature and the power dissipated in the cable affects the temperature of the dielectric material. The power handling capability of each cable is specified for a given ambient temperature, and it shall not be exceeded. The power rating and temperature limits of cables are not listed in any of the MIL-STD specifications. The cable manufacturing specification is the best source of such information. If the specification does not provide the required information, contact the manufacturer.

2.1.4.2 Cable Voltage Rating. The voltage rating of each type of cable transmission line can be obtained from the cable manufacturer. The maximum voltage that any cable will experience can be determined from its maximum operating power. The nominal rms

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voltage in the cable can be calculated from the nominal impedance of the cable and the power transmitted.

$$V_{rms} = \sqrt{Power \times Resistance}$$

The peak voltage is 1.41 times the rms voltage. If the output circuit is opened or shorted, the peak voltage in the coax cable will be doubled because of the mismatch. Cable operation under an open or shorted condition shall not exceed the manufacturers rating.

2.1.4.3 Ionization Breakdown in Transmission Cables. Transmission cables with solid dielectric cores shall not contain any air bubbles or voids in their dielectric, and they shall have good adhesion between the core and the inter-conductor. Voids may exist between the braided portions and the solid dielectric core, but they should be very small. Ionization, (corona), inception is dependent on the voltage across a gap and the pressure of the gap. In general, the power level must be very high to generate voltages greater than 50 V_{rms} across a small void in a solid dielectric cable. JPL Technical Report 32-1500, “Final Report on RF Voltage Breakdown in Coaxial Transmission Lines”, offers insight into the conditions necessary to produce ionization in coaxial cables. The report, (Table 1, page 16), shows voltages as low as 49 V_{rms} causing ionization breakdown in a 50Ω coaxial transmission line.

Transmission cables with semi-solid, (air-spaced), dielectric cores are more susceptible to ionization breakdown. The voltages across the air space between the two conductors could be 50 V in a 50Ω coax at relatively low power levels: $\rho = E^2/R = 50^2/50 = 50$ W. A nominal 12.5W, 50Ω σψστε χουλδ δεϖελοπ 50 ς ιφ ιτσ ουτπυτ ισ οπερατεδ ιντο αν οπεν ορ σηορτ. Ιφ τηε οπεν ορ σηορτεδ ουτπυτ δεϖελοπσ 50ς, τηε νο ιναλ ϖολταγε ωουλδ βε 25 ς ανδ τηε νο ιναλ ποωερ ωουλδ βε $E^2/P = 25^2/50$ = 12.5 Ω. Ιονιζατιον οχχυρσ ατ 50 ς φορ α πρεσσυρε–δισταγχε, (τορρ–χ), προδυχτ οφ αβουτ 1 τορρ–χ . Χοαξ χαβλεσ υσεδ φορ φλιγητ σηουλδ βε ϖεντεδ το οπερατε φαρ βελοω τηε 1 τορρ-cm value, but this value could occur during abnormal test conditions or if a sealed pocket of air within the coax is suddenly released into its vacuum because the pocket's enclosure ruptures.

The requirements for every system are different. Every designer must be aware of the potential problems and consider them during the design stage. Often it is clear that the

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design is far from any problem conditions, but if this is not the case, the possibility of the problem should be investigated and changes made until a reliable design is obtained. JPL Technical Report 32-1500 provides information and lists references for greater detail.

2.1.4.4 Multipaction Breakdown in Transmission Cables. Multipaction can occur when an electric field accelerates electrons between two electrodes. The kinetic energy of an electron dissipated at each electrode impact must be high enough to dislodge more than a single secondary electron. The gas pressure must be low enough that the mean free path distance is greater than the electrode spacing, thus allowing the number of electrons traveling between the electrodes to increase. The RF frequency establishes the time between field reversals and the distance between the electrodes determines the voltage necessary to accelerate the electrons between the electrodes in the time allotted by the frequency. The electrons have maximum kinetic energy when the electric field reverses and starts slowing them down.

Electrons can be accelerated between electrodes by multiple cycles. The first half-cycle accelerates the electron between electrodes and the second half-cycle slows it down. The first half of the following cycles again accelerate the electron in the direction of the starting acceleration force. Successive cycles of acceleration followed by deceleration propel the electrons between electrodes. The intensity of the field gradients determines whether or not the electrons will have sufficient kinetic energy to produce secondary electrons at electrode impact. The electron kinetic energy is highest when the field reverses, but the requirement for multipaction is that it be above a minimum level at impact.

The multipaction can also exist between dielectrics. Dielectrics can have free electrons on their surfaces and the RF fields between two dielectric surfaces can produce a multipacting oscillation condition. The impact energy necessary to produce secondary emissions from dielectrics may be higher than conductors, but it does exist and the resulting sequence will erode the surfaces of the dielectric.

The lowest rms voltage required to produce multipaction is determined by the minimum energy necessary for multipaction to occur. The frequency must provide the voltage in such a manner that an electron impacts an electrode with the required energy just when the field reverses and starts accelerating electrons to the other electrode. This is the same as saying the first half-cycle of the frequency carries the electrons from one electrode to the other and the second half-cycle returns them.

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Multipaction is covered in the same document that was referenced for ionization (JPL Technical Report 32-1500). In general, as the frequency gets higher, the time interval that allows for the electron to be accelerated from one electrode to another is less. The voltage level must then be higher to provide a greater accelerating force. Figures presented in the technical report help determine if multipaction is possible. Testing may be required to show that adequate margin exists.

2.1.5 Cable Bundling and Crosstalk.In Section 2.1.1, it was mentioned that the signal current in the shield of a coaxial cable could couple a signal into the shield of an adjacent coaxial cable. The shield of a coaxial transmission line, when bundled with other signal wires, will also interact with the signal wires as it will interact with the shield of another coax cable. When forming a wire bundle, the signals that are carried on the wires in the bundle should be considered. Wires carrying high currents and high frequency signals produce large magnetic fields and wires that have large voltage changes capacitively couple their signal to adjacent wires. Wires that generate high noise should not be bundled with noise sensitive wires or cables. It might be advantages to having more than one wire bundle and separate sensitive receiving wires from noise generating wires. The designer shall review the wires in a common bundle and select a configuration that minimize the system crosstalk.

2.2 Waveguide and Waveguide Hardware

2.2.1 Rectangular Waveguide.The specifications for rectangular waveguide, (WR3—WR2300), are contained in the latest revision of EIA Standard RS-261. Table 1 of that document specifies the frequency range for the dominant, (TE_{10}), mode and the sizes, (with tolerances), of the controlled dimensions.

The EIA Standard RS-166, “Miniature Waveguide Flanges, Unpressurized Contact Type”, is for CMR90 to CMR284 rectangular waveguide flanges. The military specification for waveguide flanges is MIL-F-3922B. There are many slash sheets associated with the main specification that provide details on individual flanges.

2.2.2 Circular Waveguide.Circular waveguides are not commonly used on JPL spacecraft. As the result of trade-off studies, rectangular waveguides and coax cables are generally used. The EIA Standard RS-200 controls circular waveguides.

2.2.3 Power Handling, Multipaction and Ionization.In general, power handling capability for JPL spacecraft application is not a problem. Voltages within the waveguide and the temperatures of the waveguide increase as the power is increased. The peak power levels

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in waveguide that produce voltage breakdowns are in the kilowatt range. Most JPL spacecraft do not operate at power levels capable of producing waveguide voltage breakdown. As operation frequencies increase, the waveguide becomes smaller and the breakdown voltage becomes lower.

As an example, a WR10 waveguide, which is good to 110 GHz, breaks down at 4.6 kW. The 4.6 kW is a theoretical value at one atmosphere of 20ºC dry air with no safety factor included. Potential mismatches, irregularities in the waveguide, pressure within the waveguide and the temperature of the waveguide would all reduce the safe operating power level. A silver-plated waveguide would have the least attenuation, which could be as high as 1 dB/ft. At high power levels, the heating effect should be considered.

2.3 Printed Circuit Transmission Lines.

Controlled impedance circuits are essential to maintaining the integrity of high frequency signals. Transmission lines take different forms with the objective of providing a controlled impedance path as a signal propagates from one location to another. It is important that the input and the output impedance of the transmission line matches the impedance of its circuit connection. The circuit designer is to understand the system specifications and select the simplest reliable solution to satisfying the requirements.

2.3.1 Stripline. A printed circuit stripline configuration is a conductor embedded in a solid dielectric between two large reference planes. IPC-D-316, Sections 6.1, 6.1.1, 6.1.2, and 6.1.3 present the equations associated with different stripline configurations.

2.3.2 Microstrip. A printed circuit microstrip configuration is a transmission line consisting of a narrow conductor separated from a large ground plane by a dielectric. IPC-D-316, Section 6.2 presents the equation associated with a microstrip configuration.

2.3.3 Coplanar Waveguide and Coplanar Strips. A microwave trace located between ground plane traces on a common planar substrate surface can function as a waveguide. The requirements and equations associated with designing such a waveguide are contained in the following book:

Title:	*Microstrip Lines and Slotlines*
Authors:	K.C.Gupta, Ramesh Gary, and I.V.Barr.
Publishers:	Artech House, Inc.
Copyright:	1979

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Chapter 7 of the above book deals with coplanar waveguide and coplanar microwave strips. Coplanar microwave traces can maintain a constant impedance between the traces. The requirement and equations for coplanar traces are presented in the above referenced book.

2.3.4 Power Handling Capability. The average power that a particular transmission line can safely handle is dependent on the heat generated in the circuit and the dielectric strength of the insulation. The load impedance will determine the current and voltage necessary to produce the power. The acceptable average power rating of the circuit depends on the heat it generates. Heat changes the substrate properties and the physical dimensions, which in turn degrade the performance and can lead to failures. The dissipation losses of the conductor and the dielectric loss tangent of the insulating material must not cause any of the system material to exceed their maximum temperature rating. The average power handling capability of all substrate materials decreases as the frequency increases. The maximum average power handling capability of a circuit is expressed as:

$$\text{Maximum Average Power} = \frac{(T_{max} - T_{amb})}{T_{coef}}$$

Where:

T_{max}= Maximum allowed substrate temperature.

T_{am}= Maximum operating ambient temperature.

T_{coef}= Temperature rise/watt for substrate configuration at the operating frequency.

The peak power that a particular circuit can handle is dependent on the voltage that is applied to the dielectric. If the circuit operates into an open or short, the nominal voltage will double. The equation that determines the maximum allowed nominal peak power is:

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$$\rho_{\rho} = \frac{V^2}{4Z}$$

Where:

ρ_{ρ} = Maximum nominal peak power.

V = Breakdown voltage of the insulation.

Z = Characteristic impedance of the circuit.

The edges of circuit conductors concentrate electric fields along the surface of the substrate. The voltage produced by the peak power must remain below the dielectric strength of the media that exists between the trace and adjacent paths to ground. Connectors and their transition must also be considered in determining the breakdown of the dielectric isolating the peak power of the circuit.

The reference noted in Section 2.1.3 of this document presents additional information on the power handling capabilities of transmission lines. It deals with microstrip circuits but the equations are the same for stripline circuits. The text on pages 78 and 79 refers to some tables in the book that present some properties of various dielectric substrates.

2.3.5 Coupling and Crosstalk. Signals on a conductor can be coupled into other conductors by mutual inductance and capacitance. The coupling between conductors shall be kept to a minimum unless required by the design. Transferring signals from one signal line to another is referred to as “crosstalk.”

High-Speed digital circuits can malfunction because of crosstalk. For this reason, high-speed circuit standards describe crosstalk, establish rules to minimize crosstalk, and provide equations to determine the amplitude of crosstalk. The information provided about crosstalk in high-speed circuits is applicable to radio frequency circuits.

A good description of crosstalk is found in Section 3.4.9 of IPC-2141. The same document presents design rules that help to control crosstalk. IPC-D-317A, Sections 5.7 through 5.7.6 provide an in-depth model and formulas for determining the magnitude of crosstalk.

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2.4 Transitions

Impedance matching, (transitions), between different forms of transmission lines is difficult and requires special attention.

2.4.1 Coax-to-PWB. The coaxial transmission line is designed to provide distributed inductance and capacitance to the signal path. Changing its configuration for attachment to a PWB, (Printed Wiring Board), disturbs its impedance. The dielectric constant of the substrate, the trace width, and the distances of the trace from conducting materials affect the impedance of the PWB. There are good computer programs that enable the design engineer to obtain the impedance transformation required. The design engineer shall use a proven computer program to establish the match.

Connector manufacturers provide assemblies, (launchers), designed to transform from a coaxial transmission line to a pin that is connected to the circuit board. The method of attaching the pin to the circuit board is extremely important. Discontinuities at the pin attachment must be minimized to get maximum electrical performance from the connector. The launchers come with different size pins that allow reasonable matches when properly installed. Physical steps at the attachment produce electrical discontinuities. Adjusting or tweaking the circuit at the pin to circuit attachment may be necessary to obtain the desired match. When the launcher's pin diameter is too large, the interface introduces inductance. When too small, it introduces capacitance.

The mechanical configuration of the pin-to-line attachment must be reliable over environment exposures. Trade-offs may be required to satisfy the electrical requirement and survive the environment. Differential expansion of materials involved could separate the pin-to-line connection during thermal transitions. Vibration or shock could effect the pin-to-line attachment. A looped-gold ribbon or a sliding contact is often used but most of these attachment methods introduce a greater discontinuity than a direct connection. A prototype of the interface should be evaluated with a fast rise-time signal to determine if the coaxial to circuit attachment is inductive of capacitive and the discontinuity should be tuned out with inductance or capacitance. Launchers with their round pins flattened at the circuit attachment portion are available if the design benefits from the change.

The four most common methods of attaching launchers-to-circuit interfaces are:

(1) Direct pin-to-line bond using solder or conductive epoxy.

(2) Gold ribbon from pin to trace with play for relative movement.

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(3) Sliding contact with female pin bonded to a microstrip line.

(4) Mechanical pressure to hold the pin in contact with the microstrip.

Microstrip is the most commonly used circuit for a coaxial interface. This may be because very limited information about stripline performance above 18 GHz is available. The approximate upper frequency limit for TE stripline is reached when the ground plane spacing is a half wavelength. At 40 GHz, the ground plane spacing of 0.060 inches is required if a Duroid® dielectric is used. Unfortunately, in the 0.060-inch configuration moding can occur well below the 40GHz frequency. Careful centering and solid ground plane seals are essential if moding is to be avoided. Moding in the stripline configuration decays rapidly, but can cause a glitch. The connector circuit interface is one of the most sensitive areas for mode excitation. Ground plane clearances are critical for proper performance of any transition.

2.4.2 Waveguide-to-Coaxial Transmission Line.Commercial transition approved for flight shall be used. They shall be qualified for acceptable performance over their specified operating environment.

2.4.3 Through-Wall to PWB.Typically, a coaxial connector with the appropriate launcher accomplishes the transition through the enclosure wall to the printed wiring board. Many types of connectors are available. The launcher can be an integral part of the connector or the connector and the launcher can be joined by a pin connection. Separating the connector and the launcher provides a significant advantage. The most difficult part of the connector-circuit interlace is the launcher attachment to the circuit. During the initial assembly and test, a launcher separated from its connector could be easily replaced if required to obtain the desired match. Once a good match is obtained by compensation or whatever is required to obtain that match, the connector or its seal can be replaced if necessary without disturbing that match.

3 CONNECTORS

3.1 Frequency Consideration

The typical RF system uses coax cables to transfer the higher frequency signal from one location to another. Some synchronization, command, and data signals have high frequency components, but are not necessarily transferred by coaxial cables. The RF system designer shall be familiar with Appendix A, “Electrical Considerations” of IPC-C-406, “Design and Application Guidelines for Surface Mount Connectors.” This

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document presents guidelines for determining the effect of connectors on signals and recommends methods for reducing the interaction of signals.

3.2 RF Cables

JPL document FP513414 contains a section on cabling and wiring. The section lists JPL control documents, (ST_____), for RF connectors and RF coaxial cables. This document shall be used as a design reference when selecting RF cables. Other cable assemblies may be used but adequate evidence of their qualification will be required.

The JPL document FP513414 requires that semi-ridged cable material be thermally cycled and its insulator trimmed after the thermal cycling. It is a very important process to minimize thermal cycling stresses on complete cable assemblies. The solder connection between semi-ridged coaxial cable material and solder type connector often crack even after the thermal cycling process. For this reason most RF cable assemblies use crimped style connectors as presented in FP513414.

3.3 Bulkhead Type Connectors

When RF signals are passed through bulkheads and one side of the signal is connected to a circuit, microstrip or stripline designs are generally used to match the circuit impedance to the coaxial impedance. This type of a connector is considered a transition and is discussed in Section 2.4.1.

3.4 Power Handling, Multipaction

The power handling capability of cable material and connectors shall be considered during the design stage. They shall be capable of operating during a shorted or open conditioning, which produces standing waves at twice the normal voltage. The completed cables assembly shall be capable of testing at a power level 6 dB higher than normal when the test condition is properly matched.

Multipaction occurs at deep vacuum when the conditions described in Section 2.1.4.4 are present. Connectors should be evaluated as per Section 2.1.4.4.

3.4.1 Venting. Venting allows gas to escape from enclosures when the atmospheric pressure decreases. This relieves the stress induced by pressure differential and prevents the enclosure from dwelling at pressures that allow arcing to occur. Cable assemblies will probably be capable of handling pressure differences, but if voltages in the enclosure are above 50 V_{rms}, arcing could occur at a particular pressure, (critical pressure), that would

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be determined by the distance between the charged electrodes. If the rms voltages in the enclosure exceed 50 V under any possible impedance match, special consideration should be given to the venting of the cable assembly. During testing or flight, unplanned events can occur which take the enclosure to critical pressure. The design should not be degraded by such events.

The general rule for venting an enclosure is that V/A < 2000 inches. V is volume in cubic inches and A is the venting area in square inches. The size of each vent opening shall not create EMC problems. Fine screens are available with many small holes which, combined, provide a large venting area. The EMC properties of any screen used for venting shall be evaluated prior to its selection. Section 7.2.4 discusses the use of waveguides beyond cutoff for venting purposes.

3.4.2 O-Rings.O-rings are sometimes used as a connector hermetic seal. If the connector is capable of safe operation at critical pressure, the O-ring may be used. If critical pressure conditions such as those discussed in Section 3.4.1 exist, the quality of the enclosure seal shall be shown to maintain a pressure above any potentially damaging region during the duration of the space mission.

4 PRINTED WIRING BOARDS

IPC-D-316, “Design Guide for Microwave Circuit Boards Utilizing Soft Substrates” has been selected as the primary document for JPL microwave designs. It references IPC-D-275, “Design Standard for Rigid Printed Boards and Rigid Printed Board Assemblies”, which is the document specified in JPL-D-8208, SECTION3.5, “Surface Mount Technology.” Any deviation from IPC-D-275 specified in SECTION3.5 shall apply to this section. Build documentation for the radio frequency subsystem shall take precedence over any requirement of this section.

4.1 Design Rule Exceptions to IPC-D-316

A review of IPC-D-316 identifies several areas that are not JPL preferred methods. The following sub-sections identify changes to IPC-D-316 when it is used by JPL.

- Change Section 1.3 “Terms and Definitions.” On page 2, change the definition of “Return Loss” to “The return loss is generally expressed in dB as the ratio of the reflected signal to the forward signal.”

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- Change Section 2.1 “IPC Applicable Document” which is found on Page 3 as follows: Replace “IPC-HF-318, Microwave End Product Board Inspection and Test” to “IPC-6018” with the same title.
- Change Figure 1 “Microwave Circuit Design Flowchart” on page 4 as follows:

  Change the first block following “TASK ASSIGNED”, which reads “Literature Search, Design Option, List Option Specs, Select Best Option”, by adding: “Select Transmission Line Type.”

  Add a new block following above block change. The new block will require a “Peer Design Review” prior to proceeding with the details of the design.

  The block following the above block shall be changed from “Transmission Line Type, Materials/Components” to “Materials/Components.”
- Change Section 4.1 “Design Features Printed” on page 5 of IPC-D-316: Change the first and second sentence of the text by replacing “IPC-HF-318” with “IPC-6018.”
- Add to “Master Drawing” in Section 4.2, page 5, the sentence: “The material to be used shall be specified.”
- Add to Section 5.1, “Microwave Printer Circuit Board Material”, page 6, the sentence: “The specification sheets for IPC-L-125/01 through 125/08 are presented on pages 20-27 of the document ANS/IPC-L-125 ‘Specifications for Plastic Substrates Clad or Unclad for High-Speed/High-Frequency Interconnections.’ Additional information on properties of circuit board material may be found in Appendix B of IPC-D-317A.”
- Change Section 5.3.2.4, “Gold”, page 9, as follows:

  Remove the first part of the second sentence, (“It is easily soldered”), and replace with “It.” The first part of the second sentence becomes: “It is ductile.” At the end of the first paragraph, add the sentence: “When soldering gold plated surfaces use the JPL double tinning process of D-8208 Section 3.14, ‘Component Mounting/Soldering’, Section 2.2.3.2, ‘Gold-plated Lead and Terminals.’”

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- Change Section 6.1.1, “Narrow Traces”, on page 11 as follows:

  The first sentence says, “For narrow traces (A > 0.35)” but should be: “For narrow traces (A < 0.35).”

4.2 IPC-2141, “Controlled Impedance Circuit Boards and High-Speed Logic Design.”

This document deals with frequencies in the microwave range. The document is referenced in Section 6, “Digital Logic.” The sections of IPC-2141 that are pertinent to the microwave printed circuit boards are listed below.

- Section 3.2.1, “Connectors”
- Section 3.2.2, “Cables”
- Section 3.3, “Printed Board and Printed Board Assemblies”
- Section 3.3.1, “Board Design”
- Section 3.4, “Performance Requirements”
- Section 3.4.1, “Power Distribution”
- Section 3.4.2, “Relative Permittivity (Dielectric Constant)”
- Section 3.4.3, “Relative Permittivity and Frequency Relationship.”
- Section 3.4.4, “Critical Signal Speed.” This section deals with high frequency digital signals like clock frequencies in some Microwave designs.
- Section 3.4.5, “Capacitive Line versus Controlled Impedance Line Environment.”
- Section 3.4.5.1, “Capacitive Line.”
- Section 3.4.5.2, “Controlled Impedance.”
- Section 3.4.6, “Bandwidth.”
- Section 3.4.7, “Propagation Time.”
- Section 3.4.7.1, “Propagation Delay Time.”
- Section 3.4.8, “Signal Loading Effect.”
- Section 3.4.9, “Crosstalk.”

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- Section 3.4.10, “Signal Attenuation.”
- Section 3.4.12.5, “V_{cc}/Ground Bounce.”
- Section 3.4.13, “Switching Noise.”
- Section 3.4.14, “Other Parasitic Noise.”
- Section 3.4.15, “Noise Budget/Noise Margin.”
- Section 3.5, “Power Distribution.”
- Section 3.5.1, “DC Power Distribution.”
- Section 3.5.2, “AC Power Distribution.”
- Section 4.6, “Crosstalk Rules.”
- Section 4.6.1, “Crosstalk Implementation.”
- Section 4.7, “Controlled Impedance Coupon Design Rules.”
- Section 4.8, “Decoupling/Capacitor Rule.”
- Section 4.8.1, “Decoupling Capacitance.”
- Section 4.8.2, “Transient Capacitance Considerations.”
- Section 4.8.3, “Line Charging Capacitance.”
- Section 4.8.4, “Low Frequency (Bulk) Capacitance.”
- Section 4.8.5, “Capacitor Model.”
- Section 4.8.6, “Decoupling/Capacitor Design Rules.”

4.3 Refining the Design for Prototype Production

The prototype design will be used to justify the design for flight. This section presents the rules that should be applied to the final design. These same rules should have been considered in the previous design stages to allow an easy transition into the prototype production.

- IPC-2141, Section 5, “Design for Manufacturing.”
- IPC-2141, Section 6, “Data Description.”
- IPC-2141, Section 7, “Material.”

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4.4 Ground Plane to Chassis Connection

The RF circuitry should be shielded from chassis by a RF ground plane. The portion of the RF circuitry that is connected to RF ground shall be tied to the ground plane as soon as it is practical. The inductance between two locations will be less in the ground plane than in a trace.

The RF ground plane shall be connected to the chassis by a low inductance and a low resistance path. The ground plane then acts as a good electrostatic shield and prevents chassis noise from disturbing the RF circuitry.

4.5 Plating, Power Handling and Heat Sink

IPC-D-316 presents general requirements for plating of RF terminal boards. When the terminal board is required to handle high power, special plating may be advisable. Thicker plating spreads the heat over a broader area with a lower temperature gradient. The secret to being able to handle higher power is to remove the heat from its source. The thicker plating starts the process but it is not a reservoir for storing the heat. Multiple plated through holes can be used to move the heat to the underside of the terminal board where the heat finds a lower thermal resistance to chassis. The chassis should provide a method to transfer the heat from the power handling circuitry.

4.6 Testing

The terminal board is an integral part of the RF circuit design. It requires component performance testing like the rest of the circuit. The completed circuit board, before any circuit board assembly takes place, shall be tested to IPC-6018, “Microwave End Product Board Inspection and Test.”

5 COMPONENTS

5.1 Mounting Conventional Components

Conventional components shall be mounted per the requirements of JPL-D-8208, SECTION3.13, “Component Mounting/Soldering.” Any deviations from SECTION3.13 shall be approved and clearly identified on the assembly drawings.

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5.2 Surface Mounted Components

Surface mounted components shall conform to the requirements of JPL-D-8208, SECTION3.5, “Surface Mount Technology.” Any deviations from SECTION3.5 shall be approved and clearly identified on the assembly drawings.

5.3 RF Components

Mounting of any unique RF component shall be clearly defined on the assembly drawing. The RF designer and the mechanical engineer shall work together to obtain an acceptable packaging solution.

5.4 High-Power Precaution

5.4.1 High-Q Multipliers. Voltages and currents in high-Q circuits reach very high levels. Such circuits should be modeled and computer analyzed to predict their performance. The configuration of the circuit shall be reviewed for potential stress locations. The validity of the analysis shall be substantiated by test results.

5.4.2 Current Density. Current levels at the various locations of the circuit should be obtained from the computer analysis. The circuit elements shall be evaluated for potential stress. Current distribution in semiconductors is not necessarily uniformed. Manufacturer specifications shall be reviewed to verify that components are operated at safe levels.

5.4.3 High Voltage. High peak and steady-state voltages may not produce early failures but may degrade material in a manner that produces a failure years later. High voltages can produce arcing at reduced pressures, (JPL-D-8208, SECTION3.9, “High-Voltage Requirements”) or multipaction at very low pressures. Arcing can occur at RF voltages as low as 50 V_{rms} if the pressure distance product is at a critical level.

5.4.4 Multipaction. Multipaction occurs when electrons are accelerated between electrodes and produce secondary electrons at each electrode impact. The conditions necessary to produce multipaction are presented in Section 2.1.4.4. A multipaction breakdown has been observed at RF voltages as lows as 25 V_{rms}.

6 DIGITAL LOGIC

RF systems typically contain high-speed logic for clock inputs and intermediate frequency, (IF), processing. The rules for processing the high frequency digital signals are similar to those used for RF. Signal propagation time is more critical for digital circuits. The clock rates are less than the higher frequency microwave circuits, but fast

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rise times are critical for digital circuits. The component part types used in the circuits and the physical construction of the circuits limit the fast rise times that transfer the signal between devices.

IPC-2141, “Controlled Impedance Circuit Boards and High-Speed Logic Design”, reinforces much of the information presented in IPC-D-316, “Design Guide for Microwave Circuit Boards Utilizing Soft Substrates.” IPC-2141 is well written and gives examples of special considerations for reliable high-speed digital circuits.

IPC-D-317A, “Design Guidelines for Electronic Packaging Utilizing High-Speed Techniques” presents the details of how to analyze and implement designs utilizing high-speed components. The references listed at the end of the document provide greater detail on specific topics.

6.1 Characteristics of Digital Devices Used in Logic Designs

Table 3 of IPC-D-317A lists some typical data for a few logic families. Appendix A of the same document presents more detailed information on some of the devices.

6.2 Properties of Different Board Types.

Paragraphs of 4.1 in IPC-D-317A contain meaningful information about printed circuit boards. Appendix B of IPC-D-317A list some of the material properties associated with the different board types.

6.3 Circuit Interfaces

Circuit interfaces are one of the major factors in system performance. IPC-2141, “Controlled Impedance Circuit Boards and High-Speed Logic Design”, Sections 3.0 “Engineering Design Overview” and 4.0 “Design of Controlled Impedance Circuits” are devoted to presenting interface requirements, concerns, and mathematical relationships. The RF designer should be familiar with the information presented in both sections.

6.3.1 Burgeon Plot.A graphical method of finding the transients in a transmission line terminated by nonlinear resistances is presented in Section 5.6.8.1 of IPC-D-317A.

6.3.2 Lattice Diagram.The lattice diagram can be used to determine the reflection waveform established by a circuit. Section 5.6.8.2 of IPC-D-317A presents information relative to a lattice diagram.

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6.4 Logic Problem Areas

High-speed logic design in a radio frequency system requires special attention to details. It is required that the designer of any RF system be familiar with the information presented in IPC-D-317A and IPC-2141. The designer should use the information presented in the documents to implement the process recommended in Figure 1 of IPC-D-317A to arrive at a design concept prior to starting detailed circuit designs. The designer shall consider each section presented in the document and be satisfied that the resulting design represents a reasonable compromise of existing information. Often circuits proven by previous experience can be phase into the design, but the steps presented in Figure 1 should be followed to avoid costly problems because all aspects of the design are not considered at the beginning of the project.

7 EMI/RFI/ESD

EMI, (Electromagnetic Interference), requirements are imposed on all S/C subsystems. The basic EMI requirement is found in MIL-STD-461C, Part 3, Category A, “Equipment Installed on Spacecraft or Launch Vehicles”. The basic requirements are generally supplemented by additional project requirements. The EMI specification controls the electromagnetic, (EM), environment of the S/C. It places limits on how much EM energy can be emitted from the RFS Subsystem and defines its external interfacing EM environment. EMI is also of great concern within any subsystem. Operation of any subsystem circuit should not result in performance degradation of the hardware. RFI, (Radio Frequency Interference), is considered a type of EMI.

EMC, (Electromagnetic Compatibility), is achieved when the effects the EM environment are acceptable or negligible. The following are sub-topic guidelines to aid the designer in providing a RF system which satisfies the EMC requirements. As a general practice, S/C sub-systems are EMC-tested to verify that the EM energy generated by them are within specified limits and that when they are subjected to specified external EM limits, their performance is acceptable. MIL-STD-462 or its equivalent is used to specify the test methods.

ESD, (Electrostatic Discharge), occurs when mechanisms for generating electrification charges exist and arc transfers charge to a different potential. ESD that occurs at a relatively steady state is refereed to as “Corona Discharge.” Lightning is a form of ESD in that a charge difference exists between a cloud and another cloud or the earth. The arc

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that transfers the charge from the cloud and neutralizes the electrostatic field is called lightning.

The energy of an ESD arc is dissipated by EM radiation into space and heat developed in the resistive components contained in the path of the current. If the path elements are reactive, the discharge path may form a resonance circuit. The dominant EM fields radiated by the arc then vary in synchronism with the resonant circuit. The starting and the stopping of an arc always produce a broad EMI frequency band. Circuit components in the vicinity of an arc may require shielding. The standard test for ESD sensitivity is to charge a 500-pF capacitor to 25,000 volts and then discharge it through an arc.

7.1 Enclosures

The critical part of any RF enclosure is how well its penetrations or apertures are controlled. All RF enclosures have inputs and outputs and therefore, require penetrations. The penetrations should keep out unwanted signals and prevent EMI emissions from leaving the enclosure.

7.1.1 Chassis.Microwave and radio frequency chassis shall be as described in D-8208, SECTION3.3-1.3.4. Chassis seams shall be completely joined electrically to prevent any EM leakage. EMI gaskets for noise shielding shall be used when required by the design.

7.1.2 Waveguide Moding.Cavities formed by an enclosure can function as a section of waveguide. Unfavorable combinations of enclosure configurations and excitation frequencies can start oscillations within the assembly. A good example of a problem design would be to assemble an x-band (8.4 GHz) circuit in an enclosure that resembled WR112 waveguide. During the packaging state, the designer shall avoid enclosures that can function as a section of waveguide for any operational frequencies of the enclosed circuit.

7.1.3 Plating, Contact Areas, Lids, and Covers.Interfaces requiring good electrical conductivity must remain free of corrosion. Lids and covers will not provide a good shield unless their interfaces provided low electrical impedance paths. Plating with the proper metals can produce low impedance, corrosion free interfaces. Interfacing metals shall be selected for low galvanic interaction. Table III of MIL-STD-1250 (MI) indicates permissible interfaces. Plating materials should be carefully chosen to provide corrosion control and effective shielding.

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When screws are used to attach lids or covers, the spacing of the screws is important. If no gasket is used the spaces between screws are considered as potential radiators. For effective shielding, (≥ 60dB), the distance between screws should not exceed 10% of the wavelength of the highest frequency to be attenuated. Table 3.10-1 below indicates the attenuation of a 200MHz, (wavelength of 59.06 inches), signal by a cover with a contact width of 0.5 inches and screw spacing as indicated in the table.

Table 3.10-1 Screw Spacing

Shielding Attenuation, (dB)	Screw Spacing	
	Inches	Wavelengths
20	69.0	1.17*
30	39.0	0.66*
40	21.5	0.36*
50	12.0	0.20*
60	6.85	0.12
70	3.8	0.06
80	2.1	0.04
90	1.15	0.019
100	0.65	0.011*

* Extrapolated Data

7.2 Shielding

To provide effective shielding, the fundamentals of the problem must be understood. Is the field electric or magnets? What are the frequencies involved? What circuits are sensitive to interference and what is the distance from the radiating source to the sensitive circuit? Early in the design, after significant radiation sources and sensitive circuits are identified, circuit layouts and methods of shielding should be considered.

The best shielding material is dependent on the application. Solid materials are preferred; aluminum is the solid material most often used. Composite materials are sometimes used; their effectiveness varies greatly for different material types. A large portion of a shield's effectiveness against electromagnetic fields is its ability to reflect radiation at the shield surface. Impedance mismatches between the radiation propagation medium and the shield's surfaces reflect much of the energy. Wire mesh or fine screens

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are effective at lower frequencies. Gaskets at metal interfaces may sometimes be required to provide adequate EMI shielding. Good grounding of any shield is necessary if the shield is not to function as an intermediate voltage plane.

7.2.1 Electrostatic Fields. Oscillating charges on an equal-potential surface produce an electrostatic field that transfers charges to other surfaces by mutual capacitance. If the electrostatic field transfers charge to a circuit location, which is not connected to ground, that location develops a voltage as the charge finds a conductive path to ground. This fact makes electrostatic shielding relatively simple. A grounded conductor should intercept electrostatic fields that would connect an electrostatic source to a sensitive circuit location.

The electrostatic field is a high impedance field, (Z = E/H), and is reflected by grounded conductors because of the large impedance mismatch. Nomographs for determining electric field losses are presented in Section 7.2.6. The closer the shield is to the source, the more effective it is because the electrostatic field impedance decreases as it propagates away from its source.

7.2.2 Magnetic Fields. Charged particle motion is the primary source of magnetic fields. These magnetic fields transfer energy to adjacent elements by mutual inductance. The attenuation of magnetic fields is accomplished primarily by absorption losses of the propagating materials. At low frequencies, (10 Hz to 3 kHz, approximately), shielding against magnetic fields is difficult. There are absorptive materials that are generally adequate for the higher frequency range. A magnetic field is a low impedance field (Z = E/H) and is attenuated most by magnetic materials. The effectiveness of reflective type shielding increases when placed further from its source because the magnetic field impedance increases as it moves away from that source. At the higher frequencies, coupling between wires and discontinuities (opening) in the shields prove to be the biggest problem. RF coils, transformers and solenoids are circuit elements that utilize current (charge particles) carrying wires, which produce magnetic fields. Without shielding, radiated fields diminish with distance at about 12dB/octive for typical current elements and 18dB/octive for solenoids. Section 7.2.6 presents nomographs pertaining to absorption losses and reflective losses as a function of frequency and material.

7.2.3 Electromagnetic Fields. Electromagnetic fields contain both electric (varying electrostatic fields) and magnetic components. Both components exist simultaneously in any electromagnetic field. Close to the radiation source, either of the two components can dominate the other. The ratio of the magnitude of the electric component to that of

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the magnetic component is the impedance of the field (Z = E/H). Most of the electromagnetic field close to the radiator (<1 wavelength) that is not absorbed by external elements is reabsorbed by the radiator. The energy that is not reabsorbed and allowed to propagate freely through space will have impedance of 376.7Ω, (Z = E/H = 376.7).

7.2.4 Waveguide Beyond Cutoff. Typical enclosures are required to be vented for space application. The preferred method of providing an opening in an enclosure and avoiding EMI problems is to have the opening function as a waveguide below cutoff. The hole then functions as a high-pass filter. The attenuation of EM energy passing through the hole (circular waveguide) is frequency dependent and is defined by the following equation:

$$A_c = 31.95\left(\frac{L_c}{D}\right)\sqrt{1-\left(\frac{Df}{6920}\right)^2}$$

Where:

A_c = Attenuation of circular waveguide, (dB).

D = Diameter of opening, (in.).

L_c = Length of cylinder with diameter D (in.).

6920/D = Cutoff frequency of a cylinder, (MHz).

f = Frequency being attenuated, (MHz).

A rectangular waveguide, (W.G.), functioning as a vent would also function as a high-pass filter for frequencies above its cutoff frequency:

$$A_r = 27.3\left(\frac{L_r}{W}\right)\sqrt{1-\left(\frac{wf}{5910}\right)^2}$$

Where:

A_r = Attenuation of rectangular waveguide, (dB).

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L_r = Length of rectangular waveguide, (in.).

W = Largest inside dimension of rectangle, (in.).

5910/W = Cutoff frequency of rectangular waveguide, (MHz).

= Frequency being attenuated, (MHz).

A circular aperture forming a cylinder with a length that is negligible relative to the radius, yields field intensity at a given distance from the aperture that is proportional to the cube of the radius. When the mechanical design requires large apertures, a cover with shielding material may be used. The shielding material may take the form of perforated metal sheets, wire mesh or honeycomb. The manufacturer of such shields should provide specifications for design purposes and test data with the hardware delivery.

7.2.5 Magnetics. Magnetics often require special shielding attention. They can generate high magnetic fields, which should be controlled near their source. Reflective shields are not effective, because the magnetic fields are at their lowest impedance when they originate. Mu metal or some other magnetic material provides the highest attenuation because of their absorption losses. The nomographs of absorption losses of different materials at different frequencies are presented in Section 7.2.6.1. As mentioned earlier and supported by the nomograph, low frequency magnetic fields are difficult to attenuate.

7.2.6 Shielding Effectiveness. Shielding reduces the magnitude of propagating EM fields by reflecting the energy in a different direction or converting some of the energy into heat by absorption. The reflection occurs because of impedance mismatches and the absorption occurs as the field moves the molecules within the propagating media. Both the reflection and the absorption characteristics depend on frequency and are related to the shielding material's conductivity and magnetic permeability. An equation exists that allows the calculation of absorption losses for plane waves, electric fields, and magnetic fields. Separate equations exist for the calculations of reflection losses for plane waves, electric fields or magnetic fields. The equations mentioned above and nomograph related to the equations are presented in the following subparagraphs.

7.2.6.1 Absorption Loss. The equation for absorption loss, (in dB), is:

$$A = 3.338 \times 10^{-3} T \sqrt{f\sigma}$$

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Where:

A = Absorption loss, (dB).

T = Thickness of the material, (mils).

f = Frequency, (Hz).

σ = Material's conductivity relative to copper.

= Material's magnetic permeability, vacuum = 1.

A review of the equation indicates that for a given thickness of material, the only variable is the frequency. This indicates that the absorption is very low at low frequencies and increases in dB as the square root of the frequency increase.

A nomograph for determining the absorption of any material is presented in Figure 3.10-1. The nomograph has 4 calibrated vertical lines and one uncalibrated vertical line. If the designer is required to use absorption to reduce the amplitude, (in dB), of EM energy at a particular frequency, the designer uses a straight edge to draw a line through the frequency, dB reduction required, and the uncalibrated vertical line. The thickness of material required to attenuate that frequency by the dB indicated is dependent on the material used. A line is next drawn through the $\times\sigma$ value for the material to be used and the intersection of the previously drawn line and the uncalibrated vertical line. Commonly used materials are indicated at their $\times\sigma$ value. Any material may be evaluated by calculating its $\times\sigma$ value and indicating it on the vertical $\times\sigma$ line. The second line that was added to the nomograph when extended, indicates the required thickness of material, (T in mils), to attenuate the frequency of concern by the desired number of dBs.If the designer has a known thickness of material, the designer can use the nomograph to calculate its absorption at any particular frequency. The designer draws a straight line between the thickness, (T in mils), and the material, ($\times\sigma$), value. The line passes through the uncalibrated line. A straight line is next drawn between the frequency to be absorbed and the intersection point of the uncalibrated line and the initial line drawn. The second line indicates the, (dB), value of that particular material with the known thickness evaluated.

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Table 3.10-2 presented below was obtained by the use of the nomograph.

Table 3.10-2 Absorption Losses

Frequency	Absorption, (dB)	Material & Thickness, (in.)	
		Aluminum	Mu Metal
1 kHz	60	0.55	0.020
10 kHz	60	0.2	0.006
1 MHz	60	0.018	0.0006

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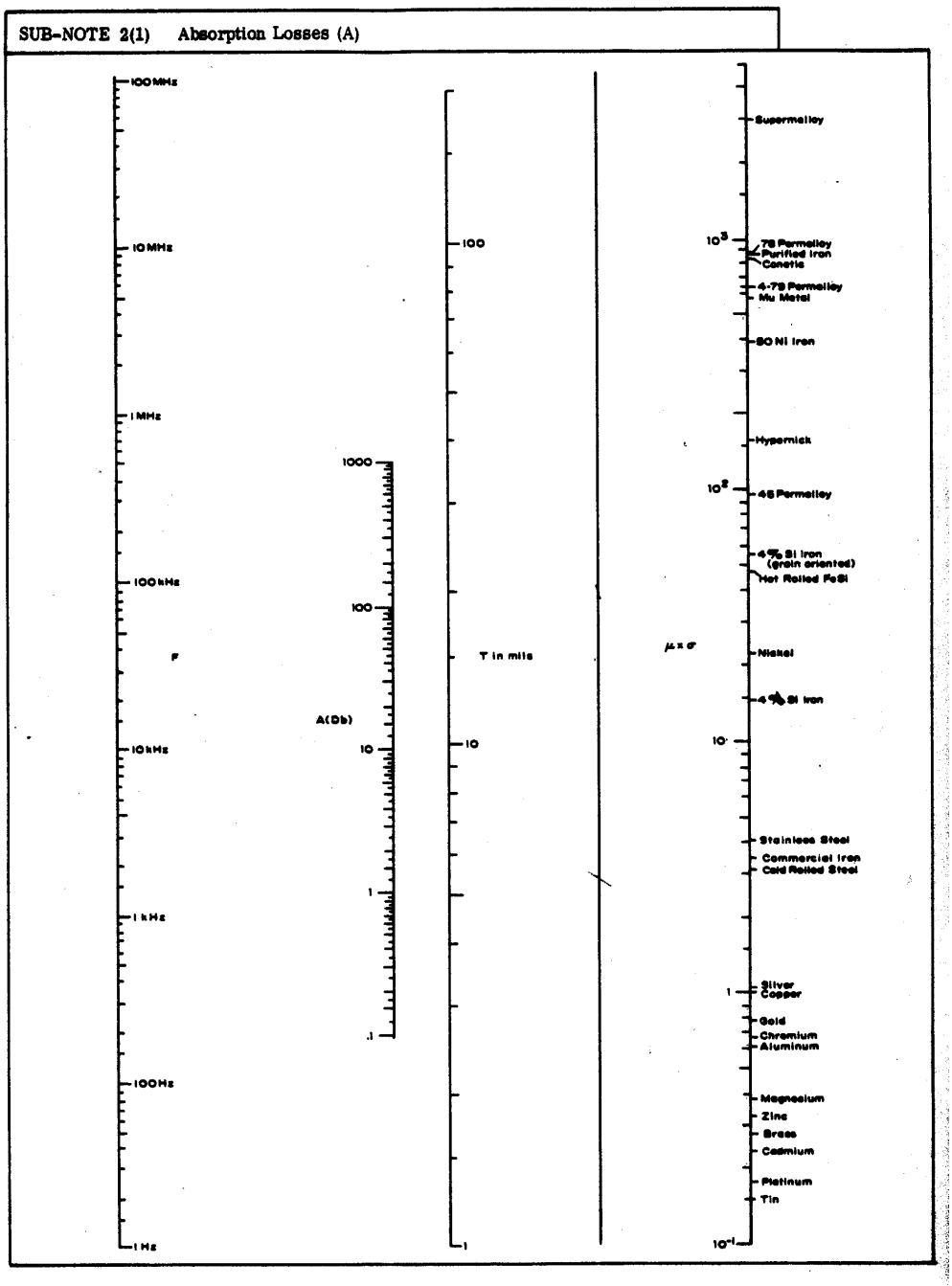

Figure 3.10-1 Absorption Losses, (A)

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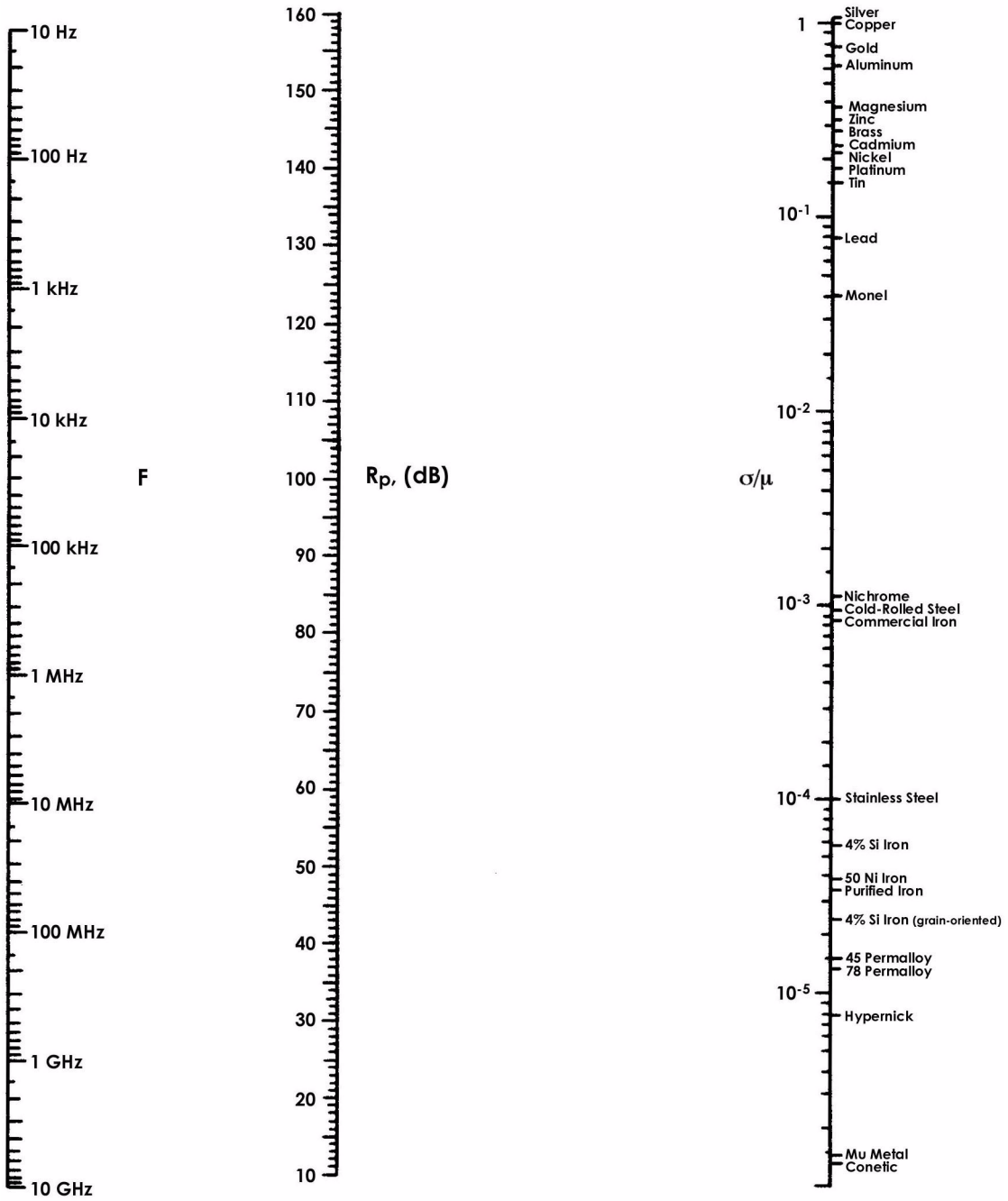

Figure 3.10-2 Plane Wave Reflection Losses, (R_ρ)

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7.2.6.2 Plane Wave Reflection Loss. The equation for calculating the plane wave reflection losses, (in dB), is:

$$R_\rho = \left(168 + 10 \log \frac{\sigma}{f}\right)$$

Where:

R_ρ = Plane Wave Reflection Losses, (dB) .

σ = Material's conductivity relative to copper.

= Material's magnetic permeability, vacuum = 1.

f = Frequency, (Hz).

A review of the equation indicates those materials with high conductivity, (σ), produce the greatest reflection. The reflection decreases as the magnetic properties of the material increases or the frequency increases.

A nomograph relative to the plane wave reflection losses is presented in Figure 3.10-2. It is very easy to use in that if your know the $\sigma/$ value of any material, you draw a straight line between the frequency of concern and the $\sigma/$ value. The R_ρ, (dB), is at the intersection of the added straight line and the calibrated R_ρ, (dB), line.

7.2.6.3 Electric Field Reflection Losses. The equation for calculating reflection losses for an electric field is:

$$R_e = 353.6 + 10\log \frac{\sigma}{f^3 \quad D^2}$$

Where:

R_e = Electric Field Reflection Losses, (dB).

σ = Material's conductivity relative to copper.

= Material's magnetic permeability, vacuum = 1.

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f = Frequency, (Hz).

D = Distance from radiation source to the reflective surface, (in.).

A review of the equation indicates those materials with a high conductivity to permeability ratio, (σ/), produce the greater electrostatic reflection losses. The closer the shield is to the source, the more effective it is; the higher the frequency, the less effective it is.

The electric field reflection losses nomograph is presented in Figure 3.10-3. A straight line through the frequency of concern and reflection loss required intersects the uncalibrated vertical line at a single point. Projected straight lines drawn from the σ/ value of a material and through the single point established on the uncalibrated line indicates the required distance between the source and the reflector to obtain the desired losses. If the distance is longer than required, the reflection loses will be less than required.

The point established on the uncalibrated line controls the relationship between the material and the rest of the nomograph. If you have a material at a known distance from a shield, a straight line should be drawn between the σ/ value for the material and the known distance indicated on the D, (inches), line. This line crosses the uncalibrated line and establishes the control point on the uncalibrated line. The reflection losses for any given frequency is next found by drawing a straight line between that frequency and the control point on the uncalibrated line; the reflection loss is indicated on the R_e, (dB), line where it is intersected by the line that joins the frequency to the control point.

Table 3.10-3 below was generated from the nomograph.

Table 3.10-3 Electric Field Reflection Losses

Frequency, (MHz)	Reflection Loss, (dB)	Material & Distance, (in.)	
		Aluminum	Mu Metal
100	60	400	0.6
100	115	0.6	0.001

NOTE: Aluminum at 0.6 inches is 55 dB better than Mu Metal at a distance of 0.6 inches.

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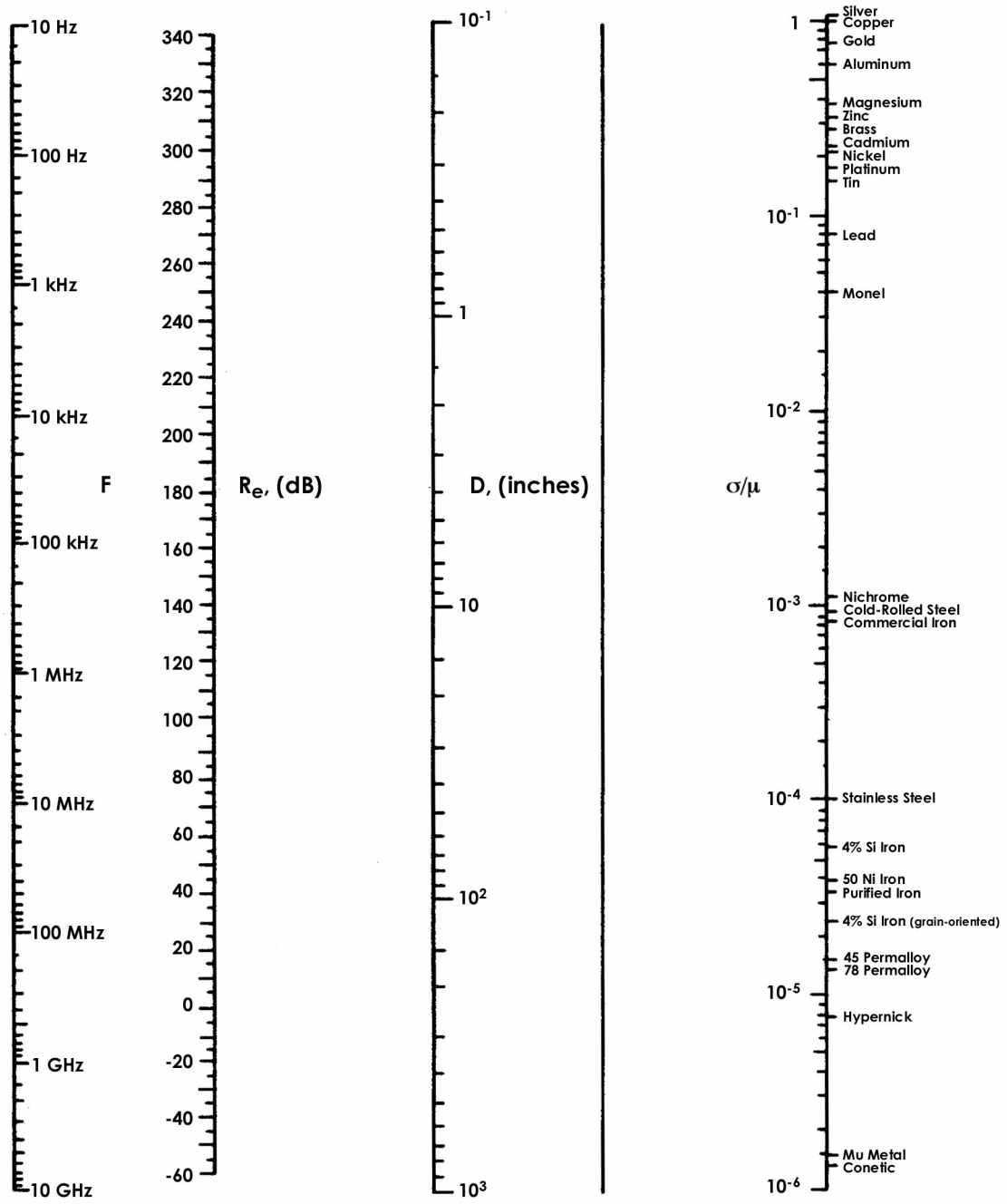

Figure 3.10-3 Electric Field Reflection Losses, (R_e)

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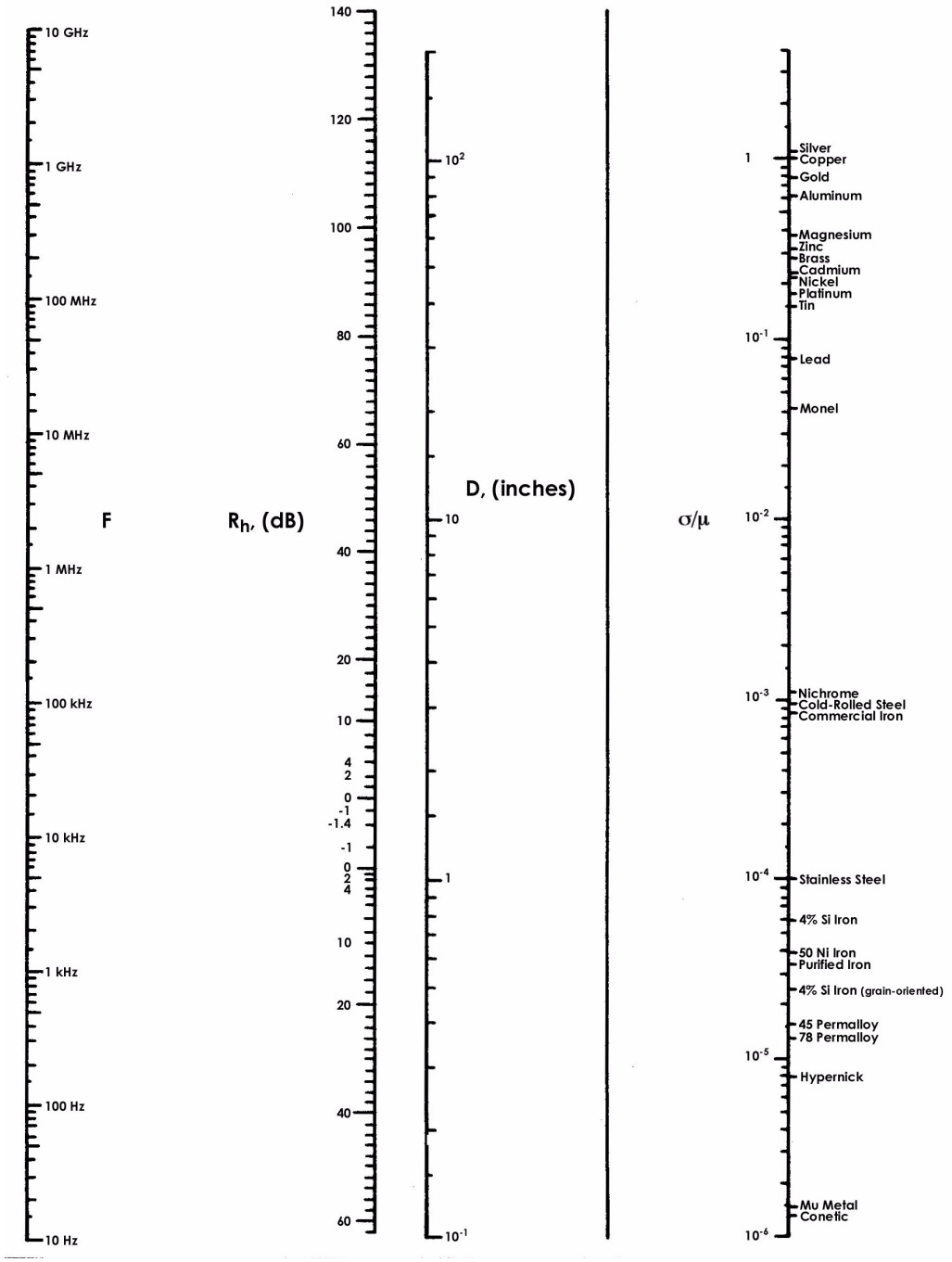

Figure 3.10-4 Magnetic Field Reflection Losses, (R_h)

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7.2.6.4 Magnetic Field Reflection Losses. The equation for calculating reflection losses for a magnetic field is:

$$R_h = 20\log\left(\frac{0.462}{D}\sqrt{\frac{}{f\sigma}} + 0.136D\sqrt{f\sigma} + 0.354\right)$$

Where:

R_h = Magnetic Field Reflection Losses, (dB).

σ = Material's conductivity relative to copper.

= Material's magnetic permeability, vacuum = 1.

f = Frequency, (Hz).

D = Distance from radiation source to the reflective surface, (inches).

A review of the equation indicates that the variables appear in two separate terms:

$$\frac{0.462}{D}\sqrt{\frac{}{f\sigma}} \quad \text{and} \quad 0.136D\sqrt{f\sigma} + 0.354$$

The effect of variations on each term is easily understood, but how they combined to produce the measured reflection losses is not clear. The table below helps to understand what may be encountered when placing shield of 2 different materials at different distances from the source of the magnetic field. The frequency is kept constant and the distance is expressed in % of a wavelength, (λ).

Table 3.10-4 Magnetic Field Reflection Losses

Frequency, (MHz)	Distance		Reflection Loss, (dB)	
	inches	%λ	Aluminum	Mu Metal
100	0.001	0.00085	3.3	31.6
100	0.01	0.0085	20.7	12.4
100	0.1	0.085	40.5	-0.9
100	1	0.85	60.5	6.3

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Table 3.10-4 Magnetic Field Reflection Losses

Frequency, (MHz)	Distance		Reflection Loss, (dB)	
	inches	%λ	Aluminum	Mu Metal
100	10	8.5	80.5	24.6
100	100	85	100.5	44.5

The nomograph that represents the equation is presented in Figure 3.10-4. It has the same variables as the nomograph for electric field reflection loss and is used in the same manor. Refer to Section 7.2.6.4 for information about the use of the nomograph.

7.3 Filters, Ferrite Beads and Suppressant Tubing.

Wires that enter or leave an enclosure must be filtered by some means. Power interfaces may involve some form of a switching regulator, which has fast rise and fall characteristics; therefore a power line filter may be required to suppress the noise produced by the switching regulator. The designer should be aware that filters composed of discrete inductors and capacitors develop resonant notches at higher frequencies because of lead lengths. Feed through filters that mount to the chassis may be required on all unshielded chassis penetrations to separate the noisy environment inside the enclosure from its external environment.

Passing the wire through a ferrite bead or beads can reduce the noise on a wire. The attenuation of a single bead with a permeability of 600 provides a peak attenuation of about 10 dB near 50 MHz. Its attenuation decreases above 50 MHz and it is totally ineffective at frequencies above 100 MHz. Thirty of the same beads on a single wire produces a peak attenuation of about 25 dB near 50 MHz and they are ineffective at frequencies above 150 MHz. One inch of suppressant tubing can provide the following insertion loss:

10 dB of insertion loss at 100 MHz, 40 dB of insertion loss at 1 GHz, and over 100 dB of insertion loss at 10 GHz. If ferrite beads or suppressant tubing are considered for a design, the material specification should be reviewed and samples tested on the functioning hardware prior to making them part of the final design.

In the microwave circuits of the RF system, special waveguide and strip-line filter designs are most commonly used. In unshielded areas, such filters can lose their effectiveness because of bypass leakage. Any aperture in the vicinity of the filter is a potential source of reduced filter performance.

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7.4 Good Practices

When considering EMI, it is important to think of every conductor as a receiving and transmitting antenna. This is of particular importance during circuit layout. Proper circuit layout can minimize the need for additional shielding. A good understanding of the circuit performance is required to effectively package the hardware. Enclosure penetrations shall be reviewed by the RF designer in order to determine which wires should be shielded and where filter blocks are required. High current loops, which form magnetic dipoles, shall be avoided. As mentioned earlier, magnetic fields are difficult to attenuate.

7.4.1 Circuit Layout.Prior to actual circuit layout, the sources of electromagnetic radiation and the circuits sensitive to interference should be identified. High impedance circuits are generally most sensitive to pick-up. During the initial layout, their location or some shielding configuration shall isolate EM sources and sensitive circuits. The shielding material type and location shall tentatively be established.

Transients should be suppressed at their source whenever possible. Slowing down fast rise and fall times should be considered; circuits may not require the speed provided by the components. The layout should minimize stray capacitance. As mentioned earlier, electrostatic fields are transferred to other locations by stray capacitance.

A modular packaging design may provide the needed isolation. A chassis with milled compartments generally provides the best separation. Aluminum chassis are inexpensive, lightweight and are excellent electrostatic shields.

7.4.2 Slot Radiators.The primary source of slot radiation from a well-designed chassis is improperly sealed intrusions. Frequent screws and the proper EMI gasket can reduce the slot lengths. An EMI gasket should be the right thickness to fill-in surface discontinuities and posses adequate resilience to allow the opening and resealing of the enclosure. The metal finishes shall provide good conductivity and be corrosion resistance. Various gasket material suppliers will provide information about the effectiveness of their products.

7.4.3 Magnetic Dipoles.During the circuit layout, the configuration of the current paths should be monitored regularly to avoid the creation of magnetic dipoles. Early detection of a circuit layout problem is beneficial. The current should not flow in a path that resembles a current loop.

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7.5 Grounding

Proper grounding is essential for stable performance. A good ground connection between the system reference ground plane and circuit board ground planes requires a low inductance path. Round wires and narrow printed circuits provide inductive paths that reduce the effectiveness of decoupling capacitors and filter. A twenty gauge round wire has a self-inductance of 300 to 400 nH/ft. At 100 MHz, a one inch length has a reactance of 1.5 to 2.1 Ω.

7.5.1 Ground Separation.The S/C power subsystem provides power to the RF subsystem. The S/C power is connected to chassis at a single point and must be isolated from chassis in the rest of the S/C to avoid ground loops. Each subsystem unitizes S/C power to generate its own power source that is isolated from S/C power. The subsystem power is then grounded to the S/C at a single point, except for the RF subsystem, (RFS). In the RFS, its chassis is used as a ground connection between modules a circuits. Signals to the RFS from other subsystem must be isolated from chassis in order to maintain the single point ground of that subsystem. In the RFS, any signals that originate from external isolated sources should be isolated from circuits operating from power with a different spacecraft grounding point. The level of isolation required is often specified by a spacecraft requirement.

The S/C chassis provides very low impedance between all subsystems. When the RFS is powered from a source other than the S/C, a low impedance path between the RFS chassis and its power source chassis must be provided. Heavy braided wires will provide an acceptable impedance. The power source should also have a heavy braided wire connecting it to a solid earth ground.

7.5.2 How Signals Flow.Signals that share a common path change according to the voltage developed across that path. That signal change applied to a sensitive circuit could present a problem. Consolidating multiple signals, shields or power returns into a single path requires careful consideration before implementation. When circuits share a common power source, circuit isolation shall be obtained by adequate filtering between stages.

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Hybrid Microelectronics and MCMs

This section defines the design and fabrication criteria for producing space flight qualified hybrid or MCM circuits.

The intent is to provide guidelines useful to circuit designers and/or circuit fabricators who need to deliver space qualified product to NASA. Ideally, a designer would review these requirements and meet with engineering representatives from Section 349 as soon as a completed circuit schematic is available. This initial contact should be scheduled prior to releasing a bill of material. Agreement should be reached on devices and materials prior to release of the bill of materials to purchasing.

1 DESIGN REQUIREMENTS

The following tasks must be finished before a hybrid or MCM design may be called complete. Finished is defined to mean that all documentation is not merely generated, but is completely signed off by all responsible parties.Unless otherwise approved, no material is to be purchased until the completed design package is available.

1.1 Design Package

A design package for a hybrid microcircuit or MCM module shall consist of the following:

1.1.1 Released Schematic Diagram.A completed electrical circuit schematic shall include the following information, as a minimum, for correct generation of substrate layout/routing. The schematic shall be fully released and signed off by responsible parties to be included in a correct bill of materials.

a. Part number, value and tolerance, and preferred reference identifier for all active and passive circuit elements

b. Input and output signal requirements

c. Power supply voltages for all conductor lines

d. Identified testpoints

e. Testing information (i.e., assembly test plan)

f. Pinout numbers and functions

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g. Identified burn-in circuit and load requirements

1.1.2 Released Bill of Materials. A completed bill of materials which agrees with the schematic shall be generated in compliance with the following:

a. The BOM shall include all the components within the schematic as well as any additional items required to complete the assembly.

b. Each item of the BOM shall include component name (or nomenclature), component type, the number or quantity of each component required, vendor name, and vendor code, if required.

1.1.3 Documentation Package.

1.1.3.1 Artwork Master Sets. Artwork is the geometric pattern used for the design of masks, screens, test patterns, etc. Artwork is required for thick film/LTCC deposit screens, thin film exposure masks, epoxy deposit screens, solder past deposit screens, and test pattern masks. All artwork shall conform to the following requirements:

a. All artwork shall contain fiducial alignment markings for aligning one level of pattern to the next. The type of fiducial marking may vary depending upon the application.

b. Circuit artwork: When creating artwork for the generation of circuitry, each layer of conductor, dielectric, ground plane.

1.1.3.2 Assembly Drawings. Finished/completed assembly drawings shall include, as a minimum, the following elements:

a. Top assembly outline drawing of deliverable module depicting the final deliverable configuration, maximum dimensions specified, pertinent markings such as ESD, pin numbering, part number, and supplier identifier.

b. Subassembly drawings shall show the module in a final assembled state and depict as many views as necessary for clarity of partial assemblies. Included in these drawings are exact component locations and orientations; all bonding wires, all bonding ribbons, any other required connectors, epoxies, solders.

c. Bonding wires and ribbons shall be identified by material type and diameter or dimension.

d. Other materials shall be labeled with a designator which corresponds to a line item on the parts list for correct identification.

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1.1.3.3 Parts lists /bills of material (BOM). Each subassembly shall have a corresponding parts list which includes the fabricated substrate, all active and passive devices used, all wires used, all ribbons used, all polymerics used, and all solders used. In addition, any other special elements such as partial assemblies or purchased devices are to be included.

1.1.3.4 Notes Lists/assembly Aids. Each subassembly shall have a corresponding notes list either on the subassembly print or as an additional stand alone document which indicates specific assembly techniques, assembly sequences, any special or unique technique required, or cautions concerning special handling.

1.1.3.5 Assembly Flow Diagrams. Flows shall be reviewed on a quarterly basis by responsible department personnel for accuracy. Updates shall be made as required.

Note: A flow diagram incorporating all essential process steps necessary for assembly of a standard hybrid /MCM is provided in FP513414. Flows for individual process steps are also available in FP513414.

1.1.3.6 Assembly Travelers. A traveler card is required for all space flight hybrid/MCM products built. The traveler is a historical record of work performed on each lot of assembled hybrids. The hybrid assembly traveler (HAT) provides the following functions:

a. A step by step sequence of operations, inspections, and in-process control points.

b. Traceability of all piece parts and materials. Any parts substitutions are to be recorded on the traveler document. This shall be signed and dated by the individual making this substitution.

c. Lot definition by means of a serial number system.

d. A roadmap of the build cycle. Each operation is linked to the approved and documented process of assembly.

e. Special process instructions or tools to be used shall be called out on the traveler which is specific for a particular assembly.

1.2 Process Specifications

All approved processes for assembly of space flight hybrid and MCM modules are documented and numbered as part of FP513414.

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1.3 Process Control

1.3.1 Assembly Area. Control and stability of a space flight qualified assembly area is maintained by:

a. Use of documented processes for assembly operations to ensure consistency and repeatable quality.

b. Verification of the use of these processes by sign-off on the build travelers.

c. Maintenance of training and certification of all assembly personnel. Training shall be periodically performed so that all assembly personnel working on space flight hardware are knowledgeable of all requirements for assembly of Class K devices.

d. Charting of yields of product built.(SPC methodology).

1.4 Inventory Control

1.4.1 Materials. General materials used in assembly of standard hybrid/MCM modules shall be stored within the laboratory work area in controlled conditions per the following requirements:

a. All bonding wire and all bonding ribbon shall be stored at ambient temperature in leakproof cabinets backfilled with dry nitrogen. (dew point equivalent -55°C or lower and oxygen content of 50 ppm or less).

b. All bonding tips shall be stored in labeled drawers. Manufacturers part number shall be used as the label identifier.

c. General use materials such as cotton tipped swabs, surgical gloves, finger protectors, glassware, tinfoil, etc. shall be stored in an orderly fashion in normal storage cabinets.

d. All solders paste, wire, foil shall be stored at ambient temperature in leakproof cabinets backfilled with dry nitrogen (dew point equivalent -55°C or lower or oxygen content of 50 ppm or less).

e. Test devices such as multimeters, temperature probes, measuring instruments, etc. shall be kept in one particular cabinet so that they are accessible to all personnel as required.

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f. Assembly kits. All materials kitted for specific jobs shall be stored in cabinets backfilled with dry nitrogen at ambient temperature. Each kit shall be kept in a separate cabinet or within a separate shelf of a multiple shelf cabinet to prevent any intermixing or loss of dedicated materials.

1.5 Quality Control

1.5.1 Classification. All hybrid /MCM modules produced for space flight applications shall be manufactured to satisfy the Class K Quality Assurance level as specified in Mil-PRF-38534.

a. A quality program shall be established and implemented following the requirements of, but not restricted to, Mil-Q-9858.

b. To assure that all hybrid /MCM devices fully satisfy the needs of the customer or procuring department, the devices shall undergo inspection and analysis by test during the assembly operations and after completion of assembly.

c. Verification by inspection is accomplished by comparing the characteristics of an item with the requirements imposed by specifications or purchase orders. Both individual component parts as well as completed assemblies shall be visually inspected to assure compliance to criteria of (a) the purchase document, (b) Mil-PRF-38534, and (c) Mil-Std-883, Methods 2009, 2010, 2017, and 2017.

d. Verification by testing is accomplished by subjecting an item to a set of controlled conditions per approved plans and procedures. During a test sequence, measured responses are recorded. Results are compared with analyses projections or previously known responses.

2 ELEMENT REQUIREMENTS DEFINED

2.1 Package Requirements

2.1.1 Packaging, (to include corresponding covers). Packaging for a hybrid/MCM circuit may vary depending upon application from a molded plastic enclosure to a fully hermetic metallic enclosure. The metallic hermetic package style is nearly always utilized for flight level circuits.

If the package and cover combination is selected from the listing of standard configurations given by a vendor, a dimensional drawing may not be required. However, the plating combination, for both the package and the cover must still be specified. If

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desired plating differs from the vendor's standard, restate the desired plating directly on the purchase order.

2.1.2 Nonstandard Purchases.If the desired package /cover combination is not standard, individual drawings for package and cover shall be made showing all required dimensions and tolerances, materials for package/cover, and plating alloys and thicknesses for package /cover will be specified

2.1.2.1 Purchase Order Information. Specific mechanical and /or electrical requirements will be stated on the purchase order. This may include pressurization, hermeticity, plating adhesion, outgassing, corrosion resistance, type of insulating glass /ceramic used in feedthroughs, impedance matching of feedthroughs, grounding of individual connector pins, etc.

2.1.2.2 Shipping Instructions. Shipping and delivery instructions for completed packages and covers is to be specific and clearly defined on the purchase order.

2.2 Substrate Requirements

The substrate is the support membrane for the functional circuit. The substrate may range from being a 2 mil thick sheet of polyimide to a 40 mil thick sheet of aluminum oxide. To define the substrate, the following callouts, as a minimum, must be given so that purchasing can procure the correct items:

2.2.1 Substrate Drawings.A specific drawing, fully dimensioned, must be made for each substrate used. The drawing will define all features, including holes, notches, radii of corners, thickness, flatness, and dielectric constant, if necessary.

2.2.2 Special Requirements.Any special requirements will also be noted on the drawing, such as: surface finish as related to height of imperfections allowed when required for high frequency circuits, porosity limits, or density requirements.

2.2.3 Metallization Requirements.Conductor and pad metallization requirements should be specifically called out using notes and drawing details if needed.

2.2.4 Passive Devices.Any passive devices which are integral to the deliverable substrate will be clearly defined within the drawing/drawing notes structure. Resistors should include value, tolerance, and TCR limits. Inductors and capacitors will define value and tolerance allowed.

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2.2.5 Special Testing. Any special testing, such as temperature cycling or burn-in testing will be specifically noted. Minimum levels for adhesion may be specified. The units used are most commonly lbs./in.2 or gms./cm.2 The test is performed by fastening a stud to a designated area of film using polymeric adhesive. Example: Minimum film adhesion will be 500 lbs./in2. An ability of the output pads to withstand several cycles of solder and rework may be specified. Example: Thick film pads for signal output are required to withstand 3 cycles of solder/desolder using Sn 63 alloy, RMA flux, and hand solder technique.

2.2.6 Shipping Instructions. Packaging and shipping instructions should be stated, giving the exact container part numbers to be used. Shipping instructions should be restated on the purchase order so that vendor has no misunderstanding.

2.3 Thick Film Metallization Requirements

Thick film circuitry generally consists of a substrate fabricated from ceramic followed by layers of deposited material which are conductive, non-conductive, or somewhat conductive. Conductive layers are usually referred to as conductors. Non-conductive layers are called insulators, or dielectric layers. Partially conductive materials are called resistors. These materials are usually deposited onto the ceramic base by means of screen printing. This is possible because the metallic and glass forming components are finely divided and suspended within a paste-like composition so that it will flow through a mesh screen and remain in place as a pattern without runout or smear. This pattern of paste is then sintered to a solid composition in a high temperature (800-900°C) furnace.

2.3.1 Conductive Ink. These inks are a combination of binder, glass forming frits, and conductive particles. The metallic particles may be gold, silver, copper, etc., or they may be a combination such as platinum/palladium/silver. Once the paste has been sintered, a conducting path is formed through the metal matrix. If the metal is one component, such as gold, the conductivity is very high. If the sintered metal layer is a solution or an alloy, conductivity may be slightly lower, but other desired properties, such as leach resistance to soldering may be achieved.

2.3.2 Purchase Order Information. The following items should be specified on a purchase order to assure equivalent material properties from batch to batch:

- Viscosity
- Container size

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- Particle size
- Conductivity range of fired ink

2.3.3 Resistive ink. The following material properties should be defined on the purchase order:

- Container size
- Viscosity limits
- Fired resistance, defined in ohms per square
- Temperature coefficient of resistance (TCR) of fired ink

2.3.4 Insulative ink (dielectric). The following material properties should be defined on the purchase order:

- Viscosity
- Container size
- Capacitance range of fired ink (xxx per thousandth of an inch)
- Breakdown voltage of fired ink (volts per thousandth of an inch)

2.4 Thin Film Metallization Requirements

Thin film metallization consists of multiple layers of deposited metals or metal alloys. The substrates on which the metals are deposited can vary from metal to silicon to ceramic (aluminum oxide) to polyimide (organic polymer). The composition combinations and varieties are many. The distinction between “thick film” and “thin film”, however, remains important. Each layer of a deposited “thick film” is approximately 12.5 microns thick (One micron = 1.0×10^{-6} meters). A single layer of deposited “thin film” metal may be only 5 microinches thick (One microinch = 1.0×10^{-6} inches). This means that the thick film layer is approximately 90 to 100 times the thickness of the thin film layer as deposited. It is possible to deposit “thin” films to greater thicknesses; 25 to 50 microns are sometimes done. However, this is not common practice due to the high cost incurred. The layer thickness of a “thin” film is significant, because a layer this thin is really of little use in a hybrid circuit. The functions of the metal layers in hybrid/MCM circuits are normally as a conductor run, a bonding pad, or as an external connection pad. To make a “thin “film usable, the thickness is frequently increased by plating an additional thickness of metal over the top of the thin film seed

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layer. In hybrid circuitry nomenclature, then, thin films actually refer to the initial deposited layer(s) and the additional plated layers.

2.4.1 Purchase Order Information.The following items should be specified on a purchase order when obtaining thin film substrates or circuits:

a. The substrate material type

b. The thin film composition defined in order of deposit. Example: Ti/Pt/Au, signifying that the composition desired would be titanium followed by platinum followed by gold.

c. The layer thickness of each metal type is also necessary. The callout is most frequently in microinches. Example: Ti = 100 m"/Pt = 250m"/Au = 80m".

d. If an annealing step is desired for stress relief it will be specified in terms of duration, temperature, and atmosphere. Example: Anneal 8 hours @ 200°C in vacuum.

e. To check for film quality and purity a short high temperature bake-out is performed to cause entrapped impurities to outgas creating bubbles in or delamination of the thin film.

Example: Bake 10 minutes at 400°C in nitrogen.

f. Adhesion quality of the film layer should be monitored by means of a tensile pull test.

A minimum acceptable level of force should be specified. The units used are most commonly lbs./in.2 or gms./cm.2 The test is performed by fastening a stud to a designated area of film using polymeric adhesive. Example: Minimum film adhesion will be 50 gms./cm.2.

2.5 Requirements for Bonding Wire

Interconnections between active devices, such as integrated circuits, and the conductor runs on the hybrid/ MCM substrate are most commonly made with small diameter wires.

2.5.1 Wire Requirements.Depending on the equipment used and/or the application within the circuit, different wire sizes and types are selected. Also the relative hardness or softness of the wire is sometimes varied to best fit the appropriate machine. Wire specifications for purchasing shall be as follows:

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a. Wire alloy or wire element purity. Example: Wire is gold at 99.9999% purity.

b. Wire diameters are specified in inches, usually to the 1/ten-thousandth of an inch, or the 4th decimal position. Example: Wire diameter will be 0.0012" 6.00005".

c. Mechanical/physical characteristics are frequently specified to improve bonding or to aid in feeding the wire through the equipment. The callout adheres to the technique used to create the wire, which is to draw it through a series of dies. Example: Wire is to be fully annealed; elongation will be 8-12%; ultimate tensile strength to be 3000 lbs. minimum.

d. Packaging information must be specified. Example: Wire is supplied on x" diameter spools individually packaged and labeled.

e. Traceability information and certification of compliance are to be included with each lot of material shipped. The date the wire was fabricated, the lot fabrication number, and the ingot melt number are required.

2.6 Requirements for Bonding Tools

Bonding tools for wirebonding are an extremely important parameter in achieving reliable, repeatable interconnection bonds. The following are characteristics which must be specified when ordering tools for wirebonding or ribbon bonding:

a. Tool length

b. Tool diameter

c. Material composition

d. Bond foot length and width

e. Surface finish of bond foot

f. Wire feed hole diameter

g. Wire feed hole angle

h. Surface finish of wire feed hole

i. Radii polishing

j. Tool weight

Note: Due to the many factors involved in specifying the tools, no tools are to be ordered without the review and approval of the process engineers.

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2.7 Requirements for Polymerics

Any organic compounds which are going to be selected for use in space flight hybrids/MCMs must have high purity, low outgassing, low levels of extractable ionics, and excellent strength at low temperature. Due to these requirements, a material which is acceptable for other electronic assembly applications, may not be acceptable for use in a hybrid package.

Goddard Space Flight Center Reliability Engineering Group has tested many of the polymeric materials which are commercially available and has gathered detailed data on outgassing of the cured polymer. As a first filter, only items which appear on this list should be considered as viable candidates for hybrid use.

Due to a variety of other factors, such as strength, curing profiles, dispensability, etc., no polymers are to be approved for use in a hybrid assembly without the review and approval of the hybrid process engineers.

2.8 Requirements for Solders

Solders which are used in space flight hybrid/MCM modules are to be selected on the basis of alloy, melt temperature, compatibility with mating surfaces, etc.

2.8.1 Solder paste.The following criteria are required as specifications for purchasing and quality control.

a. Manufacturers part number

b. Production lot number including date code of manufacture

c. Alloy composition

d. Percent of solids for mixture; viscosity specification for mixture

e. Flux vehicle specification

2.8.2 Solder Preform.The following criteria are required as specifications for purchasing and quality control.

a. Alloy composition

b. Thickness, specified

c. Dimensions, in thousandths of an inch and the tolerances allowed. Example: 0.102" x 0.050" (60.003")

2.8.3 Solder Wire.The following criteria are required as specifications for purchasing and quality control.

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a. Manufacturers part number

b. Production lot number including date code of manufacture

c. Flux vehicle specification (if flux core wire)

d. Wire diameter including tolerance

e. Alloy composition

2.9 Active Device Requirements

Active devices are circuit components which perform as a semiconductor including transistors, diodes, integrated circuits, etc. The following characteristics must be specified when purchasing these devices for use in flight hybrid/MCMs:

a. Documentation shall include manufacturing lot and wafer number for traceability

b. Performance characteristics over specified operating temperature range must be included

c. Device dimensions must be specified in x,y,z coordinates

d. Dimensions of bond pads must be clearly shown. Size of pads must be specified. Location of pads with regard to a datum location must be provided.

e. All die used for flight hardware must have a protective passivation coating everywhere except bonding pads. Passivation is normally a thin coating of glass, but may be a polymer compound.

f. Die backside metallization must be specified by JPL on the purchase contract. If die are to be attached by soldering, the backside metal scheme must include barrier layers to prevent leaching during solder alloy formation.

g. Die pad metallization must be specified by die vendor, including all layer thicknesses. Recommended limits for bonding temperature maximums should be specified.

h. Any additional lot testing which JPL desires must be clearly indicated on purchase order. This may include temperature cycle tests, radiation exposure, etc.

i. Packaging instructions for delivery to JPL must be specific. Die package size should be indicated on purchase order. ESD protection is mandatory.

2.10 Passive Device Requirements

Passive circuit elements are devices such as resistors, capacitors, and inductors which are not functionally semiconductive.

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2.10.1 Chip Capacitors. The following items should be specified when these devices are purchased:

a. Electrical characteristics such as capacitance value (including tolerances), voltage range, temperature coefficient of capacitance, stability over operational temperature range, and dissipation factors at known frequencies.

b. Device size desired must be clearly stated.

c. End termination metallization must be specified. If plated terminations are required, this must be specifically stated on the purchase order.

d. Packaging and shipping of these devices is typically in bulk packages. If something other than this is required, it must be clearly stated on the purchase order.

2.10.2 Chip Resistors. The following items should be specified when these devices are purchased:

a. Electrical characteristics such as resistance value (including tolerance), temperature coefficient of resistance, stability after long term storage/aging, and power derating must be specified and included with each delivered lot.

b. Material used for substrate member and the resistive ink series used must be specified.

c. Device size, in x,y,z coordinates, must be clearly stated.

d. Bond pad locations (if present, as on a network or thin film resistor) must be specified in relation to a specified datum location.

e. Packaging and shipping of these devices is typically in bulk packages. If something other than this is required, it must be clearly stated on the purchase order.

2.11 Handling Requirements

The requirements for handling bare die, or active devices of any kind are as follows:

a. Active devices of any kind shall always be transported in acceptable ESD containers. These containers will be partitioned die paks or gel paks which are of suitable depth to contain die without any contact being made to the die surface. Compartment sizes will be such that devices cannot rotate or flip over.

b. Bare die or plated surfaces shall not be touched with bare hands. Finger cots or gloves shall be worn at all times.

c. Active devices should be packaged and unpackaged under a laminar flow hood capable of providing a Class 1000 or better work zone.

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d. Hybrid /MCM subassemblies will be transported from assembly station to storage, etc. using ESD containers only.

2.12 Packaging and Shipping Requirements

The requirements for handling bare die, or active devices of any kind are as follows:

a. All materials coming to JPL assembly from an outside source shall be packaged per written instructions from JPL. Materials received which are improperly packaged may be returned with no further explanation.

b. Finished devices assembled at JPL shall also be properly packaged. ESD rated containers will be standard. Devices will be anchored so that they are not freely moving within the container.

c. Finished devices shall be accompanied by original traveler and other pertinent documentation used to build the assembly. Copies of documentation will be retained by Sect. 349 for reference.

d. A range of standard sized ESD containers shall be maintained at Sect. 349 assembly area.

2.13 Design Criteria

Design criteria for hybrids and MCMs shall be defined as the standard set of design guidelines and parts requirements used to develop the finished print sets needed for a completed design set.

a. Parts and components criteria

b. Hybrid design rules and guidelines

2.13.1 Modeling Analyses.Modeling analyses for mechanical stress, thermal stress, and vibration stress. Inputs for these models are not standard. Inputs must be supplied by the customer, circuit designer, or program management. The criteria are specific to each mission.

3 FABRICATION AND ASSEMBLY REQUIREMENTS

3.1 Facilities

3.1.1 Level of Cleanliness Required.Due to the submicron feature geometries encountered when working with bare die, which are commonly utilized in the fabrication of hybrid/MCM assemblies, it is imperative to observe a strict regimen with regard to

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cleanliness. All hybrid/MCM modules built as flight hardware will be assembled in a clean room environment which is compliant to Class 10,000 restrictions (per Fed-Std-209). When possible, all assembly work shall be performed inside laminar flow hoods, in a stream of constantly filtered air, providing a cleanliness level equal to Class 1000 requirements (per Fed-Std-209). Some operations, such as wirebonding, will be permissible outside the laminar flow areas, due to equipment constraints.

3.1.2 ESD Mitigation Measures.The spacing between insulators and conductors on active devices is constantly decreasing. This separation is now commonly 0.35 for most CMOS fabrication, and is rapidly transitioning to 0.18 . (One micron, , is approximately 1/100th the diameter of a human hair.) In addition, gate structures are also changing in architecture to enhance electron/hole mobilities. These changes increase the likelihood of ESD damage. Therefore, ESD vigilance is more important than it has ever been. Specific handling requirements are provided in JPL D-1348, *Electrostatic Discharge (ESD) Control for Assembly and Test Areas for Flight Projects*. General cleanroom procedures are provided in JPL FP513414, Section 1.

3.2 Quality Requirements

3.2.1 Minimum Quality Requirement.The minimum level of quality required for space qualified hybrids/MCMs is equivalent to Class K as described in Mil-PRF-38534.

3.2.2 Inspection Requirements.Inspection requirements are as noted in D-4770, Rev. M, which is overseen and maintained by Section 506.

3.3 Qualified Vendor/supplier Listing

3.3.1 Core Supplier Listing.To select a supplier of space flight hardware, refer to the Core Supplier Listing (CSL), Part II, as compiled by NASA GSFC.

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3.4 Thin-Film Design

3.4.1 Thin-Film Conductors and Pads. Design requirements for thin-film conductors and pads shall be as presented in Figure 3.11-1 and the following paragraphs; deviations must be identified and submitted to Section 349's Hybrid Microelectronic Packaging Engineer for review and approval.

3.4.1.1 Conductor Width. The conductor width shall be designed to a minimum of 0.003 inch, identified as Item 1 in Figure 3.11-1.

3.4.1.2 Conductor-to-Edge Spacing. The minimum distance from conductors to the edge of the substrate shall be 0.010 inch, identified as Item 2 in Figure 3.11-1.

3.4.1.3 Conductor-to-Conductor Spacing. Spacing between conductors shall be designed to a minimum of 0.003 inch, identified as Item 3 in Figure 3.11-1.

3.4.1.4 Conductor-to-Resistor Spacing. Spacing between conductors and resistors shall be designed to a minimum of 0.005 inch, identified as Item 4 in Figure 3.11-1.

3.4.1.5 Trim Tabs Resistors. Spacing between conductors and resistors with laser-trim tabs shall be designed to a minimum of 0.003 inch, identified as Item 5 in Figure 3.11-1.

3.4.1.6 Exit Bond Pad. Exit bond pads shall be designed to a minimum of 0.010 inch on each side, identified as Item 6 in Figure 3.11-1.

3.4.1.7 Single Bond Pad. Wire bond pads receiving a single wire shall be designed to a minimum of 0.010 inch on each side, identified as Item 7 in Figure 3.11-1.

3.4.1.8 Multiple Bond Pad. Wire bond pads receiving two wires shall be designed to a minimum of 0.015 inch, on each side, identified as Item 8 in Figure 3.11-1.

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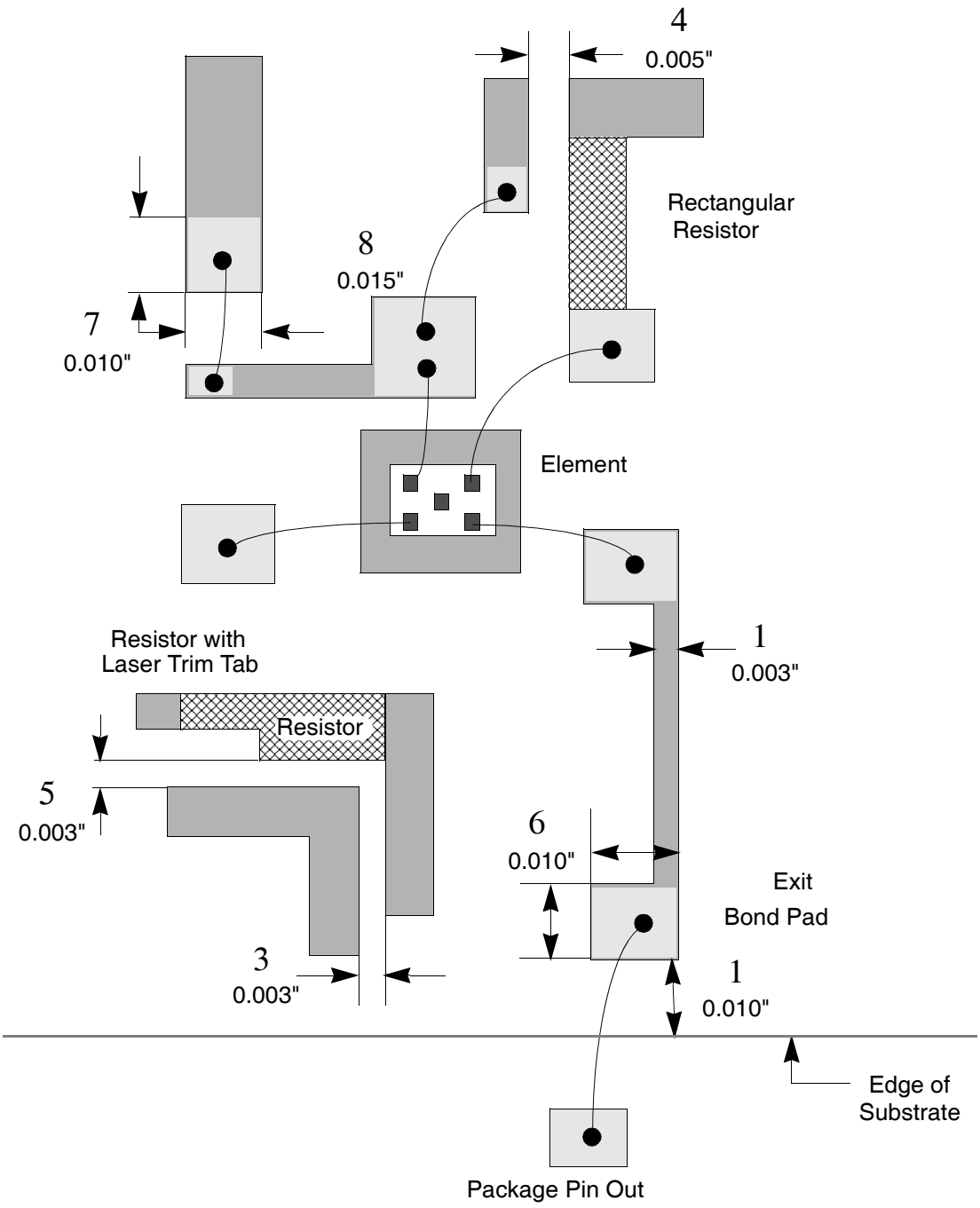

Figure 3.11-1 Thin-Film Conductors and Pads

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3.4.2 Thin-Film Resistors. The thin-film resistor requirements shall be as presented in Figure 3.11-2, Figure 3.11-3, and the following paragraphs.

3.4.2.1 Resistor Spacing. The minimum spacing between resistors shall be 0.0025 inch, identified as Item 1 in Figure 3.11-2.

3.4.2.2 Trimmed Resistor Width. The minimum width for laser-trim resistors shall be 0.0025 inch, identified as Item 2 in Figure 3.11-2.

3.4.2.3 Rectangular Resistor Width. The minimum width for rectangular resistors shall be 0.005 inch, identified as Item3 in Figure 3.11-2.

3.4.2.4 Resistor Length. The minimum resistor length shall be 0.005 inch, identified as Item 4 in Figure 3.11-2.

3.4.2.5 Trim Tab Width. The minimum width for trim tabs shall be 0.0075 inch or 3 times the width (3W) of the resistor, identified as Item 5 in Figure 3.11-2.

3.4.2.6 Tab Length. The minimum length of laser-trim tabs shall be half the total length of the resistor, identified as Item 6 in Figure 3.11-2.

3.4.2.7 Shunt Pad Length. The minimum resistor shunt-pad length shall be 0.005 inch, identified as Item 7 in Figure 3.11-2.

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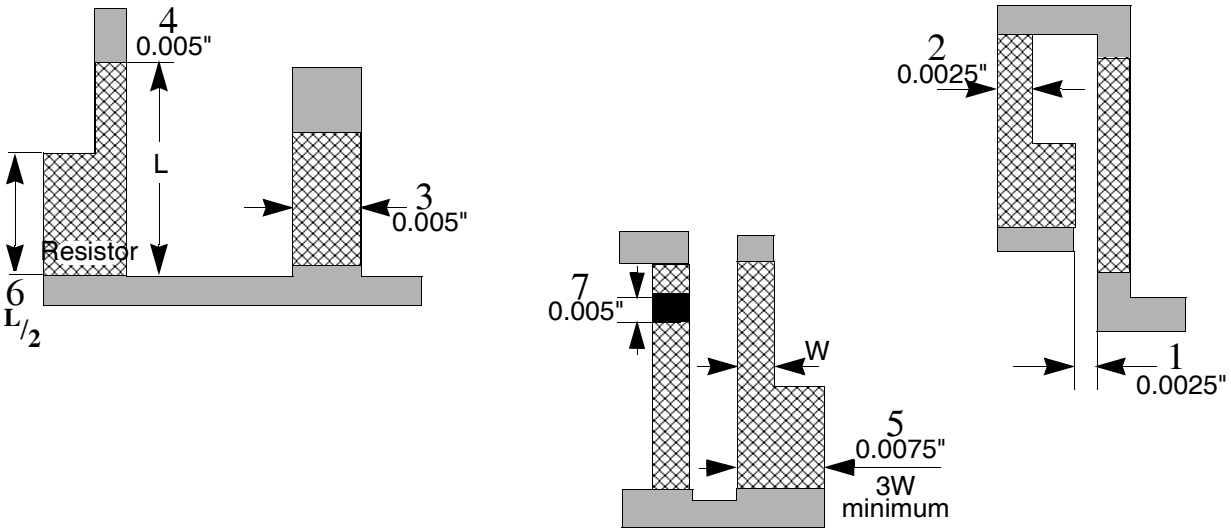

Figure 3.11-2 Thin-Film Resistors

3.4.2.8 Laser-Trim Tab Spacing. The minimum spacing between resistors with laser-trim tabs and conductors shall be 0.0025 inch, identified as Item 1 in Figure 3.11-3.

3.4.2.9 Resistor-to-Conductor Spacing. For resistors with a resistance tolerance less than 20%, the minimum spacing between conductors and the resistor pattern shall be 0.005 inch and apply to only one side of the resistor, identified as Item 2 in Figure 3.11-3.

3.4.2.10 Resistor-to-Edge Spacing. The minimum distance from resistors to the edge of the substrate shall be 0.010 inch, identified as Item 3 in Figure 3.11-3.

3.4.2.11 Resistance Loops. Resistance Loops in substrate design shall be prohibited.

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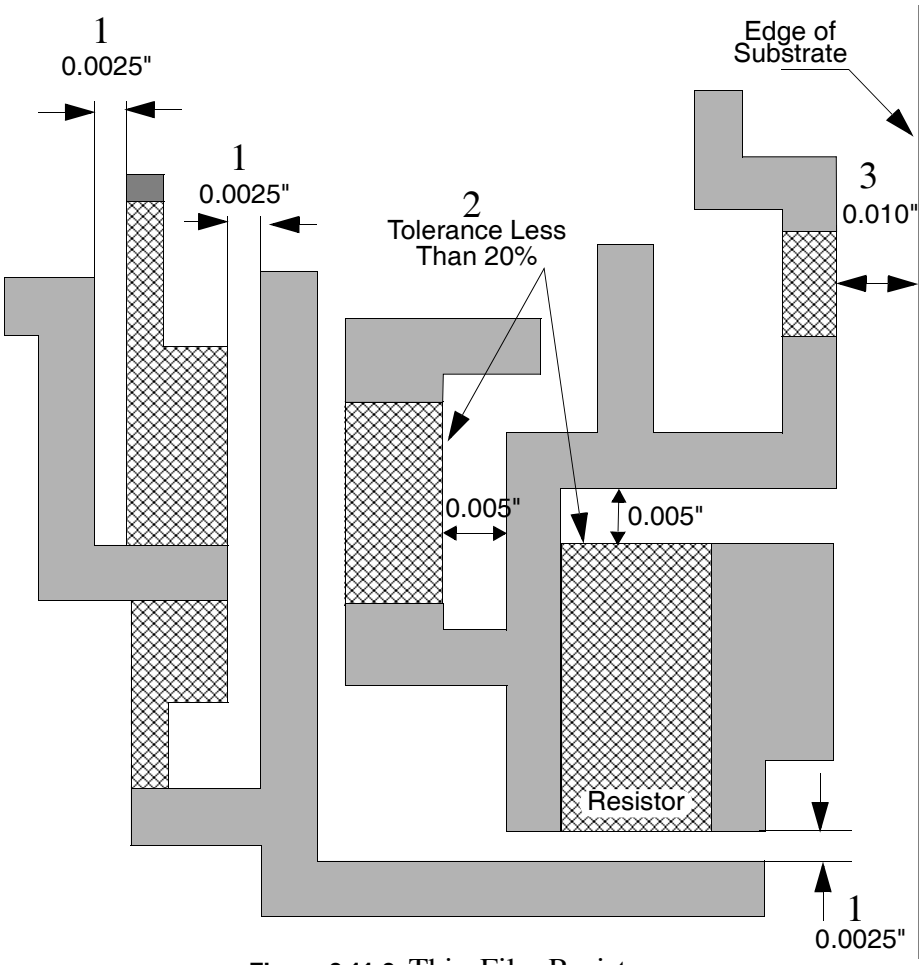

Figure 3.11-3 Thin-Film Resistors

3.5 Thick-Film Design

3.5.1 Thick-Film Conductors and Pads. Requirements for thick-film conductors and pads are presented in Figure 3.11-4 and the following paragraphs and are based on a 0.001 inch wire size.

3.5.1.1 Conductor-to-Edge Spacing. The minimum distance from conductors to the edge of the substrate shall be 0.010 inch, identified as Item 1 in Figure 3.11-4.

3.5.1.2 Single-Bond Pads. Bond pads receiving a single wire shall be a minimum of 0.010 inch on each side, identified as Item 2 in Figure 3.11-4.

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3.5.1.3 Multiple-Bond Pads. Bond pads receiving two 0.001 inch wire bonds shall be designed to a minimum of 0.015 inch on each side, identified as Item 3 in Figure 3.11-4.

3.5.1.4 Exit Bond Pads. Exit bond pads shall be a minimum of 0.010 inch on each side, identified as Item 4 in Figure 3.11-4.

3.5.1.5 Conductor Width. The minimum conductor width shall be 0.010 inch, identified as Item 5 in Figure 3.11-4.

3.5.1.6 Conductor Spacing. The minimum spacing between conductors shall be 0.010 inch, identified as Item 6 in Figure 3.11-4.

3.5.1.7 Conductor-to-Resistor Spacing. The minimum spacing between conductors and the untrimmed side of resistors shall be 0.015 inch, identified as Item 7 in Figure 3.11-4.

3.5.1.8 Laser-Trim Spacing. The minimum allowance between laser-trim resistors and adjacent conductors, resistors, and pads shall be 0.015 inch, identified as Item 8 in Figure 3.11-4.

3.5.1.9 Abrasive-Trim Spacing. The minimum allowance between abrasive-trim resistors and adjacent conductors, resistors, and pads shall be 0.030 inch, identified as Item ¥ in Figure 3.11-4.

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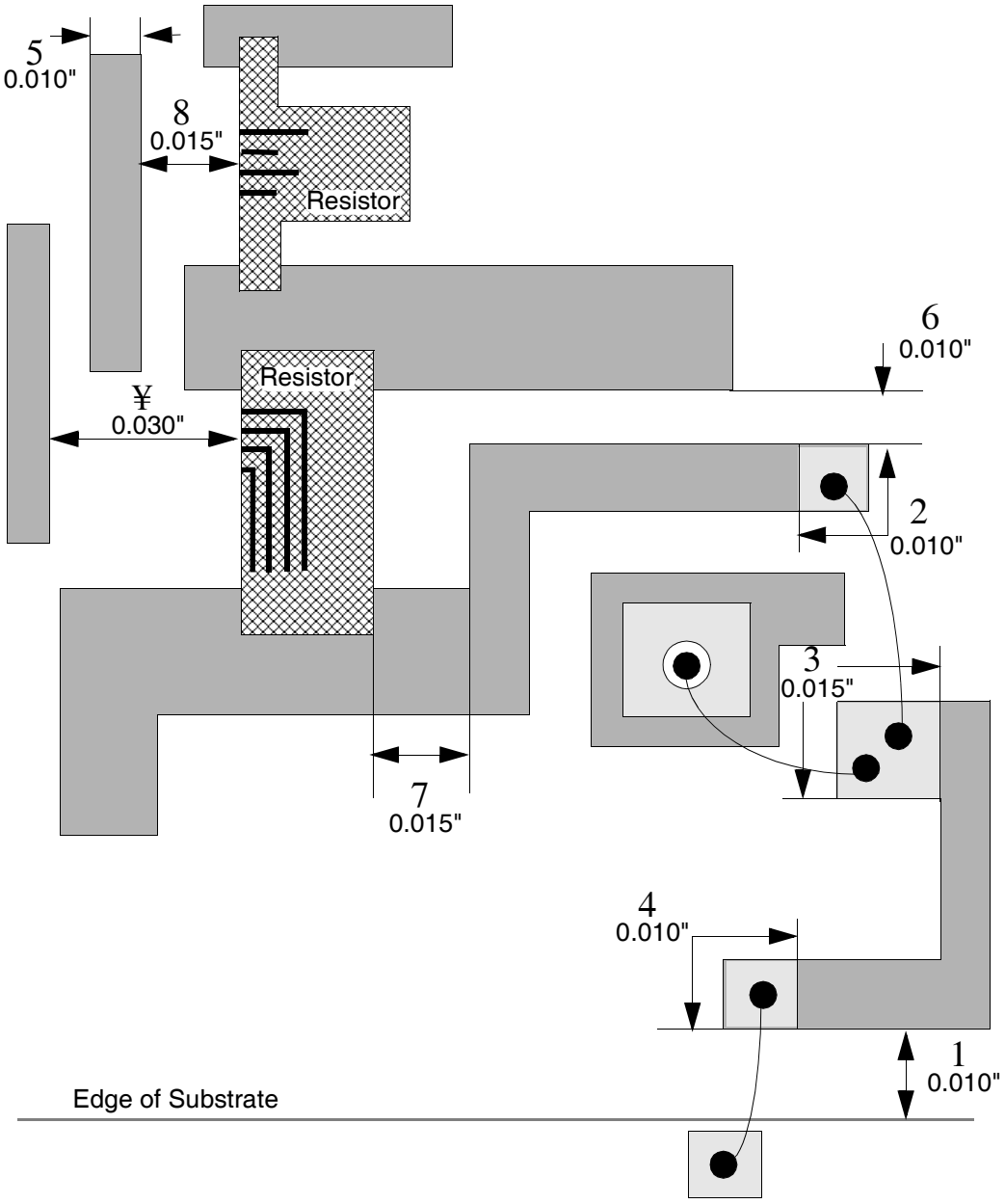

Figure 3.11-4 Thick-Film Conductors and Pads

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3.5.2 Thick-Film Resistors. The thick-film resistor requirements shall be as presented in Figure 3.11-5, Figure 3.11-6, and the following paragraphs.

3.5.2.1 Maximum Resistor Ratio. The maximum length-to-width ratio for resistors is calculated as follows: N = Aspect ratio = L/W shall be greater than 0.2 and less than 6.5 for rectangular designs of resistors whose resistance tolerance is less than 20 percent. N = 30 maximum for top-hat resistor designs after trimming.

3.5.2.2 Resistor Size. Resistors with ink value greater than 100K ohms/square shall be a minimum of 0.040 inch on each side, as depicted in Figure 3.11-5.

3.5.2.3 Resistor Size. Resistors with ink value of less than 100K ohms/square shall be a minimum of 0.030 inch on each side, as depicted in Figure 3.11-5.

3.5.2.4 Resistor Spacing. The minimum spacing between resistors shall be 0.015 inch, identified as Item 1 in Figure 3.11-5.

3.5.2.5 Resistor-to-Conductor Overlap. The resistor-to-conductor overlap shall be a minimum of 0.010 inch, identified as Item 2 in Figure 3.11-5.

3.5.2.6 Conductor Pad Length. The minimum distance from the resistor to the edge of the conductor shall be 0.005 inch, identified as Items 3 in Figure 3.11-5.

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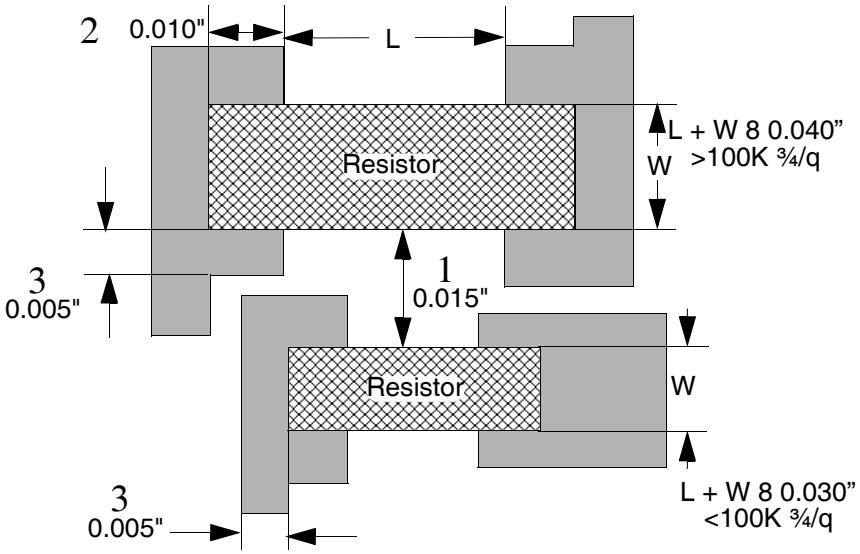

Figure 3.11-5 Thick-Film Resistors

3.5.2.7 Laser-Trim Allowance. The minimum allowance between laser-trim resistors and adjacent conductors, resistors, and pads shall be 0.015 inch, identified as Item 1 in Figure 3.11-6.

3.5.2.8 Abrasive-Trim Allowance. The minimum allowance between abrasive-trim resistors and adjacent conductors, resistors, and pads shall be 0.030 inch, identified as Item 2 in Figure 3.11-6.

3.5.2.9 Resistor Overglaze. Resistors made from inks with a sheet resistivity of less than 32 ohms per square shall require overglaze, identified as Item 3 in Figure 3.11-6.

3.5.2.10 Overglaze Overlap. The overglaze shall extend past the resistor by a minimum of 0.005 inch, identified as Item 4 in Figure 3.11-6.

3.5.2.11 Resistance Loops. Resistance loops in substrate design shall be prohibited.

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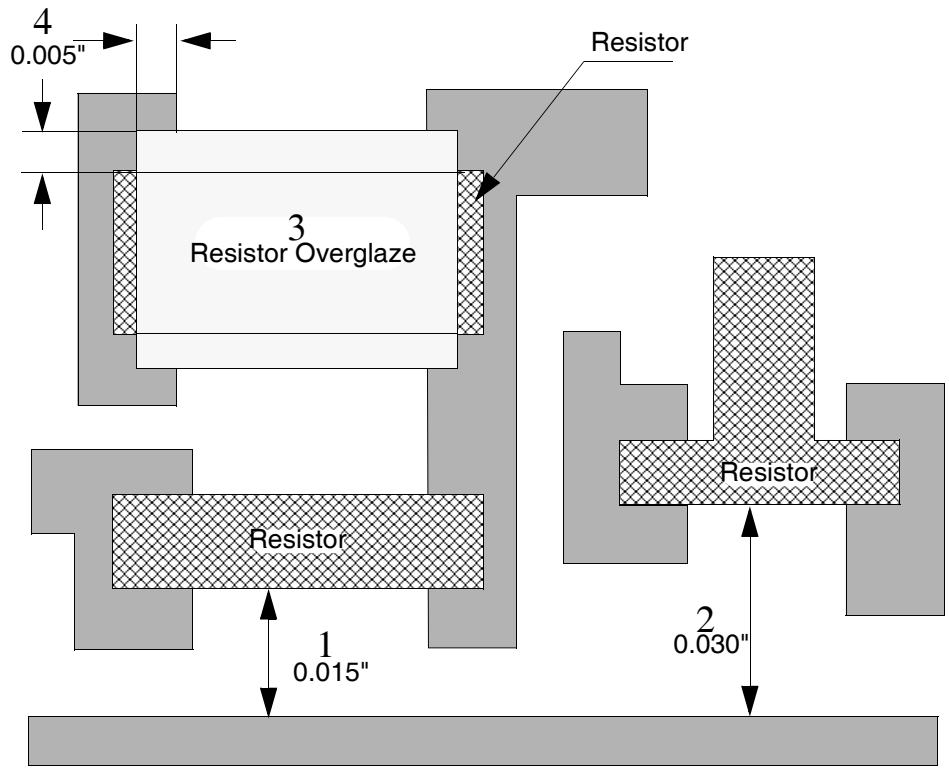

Figure 3.11-6 Thick-Film Resistors

3.5.3 Multilayer Thick-Film Conductors. The multilayer thick-film conductor requirements shall be as presented in Figure 3.11-7 and the following paragraphs.

3.5.3.1 Crossover Conductor Width. The minimum width of upper and lower conductors at a crossover shall be 0.010 inch, identified as Item 1 in Figure 3.11-7.

3.5.3.2 Conductor-to-Conductor Overlap. The minimum overlap for connecting conductors shall be 0.010 inch, identified as Item 2 in Figure 3.11-7.

3.5.3.3 Lower-to-Upper Conductor. The lower conductor of connecting conductors shall be a minimum of 0.005 inch wider than the upper conductor, identified as Item 3 in Figure 3.11-7.

3.5.3.4 Conductor Thickness. The minimum conductor thickness shall be 0.0005 inch, identified as Item 4 in Figure 3.11-7.

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3.5.3.5 Parallel Conductors. There shall be no parallel conductors running directly beneath each other.

3.5.3.6 Edge Conductors. There shall be no conductors running over the edge of multiple dielectric layers.

3.5.3.7 Maximum Layers. Thick-film multilayer conductors shall be constructed of seven (7) layers or less.

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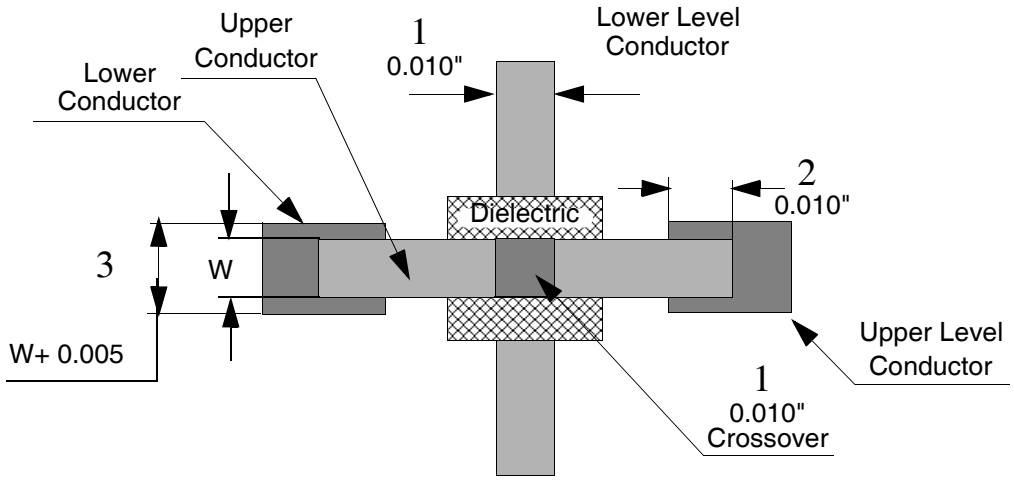

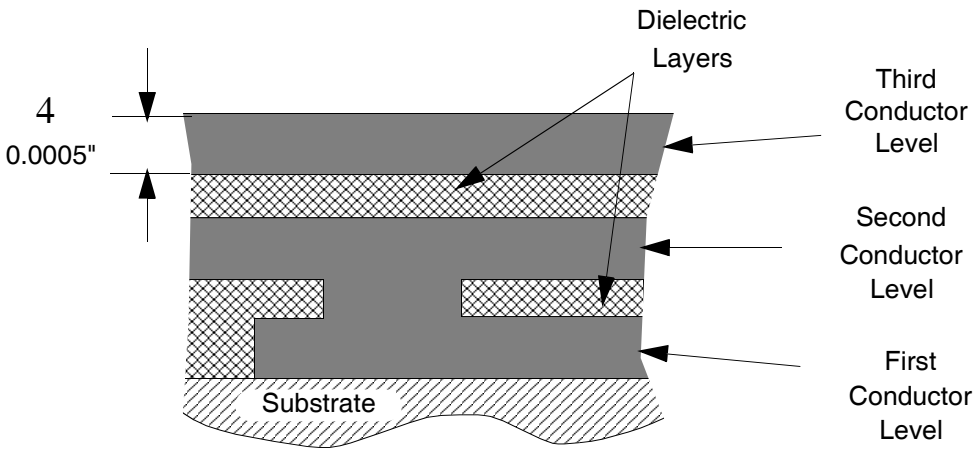

Figure 3.11-7 Multilayer Thick-Film Conductors

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3.5.4 Multilayer Dielectric Requirements. The multilayer thick-film dielectric requirements shall be as presented in Figure 3.11-8 and the following paragraphs.

3.5.4.1 Dielectric Crossover. The minimum distance from conductor to dielectric crossover shall be 0.010 inch, identified as Item 1 in Figure 3.11-8.

3.5.4.2 Dielectric-to-Resistor Spacing. The minimum dielectric-to-resistor spacing shall be 0.015 inch, identified as Item 2 in Figure 3.11-8.

3.5.4.3 Dielectric Thickness. The dielectric thickness shall be a minimum of 0.001 inch between conductor layers, identified as Item3 in Figure 3.11-8.

3.5.4.4 Dielectric Coating. There shall be a minimum of 3 layers of dielectric coating — utilizing a different screen for each layer—between conductor layers.

3.5.4.5 Dielectric Strength. The dielectric strength of fired film shall be 200 volts minimum for a 0.001 inch thickness.

3.5.4.6 Dielectric Film Usage. Dielectric films shall be capable of withstanding a minimum of 50 Vdc or twice the maximum operating voltage at maximum rated temperature, whichever is greater.

3.5.4.7 Dielectric Constant. The dielectric constant shall be 6 to 12 with an insulation resistance 1 x 10^{11} ohms minimum.

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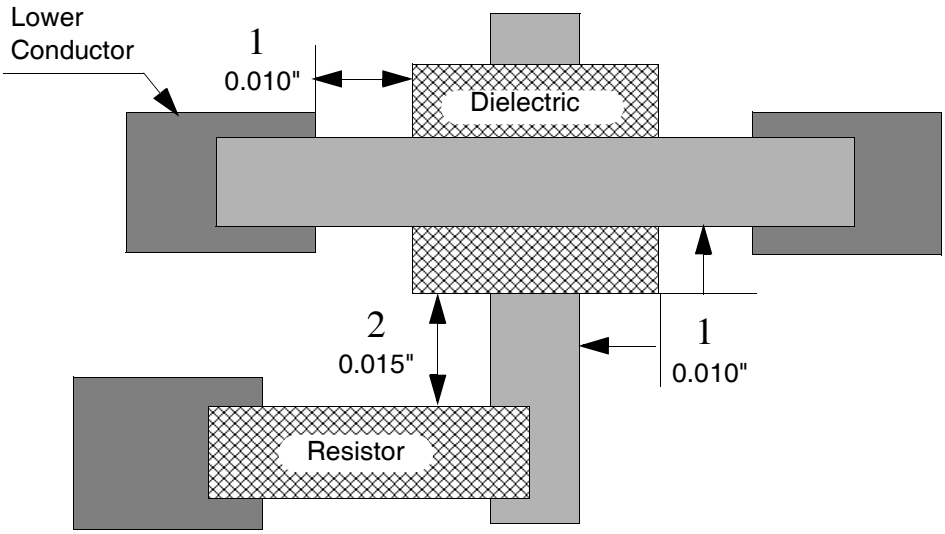

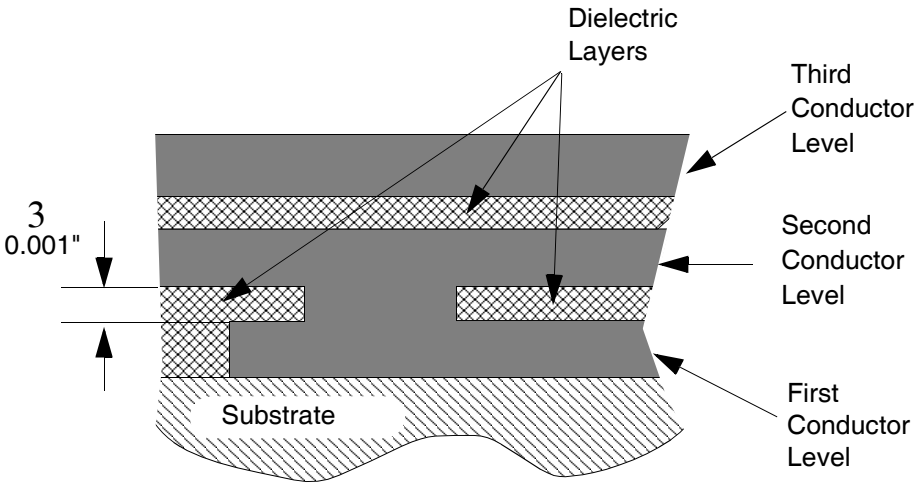

Figure 3.11-8 Multilayer Dielectric

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3.5.5 Vias. Multilayer thick-film via requirements shall be as presented in Figure 3.11-9 and the following paragraphs.

3.5.5.1 Via Design. Vias shall be square with a minimum dimension of 0.010 inch on each side, identified as Item 1 in Figure 3.11-9.

3.5.5.2 Via-to-Conductor Size. The via shall be equal to or less than conductor width, identified as Item 1 in Figure 3.11-9.

3.5.5.3 Parallel Conductor Vias. Interlevel vias on parallel conductors shall be staggered by a minimum distance of 0.010 inch, identified as Item 2 in Figure 3.11-9.

3.5.5.4 Interlevel Vias. Interlevel vias shall be made to adjacent levels of metallization, identified as Item 3 in Figure 3.11-9.

3.5.5.5 Interlevel Staggered Vias. Vias making a connection through more than one dielectric level shall be staggered vertically from level to level with a minimum distance of 0.010 inch, identified as Item 4 in Figure 3.11-9.

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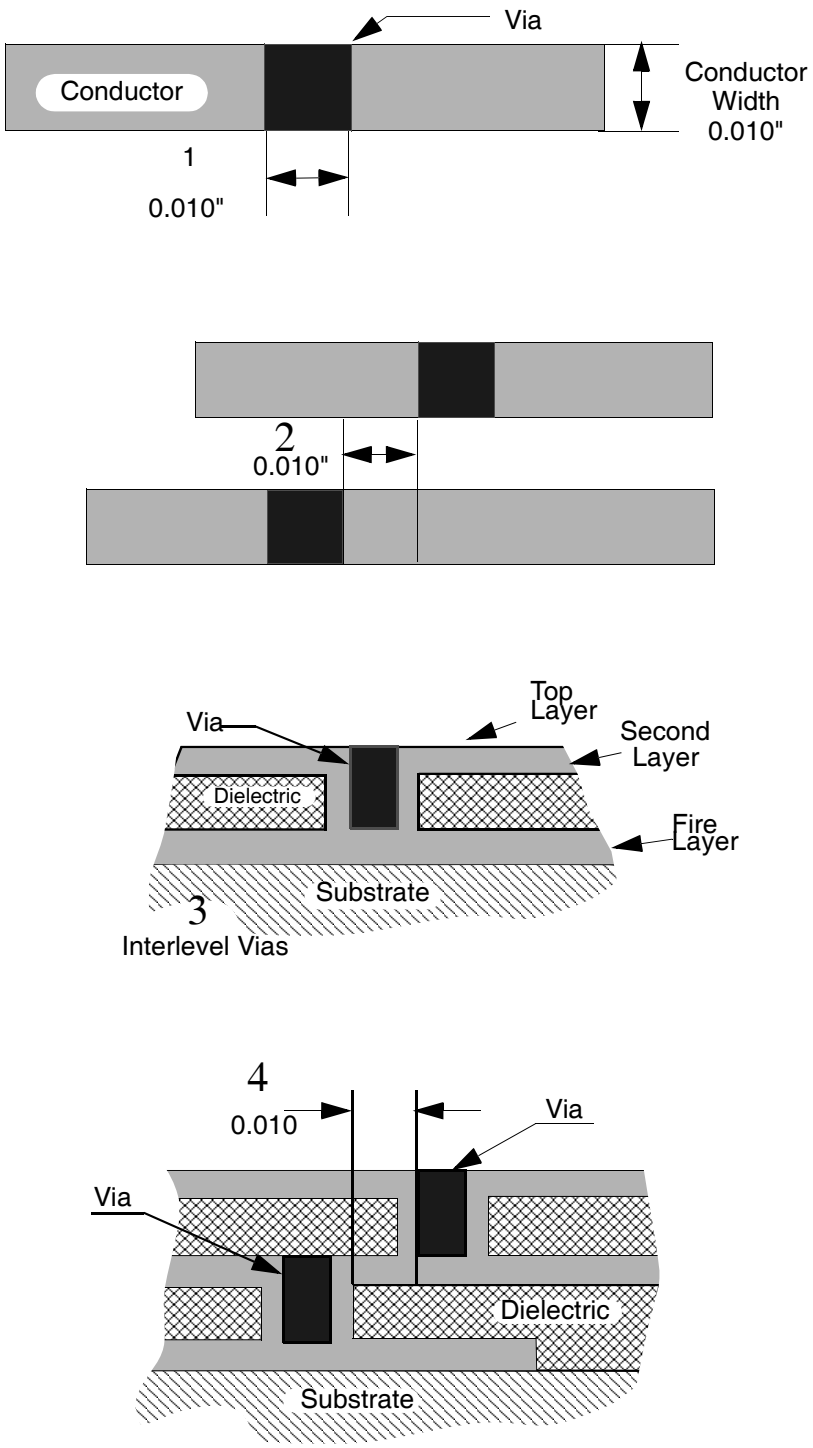

Figure 3.11-9 Dimensional Constraints for Vias

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3.5.6 Thick-Film Multilayer Resistors. The dimensional constraints for thick-film, multilayer resistors shall be as presented in Figure 3.11-10, Figure 3.11-11, and the following paragraphs.

3.5.6.1 Maximum Resistor Ratio. The maximum length -to-width ratio for resistors shall be calculated as follows: N = Aspect ratio = L /W greater than 0.2 and less than 6.5 for rectangular designs of resistors whose resistance tolerance is less than 20 percent. N = 30 maximum for top-hat resistor designs after trimming.

3.5.6.2 Resistor Spacing. The minimum spacing between resistors shall be 0.015 inch, identified as Item 1 in Figure 3.11-10.

3.5.6.3 Resistor/Conductor Overlap. The minimum resistor/conductor overlap length shall be 0.010 inch, identified as Item 2 in Figure 3.11-10.

3.5.6.4 Conductor Pad Length. The minimum distance from the resistor to the edge of the conductor shall be 0.005 inch, identified as Items 3 in Figure 3.11-10.

3.5.6.5 Resistor Size. Resistors with ink value of less than 100 K ohms/square shall be a minimum of 0.040 inch on each side, as depicted in Figure 3.11-10.

3.5.6.6 Resistor Size. Resistors with ink value greater than 100K ohms/square shall be a minimum of 0.030 inch on each side, as depicted in Figure 3.11-10.

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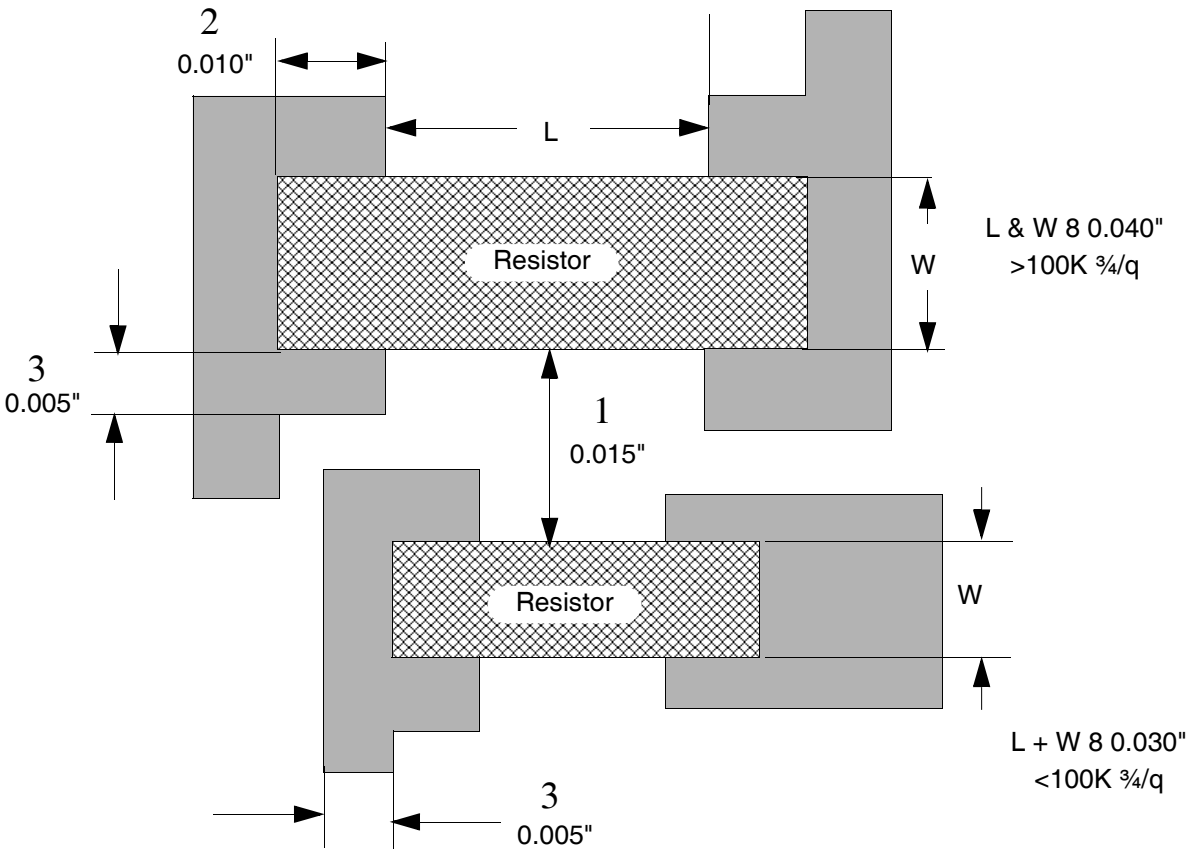

Figure 3.11-10 Thick-Film Multilayer Resistors

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3.5.6.7 Laser-Trim Allowance. The minimum laser-trim allowance between resistors and adjacent conductor, resistor, or pad shall be 0.015 inch, identified as Item 1 in Figure 3.11-11.

3.5.6.8 Abrasive-Trim Allowance. The minimum abrasive-trim allowance shall be 0.030 inch, identified as Item 2 in Figure 3.11-11.

3.5.6.9 Resistor Overglaze. Resistors made from inks with a sheet resistivity of less than 32 ohms per square shall require overglaze, identified as Item 3 in Figure 3.11-11.

3.5.6.10 Overglaze Overlap. The overglaze shall extend past the resistor by a minimum of 0.005 inch, identified as Item 4 in Figure 3.11-11.

3.5.6.11 Multilayer Test. Multilayer substrate test points for continuity and shorts checking between conductor levels shall be provided within the layout.

3.5.6.12 Resistor Placement. Resistors shall only be printed on the top layers.

3.5.6.13 Resistor Level. Resistors which require trimming shall not be located over conductors of the next two underlying levels.

3.5.6.14 Resistance Loop Exclusion. Resistance loops in the substrate design shall not be permitted.

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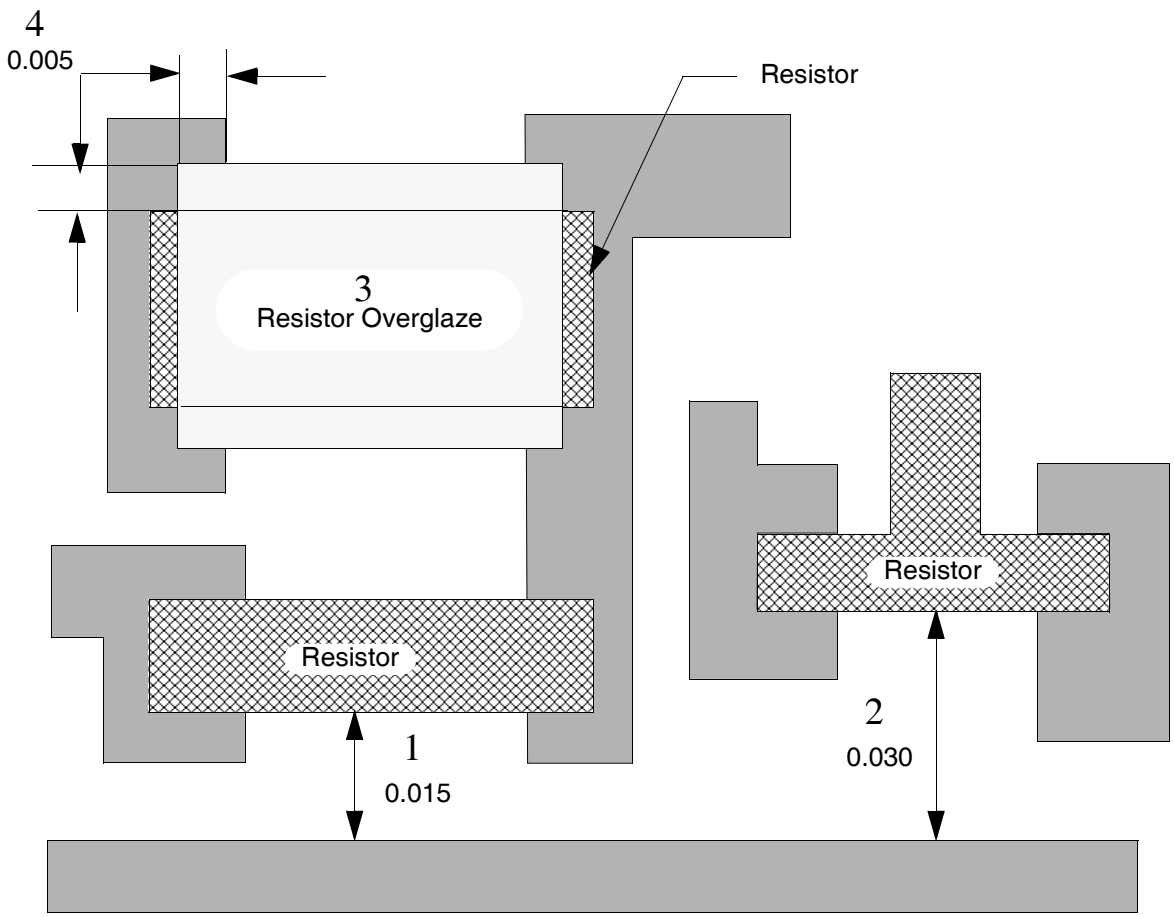

Figure 3.11-11 Thick-Film Multilayer Resistors

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3.5.7 Component Mounting Pads. The pad size and spacing requirements shall be as presented in Figure 3.11-12, Figure 3.11-13, and the following paragraphs.

3.5.7.1 Semiconductor Chip Spacing. The minimum spacing between semiconductor chips shall be 0.032 inch, identified as Item 1 in Figure 3.11-12.

3.5.7.2 Mounting Pad Size. The mounting pad beyond the semiconductor chip shall be a minimum of 0.010 inch on each side, identified as Item 2 in Figure 3.11-12.

3.5.7.3 Bond Distance. The bond distance (site) from the edge of the passive chip to the pad shall be a minimum of 0.030 inch, identified as Item 3 in Figure 3.11-12; the minimum for semiconductor chips is 0.020 inch.

3.5.7.4 Pad Width. The mounting pad shall extend beyond the sides of the passive chip by a minimum of 0.005 inch, identified as Item 4 in Figure 3.11-12.

3.5.7.5 Pad Length. The mounting pad shall extend beyond the ends of the passive chip by a minimum of 0.010 inch, identified as Item 5 in Figure 3.11-12.

3.5.7.6 Chip/Conductor Overlap. The passive chip/conductor overlap shall be a minimum of 0.010 inch, identified as Item 6 in Figure 3.11-12.

3.5.7.7 Chip-to-Bond Pad Spacing. The passive chip-to-wire bond spacing shall be a minimum of 0.040 inch, identified as Item 7 in Figure 3.11-12.

3.5.7.8 Passive Chip Spacing. The passive chip end-to-end spacing shall be a minimum of 0.030 inch, identified as Item 8 in Figure 3.11-12.

3.5.7.9 Inductor Pad Size. Inductor lead mounting pads shall be a minimum of 0.040 inch on each side, identified as Items 1 in Figure 3.11-13.

3.5.7.10 Inductor-to-Bond Pad Distance. The inductor body-to-lead bonding pad shall be a minimum of 0.005 inch, identified as Item 2 in Figure 3.11-13.

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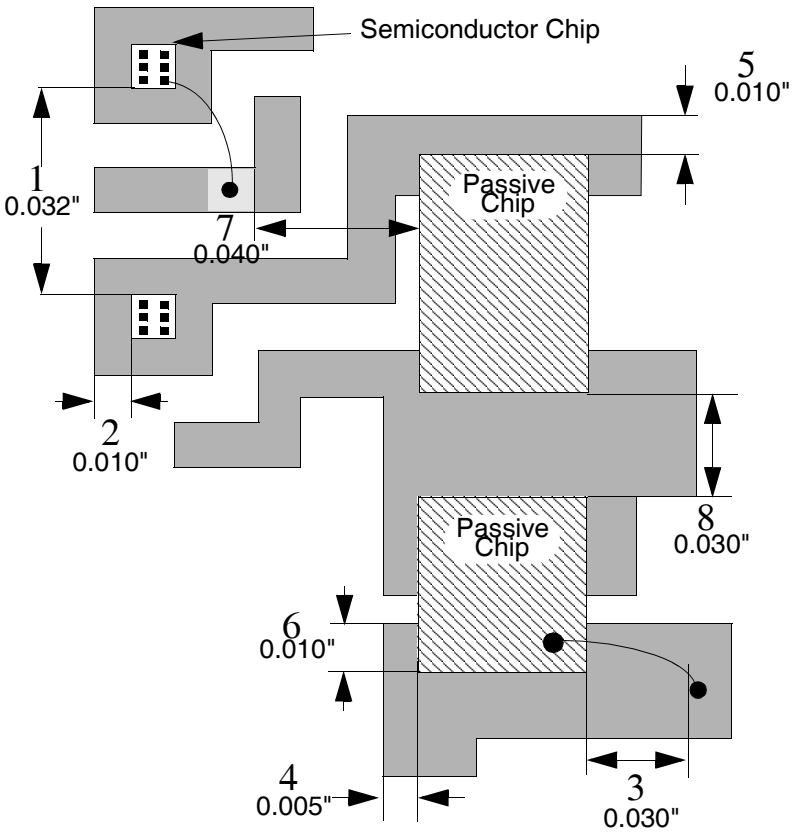

Figure 3.11-12 Mounting Pads

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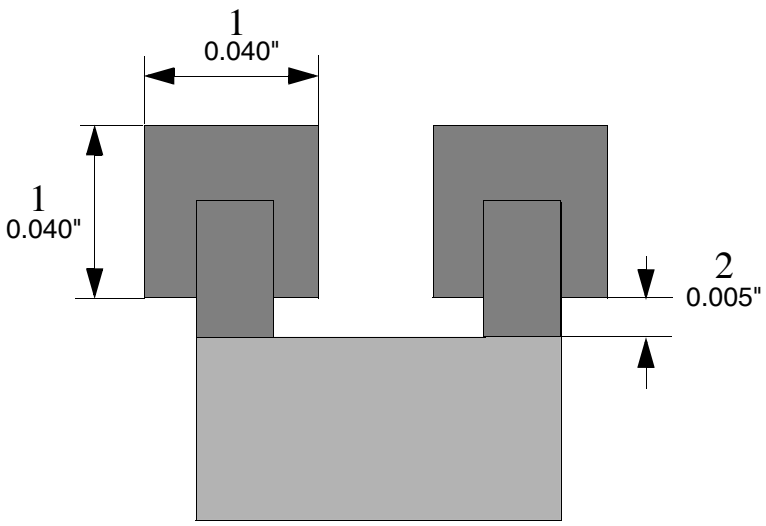

Figure 3.11-13 Component Mounting Pads

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Cabling and Wiring

1 DESIGN REQUIREMENTS

The requirements of this section apply to all electrical interconnections using electrical hookup of wire between components, subassemblies, subsystems, and remotely located elements of subsystems. Wiring and cabling that is designed to the requirements of this document will operate under conditions of vacuum, vibration, radiation, humidity, and temperature extremes. This document does not make provisions for severe environments of moisture, contamination, extensive handling, or usage that involves abrasion or tensile loading of wire bundles.

1.1 Documentation

1.1.1 Deliverable Package. The documentation used in cable fabrication—including drawings, reference designations, identification, and configuration control measures—shall meet the requirements of the applicable project documents and the current JPL drafting manual.

1.1.2 Harness Assembly Drawing. The harness assembly drawings shall provide sufficient detail to enable complete fabrication and assembly of all interconnections, and contain as a minimum the following:

a. Wire connection details for both ends

b. All connector reference designations and part or identification numbers

c. Connector contact or termination identification

d. Wire size and construction

e. Shield termination method and length of lead

f. Splice identification and detail

g. Mating connector reference designators and part or identification numbers

h. Complete circuit function names

i. Accessory parts, connector boots, lugs

j. Required bulk materials—such as lacing tape, sleeving and jacketing, splice caps, wire, solder, and potting materials

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k. Mechanical fasteners, clamps, connector brackets, rails or harness supports

l. Associated fixtures and tooling

m. Bundle category (i.e., quiet, noisy, power, etc.)

n. Circuit function nomenclature and electrical information

o. Mechanical geometry only if a simple, dimensioned, stick diagram will suffice

p. Mechanical details of a complex harness shall be established by referencing the wiring fixture drawing

q. Fully defined splice information

1.1.3 Wiring Fixture Drawing. The wiring fixture drawing shall be designed and documented separately from other drawings.

1.1.4 Master Cabling Interconnect Block Diagram. All cabling shall be shown on a master cabling interconnect diagram showing the following:

a. Each cable in relation to other cables and associated electronic assemblies, subassemblies, and connectors.

b. Connector part numbers, reference designators, and other identification (ID) required by project control documents.

1.1.5 Reference Designators. Reference designators shall be assigned to all cables, harnesses, and connectors as required by project documents for equipment identification and marking for use as follows:

a. Identification of cables and connectors in documentation

b. Identification in interconnected equipment in documentation

c. Identification of cables and connectors on hardware, by application or reference designator.

1.2 General Requirements

1.2.1 Material Selection. Parts and materials shall be selected from JPL STD00009, Flight Materials, Processes, Fasteners, Packaging and Cabling Hardware Selection Guide.

1.2.2 Reliability. Redundant conductor requirements and other specific reliability measures shall conform to applicable project documentation.

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1.2.3 Environmental Requirements. The cabling and wiring shall be designed to withstand the environment defined by the applicable project document and the rigors of physical handling during 1) Installation; 2) Removal; 3) Interim storage and rework of cabling; and 4) Installation, test, and rework on adjacent components, subassemblies, and structures.

1.2.3.1 Storage Temperature. All cables and assemblies shall be able to withstand storage temperature ranges of -55°C to +125°C (-67°F to 257°F).

1.2.3.2 Thermal Requirements. Requirements for special thermal cycling circumstances are as follows:

a. Thermal Cycling. Thermal cycling effects caused by alternate sun and shade exposure, especially for harnesses which must flex during usage, shall be considered during the design of cable harnesses.

b. Power Cycling. Wiring design shall also consider the effects caused by power modes of the system/subsystem and localized power cycling.

c. Heat Protection. Proper heat protection and dissipation shall be provided for all wiring.

1.2.4 Cleaning. All cables and harness assemblies, including connector mating faces, insulation, fastening devices and associated brackets and hardware forming the assembly, shall be designed to allow cleaning after fabrication

1.2.5 Current Carrying Capacity. The maximum amount of current a given wire may be allowed to carry is a function of the wire material (maximum allowable temperature), ambient conditions (temperature and vacuum), and installed configuration (bundle size and heat rejection capability.

1.2.5.1 Maximum Current. The maximum amount of current in a given wire shall be in accordance with Table 3.12-1, Figure 3.12-1, and Figure 3.12-2.

1.2.6 Operating Temperature. Except for special purpose cables, all cables shall be able to withstand an operating temperature range of -55°C to +105°C (67°F to 225°F) with 1 ampere current flowing per wire per Figure 3.12-1.

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Table 3.12-1 Current Carrying Ratings

This tables gives the maximum allowable current in three different situations for silver-plated conductors with TFE Teflon insulation. The table assumes an ambient temperature of 80°C with an allowable rise of 120°C to the 200°C rating of silver-plated conductors. Column 3 gives maximum permissible currents for single wires in a vacuum. Columns 4 and 5 were obtained by multiplying the column 3 values by derating factors from Figure 3.12-1.

Wire Type	Wire Size	Maximum Allowable Current Rating Amperes in a Vacuum			
		Single Wire		Wire Bundle	
		Air		>5 Wire	>33 Wire
Silver Coated Copper	12	66	23.0	17.7	12.0
	14	50	17.5	13.5	9.1
	16	36	13.0	10.0	6.8
	18	32	11.2	8.6	5.8
	20	23	8.0	6.2	4.2
	22	16	5.6	4.3	2.9
Silver Coated Alloy*	*24	10	3.5	2.4	1.6
	*26	7.7	2.7	2.1	1.4
	*28	5.9	2.0	1.6	1.0

*** Copper alloy conductivity +0.84 x copper conductivity.**

For bundle configurations other than those in the Table 3.12-1, select the appropriate bundle derating factor and apply it to the value from column 2. For other wire types or allowable temperature ranges, refer to MIL-W-5088.

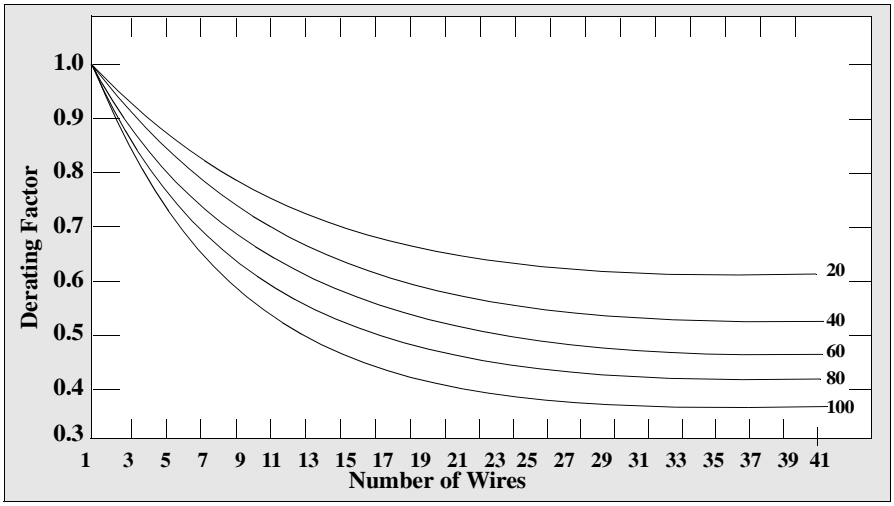

Figure 3.12-1 Bundle Derating Curves

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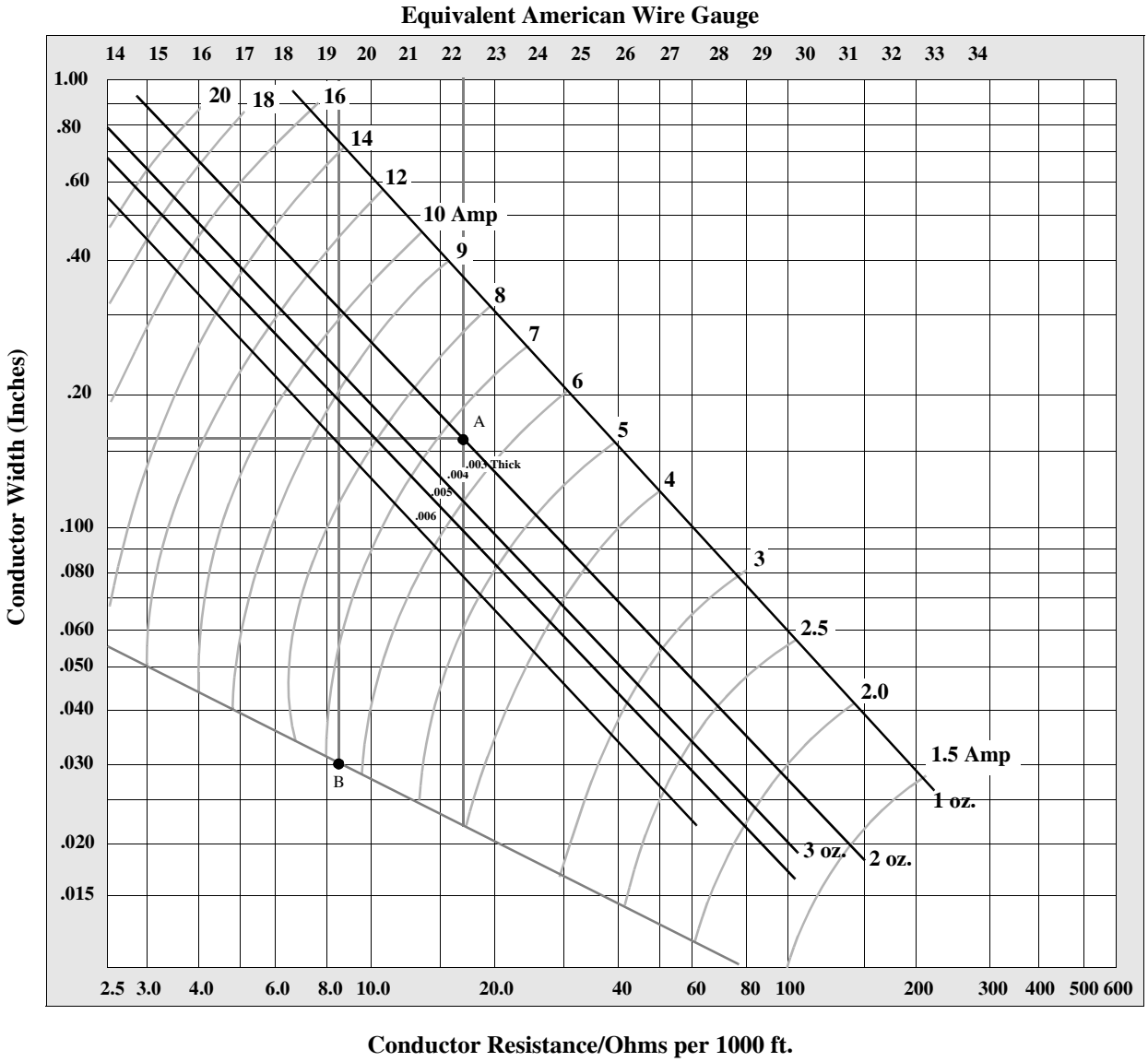

The maximum amount of current a given wire shall be allowed to carry is a function of the wire material (maximum allowable temperature), ambient conditions (temperature and vacuum), and installed configuration (bundle size and heat rejection capability).

Figure 3.12-2 Current Carrying Capacity Design Nomogram

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1.3 Electrical Design

1.3.1 Circuit Definition. Circuits included in the cabling subsystem design shall meet the requirements of the electronic equipment as stated in project functional requirements documents and interface lists which define all system level interfaces.

1.3.1.1 Intraconnects. Subsystem intraconnect requirements shall be taken from the subsystem circuit diagrams and input/output diagrams.

1.3.1.2 Specified Circuits. Only those circuits identified in applicable project documents as being required for functional operation, direct access for system test, and umbilical cables shall be incorporated in the design.

1.3.2 Conductor Size. Conductor size shall provide adequate strength and current capability for the intended application without causing excessive power loss, voltage drop, or overheating (Table 3.12-1).

1.3.2.1 Subsystem Cabling. The minimum size wire used in subsystem cabling shall be AWG 28.

1.3.2.2 System Cabling. The minimum size wire used in system cabling shall be AWG 26.

1.3.2.3 Alternate Wire Types. Other wire types or allowable temperature ranges shall be in accordance with the applicable Interface Control Document (ICD).

1.3.3 Circuit Requirements. Current carrying capacity shall meet the requirements of the circuit.

1.3.4 Contamination Control. Flight-rated parts and materials shall be used to minimize contamination from outgassing of materials.

1.3.5 Insulation. All electrical conductors, except the mating portions of connector contacts, shall be completely insulated to provide an environmental seal and prevent shorting by dust, debris, or other contaminants. Refer to the following as examples:

a. Hard-mounted, rectangular receptacles not requiring handling after installation shall be strain relieved with shrinkable tubing and sealed with CV 2510.

b. Rectangular plugs installed with loose cable with mating handling required shall be strain relieved with nylon potting boot, sealed with CV 2510, and potted with PR 1590.

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c. Circular Connectors:

(1) Subassembly mounted circular connectors not requiring handling shall be strain relieved with shrinkable sleeving and sealed with CV 2510.

(2) Hard-mounted circular connectors requiring minimum handling shall be potted with CV 2510 in a nylon potting boot.

(3) Circular connectors installed with loose cable with only mating handling required shall be potted with PR 1590 polyurethane in a nylon potting boot.

1.3.6 Interference Control. Within reliable system operation requirements, electrical cross-coupling of cabling circuits shall be controlled by categorizing circuit functions into groups defined by type and level of signal and power and then providing isolation of incompatible groups using physical separation, twisting, variations in lay length of twisted conductors, and shielding.

1.3.6.1 Cable Separation. Low-level (quiet, sensitive, “clean”) and high-level (noise producing, “dirty”) circuits shall be routing in separate bundles and terminated in separate connectors, whenever possible.

1.3.6.2 Circuit Separation. When separate connectors cannot be used to segregate high- and low-level circuits, maximum possible circuit separation at the receptacle shall be attained through connector pin assignments meeting the following requirements:

a. Group similar functions together in the connector, physically separated from incompatible functions or isolated by assignment of ground lines, return wires, or unused contacts to the area between.

b. Assign twisted multiples wires to adjacent contacts.

c. Leave spare or unused contacts reserved for future assignment in an accessible insert location in outside rows of contacts near the connector keyway (on circular connectors).

d. Project documentation shall define control and identification methods for specific circuits or compatible groups.

1.3.7 High-voltage Cables. Cables utilizing instantaneous voltage differentials in excess of 250V peak between two or more conductors shall meet the requirements of JPL D-8208, Section 3.9.

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1.3.8 Pyrotechnic Firing Lines. The wiring of circuits for the actuation of electroexplosive devices (EEDs) shall:

a. Must not share connectors with any other circuits.

b. Be isolated and routed in separate bundles without splices.

c. Be individually shielded with 360° coverage and the shield must continue through the connector shell using pyro backshells.

d. Have cabling within the limits required for operation of the firing unit.

e. Have multishield ferrules located within the metal backshell.

1.3.9 Power Cables. Cables for the distribution of AC power to subsystems shall not be routed through wire bundles containing sensitive circuits and shall not share connectors.

1.3.9.1 Bundle Separation and Shielding. The specific bundle separation and shielding shall meet the project functional requirements.

1.3.9.2 Power Loss. Line resistance and power loss in all power cabling shall be within the limits defined for proper operation of the power source and regulation and distribution equipment.

1.3.10 Grounding. The cabling and wiring design shall meet the requirements for grounding and shielding as stated in applicable project documents.

1.3.10.1 Grounding Path. The grounding path provided in the cabling shall be secondary to that provided by the equipment mounting surfaces and is included for the safety of equipment and personnel.

1.4 General Mechanical Design

1.4.1 Functional Elements. The design shall separate cabling harnesses into individual subsystems, each forming logical, functional elements capable of being fabricated, tested, delivered, and installed individually.

1.4.1.1 Cable Separation. Connector interfaces shall be provided for elements (subassemblies) or groups of elements (subsystems) that require a large number of connections, frequent removal for test, extensive testing to verify proper connection, or last minute installation into the system. At a minimum, separate cables shall be provided for the following situations:

a. Circuit isolation for EED firing lines.

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b. Minimum interference with sensitive AC power distribution cables.

c. Removal and independent test of each functional subsystem.

d. The last minute installation of externally mounted subsystems.

1.4.1.2 Interface Design. Connector interfaces shall be provided for subassemblies or groups of subsystems that require a large number of connections, frequent removal for test, extensive testing to verify proper connection, or last minute installation.

1.4.2 Connector Interfaces. Connector interfaces shall be designed per the following requirements.

1.4.2.1 Fixture Usage. Connector interface type, size, key and physical location shall allow cabling by use of an interface/fixture.

1.4.2.2 Dissimilar Connectors. Connectors shall be of sufficiently dissimilar type, size, keying and physical location to prevent incorrect coupling to other nearby connectors.

1.4.2.3 Incorrect Mating. Where identical (D series) connectors are used, the harness shall be configured, or accessory mechanical devices employed, to prevent incorrect mating.

1.4.2.4 Contact Gender. Contact gender of all connectors shall be selected so that no power will be present on protruding pin contacts when the connector is unmated (power flow is from socket to pin side of the connector).

1.4.2.5 Direct Access/Separation Connectors. Test receptacles on electronic subassemblies, direct access connectors, and in-flight separation receptacles (spacecraft side) shall employ socket contacts (not pins) which shall be recessed into the connector insert.

1.4.2.6 Conductive Mounting. All connector shells shall be conductively mounted to the associated subassembly chassis or bracket unless the subsystem requirements and drawing specifies otherwise.

1.4.2.7 Rear Mounting. Hard-mounted receptacles shall be rear-mounted wherever possible.

1.4.3 Full Scale Fixtures. The fabrication of all cables and harnesses shall be in three-dimensional form on full-scale fixtures.

1.4.3.1 Minor Variations. Minor variations in dimensions, breakouts, loops, and shape of a completed harness shall only be allowed to the extent that they do not affect interchangeability and fit of the installed harness.

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1.4.3.2 Complete Mock-up Fixtures. The fixtures shall simulate in three-dimensional form all connections, attachment points, interferences, and other special problem areas which affect the configuration and installation of the completed cabling, including the following:

a. Fabrication fixtures shall be provided for each harness.

b. Each cabling fixture shall be designed to correctly locate all connectors, harness mounting straps, clamps and/or associated brackets and to allow the harness to be removed without disassembly.

c. Fit and installation of harnesses fabricated on harnesses shall be verified on the mock-up.

d. Fabrication of system harnesses, or portions thereof, shall be completed on a full-scale mock-up of the basic equipment configured with dummy subassemblies.

e. Mockups shall be the base on which the system harness is developed and updated and serve as a guide to verify routing, fit, and installation of subsystem harnesses.

f. Mating connectors, connector and harness support brackets, and fasteners shall be provided per the following:

(1) Mating connectors shall locate the harness connectors (plugs) in the actual position with the correct shell orientation and/or insert keying.

(2) Fasteners and attachment points shall be located in their final position.

(3) The fixture shall permit mated harness connectors to be oriented in a horizontal position to allow application and curing of sealing and potting compounds.

(4) Brackets shall be provided for receptacles and rails or other harness support structure for the harness wiring.

1.5 Bundle Formation

1.5.1 Handling.

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1.5.1.1 Harness Handling. The harness shall allow for normal movement during installation, mating, and demating of connectors.

1.5.1.2 Harness Flexibility. When flexibility is required, individual harness wire components shall be twisted with a lay length between six and 16 times the cable diameter.

1.5.1.3 Bending and Twisting. The harness shall provide for flexibility either by bending or twisting.

1.5.1.4 Wire Fan-out. Harness wires shall fan-out to solder splices, shield terminations, and connectors in a manner that precludes sharp or severe wire bends.

1.5.1.5 Slack. Slack shall allow free movement of wires at junctions, supports, terminations, articulating members, shock and vibration mounted equipment, and ease of maintenance.

1.5.2 Spot Ties. Spot ties shall be used to form and secure the wires together in the harness, to secure jackets, splices, and shield terminations and to attach harness and cables to their mounting.

1.5.2.1 Knot Position. The lacing tie knot shall be positioned on cable bundles to prevent abuse or abrasion from:

a. Handling and installation

b. Chassis, structures, and hard material protrusions

c. Harness mounting surfaces and potting

1.5.2.2 Lacing Requirements. Lacing tape requirements for part type, bundle diameter, strength and spacing of spot ties shall be as specified in Table 3.12-2.

1.5.2.3 Tie Material. Tie material shall conform to JPL drawing ST12013.

1.5.2.4 Shuttle Tie Material. When used in the Shuttle crew compartment, MSFC HDBK-527 and NHB 8060.1B shall also apply.

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1.5.2.5 Bundle Breakout. Breakouts shall be configured to restrict improper mating of closely located identical connectors.

Table 3.12-2 Lacing Tape Strength

Lacing Tape Part No.	Bundle Diameter (D)	Lacing Tape Strength	Distance Between Ties	
			Minimum	Maximum
ST12013-4	< 0.25	50	0.50 inch	0.75 inch
ST12013-5	0.25 to 1.5	50	2D	3D
ST12013-6	> 1.5	80	1.2D	1.8D

1.5.2.6 Bundle Routing. The routing of cabling and wiring shall be as follows:

a. Wiring shall be routed to follow the contours of the chassis or structure so that it can be adequately supported for maximum protection from abrasion.

b. The routing shall minimize interference with areas that require access during operations.

c. Whenever possible, cables and wires shall be routed to avoid contact with rough or irregular surfaces, sharp or chamfered edges, grommets and other adverse conditions.

d. Insulating sleeving or wrapping with abrasion resistant insulating material shall be utilized where wiring is routed across sharp edges or adjacent to an object which could cause damage.

e. The cable routing shall allow accessibility to connectors, terminals, mounting screws, and replaceable or repairable items.

1.5.2.7 Operational Interference. Cabling and wiring design shall cause no interference with the operation of optical, RF, particle and magnetic field sensing or radiating devices, attitude control jets and nozzles, and articulating mechanisms.

1.5.2.8 Bend Radii. Cable bundles and individual conductors used in wiring harnesses and cable bundles that are formed into bends during fabrication shall not be bent into a tighter radius than the values noted in Table 3.12-3.

1.5.2.9 Service Loops. In general, excess lengths of cable are not allowed beyond that which is necessary to satisfy the requirements of function, operation, and installation. Slack shall be designed into cable bundles and wires for the following purposes:

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a. To facilitate the proper mating of connectors and entry into termination.

b. To permit ease of maintenance.

Table 3.12-3 Bend Radius vs. Wire Type

Type of Wire	Minimum Bend Radius
Individual Wire	3xD, 1/16 inch minimum
Multiconductor and Shielded Wires	6D
Coaxial	7D
Tied Cable Bundles	10D

c. To prevent mechanical strain on wires at junctions, supports, and terminations.

d. To permit free movement of shock and vibration mounted equipment.

e. To permit required movement of articulating members.

1.5.2.10 Cable Support. Cabling and wiring shall be adequately supported or secured to structures with clamps, tie-wraps, spot bonding or with fixtures during fabrication.

1.5.2.11 Protective Material. Additional brackets and supports shall be provided if the existing structure does not provide suitable attachment.

1.5.2.12 Tie-Wrap and Clamp Spacing. Tie-wraps and clamps shall be defined on the harness subassembly drawing based on the location and spacing requirements of Table 3.12-4.

1.5.2.13 Protection. Protection in the form of chamfered edges, grommets, insulating sleeving, or wrapping with abrasion-resistant insulating material shall be provided locally where wiring is routed across sharp edges or adjacent to an object which could cause damage, and conform to the following requirements:

a. The protective material shall be applied either to the cable or to the object in a position that protects the wiring from damage.

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b. Wire bundles not otherwise jacketed shall be wrapped with an approved insulting protective material at the point of application of support hardware clamps, tie-wraps, etc. in a manner that maintains the circular cross-section of the bundle and prevents damage to wire insulation during installation.

Table 3.12-4 Clamp Spacing vs. Cable Diameter

Cable Diameter	Maximum Distance Between Clamps (Inches)
0 to $^1/_4$	4
$^1/_4$ to $^1/_2$	5
$^1/_2$ to 1	6
1 to $1^1/_2$	8

1.5.3 Splicing. Splicing of wires shall be permitted for the following purposes:

a. Spliced wires shall be used for multiple interconnections where a significant savings in wire and connectors or contacts can be realized or where individual connector contacts cannot carry the required current or accept the required wire size.

b. Interconnecting components provided with pigtail wire leads.

c. When access to connector solder or crimp joint is not possible or practical, spliced wires shall be used as approved by the cognizant engineer.

d. Solder splicing is the preferred method.

1.5.3.1 Ferrules. Splicing ferrules shall be selected as specified in Table 3.12-5.

1.5.3.2 Inspection Visibility. The solder termination shall be designed to allow inspection visibility for each conductor before the application of the protective insulation.

1.5.3.3 Shielded Wires. Splicing of shielded wires shall result in a minimum loss of shield coverage.

1.5.3.4 Parallel Splices. Parallel wire splices shall have the stripped ends pointing in the same direction in the immediate area of the connection.

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1.5.3.5 Connections. The splice connection shall be soldered per JPL D-8208, Section 3.14, or crimped per paragraph 1.5.6.

Table 3.12-5 Wire Splice Ferrules and Insulation

Ferrules and Insulation	Reference
Solder ferrule (inner)	Thomas and Betts (T & B) Type GSB Sleeves
Insulated crimp ferrule*	AMP 328307, 328308 T & B RA 14, RB 15
Uninsulated crimp ferrule*	AMP 34130, 34137 T & B A1A, B1B
Shrink Tubing	Kynar
Tubing	FEP Teflon
Slice Caps, shrinkable	Kynar
* See Table 3.12-7 for CMA capacity and use.	

1.5.3.6 Insulation Gaps. Insulation gaps shall be provided for inspection and the terminations insulated with shrink tubing marked with the splice number.

1.5.3.7 Splice Location. Splices shall be located as near as practical to the conductor termination, within connector potting boots whenever possible, or contained within the bundles.

1.5.3.8 Splice Identification. All splices shall be identified and fully defined on the associated drawings.

1.5.3.9 Mechanical Support. Splices shall be located where they can be adequately supported, preferably within the potted area of a connector or in a rigid or semiflexible portion of the cable.

1.5.3.10 Secondary Insulation. Splices outside potted areas shall be protected with a secondary insulating layer of shrink tubing.

1.5.4 Shielding and Shield Terminations.

1.5.4.1 Electrical Connections. All cable and wire shields shall be electrically connected according to the requirements of the fabrication drawing.

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1.5.4.2 Shield Termination. Shields shall be terminated using two-piece ferrules.

1.5.4.3 Multishield Ferrules. Multishield ferrules for pyro cables shall be located within the metal backshell assembly. Ferrules shall protrude above the potting a maximum of 1/8 inch for shell sizes 12 and 14 and a maximum of 1/4 inch for all larger shell sizes.

1.5.4.4 Hookup Wires. Hookup wires shall be connected to circuitry by soldering or crimping to a connector contact, circuit, or chassis grounding terminal.

1.5.4.5 Multiple Shield Ground. When more than one shield is to be grounded at a common location, the separate shields shall be jumped together and a single grounding lead used.

1.5.4.6 Maximum Jumper Termination. A maximum of two jumpers, or one jumper and one grounding lead, shall be used at a single shield termination.

1.5.4.7 Jumper Wire Length. The length of a jumper wire to its connection point shall be as short as possible and not exceed six inches.

a. The end of the shield shall be close to the connector (0.5 inch minimum), but within 3 inches of the connector.

1.5.4.8 Insulation Gaps. Insulation gaps shall be provided for inspection and the terminations insulated with shrink tubing.

1.5.4.9 Multiple Terminations. When all of the shields at a particular connector must be connected together, as a multiple shield, they shall be crimped between a combination of inner and outer shield collector rings.

1.5.4.10 Multiple Shield Terminations. Multiple shields shall be grounded with a grounding wire and/or by employing a braid clamp to connect to a metal backshell.

a. The end of the shield shall be as close as possible to the connector but within three inches of the connector.

b. Shield terminations shall use approved ferrules or bands.

1.5.4.11 Metal Backshell Requirements. Requirements governing the use of metal backshells are as follows:

a. When connecting to a metal backshell, the shield termination shall extend inside the backshell.

b. The shield shall have a sound, low-impedance bond to the backshell, connector, mounting structure, and mating connector.

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c. In all other applications, shields shall be insulated from ground or other conductors and shields, except where specified on the harness drawings.

1.5.5 Solder Connections. Unless specified otherwise, connections to circuit terminals and solder type connector contacts shall be by soldering.

1.5.5.1 Visibility. The design of the termination shall allow visibility of each conductor before application of protective insulation.

1.5.5.2 Single-Wire Terminals. Not more than one 20-24 AWG shall terminate in one size 20 connector solder cup.

1.5.5.3 Two-Wire Terminations. Maximum of two AWG 26 or AWG 28 wires shall be terminated in one size 20 solder cup.

1.5.5.4 Hand Soldering. Hand soldering shall be in accordance with paragraph 2.5.5.

1.5.5.5 Multiple Conductor Joints. On all multiple-conductor solder joints, the individual conductors shall meet the same requirements as in single-conductor joints.

1.5.6 Crimp Terminations. Crimp terminations shall be designed to provide conductor retention values equivalent to the wire tensile strength as listed in Table 3.12-6.

Table 3.12-6 Minimum Acceptable Tensile Strength

Wire Size (AWG)	Minimum Tensile Strength	
	Pounds	Kilograms
12	100	45.0
16	50	22.7
20	20	9.0
22	12	5.5
24*	12	5.5
26*	8	3.6
28*	5	2.3
* High Strength Alloy (55,000 psi)		

1.5.7 Strain Relief. Strain relief shall be provided at all connections, at the crimp or solder joint and in the solder wicked area of the wire to prevent damage as a result of normal handling.

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1.5.7.1 Minimum Requirement. As a minimum, the strain relief shall prevent flexure of the connection at the crimp or solder joint and in the area of solder wicking.

1.5.7.2 Proper Alignment. The type of strain relief used and the method of application shall assure proper position and alignment of contacts, and prevent leakage of the potting compound from contaminating the contact area.

1.5.7.3 Supplementary Support. Additional cable and wire support shall be provided if handling forces are present.

1.5.8 Identification. Cables, harnesses, and connectors shall be identified by marking with reference designation, functional titles, and other information defined by the cognizant engineer and project documentation governing equipment ID.

1.5.8.1 Cable and Harness Marking. Cable and harness marking requires unit reference designator, functional title, drawing number, revision letter assigned by the drawing, plus the serial number, and project identifier be marked on a label and affixed so that they are visible after installation of the cable into its next assembly.

1.5.8.2 Connector Marking. Connectors shall be marked per the following:

a. Hard-mounted receptacles shall have the connector reference designator affixed to the mounting bracket near the connector, in a position that is visible during and after mating.

b. Cabling and pigtails shall be marked with the connector reference designator assigned to the engineering drawing on the connector potting boot or connector assembly or backshell if present.

c. No identifying marking shall be applied to individual wires.

d. Splices shall be hot stamped with the assigned splice number.

1.5.8.3 Identification Marking. Identification marking of cable and harness assemblies as specified on the applicable drawing shall be typed on glass tape or impression stamped on shrink tubing or ink stamped on shrink tubing.

1.5.8.4 Metallic Tags. The use of metallic tags for identification shall be strictly prohibited.

1.5.8.5 ID Location. The identification shall be attached with lacing ties to a clearly visible portion of the harness.

1.5.9 Pre-/Post-Pot Continuity/Insulation Resistance.

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(1) Circuit Continuity—10 ohms or less at 5 vdc unless otherwise specified.

(2) Insulation Resistance—100 megohms at 500 vdc unless otherwise specified.

1.5.9.1 Cable/Harness Assembly Sealing and/or Potting. The Cable/Harness Assembly shall meet this requirement both before and after sealing and/or potting of connectors.

1.5.9.2 Cable/Harness Assembly Connectors. All connectors in each Cable/Harness Assembly shall be mated with test cables to the cable tester for Circuit Continuity/Insulation Resistance Testing.

1.5.9.3 Circuit Continuity. All Cable/Harness Assemblies shall be tested (per the applicable Wiring harness drawing) for Continuity between:

a. Each conductor and all other conductors,

b. Each conductor and all shields,

c. Each conductor and its respective connector's shell, and

d. Wherever continuity should not exist.

1.5.9.4 Insulation Resistance. All Cables/Harness Assemblies shall have a minimum insulation resistance of 100 megohms at 500 VDC between:

a. Each conductor and all other conductors,

b. Each conductor and all shields,

c. Each conductor and its respective connector's shell, and

d. Wherever continuity should not exist.

1.5.10 Handling and Storage. Cable handing and storage equipment shall be designed to the following minimum requirements:

a. Retain the original shape of the cable as much as necessary to prevent damage.

b. Provide protective covering of connectors.

c. Prevent exposure of cable to adverse environmental extremes (humidity, contamination, shock, vibration, etc.).

1.5.11 Cable Bake-out. When bake-out is required, the completed cable assembly shall be baked at 200°F, 10^{-5} torr in a vacuum chamber for 48 hours.

1.5.12 Rework. All cables and harnesses shall be designed to allow for rework to the following minimum requirements:

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a. It shall be possible to remove and replace wires, rectangular, circular and coaxial connectors, and splices.

b. It shall be possible to rework shield terminations.

c. The reworked items shall meet the same design requirements as the original hardware.

2 FABRICATION REQUIREMENTS

2.1 Fabrication Contamination Control.

Contamination control shall meet the requirements of Federal Standard FED-STD-209, Clean Room and Work Station Requirements, Controlled Environment.

2.2 Documentation

2.2.1 Engineering Drawings. Engineering drawings shall take precedence over all other documents.

2.2.2 Notice of Nonconformance. Any fabrication procedures not meeting the requirements of this document shall be identified prior to the start of hardware fabrication.

2.2.3 Deliverable Package. For each deliverable item, a documentation package shall be maintained that includes an approved fabrication instruction, inspection data, deviation reports, and all MRB evaluations.

2.2.4 Manufacturing and Inspection Records. All manufacturing and inspection checks shall be recorded on approved fabrication instructions.

2.2.4.1 Materials Certification. Manufacturers of materials shall supply certification of conformance to the required and applicable specifications.

2.2.5 Traceability. Traceability shall be maintained throughout the process from receiving or source inspection to final tests.

2.2.5.1 Reverse Traceability. The information content of each document shall be sufficient to provide reverse-traceability.

2.3 Electrical Requirements

2.3.1 Circuit Continuity. The circuit continuity shall meet the requirements specified in paragraph 1.5.9.3 on page 3.12-19

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2.3.2 Insulation Resistance. The insulation resistance shall meet the requirements specified in paragraph 1.5.9.4 on page 3.12-19.

2.3.3 Conductors.

2.3.3.1 Conductor Size and Type. Conductor size, hook-up wire type, and construction shall be as specified on the applicable wiring harness drawing.

2.4 General Mechanical Requirements

2.4.1 Physical Properties. Cables and harness assemblies shall conform to the weight, physical shape, workmanship, and routing defined by the applicable assembly documentation.

2.4.1.1 Cable Construction. The cabling shall be constructed in three-dimensional form on full-scale fixtures.

2.4.1.2 Minor Variations. Minor variations in dimensions, breakouts, loops and shape of a completed harness shall be allowed only to the extent that they do not affect interchangeability or fit of the installed harness.

2.4.2 Connector Interfaces. Connector interface type, size, key, and physical location shall meet the requirements of the equipment to be cabled by use of an interface/fixture.

2.4.3 Complete Mock-up Fixtures. The fixtures shall simulate in three-dimensional form all connections, attachment points, interferences, and other special problem areas which affect the configuration and installation of the completed cabling, including the following:

Note: In the absence of harness and cable assembly drawings which fully define the physical configuration of the completed cabling, the fixtures or mock-ups shall be used to define the configuration consistent with the above.

a. Fabrication fixtures shall be provided for each harness.

b. Each cabling fixture shall correctly locate all connectors, harness mounting straps, clamps and/or associated brackets and to allow the harness to be removed without disassembly.

c. Fit and installation of harnesses fabricated on harnesses shall be verified on the mock-up.

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d. Fabrication of system harnesses, or portions thereof, shall be completed on a full-scale mock-up of the basic equipment configured with dummy subassemblies.

e. Mockups shall be the base on which the system harness is developed and updated and serve as a guide to verify routing, fit, and installation of subsystem harnesses.

f. Mating connectors, connector and harness support brackets, and fasteners shall be provided per the following:

(1) Mating connectors shall locate the harness connectors or plugs in the actual position with the correct shell orientation and/or insert keying to allow visual confirmation.

(2) Fasteners and attachment points shall be located in their final position.

(3) The fixture shall permit mated harness connectors to be oriented in a horizontal position to allow application and curing of sealing and potting compounds.

2.5 Bundle Requirements

2.5.1 General. Wires shall be formed and bound into a harness per the following requirements.

a. The location of break-outs and splices

b. Service loops and individual conductor length.

2.5.1.1 Bundle Shape. The bundle shape shall all result in the wires being equally stressed at the termination point (i.e., no taut wires at connectors).

2.5.1.2 Lacing Ties. Lacing ties shall be located and fabricated per Figure 3.12-3, Figure 3.12-4, Figure 3.12-5, and Figure 3.12-6.

2.5.2 Wire Grouping. Wire grouping shall conform to the following requirements:

a. Cable bundle connectors shall be wired to obtain an even distribution of wire tension with service loops to allow mating and demating of the connectors and entry into terminations.

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b. Individual conductors in a bundle must lie parallel and not entwine other conductors, except for multiple twisted wires and branched leads crossing other conductors as required by the plan of connection.

c. Wires that are to break out together shall be grouped together.

d. Within a cable, wire groups or bundles approaching breakout points shall be positioned to minimize the amount of harness distortion.

e. Wires approaching breakout points shall be grouped and twisted separately when necessary, with a minimum amount of crossover.

f. There shall be no splices in breakout areas.

g. Bundles shall meet the bend radius requirements of Table 3.12-3.

h. Spot ties shall be used to dress and support leads breaking out of a harness.

i. Splices shall be located as near as practical to the conductor termination, and within connector potting boots whenever possible, or buried within the bundle.

j. Splices on twisted wires are to be separated a maximum of 2 inches.

k. Shield terminations and splices shall be located away from the potting area or potting cup on a cable.

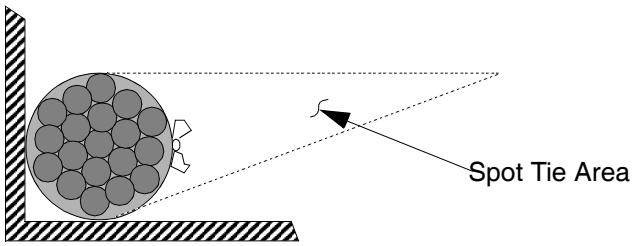

Figure 3.12-3 Lacing Knot Positioning

2.5.3 Flexibility. The harness shall meet the following flexibility requirements to allow for normal movement during installation and mating/demating of connectors:

a. Maintain flexibility of cabling assemblies by laying wires in the same direction.

b. To achieve maximum cable flexibility, wire type and cable size determine the cable lay (pitch rate).

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c. Provide for flexibility by either bending for twisting.

d. Provide adequate slack at all flexing locations.

e. Form wires that are fanned-out to solder splices or for shield terminations prior to soldering into connectors.

2.5.3.1 Special Flexible Cables. Special flexible cables which must meet specific dynamic motion requirements, i.e., articulation and deployment, shall meet the following additional flexibility requirements:

a. In cables that have to flex many times (articulation), twisting of the bundle is the recommended method of minimizing torque.

b. A development model may be required to determine the exact configuration.

c. The fixture shall include provision to simulate the movement limits.

2.5.4 Spot Ties.

2.5.4.1 Lacing Ties. Individual spot ties of lacing shall be used to form and hold wires together in the harness, to secure jackets, splices, and shield terminations, and to attach harness and cables to their mounting supports.

2.5.4.2 Individual Spot Ties. Individual spot ties shall be made using a lacing clove hitch knot as shown in JPL Specification FP513414.

2.5.4.3 Sleeve Fit. Spot ties shall be tight enough to confine the sleeving without causing compression or distortion.

2.5.4.4 Tie Spacing. Tie spacing shall meet the requirements of Table 3.12-2, except as listed Table 3.12-4 and Table 3.12-5, the first ties and those at specific locations: i.e., as shown in Figure 3.12-4, all wires emerging from potting boots are approximately parallel.

2.5.4.5 Spot Tie Location. Spot ties shall be located on both sides of a harness break-out 1/4 ±1/8 inch from the nearest edge of the breakout per Figure 3.12-5.

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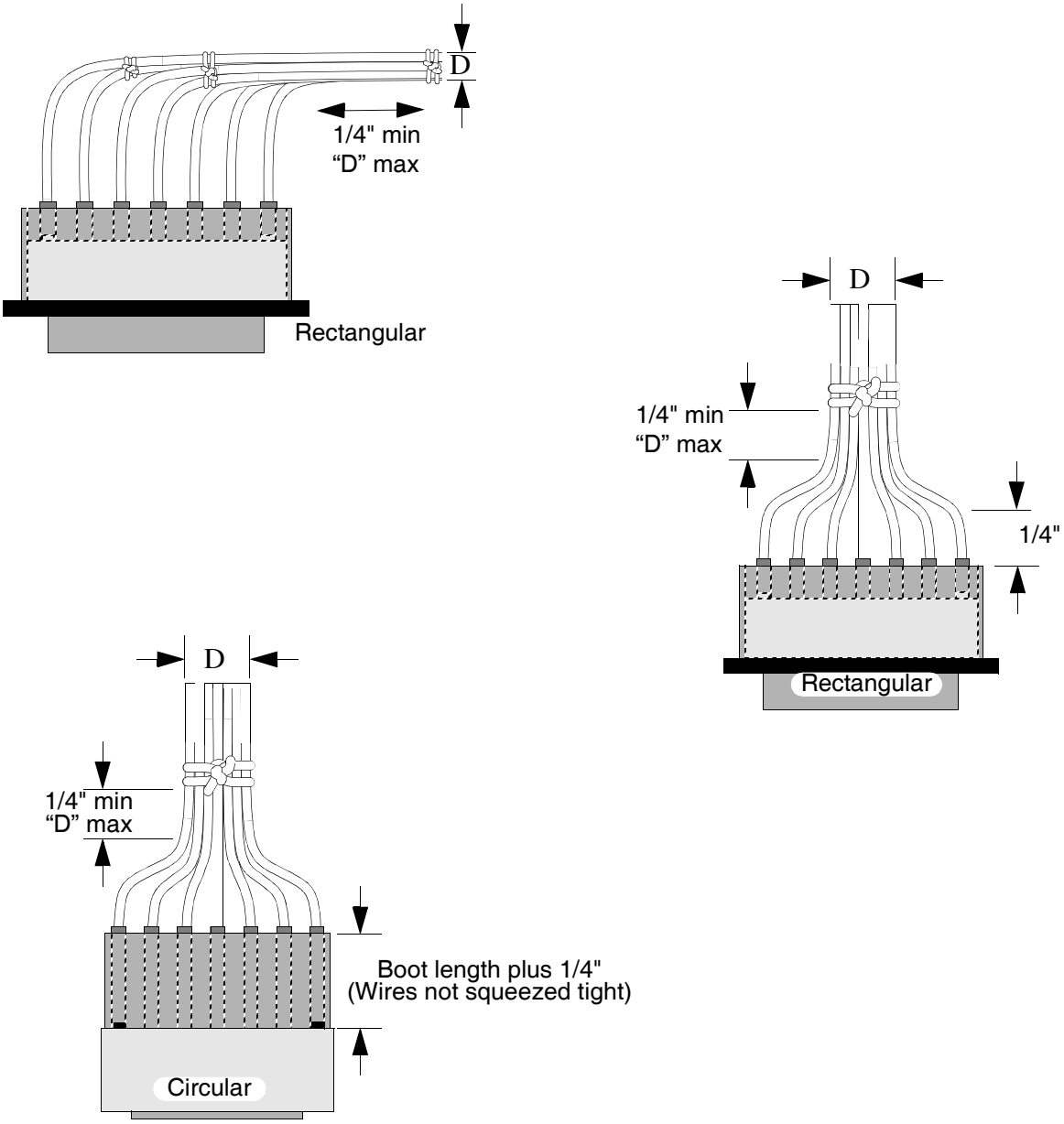

Figure 3.12-4 Lacing Tie Position at Connectors

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2.5.4.6 Spot Tie Breakouts. Spot ties shall be used to dress and support leads breaking out of a harness.

2.5.4.7 Breakout Wire Ties. Spot ties on the breakout wires shall be 3/8 ±1/8 inch from the main trunk per Figure 3.12-5.

2.5.4.8 Jacket Spot Ties. Spot ties used to secure jacketing to a cable bundle shall be located 3/16 ±1/16 inch from the end of the jacket.

2.5.4.9 Shield Termination Bundle. Spot ties used to secure shield terminations within a cable bundle shall be located over the ferrule portion or on both sides 1/2 +1/8 inch from the ferrule.

Note: For staggered terminations, there shall be not undue stress on the wires immediately next to the ferrules.

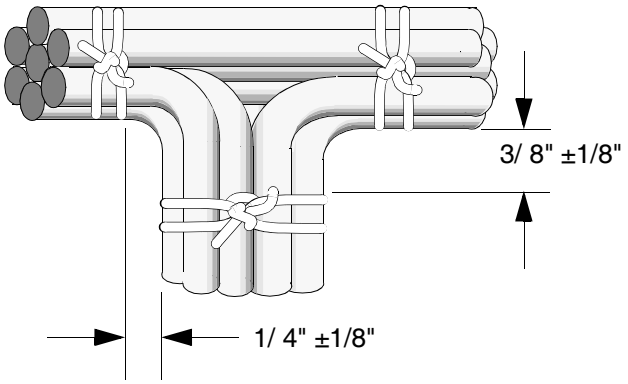

Figure 3.12-5 Spot Tying Cable Bundle Breakouts

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2.5.4.10 Spot Tie Fan Out. Spot ties shall be used to form wire bundle in place when fanning out individual wires into terminals per Figure 3.12-6.

2.5.4.11 Spot Tie Knot Position. The lacing tie knot shall be positioned on cable bundles per Figure 3.12-3 to prevent damage or abrasion from:

a. Handling
b. Chassis or structures
c. Hard material protrusions
d. Harness mounting surfaces
e. Harness potting
f. Installation

2.5.4.12 Support Structure Ties. Ties used to secure preformed and fabricated cables or harnesses to the mounting support structure shall meet the splice and shield termination tie locations criteria, and the spacing and installation requirements of applicable assembly or installation drawing.

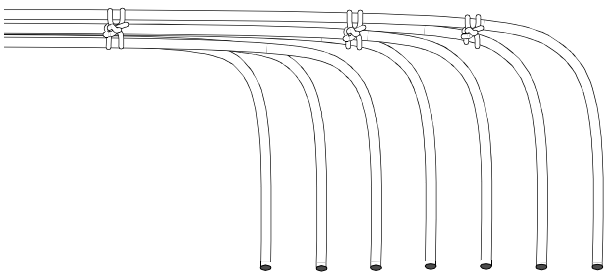

Figure 3.12-6 Fan Out Spot Tie

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2.5.5 Soldering. This subsection contains fabrication requirements for solder joints in electronic equipment. A solder joint or soldered connection is the area that joins similar or dissimilar metals by applying heat to the connection and adding solder. The connection must have solder and a solder fillet between the land material and the component termination. The amount of solder is defined in the specific paragraphs. Solder outside of the connection is not deemed part of the soldered connection and is not to be used as criteria for acceptable or unacceptable conditions.

2.5.5.1 General. To establish the electrical integrity of solder joints, special consideration shall be given to the mechanical geometry of the joints. A good solder connection shall reveal upon visual inspection:

a. Smooth surface

b. Concave fillet between conductor and termination, except for high-voltage joints

c. Contour of lead or wire visible in the solder except for high-voltage joints

d. Complete wetting

e. Lack of projections, bridging, fractures, porosity, and inclusions

f. No visible flux residues

g. Parallel lay of wire strands (i.e., no birdcaging)

2.5.5.2 Flux. Non-corrosive core solder flux and liquid rosin base flux used for tinning and soldering shall be Type R or Type RMA in accordance with MIL-F-14256.

2.5.5.3 Equipment and Operator Qualification. Manufacturers of solder joints for electronic equipment shall employ a certification plan that assures the equipment and operators used in the performance of critical processes and assembly operations are capable of performing those operations in a reliable, reproducible manner, such that the items produced will meet the requirements of this document and of the engineering drawings. The certification plan and certification records shall be available for JPL inspection.

2.5.5.4 Hand Soldering Equipment. The main criteria when selecting a soldering iron is the capability to melt solder on a wire or joint within a maximum of three seconds, as well as the capability to produce soldered joints meeting JPL criteria. The selection criteria shall provide for the greatest tip contact area and the maximum visual tip clearance. This involves tip size and geometry, and wattage.

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a. For general soldering, the tip idling temperature shall be controlled at 600 ±35°F. Other tip idling temperatures shall be approved by the responsible JPL Electronic Packaging Engineering personnel prior to use.

b. For general solder pot usage, the solder pot temperature shall be controlled at 500 ±25°F.

c. Either solid copper or plated copper tips may be used.

(1) Conductors shall be inserted to the full depth of the cup and not be too large for the cup.

(2) The soldered joint shall show a fillet of solder from the wire to all exposed edges of the solder cup.

(3) Solder joint fillets shall not be convex.

(4) Solder may wick up under the insulation, but it is desirable that the degree of wicking be only that amount which will provide adequate tinning.

(5) The contour of the wire strands above the solder joint shall be visible.

2.5.5.5 Solder Joint Profile. Figure illustrates acceptable solder joints; the solder flow shall remain within the profiles shown in Figure 3.12-7.

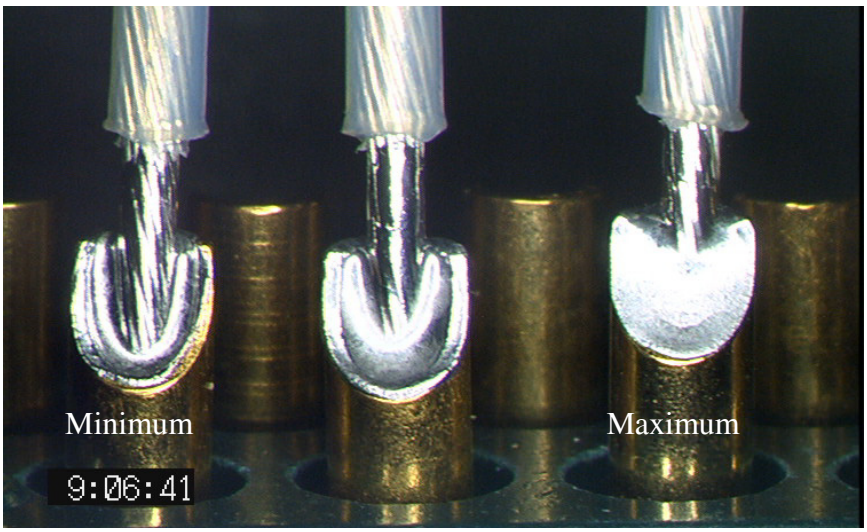

Figure 3.12-7 Solder Cup Profile

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2.5.5.6 Stripping. Stripped wires shall conform to the following requirements:

a. The distance from the end of the wire insulation to the terminal or connector solder cup shall be 0.030 to 0.090 inch.

b. The following damage shall be cause for rejection:

(1) Abrasions, cuts, gouges, nicks, scrapes, and indentations.

(2) Reduction in cross-sectional areas in solid conductors resulting from ringing, stretching, bending, or other distortions.

(3) Cracked or severed strands in stranded conductors.

(4) Punctured, crushed, or otherwise damaged conductor insulation.

(5) Plastic film deposit on the conductor strands resulting from the thermal stripping operation.

(6) Blistered or swollen wire insulation from thermal stripping (a slight discoloration is acceptable).

2.5.5.7 Tinning. Even if received tinned, solid wires and stranded wire shall be tinned by hand with a soldering iron or using a solder pot just prior to installation and joint assembly to the following requirements:

Note: Terminals and solder-through types of magnet wire are not required to be tinned. Tinning of solder cups is to be only when required by the drawing or other documentation.

a. Tinned surfaces shall be continuous, smooth, without inclusions, and with no evidence of nonwetting or dewetting.

b. Strands of stranded wire shall be visible under the solder coating.

c. Insulation on wires shall not be damaged by the tinning process.

d. The lay of the wire shall not be disturbed during tinning.

2.5.5.8 Two-Strand Wires. Two-strand wires in one solder cup shall be insulated and strain relieved with a common sleeve of shrinkable tubing.

2.5.5.9 Post Soldering Inspection. All solder joints shall be inspected using a magnification of 12X maximum. The following are cause for rejection.

a. Excess solder

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b. Insufficient solder

c. Cold or cracked solder joint

d. Any solder joint that has a solder surface with either a coarse or grainy appearance (as opposed to smooth), which exceeds 50% of the total solder surface.

e. Flux residue

f. Nonwetting

g. Pin holes

h. Any apparent build-up of solder or flux on areas adjacent to the joint

i. Solder joint fillet forming a convex solder surface

j. Wire insulation included in the soldered joint.

k. Burned or damaged wire insulation

l. Foreign inclusion in the solder joint

m. Solder projection or icicles

n. Birdcaged strands

2.5.5.10 Tubing Coverage. The insulation shrink tubing shall completely cover the uninsulated portion of the solder cup, the insulation gap and the additional length past the insulation gap as shown on Figure 3.12-8

2.5.5.11 Tubing Contour. The insulation shrink tubing shall conform to the contour of the solder cup and connection and securely grip the wire insulation.

2.5.5.12 Shrink Time and Temperature. The shrink time and temperature shall be controlled to prevent melting, damage, or stress to the solder joint or surrounding area.

2.5.5.13 Defects. Discoloration, charring, or splitting of the tubing shall not be allowed.

2.5.5.14 Sleeve Length. When using potting cups, the sleeve length shall not exceed the dimensions in the table provided in Figure 3.12-11 so that 1/8" of the wire insulation is encapsulated.

2.5.6 Cleaning. Cleaning requirements shall be as follows:

a. Removal of all flux residues shall be as specified in JPL D-8208, Section 3.16.

b. Cleaning and rinsing of solvents shall not affect or damage electronic equipment.

c. All particle contamination such as ash, loose wire fragments, insulation fragments, solder balls, and solder splatter shall be removed.

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2.5.7 Splicing.

2.5.7.1 Splice Bundles. Individual splices shall be buried and tied into the bundle without stressing the wire immediately next to the ferrules.

2.5.7.2 Splice Protection. All crimp and solder insulated splices outside potted areas shall be protected with an additional layer of shrink tubing.

2.5.7.3 Breakout Splice Prohibition. There shall be no splices in breakout areas.

2.5.7.4 Multiple-wire Splices. Splices on multiple twisted wires shall be separated by a maximum of two inches.

2.5.7.5 Location. Splices shall be located as near as practical to the conductor termination, and within the connector potting boots whenever possible, or buried within the bundle.

2.5.7.6 Identification. Splice identification shall be protected by secondary insulation as defined on the harness drawing.

2.5.7.7 Splice Numbers. The splice number assigned by the drawing shall be hot-stamped on the side of the insulated shrink tubing.

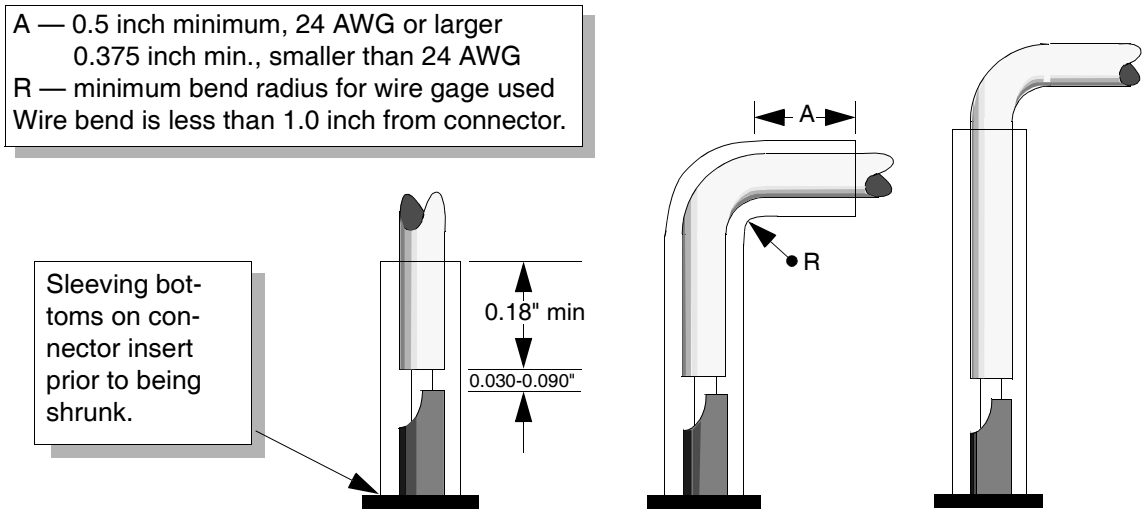

Figure 3.12-8 Solder Cup Insulation Gap

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2.5.8 Solder Splicing. The configuration of solder splices shall meet the requirements of Figure 3.12-9 and the following:

a. Solder ferrules shall be ultrasonically cleaned and tinned.

b. Solder ferrules shall not have any rough or uneven edge.

Note: For mass wire splices (4 or more wires) the insulation gaps and conductor protrusions should be on the high side of tolerance to allow for verification of wetting of each conductor without damage to the solder joint.

2.5.8.1 Solder Cup Insulation Gap. There shall be a 0.030 to 0.090 inch gap from the end of the wire insulation to the terminal or connector solder cup per Figure 3.12-8.

2.5.8.2 Connector Contacts. Stripped wires and insulation gaps shall be per Figure 3.12-9.

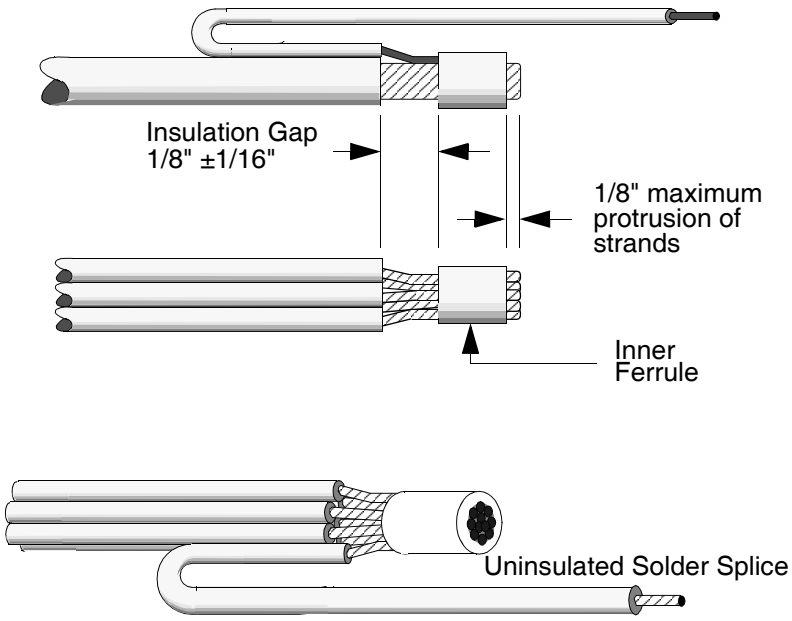

Figure 3.12-9 Solder Splices

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2.5.9 Crimp Splices.

2.5.9.1 Ferrule Selection. Ferrules and insulation used for wire splicing shall be selected from Table 3.12-7 and Table 3.12-5.

2.5.9.2 Ferrule Cleaning and Inspection. Prior to use, splice ferrules shall be ultrasonically cleaned per JPL D-8208, Section 3.16.

Table 3.12-7 Crimp Splices

Splice Ferrule			CMA Min/Max	Crimp Tool		
Type	**Amp**	**T & B**		**Amp**	**T & B**	**Nest (Die)**
Uninsulated	34130		509/3260	49935		18-22
		AIA	1000/3248		WT130A	
	34137		2050/5180	49935		16-14
		BIB	2050/5160		WT130A	
Insulated (**End Cap**)	328307		509/3248	47386** or 58250		Red (18-22) †ST11888-12
	328308		2050/5180	47387** or 59250		Blue (16-14) †ST11888-16
	329309		5180/13,100	59239-4		Yellow †ST11888-10

** Splice locator must be locked in the UP position to crimp correctly.
† JPL part number.

Note: Use any combination of wires having a total CMA within the CMA range of the splice. CMA values for wires are:

24 gauge:	22 gauge = 754	26 AWG-19 strand = 304
19-strand = 304	20 gauge = 1186	26 AWG- 7 strand = 277.83
7-strand = 277.83	16 gauge = 2426	

2.5.9.3 Insulation Gap Prohibition. There shall be no visible insulation gap on insulated end-cap ferrules as shown in Figure 3.12-10.

2.5.9.4 Inserted Strands. All wires strands shall extend into the ferrule.

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2.5.9.5 Strand Extensions. On uninsulated ferrules, individual strands shall protrude no more than 1/16 +1/32, -0 inch beyond the ferrule.

2.5.9.6 Twisted Wires. The ends of wires shall not be twisted together to form a single stranded conductor.

2.5.9.7 Bare Crimp Wire. Wires shall be untinned for crimp splice connections.

2.5.10 Crimp Contacts.

2.5.10.1 Crimp Combinations. The crimp contact, terminals, ferrule, or collector ring combination shall match the conductors being terminated.

2.5.10.2 CMA Match. The total circular mil area (CMA) of the conductors shall match the barrel size, CMA range, or wire combination specified for the crimp device per Table 3.12-7.

2.5.10.3 Tensile Tests. Tensile tests shall verify the conductor retention of the crimped joint.

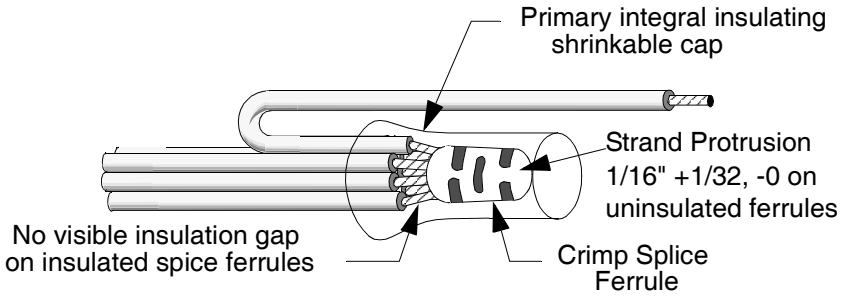

Figure 3.12-10 Insulation Gap

2.5.10.4 Wire Conformance. Crimped connections shall be made with untinned wire ends meeting the following requirements for conductor preparation:

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a. No abrasions, cuts, gouges, nicks, scrapes, indentations, cracked or severed strands after stripping the insulation from the wire.

b. No reduction in cross sectional areas of solid conductors: nicking, stretching, bending or other distortion.

c. No punctured, crushed or otherwise damaged conductor insulation or blistered or swollen wire insulation from thermal stripping.

2.5.10.5 Tool Control. Full-cycle crimping tools certified as conforming to MIL-C-22520 shall be used to make crimp connections.

2.5.10.6 Tool Calibration. The crimp tools shall be calibrated per paragraph 3.2.1.3.

2.5.10.7 Crimp Terminal Conductor Retention. Crimped contacts and terminals shall conform to the applicable areas with respect to wire retention and termination damage per MIL-C-22520 and MIL-T-7928 using compression crimping tools conforming to the tool requirements therein.

2.5.10.8 Conductor Position Verification. After crimping the connector contacts, the wire conductor shall be visible through the inspection hole at the bottom of the crimp barrel.

2.5.10.9 Open-End Barrels. For terminals having barrels open at both ends, the wire shall project through the barrel from flush to 0.06 inch.

2.5.10.10 Blind Cups. For terminals having a blind hole or cup, the wire end shall be inserted into the cup a minimum of 75% of its depth.

2.5.10.11 Fracture and Spalling. Crimped terminals, contacts, and splices shall exhibit no evidence of fracture or spalling.

2.5.10.12 Loose Strands. There shall be no loose strands or sharp ends of wire unsecured by the solderless connection.

2.5.10.13 Crimp Tool Control. Crimping tools shall be controlled as described below to assure the reliability of crimped connections:

a. Tensile tests shall be used to verify compatibility of the crimp device and matched tooling.

b. Tensile tests shall be used to establish initial calibration for each size and die combination to be used.

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c. Routine calibration gauging tests shall be used to determine that the crimping tools and die meet the established parameters

2.5.10.14 Tensile Tests. Three sample specimens for every different combination of crimp device, wire size, and dies shall be fabricated and tested for each tool used. The following requirements are a minimum:

a. The wire retention capability of the crimped connection shall be tested using a tensile tester with an accuracy of 0.5% at a head travel of 1.0 ±0.25 inch minimum

b. The mechanical connection of the wire and crimp device shall not break or become distorted before the minimum tensile strength specified inTable 3.12-6 on page 3.12-17 is reached.

2.5.10.15 Crimping Tool Check. Crimping tools shall be gauged and documented each day at the beginning and end of each work period using the tool manufacturers gauging procedures and parameters.

2.5.10.16 Tool Recalibration. Crimp tools exhibiting any dysfunction shall be adjusted and recalibrated.

2.5.10.17 Gauging Tests. Prior to use each day, crimping tools shall be gauged using the tool manufacturer's gauging procedures and parameters. Any tool exhibiting the following shall be reset and recalibrated:

a. Premature ratchet release before the dies mate (movement of dies is discernible).

b. Dies are misaligned.

2.5.10.18 Tensile Pull Samples. Test samples shall be pulled on a tensile testing machine to verify the crimp quality for JPL ST-series drawings, otherwise use MIL-T-7928. Refer to Table 3.12-6 on page 3.12-17 for crimped wire retention for lugs, contacts, and single ferrule terminations.

2.5.10.19 Crimp Tool Usage. The following information shall be made available for a specific tool model and serial number. It is to be recorded and kept as part of the permanent history.

a. Go/No-go test performed at the beginning of each work day.

b. The technician who used the tool on a specific day.

c. The results of gauging and tensile tests.

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d. The new information when the setting of the crimp tool has changed during the work period.

e. Specific connector and contact information as follows:

(1) The technician who performed the work and the date,

(2) The tool used by model and serial number, and

(3) All other contacts that were crimped by that technician on that day with that tool.

2.5.10.20 Crimp Terminations. When crimping is specified for terminating stranded wires, connector contacts, wire shields, lug terminals, and conductor splices, the ferrules and tools shall be selected from Table 3.12-7 on page 3.12-34.

2.5.10.21 Connector Contacts. Stripped wires and insulation inspection gaps shall be in accordance with Table 3.12-8.

2.5.10.22 Shrink Tubing. Shrink tubing (ST10017-2) shall be installed on crimp contacts used on connectors ST11956, ST11957, ST12023, ST12024, per Figure 3.12-11.

2.5.10.23 Inspection Hole. The shrink tubing shall line up with the inspection hole as shown in Figure 3.12-11. Shrink per paragraph 2.5.5.12 before inserting into connector.

Table 3.12-8 Contact Crimp Insulation Gap

Wire AWG	Minimum Insulation Gap
12-16	0.050
18-20	0.030
22-24	0.020
26.28	0.010

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Table 3.12-9 Crimp Connector Tooling

Contact	Crimping Tools*				Contact Insertion and Removal Tools
	Model No.	Positioner/ Turret Head	Selector Setting	Wire Size	
§030-9081-002 §031-9082-003	Daniels MH 860	86-1S Daniels	6	20#	M80969/14-02
			5	22	
			4	24	
			3	26	
M39029/4-110	Daniels AF8	Daniels TH 1A (Red Color Dot)	4	20#	
			3	22	
			2	24	
M39029/5-115	Daniels AFM8 or MH800	Daniels K 1S	7	20#	
			6	22	
			5	24	
			4	26	
030-9083-002 031-9135-000	Daniels MH 860	Daniels 86-2	7	16#	M81969/14-03
			6	18	
			5	20	
M39029/4-111 M39029/5-116	Daniels AF8	Daniels TH 1A (Blue Color Dot)	6	16#	
			5	18	
			4	20	
M39029/4-113 M39029/5-119	Daniels AF8	Daniels TH 1A (Yellow Color Dot)	6	12#	M80969/14-04
			7	14	
M39029/64-369 M39029/63-368	Daniels AFM 8 or MH800	Daniels K 13	7	20#	M81969/39-01
			6	22	
			5	24	
§330-5291-004 §031-1007-004			7	26†	
			6	28	
M39029/64-369 M39029/63-368	Daniels AFM8 or MH800	Daniels K325	4	22#	*MS27495A 22M *MS27495R 22M M81969/14-01
			3	24	
§39029/58-360 §39029/57-354			2	26	
			1	28	

*Special purpose tool—All tools must be calibrated by engineering.
Contact size (also maximum S13C)
† Contact size 20 with special crimp barrel for 26E28AWG (26AWG maximum wire size)
§ ITT Cannon part

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Table 3.12-10 Crimp Connector Tooling Selection

Contact (JPL ST No.)	Crimping Tools*				Contact Insertion and Removal Tools
	Model No.	Positioneer/Turret Head	Selector Setting	Wire Size (AWG)	
ST11280-1 ST11277-1	Daniels MH860	Daniels 86-1S	6	20	ST11961-1-20 or M81969/14-02
			5	22	
			4	24	
			3	26	
ST11279-1 ST11278-1	Daniels MH860	Daniels 86-2	7	16	ST11961-1-16 or M81969/14-03
			6	18	
			5	20	
ST11958-1-20 ST11959-1-20	Daniels MH800 or AFM8	Daniels K1S	7	20	ST11961-1-20 or M81969/14-02
			6	22	
			5	24	
ST11958-1-2026	Daniels MH800 or AFM8	Daniels K1S	6	26	ST11961-1-20 or M81969/14-02
			5	28	
ST11958-1-20 ST11959-1-20	Daniels MH800 or AFM8	Daniels K1S	7	2 wires 24	ST11961-1-20 or M81969/14-02
			6	2 wires 26	
			5	2 wires 28	
ST11958-1-16 ST11959-1-16	Daniels AF8	Daniels TH-1A (Blue Dot)	6	16	ST11961-1-16 or M81969/14-03
			5	18	
			4	20	
ST11958-1-12 ST11959-1-12	Daniels AF8	Daniels TH-1A (Yellow Dot)	8	12	ST11961-1-12 or M81969/14-04
			7	14	
			6	16	
ST11958-2-20 ST11959-2-20	Daniels MH800 or AM8	Daniels K13	7	20	ST11961-2-20 or M81969/39-01
			6	22	
			5	24	
ST11958-2-2026 ST11959-2-2026	Daniels MH800 or AM8	Daniels K13	7	26	ST11961-2-20 or M81969/39-01
			6	28	
ST11958-2-20 ST11959-2-20	Daniels MH800 or AFM8	Daniels K13	6	2 wires 26	ST11961-2-20 or M81969/39-01
			5	2 wires 28	
ST11958-3-22D ST11959-3-22D	Daniels MH800 or AFM8	Daniels K325	4	22	ST11961-3-220 or M81969/14-01
			3	24	
			2	26	
			1	28	

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Table 3.12-10 Crimp Connector Tooling Selection (Continued)

Contact (JPL ST No.)	Crimping Tools*				Contact Insertion and Removal Tools
	Model No.	Positioneer/Turret Head	Selector Setting	Wire Size (AWG)	
ST11958-3-22D ST11959-3-22D	Daniels MH800 or AFM8	Daniels K325	4	2 wires 26	ST11961-3-220 or M81969/14-01
			3	2 wires 28	

Table 3.12-11 Crimp Connector Tooling

Electrical Connector	Part Number	Contact Part Number		Wire Size	Approx. Wire Strip Length
		Pin	Socket		
Receptacle, Inflight Disconnect	DPYC-63-4	030-9081-002	--------	20,22,24	0.165
		030-9083-002	-------	16, 18,20	0.255
Plug, Inflight Disconnect	DPYC-63-3	-------	031-9082-003	20, 22, 24	0.165
			031-9135-000	16, 18, 20	0.255
Plug, Circular, Standard Contact Density	M83723/13 M83723/14	M39029/4-110	M39029/5-115	20, 22, 24	0.165
		M39029/4-111	M39029/5-116	16, 18, 20	0.250
		M39029/4-113	M30-20/5-119	12,14	0.250
Receptacle, Circular, Standard Contact Density	M83723/1 M83723/2	M39029/4-110	M39029/5-115	20, 22, 24	0.165
		M39029/4-111	M39029/5-116	16, 18, 20	0.250
		M39029/4-113	M39029/5-119	12, 14	0.250
Connector “D” Subminiature Pin	M24308/8-( )	330-5291-004		26, 28	0.165
		M39029/64-269		20, 22, 24	0.165
Connector “D” Subminiature Socket	M24308/6-( )		031-1007-004	26, 28	0.165
			M39029/62-368	20, 22, 24	0.165
Plug, Circular, High Contact Density	MS27472-( )	M39029/58-360	M39029/57-354	22, 24, 26, 28	0.150
Receptacle, Circular, High Contact Density	MS27472-( )	M39029/58-360	M39029/57-354	22, 24, 25, 28	0.150

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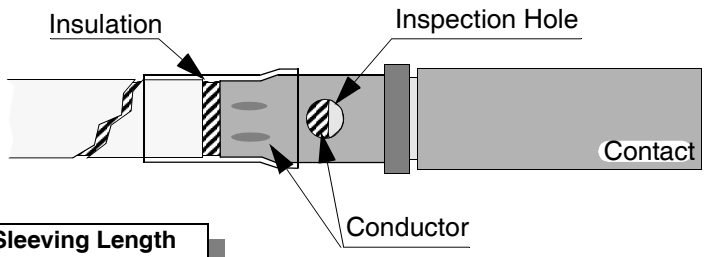
Table 3.12-12 Crimp Connectors, Contacts, Strip Length

Electrical Connector	JPL Standard Part No.	Contact JPL Standard Part No.		Wire Size	Approx. Wire Strip Length
		Pin	Socket		
Receptacle, Inflight Disconnect	ST10205-1	ST112804	----------	20,22,24	0.165
		ST11279-1	----------	16,18,20	0.255
Plug, Inflight Disconnect	ST10206-1	----------	ST11272-1	20,22,24	0.165
			ST11278-1	16,18,20	0.255
Plug, Circular, Standard Contact Density	ST11954	ST11958-1-20	ST11959-1-20	20,22,24	0.165
		ST11958-1-16	ST11959-1-16	16,18,20	0.250
Receptacle, Circular, Standard Contact Density	ST11953	ST11958-1-20	ST11959-1-20	20,22,24	0.165
		ST11958-1-16	ST11959-1-16	16,18,20	0.250
Connector "D" Subminiature Pin	ST 11957	ST11958-2-2026	----------	26, 28	0.165
		ST11958-2-20	----------	20,22,24	
Connector "D" Subminiature Socket	ST11956	----------	ST11958-2-2026	26, 28	0.165
		----------	ST11958-2-20	20,22,24	
Plug, Circular, High Contact Density	ST11949	ST11958-3-22D	ST11959-3-22D	22,24,26, 28	0.150
Receptacle, Circular, High Contact Density	ST11948	ST11958-3-22D	ST11959-3-22D	22,24,26, 28	0.150
Connector, High Density Socket, Rectangular	ST12024	----------	ST11959-3-22D	22,24,26, 28	0.150
Connector, High Density Pin, Rectangular	ST12023	ST11958-3-22D	----------	22,24,26, 28	0.150



Potting Cup No.	Sleeving Length
DS8828	1/4 inch
ST12025	3/16 inch
No Potting Cup	7/16 inch

Figure 3.12-11 Shrink Tubing Placement

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2.5.10.24 Sleeve Length. When using potting cups the sleeve length shall not exceed the dimensions provided in Figure 3.12-11 so that 1/8" of the wire insulation is encapsulated.

2.5.10.25 Unwired Cavities/Contacts. Unwired cavities/contacts in crimp connectors shall be filled with unwired contacts.

2.5.10.26 Push Test. All crimp type connectors used in flight cabling shall pass a 4-5 pound push test on 100% of the contacts.

2.5.10.27 Push Test Procedure. The push test procedure shall be as defined in JPL FP513414.

2.5.10.28 Crimp Conformance. Crimp connections exhibiting any of the following shall be cause for rejection:

a. Split, nicked or torn 0-rings or grommets
b. Scratched, gouged, nicked or otherwise damaged contact plating
c. Bent or broken contacts
d. Bent contacts which have been straightened
e. Dented or cracked connector shells
f. Cracked or split inserts or seals
g. Bent insert tines or damaged contact retention clips
h. Contacts showing signs of double crimping
i. Contacts which have been crimped by tools without a valid calibration decal
j. Crimp indentation contacting either the inspection hole or the wire crimp barrel rim
k. Less than 100% compliance to a 4.0 lb. to 5.0 lb. push test
l. Corrosion

2.5.11 Crimp-type Connector Contact Push Test Procedure. All crimp-type connectors on flight cabling must be subjected to and pass a 100% contact push test as part of final inspection and acceptance. This requirement formally complies with MSFC-STD-781, “Standard for Electrical Contact, Retention Criteria.”

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2.5.11.1 Equipment. The approved tool is manufactured by:

Russtech Engineering
23322 Madero Road
Mission Viejo, CA

Tool Part #: RTCRT

Tool Push Force: 4.0 to 6.5 lbs.

2.5.11.2 Proof the Tool. Push the tool on a scale. If the measurement is less than 6.5 lbs., it is within the required range listed above.

2.5.11.3 Push Test. The push test shall be performed as follows:

(1) Visually examine connector contacts for height and alignment variations. Unlocked contacts can sometimes be detected by uneven contact mating ends.

(2) Verify that tool calibration is current.

(3) Tools, associated hardware, and procedures shall be such that a straight push force can be applied to the mating face of the connector and contacts without any side loading of the contact, contact bending, or contact or connector damage.

(4) Tools shall be controlled so that no damage to connector is possible if a contact fails and pushes back.

(5) Push tests shall be performed without connector backshells in place to allow wired and unwired contact free movement without excessive restraints that could give a false indication of passing the force test or cause wire damage.

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Table 3.12-13 Connector Push Test Requirements

Probe Part No.	**Connector Family: MIL-C-38999 Series I**
RTCRT-12L P1	12 gage contact
RTCRT-16L-P1	16 gage contact
RTCRT-20L-P1	20 gage contact
RTCRT-22L-P1	22 gage contact
Probe Part No.	**MIL-C-38999 Series II ST11948, ST11949**
RTCRT-12-P1	12 gage contact
RTCRT-16-P1	16 gage contact
RTCRT-20-P1	20 gage contact
RTCRT-22-P1	22 gage contact
MIL-C-24308 ST11956, ST11957, ST12023, ST12024	
RTCRT-20P1	20 gage contact
RTCRT-22-P1	22 gage contact
MIL-C-26482 Series II ST11953, ST11954	
RTCRT-12-P1	12 gage contact
RTCRT-16-P1	16 gage contact
RTCRT-20-P1	20 gage contact

(6) Push tests shall be performed prior to potting, molding, or encapsulating of the wired connectors.

(7) Push tool shall provide a positive indication of application, conformance, and non-conformance to the forces specified.

(8) Any contacts that are visually discovered to be unlocked or that fail the force test shall be re-inspected, re-inserted, and force tested again.

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(9) If a second failure occurs, the connector shall be examined for mechanical damage. The wired contact shall be examined for mechanical damage, wire strands outside the crimp barrel, and insulation tags that could interfere with the connector contact retention clip. If damage is found, appropriate action shall be taken to repair or replace and document the damaged hardware, ensuring that adequate failure analysis is performed and documented.

(10) If no damage is found, the contacts shall be inserted a third time.

(11) Any further failure to lock shall be cause for rejection and replacement of contact or connector. Failure analysis shall be performed and documented.

(12) The results of the push tests of each individual contact shall be recorded on the appropriate documentation.

2.5.11.4 QA Verification. Quality Assurance shall verify the following:

a. All personnel performing the push test have been properly trained to perform this task and have demonstrated their ability to successfully accomplish the push test and inspections described here.

b. The push test tools are calibrated and have a current calibration date.

c. Push test data is included in the as-built documentation for each crimp-type connector.

d. Proper contact insertion and extraction tools are used.

e. All contact insertions are made in accordance with JPL D-8208.

f. There is no damage to contacts, connectors, or wires. Slight burnishing of contact plating surfaces is acceptable.

2.5.12 Shielding and Shield Terminations. Shielding and shield terminations shall conform to the following requirements:

a. Shields shall be brought up to the rear of the applicable connectors and the shield terminations located in the potted area.

b. Insulation gaps and other dimensions shall be as shown in Figure 3.12-12, Figure 3.12-13, and Figure 3.12-14.

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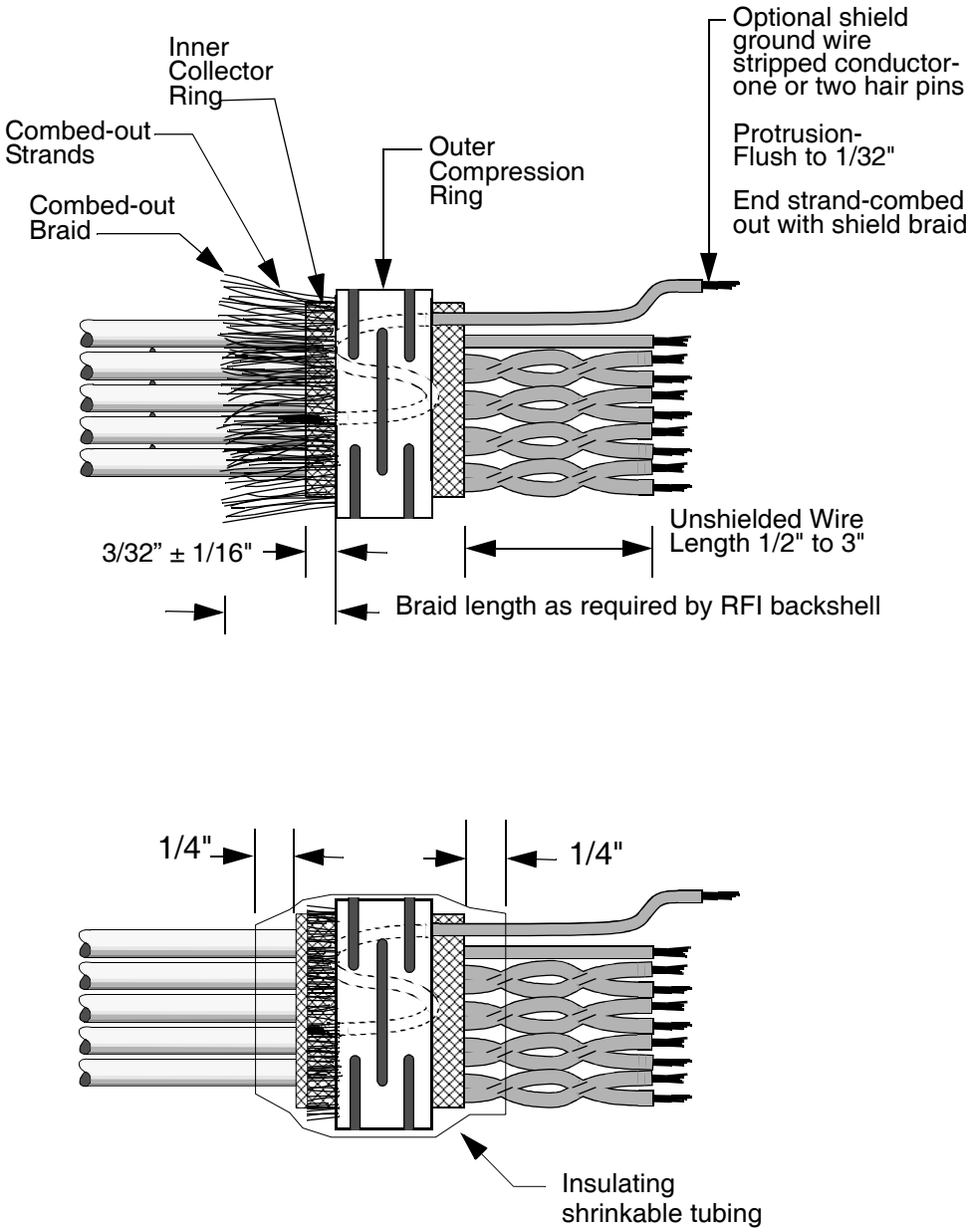

Figure 3.12-12 Multishield Crimp

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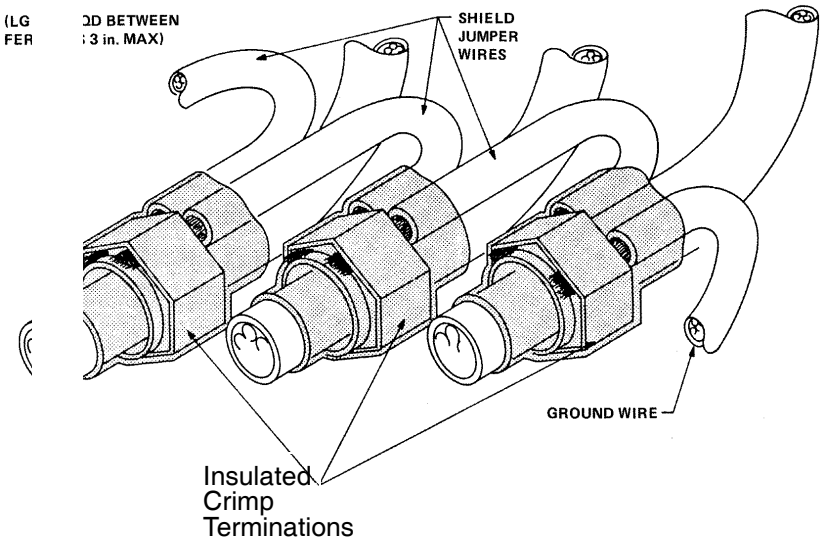

Figure 3.12-13 Series Jumper Termination

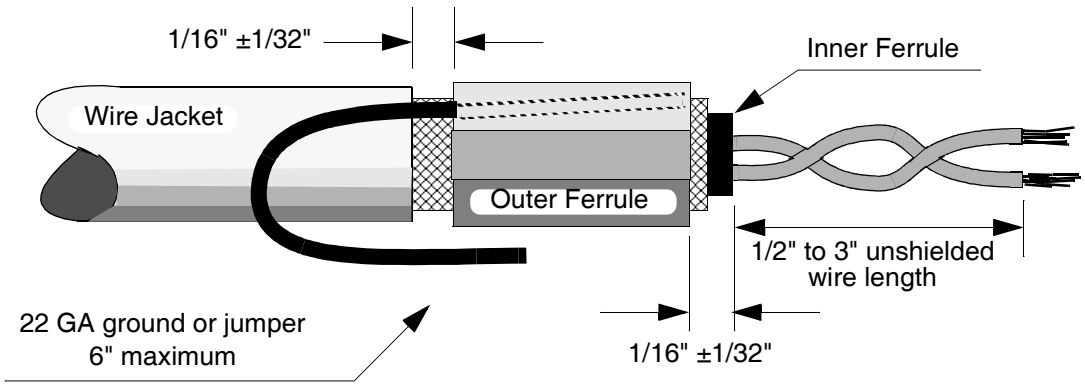

Figure 3.12-14 Crimp Terminations

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c. Crimp ferrules shall be protected and insulated with heat shrinkable tubing per Figure 3.12-15.

d. Shrinkable tubing shall conform to the contour of the underlying crimp, wires, and cable.

2.5.12.1 Staggered Terminations. For staggered terminations, there shall be no undue stress on the wires immediately next to the ferrule.

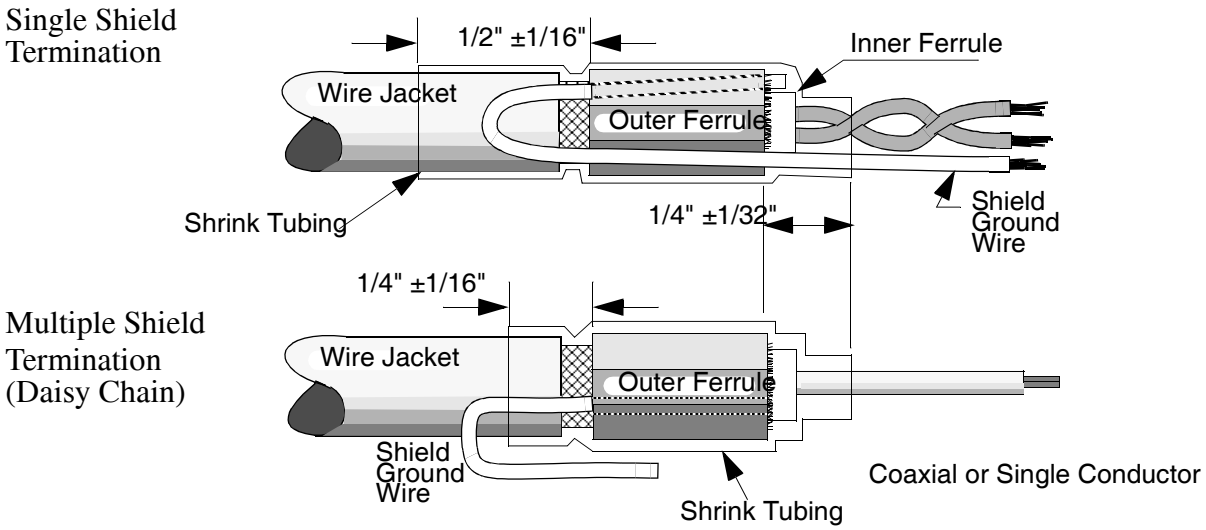
2.5.12.2 Cause for Rejection. The following imperfections shall be cause for rejection:

a. Damage to the conductor insulation, jumper, or ground wire.

b. Crimped indentation at the edge of the ferrule.

c. More than the maximum allowance of five percent damage to shield strands.

d. Discoloration to the termination tubing or wires cause by the shrinking process.



Also applies to coaxial cable.

Figure 3.12-15 Insulated Shield Terminations

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2.5.12.3 Shield Terminations. The electrical connection to an individual shield termination shall be made by crimping the end of the shield braid and one or more hookup wires together between inner and outer metal ferrules.

2.5.12.4 Shield Ferrules. Shield ferrules, sleeves, or rings shall be crimped in place using applicable matched crimping tool and die set specified for use with the ferrule combination.

2.5.12.5 Tool Control. The crimping tool and die set shall be controlled and within calibration per paragraph 3.2.1.3.

2.5.12.6 Termination Hardware. Ferrules and insulation used for shield terminations shall be selected according to Table 3.12-5.

a. Ferrules shall be ultrasonically cleaned prior to use and shall not have any rough or uneven edges.

b. Floating Shield. Unconnected, floating shields shall be fixed in place and protected with shrink tubing without the use of ferrules. See Figure 3.12-19.

c. Unshielded Wire Length. The unshielded length of the wire shall be a minimum of 1/2 inch and a maximum of 3 inches up to the connector solder cup or rear face of the insert, whichever is closer as shown in Figure 3.12-14, Figure 3.12-12, and 3.2.1.3.

2.5.12.7 Ferrule Conformance. Ferrules shall be free of indentations and bunching of the shield between the inner and outer ferrules.

2.5.12.8 Jumper Wires. The length of jumper wires shall be determined by the location of the connected shield termination. The length to its connection point shall be as short as possible and, unless otherwise specified, shall not exceed 6 inches.

2.5.13 Insulation and Strain Relief.

2.5.13.1 Insulation Exclusion. Multishield ferrules for pyro cables shall be located within the metal backshell assembly.

2.5.13.2 Ferrule Protrusion. Ferrules shall protrude above the potting a maximum of 1/8 inch for shell sizes 12 and 14 and a maximum of 1/4 inch for all larger shell sizes.

2.5.13.3 Complete Insulation. All harnesses, cables, and conductors shall be completely insulated to ensure against shorts.

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2.5.13.4 Taping. If required a spiral wrap of tape providing a minimum of 50% overlap shall be provided over the outer layer of wiring or braid in accordance with the drawing call-out.

2.5.13.5 Individual Connections. Strain relief shall be provided for individual connections.

2.5.13.6 Solder Connections. Solder connections, splices, and shield terminations at the rear of connectors shall be insulated, sealed, and potted.

2.5.13.7 Insulation. Insulation sleeving and shrinkable tubing shall be used over individual solder joints, splices, and shields not otherwise protected and insulated.

2.5.13.8 Supplementary Jacketing. Supplementary jacketing shall be applied to protect and insulate localized portions of the harness or cable as specified on the harness assembly or installation drawing.

2.5.13.9 Clamp Insulation. Pressure sensitive Teflon tape, or an approved substitute, shall be wrapped for a minimum of two layers in the area under clamps.

2.5.13.10 Spot Tie Sleeving. Insulation sleeving shall be used under all Ty-Rap plastic support straps.

2.5.13.11 Sleeving Protection. When bundles and cables must be routed across sharp or abrasive edges or corners a length of protective sleeving shall be positioned to protect the bundle from damage.

2.5.13.12 Insulation Exclusion. Separate primary insulation shall be excluded from crimp ferrules with integral end-cap insulation.

2.5.13.13 Tubing Overlap. Tubing shall overlap the insulated splice 1/4 +1/16, -0 inch as shown in Figure 3.12-16 and conform to the contour of the splice and wires.

2.5.13.14 Insulation Tubing. Individual shield termination, both uninsulated crimp ferrules and floating shield ends, shall be protected and insulated with shrink tubing (ST10017).

2.5.13.15 Shield Insulation. Insulation shall be utilized to protect shield from ground or other conductors and shields, except where specified on the harness drawings.

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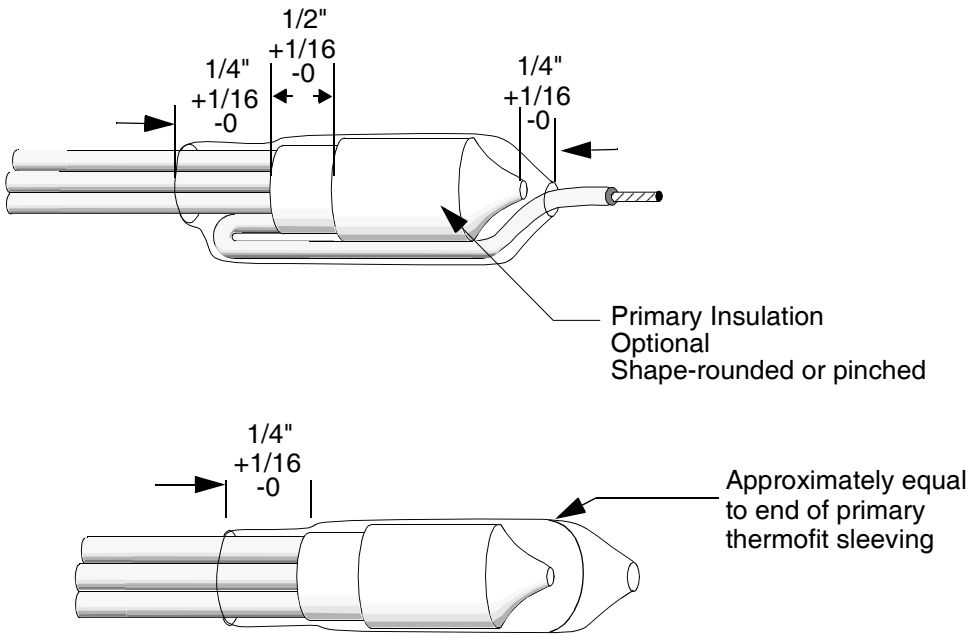

Figure 3.12-16 Additional Insulation

2.5.14 Connector Sealing and Potting.

2.5.14.1 Material Selection. All cabling connectors with solder connections shall be insulated, sealed, and/or potted with the materials listed in Table 3.17-1, JPL D-8208, Section 3.17.

2.5.14.2 Insulation, Potting and Sealing. All wired connections shall have passed an inspection for workmanship and electrical continuity prior to potting.

2.5.14.3 Connector Potting. Cabling connectors shall be potted to the full depth of the potting boot or mold.

2.5.14.4 Potting Boot Size. The potting boot shall match the connector shell size.

2.5.14.5 Surface Preparation. Inside surfaces of potting boots shall be sanded to increase adhesion to the potting material.

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2.5.14.6 Potting Boot Bonding. Potting boots for rectangular connectors shall be bonded as specified in the JPL D-8208, Section 3.17.

2.5.14.7 Potting Compound Coverage. Splice ferrules shall not protrude above the compound.

2.5.14.8 Termination Location. Shields and splice terminations on circular connectors shall be located within the potting boot as shown in Figure 3.12-17 and Figure 3.12-18.

2.5.14.9 Insulation and Strain Relief. Required methods of insulation and strain relief for several typical situations shall be as follows:

a. Rectangular Receptacles. Hard-mounted, no handling required after installation. Strain relieve with shrink tubing and seal per JPL D-8208, Section 3.17.

b. Rectangular Plugs. Installed with loose cable, mating handling required. Strain relieve with nylon potting boot, seal and pot per JPL D-8208, Section 3.17.

c. Circular Connectors. Subassembly mounted, no handling required. Strain relieve with shrink tubing and seal per JPL D-8208, Section 3.17.

d. Circular Connectors. Hard-mounted, minimum handling required. Pot in nylon potting boot or metal potting boot per JPL D-8208, Section 3.17.

e. Circular Connectors. Installed with loose cable, mating handling required. Pot in nylon potting boot or metal potting boot per JPL D-8208, Section 3.17.

f. Splices and Shield Terminations. Insulate with shrink tubing.

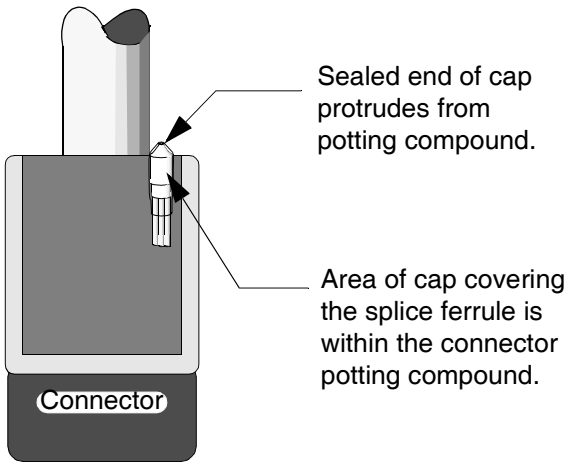

Figure 3.12-17 Splice Cap Position

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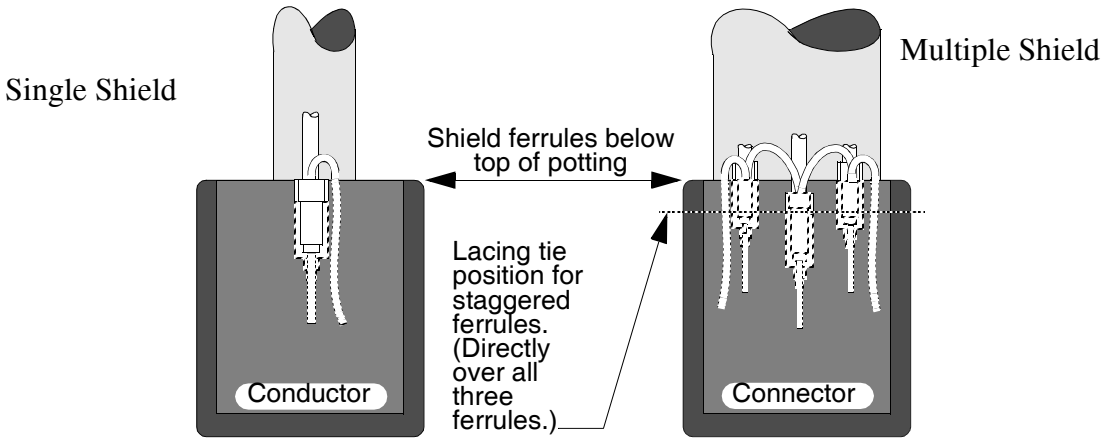

Figure 3.12-18 Individual Shield Positions

2.5.14.10 Examination. After bonding, connector contacts shall be completely free of adhesive as examined under 12-15x magnification.

2.5.14.11 Protective Jacketing. Protective insulation applied to local areas of cable bundles and cables shall conform to the following requirements:

a. Insulation sleeving shall be used under all plastic support straps (Ty-raps).

b. Sleeving covering bundles and cable routing across sharp or abrasive edges and corners shall be positioned to protect the wires in the bundle from damage.

c. Sleeves shall fit snugly.

d. Spot ties shall be tied sufficiently tight to confine to jacketing but not cause undue compression or distortion.

e. Tape used around wire bundle under clamps shall meet the following:

(1) There shall be a minimum wrap of two layers.

(2) The bundle shall be shaped into a circular cross-section.

(3) The tape shall be confined to the clamp area and provide a snug fit in the clamp.

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2.5.15 Cable Protection.

2.5.15.1 Insulation. The conductor insulation, jumper, and ground wire shall be free from damage

2.5.15.2 Post-Crimping Insulation Condition. Wire insulation shall grip the end of the wire insulation after crimping.

2.5.16 Flux Residue Removal. Removal of all flux residues shall be as specified in JPL D-8208, Section 3.16.

2.5.17 Crimp Termination Tubing. Tubing shall overlap the crimped terminations or ends of the folded back braid as shown on Figure 3.12-15 and Figure 3.12-19.

2.5.18 Two-Wire Strain Relief. Wires shall be insulated and strain relieved with a common sleeve of shrink tubing when two wires are terminated in one solder cup.

2.5.18.1 Identification Marking. Identification marking of cable and harness assemblies as specified on the applicable drawing shall be typed on glass tape and covered with kapton or teflon tape or impression stamped or shrink tubing.

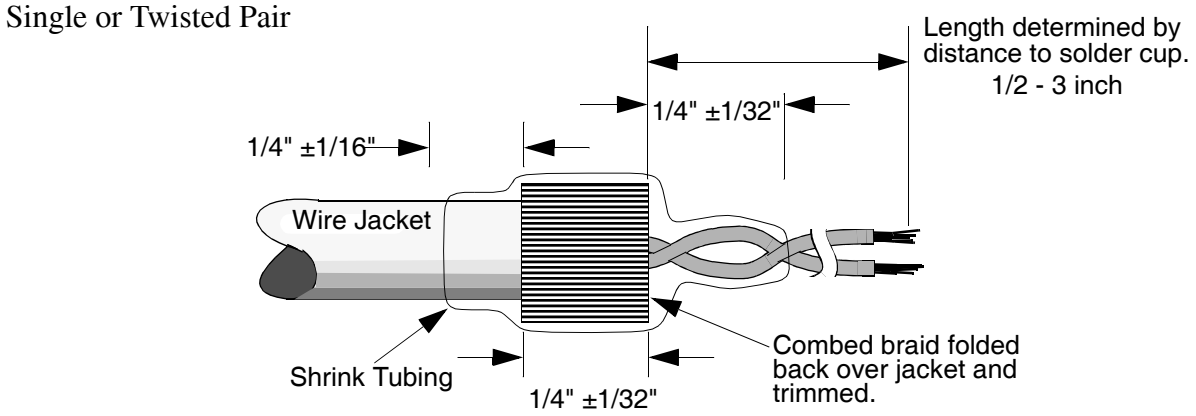

Figure 3.12-19 Floating Shield Terminations

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2.5.18.2 Cable and Harness Marking. Cable and harness marking requires unit reference designator, functional title, drawing number, revision letter, serial number, reference number, and project identifier be marked on a label and affixed so that they are visible after installation of the cable into its next assembly.

a. No identifying marking shall be applied to individual wires.

b. Splices shall be hot stamped with the assigned splice number.

2.5.18.3 Metallic Tags. The use of metallic tags for identification shall be strictly prohibited.

2.5.18.4 ID Location. The identification shall be attached to a clearly visible portion of the harness.

2.5.18.5 Connector Marking. Reference designation of connectors, per the applicable drawing, shall be applied as follows:

a. Hard-mounted receptacles shall be marked with the label affixed to the mounting bracket near the connector, in a position that is visible during and after mating.

b. Cabling and pigtails shall be marked on the connector potting boot or connector assembly or backshell if present.

c. On miniature, rectangular connectors:

(1) With potting boot: engraved or hot-stamped or ink stamped on the potting boot.

(2) Without potting boot: typed with black ink on glass tape and attached with clear Teflon tape, or approved substitute, on body of assembly

d. On miniature, circular connectors: hot-stamped, engraved, or ink stamped on the potting boot.

e. On metal backshells: rubber stamped or engraved on backshell or typed on shrinkable clear tubing.

f. As an optional method, or if hot-stamping cannot be used: typed with black ink on glass tape and attached with clear Teflon tape, or approved substitute. Height of characters shall be 1/8 inch minimum.

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2.6 Cable/Harness Fabrication Control.

A Cable/Harness Assembly Fabrication & QA Verification List should be completed for each cable/harness assembly. See Table 3.12-14. The checklist will be compiled after fabrication and completed prior to delivery of the assembly to accompany the AIDS and As-Built List.

Table 3.12-14 Cable/Harness Assembly Fabrication and QA Verification List

	Shop Verification	QA Verification
AK.Harness Identification 1. Drawing No. & Rev		
2. Drawing title		
3. Reference Designator		
4. Serial #		
AL.Harness Fabrication pre-pot electrical (Verify travelers are complete) 1. Workmanship		
2. Splices		
3. Shield Terminations		
4. Thermofit sleeving		
5. Wire type and awg		
6. Push-out test completed		
7. Contact/wire pull tests completed		
AM.Pre-pot Electrical (Visual Inspection) 1. Inspection of Harness & connectors		
2. Inspect connectors a. Gender b. Keying c. Clocking d. Cleanliness		
3. Spot-ties		
4. Verify parts to drawing		
5. Verify as built list is complete		
6. Verify AIDS are complete		
AN.Potting Cups and Hardware 1. Potting (if required)		
2. Sealing (if required)		
3. Potting cups, ears removed		
4. Clips and screws installed		

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Table 3.12-14 Cable/Harness Assembly Fabrication and QA Verification List (Continued)

5. Verify torque requirements are completed		
6. Staking of backshells if required		
AO.Final Inspection (post pot electrical) 1. Visual inspection of harness		
2. Verify electrical tests were completed		
3. Inspect connectors a. Gender b. Keying c. Clocking d. Cleanliness		
4. Verify harness label is correct		
5. Verify connector identifiers are correct		
6. Weight		
7. Verify As-built list is complete		
8. Verify AIDS are closed		
9. Date Assembly delivered		

3 QUALITY ASSURANCE

3.1 Verification Methods

3.1.1 Go/No-Go Test. The go/no-go test shall be performed prior to crimp samples; the information is to be recorded and kept as part of the permanent history.

3.1.1.1 Inspection. Verification by inspection is accomplished by comparing the requirements specified in Section 2 with the appropriate characteristics of an item. Inspection includes evaluation of mechanical functionality and accuracy as described in corroborating documentation; the information shall be recorded and kept as part of the permanent history.

3.1.1.2 Test. Verification by testing is accomplished by subjecting an item to a set of conditions under the control of approved plans, procedures, and test equipment which will provide a measurable response. The results of the test are compared with the expected results as specified in Section 2.

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3.2 Inspection Criteria

3.2.1 Crimp Sample Tests. Three crimp samples shall be made with the new setup using the same contacts and wire to be used on the flight hardware to certify the new settings. The result of this test shall be recorded and kept as a part of the permanent history.

3.2.1.1 Crimp Proof. A 3 lb. pull crimp proof test shall be performed using JPL tool 10108684 on all conductors to verify conductor retention within the crimped joint. The result of this test shall be retained for permanent history. This test is to be performed only if required by engineering drawing or approved fabrication instruction.

3.2.1.2 Crimp Tensile Strength. When tested as specified in Table 3.12-6, or if specified otherwise, refer to MIL-T-7928 for the minimum axial load required to separate the wire from the contacts (Type A) either by pulling the wire out of the wire barrel or wire barrel bushing or breaking the wire within the wire barrel or wire barrel bushing, shall be not less than the applicable limit. The average of three pull tests shall be recorded and kept as part of the permanent history. As a minimum, one out of three wires used for pull tests, with more than a minus 5% miminum, shall be doumented on an Inspection Report. No failures are permitted.

3.2.1.3 Routine Calibration. Routine calibration gauging tests shall be every 6 months to determine that the crimping tools and die meet the established parameters per MIL-C-22520, Rev. F.

3.2.2 Lacing Ties. Examination of lacing ties shall take place before the harness, cable or subassembly is accepted for potting, coating or encapsulating.

3.2.3 Tensile Tests. Tensile tests shall be used to verify quality of the crimp device and matching tooling, and to establish initial calibration for each size and die combination used.

3.2.3.1 Test Machine Accuracy. A tensile testing machine with the head travel adjusted to 1.0 inch ±1/4 inch/minute and an accuracy of ±12% shall be used.

3.2.4 Contact Push Test. All crimp type connectors must be subjected to and pass a 100% contact push test prior to potting, molding, or encapsulating the wired connector. The results of each contact push test shall be retained as permanent history.

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3.3 Cleaning

All cable and harness assemblies including connector mating faces and contacts, fastening devices and associated brackets, and hardware forming the assembly shall be cleaned when the fabrication and testing are completed. Methods and solvent used for cleaning shall not damage insulation and connector contacts and shall be per JPL D8208 Section 3.16. Cleaning of assemblies and use of cleaning solvents shall be minimized during the fabrication by proper in-process handling, protective caps or covers, and by the use of clean tools and the removal of flux residues during the different processing steps. Blow dry with clean air or high purity nitrogen at 20 ±5 psig or use a vacuum probe. Protective dust covers on connectors shall be clean and replaced after cleaning and inspection of the connectors. Cleaned cable/harness assemblies shall conform to the following:

Note: Examination of all fabrication and assembly shall be accomplished with a magnification of 12-15X maximum. Foreign material or damage visible at this magnification is permissible after consultation and with concurrence from JPL engineering.

3.3.1 Cable and Harness Assemblies. Cable and harness assemblies shall be free of:

a. Dust, dirt, grease, and other foreign debris

b. Conducting particles, solder ships, conductor strands, metallic chips on surfaces, trapped in bundles, and visible under insulating tubing

c. Contaminants and solvent cleaning residues

d. Physical damage

3.3.2 Mating Face/Insert. The mating face/insert of connectors shall be free of:

a. dust, dirt, grease, and other foreign debris

b. metallic particles, solder ships, conductor strands, metallic chips

c. Flux residues, solvent films, adhesives or potting compounds, and other nonconductive films

d. Scratches, gouges, or other visible damage

3.3.3 Contacts. Contacts shall be free of:

a. Dust, dirt, grease, and other foreign debris.

b. Metallic particles, solder chips, conductor strands

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c. Flux residues, solvent films, adhesives or potting compounds, and other nonconductive films

d. Bent or broken contacts (as manufactured)

e. Scratches, gouges, damaged contact plating, or other visible damage

3.3.4 Connectors. Connectors shall be free of:

a. Dust, dirt, grease, and other foreign debris

b. Metallic particles, solder ships, conductor strands, metallic chips

c. Flux residues, solvent films, adhesives or potting compounds, and other nonconductive films.

d. Dents or cracks

e. Damaged seals, cracks or split inserts

f. Bent insert tines

g. Scratches, gouges, and other visible damage

3.3.5 Connector Visual Inspection Guidelines. Connectors and contacts exhibiting any of the following shall be documented:

3.3.5.1 Flight (During Fabrication).

a.	Burnished Contact Plating	Acceptable
b.	Exposed Contact Basis Material	Not Acceptable
c.	Exposed Contact Underplating	Not Acceptable
d.	Corrosion	Not Acceptable
e.	Mechanical Damagey	Not Acceptable
f.	Contamination	Not Acceptable

Note: This can be a subjective call. Contamination that has thickness or can be moved with an orange stick is not acceptable. “Water marks” especially on non-mating surfaces can be acceptable. In general, these conditions can be kept to a minimum with proper cleaning methods.

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3.3.5.2 Flight (Post Fabrication).

a.	Burnished Contact Plating	Acceptable
b.	Exposed Contact Basis Material	In general, not acceptable. If exposed basis material is not on a mating surface, this can be the call of the Cog E. The exposed basis material must be cleaned to remove any remaining plating salts that might cause corrosion at a later time.
c.	Exposed Contact Underplating	In general, not acceptable. If exposed underplating is not on a mating surface, this can be the call of the Cog E. The exposed underplating must be cleaned to remove any remaining plating salts that might cause corrosion at a later time.
d.	Corrosion	Not Acceptable. Corrosion may be able to be removed leaving either exposed basis material or underplating. In that case, the above guidelines for exposed basis material and exposed underplating would apply.
e.	Mechanical Damage	In general, not acceptable. If the mechanical damage is in an area that does not affect form, fit, or function of the connector, the part may be used at the discretion of the Cog E.
f.	Contamination	Not Acceptable. It must be kept in mind that after each de-mate operation, some contamination is generated. Inspection is required after each de-mate and cleaning of some kind is required in most instances. This can also be a subjective call. How clean is clean enough? All marks from cleaning that are thick enough to be moved around with an orange stick must be removed. Most others can be minimized with proper cleaning.

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3.3.5.3 Mate with Flight.

a.	Burnished Contact Plating	Acceptable
b.	Contaimated Mating Surfaces	Not Acceptable. Part should be cleaned to remove any residue on mating surfaces.
c.	Exposed Contact Basis Material	Acceptable if mating surface is clean and will not damage mating flight contact.
d.	Exposed Contact Underplating	Acceptable if mating surface is clean and will not damage mating flight contact.
e.	Corrosion	Not Acceptable. In most cases, corrosion can be removed usually leaving either exposed basis material or underplating. Connectors should then be cleaned to remove any plating salts that might cause corrosion at a later date.
f.	Mechanical Damage	Acceptable, if damage is not on electrical or mechanical mating surfaces that could damage that mating connector.

3.4 Cable/Harness Inspection .

3.4.1 Harness/Cable Pre-Pot Electrical Verification . Verify workmanship and travelers are complete:

a. Workmanship

b. Splices

c. Shield terminations

d. Thermofit sleeving

e. Wire type and awg

f. Push-out test completed

g. Contact/wire pull tests completed

3.4.2 Harness Pre-Pot Electrical. Visual inspection

a. Inspect harness & connectors

b. Inspect connectors

(1) Gender

(2) Keying

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(3) Clocking

(4) Cleanliness

c. Spot-ties

d. Verify parts to drawing

e. Verify As-built list is complete

f. Verify AIDS is complete

3.4.3 Final Inspection Post-Pot Electrical. Final visual and completion of all documentation

a. Visual inspection of harness

b. Verify electrical tests were completed

c. Verify torque requirements were completed

d. Inspect connectors

(1) Gender

(2) Keying

(3) Clocking

(4) Cleanliness

e. Sealing or potting completed

f. Potting cup ears are removed

g. Staking of backshells if required

h. Verify harness label is correct

i. Verify connectors are identified correctly & capped or bagged

j. Weight

k. Verify As-Built List is complete

l. Verify AIDS are closed

m. Package and seal, QA verify and seal

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4 CONNECTOR MATING AND DEMATING

A special removal tool shall be used for demating individually mated rectangular "D-type" and rectangular high-density connectors. Removal tools may be used for circular connectors where access is difficult or spacing prevents a good hand grip. Demated connectors shall be protected with dust covers.

5 CABLING REWORK

The construction of all cables/harnesses shall allow for rework of the assembly. It shall be possible to remove and replace wires; rectangular, circular, and coaxial connectors; splices; and shield terminations. The reworked items shall be inspected and meet the same fabrication requirements as original hardware.

6 SHIPPING AND HANDLING

6.1 Handling Fixture

System cabling in a certified clean area shall be installed on a fabrication fixture or special handling fixture, unless special conditions of test, size, or operation preclude the use of fixtures.

6.1.1 Cabling, Handling, and Storage. Cabling, handling, and storage equipment shall be designed to the following requirements:

a. Retain the original shape of the cable as much as necessary to prevent damage.

b. Provide protective covering for connectors.

c. Prevent exposure of cable to adverse environmental extremes (humidity, contamination, shock, vibration, etc.).

6.2 Special Provisions

Transporting small cables or harness assemblies in the tote box instead of a shipping container shall be acceptable only when personally supervised by the responsible engineer or delegate.

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Magnetic Packaging Requirements

1 SCOPE

The requirements contained herein are applicable to custom magnetic devices, such as transformers, inductors, and magnetic surface mount devices (SMD).

1.1 Applicability

This specification is applicable to all NASA Jet Propulsion Laboratory (JPL) programs and contracts using magnetic devices for space flight applications and critical ground support equipment. It shall be invoked on all procurements for flight and critical ground support equipment magnetic devices. It shall apply to all in-house design efforts, all direct outside vendor procurements, and also to sub-tier vendor-manufactured magnetic devices for JPL programs and/or contracts.

2 GENERAL INFORMATION

2.1 Role of Electronic Packaging and Fabrication

As part of the DBAT process, all flight and engineering model (EM) magnetic devices should be procured through Section 349, Electronic Packaging and Fabrication. In addition to flight and EM magnetic devices, all other magnetic devices should also be procured through Section 349. Section 349 maintains a controlled Approved Vendor List (AVL) for the explicit purpose of facilitating the procurement of magnetic devices of all quality levels from flight to breadboard. Section 349 can quickly facilitate the procurement of magnetic devices since it maintains close contact with the magnetic device vendor base and periodically assesses the vendors' capabilities.

2.2 Waivers and Deviations

The requirements set forth in this document have been developed to ensure that the magnetic devices procured using this procedure meet or exceed expectations and to maintain the attendant risk at an acceptable level. Any or all of these requirements may be waived. However, the cognizant engineer must be aware that as requirements are waived, the risk of failure increases. The cognizant engineer, in conjunction with the program manager, must decide if this risk is worth waiving the requirements. All waivers to the requirements shall be obtained from the DBAT Process Owner in written form. See *Category A Waiver Request/Approval* on DMIE.

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2.3 Vendor Selection and Qualification

2.3.1 Vendor Selection. A recommendation may be made to add a particular vendor to the AVL based on either prior experience with the vendor or due to the vendor's outstanding reputation and/or unique capabilities. In this case, a JPL vendor survey team will perform a survey of the vendor's facility.

2.3.2 Vendor Capability. When assessing a vendor regarding his/her capability to build magnetic devices, the following items shall be reviewed and ascertained:

- Capability to build state-of-the-art magnetic devices;
- Capability to build specialty magnetic devices;
- Capability to build a particular category of magnetic devices;
- A proven track record for providing high reliability magnetic devices;

2.3.3 Survey Team. To determine a particular vendor's capability, a JPL survey team shall visit the vendor at his facility. Prior to being surveyed, a potential vendor shall be sent a letter informing them that a JPL Survey Team will be visiting their facility. The survey team shall consist of at least one representative from Section 349 (Electronic Packaging and Fabrication) and at least one representative from Section 506 (Quality Assurance).

2.3.4 Vendor Qualification. During or shortly after the survey, an informal profile of the vendor may be completed to conveniently summarize vendor information. If the particular facility is approved, the facility with an appropriate contact is added to the AVL (see 2.3.5). The vendor shall be notified either via telephone or email or both that he/she has been qualified.

2.3.5 Approved Vendor List. A list of suitable magnetic device vendors qualified for fabricating magnetic devices for JPL shall be kept. This list of suitable vendors shall constitute an Approved Vendor List (AVL); this AVL shall be maintained by Section 349 in a suitable spreadsheet format by the magnetic devices Process Engineer. It is to be shared only on a valid as needed basis.

2.3.6 Vendor Disqualification and Requalification. A vendor may be disqualified due to poor quality and/or untimely delivery. In the event that a particular vendor is disqualified, they shall be sent a letter specifying in exact detail why they are being disqualified and what steps are recommended in order to obtain requalification. This letter shall be written by QA and Section 349. In the event that disqualification is felt warranted, the vendor's

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name will be removed from the JPL AVL. If it is thought worthwhile to requalify the vendor based on corrective actions taken by the vendor to remedy the disapproval, a JPL Vendor Survey Team shall again perform a survey and follow the procedure stated above for new vendors.

3 UPFRONT ENGINEERING CONSIDERATIONS

3.1 Design For X

There are a number of important considerations that the designer should take into account to produce a high quality magnetic device. The following are set forth for heuristic consideration. These are:

- Design For Producibility.
- Design For Assembly.
- Design For Inspectability.
- Design For Testability.

It is the designer's responsibility to take into account all of the above in exercising the design function. Failure to take the above into consideration can result in an unsatisfactory product, that is, one that does not perform as intended in its service environment over the time period for which it was intended.

Designing for X is a nontrivial issue since if performed correctly, it results in a significant cost savings and generally a superior product. Costs escalate as the product passes out of the design stage through board fabrication and assembly and into final system test and integration. If a faulty product is not detected at that stage, it may result in a mission that is seriously compromised or that fails.

3.1.1 Design For Producibility (DFP). The aspects of DFP are:

- Do not needlessly design a magnetic device to a producibility level that makes it difficult to build the board.
- Adhere to recognized design rules.
- Plan ahead so that the magnetic device doesn't have to be fabricated under rushed conditions.

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3.1.1.1 Design Rules. The designer shall follow recognized design rules for designing the magnetic device, and shall exercise sound judgment in ensuring that the device shall not deviate too greatly from recognized designs.

3.1.1.2 Planning. In addition to following good design rules, both the designer and the project engineer should plan effectively to avoid a situation in which the magnetic device vendor must hastily fabricate the magnetic device. It is important to remember that the more complex the magnetic device, the more lead time should be allowed for its fabrication. Compressing the lead time is not recommended.

4 FABRICATION REQUIREMENTS

4.1 Documentation

4.1.1 Manufacturing Data. Manufacturing and inspection data shall be required for each assembly.

4.1.1.1 Parts and Material Certification. Certificates of conformance shall be required for all parts and materials used in the fabrication of flight-rated electronics.

4.1.1.2 Traceability. Traceability shall be maintained throughout the production process, from receiving or source inspection to final tests.

4.1.1.3 Reverse Traceability. The information content of the documents shall be sufficient to provide reverse-traceability.

4.1.2 Deliverable Package. A documentation package shall be maintained for each deliverable piece of electronic equipment to include an approved fabrication instruction, inspection reports, deviation reports, and all Material Review Board (MRB) evaluations.

4.1.3 Manufacturing and Inspection Records. All manufacturing and inspection checks shall be recorded on approved fabrication instruction accompanying each deliverable item to keep an accurate history of that part.

4.1.4 Manufacturer Approval. All magnetic devices for JPL flight electronics shall be fabricated by a JPL-approved source.

4.1.4.1 JPL Survey. JPL flight-approved manufacturers must have passed a survey performed by a JPL technical team.

4.1.4.2 Technical Team. The technical team shall consist of Electronic Packaging Engineering, Electronic Packaging Fabrication, and Quality Assurance representatives.

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4.1.4.3 Yearly Review. Qualified sources shall be reviewed on a yearly basis for continuation of their qualified status, unless they have provided quality product within the last quarter.

4.1.4.4 Key Personnel. Loss of key personnel vital to a reliable operation, transfer of operations to another facility that has not been approved, or deterioration of processes or controls beyond the point of immediate corrective action shall revoke qualification and require requalification and technical survey.

4.1.4.5 Requalification. Loss of qualified status for any reason shall require a requalification and a JPL technical survey team approval.

4.2 Cores and Windings

4.2.1 Materials. Cores, wire, and other materials shall be specified on the engineering drawing.

4.2.1.1 Toroidal Cores. Toroidal cores shall be clean, clearly identified, free from sharp edges and damage, and coated with an insulating and protective material.

4.2.1.2 Impregnated Taped Cores. Impregnated taped cores shall be clean, free from corrosion, and have laminations firmly bonded.

4.2.2 Windings. Windings shall meet the requirements of the engineering drawing.

4.2.2.1 Core Taping. All toroidal cores shall be wrapped with adhesive Mylar tape prior to winding per paragraph 6.5.1.

4.2.2.2 Winding Tension. The tension used in winding shall be the minimum required to pull the wire into position.

4.2.2.3 Wire Lay. The wire lay shall be smooth and uniform unless otherwise required by the detailed drawing.

4.2.2.4 Strain Relief Loop. A strain relief loop shall be provided for all spliced lead breakouts.

4.2.2.5 Toroid Loop Breakout. Toroid loop lead breakout shall be per Figures 3.13-23 and 3.13-24.

4.2.2.6 Splices. Interim lead wire splices and surface mount lead attachment shall conform to the requirements of paragraphs 6.5.1.11 through 6.5.1.12 and Figures 3.13-27 through 3.13-28.

4.2.2.7 Bend Radii. Wire bend radii shall conform to the requirements of paragraph 6.5.1.8

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4.2.2.8 Winding Impregnation. Magnetic assemblies using a split core configuration shall have the windings impregnated prior to core insertion

4.2.2.9 Chemical Wire Stripping. Stripping insulation from magnet wire by the use of chemical shall be prohibited per paragraph 6.4.

4.2.2.10 Mechanical Wire Stripping. Wire stripping shall done by abrasive stripping with fiber wheels.

4.2.3 Impregnated Taped Cores.

4.2.3.1 Narrow-Gap Cores. Narrow-gap cores shall have phosphor bronze bands per paragraph 6.3.3.

4.2.3.2 Non-Gapped Cores. Cores without air gaps shall have solderable tin-coated, low-carbon steel bands per paragraph 6.3.3

4.2.3.3 Core Face Bonding. Mating faces of impregnated taped cut cores shall be bonded per paragraph 6.3.2.

4.2.4 External Connections and Terminal Boards.

4.2.4.1 Terminal Boards. Terminal boards shall meet the requirements of the engineering drawing.

4.2.4.2 Minimum Clearance. Bifurcated terminals shall be spaced a 0.060 inch minimum clearance between conductors and 0.050 inch minimum between the terminals and the core and winding assembly.

4.2.4.3 Bifurcated Terminal Through-Holes. Bifurcated terminals with through-holes shall have the magnet wire soldered as shown in Figures 3.13-13 and 3.13-14.

4.3 Enclosures and Potting

4.3.1 Enclosures. Enclosures shall be per the engineering drawing.

4.3.2 Marking. Marking of the enclosure and leads shall be per the engineering drawing.

4.3.3 Lead Identification. Each lead shall have a temporary lead identification until the point when permanent identification is applied.

4.3.4 Potting. Potting shall be per the engineering drawing and paragraph 6.9.

4.3.5 Joint Inspection. All solder joints shall be inspected prior to encapsulation.

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4.3.6 Internal Solder Joint Location. Internal solder joints shall be located in accordance with the requirements of paragraphs 6.7, 6.8, and 6.13.

4.3.7 Stress Relief. Sensitive inductors and transformers requiring stress relief shall be coated using materials listed in paragraph 6.9.

5 QUALITY ASSURANCE

5.1 Verification Methods

The following methods shall be used to verify the requirements of this document.

5.1.1 Inspection. Verification by inspection is accomplished by comparing the requirements specified in JPL D-8208, Section 2 with the appropriate characteristics of an item. Inspection includes evaluation of mechanical functionality and accuracy as described in corroborating documentation.

5.1.2 Test. Verification by testing is accomplished by subjecting an item to a set of conditions under the control of approved plans, procedures, and test equipment which will provide a measurable response. The results of the test are compared with the expected results as specified in JPL D-8208, Section 2.

5.2 QA Requirements

5.2.1 Preliminary Inspection. Each magnetic part shall be examined under 12X magnification to verify that the construction meets the requirements of the assembly drawing.

5.2.2 In-process Inspection. The magnetic parts and components shall be measured to verify that the construction, physical dimensions, markings, and workmanship are in accordance with the assembly drawing and the requirements of JPL D-8208, Section 2.

5.2.3 Final Inspection. Each completed piece of magnetics shall be inspected with the unaided eye for correct markings, cleanliness, and absence of corrosion.

6 DESIGN REQUIREMENTS

6.1 Documentation Requirements

Documentation shall contain all information necessary to fabricate and inspect JPL flight-rated electronic equipment: physical, electrical, environmental, and process criteria.

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6.1.1 Drawing Standards. All drawings shall conform to JPL, STD-00001 and ANSI Y14.5 for reproducibility.

6.1.2 Assembly Drawing. The assembly drawing provides eight major types of information:

a. A detailed drawing will show the package outline, terminals or lead location, mounting, and marking. See Figure 3.13-1.

b. The schematic diagram will show the sequence for all windings. The winding nearest the core would be W1. The next winding would be W2 and continues until the last winding. The schematic diagram will also show wire gauge, number of turns, and start and finish of each winding. See Figure 3.13-2.

c. Winding Information Step-by-Step:

Toroids

A winding location, a winding type, which is continuous or progressive, a multifilar winding, insulation, wrapper, and lead wire breakout. See Figures 3.13-3 and 3.13-4.

Bobbins and Layer Windings

A winding type that is, either layer or random, a multifilar winding, insulation, wrapper, and lead wire breakout. See Figure 3.13-5.

d. Winding instructions are required in a step-by-step from start to finish. These instructions would include: wrapping the core, placement of the winding on the toroid, the use of fiberglass sleeving over the start and finish lead, the number of turns, if it is layer wound, the turns per layer, the wire gauge (AWG), including single strand or multifilar, and the required insulation. Each winding will be labeled for start and finish. See Table 3.13-1.

e. A complete electrical specification, which will include: dc resistance, winding inductance, turns ratio, magnetizing current, and the resonant frequency, and a schematic diagram of the test circuit and test equipment used.

f. A detailed drawing showing the internal construction details, such as terminations, splices, lead dressing, bonding and potting. See Figure 3.13-6.

g. Assembly notes are required in a step-by-step process from start to finish. After the transformer is wound and tested, then, place it in the cup, bond it, terminate the leads, and make it ready for in process testing. The last steps would be details on impregnating, embedment, and the final test and inspection. See Table 3.13-2.

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h. The parts List will include: item number, quantity required, part number, mil or industrial specification, nomenclature or description, material specification, and material suppliers. See Table 3.13-3.

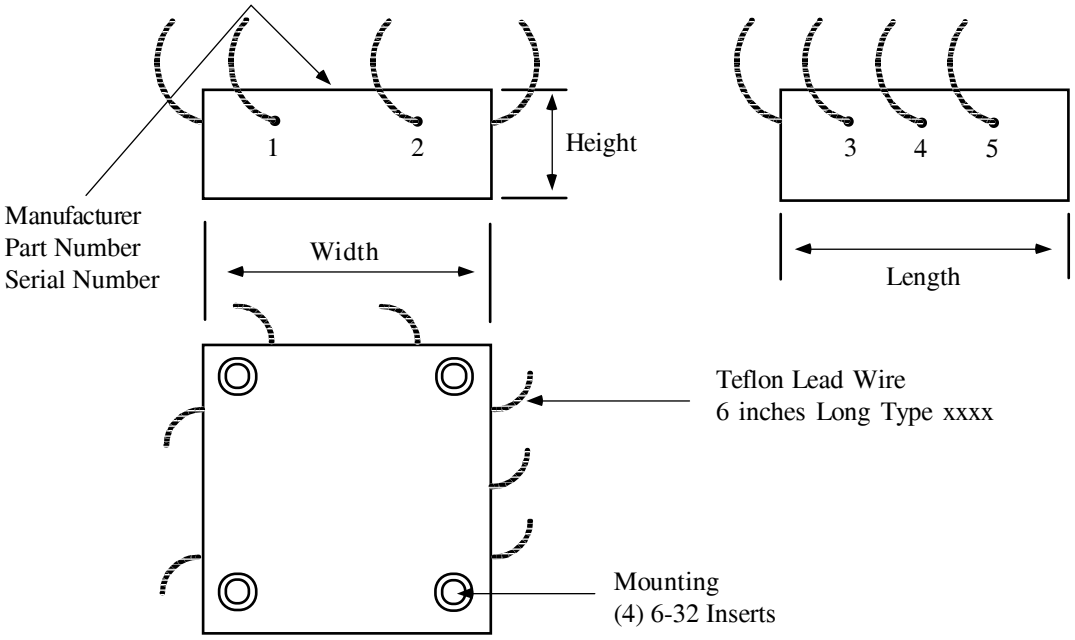

Figure 3.13-1 Typical Transformer Outline Drawing.

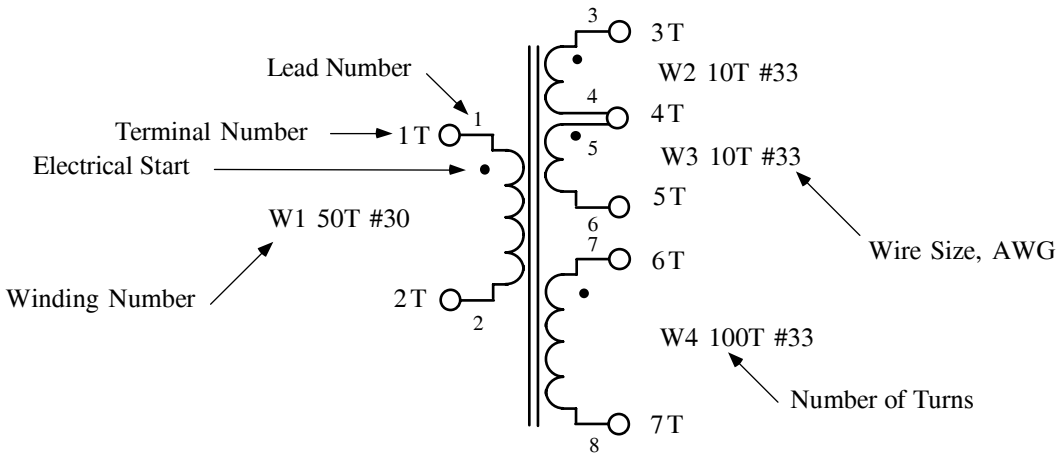

Figure 3.13-2 Typical Schematic Diagram.

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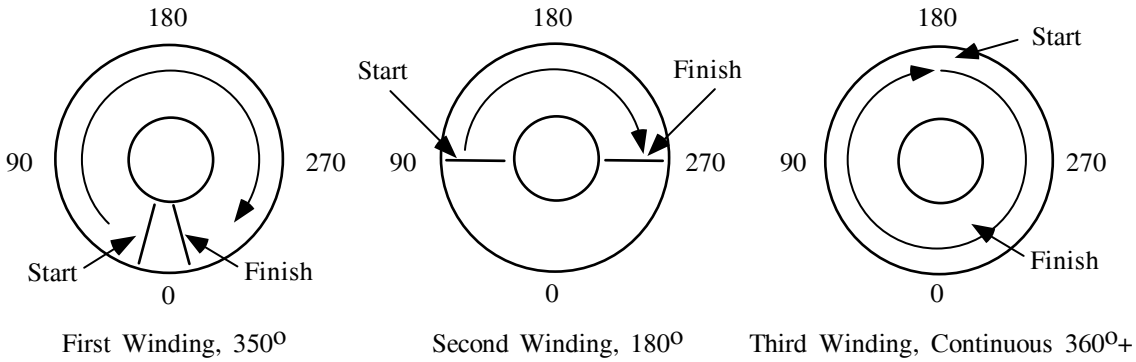

Figure 3.13-3 Winding Locations for Toroidal Transformers.

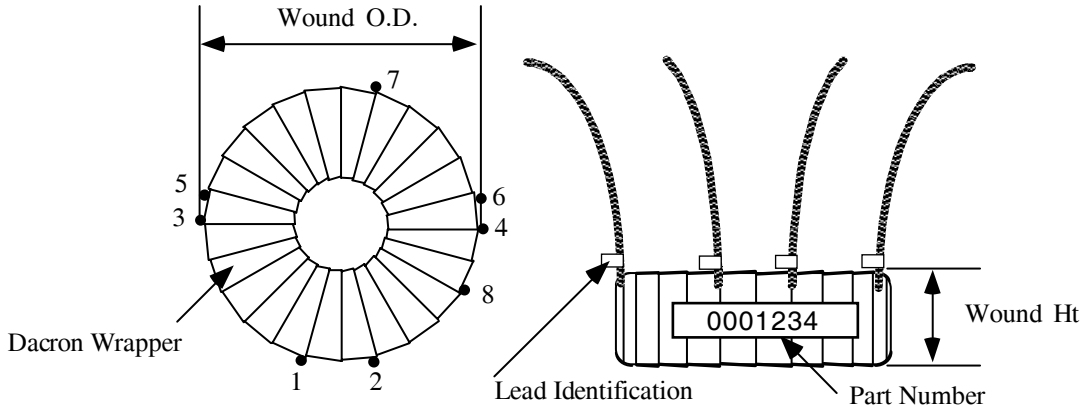

Figure 3.13-4 Finished Toroid, showing Lead Breakout and Dacron Wrapper.

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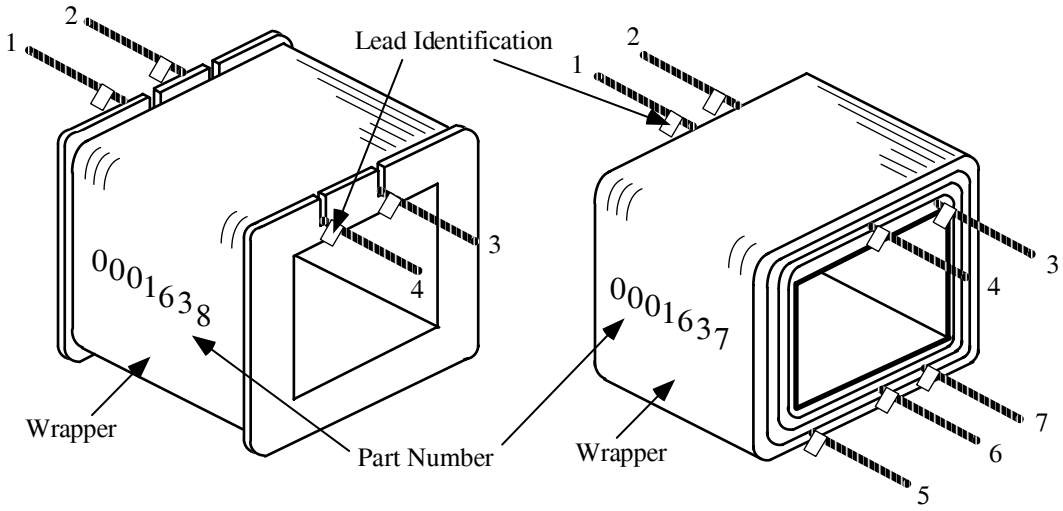

Figure 3.13-5 Finished Bobbin and Layer Coils, showing Lead Breakout.

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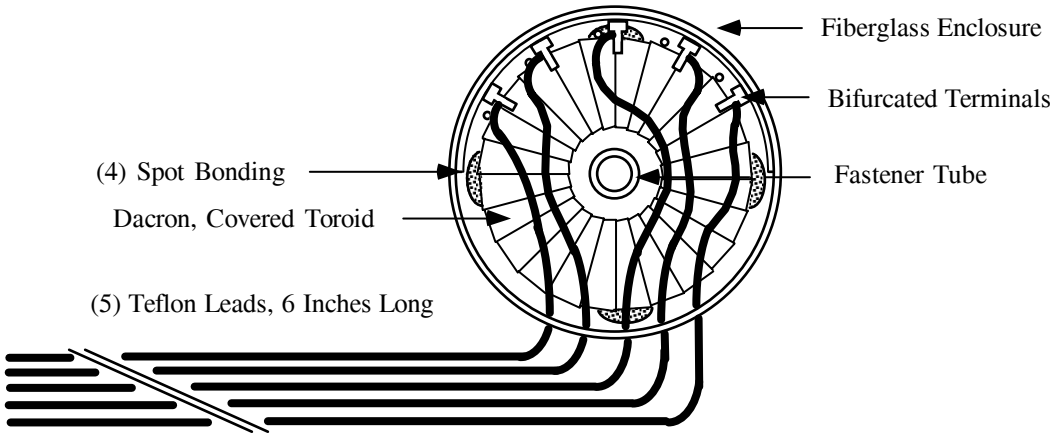

Figure 3.13-6 Transformer Top View of Assembly showing the Internal Construction.

Table 3.13-1 Example of Step-by-Step Winding Instructions.

Step by Step Winding Instructions		
Step No.	**Description**	**Reference**
1	Wrap the toroidal core, Item 1, with mylar tape, Item 2. Overlap is required, Secure the end with, Item 3.	Table 3.13-3 Figure 3.13-19
2	There are 4 windings, 2 single and 1 bifilar winding. The start and finish of each winding are distributed around the core, as shown in Figure 3.13-3.	Figure 3.13-2 Figure 3.13-3
3	(W1) Wind the core, Item 1, with 50 turns of #30 AWG magnet wire, Item 4. Place the winding, as shown in Figure 3.13-3. Progressively wind, 350°, and label Start 1 and Finish 2. Fiberglass sleeving, Item 7, will be used to cover the Start and Finish leads.	Figure 3.13-2 Figure 3.13-3 Table 3.13-3
4	Perform the required electrical test.	Paragraph 5.1.2-e
5	(W2, W3) Wind bifilar the core, Item 1, with 10 turns of #33 AWG magnet wire, Item 5. Place the winding, as shown in Figure 3.13-2 and Figure 3.13-3. Wind progressively, 180°, and label Strand 1 as Start 3 and Finish 4. Label Strand 2 as Start 5 and Finish 6. Fiberglass sleeving, Item 7, will be used to cover the start and finish leads.	Figure 3.13-2 Figure 3.13-3 Table 3.13-3
6	Perform the required electrical test.	Paragraph 5.1.2-e
7	(W4) Wind the core, Item 1, with 100 turns of #33 AWG magnet wire, Item 5. Place the winding as shown in Figure 3.13-3. Wind continuously 360 + and label as Start 6 and Finish 7. Fiberglass sleeving, Item 7, will be used to cover the start and finish leads.	Figure 3.13-2 Figure 3.13-3 Table 3.13-3
8	Perform the required electrical test.	Paragraph 5.1.2-e
9	Peripheral wrap, with mylar tape, Item 3.	Table 3.13-3
10	Dress the magnet wire leads to appropriate lead breakout locations See Figure 3.13-4.	Figure 3.13-4

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Table 3.13-1 Example of Step-by-Step Winding Instructions. (Continued)

Step by Step Winding Instructions		
Step No.	**Description**	**Reference**
11	Wind the Dacron insulating tape, item 6, 360°, progressively around the core, and secure the end with item 3.	Figure 3.13-4
12	Coil is ready for final assembly.	Figure 3.13-6

Table 3.13-2 Example of a Step-by-Step Assembly Procedure.

Step by Step Assembly		
Step No.	**Description**	**Remarks**
1 2 3	Check potting Cup, Part Number. Check potting cup (QA) approval. Check finished winding, magnet component, test data.	
4 5	Spot bond, terminal board in potting cup, using Stycast 1095. Spot bond, magnetic component in position, using Stycast 1095.	Sample
6 7 8	Inspection (QA). Cure Stycast 1095. Dress the leads of the magnetic component, as shown in the assembly drawing.	
9 10 11	Attach leads from the magnetic component to the terminals. Install and attach the external, teflon leads to the terminals. Solder all connections.	
12 13 14	Inspection (QA). Do final test before potting. Preheat magnet assembly for 3 hours at 70° C. (Bake out the moisture.)	
15	Fill the magnetic assembly with vacuum-degassed, impregnating material. When the magnetic assembly is completely covered with impregnating material, then, vacuum the complete assembly.	Sample
16	After vacuuming the impregnation, pour out the remaining impregnating material.	
17	Fill the magnetic assembly with vacuum-degassed embedment material. When the magnetic assembly is completely covered with the embedment material, then, vacuum the complete assembly.	Sample
18 19	Cure the embedment for 16 to 20 hours, at 94° C. Perform a final electrical test and visual inspection.	
20	Place in Bonded Stores	

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Table 3.13-3 Typical Parts List.

Parts List						Page 1
L1 Drawing Number 0001234						
Item No.	**Qty Reqd**	**Part Number**	**Specification**	**Nomenclature or Description**	**Material Specification**	**Material Supplier**
1	1	55059-A2		Molypermalloy Powder Core	Powder	Magnetics
2	AR		Mil-I-G31	Tape Mylar Film Non-Adhesive 1 mil	Mylar	Dupont
3	AR	No.1298		Tape Mylar Film Adhesive 3 mil		3M
4	AR	#30 AWG	ST12281-30	Magnet Wire Solderable 155° C	MW-80-C	MWS
5	AR	#33 AWG	ST12281-33	Magnet Wire Solderable 155° C	MW-80-C	MWS
6	AR	7500		Tape Dacron (3/8 inch, 5 mil)		Fralock
7	AR	No. 24	S1600	Flexible Fiberglass Sleeving	Fiberglass	Varflex
8	AR	280		Epoxy Impregnant	Epoxy	Scotchcast
9	AR	281		Epoxy Embedment	Filled-Epoxy	Scotchcast
10	AR		QQ-S-571	Solder, Type SN63	SN63, Type R	Kester
11	AR		Mil-W-22759	Stranded Wire, 26 AWG, Teflon	Clear	
12	1	1234		Fiberglass Cup	G10	Dorco

6.2 Parts and Materials

6.2.1 Material Selection. Parts and materials, exclusive of magnetic cores, shall be chosen from JPL, Standard STD00009.

6.2.2 Magnetic Core Selection.

6.2.2.1 Iron Alloy Core Configuration. There are several core configurations that have been proven to function well in space. A list of these core configurations is shown in Table 3.13-4.

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Table 3.13-4 Iron Alloy Core Configurations.

Magnetic Core Configuration *(Iron Alloy)			
Type	**Magnetic Material**	**Configuration**	**Reference**
Toroid	Iron Alloy (Tape)	This toroidal configuration puts a minimum of stress on the magnetic material. The core is placed in an aluminum case along with a damping compound. The case is then sealed and sprayed with epoxy paint.	Figure 3.13-7
Toroid	Iron Alloy (Tape)	This toroidal configuration is normally used in power applications where extreme high permeability is not a requirement.	Figure 3.13-8
Toroid	Iron Alloy (Powder)	Powder cores are pressed into shape, then, tumbled to remove the sharp corners. The cores are sprayed with epoxy paint to insulate the winding from the core. The main application for this type of core is filters.	Figure 3.13-9
C core	Iron Alloy (Tape)	C core type construction shall have all tapes epoxy-bonded together. This core configuration is normally used in power transformers and power inductors applications, where, 5000 plus, permeability is not a requirement.	Figure 3.13-10
*Iron alloy would include: nickel, cobalt, and amorphous materials.			

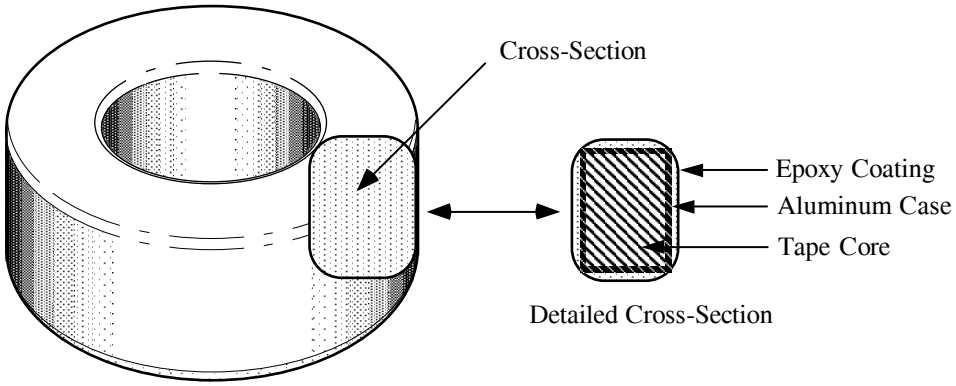

Figure 3.13-7 Epoxy-coated, Aluminum Case Toroidal Core.

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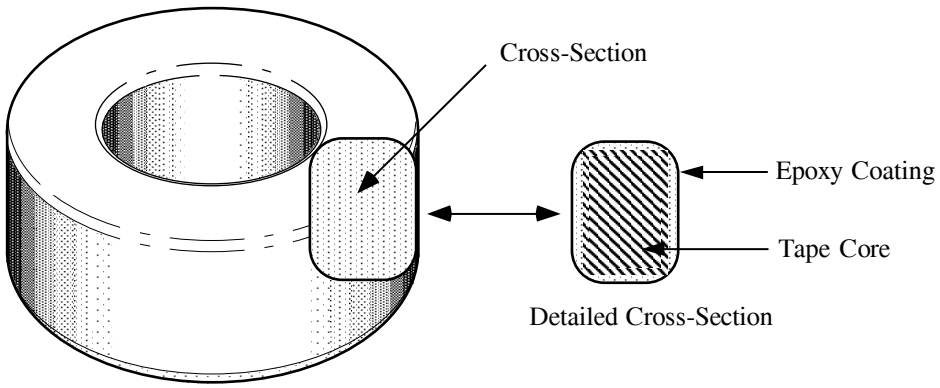

Figure 3.13-8 Epoxy-coated, Iron Alloy, Toroidal Core.

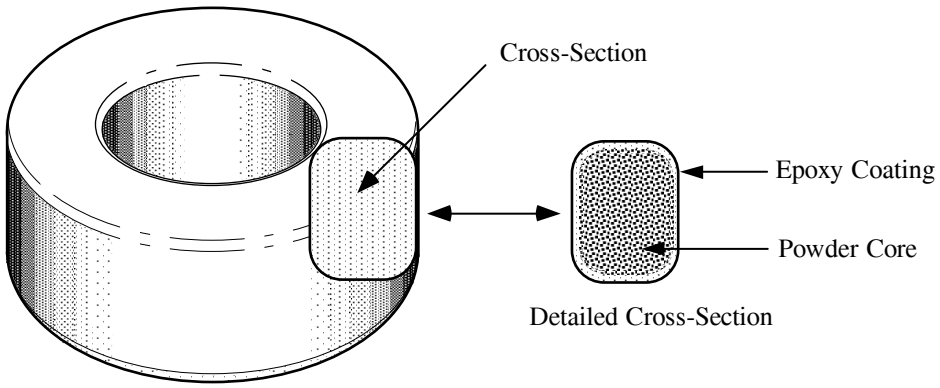

Figure 3.13-9 Epoxy-coated, Powdered Iron, Toroidal Core.

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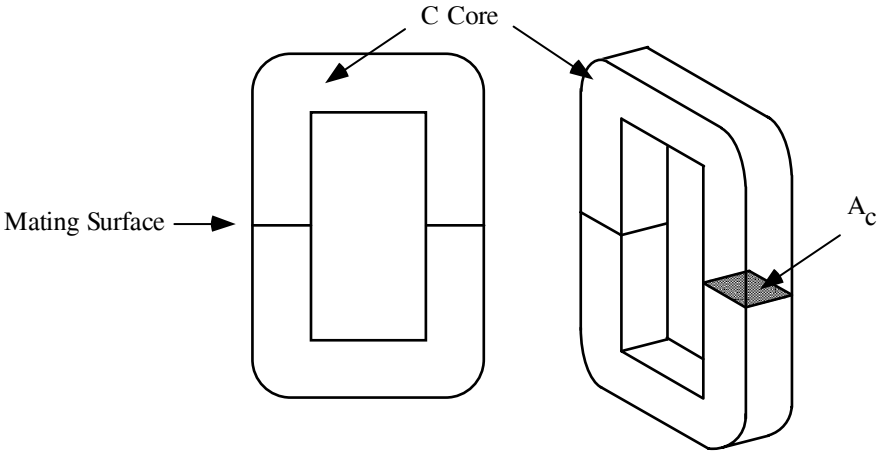

Figure 3.13-10 Epoxy Impregnated, Cut, C Core.

6.2.2.2 Ferrite Core Configuration. Ferrite cores are a ceramic material, similar to glass, and very brittle. They have a tendency to chip and/or break very easily. Ferrite cores have to be handled very carefully because of this. There are some cut, ferrite core configurations that are better suited for Hi-Rel space applications than others. A list of these core configurations is shown in Table 3.13-5. Each ferrite cut core shall be examined under a 12X magnification to verify the construction has no cracks at the corners, and at any other point that could be stressed during potting.

Table 3.13-5 Suggested Ferrite Core Types.

Magnetic Core Configuration (Ferrites)			
Type	**Magnetic Material**	**Configuration**	**Reference**
Toroid	Ferrite	Ferrite cores are pressed into shape, fired and then tumbled to remove the sharp corners. The cores are sprayed with epoxy paint to insulate the winding from the core. The typical permeability range for toroidal ferrites is 1200 to 15000.	Figure 3.13-11
E type core	Ferrite (Cut Core)	These core configurations are normally used in power transformers and power inductor applications where high permeability is not a requirement. Here is a list of core types that should function well, if care is taken when encapsulated: EE, EC, ETD, and EFD.	Figure 3.13-12 Figure 3.13-13 Figure 3.13-14 Figure 3.13-15

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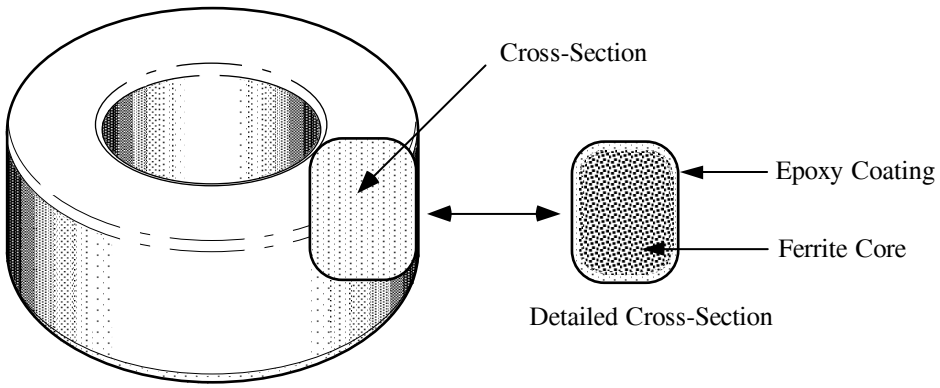

Figure 3.13-11 Epoxy-coated Ferrite Core.

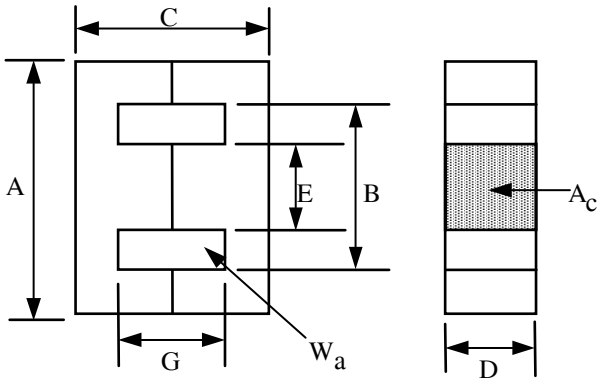

Figure 3.13-12 Ferrite EE Cut Core.

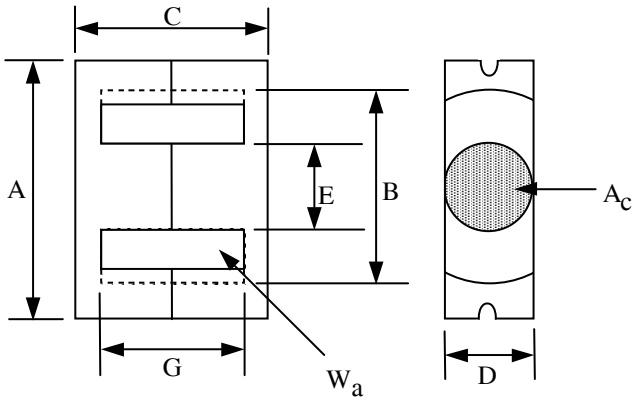

Figure 3.13-13 Ferrite EC, Cut Core.

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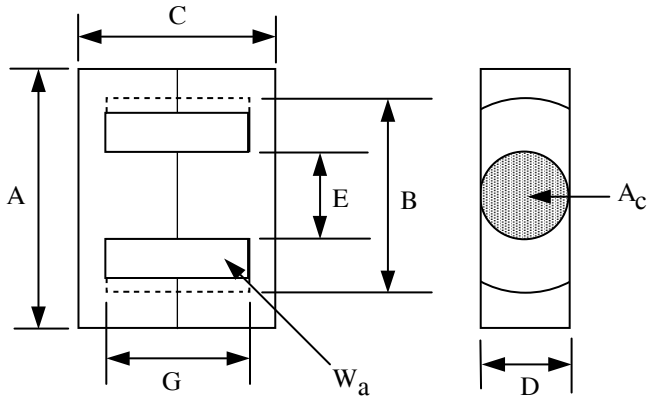

Figure 3.13-14 Ferrite ETD, Cut Core.

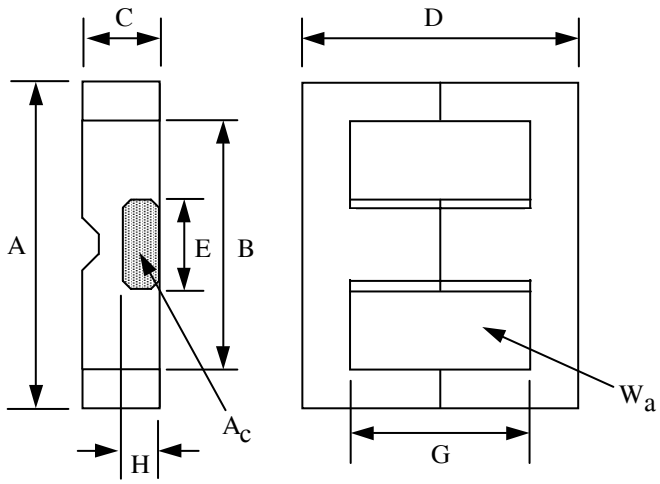

Figure 3.13-15 Ferrite EFD, Cut Core.

6.2.3 Brackets, Winding Tube and Bobbins. The bracket, when installed, shall fit snug and not put any lateral force on the magnetic core. The bobbin and winding tube shall provide adequate clearance to allow the core to be freely inserted without requiring force.

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6.2.4 Magnet Wire.

6.2.4.1 Wire Selection. Wire size and type shall be selected from JPL, standard ST10866, ST10219, ST11027, ST10865, ST10066, and ST12281, as shown in Table 3.13-6.

6.2.4.2 Preferred Magnet Wire. The preferred magnet wire is the solder-strippable, insulated, selected type ST12281, where 155 C (312 F) rating is acceptable.

6.2.4.3 Magnet Wire Size and Class. Magnet wire size and class shall be selected to provide for the maximum winding current, without exceeding the worst case, wire class temperature.

Table 3.13-6 Magnet Wire Insulation Guide.

Magnet Wire Insulation Guide				
Temperature Class	**JPL Specification**	**Insulation Type**	**Dielectric Constant**	**NEMA Standard MW 1000**
105 C	ST10066	Polyurethane*	6.20	MW-2-C
105 C	ST10065	Formvar	3.71	MW-19-C
130 C	ST10866	Polyurethane-Nylon*	6.20	MW-28-C
155 C	ST10219	Polyester		MW-5-C
155 C	ST12281	Polyurethane-155*	6.20	MW-79-C
180 C		Polyester Solderable*	3.95	MW-77-C
200 C	ST11027	Polyester-amid-imide	4.55	MW-35-C
220 C		Polyimide (ML)	3.90	MW-16-C
*Solderable insulations.				

6.3 Cut Core Assemblies

6.3.1 Banding Cores (Bands and Seals). Bands and seals for C type cores and coil assembly shall be selected from Table 3.13-7.

6.3.2 Core Mating Surface. The mating surface for gap and non gap cores, shall be coated with an adhesive, epoxy type, 3M EC2216, prior to banding. See Figure 3.13-16 and Table 3.13-13

6.3.3 Banding Material. Non gap cores shall be banded with solderable tin-plated, low-carbon steel bands. Gap cores shall be banded with phosphor bronze, banding material.

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6.3.4 Gapping Material. All cores, requiring an air gap, shall use Mylar or Kapton as the gapping material.

Table 3.13-7 C Core, Banding Data.

C Core Banding Data						
Core Dimensions (1 leg)		Band Size (Inch)	Bands Required	Seal Dimension (Inch)	*Banding Force	
A_{c_2} (cm^2)	D (cm)				(Pounds)	(kilograms)
1.21 or Less 1.21 to 2.42	Any 0.953 or Larger	0.188 x 0.006 0.375 x 0.006	1 1	0.188 x 0.25 0.375 x 0.375	37.5 75	17 34
2.42 to 4.84	0.953 to 3.81 4.13 or Larger	0.375 x 0.012 0.375 x 0.006	1 2	0.375 x 0.375 0.375 x 0.375	150 75	68 34
4.84 to 9.68	1.27 x 2.86 3.175 or Larger	0.375 x 0.012 0.375 x 0.012	1 2	0.375 x 0.375 0.375 x 0.375	150 150	68 68
*This force must be reduced from 30% to 50% when banding nickel-iron or supermendur cores.						

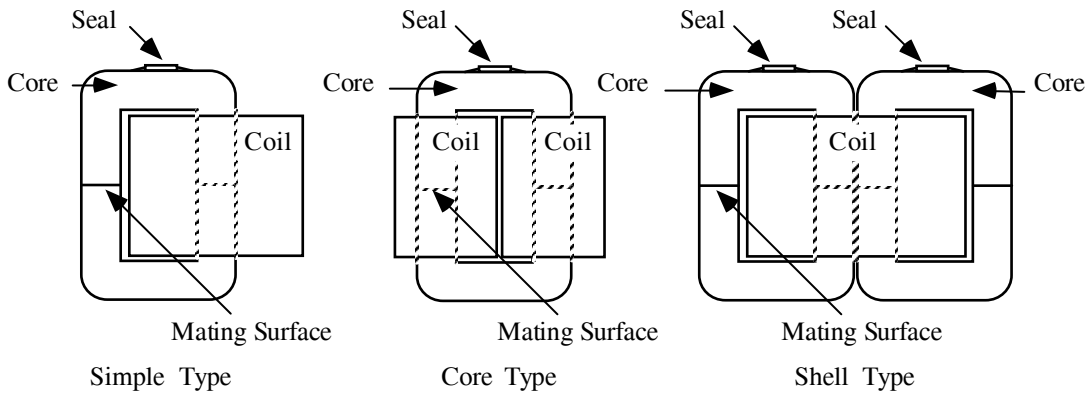

Figure 3.13-16 Typical C Core Configurations.

6.3.5 Banding Evenly Spaced. The bands shall be evenly spaced around the core, as shown in Figure 3.13-17.

6.3.6 Staggered Seals. If the design requires two bands, then the seals shall be staggered, as shown in Figure 3.13-17.

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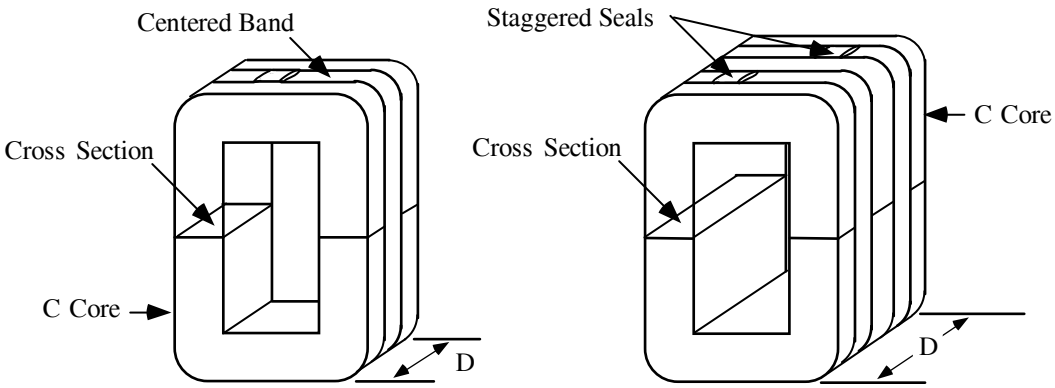

Figure 3.13-17 C Core, Banding Location.

6.3.7 High Temperature Seals. Magnetic devices designed to operate at temperatures above 177 C (350 F), shall have band seals soldered with Sn5, Sn10, or Sn96 high-temperature solder, conforming to QQ-S-571.

6.4 Removing the Enamel

6.4.1 Magnet Wire Stripping. The enamel on magnet wire can be stripped in many ways: 1. Solder pot can be used for tinning when special solderable insulations are used. 2. Abrasive fiberglass wheels are used to perform the stripping. 3. The removal of enamel insulation can be done with flame by charring the enamel, then, using an emery paper to clean. 4. Chemicals are used for stripping enamel wire. They are very toxic and cumbersome to use and are not recommended for use in space. See Figure 3.13-18.

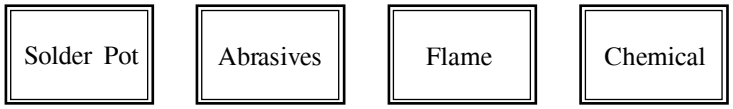

Figure 3.13-18 Methods Used to Remove Enamel from Magnet Wire.

6.4.2 Chemical Wire Stripping. To strip insulation from magnet wire by the use of chemicals, a step-by-step procedure must be submitted and approved, before starting. Stripping insulation, with the use of chemicals, will only be approved if there is not another way.

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6.5 Windings

6.5.1 Toroidal Windings.

6.5.1.1 Toroid Core Taping. All toroids, including tape cores, powder cores, and ferrites, shall have the core wrapped with Mylar polyester, prior to winding. The tape shall be either adhesive-coated, or if uncoated, the ends shall be secured with adhesive coated tape. See Figure 3.13-19.

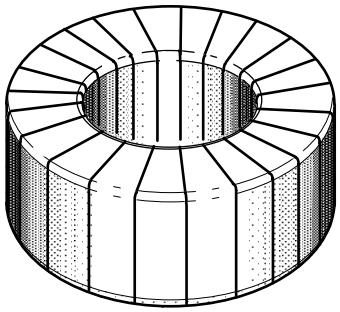

Figure 3.13-19 Mylar-Wrapped, Toroidal Core.

6.5.1.2 Intermediate Wire Leads. Magnetic devices, wound with AWG 33 or smaller wire sizes, shall be joined with an intermediate lead per Table 3.13-8.

Table 3.13-8 Intermediate Lead Wire Size.

Intermediate Lead	
Magnet Wire Size AWG	**Intermediate Wire Size**
#32 and larger	None
#33 to #40	#26
#41 and smaller	#32

6.5.1.3 Woven Glass Sleeving. Place unimpregnated, woven glass sleeving over all leads from AWG 24 to AWG 33, coming from the magnetic devices, as shown in Figures 3.13-20 and 3.13-21.

6.5.1.4 Toroid Start Lead. The Toroid, Starting Lead shall be fabricated, as shown in Figure 3.13-21.

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6.5.1.5 Toroid Self-Finish Lead. Toroid Self-Finish Lead shall be fabricated, as shown in Figure 3.13-22.

6.5.1.6 Toroid Self-Tapping Lead. Toroid Self-Tapping Lead shall be fabricated, as shown in Fgures 3.13-23 and 3.13-24.

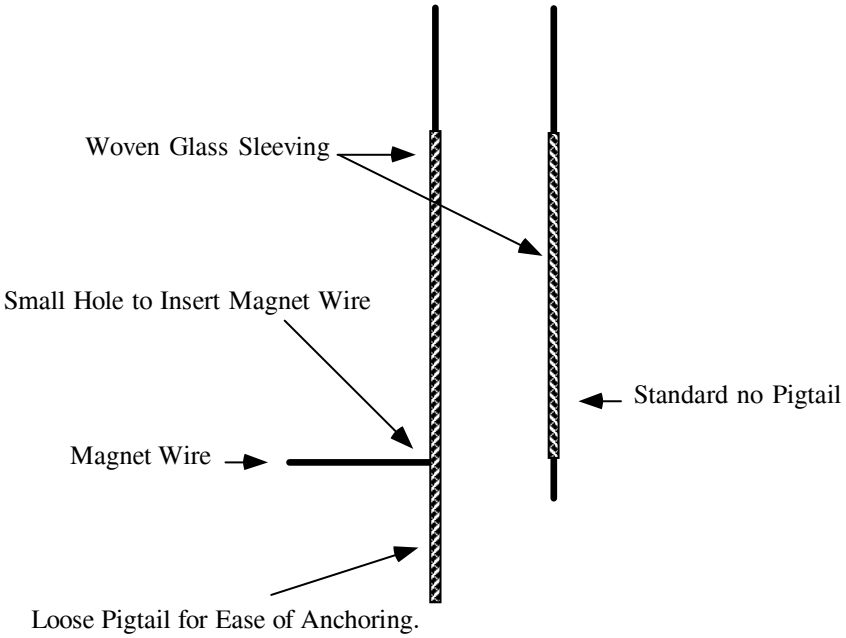

Figure 3.13-20 Magnet Wire Lead with Woven Glass Sleeving.

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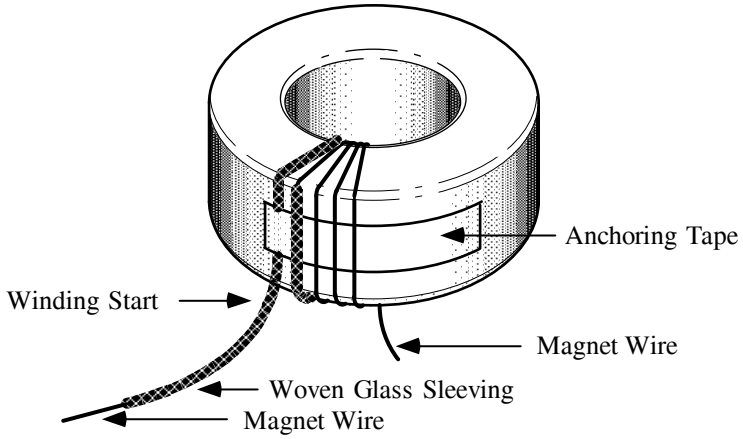

Figure 3.13-21 Toroid, Self-start Lead with Woven Glass Sleeving.

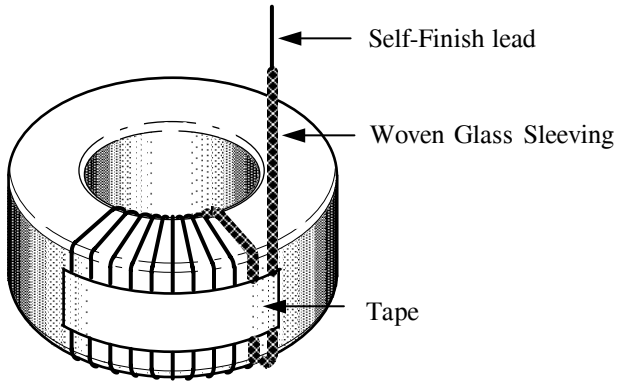

Figure 3.13-22 Toroid, Self-finished Lead with Woven Glass Sleeving.

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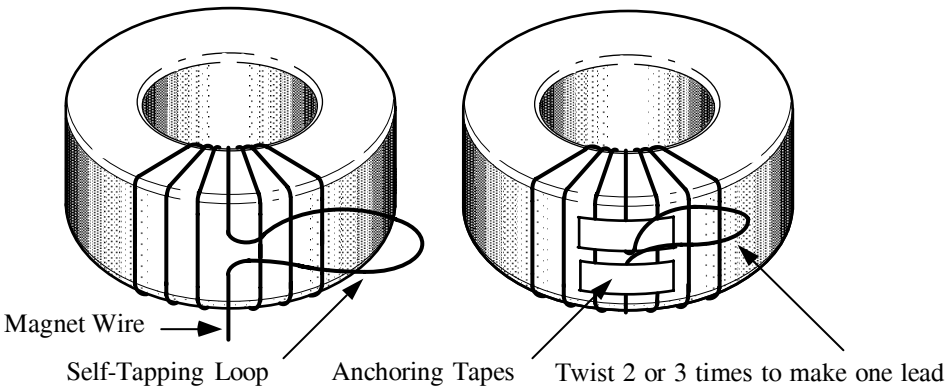

Figure 3.13-23 Breakout Loop for Self-Tapping Lead.

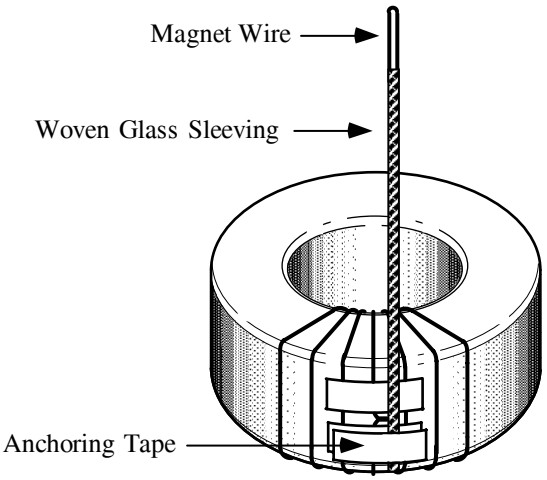

Figure 3.13-24 Breakout Loop with Woven Glass Sleeving.

6.5.1.7 Strain Relief Loop. A Strain Relief Loop shall be provided for all spliced lead breakouts, as shown in Figure 3.13-26.

6.5.1.8 Bend Radii. The wire Bend Radii shall be greater than five times the wire diameter, except for one-time bends around terminals and wire splices.

6.5.1.9 Winding Tension. The Winding Tension used in winding shall be the minimum required to pull the wire into position.

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6.5.1.10 Wire Lay. The Wire Lay shall be smooth and uniform, unless otherwise required by the detailed winding instructions.

6.5.1.11 Splice I. Splice I and solder joints are prohibited within the winding. All splicing, including the interim leads, must be placed on the periphery toroid after it is wound, See Figures 3.13-25, through 3.13-28.

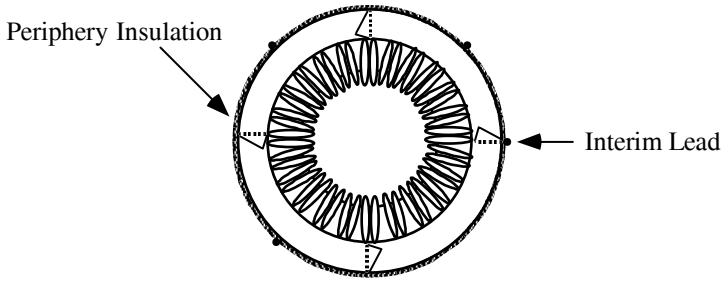

Figure 3.13-25 Finishing the Interim Lead.

6.5.1.12 Splice II. Splicing II shall not be made because of a broken wire. If a winding has a broken wire, then, the entire winding shall be replaced. The only winding splice that can be made is if the toroidal winding shuttle does not hold enough wire for the required number of turns.

6.5.1.13 External Toroid Lead (vertical). The External interim lead wire shall be fabricated, as shown in Figures 3.13-26 and 3.13-27.

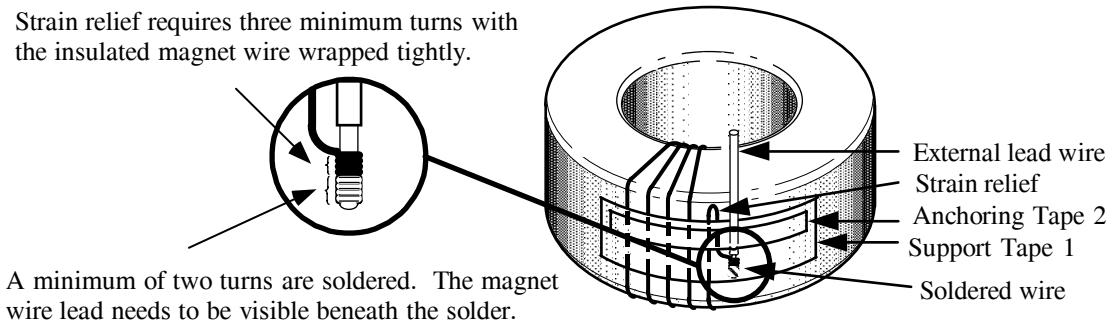

Figure 3.13-26 Soldering the Interim Lead.

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6.5.1.14 Finished External Toroid Lead (Vertical). The external interim lead wire shall be finished, as shown in Figure 3.13-27.

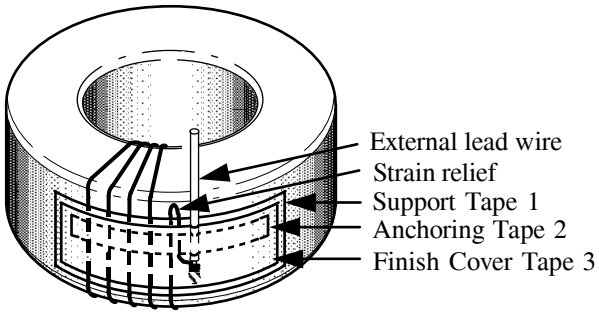

Figure 3.13-27 Finished, Vertical Interim lead.

6.5.1.15 External Toroid Lead (Horizontal). The External Interim Lead Wire shall be fabricated, as shown in Figure 3.13-28.

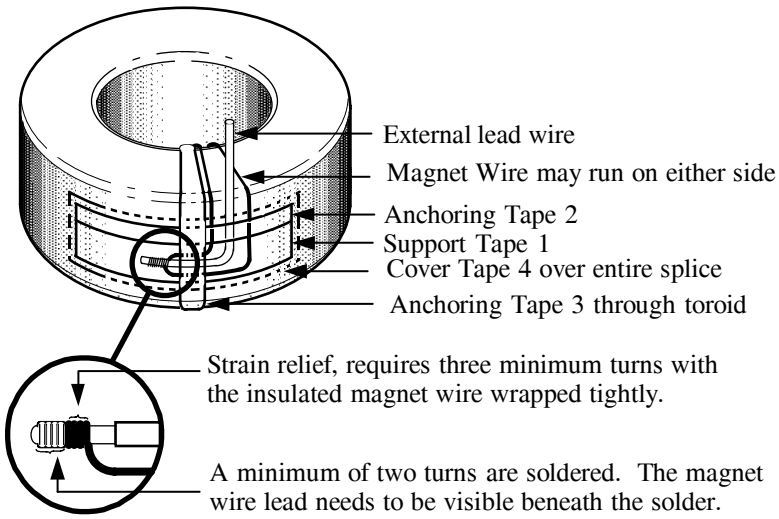

Figure 3.13-28 Finished, Horizontal Interim lead.

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6.5.2 Bobbin Windings.

6.5.2.1 No-Slot Bobbins. Bobbins, with no slots in the end plates, shall have the lead wires taped in place with the tape covering, the end plate, and 1/8 of the coil winding length with approved tape, as shown in Figure 3.13-29.

6.5.2.2 Interlayer Insulation. Bobbin interlayer insulation shall be held in place with an approved tape, and meet the requirements of the assembly drawing, as shown in Figure 3.13-30.

6.5.2.3 Tap Leads. Tap leads in bobbin windings shall be insulated from the windings, with an approved tape, both over and under the lead, as shown in Figure 3.13-31.

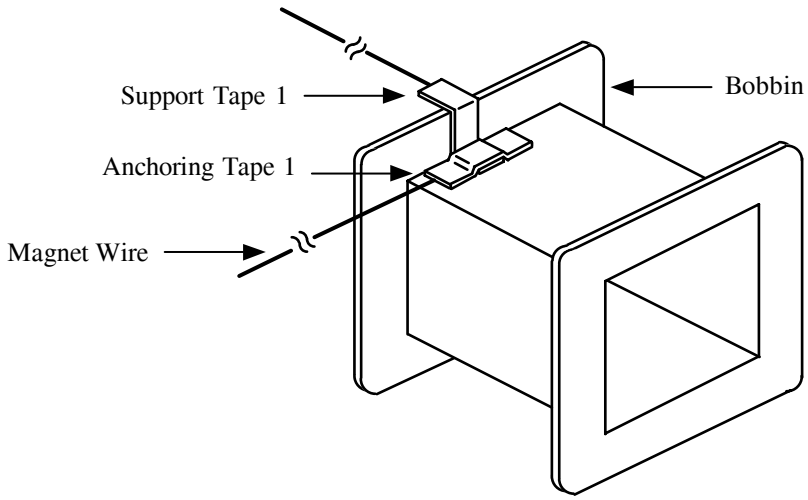

Figure 3.13-29 Start Lead on a Non-Slot Bobbin.

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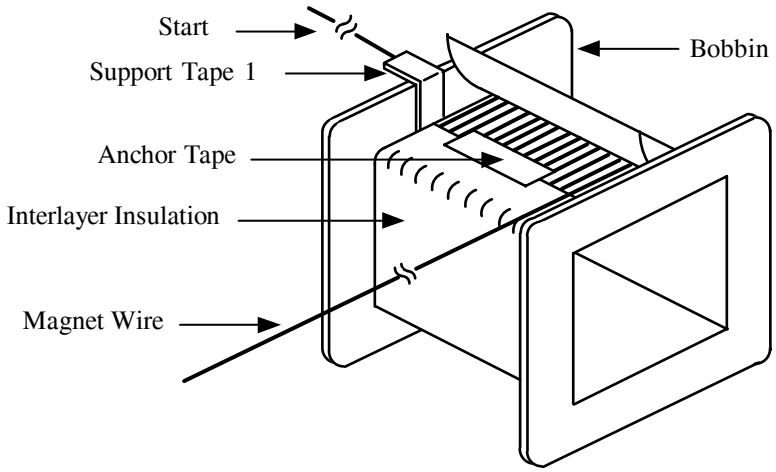

Figure 3.13-30 Applying the Interlayer, Insulation, and Taping.

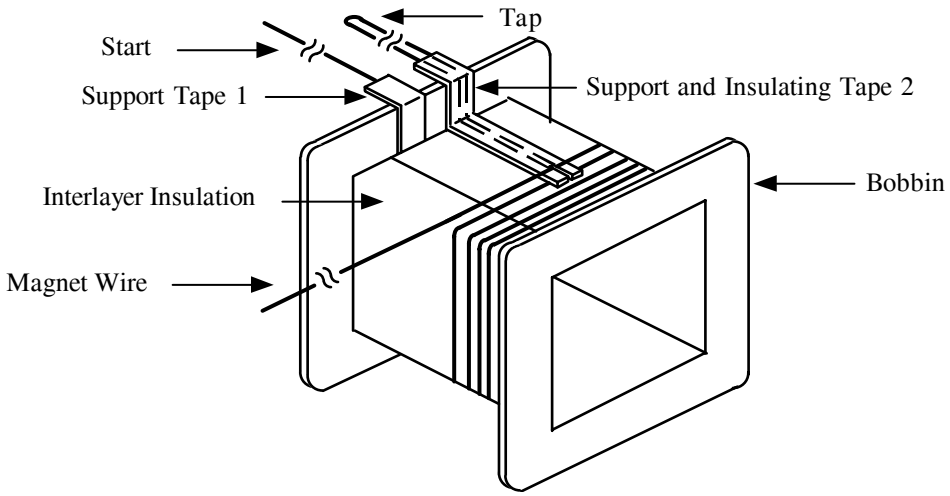

Figure 3.13-31 Insulating the Tap Lead.

6.5.2.4 Slotted Bobbins. Bobbins, with slots in the end plates, shall have the lead wires sleeved with woven glass sleeving, as shown in Figure 3.13-32.

6.5.2.5 Interlayer Insulation. Bobbin interlayer insulation shall be held in place with an approved tape, and meet the requirements of the assembly drawing, as shown in Figure 3.13-33.

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6.5.2.6 Slotted Bobbins with Tap Leads. Slotted bobbins, with tap leads using woven glass sleeving, shall be installed, as shown in Figure 3.13-34.

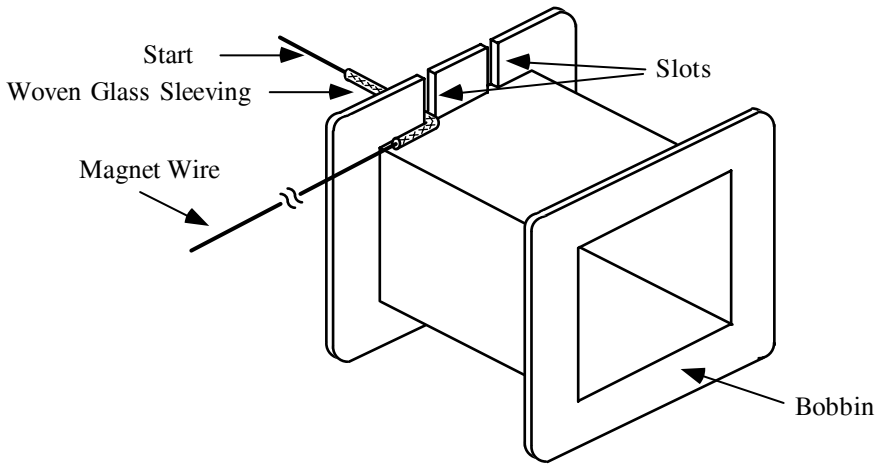

Figure 3.13-32 Start Lead on a Slotted Bobbin, using Woven Glass Sleeving.

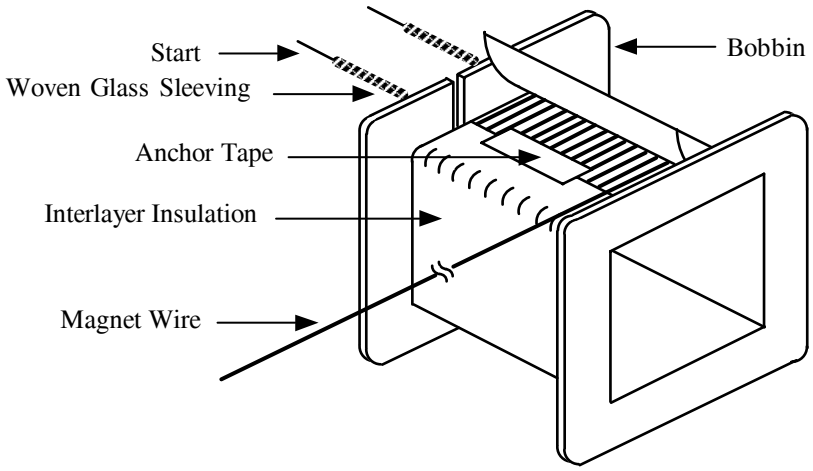

Figure 3.13-33 Applying the Interlayer Insulation and Taping.

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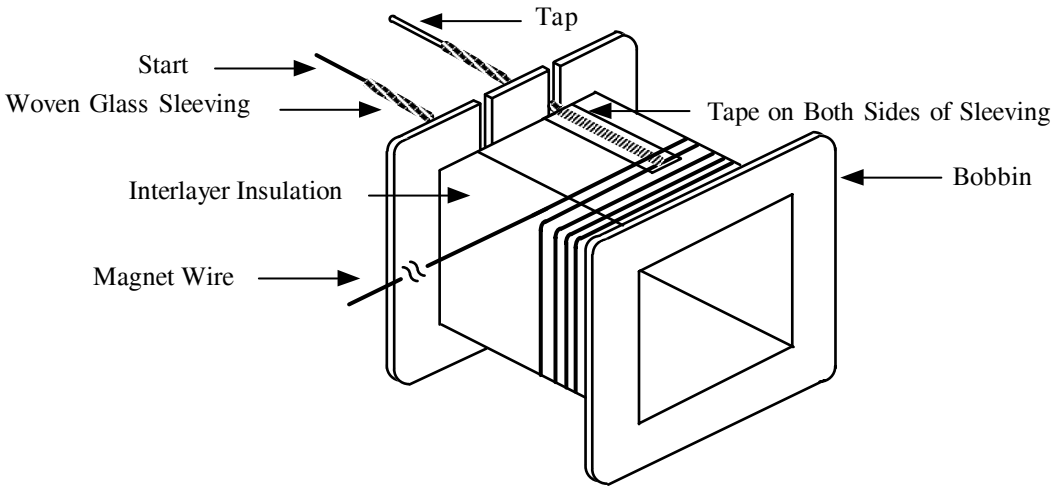

Figure 3.13-34 Insulating the Tap Lead with Woven Glass Sleeving.

6.5.3 Tube Layer Windings.

6.5.3.1 Start Leads Anchor Tapes. Anchor tapes for start leads are shown on tube type windings. See Figure 3.13-35.

6.5.3.2 Start Leads with Woven Glass Sleeving. Starting leads are shown using woven glass sleeving. See Figure 3.13-36.

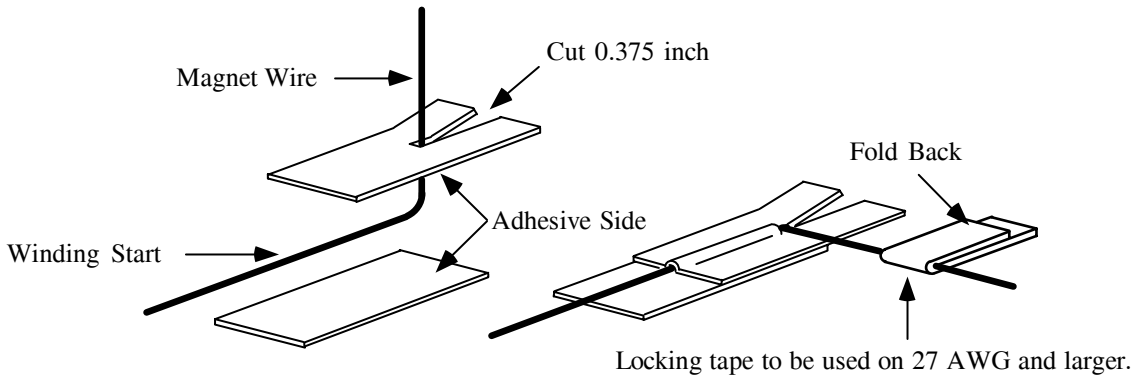

Figure 3.13-35 Layer Winding Start Lead using Tape.

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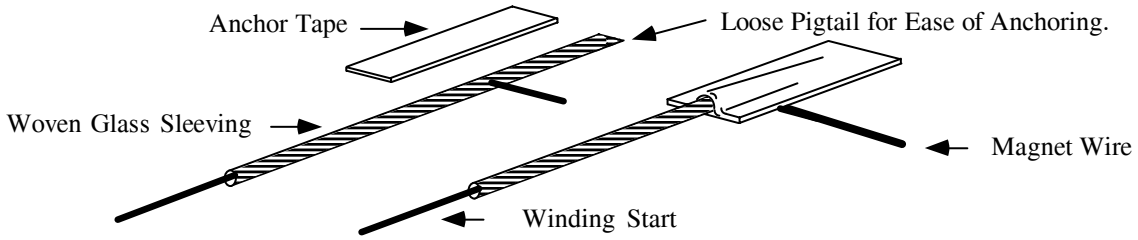

Figure 3.13-36 Layer Winding Start Lead using Woven Glass Sleeving.

6.5.3.3 Start Lead using Tape. Applying the start lead, using tape, is shown in Figures 3.13-37, 3.13-38, and 3.13-39.

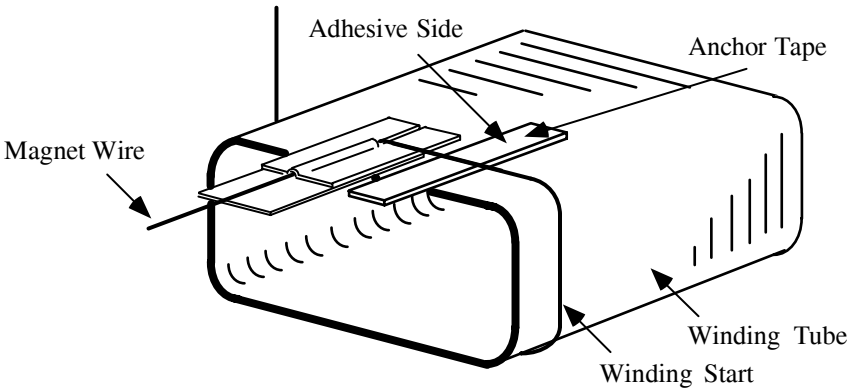

Figure 3.13-37 Step 1, for the Start Lead, Using Tape.

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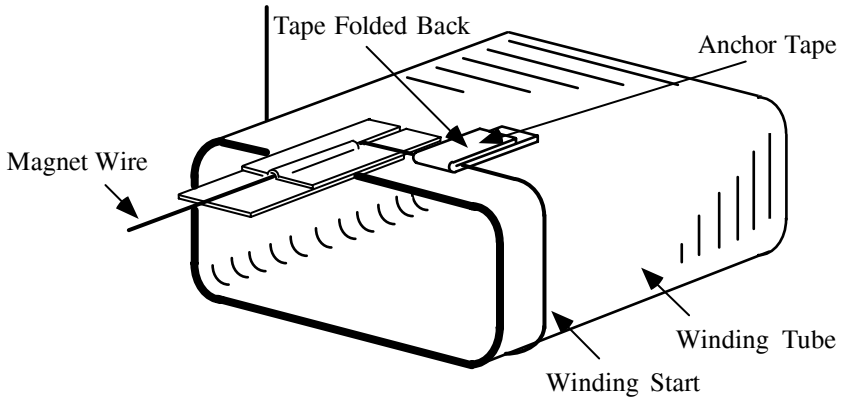

Figure 3.13-38 Step 2, for the Start Lead, for Folding the Anchor Tape.

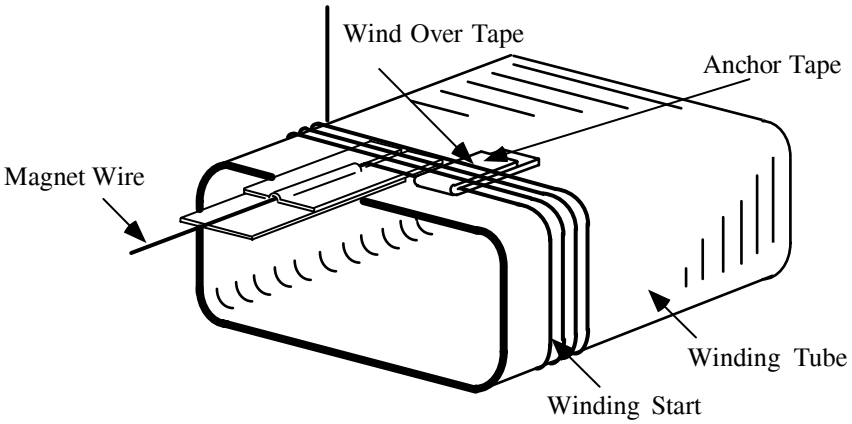

Figure 3.13-39 Step 3, for the Start for Lead, Locking the Anchor Tape.

6.5.3.4 Start Lead for Using Woven Glass Sleeving. Applying the start lead, using woven glass sleeving, is shown in Figures 3.13-40, 3.13-41, and 3.13-42.

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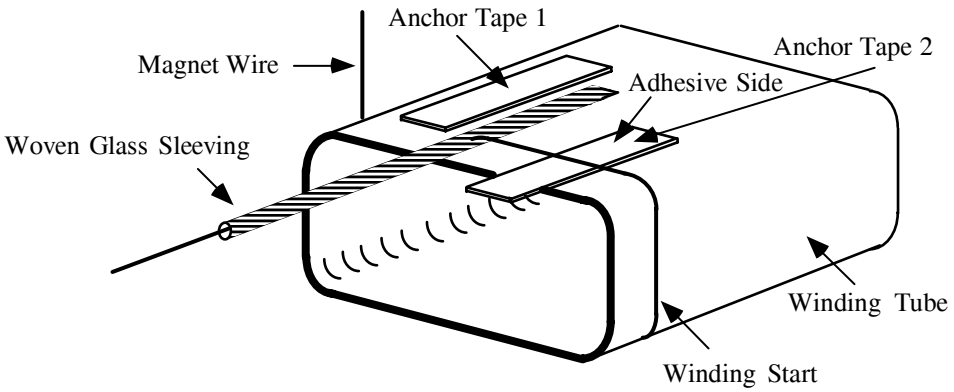

Figure 3.13-40 Step 1, for the Start Lead, Using Woven Glass Sleeving.

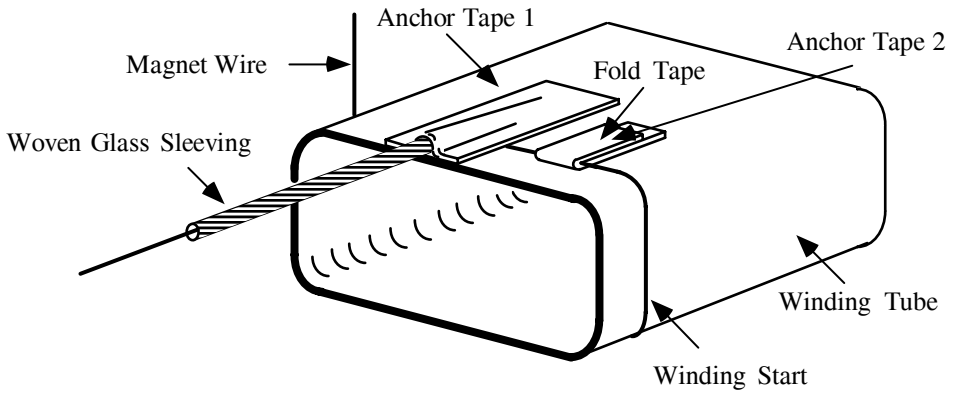

Figure 3.13-41 Step 2, for the Start Lead, for Folding the Anchor Tape.

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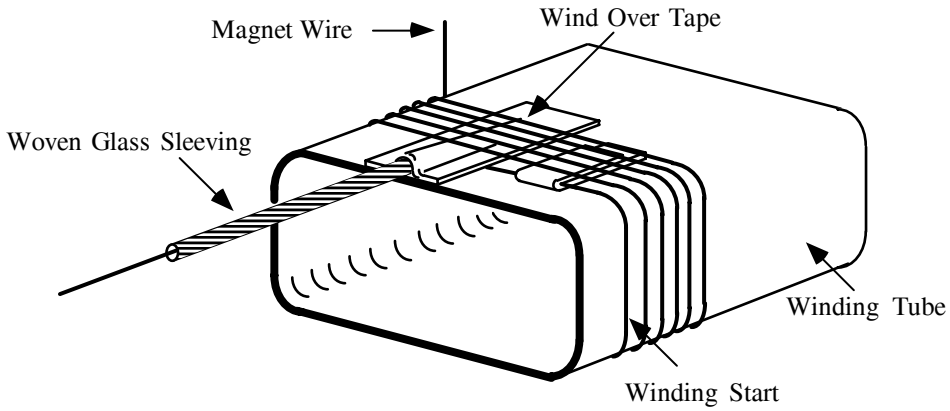

Figure 3.13-42 Step 3, for the Start Lead, for Locking the Anchor Tape.

6.5.3.5 Interlayer Insulation. Interlayer Insulation shall be held in place with an approved tape and meet the requirements of the assembly drawing, as shown in Figure 3.13-43 for tape, and Figure 3.13-44 for woven glass sleeving.

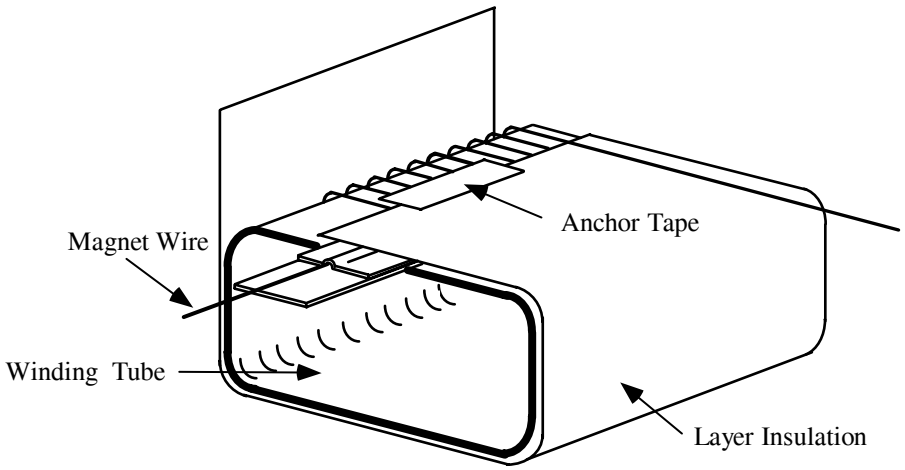

Figure 3.13-43 Applying the Interlayer Insulation and Taping.

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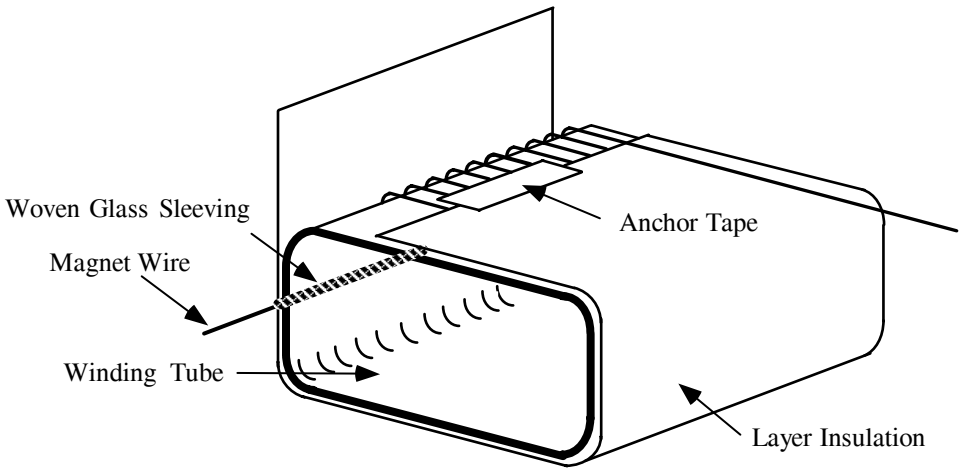

Figure 3.13-44 Applying the Interlayer Insulation and Taping.

6.5.3.6 Tap Leads Using Tape. Tap leads in a tube windings shall be insulated from the windings, using an approved tape. Tape over and under the tap lead, as shown in Figures 3.13-45, 3.13-46, and 3.13-47.

6.5.3.7 Tap Leads Using Woven Glass Sleeving. Tap leads in a tube windings shall be insulated from the windings using an approved tape. Tape over and under the sleeving, as shown in Figures 3.13-48, 3.13-49, and 3.13-50.

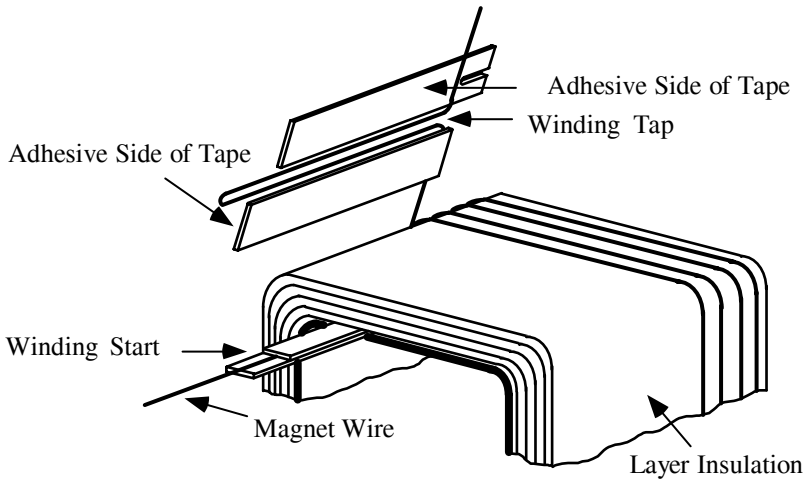

Figure 3.13-45 Tap Lead: Step 1, Showing the Exploded View.

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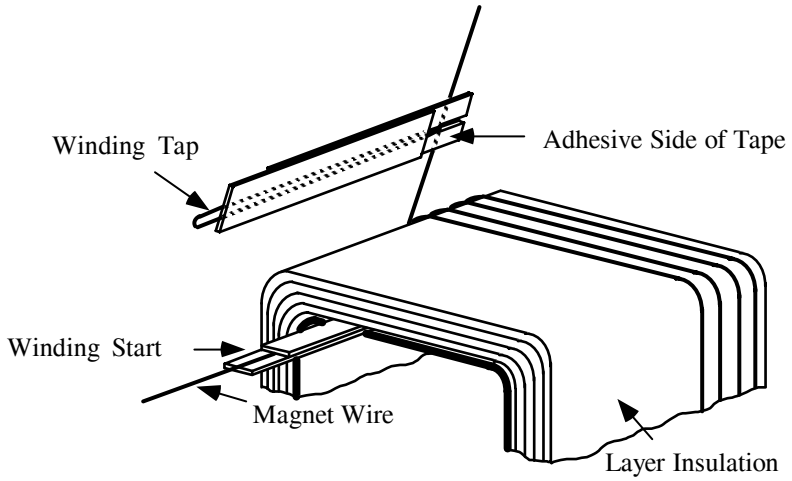

Figure 3.13-46 Tap Lead: Step 2, Showing the Compressed View.

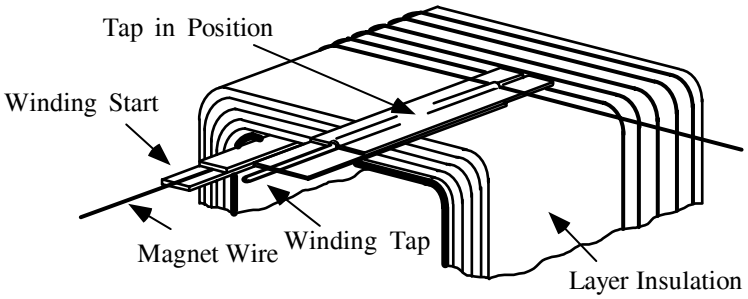

Figure 3.13-47 Tap Lead: Step 3, Showing the Tap Lead in Place.

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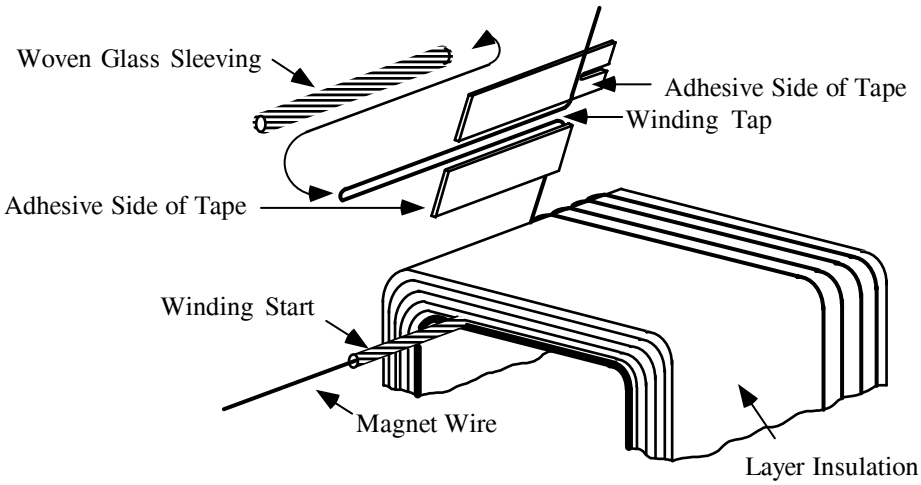

Figure 3.13-48 Tap Lead: Step 1, Showing the Exploded View, Using Sleeving.

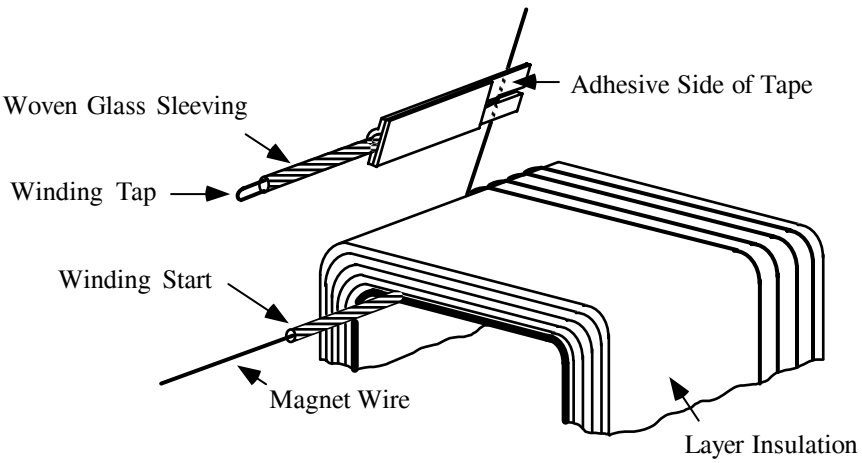

Figure 3.13-49 Tap Lead: Step 2, Showing the Compressed View, Using Sleeving.

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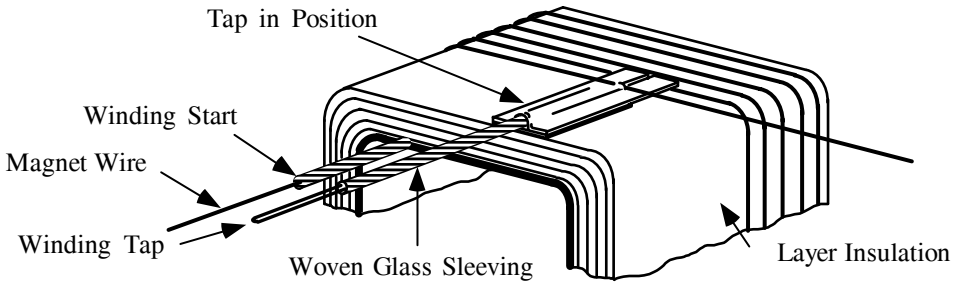

Figure 3.13-50 Tap Lead: Step 3, Showing the Tap Lead in Place, Using Sleeving.

6.5.3.8 Crossover Tap Leads Using Tape. Tap leads in a layer windings shall be insulated from the windings, using an approved tape. Tape over and under the tap lead, as shown in Figure 3.13-51.

6.5.3.9 Crossover Tap Leads Using Woven Glass Sleeving. Tap leads in a tube windings shall be insulated from the windings, using an approved tape. Tape over and under the sleeving, as shown in Figure 3.13-52.

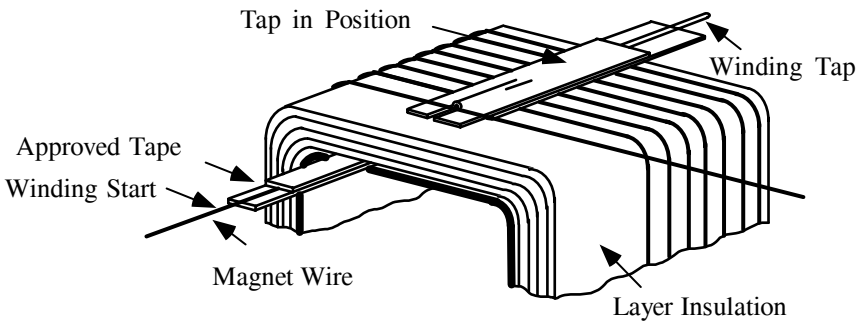

Figure 3.13-51 Tap Lead Crossing Over a Winding.

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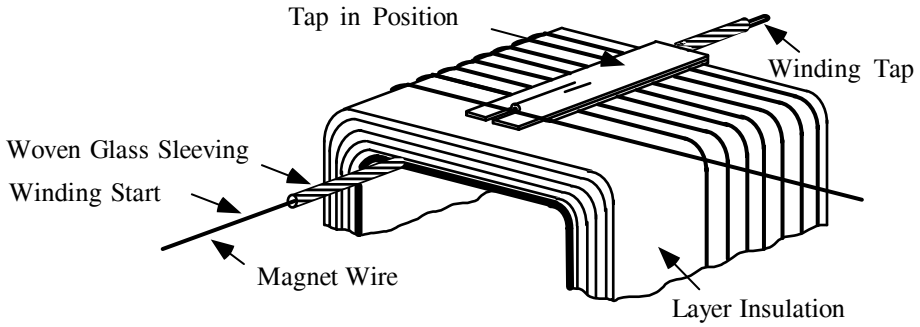

Figure 3.13-52 Tap Lead Crossing Over a Winding, Using Sleeving.

6.5.3.10 Parallel and Bifilar Windings. The start of a parallel winding shall be treated as a single magnet wire without crossovers, as shown in Figures 3.13-55 and 3.13-56. The start of a bifilar winding shall be treated as a separate magnet wire. Parallel wires can be brought out together. Bifilar wires have to be brought out separately. Multifilar windings can be brought out with a combination of both. Parallel and bifilar windings shall be wound during fabrication, as shown in Figures 3.13-53, 3.13-54, 3.13-55, and 3.13-56.

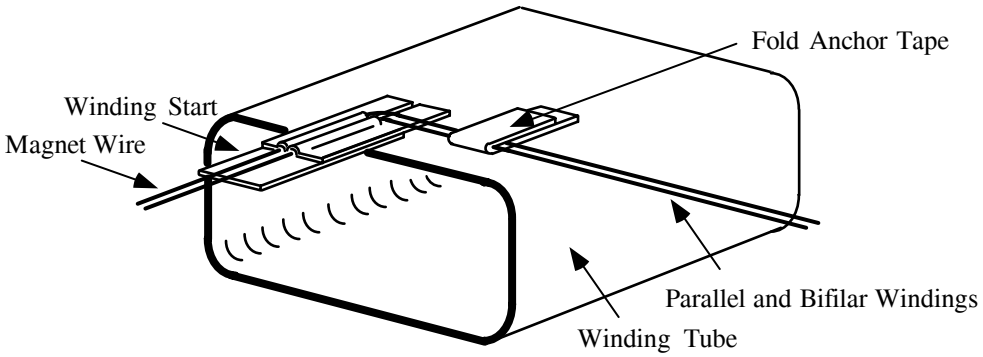

Figure 3.13-53 Start Lead Positioning for Parallel and Bifilar Windings, Using Tape.

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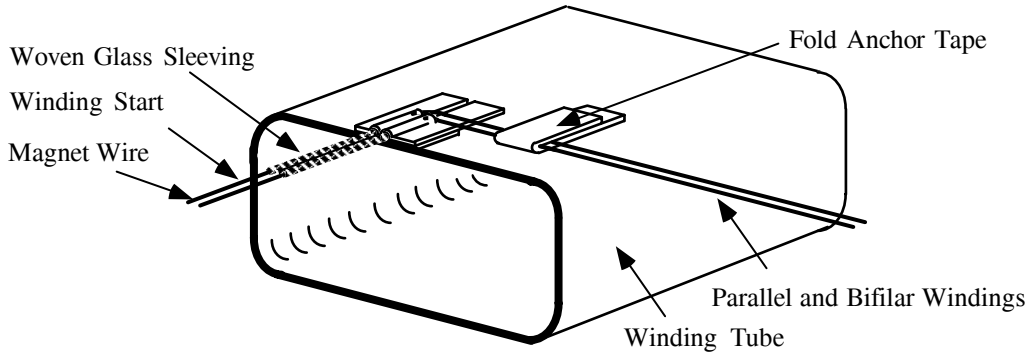

Figure 3.13-54 Start Lead Positioning for Parallel and Bifilar Windings, Using Sleeving.

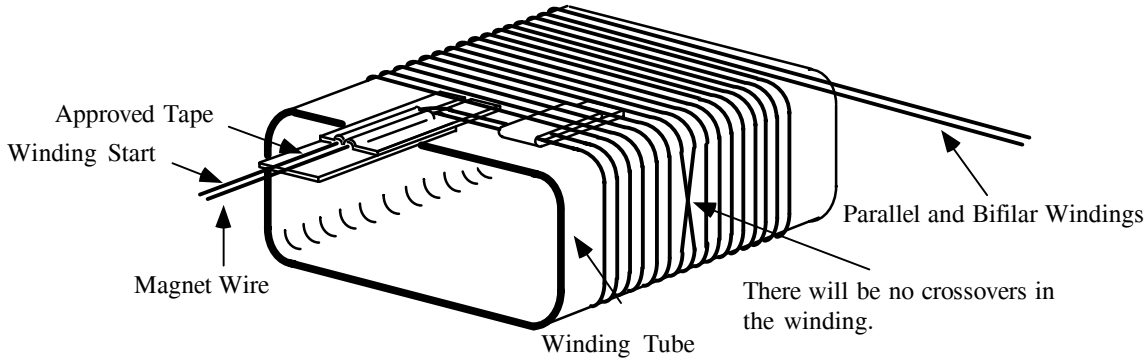

Figure 3.13-55 Parallel and Bifilar Windings shall not have Crossovers, Using Tape.

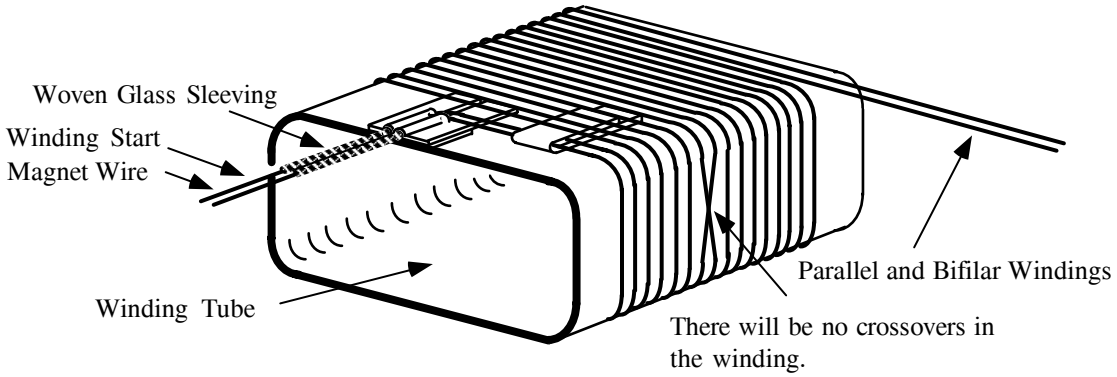

Figure 3.13-56 Parallel and Bifilar Windings shall not have Crossovers, Using Sleeving.

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6.5.3.11 Wrapper Insulation. The wrapper insulation will be the same width as the interlayer insulation, as shown in Figure 3.13-57. The anchor tape will secure the wrapper.

6.5.3.12 Completed Coil. This is a view of a finish layer, wound coil ready for the next assembly procedure. Note A: Any of the leads closer than 0.09 inches, or 0.23 cm to the inside of the coil, shall be insulated by tape, or approved, woven, glass sleeving. See Figure 3.13-57.

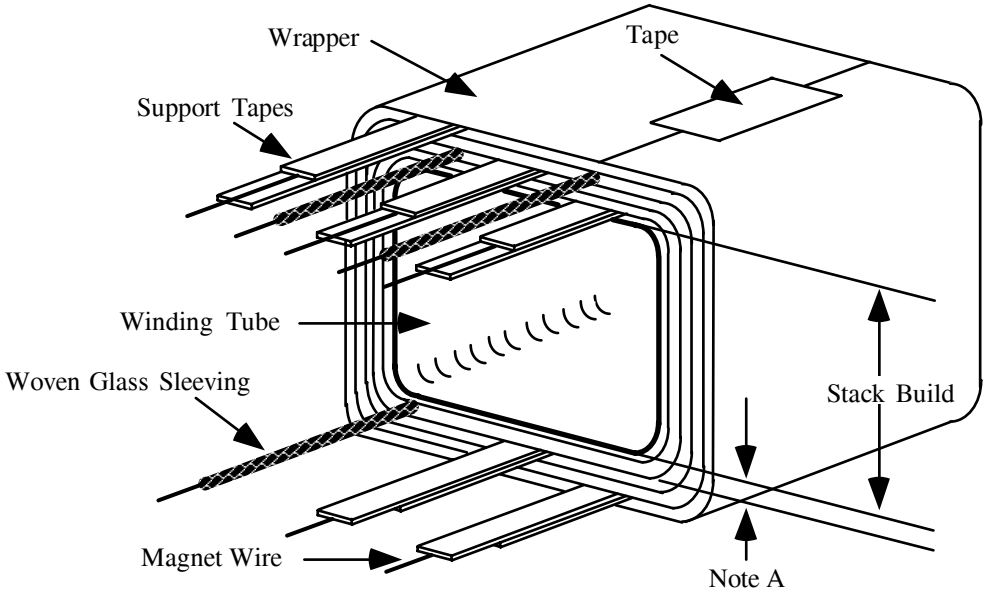

Figure 3.13-57 Completed Layer, Wound Coil Assembly.

6.5.4 Electrostatic Shield.

6.5.4.1 Foil Material. Foil shall be inspected to be sure there are no slitting burrs, as shown in Figure 3.13-58.

6.5.4.2 Exiting Leads. All exiting leads, starts, taps, and finishes will be sweat-soldered to the foil. The exiting lead or foil will make contact to, at least, 70 to 80% of the copper foil. There will be no solder-wicking at the solder joint, as shown in Figure 3.13-59.

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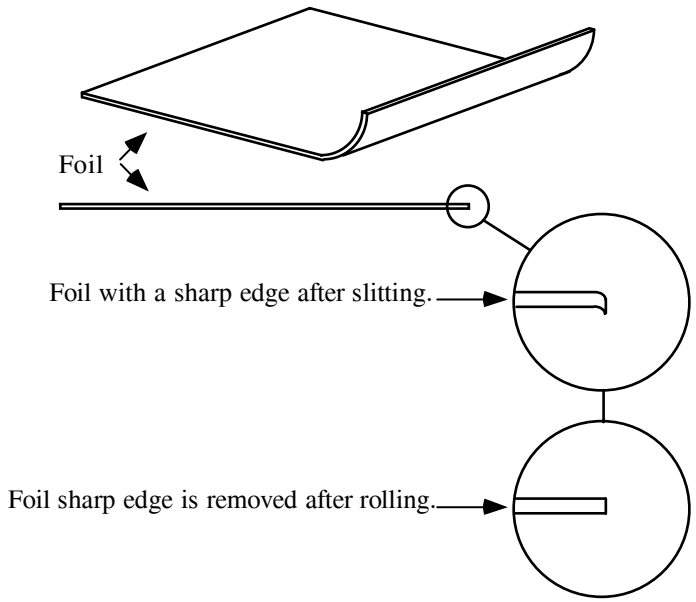

Figure 3.13-58 Copper Foil with the burr removed after rolling.

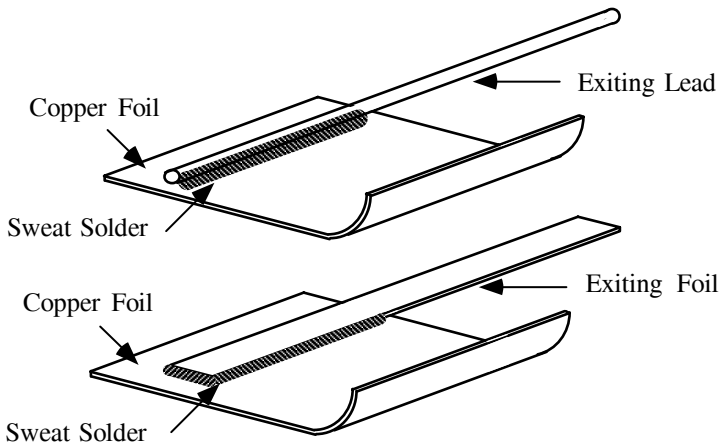

Figure 3.13-59 Attaching the Lead to the Copper Foil.

6.5.4.3 Electrostatic Shield (Faraday Shield). The electrostatic shield (copper foil) must cover the complete winding. There shall be insulation material to cover both sides of the electrostatic shield. There shall be insulating material to overlap the start of the

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electrostatic shield. The lead that is soldered to the electrostatic shield must be soldered to the center or at an equal distance from each end. The application of the electrostatic shield is shown in Figure 3.13-60 for the bobbin, and Figure 3.13-61, for the tube layer winding type.

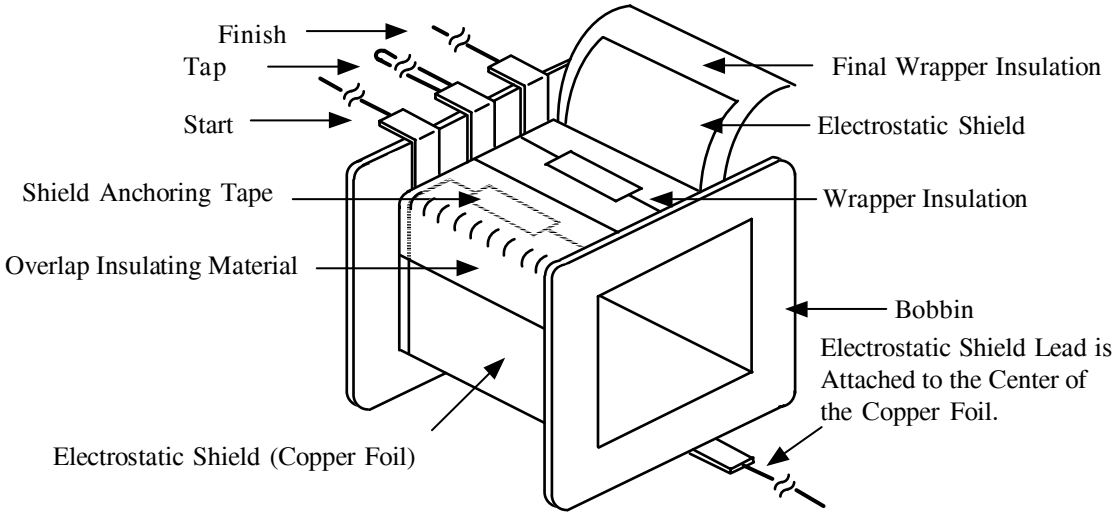

Figure 3.13-60 Bobbin Winding, with an Electrostatic Shield.

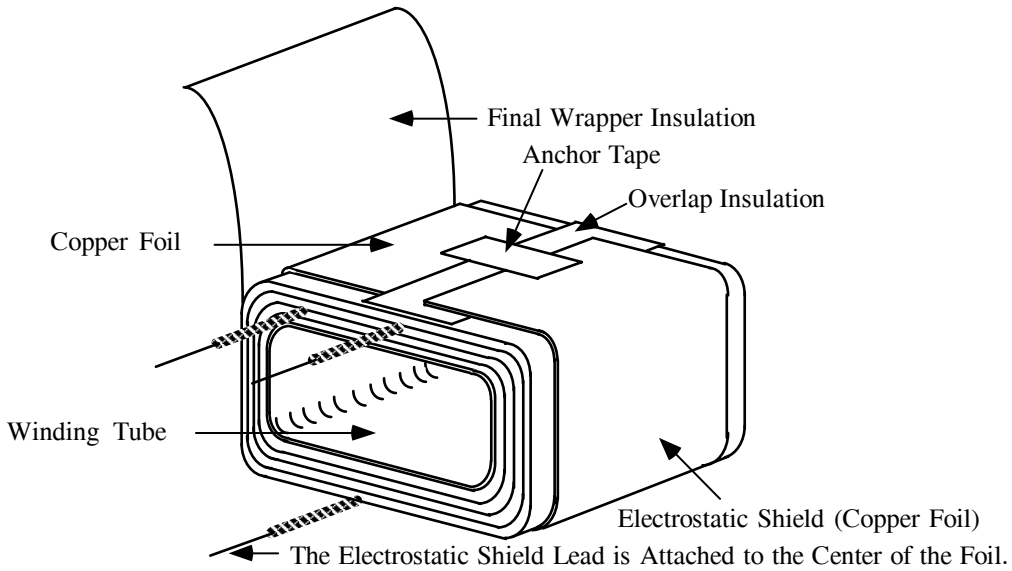

Figure 3.13-61 Tube Winding, with an Electrostatic Shield.

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6.5.5 Foil Wound Coils.

6.5.5.1 Start Lead. The anchor tape shall overlap the start lead completely, as shown in Figure 3.13-62.

6.5.5.2 Interlayer Insulation. The anchor tape for the insulation shall not overlap the foil, as shown in Figure 3.13-63. The interlayer insulation shall overlap the edge of the foil, but not extend beyond, the edge of the winding tube. The angle view of Figure 3.13-63 is shown in Figure 3.13-64.

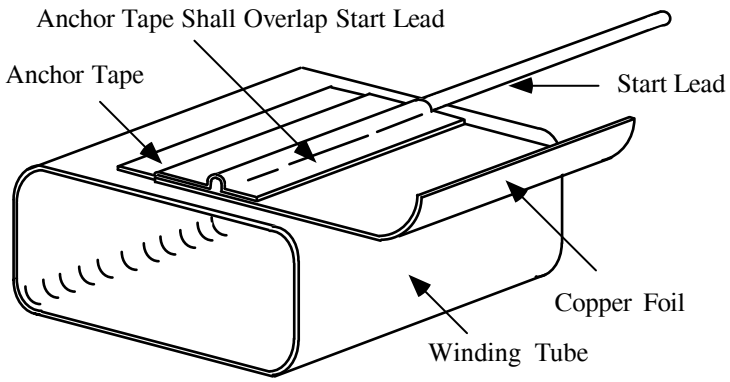

Figure 3.13-62 Anchor Tape Overlaps the Start Lead.

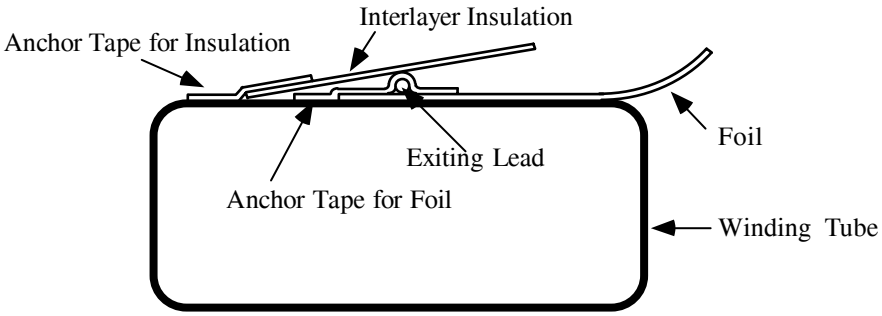

Figure 3.13-63 Attaching the Insulation to the Winding Tube.

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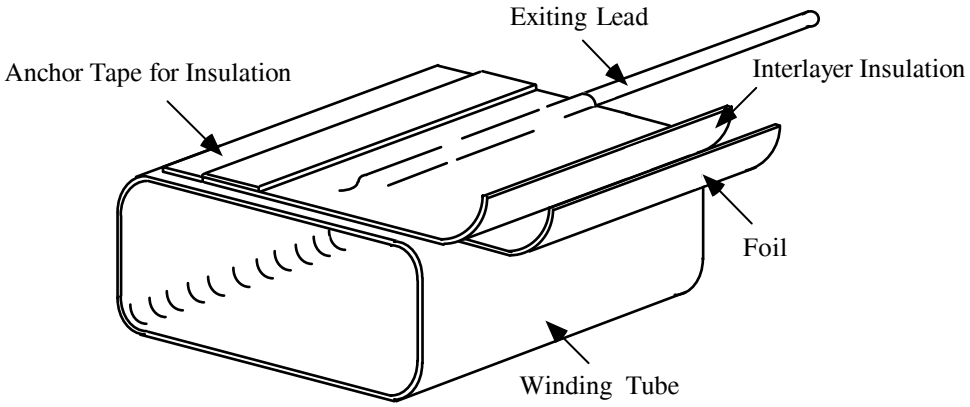

Figure 3.13-64 Attaching the Lead to the Copper Foil.

6.5.5.3 Tap Lead. The anchor tape shall overlap the tap lead completely, as shown in Figure 3.13-65. Before the application of the anchor tape, the exiting lead will be inspected for solder wicking or sharp points at the surface solder joint.

6.5.5.4 Finish Lead. The anchor tape shall overlap the finish lead completely, as shown in Figure 3.13-66. Before the application of the anchor tape, the exiting lead will be inspected for solder wicking or sharp points at the surface solder joint.

6.5.5.5 Wrapper Insulation. The wrapper insulation will be the same width as the interlayer insulation, as shown in Figure 3.13-67. The anchor tape will secure the wrapper.

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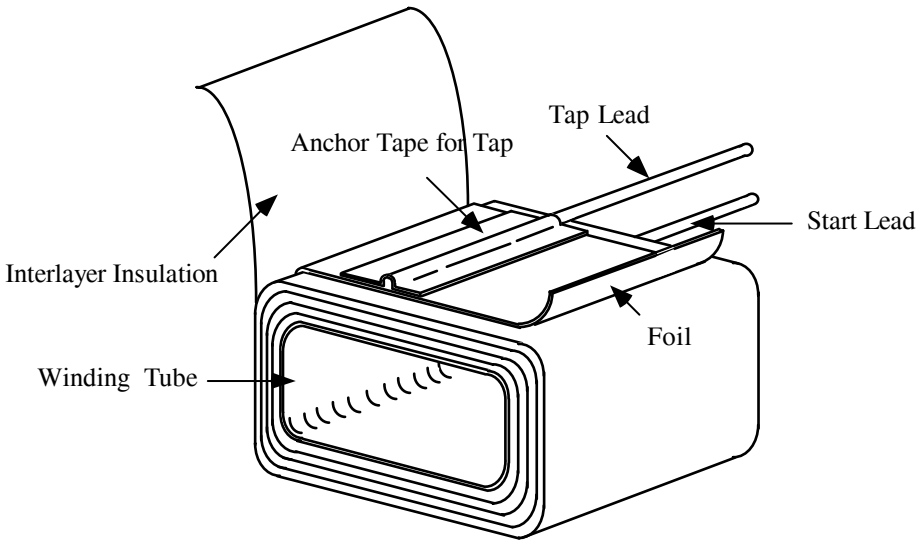

Figure 3.13-65 The Anchor Tape Overlaps the Tap Lead.

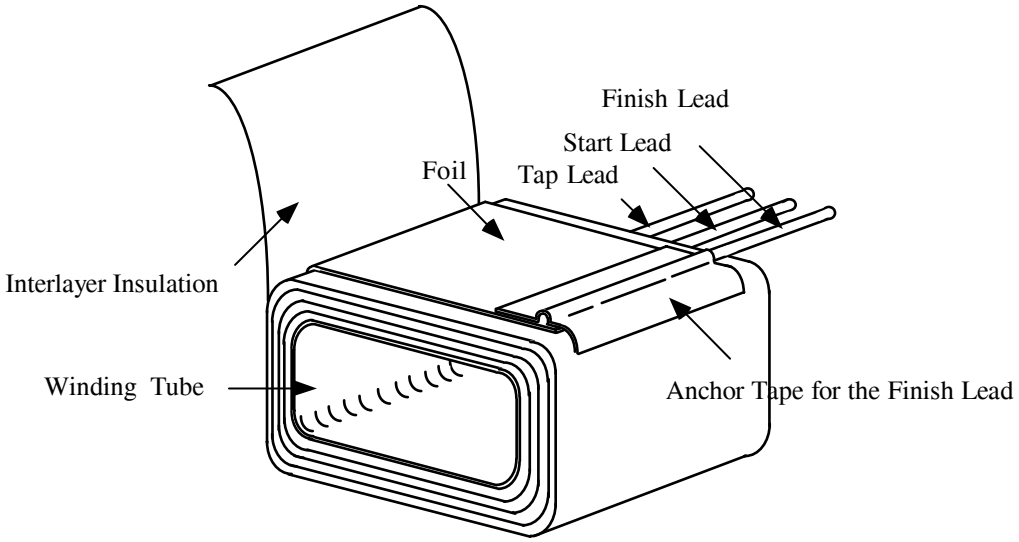

Figure 3.13-66 The Anchor Tape Overlaps the Finish Lead.

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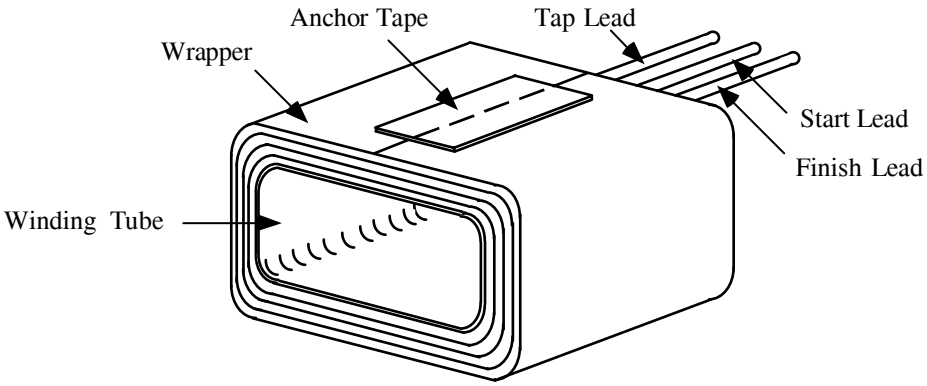

Figure 3.13-67 Finished Foil Winding with a Wrapper.

6.6 Wire Insulation Stripping and Tinning

6.6.1 Magnet Wire.

6.6.1.1 Magnet Wire Solder Pot. A typical solder pot for tinning solderable magnet wire is shown in Figure 3.13-68. The solder pot shall have a molten solder capacity of at least one Pound (453.6 grams) minimum. The solder used shall be SN63 from a solid bar, with a composition, that is shown in Table 3.13-9. The solder post capacity shall be maintained to, at least, 90%. The solder pot temperature shall be controlled at 260 C +/-20 C (500 F +/-25 F). It is measured below the solder surface and near the center of the solder mass, away from the walls. The solder pot shall have sufficient quantity to minimize the temperature drop of the molten solder, when dip tinning. Prior to dip soldering, the Dross* on the solder surface shall be removed using a stainless steel paddle. When the solder composition exceeds the contamination levels of Table 3.13-9, the solder shall be discarded and replaced with fresh solder. Records shall be maintained to ensure solder pot conforms with solder, temperature, and contamination. Solder pots shall be grounded with a resistance of less than 2 ohms from case to local ground.

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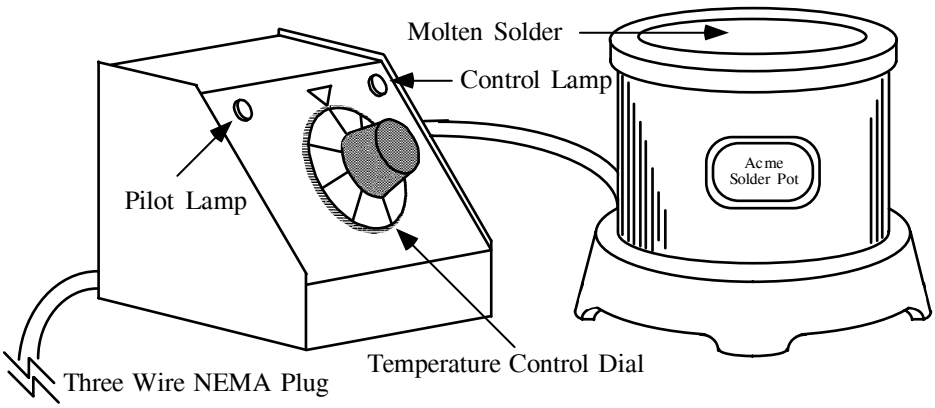

Figure 3.13-68 Typical Temperature Controlled Solder Pot.

Table 3.13-9 Typical SN63 Solder Impurities.

SN63 Solder		
Elements	**Basic Elements Limits (%)**	**Impurity Limits Maximum (%)**
Tin	60-65	
Aluminum		0.01
Antimony		1
Bismuth		1
Cadmium		0.01
Copper		0.5
Gold		0.2
Iron		0.02
Magnesium		0.01
Sulfur		0.02
Zinc		0.01
*Others		0.1
Lead		Remainder
*Total of all others (except lead remainder)		

*Dross: Oxide and other contaminants, which form on the surface of molten solder.

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6.6.1.2 Magnet Wire Using Flame. The removal of enamel insulation on magnet wire, having a diameter 0.295mm (0.016 inches 30AWG) or smaller, can be done with a flame, using an alcohol burner as shown in Figure 3.13-69. After the insulation has been blackened, the magnet wire should be immediately quenched in water to regain temper. Emery paper can now be applied to the blackened area on the magnet wire to remove the black residue left from burning. After the magnet wire has been cleaned and inspected, the wire is ready to be tinned.

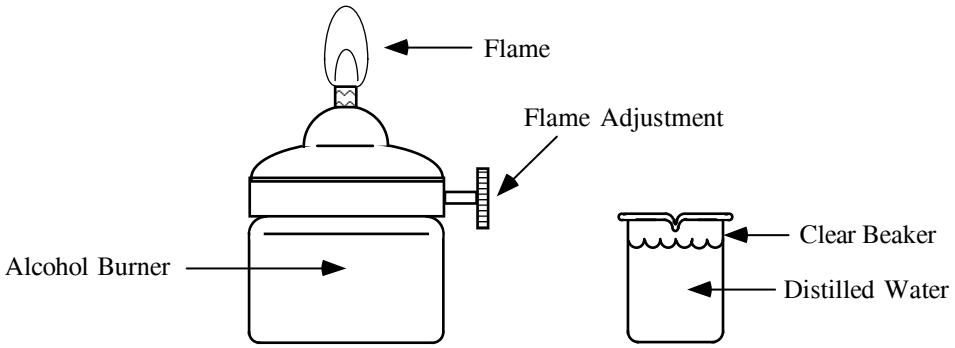

Figure 3.13-69 Typical Alcohol Burner, with Distilled Water for Quenching.

6.6.1.3 Magnet Wire Using Abrasive Wheels. Abrasive rotating wheels of fiberglass material are used to remove the magnet wire insulation, as shown in Figure 3.13-70. The fiberglass material in the wheels wipes away the insulation, thus leaving the magnet wire clean and polished. The cone type of fiberglass strippers, shown in Figure 3.13-70A, is normally for fine magnet wire (30-45 AWG), and the round fiberglass wheels, shown in Figure 3.13-70B, are normally for medium magnet wire (15-30 AWG). It is necessary to choose the correct wheel type and grade (roughness) for the gauge of wire and insulation type to be stripped. If the abrasive wheels are not adjusted with the proper tension, it will lead to grabbing and breaking of the magnet wire. The abrasive wheels shall always be adjusted, using the sample, same gauge wires, prior to being used on the flight coils.

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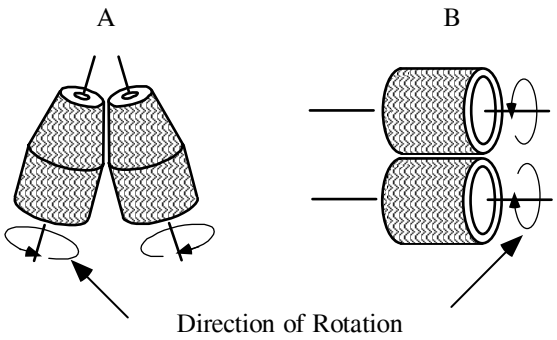

Figure 3.13-70 Typical Abrasive, Magnet Wire Strippers.

Any of the above wire stripping methods requires skilled operators. There has to be a written, complete, and thorough procedure for whichever of the above wire stripping methods is used. The operator must be capable of fine-tuning the equipment and then, be able to demonstrate the performance.

6.6.2 Stranded Wire Stripping.

6.6.2.1 Stranded Hookup Wire. The wire used for breakout leads shall be a stranded, hookup wire per JPL Specification ZPH-2239-0940. The insulation shall be 600 volt, unpigmented, bondable virgin TFE. For stranded hookup wire, per JPL Design Standards, see Table 3.13-10.

Table 3.13-10 JPL, Design Standard Hookup Wire.

JPL, Hookup Wire	
AWG	**Design Specification**
16	ST11478-16ET
18	ST11478-18ET
20	ST11478-20ET
22	ST11478-22ET
24	ST11478-24ET
26	ST11478-26ET

6.6.2.2 Wire Stripping. Using an approved wire stripper strip, approximately 0.2 inch (0.5 cm) of insulation from the wire to be tinned, remove any tag, or icicles ends of wire insulation as shown in Figure 3.13-71, using a pair of flush cutters or clippers.

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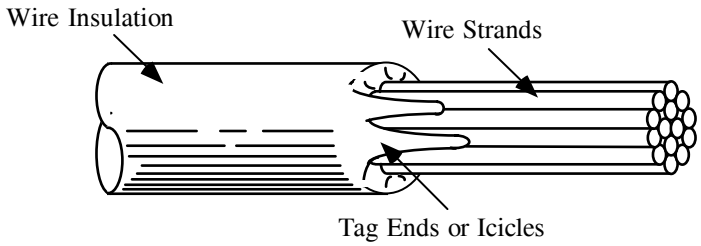

Figure 3.13-71 Stripped, Insulated Stranded Wire with Icicles.

If the lay of the outer wire strands has been disturbed, restore the lay by twisting the strands in the direction of the original lay. Do not handle the strands with bare fingers. Use either gloves, finger cots, or the equivalent. Do not over twist the strands, as this tends to increase the outer diameter of the conductor and may prevent insertion of the tinned wire into the bifurcated terminal. Do not attempt to restore the lay of the wires that have disturbed inner strands. Cut off the length containing the disturbed inner strands and restrip the wire. Reject wires with nicked or broken strands.

6.6.2.3 Thermal and Mechanical Wire Strippers. Only approved thermal or mechanical wire strippers will be used. A typical thermal wire stripper is shown in Figure 3.13-72 and a mechanical stripper is shown in Figure 3.13-73. Mechanical strippers require finer adjustment to get the performance without having cuts, nicks or a broken serve as shown in Figure 3.13-82.

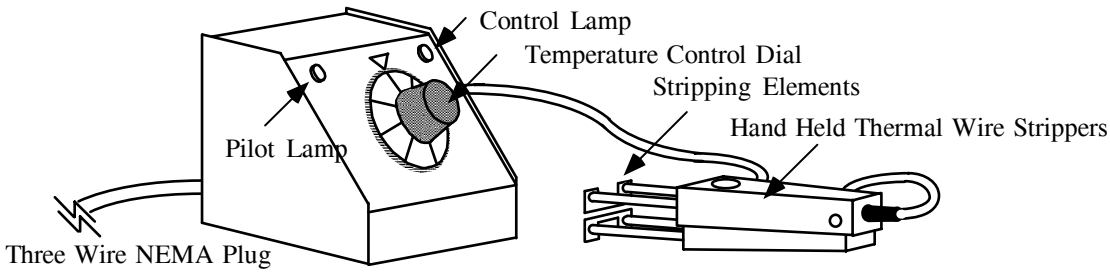

Figure 3.13-72 Typical, Thermal Wire Strippers.

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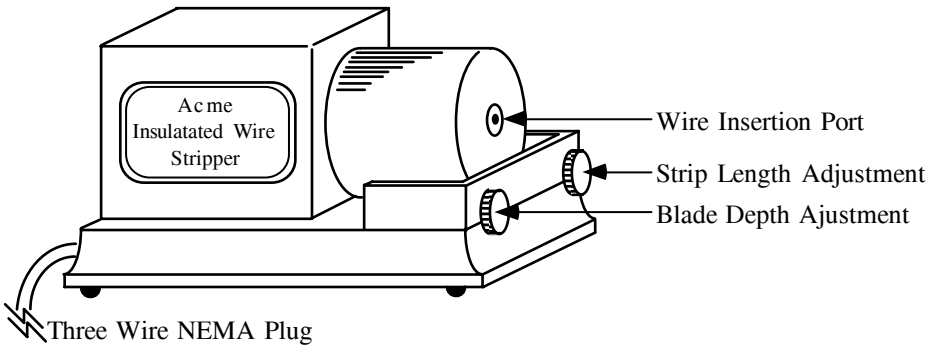

Figure 3.13-73 Typical, Mechanical Wire Stripper.

6.6.2.4 Thermal and Mechanical Stripping Damage. The damage to wires caused by the insulation stripping process is restricted as follows:

a. Stranded conductors shall not have cracked or severed strands.

b. The conductor insulation shall not be punctured, crushed, or otherwise damaged to such an extent that the wire could not pass the dielectric acceptance requirement of the wire. The ends of the insulation shall be cut square and clean except for a few remaining fibrous strands. Do not bend the conductor strands for the purpose of removing excess fibrous strands.

c. The conductor strands shall not have evidence of plastic film deposit resulting from the thermal stripping operation.

d. The wire insulation shall not be blistered or swollen, but a slight discoloration is acceptable when using thermal strippers.

e. The illustrated examples of acceptable and unacceptable wire stripping are shown in Figures 3.13-74 through 3.13-78 for thermal strippers, and Figures 3.13-79 through 3.13-82 for mechanical strippers.

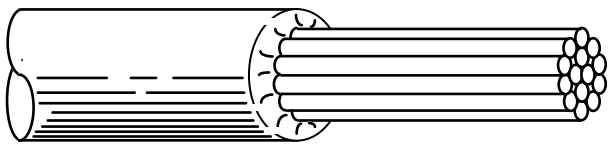

Figure 3.13-74 Acceptable Thermally Stripped, Square and Clean Insulation.

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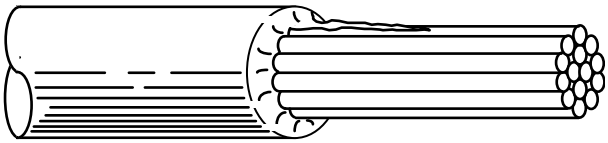

Figure 3.13-75 Unacceptable Thermally Stripped, Smeared Insulation.

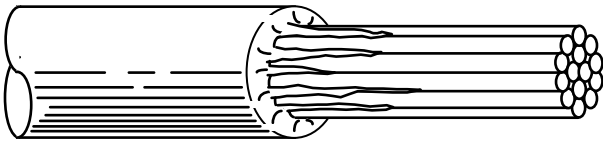

Figure 3.13-76 Unacceptable Thermally Stripped, Insulation with Icicles.

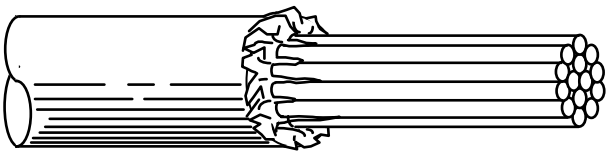

Figure 3.13-77 Unacceptable Thermally Stripped, Excess Heat Globular Appearance.

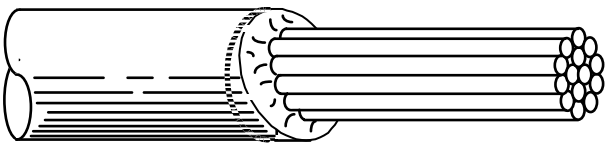

Figure 3.13-78 Unacceptable Thermally Stripped, Irregular Cut Exceeding OD/4.

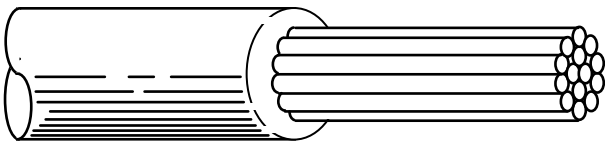

Figure 3.13-79 Acceptable Mechanically Stripped, Clean Appearance.

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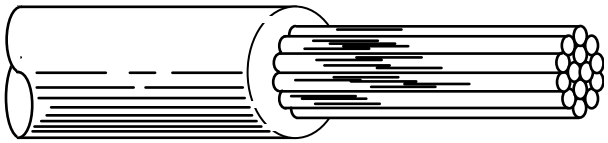

Figure 3.13-80 Acceptable Mechanically Stripped, Minor Burnishing.

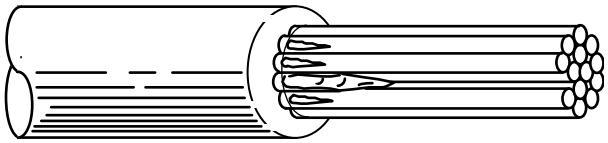

Figure 3.13-81 Unacceptable Mechanically Stripped, Nicked and/or Severed Strands.

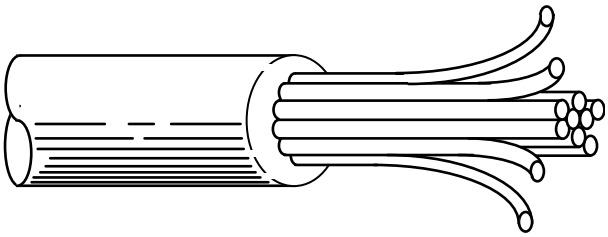

Figure 3.13-82 Unacceptable Mechanically Stripped, Broken Serve.

6.6.3 Tinning of Conductors.

6.6.3.1 Hot Solder Dip. Dip about 1/3 of the length of the conductor to be tinned into a nonactivated liquid, rosin flux. After the lead end has been coated with liquid flux, then dip the flux length of the conductor into the temperature controlled, solder pot, leaving adequate space for the insulation gap, and dwell for 3 seconds, See Figure 3.13-83. Then, slowly withdraw the conductor vertically from the solder pot. Remove solder residues with an approved flux removal solvent using a brush or swab. If the contour of the wire strands is not visible after tinning, there is an excess of solder on the wire. Remove this excess solder from the wire by repeating the dip tinning procedure. Repeat the cleaning process. If excess solder is still present, reject the wire.

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6.6.3.2 Hand Tinning. Dip about 1/3 of the length of the conductor to be tinned into a nonactivated liquid, rosin flux. Place a clean, and well-tinned, soldering iron tip on the conductor near the center of the area to be tinned and apply solder. Remove the soldering iron tip from the conductor by sliding the tip down the conductor and finally, off the end, as shown in Figure 3.13-84. Remove solder residues with an approved flux, removal solvent using a brush or swab. If the contour of the wire strands is not visible after tinning, there is an excess of solder on the wire. Remove this excess solder from the wire by fluxing the wire and then, reheating and sliding the tip down the wire and off the cut end, without applying additional solder. Repeat the cleaning process. If excess solder is still present, reject the wire.

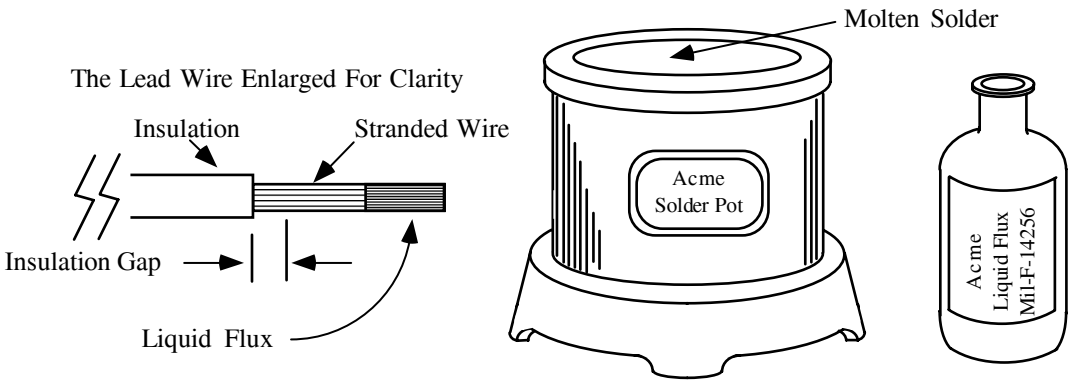

Figure 3.13-83 Using the Solder Pot to Tin Insulated Leads.

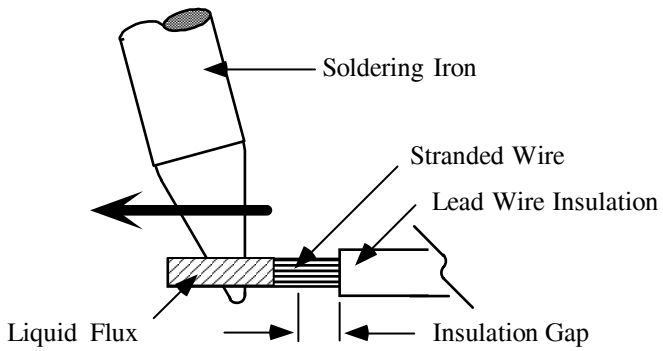

Figure 3.13-84 Using the Soldering Iron to Tin Insulated Leads.

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6.7 Magnetic Device Packaging

6.7.1 Enclosures.

6.7.1.1 Material. All magnetic devices shall be protected from direct exposure to the physical environment by the use of epoxy glass enclosures. The enclosures for magnetic devices shall be fabricated from epoxy-glass laminate per MIL-P-18177, Type GEE, flame retardant Grade 4, or MIL-P-13949, Type GF (flame retardant).

6.7.1.2 Enclosure Cup. Magnetic devices shall be protected by properly shaped enclosures designed to maintain structural integrity, provide a conductive heat path to the mounting surface, if required, and anchor the external leads to prevent stresses being applied to the terminals and the magnet wire leads. Typical enclosures are shown in Figure 3.13-85.

6.7.1.3 Enclosure Cover. A cover shall be optional for magnetic device with radial lead routing. Enclosure covers shall be required on all magnetic devices utilizing the separate impregnating and embedment processes. The enclosure covers shall be enclosed by the cup and be flush with the cup inner edge. The cover thickness shall be as specified in Table 3.13-11. The cover shall have holes, as required, to accept the applicable number of fastener holes. The cover shall have two embedment fill holes of 0.125 of an inch in diameter for covers with a maximum dimension of 1 inch and holes of 0.250 of an inch in diameter for covers greater than 1.00 inch. The embedment, fill hole centers shall be located, as shown in Figure 3.13-86.

6.7.1.4 Dimensions. The enclosure dimensions shall provide a clearance of 0.020 of an inch minimum to 0.10 of an inch maximum to the winding and core assembly, except for the bonding of the winding assembly to the terminal assembly or base. The wall and cover thickness for different enclosure sizes is given in Table 3.13-11.

6.7.1.5 Selecting the Enclosure. The enclosure must be selected to best fit the magnetic device. There must be ample room for the terminal board, and space to route the leads. The selected enclosure should provide ease of assembly and inspection. If the selected enclosure is larger than it needs to be, then, additional embedment would be required to fill these voids. See Figures 3.13-87 and 3.13-88. Always select an enclosure that requires a minimum of embedment. Too much embedment will put undue stress on the magnetic device.

6.7.1.6 Fasteners. The fastener tube wall thickness shall be 0.031 of an inch (0.08 cm), minimum, for all magnetic devices. The fastener tube length shall be identical to the

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height of the enclosure and extend through the base and cover or spacer, as applicable in all applications. The ID of the fastener tube shall be 0.125 of an inch when, a 4-40 screw is specified and 0.144 of an inch when a 6-32 is the specified screw for single fastener tube application. Fastener tubes are shown in Figure 85. Where two or more fastener tubes are used, the internal diameter shall be 0.138 of an inch when, a 4-40 screw is specified and 0.151 of an inch when a 6-32 is the specified screw.

6.7.1.7 Threaded Fasteners. Threaded Fasteners embedded in the encapsulation material shall be of the blind type as specified in JPL Standard STD00009A. The threaded fasteners or blind type inserts are shown in Figure 3.13-89.

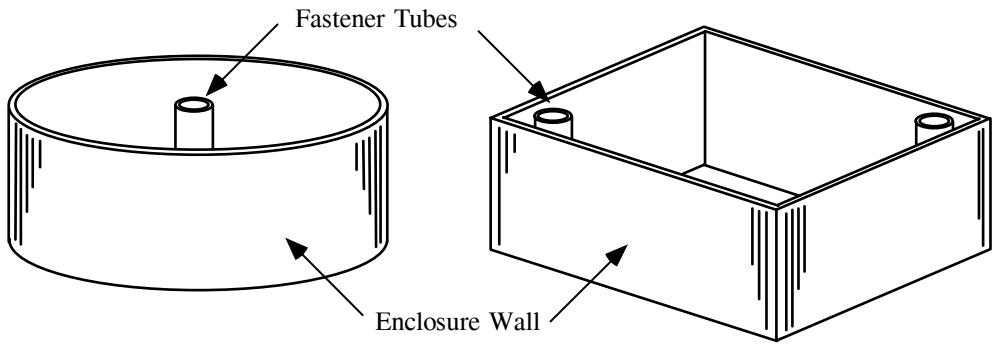

Figure 3.13-85 Typical Enclosures for a Magnetic Device.

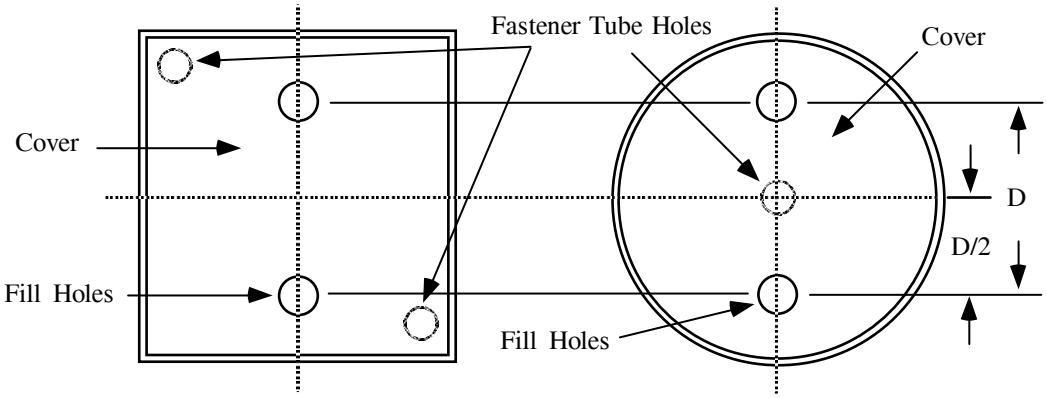

Figure 3.13-86 Embedment Fill Holes Location on the Enclosure Cover.

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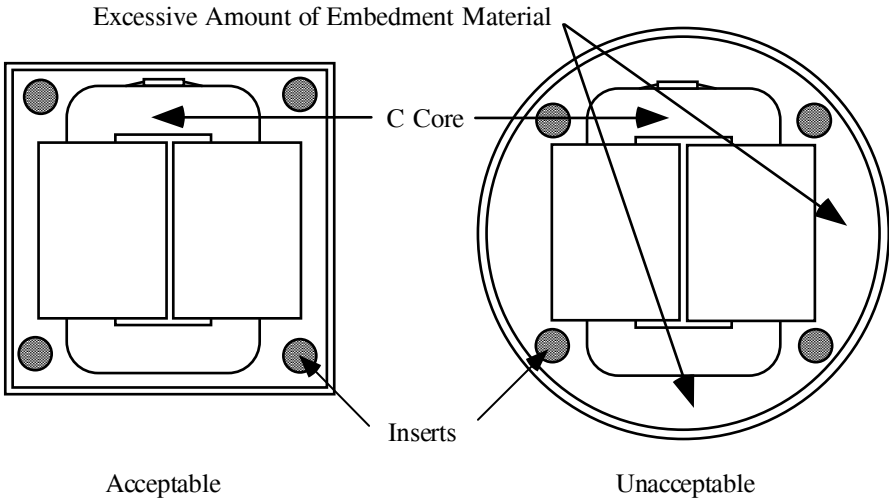

Figure 3.13-87 Comparing Enclosures for C Cores.

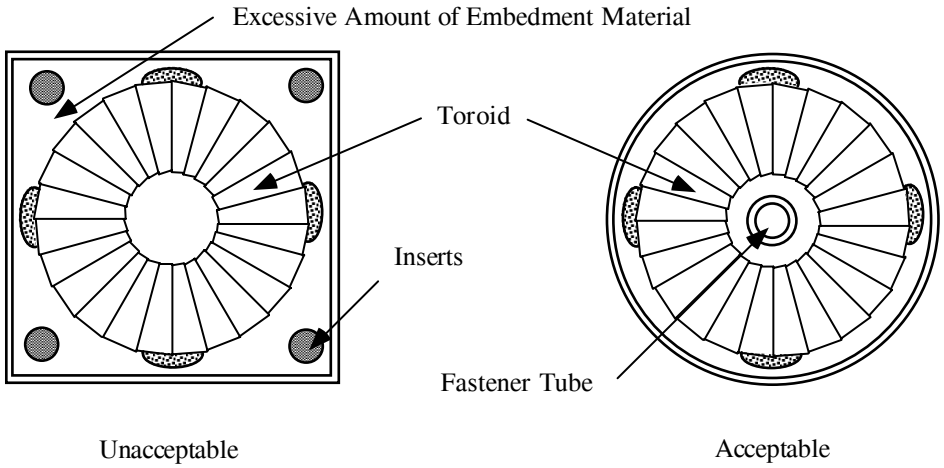

Figure 3.13-88 Comparing Enclosures for Toroids.

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Table 3.13-11 Enclosure Material Thickness.

Enclosure Material Thickness			
OD Width or Length	**Cover Thickness**	**Wall Thickness**	**Type Fastener**
< 1.5 inches	0.02 inches	0.015 inches	Screw
< 38 mm	0.51 mm	0.51 mm	Screw
> 1.5 inches	0.02 inches	0.025 inches	Screw
> 38 mm	0.51 mm	0.64 mm	Screw
*	0.031 inches (min)	0.031 inches (min)	Bracket
*	0.80 mm (min)	0.80 mm (min)	Bracket
* Magnetic device mounted by bracket, a clamp, or a similar device.			

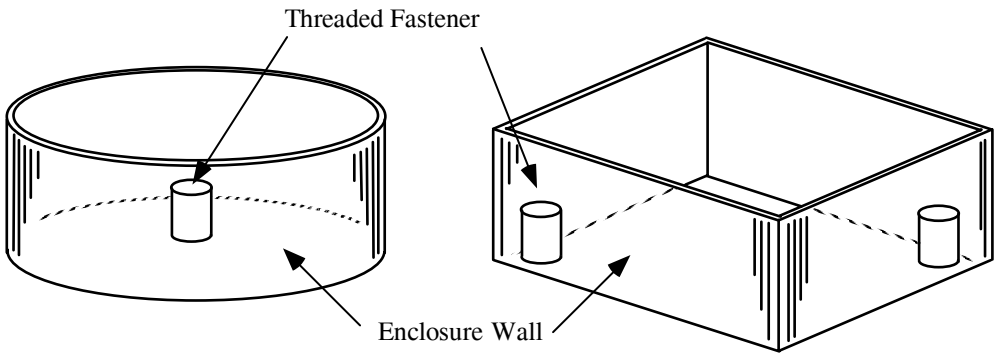

Figure 3.13-89 Enclosures, with Blind Type, Threaded Fasteners.

6.7.2 Terminal Board.

6.7.2.1 Terminal Board Material. The internal terminal boards shall be fabricated from epoxy-glass laminate, per MIL-P-18177, Type GEE, flame retardant Grade 4, or MIL-P-13949, Type GF (flame retardant).

6.7.2.2 Terminal Board Position. The terminal board shall be positioned as follows:

a. Bonded to the wall of a round cup, as shown in Figure 3.13-90.

b. Bonded to the wall of a rectangular cup, as shown in Figure 3.13-90.

c. Bonded to the core, as shown in Figure 3.13-91.

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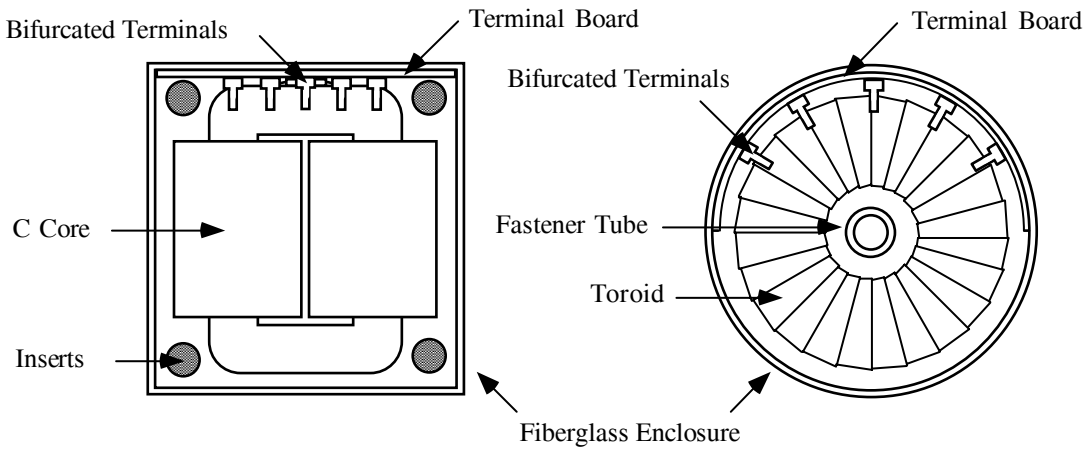

Figure 3.13-90 Terminal Boards, Bonded to the Wall.

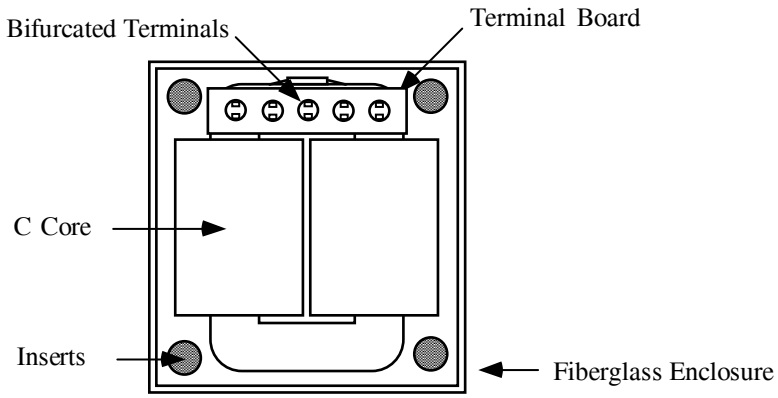

Figure 3.13-91 Terminal Board Bonded to the C Core.

6.7.2.3 Terminal Board Outline. The terminal board shall have embedment, flow-through holes. The holes shall be 0.125 to 0.25 of an inch in diameter and shall number four to each square inch of board surface. The holes shall be located a minimum of 0.050 of an inch from any edge or installed terminal. See Figure 3.13-92.

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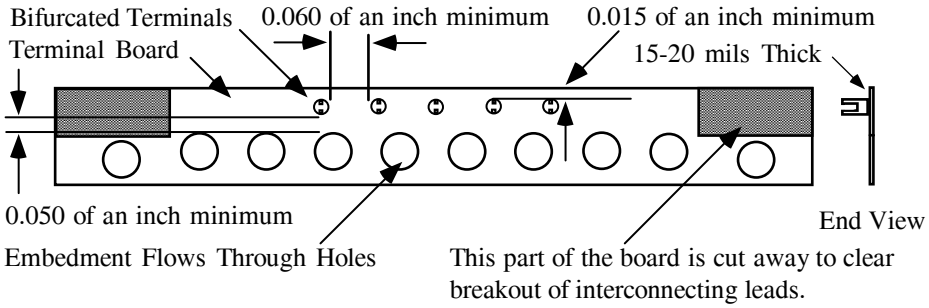

Figure 3.13-92 Terminal Board.

6.7.3 Terminals and Leads.

6.7.3.1 Terminal Description. Terminals shall be bifurcated, solderable, and capable of being permanently fastened to epoxy glass board. Terminals shall be procured per JPL Drawings ST 10591. It is common for a single bifurcated terminal to handle multiple terminations. See Figure 3.13-93. The terminal selected must be able to handle the required number of connecting lead wires.

6.7.3.2 Terminal Installation. Terminals shall be swaged using the force, specified in Table 3.13-12.

Table 3.13-12 Swage Force for Terminals.

Swaging Force for Terminals			
Approximate Size Swage Barrel	**Units**	***Nominal Force (pounds/kilograms)**	**Maximum Force (pounds/kilograms)**
0.041	pounds kilograms	80 36	100 45
0.062	pounds kilograms	130 59	150 68
0.078	pounds kilograms	200 91	225 102
0.09	pounds kilograms	250 113	300 136
0.112	pounds kilograms	500 227	800 363
*This is the force which is required to just meet minimum roll-over requirements.			

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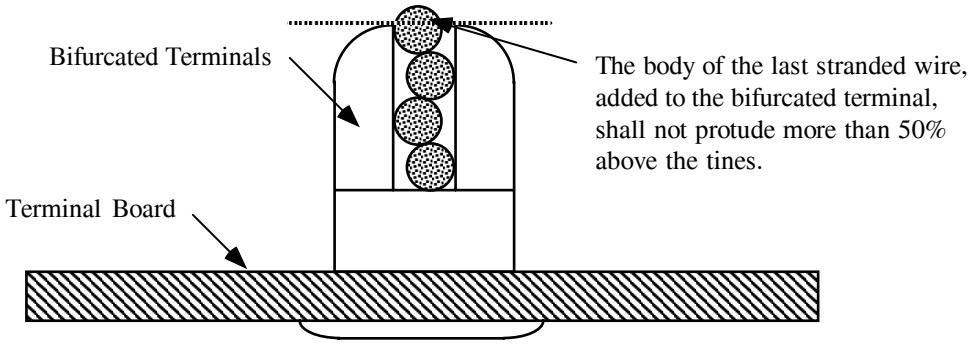

Figure 3.13-93 Bifurcated Terminal with Multiple Terminations.

6.7.3.3 Terminal Flange. The swage flange of the terminal shall be seated and there will be sufficient tightness to assure that the terminal will not more. Maximum permissible height of the terminal swage above the plane of the wiring board shall be 0.012 of an inch and the edge of the rollover shall not be more than 0.004 of an inch above the board surface.

6.7.3.4 Damaged Terminals. Damage to the funnel type swage and loose terminals are unacceptable. See Figure 3.13-94.

a. Acceptable

b. More than two cracks in the terminal flange are unacceptable.

c. A loose terminal as a result of insufficient swage force is unacceptable.

d. An edge of rollover more than 0.004 of an inch above the board surface is unacceptable.

e. Funnel type swage is unacceptable.

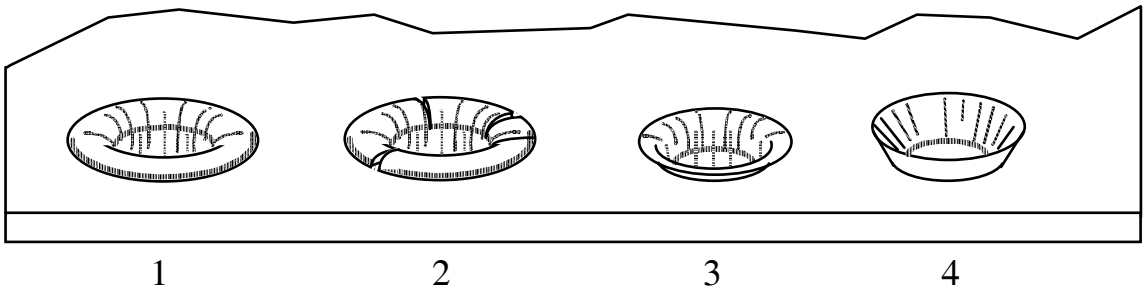

Figure 3.13-94 Terminal Swaging.

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6.7.3.5 Bifurcated Terminals Installation. The bifurcated terminals shall show no evidence of damage caused by the swaging tools. See Figure 3.13-95.

a. Acceptable

b. If the installation is not perpendicular to the plane of terminal area, it is unacceptable.

c. Bent tines are unacceptable.

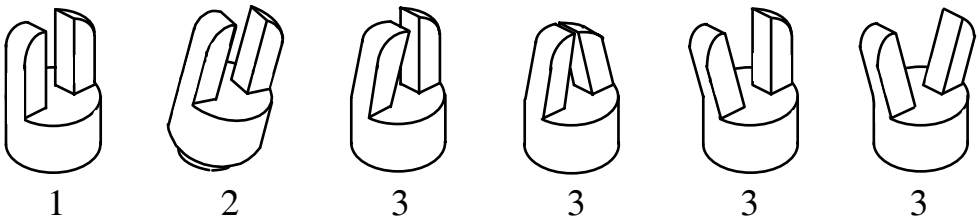

Figure 3.13-95 Terminal Installation.

6.7.3.6 Terminal Installation (measles). Small white spots, or “measles”, caused by terminal installation, shall be acceptable provided they do not form a continuous path between terminals.

6.7.3.7 Terminal Leads. A stranded, insulated terminal lead with a minimum length to facilitate testing and assembly, shall be used for connection to the magnetic device.

6.7.3.8 External Wire Size. The external lead wire size shall be equal to, or greater than, the area of the magnet wire used in the magnetic device. The minimum external conductor size shall be 26 AWG, stranded wire. Bifurcated terminals, or solder ferrules shall provide the solder interconnection between the coil and external leads for Wire 15, AWG, and smaller. The solder interconnection for wire sizes, 14 AWG, and larger, shall be soldered directly to the external lead by the use of an appropriately sized ferrule.

6.7.3.9 Small Leads. Winding leads of 33 AWG, shall be wrapped around a tine of the terminal, a maximum of 180°. See Figure 3.13-96.

6.7.3.10 Large leads. Winding leads of 32 AWG up to 15 AWG shall be terminated without wrapping. See Figure 3.13-96.

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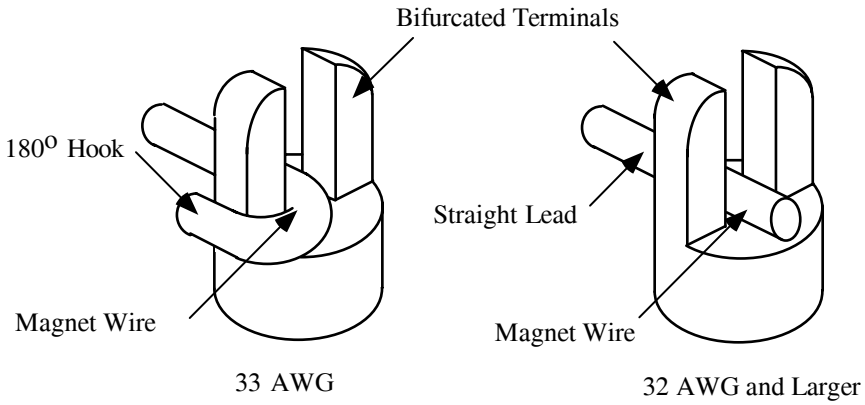

Figure 3.13-96 Winding Lead Termination.

6.7.3.11 Magnetic Device Lead Preparation (pattern). If the drawing does not call out the length of the finish leads, then do the following: Using an enclosure with terminals as a pattern, place the magnetic device in the enclosure, and align the leads with the terminals. With the magnetic device in place, route the leads to provide suitable strain relief, plus sufficient length to rework the solder joint once. See Figure 3.13-97.

6.7.3.12 External Lead Connection. External leads connected to an internal board shall extend through a separate opening in the enclosure, or encapsulation material, with spacing of 0.125 of an inch minimum on centers, as shown in Figure 3.13-98. The external leads shall emerge, evenly spaced, within a 90° sector or side, unless minimum spacing limits require a larger angle. If the number of leads is greater than that which can be accommodated around the periphery, the leads may be aligned in two rows. The external lead length will be 6 inch long unless other wise specified in the specification control drawing.

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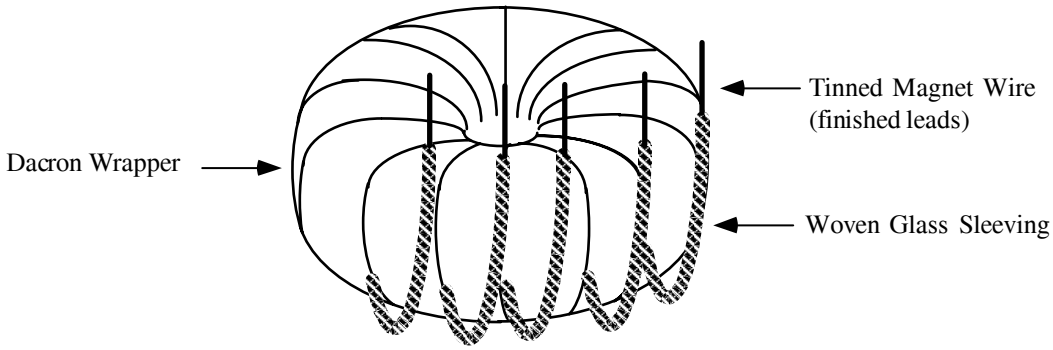

Figure 3.13-97 Winding Leads Breakout.

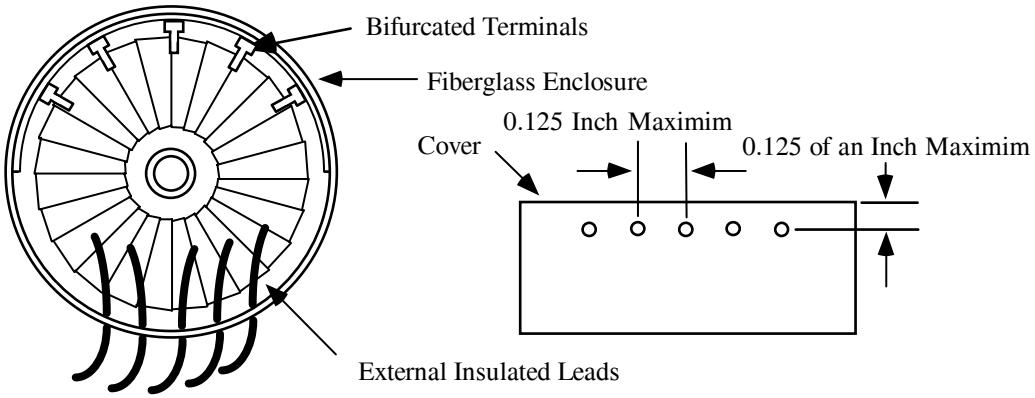

Figure 3.13-98 External Leads Breakout Location.

6.8 Installing the Magnet Device

6.8.1 Installation of Magnetic Device. The magnetic device shall be placed into the enclosure in the location specified on the drawing. If the location is not specified, the magnetic device shall be located as centrally in the enclosure cavity, as practicable. The magnetic device may be spot bonded in place, when properly located. See Figure 3.13-99.

For an approved spot bonding material, go to Table 3.13-13.

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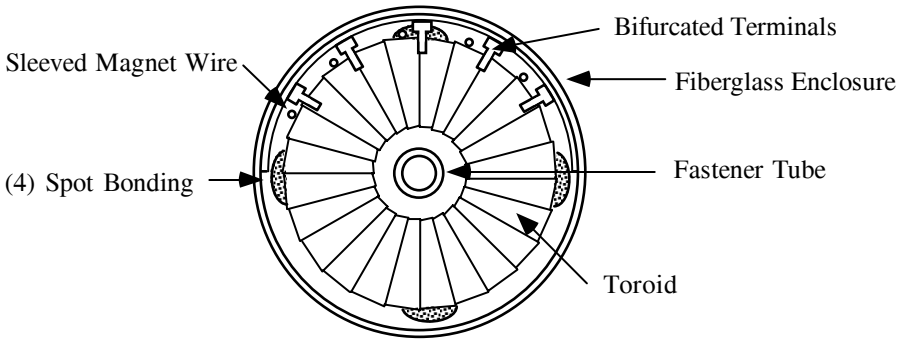

Figure 3.13-99 Spot Bonding the Toroid.

6.8.2 Terminating the Leads. After the magnet wire leads are terminated, with suitable strain relief, the external leads are attached to the terminals and soldered. The design of the enclosure and internal terminal boards shall be such that flexing of external lead wires, prior to encapsulation, shall not apply appreciable strain to the terminals. The standard length for lead wires is 6 inches, If the external lead wire is to be longer it must be called out in the assembly drawing. After the lead wires have been soldered, then a verification of the lead wire numbers, with the numbers on the magnetic device being the same, then the solder joints will be inspected. After inspection of solder joints and lead numbers, the magnetic device is ready for a pre-pot test. See Figure 3.13-100.

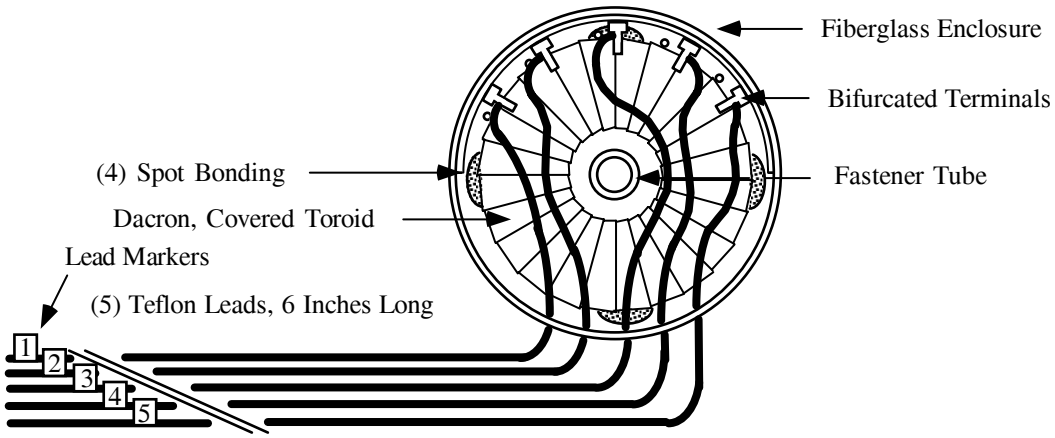

Figure 3.13-100 Magnetic Device in Final Assembly.

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6.9 Polymeric Materials

6.9.1 Material Control.

a. Polymeric materials used in the fabrication of magnetic device shall be documented and controlled using a Mixing Record Sheet, (JPL Form 1888), or an equivalent.

b. Polymeric materials used shall not have exceeded their shelf life, or their working life.

c. All polymeric materials shall have a control sample made for each batch of mixed materials and this control sample shall meet the requirement of Table 3.13-13. The control sample materials shall be stored in a clean aluminum dish, similar to the one in Figure 3.13-101.

d. Materials for embedment, impregnating, and potting shall be vacuum degassed after mixing.

e. Curing temperatures for polymeric materials shall not exceed the maximum temperature requirement of Table 3.13-13.

6.9.2 Spot Bonding.When spot bonding, a magnetic device, use Stycast 1095 and catalyst 9. The spot bonding material requirements is found in Table 3.13-13.

6.9.2.1 Magnetic Spot Bonding. When spot bonding, a magnetic device, it shall conform to the following:

a. There shall be no spot bonding material on terminals, solder joints or parts designed to rotate.

b. Cured material shall not contain dust or debris. The total combined volume of bubbles and voids shall be less than 25 percent of the volume of the bonding material.

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c. The amount and location of the spot bonding material shall be; per Figure 3.13-102.

Table 3.13-13 Polymeric Materials.

Polymeric Materials					
Application	**Manufacturer**	**Materials and Mix Ratio**		**Cure(2)**	**Cured Control Sample(3)**
		Polymeric	**Ratio(1)**		
Transformer Gap Cement	3M	EC2216A EC2216B	140 (+/-1) 100 (+/-1)	Min. cure 24 hrs. at room temp. Full cure, 7 days at room temp. 3 hrs. at 65 C (150 F)	A-93 (+/-3)
Transformer Stress Relief Open Cores	GE	RTV566A RTV566B	100 (+/-1) 0.1	Min. cure, 24 hrs. at room temp. Full cure, 7 days at room temp.	A-47
Transformer Spot Bonding	Emerson Cuming, Inc.	Stycast 1095 Catalyst	100 (+/-1) 9 (+/-1)	24 hrs. at room temp.	>D-65
Transformers and Inductors, (potting)					
Impregnation	3M	Scotchcast 235A Scotchcast 235B	1 2	16 to 20 hrs. at 94 C (200 F)	D-50 or higher
Embedment	3M	Scotchcast 241A Scotchcast 241B	1 2	16 to 20 hrs. at 94 C (200 F)	D-60 or higher
Impregnation	3M	Scotchcast 280A Scotchcast 280B	2 3	16 to 20 hrs. at 94 C (200 F)	D-60 or higher
Embedment	3M	Scotchcast 281A Scotchcast 281B	2 3	16 to 20 hrs. at 94 C (200 F)	D-60 or higher

1. All ratios are parts-by-weight (pbw).
2. Specimens being produced to provide proof of cure.
3. Shore Hardness per ASTM D-2240.

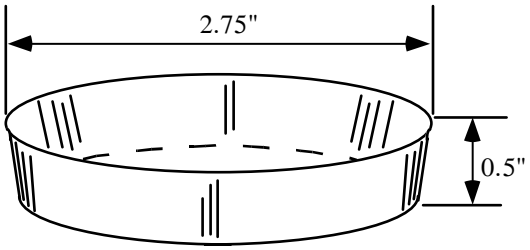

Figure 3.13-101 Proof of Cure Sample Container.

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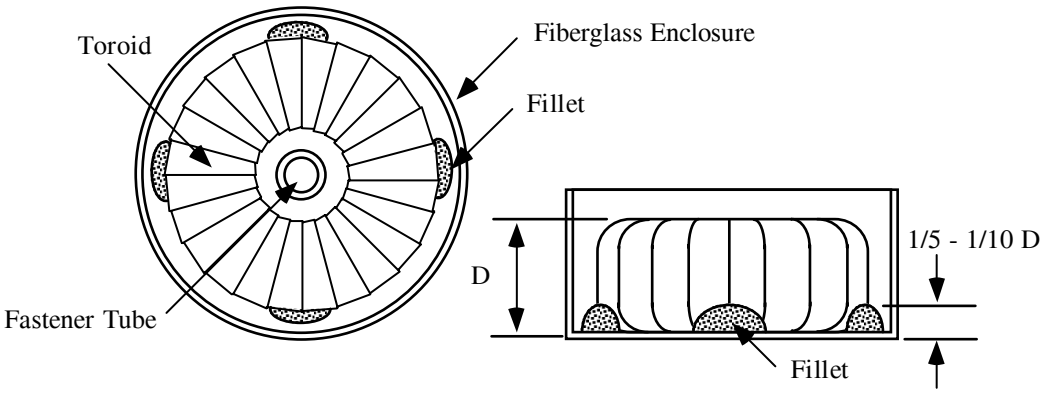

Figure 3.13-102 Spot Bonding, Fillet Size.

6.9.3 General Purpose Bonding (adhesive). General purpose, contact bonding, and gap cement, shall utilize the appropriate material, per Table 3.13-13. The gap cement is applied to the mating surface, as shown in Figure 3.13-105.

6.9.3.1 Mixing the Bonding Adhesive. The application shall conform to the following requirements:

a. Parts A and B shall be thoroughly mixed until an uniform color is obtained.

b. Excess material shall be removed from edges of the bonded area. Any smears of adhesive on the parts shall be removed.

c. Mixing ratio, cure, and control sample requirements shall be per Table 3.13-13.

d. Bonding material thickness shall be 0.006 to 0.010 of an inch.

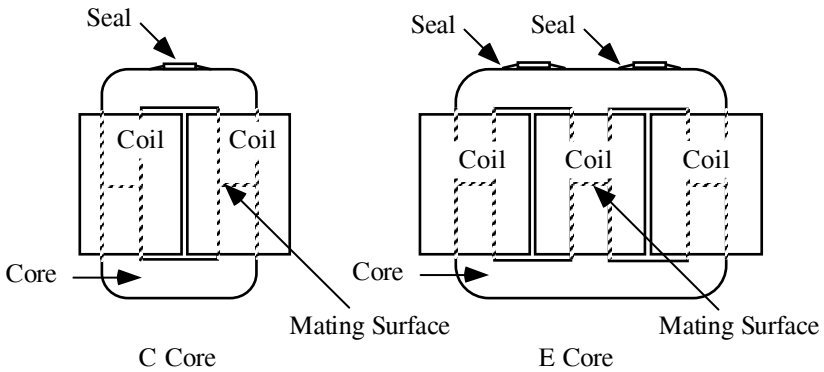

Figure 3.13-103 Mating Surface for “C” and “E” cores.

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6.9.4 Component Stress Relief Coating. When a magnetic device is designed to use a C core or an E core with pressure sensitive magnetic material, it will require stress relief when the device is impregnated. Stress relief can be accomplished by coating the core with a silicone rubber (RTV). A stress relief, silicone rubber RTV material is listed in Table 3.13-13.

6.9.4.1 Mixing the Stress Relief Coating. The coating shall conform to the following:

a. The cured coating is free of spots of uncured coating material.

b. There is no debris in the coating.

c. The silicone rubber coating will completely cover the exposed C core or E core.

d. Mixing ratios and cure, per Table 3.13-13.

6.9.5 Magnetic Device Impregnating and Embedding. A magnetic device requiring impregnation and/or embedment shall use the impregnation and embedment materials, listed in Table 3.13-13. The impregnate material is used to impregnate the coil and replace all voids within the coil completely with the impregnating material. The embedment material is normally a filled material and is much thicker and is used after the magnetic device has been impregnated.

6.9.5.1 Mixing the Impregnate and Embedment. The impregnation and/or embedment shall conform to the following:

a. The cured material is free of spots of uncured materials.

b. There is no debris in the material.

c. There are no cracks, voids, cavities, discoloration, tears or burns in the material, and the material shall not have pulled away from the enclosure.

d. There is no material on the exterior surface of the enclosure, and the potted assembly shall meet the dimensional requirements of the engineering drawing.

e. A process using vacuum impregnating shall be used.

f. Impregnating of coils, on “C” or “E” cores, shall be accomplished prior to the core insertion into the bobbin. Faces of the cores shall be coated with gap cement, per Table 3.13-13, prior to banding. A magnetic device, using split “C” or “E” cores, shall be coated with silicone rubber material, per Table 3.13-13, prior to embedment if required.

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6.10 Facilities

6.10.1 Soldering Facility (Clean Room). The soldering area shall have a controlled environment which limits the entry of contamination. This area shall be continuous controlled to a temperature of 24 +/- 6 C at a maximum humidity of 60 percent. The air entering the area shall be filtered. A positive pressure shall be maintained (with relationship to adjoining areas to prevent infiltration dust-laden air). Work areas and tools shall be maintain in a clean and orderly condition.

6.10.2 Work Station. At the start of each work day work stations shall be free of visible dirt, grime, grease, flux or solder splatters, and other foreign materials.

6.10.2.1 Restrictions. Eating, food storage, smoking, or drinking shall be prohibited at the work stations.

6.10.2.2 Cosmetics. Hand creams, ointments, perfumes, cosmetics, and other materials unessential to the fabrication operation shall not be permitted at the work station.

6.10.2.3 Comfort Zone. Temperature and humidity in the soldering area shall be monitored and maintained within the comfort zone, as shown in Figure 3.13-104.

6.10.3 Lighting. Illumination at the working surface at the soldering stations and solder pots shall be a minimum of 100 foot-candles.

6.10.4 ESD Protection Requirement. The ESD protection for the facility shall meet the requirement of JPL, D-1348.

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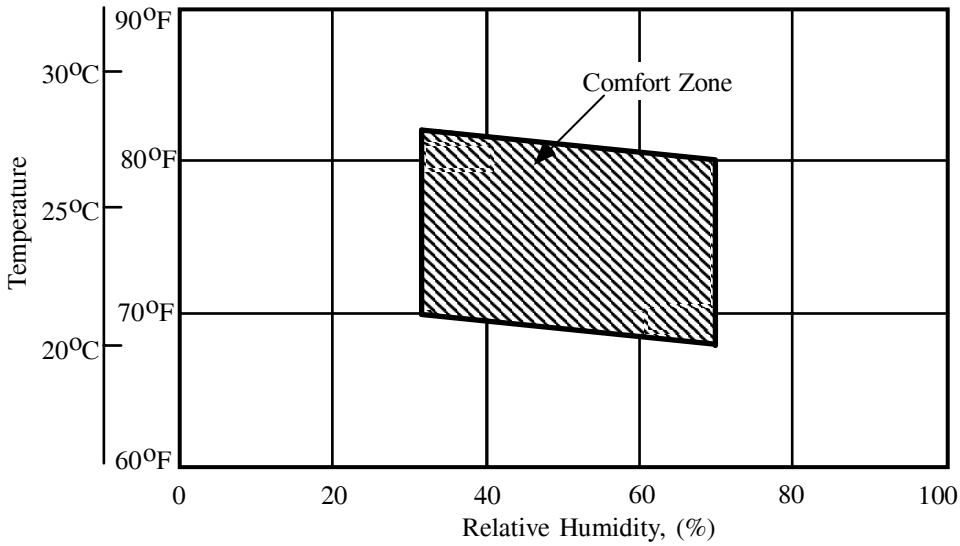

Figure 3.13-104 Comfort Zone vs. Humidity Requirements.

6.11 Equipment

6.11.1 Daily Inspection. Tools shall be checked daily for proper condition, operation, performance, and cleanliness.

6.11.2 Calibration. A calibration plan shall be in place to assure that all equipment and tools are certified to perform operations in a reliable, reproducible manner, such that the items produced will meet the requirements of this document.

6.11.2.1 Calibration Intervals. Calibration intervals shall be based on the type of tool or equipment, the critical performance critically, and the reproducibility of its function.

6.11.2.2 Calibration Records. The calibration plan and record history of the certification of equipment and tools shall be available for inspection.

6.11.3 Soldering Iron.

6.11.3.1 Melting Capability. A soldering iron shall be capable of melting solder on a wire or joint, in less than three seconds.

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6.11.3.2 Soldering Iron Holders. The soldering iron holder shall:

a. Support the soldering iron element and tip without applying excess physical stress.

b. Avoid heat sinking the tip.

c. Protect personnel from burns. See Figure 3.13-105.

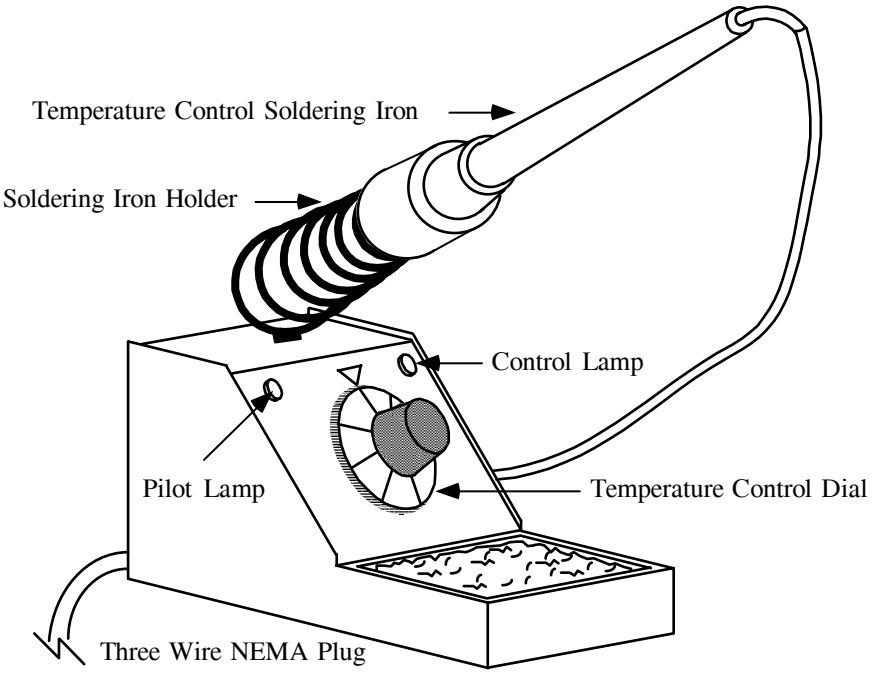

Figure 3.13-105 Temperature Controlled, Soldering Iron.

6.11.3.3 Soldering Iron Tips.

6.11.3.3.1 *Soldering iron tips shall:* a.Provide the greatest contact area while maintaining the maximum visual clearance.

b. Be controlled to 315 C +/-20 C (600 F +/-35 F), except in special applications specified in the assembly drawing.

c. Have less than 2mV leakage to the local ground.

d. Have less than 2 ohms, tip-to-ground.

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e. Be checked for proper insertion, tight attachment, cleanliness, and proper tip size relative to the work involved. Soldering iron tips shall not show signs of dewetting or eroding.

f. Be cleaned, with finely textured, and sulfur-free sponge pads.

g. Be free of oxides during use. See Figure 3.13-106.

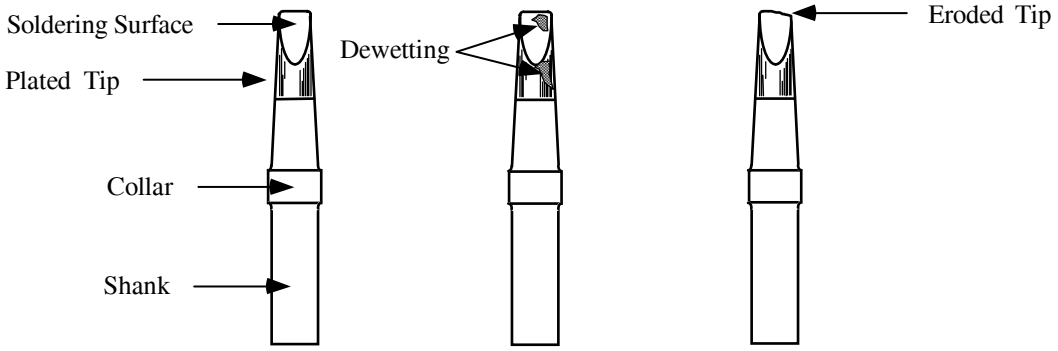

Figure 3.13-106 Soldering Iron Tips.

6.11.4 Solder Pot.

6.11.4.1 Solder Pot. Magnetic Wire Stripping. See Figure 3.13-68.

6.11.4.2 Grounding. Solder pots shall be grounded with a resistance of less than 2 ohms, from case to local ground.

6.11.5 Thermal Wire Strippers.

6.11.5.1 Thermal Strippers. Stranded Wire Strippers. See Figure 3.13-72.

6.11.5.2 Thermal Strippers Type. Thermal wire strippers shall be of a type that can provide the required regulated temperature for the insulation type.

6.11.5.3 Interchangeable Jaws. Wire strippers shall be adjustable or have interchangeable jaws to fit the wire gauge.

6.11.5.4 Grounding. Wire stripping equipment shall be grounded with a resistance of less than 2 ohms, from case to local ground.

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6.12 Soldering Materials and Aids

6.12.1 Solder Selection. Solder composition used on flight hardware shall be either Sn60, Sn62, or Sn63, in accordance with QQ-S-571.

6.12.2 Flux Selection. Noncorrosive, core solder flux and liquid, rosin base flux, used for tinning and soldering, shall be Type R or Type RMA, in accordance with MIL-F-14256D.

6.12.3 Thermal Shunts. Thermal shunts shall be used to protect components that may be damaged by tinning and soldering process. A thermal shunt design should permit rapid application and removal with minimum interference to the soldering procedure and facilitate rapid heat dissipation from the area being soldered. A typical thermal shunt design is shown in Figure 3.13-107.

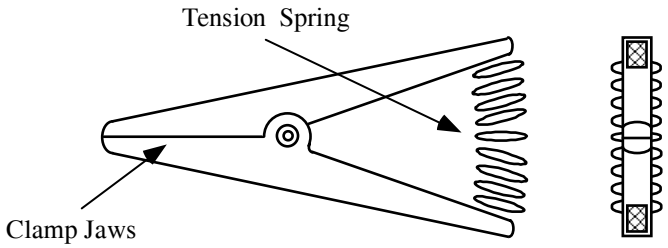

Figure 3.13-107 Typical, Commercially Available, Thermal Shunt.

6.13 General Soldering and Preparation

6.13.1 General Solder Joint Characteristics. Solder joints shall be fabricated to satisfy the following requirements:

a. A concave fillet of solder between conductor and termination.

b. The soldered surface is completely smooth and wetted with solder.

c. The contour of the wire strands are clearly visible after tinning.

d. There should be a lack of projections, bridging, fractures, porosity, and inclusions.

e. No flux residue is on the solder joint after the cleaning process.

f. There is an absence of any stress lines.

g. Insulation on the stranded wire shall show damage in the tinning process.

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h. There should be a gap of 0.030 – 0.090 of an inch between insulation and terminal.

6.13.2 Stress Relief. The lead or wire configuration shall provide stress relief for the joint.

6.13.3 Solder Tinning.

6.13.3.1 General Tinning Characteristics. Tinned components shall satisfy the following requirements:

a. All soldered surface are smooth and completely wetted with solder.

b. Lack of projections, bridging, fractures, porosity, and inclusions.

c. No flux residue on the solder joint after the cleaning process.

6.13.4 Insulation Damage. Insulation on the wire shall not be damaged by the tinning process.

6.13.5 Wire Lay. The lay of the wire shall be undisturbed by the tinning process, as shown in Figure 3.13-108.

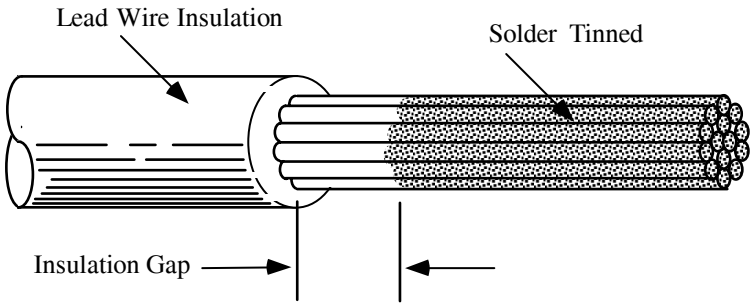

Figure 3.13-108 Solder Tinned, Insulated Lead Wire.

6.13.6 Thermal Shunts. Thermal shunts shall be applied to leads of heat sensitive parts during the tinning process. See Figure 3.13-107.

6.13.7 Excess Solder Removal. Stranded wire, wire braid, or vacuum shall be used to remove excess solder, as shown in Figure 3.13-109.

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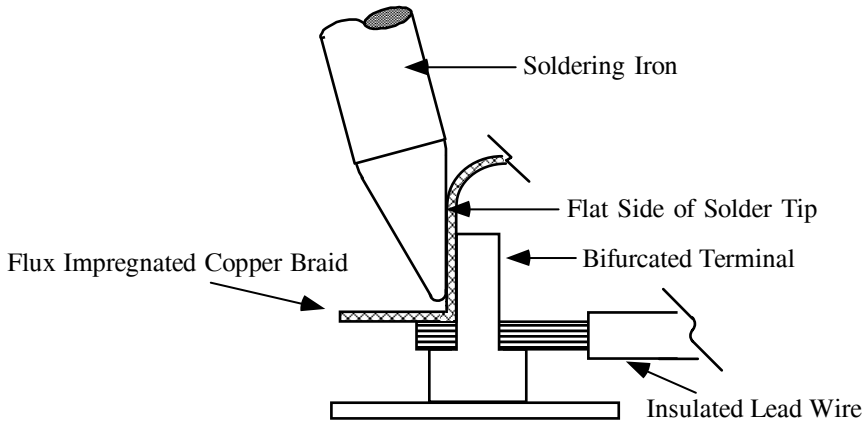

Figure 3.13-109 Removing Excess Solder from a Bifurcated Terminal.

6.13.8 Terminal Soldering.

6.13.8.1 Terminal Mounting Surface. Terminals shall be free of uneven or excessive coating on their mounting surface.

6.13.8.2 Terminal Modification. Any modification of the terminal and conductor shall be prohibited.

6.13.8.3 Bifurcated Terminals.

6.13.8.3.1 *Single Termination.* The lead or wire shall enter the terminal at 90° +/-15 degrees to the plane of the tines and shall meet the preferred solder profile, as shown in Figures 3.13-110, 3.13-111, and 3.13-112.

6.13.8.3.2 *Multiple Terminations.* The top lead or wire, soldered in a terminal, shall have less than one-half of its diameter above the tines as shown in Figure 3.13-113.

6.13.8.4 Turret Terminals. Turret solder joints shall meet the requirements of Figures 3.13-114 and 3.13-115 in their mechanical configuration and preferred solder profile.

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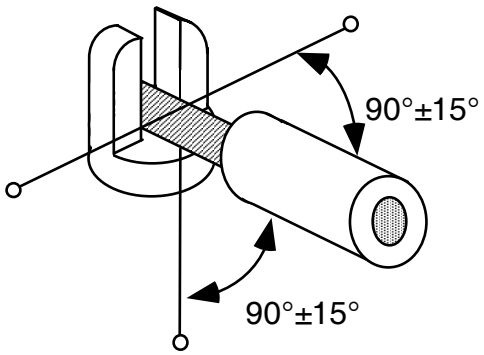

Figure 3.13-110 Bifurcated, Terminal Lead Entrance.

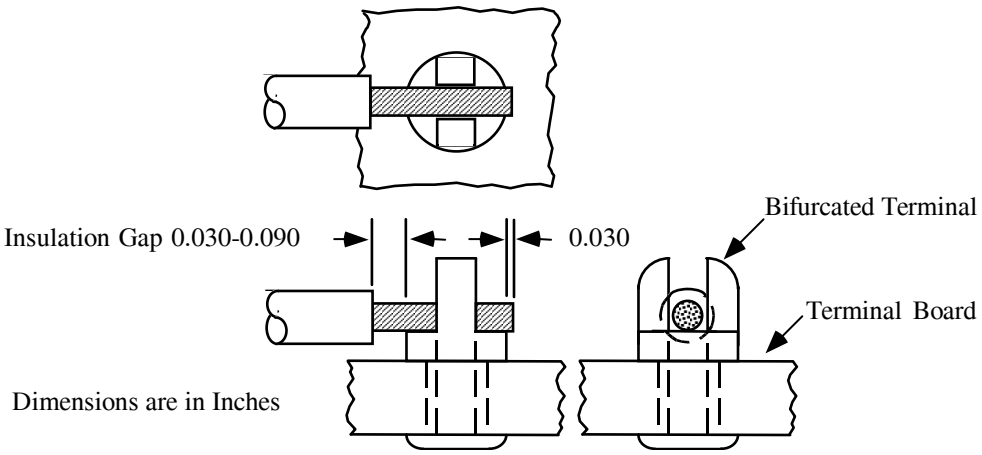

Figure 3.13-111 Bifurcated Terminal Side Routed.

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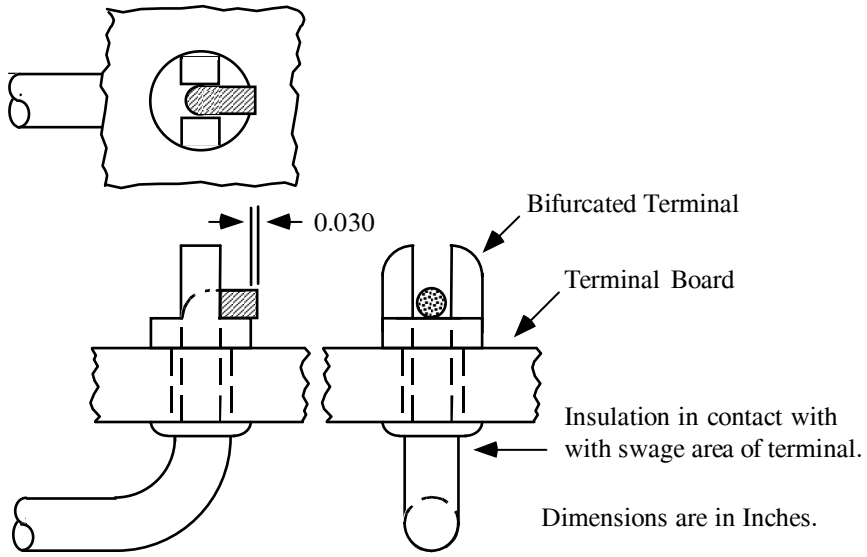

Figure 3.13-112 Bifurcated Terminal Bottom Routed.

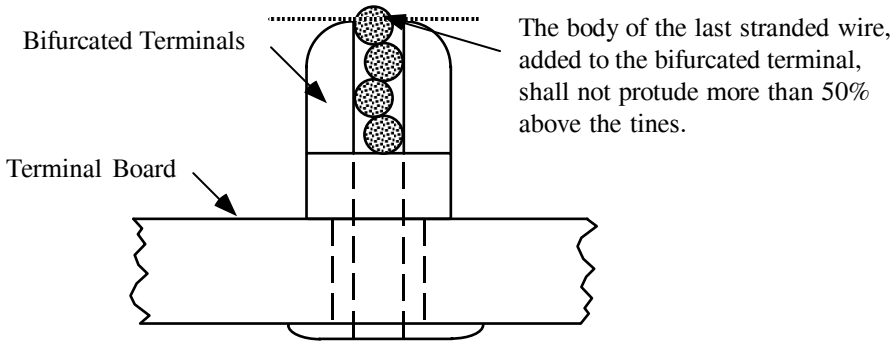

Figure 3.13-113 Bifurcated Terminal with Multiple Terminations.

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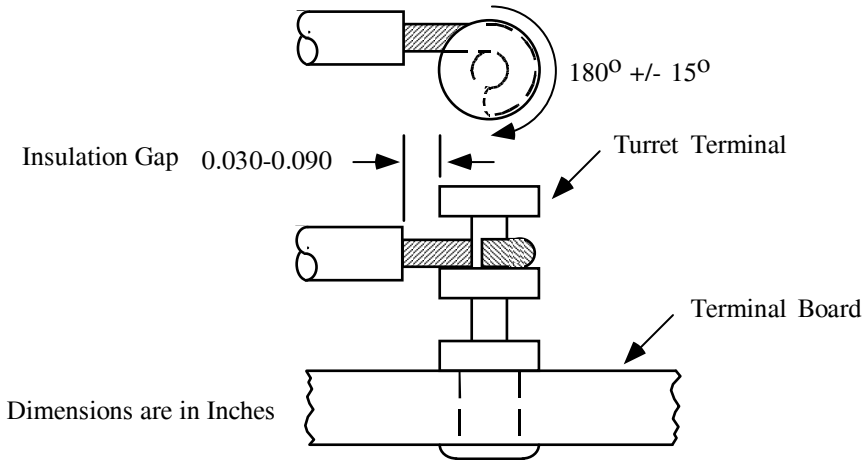

Figure 3.13-114 Dual, Turret Terminal, Solder Profile.

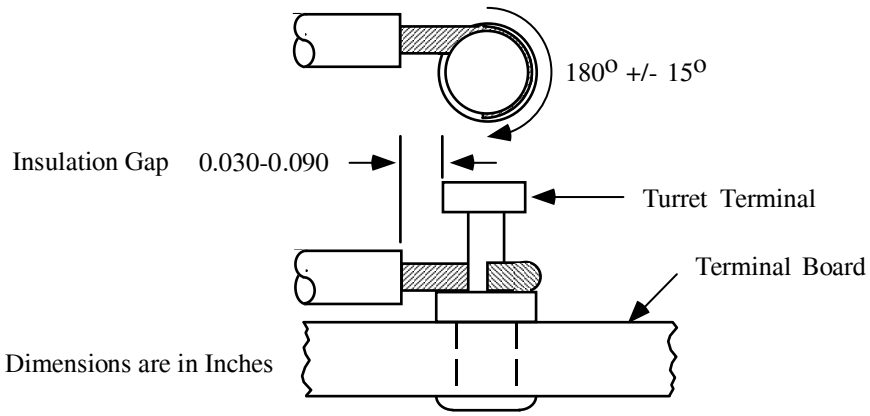

Figure 3.13-115 Single, Turret Terminal, Solder Profile.

6.13.8.5 Preparing Wire Splices for Soldering.

6.13.8.5.1 *Interim Lead (Magnet Wire or Bus Wire).* Interim lead, wire splices shall conform to Figure 3.13-116. The strain relief will consist of a minimum of three turns of magnet wire wrapped tightly, then, two turns, minimum, to be soldered. The magnet wire, lead outline shall be visible beneath the solder. There shall be no overlapping of either the strain relief or the solder

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turns, as shown in Figure 3.13-117. There shall be no protruding pigtails, as shown in Figure 3.13-118.

6.13.8.5.2 *Interim Leads with Two Magnet Wires.* Interim lead wire, with two magnet wires spliced shall conform to Figure 3.13-119. This interim splice shall also conform to Figures 3.13-117 and 3.13-118, regarding overlapping and protruding pigtails.

6.13.8.5.3 *Interim Lead (Insulated Stranded Lead Wire).* Interim lead, wire splices shall conform to Figure 3.13-120. The strain relief will consist of a minimum of three turns of magnet wire wrapped tightly, then, two turns, minimum, to be soldered. The outlines of both the insulated stranded lead wire and the magnet wire lead shall be visible beneath the solder. There shall be no overlapping of either the strain relief or the solder turns, as shown in Figure 3.13-117. There shall be no protruding pigtails, as shown in Figure 3.13-118.

6.13.8.5.4 *Internal Connection and/or Splice (20 AWG and Larger).* Terminating an internal connection or making an internal splice is shown in Figures 3.13-121 through 3.13-123. The magnet wires are brought together cut and tinned, as shown in Figure 3.13-121. The wires are then wrapped with a number 24, AWG bus wire, with a minimum of 4 turns and soldered.

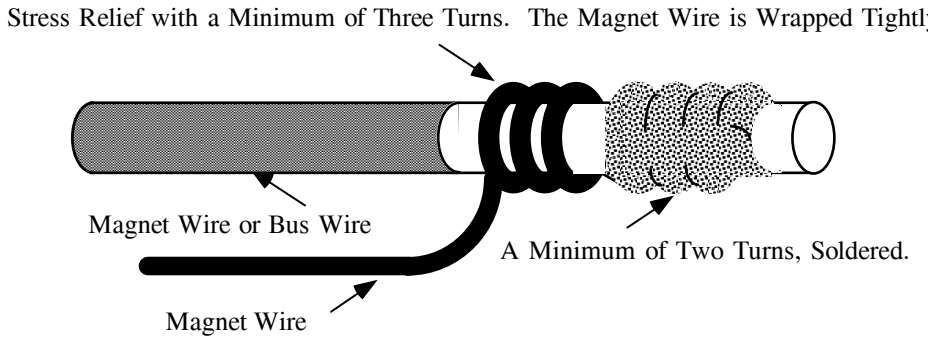

Figure 3.13-116 Acceptable Splice, with Smooth, Even Wrap.

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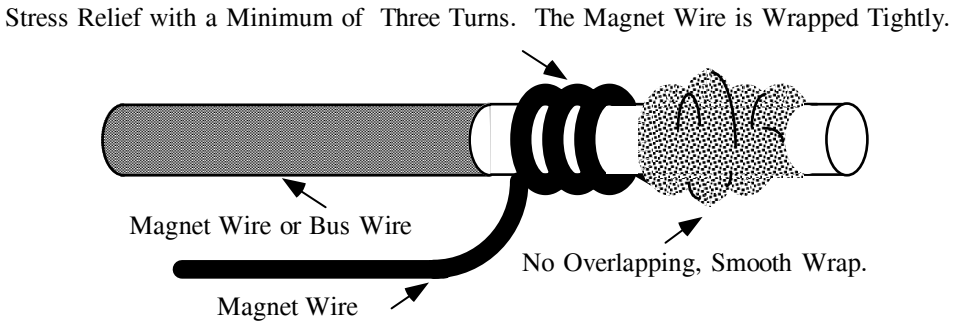

Figure 3.13-117 Unacceptable Splice with Overlap.

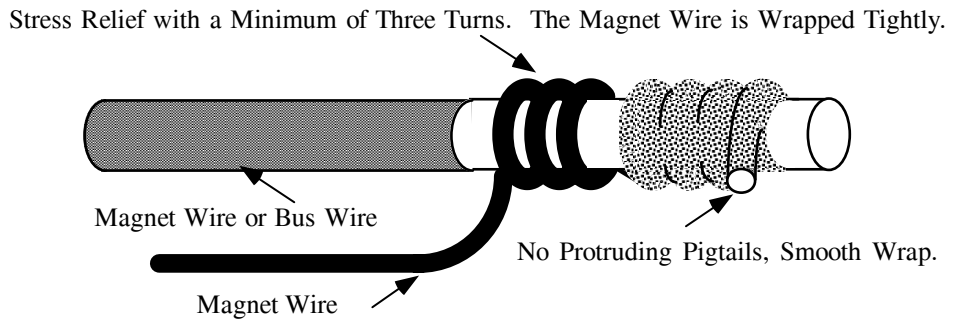

Figure 3.13-118 Unacceptable Splice with Protruding Pigtail.

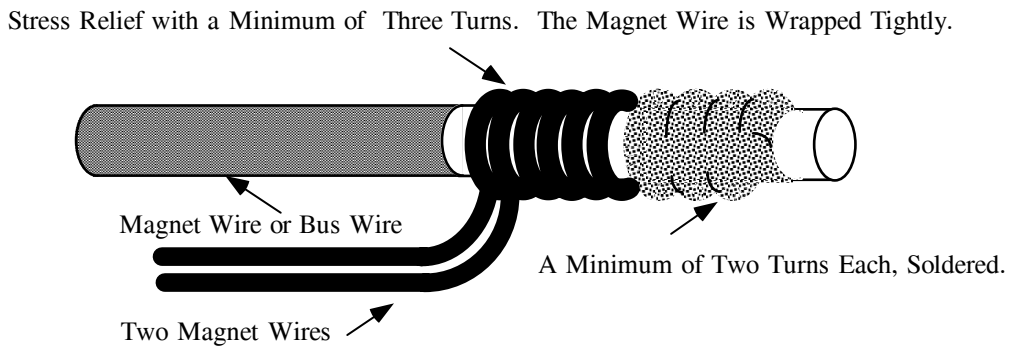

Figure 3.13-119 Acceptable Splice with Two Magnet Wires.

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Stress Relief with a Minimum of Three Turns. The Magnet Wire is Wrapped Tightly.

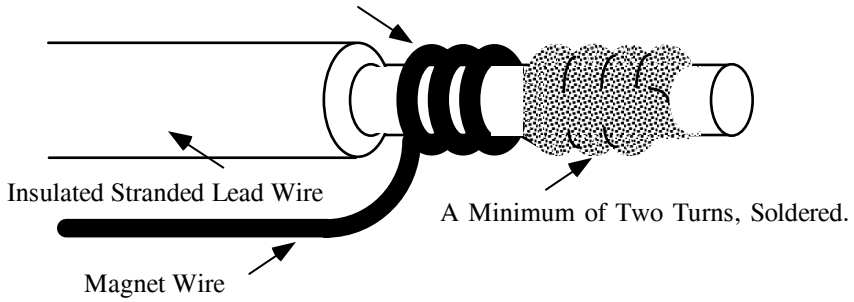

Figure 3.13-120 Splice with Stranded Lead Wire and Magnet Wire.

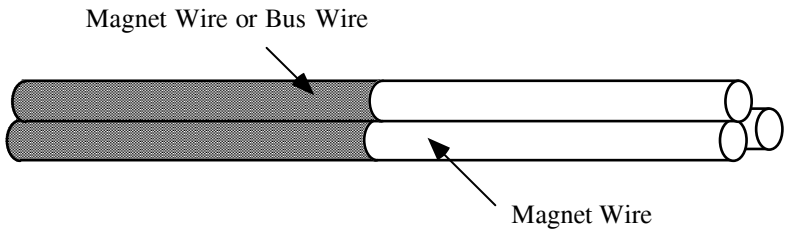

Figure 3.13-121 Interim Lead Splice with Magnet Wire (Step 1).

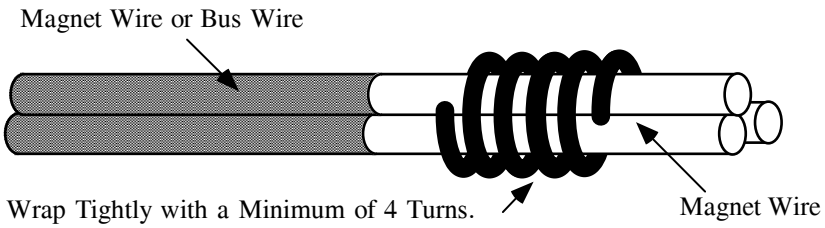

Figure 3.13-122 Interim Lead Splice with Magnet Wire (Step 2).

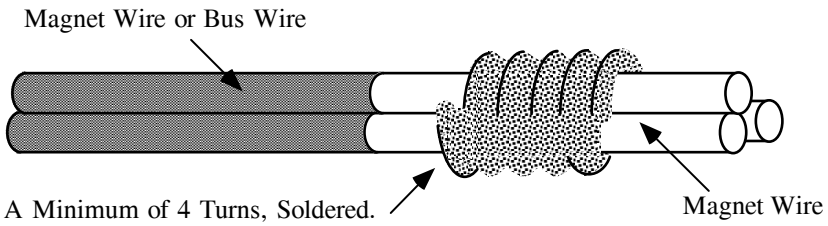

Figure 3.13-123 Interim Lead Splice with Magnet Wire (Step 3).

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6.13.8.5.5 *Magnet Wire to Terminal Lug (magnetic surface mount devices).* The magnetic device shall be placed into the enclosure in the location specified on the drawing. The magnetic device may be spot bonded in place, when properly located. For an approved spot bonding material, go to Table 3.13-13. The strain relief will consist of a minimum of three turns of magnet wire wrapped tightly, then, two turns, minimum, to be soldered. The magnet wire, lead outline shall be visible beneath the solder. There shall be no overlapping of either the strain relief or the solder turns, as shown in Figure 3.13-124.

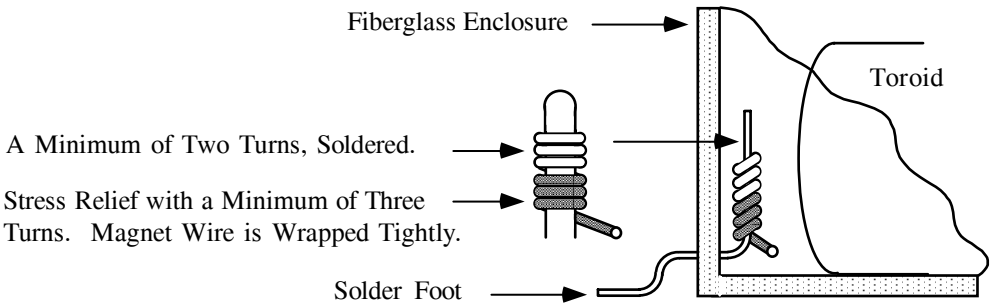

Figure 3.13-124 Typical, Solder Terminal on a Surface Mount Device.

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Component Mounting/Soldering

1 DESIGN REQUIREMENTS

For design rules, the following documents shall apply:

- ANSI/IPC-D-275 (September 1991), *"Design Standards for Rigid Printed Boards and Rigid Printed Board Assemblies."*
- NASA-STD-8739.3 w/ Change 2 (December 1997), *"Soldering Electrical Connections."*

1.1 General Requirements

1.1.1 Drawing Requirements. As a minimum, an electronic parts list and a component mounting drawing shall be generated as a part of the design effort.

1.1.1.1 Electronic Parts List. There shall be an electronics parts list identifying all electronic parts used to assemble the PWB, with reference to their appropriate schematic diagram designators.

1.1.1.2 Component Mounting (Assembly) Drawing. The printed wiring board component mounting and assembly drawing shall list the following:

a. Schematic drawing for reference

b. Fabrication drawing

c. Specifications governing that circuit card assembly

1.1.1.2.1 *Board Depiction.* The component mounting and assembly drawing shall depict the board with the separately manufactured components and parts that are specified in the electronic schematic of the board.

1.1.1.2.2 *Datums.* There shall be a minimum of three orthogonal datum planes, established by points, identified on the drawing, located on grid and featured to establish the mutually perpendicular X/Y/Z reference frame.

1.1.1.2.3 *Dimensions.* All dimensions shall be located from a datum and toleranced.

1.1.1.2.4 *Electronic Parts Size.* All electronic parts shall be shown at their maximum size with polarity and orientation symbology noted.

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1.1.1.2.5 *Component Location and Identification.* The assembly drawing shall clearly identify all circuit components, with the location of their Pin #1, and polarity as required.

1.2 Component Mounting Requirements

1.2.1 Surface Mounting. Requirements for surface mounted components are listed in JPL D-8208, Section 3.5.

1.2.2 Through Hole Mounting.

1.2.2.1 General Requirements. The following through-hole components are sometimes mounted on a PWB. The PTHs (plated through holes) used for through-hole components shall follow the general design requirements called out in JPL D-8208, Section 3.6, paragraph 4.8.2.

a. Axial leaded components

b. Radial leaded components

c. Multi radial leaded components

d. Inline leaded components

1.2.2.2 Exceptions.

a. Vertical Mounting. Vertical mounting of axial leaded components is prohibited.

b. Threaded Component/TO-3 Mounting. Threaded components and TO-3 style components shall be mounted per the requirements of paragraph 1.2.3.4 on page 3.14-6 of this document.

c. Automatic Insertion. Automatic insertion processes shall be reviewed by the procuring NASA installation.

d. Can-Mounted Spreaders. Use of spreaders for mounting TO-Cans is prohibited.

1.2.3 Special Mounting Configurations.

1.2.3.1 Terminal Mounting. Components mounted on terminals shall meet the following requirements.

a. Lead Length Requirements. The minimum lead length from component body, solder seal or butt weld of the lead to the near edge of the terminal shall be twice the diameter (2D) but not less than 0.050 inch as shown in Figure 3.14-1.

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b. Stress Relief Bend locations. Stress relief bends shall be incorporated to prevent solder joint degradation or part damage in a PWB component. Lead bends and bend radii shall be as shown in Figure 3.14-2.

c. Lead Configuration. Leads and wires shall be designed to enter the terminal at 90° + 15° to the plane of the tines.

1.2.3.2 Glass-Encased Components. Glass-encased components shall be encased in heat shrinkable sleeving, or spot bonded using System 2 spot bonding method listed in JPL D-8208, Section 3.17.

1.2.3.3 Top-Down Planar Bonding. TO-type metal can devices (TO-5, TO-99, TO-37, or equivalent configuration) mounted as shown in Figure 3.14-3 shall be bonded top down on the PWB per JPL D-8208, Section 3.17.

CAUTION: TO-Cans mounted per Figure 3.14-3 have limited capability in high vibration/shock environments and limited thermal dissipation capability.

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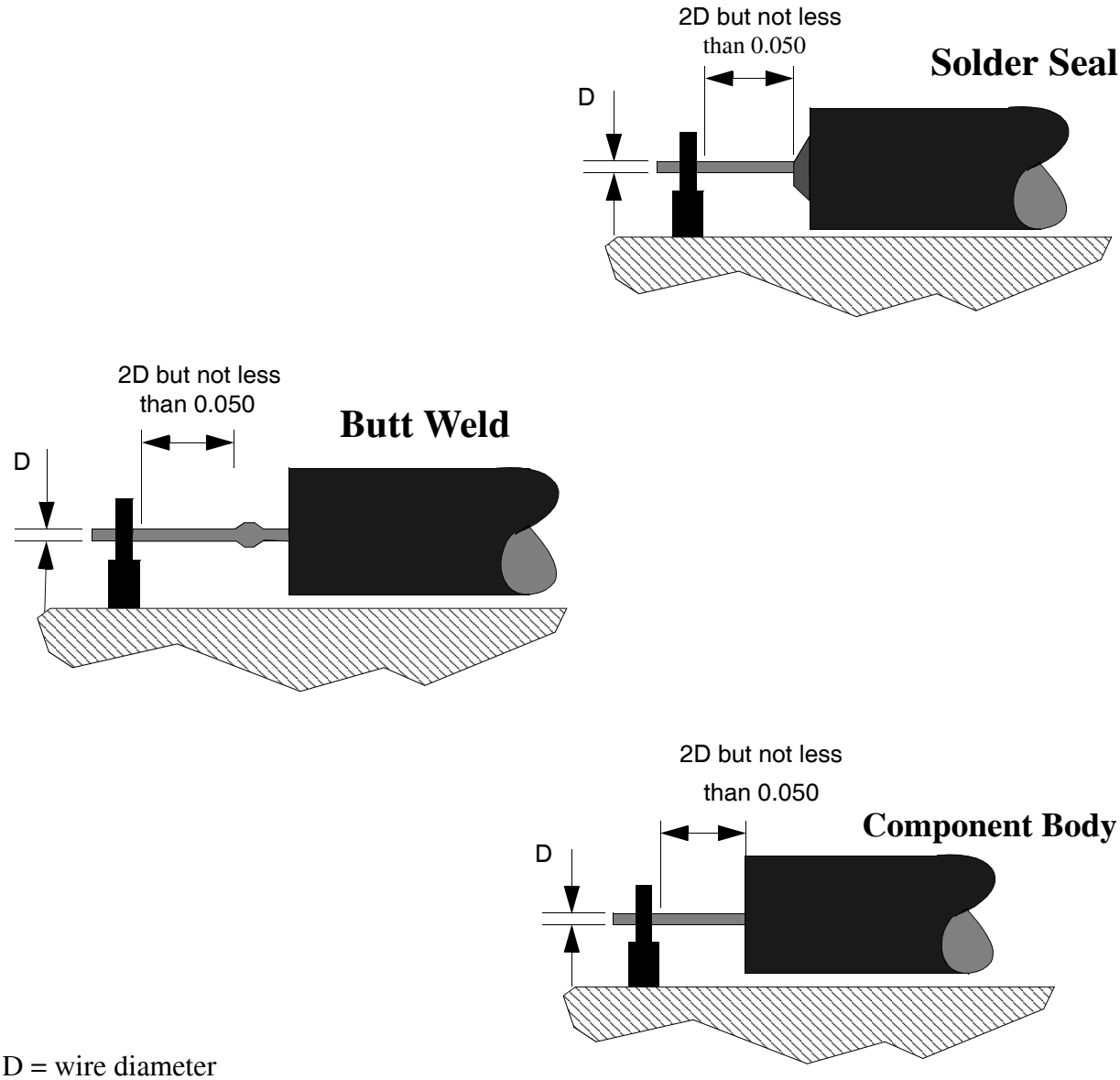

D = wire diameter

Figure 3.14-1 Lead Length

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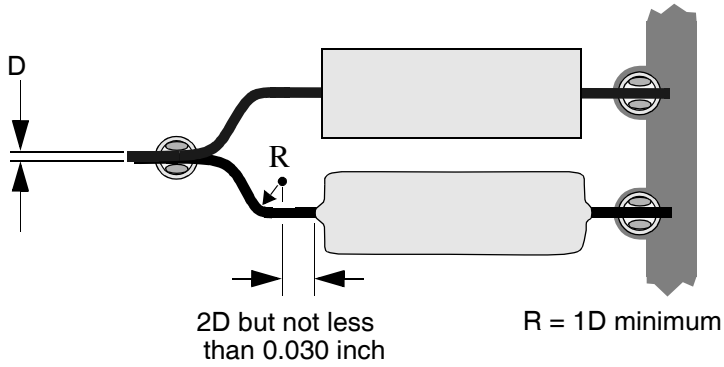

Figure 3.14-2 Location of Lead Bends

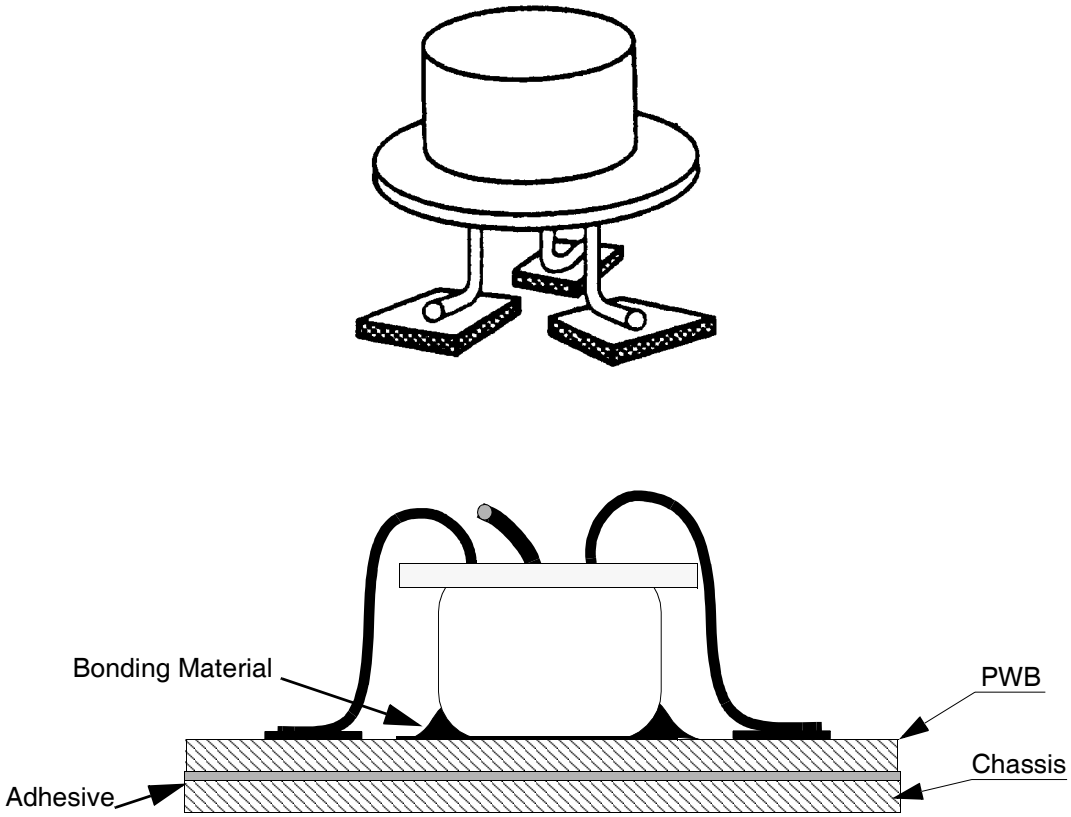

Figure 3.14-3 TO Metal Can Bonding

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1.2.3.4 Threaded Component Mounting.

a. Mounting Configurations. Qualified mounting configurations for components using threaded fasteners such as stud mounted diodes and transistors or bolt mounted clip-encased component shall be as shown in Figures 3.14-4 through 3.14-6.

b. Torque. Fasteners associated with electronic components, such as stud mounted diodes and transistors or bolt mounted clip-encased component cans, per 1.2.3.4(a.) shall be torqued to the requirements in JPL D-8208, Section 3.3.

c. Non-locking Nuts. Non-locking nuts shall be used with diodes and transistors and spot bonded as shown in Figures 3.14-4 through 3.14-6 per JPL D-8208, Section 3.17.

d. Fasteners. Fasteners without an integral locking method shall be bonded per JPL D-8208, Section 3.17.

e. Other Mounting Configurations. Mounting configurations other than that shown in Figures 3.14-4, 3.14-5, and 3.14-6 shall be approved by the procuring NASA installation.

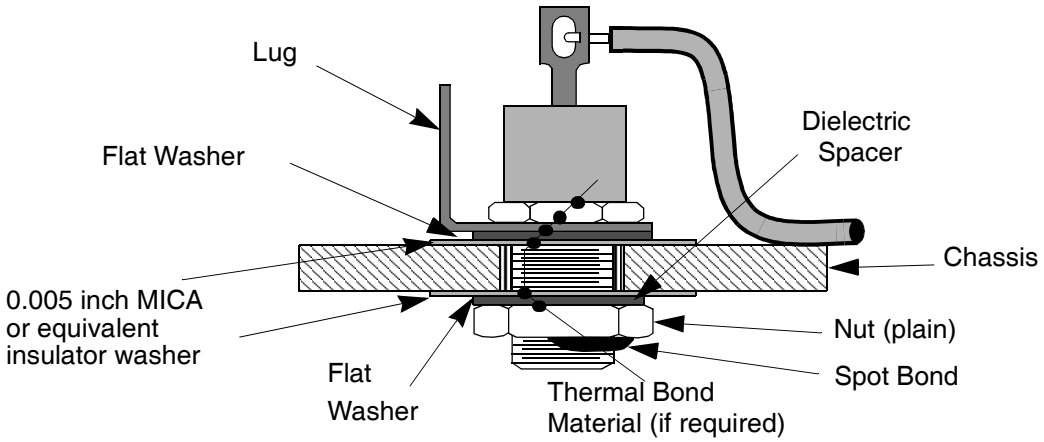

Figure 3.14-4 Stud-Mounted Semiconductor (Top Connections)

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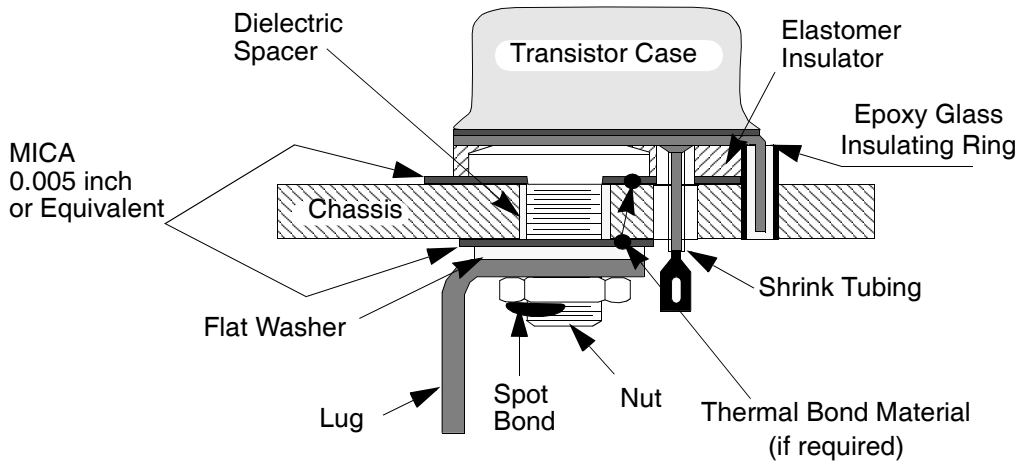

Figure 3.14-5 Stud-Mounted Semiconductors (Bottom Connections)

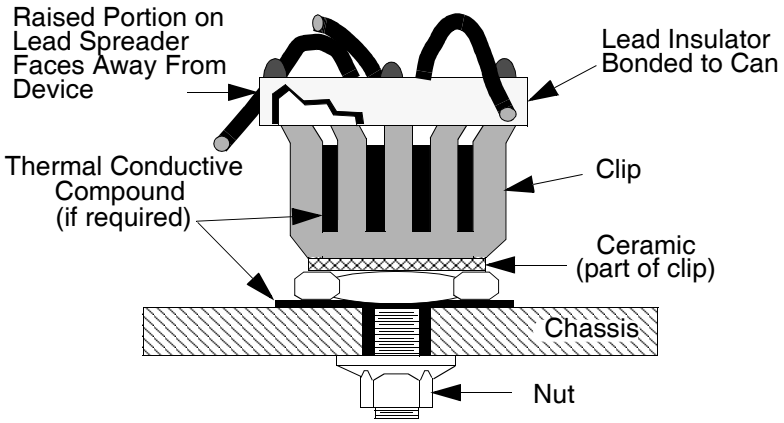

Figure 3.14-6 Bolt-Attached Clip Mounting

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1.2.3.5 Thermally Conductive Mounting.

a. Axial/Radial Leaded Discrete Components. Discrete components that require a higher thermal conductance than provided by normal mounting configurations shall be mounted per Figures 3.14-7 and 3.14-8 with thermally conductive material as detailed in JPL D-8208, Section 3.17.

b. Flat-Packages/Quad-Packages. Flat/Quad Packages requiring high thermal conductivity shall be mounted using methods detailed below.

(1) Conductive Bonding. Components mounted such that the component body is more than 0.015 inches from the PWB surface shall be bonded to the PWB or support substrate using thermally conductive material as detailed in JPL D-8208, Section 3.17.

(2) Lead Forming. Components can be lead formed such that the component body is nearer than 0.015 inch to the board surface for improved thermal conduction. Components should nominally be 0.005 inch before bonding with conductive material.

(3) Mounting with Shims. Aluminum, copper, or ceramic shims mounted per Figure 3.14-9 can be used to improve thermal conductivity. Shims shall be bonded to the component and PWB using thermally conductive material as specified in JPL D-8208, Section 3.17.

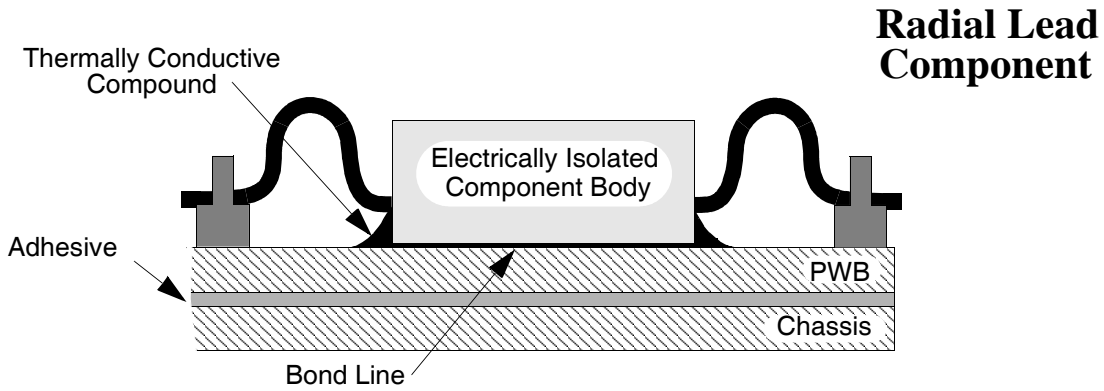

Figure 3.14-7 Thermal Mounting

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Radial Lead Component

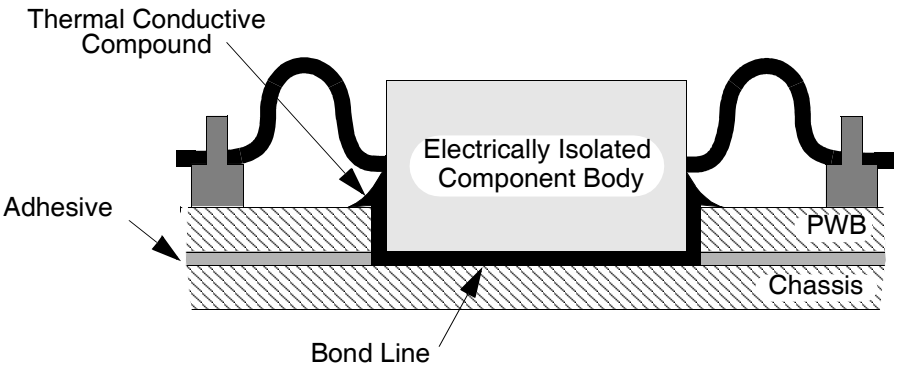

Figure 3.14-8 Thermal Mounting

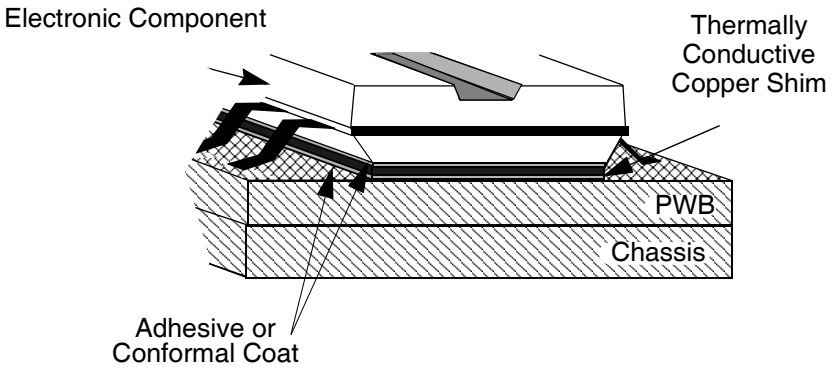

Figure 3.14-9 Planar Component with Shim

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c. Top-Down PWB Cut Out Bonding. TO-type metal can devices requiring a short thermal path shall be mounted top down in direct contact with the heat sink in a PWB cut out, as shown in Figure 3.14-10.

d. Dual Inline Packages. Dual inline packages (DIPs) requiring high thermal conductivity shall be mounted using methods detailed below.

(1) Straps/Braids. Improved thermal conductivity for surface mounted Dual Inline Packages (DIPs) shall be accomplished using straps or braids as shown in Figure 3.14-11 and the following:

- Strap/Braid Shape. The free end of the strap/braid shall be formed into an S shape prior to being installed between the package and the PWB
- Strain Relief. The "S" shape strap/braid shall provide sufficient strain relief to accommodate adhesive wicking, solder wicking, and thermal excursions so the induced stresses do not damage the solder joint.
- Installation to Package. The strap/braid shall be attached to the top of the package by bonding with thermally conductive filled adhesive per JPL D-8208, Section 3.17.
- Installation to PWB. Attachment of the strap/braid to the heat rejection path on the PWB shall be by soldering, by bonding using thermally conductive adhesive per JPL D-8208, Section 3.17, or by securing with a mechanical fastener. If adhesive bonding or soldering is used, the addition of a mechanical fastener is recommended.

(2) Ceramic Shims. Ceramic shims mounted per Figure 3.14-9 can be used to improve thermal conductivity. Shims shall be bonded to the component and PWB using thermally conductive material as specified in JPL D-8208, Section 3.17. Minimum bondline thicknesses between the shim and the component/PWB shall be maintained.

CAUTION: Use of ceramic shims under surface mounted DIPs will cause a reduction in thermal cycle fatigue life in associated solder joints. Straps and/or braids shall be used on DIPs wherever possible to improve thermal conductivity.

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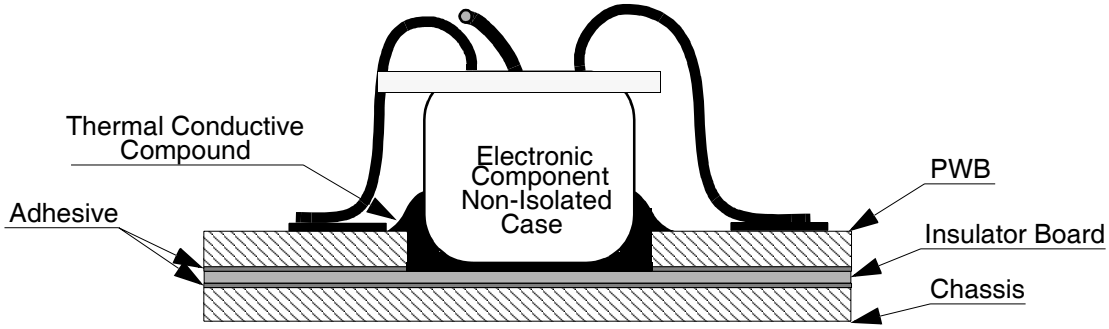

Figure 3.14-10 TO Can Thermal Bonding

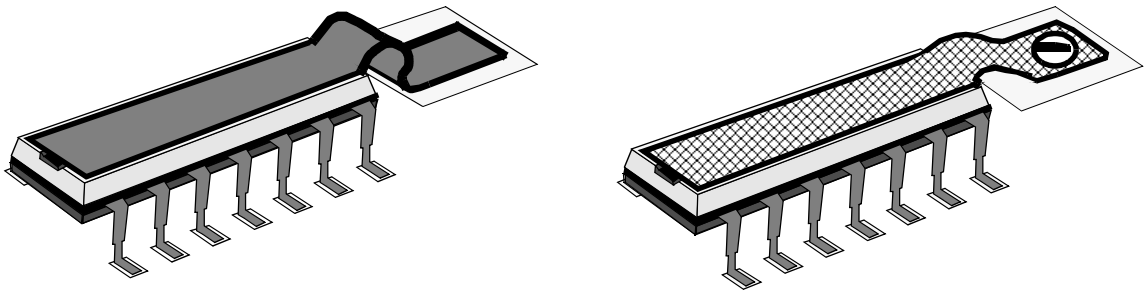

Figure 3.14-11 Planar Components with Strap and Braid

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1.2.3.6 Mechanical Support of Components. All components weighing 0.1 ounce or more per lead or greater than 0.5 ounce shall be bonded to the substrate, or supported by other mechanical means, to insure that the soldered joints and leads are not relied upon for mechanical strength.

1.2.3.7 Jumper Wires. Jumper wires, when used, shall be soldered on lands or on terminals. Acceptable configurations for leads or wires terminating in solder joints are illustrated in Figures 3.14-12 through 3.14-17, with all dimensions in inches.

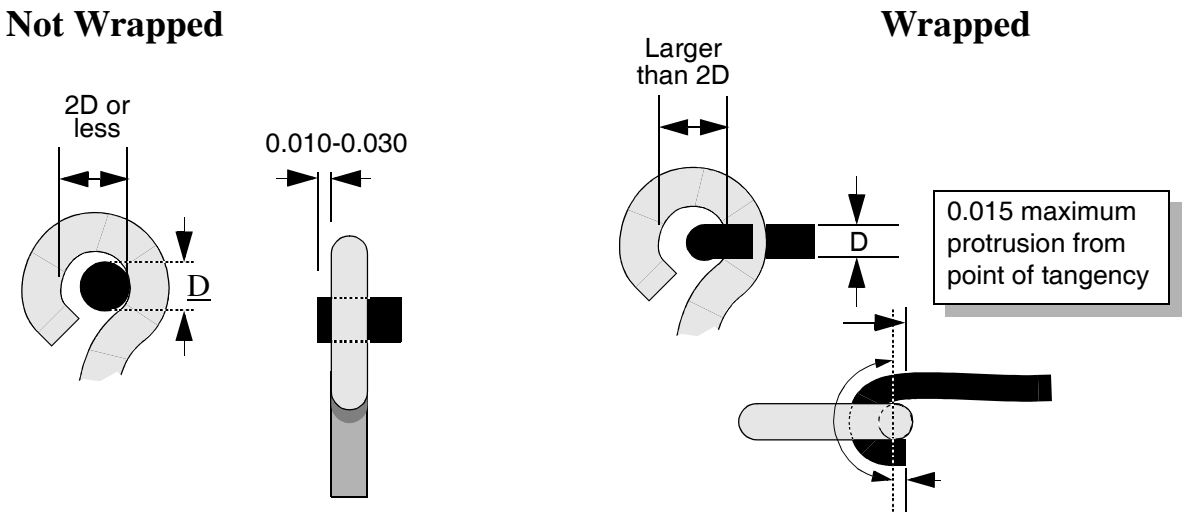

Figure 3.14-12 Hook Terminal Configuration

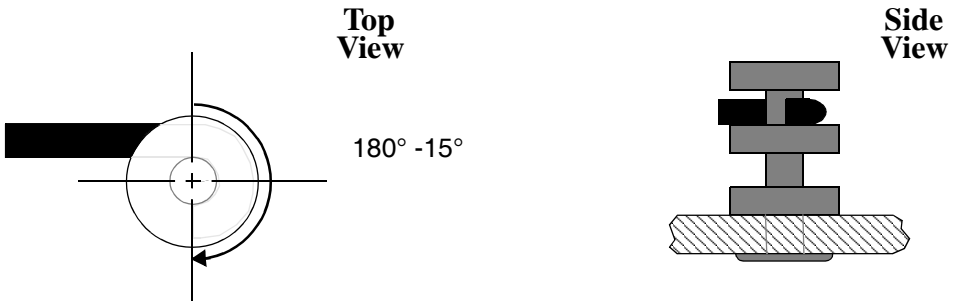

Figure 3.14-13 Turret Terminal Configuration

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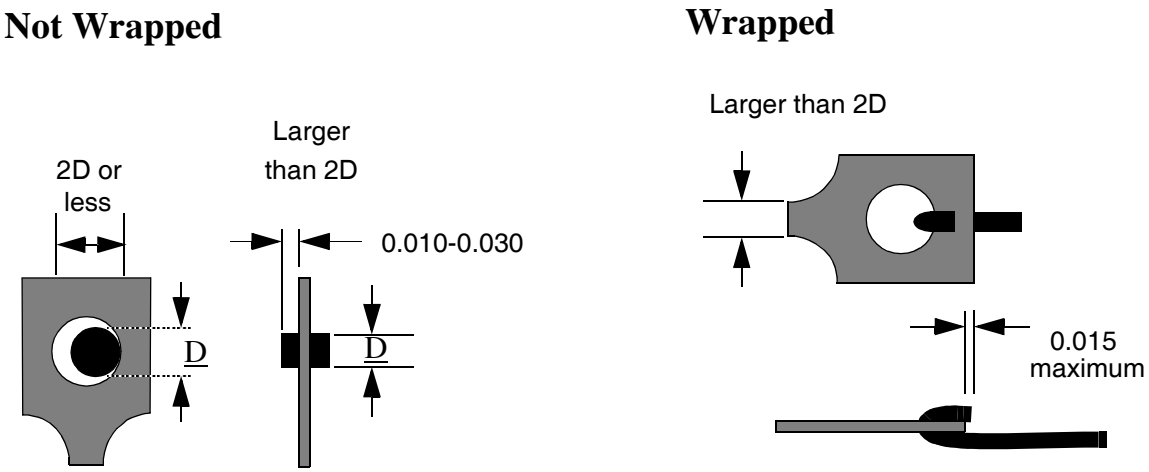

Figure 3.14-14 Eyelet Terminal Joint Configuration

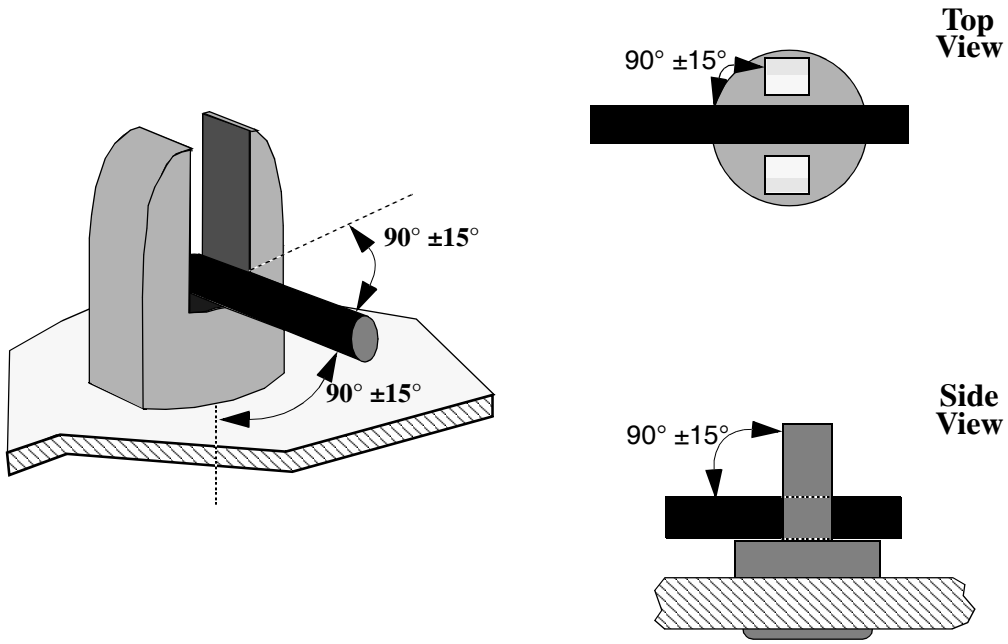

Figure 3.14-15 Bifurcated Terminal Lead Orientation

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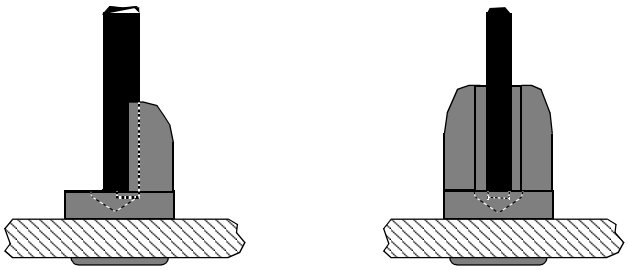

Figure 3.14-16 Single Tine Terminal Joint Configuration

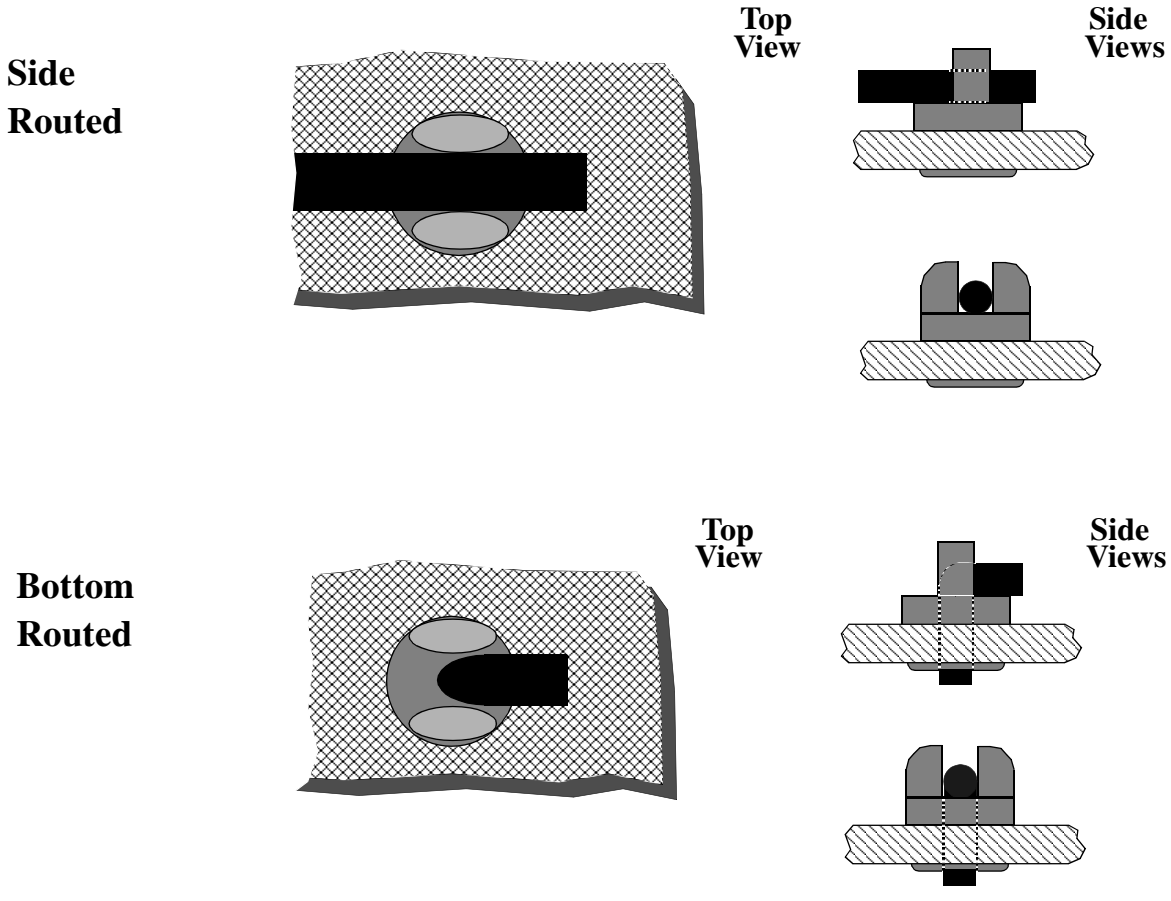

Figure 3.14-17 Bifurcated Terminal Joint Configuration

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1.2.3.8 Continuous Runs. A continuous solid bus wire may be run from terminal to terminal if three or more bifurcated or turret terminals are to be connected (see Figure 3.14-18) provided that:

a. The connections to the first and last terminal meet the requirements listed in Para. 1.2.3.1.

b. A curvature is included in the unwrapped wire portion of the jumper to provide relief of tension from environmental loading.

c. In the case of pierced or perforated terminals, the wire shall contact at least two non-adjacent contact surfaces of each intermediate terminal.

1.2.3.9 Hook Terminals. The maximum wire wrap shall not exceed the end of the hooks (see Figure 3.14-19). Wire wrap shall be 180° minimum and, as a maximum, should not overlap.

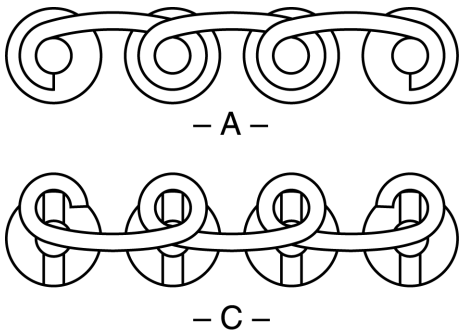

Figure 3.14-18 Continuous Run Wire Wraps.

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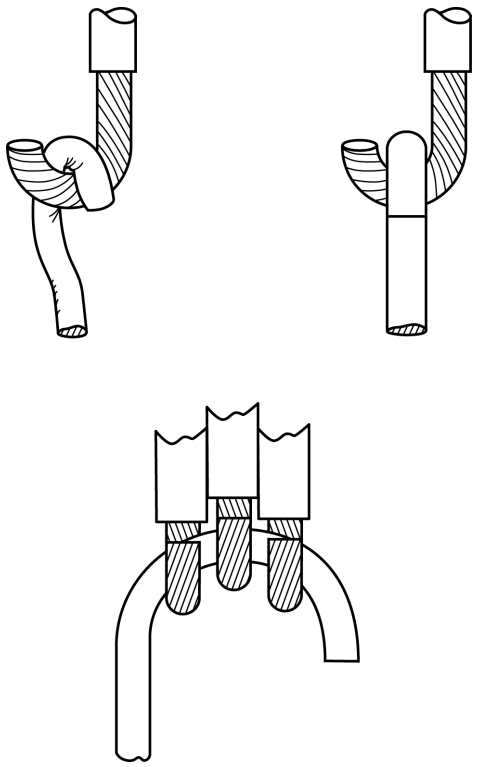

Figure 3.14-19 Hook Terminal Connections.

1.2.3.10 Radiation Shielding.

a. Shielding Provision. Electronic components and packaging materials that are sensitive to high-energy radiation shall be provided with shielding.

b. Radiation Shield Design. The shield design shall provide shielding over the complete 4-steradian angle or any portion thereof depending on the shielding analysis required to meet the mission design radiation environment.

c. Adjustable Shielding. Space Electronics Incorporated of San Diego, California, has a proprietary design called a Rad-Pak that packages die on a substrate within a radiation shield. The shielding thickness is adjustable.

d. Radiation Shield Analysis. The radiation shield analysis shall give the shield requirements in gm/cm^2 of aluminum, or equivalent.

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(1) Radiation Shield Design Analysis. The design of the radiation shield shall be based on the mass and the shielding efficiency of the shield material.

(2) Radiation Shield Sizing. The size of the radiation shielding shall depend on the physical characteristics of the electronic component as shown in Figure 3.14-20 through Figure 3.14-22.

(3) Radiation Shield Analysis Values. The aluminum equivalent values listed in Table 3.14-1 shall be used for the shield materials, thicknesses and configurations listed.

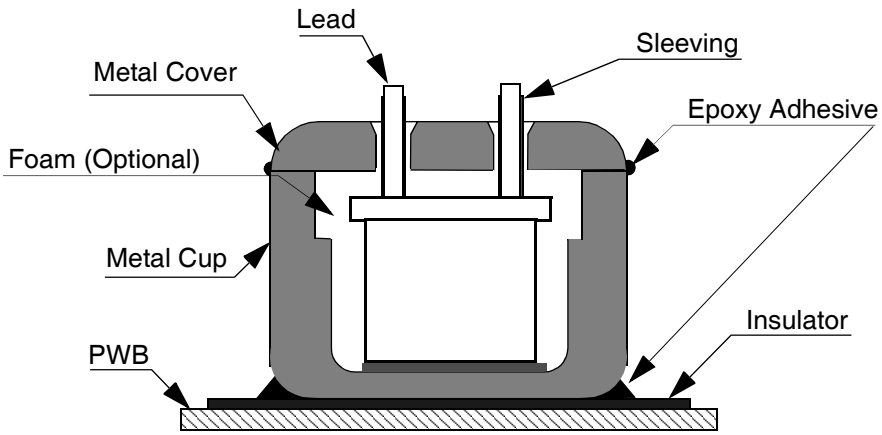

Figure 3.14-20 Radiation Shield for JEDEC-TO Cases

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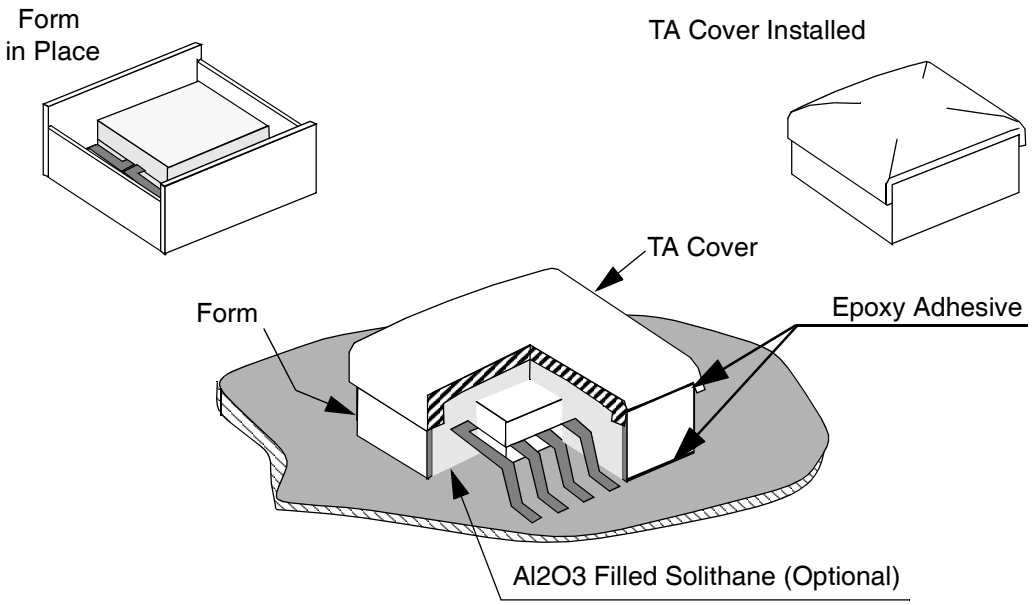

Figure 3.14-21 Flat Pack Radiation Spot Shield

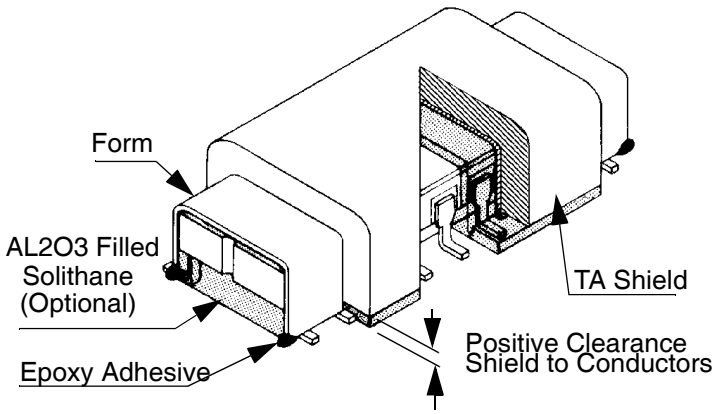

Figure 3.14-22 DIP Radiation Spot Shield

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Table 3.14-1 Radiation Shields

Case Type	Shield Type	Drawing Numbers	Material (Inch)
TO 5	Figure 3.14-20	10076662	0.10 Pb[1] 0.10 W[2] 0.05 Pb
TO 18	Figure 3.14-20	10076661	0.10 Pb 0.10 W 0.05 Pb
TO 99	Figure 3.14-20	10076660 (with modifications, 10079610)	0.10 Pb 0.10 W 0.05 Pb
Flat Pack	Figure 3.14-21	ST11999 ST11913/ST11914 (with modifications, 10078840); 10081107	- 0.04 Ta[3]
Round Form	Deleted		
Rectangular Form	Deleted		
DIP Shield Top Bottom Sides	Figure 3.14-22	ST11994 ST11995 ST11996 - ST11997is a combination of st11994 and ST11995	 0.07-0.08 Ta 0.04 Ta 0.06-0.07 Ta

1. Pb = Lead
1. W = Tungsten
1. Ta = Tantalum
1. EG = Epoxy Glass

* Aluminum Equivalent

1.2.3.11 Shock/Vibration Isolation Mounting of Components. Components requiring shock and vibration isolation shall be mounted to an approved isolator with a contact bonding material per JPL D-8208, Section 3.17 (Figures 3.14-23 and 3.14-24).

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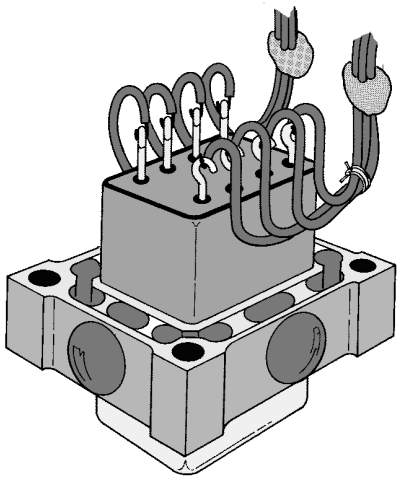

Figure 3.14-23 Shock/Vibration Isolation - Rectangular Mount (10063945 [3SBM])

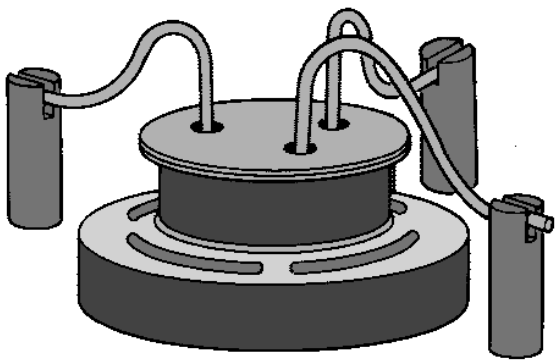

Figure 3.14-24 Shock/Vibration Isolation - Circular Mount (10063935 [TO-5])

1.3 Solder Joint Requirements

1.3.1 Parts and Materials.

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1.3.1.1 Solder Selection. Solder composition used on flight hardware shall be either Sn60 or Sn63 in accordance with NASA-STD-8739.3 w/ Change 2.

1.3.1.2 Component Protection. Thermal shunts shall be used to protect components that may be damaged by the tinning and soldering process: axial and radial parts, transistors, op amps, fuses, signal transformers, oscillators, etc. Thermal shunts shall be of such material, size, shape and design to permit rapid application and removal with minimum interference to the soldering procedure and to facilitate rapid heat dissipation from the area being soldered.

1.3.1.3 Components. Electronic components shall have solderable terminations.

1.3.1.4 Solder Joint Design. Flat lead lap joints shall be designed for a minimum shear strength of 3 lbs.

1.3.1.5 Terminals Selection. Hot dipped, tin-lead coated, hot reflowed, or electro-deposited tin-lead solder terminals shall be used.

2 FABRICATION REQUIREMENTS

2.1 Component Mounting/Soldering Requirements.

Component mounting and soldering requirements are listed in para. 1.2.3.1. Note that other requirements such as polymerics, ESD and cleaning are addressed in Sections 3.16 and 3.17 of this document.

2.2 General Procedures and Requirements.

2.2.1 General Procedures and Requirements. The following are applicable procedures and requirements.

2.2.1.1 Equipment.

a. Daily Inspection. Tools shall be checked daily for proper condition, operation, performance, and cleanliness.

b. Calibration. A calibration plan shall be in place to assure that all equipment and tools are certified to perform operations in a reliable, reproducible manner, such that the items produced will meet the requirements of this document.

c. Calibration Intervals. Calibration intervals shall be based on the type of tool or equipment, the performance criticality, and the reproducibility of its function.

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d. Calibration Records. The calibration plan and recorded history of certification of equipment and tools shall be available for inspection.

e. Soldering Iron Tips. Soldering iron tips shall be controlled to 315°C ± 20°C (600°F ± 35°F) except in special applications specified in the assembly drawings. Soldering iron tips shall be free of oxides during use.

f. Solder Pot. For general usage of Sn60 or Sn63 solder, the solder pot temperature shall be controlled at 260°C ± 20°C (500°F ± 25°F). Solder pots shall meet the voltage and resistance to ground requirements (2 V and 5 Ω, respectively) listed per FP513414 for soldering equipment.

g. Wire Stripper Requirements. Wire strippers shall meet the maximum tip voltage and resistance to ground requirements (2 V and 5 Ω, respectively) per FP513414 for soldering equipment.

2.2.1.2 Materials.

a. Flux. Flux shall be type R or RMA per NASA-STD-8739.3 w/ Change 2.

b. Solder Preforms. Use of solder preforms shall be approved by the procuring NASA installation.

2.2.1.3 Lead Forming.

a. Nicks, Cracks and Deformation. Nicks, cracks, and other deformations which expose base material is prohibited.

b. Toe-Up/Toe-Down Requirements. Toe-up/toe-down greater than 0.005 inch is prohibited.

c. Hermeticity Testing. After forming and trimming, hermetically sealed integrated circuits with lead egress directly from the package cavity and DIPs shall be tested for leaks per MIL-STD-883, Method 1014.10, fine and gross.

2.2.1.4 Terminal Mounting.

a. Plated Through Hole Mounting. Use of terminals mounted in plated through holes shall be approved by procuring NASA installation. In such cases, terminals shall be installed using a flared flange swage.

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b. Lead Wrap-around. Leads and wires are not required to be mechanically secured in bifurcated terminals, provided they meet the requirements of Figure 3.14-16. Lead wrap around turret terminals shall meet the requirement of Figure 3.14-13 on page 3.14-12**.**

c. Lead Length Requirements. The minimum lead length from component body, solder seal or butt weld of the lead to the near edge of the terminal shall be twice the diameter (2D) but not less than 0.050 inches as shown in Figure 3.14-1.

2.2.1.5 Alignment Requirements.

a. Lead Side Overhang. For surface mounted parts with lead pitch 0.050 inches a greater (including chip components), lead side overhang is not allowed. Part leads shall be at least coincident with the side of the pad.

b. Lead Toe Overhang. For gull wing leads (i.e., lap joints), lead toe overhang shall not exceed 0.010 inches or 10% of the lap joint length, whichever is less.

2.2.1.6 Wire & Cable Preparation.

a. Damaged Strands. No broken strands are allowed after wire stripping.

b. Wire-lay. The lay of the wire shall be undisturbed by the stripping process. No bird-caging is allowed.

c. Damaged Insulation. There shall be no punctured, crushed, or otherwise damaged conductor insulation or blistered or swollen wire insulation from thermal stripping.

2.2.1.7 Other Requirements.

a. Chip Component Stacking. Chip component stacking is not allowed.

2.2.1.8 Tinning. Prior to installation, component leads and wire shall be tinned in accordance with the following requirements:

a. All soldered surfaces are smooth and completely wetted with solder.

b. Lack of projections, bridging, porosity, and inclusions.

c. No flux residue after the cleaning process.

d. Insulation of wires shall not be damaged by the tinning operation.

e. The lay of the wire shall be undisturbed by the tinning process.

f. Solder cups shall be tinned using a soldering iron.

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2.2.1.9 Gold-plated Leads and Terminals. Gold shall be removed from component leads and terminals by immersion in a dedicated solder bath prior to tinning (double tinning process) per the following requirements:

a. The lead shall be immersed in a dynamic bath, or with slow movement through a static bath for 2-5 seconds.

b. Gold contamination in the first solder bath shall be less than 4%.

2.2.1.10 Terminal Soldering.

a. Terminal Modification. Any modification of the terminals and conductors shall be prohibited.

b. Bifurcated Terminal. The lead or wire shall enter the terminal at 90° ± 15° to the plane of the tines and shall meet the preferred solder profile as shown in Figure 3.14-16 on page 3.14-14.

c. Turret Terminal. Turret terminal solder joints shall meet the mechanical requirements and solder profile as depicted in Figure 3.14-14 on page 3.14-13.

d. Hook Terminal. Hook terminal solder joints shall meet the mechanical requirements and solder profile as depicted in Figure 3.14-13 on page 3.14-12.

e. Eyelet Terminal. Eyelet terminal joints shall meet the mechanical requirements and solder profile as depicted in Figure 3.14-15 on page 3.14-13.

2.2.1.11 Solder Connection Requirements. The soldered connections shall meet the following requirements.

a. Solder Fillets. A concave fillet of solder shall exist between the conductor and the termination. Soldered conditions shall indicate wetting and adherence where the solder blends to the soldered surface by forming a contact angle of 45 degrees or less, except when the configuration and quantity of solder results in a contour which extends over the edge of the land.

b. PWB Damage. Blistering or delamination which bridges 50% of the distance between plated through-holes or between subsurface conductors, or extends 50% of the distance under surface/subsurface conductors and other subsurface conductors is cause for rejection.

c. Component Damage. Damage to components beyond the allowance of the procurement specification is prohibited.

d. Stressed Solder Joints. Stress lines in solder joints are not acceptable.

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2.2.1.12 Soldered Connections for Lap Joints (Gull Wing Leads). Lap joint connections shall meet the following requirements:

a. Lap joints (both flat and round lead) shall have a complete fillet for a minimum of 75% of the joint periphery.

b. Lap joints shall have a complete heel fillet.

c. Lap joint solder fillets shall not extend into the top bend. Maximum heel fillet shall be one-half the lead bend height (Figure 3.14-25).

2.2.1.13 Rework and Repair. Rework and repair shall be in accordance with JPL D-8208, Section 3.15.

2.2.1.14 Flux Selection. Noncorrosive core solder flux and liquid rosin base flux used for tinning and soldering shall be Type R or Type RMA.

3 QUALITY ASSURANCE PROVISIONS

3.1 Approval and Reviews

The procuring NASA installation reserves the right to review critical items both prior to PWB assembly and during assembly operations. In addition, where applicable the workmanship requirements of NASA-STD-8739.3 w/ Change 2 (December 1997), *"Soldering Electrical Connections,"* shall be employed.

3.2 Acceptance Criteria

Solder joint acceptance criteria are listed in Sections 2.2.1.11–2.2.1.12.

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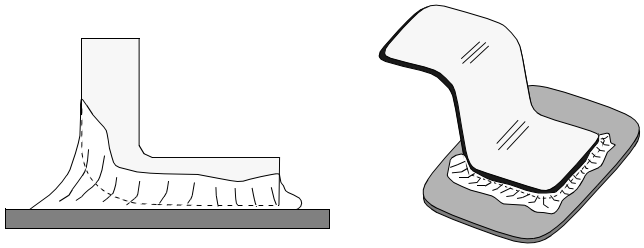
Flat Lead



Round Lead

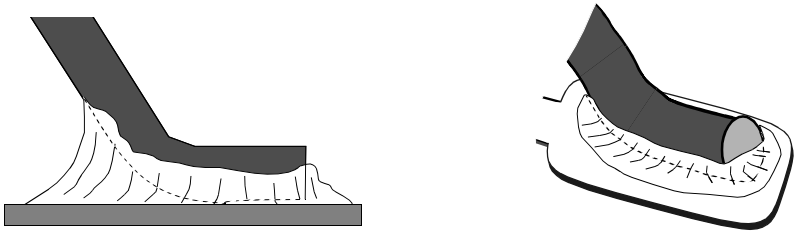


Figure 3.14-25 Lap Joint

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Rework, Modification, and Repair

1 DESIGN REQUIREMENTS

1.1 General Requirements

1.1.1 Polymeric Rework/Modification/Repair Process Requirements. All polymerics rework/repair processes shall meet the requirements of JPL D-8208, Section 3.17 of this document.

1.1.2 Non Standard Rework/Modification/Repair. When the supplier intends to use processes, materials, or parts not covered by this publication, the supplier shall document the details of fabrication and inspection, including acceptance and rejection criteria, and shall provide appropriate test data. Such documentation shall be approved by the procuring NASA installation prior to use.

2 REWORK, MODIFICATION, AND REPAIR REQUIREMENTS

2.1 General Requirements

Rework, modification and repair processes shall not incur further damage to components, PWBs or assemblies. Rework, modification, and repair processes shall not significantly decrease the reliability of the subject hardware.

2.2 Rework/Modification Requirements

Rework and modification is permissible unless excluded by other provisions of the contract. All rework and modification shall meet the requirements of this publication. Modification(s) shall be documented on the applicable fabrication and assembly drawings.

Rework is not repair. Repair shall be made only in compliance with Subsection 2.2

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2.2.1 Acceptable Rework/Modification Procedures. All rework/modification procedures are listed below. These procedures are acceptable for use as modified by the additions/exceptions listed below.

Subsection	Procedure Title	Exception/Modification
3.2.2	Coating Removal - Peeling Method.	Use an wooden orange stick instead of a heated, dull blade.
3.3.1B	Preparation and Conditioning - Baking.	Temperatures are specified by Project and Cog E.
3.4	Legend Marking.	Use marking inks listed in JPL D-8208, Section 3.17.
4.2.8	Conductor Pattern, Deleting Surface Printed Conductor Pattern.	Cut edges shall be subsequently bonded to the printed wiring board using Eccobond 55/9 per JPL D-8208, Section 3.17.
5.5.1	Solder Removal, Surface Solder Wicking Method.	Preflux with type R, use wicking braid and solder tip with appropriate geometry. Clean per JPL D-8208, Section 3.16.
5.2.2	Conductor Pattern, Surface Insulated Jumper Wire, Solder Side.	Do not use rubber erasers during this procedure. If used, adhesive tape shall meet ESD requirements as specified in JPL D-1348. Use only approved solvents/procedures for cleaning. Stake wires per JPL D-8208, Section 3.17.
5.2.3	Conductor Pattern, Surface Insulated Jumper Wire, Component Side.	Do not use rubber erasers during cleaning or this procedure. If using adhesive tape, it shall meet ESD requirements as specified in JPL D-1348. Solder joint on solder side shall not be disturbed. Use only approved solvents/procedures for cleaning. Stake wires per JPL D-8208, Section 3.17.
5.2.4	Conductive Patterns, Jumper Wires, Lap Soldered, Component Side.	If used, adhesive tape shall meet ESD requirements as specified in D-1348. Use only approved solvents/procedures for cleaning. Stake wires per JPL D-8208, Section 3.17.

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Subsection	Procedure Title	Exception/Modification
5.4.1	Component Replacement, Surface Mounted Devices, Long Leaded.	Do not tack down component body unless specified on the assembly drawing. Do Not hold any part of the lead down during soldering operations.
5.4.2	Component Replacement, Surface Mounted, Short Leaded Components.	Do not tack down component body unless specified on the assembly drawing. Do Not hold any part of the lead down during soldering operations.
5.5.2	Coating Replacement, Conformal Coating.	Coating shall be replaced using the brush application method. Polymerics application shall be per JPL D-8208, Section 3.17.

2.2.2 Conditionally Acceptable Rework/Modification Procedures. All rework/modification procedures are listed below. These procedures shall be approved by the procuring NASA installation prior to use and may be acceptable given the exceptions/additions noted below.

Subsection	Procedure Title	Exception/Modification
3.2.1	Coating Removal - Solvent Method.	Use only approved solvents. Solvent shall not cause damage to the manufactured article during or after the rework process. Procedures must limit exposed area.
4.1.2.1	Printed Wiring Board Bow and Twist.	Do not exceed 116°C (240°F) for this procedure. This procedure may be performed only one time.
5.1.10.1	Component Removal and R&R, SMD, Leaded or Leadless, Hot Air Method.	Equipment used shall be approved by the procuring NASA installation. Use only approved solvents/procedures for cleaning.

2.3 Repair Requirements

2.3.1 General Repair Requirements.Repair procedures shall be approved by the procuring NASA installation.

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2.3.2 Acceptable Repair Procedures. These repair processes are generally acceptable for use (as modified below).

Subsection	Procedure Title	Exception/Modification
4.2.1.1	Liquid Adhesive under Conductor.	Use Eccobond 55/9 per JPL D-8208, Section 3.17.
4.2.1.3	Liquid Adhesive around Conductor.	Use Eccobond 55/9 per JPL D-8208, Section 3.17.
4.2.6.1	Conductor Pattern, Surface Jumper Wire.	Use only approved solvents during cleaning operations (do not use rubber eraser to clean wire). Do not flatten wire.
4.3.1.1	Partially Delaminated Land on Printed Boards and Assemblies, Unsupported Holes.	Remove solder per JPL D-8208, Section 3.14. Adhesive shall be Eccobond 55/9 per JPL D-8208, Section 3.17.
4.4.1.1	Printed Contact Replacement, Liquid Adhesive, Lap Joint Joining Method.	Use Circuit Interrupt Pad (CIP) instead of printed contact. CIP shall be bonded to the PWB using Eccobond 55/9 adhesive per JPL D-8208, Section 3.17. Electrical connections to the CIP shall be made using surface jumper wires (haywires).
4.1.5.1	Shallow Base Material Replacement.	This procedure may be used only when the damage does not extend or affect internal PWB Layers.

3 QUALITY ASSURANCE PROVISIONS

3.1 General Quality Assurance Requirements

All modified hardware (reworked, modified or repaired) shall meet the applicable requirements of JPL D-8208. Rework, modification and repair processes shall not incur damage to components, PWBs, or assemblies.

3.2 Rework/Modification Requirements

All rework and modification shall meet the requirements of the applicable fabrication and assembly drawings.

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Cleaning

1 Appropriate Cleaning Guidelines and Documents

The following documents shall provide cleaning guidelines:

- ANSI/IPC-CH-65 (December 1990), "*Guidelines for Cleaning Printed Boards and Assemblies*."
- ANSI/IPC-SC-60 (April 1987), "*Post Solder Solvent Cleaning Handbook*."
- ANSI/IPC-SA-61 (July 1995), *"Post Solder Semiaqueous Cleaning Handbook*."
- ANSI/IPC-AC-62 (December 1986), *"Post Solder Aqueous Cleaning Handbook*."
- IPC-TR-580 (October 1989), "*Cleaning and Cleanliness Test Program Phase 1 Test Results*."

2 Scope

The requirements contained herein are applicable to the following areas:

- Electronics fabrication (manual assembly)
- Electronic fabrication (SMT)
- Cabling fabrication (cable and harness assembly)
- Hybrid microelectronic fabrication.

3 Design Requirements

3.1 Performance Class

The performance class shall be Class 3 (High Reliability Electronic Products).

3.2 Design Rule Exceptions

3.2.1 Standoff Height. For all active leaded surface mount components, the minimum standoff height after soldering shall be 0.005 inch. The preferred standoff height is 0.010 inch.

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3.3 Materials for Cleaning

3.3.1 Ozone Depleting Chemicals. The chemical cleaning agent shall not be an ODC such as the following:

- Trichlorotrifluoroethane, or 1,1,2-trichloro-1,2,2-trifluoroethane, also known as CFC-113, or any solvent constituted with this material.
- Tetrachlorodifluoroethane, or 1,1,2,2-tetrachloro-1,2-difluoroethane, also known as CFC-112, or any solvent constituted with this material.
- Trichloroethane, or 1,1,1-trichloroethane, also know as tri, tric, or TCA, or any solvent constituted with this material.

Exception: TCA shall be suitably stabilized and used in cleaning if it is an acceptable grade and is already stockpiled. A non-ODC shall be substituted when the supply is depleted. TCA in use must conform to O-T-620, Rev. E, "*1,1,1-Trichloroethane, Technical Inhibited (Methyl Chloroform).*"

3.3.2 Approved Cleaning Agents. The cleaning agents approved for the cleaning processes shall be chosen from Table 3.16-1.

3.3.3 Unapproved Solvents. Solvents not listed in Table 3.16-1 shall be submitted to the Electronic Packaging Engineering group for approval.

Table 3.16-1 Solvent Cleaning Agents

Specification (where applicable)	Solvent Material
O-E-760	Ethyl Alcohol (Ethanol)-Type I Grade A (Analytical reagent grade)
TT-I-735	Isopropyl Alcohol (Isopropanol, 2-propanol)
O-A-51	Acetone, Technical Grade
-	Deionized (DI) Water (minimum 1 MΩ resistivity)
-	Vertrel® XMS
-	AK 225T
-	Semiaqueous Material—Terpene-based*
-	Semiaqueous Material—Non-Terpene-based*
*May only be used in suitable semiaqueous cleaning equipment.	

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3.4 Cleaning PWBs Prior to Solder Mask Application

3.4.1 Cleaning PWB During Fabrication. All PWBs shall be cleaned using an approved cleaning agent (Table 3.16-1) and an approved cleaning process (Table 3.16-2) prior to the application of solder masking.

3.4.1.1 Solder Mask Cleaning. For guidelines on cleaning solder mask PWBs, see ANSI/IPC-SM-839 (April 1990), *"Pre and Post Solder Mask Application Cleaning Guidelines*."

3.5 Cleaning of PWAs after Soldering and prior to Conformal Coating Application

3.5.1 Cleaning of the PWA after Soldering and prior to Conformal Coating Application. All PWAs shall be cleaned using an approved cleaning agent (Table 3.16-1) and an approved cleaning process (Table 3.16-2) immediately after the soldering operation and also prior to the application of a conformal coating.

3.5.1.1 Cleaning Guidelines. For guidelines for cleaning PWAs after soldering and also prior to conformal coating application, see:

- ANSI/IPC-SC-60 (April 1987), "*Post Solder Solvent Cleaning Handbook*."
- ANSI/IPC-SA-61 (July 1995), *"Post Solder Semiaqueous Cleaning Handbook*."
- ANSI/IPC-AC-62 (December 1986), *"Post Solder Aqueous Cleaning Handbook*."

3.6 Cleaning of Connectors

3.6.1 Initial Cleaning. Connectors shall be cleaned before being wired. All connectors shall be cleaned using an approved cleaning agent (Table 3.16-1) and an approved cleaning process (Table 3.16-2).

3.6.2 Pigtailed Connectors. Pigtailed connectors shall be cleaned in an ultrasonic cleaner using an approved cleaning agent (Table 3.16-1).

3.6.3 Assembly Mounted Connectors. Connectors mounted on completed assemblies shall be cleaned prior to conformal coating. An acceptable cleaning agent (Table 3.16-1) and an acceptable cleaning process (Table 3.16-2) shall be used.

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3.7 Cleaning of Hybrid Microelectronic Assemblies

3.7.1 Plasma Cleaning Hybrid Microelectronic Assemblies. All hybrid substrates shall be plasma cleaned prior to wire bonding. See Table 3.16-2.

3.7.2 Cleaning Hybrid Microelectronic Assemblies. All hybrid microelectronic assemblies shall be cleaned using an approved cleaning agent (Table 3.16-1) and an approved cleaning processes shall be chosen from Table 3.16-2.

4 FABRICATION REQUIREMENTS

4.1 Cleaning Processes

4.1.1 Approved Cleaning Processes. Cleaning processes shall be chosen from Table 3.16-2.

Table 3.16-2 Cleaning Processes

Name	Description	Application
Aqueous cleaning (AC)	Rinse thoroughly using appropriate equipment. Use a saponifier to remove rosin flux and paste residue then clean and rinse with water.	Generally used prior to the application of solder mask during bare board (PWB) fabrication, immediately after the soldering process, and (3) immediately prior to conformal coating application.
Manual scrub with sodium carbonate solution–This is a specialized method of AC.	Carefully scrub the surface with a suitable brush. Rinse throroghly with a saturated solution of sodium carbonate prepared with DI water and then rinse again with alcohol.	Used to clean hybrid substrates prior to wire bonding to ensure good bondability. This procedure is normally performed prior to die attach to remove gross contamination.
Semiaqueous cleaning (SAC)	Rinse thoroughly using appropriate equipment. Clean with a semiaqueous cleaning agent and rinse with water.	Generally used prior to the application of solder mask during bare board (PWB) fabrication, immediately after the soldering process, and immediately prior to conformal coating application.
Solvent cleaning (SC)	Use an appropriate solvent cleaning agent. See Table 3.16-1 above.	Generally used prior to the application of solder mask during bare board (PWB) fabrication, immediately after the soldering process, and immediately prior to conformal coating application. Can also be used to clean connectors and hybrid microcircuits.

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Table 3.16-2 Cleaning Processes (Continued)

Name	Description	Application
Flow brush–This is a specialized method of SC.	Hold part over Pyrex baking dish, load brush with approved cleaning agent, and wipe over surface. Properly dispose of excess cleaning agent. Use a vented safety hood.	Generally used prior to the application of solder mask during bare board (PWB) fabrication, immediately after the soldering process, and immediately prior to conformal coating application. Can also be used to clean connectors and hybrid microcircuits. This method can be used with fairly large parts.
Immersion brush–This is a specialized method of SC.	Clean workpiece by immersing it in approved cleaning agent contained in a small bottle and applying brush and back and forth to remove residues. Perform in a well ventilated area or under a vented safety hood.	Generally used prior to the application of solder mask during bare board (PWB) fabrication, immediately after the soldering process, and immediately prior to conformal coating application. Can also be used to clean connectors and hybrid microcircuits.
Immersion agitation–This is a specialized method of SC.	Immerse in cleaning agent and manually agitate. Use a vented safety hood.	Generally used prior to the application of solder mask during bare board (PWB) fabrication, immediately after the soldering process, and immediately prior to conformal coating application. Can also be used to clean connectors and hybrid microcircuits.
Syringe flush–This is a specialized method of SC.	Use syringe to saturate area to be cleaned with approved cleaning agent.	Can be used to clean connectors and hybrid microcircuits.
Spray (manual)–This is a specialized method of SC.	Use approved cleaning agent in a painter's spray pot and a hose with a special orifice. Use a vented safety hood.	Generally used prior to the application of solder mask during bare board (PWB) fabrication, immediately after the soldering process, and immediately prior to conformal coating application. Can also be used to clean connectors, hybrid microcircuits, and also equipment such as spray guns used to apply conformal coatings.
Solvent wipe–This is a specialized method of SC.	Use approved cleaning agent and cloth to wipe away debris and contamination. Use a vented safety hood.	Generally used to clean connectors and metal chassis.

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Table 3.16-2 Cleaning Processes (Continued)

Name	Description	Application
Ultrasonics (Sonication)–This is a specialized method of SC.	Immerse part in approved cleaning agent (or DI water) and activate ultrasonic equipment. Use fume hood.	Can be used prior to the application of solder mask during bare board (PWB) fabrication and also to clean special connectors and hybrid microcircuits prior to component mounting.
Degreaser–This is a specialized method of SC.	Use degreaser's wand to spray part with approved cleaning agent.	Generally used prior to the application of solder mask during bare board (PWB) fabrication, immediately after the soldering process, and immediately prior to conformal coating application. Can also be used to clean connectors and hybrid microcircuits. This method can be used with fairly large parts.
Plasma	Expose part, typically a hybrid ceramic substrate, to free radicals of reactive gasses produced in the plasa generating chamber such as Ar/O2.	Generally used to clean hybrid substrates prior to wire bonding to ensure good bondability. This procedure is normally performed after die attach, before wire bonding, to remove contamination resulting from the die attach process.

4.1.2 Aqueous Cleaning (AC). AC using suitable equipment shall be permitted if a saponifier is also used and the process is appropriate to the PWA. For guidelines, see ANSI/IPC-AC-62 (December 1986), *Post Solder Aqueous Cleaning Handbook*.

4.1.3 Semiaqueous Cleaning (SAC). Semiaqueous cleaning shall be permitted. Suitable semiaqueous cleaning equipment shall be used.

4.1.4 Solvent Cleaning (SC). Solvent cleaning shall be permitted. The approved solvents are shown above in Table 3.16-1.

Two (2) solvents have been qualified as acceptable cleaning agents for cleaning, especially for manual cleaning. See Table 2 above.These two solvents are:

- Du Pont's Vertrel® XMS.
- Asahi Glass's AK 225T.

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Both of these solvents are considered acceptable cleaning agents to replace ODCs in all electronic fabrication, cable fabrication, and hybrid microelectronic fabrication applications.

4.1.5 Manual Cleaning in a Static-Sensitive Area. If manual cleaning is performed in a static-sensitive area or near static-sensitive devices, an approved static-sensitive brush or approved engineering equipment must be used.

4.1.6 Centralized Cleaning. It is recommended that a degreaser be used for centralized cleaning to ensure consistency of the cleaning operation. The degreaser, if used, shall be suitable for handling solvents. In addition, the degreaser shall possess features conductive to minimizing solvent losses, such as:

- A minimum of 100% free board area
- A suitable top to avoid the influx of air currents upon removal so that the vapor blanket isn't disturbed.

4.2 PWB Fabrication Cleaning Requirements

4.2.1 Cleaning Prior to Application of Solder Mask. Prior to applying any type of solder masking, the PWB shall be cleaned using an acceptable cleaning agent (Table 3.16-1).

4.2.2 Ultrasonic Cleaning. Ultrasonic cleaning shall be permitted for cleaning bare PWBs having no components.

4.2.3 Ionic Contamination Testing Prior to Application of Solder Mask. After cleaning, but prior to applying any type of solder masking, ionic contamination testing shall be performed and documented for each JPL PWB. A suitable ionic contamination tester shall be used.

4.2.3.1 Ionic Contamination Level. When conducted with a suitable ionic contamination tester, the ionic contamination level shall not exceed 10 micrograms per square inch. If any PWB shows an ionic contamination level equal to or greater than 10 micrograms per square inch, it shall be recleaned until it shows a less than 10 micrograms per square inch. This documentation shall be delivered to JPL along with the finished PWB.

4.2.3.2 Total Area for Ionic Contamination Testing for Bare Boards. The total area, A, shall be the area entered into the ionic contamination tester. In this case, the total area is the same as the board area.

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- The board area = L x W x 2 where L = board length and W = board width. A = (L x W x 2).

4.3 PWA Assembly Cleaning Requirements (Including SMT Assembly)

4.3.1 Cleaning after Soldering. Cleaning after soldering shall be performed within 30 ±5 minutes after the soldering operation. The PWAs shall be cleaned using an acceptable cleaning agent (Table 3.16-1) and an acceptable cleaning process (Table 3.16-2).

4.3.2 Ultrasonic Cleaning. Ultrasonic cleaning shall not be permitted for PWAs having active devices.

4.3.3 Time Window for Performing Cleaning. Cleaning shall be performed within 30± 5 minutes after the soldering operation. If a conformal coating is not applied within 4 ±1 hour, the PWAs shall be stored in a suitable dry box prior to being cleaned before conformal coating.

4.4 Cleaning Prior to Conformal Coating

4.4.1 Cleaning before Applying a Conformal Coating. If a PWA is not conformally coated within 4 ± 1 hour after being soldered and cleaned, it shall be recleaned prior to the application of a conformal coating. The PWA shall be cleaned using an acceptable cleaning agent (Table 3.16-1) and an acceptable cleaning process (Table 3.16-2).

4.4.2 Ultrasonic Cleaning. Ultrasonic cleaning shall not be permitted for PWAs having active devices.

4.4.3 Ionic Contamination Testing Prior to Conformal Coating. After cleaning, but prior to applying any type of conformal coating, ionic contamination testing shall be performed for each JPL PWA and suitably documented. A suitable ionic contamination tester shall be used.

4.4.3.1 Ionic Contamination Level. The ionic contamination level shall not exceed 10 micrograms per square inch. The approximate area of the components shall also be accounted for in computing the board area (see 4.4.3.2). If any PWA shows an ionic contamination level equal to or greater than 10 micrograms per square inch, it shall be recleaned until it shows a less than 10 micrograms per square inch. This documentation shall be delivered to JPL along with the finished PWA.

4.4.3.2 Total Area for Ionic Contamination Testing for Completed Assemblies. The total area, A, shall be the area entered into the ionic contamination tester. The approximate area of

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the components shall be accounted for in computing the total area to be entered into the ionic contamination tester.

- The board area = L x W x 2 where L = board length and W = board width.
- C = Estimated component area.
- A = Total area.
  A = (L x W x 2) + C.

4.5 Connector Cleaning

4.5.1 Solder-Type Connector Cleaning. Soldered connectors should be cleaned prior to soldering. If ultrasonics is available, this is the process of choice. Connectors which are soldered using an acceptable flux (RMA-type) should be cleaned using an acceptable cleaning agent (Table 3.16-1) and an acceptable cleaning process (Table 3.16-2).

The rear-insert solder connections and shell shall be cleaned. Cleaning should be performed within 30± 5 minutes after the soldering operation. If this is not feasible, clean as soon as possible. If ultrasonics is available, this is the process of choice.

4.5.2 Pigtailed Solder Connector. All soldered pigtail connectors shall be cleaned by a suitable process (Table 3.16-2) and one of the methods (Table 3.16-1).

4.5.3 Crimp Connectors. Crimp connectors shall be cleaned using only ethyl alcohol (see Table 3.16-1) and one of the methods of Table 3.16-2.

4.5.3.1 Pigtailed Crimp Connectors. All pigtailed crimp connectors shall be cleaned by a suitable process (Table 3.16-2) using an acceptable cleaning agent (Table 3.16-1).

4.5.3.2 Post-Cleaning Protection. All pigtailed connectors shall be covered or mated after cleaning.

4.5.4 Cabled Connectors.

4.5.4.1 Fixture Mounted Connectors. After all connectors in the harness subassembly have been terminated, the rear-insert area shall be cleaned using an acceptable cleaning agent (Table 3.16-1) and an acceptable cleaning process (Table 3.16-2) prior to potting or sealing. Fixture mounted connectors are not to be demated before potting.

4.5.4.2 Post-Potting. After potting, the mating faces shall be cleaned using an acceptable cleaning agent (Table 3.16-1) and an acceptable cleaning process (Table 3.16-2).

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4.5.4.3 System Harnessing Connectors. After all connectors in the harness have been terminated, demated, and the rear-insert cleaned, the mating faces shall be cleaned using an acceptable cleaning agent (Table 3.16-1) and an acceptable cleaning process (Table 3.16-2) prior to potting or sealing.

4.5.4.4 Harness Immersion. This process should only be used when required by engineering or drawing and documented. Ultrasonics shall be used only if the pigtails or breakout cables or the entire harness can be immersed in the ultrasonics bath. An acceptable cleaning agent (Table 3.16-1) shall be used.

4.5.4.5 Adapter and Portable Cables. Connectors, on cables which are removed from the fixture, or mock-up, shall be cleaned using an acceptable cleaning agent (Table 3.16-1) and an acceptable cleaning process (Table 3.16-2).

Cable as a Pigtailed Connector. If the cable meets the definition of a pigtailed connector and is in the pre- or post-potting cycle, the cable shall be cleaned per an acceptable cleaning agent (Table 3.16-1) and an acceptable cleaning process (Table 3.16-2).

4.5.4.6 Cable as a Non-pigtailed Connector. If the cable does not fit the definition of a pigtailed connector and is in the pre- or post-potting cycle, the cable and the mating faces shall be cleaned using an acceptable cleaning agent (Table 3.16-1) and an acceptable cleaning process (Table 3.16-2).

4.5.4.7 Coaxial Connectors. Coaxial connectors shall be cleaned using ethyl alcohol and an acceptable cleaning process (Table 3.16-2).

4.5.5 Flexprint Connectors.

4.5.5.1 Prepot. After the connector has been soldered to the flexprint cable, the connector shall be cleaned using an acceptable cleaning agent (Table 3.16-1) and an acceptable cleaning process (Table 3.16-2).

4.5.5.2 Dust Caps. The connectors shall be capped or mated with a clean dust cap to maintain cleanliness of the mating face.

4.5.5.3 Postpot. The assembled and potted connector shall be cleaned using an acceptable cleaning agent (Table 3.16-1) and an acceptable cleaning process (Table 3.16-2).

4.5.5.4 Mating Face. The mating face shall be flushed clean using the flow brush method (see Table 3.16-2) with a saturated brush and clean solvent. An acceptable solvent cleaning agent shall be used (Table 3.16-1).

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4.5.5.5 Clean Face. No cleaning shall be required of clean mating faces.

4.5.6 Assembly Mounted Connectors. Connectors mounted on completed assemblies (PWAs) prior to conformal shall be cleaned using an acceptable cleaning agent (Table 3.16-1) and an acceptable cleaning process (Table 3.16-2).

4.6 Hybrid Microelectronic Cleaning

4.6.1 Cleaning Prior to Wire Bonding. All hybrid substrates shall be cleaned prior to wire bonding. Prior to die attach, the method shall be manual scrub with sodium carbonate solution. After die attach, but prior to wire bonding, the method shall be plasma cleaning. If appropriate, solvent cleaning can be performed, typically before plasma cleaning.

4.6.2 Cleaning After Flux Application. If there is flux application, the hybrids shall be cleaned using solvent cleaning. The hybrids shall be cleaned using an acceptable solvent cleaner (Table 3.16-1) and an acceptable cleaning process (Table 3.16-2).

4.6.3 Cleaning the Sealing Surface Prior to Sealing. The sealing surface (seal ring) shall be cleaned prior to sealing. This shall be done with a swab saturated with acetone or alcohol.

4.7 Compatibility of Cleaning Solvents with Various Materials

4.7.1 Solvent Compatibility. The compatibility of the cleaning solvents with various materials is listed in Table 3.16-3 below. The solvent used shall be chosen so as not to degrade the material being cleaned. However, a small amount of swelling shall be allowed provided that the swelling disappears within 5 ± 1 minute after exposure to the solvent.

4.7.1.1 Compatibility Test. A test shall be conducted to verify compatibility of the solvent with the materials of construction of the intended manufactured article prior to the production

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of any manufactured article. The results shall be documented and reviewed with appropriate JPL personnel prior to the production of the intended manufactured article.

Table 3.16-3 Compatibility of Cleaning Solvents with Various Materials

Application	Asahiklin® AK 225T	Vertrel® XMS	Trichlor (TCA)†	Ethyl Alcohol (AE)	Isopropyl Alcohol (IPA)**
PWB Epoxy	E	E	E	E	E
Solithane 113-300	C	C	A	E	E
RTV Silicone	B	B	B	D	D
Polyolefin	E	E	E	E	E
Dialyphthalate	E	E	E	E	E
Magnet Wire Insulation Urethane	C	C	B	D	D
Resistors	E	E	E	E	E
Transistors	E	E	E	E	E
Capacitors	E	E	E	E	E
Integrated Circuits	E	E	E	E	E
Inductors Transformers*	E	E	E	E	E
Diodes	E	E	E	E	E
Connectors w/Silicone Insulator or Gasket	B	B	A-D	E	E

A = Dangerous, will cause failure
B = Will cause damage, extent unknown
C = May cause slight damage
D = Will cause some effect but will not affect function
E = Will not affect or show any change

† This solvent may or may not be available as it is no longer being produced.
* When packaged per JPL D-8208.
** Could leave a residue.

5 QUALITY ASSURANCE

5.1 Acceptance Criteria

ANSI/IPC-CH-65 (December 1990), “Guidelines for Cleaning Printed Boards and Assemblies”, shall be used as acceptance criteria using Class 3 acceptability level.

5.1.1 Visual Inspection. Verification by visual inspection shall be accomplished by use of a suitable microscope.

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5.1.1.1 Electronics Visual Inspection. For PWBs, PWAs, and cable assemblies, inspection shall be performed at 10-30x. There shall be no signs of residues.

5.1.1.2 Hybrid Visual Inspection. For hybrid assemblies prior to sealing, inspection shall be performed using a two-power microscope. Low power 10-60x minimum; high power 60-150x. There shall be no signs of residues. For finer features, or if contamination cannot be identified at a lower power, inspection at a higher power, perhaps even employing SEM, may be required. Consult with an Electronic Packaging Engineer if the latter.

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Polymeric Applications

1 DESIGN REQUIREMENTS

1.1 General Material/Process Requirements

1.1.1 Service Temperature.Unless otherwise specified, all polymeric materials shall have service temperatures in excess of -55°C to +100°C.

1.1.2 Cure Temperature.Unless otherwise specified, all polymeric processes used in the assembly of flight electronics shall have a cure temperature not to exceed 75°C (150°F).

1.1.3 Materials Compatibility.Materials selected shall be non-corrosive and compatible with the component on boards and assemblies. Bonding and coating materials shall adhere/bond to all affected parts and assemblies.

1.1.4 Process Control.All materials/processes shall be capable of consistently meeting the requirements listed in Section 2, “Fabrication Requirements,”

1.1.5 Outgassing/Flammability.All materials shall meet program and contractual outgassing requirements and shall have minimal flammability hazard.

1.1.6 Rework.Materials/processes selected shall have maintainability properties (repair and rework) compatible with the parts and board or other substrate.

1.1.7 Non-standard Processes, Materials, and Parts.When the supplier intends to use processes, materials, or parts not covered by this publication, the supplier shall document the details of fabrication and inspection, including acceptance and rejection criteria, and shall provide appropriate test data.

1.1.7.1 Prior Approval. Such documentation shall be approved by the procuring NASA installation prior to use.

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1.2 Bonding

1.2.1 General Purpose Bonding. System 1 shall be used for general purpose surface bonding per "General Purpose Contact Bonding and Transformer Gap Cement," in Table 3.17-1.

Table 3.17-1 Polymeric Usage

Application	System	Material and Mix Ratio		Cure[2]	Cured Control Sample[3]
		Polymeric	Ratio (pbw)		
Bonding– Potting Boot		Epon 828 Versamid 125	50 ±1.0 50 ± 1.0	16 hrs at 24°C (75°F) or 3 hrs at 54°C (130°F) or 30 minutes at 93°C (200°F)	D-80
Bonding-Electronic Component and Wire Bundles	1	Solithane 113 Catalyst 300 CAB-O-SIL (dry) Thermolite 12	100 ±1 74 ±1 14 ±2 0.036	72 hrs at room temp or 3 hrs at room temp plus 5 hrs at 60°C (140°F) or 3 hrs at room temp plus 6 hrs at 54°C (130°F)	A-55
	2	EC 2216 A EC 2216 B CAB-O-SIL Eccospheres	140 ±1 100 ±1 1.2 12	7 days at room temp or 3 hrs at 60°C (140°F) 2 hrs at 60°C (140°) or 30 minutes at 93°C (200°F) or	A-93 ±3
Conformal Coating	1	Uralane 5750 A Uralane 5750 B Solvent/Thinner	18 ±2 100 ±1 As required	4 hrs at room temp plus 16 hrs @ 58°C (136°F)	-
	2	Solithane 113 Catalyst 300 Thermolite 12 Fluorescent Ind*	100 ±1 74 ±1 0.036 .2	2 hrs at room temp plus 3 hrs at 60°C (140°F)	A-40
Conformal Encapsulant (Dip Daub)		Solithane 113 Catalyst 300 Thermolite 12 CAB-O-SIL (dry) Fluorescent Ind*	100 ±1 74 ±1 0.036 10 ±0.2 .2	72 hrs at room temp or 5 hrs at room temp plus 4 hrs at 54°C (130°F)	A-40

1. Fluorescent indicator is optional.
2. Free of soft areas or tackiness.
3. Specimens being produced to provide proof of cure do not require precuring at room temperature.
4. Shore Hardness per ASTM D-2240.

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Table 3.17-1 Polymeric Usage (Continued)

Application	System	Material and Mix Ratio		Cure[2]	Cured Control Sample[3]
		Polymeric	Ratio (pbw)		
Connector Potting	1	PR1590 A PR1590 B PR1523 Primer	47 ±1 100 ±1	Minimum cure-6 hrs at 82°C (180°F); Full cure-21 days at room temp or 16 hrs at 82°C (180° +5°F)	A-80
		PR1590 A/B	Premix	Thaw at 38°C (100° ±5°F) for 30 minutes.	
	2	CV2510 A CV2510 B CAB-O-SIL	100 ±.5 1 +0 -.1 1.00 ±.05	Minimum cure-24 hrs at room temp; Full cure-7 days at room temp	A-45
Connectors–Sealing Subassy Mnted		CV2510A CV2510B CAB-O-SIL	100 ±.5 1 +0 -.1 1.00 ±.05	Minimum cure 24 hrs at room temp Full cure 7 days at room temp	A-45 or higher
Fastener Bonding		EC2216 A EC2216 B	140 ±1 100 ±1	Minimum cure-24 hrs at room temp; Full cure-7 days at room temp or 3 hrs at 60°C (140°F)	A-93 ±3
Flex Circuit Connector Potting - Sub. D		Solithane 113 Catalyst 300 TiPA (Formulation 12)	100 36.5 7.5	Minimum cure-7 hrs at 54°C (130°F)	70A
Flex Circuit Connector Potting -Micro D		TBS			
General Purpose Contact Bonding and Transformer Gap Cement	1	EC2216 A EC2216 B	140 ±1 100 ±1	Minimum cure-24 hrs at room temp; Full cure-7 days at room temp or 3 hrs at 60°C (140°F)	A-93 ±3
	2	EA 9394 A EA 9394 B	100 17	Minimum cure-24 hrs at room temp plus 1 hr at 93°C (200°F); Full cure-7 days at room temp	D-88 at 77°F
	3	EA9396 A EA9396 B	100 30	5-7 days at room temp or 1 hr at 65°C (150°F)	D-80
	4	StyCast 2850 FT Catalyst 9	100 3.5	16 hrs at room temp	D-90

1. Fluorescent indicator is optional.
2. Free of soft areas or tackiness.
3. Specimens being produced to provide proof of cure do not require precuring at room temperature.
4. Shore Hardness per ASTM D-2240.

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Table 3.17-1 Polymeric Usage (Continued)

Application	System	Material and Mix Ratio		Cure[2]	Cured Control Sample[3]
		Polymeric	Ratio (pbw)		
High Voltage Potting		EN11 A EN11 B	100 ±1 55 ±1	24 hrs at 35°C (95°F) in dry N2 plus 16 hrs at 60°C (140°F) in dry N2	A-65 ±5
		PR420 A PR420 B	5 25	1 hr at room temp	N/A
Marking Ink and Protection Marking Ink Overcoat		Hysol WarnowInk, M Series Catalyst A	20 1	24 hrs at room temp or 1 hr at 60°C (140°F)	N/A
		956 A 956 B	100 58	1 hr at 60°C (140°F) plus 4 days at room temp	D-80
PTH Filling	1	Hysol 1C A Hysol 1C B	100 ±1 43 ±1	24 hrs at room temp or 2 hrs at 60°C (140°F)	See note1.
	2	Armstrong C7/W Part A (Resin) Part B (Activator W)	By weight 1:1	2 hrs at 74C (165°F)	See note1.
PWB Bonding	1	Eccobond 55 Catalyst 9	100 ±1 12 ±.5	24 hrs at room temp or 2 hrs at 65°C (150°F) or 3 hrs at 54°C (130°F)	A-82
	2	Solithane 113 Catalyst 300 TIPA Thermolite 12	100 ±1 65.5 ±1 1.5 0.030	24 hrs at room temp or 12 hrs at room temp plus 4 hrs at 54°C (130°F)	A-40 or higher
	3	Ablefilm 561K	-	2 hrs @ 135°C (275°F)	See note1.
Radiation Shielding		Solithane 113 Catalyst 300 Aluminum Oxide	100 ±1 120 ±1 660 ±.1	72 hrs at room temp or 3 hrs at room temp plus 5 hrs at 60°C (140°F)	A-25 or higher
Spot Terminal Insulation Board Bonding		Eccobond 104 A Eccobond 104 B	100±1 64 ±1	1 hr at 121°C (250°F) plus 3 hrs at 149°C (300°F)	D-80 or higher

1. Fluorescent indicator is optional.
2. Free of soft areas or tackiness.
3. Specimens being produced to provide proof of cure do not require precuring at room temperature.
4. Shore Hardness per ASTM D-2240.

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Table 3.17-1 Polymeric Usage (Continued)

Application	System	Material and Mix Ratio		Cure[2]	Cured Control Sample[3]
		Polymeric	Ratio (pbw)		
Temperature Transducer Bonding	1	Eccobond 66C A Catalyst 9	40 ±1 1	8 hrs at room temp or 4 hrs at 60°C (140°F)	D-80
	2	Solithane 113 Catalyst 300 Thermolite 12	100 ±1 74 ±1 0.036	24 hrs at room temp or 3 hrs at room temp plus 4 hrs at 54°C (130°F)	A-40 or higher
	3	EA901 Catalyst B-1	100 ±1 23 ±1	24 hrs at room temp or 3 hrs at 54°C (130° ±3°F)	See note1.
Thermal Strap Bonding		EC2216 A EC2216 B	140 ±1 100 ±1	24 hrs at room temp or 3 hrs at 60°C (140°F)	A-93 ±3
Thermally Conductive Material	1	Solithane 113 Catalyst 300 Thermolite 12 Aluminum Oxide	46 ±2 35 ±1 0.036 154 ±1	72 hrs at room temp or 3 hrs at room temp plus 5 hrs at 60°C (140°F)	A-25 or higher
	2	Stycast 2850FT Catalyst 11	100 4-5	40 hrs at 60°C(140°F) or 16 hrs at 75°C(167°F) or 2 hrs at 100°C(212°F)	D90-100
	3	StyCast 2850 FT Catalyst 24LV	100 7	16 hrs at room temp	D-85
Thermally & Electrically Conductive Material	1	Eccobond 66C A Catalyst 9	40 ±1 1	8 hrs at room temp or 4 hrs at 60°C (140°F)	D-80
	2	Eccobond 57C A Eccobond 57C B	50 ±1 50 ±1	8 hrs at room temp or 4 hrs at 60°C (140°F)	See note1.

1. Fluorescent indicator is optional.
2. Free of soft areas or tackiness.
3. Specimens being produced to provide proof of cure do not require precuring at room temperature.
4. Shore Hardness per ASTM D-2240.

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Table 3.17-1 Polymeric Usage (Continued)

Application	System	Material and Mix Ratio		Cure[2]	Cured Control Sample[3]
		Polymeric	Ratio (pbw)		
Transformers and Inductors					
Impregnation	1	Scotchcast 235 A Scotchcast 235 B	1 2	16 to 20 hrs at 94°C (200°F)	D-50 or higher
Embedment	1	Scotchcast 241 A Scotchcast 241 B	1 2	16 to 20 hrs at 94°C (200°F)	D-60 or higher
Impregnation	2	Scotchcast 280 A Scotchcast 280 B	2 3	16 to 20 hrs at 94°C (200°F)	
Embedment	2	Scotchcast 281 A Scotchcast 281 B	2 3	16 to 20 hrs at 94°C (200°F)	
Stress Relief		RTV566 A RTV566 B	100 ±1 .1	Minimum cure-24 hrs at room temp; Full cure-7 days at room temp	A-47
UV Radiation Resistant Coating		SS4155 (Primer)	N/A	1 hr at room temp	N/A
		RTV566 A RTV566 B	100 ±1 .1	Minimum cure-24 hrs at room temp; Full cure-7 days at room temp	A-47

1. Fluorescent indicator is optional.
2. Free of soft areas or tackiness.
3. Specimens being produced to provide proof of cure do not require precuring at room temperature.
4. Shore Hardness per ASTM D-2240.

1.2.2 PWB Insulation Board Bonding.

1.2.2.1 Terminals. PWBs and terminal boards mounted to electrically conductive supporting structures with exposed circuitry or terminal swages shall have an insulation board bonded to the non-component side as shown in Figure 3.17-1.

1.2.2.2 Counterbored Terminals. PWBs with counterbore depths that cause the swaged portion of the terminal to be less than 0.050 inch below the surface shall have an insulation board bonded to the noncomponent side as shown in Figure 3.17-3.

1.2.2.3 Type and Thickness. The insulation board shall be laminated glass-reinforced board material of 0.0035 inch minimum thickness.

1.2.2.4 Insulation Board Bonding. The insulation board shall be bonded to the PWB with Eccobond 55/9 and conform to the following:

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a. Non-Standard Materials. Materials other than that listed in Table 3.17-1 shall be capable of producing consistent, uniform, thin bondlines of 0.002 - 0.005 inch.

b. Tensile Strength. The material shall have a minimum of 1,000 psi tensile strength.

c. Counterbore Filling. Counterbored PWBs requiring recessed swaged terminals to be a minimum of 0.050 inch below the board surface shall have the counterbores filled with Eccobond 55/9 as depicted in Figure 3.17-3 prior to being mounted onto a surface.

1.2.3 PWB Bonding. PWBs which require a mounting to a support structure per the assembly drawing shall use System 1 for permanent rigid mounting or System 2 for removable mounting and vibration damping. System 3 shall be used only in VME card cage applications where high processing temperatures are acceptable.

1.2.3.1 Non-Standard Materials. Materials other than that listed in Table 3.17-1 shall be capable of producing consistent, uniform, thin bondlines of 0.007 - 0.010 inch and have a minimum tensile strength of 1,000 psi.

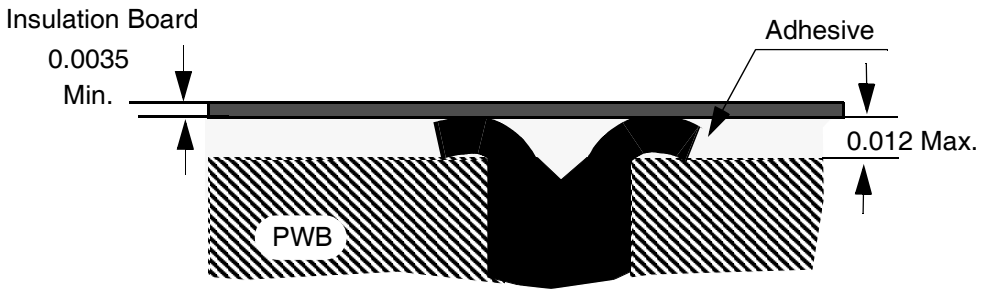

Figure 3.17-1 Backing Board on Exposed Circuitry

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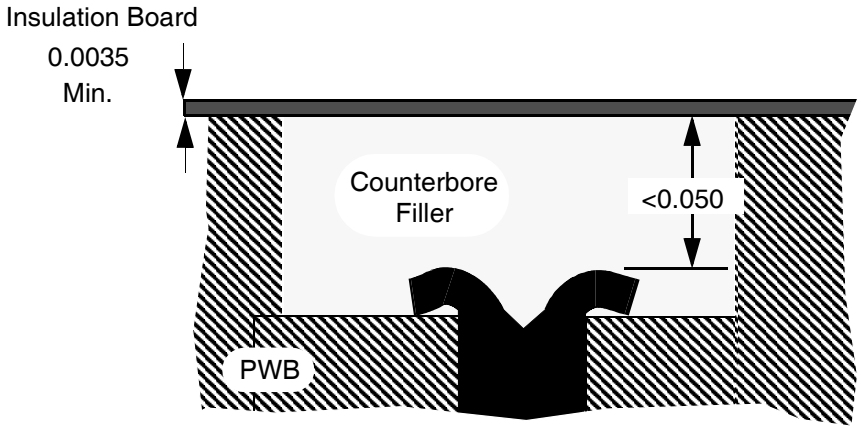

Figure 3.17-2 Swaged Terminal with Insulation Board

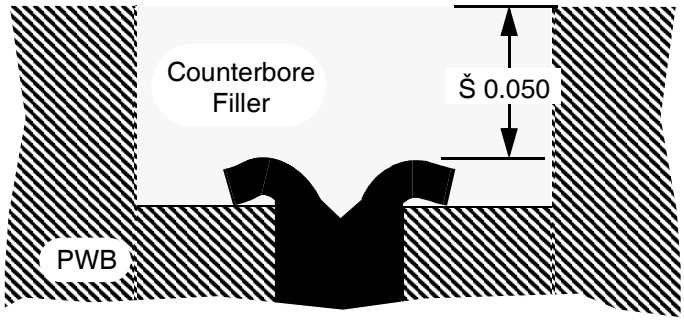

Figure 3.17-3 Counterbore Fill

1.2.4 Electronic Component Bonding/Staking. Electronic components shall be spot bonded as specified in the assembly drawing using material(s) from Table 3.17-1.

1.2.4.1 Small Discrete Components. Electronic components larger than 0.125 inch in diameter, weighing less than 0.10 ounce/lead shall be bonded less than 0.020 inch from the supporting surface with System 1 as listed in Table 3.17-1, “Bonding- Electronic Component and Wire Bundles.”

1.2.4.2 Large Discrete Components. Electronic components weighing more than 0.10 ounce/lead and less than one ounce shall be bonded with System 2 as listed in Table 3.17-1, “Bonding- Electronic Component and Wire Bundles.”

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1.2.4.3 Clamps and Fasteners. Electronic components weighing more than one ounce shall utilize clamps or fasteners and be bonded with System 2 from Table 3.17-1, "Bonding- Electronic Component and Wire Bundles."

1.2.4.4 Non-Standard Materials. Materials other than that listed in Table 3.17-1 shall be capable of meeting the following requirements:

a. Structural Properties. Staking material shall be strong enough to provide adequate mechanical support.

b. Electrical Properties. Staking material shall have dielectric properties (permittivity and dissipation factor) adequate for the particular application.

1.2.5 Wire Bundle Bonding/Staking. Wires or wire bundles shall be spot bonded with material form Table 3.17-1, "Bonding- Electronic Component and Wire Bundles."

1.2.5.1 Wire Bundle Spot Ties. Wherever possible, wire bundles shall be spot bonded over the wire bundle spot ties.

1.2.6 Fastener Bonding. Threaded fasteners which do not utilize an integral locking method shall be spot bonded with material from Table 3.17-1, "Fastener Bonding."

1.2.6.1 Fastener Bonding Configuration. Screw heads, nuts, and other threaded fasteners shall be bonded as shown in Figure 3.17-8.

1.2.6.2 Non-standard Material. Materials other that those listed in Table 3.17-1 shall have sufficient structural properties to resist fastener movement: high-modulus materials are preferred for this application.

1.2.7 Thermally Conductive Material. Applications requiring thermal conductance shall use a bonding material from Table 3.17-1, "Thermally Conductive Material."

1.2.8 Temperature Transducers.

a. Temperature transducers using a mechanical fastener shall use System 1 or System 2 from Table 3.17-1, "Temperature Transducer Bonding," as specified in the assembly drawing.

b. Temperature transducers not using a mechanical fastener shall use System 3 from Table 3.17-1, "Temperature Transducer Bonding,"

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1.2.8.1 Temperature Transducer Bonding. Temperature transducer bonding shall provide support to secure the transducers and minimize the temperature gradient between the transducer and the point-of-temperature measurement.

1.2.9 Radiation Rated Adhesive. Solithane 113/300 shall be used as specified in Table 3.17-1, "Radiation Shielding," to adhesively bond radiation shields and barriers around components.

1.2.10 Bond Lines. Items requiring a uniform bond line shall be bonded as listed in Table 3.17-1, plus 2% pbw glass beads 0.005 inches in diameter per MIL-G-9954.

1.3 Coating

1.3.1 Conformal Coating. Electronic components, leads, PWBs, current carrying conductors, and ground planes shall be conformal coated using System 1 or System 2 from Table 3.17-1, "Conformal Coating," as determined by the following parameters:

a. System 1 is preferred.

b. Modules intended to operate at a temperatures less than -25°C (-13°F) shall be conformally coated using System 1.

c. Board configuration that cannot accommodate spray application of conformal coat materials shall be brushed with System 2.

1.3.2 Non-Standard Materials. Materials other than those listed in Table 3.17-1 shall be capable of meeting the following requirements.

1.3.2.1 Materials Selection. Materials shall be selected from ANSI/IPC-CC-830.

1.3.2.2 Coverage. The conformal coating material and process shall be suited to the complexity of the assembly and be capable of covering all conductive elements (traces, terminals, components) of the assembly.

1.3.2.3 Electrical Properties. The coating material shall have dielectric properties that will meet the minimum circuit requirements in all anticipated environments.

1.3.2.4 Stability. The coating material shall be hydrolytically and thermally stable.

1.3.2.5 Conformal Coating Thickness. Conformal coating thickness shall be a minimum of 0.003 inch and no more than 0.015 inch.

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1.3.2.6 Bridging. The material/process used shall not result in bridging of components to PWB with conformal coating material when the component body is greater than 0.015 inch above the PWB.

1.4 Stress-Relief

A stress-relief coating shall be required whenever fragile components and joint configurations must survive the forces and pressures produced by the potting material.

1.4.1 Stress-Relief Material. Stress relief coatings applied prior to final potting in a rigid material shall be selected from materials listed in Table 3.17-1, "Stress Relief."

1.5 Encapsulation

1.5.1 Conformal Encapsulation. Complete protection and insulation of terminals, electronic components and leads, current carrying conductors and ground planes not obtained by conformal coating shall be conformal encapsulated with material from Table 3.17-1, "Conformal Encapsulant (Dip Daub)."

1.5.1.1 Non-Standard Materials. Materials other than that listed in Table 3.17-1 shall be capable of meeting the following requirements:

a. Electrical Properties. The coating material shall have dielectric properties that will meet the minimum circuit requirements in all anticipated environments.

b. Stability. The encapsulant material shall be hydrolytically and thermally stable.

c. Compatibility. The encapsulant shall be compatible with and adhere to the conformal coating.

d. Viscosity. The uncured encapsulant shall have sufficient viscosity to prevent slumping and exposure of electrical conductors.

1.5.2 Radiation Encapsulation Material. Solithane 13 shall be used as specified in Table 3.17-1, "Radiation Shielding," to encapsulate and provide a radiation barrier for electronic components.

1.6 Sealing

1.6.1 Subassembly-Mounted Connectors. The uninsulated section of the connector pin termination between the connector insert and the base of the shrink tubing, shall be sealed with materials listed in Table 3.17-1, "Connectors– Sealing Subassy Mnted."

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1.6.2 Non-Standard Materials. Materials other than that listed in Table 3.17-1 shall be capable of meeting the following requirements.

1.6.2.1 Electrical Insulation. The sealant material shall provide electrical insulation to exposed portions of the connector pin termination.

1.6.2.2 Sealing. The sealant material shall limit passage of debris and solvents through the connector.

1.6.2.3 Viscosity. The sealant material shall have sufficient viscosity to prevent material wicking into the connector body during cure.

1.7 Impregnating

1.7.1 Material Selection. Transformers and inductors requiring embedment or impregnation and embedment shall use materials from Table 3.17-1, “Transformers and Inductors,”

1.8 Potting

1.8.1 Harness-mounted Connectors. Harness-mounted connectors requiring electrical insulation, moisture protection, or wire support beyond that provided by sealing shall be potted with material from Table 3.17-1, “Connector Potting.”

1.8.2 Flex Circuit Terminated Connectors.

1.8.2.1 Flex Terminated Subminiature D Connectors. Flex circuit terminated, subminiature D connectors shall be potted as shown in “Flex Circuit Connector Potting.” using materials listed in Table 3.17-1, “Flex Circuit Connector Potting - Sub. D.”

1.8.2.2 Flex Terminated Micro D Connectors. Flex circuit terminated micro D connectors shall be potted as shown in Figure 3.17-5 using materials listed in Table 3.17-1, “Flex Circuit Connector Potting -Micro D.”

1.8.3 Circular Connectors. Soldered circular connectors shall be potted with PR1590 A/B (shrink sleeving shall not be used on the solder contacts when potted only with PR1590 A/B).

1.8.4 Other Connectors. Crimped connectors and soldered rectangular connectors shall be sealed with CV2510 and potted with PR1590 A/B.

1.8.5 High-Voltage Potting. High-voltage potting shall be done in a vacuum using material per Table 3.17-1, “High Voltage Potting.”

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1.8.6 Coating Exposed Conductors. Exposed conductors of rigid-flex connectors shall be coated using materials selected from Table 3.17-1.

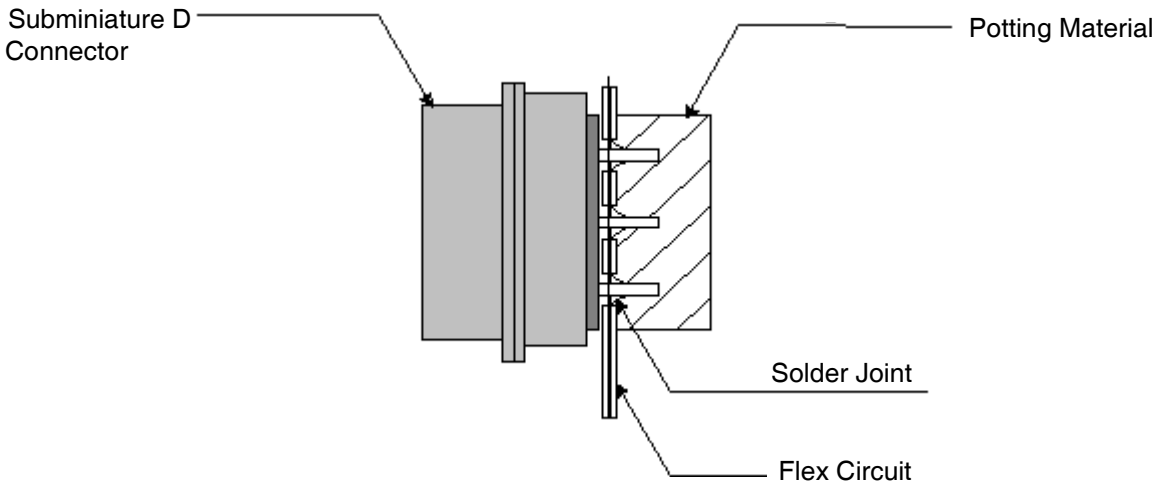

Figure 3.17-4 Flex Circuit Connector Potting

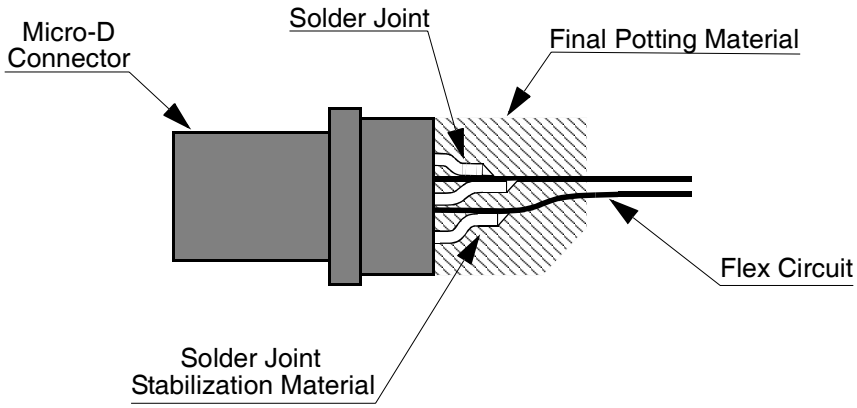

Figure 3.17-5 Potting Rigid-Flex to Connector

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2 FABRICATION REQUIREMENTS

2.1 General Polymeric Materials/Process Requirements

This section contains fabrication requirements for the use of polymeric materials in the assembly of electronic equipment

2.1.1 Material Control.

a. Polymeric materials shall not have exceeded their shelf life at the temperature range specified by the manufacturer.

b. Catalyzed polymers mixed at JPL shall have a 1-year maximum storage at or below -20°C.

c. All polymeric materials used shall be documented on a Mixing Record Sheet, JPL Form 1888 or equivalent.

d. Mixed materials used for embedment, encapsulation, conformal coating, impregnation, and potting shall be vacuum-degassed before application.

e. A minimum of one control sample shall be made from each batch of mixed polymeric materials.

f. Cure conditions shall conform to the requirements of Table 3.17-1.

g. Control samples shall meet the requirements of Table 3.17-1.

h. Cure times shall include the final curing and baking out of volatile condensable materials.

i. Material storage shall be controlled by shelf life stickers attached to each material container.

j. Records of manufacturing date, lot number, and the receiving date of each material shipment shall be maintained.

k. Many materials are hygroscopic or moisture sensitive. Their storage shall be such as to minimize moisture exposure. The isocyanate part of urethane material shall be stored in a dry nitrogen atmosphere whenever possible.

l. If material with an expired shelf life date is tested in accordance with the material specification or approved test procedure and found to be in acceptable condition, the expiration date may be extended provided the extension is less than one-half the original shelf life.

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2.1.2 Cleaning. Cleaning shall be performed prior to application of polymeric materials per JPL D-8208, Section 3.16.

2.1.3 Masking. When required, areas to be kept free of polymerics materials shall be masked with tape, covers, or other suitable masking materials or devices.

2.1.3.1 Masking Tape. Tape used for masking shall conform to the following requirements:

a. Masking tapes shall be ESD-approved (i.e., not generate a discernible charge on either the tape or the mating surface when removed).

b. Masking tapes shall not be placed over electrical components.

2.1.4 Cured Properties. Unless otherwise specified, all cured polymeric materials shall meet the following requirements.

a. The materials shall be free of chips, flakes, dust, and debris.

b. The end product shall be free of uncured material.

c. The material shall be free of cracks, voids, cavities, discolorations, tears, and burns.

d. No bubbles or pinholes greater than 0.025 inch diameter shall be acceptable.

e. No bubbles or series of bubbles shall form a continuous path between two electrically conductive elements.

2.2 Bonding

2.2.1 General Purpose Surface Bonding. This subsection pertains to applications requiring general purpose, nonstructural bonding where the surfaces to be bonded are in contact.

2.2.1.1 Materials. Materials shall be used according to Table 3.17-1, “General Purpose Contact Bonding and Transformer Gap Cement,” and the following requirements:

a. Bonding material consisting of multiple parts shall be thoroughly mixed until a uniform color is obtained.

b. Mixing ratio, cure, and control sample requirements shall conform to those found in Table 3.17-1, “General Purpose Contact Bonding and Transformer Gap Cement.”

c. Bonding material thickness shall be a minimum of 0.006 inch to a maximum of 0.010 inch.

d. Excess material shall be removed from edges of the bonded area.

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e. Smears of adhesive observed on the parts shall be removed.

2.2.2 Insulation Board Bonding. Insulation board bonding shall use System 1 per Table 3.17-1, "PWB Bonding."

2.2.2.1 Insulation Board Bonding Conformance. Insulation board bonding shall conform to the following:

a. Adhesive material shall not interfere with soldering operations on the wiring or terminal board, or with installation of electronic components and mechanical fasteners.

b. There shall be no voids bridging conductive paths, components, conductors and terminal swages or in the counterbore of a terminal swage.

c. All edges and corners shall be bonded firmly to the PWB.

2.2.2.2 Filling Recessed Holes. Counterbored holes shall be filled with Eccobond 55/9 per Table 3.17-1, "PWB Bonding." (See Figure 3.17-3.)

2.2.2.3 Curing Fill Material. The fill material shall be cured prior to bonding the board to the mounting surface.

2.2.3 PWB Bonding. Prior to the installation of components, PWBs shall be bonded to their mounting surface using System 1 or System 2 from Table 3.17-1, "PWB Bonding."

2.2.3.1 PWB Bonding Conformance. Bonded PWBs shall conform to the following:

a. Adhesive material shall be applied so as not to interfere with soldering operations or the installation of components and fasteners.

b. The thickness of the material between the subchassis and the PWB shall be between 0.007 inch and 0.010 inch.

c. All edges and corners shall be firmly bonded to the mounting surface.

2.2.4 Electronic Component Bonding. Electronic component bonding shall be per "Bonding-Electronic Component and Wire Bundles," in Table 3.17-1.

2.2.4.1 Bonded Electronic Components. Spot bonded electronic components shall conform to the following:

a. There shall be no spot bonding of terminals, solder joints, or parts designed to rotate, slide, or perform optical functions.

b. The spot bonding material shall be applied as specified in Figure 3.17-6.

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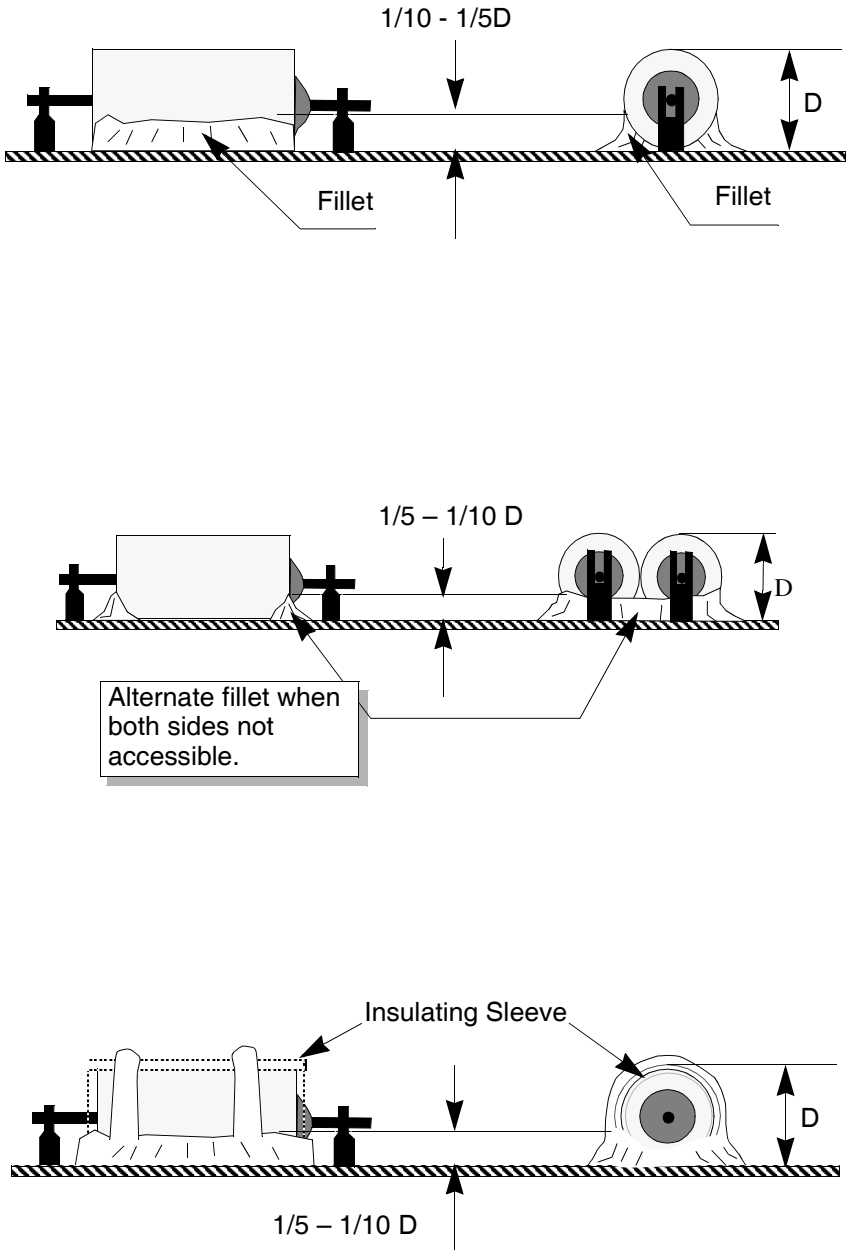

Figure 3.17-6 Spot Bonding Resistors and Capacitors

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2.2.5 Wire Bundle Bonding. Wire bundles shall be spot bonded per "Bonding- Electronic Component and Wire Bundles," from Table 3.17-1.

2.2.5.1 Wire Bundle Bonding Conformance. The wire bundle spot bonding shall conform to the following requirements:

a. Spot-bonding material shall not be applied to terminals or solder joints.

b. Wire bundles shall be spot bonded as shown in Figure 3.17-7.

2.2.6 Fastener Bonding. Fasteners requiring spot bonding shall be bonded using System 1 or System 2 from "Fastener Bonding" in Table 3.17-1.

2.2.6.1 Bonded Fastener Conformance. Spot bonding of fasteners shall conform to the following requirements:

a. There shall be no spot-bonding material applied to terminals or solder joints.

b. Material shall be applied from 25% to 50% of the circumference of the spot bonded fasteners and fastener combinations.

c. Spot-bonding material shall be applied as shown in Figure 3.17-8, not over the slots of screws or bolts.

2.2.7 Thermally Conductive Bonding Material. Bonding for thermal conductivity shall be per "Thermally Conductive Material" in Table 3.17-1.

2.2.7.1 Thermally Conductive Material Conformance. There shall be no thermally conductive material applied to terminals or solder joints.

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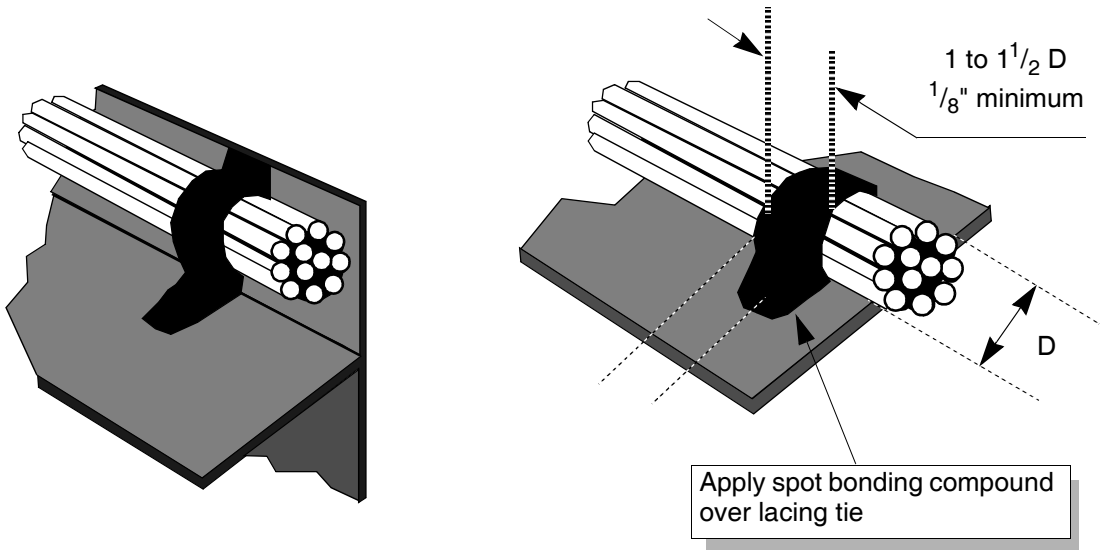

Figure 3.17-7 Wire Bundle Bonding

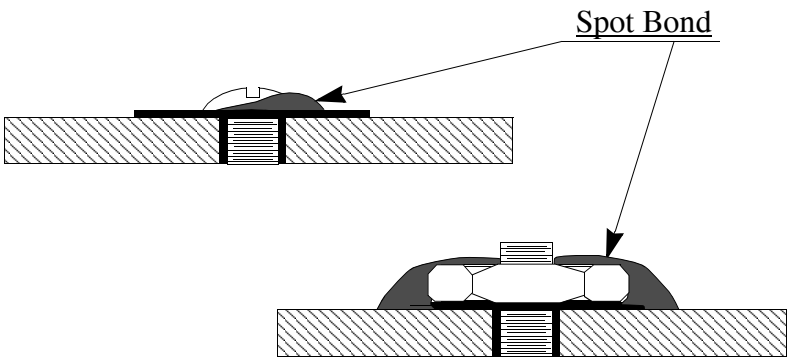

Figure 3.17-8 Fastener Spot Bonding

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2.2.8 Electrically Conductive Bonding Material. Electrically conductive material selected from Table 3.17-1 shall be used for electrical grounding only.

2.2.8.1 Electrically Conductive Bonding Material Conformance. There shall be no electrically conductive materials applied to terminals or solder joints unless the grounding is intentional.

2.3 Coating

2.3.1 Conformal Coating.

2.3.1.1 Material Selection. Conformal coating materials shall be selected from Table 3.17-1, "Conformal Coating," for application to components, leads, PWBs, and other current carrying conductors.

2.3.1.2 Process Requirements.

a. Application Method. Conformal coating shall be applied using spray or brush techniques.

b. Other Application Methods. Dip and pour techniques for applying conformal coating shall be approved by the procuring NASA installation.

2.3.2 Conformal Coating Conformance. The conformal coating shall conform to the following:

a. The conformal coating shall provide 100% coverage of all electrical conductors, including leads, components, and PWB traces as shown in Figure 3.17-9 through 3.17-12.

b. Incomplete or excessive coverage shall be cause for rejection.

c. There shall be no intermixing or overlaying of different material systems or types in an uncured state.

d. The cured coating thickness shall be a maximum of 0.015 inch, exclusive of the fillet areas.

e. There shall be a minimum of 0.010 inch and a maximum of 0.020 inch of coating material between two electrically conductive elements.

f. The maximum acceptable conformal coating thickness, when contacting both the underside of a component and the mounting surface, shall be 0.015 inch.

g. No bridging shall occur when the component body is greater than 0.015 above the PWB.

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h. The use of fluorescent indicator shall be avoided on light-sensitive equipment.

2.3.3 Component Stress Relief Coating. Components, parts requiring a stress relief coating prior to potting in a rigid material, and all transformers with split "C" or "E" cores, shall be coated with the applicable material from Table 3.17-1, "Transformers and Inductors."

2.3.3.1 Component Stress Relief Coating Conformance. The stress relief coating shall completely cover the required areas and not be located on other surfaces.

2.4 Conformal Encapsulating

2.4.1 Material Selection. Thin coatings and bare spots on terminals, electronic components and leads, and other current carrying conductors shall be covered per "Conformal Encapsulant" in Table 3.17-1, "Conformal Encapsulant (Dip Daub)."

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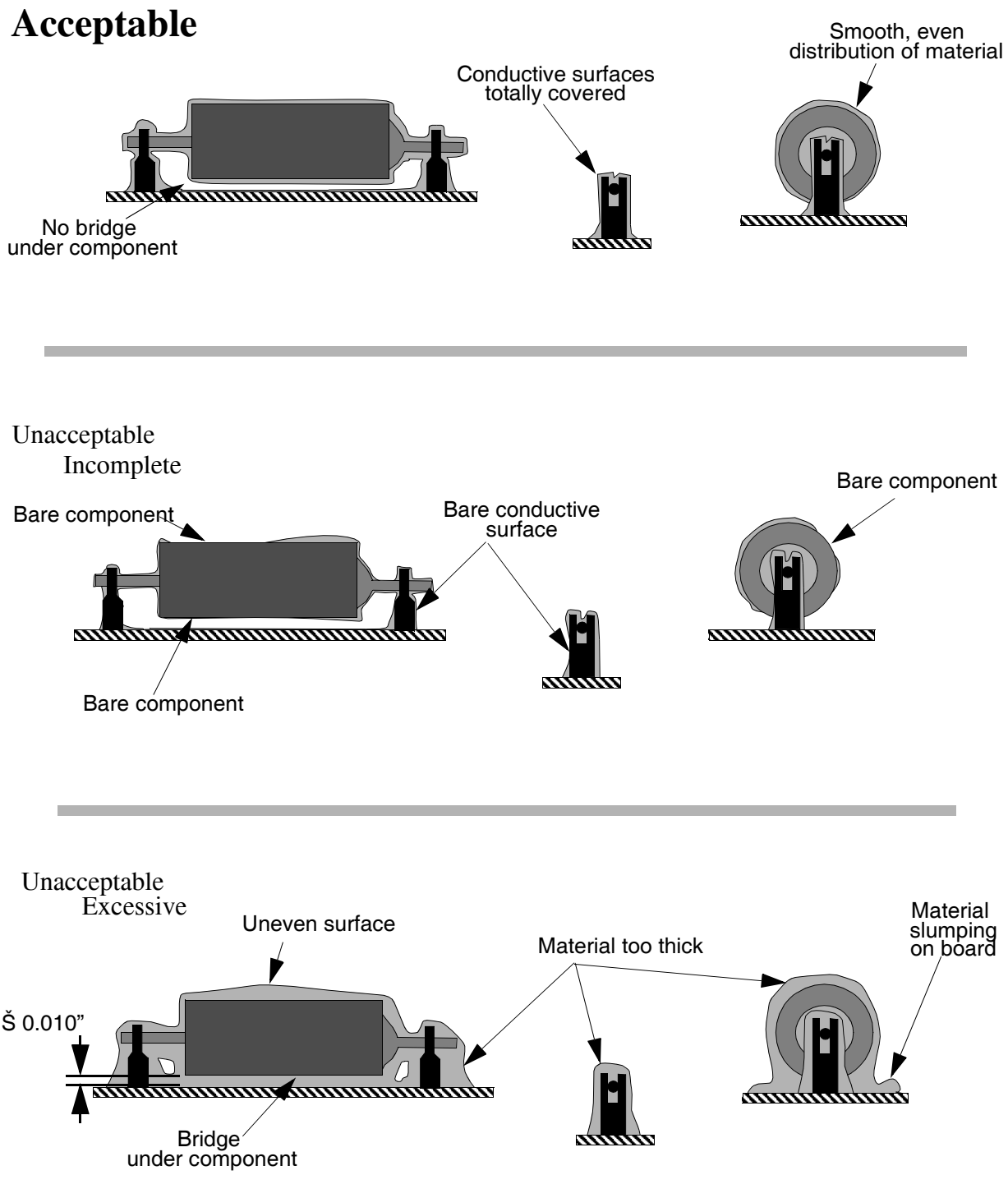

Figure 3.17-9 Axial Component Conformal Coating

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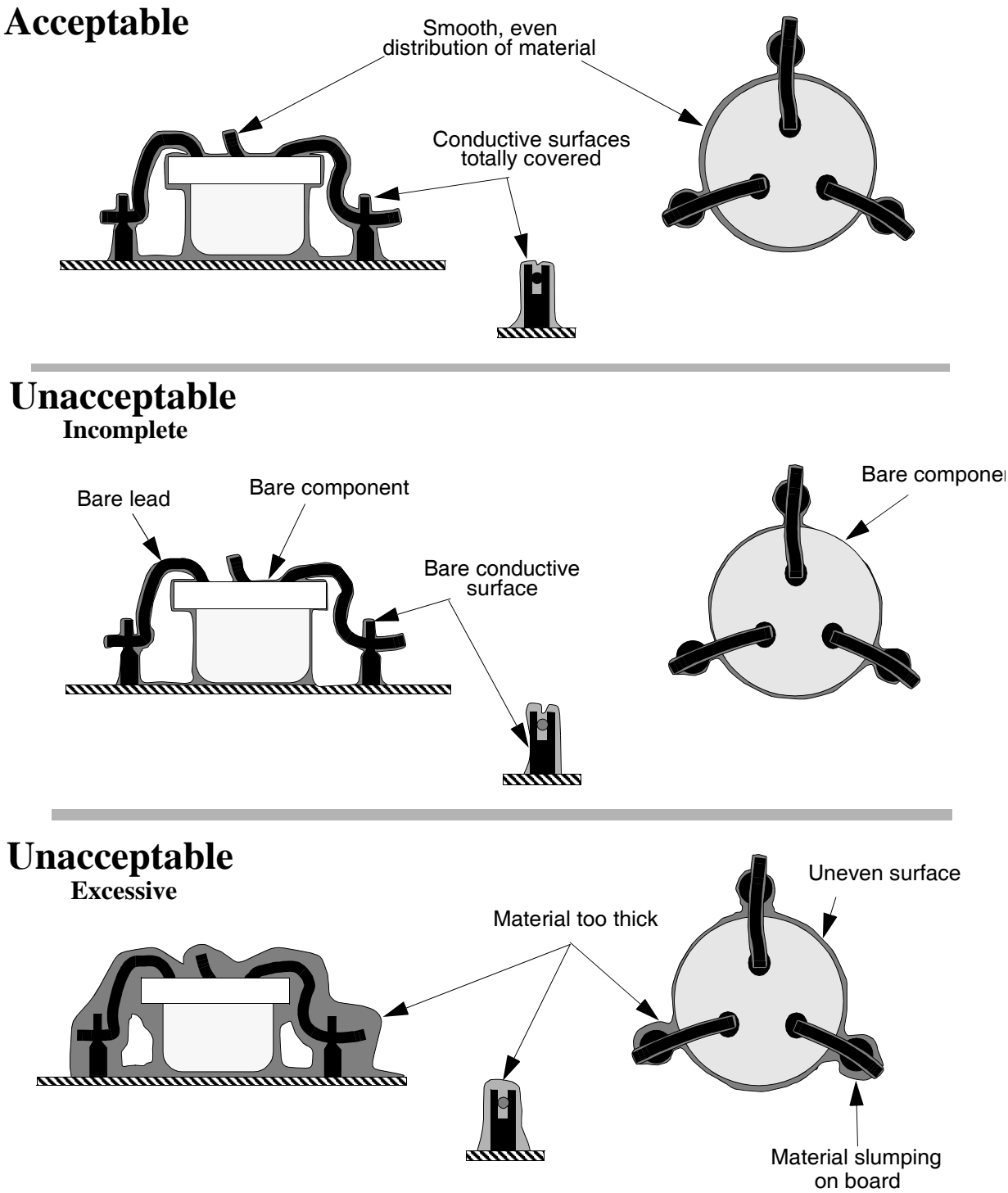

Figure 3.17-10 Transistor Conformal Coating

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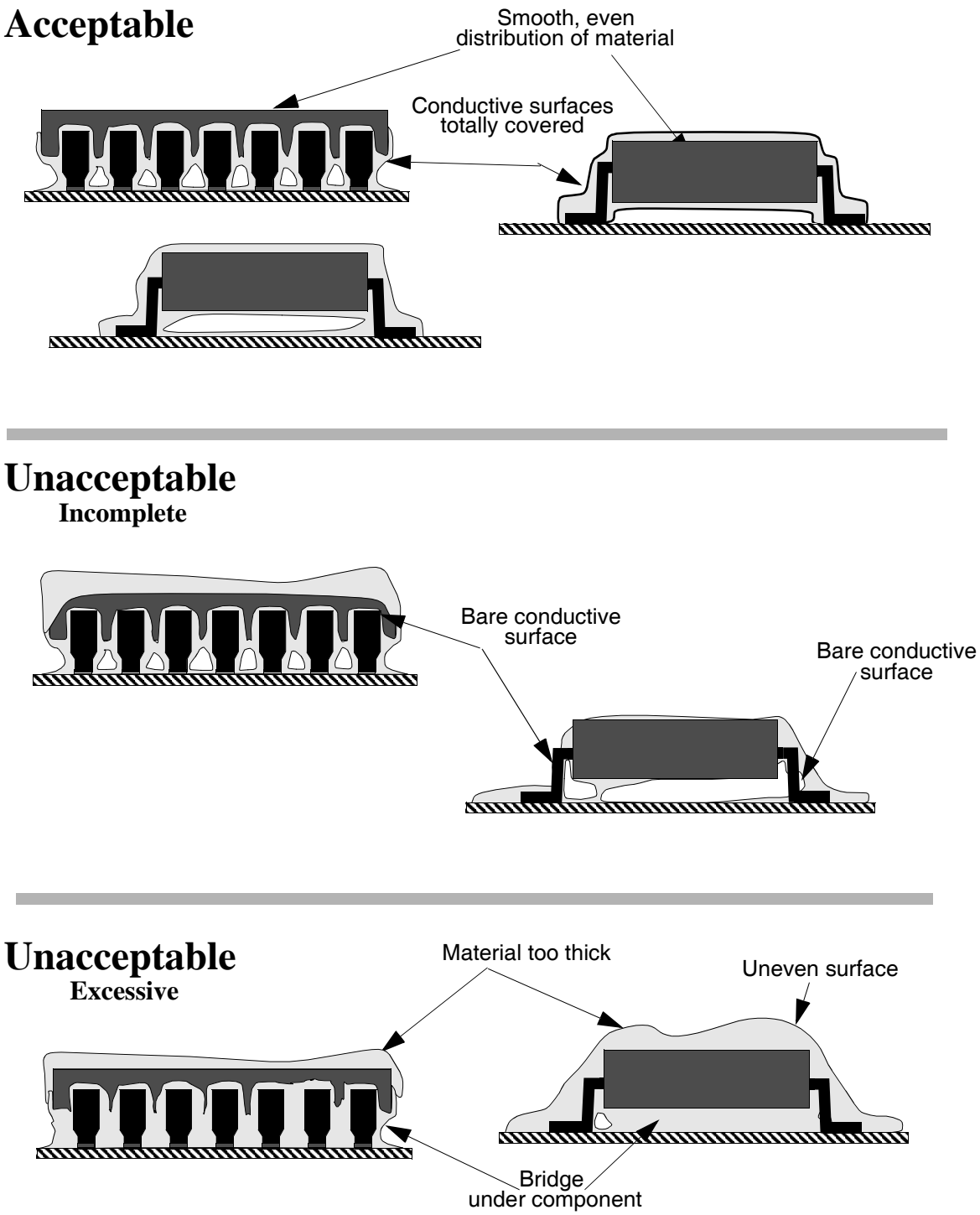

Figure 3.17-11 DIP Conformal Coating

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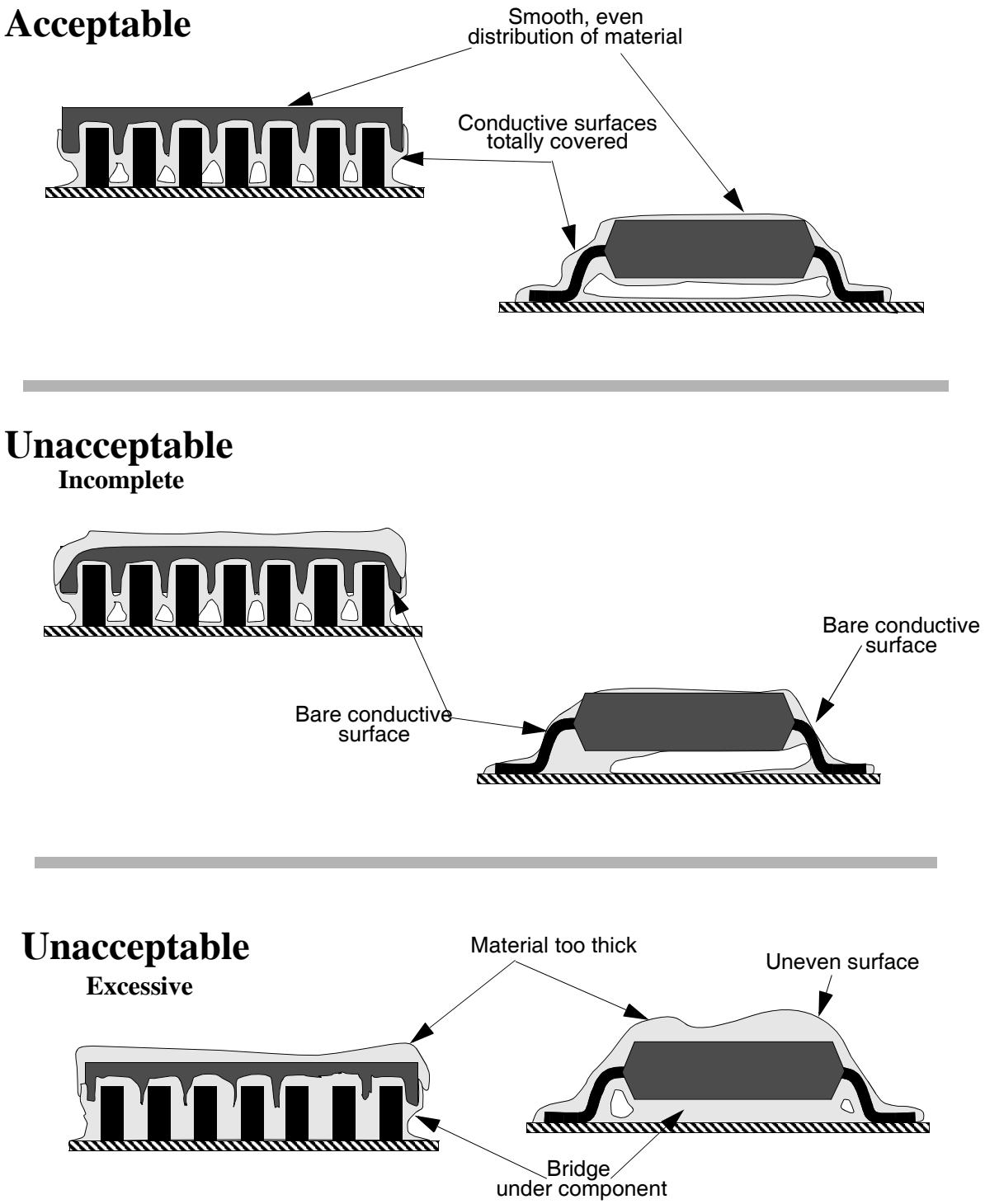

Figure 3.17-12 Flat Pack Conformal Coating

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2.4.2 Conformal Encapsulation Conformance. Conformal encapsulation shall conform to the following:

a. All terminals, electronic components, leads, and other current carrying conductors shall be 100% covered as shown in Figure 3.17-13.

b. Incomplete coverage as shown in Figure 3.17-14 shall be cause for rejection.

c. Excessive conformal coating material as shown inFigure 3.17-15 shall be cause for rejection.

d. The use of fluorescent indicator shall be avoided on light-sensitive equipment.

2.5 Sealing Subassembly-Mounted Connectors

2.5.1 Material Selection. Sealing of subassembly mounted connectors shall use the material listed in Table 3.17-1, “Connectors– Sealing Subassy Mnted.”

2.5.2 Sealant Conformance. The sealant will conform to the following:

a. Sealant shall coat the exposed connector pins between the connector and the shrink tubing as shown in Figure 3.17-16.

a. No sealant material shall reach the contact area of the connector or impede the connector pin float.

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Acceptable

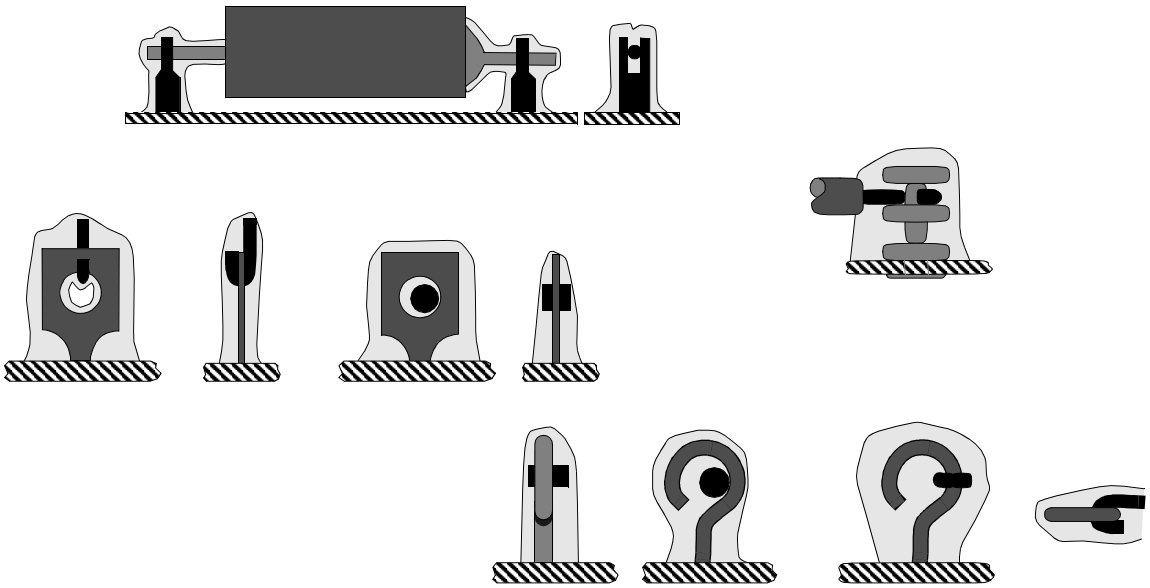

Figure 3.17-13 Conformal Encapsulation

Unacceptable
Incomplete

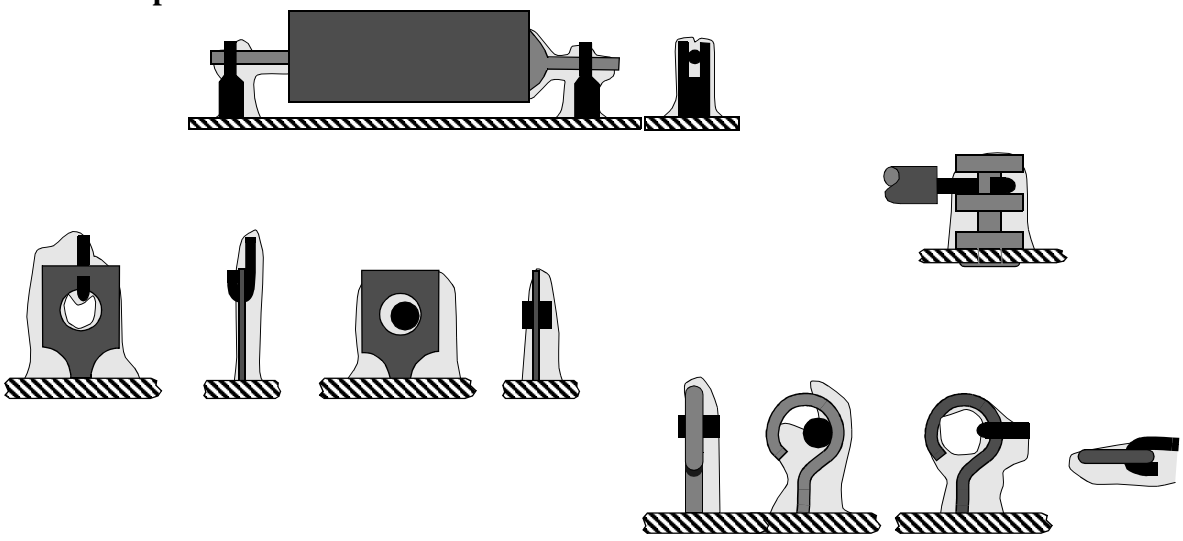

Figure 3.17-14 Conformal Encapsulation

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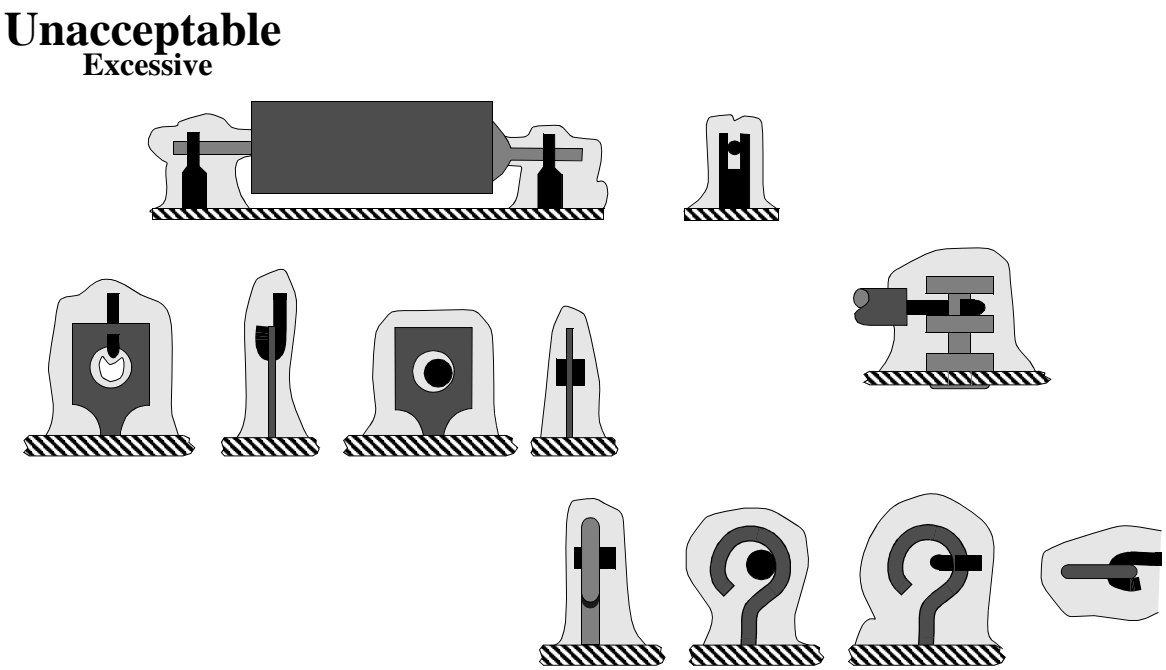

Figure 3.17-15 Conformal Encapsulation

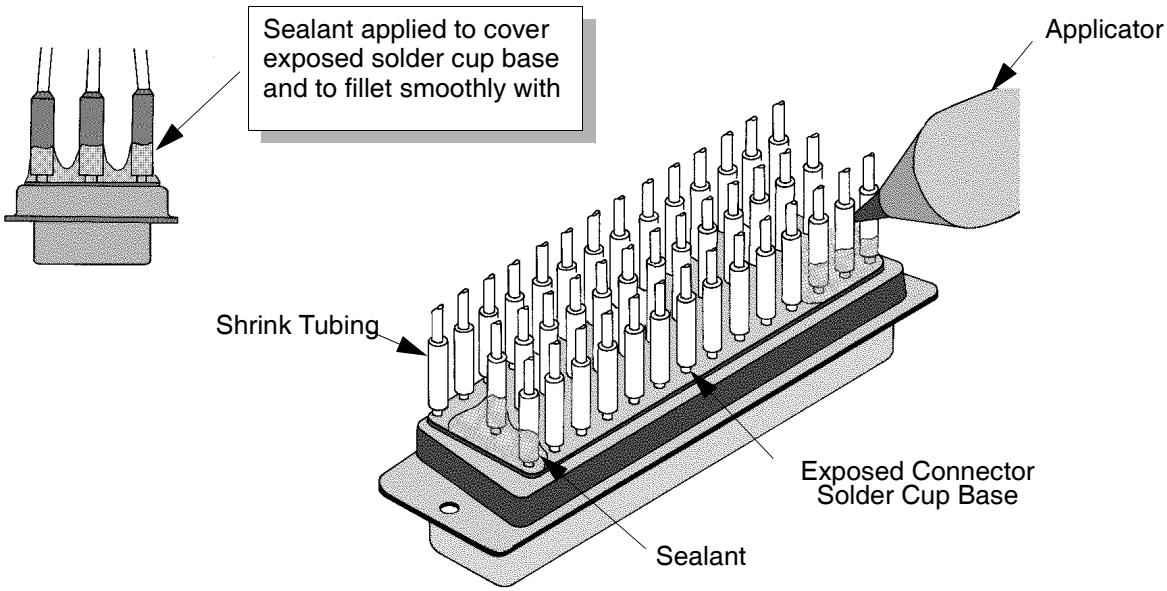

Figure 3.17-16 Connector Sealing

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2.6 Impregnating

2.6.1 Transformer and Inductor Impregnating. Transformers and inductors requiring impregnation shall use the impregnation material listed in Table 3.17-1, "Transformers and Inductors."

2.6.2 Transformer and Inductor Impregnation Conformance. The impregnation and embedment shall conform to the following:

a. A vacuum impregnation and embedment process shall be used for the application of the material.

b. There shall be no material on the exterior surfaces of the potting cup.

c. The potted assembly shall meet the dimensional requirements of the engineering drawing.

d. The material shall not be pulled away from the potting cup.

e. Coils on "C" or "E" cores shall be impregnated prior to core insertion into a coil bobbin.

f. The core gap faces shall be coated with transformer gap cement from Table 3.17-1, "General Purpose Contact Bonding and Transformer Gap Cement," prior to coil-core bonding.

g. The magnetics using split "C" or "E" cores shall be coated with transformer stress relief material from Table 3.17-1, "Stress Relief," prior to embedment.

2.7 Potting

2.7.1 Potting of Subassembly-Mounted Connectors. Subassembly mounted connectors requiring potting shall be potted with materials from Table 3.17-1, "Connector Potting."

2.7.1.1 Connector Potting Conformance. The potting of connectors shall conform to the following:

a. The material shall not be pulled away from the potting mold, connector, solder joints, or wire.

b. There shall be no potting material on the exterior surfaces of the potting mold and connector or on the wires outside of the potting mold.

c. Potting material shall not reduce the motion of floating connector contacts.

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d. A minimum of 0.010 inch of potting material shall be maintained between two electrically conductive elements.

e. A potting mold and a connector seal shall be installed on the connector prior to potting as shown in Figure 3.17-17.

f. A mating connector shall be installed to insure connector alignment prior to potting all connectors.

g. No sealant material shall be allowed on the contact area of the connector.

2.7.2 Potting of Harness-mounted Connectors. Harness-mounted connectors shall be potted per System 1 or System 2 with CV2510 A/B with Cab-O-Sil seal as listed in Table 3.17-1.

2.7.2.1 Connector Sealing and Potting Conformance. The sealing and potting of connectors shall conform to the following:

a. The material shall not be pulled away from the potting mold, connector, solder joints or wire.

b. There shall be no material on the exterior surfaces of the potting mold and connector or on the wires outside of the potting mold.

c. Potting material shall not reduce the motion of floating connector contacts.

d. The potting and abrade molds shall be installed and secured to the connector using per Table 3.17-1, “Bonding– Potting Boot,”

e. The pigtail connectors shall be sealed and potted per Figure 3.17-18.

f. Flex-print connector assemblies shall be potted as called out on the assembly drawing.

g. No sealant material shall reach the contact area of the connector.

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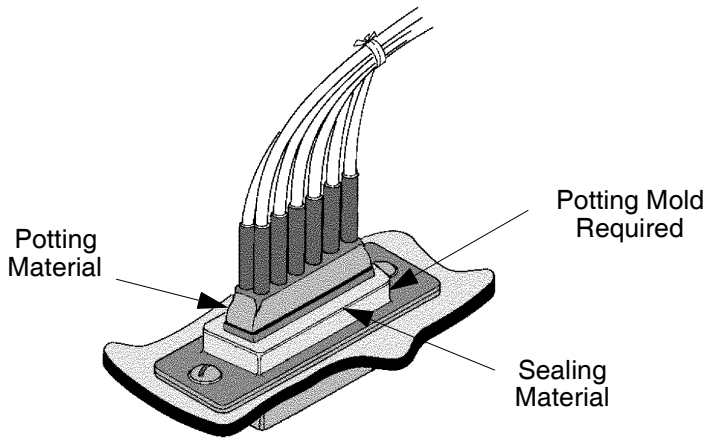

Figure 3.17-17 Mounted Connector Potting

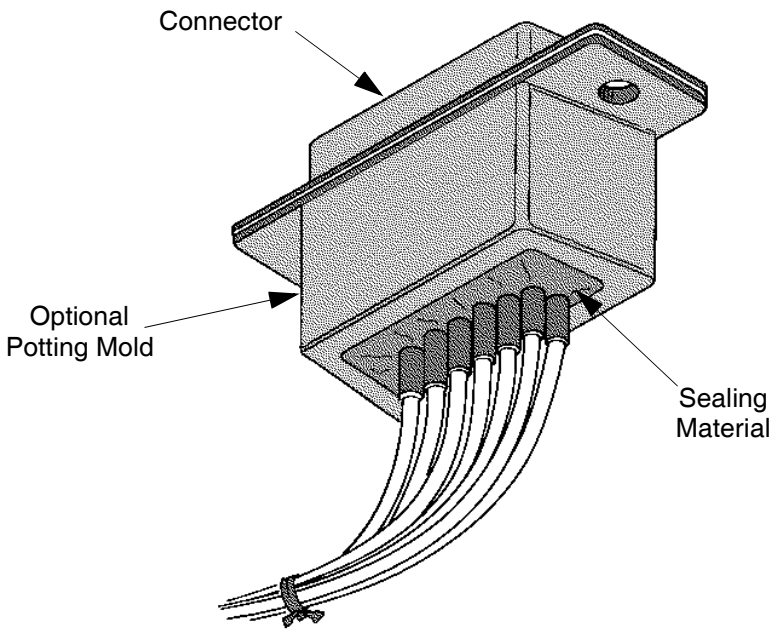

Figure 3.17-18 Pigtail Connector Potting

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2.7.3 Potting High-voltage Modules. High-Voltage electronic modules shall be potted with material listed in Table 3.17-1, "High Voltage Potting,"

2.7.3.1 High-voltage Potting Conformance. The potting of high-voltage electronic modules will conform to the following:

a. There shall be no internal voids or bubbles in the cured material.

b. The material pulled away from the potting mold, connector, solder joints or wire shall be cause for rejection.

c. There shall be no potting material on the exterior surfaces of the potting mold and connector or on the wires outside of the potting mold.

d. Potting material shall not reduce the motion of floating connector contacts.

3 QUALITY ASSURANCE

3.1 Verification Methods

The following methods shall be used to verify the requirements of this document.

3.1.1 Inspection. Verification by inspection is accomplished by comparing the requirements specified in Section 2 with the appropriate characteristics of an item. Inspection includes evaluation of mechanical functionality and accuracy as described in corroborating documentation.

3.1.2 Test. Verification by testing is accomplished by subjecting an item to a set of conditions under the control of approved plans, procedures, and test equipment which will provide a measurable response. The results of the test are compared with the expected results as specified in Section 2.

3.2 Inspection Criteria Requirements

3.2.1 Visual Inspection. Each application of any polymeric shall be inspected with the unaided eye and microscope, at a maximum magnification of 12X, as required, for compliance with the written requirement.

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Shipping and Handling

1 DESIGN REQUIREMENTS

Qualification and acceptance of the fixtures and containers shall be conducted under conditions that simulate bench handling, transportation and storage. Any electronic equipment or hardware identified as JCIs shall meet the requirements of JPL-D-560 and ES501492.

1.1 Electronic Component Handling

Electronic components shall be packaged to prevent damage if dropped and to prevent damage to leads. Lead formed components shall be in a carrier or otherwise protected from damage to the leads. ESD precautions shall be observed, and the packaging shall provide warning of potential ESD damage.

1.2 Handling Fixtures

Handling fixtures shall be required for subassembly and higher level electronics, and be in compliance with the following requirements.

1.2.1 Protection. Handling fixtures shall be designed and fabricated to protect electronic components, equipment, cabling and harness.

1.2.2 Continuous Attachment. The handling fixture shall have continuous attachment to the equipment for testing purposes.

1.2.3 Grounding.The handling fixture shall have provision for grounding.

1.2.4 Access. The handling fixture shall have adequate access for fabrication of the equipment and complete inspection.

1.2.5 Covers. The handling fixture shall have covers attached firmly to prevent potential damage to installed equipment.

1.2.6 Mounting Locations. The handling fixture design shall provide mounting locations for three axis shock indicators near the installed equipment.

1.2.7 G-Meter. The design shall include a “G” meter installed for instrumented proof load inspecting for damage during handling or transporting.

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1.2.7.1 G-Meter Usage. G meters shall be used at the electronic assembly level and higher.

1.2.8 Refurbishment. The design shall allow reuse with a minimum of refurbishment.

1.2.9 Handles. Handles or grasping rods shall be provided to permit carrying.

1.3 Primary Containers

1.3.1 Inherent Properties.The primary container shall be designed from a material with inherent antistatic properties or coated with an approved antistatic coating to protect against electrostatic discharge meeting the requirements of JPL D-1348, Level 2.

1.3.2 Protection. Primary container shall be designed to protect the electronic equipment and attached handling fixture during assembly activities, in-process storage periods, and transportation.

1.3.3 Handles. Handles or grasping points shall be provided.

1.3.4 Latches. Latches shall be provided to permit closing and locking.

1.3.5 Environmental Protection. The design shall protect against environmental and galvanic corrosion of any metal surface.

1.3.6 Desiccant Chamber. The design shall include a moisture barrier and desiccant chamber exposed to all voids and of sufficient size to hold the number of desiccant bags required.

1.3.6.1 Desiccants Bags. Desiccant bags shall meet the requirements of MIL-D-3464.

1.3.6.2 Desiccant Bag Quantity. The quantity of desiccant bags shall be determined by the formula:

$$U = 2V$$

where U is the number of desiccant units and V is the interior volume of the primary container in cubic feet.

1.3.7 Humidity Indicator. The design shall include a visible humidity indicator.

1.3.8 Documentation. A documentation holding package shall be attached to the top of the container.

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1.4 Transportation Container

1.4.1 Protection. The transportation containers shall protect the primary container during transportation or storage and meet the requirements of the applicable project documentation.

1.4.2 Inherent Properties.The transportation container shall be designed from a material with inherent antistatic properties or coated with an approved antistatic coating to protect against electrostatic discharge meeting the requirements of JPL D-1348, Level 2.

1.4.3 Shock and Vibration. The container shall provide damping suitable for isolation of the enclosed equipment from transportation shock and vibration.

1.4.4 Protection Parameters. The container shall have sufficient insulation, thermal capacity and sealing to meet the following requirements.

1.4.5 Hoist Attachment Points. The container shall have attachment points for stable hoisting.

1.4.6 Tie-Down Points. Tie-down points shall be provided to secure a loaded container during transportation.

1.4.7 Stack Height. The container shall be capable of stacking empty containers to a height of ten feet.

1.4.8 Pressure Release. A container 2 cubic feet or larger shall be designed with a pressure-equalizing valve or a pressure-release system.

1.4.9 Dimensions. Container dimensions shall allow passage through a 36 inch wide by 80 inch opening when hardware can be safely contained within said dimensions.

1.4.10 Base Design. Container base shall have a skid-type base for gross weight in excess of 250 pounds.

1.4.11 Latches. The design shall have latches to permit closing and locking.

1.4.12 Materials. The design shall specify materials that are lightweight, impact and crack resistant, oil and cleaning solvent resistant, and dimensionally stable.

1.4.13 Cushion Materials. The container design shall have a polyester cushion material of urethane foam type conforming to AMS-3570, or equivalent.

1.4.14 Chemical Neutral. The design shall provide for chemically neutral wrapping materials.

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1.4.15 "Legacy" Containers. The following shall apply when using inherited containers that are neither conductive nor static dissipative:

a. The hardware shall be packed in an Ameristat bag while still grounded at the workstation.

b. The Ameristat bag shall be closed with antistatic tape and placed in the inner shipping container.

c. Shipping containers shall be checked for charge dissipation prior to storage of unbagged flight hardware.

2 FABRICATION REQUIREMENTS

2.1 Documentation

2.1.1 Deliverable Package. For each deliverable item, certificate of conformance to the required and applicable specifications shall be supplied..

2.2 Handling Requirements

2.2.1 Equipment Selection. Choice of handling equipment, containers, and detailed installation requirements shall be in accordance with the engineering drawing.

2.2.2 Component and Equipment Installation. Electronic components and equipment shall be installed in a handling fixture unless precluded by special conditions of test or operation.

2.2.3 Fiberboard Package. Fiberboard packaging shall be utilized and able to withstand storage, handling, and reshipment without the necessity of repacking.

2.2.4 Level 2 Requirements. Handling and storage of ESDS components, subassemblies and equipment shall be accomplished through use of Level 2 approved electronic component containers, fixtures, primary containers and transportation containers as described JPL D-1348, Electrostatic Control for Assembly and Test Areas for Flight Projects.

2.2.5 Cleanliness and Inspection. Handling fixtures and containers shall be cleaned, inspected, and electrostatically tested prior to installation of the equipment.

2.2.5.1 Fastening Devices. Fastening devices shall be inspected for burrs and foreign material.

2.2.5.2 Active Desiccant. The container shall include an active desiccant.

2.2.5.3 Desiccant Replacement. The desiccant shall be replaced or reactivated when the humidity indicator displays any pink showing moisture contamination.

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2.2.6 Bench Handling. Extreme care shall be exercised handling components during the initial stages of fabrication, prior to attachment to a handling fixture.

2.3 Component and Equipment Movement

2.3.1 QA Frangible Seal. When necessary, a QA frangible seal shall be placed across the joint between the two halves of the container.

2.3.1.1 Equipment Damage. If the seal is broken upon receipt of the transport container at its destination, the equipment within the container shall be carefully inspected for damage and documented by QA on an Inspection Report form.

2.3.2 Movement Within the Fabrication Facility. When components and equipment are moved from one area to another within the same clean area facility, a handling fixture and container shall be used.

2.3.3 Uncontrolled Area. When the electronic equipment is not in a clean area, it must be in a primary container with desiccant, covered and be QA sealed.

2.3.4 Outdoor Movement. Movement through any outdoor environment shall require a handling fixture, primary container and a transportation container with a QA frangible seal.

2.3.5 Motor Vehicle Movement. Movement by motor vehicle shall require a handling fixture, primary container and a transportation container with a QA frangible seal.

2.3.6 Structural Assembly Movement. The transportation of structural elements of electronic assemblies containing no active electronic equipment or components shall be transported within the facility in the handling fixture and primary container.

2.4 PWB Packaging Requirements

PWBs shall be packaged to prevent physical damage during shipment from the supply source to the receiving destination, utilizing package material to protect against corrosion or deterioration.

2.5 Cabling Requirements

Cables shall be protected by use of fabrication fixtures, ESD tested connector dust covers, ESD-safe bags, tote boxes, and protective containers during fabrication, testing and shipment.

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2.5.1 In-Process Handling. Subsystem harness and system cabling in all phases of assembly shall be protected by the applicable fabrication fixture or a special handling fixture, except during cleaning operations, special conditions of test or operation precluding the use of fixtures.

2.5.1.1 Bend Radius. The cabling shall at no times be subjected to bending in excess of the minimum bend radius specified in JPL D-8208, Section 3.12.

2.5.1.2 Uncontrolled Area. The cabling shall be in a protective container when not in a certified clean area.

2.5.1.3 Cable Movement. Cables requiring a frangible seal or key lock across the two halves of the container shall be inspected for damage if the frangible seal or lock is broken.

2.5.1.4 Indoor Movement. When cables or harnesses are moved from one area to another within the same clean area, a handling fixture and container shall be used.

2.5.1.5 Outdoor Movement. Outdoor movement of subsystem harness or small cables shall be in transportation containers and require a frangible seal or key lock.

2.5.1.6 Motor Vehicle Movement. Motor vehicle movement of subsystem harness or cabling shall be in transportation containers and require a frangible seal or key lock.

2.5.1.7 Special Provisions. Small cables or harness assemblies, when personally supervised by the responsible engineer or delegate, may be transported in a tote box secured with a frangible seal, instead of using a shipping container.

2.6 Servicing Criteria

2.6.1 Periodic Servicing. Equipment used for handling, storing, and shipping electronic components and equipment shall be periodically serviced to ensure conformance with the requirements of this section.

2.6.2 ESDS Check. The containers shall be checked for conformance to JPL D-1348, Level 2, prior to placing ESD-sensitive hardware within.

2.6.3 Handling Fixtures.The handling fixtures shall be checked for damage, surface contamination, missing components and proper fixture usage in conformance with the applicable engineering drawing.

2.6.4 Tote Boxes. The tote boxes shall be checked for cracks, damaged gaskets or covers, cleanliness and other surface contaminants.

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2.6.5 Primary Containers. The primary containers shall be checked for cracks, damage to gaskets and latching devices and to assure they are clean, free of chips, flakes, and other surface contaminants.

2.6.6 Transportation Containers. Transportation containers shall be checked for cracks and damage to gaskets and latching devices.

2.6.7 Container Cleaning. Containers shall be clean of stickers and tape residue.

2.6.8 Damping Devices. Vibration damping devices shall be checked and certified as operational.

2.6.9 Foam Liners. Urethane foam liners shall be clean and free of trapped debris and surface dirt.

2.6.10 Relief Valve. The pressure equalization or pressure relief valve shall be checked and determined to be operational prior to use.

2.7 Container Qualification and Acceptance

Transportation containers shall pass the following qualification tests prior to use being put into service.

2.7.1 Drop Test. The adequacy of the container design shall be proven by drop testing of a pilot model.

2.7.2 Vibration Test. The container shall be attached securely to a vibration exciter with a sinusoidal wave form, sweeping from 2 to 500 Hz.

2.7.3 Thermal Protection. The container will contain insulation, thermal capacity, and sealing to maintain the following temperature ranges.

2.7.3.1 Internal Temperature. The container shall maintain the internal temperature within the range of +5°C (41°F) to +45°C (113°F) and humidity to less than 50% while exposed to external conditions of -40°C (-40°F) to +70°C (158°F) and 100% humidity for up to 4 hours.

2.7.3.2 Temperature Change Rate. The internal temperature of the container shall not change more than 5°C (9°F) per hour when exposed to external conditions between -40°C (-40°F) and +40°C (104°F) changing at no more than 15°C (59°F) per hour.

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2.7.4 Moisture. The container shall have a sealed lid that will keep the interior of the container moisture free.

2.7.5 Testing. All testing shall be performed under the cognizance of the JPL Packaging Engineer and verified by QA, or at the vendor prior to delivery.

3 NOTES

3.1 Transportation of Equipment by Common Carrier

Electronic equipment to be transported by common carrier shall be prepared in the same manner as for motor vehicle movement except that all latches shall be safety wired.

3.1.1 Packing Slips.Shipping papers, packing slips, and all documentation, shall be attached to the outside of the container in a labeled water proof package.

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