JPL D-5703

JET PROPULSION LABORATORY

RELIABILITY ANALYSES HANDBOOK

PREPARED BY

PROJECT RELIABILITY GROUP

JULY 1990

National Aeronautics and
Space Administration

JPL

Jet Propulsion Laboratory
California Institute of Technology
Pasadena, California

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Approved by:

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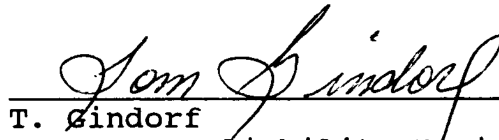

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I. INTRODUCTION

A. General

This document provides guidelines for performing and reviewing reliability analyses associated with flight equipment. It is responsive to the analysis requirements of JPL D-1489 (Ref. 1). In addition, it provider procedures for identifying, preparing, processing, tracking and resolving deficiencies in the analyses and/or design. This document does not address analyses required in direct response to safety concerns.

It should be emphasized that these analyses are not an after-the-fact documentation of what resulted from the design process, but are an active integral part of the design process. There should be immediate action taken if unacceptable analysis results are found.

B. Purpose

The analyses guidelines provide a centralized source of information on performing and reviewing reliability analyses. The purpose is to promote uniformity of the various methodologies, both within a specific project and from project to project. The review guidelines not only provide information to assist the review function, but by explicitly defining what the reviewer should be looking for, the analyst performing the analysis can provide the information in a form that is understandable to the reviewer,

C. Scope

The analyses guidelines provided in this document are primarily intended for use on hardware used by projects or tasks developing flight equipment. The guidelines may be used for other projects or tasks, if such analyses are appropriate or required.

D. Applicability

The procedures and guidelines provided in this document are applicable to JPL projects/tasks, either in-house or system contractor mode.

E. Design Approach

Risk management of flight systems requires inputs from many disciplines. The role of reliability design analyses is to provide quantitative risk assessment data in support of the risk management process. For this process to be effective, the design analyses must be consistent and based on reasonable assumptions. For example, the part stress analysis (PSA), the worst case performance analysis (WCA), and fatigue life of mechanical elements (solder joints, connectors, etc.) are all based on a thermal analysis of the electronics.

These thermal analyses should be based on a 75 °C qualification test thermal control mounting surface level for parts stress temperatures, and an 85 °C design thermal control mounting surface level for WCA temperatures. Fatigue life is based on worst case expected test/mission cycling ranges.

Because all of the "reliability" analyses tend to be interwoven, they should utilize a common data base comprised of realistic assumptions and estimates and be initiated in the conceptual design phase. It is required that these reliability design analyses be completed and independently reviewed prior to the CDR.

This approach requires good thermal design practices to assure that piece part junction temperature limits are not exceeded when module/assembly baseplates are designed and tested to levels corresponding to the above thermal control mounting surface temperature levels. Further, this approach provides the required in-flight thermal margin to assure low thermal stress and the consequent low failure rates, which translate to high reliability. In addition, it assures that the design will provide "in-spec" operation at the various thermal levels.

Analysis verification testing is a very important element in the reliability design analyses process. For example, thermal survey mapping testing significantly improves the system development/qualification cycle by providing vital feedback to the reliability design analyses process.

In summary, the quality of reliability design analyses is significantly increased when worked in a coordinated manner, using realistic assumptions and estimates, and when verification testing is part of the qualification procedure.

F. Acknowledgements

This document is the product of the efforts of a number of people within the Reliability Engineering Section (521). First, the impetus for the task came from Tom Gindorf, the Section Manager. Secondly, the bulk of the manpower came from Jim Arnett's Project Reliability Engineering Group. Special credit is given to Harry Peacock for the extensive discussions of circuit worst case and piecepart stress analyses provided in Appendices B and C. Frank Halula provided the final update to the Failure Modes, Effects and Criticality Analysis (FMECA) guidelines provided in Appendix A. Charles Hayes and Sheldon Johnson revised the Fault Tree guidelines to include the matrix form for tabulating corrective measures. Jim Clawson and Mark Gibbel provided thermal analysis discussions for the body of the document and the guidelines provided in Appendix E. The Single Event Effects guidelines (Appendix G) were provided by Steve Gabriel and Rene Aguero. The discussion of "Automated Analysis Tools" (Section VI(B)) was provided by Paul Bowerman. The discussion of "Reliability Allocation and Assessment" (Section VI(C)) was provided by Dr. Merlin Grossman. Roy Lewis provided input on digit timing to the Worst Case Analysis guidelines in Appendix B.

In addition, a number of people provided valuable review comments. Review comments were provided by Jim Arnett, Art Brown, Steve Clohset, Dr. Neil Divine, Dan Goldman, Dennis Kern, Tom Langley, Dr. Paul Robinson, Dick Sicol and Jerry Swanson.

The editor is responsible for any errors that may remain in the document and welcomes any comments which would improve its usefulness Questions or comments about the document should be directed to Dr. John E. Koch, Jet Propulsion Laboratory, Pasadena, CA 91109, (818) 354-3454. Detailed technical questions may need to be redirected to one or more of the contributors.

II. GENERAL REQUIREMENTS

This section addresses issues that are applicable to all analyses performed in support of flight equipment design and development. If specific analyses have unique requirements, they are addressed within the detailed guidelines provided in the appendices.

A. Project Classification Matrix

Table II-I defines the design temperatures required for each of the five flight equipment classifications. In addition, the analyses requirements of JPL D-1489 (Ref. 1) are summarized. The table indicates whether a particular analysis is required for a specific equipment class and to some extent the level to which the analysis is to be performed. The analysis guidelines provided in this document give the details of this latter point. The table further indicates that for class A and B equipment, all analyses must be formally documented and that they be independently reviewed. For class C equipment, formal documentation and independent review of analyses are at the discretion of the project manager. For class D and E equipment, no analyses documentation is required, except for safety issues.

B. Formal Documentation Requirements

Flight equipment design and development efforts, performing analyses as defined in paragraph IIA, should document them as outlined below. Formal documentation is an activity essential to recording the design capabilities for subsequent review during operation (i.e. test or flight) and to make the analysis readily available for independent review or audit. It should be stressed that "formally documented" does not mean edited, printed and bound report with artwork, etc. The criteria are completeness and correctness coupled with traceability and legibility to enable peer review (e.g. legible hand printing is acceptable) To this end, each analysis report should, as a minimum, contain the following elements:

1. Title Page
2. Applicable Documents
3. Functional Descriptions
4. Performance Requirements
5. Analysis Assumptions and Boundary Conditions
6. Analysis Model
7. Software Analysis Tool(s) Description
8. Analysis Results
9. Summary and Conclusions

Each of these elements is described in the following paragraphs.

1 Title Page

The title page shall provide the following information:

- Project Name
- Project Number
- System/Subsystem/Assembly/Circuit Names
- Analyst Name and Signature
- Date Analysis Completed
- Independent Reviewers Name and Signature
- Date Independent Review Completed
- A unique Analysis Identification Number

2. Applicable Documents

All documents referenced in the performance of the analysis should be cited in this section of the report. Specifically, all documents that contain requirements (functional, interface or environmental which the analysis is to validate should be cited. All circuit schematics, drawings, specifications or policy documents which are used and cited in the analyses should be included here. All document identifications should include:

- Document Name or Title
- Document Number
- Revision Number/Letter
- Release Date
- Issuing Organization

3. Functional Description

The hardware function should be clearly explained, including interfaces with other hardware and/or software items. The theory of operation should be explained in plain language, avoiding numerical values and detailed specific facts as much as possible. The discussion should provide an overview of the hardware operation. It should be provided at a level of detail consistent with the analysis being documented in the report. The discussion shall be supplemented with a block diagram that illustrates the functional relationship of the elements that make up the hardware being analyzed. Each functional element shall be identified and its interface with other elements, both internal and external to the hardware being analyzed, accurately depicted.

4. Performance Requirements

The specified and/or derived requirements for the hardware should be identified in this section. Specified requirements are those imposed directly on the hardware, whereas derived requirements are indirect as they are passed down from a higher level through other hardware or by other requirements. The requirements should be

presented in matrix format. The matrix should list the requirement parameters on one axis of the matrix and the source of the requirement on the other. The actual requirement (i.e. the specified value) is entered in the matrix cell corresponding to the parameter row and the requirement source column. The specified value becomes the acceptance criteria for the analysis. All documents cited as sources of requirements/acceptance criteria shall be included in the Applicable Documents section, described above.

5. Analysis Assumptions and Boundary Conditions

All analysis assumptions shall be clearly identified, including boundary conditions for the analysis. These may include simplifying conservative assumptions that make the analysis tractable and/or more cost effective. Boundary conditions may include physical or functional interfaces with other elements or hardware. It may also be a limitation on the number of functions modeled. Where functions are not analyzed, the rationale for that decision must be documented.

6. Analysis Model

This section shall describe the analysis methodology and the rationale for its use in proving that the hardware design is satisfactory (i.e. positive margins for all functional requirements). The methodology shall be fully described. This may be a "stand alone" description, or it may reference other available documentation. This other documentation may be the specific guidelines provided in this document, or it could be the theory manual of a mature computer program.

7. Software Analysis Tool Description

If software is used in the analysis it must be appropriately referenced. If mature software (i.e. a program that is fully developed, tested and documented) is used for the analysis, it is sufficient to reference the documentation (including source and version), if it is readily available to technical peers.

If software is specifically developed for the analysis of the subject hardware, it must be fully documented and tested. The documentation shall include the theory of operation and logic flow charts depicting its operation. The documentation shall also include a user's guide and a listing of the program. The validity of the program shall be demonstrated by documented test cases which indicate the accuracy of the program and the limits of operation. The limits of operation define the range of input parameters over which the program provides reliable output and/or over which the program has been tested.

8. Analysis Results

The results of the analysis shall be documented in this section. Where feasible, the results should be presented in matrix format with both the analysis results and requirement/acceptance criteria presented side-by-side. Any deviation from the requirement/acceptance criteria shall be clearly identified. In addition, any explanation as to why the deviation occurred and/or how it can be corrected shall also be provided.

9. Summary and Conclusion

This section shall provide a summary of the analysis results. If the analysis indicates that the hardware performance is expected to be within the performance requirements, this should be explicitly stated. If possible, the margin above the required performance should be stated.

Likewise, any and all expected deviations from the required performance that are revealed by the analysis shall be pointed out in this section. The extent and significance of the deviation should be assessed and any proposed solutions identified. In addition, any departure from the acceptable analysis methodologies and/or required environments shall be reported. Note: Any deviation from the performance requirements and/or analysis methodology must be approved via a formal waiver approval by the R&QA and project managers.

C. Inherited Hardware Analyses

The first step in the assessment of analyses of inherited hardware is to establish if the required analysis was performed for the prior application and, if performed, how it was documented.

If prior analyses are available, the applicability of the prior analyses to the new use must be assessed. This assessment should determine if there have been any significant changes in the requirements and/or the design from the prior to the current application. On the subject of requirements, the assessment should consider changes to the functional, interface and environmental requirements. Changes to requirements within one or more of these areas may invalidate the prior analyses. Likewise, changes to the design made since the prior analyses may also invalidate the prior analyses. This includes changes to the physical design and the overall architecture of the design. Thus, the assessment should consider the functional criticality and the level of redundancy of the equipment in the prior and current application. It is not intended to require extensive new analyses of inherited designs if such analyses were previously performed to requirements that meet or exceed the new project requirements. Therefore, every reasonable effort should be made to demonstrate the applicability of the prior analyses.

If it is established that the prior analyses is applicable, the technical adequacy of the analyses can be assessed using the appropriate checklist (i.e. FMECA, WCA, etc.) given in Section IV. If the prior analyses are not available or are considered technically inadequate, the analyses must be redone or revised to meet the requirements of the current application.

D. Independent Review Criteria

JPL D-1489 (Ref. 1) requires an independent review of reliability analyses performed in support of class A and B equipment. For class C equipment, this analyses review is at the option of the project. Independent review is not required for class D and E projects. This information is summarized in the "Flight Equipment Classification Matrix" (Table II-1).

The independent review is an activity required to be performed in accordance with project standards that result in the review of analyses performed by one organization's individuals by other individuals who have had no part in the original effort and generally from a different organization. The independent review is conducted by a technical peer with the expertise to generate the original analysis. When the original analysis is performed by a JPL technical division, it is reviewed by the JPL Project Reliability Group. If, on the other hand, the analysis was originated by the Project Reliability Group, the cognizant technical group is responsible for conducting the independent analysis review. When analyses are performed by a contractor, the independent review may be conducted by either or both the JPL cognizant technical group and/or the Project Reliability Group. In any case, the reviewer is required to document the findings of the review in a memo, as described in Section V of this document.

Review guidelines and checklists for each type of analysis are provided in Section IV of this document.

E. Waivers

This document provides a uniform and consistent interpretation of analyses required by JPL D-1489 for use during the design and development of JPL flight equipment. The waiver system is to be employed where differences between the actual programmatic content of an activity and the requirements which are imposed by this document cannot be reasonably or realistically implemented. These differences can develop in a number of areas, including, but not limited to:

1. Decisions not to perform a required analysis;
2. Decisions to accept out-of-spec performance under some analyzed mode of operation;
3. Departures from the analysis methodology, including the approach, environments, interfaces and/or derating criteria;
4. Decision not to have analyses independently reviewed.

The waiver processing and signoff is to be in accordance with policy of the affected project and the requirements of the JPL Standard for Waiver Requests (Reference 2).

TABLE II-1
FLIGHT EQUIPMENT CLASSIFICATION MATRIX

PROJECT CLASSIFICATION	A	B	C	D	E
THERMAL CONTROL MOUNTING SURFACE DESIGN TEMPERATURE RANGE	-30 TO +85°C except where allowable flight exceeds the range of 5°C to 50°C, then allowable flight ±35°C.	S/A CLASS A	-20 TO +75°C except where allowable flight exceeds the range of 5°C to 50°C, then allowable flight ±25°C.	Allowable flight ±10°C	Allowable flight
FMECA	Circuit (functional block level) & interfaces (piece part level)	S/A Class A	Interfaces (assembly level, unless customer supplied interface used)	Interfaces (system level to external interfaces)	S/A Class D
THERMAL	Piece part level (or assume 30°C rise to part) in support of the WCA, EEE parts stress and fatigue life	S/A Class A	S/A Class A, except at qual temp	Not required	Not required
REDUNDANCY SWITCH	Verify failure detection and adequate switching to redundant element	S/A Class A	Not required	Not required	Not required
WCA, CIRCUITS	Verify electronic circuits perform intended function under worst case conditions	S/A Class A	Substitute acceptable (see margin test)	Not required	Not required
WCA, POWER SUPPLIES TRANSIENTS	Verify adequate protection of power systems during transients and in the event of problems or failures in "user" circuits/elements	S/A Class A	S/A Class A	S/A Class A	Not required
EEE PARTS STRESS	Verify, for each part application, that actual stresses do not exceed derating guidelines	S/A Class A	S/A Class A	Safety only	S/A Class D
THERMAL/STRUCTURAL STRESS ANALYSES	Verify that actual applied stress does not exceed the design criteria at worst case conditions	S/A Class A	Safety only	S/A Class C	S/A Class C

TABLE II-1 (Continued)
FLIGHT EQUIPMENT CLASSIFICATION MATRIX

PROJECT CLASSIFICATION	A	B	C	D	E
FAULT TREE ANALYSES	Identify all failure causes of non-electronic hardware failure states	S/A Class A	Interfaces only	Safety only	S/A Class D
SINGLE EVENT EFFECTS (SEE)/LATCHUP (LU) ANALYSES	Identify SEE/LU sensitive parts. Estimate the SEE frequency of occurrence	S/A Class A	S/A Class A	Not required	Not required
ANALYSES METHODS COMPLIANT WITH D-5703	YES	YES	YES	Safety only	Safety only
ANALYSES FORMALLY DOCUMENTED	YES	YES	Project Variable	Safety only	Safety only
ANALYSES INDEPENDENTLY REVIEWED	YES	YES	Project Variable	Safety only	Safety only
DESIGN PROBLEMS DOCUMENTED BY DDRS AND TRACKED	YES	YES	Not required	Not required	Not required
PARAMETER TREND ANALYSIS	YES	YES	Project Variable	Not required	Not required

III. ANALYSES OVERVIEW

The design of spaceflight hardware involves many steps to ultimately result in reliable performance. Some of these steps include a selective parts, materials and processes program, an intense system engineering activity, conservative design practices by the technical divisions, adversarial design review by technical peers, thorough testing at all levels of hardware (including the flight system), and design validation by analysis. The latter item, design validation by analysis, is the subject of this document. This process, to be effective, is started as early as possible and continues throughout the design development.

The basic design philosophy is to develop flight systems that not only have redundancy, but also have partial survival capabilities under failure conditions of the primary hardware. Various analysis techniques are used to validate functionality of the hardware under various conditions, including the following: failures, extreme conditions and end of life. Table III-1 groups this data into a matrix of analysis type versus conditions. It can be seen that most analyses validate functionality under one specific set of conditions; thus, for complete design validation, all analysis types need to be performed. The following paragraphs provide a brief overview of each type of analysis and more details on the benefits derived from each.

TABLE III-I DESIGN VALIDATION MATRIX - ANALYSIS

	Functionality under Failures	Functionality under Extreme Conditions	Functionality for long life
FMECA	X		
WCA		X	X
EEE Parts Stress			X
Thermal		X	X
Structural Stress		X	X
FTA	X		
SEE		X	
Parameter Trend Analysis			X

A. Failure Modes, Effects and Criticality Analysis (FMECA)

The FMECA is a design tool used to systematically analyze postulated component failures and identify the resultant effects on system operations. The analysis is sometimes characterized as consisting of two sub-analyses, the first being the failure modes and effects analysis (FMEA), and the second, the criticality analysis (CA). The FMEA addresses all postulated part failure modes in a system and the resultant effect on its operation. The CA ranks each postulated failure mode according to the criticality of the effect on system operation and the probability of its occurrence. Successful development of an FMEA requires that the analyst include all significant failure modes for each contributing element or part in the system. FMEAs can be performed at the system, subsystem, assembly, subassembly or part level. In general, failures to start/stop, open/close or continue to operate should be considered.

The FMECA should be a living document during development of a hardware design. It should be scheduled and completed concurrently with the design. If completed in a timely manner, the FMECA can help guide design decisions. The usefulness of the FMECA as a design tool and in the decision making process is dependent on the effectiveness and timeliness with which design problems are identified. Timeliness is probably the most important consideration. In the extreme case, the FMECA would be of little value to the design decision process if the analysis is performed after the hardware is built. While the FMECA identifies all part failure modes, its primary benefit is the early identification of all critical and catastrophic subsystem or system failure modes so they can be eliminated or minimized through design modification at the earliest point in the development effort; therefore, the FMECA should be performed at the system level as soon as preliminary design information is available and extended to the lower levels as the detail design progresses. The analysis may be performed at the functional level until the design has matured sufficiently to identify specific hardware that will perform the functions; then the analysis should be extended to the hardware level. When performing the hardware level FMECA, interfacing hardware is considered to be operating within specification. In addition, each part failure postulated is considered to be the only failure in the system (i.e. , it is a single failure analysis). In addition to the FMEAs done on systems to evaluate the impact lower level failures have on system operation, several other FMEAs are done. Special attention is paid to interfaces between systems and in fact at all functional interfaces. The purpose of these FMEAs is to assure that irreversible physical and/or functional damage is not propagated across the interface as a result of failures in one of the interfacing units. These analyses are done to the piece part level for the circuits that directly interface with the other units. The FMEA can be accomplished without a CA, but a CA requires that the FMEA has previously identified system level critical failures. When both steps are done, the total process is called a FMECA. The detailed FMECA guidelines are provided in Appendix A of this document.

Major benefits derived from a properly implemented FMECA effort are as follows:

1 It provides a documented method for selecting a design with a high probability of successful operation and safety.

2. A documented uniform method of assessing potential failure modes and their impact on system operation, resulting in a list of failure modes ranked according to the seriousness of their system impact and likelihood of occurrence.

3. Early identification of single failure points (SFPS) and system interface problems, which may be critical to mission success and/or safety. They also provide a method of verifying that switching between redundant elements is not jeopardized by postulated single failures.

4. An effective method for evaluating the effect of pro posed changes to the design and/or operational procedures on mission success and safety.

5. A basis for in-flight troubleshooting procedures and for locating performance monitoring and fault-detection devices.

6. Criteria for early planning of tests.

From the above list, early identifications of SFPS, input to the troubleshooting procedure and locating of performance monitoring/faultdetection devices are probably the most important benefits of the FMECA. In addition, the FMECA procedures are straightforward and allow orderly evaluation of the design.

A computer program can be very useful in performing circuit FMECAS, since there may be a large number of computations and a large amount of record keeping required for hardware of reasonable size. Ideally the FMECA program would have two main features; first, it would analyze circuit performance under the condition of each piece part failure mode, and secondly, it would have database features that would record the failure mode and the resulting next higher-level performance impact. Once these steps are completed, the database function would allow editing of the database to identify corrective action planned or implemented to mitigate the affect of the failure. In addition, the criticality rating and probability of occurrence can be added to the record when they are established. Once the analysis results are in the FMECA database, it can be rank sorted to focus attention on the most critical items. Unfortunately, most available FMECA programs fall short of this ideal. Several programs are discussed in Ref. 4, page 7-118 of Vol. I. One of the newer programs was developed at the University of Georgia for the Space Shuttle.

B. Redundancy Switch Analysis

This analysis is performed to verify that if a failure of a redundant system element occurs, the source of that failure is appropriately detected and that mechanisms exist and are capable of reliably operating to effect a switch to the redundant system element to continue system operation.

Although there may be other acceptable ways of performing this analysis, the FMECA format and methods lend themselves to this task very effectively. The detailed FMECA guidelines are provided in Appendix A of this document.

C. Worst Case Analysis

Worst Case Analysis (WCA) is an extension of classical circuit analysis, but uses a different approach and has a different objective. The most significant difference in the approach is the use of part parameter data and conditions at their extreme values rather than the nominal value. In the WCA, the classical circuit analysis is repeated for each combination of extreme values of part parameters and conditions. The objective is to verify that the circuit functions as required for all combinations of allowable part parameters and conditions. Circuits that are designed to provide the required output at nominal conditions and parameters may not meet the output requirements if the operating conditions or parameters vary from the nominal values over their allowable range. Out of specification performance is even more likely when several conditions or parameters vary from the nominal design condition resulting in excessive part variation. In such cases, fault isolation can not identify any part as failed or input as unacceptable. Thus, to assure reliable performance of spacecraft circuits, it is essential that variations in these parameters and conditions from their nominal values be addressed as the circuit design is being developed. The "Worst Case Analysis" methodology has been developed over the years to address these effects for both analog and digital circuits and is briefly described below (see the Appendix B to this document for detailed guidelines for performing the WCA).

To facilitate the performance of the WCA, the analyst may reduce complex circuits to smaller functional blocks. By using this approach, the analysis becomes more manageable, aiding both the analyst and the reviewer. When a circuit is reduced to these functional blocks, performance requirements for each block need to be established. Both input and output requirements should be established. These requirements will serve as the evaluation criteria for the WCA results for the functional blocks. Some of the requirements for the functional blocks will have to be derived from higher level specification requirements. The WCA should show compliance with all requirements, both on the functional block level and at the circuit level. Proof of compliance to certain less significant requirements may be omitted provided that adequate justification for the specific omission is given. To simplify the discussion, the remainder of this discussion will refer to circuits, but is intended to apply to the lower level functional

blocks also. The worst case conditions of any given circuit will be a combination of the extreme values of the following factors:

1. Circuit interface inputs and loads
2. Piece part parameter variations

These factors are described in the following paragraphs.

The inputs to the circuit are taken to their specified maximum and minimum voltage, time and/or frequency with the intention of driving the outputs of the circuit to their maxima and minima. The variations of signals presented to the circuit being analyzed are to be those continuous values which are applied at the inputs to the circuit. If the circuit is a control circuit which feeds back, in effect, to its own input (e.g. , a regulator circuit), it is subject to the limits of its control range in the WCA. Likewise, the interface characteristics on the circuit's output side (i.e. loads, etc.) are also to be taken to the appropriate maximum or minimum extreme.

The total parameter variation depends on variations resulting from a number of causes. The worst case variation for any one part parameter is the product of the individual parametric variations, as follows:

$$(1+dP) - (1+dX)(l+dS)(l+dT)(l+dE)(l+dR)$$

where: dP is the total parametric variation
dX is the part initial tolerance
dS is the variation due to aging and drift
dT is the variation due to piece part case temperature (worst case direction)
dE is the variation due to applied voltage and frequency
dR is the variation due to radiation degradation

The analysis is a true worst case in that the value for each of the variable part parameters will be set to limits which will drive the output(s) to a maximum or minimum or both, depending on the circuit function. Piecepart temperatures are based on a thermal analysis at the shearplate design temperature levels (-30 to +85 °C).

In many cases (e.g., RF circuitry), the modeling and analysis of a circuit may prove to be extremely difficult and questionable for certain parameters. In these cases, it may be expedient to use laboratory test data in conjunction with analysis to determine the worst case response. For those parts that are difficult to model, the laboratory test is used to establish the sensitivity which can be used in a simplified analysis to achieve all worst case conditions.

D. EEE Part Stress

Electronic parts are prone to premature failure due to overstress, especially thermal. Certain parts are more stress sensitive than others. Decreases in failure rate can be achieved by reducing the stress levels by good design practices. Reducing part stress levels has become well developed and is called "derating". Derating is the procedure of designing parts to operate at stress levels below the manufacturer's rated values. Derating procedures vary with different types of parts and their application. Resistors are derated by decreasing the ratio of operating power to rated power. Capacitors are derated by maintaining the applied voltage at a lower value than the voltage for which the part is rated. Semiconductors are derated by keeping the power dissipation below the rated level. Derating electronic parts involves the use of derating curves. These curves usually relate derating levels to part parameter (function temperature) or physical factor. In addition, maximum junction temperature derating is advisable to provide some margin for analytical error.

The significant advantage of a thorough parts stress analysis is the increased life expectancy resulting from the stress derating. As most part failure rates are exponentially dependent on temperature, it is obvious that derating to achieve low operating temperature is essential to long life. Detailed guidelines for performing the EEE parts stress analysis are provided in Appendix C of this document.

E. Structural Stress

The primary consideration in the design of a spacecraft structure is the launch vehicle loads imparted to the spacecraft. These loads are imparted in two ways. First, directly through the structure via the interface structure between the launch vehicle and the spacecraft and secondly, acoustic loads imparted into the structure through all surfaces that are exposed to the acoustical environment resulting from the launch vehicle engines and the aerodynamics of the launch vehicle. Both load sources are highly dynamic in nature. The loads transmitted directly through the structure have frequency content mainly in the zero to 30 to 40 Hz range. The acoustical input has frequency content mainly in the 50 Hz to 10 KHz. Two completely separate analyses are required for each load source because of the difference in the source and more importantly the greater amount of detail required to model the higher frequency acoustical analysis. Each of these analyses is discussed in the following paragraphs.

Spacecraft structural analyses, based on the direct input from the launch vehicle, is an iterative process. First, a preliminary analytical model of the entire spacecraft is developed, based on estimated input loads and the preliminary design of the spacecraft structural members. This model is then combined with a model of the launch vehicle for the "Coupled Loads" analysis. The results of the "Coupled Loads" analysis define in greater detail the loads on the individual structural members. These newly redefined loads are then used to refine the design of the structural member

which in turn results in a modification of the preliminary analytical model This modified analytical model is then used in a second "Coupled Loads" analysis, which may or may not change the individual structural member loadings to the extent that another member design/"Coupled Loads" analysis iteration is required.

(The discussions of the analysis dealing with the acoustical inputs will be provided later)

In addition to the above analyses, the dynamic interaction of the spacecraft structure with the attitude control system (ACS) must be evaluated. Unless properly designed , unstable oscillations can occur resulting from the control system exciting a structural mode of the spacecraft. This situation can result in excessive consumption of ACS control gas, thus resulting in early termination of the mission. Of particular concern are appendages, such as solar arrays and booms. For a specific example of this type of problem consult the JPL Spaceflight Significant Event File (SSEF) (Reference 7), item number 2-111.

F. Thermal Analyses

Risk management of electronic systems requires inputs from many technical experts. The role of a thermal analysis is to provide data in support of the risk management process. Thermal analysis of electronic assemblies is the basis for:

- o The part stress analysis (PSA).
- o The worst case performance analysis (WCA).
- o Solder joint fatigue vs. temperature.

The piece part analysis estimates the thermal rise across the shearplate-module baseplate interface, the baseplate to piece part case rise, and ultimately the case to junction rise.

For this process to work effectively, the thermal analysis must be based on reasonable assumptions. The most critical assumption to a well designed thermal model is power dissipation. Often, the power dissipation assumed in the analysis is a factor of 2 or more higher than the unit's actual measured dissipation. This is sometimes attributed to power estimates based on maximum specification value rather than on the particular application. This factor alone has contributed to more unnecessary design changes than any other.

Where possible, thermal analysis verification testing should be performed. This is the most effective way to improve the accuracy of the thermal analysis.

The guidelines set forth in this document for electronic assembly level thermal analysis refer only to thermal analyses performed in direct support of the reliability analyses requirements, i.e. part stress analyses,

worst case performance analyses, solder joint reliability analyses and part life vs. temperature. They are not intended to direct the packaging engineer's conceptual thermal design or specific board layout.

General Considerations:

These thermal analyses should be performed in such a manner that they are conservative rather than non-conservative relative to reliability considerations. However, this conservatism must be managed to minimize its impact on the electrical and/or packaging design. The need to be conservative, but not overly conservative, usually requires a "smarter" rather than "cookbook" approach. This usually involves developing computer models employing standardized industry codes such as SINDA, rather than "back of the envelope" calculations or generic "expert" computer codes written primarily to aid P.C. board layout. If all of the design analyses which need piece part thermal analysis data are identified up front, usually one well thought out thermal model, run for the various boundary conditions, will be needed.

The archaic "rule of thumb" that the "thermally significant" piece parts can be screened on the basis of power dissipation has been disproven. Studies of the MGN SAR thermal analyses indicate that approximately 50% of the thermally overstressed piece parts dissipated 50 milliwatts or less and that 70% dissipated 100 milliwatts or less.

Part manufacturers tend not to worry about the thermal design of their low power dissipation parts as much as they do high power parts. This continues with the circuit designer utilizing these "worry free parts" in the circuit with little concern about "thermal" load on these parts. The packaging engineer also tends to worry less about the part placement and/or the part to board mounting of these parts than on the large dissipators. The combined result is that the junction to board temperature rises of the low dissipation parts often are as high or higher than that of the large dissipators.

Part dimensions which are conservative (realistic worst case) should be used because part dimensions from one manufacturer to another vary greatly. Differences between a particular manufacturer's part dimensions and MIL- 38510 H, Appendix C, often result in thermal resistances that differ by a factor of two. If parts are to be obtained from multiple sources, then the thermally limiting dimensional data should be used.

Understanding of the current manufacturing process used to build the hardware has a significant effect on the assumptions made in the piece part thermal analysis in support of the reliability considerations. Detailed guidelines for performing the thermal analysis are provided in Appendix E of this document.

G. Fault Tree Analyses

At the heart of Fault Tree Analysis (FTA) is the fault tree diagram. The fault tree diagram is a logic diagram depicting an undesired or failed state of the system at the top of the tree (FT) with underlying branches of the FT representing subsystem and component failures that can lead to the undesired or failed state. This latter item is referred to as the "TOP EVENT". Depending on the system configuration (i.e. redundancy, level of fault tolerance, etc.), one or more subsystem or component failures may be required before the Top Event occurs. For example, if failure of two redundant components is required to cause the Top Event, their failures would be depicted as input to a logical "AND" symbol. Likewise, if failure of any one of a series of components would result in the Top Event, their failures would be depicted as input to a logical "OR" symbol. Both of these logic symbols would be a direct input to the Top Event. Generally, the system FT is constructed with failures of the major functional element (say the subsystem) depicted as the first level below the Top Event, then failure of the next lower functional element depicted as the second level below the Top Event. This process can be carried down to the lowest level of element for which failure information is available or provide the detail desired by the analysis. An example of a simple block redundant system is depicted in Figure III-1. An example of a simple single string (or series) system, consisting of five subsystems, is depicted in Figure III-2.

The companion FT matrix is developed and addresses the corrective action, design measure or product assurance activities that the project will implement to eliminate or minimize to the extent practical for each of the identified failure modes.

It should be noted that a given system may have more than one undesired or failed state, and therefore more than one FT could be developed for that system. The analyst should carefully consider all possible undesired or failure states of the system, but select for analysis only those that are relevant to the issues being evaluated. To do otherwise will result in considerable effort being expended in doing the FTA without significant payoff from the results of the nonessential FTs.

At JPL, the FTA has traditionally been applied to mechanical and electromechanical systems; however, there is no fundamental reason why the FTA methodology could not be applied to any type of equipment. There are practical reasons, however, why it is not feasible to apply the methods to electronic equipment at the piece part level, and one is the sheer effort that would be required. In most cases the benefits would not warrant the effort. These evaluations are more economically handled by other methods, such as FMECAS. These latter methods do not provide the easy visual interpretation available with the FT logic diagram nor do they address potential multiple failures, but are considerably less labor intensive.

The analyst must be rigorous in the analysis, as any potential real life failure scenario not included in the FT model will cause the risk of

the Top Event to be underestimated. The inverse statement is that the reliability of the system is overestimated. In either case, not including legitimate failure scenarios results in a nonconservative FTA, the magnitude of which would be unknown. Detailed guidelines for performing FTA is provided in Appendix F of this document.

H. Single Event Effects Analyses

Single Event Upsets (SEUs) occur in microelectronics when a single particle, usually a heavy ion or proton, deposits enough charge at a sensitive node in a circuit to cause a change of state. Heavy ions and protons are found in galactic cosmic rays, solar flares and in radiation belts around planets. SEUs became a concern in the late 1970's because advancing technology ((both CMOS and bipolar) was evolving towards lower power and higher speed; consequently a smaller amount of charge on a circuit node was used to store, information. The state of a bit in the device was represented by a smaller amount of charge. How much charge is enough to cause an upset depends upon the electronic part, its condition and the sensitive region. Single event effects can result from the direct ionization of individual particles originating outside the spacecraft, or they can be caused by the intensely ionizing fragments from a nuclear reaction caused by individual protons originating outside the spacecraft. Such proton-induced effects may be important in inner radiation belts where intense fluxes of protons are trapped. The particle environment [flux nucleon/(cm^2-sec-Mev)] as a function of species is very dynamic and varies with solar activity. The changes in this environment can radically affect the probability of upsets occurring in a part. SEUs are produced in an integrated circuit when a particle produces a change of state (1,0) in one or more memory locations within the chip. A memory location is typically made up of more that one active device and connecting components.

The SEU analysis consists of four steps, as follows:

1. Define the radiation environment.

2. Identify the SEU sensitive electronic parts by means of critical LET and cross section.

3. Combine the information from the first two steps (1 and 2) to predict the upset rate for each sensitive part.

4. Perform a circuit (system) response analy sis using the above information to provide number of upsets per mission for the particular system, effects on operation, mission criticality, and, when applicable, percentage of data loss due to particular upsets.

I. Parameter Trend Analysis

Given the State-of-the-Art, establishing the absolute reliability of spacecraft systems by analytical models is at least very difficult, costly and perhaps intractable. Parameter trend analyses is an alternative or companion approach. Specifically, it is generally known that the values of certain parameters will directly impact on a component or systems reliability, even though the exact quantitative relationship has not been determined. Those measurable parameters that directly affect system or component reliability are sampled over time. The parameters values are examined to see if there is a pattern of deviation over time (i.e., a trend) from acceptable performance limits. In this manner, it may be possible to predict future parameter values, or at least estimate the long-term range of values of these influential variables. Thus, if these parameters are trending towards hazardous or unacceptable levels, the potential problem could be identified prior to the occurrence of high-risk situations.

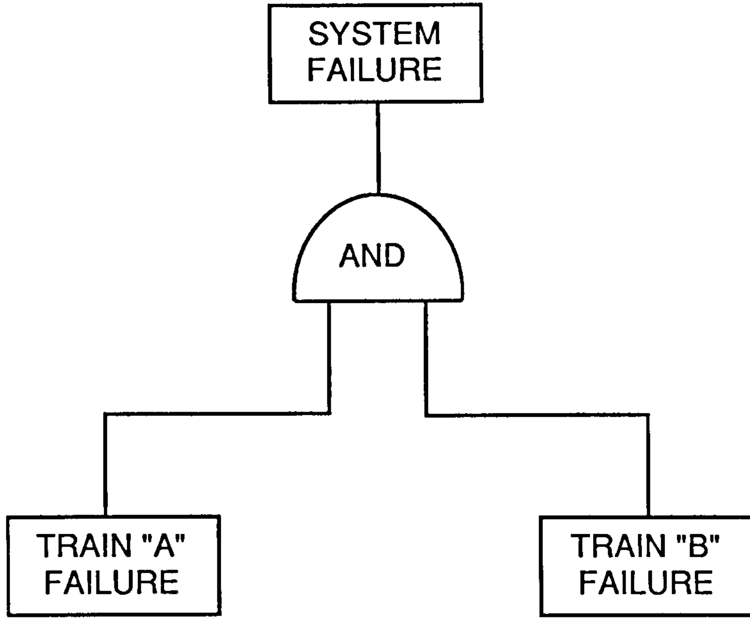

Figure III-1. Fault Tree For Simple Redundant System

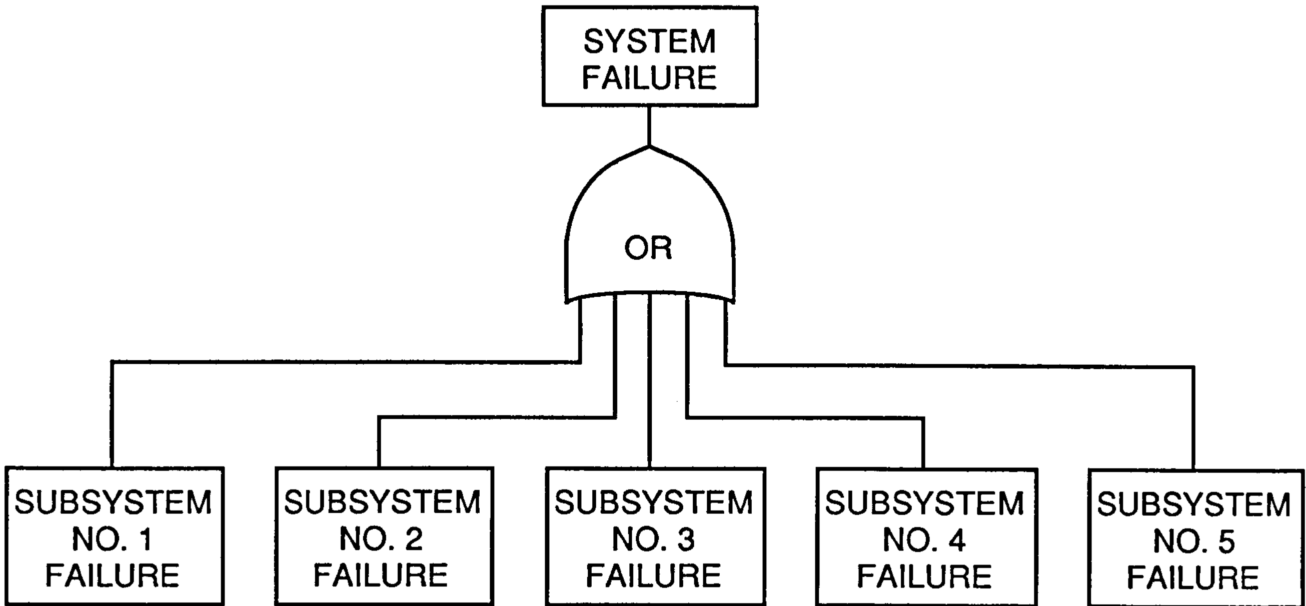

Figure III-2. Fault Tree For Simple Single String (or Series) System

IV. REVIEW GUIDELINES

The following analysis review guidelines/checklists are provided to assist the analysis reviewer and the originator. The assistance to the reviewer gives the minimum set of questions that need to be addressed in the review. The assistance to analysis originator is not as directed and therefore is not as obvious. The assistance to the originator comes from the upfront knowledge of what the reviewer will be looking for in the analysis. Thus, the information can be provided in the original documentation rather than as a backfit during the review process.

A. General Review Items

1. Does the configuration analyzed correspond to the flight configuration? If not, the originator should provide justification of the applicability of the analysis to the flight configuration within the analyses documentation package.

2. Is the basic data package, including the following elements, complete and adequately cited in the analyses?

   a. Circuit description
   b. Circuit drawing and revision designation
   c. Functional and logic block diagrams
   d. Functional and interface requirements
   e. Results summary and conclusions

In addition to the above general items, each analysis type should be checked for the following items:

B. FMECA

1. Single String Designs

   a. Was primary function protected by functional redundancy?
   b. Was verification made that loss of secondary function cannot cause loss of primary function?
   c. Was the analysis done to the piece-part level?
   d. Did the analysis include all appropriate mission modes?

2. Block Redundant Designs

   a. Was redundancy switching designed such that single failure in one branch does not propagate to the other redundant branch?
   b. Are inputs to redundant trains (i.e. power, signals, etc.) independent of each other?
   C. Was a listing of all single failure points prepared?

3 Mechanisms

a. Was FMECA or Fault Tree Analysis performed to the lowest level of disassembly?
b. Were mechanisms tested/analyzed to control failures?

C. WCA

1. Circuits

a. What functions were evaluated in the WCA?
b. What were the criteria for acceptance performance?
c. What functions were not analyzed and the justification for ignoring?
d. What were the design/analysis baseplate temperature limits that were used, and what was assumed for local part temperature rise above the baseplate temperature?
e. Was an analysis alternate such as Thermal/Voltage Margin test used?
f. Were voltage and/or frequency tolerances considered?
g. Was Extreme Value Analysis used or Root Sum of the Squares (RSS)?
h. Did parts parameter variations include initial part variation, aging (shelf life + mission), drift, special factors, radiation effects, etc?

2. Power Supply Analysis

a. Was transient performance considered, including current surges due to inrush and mode change?
b. Was the input filter reviewed for bus stability and ripple current reduction?
c. Were power consumption, power factor and DC component in AC loads considered?
d. Was overload protection (fuses and current limiters) considered?
e. Did grounding analysis consider external interactions and capacitive coupling of multiple grounds?
f. Were non-standard failure modes and the effects on power consumption, surges, ripple and power subsystem telemetry considered?
g. Were discrete semiconductors analyzed for peak transients on all terminals (i.e. cathode, base and emitter)?

D. PART STRESS ANALYSIS

a. Were all parts analyzed?
b. What shearplate and junction temperature limits were used?'
c. What source (MIL-STD-975, ZPP-2061-PPL) was used for stress derating values?

E. STRUCTURAL STRESS ANALYSES

a. Were all assemblies and critical components analyzed?
b. Were worst case estimates used?
c. Were both static and dynamic environments (loads, shock, vibrating and acoustics) considered?
d. Did the environments include fabrication, shipping, storage, launch and flight?

F. THERMAL STRESS ANALYSIS

a. Were all assemblies and piece parts analyzed?
b. Were worst case estimates used (how do they compare to measured values)?
c. What temperature extremes were used?
d. Were thermal cycling effects considered?

C. FAULT TREE ANALYSES

a. Verify that top event is consistent with specified functional requirements and is broadly enough defined to include all top level functional requirements if there are more than one.

b. Review supporting documentation (i.e. system description, specifications, functional block diagrams, schematics, etc.) to verify that the hardware has been properly modeled.

c. Verify that all reasonable failure modes have been included in the fault tree branches (As a minimum, the failure modes identified in Appendix F to this document should be included).

d. Verify that the fault tree branches have been developed down to a hardware level for which there are well established failure modes. (Note: In some cases this may be the piece part level.)

e. Verify that the companion FT matrix has been developed and addresses the corrective action, design measure or product assurance activities that the project will implement to eliminate or minimize to the extent practical each of the identified failure modes.

H. SEU

a. What ambient and/or local environment was used?
b. What parts models were used?
c. What was the predicted upset rate?
d. Was an analysis of the impact of SEUs on system performance made?
e. Were there any unacceptable results predicted?

I. PARAMETER TREND ANALYSIS

a. Verify that key performance parameters were selected for monitoring, by reviewing the functional performance requirements contained in the hardware specification and descriptive material on operation (see other analyses such as WCA, FTA, etc).

b. Verify that all available test data was included in the evaluation and that important test conditions (i.e. those conditions that have an effect on the tracked parameter) are accounted for in the analysis.

c. Compare extrapolated end-of-mission performance with specified requirements to assure that satisfactory performance can be reasonably expected.

V. ANALYSES AND DESIGN DISCREPANCY REPORTS/TRACKING SYSTEM

A. General Discussion

Independent review of analysis is required on Class A and Class B Projects and is optional on Class C Projects (at the discretion of the Project). On a typical project there will be several hundred analyses generated and reviewed. The number of documents involved requires a computerized data base to track the analyses and revisions and to periodically publish project-wide status reports.

The information to be tracked includes such items as:

1. Analysis number
2. Analysis type
3. Hardware to which analysis applies
4. Analysis originator and organization
5. Analysis reviewer
6. Release, revision, and review dates
7. Pass/Fail status
8. Analysis Review Memos

The above list is not intended to be all-inclusive, but only details the core content of the data base. The distinct output of each stage of the independent reviewer's assessment is documented in an Analysis Review Memo, and analyses that are deficient are reported in an "Analysis Discrepancy Memo" (ADM). The ADM and its contents are discussed in greater detail in Section B.

The main product of the analysis review is an assessment of the design adequacy of the hardware which was the subject of the analysis. The analysis review may reveal an actual or potential problem with the hardware design or utilization. The magnitude of the issue can range from a minor impact on the overall mission and/or a remote likelihood of occurrence to a significant or catastrophic impact on the mission and/or likely or certain change of occurrence during the mission. Table V-1 provides examples of several potential design discrepancies revealed by the various reliability analyses. All unresolved design issues are documented on a "Design Discrepancy Report" (DDR). The DDR and its contents are discussed in greater detail in Section C.

The reliability analysis review process is depicted in the flow chart of Figure V-1. Figures V-2 and V-3 are respectively sample status tracking and summary tracking forms. These forms are used to track: (1) analyses that have been reviewed and accepted, (2) analyses that have been received, but need additional work by the originator, and (3) the status of design issues (DDRs).

B. Analysis Discrepancy Memo (ADM)

The ADM is the independent reviewer's written documentation that:

1) Rejects deficient reliability analysis;

2) Describes the specific reasons for rejection (i.e. analysis methods are inadequate, significant errors are discovered, or documentation is incomplete and makes review impossible);

3) Lists the pertinent comments of the reviewer.

The ADM is identified by an "ADM" overstamp on the top of a Section 521 IOM. Subsequent revisions to the ADM may be used to document acceptance of revised analysis.

C. Design Discrepancy Report

Once all the analysis adequacy issues have been resolved, a thorough assessment of the hardware will be contained in the analysis package that represents the hardware. If the independent analysis review identifies an issue regarding the adequacy of the hardware design, a DDR will be issued.

If, during the analysis review, the reviewer discovers one or more discrepancies in the design, the relevant information on each such issue is rated as defined in Figure V-4. This rating methodology is similar to the way Problem/Failure Reports (PFRs) are rated, but instead of utilizing understanding as a discriminator, the analysis issues are rated by the application or fix status. The definitions in Figure V-4 are the criteria used to identify "Red Flag" issues. Once a "Red Flag" issue is identified, it is brought to the attention of the S/C Systems Manager for concurrence with the evaluation, and a Design Discrepancy Report (Figure V-5) is prepared to insure the issues are adequately worked and formally brought off by a closed loop review process. An issue not considered red flag remains on the DDR Summary (see example in Figure V-6) until resolved. All red flag issues and unresolved non-red flag issues are reported to the project on this listing. In order to emphasize the significance of the red flag issues, a summary of these items is prepared (Figure V-7).

D. Implementation Summary

The objective of this system is to implement a process for focusing attention on significant design issues derived from the reliability analysis and provide tracking to their resolution. Figure V-1 describes the process in a simple logic flow diagram. Required analyses are identified in the project reliability plans. Once the required analyses are performed, they are delivered to Section 521 where they are logged in and tracked on a status report (see example in Figure V-2). An independent assessment of the analysis is performed by experienced Reliability Engineers of Section 521 and interacted with the appropriate JPL Cognizant Engineer or JPL Technical

Manager. Analyses are then statused and tracked in a computer database. Periodically, summary status reports, as depicted by Figures V-3, V-6 and V7, are published. Red flag issues are tracked until appropriate corrective action is implemented and the DDR is closed.

TABLE V-1
POTENTIAL DESIGN DISCREPANCIES
REVEALED BY DIFFERENT ANALYSES

Analysis	Potential Design Discrepancies
FMECA and FTA	1. Revelation of previously unknown single failure points. 2. Inability to switch between redundant hardware trains, given a certain initiating failure. 3. The hardware does not possess the degree of fault tolerance (i.e. graceful degradation and/or partial survivability) required, given a certain initiating failure.
WCA	1. Hardware, namely electronic circuits, does not meet requirements under some combination of environmental, interface and/or end-of-life condition. 2. Similar to above item, but discrepancy is associated with violation of some performance margin. 3. Digital timing incompatibilities at key interfaces.
PSA	1. Piece part is found to be operating at too high a stress level (i.e. power, current, voltage or temperature) and violates established derating criteria. The high stress level, if uncorrected, would likely lead to premature failure of the overstressed part. 2. Overstress due to poor assessment of duty cycle or parts parameters.
TA	1. Piece part junction or hot spot temperature limit criteria violated by one of several possible causes; namely, a poor thermal path to baseplate, assumption about duty cycle, dissipation levels and/or thermal properties. 2. Thermally induced fatigue.
SEE	1. Radiation sensitive piece parts. 2 . Intolerable upset rates. 3. Latchup and/or hardware damage.

TABLE V-1 (continued)
POTENTIAL DESIGN DISCREPANCIES
REVEALED BY DIFFERENT ANALYSES

Analysis	Potential Design Discrepancies
Parameter Trend	1. Circuit designs and/or components thereof that do not have adequate performance stability to meet long term (i.e. mission duration) performance requirements. 2. Generic design flaw exists in the hardware.

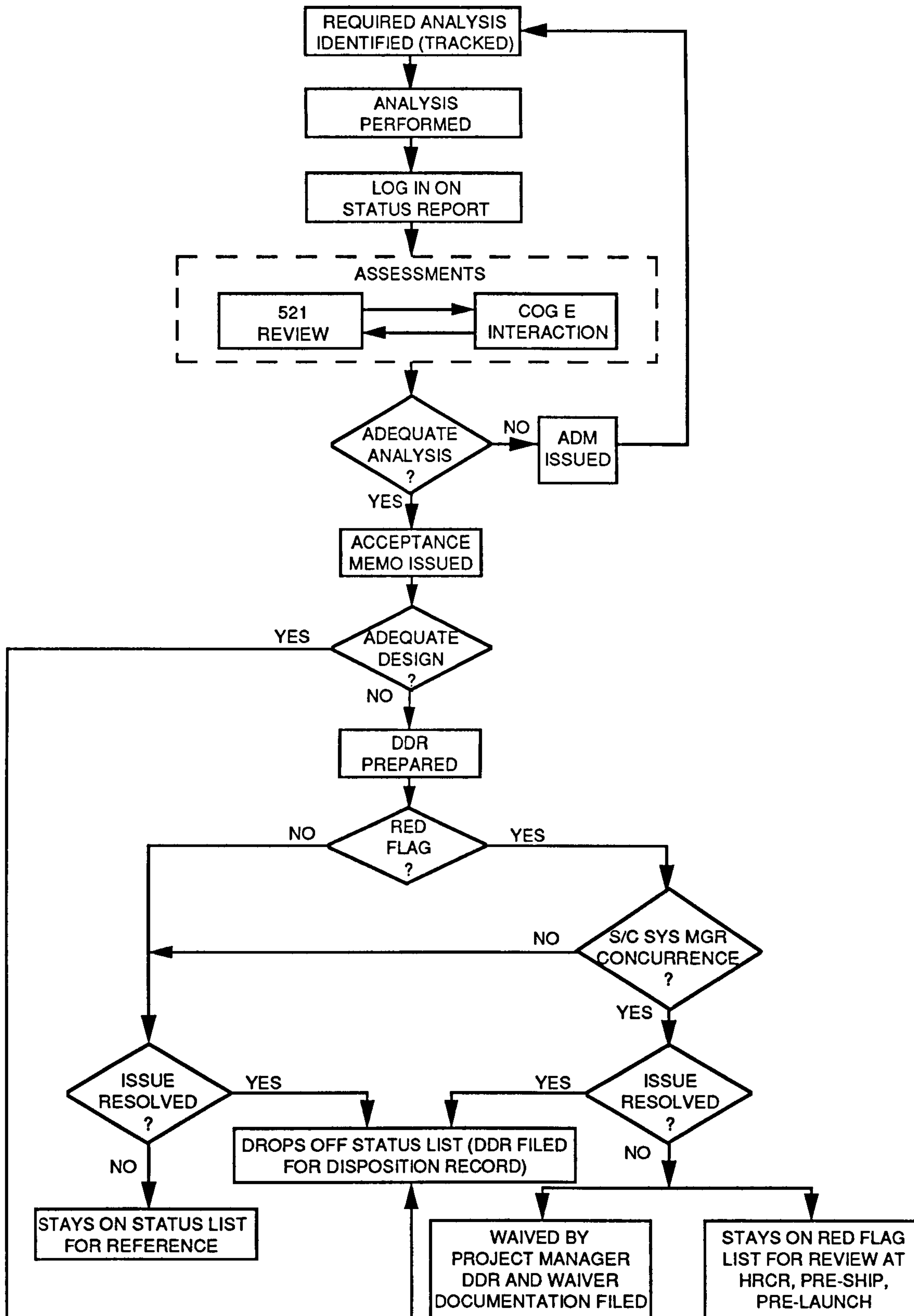

Figure V-1. Analysis Review Process Flow Chart

Contractor: **Martin Marietta Aerospace Co.** 23-MAR-89

Hardware	Report Type	Analysis Number	Rev.	Status	Review Engineer	Memo Number	Rev.	Memo Date	Author
Subsystem: **Articulation & Attitude Control Subsystem**									
AACS	FMEA	VRM-RA-002-006-023	B	Accepted	S. Clohset	NS-89-318		14-FEB-89	Martin
AACS SE	FMEA	VRM-RA-002-006-045	A	521 Review	S. Clohset	NS-89-531		13-MAR-89	Martin
ARU	FMEA	VRM-RA-002-006-009		Accepted	S. Johnson	5131-86-238		11-JUL-86	S. Johnson
ARU	WCA	VRM-RA-002-006-041	A	Accepted	S. Clohset	5211-89-069		6-FEB-89	S. Clohset
						NS-89-238		30-JAN-89	Martin
ARU	SA	VRM-RA-002-006-071		Accepted	D. Bergens	514-DB-251-87		14-AUG-87	D. Bergens
						NSS-87-2157		28-JUL-87	Martin
Buffer Board	FMEA	VRM-RA-002-006-111		Accepted	S. Clohset	5211-89-126		27-FEB-89	S. Clohset
						NS-89-277		7-FEB-89	Martin
Buffer Board	SA	VRM-RA-002-006-043	C	Waiver VPMPR	D. Bergens	NS-88-662		15-APR-88	Martin
	WCA	VRM-RA-002-006-043	C	Accepted	H. Peacock	5131-88-483		26-AUG-88	S. Solomon
						NS-88-662		15-APR-88	Martin
IODA	FMEA	VRM-RA-002-006-112		Accepted	S. Clohset	5211-89-182		14-MAR-89	S. Clohset
						NS-89-278		7-FEB-89	Martin
IODA Cntrllr	WCA	VRM-RA-002-006-035	A	Accepted	S. Clohset	5211-88-536		15-SEP-88	S. Clohset
						NS-88-2496		1-SEP-88	Martin
IODA PS	SA	VRM-RA-002-006-018	A	Accepted	D. Bergens	514-DB-420-88		16-AUG-88	D. Bergens
						NS-88-2137		18-JUL-88	Martin
	WCA	VRM-RA-002-006-018	A	Accepted	H. Peacock	5131-88-407		29-JUL-88	H. Peacock
						NS-88-2137		18-JUL-88	Martin
IODA SSU/ARU	SA	VRM-RA-002-006-019		Accepted	D. Bergens	514-DB-378-88		20-MAY-88	D. Bergens
						4661-DD-88-011		14-APR-88	Martin
						4661-DD-88-012		14-APR-88	Martin
						514-DB-139-86		20-JUN-86	D. Bergens
	WCA	VRM-RA-002-006-019	A	Accepted	S. Clohset	5211-88-535		15-SEP-88	S. Clohset
						NS-88-2497		1-SEP-88	Martin
IODA STU/A-D	SA	VRM-RA-002-006-029	A	Accepted	D. Bergens	5211-88-551		22-SEP-88	S. Clohset
	WCA	VRM-RA-002-006-029	A	Accepted	S. Clohset	5211-88-658		10-NOV-88	S. Clohset
						NS-88-2601		12-SEP-88	Martin

FIGURE V-2

ANALYSIS REVIEW STATUS AS OF (DATE)

ANALYSIS TYPE(S)

SECTION 521 RELIABILITY ENGINEERING

IN PROCESS ANALYSES:

Review Released	A	12
	B	4
	C	17
	D	14
	F	4
Subtotal Released:		51
With Cognizant Engineer		1
With 521		6
Analysis Unassigned		0
TOTAL IN-PROCESS ANALYSES:		58

DELINQUENT ANALYSES:

Not Received	64
TOTAL DELINQUENT ANALYSES:	64

TOTAL ANALYSES: 122

A = Acceptable analysis and report.
B = Internally resolvable problems with the analysis or report.
C = Conditionally acceptable with resolution of identified issues.
D = Unacceptable as is; requires rework of some areas.
F = Unacceptable; lacks resolution of failure modes or does not meet basic requirements.

NOTE: The total number of analyses will change when revised or combined reports are received.

FIGURE V-3. EXAMPLE SUMMARY STATUS REPORT

METHOD OF SCORING AND RANKING ANALYSES / RESULTS FOR ACTION AND STATUS

The categories of potential impact on mission success are:

1 - Minor impact -Can work around the problem should it occur or the effect is not significant.

2 - Significant Impact-Occurrence can have a significant effect on mission performance, but will not lead to loss of the mission.

3 - Catastrophic Impact-Occurrence can lead to loss of the mission or an unsafe condition.

The categories of application/fix are:

1. Redundant circuit or function/fix certain.
2. Single string/fix certain.
3. Redundant circuit or function/fix uncertain.
4. Single string/fix uncertain.

IMPACT	SCORE		APPLICATION/FIX STATUS
Minor	1	1	Redundant circuit or function/fix certain
Significant	2	2	Single string/fix certain
Catastrophic	3	3	Redundant circuit or function/fix uncertain
		4	Single string/fix uncertain

The scores inside the closed area are the Technical Red Flag definers (i.e, 2,3, 3,3 2,4 and 3,4 are defined as Technical Red Flag conditions).

FIGURE V-4. DDR RANKING CRITERIA

Jet Propulsion Laboratory
California Institute of Technology
4800 Oak Grove Drive
Pasadena, California 91109

DESIGN DISCREPANCY REPORT

RED FLAG Approval
Project Management ________

☐ FLT HDW ☐ SE HDW ☐ TEST HDW ☐ S/W ☐ OTHER ________ No. ________

1. PROJECT	2.	3. DATE	4.	5. LOC NO.
	A) REFERENCE DESIGNATIONS		B) NOMENCLATURE	
6. SUBSYSTEM				
7. 1ST TIER HW/SW				
8. 2ND TIER HW/SW				

I — ORIGINATOR No.

9. 10. 11. 12. 13. NOT APPLICABLE — NOTE: C) AND D) NOT APPLICABLE

14. DESCRIPTION OF DISCREPANCY: A) TYPE OF ANALYSIS — B) ANALYSIS NUMBER

C) DESCRIPTION

ORIGINATOR	DATE	COGNIZANT ENGINEER

II — VERIFICATION

15. VERIFICATION & ANALYSIS OF DISCREPANCY

16. IMPACT
1. ☐ MINOR
2. ☐ SIGNIFICANT
3. ☐ CATASTROPHIC

APPLICATION / FIX STATUS
1. ☐ REDUNDANT / FIX CERTAIN
2. ☐ SINGLE STRING / FIX CERTAIN
3. ☐ REDUNDANT / FIX UNCERTAIN
4. ☐ SINGLE STRING / FIX UNCERTAIN

17. NOT APPLICABLE

PERSON COMPLETING SECTION II	SIGNATURE	DATE

III — CORRECTIVE ACTION

18. CORRECTIVE ACTION TAKEN / PROPOSED

19. DISPOSITION
☐ REDESIGNED ☐ WAIVED ☐ OTHER ________

20. EFFECTIVITY
☐ THIS UNIT ☐ ALL UNITS ☐ OTHER ________

21. SAFETY

22. SIGNATURE COGNIZANT ENGINEER	SEC	DATE	SIGNATURE COG SEC MGR	DATE	23. FINAL IMPACT

IV

24. SYSTEM ENGINEER	DATE	PROJECT RELIABILITY ASSURANCE	DATE	25. FINAL LIKELIHOOD

JN / June 89

FIGURE V-5: DESIGN DISCREPANCY REPORT

Design Discrepancy Report Summary

<table>
<tr><th>Number</th><th>Hardware</th><th>Analysis Number</th><th>Rev.</th><th>Cognizant Engineer</th><th>DDR Author</th><th>DDR Date</th><th>Impact</th><th>Status</th></tr>
<tr><td>MGN-228</td><td>SAAM</td><td>VRM-RA-002-006-025</td><td></td><td>J. Plamondon</td><td>M. Adolo</td><td>4-APR-88</td><td>3</td><td>1</td></tr>
<tr><td>DISCRIPTION:</td><td colspan="8">There exists a potential spacecraft single point failure (SPF) traceable to having an electrical short from the high to the low side of the SAAM wrapped cable. This failure would be propagated to the power bus to disrupt power for the entire spacecraft.</td></tr>
<tr><td>DISPOSITION:
Waived
21-APR-88</td><td colspan="8">6 September 88: Solar Array Articulation Mech. Assy.; Waiver VRM-16 approved on April 21, 1988.</td></tr>
<tr><td>MGN-229</td><td>SADH</td><td>VRM-RA-002-006-026</td><td></td><td>J. Plamondon</td><td>M. Adolo</td><td>19-MAY-88</td><td>1</td><td>1</td></tr>
<tr><td>DISCRIPTION:</td><td colspan="8">There exists a potential spacecraft single point failure in the MGN SADH design, traceable to having a seizure between the hinge pin and the hinge bushings.</td></tr>
<tr><td>DISPOSITION:
Closed
21-SEP-88</td><td colspan="8">The SADH has been completely revised because of major design changes. Thus, the SADH (Solar Array Deployment Hinge) has been substituted with the Integral Beam Deployment Hinge (IBDH), whose design has no SPF. The FMEA report on the IBDH will be submitted as VRM-RA-002-006-026A, for JPL review.
15 Feb 89: FMEA for IBDH VRM-RA-002-006-108 has been reviewed and accepted by IOM 5211-88-525.</td></tr>
<tr><td>MGN-230</td><td>SARRD</td><td>VRM-RA-002-006-027</td><td>A</td><td>J. Plamondon</td><td>M. Adolo</td><td>19-MAY-88</td><td>2</td><td>1</td></tr>
<tr><td>DISCRIPTION:</td><td colspan="8">There exist several (8) single point failures in the MGN SARR design, ranging from O-ring and fastener failures to a hang up of the Solar Array push plate on the Damper/Deployment Cartridge body.</td></tr>
<tr><td>DISPOSITION:
Waived
12-SEP-88</td><td colspan="8">6 September 1988: Awaiting Waiver MGN-31A.
10 February 1989: Waiver MGN-31A approved by MMC.</td></tr>
</table>

FIGURE V-6: DESIGN DISCREPANCY REPORT SUMMARY

SUMMARY
ANALYSIS DESIGN ISSUES
(DATE)

This report summarizes the concerns of JPL Reliability Engineering in reviewing the analyses. The analyses concerns have been categorized as follows:

IMPACT SCORE		APPLICATION/FIX STATUS	
Minor Effect	1	1	Redundant Circuit or Function/Fix Certain
Significant	2	2	Single String/Fix Certain
Catastrophic	3	3	Redundant Circuit or Function/Fix Uncertain
		4	Single String/Fix Uncertain

Red Flag Design Discrepancy Reports

DDR CLASSIFICATION

There are 15 records with non-Red Flag risk/impact ratings. There are 4 preliminary ratings which comprise the Red Flag Reports divided as follows:

Impact, Redundancy/Fix	Total
2, 3	1
2, 4	0
3, 3	1
3, 4	0
Sum	2

FIGURE V-7. EXAMPLE RED-FLAG DDR SUMMARY

VI. MISCELLANEOUS ISSUES

A. <u>Risk Assessment</u>

1.0 Introduction:

Risk is exposure to the chance of injury or loss. Risk assessment is an evolving technical specialty. Currently it consists of two approaches, the qualitative and the quantitative approaches. Within NASA, the qualitative approach dominates as the preferred approach. In other industries (ie nuclear & chemical), where societal risks are a significant issue, the quantitative approach has been a major focus for the past ten to fifteen years.

In general terms, risk assessment can be thought of as an evaluation of a situation where the following three questions are addressed:

1. What can go wrong?
2. How likely is it?
3. What are the consequences?

The situation under evaluation can be any of a diverse range of human activity including technological hardware (ie transportation, energy generation, chemical production & distribution, or space exploration), a health issue (ie safety of new prescription drugs, diseases, epidemics, or the hazards of smoking or obesity), or natural phenomena (fires, floods storms, or earthquakes).

In each case the results of the risk assessment is used to determine the importance of undesirable outcomes of the activity and make decisions about the situation that would reduce the likelihood of the outcome and/or the consequence of the occurrence. This process is risk management. On NASA programs, risk management is the process of balancing risk with cost, schedule, and other programmatic considerations. It consists of risk identification, risk assessment, decision-making of the disposition of risk (acceptance, tolerance through waivers, or mitigation), and tracking the effectiveness of the results of the action resulting from the decision.

2. Qualitative Risk Assessment:

Qualitative risk assessment addresses all of the general issues described above in a qualitative way. In this approach, the description of "what can go wrong?" is addressed by a technical description of all known events that can lead to an undesired outcome. Likewise, the likelihood and consequences are also addressed by technical descriptions. For example, the likelihood of an event might be described as low, medium or high when compared to other possible events.

Qualitative methods previously used in NASA are based on standard engineering, reliability, and system safety analyses, including the various

types of hazards analysis and failure modes and effects analysis (FMEA),. Currently, an enhancement of the foregoing procedures, critical failure modes and other hazards identified through the hazards analysis and FMEA processes are categorized and prioritized at least with subjective ratings of the frequency and severities of mishaps that potentially can arise from the hazards. Risk acceptance or risk mitigation decision-making is guided by these ratings, to the extent possible, taking into account the uncertainties in them. In many cases, the risk assessment focuses on the differential risk with and without actions implemented to mitigate the consequence of the undesired event. In addition, the results can be coupled with cost/benefit evaluations to decide if the benefits resulting from the mitigation efforts out weigh the cost of those efforts.

3. Quantitative Risk Assessment:

Quantitative risk assessment (QRA) methodologies have evolved over the past thirty years. QRA had its beginnings, in the late 50s and early 60s, in the field of economics and finance where the risk of loss of money was the issue. By the late 60s and early 70s, the methods were being applied to technology (Ref.8), specifically those technologies perceived to be hazardous. Following the Space Shuttle Challenger accident, in Jan 1986, there was considerable political pressure to apply QRA methods to the manned space program. In response, NASA funded several trial applications (Ref.9). In addition, a NASA Management Instruction (NMI 8070.4, Ref 10) was issued. In this instruction, NASA made it clear that there was a role for QRA, but most risk assessments would rely on the qualitative approach, especially existing programs. Only special issues, such as the Galileo RTG safety, would be candidates for QRA (see refs. 11 & 12). New programs, like the Space Station Freedom, will rely heavily on QRA.

QRA models, like their quantitative risk assessment counter parts, are based on engineering or scientific representation of the situation under evaluation. The QRA approach differs primarily in the quantification of the likelihood of the event occurrence frequency. Thus the QRA approach includes the following three elements:

1. Event scenarios leading to the undesired outcome
2. Estimated frequency of occurrence, including uncertainty
3. Consequence of event scenarios.

As with the qualitative approach, the QRA results are used to make decisions about the assessed activity. The risk assessment may focuses on the differential risk with and without actions implemented to mitigate the consequence of the undesired event or the results may be coupled with cost/benefit evaluations to decide if the benefits resulting from the mitigation efforts out weigh the cost of those efforts. One of the advantages of the QRA approach is the fact that the results are quantitative. That is, the decisions are based on the numerical results of the evaluation. Of course the numerical results are not accepted blindly, but are scrutinized in great detail before the numbers are accepted for

comparison. In addition, uncertainty associated with the analysis, say the frequency of occurrence of an event and/or the consequence of that event, can be propagated through the analysis and their effects on the final result established. Thus, once the model's integrity is established, the conclusions of the evaluation are clear and undisputed

B. Automated Analysis Tools

Many automated analysis tools, i.e. , computer programs, exist which help perform the analyses discussed in Section III. Many programs perform the same analyses with similar capabilities, but generally, they all have different limitations of which the user must be aware. Table VII-1 provides a listing of some of the programs available to perform the analyses discussed in this document. Along with the program name is a short description of the specific types of analyses performed. If it is known, the company which developed the software is listed after the name of the program. Table VII-1 is not comprehensive; it provides examples of available software. The reader may wish to obtain further information on the programs which may be applicable to specific project needs.

It should be noted that a spreadsheet program can greatly ease the performance of a FMECA. Also, SEU analysis can be partitioned into analysis of the upset rates and the effect on part/circuit performance. Circuit analysis programs may be used to determine the performance effects. Additionally, standard statistical packages which include regression algorithms may be useful for Parameter Trend Analysis (for example, MINITAB).

NAME	DESCRIPTION
FMECA	
PREDICTOR	Automates FMECA and performs reliability prediction.
Worst Case Analysis:	
ACCUSIM [Mentor Graphics]	Performs AC, DC, power supply, transient, and sensitivity analog WCA and PSA.
ANALOG WORK BENCH	Performs analog and power supply WCA and PSA.
CADAT	Digital analysis program.
CIRCUS	Performs DC, transient, and optimization analysis.
COMPACT	Performs RF and microwave optimization.
E-SOFT	Performs microwave WCA.
ECA [TATUM Labs (Newtown, CT)]	Performs AC and DC extreme value WCA and sensitivity analysis.
HSPICE	Performs microwave WCA.
JTRAC	Performs analog WCA using extreme values.
LASAR	Logic simulation program.
MICRO-CAP [Spectrum Software (Riverside, CA)]	Performs AC, DC, transient and Fourier extreme value analysis.
MICROLOGIC [Spectrum Software (Riverside, CA)]	Logic simulation program.
MOTIVE	Digital WCA program.
PSPICE [MICROSIM (Tustin, CA)]	Analog WCA program; includes AC, DC, transient, and sensitivity analyses.

Table VI-1: Partial List of Automated Analysis Tools

NAME	DESCRIPTION
Worst Case Analysis (Continued):	
QUICKPATH [Mentor Graphics]	Performs digital timing WCA.
SCEPTRE	Performs AC, DC, transient, and sensitivity WCA.
SPICE [MICROSIM (Tustin, CA)]	Performs AC, DC, transient, and sensitivity analyses.
SUPER COMPACT	Performs microwave WCA.
SYSCAP [Information Systems Design (Santa Clara, CA)]	Performs AC, DC, and power supply WCA, PSA, and transient, Fourier, & sensitivity analysis via extreme value or Monti Carlo. SYSCAP also allows modelling of SEU effects on circuit operation.
TEGAS [Information Systems Design (Santa Clara, CA)]	Digital WCA program.
TVER	Digital WCA program.
VALID	Performs analog and digital circuit analysis and simulation.
Part Stress Analysis:	
ACCUSIM [Mentor Graphics]	Performs analog PSA.
ANALOG WORK BENCH	Performs analog PSA.
SYSCAP (Information Systems Design (Santa Clara, CA)]	Performs analog PSA.
Structural Analysis:	
DISCOS [COSMIC]	Performs dynamic simulation and stability analysis of passive and actively controlled spacecraft.

Table VI-1: Partial List of Automated Analysis Tools (cont.)

NAME	DESCRIPTION
Structural Analysis (Continued):	
NASTRAN [COSMIC] ANASYS	Program to perform finite element structural modelling.
VAPEPS [JPL]	Program to analyze vibro-acoustic effects on structures.
Thermal Analysis:	
MITAS	PC based code similar to SINDA
SINDA [COSMIC]	Industry standard thermal analyzer. 3-D steady state and transient finite difference code.
TRASYS II [COSMIC]	Industry standard radiation interchange code. Output to a SINDA input file.
Fault Tree Analysis:	
MFAULT [Batelle Pacific Northwest Labs (Richmond, WA)]	FTA cut set prediction program.
MOCUS [EC&G Idaho Inc (Idaho Falls)]	Calculates minimal sets from Fault Trees.
FTAP/Importance	Identifies cut sets and event probabilities.
Single Event Upset Analysis:	
RADSPICE	Models effects of radiation on circuits.
SEU Programs [JPL]	Set of programs which calculate the environment, shielding, flux
SYSCAP [Information Systems Design (Santa Clara, CA)]	Allows modelling of EMC effects on circuit operation.
CREME [NRL]	

Table VI-1: Partial List of Automated Analysis Tools (cont.)

NAME	DESCRIPTION
Reliability Prediction:	
CARE III [COSMIC]	Program to predict the reliability of complex redundant systems.
MATH MODEL FOR RELIABILITY TRADE STUDIES [COSMIC]	Program to assess competing system redundancy designs.
PREDICTOR	Performs reliability predictions and FMECAS.
TIGER [COSMIC]	Simulation program to evaluate system reliability, readiness and availability.

Table VI-1: Partial List of Automated Analysis Tools (cont.)

C. Reliability Allocation and Assessment

1.0 RELIABILITY ALLOCATION

INTRODUCTION

The process of allocating an overall system reliability goal is limited to those systems that have missions which have a substantial prior history upon which to draw. Typical of this is the ground support equipment for aircraft and spacecraft, operational military systems for land, sea and air, and in some cases, even spacecraft of the TIROS class and communications satellites such as COMSAT, etc. However, for unique space missions, such as planetary exploration or earth orbiting special sensor packages, it is not possible to take prior information and construct a reasonable model for reliability. There are those who do construct such models but the validity is lacking. On the other hand, subsystem reliability for such missions may be accessible by reason of similarity of hardware and environmental factors. Complex space missions have multiple means of accomplishing many of the required functions through reconfiguration or reprogramming and these affect the ultimate demonstrated reliability, but it is usually not possible to factor these into a model. For these reasons we usually do not attempt an allocation for such space missions.

1.1 METHODOLOGY

a) Where a data base adequate to establish the lower bounds for hardware reliability values exists, it is possible to use the prior values for equipments as a first approximation and compute the overall reliability resulting from them. Where the resulting value is at least as high as the contractually specified value the individual and subsystem values can stand as the prima facie allocation. These can be modified as in 2. below.

b) Where no valid data base exists or MIL-HDBK 217 estimates are not available or appropriate, the following method is often used and has some justification.

1. Assume that all components (black boxes) are of equal value and allocate the overall system unreliability (1-reliability) to give each non-redundant component and any redundant groups of components the common average unreliability value.

2. Modify these allocations by factors that depend on the following:

   a. Relative complexity
   b. Mission environment effects
   c. Criticality to mission success
   d. Degree of uncertainty about the techno logy involved
   e. Adjust discrepancy with overall requirement

3. Reallocate at intervals as increased knowledge affects any of the above factors.

2.0 RELIABILITY ASSESSMENT AS A TRADE-OFF TOOL AND SPARES DEMAND PREDICTOR

INTRODUCTION

At the outset, let it be understood that JPL discourages the use of mission probabilities, however derived. The use of MIL-HDBK 217 is particularly prone to error through the failure to understand the full implications of the assumptions underlying its use. Comparative analysis, such as that used in configuration trade-off studies, is of a different nature. By judicious use of probability ratios or equivalent, the errors of assumption tend to cancel and a reasonably useful comparative result is obtained. One may make such statements as, "this configuration is about 20% better than that", without stating any absolute magnitudes. This might be true if the use of higher reliability parts is compared to a configuration with redundancy.

The use of such probabilities in a cost/risk analysis is itself a risky process. To say that the probability of occurrence of a particular failure is so much, using the 217 handbook (Reference 6) as the only source of information, should not be done unless there is a way to verify the "sanity" of the prediction by outside data. Even then, "close calls" should not be decided on this basis alone. Every attempt should be made to get expert opinion and utilize good judgement at every stage.

A word must be said about part reliability processing. The use of parts of unknown or questionable pedigree by adding burn-in and screening tests is not to be taken as equivalent to the use of true high reliability parts. We never get enough part life history in test to assure that hidden defects (such as might be caught in pre-seal visual inspection) or excessive contaminants that may migrate over time, are not a significant potential cause of failure in the mission. Derivation of activation energies in the small sample test we perform is of small value in the prediction of the failure mechanisms over long periods of time. None of this is to say that we do not get any increase of confidence in parts/assemblies that accumulate longer test times in the various stages of integration and testing.

The reduction of infant mortality failures is of some benefit. However, unless the basic part lot is homogeneous and of high manufactured quality, there is no assurance that the population can be segregated into strong and weak groups with the strong being the dominant sub-population. In this case early failures do not indicate that the remaining population is really good. This assumption is basic to the use of any failure rate category from 217 and particularly the high-rel screened categories.

With the above caveats in mind we can evaluate the analytical methods. First, the computer program, if any, used for the analysis must be adequate to the task. Second, the assumptions that are made must be fully understood and conservative. The use of the E revision of 217 is very good since greater emphasis on space environments is given. One possible criticism; for missions longer than 15-18 months, the exponential distribution, upon which 217 is based, becomes increasingly pessimistic for electronic parts, while it becomes increasingly optimistic for electomechanical and mechanical parts after about two years. The use of the Weibull and Log Normal distributions respectively is recommended as these distributions could lead to more accurate predictions. However if the probability or other ratio, as mentioned above, is used this is of less concern.

2.1 METHODOLOGY

a) TRADE STUDIES - For reliability predictions to be used in trade studies the MIL-HDBK-217 is a source of failure rate data for hardware which has no other source. Very early in the program, where little is known about the details of circuit design , it is possible to get useful results using the parts count method. This must not be used for designs about which the application information for parts is available since it is biased to the conservative side and could lead to overdesign. If at all possible, the effort should be spent to get the application stress data needed for the stress method.

After doing predictions for the competing design configurations, a ratio is formed using the lowest MTBF (reciprocal of failure rate) as denominator and each of the values for the configurations as a numerator in turn. Then the relative merits of these can readily be seen. Where redundancy is one of the configurations, the MTTF (mean time to first system failure, sometimes called MTBCF or mean time before critical failure) must be computed using a "k-of-N" method. Where k is the minimum number of elements needed for success and N is the total number of available redundant elements.

b) SPARES PREDICTION - For repairable systems it becomes necessary to forecast the demand for spare replacement units. In this case the MTBF (or mean-time-between-failures) for each replaceable element (e.g. module, card or assembly) provides a rational means of allocating scarce resources to get a maximum chance of not running out of spares. Historic data is, of course, the best source of the MTBF values needed, but in their absence a 217 prediction is better than no information at all. The caution to be observed is to recognize the potential error in such predictions and to apply engineering judgement to the spares allocations generated by LSA programs from MTBF values.

D. Margin Testing As An Alternative to WCA

PURPOSE

It should be recognized that for projects having mission times on orbit exceeding a year, or two at most, circuit "Worst Case Analysis" (WCA) is the preferred method of assuring circuit integrity under the constraints of thermal aging, radiation degradation and initial spread of part parameters.

This section describes the test objectives and constraints for the application of the method of "Voltage/Temperature Margin Testing" (VTMT). It should be noted that while WCA is the preferred approach, it is recognized that for reasons of hardware inheritance, design complexity, or project constraints, VTMT may be a viable alternative.

Sufficient margin must be demonstrated on "Beginning of Life" (BOL) hardware to permit confident performance extrapolation, which includes those conditions unachievable at BOL, such as radiation effects, initial part tolerance variations (except when flight unit related), part aging, and unit to unit variations which define "End of Life" (EOL) conditions. a Margin Budget for each of these effects must be developed to determine, in a quantitative way, the magnitude of the required margins for testing by using the WCA defined approach for EOL deltas in parameters.

The test constraints defined herein are intended to simulate EOL conditions on BOL hardware.

TEST OBJECTS

For purposes of test definition, the possible types of test hardware objects are defined as either

1. Power Supplies (PS) (includes power converters supplied as an integral part of a functional assembly)

2. Analog Circuits (A)

3. Digital Circuits (D)

These may occur in the defined configurations of either

A. Brassboard - An assembly which is flight like in mechanical configuration (particularly thermally), but need not be constructed to and inspected to full QA requirements.

B. Protoflight or Flight - Fabricated to configuration controlled specs and drawings and certified to full QA requirements.

C Inherited - Flight quality hardware fabricated for a different project and previously flight qualified by either test or flight experience.

The test object configurations must be fabricated from parts which are either flight type or which are electrically and mechanically interchangeable with the flight parts. The use of parts which may not be fully screened or certified increases the unknowns in the process and may invalidate results. At very least, this would increase risk and should be assessed against the possible gains of WCA.

The test objects may be separately tested as multiple sub-assemblies, provided that the electrical interfaces and thermal environments are shown to be equivalent to the flight configuration.

An approved detailed test plan must accompany each test object, and a detailed test report must be issued after test completion and both must be reviewed and approved by an independent JPL approved reviewing organization.

TEST PLAN

The test plan should include the following as a minimum:

1. Identification of test object (TO).

2. Configuration of TO (i.e. applicable mechanical and electrical drawing and revision.

3. Specification pass/fail criteria or other definition of success criteria.

4. Justification of the voltage and T/V at qualification shearplate levels. This should include a discussion of the ramp rate/time and dwell time for each step.

5. A test matrix consisting of

   A. Voltage/Temperature intersects
   B. Operating modes at those intersects
   C. Circuit type (A, D, or PS)

6. A Margin Budget with the rationale for the margins chosen for each performance measurement and the voltage and temperature limits for each V/T intersect. (See Purpose above)

In general, the test should be configured to simulate the worst temperature and voltage combination for the circuit type under test. Tests shall not be considered valid unless internal circuit (secondary) voltages, as well as power supply input (primary) voltages, are varied over their limits. Those limits must be adequate to span the worst case source

variations plus additional margin to verify compliance with EOL load performance variations.

VII. REFERENCES

1. JPL D-1489, Rev. B, "Flight Equipment Classifications and Product Assurance Requirements", Jet Propulsion Laboratory, January 1990.

2. JPL D-5945, "JPL Standard for Waiver Requests", Jet Propulsion Laboratory, August 1989.

3. JPL IOM 5130-87-43, "Resolution of Analysis Issues", T. Gindorf to Distribution, April 17, 1987.

4. MIL-HDBK-338, "Electronic Reliability Design Handbook", Oct. 15, 1984.

5. JPL IOM 5210-89-42, "Reliability Analysis Tracking and Status System", T. Gindorf to Distribution, April 5, 1989.

6. MIL-STD-217C, "Reliability Stress and Failure Rate Data for Electronic Equipment".

7. "Spaceflight Significant Events File", JPL Office of Engineering and Review, April 30, 1987.

8. "Technology Assessment. I - Weighing the Benefits and Risks of New Technologies," Research Management, Vol. 13, p. 409-425 , C. Star (Univ of Calif., Los Angeles).

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10. NASA Management Instruction, (NMI 8070.4), "Risk Manag ement Policy for Manned Flight Programs," dated Feb. 3, 1988.

11. NASA Headquarters Code Q, Independent Assessment of Shuttle Accident Scenario Probabilities for the Galileo Mission, Vol. 1 & 2, Apr. 1989.

12. Final Safety Analysis Report for the Galileo Mission, Vol I,II, and III, Document No. 87SDS4213, Prepared for the Department of Energy, General Electric, Astro-Division, Spacecraft Operations, Valley Forge Space Center, Philadelphia, Pa.

APPENDIX A

FAILURE MODES EFFECTS AND CRITICALITY ANALYSIS (FMECA) GUIDELINES

1.0 INTRODUCTION

The purpose of the FMECA is to identify potential hardware design deficiencies and single-point failures. This design process is a systematic and documented analysis of the credible ways in which a system can fail, the causes for each failure mode, and the effects of each failure. The objective of the FMECA is to identify all single function failures and their effect on performance in order to validate redundancy or partial survival capability, and to verify that lower level failures do not propagate into the Spacecraft: thus the FMECA is a prime analytic method to guide design and system trade-off study.

A FMECA will be performed at the functional block level. In addition, a piece part FMECA is required at all unit to unit interface circuits to preclude any propagation of irreversible hardware failures. A piece part FMECA is also required on the support equipment-to-flight equipment interface circuits to preclude the propagation of support equipment failures into the flight units (assemblies).

It is JPL policy that connectors, harness, and internal wiring failures will be included in the FMECA only for those connections which have not been verified prior to launch by a subsystem or system testing and have remained mated.

2.0 STEPS IN PERFORMING FMECA

There are six essential steps in the performance of an FMECA:

(1) Reliability block diagram construction: A reliability block diagram is constructed indicating the functional dependencies among the various elements of the system. The detail should be down to the part level at interfaces between units.

(2) Failure definition: Rigorous failure definitions must be established for the system, subsystem, and all lower equipment levels. As a minimum, the part failure modes to be assumed are given in Table A-1.

(3) Failure effect analysis: A failure effect analysis is performed on each item in the reliability block diagram. This takes into account each different failure mode of the item and indicates the effect of that item's failure upon the performance of the next higher level in the block diagram.

(4) Bookkeeping task: The system and each sub-item must be properly identified and indexed.

(5) Critical items list: The critical items list is generated or updated based on the findings in steps 1, 2, and 3.

Table A-1. Minimum Part Failure Mode Assumptions

Part	Failure Mode
Capacitors	Short Circuit Excessive leakage (electrolytic) Open circuit
Circuit breakers	Failed open Failed closed
Coils	Open winding
Connectors	Shorts (pin to pin) (see 7.0) Shorts (pin to gnd) Opens (pin to pin)
Diodes	Short circuits Open circuits
Insulators	Electrical breakdown
Microcircuits (outputs only, digital and analog)	Saturated High Saturated Low Open (Hiz output)
Microprocessors	
Functional	TBD
Output lines	Same as microcircuits
Relays - electromechanical	Contact permanently closed Contact permanently open Excessive contact bounce
Resistors	Open circuit
Switches, rotary	High resistance contact Open/Short
Switches, toggle	Permanently open Permanently closed
Transformers	Shorted turns Open circuits
Transistors - silicon	Shorted CE Shorted CB Open circuit C, B, or E

(6) Documentation task (or as directed for Class C & D Programs): Define the baseline design configuration and operation. List the FMTCA assumptions. Attach completed FMECA worksheets, and (See Figure B1) supporting diagrams, drawings and analyses.

3.0 IDENTIFICATION OF CRITICAL FAILURE

Based on the failure effects analysis, a list of critical items is prepared. This list contains those items whose failure can result in a possible loss, probable loss, or certain loss of the next higher level in the reliability block diagram All items that can cause system loss should be identified clearly by their inclusion in the critical items list.

4.0 SINGLE POINT FAILURE IDENTIFICATION

Critical failures must also be identified in accordance with the Program Policy and Procedures Manual provisions for single point failures.

5.0 REDUNDANT BLOCK FMECA

Subsystems incorporating block redundancy must be subjected to a FMECA at the piece part level for all subsystem interface circuits between the redundant blocks and the sensing/switching circuits. This piece part FMECA is done to verify redundancy and partial survival capability for blocks with redundancy.

6.0 INTERLOCKING SYSTEM LEVEL FMECA

Multiple FMECAs are required to carry the chain of failure effects from the lowest level failure sources to the spacecraft level for some complex subsystems. The determination of a single point failure (SPF) at the spacecraft level may require an analysis of effects beyond the interface of the subsystem or system generating the failure and its effects. Multiple system effects may be generated directly from the single initial failure, some of which may result in a SPF in another system. The Fault Detection System (FDS) may prevent a SPF in a way not evident to a subsystem designer generating a lower level FMECA.

An interlocking higher level FMECA will be provided when a lower level FMECA is determined to lack sufficient visibility into the criticality of failure effects at the spacecraft level. The overlap between the lower level and higher level FMECAs should be adequate to allow analysts working at either level to communicate effectively (equipment to spacecraft and in the reverse direction). Clear understanding of the cause and effect relationships of failures that can cause SPFs must be documented.

The inability of a lower level FMECA to clearly resolve a SPF effect by the Preliminary Design Review (PDR) should immediately trigger a request for the generation of a higher level FMECA to define the SPF potential of the design in question.

The higher level FMECA (usually to the spacecraft level) should reference the lower level FMECA reviewed at the PDR. Additional failure modes arising at the PDR and design concerns resulting from the PDR are additional inputs besides the lower level FMECA at the start of the spacecraft level FMECA.

7.0 CONNECTOR, CABLE AND INSULATOR FAILURES

Because of the relatively benign nature of the mechanical and physical environments of a spacecraft, certain simplifying assumptions can be made relative to connector and cable failure FMECAs. These assumptions are based on the following facts:

A. The unit (box) and spacecraft design integrity of conductors and insulators has been verified by the flight qualification or protoflight test process.

B. Any multiple units are built and inspected to the same drawings and manufacturing processes as the qualified units.

C. The mating of all required harness interconnects is considered validated provided they have been exercised by an appropriate subsystem or system test and have not been demated since the test.

Those connectors for which FMECAs <u>are required</u> are as follows:

1. Connectors which were not verified for mating by a subsequent subsystem or system level test (umbilicals, pyros, etc.).

2. Connectors for which mismating could result in serious personal injury or hardware damage upon initial mating (i.e. to energy sources or powered mechanisms).

3. Connectors which are part of a cable assembly which experiences multiple (greater than ten) flexings as a part of its normal operation unless the full mission flex life has been demonstrated by test.

In these three cases, all physically realizable pin to pin and pin to shell shorts, as well as opens, must be considered by the FMECA.

8.0 FMECA EXAMPLE

Many treatments of failure mode, effects, and criticality analysis (FMECA) methodology have been developed and any rigorous treatment is acceptable. Figure A-1 is an example of a portion of a FMECA.

Identify and list the individual functions from a functional block diagram of the hardware to be analyzed. Break the system down to the lowest level functional hardware blocks. The composition of each block will be determined by the type of system being analyzed. It is not the intent to reduce block detail to the individual part level. It is intended that the hardware be

broken down to those functions which are essential to the task for which the hardware was designed. For example, power circuits are designed to deliver voltage and current. The functions involved in this task are usually source isolation, rectification, voltage multiplication, filtering, feedback regulation, overvoltage protection, and current limiting. All redundant or repetitive blocks should not be so complex that they encompass multiple internal functions.

Draw the block diagram with all the internal interconnections. Label the blocks and connections with sufficient detail for positive identification with schematics and other identified design sources. All external functions, command inputs, loads, and environments should also be analyzed if sufficient knowledge is available. Otherwise they must be described to the fullest extent possible.

If a block critical to the hardware performance has an excessive number of failure modes, it is a candidate for further study (FMECA at the piece-part level or other appropriate technique).

The details of required data for each column of the FMECA worksheet (Figure A-2) are defined below:

(1) Item. Name of the item under analysis. The system under analysis shall be divided into the lowest level of description practical. Include the drawing number of the reference designator by which the contractor/manufacturer identifies and describes each item or standard grouping of items.

(2) Mission phase. If appropriate, identify the mission phase(s) for which an item failure mode is being investigated (i.e., ground check, prelaunch, attitude stabilization, cruise, midcourse maneuver, final man-maneuver, orbit).

(3) Failure mode. Describe the specific failure mode, considering (as a minimum):

(a) Premature operation.

(b) Failure to operate at a prescribed time.

(c) Failure to cease operation at a prescribed time.

(d) Failure during the prescribed operating period (nonstandard operation).

Typical failure modes are: no output, rupture, drift, excess noise, etc.

(4) Most Probable Failure Cause. Describe the mechanism which has the highest probability of inducing the failure. This entry establishes the credibility of the failure mode.

(5) Failure Effect. Describe the effect of the item failure mode on:

(a) System.

(b) Interfaces.

(c) Other items.

(d) Mission.

(6) Criticality and Probability. Describe and rank the criticality of the function from 1 to 6 with 6 being most critical to the mission success as defined below:

6 - complete loss of mission: complete loss of primary mission capability.

5 - major loss or degradation of mission: capability to complete some mission objectives (or all at a degraded level) with immediate loss of a critical science instrument or loss of a major amount of critical science data, or major reduction in life of mission, or loss of spacecraft function resulting in loss of opportunity for obtaining critical science data.

4 - significant loss or degradation of mission: significant loss of spacecraft or instrument function leading to a significant loss of data, or a significant reduction in life of the mission.

3 - loss or degradation of a redundant subsystem: loss or degradation of a subsystem or science instrument producing levels 6, 5, or 4 criticality, if remaining redundancy is lost.

2 - potential for major or significant degradation of spacecraft or performance: no immediate impact on spacecraft or mission, but potential exists for future loss, at level 6-3, due to induced failure, or resulting from the conjunction of this anomaly with a future event, or potential for cumulative major loss of function over a long period of time; or major or significant degradation of mission, at levels 6-3, would have occurred if adequate alternatives or measures had not been implemented.

1 - minor or no impact on spacecraft life or performance: noticeable or no degradation, but does not lead to instrument loss, or loss of significant amount of data, or significant reduction in quality of data, or significant peril to mission.

Determine whether the probability of the failure occurring is high, low, or medium.

(7) SPF - Single Point Failure of the Mission if the mission is terminated. If unable to define at this level of analysis attach a document requesting a determination from the project office.

(8) Failure Mode Detection. Identify the indicators by which a particular failure mode is detected (test, inspection, or TLM), and list specific tests or monitor points, as well as a qualitative assessment of the indication.

(9) Remarks. List appropriate remarks with respect to each failure mode.

ITEM	MISSION PHASE	FAILURE MODE	MOST PROBABLE CAUSE	FAILURE EFFECT		PROBABILITY/ CRITICALITY TO MISSION	FAILURE MODE DETECTION	REMARKS
				SUBSYSTEM	SYSTEM			
BATTERY	BOOST	SHORTED CELL	(a) BREAKDOWN OF CELL SEPARATOR	REDUCED BATTERY VOLTAGE	LESS POWER AVAILABLE, MIGHT LIMIT MISSION SUCCESS	MEDIUM TO HIGH/MEDIUM	LOW FLIGHT T/M VOLTAGE	PROPER SEPARATOR SELECTION, PLATE/CELL FAB & QC SHOULD REDUCE PROBABILITY
			(b) METAL PARTICLE IN CELL					MONITOR CELLS FOR LOOSE PARTICLES DURING VIBRATION TEST
		OPEN CELL	(a) BROKEN CELL INTER-CONNECTS	BATTERY VOLTAGE BECOMES ZERO	REMOVES BATTERY FROM S/C SYSTEM	HIGH/HIGH	FLIGHT T/M VOLTAGE GOES TO ZERO	REDUN-DANCY WOULD GREATLY REDUCE PROBABILITY
			(b) BROKEN CASE-ELECTROLYTE LEAKAGE	(1) REDUCED CELL VOLTAGE	(1) REDUCED POWER AVAILABLE	(1) MEDIUM DURING LEAKING, HIGH/ MEDIUM WHEN DRY	FLIGHT T/M VOLTAGE DECREASES	VIBRATION TEST SHOULD VERIFY CASE DESIGN
				(2) COULD DAMAGE ADJACENT HARDWARE	(2) COULD SHORT OPEN ELECTRICAL CIRCUITS	(2) HIGH/HIGH		

Figure A-1. FMECA Example

Failure Modes, Effects, Criticality, and Analysis

Date: __________

Analyst __________
Indenture Level __________

Assembly Name: __________

Schematic No. __________
Location __________

Item	Mission Phase	Failure Mode	Most Probable Cause	Failure Effect		Probability/ Criticality to Mission	Failure Mode Detection	Remarks
				Subsystem	System			

Figure A-2. FMECA Worksheet

APPENDIX B

WORST CASE ANALYSIS GUIDELINES - CIRCUIT AND POWER SUPPLY

1.0 PURPOSE AND SCOPE

As part of the design and development of spacecraft and instruments, a worst case analysis (WCA) program is required. Performance of a WCA is an effective means for assuring the presence of positive design margins in electronic circuits. The WCA should be an integral part of the design of every electronic assembly. The analytical results will serve to assure proper operation of the circuit under the most unfavorable combination of realizable conditions or to identify potential performance problems for circuits whose worst case analytic results show deviation from specified performance requirements. The WCA should be performed as the design evolves, but prior to design freeze (i.e. CDR).

This document is intended to guide the Cognizant Engineer or his designated analyst in the performance of a worst case analysis. This analysis usually is required of all electronic assemblies.

2.0 APPLICABLE DOCUMENTS

D-XXXX	Environmental Requirements Document
JPL TM-33-763	Radiation Design Criteria Handbook
JPL 81-66	Total Dose Radiation Data for Semiconductor Devices (3 Volumes)
JPL ZPP-2061-PPL	Preferred Parts List
JPL "RADATA"	Radiation Effects Electronic Data Base

3.0 REQUIREMENTS

3.1 TRUE WORST CASE ANALYSIS

The analysis will be true worst case in that the value for each of the variable part parameters will be set to limits which will drive the output(s) to a maximum or minimum or both, depending on the circuit function. Consideration shall be given to AC, DC, and transient effects on the circuit being analyzed. Circuits consisting of interconnected digital IC's of a singular technology (e.g. all LSTTL, all CMOS, etc.) will be subject to worst case analysis for timing and capacitive load considerations and possible "race" conditions. Mixed digital technologies also require interface compatibility analyses.

One of the most important elements in the WCA is the part parameter variations used for the piece parts in solving the circuit equations. If a design is to pass a WCA, it must be designed with the same worst case part parameter variations to which it will be subjected in the WCA. Tables B-1 through B-8 serve as a guide for part parametric variations to be used in the performance of the worst case analysis.

3.2 PROCEDURAL CONSIDERATIONS

To facilitate the performance of the WCA, the analyst may reduce complex circuits to smaller functional blocks. By using this approach the analysis becomes more manageable, so both the analyst and the reviewer are aided. When a circuit is reduced to these functional blocks, performance requirements for each block need to be established. Both input and output requirements should be established. These requirements will serve as the evaluation criteria for the WCA results for the functional blocks. If such criteria exist in another document (e.g., design verification requirements document), reference to the source document should be made. Some of the requirements for the functional blocks will have to be derived from higher level specification requirements. In that case, the method of deriving these requirements shall be clearly shown.

The WCA report should show compliance with all requirements, both on the functional block level and at the circuit level. Deviations from these requirements are to be noted explicitly and any proposed solutions outlined as part of the report. Proof of compliance to certain less significant requirements may be omitted provided that adequate justification for the specific omission is given in the WCA analysis report. It is recommended that the assumptions and approach to be used in the analyses be concurred with by the project Reliability Engineer prior to the performance of the analyses. To simplify the discussion, the remainder of this guideline will refer to circuits, but is intended to apply to the lower level functional blocks also.

If design changes are made, either as a result of the WCA or for other reasons, the WCA is to be updated using the new circuit.

3.3 WORST CASE CONDITIONS

The worst case conditions of any given circuit will be a combination of the extreme values of the following factors:

1. Circuit Interface Inputs and Loads
2. Piece Part Parameter Variations

These factors are described in the following paragraphs.

Because the JPL method uses EVA (Extreme Value Analysis) for both the derivation of part variations and the combinations of circuit part values, it yields very conservative results which represent very improbable conditions. When this process yields unacceptable results, the design/analyst may, with the concurrence of the project management, perform a statistical WCA at some preagreed level such as 3 sigma. These analyses would be accomplished using either RSS'd or Monte Carlo analyses for both (or either) part variations and circuit variations.

The RSS process does not simply RSS every variation. Biases in parameters (such as temperature effects) must remain as biases and algebraically added to those variations which are truly random (i.e. indeterminant in direction and uncorrelated to other variations). The detailed steps for a statistical WCA are described in the notes used in the JPL Professional Development Course No. 1707-1, "Worst Case Circuit Analysis". Section 521 can also lend assistance for any statistical WCA efforts.

3.3.1 Circuit Interface Inputs and Loads

The inputs to the circuit shall be taken to their maximum and minimum voltage and frequency, with the intention of driving the outputs of the circuit to their maxima and minima. The variation of signals presented to the circuit being analyzed are to be those continuous values which are applied at the inputs to the circuit. If the circuit is a control circuit which feeds back, in effect, to its own input (e. g. , a regulator circuit) , it is to be subject to the limits of its control range in the WCA.

Likewise the interface characteristics on the circuit's output side must also be taken to the appropriate maximum or minimum extreme, and its input stimulus must span the limits of its specified variations.

3.3.2 Piece Part Parameter Variation

The total parameter variation depends on variations resulting from a number of causes. The EVA (Extreme Value Analysis) worst case variation for any

one part parameter is the product of the individual parametric variations ,as follows.

$$(1+dP) - (1+dX)(l+dS)(l+dT)(l+dE)(l+dR)$$

where: dP is the total parametric variation
dX is the part initial tolerance
dS is the variation due to aging and drift
dT is the variation due to temperature (worst case direction)
dE is the variation due to applied voltage and frequency
dR is the variation due to radiation degradation

All of the above deltas are normalized as variations from their nominals, that is a ±1% initial tolerance yields a dX of 0.01.

If the selected device is sensitive to mechanical or other factors, such as impact, stress, vibration, vacuum, etc. , that sensitivity must be included in the WCA.

As noted above, the equation yields an EVA solution for part variations. If a project waiver is granted to permit the statistical approach to part variations, the sources of variation must be separated into their biased portions (i.e. predictable in direction) and their random portions (i.e. not predictable in direction). The random contributors can be RSS'd and added to the biases to yield a statistical worst case. More explanation and examples of this method can be found in the course notes from the JPL Professional Development course entitled "Worst Case Analysis".

The above variations are described further in the following paragraphs.

3.3.2.1 Piece Part Initial Tolerance. The tolerances to which a manufacturer has screened the devices shall also be accounted for. There is no additional tolerance to be added to that specified by the manufacturer. Parts whose tolerances are the same cannot be assumed to track in temperature or time in the WCA.

3.3.2.2 Part Aging and Drift (End-of-Life Factors). The aging of electronic parts is a continuing process of chemical change. In most cases, the rate of chemical change is an exponential function of temperature. This temperature dependence provides a means of predicting life expectancy. For the purposes of WCA, life is considered ended when a part parameter drifts outside the circuit allowable limit for that part.

3.3.2.3 Temperature Levels. The upper temperature extreme to which parts are to be analyzed shall be based on a thermal analysis for an 85 °C design shearplate condition which predicts the operating temperature rise between the shearplate and the part. The lower analysis temperature extreme shall be at -30 °C.

3.3.2.4 <u>Applied Voltage and Frequency</u>. The parameter variation resulting from the applied voltage and frequency must be included. For example, the effective capacitance of a capacitor is a function of both the applied voltage and frequency.

3.3.2.5 <u>Effects of Radiation</u>. Most passive components are not subject to degradation at typical space exposures of total dose radiation levels. Semiconductors, however, are susceptible to degradation due to radiation. Treatment of radiation effects for WCA purposes should be accomplished as indicated in JPL TM-33-763. This same document also contains data on older devices (pre 1976). JPL 81-66 has additional data on more recent devices. The most current data is contained in a continually upgraded electronic data base entitled "RADATA" which is accessible through the GP-VAX (818-354-5125).

3.4 VERIFICATION BY TEST

In some cases, (e.g., RF circuitry) the modeling and analysis of a circuit may prove to be extremely difficult and questionable for certain parameters. In these cases, it may be expedient to use laboratory test data in conjunction with analysis to determine the worst case response. For those parts that are difficult to model, the laboratory test is used to establish the sensitivity which can be used in a simplified analysis to achieve all worst case conditions, accounting for each of the six factors mentioned above. This approach will require careful selection of the devices installed in the circuit to achieve the desired shift from nominal part values, either by selection of outlier parts or parts intentionally degraded prior to testing. This sensitivity is used to scale circuit performance for the defined worst case part variation. The remainder of the parts are evaluated by standard WCA analytical methods.

3.5 ANALYSIS

This section provides general guidelines for performing the WCA. More detailed guidelines, for specific circuit types, are provided in Section 5.

3.5.1 Analytic Preparation

In order to expedite the WCA, the parameters which affect the individual component's operation must be delineated prior to any attempt at circuit simulation or evaluation in the WCA. Tables 1 through 8 of this appendix address part parameter variability. The parameter variations include the effects described in paragraph 3.3.2.

3.5.2 Computer Aided Analysis

The WCA can be simplified by doing a computer aided analysis. The availability of WCA tools simplifies the analysis by relieving the analyst of the need to explain his personal methods as part of the WCA and standardizes the analysis methodology so that the majority of time is spent establishing good

assumptions and analyzing the results. The use of computer aided analytic tools is encouraged. The proper application of these tools requires that the analyst understand the device models used by the programs and must use the true worst case approach with the programs. If these tools are used, the analyst must include a description of the circuit models used and a summary of the analyses performed. Summary printouts should be included with the WCA report as an appendix.

3.5.3 Sensitivity Analysis

The worst case maximum or worst case minimum or both are required, depending on the circuit function, and the use of circuit simulation software will simplify the performance of the WCA. The ideal program uses the sensitivity analysis to automatically select the worst case combination of parts parameters. Other programs provide the sensitivity analysis only, so the analyst has to enter the sign and magnitude of the part variations into the network analysis program. The use of a software program which contains sensitivity analysis can prove to be the analysts most important tool. The sensitivity analysis relates a chosen dependent network parameter to any other chosen network parameter. The sensitivity of an output parameter y to another x is the expected change in y per unit change in x. Thus, if the sensitivity of parameter y to parameter x is 0.5, a 4% change in x results in a 2% change in y. This analytical technique is very powerful and highly complex for circuits with more than a few components. Digital computers handle the required matrix manipulations easily.

3.6 RESULTS

After the worst case computations have been completed, the results must be discussed and documented. Any results which show the circuitry operating beyond specified limits are to be noted. The analysis should provide adequate information to permit the necessary programmatic trades of either a modified analysis technique, redesign, or special testing. The analyst should be prepared to appropriately support the resultant actions. A flow diagram of the generation and approval of the WCA is shown in Figure B-1.

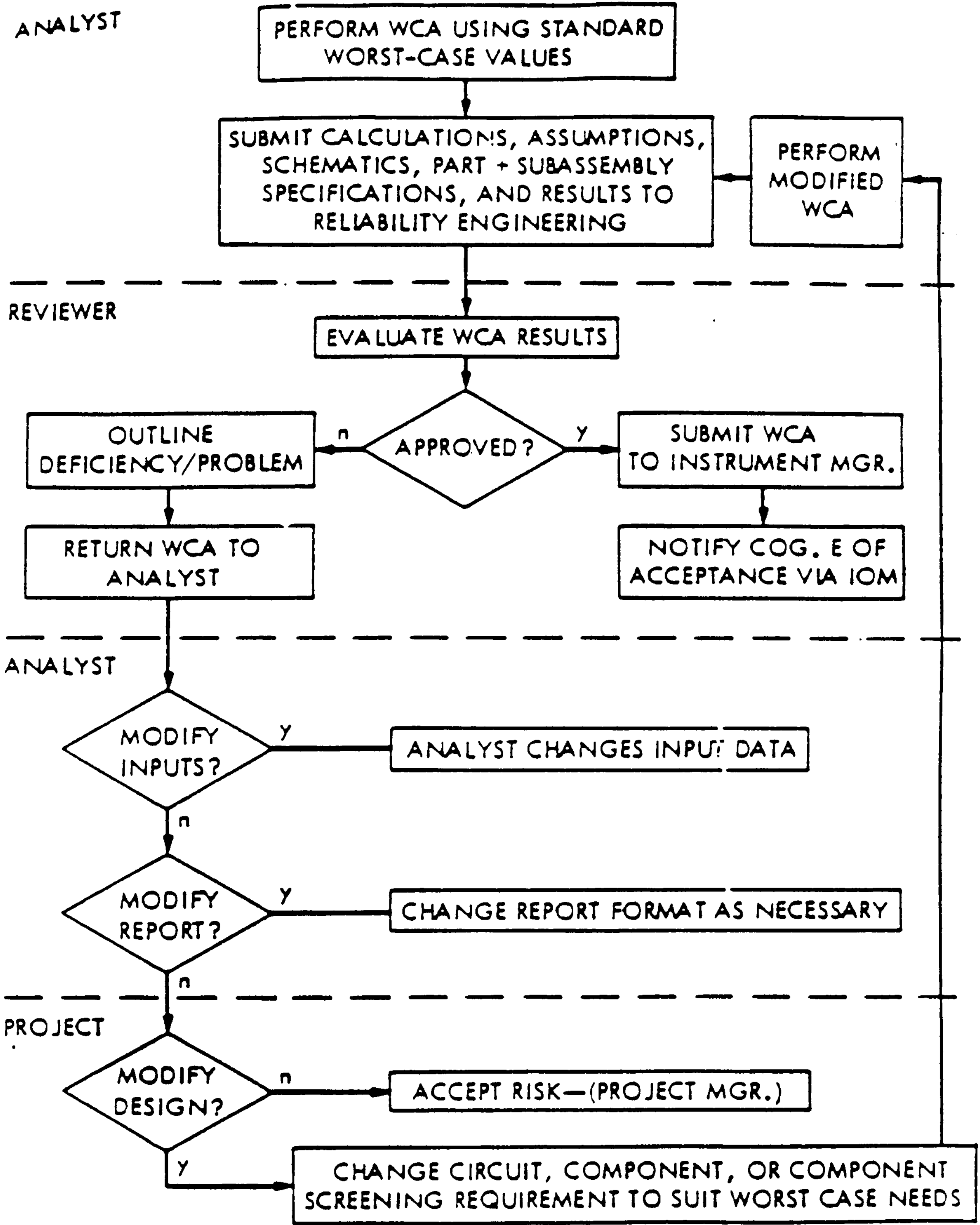


Figure B-1. WCA Flow Diagram

4.0 REPORT FORMAT AND CONTENT

General documentation requirements are discussed in Section II(B). The report should also contain the following specific information.

4.1 TITLE PAGE

The title page shall give the project name and number, the system/subsystem/assembly and circuit names, the analysts name and the date on which the analysis was performed.

4.2 APPLICABLE DOCUMENTS

All documents, which contain requirements to which the circuit is to conform, should be identified. The circuit schematic number and revision code should also be identified. The circuit schematic number and revision code should also be listed. A copy of the schematic should be included with the WCA report.

4.3 CIRCUIT DESCRIPTION

The circuit function should be clearly explained relative to any circuits with which it interfaces. In addition, the theory of operation of the circuit should be discussed in this section in plain language, avoiding numerical values and circuit specific facts as much as possible.

4.4 PERFORMANCE REQUIREMENTS

The specified and derived requirements for the circuit, which form the analysis acceptance criteria, should be listed in matrix form. The matrix should show the parameters on one axis, the source of the requirement on the other axis, and the actual specified value at the intersection of row and column. The source of all acceptance criteria should be referenced to documents listed in Section 4.2 of the report.

4.5 ANALYSIS

The analysis section shall contain the calculations and/or empirical observations that will prove the design satisfactory (i.e. positive margins for all functional requirements for the circuit). The conditions which give true worst case results shall be shown explicitly in this section. It is anticipated that only the most critical attributes of each circuit will be analyzed, but justifications must be given for all requirements not analyzed.

4.5.1 Parametric Variations Tabulation

The parametric variation for each component shall be a sum of the individual parametric variations due to end-of-life, radiation, part tolerance,

temperature, and special piece part factors. Tables B-1 through B-9 contain recommended worst case parameter variation for many component types and radiation test data is available from the references on a number of common devices. The specific minimum and maximum values used in the analysis should be tabulated for each circuit.

When the analyst has knowledge that the physical configuration or operating mode constraints preclude the assumed simultaneous worst cases, he (she) may gain relief by presenting the rationale for the use of his new values. For example, two digital gates in the same chip or two ICs on the same board cannot be simultaneously exposed to opposite temperature extremes.

4.5.2 Functional Blocks

The analysis should proceed through the circuit as a signal would flow from input to output. The contribution of each piece part to the worst case output need not be discussed, but the calculations of cumulative contribution of each stage, subcircuit, or functional block must be shown. The worst case output from preceding blocks shall be used as the input to the next block. Circuits with feedback should be considered as a single block to reduce iteration time, where practicable.

4.5.3 Iterations and Summaries

Ideally, one pass through the circuit under worst case conditions should give the worst case output from the circuit. However, it is required that the circuit/subsystem analysis be recapped with a discussion or tabulation of the worst case outputs from each stage, subcircuit, or functional block. The analysis will determine the output of the stage/subcircuit/functional block and define these to be the inputs to the corresponding next stage/subcircuit/functional block. This will proceed to the actual outputs of the assembly/subsystem. The outputs from the assembly/subsystem must then be compared with the requirements established per Section 3.2 and documented in Section 4.4 of this analysis report.

4.5.4 Software Description

If the analysis has utilized any computer simulation or software, the description of the software should be included in this section and the method of parametric variation discussed unless the program is configuration controlled and available from either commercial, DOD or NASA sources.

4.6 SUMMARY

This final section shall provide a summary of the analysis results and point out any deficiencies which the circuit worst case analysis has revealed. The analysis section will contain all detailed analytical descriptions; the summary section will only serve to outline the results.

If the performance requirements have not been met in any instance, the deficiency must be stated. If the normal analysis assumptions have been perturbed (such as by RSS analysis or modified environments the reported results should note these caveats. Note that any such deviations from the analysis requirements must be approved by the R & QA manager and must be recorded via a waiver to the project. Only one waiver per assembly is required.

5.0 CIRCUIT SPECIFIC ANALYSIS CONTENT

5.1 DIGITAL CIRCUITS WORST CASE ANALYSIS

5.1.1 Interfacing Digital Technologies

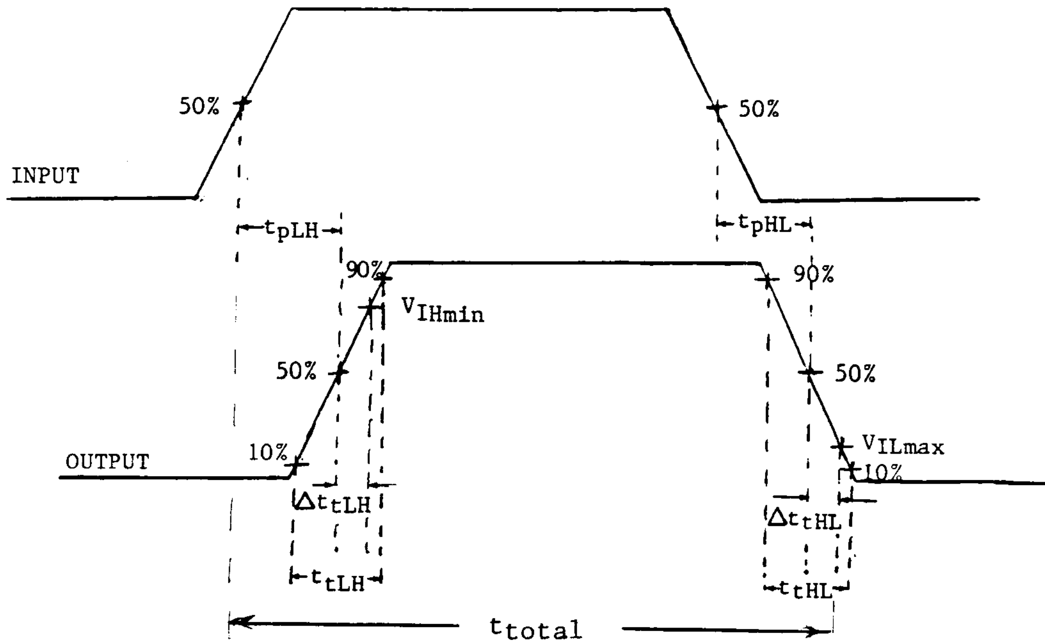
Whenever digital circuitry is not of a single technology type, a study must be made of the interface between the technologies involved. It must be demonstrated that all parts operate properly together under simultaneous worst case source and load conditions. When performing the worst case analysis of differing technology interfaces, it is suggested that particular attention be paid to noise margin at the interface. The defined input and output characteristics of various digital technologies are as shown in Table B-9. The specific devices of the various families, as noted in this table, are used in the timing examples of Section 5.1.2.

5.1.2 Timing

All sequential circuits should have a worst case timing diagram made to determine the effects of variations in switching times of the installed devices. There are many factors which affect timing in digital circuits. These factors include supply voltage, capacitive loading, clock instability, and clock skew.

5.1.2.1 Signal Delays and Response Times. The limits of the propagation delays for the circuit being analyzed must also be shown in the WCA. Response times for the circuit must comply with the required response times identified in the requirements matrix of section 4.4. For circuits which have no specified delay or response times at the unit level, the worst case response times should be explored in further detail at the system level WCA to determine if design constraints should be levied "from the top down".

The total delay of a circuit is the sum of its propagation delay and a transition time effect. This is illustrated below.



t_{total} = worst case circuit delay
= total delay from 50% point on input waveform to V_{IHmin} or V_{ILmax} on output waveform

or $t_{total} = t_p + \Delta t_t$

t_p = specified propagation delay (defined at 50% V_{DD})

t_t = specified transition time, time output slews between 10% V_{DD} and 90% V_{DD}

Δt_t = time output slews between 50% V_{DD} to V_{IH} (or 50% V_{DD} to V_{IL})

$\Delta t_{tLH} = t_{tLH} (V_{IH} - 0.5 V_{DD})/(0.9 V_{DD} - 0.1 V_{DD})$

$\Delta t_{tHL} = t_{tHL} (0.5 V_{DD} - V_{IL})/(0.9 V_{DD} - 0.1 V_{DD})$

@V_{DD} = 5V, VIH = 3.5, and V_{IH} = 1.5V, $\Delta t_{t = 1/4} t^t$ (see note 3).

NOTE: For HCS, THRESH V ≡ 50% point; therefore t_t effect = 0

Propagation delay time (in nanoseconds) takes the form t_p = t(manuf) + t(life) + t(temp) + t(cap. load) which yields the following minimum and maximum delays:

$$t_{p(min)} = \frac{t_{mt}}{2} [1 - 0.1(life)]^* - |T_c (T - 25°)|_{max} \pm C_f(C_S - C_L) \quad \text{NOTE 4,2,5}$$

+ for $C_L > C_s$
- for $C_L < C_s$

and

$$t_p(max) = t_{mm} [1 + 0.1(life)] + |T_c (T - 25°)| + C_f(C_L - C_s) \quad \text{NOTE 4,5}$$

NOTATION:
- t_p = propagation delay time
- t_{mt} = manufacturer's typical delay value
- t_{mm} = manufacturer's maximum delay value
- t_{mn} = manufacturer's minimum delay value
- t_t = transition time
- t_{tm} = manufacturer's transition maximum value
- T_c = temperature correction factor = (ns/°C)
- T = temperature extreme, a program dependent number = worst case design temperature maximum + 10°C rise at the part + 10°C rise at the base plate, or WC design minimum.
- C_s = Capacitance specified by manufacturer's test conditions.
- C_f = Capacitive scaling factor (ns/pf). See Table B-10 below.
- C_L = $V_{total\ load\ capacitance}$ (Input load + trace + cable)
- * ASTTL life effects are ±0.2.

NOTE 1: Although some portion of the Δt (transition time effect on delay) is attributed to temperature, this effect is considered small and therefore captured by the vendor's t_p temperature variation measurement definition (i.e. 50% points).

NOTE 2: Since the physical variations which yield a part with minimum t_p cannot be readily identified, it is conservatively assumed that the minimum tp device still realizes the same delay shift with load capacitance change as does a typical part. Since extrapoilation can yield negative delays, no delay shall be assumed to be less than 1.0 nanoseconds.

NOTE 3: The 1/4 Δt_t factor was derived for the 4000 series CMOS operating at 5V. Alternative values should be derived if other technologies or voltages are being analyzed.

NOTE 4: Since the life effects are expressed as a percentage effect, they are assumed to be a constant percentage of the part's initial value.

NOTE 5: The above equations do not include radiation permanent damage effects. These effects should be based on specific test data, but can be considered negligible below the following levels of total dose.

Standard TTL	75 KRADS	ASTTL	75 KRADS
LSTTL	75 KRADS	4KCMOS	3 KRADS
ALSTTL	75 KRADS	HCMOS	10 KRADS
HCS	200 KRADS		

EXAMPLES

Pulse Delay Times for Various Technologies (All times in Nanoseconds)

1. TTL (SN5400) SOURCE: TI TTL Data Book. Volume 2

   @ $V_{CC} = 5V$

   $t_{pLH}\ (min) = 11/2\ (1-0.1) - \left|0.035(T-25°)\right|_{max} \pm 0.06(C_S - C_L)$
   $t_{pHL}\ (min) = 7/2\ (1-0.1) - \left|0.05(T-25°)\right|_{max} \pm 0.06(C_S - C_L)$
   $t_{pLH}\ (max) = 22\ (1+0.1) + \left|0.035(T-25°)\right|_{max} \pm 0.06(C_L - C_S)$
   $t_{pHL}\ (max) = 15\ (1+0.1) + \left|0.05(T-25°)\right|_{max} \pm 0.06(C_L - C_S)$
   $t_{total}\ (max) = t_p\ (max)*$

2. LSTTL (SN54LS00) SOURCE: TI TTL Data Book

   @ $V_{CC} = 5V$

   $t_{pLH}\ (min) = 9/2\ (1-0.1) - \left|0.0035(T-25°)\right|_{max} \pm 0.08(C_S - C_L)$
   $t_{pHL}\ (min) = 10/2\ (1-0.1) - \left|0.0035(T-25°)\right|_{max} \pm 0.08(C_S - C_L)$
   $t_{pLH}\ (max) = 15\ (1+0.1) + \left|0.0035(T-25°)\right|_{max} \pm 0.08(C_L - C_S)$
   $t_{pHL}\ (max) = 15\ (1+0.1) + \left|0.0035(T-25°)\right|_{max} \pm 0.08(C_L - C_S)$
   $t_{total}\ (max) = t_p\ (max)*$

3. 4KCMOS (CD4011B) SOURCE: RCA CMOS Data Book

   @ $V_{DD} = 5V$

   $t_p = t_{pLH} = t_{pHL}$
   $t_p\ (min) = 125/2\ (1-0.1) - \left|0.002(T-25°)\right|_{max} \pm 1.25(C_S - C_L)$
   $t_p\ (max) = 250\ (1+0.1) + \left|0.002(T-25°)\right|_{max} \pm 1.25(C_L - C_S)$
   $t_t\ (max) = 200\ (1+0.1)\ \Big|_{max} \pm 1.25(C_L - C_S)$
   $t_{total}\ (max) = t_p\ (max) + 1/4\ t_t\ (max)$

4. HCMOS (SN54HC00) SOURCE: TI HCMOS Data Book

   @ $V_{CC} = 4.5V$

   $t_p = t_{pLH} = t_{pHL}$
   $t_p\ (min) = 9/2\ (1-0.1) - \left|0.10(T-25°)\right|_{max} \pm 0.063(C_S - C_L)$
   $t_p\ (max) = 18\ (1+0.1) + \left|0.10(T-25°)\right|_{max} \pm 0.063(C_L - C_S)$
   $t_t\ (max) = 15\ (1+0.1 \pm 0.003(C_L - C_S))$
   $t_{total}\ (max) = t_p\ (max) + 1/4\ t_t\ (max)$

5. ALS (SN54ALS00A) SOURCE: TI ALS/AS Data Book

   @ $V_{CC} = 5V$

   $t_{pLH}\ (min) = 7/2\ (1-0.1) - \left|0.025(T-25°)\right|_{max} \pm 0.046(C_S - C_L)$ for $25° < T < 125°C$
   $t_{pLH}\ (min) = 7/2\ (1-0.1) \pm 0.046(C_S - C_L)$ for $-55° < T < 25°C$
   $t_{pHL}\ (min) = 5/2\ (1-0.1) - \left|0.01(T-25°)\right|_{max} \pm 0.046(C_S - C_L)$
   $t_{pLH}\ (max) = 16\ (1+0.1) + \left|0.025(T-125°)\right|_{max} \pm 0.046(C_L - C_S)$ for $25° < T < 125°C$
   $t_{pLH}\ (max) = 16\ (1+0.1) \pm 0.046(C_L - C_S)]$ for $-55° < T < 25°C$
   $t_{pHL}\ (max) = 13\ (1+0.1) + \left|0.01(T - 25°)\right|_{max} \pm 0.046(C_L - C_S)$
   $t_{total}\ (max) = t_p\ (max)*$

6. AS (SN54AS00) SOURCE: TI ALS/AS Data Book
@ V_{CC} = 5V

t_{pLH} (min) = 7/2 (1-0.2)-$|0.025(T-25°)|_{max} \pm 0.046(C_S - C_L)$ ** for 25°<T<125°C

t_{pLH} (min) = 7/2 (1-0.2) $\pm 0.046(C_S - C_L)$ for -55°<T<25°C

t_{pHL} (min) = 5/2 (1-0.2)-$|0.1(T-25°)|_{max} \pm 0.046(C_S - C_L)$

t_{pLH} (max) = 16 (1+0.2)+$|0.025(T-25°)|_{max} \pm 0.046(C_L - C_S)$ for 25°<T<125°C

t_{pLH} (max) = 16 (1-2.5 + 0.2) + $0.046(C_L - C_S)$ for -55°<T<25°C

t_{pHL} (max) = 13 (1+0.2)+$|0.01(T - 25°)|_{max} \pm 0.046(C_L - C_S)$

t_{total} (max) = t_p (max)*

* Transition times are considered negligible compared to t_p's.
** End of Life and Temperature variations reflect conservative view.

7. HCSMOS (Later)

NOTE: The use of transition times in total CMOS delay computations is necessary only at the input to the device at which propagation race results are measured, and only if the margin is less than 5 nanoseconds.

5.1.2.2 Matched Delay Times. It cannot be assumed that identical manufacturer and lot devices are matched. If the design depends on time critical devices, the devices must be screened for individual matching or restricted parametric values. Identical paths on the same IC chip can be assumed to be matched to within 20% of the same value over their limits of time and temperature.

5.1.2.3 Supply Voltage and Delay Times. Propagation delay is a function of supply voltage. Specifications for a typical IC will call out test conditions or circuit conditions for which the specs are guaranteed. If the application is different from the manufacturers test conditions, compensation for the difference must be made. Manufacturers sometimes include graphs of Vcc vs. delay times, but if this is not available contact Reliability Engineering for further assistance.

5.1.2.4 Setup and Hold Times. The worst case set up and hold times for IC latches and buffers must be investigated and their adequacy determined in relation to other circuit functions. These times must be included in any delay determinations and therefore become a part of the total unit response time result.

Set-Up (t_{su}), Hold (t_h) and Pulse Width (t_w) expressed in nanoseconds can be derated as:

$$t(min) = t_{mn} [1 + 0.1(life)] + |T_c(T - 25°)|_{max}$$

See paragraph 5.1.2.1 for nomenclature.

EXAMPLES OF WORST CASE MINIMUM SET UP, HOLD AND WIDTH CALCULATIONS

1. TTL (SN5473) SOURCE: TI TTL Data Book, Volume 2

   @ V_{CC} = 5V

   t_{su} (min) = t_h (min) = 0

   t_w (min) = $t_{mn}(1+0.1)|0.035\ (T - 25°)|_{max}$

   where t_{mn} = 20 for CLK High

   = 47 for CLK Low

   = 25 for $\overline{CLR}$ Low

2. LSTTL (SN54LS73A) SOURCE: TI TTL Data Book, Volume 2

   @ V_{CC} = 5V

   t_{su} (min) = $20[1 +|0.35(T-25°)|_{max} + 0.1]$

   t_h (min) = 0

   t_w (min) = $t_{mn}(1+0.1)+|0.035(T-25°)|$

   where t_{mn} = 20 for CLK High

   = 25 for $\overline{CLR}$ Low

3. 4KCMOS (CD40138) SOURCE: RCA Data Book

   @ V_{DD} = 5V

   t_{su} (min) = $40(1+0.1)+|0.002(T-25°)|_{max}$

   t_h (min) = t_{su} (min)

   t_w (min) = $140(1+0.1)+|0.002(T-25°)|_{max}$

4. HCMOS (SN54HC74) SOURCE: TI HCMOS Data Book

   @ V_{CC} = 4.5V

   t_{su} (min) = $t_{mn(}[1+0.1)+|0.0035(T-25°)|_{max}$

   where t_{mn} = 30 for DATA

   = 8 for $\overline{PRE}/\overline{CLR}$

   t_h (min) = 0

   t_w (min) = $t_{mn}\ (1+0.1)+|0.0035\ (T-25°)|_{max}$

   where t_{mn} = 30 for $\overline{PRE}/\overline{CLR}$ Low

   = 24 for CLK High/Low

   SOURCE: Ti ALS/AS Data Book

5. ALS (54ALS74A)

   @ V_{CC} = 5V

   t_{su} (min) = $t_{mn}(1+0.1)+|0.025(T-25°)|_{max}$

   where t_{mn} = 16 Data

   = 10 $\overline{PRE}/\overline{CLR}$ Inactive

   t_h (min) = $2[1+|0.025(T-25°)|_{max} + 0.1]$

   t_w (min) = $t_m n(1+0.1)+|0.025(T-25°)|_{max}$

   where t_{mn} = 15 for $\overline{PRE}/\overline{CLR}$ Low

   = 17.5 CLK High/Low

6. AS (SN54AS74) SOURCE: TI ALS/AS Logic Data Book

@ V_{CC} = 5V

t_{su} (min) = $t_{mn}(1+0.2)+|0.025(T-25°)|_{max}$

where t_{mn} = 4.5 for Data

= 2 for $\overline{PRE}/\overline{CLR}$ inactive

t_h (min) = 0

t_w (min) = $t_m(1+0.2)+|.025(T-25°)|_{max}$

where t_{mn} = 4 for $\overline{PRE}/\overline{CLR}$ Low

= 4 for CLK High

= 5.5 for CLK Low

5.1.3 Power Consumption

The power for individual components shall be tabulated in the part stress analysis. The WCA shall contain the total worst case consumption of power, which for digital circuits usually occurs at low temperature. Manufacturers data sheets or appropriate specification sheets usually contain device power consumption graphs. Recall that the WCA is to be performed at -30 to 85°C shearplate temperatures. Power consumption can be affected by radiation total dose and should be considered.

5.1.4 Decoupling

Each printed wiring board containing digital microcircuits should have been analyzed for lead inductances and appropriate decoupling capacitance added to compensate for the board inductance. Adequate capacitance must be provided for protection to assure that the device will not be subject to local power supply fluctuations which might affect its operation. The adequacy shall be tested by showing that the sum of the DC variations, normal supply ripple, and local board induced fluctuations result in instantaneous voltages within the suppliers allowable operating voltages.

5.1.5 Miscellaneous

For devices which contain memory and are part of a state machine, (i.e. counters, registers, etc.) unused states must be defined and provision made for the release from this state without damage or fault generation. The effects of the device entering into one of these unused states must be evaluated and the clearing method outlined.

For one-shot functions, the prevention of false triggering must be included in the WCA. Noise transients should not trigger the one-shot. When the one-shot functions as an interrupt driver, software should be checked for interrupt truth in its service routine to preclude the service of unprepared devices. The one-shot external timing components shall be selected such that the one-shot has a worst case maximum and minimum pulse width which is within +25% of its nominal, and this tolerance shall be used as an input variation to its load circuit.

Table B-10

CAPACITIVE SCALING FACTORS (Cf)

Technology	C_f (ns/pf)	Source
TTL	0.06	FSCM WCA Procedure
LSTTL	0.08	''
LS Bus Driver	0.03	''
STTL	0.04	''
FTTL	0.033	''
ALS	0.046	''
ALS Buffer	0.023	''
HC MOS	0.063	TI HCMOS Data Book
4KCMOS	1.25	RCA CMOS Data Book

5.2 SWITCHING CIRCUITS WORST CASE ANALYSIS

5.2.1 Considerations

Switching circuits, such as those used in switching power supplies servo drivers, and push-pull amplifiers are considered in this category. The critical function of these types of circuits is the positive switching of the desired signal and the lockout of the complementary switch during crossover. Parameters of this type of circuit which should be given attention are the rise and fall times of the switches, transient conditions, switch stress during peak power delivery, and output impedance matching (for efficiency). The WCA shall also consider the power-up and power-down states of the switching circuit to assure that no loss of accuracy or overstress occurs during these intervals.

5.2.2 Solid State Switching

The use of transistor switches to implement signal transfer is common and requires special analyses. In general, solid state switching circuits function as power switches, either in continuous or pulsed mode. The smooth delivery of this power with low distortion is critical to the circuit's proper operation. The following items should be checked by the WCA.

5.2.2.1 Switching Transistors. The operation of transistor switches shall be within the safe operating limits for all worst case loads. The locus of I-V operating points shall fall into the derated, safe operating regions from the device specification.

The average dissipated power in the switching transistors shall be determined from the sum of the operating, quiescent, and transitional power dissipations. Switches not used in the push-pull mode are to be analyzed for their dissipation of power with worst case loads and drive circuitry characteristics.

5.2.2.2 Drive Circuitry. Drive circuits are to be examined for crossover overlap in push-pull configurations. If the possibility of both switches being on at once is found, steps must be taken to control the current through the output stage and bring the overlap under acceptable control. The power dissipated in the case of crossover shall be calculated.

5.2.3 Electromechanical Switching

A WCA or appropriate test data should demonstrate that relay or solenoid drive circuitry precludes the possibility of "hang-up" in a state between set and reset. The WCA should consider the worst case EM device, drive circuit and environmental conditions. The analysis should also verify that coil power is not routed through its own contacts.

It should be verified that the assumed source of power is well regulated and does not suffer voltage droop as a result of the relay event (such as a capacitor bank or an inductive source). Any RC timing circuits used to control applied coil energy should be analyzed. The presence of adequate coil and contact suppression should be verified. A common WCA report section should summarize the analysis results of all included relays and assume that all relays have been analyzed.

5.2.3.1 Drive Circuitry. Drive circuitry for the electromechanical switching circuits is not often subject to crossover. In most cases, relays are used to make one-time, contact to transfer power or control to some assembly or device. The drive circuitry must satisfy all expected worst case conditions such as pickup and dropout voltage and reaction times, over the limits of coil resistance, temperature and any applied mechanical loads. The drive circuits must also supply pulses of sufficient width to insure latching.

5.2.3.2 Contact and Load Considerations. Load considerations for electromechanical switching must further be delineated in terms of the type of load, the amperage to be delivered, suppression (if any) of RFI, contact voltage drop, and load tolerance to contact bounce. The switching of the device shall not degrade the load operation due to transients generated by the switch. It is the responsibility of the switch designer to inform the down-line user and subassembly designers of the expected transients so that they may include these worst case transients in their analyses.

Contact capability is usually specified to guarantee that the contact resistance stays below X ohms at a defined current after a defined number of operations. For purposes of WCA, the designer should assure that the number of intended mission operations is less than the specified. Even if the actual operations are far less than the specified, the maximum defined resistance should be used in the WCA while adhering to the current derating requirements.

5.3 ANALOG CIRCUITS WORST CASE ANALYSIS

5.3.1 Considerations

Analog circuits include functions such as amplifiers, signal generators, line drivers and receivers, integrators, and other signal conditioners. Parameters which are important to these circuits are described below.

5.3.2 Amplifiers

Amplifiers must operate properly under worst case conditions of power supply voltage, load, and peripheral component degradation. Amplifiers shall meet their requirements for gain, stability, distortion, phase-gain margin, linearity, common mode rejection ratio, noise rejection, and offset voltage.

5.3.3 Signal Conditioning

If the circuit does any conditioning of the input signal such as differentiation, integration, or active filtering, the performance of that conditioning must be assured for worst case conditions. The functions depend on the interaction of the circuit with certain critical parts. The worst case extremes of these parts must be included in the WCA. For these types of signal conditioners, the controlled distortion (shaping) of the input signal is the primary function of the circuit. The worst case loading of these signal conditioners can affect that function, so consideration of the load on the circuit is also important.

5.4 RF CIRCUITS WORST CASE ANALYSIS

5.4.1 Considerations

RF circuits shall be analyzed for worst case response under AC, DC, and transient modes of operation. The analysis shall take into account all worst case variations in components due to temperature, voltage and frequency tolerance, aging, manufacturer tolerance, and radiation degradation.

RF circuitry functions in many differing configurations. As such, the guidelines for RF circuitry will be listed rather than explained. The lists give some of the parameters which the WCA should address, although not necessarily the only ones.

5.4.2 RF Amplifier Parameters

- Bias and/or operating point
- Dynamic range (input and output)
- Input/output impedance (magnitude and phase)
- Input/output VSWR
- Gain/phase stability
- Feedback stability margins
- Frequency response (bandwidth, flatness)
- Compression points
- Power Dissipation

5.4.3 Oscillator Parameters
- Frequency stability and accuracy
- Output power level and stability
- Spectral purity
- Phase stability and locking accuracy
- Signal isolation
- Output impedance/load impedance match
- Noise and stray RF control

5.4.4 Comparator Parameters
- Threshold precision
- Switching, speed/time constant
- Hysteresis
- Offset stability

5.4.5 RF Switches
- Power dissipation
- Switching speed
- Power capacity
- Drive requirements
- VSWR
- Insertion loss
- Frequency response
- Video feed through
- Isolation
- Input/output impedance and matching

5.4.6 Mixers
- Noise figure
- Frequency response
- Drive levels
- Compression points
- Intercept points
- Group delay
- Isolation
- Power dissipation
- Spectral purity
- Conversion loss
- Port impedances
- Intermodulation distortion

5.4.7 Filters
- Insertion loss
- Frequency response and bandwidth
- Input and output impedances and matching
- VSWR (input and output)
- Phase linearity

5.4.8 Coupler and Circulator Parameters

- Insertion loss
- Frequency response
- Power capability
- Isolation
- Directivity
- Magnetic leakage
- VSWR
- Input and output impedances

5.4.9 Stripline, Waveguide, and Cavity Parameters

- Mode suppression
- Insertion loss
- Dimensional stability, aging, environmental effects
- Input and output impedances
- VSWR

5.4.10 Modulator Parameters

- Frequency response
- Input and output impedances
- Insertion loss Output spectrum
- Phase response and linearity
- Output level
- VSWR

5.4.11 General Parameters

- Power supply decoupling
- EMC

5.4.12 Multiplier Parameters

- Input and output impedances
- Input drive levels
- Output power
- Isolation
- Frequency response
- Output spectrum

5.4.13 Detector Parameters

- Bias voltage
- Frequency range
- Input and output impedance
- Input VSWR

5.4.14 Power Splitter Parameters

Insertion loss
VSWR
Input and output impedance
Power handling capability
Frequency response

5.5 POWER CONDITIONING CIRCUITS WORSE CASE ANALYSIS

5.5.1 Considerations

Typical electronic circuitry usually requires the conditioning of power from a noisy, poorly regulated source to a load which demands a highly regulated well filtered voltage or current. This conversion can involve any\combination of AC and DC inputs and outputs and generally involves the operations of transformers, switches, regulators and filters. The following sections provide a discussion of possible topics for analysis although it is anticipated that the typical WCA will address only the most critical of these as dictated by the specific application. Because of the complexities and non-linearities inherent in power conditioning, inputs to the part stress analyses are complex and therefor usually performed by the WCA analyst. Computations of the internal workings of magnetic elements are necessary only if they are not procured to a source control specification.

5.5.2 Regulation

Determine the worst case regulation limits under line, load, environmental and life extremes. For switching regulators, consider the effects of ripple on regulation. If output filters are used, the output voltage variation due to load changes should be evaluated.

5.5.3 Efficiency

The power dissipated within the supply should be determined, and the efficiency calculated at minimum load, maximum peak load and maximum steady state load to show compliance with the input power and efficiency requirements.

5.5.4 Transient Response

Power supply transient response should be determined due to line changes, load changes and power on/off operations. The following effects shall be investigated.

(1) Outputs. Determine the maximum/minimum output voltages and response times. In particular, the possibility of output overshoot should be considered.

(2) Stress. Additional stress imposed by transients should be determined. In particular, the start current, voltage, and power transients should be shown to be less than the safe operating limits of the switching transistors.

(3) Magnetic Saturation. Transient conditions should be analyzed for the possibility of unwanted magnetic element saturation.

(4) Inrush. The maximum inrush current and energy at power up should be determined and compared with requirements.

5.5.5 Operating Frequency

The designer shall determine the worst case operating frequency and duty cycle limits for line, load, temperature, end of life extremes, and radiation effects. Internal oscillators shall be analyzed for frequency stability. Freedom from mode shift to sub or multiple harmonics should be demonstrated.

5.5.6 Starting

It shall be verified that the switching power supply can start under all worst case conditions. Normally cold temperature maximum DC load, and maximum capacitance represent worst case conditions.

5.5.7 Switching

The switching transistors shall be analyzed in detail in order to demonstrate that switching is performed in a predictable and consistent manner under all worst case conditions, and that the drive to the switching elements is adequate.

The drive circuit analysis should show that both switches in a two switch drive stage cannot be on simultaneously, or that current limiting is provided during intentional simultaneous conduction. The impact of transistor crossover and of crossover protection circuits on switching and on regulation should be investigated and the additional power dissipation due to crossover calculated.

5.5.8 Inductor and Transformer Considerations

Magnetic drive stages shall be shown to have adequate suppression under worst case voltage and duty cycle conditions.

Transformer applications shall be analyzed for the possibility of DC unbalance. The primary open circuit voltage and the secondary unbalance current shall be determined, and the resulting stress on the switching transistor due to the unbalance shall be assessed. Transformer DC unbalance is a common problem in DC/DC converters, particularly those having an independent drive transformer.

The possibility of zero current inductor (dry choke) operation in switching regulators should be investigated. If a zero current condition can exist, the effect on output ripple voltage, capacitor ripple current, output regulation, frequency and stress must be investigated. Control loop stability must also be investigated for modes of operation which include zero current in the output inductor current.

The possibility of the output transformer magnetizing current being greater than the load current should be investigated.

5.5.9 Filtering and Stability Considerations

In general, special precautions must be taken to prevent peak detecting of outputs under light load. Peak detecting is caused from output transformers having excessive leakage and inductance in the secondary/primary windings or discontinuous inductor current.

Power supply phase and gain margin shall be determined by an open loop frequency response analysis. The allowable worst case phase margin shall be assumed as 30 degrees and the allowable worst case gain margin assumed as 10 dB, unless specified otherwise.

The possibility of power supply instability caused by an input filter loaded by the negative impedance presented by a switching regulator input should be investigated.

The possibility of polarized filter capacitors becoming reverse biased at power down shall be prevented. If reverse bias occurs, the consequences shall be determined by considering the type of capacitor, the magnitude of the reverse bias voltage and the level of the breakdown current flow.

Capacitor ripple currents shall be determined. Ripple currents in the input and output filter capacitors are especially critical. The ripple current shall not exceed the derating requirements.

The effect of voltage transients during switching intervals should be determined. Suppression of inductors subject to being open circuited should be analyzed to verify the limiting of transient voltages to acceptable levels, as dictated by part stress derating criteria.

5.5.10 Second Breakdown

All power transistors, switching or linear, should be analyzed for forward-bias and reverse-bias second breakdown and compared to the safe operating area requirements for the maximum junction temperature.

5.5.11 Protection Circuits and Their Trimming

The worst case overvoltage, undervoltage, and overcurrent set point ranges should be verified relative to the power supply and load circuit requirements. The overcurrent results should be reported as a part of the power system analysis.

The trimming procedure should be analyzed in detail. Output voltage, overcurrent set point, overvoltage set point and undervoltage set point trim procedures should be considered. Input voltage, environments, loads on all outputs and the trim tolerances (e.g., EOL and setting resolution) should be included. The resistor range and increments shall be verified to provide the desired trim tolerance.

5.5.12 Magnetics WCA

For magnetic devices not purchased to a source control spec, the analyst should determine the minimum and maximum inductance as a function of temperature, initial tolerance, DC magnetic field intensity (oersteds) and peak flux density (gauss). In some instances, as in tape wound cores, the inductance has little meaning. In such cases, magnetizing current should be measured under anticipated operating conditions.

Show that the worst case transformer core maximum flux density (Bm) is not exceeded. Temperature, minimum frequency and maximum voltage must be considered. An example of a transformer requiring this analysis is a DC/DC converter output transformer. Special attention must be given to the temperature dependence of Bm when using ferrite cores.

Determine the circular mil per ampere actuals (CM/AMP) for all inductor and transformer windings. The allowable current density in copper is 500 CM/AMP. In some instances, this can be exceeded in which case a thermal analysis should be performed on the magnetic device.

Winding resistance should be measured or calculated. The resistance should be adjusted for temperature by the copper resistivity temperature coefficient.

6.0 PART PARAMETER VARIATIONS

A W. C. A. requires knowledge of the total part variations over the life and environmental extremes of the particular project. Life effects include both powered (aging) and unpowered (drift) effects. The following tables give the recommended variations to be used for a program with an anticipated unpowered life of three years at room ambients from the time of part purchase to flight, and an assumed powered life of three years for test and flight at an assumed 95'C part temperature and with semiconductor junctions of 110'C. (Note: For programs where the times and temperatures vary from these values, parameter variations may require adjustment.)

The total variations listed are for part ambients from -35 to +95 °C when combined with life, mechanical stress and electrical stress effects. They do not include radiation effects which will be additive. Single event upsets (SEU) analysis will be treated in a separate analysis.

Any deviations from the tabulated variations should be substantiated by modified environment or specific device test data or modified analytical techniques (RSS, Monte Carlo, etc.). For parts not listed here, the analyst may either derive his own values or confer with JPL Reliability for assistance.

As an aid to the circuit designer's worst-case analyses, the maximum expected parameter variations for system life and temperature are given. It is noted that all parameter changes are based on the specific value given in the application of the JPL part standard or manufacturer specifications, except for hFE. For this parameter, the variation is from the design value as established by appropriate design curves at 25 °C and the design value of IC. For the case of saturated switches, the parameter changes of hFE will be established from the minimum value specified in the manufacturer specifications, or ST. The data in Table B-1 applies to all bipolar transistors listed in the JPL Preferred Parts List, ZPP-2061-PPL.

Table B-1. Worst-Case Parameter Variations for Transistors

Parameter	Variations	Conditions	Remarks
hFE (Note 1)	+0.9%/°C *	For temperature	Change from design value mfr. spec.
	-10%	For life	Not additive to rad effects.
VCE(SAT) (Note 2)	+15%	For life	Change from max. value in mfr. spec.
	+0.2mV/°C	For temperature	
VBE(SAT)	+15%	For life and temperature	Change from max. value in mfr. spec.

* Manufacturer's data may be used when available.

NOTE 1: $h_{FE\ max}$ @ 25°C = 2.5 x $H_{FE\ nom}$ @ 25°C unless specfied otherwise by the vendor.

NOTE 2: VCE(SAT),min shall be assumed equal to zero.

Table B-1. Worst-Case Parameter Variations for Transistors (cont.)

Parameter	Variations	Conditions	Remarks
ICBO	doubles every 10°C increase	For temperature	Change from max. value in mfr. spec. at 25°C.
	+50%	For life	Not additive to rad effects.
IEBO	doubles every 10°C	For temperature	Change from max. value in mfr. spec at 25°C.
	+50%	For life	Added to temperature effects - not additive to rad effects.
ICES	3OX	For life and temperature	Change from max. value in mfr. spec.
tr (1)	+10%	For life and temperature	Change from max. value in mfr. spec.
td (1)	+10%	For life and temperature	Change from max. value in mfr. spec.
ts (1)	+10%	For life and temperature	Change from max. value in mfr. spec.
tf (1)	+10%	For life and temperature	Change from max. value in mfr. spec.
Cobo (1)	+5%	For life and temperature	Change from max. value in mfr. spec.
Cibo (1)	+5%	For life and temperature	Change from max. value in mfr. spec.
fT (1)	-5%	For life and temperature	Change from min. value in mfr. spec.

NOTE (1): Minimum values shall be assumed equal to 50% of nominal or 33% of maximum if not specified.

Table B-2. Worst-Case Parameter Variations for Resistors

Part description: General, class, type	Manufacturer	Manufacturer's type number	Tolerance, % Purchase	Design[a,b]
Carbon comp.	ABC	RCRO5,7,20	+5	+20
Precision WW	SHA	HR series RBR series	+0.1	+0.4
Metal film	MEP	RNC55H	+1	+2
Metal film	MEP	RNC50H	+1	+2

[a]Design tolerance includes purchase, temperature, and end-of-life tolerances except where noted.

[b]Design tolerance does not include voltage coefficient effects for which the JPL ST or mfg. spec. should be consulted.

Table B-3. Worst-Case Parameter Variations for Fixed Capacitors

Part description: General, class, type	Manufacturer	Manufacturer's type number	Tolerance Purchase	Tolerance Design[a]
Solid tantalum	SPR	CSR13-KS	±5%	±15
Solid tantalum	SPR	CSR13-KS	±10%	±20
Ceramic	AUX	CKR05BX-KS	±10	±33
Ceramic	AUX	CKR05BX-KJ	±10	±25
Ceramic	AUX	CKR11BX-KR	±10	±25
Ceramic	AUX	CKR12BX-KR	±10	±25
Ceramic	AUX	CKR14BR-KR	±10	±30
Ceramic	AUX	CKR15BR-KR	±10	±30
Ceramic temp. comp.	AUX	ML10 MC70 ML11 MC90	±5	±6
Ceramic, HV disc.	ERIE	800 series	±10	±17
Class	CGW	CYFR series	±1	±2.1
Porcelain	VIT	VY series	±10	±11

[a]Design tolerance includes purchase, temperature, and end-of-life tolerances except where noted.

Table B-4. Worst-Case Parameter Variations for Diodes

DIODES

Parameter	Variations	Conditions	Remarks
VF	+1%	For life	Change from initial value.
	+150 mv	For temperature	
c	+25%	For life and temperature	Change from value in mfr. spec.
tr	+10%	For life and temperature	Change from value in mfr. spec.
IR	5X	For life	Change from value in mfr. spec.
	2X For every l0°C	For temperature	Change from value in mfr. spec.

Table B-5. Zener Diodes

Parameter	Variations	Conditions	Remarks
VZT	±2%	For life	Added to tolerance in mfr. spec.
ZZT	+10%	For life and temperature	Change from value in mfr. spec.
TC	+10%	For life and temperature	Change from value in mfr. spec.
IR (Below knee)	3OX	For temperature	Change from value in mfr. spec.
	lox	For life	
VF	+10%	For life and temperature	Change from value in mfr. spec.

Table B-6. Worst-Case Parameter Variations for Zener Reference Diodes

Voltage referenced diodes

Parameter	Variations	Conditions	Remarks
VZT	±0.25%	For life	Change to tolerance in mfr. spec.
IR (Below knee)	3OX	For temperature	Change from value in mfr. spec.
	10X	For life	
ZZT	+10%	For life and temperature	Change from value in mfr. spec.
Temp. Coef.	+10%	For life	Added to mfr. temperature coefficient

Note: Consult with part specialist on life stability factors.

Table B-7. Worst-case Parameter Variations for Bipolar Integrated Circuits

DIGITAL IC's (TTL AND LOW POWER TTL)

Parameter	Variations	Conditions
IIN(L)	+75%	Life and temperature
IIN(O)	+20	
IOUT(L)	-20	(Source capability decreases for same VOUT spec)
IOUT(O)	-20	(Sink capability decrease for same VOUT spec)
IOS	+25	
TPDH	Table B9	
TPDL	Table B9	
Icc	+25	
Clock pulse width (input)		

LINEAR IC'S

Parameter	Variations	Conditions
AV	-40	Life and temperature
VOS	+20	
IIN	+30	
EO	-10	
IBIAS	+10	
VOS/T	+40	
IOS	+10	
Icc	+10	
IEE	+10	

Table B-8. Worst-case Parameter Variations for CMOS Integrated Circuits

Parameter	Variations,% (life)	Variations,%/C° (temperature)	Remarks
IOUT(l), (0)	-10	-0.5	Source capability decreases for same VOUT spec
ISS	+50	+10	Quiescent Current
TPLH	See Section 5.1.2.1		
TPHL	See Section 5.1.2.1		

TABLE B-9

ELECTRICAL CHARACTERISTICS

	Source	V_{CC}	V_{OH}	V_{IH}	V_{OL}	V_{IL}	I_{OH}	I_{IH}	I_{OL}	I_{IL}
TTL (SN5400) R_L-DOMINATED	1	@5V	2.4V	2.0V	0.4V	0.8V	-0.4mA	40uA	16mA	-1.6mA
LSTTL (SN54LS20) R_L-DOMINATED	1	@5V	2.5V	2.0V	0.4V	0.7V	-0.4m	20uA	4mA	-0.4mA
HCMOS (SN54HC00) C_L-DOMINATED	3	@4.5V	4.4V 3.7V	3.15V	0.1V 0.4V	0.9V	20uA -4mA	1000nA	20uA 4mA	-1000nA
4KCMOS (CD4011B) C_L-DOMINATED	2	@5V	4.95V	3.5V	0.05V	1.5V	-1.0mA	1000nA	0.9mA	-1000nA
HCT (SN54HCT189) C_L-DOMINATED	3 5	@4.5V	4.4V 3.7V	2.0V	0.1V 0.4V	0.8V	20uA -4mA	1000nA	20uA 4mA	-1000nA
AS (SN54AS00) R_L-DOMINATED	4	@5V	3.0V	2.0V	0.5V	0.8V	-2mA	20uA	20mA	-0.5mA
ALS (SN54ALS00A) R_L-DOMINATED	4	@5V	3.0V	2.0V	0.4V	0.7V	-0.4m	20uA	4mA	-0.1mA
HCS (LATER)										

ALL DATA @ 25#C

COMPATIBILITY REQ'T

$V_{OH} > V_{IH}$
$V_{OL} < V_{IL}$
$I_{OH} > I_{IH}$ (sum of all loads)
$I_{OL} > I_{IL}$ (sum of all loads

SOURCES:

1. TI TTL Data Book, Volume 2
2. RCA CMOS Data Book
3. TI HCMOS Data Book
4. TI ALS/AS Data Book
5. RCA QCMOS Data Book

APPENDIX C

ELECTRONIC/ELECTROMECHANICAL/ELECTRICAL PARTS STRESS ANALYSIS GUIDELINES

This Appendix is a guideline that identifies parts applications limitations and the data to be developed in performing a parts stress analysis. The electronic/electromechanical/electrical parts application analysis shall be performed to verify that the applied stresses on the components at qualification test temperature levels do not exceed the parts stress derating guidelines identified herein. In the analysis, it shall be assumed that the unit/assembly baseplate is set at the high qualification temperature limit; the piece part operating temperature should then be determined by thermal analysis.

The stress analysis report shall contain all schematics and other applicable drawings with number and revision letter, as applicable to the analysis. Documentation requirements are discussed in Section II(B).

The detailed JPL stress sheets and entry explanations are included as part of Appendix C. These sheets or their equivalent should be provided in any stress analysis submission.

APPLICATION DATA: CAPACITORS & FILTERS

Capacitor and filter deratings shall comply with Sections 1.2.1 and 1.2.7 of MIL-STD-975G unless noted otherwise.

The ac rating of a capacitor is influenced by capacitance, dissipation factor, mass, geometric configurations, and the ambient operating temperature. The following basic rules should be considered for ac applications:

(a) The capacitor should be packaged to maximize the heat dissipation capability of the device.

(b) Current limiting should be applied to the extent that it does not deteriorate the required circuit performance.

(c) Do not apply peak ac voltages that exceed the recommended dc rating of the capacitor.

(d) Determine whether the capacitor is corona-free where the applied voltage exceeds 250 V.

(e) Manufacturer's ac ratings should be derated by a factor of 0.7.

Exceptional Application Requirements. For charge/discharge, energy storage applications, the following additional information is required:

(a) Pulse width

(b) Repetition rate

(c) Rise time

(d) Maximum charge/discharge current

APPLICATION DATA: Diodes and Transistors

Diode and transistor deratings shall conform with Section 1.2.4 of MILSTD-975G unless noted otherwise. Junctions shall be limited to 110 °C.

Exceptional Application Requirements. The following temperature-compensated zener reference diodes have minimum temperature rating of 0 °C rather than -55°C.

IN935 through IN946
FCT 1021, 22, 25
IN2620 through IN2624

APPLICATION DATA REQUIREMENTS: Fuses

Fuse derating requirements shall meet Table 1.2.9 of MIL-STD-975 as amended herein to account for temperature and vacuum conditions.

The DC derating factors for fuses must be varied per fuse size according to the following table.

Fuse Current Rating (amperes) @ 25°C	Fuse 1/ Current Rating (amperes) @ 95°C	Derating 2/ Factor for Vacuum and Reliability on PC Board	Max Allowable DC Operating Current in Vacuum @ 95°C
15	13.2	0.5	6.6
10	8.8	0.5	4.4
5	4.4	0.5	2.2
2	1.76	0.5	0.88
1	0.88	0.45	0.40
1/2	0.44	0.4	0.18
3/8	0.33	0.35	0.12
1/4	0.22	0.30	0.066
1/8	0.11	0.25	0.027

1/ Based on 0.2%/C° per ZPP-2061-PPL for med and fast bio fuses.

2/ Derating factors are based on data from fuses mounted on printed circuit boards in vacuum and conformally coated. For other type mountings or pulsed waveforms, consult the project parts engineer for recommendations.

APPLICATION DATA: Inductors and Transformers

Transformers and inductors shall meet the derating requirements of Sections 1.2.5 and 1.2.6 of MIL-STD-975G.

(1) Current density shall be less than 1 ampere per 500 circular mils.

(2) Temperature hot spots shall be determined based on the manufacturer's computed, measured or guaranteed max temperature rise from the part mounting surface to its hot spot. Typical good designs will limit the rise to 20 °C.

APPLICATION DATA: Integrated circuits

CMOS and TTL, Digital.

Maximum Stress Guidelines.

(1) Supply Voltage

(a) TTL

(i) Continuous supply voltage shall not exceed the manufacturer's recommended operating supply voltage.
(ii) Transient supply voltage shall not exceed the manufacturer's absolute maximum supply voltage.

(b) CMOS. The continuous and transient supply voltages shall not exceed 70 percent of the V_{DD}-V_{SS} voltage used in screening the CMOS parts (only applicable if subjected to special screening tests).

(2) Power Dissipation. The power dissipation per logic element and per package shall be limited so the semi-conductor junction/ channel temperatures do not exceed 110 °C. For CMOS, the power dissipation is also a function of operating frequency.

(3) Input Voltage

(a) CMOS. The input voltage shall not exceed 70 percent of the V_{DD}-V_{SS} voltage used in screening the CMOS parts.
(b) TTL. The instantaneous input voltage shall not exceed the manufacturer's absolute maximum ratings.

(4) Output Voltage. Open collector output voltage shall not exceed 80 percent of the manufacturer's recommended output voltage.

(5) Output Current

(a) Driving other logic elements, the output current shall not exceed 80 percent of the manufacturer's rating.

(b) Driving elements which not parts of logic families, the output current shall not exceed 50 percent of the manufacturer's ratings.

(6) Input Current

(a) TTL input current at terminated, unused inputs shall be 100 microamperes or less.

(b) CMOS input current shall be externally limited to 10 milliamperes or less if driven when V_{DD}-V_{SS} is zero. The parts can be damaged if this is not done.

(c) Unused inputs of CMOS devices should be pulled to either V_{DD} or V_{SS}, whichever is appropriate for the logic circuit involved, and may be directly connected without current limiting provided that its own supply is used for the pull-up.

LINEAR INTEGRATED CIRCUITS

Maximum Stress Guidelines. The factors listed in Table C-3 shall be applied to the device manufacturer's published maximum ratings except where the device is screened for a higher rating. In the latter case, the derating factors shall be applied to the screened parameters. For circuit types not specifically listed in Table C-3, a general derating factor of 80 percent is recommended for output currents, applied voltages, and power dissipation.

APPLICATION DATA REQUIREMENTS: Relays

Relays shall meet the derating requirements of Section 1.2.11 of MILSTD-975G.

(1) Predominant dc switching functions.

(a) Coil. Characteristics of coil drive current and/or voltage shall be noted; e.g., in a pulse operated mode the current wave form should be supplied or in an unregulated drive voltage mode the voltage range should be defined. General limits are manufacturer's rated normal values.

(b) Contacts. For reliability, the contacts should be derated per MIL-STD-975 using the factors which account for temperature, load application and cycle rate. Additional information relating to drive and

load conditions is discussed separately in the JPL Preferred Parts List (ZPP-2061-PPL).

Special Requirements

The relay electronic drive circuitry must be designed so that under no circumstances the following conditions could arise:

(a) Relay hangs up in midpoint and opens the coil drive circuitry.

(b) Relay cannot be reset.

In general, this requirement will restrict the use of interconnecting relay contacts for coil drive purposes and also restrict the use of timing circuits when proper circuit operation requires relay reaction times for proper switching.

APPLICATION DATA: Resistors

Resistors shall meet the derating requirements of Section 1.2.3 of MILSTD-975G.

Exceptional Application Requirements.

(1) Power stress. Resistors generate heat, and one critical area of analysis is to determine how that heat is dissipated. Anything which lowers the element temperature of the resistor, decreases the stress on the part. For example, an Allen Bradley resistor operating at 150% rated power at O°C ambient is stressed less than the same part operating at 50% power and 70°C ambient. Generally, 50% derating is recommended. Carbon composition and film resistors can safely be operated at 70% if the ambient temperature is 50 °C or less. Power resistors should never be operated at greater than 50% average power, and the chassis mount parts may have to be even further derated, depending on the available heat sink.

(2) Pulse power. Individual cases have to be evaluated. Conservatively, for all resistors, no problems can be expected at 100 times rated power if the single pulse power, when averaged over the thermal time constant period, is less than the rated DC power. A safe minimum value for thermal time constant is 1 sec. Some resistors have thermal time constants up to 1 min for the larger devices.

Table C-1. DC Voltage Derating Factors

Type of Capacitor	Derating Factor*
Ceramic Disc	
Less than 1000 Vdc	0.6
1000 Vdc or greater	0.5
Glass	0.5
Porcelain	0.7
Mica	
Less than 1000 Vdc	0.7
1000 Vdc or greater	0.5
Plastic Film	0.6
Paper	0.8
Metallized Film**	0.6
Tantalum, Solid	0.5
Tantalum, Wet Slug	0.6
Tantalum, Foil	0.5

*Derating factor = actual stress/manufacturer's rated stress

**The metallized dielectric has a self-healing characteristic. Since the self-healing phenomenon is dependent on energy surges to clear the defect, use of this device should be avoided where high impedance and low voltage are circuit factors, as well as those circuits whose performance would be degraded by the presence of occasional transients.

Table C-2. DIGITAL MICROCIRCUITS

Item	Parameters		TTL	LP TTL	NMOS CMOS	Line Drivers and Receivers	
1	Supply voltage	1/	5.5V max	5.5V max	0.70 2/	1.00	3/
2a 2b	Power dissipation (percent of rated power at maximum operating temperature)		0.80 4/	0.80 4/	0.80	0.80	
3	Devices shall be operated at <80% of maximum frequency						
4	Differential dc input voltage	1/	N/A	N/A	N/A	1.00	3/
4	Single-ended dc input voltage	1/	1.00	1.00 3/ 5/	0.70 2/	1.00	3/
5	Operating ac or dc output current		0.80 2/	0.80 2/	0.80 2/	0.80	
6	Open collector (or drain) dc output voltage		0.80	0.80	N/A	0.75	
7	All unused inputs shall be tied either Vcc or ground through vendor recommended resistances						
8	Maximum input current available to unpowered CMOS devices shall be 10 ma.						

1/ Under no circumstances shall the input voltage be allowed to exceed the supply voltage unless specifically permitted by spec or lot test verification.

2/ Further derating may be required for radiation environments (i.e. minimum Vcc to insure minimum dc reference for transients).

3/ Use 1.00 when used with digital logic families and 0.75 when used with analog logic families.

4/ Power dissipation shall be limited to meet 110° T_J criteria.

5/ Transient input currents caused by the below-zero portion of ringing waveforms shall be limited to 2 mA. This condition may occur where LPTTL is driven by standard TTL.

Table C-3. Application Data Required

Required Data	54	TTL 54L	54LS	CMOS B-series
1. Supply voltages, maximum and minimum values	X	X	X	X
2. Maximum power dissipation				
a. per logic output	X	X	X	X
b. per package	X	X	X	X
3. Operating frequency maximum				X
4. Input voltage, maximum and minimum	X	X	X	X
5. Output current, maximum or fanout for each logic output	X	X	X	X
6. Open collector (or drain) DC output voltage	X	X	X	X
7. Termination of unused inputs	X	X	X	X
8. Maximum input current if $V_{DD}-V_{SS} = 0$				X

Table C-4. Application Data Required, Linear ICs and Analog Switches

Type of Data Required	Diff'l Amp.	Com-para-tors	Sense Ampl.	Cur-rent Ampl.	V Reg.	Analog Switch
1. All supply voltages, their regulation (in % or magnitude) and the duration and magnitude of max. expected transients	X	X	X	X		X
2. Device power dissipation, including that caused by maximum loads	X	X	X	X	X	X
3. Peak (or p. top.) ac input	X	X	X	X		
4. Differential dc input	X	X	X			
5. Single-ended dc input voltage				X	X	
6. Maximum signal voltage						X
7. Input-Output voltage differential					X	
8. Output ac voltage, Specify inductive loads	X			X		
9. Open collector dc output voltage		X	X			
10. Maximum output current ac or dc	X	X	X	X	X	X
11. Method of output short-circuit protection	X	X	X	X	X	

Table C-5. Derating Factors in % of Published or Screen Maximum Values, Linear ICs and Analog Switches

Type of Data Required	Diff'l Amp.	Com-para-tors	Sense Ampl.	Cur-rent Ampl.	V Reg.	Analog Switch
1. Supply Voltages	80	90	80	80	--	90
2. Power dissipation (percent)	75	75	75	75	80	80
3. ac input voltage (percent of rated ac voltage at actual supply voltage)	100	100	100	100		
4. Differential dc input voltage	30 (1)	30 (1)	70			
5. Single-ended dc input voltage	-	-	-	80	90	-
6. Signal voltage referenced to negative supply voltage						80
7. Input-Output voltage					80	
8. Output ac voltage	100			100		
9. Open collector dc output voltage		90	90	-	-	-
10. Operating ac or dc output current	80	80	80	80	80 (2)	80
11. Maximum short-circuit output current set by external means	90	90	90	90	90	-

NOTES: (1) Should not exceed the BV_{EBO} of the transistors in the input circuit.

(2) 50% of rated current for two terminal regulators. Derating = actual stress/manufacturer's rated stress.

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PART USAGE AND APPLIED STRESS DATA
CAPACITORS – FIXED AND VARIABLE

SUBSYSTEM NAME AND REFERENCE NO.	SCHEMATIC TITLE NO. REV.	NEXT ASSY. TITLE
	ASSY. TITLE NO. REFERENCE NO.	NO. REV. REFERENCE NO.

CKT. SYM. NO.	CONSTRUCTION		JPL PART NO., VENDOR OR MIL TYPE NUMBER	VENDOR	PART AMB. TEMP °C MAX/MIN	CAP VALUE PF	MFG. TOL. %	VOLTAGE										STRESS RATIO		WAVE FORM (DC, SINE PULSE, ETC.)	REMARKS (CORONA FREE, CHARGE/ DISCHARGE CURRENT *, ETC.)	APPLICATION RATING	
	DIELECTRIC	TYPE CASE						RATED 25°C NOM.		RATED MAX AMB.		OPERATING											
												(3)	AC			PULSE							
								DC	RMS	(1) DC	(2) RMS	DC	PEAK	(4) RMS	FREQ	PEAK	REP RATE	(3)/(1)	(4)/(2)			A	U

REPORT NO. AND REVISION DATE	ANALYST NAME DATE	COG. ENG. APPROVED DATE
JPL SECTION NO. APPROVED DATE	JPL RELIABILITY APPROVED DATE	SHEET OF

*FOR ENERGY STORAGE APPLICATIONS ONLY

JPL 2291 R 7/75

D-5703

CAPACITORS, FIXED AND VARIABLE (JPL Form 2291 Rev. 1/75)

- Circuit Symbol Number

This number should be recognizable from the schematic diagram supplied with the stress analysis.

- Construction

1. Dielectric The type dielectric used should be put in t his column (i.e. Tantalum, Ceramic, Ta wet slug, etc.).

2. Type case The case type, such as axial lead, disc, chip, etc., goes here.

- JPL part number; vendor or MIL type number

This entry should be enough to specify completely the type of part being used. JPL part number is preferred, vendor and MIL type numbers and vendors numbers are second and third choices, respectively.

- Vendor

The vendor is specified in this column. Use the vendor designations from the JPL ZPP-2061-PPL. If the vendor is not listed, write in vendor name.

- Part ambient temperature

Used for derating purposes; the expected part temperature during qualification testing is to be put in this column.

- Capacitance value (pF)

The capacitance value of the part is given here in picofarads (pF). If capacitance is in units other than pF, such as uF or nF, please specify.

- Manufactured tolerance

The manufacturer's initial purchase tolerance goes in this column.

- Voltage

1. Rated 25°C nominal
   a. DC
      This should be in the DC voltage r ating of the capacitor at 25 °C.

   b. RMS
      This should be the RMS voltage rating of the capacitor at 25 °C (only required for AC applications).

2. Rated maximum ambient
   a. DC
      This should be the DC voltage rating of the capacitor at the maximum ambient temperature expected during qualification testing.
   b. RMS
      This should be the RMS voltage rating of the capacitor at the maximum ambient temperature expected during qualification testing.

3. Operating
   a. DC
      This entry should specify the DC operating voltage of the capacitor. If the waveform seen by the capacitor is a DC-shifted periodic type, note the maximum DC value here.

   b. AC
      i) The peak AC operating voltage belongs in this column. For peak AC voltages superposed on DC shifts, include ONLY the AC component; DC shift stresses are handled in Section 3a above.

      ii) RMS
         The RMS operating voltage belongs in this column. Again, RMS values do not include DC shifts handled in Section 3a above.

      iii) Frequency
         The maximum operating frequency of the capacitor is entered in this column.

   c. Pulse
      i) Peak
         The peak pulse voltage to which the capacitor may be subjected is entered in this column. Turn-on transients are included in this category, as well as the sum of DC plus AC peak voltages.

      ii) Repetition rate
         For repeated pulsed voltages, the repetition rate is entered in this column. If a capacitor is subject to repeated pulse trains (as is seen in Radar PRF), note the pulse repetition frequency and its duty cycle.

- Stress Ratio

1. The stress ratio entered in the first stress ratio column is the DC stress ratio. That is, the DC stress ratio is the operating DC voltage from Section 3a above divided by the maximum rated DC voltage at ambient temperature from 2a above.

2. The stress ratio entered in the second stress ratio column is the RMS or AC stress ratio. The RMS stress ratio is the RMS operating voltage from section 3b(ii) above divided by the maximum rated RMS voltage at ambient temperature from Section 2b above.

- Waveform

If known, the waveform seen by the part should be entered here.

- Remarks

The resistance in series with solid tantalum capacitors should be noted. If the series resistance is less than 1 ohm per volt applied, the current capability of the power source should be noted, and if it exceeds 1 ampere, the part should be considered over stressed unless the part is screened for inrush current capability (i.e. CSS is screened but CSR is not unless procured with extra screening tests).

PART USAGE AND APPLIED STRESS DATA
DIGITAL MICROCIRCUITS

Subsystem Name and Reference No.	Schematic Title No. Rev.	Next Assy Title
	Assy Title No. Reference No.	No. Rev. Reference No.

Line No.	Ckt Ref Sym	Part Number	Mfg Part Number	Package Type	Mfr	Part Parameters - Rated							
						Supply Voltage V_{CC}	V_I Min	V_I Max	Operating I_{OH}	Operating I_{OL}	Power Dissip Max	Case Temp Max	Open Collector Dc Output Voltages

Report No. and Revision Date	Analyst Name Date	Cog. Eng. Approved Date
JPL Section No. Approved Date	JPL Reliability Approved Date	Sheet ____ of ____

DIGITAL MICROCIRCUITS (JPL Form 2302 Rev. 11/79 Page 1)

NOTE: Page 1 gives only the parameter ratings.

- **Circuit symbol number**
  This number should be recognizable from the schematic diagram supplied with the stress analysis.

- **Part number**
  This entry should be enough to specify completely the type of part being used. JPL part number is preferred.

- **Manufacturer part number**
  The vendor part number is specified in this column. Use the vendor code from the JPL ZPP-2061-PPL. If the vendor is not listed, write in the vendor name.

- **Package type**
  The package in which the actual device is enclosed is entered in this column. This column is conveniently located right after the part number, where the device package information is usually appended.

- **Manufacturer (vendor)**
  The manufacturer is specified in this column. For devices screened at off-lab sites, the screening house should be entered also. If the manufacturer is not listed in the PPL with a manufacturer code, enter the name here if possible.

- **Rated supply voltage**
  The voltage specified in data books or sheets for which the device operation is guaranteed is entered in this column. Do not use absolute maximum ratings.

- **Rated V_I min.**
  The device's rated signal input voltage minimum is the absolute minimum voltage.

- **Rated V_I max.**
  The device's rated signal input voltage maximum is the absolute maximum input voltage at which the device will not be damaged due to overstress.

- **Rated Operating I_{OH}**
  The operating "output high" current is specified here. Usually this parameter is of concern when mixing different digital technologies or using "wired" logic. It is a measure of the ability of the device to source current.

- Rated Operating I_{OL}

The operating "output low" current is of concern for the same reason. This parameter is a measure of the ability of the device to sink current.

- Maximum rated power dissipation

The power dissipation of the device is of prime concern since it affects not only the reliability of this device but also the thermal contribution of the device to the local temperature. If not specified directly, the TTL power dissipation can be calculated as the product of the max VCC and the max ICC.

- Maximum rated case temperature

The maximum rated case temperature is usually the same as the maximum rated device temperature available from the manufacturer's data sheets.

- Rated open collector DC output voltage

For digital devices with open collector outputs, the open collector DC output voltage is most often used in level shifting, logic family interfacing, or low power drivers.

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PART USAGE AND APPLIED STRESS DATA
DIGITAL MICROCIRCUITS

Subsystem Name and Reference No.	Schematic Title No. Rev.	Next Assy Title
	Assy Title No. Reference No.	No. Rev. Reference No.

Line No.	Ckt Ref Sym	Part Number	Stress Data - Actual								Remarks	Application Rating	
			Supply Voltage V_{CC}	V_I Min	V_I Max	Operating I_{OH}	Operating I_{OL}	Power Dissip Max	Case Temp Max	Open Collector Dc Output Voltage		A	U

Report No. and Revision Date	Analyst Name Date	Cog. Eng. Approved Date
JPL Section No. Approved Date	JPL Reliability Approved Date	Sheet _____ of _____

PAGE 2 JPL 2302 R 11/79

DIGITAL MICROCIRCUITS (JPL Form 2302 Rev. 11/79 Page 2)

NOTE: Page 2 gives only the operating parameter actuals.

- Circuit symbol number

This number should be recognizable from the schematic diagram supplied with the stress analysis.

- Part number

This entry should be enough to specify completely the type of part being used. JPL part number is preferred.

- Actual supply voltage

This is the maximum actual supply voltage.

- Actual V_I min.

This is the minimum actual input voltage.

- Actual V_I max.

This is the maximum actual input voltage. If more than one type of input is available on the part, give the maximum actual input voltage for each type.

- Actual operating I_{OH}

The operating "output high" current is the maximum current which the device must source. Care must be taken that the device is not subject to greater "fan-out" than it is rated for. This column may be specified in terms of the maximum number of digital inputs driven by the device or preferably by the maximum current which the device is required to source. On multiple output devices, give the maximum current for the worst output.

- Actual operating I_{OL}

The operating "output low" current is the maximum current which the device must sink. Again, care must be taken that the device not be subject to excessive "fan-out". On multiple output devices, give or indicate the maximum current for the worst output terminal.

- Maximum actual power dissipation

The power dissipation is intimately related to the reliability of the device and the device's junction temperature. Some TTL circuits can dissipate up to 500 mW, depending on function and duty cycle. Give the maximum power dissipation. If the power dissipation exceeds the maximum rated power dissipation, give the duration of the excess and the duty cycle. The actual power dissipation can be conservatively calculated as the product of the actual maximum V_{CC} and the maximum rated I_{CC}. Note that the power

dissipation derating requirements are not applicable for digital devices which do not have variable output currents. For CMOS devices, the high switching rate losses into a predominantly capacitive load are calculated as CV^2f. These must be added to the standby power. Multiple output devices with "N" identical outputs are assumed to have a rated power per output equal to the device dissipation over N.

- Maximum actual case temperature

If the part has a heat sink, give the maximum actual case temperature and define the heat sink. If the part has no heat sink, give the maximum actual case temperature obtained from a thermal analysis.

- Actual open collector DC output voltage

If the device has open collector outputs, write in the maximum switched voltage in this column, otherwise leave blank.

Note that there are no entries for junction temperature. The JPL standard 110 °C maximum is assumed to be met if the case temperature of the IC is less than 95 °C and all other parameters are within the defined derating criteria of MIL-STD-975.

Note also that due to space limitations there are no stress ratio blocks provided; however, it is the analysts' responsibility to compare the page I allowables to the page 2 actuals and verify that the applicable derating criteria have been met.

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PART USAGE AND APPLIED STRESS DATA
DIODES SIGNAL, GENERAL PURPOSE AND RECTIFIER

SUBSYSTEM NAME AND REFERENCE NO.	SCHEMATIC TITLE / NO. / REV. ASSY. TITLE / NO. / REFERENCE NO.	NEXT ASSY. TITLE NO. / REV. / REFERENCE NO.

CKT. SYM. NO.	JPL PART NO., EIA REGISTRATION OR VENDOR PART NO.	MAX. RATED TEMP.		PART AMB. TEMP. °C	OPERATING FREQUENCY	POWER DISSIPATION					PEAK INVERSE VOLTAGE			FORWARD CURRENT			REMARKS	APPLICATION RATING	
		VENDOR	°C			RATED +25°C (NOMINAL)	(1) RATED MAX. AMB.	(2) PEAK ACTUAL	MAX. ACTUAL JUNCT. TEMP.	(2)/(1) STRESS RATIO	(3) MAX. RATED	(4) ACTUAL	(4)/(3) STRESS RATIO	(5) MAX. RATED	(6) PEAK ACTUAL	(6)/(5) STRESS RATIO	(DUTY CYCLE, HEAT SINK)	A	U

REPORT NO. AND REVISION / DATE	ANALYST NAME / DATE	COG. ENG. APPROVED / DATE
JPL SECTION NO. / APPROVED / DATE	JPL RELIABILITY APPROVED / DATE	SHEET ___ OF ___

JPL 2292 1/76

DIODES, SIGNAL, GENERAL PURPOSE, AND RECTIFIER (JPL Form 2292 Rev. 1/76)

- Circuit Symbol Number

This number should be recognizable from the schematic diagram supplied with the stress analysis.

- JPL part number; EIA registration or vendor part number

This entry should be enough to specify completely the type of part being used. JPL part number is preferred, EIA registration and vendor part numbers are second and third choices.

- Vendor

The vendor is specified in this column. Use the vendor designations from the JPL ZPP-2061-PPL. If the vendor is not listed, write in vendor name.

- Maximum rated temperature

This is the maximum rated operating temperature from the vendor data sheets or other applicable specification sheets.

- Part ambient temperature

Used for derating purposes; the expected ambient temperature during qualification testing is to be put in this column.

- Operating frequency

If this diode is used as a rectifier or frequency source, the operating frequency is filled in here.

- Power dissipation

1. Rated 25°C nominal
   The 25°C power rating for the diode is specified in this column. Clearly mark units of power at top of column.

2. Rated (at) maximum ambient
   The rated power dissipation for the device at maximum expected temperature is specified in this column. This value is most often drawn from power vs. temperature graphs in the manufacturer's data sheets.

3. Peak actual
   The actual peak power dissipation during normal duty in normal operation is put in this column. Protection diodes which function only in case of another component failure or malfunction are an exception; in that case, the diode normal operating mode is due to a circuit malfunction or failure mode and the diode peak power dissipation is the power dissipation during this abnormal mode.

4. Maximum actual junction temperature
   Semiconductor junction temperature is the most influential parameter in determining the expected life of the device. Junction temperatures are usually determined from knowledge of device construction and power dissipation. Thermodynamic models of the part and its mounting are required to adequately determine expected junction temperatures. Contact Reliability Engineering for further information.

5. Stress ratio
   The stress ratio is the Peak Actual power dissipation from item 3 above divided by the Rated Max Ambient power dissipation from item 2 above. Note that if the duration of the peak is less than the thermal time constant of the diode junction, an effective peak can be analytically determined and used in item 3.

- Peak inverse voltage

1. Maximum rated
   The maximum rated peak inverse voltage is a measure of the voltage which can be applied to the device without damage or degradation due to punch-through.

2. Actual
   The actual peak inverse voltage is the maximum which the device sees in normal use.

3. Stress ratio
   The stress ratio is the peak inverse voltage in actual use divided by the maximum rated peak inverse voltage.

- Forward current

1. Maximum rated
   The maximum rated forward current is the amount of current which can be conducted by the diode without excessive heating. This parameter is sometimes specified along with temperature in graphical form. In that case, the expected qualification ambient temperature should be used.

2. Peak actual
   The actual peak forward current which the device sees in normal use is put in this column.

3. Stress ratio
   The stress ratio is the peak actual forward current divided by the maximum rated forward current.

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PART USAGE AND APPLIED STRESS DATA
DIODE-ZENER

SUBSYSTEM NAME AND REFERENCE NO.	SCHEMATIC TITLE / NO. / REV.	NEXT ASSY. TITLE
	ASSY. TITLE / NO. / REFERENCE NO.	NO / REV. / REFERENCE NO.

CKT. SYM. NO.	JPL PART NO., EIA REGISTRATION OR VENDOR PART NO.	VENDOR	PART AMB. TEMP. °C	POWER DISSIPATION					ZENER VOLTAGE		ZENER CURRENT			REMARKS	APPLI-CATION RATING	
				RATED +25°C (NOMINAL)	(1) RATED MAX. AMB.	(2) PEAK ACTUAL	(2)/(1) STRESS RATIO	MAX. ACTUAL JUNCT. TEMP.	RATED NOM.	ACTUAL	(3) RATED NOM	(4) PEAK ACTUAL	(4)/(3) STRESS RATIO	(DUTY CYCLE, HEAT SINK)	A	U

REPORT NO. AND REVISION / DATE	ANALYST NAME / DATE	COG. ENG. APPROVED / DATE
JPL SECTION NO. / APPROVED / DATE	JPL RELIABILITY APPROVED / DATE	SHEET OF

JPL 2293 1/75

DIODES, ZENER (JPL Form 2293 Rev. 1/75)

- Circuit Symbol Number

This number should be recognizable from the schematic diagram supplied with the stress analysis.

- JPL part number; EIA registration or vendor part number

This entry should be enough to specify completely the type of part being used. JPL part number is preferred, EIA registration and vendor part numbers are second and third choices.

- Vendor

The vendor is specified in this column. Use the vendor designations from the JPL ZPP-2061-PPL. If the vendor is not listed, write in vendor name.

- Part ambient temperature

Used for derating purposes; the expected part ambient temperature during qualification testing is to be put in this column.

- Power dissipation

1. Rated 25°C nominal
   The 25°C power rating for the diode is specified in this column. Clearly mark units of power at top of column.

2. Rated maximum ambient
   The maximum rated power dissipation for the device at qualification mission temperature is specified in this column. This value is most often drawn from power vs. temperature graphs in the manufacturer's data sheets.

3. Peak actual
   The actual peak power dissipation during normal duty in normal operation is put in this column. Protection diodes which function only in case of another component failure or malfunction are an exception; in that case, the diode normal operating mode is due to a circuit malfunction or failure mode and the diode peak power dissipation is the power dissipation during this abnormal mode.

4. Stress ratio
   The stress ratio is the peak actual power dissipation divided by the rated maximum ambient power dissipation.

5. Maximum actual unction temperature
   Semiconductor junction temperature is the most influential parameter in determining the expected life of the device.

Junction temperatures are usually determined from knowledge of device construction and power dissipation. Thermodynamic models of the part and its mounting are required to adequately determine expected Junction temperatures. Contact Reliability Engineering for further information.

- Zener voltage

1. Rated nominal
   The nominal rated zener (or avalanche) voltage is specified here.

2. Actual
   The maximum actual operating zener or avalanche voltage is specified here (nominal plus manufacturer's initial tolerance).

- Zener current

1. Rated nominal
   The nominal rated zener conduction current is given in this column. Rated current is sometimes related to temperature and may reside in the form of graphical plots in the specification. NOTE: The "ra ted nominal" should not be confused with the zener test current. The "rated nominal" current is based on the diode "rated 25°C nominal" power divided by the "actual zener voltage". This rated max ambient power may be lead length dependent, since the leads and not the case are usually the major conduction path for nonstud- or nontab-mounted diodes.

2. Peak actual
   The actual peak current to which the diode is subjected is put in this column. Peak currents can cause the diode to fail to mai ntain zener voltage in some cases, or can cause excessive dissipations.

3. Stress ratio
   The stress ratio of the diode is the actual peak current divided by the rated nominal current.

Note that the purpose of this entry is current density and voltage regulation oriented, rather than power dissipation oriented.

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PART USAGE AND APPLIED STRESS DATA
LINEAR MICROCIRCUITS

Key
O Operational Amplifiers
R Regulators
C Comparators
S Sense Amplifiers
A Analog Switches
I Current Amplifiers

Subsystem Name and Reference No.	Schematic Title No. Rev.	Next Assy Title
	Assy Title No. Reference No.	No. Rev. Reference No.

Line No.	Ckt Ref Sym	Part No.	Mfg Part No.	Part Parameters - Rated											
				(All) Power Supply Voltages		(All) Power Diss	(All) Output Current	(ORCSI) Max Short Circuit Current	(All) Temp Max 85°C Amb	(All) Power Supply Sequence	(O,C,S) Max Diff Voltage Input	(R,I) Single Ended Input Voltage	(C,S) Open Collector DC Input Voltage	(O,I) Output AC Voltage	(R) Input/ Output Voltage Diff
				V+	V-										

Report No. and Revision Date	Analyst Name Date	Cog. Eng. Approved Date
JPL Section No.	JPL Reliability Approved Date	Sheet ______ of ______
Approved Date		

LINEAR MICROCIRCUITS (Page 1 JPL Form 2305 Rev. 4/80)

NOTE: Page 1 gives only the parameter ratings.

- **Circuit Symbol Number**

This number should be recognizable from the schematic diagram supplied with the stress analysis.

- **Part number**

This entry should be enough to specify completely the type of part being used. JPL part number is preferred.

- **Manufacturer part number**

The vendor part number is specified in this column. Use the vendor code from the JPL ZPP-2061-PPL. If the vendor is not listed, write in the vendor name.

- **Power supply voltages**

1. V+
   V+ is the maximum rated positive supply voltage. If the device only operates with a grounded positive supply, enter zero in this column.

2. V-
   V- is the maximum rated negative supply voltage. If the device only operates with this supply grounded, enter zero.

- **Rated power dissipation**

The rated device power dissipation is entered in this column.

- **Rated output current**

The rated output current for the device is entered in this column. If the device can source more current than it sinks, or vice versa, put both values down with a diagonal slash through the column.

- **Rated maximum short circuit current (not applicable to analog switches)**

The maximum rated short-circuit current is entered in this column. If time or temperature dependent, this should be so noted.

- **Maximum rated temperature**

The maximum rated temperature is taken from the device specification sheet and is the maximum package temperature at which the device is operable to guaranteed performance limits.

- **Power supply sequence**

Any limitations of turn on sequences of voltages should be noted (e.g. no input V before supply V, etc.).

This entry is applicable only to circuits which may approach this condition during normal operation or as the result of erroneous box level testing procedures; otherwise, enter N/A.

- Maximum rated differential input voltage

This parameter is applicable only to op-amps, comparators, and sense amplifiers.

- Rated single ended input voltage

Applicable only for regulators and current amplifiers; this parameter is a measure of the inherent percentage regulation or gain.

- Open collector DC input voltage

This is applicable only to comparators and sense amplifiers with open collector output configurations, which apply an external voltage as an input to the IC output terminal.

- Rated output AC voltage

Applicable only to op-amps and current amplifiers, this parameter is related to slew rate, the pole (resonance) frequencies, and the compensation applied to the amplifier.

- Input/output voltage differential

Applicable only to regulator ICs. This parameter is a measure of the device's relative regulation capacity. Regulators are designed to operate near the regulated voltage value. I/O differential is specified to give the designer a range of regulatable input voltages for the device.

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PART USAGE AND APPLIED STRESS DATA
LINEAR MICROCIRCUITS

Key
- O Operational Amplifiers
- R Regulators
- C Comparators
- S Sense Amplifiers
- A Analog Switches
- I Current Amplifiers

Subsystem Name and Reference No.	Schematic Title / No. / Rev.	Next Assy Title
	Assy Title / No. / Reference No.	No. / Rev. / Reference No.

Line No.	Ckt Ref Sym	Part No.	Stress Data - Actual												Remarks	Application Rating	
			(All) Power Supply Voltages		(All)	(All)	(ORCSI)	(All)	(All)	(O,C,S)	(R,I)	(C,S)	(O,I)	(R)			
			V+	V-	Power Diss	Output Current	Max Short Circuit Current	Temp Max Amb	Power Supply Sequence	Max Diff Voltage Input	Single Ended Input Voltage	Open Collector DC Input Voltage	Output AC Voltage	Input/Output Voltage Diff		A	U

Report No. and Revision — Date	Analyst Name — Date	Cog. Eng. Approved — Date
JPL Section No.	JPL Reliability Approved — Date	
Approved — Date		Sheet _______ of _______

LINEAR MICROCIRCUITS (Page 2 JPL Form 2305 Rev. 4/80)

NOTE: Page 2 gives only the operating parameter actuals

- Circuit Symbol Number

(Should be the same as was entered on page 1)

- Part Number

(Should be the same as was entered on page 1)

- Manufacturer part number

(Should be the same as was entered on page 1)

- Actual power supply voltages

1. V+
   V+ is the maximum actual positive supply voltage. If the device operates with a grounded positive supply, enter zero in this column.

2. V-
   V- is the maximum actual negative supply voltage. If the device operates with this supply grounded, enter zero.

- Actual power dissipation

The actual device power dissipation is entered in this column.

- Actual output current

The actual output current for the device is entered in this column. If the device must source more current than it sinks, or vice versa, put both values down with a diagonal slash through the column.

- Actual maximum short circuit current (not applicable to analog switches) The maximum actual short-circuit current is entered in this column for devices with settable current limiters. This entry is applicable to circuits which may approach this condition during normal operation or as the result of erroneous box level testing procedures; otherwise, enter N/A.

- Maximum actual device temperature

The maximum actual temperature is taken from the expected device temperature and is the maximum package temperature at which the device operates during qual testing. A thermal analysis will be required to determine the mounted part ambient temperature.

- Power supply sequence

Define the usage sequence for any devices noted on page 1.

- Maximum actual differential input voltage

This parameter is applicable only to op-amps, comparators, and sense amplifiers. It is the maximum differential input voltage to which the device is subject during operation.

- Actual single ended input voltage

Applicable only for regulators and current amplifiers; this parameter delineates the maximum regulated or sampled voltage and serves as a measure of the stress applied to the input circuit.

- Actual open collector DC input voltage

The maximum actual voltage applied to the open collector from an external source should be entered here.

- Actual output AC voltage

Applicable only to op-amps and current amplifiers, this parameter serves to evaluate the stress on the output circuitry of the device when related to the rated AC output voltage.

- Actual input/output voltage differential

Applicable only to regulator ICs. This parameter is a measure of the device's relative regulation capacity. Regulators are designed to operate near the regulated voltage value. It is possible to operate the device only within the rated limits.

Note that there are no entries for junction temperature. The JPL standard 110 °C maximum is assumed to be met if the case temperature of the IC is less than 95 °C and all other parameters are within the defined derating criteria of MIL-STD-975. Specific junction temperatures may be computed if vendor supplied 0_{JC} values are attainable.

Note also that due to space limitations there are no stress ratio blocks provided; however, it is the analysts' responsibility to compare the page 1 allowables with the page 2 actuals and verify that the applicable derating criteria have been met.

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PART USAGE AND APPLIED STRESS DATA
RESISTORS – FIXED

SUBSYSTEM NAME AND REFERENCE NO.	SCHEMATIC TITLE	NO.	REV.	NEXT ASSY. TITLE		
	ASSY. TITLE	NO.	REFERENCE NO.	NO.	REV.	REFERENCE NO.

CKT. SYM. NO.	CONSTRUCTION		JPL PART NO., VENDOR OR MIL TYPE NUMBER	VENDOR	NOM. RES (OHMS)	MFG. TOL. %	PART AMB. TEMP °C MAX/MIN	VOLTAGE			POWER DISSIPATION						WAVE FORM (DC, SINE, PULSE, ETC.)	REMARKS (HEAT SINK, DUTY CYCLE)	APPLICATION RATING	
	RESISTIVE ELEMENT	TYPE ENCLOSURE						(1) NOM RATED	(2) ACTUAL MAX	(2)/(1) STRESS RATIO	MAX RATED	TEMP AT PD MAX	TEMP AT PD=O	(3) RATED AT T AMB.	(4) ACTUAL MAX	(4)/(3) STRESS RATIO			A	U

REPORT NO. AND REVISION	DATE	ANALYST NAME	DATE	COG. ENG. APPROVED	DATE
JPL SECTION NO.	APPROVED	DATE	JPL RELIABILITY APPROVED	DATE	SHEET OF

JPL 2297 1/76

RESISTORS, FIXED (JPL Form 2297 Rev. 1/75)

- Circuit Symbol Number

This number should be recognizable from the schematic diagram supplied with the stress analysis.

- Construction

1. Resistive element - Specify the composition of the material which ma kes up the resistive element (i.e. Carbon comp., wirewound, film, etc.)
2. Type enclosure - Specify the package which encloses the resistive element. Normally, resistors are of the axial lead type, but sometimes may be pc mounted or rectangular or "chip" type.

- JPL part number; vendor or MIL type number

This entry should be enough to specify completely the type of part being used. JPL part number is preferred, vendor and MIL type numbers and vendors numbers are second and third choices. respectively.

- Vendor

The vendor is specified in this column. Use the vendor designations from the JPL ZPP-2061-PPL. If the vendor is not listed, write in vendor name.

- Nominal resistance

Write in the nominal resistance value of the resistor.

- Manufactured tolerance

The manufacturer's tolerance goes in this column.

- Part ambient temperature

Used for derating purposes; the expected ambient temperature during qualification testing is to be put in this column.

- Voltage

For resistors, the voltage rating is sometimes related to their power capacity. Most types, however, do have specified voltage ratings. Fill in the nominal rated value, the actual maximum value, and the stress ratio. The voltage rating is intended to be a measure of its dielectric strength from end to end or end to chassis, or body to chassis.

- Power dissipation

1. Maximum rated
   The maximum rated power dissipation is usually a function of the cross sectional area of the resistive element and is most often specified in milliwatts.

2. Temperature at P_d max.
   This temperature is interpreted as the maximum safe temperature of the body of the resistor itself at full dissipation and determines the weak point for the required power derating.

3. Temperature at $P_d = 0$
   This is the maximum safe temperature of the resistor body when it is dissipating no power. It is the upper end point of the power derating curve.

4. Rated at $T_{ambient}$
   This is the power dissipation rating at any ambient body temperature of interest (the qual plus rise to the part in most cases).

5. Actual maximum
   The actual maximum expected power dissipation is put here. This should be calculated based on the expected normal waveshape conditions (in AC cases) obeying

$$P_d = \frac{1}{T} \int_o^t VI\,dt$$

6. Stress ratio
   The stress ratio is the actual maximum power dissipation divided by the $T_{ambient}$ rated power dissipation.

- Waveform

If know, the waveform seen by the part should be entered here.

- Remarks

For pulse application, give the following:
Peak Pulse Power
Pulse Width (in seconds)
Number of Pulses
Time Period of One Cycle (on plus off time in seconds)

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PART USAGE AND APPLIED STRESS DATA
TRANSISTORS - BIPOLAR

SUBSYSTEM NAME AND REFERENCE NO.	SCHEMATIC TITLE / NO. / REV.	NEXT ASSY. TITLE
	ASSY. TITLE / NO. / REFERENCE NO.	NO. / REV / REFERENCE NO.

CKT. SYM. NO.	JPL PART NO., EIA REGISTRATION OR VENDOR PART NO	VENDOR	PART AMB. TEMP °C	OPERATING FREQUENCY	POWER DISSIPATION				V_{CE}			V_{CB}			V_{EB}			I_C			REMARKS (DUTY CYCLE, HEAT SINK)	APPLICATION RATING	
					RATED +25°C (NOMINAL)	RATED MAX AMB	PEAK ACT	MAX. ACT. JUNCT TEMP	(1) MAX RATED	(2) PEAK ACT.	(2)/(1) STRESS RATIO	(3) MAX RATED	(4) PEAK ACT.	(4)/(3) STRESS RATIO	(5) MAX RATED	(6) PEAK ACT.	(6)/(5) STRESS RATIO	(7) MAX RATED	(8) PEAK ACT.	(8)/(7) STRESS RATIO		A	U

REPORT NO. AND REVISION / DATE	ANALYST NAME / DATE	COG. ENG. APPROVED / DATE
JPL SECTION NO. / APPROVED / DATE	JPL RELIABILITY APPROVED / DATE	SHEET OF

JPL 2331 3/75

TRANSISTORS, BIPOLAR (JPL Form 2331 Rev. 3/75)

- Circuit Symbol Number

This number should be recognizable from the schematic diagram supplied with the stress analysis.

- JPL part number; EIA registration or vendor part number

This entry should be enough to specify completely the type of part being used. JPL part number is preferred, EIA registration and vendor part numbers are second and third choices.

- Vendor

The vendor is specified in this column. Use the vendor designations from the JPL ZPP-2061-PPL. If the vendor is not listed, write in vendor name.

- Part ambient temperature

Used for derating purposes; the expected part case temperature during qualification testing is to be put in this column.

- Operating frequency

The operating frequency of the transistor is entered here.

- Power dissipation

1. Rated 25°C nominal
   The 25°C power rating for the transistor is specified in this column. Clearly mark units of power at top of column.

2. Rated maximum ambient
   The rated power dissipation for the device at maximum expected ambient case temperature is specified in this column. This value is most often drawn from power vs. temperature graphs in the manufacturer's data sheets.

3. Peak actual
   The actual peak power dissipation during normal duty in qual testing is put in this column.

4. Maximum actual junction temperature
   Semiconductor junction temperature is the most influential parameter in determining the expected life of the device. Junction temperatures are usually determined from knowledge of device construction and power dissipation. Thermodynamic models of the part and its mounting are required to adequately determine expected junction temperatures. Contact Reliability Engineering for further information. The maximum junction temperature is that resulting from dissipation of the "peak actual" power at the maximum ambient temperature

unless the duration of the peak power can be shown to be shorter than the transistor junction thermal time constant.

- V_{ce}

1. Maximum rated
   The rated maximum collector-emitter voltage from the applicable data sheet is entered here.

2. Peak actual
   The expected peak collector-emitter voltage in normal operation is entered here.

3. Stress ratio
   The V_{ce} stress ratio is the peak actual V_{ce} divided by the maximum rated V_{ce},

- V_{cb}

1. Maximum rated
   The rated maximum collector-base voltage from the applicable data sheet is entered here.

2. Peak actual
   The expected peak collector-base voltage in normal operation is entered here.

3. Stress ratio
   The V_{cb} stress ratio is the peak actual Vcb divided by the maximum rated V_{cb}.

- V_{eb}

1. Maximum rated
   The rated maximum emitter-base voltage from the applicable data sheet is entered here.

2. Peak actual
   The expected peak emitter-base voltage in normal operation is entered here.

3. Stress ratio
   The V_{eb} stress ratio is the peak actual V_{eb} divided by the maximum rated $V_{eb.}$

- I_c

1. Maximum rated
   The rated maximum collector current from the applicable data sheet is entered here (use value specified at qual case temperature).

2. Peak actual
   The expected peak collector current in normal operation is entered here.

3. Stress ratio
   The I_C stress ratio is the peak actual I_C divided by the maximum rated I_C.

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PART USAGE AND APPLIED STRESS DATA
TRANSISTORS - JFET

SUBSYSTEM NAME AND REFERENCE NO.	SCHEMATIC TITLE / NO. / REV.	NEXT ASSY. TITLE
	ASSY. TITLE / NO. / REFERENCE NO.	NO. / REV. / REFERENCE NO.

CKT. SYM. NO.	JPL PART NO., EIA REGISTRATION OR VENDOR PART NO.	VENDOR	PART AMB. TEMP °C	OPERATING FREQUENCY	POWER DISSIPATION				V_{GS}			V_{DS}			I_G			I_D			REMARKS (DUTY CYCLE, HEAT SINK)	APPLICATION RATING	
					RATED +25°C (NOMINAL)	RATED MAX AMB	PEAK ACT	MAX. ACT. JUNCT TEMP	(1) MAX RATED	(2) PEAK ACT.	(2)/(1) STRESS RATIO	(3) MAX. RATED	(4) PEAK ACT.	(4)/(3) STRESS RATIO	(5) MAX RATED	(6) PEAK ACT.	(6)/(5) STRESS RATIO	(7) MAX. RATED	(8) PEAK ACT.	(8)/(7) STRESS RATIO		A	U

REPORT NO. AND REVISION / DATE	ANALYST NAME / DATE	COG. ENG. APPROVED / DATE
JPL SECTION NO. / APPROVED / DATE	JPL RELIABILITY APPROVED / DATE	SHEET OF

JPL 2299 R 3/75

TRANSISTORS, JFET (JPL Form 2299 Rev. 3/75)

- Circuit Symbol Number

This number should be recognizable from the schematic diagram supplied with the stress analysis.

- JPL part number; EIA registration or vendor part number

This entry should be enough to specify completely the type of part being used. JPL part number is preferred, EIA registration and vendor part numbers are second and third choices.

- Vendor

The vendor is specified in this column. Use the vendor designations from the JPL ZPP-2061-PPL. If the vendor is not listed, write in vendor name.

- Part ambient temperature

Used for derating purposes; the expected part ambient temperature during qualification testing is to be put in this column.

- Operating frequency

The operating frequency of the transistor is entered here.

- Power dissipation

1. Rated 25°C nominal
   The 25°C power rating for the transistor is specified in this column. Clearly mark units of power at top of column.

2. Rated (maximum ambient)
   The rated power dissipation for the device at maximum expected ambient case temperature is specified in this column. This value is most often drawn from power vs. temperature graphs in the manufacturer's data sheets.

3. Peak actual
   The actual peak power dissipation duri ng normal duty in qualification testing is put in this column.

4. Maximum actual junction temperature
   Semiconductor unction temperature is the most influential parameter in determining the expected life of the device. Junction temperatures are usually determined from knowledge of device construction and power dissipation. Thermodynamic models of the device and its mounting are required to adequately determine expected junction temperatures. Contact Reliability Engineering for further information. The maximum junction temperature is that resulting from dissipation of

the "peak actual" power at the maximum ambient temperature unless the duration of the peak power can be shown to be shorter than the transistor junction thermal time constant, in which case the average power shall be used.

- V_{gs}

1. Maximum rated

   The rated maximum gate-to-source voltage from the applicable data sheet is entered here.

2. Peak actual
   The expected peak gate-to-source voltage in normal operation is entered here.

3. Stress ratio
   The V_{gs} stress ratio is the peak actual V_{gs} divided by the maximum rated V_{gs}.

- V_{ds}

1. Maximum rated
   The rated maximum drain-to-source from the applicable data sheet is entered here.

2. Peak actual
   The expected peak drain-to-source voltage in normal operation is entered here.

3. Stress ratio
   The V_{ds} stress ratio is the peak actual V_{ds} divided by the maximum rated V_{ds}.

- I_g

1. Maximum rated
   The rated maximum gate current from the applicable data sheet is to be entered here.

2. Peak actual
   The expected peak gate current in normal operation is entered here.

3. Stress ratio
   The I_g stress ratio is the peak actual I_g divided by the maximum rated I_g.

- I_d

1. Maximum rated
   The rated maximum drain current from the applicable data sheet is entered here.

2. Peak actual
   The expected peak drain current in normal operation is entered here.

3. Stress ratio
   The I_d stress ratio is the peak actual I_d divided by the maximum rated I_d.

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PART USAGE AND APPLIED STRESS DATA
GENERAL PURPOSE

SUBSYSTEM NAME AND REFERENCE NO.	SCHEMATIC TITLE	NO.	REV	NEXT ASSY. TITLE		
	ASSY. TITLE	NO.	REFERENCE NO.	NO.	REV.	REFERENCE NO.

CKT. SYM. NO.	VENDOR	PROCUREMENT DOCUMENT	PART AMB. TEMP. °C	APPLICABLE SPECIFICATION DATA (RATED-WATTAGE, VOLTAGE, CURRENT, TEMPERATURE RISE, ETC.)	PEAK VALUE, DUTY CYCLE, WATTAGE, VOLTAGE, CURRENT, TEMP. RISE, ETC.	STRESS RATIO	APPLI-CATION RATING	
							A	U

REPORT NO. & REVISION	DATE	ANALYST NAME	DATE	COG. ENG. APPROVED	DATE
JPL SECTION NO.	APPROVED	DATE	JPL RELIABILITY APPROVED	DATE	SHEET OF

JPL 2290 1/75

GENERAL PURPOSE (JPL Form 2290, 1/75)

Entries are the same as for other parts, except that a separate line is used for every significant stress parameter. This form could be used for fuses, relays and any other parts which do not fit the previously described forms.

D. STRUCTURAL STRESS ANALYSIS GUIDELINES

(LATER)

APPENDIX E

THERMAL ANALYSES GUIDELINES

While the other sections of this document set forth guidelines which are relatively mature, this is the first generation of thermal analysis guidelines. MIL Handbook 251 "Reliability/Design Thermal Applications", published in 1978, a 700 page handbook which gives step by step guidelines, requires significant updating and therefore is not recommended as a source for detailed guidance at this time.

Presented herein are a get of questions that the thermal analysis report should address and a checklist that is applicable for design reviews and consent to ship data packages, etc. This material is intended to be of value not only to the thermal reliability analyst, but also to the reviewer. Questions relative to the report documentation are organized in outline format. The review questions are intended to help in a qualitative assessment of the analyses and the communication process critical to meaningful analyses.

1.0 Summary

- o The specific purpose for the analysis:
  - o Part stress analysis data (PSA).
  - o Worst case analysis data (WCA).
  - o Fatigue life considerations - Thermal cycling environmental qualification.
- o Statement of the boundary conditions temperatures and conditions.
- o Type of analysis, i.e. steady state or transient.
- o Power dissipation assumed.
- o Summarize Results
  - o State the limiting condition or case.
  - o Indicate the number and magnitude of deviations, if any, that exist.
  - o Define the delta risk attributed to these deviations, including the effect of incorporating any design changes recommended.

2.0 Discussion

2.1 Unit Description - overview of the electromechanical packaging.

To include:

- o Verbal description of the housing type, material and dimensions.
- o A sketch of the packaging concept/design.
- o Number of subassemblies/boards, board typ e(s) and size(s).
  - o Example: four of the 10 boards are 10 layer "G-10" boards and the rest are two sided Duroid boards, etc.
- o Method of attaching the board(s) to the housing.
  - o Example: four of the 10 boards are bonded and mechanically fastened to the web while 6 of the 10 are stacked.

2.2 Thermal Environment

- o Reference the particular project documents which specify the thermal environments) for design and test including the levels for each particular analysis type (piece part stress analysis, WCA, solder joint fatigue, etc.).
- o Are these environments steady state or transient?
- o What modes of heat transfer (radiation, conduction or convection) were included in the model internally and externally?
- o Was the Spacecraft (S/C) thermal control surface (TCS) considered isothermal (uniform in temperature)?

2.3 Power Dissipation

- o Individual piece part power dissipations should be obtained from the Piece Part Stress Analysis Sheets. These dissipations should represent worst case **realistic** piece part dissipations based on the circuit design. To the extent necessary, module/unit/assembly level dissipations should reflect actual (measured or expected) dissipations rather than the maximum specification value.

Engineering judgement should be intelligently applied when considering a basis for the module/unit/assembly level dissipations because changes that occur during the normal product development cycle can necessitate updates to the thermal model if too low of a module/unit/assembly dissipation is initially chosen.

- Redundancy - Circuit redundancy is not typically identified on the parts stress sheet, thus this should always be determined. For example most redundancy designs have a side "A" and "B", of which only one side is "on" at a time. However, some system redundancies have the "prime" side "on" and the other in "standby". Check the for system redundancy and the nature of the redundancy before proceeding.

- Does the circuit contain exclusive or's which allow only one **or** the other to be "on" at a time? How was this handled?

- Is the power dissipation continuous or pulsed? Was a duty cycle assumed? If so, what is the dwell time and pulse width?

3.0 Results

- Were all piece parts analyzed? If not, state reason why? (Power density is not a valid argument). See the overview section for the background explanation.

- For those parts where deviations were reported, has the supplier of the power dissipation data been notified of the exceedance and asked if the power dissipations are in fact that much?

4.0 Recommendations/Conclusions

- What do these recommendations "buy"?

- If packaging changes are recommended, what risks are associated with them?

5.0 Thermal Model

- What type of model was generated? Steady State, Transient?

- o Description of model
  - o Number of nodes.
  - o How were the boundary conditions treated?
  - o Material property and dimensional values assumed.
  - o Masses assumed for transients.
- o Was a thermal analysis code used?
  - o If so, which one?
  - o Are there self explanatory comments in the input file which show the assumptions, etc.?
    - o Are the comments sufficient to spot check some of the calculations?
- o What was the source for piece part dimensions, theta junction-to-case, etc.?

Check List PDR, CDR, Pre Environmental Test Review (PEnv) and Consent-to-Ship (Cship)

PDR,CDR, PEnv,Cship o If the thermal analysis recommended design changes. were these incorporated into the design.

PEnv o Is the expected power dissipation during the environmental test equal to or less than the dissipation assumed in the thermal analysis?

Cship o What changes have been made since the thermal analysis was performed?

- o Were the reliability analyses updated to include these changes?
  - o Were these changes thermally analyzed?

Cship o How does the measured power dissipation contained in the Consent-to-Ship package compare with the dissipation assumed in the thermal analysis?

Cship o Were any problems encountered during the build process which necessitated a change in the packaging?

APPENDIX F

FAULT TREE ANALYSES GUIDELINES

1.0 INTRODUCTION

A comprehensive program to anticipate nearly all identifiable causes of failure and endeavor to prevent their occurrence can be used to insure that hardware will achieve a high level of reliability. The program is initiated by developing a comprehensive fault tree where the user strives to identify all of the possible failure causes of a subsystem or component. These failure causes are compiled and combined with the prevention measures of the program to form a matrix. The fault tree and the matrix-form are two essential tools of this program. The fault tree is used for the identification of critical fault paths. The matrix-form is used for identifying detailed faults that lead to component design changes and to programmatic changes, i.e., the matrix-form can help in identifying additional analysis, testing or inspections that are needed for a failure prevention program.

To provide the level of detail required, the failure causes that can occur from the interworking of the mechanical piece parts, as well as those failure causes that can occur from the operating environment acting on the individual piece parts, must be identified. The program is flexible and can be applied successfully to many different types of equipment, including the following types of components: mechanical, electromechanical, photodetector, blanket and heater. When properly used, fault tree/matrixform program will appreciably reduce the probability of failure during equipment use.

2.0 FAULT TREE/MATRIX-FORM PREPARATION

There are three steps in the fault tree and matrix-form preparation program:

A. The evolutionary compilation of discrete modes of failure and their associated causes, using a detailed fault;
B. The development of the corresponding matrix-form that combines the "generated failure causes from the fault tree" with the "planned preventive measures of the program."
C. Concurrence by the design agency that the applicable preventive measures regarding the matrix items are, or will be, part of its reliability program; this concurrence must be among individuals in analysis, design, quality assurance, manufacturing, and/or other disciplines involved in delivering the equipment.

A brief description of each of the program's three main steps is given below.

2.1 STEP 1: THE FAULT TREE

A fault tree analysis (FTA) can be described as an analytical technique, whereby an undesired or failed state of the system is specified, and all credible ways (faults) that the operating environment and/or lower levels of the system can cause this state to occur are identified. The fault tree (FT) itself is a graphical model of the system, which shows the logical interrelationship of the faults in the lower levels of the system. A fault tree thus depicts the logical interrelationship of basic events that lead to the undesired event - which is the top event of the fault tree. These faults can be associated with component hardware failure, human errors, or any other pertinent events which can lead to the undesired or failed state. It is important to realize that a fault tree is not a model of all possible system failure or all possible causes for system failure. A fault tree is tailored to a specific top event, thus includes only those lower level faults that contribute to that top event. Thus, if there is more than one undesired or failed state of the system, a fault tree for each must developed.

The fault tree is based upon deductive reasoning, that is, reasoning from the general to the specific. A specific fault is postulated, and then an attempt is made to determine modes of system or component behavior that contributed to this failure. Fault tree analysis focuses on one particular undesired event at a time and determines all credible causes of that event. The undesired event is the top event in that fault tree diagram. It is generally a complete, or catastrophic, failure rather than a drift type of failure. Careful definition of the top event is extremely important to the success of the analysis. If the top event is too general, the analysis becomes unmanageable if it is too specific, the analysis does not provide a sufficiently broad view of the system. Fault tree analysis can be a time-consuming exercise, and its cost must be measured against the cost associated with the occurrence of that specific undesired event. Fault tree analysis is particularly useful in studying highly complex functional paths for which the outcome of one or more combinations of noncritical events may produce an undesirable critical event. Typical FTA candidates are functional paths or interfaces that could have a critical impact upon the safety or yield undesired performance of a given functional system. It is important to point out that a fault tree is not in itself a quantitative model. It is a qualitative model that can be evaluated quantitatively and often is.

Fault tree methods should be applied in the early design phase, and then progressively refined and updated as the design evolves to track the probability of an undesired event. Initial fault tree diagrams might represent functional blocks (for example, units, or equipments), becoming more definitive at lower levels as the design materializes in the form of specific parts and materials.

Potential applications for the results of a fault tree analysis re shown in Table F-1. The input data requirements for performing an FTA are summarized in Table F-2.

Figure F-1 shows an example FT with some possible types of faults which would lead to the postulated failure.

The first step in formulating the FT is the choice of an observed subsystem level functional fault (e.g., antenna fails to move, scan mirror failure, etc.). This functional fault is then the top level of the Fault tree. The analyst must then postulate the various lower level faults or failures which, individually or in combination, lead to the next level fault in question. As a rule, the FT should be performed to the level at which preventive measures can be effected. This level will most often be to that of the failed mechanical component (i.e., motor, bearing, shaft, etc.) excepting parts which are internal to procured items and which are not specifically called out in detailed specifications of the item.

The use of logical "AND" and "OR" symbols graphically depicts the combination of mechanical faults which lead to the observed higher level fault. The "AND" symbol means that the failures which feed into it on the FTA must both occur for the observed higher level fault to occur. The "OR" symbol means that either of the failures which feed into the symbol will cause the observed higher level fault to occur.

Events or observations related to the fault are, as the fault itself, put into rectangular boxes. An event or observation which is described by a basic system component or part failure is put into a circle. Events or observations which are terminations of the fault sequence (for reasons of lack of sufficient information or to indicate further development) are put into diamond shaped parallelograms. These circles, boxes, and diamonds are logically connected by the logical "AND" and "OR" gates in pursuit of the description of the relation between the lower level and upper level faults.

Table F-1. Potential Applications for FTA Results

1. Allocation of critical failure mode probabilities among lower levels of the system
2. Comparison of alternative design configuration from a functionality or safety point of view
3. Identification of critical fault paths and design weaknesses for subsequent correction action
4. Evaluation of alternative corrective action approaches
5. Development of operational, test, and maintenance procedures to recognize and accommodate unavoidable critical failure modes

Table F-2. Input Requirements for an FTA

1. Definition of events and interconnections
2. Definition of the principle postulated fault and its modes of failure
3. Definition of applicable possible human errors
4. Equipment design information
5. Definition of the maintenance concept for the equipment
6. Definition of the equipment operating conditions
7. Definition of the equipment use

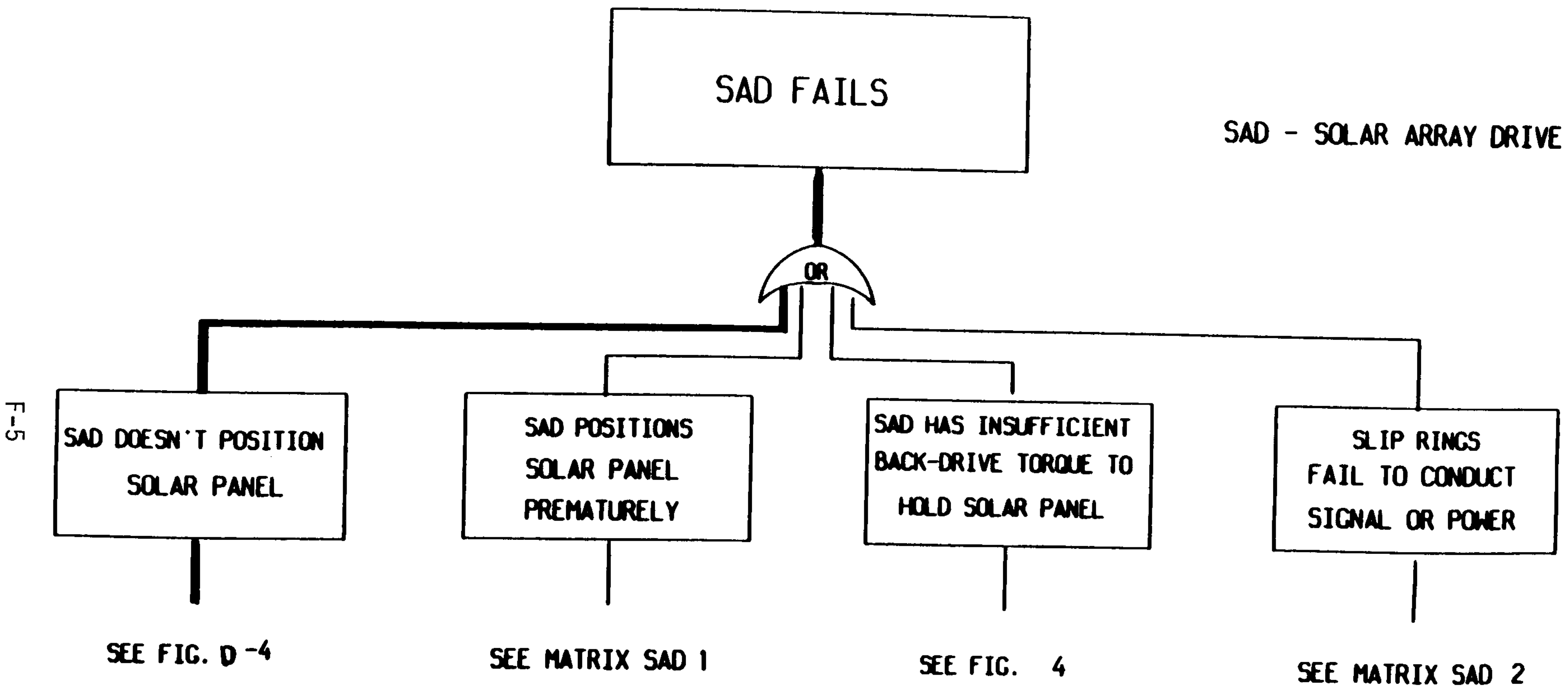

Figure F-1. Fault Tree Analysis Example

2.2 STEP 2: THE MATRIX FORM

After the fault tree has been constructed, the information is transferred to the matrix-form. In effect, the top section of the matrix form represents the bottom levels of the fault tree (or fault tree branch) with the causes of failure indicated in the vertical columns. The information on the fault tree matrix form need not be detailed on the fault tree itself. Rather than actually constructing the bottom-most branches of the fault tree, simply refer to the appropriate page number of the matrix (see example in Figure F-2). The preventive measures are listed down the left-hand side of the matrix (the y-axis). The circle symbol in the matrix grid ties the failure causes to the preventive measures.

After the top section of the matrix-form has been completed by the engineer responsible for the design or for monitoring the design, various product assurance specialists should be consulted to assist in listing preventive measures. The overall process, however, requires contact with specialists of various disciplines. Conferees can include, in addition to designers, quality assurance engineers, inspectors, systems engineers, and others, as may be needed to complete the forms. As might be anticipated, the better the communications with these specialists, the higher the matrix quality.

An underlying premise of the matrix-form process part of this program is that failure causes usually cannot be separated into groups, or ranked, according to their probability of occurrence. Therefore, when the matrices are being developed, the user should refrain from selecting one failure cause over another, but should list all causes of failure (even trivial ones), discarding only the most extreme causes, e.g., a meteorite damaging the spacecraft on the launch pad. This method of selection ensures that a complete ensemble of discrete failure causes is available for comparison on the matrix with the planned preventive measures of the program.

An important part of the matrix-form process is to use imagination together with component knowledge to search for failures which are not evident at first inspection. The identified failure causes are not removed from the matrix form even if later they are considered to be unlikely, untestable, intractable or not checkable.

The matrices should show what has happened, what is being done, and what future work will be done. They should reflect what will be done on the program.

The drawing of forms and the recording/manipulation of the data can be computerized.

2.3 STEP 3: FINAL CONCURRENCE OF THE FAULT TREE AND MATRIX-FORM DATA

The final phase of this task is getting concurrence from the project office that the corrective measures will be implemented. If corrective measures cannot be implemented to preclude or minimize the risk of a critical failure, the issue should be documented on a DDR form, as described in Section V of the document.

FAULT TREE MATRIX

NOTES (CONTD):
(9) THERMAL CYCLING/VIB
(8) CAL ERROR
(7) DUAL POTS (R1 & R2)
(6) DUE TO WEAR/OUT-OF-ROUNDNESS OF RESISTIVE ELEMENT

ABB .... & SYMBOLS:
POT - POTENTIOMETER
LI - LITTON INSTRUMENTS, NY STATE (POT VENDOR)
**REFERENCE ONLY, NO COVERAGE
MTG - MOUNTING
CAL - CALIBRATION
R - REFERENCE

DATE: 1/20/82
REVISION: NONE
JPL 3870 R 10/81

MATRIX (MX) NO: SHD 5
COMPONENT: POT (R1) ASS'Y (7)
COMPONENT FAILURE MODE: FAILS, GIVES ERRONEOUS TELEMETRY
PAGE: 11 OF 12

NEXT LEVEL FAILURE MODE	SINGLE POINT FAILURE?
UNEQUAL RESISTANCE POINT TO POINT/OPEN	NO
WIPER ARM FINGERS FRACTURE/WEAR OUT(6)	NO
DAMAGE	NO
ROTATION SHIFT (OUT OF CAL)/(8)	YES
ELECTRICAL CONDUCTION FAILURE	NO
ANGULAR CONTACT BEARING SEIZES	YES

NOTES:
(1) EXCESSIVE CURRENT
(2) RESULTS IN (TERMINAL TO RESISTIVE ELEMENT) DAMAGE, FROM SOLDERING
(3) FROM RESISTIVE ELEMENT (WIPERS ARE GANGED)
(4) BOTH POTS WOULD PROBABLY SHIFT
(5) BEFORE & AFTER VIB & THERMAL (WITH CAL CHECKS

ANGULAR CONTACT BEARING SEIZES — causes: SAME AS MOTOR BEARING, PAGE 2 LBA 18 (ENTIRE PAGE) EXCEPT POT BEARING LUBE TYPE IS OIL GE F50, SILICONE

ITEM NUMBER		PREVENTIVE MEASURES LIST	TO BE PERFORMED	RADIATION	NON-HOMOGENOUS MIX	FOREIGN PARTICLES	CRACKS, PLASTIC (9)	FATIGUE/FRACTURE	FAULTY MAT'L	WEAR OUT	WIPER FINGERS BURN (1)	OVERHEATED MTG PLASTIC (2)	OVER CYCLED-WEAR	ROUGH HANDLING	AXIAL SHIFT OF WIPER ARM (3)	WIPER ROTATION SLIP	CAL ERROR	POT HOUSING ROTATES (4)	LOOSE CONNECTION (VIB)	" (THERMAL)
1	ANALYSIS																			
2		RADIATION (JPL)	X	0																
3–9																				
10	TEST																			
11		FLT HDW FUNCTIONAL (5) (JPL)	X		0		0				0				0	0	0	0	0	0
12																				
13		FLT HDW THERMAL (NO VAC) (JPL)	X				0													0
14																				
15		LBA (SINE & RANDOM VIB) (JPL)	X				0													
16–21																				
22		VENDOR LIFE-CYCLE (TBD CYCLES) (LI)	X					0		0			0							
23		LIFE (GLL) THERMAL (TBD) (JPL)	X					0		0			0							
24	PROCESSES	CAL PROCEDURE (JPL)	X																	0
25–27																				
28	INSPECTION																			
29		VENDOR LINEARITY CHECK (LI)	X		0															
30																				
31		VISUAL @ VENDOR (OPEN LID) (JPL)	X			0						0		0						
32																				
33		MAT'L CERTS																		
34																				
35		VISUAL OF SOLDERING (CHECK TEMP) (JPL)	X									0								
36																				
37		TEAR DOWN BEFORE & AFTER (9) (JPL)	X				0													
38		TEAR DOWN, LIFE GLL (JPL)	X							0			0						0	0
39	COMMENTS	HI CERTS, PURCHASED PARTS	R						**											0
40–42																				

Figure F-2. Sample Fault Tree Matrix

APPENDIX G

SINGLE EVENT UPSET ANALYSIS GUIDELINES

1.0 INTRODUCTION

Single event upsets are any disturbance of a circuit caused by the energy deposited by a high energy particle as it interacts with the sensitive portions of an electrical device. The response could be a soft error (a bit flip which can be reset) or it could be a latch-up which could only be reset by a power down or could possibly burn out the device unless certain precautions (e.g., detecting a current surge and shutting off the power) are taken. The environments contributing to SEUs are predictable only in a statistical sense. Furthermore, the response of a susceptible device in a known environment is predictable only in a statistical sense. Therefore, SEU hardness can often be assured only in a statistical sense.

2.0 ASSURANCE PROCEDURES

The first step in developing hardness assurance is to obtain the necessary environmental description, such as omnidirectional flux as a function of particle species and energy. This information is provided by JPL Natural Space Environments Group (5217). The next step is to separate the electrical equipment into two classes (mission-critical and Other), identifying each subsystem according to its class. Within each subsystem, the parts susceptible to SEUs must be identified. For each susceptible part, the necessary susceptibility data must be obtained. This information is provided by Section 514. The next step is to combine the environmental data with the part susceptibility data to obtain an estimate on the SEU rate or probability. This calculation is performed by Group 5217 on request. The environmental data to be used depends on the individual case. If the device is in the mission-critical category and no upsets can be tolerated, and if the device has no protection against failures from upsets other than a low probability for upsets (due to a small cross section and/or a high threshold LET), fluence data should be used so that the probability of an upset during the mission can be estimated. If the device is missioncritical, but there are safeguards which will prevent failures due to upsets providing the upset rates do not get too large, peak flux should be used so that the peak upset rates can be estimated. If the device is in the "Other" category and occasional anomalies (e.g., noise in the data) can be tolerated, typical fluxes are usually most appropriate, providing the upset is a soft error which will not damage the device or other devices.

3.0 SEU ASSURANCE GUIDELINES

In general, a SEU hardness assurance plan has seven phases, as follows:

(a) Environment Definition.
(b) Setting of Allowable Malfunction Limits.
(c) Equipment Analysis.
(d) Malfunction Rate Predictions.
(e) Comparison of Predictions with Limits.
(f) Malfunction Effect and Design and/or Limits Revision.
(g) Repeat c) through f) until Predictions fall within Limits.

Part (a) "Environment Definition" - JPL Group 5217 personnel will provide environmental data appropriate for the mission trajectory,

Part (b) "Setting of Allowable Project Malfunction Modes and Rates" - will be performed at the project level. JPL Group 5217 participation will provide advisory inputs.

Part (c) "Equipment analysis" - The separation into Missioncritical and Other subsystems will be performed at the project level. Specification of LET threshold and cross-section as a function of shielding for parts within the system is the driving factor.

Part (d) "Malfunction Predictions" - the statistical rate of part malfunction predictions are made by JPL Group 5217 on request. Use of parts (a) and (c).

Part (e) "Malfunction Effect and Comparison of Predictions with Limits" - this task will be performed by reliability engineering or equipment designers, subsystem designers, and system designers.

Part (f) "Design and/or Limit Revisions" - this task will be performed by the appropriate combination of project personnel, system and subsystem designers.

4.0 HARDNESS DEMONSTRATION

The analysis should demonstrate that each mission-critical subsystem will perform within specifications during its time of operation and when exposed to the predicted environment. In addition, it should demonstrate that for each other subsystem, the time during which SEUs will cause it to operate out of specifications will not exceed the corresponding maximum acceptable limit set by the Project for that subsystem .

No direct testing for SEU hardness is required at the subsystem level. Performing the analyses, however, may require testing of some parts to determine their SEU thresholds and SEU cross-sections.

5.0 DATA AND CALCULATIONS

5.1 Time Related Characterizations of the Environment

Since the environment varies with time, it is useful to characterize it in three ways. The first way is to specify total fluence. This information would be used to calculate the total number of upsets that should be expected during the mission or the probability that an upset will occur sometime during the mission. This is a useful environmental description for critical components that are required to never malfunction and that have no safeguards against malfunctions (e.g., detector-corrector circuits) other than a low probability for upsetting (due to a small cross section and/or a high threshold LET). This is also a useful environmental description for parts that can suffer an occasional soft error, but are susceptible to, and not protected from, latchups.

The second characterization is the specification of peak fluxes. This is a useful environmental description for components that are required to never malfunction and that do have safeguards (e.g., detector-corrector circuits) that will prevent malfunctions providing that upset rates do not get too high.

The third characterization is the specification of typical orbit averaged fluxes together with a statement of when the fluxes are expected to be exceeded. A time profile would be desirable, but such information is rarely available, and a statement, such as "these fluxes will be exceeded during solar particle events, but such events are in progress less than 2% of the time", may have to suffice. This information is useful for devices that are not required to operate to specification during atypical times. It specifies how hard a part must be to have an acceptably low upset rate or probability during typical conditions, and it provides the designer with an idea of how often conditions will be atypical and the device performance below specification.

Since the environment is of a statistical nature, quantities such as total fluence and peak flux require a definition. The fluence from solar flare particles is the fluence (modulated by the Earth's magnetic field and mass shielding, as appropriate) that corresponds to a given confidence level (typically 95% for a class A project) as predicted by the current solar flare statistical model. Solar flare peak flux is the peak flux from a model that is intended to represent a flare that is as large or larger than any that have actually been measured. Documentation for these models is presently being constructed.

In the case of trapped particles, statistical models have not yet been developed. The current proton model (AP8, described in Reference (1)) refers to time average fluxes. Fluence over time periods of 6 months or more are not treated statistically, because the random time variations are

expected to have averaged out in that amount of time. Peak fluxes, as predicted by the current model, refer to fluxes that are maximized in location, but still averaged over time. To obtain a peak flux that includes short term time variations, it is necessary to apply an uncertainty factor to the model predictions (uncertainty factors, which represent variability of or lack of knowledge of the environment, should not be confused with design margins which are additional factors). The uncertainty factor is the product of two factors. The first factor represents uncertainty in the model's ability to predict time average fluxes (this factor should also be applied to the fluence prediction), and the second factor represents shortterm time variations. Since a statistical model does not exist, this uncertainty factor is based more on judgment than on analysis. More details can be found in Reference (2).

In the case of galactic cosmic rays, fluxes and fluences are easier to quantify, because the statistical variations are relatively small. The greatest uncertainty is in the prediction of future levels of solar modulation. Upper bound estimates (assuming no errors in the model) can be obtained by assuming solar minimum conditions regardless of the launch date. If this procedure is followed, a statistical treatment is not needed. Uncertainty factors may still be needed to account for other model uncertainties. No uncertainty factor is needed during solar maximum conditions if the environmental description applies to solar minimum because the estimate is conservative. An uncertainty factor should be used during solar minimum conditions. The model used for galactic cosmic rays is described in References (3) and (4).

The environmental requirements document should state the recommended uncertainty factor, if applicable, or the confidence level that was used, if applicable, for each component of the environment.

5.2 Particle Species Characterization of the Environment

The environmental description should discuss protons and the heavier ions separately, because the dominant SEU mechanism is normally different for the two classes of particles. The dominant contribution to upsets from the heavier ions is through direct ionization (the ion passes through a sensitive volume, such as a depletion region, and creates electron-hole pairs in sufficient quantity to trigger an upset). For protons, the dominant mechanism is usually through spallation (the proton hits the nucleus of a resident atom, and fragments produce the majority of the electron-hole pairs). Very sensitive parts can be upset by protons through direct ionization, but such parts should not be used in spacecraft applications.

The most convenient environmental description for protons, for calculating spallation-induced upsets, is omnidirectional integral flux (or fluence, see Section 5.1) versus energy. For the heavier ions, the most

convenient environmental description is the Heinrich flux. The Heinrich flux evaluated at a given LET (LET is linear energy transfer and is also called stopping power) is the flux of particles that have a LET greater than a given value.

A recent Shuttle experiment has found a surprisingly large flux of trapped helium in the radiation belts. A model for trapped helium does not yet exist. But only low energy helium ($E \leq 10$MeV) was detected in significant quantity, which suggests that a 40 mil aluminum shield should be adequate protection against it (see Reference (5)).

5.3 Characterization of Part Susceptibility

An experimental test is the only reliable way to characterize the susceptibility of a part. The part is placed in a high energy ion beam and the number of upsets is recorded. This test is done routinely by Section 514.

Typically, two tests are done: a proton test and a heavy ion test. Proton test data, in its most complete form, is a curve of device cross section versus proton energy. Sometimes only the asymptotic value of the cross section is given. This information is adequate for placing an upper bound on the proton induced upset rate via spallation (set the cross section equal to zero at energies below 15 mev and set it equal to its asymptotic value at energies above 15 mev). Heavy ion test data, in its most complete form, is a curve of device cross section versus LET. Sometimes only the threshold LET (the lowest LET such that upsets are observed) and the asymptotic value of the cross section are given. This information is adequate for placing an upper bound on the heavy ion induced upset rates (set the cross section equal to zero for LETs below the threshold and set it equal to its asymptotic value for LETs above the threshold).

Changes in part susceptibility due to total dose degradation or temperature effects have not been carefully monitored in previous tests. If the hardware cognizant engineer suspects significant total dose degradation or that the temperature of the part during operation will be significantly different than during the susceptibility test, he should consult Section 514 for guidance. They may recommend that another test be performed.

5.4 Combining Environmental Data with Part Susceptibility Data

Upsets due to spallation are a relatively simple calculation, because the cross section can be approximated as being independent of particle arrival direction (see Reference (6)). The curve of cross section versus energy and the curve of omnidirectional proton flux versus energy are combined in the obvious way to estimate upset rates.

The heavy ion induced upset rate is a non-trivial calculation, because the susceptibility of the part has a strong dependence on particle arrival direction. Furthermore, most test data come from cyclotron tests, which are limited in the angles that can be tested, so the part susceptibility is not completely characterized. There are still unknown parameters in the susceptibility characterization. Group 5217 calculates upset rates, on request, using a computer code that is based on the calculational methods described in Reference (7). The unknown parameters are adjusted between reasonable limits, so that a range of possible rates are given or an upper bound on the upset rate is given.

The duty cycle of the part should be considered when interpreting the results of these calculations. If the part is susceptible only during a small fraction of a given time interval, the probability of an upset during that time interval is modified accordingly.

5.5 Circuit Response to Parts Upsets

Group 5211 or the cognizant design group will perform this activity using the part upset rate calculated by Group 5217 for each of the parts being used in the system. All parts upset rates will be used in conjunction with the functional description and time of operation of the system to arrive at a number (upsets per mission) which describes the sensitivity of the system under analysis to the external environment. Depending on the data provided by 5217 for each of the parts (range of upset rates or worst case upset rate), Group 5211 will provide a range of upsets or worst case number of upsets for mission life.

Group 5211 will also provide a description and severity of each of the possible upsets, effects on operation, and, when applicable, percentage of data lost due to each particular upset.

6.0 REFERENCES

(1) Sawyer, D. M., and J. I. Vette, "AP-8 Trapped Proton Environment for Solar Maximum and Solar Minimum," National Space Science Data, Center, December 1976

(2) L. Edmonds to Distribution, "A Statistical Model for the Dose, For an Esc ape Trajectory, From Earth's Trapped Electrons," IOM 513786-161, August 4, 1986

(3) Edmonds, L., "Final Report: Cosmic Ray Environment Model for Earth Orbit," JPL Publication 84-98. January 15, 1985

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APPENDIX H

PARAMETER TREND ANALYSES

1.0 INTRODUCTION

All subsystems and components should be assessed to determine the measurable parameters that relate to performance stability. These parameters shall be monitored for trends starting at component acceptance testing and continuing during the system integration and test phases of the end items. The parameters shall be monitored within the normal test framework (i.e. , during functional tests, environmental tests, etc.). A system shall be established for recording and analyzing the parameters and any changes from the nominal, even if the levels are within specified limits. Trend analysis data shall be reviewed with the operational personnel to continue to record the trends throughout the life of the mission.

2.0 GUIDELINES

The most important aspect of the trend analysis task is the selection of the performance parameter to be tracked. These parameters not only need to be important to the functional performance of equipment, but they must be measurable during the test and mission phases. The statistical approach to be employed in the analysis are generally the most fundamental and elementary: including raw data frequencies and tabulations, and simple measures such as the mean (average), median, and percentiles. More sophisticated analyses may be used, but should be preceded by the generation and examination of the basic descriptive statistics discussed above. In many cases, a descriptive statistics approach, coupled with a graphical portrayal of the data, will be sufficient for trending purposes. General guidelines for the trend analyses are provided in NASA-STD-8070.5, dated October 1988, "NASA Standard, Trend Analysis Techniques."