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JPL D-15129

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**JPL AIRS, ARTP, DS1 AND TES PROJECTS,
JPL TECHNICAL INFRASTRUCTURE PROGRAM**

AND

**NASA RTOP NOS. UPN 323-79-2C/323-32-20
HIGH PERFORMANCE, HI-REL 16 BIT ADC FOR SPACE APPLICATIONS**

ANALOG-TO-DIGITAL CONVERTER PARTS EVALUATION FOR SPACE APPLICATIONS

OCTOBER 31, 1997

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OFFICE 507 ELECTRONIC PARTS ENGINEERING

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ACKNOWLEDGEMENTS

The work described in this report was performed by the Jet Propulsion Laboratory, California Institute of Technology, and was sponsored by the National Aeronautics and Space Administration, Office of Safety and Mission Assurance, Washington D.C. The activity reported herein was accomplished under NASA RTOP Nos. UPN 323-79-2C/323-32-20, the JPL Technical Infrastructure Program and JPL AIRS, ARTP, DS1 and TES projects.

The author wishes to acknowledge the contributions of the following individuals and firms:

JPL:

Mike Sandor
Sam Tauch
Dan Bergens
Edgar Svendsen
Tom Gindorf
Donna Turnbow
Bernie Rax
Jim Coss
Gary Swift
Harvey Schwartz
Linda Mayo
Susan Mackey
Phil Szeto
Sammy Kayali
Kevin Clark
Steve Manion
Sid Johnson
Tets Miyahira
Allan Johnston
Choon Lee
Mike Wiedeman

Parts Suppliers and Suppliers' Representatives:

Datel Inc.
Signal Processing Technology, Inc. (SPT)
Select Electronics
Linear Technology, Inc.
Bager Electronics
Maxim Semiconductors
Zeus Electronics
Harris Semiconductor
National Semiconductor
Burr-Brown Corp.
Analog Devices, Inc. (ADI)
Space Electronics, Inc. (SEI)
Megarad Sales, Inc.

Parts Users:

The Aerospace Corporation
Lockheed Martin Infra-Red Imaging Systems (LMIRIS)
Naval Research Laboratory (NRL)
US Army Space and Strategic Defense Command (USASSDC)
NASA Langley
NASA GSFC
NASA JPL

FORWARD

This report focuses on the work that was done recently evaluating several analog to digital converters (A/Ds). Some design engineers, who responded to our request for candidate test devices, were sufficiently interested to follow the effort to its conclusion.

The initial funding was provided by NASA, but included the supplementary contributions of multiple partners. RTOP funding is specifically intended for devices of interest to multiple NASA projects; to fully qualify a part for a specific project or mission requires project funds. In this case the TES project contributed half the costs of evaluating the 16 bit 7809. Leveraging possibilities were accomplished by simply communicating on goals. The vendor and we planned the pre and post electrical testing at the vendor site while JPL took responsibility for the radiation and reliability portion. This was the agreement with Datel and SPT. This use of vendor equipment saved significantly on test hardware and software development costs. When testing 24 bit devices, it became imperative to do so or else it was deemed cost prohibitive, as was the case with the ADI's product line overseas.

By communicating with other potential users, additional funding was leveraged over time as initial tests showed more promise. In our case, the most critical gate was latchup. While electronics cannot, in general, be shielded from single event effects, total dose can be mitigated with shielding. Space Electronics Inc. has been a regular JPL partner who provides shielded parts as a standard product. Some of their initial work was on a latchup protection circuit, which would ameliorate the single event effects, which the shielding could not affect, was begun under our effort with TES.

In order to keep pace with all the process and architectural changes it is necessary to form cooperatives that develop and nurture common goals. To keep pace with the move to commercial (COTS) type devices, it is necessary to establish partners to both analyze and test to obtain empirical data.

Lastly, I want to thank Shri Agarwal for his dedicated work as the technical lead in this effort. His work in the area of A/Ds, particularly in the low power area, helped us establish our leadership position.

Susan Mackey

Manager
NASA RTOP 323-79-2C/20
October 23, 1997

SUMMARY

As is clear from the list of acknowledgments, this work couldn't have been accomplished without the cooperation among the suppliers, users, and the NASA centers. Not only was the work done in an efficient and timely manner, but savings in several hundreds of thousands of dollars in the resources were realized as well. A variety of analog -to-digital converter (A/D) parts including the COTS (commercial-off-the-shelf) parts were evaluated. Reported herein is the status of various A/Ds evaluations, JPL usage is shown where applicable. Also, the A/D parts used on recent JPL projects have been included. Recommendations are made for future new work.

The information contained herein will be updated periodically to include newly evaluated devices of interest to the JPL/NASA community. Eventually this report and updates will be available at the following web site: http://parts.jpl.nasa.gov

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SECTION 1.0 INTRODUCTION

A variety of analog-to-digital converters (A/Ds) including the COTS (commercial-off-the-shelf) parts were evaluated. They can be divided into four distinct groups as distinguished by their speed, power and resolution: high speed, low power; ultra high speed, low resolution; very high resolution, low power; and general purpose, low power. The details of the evaluation performed and results obtained are summarized in section 2.0 with a brief description of each evaluated part given in section 3.0. The recommendations for future work are made in section 4.0. Given below are some of the highlights of the evaluation effort:

(i) Universal Test Board: An A/D motherboard was developed in-house to provide a test platform for performing single event latchup (SEL) and single event upset (SEU) testing. This will potentially save on future test development effort.

(ii) Spreading Resistance Measurements: Spreading resistance measurements were used as a diagnostic tool for the radiation susceptibility of integrated circuits.

(iii) Evaluation Boards: Evaluation boards available from the suppliers were utilized wherever possible.

(iv) Partnerships established: (1) Aerospace Corporation's Laser Test Facility was used for SEL testing of the Datel ADS937. (2) SPT and Datel performed pre and post irradiation electrical measurements at their respective facilities using their standard production test tapes - SPT tested the SPT7725 and Datel the ADS937.

(v) Communication /partnership with other NASA Centers: On devices of mutual interest with other NASA organizations, the single event tests at Brookhaven were jointly done. All NASA Centers were kept abreast of our progress via the RTOP quarterly reviews, phone calls, articles in NASA/GSFC publication EEE Links and JPL Office 507 electronic parts bulletin (EPB), etc.

(vi) Unexpected Test Results:

(a) Encountered cases where the parts with epi layer failed SEL test and those without it passed: National ADC12062 12-bit CMOS/epi A/D, and the Burr-Brown ADS7809 16-bit CMOS/epi A/D failed whereas the Linear Tech LTC1419 14-bit CMOS A/D passed the SEL test.

(b) Got mixed results from SEL testing of the 8-bit ultra high-speed bipolar ECL parts: Maxim MAX101 500Msps converter destructively failed SEL whereas the Signal Processing Technology SPT7725 200Msps part and the Harris HI1276 500Msps A/D showed no latchup.

This effort could not have been possible without the support of so many organizations and individuals.

SECTION 2.0 STATUS

Section 2.1

8-Bit Analog to Digital Converters Status

Part Information	**Manufacturer**	**Maxim**	**SPT**	**Harris**	**Harris**
	Part No.	MX101	SPT7725	HI1276	HS9008
	Process	Bipolar	Bipolar	Bipolar	CMOS
	Power Supply	+5V, -5.2V	-5.2V	-5.2V	5V
	Power Dissipation	7.5 W	2.2 W	2.8 W	400 mW
	Conversion rate/time	500 Msps	300 Msps	500 Msps	20 Msps
	JPL Usage	None	ARTP (?)	None	Cassini
	Availability	Yes	Yes	Yes	Yes
Test Results	**Construction Analysis**	Passed[1]	Passed	No Data	Passed
	Single Event Latchup	Destructively Failed	No Latchup, LET>100	No Latchup, LET>100	No Latchup
	Total Ionizing Dose	No Data	>100 krads (High dose rate)	No Data	>100 krads
	Reliability	No Data	Acceptable (Vendor Data)	No Data	Acceptable (JPL Data)
	Other	N/A	N/A	N/A	N/A

Notes:
LET units = MeV-cm2/mg
These converters use the parallel or flash architecture. MX101, SPT7725 and HI1276 were evaluated in FY97.
1. COB (Chip-on-board) Technology

Section 2.2

12-Bit Analog to Digital Converters Status

Part Information	**Manufacturer**	**ADI**	**National**	**MAXIM**	**MAXIM**	**Harris**
	Part No.	9871XE	ADC12062	7672RP	MX674A	HI574A
	Process	RBCMOS	CMOS	CMOS	BiCMOS	CMOS/Bipolar[1]
	Power Supply	+5V, -5V	+5V	+5V, -12V	+5V, +/-15V	+/-15V, +5V
	Power Dissipation	1 W	75 mW	110 mW	150 mW	500mW(+/-15V) 385mW(+/-12V)
	Conversion rate/time	5 Msps	1 Msps	5 us	15 us	25 us
	JPL Usage	AIRS	DS1	Cassini,MARS	Cassini(?)	Cassini
	Availability	See note 2	Yes	Yes	Yes	Yes
Test Results	**Construction Analysis**	Passed	No Data	Passed	Passed	Passed
	Single Event Latchup	No Latchup	LET=12	No Latchup	No Latchup	No Latchup
	Total Ionizing Dose	>200 krads	No Data	10 krads w/o RAD-PAK®	2 krads (Low dose rate)	5 krads (?)
	Reliability	Planned	No Data	Acceptable	Acceptable	Acceptable
	Other	N/A	N/A	N/A	N/A	N/A

Notes:
LET units = MeV-cm^2/mg
Converters in the first two columns use the flash architecture and the rest use the SAR conversion approach. ADC12062 was evaluated in FY97.
1. Two die solution; digital CMOS and analog bipolar.
2. Available through JPL only as overage from custom build.

Section 2.3

14-Bit Analog to Digital Converters Status

Part Information	**Manufacturer**	**Linear Tech**	**ADI/SEI**	**ADI**
	Part No.	LTC1419	7872	AD6644
	Process	CMOS	CMOS	Bipolar
	Power Supply	+5V, -5V	+5V, -5V	+5V
	Power Dissipation	150 mW	50 mW	(TBD)
	Conversion rate/time	800 ksps	10-10.5 us	65 Msps
	JPL Usage	None	MISR	None
	Availability	Yes	Yes	Development
Test Results	**Construction Analysis**	Passed	Passed	No Data
	Single Event Latchup	No Latchup, LET>100	No Latchup	No Data
	Total Ionizing Dose	No Data	4 krad (die) shielded in RAD-PAK®	No Data
	Reliability	No Data	Acceptable	No Data
	Other	N/A	N/A	N/A

Notes:
LET units = MeV-cm^2/mg
Converters in the first two columns use the SAR architecture. LTC1419 was evaluated in FY97.

Section 2.4

16-Bit Analog to Digital Converters Status

Part Information	**Manufacturer**	**Datel**	**Burr-Brown/SEI**
	Part No.	ADS937	SEI 7809 LPTRP
	Process	Hybrid	CMOS
	Power Supply	+5V, -5V, +15V, -15V	+5V
	Power Dissipation	1.1 W	150 mW
	Conversion rate/time	1 Msps	100 ksps
	JPL Usage	None	TES[1]
	Availability	Yes	Development
Test Results	**Construction Analysis**	Passed	Passed
	Single Event Latchup	LET<10	LET=19.9
	Total Ionizing Dose	25 krads (High dose rate)	10 krads
	Reliability	No Data	Planned
	Other	N/A	N/A

Notes:
LET units = MeV-cm^2/mg
The Datel part uses the flash architecture and the 7809 uses the SAR conversion approach. Both were evaluated in FY97.
1. Designed-in. A two die solution (A/D die and de-latch circuit as an ASIC die) is being worked.

24-Bit Analog to Digital Converters Status

Part Information	**Manufacturer**	**Harris**	**ADI**	**Burr-Brown**
	Part No.	HI7190	AD7714-5, AD7714-3	ADS 1210
	Process	CMOS	CMOS	CMOS
	Power Supply	+5V, -5V	+5V (-5), +3V (-3)	+5V
	Power Dissipation	15 mW	5 mW (-5), 2.6 mW (-3)	26 mW
	Conversion rate/time	Note 1	Note 1	Note 1
	JPL Usage	None	DS2 (?)	None
	Availability	Yes	Yes	Yes
Test Results	**Construction Analysis**	Passed	Passed	Passed
	Single Event Latchup	No Data	LET=55 for AD7714-3	No Data
	Total Ionizing Dose	No Data	No Data	No Data
	Reliability	No Data	No Data	No Data
	Other	N/A	N/A	N/A

Notes:

LET units = MeV-cm^2/mg

These converters use delta-sigma designs which feature the highest resolution and the lowest power. They were evaluated in FY97.

1. Consult vendor data sheet for information on effective resolution vs conversion rate and gain setting for a given clock frequency.

SECTION 3.0 PARTS DESCRIPTION

SECTION 3.0 Brief Description of Parts

The parts can be broken down into four distinct groups: high speed, low power; ultra high speed, low resolution; very high resolution, low power; and general purpose, low power A/Ds.

3.1 High-speed, low power A/Ds

3.1.1 Datel ADS 937 16-bit, 1MHz, 1.1W, hybrid A/D

Description: The ADS 937 is a 16-bit, 1MHz sampling A/D. It is built as a hybrid and contains a sample and hold amplifier, an internal reference, timing/control logic, and error correction circuitry. It accepts both bipolar (+/-5V) and unipolar (0-10V) analog inputs. It runs on +/-5V and +/-15V power supplies and typically draws 1.1watts. The device is available in both commercial and military grades.

Construction analysis: The engineering model part was found unacceptable, but the production part showed a very well designed hybrid device. See JPL FA log 6773 (D-15126).

Single Event Latch-up: Single event latch-up test was performed as a joint effort with the Aerospace Corp using their laser set-up. It should be noted that the correlation between the results obtained with the laser set-up and those obtained at Brookhaven National Laboratory (BNL) has not been conclusively established. The data taken on a couple of part types show good correlation but much more tests need to be run. Based on the results obtained at the Aerospace Corp, the LSI ASIC chip in the hybrid has a very low latch-up threshold. All other elements were found to have acceptably high thresholds. See JPL D-15128.

Total dose: High dose rate tests were performed with supplier collaboration. The parts were irradiated to 5krads, 10krads, 15krads, 25krads and 50 krads level. They failed functional test at 50krads. At 25krads level, a considerable parametric degradation was observed. The test results are being reviewed. See JPL D-15127.

Suggestions for improving radiation performance of the part: In order to improve the radiation performance of the ADS937 hybrid, JPL has made several suggestions to Datel. These mainly involve substituting known rad hard elements for the commercial ones currently used in the design.

3.1.2 Linear Technology LTC1419 14-bit 800ksps, 150mW CMOS A/D

Description: The LTC1419 is a 14-bit, 800ksps sampling A/D. It runs on +/-5V supplies and typically draws 150mW (7mW in nap mode, 10µW in sleep mode). It is available in 28-pin SO and SSOP packages. Two versions, 1419 and 1419A, are available with the 1419A being selected for tighter specs.

Construction analysis: The results were found acceptable. See JPL FA log 6756 (D-14755).

Single event latch-up: The part was found to have an SEU threshold of 16 MeV/mg/sq cm and showed no other anomalies upto LET=74 MeV/mg/sq cm. Provided that a system is noise tolerant or redundancy checking is incorporated in the system design, this device is acceptable for SEL. See JPL D-14755.

Total dose: Not performed. Supplier collaboration is being explored.

Die availability: yes

3.1.3 **ADI AD9871XE** 12-bit, 5Msps, 1W radiation-hardened BiCMOS A/D

Description: This is the radiation hardened version of AD871 12-bit 5 Msps monolithic A/D. It should be noted that the AD9871XE is not available as a standard product (ADI made a special run for JPL). Contact the author for details.

3.1.4 **NSC ADC12062** 12-bit, 1MHz, 75mW CMOS A/D

Description: Using an innovative multistep conversion technique, the 12-bit ADC12062 CMOS A/D digitizes signals at a 1MHz sampling rate while consuming a maximum of only 75mW on a single +5V supply. When the converter is not digitizing signals, it can be placed in the Standby mode; typical power consumption in this mode is 100µW. It is available in 44-pin plastic leaded chip carrier and plastic quad flat pack packages.

Single Event Latch-up: The part was found to have an LET of 12 MeV/mg/sq cm.

Construction Analysis and Total Dose Tests: Not done.

3.2 Ultra high speed, low resolution A/Ds

3.2.1 **Maxim MAX101** 8-bit 500Msps, 7.5W bipolar A/D

Description: The MAX101 is a 500Msps 8-bit A/D which allows accurate digitizing of analog signals from DC to 250MHz. Designed with Maxim's proprietary advanced bipolar processes, the MAX101 contains a high-performance T/H amplifier and two quantizers in an 84-pin ceramic flat pack. It operates on +5.0 V and –5.2V supplies and typically draws 7.5W power.

Construction Analysis: Passed. The device uses COB (chip-on-board) technology. See JPL FA log 6854.

Single Event Latch-up: Destructively failed SEL test. These results were totally unexpected.

Total Dose: Not done.

3.2.2 **Signal Processing Technologies SPT 7725** 8-bit 300Msps, 2.2W bipolar A/D

Description: The SPT7725 is a monolithic (ECL) 8-bit flash converter. It operates at 300 Msps conversion rate. A single –5.2V supply is required for operation. The typical power dissipation is 2.2W. The military version of the part is available in 42 lead ceramic side brazed DIP and 44 lead surface-mount cerquad packages.

Construction Analysis: Passed. The device employs three level interconnects. See JPL FA log 6855.

Single Event Latch-up: The part did not show latch-up. The LET is estimated to be >100 MeV/mg/sq cm.

Total Dose: High dose rate tests were run as a JPL/SPT joint effort. The testing was done at 20krads, 50krads and 100krads levels. No significant parametric shifts were observed.

3.2.3 **Harris HI1276** 8-bit 500Msps, 2.8W bipolar A/D

Description: The HI1276 is an 8-bit ultra high speed flash A/D capable of digitizing analog signals at a maximum rate of 500 Msps. It runs on a single –5.2V supply and typically draws 2.8W power. It is supplied in a 68 lead ceramic LCC package.

Single Event Latch-up: The part did not show latch-up. The LET is estimated to be >100 MeV/mg/sq cm.

Construction Analysis and Total Dose tests: Not done.

3.2.4 **Harris HS9008** 8-bit 20MHz, 400mW CMOS Rad Hard A/D

Description: The HS9008 is an 8-bit high speed flash A/D. It operates on a single 5V supply with a typical dissipation of 400mW. It is fabricated in Harris' AVLSI1RA process, which is dual level metal, twin well, thin epi, 1.25u junction isolated CMOS process. This process is single event latch up immune and its total dose hardness is specified to 300krads. It is available in a 28-pin package.

3.3 Very high resolution, low power (delta-sigma) A/Ds

3.3.1 **Harris HI7190** 24-bit, 15mW, CMOS A/D

Description: The HI7190 is a 24-bit delta-sigma converter which offers 22-bit resolution with no missing codes. It operates from +/-5V supplies and typically draws 15mW (5mW in the standby mode). The part is offered in 20 pin plastic DIP and SOIC packages.

Construction Analysis: Completed. Some side wall metal thinning was found in the metal-1 contact apertures to silicon and polysilicon, however, the Ti/W layer was found to be uniform. The samples analyzed were in SOIC package. See JPL FA log 6850 (D-15123).

Single Event Latch-up and Total Dose Tests: Not done.

3.3.2 **ADI AD7714-5** (24-bit, 5V), and **AD7714-3** (24-bit, 3V) <5mW CMOS A/Ds

Description: The AD7714 is a 24-bit delta-sigma converter. It operates from a single supply (+5V for AD7714-5, or +3V for AD7714-3). The typical power levels are: 5mW (100µW in standby mode) for the AD7714-5, and 2.6mW (15µW in standby mode) for the AD7714-3. It offers 24-bit resolution with no missing codes. The part comes in 24-pin (plastic DIP, hermetic DIP and SOIC) and 28-pin (SSOP) packages.

Construction Analysis**:** Completed on AD7714-3. No significant construction defects were found. The sample analyzed were in SOIC package. See JPL FA log 6852 (D-15124)**.**

Single Event Latch-up: Done on AD7714-3. LET=55 MeV/mg/sq cm.

Total Dose Test: On hold. We explored with ADI the feasibility of doing a joint test. But, this product is built at their Ireland facility and therefore, it deemed impractical to test.

3.3.3 **Burr-Brown ADS1210** 24-bit , 26mW CMOS A/D

Description: The ADS 1210 is a 24-bit delta-sigma converter which operates from a single +5V supply. It typically draws 26mW (11mW in the sleep mode). It offers 24-bit resolution with no missing codes. It is available in 18-pin DIP and SOIC packages. Note: The evaluation results would also apply to ADS1211 which includes a 4-channel MUX. The ADS1211 is available in 24-pin (DIP and SOIC) and 28-pin (SSOP) packages.

Construction Analysis: Completed. Considerable notching of the metal-2 aluminum interconnects was found, however, this is not cause for rejection. The samples analyzed were in SOIC package. See JPL FA log 6853 (D-15125).

Radiation Tests: Not done.

3.4 General purpose, low power A/Ds

3.4.1 **Maxim/SEI 7672** 12-bit, 5µs, 110mW A/D

Description: The Maxim 7672 is a 12-bit, 5us (version JPL procured), 110mW, BiCMOS A/D. It requires an external –5V reference. Analog input range is pin-selectable for 0 to +5V, 0 to +10V, or +/-5V.It operates with +5V and –12V supplies. The device has parallel (three-state) outputs. It does not have an on-chip sample and hold.

Role of SEI: JPL tests showed that Maxim part did not go into single event latch-up, however, the process was found to be hard to 10krads. In order to meet project requirement of 100krads total dose, Maxim die were packaged in a 24-pin RAD-PAK® flatpack (same pin-out as the standard Maxim part) at Space Electronics, Inc. (SEI). SEI did the screening and qualification per the JPL specification ST12075. The part is now available as a standard product (7672RP) from SEI.

Application Note: The part has been found to go into latch up under certain conditions. See JPL PIP No. 332 for details.

3.4.2 **Maxim MX674A** 12-bit, 15µs, 150mW A/D

Description: The Maxim MX674A is a complete 12-bit A/D, including a voltage reference, clock, parallel (three-state) outputs and a digital interface for microprocessor control. Successive approximation conversion is performed by a monolithic BiCMOS die housed in a 28-pin package. It operates on +5V and +/-12V to +/-15V power supplies, with typical dissipation of 150mW at +/-15V. It accepts +/-5V, +/-10V, 0 to +10V and 0 to +20V inputs.

JPL tests showed that this part did not go into single event latch-up. However, it has been found very soft as far as the total dose at low dose rates.

3.4.3 **Harris HI574A** 12-bit, 25µs, 515mW A/D

Description: The Harris HI-574A is a complete 12-bit A/D, including a voltage reference, clock, parallel (three-state) outputs and a digital interface for microprocessor control. Successive approximation conversion is performed by two monolithic dice (bipolar analog and CMOS digital) housed in a 28-pin ceramic sidebrazed DIP package. The bipolar analog die features the Harris Dielectric Isolation process, which provides enhanced AC performance and freedom from latch-up. It operates on +5V and +/-12V to +/-15V power supplies, with typical dissipation of 385mW at +/-12V (515mW typical at +/-15V). It accepts +/-5V, +/-10V, 0 to +10V and 0 to +20V inputs. The part is available as MIL-STD-883 compliant.

JPL tests showed that the part did not go into single event latch-up.

3.4.4 **ADI/SEI 7872** 14-bit, 10µs, 95mW A/D

Description: The Maxim 7672 is a 14-bit, 10µs, 95mW, BiCMOS A/D. It consist of on-chip clock, track and hold amplifier and voltage reference. Analog input range is +/- 3V. It operates with +/- 5V supplies. The device has serial output.

Role of SEI: JPL tests showed that the ADI part did not go into single event latch-up, however, the process was found to be soft for total dose. In order to meet the project requirement of 38krads total dose, the ADI die were packaged in a 16-pin RAD-PAK® flatpack (same pin-out as the standard ADI part) at Space Electronics, Inc. (SEI). SEI did the screening and qualification per the JPL specification ST12196. The part is now available as a standard product (7872RP) from SEI.

3.4.5 **Burr-Brown ADS7809** 16-bit, 100kHz, 100mW CMOS A/D (with Latch-up protection circuit)

Description: The ADS7809 is a complete 16-bit 100kHz sampling A/D using CMOS-epi process. It operates from a single +5V supply, with power dissipation under 100mW. The part offers six analog input ranges: +/-10V, +/-5V, +/-3.33V, 0 to 10V, 0 to 5V, and 0 to 4V. It has serial output. As noted in footnote 8/ of the previous section, the latch-up protection circuit is under development at SEI.

Construction Analysis: Completed at Space Electronics (SEI). Passed**.**
See JPL D-14759.
Single Event Latch-up: Completed. LET=19.9 MeV/mg/sq cm. See JPL D-14757.
Total Dose Test: Completed. 10krads. See JPL D-14758.

SECTION 4.0 RECOMMENDATIONS FOR FUTURE WORK

SECTION 4.0 Recommendations for Future Work

4.1 New Parts in Production (Will require funding for evaluation)

4.1.1 Datel ADS947 14-bit, 10 MHz, 2W, Hybrid A/D

One of the NASA centers is interested in evaluating this part.

Description: The ADS947 is a 14-bit, 10MHz sampling A/D. It contains a fast-settling sample and hold amplifier, a voltage reference, timing/control logic, and error-correction circuitry. Digital input and output levels are TTL. It only requires the rising edge of a start convert pulse to operate. Requiring only +5V and –5.2V supplies, the ADS-947 typically dissipates 2 Watts. The device is offered with a bipolar input range of +/-2V. It is available for use in either commercial (0ºC to +70ºC) or military (-55ºC to +125ºC) operating temperature ranges.

4.2 Parts in Development (Their progress would have to be monitored)

4.2.1 ADI AD6644 14-bit, 65Msps, A/D

Description: The AD6644 is a monolithic, single 5V supply, 65Msps, 14-bit A/D with an on-chip sample and hold amplifier and voltage reference. The power dissipation is yet to be specified. The AD6644 is built on Analog Devices high-speed complementary bipolar process (XFCB) and uses a multi-pass architecture. This manufacturing process is inherently radiation hard. Units are packaged in a 52-pin package. The part is in development.

4.2.2 ADI AD9225 12-bit, 25Msps, 300mW A/D

Description: The AD9225 is a monolithic, single 5V supply 12-bit, power scalable 25Msps A/D with an on-chip, high performance sample-and-hold amplifier and programmable voltage reference. An external reference can also be used. The output drivers can be operated from a separate 3V-5V supply if desired. The commercial part comes in a 28 pin package. ADI has plans to transfer this design to a radiation hard foundry to make it available to the space and military users.

4.2.3 Harris HS-5766 10-bit, 60Msps A/D

Description: The commercial version, HI5766, is a monolithic, 10-bit, 60Msps, 260mW A/D. It runs on a single +5V supply. The outputs are CMOS compatible and can be operated from a separate 3V or 5V supply. It comes in a 28-pin package. The goal with the radiation hardened version, HS5766, is to achieve 200krads total dose hardness. The process is latchup immune.

4.3 Others Promising Parts: (Will require funding for product development)

4.3.1 12-bit Rad Hard A/D from Sandia National Laboratory (SNL)
SNL feels it is feasible to fabricate a low power, 12-bit A/D that will tolerate 1Mrads.

4.3.2 Rad Hard, Low Power A/Ds in Silicon-On-Insulator (SOI) from Allied Signal

There are currently no commercially available A/Ds in SOI. The prospects of building SOI A/Ds with certain important features needed for upcoming JPL/NASA programs are discussed below:

4.3.2.1 8-bit Rad Hard, Low Power A/D. Allied Signal's cell library includes an A/D with the following characteristics: 8-bit resolution, 1.2u 2-layer metal SOI process, 5V operating voltage, 28µs conversion time, 10mW power dissipation. An 8-bit A/D product could be built by adding the customer defined I/O circuitry to the existing cell.

4.3.2.2 12-bit or 14-bit Rad Hard A/D. Allied can build a 12-bit, or even a 14-bit, A/D product in SOI with their existing process (without doing any R & D) provided an off-chip reference can be used. A suitable rad hard precision voltage reference could be chosen: Several of JPL projects have used Linear Tech's rad hard 5V reference, RH1021-5, which draws 1.5mA max. Actually, the voltage reference could be procured in the die form and packaged in the same package with the A/D die. Depending upon the user interest, the following variations of a 14-bit A/D (with 12-bit minimum performance over the specified conditions) could be pursued:

Without on-chip reference

> General purpose, mil temp range, low power (<250mW), rad hard (100krads) 100ksps A/D
> This should not require any R&D effort.
>
> Low power (<100mW), low temperature (-100ºC to +75ºC operating temp range for MARS), 100ksps A/D
> This would require an adjustment to their process.
>
> Low power (<100mW), 500ksps, rad hard (1Mrad to 4Mrad hardness for X2000), industrial temp range (-40ºC to +85ºC) A/D
> This would require a process adjustment.

With on-chip reference (R & D Effort)

> Work on developing a complete (with on-chip reference) general purpose, low power, rad hard 100ksps A/D

4.3.2.3 10-bit, High Speed, Low Power, Rad Hard ADC from Insyte. Insyte has designed an RHLP AD-1 with the following features: 8 single ended inputs, on-chip sample and hold, 10-bit parallel outputs (tri-state, cold spareable), single power supply with multiple (2V, 2.5V, 3.3V, 5V) options, operating power at 10µW/MHz, standby power less than 0.1µW, auto calibration for radiation induced Vt shifts, auto temperature compensation, pin configurable performance options: eight, 10MHz channels, or one, 80MHz channel.

END