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NOTICE OF
CHANGE

MIL-STD-2217(AS)
NOTICE 1
28 MAY 1993

MILITARY STANDARD
REQUIREMENTS FOR
MEMORY LOADER/VERIFIER MULTIPLEX BUS INTERFACE
WITH AVIONIC SYSTEMS

TO ALL HOLDERS OF MIL-STD-2217(AS)

1. The following pages of MIL-STD-2217(AS) have been revised and supersede
the pages listed.

NEW PAGE	DATE	SUPERSEDED PAGE	DATE
13	16 October 1991	13	Reprinted without change
14	28 May 1993	14	16 October 1991
15	28 May 1993	15	16 October 1991
16	16 October 1991	16	Reprinted without change
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165	28 May 1993	165	16 October 1991
166	16 October 1991	166	Reprinted without change
183	28 May 1993	183	16 October 1991
184	16 October 1991	184	Reprinted without change

2. RETAIN THIS NOTICE AND INSERT BEFORE TABLE OF CONTENTS.

3. Holders of MIL-STD-2217(AS) will verify that page changes and additions
indicated above have been entered. This notice page will be retained as a
check sheet. This issuance, together with appended pages, is a separate
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TABLE IV. Discrete Connector J2 Pin Designations
for Type II Interface Connection. - Continued

NUMERICAL ORDER		FUNCTIONAL ORDER	
PIN NO.	FUNCTION	FUNCTION	PIN NO.
40	IPL FAIL 4-	PWR OFF/ON 3	38
41	IPL 4-	PWR OFF/ON 3 REF GND	45
42	EW UDM REPROG EN	PWR OFF/ON 4	51
43	RESERVED	PWR OFF/ON 4 REF GND	55
44	CONFIG 2^1	REFERENCE GND	48
45	PWR OFF/ON 3 REF GND	RESERVED	21
46	SPARE	RESERVED	29
47	EXTERNAL PROCESSOR ON/OFF	RESERVED	36
48	REFERENCE GND	RESERVED	43
49	IPL 3+	SPARE	1
50	CONFIG 2^2	SPARE	9
51	PWR OFF/ON 4	SPARE	16
52	SPARE	SPARE	24
53	IPL 3-	SPARE	39
54	CONFIG 2^3	SPARE	46
55	PWR OFF/ON 4 REF GND	SPARE	52

TABLE V. Bus Connectors J3 and J4 Contact Designations
for Type II Interface Connection.

CONNECTOR/PIN NO.	FUNCTION
J3-A CENTER CONDUCTOR	PRIMARY AV BUS 1+
J3-A INNER SHIELD	PRIMARY AV BUS 1-
J3-A OUTER SHIELD	PRIMARY AV BUS 1 SHIELD
J3-B CENTER CONDUCTOR	EW BUS +
J3-B INNER SHIELD	EW BUS -
J3-B OUTER SHIELD	EW BUS SHIELD
J3-C CENTER CONDUCTOR	PRIMARY AV BUS 3+
J3-C INNER SHIELD	PRIMARY AV BUS 3-
J3-C OUTER SHIELD	PRIMARY AV BUS 3 SHIELD
J3-D CENTER CONDUCTOR	RESERVED
J3-D INNER SHIELD	RESERVED
J3-D OUTER SHIELD	RESERVED
J4-A CENTER CONDUCTOR	RESERVED
J4-A INNER SHIELD	RESERVED
J4-A OUTER SHIELD	RESERVED
J4-B CENTER CONDUCTOR	PRIMARY AV BUS 2+
J4-B INNER SHIELD	PRIMARY AV BUS 2-
J4-B OUTER SHIELD	PRIMARY AV BUS 2 SHIELD
J4-C CENTER CONDUCTOR	SPARE
J4-C INNER SHIELD	SPARE
J4-C OUTER SHIELD	SPARE
J4-D CENTER CONDUCTOR	PRIMARY AV BUS 4+
J4-D INNER SHIELD	PRIMARY AV BUS 4-
J4-D OUTER SHIELD	PRIMARY AV BUS 4 SHIELD

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TABLE VI. Redundant Bus Connector J5 Contact Designations
for Type II Interface Connection.

CONNECTOR/PIN NO.	FUNCTION
J5-A CENTER CONDUCTOR	SECONDARY AV BUS 1+
J5-A INNER SHIELD	SECONDARY AV BUS 1-
J5-A OUTER SHIELD	SECONDARY AV BUS 1 SHIELD
J5-B CENTER CONDUCTOR	SECONDARY AV BUS 2+
J5-B INNER SHIELD	SECONDARY AV BUS 2-
J5-B OUTER SHIELD	SECONDARY AV BUS 2 SHIELD
J5-C CENTER CONDUCTOR	SECONDARY AV BUS 3+
J5-C INNER SHIELD	SECONDARY AV BUS 3-
J5-C OUTER SHIELD	SECONDARY AV BUS 3 SHIELD
J5-D CENTER CONDUCTOR	SECONDARY AV BUS 4+
J5-D INNER SHIELD	SECONDARY AV BUS 4-
J5-D OUTER SHIELD	SECONDARY AV BUS 4 SHIELD

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5.1.2.3 <u>Optional Connections for Redundant Buses</u>. For those cases where all four of the primary bus connections are not utilized it is an option to connect the secondary side of the redundant bus(es) to the Primary Bus Connector, thus avoiding the need for the Redundant Bus Connector. When this option is utilized in the aircraft wiring, the MLV shall not be required to utilize the secondary connection for true redundant bus operation. When this option is utilized, the MLV whether acting as BC or RT will only switch one time from the primary connection to the secondary connection.

5.1.2.4 <u>Electrical Characteristics</u>. (Type I and Type II Interface Connections.)

Connector pins in each interface connection will provide for the following:

   a. Five sets of primary data bus lines (one EW and four Avionic Buses)

   b. Four sets of redundant data bus lines (four Avionic Buses)

   c. Two sets of Avionic (AV) reprogram enabling discretes

   d. Two Electronic Warfare (EW) reprogram enable discretes

   e. One set of Aircraft Identification pins (Aircraft Type and Aircraft Configuration Modification)

   f. AN/AYK-14 Discretes

       1. Four sets of AN/AYK-14 IPL (Initiate Program Load) lines
       2. Four sets of AN/AYK-14 IPL fail lines
       3. Four sets of AN/AYK-14 PWR OFF/ON lines

   g. One Set of Boot Enable Stores Management System (SMS)

   h. AN/ALQ-165 External Processor ON/OFF discrete

   i. One set of MLV reserved pins

   j. Five reserved pins for F/A-18 (Type I only)

   k. Associated ground pins and spare pins.

5.1.2.4.1 <u>Primary Data Bus Contacts</u>. Each of the five sets of data bus connections will consist of three contacts to accommodate a twisted pair plus a shield ground. The maximum line-to-line, peak-to-peak voltage at the connector will be 48 volts. The nominal operating current will be 200 milliamperes RMS per line.

5.1.2.4.2 <u>Redundant Data Bus Contacts</u>. Each of the four sets of data bus connections will consist of three contacts to accommodate a twisted pair plus a shield ground. These contacts shall conform to the electrical requirement specified for the Primary Data Bus Contacts (5.1.2.4.1). Use of the redundant buses and connector is optional.

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20.4.4.1.1 <u>Header Message Utilization</u>. This message is used to pass Load/ Verify parameters to the unit.

20.4.4.2 <u>Data Words</u>.

20.4.4.2.1 <u>Data Word 1</u>.

a. TM (bits 14-15). The Transfer Mode (TM) bits are used to describe the Memory Data Load or Memory Data Verify DATA WORD content. The TM bits are binary coded as follows:

   1. TM = 00 No transfer. In the No Transfer Mode the Buffer Transfer Count and Initial Load Address have no meaning. This mode is used to transfer the Program Entry Address and Page Number or is used as a preamble to the Trailer Message.

   2. TM = 01 8 bit transfer. Each 16 bits of data transmitted in a DATA WORD will contain only 8 bits of information in bits 0-7.

   3. TM = 10 16 bit transfer. Each 16 bits of data transmitted in a DATA WORD will contain 16 bits of information in bits 0-15.

   4. TM = 11 32 bits transfer. The 16 bits of data transmitted in each odd word (first is odd) contains the 16 MSBs of data in bits 0-15 and each even word (second is even) contains the 16 LSBs of data in bits 0-15.

b. HT (bits 12-13). The Header Type (HT) bits are used to describe the Header. The Header Type has no meaning when the Transfer Mode is 00. The HT bits are binary coded as follows:

   1. HT = 00 Normal Header. (Buffer Transfer Count equals number of words.)

   2. HT = 01 Normal Header. (Buffer Transfer Count equals number of messages.)

   3. HT = 10 Undefined.

   4. HT = 11 Reserved for internal MLV use. This type of Header will not be transmitted on the bus.

c. Buffer Transfer Count (bits 0-11). The Buffer Transfer Count is used to indicate the amount of data that will follow the Header Message. The Buffer Transfer Count has no meaning when the Transfer Mode is 00. The range of the Buffer Transfer Count is 1 to 4096 (value of 0 = 4096).

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1. For HT = 00, the Buffer Transfer Count is the total number of DATA WORDS that will be transmitted after the Header. The DATA WORDS will be transmitted in 32-word messages with the last message containing 1 to 32 DATA WORDS. The maximum transfer for HT = 00 is 4096 words using 128 Memory Data Load or Memory Data Verify Messages.

2. For HT = 01, the Buffer Transfer Count is the number of Memory Data Load or Memory Data Verify messages that will follow the HEADER. Thus, the maximum data transfer per Header Message is 4096 x 32 DATA WORDS (per Memory Data Load or Memory Data Verify Message) which equals 131,072 16 bit words (128K). If paging is utilized for transfer modes 01 or 10 (see 20.4.4.2.4), the maximum value of the Buffer Count will be 2048. (Yields 65,536 16 bit data words (64K) for transfer modes 01 and 10 using paging.)

20.4.4.2.2 Data Word 2.

a. Initial Load Address (bits 0-15). The Initial Load Address is the 16 or less LSB of the point in memory into which data is to be loaded or read. The maximum value (number of bits) used in the Initial Load Address will be compatible with the page size of units using paging. Unused bits shall equal 0.

20.4.4.2.3 Data Word 3.

a. Program Entry Address (bits 0-15). The Program Entry Address has meaning only for Transfer Mode = 00. The Program Entry Address is the 16 or less LSB of the point in memory at which the unit being reprogrammed is to begin execution after receipt of the Execute command in the Reprogram Control Message (only used for units requiring this command) or when a Transfer Control is indicated in DATA WORD 4. The maximum value (number of bits) used in the Program Entry Address will be compatible with the page size of units using paging. Unused bits shall equal 0.

20.4.4.2.4 Data Word 4.

a. Page Number (bits 3-15). The Page Number represents up to 13 MSB bits for paged memory address. The Page Number applies to the Program Entry Address for Transfer Mode = 00. The Page Number applies to the Initial Load Address for Transfer Mode = 01, 10, or 11. Unused bits shall equal 0.

b. TC bits (0-1). The Transfer Control (TC) may be used to transfer control to the loaded program after a verify or to an unaltered memory area after a load.

1. Transfer Control = 00 indicates this is the last HEADER, MEMORY DATA, ..., MEMORY DATA, TRAILER or HEADER, TRAILER transaction.

30.4.4.1.1 <u>Header Message Utilization</u>. This message is used to pass Load/ Verify parameters to the unit.

30.4.4.2 <u>Data Words</u>.

30.4.4.2.1 <u>Data Word 1</u>.

a. TM (bits 14-15). The Transfer Mode (TM) bits are used to describe the Memory Data Load or Memory Data Verify DATA WORD content. The TM bits are binary coded as follows:

  1. TM = 00 No transfer. In the No Transfer Mode the Buffer Transfer Count and Initial Load Address have no meaning. This mode is used to transfer the Program Entry Address and Page Number or is used as a preamble to the Trailer Message.

  2. TM = 01 8 bit transfer. Each 16 bits of data transmitted in a DATA WORD will contain only 8 bits of information in bits 0-7.

  3. TM = 10 16 bit transfer. Each 16 bits of data transmitted in a DATA WORD will contain 16 bits of information in bits 0-15.

  4. TM = 11 32 bits transfer. The 16 bits of data transmitted in each odd word (first is odd) contains the 16 MSBs of data in bits 0-15 and each even word (second is even) contains the 16 LSBs of data in bits 0-15.

b. HT (bits 12-13). The Header Type (HT) bits are used to describe the Header. The Header Type has no meaning when the Transfer Mode is 00. The HT bits are binary coded as follows:

  1. HT = 00 Normal Header. (Buffer Transfer Count equals number of words.)

  2. HT = 01 Normal Header. (Buffer Transfer Count equals number of messages.)

  3. HT = 10 Undefined.

  4. HT = 11 Reserved for internal MLV use. This type of Header will not be transmitted on the bus.

c. Buffer Transfer Count (bits 0-11). The Buffer Transfer Count is used to indicate the amount of data that will follow the Header Message. The Buffer Transfer Count has no meaning when the Transfer Mode is 00. The range of the Buffer Transfer Count is 1 to 4096 (value of 0 = 4096).

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1. For HT = 00, the Buffer Transfer Count is the total number of DATA WORDS that will be transmitted after the Header. The DATA WORDS will be transmitted in 32-word messages with the last message containing 1 to 32 DATA WORDS. The maximum transfer for HT = 00 is 4096 words using 128 Memory Data Load or Memory Data Verify Messages.

2. For HT = 01, the Buffer Transfer Count is the number of Memory Data Load or Memory Data Verify messages that will follow the HEADER. Thus, the maximum data transfer per Header Message is 4096 x 32 DATA WORDS (per Memory Data Load or Memory Data Verify message) which equals 131,072 16 bit words (128K). If paging is utilized for transfer modes 01 or 10 (see 30.4.4.2.4), the maximum value of the Transfer Buffer Count will be 2048. (Yields 65,536 16 bit data words (64K) for transfer modes 01 and 10 using paging.)

30.4.4.2.2 Data Word 2.

a. Initial Load Address (bits 0-15). The Initial Load Address is the 16 or less LSB of the point in memory into which data is to be loaded or read. The maximum value (number of bits) used in the Initial Load Address will be compatible with the page size of units using paging. Unused bits shall equal 0.

30.4.4.2.3 Data Word 3.

a. Program Entry Address (bits 0-15). The Program Entry Address has meaning only for Transfer Mode = 00. The Program Entry Address is the 16 or less LSB of the point in memory at which the unit being reprogrammed is to begin execution after receipt of the Execute command in the Reprogram Control Message (only used for units requiring this command) or when a Transfer Control is indicated in DATA WORD 4. The maximum value (number of bits) used in the Program Entry Address will be compatible with the page size of units using paging. Unused bits shall equal 0.

30.4.4.2.4 Data Word 4.

a. Page Number (bits 3-15). The Page Number represents up to 13 MSBs for page memory address. The Page Number applies to the Program Entry Address for Transfer Mode = 00. The Page Number applies to the Initial Load Address for Transfer Mode = 01, 10, or 11. Unused bits shall equal 0.

b. TC bits (0-1). The Transfer Control (TC) may be used to transfer control to the loaded program after a verify or to an unaltered memory area after a load.

1. Transfer Control = 00 indicates this is the last HEADER, MEMORY DATA, ..., MEMORY DATA, TRAILER or HEADER, TRAILER transaction.

40.4.5.1.1 <u>Header Message Utilization</u>. This message is used to pass Load/ Verify parameters to the unit.

40.4.5.2 <u>Data Words</u>.

40.4.5.2.1 <u>Data Word 1</u>.

    a. TM (bits 14-15). The Transfer Mode (TM) bits are used to describe the Memory Data Load or Memory Data Verify DATA WORD content. The TM bits are binary coded as follows:

        1. TM = 00 No transfer. In the No Transfer Mode the Buffer Transfer Count and Initial Load Address have no meaning. This mode is used to transfer the Program Entry Address and Page Number or is used as a preamble to the Trailer Message.

        2. TM = 01 8 bit transfer. Each 16 bits of data transmitted in a DATA WORD will contain only 8 bits of information in bits 0-7.

        3. TM = 10 16 bit transfer. Each 16 bits of data transmitted in a DATA WORD will contain 16 bits of information in bits 0-15.

        4. TM = 11 32 bits transfer. The 16 bits of data transmitted in each odd word (first is odd) contains the 16 MSBs of data in bits 0-15 and each even word (second is even) contains the 16 LSBs of data in bits 0-15.

    b. Buffer Transfer Count (bits 0-11). The Buffer Transfer Count is used to indicate the amount of data that will follow the Header Message. The Buffer Transfer Count has no meaning when the Transfer Mode is 00. The range of the Buffer Transfer Count is 1 to 4096 (value of zero equals 4096). The Buffer Transfer Count is the total number of DATA WORDS that will be transmitted after the Header. The DATA WORDS will be transmitted in 32-word messages with the last message containing the remaining 32 or less words. The maximum transfer is 4096 words using 128 Memory Data Load Messages.

    c. Other bits. Bits 12 and 13 shall be zero.

40.4.5.2.2 <u>Data Word 2</u>.

    a. Initial Load Address (bits 0-15). The Initial Load Address is the 16 or less LSB of the point in memory into which data is to be loaded. The maximum value (number of bits) used in the Initial Load Address will be compatible with the page size of units using paging. Unused bits shall be set to zero.

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40.4.5.2.3 <u>Data Word 3.</u>

a. Program Entry Address (bits 0-15). The Program Entry Address has meaning only for Transfer Mode = 00. The Program Entry Address is the 16 or less LSB of the point in memory at which the unit being reprogrammed is to begin execution. The maximum value (number of bits) used in the Program Entry Address will be compatible with the page size of units using paging. Unused bits shall equal zero.

40.4.5.2.4 <u>Data Word 4.</u>

a. Page Number (bits 3-15). The Page Number represents up to 13 MSBs for page memory address. The Page Number applies to the Program Entry Address for Transfer Mode = 00. The Page Number applies to the Initial Load Address for Transfer Mode 10 and 11. Unused bits shall equal zero.

b. TC bits (bit 0-1). The Transfer Control (TC) may be used to transfer control to the program loaded after reprogramming.

1. Transfer Control = 00 indicates this is the last HEADER, MEMORY DATA, ..., MEMORY DATA, TRAILER or HEADER, TRAILER transaction.

2. Transfer Control = 01 indicates that more data is to follow the current HEADER, MEMORY DATA, ..., MEMORY DATA, TRAILER or HEADER, TRAILER transaction and control should not be transferred. For units using paging and the Program Entry Address, the TC will remain = 01, even for the last data transaction, until a Transfer Mode = 00 message is used to supply the Program Entry Address and Page Number.

3. Transfer Control = 10 shall indicate that control is to be transferred to the Program Entry Address. When control is transferred, the action shall not take place until after the Trailer Message and shall transfer control only to non-reprogrammed areas or verified areas.

4. Transfer Control = 11 is invalid.

c. Other Bits (bit 2). Bit 2 shall equal 0.

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50.4.4.1.1 **Header Message Utilization**. This message is used to pass Load/ Verify parameters to the unit.

50.4.4.2 **Data Words**.

50.4.4.2.1 **Data Word 1**.

a. TM (bits 14-15). The Transfer Mode (TM) bits are used to describe the Memory Data Load or Memory Data Verify DATA WORD content. The TM bits are binary coded as follows:

1. TM = 00 No transfer. In the No Transfer Mode the Buffer Transfer Count and Initial Load Address have no meaning. This mode is used to transfer the Program Entry Address and Page Number or is used as a preamble to the Trailer Message.

2. TM = 01 8 bit transfer. Each 16 bits of data transmitted in a DATA WORD will contain only 8 bits of information in bits 0-7.

3. TM = 10 16 bit transfer. Each 16 bits of data transmitted in a DATA WORD will contain 16 bits of information in bits 0-15.

4. TM = 11 32 bits transfer. The 16 bits of data transmitted in each odd word (first is odd) contains the 16 MSBs of data in bits 0-15 and each even word (second is even) contains the 16 LSBs of data in bits 0-15.

b. Buffer Transfer Count (bits 0-11). The Buffer Transfer Count is used to indicate the amount of data that will follow the Header Message. The Buffer Transfer Count has no meaning when the Transfer Mode is 00. The range of the Buffer Transfer Count is 1 to 4096 (value of zero equals 4096). The Buffer Transfer Count is the total number of DATA WORDS that will be transmitted after the Header. The DATA WORDS will be transmitted in 32-word messages with the last message containing the remaining 32 or less words. The maximum transfer is 4096 words using 128 Memory Data Load Messages.

c. Other bits. Bits 12 and 13 shall be zero.

40.4.5.2.2 **Data Word 2**.

a. Initial Load Address (bits 0-15). The Initial Load Address is the 16 or less LSB of the point in memory into which data is to be loaded. The maximum value (number of bits) used in the Initial Load Address will be compatible with the page size of units using paging. Unused bits shall be set to zero.

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50.4.4.2.3 Data Word 3.

   a. Program Entry Address (bits 0-15). The Program Entry Address has meaning only for Transfer Mode = 00. The Program Entry Address is the 16 or less LSB of the point in memory at which the unit being reprogrammed is to begin execution. The maximum value (number of bits) used in the Program Entry Address will be compatible with the page size of units using paging. Unused bits shall equal zero.

50.4.4.2.4 Data Word 4.

   a. Page Number (bits 3-15). The Page Number represents up to 13 MSBs for page memory address. The Page Number applies to the Program Entry Address for Transfer Mode = 00. The Page Number applies to the Initial Load Address for Transfer Mode 10 and 11. Unused bits shall equal zero.

   b. TC bit (bit 0). The Transfer Control bit may be used to transfer control to the program loaded after a Memory Load.

      1. TC = 0   Indicates this is the last HEADER, MEMORY DATA, ..., MEMORY DATA, TRAILER or HEADER, TRAILER transaction.

      2. TC = 1   Indicates that more data is to follow the current HEADER, MEMORY DATA, ..., MEMORY DATA, TRAILER or HEADER, TRAILER transaction and control should not be transferred. For units using paging and the Program Entry Address, the TC will remain equal to one, even for the last data transaction, until a Transfer Mode = 00 message is used to supply the Program Entry Address and Page Number.

   c. Other bits. Bits 1-2 shall be zero.

The only time the MLV will check the Success bit in the Status Message before the Header Message is in the case of multiple transactions during a load where the Status Message occurs between a Trailer Message and the next Header Message. If a transaction is retried because of an error, the MLV will send the Header Message without first sending another Status Message.

60.4.4.1.1 <u>Header Message Utilization</u>. This message is used to pass Load/ Verify parameters to the unit.

60.4.4.2 <u>Data Words</u>.

60.4.4.2.1 <u>Data Word 1</u>.

    a. TM (bits 14-15). The Transfer Mode (TM) bits are used to describe the Memory Data Load or Memory Data Verify DATA WORD content. The TM bits are binary coded as follows:

        1. TM = 00 No transfer. In the No Transfer Mode the Buffer Transfer Count and Initial Load Address have no meaning. This mode is used to transfer the Program Entry Address and Page Number or is used as a preamble to the Trailer Message.

        2. TM = 01 8 bit transfer. Each 16 bits of data transmitted in a DATA WORD will contain only 8 bits of information in bits 0-7.

        3. TM = 10 16 bit transfer. Each 16 bits of data transmitted in a DATA WORD will contain 16 bits of information in bits 0-15.

        4. TM = 11 32 bits transfer. The 16 bits of data transmitted in each odd word (first is odd) contains the 16 MSBs of data in bits 0-15 and each even word (second is even) contains the 16 LSBs of data in bits 0-15. Not used with the SMS or the SDC.

    b. RT (bits 12-13). The Record Type (RT) bits are defined to describe the meaning of the Header Message. The only value transmitted by the MLV shall be 00. Record Types other than 00 are defined only for other than MLV use and are not addressed in this standard.

    c. Buffer Transfer Count (bits 0-11). The Buffer Transfer Count is used to indicate the amount of data that will follow the Header Message. The Buffer Transfer Count has no meaning when the Transfer Mode is 00. The Buffer Transfer Count is the total number of DATA WORDS that will be transmitted after the Header Message. The DATA WORDS will be transmitted in 32-word messages with the last message containing the remaining 32 or less words. For the SDC, the range of the Buffer Transfer Count is 1-1024 (value of zero equals 1024 and bits 10 and 11 are always zero). The maximum transfer for the SDC is done with 32 messages of 32 words each. For the AYQ-9 or

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AYQ-15 SMS, a Buffer Transfer Count of zero is invalid unless
TM = 00. For the EEPROM version of the AYQ-9 or AYQ-15, the range
of the Buffer Transfer Count is 1-1024, with the maximum transfer
using 32 messages of 32 words each. For the core memory version of
AYQ-9, the range of the Buffer Transfer Count is 1-4095 with the
maximum transfer using 127 messages of 32 words each and one 31 word
message.

60.4.4.2.2 Data Word 2.

a. Initial Load Address (bits 0-15). The Initial Load Address is the
16 or less LSB of the point in memory into which data is to be
loaded. (When required, MSB information is provided in the Page
Register Content field of DATA WORD 4.) The maximum value (number
of bits) used in the Initial Load Address will be compatible with
the page size of units using paging. Unused bits shall be set to
zero. The Initial Load Address has no meaning for TM = 00. For the
SDC, the physical memory that the Initial Load Address applies to
shall be as indicated by the MS bit in DATA WORD 4.

60.4.4.2.3 Data Word 3.

a. Program Entry Address (bits 0-15). The Program Entry Address has
meaning only for Transfer Mode = 00. The Program Entry Address is
the 16 or less LSB of the point in memory at which the unit being
reprogrammed is to begin execution. (When required, MSB information
is provided in the Page Register Content field of DATA WORD 4.) The
maximum value (number of bits) used in the Program Entry Address
will be compatible with the page size of units using paging. Unused
bits shall equal zero.

60.4.4.2.4 Data Word 4.

a. MS (bit 11). For the AYQ-9 or AYQ-15 SMS, the MS bit will always be
zero. For the SDC, the Memory Select (MS) bit indicates that the
SDC Input Output Memory (MS = 1) or the SDC Main Memory (MS = 0) is
the selected memory area. When Input Output Memory is selected, the
Initial Load Address in DATA WORD 2 shall be an absolute address in
Input Output Memory.

b. Page Register Content (bits 3-10). The Page Register Content repre-
sents up to 8 MSBs for page memory addressing. The Page Register
Content applies to the Program Entry Address for Transfer Mode = 00.
The Page Register Content applies to the Initial Load Address for
Transfer Mode 10. For the SDC, the Page Register Content has no
meaning when Input Output Memory is selected by MS = 1. The AYQ-9
or AYQ-15 SMS only uses bits 3 to 6 to indicate 4 MSBs for memory
addressing. The Page Register Content may also be used to provide
the data to be loaded into the register(s) pointed to by the Initial
Page Register in DATA WORD 1 of the Trailer Message. Unused bits
shall equal zero.

70.4.4.1.1 <u>Header Message Utilization</u>. This message is used to pass Load/
Verify parameters to the unit.

70.4.4.2 <u>Data Words</u>.

70.4.4.2.1 <u>Data Word 1</u>.

   a. TM (bits 14-15). The Transfer Mode (TM) bits are used to describe the
      Memory Data Load or Memory Data Verify DATA WORD content. The TM bits
      are binary coded as follows:

      1. TM = 00 No transfer. In the No Transfer Mode the Buffer Transfer
               Count and Initial Load Address have no meaning. This mode
               is used to transfer the Program Entry Address and Page
               Number or is used as a preamble to the Trailer Message.

      2. TM = 01 Not used. An AYK-14 IPL fails will occur and processor
               will hang if this code were used.

      3. TM = 10 16 bit transfer. Each 16 bits of data transmitted in a
               DATA WORD will contain 16 bits of information in bits 0-15.

      4. TM = 11 32 bits transfer. The 16 bits of data transmitted in each
               odd word (first is odd) contains the 16 MSBs of data in
               bits 0-15 and each even word (second is even) contains the
               16 LSBs of data in bits 0-15.

   b. Buffer Transfer Count (bits 0-11). The Buffer Transfer Count is used
      to indicate the amount of data that will follow the Header Message.
      The Buffer Transfer Count has no meaning when the Transfer Mode is 00.
      The range of the Buffer Transfer Count is 1 to 4096 (value of zero
      equals 4096). The Buffer Transfer Count is the total number of DATA
      WORDS that will be transmitted after the Header. The DATA WORDS will
      be transmitted in 32-word messages with the last message containing the
      remaining 32 or less words. The maximum transfer is 4096 words using
      128 Memory Data Load Messages.

   c. Other bits. Bits 12 and 13 shall be zero.

70.4.4.2.2 <u>Data Word 2</u>.

   a. Initial Load Address (bits 0-15). The Initial Load Address is the 16
      or less LSB of the point in memory into which data is to be loaded.
      The maximum value (number of bits) used in the Initial Load Address
      will be compatible with the page size of units using paging. Unused
      bits shall be set to zero.

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70.4.4.2.3 Data Word 3.

a. Program Entry Address (bits 0-15). The Program Entry Address has meaning only for Transfer Mode = 00. The Program Entry Address is the 16 or less LSB of the point in memory at which the unit being reprogrammed is to begin execution. The maximum value (number of bits) used in the Program Entry Address will be compatible with the page size of units using paging. Unused bits shall equal zero.

70.4.4.2.4 Data Word 4.

a. Page Number (bits 3-15). The Page Number represents up to 13 MSBs for page memory address. The Page Number applies to the Program Entry Address for Transfer Mode = 00. The Page Number applies to the Initial Load Address for Transfer Mode 10 and 11. Unused bits shall equal zero.

b. TC bit (bit 0). The Transfer Control bit may be used to transfer control to the program loaded after a memory load.

   1. TC = 0   Indicates this is the last HEADER, MEMORY DATA, ..., MEMORY DATA, TRAILER or HEADER, TRAILER transaction.

   2. TC = 1   Indicates that more data is to follow the current HEADER, MEMORY DATA, ..., MEMORY, DATA, TRAILER or HEADER, TRAILER transaction and control should not be transferred. For units using paging and the Program Entry Address, the TC will remain equal to one, even for the last data transaction, until a Transfer Mode = 00 message is used to supply the Program Entry Address and Page Number.

c. Other bits. Bits 1-2 shall be zero.