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MIL-STD-2217(AS)
16 OCTOBER 1991

DEPARTMENT OF DEFENSE

INTERFACE STANDARD

MEMORY LOADER/VERIFIER MULTIPLEX BUS INTERFACE WITH AVIONIC SYSTEMS

AMSC N/A AREA GDRQ

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DEPARTMENT OF DEFENSE

Washington, D.C. 20402

Requirements for Memory Loader/Verifier Multiplex Bus Interface with Avionic Systems

MIL-STD-2217

1. This military standard is approved for use by all Departments and Agencies of the Department of Defense.

2. Beneficial comments (recommendations, additions, deletions) and any pertinent data which may be of use in improving this document should be addressed to: Naval Air Development Center Code 5021, Warminster, PA 18974-5000, by using the self-addressed Standardization Document Improvement Proposal (DD Form 1426) appearing at the end of this document or by letter.

FORWARD

This standard contains requirements establishing the technical characteristics of the common interface between the AN/ASM-( ) Memory Loader/Verifier (MLV) and avionic subsystems aboard military aircraft.

It defines the interface for all newly developed/modified equipment that utilize the MIL-STD-1553 multiplex bus for reprogramming. This standard does not address any revision to MLV operation with equipment currently reprogrammed via an MLV. Modifications of existing MLVs to incorporate the provisions of this standard will be performed in such a manner as to retain the applicable existing capabilities.

For completeness this standard documents the protocol of the MIL-STD-1553 loading techniques currently in fleet use and makes provisions for adaptation of the common interface to the existing interface.

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Appendix C - Continued.

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Appendix H - Continued.

1. SCOPE

1.1 Scope. The Memory Loader/Verifier (MLV) will provide the means for loading and verifying avionics memories in military aircraft utilizing a multiplex bus interface.

New or modified memory data will first be processed by designated facilities for each avionic system. It will then be transmitted to each user and transferred to the MLV Memory Storage Device (MSD) at the Intermediate Maintenance Activity (IMA). The MSD in each MLV will then contain a completely updated record of all memory data to be loaded into the avionic memories.

The MLV, using the interfaces defined herein, will be utilized to reprogram all applicable systems aboard an aircraft at the organizational maintenance level (O-Level). It will load the new data into the memories of the appropriate avionics systems and verify that the memories have been correctly loaded where possible.

1.2 Interfacing Aircraft. Two types (Type I and Type II) of aircraft interface connections are called out in this document. The two types are defined in order to allow for compliance with contractual requirements and physical constraints that differ between aircraft. The Type I interface is defined to accommodate the physical constraints of existing aircraft and if within contractual constraints may be used for all existing aircraft. The Type II interface shall be used for all new designs and may be used for any existing aircraft. Individual Interface Control Documents (ICD) for each aircraft will define user definable items such as specific bus connections. These ICDs shall not repeat items specified herein.

1.3 Interfacing Systems. This standard shall be used for the development of MLV interfaces for all avionic equipment to be reprogrammed via MIL-STD-1553 type bus interfaces. Individual Interface Control Documents (ICDs) for each unit, to specify user definable items described herein, will be required to allow Memory Storage Device preparation. These ICDs shall comply with this document and shall not repeat items specified herein.

1.4 Applicability. This standard is applicable to all equipment reprogrammable at "O" level via a MIL-STD-1553 multiplex data bus and all new aircraft or aircraft modified to incorporate avionic equipment in conformance to this standard. All new equipment designs designated as Remote Terminals shall utilize the protocol defined in Appendix B of this document. All new equipment designs designated as Bus Controller shall utilize the protocol of Appendix C of this standard until the MLV is allocated the Bus Controller function and then shall utilize the protocol of Appendix B of this document. Equipment previously designed for which reprogramming capability is being added shall utilize the protocol of Appendix B or C of this document. Only equipment that is currently reprogrammable in the fleet via a MIL-STD-1553 multiplex data bus (or modifications to those equipments) shall utilize the protocol of Appendices D, E, F, G or H. All reprogrammable equipment not committed to production prior to the date of this document shall use at least one reprogramming enable discrete.

2. REFERENCED DOCUMENTS

2.1 Government Documents.

2.1.1 Specifications, Standards and Handbooks. Unless otherwise specified, the following specifications, standards and handbooks of the issue listed in that issue of the Department of Defense Index of Specifications and Standards (DoDISS) specified in the solicitation form a part of this standard to the extent specified herein.

SPECIFICATIONS

NAVAL AVIONICS CENTER (NAC)

1097A50101A	Program Performance Specification Advanced Bootstrap Loader for AN/AYK-14(V) Single Card Processor. 13 June 1985.
1097A50103A	User's Manual Advanced Bootstrap Loader for AN/AYK-14(V) Single Card Processor. 13 June 1985.

STANDARDS

FEDERAL

FED-STD-1020	Telecommunications: Electrical Characteristics of Balanced Voltage, Digital, Interface Circuits (RS-422)

MILITARY

MIL-STD-461	Electromagnetic Interference Characteristics, Requirements for Equipment
MIL-STD-704	Aircraft Electrical Power Characteristics
MIL-STD-1553	Aircraft Internal Time Division Command/Response Data Bus

2.1.2 Other Government Documents, Drawings and Publications. The following other Government documents, drawings and publications form a part of this standard to the extent specified herein.

DRAWINGS

NAVAIRDEVCEN (Code 80206)	Drawing No. SK302-850001, Type I Memory Loader/ Verifier Aircraft Interface
	Drawing No. SK302-850002, Type II Memory Loader/ Verifier Aircraft Interface

2.2 Other Publications. The following documents form a part of this standard to the extent specified herein. Unless specified, the issues of the documents which are DoD adopted shall be those listed in the issue of the DoDISS specified in the solicitation. The issue of documents which have not been adopted shall be those in effect on the date of the cited DoDISS.

SPECIFICATIONS

MCDONNELL AIRCRAFT COMPANY

MDC A3818 (Revision B) (15 March 1976) F-18 Avionics Multiplex Design Specification

2.3 Availability of Documents. Copies of specifications, standards and drawings required by manufacturers in connection with specific acquisitions should be obtained from the procuring activity.

2.4 Order of Precedence. In the event of conflict, this standard shall take precedence over the referenced documents and over the specifications of interfacing systems (i.e., AN/ASM-( ) and the applicable avionic systems).

3. DEFINITIONS

3.1 Asynchronous. For the purpose of this document, asynchronous bus operation means an independent clock source at each remote terminal which is utilized for the transmission of messages. The received message shall be decoded using clock information derived from the received signal.

3.2 Bit. Contraction of binary digit; it has a value of either zero or one. In information theory, a binary digit is equal to one binary decision or the designation of one of two possible values or states used to store or convey information.

3.3 Bit Rate. The number of bits transmitted per second, assuming continual bit transmission.

3.4 Bootstrap Loading. A method of loading in which the device being loaded controls the loading process.

3.5 Bus Controller (BC). Each multiplex bus will have one Bus Controller operating on each data bus at any one time. The controller establishes communications on the data bus by scheduling all messages.

3.6 Command/Response Mode. The operation of a multi-terminal data communication system in which the Remote Terminal (RT) will respond only when commanded by the Bus Controller (BC).

3.7 Data Bus. Whenever a data bus or bus is referred to in this document, it shall imply a twisted pair shielded cable.

3.8 Message. A time sequential transmission of words on a data bus. A message transfer is complete when the command word, data word(s) and the status word have been transmitted.

3.9 Modified Dynamic Bus Allocation. Modified dynamic bus allocation is the reassignment of the bus control function from a primary Bus Controller (BC) to a second BC using a hardwired discrete and/or multiplex bus messages.

3.10 Pulse Code Modulation. The form of modulation in which the modulation signal is sampled, quantized and coded so that information consists of a train of pulses and spaces.

3.11 Remote Terminal (RT). The electronics necessary to interface a multiplex bus with a subsystem and the subsystem with the bus. These electronics shall exist as an integral part of a Weapons Replaceable Assembly (WRA) associated with a subsystem and not as a separate WRA.

3.12 Time Division Multiplexing. The transmission of samples of information from several signal channels through one communication system with different channel sample times sequenced to form a composite signal that can be transmitted over the single communication channel.

3.13 Word. In the multiplex buses, a word is a sequence of a three bit time sync signal, 16 data bits, and a parity bit. There are three types of data bus words: command, status and data.

4. GENERAL REQUIREMENTS

4.1 Application. This standard defines the interface between the MLV, exterior to the aircraft, with the electrical power system and the avionic subsystems, interior to the aircraft. The portable MLV will be connected to the aircraft with electrical cables which will be approximately ten feet long. Two different connector/cable interface connections are provided between the MLV and the aircraft and are designated Type I and Type II.

4.2 Characteristics.

4.2.1 Type I Characteristics. The Type I interface connection consists of a power connector, a bus and discrete signal connector, and an optional redundant bus connector. This interface is shown in Figure 1.

4.2.2 Type II Characteristics. The Type II interface connection consists of a power connector, a discrete signal connector, and three bus connectors that contain triaxial connector feed throughs for increased shielding. The third bus connector is an optional redundant bus connector. This interface is shown in Figure 2.

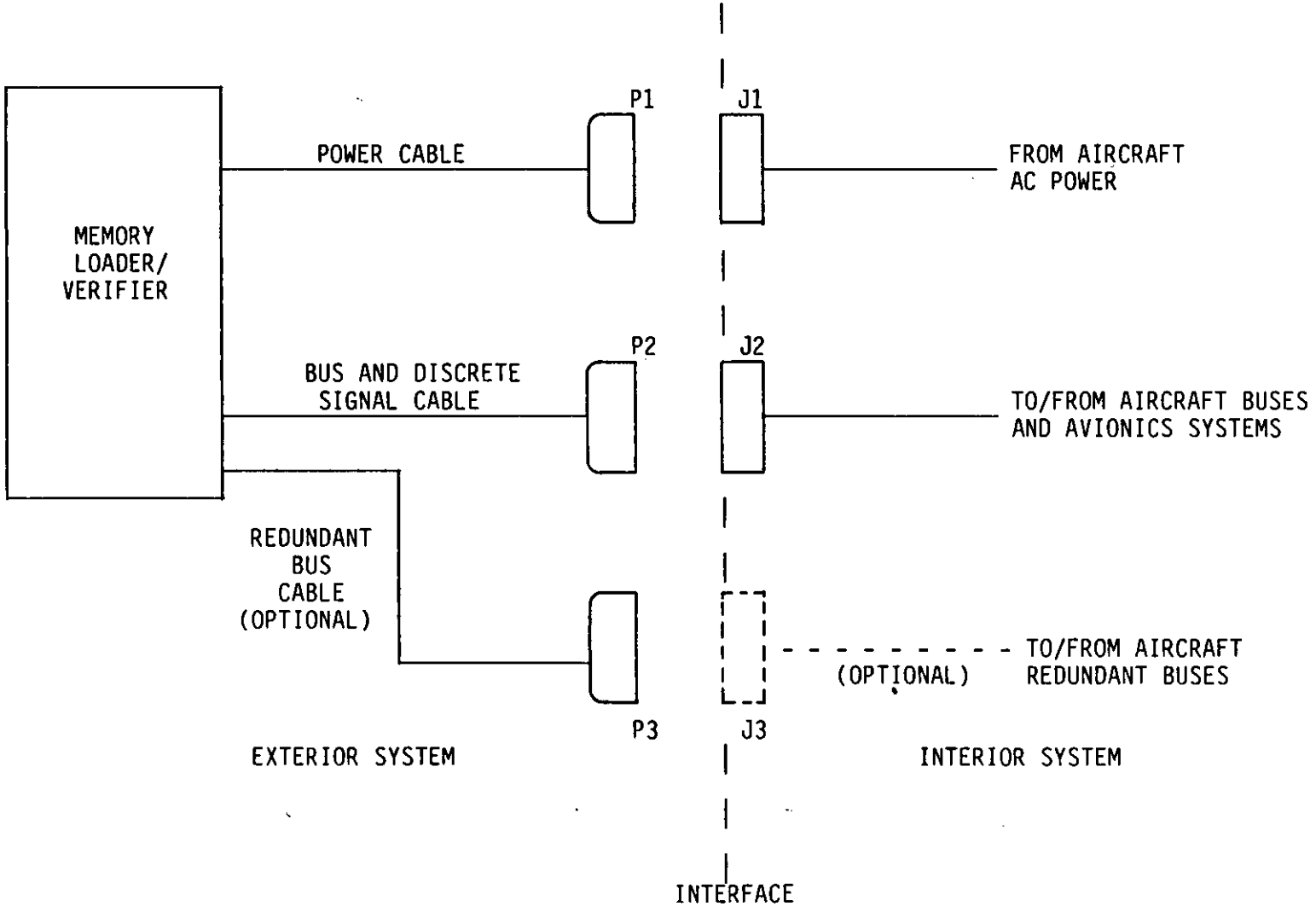

FIGURE 1. Type I Interface Connection Diagram.

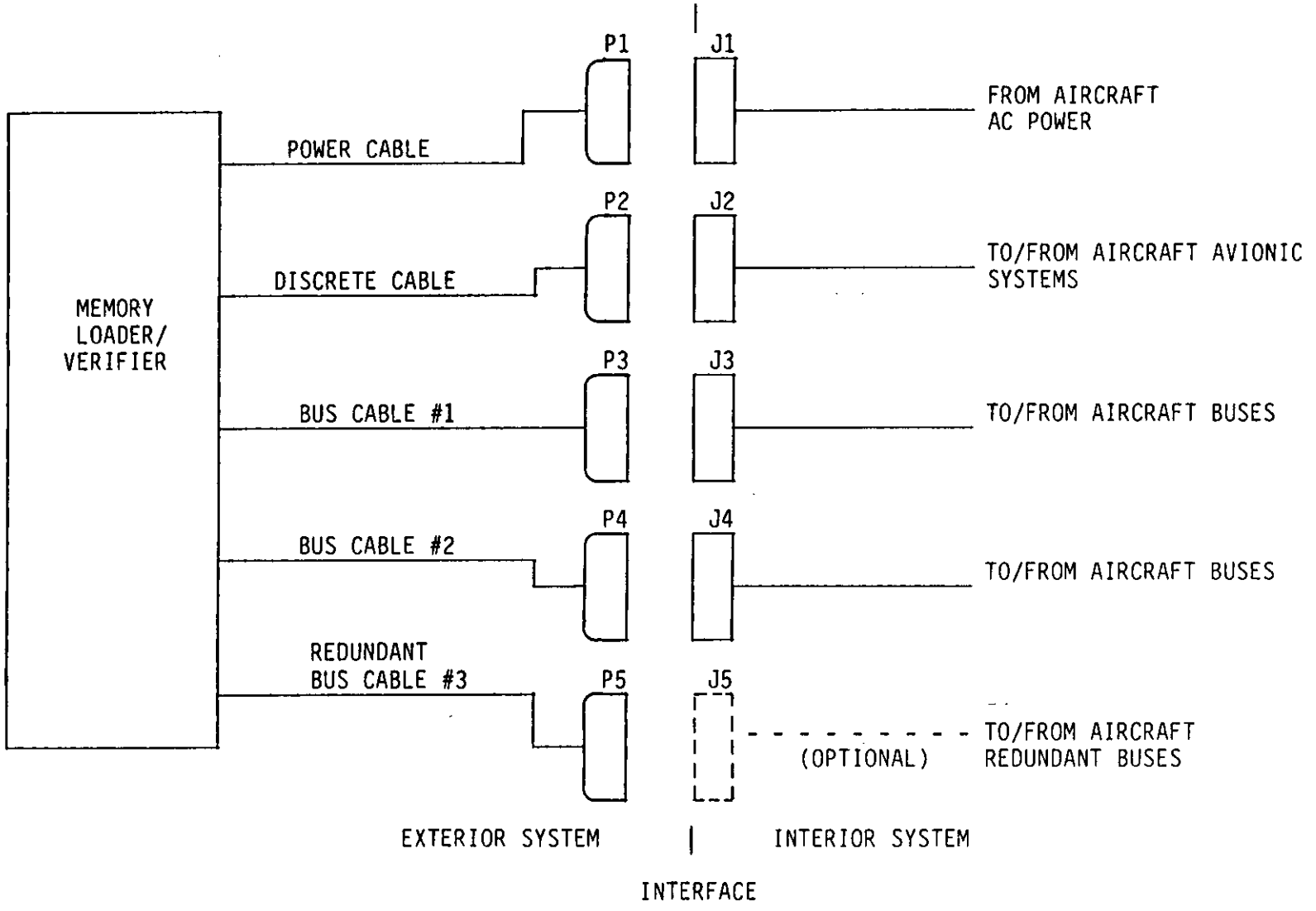

FIGURE 2. Type II Interface Connection Diagram.

5. DETAILED REQUIREMENTS

5.1 Aircraft Subsystem.

5.1.1 Power Connector. The power connector will enable aircraft AC power to be supplied to the MLV. The power connector will be a 7-pin connector, (aircraft provides a mate to type MS3106R18-9P). Both Type I and Type II interface connections will use this connector. The A-7E aircraft is a special case and will use an existing connector (mate to MS3106A20-29P). Provisions for 28VDC power are also identified; however, 28VDC power is provided for other ground support equipment and is not utilized by the MLV even though wiring is provided in the power cable. The pin designations for these connectors are shown in Table I.

5.1.1.1 Electrical Characteristics. The MLV will operate from a three-phase 230/115 VAC, 400 Hz wye connected source under the conditions specified in MIL-STD-704 for Category B equipment. The nominal current consumption on each connector pin will be 1.0 ampere RMS.

5.1.1.2 Mechanical Characteristics. The aircraft power connector will be mounted on a surface of the aircraft in the vicinity of the other interface connectors and will be accessible to O-Level personnel. The location of the power connector shall be compatible with the 10 ft. interface cables and a 10 ft. power cable for the MLV. A metal protective cap shall be provided to cover the connector and shall be physically attached to the aircraft.

5.1.2 Bus and Discrete Signal Connectors. The Bus and Discrete Signal connectors will enable the MLV to communicate with the aircraft's data buses and avionic systems.

5.1.2.1 Type I Connection. For the Type I Interface Connection a single 79-pin Bus and Discrete Connector (aircraft provides mate to type D38999/46-W-G-35PN) contains the primary bus connections and all of the discrete signal connections. The pin designations for this connector are shown in Table II. An optional 22-pin Redundant Bus Connector (aircraft provides mate to type D38999/46-W-C-35PN) contains the secondary side of the redundant avionic buses. The pin designations for this connector are shown in Table III.

5.1.2.2 Type II Connection. For the Type II Interface Connection a 55-pin Discrete Signal Connector (aircraft provides mate to type D38999/46-W-E-35PN) contains just the discrete signal connections. The pin designations for this connector are shown in Table IV. Two separate Bus Connectors (aircraft provides mate to type BLBPW19-4PN and BLBPW19-4PA), with four sets of triaxial inserts each, contain the primary bus connections. The pin designations for these connectors are shown in Table V. An optional Redundant Bus Connector (aircraft provides mate to type BLBPW19-4PB) contains the secondary side of the redundant bus connections. The pin designations for this connector are shown in Table VI.

TABLE I. Power Connector J1 Pin Designation for Type I and Type II Interface Connection.

PIN #	FUNCTION	PIN # (A-7E ONLY)
E	ϕA, 115V, 400HZ, 1.0A	A
F	ϕB, 115V, 400HZ, 1.0A	B
G	ϕC, 115V, 400HZ, 1.0A	C
B	NEUTRAL	D
C	CHASSIS GND	
A	28 VDC	F
D	28 VDC GND	

NOTES: 1) Phase Rotation will be from ϕA to ϕB to ϕC

TABLE II. Bus and Discrete Connector J2 Pin Designations for Type I Interface Connection.

NUMERICAL ORDER

PIN NO.	FUNCTION
1	EXTERNAL PROCESSOR ON/OFF
2	SPARE
3	SPARE
4	IPL FAIL 4-
5	IPL FAIL 4+
6	SPARE
7	SPARE
8	IPL FAIL 3-
9	IPL FAIL 3+
10	SPARE
11	SPARE
12	IPL FAIL 2-
13	IPL FAIL 2+
14	SPARE
15	SPARE
16	IPL FAIL 1-
17	IPL FAIL 1+
18	BOOT EN SMS RTN
19	BOOT EN SMS HI
20	RESERVED
21	RESERVED
22	RESERVED
23	RESERVED
24	RESERVED (BOOT EN RDP HI)
25	RESERVED (BOOT EN RDP RTN)
26	SPARE
27	SPARE
28	SPARE
29	PWR OFF/ON 3 REF GND
30	AV BUS 3 SHIELD
31	AV BUS 3+
32	AV BUS 3-
33	PWR OFF/ON 2 REF GND
34	AV BUS 2 SHIELD
35	AV BUS 2+
36	AV BUS 2-
37	PWR OFF/ON 4 REF GND
38	AV BUS 4 SHIELD
39	AV BUS 4+
40	AV BUS 4-

FUNCTIONAL ORDER

FUNCTION	PIN NO.
AIRCRAFT 2^0	54
AIRCRAFT 2^1	68
AIRCRAFT 2^2	77
AIRCRAFT 2^3	78
AIRCRAFT 2^4	70
AV BUS 1+	42
AV BUS 1-	43
AV BUS 1 SHIELD	44
AV BUS 2+	35
AV BUS 2-	36
AV BUS 2 SHIELD	34
AV BUS 3+	31
AV BUS 3-	32
AV BUS 3 SHIELD	30
AV BUS 4+	39
AV BUS 4-	40
AV BUS 4 SHIELD	38
AV REPROG EN 1+	75
AV REPROG EN 1-	74
AV REPROG EN 2+	79
AV REPROG EN 2-	72
BOOT EN SMS HI	19
BOOT EN SMS RTN	18
CONFIG 2^0	64
CONFIG 2^1	47
CONFIG 2^2	46
CONFIG 2^3	45
CONFIG GND	57
EW BUS+	49
EW BUS-	50
EW BUS SHIELD	48
EW OSM REPROG EN	76
EW UDM REPROG EN	65
EXTERNAL PROCESSOR ON/OFF	1
IPL 1+	59
IPL 1-	41
IPL 2+	69
IPL 2-	55
IPL 3+	67
IPL 3-	52

TABLE II. Bus and Discrete Connector J2 Pin Designations for Type I Interface Connection. - Continued

NUMERICAL ORDER

PIN NO.	FUNCTION
41	IPL 1-
42	AV BUS 1+
43	AV BUS 1-
44	AV BUS 1 SHIELD
45	CONFIG 2^3
46	CONFIG 2^2
47	CONFIG 2^1
48	EW BUS SHIELD
49	EW BUS +
50	EW BUS -
51	REFERENCE GND
52	IPL 3-
53	PWR OFF/ON 2
54	AIRCRAFT 2^0
55	IPL 2-
56	PWR OFF/ON 4
57	CONFIG GND
58	IPL 4-
59	IPL 1+
60	RESERVED (RELAY TEST A/C OPEN CK)
61	PWR OFF/ON 1
62	RESERVED (MSDRS RELAY RTN)
63	RESERVED (MSDRS RELAY HI)
64	CONFIG 2^0
65	EW UDM REPROG EN
66	PWR OFF/ON 3
67	IPL 3+
68	AIRCRAFT 2^1
69	IPL 2+
70	AIRCRAFT 2^4
71	IPL 4+
72	AV REPROG EN 2-
73	PWR OFF/ON 1 REF GND
74	AV REPROG EN 1-
75	AV REPROG EN 1+
76	EW OSM REPROG EN
77	AIRCRAFT 2^2
78	AIRCRAFT 2^3
79	AV REPROG EN 2+

FUNCTIONAL ORDER

FUNCTION	PIN NO.
IPL 4+	71
IPL 4-	58
IPL FAIL 1+	17
IPL FAIL 1-	16
IPL FAIL 2+	13
IPL FAIL 2-	12
IPL FAIL 3+	9
IPL FAIL 3-	8
IPL FAIL 4+	5
IPL FAIL 4-	4
PWR OFF/ON 1	61
PWR OFF/ON 1 REF GND	73
PWR OFF/ON 2	53
PWR OFF/ON 2 REF GND	33
PWR OFF/ON 3	66
PWR OFF/ON 3 REF GND	29
PWR OFF/ON 4	56
PWR OFF/ON 4 REF GND	37
REFERENCE GND	51
RESERVED	20
RESERVED	21
RESERVED	22
RESERVED	23
RESERVED (MSDRS OFF/ON HI)	63
RESERVED (MSDRS OFF/ON RTN)	62
RESERVED (RELAY TEST A/C OPEN CKT)	60
RESERVED (BOOT EN RDP HI)	24
RESERVED (BOOT EN RDP RTN)	25
SPARE	2
SPARE	3
SPARE	6
SPARE	7
SPARE	10
SPARE	11
SPARE	14
SPARE	15
SPARE	26
SPARE	27
SPARE	28

TABLE III. Redundant Bus Connector J3 Pin Designations for Type I Interface Connection.

PIN NO.	FUNCTION
1	SECONDARY AV BUS 1 SHIELD
2	SECONDARY AV BUS 1+
3	SECONDARY AV BUS 1-
4	SECONDARY AV BUS 2 SHIELD
5	SECONDARY AV BUS 2+
6	SECONDARY AV BUS 2-
7	SECONDARY AV BUS 3 SHIELD
8	SECONDARY AV BUS 3+
9	SECONDARY AV BUS 3-
10	SECONDARY AV BUS 4 SHIELD
11	SECONDARY AV BUS 4+
12	SECONDARY AV BUS 4-
13	SPARE
14	SPARE
15	SPARE
16	SPARE
17	SPARE
18	SPARE
19	SPARE
20	SPARE
21	SPARE
22	SPARE

TABLE IV. Discrete Connector J2 Pin Designations for Type II Interface Connection.

NUMERICAL ORDER

PIN NO.	FUNCTION
1	SPARE
2	AIRCRAFT 2^1
3	AIRCRAFT 2^0
4	IPL 1+
5	AV REPROG EN 1+
6	BOOT ENABLE SMS HI
7	AIRCRAFT 2^2
8	PWR OFF/ON 1
9	SPARE
10	IPL FAIL 1+
11	IPL 1-
12	AV REPROG EN 1-
13	BOOT ENABLE SMS RTN
14	AIRCRAFT 2^3
15	PWR OFF/ON 1 REF GND
16	SPARE
17	IPL FAIL 1-
18	IPL FAIL 2+
19	IPL 2+
20	AV REPROG EN 2+
21	RESERVED
22	AIRCRAFT 2^4
23	PWR OFF/ON 2
24	SPARE
25	IPL FAIL 3+
26	IPL FAIL 2-
27	IPL 2-
28	AV REPROG EN 2-
29	RESERVED
30	CONFIG GND
31	PWR OFF/ON 2 REF GND
32	IPL FAIL 3-
33	IPL FAIL 4+
34	IPL 4+
35	EW OSM REPROG EN
36	RESERVED
37	CONFIG 2^0
38	PWR OFF/ON 3
39	SPARE

FUNCTIONAL ORDER

FUNCTION	PIN NO.
AIRCRAFT 2^0	3
AIRCRAFT 2^1	2
AIRCRAFT 2^2	7
AIRCRAFT 2^3	14
AIRCRAFT 2^4	22
AV REPROG EN 1+	5
AV REPROG EN 1-	12
AV REPROG EN 2+	20
AV REPROG EN 2-	28
BOOT ENABLE SMS HI	6
BOOT ENABLE SMS RTN	13
CONFIG 2^0	37
CONFIG 2^1	44
CONFIG 2^2	50
CONFIG 2^3	54
CONFIG GND	30
EW OSM REPROG EN	35
EW UDM REPROG EN	42
EXTERNAL PROCESSOR ON/OFF	47
IPL 1+	4
IPL 1-	11
IPL 2+	19
IPL 2-	27
IPL 3+	49
IPL 3-	53
IPL 4+	34
IPL 4-	41
IPL FAIL 1+	10
IPL FAIL 1-	17
IPL FAIL 2+	18
IPL FAIL 2-	26
IPL FAIL 3+	25
IPL FAIL 3-	32
IPL FAIL 4+	33
IPL FAIL 4-	40
PWR OFF/ON 1	8
PWR OFF/ON 1 REF GND	15
PWR OFF/ON 2	23
PWR OFF/ON 2 REF GND	31

TABLE IV. Discrete Connector J2 Pin Designations for Type II Interface Connection. - Continued

NUMERICAL ORDER		FUNCTIONAL ORDER	
PIN NO.	FUNCTION	FUNCTION	PIN NO.
40	IPL FAIL 4-	PWR OFF/ON 3	38
41	IPL 4-	PWR OFF/ON 3 REF GND	45
42	EW UDM REPROG EN	PWR OFF/ON 4	51
43	RESERVED	PWR OFF/ON 4 REF GND	55
44	CONFIG 2^1	REFERENCE GND	48
45	PWR OFF/ON 3 REF GND	RESERVED	21
46	SPARE	RESERVED	29
47	EXTERNAL PROCESSOR ON/OFF	RESERVED	36
48	REFERENCE GND	RESERVED	43
49	IPL 3+	SPARE	1
50	CONFIG 2^2	SPARE	9
51	PWR OFF/ON 4	SPARE	16
52	SPARE	SPARE	24
53	IPL 3-	SPARE	39
54	CONFIG 2^3	SPARE	46
55	PWR OFF/ON 4 REF GND	SPARE	52

TABLE V. Bus Connectors J3 and J4 Contact Designations for Type II Interface Connection.

CONNECTOR/PIN NO.		FUNCTION
J3-A	CENTER CONDUCTOR	PRIMARY AV BUS 1+
J3-A	INNER SHIELD	PRIMARY AV BUS 1-
J3-A	OUTER SHIELD	PRIMARY AV BUS 1 SHIELD
J3-B	CENTER CONDUCTOR	EW BUS +
J3-B	INNER SHIELD	EW BUS -
J3-B	OUTER SHIELD	EW BUS SHIELD
J3-C	CENTER CONDUCTOR	RESERVED
J3-C	INNER SHIELD	RESERVED
J3-C	OUTER SHIELD	RESERVED
J3-D	CENTER CONDUCTOR	PRIMARY AV BUS 3+
J3-D	INNER SHIELD	PRIMARY AV BUS 3-
J3-D	OUTER SHIELD	PRIMARY AV BUS 3 SHIELD
J4-A	CENTER CONDUCTOR	RESERVED
J4-A	INNER SHIELD	RESERVED
J4-A	OUTER SHIELD	RESERVED
J4-B	CENTER CONDUCTOR	PRIMARY AV BUS 2+
J4-B	INNER SHIELD	PRIMARY AV BUS 2-
J4-B	OUTER SHIELD	PRIMARY AV BUS 2 SHIELD
J4-C	CENTER CONDUCTOR	SPARE
J4-C	INNER SHIELD	SPARE
J4-C	OUTER SHIELD	SPARE
J4-D	CENTER CONDUCTOR	PRIMARY AV BUS 4+
J4-D	INNER SHIELD	PRIMARY AV BUS 4-
J4-D	OUTER SHIELD	PRIMARY AV BUS 4 SHIELD

TABLE VI. Redundant Bus Connector J5 Contact Designations for Type II Interface Connection.

CONNECTOR/PIN NO.		FUNCTION
J5-A	CENTER CONDUCTOR	SECONDARY AV BUS 1+
J5-A	INNER SHIELD	SECONDARY AV BUS 1-
J5-A	OUTER SHIELD	SECONDARY AV BUS 1 SHIELD
J5-B	CENTER CONDUCTOR	SECONDARY AV BUS 2+
J5-B	INNER SHIELD	SECONDARY AV BUS 2-
J5-B	OUTER SHIELD	SECONDARY AV BUS 2 SHIELD
J5-C	CENTER CONDUCTOR	SECONDARY AV BUS 4+
J5-C	INNER SHIELD	SECONDARY AV BUS 4-
J5-C	OUTER SHIELD	SECONDARY AV BUS 4 SHIELD
J5-D	CENTER CONDUCTOR	SECONDARY AV BUS 3+
J5-D	INNER SHIELD	SECONDARY AV BUS 3-
J5-D	OUTER SHIELD	SECONDARY AV BUS 3 SHIELD

5.1.2.3 Optional Connections for Redundant Buses. For those cases where all four of the primary bus connections are not utilized it is an option to connect the secondary side of the redundant bus(es) to the Primary Bus Connector, thus avoiding the need for the Redundant Bus Connector. When this option is utilized in the aircraft wiring, the MLV shall not be required to utilize the secondary connection for true redundant bus operation. When this option is utilized, the MLV whether acting as BC or RT will only switch one time from the primary connection to the secondary connection.

5.1.2.4 Electrical Characteristics. (Type I and Type II Interface Connections.)

Connector pins in each interface connection will provide for the following:

a. Five sets of primary data bus lines (one EW and four Avionic Buses)

b. Four sets of redundant data bus lines (four Avionic Buses)

c. Two sets of Avionic (AV) reprogram enabling discretes

d. Two Electronic Warfare (EW) reprogram enable discretes

e. One set of Aircraft Identification pins (Aircraft Type and Aircraft Configuration Modification)

f. AN/AYK-14 Discretes

1. Four sets of AN/AYK-14 IPL (Initiate Program Load) lines
2. Four sets of AN/AYK-14 IPL fail lines
3. Four sets of AN/AYK-14 PWR OFF/ON lines

g. One Set of Boot Enable Stores Management System (SMS)

h. AN/ALQ-165 External Processor ON/OFF discrete

i. One set of MLV reserved pins

j. Five reserved pins for F/A-18 (Type I only)

k. Associated ground pins and spare pins.

5.1.2.4.1 Primary Data Bus Contacts. Each of the five sets of data bus connections will consist of three contacts to accommodate a twisted pair plus a shield ground. The maximum line-to-line, peak-to-peak voltage at the connector will be 48 volts. The nominal operating current will be 200 milliamperes RMS per line.

5.1.2.4.2 Redundant Data Bus Contacts. Each of the four sets of data bus connections will consist of three contacts to accommodate a twisted pair plus a shield ground. These contacts shall conform to the electrical requirement specified for the Primary Data Bus Contacts (5.1.2.4.1). Use of the redundant buses and connector is optional.

5.1.2.4.3 Reprogramming Enable Discretes.

5.1.2.4.3.1 Reprogramming Enable Types. The two types of hardwired reprogram enable discretes are as follows:

5.1.2.4.3.1.1 EW Reprogramming Enable Discretes. Three pins are provided for the following signals.

a. EW User Data Memory (UDM) Reprogram Enable
b. EW Operating Software Memory (OSM) Reprogram Enable
c. Reference Ground

5.1.2.4.3.1.2 AV Reprogramming Enable Discretes. Four pins are provided for the following signals.

a. AV Reprogram Enable 1+
b. AV Reprogram Enable 1-
c. AV Reprogram Enable 2+
d. AV Reprogram Enable 2-

5.1.2.4.3.2 Reprogram Enable Functions.

5.1.2.4.3.2.1 EW UDM Reprogram Enable Discrete Functions. The EW UDM Reprogram Enable discrete has three functions. First, while activated, it will enable both the erase and write functions of all UDMs (i.e., EEPROMs) of all avionic units communicating on the associated data bus. Second, upon initial activation, it will, if required, cause the associated Bus Controller (BC) to start polling the MLV on the associated bus (i.e., the EW MUX BUS in this case), and, upon deactivation, will, if required, cause the BC to stop polling the MLV. Third, the Enable is used to indicate to the BC that it is to resume its Bus Controller functions when the Enable is released. The EW OSM Reprogram Enable discrete has the same function in relation to the reprogrammable Operating Software Memories (OSM) in units connected to the EW Mux Bus.

5.1.2.4.3.2.2 AV Reprogram Enable Discrete Functions. The AV Reprogram Enable discretes are used similar to the EW Reprogram Enable discretes; however, the same two discretes are used for all four avionics buses. Both AV Reprogram Enables may be connected to individual avionics equipment to control two memory areas in a manner identical to the way the EW Reprogram Enable discretes are used. Or the two AV Reprogram Enables may be routed separately to equipment that does not require control of two memory areas in any fashion desired. The AV Reprogram Enables are not used with the AN/AYK-14. The IPL, IPL Fail, and PWR OFF/ON discretes discussed later are used to control AN/AYK-14 loading.

5.1.2.4.3.3 Driving the Enable Discretes. Each of the two EW Reprogramming Enable discretes will be driven by a single-ended transmission line, i.e., use only one signal line, in the MLV. Each line driver will be capable of driving up to 24 line receivers. Each receiver will have a minimum impedance of 6K ohms. The MLV output for each EW Reprogramming discrete shall also be capable of sinking 30 ma. to activate a 28 VDC relay (MLV provides an active ground

output referenced to the Reference Ground to a relay with a maximum open circuit voltage of 30 VDC) in lieu of driving the 24 line receivers. Each of the two AV Reprogramming Enable discretes will be driven by a differential transmitter, i.e., use two signal lines, in the MLV. Each line driver will be capable of driving up to 24 RS-422 differential line receivers. Each receiver will have a minimum impedance of 6K ohms.

5.1.2.4.3.4 Equipment Timing. Equipment utilizing either the EW Reprogramming Enable discretes or the AV Reprogramming Enable discretes will wait 500 usec. before recognizing the discretes to avoid misinterpreting a transient during MLV power up, etc.

5.1.2.4.4 Aircraft Identification Pins. One set of ten pins will be selectively jumpered within the aircraft to provide an initial cable attachment check, to identify the aircraft type and to identify the configuration modification. The pin functions are:

a. Ground Reference (1 Pin)
b. Aircraft Type (5 Pins)
c. Aircraft Configuration Modification (4 Pins)

Each type and modification pin will carry one milliampere or less DC current with jumpers between the ground reference and the appropriate pins.

5.1.2.4.4.1 Aircraft Type. The shorting pattern of these pins enables $2^5 - 1 = 31$ aircraft types to be defined as indicated in Table VII. At least one of the Aircraft Type pins will always be jumpered to the ground reference within all aircraft. This will allow the MLV to run a continuity check to verify that the discrete cable has been attached. Assignment of Aircraft Type Codes shall be by application to Naval Air Development Center, Code 5021, Warminster PA 18974-5000.

5.1.2.4.4.2 Aircraft Configuration Modification. The Aircraft Configuration Modification pins will enable up to $2^4 = 16$ modifications to be identified for each aircraft type. For a given aircraft, new Aircraft Configuration Modification numbers will only be defined for avionics configuration changes which affect memory loading. The determination of the request to change Aircraft Configuration Modification code will be made based on directed aircraft changes.

5.1.2.4.5 AN/AYK-14 Discretes. The IPL, IPL Fail and PWR OFF/ON discretes will be implemented between each AN/AYK-14 computer (up to four) and the MLV. The IPL and IPL FAIL discretes will consist of a twisted balanced pair utilizing RS-422 line drivers/receivers in the MLV. These discretes will be used to initiate loading and to indicate an error in loading the AN/AYK-14. The PWR OFF/ON discrete will be a TTL compatible single ended active low which will cause the AN/AYK-14 to execute a power down. This discrete will be used to silence the AN/AYK-14 while reprogramming other equipments on the bus and to force the AN/AYK-14 to recognize the IPL discrete. The MLV output for each of the PWR OFF/ON discretes shall also be capable of sinking 200 ma. to activate a 28 VDC relay (MLV provides an active ground output referenced to the PWR OFF/ON Reference Ground to a relay with a maximum open circuit voltage of 32 VDC) in lieu of the direct TTL connection to the AN/AYK-14.

TABLE VII. Aircraft Type Code.

Aircraft Type	Pin 2^4	Pin 2^3	Pin 2^2	Pin 2^1	Pin 2^0
Not Used	0	0	0	0	0
A-4M	0	0	0	0	1
F-4S	0	0	0	1	0
F-4N	0	0	0	1	1
RF-4B	0	0	1	0	0
A-6E	0	0	1	0	1
A-6F	0	0	1	1	0
EA-6B	0	0	1	1	1
A-7E	0	1	0	0	0
AV-8B	0	1	0	0	1
AV-8C	0	1	0	1	0
F-14A+	0	1	0	1	1
F-14D	0	1	1	0	0
F/A-18A/B/C/D	0	1	1	0	1
Spare	0	1	1	1	0
V-22	0	1	1	1	1
F-14A	1	0	0	0	0
Spare Codes	1	0	0	0	1
Through	1	1	1	1	0
Reserved	1	1	1	1	1

Notes: (1) 0 = Open to Ground
1 = Short to Ground

(2) Since the 0-0-0-0-0 combination is never used, a 0-0-0-0-0 code read by the MLV would indicate that the cable is not attached.

5.1.2.4.5.1 AN/AYK-14 Discrete Usage. This standard allows for up to four Avionics Buses with an IPL, IPL Fail and PWR OFF/ON discrete assigned to each bus. For the special case where a second AN/AYK-14 (acting as an RT) is on a bus, the IPL, IPL Fail and PWR OFF/ON discrete from an unused bus can be utilized to control the second AN/AYK-14.

5.1.2.4.6 Boot Enable Stores Management System (SMS). The Boot Enable SMS signal is utilized for aircraft with an SMS requiring this input to enable the boot strap load operation. The interface is a contact closure internal to the MLV with a maximum current of 200 ma. and a maximum open circuit voltage of 32 VDC and is applicable to Appendix F operation.

5.1.2.4.7 AN/ALQ-165 External Processor ON/OFF Discrete. A one wire discrete to control power on/off of the ALQ-165 during reprogramming is provided. This discrete shall be utilized by the MLV when use is indicated in the Lookup Table (see 6.1.c.3). The purpose of this discrete is to limit ALQ-165 power on time to less than 1 minute for a Load/Verify of 32K data words of UDM. This discrete is shorted to the Reference Ground signal (200 ma. maximum current, 32 VDC maximum open circuit voltage) associated with the EW UDM and OSM Reprogram Enable discretes by the MLV 500 msec prior to any multiplex bus communications with AN/ALQ-165. The MLV shall open this line (open circuit impedance to Reference Ground > or = 100K ohms) after the completion of a Load/Verify or a Verify (indicated by Busy Bit clear in STATUS RESPONSE WORD of the Activity Message after the Reprogram Control Message at the end of the Verify (see Appendix B)). Additionally the MLV will open this line 10 seconds after halting to display an error requiring operator input or after the total on time programmed in the Lookup Table (see 6.1.1) (nominally 3 minutes).

5.1.2.4.8 MLV Reserved Pins. Four pins of the interface connector are to be open circuit in the aircraft wiring in order to allow for MLV self test functions through the interface connector.

5.1.2.4.9 F/A-18 Reserved Pins (Type I only). Five pins are reserved on the Type I interface connector for utilization of existing F/A-18 functions. The reserved pins are: Maintenance Signal Data Recording Set (MSDRS) OFF/ON two wire contact closure 200 ma. maximum current, 32 VDC maximum open circuit voltage; BOOT ENABLE Radar Data Processor (RDP) two wire contact closure 200 ma. maximum current, 32 VDC maximum open circuit voltage; and, a one wire Relay Test signal maximum 32 VDC signal at 200 ma.

5.1.2.4.10 Associated Ground Pins and Spares. Pins for shield/grounding and designated spares are provided as called out in Tables II and IV.

5.1.2.5 Mechanical Characteristics. The aircraft signal cable connectors will be mounted on a surface of the aircraft accessible to O-Level personnel. A metal protective cap shall be provided to cover the connector and shall be physically attached to the aircraft.

5.1.2.6 F/A-18 Bus and Discrete Signal Connections. The F/A-18A/B/C/D aircraft utilizes an existing 37 pin connector for bus and discrete signal connections that does not comply with this standard. However, all MLV

interconnections are equivalent except that: only three Avionics Buses are provided for in F/A-18A/B (four in F/A-18C/D) (all redundant); only two IPL discretes are provided for; no AYK-14 POWER OFF/ON or IPL FAIL wiring is incorporated (however, two reserved pins are designated for future use of two POWER OFF/ON discretes, and this wiring will be provided in the MLV cable) (future use of these reserved pins assumes that Lookup Table information will preclude use of these pins when the redundant bus connections to AV MUX 3 are present on these pins); the AV Reprogram Enable discretes are not provided for; the MSDRS OFF/ON discrete is utilized in F/A-18A/B only, the BOOT ENABLE RDP discrete is utilized; the Aircraft Type and Aircraft Configuration Modification discretes are physically jumpered internal to the F/A-18 peculiar cable (however, two reserved pins for future use of Aircraft Configuration are provided and will be wired in the MLV cable); several shield grounds are combined; and an aircraft chassis ground is provided. The EW Mux Bus, the EW Reprogram Enable, and AN/ALQ-165 Processor ON/OFF wiring are currently only incorporated in the F/A-18C/D.

5.1.3 Aircraft Wiring Provisions. Each aircraft shall supply the appropriate connectors for the aircraft bus and discrete connectors and power connectors (5.1.1 and 5.1.2) with the on-board subsystems.

5.1.3.1 Electrical Characteristics. Generalized cable schematics are shown in Figures 3 and 4 for Type I and Type II Interface Connections. See also NAVAIRDEVCEN Drawing 80206-SK302-850001, Type I Memory Loader/Verifier Aircraft Interface and NAVAIRDEVCEN Drawing 80206-SK302-850002, Type II Memory Loader/Verifier Aircraft Interface.

The electrical cabling will route electrical power from the aircraft AC power system to the Power Connector (5.1.1). The electrical cabling will provide selectively grounded pins for continuity checking and Aircraft Type and Aircraft Configuration identification (5.1.2.4.4); it will provide for data communications on up to five sets of data lines (5.1.2.4.1 and 5.1.2.4.2); it will provide for up to four hardwired enabling discretes (5.1.2.4.3); it will provide for up to four IPL discretes, four IPL Fail discretes, four PWR OFF/ON discretes (5.1.2.4.5); it will provide for the Boot Enable SMS discrete (5.1.2.4.6) when required; it will provide for the AN/ALQ-165 External Processor On/Off discrete (5.1.2.4.7) when AN/ALQ-165 is part of the Aircraft provisions; it will provide for the MLV Reserved Pins and Associated Ground Pins and Spares (5.1.2.4.8 and 5.1.2.4.10); and, for the Type I interface, it will accommodate the F/A-18 Reserved Pins (5.1.2.4.9) at the signal connector. Cabling provisions will be installed in each aircraft type based on the equipment in that aircraft.

5.1.3.1.1 Data Bus Characteristics.

5.1.3.1.1.1 EW MUX BUS. This bus will be designed in accordance with MDC A3818B or MIL-STD-1553B using a shielded twisted pair cable with an impedance of 63 to 85 ohms. Bus connections shall be as described in Section 5.2.

This bus will normally communicate with the applicable mix of the EW avionics units. This bus will be associated with the EW UDM Reprogram Enable and the EW OSM Reprogram Enable discretes. For U.S. Navy tactical aircraft the mixture will typically consist of the following units:

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a. AN/ALQ-126B (One or Two Units)
b. AN/ALQ-162
c. AN/ALQ-164
d. AN/ALQ-165 (Pod)
e. AN/ALQ-165
f. AN/APR-43
g. AN/ALR-45F
h. AN/ALR-67
i. Other units as added

with the AN/ALR-45F or AN/ALR-67 acting as the on-board EW MUX Bus Controller. The equipment listed above is designed to MDC A3818B and not MIL-STD-1553B.

5.1.3.1.1.2 Avionics MUX BUS I, II, III and IV . (Primary and optional Secondary). This bus will be designed in accordance with MDC A3818B or MIL-STD-1553B using a shielded twisted pair cable with an impedance of 63 to to 85 ohms. Bus connections shall be as described in Section 5.2. Avionics MUX BUS I, II, III, and IV will all be associated with the Avionics Reprogram Enable discretes jointly, and when applicable an individual set of IPL, IPL Fail and PWR OFF/ON discretes for each AN/AYK-14. Each of the four avionic mux buses (i.e., Avionic MUX BUS I, II, III and IV) will communicate via the primary half of the on-board redundant buses. For aircraft utilizing the optional redundant bus connections, the MLV when acting as a BC will switch to the redundant bus if after 2 seconds it does not receive a Status Word from the Remote Terminal (RT) currently being processed. When acting as BC the MLV will only switch once between the primary and secondary buses. After switching to the redundant bus, if communications are not established within 2 seconds or a subsequent communication error occurs, the MLV will declare a fault. When acting as RT the MLV will operate as a redundant terminal at the discretion of the BC. The MLV acting as RT will declare an error only if communications with the BC are interrupted for 2 seconds or greater. The selection of which equipments are attached to which bus will vary by aircraft type and configuration.

5.1.3.2 Mechanical Characteristics. The internal cabling will be designed to meet the specific requirements of each aircraft and to meet the previously cited general requirements. In addition, the cables will be designed so that bus-to-bus cross-coupling will not degrade the Bit Error Rate (BER) and Word Error Rate (WER) characteristics of each bus. Also, the discrete lines will be designed to provide comparable cross-coupling rejection.

5.2 MLV Subsystem.

5.2.1 MLV Description. The MLV will be a small portable device containing a Memory Storage Device (MSD) and the appropriate (Type I or Type II) interface cables. The MSD will contain the information necessary to load and verify the memories of all applicable avionic systems. This storage device will normally be prepared by the IMA. Because of capacity limitations the MSD referred to herein may actually consist of a set of MSDs which are sequentially loaded into the MLV manually. To load avionic system data into the equipment of a particular aircraft, the portable MLV, containing the updated

MSD, will be connected to the aircraft at the "O-Level." This connection will be made by the cables provided. These cables will be nominally 10 feet in length, and will be designed for use in a carrier flight deck environment.

5.2.1.1 Power Cable. The Power Cable will enable aircraft electrical power to be supplied to the MLV in accordance with requirements of Section 5.1.1 and subsidiary sections.

5.2.1.2 Bus and Discrete Signal Cable. The Bus and Discrete signal cable(s) will enable signals to be exchanged between the MLV and the aircraft in accordance with the requirements of Section 5.1.2 and subsidiary sections. The MLV shall provide for all signal interfaces independent of aircraft application.

5.2.1.2.1 MLV Bus Connection. The MLV interface cables will provide 9 mux bus cables to the MLV (1 EW BUS, 4 PRIMARY AVIONIC BUSES, and 4 SECONDARY AVIONIC BUSES). When acting as BC the MLV internal mux bus circuitry (input/output transformer) will be connected to only one of these cables at any one time. When acting as RT the MLV mux bus circuitry will be connected to the primary connection and the redundant bus circuitry will be connected to the secondary connection if redundant bus operation is specified on the Lookup Table (see 5.2.2.1.3.1). The specific bus connected at any one time will be a function of which equipment is being processed at that time. When the MLV selects a bus for connection it will, based on aircraft type and configuration, select the type of mux bus connection to be utilized (see Figure 5). For aircraft that utilize coupling transformers between the aircraft buses and the MLV interface connector (Long Stub Transformer Coupling) the MLV will select unisolated coupling (i.e., no isolation resistors in series with the MLV input/output transformer). For aircraft that do not utilize coupling transformers between the aircraft buses and the MLV interface connector (Short Stub Direct Coupling) the MLV will select isolated coupling (i.e., isolation resistors in series with the MLV input/output transformer). Additionally the MLV will ground or open circuit the center tap of its input/output transformer based on the aircraft type and configuration. The use of isolated or unisolated coupling and grounded or open circuit transformer center tap may vary between the individual buses (i.e., the MLV will utilize aircraft type and configuration codes as well as the currently selected bus to determine the type of mux bus connection).

5.2.1.2.2 MLV Discrete Connections. The MLV shall be capable of providing simultaneous control of the active/inactive state of all discretes.

5.2.1.2.3 Nomenclature Conventions.

5.2.1.2.3.1 Multiplex Buses. For all bus interfaces the connection labeled "+" shall be of greater potential than the connection labled "-" during the first one and one-half bit times of the COMMAND WORD or STATUS WORD (see Appendix A).

5.2.1.2.3.2 RS-422 Interface. Active state + line at greater potential than - line. Inactive state open circuit or - line at greater potential than + line.

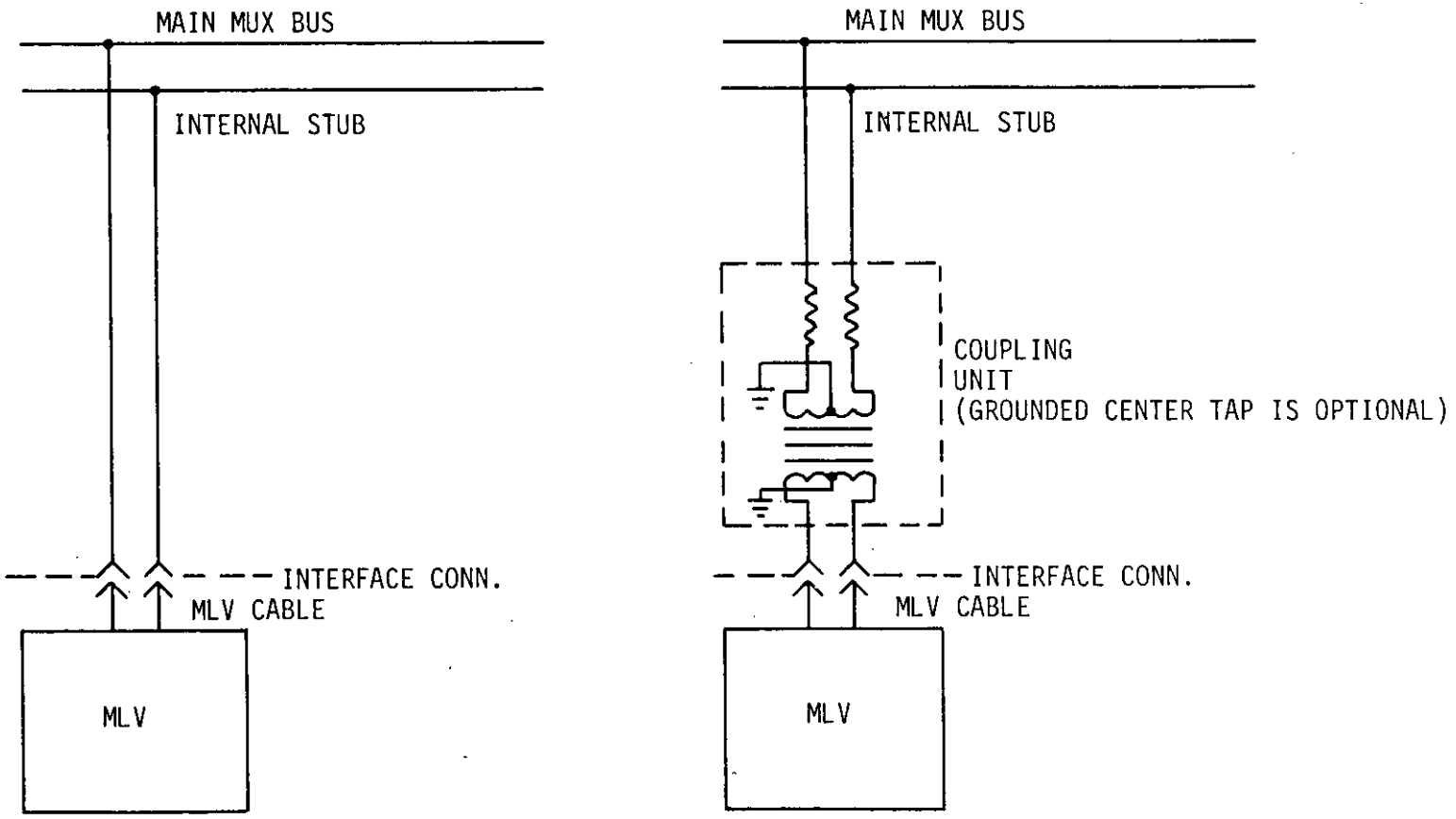

FIGURE 5. Bus Coupling Methods.

5.2.2 MLV Operation. The following paragraphs describe the sequence of operations starting with the attachment of the MLV cables to the aircraft to be loaded. These functions are summarized in Figure 6 (located at the end of Section 6) and described in detail in Section 5.2.2.2 through 5.2.2.4.2. The multiplex bus protocol and word formats are described in Appendices A through H.

5.2.2.1 MLV Preparation. The MLV will be tested and loaded prior to its connection to an aircraft to be loaded. The MLV will contain a removable Memory Storage Device (or will use a set of removable MSDs if necessary) which will contain an image of the current update version of the contents of all reprogrammable avionic system memories as well as the information required to update portions of the previous version for units that do not require a complete memory rewrite. The MLV will also contain all necessary software for MLV operation which may also be stored on the MSD. The MSD will have a minimum of 14.4 million bits of data storage capacity and a minimum read/write transfer rate of 40,000 bits per second. The minimum usable storage capacity for Memory Files (unit reprogramming data) will be 482K, 16 bit words. The Memory Storage Device will contain a Library file and Memory file(s) for each subsystem to be programmed, and may contain MLV operating software.

5.2.2.1.1 MLV Operating Software. The MLV Operating Software will consist of embedded firmware in the MLV and Operating Software which may be stored on the MSD. The combination of the embedded software and MSD stored software, which may be used as overlays, will provide for satisfying all the requirements of this standard without the need to change the MSD for any purpose other than additional avionic subsystem memory storage capacity.

5.2.2.1.2 Library File. The MLV will maintain a Library file on the MSD that describes the MSD contents. The Library file will have a descriptor that is generated by the MLV when the MSD is prepared or modified. This descriptor will contain the aircraft identification code, the MSD sequence number (MSD sequence when more than one MSD is required for a particular aircraft); and date information stored as month/day/year to describe the date the MSD was prepared or modified. The Library file descriptor will also contain flags indicating the MSD status, namely: one flag will indicate whether or not the MSD is for fleet release and when fleet release is indicated any MLV laboratory functions stored on the MSD will not be accessible; one flag will indicate whether or not the MSD is automatic mode compatable (see 5.2.2.2.1); and one flag will indicate whether or not a write to the MSD is permitted (see 5.2.2.2.e.5) (normally an MSD for fleet release will indicate that a write to the MSD is not permitted). Each MSD will be used to support only one aircraft type and shall be compatible with storing at least 23 Memory Files. For each Memory File on the MSD the Library will contain a memory file description consisting of:

a. Applicable aircraft configuration code

b. The number of the aircraft bus on which the unit is to be reprogrammed

5.2.2.1.2 Continued.

c. The terminal address on the bus (value of 0 indicates that the unit is the normal Bus Controller)

d. An AYK-14 file identifier. This description shall consist of four bits and shall be identical to the four bits in the Lookup Table Data that describe discrete utilization during processing (see 5.2.2.1.3.1.c and 6.1.c.2). All four bits shall be zero for non AYK-14 Library Files. For AYK-14 Library Files, only one of the four bits shall be set and the bit that is set shall indicate which AYK-14 POWER OFF/ON, IPL and IPL fail discretes are associated with the AYK-14 that the Library File pertains to. In addition, these bits shall be utilized along with the terminal address on the bus to identify which AYK-14 file is associated with which AYK-14, since more than one AYK-14 with the same terminal address may exist on the same bus.

e. A protocol identifier (i.e., applicable appendix)

f. A file name identifier consisting of at least eight alphanumeric ASCII characters

g. An F/A-18 SMS file identifier. This description shall consist of two bits and shall describe which type of SMS the file applies to. For non Appendix F protocol files and non SMS files, this descriptor shall have a value of 0. If there are not two SMS files on the MSD with the same aircraft configuration code, this descriptor shall also have a value of 0 for Appendix F SMS protocol files. If there are two SMS files on the MSD with the same aircraft configuration code, the descriptor shall then indicate which type of SMS the file applies to. When the MLV attempts to utilize any library file with this descriptor having a value other than 0, the MLV shall query the operator to indicate the type of SMS installed in the aircraft (AYQ-9 core memory, or AYQ-9/AYQ-15 EEPROM). After operator response, the MLV shall use the file with a descriptor value of 1 if AYQ-9 core memory was indicated, or the file with a discriptor value of 2 if AYQ-9/AYQ-15 EEPROM was indicated. A descriptor value of 3 shall be invalid. This descriptor will allow use of the correct SMS file when two files with the same aircraft configuration and terminal address are present on the MSD.

h. The Memory Area(s) that the entry applies to

i. A flag indicating whether the entry is for a patch file or a complete file

j. Memory File location and status information.

The limit on the number of Memory files (23 minimum) for the Library File will not allow a corresponding maximum number of units if separate memory areas or patch files are present, since separate Library file entries are required for these files.

A patch file and a non-patch file (complete file) may exist on the MSD for the same unit. The Memory Configuration (see Memory Files 5.2.2.1.3) will determine whether the patch file or complete file will be used. If the current Memory Configuration of the device is the same as the patch file, the patch file will be used (Memory Configuration for a patch file identifies the Memory Configuration that the patch applies to). If the current Memory Configuration of the device is less than the complete file (non patch file) Memory Configuration, then the complete file will be used. Patch files may not be used if the unit does not allow Memory Configuration Messages. The MLV processing will assume that the MSD is properly prepared and will not contain a patch file and a complete file with the same Memory configuration for the same unit. It is also assumed that a patch file will not create a new Memory Configuration that is less than the complete file Memory Configuration.

5.2.2.1.3 Memory Files. There will be individual Memory Files describing MLV operation and containing the necessary data to reprogram an individual unit. The Memory File will contain a Lookup Table and Reprogramming Data. A Memory File must be wholly contained on the MSD (i.e., a Memory File may not be split between multiple MSDs).

5.2.2.1.3.1 Lookup Table. The Lookup Table will contain information necessary for the MLV to communicate with the unit being processed. The details of the Lookup Table data are provided in Section 6.1. The following is a summary of the minimum data contents.

a. Physical bus parameters (center tap grounding, coupling method, bus number)

b. Initial states for MLV discrete outputs

c. Discrete utilization during processing

d. MLV bus takeover method

e. Unit protocol

f. RT address

g. Allowable "0" level functions, namely: Load/Verify or Load only; and Verify allowed.

h. Single, sequential, simultaneous Memory Area(s)

i. Memory Configuration Message information

j. Reprogram Control Message information

k. Message handling options to be implemented by the MLV (Busy bit usage/operation, redundant bus use, message delays, busy bit error criteria; and maximum number of retries)

l. Maximum unit on time to be used in controlling the AN/ALQ-165 External Processor ON/OFF discrete

m. Transfer Control and Start Execution Message data.

5.2.2.1.3.2 Reprogramming Data. The reprogramming data will be stored on the MSD in blocks, records, etc., necessary for MLV operation. Actual Storage format will be controlled by the MLV and will not require user specification. Relative to the user the data stored will be groupings of transaction (e.g., Header, Memory Data, ..., Memory Data, Trailer or Header, Trailer) information. The data stored will be the Data Words required for the transaction (e.g., for Appendices B and C the stored data will be four Data Words for the Header Message, all the Data Words of the Memory Data Load/Verify Messages, and the two Data Words of the Trailer Message).

5.2.2.2 Initial On-Line Operations. (See Figure 6 located at the end of Section 6.)

Prior to cable attachment to the aircraft, the MLV will have its Power Switch in the OFF position.

a. Cable Attachment - The MLV Power, Bus and Discrete Connectors (and, when utilized, Redundant Bus Connector) will be connected to the aircraft to be loaded.

b. MLV Power Up/BIT - Once all cables have been attached, the MLV Power Switch will be manually activated. This will turn on the MLV power and automatically cause the MLV to perform initialization and an internal BIT check.

c. Loop Test/Aircraft ID - Once the cables have been attached (sensed by the fact that at least one of the aircraft type identification pins is always shorted to ground) the MLV will scan the five Aircraft Type lines to determine which combination is shorted to ground. This will enable the identification of one of up to thirty-one aircraft types as shown in Table VII. After the aircraft type has been determined, the MLV will scan the four aircraft configuration lines to determine the specific aircraft configuration. The aircraft type and configuration will determine the MLV RT address for each of the applicable buses. The reserved Aircraft Type Code may be used for any non-aircraft manual application (e.g., loading a pod prior to aircraft attachment). When the reserved Aircraft Type Code (11111) is read, the MLV will ignore the Configuration code, select direct coupling and ground the transformer center tap.

If the loop test for aircraft ID, after MLV power up and internal self test, fails, the MLV will display an "ATTACH CABLES" message

5.2.2.2.c. Continued.

and after being signaled by the operator that the cables have been attached the MLV will proceed normally.

d. Memory Storage Device Check - Once the aircraft type and configuration have been established, the MLV will read the Library File on the MSD to verify that the proper MSD has been loaded.

e. Operator Selections - The MLV will then halt and cue the operator to select the desired function. The available functions are:

1. Automatic Load/Verify as described in 5.2.2.2.1/5.2.2.2.3 and in the applicable appendix.

2. Manual Load/Verify as described in Sections 5.2.2.2.2/5.2.2.2.3 and in the applicable appendix.

3. Manual Verify only which is identical to the Manual Load/Verify except that no Load is performed (applicable only to Appendices B, C, D, F, and H).

4. Display Library function which will allow examination of the Library File in sequential fashion (one Library File entry displayed and manual sequencing). This function or a seperate function shall also display the date and aircraft type for the MSD.

5. Save function which will allow the creation of a tape Memory File for a unit. Normally, this function will not be available on MSDs prepared for "O" level use. Special MSDs for use with the Save function will be prepared for "O" level use and a flag in the MSD Library File will indicate whether or not a Save (Write) to the MSD may be performed. The special MSDs for use with the "O" level Save function will also contain a permitted unit file. This file will constitute a list of all equipment for which a Save function can be performed on the MSD. The file will contain all the Lookup Table information for the unit(s). In order to create the MSD memory file, a unit with the desired Memory Data physically resident in it will be required. Relative to the unit for which the MSD file is being created, the Save will appear to be a Verify (i.e., all data transfers will be identical to the Verify function except no Load will precede the Verify). During the Save, the MLV will request the operator to manually input all required information except the Memory Data itself. The operator will be required to enter all the Library File information except the aircraft configuration code which is read from the MLV connector and the information that is redundant with the Lookup Table data (i.e., the parameters called out in 5.2.2.1.2 except: the aircraft configuration; the aircraft bus number; the terminal address; the AYK-14 file identifier; and the protocol identifier). The operator will also be

required, for each Header, Data, ..., Data, Trailer sequence to enter the Header information (4 words) and Trailer information (1 word, checksum is computed by MLV). The Header, Trailer information will be entered as many times as necessary to complete the desired Save file (i.e., Verify the unit Memory Area).

6. Other MLV functions may be contained on the MSD for non "0" level functions but will not be accessible with the MLV connected to the aircraft.

It is the intention of this standard to require that any load operation will always be followed by a verify operation when possible (Appendices B, C, D, F (for other than AYQ-9), and H). Except when determined otherwise by the cognizant Software Support Activity this shall be the normal mode of operation. The automatic verify after a load and/or the use of a stand alone verify in manual mode may be inhibited for a particular unit by parameters in the Lookup Table for that unit, only when this restriction in operation has been authorized by the cognizant Software Support Activity.

5.2.2.2.1 Automatic Reprogram Operation. Automatic Reprogram Operation assumes that all equipments on the bus(es) are operating and that MLV will control the equipment to be reprogrammed and the order in which they are to be reprogrammed. Automatic Reprogram Operation also requires that the MSD be properly prepared, namely, that there is only one Memory File for each unit on the MSD. A flag in the Library File on the MSD will be used to indicate that the MSD is compatible with Automatic Reprogram Operation.

a. Methods of Loading/Verifying - Three methods of loading and verifying are used. The special case for the AN/AYK-14 is discussed in 5.2.2.2.3.

1. Modified Dynamic Bus Allocation to the MLV - The MLV is initially an RT and after being polled by the normal aircraft BC requests to become the BC (MLV=BC). The normal aircraft BC then reverts to an RT for the loading and verifying of itself and all other RTs on the bus.

2. MLV acts as BC - The MLV is initially and remains the BC for any aircraft configuration that does not have an on-board BC.

3. MLV acts as RT - The MLV is initially an RT for the loading and verifying of the normal aircraft BC, for the case where the aircraft BC cannot become an RT (MLV=RT). Under this method the normal aircraft BC would be loaded and verified first (if it is to be loaded and verified) and then the BC would be requested to turn-off (BC=Quiet) while the MLV acts as BC for the loading and verifying of the remaining RTs. For the case where the AN/AYK-14 is the BC and cannot revert to an RT, the AN/AYK-14 will be turned off via the PWR OFF/ON discrete and AN/AYK-14 reprogramming will be performed last (see 5.2.2.2.3).

5.2.2.2.1.a. Continued.

The preferred method for loading and verifying is Modified Dynamic Bus Allocation and this method will be used wherever possible.

The preferred method for loading the AN/AYK-14 with MIL-STD-1553B bus capability is that the AN/AYK-14 will become an RT upon generation of the IPL by the MLV (Appendix D.) This will allow the AN/AYK-14 to be verified after loading.

Prior to connection of the MLV, the normal aircraft BC for each bus will control communications with all RTs operating on that bus.

b. Initial MLV State - The MLV will contain a bus compatible terminal which is capable of acting as either an RT or BC. When first connected, the MLV terminal will normally be in the RT mode with a distinct address (determined by the aircraft configuration and defined in the Lookup tables). When the MLV assumes RT status as the initial state, processing will continue as described in c and d below. For aircraft configurations that do not have an on-board BC, the MLV will act as BC at MLV startup for the selected bus. In this case, (MLV initially BC) the MLV, after setting the appropriate Reprogram Enable discretes, will verify that all equipments are present by sending an Activity Message to each RT on the bus. The MLV will not send any messages to an RT until at least 10 msec after the Reprogram Enable discretes are set. After verification that all RTs are present, the MLV will proceed to perform the memory Load and Verify functions for each unit on the bus that requires reprogramming (see 5.2.2.3 and the applicable appendix).

c. Discrete Initiation - The MLV acting as an RT will set the appropriate Reprogram Enable discrete(s) for the bus selected. When required (i.e., when the MLV is not normally polled by the BC) the setting of the Reprogram Enabling discrete(s) shall cause the BC to initiate polling of the MLV. The BC shall poll for the MLV by sending Activity Messages to the MLV RT address as long as the appropriate discrete is active, regardless of whether or not the MLV responds. In any configuration where more than one discrete is connected to the BC, the active state of either discrete shall cause the BC to poll the MLV RT address. (Note that this discrete also has other functions discussed below.) The active state of the Reprogram Enable discrete input(s) to the BC shall not alter normal BC operation other than by adding the MLV to the RT address list. Only the simultaneous presence of an active Reprogram Enable discrete and the receipt of a valid Reprogram Control Message (see Appendix B or C) from the MLV shall cause the BC to suspend normal operation. If other fail safe discretes are also used (i.e., Reprogram Enable and weight on wheels), then it is permissible for the Reprogram Enable to alter normal operations.

d. Bus Communication - When the MLV has selected a bus on which it will initially act as an RT, the following operations will be performed.

1. If the BC cannot revert to an RT, the MLV will perform the Avionic Subsystem Memory Load/Verify functions below for the BC with the MLV acting as an RT. Upon completion of the BC Load/Verify the MLV will then request via a Reprogram Control Message that the BC stop all bus communications.

2. If the BC can revert to an RT, the MLV will utilize the Activity Message to request a Reprogram Control Message in order to cause the BC to revert to an RT.

3. Once the MLV has obtained BC status the MLV will if necessary Load/Verify the normal BC. The MLV will then verify that all Appendix B equipments are present by sending an Activity Message to each RT on the bus. Only the presence of Appendix B protocol subsystems will be checked by the MLV. The MLV will not send any messages to an RT until at least 10 msec after the Reprogram Enable discretes are set. After verification that all Appendix B RTs are present the MLV will proceed to perform the Avionic Subsystems Memory Load Verify functions for each RT on the bus. (See 5.2.2.3 and the applicable appendix.)

5.2.2.2.2 Manual Reprogram Operation. Manual Reprogram Operation allows for the operator to control reprogramming on a bus by bus and unit by unit basis (allows for the case where all units on the bus are not present or operating). The initial on-line operations and points of operator intervention are shown in Figure 6 located at the end of Section 6.

a. Methods of Loading/Verifying - Manual Reprogram Operation provides for the three methods of loading and verifying described in 5.2.2.2.1.a (including the case where the on-board BC is not communicating on the bus, in which case the MLV acts as BC for the loading and verifying of the unit(s) selected).

b. Initial MLV State - The initial MLV state for Manual Reprogram is essentially the same as for Automatic Reprogram described in 5.2.2.2.1.b. Once the operator has selected the Manual Reprogram Operation mode, the MLV will request the operator to indicate the bus and the unit (and unit Memory Area when applicable) on that bus which is to be reprogrammed. The method of selecting the unit, bus, memory area is optional and may be selected by specifying unique file names (unique to unit, bus, memory area) for example. If the MLV normally assumes an RT state for the selected bus, processing will continue as described in c and d below. If the MLV normally assumes a BC state for the selected bus, the MLV, after setting the appropriate Reprogram Enable discretes, will verify that the selected unit is present by sending an Activity Message. The MLV will Load/Verify the selected unit to be reprogrammed, and then ask if another unit is to be reprogrammed.

c. Discrete Initiation - This process for Manual Reprogram is the same as for Automatic Reprogram described in 5.2.2.2.1.c.

d. Bus Communication - Once the operator has selected a bus and unit (and unit Memory Area when applicable) to be reprogrammed, the MLV will check the MSD for reprogramming information for that unit. The following operations will then be performed.

1. The MLV after having set the appropriate discretes and acting as an RT will listen on the selected bus to determine if the BC is operating. The MLV will assume the BC is not operating if an Activity Message is not sent to the MLV address within 2 seconds of the setting of the discrete(s).

2. If the MLV determines that the on-board BC is not operating, the MLV will assume the role of BC and establish communications with the RT to be loaded and verified. If the BC is not communicating and is the unit selected for reprogramming, an error will be declared.

3. If the on-board BC is operating and can revert to an RT, the MLV will utilize the Activity Message to request a Reprogram Control Message in order to cause the on-board BC to revert to an RT. The Avionics Subsystem Memory Load Verify function (see 5.2.2.3 and the appropriate appendix) will be performed with the MLV acting as BC for the selected RT.

4. If the on-board BC is operating but cannot revert to an RT and is not the unit to be reprogrammed, the MLV will request via a Reprogram Control Message that the on-board BC stop all bus communications (BC=Quiet). The Avionics Subsystem Memory Load Verify function (see 5.2.2.3 and appropriate appendix) will be performed with the MLV acting as BC for the selected unit.

5. If the on-board BC is operating and cannot revert to an RT and is the selected unit, the MLV will perform the Avionic Subsystem Memory Load/Verify function for the BC with the MLV acting as an RT. (See 5.2.2.3 and the appropriate appendix.)

5.2.2.2.3 MLV Control of AN/AYK-14 (Automatic and Manual Reprogram Operation).

a. In order for the MLV to properly load the AN/AYK-14, or to properly load other devices over a bus for which the AN/AYK-14 is the Bus Controller, special interfaces are provided. The MLV will provide individual IPL (Initiate Program Load) and PWR OFF/ON discrete signals to the AN/AYK-14. The AN/AYK-14 will not utilize the Avionics Reprogramming Enable discretes.

b. For each bus selected for reprogramming (either manual or automatic operation) which is normally controlled by an AN/AYK-14, the following procedures will be utilized. The MLV will set the PWR OFF/ON discrete for the AN/AYK-14 on the selected bus. This will turn the AN/AYK-14 off. If other AN/AYK-14's can assume the BC roll

5.2.2.2.3.b. Continued.

on the selected bus (or another AN/AYK-14 is an RT on the selected bus), their PWR OFF/ON discretes shall also be set, turning them off.

c. Any RTs on the selected bus to be reprogrammed will be reprogrammed first. In the manual mode the MLV will load and verify the selected RT and then ask the operator if another RT is to be reprogrammed. Once all RTs that are to be reprogrammed on the selected bus have been reprogrammed, the MLV will determine if the AN/AYK-14 is to be reprogrammed (for both the manual and automatic modes the operator will be queried as to whether the AN/AYK-14 is to be reprogrammed). For the special case where a second AN/AYK-14 (acting as an RT) is on the selected bus to be reprogrammed, it will be reprogrammed prior to the AN/AYK-14 acting as BC.

d. If the AN/AYK-14 is not to be reprogrammed, the MLV will determine if another bus is to be reprogrammed (for the manual mode the operator will be queried as to whether another bus is to be reprogrammed).

e. If the AN/AYK-14 is to be reprogrammed, the MLV will set the IPL discrete for the selected bus and then release the PWR OFF/ON discrete for the selected bus only, reactivating the AN/AYK-14. Turning the AN/AYK-14 on with the IPL discrete active will cause it to execute the Boot Loader. The MLV will then release the IPL discrete, initiate the AN/AYK-14 boot loader and reprogram in accordance with Appendix D, E or G, depending on the AN/AYK-14 version associated with the aircraft type and configuration codes.

f. After completion of the reprogramming of the AN/AYK-14 and thus all units on the selected bus, the MLV will determine if another bus is to be reprogrammed (for the manual mode the operator will be queried as to whether another bus is to be reprogrammed). If another bus is selected, the AN/AYK-14 PWR OFF/ON discrete for the previous bus, if still active, will be released if indicated in the Lookup Table for the next unit on the selected bus. If another bus is not selected, the MLV will clear all discretes including the AN/AYK-14 PWR OFF/ON discretes as part of the final on line operations.

g. In the F-18 aircraft the AYK-14 POWER OFF/ON and IPL FAIL discretes are not wired. There are provisions for future incorporation of two POWER OFF/ON discretes and the MLV wiring will be supplied to these reserved pins. The MLV will control these discretes as described above, however, there will be no response by the AYK-14. When the MLV Aircraft Type Code indicates F-18A/B/C/D, the MLV, after connection to the appropriate bus and setting of discretes, shall monitor the bus for message activity to any terminal address. If activity is detected, indicating that the BC is still active and the Power OFF/ON discretes are not wired, the MLV shall request manual operator intervention to power up or down the appropriate AYK-14's for each change in state of the POWER OFF/ON discretes.

5.2.2.3 Avionics Subsystem Memory Load-Verify. The Reprogram Enable discretes will be routed to all applicable equipment. These discretes will be utilized by applicable equipments to enable the memory erase and write functions and to qualify the Reprogram Control Message functions. The MLV will reprogram each equipment in the manner described in the applicable appendices. The appendices are:

a. Appendix A, Bus Protocol, describes the general bus message transfer on the A3818B and MIL-STD-1553 multiplex data buses.

b. Appendix B, Message Formats (MLV=BC), describes the message format between the MLV and avionic systems with the MLV acting as BC. Applies to all new equipment. Not applicable to AN/AYK-14. The Memory Configuration Message will only be utilized when indicated as usable in the unit Lookup Table.

c. Appendix C, Message Formats (MLV=RT), describes the message format between the MLV and avionic systems with the MLV acting as an RT. Applies to all existing equipment that cannot become an RT except the AN/AYK-14. The Memory Configuration Message will only be utilized when indicated as usable in the unit Lookup Table.

d. Appendix D, Message Formats (MLV=BC, AN/AYK-14 SIM-B=RT), describes the message format between the MLV and the AN/AYK-14 with MLV acting as BC and the SIM B version of the AN/AYK-14 acting as RT. This is the preferred method of loading the AN/AYK-14.

e. Appendix E, Message Formats (MLV=RT, AN/AYK-14 SIM-B=BC), describes the message format between the MLV and the AN/AYK-14 with the MLV acting as an RT and the SIM B version of the AN/AYK-14 acting as BC.

f. Appendix F, Message Format (MLV=BC, Stores Management System (SMS) or Signal Data Computer (SDC)=RT), describes the message format between the MLV and the AYQ-9 SMS core memory version, the AYQ-9 EEPROM version or the AYQ-15 SMS and the F/A-18 SDC, with the MLV acting as BC and SMS or SDC acting as RT.

g. Appendix G, Message Formats (MLV=RT, AN/AYK-14 SIM-A=BC), describes the message format between the MLV and the AN/AYK-14 with SIM-A. Since SIM-A is not capable of acting as an RT the MLV must act as RT. This is the least preferred method for loading the AN/AYK-14.

h. Appendix H, Message Formats (MLV=BC, CP-1001=RT), describes the message format between the MLV and the CP-1001 HARM Command Launch Computer with the MLV acting as BC and the CLC acting as RT.

5.2.2.4 Final On-Line Operations.

5.2.2.4.1 Bus Processing Completion. After completing reprogramming of all units on the bus that are to be reprogrammed the MLV will send, via a Reprogram Control Message, a command for the normal bus controller to revert from the RT to BC mode in order to resume normal bus operation. Since the Avionics

Reprogram Enable discretes may be used for other buses, the discrete may remain active after bus operation is returned to the normal BC. In the case where the normal BC could not revert to an RT and the BC was commanded to stop bus communications, when the MLV switches to the next bus if the MLV does not release the active discrete, the previous bus will remain quiet until all buses are completed and the final on-line operations below are completed. For each bus on which the AN/AYK-14 is the Bus Controller the PWR OFF/ON discrete will be released by the MLV prior to the selection of the next bus for reprogramming only when the AN/AYK-14 is reprogrammed.

5.2.2.4.2 Aircraft Processing Completion. After processing for all buses on the aircraft has been completed the MLV will clear the Reprogram Enable and/or PWR OFF/ON discretes and the operator will be informed that the aircraft reprogramming function is complete. The release of the Reprogram Enable and/or PWR OFF/ON discretes shall cause any BC that has stopped communicating on the bus to resume normal operations. Each RT shall suspend declaring bus errors while the Reprogram Enable discrete(s) are present in order to preclude bus errors being caused by a quiet bus in the case of a BC that has been commanded to suspend bus communications. Additionally the BC shall not declare a bus error when the MLV stops communicating on the bus (e.g., at bus reprogram completion).

Upon being notified that processing for all units and all buses has been completed, the MLV operator will manually perform the following functions:

a. MLV Power Down - Manually turn off the MLV power switch.
b. Power Cable Detachment - Disconnect all cables.

5.3 Avionic Equipment Requirements. All avionic equipment shall conform to the specified requirements of the aircraft subsystem and the MLV interface requirements defined herein. Any of the options allowed by this standard may be implemented (i.e., transformer coupling, grounded transformer, busy bit utilization, etc.) provided that they are consistent with the procurement specifications and the intended aircraft installation(s). Protocol usage shall be in accordance with Section 1.4 and the procurement specification.

6. NOTES

6.1 Lookup Table Data. The Lookup Table (see 5.2.2.1.3.1) will contain information necessary for the MLV to communicate with the unit being processed. Unless otherwise specified all bits set to 1 shall mean active (i.e., MLV output is to be active) and all bits set to 0 shall mean inactive (i.e., MLV output is to be inactive). The Lookup Table will contain as a minimum the following information:

a. Bus parameters for the MLV bus hardware and software

   1. One bit for center tap open/grounded. (0 = grounded, 1 = open)

   2. One bit for coupling type to be used. (0 = Transformer Coupling, 1 = Direct Coupling).

6.1.a. Continued.

3. Three bits describing the bus the MLV is to couple to (Redundant with Library File):

value = 0 = none (not used)
1 = Avionics Bus No 1
2 = Avionics Bus No 2
3 = Avionics Bus No 3
4 = Avionics Bus No 4
5 = EW Bus
6 = Not used
7 = Not used

b. Discrete settings to be performed by the MLV prior to MLV communication on the bus. Fifteen bits shall describe the status of the following signal lines:

EW UDM Reprogram Enable (5.1.2.4.3.2.1)
EW OSM Reprogram Enable (5.1.2.4.3.2.1)
AV Reprogram Enable 1 (5.1.2.4.3.2.2)
AV Reprogram Enable 2 (5.1.2.4.3.2.2)
Boot Enable SMS (5.1.2.4.6)
MSDRS OFF/ON (5.1.2.4.9)
Boot Enable RDP (5.1.2.4.9)
AYK-14 Power OFF/ON 1 (5.1.2.4.5)
AYK-14 Power OFF/ON 2 (5.1.2.4.5)
AYK-14 Power OFF/ON 3 (5.1.2.4.5)
AYK-14 Power OFF/ON 4 (5.1.2.4.5)
AYK-14 IPL 1 (5.1.2.4.5)
AYK-14 IPL 2 (5.1.2.4.5)
AYK-14 IPL 3 (5.1.2.4.5)
AYK-14 IPL 4 (5.1.2.4.5)

c. Discrete utilization parameters for controlling the Load/Verify.

1. One bit shall indicate whether the normal Bus Controller is an AYK-14. When this bit is set (=1), it will cause the MLV to request operator intervention to determine if the AYK-14 should be reprogrammed prior to switching off the selected bus. The quieting of the AYK-14(s) prior to communication with the selected unit shall be controlled by the AYK-14 Power Off/On 1 through 4 discrete settings indicated by the bits described in 6.1.b. independent of the setting of this bit. This bit will be utilized for all Memory Files.

2. Four bits shall describe the use of the four AYK-14 interfaces for reprogramming the AYK-14 (redundant with Library File). Only one of the four AYK-14 bits shall be set and the set bit shall indicate which AYK-14 POWER OFF/ON, IPL, and IPL fail discretes should be used to control the AYK-14 being processed

6.1.c. Continued.

(i.e., for Appendix D, E or G operation which discretes are to be toggled or read to control the AYK-14). These bits are only used for processing of AYK-14 Memory Files.

3. One bit shall indicate usage of the ALQ-165 External Processor On/Off discrete for ALQ-165 only. The ALQ-165 External Processor On/Off bit when set shall indicate that the ALQ-165 External Processor On/Off discrete (5.1.2.4.7) is to be used to control the ALQ-165 Appendix B operation.

d. MLV operation to obtain control of the bus. Three bits shall describe MLV operation as follows:

value = 0 = Not used
1 = The MLV begins operation on the bus as a Remote Terminal (RT) and converts the normal Bus Controller (BC) to an RT, then the MLV operates as BC
2 = The MLV begins operation on the bus as the BC
3 = The MLV begins and continues operation as an RT
4 = The MLV begins operation on the bus as an RT, then quiets the normal BC and the MLV then operates as BC
5 = Not used
6 = Not used
7 = Not used

e. MLV operation mode. Four bits shall describe the MLV operation mode (i.e., protocol identifier) (Redundant with Library File).

value = 0 = Not used
1 = Appendix B (20.) protocol
2 = Appendix C (30.) protocol
3 = Appendix D (40.) protocol
4 = Appendix E (50.) protocol
5 = Not used.
6 = Appendix G (70.) protocol
7 = Appendix H (80.) protocol
8 = Appendix F (60.) protocol for SMS core memory
9 = Appendix F (60.) protocol for SMS EEPROM memory
10 = Appendix F (60.) protocol for SDC
11-15 = Not used

f. RT address assignments. Three variables each with 5 bits of data shall describe RT addressing requirements. The three variables are for: the RT to be reprogrammed by the MLV when the unit is normally an RT (Redundant with Library File); the RT address that the current BC will utilize after being converted from a BC to an RT; and the RT address the MLV is to assume when the MLV connects to the bus as an RT.

6.1 Continued.

g. Allowable "0" level functions. Two bits shall describe the functions that are allowed to be performed on the unit being reprogrammed. One bit shall indicate whether or not to inhibit the automatic verify at the end of a load (1 = do not do a verify, 0 = do a verify). One bit shall indicate whether or not a manual verify at "0" level is disallowed or not (1 = verify not allowed, 0 = verify is not inhibited).

h. File type description parameter. Two bits shall be used to describe the Memory File type, namely: single Memory Area (one Load/Verify); a simultaneous Memory Area (two Loads followed by two Verifies using one Memory File and one Library File entry); or a sequential Memory Area (one Load/Verify followed by a second Load/Verify using a second Memory File and a second Library File entry). The MLV will automatically process (chain) the second file for a sequential load; however, only one chain operation is possible, since the Memory Area identifier in the Library File only allows for the definition of Memory Area 1 and 2.

value = 0 = Single Memory Area
1 = Sequential Memory Areas
2 = Simultaneous Memory Area
3 = Not used

i. Memory Configuration information. This data shall determine whether or not to check the current device configuration, which data words to utilize, and what the configuration of the memory image on the MSD is. One bit shall indicate that the Appendix B or C Memory Configuration Message is or is not to be utilized (see applicable protocol). If the Memory Configuration Message is usable, in Manual Mode the MLV will display the configuration data received from the unit to the operator after setting the discretes and prior to any other reprogramming action being started. The operator may proceed with the action or abort at that time. Two bits shall describe which Memory Configuration Message Data Words are to be checked by the MLV.

value = 0 = Not used
1 = Check only Data Word 1 of Memory Configuration Message
2 = Check only Data Word 2 of Memory Configuration Message
3 = Check both Data Words 1 and 2 of the Memory Configuration Message

Two 16 bit words in the Lookup Table shall contain the Memory Configuration Message Data Word 1 and Data Word 2 comparison information. These data words will only be used for units that allow the Memory Configuration Message. In manual mode these words are only

6.1.i. Continued.

used to determine whether the MLV is to use a patch file or a complete memory file. In automatic mode these words are used to determine if the unit requires reprogramming and whether to use a patch file or a complete memory file. In determining which file to use, the MLV will always check the patch file Library entry if it exists before checking the complete memory file if it exists.

j. Reprogram Control Message Data Word information. These Lookup Table parameters will describe: Remote Terminal nomenclature; Bus Controller nomenclature; control information for the unit being processed; and the Fill data for the Reprogram Control Message. Information for the Reprogram Control Message used to convert the BC to an RT or quiet the BC will also be stored.

1. Three 16 bit words shall provide the unit nomenclature for the RT to be processed. If the unit being processed (reprogrammed) is the bus controller, these data words shall be set to zero value. If the unit being processed is an RT (or a BC that has been converted to an RT), these data words will be used for the Reprogram Control Message nomenclature information when the MLV is acting as BC.

2. Three 16 bit words shall provide the unit nomenclature for the normal (Appendix C) bus controller. These data words will be used for the Reprogram Control Message nomenclature information when the MLV is acting as an RT (i.e., during the time the MLV acting as an RT is communicating with the BC in order to convert it to an RT, to quiet it, or to reprogram it).

3. Two 16 bit words shall provide the information to be used by the MLV in constructing the fourth data word of the Reprogram Control Message during reprogramming of the unit. The two words represent two variables, the second of which is used only when two memory areas are being loaded simultaneously (i.e., both from the same Library File). The second variable is used after the first memory area is completed (indicated by Transfer Control = 00 or 10 in the last Header Message sent) when a simultaneous memory area is indicated. The MLV will utilize the appropriate variable for the memory area being processed. The data used by the MLV is extracted from the variable selectively (i.e., by masking).

The Fill bits of the fourth data word (bits 10 to 15) are derived from the variable for every Reprogram Control Message.

Bits 7 and 6 (memory area enables) of the fourth data word of the Reprogram Control Message are extracted from the variable to construct the first Reprogram Control Message for the Load Function (these bits are 0 for the Verify Function).

6.1.j. Continued.

Bits 5 and 4 (memory area disables) of the fourth data word of the Reprogram Control Message are extracted from the variable to construct the Reprogram Control Message at the end of a Load (end of Load is indicated by Transfer Control = 00 or 10 in the last Header Message sent). These bits are 0 for the Verify function. The state of bits 8 and 9 (Load/Verify) will always be 00 for the Reprogram Control Message at the end of a Load or Verify.

Bit 0 (transfer control) of the fourth data word of the Reprogram Control Message is extracted from the variable to construct the Reprogram Control Message at the end of a Verify (end of Verify is indicated by Transfer Control = 00 in the last Header Message sent). This bit is 0 for all other cases including Transfer Control = 10 (signifying Transfer Control) in the last Header Message of the VERIFY. When Transfer Control = 10 in the last Header Message for a Verify, the MLV will send the Reprogram Control Message with bits 0-9 of the fourth data word = 0. This implementation (Transfer Control bit in the fourth data word of the Reprogram Control Message set to value indicated by Lookup Table only after a Verify) precludes the transfer control via the Reprogram Control Message before a Verify shown in the center of Figures 10 and 11 (Appendices B and C). This operation precludes transfer to an unverified memory area as discussed in general operation 20.2.e and 30.2.e of Appendices B and C. Transfer of control to an unaltered Memory Area (as shown in Figures 10 and 11) prior to the Verify of the reprogrammed Memory Area using the Transfer Control (bits 0-1 of Data Word four) of the Header Message is possible but not recommended.

4. Six bits of data shall provide the information for the Fill field (bits 15-10) of the fourth Data Word of the Reprogram Control Message when the MLV acting as an RT is converting the BC to an RT or quieting the BC.

k. Message handling options to be implemented by the MLV.

1. One bit of information shall indicate whether or not the Status Word BUSY Bit for an RT is usable or whether the MLV is to use bit 15 of the Data Word in the Activity Message to detect a busy condition (1 = BUSY bit in Status Word is usable, 0 = BUSY bit in Status Word will always be 0) for Appendix B protocol. The MLV hardware will ignore all data words received after the Status Word if the Busy Bit (bit 3 of the STATUS RESPONSE WORD) in the Status Word is set (Appendices B, D, F and H). For this reason the MLV will always assume that an RT is busy if the Status Word Busy Bit is set. For Appendix B protocol, even if the Lookup Table indicates that the Busy Bit in the Activity Message DATA WORD is to be used, the MLV will assume the RT is

6.1.k. Continued.

busy if the Status Word Busy Bit is set. The Busy Bit in the Activity Message DATA WORD will be used by the MLV if the Status Word Busy Bit is indicated as unusable after the Status Word Busy Bit is cleared. Since the first message commanded by the MLV will be an Activity Message, the MLV will assume that the RT that uses the Data Word Busy Bit is Busy until an Activity Message response with both the status word and data word Busy Bits clear is received.

2. One bit of information shall indicate what MLV action is to be taken by the MLV when the RT Status Word response to a receive type message has the Busy Bit set. If the Lookup Table value of this bit = 1, the MLV will assume that the message was properly received and will continue normal processing after the Busy bit is cleared. If the Lookup Table value = 0, the MLV will assume that the Data Word(s) in the message were not received by the RT and when the Busy Bit is cleared the last receive message will be repeated.

3. One bit shall indicate whether the redundant bus is usable or not. If the Lookup Table value of this bit = 1, the MLV will assume the redundant bus is usable. If the Lookup Table value = 0, the MLV will assume the redundant bus is not usable. An additional 4 bits shall indicate which MLV bus connection is to be used to communicate on the redundant bus. These bits are required to allow the optional connection for redundant buses called out in 5.1.2.3. The MLV will utilize the redundant input connection indicated by the value of these bits.

value = 0 = None (not used)
1 = Primary Avionics Bus No. 1
2 = Primary Avionics Bus No. 2
3 = Primary Avionics Bus No. 3
4 = Primary Avionics Bus No. 4
5 = EW Bus
6-8 = Not used
9 = Secondary Avionics Bus No. 1
10 = Secondary Avionics Bus No. 2
11 = Secondary Avionics Bus No. 3
12 = Secondary Avionics Bus No. 4
13-15 = Not used

If a value less than 8 is indicated (values 5 through 8 are not valid for redundant bus usage), the MLV shall not be required to allow true redundant bus operation. In this case the MLV will assume that optional redundant bus connections are utilized and will only allow a one time switch from the designated primary to the designated optional connection.

6.1.k. Continued.

4. Eight bits shall indicate modification of the Appendix B normal 10 msec. Activity Message cycle (see Appendix B 20.3.d). The eight bit value shall represent 0 to 255 milliseconds of time added to the MLV minimum Activity Message interval. The normal value of the variable is 0A hex (10 msec.). The use of other values will allow optimizing the total load time for any particular unit. For example, shorter times may be used to speed up detecting the Busy Bit clearing, or longer times may be used to allow sufficient time for terminal processing so the Busy Bit will be cleared for the second activity message. A value of 0 shall indicate maximum MLV hardware capability.

5. Sixteen bits shall indicate the number of times during a transaction (Header, Memory Data, ..., Memory Data, Trailer or Header, Trailer) the Busy Bit may be set before the MLV declares an error. The sixteen bit value (0 to 65535) is the total count of busy bits that may be incurred during a transaction. The time to detect an error in Appendix B protocol is this count times the interval between Activity Messages. This field may also be used as a timer for other protocols.

6. Sixteen bits shall indicate the maximum number of times the operator is allowed to request a retry for an Appendix B or C manual retry Reprogram Status error (Data Word value of 8003 Hex).

l. A minimum of eight bits shall be used to indicate the maximum on-time for the AN/ALQ-165 External Processor On/Off discrete. This variable shall have a minimum resolution of 10 seconds and shall be compatible with allowing a maximum on-time of between 10 seconds and 30 minutes.

m. Transfer Control and Start Execution Message data.

1. One bit shall provide the MLV masking information for bit 1 of the fourth DATA WORD of the Header Message to be used during a Load function. During a Load the MLV will logically "and" the value of this bit with bit 1 of the fourth DATA WORD of the Header Message regardless of the protocol selected. (Appendix H does not use the Header Message.) This bit should be set to 0 to preclude a transfer control during a load which is to be followed by a verify. This operation is provided to allow a transfer of control after a verify but prevent the transfer of control during a Load to a memory area that is not part of the reprogramming software. Masking is required because the same Header information is used for the Load and Verify functions. For the protocols of Appendicies E, F, and G this bit is not required, since there is no transfer of control allowed via the Header Message; however, this bit should be set to 0 to ensure the correct format of the Header Message.

2. Three bits shall control the issuance of a Start Execution Message for the Appendix F protocol. Each bit shall indicate whether the MLV should command a Start Execution Message at: the end of a load during a load/verify operation; the end of a load during a load only operation (auto verify inhibited); and at the end of a verify/save whether or not preceded by a load.

6.2 Flow Chart Notation. In the flow charts of this document dashed rectangles indicate action to be taken if required or when applicable. Solid rectangles indicate action that will always be taken.

6.3 Subject Term (Key Word) Listing.

Asynchronous
Bit rate
Bootstrap loading
Bus controller (BC)
Data bus
Data word
Library file
Lockup table
Memory file
Message
Pulse code modulation
Remote terminal (RT)
Reprogramming data
Status word
Time division multiplexing (TDM)

Preparing activity:
Navy - AS
Project GDRQ-N120

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The digital copy of MIL-STD-2217(AS), dated 16-October 1991 does not include the foldout pages 23, 25, and 51. If you need a copy of them must be ordered these foldouts separately, please fax this page to 215-697-9398 and include your complete mailing address below. Pages 24, 26 and 52 are blanks.

APPENDIX A

BUS PROTOCOL

10. MESSAGE TRANSFER

This section applies to message transfers on MIL-STD-1553A, MDC A3818B or MIL-STD-1553B Multiplex data buses between the MLV and each component of the aircraft avionics system. It does not necessarily apply to transfers between on-board subsystems.

The signals will be transferred in the form of Asynchronous serial digital pulse code modulation using Manchester bi-phase modulation. A logic one will be transmitted as a bipolar coded signal 1/0 (i.e., a positive pulse followed by a negative pulse). A logic zero will be a bipolar coded signal 0/1 (i.e., a negative pulse followed by a positive pulse). A transition through zero occurs at the midpoint of each bit time. An absence of either pulse within a bit time is a Manchester code error. The transmission rate will be 1 MHz.

10.1 Word Types. Word size will be twenty bits as follows:

a. Three Bit Period Sync Waveform
b. Sixteen Data Bits
c. One Parity Bit

Three types of words will be used as shown in Figure 7. Each of these word types are defined in the following sections.

10.1.1 Command Word Format. Command words are always transmitted by the Bus Controller (BC). Each command word will consist of the following fields:

a. Command Sync (Bit times 1 to 3) - The command sync waveform will be an invalid Manchester waveform. The width will be three bit times, with the waveform being positive for the first one and one-half bit times, and then negative for the following one and one-half bit times. If the next bit following the sync is a logic zero, then the last half of the sync waveform will have an apparent width of two clock periods due to the Manchester encoding.

b. Terminal Address (Bit times 4 to 8, bits 11-15) - The next five bits following the sync waveform will be the RT address. The 00000 and 11111 codes will not be used for new designs, leaving a maximum of 30 addressable units per bus. The most significant bit of the address will be transmitted first. The definitions of these addresses will vary by aircraft and selected bus.

c. TR (Transmit/Receive) Bit (Bit time 9, bit 10) - The next bit following the address will be the transmit/receive bit, which will indicate the action required of the RT. A logic zero will indicate the RT is to receive, and a logic one will indicate the RT is to transmit.

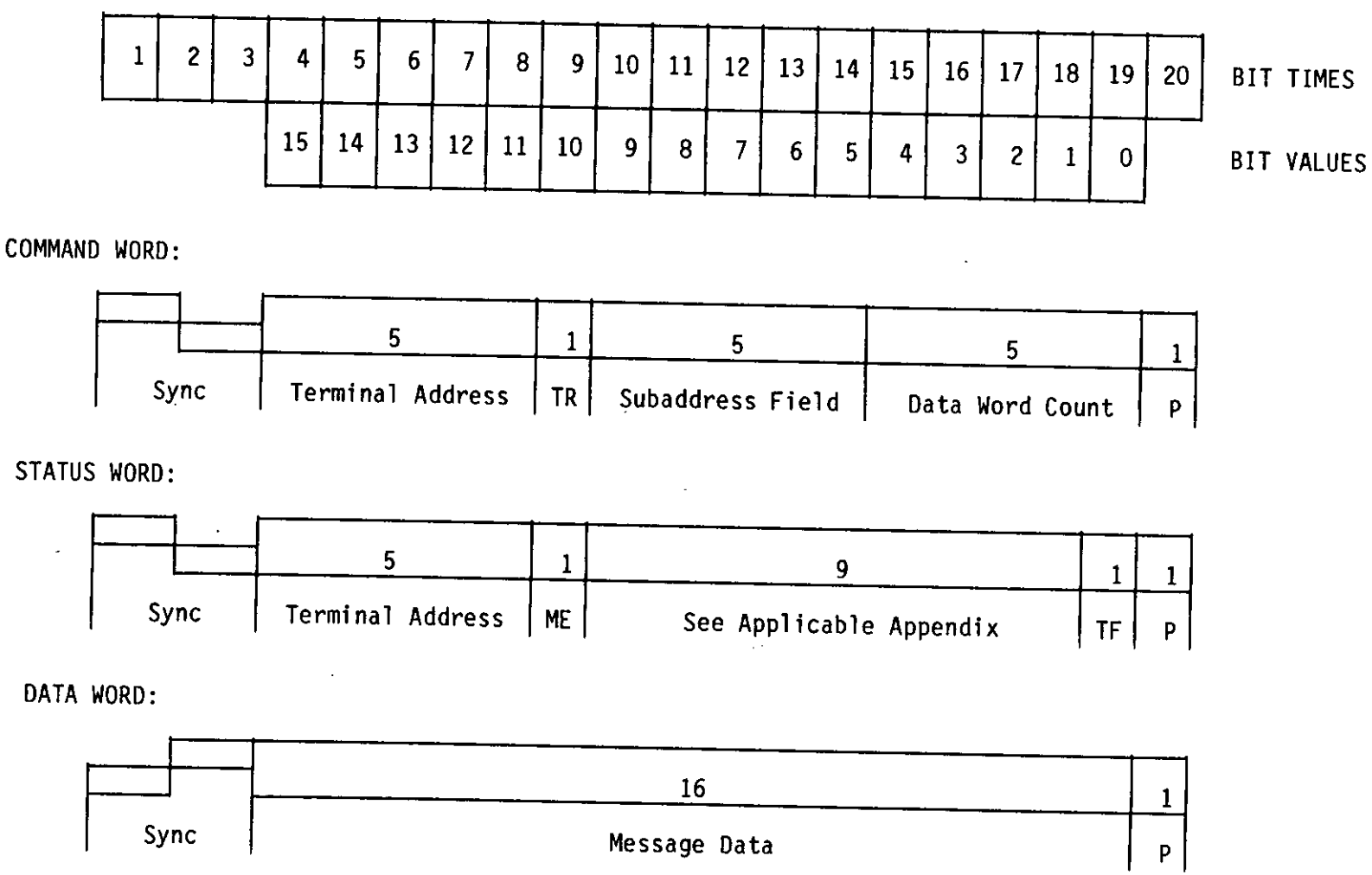


FIGURE 7. Word Formats.

d. Subaddress Field (Bit times 10 to 14, bits 5-9) - The next five bits following the transmit/receive bit will be utilized as a subaddress field. The subaddress values of 00000 and 11111 will not be used for new designs, i.e., mode commands will not be used. Subaddress 00000 (Mode Code) is used for protocols of Appendices D, E, F and G only. The subaddress used shall be as defined in the applicable appendix.

e. Data Word Count (Bit times 15 to 19, bits 0-4) - The next five bits following the subaddress field will be the number (in binary form) of data words to be either sent out or received by the RT. A maximum of 32 data words may be transmitted or received in any one message block. All 1's will indicate a decimal count of 31, and all 0's will indicate a decimal count of 32. The most significant bit of the word count will be transmitted first. In the protocol of Appendices D, E, F and G only, the Data Word Count field is also used as the Mode Code identifier.

f. P (Parity Bit) (Bit time 20) - The last bit in the word will be used for parity over the preceding sixteen bits. Odd ones parity will be utilized.

10.1.2 Status Word Format. Status words are transmitted by a Remote Terminal (RT) after receipt of a BC generated Command Word or following a BC to RT data transfer. Each status word will consist of the following fields:

a. Status Sync (Bit times 1 to 3) - The status word sync waveform will be identical to the command sync waveform described in 10.1.1.a.

b. Terminal Address (Bit times 4 to 8, bits 11-15) - The next five bits following the sync will contain the address of the terminal which is transmitting the status word as defined in 10.1.1.b.

c. ME (Message Error Bit) (Bit time 9, bit 10) - A logic one will indicate the presence of a message error, and a logic zero its absence. See the applicable appendix for usage of the Message Error bit.

d. Status Code Field (Bit times 10 to 18, bits 1-9) - The next nine bits will be used to convey RT status information to the BC. These bits are defined in the appendix for each protocol defined.

e. TF (Terminal Flag) (Bit time 19, bit 0) - Bit 0 in the status word is reserved for a terminal flag bit. This bit will be set to one to indicate that the status code field should be examined by the bus controller. See applicable appendix for usage of the Terminal Flag bit.

f. P (Parity Bit) (Bit time 20) - The last bit of the status word will be used for parity as described in 10.1.1.f.

10.1.3 Data Word Format. Sequences of up to thirty-two data words may be sent from the BC to an RT or from an RT to the BC. Each data word will consist of the following fields:

a. Data Sync (Bit times 1 to 3) - The data sync waveform will be an invalid Manchester waveform. The width will be three bit times, with the waveform being negative for the first one and one-half bit times, and then positive for the following one and one-half bit times. Note that if the bits preceding and following the sync are logic ones, then the apparent width of the sync waveform will be increased to four bit periods.

b. Message Data (Bit times 4 to 19, bits 0-15) - The sixteen bits following the sync may be used for message data transmission.

c. P (Parity Bit) (Bit time 20) - The last bit in the data word will be used for parity as described in 10.1.1.f.

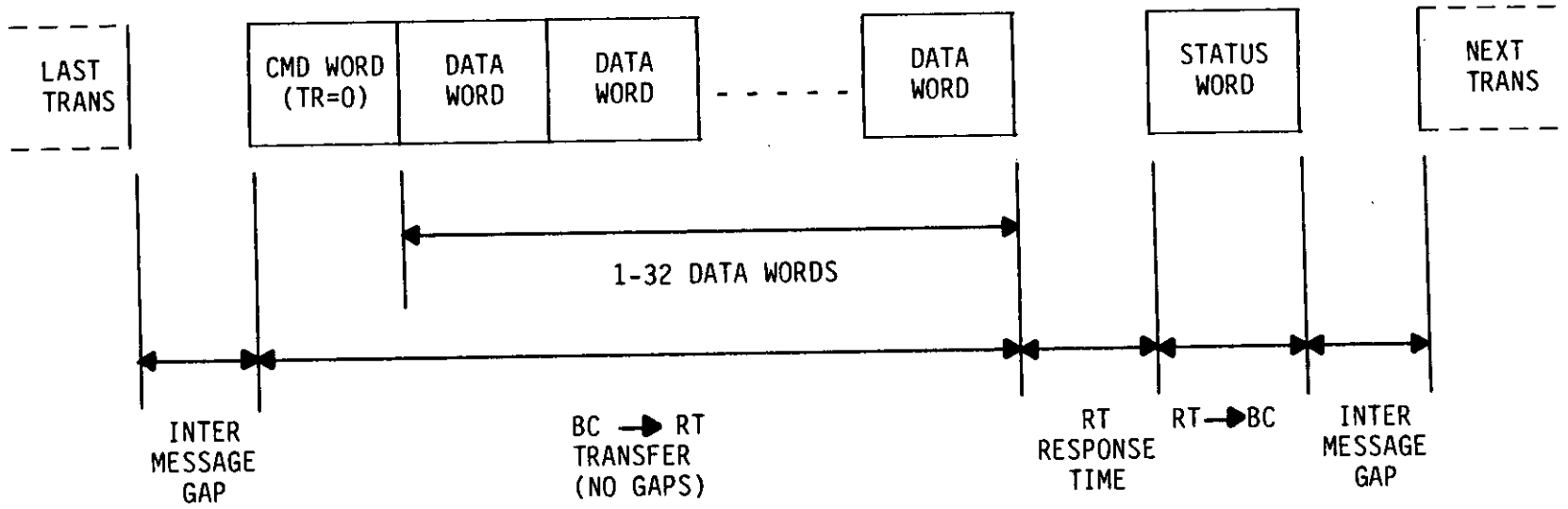
10.2 Message Formats. All messages will be transferred using a command/response mode format. Two types of message transfer sequences will be possible:

a. BC --> RT Data Transfer
b. RT --> BC Data Transfer

RT to RT transfers will not be used. Mode command transfers will not be used for new designs and are applicable only to the protocols of Appendices D, E, F and G.

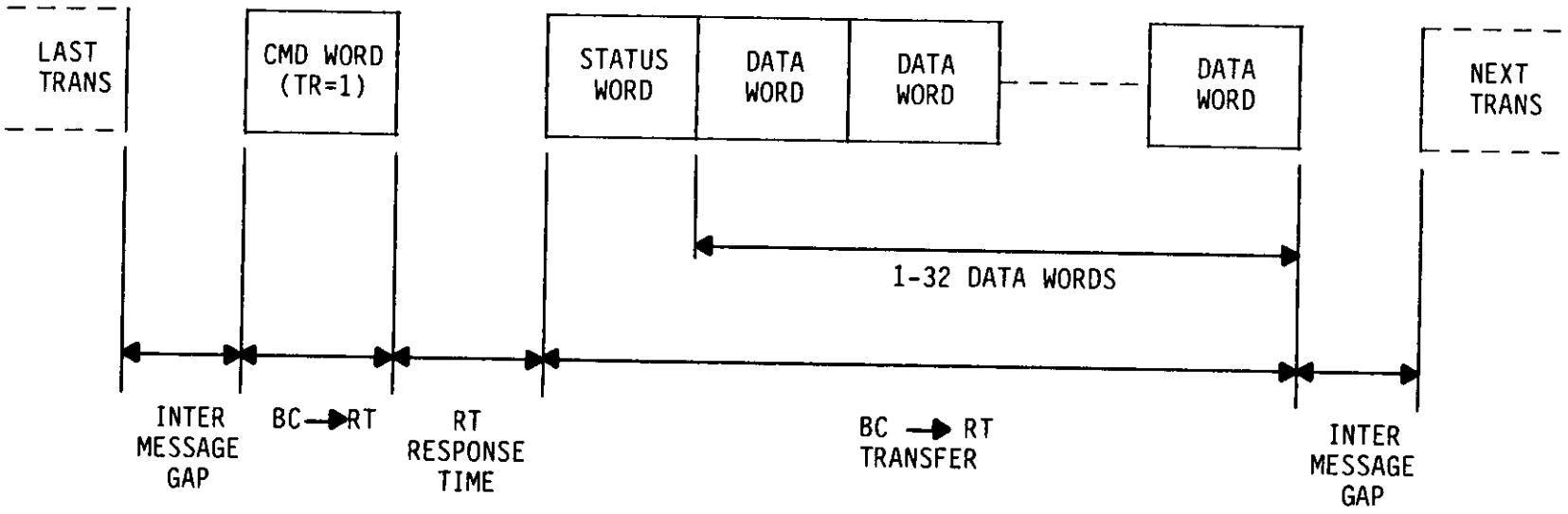
10.2.1 BC to RT Transfer Sequence. Figure 8 shows the BC to RT data transfer sequence. The BC will transmit a Command Word with its TR bit set to 0. This word will be followed immediately by from 1 to 32 Data Words also generated by the BC. There will be no gaps between any of these command or data words. The RT will respond with a Status Word (see applicable appendix for timing).

10.2.2 RT to BC Transfer Sequence. Figure 9 shows the RT to BC data transfer sequence. The BC will transmit a Command Word with its TR bit set to 1. The RT will respond with a Status Word followed with 1 to 32 Data Words. There will be no gaps between the status word or the Data Words (see applicable appendix for timing).



Note: Inter Message Gap and RT Response Times as given in each protocol appendix.

FIGURE 8. Bus Controller to Remote Terminal Data Transfer.



Note: Inter Message Gap and RT Response Times as given in each protocol appendix.

FIGURE 9. Remote Terminal to Bus Controller Data Transfer.

APPENDIX B

MESSAGE FORMATS MLV = BC

20. STANDARD PROTOCOL FOR REMOTE TERMINALS

20.1 Applicability. The protocol of this Appendix is applicable to all new designs for Remote Terminals and Bus Controllers. (Bus Controller reverts to Remote Terminal for reprogramming.)

20.2 General Operation. The MLV will reprogram each unit in the following manner (see Figure 10).

a. When indicated as usable in the Lookup Table, the MLV will request a Memory Configuration Message from the unit being processed. The Memory Configuration will describe the current memory contents for one or two memory areas as applicable. The MLV will compare the received Memory Configuration to the current Memory Configuration stored on the MLV Memory Storage Device (MSD). In automatic mode, if the unit already contains the current Memory Configuration, the MLV will then continue on to the next unit to be processed. If the Memory Configuration Message was not usable, the MLV will assume that the unit requires reprogramming. In Manual Mode, the MLV will display the Memory Configuration data and continue reprogramming for the selected unit.

b. If the unit in process requires reprogramming of either or both memory areas, the MLV will check the old and new memory configurations to determine if the information in the MLV MSD is compatible with updating the old memory (will use the patch file if it exists). If a patch file does not exist or is not usable, the MLV will check to see if a complete file exists and check if it will result in a newer revision level. If the Configuration Message was not usable, no patch file should exist (see 5.2.2.1.2) and the MLV will use the complete file for reprogramming. The MLV will declare an error if the MSD information is insufficient. If the MSD information is correct for reprogramming, the MLV will then send a Reprogram Control Message to enable the reprogramming function for the appropriate Memory Area(s) (depending on unit requirements memory areas will be enabled simultaneously or sequentially). The unit will then check the validity of the Reprogram Control Message utilizing internally stored information and the Reprogram Enable discrete(s) if applicable.

c. Once the reprogramming mode is entered, the MLV will then proceed to load the new memory contents in blocks of varying size depending on the unit and update requirements. There will be no specific erasure commands from the MLV. The unit being reprogrammed will be responsible for erasure based on the directed write information. The reprogramming will be conducted by a series of one or more HEADER MESSAGE, MEMORY DATA LOAD MESSAGE, ..., MEMORY DATA LOAD MESSAGE,

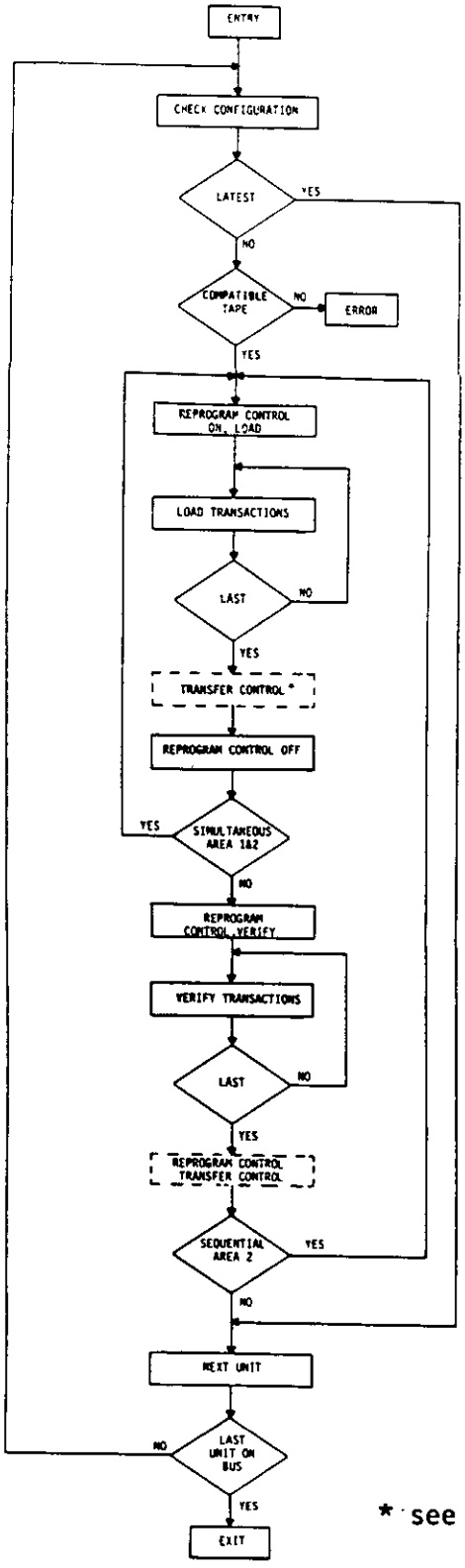


FIGURE 10. Avionics Subsystem = RT Load/Verify Procedure.

TRAILER MESSAGE transactions. If required, a HEADER MESSAGE, TRAILER MESSAGE transaction will also be present for paging or transfer of control functions. If the unit being reprogrammed is required to keep track of how many times a particular memory device has been reprogrammed, the device being reprogrammed shall declare an Abort error (Reprogram Status Message) if the predetermined memory write capability has been exceeded. The storage of this information within the unit memory shall not affect the validity of the memory verify function (i.e., the unit being reprogrammed shall mask out this information during the Verify operation).

d. After completion of the load the MLV will, if required, then provide transfer of control information to the unit using a HEADER MESSAGE, TRAILER MESSAGE transaction. Transfer control prior to a Verify via the Reprogram Control Message is not permitted as discussed in 6.1.j. The transfer of control prior to a verify shall not be used to transfer control to a memory area that has been loaded but not verified. If it is necessary to transfer control prior to the completion of a memory area Load/Verify, the two parts of the memory area will be loaded/verified separately using the same technique as for sequentially loading Memory Areas 1 and 2. The transfer of control via the Header Message may be inhibited during the load as discussed in 6.1.m.

e. After all required data for a particular memory area have been transferred the MLV will, via the Reprogram Control Message, disable the reprogramming function for that memory area.

f. When simultaneous reprogramming of Memory Areas 1 and 2 is utilized, the MLV will load the second memory area prior to the verify operation. When sequential (or single Memory Area) reprogramming is utilized, the MLV will at this time verify the previously loaded memory area prior to the Memory Area 2 load operation. The MLV will perform the memory verify utilizing the same transactions that were used for the memory load except that the MLV will receive the data from the unit being reprogrammed and compare the received data with the stored MSD data. The automatic verify after a load may be inhibited as discussed in 6.1.g.

g. After completion of the verify the MLV will, if required, then provide transfer of control information to the unit using either a HEADER MESSAGE, TRAILER MESSAGE transaction or via the Reprogram Control Message. When sequential reprogramming of Memory Areas 1 and 2 is utilized, the MLV will at this time repeat the Load/Verify operations for the second memory area.

h. Assuming there were no errors, the MLV will continue on to process the next unit on the bus or the next bus as appropriate. If an error did occur, operator intervention would be requested by the MLV fault display.

20.3 Status Response Word: MLV = BC.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
S	TERMINAL ADDRESS					ME		SR					BSY			TF
	Y	Y	Y	Y	Y	X	X	X	X	X	X	X		X	X	

A STATUS RESPONSE WORD will be provided by the RT for each message transaction. The STATUS RESPONSE WORD will follow the data on an RT receive type transaction and will precede the data on an RT transmit type transaction. The MLV will allow a response time gap of 12 usec from the end of the last transmitted COMMAND WORD (transmit type message) or the end of the last transmitted DATA WORD (receive type message), to the start of the RT STATUS RESPONSE WORD before declaring a no response error (Equivalent of 14 usec when measured in accordance with MIL-STD-1553B). Under normal conditions the RT shall begin the STATUS RESPONSE WORD within the period of 2-10 usec from the receipt of the end of the last COMMAND WORD (transmit type message) or the receipt of the end of the last DATA WORD (receive type message) (Equivalent of 4-12 usec when measured in accordance with MIL-STD-1553B). The MLV will ensure that the time from the end of the RT transmission of the last DATA WORD (transmit type message) or the end of the last STATUS RESPONSE WORD (receive type message) to the beginning of the next COMMAND WORD is at least 8 usec (equivalent of 10 usec when measured in accordance with MIL-STD-1553B). The STATUS RESPONSE WORD bits are as follows:

a. TERMINAL ADDRESS (bits 11-15). The RT address will be the normal RT address of the unit being reprogrammed. The RT address will be determined by the Aircraft Type and Aircraft Configuration Modification information provided to the MLV and based on the particular bus selected by the MLV switching network for all units including the normal Bus Controller. Throughout the remainder of this appendix the RT address of the unit being reprogrammed will be referred to as YYYYY.

b. ME bit (bit 10). The Message Error (ME) bit may be set by the RT under the following conditions.

   1. The STATUS RESPONSE WORD following a COMMAND WORD requesting an undefined subaddress Transmit/Receive combination may result in bit 10 = 1 for that STATUS RESPONSE WORD. If an RT transmission was requested, the data words requested may or may not be present.

   2. The STATUS RESPONSE WORD for the next COMMAND WORD after a receive type message may result in bit 10 = 1 if the data received in the previous message: was short in data word count;

failed to pass word validation; had an improperly timed data sync; or had non-contiguous data.

The ME bit, if set, will be set once for a message error and then cleared for the next message if there was no subsequent error. The ME bit will not be utilized by the MLV; thus, the bit may be 0 or 1.

c. SR bit (bit 8). The Service Request (SR) bit will not be utilized by the MLV; thus, the bit may be 0 or 1.

d. BSY (BUSY) bit (bit 3). The BUSY bit will be utilized by the MLV if it is set. If the unit being reprogrammed is compatible with setting the BUSY bit, the setting of this bit to 1 will indicate to the MLV that it is necessary to suspend or slow down communications. The first STATUS RESPONSE WORD received by the MLV with the BUSY bit set shall cause the MLV to send only Activity Messages (normally every 10 msec) until the BUSY bit is cleared. As long as the BUSY bit is clear in the STATUS RESPONSE WORD from a compatible RT, the MLV will assume that the RT can support a continuous stream of identical messages with 2 msec from the end of one message to the start of the next COMMAND WORD. The continuous stream of identical messages is assumed to be either Memory Data Load or Memory Data Verify messages. The continuous stream will be sustained only for a period compatible with the MLV Memory Storage Device and internal memory capabilities. As a minimum, the MLV shall be capable of transferring 2K data words (in Memory Data Load or Memory Data Verify Messages) per second when the RT does not indicate busy during the transfer. Any DATA WORDS transmitted after a STATUS WORD with the BUSY bit set will be ignored by the MLV. If the RT being reprogrammed cannot set the BUSY bit in the RT STATUS RESPONSE WORD, then prior to each non Activity Message transmission the MLV will command an Activity Message from the RT and inspect the BUSY bit in the DATA WORD following the STATUS RESPONSE WORD to determine if the RT is ready to communicate.

The operation of the MLV after the BUSY bit has been set and then cleared will vary depending on RT operation.

1. If the BUSY bit was set in the STATUS RESPONSE WORD for a transmit type command, after the BUSY bit is cleared (in the response to the Activity Message) the last transmit command will be repeated so the MLV can receive the DATA WORD(s) that were ignored when the BUSY bit was set.

2. If the BUSY bit was set in the DATA WORD of the Activity Message (only applicable when the BUSY bit is not set in the STATUS RESPONSE WORD), the DATA WORD for the first Activity Message with the BUSY bit cleared will be processed normally.

3. If the BUSY bit is set in the STATUS RESPONSE WORD for a receive type command, then two options (selectable by terminal) will be allowed.

(a) The MLV will assume that the DATA WORD(s) were not received by the RT and when the BUSY bit is cleared (in the STATUS RESPONSE WORD for the Activity Message) the last receive message will be repeated.

(b) The MLV will assume that the DATA WORD(s) were received by the RT and when the BUSY bit is cleared (in the STATUS RESPONSE WORD for the Activity Message) the last receive message will not be repeated.

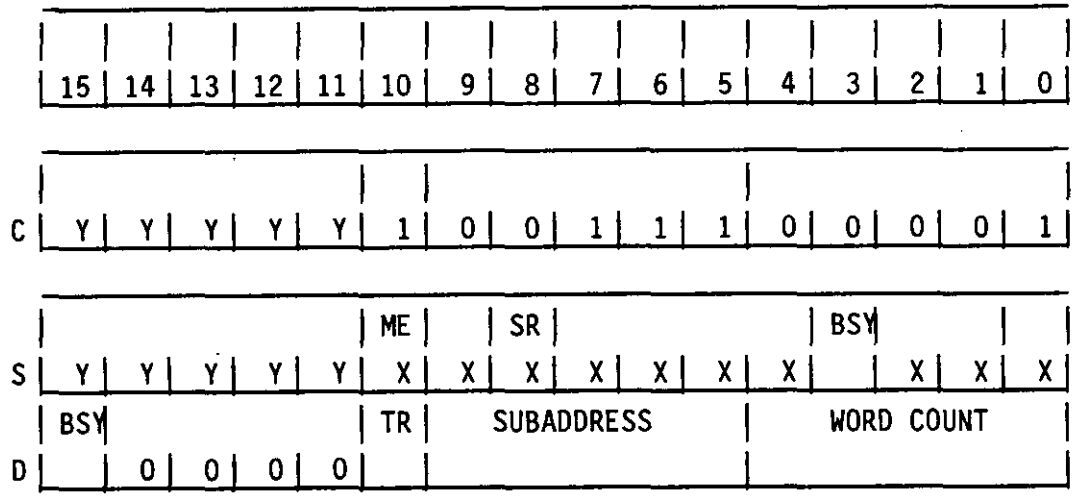
e. TF bit (bit 0). The Terminal Flag (TF) bit will not be utilized by the MLV; thus, the bit may be 1 or 0.

f. Other bits. Bits 9, 7, 6, 5, 4, 2 and 1 will not be utilized by the MLV; thus, these bits may be 1 or 0.

20.4 Messages.

20.4.1 Activity: MLV = BC: TR = 1: SUBADDRESS = 07H.

20.4.1.1 Activity Message Bus Data.



20.4.1.1.1 Activity Message Utilization. This message will be utilized by the BC (MLV) to determine whether the remote terminal is ready to receive data and will allow the RT to request to send information to the BC or receive information from the BC.

20.4.1.1.2 Status Word. The status word response to the Activity Message shall be as defined for the STATUS RESPONSE WORD (see 20.3) and shall utilize bits 3 and 8 as follows:

a. SR bit (bit 8). The SR bit will not be utilized by the MLV; thus, the bit may be 0 or 1. The MLV will determine that the RT wishes to enact a message transaction based on the fact that the contents of bits 0 through 10 of the data word that follows is non-zero.

b. BSY (BUSY) bit (bit 3). The BUSY bit if set will be used to indicate that the RT is not ready to process any message from the MLV other than the Activity Message. Prior to the transmission of any other type messages to the RT, the MLV will continue to send Activity Messages (normally every 10 msec) to the RT until the BUSY bit is cleared, or a Reprogram Status Message is requested. The MLV will respond to the BUSY bit (bit 15) in the data word that follows only when the BUSY bit in the status word is not set.

20.4.1.2 Data Words.

20.4.1.2.1 Data Word 1. The MLV will ignore the DATA WORD of the Activity Message when the BUSY bit is set in the STATUS RESPONSE WORD; thus, the RT need not transmit the DATA WORD. (Should not for MIL-STD-1553B terminals.)

a. BSY (BUSY) bit (bit 15). The BUSY bit in the data word for the Activity Message shall function identically to the BUSY bit in the status word (bit 3) described above. This bit is provided to accommodate an RT that does not utilize bit 3 of the status word to indicate busy. The BUSY bit and the RT Request Bits (bits 0-10) will not be set simultaneously unless the RT requires sending a Reprogram Status Message to the MLV. The BUSY bit need not be set in order to send a Reprogram Status Message. The MLV will not honor the Reprogram Status Message request until an Activity Message containing the request with the BUSY bit clear is received.

b. RT Request Bits (bits 0-10). Bits zero through 10 shall be utilized to allow the RT to request that the MLV send a specific command to the RT. As a result of the RT request, the MLV will transmit a COMMAND WORD with the RT terminal address in bits 11 through 15 and the contents of the activity message RT Request Bits in bits 0-10.

1. TR bit (bit 10). The TR bit will be set to 1 if the RT wishes to transmit a message and will be set to 0 if the RT wishes to receive a message.

2. SUBADDRESS bits (bits 5-9). The subaddress bits will indicate the subaddress of the desired message.

3. WORD COUNT bits (bits 0-4). The word count bits will indicate the data word count for the desired message.

c. Other bits (bits 11-14). Bits 11-14 shall equal 0.

20.4.1.3 Activity Messages Prior to Beginning a Load/Verify or Verify. After the setting of the discretes and expiration of the 10 msec wait period, the first message(s) commanded by the MLV will be Activity Messages regardless of whether or not the Lookup Table for the unit indicates that Activity Messages are required for every transaction. Bits 11-14 of the Activity Message DATA WORD are never used by the MLV. The information received in bits 0-10 of the DATA WORD for all Activity Messages commanded before the first Reprogram Control Message will be ignored by the MLV. This operation is implemented to permit use of the normal Activity Message subaddress for other uses when reprogramming is not underway. (i.e., the MLV will only assume the Activity Message data is valid after reprogramming has begun, namely by setting of discretes and receipt of a valid Reprogram Control Message.) The information received in bit 15 of the DATA WORD for all Activity Messages commanded before the Reprogram Control Message will only be used if the Lookup Table for the unit indicates that Activity Messages are required for every transaction and the busy bit is not set in the STATUS WORD response to the Activity Message. In this case the remote terminal must ensure that bit 15 of the DATA WORD is

valid or set to zero prior to receipt of the Reprogram Control Message. In manual mode, if the unit Lookup Table indicates that Memory Configuration Messages are supported, then there will be a Memory Configuration Message commanded before the Reprogram Control Message and the MLV will expect valid Memory Configuration data. Ignoring the Activity Message DATA WORD bits 0-14 will preclude an RT from sending a Reprogram Status Message prior to receipt of the Reprogram Control Message; however, a Reprogram Status Message would not be valid before reprogramming was initiated. An RT should not request this message until after the Reprogram Control Message is received.

20.4.2 Memory Configuration: MLV = BC: TR = 1: SUBADDRESS = 13H.

20.4.2.1 Memory Configuration Bus Data.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ACTIVITY MESSAGE																
C	Y	Y	Y	Y	Y	1	0	0	1	1	1	0	0	0	0	1
S	Y	Y	Y	Y	Y	X	X	X	X	X	X	X	0	X	X	X
D	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
MEMORY CONFIGURATION MESSAGE																
C	Y	Y	Y	Y	Y	1	1	0	0	1	1	0	0	0	1	0
S	Y	Y	Y	Y	Y	ME	X	X	X	X	X	X	BSY	X	X	X
D1	MEMORY AREA 1 CONFIGURATION															
D2	MEMORY AREA 2 CONFIGURATION															

The DATA WORD in the Activity Message shown prior to the Memory Configuration will only be processed when the MLV is required to check the BUSY bit status of RTs that do not use the BUSY bit in the STATUS RESPONSE WORD.

20.4.2.1.1 Memory Configuration Message Utilization. This message is utilized to read the current memory configuration of the unit. This message is only used when its use is indicated in the Lookup Table.

20.4.2.2 Data Words.

20.4.2.2.1 Data Word 1. Memory Area 1 Configuration (bits 0-15). The data shall be in individual unit format and shall represent the configuration of the data stored in Memory Area 1. Unused bits shall equal zero. In automatic mode this message is used for the purpose of comparing the unit configuration stored on the MSD with reported unit configuration. The MLV will assume that the largest numerical value (MSD vs. reported) indicated by bits 0-15 is the latest configuration.

20.4.2.2.2 Data Word 2. Memory Area 2 Configuration (bits 0-15). The data shall be in individual unit format and shall represent the configuration of the data stored in Memory Area 2. Unused bits (including equipments that do not utilize Memory Area 2) shall equal 0. In automatic mode this message is used for the purpose of comparing the unit configuration stored on the MSD with reported unit configuration. The MLV will assume that the largest numerical value (MSD vs. reported) indicated by bits 0-15 is the latest configuration.

20.4.3 Reprogram Control: MLV = BC: TR = 0: SUBADDRESS = 1DH.

20.4.3.1 Reprogram Control Bus Data.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ACTIVITY MESSAGE																
C	Y	Y	Y	Y	Y	1	0	0	1	1	1	0	0	0	0	1
S	Y	Y	Y	Y	Y	X	X	X	X	X	X	X	0	X	X	X
D	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
REPROGRAM CONTROL MESSAGE																
C	Y	Y	Y	Y	Y	0	1	1	1	0	1	0	0	1	0	0
D1	TYPE								TYPE							
D2	NUMBER								NUMBER							
D3	NUMBER								NUMBER							
D4	FILL						L/V		CONTROL CODE							
S	Y	Y	Y	Y	Y	ME	X	X	X	X	X	X	BSY	X	X	X

For the first Reprogram Control Message the DATA WORD in the Activity Message shown prior to the Reprogram Control will only be processed when the MLV is required to check the BUSY bit status of RTs that do not use the BUSY bit in the STATUS RESPONSE WORD and in this case bits 14-0 will be ignored.

20.4.3.1.1 Reprogram Control Message Utilization. The Reprogram Control message shall provide a key for entering/leaving the reprogramming mode. For units utilizing Reprogram Enable discretes the Reprogram Control Message shall have no effect on the receiving unit if the appropriate Reprogram Enable discrete is not present. Each field in the data shall be checked by the RT for compliance with the following prior to execution of the Reprogram Control Code. The Type and Number fields shall be based on WRA nomenclature (e.g., RT-1079); however, if this creates a conflict, the system nomenclature (e.g., ALQ-126) shall be utilized instead.

20.4.3.2 Data Words.

20.4.3.2.1 Data Word 1. Type (bits 0-15). The type field shall be made up of the first two 8 bit ASCII characters that represent the nomenclature of the unit being controlled. For example, for RT-1079 the two characters would be "R," "T."

20.4.3.2.2 Data Word 2. Number (bits 0-15). The number field shall be made up of the third and fourth 8 bit ASCII characters that represent the nomenclature of the unit being controlled. For example, for RT-1079 the two characters would be "1," "0" (zero).

20.4.3.2.3 Data Word 3. Number (bits 0-15). The number field shall be made up of the last two 8 bit ASCII characters that represent the nomenclature of the unit being controlled. For example, for RT-1079 the two characters would be "7," "9."

20.4.3.2.4 Data Word 4.

a. Fill (bits 10-15). The fill field may be any bit pattern including 0 and is to be defined by the individual equipment being controlled. The fill field shall be checked even if the field is defined as 0.

b. L/V (bits 8-9). The Load/Verify (L/V) bits are used to describe whether a Load, Verify, or other type transaction will follow. These bits are coded as follows:

    L/V = 01 A Memory Load follows
    L/V = 10 A Memory Verify follows
    L/V = 11 Not used
    L/V = 00 Reprogram Control Message is being sent for some reason other than loading/verifying (e.g., to quiet the BC, etc.)

c. Control Code (bits 0-7)

    BIT 7 Reprogram Enable 1 = 80H
    BIT 6 Reprogram Enable 2 = 40H
    BIT 5 Reprogram Disable 1 = 20H
    BIT 4 Reprogram Disable 2 = 10H

BIT 3 BC convert to RT = 08H
BIT 2 BC stop transmitting/receiving on bus = 04H
BIT 1 RT revert to BC = 02H
BIT 0 Execute from Program Entry Address supplied previously in Header Message Data Word 3/Data Word 4 = 01H

20.4.3.2.4.1 Control Code Processing.

20.4.3.2.4.1.1 Field Validity. The Control Code field shall be valid only if all other fields are correct and only if either the Avionics Reprogram Enable 1/EW UDM Reprogram Enable discrete or the Avionics Reprogram Enable 2/EW OSM Reprogram Enable discrete is present. At the end of reprogramming, the MLV will maintain the active discrete for at least 100 msec after the transmission of the Reprogram Control Message that ends the reprogramming mode.

20.4.3.2.4.1.2 Valid Control Codes. The following are the only valid Control Codes that can occur when the MLV is the BC. Any other code shall cause the RT to not execute the Reprogram Control Code.

a. Code 00000000 = 00H - this code shall indicate no reprogram control action is to be taken (code 00H used when Verify operation is indicated).

b. Code 00000001 = 01H - this code shall cause the RT to begin execution starting at the address previously supplied via Data Word 3/ Data Word 4 of the Header Message.

c. Code 00000010 = 02H - this code shall cause the RT to revert back to a BC. Upon execution of this Reprogram Control Code the message traffic shall be as defined in Appendix C (MLV = RT).

d. Code 00010000 = 10H - this code shall cause the RT to exit the reprogramming mode for Memory Area 2. This code shall only be valid if the Avionics Reprogram Enable 2/EW OSM Reprogram Enable discrete is active, or when only one enable is utilized, this code shall apply only if the enable is present. The presence or absence of the Avionics Reprogram Enable 1/EW UDM Reprogram Enable discrete shall not affect the validity of this code when both enables are used.

e. Code 00100000 = 20H - this code shall cause the RT to exit the reprogramming mode for Memory Area 1. This code shall only be valid if the Avionics Reprogram Enable 1/EW UDM Reprogram Enable discrete is active, or when only one enable is utilized, this code shall apply only if the enable is present. The presence or absence of the Avionics Reprogram Enable 2/EW OSM Reprogram Enable discrete shall have no affect on the validity of this code when both enables are used.

f. Code 00110000 = 30H - combination of 10H and 20H for simultaneous Memory Areas 1 and 2 exit reprogramming mode. (Both Reprogram Enables must be present if both Reprogram Enables are incorporated.)

g. Code 01000000 = 40H - this code shall cause the RT to enter the reprogramming mode for Memory Area 2. This code shall only be valid if the Avionics Reprogram Enable 2/EW OSM Reprogram Enable discrete is active, or when only one enable is utilized, this code shall apply only if the enable is present. The presence or absence of the Avionics Reprogram Enable 1/EW UDM Reprogram Enable discrete shall not affect the validity of this code when both enables are used.

h. Code 10000000 = 80H - this code shall cause the RT to enter the reprogramming mode for Memory Area 1. This code shall only be valid if the Avionics Reprogram Enable 1/EW UDM Reprogram Enable discrete is active, or when only one enable is utilized, this code shall apply only if the enable is present. The presence or absence of the Avionics Reprogram Enable 2/EW OSM Reprogram Enable discrete shall not affect the validity of this code when both enables are used.

i. Code 11000000 = C0H - combination of 40H and 80H for simultaneous Memory Areas 1 and 2 enter reprogramming mode. (Both Reprogram Enables must be present if both Reprogram Enables are incorporated.)

20.4.4 Header: MLV = BC: TR = 0: SUBADDRESS = 14H.

20.4.4.1 Header Bus Data.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ACTIVITY MESSAGE																
C	Y	Y	Y	Y	Y	1	0	0	1	1	1	0	0	0	0	1
S	Y	Y	Y	Y	Y	X	X	X	X	X	X	X	0	X	X	X
D	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
HEADER MESSAGE																
C	Y	Y	Y	Y	Y	0	1	0	1	0	0	0	0	1	0	0
D1	TM		HT		BUFFER TRANSFER COUNT											
D2	INITIAL LOAD ADDRESS															
D3	PROGRAM ENTRY ADDRESS															
D4	PAGE NUMBER													0	TC	
S	Y	Y	Y	Y	Y	ME	X	X	X	X	X	X	BSY	X	X	X

The Activity Message shown prior to the HEADER will only be present when the MLV is required to check the BUSY status of RTs that do not use the BUSY bit in the STATUS RESPONSE WORD.

20.4.4.1.1 Header Message Utilization. This message is used to pass Load/Verify parameters to the unit.

20.4.4.2 Data Words.

20.4.4.2.1 Data Word 1.

a. TM (bits 14-15). The Transfer Mode (TM) bits are used to describe the Memory Data Load or Memory Data Verify DATA WORD content. The TM bits are binary coded as follows:

1. TM = 00 No transfer. In the No Transfer Mode the Buffer Transfer Count and Initial Load Address have no meaning. This mode is used to transfer the Program Entry Address and Page Number or is used as a preamble to the Trailer Message.

2. TM = 01 8 bit transfer. Each 16 bits of data transmitted in a DATA WORD will contain only 8 bits of information in bits 0-7.

3. TM = 10 16 bit transfer. Each 16 bits of data transmitted in a DATA WORD will contain 16 bits of information in bits 0-15.

4. TM = 11 32 bit transfer. The 16 bits of data transmitted in each odd word (first is odd) contains the 16 LSBs of data in bits 0-15 and each even word (second is even) contains the 16 MSBs of data in bits 0-15.

b. HT (bits 12-13). The Header Type (HT) bits are used to describe the Header. The Header Type has no meaning when the Transfer Mode is 00. The HT bits are binary coded as follows:

1. HT = 00 Normal Header. (Buffer Transfer Count equals number of words.)

2. HT = 01 Normal Header. (Buffer Transfer Count equals number of messages.)

3. HT = 10 Undefined.

4. HT = 11 Reserved for internal MLV use. This type of Header will not be transmitted on the bus.

c. Buffer Transfer Count (bits 0-11). The Buffer Transfer Count is used to indicate the amount of data that will follow the Header Message. The Buffer Transfer Count has no meaning when the Transfer Mode is 00. The range of the Buffer Transfer Count is 1 to 4096 (value of 0 = 4096).

1. For HT = 00, the Buffer Transfer Count is the total number of DATA WORDS that will be transmitted after the Header. The DATA WORDS will be transmitted in 32-word messages with the last message containing 1 to 32 DATA WORDS. The maximum transfer for HT = 00 is 4096 words using 128 Memory Data Load or Memory Data Verify Messages.

2. For HT = 01, the Buffer Transfer Count is the number of Memory Data Load or Memory Data Verify messages that will follow the HEADER. Thus, the maximum data transfer per Header Message is 4096 x 32 DATA WORDS (per Memory Data Load or Memory Data Verify Message) which equals 131,072 16 bit words (128K). If paging is utilized for transfer modes 01 or 10 (see 20.4.4.2.4), the maximum value of the Buffer Count will be 2048. (Yields 65,536 16 bit data words (64K) for transfer modes 01 and 10 using paging.)

20.4.4.2.2 Data Word 2.

a. Initial Load Address (bits 0-15). The Initial Load Address is the 16 or less LSB of the point in memory into which data is to be loaded or read. The maximum value (number of bits) used in the Initial Load Address will be compatible with the page size of units using paging. Unused bits shall equal 0.

20.4.4.2.3 Data Word 3.

a. Program Entry Address (bits 0-15). The Program Entry Address has meaning only for Transfer Mode = 00. The Program Entry Address is the 16 or less LSB of the point in memory at which the unit being reprogrammed is to begin execution after receipt of the Execute command in the Reprogram Control Message (only used for units requiring this command) or when a Transfer Control is indicated in DATA WORD 4. The maximum value (number of bits) used in the Program Entry Address will be compatible with the page size of units using paging. Unused bits shall equal 0.

20.4.4.2.4 Data Word 4.

a. Page Number (bits 3-15). The Page Number represents up to 13 MSB bits for paged memory address. The Page Number applies to the Program Entry Address for Transfer Mode = 00. The Page Number applies to the Initial Load Address for Transfer Mode = 01, 10, or 11. Unused bits shall equal 0.

b. TC bits (0-1). The Transfer Control (TC) may be used to transfer control to the loaded program after a verify or to an unaltered memory area after a load.

1. Transfer Control = 00 indicates this is the last HEADER, MEMORY DATA, ..., MEMORY DATA, TRAILER or HEADER, TRAILER transaction.

2. Transfer Control = 01 indicates that more data is to follow the current HEADER, MEMORY DATA, ..., MEMORY DATA, TRAILER or HEADER, TRAILER transaction and control should not be transferred. For units using paging and the Program Entry Address, the TC will remain = 01, even for the last data transaction, until a Transfer Mode = 00 message is used to supply the Program Entry Address and Page Number.

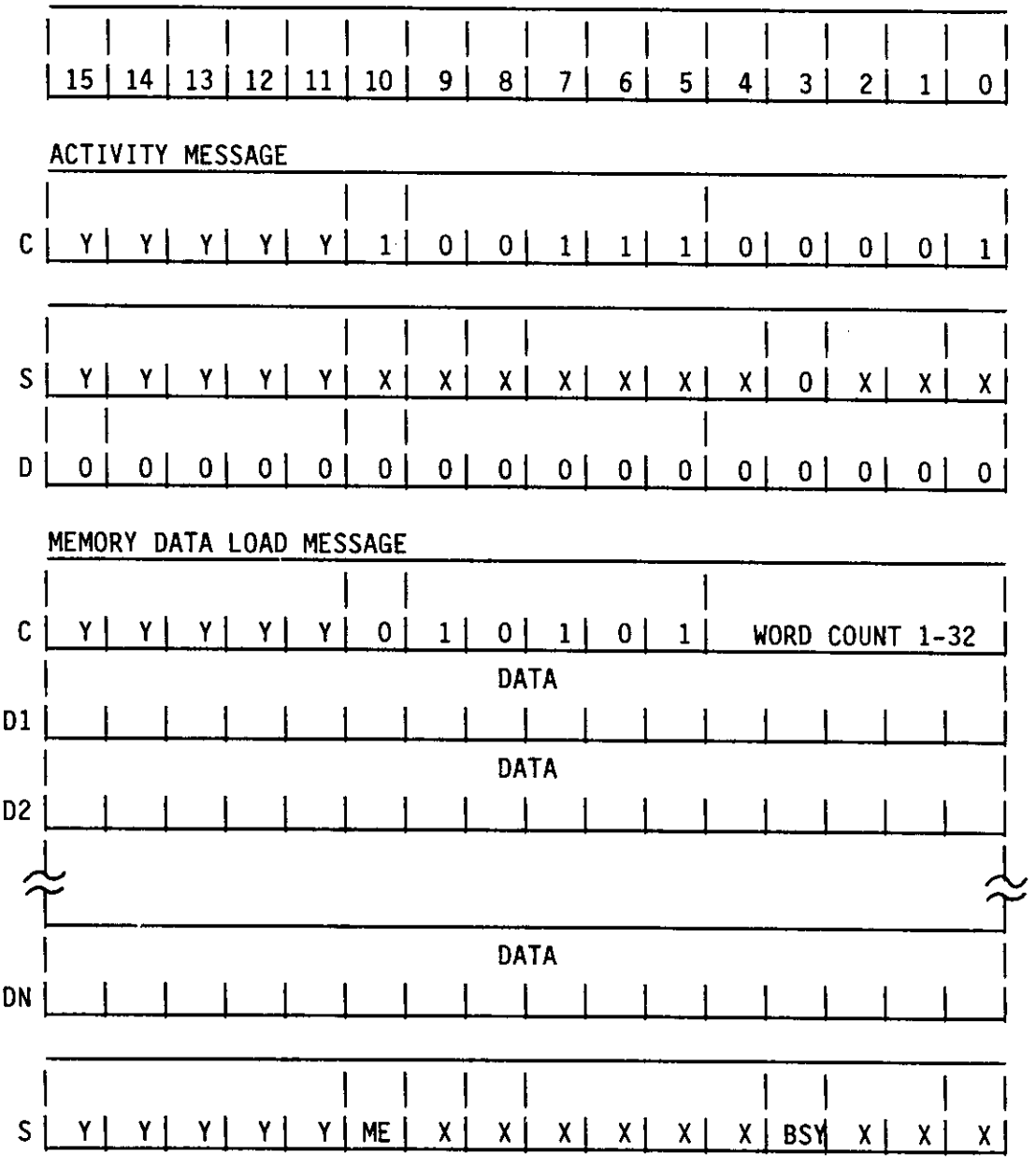
3. Transfer Control = 10 shall indicate that control is to be transferred to the Program Entry Address. When control is transferred, the action shall not take place until after the Trailer Message and shall transfer control only to non reprogrammed areas or verified areas.

4. Transfer Control = 11 is invalid.

c. Other Bits (bit 2). Bit 2 shall equal 0.

20.4.5 Memory Data Load: MLV = BC: TR = 0: SUBADDRESS = 15H.

20.4.5.1 Memory Data Load Bus Data.



The Activity Message shown prior to the Memory Data Load will normally only be present when the MLV is required to check the BUSY bit status of RTs that do not use the BUSY bit in the STATUS RESPONSE WORD.

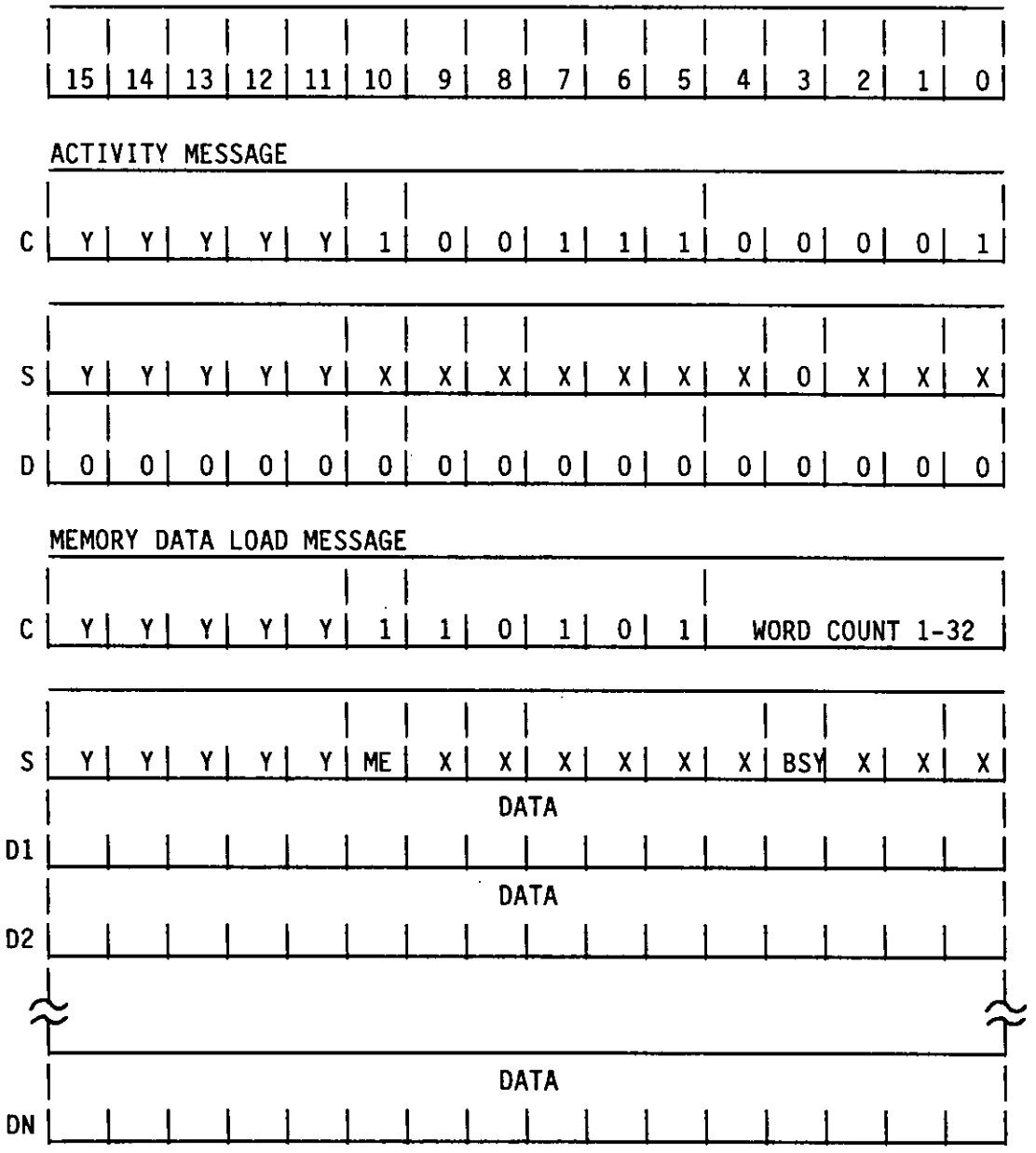
20.4.5.1.1 Memory Data Load Message Utilization. This message is used to pass the data to be loaded into the unit memory.

20.4.5.1.1.1 BUSY Bit. If the BUSY bit had been set in the STATUS RESPONSE WORD for a Memory Data Load Message and the RT was of the type that required retransmission of the message, the Memory Data Load Message for which the BUSY bit had previously been set would be repeated after the BUSY bit in the Activity Message had been cleared.

20.4.5.2 Data Words. The number of Data Words will equal the WORD COUNT in the Memory Data Load Message COMMAND WORD.

20.4.6 Memory Data Verify: MLV = BC: TR = 1: SUBADDRESS = 15H.

20.4.6.1 Memory Data Verify Bus Data.



The Activity Message shown prior to the Memory Data Verify will normally only be present when the MLV is required to check the BUSY bit status of RTs that do not use the BUSY bit in the STATUS RESPONSE WORD.

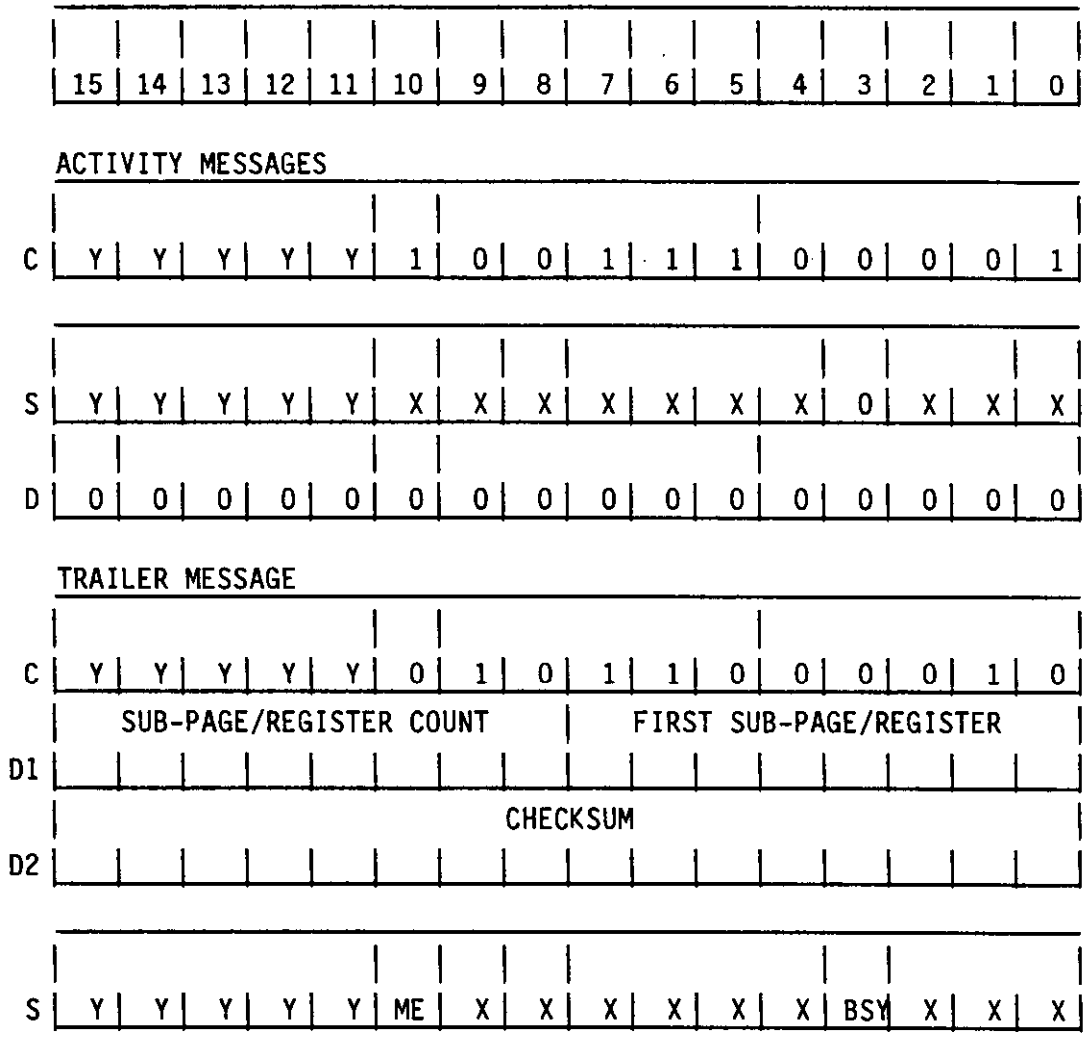
20.4.6.1.1 Memory Data Verify Message Utilization. This message is used to pass the data that the MLV will compare to the data stored on the MSD.

20.4.6.1.1.1 BUSY Bit. If the BUSY bit had been set in the STATUS RESPONSE WORD for a Memory Data Verify Message, then any DATA WORDs transmitted by the RT would have been ignored. After the BUSY bit is cleared in the STATUS WORD RESPONSE for the Activity Message, the MLV will recommand the Memory Data Verify Message. The RT shall ensure that the DATA WORD(s) transmitted are for the Memory Data Verify Message for which the BUSY bit was set, even if the DATA WORD(s) were previously transmitted.

20.4.6.2 Data Words. The number of Data Words will equal the WORD COUNT in the Memory Data Verify Message COMMAND WORD.

20.4.7 Trailer: MLV = BC: TR = 0: SUBADDRESS = 16H.

20.4.7.1 Trailer Bus Data.



The Activity Message shown prior to the TRAILER will only be present when the MLV is required to check the BUSY bit status of RTs that do not use the BUSY bit in the STATUS RESPONSE WORD.

20.4.7.1.1 Trailer Messge Utilization. This message is used to pass the data checksum and additional Load/Verify parameters to the unit.

20.4.7.2 Data Words.

20.4.7.2.1 Data Word 1. DATA WORD 1 will contain the number of sub-pages and the first sub-page for units utilizing this form of paging or sub-paging. This word may also be used for internal register control. These fields represent the values to be used in the next HEADER, MEMORY DATA, ..., MEMORY DATA, TRAILER transaction. For the first HEADER, MEMORY DATA, ..., MEMORY DATA, TRAILER transaction this information will be transmitted prior to the Memory Data transaction via a HEADER, TRAILER transaction in which the TM (Transfer Mode) field in DATA WORD 1 of the Header is 00 (no transfer).

a. Sub-Page/Register Count (bits 8-15). This field may be used in lieu of or in conjunction with the Page Number field in DATA WORD 4 of the Header Message and is individual user definable. Unused bits shall equal 0. An example of the use of this field is as follows.

   In order to load 256K of memory into a unit with bank switching and 64K of address capability and a page size definition of 2048 words, the following approach might be used.

   To load 256K with sub-pages 2048 words long requires 128 HEADER, MEMORY DATA, ..., MEMORY DATA, TRAILER transactions. (256K/2048 = 128). The 128 transactions would consist of 32 transactions for each of the four banks. Thus for each 32 transactions the Header Data 4 Page Number = Bank Number would be incremented (0-3). Within each group of 32 transactions the Sub-page count would increment every transaction (0-31). For each transaction (assuming HT = 01 for Buffer Transfer Count = number of messages) the Header Data 1 Buffer Transfer Count would be 64 (2048 words/32 words per message).

b. First Sub-Page/Register (bits 0-7). This field may be used in lieu of or in conjunction with the Page Number field in DATA WORD 4 of the Header Message and is individual user definable. Unused bits shall equal 0. Examples of use would be: specifying the processor register into which Page Number field in DATA WORD 4 of the Header Message is to be loaded; or specifying the initial sub-page count in the example above to 1 so as to not reprogram the first 2048 memory locations (the first group of transactions would only be 31 transactions long (1 to 31) and the Sub-page count for the first transaction would be set to 1 to indicate a starting address of 2048).

20.4.7.2.2 Data Word 2.

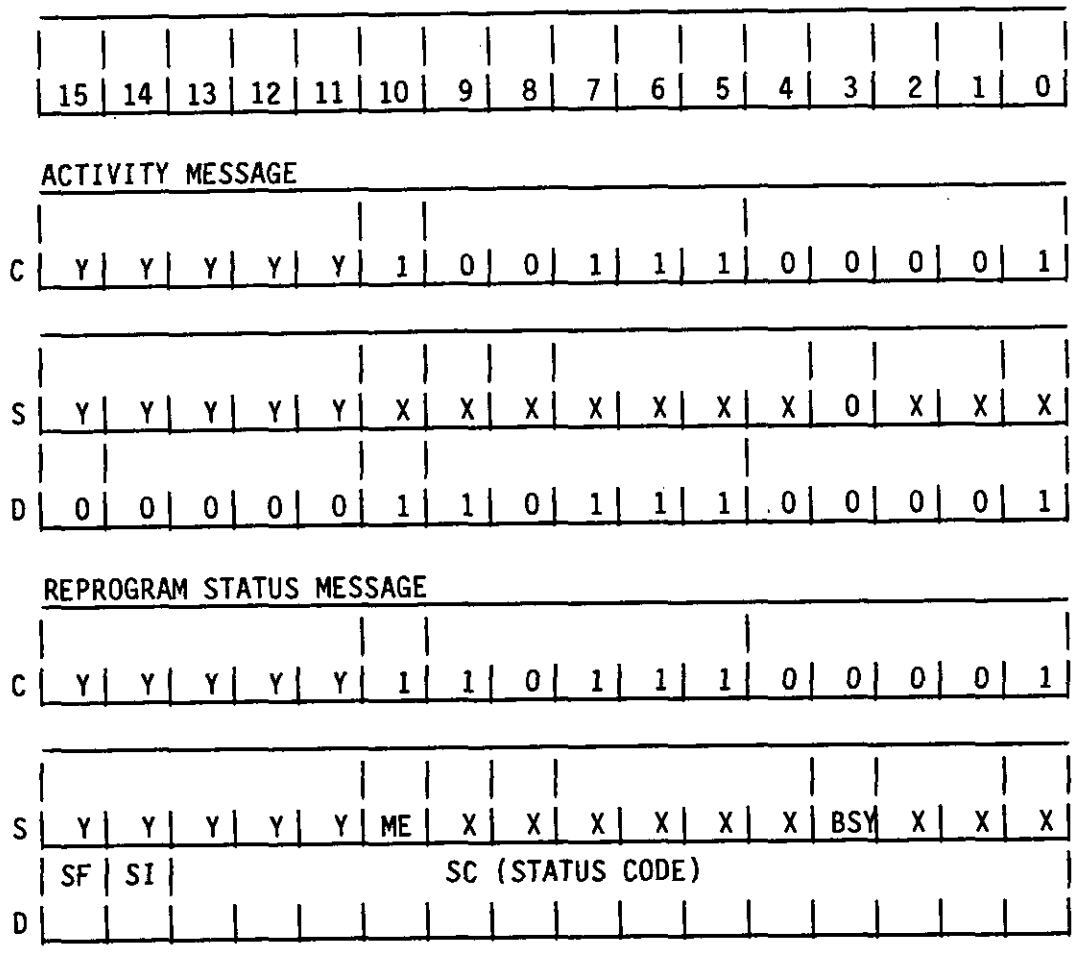
a. Checksum (bits 0-15). The checksum will be the checksum of an entire transaction, i.e., HEADER, MEMORY DATA, ..., MEMORY DATA, TRAILER (when TM in Header Data 1 is not equal to 0) or HEADER, TRAILER (when TM in Header Data 1 is equal to 0). The checksum will be derived by a 2's complement 16 bit addition of every DATA WORD in

the transaction (i.e., Header, Memory Data, and Trailer DATA WORDS) with the exception of the Checksum DATA WORD (Trailer Data 2). The 2's complement 16-bit addition is binary addition with the carry discarded (i.e., no end around carry) (e.g., FFFF (hex) + 1 = 0).

The unit being reprogrammed shall be responsible for comparing the checksum received from the MLV with the data words for both load and verify functions. The Checksum value in DATA WORD 2 of the Trailer is the checksum that should be computed by the unit. If the value computed does not match the value received for either a load or verify operation, an error shall be declared and a Reprogram Status Message shall be requested.

20.4.8 Reprogram Status: MLV = BC: TR = 1: SUBADDRESS = 17H.

20.4.8.1 Reprogram Status Bus Data.



The Activity Message shown prior to the Reprogram Status Message requests that the MLV command the Reprogram Status Message.

20.4.8.1.1 Reprogram Status Message Utilization. During reprogramming operations the unit being reprogrammed may halt the operation and notify the MLV of an error by setting the BUSY bit in the STATUS RESPONSE WORD or in the Activity Message DATA WORD. When the MLV receives the BUSY bit, it will then transmit Activity Messages until the BUSY bit is cleared. The service request to transmit the Reprogram Status Message will be honored after the first Activity Message response with the BUSY bit cleared. By this means the unit can notify the MLV of the error.

20.4.8.2 Data Words.

20.4.8.2.1 Data Word 1.

a. SF (Status Flag) bit (bit 15). This bit shall be set to 1 to indicate that the remainder of the Data Word should be processed by the MLV. (i.e., Reprogram Status Message contains valid data.) If this bit is set to 0, the Reprogram Status Message will be ignored by the MLV.

b. SI (Status Indicator) bit (bit 14). The SI bit defines the meaning of the remainder of the Data Word namely an error code or a status code to be displayed by the MLV.

   1. SI = 0 indicates that an error has occurred and the error code defined below shall be processed by the MLV.

   2. SI = 1 indicates that no error has occurred and the Status Code in bits 13-0 are to be displayed on the MLV display as 4 hexidecimal characters (bits 15 and 14 of the display value are 0). With SI = 1 the values of bits 13-0 will be used to indicate status or progress through the Load/Verify (ex., increment the value of Status Code after each 1K of data is transferred). The use of SI=1 to display status is optional.

c. SC (Status Code) (bits 0-13). When SF = 1 and SI = 1, these bits are display characters as described in b above. When SF = 1 and SI = 0, these bits represent error codes and the desired MLV action. The error codes are:

   SC = 0001(H) = Abort. This will indicate to the MLV that the Load/Verify has been aborted and should not be retried. The MLV shall display the error code and wait for operator response. On receiving the correct response, the MLV shall abort the load of that unit and continue with the load of the next unit (if it exists).

   SC = 0002(H) = Restart. This will indicate that an unrecoverable error has occurred in the unit being loaded and a reload of the unit is desired. The MLV shall display

the error code and wait for operator response. On receiving the correct response, the MLV shall start the load of that unit over again.

SC = 0003(H) = Retry. This will indicate that an error has occurred in the last message sequence transaction and a repeat of the sequence is desired. The MLV shall display the error code and wait for operator response. On receiving the correct response, the MLV shall repeat the last transaction over again.

SC = 0004(H) = Automatic Retry. This will indicate that an error has occurred in the last message sequence transaction. After three consecutive retries, the MLV shall display the error code and wait for operator response. (If the retry is successful before reception of the third consecutive error, operation will continue as normal.) On receiving the correct operator response, the MLV shall abort the load of that unit and continue with the load of the next unit (if it exists).

SC = 0005 - 3FFF(H) = Spare. Not to be utilized without a revision to this standard.

20.4.9 MLV Error: MLV = BC: TR = 0: SUBADDRESS = 17H.

20.4.9.1 MLV Error Bus Data.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ACTIVITY MESSAGE																
C	Y	Y	Y	Y	Y	1	0	0	1	1	1	0	0	0	0	1
S	Y	Y	Y	Y	Y	X	X	X	X	X	X	X	0	X	X	X
D	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
MLV ERROR MESSAGE																
C	Y	Y	Y	Y	Y	0	1	0	1	1	1	0	0	0	0	1
D	0	0	0	0	0	0	0	0	0	0	0	0	0	A	C	T
S	Y	Y	Y	Y	Y	ME	X	X	X	X	X	X	BSY	X	X	X

The Activity Message shown prior to the MLV Error Message will only be present when the MLV is required to check the BUSY bit status of RTs that do not use the BUSY bit in the STATUS RESPONSE WORD.

20.4.9.1.1 MLV Error Message Utilization. This message will be utilized to inform the unit that the MLV has detected an error in the Load/Verify.

20.4.9.2 Data Words.

20.4.9.2.1 Data Word 1.

a. A (Abort) (bit 2). This bit will be set to 1 by the MLV to notify the RT that the Load or Verify has been aborted and no further retries will be made.

b. C (Complete Restart) (bit 1). This bit will be set to 1 by the MLV to notify the RT that an unrecoverable error has occurred and all Memory Data Load or Memory Data Verify transactions will be restarted.

c. T (Transaction) (bit 0). This bit will be set to 1 by the MLV to notify the RT that there was an error detected in the last HEADER, MEMORY DATA, ..., MEMORY DATA, TRAILER or HEADER, TRAILER transaction and that the transaction will be repeated.

d. Other bits (bits 3-15). Bits 3-15 shall equal 0.

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APPENDIX C

MESSAGE FORMATS MLV = RT

30. STANDARD PROTOCOL FOR BUS CONTROLLERS

30.1 Applicability. The protocol of this Appendix is applicable to all new Bus Controller designs and to previously existing Bus Controller equipment where the existing hardware does not allow the Bus Controller to revert to a Remote Terminal.

30.2 General Operation. The MLV will reprogram each equipment in the following manner (see Figure 11).

a. When indicated as usable in the Lookup Table, the MLV will request a Memory Configuration Message from the unit being processed. The Memory Configuration will describe the current memory contents for one or two memory areas as applicable. The MLV will compare the received Memory Configuration to the current Memory Configuration stored on the MLV Memory Storage Device (MSD). In automatic mode, if the unit already contains the current Memory Configuration, the MLV will then continue on to the next unit to be processed. If the Memory Configuration Message was not usable, the MLV will assume that the unit requires reprogramming. In Manual Mode, the MLV will display the Memory Configuration data and continue reprogramming for the selected unit.

b. If the unit in process requires reprogramming of either or both memory areas, the MLV will check the old and new memory configurations to determine if the information in the MLV MSD is compatible with updating the old memory (will use the patch file if it exists). If a patch file does not exist or is not usable, the MLV will check to see if a complete file exists and check if it will result in a newer revision level. If the Configuration Message was not usable, no patch file should exist (see 5.2.2.1.2) and the MLV will use the complete file for reprogramming. The MLV will declare an error if the MSD information is insufficient. If the MSD information is correct for reprogramming, the MLV will then send a Reprogram Control Message to enable the reprogramming function for the appropriate Memory Area(s) (depending on unit requirements memory areas will be enabled simultaneously or sequentially). The unit will then check the validity of the Reprogram Control Message utilizing internally stored information and the Reprogram Enable discrete(s) if applicable.

c. Once the reprogramming mode is entered, the MLV will then proceed to load the new memory contents in blocks of varying size depending on the unit and update requirements. There will be no specific erasure commands from the MLV. The unit being reprogrammed will be responsible for erasure based on the directed write information. The reprogramming will be conducted by a series of one or more HEADER

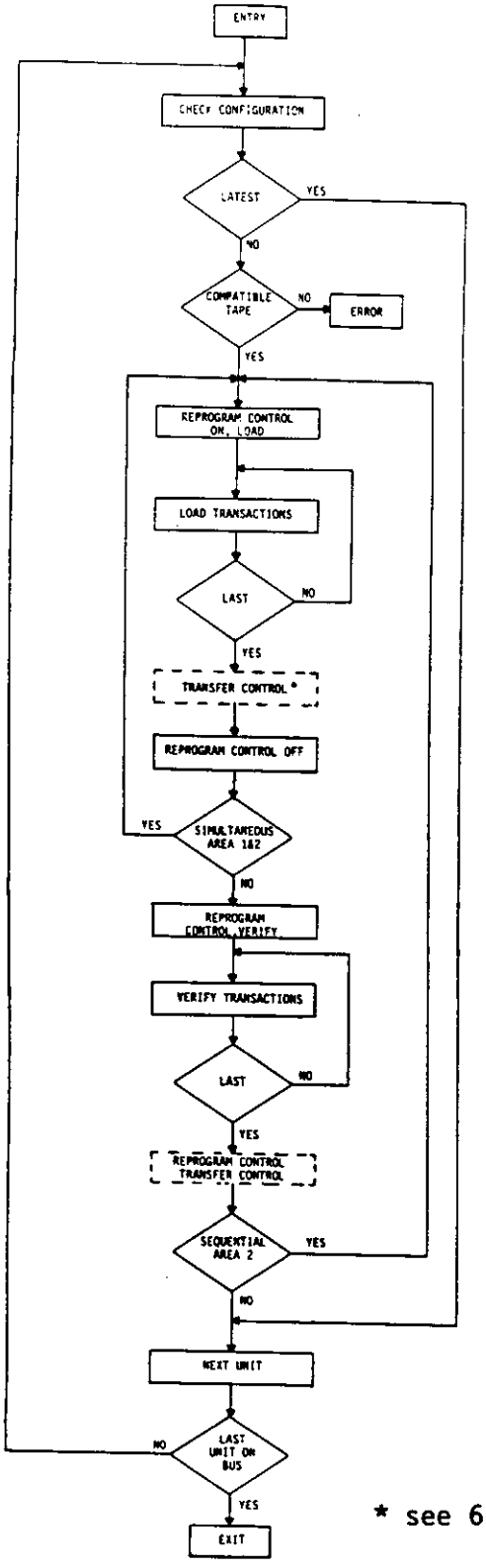


FIGURE 11. Avionics Subsystem = BC Load/Verify Procedure.

MESSAGE, MEMORY DATA LOAD MESSAGE, ..., MEMORY DATA LOAD MESSAGE, TRAILER MESSAGE transactions. If required, a HEADER MESSAGE, TRAILER MESSAGE transaction will also be present for paging or transfer of control functions. If the unit being reprogrammed is required to keep track of how many times a particular memory device has been reprogrammed, the device being reprogrammed shall declare an Abort error (Reprogram Status Message) if the predetermined memory write capability has been exceeded. The storage of this information within the unit memory shall not affect the validity of the memory verify function. (i.e., the unit being reprogrammed shall mask out this information during the Verify operation.)

d. After completion of the load the MLV will, if required, then provide transfer of control information to the unit using a HEADER MESSAGE, TRAILER MESSAGE transaction. Transfer control prior to a Verify via the Reprogram Control Message is not permitted as discussed in 6.1.j. The transfer of control prior to a verify shall not be used to transfer control to a memory area that has been loaded but not verified. If it is necessary to transfer control prior to the completion of a memory area Load/Verify, the two parts of the memory area will be loaded/verified separately using the same technique as for sequentially loading Memory Areas 1 and 2. The transfer of control via the Header Message may be inhibited during a load as discussed in 6.1.m.

e. After all required data for a particular memory area have been transferred the MLV will, via the Reprogram Control Message, disable the reprogramming function for that memory area.

f. When simultaneous reprogramming of Memory Areas 1 and 2 is utilized, the MLV will load the second memory area prior to the verify operation. When sequential (or single Memory Area) reprogramming is utilized, the MLV will at this time verify the previously loaded memory area prior to the Memory Area 2 load operation. The MLV will perform the memory verify utilizing the same transactions that were used for the memory load except that the MLV will receive the data from the unit being reprogrammed and compare the received data with the stored MSD data. The automatic verify after a load may be inhibited as discussed in 6.1.g.

g. After completion of the verify the MLV will, if required, then provide transfer of control information to the unit using either a HEADER MESSAGE, TRAILER MESSAGE transaction or via the Reprogram Control Message. When sequential reprogramming of Memory Areas 1 and 2 is utilized, the MLV will at this time repeat the Load/Verify operations for the second memory area.

h. Assuming there were no errors, the MLV will continue on to process the next unit on the bus or the next bus as appropriate. If an error did occur, operator intervention would be requested by the MLV fault display.

30.3 Status Response Word: MLV = RT.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
S	TERMINAL ADDRESS					ME		SR				BSY			TF
Z	Z	Z	Z	Z		0		0	0	0	0		0	0	

A STATUS RESPONSE WORD will be provided by the MLV for each message transaction. The STATUS RESPONSE WORD will follow the data on a MLV receive type transaction and will proceed the data on an MLV transmit type transaction. The BC will allow a response time gap of at least 6.5 usec from the end of the last transmitted COMMAND WORD (transmit type message) or the end of the last transmitted DATA WORD (receive type message), to the start of the MLV STATUS RESPONSE WORD before declaring a no response error (Equivalent of 8.5 usec when measured in accordance with MIL-STD-1553B). Under normal conditions the MLV shall begin the STATUS RESPONSE WORD within the period of 2-5 usec from the receipt of the end of the last COMMAND WORD (transmit type message) or the receipt of the end of the last DATA WORD (receive type message) (Equivalent of 4-7 usec when measured in accordance with MIL-STD-1553B). The BC will ensure that the time from the end of the MLV transmission of the last DATA WORD (transmit type message) or the end of the last STATUS RESPONSE WORD (receive type message) to the beginning of the next COMMAND WORD is at least 2 usec (Equivalent of 4 usec when measured in accordance with MIL-STD-1553B). The STATUS RESPONSE WORD bits are as follows:

a. TERMINAL ADDRESS (bits 11-15). The MLV RT address will be that which has been assigned to each individual aircraft and each individual bus on that aircraft. The MLV will assume the proper RT address based on the Aircraft Type and Aircraft Configuration Modification information provided to the MLV and based on the particular bus selected by the MLV switching network. Throughout the remainder of this appendix the MLV RT address will be referred to as ZZZZZ.

b. ME bit (bit 10). The Message Error (ME) bit may be set by the MLV under the following conditions.

   1. The STATUS RESPONSE WORD following a COMMAND WORD requesting an undefined subaddress Transmit/Receive combination may result in bit 10 = 1 for that STATUS RESPONSE WORD. If an MLV transmission was requested, the data words requested may or may not be present.

   2. The STATUS RESPONSE WORD for the next COMMAND WORD after a receive type message may result in bit 10 = 1 if the data received in the previous message was: short in data word count; failed to pass word validation; had an improperly timed data sync; or had non-contiguous data.

The ME bit, if set, will be set once for a message error and then cleared for the next message if there was no subsequent error.

c. SR bit (bit 8). The Service Request (SR) bit will only be set to 1 by the MLV in response to an Activity Message. (See Activity Message in 30.4.1.) In all other cases the SR bit shall equal 0.

d. BSY (BUSY) bit (bit 3). The BUSY bit may be set by the MLV for the STATUS RESPONSE WORD for any COMMAND WORD from the BC. The setting of the BUSY bit means that a message previously received (or internal MLV requirements) necessitate a suspension or slowdown of communications. If the MLV sets the BUSY bit in the STATUS RESPONSE WORD, it will suppress transmission of the DATA WORDS associated with a message. All additional message traffic other than the Activity Message shall be suspended until the BUSY bit is cleared. While the BC is waiting for the BUSY bit to clear, the Activity Message shall be sent every 10 to 100 msec. As long as the BUSY bit is clear the BC may assume that the MLV can support a continuous stream of identical messages with 2 msec from the end of one message to the start of the next COMMAND WORD. The continuous stream of identical messages is assumed to be either Memory Data Load or Memory Data Verify messages. The continuous stream can only be sustained by the MLV for a period of time compatible with the Memory Storage Device and internal memory capabilities. The MLV will utilize the BUSY bit to suspend the continuous stream when required. As a minimum the MLV shall be capable of providing 2K data words (in Memory Data Load or Memory Data Verify messages) per second. The BC shall ensure that the message for which the MLV initially replied with the BUSY bit set in the STATUS RESPONSE WORD will be retransmitted once the BUSY bit is cleared.

e. TF bit (bit 0). The Terminal Flag (TF) bit will be set to 1 by the MLV if bit 10, 8, or 3 is set to 1.

f. Other bits. Bits 9, 7, 6, 5, 4, 2 and 1 will always be 0 in the MLV STATUS RESPONSE WORD.

30.4 Messages.

30.4.1 Activity Message: MLV = RT: TR = 1: SUBADDRESS = 07H.

30.4.1.1 Activity Message Bus Data.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C	Z	Z	Z	Z	Z	1	0	0	1	1	1	0	0	0	0	1
S	Z	Z	Z	Z	Z	ME	0	SR	0	0	0	0	0	0	0	TF
D	BSY	0	0	0	0	TR	SUBADDRESS					WORD COUNT				

30.4.1.1.1 Activity Message Utilization. This message will be utilized by the BC to determine whether the MLV remote terminal is ready to receive data and will allow the MLV to request to send information to the BC or receive information from the BC. This message will allow the MLV to control the loading sequence when operating as an RT. The BC shall command this message at a periodic rate until a HEADER MESSAGE, MEMORY DATA MESSAGE, ..., MEMORY DATA MESSAGE, TRAILER MESSAGE transaction is begun. After receipt of a Header Message requiring data transfer (TM not = 00), the BC may utilize the Activity Message to control the transfer of Memory Data messages or may use the Header Message information to internally control the number of Memory Data messages so long as the BUSY bit in the MLV STATUS RESPONSE WORD is checked by the BC. The BC may control the entire load or the entire verify (i.e., all the HEADER MESSAGE, MEMORY DATA MESSAGE, ..., MEMORY DATA MESSAGE, TRAILER MESSAGE transactions) without the use of the Activity Message by monitoring the TC bits in the Header Message.

30.4.1.1.2 Status Word. The status word response to the Activity Message shall be as defined for STATUS RESPONSE WORD in 30.3 and shall utilize bits 3 and 8 as follows:

a. SR bit (bit 8). The MLV will set the Service Request (SR) bit to 1 whenever the contents of bits 0 through 10 of the DATA WORD are other than 0. The BC may utilize the SR bit to determine if it is necessary to examine bits 0 through 10 of the data word that follows. Since the contents of bits 0 through 10 of the data word will control the state of the SR bit, it is not necessary for the BC to process the SR bit.

b. BSY (BUSY) bit (bit 3). The BUSY bit will indicate that the MLV is not ready to process any message from the BC other than the Activity Message. Prior to the transmission of any other type messages to the MLV, the BC will continue to send activity messages to the MLV every 10 to 100 msec until the BUSY bit is cleared. The BUSY bit and the SR bit will not be set simultaneously by the MLV.

30.4.1.2 Data Words.

30.4.1.2.1 Data Word 1. The DATA WORD will only be transmitted by the MLV acting as RT when the BUSY bit is not set in the STATUS RESPONSE WORD. The MLV will suppress transmission of the DATA WORD if the BUSY bit is set in the STATUS RESPONSE WORD.

a. BSY (BUSY) bit (bit 15). The BUSY bit in the data word for the Activity Message shall not be used when the MLV is acting as an RT since, when the MLV is busy, no data word will be transmitted.

b. MLV Request Bits (bits 0-10). Bits zero through 10 shall be utilized to allow the MLV to request that the BC send a specific command to the MLV. As a result of the MLV request, the BC will transmit a COMMAND WORD with the MLV terminal address in bits 11 through 15 and the contents of the Activity Message MLV Request Bits in bits 0-10.

1. TR bit (bit 10). The TR bit will be set to 1 if the MLV wishes to transmit a message and will be set to 0 if the MLV wishes to receive a message.

2. SUBADDRESS bits (bits 5-9). The subaddress bits will indicate the subaddress of the desired message.

3. WORD COUNT bits (bits 0-4). The word count bits will indicate the data word count for the desired message.

c. Other Bits (bits 11-14). Bits 11-14 shall equal 0.

30.4.2 Memory Configuration: MLV = RT: TR = 0: SUBADDRESS = 13H.

30.4.2.1 Memory Configuration Bus Data.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ACTIVITY MESSAGE																
C	Z	Z	Z	Z	Z	1	0	0	1	1	1	0	0	0	0	1
S	Z	Z	Z	Z	Z	ME	0	1	0	0	0	0	0	0	0	TF
D	0	0	0	0	0	0	1	0	0	1	1	0	0	0	1	0
MEMORY CONFIGURATION MESSAGE																
C	Z	Z	Z	Z	Z	0	1	0	0	1	1	0	0	0	1	0
D1	MEMORY AREA 1 CONFIGURATION															
D2	MEMORY AREA 2 CONFIGURATION															
S	Z	Z	Z	Z	Z	ME	0	0	0	0	0	0	BSY	0	0	TF

The Activity Message shown prior to the Memory Configuration Message requests that the BC command the Memory Configuration Message.

30.4.2.1.1 Memory Configuration Message Utilization. This message is utilized to read the current memory configuration of the unit. This message is only used when its use is indicated in the Lookup Table.

30.4.2.2 Data Words.

30.4.2.2.1 Data Word 1. Memory Area 1 Configuration (bits 0-15). The data shall be in individual unit format and shall represent the configuration of the data stored in Memory Area 1. Unused bits shall equal zero. In automatic mode this message is used for the purpose of comparing the unit configuration stored on the MSD with the reported unit configuration. The MLV will assume that the largest numerical value (MSD vs. reported) indicated by bits 0-15 is the latest configuration.

30.4.2.2.2 Data Word 2. Memory Area 2 Configuration (bits 0-15). The data shall be in individual unit format and shall represent the configuration of the data stored in Memory Area 2. Unused bits (including equipments that do not utilize Memory Area 2) shall equal 0. In automatic mode this message is used for the purpose of comparing the unit configuration stored on the MSD with the reported unit configuration. The MLV will assume that the largest numerical value (MSD vs. reported) indicated by bits 0-15 is the latest configuration.

30.4.3 Reprogram Control: MLV = RT: TR = 1: SUBADDRESS = 1DH.

30.4.3.1 Reprogram Control Bus Data.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ACTIVITY MESSAGE																
C	Z	Z	Z	Z	Z	1	0	0	1	1	1	0	0	0	0	1
S	Z	Z	Z	Z	Z	ME	0	1	0	0	0	0	0	0	0	TF
D	0	0	0	0	0	1	1	1	1	0	1	0	0	1	0	0
REPROGRAM CONTROL MESSAGE																
C	Z	Z	Z	Z	Z	1	1	1	1	0	1	WORD COUNT				
S	Z	Z	Z	Z	Z	ME	0	0	0	0	0	0	0	0	0	TF
D1	TYPE								TYPE							
D2	NUMBER								NUMBER							
D3	NUMBER								NUMBER							
D4	FILL						L/V		CONTROL CODE							

The Activity Message shown prior to the Reprogram Control Message requests that the BC command the Reprogram Control Message.

30.4.3.1.1 Reprogram Control Message Utilization. The Reprogram Control message shall provide a key for entering/leaving the reprogramming mode. For units utilizing Reprogram Enable discretes, the Reprogram Control Message shall have no effect on the BC if the appropriate Reprogram Enable discrete is not present. Each field in the data shall be checked by the BC for compliance with the following prior to execution of the Reprogram Control Code. The Type and Number fields shall be based on WRA nomenclature (e.g., CP-1293); however, if this creates a conflict, the system nomenclature (e.g., ALR-67) shall be utilized instead.

30.4.3.2 Data Words.

30.4.3.2.1 Data Word 1. Type (bits 0-15). The type field shall be made up of the first two 8 bit ASCII characters that represent the nomenclature of the unit being controlled. For example, for CP-1293 the two characters would be "C," "P."

30.4.3.2.2 Data Word 2. Number (bits 0-15). The number field shall be made up of the third and fourth 8 bit ASCII characters that represent the nomenclature of the unit being controlled. For example, for CP-1293 the two characters would be "1," "2."

30.4.3.2.3. Data Word 3. Number (bits 0-15). The number field shall be made up of the last two 8 bit ASCII characters that represent the nomenclature of the unit being controlled. For example, for CP-1293 the two characters would be "9," "3."

30.4.3.2.4 Data Word 4.

a. Fill (bits 10-15). The fill field may be any bit pattern including 0 and is to be defined by the individual equipment being controlled. The fill field shall be checked even if the field is defined as 0.

b. L/V (bits 8-9). The Load/Verify (L/V) bits are used to describe whether a Load, Verify, or other type transaction will follow. These bits are coded as follows:

    L/V = 01 A Memory Load follows
    L/V = 10 A Memory Verify follows
    L/V = 11 Not used
    L/V = 00 Reprogram Control Message is being sent for some reason other than loading/verifying (e.g., to quiet the BC, etc.)

c. Control Code (bits 0-7)

    BIT 7 Reprogram Enable 1 = 80H
    BIT 6 Reprogram Enable 2 = 40H
    BIT 5 Reprogram Disable 1 = 20H

BIT 4 Reprogram Disable 2 = 10H
BIT 3 BC convert to RT = 08H
BIT 2 BC stop transmitting/receiving on bus = 04H
BIT 1 RT revert to BC = 02H
BIT 0 Execute from Program Entry Address supplied previously in Header Message Data Word 3/Data Word 4 = 01H

30.4.3.2.4.1 Control Code Processing.

30.4.3.2.4.1.1 Field Validity. The Control Code field shall be valid only if all other fields are correct and only if either the Avionics Reprogram Enable 1/EW UDM Reprogram Enable discrete or the Avionics Reprogram Enable 2/EW OSM Reprogram Enable discrete is present. At the end of reprogramming, the MLV will maintain the active discrete for at least 100 msec after the transmission of the Reprogram Control Message that ends the reprogramming mode.

30.4.3.2.4.1.2 Valid Control Codes. The following are the only valid Control Codes that can occur when the MLV is the RT. Any other code shall cause the BC to not execute the Reprogram Control Code.

a. Code 00000000 = 00H - this code shall indicate no reprogram control action is to be taken (Code 00H used when Verify operation is indicated).

b. Code 00000001 = 01H - this code shall cause the BC to begin execution starting at the address previously supplied via Data Word 3/ Data Word 4 of the Header Message.

c. Code 00000100 = 04H - this code shall cause the BC to stop communications on the bus. Once the BC has stopped communications on the bus, activity shall remain stopped until both the Avionics Reprogram Enable 1/EW UDM Reprogram Enable discrete and the Avionics 2/EW OSM Reprogram Enable discretes are inactive.

d. Code 00001000 = 08H - this code shall cause the BC to revert to an RT. Upon execution of this Reprogram Control Code the message traffic shall be as defined in Appendix B.

e. Code 00010000 = 10H - this code shall cause the BC to exit the reprogramming mode for Memory Area 2. This code shall only be valid if the Avionics Reprogram Enable 2/EW OSM Reprogram Enable discrete is active, or when only one enable is utilized, this code shall apply only if the enable is present. The presence or absence of the Avionics Reprogram Enable 1/EW UDM Reprogram Enable discrete shall not affect the validity of this code when both enables are used.

f. Code 00100000 = 20H - this code shall cause the BC to exit the reprogramming mode for Memory Area 1. This code shall only be valid if the Avionics Reprogram Enable 1/EW UDM Reprogram Enable discrete is active, or when only one enable is utilized, this code shall

apply only if the enable is present. The presence or absence of the Avionics Reprogram Enable 2/EW OSM Reprogram Enable discrete shall have no affect on the validity of this code when both enables are used.

g. Code 0011000 = 30H - combination of 10H and 20H for simultaneous Memory Areas 1 and 2 exit reprogramming mode. (Both Reprogram Enables must be present if both Reprogram Enables are incorporated.)

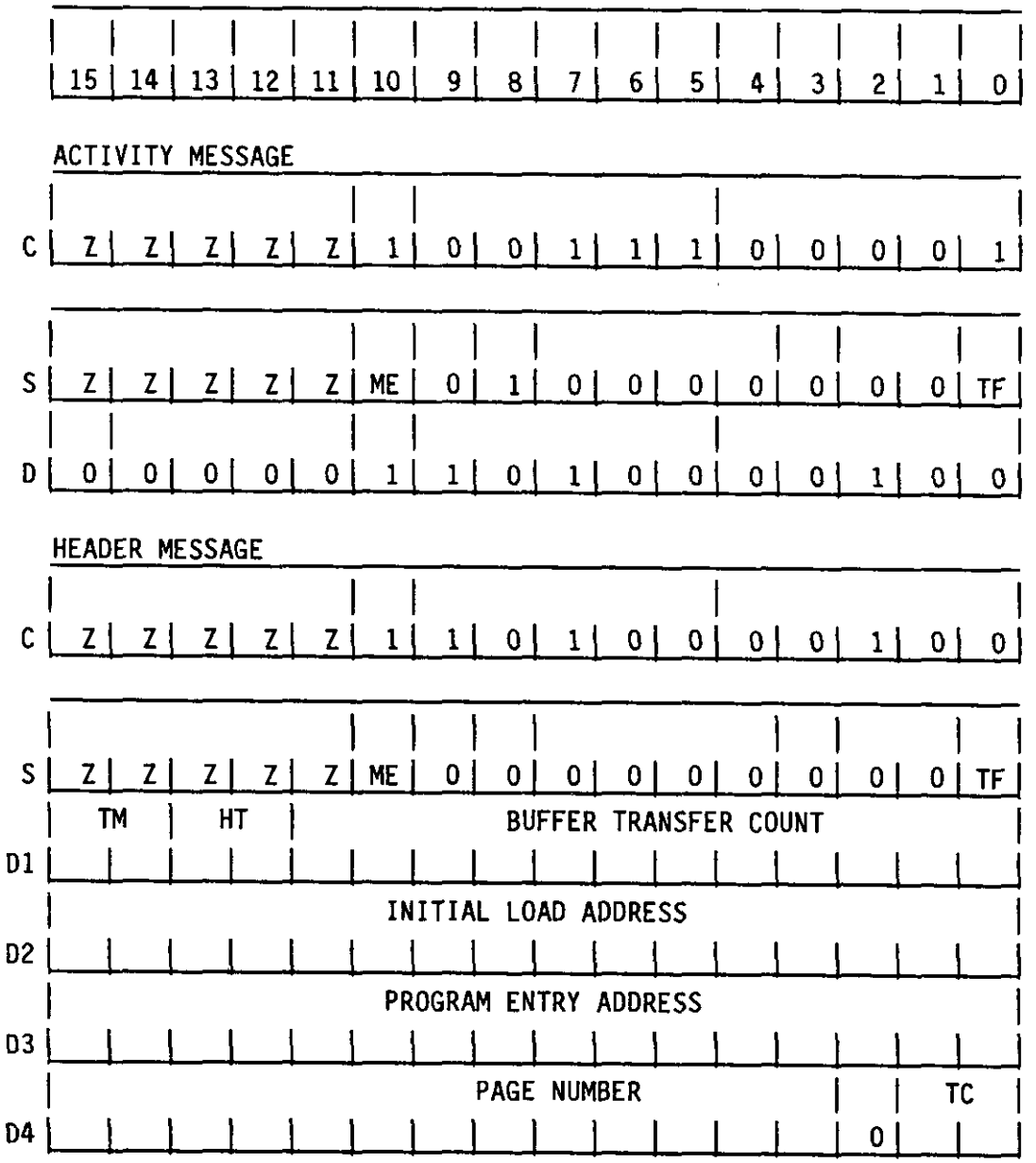
h. Code 01000000 = 40H - this code shall cause the BC to enter the reprogramming mode for Memory Area 2. This code shall only be valid if the Avionics Reprogram Enable 2/EW OSM Reprogram Enable discrete is active, or when only one enable is utilized, this code shall apply only if the enable is present. The presence or absence of the Avionics Reprogram Enable 1/EW UDM Reprogram Enable discrete shall not affect the validity of this code when both enables are used.

i. Code 10000000 = 80H - this code shall cause the BC to enter the reprogramming mode for Memory Area 1. This code shall only be valid if the Avionics Reprogram Enable 1/EW UDM Reprogram Enable discrete is active, or when only one enable is utilized, this code shall apply only if the enable is present. The presence or absence of the Avionics Reprogram Enable 2/EW OSM Reprogram Enable discrete shall not affect the validity of this code when both enables are used.

j. Code 11000000 = C0H - combination of 40H and 80H for simultaneous Memory Areas 1 and 2 enter reprogramming mode. (Both Reprogram Enables must be present if both Reprogram Enables are incorporated.)

30.4.4 Header: MLV = RT: TR = 1: SUBADDRESS = 14H.

30.4.4.1 Header Bus Data.



The Activity Message shown prior to the HEADER Message requests that the BC command the Header Message. The Activity Message will not be used by BCs that keep track of the HEADER, MEMORY DATA, ..., MEMORY DATA TRAILER Message Sequence (i.e., the BC automatically commands this message sequence without the MLV requesting each message in turn).

30.4.4.1.1 Header Message Utilization. This message is used to pass Load/Verify parameters to the unit.

30.4.4.2 Data Words.

30.4.4.2.1 Data Word 1.

a. TM (bits 14-15). The Transfer Mode (TM) bits are used to describe the Memory Data Load or Memory Data Verify DATA WORD content. The TM bits are binary coded as follows:

   1. TM = 00 No transfer. In the No Transfer Mode the Buffer Transfer Count and Initial Load Address have no meaning. This mode is used to transfer the Program Entry Address and Page Number or is used as a preamble to the Trailer Message.

   2. TM = 01 8 bit transfer. Each 16 bits of data transmitted in a DATA WORD will contain only 8 bits of information in bits 0-7.

   3. TM = 10 16 bit transfer. Each 16 bits of data transmitted in a DATA WORD will contain 16 bits of information in bits 0-15.

   4. TM = 11 32 bit transfer. The 16 bits of data transmitted in each odd word (first is odd) contains the 16 LSB of data in bits 0-15 and each even word (second is even) contains the 16 MSB of data in bits 0-15.

b. HT (bits 12-13). The Header Type (HT) bits are used to describe the Header. The Header Type has no meaning when the Transfer Mode is 00. The HT bits are binary coded as follows:

   1. HT = 00 Normal Header. (Buffer Transfer Count equals number of words.)

   2. HT = 01 Normal Header. (Buffer Transfer Count equals number of messages.)

   3. HT = 10 Undefined.

   4. HT = 11 Reserved for internal MLV use. This type of Header will not be transmitted on the bus.

c. Buffer Transfer Count (bits 0-11). The Buffer Transfer Count is used to indicate the amount of data that will follow the Header Message. The Buffer Transfer Count has no meaning when the Transfer Mode is 00. The range of the Buffer Transfer Count is 1 to 4096 (value of 0 = 4096).

1. For HT = 00, the Buffer Transfer Count is the total number of DATA WORDS that will be transmitted after the Header. The DATA WORDS will be transmitted in 32-word messages with the last message containing 1 to 32 DATA WORDS. The maximum transfer for HT = 00 is 4096 words using 128 Memory Data Load or Memory Data Verify Messages.

2. For HT = 01, the Buffer Transfer Count is the number of Memory Data Load or Memory Data Verify messages that will follow the HEADER. Thus, the maximum data transfer per Header Message is 4096 x 32 DATA WORDS (per Memory Data Load or Memory Data Verify message) which equals 131,072 16 bit words (128K). If paging is utilized for transfer modes 01 or 10 (see 30.4.4.2.4), the maximum value of the Transfer Buffer Count will be 2048. (Yields 65,536 16 bit data words (64K) for transfer modes 01 and 10 using paging.)

30.4.4.2.2 Data Word 2.

a. Initial Load Address (bits 0-15). The Initial Load Address is the 16 or less LSB of the point in memory into which data is to be loaded or read. The maximum value (number of bits) used in the Initial Load Address will be compatible with the page size of units using paging. Unused bits shall equal 0.

30.4.4.2.3 Data Word 3.

a. Program Entry Address (bits 0-15). The Program Entry Address has meaning only for Transfer Mode = 00. The Program Entry Address is the 16 or less LSB of the point in memory at which the unit being reprogrammed is to begin execution after receipt of the Execute command in the Reprogram Control Message (only used for units requiring this command) or when a Transfer Control is indicated in DATA WORD 4. The maximum value (number of bits) used in the Program Entry Address will be compatible with the page size of units using paging. Unused bits shall equal 0.

30.4.4.2.4 Data Word 4.

a. Page Number (bits 3-15). The Page Number represents up to 13 MSBs for page memory address. The Page Number applies to the Program Entry Address for Transfer Mode = 00. The Page Number applies to the Initial Load Address for Transfer Mode = 01, 10, or 11. Unused bits shall equal 0.

b. TC bits (0-1). The Transfer Control (TC) may be used to transfer control to the loaded program after a verify or to an unaltered memory area after a load.

1. Transfer Control = 00 indicates this is the last HEADER, MEMORY DATA, ..., MEMORY DATA, TRAILER or HEADER, TRAILER transaction.

2. Transfer Control = 01 indicates that more data is to follow the current HEADER, MEMORY DATA, ..., MEMORY DATA, TRAILER or HEADER, TRAILER transaction and control should not be transferred. For units using paging and the Program Entry Address, the TC will remain = 01, even for the last data transaction, until a Transfer Mode = 00 message is used to supply the Program Entry Address and Page Number.

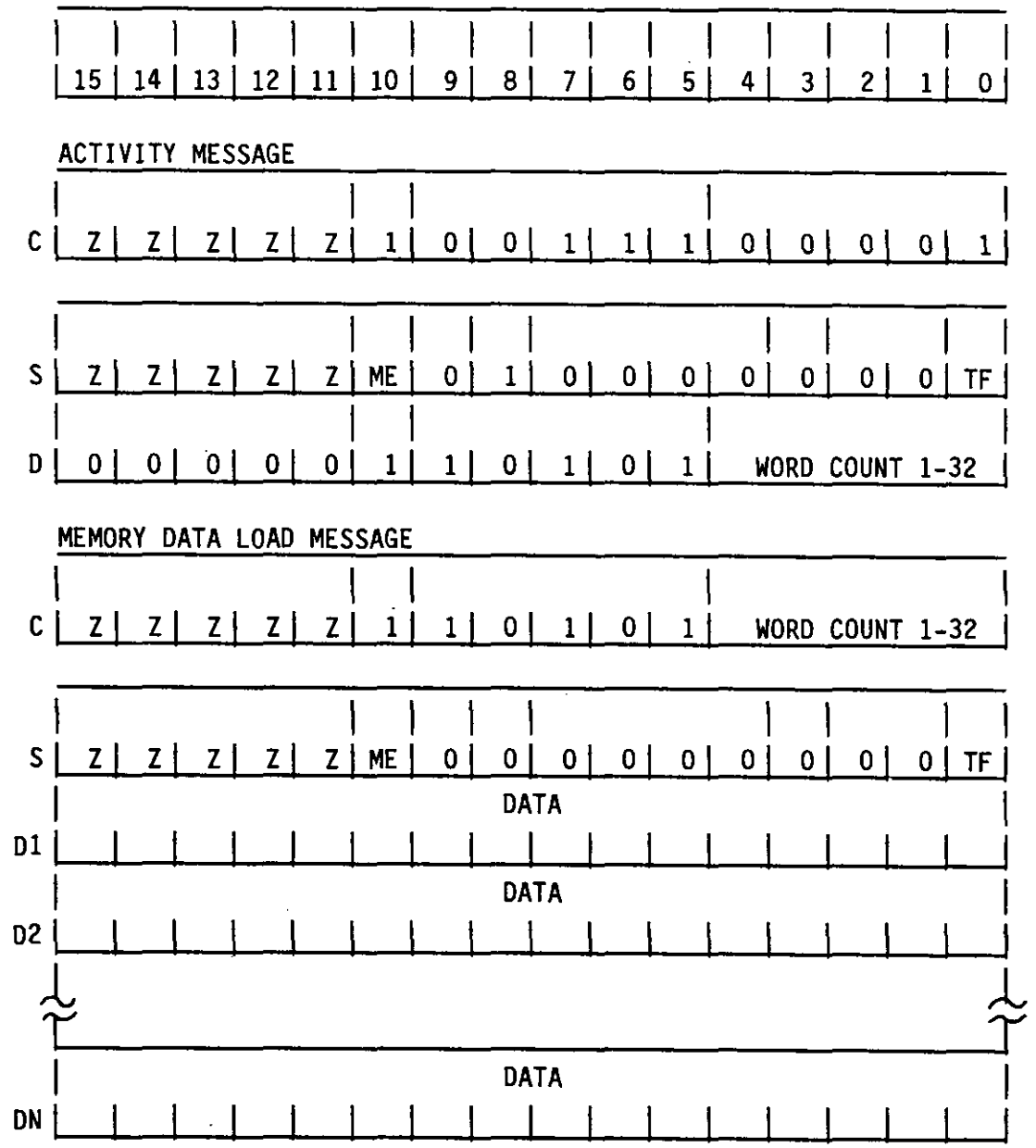
3. Transfer Control = 10 shall indicate that control is to be transferred to the Program Entry Address. When control is transferred, the action shall not take place until after the Trailer Message and shall transfer control only to non-reprogrammed areas or verified areas.

4. Transfer Control = 11 is invalid.

c. Other bits (bit 2). Bit 2 shall equal 0.

30.4.5 Memory Data Load: MLV = RT: TR = 1: SUBADDRESS = 15H.

30.4.5.1 Memory Data Load Bus Data.



The Activity message shown prior to the Memory Data Load will normally only be used for BCs that do not keep track of the number of Memory Data Load messages required for each HEADER, MEMORY DATA, ..., MEMORY DATA, TRAILER transaction or for BCs that do not check the BUSY bit in the MLV status response.

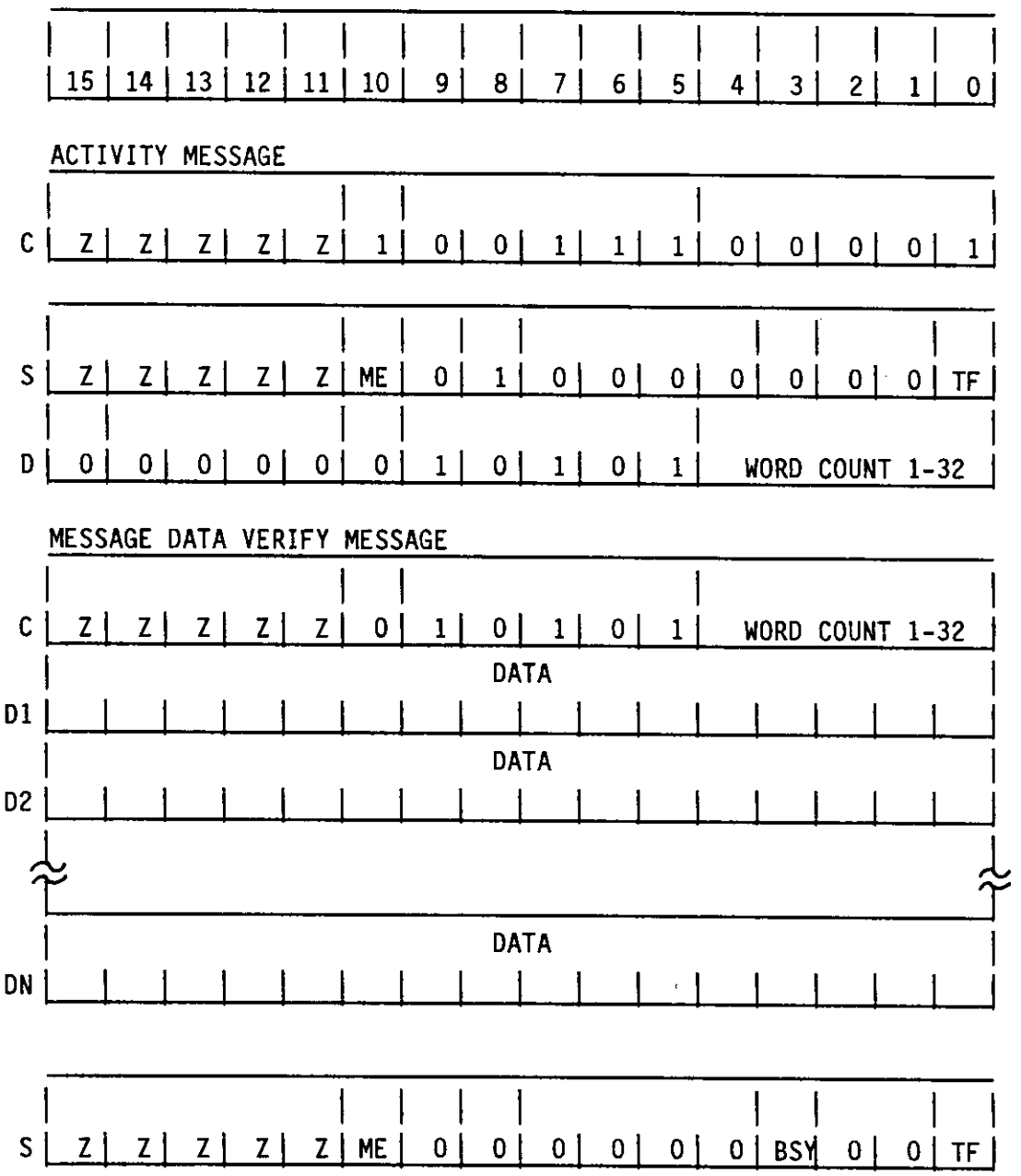
30.4.5.1.1 Memory Data Load Message Utilization. This message is used to pass the data to be loaded into the unit memory.

30.4.5.1.1.1 BUSY Bit. If the BUSY bit had been set in the STATUS RESPONSE WORD for a Memory Data Load Message, no DATA WORDS would have been sent by the MLV. After the BUSY bit is cleared in the STATUS RESPONSE WORD of the Activity Message, the BC shall recommand the Memory Data Load Message for which no data was received.

30.4.5.2 Data Words. The number of Data Words will equal the WORD COUNT in the Memory Data Load Message COMMAND WORD.

30.4.6 Memory Data Verify: MLV = RT: TR = 0: SUBADDRESS = 15H.

30.4.6.1 Memory Data Verify Bus Data.



The Activity Message shown prior to the Memory Data Verify will normally only be used for BCs that do not keep track of the number of Memory Data Verify messages required for each HEADER, MEMORY DATA, ..., MEMORY DATA, TRAILER transaction.

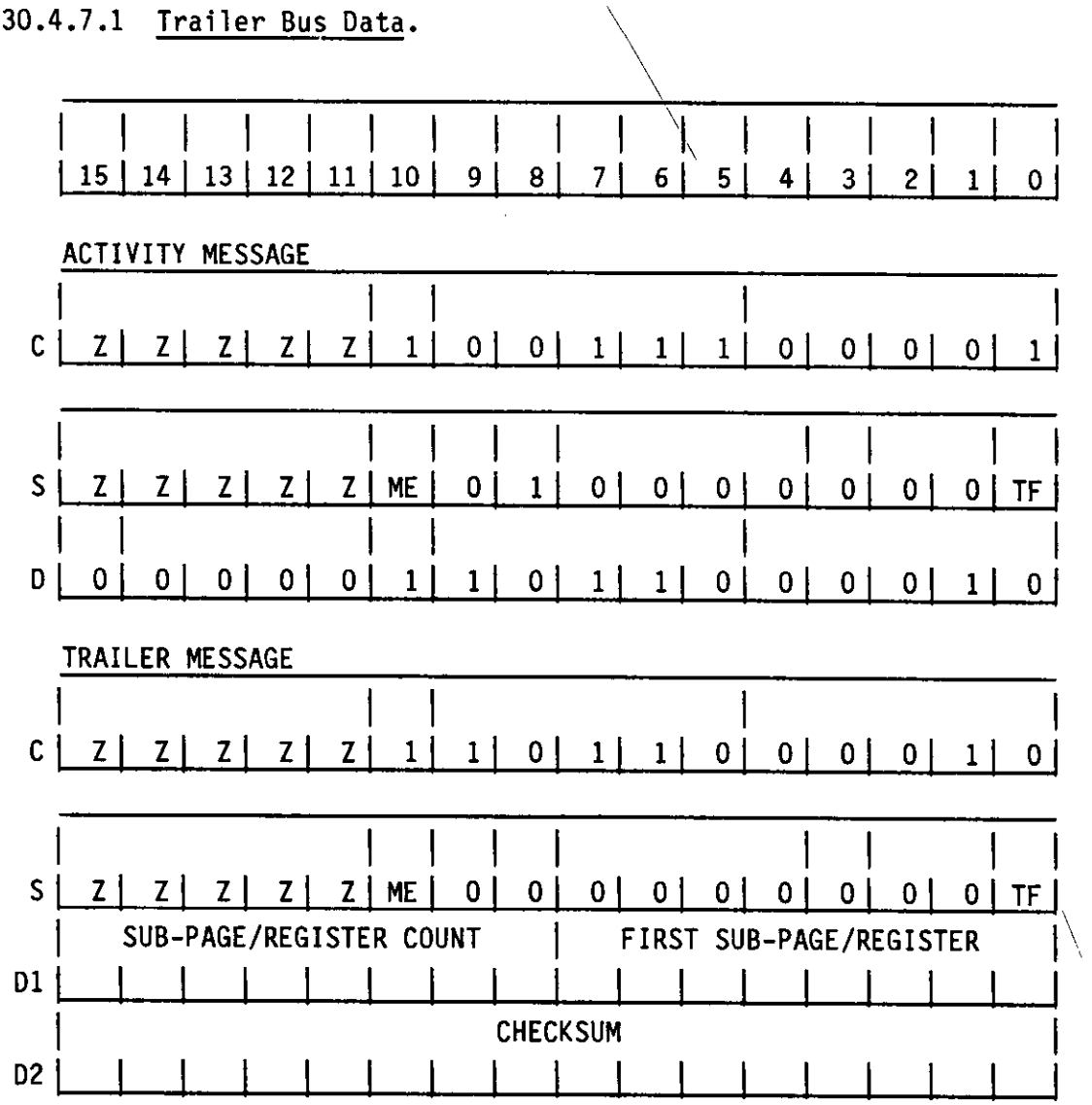
30.4.6.1.1 Memory Data Verify Message Utilization. This message is used to pass the data that the MLV will compare to the data stored on the MSD.

30.4.6.1.1.1 BUSY Bit. If the BUSY bit is set in the MLV STATUS RESPONSE WORD for a Memory Data Verify Message, the BC shall retransmit that Memory Data Verify Message (i.e., same DATA WORD(s)) after the BUSY bit is cleared in the STATUS RESPONSE WORD of the Activity Message.

30.4.6.2 Data Words. The number of Data Words will equal the WORD COUNT in the Memory Data Verify Message COMMAND WORD.

30.4.7 Trailer: MLV = RT: TR = 1: SUBADDRESS = 16H.

30.4.7.1 Trailer Bus Data.



The Activity Message shown prior to the Trailer Message requests that the BC command the Trailer Message. The Activity Message will not be used by BCs that keep track of the HEADER, MEMORY DATA, ..., MEMORY DATA, TRAILER Message sequence (i.e., the BC automatically commands this message sequence without the MLV requesting each message in turn).

30.4.7.1.1 Trailer Message Utilization. This message is used to pass the data checksum and additional Load/Verify parameters to the unit.

30.4.7.2 Data Words.

30.4.7.2.1 Data Word 1. DATA WORD 1 will contain the number of sub-pages and the first sub-page for units utilizing this form of paging or sub-paging. This word may also be used for internal register control. These fields represent the values to be used in the next HEADER, MEMORY DATA, ..., MEMORY DATA, TRAILER transaction. For the first HEADER, MEMORY DATA, ..., MEMORY DATA, TRAILER transaction this information will be transmitted prior to the Memory Data transaction via a HEADER, TRAILER transaction in which the TM (Transfer Mode) field in DATA WORD 1 of the Header is 00 (no transfer).

a. Sub-page/Register Count (bits 8-15). This field may be used in lieu of or in conjunction with the Page Number field in DATA WORD 4 of the Header Message and is individual user definable. Unused bits shall equal 0. An example of the use of this field is as follows.

   In order to load 256K of memory into a unit with bank switching and 64K address capability and a page size definition of 2048 words, the following approach might be used.

   To load 256K with sub-pages 2048 words long requires 128 HEADER, MEMORY DATA, ..., MEMORY DATA, TRAILER transactions (256K/2048 = 128). The 128 transactions would consist of 32 transactions for each of the four banks. Thus for each 32 transactions the Header Data 4 Page Number = Bank Number would be incremented (0-3). Within each group of 32 transactions the Sub-page count would increment every transaction (0-31). For each transaction (assuming HT = 01 for Buffer Transfer Count = number of messages) the Header Data 1 Buffer Transfer Count would be 64 (2048 words/32 words per message).

b. First Sub-Page Register (bits 0-7). This field may be used in lieu of or in conjunction with the Page Number field in DATA WORD 4 of the Header Message and is individual user definable. Unused bits shall equal 0. Examples of use would be: specifying the processor register into which Page Number field in data word 4 of the Header Message is to be loaded; or specifying the initial sub-page count in the example above to 1 so as to not reprogram the first 2048 memory locations (the first group of transactions would only be 31 transactions long (1 to 31) and the Sub-page count for the first transaction would be set to 1 to indicate a starting address of 2048).

30.4.7.2.2 Data Word 2.

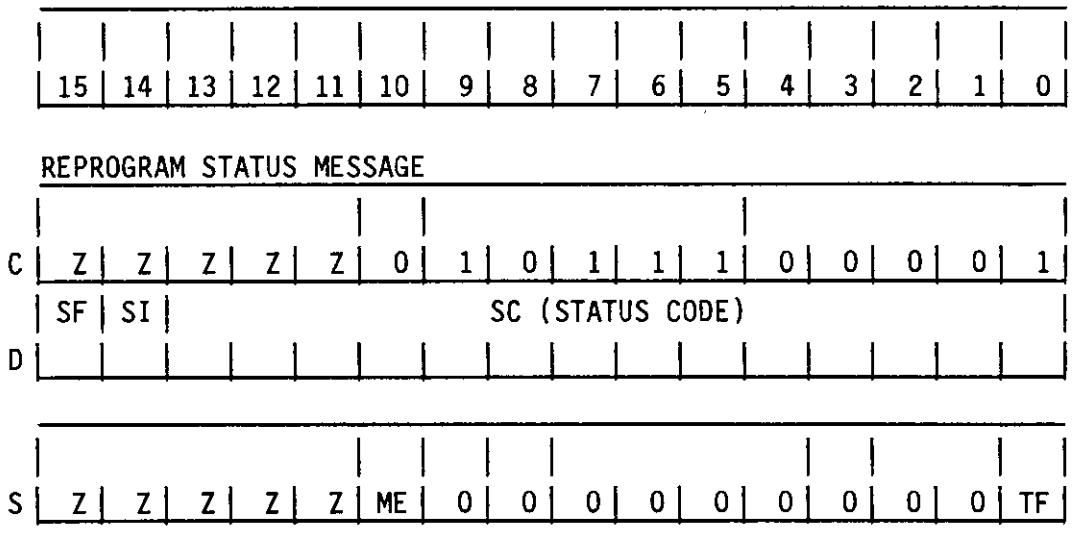
a. Checksum (bits 0-15). The checksum will be the checksum of an entire transaction, i.e., HEADER, MEMORY DATA, ..., MEMORY DATA, TRAILER (when TM in Header Data 1 is not equal to 0) or HEADER, TRAILER (when TM in Header Data 1 is equal to 0). The checksum will be derived by a 2's complement 16 bit addition of every DATA WORD in

the transaction (i.e., Header, Memory Data, and Trailer DATA WORDS) with the exception of the Checksum DATA WORD (Trailer Data 2). The 2's complement 16-bit addition is binary addition with the carry discarded (i.e., no end around carry) (e.g., FFFF (hex) + 1 = 0).

The unit being reprogrammed shall be responsible for comparing the checksum received from the MLV with the data words for both load and verify functions. The Checksum value in DATA WORD 2 of the Trailer is the checksum that should be computed by the unit. If the value computed does not match the value received for either a load or verify operation, an error shall be declared and a Reprogram Status Message shall be sent.

30.4.8 Reprogram Status: MLV = RT: TR = 0: SUBADDRESS = 17H.

30.4.8.1 Reprogram Status Bus Data.



30.4.8.1.1 Reprogram Status Message Utilization. The Reprogram Status Message is used by the BC to inform the MLV of an error condition.

30.4.8.2 Data Words.

30.4.8.2.1 Data Word 1.

a. SF (Status Flag) bit (bit 15). This bit shall be set to 1 to indicate that the remainder of the Data Word should be processed by the MLV. (i.e., Reprogram Status Message contains valid data.) If this bit is set to 0, the Reprogram Status Message will be ignored by the MLV.

b. SI (Status Indicator) bit (bit 14). The SC bit defines the meaning of the remainder of the Data Word namely an error code or a status code to be displayed by the MLV.

   1. SI = 0 indicates that an error has occurred and the error code defined below shall be processed by the MLV.

   2. SI = 1 indicates that no error has occurred and the Status Code in bits 13-0 are to be displayed on the MLV display as 4 hexidecimal characters (bits 15 and 14 of the display value are 0). With SI = 1 the values of bits 13-0 will be used to indicate status or progress through the Load/Verify (ex., increment the value of Status Code after each 1K of data is transferred). The use of SI=1 to display status is optional.

c. SC (Status Code) (bits 0-13). When SF = 1 and SI = 1, these bits are display characters as described in b above. When SF = 1 and SI = 0, these bits represent error codes and the desired MLV action. The error codes are:

   SC = 0001(H) = Abort. This will indicate to the MLV that the Load/Verify has been aborted and should not be retried. The MLV shall display the error code and wait for operator response. On receiving the correct response, the MLV shall abort the load of that unit and continue with the load of the next unit (if it exists).

   SC = 0002(H) = Restart. This will indicate that an unrecoverable error has occurred in the unit being loaded and a reload of the unit is desired. The MLV shall display the error code and wait for operator response. On receiving the correct response, the MLV shall start the load of that unit over again.

SC = 0003(H) = Retry. This will indicate that an error has occurred in the last message sequence transaction and a repeat of the sequence is desired. The MLV shall display the error code and wait for operator response. On receiving the correct response, the MLV shall repeat the last transaction over again.

SC = 0004(H) = Automatic Retry. This will indicate that an error has occurred in the last message sequence transaction. After three consecutive retries, the MLV shall display the error code and wait for operator response. (If the retry is successful before reception of the third consecutive error, operation will continue as normal.) On receiving the correct operator response, the MLV shall abort the load of that unit and continue with the load of the next unit (if it exists).

SC = 0005 - 3FFF(H) = Spare. Not to be utilized without a revision to this standard.

30.4.9 MLV Error: MLV = RT: TR = 1: SUBADDRESS = 17H.

30.4.9.1 MLV Error Bus Data.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ACTIVITY MESSAGE																
C	Z	Z	Z	Z	Z	1	0	0	1	1	1	0	0	0	0	1
S	Z	Z	Z	Z	Z	ME	0	1	0	0	0	0	0	0	0	TF
D	0	0	0	0	0	1	1	0	1	1	1	0	0	0	0	1
MLV ERROR MESSAGE																
C	Z	Z	Z	Z	Z	1	1	0	1	1	1	0	0	0	0	1
S	Z	Z	Z	Z	Z	ME	0	0	0	0	0	0	0	0	0	TF
D	0	0	0	0	0	0	0	0	C	0	0	0	0	A	C	T

30.4.9.1.1 MLV Error Message Utilization. If an MLV error occurs, the MLV will set the BUSY bit in the STATUS RESPONSE WORD for all messages and suppress transmission of any DATA WORDs. The BC will then poll the MLV with Activity Messages. When the MLV is ready for the BC to command the MLV Error Message, it will clear the BUSY bit, set the Service Request bit in the STATUS RESPONSE WORD to the Activity Message, and transmit the DATA WORD requesting that the BC command the MLV Error Message.

30.4.9.2 Data Words.

30.4.9.2.1 Data Word 1.

a. A (Abort) (bit 2). This bit will be set to 1 by the MLV to notify the BC that the Load or Verify has been aborted and that no further retries will be made.

b. C (Complete Restart) (bit 1). This bit will be set to 1 by the MLV to notify the BC that an unrecoverable error has occurred and all Memory Data Load or Memory Data Verify transactions will be re-started.

c. T (Transaction) (bit 0). This bit will be set to 1 by the MLV to notify the BC that there was an error detected in the last HEADER, MEMORY DATA, ..., MEMORY DATA, TRAILER or HEADER, TRAILER transaction and that the transaction will be repeated.

d. Other bits (bits 3-15). Bits 3-15 shall equal 0.

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APPENDIX D

MESSAGE FORMATS MLV = BC, AN/AYK-14 SIM-B = RT

40. AN/AYK-14 WITH A SERIAL INTERFACE MODULE (SIM) TYPE B ACTING AS AN RT.

40.1 Applicability. The protocol of this Appendix is applicable to the AN/AYK-14 with a Serial Interface Module (SIM) Type B acting as an RT for the bootload operation. This appendix is also applicable to an AYK-14 with a Discrete Serial Module (DSM) emulating the SIM Type B. The protocol of this Appendix shall not be used for new designs without written approval of NAVAIRSYSCOM. Additional protocol information can be found in the Naval Avionic Center (NAC) documents listed in Section 2.

40.2 General Operation.

a. Once the AN/AYK-14 recognizes the IPL discrete (see Section 5.2.2.2.3), the AN/AYK-14 bootloader shall determine if it is to be a remote terminal and what RT address is to be used. This is determined via external jumper wire inputs to the AN/AYK-14 (an even RT number means the AN/AYK-14 is to be the RT). If no jumpers are present on the AN/AYK-14 inputs, the AN/AYK-14 will default to the protocol of Appendix G. If there is no response from the MLV to the Initialize Device Message of Appendix G (there will be no response from the MLV when this protocol (Appendix D) has been selected), then the AN/AYK-14 will default to the protocol of this appendix. After setting the discretes to ensure that the AN/AYK-14 will recognize the IPL, the MLV acting as BC will transfer the Initiate Load Message to place the RT in the program download mode (see Figure 12). The MLV then polls the RT with IPL Read Messages until the Busy bit is cleared in the STATUS RESPONSE WORD. If the Busy bit is still set high after one second, a timeout occurs and the load operation is terminated.

b. Once the AN/AYK-14, acting as the RT, enters the load mode, any indication of an unsuccessful load attempt will terminate the load operation. In this configuration no retries or alternate bus switching are permitted.

c. A successful IPL Read Message tells the RT to prepare to receive a data record. The MLV polls the RT with Get Status Messages until the Data Ready bit is set high and the Busy bit set low in the STATUS RESPONSE WORD. The MLV then transfers the Header Message.

d. Prior to the transfer of the first Memory Data Load Message of a data record, the MLV will poll the RT with Get Status Messages until the Data Ready bit is set high and the Busy bit set low in the STATUS RESPONSE WORD. This response notifies the MLV that the Header transfer is complete and that the AN/AYK-14 is prepared for a

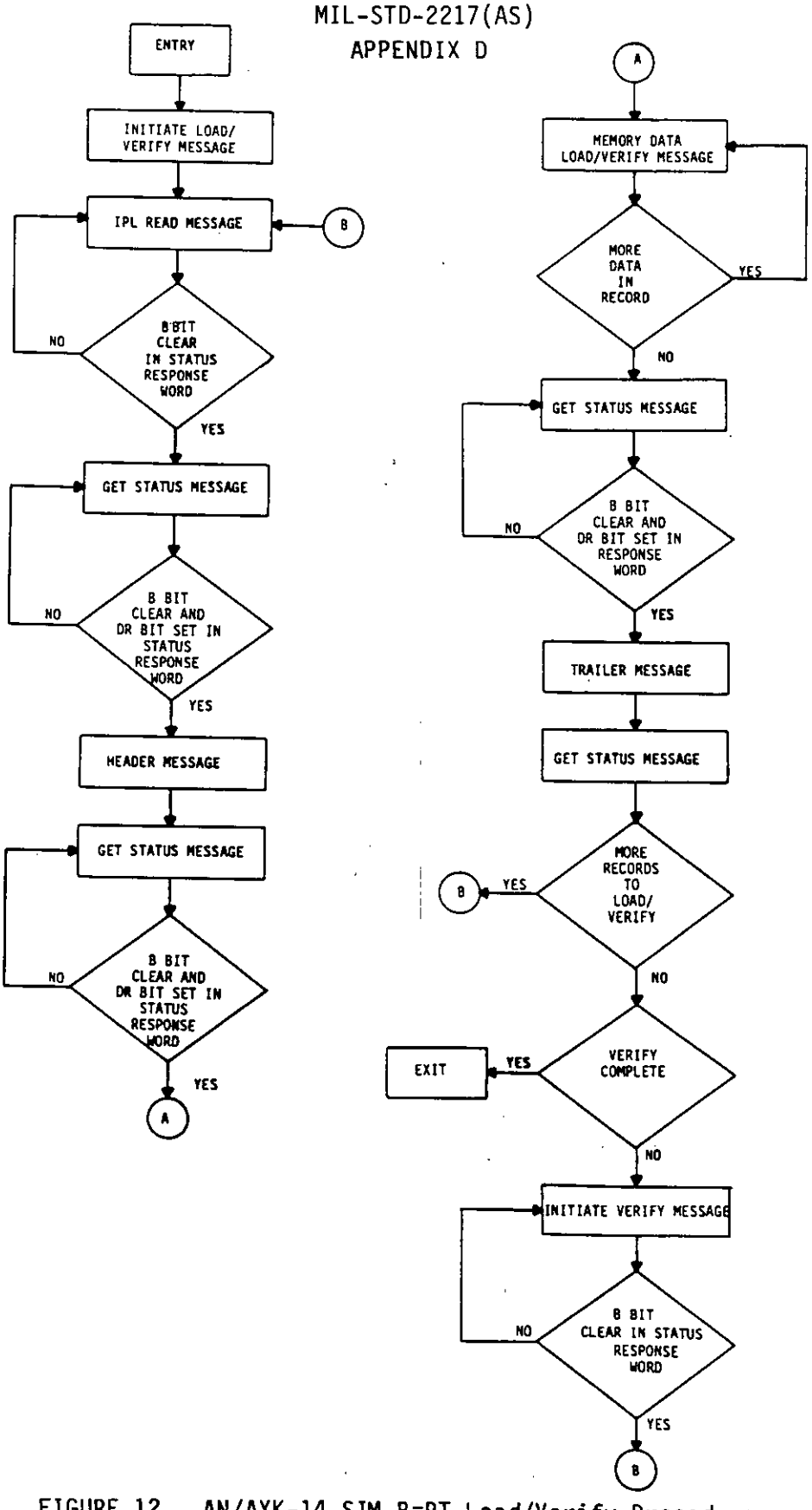


FIGURE 12. AN/AYK-14 SIM-B=RT Load/Verify Procedure.

data record transfer. All subsequent Memory Data Load Messages in the data record are sent contiguously with no Get Status Message polling interspersed.

e. Once all of the data in the record has been transferred, the MLV polls the RT with Get Status Messages until the Data Ready bit is set high and the Busy bit set low in the STATUS RESPONSE WORD. The MLV then sends the Trailer Message followed by a Get Status Message. After receipt of the Trailer Message the AN/AYK-14 will compute the Checksum and an error will terminate the load operation (set IPL fail) in which case the entire loading process including the setting of discretes must be repeated. If another record is to be loaded, the MLV repeats the load procedure by sending the IPL Read Message.

f. If the load is complete and if the MLV is to verify the load, an Initiate Verify Message is transferred. This message shall be commanded by the MLV within 2 seconds after the successful Get Status Message at the end of the load. If this message is not received, the AN/AYK-14 Bootstrap Loader will begin execution of the program at the Program Entry Address. If the Busy bit is set high in the STATUS RESPONSE WORD for the Initiate Verify Message, the MLV will repeat the Initiate Verify Message until the Busy bit is set low. After an RT STATUS RESPONSE WORD for the Initiate Verify Message with the Busy bit set low, the MLV will proceed with the IPL Read Message.

g. The program verify (upload) follows the same procedure as the program load with the only differences being the direction of the memory data flow and the Checksum is computed by the MLV.

h. The Initiate Load Message, the Initiate Verify Message, and the IPL Read Message use mode code 11H (17 decimal) with the message identified in the DATA WORD. The Header, Memory Data Load, Memory Data Verify, and Trailer Messages all use subaddress 1 messages and the assumption is made that all data will follow in the proper order.

40.3 Status Response Word: MLV = BC.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
S	TERMINAL ADDRESS					ME		DR					B			TF
	Y	Y	Y	Y	Y		X		X	X	X	X		X	X	

A STATUS RESPONSE WORD will be provided by the RT for each message transaction. The STATUS RESPONSE WORD will follow the data on an RT receive type transaction and will precede the data on an RT transmit type transaction. The MLV will allow a response time gap of 12 usec from the end of the last transmitted COMMAND WORD (transmit type message) or the end of the last transmitted DATA WORD (receive type message), to the start of the RT STATUS RESPONSE WORD before declaring a no response error (equivalent of 14 usec when measured in accordance with MIL-STD-1553B). Under normal conditions the RT shall begin the STATUS RESPONSE WORD within the period of 2-10 usec from the receipt of the end of the last COMMAND WORD (transmit type message) or the receipt of the end of the last DATA WORD (receive type message) (equivalent of 4-12 usec when measured in accordance with MIL-STD-1553B). The STATUS RESPONSE WORD bits are as follows:

a. Terminal Address (bits 11-15). The RT address will be the address assumed by the AYK-14 BC when it determines it is to be reprogrammed in the remote terminal mode. This address will be determined via jumper wire inputs to the AN/AYK-14 and by the Aircraft Type and Aircraft Configuration Modification information provided to the MLV as well as the particular bus selected by the MLV switching network. Throughout the remainder of this appendix this address shall be referred to as YYYYY.

b. ME bit (bit 10). The Message Error (ME) bit may be set high (= 1) by the RT under any of the following conditions:

   1. message short in data word count
   2. failure to pass word validation
   3. improperly timed data sync
   4. non-contiguous data
   5 undefined subaddress/mode code

   Since no retries are allowed on the MIL-STD-1553B bus with the AYK-14 in the RT mode, the setting of the Message Error bit will indicate that AYK-14 has terminated the Load/Verify operation.

c. DR bit (bit 8). The Data Ready (DR) bit will be set high (= 1) by the RT to indicate that a data transfer (Header, Memory Data or Trailer Message) may proceed. The MLV will examine this bit in the

STATUS RESPONSE WORDS associated with Get Status Messages. The DR bit may be set for no longer than two seconds or the load will be terminated.

d. B bit (bit 3). The Busy (B) bit will be set high (= 1) by the RT during the Load/Verify initialization period to indicate that the bootstrap loader has not entered the Load/Verify mode or during the Load/Verify sequence to indicate that the RT has not completed buffer pointer setup.

e. TF bit (bit 0). The Terminal Flag (TF) bit will be set high (= 1) by the RT to indicate a failure in the Bootstrap Loader itself.

f. Other bits. Bits 1, 2, 4-7, and 9 will not be utilized by the MLV; thus, these bits may be 1 or 0.

40.3.1 Message Timing. For message transactions not using mode codes in the COMMAND WORD (i.e., Header, Memory Data Load/Verify, and Trailer Messages) the MLV will ensure that the time from the end of the RT transmission of the last DATA WORD (transmit type message), or the end of the STATUS RESPONSE WORD (receive type message) to the beginning of the next COMMAND WORD is at least 8 usec (equivalent of 10 usec when measured in accordance with MIL-STD-1553B). For all message transactions using mode codes in the COMMAND WORD, the MLV will ensure that the time from the end of the RT transmission of the STATUS RESPONSE WORD to the beginning of the next COMMAND WORD is at least one millisecond (1 msec). This is required to guarantee that the RT receives all the DATA WORDS correctly and in the proper sequence and to preclude an improper or aborted load.

40.4 Messages.

40.4.1 Get Status Message: MLV = BC: TR = 1: MODE CODE = 01H.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C	Y	Y	Y	Y	Y	1	0	0	0	0	0	0	0	0	0	1
S	Y	Y	Y	Y	Y	ME	X	DR	X	X	X	X	B	X	X	TF

The Get Status Message is used by the MLV to ascertain the readiness of the RT for message transactions and data transfers. The MLV must send the Get Status Message before the Header Message and after the Header Message, the last Memory Data Message, and the Trailer Message. This will notify the RT that these transfers are complete and that the RT can prepare for the next data transfer.

40.4.1.1 Status Response Word. The STATUS RESPONSE WORD for this message shall be as defined in 40.3 of this appendix; bits 3 and 8 are used as follows:

a. DR bit (bit 8). The Data Ready (DR) bit shall be set high (= 1) by the RT to indicate that the AYK-14 is prepared for a transfer of data. It is used in Get Status Messages prior to Header, Memory Data Load/Verify and Trailer Messages. This bit shall be set by the RT whenever data is ready to be transferred.

b. B bit (bit 3). The Busy (B) bit is set high (= 1) for the STATUS RESPONSE WORD to the IPL Read Message during the initialization period (after transfer of the Initiate Load/Verify Message) to indicate that the RT is not ready for the data record transfer to proceed. The bit is lowered to indicate that initialization is complete. This bit is also set high for the STATUS RESPONSE WORD to Get Status Messages in order to allow RT setup prior to the transfer of Header, Data, or Trailer Messages.

40.4.2 Initiate Load Message: MLV = BC: TR = 0: MODE CODE = 11H.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C	Y	Y	Y	Y	Y	0	0	0	0	0	0	1	0	0	0	1
D	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0
S	Y	Y	Y	Y	Y	ME	X	X	X	X	X	X	X	X	X	TF

The Initiate Load Message is used to initialize the bootstrap loader of the AN/AYK-14 to perform the download function. The COMMAND WORD is the Synchronize with Data mode command (mode code = 11H) and the associated DATA WORD (value = 14H) is the message identifier, indicating that the RT is to enter the program load mode (Download).

40.4.3 Initiate Verify Message: MLV = BC: TR = 0: MODE CODE = 11H.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C	Y	Y	Y	Y	Y	0	0	0	0	0	0	1	0	0	0	1
D	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	1
S	Y	Y	Y	Y	Y	ME	X	X	X	X	X	X	X	X	X	TF

The Initiate Verify Message is used to initialize the AN/AYK-14 bootstrap loader to perform the upload (verify) function. The COMMAND WORD is the Synchronize with Data mode command (mode code = 11H) and the associated DATA WORD (value = 13H) is the message identifier, indicating that the RT is to enter the program verify mode (Upload). The Initiate Verify Message must be transferred within two seconds after the conclusion of the load operation if a verify of the memory load is desired. Otherwise, the AN/AYK-14 will abort the reprogramming mode and begin execution of the normal operating program. This message is called the Initialize Upload Message in the Naval Avionics Center document entitled "Program Performance Specification Advanced Bootstrap Loader for AN/AYK-14(V) Single Card Processor."

40.4.4 IPL Read Message: MLV = BC: TR = 0: MODE CODE = 11H.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C	Y	Y	Y	Y	Y	0	0	0	0	0	0	1	0	0	0	1
D	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1
S	Y	Y	Y	Y	Y	ME	X	X	X	X	X	X	B	X	X	TF

The IPL Read Message is used to prepare the AN/AYK-14 bootstrap loader for a HEADER, MEMORY DATA, ..., MEMORY DATA, TRAILER transaction. The COMMAND WORD is the Synchronize with Data mode command (mode code = 11H) and the associated DATA WORD (value = 15H) is the message identifier, indicating that the RT is to prepare to receive/send data depending on whether the RT is in a Load/Verify mode. This message is used as a polling message at the beginning of each transaction. The IPL Read Message will continue to be sent until the B bit is cleared in the STATUS RESPONSE WORD.

40.4.5 Header: MLV = BC: TR = 0: SUBADDRESS = 01H.

40.4.5.1 Header Bus Data.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GET STATUS MESSAGE																
C	Y	Y	Y	Y	Y	1	0	0	0	0	0	0	0	0	0	1
								DR					B			
S	Y	Y	Y	Y	Y	ME	X	1	X	X	X	X	0	X	X	TF
HEADER MESSAGE																
C	Y	Y	Y	Y	Y	0	0	0	0	0	1	0	0	1	0	0
	TM					BUFFER TRANSFER COUNT										
D1			0	0												
	INITIAL LOAD ADDRESS															
D2																
	PROGRAM ENTRY ADDRESS															
D3																
	PAGE NUMBER														TC	
D4														0		
S	Y	Y	Y	Y	Y	ME	X	X	X	X	X	X	X	X	X	TF

Once the IPL Read Message polling is complete, the first response to a Get Status Message with the DR bit set high (= 1) and the B bit clear (= 0) in the STATUS RESPONSE WORD indicates that the RT is ready for the Header Message to be transferred.

40.4.5.1.1 Header Message Utilization. This message is used to pass Load/Verify information to the unit.

40.4.5.2 Data Words.

40.4.5.2.1 Data Word 1.

a. TM (bits 14-15). The Transfer Mode (TM) bits are used to describe the Memory Data Load DATA WORD content. The TM bits are binary coded as follows:

1. TM = 00 No transfer. In the No Transfer Mode the Buffer Transfer Count and Initial Load Address have no meaning. This mode is used to transfer the Program Entry Address and Page Number or is used as a preamble to the Trailer Message.

2. TM = 01 Not used. An AN/AYK-14 IPL fail will occur and processor will hang if this code were used.

3. TM = 10 16 bit transfer. Each 16 bits of data transmitted in a DATA WORD will contain 16 bits of information in bits 0-15.

4. TM = 11 32 bit transfer. The 16 bits of data transmitted in each odd word (first word is odd) contains the 16 LSB of data in bits 0-15 and each even word contains the 16 MSB of data in bits 0-15.

b. Buffer Transfer Count (bits 0-11). The Buffer Transfer Count is used to indicate the amount of data that will follow the Header Message. The Buffer Transfer Count has no meaning when the Transfer Mode is 00. The range of the Buffer Transfer Count is 1-4096 (value of zero equals 4096). The Buffer Transfer Count is the total number of DATA WORDS that will be transmitted after the Header. The DATA WORDS will be transmitted in 32-word messages with the last message containing the remaining 32 or less words. The maximum transfer is 4096 words using 128 Memory Data Load Messages.

c. Other bits. Bits 12 and 13 shall be zero.

40.4.5.2.2 Data Word 2.

a. Initial Load Address (bits 0-15). The Initial Load Address is the 16 or less LSB of the point in memory into which data is to be loaded. The maximum value (number of bits) used in the Initial Load Address will be compatible with the page size of units using paging. Unused bits shall be set to zero.

40.4.5.2.3 Data Word 3.

a. Program Entry Address (bits 0-15). The Program Entry Address has meaning only for Transfer Mode = 00. The Program Entry Address is the 16 or less LSB of the point in memory at which the unit being reprogrammed is to begin execution. The maximum value (number of bits) used in the Program Entry Address will be compatible with the page size of units using paging. Unused bits shall equal zero.

40.4.5.2.4 Data Word 4.

a. Page Number (bits 3-15). The Page Number represents up to 13 MSBs for page memory address. The Page Number applies to the Program Entry Address for Transfer Mode = 00. The Page Number applies to the Initial Load Address for Transfer Mode 10 and 11. Unused bits shall equal zero.

b. TC bits (bit 0-1). The Transfer Control (TC) may be used to transfer control to the program loaded after reprogramming.

   1. Transfer Control = 00 indicates this is the last HEADER, MEMORY DATA, ..., MEMORY DATA, TRAILER or HEADER, TRAILER transaction.

   2. Transfer Control = 01 indicates that more data is to follow the current HEADER, MEMORY DATA, ..., MEMORY DATA, TRAILER or HEADER, TRAILER transaction and control should not be transferred. For units using paging and the Program Entry Address, the TC will remain = 01, even for the last data transaction, until a Transfer Mode = 00 message is used to supply the Program Entry Address and Page Number.

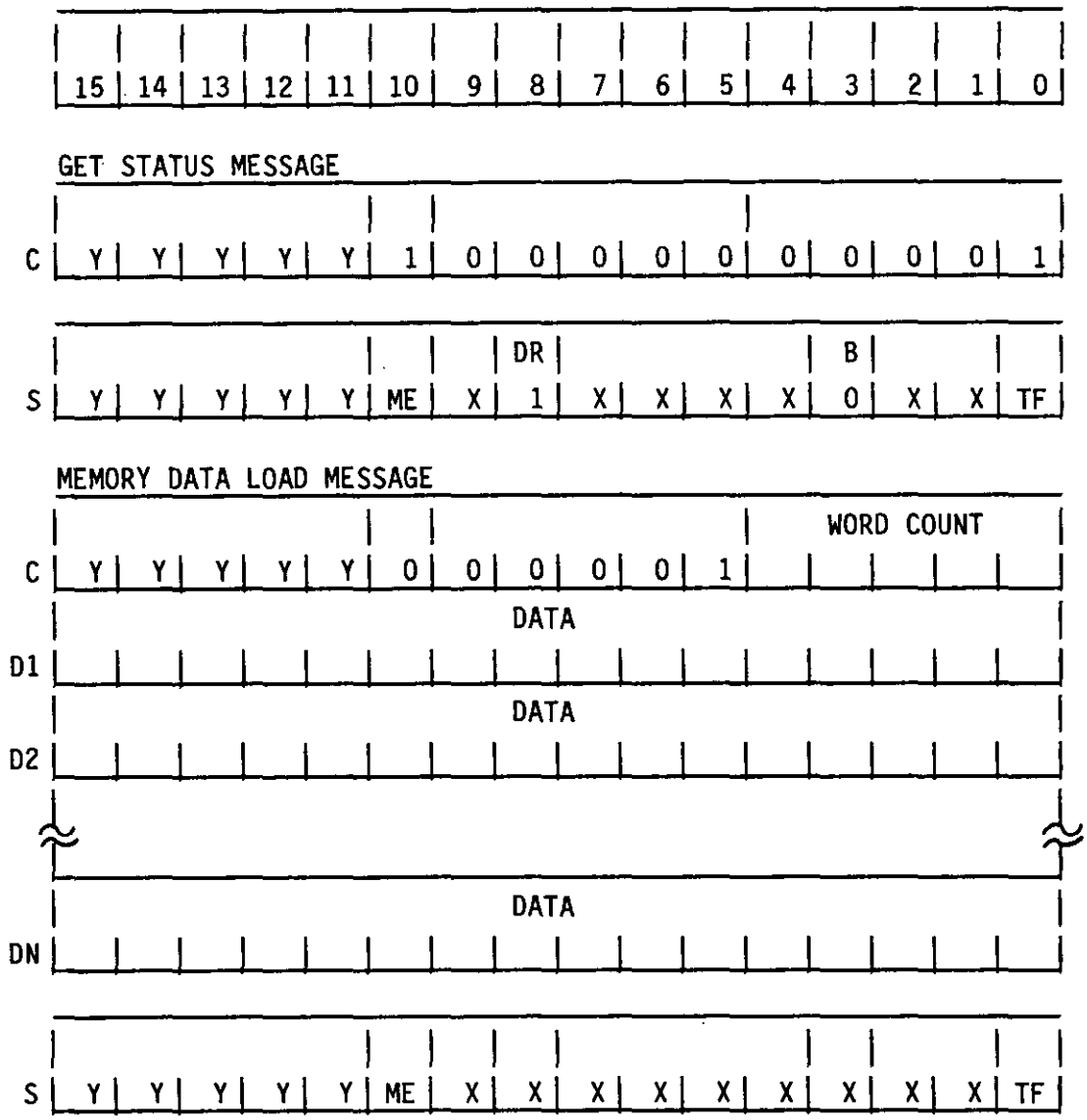
   3. Transfer Control = 10 shall indicate that control is to be transferred to the Program Entry Address. When control is transferred, the action shall not take place until after the Trailer Message and shall transfer control only to non-reprogrammed areas or verified areas.

   4. Transfer Control = 11 is invalid.

c. Other Bits (bit 2). Bit 2 shall equal 0.

40.4.6 Memory Data Load: MLV = BC: TR = 0: SUBADDRESS = 01H.

40.4.6.1 Memory Data Load Bus Data.



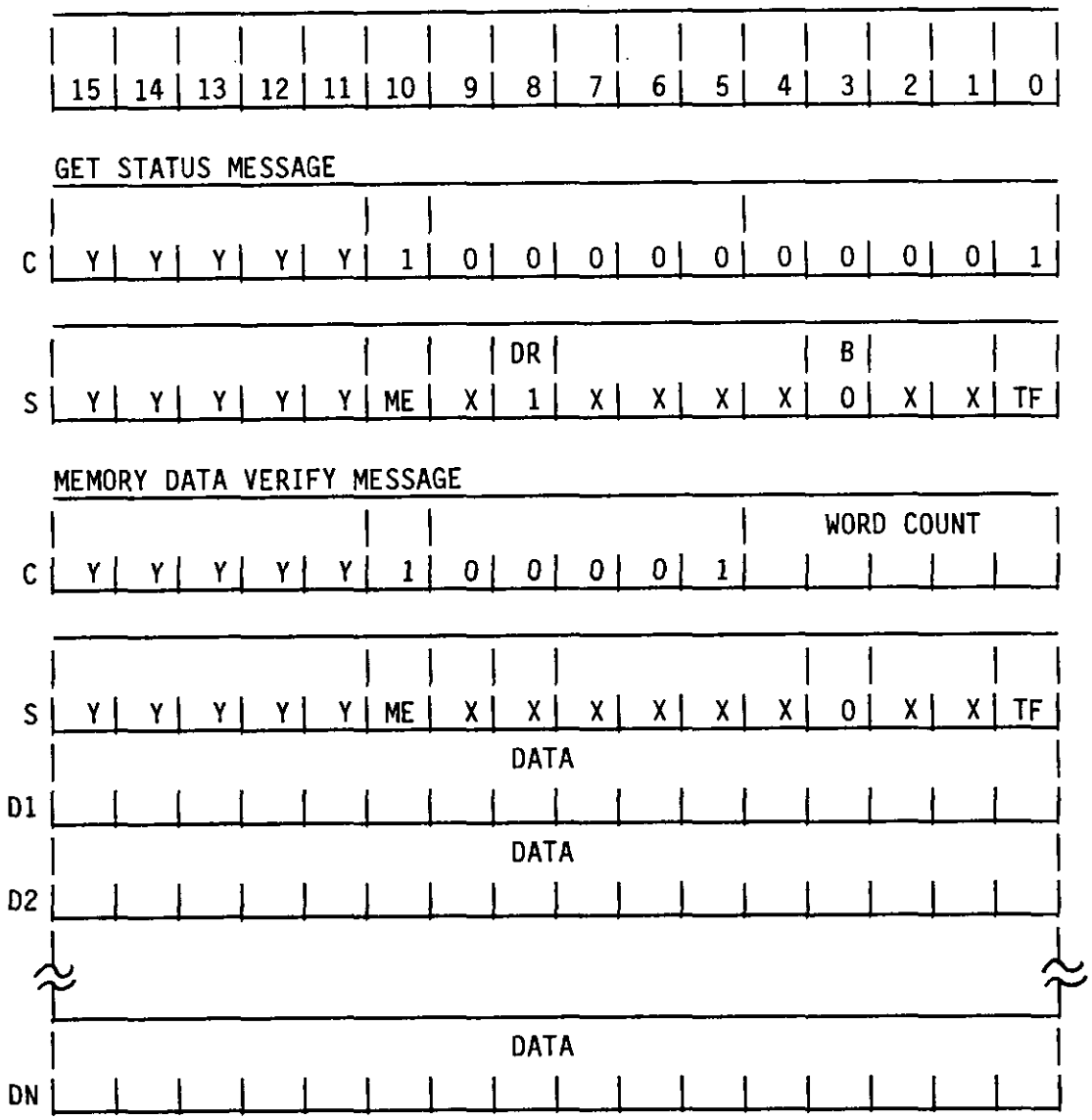
The Get Status Message shown prior to the Memory Data Load Message will only be present prior to the first Memory Data Load Message in a record transfer. The B bit clear (= 0) and the DR bit set (= 1) in the STATUS RESPONSE WORD for the Get Status Message indicates that the entire sequence of Memory Data Load Messages for a record may be transferred.

40.4.6.1.1 Memory Data Load Message Utilization. This message is used to pass the data to be loaded into the unit memory.

40.4.6.2 Data Words. The number of Data Words will equal the WORD COUNT in the Memory Data Load Message COMMAND WORD.

40.4.7 Memory Data Verify: MLV = BC: TR = 1: SUBADDRESS = 01H.

40.4.7.1 Memory Data Verify Bus Data.



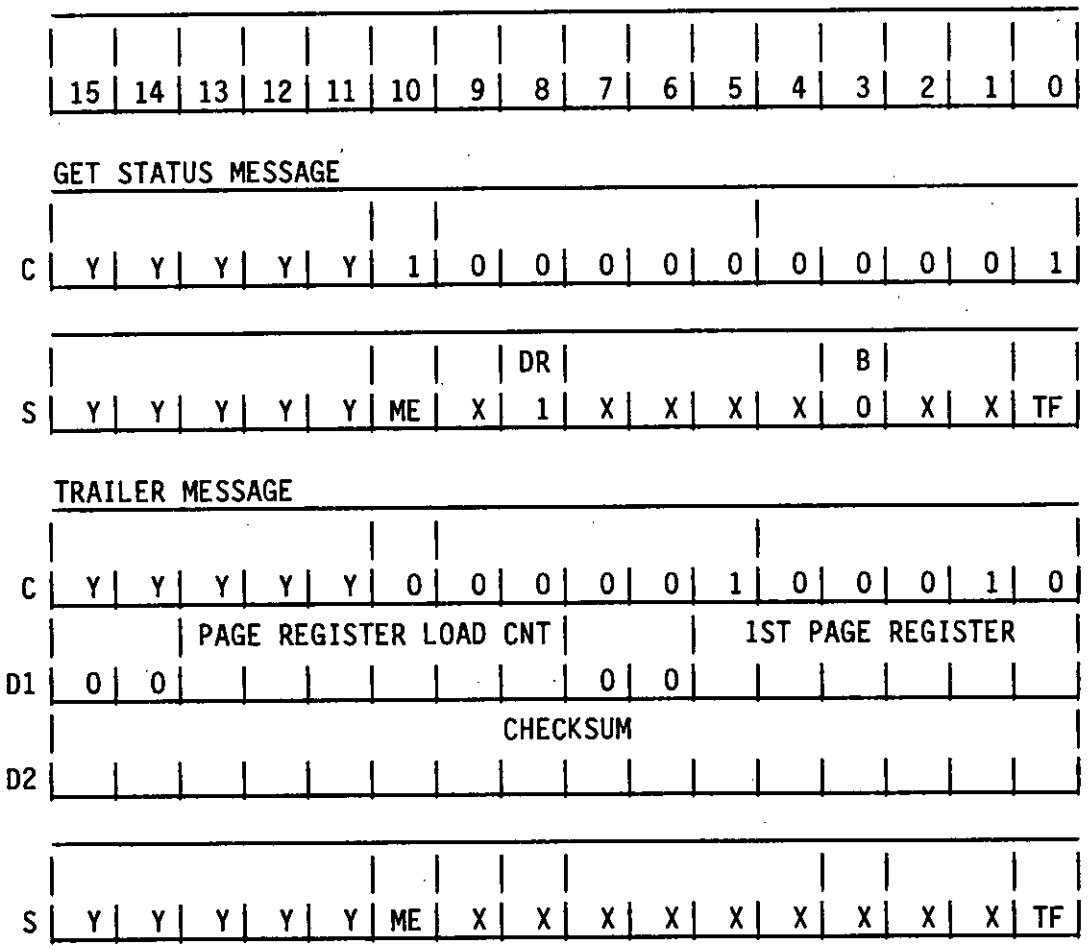
The Get Status Message shown prior to the Memory Data Verify Message will only be present prior to the first Memory Data Verify Message in a record transfer. The B bit clear (= 0) and the DR bit set (= 1) in the STATUS RESPONSE WORD for the Get Status Message indicates that the entire sequence of Memory Data Verify Messages for a record may be transferred.

40.4.7.1.1 Memory Data Verify Message Utilization. This message is used to pass the data that the MLV will compare to the data stored on the MSD.

40.4.7.2 Data Words. The number of Data Words will equal the word count in the Memory Data Verify Message COMMAND WORD.

40.4.8 Trailer: MLV = BC: TR = 0: SUBADDRESS = 01H.

40.4.8.1 Trailer Bus Data.



Once all Memory Data Load/Verify Messages for a HEADER, MEMORY DATA, ..., MEMORY DATA, TRAILER transaction have been transferred (or after a Header Message with TM = 00), the first response to a Get Status Message with the DR bit set (= 1) and the B bit clear (= 0) in the STATUS RESPONSE WORD indicates that the RT is ready for the Trailer Message to be transferred. After the Trailer Message is transferred an additional Get Status Message will be transferred to complete the record transaction.

40.4.8.1.1 Trailer Message Utilization. This message is used to pass the data checksum and additional Load/Verify parameters to the unit.

40.4.8.2 Data Words.

40.4.8.2.1 Data Word 1.

a. Page Register Load Count (bits 8-13). The Page Register Load Count field specifies the number of consecutive pages needed to load the succeeding data record. The value of this number is written as one less than the actual number of pages (e.g., a count of zero in this field indicates that one page register is to be loaded). However, when the Page Number in the fourth word of the Header indicates Page Number zero, a zero in this field indicates that no (zero) page registers are to be loaded.

b. First Page Register (bits 0-5). This field specifies the number of the first page register which is to be modified with the page number given in the fourth word of the Header. Any attempt to modify page register zero (0) shall result in a load error.

c. Other bits. Bits 6-7 and 14-15 are not used and are set to zero.

40.4.8.2.2 Data Word 2.

a. Checksum (bits 0-15). The checksum will be the checksum of an entire transaction, i.e., HEADER, MEMORY DATA, ..., MEMORY DATA, TRAILER (when TM in Header Data 1 is not equal to zero) or HEADER, TRAILER (when TM in Header Data 1 is equal to zero). The checksum will be derived by a 2's complement 16 bit addition of every DATA WORD in the transaction (i.e., Header, Memory Data Load, and Trailer DATA WORDS) with the exception of the Checksum DATA WORD (Trailer Data 2). The 2's complement 16-bit addition is binary addition with the carry discarded (i.e., no end around carry) (e.g., FFFF (hex) + 1 = 0).

40.4.8.2.2.1 Comparing the Checksum. The unit being reprogrammed shall be responsible for comparing the checksum received from the MLV with the DATA WORDS received during a load operation. The checksum value in the second DATA WORD of the Trailer is the checksum that should be computed by the unit. If the value computed does not match the value received, the IPL fail indicator is set and the load shall be terminated. The MLV will compute the checksum of the DATA WORDS received during a verify operation.

APPENDIX E

MESSAGE FORMATS MLV = RT, AN/AYK-14 SIM-B = BC

50. AN/AYK-14 WITH A SERIAL INTERFACE MODULE (SIM) TYPE B ACTING AS A BC.

50.1 Applicability. The protocol of this Appendix is applicable to the AN/AYK-14 with a Serial Interface Module (SIM) Type B acting as a BC for the bootload operation. This appendix is also applicable to the AYK-14 with a Discrete Serial Module (DSM) emulating the SIM Type B. The protocol of this appendix shall not be used for new designs without written approval of NAVAIRSYSCOM. Additional protocol information can be found in the Naval Avionics Center (NAC) documents listed in Section 2.

50.2 General Operation.

a. Once the AN/AYK-14 recognizes the IPL discrete from the MLV (see Section 5.2.2.2.3) the AN/AYK-14 bootloader shall determine if it is to be the bus controller and what RT address is to be used for the MLV. This is determined via external jumper wire inputs to the AYK-14. The AN/AYK-14 acting as the bus controller (BC) then sends the Initiate Load Message to the MLV (see Figure 13). The BC will then poll the MLV with Get Status Messages until the Busy bit is set low in the STATUS RESPONSE WORD.

b. After a successful initialization, the BC sends the IPL Read Message which tells the MLV to ready a record of data for transfer. The BC polls the MLV with Get Status Messages until the Data Ready (DR) bit is set high (bit 8 = 1) in the STATUS RESPONSE WORD. The Header Message is then transferred to the BC.

c. Prior to the transfer of each Memory Data Load Message, the BC will poll the MLV with Get Status Messages until the DR bit is set in the STATUS RESPONSE WORD. Prior to the transfer of the first Memory Data Load Message, because of an anomaly in the BC loader which fails to recognize the Data Ready bit in the STATUS RESPONSE WORD of a Get Status Message after the Header Message, a second Get Status Message will be sent. Once all the data in the record has been transferred, the BC will again poll for the DR bit set and then command transfer of the Trailer Message. The BC will then compute and verify the checksum. If the checksum is correct and more records are to be loaded, the above process will repeat with the IPL Read Message.

d. There is no verify operation for this AN/AYK-14 protocol.

e. The Initiate Load Message and IPL Read Message both use mode code 11H (17 decimal) with the message identifier in the DATA WORD. The Header, Memory Data Load, and Trailer Messages all use subaddress 1 messages and the assumption is made that all data will follow in the proper order.

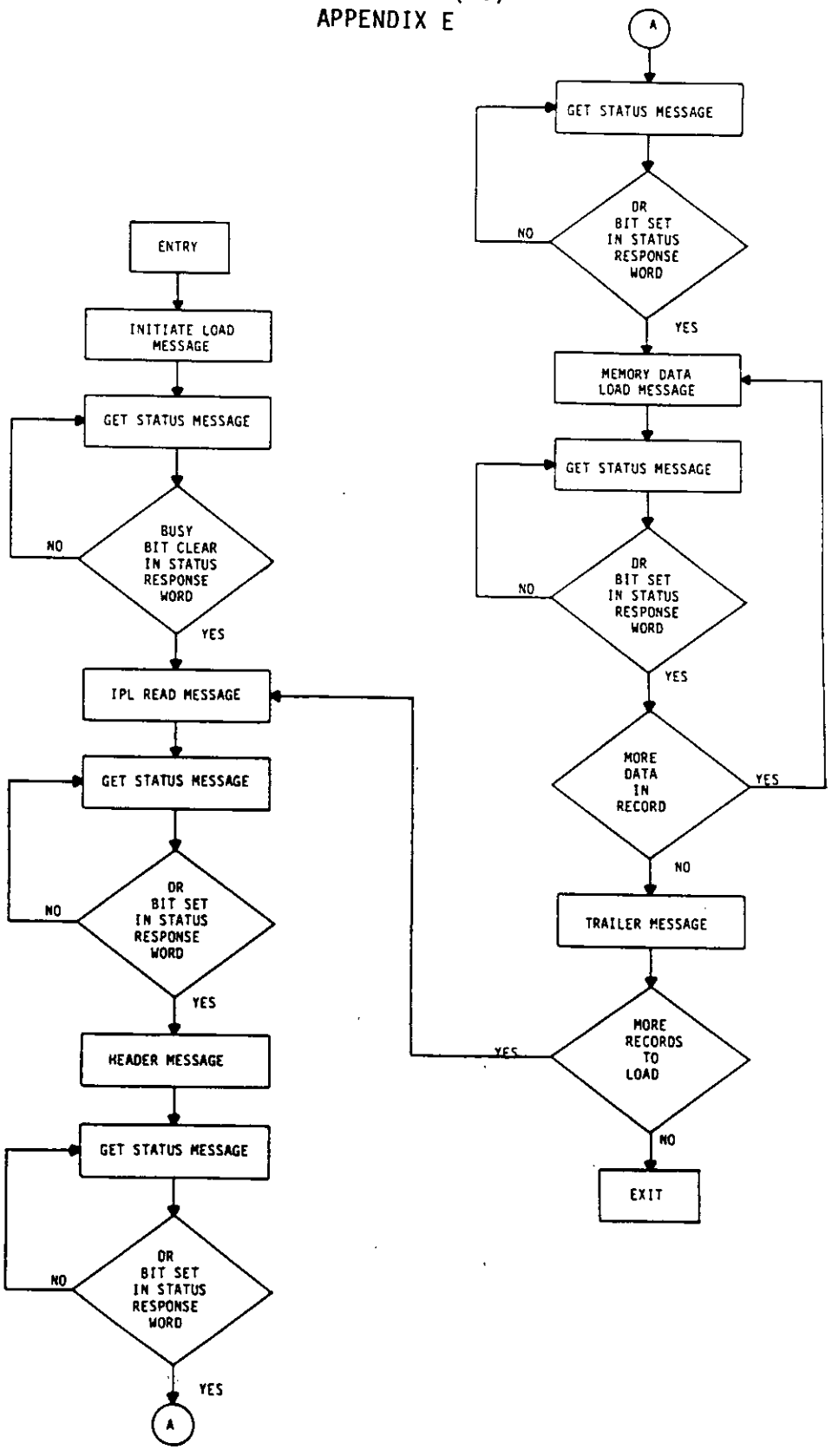


FIGURE 13. AN/AYK-14 SIM-B=BC Load Procedure.

50.3 Status Response Word: MLV = RT.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
S	TERMINAL ADDRESS					ME		DR					B			TF
	Y	Y	Y	Y	Y		0		0	0	0	0		0	0	

A STATUS RESPONSE WORD will be provided by the MLV acting as the RT for each message transaction. This word will precede the data transferred to the BC in the Header Message, Memory Data Load Message and Trailer Message. The BC will allow a response time gap of at least 6.5 usec from the end of the last transmitted COMMAND WORD to the start of the MLV STATUS RESPONSE WORD before declaring a no response error (equivalent of 8.5 usec when measured in accordance with MIL-STD-1553B). Under normal conditions the MLV shall begin the STATUS RESPONSE WORD within the period of 2-5 usec from the receipt of the end of the last COMMAND WORD (equivalent of 4-7 usec when measured in accordance with MIL-STD-1553B). The BC will ensure that the time from the end of the MLV transmission of the last STATUS RESPONSE WORD (receive type message or Mode Code) or the end of the last DATA WORD (transmit type message) to the beginning of the next COMMAND WORD is at least 2 usec (equivalent of 4 usec when measured in accordance with MIL-STD-1553B).

a. TERMINAL ADDRESS (bits 11-15). The RT address will be the address assumed by the SIM-B when the Load/Verify operation is performed with the AYK-14 SIM-B acting as BC. This address will be determined via jumper wire inputs to the AYK-14 and by the Aircraft Type and Aircraft Configuration modification information provided to the MLV as well as the particular bus selected by the MLV switching network. Throughout the remainder of this appendix, this address will be referred to as YYYYY.

b. ME bit (bit 10). The Message Error (ME) bit may be set high (= 1) by the MLV under any of the following conditions:

   1. message short in data word count
   2. failure to pass word validation
   3. improperly timed data sync
   4. non-contiguous data
   5. undefined subaddress/mode code

c. DR bit (bit 8). The MLV will set the Data Ready (DR) bit high (= 1) to indicate that a data transfer (Header, Memory Data Load, or Trailer Message) may proceed.

d. B bit (bit 3). The MLV will set the Busy (B) bit high (= 1) during the load initialization period (after receipt of the Initialize Load Message) to indicate that it is not ready for a data record transfer.

e. TF bit (bit 0). The Terminal Flag (TF) bit will be set high (= 1) to indicate that the MLV is not functioning properly.

f. Other bits. Bits 1, 2, 4-7 and 9 will be zero.

50.4 Messages.

50.4.1 Get Status Message: SIM-B = BC: TR = 1: MODE CODE = 01H.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	GET STATUS MESSAGE															
C	Y	Y	Y	Y	Y	1	0	0	0	0	0	0	0	0	0	1
S	Y	Y	Y	Y	Y	ME	0	DR	0	0	0	0	B	0	0	TF

The Get Status Message is used by the BC to determine when the MLV is prepared to transfer the Header Message, Memory Data Load Message(s), or Trailer Message. It is also used during the initialization period (after the Initiate Load Message) to alert the BC that the MLV does not have a record of data ready for transfer and that the BC should not yet send the IPL Read Message.

50.4.1.1 Status Response Word. The STATUS RESPONSE WORD to this message shall be as defined previously in this appendix; bits 3 and 8 are used as follows:

a. DR bit (bit 8). The Data Ready (DR) bit shall be set high (= 1) by the MLV to indicate that it is ready to transfer data to the BC. It is used in Get Status Messages prior to Header, Memory Data Load, and Trailer Messages.

b. B bit (bit 3). The Busy (B) bit is set high (= 1) by the MLV to indicate that it has not been initialized (viz. does not have a record of data ready for transfer). The BC will poll the MLV for approximately 3.5 minutes (1 second if other than AN/AYK-14 channel 1 communications) and if the B bit has not been lowered will try communications on the alternate bus.

50.4.2 Initiate Load Message: MLV = RT: TR = 0: MODE CODE = 11H.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INITIATE LOAD MESSAGE																
C	Y	Y	Y	Y	Y	0	0	0	0	0	0	1	0	0	0	1
D	0	0	0	0	0	X	0	0	0	0	0	1	0	1	0	0
S	Y	Y	Y	Y	Y	ME	0	X	0	0	0	0	X	0	0	TF

The AN/AYK-14 bootstrap loader begins the load by issuing the Initiate Load Message. This message is interpreted by the MLV, causing it to enter the initial program load mode, reset the load media, and prepare to transfer load records to the bootstrap loader. The COMMAND WORD is the Synchronize with Data mode command (mode code = 11H) and the associated DATA WORD (value = 14H) is the message identifier, indicating that the MLV is to prepare to load the BC (Program Download).

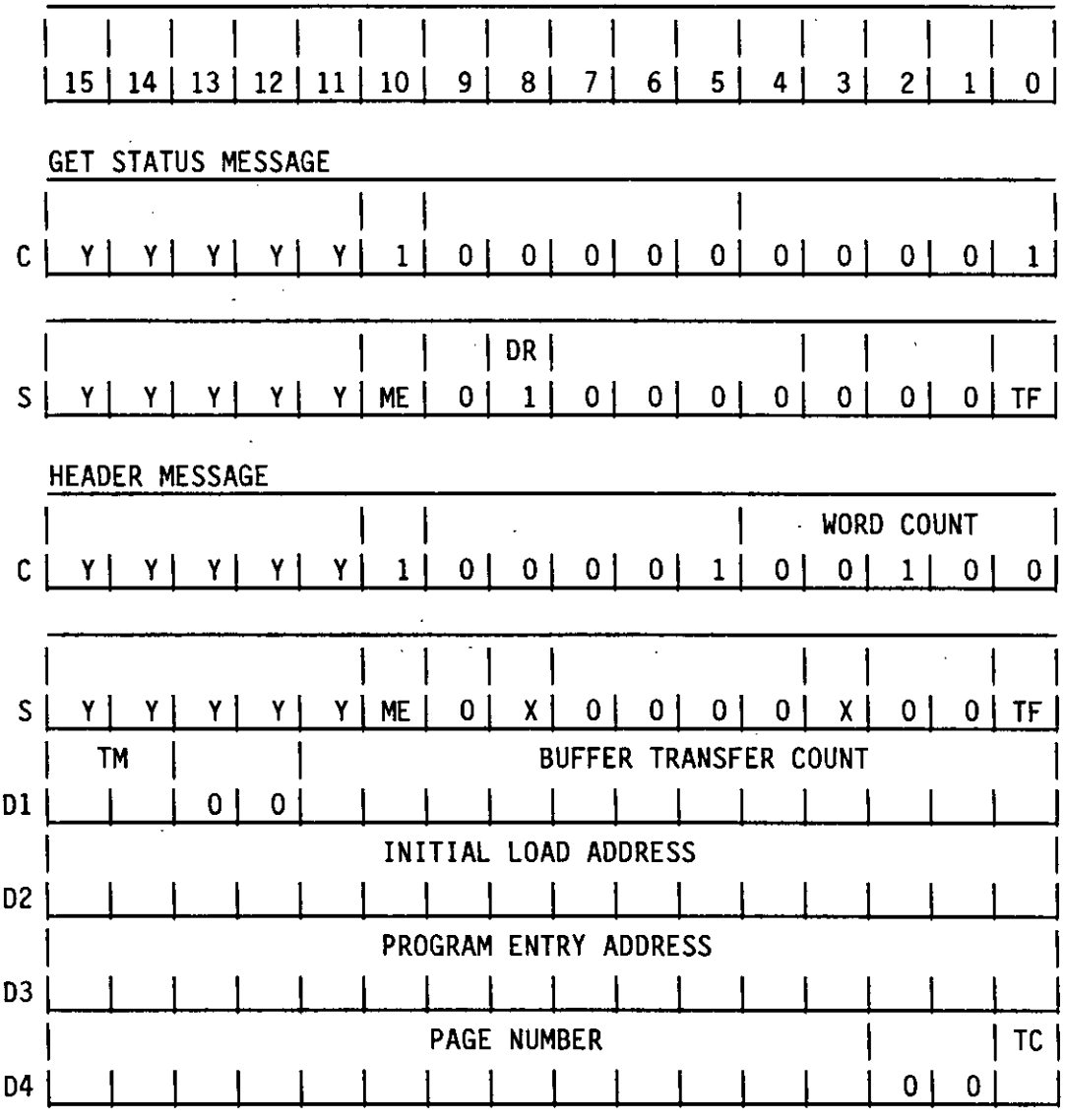
50.4.3 IPL Read Message: MLV = RT: TR = 0: MODE CODE = 11H.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IPL READ MESSAGE																
C	Y	Y	Y	Y	Y	0	0	0	0	0	0	1	0	0	0	1
D	0	0	0	0	0	X	0	0	0	0	0	1	0	1	0	1
S	Y	Y	Y	Y	Y	ME	0	X	0	0	0	0	X	0	0	TF

The AN/AYK-14 bootstrap loader sends the IPL Read Message to the MLV to indicate that the MLV shall prepare a HEADER, MEMORY DATA, ..., MEMORY DATA, TRAILER transaction to be sent to the BC. The COMMAND WORD is the Synchronize with Data mode command (mode code = 11H) and the associated DATA WORD (value = 15H) is the message identifier, indicating that the MLV is to prepare to send data.

50.4.4 Header: MLV = RT: TR = 1: SUBADDRESS = 01H.

50.4.4.1 Header Bus Data.



Once the IPL Read Message has been sent, the first response to a Get Status Message with the DR bit set (= 1) in the STATUS RESPONSE WORD indicates that the MLV is ready for the Header Message to be commanded.

50.4.4.1.1 Header Message Utilization. This message is used to pass Load data to the unit.

50.4.4.2 Data Words.

50.4.4.2.1 Data Word 1.

a. TM (bits 14-15). The Transfer Mode (TM) bits are used to describe the Memory Data Load DATA WORD content. The TM bits are binary coded as follows:

TM = 00 No transfer. In the No Transfer Mode the Buffer Transfer Count and Initial Load Address have no meaning. This mode is used to transfer the Program Entry Address and Page Number or is used as a preamble to the Trailer Message.

= 01 Not used. An AN/AYK-14 IPL fail will occur and processor will hang if this code were used.

= 10 16 bit transfer. Each 16 bits of data transmitted in a DATA WORD will contain 16 bits of information in bits 0-15.

= 11 32 bit transfer. The 16 bits of data transmitted in each odd word (first word is odd) contains the 16 LSB of data in bits 0-15 and each even word contains the 16 MSB of data in bits 0-15.

b. Buffer Transfer Count (bits 0-11). The Buffer Transfer Count is used to indicate the amount of data that will follow the Header Message. The Buffer Transfer Count has no meaning when the Transfer Mode is 00. The range of the Buffer Transfer Count is 1-4096 (value of zero equals 4096). The Buffer Transfer Count is the total number of DATA WORDS that will be transmitted after the Header. The DATA WORDS will be transmitted in 32-word messages with the last message containing the remaining 32 or less words. The maximum transfer is 4096 words using 128 Memory Data Load Messages.

c. Other bits. Bits 12 and 13 shall be zero.

50.4.4.2.2 Data Word 2.

a. Initial Load Address (bits 0-15). The Initial Load Address is the 16 or less LSB of the point in memory into which data is to be loaded. The maximum value (number of bits) used in the Initial Load Address will be compatible with the page size of units using paging. Unused bits shall be set to zero.

50.4.4.2.3 Data Word 3.

a. Program Entry Address (bits 0-15). The Program Entry Address has meaning only for Transfer Mode = 00. The Program Entry Address is the 16 or less LSB of the point in memory at which the unit being reprogrammed is to begin execution. The maximum value (number of bits) used in the Program Entry Address will be compatible with the page size of units using paging. Unused bits shall equal zero.

50.4.4.2.4 Data Word 4.

a. Page Number (bits 3-15). The Page Number represents up to 13 MSBs for page memory address. The Page Number applies to the Program Entry Address for Transfer Mode = 00. The Page Number applies to the Initial Load Address for Transfer Mode 10 and 11. Unused bits shall equal zero.

b. TC bit (bit 0). The Transfer Control bit may be used to transfer control to the program loaded after a Memory Load.

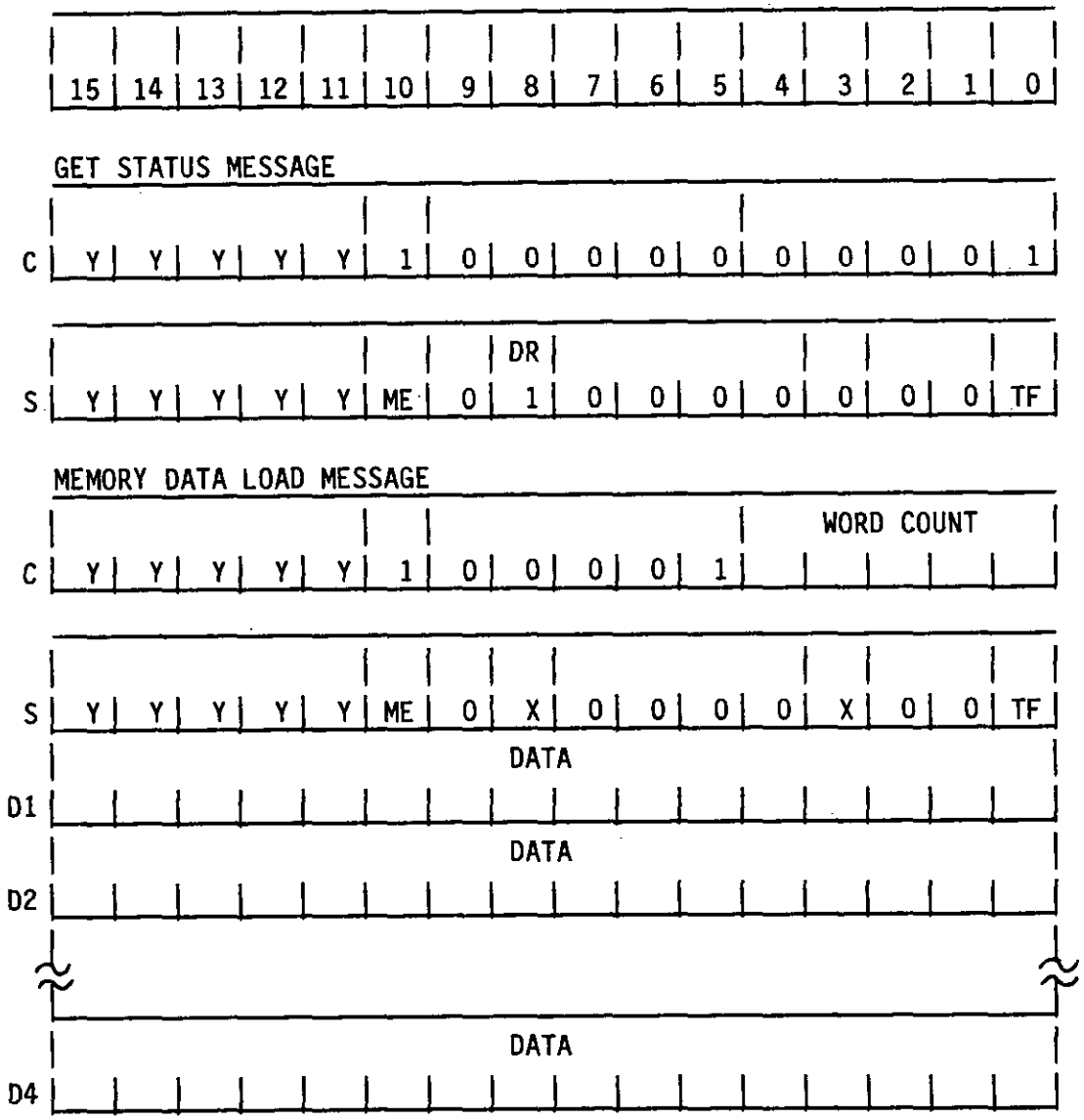
1. TC = 0 Indicates this is the last HEADER, MEMORY DATA, ..., MEMORY DATA, TRAILER or HEADER, TRAILER transaction.

2. TC = 1 Indicates that more data is to follow the current HEADER, MEMORY DATA, ..., MEMORY DATA, TRAILER or HEADER, TRAILER transaction and control should not be transferred. For units using paging and the Program Entry Address, the TC will remain equal to one, even for the last data transaction, until a Transfer Mode = 00 message is used to supply the Program Entry Address and Page Number.

c. Other bits. Bits 1-2 shall be zero.

50.4.5 Memory Data Load: MLV = RT: TR = 1: SUBADDRESS = 01H.

50.4.5.1 Memory Data Load Bus Data.



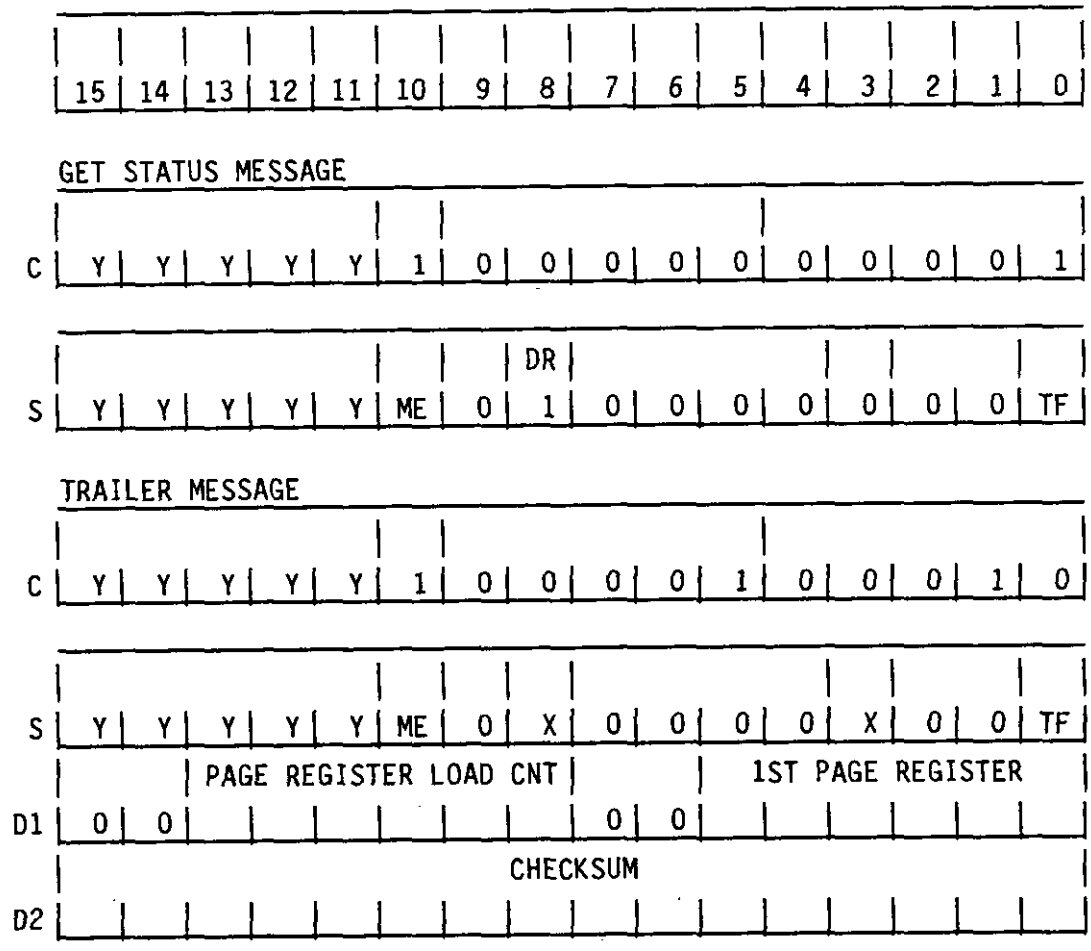
Once the Header Message has been transferred, or Memory Data Load Message transactions have started, the first response to a Get Status Message with the DR bit set (= 1) in the STATUS RESPONSE WORD indicates that the MLV is ready for the next Memory Data Load Message to be commanded. Because of an anomaly in the BC loader, the first MLV response after a Header message with the DR bit set is ignored and the second Get Status Message response with the DR bit set initializes the first Memory Data Load Message.

50.4.5.1.1 Memory Data Load Message Utilization. This message is used to pass the data to be loaded into the unit memory.

50.4.5.2 Data Words. The number of Data Words will equal the WORD COUNT in the Memory Data Load Message COMMAND WORD.

50.4.6 Trailer: MLV = RT: TR = 1: SUBADDRESS = 01H.

50.4.6.1 Trailer Bus Data.



Once all Memory Data Load Messages for a HEADER, MEMORY DATA, ..., MEMORY DATA, TRAILER transaction have been transferred (or after a Header Message with TM = 00), the first response to a Get Status Message with the DR bit set (= 1) in the STATUS RESPONSE WORD indicates that the MLV is ready for the Trailer Message to be commanded.

50.4.6.1.1 Trailer Message Utilization. This message is used to pass the data checksum and additional load parameters to the unit.

50.4.6.2 Data Words.

50.4.6.2.1 Data Word 1.

a. Page Register Load Count (bits 8-13). The Page Register Load Count field specifies the number of consecutive pages needed to load the succeeding data record. The value of this number is written as one less than the actual number of pages (e.g., a count of zero in this field indicates that one page register is to be loaded). However, when the Page Number in the fourth word of the Header indicates Page Number zero, a zero in this field indicates that no (zero) page registers are to be loaded.

b. First Page Register (bits 0-5). This field specifies the number of the first page register which is to be modified with the page number given in the fourth word of the Header. Any attempt to modify page register zero (0) shall result in a load error.

c. Other bits. Bits 6-7 and 14-15 are not used and are set to zero.

50.4.6.2.2 Data Word 2.

a. Checksum (bits 0-15). The checksum will be the checksum of an entire transaction, i.e., HEADER, MEMORY DATA, ..., MEMORY DATA, TRAILER (when TM in Header Data Word 1 is not equal to zero) or HEADER, TRAILER (when TM in Header Data Word 1 is equal to zero). The checksum will be derived by a 2's complement 16 bit addition of every DATA WORD in the transaction (i.e., Header, Memory Data Load, and Trailer DATA WORDS) with the exception of the Checksum DATA WORD (Trailer Data 2). The 2's complement 16-bit addition is binary addition with the carry discarded (i.e., no end around carry) (e.g., FFFF (hex) + 1 = 0).

50.4.6.2.2.1 Comparing the Checksum. The unit being reprogrammed shall be responsible for comparing the checksum received from the MLV with the DATA WORDS. The checksum value in the second DATA WORD of the Trailer is the checksum that should be computed by the unit. If the value computed does not match the value received, the IPL fail indicator is set and the load shall be terminated.

APPENDIX F

MESSAGE FORMATS MLV = BC, SMS/SDC = RT

60. STORES MANAGEMENT SYSTEM/SIGNAL DATA COMPUTER

60.1 Applicability. The protocol of this appendix is applicable to loading and verifying the memory of the AYQ-9 and AYQ-15 Stores Management Systems (SMS) and, on the F/A-18 aircraft, the CP-1726/ASQ-194 Signal Data Computer (SDC). The AYQ-9 SMS has two variants, namely, the original core memory version used on F/A-18A/B aircraft only and the EEPROM version used on several aircraft. The EEPROM AYQ-9 SMS and the AYQ-15 SMS are identical relative to MLV operation; thus, there are only two SMS variants relative to this standard, namely: AYQ-9 Core Memory and AYQ-9 EEPROM or AYQ-15. The protocol of this appendix applies to both SMS variants and to the SDC. Where there are differences between the two SMS variants and/or the SDC the differences are noted in the text. Unless otherwise noted, the text is applicable to all three items. The protocol of this Appendix shall not be used for new designs without written approval of NAVAIRSYSCOM.

60.1.1 Applicability of MLV Requirements. The currently deployed MLV operates with the SMS and SDC utilizing two separate MLV software programs. One program is used for the Core Memory AYQ-9 and supports only the Load function without a Verify at the "0" level. In a special laboratory mode, which is not accessible with the MLV connected to the aircraft, a Save function, as well as several other functions not applicable to this standard, is provided. There is no Verify function for the Core Memory AYQ-9 SMS in the currently deployed MLV software. The second program, which is applicable to the SDC and the EEPROM AYQ-9 or AYQ-15 SMS, supports only the Load function without a Verify at the "0" level. In a special laboratory mode, which is not accessible with the MLV connected to the aircraft, Load/Verify, Verify and Save functions are supported as well as other functions which are not applicable to this standard. Primarily because two programs are utilized, the message traffic sequences for the Core Memory AYQ-9 and the message traffic sequences for the EEPROM AYQ-9, EEPROM AYQ-15, and SDC are not identical.

The operation described in this standard is based on the actual requirements to correctly Load/Verify or Verify: the AYQ-9 Core Memory; the AYQ-9 EEPROM; the AYQ-15 EEPROM; and the SDC memory. The operation described assumes that the Load/Verify and Verify functions will be available at "0" level if not inhibited in the Lookup Table. This standard also assumes that the Save function will be available for all units. The operation discribed in this standard differs from that of the currently deployed MLV software because certain message sequences in the currently deployed software are not required for correct operation (for example the currently deployed software repeats the Boot Load Message in the case of a transaction error). For the purposes of compliance with this standard either the message sequences performed by the currently deployed MLV software or the MLV operation as described herein are considered applicable to meeting the requirements of this standard. The description in this standard is the preferred operation particularly since Load/Verify and Verify are available for all units.

60.2 General Operation.

a. After the MLV assumes the role of Bus Controller (BC), it will set the appropriate discretes to program the SMS or SDC. The Bootstrap Enable interlock is used for the SMS and, for the F-18C/D only, the Boot Enable Radar Data Processor discrete is used for the SDC. The BC then sends the Bootstrap Load Message (see Figure 14) which will enable the RT in the bootstrap mode. For the F/A-18 only, an SDC that contains an invalid Operational Flight Program will require a Consumables Enable Not discrete simultaneous with the Boot Enable Radar Processor discrete prior to the Bootstrap Load Message in order to enter the bootstrap mode. The Consumables Enable Not discrete is provided by aircraft wiring and a momentary contact switch. The MLV does not generate this discrete. The first indication of the successful entry into bootstrap mode is indicated by the receipt of a STATUS RESPONSE WORD with no message error returned for the Bootstrap Load Message. If the Bootstrap Load Message is unsuccessful, the MLV will attempt the Bootstrap Load Message two more times before terminating the load operation.

b. The MLV will then poll the RT with Status Messages until the RT indicates its readiness to accept the Header Message by clearing the Wait bit in its STATUS RESPONSE WORD. When the Wait bit is set in the STATUS RESPONSE WORD for the Status Message, the MLV will continue to send Status Messages to the RT until the retry limit count programmed in the Lookup Table is exceeded. If there is not a good response to the Status Message after the Bootstrap Load Message (no response, Wait bit doesn't clear, or message error), an unsuccessful attempt to enter the bootstrap mode is indicated and the Bootstrap Load Message will be repeated up to three times before an error is declared. After a good Status Message is received, the MLV then sends the four word Header Message. Note: The currently deployed MLV software for the Core Memory SMS does not command a Status Message between the Bootstrap Load Message and the Header message; however, there is no known reason the MLV could not command this message and expect a valid response. After the Header Message, the MLV sends a Status Message checking for a clear Wait bit in the STATUS RESPONSE WORD before sending the first Memory Data Load Message. Note: The currently deployed MLV software for the Core Memory SMS does not command a Status Message between the Header Message and the first Memory Data Load Message; however, there is no known reason why the MLV could not command this messsage and expect a valid response. After each Memory Data Load Message, the MLV will poll the RT with Status Messages before sending the next Memory Data Load Message or the Trailer Message. After all the data in the record has been transferred, and the Trailer Message has been sent, the MLV waits for a Lookup Table programmable period before sending the next Status Message.

c. The Wait bit in the STATUS RESPONSE WORD after the Trailer Message is used to indicate that the RT is still in the process of computing the checksum and is not ready to provide a load successful/

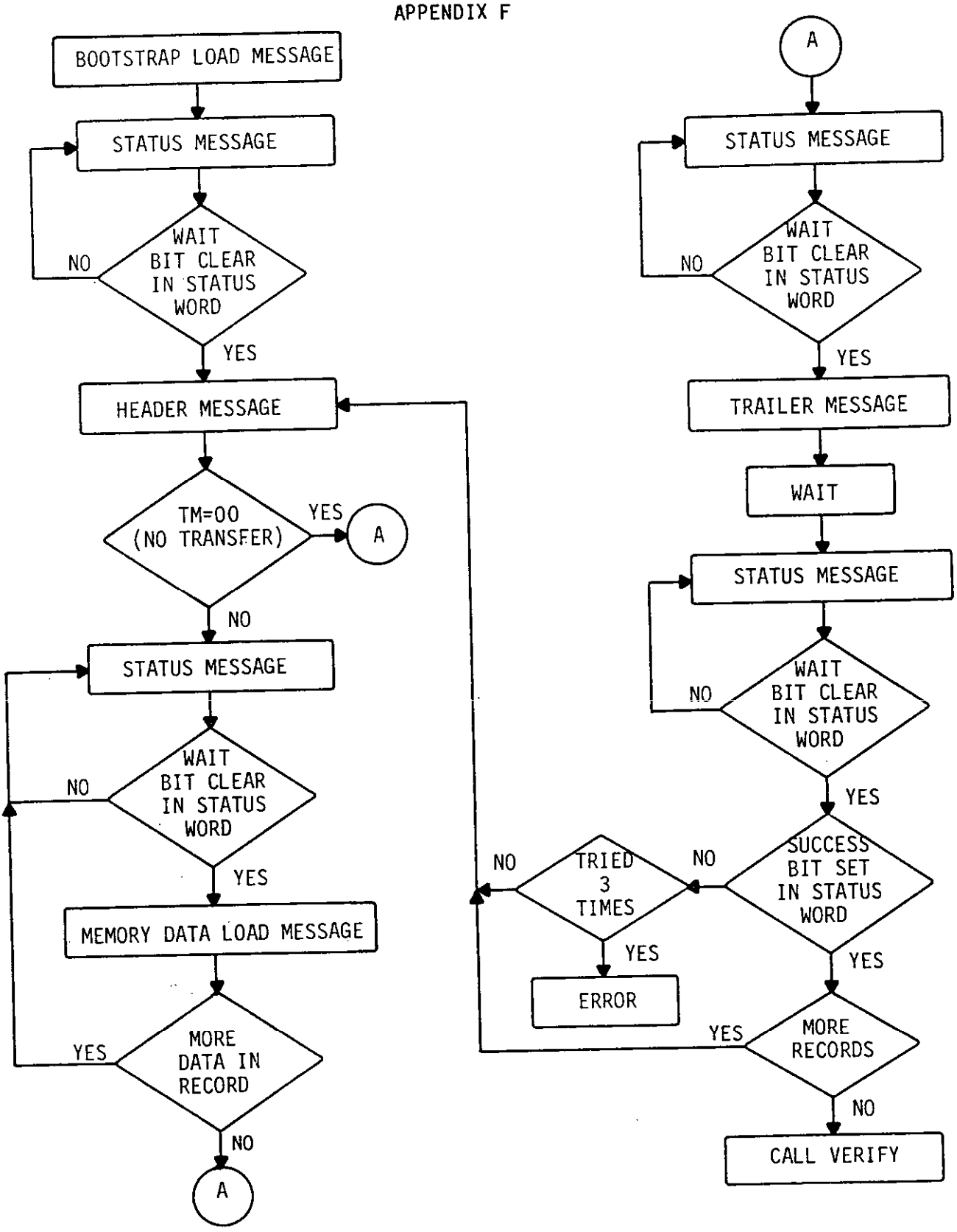


FIGURE 14. F/A-18 SMS/SDC Load Procedure.

unsuccessful indication to the MLV. After the Wait bit is cleared, the Success bit in the STATUS RESPONSE WORD indicates the success of the record loading operation. If the record load was unsuccessful, the MLV will twice attempt to reload the record before terminating the load operation. After a successful record load, if there are more records to be loaded, the MLV will transfer the Header Message and proceed to load the next record.

d. If there are no more records to be loaded, the MLV will command the Start Execution Message if indicated for in the Lookup Table for the current operation (load or load/verify) and, if not inhibited by the Lookup Table, will verify the entire load (see Figure 15). First the MLV sends the Bootstrap Verify Message. If the Bootstrap Verify Message is unsuccessful, as indicated by the returned STATUS RESPONSE WORD, the MLV twice retries the Bootstrap Verify Message before terminating the verify operation.

e. If successful, the MLV will poll the RT with Status Messages until the RT indicates its readiness to accept the Header Message by clearing the Wait bit in the STATUS RESPONSE WORD. If there is not a good response to the Status Message after the Bootstrap Verify Message (no response, Wait bit doesn't clear, or message error), an unsuccessful attempt to enter the bootstrap mode is indicated and the Bootstrap Verify Message will be repeated up to three times before an error is declared. The MLV then sends the four word Header Message. Note: The currently deployed MLV software for the Core Memory SMS (which currently only operates a laboratory Save function and not a Verify) does not command a Status Message between the Bootstrap Verify Message and the Header Message or before each new Header Message; however, there is no known reason why the MLV could not command this message and expect a valid response. After the Header Message, the MLV again polls the RT with Status Messages until the RT indicates the readiness of memory data by clearing the Wait bit. The MLV then commands the first Memory Data Verify Message and the RT reply contains the data read from RT memory. If there is more data in the record, the MLV will poll the RT with Status Messages prior to each subsequent Memory Data Verify Message.

f. If there is no more data in the record, the MLV creates a two word trailer and stores it with the record (no Trailer Message is sent). This record is then verified by the MLV performing a word-for-word comparison with the record on the MLV MSD. If the comparison is good, the MLV after commanding a Status Message transmits the Header Message and the next record in the RT memory is then read and verified. This procedure continues until all records are verified or until a compare error occurs.

g. When all records have been read and verified, the Start Execution Message is sent if the Lookup Table indicates that it is to be sent after a Verify and reprogramming is complete.

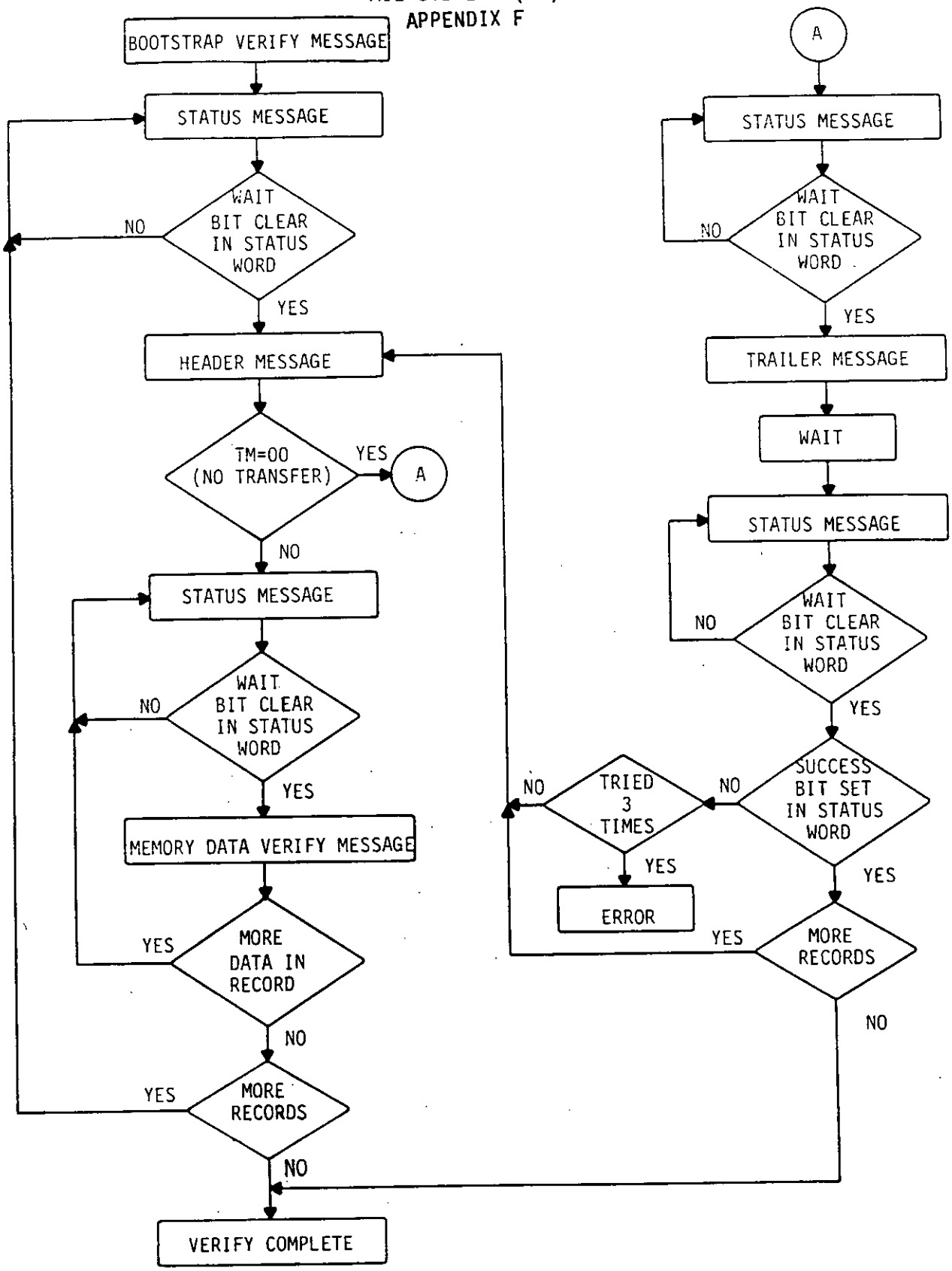
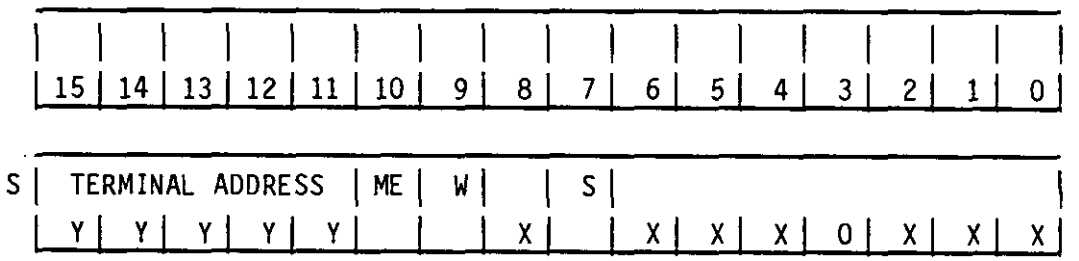


FIGURE 15. F/A-18 SMS/SDC Verify Procedure.

60.3 Status Response Word: MLV = BC.



A STATUS RESPONSE WORD will be provided by the RT for each message transaction. The STATUS RESPONSE WORD will follow the data on an RT receive type transaction and will precede the data on an RT transmit type transaction.

The MLV will allow a response time gap of 12 usec from the end of the last transmitted COMMAND WORD (transmit type message) or the end of the last transmitted DATA WORD (receive type message), to the start of the RT STATUS RESPONSE WORD before declaring a no response error (equivalent of 14 usec when measured in accordance with MIL-STD-1553B). Under normal conditions the RT shall begin the STATUS RESPONSE WORD within the period of 2-10 usec from the receipt of the end of the last COMMAND WORD (transmit type message) or the receipt of the end of the last DATA WORD (receive type message) (Equivalent of 4-12 usec when measured in accordance with MIL-STD-1553B). The MLV will ensure that the time from the end of the RT transmission of the last DATA WORD (transmit type message) or the end of the last STATUS RESPONSE WORD (receive type message or Mode Code) to the beginning of the next COMMAND WORD is at least 8 usec (Equivalent of 10 usec when measured in accordance with MIL-STD-1553B). The fields within this word are as follows:

a. TERMINAL ADDRESS (bits 11-15). The RT address will be the normal RT address of the unit being reprogrammed. This address will be determined by the MLV from the Aircraft Type and Aircraft Configuration Modification information provided to the MLV and based on the particular bus selected by the MLV switching network. The RT address for the SMS is 6. The RT address for the SDC is 1E hex. Throughout the remainder of this appendix the RT address of the unit being reprogrammed will be referred to as YYYYY.

b. ME bit (bit 10). The Message Error (ME) bit may be set high (= 1) for either a Manchester encoding error or a parity error detected in one or more data words of a message. If set, the RT shall clear the ME bit as soon as it has completed transmission of status or has suppressed status because of message anomalies. Upon receipt of a STATUS RESPONSE WORD with the ME bit set, or no status, the MLV will retry the most recent record two more times. If the message error bit is set in the STATUS RESPONSE WORD for the Bootstrap Load Message, the Bootstrap Verify Message, or the Status Message that follows these messages, the Bootstrap Load Message or Bootstrap Verify Message will be retried two more times. If unsuccessful at this point, the load operation will be terminated.

c. W bit (bit 9). The Wait (W) bit will be set high (= 1) to indicate that the RT is not ready to send or receive messages or that an error has occurred. The MLV will only examine this bit in STATUS RESPONSE WORDS associated with Status Messages.

d. S bit (bit 7). The Success (S) bit shall be set high (= 1) to indicate a successful record load. An unsuccessful load operation is indicated by the Success bit set for low (= 0). The MLV will only examine this bit in STATUS RESPONSE WORDS associated with the Status Message(s) after the Trailer Message.

e. Bit 3 although not utilized in the protocol must be set to 0 in order to allow the MLV to receive the Data Words transmitted by the RT.

f. Other bits. Bits 0-2, 4-6, 8 will not be used by the MLV; thus, the bit may be 1 or 0. For the SDC, bit 0 will always be 0.

60.4 Messages.

60.4.1 Status Message: MLV = BC: TR = 1: MODE CODE = 02.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C	Y	Y	Y	Y	Y	1	0	0	0	0	0	0	0	0	1	0
S	Y	Y	Y	Y	Y	ME		W	X		S	X	X	X	X	X	X	X

Status Messages shall be sent after each message. The status is indicated by the status of the Wait (W) and Success (S) bits in the STATUS RESPONSE WORD. The purpose of the Status Message is to determine if the RT properly received the last message and is ready to proceed with the next message. The MLV shall wait a fixed period of time (indicated in the Lookup Table) after commanding a Trailer Message before commanding the Status Message. For the SMS, this value is nominally 1 msec. For the SDC, this value is nominally 3 msec.

60.4.1.1 Status Response Word. The STATUS RESPONSE WORD to this message shall be as defined previously in this appendix; bits 7 and 9 are used as follows:

a. W bit (bit 9). The Wait (W) bit will be set to indicate that the RT is not ready to send or receive messages. This condition may occur because of an error or because the RT is busy. The Wait bit set in response to all Status Messages sent during a one second (three seconds for the SDC) period will indicate that an error has occurred (vice RT busy) and the MLV shall retry the entire transaction in progress (HEADER, MEMORY DATA, ..., MEMORY DATA, TRAILER or HEADER, TRAILER sequence). If the error occurs in the Status Message for the Bootstrap Load Message or the Bootstrap Verify Message, then the Bootstrap message shall be retried. If unsuccessful after two consecutive transaction retries, the MLV shall abort the processing of the RT and declare an error.

b. S bit (bit 7). The Success (S) bit shall be set (= 1) to indicate a successful record load. The MLV shall only examine the Success bit for a value = 1 in Status Messages that follow a Trailer message. An unsuccessful load shall result in two retries of the most recent record load after which the MLV will terminate the load operation. An unsuccessful load operation (S = 0) is defined as follows:

1. a checksum error

2. a difference between the number of data words transmitted and the number specified in the record header

3. RT did not enter Load or Verify mode.

This bit will normally be set only in the STATUS RESPONSE WORD associated with the Status Messages sent after the Trailer Message for a load operation and only when the checksum calculation was correct for the previous HEADER, MEMORY DATA, ..., MEMORY DATA, TRAILER or HEADER, TRAILER transaction.

e. Other bits. Bits 0-6, 8 shall be zero.

60.4.2 Bootstrap Load Messsage: MLV = BC: TR = 1: MODE CODE = 11H.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C	Y	Y	Y	Y	Y	1	0	0	0	0	0	1	0	0	0	1
S	Y	Y	Y	Y	Y	ME	0	X	X	X	X	X	X	X	X	X

The Bootstrap Load Message is sent by the MLV after closing the Bootstrap Enable interlock. Successful receipt of the Bootstrap Load Message by the RT is indicated by the presence of the STATUS RESPONSE WORD for the Bootstrap Load Message. Successful receipt is confirmed by receipt of the STATUS RESPONSE WORD for the Status Message that follows the Bootstrap Load Message and precedes the Header Message. The MLV will attempt up to three successive Bootstrap Load Messages looking for acknowledgement before terminating the load. For all cases except the EEPROM version of the AYQ-9 or AYQ-15, upon receipt the RT shall halt all Operational Flight Program (OFP) processing and enter the Bootstrap Load Mode. The EEPROM version of the AYQ-9 or AYQ-15 will execute the bootstrap function within a valid Operational Flight Program when loading the bootstrap EEPROM memory. The Bootstrap Load Message may be sent without the MLV previously checking the RT status via a Status Message.

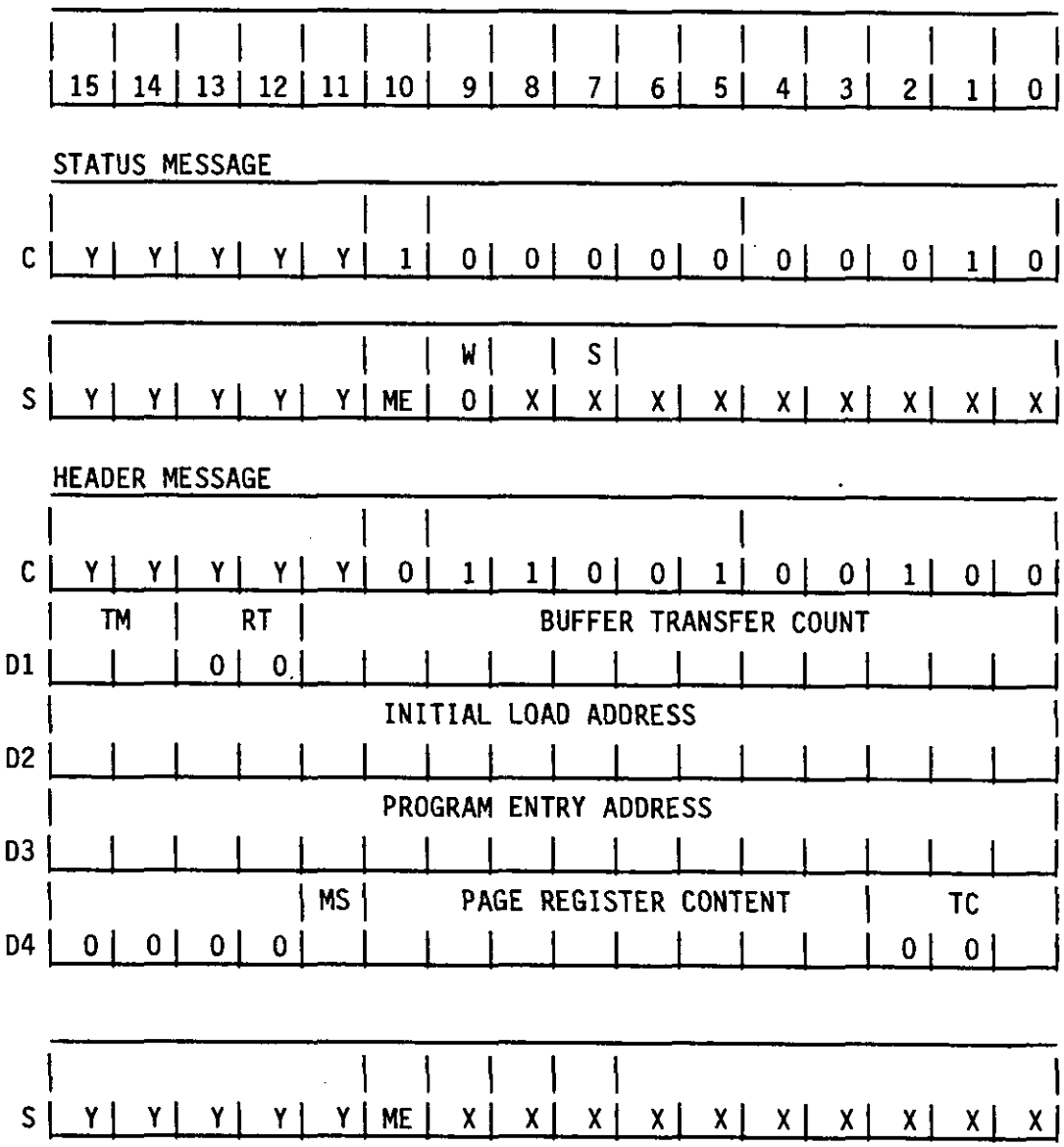
60.4.3 Bootstrap Verify Message: MLV = BC: TR = 1: MODE CODE = 12H.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C	Y	Y	Y	Y	Y	1	0	0	0	0	0	1	0	0	1	0
S	Y	Y	Y	Y	Y	ME	W 0	X	S X	X	X	X	X	X	X	X

With the Bootstrap Enable interlock closed the RT shall enter the Bootstrap Verify mode upon receipt of the Bootstrap Verify Message. Successful receipt of the Bootstrap Verify Message by the RT is indicated by the presense of the STATUS RESPONSE WORD for the Bootstrap Verify Message. Successful receipt is confirmed by receipt of the STATUS RESPONSE WORD for the Status Message that follows the Bootstrap Verify Message and precedes the Header Message. The MLV will attempt up to three successive Bootstrap Verify Messages looking for acknowledgement before terminating the Verify operation (Bootstrap Read mode). The Bootstrap Verify Message may be sent without the MLV previously checking the RT status via a Status Message.

60.4.4 Header: MLV = BC: TR = 0: SUBADDRESS = 19H.

60.4.4.1 Header Bus Data.



The first response to a Status Message with the W bit clear (bit 9 = 0) in the STATUS RESPONSE WORD indicates that the RT is ready to receive the Header Message. The state of the Success bit is normally a don't care to the MLV.

The only time the MLV will check the Success bit in the Status Message before the Header Message is in the case of multiple transactions during a load where the Status Message occurs between a Trailer Message and the next Header Message. If a transaction is retried because of an error, the MLV will send the Header Message without first sending another Status Message.

60.4.4.1.1 Header Message Utilization. This message is used to pass Load/Verify data to the unit.

60.4.4.2 Data Words.

60.4.4.2.1 Data Word 1.

a. TM (bits 14-15). The Transfer Mode (TM) bits are used to describe the Memory Data Load DATA WORD content. The TM bits are binary coded as follows:

1. TM = 00 No transfer. In the No Transfer Mode the Buffer Transfer Count and Initial Load Address have no meaning. This mode is used to transfer the Program Entry Address and Page Number or is used as a preamble to the Trailer Message.

2. TM = 01 8 bit transfer. Each 16 bits of data transferred in a DATA WORD will contain only 8 bits of information in bits 0-7. Not used with the SMS or the SDC.

3. TM = 10 16 bit transfer. Each 16 bits of data transmitted in a DATA WORD will contain 16 bits of information in bits 0-15.

4. TM = 11 32 bit transfer. The 16 bits of data transmitted in each odd word (first word is odd) contains the 16 LSB of data in bits 0-15 and each even word contains the 16 MSB of data in bits 0-15. Not used with the SMS or the SDC.

b. RT (bits 12-13). The Record Type (RT) bits are defined to describe the meaning of the Header Message. The only value transmitted by the MLV shall be 00. Record Types other than 00 are defined only for other than MLV use and are not addressed in this standard.

c. Buffer Transfer Count (bits 0-11). The Buffer Transfer Count is used to indicate the amount of data that will follow the Header Message. The Buffer Transfer Count has no meaning when the Transfer Mode is 00. The Buffer Transfer Count is the total number of DATA WORDS that will be transmitted after the Header Message. The DATA WORDS will be transmitted in 32-word messages with the last message containing the remaining 32 or less words. For the SDC, the range of the Buffer Transfer Count is 1-1024 (value of zero equals 1024 and bits 10 and 11 are always zero). The maximum transfer for the SDC is done with 32 messages of 32 words each. For the AYQ-9 or

AYQ-15 SMS, a Buffer Transfer Count of zero is invalid unless TM = 00. For the EEPROM version of the AYQ-9 or AYQ-15, the range of the Buffer Transfer Count is 1-1024, with the maximum transfer using 32 messages of 32 words each. For the core memory version of AYQ-9, the range of the Buffer Transfer Count is 1-4095 with the maximum transfer using 127 messages of 32 words each and one 31 word message.

60.4.4.2.2 Data Word 2.

a. Initial Load Address (bits 0-15). The Initial Load Address is the 16 or less LSB of the point in memory into which data is to be loaded. (When required, MSB information is provided in the Page Register Content field of DATA WORD 4.) The maximum value (number of bits) used in the Initial Load Address will be compatible with the page size of units using paging. Unused bits shall be set to zero. The Initial Load Address has no meaning for TM = 00. For the SDC, the physical memory that the Initial Load Address applies to shall be as indicated by the MS bit in DATA WORD 4.

60.4.4.2.3 Data Word 3.

a. Program Entry Address (bits 0-15). The Program Entry Address has meaning only for Transfer Mode = 00. The Program Entry Address is the 16 or less LSB of the point in memory at which the unit being reprogrammed is to begin execution. (When required, MSB information is provided in the Page Register Content field of DATA WORD 4.) The maximum value (number of bits) used in the Program Entry Address will be compatible with the page size of units using paging. Unused bits shall equal zero.

60.4.4.2.4 Data Word 4.

a. MS (bit 11). For the AYQ-9 or AYQ-15 SMS, the MS bit will always be zero. For the SDC, the Memory Select (MS) bit indicates that the SDC Input Output Memory (MS = 1) or the SDC Main Memory (MS = 0) is the selected memory area. When Input Output Memory is selected, the Initial Load Address in DATA WORD 2 shall be an absolute address in Input Output Memory.

b. Page Register Content (bits 3-10). The Page Register Content represents up to 8 MSBs for page memory addressing. The Page Register Content applies to the Program Entry Address for Transfer Mode = 00. The Page Register Content applies to the Initial Load Address for Transfer Mode 10. For the SDC, the Page Register Content has no meaning when Input Output Memory is selected by MS = 1. The AYQ-9 or AYQ-15 SMS only uses bits 3 to 6 to indicate 4 MSBs for memory addressing. The Page Register Content may also be used to provide the data to be loaded into the register(s) pointed to by the Initial Page Register in DATA WORD 1 of the Trailer Message. Unused bits shall equal zero.

c. TC bits (bits 0-2). The Transfer Control bits indicate whether more data is to follow. Bits 1 and 2 will always be zero.

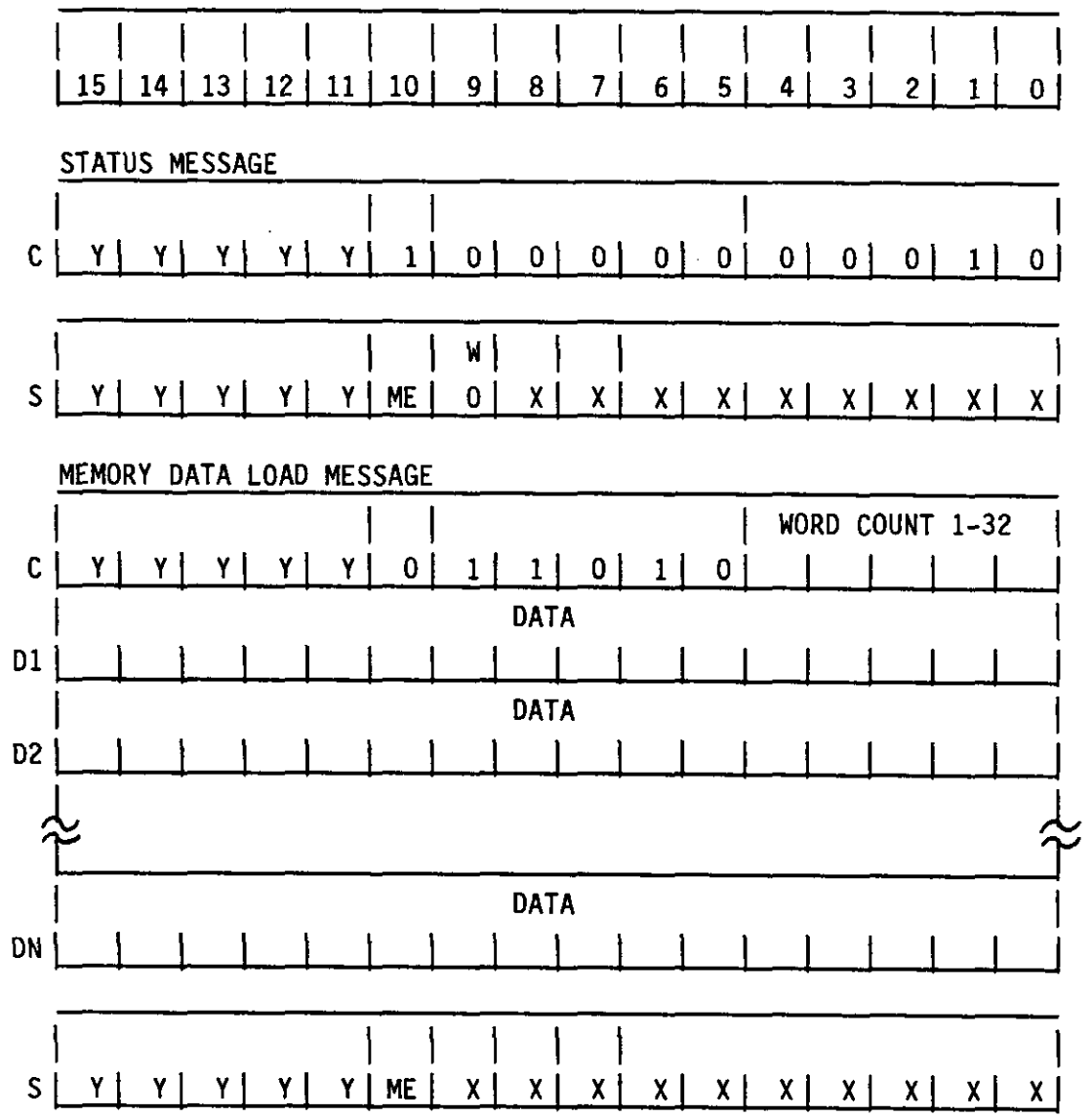
1. TC = 000 Indicates this is the last HEADER, MEMORY DATA, ..., MEMORY DATA, TRAILER or HEADER, TRAILER transaction and control may be transferred if the Load/Verify is complete.

2. TC = 001 Indicates that more data is to follow the current HEADER, MEMORY DATA, ..., MEMORY DATA, TRAILER or HEADER, TRAILER transaction and control should not be transferred. For units using paging and the Program Entry Address, the TC will remain equal to one, even for the last data transaction, until a Transfer Mode = 00 message is used to supply the Program Entry Address and Page Number.

d. Other bits. Bits 12-15 shall be zero.

60.4.5 Memory Data Load: MLV = BC: TR = 0: SUBADDRESS = 1AH.

60.4.5.1 Memory Data Load Bus Data.



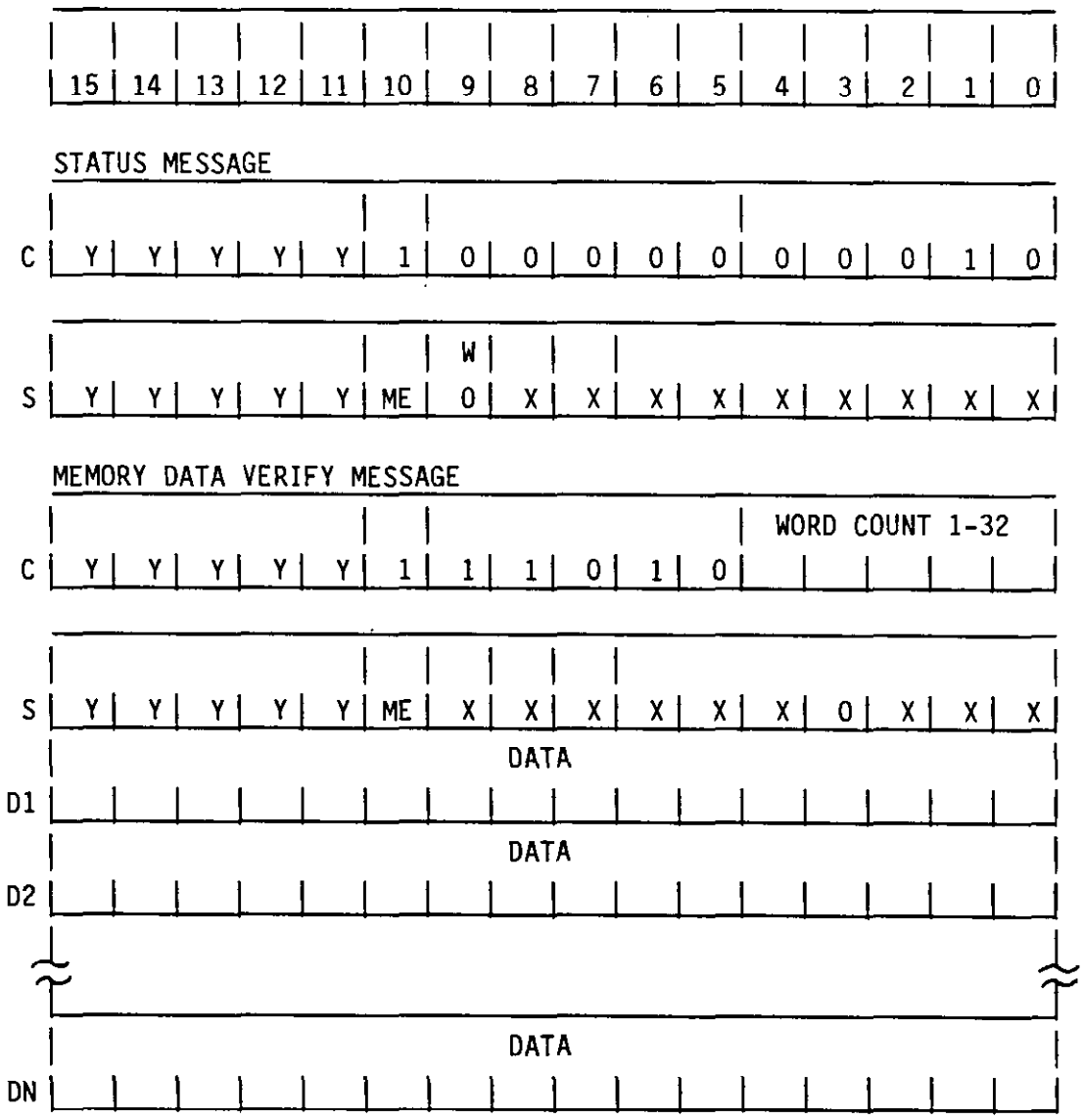
The Wait bit = 0 in the STATUS RESPONSE WORD of the Status Message indicates that the RT is ready to receive the next Memory Data Load message. Since the Header Message is followed by a Status Message and each Memory Data Load Message will be followed by a Status Message, the Status Message will be present before all Memory Data Load Messages in a sequence.

60.4.5.1.1 Memory Data Load Message Utilization. This message will be used to pass the data to be loaded into the unit memory.

60.4.5.2 Data Words. The number of Data Words will equal the WORD COUNT in the Memory Data Load Message COMMAND WORD. Data to be loaded into the RT memory will be transmitted in groups of 32 words except for the last transmission which may contain fewer words.

60.4.6 Memory Data Verify: MLV = BC: TR = 1: SUBADDRESS = 1AH.

60.4.6.1 Memory Data Verify Bus Data.



The Wait bit = 0 in the STATUS RESPONSE WORD of the Status Message indicates that the RT is ready to accept the next Memory Data Verify command. Since the Header Message is followed by a Status Message and a Status Message will also follow each Memory Data Verify transfer, the Status Message will be present before all Memory Data Verify Messages in a sequence. An unsuccessful transmission will result in the MLV retransmitting the most recent Header. After three unsuccessful attempts the read operation will be terminated. At the end of all Memory Data Verify messages required for a record no Trailer

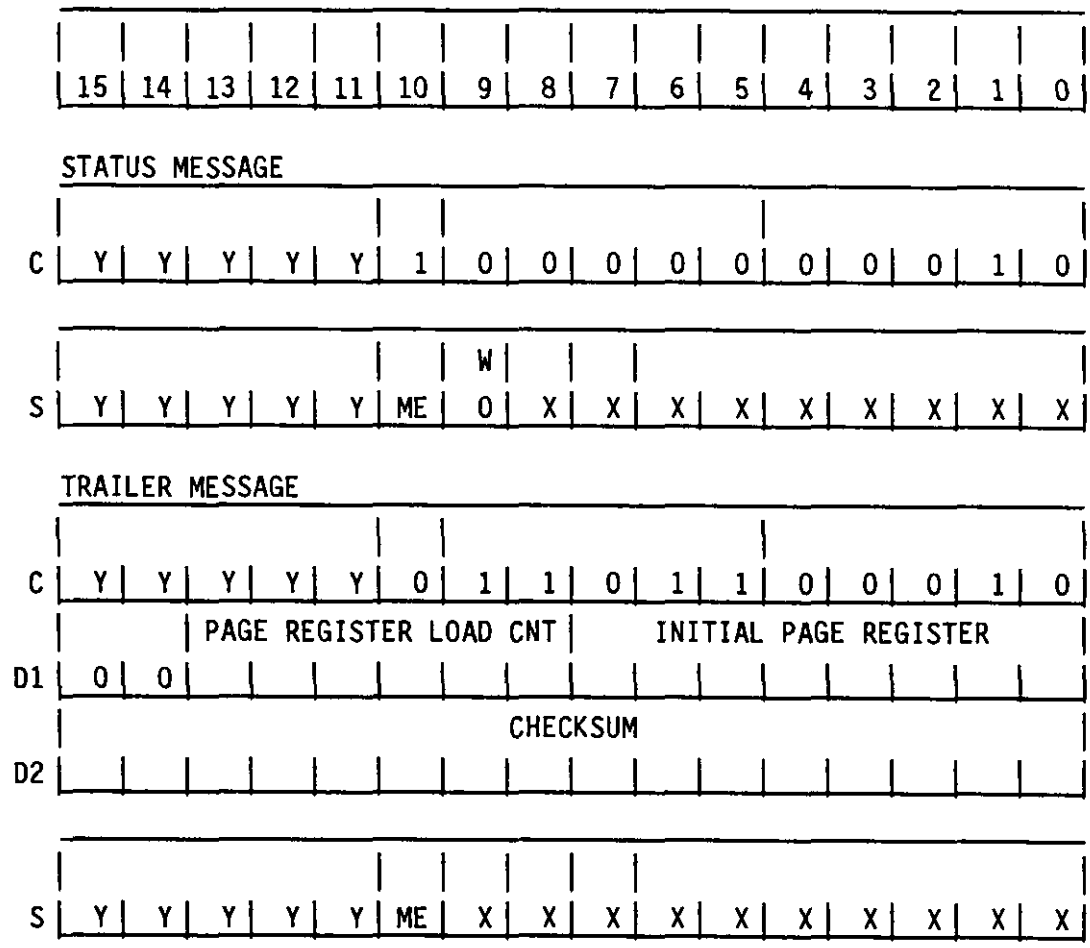
Message will be sent. The checksum will be checked by the MLV. For the verify function the transaction will be HEADER, MEMORY DATA, ..., MEMORY DATA followed by the next HEADER, MEMORY DATA, ..., MEMORY DATA transaction.

60.4.6.1.1 Memory Data Verify Message Utilization. This message will be used to pass the data that the MLV will compare to the data on the MSD.

60.4.6.2 Data Words. The number of Data Words will equal the WORD COUNT in the Memory Data Verify Message COMMAND WORD.

60.4.7 Trailer: MLV = BC: TR = 0: SUBADDRESS = 1BH.

60.4.7.1 Trailer Bus Data.



Once all Memory Data Load Messages have been transferred, the first response to a Status Message with the W bit clear (= 0) in the STATUS RESPONSE WORD indicates that the RT is ready to receive the Trailer Message. The Trailer Message will not be used during a verify operation unless a TM mode 00 (i.e., a HEADER, TRAILER transaction) is required for paging information during the verify operation. After each Trailer Message the MLV, after waiting a time period specified in the Lookup Table, will always follow the Trailer Message with a Status Message looking for the Success bit (bit 7) to be set in the STATUS RESPONSE WORD for the Status Message.

60.4.7.1.1 Trailer Message Utilization. This message is utilized to pass the data checksum and additional Load/Verify parameters to the unit.

60.4.7.2 Data Words.

60.4.7.2.1 Data Word 1.

a. Page Register Load Count (bits 8-13). The Page Register Load Count field specifies the number of consecutive page registers, if any, that are to be loaded after processing of the current transaction is completed. The SMS does not utilize these bits and the bits should be set to zero in this application. For the SDC, the range of the load count is 0 to 63 and the number of registers specified will be loaded starting from the Initial Page Register location specified. Since there are only 256 page registers that can be loaded by the SDC boot loader, the Initial Page Register specified plus the load count should not exceed 255. When the Memory Select = 1 in the fourth DATA WORD of the Header Message, the Page Register Load Count should be zero.

b. Initial Page Register (bits 0-7). The SMS does not utilize these bits and the bits should be set to zero in this application. For the SDC, this field specifies the number of the first page register which is to be modified with the Page Register Content given in the fourth word of the Header. The SDC subdivides this field into a Page Register Group Subfield (bits 4-7) and a Page Register Select Subfield (bits 0-3). For bootloading, the normal value of both subfields is 4; thus, the normal value of the Initial Page Register is 44 hex. For bootload purposes, the Page Register Select Subfield (bits 0-3) may not be set to values 0 through 3.

c. Other bits. Bits 14-15 are not used and are set to zero.

60.4.7.2.2 Data Word 2.

a. Checksum (bits 0-15). The checksum will be the checksum of an entire transaction, i.e., HEADER, MEMORY DATA, ..., MEMORY DATA, TRAILER (when TM in Header Data Word 1 is not equal to zero) or HEADER, TRAILER (when TM in Header Data Word 1 is equal to zero). The checksum will be derived by a 2's complement 16 bit addition of every Data Word in the transaction (i.e., Header, Memory Data Load, Trailer DATA WORDS) with the exception of the Checksum DATA WORD (Trailer Data 2). The 2's complement 16 bit addition is binary addition with the carry discarded (i.e., no end around carry) (e.g., FFFF hex + 1 = 0).

60.4.7.2.2.1 Comparing The Checksum. The unit being reprogrammed shall be responsible for comparing the checksum received from the MLV with the DATA WORDS. The checksum value in the second word of the Trailer is the checksum that should be computed by the unit. If the value computed does not match the value received, the unit should not set the success bit in the Status Message that follows, thus causing the MLV to retry the transaction.

60.4.7.2.3 Start Execution Message: MLV = BC: TR = 1: MODE CODE = 13H.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C	Y	Y	Y	Y	Y	1	0	0	0	0	0	1	0	0	1	1
S	Y	Y	Y	Y	Y	ME	X	X	X	X	X	X	X	X	X	X

Depending on Lookup Table information for the following three cases: the end of a Load operation that is part of a Load/Verify; or at the end of a Load for which the verify was inhibited; or at the end of a Verify, the MLV will command or inhibit the command of a Start Execution Message. The Start Execution Message will be generated by the MLV (will not be recorded on the MSD). When the MLV transfers the Start Execution Message, the RT begins program execution at the Program Entry Address which was previously specified in the third word of the Header of a HEADER, TRAILER transaction (Program Entry Address can only be loaded by a TM = 00 transfer). For the SMS, if a Start Execution Message is sent without previously specifying the Program Entry Address, execution will begin at the power up autostart location. The successful receipt of the Start Execution Message is indicated by the presence of the STATUS RESPONSE WORD with no message error indicated.

APPENDIX G

MESSAGE FORMATS MLV = RT, AN/AYK-14 SIM-A = BC

70. AN/AYK-14 WITH A SERIAL INTERFACE MODULE TYPE A

70.1 Applicability. The protocol of this appendix is applicable to the AN/AYK-14 with a Serial Interface Module (SIM) Type A. This protocol is also applicable for AYK-14's equipped with a SIM Type B or a Discrete Serial Module (DSM) emulating the SIM Type A. The protocol of this appendix shall not be used for new designs without written approval of NAVAIRSYSCOM. Additional protocol information can be found in the Naval Avionics Center (NAC) documents listed in Section 2.

70.2 General Operation.

a. Once the AN/AYK-14 recognizes the IPL from the MLV (see Section 5.2.2.2.3), the AN/AYK-14 acting as BC responds by sending the Initialize Device Message to initialize the remote terminal (the MLV) at address 31 (see Figure 16). The BC then polls the MLV with Status Messages until the Busy bit is cleared in the STATUS RESPONSE WORD. At this point the BC sends the Initialize I/O Transfer Message to initialize the data transfer sequence.

b. The BC again polls the MLV with Status Messages until the Data Ready bit is set in the STATUS RESPONSE WORD. The BC then sends a command requesting the four words of the Header Message. The information contained in the Header Message will be used to set up various parameters needed to perform the loading of the data. Prior to the transfer of each Memory Data Load Message, the BC polls the MLV with Status Messages until the Data Ready bit is set. Prior to the transfer of the first Memory Data Load Message, because of an anomaly in the BC loader which fails to recognize the Data Ready bit in the STATUS RESPONSE WORD of a Status Message after the Header Message, a second Status Message will be sent. The data is sent to the BC in 32 word Memory Data Load Messages with any residual data sent in the last message. At the end of the data messages the BC polls the MLV with Status Messages until the Data Ready bit is set. The BC then commands the Trailer Message.

c. The BC computes a checksum of all DATA WORDS transferred (Header Message, Data Messages, and the first word of the Trailer Message). This checksum is compared to the one sent by the MLV in the second word of the Trailer Message. If there is an error, the IPL fail indicator is set and the AN/AYK-14 will hang. Upon a successful checksum, the Transfer Control bit in the fourth word of the Header is examined to determine if another record is to be loaded. If so, the processing starts over with the Initialize I/O Transfer Message.

d. The AN/AYK-14 bootloader uses subaddress 01 in the COMMAND WORD for the Header Message, Memory Data Load Message, and Trailer Message and assumes that these messages will be sent in the correct order by the MLV.

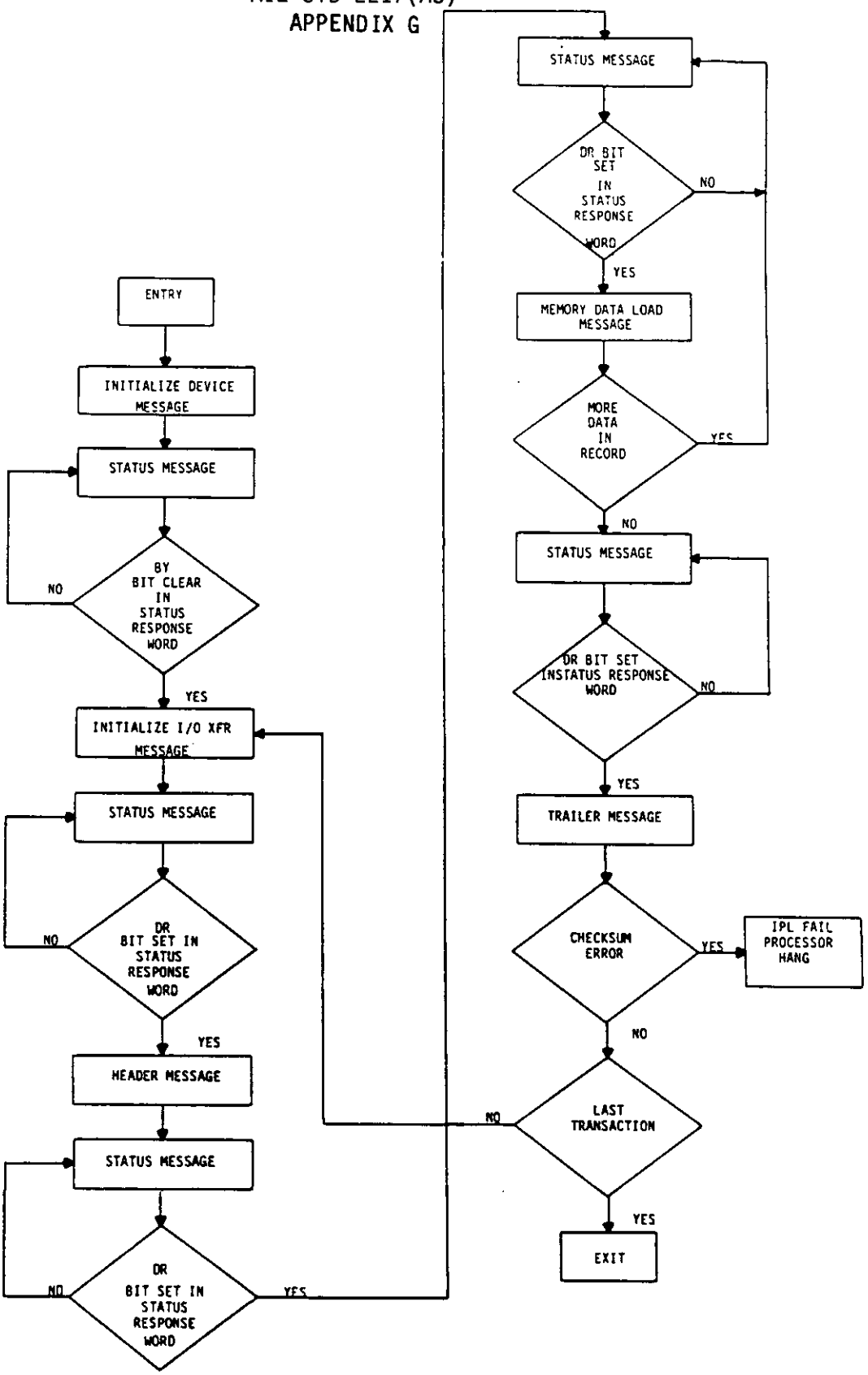
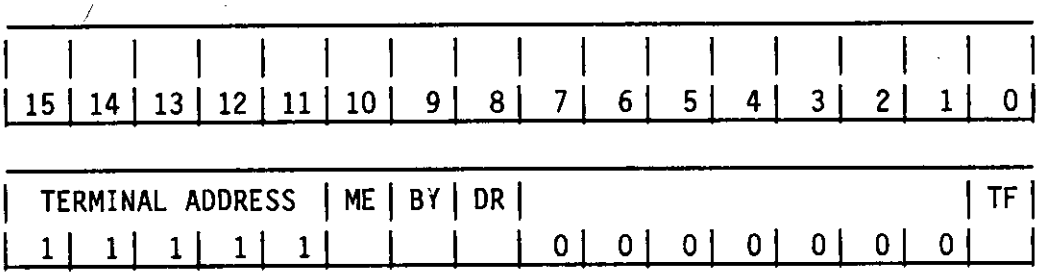


FIGURE 16. AN/AYK-14 SIM-A Load Procedure.

70.3 Status Response Word: MLV = RT.



The STATUS RESPONSE WORD will be provided by the MLV acting as the RT for each message transaction. This word will precede the data transferred to the BC in the Header Message, Memory Data Load Message, and Trailer Message. The BC will allow a response time gap of at least 6.5 usec from the end of the last transmitted COMMAND WORD to the start of the MLV STATUS RESPONSE WORD before declaring a no response error (equivalent of 8.5 usec when measured in accordance with MIL-STD-1553B). Under normal conditions the MLV shall begin the STATUS RESPONSE WORD within the period of 2-5 usec from the receipt of the end of the last COMMAND WORD (equivalent of 4-7 usec when measured in accordance with MIL-STD-1553B). The BC will ensure that the time from the end of the MLV transmission of the last STATUS RESPONSE WORD (receive type message or Mode Code) or the end of the last DATA WORD (transmit type message) to the beginning of the next COMMAND WORD is at least 2 usec (equivalent of 4 usec when measured in accordance with MIL-STD-1553B). The fields within this word are as follows:

a. TERMINAL ADDRESS (bits 11-15). When the protocol of this appendix is used, the MLV RT address shall be 31.

b. ME bit (bit 10). The Message Error (ME) bit may be set high (= 1) when an undefined mode code is received. The ME bit, if set, will be set once for a message error and then cleared for the next message if there was no subsequent error.

c. BY bit (bit 9). The MLV will set the Busy (BY) bit high (= 1) until it is ready to receive the Initialize I/O Transfer Message, at which point the bit is lowered in the STATUS RESPONSE WORD. The BC only utilizes this bit to determine when to send the first Initialize I/O Transfer Message. In all other instances the bit is a "don't care" state and is not read by the BC. Although referred to as the Busy bit, the bit position used in this protocol is different than that of MIL-STD-1553B.

d. DR bit (bit 8). The Data Ready (DR) bit is set high (= 1) in the STATUS RESPONSE WORD to indicate that the appropriate data is ready for transfer via a subaddress 01 command. If the bit is low, and the BC is expecting data, the BC will continue to send Status Messages until the bit goes high.

e. TF bit (bit 0). The Terminal Flag (TF) bit will be set high (= 1) to indicate that the RT is not functioning properly.

f. Other bits. Bits 1-7 will be zero in the STATUS RESPONSE WORD.

70.4 Messages.

70.4.1 Status Message: MLV = RT: TR = 1: MODE CODE = 02H.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	0
S	1	1	1	1	1	ME	BY	DR	0	0	0	0	0	0	0	TF

The Status Message is used by the BC to determine when to send the first Initialize I/O Transfer Message, and to determine when to send the Header Message, Memory Data Load Message(s), and the Trailer Message. The RT indicates its readiness for the first Initialize I/O Transfer Message by lowering the Busy bit (= 0) in the STATUS RESPONSE WORD. The BC will continue to command Status Messages until the Busy bit is set low. If the Busy bit is not lowered, the BC will wait approximately 3.5 minutes on channel one until a timeout has occurred and will then switch to the redundant bus, to retry establishing communications before declaring an error. If a second timeout occurs, an IPL fail will result. For the Header Message, Memory Data Load Message(s), and Trailer Message, the MLV will indicate the availability of data by setting the Data Ready (DR) bit (= 1) in the STATUS RESPONSE WORD. If the DR bit is not set, the BC will continue to send Status Message commands for two seconds until the MLV indicates, via the DR bit, that data is ready. After two seconds the BC will switch to the redundant bus, if possible, and send Status Message commands for an additional two seconds before declaring an error. When passing Memory Data Load Messages, the BC will command the Status Message(s) prior to the transfer of each 32 word data group.

70.4.1.1 Status Response Word. The STATUS RESPONSE WORD to the Status Message shall be as defined previously in this appendix; bits 8 and 9 are used as follows:

a. BY bit (bit 9). The MLV will set the Busy (BY) bit high until it is ready to receive the first Initialize I/O Transfer Message, at which point the bit is lowered in the STATUS RESPONSE WORD. In all other instances the bit is in a "don't care" state and is not read by the BC.

b. DR bit (bit 8). The Data Ready bit is set high in the Status Response word to indicate that the appropriate data is ready for transfer. If the bit is low, and the BC is expecting data, the BC will continue to send Status Messages until the bit goes high.

70.4.2 Initialize Device Message: MLV = RT: TR = 1: MODE CODE = 14H.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C	1	1	1	1	1	1	0	0	0	0	0	1	0	1	0	0
S	1	1	1	1	1	ME	X	X	0	0	0	0	0	0	0	TF

At the start of the bootloader operation the Initialize Device Message is transferred once to initiate the loading process.

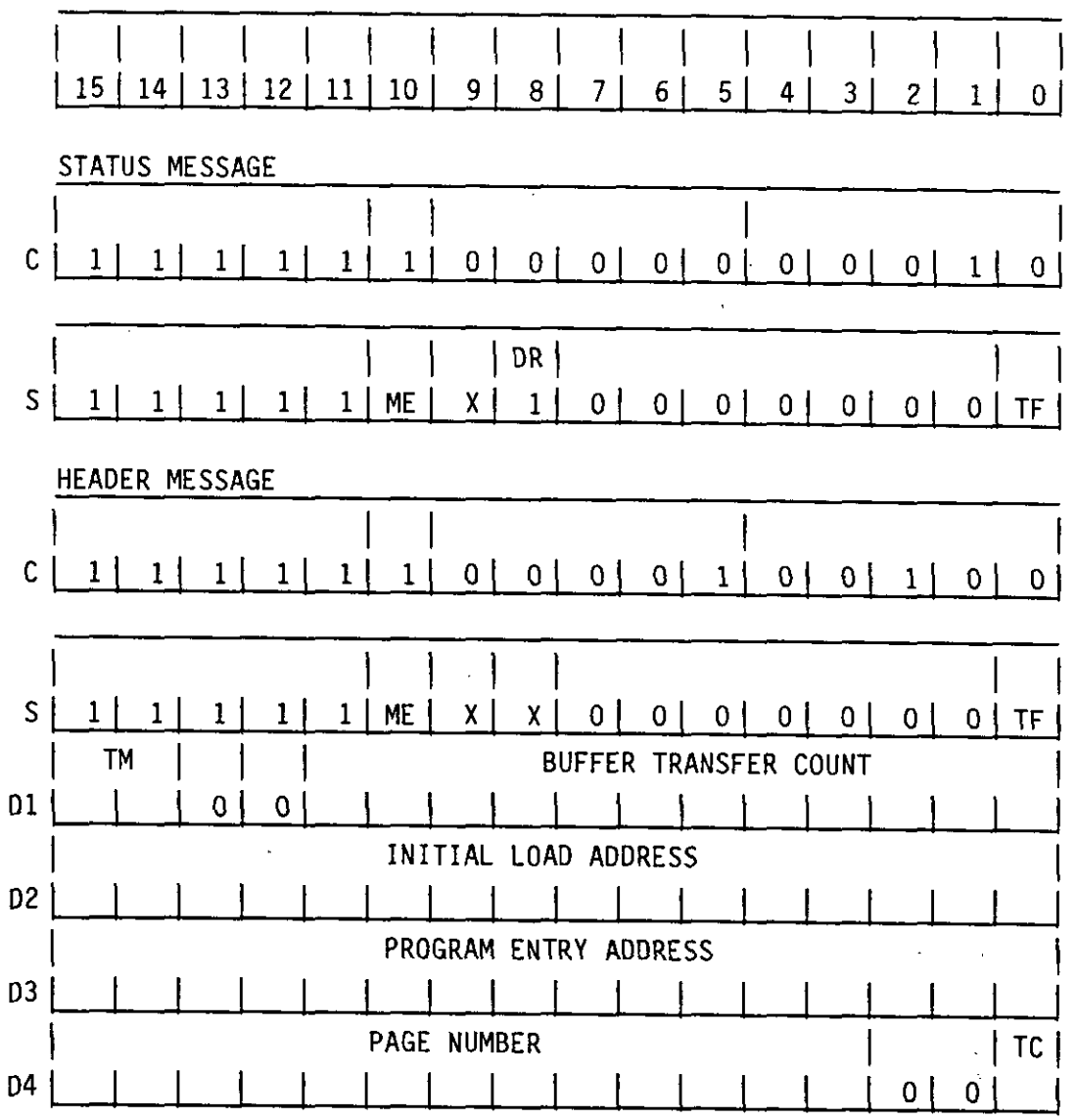
70.4.3 Initialize I/O Transfer Message: MLV = RT: TR = 1: MODE CODE = 15H.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STATUS MESSAGE																
C	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	0
S	1	1	1	1	1	ME	BY 0	X	0	0	0	0	0	0	0	TF
INITIALIZE I/O TRANSFER MESSAGE																
C	1	1	1	1	1	1	0	0	0	0	0	1	0	1	0	1
S	1	1	1	1	1	ME	X	X	0	0	0	0	0	0	0	TF

After transfer of the Initialize Device Message, the BC will poll the MLV with Status Messages. When the BY (Busy) bit in the STATUS RESPONSE WORD has been lowered (= 0), the BC will send the first Initialize I/O Transfer Message. This message is a command to the MLV to prepare for a HEADER, MEMORY DATA, ..., MEMORY DATA, TRAILER transaction; however, the Status Message will only precede the Initialize I/O Transfer Message for the first transfer of the Initialize I/O Transfer Message. The Initialize I/O Transfer Message is called the IPL Read Message in the Naval Avionics Center document entitled "Program Performance Specification Advanced Bootstrap Loader for AN/AYK-14(V) Single Card Processor."

70.4.4 Header: MLV = RT: TR = 1: SUBADDRESS = 01.

70.4.4.1 Header Bus Data.



Once the Initialize I/O Transfer Message has been sent, the first response to a Status Message with the DR bit set (= 1) in the STATUS RESPONSE WORD indicates that the MLV is ready for the Header Message to be commanded.

70.4.4.1.1 Header Message Utilization. This message is used to pass Load data to the unit.

70.4.4.2 Data Words.

70.4.4.2.1 Data Word 1.

a. TM (bits 14-15). The Transfer Mode (TM) bits are used to describe the Memory Data Load DATA WORD content. The TM bits are binary coded as follows:

1. TM = 00 No transfer. In the No Transfer Mode the Buffer Transfer Count and Initial Load Address have no meaning. This mode is used to transfer the Program Entry Address and Page Number or is used as a preamble to the Trailer Message.

2. TM = 01 Not used. An AYK-14 IPL fail will occur and processor will hang if this code were used.

3. TM = 10 16 bit transfer. Each 16 bits of data transmitted in a DATA WORD will contain 16 bits of information in bits 0-15.

4. TM = 11 32 bit transfer. The 16 bits of data transmitted in each odd word (first word is odd) contains the 16 LSB of data in bits 0-15 and each even word contains the 16 MSB of data in bits 0-15.

b. Buffer Transfer Count (bits 0-11). The Buffer Transfer Count is used to indicate the amount of data that will follow the Header Message. The Buffer Transfer Count has no meaning when the Transfer Mode is 00. The range of the Buffer Transfer Count is 1-4096 (value zero equals 4096). The Buffer Transfer Count is the total number of DATA WORDS that will be transmitted after the Header. The DATA WORDS will be transmitted in 32 word messages with the last message containing the remaining 32 or less words. The maximum transfer is 4096 words using 128 Memory Data Load messages.

c. Other bits. Bits 12 and 13 shall be zero.

70.4.4.2.2 Data Word 2.

a. Initial Load Address (bit 0-15). The Initial Load Address is the 16 or less LSB of the point in memory into which data is to be loaded. The maximum value (number of bits) used in the Initial Load Address will be compatible with the page size of units using paging. Unused bits shall be set to zero.

70.4.4.2.3 Data Word 3.

a. Program Entry Address (bits 0-15). The Program Entry Address has meaning only for Transfer Mode = 00. The Program Entry Address is the 16 or less LSB of the point in memory at which the unit being reprogrammed is to begin execution. The maximum value (number of bits) used in the Program Entry Address will be compatible with the page size of units using paging. Unused bits shall equal zero.

70.4.4.2.4 Data Word 4.

a. Page Number (bits 3-15). The Page Number represents up to 13 MSBs for page memory address. The Page Number applies to the Program Entry Address for Transfer Mode = 00. The Page Number applies to the Initial Load Address for Transfer Mode 10 and 11. Unused bits shall equal zero.

b. TC bit (bit 0). The Transfer Control bit may be used to transfer control to the program loaded after a memory load.

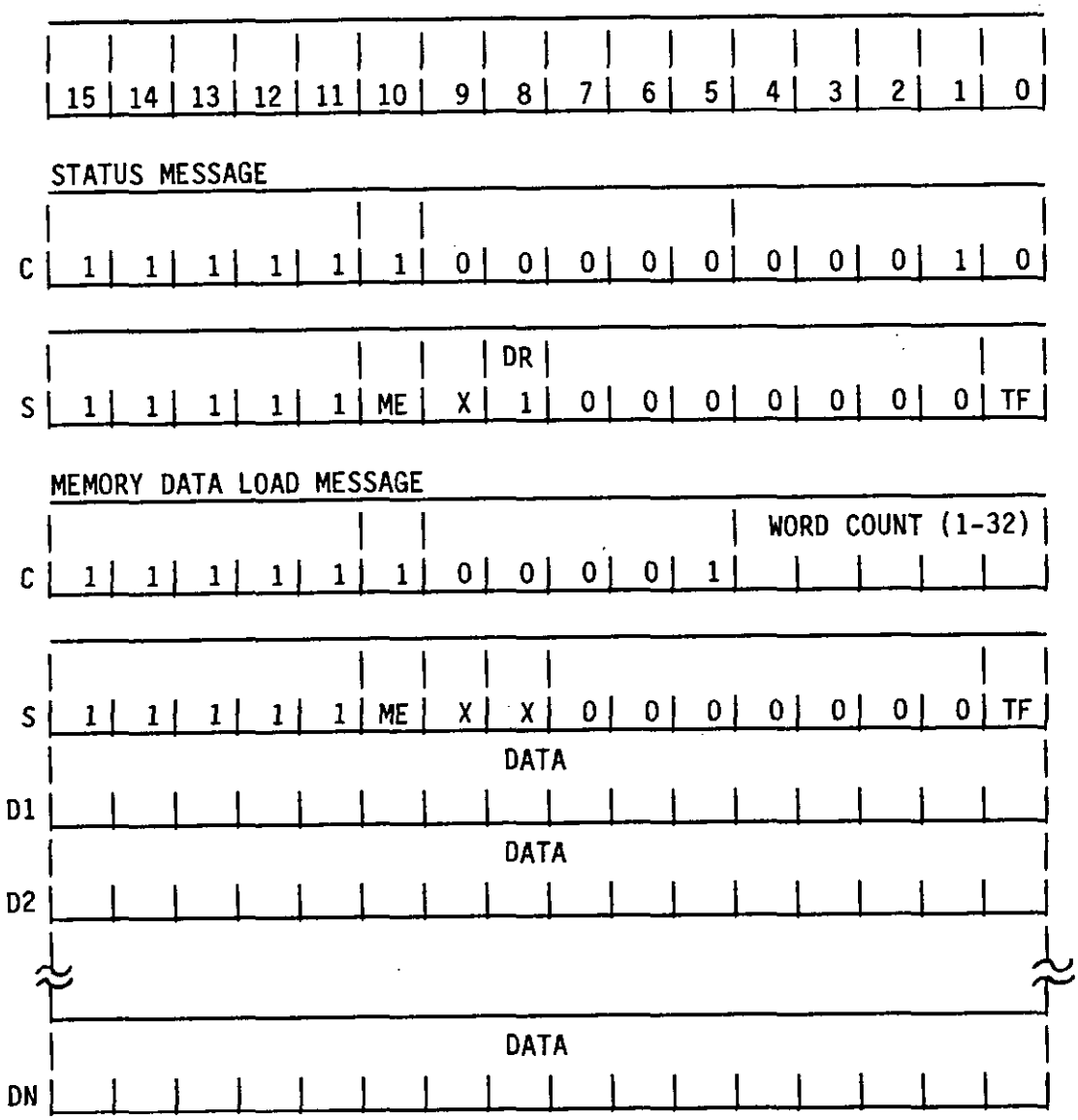
   1. TC = 0 Indicates this is the last HEADER, MEMORY DATA, ..., MEMORY DATA, TRAILER or HEADER, TRAILER transaction.

   2. TC = 1 Indicates that more data is to follow the current HEADER, MEMORY DATA, ..., MEMORY, DATA, TRAILER or HEADER, TRAILER transaction and control should not be transferred. For units using paging and the Program Entry Address, the TC will remain equal to one, even for the last data transaction, until a Transfer Mode = 00 message is used to supply the Program Entry Address and Page Number.

c. Other bits. Bits 1-2 shall be zero.

70.4.5 Memory Data Load: MLV = RT: TR = 1: SUBADDRESS = 01.

70.4.5.1 Memory Data Load Bus Data.



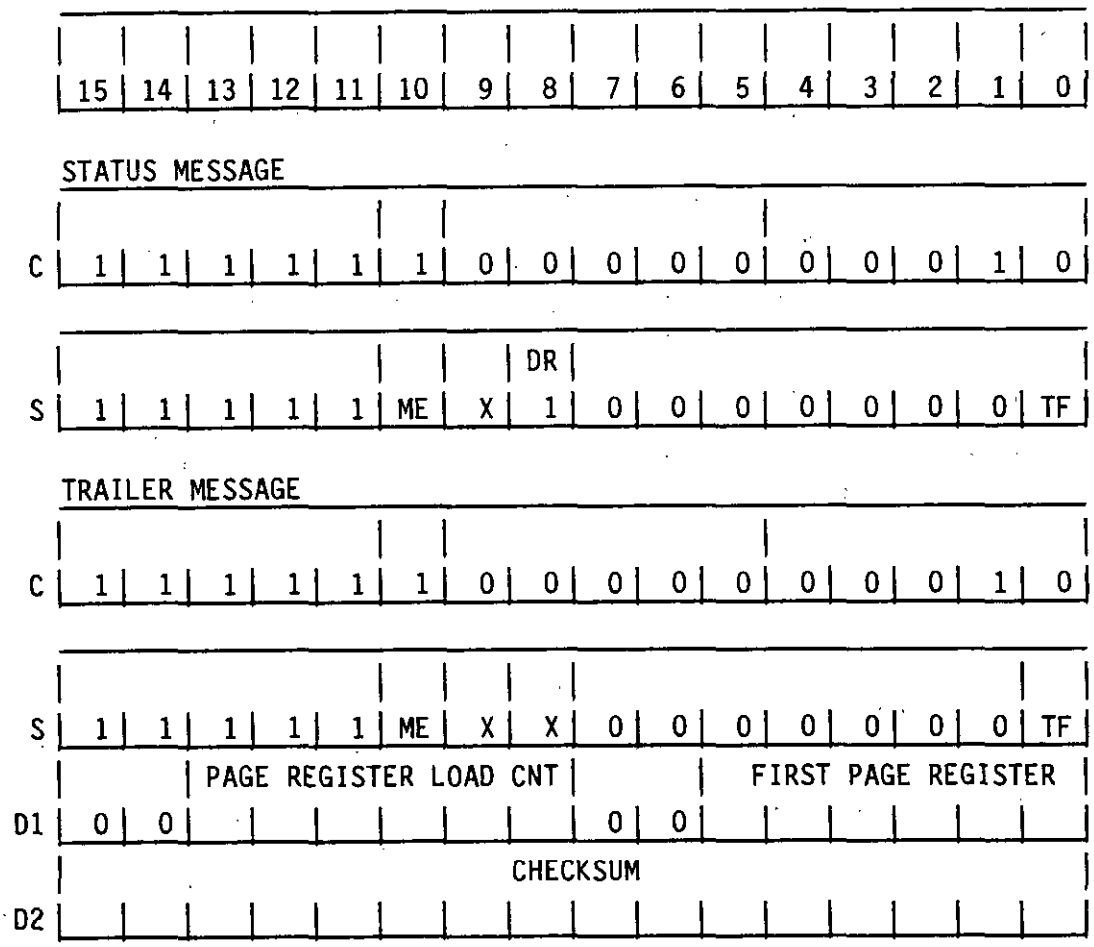
Once the Header Message has been transferred, or Memory Data Load Message transactions have started, the first response to a Status Message with the DR bit set (= 1) in the STATUS RESPONSE WORD indicates that the MLV is ready for the Memory Data Load Message to be commanded. Because of an anomaly in the BC loader, the first MLV response after a Header Message with the DR bit set is ignored and the second Status Message response with the DR bit set initializes the first Memory Data Load Message.

70.4.5.1.1 Memory Data Load Message Utilization. This message will be used to pass the data to be loaded into the unit.

70.4.5.2 Data Words. The number of Data Words will equal the WORD COUNT in the Memory Data Load Message COMMAND WORD.

70.4.6 Trailer Message: MLV = RT: TR = 1: SUBADDRESS = 01.

70.4.6.1 Trailer Bus Data.



Once all Memory Data Load Messages for a HEADER, MEMORY DATA, ..., MEMORY DATA, TRAILER transaction have been transferred (or after a Header Message with TM = 00), the first response to a Status Message with the DR bit set (= 1) in the STATUS RESPONSE WORD indicates that the MLV is ready for the Trailer Message to be commanded.

70.4.6.1.1 Trailer Message Utilization. This message is used to pass the data checksum and additional Load parameters to the unit.

70.4.6.2 Data Words.

70.4.6.2.1 Data Word 1.

a. Page Register Load Count (bits 8-13). The Page Register Load Count field specifies the number of consecutive pages needed to load the succeeding data record. The value of this number is written as one less than the actual number of pages (e.g., a count of zero in this field indicates that one page register is to be loaded). However, when the Page Number in the fourth word of the Header indicates Page Number zero, a zero in this field indicates that no (zero) page registers are to be loaded.

b. First Page Register (bits 0-5). This field specifies the number of the first page register which is to be modified with the page number given in the fourth word of the Header. Any attempt to modify page register zero (0) shall result in a load error.

c. Other bits. Bits 6-7 and 14-15 are not used and are set to zero.

70.4.6.2.2 Data Word 2.

a. Checksum (bits 0-15). The checksum will be the checksum of an entire transaction, i.e., HEADER, MEMORY DATA, ..., MEMORY DATA, TRAILER (when TM in Header Data 1 is not equal to zero) or HEADER, TRAILER (when TM in Header Data 1 is equal to zero). The checksum will be derived by a 2's complement 16 bit addition of every DATA WORD in the transaction (i.e., Header, Memory Data Load, Trailer DATA WORD) with the exception of the Checksum DATA WORD (Trailer Data 2). The 2's complement 16-bit addition is binary addition with the carry discarded (i.e., no end around carry) (e.g., FFFF (hex) + 1 = 0).

70.4.6.2.2.1 Checksum. The unit being reprogrammed shall be responsible for comparing the checksum received from the MLV with the data words. The checksum value in the second word of the Trailer is the checksum that should be computed by the unit. If the value computed does not match the value received, the IPL fail indicator is set and the load shall be terminated.

APPENDIX H

MESSAGE FORMATS MLV = BC, CP-1001 = RT

80. HARM CLC (CP-1001)

80.1 Applicability. The protocol of this appendix is applicable to loading and verifying the High Speed Anti-Radiation Missile (HARM) Command Launch Computer (CLC). This protocol is only applicable to the HARM CLC with nomenclature CP-1001. The protocol of this Appendix shall not be used for new designs without written approval of NAVAIRSYSCOM.

80.2 General Operation.

a. The MLV will have assumed Bus Controller (BC) status prior to utilizing this protocol and will assume the CLC acting as RT address 17 (11 hex) is ready to respond. The MLV will also have set the Avionics Reprogram Enable discretes. These discretes are not currently utilized by the CLC although they are wired to it. Depending on the operation indicated by the operator the MLV will proceed to load or verify the CLC. The UDF and OFP memories will be loaded and/or verified separately. The entire UDF (4,096 words) or the entire OFP (24,576 words) are always processed for either a load or verify function.

b. For the load operation the MLV will immediately start a sequence consisting of a Memory Data Load Message followed, after a 5 msec delay, by a Send Status Message. The MLV will only check for the presence of the STATUS RESPONSE WORD to the Memory Data Load Message (any STATUS RESPONSE WORD with the correct terminal address will be accepted by the MLV). The CLC status will be ascertained by the Send Status Message that follows the Memory Data Load Message (see Figure 17). After receipt of a valid Memory Data Load Message in which the checksum and parity are valid, the CLC shall enter boot-load mode and shall cease all other operations until CLC power has been cycled. The sequence of Memory Data Load Messages and Send Status Messages will continue until programming is completed (entire UDF or OFP requires 2048 sequences) or an error is detected. When the CLC response to a Send Status Message indicates a wait condition, the MLV will ignore the data in the Send Status Message and, after a 500 usec delay, will repeat the Send Status Message until a wait condition is no longer indicated. If the wait condition does not clear after the number of tries indicated in the Lookup Table (busy bit count in Lookup Table), the MLV will declare an error. If the Ready bit in DATA WORD 1 of the Send Status does not indicate ready within the number of tries indicated in the Lookup Table, the MLV will declare an error. For each Send Status Message received, the MLV will check for CLC errors by checking that: the indicated Received Data Status is correct; that the CLC Starting Address returned was the same as what was sent; that the CLC correctly completed the reprogramming from the last Memory Data Load Message;

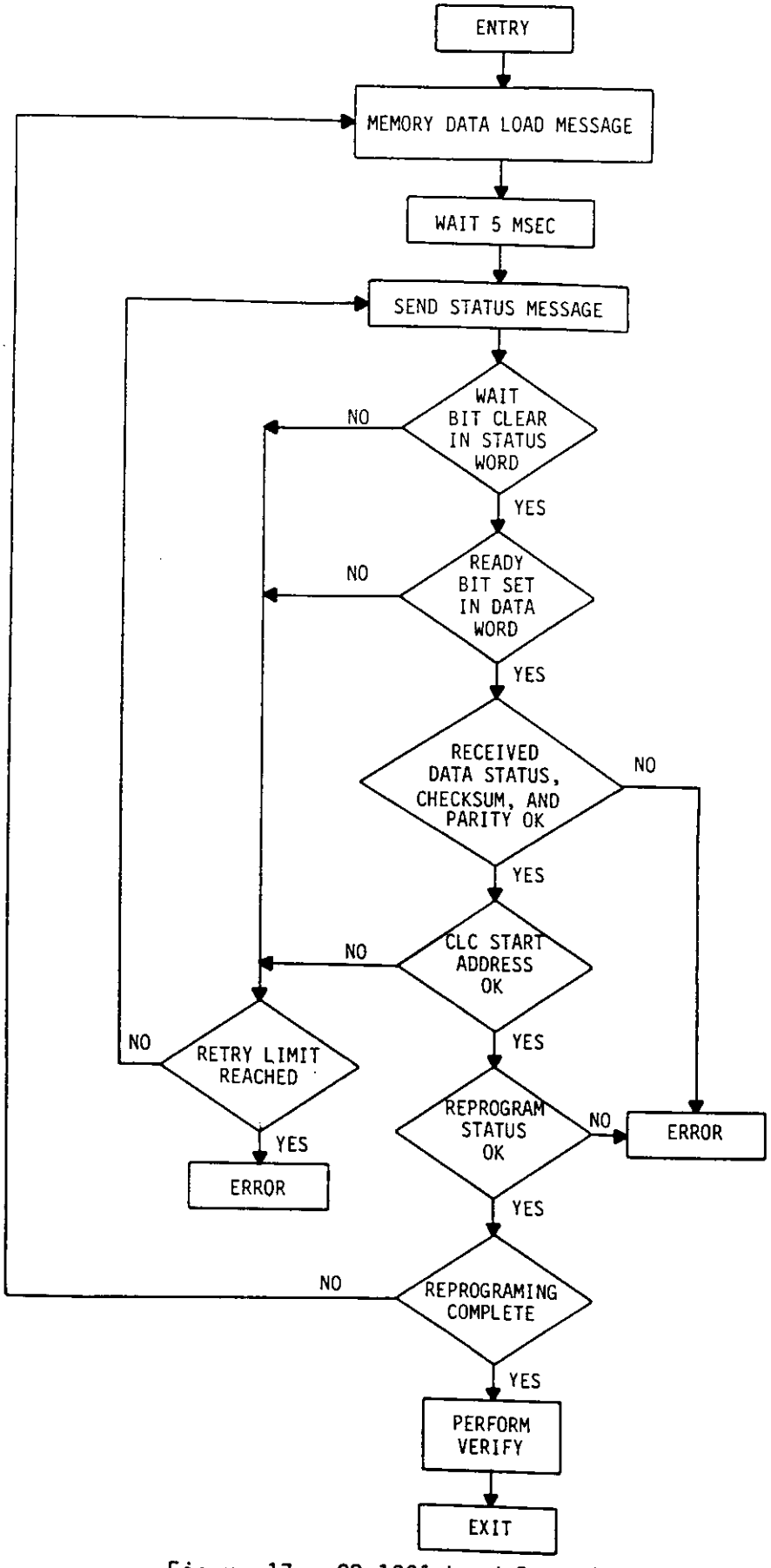


Figure 17. CP-1001 Load Procedure.

and, that the Checksum and Parity computed by the CLC is correct. If the CLC Starting Address returned is incorrect, the MLV will repeat Send Status Messages as if the wait condition was indicated in the STATUS RESPONSE WORD. For any other discrepancy the MLV will declare an error.

c. For the verify operation the MLV will immediately start a sequence consisting of a Prepare Memory Verification Data Message followed, after a 5 millisecond delay, by a Send Memory Verification Data Message (see Figure 18). The MLV will only check for the presence of the STATUS RESPONSE WORD to the Prepare Memory Verification Data Message (any STATUS RESPONSE WORD with the correct terminal address will be accepted by the MLV). The CLC status will be ascertained only by examining the CLC starting address in the Send Memory Verification Data Message. After receipt of a valid Prepare Memory Verification Data Message with a valid Checksum, the CLC shall enter bootload mode and shall cease all other operations until CLC power has been cycled. The sequence of Prepare Memory Verification Data Messages and Send Memory Verification Data Messages shall continue until programming is completed (entire UDF or OFP requires 2048 sequences) or an error is detected. If the CLC starting address returned in the Send Memory Verification Data Message does not match the CLC Starting Address sent in the Prepare Memory Verification Data Message, the MLV will ignore the remainder of the data in the Send Memory Verification Data Message and will repeat the Send Memory Verification Data Message until the correct CLC Starting Address is returned. If the correct CLC Starting Address is not returned after the number of tries indicated in the Lookup Table, the MLV will declare an error.

80.3 Status Response Word: MLV = BC.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
S	TERMINAL ADDRESS					ME	W									
	1	0	0	0	1			X	X	X	X	X	0	X	X	X

A STATUS RESPONSE WORD will be provided by the CLC for each message transaction. The STATUS RESPONSE WORD will follow the data on an RT receive type transaction and will precede the data on an RT transmit type transaction. The MLV will allow a response time gap of 12 usec from the end of the last transmitted COMMAND WORD (transmit type message) or the end of the last transmitted DATA WORD (receive type message), to the start of the RT STATUS RESPONSE WORD

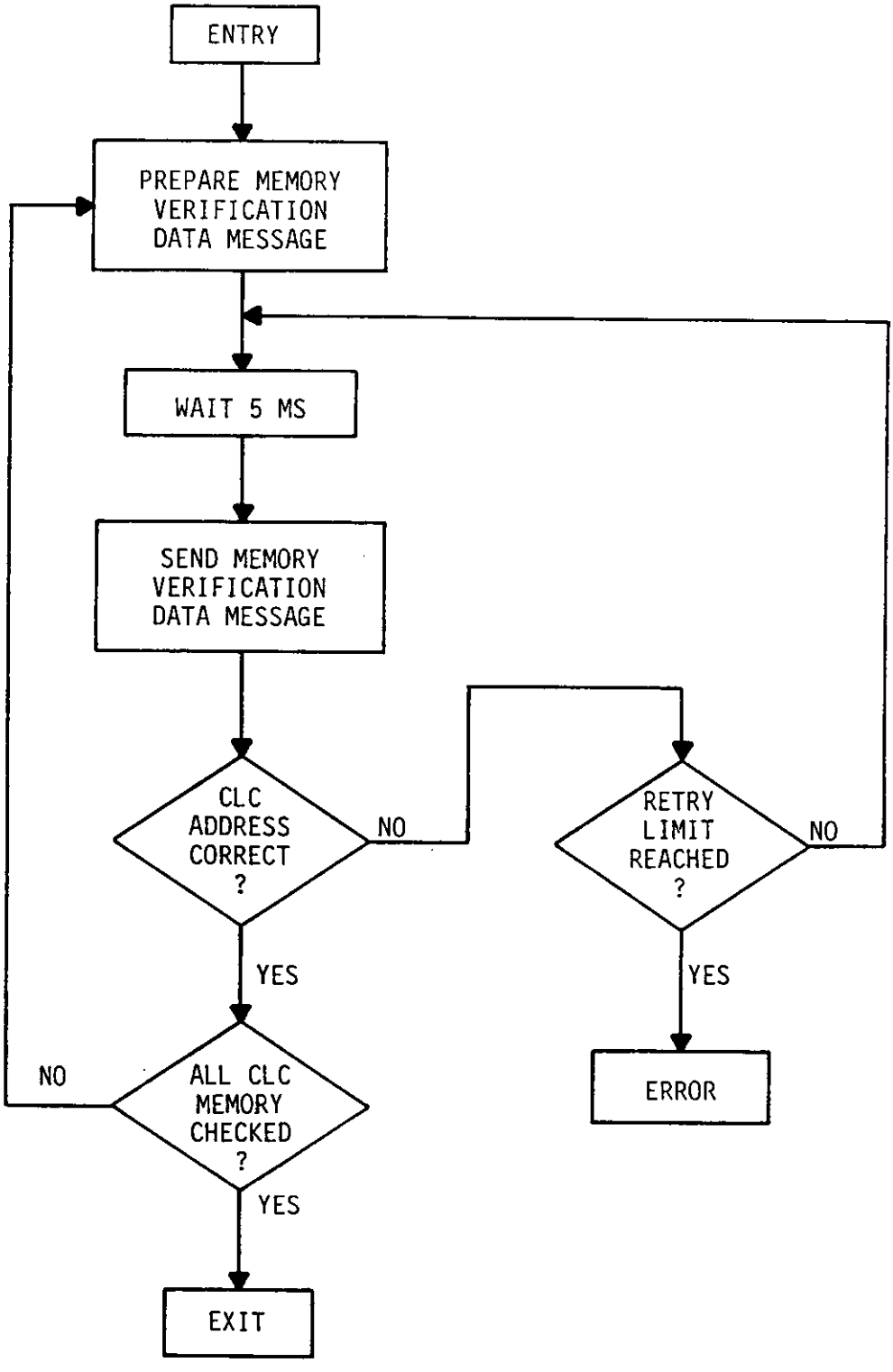


Figure 18 CP-1001 Verify Procedure

before declaring a no response error (equivalent of 14 usec when measured in accordance with MIL-STD-1553B). Under normal conditions the RT shall begin the STATUS RESPONSE WORD within the period of 2-10 usec from the receipt of the end of the last COMMAND WORD (transmit type message) or the receipt of the end of the last DATA WORD (receive type message) (equivalent of 4-12 usec when measured in accordance with MIL-STD-1553B). The MLV will ensure that the time from the end of the RT transmission of the last DATA WORD (transmit type message), or the end of the last STATUS RESPONSE WORD (receive type message) to the beginning of the next COMMAND WORD is at least 8 usec (Equivalent of 10 usec when measured in accordance with MIL-STD-1553B). The fields within this word are as follows:

a. TERMINAL ADDRESS (bits 11-15). The RT address will be the normal RT address of the unit being reprogrammed. This address is fixed for the CLC as 17 (11 hex).

b. ME bit (bit 10). The Message Error (ME) bit may be set high (= 1) by the RT under any of the following conditions:

   1. message short in data word count
   2. failure to pass word validation
   3. improperly timed data sync
   4. non-contiguous data
   5. undefined subaddress/mode code

   If set, the RT shall clear the ME bit as soon as it has completed transmission of status or has suppressed status because of message anomalies. Upon receipt of a STATUS RESPONSE WORD with the ME bit set, or no status, the MLV will retry the most recent record two more times. If unsuccessful at this point, the load operation will be terminated.

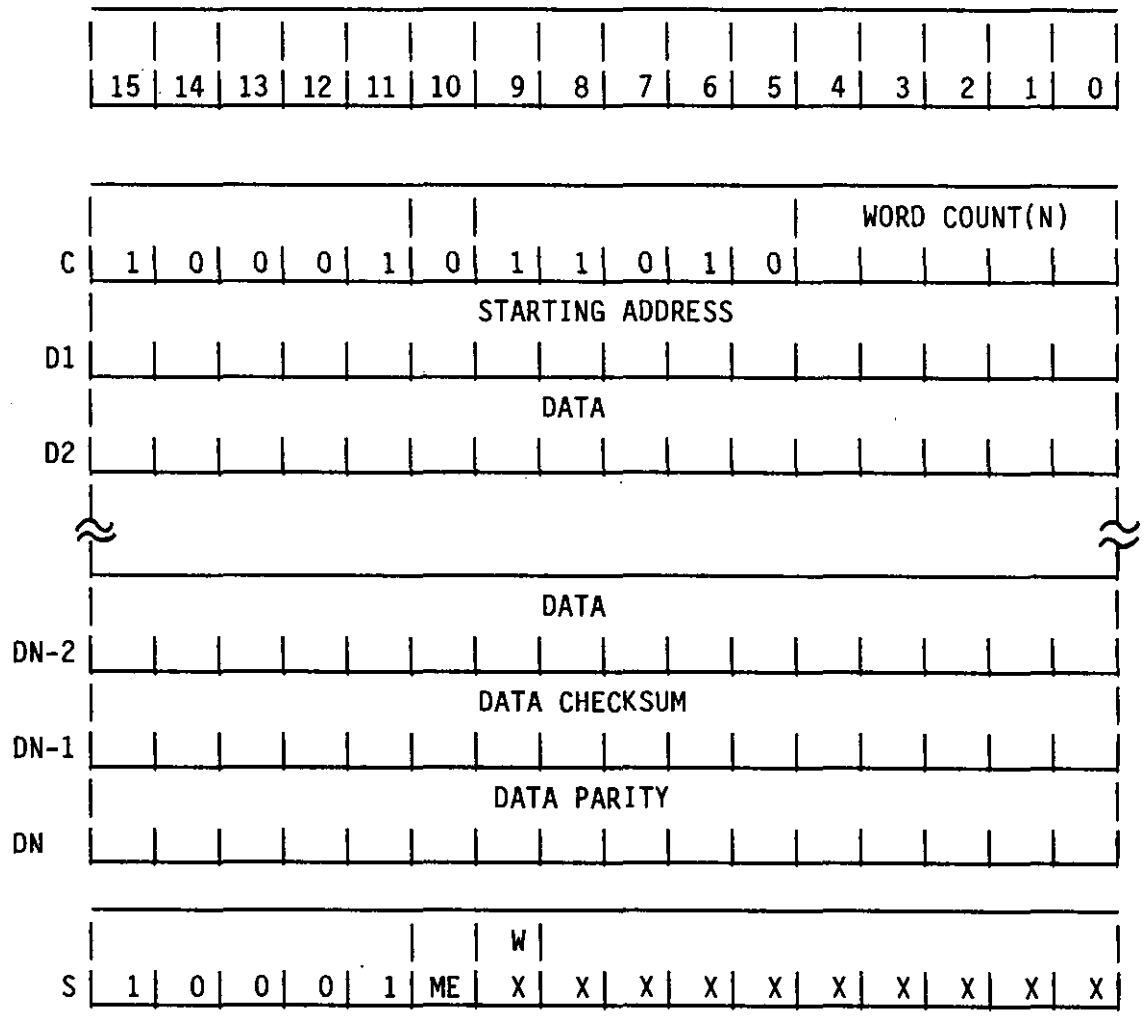
c. W bit (bit 9). The Wait (W) bit will be set high (= 1) to indicate that the RT is not ready to send or receive messages. The MLV will only examine this bit in STATUS RESPONSE WORDS associated with Send Status Messages.

d. Bit 3 although not utilized in the protocol must be set to 0 in order to allow the MLV to receive the Data Words transmitted by the RT.

e. Other bits. Bits 0-2, 4-8 will not be used by the MLV; thus, the bit may be 1 or 0.

80.4 Messages.

80.4.1 Memory Data Load Message: MLV = BC: TR = 0: SUBADDRESS = 1AH.



80.4.1.1 Memory Data Load Message Utilization. The Memory Data Load Message shall be used by the MLV to transfer memory data to the RT to be programmed into its EEPROM memory. Each Memory Data Load Message shall be followed by one or more Send Status Messages until the RT has processed the last data sent and is not indicating a wait condition in the Send Status Message.

80.4.1.2 Data Words. When reprogramming the CLC OFP memory, twelve memory locations shall be reprogrammed with the same Memory Data Load Message, resulting in a COMMAND WORD WORD COUNT (N) of 15. When reprogramming UDF memory, two memory locations shall be reprogrammed with the same Memory Data Load Message, resulting in a COMMAND WORD WORD COUNT (N) of 5. The extra 3 words required in either case are the Starting Address, the Data Checksum, and the Data Parity.

80.4.1.2.1 Data Word 1.

a. Starting Address (bits 0-15). The Starting Address is the memory location corresponding to DATA WORD 2 of the message. The memory location of each succeeding DATA WORD shall correspond to plus 2048 locations (800H) in memory relative to the memory location of the preceding DATA WORD.

80.4.1.2.2 Data Words 2 through N-2.

a. Data (bits 0-15). The data sent to the CLC shall provide the information to be programmed into the RT memory.

80.4.1.2.3 Data Word N-1.

a. Data Checksum (bits 0-15). The checksum of all the RT memory data shall be sent as DATA WORD N-1. The checksum shall be the 2's complement of the addition of DATA WORDS 2 through N-2 using 2's complement 16-bit addition. The 2's complement 16 bit addition is binary addition with the carry discarded (i.e., no end around carry) (e.g., FFFF hex + 1 = 0). The 2's complement of this result is the result exclusive ORed with the value FFFF (hex) and then added to 1 with any carry discarded. If the 2's complement addition result was 2ADF (hex), the Checksum value would be D521 (hex).

80.4.1.2.4 Data Word N.

a. Data Parity (bits 0-15). The parity of all of the RT memory data shall be sent as message word N. The Parity shall be the exclusive OR of DATA WORDS 2 through N-2.

80.4.2 Send Status Message: MLV = BC: TR = 1: SUBADDRESS = 1AH.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C	1	0	0	0	1	1	1	1	0	1	0	0	0	1	0	0
							W									
S	1	0	0	0	1	ME	0	X	X	X	X	X	X	X	X	X
	SPARES												RDS	PSTAT		R
D1	X	X	X	X	X	X	X	X	X	X	X	X				
	DATA CHECKSUM															
D2																
	DATA PARITY															
D3																
	STARTING ADDRESS															
D4																

80.4.2.1 Send Status Message Utilization. The Send Status Message shall be used by the MLV to ascertain the RT's current status. When the Wait (W) bit is set (= 1) in the STATUS RESPONSE WORD, it shall indicate that the RT's status data is not up-to-date.

80.4.2.2 Data Words.

80.4.2.2.1 Data Word 1.

a. RDS (bit 3). The Received Data Status (RDS) bit shall indicate whether the RT received the last Memory Data Load Message data without error. The RDS bit shall be set high (= 1) to indicate an error.

b. PSTAT (bits 1-2). The Programming STATus (PSTAT) bits shall be used to indicate the status of RT memory programming. The RT shall attempt to program its memory with the data from a single Memory Data Load Message up to three times before declaring an error. The bits shall be coded as follows:

1. PSTAT = 00 The RT was able to correctly program the memory data from the previous Memory Data Load Message on the initial attempt.

2. PSTAT = 01 The RT was able to correctly program the memory data from the previous Memory Data Load Message on the second attempt.

3. PSTAT = 10 The RT was able to correctly program the memory data from the previous Memory Data Load Message on the third attempt.

4. PSTAT = 11 The RT was unable to correctly program the memory data from the previous Memory Data Load Message after three tries to do so. This may also indicate a generic failure in the RT.

c. R (bit 0). The Ready bit shall indicate whether the RT is busy performing the last operation or is ready to continue. The R bit shall be set high (= 1) to indicate Ready and set low (= 0) to indicate that the RT is busy.

d. Other bits. Bits 4-15 will *not* be utilized by the MLV; thus, these bits may be 1 or 0.

80.4.2.2.2 Data Word 2.

a. Data Checksum (bits 0-15). The checksum computed by the RT for all the reprogrammed memory data received in DATA WORDS 2 through N-2 of the last Memory Data Load Message. The Data Checksum shall be computed by the RT as described in 80.4.1.2.3.

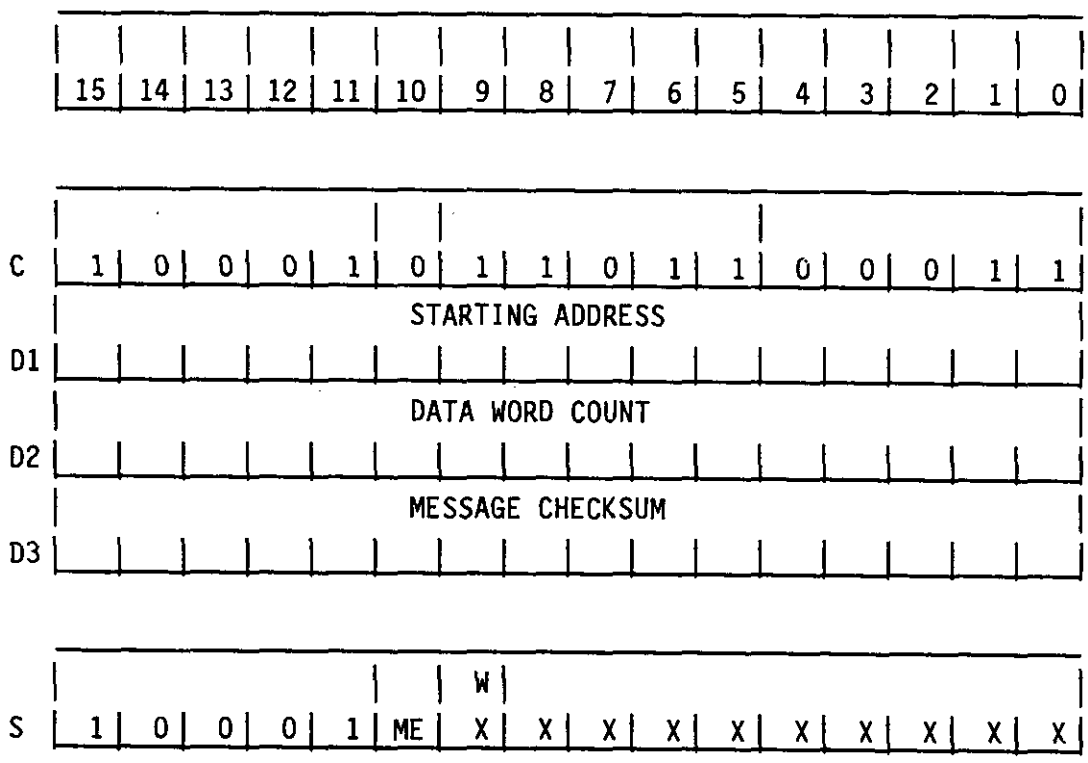
80.4.2.2.3 Data Word 3.

a. Data Parity (bits 0-15). The parity of all the reprogrammed memory data computed by the RT by an exclusive OR of the information in DATA WORDS 2 through N-2 of the last Memory Data Load Message.

80.4.2.2.4 Data Word 4.

a. Starting Address (bits 0-15). The Starting Address received by the RT in the first DATA WORD of the last Memory Data Load Message.

80.4.3 Prepare Memory Verification Data Message: MLV = BC: TR = 0: SUBADDRESS = 1BH.



80.4.3.1 Prepare Memory Verification Data Message Utilization. The Prepare Memory Verification Data Message shall be used to tell the RT to prepare a set of memory words for transmission to the bus controller.

80.4.3.2 Data Words.

80.4.3.2.1 Data Word 1.

a. Starting Address (bits 0-15). The first data word contains the RT Starting Address. This address is the memory location that determines the contents of the first data word to be returned in the following Send Memory Verification Data Message. The memory location that determines the contents of each succeeding DATA WORD in the Send Memory Verification Data Message that follows shall be incremented by 2048 locations (800H).

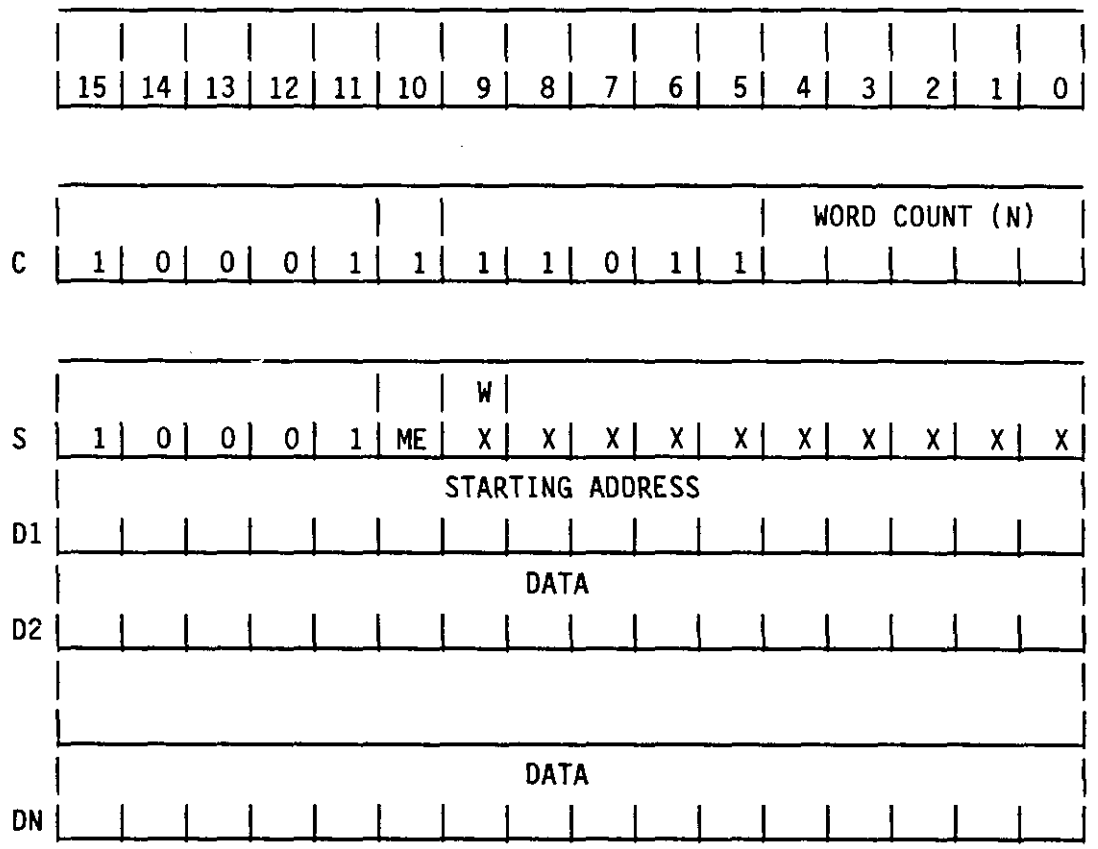
80.4.3.2.2 Data Word 2.

a. Data Word Count (bits 0-15). Any area of RT memory may be verified (read). When verifying the OFP, twelve memory locations shall be read at the same time; thus, a Data Word Count of 12 shall be used. When verifying the UDF memory, two memory locations shall be read at the same time; thus, a Data Word Count of 2 shall be used.

80.4.3.2.3 Data Word 3.

a. Message Checksum (bits 0-15). The third data word shall contain the checksum of the Starting Address and the Data Word Count provided in DATA WORDS 1 and 2 of this message. The checksum shall be the 2's complement of the addition of these DATA WORDS using 2's complement 16-bit addition. The 2's complement 16 bit addition is binary addition with the carry discarded (i.e., no end around carry) (e.g., FFFF hex + 1 = 0). The 2's complement of this result is the result exclusive ORed with the value FFFF (hex) and then added to 1 with any carry discarded. If the 2's complement addition result was 2ADF (hex), the Checksum value would be D521 (hex).

80.4.4 Send Memory Verification Data Message: MLV = BC: TR = 1: SUBADDRESS = 1BH.



80.4.4.1 Send Memory Verification Data Message Utilization. The Send Memory Verification Data Message shall be used to retrieve from the RT the set of memory words requested by the preceding Prepare Memory Verification Data Message.

80.4.4.2 Data Words. The WORD COUNT (N) indicated in the COMMAND WORD will always be one greater than the Data Word Count provided in DATA WORD 2 of the previous Prepare Memory Verification Data Message. The value of N will be three for a UDF verify and 13 for an OFP verify.

80.4.4.2.1 Data Word 1.

a. Starting Address (bits 0-15). The Starting Address shall be the memory location corresponding to DATA WORD 2 of the message. The memory location of each succeeding DATA WORD shall correspond to plus 2048 locations (800H) in memory relative to the memory location of the preceding DATA WORD.

80.4.4.2.2 Data Words 2 through N.

a. Data (bits 0-15). The data sent by the RT shall be used by the MLV to verify the memory contents.

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APPENDIX I

GLOSSARY

AC	Alternating Current
ASCII	American Standard Code for Information Interchange
ASPJ	Advanced Self Protection Jammer
AV	Avionics
B	Busy
BC	Bus Controller
BER	Bit Error Rate
BIT	Built-In Test, Binary Digit
BSY	Busy
BUS	Data Bus
BY	Busy
C	Command Word or Complete Restart
CLC	Command Launch Computer (HARM)
CWJ	Continuous Wave Jammer
D	Data Word
DC	Direct Current
DECM	Deceptive ECM
DR	Data Ready
DSM	Discrete Serial Module
ECM	Electronic Counter-Measures
EEPROM	Electrically Erasable Programmable Read Only Memory
EMC	Electromagnetic Compatibility
EN	Enable
EW	Electronic Warfare
GND	Ground
GSE	Ground Support Equipment
H	Hexadecimal
HARM	High-speed Anti-Radiation Missile
HT	Header Type
Hz	Hertz
ICD	Interface Control Document
ID	Identification
IMA	Intermediate Maintenance Activity
IPL	Initiate Program Load
K	One Thousand or a One Thousand Twenty Four in Decimal
LSB	Least Significant Bit
L/V	Load/Verify

GLOSSARY - Continued

MA	Milliamperes
MDC	McDonnell Douglas Corporation
ME	Message Error
MHz	MegaHertz
MLV	Memory Loader/Verifier
MS	Memory Select
MSB	Most Significant Bit
MSD	Memory Storage Device
MSDRS	Maintenance Signal Data Recording Set
MUX	Multiplex
N	Number of DATA WORDS in WORD COUNT
NAVAIRDEVCEN	Naval Air Development Center
O-Level	Organizational Level Maintenance
OFP	Operational Flight Program
OS	Operating Software
OSM	Operating Software Memory
P	Parity
PROM	Programmable Read Only Memory
PWR	Power
PSTAT	Programming STATus
R	Ready
RDP	Radar Data Processor
RDS	Received Data Status
RMS	Root Mean Square
RT	Remote Terminal, Record Type
RWR	Radar Warning Receiver
S	Status or Success
SC	Status Code
SDC	Signal Data Computer
SF	Status Flag
SI	Status Indicator
SIM	Serial Interface Module
SMS	Stores Management System
SR	Service Request
SYNC	Synchronization Waveform
T	Transaction
TC	Transfer Control
TF	Terminal Flag
TM	Transfer Mode
TR	Transmit/Receive

GLOSSARY - Continued

UDF	User Data File
UDM	User Data Memory
V	Volt
VAC	Volts AC
VDC	Volts DC
W	Wait
WER	Word Error Rate
WRA	Weapons Replaceable Assembly
X	Don't Care (0 or 1)
u	Micro
ϕ	Phase
1	Bit ON, Set, HIGH
0	Bit OFF, Clear, LOW

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