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MILITARY STANDARD

FLEXIBLE AND RIGID-FLEX

PRINTED-WIRING FOR

ELECTRONIC EQUIPMENT

DESIGN REQUIREMENTS FOR

TO ALL HOLDERS OF MIL-STD-2118:

1. THE FOLLOWING PAGES OF MIL-STD-2118 HAVE BEEN REVISED AND SUPERSEDE THE PAGES LISTED:

NEW PAGE	DATE	SUPERSEDED PAGE	DATE
21	4 May 1984	21	REPRINTED WITHOUT CHANGE
22	12 May 1986	22	4 May 1984
22a	12 May 1986	22	4 May 1984
22b	12 May 1986	23	4 May 1984
23	12 May 1986	23	4 May 1984
24	4 May 1984	24	REPRINTED WITHOUT CHANGE

2. RETAIN THIS NOTICE AND INSERT BEFORE TABLE OF CONTENTS.

3. Holders of MIL-STD-2118 will verify that page changes and additions indicated above have been entered. This notice page will be retained as a check sheet. This issuance, together with appended pages, is a separate publication. Each notice is to be retained by stocking points until the military standard is completely revised or canceled.

Custodians:
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Navy - EC
Air Force - 17

Review activities:
Army - AR, MI
Navy - OS, SH
Air Force - 11, 16, 85, 99
DLA - ES
NSA/S2

User activities:
Navy - AS, CG, MC
Air Force - 19

Preparing activity:
Navy - EC

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DLA - ES

(Project 5999-0175)

AMSC N/A

FSC 5999

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NOTES:
1. Dimensions are in inches.
2. Test coupons are to be identified with the following:
   a. FSCM.
   b. Part number and revision letter.
   c. Board traceability or lot number.
3. All lines shall be .020 (0.51 mm) ±.003 (0.08 mm), unless otherwise specified.
4. Unless otherwise specified, the tolerances shall meet the requirements of this standard.
5. The minimum land dimension shall be .070 (1.78 mm) ±.005 (0.13 mm) and represent the land shape used on the associated board. Holes in lands shall be the diameter of the smallest component hole in the associated board.
6. All first layers and internal layers shall be as specified on the master drawing. Copper plane areas shall be used on all coupons on appropriate plane layers, except for the D and E segments. When shields are used (see 5.11) appropriate layers shall be added to the coupons.
7. The lengths of test circuits D and E are dependent upon the number of layers in the panel. For test circuits D, a pair of holes and a conductor between same shall be provided for each layer. Electrical connection shall be in series, stepwise, through each conductor layer of the board. For test circuit E, a pair of holes and conductors shall be provided for the first layer and each internal layer.
8. Coupon F shall be positioned in the flexible area on the associated board.
9. The quality conformance test circuitry may be segmented; however, test circuitry A and B shall be joined together. Test circuit C, D, E, and F may be arranged to optimize board layout. All test coupons illustrated shall appear on each panel. The number of layers shall be identical to the number of layers in the boards derived from the panel.
10. Letters on coupons are for identification purposes only and shall be etched or applied by the use of a permanent ink which will withstand board processing. Location of letters on applicable coupons is optional.
11. Number of layers shown in these test coupons are for illustration purposes only. Conductor layer number 1 shall be the first layer on the component side, and all other conductor layers shall be counted consecutively downward through the laminated board to the bottom conductor layer which is the solder side. Surface layers shall consist of the outer layers of a printed-wiring board, the first layer (component side) and the last layer (solder side).

FIGURE 1. Quality conformance test circuitry - Continued.

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(FOR USE IN DETERMINING CURRENT CARRYING CAPACITY AND SIZES OF ETCHED COPPER CONDUCTORS FOR VARIOUS TEMPERATURE RISES ABOVE AMBIENT)

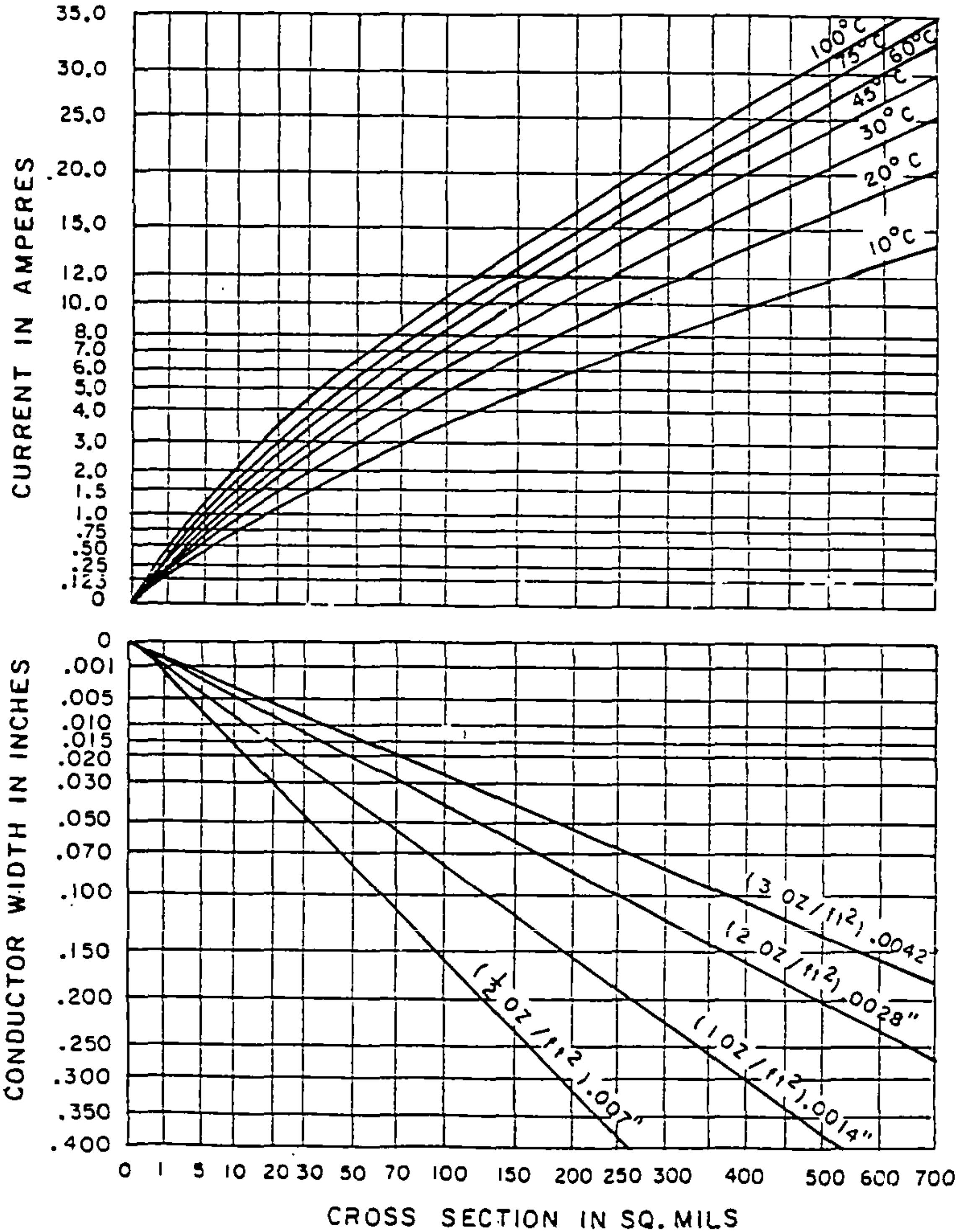

FIGURE 2. Current carrying capacities.

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NOTES:

1. The design chart has been prepared as an aid in estimating temperature rises (above ambient) vs current for various cross-sectional areas of etched copper conductors. It is assumed that for normal design conditions prevail where the conductor surface area is relatively small compared to the adjacent free panel area. The curves as presented include a nominal 10 percent derating (on a current basis) to allow for normal variations in etching techniques, copper thickness, conductor width estimates, and cross-sectional area.
2. Additional derating of 15 percent (current-wise) is suggested under the following conditions:
   (a) For panel thickness of 1/32 inch or less.
   (b) For conductor thickness of 0.0042 inch (3 oz/ft^2) or thicker.
3. For general use the permissible temperature rise is defined as the difference between the maximum safe operating temperature of the laminate and the maximum ambient temperature in the location where the panel will be used.
4. For single conductor applications the chart may be used directly for determining conductor widths, conductor thickness, cross-sectional area, and current-carrying capacity for various temperature rises.
5. For groups of similar parallel conductors, if closely spaced, the temperature rise may be found by using an equivalent cross-section and an equivalent current. The equivalent cross-section is equal to the sum of the cross-sections of the parallel conductors, and the equivalent current is the sum of the currents in the conductors.
6. The effect of heating due to attachment of power dissipating parts is not included.
7. The conductor thicknesses in the design chart do not include conductor overplating with metals other than copper.

Current-carry capacity for surface layers.

FIGURE 2. Current carrying capacities - Continued.

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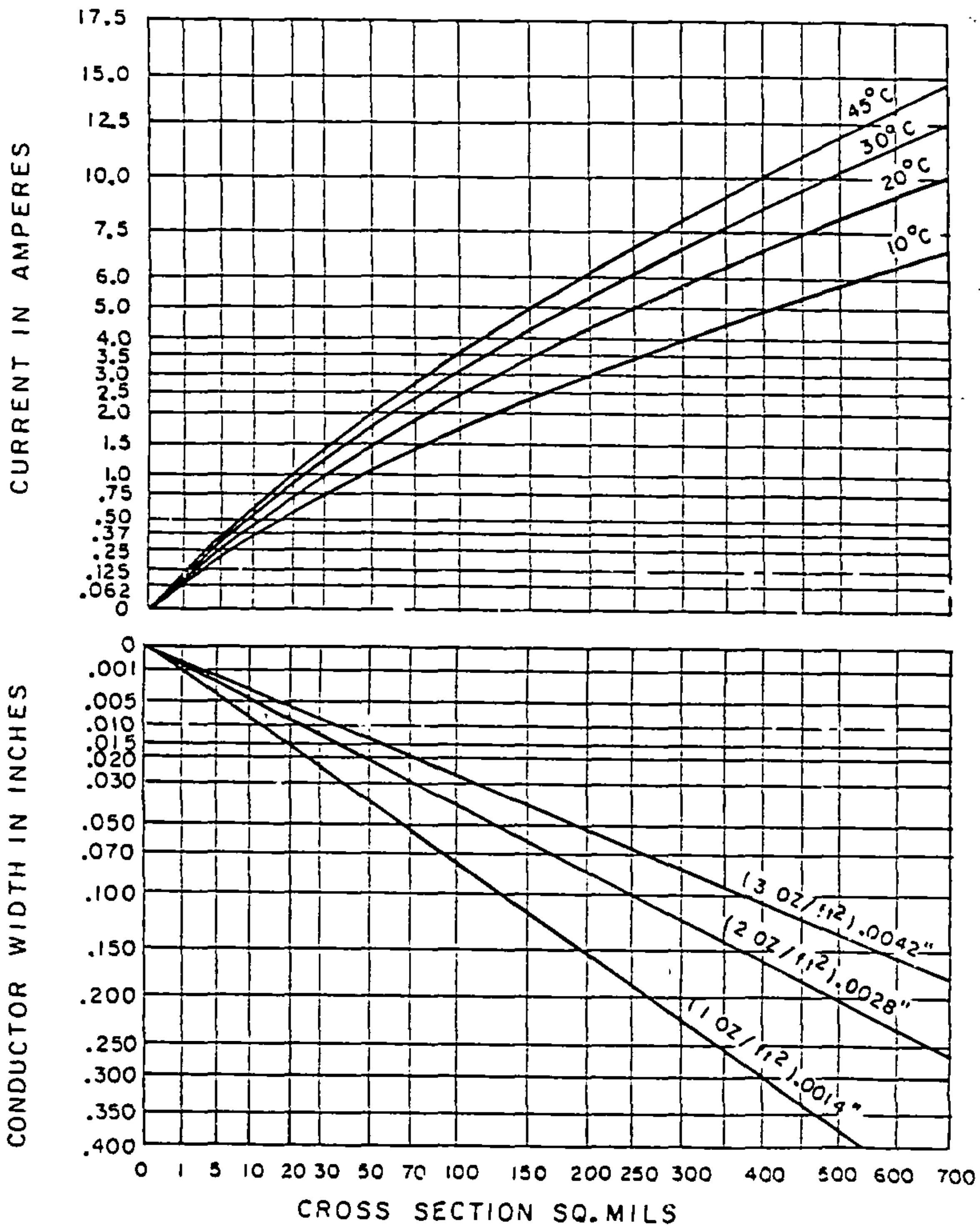

FIGURE 2. Current carrying capacities - Continued.

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NOTES:

1. The design chart has been prepared as an aid in estimating temperature rises (above ambient) vs current for various cross-sectional areas of etched copper conductors. It is assumed that for normal design conditions prevail where the conductor surface area is relatively small compared to the adjacent free panel area. The curves as presented include a nominal 10 percent derating (on a current basis) to allow for normal variations in etching techniques, copper thickness, conductor width estimates, and cross-sectional area.
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3. For general use the permissible temperature rise is defined as the difference between the maximum safe operating temperature of the laminate and the maximum ambient temperature in the location where the panel will be used.
4. For single conductor applications the chart may be used directly for determining conductor widths, conductor thickness, cross-sectional area, and current-carrying capacity for various temperature rises.
5. For groups of similar parallel conductors, if closely spaced, the temperature rise may be found by using an equivalent cross-section and an equivalent current. The equivalent cross-section is equal to the sum of the cross-sections of the parallel conductors, and the equivalent current is the sum of the currents in the conductors.
6. The effect of heating due to attachment of power dissipating parts is not included.
7. The conductor thicknesses in the design chart do not include conductor overplating with metals other than copper.

Current-carry capacity for internal layers (includes conductors with coverlayers).

FIGURE 2. Current carrying capacities - Continued.

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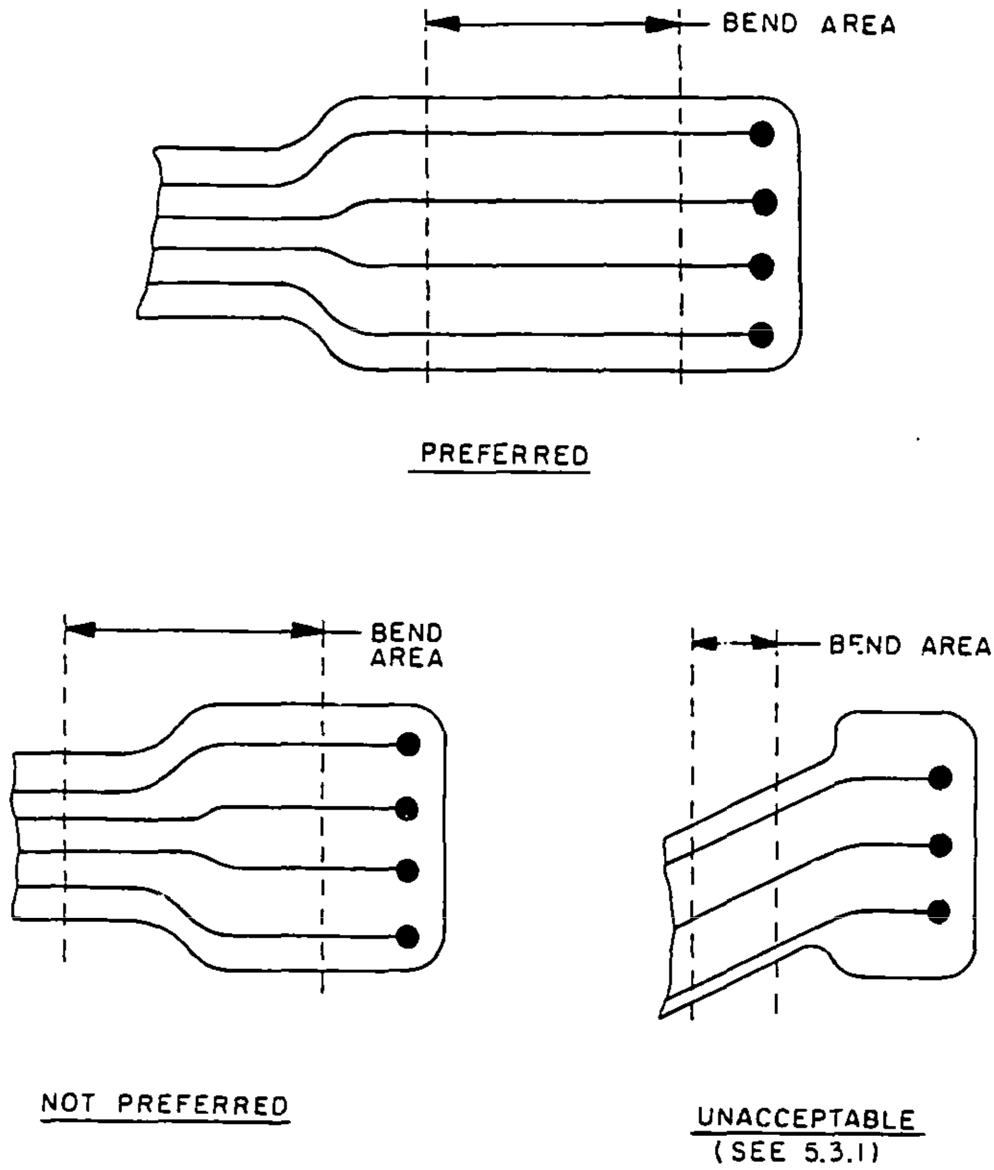

FIGURE 3. Bend position.