MIL-STD-2117(EC)
27 FEBRUARY 1981

MILITARY STANDARD

COMMUNICATIONS, DIGITAL CONTROL AND STATUS INFORMATION INTERCHANGE STANDARD

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FSC TCTS

DEPARTMENT OF DEFENSE
Washington, D.C. 20301

Control and Status Information Interchange Standard

MIL-STD-2117(EC)

1. This Military Standard is approved for use by the Naval Electronic Systems Command, Department of the Navy, and is available for use by all Departments and Agencies of the Department of Defense.

2. Beneficial comments (recommendations, additions, deletions) and any pertinent data which may be of use in improving this document should be addressed to: Commander, Naval Electronic Systems Command (ELEX 5043), Washington, D.C. 20360, by using the self-addressed Standardization Document Improvement Proposal (DD Form 1426) appearing at the end of this document or by letter.

FOREWORD

This document defines the interface standards for the automatic interchange of control and status (C&S) digital information in the shipboard Naval Telecommunications System (NTS). The standard is intended to provide guidelines for the design and acquisition of equipments, systems, software and firmware related to the U.S. Navy's automated communications systems. Physical, functional, and electrical characteristics are addressed.

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APPENDIX

1. SCOPE

1.1 Purpose. The purpose of this document is to define bus interface standards for the automatic interchange of control and status information for shipboard use.

1.2 Scope. This standard establishes the physical, functional, electrical and optical interface requirements for the automatic interchange of control and status information for shipboard use.

a. Where supervision or signaling or supervision and signaling (S/S) information is transferred (in-band or out of band) on a traffic circuit, the traffic standards shall govern and the S/S information shall be retrieved (and conditioned as necessary) from the control and status (C&S) word by applique items (or circuitry) not presently within the scope of this document.
b. This document is not concerned with operational traffic signal samples utilized with communication performance assessment (CPA). However, status decisions provided by built-in test equipment (BITE) concerning the quality of these traffic signals shall be considered as C&S information, and is within the scope of this document.
c. Semi-automatic (and remote) control schemes are currently in extensive use aboard U.S. Navy ships. Existing Naval telecommunication system (NTS) ships equipped with these semi-automatic schemes may require appliques to provide adaptation to the standard defined herein.

1.3 Data interface classification. For the purpose of implementing this document, certain interface classifications shall apply. Summary definitions of each classification are included in 1.3.1 and 1.3.2.

1.3.1 Type B-Naval tactical data system (NTDS) fast (MIL-STD-1397). Full duplex parallel data transfer of up to 250.000 words (four byte words) per second on each cable. Binary voltage level differentials of 0 volt, direct current (VDC) (logical 1) and minus 3 VDC (logical 0). Separate input and output cables and connectors.

1.3.2 Multiplex serial (MIL-STD-1553). Half duplex, command or response or both (C/R) asynchronous data bus utilizing a single, balanced transmission line (shielded wire pair) for transfer of self-clocking input or output or input and output (I/O) data in serial (PCM) format at a clock frequency of one megahertz (MHz). Logic level, at transmitter connection to transmission line is between 3 and 10 peak volts, plus or minus. Sixteen bits (2 bites) per word variable length messages (with a 20-bit frame length) but with a maximum of 32 data words in any one message block on a data bus. Up to 32 remote terminal (RT) primary addresses on any one data bus. Alternating current (AC)-coupled operation on a single (common) cable and special connector. Utilizes a direct current (DC)-isolation pulse transformer for each I/O transfer point and for each bus stud of over one foot in length. Total cable length is limited to less than 91.5 meters (m) (300 feet (ft)).

1.4 Implementation. FIGURE 1 shows the general relationship between the implementation levels as defined below.

a. Level 1. This level concerns only equipments that contain built-in interfaces which are capable of operating with the C&S bus system.
b. Level 2. This level concerns equipments that require an applique to interface with the C&S bus system.

1.5 Specific interface formatting requirements. This document outlines the general formats to be used for command words, data words and status words. Specific bit assignments are not made in an effort to allow design flexibility. It is envisioned that standard words will be developed for each equipment type and will be contained in each equipment specification. These specific command, data and status word bit assignments shall be requested from the Naval Electronic Systems Command (NAVELEX), which will coordinate the word uses. The Appendix provides a brief example outlining how the individual bits of a command word may be assigned to perform required functions.

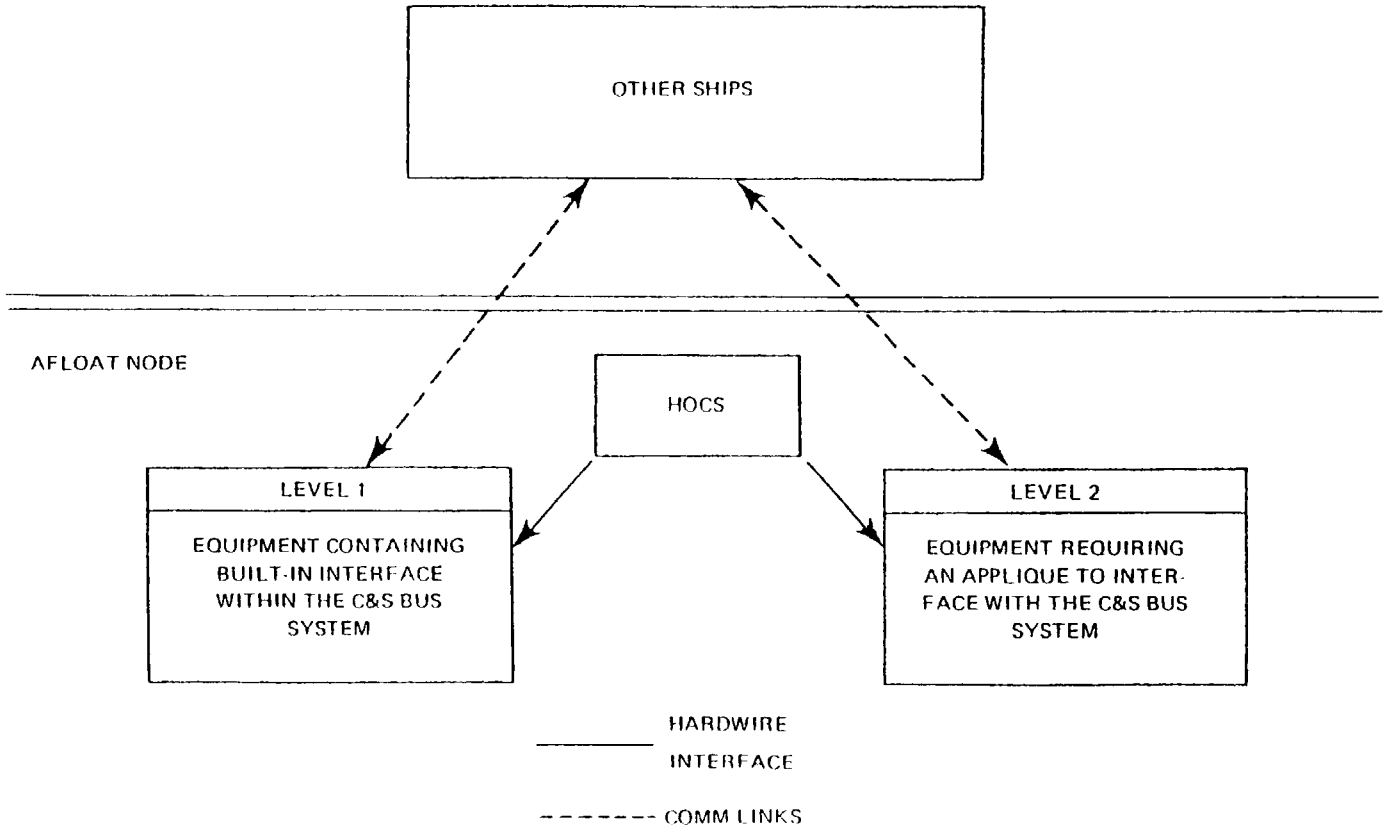


FIGURE 1. NTS control and status interface levels.

2. REFERENCED DOCUMENTS

2.1 Government documents. The following documents, of the issue listed in the Department of Defense Index of Specifications and Standards (DoDISS) and its supplements, form a part of this document to the extent specified herein. The date of the applicable DoDISS and supplements thereto shall be as specified in the solicitation.

SPECIFICATIONS

MILITARY

MIL-C-17/45D	Cable, Radio Frequency, Flexible, Twin, 78 Ohms, M17/045-RG108
MIL-C-915/63(SH)	Cable, Electrical, 300 Volts, Type 2U
MIL-E-6051	Electromagnetic Compatibility Requirements, Systems
MIL-T-21038	Transformer, Pulse, Low Power, General Specification For
MIL-C-28830	Cable, Radio Frequency, Coaxial, Semirigid, Corrugated Outer Conductor, General Specification For
MIL-C-28840	Connector, Electrical, Circular Threaded, High Density, High Shock Shipboard, Class D
MIL-C-39012/83	Connector, Coaxial, Radio Frequency Series Sma(Cabled Receptacle, Socket, Jam Nut Mounted, Class 2, Semirigid Cable)
MIL-C-39012/84	Connector, Coaxial, Radio Frequency Series Qsc (Cabled-Plugs, Pin Contact, Right Angle, Class 2)

STANDARDS

MILITARY

MIL-STD-188-100	Common Long Haul And Tactical Communication System Standards
MIL-STD-188-114	Electrical Characteristics Of Digital Interface Circuits
MIL-STD-188-120	Military Communication System Standards, Terms And Definitions
MIL-STD-461	Electromagnetic Emission And Susceptibility Requirements For The Control Of Electromagnetic Interference
MIL-STD-462	Electromagnetic Interface Characteristics, Measurement Of
MIL-STD-1309	Definition Of Terms For Test, Measurement And Diagnostic Equipment
MIL-STD-1310	Shipboard Bonding, Grounding, And Other Techniques For Electromagnetic Compatibility And Safety
MIL-STD-1397	Input/Output Interfaces, Standard Digital Data, Navy Systems
MIL-STD-1399, Sec. 406	Interface Standard For Shipboard Systems, Digital Computer Grounding
MIL-STD-1553	Aircraft Internal Time Division Command/Response Multiplex Data Bus
MIL-STD-1680	Installation Criteria For Shipboard Secure Electrical Information Processing Systems (U)
MIL-STD-1698	Insert Arrangements For MIL-C-28840(EC), High Density High Shock Circular Electrical Connectors

MS-3400	Connector, Receptacle, Electrical, Wall Mounting, Front Release, Crimp Contact, AN Type
MS-3406	Connector, Plug, Electric, Front Release, Crimp Contact, AN Type

PUBLICATIONS

DOA Technical Manual TM 11-486-11	Electrical Communications Systems Engineering: Definitions And Abbreviations
AF Manual Administrative Practices AFM 11-1, Volume III	Communications-Electronics Terminology

(Copies of specifications, standards, drawings, and publications required by contractors in connection with specific procurement functions should be obtained from the procuring activity as directed by the contracting officer.)

2.2 Other publications. The following documents form a part of this standard to the extent specified herein. Unless otherwise indicated, the issue in effect on date of invitation for bids or request for proposal shall apply.

Institute of Electrical and Electronic Engineers 488-1975	IEEE Standard Digital Interface For Programmable Instrumentation

(Application for copies should be addressed to the Institute of Electrical and Electronics Engineers, 345 East 47th Street, New York, N.Y. 10017.)

(Technical society and technical association specifications and standards are generally available for reference from libraries. They are also distributed among technical groups and using Federal agencies.)

3. DEFINITIONS

3.1 Introduction. For the purpose of implementing this document, certain general terminology and definitions shall apply. Except where otherwise specifically invoked in this document, they have been adapted from MIL-STD-188-120, MIL-STD-1397, MIL-STD-188-114, MIL-STD-1553, and IEEE STD-488-1975. This glossary has sufficient scope to encompass most interfaces to be defined by this document. Additional applicable definitions may be obtained by referencing MIL-STD-1309, AFM 11-1 (Volume III) and TM 11-486-11.

3.2 Definitions.

3.2.1 Asynchronous data transmission channel. A data channel utilizing digital modulation (or demodulation) in such a way that for the time interval separating any two significant instants in the same message, there is always an integral number of unit intervals, However, between two significant instants located in different messages, there is not always an integral number of unit intervals.

3.2.2 Back-to-back (loop) bit error rate (BER). This BER is defined as follows: The bus controller transmits 32 data words to a given RT and the RT responds with a status word indicating no message errors. The bus controller then commands the RT to transmit the same 32 data words which it previously received. Upon receipt of a valid response from the RT, the controller then compares each data word which it sent to the RT with each corresponding one it received back from the RT. The 16 bits in each word pair are compared and if any bit does not match, this is considered to be a bit error (loop) which was not detected within the system. This process must be repeated until statistically significant data are accumulated. For the system (including transmission lines and noise environment), the confidence level must be at least 99.99 percent. The total number of data bits transmitted during a specific time period are counted. The BER is then defined as the number of bit errors, divided by the total number of bits transmitted.

The BER is then defined as the number of bit errors, divided by the total number of bits transmittted.

3.2.3 Baud. This is the name given to a unit of modulation rate. One baud corresponds to a rate of one unit interval per second. The modulation rate is expressed as the reciprocal of the duration in seconds of the unit interval. The expression bit rate is sometimes erroneously substituted for this word. See Rate, Data Signaling and Effective speed of transmission.

3.2.4 Bit. A contraction of the term binary digit: may be either zero or one and is equal to one binary decision or the designation of one of two possible values or states of anything used to store or convey information.

3.2.5 Bit, erroneous. A bit that is not in accordance with that which should have been received.

3.2.6 Bit error rate (BER). The number of incorrect or erroneous bits divided by the total number (correct plus incorrect bits) over some stipulated (and statistically significant) period of time. The BERs expressed herein are given as a number in 10^n (for example, 2.5×10^{-5}). Several different kinds of BER are recognized herein (see Detected BER, Undetected BER).

3.2.7 Bit(s), framing. A bit, group of bits, or group of bit-intervals utilized to denote the beginning or end of the information field contained within a block. For the high order control system (HOCS) standard interface-bus system, the sync waveforms (at the beginning of each word, in a command or response message) have a time duration equal to 3 bit-intervals and serve the additional role of framing (to denote the beginning of each word). The parity-bit at the end of the block (information field) serves the additional role of framing (to denote the end of each word).

3.2.8 Bit, parallel. Refers to a set of concurrent data bits present on a like number of signal lines (with return line, or lines) which signal lines are used to carry information. Bit-parallel data bits may be acted upon concurrently as a group (byte) or independently as individual data bits.

3.2.9 Bit, parity. A bit associated with a character or block for the purpose of checking the absence of error within the character or block; may be the same as, or part of, a check digit which is used for checking purposes but which is otherwise redundant.

3.2.10 Bit, service. An overhead bit which is not a parity bit (for example, request for repetition, message length identification, and so forth).

3.2.11 Block. A group of bits, or binary digits, transmitted as a unit over which an encoding procedure is generally applied (for error detection purposes).

3.2.12 Block, erroneous. A block in which there are one or more erroneous bits.

3.2.13 Channel. The term channel (used by itself) may signify either a one-way (unidirectional) path providing transmission in one direction only or a two-way (bidirectional) path providing transmission in both directions (alternate or simultaneously). The term channel must be used with modifiers (words or phases) which classify the type of channel (for example, one way only, half duplex or duplex) as defined herein. The word path as used herein is to be interpreted in a broad sense to include separation (from other paths) by frequency or time division. Unless otherwise stated, however, the separation is considered to be accomplished by the usage of separate wire(s) or line(s) for each path. The term channel, as used herein, includes the intervening data-signal conversion equipment as well as the transmission media. Channels must be further defined as input channels or output channels or both (I/O).

3.2.14 Code. A system of rules and conventions according to which the data signal within a block is formed, transmitted, received and processed.

3.2.15 Command or response data bus. As used in this document, all RTs listen-to (receive transmission from) the controller but respond (transmit or talk) and take implementing action only

when specifically addressed by the bus-controller. Broadcast operation is not possible in this mode. Two one-way only (unidirectional) channels are used in this system. The output channel carries transmissions from the bus-controller to the RT and the input channel carries the transmission from the selected (addressed) RT to the bus-controller. Talker/listener interchanges are accomplished in a time-sequential time division multiplex (TDM) manner. The bus-controller is constrained from issuing a command to a given RT while simultaneously receiving the answer to a query issued earlier to another RT, on the same bus.

3.2.16 Compatibility. The degree to which devices may be interconnected and used (without internal modification or without use of external adaptors or appliques).

3.2.17 Controller. The controller shall be a unit that is either programmable or controlled by a processor and that serves the function of commanding, scanning and monitoring bus traffic.

3.2.18 Data processing system (DPS). A general purpose digital data processing capability which includes one or more processing unit(s), program storage, scratch pad memory, I/O controller(s) and a quantity of asynchronous I/O channels. For this standard, the DPS shall utilize a basic word length (information field) of 16 bits. The DPS shall also have a real time clock (RTC) and a monitor clock which operates either from an internal oscillator or from an external (or master) RTC input.

3.2.19 Detected BER. For the purpose of this document, this value is the ratio of the number of received erroneous but detected bits to the total number of bits transmitted. For the HOCS Standard interface system, erroneous bits detected by the RT will trigger (via a message error bit in the status word) an automatic request (ARQ) for retransmission.

3.2.20 Device, input-output (I/O). Any equipment which introduces data into or extracts data from a data communication system. As used herein, this definition encompasses computer I/O channels, bus-controllers, RTs and the I/O ports for the remote multiplexers.

3.2.21 Driver (line driver).

a. The electronic circuitry at the transmitting end (source) of an interchange circuit which transmits binary digital signals to a terminator via an interconnecting cable.
b. The transmitter (generator) of a binary digital signal.
c. The mechanism which enables a device to become a talker.

3.2.22 Duplex channel (full duplex channel). A primary or secondary channel capable of operating in both directions simultaneously. It permits simultaneous two-way conversations, message or information to be passed between any two given points. The term duplex (or full duplex) used to describe a primary channel does not imply anything about the type of secondary channel or the existence of a secondary channel; similarly, the use of the term to describe a secondary implies nothing about the type of primary channel present. (Note that a full duplex channel has the same signaling rate capability in both directions. Equipment with a common (shared) interface connector but which utilizes different signaling rates for input or output messages would be considered to possess a one way only primary channel in one direction and a one way only secondary channel in the opposite direction.)

3.2.23 Effective speed of transmission. The rate at which information is processed by a transmission facility and is expressed in terms of the average rate over some significant time interval. This quantity may be expressed as average bits per unit time. Rate of transmission, average is a more common usage.) For asynchronous operation, the ratio of this value to the data signaling rate will approach 50 percent under ideal conditions.

3.2.24 Error-detecting and feedback system. Sometimes known as decision feedback system, request repeat system, or ARQ system. A system employing an error-detecting code and is so arranged that a signal detected as being in error automatically initiates a request for retransmission (of the signal detected as being in error). For the interface systems identified in this document, the message error (ME) bit in the status word response (from the RT) represents the trigger for ARQ purposes.

3.2.25 External function (EF) data. Where utilized, the EF is part of the handshake cycle (protocol) applicable to the transfer of command instructions from the transmitting computer or bus-controller to an RT or other receiving device. The word size and bit format of the EF data shall be as specified for the the particular type, category or combination thereof of interface type.

3.2.26 Half duplex channel. A primary or secondary channel capable of operating in both directions on a bidirectional path but not simultaneously. The direction of transmission is reversible. The term half duplex used to describe a primary channel does not imply anything about the type of existence of a secondary channel; similarly, the use of the term to describe a secondary channel implies nothing about the type of primary present. (Note that, as defined herein, both directions of a half duplex channel have the same signaling rate capability.)

3.2.27 High-state. The relatively more positive signal level used to assert a specific message content associated with one of two binary logic states.

3.2.28 HOCS. High order control system. A control system which has complete responsiblity for control of the equipment on the bus.

3.2.29 Input. Input to the computer except where specifically stated as input to a bus-controller or as input to an RT.

3.2.30 Instants, significant. The instants at which significant conditions or states (recognized by the appropriate device) of the modulation or restitution begin. Each of these instants is determined as soon as the appropriate device takes up the significant condition usable for processing.

3.2.31 Interval, significant. Time interval between two consecutive significant instants.

3.2.32 Interval, unit. In a system using an equal-length code or in a system using isochronous modulation (demodulation), that interval of time such that the theoretical durations of the significant intervals of telegraph (data) modulation are all whole multiples of the interval.

3.2.33 Isochronous data transmission. The process utilizing digital modulation (or demodulation) in which the time interval separating any two significant instants is theoretically equal to the unit interval, or multiple thereof.

3.2.34 Low state. The relatively less positive voltage level used to assert a specific message content associated with one of two binary logic states.

3.2.35 Manchester II, biphase level. A data format resulting from an encoding technique which is accomplished by Exclusive OR addition of data clock to the unipolar non-return-to-zero (NRZ) data (binary information) signal. In the coded (composite) signal on the buses, each valid data bit interval is divided into two nominally equal half-intervals: in the first-half interval, the base band signal (NRZ data) is transmitted; and in the second half-interval, the complement of the baseband signal (NRZ data) is transmitted. The number of pulses per unit time, the pulse duration and the spacing between pulses (referring to the bus signals) all depend on the NRZ data. These factors, plus the sync waveforms make terms such as modulation rate, and data signaling rate not applicable.

3.2.36 Message. A transmission (with information in a suitable language) from a source to one or more destinations. For the purposes of the HOCS standard interface, a bus message is a transmission of words on the data bus cable (input or output). There are two types of bus messages: (a) bus-controller to RT; (b) RT to bus-controller. These two are known as command message and response message, respectively. Either type contains a block of words ranging in size from a minimum of one word to a maximum of 33 words. As a minimum, the command message contains a command word which may serve as the preamble to a longer message. Similarly, the response message contains at least a status word which also may serve as a preamble and, additionally, always serves as an acknowledgement of the command or as a trigger for ARQ purposes. The remainder of the bus message may consist of data words (up to a maximum of 32). A bus message transaction is complete when the command word, data word(s) and the status word have been transmitted.

3.2.37 Multiplex. Use of a command channel in such a way as to make two or more channels. This action may be implemented by the splitting of the frequency band (allotted to the common channel) into narrower bands, each of which is used to constitute a distinct and continuous channel. This approach provides a number of parallel channels and is known as FDM. Alternatively, the common channel may be allotted in timed sequence to different combinations of users. This approach provides intermittent (but interleaved) channels and is known as time-division multiplex (TDM). During a given time interval, the entire common channel bandwidth can be used by the individual TDM channel to which it is assigned. For the purpose of this document, the TDM schemes utilize composite pulse trains which are formed by interleaving the pulse trains of the individual channels. Also for the purpose of this document, the individual pulse trains will be modulated in a digital manner. Certain of the TDM interface systems identified herein convert digital data existing virtually simultaneously on a number of parallel digital channels into serial format and vice versa. The short hand notation for the multiplex device is Mux. The device utilized to recover the original individual pulse trains may also be known as mux, particularly if it is packaged with a parallel-to-serial converter. The term de-mux, although not universally recognized, also may be used for the recovery function. For the TDM systems identified herein, the RTs are active only when specifically addressed. Consequently the bus-controller is the only device possessing a simultaneous mux and de-mux capability encompassing all channels.

3.2.38 NODE. Refers to Naval platforms and shore-based communication stations.

3.2.39 NTDS. Navy tactical data system.

3.2.40 One-way channel BER. The ratio of the number of erroneous bits received to the total number of bits transmitted. The erroneous bits may be generated in the transmitting or receiving electronics (or both) or may result from noise injected via the transmission media (for example, cables, connectors) as a result of ambient EMI, or as a result of excessive signal-line attenuation. This ratio is expressed at the 99 percent confidence level, unless otherwise specified.

3.2.41 One way only (unidirectional) channels. A primary or secondary channel capable of operation in only one direction. The direction is fixed (by firmware) and cannot be reversed. The term one way only used to describe a primary channel does not imply anything about the type of secondary channel or the existence of a secondary channel; similarly, the use of the term to describe a secondary channel implies nothing about the type of primary channel present.

3.2.42 Output. Output from the computer except where specifically stated as output from a bus-controller or as output from an RT.

3.2.43 PCM multiplex system. The form of a TDM system in which a series of coded binary pulses, said series corresponding to discrete information, is transmitted for each of the data channels being serially multiplexed as a function of time.

3.2.44 Pulse code modulation (PCM). That form of modulation in which the modulating signal is coded so that each sampled element of information consists of different kinds or numbers of pulses and spaces.

3.2.45 Rate, data signaling. This quantity is expressed in bits-per-second (bps) and only for a single but serial binary transmission channel is numerically equal to the modulation rate (in baud). This statement is further conditioned on the basis that all pulses occupy the complete unit interval. Modulation rate and data signaling rate are not numerically equal if M-ary signaling is used over the transmission media. They also are not numerically equal if parallel transmission is provided for the data.

3.2.46 Remote multiplexer (RM). This terminology identifies a shipboard data multiplex system (SDMS) RT which has multiplexing capability so that it is capable of accessing up to 64 colocated devices via its various I/O ports.

3.2.47 Remote terminal (RT). The remote terminal is the electronic apparatus (located at a position remote from the controlling computer's I/O channel and interfacing bus-controller) necessary to provide the control and status (C&S) interface for the remotely-located equipment,

group or subsystem. These electronics may exist as a standardized and separate line replaceable unit (LRU) or may be customized and contained within the remotely-located equipment, group or subsystem. In the latter cases, the RT will contain any required circuitry.

3.2.48 Signal. The physical representation which conveys data from one point to another. (Note: For the purpose of this document, this is a restricted definition of what is often called signal in a more general sense. The term hereinafter is to be considered as referring to digital electrical signals, unless otherwise specifically identified. Such signals are nominally discontinuous and change from one state or polarity to another in discrete steps and in response to outputs from computers, teletypewriters, and so forth).

3.2.49 Signal conversion equipment. Those portions of the interface system equipments which transform (for example, modulate, shape, and so forth) the data signals to be exchanged across the interface into signals suitable for transmission through the associated communication media or which transform (for example, demodulate, slice, regenerate, and so forth) the received signals into data signals suitable for presentation to the data terminal equipment (that is, controller or RT).

3.2.50 Signal element. Each of the parts constitute a telegraph or data signal and distinguished from the other parts by its nature, magnitude, duration, and relative position (or by one or some of these features only).

3.2.51 Signal level. The magnitude of a signal when considered in relation to an arbitrary reference magnitude (voltage in the case of this document). Logical high and low states are defined in terms of nominal signal levels (with tolerances and switching or transition dead zones) specified for the various types of interfaces.

3.2.52 Signal line. One of a set of signal conductors in an interface system used to transfer messages among interconnected devices. A signal line is part of an interchange circuit used for the purpose of exchanging data, interface management protocol or timing signals. It is necessary to be explicit about the signal return (for example, common, signal ground, part of balanced pair) when discussing a given digital interface.

3.2.53 Signal parameter. That parameter of an electrical quantity whose values (or sequence of values) convey information.

3.2.54 Signal transition. The change from one signaling condition to another; for example, the change from the logical one level to the logical zero level or vice versa.

3.2.55 Start-stop data transmission channel. A data channel (either synchronous or asychronous) for which the information transfers occur in bursts. These bursts correspond to words, or messages, as applicable. The information bursts are delimited by the conventions, or protocol, established for the given type of channel. For the HOCS standard interface bus system, the delimiting is included partially in the structure of the bursts (for example, sync waveforms, parity bits) and partially in the protocol establishing the minimum and maximum message lengths and the number of words to be contained in a specific message.

3.2.56 Synchronous data transmission channel. The process such that between any two significant instants in the overall bit stream, there is always an integral number of unit intervals. A synchronous data channel will not accommodate start or stop data signals unless they are transmitted isochronously and unless timing signals (data clock) accompany the data transfer. Timing signals (data clock) accompany the data transfer between the controller and RT.

3.2.57 Terminator (line terminator).

a. The electronic circuitry at the receiving end (sink) of an interchange circuit and which receives binary digital signals from a driver (via an interconnecting cable).
b. The receiver (input amplifier) of a binary digital signal transmitted via an interchange circuit.

c. A load (power sink) at the far end of an interchange ciruit.
d. The mechanism which enables a device to become a listener.

3.2.58 Undetected BER. This value is also known as residual bit error rate and represents the ratio of erroneous bits (erroneously received but undetected) to the total number of bits transmitted. The value is proportional to the received erroneous bits which are not recognized by the error checking (or detection) process. Consequently, they cannot trigger a request for retransmission.

3.2.59 Word. A group of bits which is treated as a unit and transferred as such. Although a given word may contain characters (to some standard such as ASCII), it is not required that the word be so constructed. The word may consist of all individually evaluated bits plus one or more bytes with sizes ranging from three to either eight or more bits. For the HOCS Standard interface-bus system, the word size shall be 16 bits. When the expression word is used in connection with the signals on the bus(es) of this system, it shall connote a transmission interval corresponding to an information field of 16 bits preceded by a sync waveform and followed by a parity-bit. That is, a word on the bus shall require a transmission time equal to 20 bit-intervals.

4. GENERAL REQUIREMENTS

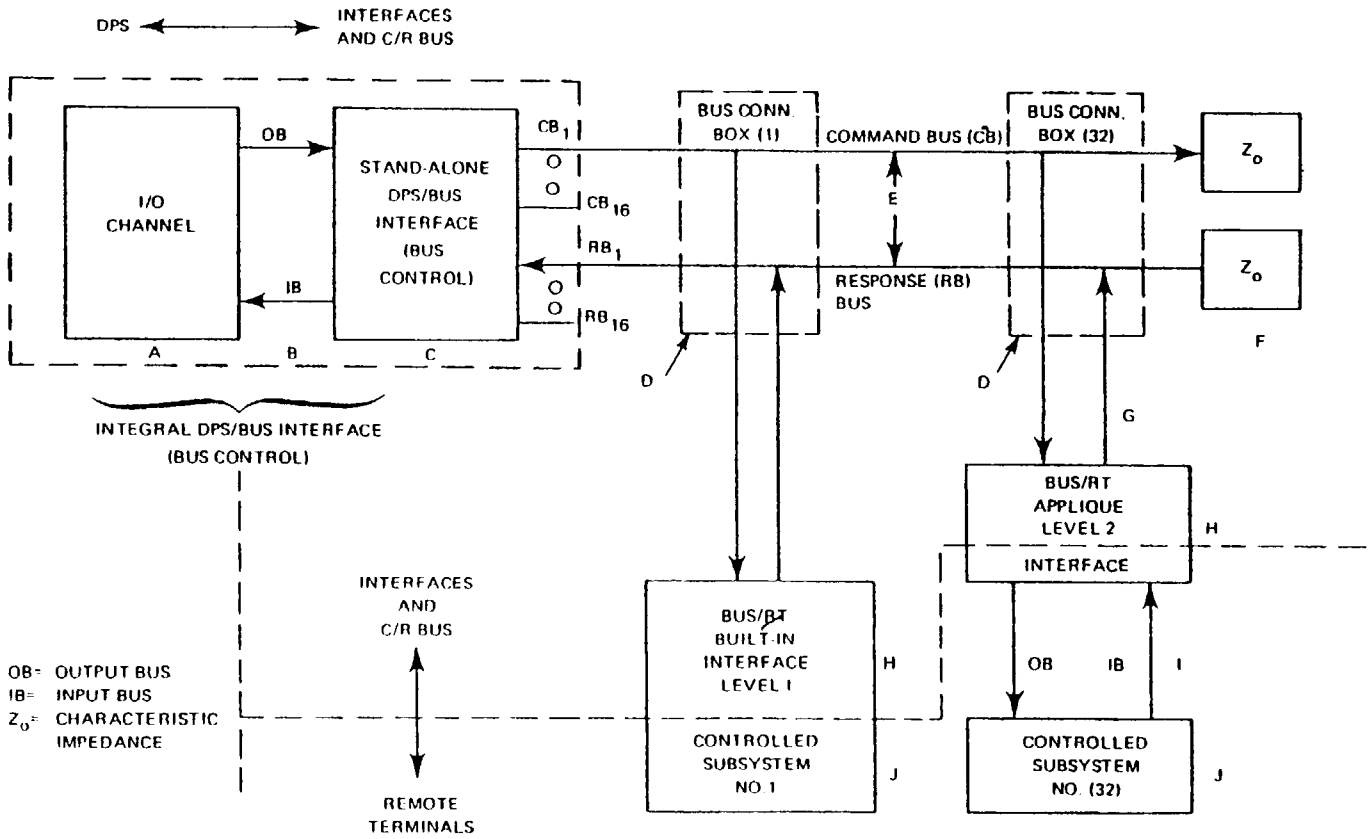
4.1 Introduction. This NTS Interface Standard establishes certain Higher Order Control System (HOCS) requirements in terms of electrical, functional, and physical characteristics supportive of automated control and status information interchanges between the HOCS data processing system (DPS) and RTs, such as binary-controlled switches, transmitters and receivers. This interface standard encompasses the various circuits, the C/R buses, bus connection boxes and connectors as depicted in FIGURE 2. Also as depicted, the bus controller implementation may be either stand alone or an integral I/O capability for the HOCS DPS. The block diagram can be divided into the following subsections:

a. The interface between an I/O channel of the HOCS DPS (equipment A), the cables B and the DPS side of a stand-alone bus-controller (equipment C).
b. The interface between the bus-controller, either stand-alone (equipment C) or integral to the DPS (equipments A plus C), and the C/R buses (cables E).
c. The unidirectional buses (named command bus and response bus respectively), shown as cables E, and the end terminating impedances F.
d. The branches between the C/R buses E, and the RTs (equipment J), via the bus connection box D, cables G and the interface between the bus and the RT (bus/RT interface) (equipment H). If the bus/RT interface circuit cannot be built into the controlled subsystem J, then cables I are required to connect them.

4.2 Standard bus interface system. The relationship of the standard bus system with respect to the HOCS DPS and the RTs to be controlled by the DPS is illustrated in FIGURE 2. The bus system shall include the following major sections:

a. In the case where a stand-alone bus controller is utilized, the interface circuit and cables between the HOCS DPS and a stand-alone bus controller. The requirements of the type B (Navy tactical data system (NTDS) fast) interface, as specified in MIL-STD-1397, shall be applied to this section.
b. The interface between the bus controller (either stand-alone or integral to the DPS) and the C/R buses. The relevant requirements are set forth in sections 5.2 and 5.3.
c. The C/R buses and their terminations.
d. The interface circuit and cables between the C/R buses and the RTs as specified in sections 5.1, 5.2 and 5.3. If the bus/RT interface circuit cannot be built into the RT, the additional cables between the interface circuit and the RT shall be as specified in the applicable equipment interface specification.

4.3 C/R buses.



NOTE: DASHED LINE DENOTES THE BOUNDARY WHERE THIS STANDARD APPLIES.

FIGURE 2. Block diagram of interfaces and C/R bus.

4.3.1 Data bus operation. The multiplex data bus system in its most elemental configuration shall operate as shown in FIGURE 2. The system shall provide two start-stop channels (unidirectional) and shall function in a C/R mode. Sole control of information transmission on the bus shall reside with the bus controller, which shall initiate all transmission. The information flow on the bus shall be comprised of message blocks which are, in turn, formed by three types of words (command, data and status) (see 5.1.3.2). All elements of the bus system including the transmission cable, RTs and controller shall conform to the electromagnetic interference (EMI) requirements specified in MIL-STD-461 and the electromagnetic compatibility (EMC) requirements of MIL-E-6051. The bus system defined herein shall be considered BLACK within the context of MIL-STD-1680.

4.3.2 Information transfer modes. The bus system shall employ two modes of information transfer: (a) Bus controller to RT transfer, and (b) RT to controller transfer. These modes shall operate as specified in 5.1.3.1 through 5.1.3.1.4. Information is transferred in serial form on the C/R buses for all modes.

4.3.3 Modulation rate. The information modulation rate shall be 1.0 million (M) baud for the burst-transmissions on the C/R bus in each mode of transmission. The direct timing shall be inherent in and may be derived (for receive purposes) from the bus signals.

4.3.4 RTs. Each bus controller (either integral to the DPS or stand-alone) shall provide the capability for addressing and communicating with up to maximum of 32 RTs via one each C/R bus for distances equal to or less than 243 m (800 ft) excluding stub lengths and without use of regenerative repeaters. When the NODE contains more than 32 RTs (for example, a combined total of up to 512 RTs, including programmable switches, modems, transmitters, couplers, receivers), the bus controller (either integral to the DPS or stand-alone) shall provide the management and circuit capability for the next higher level of multiplexing.

4.3.5 Long distance control. When equipment to be connected to the C/R bus is located in remote areas requiring cable runs in excess of 243 m (800 ft), a method for extending the effective length of the C/R bus must be employed. Two of the various options identified for extending the C&S interface from the HOCS DPS to equipment in remote communications areas are shown for guidance in FIGURE 3. One of the options is preferred for use on those facilities that do not have a Shipboard Data Multiplex System (SDMS). The other option is preferred for use on ships where the SDMS is available.

4.3.5.1 Non-SDMS facilities. This option utilizes a bus repeater to extend the standard C&S bus to remote communications areas where the distance between the bus controller and remote equipment exceeds 243 m (800 ft). Functionally, the bus repeater for the command bus generates the signals from the bus controller and transmits these signals on the bus extension to the remote communications area. The repeater for the response bus regenerates signals returned from the RTs and transmits these signals on the bus to the bus controller. The repeaters are functionally transparent to both the bus controller and the RTs; however, the bus repeater design shall be such as to add an integral equipment-propagation delay-time (in each direction) of greater than one-half and less than two data unit intervals (at the nominal modulation rate of 1.0 M baud). The two-way delay attributable to the bus repeater is directly additive to the gap shown in FIGURE 4 and specified in 5.2.3.5.1. Software design for the HOCS DPS must accommodate this addition to the response-delay. The bus repeater may be located at any convenient location between the central communications area and the remote communications area as long as either section of the bus does not exceed the maximum unrepeatered bus length of 243 m (800 ft).

4.3.5.2 SDMS equipped platforms. This option utilizes the SDMS to extend the C&S interface to remote ommunications areas of the ship. In the central communications area , the interface to SDMS is p ovided by a connection between an I/O channel of the HOCS DPS and the parallel I/O modules of an SDMS remote muliplexer (RM). This connection is implemented as a MIL-STD-1397 category B type 1 (16 bit) interface. The DPS functions as a computer and the SDMS RM functions as a peripheral for this interface. In the remote communications area, the interface to SDMS is provided by a connection betweeen parallel I/O modules of an SDMS RM and the parallel I/O port of a bus controller. This connection is implemented as a MIL-STD-1397 category B type 1 (16 bit) interface with the SDMS RM functioning as a computer. The bus controller used in the remote communications area shall comply with the requirements for the stand-alone bus controller option

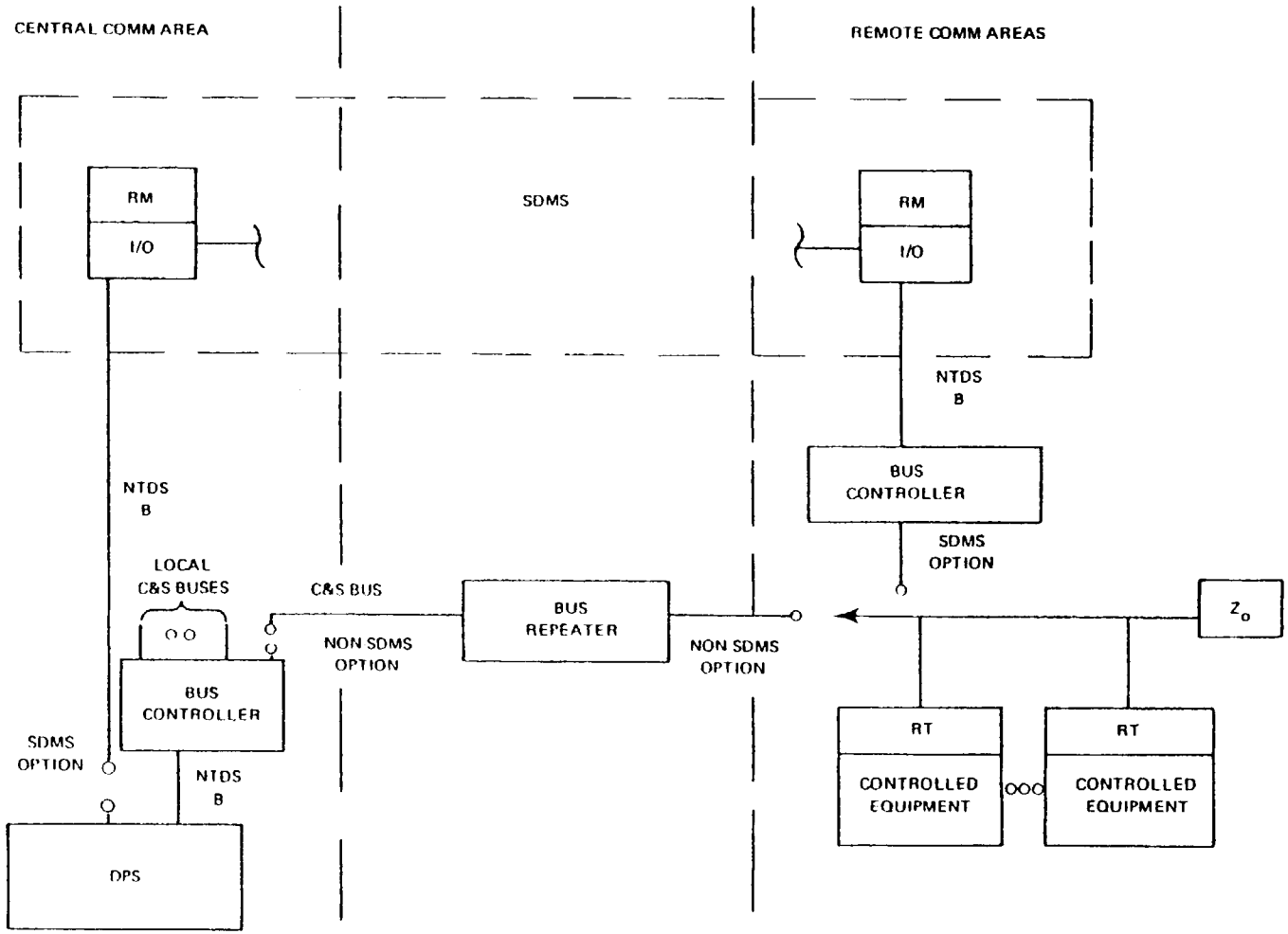
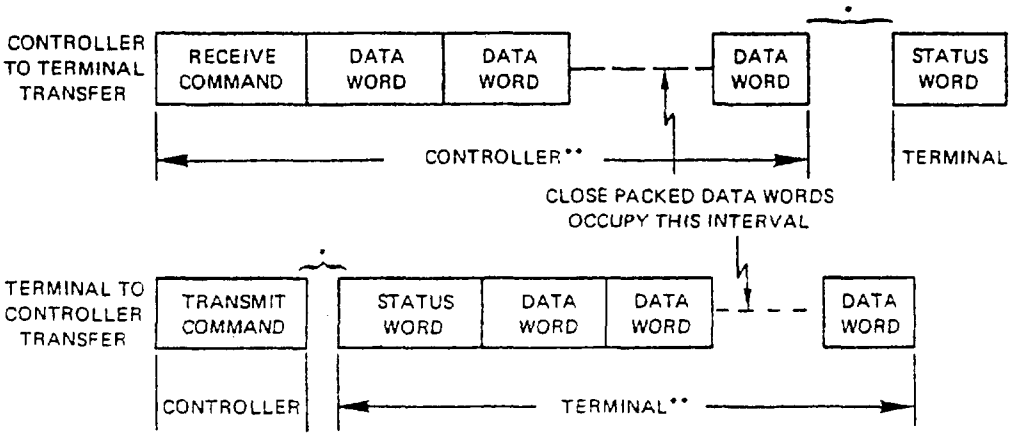


FIGURE 3. Extended bus options, block diagram.



*GAP AS SPECIFIED IN 5.2.3.5.1.

**MAXIMUM TRANSMISSION INTERVAL AS SPECIFIED IN 5.2.3.5.2

FIGURE 4. NTS interface standard message formats.

which may be used in the central communications area. It utilizes a standard C&S bus to communication with RTs in the remote communications area. Functionally, the use of SDMS in this option is transparent to RTs in the remote communications areas. From the HOCS viewpoint there are functional differences between the two options in message formats and response timing. The DPS must add to the standard C&S message formats the control words necessary to administer the HOCS-SDMS interface. Since the SDMS may be used to extend the C&S interface to more than one remote communications area, transmissions from the DPS to remote areas (via a local SDMS RM) must be preceded by two (SDMS interface) external function (EF) command words, which include the address of the RM in the desired remote area and the message length. The expected response times for receiving status replies from RTs must be changed in the HOCS when this option is used. In the usual C&S configuration (without repeater), the HOCS expects to receive a status reply from an RT within the time specified in 5.2.3.5.1. This interval is measured starting from the moment that the last bit in the command message is transmitted. When the SDMS option is used, the DPS must allocate additional time (for SDMS delay, which will not exceed one millisecond (ms)) to the wait for the status reply from any RT accessed via the SDMS. Although the bus controller in the remote communications area may be essentially the same as the optional stand-alone controller identified for the central communications area, its functions are altered slightly for interfacing with the DPS via the SDMS. When status messages are to be sent (via the SDMS) from the RTs to the DPS, the remotely located bus controller must precede the status message with an SDMS EF command word and must append on all ones word to the message.

5. DETAILED REQUIREMENTS

5.1 Functional requirements, standard bus system.

5.1.1 Bus system interface for the HOCS DPS. Two possible interface options are recognized herein for the bus controller function. In the first case, the function is absorbed into the DPS and is provided through (an) I/O channel(s) of the DPS. In the second case, the function is provided by a stand-alone bus controller which functions as a peripheral to the DPS. For this second case, information shall be transferred in parallel into and out of an I/O channel of the DPS as specified in MIL-STD-1397 for type B (NTDS fast) data interfaces. However, for both cases, information shall be transmitted and received from the C/R buses in serial, as specified in this standard. Therefore, the bus controller function shall include suitable provisions for parallel-serial and serial-parallel word format conversion.

5.1.2 Bus selection. As indicated in 4.3.4, C&S information interchanges with more than 32 RTs will require utilization of multiple sets of C/R buses. This expanded capability may be provided by use of multiple, bus-compatible, I/O channels in the DPS. Alternatively, where stand-alone bus controllers are utilized, it is preferred that the bus controllers provide a multiplexing function which allows multiple sets of C/R buses to be combined into a single NTDS fast I/O channel into the DPS. This multiplexing function for the stand-alone bus controller necessitates that a bus identifier accompany the C&S information interchanges between the bus controllers and the DPS. Thus for this latter case, the C/R messages traversing the MIL-STD-1397 type B (NTDS fast) interface shall contain additional words utilized or added by the stand-alone bus controller multiplexing function.

5.1.3 Detailed C/R buses requirements. These buses shall provide the transmission media for transferring the information between the bus controller and the remote terminals. The information includes instructions, data timing, alarms, and others required for automated control of remote terminals (by the DPS via the bus controller). The information on the buses shall be limited always to command or status word plus a maximum of 32 data words of the appropriate type.

5.1.3.1 Message formats. The messages transmitted on the C/R bus shall be in accordance with the formats shown in FIGURE 4. The maximum and minimum response times for the addressed RTs shall be as stated in 5.2.3.5.1.

5.1.3.1.1 Controller to RT transfers. The controller shall issue a receive command followed by a number of data words. The RT shall, after message validation, transmit a status word back to the controller. The command and data words shall be transmitted in a continuous fashion with no interword gaps. The formats of command, status, and data words shall be as specified in 5.1.3.2.

5.1.3.1.2 RT to controller transfers. The controller shall issue a transmit command to the RT. The RT shall, after command verification, transmit a status word back to the controller, followed by a number of data words. The status and data words shall be transmitted in a continuous fashion with no interword gaps.

5.1.3.1.3 Data form. Digital data before encoding shall be in unpopular non-return to zero (NRZ) form and shall be compatible with the message and word formats defined in this standard. Any unused bit position in a word shall be transmitted as logic zero.

5.1.3.1.4 Bit count. The number of bits required to define a quantity shall be the minimum consistent with the resolution or accuracy required.

5.1.3.2 Word formats on the bus.

5.1.3.2.1 Word size. The word size shall be 16 bits plus the sync waveform (3 bit times) and a parity bit for a total of 20 bit times as shown in FIGURE 5.

5.1.3.2.2 Command word. A command word shall be comprised of a sync waveform, address, T/R bit, command codes (as defined in the applicable equipment interface specification) and a parity bit (see FIGURE 5).

5.1.3.2.2.1 Command sync. The command sync waveform shall be an invalid Manchester waveform as shown on FIGURE 5. The width shall be three bit times, with the waveform being positive for the first one and one-half bit times, and then negative for the following one and one-half times. If the next bit following the sync is a logic zero, then the last half of the sync waveform will have an apparent width of two clock periods due to the Manchester encoding (see FIGURE 6 a).

5.1.3.2.2.2 Command RT address. The next five bit times following the sync shall provide for the RT address. This permits a maximum of 32 RTs to be attached to any one data bus. All ones shall indicate a decimal address of 31, and all zeroes shall indicate a decimal address of 32. The most significant bit of the address shall be transmitted first.

5.1.3.2.2.3 Transmit or receive or both (T/R). The next bit following the address shall be the T/R bit, which shall indicate the action required of the RT. A logic zero shall indicate the RT is to receive, and a logic one shall indicate the RT is to transmit.

5.1.3.2.2.4 Command codes. The next ten bits following the T/R bit shall be utilized for command codes. See the applicable equipment specification for details.

5.1.3.2.2.5 Command parity. The last bit in the word shall be used for parity over the preceding 16 bits. Odd parity shall be utilized.

5.1.3.2.3 Data word. A data word shall be comprised of a sync waveform, data bits, and a parity bit (see FIGURE 5).

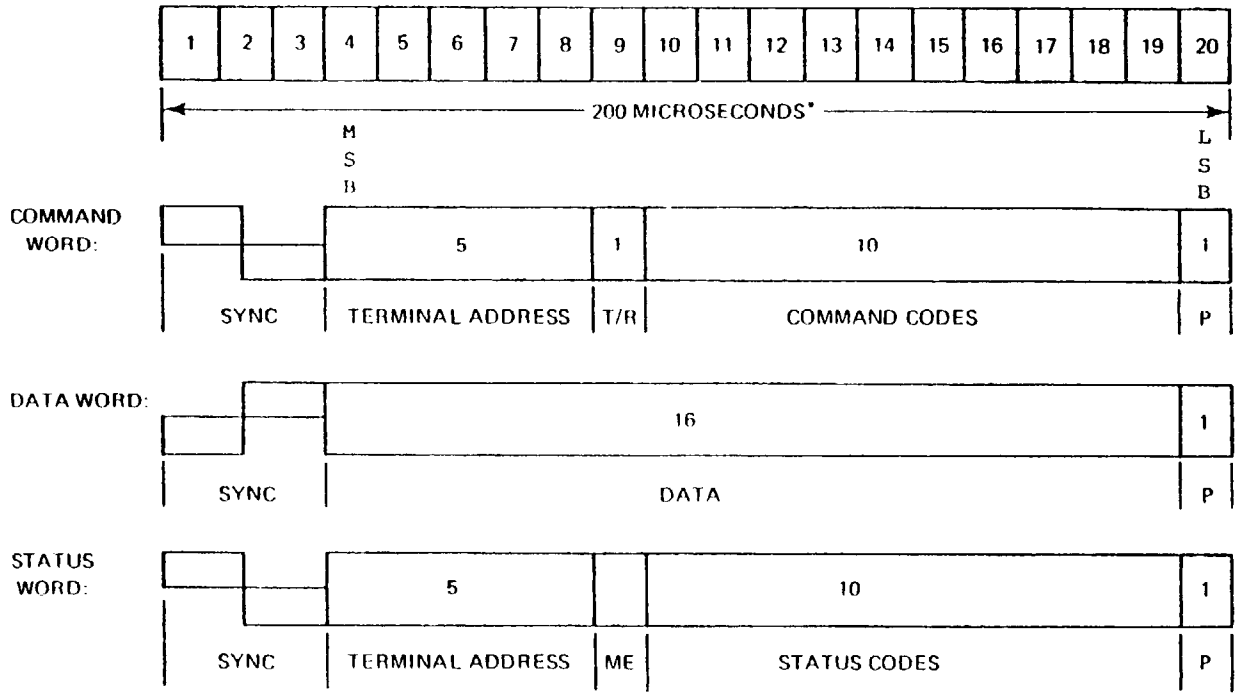
5.1.3.2.3.1 Data sync. The data sync waveform shall be an invalid Manchester waveform as shown on FIGURE 5. The width shall be three bit times, with the waveform being negative for the first one and one-half bit times, and then positive for the following one and one-half bit times. Note that if the bits preceding and following the sync are logic ones, then the apparent width of the sync waveforms will be increased to four bit times (see FIGURE 6 b).

5.1.3.2.3.2 Data. The 16 bits following the sync shall be utilized for data transmission as specified in 5,1.3.1.4.

5.1.3.2.3.3 Data parity. The last bit shall be utilized for parity over the preceding 16 bits. Odd parity shall be used.

5.1.3.2.4 Status word. A status word shall be comprised of a sync waveform, RT address, message error bit, status codes, and a parity bit (see FIGURE 5).

5.1.3.2.4.1 Status sync. The sync waveform shall be as specified for the command word.



*(20 BITS EACH 1 MICROSECOND LONG. SEE 4.3.3, 5.1.3.2 AND 5.2.2.3.7)

FIGURE 5. Word formats on the NTS standard bus.

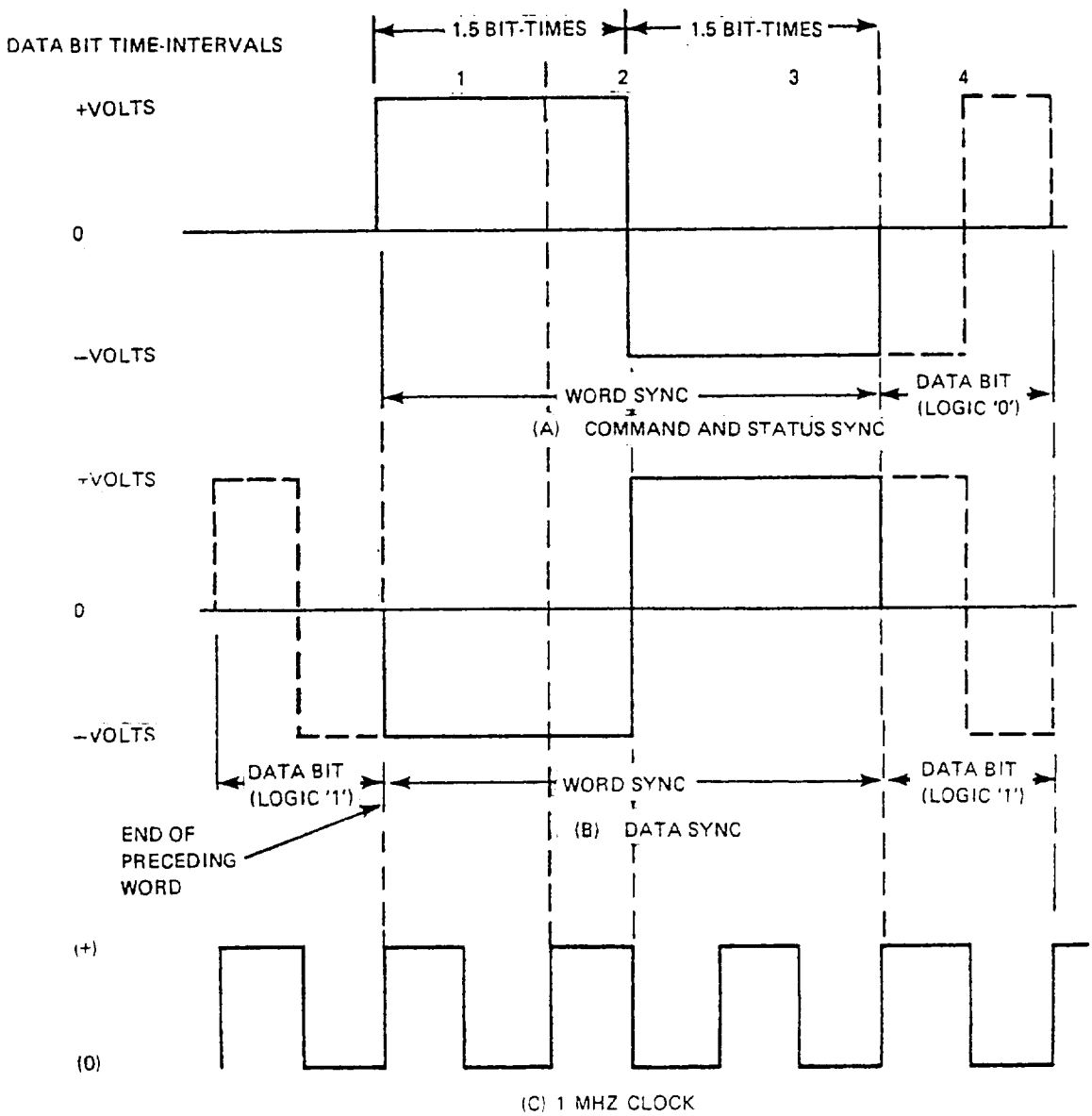


FIGURE 6. Bus signal wave forms for synchronization.

5.1.3.2.4.2 Status RT address. The next five bit times following the sync shall contain the address of the terminal which is transmitting the status word as defined in 5.1.3.2.2.2.

5.1.3.2.4.3 Message error. The first bit after the address shall be utilized to indicate that the preceding command message failed to pass the RT's validity tests. This error condition shall include parity errors. A logic one shall indicate the presence of a message error, and a logic zero its absence. A message error shall be indicated when the preceding command message to an RT has failed either the word or message validity criteria for the RT. The data validation criteria in 5.2.3.4.2 shall be used.

5.1.3.2.4.4 Status codes. The next ten bits following the message error bit shall be utilized indicating controller equipment status, as defined in the applicable equipment specification. All zeros shall indicate a normally functioning terminal, unless otherwise defined in the applicable equipment specification.

5.1.3.2.4.5 Status parity. The last bit shall be utilized for parity over the preceding 16 bits. Odd parity will be used.

5.1.4 C/R bus to RT interface. The RT shall provide the necessary electronics to interface between the C/R bus and the terminal itself. The bus side interface shall accommodate the standard biphase PCM signal as specified in paragraphs 5.2.3.3, 5.2.3.4, and 5.2.3.5. The terminal side interface shall have special provisions to satisfy the individual controller subsystem requirements. If this latter interface circuit is not built in the subsystems (for example, for subsystem standardization reasons), an independent applique (or adapter) and tie cables shall be provided. This latter interface shall be specified in the applicable equipment specification.

5.2 Electrical requirements, standard bus.

5.2.1 Bus controller. As identified in FIGURE 2 and more specifically in paragraphs 4.1, 4.2, 5.1.1 and 5.1.2 herein, the bus controller function may be implemented, either as an integral capability of the DPS or as a stand-alone capability. The use of ground cables and cabinet or enclosure grounds shall comply with MIL-STD-1399, Section 406 for the DPS-side of the stand-alone bus-controller interfaces. Futhermore, 5.1.1 and 5.1.2 identify alternate multiplexing possibilities for accommodating a large (more than 32) number of RTs. The stand-alone capability, utilized with the MIL-STD-1397 type B interface, requires utilization or generation of the address identification words required in the interface management function identified in 5.1.2. In addition to any management and multiplexing circuitry required, the following additional circuits (as a minimum) shall be included in the bus controller (those required only for a stand-alone capability are labeled SA).

a. Serial to parallel and parallel to serial converters. SA
b. Thirty-three word buffer registers, for each bus. SA
c. EMI protection for DPS per MIL-E-6051.
d. Mux and demux, for time-sequential transmission or reception or both of data (to or from each of up to 16 command buses and response buses). SA
e. Manchester II modems, including synchronization circuits.
f. Parity computing bit generating and detecting circuits.
g. AC coupling between the controller and the C/R buses.
h. System-clock generation and distribution provisions (as identified in 5.2.2.3.2).
i. Added circuitry, as necessary, to meet the following differential balanced bus requirements:
   (1) An input-port shall terminate one end of the relevant response-bus in its characteristic-impedance (Z_0), in order to minimize the effects of pulse reflections caused by the sub-connections.
   (2) An output-port shall terminate one end of the relevant command-bus in its characteristic-impedance (Z_0), in order to minimize pulse reflections caused by the stub-connections. In other words, the command-signal-generator shall have an internal-impedance equal to Z_0.
   (3) When terminated in a resistive load of magnitude equal to Z_0, the peak-signal output-voltage shall be plus or minus ($\pm$) 12$\pm$2 volts, line-to-line, measured at the output-port connections.

(4) The output-waveform shall meet the requirements of 5.2.2.3.7, when measured at the controller's output-port connections across a resistance equal in magnitude to Z_o. However, the rise and fall times shall not exceed .15 microseconds (μs).
(5) The receive-circuitry associated with an input-port shall equal or exceed, in performance, the requirements set forth in 5.2.3.4.1.1 except that the voltage shall be measured at the response-bus connections to the relevant input-port of the bus-controller.

5.2.2 C/R bus media.

5.2.2.1 Transmission media. Each bus shall utilize a cable that is electrically equivalent to RG-108 specified in MIL-C-17/45D. Each individual wire shall be terminated independently and via a connector-pin. Additionally, the shield-grounds shall be extended through (to bus and branch) and insulated from the bus connection box. The latter is identified as Item D in paragraph 4.1 (c) and FIGURE 2. The bus connection-box shall be grounded in accordance with MIL-STD-1399 (Navy), Section 406. Penetrations through secure perimeters (within the meaning of MIL-STD-1680) shall utilize shield-ground extensions as done for the bus connection-box, in addition to any metallic perimeter grounds required by MIL-STD-1680.

5.2.2.2 Terminating impedance. In addition to the termination provided at one end by the bus controller each bus shall be terminated at the far end in an impedance equal to the cable's characteristic or surge impedance of 78 ohms $\pm$3 ohms (measured at 1 MHz). See impedance Z_o in FIGURE 2.

5.2.2.3 Signal characteristics.

5.2.2.3.1 System clock, distribution and utilization. The bus controller, whether implemented as a stand-alone capability or integral to the DPS, shall provide the system (master) clock reference for the timing of all bus signals. The bus controller shall be capable of accepting and utilizing external clock signals for purposes of generating system clock. The frequency stability limit requirements for system clock (and hence the minimum requirements for external clock) shall be equal to or better that those set forth for the RT's internal clock in 5.2.2.3.2. Timing signals which are in phase with the clocking of the transmissions on the C/R bus shall be available (external to the bus controller) for distribution over the system clock bus. These timing signals shall be utilized for the timing control of any regenerative repeater utilized for long distance control as described in 4.3.5.1. These distributed timing signals may be utilized by the RT and its clock-driven circuitry associated with the received signal recovery and utilization at the RT. Similarly, these timing signals (with suitable phase shifts) may be utilized for transmit (response) logic circuitry and for the clocking of status information onto the response bus. For the transmit clock stabilities specified in 5.2.2.3.3, the receive-circuitry-performance (of the RT and controller) shall be such as to achieve synchronism as specified in 5.2.2.3.6 in less than 3 bit times and shall be such as to maintain synchronism, over the next 17 bit times, to within 0.2 percent of the clock unit interval. This synchronization performance shall be achieved over a range of input waveforms and levels identical to those of 5.2.3.4.1.1.

5.2.2.3.2 Receive clock. The signal shall be transferred (utilizing a direct data clock) over the data bus in serial digital format. The data clock shall have a cyclic frequency of 1.0 MHz (1,000,000 each alternate high and low states per second) with a duty cycle of 50$\pm$ 5 percent. One clock cycle shall represent two clock unit intervals, each with a duration equal to one-half the unit interval for the data being transferred. Consequently, the clock's modulation rate (in Baud) is two times that of the data. The Clock Equipment, Control and Timing paragraph and the designations of emissions and Bandwidth appendix of MIL-STD-188-100 illustrate clock-to-data relationships. For the NTS interface standard, CASE FIVE of the Standard Arrangements for Clock/Data Phase Relationships paragraph of MIL-STD-188-100 shall apply. The internal clock signal waveform, like the data signal waveform, is unipolar NRZ (see FIGURE 7). Furthermore, the transmit-clock signal is combined by Modulo 2 Addition (Exclusive OR) with the data signal and applied to the bus. Therefore, the clock is inherent in, and for the receive purpose may be derived from, the bus signal (see FIGURE 7). Receive clock for the RTs shall normally be derived

FIGURE 7. Data encoding.

from the system clock distributed by the bus controller. However, if the RT does not utilize system clock (because it contains an internal clock meeting the requirements set forth above) it shall derive receive clock from the command-message sync waveforms otherwise used only for start-of-word and message validation purposes. If the RT is provided as a separate applique, it shall make receive clock available (externally) for utilization by the applicable remotely controlled equipment group or subsystem.

5.2.2.3.3 Transmit clock. The general design objective for the RTs and the controller for each bus is such that the equipment has a capability of operating with external (master) clock control at the applicable modulation rate in the bit synchronous transmission mode. For this requirement, the character interval consists of 20 units. Furthermore, the controller design shall be such that it is capable of distributing clock (either the controller's internal or the external) to the RTs over another conductor in the same cable utilized for the command and response buses. For those RTs otherwise required to have an internal clock (for example, RTs with integral-processor) this general design objective may be waived provided the performance of the internal clock satisfies the additional clock requirements set forth herein. When clock is distributed to controller and RT receive circuitry, the sync waveforms still shall be retained for start-of-word and message validation purposes. The limit requirements for internal clock frequency-stability (and hence the minimum requirements for external clock) are as follows:

a. Long term (24 hour) ± 0.001 percent of nominal (that is, ± 10 Hz).
b. Short term (one-second), ± 0.0001 percent of nominal (that is, 1.0 Hz).
c. Character interval (20 μs) ± 0.00001 percent of clock unit interval (that is, 0.01 Hz).

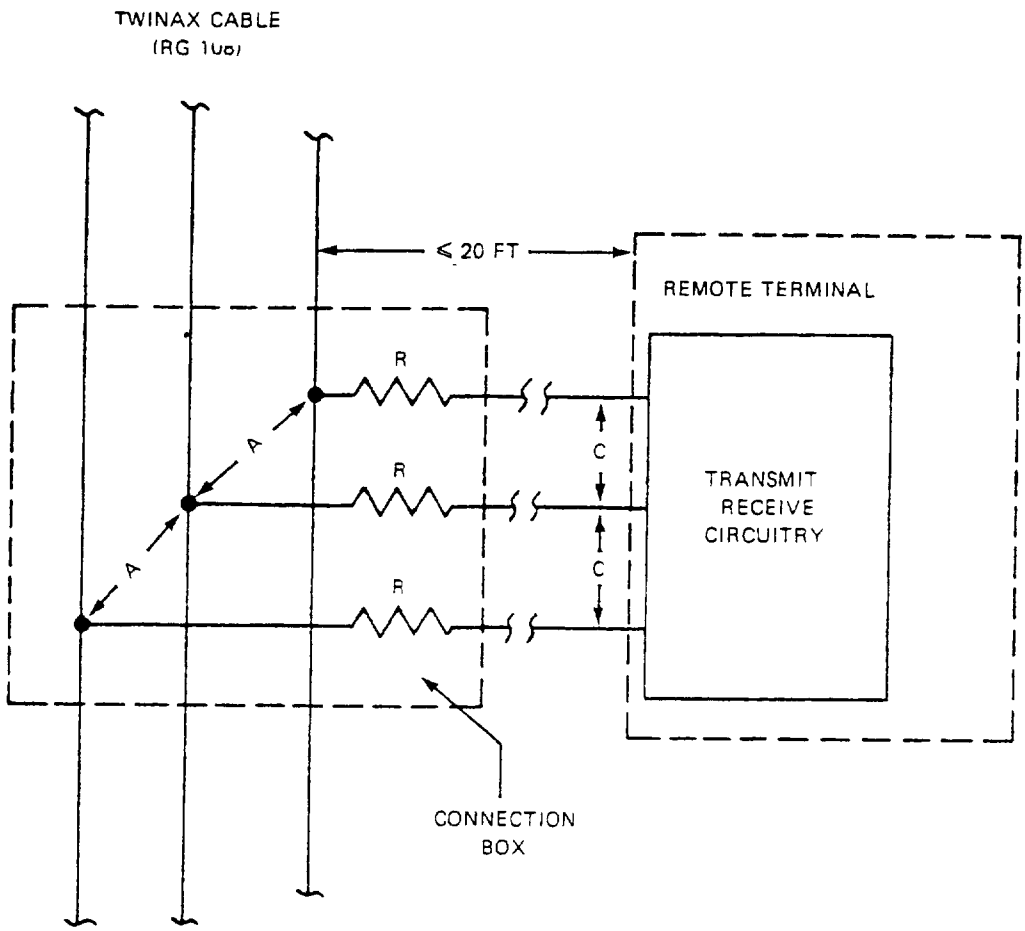
5.2.2.3.4 Data coding. Data shall be encoded so as to produce the form known as Manchester II, biphase level. A logic one shall be transmitted as a one to zero (1/0) transition (that is, a positive pulse followed by a negative pulse). A logic zero shall be transmitted as a zero to one (0/1) transition (that is, a negative pulse followed by a positive pulse). A transition through zero occurs at the midpoint of each data bit unit interval (see FIGURE 7).

5.2.2.3.5 Bus signaling. The maximum (instantaneous) signaling rate on the bus shall be 2.0 M pulses (alternative positive and negative states) per second corresponding to the clock modulation rate of 2.0 M Bauds. The corresponding maximum data bit rate is 1.0 M bps.

5.2.2.3.6 Sync. The data bus sync waveform is explained for command, data, and status words in paragraphs 5.1.3.2.2.1, 5.1.3.2.3.1, and 5.1.3.2.4.1, respectively. The applicable waveforms are shown in FIGURE 6. Increased detail is provided in FIGURE 6a and 6b. FIGURE 6b illustrates apparent widening of the sync waveform due to the fact that the bits preceding and following the sync are logic one bits.

5.2.2.3.7 Controller output levels. The command bus transmit circuitry shall be capable of driving the RG-108 cable up to 243 m (800 ft) in length and additionally shall drive up to 32 total RTs, each attached to the cable by means of stubs (as defined in MIL-STD-1553A) with a maximum of 6.1 m (20 ft). The bus controller's transmit circuitry shall satisfy the requirements of 5.2.1. The command bus installation (design stud locations, numbers, length, and so forth) shall be such that the controller's transmit circuitry will be able to maintain the specified operation with the exception of a 25 percent maximum reduction (design objective) of the data bus signal amplitude (at the command bus cable connection to the output port). This reduction may occur in the event that one of the RTs has a fault that causes it to reflect the fault impedance specified in 5.2.3.2 on the bus. Furthermore, the installation design shall be such that the peak signal output voltage will be between ± 3.0 volts and ± 15.0 volts, line-to-line when measured at the command bus cable connection to the stub (see point A on FIGURE 8).

5.2.2.3.8 RT output waveform. The waveform output from the transmit circuitry of the RT shall consist of a stream of nominally rectangular pulses which may vary in spacing and in duration. The shortest duration for either a positive pulse or a negative pulse is one-half of the period (nominally .5 μs) corresponding to a clock frequency of 1.0 MHz. These shortest duration pulses are generated at those moments when two adjacent data bits in a word are the same



A = BUS STUB CONNECTION POINT FOR BUS STUB
R = ISOLATION RESISTORS
C = R/T END OF BUS STUB

FIGURE 8. Data bus interface (transmit or receive).

value (that is, both ones or both zeros). These pulse characteristics for the PCM signal are shown in FIGURE 7c. A detailed portrayal of the waveform (including transitions) is shown for a logic one in FIGURE 9.

5.2.2.3.9 RT output noise. Noise transferred to either the command bus or response bus by any RT which is not transmitting, or has power removed, shall be minimized at the relevant connection (point A in FIGURE 8) to the respective bus. The peak-to-peak value of the composite noise shall not exceed .1 percent of the maximum cable energy. The random white noise component (that is, thermal or shot noise) shall be less than 0.03 millivolts (mV) (root mean square (rms)) line to line measurements and shall utilize a bandwidth equal to that of the receive circuitry up to and including the pulse detectors.

5.2.3 Interface between C/R bus and RT. The interface shall provide at least the following circuits:

a. Buffer registers.
b. Manchester II modem, including synchronization acquisition and generation circuits and any receive-clock deriving circuits.
c. Parity detecting and generating circuits.
d. Level shifting and timing control as required.
e. Serial to parallel and parallel to serial converters as required.

The bus side interface shall be digital serial as specified herein, whereas the equipment side shall be specialized to the equipment itself and will be specified in the applicable equipment interface specification.

5.2.3.1 Bus AC coupling technique. The remote terminal shall tap onto the command and response bus respectively. This tap shall be accomplished by an AC coupling technique utilizing internal transformers and utilizing external stubs with two isolation resistors as shown in FIGURE 8. This technique provides DC isolation between the bus and remote terminals. Magnetizing inductance and other parameter characteristics of the transmit and receive coupling transformers shall be such as to contribute less than 10 percent degradation to the rise and fall times of the output waveforms or to the receive waveform at the RT pulse detectors.

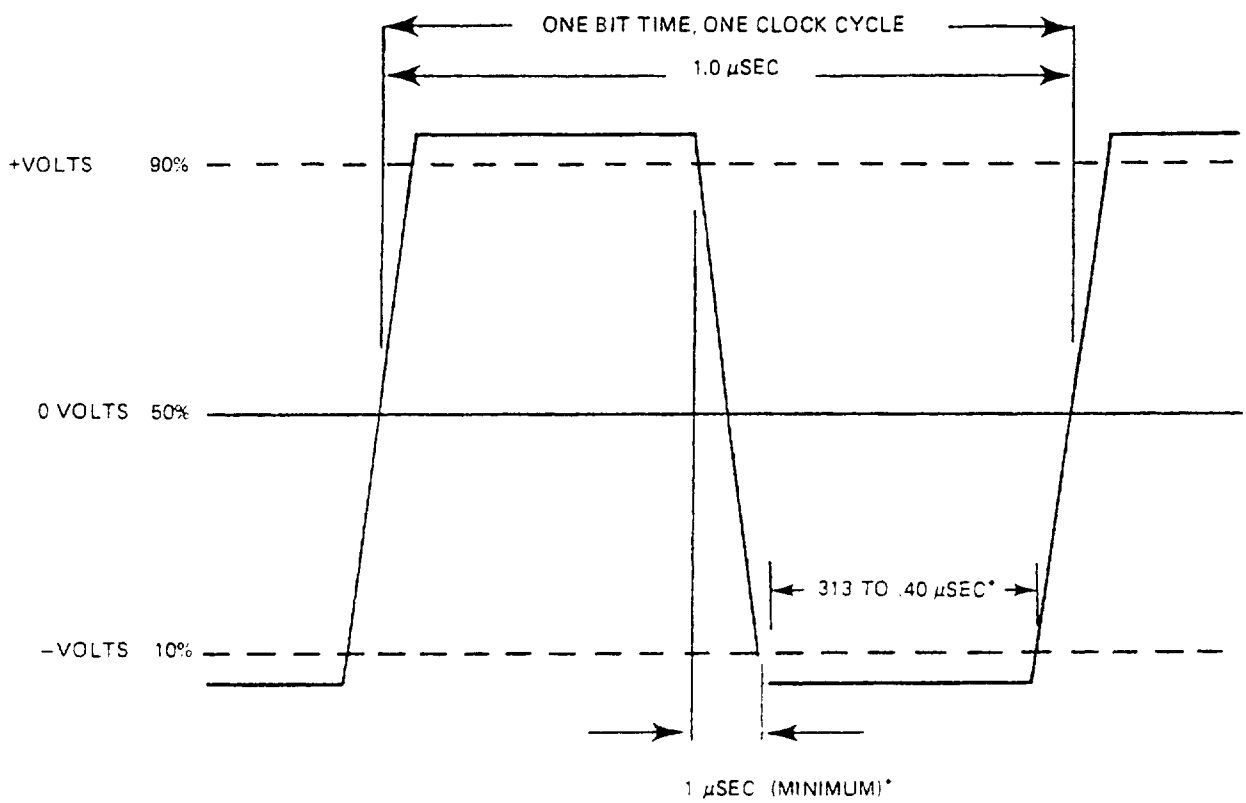
5.2.3.2 Bus fault isolation. For the purpose of minimizing stub-bus interaction effects, a composition type isolation resistor shall be placed in series with each connection to the data bus cable (for each pair of the bus). The resistor shall be selected such that the resulting impedance shall in no way degrade the performance of the bus. In any case, the impedance placed across the data bus shall be no less than 1.5 Z_0 ohms for any failure of the stub isolation transformer, cable stub, or RT. The coupling transformer shall meet the requirements of MIL-T-21038.

5.2.3.3 Typical signal characteristics between the bus and RT.

5.2.3.3.1 Bus interface. The receive (input) circuits of the RT shall present a minimum impedance of 2 thousand (K) ohms, when measured, on the controller's command bus at point C on FIGURE 8. When the transmit circuitry of a RT is not transmitting, or has power removed, the load reflected to point C on FIGURE 8 of the response stub bus shall be a minimum of 10K ohms. Overvoltage faults line-to-line at point C, up to ±20 volts, shall not damage the receiver or transmitter circuitry. Short circuits line-to-line on either command or response bus connections (reference the connection boxes on FIGURE 2) shall not damage either the transmit or receive circuitry of the RT. No elements of the interface system shall be damaged when a bus, or bus-stub is subjected to: short to ground; shorts between lines; common mode transients of plus or minus 100 volts peak, line-to-ground. The term ground, as used herein, shall be considered synonymous with the term signal ground.

5.2.3.3.2 Serial digital signal characteristics. The characteristics of the serial digital signals on the bus shall be in accordance with the following:

a.	Data code	(NRZ), Manchester II.
b.	Type	Differential balanced signaling.



*SEE 5.2.2.3.7

FIGURE 9. Output waveform (logic one).

c.	Word size	20 bit times (16 data bits plus 1 parity bit plus 3 bit times for sync).
d.	Data rate	See modulation rate 4.3.3 and bus signaling, 5.2.2.3.5.
e.	Rise and fall time	As consistent with the output waveform of 5.2.1 and 5.2.2.3.6 as modified by the bus structure (including stubs as per 5.2.3.1) and as modified by the RT input impedance in 5.2.3.4.1.3.
f.	(S+N)/N ratio	In the absence of external noise but with 32 receivers on the command bus, the (S+N)/N Ratio* at the input to the receive shall be adequate to provide better than 20 dB margin in meeting (with 99 percent confidence) the BER and incomplete message requirements of 5.2.3.6.2 and 5.2.3.6.3, respectively.

* System self noise consistent with 5.2.2.3.7, signal consistent with 5.2.3.4.1.

g.	Common mode output voltage	The common mode voltage (measured from each line to the signal ground) shall be no greater than ±0.5 volt peak when measured at either Point A or C of FIGURE 8.
h.	Message size	A fixed number of words for each command or response message block with a maximum of 32 words.

5.2.3.4 RT characteristics.

5.2.3.4.1 RT input characteristics.

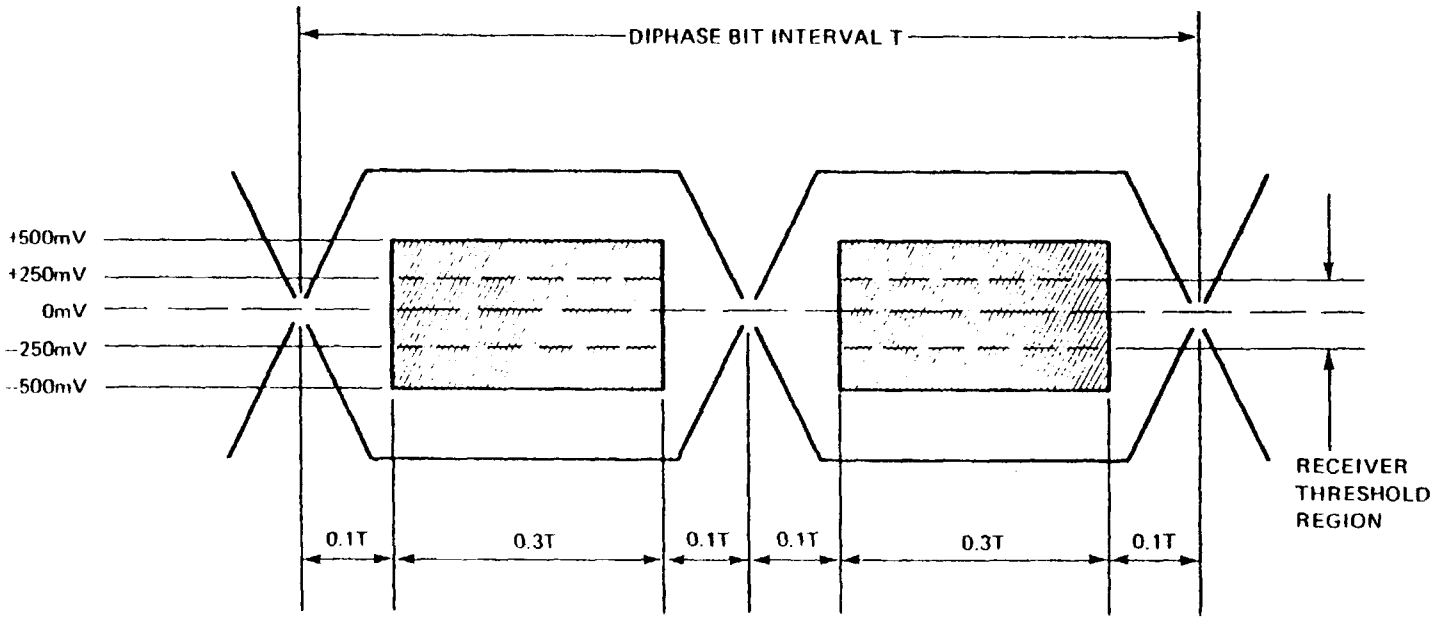
5.2.3.4.1.1 Input waveform compatibility. The RT shall be capable of receiving and operating with the incoming signals specified herein, and shall accept waveforms varying from a square wave to a sine wave. The receive circuitry of the RT shall recover data (error-free) from a differentially balanced command bus signal whose positive or negative peak amplitude, line-to-line, may have a value of up to 15 volts maximum. The same error-free recovery shall be obtained if the received signal is less than the maximum but remains outside the shaded area of the eye pattern shown in FIGURE 10. The receive-circuitry of RT shall not respond (that is, shall produce no transitions) to noise spikes or attenuated signals having positive or negative peak amplitudes, line-to-line, which are less than the receiver sensitivity-threshold of 250 mV, the voltages are measured at point C in FIGURE 8.

5.2.3.4.1.2 Common mode rejections. Any common mode signals from DC to 2.0 MHz, with amplitudes equal to or less than ±10.0 volts peak, line-to-ground, applied to either conductor at Point A of the balanced bus as shown in FIGURE 8 shall not degrade the performance of the RT. The ground-reference for common-mode signal-rejection measurements shall be the signal ground for the relevant conductor pair.

5.2.3.4.1.3 Input impedance. The minimum magnitude at the clock frequency of the RT receive circuitry input impedance and the quiescent output impedance of the RT transmit circuitry shall be as specified in 5.2.3.3.1. These minimum values shall be applicable over the bandwidth from 10 kHz to 1.0 MHz, with a design objective of from 5 kHz to 1.5 MHz. The impedances are permitted to decrease monotonically above and below the specified bandwidth. Under no circumstances shall an odd-harmonic impedance be permitted to exceed the value determined at any lower harmonic frequency (including the clock frequency). All impedance measurements shall be made utilizing test voltages up to 15 volts peak-to-peak applied across point C on FIGURE 8.

5.2.3.4.2 Data validation. Logic shall be provided in each RT to recognize improperly coded signals, data dropouts, or excessively noisy signals. Each word shall conform to the following minimum validating criteria:

a. The word begins with a valid sync field.



NOTE: RECEIVED SIGNAL SHOULD BE OUTSIDE OF SHADED (RESTRICTED) AREA. MEASUREMENTS ARE MADE LINE-TO-LINE. POLARITY CHANGES DURING THE BIT INTERVAL.

FIGURE 10. Input signal minimum requirements.

b. The information field bits are in a valid Manchester II code.
c. The information field has 16 bits plus parity.
d. The word parity is odd.

Where a word fails to conform to the preceding criteria, the word shall be considered invalid and shall not be used by the receiving RT. Where an invalid word sync occurs, the receiving RT shall reset and wait for a new valid message sync. An invalid word count (for data words, in the command message received at the RT) shall be construed as a message error. The RT shall not use the message but shall report the error in its status (single word) response or acknowledgement. If the command word fails to conform to all the preceding criteria including absence of parity error the RT shall remain silent and shall reset (for a new command message) without further action by the RT.

5.2.3.4.3 RT output characteristics. Refer to section 5.2.2.3.7. The transmit circuitry of the RT shall be capable of driving (via bus coupling) the full length of the cable. The cable sections are tapped randomly for up to a total of 32 other transmit circuits, accessed via their respective bus connections. These other quiescent transmit circuits shall comply as necessary with the applicable requirements of 5.2.2.3.8 (noise), 5.2.3.3 (impedance) and 5.2.3.4.1.3 (quiescent transmitter).

5.2.3.4 Terminal operation. The RT shall operate in response to commands received from the bus controller. The RT shall be capable of receiving a command word at any time except when it is transmitting. A received command word shall always be responded to by a status word -- unless said status word contains a parity error or otherwise is considered invalid in accordance with the criteria of 5.2.3.4.2. For these exceptions, the RT shall remain silent and the message-transaction shall be considered incomplete (5.2.3.6.3). The second command word sent to a terminal, after it has commenced processing operations in accordance with a previous command, shall be handled in accordance with unique programming considerations set forth in the relevant equipment specification. Unless specifically stated in that relevant equipment specification, a second command word sent to an RT after it is already operating on one shall invalidate the first command and cause the RT to begin operation on the second command.

5.2.3.5.1 Response time. The RT shall respond to a valid transmit data command in not less than 2 μsec nor more than 5 μsec after receipt of the last bit of the command word. (See TERMINAL TO CONTROLLER TRANSFER in FIGURE 4). The RT shall respond to a valid receive data command in not less than 2 μsec nor more than 5 μsec after receipt of the last bit of the last data word. (See CONTROLLER TO TERMINAL TRANSFER in FIGURE 4.)

5.2.3.5.2 Terminal fail-safe operation. The RT shall contain the self-test circuitry necessary to detect an erroneous transmission of data onto the response bus. This circuit shall include a transmission time-out which will preclude a signal transmission period of greater than .66 milliseconds (ms) (one status, and 32 data words). When the self-test circuitry detects any such erroneous transmission it shall automatically shut down the transmit circuitry of the RT.

5.2.3.6 Environmental considerations. The interface system shall function properly under the test conditions specified in 5.2.3.6.4 and the electromagnetic environment specified in 5.2.3.6.1. The interface system shall exhibit a maximum undetected bit error rate of 10^{-11}, where the bit error rate is as defined in 5.2.3.6.2. The system shall also exhibit a maximum incomplete message rate of 10^{-6} where the incomplete message rate is as defined in 5.2.3.6.3.

5.2.3.6.1 Electromagnetic emissions and susceptibility. The RT and data bus cable emissions and susceptibility shall comply with the applicable requirements of MIL-STD-461.

5.2.3.6.2 BER. For the purposes of 5.2.3.6, the BER is defined in Section 3 as back-to-back (loop) BER. The loop-BER test-scheme involves the process sometimes known as an echo test. The process, when applied to the bus interface system defined herein, makes use of test message pairs. Each message in the pair requires the use of a set of command, data and status words as specified in 5.1.3.2. For the first message, the controller transmits a maximum of 32 data words preceded by a test-coded receive data command word to an RT. This transmission is acknowledged by a no message error status word from the addressed RT. The test-coding shall be defined in the applicable equipment interface specification. This test-coding instructs the RT to store, without

further action, the data words as received from the bus controller. The bus controller then issues a test-coded transmit data command. The RT responds with a status word plus the stored data word so as to complete the second message of the pair. The process is repeated and the BER is calculated in accordance with methods incorporated in this paragraph.

5.2.3.6.3 Incomplete message rate. For the purposes of 5.2.3.6, the incomplete message rate is defined as follows: A message-transaction is the complete set of command, data, and status words as specified in 5.1.3.2. An incomplete message is defined as a message-transaction for which the RT does not properly respond to a command by the bus controller. Included in the foregoing incomplete message definition are the silent response, identified in 5.2.3.5, and the RT reset, identified in 5.2.3.4.2. Not included in the incomplete message definition are the invalid and, therefore, unused data word (in the command message) identified by the receiving RT as stated in 5.2.3.4.2, and, the invalid word count (for the data words) because of unusable or missing data words in the command message (received at the RT). As stated in 5.2.3.4.2, either one of the last two cases may be identified as one in which both the message error bit is set in the RT status word and the RT does not use (that is, operate in accordance with) the bus controller command. Neither case shall be included in the incomplete message count. In all cases, hereunder, the message formats shall be as described in 5.1.3.1. The total number of incomplete messages are counted during a specific time period, as are the total number of messages. The incomplete message rate is given by the total number of incomplete messages divided by the total number of messages. For purposes of system (including software) verification, a separate accounting shall be made of the number of (command) message errors reported by the RT, during the same time period. As a system design objective, the (command) message error rate (determined from RT reports) shall be less than 1×10^{-5}. Errors in the response-messages shall be identified at the bus controller/software interface and also shall be less than the design objective (1×10^{-5}) during the same time period.

5.2.3.6.4 Test conditions. For purposes of the noise tests, the following conditions shall be observed. All data words shall be changed to random bit patterns prior to transmission or reception of the message as stated in 5.2.3.6.2. The test shall be conducted with the bus controller and two RTs both connected by 6.1 m (20 ft) stubs to the main C/R buses which shall be 243 m (800 ft) long and terminated at the far end in a resistance, if applicable. There shall be a minimum distance of 30.5 m (100 ft) between the RT connections. The transmit circuitry of the addressed RT shall provide an output as specified in 5.2.2.3.7 and 5.2.3.4.3. The transmit circuitry of the bus controller shall have its output adjusted downward so as to provide the minimum signal amplitude specified in 5.2.3.4.1.1 at the addressed RT.

5.3 Physical requirements, standard bus. This section provides the requirements of the standard bus for items such as cable junction boxes and connectors.

5.3.1 Cabling, stand-alone bus controller to DPS. This part of the bus system (cables B of FIGURE 2) shall utilize the Type B (NTDS fast) interface specified in MIL-STD-1397, but with 16 bits instead of 32 bits.

5.3.1.1 Cable. A type 2U-45 cable per MIL-C-915/63 shall be utilized for both the input cable and the output cable for the I/O channel of the DPS. The cable lengths shall not exceed 61 m (200 ft).

5.3.1.2 Cable connectors. The connectors for the DPS side of the I/O cable will be the 120 Pin Type and compliant with the applicable requirements of MIL-STD-1397. The connectors for the bus controller side of the I/O cables shall be as follows:

Plugs: (to be mounted on I/O cable)
M28840/21CF1BS1 (Input Cable)
M28840/21CF1P1 (Output Cable)

Receptacles: (to be mounted on bus controller case)
M28840/12AF1XP1 (Input Cable)
M28840/12AF1X51 (Output Cable)

The general specifications for these connectors are set forth in MIL-C-28840(EC), with connector inserts selected from MIL-STD-1698. The contact mating end shall be size 20. The contact size is 20-22 in accordance with MIL-C-39029/83 (Pin) or MIL-C-39029/84 (Socket). The contact style (designator) is P (for pin contact) and S (for socket contacts).

5.3.1.3 Connector pin assignments. The connector pin assignments for the DPS side of the I/O cables shall follow the category I, II, and III parallel connector pin assignments table of APPENDIX A of MIL-STD-1397. The connector pin assignments for the bus controller side of the I/O cables shall follow TABLE I, herein.

5.3.1.4 Connector keying. Keyed connectors used on cable assemblies are keyed with the mating connector mounted on the equipment to prevent improper mating of the connectors, and provide alignment of male connector pins with the female connector.

5.3.2 The cables and connectors of C/R bus. This part of the bus system is unique to HOCS standard and shall be as specified in 5.3.2.1 through 5.3.2.3.

5.3.2.1 Cable. Cables E and G of FIGURE 2 are Type RG-108 in accordance with MIL-C-17/45D. One shielded twisted pair is utilized for the command bus while a second pair is utilized for the response bus. A third pair is reserved and is utilized for distribution of the system clock from the bus controller (see 5.2.2.3.2).

5.3.2.2 Cable coupling. All stub connections to each data bus shall utilize shielded connection boxes. These boxes shall be selected among the listings of junction-boxes (J-box) standardized by common usage aboard Navy surface-based platforms. The box's terminal board(s) and cable entrances shall be such as to provide for electrical and mechanical integrity of the terminations for the conductors and shields of the three Type RG-108 cables entering the box. Additionally, terminals and mounting means shall be provided for the stub-isolation resistors identified in 5.2.3.1 (and in FIGURE 8) and specified in 5.2.3.2. Weight, space and spare terminals also shall be provided in the J-Box, so as to accommodate additional isolation-transformers (not shown in FIGURES 2 or 8). These extra isolation-transformers may be necessary for interfacing stubs of lengths significantly in excess of 6.1 m (20 ft). All grounding shall meet the requirements of MIL-STD-1399 (Navy), Section 406.

5.3.2.3 Cable connectors. Each bus set shall use twinaxial connectors. These connectors shall terminate the RG-108 cable at the RT location and at the appropriate C/R port of the bus controller.

TABLE I. I/O cable-pin assignments (central processor interface with bus controller).

FUNCTION	20 Pin*						
INSERT F-1**	WIRE GROUP						
COLOR CODE							
SIGNAL (2U-45)	RETURN (2U-45)	SIGNAL	RETURN				
IDR/ODA	B-5	A-5	1	6	28	Gray	- Red
IDA/ODR	B-6	A-6	2	7	27	Yellow	- Red
EIR/EFA	B-7	A-7	3	8	26	Purple	- Red
EIE/EFR	B-8	A-8	4	9	25	Brown	- Red
Bit 00	D-1	C-1	12	20	30	Pink	- Red
Bit 01	D-2	C-2	13	21	29	Light Brown	- Red
Bit 02	D-3	C-3	14	22	21	Pink	- White
Bit 03	D-4	C-4	15	23	12	Red	- White
Bit 04	D-5	C-5	16	24	11	Pink	- Black
Bit 05	D-6	C-6	17	25	10	Light Brown	- Black
Bit 06	D-7	C-7	18	26	20	Brown	- White
Bit 07	D-8	C-8	19	27	19	Purple	- White
Bit 08	D-9	C-9	29	37	23	Orange	- Red

TABLE I. I/O cable-pin assignments (central processor interface with bus controller). (Continued)

FUNCTION 20 Pin* INSERT F-1** WIRE GROUP COLOR CODE SIGNAL (2U-45)	RETURN (2U-45)	SIGNAL	RETURN				
Bit 09	D-10	C-10	30	38	22	Green	- Red
Bit 10	D-11	C-11	31	39	13	Green	- White
Bit 11	D-12	C-12	32	40	04	Orange	- Black
Bit 12	G-1	H-1	33	41	01	White	- Black
Bit 13	G-2	H-2	34	42	09	Purple	- Black
Bit 14	G-3	H-3	35	43	16	Dark Brown	- White
Bit 15	G-4	H-4	36	44	18	Yellow	- White
SPARE	G-5	H-5	49	56	2	Red	- White
SPARE	G-6	H-6	50	57	3	Green	- Black
SPARE	G-7	H-7	48	55	5	Blue	- White
SPARE	G-8	H-8	61	62	6	Brown	- Black
SPARE	G-9	H-9	63	64	7	Green	- White
SPARE	G-10	H-10	51	58	8	Yellow	- Black
SPARE	G-11	H-11	47	54	14	Orange	- White
SPARE	G-12	H-12	52	59	15	Blue	- Black
SPARE	J-1	K-1	53	60	17	Gray	- White
SHIELD	--	B-1	--	28	--		
Wire Groups not Connected 31-45							
Spare Pins 5-45-46							

* Per the Category I, II, and III parallel connector pin assignments table of APPENDIX A to MIL-STD-1397

** Insert (from MIL-STD-1698(EC)) for MIL-C-28830, MIL-C-28840(EC) Connectors

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APPENDIX

10.0 General. This appendix is presented to provide the user of this standard more insight into the application of this standard. The flexibility and constraints inherent in this standard are highlighted below.

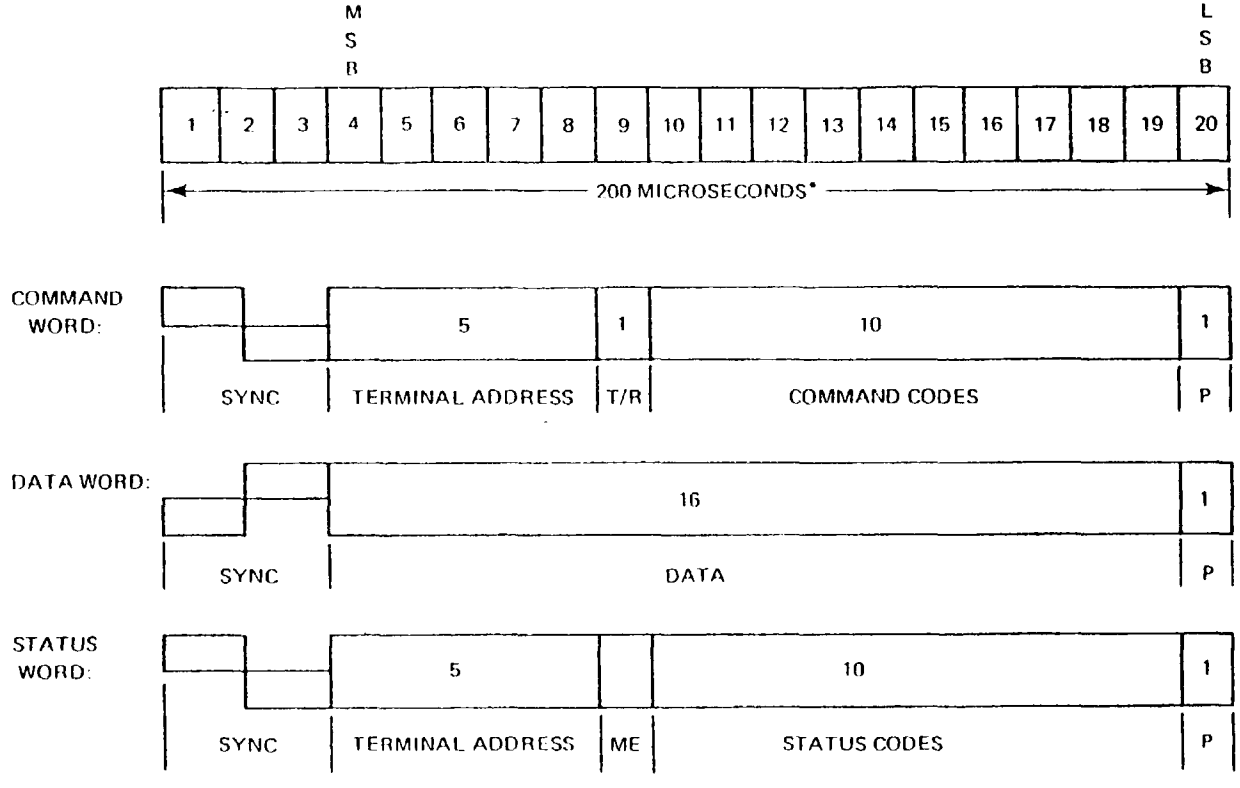
10.1 Bus controller. The bus controller, whether integral to the DPS or stand-alone, is a key part of the data bus system. The functions of the controller, in addition to the issuance of commands, must include the constant monitoring of the data bus and the traffic on the bus. It is possible that many of the routine details of bus monitoring (for example, parity checking, terminal response time-out, and so forth) could be embodied in hardware, while the algorithms for bus control and decision making could reside in software. It is important to remember that since the bus controller function is a focal point for modification and growth within this multiplex system, any software must be written in such a manner as to permit modification with relative ease and to be transparent to bus users.

10.2 Word formats. The standard bus will handle three kinds of messages: command words, data words, status words. The word formats for each are shown in FIGURE 11. The word size shall be 16 bits plus the synchronization waveform (3 bit times) and a parity bit for a total of 20 bit times.

10.2.1 Command word. The command word shall be comprised of a sync waveform, address, T/R bit, command codes and a parity bit. Command codes (and the ten bits associated with them) are purposely left undefined in the body of this standard. In this way, the ten bits associated with the command word may be utilized in any manner that two or more users of the bus choose. The choice and definition of the 10 bits for command (or status, as discussed in 10.2.3) is left to the designers or maintainers of the equipment types to be controlled through the control and status interface bus. It is envisioned that standard command will be developed for certain equipment types and systems and that NAVELEX will serve as the point of contact for dissemination of these standard commands as they are developed. By allowing for this flexibility in the assignment of command word codes for the equipment types, the control and status needs for each equipment type can be best satisfied without unduly burdening the bus system. FIGURE 12 is an example illustrating how a command code field may be assigned, in this case for a radio.

10.2.2 Data words. The data word shall be comprised of a sync waveform, 16 data bits and a parity bit as shown in FIGURE 11. The data to be transferred does not have a particular format defined in this standard.

10.2.3 Status word. The status word is shown in FIGURE 11 and shall be comprised of sync waveform, RT address, message error bit, status codes and a parity bit. Status codes have purposely been left undefined in the body of this standard for the same reason as explained in 10.2.1. This approach allows the nine bits associated with status codes to be allocated in any way two or more bus users choose. Just as in the command word case, however, it is envisioned that standard status codes will be developed and that NAVELEX will serve as the point of contact for dissemination of these standard codes. FIGURE 13 illustrates a sample allocation of the status code bits. It is important to emphasize that the status codes will be developed and standardized to satisfy equipment type needs.



*(20 BITS EACH 10 MICROSECONDS LONG. SEE 4.3.3, 5.1.3.2 AND 5.2.2.3.7)

FIGURE 11. Word formats on the standard bus.

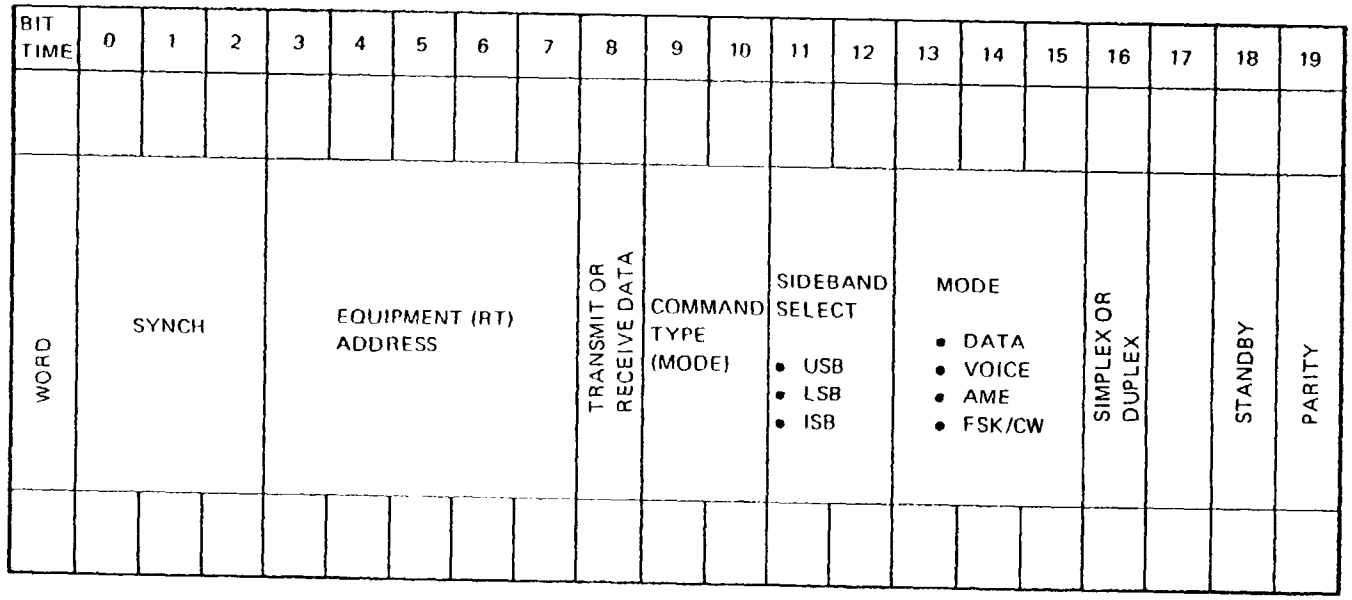


FIGURE 12. Sample command word bit assignment.

BIT TIME	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
WORD	SYNC			EQUIPMENT (RT) ADDRESS					MESSAGE ERROR	POWER SUMMARY FAULT	PHASE LOCK LOOP SUMMARY FAULT	FREQUENCY STANDARD FAULT	RECEIVER SUMMARY FAULT	ANTENNA COUPLER SUMMARY FAULT	OPERATE	STANDBY	TUNE SUMMARY FAULT	TUNING (IN PROGRESS)	RECEIVER KEY ENABLE	PARITY

FIGURE 13. Sample status word bit assignment.

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