

NOTICE OF CHANGE

INCH-POUND

MIL-STD-1835B
NOTICE 2
15 December 1997

DEPARTMENT OF DEFENSE

INTERFACE STANDARD FOR MICROCIRCUIT CASE OUTLINES

TO ALL HOLDERS OF MIL-STD-1835B:

1. THE FOLLOWING PAGES OF MIL-STD-1835B HAVE BEEN REVISED AND SUPERSEDE THE PAGES LISTED:

NEW PAGE	DATE	SUPERSEDED PAGE	DATE
59	3 September 1996	59	REPRINTED WITHOUT CHANGE
60	15 December 1997	60	3 September 1996
131	3 September 1996	131	REPRINTED WITHOUT CHANGE
132	15 December 1997	132	3 September 1996
135	3 September 1996	135	REPRINTED WITHOUT CHANGE
136	15 December 1997	136	3 September 1996
141	15 December 1997	141	3 September 1996
142	3 September 1996	142	REPRINTED WITHOUT CHANGE

2. RETAIN THIS NOTICE AND INSERT BEFORE TABLE OF CONTENTS.

3. Holders of MIL-STD-1835B will verify that page changes and additions indicated above have been entered. This notice will be retained as a check sheet. This issuance, together with appended pages, is a separate publication. Each notice is to be retained by stocking points until the standard is completely revised or canceled.

CONCLUDING MATERIAL

Custodians:
Army - CR
Navy - EC
Air Force - 17
NASA - NA

Preparing activity:
DLA - CC

Review activities:
Army - AR, MI, SM
Navy - AS, CG, MC, OS, SH
Air Force - 19, 85, 99

(Project 5962-1803)

Civil Agency Coordinating Activities:
DOT-FAA(RD-650)

AMSC N/A
DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1 of 1

FSC 5962

This page intentionally blank

MIL-STD-1835B
NOTICE 2

1/ <

FIGURE 13. Can style.

REPRINTED WITHOUT CHANGE

MIL-STD-1835B
NOTICE 2

*

1/ Symbol	Variations (all dimensions shown in millimeters) 2/											
	A1			A2			A3			A4		
	Min	Max	Note	Min	Max	Note	Min	Max	Note	Min	Max	Note
A	4.19	4.70		4.19	4.70		4.19	4.70		6.10	6.60	
φb	0.41	0.48	1	0.41	0.48	1	0.41	0.48	1	0.41	0.48	1
φb1	0.41	0.53	1	0.41	0.53	1	0.41	0.53	1	0.41	0.53	1
φb2	0.41	0.61		0.41	0.61		0.41	0.61		0.41	0.61	
φD	8.51	9.52		8.51	9.52		8.51	9.52		8.89	9.40	
φD1	7.75	8.51		7.75	8.51		7.75	8.51		8.00	8.51	
φD2	2.79	4.06		2.79	4.06		2.79	4.06				2
e	5.08 BSC			5.84 BSC			5.84 BSC			5.08 BSC		
e1	2.54 BSC			2.92 BSC			2.92 BSC			2.54 BSC		
F	---	1.02		---	1.02		---	1.02		---	1.02	
k	0.69	0.86		0.69	0.86		0.69	0.86		0.69	0.86	
k1	0.69	1.14	3	0.69	1.14	3	0.69	1.14	3	0.69	1.14	3
L	12.70	19.05	1	12.70	19.05	1	12.70	19.05	1	12.70	19.05	1
L1	---	1.27	1	---	1.27	1	---	1.27	1	---	1.27	1
L2	6.35	---	1	6.35	---	1	6.35	---	1	6.35	---	1
Q	0.25	1.14		0.25	1.14		0.25	1.14				2
α	45° BSC			36° BSC			30° BSC			45° BSC		
β	45° BSC			36° BSC			30° BSC			90° BSC		
N	8			10			12			3		
Notes	6, 7, 8											

FIGURE 13. Can style - Continued.

SUPERSEDES PAGE 60 OF MIL-STD-1835B

MIL-STD-1835B
NOTICE 2

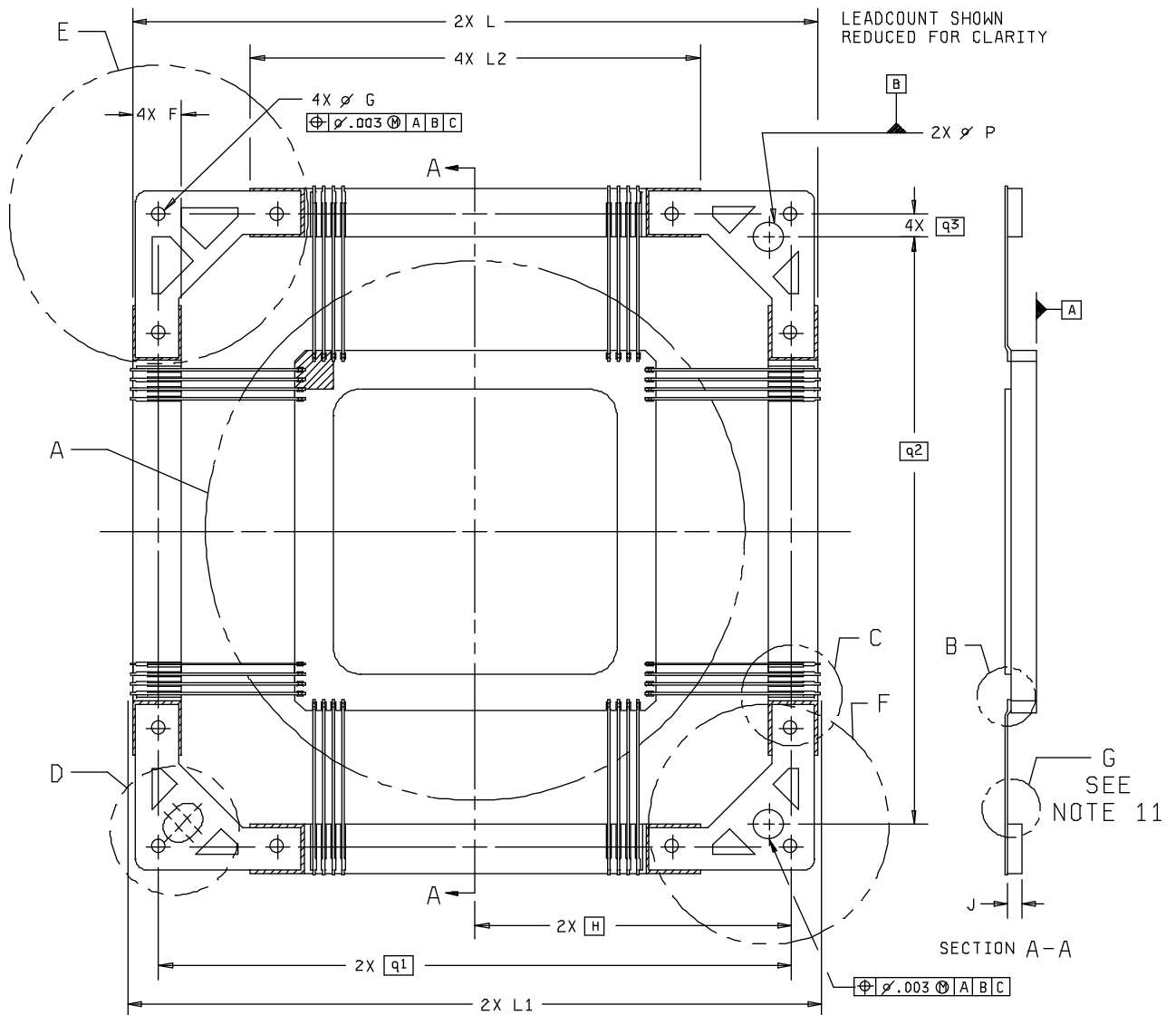
NOTES:

1. Controlling dimension: inch.
2. Metallized castellations shall be connected to Plane 1 terminals.
3. Index area: An identification mark shall be located adjacent to pin one within the shaded area shown. Plane 1 terminal identification may be an extension of the length of the metallized terminal which shall not be wider than the b dimension.
4. The cover shall not extend beyond the edges of the body.
5. The corner shape (square, notch, radius, etc.) may vary at the manufacturer's option.
6. N indicates total number of terminal positions.
7. Unless otherwise specified, a minimum clearance of .015 inch shall be maintained between all metallized features (e.g., lid, castellation, terminals, thermal pads, etc.).
8. Solder finish is optional with a maximum allowable thickness of .007 inch. Measurement of dimensions A, b1, and L2 may be made prior to solder application.
9. For terminal identification purposes only, terminals between N1 and N2 and between N3 and N4 are omitted if values for N1, N2, N3 and N4 are listed on the table.

FIGURE 23. Dual leadless chip carrier style - Continued.

REPRINTED WITHOUT CHANGE

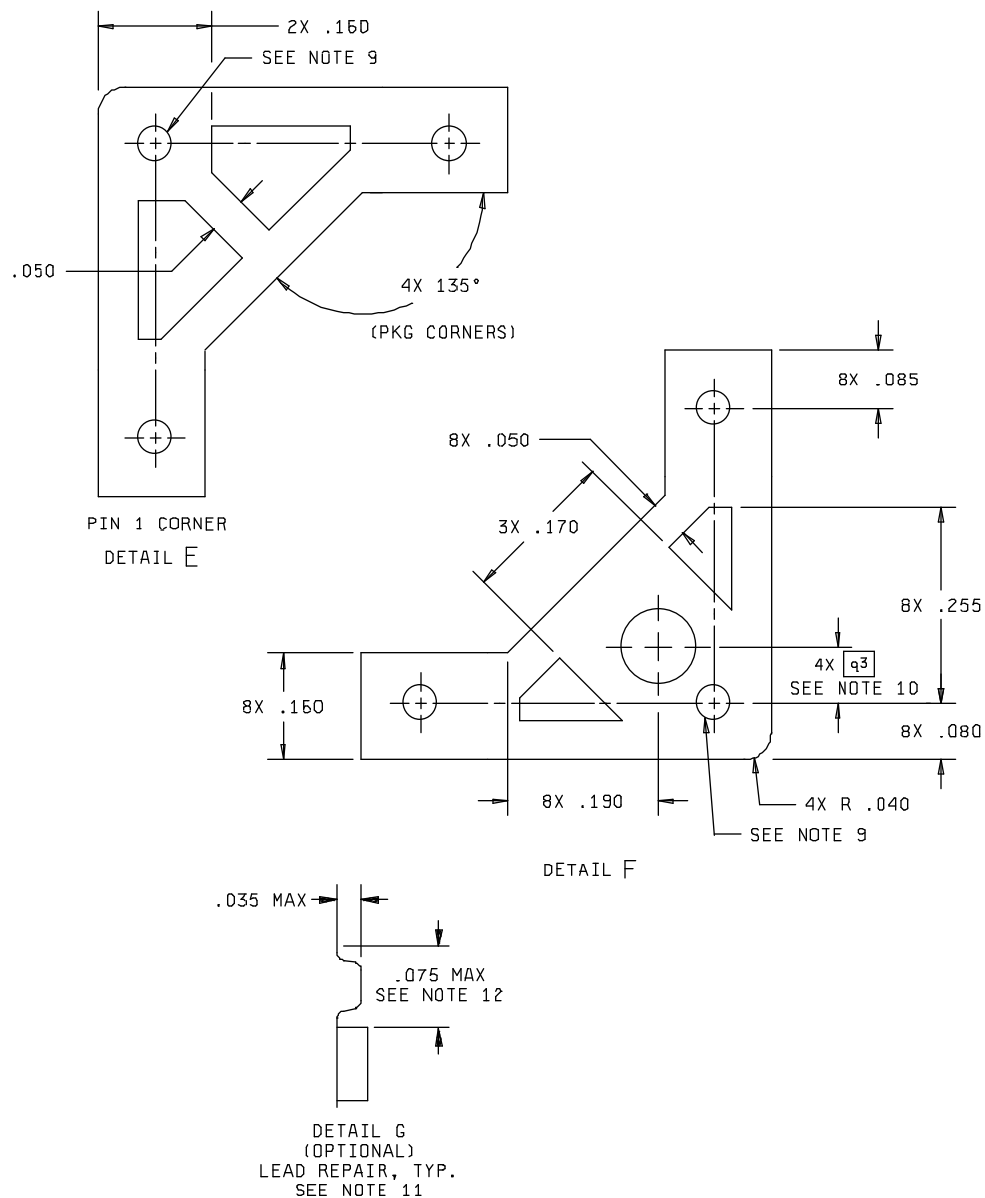
MIL-STD-1835B
NOTICE 2



* FIGURE 24. Ceramic, quad leaded chip carrier style with non-conductive tie bar.

SUPERSEDES PAGE 132 OF MIL-STD-1835B

MIL-STD-1835B
NOTICE 2



NOTE:

The user's attention is called to the possibility that compliance with this figure may require use of an invention covered by patent rights; specifically, National Semiconductor, Inc. has stated that U. S. Patent No. 4,796,080 may relate to a certain implementation of this product outline. By publication of this figure, no position is taken with respect to the validity of this claim of any patent rights in connection therewith.

* FIGURE 24. Ceramic, quad leaded chip carrier style with non-conductive tie bar - Continued.

MIL-STD-1835B
NOTICE 2

NOTES:

1. A terminal 1 identification mark shall be located at the index corner in the shaded area shown. Terminal 1 is located immediately adjacent to and counterclockwise from the index corner. Terminal numbers increase in a counterclockwise direction when viewed as shown.
2. Generic lead attach dogleg depiction. May be flat lead configuration.
3. Includes lead attach dogleg height and lid height, whichever is greater. Dimension A and A1 do not include heat sinks or other attached features.
4. Corner chamfers and or notches are optional. Pin #1 may have optional feature (larger or smaller chamfer or notch) for mechanical orientation purposes.
5. Dimension N: Number of terminals.
6. Dimension ND/NE: Number of terminals per package edge.
7. Controlling dimension: inch.
8. Dimensions b1 and c1 apply to base metal only, dimension M applies to the plating thickness.
9. Optional hole configuration applicable to all four corners.
10. Circular corner hole only. Slotted hole locations are shown on Detail D (optional).
- * 11. Lead repair is optional. This view shows the drawn portion of the lead that must reside within these dimensions. The shape of the repaired lead (as shown) is for reference only.
- * 12. Coplanarity requirements do not apply in this area of a repaired lead.

FIGURE 24. Ceramic, quad leaded chip carrier style with non-conductive tie bar - Continued.

MIL-STD-1835B
NOTICE 2

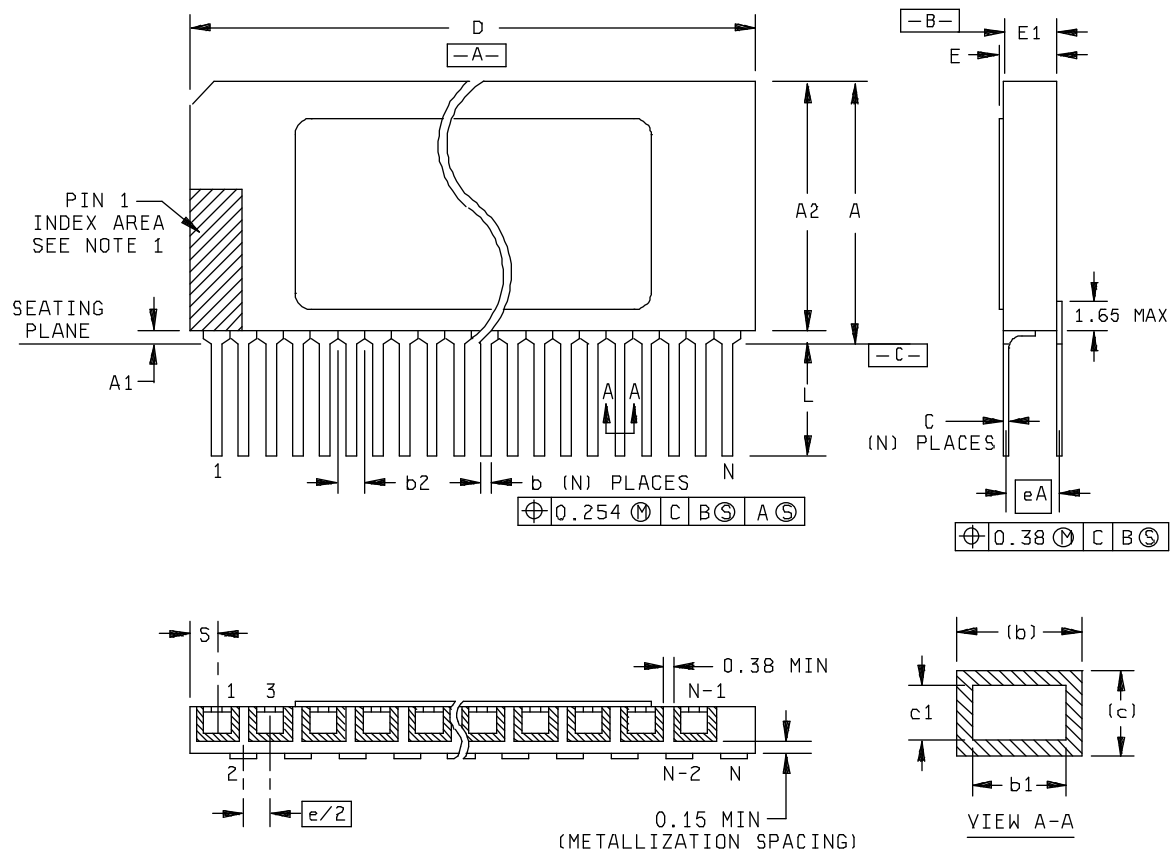


FIGURE 25. Ceramic, zig-zag in-line package style.

REPRINTED WITHOUT CHANGE