Downloaded from http://www.everyspec.com

MIL-STD-1779 (USAF)
1 NOVEMBER 1983

MILITARY STANDARD

INTERFACES FOR HIGH CAPACITY C^3 LOCAL AREA NETWORKS

NO DELIVERABLE DATA
REQUIRED BY THIS DOCUMENT

FSC-5895

fence with programs for infants and toddlers with disabilities.

Downloaded from http://www.everyspec.com

Department Of Defense
Washington D.C.,20301

Input/Output Interfaces for High Capacity C3 Networks,Air Force Systems.

MIL-STD-1779(USAF)

1. This Military Standard is approved for use by Rome Air Development Center, Department of the Air Force, and is available for use by all Departments and Agencies of the Department of Defense.

2. Beneficial comments (recommendations, additions, deletions) and any pertinent data which may be of use in improving this document should be addressed to Rome Air Development Center, Attn: DCLW/Mr J. Davis, Griffiss Air Force Base, New York 13441, by letter or by using the self-Adressed Standardization Document Proposal (DD Form 1426) appearing at the end of this document.

Downloaded from http://www.everyspec.com

FOREWORD

1. This standard is intended for use by equipment designers and computer programmers as well as systems engineers and is limited to interface characteristics--physical, functional and electrical. This standard, by specifying functional interface requirements, does not specify the specific philosophy to be used for any system application; rather it is limited to functional characteristics of the interface signals and formats.

Downloaded from http://www.everyspec.com

CONTENTS

Paragraph		Page
1.	SCOPE	1
1.1	Principal Statement	1
2.	REFERENCED DOCUMENTS	1
2.1	Issues of Documents	1
3.	DEFINITIONS	1
3.1	List of acronyms	1
4.	GENERAL REQUIREMENTS	2
4.1	Digital Interface	2
4.1.1	Digital Physical Interface	2
4.1.2	Digital Link Interface	2
4.1.3	Digital Network Interface	2
5.	DETAILED REQUIREMENTS	2
5.1	Digital Interface	2
5.1.1	Digital Physical Interface	2
5.1.1.1	Interface Application	2
5.1.1.2	Signal Lines	2
5.1.1.3	Line Configuration	2
5.1.1.4	Control Lines	2
5.1.1.5	Timing Utility Line	3
5.1.1.6	Data Lines	3
5.1.1.7	Data Transmission Rate	3
5.1.1.8	Timing	3
5.1.1.9	Precedence of Direction	4
5.1.1.10	Data Transfer Procedure	4
5.1.1.11	Control Signal Direction	4
5.1.1.12	Electrical Requirements	4
5.1.1.13	Connector Requirements	5
5.1.2	Digital Link Interface	5
5.1.2.1	Interface Header Section	5
5.1.2.1.1	Header Word Formats	5
5.1.2.1.2	Header Field Formats	5

Downloaded from http://www.everyspec.com

CONTENTS

Paragraph		Page
5.1.2.1.2.1	Word One	6
5.1.2.1.2.2	Word Two	7
5.1.2.1.2.3	Word Three	7
5.1.2.1.2.4	Word Four	8
5.1.2.1.2.5	Word Five	8
5.1.2.1.2.6	Word Six	9
5.1.2.1.2.7	Word Seven	10
5.1.2.1.2.8	Word Eight	10
5.1.2.1.2.9	Word Nine	10
5.1.2.1.2.10	Word Ten	11
5.1.2.1.2.11	Word Eleven	11
5.1.2.1.2.12	Word Twelve	11
5.1.2.1.2.13	Words Thirteen through Fifteen	12
5.1.2.1.2.14	Word Sixteen	12
5.1.2.1.2.15	Header Map	12
5.1.2.1.3	Relationship to Digital Interface	12
5.1.2.2	Data Section	12
5.1.2.2.1	Data Section Size	13
5.1.2.2.2	Word Definition	13
5.1.2.2.2.1	Preferred Subsets	13
5.1.2.3	Trailer Section	14
5.1.2.3.1	Very Short Blocks	14
5.1.2.3.2	Word Data Subsets	15
5.1.2.3.3	Unused Data Bits	15
5.1.2.4	Data Message Block Format	15
5.1.2.5	Order of Presentation	15
5.1.3	Digital Network Interface	15
5.1.3.1	Header Interpretation by Message Type	15
5.1.3.1.1	Local Broadcast Messages	16
5.1.3.1.2	External Broadcast Messages	16
5.1.3.1.3	Command Messages from DTE	16
5.1.3.1.4	Command Messages from BUS	17
5.1.3.1.5	Discrete Messages	17
5.1.3.1.6	Subbus Message-Virtual Bus	17
5.1.3.1.7	Subbus Message-Lazy Susan Bus	19
5.1.3.2	Header Interpretation-General	21
5.1.3.3	Command Message Data Interpretation	21

Downloaded from http://www.everyspec.com

List of Figures

Figure	Para Ref	Title
1	5.1.1.3	Hardware Interface
2	5.1.1.8	Bus Response Times
3	5.1.1.10	Transfer - Bus to DTE
4	5.1.1.10	Transfer - Bus to DTE
5	5.1.1.10	Transfer - DTE to Bus
6	5.1.1.10	Transfer - DTE to Bus
7	5.1.1.10	State Diagrams-Bus Arbitration
8	5.1.1.10	State Diagrams-Bus to DTE
9	5.1.1.10	State Diagrams-Bus Signoff
10	5.1.1.10	State Diagrams-DTE to Bus
11	5.1.1.10	State Diagrams-DTE Signoff
12	5.1.1.12	Electrical Interface Schematic
13	5.1.1.12	Interface Waveshape
14	5.1.1.13	Physical Digital Interface
15	5.1.2.1.2.15	Header Map
16	5.1.2.3	Trailer Word Allocation
17	5.1.3	Message Block Format

Downloaded from http://www.everyspec.com

List of Tables

Table	Para Ref	Title
I	5.1.1.4	Control Lines Bus to DTE
II	5.1.1.4	Control Lines DTE to Bus
III	5.1.1.12	TTL Voltages
IV	5.1.2.1.2.6	Header Word Six (word count)
V	5.1.2.5	Order of Presentation

Downloaded from http://www.everyspec.com

1. SCOPE

1.1 Scope. This standard defines requirements for digital input/output interfaces to the Flexible Intraconnect Bus System.

2. REFERENCED DOCUMENTS

2.1 Government Documents. The following documents of the issue in effect on date of invitation for bids or request for proposal, form a part of this standard to the extent specified herein.

Military MIL-M-38510/420(USAF),Microcircuits,N-channel,Silicon Gate monolithic 8 Bit Microprocessor.(Copies of specifications required by contractors in connection with specific procurement functions should be obtained from the contracting activity or as directed by the contracting officer)

3. DEFINITIONS

3.1 List of Acronyms.

BDA	Bus Data Available
BMF	Bus Mode Flag
BOR	Bus Output Request
BRR	Bus Receiver Ready
Bus	Refers to the FILAN
DDA	DTE Data Available
DMF	DTE Mode Flag
DOR	DTE Output Request
DRR	DTE Receiver Ready
DTE	Digital Terminal Equipment
FI	Flexible Intraconnect
I/O	Input/Output
LAN	Local Area Network
LS	Lazy Susan bus
LSB	Least Significant Bit
MSB	Most Significant Bit
TTL	Transistor-Transistor Logic
VB	Virtual Bus

Downloaded from http://www.everyspec.com

4. GENERAL REQUIREMENTS

4.1 Digital Interfaces. The I/O requirements specified herein include requirements for physical interface, link interface, and network interface for digital message blocks.

4.1.1 Digital Physical Interface. The I/O requirements include control and data signal definition and timing requirements for establishing and executing the transfer of a block of digital words.

4.1.2 Digital Link Interface. The I/O requirements include generation, definition, and interpretation of certain information within message block headers, message block data sections, and message block trailers.

4.1.3 Digital Network Interface. The I/O requirements include generation, definition, and interpretation of certain information within message block headers not defined in 4.1.2.

5. DETAILED REQUIREMENTS

5.1 Digital Interface.

5.1.1 Digital Physical Interface. The digital hardware interface shall be that combination of control and data signals that exists between a Digital Terminal Equipment (DTE) and the Flexible Intraconnect Local Area Network (hereinafter referred to as "the Bus" or "Bus").

5.1.1.1 Interface Application. The digital hardware interface shall facilitate the transfer of digital information from a DTE to the Bus and from the Bus to a DTE.

5.1.1.2 Signal Lines. There shall be five control lines, eighteen data lines and one timing utility line. The direction of the data lines shall be determined by their usage, i.e., to transmit or receive data.

5.1.1.3 Line Configuration. The digital hardware interface shall be configured as shown in Figure 1.

5.1.1.4 Control Lines. The five control lines shall be designated as C1, C2, C3, C4 and C5. The logical signal designations for the control lines shall be as shown in Table I for data transfer from Bus to DTE. The logical signal designations for the control lines shall be as shown in Table II for data transfer from the DTE to the Bus.

Downloaded from http://www.everyspec.com

5.1.1.5 Timing Utility Line. The timing utility line shall be designated as T1. The timing utility line shall be a unidirectional line carrying utility clock pulses from the Bus to the DTE. There is no expressed or implied function of the clock pulse signals within the scope of this standard. The frequency of the clock shall be 15.25878906 MHz (nominal) (see para 5.1.3.2 for more detail).

5.1.1.6 Data Lines. The eighteen data lines shall be designated as D0, D1, D2,...D17. The direction of all eighteen data lines shall be consistent among the lines. That is, data flow shall be permitted in either direction, i.e., Bus to DTE or DTE to Bus, at any time but not in both directions at the same time. The data lines shall use half-duplex operation. Lower numbered data lines shall be considered to be Least Significant Bits (LSB) and higher numbered data lines shall be considered to be Most Significant Bits (MSB), as shown in FIGURE 14. Physical Digital Interface.

5.1.1.7 Data Transmission Rate. The interface shall permit data transfer rates within the range of one tenth of a bit per second (0.1 bit/sec) nominal to ten million bits per second (10 Mb/s) nominal with respect to each of the data lines. The equivalent eighteen bit word parallel transfer range is from one tenth of a word per second to ten million words per second. The equivalent composite range of data transfer rates with respect to the eighteen data lines shall be 1.8 bits per second to 180 million bits per second (180 Mb/s). Transfer at lower rates than one bit per ten seconds can be accomplished by the process of transmitting data blocks at the desired interval and transmitting zero length blocks at the rate required to preclude timeout; e.g., at least one block every 10 seconds. The zero length block can be addressed to the source, rather than the destination intended for the data, if this avoids complications at the destination.

5.1.1.8 Timing. Transfer with respect to data words shall be completely asynchronous. Bus response times shall be as shown in Figure 2.

Downloaded from http://www.everyspec.com

5.1.1.9 Precedence of Direction. In the event both the Bus and the DTE wish to initiate a data transfer at the same time, the Bus shall prevail. Resolution of such conflict shall occur within two microseconds of the bus initiated transfer.

5.1.1.10 Data Transfer Procedure. Data shall be transferred across the interface in blocks. Transfer of data shall be conducted in accordance with a sequence of logical states of the control signals C1, C2, C3, and C4. The sequence of states of the four control signals shall be as shown in Figures 3, 4, 5, and 6. Figures 3 and 4 depict the sequence of control signal states applicable to the transfer of information from the Bus to the DTE. Figures 5 and 6 specify the sequence of control signal states applicable to the transfer of data from the DTE to the Bus. The interface transfer procedure shall be as depicted by the state diagrams in Figures 7, 8, 9, 10 11.

5.1.1.11 Control Signal Direction. The direction of the control signals C1 and C2 shall be unidirectional. The direction of control signals C3, C4, and C5 shall be bidirectional. The logical name of the signal shall be determined based on the direction of data transfer. These names shall be as shown in Tables I and II.

5.1.1.12 Electrical Requirements. Electrical requirements for the interface circuits defined in 5.1.1 shall be as specified herein. The interface shall be compatible with Transistor Transistor Logic (TTL), having logic levels in accordance with MIL-M-38510/420. All lines shall be tri-state, i.e., three possible output states--two normal low-impedance logic "1" or "0" states and a high-impedance state that allows up to 128 tri-state outputs to be tied together and connected to a common bus line. In the high impedance state, maximum current leakage shall be no greater than 40 microamperes with 5.5 Vdc applied to the output. Figure 12 specifies a schematic representation of the electrical interface.Figure 13 specifies the electrical interface waveshape. Voltages shall be as shown in Table III.

Downloaded from http://www.everyspec.com

5.1.1.13 Connector Requirements. Connector requirements and pin assignments shall be as shown in Figure 14.

5.1.2 Digital Link Interface. Data message block transfers across the I/O interface shall consist of a block of words containing a header section, a data section, and a trailer section in that order.

5.1.2.1 Interface Header Section. The interface header section shall consist of sixteen words and each header word shall be eighteen bits wide. The bits in each word of the header shall be referred to as bit 0, bit 1,...bit 17 where bit 0 is the least significant bit and bit 17 is the most significant bit.

5.1.2.1.1 Header Word Formats. The first fifteen words of the header shall consist of two nine bit halfwords. Bits 0 through 8 define the least significant halfword. Bits 9 through 17 define the most significant halfword. In each halfword the most significant bit shall be a latitudinal odd parity bit, that is, bit 8 is the parity bit for the least significant halfword and bit 17 is the parity bit for the most significant halfword. The last (sixteenth) word of the header shall be longitudinal odd parity of the first fifteen header words.

5.1.2.1.2 Header Field Formats. The header shall consist of fields. The header fields shall not include bit 8 or bit 17 of the header words. The format, definition, word position, interpretation, and constraints applicable to each header field shall be as described below. The notation used below follows these conventions:

a. Fields are designated by a string of identical characters.

b. Each character represents one bit of the header word/field.

c. The right-most symbol represents the least significant bit.

d. The left-most symbol represents the most significant bit.

e. All unused bit positions are designated by the character "/" and shall be set equal to 0 (zero).

f. The letter "p" designates latitudinal parity bits.

Downloaded from http://www.everyspec.com

5.1.2.1.2.1 Word One. Word one of the header shall have the following format and interpretation:

p gggg aqqq p rrvv vvvv

Field	Bit Position	Definition
g	13-16	Message type
a	12	ACK/NACK mode
q	9-11	System mode
r	6-7	Message priority
v	0-5	Subbus number

gggg field	Interpretation
0010	Local broadcast messages
0011	External broadcast messages
0100	Command messages (from DTE)
0101	Command messages (from Bus)
0110	Discrete messages
1010	Subbus message, virtual bus
1100	Subbus message, ring bus

a field	Interpretation
0	ACK/NACK procedure disabled
1	ACK/NACK procedure enabled

rr field	Interpretation
00	Lowest priority
01	Next to lowest priority
10	Next to highest priority
11	Highest priority

qqq field Only value permitted is 000

vvvvvv field Value 000000 not permitted

Downloaded from http://www.everyspec.com

5.1.2.1.2.2 Word Two. Word two of the header shall have the following format and definition:

p u/ww wwww p //xx xxxx

Field	Bit Position	Definition
u	16	Virtual/real selector (0 = virtual, 1 = real)
w	9-14	Destination virtual address, high order
x	0-5	Destination virtual address, low order

All values shall be permitted for each field except only all zeros is used with Command Messages from the DTE, i.e., gggg (message type) field equal to 0100.

5.1.2.1.2.3 Word Three. Word three of the header shall have the following format, definition and interpretation:

p //yy yyyy p ffzz zzzz

Field	Bit Position	Definition
y	9-14	Destination real address (high order)
f	6-7	Header interpretation flag
z	0-5	Destination real address (low order)

Fields y and z are each permitted all values except 000000.

Field ff	Interpretation
Bit 6	Bit Set = 1 only by DTE when DTE is sending and indicating header interpretation is necessary
Bit 7	Bit Set = 1 only by Bus when Bus is sending and indicating header interpretation is necessary.

Note: Use of field ff is reserved for future use. Current implementation only requires capability for specified action.

Downloaded from http://www.everyspec.com

5.1.2.1.2.4 Word Four. Word four of the header shall have the following format and definition:

p //jj jjjj p //kk kkkk

Field	Bit Position	Definition
j	9-14	Source virtual address, high order
k	0-5	Source virtual address, low order

All values shall be permitted for each field except 000000, which shall only be used with Command Messages from the Bus, i.e., gggg (message type) field equal to 0101.

5.1.2.1.2.5 Word Five Word five of the header shall have the following format, definition and interpretation:

p //ll llll p ddmm mmmm

Field	Bit Position	Definition
l	9-14	Source real address, high order
d	6-7	Data block sizing code
m	0-5	Source real address, low order

Fields l and m shall each be permitted all values except 000000.

Field dd	Interpretation
00	Data block length is not longer than 40 full words
01	Data block length is not longer than 1024 full words
10	Data block length is not longer than 2048 full words
11	Data block length is exactly 4096 full words

Downloaded from http://www.everyspec.com

5.1.2.1.2.6 Word Six. Word six of the header shall have the following format, definition and interpretation.

p cccc cccc p ccch bbbb

Field	Bit Position	Definition
c	9-16	Data word (full word) count (upper portion)
c	5-7	Data word (full word) count (lower portion)
h	4	Halfword indicator
b	0-3	Halfword unused bit count

Field h	Intrepretation
0	Least significant halfword (bits 0 through 8) of last data word (following last full word) is not included
1	Both halfwords are included in last word of data (following last full word)

Field bbbb Value shall indicate number of least significant bits included in last halfword included in the last data word (following the last full word). Range of bbbb field is 0 through 9.

The total number of bits in the data section of the message block shall, therefore, be represented by the following expression: (c x 18) + (h x 9) + (9-b) where c, h and b are the decimal equivalents of the binary values of each of the three fields. Refer to Table IV for a representative list of values for these fields. The user shall be responsible for formatting the bits in the last word and halfword, if he chooses to transmit less than full words. The software in the interface shall set the indicated unused halfwords or bits to zero, if not already such, to allow minimum transfer over related serial interfaces.

Downloaded from http://www.everyspec.com

5.1.2.1.2.7 Word Seven Word seven of the header shall have the following format and definition:

p nnnn nnnn p nnnn nnnn

Field	Bit Position	Definition
n	9-16	Message number (upper portion)
n	0-7	Message number (lower portion)

5.1.2.1.2.8 Word Eight Word eight of the header shall have the following format and definition.

p ssss ssss p ssss ssss

Field	Bit Position	Definition
s	9-16	Sequence number (upper portion)
s	0-7	Sequence number (lower portion)

5.1.2.1.2.9 Word Nine Word nine of the header shall have the following format and definition:

p //// //// p tttt tttt

Field	Bit Position	Definition
t	0-7	System time (high order bits of a 56 bit system time field)

Laudable recognition for acts of valor, exceptional service or achievement

Downloaded from http://www.everyspec.com

5.1.2.1.2.10 Word Ten Word ten of the header shall have the following format and definition:

p tttt tttt p tttt tttt

Field	Bit Position	Definition
t	9-16	System time (portion of 56 bit field)
t	0-7	System time (portion of 56 bit field)

5.1.2.1.2.11 Word Eleven Word eleven of the header shall have the following format and definition:

p tttt tttt p tttt tttt

Field	Bit Position	Definition
t	9-16	System time (portion of 56 bit field)
t	0-7	System time (portion of 56 bit field)

5.1.2.1.2.12 Word Twelve Word twelve of the header shall have the following format and definition:

p tttt tttt p tttt tttt

Field	Bit Position	Definition
t	9-16	System time (portion of 56 bit field)
t	0-7	System time (portion of 56 bit field)

Downloaded from http://www.everyspec.com

5.1.2.1.2.13 Words Thirteen through Fifteen Words thirteen, fourteen, and fifteen of the header shall have the following format and definition:

p //// //// p //// ////

5.1.2.1.2.14 Word Sixteen. Word sixteen of the header shall have the following format and definition:

e eeee eeee e eeee eeee

Word sixteen shall be a longitudinal (vertical) odd parity of the first fifteen words of the header.

5.1.2.1.2.15 Header Map. Figure 15 specifies a composite map of the header, illustrating field locations and codes.

5.1.2.1.3 Relationship to Digital Physical Interface. With the exception of control line C5 (see para 5.1.1.4), there shall be no relationship between the Digital Network Interface and the Digital Physical Interface. The relationship between control line C5 and the header shall be as follows:

Word 3 field f bit 6 is associated with transfer from the DTE to the Bus. C5 shall reflect the logical state of bit 6 during the period of message block transfer. Word 3 field f bit 7 is associated with transfer from the Bus to the DTE. C5 shall reflect the logical state of bit 7 during the period of message block transfer. Note: This C5 function is reserved for future use. The current implementation shall be required only to provide this capability.

5.1.2.2 Data Section. The data section shall follow the header section and shall have the following limitations, constraints and conventions.

Downloaded from http://www.everyspec.com

5.1.2.2.1 Data Section Size. The data section shall be defined in terms of numbers of data words as follows:

Type	Range Inclusive (Number of words)
00	0 - 40
01	0 - 1024
10	0 - 2048
11	4096

In types 00, 01, and 10 the last word to be transmitted may consist of either one or two halfwords with the final halfword transmitted to consist of any number of bits from 1 to 9. Unused bits shall be the bits of higher significance.

5.1.2.2.2 Word Definition. A standard data word shall be defined as an eighteen bit word. The bits in the standard data word shall be referred to as bit 0, bit 1,...bit 17 where bit 0 is the least significant and bit seventeen is the most significant bit. The number of words permitted in the data section shall be as specified in 5.1.2.2.1.

5.1.2.2.2.1 Preferred Subsets. The following data word subsets shall be defined as preferred subsets. The preferred defined subsets shall be: a 16 bit subset, an 8 bit subset, and a 9 bit subset. The bit positions for these preferred word subsets shall be as shown below. "B" shall indicate used bit position, "/" shall indicate unused bit position. Note: Use of 18 bit data field has no mandatory requirements. Random bit patterns are allowed.

Bit Position

	MSB																	LSB
Preferred subset	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
16 bit subset	/		B	B	B	B	B	B	B	B	/		B	B	B	B	B	B
8 bit subset	/		/	/	/	/	/	/	/	/	/		B	B	B	B	B	B
9 bit subset	/		/	/	/	/	/	/	/	/	B		B	B	B	B	B	B

For the purposes of establishing word count, each word subset shall count as one word.

Downloaded from http://www.everyspec.com

5.1.2.3 Trailer Section. The trailer section of the message block shall follow the data section and shall consist of eight words. The eight words shall consist of vertical odd parity bits based on the contents of the data section. The eight parity words shall be applied uniformly to the overall data section where each of the parity words is associated with approximately one eighth of the words in the data section. The first parity word in the trailer shall be the first word to follow the last word of the data section. The first word of the trailer shall be associated with the first eighth of the data section, the second word of the trailer shall be associated with the second eighth of the data section, etc. The eighth word of the trailer shall be associated with the last (remaining) "eighth" of the data section. The actual number of words in the last "eighth" of the data section may be more than the true arithmetic value of one-eighth of the total number of data words. In the event the number of data words in the data section is not evenly divisible by eight, the number of words contained in the final "eighth" shall be equal to the numerical equivalent obtained by dividing the total number of words in the data section by eight and adding the remainder. For example:

Total number of words = 747 4p Divided by 8 = 93, remainder = 3

In this case, the first seven parity (trailer) words shall each be applied to each of the seven corresponding sets of 93 words in the data section. The last (eighth) trailer word shall apply to the last set of 93 words plus the 3 remaining data words (total of 96 words in last "one-eighth" of the data section).

5.1.2.3.1 Very Short Blocks. For blocks with a data section of less than eight words, the eight trailer words shall be evenly distributed against the data words. For example, if the data section contained seven words, the first seven parity words would each be associated with each of the data words one through seven. The eighth parity word shall be associated with word one, or if the data section contained four words, the first and fifth parity words shall each be associated with the first data word, the second and sixth parity words shall each be associated with the second data word, etc. If there were only one data word, each of the eight parity words shall be associated with the one data word. The allocation for all cases (from zero words through 7 words) shall be as specified in Figure 16.

Downloaded from http://www.everyspec.com

5.1.2.3.2 Word Data Subsets. The parity words in the trailer shall follow the same subset conventions used in the data section. That is if the data words are using the nine bit subset the parity words in the trailer shall be nine bit words.

5.1.2.3.3 Unused Data Bits. If the last word (or word subset) in the data section has unused bits, these bits shall be considered as equal to zero for purposes of computing the associated vertical parity trailer word.

5.1.2.4 Data Message Block Format. Figure 17 specifies the composition of the complete message block for the digital link interface.

5.1.2.5 Order of Presentation. The message block shall be presented in the following order: header section followed by the data section followed by the trailer section. Within each section, words shall be presented in natural sequence, i.e., word one of the header is the first word to be presented. In the event that individual words are not presented in full parallel style, the least significant halfword shall be presented first. In the event that complete halfwords are not fully present, the bits shall be presented in the order of least significant bits(if any) from the least significant halfword followed by the least significant bits from the most significant halfword.Refer to table v for a clarification of this requirement.

5.1.3 Digital Network Interface. The network interface protocol shall relate to the interpretation of information transferred across the standard interface. Transfers of information across the interface shall be constructed as specified in Figure 17.

5.1.3.1 Header Intrepretation by Message Type. Interpretation and contents of certain fields of the header section shall depend on the contents of the message type field (bits 13-16, word one) of the header section of the message block.

Downloaded from http://www.everyspec.com

5.1.3.1.1 Local Broadcast Messages. Message type code 0010 shall define a Local Broadcast message. There shall be no fields that require special interpretation for a local broadcast message. The following fields shall have no function for local broadcast messages:

Field Code/Size/ Position			Definition
a	1	W1	ACK/NACK
s	16	W8	Sequence number
v	6	W1	Subbus number
x	6	W2	Destination virtual address (low)
z	6	W3	Destination real address (low)

Fields x and z shall be set = to 111 111.

5.1.3.1.2 External Broadcast Messages. Message type code 0011 shall define an External Broadcast message. There are no fields that require special interpretation for a external broadcast message. The following fields have no function for external broadcast messages:

Field Code/Size/ Position			Definition
a	1	W1	ACK/NACK
s	16	W8	Sequence number
u	1	W2	Virtual/real indicator
v	6	W1	Subbus number
w	6	W3	Destination virtual address (high)
x	6	W3	Destination virtual address (low)
y	6	W4	Destination real address (high)
z	6	W4	Destination real address (low)

Fields w, x, y and z shall each be set = to 111 111.

5.1.3.1.3 Command Message from DTE. Message type code 0100 shall define a command message from DTE. There shall be no header fields that require special interpretation for a command message from the DTE message. (Data interpretation shall be required as specified in 5.1.3.3). The following fields shall be constrained as follows:

Field Code/Size/ Field			Constraint
w	6	W2	Destination virtual address (high) shall be 000000 (a pseudo address).
x	6	W2	Destination virtual address (low) shall be 000000.

Downloaded from http://www.everyspec.com

5.1.3.1.4 Command Message from Bus. Message type code 0101 shall define a command message from the Bus message. There shall be no header fields that require special interpretation for a command message from the Bus message. (Data interpretation shall be required in 5.1.3.3). The following fields shall be constrained as specified:

Field	Code/Size/ Position		Constraint
y	6	W3	Source virtual address (high) shall be 000000 (a pseudo address).
z	6	W3	Source virtual address (low) shall be 000000.

5.1.3.1.5 Discrete Messages. Message type code 0110 shall define a discrete (point-to-point) message. There shall be no fields that require special interpretation for a discrete message.

5.1.3.1.6 Subbus Message-Virtual Bus. Message type code 1010 shall define a subbus Message-Virtual Bus. (The Virtual Bus (VB) shall also be known as a passive subbus.) The following header fields shall be interpreted as follows:

Field	Code/Size/ Position		
v	6	W1	The subbus number shall be used to identify one of sixty-three unique VB subbuses within the overall FI bus structure. The VB subbus number is used as a common address reference by those DTEs that are members of a particular subbus (virtual bus).(Code all 1, not legal).

Downloaded from http://www.everyspec.com

Field Code/Size/ Position		
s	16	W8

The VB sequence number shall be used to indicate order of transmission on a virtual bus. The sequence number has no interpretation for non-transmitting members of a virtual bus. Interpretation of the VB sequence number is dependent on whether a particular subbus (virtual bus) is operating in mode A or mode B. In Virtual bus mode A, members of the bus shall transmit message blocks in a strict preestablished sequential order. The VB sequence number shall be used to determine the order in which each member of a virtual bus is to transmit. The VB sequence number shall be incremented by one count at each transmission. During initialization of a virtual bus each transmitting member is provided with three numbers:

(1) A start up (initial) sequence number,
(2) A repetition interval, and
(3) A wait time.

As a VB begins operation, each member compares the received header VB sequence number to its assigned start up sequence number. If the two numbers match, the member is obligated to provide the next transmission on the VB. The transmission is delayed by the member until the wait time has been counted. The wait time is the amount of time a member must hold its transmission following receipt of its enabling sequence number. For example, if VB member "M" is assigned start up sequence number = 17 and repetition interval = 20, M will transmit following receipt of VB message block header with sequence numbers 17, 37, 57, 77,.... (Choice and assignment of the initial sequence number, repetition interval, and wait time are accomplished at a higher level protocol outside the FI system.) Calculations are modulo, 16 bits (65536).

Downloaded from http://www.everyspec.com

In virtual bus mode B, the transmit order and transmit enabling rate shall be regulated by a protocol established by the members of a VB. The header sequence number shall not be used. In VB mode B, members transmit at quasi-periodic times based on control information provided by one member, designated as the VB "master." Individual members calculate time for transmission by the algorithm to + n(ti) +/- correction (t zero plus n times t sub i + or - correction), where to = original assigned time, ti = time interval between transmissions, and correction = time difference provided by the VB master. The bus shall quantify time to one microsecond for the purpose of regulating VB mode B operation.

5.1.3.1.7 Subbus Message-Lazy Susan Bus. Message type code 1100 shall define a subbus message - Lazy Susan Bus. (The Lazy Susan (LS) bus is also known as an active subbus or virtual ring in that each member of a LS subbus is obligated to accept a message block from the member preceding it in the ring. In the VB, or passive subbus, there is no obligation on any member to accept message blocks from other members.) The following header fields shall be interpreted as follows:

Field	Code/Size/ Position	
v	6	W1

The subbus number shall be used to identify one of sixty-three unique LS subbuses within the overall FI bus structure. The LS subbus number is used as a common address reference by those DTEs that are members of a particular subbus (Lazy Susan).(Code all 1, not legal)

Downloaded from http://www.everyspec.com

Field Code/Size/ Position		
j	6	W4
k	6	W4

The source virtual address (j = high, k = low) shall be used for queuing sequence of transmission among members of a LS subbus. When a LS subbus is established, one master shall be designated for the subbus. The participating members shall be identified as to their position on the LS ring. Device sequence shall be based on the source virtual address of the device which precedes it in the ring. Therefore, each member of the LS subbus is assigned a number that corresponds to the source virtual address of its predecessor in the ring. (Each member shall be also assigned a wait time. The wait time shall be the amount of time a member must delay transmission following receipt of a message block from its designated predecessor.) If the DTE has not accepted the transmission or has not returned the message to the system at the time for transmission, the system shall transmit the original block received.

NOV 10, 94

Downloaded from http://www.everyspec.com

5.1.3.2 Header Intrepretation-General. The header words shall be interpreted as follows:

Field code/Size/ Position		
t	56	W9-W12

System time. System time is entered by the bus, at the time a message block is released for transmission on the FI network. System time shall be measured from the beginning of the first day of the month of January, year 1900. The least significant digit of the system time field shall represent 2**16 picoseconds (65536 psec) which shall correspond to a clock rate for the least significant digit (word 12 Bit 0) of the system time field of 15.2587890603 MHz. This shall yield a pulse interval at bit 4 word 12 of the system time field of 1.048576 microseconds. The minimum rate for time shall correspond to incrementing bit 4 of word 12. Note: The system time field shall normally be supplied by the bus.

5.1.3.3 Command Message Date Interpretation. To be supplied by Preparing activity.

Preparing Activity
Air Force - 17
(Proj 5895-F306)

Downloaded from http://www.everyspec.com

TABLE I. Control Lines Designations

for

Data Transfer from Bus to DTE

Control Line Reference No.	Name of Line	Direction of Signal	Function of Signal
C1	Bus Output Request (BOR)	Bus to DTE	Set condition indicates bus system wants to transfer data block to DTE
C2	DTE Output Request (DOR)	DTE to Bus	Set condition indicates DTE system wants to transfer signoff to bus
C3	Bus Data Available (BDA)	Bus to DTE	Set condition indicates a bus data word is available (for acceptance by DTE)
C4	DTE Receiver Ready (DRR)	DTE to Bus	Set condition indicates DTE is ready to accept a data word from bus
C5	Bus Mode Flag (BMF)	Bus to DTE	Set condition indicates interpretation is required within DTE

is signed in the United States by the military member

Downloaded from http://www.everyspec.com

TABLE II. Control Line Designation

for

Data Transfer from DTE to Bus

Control Line Reference No.	Name of Line	Direction of Signal	Function of Signal
C1	Bus Output Request (BOR)	Bus to DTE	Set condition indicates Bus system wants to transfer signoff to DTE.
C2	DTE Output Request (DOR)	DTE to Bus	Set condition indicates readiness of DTE to transfer data block to Bus system.
C3	DTE Data Available (DDA)	DTE to Bus	Set condition indicates DTE data word is available (for acceptance by Bus)
C4	Bus Receiver Ready (BRR)	Bus to DTE	Set condition indicates DTE ready to accept a data word from DTE.
C5	DTE Mode Flag (DMF)	DTE to Bus	Set condition indicates interpretation is required within Bus system.

Downloaded from http://www.everyspec.com

TABLE III. TTL Compatible Voltages (Nominal)

NOMINAL VOLTAGE, V_T	OUTPUT CURRENT, I_T
Logic 0: 0 Vdc to 0.7 Vdc	+2.0 ma
Logic 1: 2.7 Vdc to 5.5 Vdc	-0.4 ma
V_T Max: 7 Vdc, - .30 Vdc	

Tri-State High Impedance State

Max Current Leakage: +/- 40 microamp with a V_T of 5.5 Vdc

MIL-M-38510/420-01

Downloaded from http://www.everyspec.com

TABLE IV. Representative Values for Header Word Six

Binary Value of Register		Decimal Equivalent of		
No. of Full Words	No. Bits in Partial Word	"c"(11 bits)	"h"(1 bit)	" b"(4 bits)
0	0	0	0	9
1	0	1	0	9
2	0	2	0	9
2047	0	2047	0	9
2048	0	2047	1	0
0	1	0	0	8
0	2	0	0	7
0	9	0	0	0
0	10	0	1	9
0	17	0	1	8
1	1	1	0	8
1	2	1	0	7
1	9	1	1	9
1	10	1	1	1
1	17	1	1	8

* Note-values of 10,11,12,13,14,15 are illegel and presence of such values shall cause an error message.

Downloaded from http://www.everyspec.com

Table V. Order of Presentation

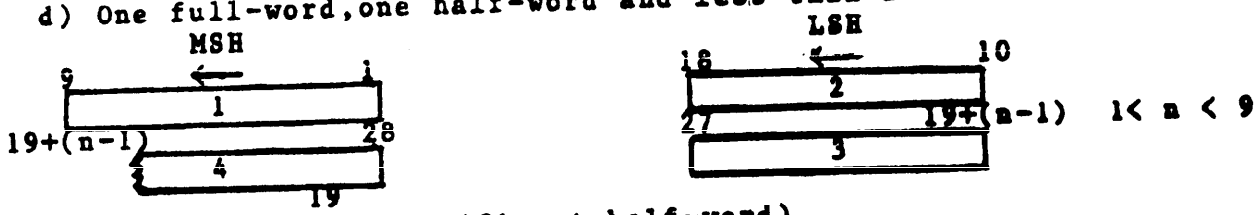
The following diagram illustrates the order of presentation of the bits of a message onto a serial link:

a) Two full words:

b) One full-word and one halfword:

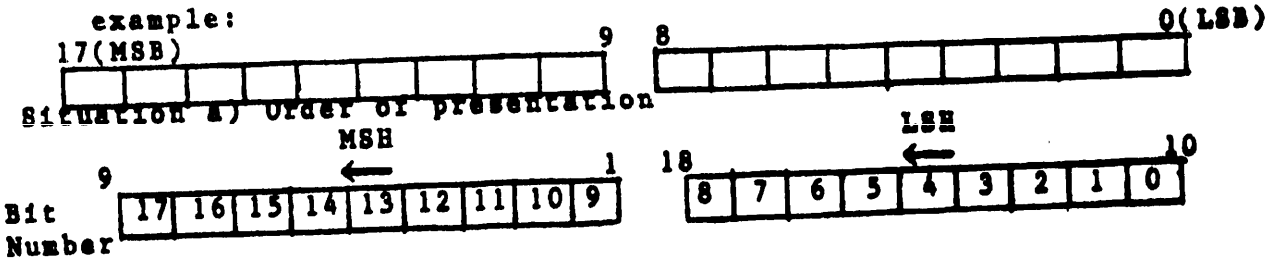
C) One full-word and less than a halfword:

d) One full-word, one half-word and less than a half-word;



Note: LSH(Least significant half-word)
MSH(Most significant half-word)

The numbers in these diagrams represent the order of presentation only, and do not represent the normal bit numbers as otherwise referenced in this document. For example:



Downloaded from http://www.everyspec.com

Signal Line Number	Line Name
D0	Data Line No. 1
D1	" " " 2
D2	" " " 3
D3	" " " 4
D4	" " " 5
D5	" " " 6
D6	" " " 7
D7	" " " 8
D8	" " " 9
D9	" " " 10
D10	" " " 11
D11	" " " 12
D12	" " " 13
D13	" " " 14
D14	" " " 15
D15	" " " 16
D16	" " " 17
D17	Data Line No. 18
C1	Control Line No. 1
C2	" " " 2
C3	" " " 3
C4	" " " 4
C5	Control Line No. 5
T1	Timing Utility Line

FIGURE 1. Digital Hardware Interface

Downloaded from http://www.everyspec.com

Propagation Delays in Nanoseconds

	Min	Typ	Max
DRRL to BDAL	5	28	43
DRRH to BDAH	5	17	27
DORL to BRRL	600	--	2000*
BDAL to BDAL(cycle)	50	--	10sec

* plus software time.

NOTE: All Propagation delay measurements shall be taken at the Bus interface connector (no cable length delays are included) An identical interface (mating)equal to the bus side interface shall be used. An interface for a DTE can operate at a lower rate as limited by the circuitry or the rate of the DTE.

FIGURE 2. Bus Response Times

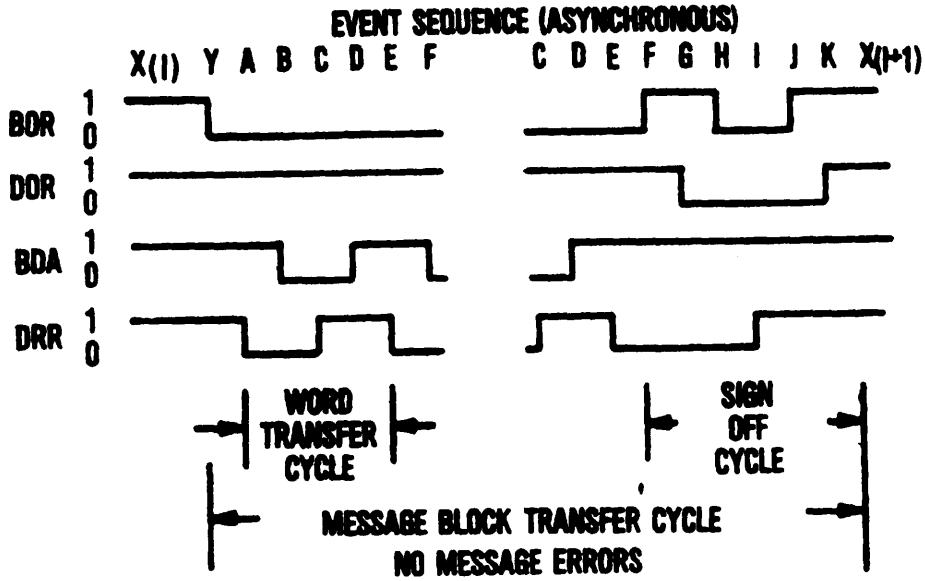
Downloaded from http://www.everyspec.com

SIGNAL LINE STATE

EVENT	BOR C1	DOR C2	BDA C3	DRR C4	ACTION/INTERPRETATION
X(i)	1	1	1	1	Quiescent
Y	0	1	1	1	Bus initiates message transfer
A	0	1	1	0	DTE indicates ready for message transfer
B	0	1	0	0	Bus indicates word is on lines
C	0	1	0	1	DTE indicates word is accepted (by DTE)
D	0	1	1	1	Bus indicates word transfer complete
E	0	1	1	0	DTE indicates ready for next word
F	0	1	0	0	Bus indicates word is on lines; return to event C for next word (C1=0)
or					or
F*	1	1	1	0	Bus indicates no more words (C1=1)
G	1	0	1	0	DTE indicates signoff
H	0	0	1	0	Bus indicates start of signoff
I	0	0	1	1	DTE continues signoff
J	1	0	1	1	Bus indicates message transfer complete
K	1	1	1	1	DTE indicates message transfer complete, no message errors(C2=0)
X(i+1)	1	1	1	1	Quiescent
or					or
K*	1	0	1	0	DTE indicates message transfer complete, message has errors(C4=0)
L	0	0	1	0	Bus continues signoff
M	0	0	1	1	DTE continues signoff
N	1	0	1	1	Bus indicates message transfer complete
O	1	1	1	1	DTE indicates message transfer complete
X(i+1)	1	1	1	1	Quiescent

FIGURE 3. Block Data Transfer Procedure-
Bus to DTE.

Downloaded from http://www.everyspec.com



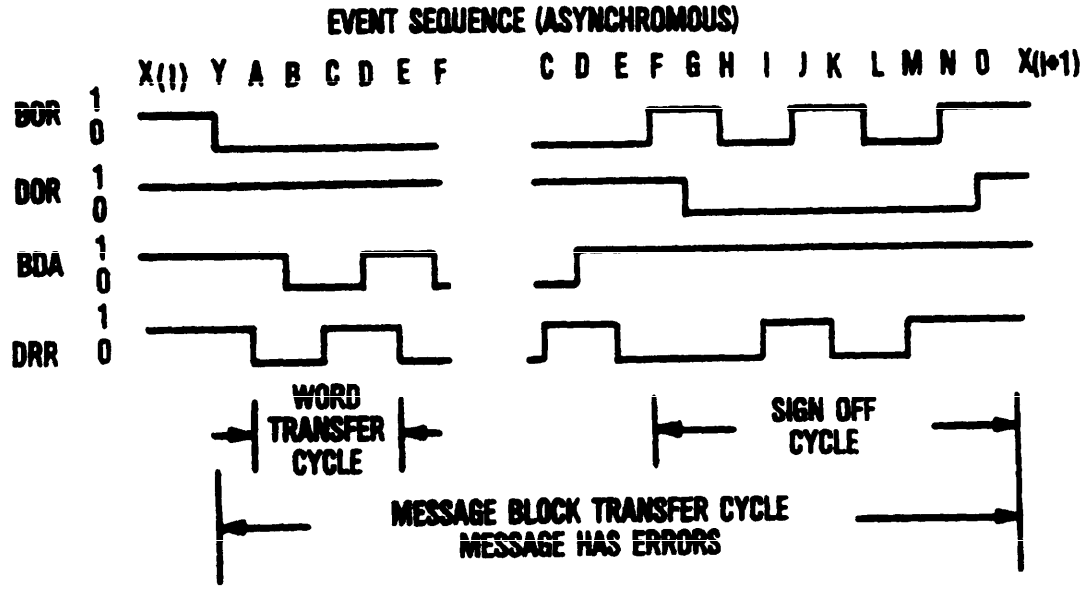


FIGURE 4. Block Data Transfer Procedure-Bus to DTE.

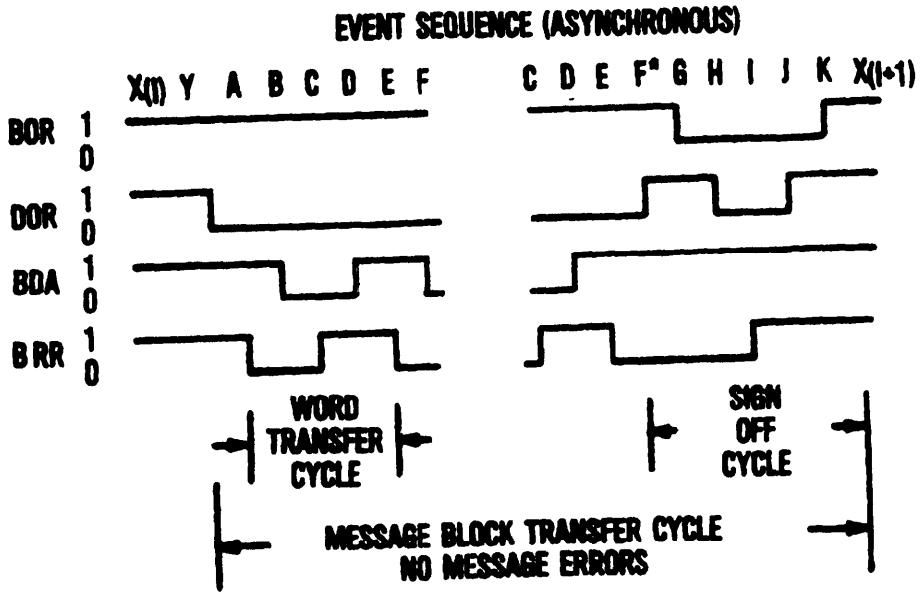
Downloaded from http://www.everyspec.com

SIGNAL LINE STATE

EVENT	BOR C1	DOR C2	DDA C3	BRR C4	ACTION/INTERPRETATION
X(i)	1	1	1	1	Quiescent
Y	1	0	1	1	DTE initiates message transfer
A	1	0	1	0	Bus indicates ready for message transfer
B	1	0	0	0	DTE indicates word is on lines
C	1	0	0	1	Bus indicates word is accepted (by bus)
D	1	0	1	1	DTE indicates word transfer complete
E	1	0	1	0	Bus indicates ready for next word
F	1	0	0	0	DTE indicates word on lines; Return to event C for next word (C2=0)
or					or
F*	1	1	1	0	DTE indicates no more words (C2=1)
G	0	1	1	0	Bus indicates signoff
H	0	0	1	0	DTE indicates start of signoff
I	0	0	1	1	Bus continues signoff
J	0	1	1	1	DTE indicates message transfer complete
K	1	1	1	1	Bus indicates message transfer complete, no message errors (C1=1)
X(i+1)	1	1	1	1	Quiescent
or					or
K*	0	1	1	0	Bus indicates message transfer complete, message has errors(C4=0)
L	0	0	1	0	DTE continues signoff
M	0	0	1	1	Bus continues signoff
N	0	1	1	1	DTE indicates message transfer complete
O	1	1	1	1	Bus indicates message transfer complete
X(i+1)	1	1	1	1	Quiescent

FIGURE 5. Block Data Transfer Procedure-DTE to Bus.

Downloaded from http://www.everyspec.com



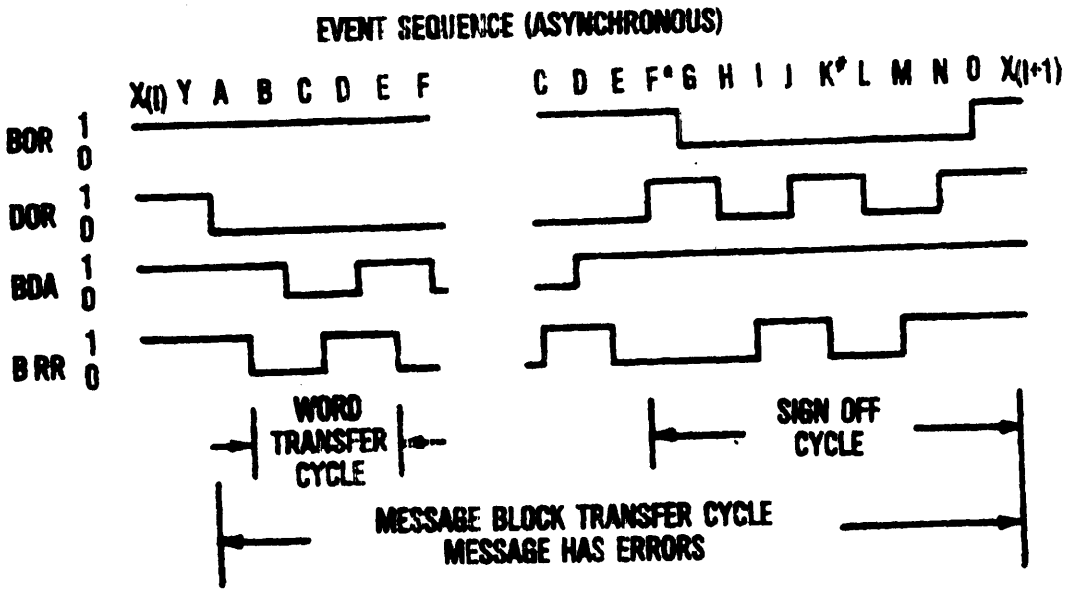


FIGURE 6. Block Data Transfer Procedure-DTE to Bus.

Downloaded from http://www.everyspec.com

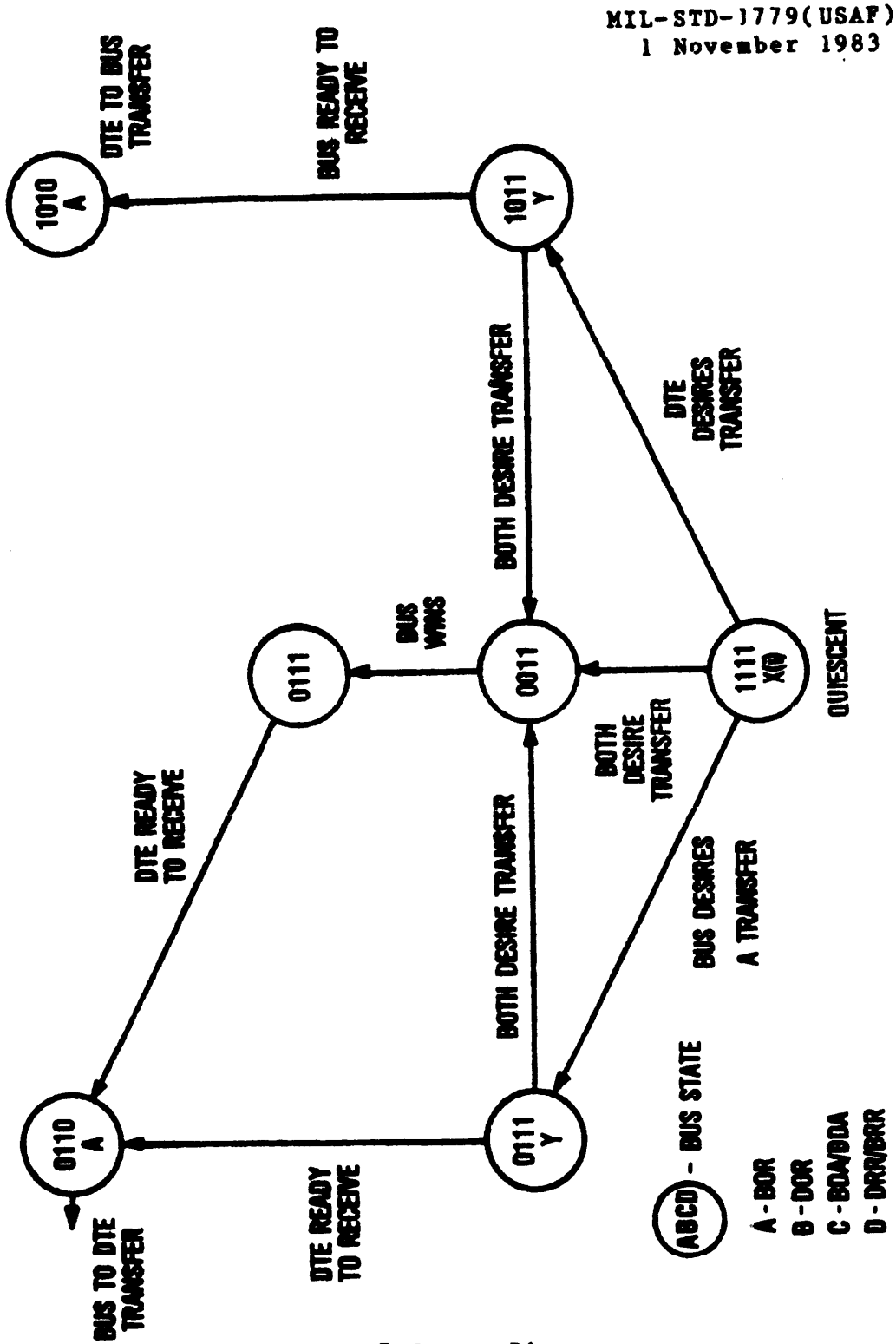


FIGURE 7. State Diagrams-
Bus Arbitration

Downloaded from http://www.everyspec.com

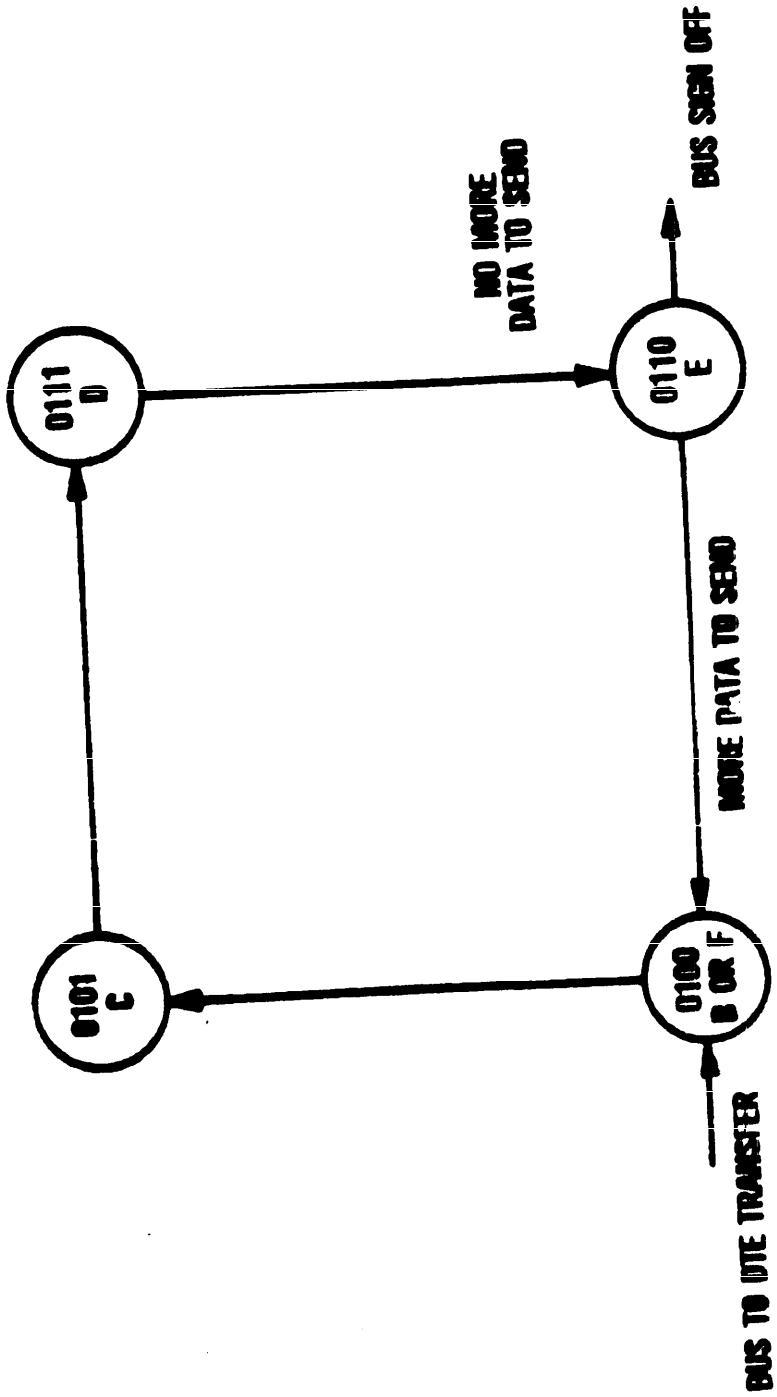


FIGURE 8. State Diagrams-
Bus to DTE

Downloaded from http://www.everyspec.com

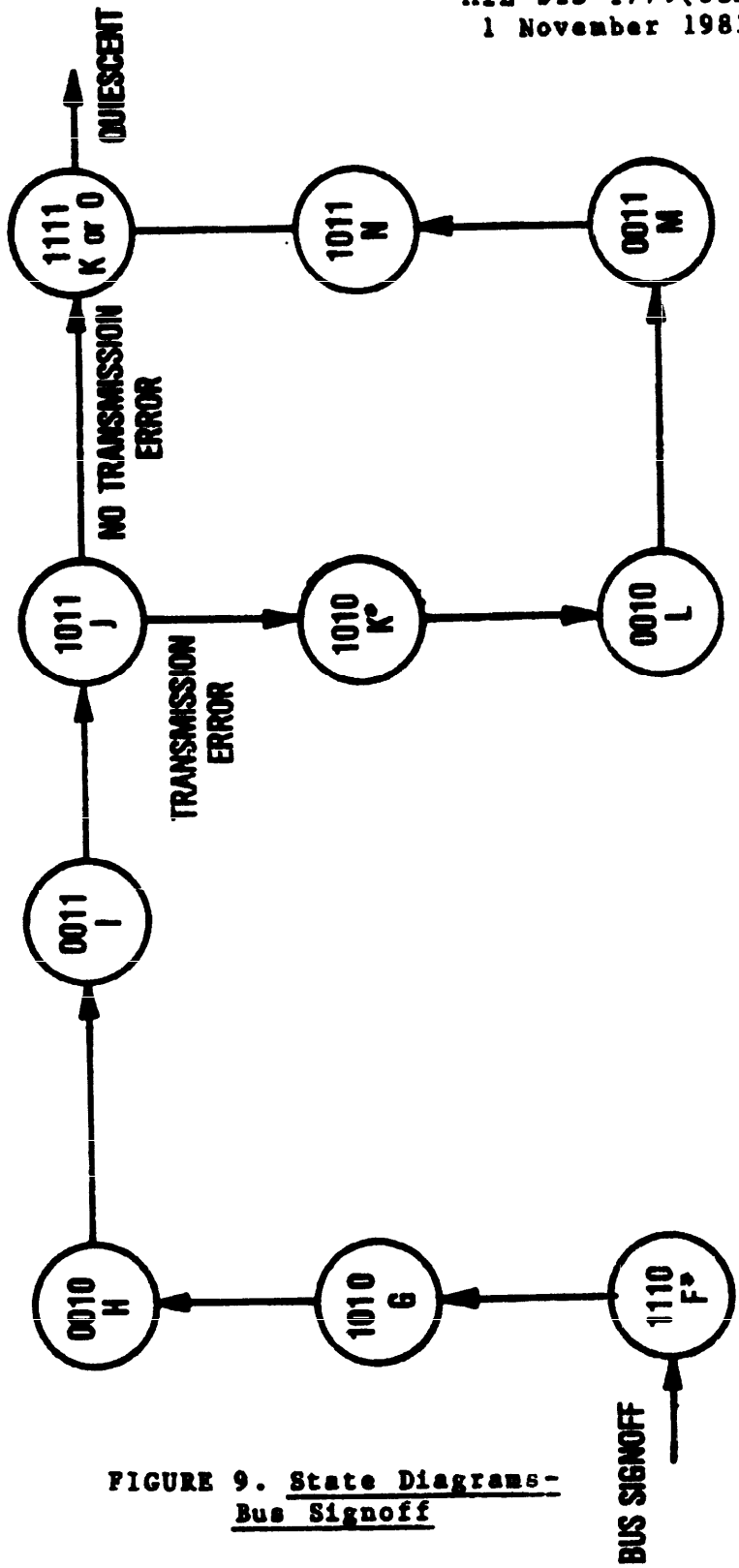


FIGURE 9. State Diagrams-
Bus Signoff

Downloaded from http://www.everyspec.com

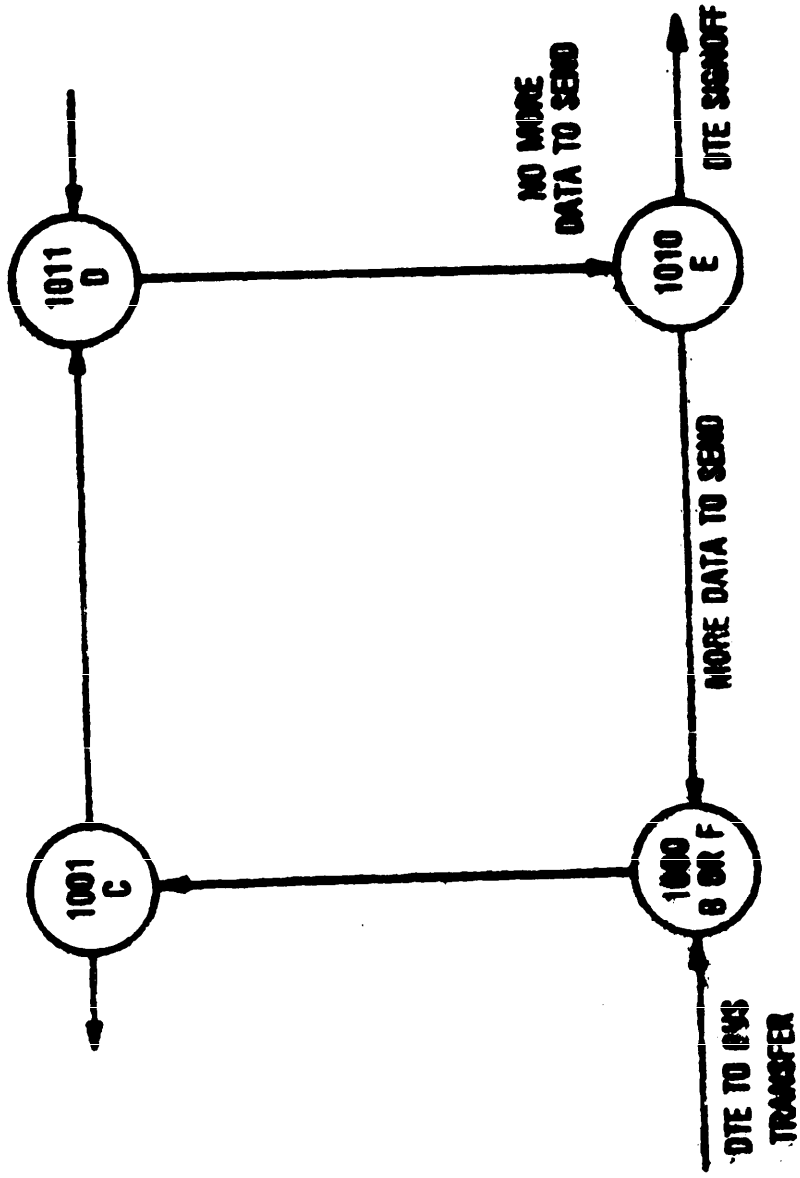


FIGURE 10. State Diagrams-
DTE to Bus

Downloaded from http://www.everyspec.com

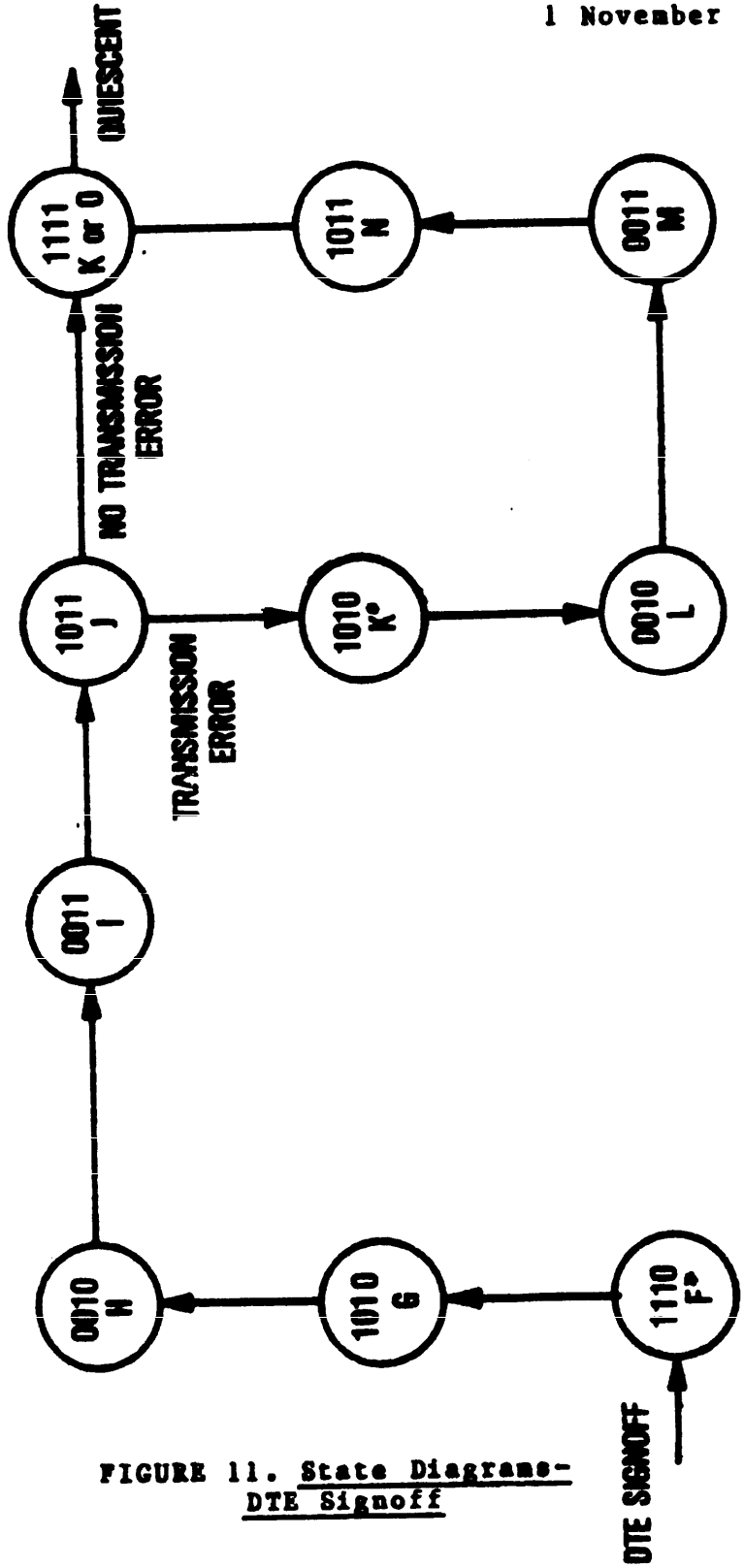
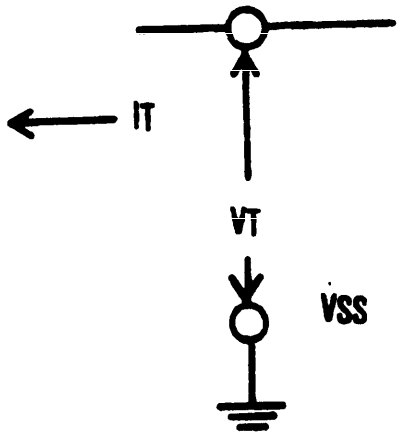


FIGURE 11. State Diagrams-
DTE Signoff

Downloaded from http://www.everyspec.com



I_T Output Current

V_T Logic Voltage

V_{ss} Ground Reference Voltage and Logic Reference Zero

FIGURE 12. Electrical Interface

Downloaded from http://www.everyspec.com

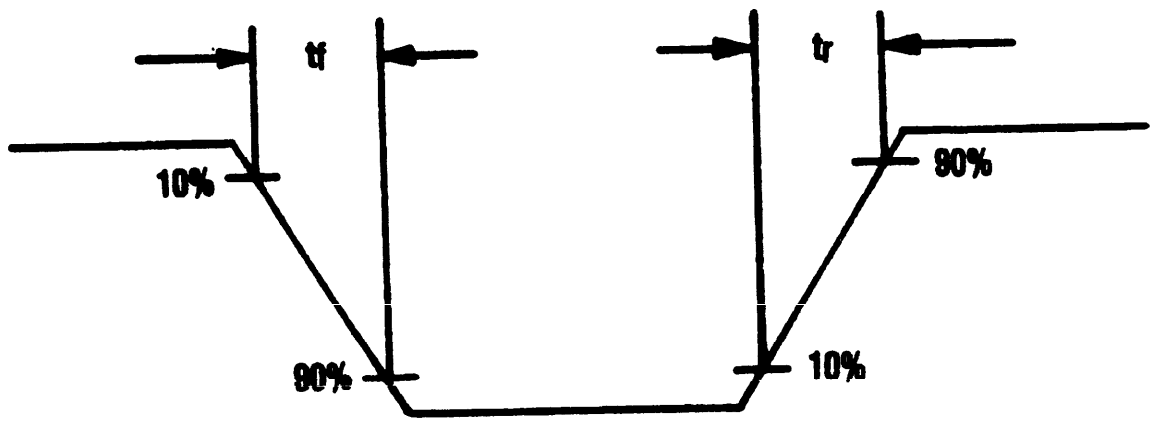


FIGURE 13. Interface Waveshape

Downloaded from http://www.everyspec.com

BDA/DDA		1	26	Signal Ground
		2	27	
Timing Utility		3	28	Signal Ground
Mode Flag		4	29	Signal Ground
BOR		5	30	Signal Ground
DOR		6	31	Signal Ground
DRR/BRR		7	32	Signal Ground
Data Bit	0(LSB)	8	33	Signal Ground
	1	9	34	Signal Ground
	2	10	35	Signal Ground
	3	11	36	Signal Ground
	4	12	37	Signal Ground
	5	13	38	Signal Ground
	6	14	39	Signal Ground
	7	15	40	Signal Ground
	8	16	41	Signal Ground
	9	17	42	Signal Ground
	10	18	43	Signal Ground
	11	19	44	Signal Ground
	12	20	45	Signal Ground
	13	21	46	Signal Ground
	14	22	47	Signal Ground
	15	23	48	Signal Ground
	16	24	49	Signal Ground
Data Bit	17(MSB)	25	50	Signal Ground

Pin Nos.

Connector AMP Part No. 87474-7 or physically and electrically equivalent (and compatible with such mating AMP part on a plug to plug basis.)

FIGURE 14. Physical Digital Interface

Downloaded from http://www.everyspec.com

Header Word	Bit Position / Field Code																	
	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	p	g	g	g	g	a	q	q	q	p	r	r	v	v	v	v	v	v
2	p	u	/	w	w	w	w	w	w	p	/	/	x	x	x	x	x	x
3	p	/	/	y	y	y	y	y	y	p	f	f	z	z	z	z	z	z
4	p	/	/	j	j	j	j	j	j	p	/	/	k	k	k	k	k	k
5	p	/	/	l	l	l	l	l	l	p	d	d	m	m	m	m	m	m
6	p	c	c	c	c	c	c	c	c	p	c	c	c	h	b	b	b	b
7	p	n	n	n	n	n	n	n	n	p	n	n	n	n	n	n	n	n
8	p	s	s	s	s	s	s	s	s	p	s	s	s	s	s	s	s	s
9	p	/	/	/	/	/	/	/	/	p	t	t	t	t	t	t	t	t
10	p	t	t	t	t	t	t	t	t	p	t	t	t	t	t	t	t	t
11	p	t	t	t	t	t	t	t	t	p	t	t	t	t	t	t	t	t
12	p	t	t	t	t	t	t	t	t	p	t	t	t	t	t	t	t	t
13	p	/	/	/	/	/	/	/	/	p	/	/	/	/	/	/	/	/
14	p	/	/	/	/	/	/	/	/	p	/	/	/	/	/	/	/	/
15	p	/	/	/	/	/	/	/	/	p	/	/	/	/	/	/	/	/
16	e	e	e	e	e	e	e	e	e	e	e	e	e	e	e	e	e	e

Field/Size		Definition	Field/Size		Definition
a	1	ACK/NACK mode	n	16	message number
b	4	unused bit count	p	1	lat parity (1/2 wd)
c	11	word count	q	3	system mode
d	2	block sizing code	r	2	priority
e	18	longit parity	s	16	subbus seq no
f	2	header interpret	t	56	system time
g	4	message type	u	1	virtual/real ind
h	1	half word ind	v	6	subbus number
j	6	source virtual address (high)	w	6	destination virtual address (high)
k	6	source virtual address (low)	x	6	destination virtual address (low)
l	6	source real address (high)	y	6	destination real address (high)
m	6	source real address (low)	z	6	destination real address (low)
			/	-	unused bit position

FIGURE 15. Message Header Map and Field Codes.

Downloaded from http://www.everyspec.com

Data Word	Trailer Word(s)
1	1, 8
2	2
3	3
4	4
5	5
6	6
7	7
1	1, 7
2	2, 8
3	3
4	4
5	5
6	6
1	1, 6
2	2, 7
3	3, 8
4	4
5	5

Data Word	Trailer Word(s)
1	1, 5
2	2, 6
3	3, 7
4	4, 8
1	1, 4, 7
2	2, 5, 8
3	3, 6
1	1, 3, 5, 7
2	2, 4, 6, 8
1	1,2,3,4,5,6,7,8
0	All trailer words are set = to all ones

FIGURE 16. Allocation of Trailer Words to Less Than Eight Data Words.

Downloaded from http://www.everyspec.com

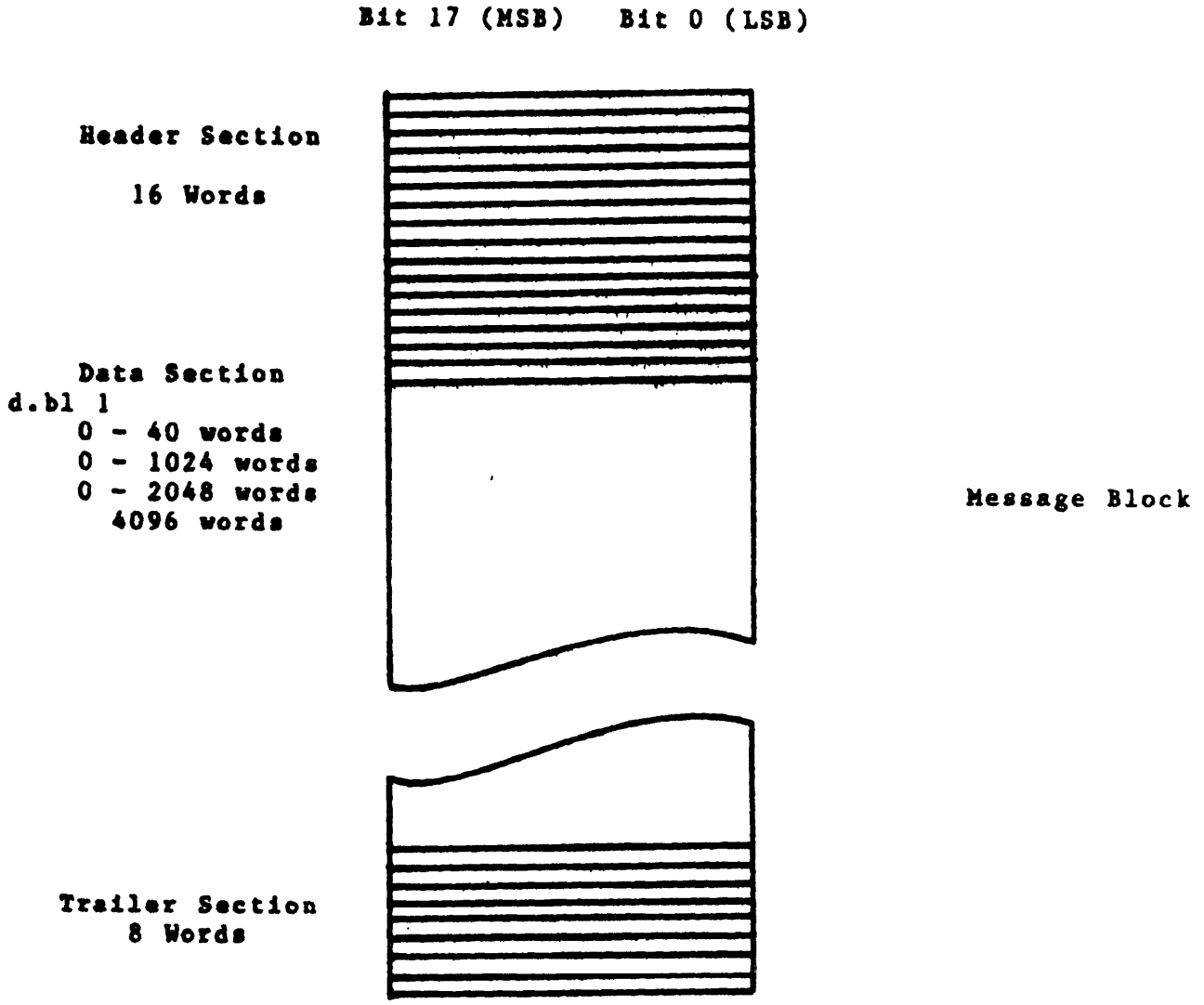


FIGURE 17. Digital Link Interface Message Block Format.

☆U.S. GOVERNMENT PRINTING OFFICE: 1983 785 048 484

Downloaded from http://www.everyspec.com

STANDARDIZATION DOCUMENT IMPROVEMENT PROPOSAL

(See Instructions – Reverse Side)

1. DOCUMENT NUMBER

2. DOCUMENT TITLE

3a. NAME OF SUBMITTING ORGANIZATION

4. TYPE OF ORGANIZATION *(Mark one)*

- ☐ VENDOR
- ☐ USER
- ☐ MANUFACTURER
- ☐ OTHER *(Specify)*: _____

b. ADDRESS *(Street, City, State, ZIP Code)*

5. PROBLEM AREAS

a. Paragraph Number and Wording:

b. Recommended Wording:

c. Reason/Rationale for Recommendation:

6. REMARKS

7a. NAME OF SUBMITTER *(Last, First, MI)* – Optional

b. WORK TELEPHONE NUMBER *(Include Area Code)* – Optional

c. MAILING ADDRESS *(Street, City, State, ZIP Code)* – Optional

8. DATE OF SUBMISSION *(YYMMDD)*

DD FORM 82 MAR 1426

PREVIOUS EDITION IS OBSOLETE.

Downloaded from http://www.everyspec.com

INSTRUCTIONS: In a continuing effort to make our standardization documents better, the DoD provides this form for use in submitting comments and suggestions for improvements. All users of military standardization documents are invited to provide sugg[illegible]s. This form may be detached, folded along the lines indicated, taped along the loose edge *(DO NOT STAPLE)*, and mail[illegible] in block 5, be as specific as possible about particular problem areas such as wording which required interpretation, was too rigid, restrictive, loose, ambiguous, or was incompatible, and give proposed wording changes which would alleviate the problems. Enter in block 6 any remarks not related to a specific paragraph of the document. If block 7 is filled out, an acknowledgement will be mailed to you within 30 days to let you know that your comments were received and are being considered.

NOTE: This form may not be used to request copies of documents, nor to request waivers, deviations, or clarification of specification requirements on current contracts. Comments submitted on this form do not constitute or imply authorization to waive any portion of the referenced document(s) or to amend contractual requirements.

(Fold along this line)

(Fold along this line)

DEPARTMENT OF THE AIR FORCE

RADC/RBE-2
Griffiss AFB NY 13441

OFFICIAL BUSINESS
PENALTY FOR PRIVATE USE $300

NO POSTAGE NECESSARY IF MAILED IN THE UNITED STATES

BUSINESS REPLY MAIL
FIRST CLASS PERMIT NO. 73236 WASHINGTON D. C.
POSTAGE WILL BE PAID BY THE DEPARTMENT OF THE AIR FORCE

Rome Air Development Center
ATTN: RBE-2
Griffiss AFB NY 13441