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MILITARY STANDARD

INPUT / OUTPUT INTERFACES, STANDARD DIGITAL DATA, NAVY SYSTEMS

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DEPARTMENT OF THE NAVY
NAVAL SEA SYSTEMS COMMAND

Washington, DC 20362-5101

Input / Output Interfaces, Standard Digital Data, Navy Systems

1. This Military Standard is approved for use by the Naval Sea Systems Command, Department of the Navy, and is available for use by all Departments and Agencies of the Department of Defense.

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FORWARD

This standard provides guidance for equipment designers as well as systems engineers, and is limited to interface characteristics -- physical, functional, and electrical. This standard does not describe the input/output (I/O) of any equipment. By specifying functional interface requirements, this standard does not specify the specific interface type requirements for any system application; rather it describes functional characteristics of the interface signals.

Appendix A provides information regarding interconnection requirements of this standard. Appendix A contains the general philosophy of the I/O interfaces as specified in this standard.

Appendix B contains special requirements associated with CP-642A/B and CP-789 computers.

Appendix C provides design guidance for Type E interface including: burst transfer mode, error detection, and conformance tests.

For the Type K interface, appendix D defines the Type K interface command set.

Appendix E provides design guidance for Type K interface.

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APPENDICES

1. SCOPE

1.1 Scope. This standard establishes the requirements for the physical, functional, and electrical characteristics of a standard I/O interface for digital data.

1.2 Classification. The digital data interfaces specified herein are classified as follows:

a. Type A (Naval Tactical Data System (NTDS) slow)). Parallel data transfer of up to 41,667 words per second on one cable. Binary voltage levels of 0 volt direct current (Vdc) (logical 1) and -15 Vdc (logical 0).
b. Type B (NTDS fast). Parallel data transfer of up to 250,000 words per second on one cable. Binary voltage levels of 0 Vdc (logical 1) and -3 Vdc (logical 0).
c. Type C (ANEW). Parallel data transfer of up to 250,000 words per second on one cable. Binary voltage levels of 0 Vdc (logical 1) and +3.5 Vdc (logical 0).
d. Type D (NTDS serial) interface. Asynchronous serial data transfer using a 10 megabit per second (Mb/s) data rate. Bipolar ± 3.25 volts nominal.
e. Type E (NATO serial) interface. Asynchronous serial data transfer using a 10 megabit per second (Mb/s) data rate. Bipolar ± 600 mV nominal. Serial data transfer of up to 300,000 words per second in burst transfer mode and 175,000 words per second in single word transfer mode on a 100 foot cable.
f. Type F (aircraft internal time division multiplex bus). MIL-STD-1553B implementation within Navy computers systems.
g. Type G (RS-449 compatible with RS-232). RS-449/RS-232 implementation within Navy computers.
h. Type H (high throughput parallel). Parallel data transfer up to 500,000 words per second on one cable. Binary voltage levels of 0 Vdc (logical 1) and +3.5 Vdc (logical 0).
i. Type J (fiber optic NATO serial). Fiber optic implementation of Type E using four optical fibers.
j. Type K (Small Computer System Interface (SCSI)). Bus interface based on the ANSI X3.131-rev 10h Small Computer System Interface-2 (SCSI-II) standard.

2. REFERENCED DOCUMENTS

2.1 Government documents.

2.1.1 Specifications and standards. Unless otherwise specified, the following specifications and standards form a part of this standard to an extent specified herein. Each is listed in the current Department of Defense Index of Specifications and Standards (DoDISS):

SPECIFICATIONS

MILITARY

MIL-C-17	- Cables, Radio Frequency, Flexible and Semi-rigid, General Specification for.
MIL-C-17/6	- Cables, Radio Frequency, Flexible Coaxial, 75 Ohms, M17/6-RG11, Unarmored, M17/6-RG12, Armored.
MIL-C-17/134	- Cable, Radio Frequency, Triaxial, 0.245 Inch, 50 Ohm, Water Blocked and Non-Water Blocked
MIL-C-17/135	- Cable, Radio Frequency, Triaxial, 50 Ohm, Water Blocked and Non-Water Blocked.
MIL-C-28876	- Connectors, Fiber Optics, J Circular Plug and Receptacle Style, Multiple Removable Termini, General Specification for (Metric).
MIL-C-49142	- Connector, Triaxial, Radio Frequency, General Specification for.
MIL-C-49142/2	- Connectors, Triaxial, Radio Frequency (Series TRC-Receptacle, Pin Contacts, Jam Nut Mounted Class 2).
MIL-C-85045	- Cable, Fiber Optical, Shipboard, General Specification for (Metric).
MIL-F-49291	- Fiber, Optical, General Specification for (Metric).

STANDARDS

MILITARY

DOD-STD-1399 - Interface Standard for Shipboard Systems. Section 406 Digital Computer Grounding. (Metric)
MIL-STD-1310D - Shipboard Bonding, Grounding and other Techniques for Electromagnetic Compatibility and Safety.
MIL-STD-1553B - Aircraft Internal Time Division Command/Response Multiplex Data Bus.

2.1.2 Other Government documents. The following other Government documents forms a part of this standard to the extent specified herein.

INTERNATIONAL STANDARDIZATION AGREEMENT

NATO STANAG 4153 2nd edition -
Standard Specification For an Asynchronous Serial Data Interface for Point to Point Connections and for Connection to Data Networks in NATO Naval Systems.
NATO Allied Naval Engineering Publication (ANEP) 12 -
Throughput Improvement for Systems Implementing the Standard Serial Interface Defined in STANAG 4153
NATO Allied Naval Engineering Publication (ANEP) 13 -
System Integrity Feature Improvements for Systems Implementing the Standard Serial Interface Defined in STANAG 4153
NATO Allied Naval Engineering Publication (ANEP) 35 -
Improved Techniques and Technologies for Ships Implementing the Standard Serial Interface Defined in STANAG 4153

(Copies of specifications, standards, and other Government documents required by contractors in connection with specific acquisition functions should be obtained from the contracting activity.)

2.2 Other publications. The following documents form a part of this standard to the extent specified herein. Unless otherwise specified, use those documents listed in the solicitation's DoDISS. The issues of documents which have not been adopted shall be those in effect on the date of the cited DoDISS.

AMERICAN NATIONAL STANDARDS INSTITUTE (ANSI)

ANSI X3.131-1986 - Small Computer System Interface (SCSI-I).
ANSI X3T9.2/375R -rev 10h - Small Computer System Interface-2 (SCSI-II).

(Application for copies should be addressed to the American National Standards Institute, 1430 Broadway, New York, NY 10018-3308.)

ELECTRONIC INDUSTRIES ASSOCIATION (EIA)

RS-232 - Interface Between Terminal Equipment and Data Circuit-Terminating Equipment Employing Serial Binary Data Interchange.
RS-449 - General Purpose 37-Position and 9-Position Interface for Data Terminal Equipment and Data Circuit Terminating, Equipment Employing Serial Binary Data Interchange, (Including Bulletin No. 12, Application Notes).
RS-485 - Standard for Electrical Characteristics of Generators and Receivers for use in Balanced Digital Multi-point Systems.

(Address applications for copies to the Electronic Industries Association, 2001 Eye Street, NW, Washington, DC 20006.)

(Non-government standards are generally available for reference from libraries. They are also distributed among non-government standards bodies and using Federal agencies.)

2.3 Order of precedence. In the event of a conflict between the text of this standard and the references cited herein, the text of this standard shall take precedence.

3. DEFINITIONS

3.1 General definitions.

3.1.1 External function (EF) data. The EF function transfers command information from the transmitting computer or peripheral equipment to the receiving device using appropriate control signals. The word size and bit format of the EF data shall be specified by the appropriate system design data or the individual equipment specification.

3.1.2 External interrupt (EI) data. The EI function transfers status information from a transmitting device to the receiving computer or peripheral equipment using appropriate control signals. The word size and bit format of the EI data shall be specified by the appropriate system design data or the individual equipment specification.

3.1.3 Full duplex channel. A full duplex channel is comprised of two simultaneous unidirectional channels.

3.1.4 Forced command. A forced command is a command sent by the computer even though the peripheral has not declared that a command is acceptable.

3.1.5 Input. Input refers to input to the computer, except where specifically stated as input to the peripheral or receiving equipment.

3.1.6 Input data (ID). Using appropriate control signals, the ID function receives information from a transmitting device by the receiving computer or peripheral equipment. The word size and bit format of the ID shall be specified by the appropriate system design data or the individual equipment specification.

3.1.7 Input/output (I/O). A digital word of specified number of bits, which has been agreed upon as the basic unit of communication between interconnected units.

3.1.8 Odd parity. Odd parity is the inclusion of an additional bit (the parity bit) to the data word for error detection using the following criteria: if the number of bits in the data unit being logical one is even, the parity bit shall be set to logical one; or if the number of bits in the data unit being logical one is odd, the parity bit shall be set to logical zero.

3.1.9 Output. Output refers to output from the computer, except where specifically stated as output from the peripheral equipment or data source.

3.1.10 Output data (OD). The OD function transfers information from a transmitting computer or peripheral equipment to the receiving device using appropriate control signals. The word size and bit format of the OD shall be specified by the appropriate system design data or the individual equipment specification.

3.1.11 Single pulsed signals. Any signal which exists in the stable "one" state for a limited time, regardless of the duration of the input or inputs to the circuit used to generate that signal.

3.1.12 Throughput. Throughput is the number of data words that are transmitted over the channel per unit of time. For parallel interfaces, this is independent of the data word size. For serial interfaces, this is directly related to the size of the data word. Larger data words require more time for transmission at a fixed serial data rate. For either parallel or serial interfaces, the throughput includes all timing caused by handshaking or other overhead functions.

3.1.13 Timeout. A timeout is the failure to complete a timed function within the specified time.

3.1.14 Unidirectional channel (simplex). A unidirectional channel is one-half of a full duplex channel in which information is sent in one direction only, but control signals (handshake) can be sent in both directions.

3.2 Type E definitions.

3.2.1 Burst transfer. Burst transfer occurs when an IF has one S bit, one WI bit, and a multiple number of information words (IWs).

3.2.2 Channel. A channel is a facility that permits information to be sent from one unit to another unit. It includes transceivers and control circuits at both ends, and the cable between.

3.2.3 Command/interrupt word (CIW). A CIW is used to transfer commands from the source to the sink. External functions (EFs) are sent as CIWs over low level serial (LLS) cables.

3.2.4 Control frames. Control frames transfer control information over a unidirectional channel. There are two types of control frames: The source status (SOS) control frame, originating at the source, and the sink status (SIS) control frame, originating at the sink.

3.2.4.1 Source status (SOS) control frame. The SOS control frame advises on the availability of an IF at the source for transmission to the sink.

3.2.4.2 Sink status (SIS) control frame. The SIS control frame advises on the acceptability of an IF by the sink.

3.2.5 Information frames (IFs). When using single word transfer (SWT), an IF consists of a synchronization bit (S), a word identifier bit (WI), a 32-bit word, and an optional parity bit (P). The WI bit identifies the 32-bit word as either a command/interrupt word (CIW) or a data word. When using burst transfer, an IF consists of a S bit, a WI bit, and a multiple number of IWs including an optional parity bits.

3.2.6 Serial data rate. The serial data rate is the clock rate at which data bits are transmitted on the cable. The serial data rate is not a throughput definition because throughput is dependent upon both data word size and overhead (handshaking) implementations.

3.2.7 Single word transfer (SWT). SWT occurs when an IF has one S bit, one WI bit, and one information word (IW).

3.2.8 Sink. The sink is that end of a unidirectional channel that receives information frames (IFs).

3.2.9 Source. The source is that end of a unidirectional channel that transmits information frames (IFs).

3.2.10 System integrity features (SIFs). SIFs are those additional features, such as parity or timeouts, that are included as part of the implementation of STANAG 4153 2nd Edition. These features are not to affect the defined characteristics of STANAG 4153 2nd Edition, but are to provide error detection capability for the system employing these channels.

3.3 Type J definitions.

3.3.1 Attenuation (optical). Optical power loss, expressed in decibels.

3.3.2 Bit error ratio (BER). The ratio of incorrectly transmitted bits to the total number of transmitted bits.

3.3.3 Connector plug. A device used to terminate optical fibers.

3.3.4 Connector receptacle. The fixed half of a connection that is mounted on a panel/bulkhead. Receptacles mate with plugs.

3.3.5 Fiber. Dielectric structure that guides light: optical wave guide.

3.3.6 Fiber optic cable. A cable containing one or more optical fibers.

3.3.7 Graded index. A type of multimode optical fiber in which the chemical composition of the fiber core is not uniform. Graded index composition results in a non-uniform refractive index which bends light towards the fiber's core, increasing the fiber's bandwidth.

3.3.8 Multimode. In an optical fiber, a method of light propagation where all light rays do not travel in a path parallel to the axis of the fiber. These rays travel paths which cause differences in transit times which in turn limit the bandwidth a multimode fiber can transmit.

3.3.9 Optical fall time. The time interval for the falling edge of an optical pulse to transition from 90% to 10% of the pulse amplitude.

3.3.10 Optical rise time. The time interval for the rising edge of an optical pulse to transition from 10% to 90% of the pulse amplitude.

3.3.11 Power (optical). The radiant power, expressed in watts.

3.3.12 Receiver (optical). An opto-electronic circuit that converts an optical signal to an electrical logic signal.

3.3.13 Spectral width Full Width Half Maximum (FWHM). The absolute difference between the wavelengths, at which the spectral radiant intensity is 50% of the maximum power.

3.3.14 Transmitter (optical). An opto-electrical circuit that converts an electrical logic signal to an optical signal.

3.4 Type K definitions.

3.4.1 Average measured composite DC voltage (V_{AM}). The average measured composite DC voltage shall be the sum of the following four DC voltage levels divided by four:

SIGNAL(+) before the logic state transition,
SIGNAL(-) before the logic state transition,
SIGNAL(+) after the logic state transition,
SIGNAL(-) after the logic state transition.

3.4.2 SCSI-I. SCSI-I (Small Computer Systems Interface I) shall specifically refer to ANSI X3.131/1986 standard.

3.4.3 SCSI-II. SCSI-II (Small Computer Systems Interface II) shall specifically refer to ANSI X3T9.2/375 standard.

3.4.4 Stub. The stub is the interconnection length of the internal cable (including but not limited to wires, connector pins and circuit board traces) required to convey signals from the transceiver circuitry to the Type K bus.

3.5 Acronyms. Acronyms used in this standard are defined as follows:

BER	Bit Error Ratio
CIW	Command/Interrupt Word
DoD	Department of Defense
DoDISS	Department of Defense Index of Specifications and Standards
EF	External Function
EFA	External Function Acknowledge
EFE	External Function Enable
EFR	External Function Request
EI	External Interrupt
EIE	External Interrupt Enable
EIR	External Interrupt Request
ESA	Externally Specified Address
ESI	Externally Specified Index
FWHM	Full Width Half Maximum
IA	Input Acknowledge
IACW	Initial Address Control Word
IC	Intercomputer
ID	Input Data
IDA	Input Data Acknowledge
IDE	Input Data Enable
IDR	Input Data Request
IECF	Input Enable Control Frame
IF	Information Frame
I/O	Input/Output
IRCF	Input Request Control Frame
IW	Information Word
LLS	Low Level Serial
LLSIO	Low Level Serial Input/Output
NA	Numerical Aperture
NATO	North Atlantic Treaty Organization
NTDS	Naval Tactical Data System
OD	Output Data
ODA	Output Data Acknowledge
ODE	Output Data Enable
ODR	Output Data Request
OECF	Output Enable Control Frame
ORCF	Output Request Control Frame
P	Parity (bit)
S	Synchronization (bit)
SCSI	Small Computer Systems Interface
SIF	System Integrity Features
SIS	Sink Status
SOS	Source Status
SWT	Single Word Transfer
TACW	Terminal Address Control Word
WI	Word Identifier

4. GENERAL REQUIREMENTS

4.1 I/O control and data signal categories. The I/O requirements specified herein include control and data signal definitions and timing requirements. The control signal definitions are tailored to the functional categories of equipment being interconnected. The categories of equipment combinations that require interface definitions are:

a.. Category I - Computer to peripheral
b. Category II - Computer to computer, intercomputer (IC)
c. Category III - Peripheral to peripheral

4.2 Parallel interface physical requirements. Unless otherwise specified in the equipment specification, the physical interface for parallel category I, II, and III interfaces shall consist of the interconnection of compatible equipments by means of a pair of cables. The interconnected equipment shall transfer ID and associated control signals on one cable and shall transfer OD and associated control signals on the other cable. The connector types, connector pin assignments, and cable type are provided for information only in appendix A. Special requirements unique to particular computer interface are specified in appendix B.

4.3 Grounding. The systems ground installation for interface Types A, B, C, and H shall meet the requirements specified in DOD-STD-1399, section 406. For grounding requirements for Type D NTDS serial I/O cables, see 5.3.9.1. The grounding requirements for Type E interface shall be as specified in 5.4.5.5 and in DOD-STD-1399, section 406. For grounding requirements for Type K interface, see 5.8.1.6.3.7.

4.4 Programming considerations.

4.4.1 Peripheral equipment. Restrictions to the possible rate of forced EF shall be specified for the peripheral equipment if it cannot accept forced EF at the maximum rate specified herein.

4.4.2 Intercomputer (IC). Forced EF may be lost when used for IC operation. Therefore, IC forced EF should be used only when it is the only possible method of communication. If forced EF are required for IC operation, steps shall be taken to ensure the interrupts are not locked out in the receiving computer and the input register is available when the forced EF is transmitted from the transmitting computer. Forced EF words may be transmitted even though the Output Request Control Frame (ORCF) External Interrupt Enable (EIE) does not specify the External Function Request (EFR) control function. The receiving computer will not accept the EI word (forced EF word from the transmitting computer) if the input register is not available.

4.4.3 IC channels. The conversion from a standard computer peripheral channel (category I) interface to an IC communication channel (category II) interface requires I/O circuit changes of varying complexities within the computer. The required circuit changes to convert a category I interface to a category II interface shall be accomplished by means of switches, printed circuit card changes, or chassis change. The changes required to convert a category I interface to category II interface shall consist of the following as specified in the individual equipment specification:

a. Only the output channel is affected.
b. The output control signals category I (External Function Acknowledge (EFA), Output Data Acknowledge (ODA), and Output Data Request (ODR)) take on different names and functions in a category II interface.
c. The signal line in a category I interface that carries the ODA shall be used to carry the category II Ready signal. The category II Ready line is not single pulsed as is the category I ODA. The Ready signal in a category II interface is set in accordance with the requirements of 5.1.2.3.b. The Ready signal in a category II interface shall be cleared by the Resume signal (category I ODR) as specified in 5.1.2.3.f and g.
d. The signal line in a category I interface that carries the ODR shall be used to carry the category II Resume signal.

e. The category I EFA signal retains the same name in a category II interface as it is in a category I interface. The EFA signal in a category II interface shall be set as specified in 5.1.2.1.c and d. The EFA signal in a category II interface shall be cleared by the receipt of a Resume signal (category I ODR) as specified in 5.1.2.1 i and j.

f. There shall be no change in the name, function, or operation of the category I EFA signal or OD lines for a category II interface.

4.4.4 IC timeout interrupt. When transferring either external function words or output data words in the intercomputer mode, if the transmitting computer does not receive an acknowledge from the receiving computer within a specified time, an IC timeout interrupt shall be generated.

5. DETAILED REQUIREMENTS

5.1 Parallel interface functional requirements. Type A, B, C, and H parallel interface characteristics shall be the same, except for the timing and electrical requirements. Type A, B, C, and H interfaces shall each have three functional classifications: categories I, II, and III (see 4.1).

5.1.1 Category I, sequence of I/O events. An I/O channel between a computer and peripheral shall transfer control words and data words by means of the reciprocal interaction specified herein for each form of communication.

5.1.1.1 Output communication. When interconnected as shown on figure 1, a computer and a peripheral equipment shall transfer data from the computer to the peripheral equipment as specified herein. Output channel control lines shall function as specified in table I.

TABLE I. Function of output channel control lines.

Name of line	Direction of signal	Function
EFR1/	Peripheral equipment to computer	Set condition indicates readiness of the peripheral equipment to accept an EF code word on that channel.
EFA2/	Computer to peripheral equipment	Set condition indicates the computer has placed an EF code word on the OD lines of that channel.
ODR	Peripheral equipment to computer	Set condition indicates readiness of the peripheral equipment to accept a data word on that channel.
ODA2/	Computer to peripheral equipment	Set condition indicates the computer has placed a data word on the OD lines of that channel.

1/ Not all computers have the EFR line; see individual equipment specification.

2/ Signals on the output data lines shall be settled to their intended values before the EFA or ODA line is set by the computer.

5.1.1.1.1 Transfer of a buffer EF code word. Whenever an EF buffer has been established for a channel, the computer and the peripheral equipment on that channel shall transfer EF code word as follows:

a. When the peripheral equipment is ready to accept an EF code word, the peripheral equipment shall set the EFR line (this may have already happened before the EF buffer was established).
b. The computer shall detect the setting of the EFR line in accordance with internal priority.
c. The computer shall place an EF code word on the OD lines.
d. The computer shall set the EFA line (to indicate that the EF code word is on the OD lines).
e. The peripheral equipment shall detect the setting of the EFA line. (The peripheral equipment may clear the EFR line any time after detecting the setting of the EFA line, but shall clear the EFR line before the computer will recognize the next EFR.)
f. The peripheral equipment shall sample the EF code word that is on the OD lines.
g. The computer shall clear the EFA line before placing the next word on the OD lines.

The computer and the peripheral shall repeat this sequence for each successive EF code word until they have transferred the block of code words specified by the EF buffer control words. Peripheral devices designed to meet the requirements for transfer of buffered EF code word shall also meet the requirements for transfer of a forced EF code word.

5.1.1.1.2 Transfer of a forced EF code word. Whenever the current instruction of the computer program is a forced EF, the computer and the peripheral equipment on the designated channel shall transfer a single EF code word as specified in 5.1.1.1.1, except that the EFR line is not involved. The transfer shall proceed whether or not the EFR line is set. Peripheral equipment that does not have the EFR line shall transfer an EF code word as follows:

a. The computer shall place a word of data on the OD lines.
b. The computer shall set the EFA line (to indicate that the EF code word is on the OD lines).
c. The peripheral equipment shall detect the setting of the EFA line.
d. The peripheral equipment shall sample the EF code word that is on the OD lines.
e. The computer shall clear the EFA line before placing the next word on the OD lines.

The peripheral equipment specification shall state the maximum rate at which the peripheral equipment is to accept forced EF whenever the rate is less than the maximum rate possible from the computer. Programming restrictions shall be imposed for peripheral equipment that cannot accept forced EF at the maximum rate possible from the computer.

5.1.1.1.3 Transfer of OD. Whenever an OD buffer has been established for a channel, the computer and the peripheral equipment on that channel shall transfer data as follows:

a. When the peripheral equipment is ready to accept data, the peripheral equipment shall set the ODR line (this may already have happened before the OD buffer was established).
b. The computer shall detect the setting of the ODR line in accordance with internal priorities.
c. The computer shall place a word of data on the OD lines.
d. The computer shall set the ODA line to indicate that a word of data is on the OD lines.
e. The peripheral equipment shall detect the setting of the ODA lines. (The peripheral equipment may clear the ODR line any time after detecting the setting of the ODA line, but shall clear the ODR line before the computer will recognize the next ODR.)
f. The peripheral equipment shall sample the data word that is on the OD lines.
g. The computer shall clear the ODA line before placing the next word on the OD lines.

The computer and the peripheral equipment shall repeat this sequence for each successive word of data until all words have been transferred.

5.1.1.2 Input communication. When interconnected as shown on figure 2, the computer and peripheral equipment shall transfer data from the peripheral equipment to the computer as specified herein. Input channel control lines shall function as specified in table II.

TABLE II. Function of input channel control lines.

Name of line	Direction of signal	Function
EIE1/	Computer to peripheral equipment	Set condition indicates readiness of the computer to accept an EI code word on that channel.
IDR2/	Peripheral equipment to computer	Set condition indicates that the peripheral equipment has placed a word of data available to the computer on the ID lines of that channel.
EIR2/	Peripheral equipment to computer	Set condition indicates the peripheral equipment has placed an interrupt code word available to the computer on the ID lines of that channel.
IDA	Computer to peripheral equipment	Set condition indicates that the computer has sampled the ID lines of that channel.

1/ Not all computers have the EIE line; see individual equipment specification.
2/ Signals on the input data lines from the peripheral equipment shall be settled to their intended values before the Input Data Request (IDR) or External Interrupt Request (EIR) is set by the peripheral.

5.1.1.2.1 Transfer of an EI code word with EIE. The computer and a peripheral equipment shall transfer an EI code word in the following steps:

a. The computer, under program control, shall set the EIE line when ready to accept an EI.
b. The peripheral equipment shall detect the state of the EIE line.
c. When the status requires that the computer be interrupted, the peripheral equipment shall place an EI code word on the ID lines.
d. The peripheral equipment shall set the EIR line to indicate that the EI code word is on the ID lines.
e. The computer shall detect the setting of the EIR line in accordance with internal priorities.
f. The computer shall sample the EI code word that is on the ID lines.
g. The computer shall clear the EIE line.
h. The computer shall set the Input Data Acknowledge (IDA) line.
i. The peripheral equipment shall detect step "h" or both steps "g" and "h". (The peripheral equipment may clear the EIR line any time after detecting the setting of the IDA line, but shall clear the EIR line before the computer will recognize the next EIR.)
j. The computer shall clear the IDA line before sampling the next word on the ID lines.

The computer and peripheral equipment shall repeat this sequence for each successive EI code word for non-buffered interrupt transfers, or until they have transferred the block of interrupt code words.

5.1.1.2.2 Transfer of an EI code word without the EIE. The computer and a peripheral equipment shall transfer an EI code word in the following steps:

a. When the status requires that the computer be interrupted, the peripheral equipment shall place an EI code word on the ID lines.
b. The peripheral equipment shall set the EIR line to indicate that the EI code word is on the ID lines.
c. The computer shall detect the setting of the EIR line in accordance with internal priorities.
d. The computer shall sample the EI code word that is on the ID lines.
e. The computer shall set the IDA line.
f. The peripheral equipment shall detect step "e". (The peripheral equipment may clear the EIR line any time after detecting the setting of the IDA line, but shall clear the EIR line before the computer will recognize the next EIR.)
g. The computer shall clear the IDA line before sampling the next word on the ID lines.

Any peripheral device constructed to meet the requirements specified in 5.1.1.2.1 shall also meet the requirements specified in 5.1.1.2.2. In order to meet these requirements, peripheral equipment constructed to use the EIE shall be constructed to either simulate the EIE or disable the circuits that detect the EIE.

5.1.1.2.3 Transfer of ID. Whenever an ID buffer has been established for a channel, the computer and the peripheral equipment on that channel shall transfer data as follows:

a. The peripheral equipment shall place word of data on the ID lines.
b. The peripheral equipment shall set the IDR line to indicate that a word of data is on the ID lines.
c. The computer shall detect the setting of the IDR line in accordance with internal priorities.
d. The computer shall sample the data word that is on the ID lines.
e. The computer shall set the IDA line, indicating that it has sampled the data word on the ID lines.
f. The peripheral equipment shall detect the setting of the IDA line. (The peripheral equipment may clear the IDR line any time after detecting the setting of the IDA line, but shall clear the IDR before the computer will recognize the next IDR.)
g. The computer shall clear the IDA line before reading the next word on the ID lines.

The computer and peripheral equipment shall repeat this sequence for each successive word of data until they have transferred the block of data words specified by the input buffer control words.

5.1.1.3 Externally specified indexing (ESI). (Not all equipment have the ESI mode, see individual equipment specification.) ESI is a mode of I/O whereby a peripheral equipment can, under its control, send data to or receive data from one of any number of assigned storage areas in the computer's memory. In the ESI mode, data transfers are governed by buffer control words specified through an index provided by the peripheral device. The index points to an ESI accessible address in main memory that contains the buffer control word used to control the data transfer for that peripheral device. Under ESI control, buffer sizes shall be limited by the length of the buffer control word which is a function of the main memory word length. Because of the memory address structures in some computers, it may not be possible in ESI mode to access all of main memory. Any I/O channel shall be capable of ESI buffer mode operation. ESI data transfers shall be identical to normal buffer mode data transfers, except that the external device shall specify the index address in accordance with procedures for the particular computer.

5.1.1.3.1 ESI ID buffer. Whenever an ESI ID buffer has been established for a channel, the computer and the peripheral equipment on that channel shall transfer data as follows:

a. The peripheral equipment shall place the ESI address on the lower half of the ID lines and a word of data on the upper half of the ID lines.
b. The peripheral equipment shall set the IDR line to indicate that an ESI index address and a word of data is on the ID lines.
c. The computer shall detect the setting of the IDR line in accordance with internal priorities.
d. The computer shall sample the ESI address and the data word that is on the ID lines.
e. The computer shall read the buffer control words specified by the ESI address and shall store the data word as specified by the buffer control words. Then the IDA line shall be set, indicating that the ESI address and the data word on the ID lines has been sampled, and that the buffer control words specified by the ESI index have been updated and restored.
f. The peripheral equipment shall detect the setting of the IDA line. (The peripheral equipment may clear the IDR line any time after detecting the setting of the IDA line, but shall clear the IDR before the computer will recognize the next IDR).
g. The computer shall clear the IDA line before reading the next ESI address and data word on the ID line.

The computer and peripheral equipment shall repeat this sequence for each successive ESI address and data word until they have transferred the block of data words specified by any one of the ESI input buffer control words, at which time the input shall automatically terminate.

5.1.1.3.2 ESI OD buffer. Whenever an ESI OD buffer has been established for a channel, the computer and the peripheral equipment on that channel shall transfer data as follows:

a. When the peripheral equipment is ready to accept data, the peripheral equipment shall place the ESI output address on the ID lines and set the ODR line (this may already have happened before the OD buffer was established).
b. The computer shall detect the setting of the ODR line in accordance with internal priorities.
c. Upon detection of the ODR, the computer shall read the ESI output address present on the ID lines. (This will cause the computer to read the appropriate buffer, control words, output the word from the appropriate buffer, and update and restore the buffer control words.)
d. The computer shall place a word of data, from the appropriate buffer, on the OD lines.
e. The computer shall set the ODA line to indicate that a word of data is on the OD lines.
f. The peripheral equipment shall detect the setting of the ODA line. (The peripheral equipment may clear the ODR line any time after detecting the setting of the ODA line, but shall clear the ODR line before the computer will recognize the next ODR.)
g. The peripheral equipment shall sample the data word that is on the OD lines.
h. The computer shall clear the ODA line before placing the next word on the OD lines.

The computer and the peripheral equipment shall repeat this sequence for each successive word of data until they have transferred a block of data words as specified by one of the ESI output buffer control words, at which time the output shall be automatically terminated.

5.1.1.4 Externally specified addressing (ESA). (Not all equipments have the ESA mode, see individual equipment specifications.) Any I/O channel shall be capable of externally specified addressing operations. (The selection of ESA mode shall be accomplished through switch selection, printed circuit card changes, or chassis changes, and shall be specified in the individual equipment specification.) An ESA mode shall provide peripheral devices with a means of specifying an absolute memory location for storage or retrieval of data on a word-by-word basis. An ESA input (input or EI) active channel shall respond to an input request (input or EI) as follows. The lower one-half of the input lines shall be sampled to determine the memory address into which the data is to be stored. The data on the ID lines shall be stored at the address (only the upper one-half of the input lines shall contain significant data; the lower one-half of the input lines shall contain the memory address). An ESA output (output or EF) active channel shall respond to an output request (output or EF) as follows. The lower one-half of the input lines shall be sampled to determine the memory address that contains the data. The content of that memory location shall be transmitted to the output channel.

5.1.2 Category II, sequence of I/O events. When connected as shown on figure 3, two computers shall transfer data, as specified herein. IC channel control lines shall function as specified in table III.

TABLE III. Function of IC channel control lines.

Receiving computer line	Transmitting computer line	Direction of signal	Function
EIE1/	EFR	Receiving computer to transmitting computer	Set condition indicates readiness of the receiving computer to accept an EF command word on that channel.
IDR	Ready (ODA)	Transmitting computer to receiving computer	Set condition indicates that the transmitting computer has placed a word of data on the OD lines of that channel.
EIR	EFA	Transmitting computer to receiving computer	Set condition indicates the transmitting computer has placed an EF command word on the OD lines of that channel.
IDA	Resume (ODR)	Receiving computer to transmitting computer	Set condition indicates the receiving computer has sampled the ID lines of that channel.

1/ Not all computers have the EIE line; see the individual equipment specification.

The computer that is outputting data is defined as the transmitting computer. The computer that is receiving the data being outputted by the transmitting computer is defined as the receiving computer.

5.1.2.1 Transfer of buffered command words. Whenever the transmitting computer has an EFR line and the receiving computer has an EIE line, then transfer of buffered command words shall be possible. Whenever an EF buffer has been established in the transmitting computer for a channel, the transmitting computer and the receiving computer shall transfer a command word as follows:

a. When the receiving computer is ready to accept an EF command word, the receiving computer, under program control, shall set the EIE line.
b. In accordance with internal priority, the transmitting computer shall detect the setting of the EIE line (which will be recognized as the EFR line).
c. The transmitting computer shall place an EF command word on the OD lines. The EF command word shall be held on the data lines until the receiving computer sets the Resume line or until the transmitting computer program intervenes to resolve the no Resume condition.
d. The transmitting computer shall set the EFA line to indicate that the EF command word is on the OD lines.
e. In accordance with internal priorities, the receiving computer shall detect the setting of the EFA line of the transmitting computer (which will be recognized as the EIR line).
f. The receiving computer shall sample the ID lines.
g. The receiving computer shall clear the EIE line.
h. The receiving computer shall set the IDA line.
i. The transmitting computer shall detect the setting of the IDA line of the receiving computer (which will be recognized as the Resume line).
j. The transmitting computer shall clear EFA line before placing the next word on the OD lines, and the receiving computer shall clear the IDA line before reading the next word on the ID lines.

The transmitting and receiving computers shall repeat this sequence for each successive command word until they have transferred the block of command words specified by the transmitting computer EF buffer control words. In the event that the receiving computer is capable of buffered EI transfers, then the receiving computer's EI buffer control words shall specify a buffer length equal to the transmitting computer's EF buffer length.

5.1.2.2 Transfer of a forced command word. Whenever the transmitting computer does not have an EFR line, or the receiving computer does not have an EIE line, then a command word shall be transferred with force. Whenever the current instruction of the transmitting computer program is a forced EF, that computer shall transfer a single command word to the other computer as follows:

a. The transmitting computer shall place an EF command word on the OD lines. The EF command word shall be held on the data lines until the receiving computer sets the Resume line, or until the transmitting computer program intervenes to resolve the no-Resume condition.
b. The transmitting computer shall set the EFA line to indicate that a command word is on the data lines.
c. In accordance with internal priorities, the receiving computer shall detect the setting of the EFA line of the transmitting computer (which will be recognized as the EIR line).
d. The receiving computer shall sample the ID lines.
e. The receiving computer shall set the IDA line.
f. The transmitting computer shall detect the setting of the IDA line of the receiving computer (which will be recognized as the Resume line).
g. The transmitting computer shall clear the EFA line before placing the next word on the OD lines, and the receiving computer shall clear the IDA line before sampling the next word on the ID lines.

5.1.2.3 Transfer of data. Whenever an OD buffer has been established in the transmitting computer and an ID buffer has been established in the receiving computer for the same channel, the transmitting computer and the receiving computer shall transfer data as follows:

a. The transmitting computer shall place a word of data on the OD lines. The OD word shall be held on the data lines until the receiving computer sets the Resume line, or until the transmitting computer program intervenes to resolve the no-Resume condition.
b. The transmitting computer shall set the Ready line to indicate that a word of data is on the OD lines.
c. In accordance with internal priorities, the receiving computer shall detect the setting of the Ready line of the transmitting computer (which will be recognized as the IDR line).
d. The receiving computer shall sample the ID lines.
e. The receiving computer shall set the IDA line.
f. The transmitting computer shall detect the setting of the IDA line of the receiving computer (which will be recognized as the Resume line).
g. The transmitting computer shall clear the Ready line before placing the next word of data on the OD lines, and the receiving computer shall clear the IDA line before sampling the next word on the ID lines.

The computers shall repeat this sequence until they have transferred the block of words specified by the buffer control words. Buffer lengths specified by both computers shall be the same.

5.1.3 Category III, sequence of I/O events. The category III interface shall require one of the peripherals to perform the function of the computer as specified for category I interface (see 5.1.1). The I/O interface between a peripheral-peripheral shall transfer control and data words by means of the reciprocal interaction as specified for category I (see 5.1.1).

5.2 Parallel interface, electrical. The following general rules shall apply to each of the categories for each interface Type A, B, C, and H:

a. Data signals (parallel) - the actual state (binary one or zero) of the data lines shall be detected by sensing the dc level rather than by detecting a change from binary zero to binary one (as in the case for control signals, see 5.2 b). Therefore, the lines need not be cleared between successive words as is the case with control lines. The data on the data lines shall be stable at the time the lines are sampled.
b. Control signals - Equipment, either computer or peripheral, shall recognize each binary one received on any control line by detecting the voltage change of the signal. The equipment, either computer or peripheral, shall not recognize another binary one on that control line until the circuits have been cleared by a binary zero on that control line is again set to binary one. Control signals shall be logically detected as specified herein.
c. Output - For output, the computer shall provide a delay between gating data to the output lines and setting the ODA or EFA lines. This shall ensure that data signals are stable for sampling any time the ODA or EFA lines are set. Once set by the peripheral equipment, the ODR and EFR signals shall remain set until the computer sets the corresponding acknowledge line (ODA for ODR; EFA for EFR).
d. Input - Once the IDR or EIR has been set, the peripheral equipment shall not change the state of the ID lines before the computer has acknowledged the request. The only exceptions are that the IDR or EIR may be cleared before the IDA is received, if the possible loss of data is of secondary importance.

5.2.1 Type A interface. The Type A (NTDS slow) interface shall be characterized by nominal values of 0 Vdc and -15 Vdc to represent binary one and binary zero, respectively, and by a switching threshold of -6.0 ± 1.5 Vdc. Parallel data transfer shall consist of up to 41,667 words per second on one cable.

5.2.1.1 Type A timing. Duration of signals and timing between signals in the communication sequence shall conform to the applicable limits shown on figures 4 through 7. The limits are expressed as absolute minimums or absolute maximums and shall denote the following requirements:

a. Neither the initiation nor the termination of any control or data signal shall occur sooner than specified on figures 4 through 7.
b. Each equipment shall recognize data and control signals that occur at the times specified, or at any time later than the times specified and that exist for any duration equal to or greater than the duration specified.
c. The timing requirements apply to category I, II, and III interfaces.

5.2.1.1.1 EI when IDR line is set. The peripheral equipment shall clear the IDR line at least 20 microseconds (µs) before changing data on the ID lines and shall set the EIR line. This timing shall prevent the computer from interpreting the EI code word on the ID lines as an ID word.

5.2.1.1.2 IDR when EIR line is set. The peripheral equipment shall clear the EIR line at least 20 µs before changing the EI data on the ID lines and shall set the IDR line. This timing shall prevent the computer from interpreting the ID word on the ID lines as an EI code word.

5.2.1.2 Type A interface, circuit.

5.2.1.2.1 Type A input amplifier. Each Type A input amplifier circuit shall be a single-ended amplifier and shall have the following characteristics:

a. The output of the circuit shall switch from binary zero to binary one whenever the input signal changes in the positive direction through the range of -7.5 Vdc to -4.5 Vdc.
b. The output of the circuit shall switch from binary one to binary zero whenever the input signal changes in the negative direction through the range of -4.5 Vdc to -7.5 Vdc.
c. The output of the circuit shall not switch as a result of any input transient-pulse signal that has an integrated amplitude-duration of less than 15 Vdc per µs (delay of 1.5 ± 0.5 µs with a 15 Vdc step input).
d. The output of the circuit shall be binary zero whenever the input is open-circuited.
e. The circuit shall not sink more than 4.0 milliamperes (mA) for a steady state binary one input nor source more than 1.0 mA for steady state binary zero input.
f. The output of the circuit shall be binary zero whenever the steady state input signal is more negative than -7.5 Vdc.
g. The output of the circuit shall be binary one whenever the steady state input signal is more positive than -4.5 Vdc.

5.2.1.2.2 Type A output line and control line drivers. Each Type A output line and control line driver circuit shall drive a single-ended input amplifier and shall have the following characteristics when driving a load with capacitance of 6000 picofarads:

a. The steady state output voltage representing a binary one shall be -1.5 to +1.5 Vdc.
b. The steady state output voltage representing a binary zero shall be -10.0 to -17.5 Vdc.
c. The voltage variation among all binary zero output signals on one channel shall not exceed 1.0 Vdc.
d. The voltage variation among all binary one output signals on one channel shall not exceed 1.0 Vdc.
e. The circuit shall be able to source 4.0 mA per line for a steady state binary one output. Each data line driver circuit that drives more than one line (for example, four data lines per circuit in computers) shall have proportionally more capability than specified here.

f. The circuit shall be able to sink 1.0 mA per line for a steady state binary zero output. Each data line driver circuit that drives more than one line (for example, four data lines per circuit in computers) shall have proportionally more capability than specified here. Sinking describes the driver's ability to accommodate current flow into the normal output circuit due to the bias voltage on the input circuit on the other end of the line. Whenever the driver output is more negative than the bias on the input circuit on the other end of the line, current will flow toward the driver's normal output (the condition opposite to the driver being the current source) and the driver shall be able to absorb (sink) the specified current flowing toward the output.
g. The output of the circuit shall switch in not more than 6.0 µs (measured between 10 and 90 percent amplitude points).
h. The output of the circuit shall switch at a rate of not more than 5.0 Vdc per µs.
i. The circuit shall drive the lines and terminations (input amplifier) while switching as well as in the steady state condition.
j. Whenever power to a control line driver circuit is removed, the driver shall present not less than 100,000 ohms impedance to the line, with the restriction that the line voltage (because of the input circuit on the other end of the line) shall be within the range -10 to -17.5 Vdc.

5.2.2 Type B interface. The Type B (NTDS fast) interface shall be characterized by nominal values of 0.0 and -3 Vdc to represent binary one and binary zero, respectively, and by a switching threshold of -1.5 ± 0.4 Vdc. Parallel data transfer shall consist of up to 250,000 words per second on one cable.

5.2.2.1 Type B timing. Duration of signals and timing between signals communication sequence shall conform to the applicable limits shown on figures 8 through 11. The limits are expressed as absolute minimums or absolute maximums and shall denote the following requirements:

a. Neither the initiation nor the termination of any control or data signal shall occur sooner than shown on figures 8 through 11.
b. Each equipment shall recognize data and control signals that occur at the times specified and that exist for any duration equal to or greater than the duration specified.
c. The timing requirements apply to category I, II, and III interfaces.

5.2.2.1.1 Input timing, peripheral equipment interrupts. Requirements shall be the same as specified in 5.2.1.1.1 and 5.2.1.1.2.

5.2.2.2 Type B interface, circuit.

5.2.2.2.1 Type B input amplifier. Each Type B input amplifier circuit shall be differential type amplifier and shall have the following characteristics:

a. The output of the circuit shall switch from binary zero to binary one whenever the input signal changes in the positive direction through the range of -1.9 to -1.1 Vdc.
b. The output of the circuit shall switch from binary one to binary zero whenever the input signal changes in the negative direction through the range of -1.1 to -1.9 Vdc.
c. The output of the circuit shall not switch as a result of any input transient-pulse signal that has an amplitude between +7.5 Vdc to -7.5 Vdc if the duration and amplitude are common to both sides of the line (common mode).
d. The output of the circuit shall be binary zero whenever the input is open-circuited.
e. The circuit shall not sink more than 1.5 mA for a steady state binary one nor source more than 0.5 mA for a steady state binary zero.
f. The output of the circuit shall be binary zero whenever the steady state input signal is more negative than -1.9 Vdc.
g. The output of the circuit shall be binary one whenever the steady state input signal is more positive than -1.1 Vdc.
h. The input circuit shall present a terminal impedance to the line equivalent to a resistance of 150 to 180 ohms in series with a capacitance of 0.0068 to 0.0100 microfarad.

5.2.2.2.2 Type B output line and control line drivers. Each Type B output line and control line driver circuit shall drive a differential type of input amplifier (data line return shall be incorporated into the driver in order to maintain differential integrity) and shall have the following characteristics when driving a line with any characteristic impedance between 100 and 180 ohms:

a. The steady state output voltage representing a binary one shall be 0.0 to -0.5 Vdc. The -0.5 Vdc point shall be indicated on all Type B timing diagrams and is a timing reference.
b. The steady state output voltage representing a binary zero shall be -3.0 to -4.5 Vdc (it may be more negative if the input circuit being driven presents a more negative signal, with the restriction that the negative voltage present from the input circuit being driven shall not exceed -7.0 Vdc). The -3.0 Vdc point shall be indicated on all Type B timing diagrams and is a timing reference.
c. The circuit shall be able to source 1.5 mA for a steady state binary one output. Each data line driver circuit that drives more than one line (for example, four data lines per circuit in computers) shall have proportionally more capability than specified here.
d. The circuit shall be able to sink 0.5 mA for a steady state binary zero output. Sinking describes the driver's ability to accommodate current flow into the normal output circuit due to the bias voltage on the input circuit on the other end of the line. Whenever the driver output is more negative than the bias on the input circuit on the other end of the line, current will flow toward the driver's normal output (the condition opposite to the driver being the current source) and the driver shall be able to absorb (sink) the specified current flowing toward the output.
e. The output of the circuit shall switch in not more than 0.4 µs (measured between -0.5 and -3.0 Vdc.).
f. The circuit shall drive the lines and terminations (input amplifier) while switching, as well as in the steady state conditions. Each data line driver circuit that drives more than one line (for example, four data lines per circuit in computers) shall have proportionally more capability than specified here.
g. Whenever power to a control line driver circuit is removed, the driver shall present not less than 100,000 ohms impedance to the line, with the restriction that the line voltage (because of the input circuit on the other end of the line) shall be within the range of -3.0 to -7.0 Vdc.

5.2.3 Type C interface. The Type C (ANEW) interface shall be characterized by nominal values of 0.0 and +3.5 Vdc to represent binary one and binary zero, respectively, and by a switching threshold of +1.5 ± 0.7 Vdc. Parallel data transfer shall consist of up to 250,000 words per second on one cable.

5.2.3.1 Type C timing. Duration of signals and timing between signals in the communication sequence shall conform to the applicable limits shown on figures 12 through 15 (signal requirements for the Type C interface). The limits are expressed as absolute minimums or absolute maximums that shall denote the following requirements:

a. Neither the initiation nor the termination of any control or data signal shall occur sooner than shown on figures 12 through 15.
b. Each equipment shall recognize data and control signals that occur at the times specified, or at any time later than the times specified, and that exist for any duration equal to or greater than the duration specified.
c. The timing requirements apply to category I, II, and III interfaces.

5.2.3.1.1 Type C input timing, peripheral equipment interrupts. Requirements shall be the same as specified in 5.2.1.1.1 and 5.2.1.1.2.

5.2.3.2 Type C interface, circuit.

5.2.3.2.1 Type C input amplifier. Each Type C input amplifier circuit shall be a differential type of amplifier and shall have the following characteristics:

a. The output of the circuit shall switch from binary zero to binary one whenever the input signal changes in the negative direction through the range of +2.2. to +0.8 Vdc.
b. The output of the circuit shall switch from binary one to binary zero whenever the input signal changes in the positive direction through the range of +0.8. to +2.2 Vdc.
c. The output of the circuit shall not switch as a result of any input transient-pulse signal that has an amplitude between +6.0 and -6.0 Vdc if the duration and amplitude are common to both sides of the line (common mode).
d. The output of the circuit shall be binary zero whenever the input is open-circuited.
e. The circuit shall not sink more than 2.5 mA when a +3 Vdc signal is applied to the signal input terminal, and shall source not more than 2.5 mA when 0.0 Vdc is applied at the signal input terminal (return terminal grounded).
f. The output of the circuit shall be binary zero whenever the steady state input signal is more positive than +2.2 Vdc.
g. The output of the circuit shall be binary one whenever the steady state input signal is more negative than +0.8 Vdc.
h. The input circuit shall present a terminal impedance to the line equivalent to a resistance of 110 to 160 ohms in series with a capacitance of 0.0068 to 0.0100 microfarads.
i. The input resistance of the signal input and return input terminals shall be matched to within ± 8 percent.

5.2.3.2.2 Type C output line and control line drivers. Each Type C output line and control line driver circuit shall drive a differential type of input amplifier and shall have the following characteristics when driving a line with any characteristic impedance between 100 and 180 ohms.

a. The steady state output voltage representing a binary one shall be between 0.0 and +0.45 Vdc. The output driver shall be able to sink a current of at least 40 mA at the +0.45 Vdc level. The +0.45 Vdc point shall be indicated on all Type C timing diagrams for a timing reference. Sinking describes the driver's ability to accommodate current flow into the normal output circuit due to the bias voltage on the input circuit on the other end of the line. Whenever the driver output is more negative than the bias on the input circuit on the other end of the line, current will flow toward the driver's normal output (the condition opposite to the driver being the current source) and the driver shall be able to absorb (sink) the specified current flowing toward the output.
b. The steady state output voltage representing a binary zero shall be:
    1. Plus 2.7 Vdc minimum when sourcing 27 mA. The +2.7 Vdc point shall be indicated on all Type C timing diagrams and is a timing reference. Each data line driver circuit that drives more than one line (for example, four data lines per circuit in computers) shall have proportionally more capability than specified here.
    2. Plus 4.5 Vdc maximum when open-circuited.
c. The output voltage fall time (90 to 10 percent) shall be less than 100 nanoseconds (ns).
d. The output voltage rise time (10 to 90 percent) shall be less than 100 ns.
e. The circuit shall drive the lines and terminations (input amplifier) while switching, as well as in the steady state condition. Each data line driver circuit that drives more than one line (for example, four data lines per circuit in computers) shall have proportionally more capability than specified here.
f. Whenever power to a control line driver circuit is removed, the driver shall present not less than 100,000 ohms impedance to the line with the restriction that the line voltage (due to the input circuit on the other end of the line) is within the range of +3 to +7 Vdc.

5.2.4 Type H interface. The Type H interface shall be characterized by nominal values of 0.0 Vdc and +3.5 Vdc to represent binary one and binary zero, respectively, and by a switching threshold of +1.5 ± 0.7 Vdc. Parallel data transfer shall consist of up to 500,000 words per second on one cable.

5.2.4.1 Type H timing. Duration of signals and timing between signals in the communication sequence shall conform to the applicable limits shown on figures 16 through 19 (signal requirements for the Type H interface). The limits are expressed as absolute minimums or absolute maximums that shall denote the following requirements:

a. Neither the initiation nor the termination of any control or data signal shall occur sooner than shown on figures 16 through 19.
b. Each equipment shall recognize data and control signals that occur at the times specified, or at any time later than the times specified, and that exist for any duration equal to or greater than the duration specified.
c. The timing requirements apply to category I, II, and III interfaces.

5.2.4.1.1 Type H input timing, peripheral equipment interrupts. Requirements shall be the same as specified in 5.2.1.1.1 and 5.2.1.1.2.

5.2.4.2 Type H interface, circuit. Requirements shall be the same as specified in 5.2.3.2.

5.3 Type D interface.

5.3.1 Type D interface, physical. Type D I/O channels shall transfer up to 10 Mb/s binary information using bipolar serial pulse trains on two cables. The signals required for input transfer shall occur on the input channel. The signals required for output transfer shall occur on the output channel. The Type D interface shall be designed to interface with Type RG-12A coaxial cable as specified in MIL-C-17 and MIL-C-17/6, or with coaxial cable having characteristics equivalent to RG-12A coaxial cable. Each input channel shall require one coaxial cable, and each output channel shall require one coaxial cable.

5.3.2 Type D interface, functional. Type D transfers shall be accomplished using two types of bipolar pulse trains: control frames as specified in 5.3.2.1 and control and data words as specified in 5.3.3. The first bipolar pulse or bit of each pulse train shall be a synchronization pulse and shall be a high , logic one. A binary one shall be a pulse of phase zero degrees and shall be a high polarity followed by a low polarity. A binary zero shall be a pulse of phase 180 degrees and shall be a low polarity followed by high polarity. The transfer of a word from one equipment to another equipment shall use the following general sequence of events:

a. The transmitting equipment (the equipment that will transmit the word) shall send a control frame requesting an eventual word transfer to the receiving equipment.
b. The receiving equipment (the equipment that will receive the word) shall send a control frame granting permission to transfer the word to the transmitting equipment.
c. The transmitting equipment shall send the word to the receiving equipment.

5.3.2.1 Control frames. Control frames shall be three bits, a synchronization bit followed by two control bits. The control frames used on an input channel shall be as shown on figure 20. The control frames used on an output channel shall be as shown on figure 21. Both control bits may be set in one control frame. The data word transmitted following the control frames exchanged shall be identified at the receiving equipment by a word identifier bit transmitted with the data word.

5.3.2.1.1 Restrictions for computer. The use of control frames by the computer shall have the following restrictions:

a. The computer (transmitting computer for IC operation) shall be required to send the EF word or OD word only when the corresponding control function is specified by the ORCF and the corresponding buffer is active. When these conditions do not exist, the computer (transmitting computer for IC operation) shall be required to re-initiate the transfer sequence by sending another output enable control frame (OECF).
b. In response to an input request control frame (IRCF), the computer (transmitting computer for IC operation) shall be required to send an input enable control frame (IECF) that corresponds to the active ID or EI buffer.

5.3.2.1.2 Restrictions for peripheral. The use of control frames by peripheral equipment shall have the following restrictions:

a. Peripheral equipment shall distinguish between control frames and data words by means other than the fixed sequence of events specified herein, as the possibility exists for a computer to terminate and re-initiate an output or EF buffer between events in the sequence. This situation would cause the computer to send two consecutive OECF.
b. Peripheral equipment shall be required to accept and send data words that are the length of the computer word even if the peripheral equipment does not use all the information bits in the data word.
c. Peripheral equipment shall be required to send the EI word or ID word only when the corresponding control function specified by the IECF corresponds to the peripheral equipment's EI or ID status. When this condition does not exist, the peripheral equipment shall be required to re-initiate the input transfer by sending another IRCF.
d. In response to an OECF, peripheral equipment shall be required to send an ORCF that corresponds to the status, that is, the capability to accept an EF or OD word.

5.3.3 Data word format. Data words shall be a synchronization bit followed by a word identifier bit and the information bits as shown on figure 22. When the data word is an input word, the transmitting equipment shall condition the word identifier bit as follows: binary zero if the word is input data; binary one if the word is an EI. When the data word is an output word, the transmitting equipment shall condition the word identifier bit as follows: binary zero if the word is OD; binary one if the word is an EF. The number of information bits shall normally be equal to the computer word length. Data words transmitted to a computer shall require that the number of information bits be equal to the word size used by the computer.

5.3.4 Category I output channel operation. The transmission of OD words and EF words from a computer output channel to a peripheral equipment shall occur in accordance with the event sequences specified herein. The timing requirements shall be as specified in 5.3.8.

5.3.4.1 EF transfer sequence. When the computer and the peripheral are ready to perform an EF transfer, the sequence shall be in the following steps:

a. The computer shall send the OECF with the external function enable (EFE) bit set to the peripheral equipment.
b. The peripheral equipment shall respond by sending the ORCF with the EFR bit set to the computer.
c. The computer, in accordance with internal priorities, shall send the EF word to the peripheral equipment.

Steps "a" through "c" shall be repeated for each EF word transferred.

5.3.4.2 Forced EF transfer. The transfer of a forced EF shall be the same as the EF, except that the computer shall send the forced EF word whether or not the ORCF from the peripheral equipment specifies the EFR.

5.3.4.3 OD word transfer sequence. When the computer and the peripheral equipment are ready to perform an OD word transfer, the sequence shall be in the following steps:

a. The computer shall send the OECF with the output data enable (ODE) bit set to the peripheral equipment.
b. The peripheral equipment shall respond by sending the ORCF with the ODR bit set to the computer.
c. The computer, in accordance with internal priorities, shall send the OD word to the peripheral equipment.

Steps "a" through "c" shall be repeated for each OD word transferred.

5.3.4.4 Peripheral "not ready" operation. If the computer is ready to transfer an EF or an OD word and the peripheral equipment is not ready, the peripheral equipment shall respond with a "not ready" control frame. The computer shall repeat sending the OECF for each "not ready" control frame from the peripheral equipment until the peripheral equipment is ready to accept an EF or an OD word.

5.3.5 Category I input channel operation. The transmission of ID words and EI words to a computer input channel from a peripheral equipment shall occur in accordance with the event sequences specified herein. The timing requirements shall be as specified in 5.3.8.

5.3.5.1 ID word transfer sequence. When the computer and peripheral equipment are ready to perform an ID word transfer, the sequence shall be in the following steps:

a. The peripheral equipment shall send the IRCF with the IDR bit set to the computer.
b. The computer shall respond by sending the IECF with the input data enable (IDE) bit set to the peripheral equipment.
c. The peripheral equipment shall send the ID word to the computer.

Steps "a" through "c" shall be repeated for each ID word transferred.

5.3.5.2 EI transfer sequence. When the computer and peripheral equipment are ready to perform an EI transfer, the sequence shall be in the following steps:

a. The peripheral equipment shall send the IRCF with the EIR bit set to the computer.
b. The computer shall respond by sending the IECF with the EIE bit set to the peripheral equipment.
c. The peripheral equipment shall send the EI word to the computer.

Steps "a" through "c" shall be repeated for each EI word transferred.

5.3.5.3 Computer "not ready" operation. If the peripheral equipment requests the transfer of an ID or an EI word and the computer is not ready to accept the word, the computer shall send the "not ready" control frame to the peripheral equipment. The peripheral equipment shall repeat sending the IRCF for each "not ready" control frame received from the computer until the peripheral equipment receives the IECF (with the appropriate enable bit set) from the computer.

5.3.6 Category II channel operation. For IC operation, the output channel of the transmitting computer shall be connected to the input channel of the receiving computer. The timing requirements shall be as specified in 5.3.8.

5.3.6.1 IC EF sequence. When the transmitting computer is ready to transmit an EF and the receiving computer is ready to accept an EI, the sequence shall be in the following steps:

a. The transmitting computer shall send the OECF with the EFE bit set to the receiving computer.
b. The receiving computer shall receive the OECF as an IRCF with the EIR bit set.
c. The receiving computer shall respond by sending the IECF with the EIE bit set to the transmitting computer.
d. The transmitting computer shall receive the IECF as an ORCF with the EFR bit set.
e. The transmitting computer, in accordance with internal priorities, shall send an EF word to the receiving computer.
f. The receiving computer shall accept the EF word as an EI word.

Steps "a" through "f" shall be repeated for each EF word transferred.

5.3.6.2 IC forced EF. After the transmitting computer has transmitted an OECF, and after either an ORCF with any combination of OD request or EF request or neither bits set is received from the receiving computer or a minimum timeout of 20 µs occurs, the transmitting computer shall send the EF word. The use of IC forced EF words shall require certain programming considerations as specified in 4.4.2.

5.3.6.3 IC OD sequence. When the transmitting computer is ready to transmit an OD word and the receiving computer is ready to accept an ID word, the sequence shall be in the following steps:

a. The transmitting computer shall send the OECF with the ODE bit set to the receiving computer.
b. The receiving computer shall receive the OECF as an IRCF with the IDR bit set.
c. The receiving computer shall respond by sending the IECF with the IDE bit set to the transmitting computer.
d. The transmitting computer shall receive the IECF as an ORCF with the ODR bit set.
e. The transmitting computer, in accordance with internal priorities, shall send an OD word to the receiving computer.
f. The receiving computer shall accept the OD word as an ID word.

Steps "a" through "f" shall be repeated for each OD word transferred.

5.3.6.4 IC "not ready" operation. If the transmitting computer is ready to transfer an IC EF or IC OD word and the receiving computer is not ready the receiving computer shall respond with a "not ready" control frame. The transmitting computer shall repeat sending the OECF for each "not ready" control frame from the receiving computer until the receiving computer is ready to accept an EI or an ID word.

5.3.7 Category III. The category III interface shall require one of the peripheral equipments to perform the function of the computer as specified for category I interface (see 5.3.4 and 5.3.5); the other peripheral equipment shall function as a normal peripheral device. The I/O interface between a peripheral-peripheral shall transfer control and data words by means of the reciprocal interaction as specified for category I (see 5.3.4 and 5.3.5).

5.3.8 Type D channel timing (categories I, II, and III). To assure reliable data transfer, the following signal timing restrictions shall be required of equipments involved. The timing specified herein is predicated on and includes propagation times for a cable 1000 feet long. The nominal propagation time is 1.5 ns/foot or 1.5 µs for the 1000 foot cable. Unless otherwise specified herein, the timing requirements shall be measured from the leading edge of the synchronization pulse associated with one event to the leading edge of the synchronization pulse associated with the succeeding event. Each of the following timing requirements refer to the timing on each individual cable:

a. Consecutive control frames. The time between consecutive control frames (transmitted by the same equipment) shall be not less than 20 µs.
b. OECF or ORCF. The time between computer transmission of an OECF and the receipt of an ORCF from a peripheral equipment shall be not greater than 10 µs.

c. Enable-to-request time exceeded. If this time exceeds 20 µs the computer shall be required to send the OECF again if data transfer is still desired.
d. ORCF to data. There shall be not time limit between the time the computer receives the ORCF and the time the computer transmits the requested OD word.
e. Output to synchronization. The time between the trailing edge of the last word and next synchronization bit shall be not less than 200 ns.
f. IRCF to IECF. The time between receipt of an IRCF and the transmission of the IECF shall be not greater than 15 µs.
g. IECF to input. A peripheral equipment shall be required to transmit an input word within 15 µs of receiving an IECF. The time between transmission of an IECF and the receipt of an input word shall be not greater than 20 µs.
h. Input to synchronization. The time between the trailing edge of the last bit of an input word to the next IRCF bit shall be not less than 200 ns.
i. Transmitter receiver pair. Except when the transmitter is transmitting, the receiver shall receive signals at all times.
j. Bipolar pulse. Timing requirements of the bipolar pulses shall be as shown on figure 23.

5.3.9 Type D electrical interface (categories I, II, and III).

5.3.9.1 Termination. The Type D interface termination shall be electrically as shown on figure 24. The coaxial shield shall be connected to signal ground at both ends and the coaxial armor shall be connected to cabinet ground at both ends. Both the transmitter and receiver shall be required to incur no damage and shall resume normal operation after a short circuit between the serial interface lines either at the coaxial connector or at the transmitter-receiver connections.

5.3.9.2 Bipolar pulse. At the transmitter end, the bipolar pulse of ± 3.25 volts shall have the timing, voltage levels, and transition times as shown on figure 23. The bipolar pulse train shall represent the serial binary data shown on figure 25.

5.3.9.3 Switching levels. The receiver input voltage switching levels shall be as follows (input voltage refers to the voltage at the receiver input pins):

a. The receiver output shall remain stable (not switch) when the input voltage is from 0.0 to ± 0.5 Vdc.
b. The receiver output shall switch whenever the input voltage exceeds ± 1.25 Vdc (absolute).

5.4 Type E interface. The Type E (Low Level Serial (LLS)) interface is derived from STANAG 4153 and applies to category I, II, and III interfaces. The Type E protocol does not change regardless of whether the interface is functioning as category I, II or III. A Type E I/O interface consists of an output function (source) and an input function (sink). Type E operation requires interconnection of a source to a sink. The source is that end of the interface which transmits information frames (IFs). The sink is that end of the interface which receives IFs. Both the source and the sink shall be capable of transmitting and receiving control frames. A Type E interface shall transfer IFs from the source to the sink after the exchange of control frames. A Type E source to sink interconnection is shown in figure 26. The source and the sink functions shall be present for a two-way data transfer. A Type E interface full duplex signal flow is shown in figure 27.

5.4.1 Frames. Type E interface shall use two frame types: control and information.

5.4.1.1 Control frames. Control frames shall be used to coordinate the transfer of information over the Type E interface. All control frames shall be 4 bits in length with no parity checking. There shall be two types of control frames: source status control frames and sink status control frames.

5.4.1.1.1 Source status control frame. The source shall transmit source status (SOS) control frames to indicate the status of the source as shown in figure 28. The fourth bit of the SOS control frame shall be zero. This bit was reserved prior to Revision C of MIL-STD-1397. The individual equipment specification shall define whether compatibility with equipment having undefined settings for this bit shall be required.

5.4.1.1.2 Sink status control frame. The sink shall transmit sink status (SIS) control frames to indicate the status of the sink as shown in figure 29. The fourth bit of the SIS control frame shall always be one. This bit was reserved prior to Revision C of MIL-STD-1397. The individual equipment specification shall define whether compatibility with equipment having undefined settings for this bit shall be required.

5.4.1.2 Information frames. The Type E interface shall use information frames (IFs), shown in figure 30, to transfer information from the source to the sink. The Type E interface shall use two modes of IF transfer: single word transfer (SWT) IFs and burst transfer IFs.

5.4.1.2.1 SWT information frame. The SWT IF shall consist of a synchronization (S) bit, a word identifier (WI) bit, one 32 bit information word (IW), and one optional parity bit. The IW shall consist of either a data word or a command/interrupt word (CIW). The data word transfers data from source to sink. The CIW transfers commands from source to sink. The CIW shall always be sent as a SWT. For Navy system compatibility, the required number of bits in the information word, for either a data word or a CIW, shall be 32 with no parity or 33 with parity. See figure 31. The SWT IF is the default mode.

5.4.1.2.2 Burst transfer information frame. The burst transfer IF shall be restricted to the transfer of data words. The burst transfer IF shall be variable in length within the range of one data word to a maximum of 32 data words. The burst transfer IF shall consist of one synchronization (S) bit and one word identification (WI) bit followed by a minimum of 32 bits in the data word with no parity or 33 bits with parity, to a maximum of 1024 bits with no parity or 1056 bits with parity. See figure 31.

5.4.1.2.3 Parity generation. When parity is implemented, the source shall generate odd parity on transmitted IFs. For SWT IF, odd parity shall be generated using the WI bit and the 32 bits of either the data word or CIW as shown in figure 31. For burst transfer IFs, the parity bit for the first 32 bit data word shall be generated in the same manner as for the SWT IF mode. All succeeding 32 bit words in the burst transfer IF shall have odd parity generated on the 32 bit data word only. The parity bit for each word shall follow the last bit of the data word. See figure 31.

5.4.2 Protocol. The Type E interface sink and source shall operate per the following protocol:

a. The source transmits either a SOS control frame or an IF and receives SIS control frames. The SOS control frame indicates the availability of an IF at the source.
b. The sink receives SOS control frames and IF's and transmits SIS control frames. The SIS control frame indicates the ability of the sink to receive an IF from the source.
c. The sink shall be quiescent until it receives a SOS control frame.
d. The source shall initiate channel activity by sending a SOS control frame.
e. The source shall re-transmit a SOS control frame if the SIS control frame from the sink is not received within the response time limit.
f. The sink shall recognize an IF by the fact that more than four bits are received sequentially.
g. The source and sink shall exchange control frames even when there are no IFs to transfer.
h. The ability of the sink to accept an IF shall determine the coding of the SIS control frame. The source shall use the SIS control frame to determine which IF type (data or CIW) the sink is capable of receiving.
i. The source shall determine the coding of the SOS control frame based upon the IF type (data or CIW) available for transmission. The sink shall use either a SOS control frame or IF to trigger the next SIS control frame. The sink need not decode the 2nd and 3rd bits of the SOS control frame. The code may be used for purposes such as monitoring and analysis.
j. A CIW transmitted without the preceding SIS control frame indicating a readiness to accept a CIW is defined as a forced command.

5.4.2.1 Forced command. If required, the use of forced commands shall be as specified in the individual equipment specification.

5.4.2.2 Transfer Sequence. The Type E information transfer sequence shall be as follows:

a. The source shall send a SOS control frame to the sink.
b. The sink shall send a SIS control frame to the source.
c. The source shall send a SOS control frame or IF to the sink in accordance with the SIS control frame type received and the source condition, all in accordance with table IV.
d. Steps "b" and "c" shall be repeated continuously.

TABLE IV. Type E source response to SIS control frame.

	Source Condition				
SIS Received	Nothing to send	Have CIW	Have Data	Have Both CIW and data	Have Forced Command
Not Ready	No Information SOS	Have CIW SOS	Have Data SOS	Have Both SOS	CIW Frame
Ready for CIW	No Information SOS	CIW Frame	Have Data SOS	CIW Frame	CIW Frame
Ready for data	No Information SOS	Have CIW SOS	Data Word Frame	Data Word Frame	CIW Frame
Ready for either	No Information SOS	CIW Frame	Data Word Frame	CIW Frame	CIW Frame

5.4.3 Timing. The Type E interface timing between frames shall be as shown in table V.

TABLE V. Type E timing intervals.

Responsibility	From	To	Time Interval
Sink	Trailing edge of SOS control frame or IF	Leading edge of SIS control frame	500 ns min. 150 µs max.
Source	Trailing edge of SIS control frame	Leading edge of SOS control frame or IF	500 ns min. 1 ms max.1/

1/ The 1 millisecond (ms) maximum interval for the source response shall be imposed to permit independent line monitoring, or to permit the sink to detect a source or cable failure by the cessation of repetitive signals from the source.

5.4.3.1 Reinitiation. A source receiving no SIS control frame response shall transmit control frames at a rate of one frame every 300 µs ± 100 µs.

5.4.3.2 Sink response. If the sink cannot transmit the SIS control frame within limits shown in table V, the sink shall not send any SIS control frame.

5.4.3.3 Receiver recovery. The receiver shall be ready to respond to the frames specified herein except when the transceiver is transmitting and for a minimum of 350 ns to a maximum of 500 ns, thereafter.

5.4.3.4 Modulation timing. The modulation rate shall be 10 million bits per second with a tolerance of 0.1 percent. The bit timing shall be as shown on figure 32.

5.4.4 Modulation. The Type E interface frame bit modulation shall be Manchester II split phase modulation (also known as bi-phase level modulation). A one bit is represented by a positive pulse followed by a negative pulse. A zero bit is represented by a negative pulse followed by a positive pulse. The one and zero pulse phases shall be as shown on figure 32.

5.4.4.1 Synchronization. The exchange of signals on the Type E interface channel shall be asynchronous. Asynchronous operation implies an independent clock source (not in synchronism but at the same frequency) at each receiver. Clock information shall be derived from the received signal at the receiver. The first bit of every transmission, designated the synchronization bit, shall be a one.

5.4.5 Electrical characteristics.

5.4.5.1 Output characteristics. Measurement of the output voltage, waveform distortion, output noise, etc., shall be made line-to-line at the equipment I/O connector when the output is terminated at the I/O connector with an impedance of 50 ± 5 ohms.

5.4.5.1.1 Output power. The output shall drive the cable referenced in 5.4.6.1 terminated by one transceiver circuit.

5.4.5.1.2 Output waveform. The output waveform envelope shall be as shown in figure 32. The nominal output voltage shall be ± 600 mV. The output signal shall have the timing, voltage levels and transition times as shown in figure 32. There shall be no reversal of direction of voltage change while the signal is in the transition region of ± 250 mV. For output waveform measurements, the beginning of the first bit shall be measured from the +60mV level, and the end of the last bit if it is 0, it shall be measured from the +60mV level, if it is 1, shall be measured from the -60mV level..

5.4.5.1.3 Output noise. Output noise shall not be greater than ± 30 mV peak-to-peak with the power on but not transmitting.

5.4.5.1.4 Output waveform distortion. The combination of overshoot and undershoot distortion shall not exceed 150 mV. The residual transmitter voltage distortion shall not exceed ± 60 mV in the interval between the end of the last bit and 2 bit times after the last valid transition of the last bit. The total transmitter output noise shall not exceed ± 30 mV in the interval between 2 bit times after the zero crossing in the middle of the last bit and the next transmission. The output waveform distortion shall conform to the waveform as shown in figure 32.

5.4.5.2 Input characteristics. Input requirements apply at the equipment I/O connector, measured line-to-line from a nominal source impedance of 50 ohms.

5.4.5.2.1 Input compatibility. The input shall be compatible with the incoming signals shown in figure 33.

5.4.5.2.2 Receiver input sensitivity. The receiver shall respond to input signals having peak amplitudes between 220 mV to 900 mV inclusive. The receiver shall not respond to input signals having peak amplitudes not greater than 155 mV, or a volt-time product equal to or less than 1E-9 volt-seconds.

5.4.5.2.3 Receiver pulse width. Input shall decode received signal pulse widths specified in figure 33. The minimum pulse width shall be 5 ns as measured at the ± 220 mV level. For input waveform measurements, the beginning of the first bit shall be measured from the +60mV level, and the end of the last bit if it is 0, it shall be measured from the +60mV level, if it is 1, shall be measured from the -60mV level.

5.4.5.2.4 Impedance. With the equipment either on or off and the transmitter not transmitting, the magnitude of the complex input impedance Z shall be 50 ohms nominal. The impedance presented to the interface cable at the equipment I/O connector shall be such that the return loss from 1 MHz to 60 MHz does not exceed the levels specified in figure 34. The shaded area in the figure 34 represents the range of acceptable values across the frequency range of interest. Conformance with the return loss of -22 dB, as measured with a network analyzer between 5 MHz and 10 MHz, corresponds to an impedance magnitude range of 42.6 ohms to 58.6 ohms. Conformance with the return loss profile of figure 34 shall be demonstrated by passing the test as defined in 50.1.1 of appendix C.

5.4.5.2.5 Reflections. The input impedance shall be such that with the use of the cable specified in 5.4.6.1, the reflected voltage due to an incident waveform shown in figure 32 with a peak amplitude of 750 mV and rise/fall time of 6.5 to 7.0 ns (10 to 90%) shall be not greater than ± 250 mV as observed at the source interface 200 ns after the last valid transition of the last bit of the frame. Conformance to this requirement shall be demonstrated by passing the reflection test as defined in 50.1.2 of appendix C.

5.4.5.2.6 Composite system channel noise. The composite system channel noise at the cabinet connector interface in the time period of 400 ns after the last zero voltage crossing in the middle of the last bit of the frame and until the transmission of the next frame due to all causes (reflections, transmitter output noise, transmitter residual noise, etc.) shall not exceed 200 mV peak-to-peak as shown in figure 68. Conformance to this requirement shall be demonstrated by passing the composite system channel noise test as defined in 50.1.3 of appendix C.

5.4.5.2.7 Common mode rejection. Common mode signals from DC to 2 MHz with amplitudes up to 20 volts, peak-to-peak, and signals from 2 MHz to 20 MHz with amplitudes up to 5 volts, peak-to-peak, shall not degrade the performance of the receiver.

5.4.5.3 Interface circuits. The interface shall not be damaged by cable open circuits or by short circuits of the following types:

a. Line-to-line.
b. Line-to-ground.
c. Voltage sources of 0 to 115 VAC, 60 Hz, line-to-ground.

5.4.5.4 Grounding. The grounding system shall be in accordance with DOD-STD-1399, section 406. Additional grounding requirements for the Type E interface shall be as follows:

a. The cable grounding shall be as shown on figure 26.
b. The outer shield shall be considered as a continuation of the cabinet ground and shall not be used as the signal ground.
c. The outer shield shall be terminated at cabinet ground at both the source and the sink.
d. Both the signal conductor (center conductor) and the inner shield (return) shall be isolated from cabinet ground and signal ground
e. The signal ground shall be isolated from the cabinet ground within the cabinet.

5.4.6 Physical interface.

5.4.6.1 Cable. A 50 ohm triaxial cable shall be the medium for the Type E interface. The triaxial cable consists of a center conductor, an inner shield and an outer shield. The center conductor (signal) and inner shield (return) provide the transmission line, and both shall be isolated from the outer shield (cabinet ground). MIL-C-17/134 (TRF-58) cable shall be used for cables lengths up to 120 meters and MIL-C-17/135 (TRF-8) for cables lengths up to 300 meters. (See 30.1 of appendix A).

5.4.6.2 Connectors. The connector mounted on the equipment bulkhead shall be identical, in so far as those portions that lie outside of the cabinet, with the bulkhead jack specified in MIL-C-49142/02. When using the cables defined in 5.4.6.1, the mating plugs specified in MIL-C-49142/01 (refer to 30.3.2 of appendix A.) shall be used.

5.4.7 System integrity features (SIFs) The Type E interface SIFs shall be implemented for improved diagnostic capability and system reliability. These error detection features improve the integrity of the system by detecting loss of communication, protocol violations, and data corruption. The SIFs operation, which include source timeout, sink timeout, sink parity, sink timing, sink illegal condition, and control frame validation, is defined in the following paragraphs:

5.4.7.1 Source timeout. A source timeout error shall occur under the two following conditions:

a. The sink fails to respond within the source timeout period to SOS control frames indicating that the source has an IF to send, or
b. The sink responds within the source timeout period and the SIS control frame response does not allow the source to transmit the IF.

When the source has an IF available for transmission, it shall start the source timeout timer. Failure of the sink to respond with a SIS control frame indicating it is ready to accept the IF within the source timeout period shall be detected as a source timeout error. The timer shall be reset upon receipt of a SIS control frame indicating the sink is ready to receive the IF or when the source is no longer ready to transmit the IF. Upon the timer reaching the timeout value, an error bit shall be set in the channel status register, if implemented. If the source is located within equipment having stored program capability, an interrupt shall be generated. If the source does not have stored program capability, an equipment indicator or other means of operator notification shall be used, if implemented. The value of the source timeout period shall be specified by the individual application. (See 40.2.1.2.1.1 in appendix C.)

5.4.7.2 Sink timeout. A sink timeout error occurs when the source does not respond with a SOS control frame or IF within the timeout period. A sink timeout timer shall monitor the communication of the sink with the source. The sink timeout timer shall start when the sink is ready to receive an IF. The timer shall reset upon receipt of a SOS control frame or IF, or when the sink is not ready to receive an IF. Upon the expiration of sink timeout timer, an error bit shall be set in the channel status register, if implemented. If the sink is located within equipment having stored program capability, an interrupt shall be generated for the channel. If the sink does not have stored program capability, an equipment indicator (if implemented) or other means of operator notification may be used.

5.4.7.2.1 Sink timeout period. The value of the sink timeout period shall be 1.5 ms.

5.4.7.2.2 "SOS Start" mode. If implemented, the "SOS Start" mode shall be a selectable. When the "SOS Start" mode is disabled, the sink timeout timer shall operate as described in 5.4.7.2. When it is enabled upon either system power up or initialization, one SOS control frame shall be received before the sink timeout function is enabled, then sink timeout timer operation shall be as described above. This shall be used to verify the host interface is operating before monitoring sink timeout conditions.

5.4.7.3 Sink parity. The Type E channel sink shall monitor the IF received for correct parity. SOS and SIS control frames shall not be monitored for parity. Parity error detection as defined by paragraph 5.4.1.2.3 and figure 36 shall result in a bit set in the channel status register, if implemented. If the sink is located within equipment having stored program capability, the setting of this bit in the channel status register shall result in a channel interrupt. If the sink is located within equipment with no stored program capability, the setting of the bit in the channel status register shall result in the transmission of the channel status register by means of the source channel, if one is implemented. Otherwise, an equipment indicator (if implemented) or other means of operator notification may be used to indicate the sink parity error.

5.4.7.4 Sink timing. The Type E channel sink shall monitor the IF to verify the reception of the correct number of bits. For SWT, the channel shall verify the reception of 34 bits for no parity or 35 bits with parity. For burst transfer, the sink shall verify that after the first 34 bits have been received for no parity, or 35 bits with parity, that the rest of the bits in the IF are multiples of 32 for no parity or 33 with parity. Reception of less than or more than the correct number of bits shall result in the setting of a bit in the channel status register, if implemented. If the sink is located within equipment having stored program capability, the setting of this bit in the channel status register shall result in a channel interrupt. If the sink is located within equipment having no stored program capability, the setting of the bit in the channel status register shall result in the transmission of the channel status register by means of the source channel, if one is implemented. Otherwise, an equipment indicator (if implemented) or other means of operator notification may be used to indicate the sink timing error.

5.4.7.5 Sink illegal condition. The Type E channel sink shall verify that when the "not ready for CIW" or "not ready for data word" bits have been transmitted by means of the SIS control frame, that the source does not respond with the corresponding IF. If the sink receives an IF with a data word after transmitting a "not ready for data" bit in the previous SIS control frame, the sink shall set an error bit in the channel status register, if implemented. If the sink receives an IF with a CIW after transmitting a "not ready for CIW" bit in the previous SIS control frame, the sink shall set an error bit in the channel status register, if implemented. If the sink is permitted to accept forced commands, the sink shall not set an error bit in the channel status register when the sink receives an IF with a CIW after transmitting a "not ready for CIW" bit in the previous SIS control frame. If the sink is located in equipment having stored program capability, an interrupt shall be generated for the channel. If the equipment does not have stored program capability, an indicator (if implemented) or other means of operator notification may be used.

5.4.7.6 Control frame validation. When implemented, the control frame validation shall operate as defined in this paragraph. The source and sink shall monitor received control frames for validity. Frames of less than four bits shall be discarded by both source and sink. The source shall detect an error upon receipt of a control frame in which the 4th bit is not a logic one or upon receipt of a frame of greater than four bits. The sink shall detect an error upon receipt of a control frame in which the 4th bit is not a logic zero. These conditions are indications of shorted or open cables. Detection of these errors shall result in the setting of a bit in the channel status register, if implemented. If the equipment has stored program capability, an interrupt shall be generated for the channel. If the equipment does not have stored program capability, an indicator (f implemented) or other means of operator notification may be used.

5.4.8 Type E channel registers. Type E channel registers shall be as specified in 5.4.8.1 and 5.4.8.2.

5.4.8.1 Channel status register and indicators. Each Type E channel shall have at least one status register or equivalent equipment indicators to indicate the following status (error condition) information:

a. Source timeout.
b. Sink timeout.
c. Sink parity.
d. Sink timing.
e. Sink illegal condition.
f. Control frame validation.

5.4.8.2 Channel mode register. Each Type E channel shall have a mode register or control switches to provide for enabling and disabling the following conditions:

a. Burst transfer.
b. Source parity.
c. Source timeout.
d. Source forced command (if required to be enabled by hardware action).
e. Sink parity.
f. Sink "SOS Start."
g. Sink forced command (if receiving forced CIW capability is supported).
h. Control frame validation.

5.4.9 Source/Sink logic flow. To ensure that all equipment follows identical approaches to mechanization, logic flow diagrams are provided. They are as follows:

a. Source diagram (see figure 35).
b. Sink diagram (see figure 36).

Equipment employing Type E channels shall be in accordance with these logic sequences or have deviations approved by the contracting agency.

5.5 Type F interface. Refer to MIL-STD-1553B (aircraft internal time division multiplex bus).

5.6 Type G interface. Refer to RS-449/RS-232 (RS-449 compatible with RS-232).

5.7 Type J interface. The Type J (fiber optic LLS) interface is the fiber optic implementation of the Type E interface using four (4) optical fibers. The Type J interface shall be identical to the Type E interface of 5.4 except as described in the following:

5.7.1 Framing and protocol. The same control and information frames as the Type E interface shall be used for the Type J interface. The protocol for the Type J interface shall be same as the Type E interface. See section 5.4 and appendix C.

5.7.2 Modulation. The Type J interface frame bit modulation shall be unipolar Manchester II. Manchester II code uses a level transition in the middle of each bit period. For a binary one, the first half of the period is high, and the second half is low. For a binary zero, the first half is low, and the second half is high. The relationship between the electrical signals which are transmitted over the triaxial cable of the Type E and optical waveform on the fiber optic cable is shown in figure 37.

This section of the standard shall apply to point-to-point connections using fiber optic cables. The Type J interface, specifies unipolar, baseband, Manchester II modulation of the optical signal in the place of the three level, bi-phase modulation of the electrical Type E interface. In practice this affects the first and the last bits. The Type E interface protocol specifies that the first bit shall be a binary one. The fiber optic channel shall be driven from the low to a high state on the first transition.

5.7.3 Timing. The Type J interface timing between frames shall be identical to table V of the Type E interface definition. Modulation timing is shown in figure 38.

5.7.4 Optical requirements.

5.7.4.1 Interface definition. The interface shall be defined with respect to the bulkhead connector. Each half duplex channel requires two fibers for transmitting information and control frames. The fibers for each half duplex channel are contained in a single cable terminated in a multi-pin connector as shown in figure 39. In the case of a full duplex channel, two half duplex cables (each with 2 fibers) or a single cable containing four (4) fibers shall be used as shown in figure 40.

5.7.4.2 Cable plant assembly. The optical parameters are defined on the basis of a multi-mode, long wavelength, 1310 nm transmission system using a fiber with a core/cladding diameter of 62.5/125 µm.

5.7.4.2.1 Optical fiber. The optical fiber shall be a multimode, graded index fiber meeting the requirements of MIL-F-49291/6.

5.7.4.2.2 Optical cable. The fiber optic cables shall meet the requirements of MIL-C-85045 using fibers meeting the requirements of 5.7.4.2.1.

5.7.4.2.3 Optical cable length. The Type J channel shall operate when the interconnecting fiber optic cable length is up to 300 meters. (See appendix A.)

5.7.4.2.4 Fiber optic interface connector. The fiber optic interface connector shall meet the requirements of MIL-C-28876 using 62.5/125 µm fiber with a maximum insertion loss of 1.0 dB.

5.7.5 Transmitter optical interface.

5.7.5.1 Optical power output. The transmitter shall be capable of coupling optical power into the mating fiber of the output optical connector within the range specified in figure 38.

5.7.5.2 Optical output waveform. The transmitter shall produce the modulated optical signal waveform as shown in figure 38.

5.7.5.3 Emitted radiation. The nominal peak wavelength shall be within the range of 1270 and 1380 nm. The spectral width (FWHM) shall be less than 200 nm.

5.7.6 Receiver optical interface.

5.7.6.1 Input optical waveform. The receiver shall respond to the optical signal specified herein. The bit error ratio (see 5.7.6.2) applies for receiver input power level and timing as shown in figure 38.

5.7.6.2 Receiver bit error ratio. The bit error ratio (BER) at the output, with respect to the transmitter input, shall not exceed 1E-12.

5.8 Type K interface. The Type K (SCSI-II bus) interface is derived from the differential version of the commercial draft ANSI-X3T9.2/86-109 Rev 10h Small Computer Systems Interface-II standard (SCSI-II). The Type K interface shall adhere to SCSI-II except as defined herein. If implemented, any SCSI-II optional commands shall adhere to appendix D (Type K Command Set). Refer to appendix E for design guidance.

A Type K interface shall function as either a target or initiator, or both. Type K operation requires interconnection of one or more targets to one or more initiators. Devices shall support one or more of the following combinations: single initiator/single target, single initiator/multiple target, multiple initiator/single target, and multiple initiator/multiple target. The maximum number of devices that shall be on a bus is eight.

The Type K interface shall apply to category I, II, and III interfaces. The Type K protocol does not change regardless of whether the interface is functioning as category I, II, or III.

5.8.1 Physical characteristics. The cables and connectors specified in appendix A shall be used for all Type K interfaces.

5.8.1.1 Physical description. The electrical portion of the Type K interface shall be a bus configuration consisting of series-connected, daisy-chained grouped parallel signals. The interface shall connect two or more devices facilitating time shared digital intercommunication between devices. The cable system shall be comprised of several internal and external cable segments. External cable segments shall consist of those cables and connectors externally accessible to the devices. Internal cable segment shall consist of those cables and connectors inside the device cabinet. Each Type K device shall provide a pair of identical connectors on the cabinet or enclosure exterior. An external resistive termination shall be required at each end of the cable system as shown on figure 41.

5.8.1.2 Cable requirements. The total bussing system length including internal and external cable segments shall not exceed 25 meters.

5.8.1.2.1 External cabling. All external cable segments shall conform to the cable requirements in appendix A. See figure 41.

5.8.1.2.2 Internal cabling. All internal cable segments shall adhere to the same electrical requirements as defined for external cables. Internal cable length shall be a minimum from the equipment receptacles to the bus transceiver circuitry. The stub length shall not exceed 20 centimeters (cm) with a capacitance of less than 25 pF. For internal cabling, stub spacing shall be a minimum of 30 cm. See figure 41. Differences in the stub lengths between all the signals shall not exceed more than 4 cm.

5.8.1.2.3 Cabling electrical characteristic restriction. The internal wiring harness of the Type K devices shall form a part of the total interface bus and provide a through path for other devices connected to the bus. This connectivity shall be provided for other devices even if/when the device in question is powered down or inoperative. To ensure compatibility in all shipboard configurations, certain restrictions on the internal wiring harness shall be imposed.

5.8.1.2.3.1 Signal-to-signal maximum skew times. Any/all signals on the Type K bus shall exhibit a maximum signal-to-signal skew time of 1 ns per stub when measured from external connector to external connector of the cabinet.

5.8.1.2.3.2 Insertion and return loss. Any/all ports when terminated shall exhibit a maximum return loss of 15 dB from 0 to 50 MHz. Any/all ports shall exhibit a maximum insertion loss of 1.6 dB at 10 MHz and 2.5 dB at 50 MHz.

5.8.1.3 Connector requirements. The external Type K cabling and mating connectors and jacks on each cabinet of each Type K device shall use the requirements specified in 30.3.4 of appendix A. Connectors wired to external cables and jacks wired to internal cables shall be in accordance with the signal details provided in 30.4.1.3 of appendix A.

5.8.1.4 Address selection. The address selection of each device shall be user selectable. The address selection mechanism shall be as specified in the individual equipment specification.

5.8.1.5 External termination. An impedance matching terminator shall be placed at each end of the Type K bus system. All terminators shall be exterior to the cabinet of the Type K device. The external termination shall consist of a mating plug and a sealed backshell containing the termination networks which can be placed on any Type K jack of a device. See 30.8 of appendix A.

5.8.1.5.1 Terminators. Each terminator network shall provide a resistive termination for each bus signal consisting of a series connection of one 330, one 150, and one 330 ohm resistors. One 330 ohm resistor shall be connected to ground, the other shall be connected to a 5 volt (nominal) signal called 'TERMPWR.' This resistive impedance combination to the signal pair which is terminated at each end with the 150 ohm resistor shall be 122 ohms (measured across the 150 ohm resistor). See figure 63.

5.8.1.6 Electrical description. Type K shall be implemented as a multiple user bus architecture retaining all the features detailed in SCSI-II except as noted. The multi-user bus protocol shall be maintained for all implementations including point-to-point. Each Type K differential bus signal shall be implemented as one of the following five electrical signal types:

a. Complementary Driven -- complementary driven signals shall be actively asserted, actively negated, and contain an off state. Assertion, negation and off shall be sensed by the receiver in a differential manner.
b. Wired-ORed – wired ORed signals shall be actively asserted, passively negated and contain an off state. Assertion and negation shall be sensed by the receiver in a differential manner.
c. Signal Ground Lines – shall provide zero voltage reference and shall be provided in pairs (GND).
d. Terminator DC -- shall be 5 volt (nominal) and shall be provided in pairs (TERMPWR).
e. Differential Sense – Safety Feature Control Line, Single Ended (DIFFSENS).

5.8.1.6.1 Output characteristics. The output drivers for complementary and wired-ORed drivers shall conform to the requirements of 5.8.1.6.1.1 and 5.8.1.6.1.2, respectively. Voltages on the Type K bus shall be determined using the average measured composite DC voltage (V_{AM}) described in 50.1.2.1 of appendix E.

5.8.1.6.1.1 Complementary driver characteristics. Each individual complementary driver circuit shall consist of a two-port network containing two electrically matched, single-ended, three level transistor driver circuits. For assertion and negation both transistor circuits shall be driven simultaneously to opposite voltage states as complementary signals referred to as SIGNAL(+) and SIGNAL(-) lines. Control line assertion or negation and/or data bit binary logic states shall be indicated by voltage differences between the SIGNAL(+) and SIGNAL(-) driver complementary outputs.

In addition to the two complementary driven states, both SIGNAL(+) and SIGNAL(-) output circuits shall have the ability to be simultaneously "tri-stated" (both ports shall have a high impedance state) which is during data reception periods or to indicate a Type K bus inactivity state (Bus Free).

5.8.1.6.1.2 Wire-ORed driver characteristics. Each individually wire-ORed driver shall consist of a two-port network containing two electrically matched transistor driver circuits. For assertion, both transistor circuits shall be driven simultaneously to opposite voltage states as complementary signals referred to as SIGNAL(+) and SIGNAL(-) lines. Control line assertion shall be indicated by a positive voltage difference between the SIGNAL(+) and SIGNAL(-) driver complementary outputs.

5.8.1.6.1.3 Driver output logic state definitions. The three output states of a Type K complementary or wired-ORed output circuits shall be defined as follows and are shown in figure 42:

State (1) -- a SIGNAL(+) voltage which is greater than + 0.5 volts from the average measured composite DC voltage (V_{AM}) in conjunction with a SIGNAL(-) which is less than - 0.5 volts from the average measured composite DC voltage (V_{AM}) shall indicate an asserted control line state, a binary logic one, or true state for both complementary and wire-OR drivers.

State (2) -- a SIGNAL(+) voltage which is less than - 0.5 volts from the average measured composite DC voltage (V_{AM}) in conjunction with a SIGNAL(-) which is greater than + 0.5 volts from the average measured composite DC voltage (V_{AM}) shall indicate a negated control line state, a binary logic zero, or false state for a complementary driver. Wire-OR drivers shall never assume this state.

State (3) -- both SIGNAL(+) and SIGNAL(-) tri-stated circuit impedances shall be greater than 10K ohms and shall indicate a relinquishment of the bus and/or a deactivated bus (Bus Free) or data receipt for both complementary and wire-ORed drivers. When both signal drivers on the bus are tri-stated, the resulting voltages on the bus lines shall obey the terminator voltage-division states of figure 44.

5.8.1.6.1.4 Output driver characteristics. Each complementary and wire-ORed driver output shall obey the following output characteristics:

a. Each driver shall be capable of driving into 30 meters of terminated LS2U-45 type cable, with the minimum output characteristics as shown in figure 44.
b. Each device transceiver (driver and receiver combination) measured at each SIGNAL(+) and SIGNAL(-) port shall have a tri-state impedance greater than 10k ohms.
c. Each driver port shall have a signal to signal state transition skew time less than or equal to 12 ns when measured at the V_{AM} volt crossing point between any matched SIGNAL(+) and SIGNAL(-) voltages.
d. Each driver SIGNAL(+) and SIGNAL(-) output shall have a rise time between 5 and 60 ns when measured between V_{AM} + 0.5 volts and V_{AM} - 0.5 volts.
e. Each driver port shall supply/sink minimum of 55 mA of current.
f. Each driver port shall be provided with output driver protection for short circuits and shorts to voltage sources between -7 to +12 volts. This shall include voltages supplied from common mode source drivers.
h. Wire-ORed control lines of Type K shall not have a driven low state and will float to the terminator power voltages shown in figure 44.
i. The maximum voltage on any SIGNAL(+) and SIGNAL(-) line shall not exceed 4.4 volts. The minimum voltage on any SIGNAL(+) and SIGNAL(-) line shall be greater than 0 volts. The measured average DC voltage difference between any SIGNAL(+) and SIGNAL(-) pair shall not exceed ± 0.5 Vdc. The minimum peak to peak amplitude shall be greater than 1.25 volts.
j. The driver output characteristics shall conform to EIA RS-485.

5.8.1.6.2 Input characteristics. The minimum values delivered on the bus to an input circuit from each of the three states of a Type K differential input circuit shall be as follows:

5.8.1.6.2.1 Receiver characteristics. Both complementary and wire-ORed signals are sensed by all Type K receivers in an identical differential manner. The signal states shall be defined as follows:

State (1) -- a differential voltage measured between the SIGNAL(+) and SIGNAL(-) lines which is greater than + 1.0 V shall indicate an asserted control line state, a binary logic one, or true state.

State (2) – a differential voltage measured between the SIGNAL(+) and SIGNAL(-) lines which is less than - 1.0 V shall indicate a negated control line state, a binary logic zero or false state.

State (3) -- both SIGNAL(+) and SIGNAL(-) tri-stated circuit impedances greater than 10K ohms shall indicate a relinquishment of the bus and/or a deactivated bus (Bus Free) or data receipt mode. When both signal drivers on the bus are tri-stated, the resulting voltages on the bus lines shall obey the terminator voltage-division states of figure 44. The input receiver shall consider this resultant tri-stated negative differential voltage (- 0.8 V nominal) value as a negated, logic zero, or false state from open collector drivers if it is less than - 35 mV.

5.8.1.6.2.2 Input receiver characteristics. Each control and data bit receiver input shall obey the following characteristics:

a. Each port shall be capable of receiving signals at the end of 30 meters of terminated LS2U-45 type cable, with the minimum input composite characteristics as shown in figure 44.
b. Each device transceiver (driver and receiver combination) measured at each SIGNAL(+) and SIGNAL(-) port shall have a tri-state impedance greater than 10k ohms.
c. Each device transceiver shall be capable of discerning composite signals with rise and/or fall times between 5 and 50 ns.
d. Each driver port shall supply/sink maximum of 2 mA of current as measured at the stub.
e. Input circuit protection shall be provided for short circuits and shorts to voltage sources between - 7 to + 12 volts.
f. Common mode noise immunity shall be provided from signals between -7 to +12 volts. This shall include outputs from common mode sources.
g. Wire-ORed control lines of Type K shall not have a driven low state and will float to the terminator power voltages shown in figure 44.
h. The receiver sensitivity shall be ± 35 mV whereby an asserted signal shall be detected from a voltage greater than +35 mV and a negated signal shall be detected as a voltage less than -35 mV.
i. The total capacitance of each stub length and its corresponding transceiver circuit when measured looking in to the stub length shall be less than 25 pF.
j. The receiver shall be capable of operating with composite differential voltages up to but not exceeding ± 4.4 volts.

5.8.1.6.3 Ground signals. Each Type K device shall supply signal ground (GND) which represents the reference point by which other signals on the bus are generated and measured. Provisions shall be made to allow the separation of the signal ground from the safety or cabinet ground to avoid ground loop noise.

5.8.1.6.4 Bonding and grounding. Each Type K device shall extend the system cabinet ground to the MIL-STD-28840 connector to act as a faraday shield for the Type K signals on the external LS2U-45 cables (see figure 45). The Type K device shall allow Class B bonds to cabinet exteriors in accordance with MIL-STD-1310.

5.8.1.6.5 Terminator DC power. Each Type K device shall supply TERMINATOR POWER (TERMPWR) voltage for pull-up power source to the terminator networks used on all bus signals. This DC power shall be diode coupled to the bus and shall be restricted to values between 4.4 and 5.25 volts (as measured on the bus). TERMPWR sources for the Type K bus shall be able to supply a minimum of 2 amperes and shall be current limited to 3 amperes.

5.8.1.6.6 Differential circuit sense. The differential circuit sense shall be enabled for Type K drivers. This 5 volt protection circuit signal shall be implemented according to figure 46.

5.8.1.6.7 Reserved and unused lines. All Type K devices shall provide total capability, whereby all unused but still designated signal and reserve (RSVD) pairs from the external cable shall be brought through each device at the same electrical transit length as active signals for termination. All Type K external cables shall supply extra signal pairs for each layer for signal connector rework. These spare signal pairs shall be grounded at the Type K device to the same signal ground supplied to the bus. The upper 8 bits and DBP bits on all 8 bit Type K devices shall be brought through each device for terminator connect for compatibility with 16 bit applications.

5.8.1.6.8 Transceiver muting and common mode voltage drivers. When receiving signals from the bus or in an off state, the driver circuits of the transceiver shall be tri-stated (or high impedance state). Driver common mode voltages shall not be a part of the Type K bus electrical characteristics in a Bus Free state. The resulting bus voltages in a Bus Free state shall be determined solely by the applied TERMPWR voltages and the terminator networks only. Any common mode voltages from the driver circuits shall be segregated from the bus via high impedances.

5.8.1.6.9 Additional physical specifications.

Harness Characteristic Impedance	90 to 132 ohms (122 Ohms nominal)
Minimum Gauge Wire for Harnesses	28 AWG
Connector Type (sockets)	MIL-C-28840 (S3)
Jack Type and Keying (pins)	MIL-C-28840 (P3 or D3)

5.8.1.7 Type K bus signals.

5.8.1.7.1 Type K bus signal descriptions. The Type K bus shall contain a total of 30 actively used interface signals grouped into 3 different categories. The Type K bus signals are as follows:

5.8.1.7.1.1 Data and parity. The following signals shall be used to transfer digital words of information between devices:

Data Signals -- The Type K interface bus shall contain 16 bi-directional data signals labeled (DB 0-15). These signals shall transfer data, commands, status, and messages. These signals shall also be used for the bus device ID codes. The ID codes shall be numbered from 0 to 7 corresponding one-to-one with the assertion of the same numbered data signal line. Seven shall be the highest priority. All data signals shall be complementary driven high/low pairs.

Data Bus Parity -- Parity shall be an option in Type K. All Type K devices shall be capable of odd parity. Type K shall use two parity bits "DP" and "DP1." DP is associated with DB 0-7 and DP1 is associated with DB 8-15. Both data bus parity signals shall be complementary driven high/low pairs.

5.8.1.7.1.2 Control signals. The following signals shall be used to convey bus information and data direction between devices:

C/D (Control/Data) -- The C/D signal shall be controlled by the target. The C/D signal shall indicate whether control or data information is being transferred. The negated state shall indicate data. The asserted state shall indicate command, status or message information. The C/D signal shall be a complementary driven high/low pair.

I/O (Input/Output) -- The I/O signal shall be controlled by the target. The I/O signal shall indicate the signal direction with respect to the initiator: asserted indicating information from the target to the initiator, negated indicating transfer from the initiator to the target. The I/O signal shall be a complementary driven high/low pair.

MSG (Message) -- The MSG signal shall be controlled by the target. The asserted MSG signal shall indicate messages from other information transfers. The MSG signal shall be a complementary driven high/low pair.

REQ (Request) -- The REQ signal shall be controlled by the target. The REQ signal shall initiate or sustain information transfers as part of the REQ/ACK handshake protocol. The REQ/ACK handshake shall be used for all information transfers between initiator and target. The REQ signal shall be a complementary driven high/low pair.

ACK (Acknowledge) -- The ACK signal shall be controlled by the initiator. The ACK signal shall respond to the assertion of the REQ signal by the target. The REQ/ACK handshake shall be used for all information transfers between initiator and target. The ACK signal shall be a complementary driven high/low pair.

ATN (Attention) -- The ATN signal shall be controlled by the initiator. The ATN signal shall indicate to the target that a message is available. The ATN signal shall be a complementary driven high/low pair.

RST (Reset) -- The RST signal shall be a wire-ORed signal used by any device on the Type K bus. Normally, the RST signal is asserted only by the initiator during power up. Targets may also assert the RST signal during power up and power down.

BSY (Busy) -- The BSY signal shall be a wire-ORed signal that indicates the Type K bus is in use (busy). The initiator uses the BSY signal during the Arbitration phase. The selected target uses the BSY signal to acknowledge selection indicating the target controls the Type K bus. The target also uses the BSY signal to participate in the Arbitration phase.

SEL (Select) -- The SEL signal shall be a wire-ORed signal controlled by the initiator. The initiator shall use the SEL signal to select a target to perform a command.

DIFFSENS (Differential Circuit Sense) -- The DIFFSENS signal shall be an active high enable for the differential drivers.

5.8.1.7.1.3 Bias signals. The following signals shall be used to bias the bus termination networks and provide voltage reference:

TERMPWR (Terminator Power) -- The TERMPWR lines shall supply the 5 volts (nominal) signal required by the terminator bias networks. All Type K devices shall supply a TERMPWR signal.

GND (Ground) -- The GND lines shall be dedicated as the signal reference ground used by the bus. All Type K devices shall use GND as zero voltage reference.

5.8.1.8 Type K bus functional. Type K shall use the SCSI-II architecture which provides for a protocol containing eight (8) distinct phases as follows:

a. Bus Free phase
b. Arbitration phase
c. Selection phase
d. Reselection phase
e. Command phase
f. Data Transfer phase
g. Status phase
h. Message phase

The Type K bus shall never be in more than one of these phases at any given time. When the Type K bus is between two information transfer phases, the following restrictions shall apply to the Type K bus signals:

a. The BSY, SEL, REQ, REQB, ACK and ACKB signals shall not change.
b. The C/D, I/O, MSG, and DATA BUS signals may change. When switching the DATA BUS direction from out to in, the target shall delay driving the DATA BUS by at least a data release delay plus a bus settle delay after asserting the I/O signal and the initiator shall release the DATA BUS no later than a data release delay after the transition of the I/O signal to true. When switching the DATA BUS direction from in to out, the target shall release the DATA BUS no later than a deskew delay after negating the I/O signal.
c. The ATN and RST signals may change as defined under the descriptions for the attention condition and reset condition.

5.8.1.8.1 Type K bus timing. The bus timing relationships between phases shall be as described as following. Base timing parameters shown in figure 47 shall be used in figures 48-54.

5.8.1.8.1.1 Reset timing. The timing of the Type K bus signals after the assertion of the RST signal line shall be as shown in figure 48. The sequence shall start from the detection of the asserted RST signal line and the corresponding release of all signals by all devices resulting in a Bus Free phase (after a maximum of 800 ns). The RST signal shall be held for a minimum of 25 µs. The sequence shall end with the transition from the Bus Free phase to the next phase (i.e. Selection phase) indicated by the assertion of the BSY signal.

5.8.1.8.1.2 Arbitration/Selection. The timing of the Type K bus signals for the Arbitration and Selection phases shall be as shown in figure 49. The sequence shall start from the detection of the Bus Free phase (once both SEL and BSY signals are false for a minimum of 400 ns) and shall end with the transition from the Selection phase to the next phase chosen by the selected target. This shall be indicated by the release of the SEL signal by the initiator and the setting of the Message, Command, and I/O signals by the selected target indicating the next phase. To distinguish this Selection phase from the Reselection phase, the I/O signal shall be negated.

The initiator may optionally assert the ATN signal during the Selection phase to inform the selected target that a message is available. However, this line may optionally be asserted by the initiator at any time after Selection while the target has control of the bus. The target may optionally request the message by transitioning to a Message Out phase via assertion of the MSG and C/D and negation of the I/O signals.

5.8.1.8.1.3 Arbitration/Reselection. The timing of the Type K bus signals for the Arbitration and Reselection Phases shall be as shown in figure 50. The sequence shall start from the detection of the bus free phase (once both SEL and BSY signals are false for a minimum of 400 ns) and ends with the transition from the Selection phase to the next (to be selected by the target) phase. This shall be indicated by the release of the SEL signal by the initiator and the setting of the Message, Command, and I/O signals by the selected target indicating the next phase.

5.8.1.8.1.4 Asynchronous Information Transfer timing - target to initiator (input). The timing of the Type K bus signals for an Asynchronous Information Transfer phase shall be as shown in figure 51. The sequence shall start from the bus timing restrictions regarding a change in signal direction on the bus and the time required for the initiator to disable its drivers. The sequence shall end when there is no more data to be sent and the target changes the MSG, C/D, and I/O lines to indicate another phase. Each 8 bit data exchange shall be predicated on an ACK/REQ handshake protocol and there shall be no time limit on each exchange.

5.8.1.8.1.5 Asynchronous Information Transfer timing - initiator to target (output). The timing of the Type K bus signals for the Asynchronous Information Transfer phase shall be as shown in figure 52. The sequence shall start from the bus timing restrictions regarding a change in signal direction (I/O signal) on the bus and the time required for the target to disable its drivers. The sequence shall end when there is no more data to be sent and the target changes the MSG, C/D, and I/O lines to indicate another phase. Each 8 bit data exchange shall be predicated on an ACK/REQ handshake protocol which is performed for every byte and there shall be no time limit on each exchange.

5.8.1.8.1.6 Synchronous Data Transfer timing - target to initiator (input). The timing of the Type K bus signals for the Synchronous Data Transfer phase shall be as shown in figure 53. The sequence shall start from the bus timing restrictions regarding a change in signal direction on the bus and the time required for the initiator to disable its drivers. The sequence shall end when there is no more data to be sent and the target changes the MSG, C/D, and I/O lines to indicate another phase. Data exchanges shall be performed in groups which are predicated on predetermined number of REQ signals/bytes which shall be sent prior to receiving the same number of ACK signals in response. The number of REQ and ACK toggles shall be equal per group which supplies a pacing mechanism.

5.8.1.8.1.7 Synchronous Data Transfer timing - initiator to target (output). The timing of the Type K bus signals for the Synchronous Data Transfer phase shall be as shown in figure 54. The sequence shall start from the bus timing restrictions regarding a change in signal direction on the bus and the time required for the target to disable its drivers. The sequence shall end when there is no more data to be sent and the target changes the MSG, C/D, and I/O lines to indicate another phase. Data exchanges shall be performed in groups which are predicated on predetermined number of REQ signals/bytes which shall be sent prior to receiving the same number of ACK signals in response. The number of REQ and ACK toggles shall be equal per group which supplies a pacing mechanism.

5.8.2 Logical requirements. This section contains detailed requirements for logical aspects of the Type K bus. The bus phases, bus conditions, pointers and messages shall be detailed as follows:

5.8.2.1 Selection time-out procedure. A selection timeout procedure shall be implemented as per Option (2) of ANSI X3T9.2/375 standard. Assertion of the RST signal shall not be allowed to accomplish a selection phase timeout.

5.8.2.2 Reselection phase. The Reselection phase shall be a mandatory phase under this standard.

5.8.2.3 Reselection time-out procedure. A reselection timeout procedure shall be implemented as per Option (2) of ANSI X3T9.2/375 standard. Assertion of the RST signal shall not be allowed to accomplish a reselection phase timeout.

5.8.2.4 Synchronous data transfer. When implemented, synchronous data transfer shall be in accordance with ANSI X3T9.2/375 standard.

5.8.2.5 Reset condition. All Type K devices shall implement both a hard reset and a soft reset as per ANSI X3T9.2/375 standard. The hard or soft options shall be user selectable and are mutually exclusive.

5.8.2.6 Abort message. The Abort message shall be implemented for all initiators.

5.8.2.7 Disconnect message. The Disconnect message shall be implemented for all Type K devices.

5.8.2.8 Synchronous data transfer request message. The Synchronous Data Transfer Request message shall be implemented for all Type K devices.

5.8.2.9 Terminate I/O process message. The Terminate I/O Process message shall be implemented for all Type K devices.

6. NOTES

6.1 International interest. Certain provisions of this standard are the subject of international standardization agreement NATO STANAG 4153. When change notice, revision, or cancellation of this standard is proposed which will modify the international agreement concerned, the preparing activity will take appropriate action through international standardization channels, including departmental standardization offices, to change the agreement or make other appropriate accommodations.

6.2 Subject term (key word) listing.

Bipolar pulse
Buffered command word
Burst transfer mode
Data destruct
Data protect
External function
External interrupt
Externally specified addressing
Externally specified indexing
Fiber optic
Forced command word
Intercomputer
Parallel
Peripheral
Protocol
Single pulsed signal
Single word transfer
Sink
Small systems computer interface
Source
System integrity features

6.3 Changes from previous issue. Asterisks are not used in this revision to identify changes with respect to the previous issue due to the extensive nature of the changes.

Preparing activity:
NAVY-SH
(Project MCCR-N101)

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CABLES, INTERFACE CIRCUITS, AND GENERAL I/0 PHILOSOPHY

10. SCOPE

10.1 Scope. This appendix provides information regarding the I/0 interconnecting cables, interface circuits, and cable connector that meet the requirements of this standard. It also describes the I/O interface of NTDS computers to provide an understanding of the functional operations of the computer's I/O section. This appendix forms a mandatory part of this standard.

20. REFERENCED DOCUMENTS

20.1 Government documents.

20.1.1 Specifications. Unless otherwise specified, the following specifications of the issue listed in that issue of the Department of Defense Index of Specifications and Standards (DoDISS) specified in the solicitation form a part of this standard to the extent specified herein.

SPECIFICATIONS

MILITARY

MIL-C-17/134	- Cable, Radio Frequency, Triaxial, 0.245 Inch, 50 Ohm, Waterblocked, Non-Water Blocked.
MIL-C-17/135	- Cable, Radio Frequency, Triaxial, 50 Ohm, Water Blocked and Non-Water Blocked.
MIL-C-24643	- Cable and Cord, Electrical, Low Smoke, for Shipboard Use, General Specification for.
MIL-C-915	- Cable and Cord, Electrical, for Shipboard Use, General Specification for.
MIL-C-28876	- Connectors, Fiber Optics, J Circular Plug and Receptacle Style, Multiple Removable Termini, General Specification for (Metric).
MIL-C-49142/2	- Connector, Triaxial, Radio frequency (Series TRC- Receptacle, Pin Contacts, Jam Nut Mounded. Class 2).
MIL-C-81511	- Connectors, Electrical, Circular, High Density, Quick Disconnect, Environment Resisting: and Accessories General Specification for.
MIL-C-81511/6	- Connectors, Electrical, Circular, High Density, Quick Disconnect, Environment Resisting; and Accessories: Plug, Crimp-Type Contacts, Class A, F and E (Series 2).
MIL-C-85045	- Cable, Fiber Optical, Shipboard, General Specification for (Metric).
MIL-F-49291	- Fiber, Optical, General Specification for (Metric).

(Copies of specifications required by contractors in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting officer.)

30. REQUIREMENTS

30.1 Cable lengths. The maximum length of cables allowed depends on the cable type and the interface type (see table VI). These are the maximum cable lengths for which proper operation is assured for equipment interfaces conforming to this standard. Greater cable lengths may be employed with some equipment under some conditions, depending primarily upon the characteristics of the line drivers and receivers in the individual equipments. Each system shall be analyzed for proper operation with the longer cables.

TABLE VI. Maximum cable lengths (feet/meters).

Interface	Cable type	
	2U or 2UW or LS2U	2AU or 2WAU or LS2AU
Type A	300/91.4	300/91.4
Type B	50/15.2	150/45.7
Type C	100/30.5	250/76.2
Type H	100/30.5	250/76.2
Type D	RG-12A coaxial cable 1000/304.8	
Type E	TRF-8 triaxial cable 985/300	TRF-58 triaxial cable 395/120
Type F	Characteristics as specified in MIL-STD-1553.	
Type G	As specified in RS-449 or RS-232 in EIA Industrial Bulletin 12.	
Type K	LS2U/45 (external only) 82/25 1/	

1/ The length for entire bussing system includes internal and external cabling.

30.2 Cable types. The following cable types shall be used with the respective interface types as shown in table VI:

a. Cables for the parallel interfaces (Types A, B, C, and H):

Type 2AU, 2U, 2WAU, or 2UW in accordance with MIL-C-915
Type LS2AU or LS2U in accordance with MIL-C-24643 (for the low-smoke requirement).

b. Cable for the Type D serial interface:

Type RG-12A coaxial cable.

c. Cables for the Type E interface:

TRF-8 triaxial cable (MIL-C-17/135)
TRF-58 triaxial cable (MIL-C-17/134).

d. Cable for Type J interface:

MIL-F-49291/6
MIL-C-85045

e. Cables for the Type K interface:

Type LS2U in accordance with MIL-C-24643/45 (26 gauge)

30.3 Cable connectors.

30.3.1 Type A, B, C, and H interface connectors. The computer and peripheral equipment I/O connectors may be as shown in table VII, except that M81511 is inactive for new design.

a. The Type A, B, C, or H input channel connector mounted on the computer may be the same as the output channel connector mounted on the peripheral equipment (peripheral output channel is in reference to the peripheral equipment).

b. The Type A, B, C, or H output channel connector mounted on the computer may be the same as the input channel connector mounted on the peripheral equipment (peripheral input channel is in reference to the peripheral equipment).

(Older NTDS computer and peripheral equipment used 90-pin I/0 connectors as follows. The 90-pin equipment mounted I/0 connector (MALE) is NSN 5935-00-841-6204. The cable ending I/O connector (FEMALE) is NSN 5935-00-888-7491.)

TABLE VII. Computer connectors and cable mates (parallel).

Type computer function		Cabinet connector	Cable connector
A, B, C, H	79 Pin input	M38999/20WG35PN	M38999/26WG35SN
A, B, C, H	79 Pin output	M38999/20WG35PA	M38999/26WG35SA
A, B, C, H	85 Pin input	M81511/01EF-85P1	M81511/06EF-01S1
A, B, C, H	85 Pin output	M81511/01EF-85P2	M81511/06EF-01S2
A, B, C, H	92 Pin input	M28840/12AG1P1	M28840/16AG1S1
A, B, C, H	92 Pin output	M28840/12AG1P2	M28840/16AG1S2
E	Triaxial	M49142/02-0001	M49141/01-0001 M49142/01-0002
A, B, C, H	90 Pin	NSN 5935-00-841-6204	NSN 5935-00-888-7491

30.3.2 Type E interface connector. The connector shall be in accordance with MIL-C-49142 and MIL-C-49142/02. The bulkhead connectors mounted on the source and sink shall be identical and shall mate with the connectors on the cable ends. Connectors permanently mounted on equipment shall be in accordance with M49142/02-0001 of MIL-C-49142/02.

30.3.3 Type J interface connectors. The fiber optic interface connector shall meet the requirements of MIL-C-28876 with a requirement for a 62.5/125 fiber @ 1.31 µm of mated optical power loss 1.0 dB (max.). The bulkhead mounted receptacles for the source and sink shall be identical and shall mate with the plugs.

30.3.4 Type K interface connectors. The computer and peripheral equipment Type K connectors (M28840 series) shall be as shown in table VIII. Connector selection shall be as per table VIII. The cable system shall contain common keyed socketed connectors. The common keying allows the Type K cable and terminator assemblies to be generic.

TABLE VIII. Computer connectors and cable mates (Type K).

Type computer function	Cabinet connector	Cable connector
SCSI	M28840/xxAG1z3	M28840/yyAG1S3
xx can be any one of the following: 10,11,12,14,20,21. xx is a receptacle type. yy is a plug type. z can be either P or D.		

30.4 I/0 cable interchangeability. I/0 cable assemblies having connectors with the same number of pins on each end are interchangeable. Input cables may be interchanged with output cables, either directly as with the 90- and 120-pin configurations, or by turning them end-for-end as with cables having the 85-pin connectors. When the equipment requires I/O cable assemblies with different connector types on each end, then the input and output cables are not interchangeable.

30.4.1 Cable connector pin assignments.

30.4.1.1 Cable connector pin assignments for Type A, B, C and H interfaces. Standard function to connector pin assignments for the connectors listed in table VII are specified in tables IX and X. The 85-, 90-, and 120-pin connector pin assignments are specified in table IX. The 79- and 92-pin connector pin assignments are specified in table X. When a channel has fewer than 36 data lines, pins assigned to the unused data bits need have no connection within the equipment. Pin 45 of the 90-pin connector, pin B1 of the 120-pin connector, and pin 74 of the 85-pin connector may be grounded (shield). Pins not listed in table IX or table X may have no connections.

TABLE IX. Function to pin assignments: 120-, 90-, and 85-pin connectors.

Function		120-Pin		90-Pin		85-Pin	
Input	Output	Signal	Return	Signal	Return	Signal	Return
IDA	ODA or Ready	B-5	A-5	1	11	1	6
IDA	ODR or Resume	B-6	A-6	2	12	2	7
EIR	EFA	B-7	A-7	3	13	3	8
EIE	EFR	B-8	A-8	4	14	4	9
Data bit	00	D-1	C-1	9	19	13	21
Data bit	01	D-2	C-2	10	20	14	22
Data bit	02	D-3	C-3	22	33	15	23
Data bit	03	D-4	C-4	23	34	16	24
Data bit	04	D-5	C-5	24	35	17	25
Data bit	05	D-6	C-6	25	36	18	26
Data bit	06	D-7	C-7	26	37	29	39
Data bit	07	D-8	C-8	27	38	30	40
Data bit	08	D-9	C-9	28	39	31	41
Data bit	09	D-10	C-10	29	40	32	42
Data bit	10	D-11	C-11	30	41	33	43
Data bit	11	D-12	C-12	31	42	34	44
Data bit	12	G-1	H-1	32	43	35	45
Data bit	13	G-2	H-2	47	58	36	46
Data bit	14	G-3	H-3	48	59	37	47
Data bit	15	G-4	H-4	49	60	49	58
Data bit	16	G-5	H-5	50	61	50	59
Data bit	17	G-6	H-6	51	62	51	60
Data bit	18	G-7	H-7	52	63	52	61
Data bit	19	G-8	H-8	53	64	53	62
Data bit	20	G-9	H-9	54	65	54	63
Data bit	21	G-10	H-10	55	66	55	64
Data bit	22	G-11	H-11	56	67	56	65
Data bit	23	G-12	H-12	57	68	57	66
Data bit	24	J-1	K-1	70	80	67	75

TABLE IX. Function to pin assignments: 120-, 90-, and 85-pin connectors. - Continued

Function		120-Pin		90-Pin		85-Pin	
Input	Output	Signal	Return	Signal	Return	Signal	Return
Data bit	25	J-2	K-2	71	81	68	76
Data bit	26	J-3	K-3	72	82	69	77
Data bit	27	J-4	K-4	73	83	70	78
Data bit	28	J-5	K-5	74	84	71	79
Data bit	29	J-6	K-6	75	85	72	80
Data bit	30	J-7	K-7	76	86	73	81
Data bit	31	J-8	K-8	77	87	5	12
Shield		J-9	K-9	5	15	10	11
Reserved		J-10	K-10	6	16	82	83
Reserved		J-11	K-11	7	17	19	27
Reserved		J-12	K-12	8	18	84	85
			B-1		45		74
Spare			1/ A-1		1/ 69		
Spare		B-3	A-3	21		20	
Spare		B-4					
Spare		A-4	44		28		
Spare		B-2	A-2	46		38	not used
Spare		B-9	A-9	78		48	
Spare		B-10	A-10	79	not used		
Spare	See the	B-11	A-11	88			
Spare	individual	B-12	A-12	89			
Spare	cable	F-1	E-1	90			
Spare	drawing	F-2	E-2				
Spare		F-3	E-3				
Spare		F-4	E-4				
Spare		F-5	E-5				
Spare		F-6	E-6				
Spare		F-7	E-7				
Spare		F-8	E-8				
		F-9	E-9				
		F-10	E-10				
		F-11	E-11				
		F-12	E-12				

1/ Pins A-1 and 69 are the secondary shield connections.

TABLE X. Function to pin assignments: 79- and 92-pin connectors.

Function		79-Pin		92-Pin	
Input	Output	Signal	Return	Signal	Return
IDA	ODA or Ready	79	78	1	7
IDA	ODR or Resume	77	76	2	8
EIR	EFA	75	74	3	9
EIE	EFR	73	72	4	10
Data bit	00	71	70	14	23
Data bit	01	69	68	15	24
Data bit	02	67	66	16	25
Data bit	03	65	64	17	26
Data bit	04	63	62	18	27
Data bit	05	61	60	19	28
Data bit	06	59	58	33	42
Data bit	07	57	56	34	43
Data bit	08	55	54	35	44
Data bit	09	53	52	36	45
Data bit	10	51	50	37	46
Data bit	11	49	48	38	47
Data bit	12	47	46	39	48
Data bit	13	45	44	40	49
Data bit	14	43	42	41	50
Data bit	15	41	40	52	61
Data bit	16	39	38	53	62
Data bit	17	37	36	54	63
Data bit	18	35	34	55	64
Data bit	19	33	32	56	65
Data bit	20	31	30	57	66
Data bit	21	29	28	58	67
Data bit	22	27	26	59	68
Data bit	23	25	24	60	69
Data bit	24	23	22	71	80
Data bit	25	21	20	72	81
Data bit	26	19	18	73	82
Data bit	27	17	16	74	83
Data bit	28	15	14	75	84
Data bit	29	13	12	76	85
Data bit	30	11	10	77	86
Data bit	31	9	8	78	87
Shield		7		6	
Spares		6	5	5	11
Spares		4	3	12	13
Spares		2	1	20	29
				21	30
				22	31
				32	51
				79	70
				88	89
				90	91
				92	

30.4.1.2 Cable connector pin assignments for Type J interfaces. The Type J signal to connector pin assignments shall be as shown in figure 39 or figure 40.

30.4.1.3 Cable connector pin assignments for Type K interfaces. The Type K signal to connector pin assignments shall be as shown in table XI and figure 55. Each device shall route all signals through its connector pairs as indicated in the pin assignment tables. This will ensure all cables are wired exactly the same and also allows the equipment to be used in a mixed 8/16 bit future implementation or in a complete 16 bit implementation without having to fabricate and install new cables. All signals shall be terminated.

TABLE XI. M28840 pin assignments.

BUS SIGNAL	CONTACT / PIN	CABLE PAIR	CABLE LAYER
REQ-	82	01	Inner Core
REQ+	73	01	Inner Core
ACK-	67	02	Inner Core
ACK+	58	02	Inner Core
TERMPWR	86	03	Layer 1
TERMPWR	77	03	Layer 1
TERMPWR	87	04	Layer 1
TERMPWR	78	04	Layer 1
Spare	11	05	Layer 1
Spare	5	05	Layer 1
Ground	7	06	Layer 1
Ground	1	06	Layer 1
Ground	42	07	Layer 1
Ground	33	07	Layer 1
Ground	62	08	Layer 1
Ground	53	08	Layer 1
Ground	84	09	Layer 1
Ground	75	09	Layer 1
Ground	64	10	Layer 1
Ground	55	10	Layer 1
BSY-	66	11	Layer 2
BSY+	57	11	Layer 2
Spare	29	12	Layer 2
Spare	20	12	Layer 2
SEL-	80	13	Layer 2
SEL+	71	13	Layer 2
DIFFSENS	54	14	Layer 2
Ground	63	14	Layer 2
RST-	68	15	Layer 2
RST+	59	15	Layer 2
Spare	13	16	Layer 2
Spare	12	16	Layer 2
ATN-	65	17	Layer 2
ATN+	56	17	Layer 2
Spare	30	18	Layer 2
Spare	21	18	Layer 2
MSG-	69	19	Layer 2
MSG+	60	19	Layer 2
Spare	31	20	Layer 2
Spare	22	20	Layer 2
I/O-	83	21	Layer 2
I/O+	74	21	Layer 2

TABLE XI. M28840 pin assignments. - Continued

BUS SIGNAL	CONTACT / PIN	CABLE PAIR	CABLE LAYER
Spare	51	22	Layer 2
Spare	32	22	Layer 2
C/D-	81	23	Layer 2
C/D+	72	23	Layer 2
Spare	79	24	Layer 2
Spare	70	24	Layer 2
DB0-	8	25	Outer Layer
DB0+	2	25	Outer Layer
DB8-	43	26	Outer Layer
DB8+	34	26	Outer Layer
DB1-	9	27	Outer Layer
DB1+	3	27	Outer Layer
Ground	85	28	Outer Layer
Ground	79	28	Outer Layer
DB2-	10	29	Outer Layer
DB2+	4	29	Outer Layer
DB9-	44	30	Outer Layer
DB9+	35	30	Outer Layer
DBP1-	61	31	Outer Layer
DBP1+	52	31	Outer Layer
DB3-	23	32	Outer Layer
DB3+	14	32	Outer Layer
DB10-	45	33	Outer Layer
DB10+	36	33	Outer Layer
DB4-	24	34	Outer Layer
DB4+	15	34	Outer Layer
DB11-	46	35	Outer Layer
DB11+	37	35	Outer Layer
DB5-	25	36	Outer Layer
DB5+	16	36	Outer Layer
DB12-	47	37	Outer Layer
DB12+	38	37	Outer Layer
DB6-	26	38	Outer Layer
DB6+	17	38	Outer Layer
DB13-	48	39	Outer Layer
DB13+	39	39	Outer Layer
Spare	91	40	Outer Layer
Spare	90	40	Outer Layer
DB7-	27	41	Outer Layer
DB7+	18	41	Outer Layer
DB14-	49	42	Outer Layer
DB14+	40	42	Outer Layer
Spare	89	43	Outer Layer
Spare	88	43	Outer Layer
DB15-	50	44	Outer Layer
DB15+	41	44	Outer Layer
DBP-	28	45	Outer Layer
DBP+	19	45	Outer Layer
None	6	None	-
None	92	None	-

30.4.2 Function to color code assignments.

30.4.2.1 Function to color code assignments for Type A, B, C and H interfaces. Standard function to cable color code assignments are listed in table XII. This table applies to cables with one or more wire pairs.

TABLE XII. Function to color code assignments for 42- to 60-pair digital I/O transmission cables.

Function	Twisted pair no.	Signal	Return	Function	Twisted pair no.	Signal	Return
IDR, ODA, or Ready	40	ORN	BRN	Data bit 27	28	RED	PRP
IDA, ODR, or Resume	39	ORN	BLU	Data bit 28	29	RED	TAN
EIR or EFA	38	GRN	PINK	Data bit 29	30	RED	PINK
EIE or EFR	37	GRN	TAN	Data bit 30	31	GRN	ORN
Data bit 00	15	WHT	BLU	Data bit 31	32	GRN	BLU
Data bit 01	14	WHT	ORN	Data bit 32	17	WHT	GRAY
Data bit 02	24	RED	BLU	Data bit 33	36	GRN	PRP
Data bit 03	21	WHT	PINK	Data bit 34	16	WHT	BRN
Data bit 04	20	WHT	TAN	Data bit 35	35	GRN	YEL
Data bit 05	18	WHT	YEL	SPARE	41	ORN	GRAY
Data bit 06	19	WHT	PRP	SPARE	42	ORN	YEL
Data bit 07	7	BLK	GRAY	SPARE	43	ORN	PRP
Data bit 08	1	BLK	WHT	SPARE	44	ORN	TAN
Data bit 09	6	BLK	BRN	SPARE	45	ORN	PINK
Data bit 10	5	BLK	BLU	SPARE	46	BLU	BRN
Data bit 11	13	WHT	GRN	SPARE	47	BLU	GRAY
Data bit 12	34	GRN	GRAY	SPARE	48	BLU	YEL
Data bit 13	25	RED	BRN	SPARE	49	BLU	PRP
Data bit 14	22	RED	GRN	SPARE	50	BLU	TAN
Data bit 15	2	BLK	RED	SPARE	51	BLU	PINK
Data bit 16	8	BLK	YEL	SPARE	52	BRN	GRAY
Data bit 17	9	BLK	PRP	SPARE	53	BRN	YEL
Data bit 18	3	BLK	GRN	SPARE	54	BRN	PRP
Data bit 19	4	BLK	ORN	SPARE	55	BRN	TAN
Data bit 20	10	BLK	TAN	SPARE	56	BRN	PINK
Data bit 21	11	BLK	PINK	SPARE	57	GRAY	YEL
Data bit 22	12	WHT	RED	SPARE	58	GRAY	PRP
Data bit 23	33	GRN	BRN	SPARE	59	GRAY	TAN
Data bit 24	26	RED	GRAY	SPARE	60	GRAY	PINK
Data bit 25	27	RED	YEL				
Data bit 26	23	RED	ORN				

30.4.2.2 Signal wiring of LS2U/45 cable to M28840 connector for Type K interfaces. The assignment of Type K bus signals to LS2U/45 cable pairs is given in table XI. Figure 55 is a pictorial of the MIL-C-28840 connector which shows the mapping of Type K bus signals to connector pin pairs as given in table XI. Figure 55 also includes a cross section of the LS2U/45 cable type.

30.4.3 Alternate color code assignments. Alternative color code assignments are specified to standardize the use of cable with less than 42 wire pairs.

30.4.3.1 Color code assignments for 30-pair cable. Table XIII specifies function to color code assignments for use with 30-pair parallel digital I/O transmission cables. The 30-pair cable may be used with any 16- or 24-bit parallel I/0 channel.

TABLE XIII. Function to color code assignments for 30-pair digital I/O transmission cables.

Function	Twisted pair no.	Signal	Return
IDR, ODA, or Ready	30	RED	PINK
IDA, ODR, or Resume	29	RED	TAN
EIR or EFA	28	RED	PRP
EIE or EFR	27	RED	YEL
Data bit 00	15	WHT	BLU
Data bit 01	14	WHT	ORN
Data bit 02	24	RED	BLU
Data bit 03	21	WHT	PINK
Data bit 04	20	WHT	TAN
Data bit 05	18	WHT	YEL
Data bit 06	19	WHT	PRP
Data bit 07	7	BLK	GRAY
Data bit 08	1	BLK	WHT
Data bit 09	6	BLK	BRN
Data bit 10	5	BLK	BLU
Data bit 11	13	WHT	GRN
Data bit 12	26	RED	GRAY
Data bit 13	25	RED	BRN
Data bit 14	22	RED	GRN
Data bit 15	2	BLK	RED
Data bit 16	8	BLK	YEL
Data bit 17	9	BLK	PRP
Data bit 18	3	BLK	GRN
Data bit 19	4	BLK	ORN
Data bit 20	10	BLK	TAN
Data bit 21	11	BLK	PINK
Data bit 22	12	WHT	RED
Data bit 23	23	RED	ORN
Spare	16	WHT	BRN
Spare	17	WHT	GRAY

30.4.3.2 Color code assignments for 19- and 24-pair cable. Table XIV specifies function to color code assignments for use with 19- or 24-pair digital I/O transmission cables. The 24-pair cable may be used with any 16-bit parallel I/O channel. The 19-pair cable may be used with 16-bit parallel I/O channels where the EFR or EIE function is not implemented (see 5.1.1.1.2, 5.1.1.2.2, and note 1 to tables II and III).

TABLE XIV. Function to color code assignments for 19- and 24-pair digital I/O transmission cables.

Function	Twisted pair no.	Signal	Return
IDR, ODA, or Ready	19	WHT	PRP
IDA, ODR, or Resume	18	WHT	YEL
EIR or EFA	17	WHT	GRAY
EIE or EFR	20	WHT	TAN
Data bit 00	7	BLK	GRAY
Data bit 01	8	BLK	YEL
Data bit 02	14	WHT	ORN
Data bit 03	12	WHT	RED
Data bit 04	11	BLK	PINK
Data bit 05	9	BLK	PRP
Data bit 06	10	BLK	TAN
Data bit 07	5	BLK	BLUE
Data bit 08	1	BLK	WHT
Data bit 09	4	BLK	ORN
Data bit 10	3	BLK	GRN
Data bit 11	6	BLK	BRN
Data bit 12	16	WHT	BRN
Data bit 13	15	WHT	BLUE
Data bit 14	13	WHT	GRN
Data bit 15	2	BLK	RED
Spare	21	WHT	PINK
Spare	22	RED	GRN
Spare	23	RED	ORN
Spare	24	RED	BLUE

30.4.4 Connector keying.

30.4.4.1 Connector keying for Type A, B, C and H interfaces. Keyed connectors used on cable assemblies are keyed with the mating connector mounted on the equipment to prevent improper mating of the connectors and provide alignment of male connector pins with the female connector. The 90- and 120-pin connectors have the same keyed input and output. Construction of cables using the 85-pin connectors may use an input connector in accordance with MIL-C-81511 and MIL-C-81511/6 for type M81511/06EF-0151 on one end and an output connector. Type M81511/06EF-01S2, on the other end to be compatible with the cable connector requirements of this standard.

30.4.4.2 Connector keying for Type K interface. The connector keying code for the Type K interface uses common socketed connectors which are different than the ones specified for Type A, B, C and H in an attempt to eliminate confusion when installing a system containing both Type A, B, C or H channels and Type K channels that use the same type connector. The keying code is also specified to be implemented at both ends of the Type K cable. The Type K cable system is not a point-to-point bus like Type A, B, C or H and does not need to differentiate cable ends as "IN" or "OUT". By supporting a common keying code on both ends of the Type K cable system and terminator, the Type K cable can be generic.

30.5 Computer interface. A computer transfers data through the use of an I/O interface. The transfer of data between the computer and the outside world, represented by peripherals, is controlled by the interaction of hardware defined operations and a computer program consisting of I/O instructions. The relationship that exists between the computer and the peripherals during any I/O transfer is as follows: the computer is the controlling device or master while the peripheral is the controlled device or slave. The two basic modes of transfer are input and output where transfers are always defined in relationship to the computer. Data is transmitted in either a serial or parallel manner depending upon the physical configuration of the channel. Since the basic I/O philosophy is relatively independent of the technique. this appendix describes the I/O philosophy using only parallel interface examples.

30.5.1 Channels. Peripherals are connected to the computer by cables that transfer both data and control signals. An input cable and an output cable make up a physical channel. The usual practice is to connect one peripheral device to the computer through a channel. Each channel is bi-directional and able to handle data transfers up to a specified I/O word length. The data size transferred from the peripheral may be any size up to an I/0 word in length, but to the computer it will always appear to be an I/O word in length. For data transfers from the computer, the computer may transfer data whose length is equal to an I/0 word, but the peripheral may (because of its function) only sample a portion of that data word. The common practice is to arrange channels in a computer in groups of four in order to conserve hardware and also allow intermixing of interface levels. When channels are grouped, one output data register and data line driver set is used for four output channels; however, separate control line circuits are used for each channel. The input channels, either grouped or separate, have separate input amplifier sets and control line circuits for each channel. Data and control signals are maintained on the channels by a specific voltage level called the channel interface. The interface level on any channel or channel group may be NTDS fast, (-3 V), NTDS slow, (- 15 V), ANEW or High Throughput Parallel (+3.5 .V), NTDS serial (+ or -3.25 V), NATO serial (+ or -0.6 V), fiber optic NATO serial, or SCSI-II (8/16 bit fast).

30.5.2 Priority. The computer is able to have all channels active simultaneously. Because of the activity required to service all channels, the computer shall maintain a system where all channels can be serviced without letting any one channel dominate the computer. For this reason, a priority system called channel priority has been established that allows for orderly processing of data transfers on all channels. In addition, because a channel is able to carry on data transfers of more than one function (input, output, external function. and interrupt), a priority scheme for function has also been established. The priority scheme operates to resolve conflicts when more than one request exists at any one moment in the computer. While multiple activities on many channels may be possible, the actual number of requests present at any one time may be fewer because of the asynchronous nature of the peripherals being serviced. In other words, all activities on all channels will not make requests at the same moment in time.

30.5.3 I/O. The exchange of control signals or handshaking between computer and peripheral is used to control the transfer of data between the computer and peripheral. A control signal called a request is sent by the peripheral to the computer whenever it is ready to transfer a word of data to, or desires a word of data from the computer. When the computer recognizes this control signal, it will allow the transfer of data to take place and generate a control signal to the peripheral, called an acknowledge. This acknowledge is interpreted by the peripheral as a signal to take the data off the lines or clear the data lines. Once the acknowledge signal has been recognized, the peripheral is free to prepare itself to accept or send another word. For each word of data transferred, one request is generated by the peripheral and one acknowledge is generated by the computer. In certain types of transfers, referred to as transfers with force, the computer can send a word to a peripheral with no request from the peripheral. In any event, a handshaking type of interface is used, and the degree of handshaking is specified in section 5 of this standard for each type of interface.

30.5.4 Basic transfer types. There are four types of transfers: EF, EI, OD, and ID. When data is transferred out of or into the computer, the transfer takes place from main memory to the peripheral or vice versa. The location in main memory is called a buffer and is completely under the control of the programmer. The following discussion of buffering is not intended to specify buffer requirements of any one computer; it is included to more completely explain the I/O philosophy. The programmer defines the buffer using buffer control words (BCW) to describe two addresses, the initial address control word (IACW),

and the terminal address control word (TACW). The location in main memory affected by the transfer of data is specified by the IACW of the BCW. The IACW is the initial memory location in the buffer that will be filled on input or emptied on output. The TACW is the final memory address filled or emptied. The size of the buffer is limited by the length of the control word and the memory size of the computer. The buffer may range in size from one word, in which case the IACW and TACW are the same, up to the limit that can be described by the control words. For each transfer of data, the following operations concerning the BCW take place:

a. Transfer of data occurs.
b. Comparison of IACW and TACW is made.

(1) If equal, all transfer have been made.
(2) If unequal, more transfers can be made.

c. The IACW is incremented by 1.

30.5.4.1 Transfer to special or assigned memory. If the computer finds that an equality exists, the transfer of data will be terminated. If an inequality exists, another transfer can take place. In both instances, the IACW is incremented. The computer has special or assigned memory locations that will hold the BCW while buffers are active. As part of the initiate buffer instruction, BCW's are transferred from a program area of main memory to special or assigned memory locations. Each location corresponds to a particular function on a particular channel.

30.5.5 EF (see figure 56). There are two types of EF transfer, buffered EF and EF with force (unbuffered) described in 30.5.5.1 and 30.5.5.2, respectfully. In either case, the purpose of the EF transfer is to send a command to the peripheral device to tell the peripheral what functions, within its capability, to perform. In other words, EF commands are instructions within the repertoire of the peripheral to tell it what to do. An EF command word would be used, for example, to select a peripheral mode of operation. It is important to note that the peripheral device shall store the EF command in its internal function register throughout the entire duration of the particular mode of operation. This is necessary so that the peripheral will remain in the selected mode and thus know what operation it is performing.

30.5.5.1 Buffered EF. Buffered EF transfers are very similar to OD transfers with the exception that the word sent to the peripheral is a command word and not a data word. To cause an EF transfer to take place, the peripheral sends an EFR to the computer. If the computer has an EF buffer active, it will read the command word from memory and send it out on the OD lines accompanied by an EFA. The command may be more than one word in length, but only one word is sent for each request/acknowledge sequence. In this case the request/acknowledge is the EFR/EFA. These lines, EFR/EFA, are unique to the EF transfer. However, the data lines that carry the EF command word are common to both output data word transfers and EF command word transfers. The peripheral detects the difference between command words and data words by means of their unique acknowledge signal, that is, EFA with an EF command word, ODA with an OD word.

30.5.5.2 EF with force. Many peripheral devices (designed for earlier computers and systems) are not able to generate an EFR. In this case, the computer may send an EF command word and an EFA with no request from the peripheral. This is said to be an EF with force. Figure 56 applies, except that the EFR line is not used. One command word is transferred with each forced EFA sent by the computer. The computer shall be programmed to execute a special instruction (the force EF instruction) for each command word to transferred in order to internally generate the EFR signal.

30.5.6 OD (see figure 57). The purpose of this operation is to transfer data from a computer memory buffer to the peripheral. One data word is transferred for each request/acknowledge. The request that the peripheral sends is an ODR. If the computer has an active output buffer (that is, the computer is in a condition on that specific channel, so that it can logically sense the request), a data word is obtained from memory and sent to the peripheral by means of the OD lines. An ODA is sent to the peripheral concurrently with the data. The data is held on the lines in a stable state and the ODA held in the binary one state for only a short period of time that varies with type of interface being used. For actual timing, refer to the appropriate section of the standard. During acknowledge time, the peripheral device shall accept the data or it will be lost after the specified time has elapsed.

30.5.7 ID (see figure 58). The purpose of this operation is to store data that is being transferred from the peripheral device in the memory of the computer. One data word is transferred for each request/acknowledge sequence. In this case, the request is the IDR and the acknowledge in the IDA. The peripheral places a word of data on the ID lines and sets the IDR line to indicate a data word is on the ID lines. If the computer has an input buffer active (that is, the computer is in a condition on that specific channel, so that it can logically sense the request), it will store the data in main memory and send a IDA. The data and the request are held in a binary "one" state until the acknowledge is received by the peripheral. When the peripheral receives the acknowledge it drops the request and then prepares the next word for transfer to the computer. When the next word is ready, the peripheral sends another request. The cycle repeats until the peripheral has no more data to send or the input function is terminated (that is, the input buffer terminates and the computer automatically shuts off the transfer on that channel and refuses to accept additional data).

30.5.8 EI (see figure 59). The purpose of this operation is to provide the peripheral with the ability to interrupt the computer. This interrupt may or may not be accompanied by a status code generated by the peripheral. If the peripheral does not generate a specific interrupt status code, then the code should be all zeros. The transfer is very similar to the input operation, except that the input word is a status word indicating either a particular state of the peripheral or some condition relative to the I/O operation. A status word is not a data word since it indicates that a particular equipment or I/O condition exists, for example, input operation complete, parity error, equipment desires to input to the computer, and so forth. The status information may be several words, but only one word is transferred for each request/acknowledge sequence. In this case, the request/acknowledge is an EIR/IDA. The computer controls whether the peripheral can formulate and send an EI by means of the EIE line. This line is active if there is an active EI buffer (an active EI buffer means that the computer is in a condition, on that particular channel, so that it can receive interrupt data). If its active, the peripheral may formulate a status word. The peripheral puts the status word on the data lines and sends an EIR to the computer. The computer responds by accepting the status word on the input lines and sending a IDA to the peripheral. The IDA is used for either ID or interrupt data. Therefore, the peripheral shall be able to discriminate between an IDA to an EIR and an IDA to an IDR. So that the peripheral can differentiate a data word acknowledge and EI status word acknowledge, the computer will deactivate the EIE line while the IDA is sent in response to an EIR. Some computers do not have the EIE line, and therefore interrupts are always enabled unless disabled by program instruction. EI are viewed slightly differently depending on whether you are looking at them from the computer or peripheral.

30.5.8.1 From the computer viewpoint. There are two basic types of interrupts: these are the external and the internal interrupts. The EI originate in a peripheral device and have status words (interrupt code) associated with them. The internal interrupts are generated within the computer generally a result of some internal status condition. For the purpose of this appendix, only the EI will be discussed, since their origin is the peripheral device.

30.5.8.2 From the peripheral viewpoint. When an EI is generated in a peripheral device, that device provides a status word as information to the computer. The content and format of the status word is unique to that device. The computer, upon detection of the EI signal from the peripheral, stores the status word in a memory location and sends a IDA to indicate that the status word has been stored.

30.5.8.3 Interrupt codes. EI indicate equipment status. The number of unique status conditions is proportional to the complexity of the peripheral device. Whenever there is more than one status condition, some means of identification of the particular conditions is necessary. A method commonly used is to associate a particular condition with a number or code. Thus the term interrupt code means that a particular number (code) is associated with a particular status condition. The actual code associated with a status condition can be very simple, for example, sequentially numbering the status conditions and using that number as the interrupt code. Another possible method of identifying the status condition is to assign a bit position to each status condition. Thus the interrupt code can indicate the entire status in one word, that is, a bit is set (binary one) if the status condition exists. The particular method of coding status conditions will have to consider the following:

a. Complexity of the device.
b. Use of the device in a particular system, that is, how does the peripheral affect the overall operation of the system.
c. How many status conditions are realistic from a system stand point and how complex the computer program need be in order to effectively utilize the peripheral.
d. Do not include interrupts for the sake of having interrupts. Some devices do not require the incorporation of interrupts, either because of their simplicity, or because of their use in the system.

30.5.8.4 Design constraints. In the design of peripheral equipment which utilize EI, there are two major design constraints:

a. The peripheral shall be so designed that it is impossible for the peripheral to simultaneously set or set sequentially the IDR and EIR signals so that both signals are presented to the computer for the same input word.
b. Some means of determining that an IDA is a response to an EIR rather than an IDR (since the same acknowledge signal line is used for both) shall be incorporated into the peripheral device.
c. Conversely, some means of determining that the IDA signal is a response to an IDR, rather than an EIR shall be incorporated into the design of the peripheral device

These constraints are further explained in 5.1.1.2.

30.5.8.5 EIR/IDR interlock. The EIR/IDR constraints indicate an interlock is required between the IDR and the EIR so that both the computer and the peripheral device will know which is which. The standard specifies that the IDR signal shall be cleared at least 20 µs before the EIR can be set and visa versa. This means that 20 µs after the IDR signal has been cleared because of the receipt of the IDA, the interrupt code can be generated and the EIR signal can be set. The timing restriction further states that the EIR signal shall be cleared at least 20 µs before the IDR signal can be set. This means that if the IDA is a response to an EIR, the EIR signal shall be in the cleared state at least 20 µs, due to an input acknowledge (IA) in response to the EIR, before the IDR can be set. The reason for the above restrictions is so that the peripheral and the computer do not become confused about ID and EI status data. It should be noted, upon examination of the input cable interface signals, that the ID lines and the IDA signal are common to both ID an EI status data. The only difference, from an interface signal viewpoint, between ID and EI status data is that ID is signified by the IDR while EI status data is signified by the EIR signal. Therefore, the peripheral device shall ensure that it can determine when an IDA is a response to an IDR and when the IDA is a response to an EIR, otherwise, both computer and peripheral will become confused. The IDR/EIR interlock can be accomplished by timing triggered from the IDA.

30.6 IC interface philosophy. The IC mode is used when two computers transfer data between each other. Computers can be designed so that normal data channels can be converted, by means of switches, plug-in modules, printed circuit cards, and so forth to operate in the IC mode. When a normal data channel is converted for use in the IC mode, only the output channel requires modification. The input channel is not modified. In order to convert a normal output channel to operate in the IC mode, the following modifications are required:

a. The EFA is not a single pulse as it is in a normal channel; instead, the EFA, when set to the binary one state, shall remain set until a Resume signal is received.
b. The normal channel ODA signal is labeled the Ready signal for IC mode. The Ready signal when set to the binary one state shall remain set until the Resume signal is received. In other words, the normal channel ODA has been renamed Ready and is not single pulsed as it is for normal channel operations.
c. The normal channel ODR line is renamed the Resume for IC mode. In addition for the IC mode, the Resume signal clears either the EFA or Ready, whichever is set.

An output channel on one computer connects to an input channel on the other computer, and, correspondingly, an output channel of the second computer connects to an input channel of the first computer. Each computer looks like a peripheral device to the other input.

30.6.1 Data and control signals. The control signal and lines governing IC communication are shown in figure 60 which illustrates the interface between two computers. Computer A is transmitting to computer B. The selection of a given channel as an IC channel affects only the logic concerning the output and EF buffers. A channel sending data or EF messages to a given peripheral equipment holds the data in the output registers for a fixed minimum time period, after which any other output or EF request on any channel can cause the data to be changed. However, a channel sending data or EF messages to another computer shall hold the information in the output registers until the receiving computer acknowledges receipt of the data. This acknowledge signal is received on what is know as the ODR line when not in IC mode. This line, in the IC mode, is known as the Resume line. The control signals in the input cable are the same for IC communication as for communication with peripheral equipment. In the output cable, Ready and Resume signals are used to control the IC transfer of data.

30.7 Examples of I/O operations. The following discussion utilizes the NTDS paper tape unit as an example to illustrate typical EF output and input operations (see figure 61). Figure 62 illustrates the bit position coded EF command word. When a particular mode or function is to be selected, an EF command word with the appropriate bit or bits set is sent to the unit.

30.7.1 EF codes. The peripheral is required to store the EF code in an internal function register. Refer to figure 61 block diagram of the punched tape unit. The only exception to the EF code storage requirement is that the master clear EF code bit is not stored. The reason for not storing the master clear bit is that the clearing of all circuits within the peripheral is a one shot operation that is accomplished upon detection of the EFA signal and the master clear bit being in the binary one state. The peripheral is designed so that the master clear bit can be set in conjunction (contained in the same EF command word) with any other function bit and the master clearing of the peripheral will take place first, and then the selected function will be performed (for example, master clear and enable punch). See the following example:

7 6 5 4 3 2 1 0	
0 0 0 1 1 0 0 0	(30g) will cause the unit to be first master cleared and then enable the punch (that is, start punch motor and set the ODR).

Certain combinations of bits set in the EF command word are illegal, for example, both bits 4 and 7 set to binary one indicates that the punch should be both enabled and disabled at the same time. If damage to equipment would result from illegal EF command bit combinations, then the control logic shall be designed to ignore or nullify those illegal combinations. The particular bit or bits selected to perform a given function

or set of functions is dependent on the nature of the peripheral device and is a function of system design. There are no restrictions from the computer standpoint as to the EF command word format, other than computer word length. However, it is usual practice to use the lower bits first, and expand upward as necessary. In general, a historical analysis of various peripheral EF command words reveals that certain major functions such as master clear, output mode, and input mode seem to use the standard bit positions, regardless of the nature of the peripheral (for example, master clear 23, output mode 24, and input mode 25). The actual EF command used (designed into the hardware) shall be appropriate to the device and shall be foolproof. Foolproof means that illegal combinations will be ignored by the hardware or will not in any way damage the equipment or cause unexpected results.

30.7.2 Example of an output operation. This example is intended to more clearly illustrate the relationship of computer and peripheral that shall exist during an output operation. The paper tape unit is a very simple device. The only output function that it can perform is punching paper tape. It is assumed that the enable punch EF command has been previously sent to the paper tape unit. The paper tape unit is therefore ready for OD (the ODR signal is set). Assuming that the computer has an active output buffer set up for that channel, the computer I/O section will sense the ODR and respond with OD word and an ODA. The paper tape will detect the ODA, accept the output word, store the output word in the punch data register, and clear the ODR signal. The data stored in the punch register will be punched as controlled by timing of the punch control logic. When the punching is complete, the punch control logic will again set the ODR signal indicating that the punch is ready for another word from the computer. The above sequence will continue until the computer output buffer is exhausted, that is, the buffer terminates. The ODR repetition rate is a function of the speed of the punch, that is, the ODR's rate is determined by how fast the punch can use the data. The OD rate for any peripheral is determined by the speed of the output device (in this case, the punch) and the amount of other computer I/O activity and the priority of the peripheral, which is based on the channel and function for all I/O.

30.7.3 Example of an input operation. The NTDS paper tape unit is used to explain the relationship of the computer and the peripheral that shall exist during an input transfer. It is assumed that previous to activating the computer channel for input, an EF command (enable reader) was sent to the paper tape unit. It is also assumed that the paper tape to be read has been positioned at the read station so that it can be read. If the above conditions have been met, the reader will have read the first frame, placed the data on the data lines to the computer, and set the IDR signal. If the channel is active for input, the computer will sense the IDR, read the ID lines, and respond with an IDA. When the paper tape unit receives the IDA, it will clear the IDR signal, clear the ID lines, read the next frame, place the data on the data lines to the computer, and set the IDR signal. The sequence of the request/acknowledge continues until the input buffer is filled, at which time the computer automatically terminates the buffer. The IDR will still be set, but the computer input channel is inactive; therefore, the IDR is not sensed by the I/O section. Since the data transfer stops because of buffer termination, the tape is stopped.

30.8 Type K external termination. The external bus terminators to be used are placed on both ends of the Type K bus system. The external termination method shall involve a mating connector plug and sealed backshell that can be used on any Type K receptacle at each end of the Type K bus system. See figure 63 for a typical implementation of the Type K interface bus termination. The terminator shall mate with the M28840 cabinet connector and shall meet all electrical characteristics detailed in this standard. The terminator connector shall adhere to the pin assignment as given in table XI. Reference part number 13219389-03. This part has been produced in accordance with this standard.

30.9 Summary. Information is transferred to and from the computer by means of the I/O section. The interaction of hardware- and software-defined operations causes an orderly transfer of data. Four data transfers are possible: EF, output, EI and input. Instructions within a user's program cause buffers to be activated for a particular function. The I/O section then governs the exchange of data between computer and peripheral, transferring data when requested and terminating the buffer when data transfer is complete.

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SPECIAL REQUIREMENTS FOR CP-642A/B AND CP-789 COMPUTERS

10. SCOPE

10.1 Scope. This appendix provides information regarding the special requirements applicable to CP-642A/B and CP-789 computers and is a mandatory part of this standard.

20. REFERENCED DOCUMENTS

Not applicable.

30. DEFINITIONS

Not applicable.

40. GENERAL REQUIREMENTS

Not applicable.

50. DETAILED REQUIREMENTS

50.1 Functional requirements.

50.1.1 Interface type. The interface type used by the computer and related equipment is the Type A interface as specified in 5.2.1.

50.1.2 Channel configuration. Communication with the computer is carried on in a parallel mode of up to a 30-bit data word. The computer is provided with 14 I/O channels consisting of two IC channels and 12 computer-peripheral channels. The IC channels are assigned to I/O channels 0 and 1.

50.1.3 Control signals.

50.1.3.1 Computer-peripheral communications. The control lines used by the computer to communicate with the peripheral equipment are specified in table XV. The sequence of events for data transfer applicable to all control lines specified in table XV are specified in 5.1.1 through 5.1.1.4.

TABLE XV. Computer-peripheral control signals.

Function	Channel	Direction of signal
IDR	Input	Peripheral equipment to computer
IDA	Input	Computer to peripheral equipment
EIE	Input	Computer to peripheral equipment
EIR	Input	Peripheral equipment to computer
ODR	Output	Peripheral equipment to computer
EFR	Output	Peripheral equipment to computer
ODA	Output	Computer to peripheral equipment
EFA	Output	Computer to peripheral equipment

50.1.3.2 IC communication. The control lines used by the computer to communicate with another computer are specified in table XVI. The sequence of events for data transfer applicable to all control lines in table XVI are specified in 5.1.2, except for the input buffer active control line as specified herein.

TABLE XVI. IC control signals.

Function	Direction of signal
Ready (IDR)	Transmitting computer to receiving computer
Resume (IDA)	Receiving computer to transmitting computer
Input buffer active 1/	Receiving computer to transmitting computer

1/ Input buffer active line is set and cleared by the computer receiving ID and is detected by the computer transmitting OD.

50.2 Serial requirements for CP-642A.

50.2.1 CP-642A/CP-642A IC communication. When connected as shown on figure 64, two CP-642A computers are able to transfer data as specified herein. The transmitting computer holds the data on the OD lines until either:

a. The receiving computer sets the Resume line, or
b. The transmitting computer program intervenes to resolve the no-Resume condition.

50.2.1.1 Input buffer. The input buffer active line is set by the receiving computer whenever an input buffer has been established. The input buffer active line is detected by the transmitting computer by the execution of a special instruction. Therefore, the use of the input buffer active line enables the transmitting computer to initiate the IC output buffer only when assured that the receiving computer IC input buffer has been initiated. IC data transfer from the transmitting computer to the receiving shall be as follows:

a. The receiving computer initiates an input buffer and sets the input buffer active line.
b. The transmitting computer, by executing a special program instruction, detects the input buffer active line.
c. The transmitting computer initiates an output buffer on the IC output channel.
d. The transmitting computer places a data word on its OD lines.
e. The transmitting computer sets the Ready line to indicate that data is available.
f. In accordance with internal priority, the receiving computer detects the setting of the Ready line of the transmitting computer (which is recognized as the IDR).
g. The receiving computer samples the ID lines.
h. The receiving computer sets the IDA line.
i. The transmitting computer detects the setting of the IDA line of the receiving computer (which it recognizes as the Resume line).
j. The transmitting computer clears the Ready line before placing the next word of data on the OD lines, and the receiving computer clears the IDA line before sampling the next word on the ID lines.

The computer shall repeat steps "d" through "j" until the block of words specified by the buffer control word is transferred.

50.2.1.2 CP-642A/non-CP-642A IC communications. The IC interface between a CP-642A computer and a non-CP-642A computer has the special relationship between the control lines as shown in figure 65. The control lines shown on figure 65 are defined in 5.1.2 and herein. Precautions should be taken if the control line combinations shown in figure 65 are used. These program limitations are defined by the activities utilizing this IC interface and depend upon the system requirements defined for that application. The functions to be considered are as follows:

a. EIR detected by the CP-642A (EFA from the non-CP-642A) input channel causes the CP-642A to interrupt the CP-642A program and execute the instruction placed at the timeout interrupt entrance address.
b. EFA signal having a finite duration may not be set long enough for the CP-642A to detect it as an EIR.
c. Input buffer active line and EIE line are computer program controlled and shall be cleared and set for each word transferred.

50.2.2 Data transfer rate. The maximum data transfer rate for a single computer input or output channel is as follows:

Type A (Slow interface)
Input channel - 25 kilohertz (KHz)
Output channel - 30 KHz

50.3 Special requirements for CP-642B.

50.3.1 Functional requirements.

50.3.1.1 Interface type. The interface types used by the computer and the related equipment are Type A and B interfaces as specified in 5.2.1 and 5.2.2. The computer I/O channels are separated into functional groups of four channels each. Each group of the four I/O channels may use either Type A or Type B interface.

50.3.1.2 Channel configuration. Communication with the computer will be carried on in a parallel mode of up to a 30-bit data word. The number of computer I/O channels may equal 4, 8, 12, or 16. Each group of four I/O channels is assembled on a CP-642A chassis or a CP-642B chassis. The CP-642A and CP-642B chassis may be implemented with either the Type A or B interface as specified in 50.3.1.1. The CP-642A chassis may only interface with peripheral equipment, and CP-642B chassis may interface with peripheral equipment or other computers.

a. Each group of four I/O channels shall operate independently of the other I/O channels.
b. Each of the four I/O channels in an I/O group shall have the same data transfer rate (Type A interface or Type B interface).

50.3.2 Control signals.

50.3.2.1 Computer-peripheral communications. The control lines used by the computer to communicate with the peripheral equipment are specified in 5.1.1.2.

50.3.2.2 IC communication. The control lines used by the computer to communicate with another computer are specified in 5.1.3.

50.3.3 Data transfer rates. The maximum data transfer rate for a single computer input or output channel is as follows:

Type A (Slow interface) - 40 KHz
Type B (Fast interface) - 125 KHz

The data transfer rate for a given system configuration is determined by additional factors such as computer internal priorities and the response time of the interconnecting equipment.

50.4 Special requirements for CP-789.

50.4.1 Functional requirements.

50.4.1.1 Interface type. The interface types used by the computer and related equipment shall be Type

A and B interfaces as specified in 5.2.1 and 5.2.2, respectively.

50.4.1.2 Channel configuration. Communication with the computer is carried on in a parallel mode of up to an 18- or 36-bit data word. The number of the I/O channels used by the computer is four or eight. The computer has four modes of operation.

a. Single-channel.
b. Dual-channel.
c. Intercomputer (IC).
d. Externally specified index (ESI).

These modes of operation are controlled by switches in the front panel at the computer.

50.4.1.3 Single-channel mode. In the single-channel mode, the transfer of information to and from the computer is 18 bits parallel.

50.4.1.4 Dual-channel mode. In the dual-channel mode, the transfer of information to and from the computer is 36 bits parallel. Two sequential even and odd numbered I/O channels are combined for dual-channel operation. Data transfer is by 36 parallel lines contained in one cable. The 36-data-bit input and output cables shall be connected to the odd channel of the channel pair. Control on dual-channel is maintained by the odd channel control lines. No external I/O cables can be connected to the even channel while in the dual channel mode.

50.4.1.5 IC mode. In the IC mode, the transfer of information between computers is 18 bits (single-channel) or it is 36 bits if the computer is in the dual-channel or ESI mode.

50.4.1.6 ESI mode. In the ESI mode, the transfer of information to and from the computer is 36 bits parallel. When transferring information into the computer, 18 bits are data and 18 bits are an address that indirectly specifies where to store the data. When transferring information out of the computer, the receiving equipment sends an 18-bit address that indirectly specifies from where to remove the data, and the computer sends 18 bits of data. Selecting the ESI mode automatically forces the computer in the dual-channel mode for that adjacent pair of even-odd channels.

50.4.2 Control signals.

50.4.2.1 Computer-peripheral communication. The control lines used by the computer to communicate with a peripheral equipment are specified in 5.1.1.2. The computer does not utilize the EIE line during interrupt communication.

50.4.2.2 IC communication. The control lines used by the computer to communicate with another computer are specified in 5.1.2.

50.4.3 Data transfer rates. The maximum data transfer rate for a single computer input or output channel is as follows:

	Single (18-bit mode)	Dual (36-bit mode)
Type A (Slow interface)	41.6 KHz	35.7 KHz
Type B (Fast interface)	50 KHz	41.6 KHz

In the event a high speed peripheral is used with the computer, care shall be exercised so data will not be lost. For example, if the transfer rate of the peripheral were one data word every 48 µs, and the computer program were to execute a multiply or divide instruction, a word may be lost because a multiply or divide instruction can require up to 48 µs. The data transfer rate for a given system configuration is determined by additional factors such as computer internal priorities and the response time of the interconnecting equipment.

TYPE E ADDITIONAL FEATURES

10. SCOPE

10.1 Scope. This appendix contains operational characteristics and design guidance for Type E interface, system integrity features (SIFs) which allow computer systems to detect errors and failures, and burst transfer mode which is a means of increasing throughput on a Type E interface. Additionally, this appendix contains conformance tests for Type E. This appendix forms a mandatory part of this standard.

20. REFERENCED DOCUMENTS

Not applicable

30. DEFINITIONS

Not applicable

40. GENERAL REQUIREMENTS

40.1 Throughput improvement. Improvement in throughput can be achieved as specified in 40.1.1 through 40.1.5. The throughput of both the SWT and burst transfer is shown on figure 66. This is the theoretical maximum throughput achievable, including the effects of both the addition of a parity bit to the IF and the delays caused by cable lengths.

40.1.1 Minimum throughput for SWT. For SWT, the protocol has been defined by Type E along with a data rate of 10 million bits per second (Mb/s). The first protocol is for that sink that requires time to internally transfer the received IW before accepting the next IW. This protocol is as follows:

Source (SOS) —> sink "Are you ready for data or CIW?"
Source <— (SIS) sink "I am ready for data or CIW or both."
Source (IF) —> sink "Here is the data."

If this sequence is followed for each CIW or data word to be transferred, the throughput for the unidirectional channel, based on a 32-bit word (no parity), can be defined as follows:

Sequence		Time (based on 10 Mb/s)
Source (SOS) ---> sink		0.4 µs
Source minimum delay		0.5 µs
Source <— (SIS) sink		0.4 µs
Source minimum delay		0.5 µs
Source (IF) —>sink		3.4 µs
Sink minimum delay		0.5 µs
Source <— (SIS) sink		0.4 µs
Source minimum delay		0.5 µs
Total time	=	6.6 µs

40.1.2 Additional factors affecting throughput. The throughput for this sequence would be 1000/6.6 or 151.52 thousand words per second (Kw/s). The LLSIO normal protocol requires a control word to be transferred between data words. The time required for this control frame to propagate in the cable (66 percent of the speed of light in a vacuum) causes a delay between word transfers, thus longer cables result in lower throughput. The maximum cable length specified for the Type E interface is 300 meters using TRF-8 triaxial cable. For one way transmission on this cable, this would result in an additional delay of 1.507 µs for each SOS control frame, SIS control frame, or IF transmission. If an additional 3 µs per sink or source transmission is added for the two way cable delay over a 300-meter cable, then throughput is reduced to about 79.3 Kw/s. For applications currently using parallel interfaces with throughput of 170 Kw/s, this would not be an attractive implementation. A better implementation would be to provide buffering within the sink so it could be immediately ready to accept another IF.

40.1.3 Optimum throughput for SWT. If the sink is able to accept another IW after receiving an IW, the protocol would be as follows:

Source (SOS) --> sink "Are your ready for data or CIW?"
Source <-- (SIS) sink "I am ready for data or CIW."
Source (IF) --> sink "Here is the data."
Source <-- (SIS) sink "I am ready for data or CIW."
Source (IF) --> sink "Here is the data."

\- - The above sequence is repeated until all
\- - data or CIW have been transferred.

Source <-- (SIS) sink "I am ready for data or CIW."

If this sequence is followed, the throughput for the unidirectional channel, with and without the implementation of parity, can be defined as follows:

Sequence	Time (no parity)	Time (parity)
Source (SOS) --> sink	0.4 µs	0.4 µs
Sink minimum delay	0.5 µs	0.5 µs
Source <-- (SIS) sink	0.4 µs	0.4 µs
Source minimum delay	0.5 µs	0.5 µs
Source (IF) --> sink	3.4 µs	3.5 µs
Sink minimum delay	0.5 µs	0.5 µs
Source <-- (SIS) sink	0.4 µs	0.4 µs
Source minimum delay	0.5 µs	0.5 µs
Source (IF) --> sink	3.4 µs	3.5 µs
\- -	Repeated until n words have been transferred.	
Sink minimum delay	0.5 µs	0.5 µs
Source <-- (SIS) sink	0.4 µs	0.4 µs
Total time =	0.4 + n(4.8)	0.4 + n(4.9)
Throughput =	$\frac{1}{\text{total time}}$	Where n = the number of words transferred.

The throughput in Kw/s for various numbers of words transferred is:

Words	Total time (no parity)	Throughput (no parity)	Total Time (parity)	Throughput (parity)
5	24.4 µs	204.90 Kw/s	24.9 µs	200.80 Kw/s
10	48.4 µs	206.61 Kw/s	49.4 µs	202.43 Kw/s
25	120.4 µs	207.64 Kw/s	122.9 µs	203.42 Kw/s
50	240.4 µs	207.99 Kw/s	245.4 µs	203.75 Kw/s

40.1.4 Cable delay. The throughput shown for the sequence above does not take into consideration the additional degradation resulting from cable delay. This delay is shown in the following:

Sequence(300 meter cable)	Time (no parity)	Time (parity)
Source (SOS) —> sink	0.4 µs	0.4 µs
Cable delay —> sink	1.507 µs	1.507 µs
Sink minimum delay	0.5 µs	0.5 µs
Source <— (SIS) sink	0.4 µs	0.4 µs
Source <— cable delay	1.507 µs	1.507 µs
Source minimum delay	0.5 µs	0.5 µs
Source (IF) —> sink	3.4 µs	3.5 µs
Cable delay —> sink	1.507 µs	1.507 µs
Sink minimum delay	0.5 µs	0.5 µs
Source <— (SIS) sink	0.4 µs	0.4 µs
Source <— cable delay	1.507 µs	1.507 µs
Source minimum delay	0.5 µs	0.5 µs
Source (IF) —> sink	3.4 µs	3.5 µs
Cable delay —> sink	1.507 µs	1.507 µs
- -	Repeated until n words have been transferred.	
- -		
- -		
Sink minimum delay	0.5 µs	0.5 µs
Source <— (SIS) sink	0.4 µs	0.4 µs
Source <— cable delay	1.507 µs	1.507 µs
Total time =	1.907 + n(7.814)	1.907 + n(7.914)

$$\text{Throughput (300 meters)} = \frac{1}{\text{total time (300 meters)}}$$

Where n = the number of words transferred.

The throughput in Kw/s for various numbers of words transferred is:

Words	Total time (no parity)	Throughput (no parity)	Total Time (parity)	Throughput (parity)
5	40.98 µs	122.02 Kw/s	41.48 µs	120.54 Kw/s
10	80.05 µs	122.93 Kw/s	81.05 µs	123.38 Kw/s
25	197.26 µs	126.74 Kw/s	199.76 µs	125.16 Kw/s
50	392.61 µs	127.35 Kw/s	397.61 µs	125.75 Kw/s

The graph, shown on figure 66, ranks channels in order of their maximum throughput rates. This graph shows the dependency of maximum channel throughput as a function of cable length. The hash marks serve as a reminder that a maximum throughput is specified for the channel and that actual equipment implementations may be below the specified value. The numbers shown above show that the throughput can be improved by increasing the number of words transmitted, thus reducing the overhead for each transmission. The optimum implementation, burst transfer, can increase the number of words transmitted for each IF without violating the timing requirements of the Type E interface.

40.1.5 Burst transfer. The throughput shown in the SWT mode of transmission is dependent upon the overhead delay of SIS control frame responses from sink for each IF and the cable delay. However, this is not the maximum throughput that can be achieved with this channel. The optimum throughput can be achieved by transferring more words without requiring control frames for handshaking. Type E does not provide for an upper limit on the size of the IF. A lower limit of six bits is provided to allow the sink to detect whether the incoming data is either an SOS control frame or an IF. If the source has the capability of appending more words within a single IF, then the throughput on the channel could be increased without changing the protocol. These factors are the basis for the following definition of burst transfer.

40.1.5.1 Burst transfer requirements. A new mode of operation for both sources and sinks using this approach has been implemented. This approach is called burst transfer and provides for the transfer of up to 32 data words within one IF. A burst transfer of 32 data words within an IF was chosen as the minimum number of words that would provide efficiency of transmission. The following requirements are used for this implementation:

a. Only multiple data words shall be allowed within an IF. Multiple CIWs shall not be permitted because present equipment is set up to process one command at a time. The receipt of multiple commands within one IF cannot be accommodated at this time.

b. A minimum of one to a maximum of 32 data words shall be included within an IF. Gaps between data words within an IF shall not be permitted. If the source is not able to append another data word to the IF, the source shall consider the IF completed. After receipt of the next SIS control frame indicating that the sink is ready for data, the source shall transmit a new IF starting with the next data word. The sink shall detect the end of the IF by the cessation of data bits being received. The use of a fixed number of words to be transferred within one IF would be counterproductive to the intent of improving throughput. While the amount of computer circuitry would be reduced for both transmission and reception using a fixed number of words with an IF, this would reduce the improvement of throughput for applications with varying sizes of data buffers to be transmitted. This approach to data transmission requires the sink to be able to accept the maximum number of data words in the IF. The source would not be obligated to transmit the maximum number of data words within each IF. The source would begin the IF with the S bit followed by the WI bit. After these two bits, the first data word would be transmitted. As additional data words were available to the source, they would be concatenated to the IF. If a data word was not available or the maximum number of data words had been included within the IF, the source would conclude the transmission. The sink would detect the end of the IF by the cessation of bits being transmitted from the source and respond with a SIS control frame as appropriate.

c. Any channel capable of burst transfer will also be capable of single word transmission. This will allow equipment with MIL-STD-1397 Type E channels (but without burst transfer capability) to communicate with equipment having both.

40.1.5.2 Burst transfer protocol. The protocol for this mode of transmission would be the same as that used for any data word or CIW transmission as shown below:

Source (SOS) --> sink	"Are your ready for data?"
Source <-- (SIS) sink	"I am ready for data."
Source (IF) --> sink	"Here is the data."
Source <-- (SIS) sink	"I am ready for data."
Source (IF) --> sink	"Here is the data."
- -	
- -	The above sequence is repeated until all data has been transferred.
- -	
Source <-- (SIS) sink	

40.1.5.3 Burst transfer timing. The timing for data word transmission with parity not being implemented and with a parity bit is:

Sequence	Time (no parity)	Time (parity)
Source (SOS) ---> sink	0.4 µs	0.4 µs
Sink minimum delay	0.5 µs	0.5 µs
Source <--- (SIS) sink	0.4 µs	0.4 µs
Source minimum delay	0.5 µs	0.5 µs
Source (IF) ---> sink	102.6 µs	105.8 µs
Sink minimum delay	0.5 µs	0.5 µs
Source <--- (SIS) sink	0.4 µs	0.4 µs
Source minimum delay	0.5 µs	0.5 µs
Source (IF) ---> sink	102.6 µs	105.8 µs
- -	Repeated until n words have been transferred.	
Sink minimum delay	0.5 µs	0.5 µs
Source <--- (SIS) sink	0.4 µs	0.4 µs
Total time =	0.4 + n(104)	0.4 + n(107.2)
Throughput =	$\frac{1}{\text{total time}}$	Where n = the number of groups of 32 words transferred.

The throughput in Kw/s for various numbers of words transferred is:

Words	Total time (no parity)	Throughput (no parity)	Total Time (parity)	Throughput (parity)
32	104.4 µs	306.50 Kw/s	107.6 µs	297.40 Kw/s
64	208.4 µs	307.10 Kw/s	214.8 µs	297.95 Kw/s
96	312.4 µs	307.30 Kw/s	322.0 µs	298.14 Kw/s

40.1.5.4 Cable delay. When the cable delay is taken into consideration, the timing is as follows:

Sequence (300 meter cable)	Time (no parity)	Time (parity)
Source (SOS) ---> sink	0.4 µs	0.4 µs
Cable delay ---> sink	1.507 µs	1.507 µs
Sink minimum delay	0.5 µs	0.5 µs
Source <--- (SIS) sink	0.4 µs	0.4 µs
Source <--- cable delay	1.507 µs	1.507 µs
Source minimum delay	0.5 µs	0.5 µs
Source (IF) ---> sink	102.6 µs	105.8 µs
Cable delay ---> sink	1.507 µs	1.507 µs
Sink minimum delay	0.5 µs	0.5 µs
Source <--- (SIS) sink	0.4 µs	0.4 µs
Source <--- cable delay	1.507 µs	1.507 µs
Source minimum delay	0.5 µs	0.5 µs
Source (IF) ---> sink	102.6 µs	105.8 µs
Cable delay ---> sink	1.507 µs	1.507 µs
- -	Repeated until n words have been transferred.	
Sink minimum delay	0.5 µs	0.5 µs
Source <--- (SIS) sink	0.4 µs	0.4 µs
Source <--- cable delay	1.507 µs	1.507 µs
Total time =	1.907 + n(107.014)	1.907 + n(110.214)
Throughput (300 meters) =	$\frac{1}{\text{total time (300 meters)}}$	Where n = the number of words transferred.

The throughput for various numbers of words transferred is:

Words	Total time (no parity)	Throughput (no parity)	Total Time (parity)	Throughput (parity)
32	109.02 µs	293.52 Kw/s	112.21 µs	285.18 Kw/s
64	216.14 µs	296.11 Kw/s	222.54 µs	287.60 Kw/s
96	323.25 µs	296.98 Kw/s	332.25 µs	288.94 Kw/s

The curve for the Type E interface versus cable length is shown on figure 66. This curve shows that burst transfer provides both the highest throughput for the interface and least dependence upon cable length. All applications of the Type E interface may not require the throughput available using burst transfer, but any design that would be concerned with throughput should include it as part of the design consideration.

40.2 System integrity features. The Type E interface is concerned only with the electrical or physical characteristics of the interface. The protocol, signal levels, timing, cables, and connector are specified within these documents. What has not been addressed is system considerations in the area of error detection. It has been recognized that the use of triaxial cable for point-to-point application of this interface would greatly reduce the error probability during data transmission. However, the use of this interface is not limited only to point-to-point connections. Where equipment with a single port is used, some form of digital switching may be used with this interface to improve the reconfiguration capability of the system. In addition, if this interface is used as part of a bus interconnection system, system recovery techniques may require the knowledge of the point of either data corruption or loss. Such information cannot be retrieved without the application of error detection techniques to the interface. Systems currently implemented with parallel interfaces depend upon system software to detect loss of communication. The Type E "ping-pong" method of communication allows hardware within the interfaces to detect loss of communication, to perform system notification, and to initiate orderly reconfiguration procedures.

40.2.1 Error detection. The types of errors that need to be detected are those that would cause system problems because of data contamination or would prevent system communication between elements of the system. These errors are outlined in 40.2.1.1 through 40.2.1.4.

40.2.1.1 Data errors. The type of noise environment encountered with this interface is not completely known at this time. The use of triaxial cable should reduce the incidence of induced errors, but since each equipment may have a different physical implementation of the interface, errors caused by internal noise or grounding problems may arise. If the time period of the interference is only sufficient to disrupt a single bit on the data transmission, the use of parity may be sufficient for this detection. If the time period of the noise is sufficient to disrupt more than one bit, then the detection of other types of degradation of the serial bit stream would be required. The use of Manchester coding for data transmission requires precise detection of the zero crossing points for data recovery. If the noise is of sufficient duration or amplitude to generate additional zero crossing points or to mask out the correct zero crossing, the sink would detect too many or not enough bits in the IF. Without this ability of detection, corrupted data may enter the system.

40.2.1.2 Communication loss. Present equipment using parallel interface protocols only have the capability of detecting loss of communication between system computers. Loss of communication between other elements of the system shall be handled by software. For equipment with large numbers of channels, this software overhead shall be accommodated within the constraints of system timing. With the defined protocol of Type E, this system overhead can be removed from the software and transferred to the logic within the Type E interface. Three types of communication loss can be detected by the Type E interface.

40.2.1.2.1 No SIS control frame response from sink. The first loss would be in the case where a source has either a CIW or a data word ready for transmission. Each time the source has transmitted a SOS control frame on the channel, there has been no SIS control frame response from the sink. The source has repeated the SOS control frame transmission on the channel and is continuing to receive nothing from the sink.

40.2.1.2.1.1 Source timeout period. The value of the source timeout period shall be specified by the individual application. It is recommended that the source timer timeout period be similar to that used for intercomputer timeouts as defined for parallel channels. Forced EF (CIW) commands may or may not be timed by the source timeout timer (refer to the individual equipment specification).

40.2.1.2.2 SIS control frame not ready response from sink. The second loss would be in the case where the source has either a CIW or a data word ready for transmission, but the responding SIS control frame from the sink indicates that the sink is not ready for either data or CIWs. This type of failure could occur where the Type E interface has been mechanized using logic within the interface to control the "ping-pong" action. Thus, if the equipment is not functioning or is stopped, the Type E interface would continue to pass control frames on the channel.

40.2.1.2.3 No SOS control frame or IF from source. The third loss would be in the case of sink being ready to receive either CIW or data words. If an SOS control frame was received from the source, the sink should respond with a SIS control frame. However, because of either equipment or cable failure the sink has not received an SOS control frame. The implementation chosen requires that the sink shall receive an SOS control frame within 1 ms after the sink has transmitted its SIS control frame. This allows error detection circuitry within the sink to detect this type of failure.

40.2.1.2.3.1 Sink timeout timer. Implementing the ability to enable and disable sink timeout is recommended for both user and application flexibility.

40.2.1.3 False signals because of cable reflections. Present parallel data communication between elements in a system use unidirectional communication. Signals are transmitted in one direction only on a cable. Thus "handshaking" response signals are required to be transmitted by the receiving device to the sending device on a separate cable in that direction. If either cable is opened because of either reconfiguration or battle damage, communication has been cut, but erroneous signals cannot be produced by the transmitting or receiving device. Using the protocol defined in STANAG 4153, data communication is unidirectional on a cable, but handshaking signals are transmitted in both directions on the single cable. If the cable is properly terminated at both ends, there is no problem of errors caused by reflected signals. But in the case where the cable has been opened because of either system reconfiguration or battle damage, the SOS control frame transmission by the source would be reflected from the open cable. Since both the SOS control frame and the SIS control frame use a four-bit code, an SOS control frame sent with bits set for both CIW and data words available would be reflected as an SIS control frame with bits signifying that the sink is ready for either CIW or data words. The source, having received this false SIS control frame, would then transmit an IF. Depending upon the length of the IF and the location of the discontinuity, it would be possible for the IF to be reflected by and received by the source as an additional SIS control frame response from the sink. This can be seen from the following example:

> The source is connected to a sink over a 300-meter cable. A break in the cable occurs at the connection to the sink. The source transmits an SOS control frame down the cable. If the SOS control frame transmission is at maximum amplitude and the cable losses do not attenuate this amplitude below the minimum required for detection, then the SOS control frame would be reflected from the open end of the cable and received by the source as an SIS control frame at 3.01 µs after transmission. The source does not respond to signals until 500 ns after transmission. Since this false SIS control frame would come after this time, the source would recognize the SIS control frame and would respond to it. If the false SIS control frame indicated that the sink was ready for data, the source would transmit an IF. This IF would also be reflected from the open cable. The characteristics of this reflected waveform would depend upon the size of the IF along with distortions caused by interaction between the transmitted and reflected waveforms. After transmission of the SOS control frame, the source would begin looking for an SIS control frame response. If the bits reflected from the IF could be recognized by the source as an SIS control frame response, it could assume that the IF has been received by the sink. This would be an erroneous data communication. If the reflected bits are distorted to the point where the source cannot determine that it is an SIS control frame, it is important that the source recognize that there is a problem on the interface and data communications are not proceeding properly.

40.2.1.4 Illegal conditions. The ability to implement forced commands requires that the sink be able to determine that the received IF is in accordance with its defined operating state. If the sink was allowed to accept forced CIWs within the IF, then the arrival of such an IF when the last SIS control frame sent from the sink indicated that the sink was not ready for CIWs would be permitted. However, if such an event occurred with the arrival of a data word within the IF, this would be indication of a problem within the channel. A set of error possibilities could exist. The source may have malfunctioned, the source may not have interpreted the last received SIS control frame correctly, or the sink may not have recognized the correct WI bit of the received IF. Whatever the cause of the problem, there would be a chance for incorrect system operation unless the system detects and corrects for this failure condition.

50 DETAILED REQUIREMENTS.

50.1 Conformance tests.

50.1.1 Return loss conformance test. Conformance with the Type E interface impedance return loss profile of figure 34 is demonstrated by performing the following test. The test shall be performed on every Type E interface source and sink interface in the equipment under test.

a. Connect a 50 ohm signal divider network (HP 35676A Reflection/Transmission Test Kit or equivalent) or an S-Parameter Test Set (HP 35677A or equivalent) to the output, reference, and input ports of a network analyzer (HP 3577A/B or equivalent).
b. Configure the network analyzer for a log frequency sweep from 1 MHz to 100 MHz, a sweep time of 2 seconds, a bandwidth of 1 KHz, and a signal amplitude of ± 200 mV open-circuit or ± 100 mV terminated (50 ohms) at the output of the signal divider or S-Parameter Test Set. The display should be configured for linear magnitude at a scale of 5 dB per vertical division.
c. Connect a short (approximately 5 feet or 1.5 meters) 50 ohm coaxial test cable to the output port of the signal divider network or Port 1 of the S-Parameter Test Set using an N-to-BNC adapter connector. Attach a BNC-to-triaxial adapter connector to the far end of the cable.
d. With the coaxial test cable and all adapter connectors in place, perform a one-port reflection calibration in accordance with the instructions provided with the specific network analyzer being used. This will typically involve calibration with the test cable open-circuited and then terminated with a precision 50 ohm load.
e. Connect the far end of the test cable to the interface connector of the Type E device under test. Observe the resulting return loss profile displayed by the network analyzer and compare with the acceptable return loss profile of figure 34. Perform this step with the device power on and off.

A final determination on the acceptability of Type E interface equipment impedance shall be achieved by evaluating the return loss test results together with those obtained from the reflection test, refer to 50.1.2. Conformance with the return loss specification from 1 MHz to 60 MHz is mandatory. Return loss values in this range that exceed those specified in figure 34 indicate potential problems in the equipment design which shall be corrected by the equipment vendor. The reflection test in 5.4.5.2.5 shall be the final measure of acceptable performance.

50.1.2 Reflection conformance test. With the transmitter not transmitting and with DC power on or off, a 4 bit input Manchester II waveform (conforming to a 1101 bit pattern) at a clock rate of 10 MHz and repetition rate of 100 KHz, with a peak amplitude of 750 mV and rise/fall time of 6.5 to 7.0 ns (10 to 90%) shall be applied to the interface connector through a 36 meter length of MIL-C-17/135 (TFR-8) 50 ohm cable. The amplitude of the reflected voltage, measured 200 ns after the last valid transition of the last bit, shall not exceed ± 250 mV. (See figure 67)

50.1.3 Composite system channel noise test. Conformance to the composite system channel noise requirement is demonstrated by performing the following test:

a. Connect the source and the sink interfaces together (end-around) through a 60 meter length of MIL-C-17/135 (TFR-8) 50 ohm cable.
b. Control frames shall be exchanged between the source and the sink.
c. The reflected voltage shall be measured at the transmitting connector interface.
d. The following transmitted control frames shall be tested:

(1) Source control frames of 1000 and 1010, and
(2) Sink control frames of 1011 and 1001.

The amplitude of the composite noise, existing more than 400 ns after the zero voltage crossing in the middle of the last bit, shall not exceed 200 mV peak-to-peak (see figure 68). This test limit is intentionally set below the maximum possible composite noise of 254 mV peak-to-peak for a 60 meter cable to screen out equipment which exhibits marginal performance with respect to more than one electrical parameter.

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Type K COMMAND SET

10. SCOPE

10.1 Scope. This appendix provides the Type K command set requirements. Some of the commands have been modified. These modifications include: changing a SCSI-II command from optional to mandatory; or, imposing restriction(s) on particular command(s). New commands for unique security and data integrity, which are not found in the SCSI-II, shall be optional. This appendix forms a mandatory part of this standard.

Guidance for selecting optional commands is also given. Optional commands are grouped into the following functional areas: Data Integrity; Backup and Archive; Performance; Security; and Maintenance. An explanation of the individual functional areas is given along with each optional command within the functional area.

20. REFERENCED DOCUMENTS

Not applicable.

30. DEFINITIONS

30.1 Acronyms. Acronyms used exclusively in this appendix are defined as follows:

ASC	Additional Sense Code
ECC	Error Correction Code
DFLT	Default
DLIST	Data defect List
DPM	Data Protect Mode
GLIST	Grown defect List
HSEC	Hard Sector
LUN	Logical Unit Number
PF	Page Format
PS	Parameters Savable
RMB	Removable Medium
SSEC	Soft Sector
SURF	Surface
TD	Table Data
TL	Table Length
TOC	Table of Contents

40. GENERAL REQUIREMENTS

40.1 Type K command set. The following sections identify all mandatory commands for a Type K device. Some mandatory Type K commands originate from optional commands in SCSI-II. Commands specified shall adhere to the restrictions identified herein. Unless otherwise specified, items defined in SCSI-II as being optional shall remain optional. Unless otherwise specified, all mandatory SCSI-II items shall remain mandatory. All optional commands within the SCSI-II are included following the mandatory commands.

40.1.1 Direct-access devices. Commands identified in 40.1.1.1 shall be implemented as defined. Included in the list are changes to commands which are mandatory in SCSI-II which have additional restrictions on the implementation of the command within this standard.

40.1.1.1 Mandatory commands for direct-access devices.

40.1.1.1.1 Format Unit (04h). This command shall be mandatory, refer to 8.2.1 of SCSI-II.

40.1.1.1.1.1 Command restrictions. The following Format Unit Defect Descriptor format and requirements table XVII shall replace table 112 in SCSI-II. Table XVIII replaces table 163 in SCSI-II.

TABLE XVII. Format Unit Defect Descriptor format and requirements.

FmtData	CmpLst	Defect List Format	Defect List Length	Command Type	Comments
0	0	000b	N/A	Mandatory	Target-defined use of defect source
BLOCK FORMAT:					
1	0	000b	Zero	Mandatory	1/ 3/ 5/
1	1	000b	Zero	Mandatory	1/ 4/ 5/
1	0	000b	>0	Optional	2/ 3/
1	1	000b	>0	Optional	2/ 4/
BYTES FROM INDEX FORMAT:					
1	0	100b	Zero	Mandatory	1/ 3/ 5/
1	1	100b	Zero	Mandatory	1/ 4/ 5/
1	0	100b	>0	Optional	2/ 3/
1	1	100b	>0	Optional	2/ 4/
PHYSICAL SECTOR FORMAT:					
1	0	101b	Zero	Mandatory	1/ 3/
1	1	101b	Zero	Mandatory	1/ 4/
1	0	101b	>0	Optional	2/ 3/
1	1	101b	>0	Optional	2/ 4/
1	0	110b	Vendor-Specific		
1	1	110b	Vendor-Specific		

1/ No Dlist is transferred to the target during the DATA OUT phase.
2/ A Dlist is transferred to the target during the DATA OUT phase. Add the Dlist defects to the new Glist.
3/ Use the existing Glist as a defect source. Add existing Glist defects to the new Glist.
4/ Discard the existing Glist. Do not add existing Glist defects to the new Glist.
5/ Type K definitions not defined as mandatory in SCSI-II.

TABLE XVIII. Format Device Page.

	BIT							
BYTE	7	6	5	4	3	2	1	0
0	PS	PAGE CODE (03h)						
1	PAGE LENGTH (Bytes)-(16h)							
2	(MSB)	TRACKS PER ZONE						
3	TRACKS PER ZONE							(LSB)
4	(MSB)	ALTERNATE SECTORS PER ZONE						
5	ALTERNATE SECTORS PER ZONE							(LSB)
6	(MSB)	ALTERNATE TRACKS PER ZONE						
7	ALTERNATE TRACKS PER ZONE							(LSB)
8	(MSB)	ALTERNATE TRACKS PER VOLUME						
9	ALTERNATE TRACKS PER VOLUME							(LSB)
10	(MSB)	SECTORS PER TRACK						
11	SECTORS PER TRACK							(LSB)
12	(MSB)	DATA BYTES PER PHYSICAL SECTOR						
13	DATA BYTES PER PHYSICAL SECTOR							(LSB)
14	(MSB)	INTERLEAVE						
15	INTERLEAVE							(LSB)
16	(MSB)	TRACK SKEW FACTOR						
17	TRACK SKEW FACTOR							(LSB)
18	(MSB)	CYLINDER SKEW FACTOR						
19	CYLINDER SKEW FACTOR							(LSB)
20	SSEC	HSEC	RMB	SURF	RESERVED			DPM1/
21	RESERVED							
22	RESERVED							
23	RESERVED							

1/ DPM (Data Protect Mode) Type K definition not defined in SCSI-II.

40.1.1.1.2 Inquiry (12h). This command shall be mandatory, refer to 7.2.5 of SCSI-II.

40.1.1.1.3 Mode Select(6) (15h). This command shall be mandatory, refer to 7.2.8 of SCSI-II.

40.1.1.1.3.1 Command restrictions. Implementors of the data protection scheme option, defined in 40.4.1, shall provide a software changeable control bit (Byte 20, Bit 0) in the Format Device Page titled "Data Protect Mode (DPM)". This bit, when enabled, shall be used to signal the device to build and maintain a read/write lock table to support the 40.1.1.2.25 Set Locks and 40.1.1.2.15 Read Lock Table commands. This bit requires the device to reject normal read/write commands and only allow 40.1.1.2.17 Read With Locks and 40.1.1.2.33 Write With Locks commands to transfer data to/from the media.

40.1.1.1.4 Mode Sense(6) (1Ah). This command shall be mandatory, refer to 7.2.10 of SCSI-II.

40.1.1.1.4.1 Command restrictions. Implementors of the Type K data protection scheme option shall provide the current setting of the "Data Protect Mode (DPM)" control bit in the Format Device Page.

40.1.1.1.5 Read(6) (08h). This command shall be mandatory, refer to 8.2.5 of SCSI-II.

40.1.1.1.6 Read(10) (28h). This command shall be mandatory, refer to 8.2.6 of SCSI-II.

40.1.1.1.7 Read Capacity (25h). This command shall be mandatory, refer to 8.2.7 of SCSI-II.

40.1.1.1.8 Receive Diagnostic Results (1Ch). This command shall be mandatory. Refer to 7.2.13 of SCSI-II.

40.1.1.1.9 Release (17h) . This command shall be mandatory, refer to 8.2.11 of SCSI-II.

40.1.1.1.10 Request Sense (03h). This command shall be mandatory, refer to 7.2.14 of SCSI-II.

40.1.1.1.10.1 Command restrictions. Implementors of the data protection scheme option, defined in 40.4.1, shall provide sense data indicating errors in this area as follows:

a. Errors detected during the processing of the 40.1.1.2.17 Read With Locks or 40.1.1.2.33 Write With Locks commands because of violations of the data protection scheme shall:

   (1) Cause a CHECK CONDITION status,
   (2) Return a sense key of 07h (DATA PROTECT) to be returned in the REQUEST SENSE data packet,
   (3) Return an additional sense code (ASC) of BBh (PROTECTION VIOLATION).

b. Overlapping definitions, detected during the processing of the 40.1.1.2.25 Set Locks command, within lock table partitions and the partitions lock is changing from a valid non-zero lock code to zero shall:

   (1) Cause a CHECK CONDITION status,
   (2) Return a sense key of 07h (DATA PROTECT) to be returned in the REQUEST SENSE data packet,
   (3) Return an additional sense code (ASC) of BCh (LOCK TABLE REDEFINED).

40.1.1.1.11 Reserve (16h). This command shall be mandatory, refer to 8.2.12 of SCSI-II.

40.1.1.1.12 Rezero Unit (01h). This command shall be mandatory, refer to 8.2.13 of SCSI-II.

40.1.1.1.13 Send Diagnostic (1Dh). This command shall be mandatory, refer to 7.2.15 of SCSI-II.

40.1.1.1.13.1 Command restrictions. Diagnostic pages and page structures shall be device specific. Each device subjected to diagnostics shall implement a page defining the tests to be run and a page format delineating how the test results will be displayed.

The SEND DIAGNOSTIC command with a page format (PF) bit of one instructs the target to execute zero or more diagnostic pages and that the data returned shall use the diagnostic page format described by SCSI-II for the applicable device. Each diagnostic page shall define a function or operation that the target performs during the test execution. A PF bit of zero shall indicate that the SEND DIAGNOSTIC parameters are as specified in the SCSI-I standard.

40.1.1.1.14 Test Unit Ready (00h). This command shall be mandatory, refer to 7.2.16 of SCSI-II.

40.1.1.1.15 Write(6) (0Ah). This command shall be mandatory, refer to 8.2.20 of SCSI-II.

40.1.1.1.16 Write(10) (2Ah). This command shall be mandatory, refer to 8.2.21 of SCSI-II.

40.1.1.2 Optional Commands for Direct-Access Devices.

40.1.1.2.1 Change Definition (40h). This command shall be optional, refer to 7.2.1 of SCSI-II.

40.1.1.2.2 Compare (39h). This command shall be optional, refer to 7.2.2 of SCSI-II.

40.1.1.2.2.1 Command restrictions. The Parameter List Length of this command shall be 14h. The Copy Function Code supported for this command shall be code 02h (Block Device to Block Device). There shall be a maximum of one Segment Descriptor.

40.1.1.2.3 Copy (18h). This command shall be optional, refer to 7.2.3 of SCSI-II.

40.1.1.2.3.1 Command restrictions. The Parameter List Length of this command shall be 14h. 'Flag' and 'Link' bits shall be supported in full. The Copy Function Code supported for this command shall be code 02h (Block Device to Block Device). There shall be a maximum of one Segment Descriptor.

40.1.1.2.4 Copy and Verify (3Ah). This command shall be optional, refer to 7.2.4 of SCSI-II.

40.1.1.2.4.1 Command restrictions. The Parameter List Length of this command shall be 14h. The Copy Function Code supported for this command shall be code 02h (Block Device to Block Device). There shall be a maximum of one Segment Descriptor.

40.1.1.2.5 Data Destruct command (0Ch). This command shall be optional. This command which is not found in SCSI-II shall be defined by table XIX and table XX.

TABLE XIX. Data Destruct command.

	BIT							
BYTE	7	6	5	4	3	2	1	0
0	Operation Code For Data Destruct Command (0Ch)							
1	Logical Unit Num			DFLT	Reserved			
2	(MSB)	Parameter List Length						
3	Parameter List Length							(LSB)
4	Applicable LUN							
5	Reserved							

The Data Destruct command performs data erasure on the medium. If this command completes successfully (no check condition), the disk subsystem will have performed the command without error. If an error condition is detected while writing to the medium, the Check Condition Status will reflect that a "Multiple Medium Error" has been detected and the Request Sense command shall provide specific error information.

The Data Destruct Command shall override any reservations currently established by the disk subsystem for the unit(s) specified (this command does temporary release). If any of the LUNs are reserved by another host adapter, the command shall be aborted with a "Reservation Conflict" status. In this case, the "Reservation Conflict" status implies "Check Condition". Before the disk subsystem initiates the "Data Destruct" on the LUNs, the LUNs are reserved to the initiator. Upon the completion of the "Data Destruct" all reservations that were in effect prior to the "Data Destruct" remain in effect. Furthermore, any LUNs that were specified by the "Data Destruct" that were not previously reserved shall be reserved to the initiator issuing the "Data Destruct". The "Data Destruct" command causes the selected LUNs to transition with "Unit Attention" status.

The number of available LUNs is configuration specific. The LUN field is only applicable to commands that do not have default bit (DFLT) set in the command. If the default bit (DFLT) is set, the LUN field is ignored and all LUNs selected by a one in the bit significant Applicable LUN field shall be targeted for the Data Destruct. An Applicable LUN byte of 55h shall select units 0, 2, 4, and 6 for the Data Destruct.

If the Parameter List Length is zero, the default data patterns FFFFh, 0000h, FFFFh, and 4141h are written to every data block on the selected LUNs during successive passes. If the field is non-zero, it shall be an even value and shall specify the number of bytes in the data patterns included in the Data Pattern parameter (see table D-2). For example, the default patterns could also be specified by setting the Parameter List Length to 8 and specifying the data patterns of FFFFh, 0000h, FFFFh, and 4141h in the parameter. The 16 bit data pattern shall be replicated throughout the data blocks written to the unit. The maximum parameter list length shall be 256 (128 patterns).

TABLE XX. Data Destruct Patterns.

	BIT							
BYTE	7	6	5	4	3	2	1	0
0	(MSB)	Data Pattern						
1	Data Pattern							(LSB)
. . .	. . .							
n-2	(MSB)	Data Pattern						
n-1	Data Pattern							(LSB)

40.1.1.2.6 Lock-Unlock Cache (36h). This command shall be optional, refer to 8.2.2 of SCSI-II.

40.1.1.2.7 Log Select (4Ch). This command shall be optional, refer to 7.2.6 of SCSI-II.

40.1.1.2.8 Log Sense (4Dh). This command shall be optional, refer to 7.2.7 of SCSI-II.

40.1.1.2.9 Mode Select(10) (55h). This command shall be optional, refer to 7.2.9 of SCSI-II.

40.1.1.2.9.1 Command restrictions. If implemented this command shall have the same restrictions as Mode Select (15h) as called out in 40.1.1.1.3.

40.1.1.2.10 Mode Sense(10) (5Ah). This command shall be optional, refer to 7.2.11 of SCSI-II.

40.1.1.2.10.1 Command restrictions. If implemented this command shall have the same restrictions as Mode Sense (1Ah) as called out in 40.1.1.1.4.

40.1.1.2.11 Pre-Fetch (34h). This command shall be optional, refer to 8.2.3 of SCSI-II.

40.1.1.2.12 Prevent-Allow Medium Removal (1Eh). This command shall be optional. Refer to 8.2.4 of SCSI-II.

40.1.1.2.13 Read Buffer (3Ch). This command shall be optional, refer to 7.2.12 of SCSI-II.

40.1.1.2.13.1 Command restrictions. The Read Buffer Modes 'DATA' (010b) and 'DESCRIPTOR' (011b) shall be supported in full.

40.1.1.2.14 Read Defect Data (37h). This command shall be optional, refer to 8.2.8 of SCSI-II.

40.1.1.2.14.1 Command restrictions. The Defect List Format field shall be defined as indicated by table XVII as found under the Format Unit command.

40.1.1.2.15 Read Lock Table (06h). This command shall be optional. This command which is not found in SCSI-II shall be defined in Table XXI.

TABLE XXI. Read Lock Table command.

	BIT							
BYTE	7	6	5	4	3	2	1	0
0	Operation Code (06h)							
1	Logical Unit Num			Reserved				TL/TD
2	Reserved							
3	Reserved							
4	Reserved							
5	Control Field							

The Read Lock Table command (table XXI) shall request the target to return the Read Lock Table information identified by the TL/TD control bit as specified in table XXII.

TABLE XXII. Read Lock Table TL/TD control bit definition.

TL/TD	DEFINITION
0	The target shall return two bytes of data that indicate the table length (TL) of parameters contained in the Read/Write Lock Table. The value returned shall equal one when the request for table length is issued after formatting, with the "Data Protect Mode (DPM)" bit set in the Mode Select-Format Device Page, and no Set Locks commands have been received by the target. The format of the data returned during the request for lock table length (TL) shall be defined in table XXIII.
1	The target shall return ten bytes of table data (TD) for every table parameter indicated in the request for table length response data. This implies that the target shall return eighty bytes of table data when the table length returned equals eight. The format of the data returned during the request for lock table data (TD) shall be defined in table XXIV.

TABLE XXIII. Read Lock Table Length format.

	BIT							
BYTE	7	6	5	4	3	2	1	0
0	(MSB)	Table Length						
1	Table Length							(LSB)

TABLE XXIV. Read Lock Table data format.

	BIT							
BYTE	7	6	5	4	3	2	1	0
0	(MSB)	Starting Logical Block Address						
1	Starting Logical Block Address							
2	Starting Logical Block Address							
3	Starting Logical Block Address							(LSB)
4	(MSB)	Ending Logical Block Address						
5	Ending Logical Block Address							
6	Ending Logical Block Address							
7	Ending Logical Block Address							(LSB)
8	Read Lock							
9	Write Lock							
.	.							
.	.							
.	.							
(TL-1)x10	(MSB)	Starting Logical Block Address						
(TL-1)x10+1	Starting Logical Block Address							
(TL-1)x10+2	Starting Logical Block Address							
(TL-1)x10+3	Starting Logical Block Address							(LSB)
(TL-1)x10+4	(MSB)	Ending Logical Block Address						
(TL-1)x10+5	Ending Logical Block Address							
(TL-1)x10+6	Ending Logical Block Address							
(TL-1)x10+7	Ending Logical Block Address							(LSB)
(TL-1)x10+8	Read Lock							
(TL-1)x10+9	Write Lock							

40.1.1.2.16 Read Long (3Eh). This command shall be optional, refer to 8.2.9 of SCSI-II.

40.1.1.2..16.1 Command restrictions. The host shall be capable of suppressing ECC correction by setting 'CORRECT' bit to zero.

40.1.1.2.17 Read With Locks (BBh). This command shall be optional. This command which is not found in SCSI-II shall be defined in table XXV.

TABLE XXV. Read with Locks command.

	BIT							
BYTE	7	6	5	4	3	2	1	0
0	Operation Code (BBh)							
1	Logical Unit Num			Reserved				
2	(MSB)	Logical Block Address						
3	Logical Block Address							
4	Logical Block Address							
5	Logical Block Address							(LSB)
6	Reserved							
7	(MSB)	Transfer Length						
8	Transfer Length							(LSB)
9	Read Key							
10	Reserved							
11	Control Field							

The Read With Locks command (table XXV) requests that the target transfer data to the initiator provided the read key matches the read lock, within the Read/Write Lock Table, for all logical blocks requested. Upon compare of the read key and read lock the most recent data value written in the addressed logical block(s) shall be returned.

The logical lock address field specifies the logical block at which the read operation shall begin.

The transfer length field shall specify the number of contiguous logical blocks of data to be transferred. A transfer length of zero indicates that 65536 logical blocks shall be transferred. Any other value shall indicate the number of logical blocks to be transferred.

The read key field shall specify the key code to be applied to the compare process with the read lock contained in the Read/Write Lock Table. When the read lock is zero for all logical blocks in the range of logical blocks requested, no compare shall be required and the value of this field shall not be interpreted. Otherwise, the read key field value shall equal the read lock for the read to be approved and the requested data transferred to the initiator.

40.1.1.2.18 Reassign Blocks (07h). This command shall be optional, refer to 8.2.10 of SCSI-II.

40.1.1.2.19 Search Data Equal (31h). This command shall be optional, refer to 8.2.14.1 of SCSI-II.

40.1.1.2.20 Search Data High (30h). This command shall be optional, refer to 8.2.14.2 of SCSI-II.

40.1.1.2.21 Search Data Equal (32h). This command shall be optional, refer to 8.2.14.3 of SCSI-II.

40.1.1.2.22 Seek(6) (0Bh). This command shall be optional, refer to 8.2.15 of SCSI-II.

40.1.1.2.23 Seek(10) (2Bh). This command shall be optional, refer to 8.2.15 of SCSI-II.

40.1.1.2.24 Set Limits (33h). This command shall be optional, refer to 8.2.16 of SCSI-II.

40.1.1.2.25 Set Locks (BDh). This command shall be optional. This command which is not found in SCSI-II shall be defined in table XXVI.

TABLE XXVI. Set Locks command.

	BIT							
BYTE	7	6	5	4	3	2	1	0
0	Operation Code (BDh)							
1	Logical Unit Num			Reserved				
2	(MSB)	Logical Block Address						
3	Logical Block Address							
4	Logical Block Address							
5	Logical Block Address							(LSB)
6	Reserved							
7	(MSB)	Number of Blocks						
8	Number of Blocks							(LSB)
9	Read Lock							
10	Write Lock							
11	Control Field							

The Set Locks command (table XXVI) shall provide the information to build the device read/write lock table used to provide data protection of the device media. Targets implementing the Set Locks command shall also implement the Read With Locks command, Write With Locks command, Read Lock Table command, and the "Data Protect Mode (DPM)" bit option within the Mode Select-Format Device Page.

At the completion of drive formatting, with the "Data Protect Mode (DPM)" bit set in the Format Device Page, a lock table establishing all device logical blocks as being not protected (all read and write locks are set to zero) shall be built. If the Read Lock Table command is sent to a target at this time, the target shall return ten (10) bytes of data as defined in the Read Lock Table command description.

For each Set Locks command received the target shall create a lock table partition of ten (10) bytes reflecting the parameters within the command. Upon receipt of the Set Locks command, the target shall interrogate all previous lock table partitions for overlapping definitions and return a Target Check condition with status "Lock Table Redefined" indicating so when detected. Changing the lock of a partitions from zero to a valid non-zero lock code shall not cause a "Lock Table Redefined" interrupt. However, changing the lock of a partition from a previously defined non-zero value to zero shall cause the Lock Table Redefined interrupt. A device shall be capable of supporting a lock table with a minimum of 1024 partitions.

The logical block address field shall contain the starting logical block of the lock table partition.

The number of blocks field shall contain the range of logical blocks, beginning from the starting logical block that the read and write lock codes applies. A number of blocks value of zero shall indicate a range of 65536 logical blocks.

The read lock field shall contain the read lock for the partition of logical blocks defined within the command. The read lock shall be defined in table XXVII.

The write lock field shall contain the write lock for the partition of logical locks defined within the command. The write lock shall be defined in table XXVII.

The Set Locks command for a band of protected logical blocks shall be rejected when any existing write lock within the band is set to 255. In this case the device shall communicate a "Check Condition" status and sense data indicating a "Protection Violation" error.

A write lock of 255 shall only be removed by executing the Format command with the "Data Protect Mode (DPM)" bit set in the Mode Select-Format Device Page, or, by executing the Data Destruct command.

TABLE XXVII. Read/Write Lock code definitions.

Read or Write Lock	Read With Locks Command Received	Write With Locks Command Received
Zero	No lock/key compare performed. Reading permitted.	No lock/key compare performed. Writing permitted.
001 - 254	Lock/key compare required before reading permitted.	Lock/key compare required before writing permitted.
255	Lock/key compare required before reading permitted.	Write command rejected.

40.1.1.2.26 Start Stop Unit (1Bh). This command shall be optional, refer to 8.2.17 of SCSI-II.

40.1.1.2.27 Synchronize Cache (35h). This command shall be optional, refer to 8.2.18 of SCSI-II.

40.1.1.2.28 Verify (2Fh). This command shall be optional, refer to 8.2.19 of SCSI-II.

40.1.1.2.28.1 Command restrictions. The 'BytChk' bit shall be supported in full for both the values of zero and one. The 'RelAdr' bit shall be supported in full for both the values of zero and one. 'Flag' and 'Link' shall be supported in full.

40.1.1.2.29 Write and Verify (2Eh). This command shall be optional, refer to 8.2.22 of SCSI-II.

40.1.1.2.29.1 Command restrictions. The 'BytChk' bit shall be supported in full for both the values of zero and one. The 'RelAdr' bit shall be supported in full for both the values of zero and one. 'Flag' and 'Link' shall be supported in full.

40.1.1.2.30 Write Buffer (3Bh). This command shall be optional, refer to 7.2.17 of SCSI-II.

40.1.1.2.30.1 Command restrictions. Write buffer mode 'WRITE DATA' (010b) shall be supported as specified in SCSI-II. The download modes shall be optional on a per application basis. The download mode shall also support a download and save option which may alter device media or other nonvolatile memory.

40.1.1.2.31 Write Long (3Fh). This command shall be optional, refer to 8.2.23 of SCSI-II.

40.1.1.2.32 Write Same (35h). This command shall be optional, refer to 8.2.24 of SCSI-II.

40.1.1.2.33 Write With Locks (BCh). This command shall be optional. This command which is not found in SCSI-II shall be defined in table XXXVIII.

TABLE XXVIII. Write with Locks command.

	BIT							
BYTE	7	6	5	4	3	2	1	0
0	Operation Code (BCh)							
1	Logical Unit Num			Reserved				
2	(MSB)	Logical Block Address						
3	Logical Block Address							
4	Logical Block Address							
5	Logical Block Address							(LSB)
6	Reserved							
7	(MSB)	Transfer Length						
8	Transfer Length							(LSB)
9	Reserved							
10	Write Key							
11	Control Field							

The Write With Locks command (table XXVIII) shall request that the target write the data transferred by the initiator to the medium provided the write key matches the write lock, within the Read/Write Lock Table, for all logical blocks requested.

The logical block address field shall specify the logical block at which the write operation begins.

The transfer length field shall specify the number of continuous logical blocks of data being transferred. A transfer length of zero shall indicate that 65536 logical blocks to be transferred. Any other value shall indicate the number of logical blocks to be transferred.

The write key field shall specify the key code to be applied to the compare process with the write lock contained in the Read/Write Lock Table. When the write lock is zero for the range of logical blocks requested, no compare shall be required and the field value shall not be interpreted. Otherwise, the write key field value shall equal the write lock for the write to be approved and the transferred data to be written.

40.1.2 Sequential-access devices. Commands identified in 40.1.2.1 shall be implemented as defined. Included in the following list are mandatory SCSI-II commands which Type K requires additionally implementation restrictions.

40.1.2.1 Mandatory commands for sequential-access devices.

40.1.2.1.1 Erase (19h). This command shall be mandatory, refer to 9.2.1 of SCSI-II.

40.1.2.1.2 Inquiry (12h). This command shall be mandatory, refer to 7.2.5 of SCSI-II.

40.1.2.1..3 Mode Select(6) (15h). This command shall be mandatory, refer to 7.2.8 of SCSI-II.

40.1.2.1..4 Mode Sense(6) (1Ah). This command shall be mandatory, refer to 7.2.10 of SCSI-II.

40.1.2.1..5 Read(6) (08h). This command shall be mandatory, refer to 9.2.4 of SCSI-II.

40.1.2.1.6 Read Block Limits (05h). This command shall be mandatory, refer to 9.2.5 of SCSI-II.

40.1.2.1.7 Receive Diagnostic Results (1Ch). This command shall be mandatory. Refer to 7.2.13 of SCSI-II.

40.1.2.1.8 Release Units (17h). This command shall be mandatory, refer to 9.2.9 of SCSI-II.

40.1.2.1.9 Request Sense (03h). This command shall be mandatory, refer to 7.2.14 of SCSI-II.

40.1.2.1.10 Reserve Unit (16h). This command shall be mandatory, refer to 9.2.10 of SCSI-II.

40.1.2.1.11 Rewind (01h). This command shall be mandatory, refer to 9.2.11 of SCSI-II.

40.1.2.1.12 Send Diagnostic (1Dh). This command shall be mandatory, refer to 7.2.15 of SCSI-II.

40.1.2.1.12.1 Command restrictions. The self-test feature shall be the only mandatory implementation of this command. All targets shall support the page format (PF) bit equal to both zero and one. When PF is equal to one the diagnostic page format (see table 77 in SCSI-II) shall be supported.

40.1.2.1.13 Space (11h). This command shall be mandatory, refer to 9.2.12 of SCSI-II.

40.1.2.1.14 Test Unit Ready (00h). This command shall be mandatory, refer to 7.2.16 of SCSI-II.

40.1.2.1.15 Write (0Ah). This command shall be mandatory, refer to 9.2.14 of SCSI-II.

40.1.2.1.16 Write Filemarks (10h). This command shall be mandatory, refer to 9.2.15 of SCSI-II.

40.1.2.2 Optional Commands for Sequential-Access Devices.

40.1.2.2.1 Change Definition (40h). This command shall be optional, refer to 7.2.1 of SCSI-II.

40.1.2.2.2 Compare (39h). This command shall be optional, refer to 7.2.2 of SCSI-II.

40.1.2.2.3 Copy (18h). This command shall be optional, refer to 7.2.3 of SCSI-II.

40.1.2.2.4 Copy and Verify (3Ah). This command shall be optional, refer to 7.2.4 of SCSI-II.

40.1.2.2.5 Load Unload (1Bh). This command shall be optional, refer to 9.2.2 of SCSI-II.

40.1.2.2.6 Locate (2Bh). This command shall be optional, refer to 9.2.3 of SCSI-II.

40.1.2.2.7 Log Select (4Ch). This command shall be optional, refer to 7.2.6 of SCSI-II.

40.1.2.2.8 Log Sense (4Dh). This command shall be optional, refer to 7.2.7 of SCSI-II.

40.1.2.2.9 Mode Select(10) (55h). This command shall be optional, refer to 7.2.9 of SCSI-II.

40.1.2.2.9.1 Command restrictions. If implemented this command shall have the same restrictions as Mode Select (15h) as called out in 40.1.1.1.3.

40.1.2.2.10 Mode Sense(10) (5Ah). This command shall be optional, refer to 7.2.11 of SCSI-II.

40.1.2.2.10.1 Command restrictions. If implemented this command shall have the same restrictions as Mode Sense (1Ah) as called out in 40.1.1.1.4.

40.1.2.2.11 Prevent-Allow Medium Removal (1Eh). This command shall be optional. Refer to 8.2.4 of SCSI-II.

40.1.2.2.12 Read Buffer (3Ch). This command shall be optional, refer to 7.2.12 of SCSI-II.

40.1.2.2.12.1 Command restrictions. The Read Buffer Modes 'DATA' (010b) and 'DESCRIPTOR' (011b) shall be supported in full.

40.1.2.2.13 Read Position (34h). This command shall be optional, refer to 9.2.6 of SCSI-II.

40.1.2.2.14 Read Reverse (0Fh). This command shall be optional, refer to 9.2.7 of SCSI-II.

40.1.2.2.15 Recover Buffered Data (14h). This command shall be optional, refer to 9.2.8 of SCSI-II.

40.1.2.2.16 Verify (13h). This command shall be optional, refer to 9.2.13 of SCSI-II.

40.1.2.2.17 Write Buffer (3Bh). This command shall be optional, refer to 7.2.17 of SCSI-II.

40.1.3 Printer devices. The commands required for printer devices shall be the same as those specified as mandatory for both printer devices and all device types in SCSI-II. No further restrictions shall be imposed.

40.1.4 Processor devices. The commands required for processor devices shall be the same as those as specified as mandatory for both processor devices and all device types in SCSI-II. No further restrictions shall be imposed.

40.1.5 Write-once devices. Commands identified in 40.1.5.1 shall be implemented as defined. Included in the following list are mandatory SCSI-II commands which Type K requires additionally implementation restrictions.

40.1.5.1 Mandatory commands for write-once devices.

40.1.5.1.1 Inquiry (12h). This command shall be mandatory, refer to 7.2.5 of SCSI-II.

40.1.5.1.2 Mode Select(6) (15h). This command shall be mandatory, refer to 7.2.8 of SCSI-II.

40.1.5.1.3 Mode Sense(6) (1Ah). This command shall be mandatory, refer to 7.2.10 of SCSI-II.

40.1.5.1.4 Read(10) (28h). This command shall be mandatory, refer to 8.2.6 of SCSI-II.

40.1.5.1.5 Read Capacity (25h). This command shall be mandatory, refer to 8.2.7 of SCSI-II.

40.1.5.1.6 Receive Diagnostic Results (1Ch). This command shall be mandatory. Refer to 7.2.13 of SCSI-II.

40.1.5.1.7 Release (17h). This command shall be mandatory, refer to 8.2.11 of SCSI-II.

40.1.5.1.8 Request Sense (03h). This command shall be mandatory, refer to 7.2.14 of SCSI-II.

40.1.5.1.9 Reserve (16h). This command shall be mandatory, refer to 8.2.12 of SCSI-II.

40.1.5.1.10 Rezero Unit (01h). This command shall be mandatory, refer to 8.2.13 of SCSI-II.

40.1.5.1.11 Send Diagnostic (1Dh). This command shall be mandatory, refer to 7.2.15 of SCSI-II.

40.1.5.1.11.1 Command restrictions. Diagnostic pages and page structures shall be device specific. Each device requiring diagnostics shall have a page defining the tests to be run and a page format delineating how the test results will be displayed.

The SEND DIAGNOSTIC command with a page format (PF) bit of one instructs the target to execute zero or more diagnostic pages and that the data returned shall use the diagnostic page format described by SCSI-II for the applicable device. Each diagnostic page shall define a function or operation that the target performs during the test execution. A PF bit of zero shall indicate that the SEND DIAGNOSTIC parameters are as specified in the SCSI-I standard.

40.1.5.1.12 Test Unit Ready (00h). This command shall be mandatory, refer to 7.2.16 of SCSI-II.

40.1.5.1.13 Write(10) (2Ah). This command shall be mandatory, refer to 8.2.21 of SCSI-II.

40.1.5.2 Optional Commands for Write-Once Devices.

40.1.5.2.1 Change Definition (40h). This command shall be optional, refer to 7.2.1 of SCSI-II.

40.1.5.2.2 Compare (39h). This command shall be optional, refer to 7.2.2 of SCSI-II.

40.1.5.2.2.1 Command restrictions. The Parameter List Length of this command shall be 14h. The Copy Function Code supported for this command shall be code 02h (Block Device to Block Device). There shall be a maximum of one Segment Descriptor.

40.1.5.2.3 Copy (18h). This command shall be optional, refer to 7.2.3 of SCSI-II.

40.1.5.2.3.1 Command restrictions. The Parameter List Length of this command shall be 14h. 'Flag' and 'Link' bits shall be supported in full. The Copy Function Code supported for this command shall be code 02h (Block Device to Block Device). There shall be a maximum of one Segment Descriptor.

40.1.5.2.4 Copy and Verify (3Ah). This command shall be optional, refer to 7.2.4 of SCSI-II.

40.1.5.2.4.1 Command restrictions. The Parameter List Length of this command shall be 14h. The Copy Function Code supported for this command shall be code 02h (Block Device to Block Device). There shall be a maximum of one Segment Descriptor.

40.1.5.2.5 Lock-Unlock Cache (36h). This command shall be optional, refer to 8.2.2 of SCSI-II.

40.1.5.2.6 Log Select (4Ch). This command shall be optional, refer to 7.2.6 of SCSI-II.

40.1.5.2.7 Log Sense (4Dh). This command shall be optional, refer to 7.2.7 of SCSI-II.

40.1.5.2.8 Medium Scan (38h). This command shall be optional, refer to 15.2.3 of SCSI-II.

40.1.5.2.9 Mode Select(10) (55h). This command shall be optional, refer to 7.2.9 of SCSI-II.

40.1.5.2.9.1 Command restrictions. If implemented this command shall have the same restrictions as Mode Select (15h) as called out in 40.1.1.1.3.

40.1.5.2.10 Mode Sense(10) (5Ah). This command shall be optional, refer to 7.2.11 of SCSI-II.

40.1.5.2.10.1 Command restrictions. If implemented this command shall have the same restrictions as Mode Sense (1Ah) as called out in 40.1.1.1.4.

40.1.5.2.11 Pre-Fetch (34h). This command shall be optional, refer to 8.2.3 of SCSI-II.

40.1.5.2.12 Prevent-Allow Medium Removal (1Eh). This command shall be optional, refer to 8.2.4 of SCSI-II.

40.1.5.2.13 Read(6) (08h). This command shall be optional, refer to 8.2.5 of SCSI-II.

40.1.5.2.14 Read(12) (A8h). This command shall be optional, refer to 15.2.4 of SCSI-II.

40.1.5.2.15 Read Buffer (3Ch). This command shall be optional, refer to 7.2.12 of SCSI-II.

40.1.5.2.15.1 Command restrictions. The Read Buffer Modes 'DATA' (010b) and 'DESCRIPTOR' (011b) shall be supported in full.

40.1.5.2.16 Read Long (3Eh). This command shall be optional, refer to 8.2.9 of SCSI-II.

40.1.5.2.16.1 Command restrictions. The host shall be capable of suppressing ECC correction by setting 'CORRECT' bit to zero.

40.1.5.2.17 Read With Locks (BBh). This command shall be optional, refer to 40.1.1.2.16.

40.1.5.2.18 Reassign Blocks (07h). This command shall be optional, refer to 8.2.10 of SCSI-II.

40.1.5.2.19 Read Lock Table (06h). This command shall be optional, refer to 40.1.1.2.18.

40.1.5.2.20 Search DataEqual(10)(31h). This command shall be optional, refer to 8.2.14.1 of SCSI-II.

40.1.5.2.21 Search Data Equal(12) (B1h). This command shall be optional, refer to 15.2.8 of SCSI-II.

40.1.5.2.22 Search Data High(10)(30h). This command shall be optional, refer to 8.2.14.2 of SCSI-II.

40.1.5.2.23 Search Data High(12)(B0h). This command shall be optional, refer to 15.2.8 of SCSI-II.

40.1.5.2.24 Search DataEqual(10)(32h). This command shall be optional, refer to 8.2.14.3 of SCSI-II.

40.1.5.2.25 Search Data Equal(12)(B2h). This command shall be optional, refer to 15.2.8 of SCSI-II.

40.1.5.2.26 Seek(6) (0Bh). This command shall be optional, refer to 8.2.15 of SCSI-II.

40.1.5.2.27 Seek(10) (2Bh). This command shall be optional, refer to 8.2.15 of SCSI-II.

40.1.5.2.28 Set Limits(10) (33h). This command shall be optional, refer to 8.2.16 of SCSI-II.

40.1.5.2.29 Set Limits(12) (B3h). This command shall be optional, refer to 15.2.9 of SCSI-II.

40.1.5.2.30 Set Locks (BDh). This command shall be optional, refer to 40.1.1.2.25.

40.1.5.2.31 Start Stop Unit (1Bh). This command shall be optional, refer to 8.2.17 of SCSI-II.

40.1.5.2.32 Synchronize Cache (35h). This command shall be optional, refer to 8.2.18 of SCSI-II.

40.1.5.2.33 Verify(10) (2Fh). This command shall be optional, refer to 15.2.11 of SCSI-II.

40.1.5.2.33.1 Command restrictions. The 'BytChk' bit shall be supported in full for both the values of zero and one. The 'RelAdr' bit shall be supported in full for both the values of zero and one. 'Flag' and 'Link' shall be supported in full.

40.1.5.2.34 Verify(12) (AFh). This command shall be optional, refer to 15.2.12 of SCSI-II.

40.1.5.2.34.1 Command restrictions. The 'BytChk' bit shall be supported in full for both the values of zero and one. The 'RelAdr' bit shall be supported in full for both the values of zero and one. 'Flag' and 'Link' shall be supported in full.

40.1.5.2.35 Write(6) (0Ah). This command shall be optional, refer to 8.2.20 of SCSI-II.

40.1.5.2.36 Write(12) (AAh). This command shall be optional, refer to 15.2.14 of SCSI-II.

40.1.5.2.37 Write and Verify (10) (2Eh). This command shall be optional, refer to 15.2.15 of SCSI-II.

40.1.5.2.37.1 Command restrictions. The 'BytChk' bit shall be supported in full for both the values of zero and one. The 'RelAdr' bit shall be supported in full for both the values of zero and one. 'Flag' and 'Link' shall be supported in full.

40.1.5.2.38 Write and Verify(12) (AEh). This command shall be optional, refer to 15.2.16 of SCSI-II.

40.1.5.2.38.1 Command restrictions. The 'BytChk' bit shall be supported in full for both the values of zero and one. The 'RelAdr' bit shall be supported in full for both the values of zero and one. 'Flag' and 'Link' shall be supported in full.

40.1.5.2.39 Write Buffer (3Bh). This command shall be optional, refer to 7.2.17 of SCSI-II.

40.1.5.2.39.1 Command restrictions. Write buffer mode 'WRITE DATA' (010b) shall be supported as specified in SCSI-II. The download modes shall be optional on a per application basis. The download mode shall also support a download and save option which may alter device media or other nonvolatile memory.

40.1.5.2.40 Write Long (3Fh). This command shall be optional, refer to 8.2.23 of SCSI-II.

40.1.5.2.41 Write With Locks (BCh). This command shall be optional, refer to 40.1.1.2.33.

40.1.6 CD-ROM devices. The commands required for CD-ROM devices are those as specified as mandatory for both CD-ROM devices and all device types in SCSI-II along with the optional commands which follow. Included in the following list are mandatory SCSI-II commands which Type K requires additionally implementation restrictions.

40.1.6.1 Mandatory commands for CD-ROM devices.

40.1.6.1.1 Inquiry (12h). This command shall be mandatory, refer to 7.2.5 of SCSI-II.

40.1.6.1.2 Mode Select(6) (15h). This command shall be mandatory, refer to 7.2.8 of SCSI-II.

40.1.6.1.3 Mode Sense(6) (1Ah). This command shall be mandatory, refer to 7.2.10 of SCSI-II.

40.1.6.1.4 Read(10) (28h). This command shall be mandatory, refer to 8.2.6 of SCSI-II.

40.1.6.1.5 Read CD-ROM Capacity (25h). This command shall be mandatory. Refer to 13.2.8 of SCSI-II.

40.1.6.1.6 Receive Diagnostic Results (1Ch). This command shall be mandatory. Refer to 7.2.13 of SCSI-II.

40.1.6.1.6.1 Command restrictions. All targets shall support the page format (PF) bit equal to both zero and one. When PF bit is equal to one, the diagnostic page format (table 7-47 in SCSI-II) shall be supported.

40.1.6.1.7 Release (17h). This command shall be mandatory, refer to 8.2.11 of SCSI-II.

40.1.6.1.8 Request Sense (03h). This command shall be mandatory, refer to 7.2.14 of SCSI-II.

40.1.6.1.9 Reserve (16h). This command shall be mandatory, refer to 8.2.12 of SCSI-II.

40.1.6.1.10 Rezero Unit (01h). This command shall be mandatory, refer to 8.2.13 of SCSI-II.

40.1.6.1.11 Send Diagnostic (1Dh). This command shall be mandatory, refer to 7.2.15 of SCSI-II.

40.1.6.1.11.1 Command restrictions. Diagnostic pages and page structures shall be device specific. Each device requiring diagnostics shall have a page defining the tests to be run and a page format delineating how the test results will be displayed.

The SEND DIAGNOSTIC command with a page format (PF) bit of one instructs the target to execute zero or more diagnostic pages and that the data returned shall use the diagnostic page format described by SCSI-II for the applicable device. Each diagnostic page shall define a function or operation that the target performs during the test execution. A PF bit of zero shall indicate that the SEND DIAGNOSTIC parameters are as specified in the SCSI-I standard.

40.1.6.1. Test Unit Ready (00h). This command shall be mandatory, refer to 7.2.16 of SCSI-II.

40.1.6.2 Optional commands for CD-ROM devices.

40.1.6.2.1 Change Definition (40h). This command shall be optional, refer to 7.2.1 of SCSI-II.

40.1.6.2.2 Compare (39h). This command shall be optional, refer to 7.2.2 of SCSI-II.

40.1.6.2.2.1 Command restrictions. The Parameter List Length of this command shall be 14h. The Copy Function Code supported for this command shall be code 02h (Block Device to Block Device). There shall be a maximum of one Segment Descriptor.

40.1.6.2.3 Copy (18h). This command shall be optional, refer to 7.2.3 of SCSI-II.

40.1.6.2.3.1 Command restrictions. The Parameter List Length of this command shall be 14h. 'Flag' and 'Link' bits shall be supported in full. The Copy Function Code supported for this command shall be code 02h (Block Device to Block Device). There shall be a maximum of one Segment Descriptor.

40.1.6.2.4 Copy and Verify (3Ah). This command shall be optional, refer to 7.2.4 of SCSI-II.

40.1.6.2.4.1 Command restrictions. The Parameter List Length of this command shall be 14h. The Copy Function Code supported for this command shall be code 02h (Block Device to Block Device). There shall be a maximum of one Segment Descriptor.

40.1.6.2.5 Lock-Unlock Cache (36h). This command shall be optional, refer to 8.2.2 of SCSI-II.

40.1.6.2.6 Log Select (4Ch). This command shall be optional, refer to 7.2.6 of SCSI-II.

40.1.6.2.7 Log Sense (4Dh). This command shall be optional, refer to 7.2.7 of SCSI-II.

40.1.6.2.8 Mode Select(10) (55h). This command shall be optional, refer to 7.2.9 of SCSI-II.

40.1.6.2.8.1 Command restrictions. If implemented this command shall have the same restrictions as Mode Select (15h) as called out in 40.1.1.1.3.

40.1.6.2.9 Mode Sense(10) (5Ah). This command shall be optional, refer to 7.2.11 of SCSI-II.

40.1.6.2.9.1 Command restrictions. If implemented this command shall have the same restrictions as Mode Sense (1Ah) as called out in 40.1.1.1.4.

40.1.6.2.10 Pause/Resume (4Bh). This command shall be optional, refer to 13.2.1 of SCSI-II.

40.1.6.2.11 Play Audio(10) (45h). This command shall be optional, refer to 13.2.2 of SCSI-II.

40.1.6.2.12 Play Audio(12) (A5h). This command shall be optional, refer to 13.2.3 of SCSI-II.

40.1.6.2.13 Play Audio MSF (47h). This command shall be optional, refer to 13.2.4 of SCSI-II.

40.1.6.2.14 Play Audio Track/Index(48h). This command shall be optional, refer to 13.2.5 of SCSI-II.

40.1.6.2.15 Play Track Relative(10)(49h). This command shall be optional, refer to 13.2.6 of SCSI-II.

40.1.6.2.16 Play Track Relative(12)(A9h). This command shall be optional, refer to 13.2.7 of SCSI-II.

40.1.6.2.17 Pre-Fetch (34h). This command shall be optional, refer to 8.2.3 of SCSI-II.

40.1.6.2.18 Prevent-Allow Medium Removal (1Eh). This command shall be optional. Refer to 8.2.4 of SCSI-II.

40.1.6.2.19 Read(6) (08h). This command shall be optional, refer to 8.2.5 of SCSI-II.

40.1.6.2.20 Read(12) (A8h). This command shall be optional, refer to 15.2.4 of SCSI-II.

40.1.6.2.21 Read Buffer (3Ch). This command shall be optional, refer to 7.2.12 of SCSI-II.

40.1.6.2.21.1 Command restrictions. The Read Buffer Modes 'DATA' (010b) and 'DESCRIPTOR' (011b) shall be supported in full.

40.1.6.2.22 Read Header (44h). This command shall be optional, refer to 13.2.9 of SCSI-II.

40.1.6.2.23 Read Long (3Eh). This command shall be optional, refer to 8.2.9 of SCSI-II.

40.1.6.2.23.1 Command restrictions. The host shall be capable of suppressing ECC correction by setting 'CORRECT' bit to zero.

40.1.6.2.24 Read Sub-Channel (42h). This command shall be optional, refer to 13.2.10 of SCSI-II.

40.1.6.2.25 Read TOC (43h). This command shall be optional, refer to 13.2.11 of SCSI-II.

40.1.6.2.26 Search Data Equal(10)(31h). This command shall be optional, refer to 8.2.14.1of SCSI-II.

40.1.6.2.27 Search Data Equal(12)(B1h). This command shall be optional, refer to 15.2.8 of SCSI-II.

40.1.6.2.28 Search Data High(10)(30h). This command shall be optional, refer to 8.2.14.2 of SCSI-II.

40.1.6.2.29 Search Data High(12)(B0h). This command shall be optional, refer to 15.2.8 of SCSI-II.

40.1.6.2.30 Search Data Equal(10)(32h). This command shall be optional, refer to 8.2.14.3 of SCSI-II.

40.1.6.2.31 Seek(6) (0Bh). This command shall be optional, refer to 8.2.15 of SCSI-II.

40.1.6.2.32 Seek(10) (2Bh). This command shall be optional, refer to 8.2.15 of SCSI-II.

40.1.6.2.33 Set Limits(10) (33h). This command shall be optional, refer to 8.2.16 of SCSI-II.

40.1.6.2.34 Set Limits(12) (B3h). This command shall be optional, refer to 15.2.9 of SCSI-II.

40.1.6.2.35 Start Stop Unit (1Bh). This command shall be optional, refer to 8.2.17 of SCSI-II.

40.1.6.2.36 Synchronize Cache (35h). This command shall be optional, refer to 8.2.18 of SCSI-II.

40.1.6.2.37 Verify(10) (2Fh). This command shall be optional, refer to 15.2.11 of SCSI-II.

40.1.6.2.37.1 Command restrictions. The 'BytChk' bit shall be supported in full for both the values of zero and one. The 'RelAdr' bit shall be supported in full for both the values of zero and one. 'Flag' and 'Link' shall be supported in full.

40.1.6.2.38 Verify(12) (AFh). This command shall be optional, refer to 15.2.12 of SCSI-II.

40.1.6.2.38.1 Command restrictions. The 'BytChk' bit shall be supported in full for both the values of zero and one. The 'RelAdr' bit shall be supported in full for both the values of zero and one. 'Flag' and 'Link' shall be supported in full.

40.1.6.2.39 Write Buffer (3Bh). This command shall be optional, refer to 7.2.17 of SCSI-II.

40.1.6.2.39.1 Command restrictions. Write buffer mode 'WRITE DATA' (010b) shall be supported as specified in SCSI-II. The download modes shall be optional on a per application basis. The download mode shall also support a download and save option which may alter device media or other nonvolatile memory.

40.1.7 Scanner devices. The commands required for scanner devices are those as specified as mandatory for both scanner devices and all device types in SCSI-II. No further restrictions shall be imposed.

40.1.8 Optical memory devices. The commands required for optical memory devices are those as specified as mandatory for both optical memory devices and all device types in SCSI-II along with the optional commands which follow. Included in the following list are mandatory SCSI-II commands which Type K requires additionally implementation restrictions.

40.1.8.1 Mandatory commands for optical memory devices.

40.1.8.1.1 Inquiry (12h). This command shall be mandatory, refer to 7.2.5 of SCSI-II.

40.1.8.1.2 Mode Select(6) (15h). This command shall be mandatory, refer to 7.2.8 of SCSI-II.

40.1.8.1.3 Mode Sense(6) (1Ah). This command shall be mandatory, refer to 7.2.10 of SCSI-II.

40.1.8.1.4 Read(10) (28h). This command shall be mandatory, refer to 8.2.6 of SCSI-II.

40.1.8.1.5 Read CD-ROM Capacity(25h). This command shall be mandatory, refer to 13.2.8of SCSI-II.

40.1.8.1.6 Receive Diagnostic Results (1Ch). This command shall be mandatory, refer to 7.2.13 of SCSI-II.

40.1.8.1.7 Release (17h). This command shall be mandatory, refer to 8.2.11 of SCSI-II.

40.1.8.1.8 Request Sense (03h). This command shall be mandatory, refer to 7.2.14 of SCSI-II.

40.1.8.1.9 Reserve (16h). This command shall be mandatory, refer to 8.2.12 of SCSI-II.

40.1.8.1.10 Rezero Unit (01h). This command shall be mandatory, refer to 8.2.13 of SCSI-II.

40.1.8.1.11 Send Diagnostic (1Dh). This command shall be mandatory, refer to 7.2.15 of SCSI-II.

40.1.8.1.11.1 Command restrictions. Diagnostic pages and page structures shall be device specific. Each device requiring diagnostics shall have a page defining the tests to be run and a page format delineating how the test results will be displayed.

The SEND DIAGNOSTIC command with a page format (PF) bit of one instructs the target to execute zero or more diagnostic pages and that the data returned shall use the diagnostic page format described by SCSI-II for the applicable device. Each diagnostic page shall define a function or operation that the target performs during the test execution. A PF bit of zero shall indicate that the SEND DIAGNOSTIC parameters are as specified in the SCSI-I standard.

40.1.8.1.12 Test Unit Ready (00h). This command shall be mandatory, refer to 7.2.16 of SCSI-II.

40.1.8.1.13 Write(10) (2Ah). This command shall be mandatory, refer to 8.2.21 of SCSI-II.

40.1.8.2 Optional commands for optical memory devices.

40.1.8.2.1 Change Definition (40h). This command shall be optional, refer to 7.2.1 of SCSI-II.

40.1.8.2.2 Compare (39h). This command shall be optional, refer to 7.2.2 of SCSI-II.

40.1.8.2.2.1 Command restrictions. The Parameter List Length of this command shall be 14h. The Copy Function Code supported for this command shall be code 02h (Block Device to Block Device). There shall be a maximum of one Segment Descriptor.

40.1.8.2.3 Copy (18h). This command shall be optional, refer to 7.2.3 of SCSI-II.

40.1.8.2.3.1 Command restrictions. The Parameter List Length of this command shall be 14h. 'Flag' and 'Link' bits shall be supported in full. The Copy Function Code supported for this command shall be code 02h (Block Device to Block Device). There shall be a maximum of one Segment Descriptor.

40.1.8.2.4 Copy and Verify (3Ah). This command shall be optional, refer to 7.2.4 of SCSI-II.

40.1.8.2.4.1 Command restrictions. The Parameter List Length of this command shall be 14h. The Copy Function Code supported for this command shall be code 02h (Block Device to Block Device). There shall be a maximum of one Segment Descriptor.

40.1.8.2.5 Data Destruct Command (0Ch). This command shall be optional, refer to 40.1.1.2.5.

40.1.8.2.6 Erase(10) (2Ch). This command shall be mandatory, refer to 15.2.1 of SCSI-II.

40.1.8.2.7 Erase(12) (2Ch). This command shall be mandatory, refer to 15.2.2 of SCSI-II.

40.1.8.2.8 Format Unit (04h). This command shall be mandatory, refer to 8.2.1 of SCSI-II.

40.1.8.2.9 Lock-Unlock Cache (36h). This command shall be optional, refer to 8.2.2 of SCSI-II.

40.1.8.2.10 Log Select (4Ch). This command shall be optional, refer to 7.2.6 of SCSI-II.

40.1.8.2.11 Log Sense (4Dh). This command shall be optional, refer to 7.2.7 of SCSI-II.

40.1.8.2.12 Medium Scan (38h). This command shall be optional, refer to 15.2.3 of SCSI-II.

40.1.8.2.13 Mode Select(10) (55h). This command shall be optional, refer to 7.2.9 of SCSI-II.

40.1.8.2.13.1 Command restrictions. If implemented this command shall have the same restrictions as Mode Select (15h) as called out in 40.1.1.1.3.

40.1.8.2.14 Mode Sense(10) (5Ah). This command shall be optional, refer to 7.2.11 of SCSI-II.

40.1.8.2.14.1 Command restrictions. If implemented this command shall have the same restrictions as Mode Sense (1Ah) as called out in 40.1.1.1.4.

40.1.8.2.15 Pre-Fetch (34h). This command shall be optional, refer to 8.2.3 of SCSI-II.

40.1.8.2.16 Prevent-Allow Medium Removal (1Eh). This command shall be optional, refer to 8.2.4 of SCSI-II.

40.1.8.2.17 Read(6) (08h). This command shall be optional, refer to 8.2.5 of SCSI-II.

40.1.8.2.18 Read(12) (A8h). This command shall be optional, refer to 15.2.4 of SCSI-II.

40.1.8.2.19 Read Buffer (3Ch). This command shall be optional, refer to 7.2.12 of SCSI-II.

40.1.8.2.19.1 Command restrictions. The Read Buffer Modes 'DATA' (010b) and 'DESCRIPTOR' (011b) shall be supported in full.

40.1.8.2.20 Read Defect Data(10) (37h). This command shall be optional, refer to 8.2.8 of SCSI-II.

40.1.8.2.21 Read Defect Data(12) (B7h). This command shall be optional, refer to 15.2.5 of SCSI-II.

40.1.8.2.21.1 Command restrictions. The Defect List Format field shall be defined by table XVII found under the Format Unit command.

40.1.8.2.22 Read Generation (29h). This command shall be optional, refer to 15.2.6 of SCSI-II.

40.1.8.2.23 Read Long (3Eh). This command shall be optional, refer to 8.2.9 of SCSI-II.

40.1.8.2.23.1 Command restrictions. The host shall be capable of suppressing ECC correction by setting 'CORRECT' bit to zero.

40.1.8.2.24 Read Updated Block (2Dh). This command shall be optional, refer to 15.2.7 of SCSI-II.

40.1.8.2.25 Read With Locks (BBh). This command shall be optional, refer to 40.1.1.2.16.

40.1.8.2.26 Reassign Blocks (07h). This command shall be optional, refer to 8.2.10 of SCSI-II.

40.1.8.2.27 Read Lock Table (06h). This command shall be optional, refer to 40.1.1.2.18.

40.1.8.2.28 Search Data Equal(10)(31h). This command shall be optional, refer to 8.2.14.1 of SCSI-II.

40.1.8.2.29 Search Data Equal(12)(B1h). This command shall be optional, refer to 15.2.8 of SCSI-II.

40.1.8.2.30 Search Data High(10)(30h). This command shall be optional, refer to 8.2.14.2 of SCSI-II.

40.1.8.2.31 Search Data High(12)(B0h). This command shall be optional, refer to 15.2.8 of SCSI-II.

40.1.8.2.32 Search Data Equal(10)(32h). This command shall be optional, refer to 8.2.14.3 of SCSI-II.

40.1.8.2.33 Search Data Equal(12)(B2h). This command shall be optional, refer to 15.2.8 of SCSI-II.

40.1.8.2.34 Seek(6) (0Bh). This command shall be optional, refer to 8.2.15 of SCSI-II.

40.1.8.2.35 Seek(10) (2Bh). This command shall be optional, refer to 8.2.15 of SCSI-II.

40.1.8.2.36 Set Limits(10) (33h). This command shall be optional, refer to 8.2.16 of SCSI-II.

40.1.8.2.37 Set Limits(12) (B3h). This command shall be optional, refer to 15.2.9 of SCSI-II.

40.1.8.2.38 Set Locks (BDh). This command shall be optional, refer to 40.1.1.2.25.

40.1.8.2.39 Start Stop Unit (1Bh). This command shall be optional, refer to 8.2.17 of SCSI-II.

40.1.8.2.40 Synchronize Cache (35h). This command shall be optional, refer to 8.2.18 of SCSI-II.

40.1.8.2.41 Update Block (3Dh). This command shall be optional, refer to 15.2.10 of SCSI-II.

40.1.8.2.42 Verify(10) (2Fh). This command shall be optional, refer to 15.2.11 of SCSI-II.

40.1.8.2.42.1 Command restrictions. The 'BytChk' bit shall be supported in full for both the values of zero and one. The 'RelAdr' bit shall be supported in full for both the values of zero and one. 'Flag' and 'Link' shall be supported in full.

40.1.8.2.43 Verify(12) (AFh). This command shall be optional, refer to 15.2.12 of SCSI-II.

40.1.8.2.43.1 Command restrictions. The 'BytChk' bit shall be supported in full for both the values of zero and one. The 'RelAdr' bit shall be supported in full for both the values of zero and one. 'Flag' and 'Link' shall be supported in full.

40.1.8.2.44 Write(6) (0Ah). This command shall be optional, refer to 8.2.20 of SCSI-II.

40.1.8.2.45 Write(12) (AAh). This command shall be optional, refer to 15.2.14 of SCSI-II.

40.1.8.2.46 Write and Verify(10) (2Eh). This command shall be optional, refer to 15.2.15 of SCSI-II.

40.1.8.2.46.1 Command restrictions. The 'BytChk' bit shall be supported in full for both the values of zero and one. The 'RelAdr' bit shall be supported in full for both the values of zero and one. 'Flag' and 'Link' shall be supported in full.

40.1.8.2.47 Write and Verify(12)(AEh). This command shall be optional, refer to 15.2.16 of SCSI-II.

40.1.8.2.47.1 Command restrictions. The 'BytChk' bit shall be supported in full for both the values of zero and one. The 'RelAdr' bit shall be supported in full for both the values of zero and one. 'Flag' and 'Link' shall be supported in full.

40.1.8.2.48 Write Buffer (3Bh). This command shall be optional, refer to 7.2.17 of SCSI-II.

40.1.8.2.48.1 Command restrictions. Write buffer mode 'WRITE DATA' (010b) shall be supported as specified in SCSI-II. The download modes shall be optional on a per application basis. The download mode shall also support a download and save option which may alter device media or other nonvolatile memory.

40.1.8.2.49 Write Long (3Fh). This command shall be optional, refer to 8.2.23 of SCSI-II.

40.1.8.2.50 Write With Locks (BCh). This command shall be optional, refer to 40.1.1.2.33.

40.1.9 Medium-changer devices. The commands required for medium-changer devices shall be those specified as mandatory for both medium-changer devices and all device types in SCSI-II. No further restrictions shall be imposed.

40.1.10 Communications devices. The commands required for communications devices are those as specified as mandatory for both communications devices and all device types in SCSI-II. No further restrictions shall be imposed.

40.2 SCSI-II 6/10/12 byte command options. The command set of SCSI-II permits several options in standard command packet sizes, for example the READ command in various device types is available in 6-byte, 10-byte, & 12-byte commands. When implemented, the 6-byte commands shall be optional. The 6-byte commands are basically carryovers from SCSI-I and should be implemented for compatibility with existing earlier SCSI-I device driver routines. The 10-byte commands shall be mandatory. When implemented, the 12-byte commands shall be optional. The 12-byte commands should be implemented to provided support for future advances in device capacities.

40.3 Type-K optional command selection guidance. The unique Type K and optional SCSI-II commands are grouped by device type being further divided into the functional areas of Data Integrity Enhancing Commands, Backup and Archive Enhancing Commands, Performance Enhancing Commands, Security Enhancing Commands and Maintenance Enhancing Commands. This grouping of commands should provide a design checklist to balance design considerations during system requirements identification.

40.3.1 Command selection guidance for direct access devices. Table XXIX provides selection guidance for Type-K direct access optional commands. The commands are functionally grouped.

TABLE XXIX. Optional command guidance for direct access devices.

Command	Data Integrity	Backup and Archive	Performance	Security	Maintenance	Type K Cross Reference	SCSI-II Cross Reference
Change Definition			*			40.1.1.2.1	7.2.1
Compare	*					40.1.1.2.2	7.2.2
Copy		*				40.1.1.2.3	7.2.3
Copy & Verify		*				40.1.1.2.4	7.2.4
Data Destruct				*		40.1.1.2.5	Type K Unique
Lock Unlock Cache			*			40.1.1.2.6	8.2.2
Log Select					*	40.1.1.2.7	7.2.6
Log Sense					*	40.1.1.2.8	7.2.7
Pre-Fetch			*			40.1.1.2.11	8.2.3
Prevent-Allow Medium Removal				*		40.1.1.2.12	8.2.4
Read Buffer	*					40.1.1.2.13	7.2.12
Read Defect Data					*	40.1.1.2.14	8.2.8
Read Long					*	40.1.1.2.15	8.2.9
Read with Locks				*		40.1.1.2.16	Type K Unique
Reassign Blocks					*	40.1.1.2.17	8.2.10
Request Lock Table				*		40.1.1.2.18	Type K Unique
Search Data Equal			*			40.1.1.2.19	8.2.14.1
Search Data High			*			40.1.1.2.20	8.2.14.2
Search Data Low			*			40.1.1.2.21	8.2.14.3
Seek			*		*	40.1.1.2.22	8.2.15
Set Limits				*		40.1.1.2.24	8.2.16
Set Locks				*		40.1.1.2.25	Type K Unique
Start Stop Unit				*	*	40.1.1.2.26	8.2.17
Synchronize Cache			*			40.1.1.2.27	8.2.18
Verify	*					40.1.1.2.28	8.2.19
Write and Verify	*					40.1.1.2.29	8.2.22
Write Buffer	*					40.1.1.2.30	7.2.17
Write Long					*	40.1.1.2.31	8.2.23
Write Same	*				*	40.1.1.2.32	8.2.24
Write with Locks				*		40.1.1.2.33	Type K Unique

40.3.2 Command selection guidance for sequential access devices. Table XXX provides selection guidance for Type-K sequential access optional commands. The commands are functionally grouped.

TABLE XXX. Optional command guidance for sequential access devices.

Command	Data Integrity	Backup and Archive	Performance	Security	Maintenance	Type K Cross Reference	SCSI-II Cross Reference
Change Definition			*			40.1.2.2.1	7.2.1
Compare	*					40.1.2.2.2	7.2.2
Copy		*				40.1.2.2.3	7.2.3
Copy & Verify		*				40.1.2.2.4	7.2.4
Load Unload				*		40.1.2.2.5	9.2.2
Locate			*			40.1.2.2.6	9.2.3
Log Select					*	40.1.2.2.7	7.2.6
Log Sense					*	40.1.2.2.8	7.2.7
Prevent-Allow Medium Removal				*		40.1.2.2.11	8.2.4
Read Buffer	*					40.1.2.2.12	7.2.12
Read Position			*			40.1.2.2.13	9.2.6
Read Reverse			*			40.1.2.2.14	9.2.7
Recover Buffered Data	*					40.1.2.2.15	9.2.8
Verify	*					40.1.2.2.16	9.2.13
Write Buffer	*					40.1.2.2.17	7.2.17

40.3.3 Command selection guidance for write-once devices. Table XXXI provides selection guidance for Type-K write-once optional commands. The commands are functionally grouped.

TABLE XXXI. Optional command guidance for write-once devices.

Command	Data Integrity	Backup and Archive	Performance	Security	Maintenance	Type K Cross Reference	SCSI-II Cross Reference
Change Definition			*			40.1.5.2.1	7.2.1
Compare	*					40.1.5.2.2	7.2.2
Copy		*				40.1.5.2.3	7.2.3
Copy & Verify		*				40.1.5.2.4	7.2.4
Lock Unlock Cache			*			40.1.5.2.5	8.2.2
Log Select					*	40.1.5.2.6	7.2.6
Log Sense					*	40.1.5.2.7	7.2.7
Medium Scan			*			40.1.5.2.8	15.2.3
Pre-Fetch			*			40.1.5.2.11	8.2.3
Prevent-Allow Medium Removal				*		40.1.5.2.12	8.2.4
Read Buffer	*					40.1.5.2.15	7.2.12
Read Long					*	40.1.5.2.16	8.2.9
Read with Locks				*		40.1.5.2.17	Type K Unique
Reassign Blocks					*	40.1.5.2.18	8.2.10
Request Lock Table				*		40.1.5.2.19	Type K Unique
Search Data Equal			*			40.1.5.2.20	8.2.14.1
Search Data High			*			40.1.5.2.22	8.2.14.2
Search Data Low			*			40.1.5.2.24	8.2.14.3
Seek			*		*	40.1.5.2.26	8.2.15
Set Limits				*		40.1.5.2.28	8.2.16
Set Locks				*		40.1.5.2.30	Type K Unique
Start Stop Unit				*	*	40.1.5.2.31	8.2.17
Synchronize Cache			*			40.1.5.2.1	8.2.18
Verify	*					40.1.5.2.33	15.2.11
Write and Verify	*					40.1.5.2.37	8.2.22
Write Buffer	*					40.1.5.2.39	7.2.17
Write Long					*	40.1.5.2.40	8.2.23
Write with Locks				*		40.1.5.2.41	Type K Unique

40.3.4 Command selection guidance for CD-ROM devices. Table XXXII provides selection guidance for Type-K CD-ROM optional commands. The commands are functionally grouped.

TABLE XXXII. Optional command guidance for CD-ROM devices.

Command	Data Integrity	Backup and Archive	Performance	Security	Maintenance	Type K Cross Reference	SCSI-II Cross Reference
Change Definition			*			40.1.6.2.1	7.2.1
Compare	*					40.1.6.2.2	7.2.2
Copy		*				40.1.6.2.3	7.2.3
Copy & Verify		*				40.1.6.2.4	7.2.4
Lock Unlock Cache			*			40.1.6.2.5	8.2.2
Log Select					*	40.1.6.2.6	7.2.6
Log Sense					*	40.1.6.2.7	7.2.7
Pre-Fetch			*			40.1.6.2.17	8.2.3
Prevent-Allow Medium Removal				*		40.1.6.2.18	8.2.4
Read Buffer	*					40.1.6.2.21	7.2.12
Read Header					*	40.1.6.2.22	13.2.9
Read Long					*	40.1.6.2.23	8.2.9
Read Sub-Channel					*	40.1.6.2.24	13.2.10
Read TOC					*	40.1.6.2.25	13.2.11
Search Data Equal			*			40.1.6.2.26	8.2.14.1
Search Data High			*			40.1.6.2.28	8.2.14.2
Search Data Low			*			40.1.6.2.30	8.2.14.3
Seek			*		*	40.1.6.2.31	8.2.15
Set Limits				*		40.1.6.2.33	8.2.16
Start Stop Unit				*	*	40.1.6.2.35	8.2.17
Synchronize Cache			*			40.1.6.2.36	8.2.18
Verify	*					40.1.6.2.37	15.2.11
Write Buffer	*					40.1.6.2.39	7.2.17

40.3.5 Command selection guidance for optical memory devices. Table XXXIII provides selection guidance for Type-K Optical Memory optional commands. The commands are grouped functionally.

TABLE XXXIII. Optional command guidance for optical memory devices.

Command	Data Integrity	Backup and Archive	Performance	Security	Maintenance	Type K Cross Reference	SCSI-II Cross Reference
Change Definition			*			40.1.8.2.1	7.2.1
Compare	*					40.1.8.2.2	7.2.2
Copy		*				40.1.8.2.3	7.2.3
Copy & Verify		*				40.1.8.2.4	7.2.4
Data Destruct				*		40.1.8.2.5	Type K Unique
Erase			*			40.1.8.2.6	15.2.1
Lock Unlock Cache			*			40.1.8.2.9	8.2.2
Log Select					*	40.1.8.2.10	7.2.6
Log Sense					*	40.1.8.2.11	7.2.7
Medium Scan					*	40.1.8.2.12	15.2.3
Pre-Fetch			*			40.1.8.2.15	8.2.3
Prevent-Allow Medium Removal				*		40.1.8.2.16	8.2.4
Read Buffer	*					40.1.8.2.19	7.2.12
Read Defect Data					*	40.1.8.2.20	8.2.8
Read Generation		*				40.1.8.2.22	15.2.6
Read Long					*	40.1.8.2.23	8.2.9
Read Updated Block		*				40.1.8.2.24	15.2.7
Read with Locks				*		40.1.8.2.25	Type K Unique
Reassign Blocks					*	40.1.8.2.26	8.2.10
Request Lock Table				*		40.1.8.2.27	Type K Unique
Search Data Equal			*			40.1.8.2.28	8.2.14.1
Search Data High			*			40.1.8.2.30	8.2.14.2
Search Data Low			*			40.1.8.2.32	8.2.14.3
Seek			*		*	40.1.8.2.34	8.2.15
Set Limits				*		40.1.8.2.36	8.2.16
Set Locks				*		40.1.8.2.38	Type K Unique
Start Stop Unit				*	*	40.1.8.2.39	8.2.17
Synchronize Cache			*			40.1.8.2.40	8.2.18
Update Block		*				40.1.8.2.41	15.2.10
Verify	*					40.1.8.2.42	15.2.11
Write and Verify	*					40.1.8.2.46	15.2.15
Write Buffer	*					40.1.8.2.48	7.2.17
Write Long					*	40.1.8.2.49	8.2.23
Write with Locks				*		40.1.8.2.50	Type K Unique

40.4 Data Protection.

Data Protection for direct-access devices. Current Navy standard disks (i.e. AN/UYH-2, AN/UYH-3, AN/BYH-1, UYH-16 and AN/UYK-43 EMS) provide a data protection scheme prohibiting read/write accesses to the media unless certain conditions are met. This capability is a requirement for Navy disks being used on systems that require the data on the media be safeguarded. The commands, protocol, and hardware device protection of SCSI-II were evaluated and found inadequate to support the level of data protection required by most Navy applications. For this reason, additional optional SCSI-II commands, auxiliary definitions to existing commands, and a hardware device protection were developed and defined to fill the void. The level of protection defined by this standard applies to systems that have a host computer communicating externally to a disk over the Type K bus. It does not apply to systems that incorporate SCSI internally but communicate externally over another NTDS interface type. Those systems have their own protection scheme built into the communication protocol. The Type K bus data protection scheme was designed to be similar to other Navy user data protection schemes.

40.4.1.1 Data Protection commands for direct-access devices. Earlier in this section it was mentioned that SCSI-II defines some provisions for data protection (RESERVE, RELEASE, and SET LIMITS commands, etc.) but these do not meet Navy data security requirements. Although they can provide conditions whereby the data is protected (i.e., unit or extent reservations within the RESERVE and RELEASE commands), the protection condition is temporary. SCSI-II does not protect data on the bus from Bus Reset, hard reset, or a power cycle. Any one of these resets (clears) the protection condition leaving the media unprotected until an initiator re-establishes the protection conditions. The Type K data protection commands should create a permanent level (conditions) of protection which is still in effect (doesn't need re-establishing by an initiator) after a power cycle or reset. The Type K data protection shall be satisfied before access of the data on the media is allowed. Table XXXIV lists all commands supporting data protection.

TABLE XXXIV. Data Protection commands for direct-access devices.

Command (Code)	(New or Modified)	(Mandatory or Optional)	Paragraph
Mode Select(6) (15h)	Modified	Mandatory	40.1.1.1.3.1
Mode Select(10) (55h)	Modified	Optional	40.1.1.2.9.1
Mode Sense(6) (1Ah)	Modified	Mandatory	40.1.1.1.4.1
Mode Sense(10) (5Ah)	Modified	Optional	40.1.1.2.10.1
Request Sense (03h)	Modified	Mandatory	40.1.1.1.10.1
Read With Locks (BBh)	New	Optional	40.1.1.2.16
Read Lock Table (06h)	New	Optional	40.1.1.2.18
Set Locks (BDh)	New	Optional	40.1.1.2.25
Write With Locks (BCh)	New	Optional	40.1.1.2.33

To invoke data protection the user shall first send the Mode Select/Format Device Page command, with the "Data Protect Mode" bit set in the Format Device Page parameters, followed by the Format Unit command. Upon receipt of the format command the device controller shall, along with its normal operation of reformatting the media, build and maintain a non-volatile read/write lock table stored in the device. After successful completion of the format command the target device shall be in protect mode and shall have a read/write lock table built and maintainable for each LUN formatted. The LUN read/write lock table is usually located on the corresponding LUN's media in a reserved area not directly user accessible. For better performance a copy of the lock table should be kept in the internal memory of the target so that a read of the table off the media would not have to always be done for each read/write operation. If implemented, changes to the table should be maintained in both locations.

40.4.1.2 Data Protection hardware for direct-access devices. To support total functionality of the Type K data protection scheme a hardware switch shall be provided for each direct access device (target) in the hardware enclosure. For systems where a target has addressable logical units (LUNs) then, to segment the functionality, each LUN shall be required to have its own switch, otherwise, operation of all LUNs shall be

based on the target's hardware switch. The target processor shall be capable of reading the position of the hardware protection switch for each device it has the responsibility for doing the software protection checking. This document defines the switch to be two-position switch with the positions defined as ON and OFF. Table XXXV defines the actions of the target processor based on the software accesses made and the position of the switch.

TABLE XXXV. Command response to Data Protection.

COMMAND	Data Protection Switch – OFF 1/	Data Protection Switch -- ON 1/
Mode Select(6) (15h) Mode Select(10) (55h)	Process command, save "ENABLE PROTECT MODE" bit in Format Device Page	Reject command, send check condition status and sense data of "PROTECTION VIOLATION"
Format Unit (04h)	Process command, build Lock Table on device and internal RAM, allow access to all logical blocks	Reject command, send check condition status and sense data of "PROTECTION VIOLATION"
Data Destruct (0Ch)	Process command as specified herein	Reject command, send check condition status and sense data of "PROTECTION VIOLATION"
Set Locks (BDh) Read Lock Table (06h)	Process command if protect mode enabled, otherwise reject with "INVALID COMMAND"	Reject command, send check condition status and sense data of "PROTECTION VIOLATION"
Compare (39h) Change Definition (40h) Copy (18h) Copy and Verify (3Ah) Pre-Fetch (34h) Read(6) (08h) Read(10) (28h) Read Long (3Eh) Set Limits (33h) Search Data Equal (31h) Search Data High (30h) Search Data Low (32h) Write(6) (0Ah) Write(10) (2Ah) Write and Verify (2Eh) Write Long (3Fh) Write Same (41h)	Process command if protect mode enabled and read/write locks equal zero on all logical blocks referenced	Reject command, send check condition status and sense data of "PROTECTION VIOLATION"
Read With Locks (BBh) Write With Locks (BCh)	Process command if protect mode enabled, otherwise reject with "INVALID COMMAND"	Process command if read/write keys of command equal the read/write locks in the table for all logical blocks referenced
Inquiry (12h) Read Capacity (25h) Receive Diagnostic Results (1Ch) Release (17h) Request Sense (03h) Reserve (16h) Rezero Unit (01h) Send Diagnostics (1Dh) Start Stop Unit (1Bh) Test Unit Ready (00h) Verify (2Fh)	Always legal	Always legal

1/ This document does not require that each switch, defined in the system that implements Type K, to be a key switch with it's own unique keycode, that the key be captive/non-captive in either position, or that it even needs to be a key switch at all. Maybe a simple toggle switch that is protected will satisfy the requirements in this area. It only states that these are important options that shall be evaluated during the design of the target system.

TYPE K (SCSI-II) DESIGN GUIDANCE

10. SCOPE

10.1 Scope. This appendix provides additional background and information for the implementation of Type K interfaces specified in this standard. This appendix forms an optional part of this standard.

20 REFERENCE DOCUMENTS

Not applicable.

30 DEFINITIONS

Not applicable.

40 GENERAL REQUIREMENTS

40.1 Background. The Type K interface is derived from the commercial bus standard, SCSI-II. The commercial standard has been tailored for use in Navy Mission Critical Computer Resource (MCCR) systems. SCSI-II includes many options with regards to every aspect of the bus including the physical medium, physical connectors, command sets, and the message system. The purpose of this standard is to define specific requirements in these areas and identify which options within the SCSI-II are mandatory requirements for Navy Systems. This standard is not all inclusive. SCSI-II shall accompany this standard when using this standard for the Type K interface. The Type K designer shall follow SCSI-II for any electrical performance items not addressed by this standard. Options identified in SCSI-II but not addressed in this standard shall remain optional.

40.2 Compatibility. Adherence to Type K should result in the production of devices which are 100% compatible with any properly made commercially available differential optioned SCSI-II device. Adherence to this standard shall not jeopardize system level performance with commercial devices and may even provide interface enhancement under certain circumstances.

SCSI-II defines extensions to the ANSI X3.131-1986 (SCSI-I). One of the key objectives of SCSI-II is to provide compatibility with those SCSI-I devices which support bus parity. Therefore there is no need to specifically reference material in SCSI-I unless it is not captured in SCSI-II.

50 DETAILED REQUIREMENTS

50.1 Physical characteristics.

50.1.1 Cabling.

50.1.1.1 Cable requirements. The A and B cable requirements in SCSI-II do not apply to Type K.

50.1.1.2 *Total system cable length.* The Type K interface is a parallel signal bus designed for external device connectivity. Each device is considered part of the total bus and is connected to the rest of the bus configuration via two connectors. Internally, these connectors are interconnected with cabling fashioned in a loop-through manner. Externally, the devices are connected to each other via multi-conductor cabling. In Type K this bus cabling is composed of the complete summed length of internal wiring harnesses (of each of the Type K devices on the bus) interconnected with MIL-C-24643 LS2U-45 external cabling. The LS2U-45 military cable is a 45-twisted-pair, planetary lay cable, with an optimized (high noise immunity) braided shield and low smoke outer jacket. Since each bus signal communicates via two wires, each signal is assigned to one twisted pair in the LS2U-45 cabling. The internal wiring harnesses consist of flexible cabling (which is usually flat or ribbon type) and the pairing of signals internally is left to the equipment designer (i.e. within certain electrical parameters to maintain bus integrity which will be described later in more detail). SCSI-II and Type K both require the total bus length to be limited to 25 meters or approximately 82 feet. Longer length interfaces may be possible on a case to case basis if electrical and timing parameters are met.

50.1.1.3 Total internal cable length. It is recommended that the maximum delay due to internal cable length for each electrical cabinet not exceed 27 ns with a maximum skew of 1 ns between lines.

50.1.1.4 Cable spacing. To ensure impedance characteristics and signal quality, spacing between Type K internal cables and equipment ground planes or other cables within the equipment shall be a minimum of 0.6 centimeters.

50.1.2 Type K electrical description. Type K electrical signals are implemented on a multiple user bus architecture retaining most of the features detailed in SCSI-II. The multi-user bus protocol is maintained even for a two device point-to-point implementation. Since certain bus signals are bi-directional, the electrical characteristics of input and output are intertwined and interactive. However, in Type K, the differential composite signals have been detailed for input parameters and single-ended values have been supplied for output parameters. The input and output parameters have been segregated in this specification to convey more stringent electrical guidelines. This will ensure proper signal integrity in a noisy electromagnetic shipboard environment.

Single-Ended signal drivers shall not be permitted in this standard. Single-Ended parameters are included because they apply to the differential option when no specific parameters are given.

50.1.2.1 Average measured composite DC voltage (V_{AM}). SCSI-II delineates the EIA RS-485 specification for signal drivers and receivers. RS-485 is a true differential specification and does not preclude common mode voltage drivers. Since Type K differential signal lines contain DC voltages and currents (supplied by the termination circuits on each end of the bus), using common mode driver circuits with Type K differential receivers and terminators will display driver DC offset values when measured on the bus. The DC offset values are dependent upon common mode voltages of the drivers on the bus and the distance from the measurement point to the drivers and the terminators on the bus.

To make consistent measurements of operating circuits at any point on the Type K bus, an averaging voltage measurement technique is required. This technique requires taking a 50% DC voltage measurement of each SIGNAL(+) and SIGNAL(-) line and averaging the two together. This average measured composite DC voltage (V_{AM}) is then used to calculate the maximum and minimum parameters for amplitude, rise and fall times, and skew. Since the Type K receiver is truly differential, the averaging measurement technique ensures a minimum differential signal swing between the SIGNAL(+) and SIGNAL(-) lines and precludes large amplitude single-ended drivers with a single DC offset.

50.1.2.2 Wire-ORed Signals. SCSI-II does not specifically provide for the open collector driver signals RST, BSY and SEL signals in differential circuits. Single-ended SCSI-II specifies open collector drivers for ORed signals RST, BSY and SEL. Because of the terminator voltage division in differential SCSI-II, it is not possible to obtain a SIGNAL(+) greater than 2.7 Vdc and a SIGNAL(-) less than 1.7 Vdc simultaneously with purely open collector drivers. Type K implementation of differential ORed drivers for RST, BSY and SEL signals shall be actively driven true (State 1) and tri-stated (State 3) on a false condition.

50.1.2.3 Output Characteristics of Signal Lines. Each control and data bit driver output shall obey the following output characteristics:

a. Each port shall be capable of driving into 100 feet of terminated LS2U-45 type cabling, with the minimum output characteristics shown in figure 44. This will ensure that the devices will be able to drive 7 devices @ 25 pF/stub +82 feet of system bus cabling in a maximum length configuration. The 100 feet of terminated LS2U-45 type cable represents a maximum configuration.

c. Each port will have a signal to signal state transition skew time less than or equal to 12 ns when measured at the V_{AM} volts crossing point between any matched SIGNAL(+) and SIGNAL(-) voltages. This will ensure the devices will not linger at the state change region and will limit the length of time of a state change to a predictable region.

d. Each SIGNAL(+) and SIGNAL(-) output signal will have rise times between 5 and 60 ns when measured between V_{AM}+.5 and V_{AM}-.5 Volts. The lower limit ensures that signals will not respond to impedance inconsistencies between the external cabling, wiring harnesses, and stubs due to reflections. The upper limit ensures waveform topology that is commensurate with the pulse widths of nominal Type K signals, this decreases possible additional skew times between bus signals due to highly divergent drivers.

50.1.2.4 TERMINATOR POWER (TERMPWR). Using the TERMPWR voltage, each Type K device shall supply pull-up power to the terminator networks for all the bus signals. TERMPWR shall be diode coupled to the bus with voltage range of 4.4 to 5.25 volts (measured on the bus). SCSI-II is considered too liberal for Navy applications with the voltage range of this power, and will allow significant voltage differences between devices. This voltage difference can shift a valid transmitted pulse at one end of the bus to a different value at the receiver by the difference of this DC value. Since the voltage waveforms are measured with respect to specific values, a DC shift can be misinterpreted as out of the specified range. To ensure that voltages transmitted at one end of the bus are not significantly DC shifted, the voltage range of this DC signal shall be tightened and each device shall diode couple their supply from the bus. TERMPWR supplies for Type K shall be able to supply up to 2 amperes of current.

50.1.2.5 Bonding and Grounding. Each Type K device will extend the system cabinet ground to the MIL-STD-28840 connector to act as a faraday shield for Type K signals on external LS2U-45 cables. The Type K device will allow Class B bonds to the cabinets exterior in accordance with MIL-STD-1310D.

It should be noted that the differential option of SCSI-II is not a true 'differential' transceiver design (in the purest sense of the definition) since the signals are not truly high impedance decoupled or 'floated' from ground and power sources. Each signal voltage is pulled up/down via voltage division of the terminator network to the power and grounds of the individual devices. This is accomplished when all drivers are tri-stated via the termination resistor networks on the ends of the bus. This 'psendo' differential mode (complementary voltage mode) requires that specific voltage values define each high/low signal of the pseudo-differential pair, not just their difference. If the bus has the capability to operate with common mode induced voltages, then the high and low state values of the drivers shall be measured with respect to the common mode voltage that is induced, not external ground. In the differential option of SCSI-II, the ground wires and terminator power wires are also on the bus, therefore, they shall also contain the same value of common mode induced voltages as the signals themselves. In this light it is difficult to determine the exact nature of the common mode operational and protection capabilities listed for RS-485 signals with respect to the differential option of SCSI-II operation and the effects of differing connection schemes between the earth, chassis, and signal grounds. See figure 45 for an example of a point-to-point single signal transceiver interconnection in a Type K bus or multi-point implementation. Figure 45 also shows relationships between device grounds, terminator power, and terminator electrical connectivity.

50.2 Logical characteristics.

50.2.1 Message system. The message system permits communication between an initiator and a target for the purpose of interface management. SCSI-II allows many optional implementations of the message system. The message system provides a level of control between individual phase transactions and the command level operations of the bus. Generally, messages accomplish the following:

a. Establish modes of operation for phase transactions (i.e. wide transfer, synchronous transfer),
b. Link and queue commands to establish order of execution (i.e. queue tag messages),
c. Abort or reset target operations (i.e. abort, reset, terminate I/O process).
d. Report or recover from errors that occur during transactions (i.e. bus parity errors),
e. Maintain data pointers during data transfers (i.e. save or restore data pointers),

A message going either direction shall be one, two, or multiple bytes in length. One or more messages may be sent during a single MESSAGE phase, but a message shall not be split between multiple MESSAGE phases. The initiator shall end the MESSAGE OUT phase by negating ATN when it sends certain messages.

The first message sent by the initiator after the SELECTION phase shall be either: IDENTIFY, ABORT, or BUS DEVICE RESET message. If a target receives any other message, then it shall go to BUS FREE phase.

50.2.1.1 Message system implementation. The message system implementation causes the most attachment difficulties between Type K devices. Since no minimum working set of messages is defined, the number of possible variations is enormous. The systems integrator shall be responsible for insuring proper systems compatibility between different devices on the Type K bus. The systems integrator shall identify which messages are supported and implemented (see 50.2.1.2 for a minimum message system implementation). A process for error handling shall also be identified and specified.

50.2.1.2 Minimum message system. Provided in this section is an example of how the message system implementation for a Type K device should be documented. Included are the following: the message system support table, message system phase implementation table and message system error recovery procedures.

50.2.1.2.1 Message system support. The message system support table (table XXXVI) shall be used to identify the messages supported by individual equipment. This table contains a list of all messages identified in SCSI-II and indicates whether initiator and/or target modes are supported. This table is based upon the implementation of the AN/UYH-16(V) Mass Memory Storage Device (a militarized disk system supporting target mode only).

The "Support" column in table XXXVI should be expanded by the systems integrator to include a column for each possible device on the Type K bus. Any conflicts (supported vs. not supported) should be clearly defined and documented to address possible incompatibilities impacting system operation.

TABLE XXXVI. Message system support.

Code	Support Initiator	Support Target	Message Name	Direction		Negate ATN before last ACK
06h	M	M	ABORT		Out	Yes
0Dh	–	–	ABORT TAG 1/		Out	Yes
0Ch	M	M	BUS DEVICE RESET		Out	Yes
0Eh	–	–	CLEAR QUEUE 1/		Out	Yes
00h	M	M	COMMAND COMPLETE	In		n/a
04h	–	M	DISCONNECT	In		n/a
04h	–	–	DISCONNECT		Out	Yes
80h-FFh	M	M	IDENTIFY	In		n/a
80h-FFh	M	M	IDENTIFY		Out	no
23h	–	–	IGNORE WIDE RESIDUE (two bytes)	In		n/a
0Fh	–	–	INITIATE RECOVERY	In		n/a
0Fh	–	–	INITIATE RECOVERY 2/		Out	Yes
05h	M	M	INITIATOR DETECTED ERROR		Out	Yes
0Ah	–	–	LINKED COMMAND COMPLETE	In		n/a
0Bh	–	–	LINKED COMMAND COMPLETE (WITH FLAG)	In		n/a
09H	M	M	MESSAGE PARITY ERROR		Out	Yes
07h	M	M	MESSAGE REJECT	In	Out	Yes
note 3/	–	–	MODIFY DATA POINTER	In		n/a
08h	M	M	NO OPERATION		Out	Yes
			Queue tag messages (two bytes)			
21h	–	–	> HEAD OF QUEUE TAG		Out	No
22h	–	–	> ORDERED QUEUE TAG		Out	No
20h	–	–	> SIMPLE QUEUE TAG	In	Out	No
10h	–	–	RELEASE RECOVERY		Out	Yes
03h	–	–	RESTORE POINTERS	In		n/a
02h	–	–	SAVE DATA POINTERS	In		n/a
note 3/	M	M	SYNCHRONOUS DATA TRANSFER REQUEST	In	Out	Yes
11h	–	–	TERMINATE I/O PROCESS		Out	Yes
note 3/	M	M	WIDE DATA TRANSFER REQUEST	In	Out	Yes
12h-1Fh	–	–	(Reserved)			
24h-2Fh	–	–	(Reserved for two-byte messages)			
30h-7Fh	–	–	(Reserved)			

Key:			
	M	=	Mandatory support
	–	=	Not implemented
	In	=	Target to Initiator
	Out	=	Initiator to target
	Yes	=	Initiator shall negate ATN before last ACK of message.
	No	=	Initiator may or may not negate ATN before last ACK of message. See 6.2.1 of SCSI-II.

1/ The ABORT TAG and CLEAR QUEUE messages are required if tagged queuing is implemented.
2/ Outbound INITIATE RECOVERY messages are only valid during the asynchronous event notification protocol.
3/ Extended message, refer to table 11 and table 12 of SCSI-II.

50.2.1.2.2 Message system phase implementation. The minimum message system phase implementation table shall identify when messages are supported in the process of implementing a SCSI-II command. Table XXXVII gives an example. Each row of the table represents a message supported by one or more devices on the Type K bus. The response of each device under each of the bus phases shall be shown in the row. Table XXXVII should be used to identify incompatibilities between devices on the bus. Each incompatibility shall be documented by the system integrator identifying impacts on the system.

Table XXXVII. Minimum message implementation.

			PREVIOUS PHASES						
Code	Message Name	Device	Cmd	Status	Msg In	Msg Out	Data In	Data Out	Sel / Resl
06	Abort	I	S	S	S	S	S	S	N/A
		T	A	A	A	A	A	A	CE
0C	Bus Device Reset	I	S	S	S	S	S	S	S
		T	A	A	A	A	A	A	A
00	Command Complete	I	A	A	A	A	A	A	A
		T	N/A	S	S	S	N/A	N/A	N/A
04	Disconnect	I	A	A	A	A	A	A	A
		T	S	S	S	S	S	S	N/A
80-FF	Identify (Initiator)	I	N/A	N/A	N/A	N/A	N/A	N/A	S
		T	MR	MR	MR	MR	MR	MR	A
80-FF	Identify (Target)	I	A	A	A	A	A	A	A
		T	N/A	N/A	N/A	N/A	N/A	N/A	S
05	Initiator Detected	I	S	S	S	S	S	S	S
	Error	T	CE	A	A	A	A	A	CE
09	Message Parity	I	N/A	N/A	S	N/A	N/A	N/A	N/A
	Error	T	MR	MR	A	MR	MR	MR	CE
07	Message Reject	I	A	A	A	A	A	A	A
		T	N/A	N/A	N/A	S	N/A	N/A	N/A
08	No Operation	I	S	S	S	S	S	S	N/A
		T	A	A	A	A	A	A	CE
note 1/	Synchronous Data	I	S	N/A	S	S	N/A	N/A	N/A
	Transfer Request	T	A	MR	A	A	MR	MR	CE
note 1/	Wide Data	I	S	N/A	S	S	N/A	N/A	N/A
	Transfer Request	T	A	MR	A	A	MR	MR	CE

KEY:
A = Accepted
S = Sent
MR = Message Rejected
CE = Catastrophic Error (Bus Released)
N/A = Not Applicable

1/ Extended message , refer to table 11 and table 12 of SCSI-II.

50.2.1.2.3 Message system error recovery procedures. The system implementor shall define how messages are used in the error recovery procedures. SCSI-II allows the message system to recover from certain transfer errors at the device interface level. An example might be when a parity error is detected on the bus during a data transfer. Some devices may try to recover by restoring data pointers to the last saved value and restarting the transfer at that point. If this type of approach is not supported by both devices, problems occur. The evaluation of error handlers is not straight forward. In general, each error handler approach needs to be defined for each bus phase for each device and compared with other devices for compatibility. The large number of possible error handler combinations precludes a table type of comparison approach but requires a detailed analysis. What is suggested is to not handle errors at the device interface level but instead perform error reporting as described in 50.2.1.2.3.1.

50.2.1.2.3.1 Initiator error handling (AN/UYH-16(V) example). The error recovery approach presented does not provide for device level recovery, but provides a consistent approach from device to device.

"Message Parity Error"
For all phases operating in the target mode shall respond to a "Message Parity Error" message received from the initiator by entering into Status Phase and responding with a "Check Condition" status. The sense data shall be set to "Communication Error".

"Initiator Detected Error"
For all phases operating in the target mode shall respond to a "Initiator Detected Error" message received from the initiator by entering into Status Phase and responding with a "Check Condition" status. The sense data shall be set to "Communication Error".

"Detected Error"
The device shall response to errors detected during bus transfers by entering into Status Phase and responding with a "Check Condition" status. The sense data shall be set to "Communication Error".

"Unreportable Errors"
For any other error conditions not described above, the device shall respond using a "Catastrophic Error" (unexpected disconnect).

50.2.1.3 Design recommendations. Ultimately, the systems integrator is responsible for insuring device compatibility. Whenever possible, the tables and descriptions identified in 50.2.1.2 should be completed and agreed upon at the beginning of device development.

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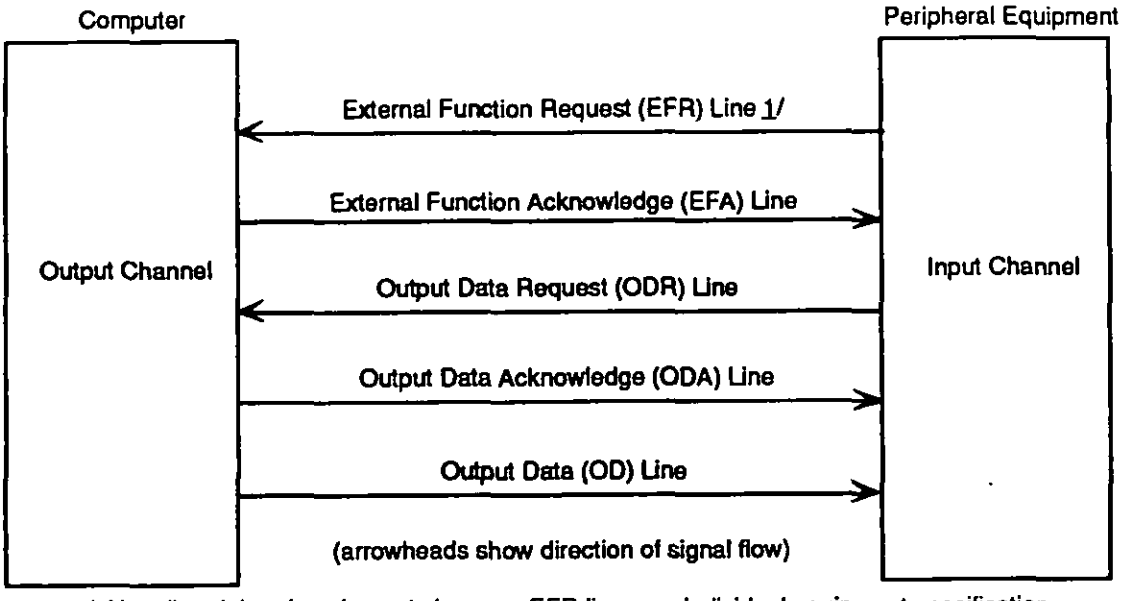
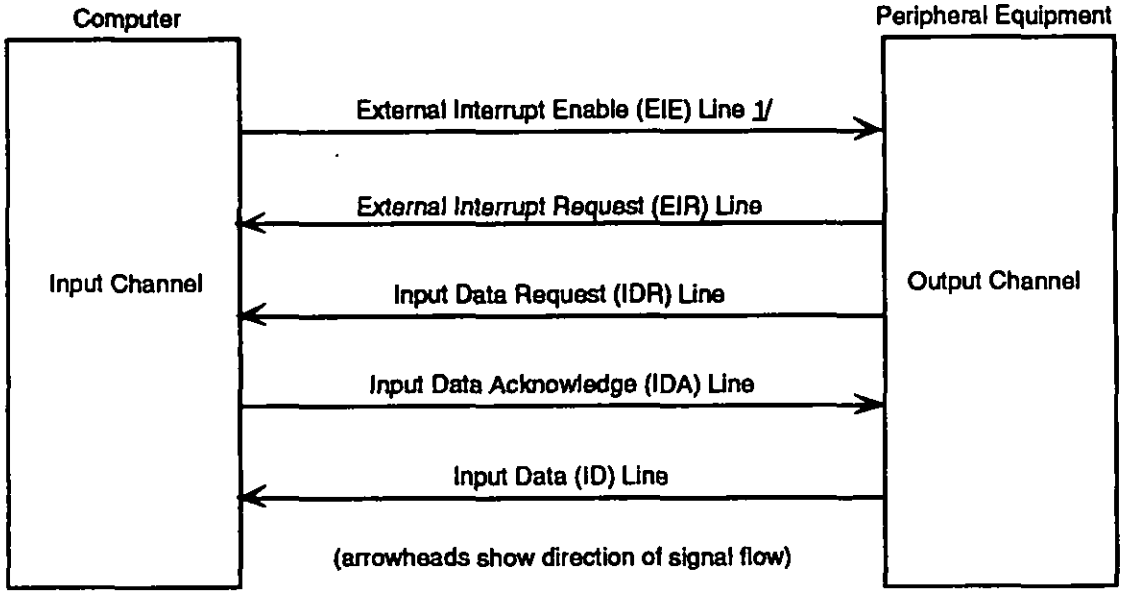


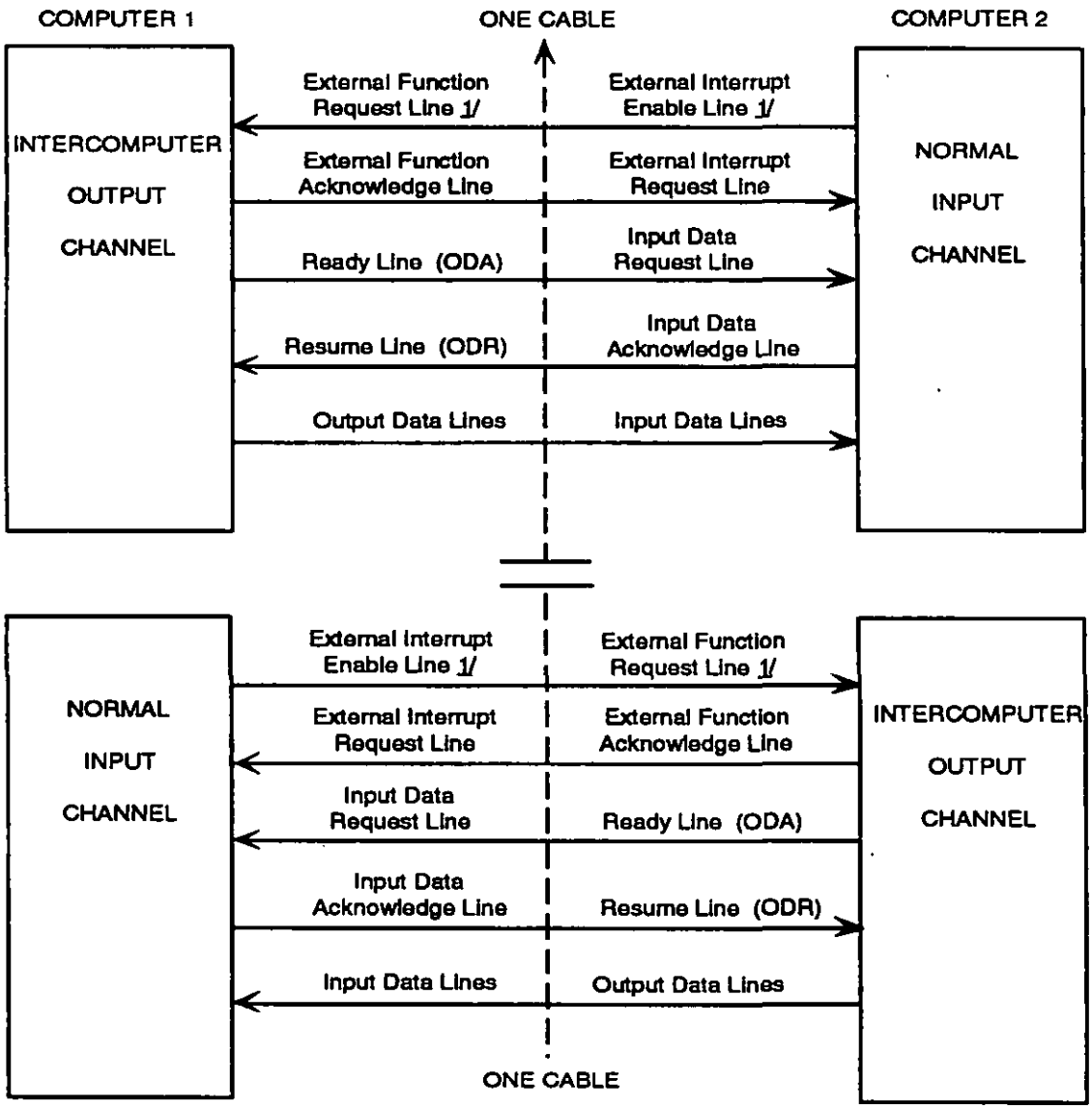
1/ Not all peripheral equipments have an EFR line, see individual equipment specification.

FIGURE 1. Output communication interface.



1/ Not all computers have an EIE line, see individual equipment specification.

FIGURE 2. Input communication interface.



(arrowheads show direction of signal flow)

1/ Not all equipments have an EIE or EFR line, see individual equipment specification.

FIGURE 3. Intercomputer interface.

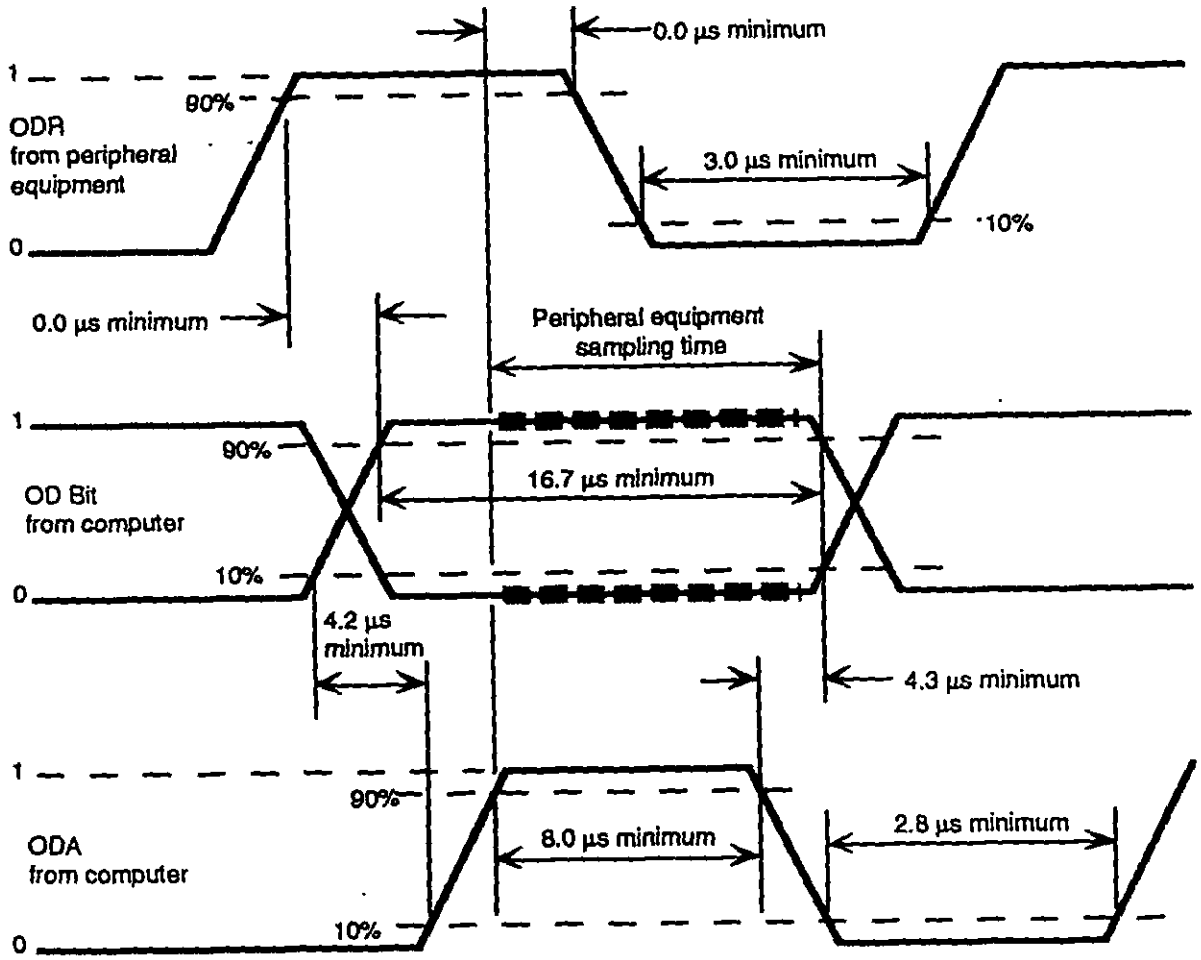
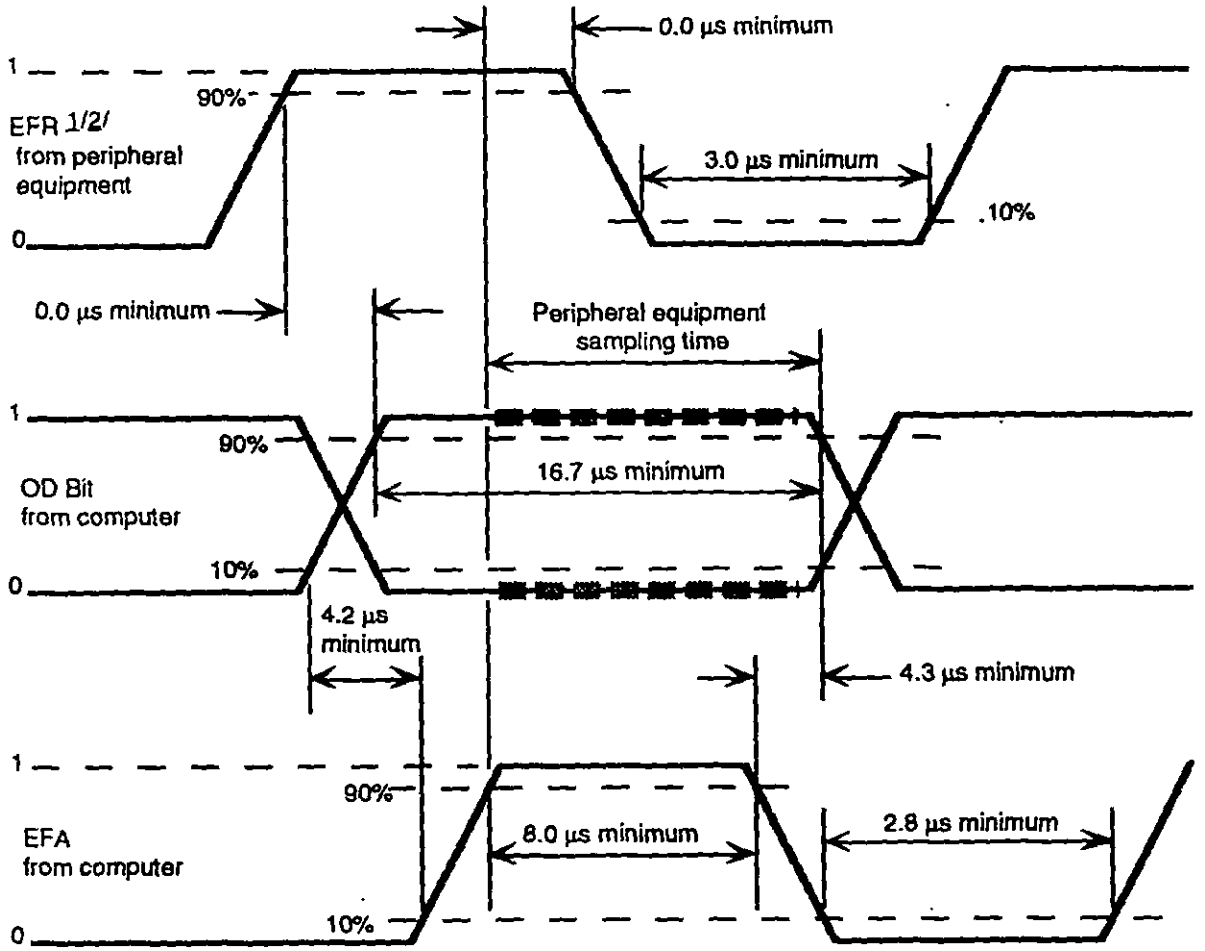


FIGURE 4. Type A output data timing.



1/ EFR not used for forced EF.
2/ When the EFR is not provided by the peripheral, then forced EF shall be used.

FIGURE 5. Type A external function timing.

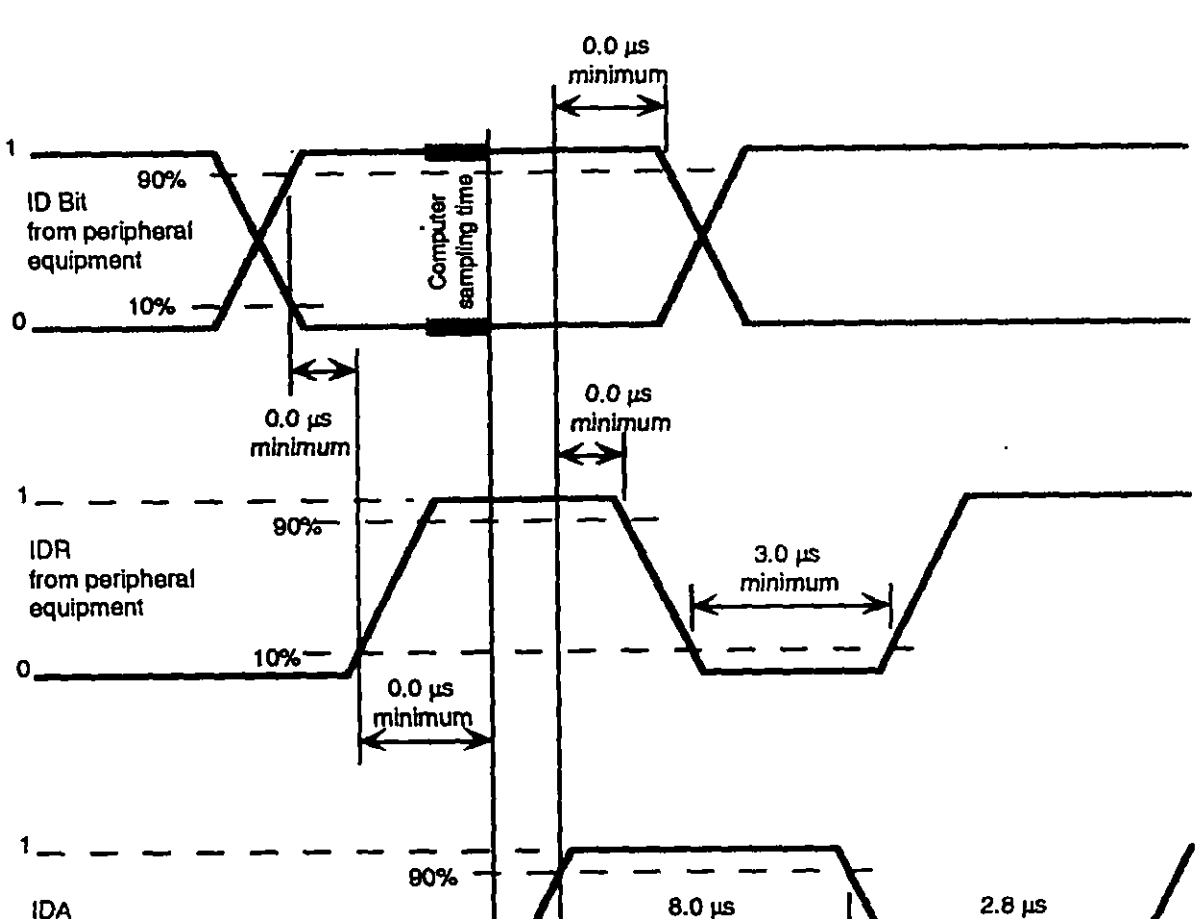
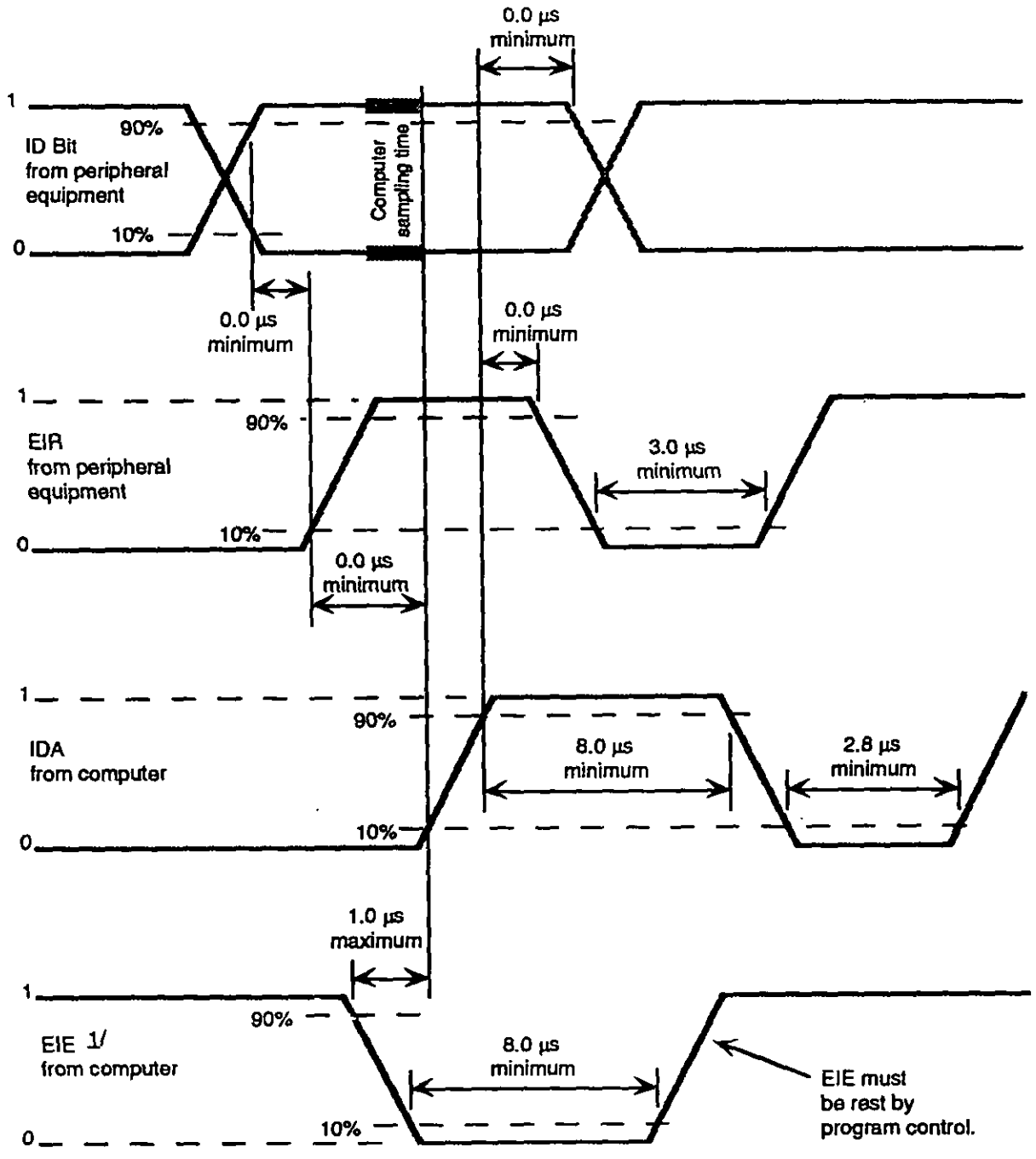


FIGURE 6. Type A input data timing.



1/ EIE signal not provided by some computers.

FIGURE 7. Type A external interrupt timing.

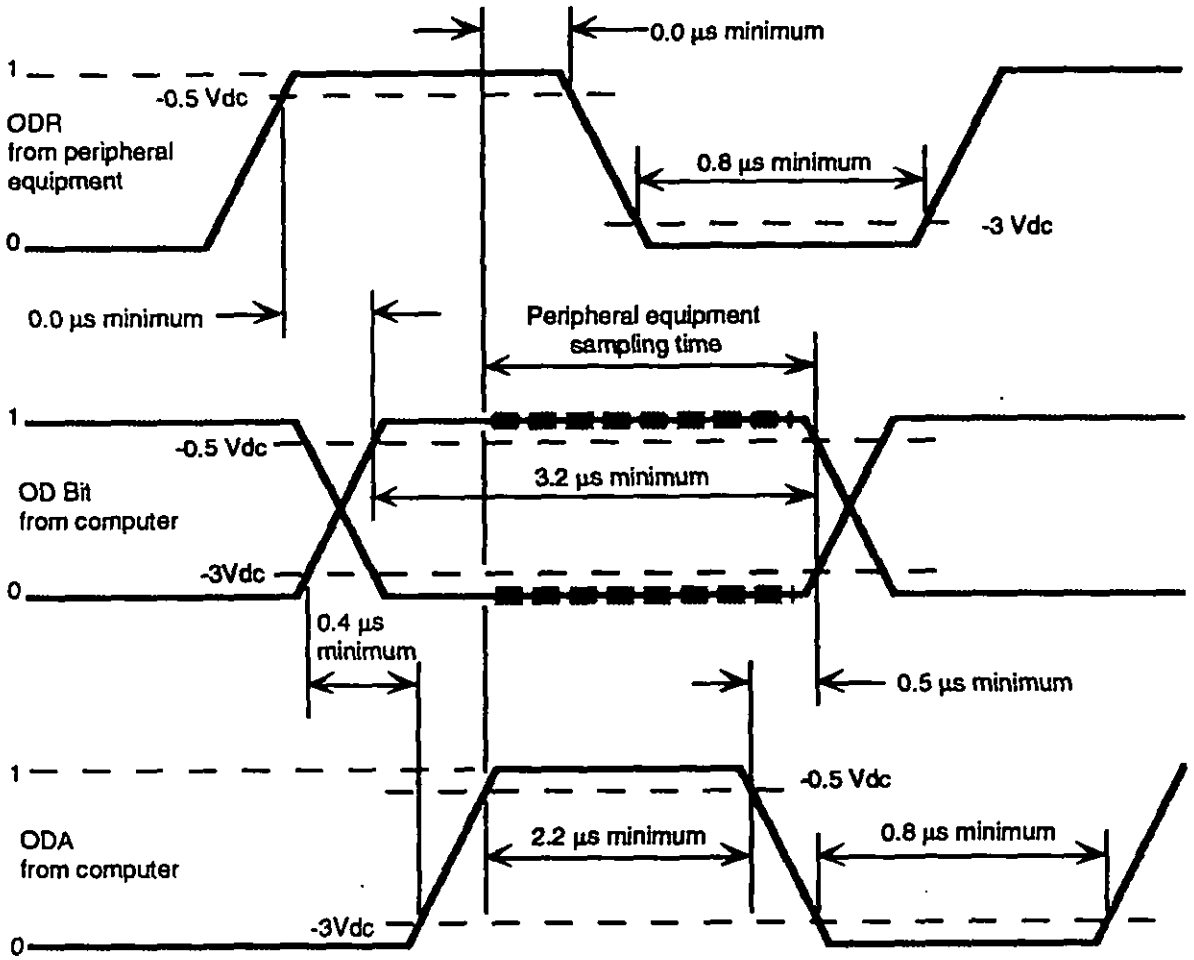
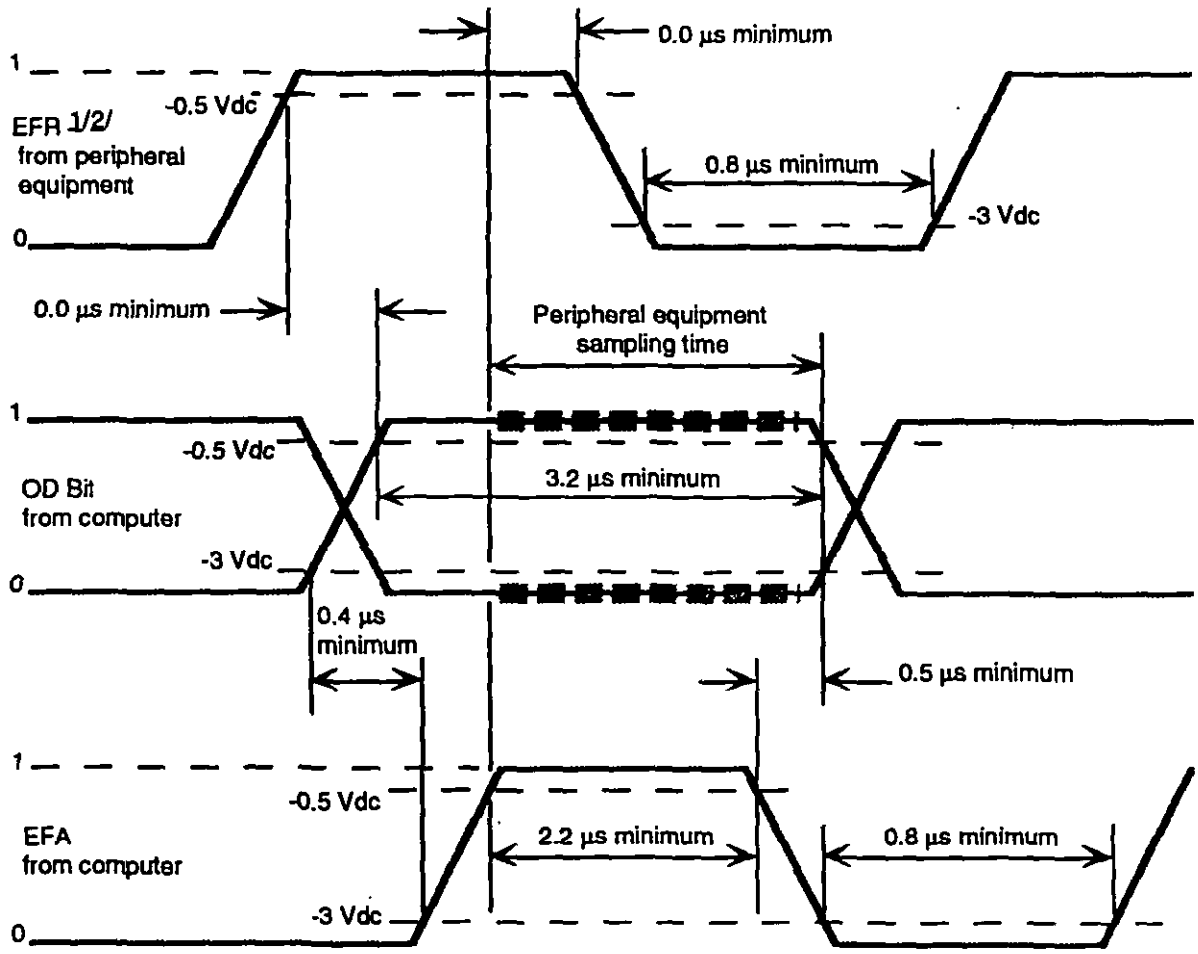


FIGURE 8. Type B output data timing.



1/ EFR not used for forced EF.
2/ When the EFR is not provided by the peripheral, then forced EF shall be used.

FIGURE 9. Type B external function timing.

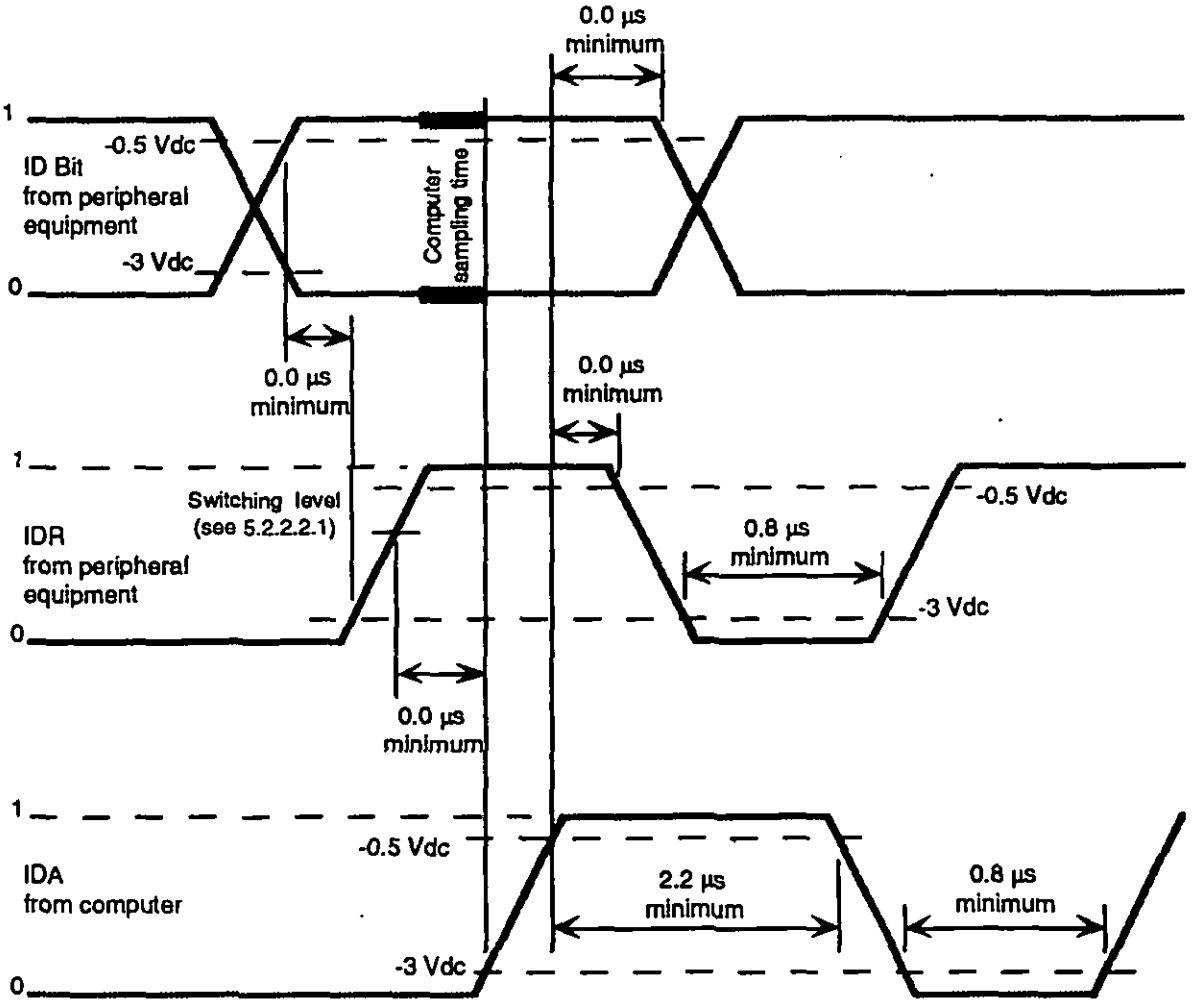
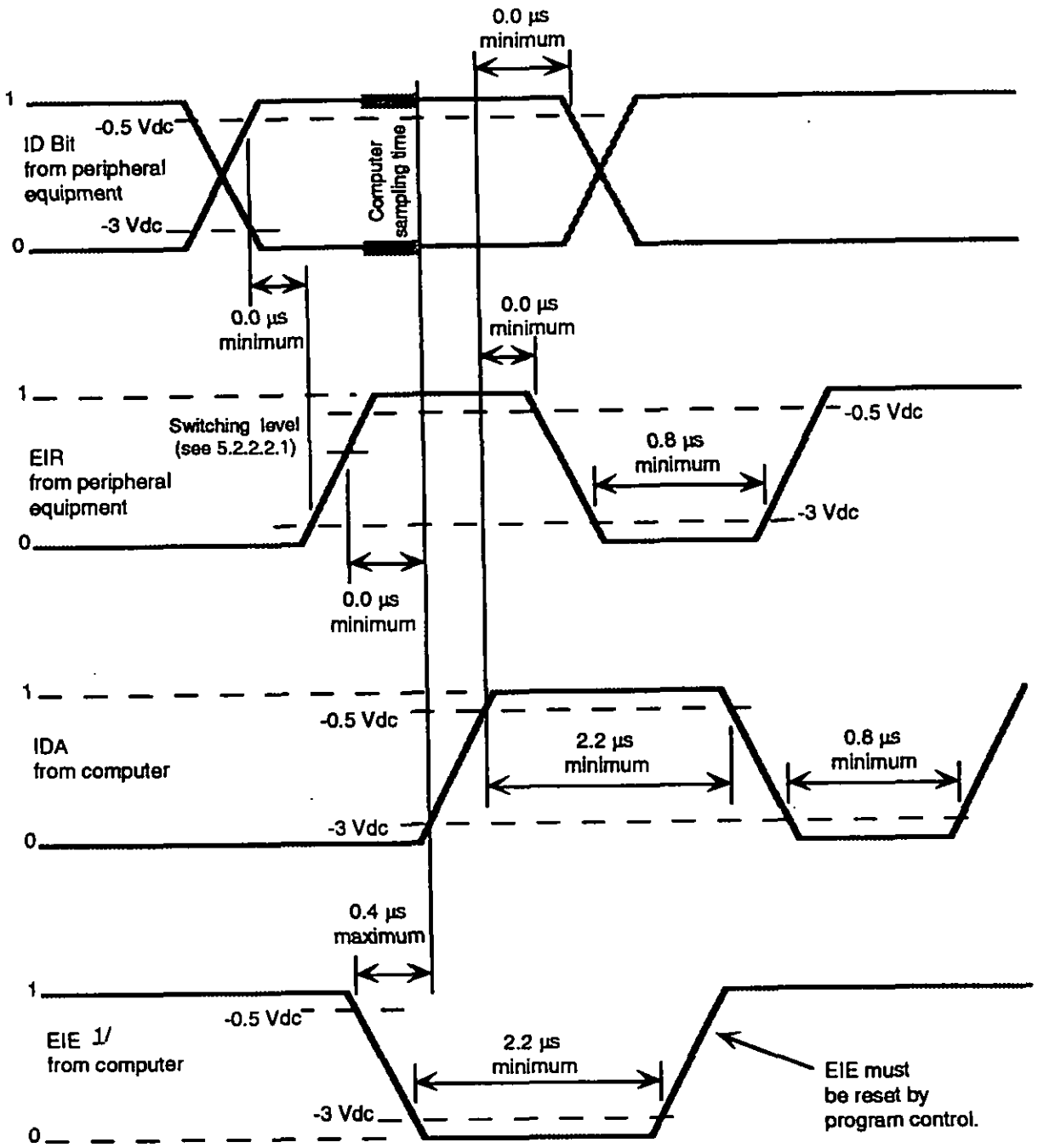


FIGURE 10. Type B input data timing.



1/ EIE signal not provided by some computers.

FIGURE 11. Type B external interrupt timing.

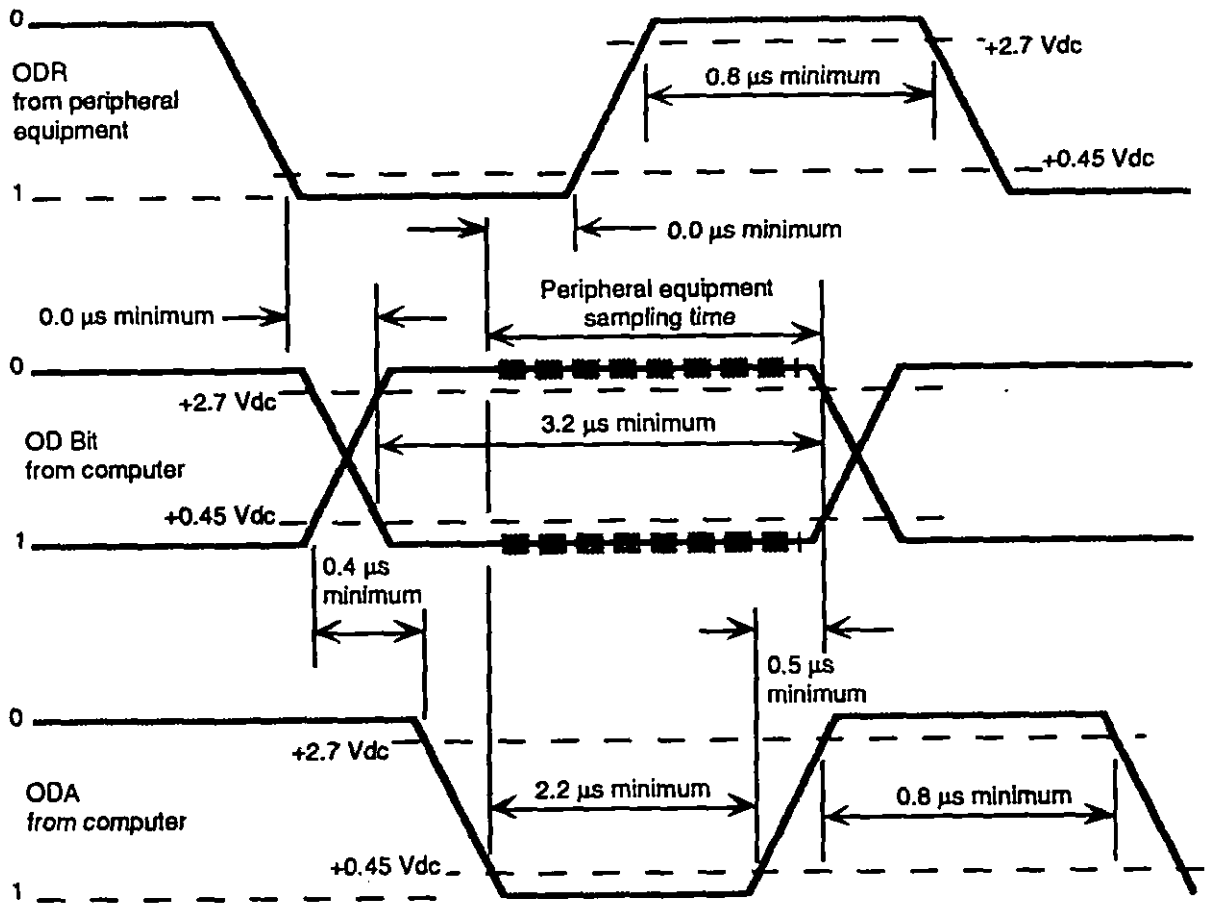
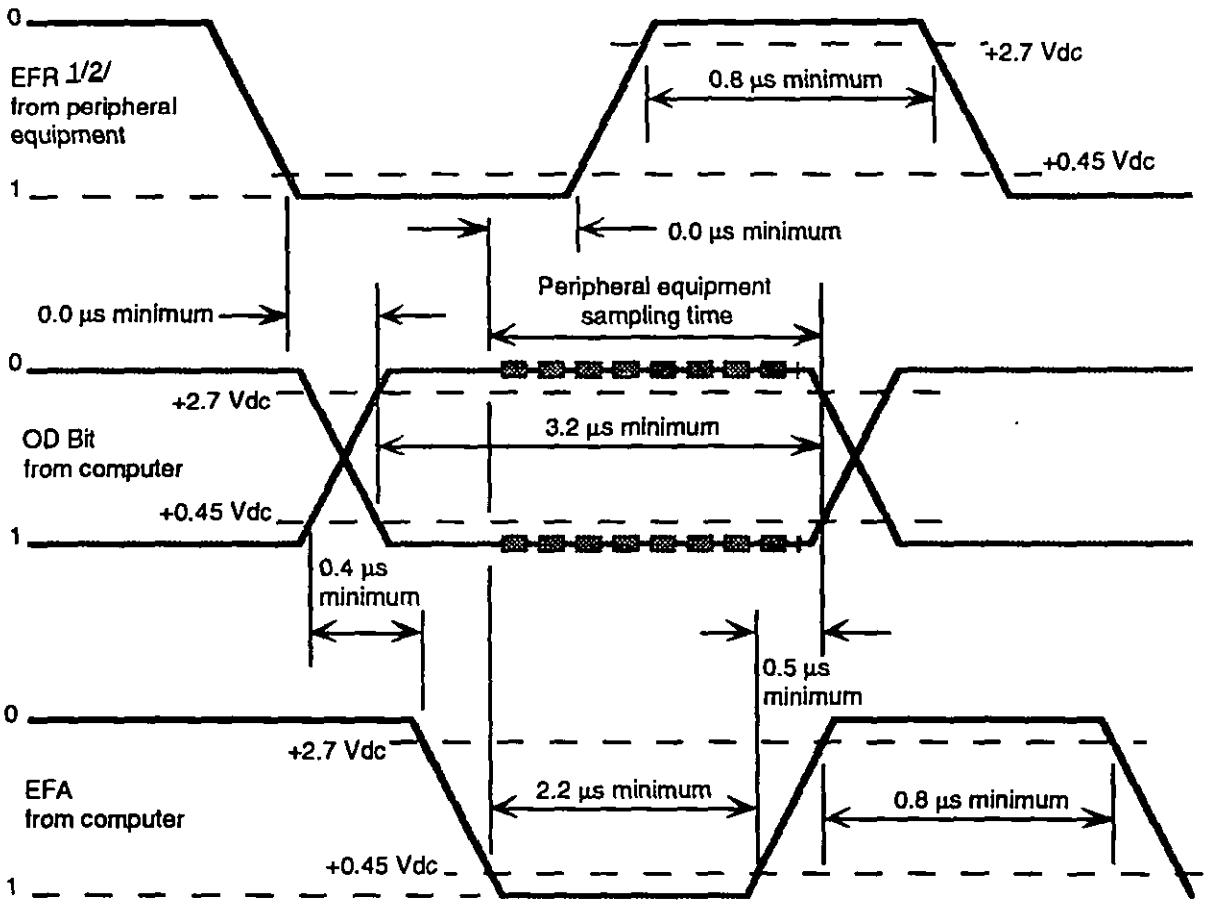


FIGURE 12. Type C output data timing.



1/ EFR not used for forced EF.
2/ When the EFR is not provided by the peripheral then forced EF shall be used.

FIGURE 13. Type C external function timing.

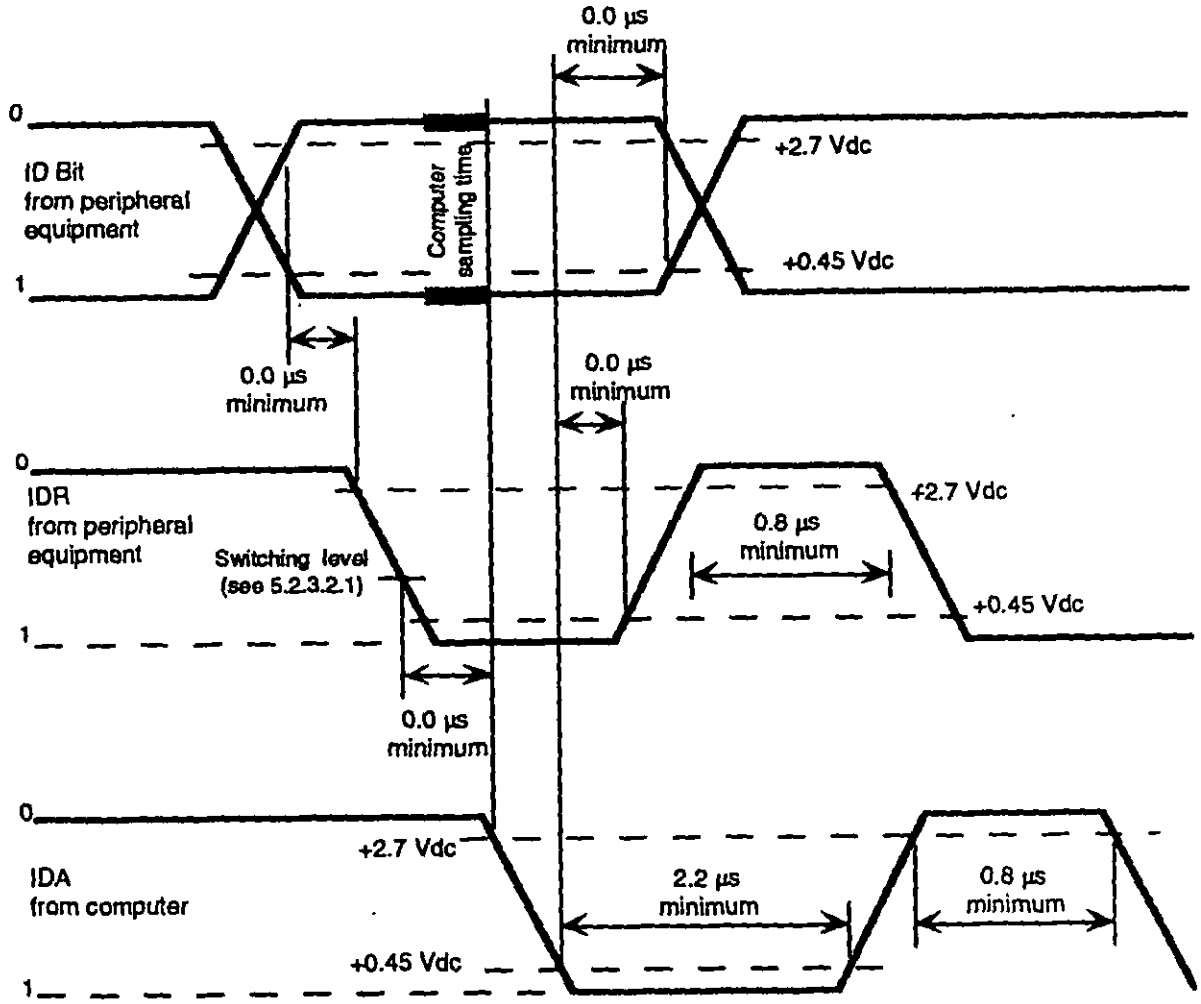
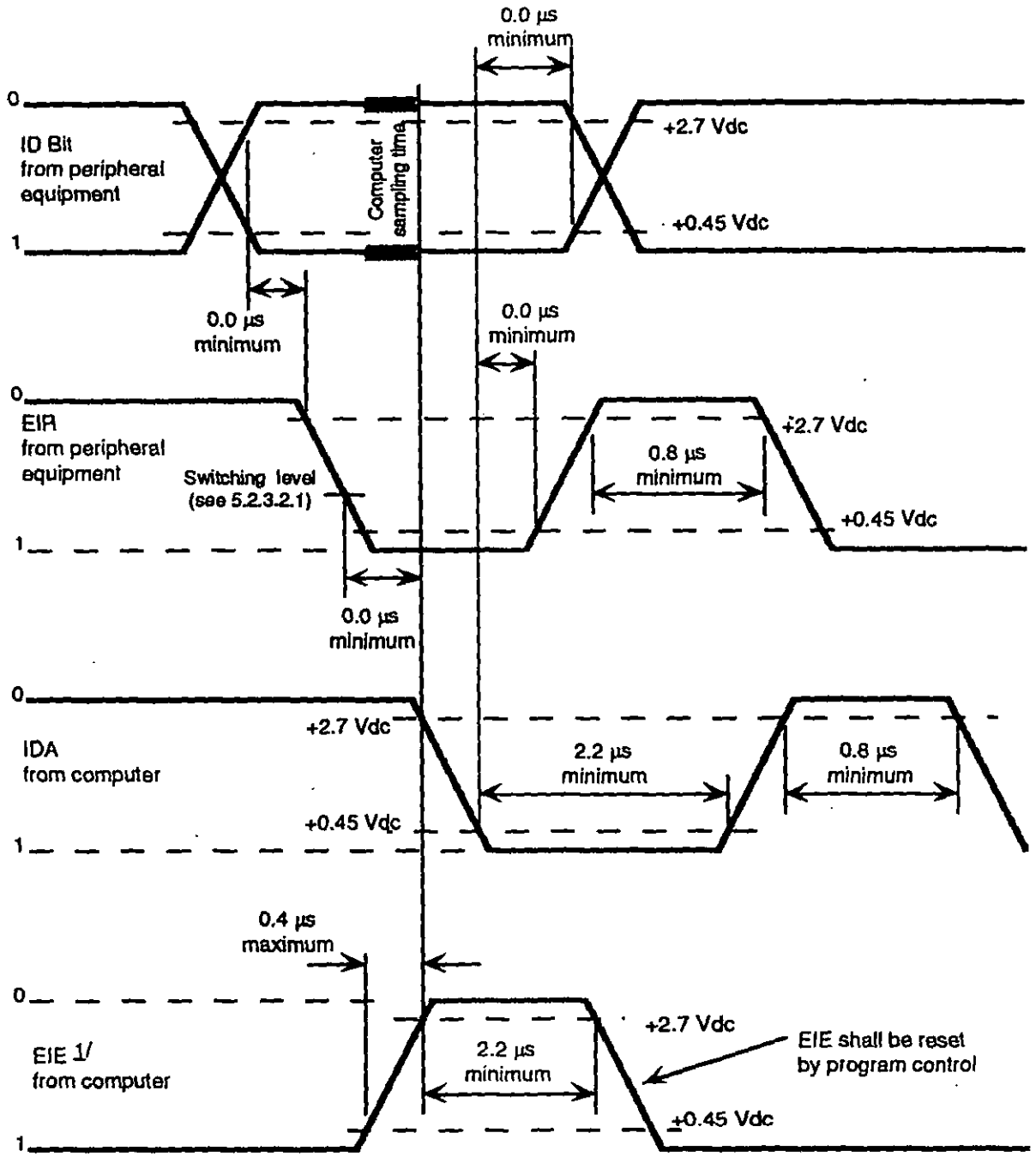


FIGURE 14. Type C input data timing.



1/ EIE signal not provided by some computers.

FIGURE 15. Type C external interrupt timing.

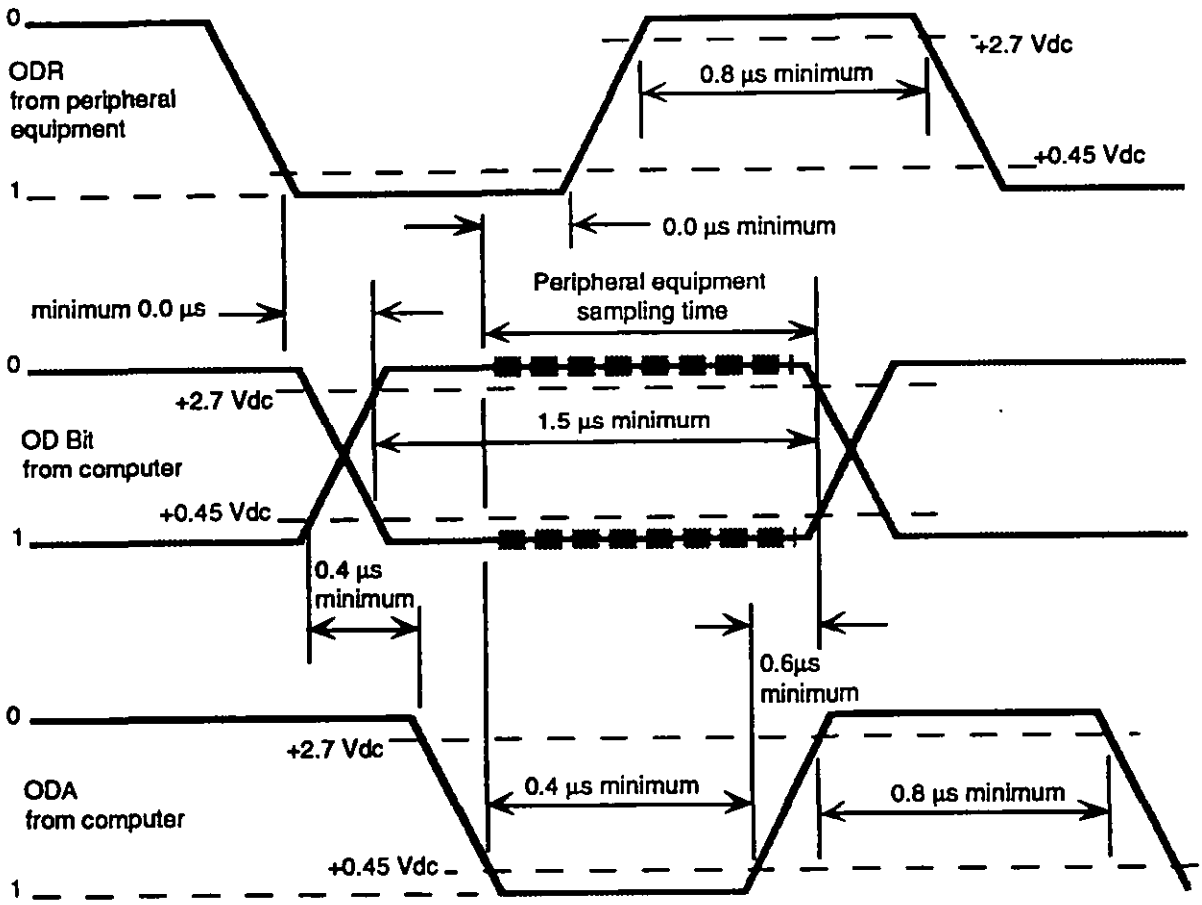
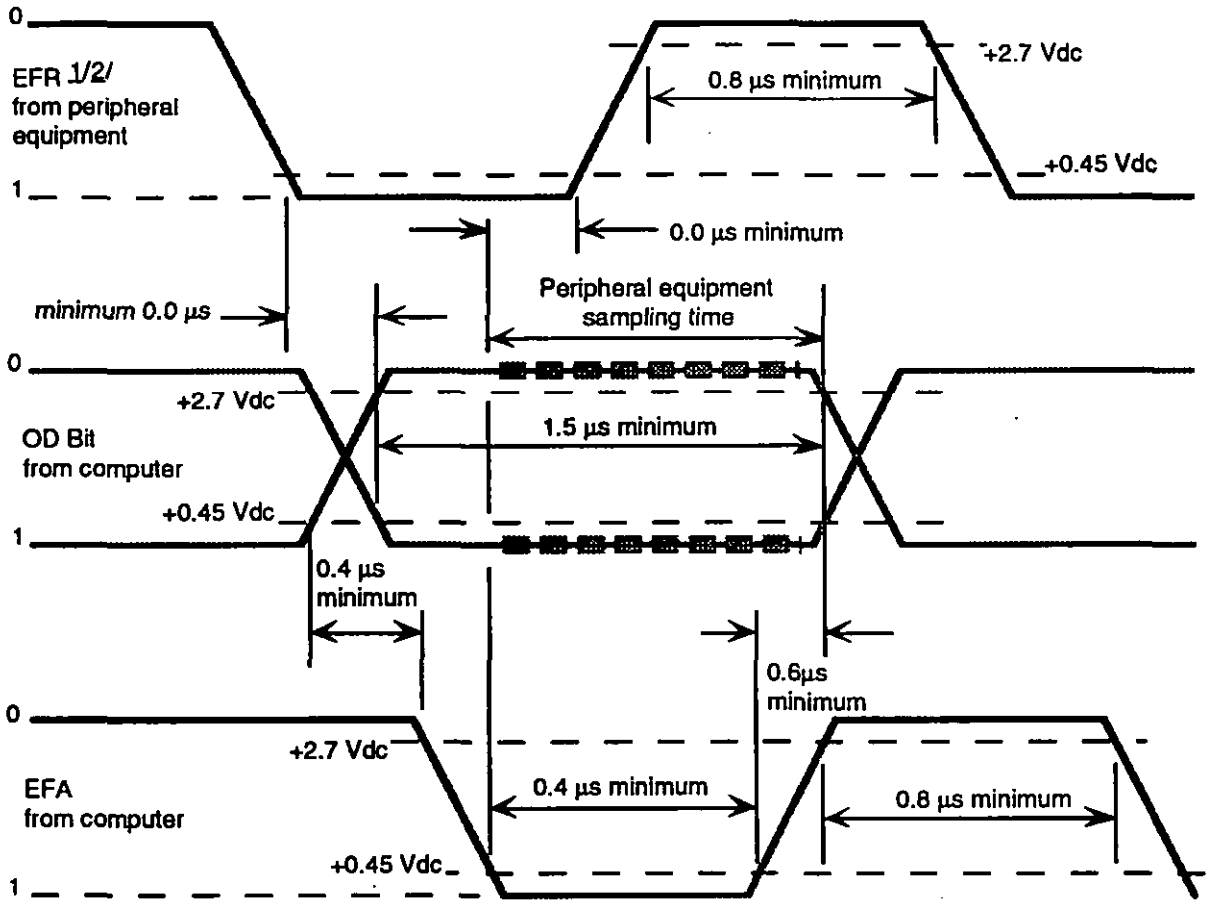


FIGURE 16. Type H output data timing.



1/ EFR not used for forced EF.
2/ When the EFR is not provided by the peripheral then forced EF shall be used.

FIGURE 17. Type H external function timing.

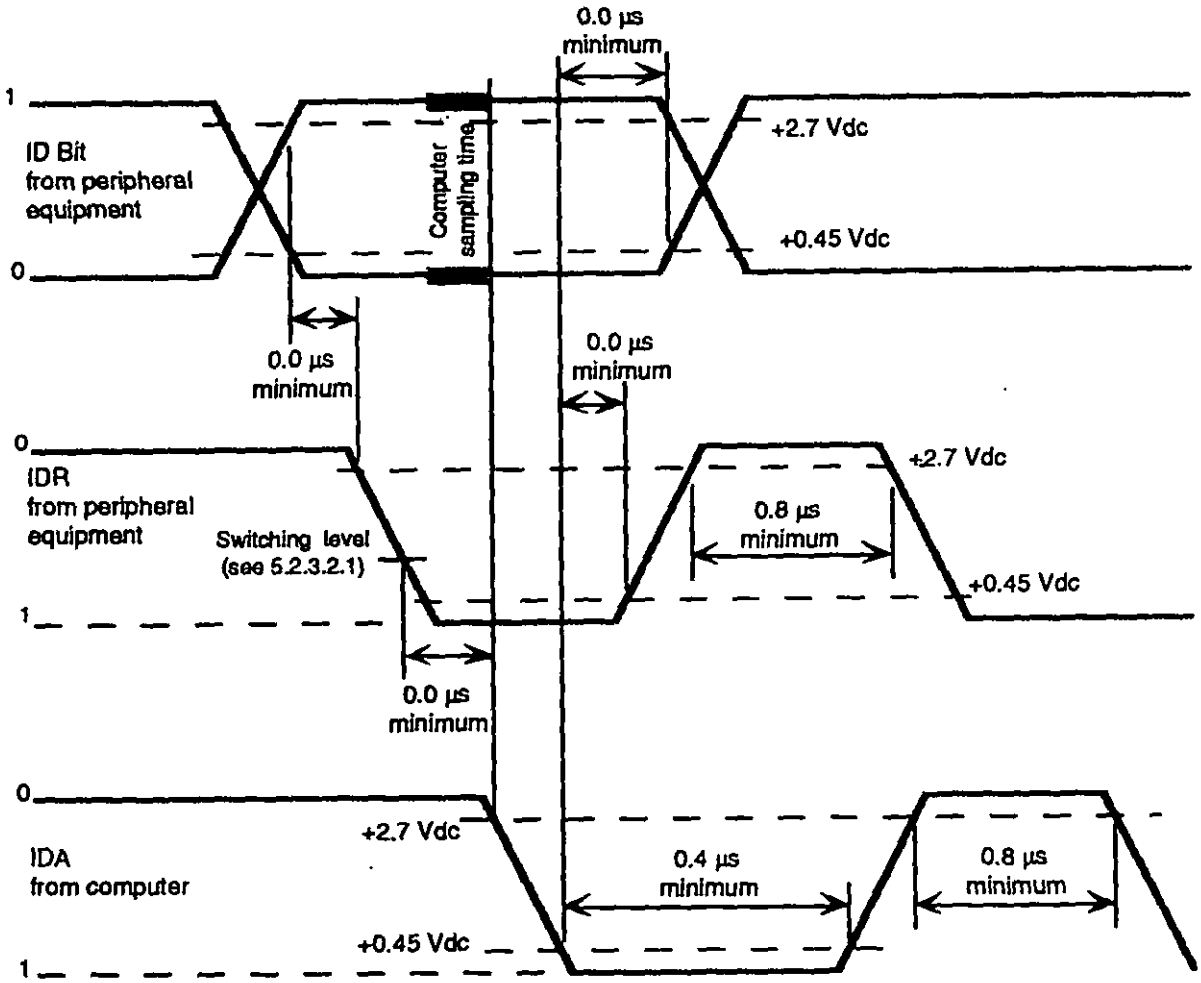
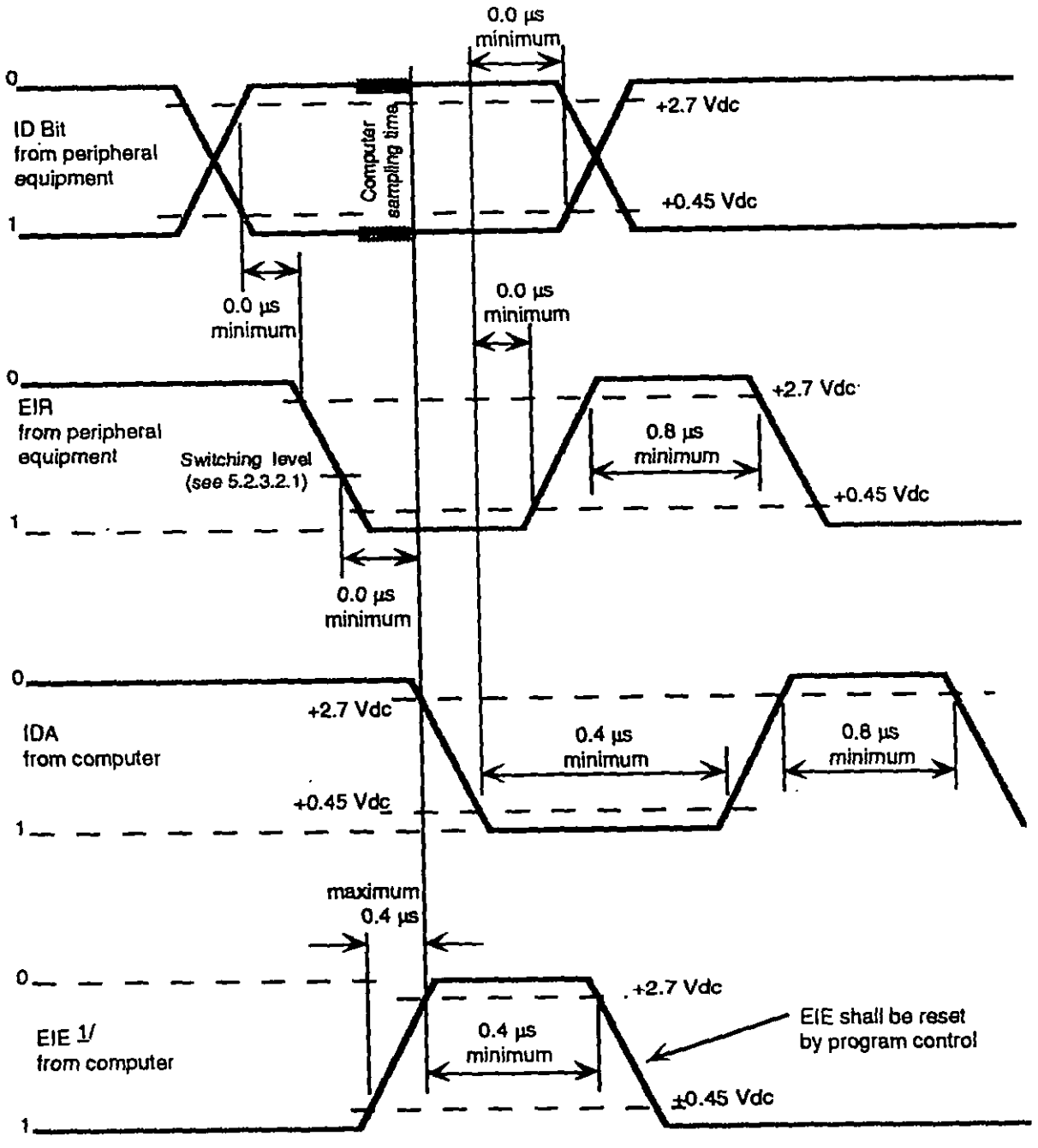


FIGURE 18. Type H input data timing.



1/ EIE signal not provided by some computers.

FIGURE 19. Type H external interrupt timing.

Control Bits			
		Synchronization Bit	
3rd	2nd	1st	
0	0	1	NO INFORMATION REQUESTED
0	1	1	INPUT DATA REQUEST
1	0	1	EXTERNAL INTERRUPT REQUEST
1	1	1	INPUT DATA & EXTERNAL INTERRUPT REQUEST

Input Request Control Frame (IRCF) (from Receiver)

Control Bits			
		Synchronization Bit	
3rd	2nd	1st	
0	0	1	NOT READY
0	1	1	INPUT DATA ENABLED
1	0	1	EXTERNAL INTERRUPT ENABLED
1	1	1	INPUT DATA & EXTERNAL INTERRUPT ENABLED

Input Enable Control Frame (IECF) (to Receiver)

FIGURE 20. Type D control frames on an input channel.

Control Bits			
		Synchronization Bit	
3rd	2nd	1st	
0	0	1	NOT READY
0	1	1	OUTPUT DATA REQUEST
1	0	1	EXTERNAL FUNCTION REQUEST
1	1	1	OUTPUT DATA & EXTERNAL FUNCTION REQUEST

Output Request Control Frame (ORCF) (to Transmitter)

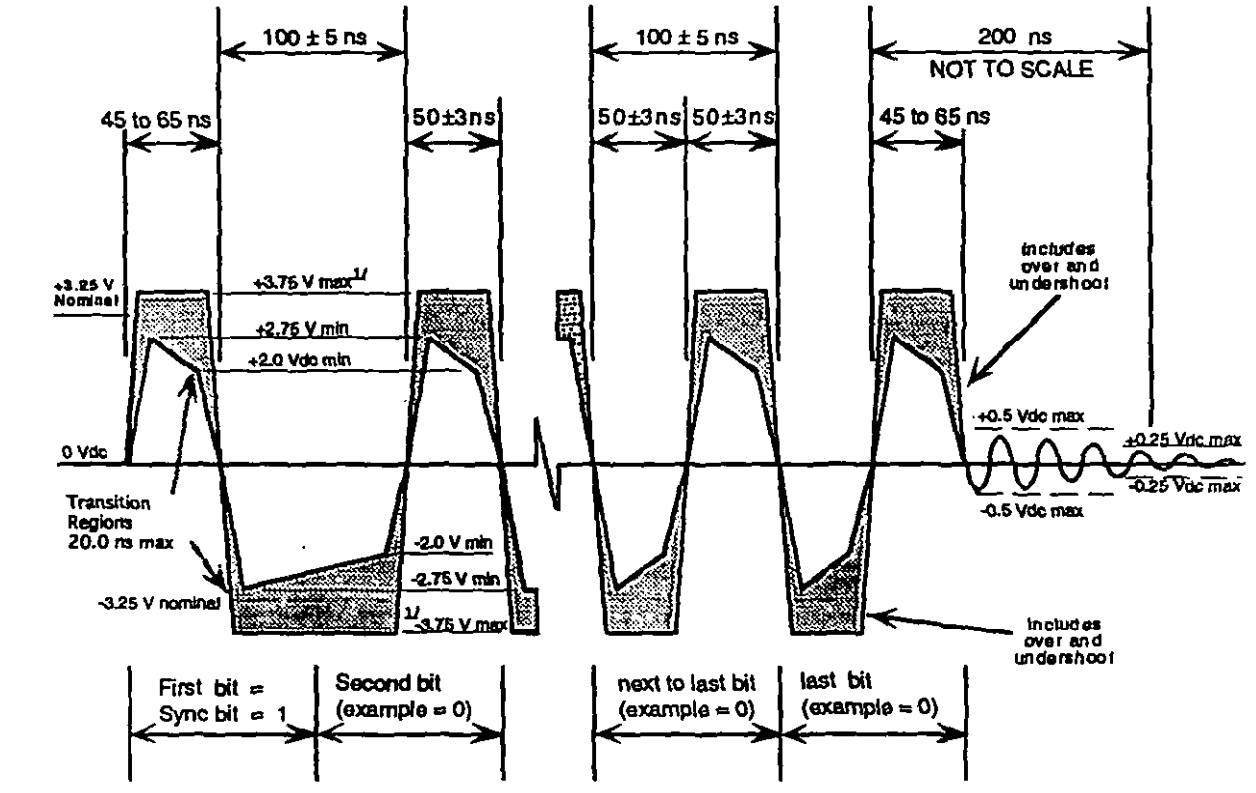
Control Bits			
		Synchronization Bit	
3rd	2nd	1st	
0	0	1	NO INFORMATION
0	1	1	OUTPUT DATA ENABLE
1	0	1	EXTERNAL FUNCTION ENABLE
1	1	1	OUTPUT DATA & EXTERNAL FUNCTION ENABLE

Output Enable Control Frame (OECF) (from Transmitter)

FIGURE 21. Type D control frames on an output channel.

N^{th}		9^{th}	8^{th}	7^{th}	6^{th}	5^{th}	4^{th}	3^{rd}	2^{nd}	1^{st}
Bit X-1		Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0		Synchronization bit
Information bits *(X is normally the length of the computer word)*									Word identifier bit	

FIGURE 22. Type D data word format.



1/ The absolute values of these two levels shall be within 10 percent of each other.

FIGURE 23. Type D output waveform envelope.

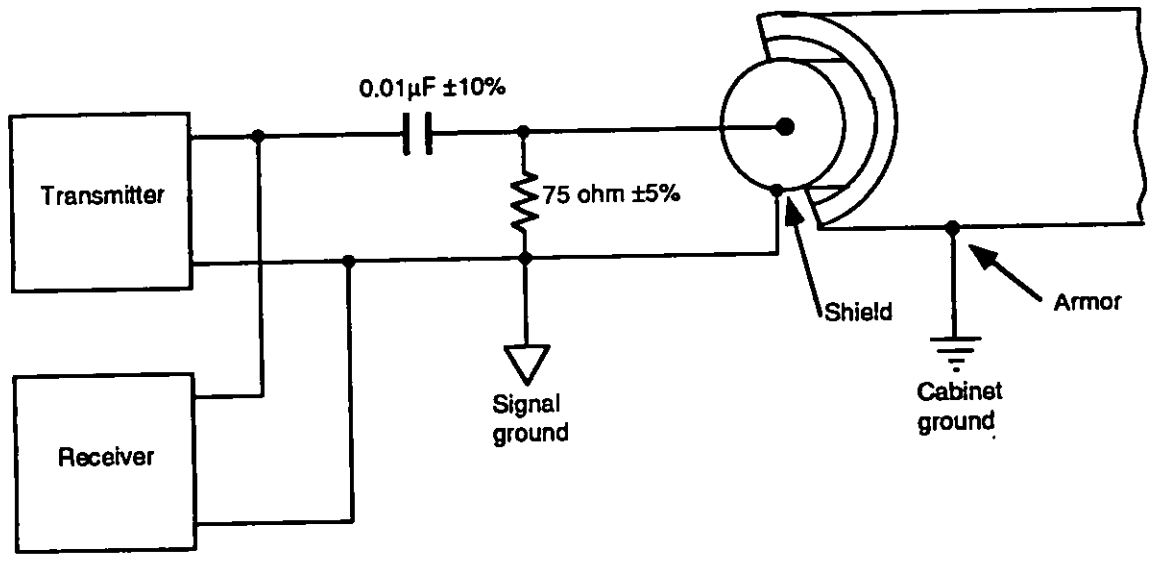
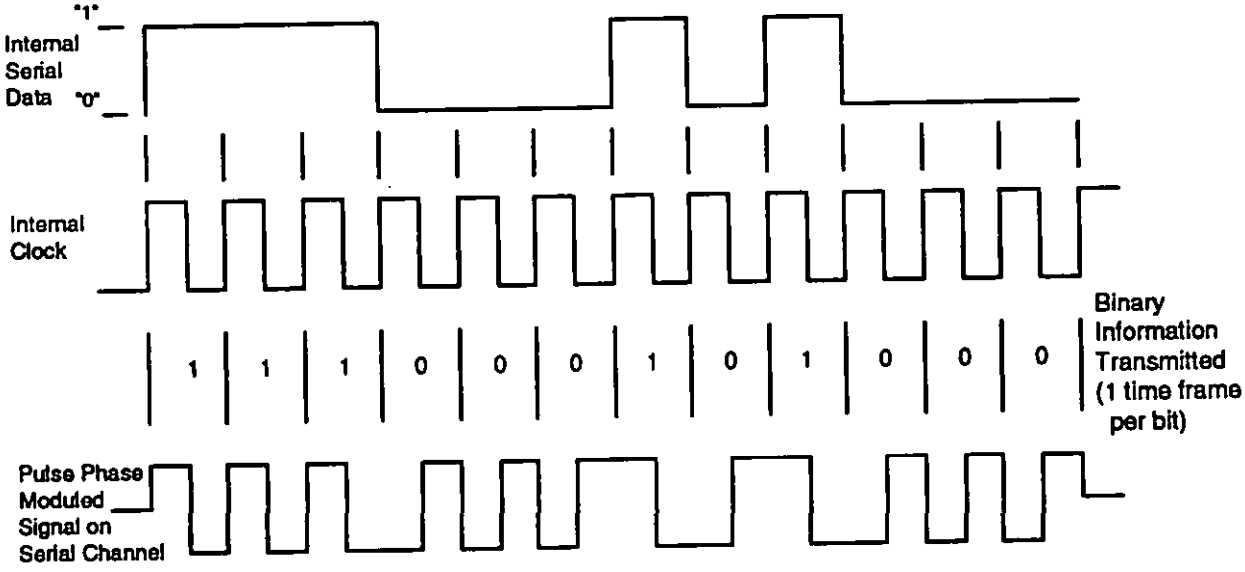


FIGURE 24. Type D interface termination.



The pulse phase modulated signal is the exclusive NOR combination of the data signal and the clock signal.

FIGURE 25. Type D pulse phase modulated signal.

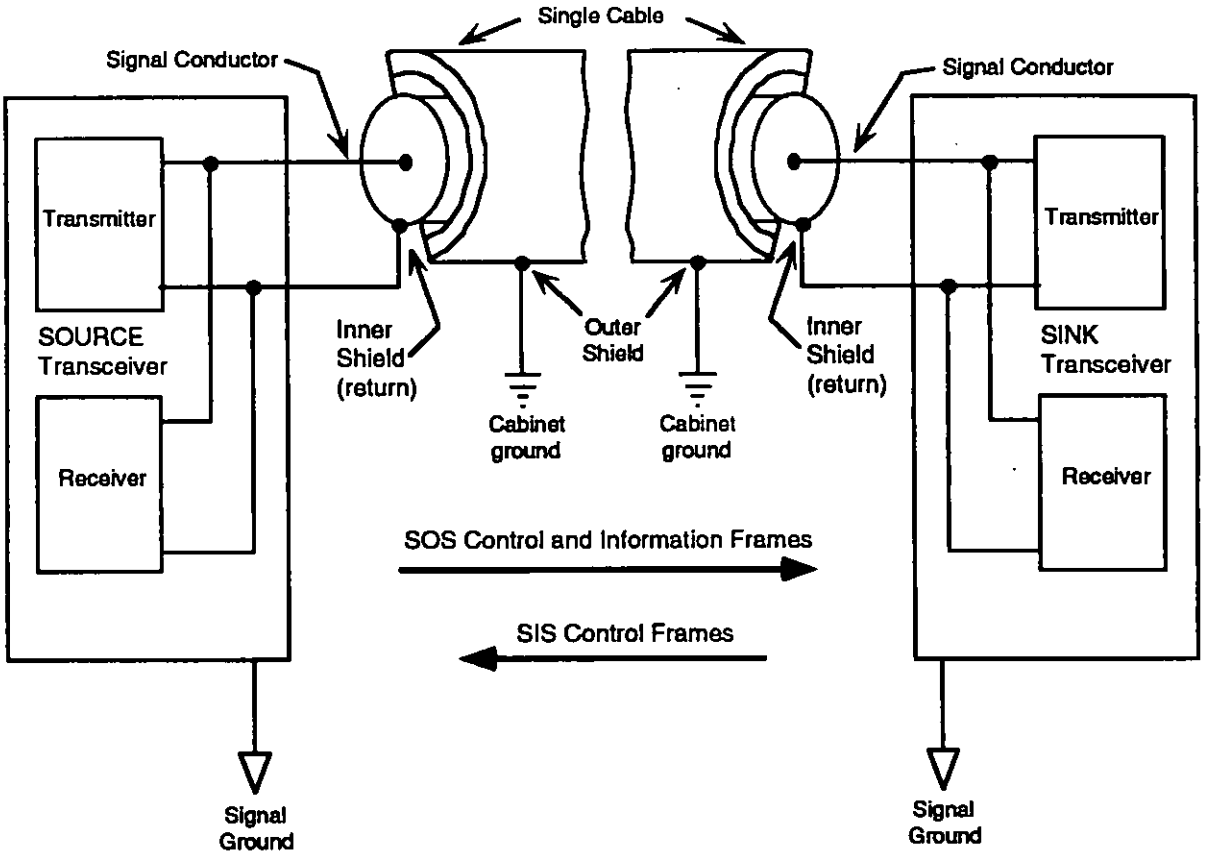


FIGURE 26. Type E source to sink interconnection diagram.

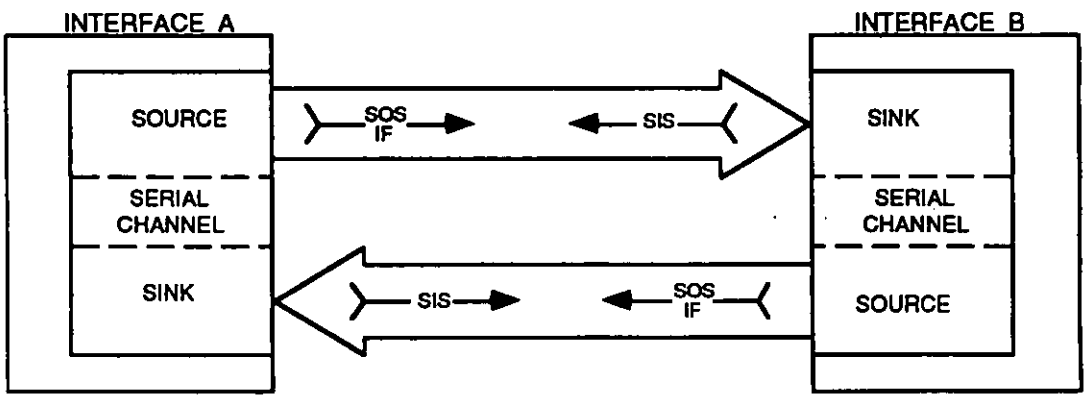


FIGURE 27. Type E interface signal flow diagram.

1st bit (Sync)	2nd bit (Data)	3rd bit (C/I)	4th bit * (SOS ID)	SOURCE OUTPUT BUFFER STATUS
1	0	0	0	Source has no Information Word(s) to send.
1	1	0	0	Source has Data Word(s) (but no Command/Interrupt Word) to send.
1	0	1	0	Source has a Command/Interrupt Word (but no Data Word(s)) to send.
1	1	1	0	Source has both Data Word(s) and a Command/Interrupt Word to send.

* Earlier revisions of this standard defined this bit as being "Reserved."

FIGURE 28. Type E SOS control frame contents.

1st bit (Sync)	2nd bit (Data)	3rd bit (C/I)	4th bit * (SIS ID)	SINK INPUT BUFFER STATUS
1	0	0	1	Sink is not ready to accept any Information Word(s).
1	1	0	1	Sink is only ready to accept Data Word(s).
1	0	1	1	Sink is only ready to accept Command/Interrupt Word.
1	1	1	1	Sink is ready to accept either Data Word(s) or a Command Interrupt Word.

* Earlier revisions of this standard defined this bit as being "Reserved."

FIGURE 29. Type E SIS control frame contents.

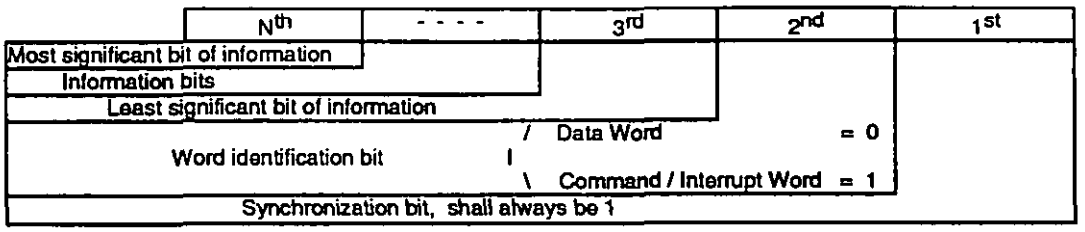
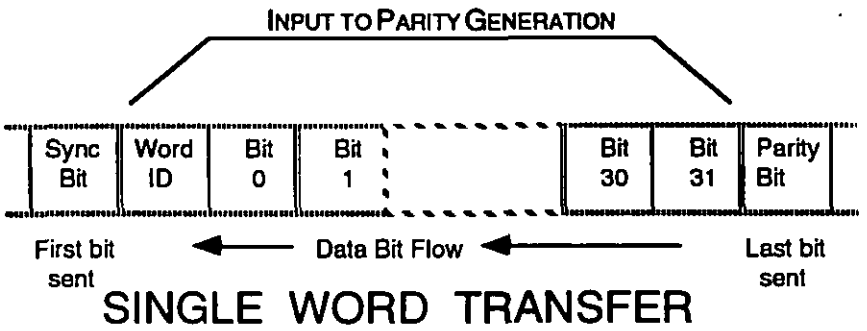


FIGURE 30. Type E information frame contents.



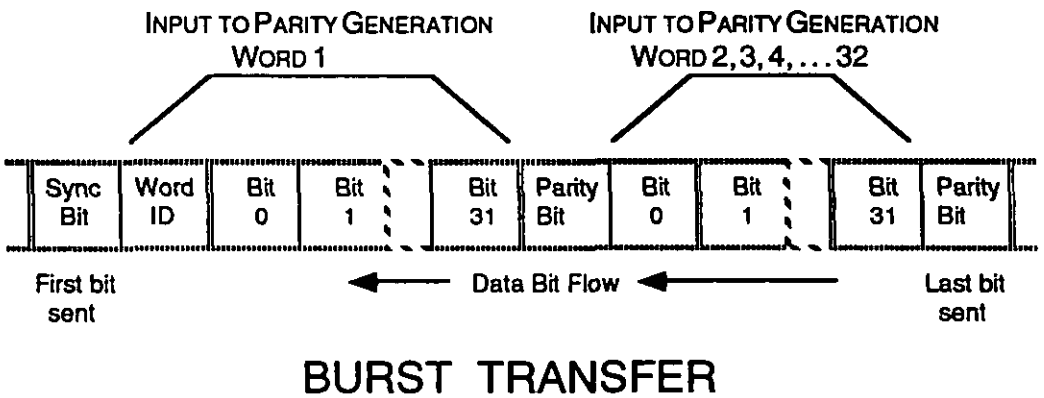


FIGURE 31. Type E parity bit generation.

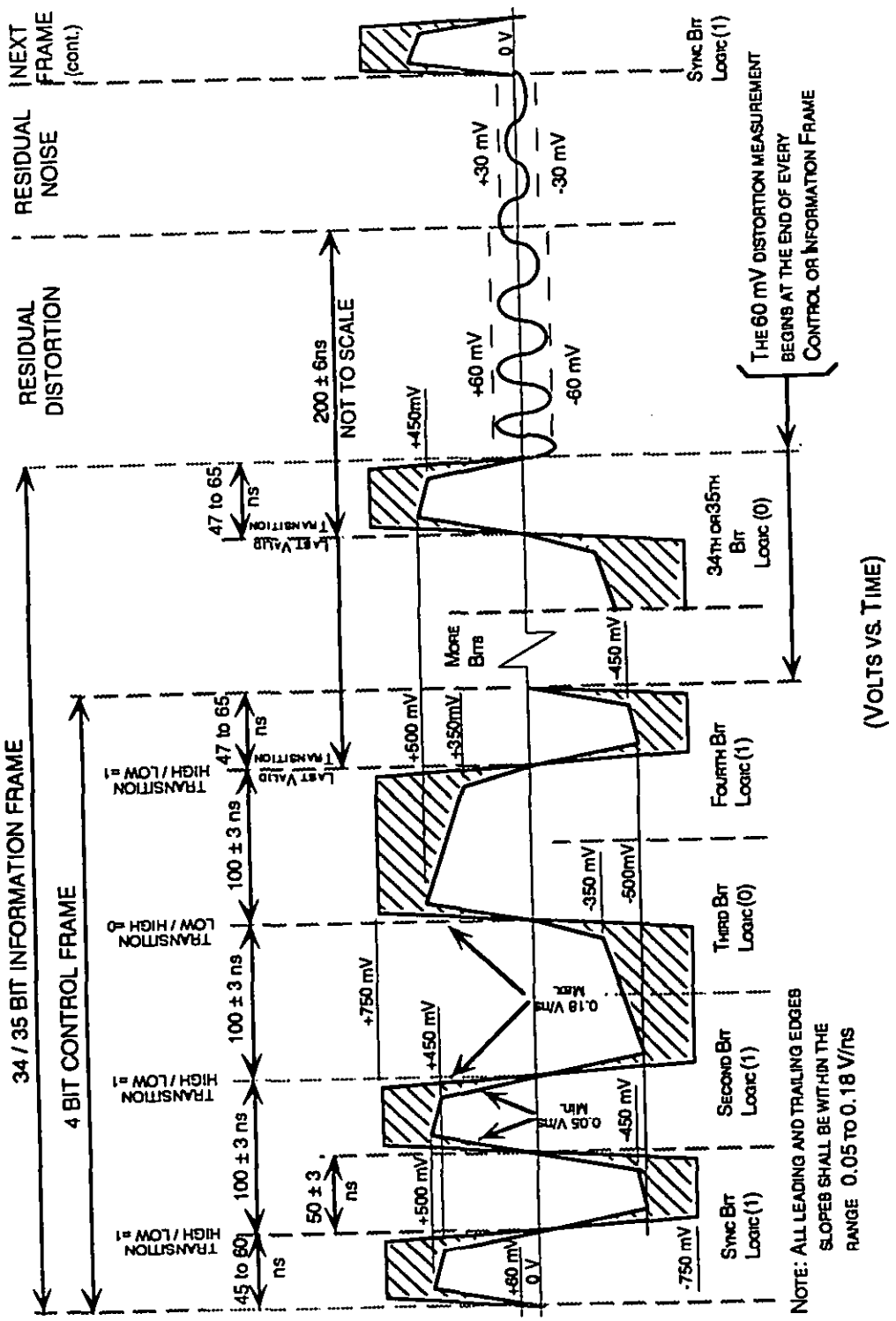


FIGURE 32. Type E output waveform envelope.

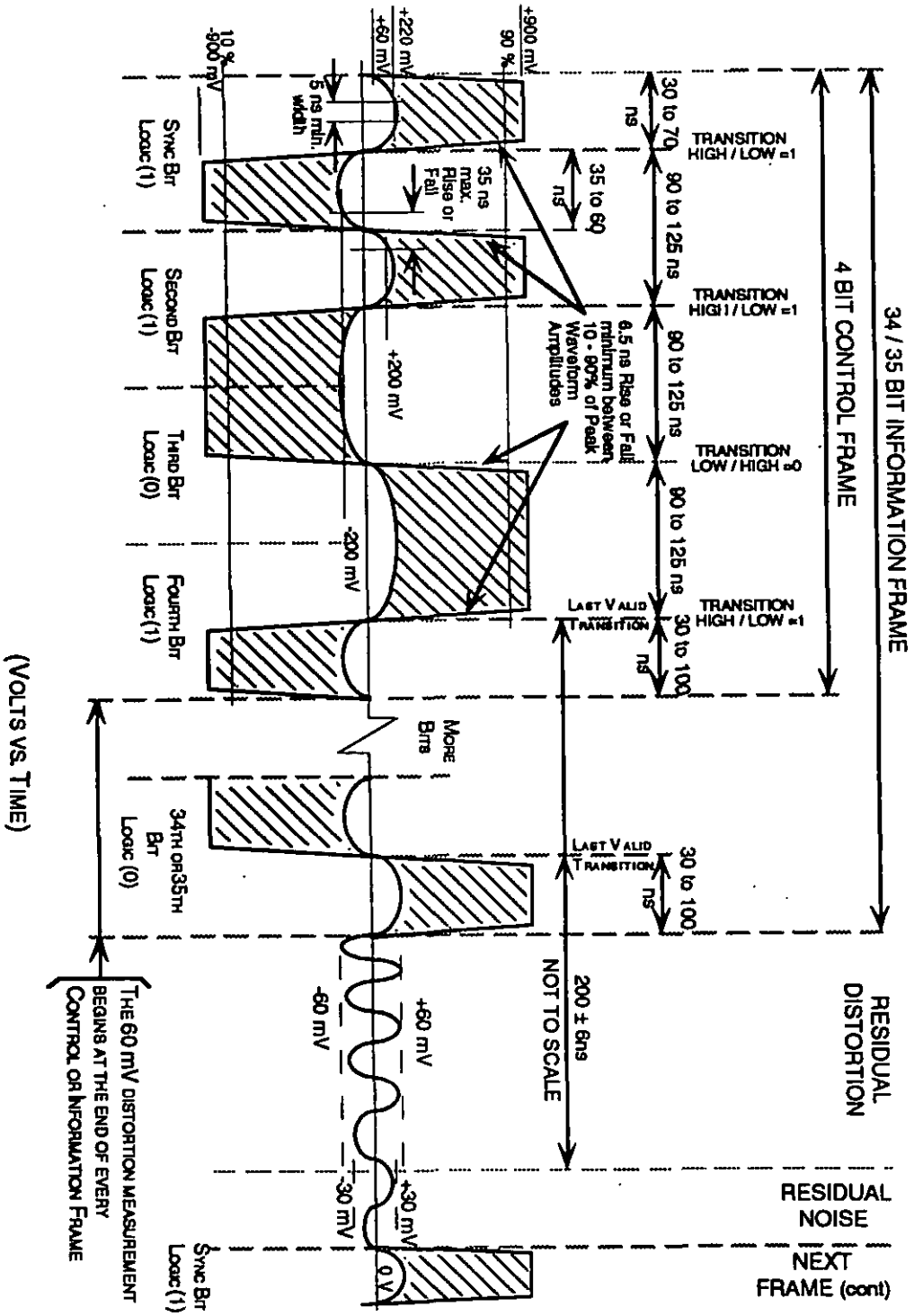


FIGURE 33. Type E input waveform envelope

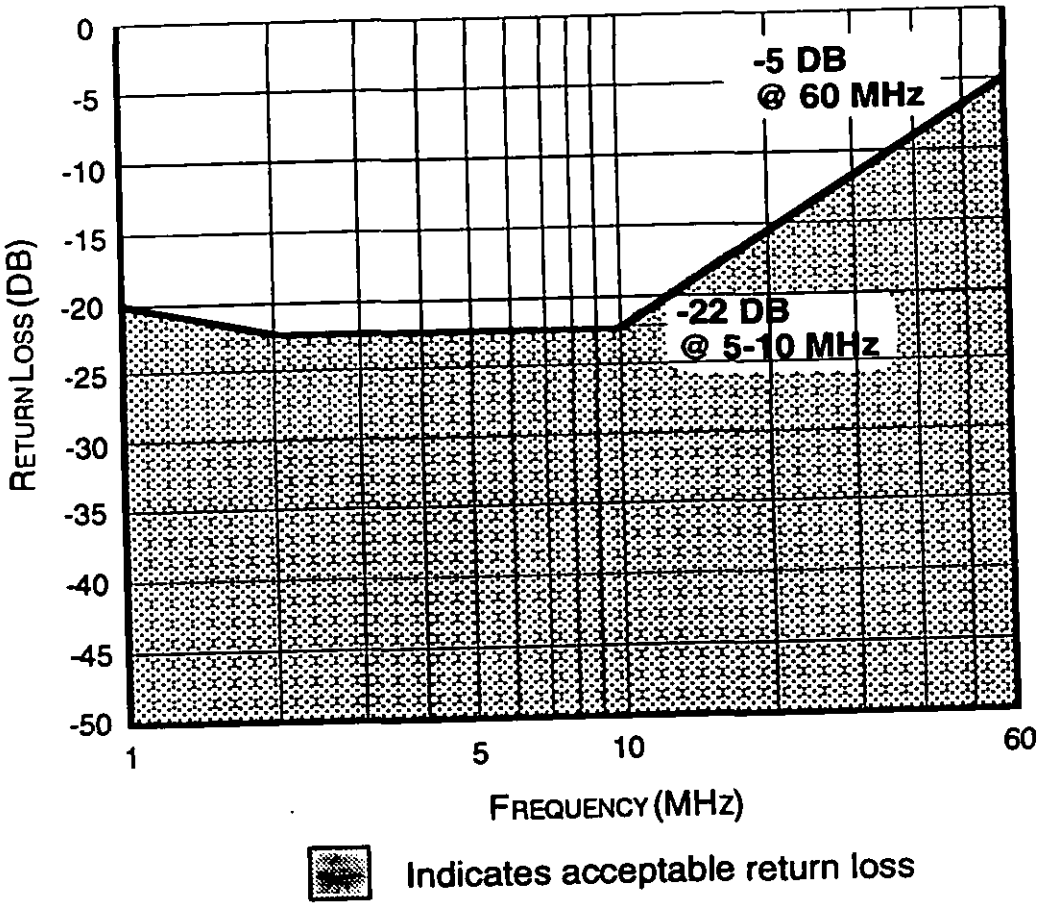


FIGURE 34. Type E sink return loss profile

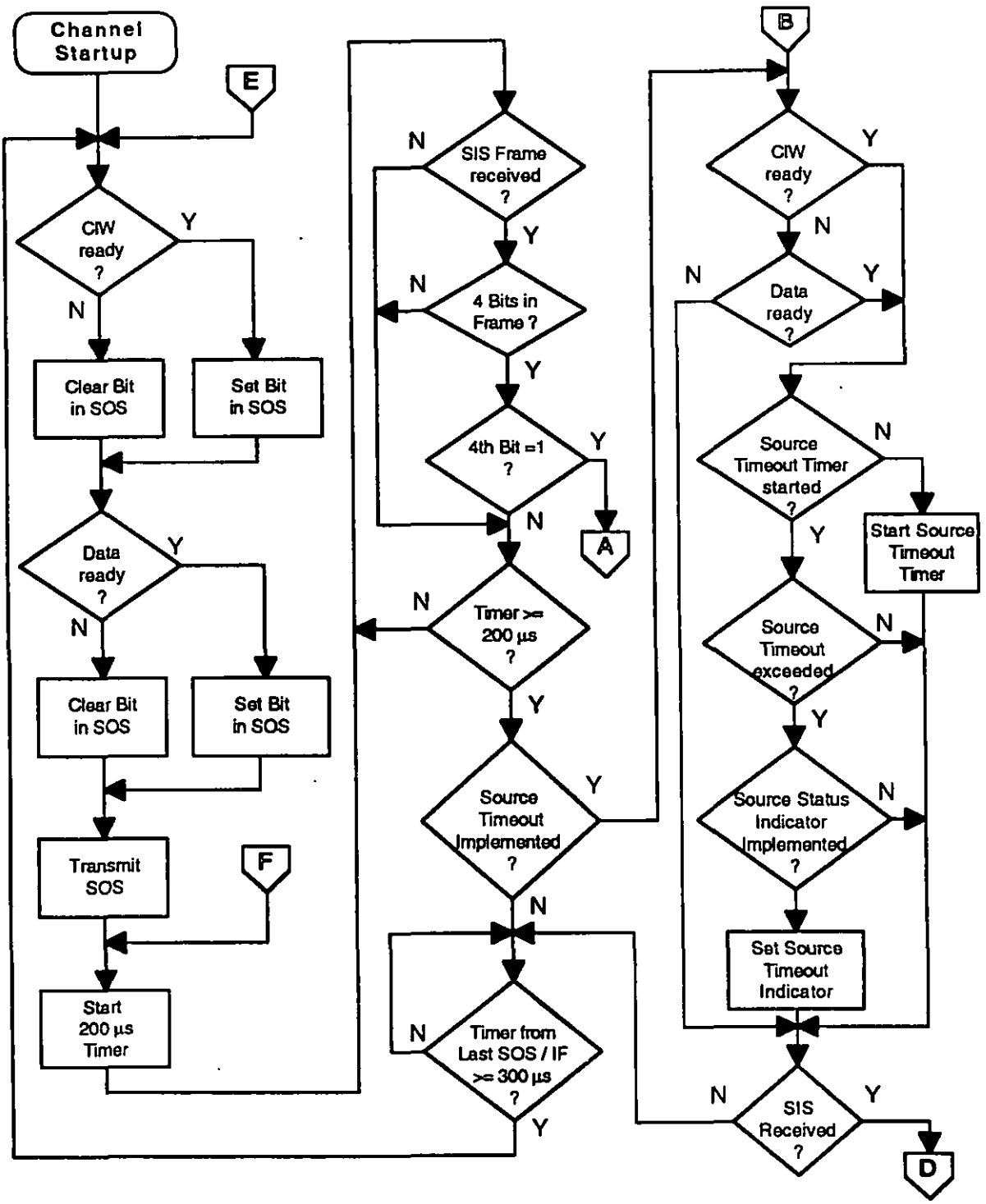


FIGURE 35. Source flow diagram (Sheet 1 of 2).

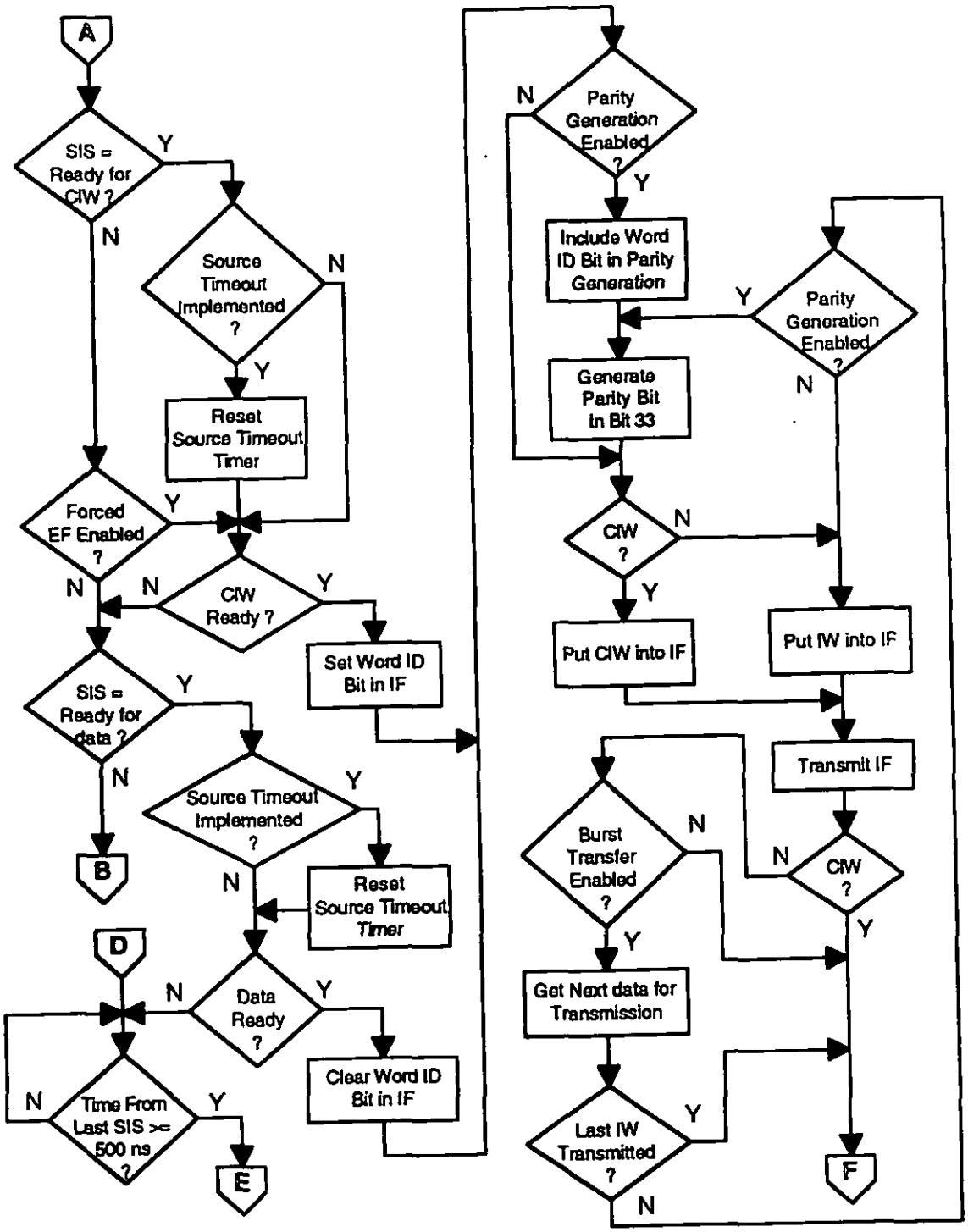


FIGURE 35. Source flow diagram (Sheet 2 of 2).

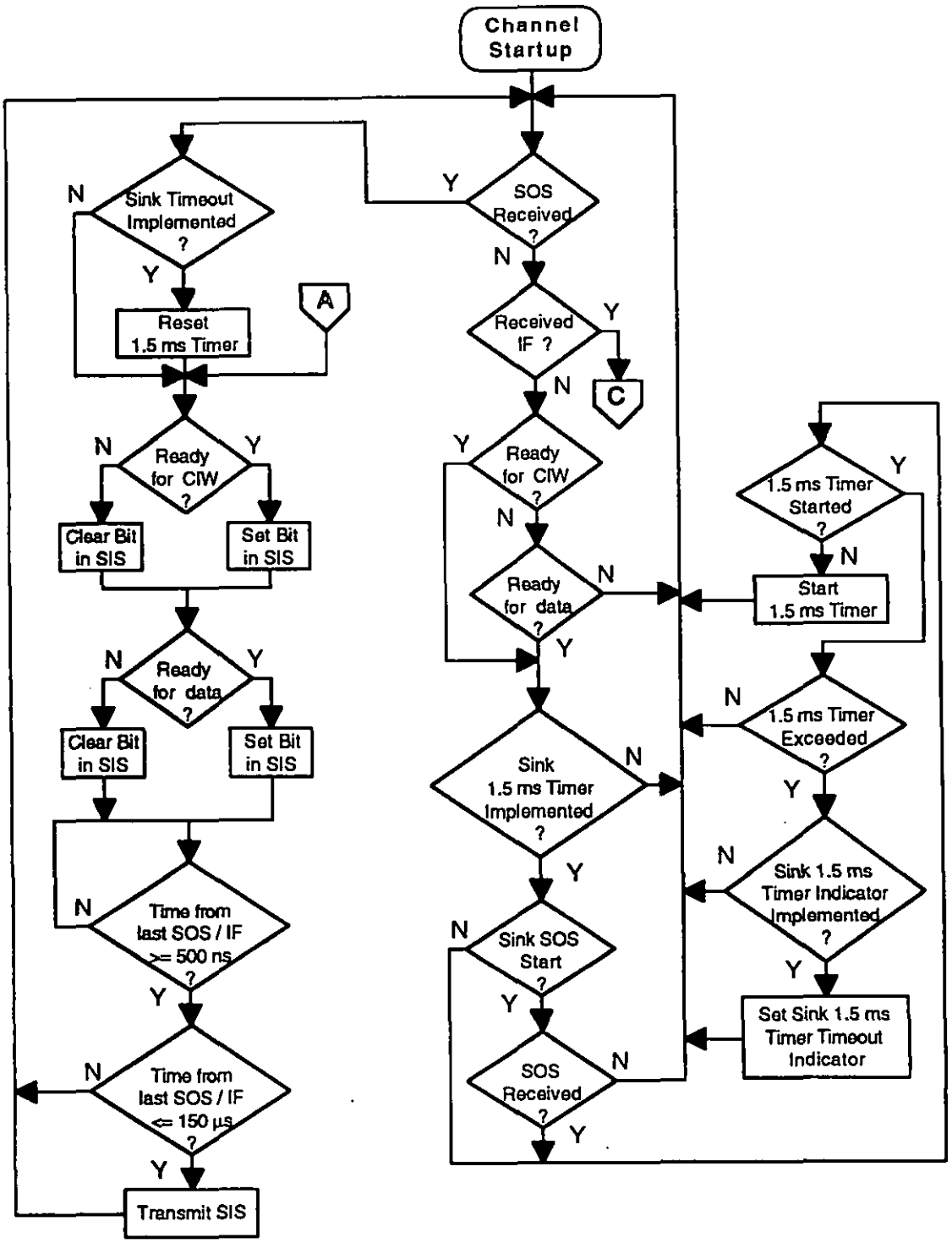


FIGURE 36. Sink flow diagram (Sheet 1 of 2).

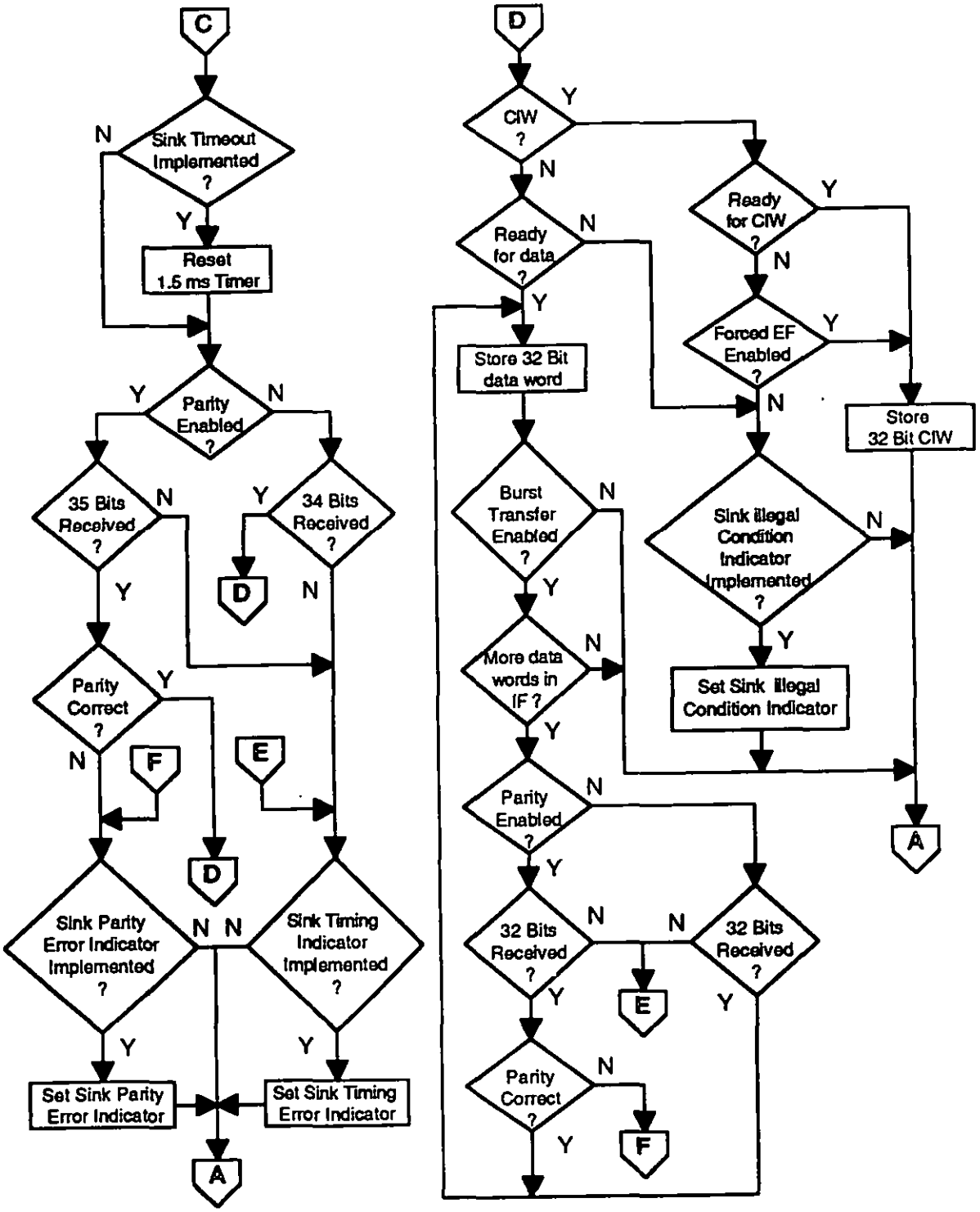


FIGURE 36. Sink flow diagram (Sheet 2 of 2).

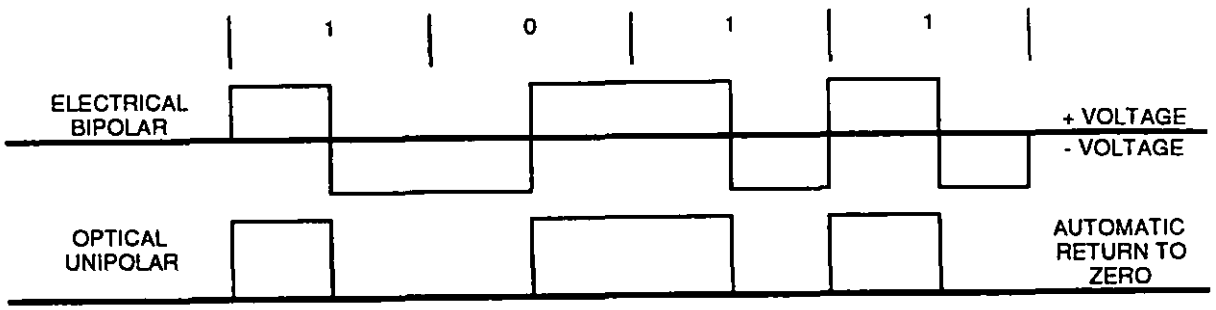
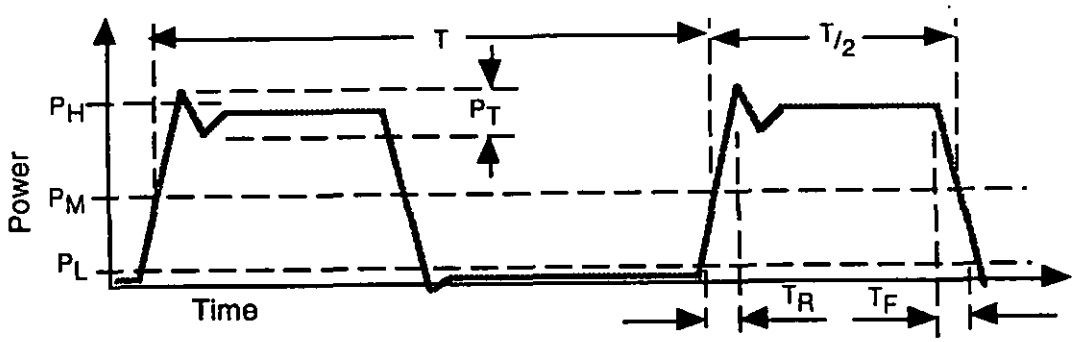


FIGURE 37. Type J waveform modulation



PARAMETER	PARMETER DEFINITION	T_x INTERFACE	R_x INTERFACE
P_H	The high-state optical power level.	-13 dBm to -7 dBm	-31 dBm to -8 dBm
P_L	The low-state optical power level threshold.	$(0.1)P_H$ max.	$(0.1)P_H$ max.
P_T	The peak-to-peak overshoot and undershoot for either rising or the failing edges.	$(0.15)P_H$ max.	$(0.15)P_H$ max.
P_M	The median optical power level.	$(0.5)(P_H - P_L)$	
T	The bit interval is 100 nanoseconds (nominal).	94 to 104 nanoseconds	
$T_{/2}$	Pulse width: Nominal value. First and last bits only.	44 to 56 nanoseconds 42 to 68 nanoseconds	
T_R, T_F	The10 to 90 % rise and fall times equals the time interval between $(0.1)(P_H-P_L) + P_L$ and $(0.9)(P_H-P_L) + P_L$	12 nanoseconds maximum	
$\lvert T_R - T_F \rvert$	Absloute value of the difference of the rise and fall times.	6 nanoseconds maximum	

FIGURE 38. Type J optical waveform

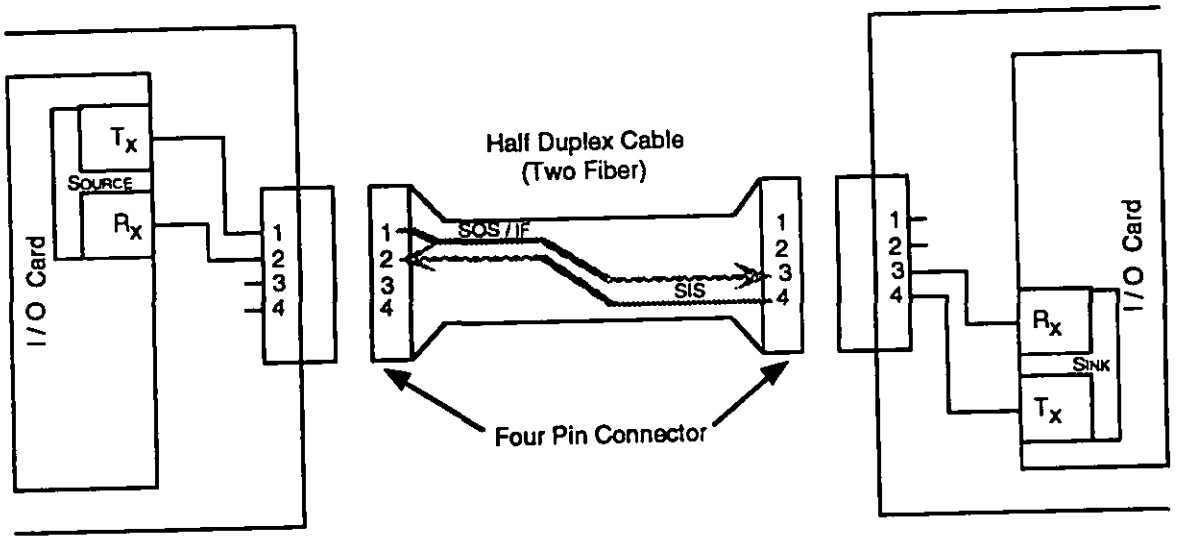


FIGURE 39. Type J half duplex interface

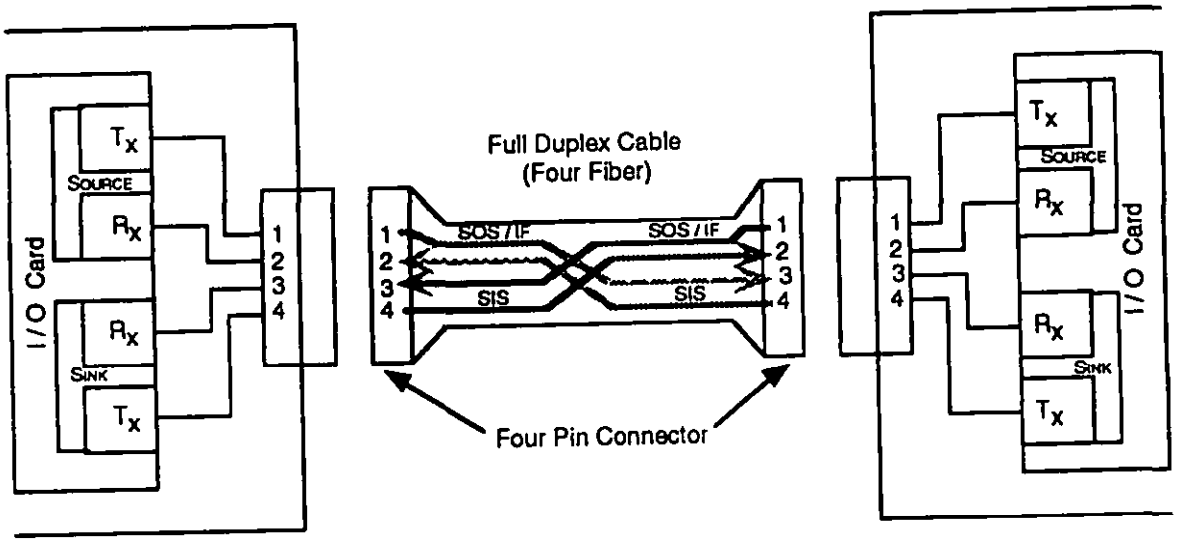


FIGURE 40. Type J full duplex interface

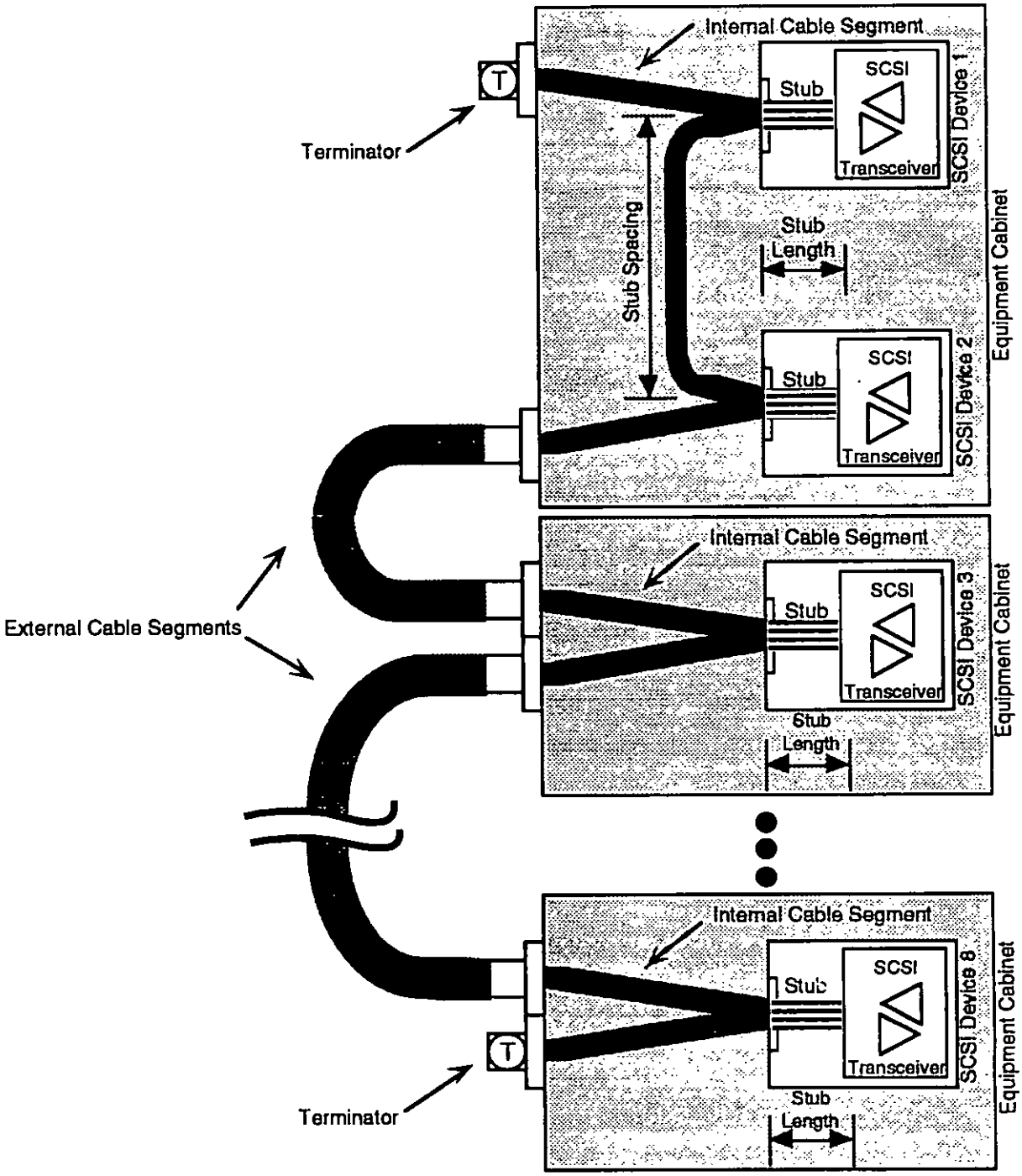


FIGURE 41. Type K cable diagram

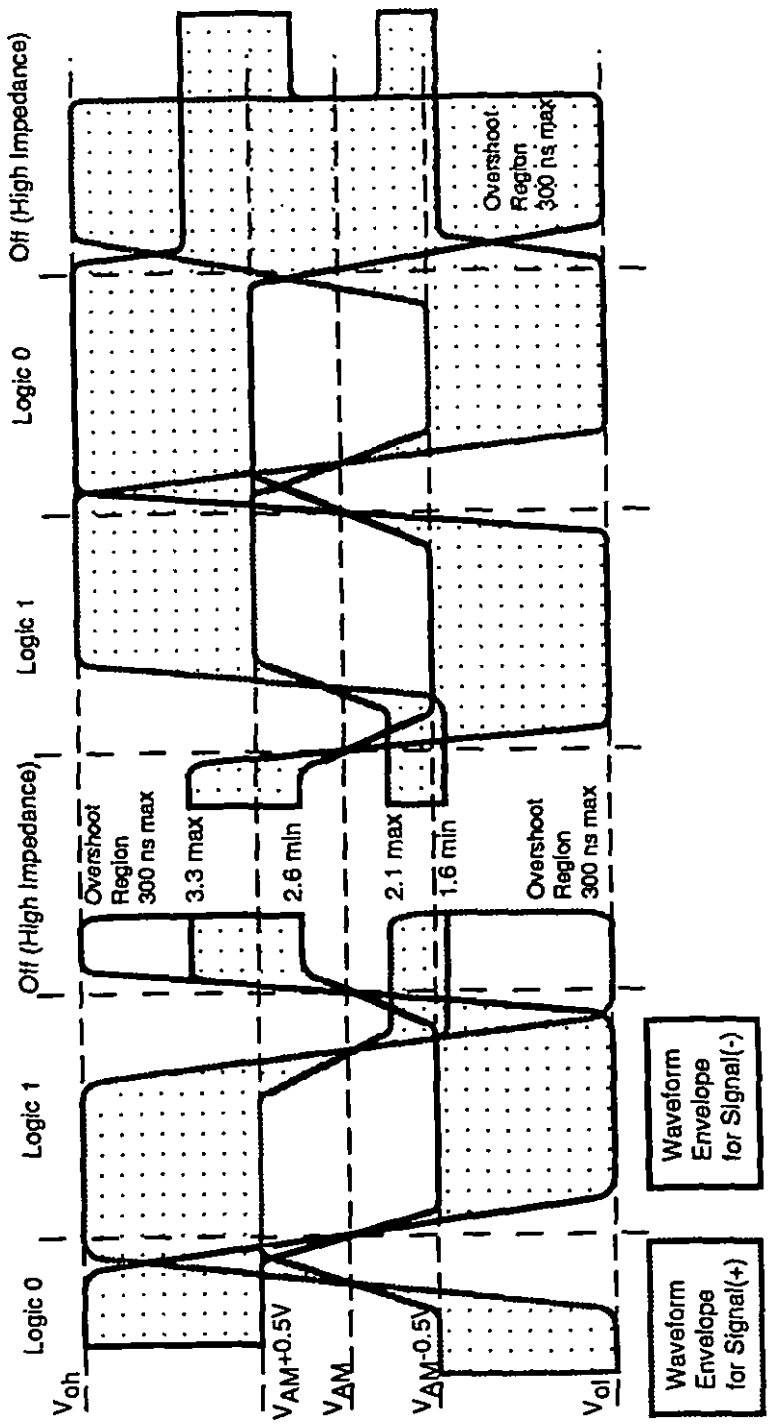


FIGURE 42. Type K SIGNAL(+) & SIGNAL(-) envelopes

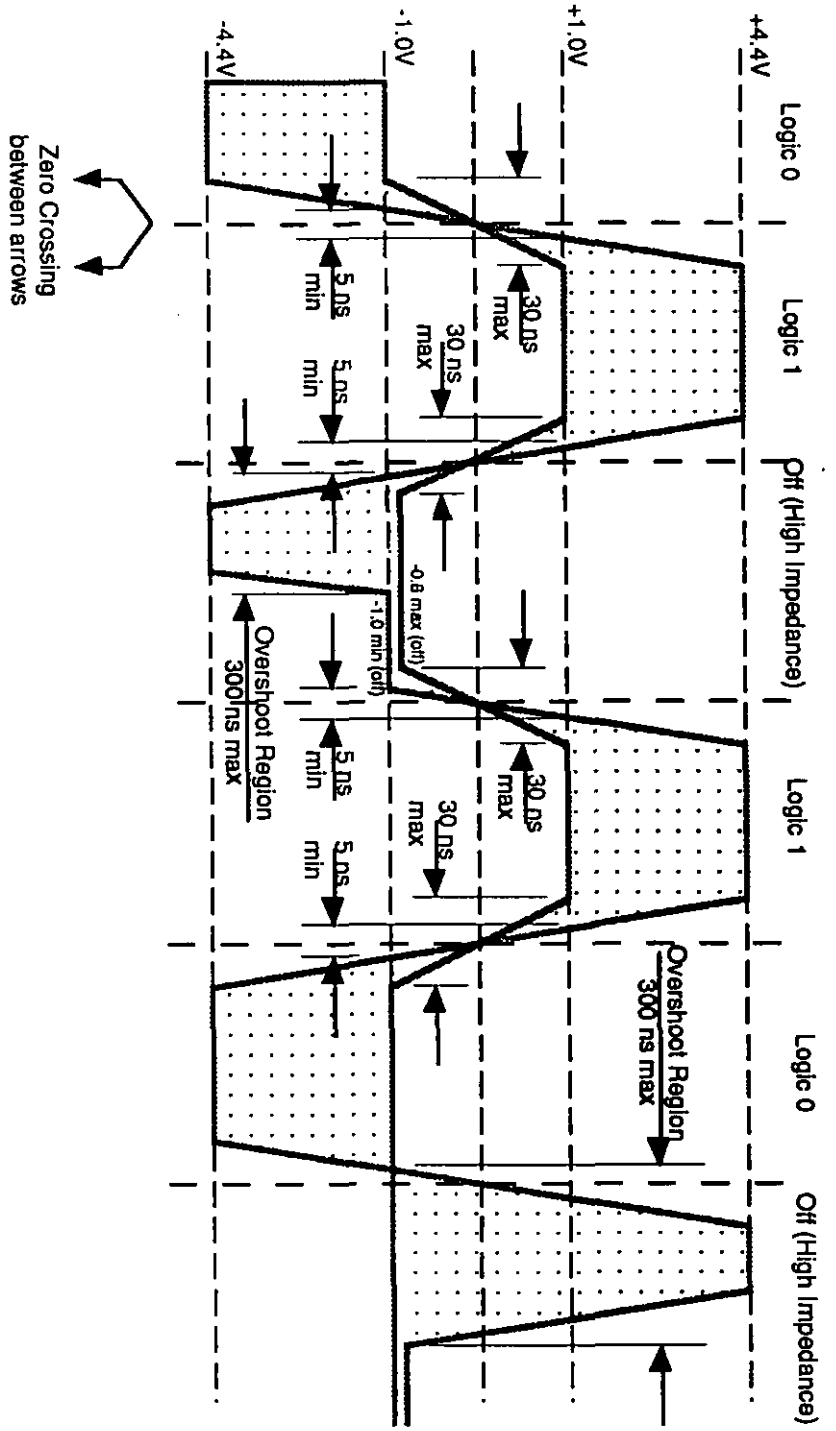


FIGURE 43. Type K composite waveform input parameters (volts vs. time)

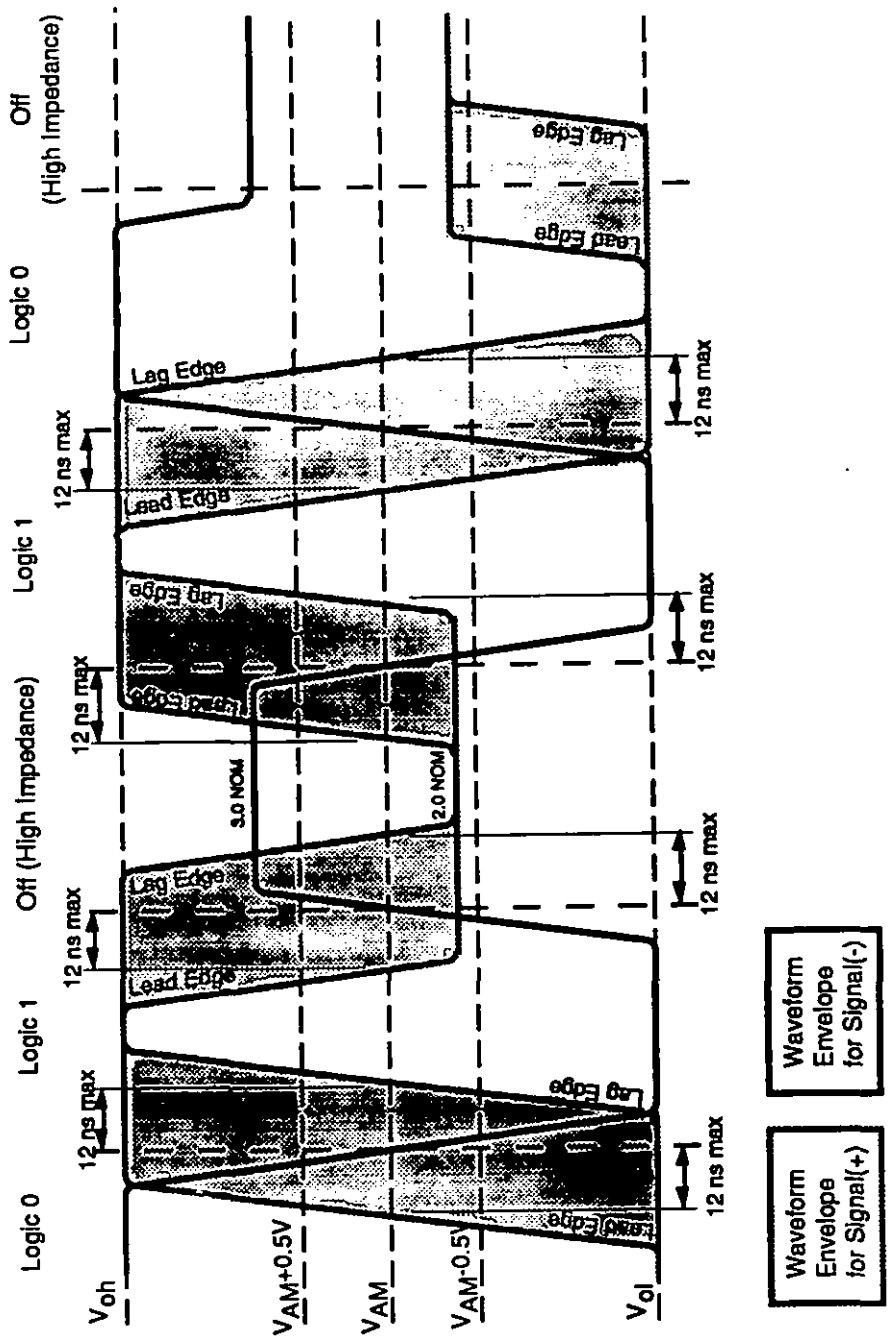


FIGURE 44. Type K SIGNAL(+) & SIGNAL(-) output parameters (volts vs. time)

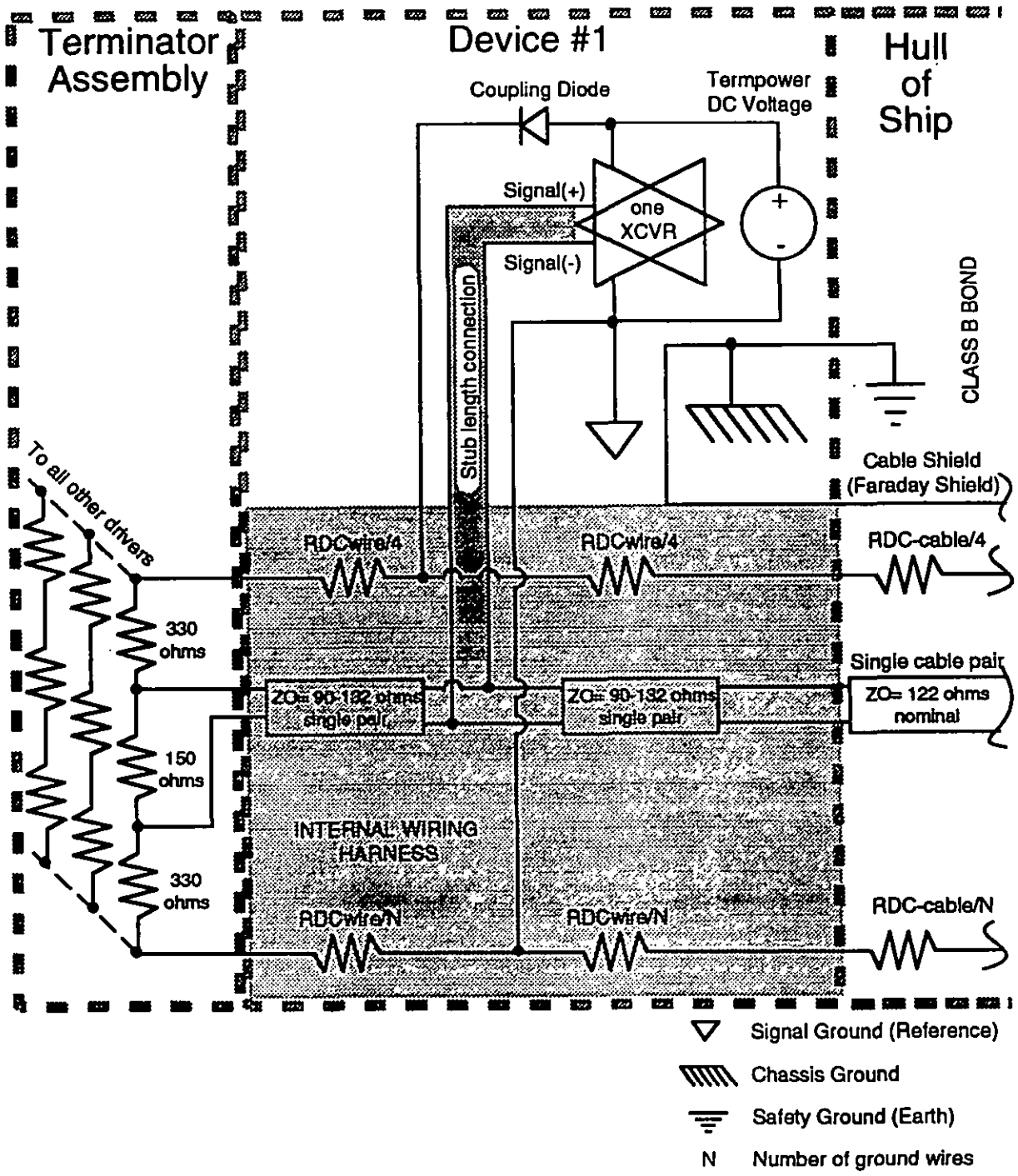


FIGURE 45. Type K multipoint interconnect diagram. (Sheet 1 of 2)

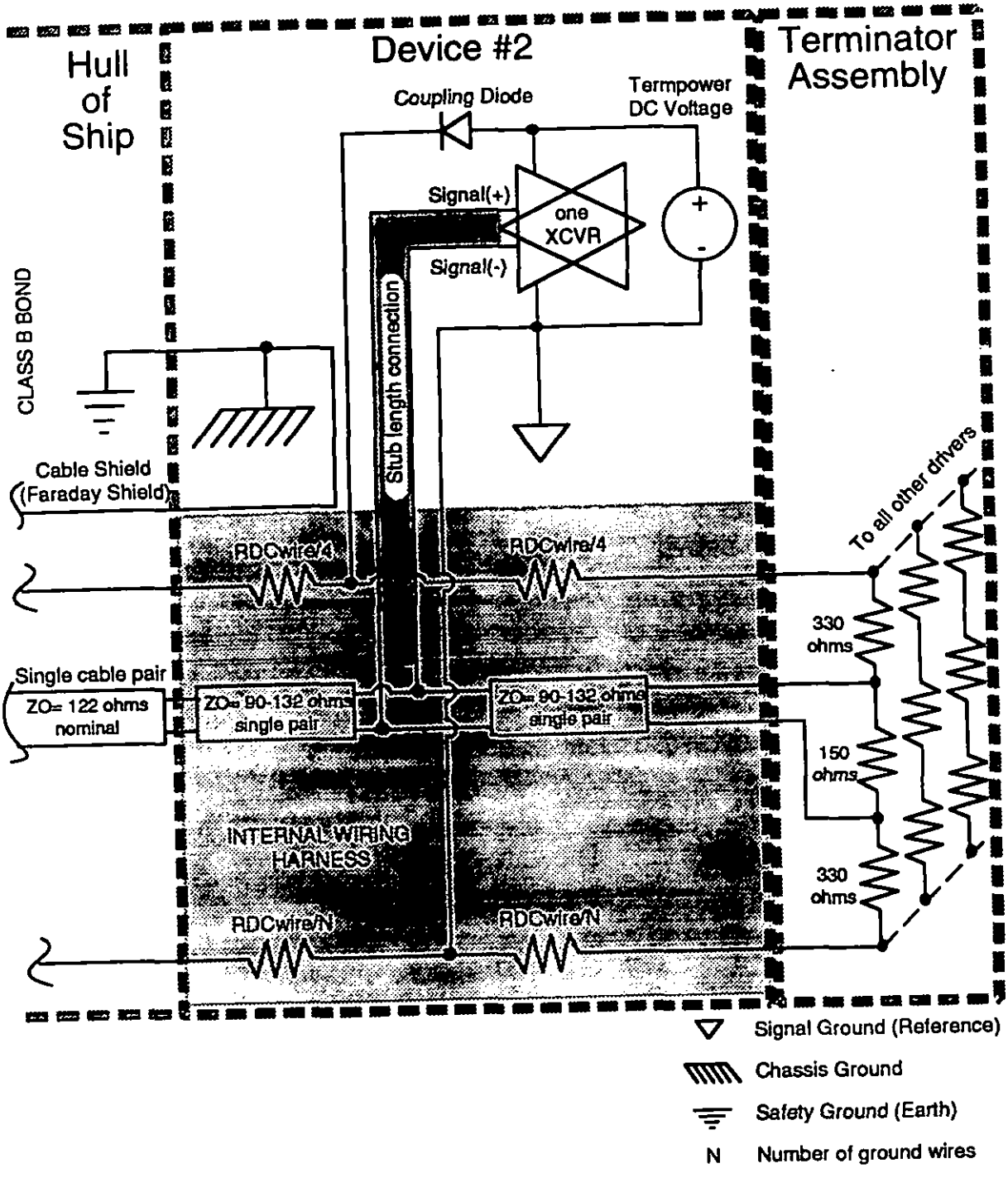


FIGURE 45. Type K multipoint interconnect diagram. (Sheet 2 of 2)

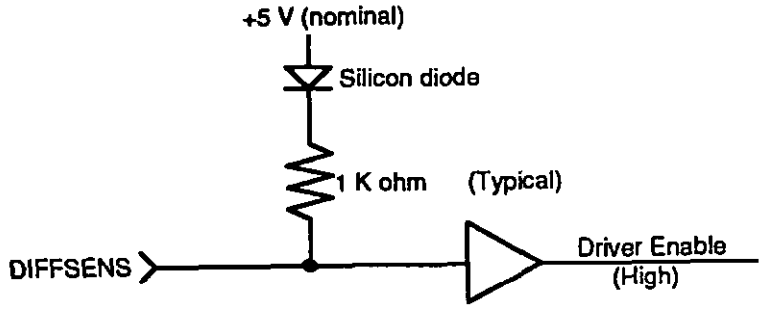
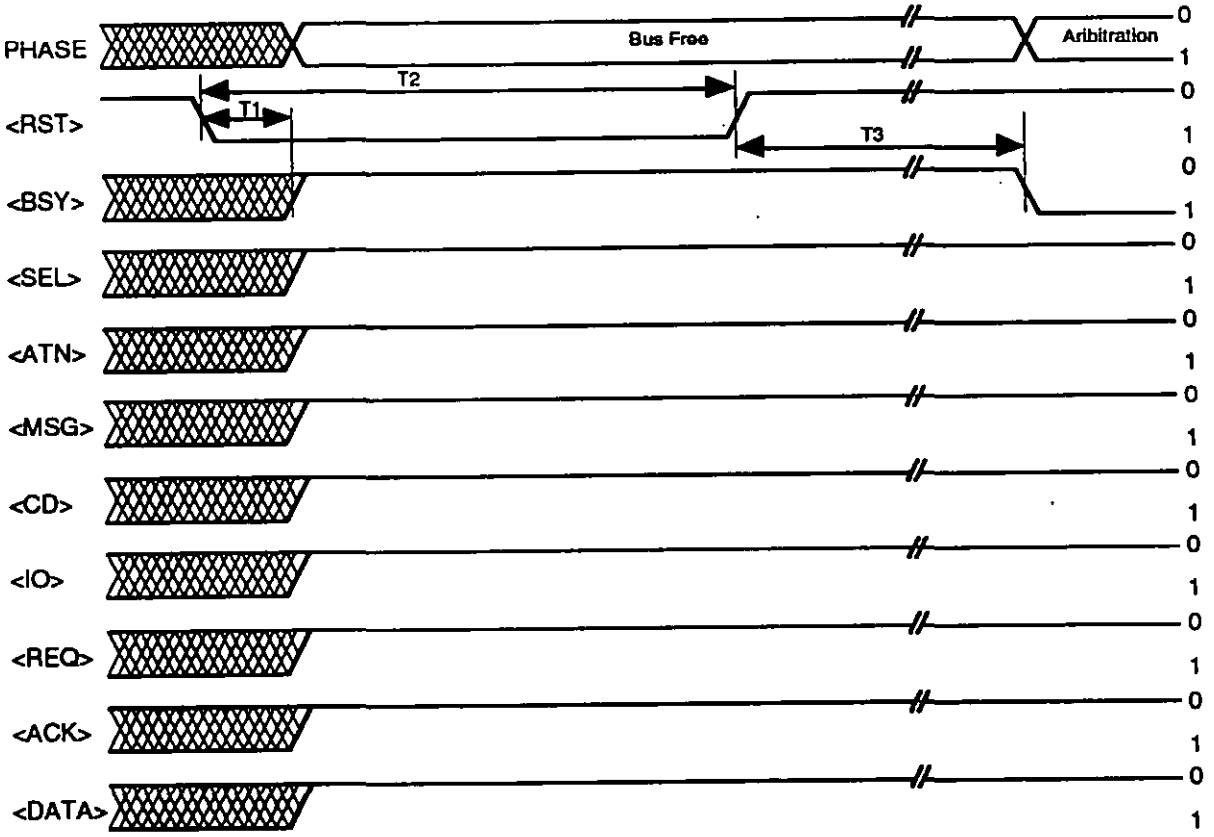


FIGURE 46. Type K protection circuit

Parameter	Description	Min.	Max.	Units
AD	Arbitration Delay	2.4		µs
AP	Assertion Period	90		ns
BCD	Bus Clear Delay		800	ns
BFD	Bus Free Delay	800		ns
BSD	Bus Set Delay		1.8	µs
BSLD	Bus Settle Delay	400		ns
CSD	Cable Skew Delay	10		ns
DRD	Data Release Delay		400	ns
DD	Deskew Delay	45		ns
DSCD	Disconnection Delay	200		µs
HT	Hold Time	45		ns
NP	Negation Period	90		ns
POST	Power On Selection Time		10	s
RTST	Reset to Selection Time		250	ms
RHT	Reset Hold Time	25		µs
SAT	Selection Abort Time		200	µs
STOD	Selection Time-out Delay	250		ms
	Transfer Period	4		ns

1/ Timing parameters listed above are for timing calculations in figures 48 through 54.
2/ In some cases minimum timing parameters listed above may be used as a maximum value in the implied equations in figures 48 through 54.

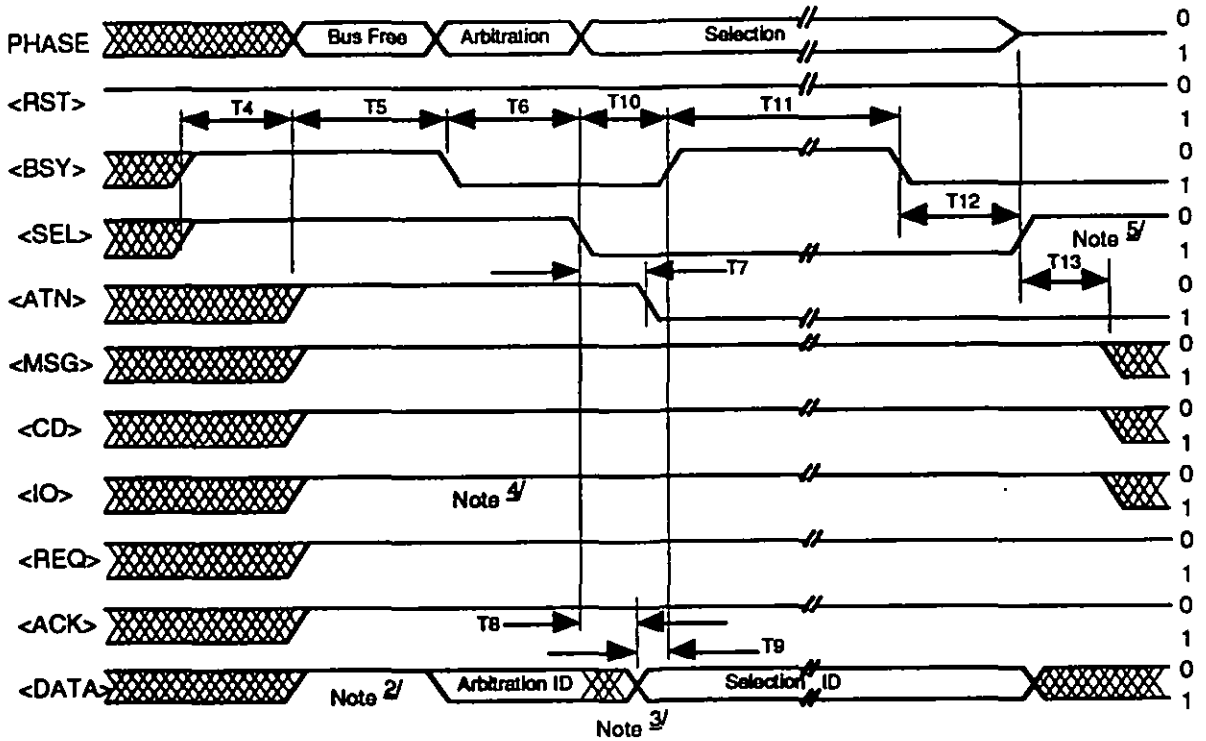
FIGURE 47. Type K base timing parameters



Parameter	Description	Implied Equation	Min.	Max.	Units
T1	RESET active to release of all Bus signals	BCD	--	800	ns
T2	RESET Hold Time	RHT	25	--	µs
T3	RESET Recovery Time	RTST	--	250	ms

1/ Refer to paragraph 5.8.1.8.1.1.
2/ Non-specified parameters shall be represented by "--".
3/ Not to scale.

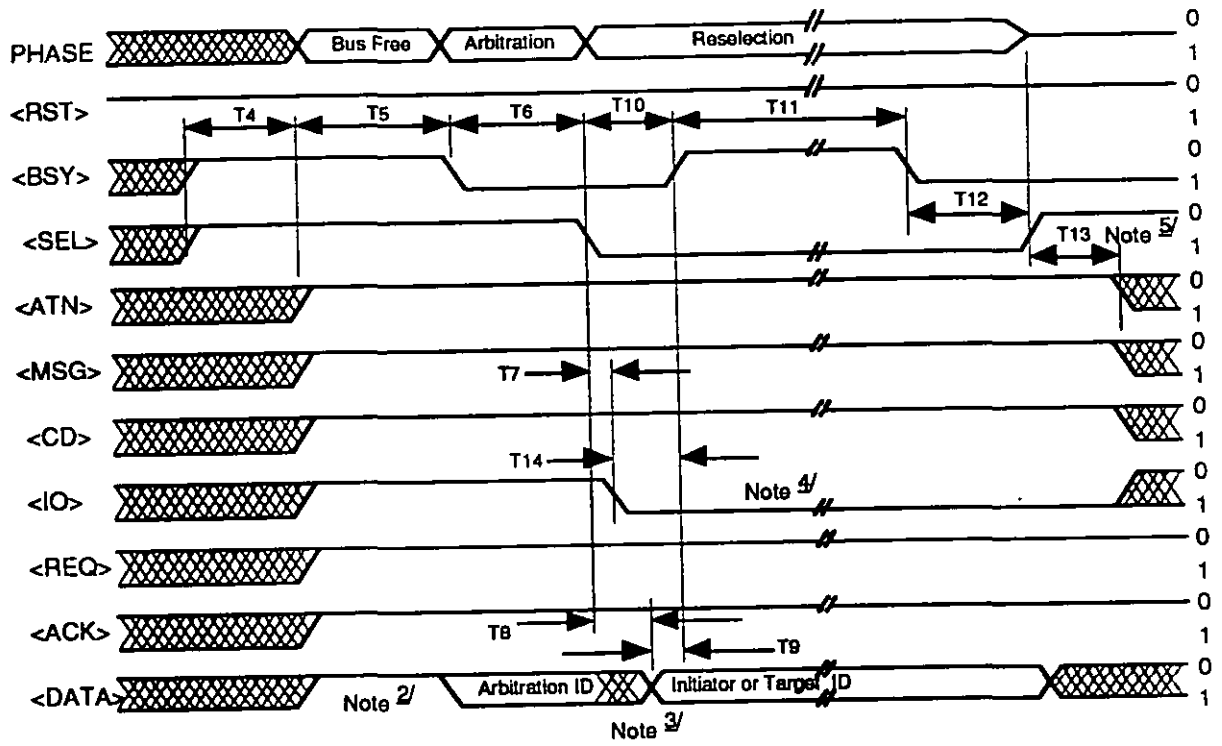
FIGURE 48. Type K reset timing



Parameter	Description	Implied Equation	Min.	Max.	Units
T4	BSY and SEL inactive to BUS FREE phase	BSLD	400	–	ns
T5	BUS FREE to start of Arbitration (BSY active)	BFD	800	–	ns
T6	BUSY active to Select active (Arbitration)	AD	2.4	–	µs
T7	SELECT active to Selection ID and ATTN active	BCD+BSLD	1.2	–	µs
T8	SELECT active to release of loser Arbitration bits	BCD	–	800	ns
T9	Selection ID / ATTN active to release of BSY	2(DD)	90	–	ns
T10	SEL active to BSY inactive	BCD+BSLD+2(DD)	1.29	–	µs
T11	Initiator BSY inactive to Target BSY active	SAT	–	200	µs
T12	BSY active to SEL release	2(DD)	90	–	ns
T13	SEL inactive to MSG / CD / IO change	–	0	–	ns

1/ Refer to paragraph 5.8.1.8.1.2.
2/ No Arbitration allowed after one (1) BSD unless bus remains in Bus Free Phase.
3/ Lower Priority Devices drop their Arbitration ID bits.
4/ The negated IO line indicates Selection.
5/ Whenever a signal transition is required to follow but not precede another signal transition, the specified parameter for this relationship shall be a minimum value of 0 ns in the parameter chart.
6/ Non-specified parameters shall be represented by "--".
7/ Not to scale.

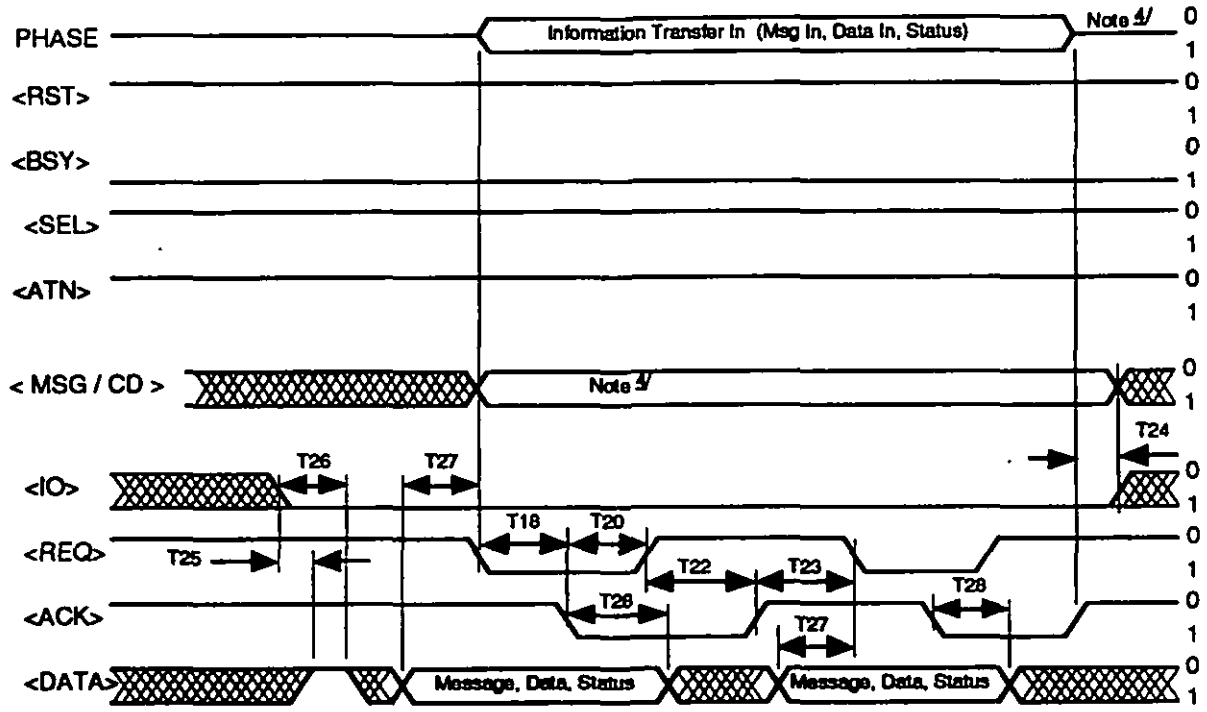
FIGURE 49. Type K arbitration/selection timing



Parameter	Description	Implied Equation	Min.	Max.	Units
T4	BSY and SEL inactive to BUS FREE phase	BSLD	400	--	ns
T5	BUS FREE to start of Arbitration (BSY active)	BFD	800	--	ns
T6	BUSY active to Select active (Arbitration)	AD	2.4	--	µs
T7	SELECT active to Selection ID and IO active	BCD+BSLD	1.2	--	µs
T8	SELECT active to release of loser Arbitration bits	BCD	--	800	ns
T9	Initiator ID / Target ID / ATTN active to release of BSY	2(DD)	90	--	ns
T10	SEL active to BSY Inactive	BCD+BSLD+2(DD)	1.29	--	µs
T11	Initiator BSY inactive to Target BSY active	SAT	--	200	µs
T12	BSY active to SEL release	2(DD)	90	--	ns
T13	SEL inactive to MSG / CD / IO change	--	0	--	ns
T14	IO active to BSY inactive (Reselection)	2(DD)	90	--	ns

1/ Refer to paragraph 5.8.1.8.1.3.
2/ No Arbitration allowed after one (1) BSD unless bus remains in Bus Free Phase.
3/ Lower Priority Devices drop their Arbitration ID bits.
4/ The asserted IO line indicates Reselection.
5/ Whenever a signal transition is required to follow but not precede another signal transition, the specified parameter for this relationship shall be a minimum value of 0 ns in the parameter chart.
6/ Non-specified parameters shall be represented by "--".
7/ Not to scale.

FIGURE 50. Type K arbitration/reselection timing



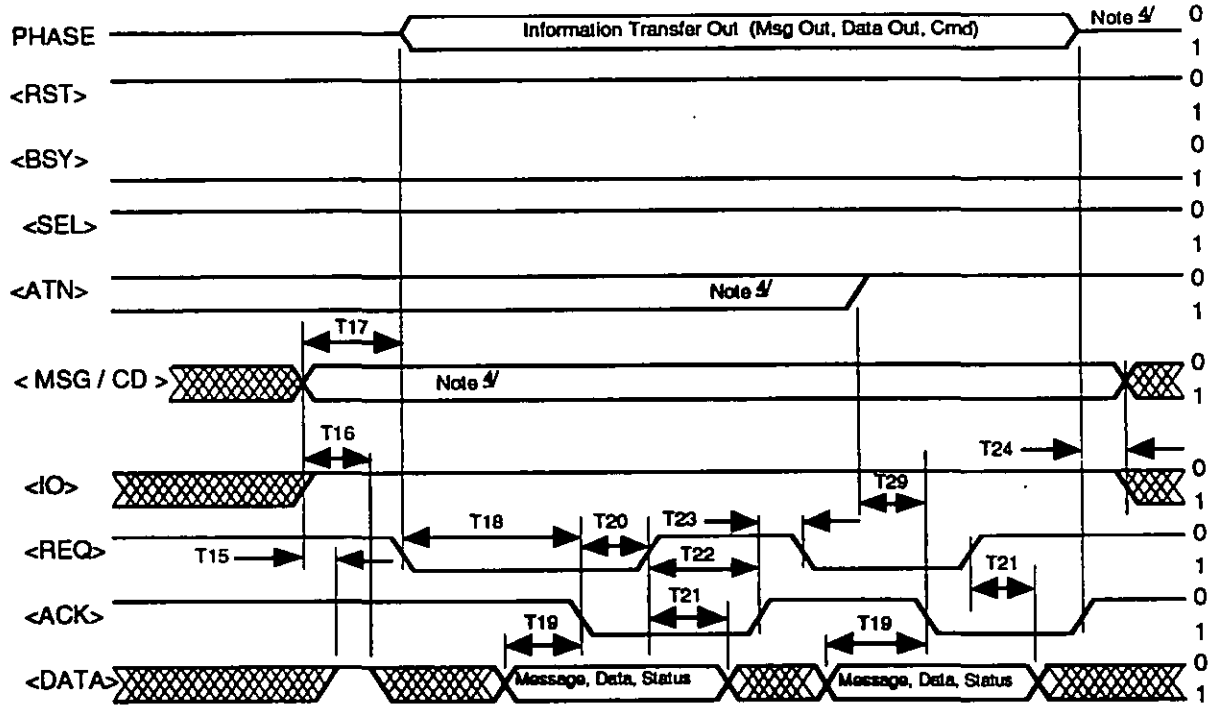
Parameter	Description	Implied Equation	Min.	Max.	Units
T18	Asynchronous Transfer: REQ active to ACK active	--	0	--	ns
T20	Asynchronous Transfer: ACK active to REQ inactive	--	0	--	ns
T22	Asynchronous Transfer: REQ inactive to ACK inactive	--	0	--	ns
T23	Asynchronous Transfer: ACK inactive to REQ active	--	0	--	ns
T24	*Last ACK active to MSG / CD / IO change*	--	0	--	ns
T25	IO active to Initiator drivers disabled	DRD	--	400	ns
T26	IO active to Target drivers enabled	DRD + BSLD	800	--	ns
T27	Input Transfer: Data setup to REQ active	CSD + DD	55	--	ns
T28	Asynchro IN Transfer: Data Hold time from ACK active	--	0	--	ns

1/ *Refer to paragraph 5.8.1.8.1.4.*
2/ Whenever a signal transition is required to follow but not precede another signal transition, the specified parameter for this relationship shall be a minimum value of 0 ns in the parameter chart.
3/ Non-specified parameters shall be represented by "--".
4/ Allowable phase combinations are as follows:

	MSG	CD	IO
Message in	1	1	1
Status	0	1	1
Data in	0	0	1

5/ Not to scale.

FIGURE 51. Type K asynchronous information transfer timing: input transfers -- target to initiator



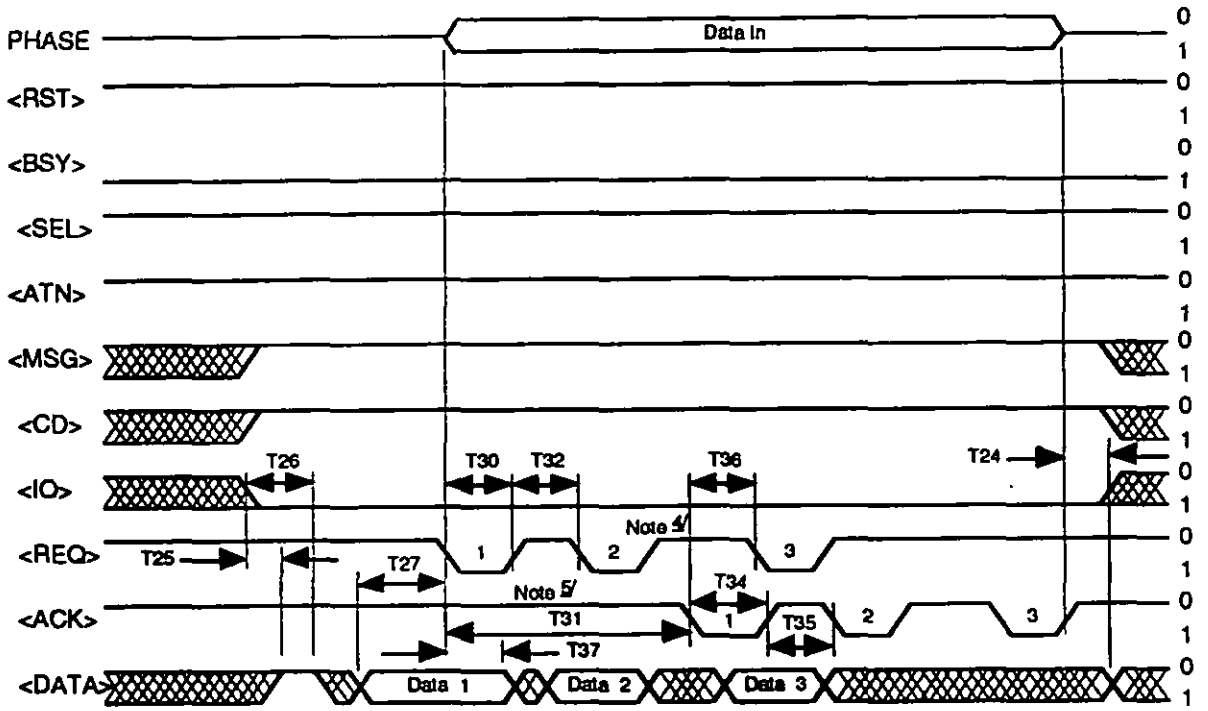
Parameter	Description	Implied Equation	Min.	Max.	Units
T15	IO inactive to Target drivers disabled	DRD	--	400	ns
T16	IO inactive to Initiator drivers enabled	DRD + BSLD	800	--	ns
T17	MSG / CD / IO change to REQ active	BSLD	400	--	ns
T18	Asynchronous Transfer: REQ active to ACK active	--	0	--	ns
T19	Data setup to ACK active (Output transfers)	CSD + DD	55	--	ns
T20	Asynchronous Transfer: ACK active to REQ inactive	--	0	--	ns
T21	Data Hold Time from REQ inactive (Output transfers)	--	0	--	ns
T22	Asynchronous Transfer: REQ inactive to ACK inactive	--	0	--	ns
T23	Asynchronous Transfer: ACK inactive to REQ active	--	0	--	ns
T24	Last ACK active to MSG / CD / IO change	--	0	--	ns
T29	MSG OUT phase: ATTN inactive to last ACK active	2(DD)	90	--	ns

1/ Refer to paragraph 5.8.1.8.1.5.
2/ Whenever a signal transition is required to follow but not precede another signal transition, the specified parameter for this relationship shall be a mimimum value of 0 ns in the parameter chart.
3/ Non-specified parameters shall be represented by "--".
4/ Allowable phase combinations are as follows:

	MSG	CD	IO	ATTN
Message out	1	1	0	1
Command	0	1	0	0
Data out	0	0	0	0

5/ Not to scale.

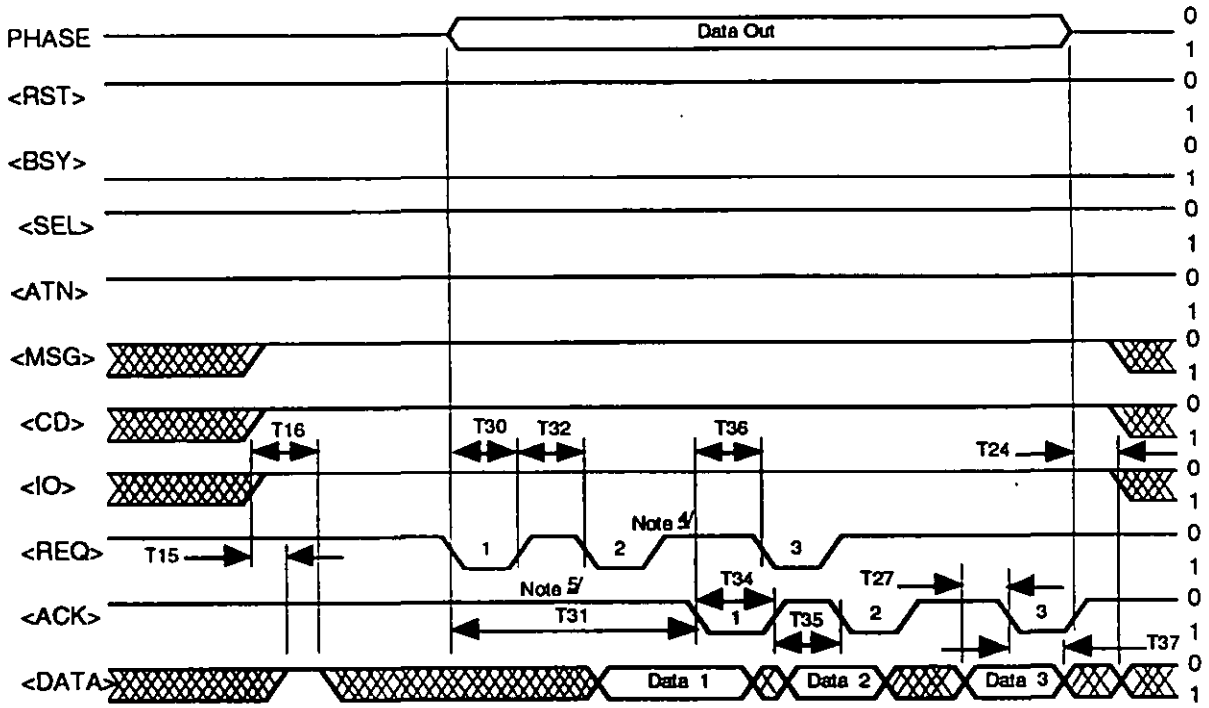
FIGURE 52. Type K asynchronous information transfer timing: output transfers -- initiator to target



Parameter	Description	Implied Equation	Min.	Max.	Units
T24	Last ACK active to MSG / CD / IO change	--	0	--	ns
T25	IO active to Initiator drivers disabled	DRD	--	400	ns
T26	IO active to Target drivers enabled	DRD + BSLD	800	--	ns
T27	Input transfer: Data setup to REQ active	CSD + DD	55	--	ns
T30	Synch Transfer: REQ pulse width	AP	90	--	ns
T31	Synch Transfer: REQ active to ACK active	--	0	--	ns
T32	Synch Transfer: REQ inactive to next REQ active	NP	90	--	ns
T34	Synch Transfer: ACK pulse width	AP	90	--	ns
T35	Synch Transfer: ACK inactive to next ACK active	NP	90	--	ns
T36	Synch Transfer: ACK active to REQ active	--	0	--	ns
T37	Synch IN Transfer: Data Hold Time after REQ active	CSD + DD + HT	100	--	ns

1/ Refer to paragraph 5.8.1.8.1.6.
2/ Whenever a signal transition is required to follow but not precede another signal transition, the specified parameter for this relationship shall be a mimimum value of 0 ns in the parameter chart.
3/ Non-specified parameters shall be represented by "--".
4/ Synchronous offset for the purposes of this diagram shall be set to 2.
5/ The maximum transfer rate shall be negotiated via the message system. T32 and T35 on the timing diagram shall be dependent upon the negotiated rate and shall be 90 ns minimum.
6/ Not to scale.

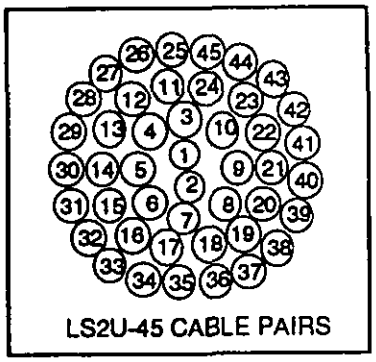
FIGURE 53. Type K synchronous data transfer timing: input transfers -- target to initiator

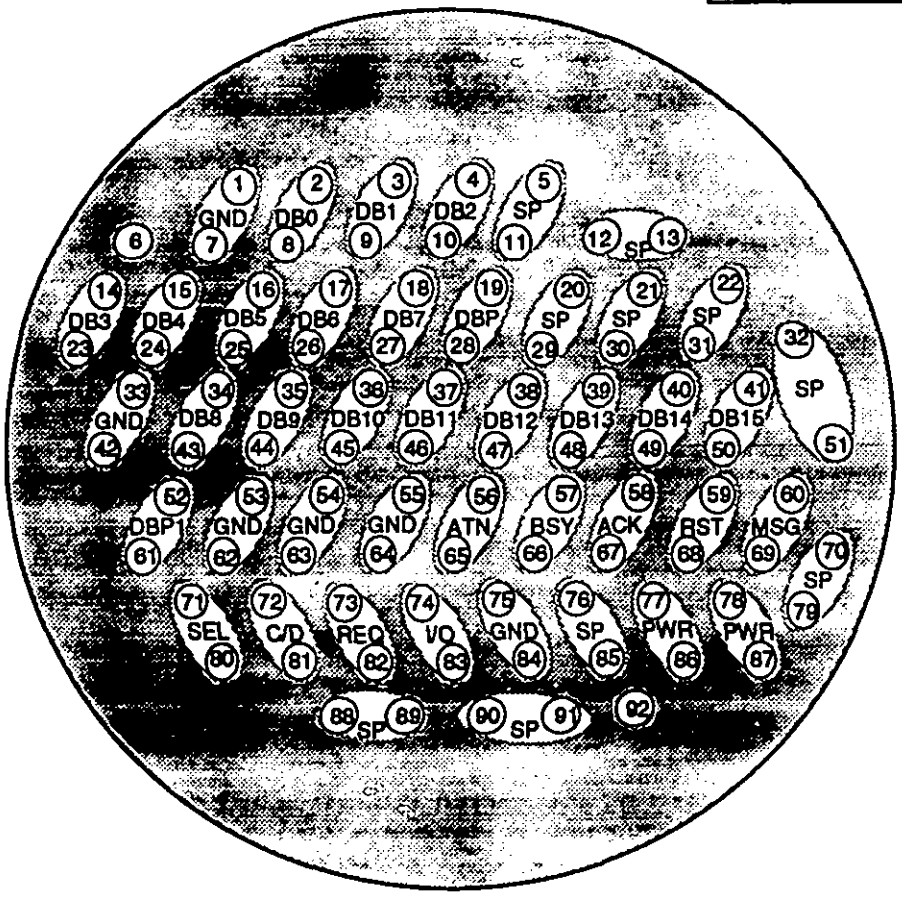


Parameter	Description	Implied Equation	Min.	Max.	Units
T15	IO inactive to Target drivers disabled	DRD	--	400	ns
T16	IO inactive to Iniator drivers enabled	DRD + BSLD	800	--	ns
T19	Data setup to ACK active (Output transfers)	CSD + DD	55	--	ns
T24	Last ACK active to MSG / CD / IO change	--	0	--	ns
T30	Synch Transfer: REQ pulse width	AP	90	--	ns
T31	Synch Transfer: REQ active to ACK active	--	0	--	ns
T32	Synch Transfer: REQ inactive to next REQ active	NP	90	--	ns
T34	Synch Transfer: ACK pulse width	AP	90	--	ns
T35	Synch Transfer: ACK inactive to next ACK active	NP	90	--	ns
T36	Synch Transfer: ACK active to REQ active	--	0	--	ns
T37	Synch IN Transfer: Data Hold Time after REQ active	CSD + DD + HT	100	--	ns

1/ Refer to paragraph 5.8.1.8.1.7.
2/ Whenever a signal transition is required to follow but not precede another signal transition, the specified parameter for this relationship shall be a mimimum value of 0 ns in the parameter chart.
3/ Non-specified parameters shall be represented by "--".
4/ Synchronous offset for the purposes of this diagram shall be set to 2.
5/ The maximum transfer rate shall be negotiated via the message system. T32 and T35 on the timing diagram shall be dependent upon the negotiated rate and shall be 90 ns minimum.
6/ Not to scale.

FIGURE 54. Type K synchronous data transfer timing: output transfers -- initiator to target





MIL-C-28840 CONNECTOR PIN DEFINITION

FIGURE 55. Type K cable pair and connector pin diagram

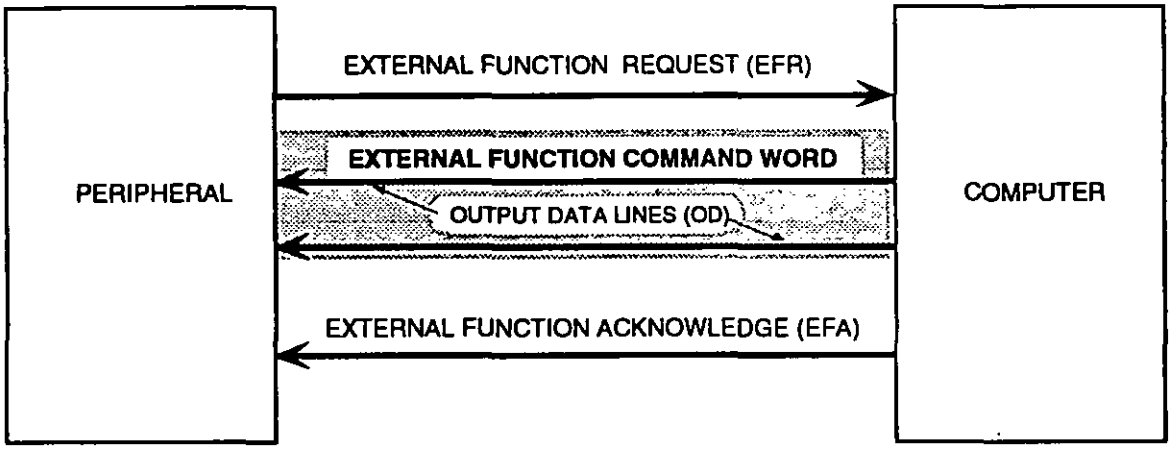


FIGURE 56. External function operations

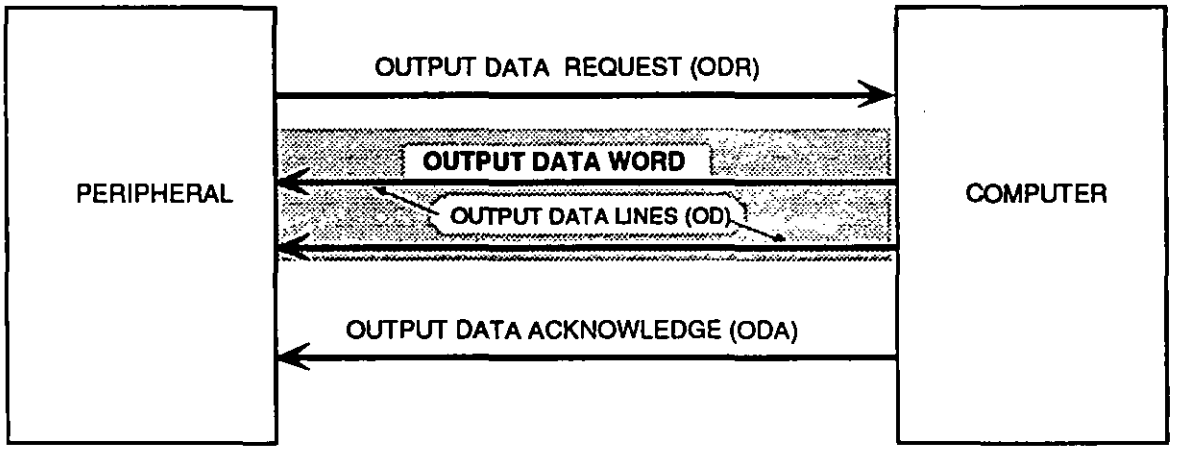


FIGURE 57. Output data operations

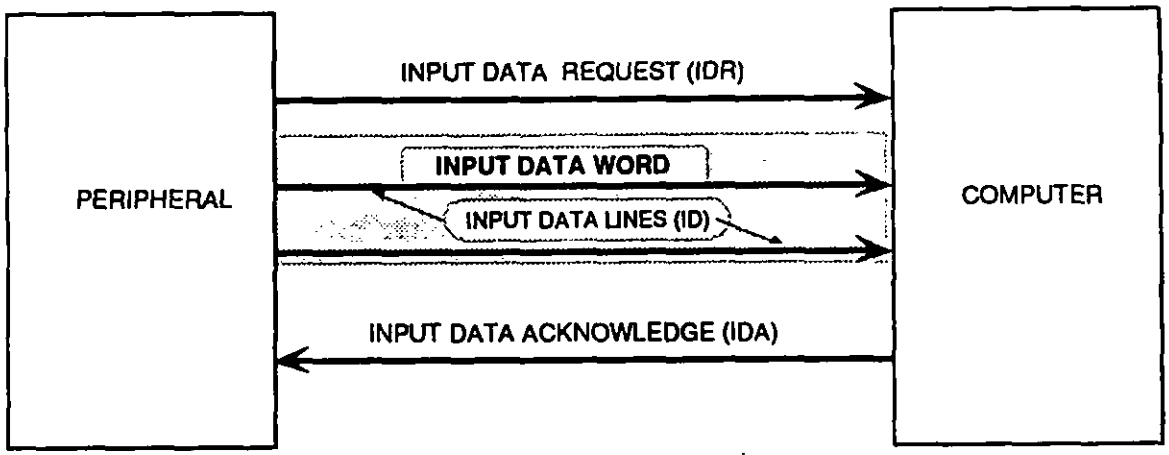


FIGURE 58. Input data operations

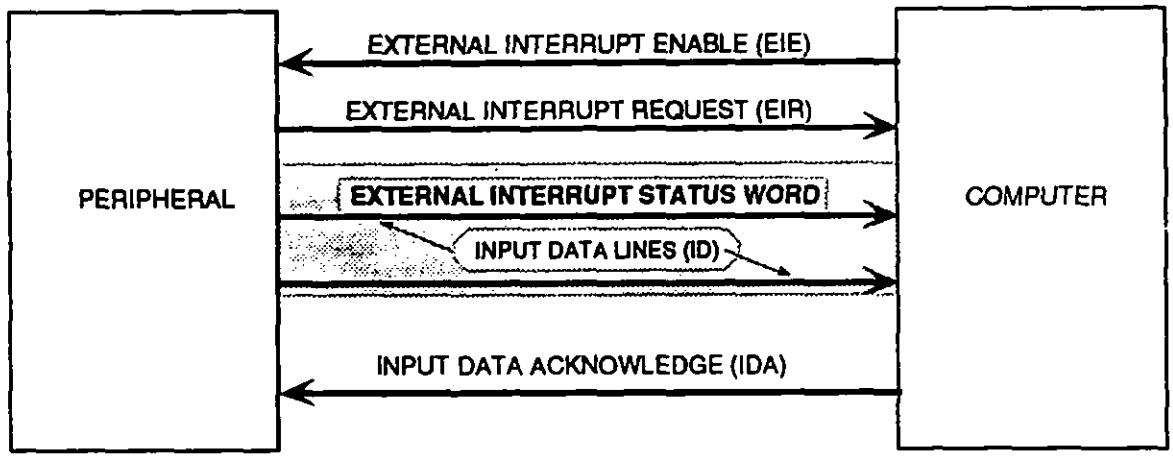
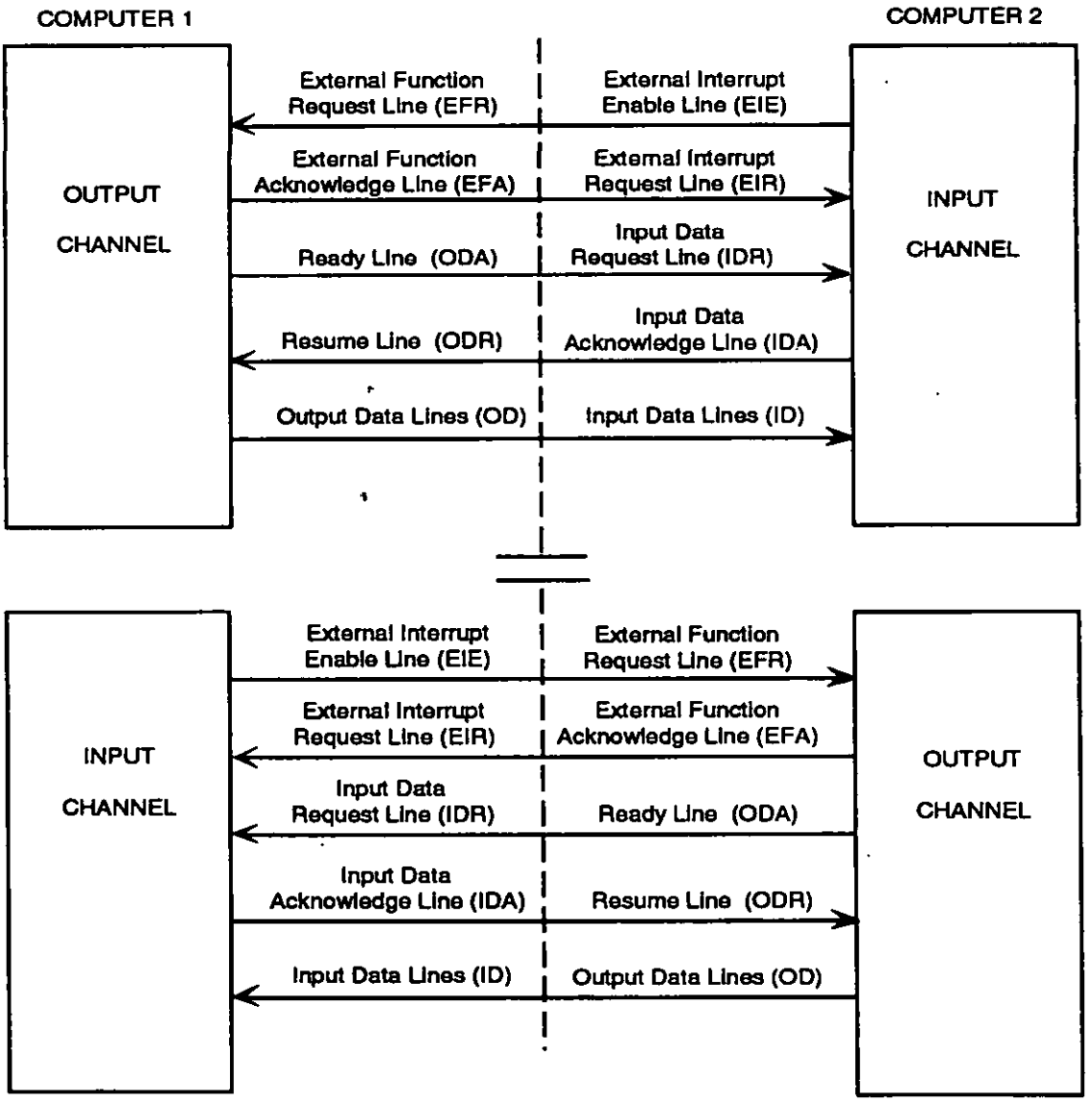


FIGURE 59. External interrupt operations



(arrowheads show direction of signal flow)

FIGURE 60. Computer-to-computer interface

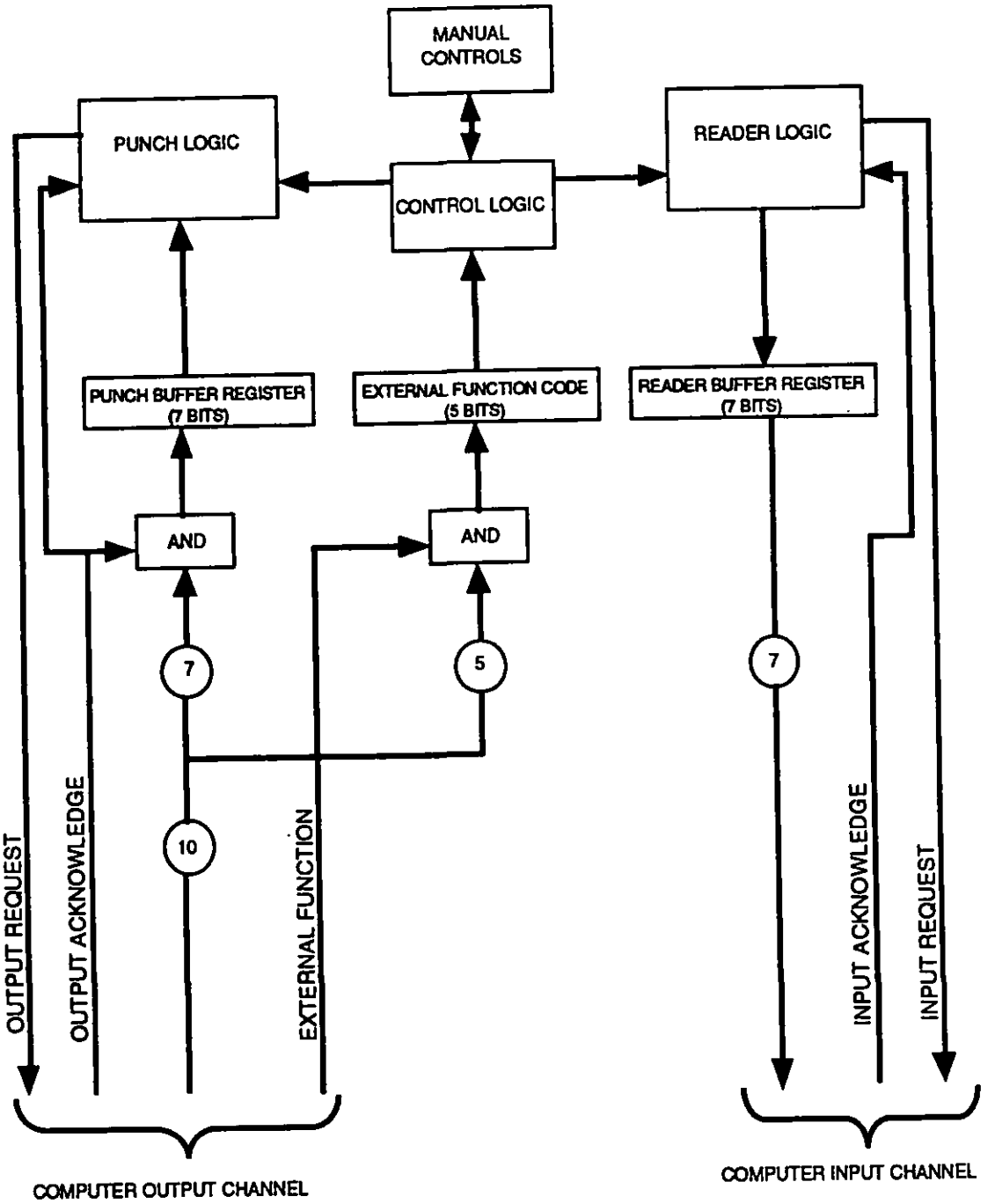


FIGURE 61. Punched tape unit block diagram

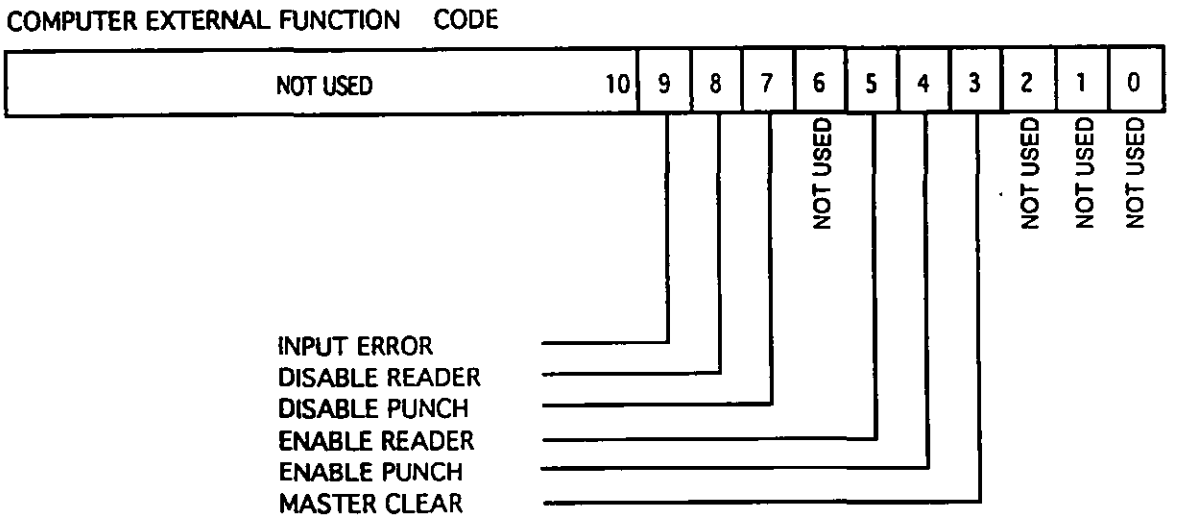


FIGURE 62. External function word format

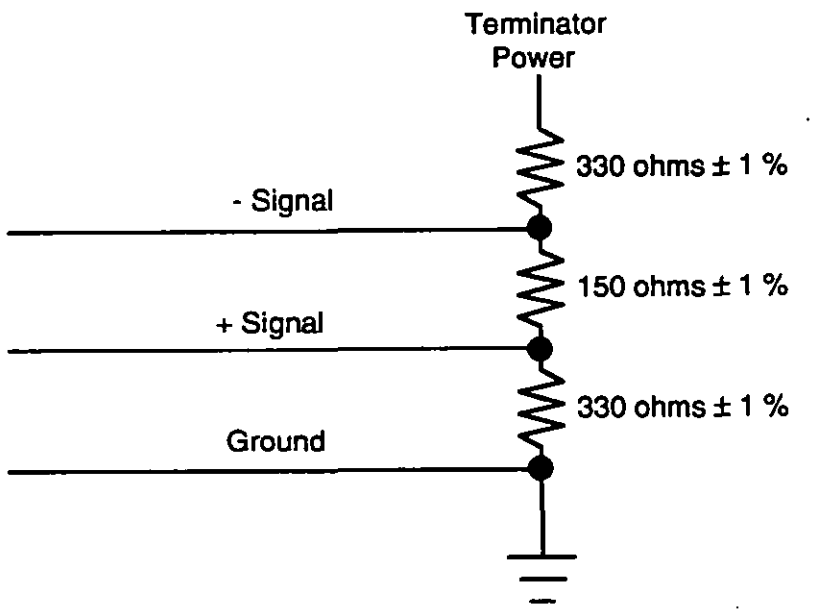
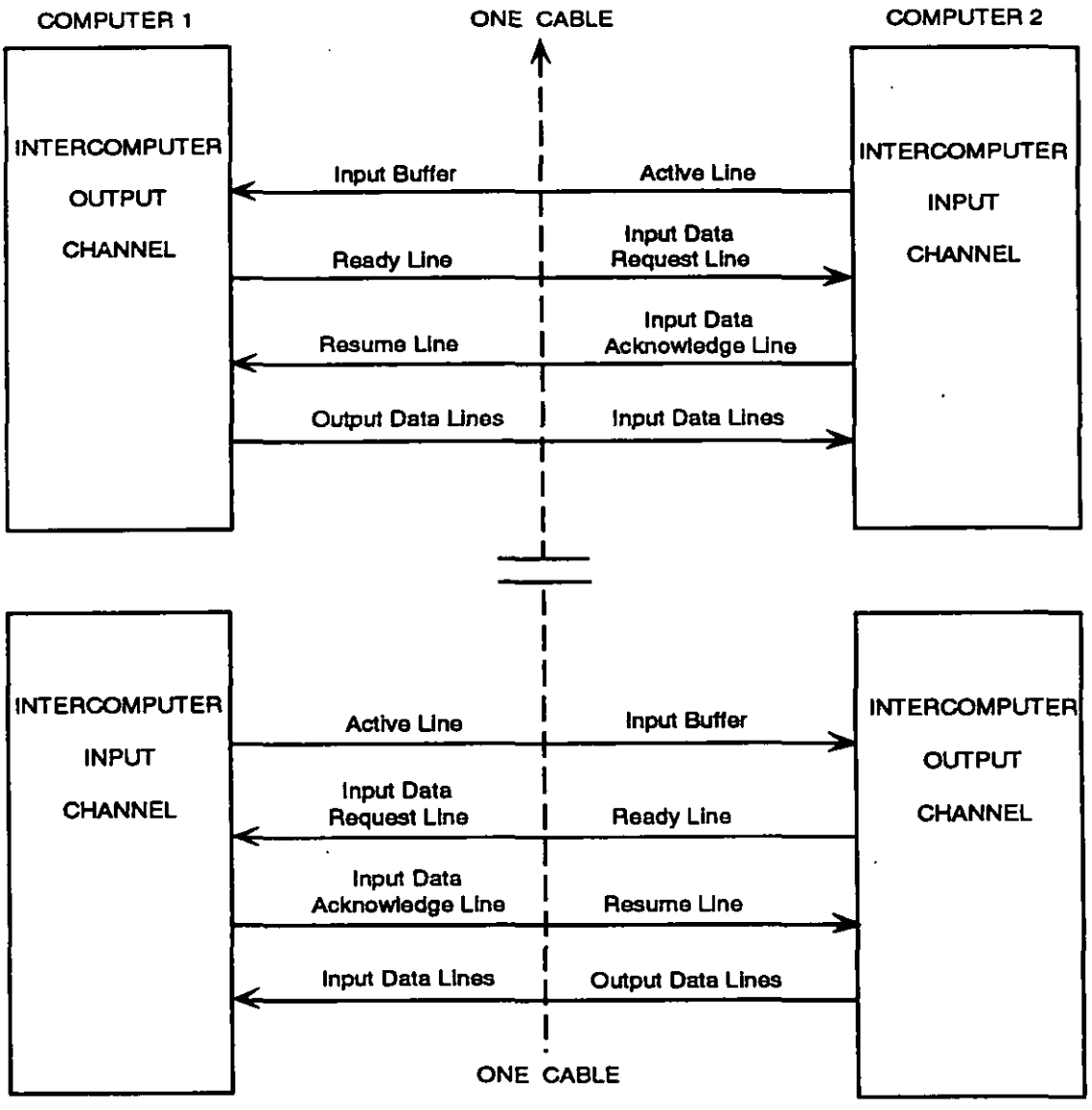
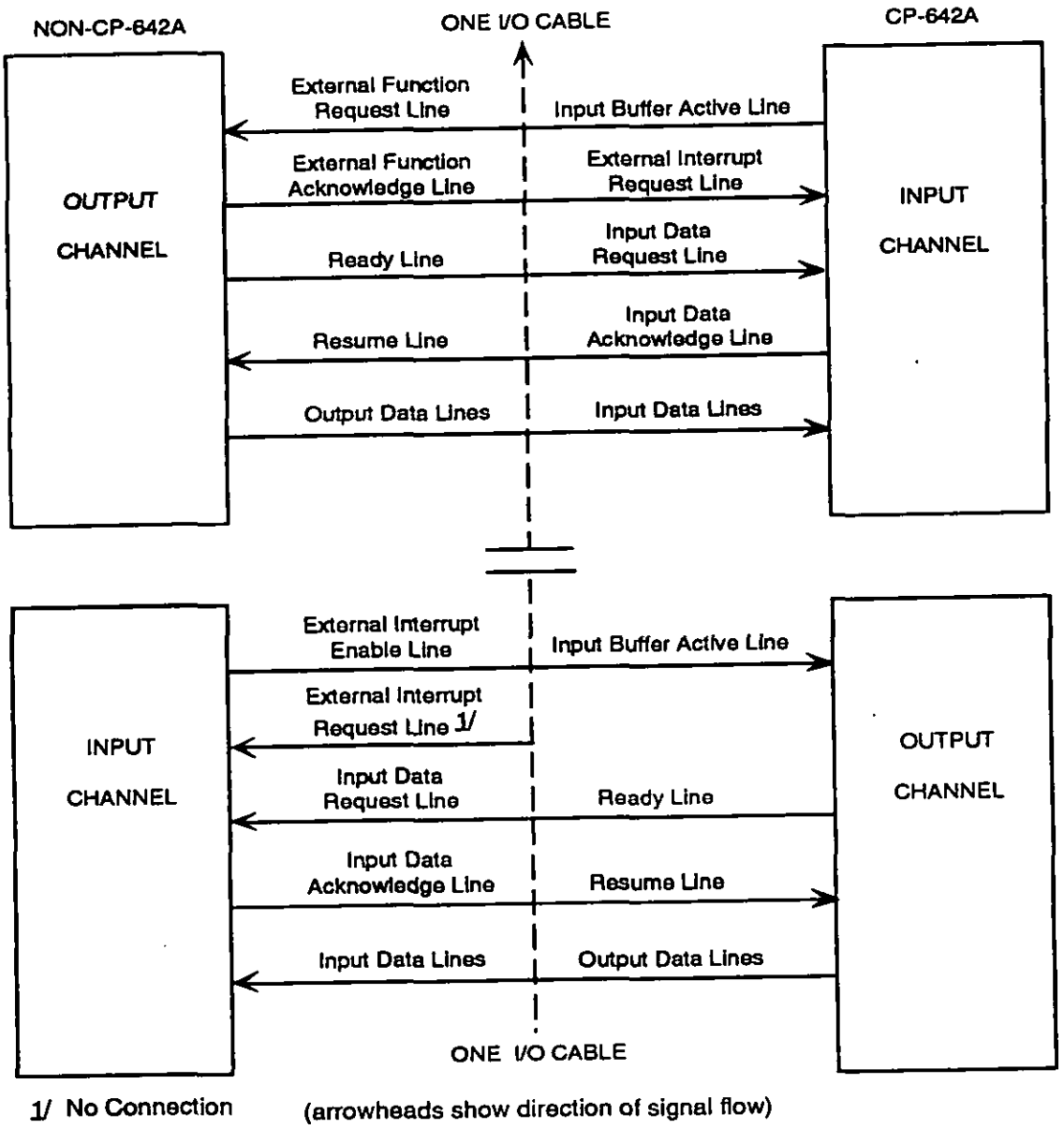


FIGURE 63 Type K bus termination



(arrowheads show direction of signal flow)

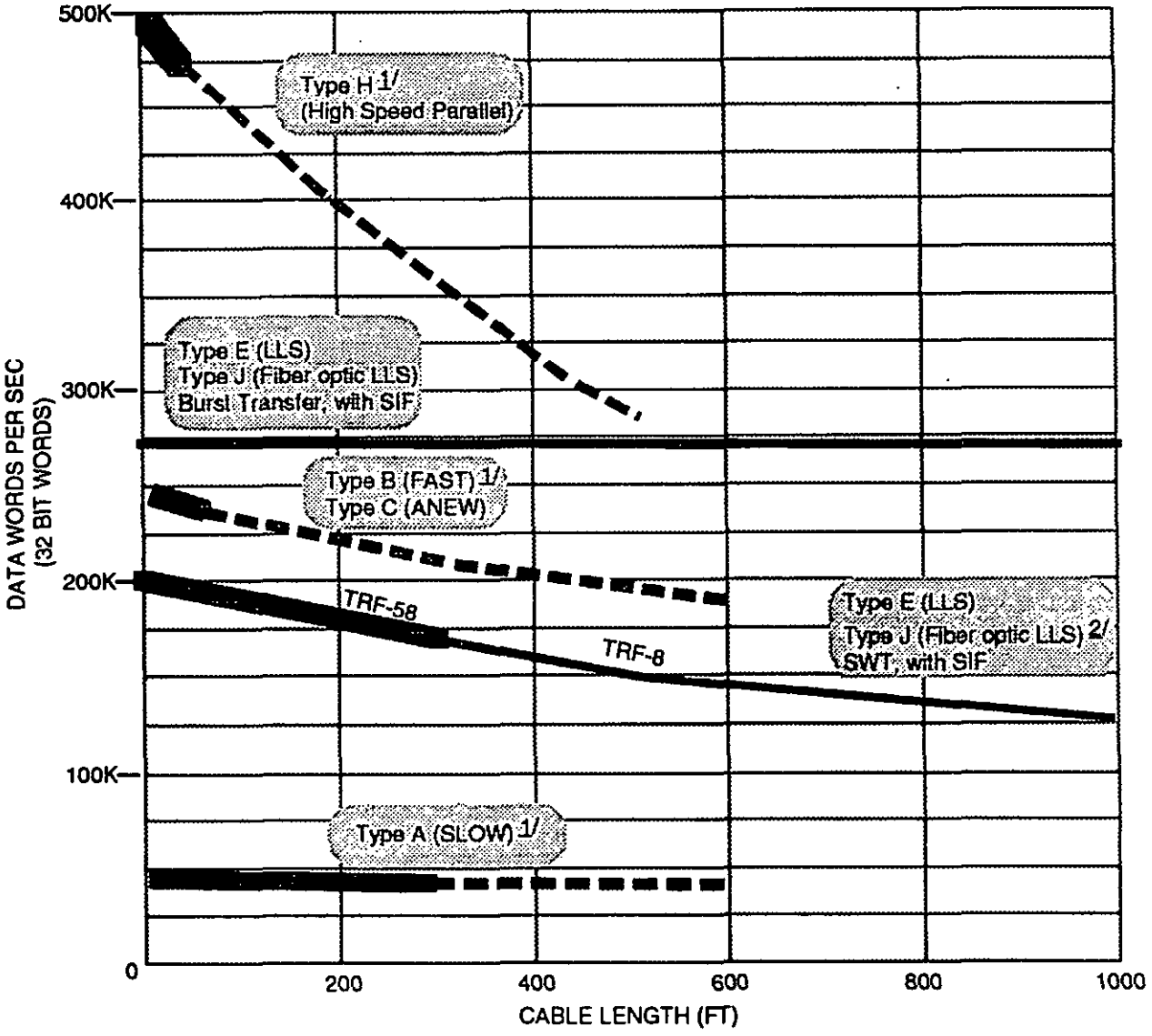
FIGURE 64. CP-642A intercomputer interface



1/ No Connection

(arrowheads show direction of signal flow)

FIGURE 65. Non-CP-642A/CP-642A intercomputer interface



1/ Maximum length is unclear in specification.
2/ Fiber optic application may work up to several kilometers.

FIGURE 66. Effects of cable length on channel throughput

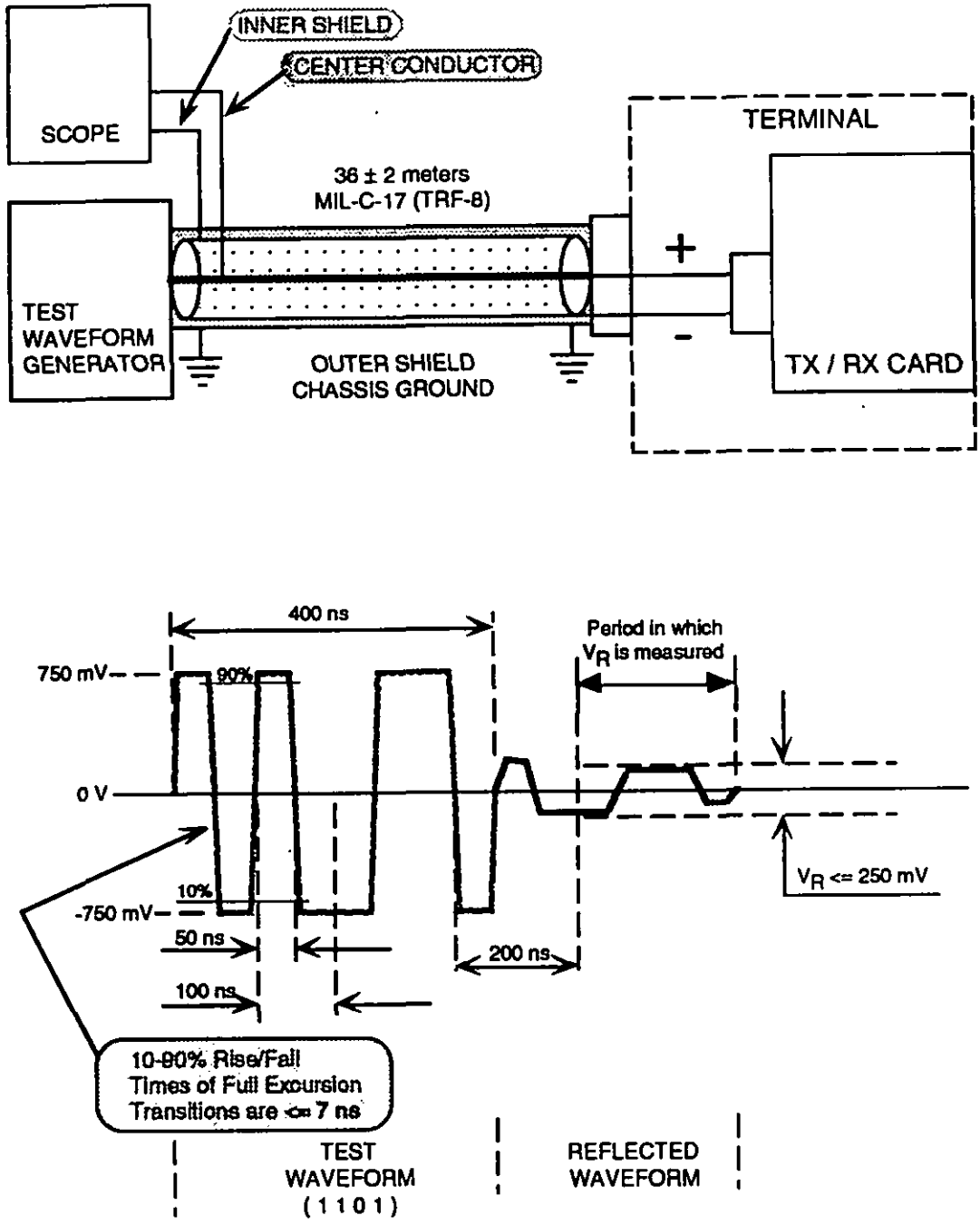


FIGURE 67. Type E reflection test set-up

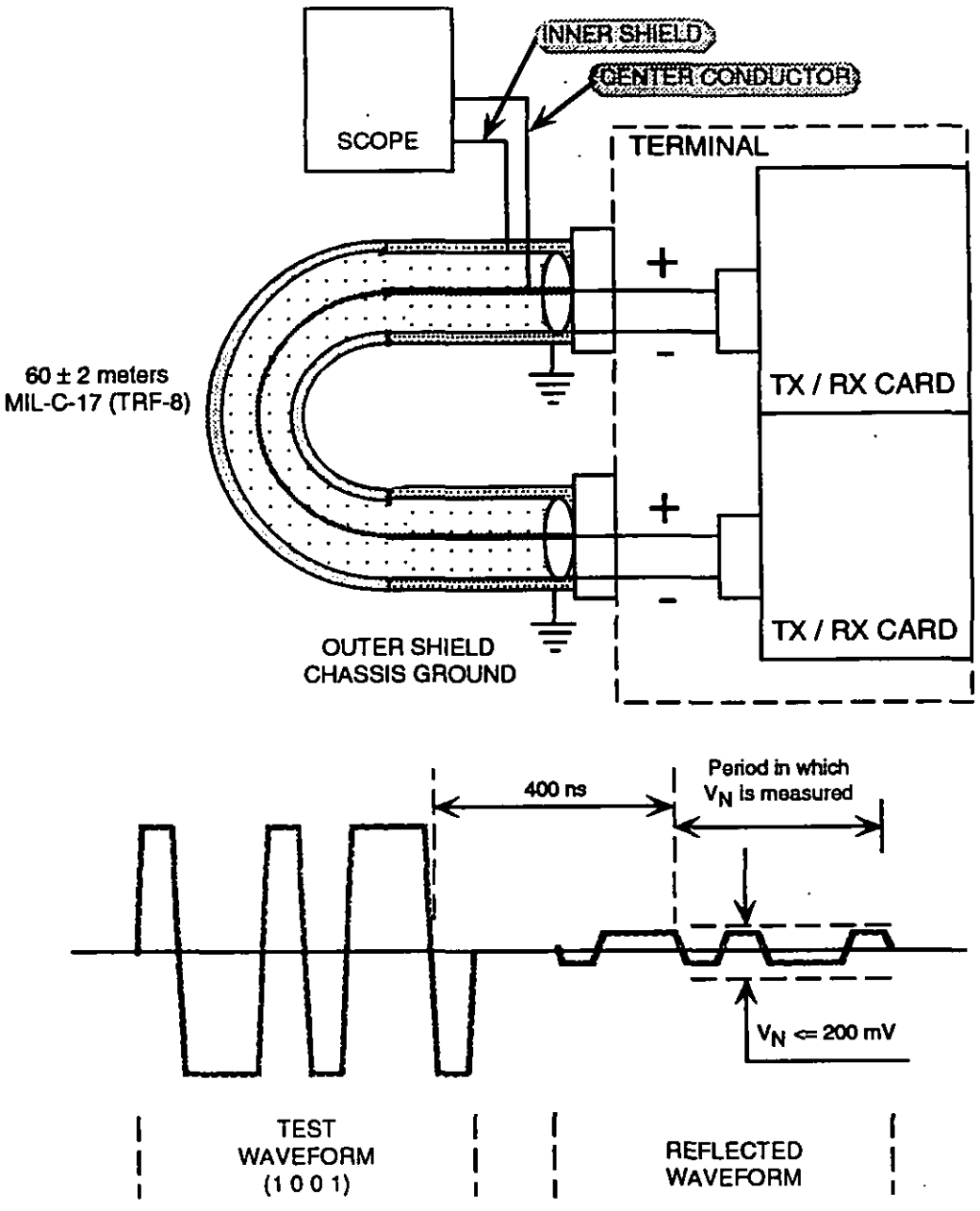


FIGURE 68. Type E composite system channel noise test set-up

STANDARDIZATION DOCUMENT IMPROVEMENT PROPOSAL

INSTRUCTIONS

1. The preparing activity must complete blocks 1, 2, 3, and 8. In block 1, both the comment number and revision letter should be given.
2. The submitter of this form must complete blocks 4, 5, 6, and 7.
3. The preparing activity must provide a reply within 30 days from receipt of this form.

NOTE: This form may not be used to request copies of documents, nor to request waivers, or clarification of requirements on current contracts. Comments submitted on this form do not constitute or imply authorization to waive any portion of the referenced document(s) or to amend contractual requirements.

I RECOMMEND A CHANGE:	1. DOCUMENT NUMBER MIL-STD-1397C(SH)	2. DOCUMENT DATE (YYMMDD) 950601

3. DOCUMENT TITLE
INPUT/OUTPUT INTERFACES, STANDARD DIGITAL DATA, NAVY SYSTEMS

4. NATURE OF CHANGE (Identify paragraph number and include proposed rewrite, if possible. Attach extra sheets as needed.)

5. REASON FOR RECOMMENDATION

6. SUBMITTER

a. NAME (Last, First, Middle Initial)	b. ORGANIZATION	
c. ADDRESS (Include Zip Code)	d. TELEPHONE (Include Area Code) (1) Commercial (2) DSN (if applicable)	7. DATE SUBMITTED (YYMMDD)

8. PREPARING ACTIVITY

a. NAME Technical Point of Contact (TPOC) MR. JAMES R. BABCOCK NRaD Code 823 ADDRESS ALL CORRESPONDENCE AS FOLLOWS:	b. TELEPHONE (Include Area Code) (1) Commercial: DSN: TPOC: 619-553-1075 8-553-1075
c. ADDRESS (Include Zip Code) COMMANDER, NAVAL SEA SYSTEMS COMMAND ATTN: SEA 03R42 [illegible]31 JEFFERSON DAVIS HIGHWAY [illegible]LINGTON, VA 22242-5160	IF YOU DO NOT RECEIVE A REPLY WITHIN 45 DAYS, CONTACT: Defense Quality and Standardization Office 5203 Leesburg Pike, Suite 1403 Falls Church, VA 22041-3466 Telephone 703-756-2340 DSN 289-2340