NOT MEASUREMENT SENSITIVE

MIL-STD-1378E
21 APRIL 1989
SUPERSEDING
MIL-STD-1378D
16 MAY 1986
(SEE 6.6)

MILITARY STANDARD

REQUIREMENTS FOR EMPLOYING STANDARD ELECTRONIC MODULES

AMSC N/A FSC 5963

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

FOREWORD

1. This military standard is approved for use by all Departments and Agencies of the Department of Defense.

2. Beneficial comments (recommendations, additions, deletions) and any pertinent data which may be of use in improving this document should be addressed to: Commander Naval Sea Systems Command, SEA 55Z3, Department of the Navy, Washington, DC 20362-5101 by using the self-addressed Standardization Document Improvement Proposal (DD Form 1426) appearing at the end of this document or by letter.

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1. SCOPE

1.1 Scope. This standard establishes the requirements for the implementation of Standard Electronic Modules (SEM) in the design and construction of selected military electronic systems. The selection of systems for which this standard will be invoked in a contract should be based upon the criteria set forth in MIL-HDBK-246.

1.2 Purpose. The purpose of this standard is to provide the acquisition activity with specific instructions for implementation of the Standard Electronic Modules (SEM) in order to reduce system life cycle costs. This standard also provides instructions for the preparation of a standard electronic module design approval request, instructions for preparing module descriptions, instructions for preparing module specifications, test requirements for digital modules, and test requirements for analog modules.

2. APPLICABLE DOCUMENTS

2.1 Government documents.

2.1.1 Specifications and standards. The following specifications and standards form a part of this standard to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DODISS) and supplement thereto, cited in the solicitation (see 6.2).

SPECIFICATIONS

MILITARY

MIL-E-5400	-	Electronic Equipment, Aerospace, General Specification for.
MIL-E-16400	-	Electronic, Interior Communication and Navigation Equipment, Naval Ship and Shore, General Specification for.
MIL-P-24423	-	Basic Design Requirements for Propulsion and Auxiliary Control Consoles and Associated Control and Instrumentation Equipment, Navy Shipboard use.
MIL-M-28787	-	Modules, Standard Electronic General Specification for.

STANDARDS

MILITARY

MIL-STD-965	-	Parts Control Program.
MIL-STD-1331	-	Parameters to be Controlled for the Specification of Microcircuits.
MIL-STD-1389	-	Design Requirements for Standard Electronic Modules.
MIL-STD-1634	-	Module Descriptions for the Standard Electronic Modules Program.

(Unless otherwise indicated, copies of federal and Military specifications and standards are available from the Naval Publications and Forms Center, (ATTN: NPODS), 5801 Tabor Avenue, Philadelphia, PA 19120-5099.)

2.2 Order of precedence. In the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. DEFINITIONS

3.1 Terms and definitions. The definitions of terms used in this standard shall be as specified herein and in MIL-STD-1331.

3.1.1 SHARP. Standard Hardware Acquisition and Reliability.

3.1.2 SEM. Standard Electronic Modules (includes all modules in the SHARP).

3.1.3 Equipment contractor (EC). EC applies to both system developers and developers of electronic assemblies and subassemblies in which SEM are to be employed.

3.1.4 SEM quality assurance activity (SEM-QAA). The SEM-QAA is the activity responsible for performing SEM qualification testing. (This function is performed by the Naval Weapons Support Center, Code 603, Crane, IN 47522-5060.)

3.1.5 SEM design review activity (SEM-DRA). The SEM-DRA is the activity responsible for the review and approval of SEM designs. (This function is performed by the Naval Avionics Center, Code 814, 6000 E 21st Street, Indianapolis, IN 46219-2189.)

3.1.6 Government program manager (PM). The PM is the Government program manager who is initiating the particular system application.

3.1.7 Design approval request (DAR). DAR is data item necessary to justify a new design for a SEM. It is used to describe new SEM functions in order that they can be classified by the SEM-DRA (see 6.3).

3.1.8 Functional specification. A functional specification is the documentation which completely describes the form, fit, and function of a module assembly. This includes the outer module dimensions including interfaces and the precise electronic function with inputs and outputs. A functional specification also includes a complete and exhaustive series of tests to verify this function.

3.1.9 Design disclosure to SEM-QAA. A design disclosure to SEM-QAA is the documentation needed to manufacture or repair a module. This includes the component lists complete with manufacturer's part numbers, the schematic and artwork of the exact circuitry, and the necessary processes to make the assembly.

3.1.10 SEM standard. A SEM standard is a module for which the SEM-DRA anticipates multisystem applications (see 5.2). Attributes of SEM standard are:

(1) The module has potential multisystem applications.
(2) Complete documentation to SEM-QAA requirements has been prepared.
(3) Documentation is controlled by SEM.
(4) Complete quality assurance is held to SEM requirements.

3.1.11 Candidate SEM standard. A candidate SEM standard module is one for which the SEM-DRA anticipates multisystem applications but for which documentation and qualification have been deferred (see 5.3). Attributes of candidate SEM standard are:

(1) The module has potential multisystem applications.
(2) Complete documentation to SEM requirement unless otherwise specified by the cognizant PM.
(3) SEM-DRA is kept updated on configuration control.
(4) Complete quality assurance is held to SEM requirements unless otherwise specified by the cognizant PM.

3.1.12 SEM special. A SEM special module is one for which the SEM-DRA anticipates a limited scope of applications (intrasystem uses) (see 5.4). The attributes of SEM specials are:

(1) Limited applications.
(2) SEM-DRA is kept updated on configuration control unless otherwise specified by cognizant PM.
(3) Complete documentation to SEM requirements unless otherwise specified by the cognizant PM.
(4) Complete quality assurance is held to SEM requirements unless otherwise specified by cognizant PM.

4. GENERAL REQUIREMENTS

4.1 General. When this standard is invoked, all electronic circuitry shall be designed in accordance with MIL-STD-1389. Any exceptions to implementation of SEM requirements must be specified in the contract. For special and candidate standard modules all documentation and hardware deliverables shall be as specified in the Contract Data Requirement List (CDRL) or line item.

4.2 Priority of implementation. The EC shall implement electronic circuitry requirements in accordance with the priority sequence in 4.2.1 through 4.2.4.

4.2.1 Existing SEM standards. The EC shall initially attempt to implement system electronic circuitry requirements with existing SEM standards as listed in MIL-STD-1634.

4.2.2 In-process SEM standards. The EC shall coordinate with the SEM-DRA to determine whether there are any new SEM being developed within the SEM which are not as yet included in MIL-STD-1634. In the event that there is an applicable module design whose completion schedule will not impose any scheduling incompatibility, the module shall be used in lieu of proposing the development of another new module function.

4.2.3 Existing SEM specials. The next order of priority in SEM implementation shall be to employ an existing SEM special module which has been fully designed to the requirements of MIL-STD-1389. Change control of SEM specials lies with the PM who originated the special module. Therefore, use of an existing SEM special will depend on whether or not the PM can arrange joint change control with the PM who originated the SEM special module. Information regarding these modules shall be obtained from the SEM-DRA. If the need and desire exists, SEM specials may be upgraded to SEM standards.

4.2.4 New SEM designs. New SEM designs shall be proposed by the EC only under one of the exceptions specified in 4.2.4.1 through 4.2.4.4.

4.2.4.1 Circuit functional requirements. New SEM designs shall be proposed when a system partitioning analysis shows that the required system function cannot be implemented and the system operating parameters cannot be achieved by utilizing existing SEM.

4.2.4.2 System packaging constraints. When a packaging analysis shows that the system cannot be implemented in the space available by using existing SEM, new and functionally complex SEM designs which would achieve the necessary requirements may be proposed.

4.2.4.3 System environmental constraints. When the environmental requirements of a system preclude the use of an otherwise functionally suitable SEM which has been developed to a less stringent SEM environmental class, a new module design shall be proposed to meet the more stringent requirement. Such a new design, however, shall be functionally interchangeable and contact compatible with the existing module of the less stringent SEM environmental class.

4.2.4.4 Cost effectiveness requirements. A new module design shall be proposed in lieu of an applicable existing SEM where substantial cost savings may result. It shall be demonstrated through a detailed cost analysis that on a life cycle cost basis the use of a new SEM design is more cost effective than an existing module. This cost analysis shall directly compare the cost of implementing the required system function with an existing SEM versus the new SEM design.

4.3 Design requirements for new SEM. New SEM designs shall be developed in accordance with the following requirements.

4.3.1 Design objectives. The developer of a new SEM shall, where feasible, design the new module with the objective of its being classified as a SEM standard.

4.3.1.1 Maximum flexibility. Except as otherwise specified in 5.3, the design of SEM shall be such that each module can be utilized in a broad range of system applications.

4.3.1.2 Proprietary parts or processes. It is the intent of this standard to encourage competition so that those modules which are standard can be made by more than one vendor. The utilization of proprietary parts, processes, or techniques is discouraged.

4.3.1.3 Repairability. A cost analysis shall be made of the module design and evaluated by the PM to determine whether or not it would be cost effective to repair the module if it should fail. If the evaluation shows that it would be cost effective to repair a failed module, those classified as SEM standard shall be documented with both design disclosed and functional specifications in accordance with appendix C. A module classified as a repairable SEM special shall be documented with a design disclosed specification in accordance with appendix C, unless otherwise specified by the PM.

5. DETAILED REQUIREMENTS

5.1 Purpose. The requirements herein define and explain the documentation and quality assurance requirements which make up the different types of SEM. The steps involved in implementing a new SEM are also described.

5.2 SEM standard requirements. A SEM standard is a module function which has the potential for being used in many military electronic systems and shall meet the following requirements.

5.2.1 SEM standard design requirements. A SEM standard shall be designed in accordance with the requirements of MIL-STD-1389.

5.2.2 SEM standard quality assurance requirements. A SEM standard shall conform to the quality assurance requirements specified in MIL-M-28787.

5.2.3 SEM standard documentation requirements. A SEM standard shall be documented in accordance with appendix C, both with a functional specification (also called a "slash sheet") and a design disclosed specification unless otherwise specified by the SEM-DRA and SEM-QAA (see 5.10).

5.2.4 Nonstandard parts waiver. In the event a SEM standard employs parts other than those specified in MIL-E-16400, MIL-E-5400, or MIL-P-24423 (or other contractually specified documents) as standard parts, the EC shall submit to the SEM-QAA documentation in accordance with MIL-STD-965 explaining the need for such parts and the reason or reasons that the equipment performance requirements cannot be met using the nearest similar standard parts (see 5.11).

5.3 Candidate SEM standard requirements. A candidate SEM standard is a module which has the potential for being used in multisystem applications, however, due to program constraints during the system development phase, the documentation and qualification have been deferred. A candidate SEM standard shall be developed into a SEM standard when the initial system application evolves into a production phase or earlier if another system application enables the development of the standard.

5.3.1 Candidate SEM standard design requirements. A candidate SEM standard shall be designed in accordance with the requirements of MIL-STD-1389.

5.3.2 Candidate SEM standard quality assurance requirements. A candidate SEM standard shall conform to the quality assurance requirements of MIL-M-28787 unless otherwise specified by the cognizant PM.

5.3.3 Candidate SEM standard documentation requirements. A candidate SEM standard shall be documented in accordance with appendix C. The type of documentation to be prepared shall be as directed by the cognizant PM, but it is recommended that documentation to the level of a SEM standard be planned. Upon preparation of the rough draft documentation for a candidate SEM standard, a copy shall be forwarded to the SEM-DRA for approval. Thereafter, the EC shall identify to the SEM-DRA within 25 working days of any changes made to this documentation, design of the module, or selection of components. The changes shall be identified in writing.

5.3.4 Nonstandard parts approval. In the event a candidate SEM standard employs parts other than those specified in MIL-E-16400, MIL-E-5400, or MIL-P-24423 (or other contractually specified documents) as standard parts, the EC shall submit to the SEM-DRA documentation in accordance with MIL-STD-965 explaining the need for such parts and the reason or reasons that equipment performance requirements cannot be met using the nearest similar standard parts (see 5.11).

5.4 SEM special requirements. A SEM special is a module function which does not have the potential for broad applicability. These modules shall be designed to meet the following requirements.

5.4.1 SEM special design requirements. SEM special modules shall meet the mechanical and electrical design requirements of MIL-STD-1389.

5.4.2 SEM special quality assurance requirements. SEM special modules shall be in accordance with the quality assurance requirements of MIL-M-28787 unless otherwise specified by the cognizant PM.

5.4.3 SEM special documentation requirements. SEM special modules shall be documented in accordance with appendix C. The level of documentation shall be directed by the cognizant PM. However, if the module is repairable, it is recommended that both functional and design disclosed specifications be prepared, and if non-repairable, it is recommended that a functional specification only be prepared.

5.4.4 Nonstandard parts approval. In the event that a SEM special module employs parts other than those specified in MIL-E-16400 (or other contractually specified documents) as standard parts, the contractor shall submit documentation in accordance with MIL-STD-965 explaining the need for such parts and the reason or reasons that equipment performance requirements cannot be met using the nearest similar standard parts (see 5.11). Existing SEM special modules using nonstandard parts which have been fully designed, documented, and qualified to the requirements of MIL-STD-1389 and MIL-M-28787 do not require reapproval of nonstandard parts.

5.5 Implementation procedures. The procedure for obtaining approval of new associated detail specifications is illustrated on figure 1. The function of the elements depicted on figure 1 are as defined in 5.6 through 5.10.4.

5.6 Submission of design approval requests (Block 1). The EC shall complete and forward the DAR (in accordance with appendix A) concurrently to the SEM-DRA and the PM for each new module design proposed (see 5.11 and 6.4.1).

5.6.1 DAR action (Block 2). Following receipt of each DAR, the SEM-DRA will forward the DAR action notification to the EC and the PM. If the DAR is approved, the following will be indicated on the action notification:

(a) Module classification (SEM standard or SEM special).

(b) Module key code.

(c) Module name.

(d) MIL-M-28787 detail specification number for SEM standards.

(e) SEM special module document numbers are assigned by the PM (or his agent). If the module is classified as a special, the procedure is concluded at this point. If the DAR is disapproved, the action notification will give a complete explanation for the disapproving action. If the PM elects to treat the special as a standard in documentation and quality assurance, the procedure continues as for a standard.

5.6.1.1 PM review (Block 3). The PM shall review the DAR, comment, and approve or disapprove for a particular system application.

5.6.1.2 Status notification. The EC shall notify the SEM-DRA and the PM at periodic intervals of the current design status of modules with approved DARs (see 5.11 and 6.4.2).

5.7 Submission of module descriptions (Block 4). The EC shall prepare a module description in accordance with appendix B for each module classified as standard by the SEM-DRA and shall forward the completed description concurrently to the SEM-DRA and the SEM-QAA (see 5.11 and 6.4.3).

5.8 Preparation of detail specification draft (Block 4). The EC proposing a new SEM design shall develop the appropriate associated detail specification for the module in accordance with appendix C. The EC shall submit a rough draft detail specification to the PM, the SEM-DRA, and the SEM-QAA for review and comment (Blocks 5 and 6) prior to the preparation of the preliminary associated detail specification (see 5.11).

5.9 Preparation of preliminary associated detail specification (Block 7). Upon approval of the associated detail specification draft by the PM, the SEM-DRA, and the SEM-QAA, the EC shall prepare the preliminary associated detail specification in accordance with appendix C. The EC obtains proof and correlation modules and submits them to SEM-QAA.

5.9.1 SEM correlation (Block 9). The SEM-QAA performs correlation testing on the submitted modules and verifies the contents of the preliminary associated detail specification. The SEM-QAA then submits the results to the EC, the SEM-QAA, and the PM.

5.10 SEM initial qualification submission (Block 13). Upon completion of the preliminary associated detail specification, the EC shall submit the appropriate number of module samples and the preliminary detail specification to the SEM-QAA for initial qualification in accordance with MIL-M-28787. At the same time, a copy of the associated detail specification shall be submitted to the SEM-DRA and the PM for review. (Blocks 8 and 10). The SEM-DRA and the PM review the preliminary associated detail specification and submit comments to the EC and the SEM-QAA.

5.10.1 Notification for initial qualification. The EC shall notify the SEM-QAA not later than 90 days prior to submission of the module samples and associated detail specification for initial qualification testing.

5.10.2 Completion of initial qualification (Block 14). The time required to complete qualification procedures for SEM will not exceed 120 days after receipt of the module samples at the SEM-QAA. The SEM-QAA submits the results to the EC, the SEM-DRA, and the PM.

5.10.3 Retention of module samples. All modules supplied for initial qualification to the SEM-QAA will be retained by the SEM-QAA unless otherwise agreed to by the PM and the SEM-QAA.

5.10.4 Repository for final detail specification (Block 11). Upon completion of correlation data and approval of the preliminary detail specification by the SEM-QAA and the SEM-DRA, the EC shall prepare the final detail specification. The final detail specification shall include recommendations made as a result of design review and correlation data. The EC shall submit copies of the final detail specification to the PM, the SEM-DRA, and the SEM-QAA for approval. After approval, the detail specification masters for SEM standards will be forwarded to the SEM-QAA (Block 12). The SEM-QAA will forward the detail specification to the MIL-M-28787 preparing activity. The SEM-QAA is responsible for maintaining

configuration management for all SEM standard modules. They review all proposed revisions and coordinate with common module users to determine whether module interchangeability would be adversely affected. SEM special module configuration management remains the responsibility of the developer (for example, the sponsoring program office or acquisition office). SEM candidate standard module configuration remains the responsibility of the developer until the time the module is fully developed as a SEM standard. However, prior to that time, any changes to the documentation, design of the module, or selection of components must be identified to the SEM-DRA.

5.10.5 Initial qualification rejection. In the event of module failure during initial qualification tests, the SEM-QAA will forward a detailed report of test results and recommendations to the PM and the EC for corrective action.

5.10.6 Resubmission. The EC shall make all necessary corrections to the module design and documentation or module construction, or both, and resubmit new module samples for qualification or revised detail specification, or both, to the SEM-QAA.

5.11 Contract data requirements. Data required by this standard are not deliverable unless specified on the Contract Data Requirements List (DD Form 1423) or the contract schedule (see 6.3).

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory.)

6.1 Intended use. This standard contains requirements for employing standard electronic modules.

6.2 Issue of DODISS. When this standard is used in acquisition, the issue of the DODISS to be applicable to this solicitation must be cited in this solicitation (see 2.1.1).

6.3 Data requirements. The following Data Item Descriptions (DID's) must be listed, as applicable, on the Contract Data Requirements List (DD Form 1423) when this standard is applied on a contract, in order to obtain the data, except where DOD FAR Supplement 27.475-1 exempts the requirement for a DD Form 1423. The deliverable data includes the following:

Reference Paragraph	DID Number	DID Title
5.3.4, 5.4.4	DI-MISC-80071	Parts Approval Request.
3.1.7, 5.6, 5.6.1, 5.6.1.1, 5.7	DI-E-7042	Request, Design Approval for Standard Electronic Modules Program.
5.8	DI-E-7043	Specifications, Standard Electronic Modules Program (SEMP).
5.3.4, 5.4.4	DI-E-7044	Request, Exception, Standard Electronic Modules Program (SEMP).

The above DID's were those cleared as of the date of this standard. The current issue of DOD 5010.12-L, Acquisition Management Systems and Data Requirements Control List (AMSDL), must be researched to ensure that only current, cleared DID's are cited on the DD Form 1423.

6.4 Timely submission and approval.

6.4.1 DAR. Submission of the DAR should be made within 120 calendar days after award of contract, but no later than 30 days prior to the Critical Design Review (CDR). In addition, updated DARs should be submitted within 14 days after additional requirements are realized. DAR action notification should be forwarded to the PM within 25 working days of DAR receipt.

6.4.2 Status. EC notification of the PM as to module design status occurs at intervals not exceeding 90 days.

6.4.3 Module descriptions. Submission of the module description should be made no later than 25 working days after receipt of the SEM-DRA letter approving and classifying the module DAR as a standard.

6.5 Subject term (keyword) listing.

Modules, Standard Electronic
SEM
Standard Electronic Modules

6.6 Changes from previous issue. Marginal notations are not used in this revision to identify changes with respect to the previous issue due to the extensiveness of the changes.

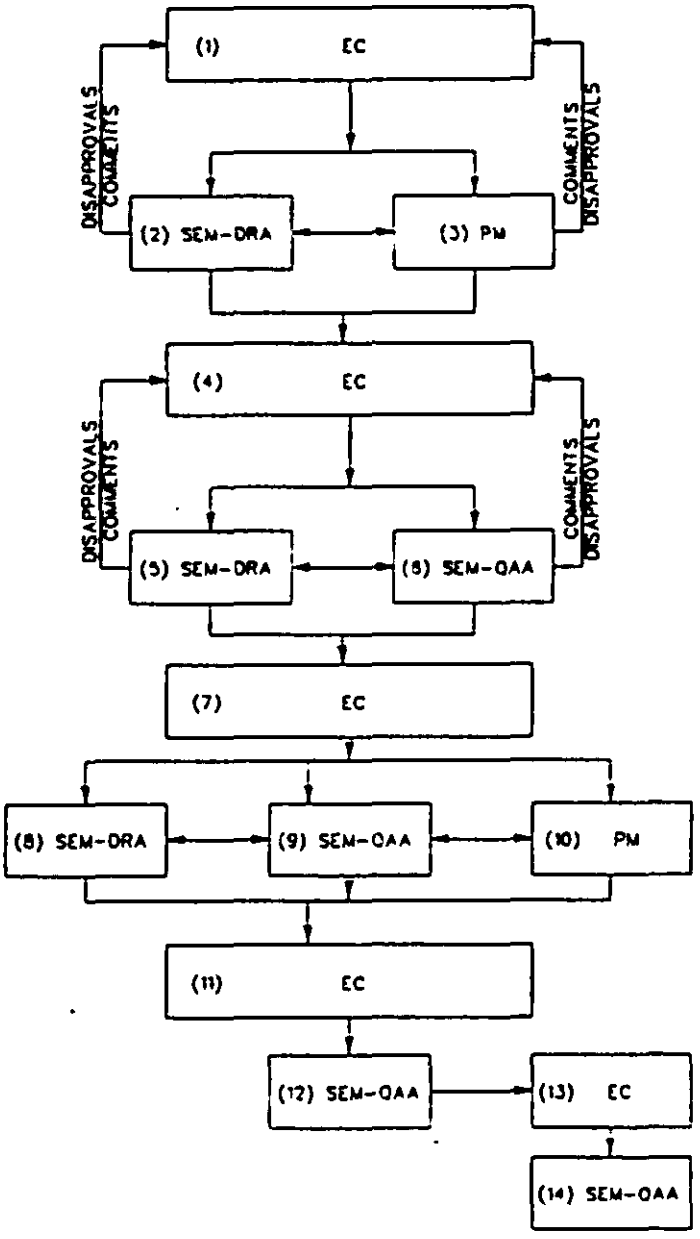
Custodians
Army - ER
Navy - SH
Air Force - 85

Review activities:
Army - AT, AV
Navy - AS, MC
Air Force - 13, 17, 19
DLA - ES

Preparing activity:
Navy - SH

Agent:
NWSC Crane

(Project 5963-0038)



NOTES:
1. See 3.1 for definition of activities.
2. See 5.6 through 5.10.4 for function of each block.

FIGURE 1. SEM design approval procedure.

APPENDIX A

SAMPLE STANDARD ELECTRONIC MODULE DESIGN APPROVAL REQUEST

10. SCOPE

10.1 Scope. This appendix is not a mandatory part of the standard. The information contained herein is intended for guidance only. This appendix provides a sample blank design approval request form. It may be reproduced as necessary.

20. APPLICABLE DOCUMENTS. This section is not applicable to this appendix.

APPENDIX A

STANDARD ELECTRONIC MODULE DESIGN APPROVAL REQUEST	DAR NUMBER _____ FOR DATE RECEIVED _____ DRA CLASSIFICATION _____ USE DETAIL SPECIFICATION _____ ONLY KEY CODE _____ MILITARY PART NO _____ NAME _____

INITIATOR INFORMATION:

ACTIVITY NAME _____

ADDRESS _____

_____

INITIAL SYSTEM APPLICATION _____

NAME OF COGNIZANT INDIVIDUAL _____

In order to uniquely identify this system, the system information on the final pages of this DAR *must be completed when the first DAR for this system is submitted.*

Will this module be designed in accordance with MIL-STD-1389? _____

If not, give exceptions. _____

MODULE INFORMATION: Identification number (reference DAR, assembly, and so forth) for this module? _____ (for correspondence purposes)

NAME _____ SIZE _____

TYPE: DIGITAL ANALOG OTHER _____

DRAWING ASSY NO _____ CODE IDENT _____ FORMAT: A B C D E

NUMBER OF COMPLETE CIRCUITS PER MODULE _____. PITCH _____

NUMBER OF CONNECTOR CONTACTS _____.

DOES MODULE CONTAIN PROGRAMMABLE ELEMENTS? _____ IF SO, SEE PROGRAMMABLE ELEMENTS SECTION (EX: PROM, CONFIGURABLE GATE ARRAY, PROGRAMMABLE LOGIC ARRAY, AND SO FORTH)

COMPONENT INFORMATION:

FUNCTION	TECHNOLOGY	VENDOR AND PART NUMBER	ALTERNATE PART NUMBER

APPENDIX A

WILL PROPRIETARY DESIGNS, PARTS, OR PROCESSES BE USED? _____ YES _____ NO

IF YES, IDENTIFY _____

_____

_____

MODULE QUANTITY PER SYSTEM APPLICATION _____

NUMBER OF SYSTEMS CONTRACTED _____

ESTIMATED PER MODULE PARTS COST _____

WHICH EXISTING SEM HAVE BEEN CONSIDERED FOR THE IMPLEMENTATION OF THIS FUNCTION? _____

_____

_____

ESTIMATED COMPLETION DATE:

DESIGN _____

PROTOTYPE _____

MODULE SPECIFICATION _____

PRODUCTION READINESS _____

FUNCTIONAL DESCRIPTION:

(TYPICALLY THE DESCRIPTION SHALL INCLUDE, AS APPLICABLE, INPUT/OUTPUT REQUIREMENTS AND RELATIONSHIPS, TRUTH TABLES, BLOCK DIAGRAMS, BOOLEAN EQUATIONS, CONTROL REQUIREMENTS, PROGRAMMABILITY, AND SO FORTH)

APPENDIX A

LOGIC/SCHEMATIC DIAGRAM

(A LOGIC/SCHEMATIC DIAGRAM SHALL BE INCLUDED, DENOTING CONTACT ASSIGNMENTS (IF KNOWN), PART NUMBERS, AND COMPONENT VALUES). IF PROGRAMMABLE GATE FUNCTIONS ARE USED, THE GATE EQUIVALENT DIAGRAMS, TRANSFER FUNCTIONS, OR TRUTH TABLES SHALL BE PROVIDED.

APPENDIX A

DIGITAL CHARACTERISTICS: (THE FOLLOWING SHALL BE DEFINED FOR DIGITAL MODULES AS APPLICABLE)

INPUT CHARACTERISTICS	MINIMUM	TYPICAL	MAXIMUM	CONDITIONS
V_{IL}				
V_{IH}				
I_{IL}				
I_{IL}				
I_{IL}				
I_{IH}				
I_{IH}				
I_{IH}				
CAPACITANCE				
OUTPUT CHARACTERISTICS				
V_{OL}				
V_{OH}				
I_{OL}				
I_{OH}				
PROPAGATION DELAY TIMES				
MAXIMUM LOAD CAPACITANCE				
POWER SUPPLY VOLTAGES AND TOLERANCES				
ABSOLUTE MAXIMUM				
NORMAL VOLTAGE(S)				
MODULE POWER DISSIPATION				

LIST ANY ADDITIONAL PARAMETER REQUIREMENTS

ANALOG CHARACTERISTICS: (THE FOLLOWING SHALL BE DEFINED FOR ANALOG MODULES AS APPLICABLE)

ANALOG INPUTS

INPUT AMPLITUDE _____ TOLERANCE _____

MINIMUM INPUT IMPEDANCE _____ CONDITIONS _____

INPUT FREQUENCY RANGE _____

SIGNAL TYPE (SINE WAVE, SQUARE WAVE, ETC.) _____

INPUT OFFSET VOLTAGE _____

INPUT OFFSET CURRENT _____

INPUT BIAS CURRENT _____

ANALOG OUTPUTS

AMPLITUDE RANGE _____ TO _____ TOLERANCE _____

SIGNAL TYPE _____

OUTPUT IMPEDANCE _____

MAXIMUM OUTPUT CURRENT _____

FREQUENCY _____ TOLERANCE _____

ACCURACY OF FUNCTION _____

PHASE SHIFT _____

SIGNAL WAVEFORM DISTORTION _____

VOLTAGE GAIN _____

POWER GAIN _____

UPPER 3 dB POINT (Hz) _____

LOWER 3 dB POINT (Hz) _____

SLEW RATE _____

COMMON MODE REJECTION _____

SETTLING TIME _____

ACCURACY FOLLOWING SETTLING TIME _____

TURNS RATIO (FOR TRANSFORMERS) _____

POWER SUPPLY VOLTAGES AND TOLERANCES _____

MODULE POWER DISSIPATION: TYPICAL _____ MAXIMUM _____

LIST ADDITIONAL PARAMETER REQUIREMENTS _____

_____

_____

OTHER CHARACTERISTICS: (FOR ADDITIONAL INFORMATION OR FOR FUNCTIONS THAT ARE OTHER THAN DIGITAL OR ANALOG TYPICALLY CONVERTERS, POWER SUPPLIES AND SO FORTH)

_____

_____

_____

APPENDIX A

SYSTEM INFORMATION SECTION

Name of this system/equipment. (Please define acronyms) _____

_____

_____

List other names which also identify this system/equipment. _____

_____

_____

Please give a brief description of this system/equipment. _____

_____

_____

_____

Is this equipment a part of another equipment, or made up of several different subequipment units (cabinets, and so forth) or is it an update of an existing equipment? If so, please explain the relationship. _____

_____

_____

_____

What is the cognizant Government activity?

Activity name _____

Activity address _____

_____

Who is the cognizant Government individual?

Name and Code _____

Address _____

_____

Telephone _____

Government contract number _____

What is the schedule for this system/equipment? _____

Prototype request for bids (RFB) date. _____

Prototype delivery date. _____

Production RFB date. _____

First production delivery date. _____

APPENDIX A

Who is the prime contractor?

Company name _____

Division _____

Address _____

_____

Cognizant individual _____

Telephone _____

Name of the subcontractor(s) for major subassemblies (involving new module designs).

Company name _____

Division _____

Address _____

_____

Cognizant individual _____

Telephone _____

How may equipment units will be produced?

During prototype phase _____

During production phase _____

What environmental class are these modules designed to meet? _____

Are special modules in this system designed to be repairable? _____

Where will this equipment be installed? Describe each different installation.

_____

How many systems will be installed at each different type of installation? _____

Will each installation of this system contain the same complement of modules, or will each installation be entirely different? (Please explain). _____

_____

_____

_____

APPENDIX A

PROGRAMMABLE ELEMENTS

What type of programmable element is used? _____

_____

How many program versions of this module will exist in the system/equipment at a given time? _____

_____

Describe the type of information programmed on these module(s). _____

_____

How many ROM key codes are anticipated? _____

(A drawing number is required for each key code assigned). Should these modules all be keyed the same or keyed differently? (Explain) _____

_____

If you need assistance in completing this form, please contact:

Naval Avionics Center (B/814)
6000 E 21st Street
Indianapolis, IN 46219-2189

Telephone: (317) 353-3735

APPENDIX A

What modules are to be used in this equipment? (Exact quantities are not expected but be as accurate as you can. Also please list any new modules which will be designed for this equipment).

Key code and military part number or reference number	Description	Modules per equipment	Comments

Use additional sheets, if required.

APPENDIX B

INSTRUCTIONS FOR PREPARING MODULE DESCRIPTIONS

10. SCOPE

10.1 Scope. This appendix is a mandatory part of the standard and shall be used in the preparation of module descriptions for the Standard Electronic Modules (SEM) Program. The information contained herein is intended for compliance. This appendix does not attempt to specify how a module shall be designed, tested, or used, but describes the information that shall be included in the module description and the format for presenting the information.

20. APPLICABLE DOCUMENTS

20.1 Non-Government publications. The following documents form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents which are DOD adopted are those listed in the issue of the DODISS cited in the solicitation. Unless otherwise specified, the issues of documents not listed in the DODISS are the issues of the documents cited in the solicitation.

AMERICAN NATIONAL STANDARDS INSTITUTE (ANSI)

Y 14.15	-	Electrical and Electronics Diagrams.
STD 91	-	Standard Graphic Symbols for Logic Functions
Y 32.2	-	Graphic Symbols for Electrical and Electronics Diagrams.

(Application for copies should be addressed to the American National Standards Institute, Inc., 1430 Broadway, New York, NY 10018.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

APPENDIX B

30. GENERAL REQUIREMENTS

30.1 General requirements. Module descriptions prepared in accordance with this appendix will be included in MIL-STD-1634 and used for selection and application of SEM modules. Information, in addition to that required by this appendix, may be added to the module description as required so that selection and application of a particular module to a system will be more easily accomplished.

30.1.1 Style, format, and identification. An example of the style, format, and identification of module descriptions is available from the SEM-DRA.

30.1.2 Warnings, cautions, and notes. Warnings and cautions shall precede the text to which they apply. Notes may either precede or follow, or both, the text to which they apply depending on the material to be highlighted. Inserts in the text shall be short and concise and be used to emphasize important and critical instructions.

30.1.2.1 Warnings. Warnings shall be used when an operating procedure or practice if not followed correctly, could result in personal injury or loss of life.

30.1.2.2 Cautions. Cautions shall be used when an operating procedure or practice if not strictly observed, could result in damage to, or destruction of, equipment.

30.1.2.3 Notes. Notes shall be used when it is necessary to highlight an operating procedure, practice or condition.

30.1.3 Diagrams and graphic symbols. Diagrams and graphic symbols shall be in accordance with ANSI Y 14.15, ANSI Y 32.2, and ANSI STD 91.

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40. DETAILED REQUIREMENTS

40.1 Module descriptions. The module descriptions shall have the content and pages in the order specified herein. The parameters and other information shall be complete and compatible with that which is in or will be in the detail specification.

40.1.1 Page numbers. Each page of the module description shall be marked at the bottom center with a module key code and a page number.

40.1.2 Parameters and information. The following is a list of the parameters and information which shall be included in the module description and the contents of each item.

(a) KEY CODE: (Each page of the module description shall be marked in the upper right corner with the module key code).

(b) NAME: (Insert the official module name assigned by the SEM-DRA).

(c) SPEC NUMBER: MIL-M-28787/ (Insert detail specification number).

(d) DESCRIPTION: (Insert a brief functional description).

(e) DESIGN DISCLOSED: /FUNCTIONALLY SPECIFIED: (Place an "X" in the appropriate box).

(f) FAMILY: (Insert appropriate family type, in other words, digital, analog, and so forth).

(g) ORIGINAL TECHNOLOGY: (Insert name of technology used in the original module design, in other words, Schottky TTL, MOS, bipolar, and so forth)..

(h) CIRCUITS PER MODULE: (Insert the number of circuits, components, and so forth, per module).

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(i) MECHANICAL SIZE: (Insert mechanical size and a note if the module extends below the interface plane and a note if holddown screws are used).

(j) MECHANICAL FORMAT: (Insert the applicable module format).

(k) PITCH: (Insert the pitch for the module, if applicable).

(l) CONNECTOR CONTACTS: (Insert the number of connector contacts).

(m) ENVIRONMENT: (Insert appropriate environment class).

(n) POWER DISSIPATION (MAX): (Insert worst case power dissipation as ensured by the detail specification and the applicable power supply voltages).

(o) POWER SUPPLY REQUIREMENTS: (Insert the power supply voltages necessary for module operation and the allowable tolerances of each).

(p) INITIAL DESIGN COG: (Insert the name of the company or activity which is responsible for the initial module design).

(q) APPLICATION INFORMATION: (Insert applications information which is necessary and useful for module users. The information should be concise and for functionally specified modules should be limited to those parameters which will be directly or indirectly ensured by the detail specification or other SEM requirements document. As a minimum the following areas shall be addressed:

(1) Paralleling of outputs, if applicable.

(2) Designation of inputs and outputs exactly as they will appear in the detail specification.

(3) Generic component types.

(4) User application rules: A space of not less than 20 lines shall be left for each user to insert or reference application rules unique to each user application. This should be the last item under APPLICATION INFORMATION).

(r) INPUT - OUTPUT RELATIONSHIP: (Module descriptions for digital modules shall contain truth tables and instruction sets if applicable defining the logical input-output relationship).

(s) CONTACT PROGRAMMING: (If applicable, analog module descriptions shall have contact programming tables or other useful tabulated information.)

(t) SCHEMATIC: (Insert module function diagram figure. This figure shall be a functional block diagram of the module and shall be prepared in accordance with ANSI Y 14.15, using symbols in accordance with ANSI Y 32.14 and ANSI STD 91. The module function diagram figure shall be as it will appear in the detail specification. The designation of inputs and outputs shall be exactly as they will appear in the detail specification. In addition, a figure shall be included showing the module contacts in their relative physical locations as viewed from the bottom of the module and the designation of each including unused contacts. Power supply filter capacitance shall be shown as a single bulk capacitance for each power supply. The value and tolerance as ensured by the detail specification shall be shown for each).

(u) STATIC CHARACTERISTICS: (Insert applicable operating temperature range (NOTE: Values are approximate and will not be finalized until after qualification testing). The static characteristics table shall list all static parameters of interest to module users during selection and design, minimum and maximum end-of-life limits over the operating temperature range, and the units for the limits. Static characteristics should also show significant absolute maximum ratings, such as input breakdown limits. The parameter column shall also show significant conditions under which the limits apply. All limits shall be exactly as they will appear in the detail specification or derived directly from those limits. The limits shall, in general, reflect worst case conditions.)

(v) DYNAMIC CHARACTERISTICS: (Insert applicable operating temperature range (NOTE: Values are approximate and will not be finalized until after qualification testing). The dynamic characteristics table shall list all dynamic parameters of interest to module users during selection and design, minimum and maximum end-of-life limits over the operating temperature range, and the units for the limits. The limits and parameters columns should indicate any significant conditions under which the limits apply. All limits shall be exactly as they will appear in the detail specification or derived directly from those limits. The limits shall reflect worst case conditions.)

(w) WAVEFORMS: (Additional pages may be included for more complex functions. This page shall consist of useful or clarifying graphic representation such as waveforms showing timing relationships and parameter definitions or frequency response curves, and so forth. The title shall be changed to reflect the nature of the information given.)

APPENDIX C

INSTRUCTIONS FOR PREPARING MODULE SPECIFICATIONS

10. SCOPE

10.1 Scope. This appendix is a mandatory part of the standard in the preparation of detail specifications for the SEM program. The information contained herein is intended for compliance. This appendix does not attempt to specify how a module shall be designed or tested, but describes the information that shall be included in the detail specification in conjunction with the requirements specified in the standard and the format for presenting the information.

10.2 Classification. The specifications covered by this appendix shall be of the following types:

Design disclosed specifications.
Functional specifications.

20. APPLICABLE DOCUMENTS.

20.1 Government documents.

20.1.1 Specifications and standards. The following specifications and standards form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DODISS) and supplement thereto, cited in the solicitation.

SPECIFICATIONS

MILITARY

MIL-M-28787/269	-	Modules, Standard Electronic, Amplifier, Differential, Analog, Key Code FGH.
MIL-M-28787/305	-	Modules, Standard Electronic, Controller, Interrupt, Digital, Key Code ZJX.
MIL-M-28787/308	-	Modules, Standard Electronic, Program Control Unit, Key Code MJC.

MIL-M-28787/322	-	Modules, Standard Electronic, Converter, D/A, Key Code DBK.
MIL-M-28787/352	-	Modules, Standard Electronic, Microprocessor Control and Maintenance, Key Code ADP.
MIL-M-28787/353	-	Modules, Standard Electronic, Microprocessor, Key Code NAH.

STANDARDS

MILITARY

DOD-STD-100	-	Engineering Drawing Practices.
MIL-STD-961	-	Military Specifications and Associated Documents, Preparation of.

(Unless otherwise indicated, copies of federal and Military specifications and standards are available from the Naval Publications and Forms Center, (ATTN: NPODS), 5801 Tabor Avenue, Philadelphia, PA 19120-5099).

30. GENERAL REQUIREMENTS

30.1 General requirements. Specifications prepared in accordance with this appendix shall be the documents used for the acquisition and testing of modules. Information, in addition to that required by this appendix, may be added to the detail specification as required for the acquisition and testing of a particular module.

30.1.1 Types of specifications. All military specifications prepared for SEM in accordance with this appendix shall be in accordance with MIL-STD-961. Military specifications required to be design disclosed shall also be in accordance with requirements of this appendix (see 40.). Examples of functional specifications for SEM standard modules (also known as "slash sheets") are MIL-M-28787/269, MIL-M-28787/305, MIL-M-28787/308, MIL-M-28787/352, MIL-M-28787/353, and MIL-M-28787/322. An example of a design disclosed specification is available from the SEM-QAA. Specifications for SEM special modules shall be prepared as bookform drawings on "A" size drawing forms in accordance with DOD-STD-100.

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30.1.2 Style, format, and identification. The style, format, and identification of the detail specification shall be as specified in MIL-STD-961 and this appendix.

30.1.3 Assembly data sheets. Design disclosed specifications shall include following the numbered sections, the assembly, note, and parts list sheets which depict the complete module assembly instructions (see 40.1.1, 40.1.2, and 40.1.3).

40. DETAILED REQUIREMENTS

40.1 Detailed requirements. The requirements and test procedures shall be in accordance with MIL-M-28787 and appendices D and E of this standard.

40.1.1 Assembly sheets. The module assembly sheets shall depict the final assembly, specifying component location and identification, printed wiring boards and module structure.

40.1.2 Note sheets. The note sheets shall contain the notes referenced on the assembly sheets.

40.1.3 Parts list sheets. The parts list sheets shall define the items applicable to the manufacturer of the module. Items are identified by quantity, identification number, and nomenclature. Where applicable, the unit measure, code identification number, reference designation, and mounting hardware item number shall also be specified.

40.1.4 Artwork and schematic. Figures included with the documentation shall include a schematic of the electrical circuit and a pictorial view covering the artwork.

APPENDIX D

TEST REQUIREMENTS FOR DIGITAL MODULES

10. SCOPE

10.1 Scope. This appendix is a mandatory part of the standard in the preparation of detail specifications for digital modules for the SEM. The information contained herein is intended for compliance. This appendix provides a baseline against which new digital module detail specifications are written and reviewed.

20. APPLICABLE DOCUMENT

20.1 Government documents.

20.1.1 Specification. The following specification forms a part of this document to the extent specified herein. Unless otherwise specified, the issue of this document is that listed in the issue of the Department of Defense Index of Specifications and Standards (DODISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

MILITARY

MIL-M-38510	-	Microcircuits, General Specification for.

(Unless otherwise indicated, copies of federal and Military specifications are available from the Naval Publications and Forms Center, (ATTN: NPODS), 5801 Tabor Avenue, Philadelphia, PA 19120-5099.)

30. GENERAL REQUIREMENTS

30.1 General requirements. This appendix shall be used when determining which tests shall be included in the detail specification and how these tests shall be implemented and performed.

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30.1.1 Types of tests. Two types of tests shall be performed by the module supplier. These tests are 100 percent (X) tests which are performed on all modules and sample (S) tests which are performed on 1 percent or a minimum of two modules from each inspection lot and generally includes stress and dynamic tests. Three types of tests are performed by the SEM-QAA. These tests are 100 percent (X) tests, sample (S) tests, and qualification (Q) tests. Qualification tests are generally tests which check the module design such as input capacitance and crosstalk.

30.1.2 Test limits. Test limits shall be as specified in MIL-M-38510 detail specifications or derived from module usage criteria where applicable. When MIL-M-38510 detail specifications do not exist or do not address a particular parameter and module usage criteria is not available, limits shall be as specified in Standard Military Drawings (SMDs) or Defense Electronic Supply Center (DESC) drawings, or the integrated circuit (IC) vendor's specification as available. Limits shall be modified as necessary for special test configurations. When limits are not specified and module usage criteria is not available, engineering judgement and experimental data shall be used to determine the applicable limits.

30.1.3 Logic load circuit. The logic load circuit for 5 volt logic shall be as shown on figure 2. Different loads or modifications of this load may be used where applicable. Use of this load shall be specified for particular tests where applicable.

30.1.4 Order of testing. The order of testing paragraph shall specify that the isolation tests and stress tests shall be performed first in any sequence of tests. During quality assurance inspection testing, the performance of isolation and stress tests shall be followed by all 100 percent (X) tests as a minimum.

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30.1.5 Paralleling of outputs. A paragraph shall appear in each detail specification which states whether or not paralleling of outputs is permissible. If paralleling of outputs is permissible, the paragraph shall specify which outputs can be paralleled and under what conditions they may be paralleled. Outputs that are able to be paralleled for added output drive capability shall be tested by physically shorting the output pins and then testing the shorted pins as a single pin for output voltage low and high level utilizing a load current that is the sum of the specified load current for each of the pins.

30.1.6 Overdriving of active outputs. No overdriving of active outputs shall be allowed during acceptance testing, qualification testing or fault isolation testing.

30.1.7 ESD identification. The detail specification for modules shall contain a paragraph which identifies the classification of ESD for the module.

30.1.8 Powered socket. The detail specification shall contain caution notices of susceptibility to damage for modules containing devices which cannot be protected, by the module design, from removal or insertion into a powered socket.

30.1.9 Operating temperature test conditions. The operating temperature test in MIL-M-28787 shall be performed with the module power supply(s) set at nominal values plus or minus 10 percent. The module shall be conditioned, as closely as possible, to simulate actual module operation. The module outputs shall be loaded as specified in the detail specification. Before starting this test, all 100 percent and nonstress sample tests shall be performed as specified in 30.1.4 using the initial limits at 25 ±5 degrees Celsius (°C) ambient. When electrical testing is called for at the end of each temperature stabilization period, all 100 percent and nonstress sample tests shall be performed as specified in 30.1.4 using the initial limits for the applicable operating temperature. At other times during this test, the module shall be operated as shown on the operating temperature test circuit, shown on each slash sheet.

30.1.10 Component thermal test. The component thermal test shall be performed in accordance with MIL-M-28787. The module shall be operated as shown on the component thermal test circuit.

30.1.11 Life test conditions. The life test in MIL-M-28787 shall be performed with the module power supply(s) set at nominal values plus or minus 10 percent. The module shall be conditioned, as closely as possible, to simulate actual module operation. The module outputs shall be loaded as specified in the detail specification. Following the life test and while still at the maximum class temperature, all 100 percent and nonstress sample tests shall be performed as specified in 30.1.4 using the operating temperature end-of-life requirements. Following the return of the module to 25°C, all 100 percent and nonstress sample tests shall be performed as specified in 30.1.4 using the 25 ±5°C ambient end-of-life requirements.

30.1.12 Vibration test conditions. The vibration test in MIL-M-28787 shall be performed with the module power supply(s) set at nominal values plus or minus 10 percent. The outputs shall be open (no load) and the inputs may be connected to a low level, high level, or open circuit. Following the vibration tests, all 100 percent tests and the power supply filter capacitance test, as applicable, shall be performed using the initial limits at 25 ±5°C ambient.

30.1.13 Thermal shock. The thermal shock test shall be performed in accordance with MIL-M-28787. No power shall be applied during this test.

30.1.14 Detail specification title. Detail specifications for digital modules shall indicate in the title that the detail specification covers a digital module.

30.1.15 Test tables. Test tables are used to convey necessary information. Figures 3 and 4 are examples of test tables used for an input test and figures 5 and 6 are examples of test tables used for an output test.

30.1.16 Test figures. Test figures are used to convey test setup information or to clarify a test. Their use shall be limited to these areas.

30.1.17 Functional block diagram. A block diagram conveys needed information on the flow of signals. A sample module functional block diagram is shown on figure 7.

40. DETAILED REQUIREMENTS

40.1 Detailed requirements. The following tests, or a subset based on module function or application, shall be performed on all digital modules. Other tests may be added as necessary to characterize the module function.

40.1.1 100 percent tests. These tests shall be performed on all modules during 25°C acceptance testing. All of these tests shall be performed unless otherwise specified.

40.1.1.1 Used-to-unused contact isolation. If the module has unused contacts, this test shall be performed to insure that no continuity exists between used and unused contacts. No power shall be applied to the module and the isolation shall be checked using a megohm bridge with the bridge voltage set at 30 volts direct current (Vdc) plus or minus 10 percent. The minimum initial limits shall be 10 megohms and the minimum end-of-life limits shall be 1 megohm.

40.1.1.2 Unused to unused contact isolation. If the module has unused contacts, this test shall be performed to insure that no continuity exists between individual unused contacts. No power shall be applied to the module and the isolation shall be checked using a megohm bridge with the bridge voltage set at 30 Vdc plus or minus 10 percent. The minimum initial limits shall be 10 megohms and the minimum end-of-life limits shall be 1 megohm.

40.1.1.3 Continuity. The following continuity tests shall be performed when applicable.

(a) Ground (zero-volt reference) contact. If the module has multiple ground contacts which are internally tied together, this test shall be performed to insure that the connections exist. No power shall be applied to the module and the continuity shall be checked using an ohmmeter. The limits shall be zero-ohm minimum and 1 ohm maximum.

(b) Power supply contact. If the module has multiple power supply contacts which are internally tied together, this test shall be performed to insure that the connections exist. No power shall be applied to the module and the continuity shall be checked using an ohmmeter. The limits shall be zero-ohm minimum and 1 ohm maximum.

40.1.1.4 Input current. The following input current tests shall be performed when applicable.

(a) Input current (high level). Power supply voltage shall be maximum. The input test voltage shall be equal to that specified in the MIL-M-38510 detail specification or equivalent for the particular device family. The other inputs to the module under test shall be conditioned to force maximum leakage current into the input under test with all other inputs connected to zero-volt in order to check for module input contact to input contact shorts where feasible. The conditioning voltages shall be typical low level and high level values. For 5-volt logic these values are zero-volt and 3-volt, respectively. Every module input shall be tested individually. The purpose of this test is to ensure worse case high level input current loading. The limits shall be determined from the MIL-M-38510 detail specification, the SMDs or DESC drawings, or the IC vendor's specification, or from module usage. Device parameters may be grouped for similar device families.

(b) Input current (low level). Power supply voltage shall be maximum. The input test voltage shall be equal to that specified in the MIL-M-38510 detail specification or equivalent for the particular device family. The other inputs to the module under test shall be conditioned to force maximum current out of the input under test. The conditioning voltages shall be typical 5-volt logic values. Every module input shall be tested individually. The purpose of this test is to ensure worst case low level input current loading. The limits shall be determined from the MIL-M-38510 detail specification, the SMDs or DESC drawing, or the IC vendor's specification or from module usage. Device parameters may be grouped for similar device families.

40.1.1.5 Output leakage current. The following output leakage current tests shall be performed on three-state and open-collector outputs when applicable.

(a) Three-state outputs, high impedance leakage current (high level). Power supply voltage shall be maximum. The inputs shall be conditioned so that the output under test is at a high impedance. The conditioning voltages shall be typical 5-volt logic values. A voltage shall be applied to the output and the current shall then be measured. The voltage applied to the output shall be equal to-that specified in the MIL-M-38510 detail specification or IC vendor specification for the particular device family. The purpose of this test is to ensure worst case high impedance high level output loading. The limits shall be determined from the MIL-M-38510 detail specification, the SMDs or DESC drawings, or the IC vendor's specification, or from module usage. Device parameters may be grouped for similar device families.

(b) Three-state outputs, high impedance leakage current (low level). Power supply voltage shall be maximum. The inputs shall be conditioned so that the output is at a high impedance state. The conditioning voltages shall be typical 5-volt logic values. A voltage shall be applied to the output and the current shall then be measured. The voltage applied to the output shall be equal to that specified in the MIL-M-38510 detail specification or IC vendor specification for the particular device family. The purpose of this test is to ensure worst case high impedance low level output loading. The limits shall be determined from the MIL-M-38510 detail specification, the SMDs or DESC drawings, or the IC vendor's specification, or from module usage. Device parameters may be grouped for similar device families.

(c) Open-collector outputs. Power supply voltage shall be maximum. The inputs shall be conditioned so that the output is in the off state. The conditioning voltages shall by typical 5-volt logic values. The maximum power supply voltage shall be applied to the output and the current into the output shall then be measured. The voltage applied to the output may be greater than the maximum power supply voltage depending on the module application. The purpose of this test is to ensure worst case open-collector leakage current. The limits for open-collector leakage current shall be determined from the MIL-M-38510 detail specification, the SMDs or DESC drawings, or the IC vendor's specification, or from module usage. Device parameters may be grouped for similar device families.

40.1.1.6 Output voltage. The following output voltage tests shall be performed when applicable.

(a) Output voltage (high level). Power supply voltage shall be minimum. The inputs shall be conditioned to force a high level at the output. The conditioning voltages shall be threshold values for the particular device family. (For example, for TTL, $V(_{IL})$ = 0.8V and $V(_{IH})$ = 2.0V.) The output under test shall be loaded with the applicable logic load

circuit for the particular output. In the event of a common output node (multiple device outputs brought out to a common module contact), all outputs connected to the node shall be tested for output voltage high level. The limits shall be determined from the MIL-M-38510 detail specification, the SMDs or DESC drawings, or the IC vendor's specification, or from module usage. Device parameters may be grouped for similar device families.

(b) Output voltage (low level). Power supply voltage shall be minimum. The inputs shall be conditioned to force a low level at the output. The conditioning voltages shall be threshold values for the particular device family. (For example, for TTL, $V(_{IL})$ = 0.8V and $V(_{IH})$ = 2.0V.) The output under test shall be loaded with the applicable logic load circuit for the particular output. In the event of a common output node (multiple device outputs brought out to a common module contact), all outputs connected to the node shall be tested for output voltage low level. The limits shall be determined from the MIL-M-38510 detail specification, the SMDs or DESC drawings, or the IC vendor's specification, or from module usage. Device parameters may be grouped for similar device families.

40.1.1.7 Power supply current. Power supply voltage shall be maximum. The tests shall be performed with the outputs not loaded. The power supply current shall be tested as follows:

(a) Quiescent power supply current. All inputs shall be conditioned such that the module draws maximum power supply current. The conditioning voltages shall be typical 5 volt logic levels. The inputs shall be static values when the current level is measured.

(b) Operating power supply current. The operating power supply current shall be measured while the module is functioning at the maximum clock frequency using the functional vector set or a portion thereof such that the module draws maximum power supply current.

(c) Power down power supply current. If the module has a powered down state where the quiescent power supply current is reduced when the module is disabled, the power supply current shall be measured for this condition also. The inputs shall be at static levels when the current is measured.

40.1.1.8 Functional tests. The functional tests shall depend on the type of circuit to be tested. All small and medium function modules shall be tested as specified in 40.1.1.8(a) while all large function modules shall be tested as specified in 40.1.1.8(b). The decision of whether a module is a small, medium or a large function module shall be made by the SEM-QAA and implemented in the detail specification.

If a clock pulse is necessary to perform the functional tests, the logic levels of the clock pulse shall be at threshold values. The clock pulse dynamic parameters shall be specified to allow functional tests to be performed on automatic testing equipment. Verification of the output patterns shall be accomplished by monitoring the outputs and comparing the results with the guaranteed output low and high levels. The tests in the detail specification shall be written using this method; however, equivalent methods may also be employed when performing the actual tests.

(a) Functional test for small and medium function modules. Functional tests shall achieve minimum fault detection levels as required in table I. The vectors shall be derived from the actual gate implementation of the circuits used in the module. Power supply voltage shall be minimum. Input conditioning voltages shall be threshold values. All vectors necessary to perform the functional tests shall be included in the detail specification test table and the test table shall contain both the input and output patterns for each vector.

(b) Functional test for large function modules (capacitive load only). The module shall be tested at both minimum and maximum power supply levels. The functional vector set shall achieve minimum fault detection levels as required in table I. The vectors shall be executed at the maximum module clock frequency and, where applicable (dynamic devices), at the minimum clock frequency, with a defined capacitive load per output. The input voltages shall be input threshold levels for the particular device family (for example, for TTL, V_{IH} = 2.0V and V_{IL} = 0.8V) and the output compare levels shall be V_{OL} maximum and V_{OH} minimum for the particular device family (for example, for TTL, the V_{OL} maximum = 0.4V and V_{OH} minimum = 2.4V). Modules, or portions of modules, which contain ordered structures such as memories, may be functionally tested using appropriate algorithms such as walking ones-and-zeroes. Some modules, or individual components within modules, may be of a very high complexity and it may be considered impossible or prohibitively expensive to perform gate level modeling simulation, or fault grading. With prior approval of the SEM-QAA only, a functional approach to test generation may be used. Using functional modeling and simulation techniques, an in-depth functional test shall be generated to exercise the individual components or the module function in each of its operating modes. This test approach shall be based on functional and timing requirements of the system application. The tests shall include, but shall not be limited to, exercising each instruction of its instruction set, if applicable, writing and reading from each register, verifying all addressing, and so forth. A proposed test plan shall be submitted to the SEM-QAA for review prior to starting test pattern development. Documentation of the final pattern set shall include a detailed description of the operations or modes being exercised throughout the test pattern set. Final acceptance of the test pattern set shall require review and approval by the SEM-QAA.

APPENDIX D

TABLE I. Functional test pattern coverage.

Fault condition	Universe considered	Minimum required fault detection 1/	
		Small and med. function (40.1.1.8(a)) (percent)	Large function (40.1.1.8(b)) (percent)
SA1/0	Internal primitive 2/ outputs	100	95
SA1/0	Internal primitive 2/ inputs	100	95
SA1/0	IC output contacts	100	99
SA1/0	IC input contacts	100	99
SA1/0	Module output contacts	100	100
SA1/0	Module input contacts	100	100
Shorts	Module contact-to-contact physically adjacent	100	100

1/ The minimum required fault detection is specified for the total module composite of all detectable faults for each type of universe considered.

2/ Primitive for small and medium function modules is defined as the gate. Primitive for large function modules is defined as a simulation primitive such as a logic gate, exclusive OR/NOR, memory or data latch, or other primitive of similar complexity, but not greater in complexity than a J-K or D-type flip-flop.

40.1.2 Sample tests. These tests shall be performed on 1 percent or a minimum of two modules from each inspection lot during 25°C acceptance testing. All of the following tests shall be performed unless otherwise specified.

40.1.2.1 Frame isolation. Frame isolation shall be the first test performed. This test is performed to ensure that isolation exists between the module frame and all module contacts. No power shall be applied. Isolation shall be checked using a megohm bridge with a test voltage of 100 Vdc plus or minus 10 percent. The minimum initial limit shall be 10 megohms and the minimum end-of-life limit shall be 1 megohm.

40.1.2.2 Power supply stress check. This is a maximum stress test and is performed to ensure that the module is not damaged by overvoltage. Power supply voltage shall be absolute maximum. The module shall be in a known state. There shall be no measurement taken. The module shall pass all remaining tests.

40.1.2.3 Input breakdown current. This test is a maximum stress test and is performed to ensure that the inputs to the module are not damaged or destroyed when the absolute maximum input voltage is applied. Power supply voltage shall be maximum. The absolute maximum input voltage shall be applied to each input individually and the input leakage current shall then be measured. The minimum limit shall be zero milliamperes and the maximum limit shall be as specified in the MIL-M-38510 detail specification, the SMDs or DESC drawings, or the IC vendor's specification. Device parameters may be grouped for similar device families.

40.1.2.4 Output short circuit current. This test is a maximum stress test and is performed to ensure that the module outputs are not damaged when shorted to the zero-volt reference. Power supply voltage shall be maximum. The inputs of the module under test shall be conditioned to force a high level voltage at the output. The conditioning voltages shall be typical 5-volt logic values. One output at a time shall be tested by shorting to the zero-volt reference and then measuring the current. A

maximum allowable shorting time shall be specified to prevent damage to the output. The limits shall be as specified in the MIL-M-38510 detail specification, the SMDs or the DESC drawings, or the IC vendor's specification. In the event of a common node, all outputs connected to the node shall be tested for output short circuit current.

40.1.2.5 Input clamp diode voltage. The purpose of this test is to ensure the existence of clamp diodes on the inputs of the module. The power supply voltage shall be minimum. The test shall be performed by forcing maximum current through the clamp diode and measuring the voltage across the diode. CAUTION: This test should not be performed on modules which do not have clamp diodes. Device parameters may be grouped for similar device families.

40.1.2.6 Functional tests for large function modules (current and capacitive load). The functional vector set shall achieve minimum fault detection levels as required in table I. Alternate methods shall be approved in advance. The vectors shall be executed with the outputs fully loaded with current and capacitance. The patterns and test program used for dynamic functional tests shall guarantee the dynamic parameters required by the module specification by verification or measurement techniques. The patterns shall apply and propagate signals in all module or component operating modes, through all bus, data, and control paths, in each logic state, and for all specified inputs and outputs necessary to guarantee that all of the dynamic parameters are met under all possible logic conditions. Testing can be limited to worst-case situations (for example, operating modes and propagation paths) if they can be identified. The conditions tested shall guarantee module specification values for all other untested situations. The verification method of testing is preferred over the one-time measurement method, except where data is required. When verification is used, parameters shall be verified as often, and under as many different logic conditions throughout the pattern as possible. In other words, it will not be acceptable to verify a parameter at only one place in a pattern if it could reasonably have been verified throughout, or in several places in the pattern. The functional test shall test for the following items, with items (a) through (d) being tested simultaneously.

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(a) Input voltage levels. The input voltage levels shall be V_{OL} maximum and V_{OH} minimum for the particular device family. (For example, for TTL, V_{OL} maximum = 0.4V and V_{OH} minimum = 2.4V.)

(b) Output voltage check. The output compare levels shall be the minimum output high voltage level and the maximum output low voltage level.

(c) Power supply margins. The modules shall be tested using the minimum and maximum power supply levels.

(d) Clock frequency. The functional vector set shall be tested using the maximum clock frequency, and where applicable (dynamic devices), with the minimum clock frequency. The maximum and minimum clock frequencies are the maximum and minimum possible frequencies of operation in any application.

(e) Minimum setup and hold times. Setup and hold times shall be tested on all applicable module contacts to guarantee module operation. The setup and hold times shall be derived from the IC vendor's specification or module usage criteria.

(f) Maximum propagation delay time check. The propagation delay time check verifies that the module outputs are in valid states within the maximum propagation delay time. The propagation delay times shall be derived from the IC vendor's specification or module usage.

(g) Enable and disable delay time check. The enable and disable delay time check (t_{PZL}, t_{PZH}, t_{PLZ}, t_{PHZ}) verifies that the module's three-state outputs are in their proper states within the maximum enable or disable delay time. The enable and disable delay times shall be derived from the IC vendor's specification or module usage criteria.

Items (e) and (f) may be tested during the functional test or as a separate test. When testing items (d), (e), or (f), items (a), (b), and (c) shall also be performed. The waveforms (input and output) necessary to perform the tests shall be included on a figure. All measurement points (voltage and tolerance) shall be shown on the waveforms along with the necessary tolerances. The waveforms shall be drawn to a reasonable scale. Any information that clarifies the waveforms or the test shall be included as notes on the figure. Examples of input and output waveforms are shown on figures 8 and 9. The input pulses shall have the following parameters specified: pulse repetition period (PRP) in time units; pulse width (PW) in time units; transition times (t_{TLH} and t_{THL}) in time units; pulse amplitude (PA) in voltage units; pulse low level in voltage units; voltage reference points (V_{REF}) in voltage units; overshoot and undershoot in voltage units; and time relationships between input pulses.

40.1.2.7 Output pulse characteristics. These are dynamic tests (transition times, propagation delay times, setup and hold times, and so forth) which are generally performed on small and medium function modules. Output pulse characteristics shall be tested as required to ensure proper module operation. The following input pulse parameters shall be specified, where applicable, when performing the dynamic tests: pulse repetition period (PRP) in time units; PW in time units; t_{TLH} and t_{THL} in time units; PA in voltage units; pulse low level in voltage units; V_{REF} in voltage units; overshoot and undershoot in voltage units; and time relationship between multiple input pulses when more than one input pulse is necessary to perform a test. The waveforms (input and output) necessary to perform the tests shall be included on a figure. All measurement points (voltage and tolerance) shall be shown on the waveforms along with the necessary tolerances. The waveforms shall be drawn to a reasonable scale. Any information that clarifies the waveforms or the tests shall be included as notes on the figure.

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(a) Output transition times (t_{TLH} and t_{THL}). Power supply voltages shall be typical. These tests shall be performed using the logic load circuit with a defined load capacitance. These tests shall be performed a minimum of one time on each output. The reference measurement points can be either voltage points or percentage points. In the event of a common output node, all outputs connected to the node shall be tested. Maximum limits shall be derived from engineering judgement, experimental data or module usage. Minimum limits shall be determined by engineering judgement and experimental data considering system wiring rules and noise susceptibility of the logic devices.

(b) Output propagation delay times (t_{PLH} and t_{PHL}). Power supply voltages shall be typical. These tests shall be performed using the logic load circuit with a defined load capacitance. Unused inputs to the circuit under test shall not be left open, but shall be connected to an applicable high or low voltage level. The propagation delay times (t_{PLH} and t_{PHL}) shall be measured from each input to every output which is controlled by that input. The tests shall be written from the gate level representation of the device under test and each internal gate shall be exercised a minimum of one time. The output under test and any output which affects the output under test shall be loaded. Maximum limits shall be as specified in MIL-M-38510, the SMDs or DESC drawings, or the IC vendor's specification, or module usage with corrections for test configuration and load. Minimum limits shall be determined by engineering judgement and experimental data considering system wiring rules and noise susceptibility of the logic devices.

(c) Maximum clock frequency and minimum clock pulse width. Power supply voltage shall be typical. These tests shall be performed simultaneously with the maximum input repetition rate and the minimum pulse width being applied to the clock input and the output repetition period or pulse width being measured to verify the setup. These tests shall be performed using the logic load circuit with a defined load capacitance. Clock input requirements shall be

obtained from the detailed slash sheet of MIL-M-38510, the SMDs or DESC drawings, or the IC vendor's specification, or module usage where applicable. Test limits shall be based on the input setup when measuring the output pulse period or pulse width.

(d) Setup and hold times. Definition of setup and hold times shall be as follows:

(1) Setup time: The minimum time before the triggering edge of the clock pulse that data must be present on an input to be recognized as valid data.

(2) Hold time: The minimum time after the triggering edge of the clock pulse that data must be present on an input to be recognized as valid data.

The minimum input setup and hold time requirements shall be obtained from MIL-M-38510, the SMDs or DESC drawings, or the IC vendor's specification, or module usage. Power supply voltage shall be typical. The logic load circuit shall be used with a defined load capacitance. The minimum setup and hold times shall be verified by adjusting the time relationship between the data input and the clock input and measuring the output period or pulse width.

(e) Minimum pulse width and recovery time for asynchronous inputs. These tests may be performed simultaneously, if possible, and may be incorporated in the propagation delay time tests. Recovery time is defined as the minimum time required between the trailing edge of an asynchronous pulse and the triggering edge of the clock pulse for data to be recognized and transferred to the output.

Power supply voltage shall be typical. The output under test shall be loaded with the logic load circuit using a defined load capacitance. If these tests are incorporated in the propagation delay time tests, the measurement of the propagation delay time shall verify the minimum pulse width or recovery time. If these tests cannot be incorporated in the delay time tests, verification can be made by measuring the output period or pulse width. Limits shall be obtained from MIL-M-38510, the SMDs or DESC drawings, or the IC vendor's specification, or module usage.

40.1.2.8 Power supply filter capacitance. This test verifies the value of the bulk power supply capacitor. This test shall be performed using a capacitance bridge at a frequency of 1 kilohertz (kHz) and a voltage of 0.3 volt peak maximum. The limits shall be plus or minus 30 percent of the nominal capacitance value.

40.1.3 Qualification tests. These tests shall be performed during qualification testing only.

40.1.3.1 Input capacitance. No power shall be applied. The capacitance from each input to the zero-volt reference shall be measured on each input individually. The minimum limit for a single input shall be 1 picofarad (pF) and the maximum limits shall be derived from engineering judgement, experimental data, and module usage.

40.1.3.2 Output capacitance. No power shall be applied. The capacitance from each output to the zero-volt reference contact shall be measured on each output individually. The minimum limit for a single output shall be 2 pF and the maximum limits shall be derived from engineering judgement, experimental data, and module usage.

40.1.3.3 Power supply transient amplitude. The purpose of this test is to verify the ability of the module to operate under and suppress high frequency transients induced during module operation. Power supply voltage shall be typical. The module shall be conditioned for maximum power supply current switching on the module. The power supply contact shall be monitored and the amplitude of the most negative or positive spike (as applicable) shall be measured from the steady state power supply baseline. The test shall be performed with no outputs loaded. The minimum limit shall be zero-volt and the maximum limit shall be determined from engineering judgement and experimental data.

40.1.3.4 Output crosstalk tests. These tests check the circuits and the circuit board layout for noise generated by the circuits switching.

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(a) Output crosstalk (high level). Power supply voltage shall be typical. All outputs shall be loaded with the logic load circuit and a defined load capacitance. The inputs shall be conditioned so that the output under test is at a stable high level and as many other outputs as possible are switching. Input conditioning voltages shall be typical 5-volt logic values. The input pulse amplitudes shall be typical 5-volt logic values. The amplitude of the most negative spike on the output under test shall be measured from the high level voltage baseline to the most negative peak. Power supply noise may be filtered with external capacitors to assure that the measurement is output crosstalk. Minimum limits shall be zero-volt. Maximum limits shall be determined from engineering judgement and experimental data. Noise margins shall be a prime consideration when specifying maximum limits.

(b) Output crosstalk (low level). Power supply voltage shall be typical. All outputs shall be loaded with the logic load circuit and a defined load capacitance. The inputs shall be conditioned so that the output under test is at a stable low level and as many other outputs as possible are switching. Input conditioning voltages shall be typical 5-volt logic values. The input pulse amplitudes shall be typical 5-volt logic values. The amplitude of the most positive spike on the output under test shall be measured from the low level voltage baseline to the most positive peak. Power supply noise may be filtered with external capacitors. Minimum limits shall be zero-volt. Maximum limits shall be determined from engineering judgement and experimental data. Noise margins shall be a prime consideration when specifying maximum limits.

(c) Output crosstalk for maximum noise margin (low level and high level). When experimental data on crosstalk for a module is below 500 millivolts (mV) for Schottky TTL or below 400 mV for TTL, low power Schottky TTL, and low power TTL, the maximum limit shall be appropriately 500 mV or 400 mV. If a module exceeds the 400 mV or 500 mV limit and it is determined to have the best possible design for factors affecting crosstalk, one of the following methods will be used to guarantee maximum noise margin.

(1) Nonclocked functions. For nonclocked functions, the crosstalk is attributed to outputs switching within an IC package. The test for these functions will have fewer outputs switching. This is usually accomplished by having all the outputs of one IC quiet with all others switching. Nonclocked function test is in addition to those of 40.1.3.4(a) and 40.1.3.4(b), and shall be employed only when the module design is determined to be the best possible.

(2) Clocked functions. For clocked functions, the data on any output is not valid until after the maximum propagation delay time from the clock. These modules are tested with all outputs switching. Measurements are taken after the maximum propagation delay time. Clocked function test is in addition to those of 40.1.3.4(a) and 40.1.3.4(b), and shall be employed only when the module design is determined to be the best possible.

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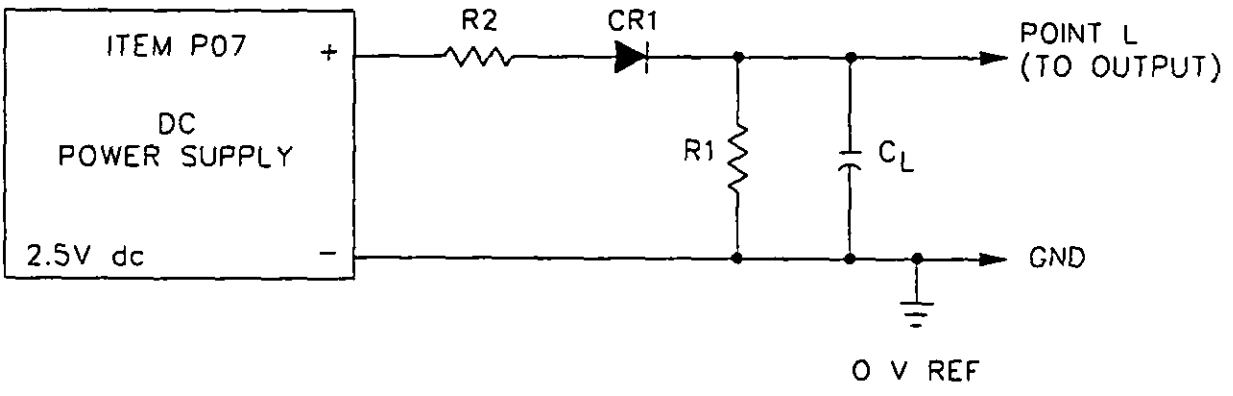

NOTES:

1. CR1 = IN_____, or equivalent.
2. R1 = _____ plus or minus 1 percent (insert power rating). The value of R1 should be selected to give maximum high-level drive current with point L held at (insert the minimum high-level voltage) volts.
3. R2 = Select value for a current flow of (insert maximum low-level drive current) plus or minus 5 percent out of point L with point L held at (insert maximum low-level output voltage) volts.
4. C_L = 50 plus or minus 5 pF (including probe and parasitic capacitance) as specified in individual detail specifications.
5. C_L = 150 plus or minus 15 pF (including probe and parasitic capacitance) as specified in individual detail specifications.
6. C_L = 300 plus or minus 30 pF (including probe and parasitic capacitance) as specified in individual detail specifications.
7. C_L is not required in performing direct current (dc) electrical tests.

FIGURE 2. Logic load circuit.

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TABLE ( ). Input current (low-level) test.

Test condition	Signal name	Contact number	25 ±5°C Initial limits		Units	Notes
			Min	Max		

FIGURE 3. Example of an input test condition test table.

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TABLE ( ). Input current (low-level) test tolerance table.

Condition	Value	Accuracy	Current limit	Test condition
Power supply				
Forcing voltage (V_{IL}) Forcing voltage (V_{IL})				
Pattern voltage HIGH (V_H) LOW (V_L)				
Input current measurement Input current measurement Input current measurement Input current measurement Input current measurement				

FIGURE 4. Example of an input test condition test tolerance table.

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TABLE ( ). Output voltage (high-level) test.

Test condition	Signal name	Contact number	25 ±5°C Initial limits		Units	Notes
			Min	Max		

FIGURE 5. Example of an output test condition test table.

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TABLE ( ). Output voltage (high-level) test tolerance table.

Condition	Value	Accuracy	Current limit	Test condition
Power supply				
Forcing current (I_{OH}) Forcing current (I_{OH})				
Pattern voltage HIGH (V_H) LOW (V_L)				
Output voltage measurement				

FIGURE 6. Example of an output test condition test tolerance table.

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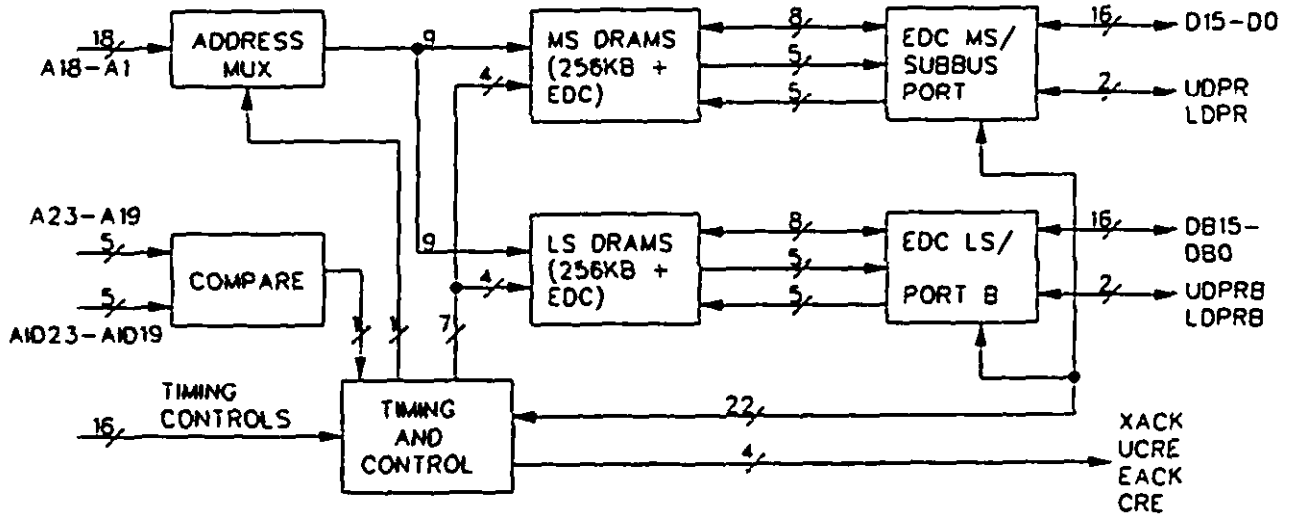

FIGURE 7. Example of a module functional block diagram.

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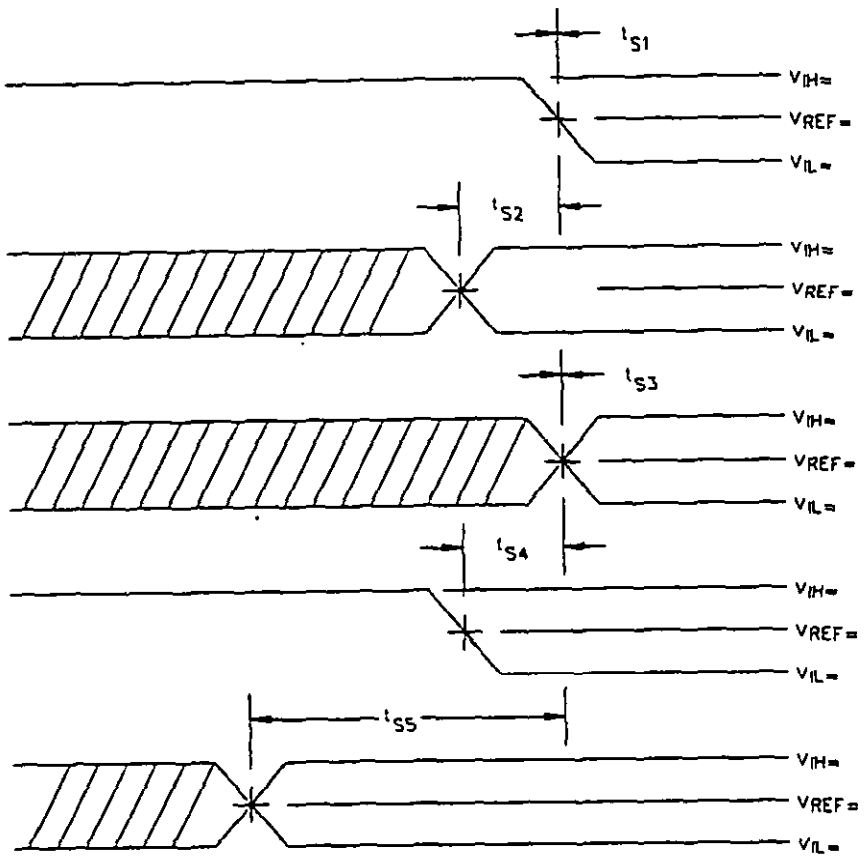

FIGURE 8. Example of input waveforms.

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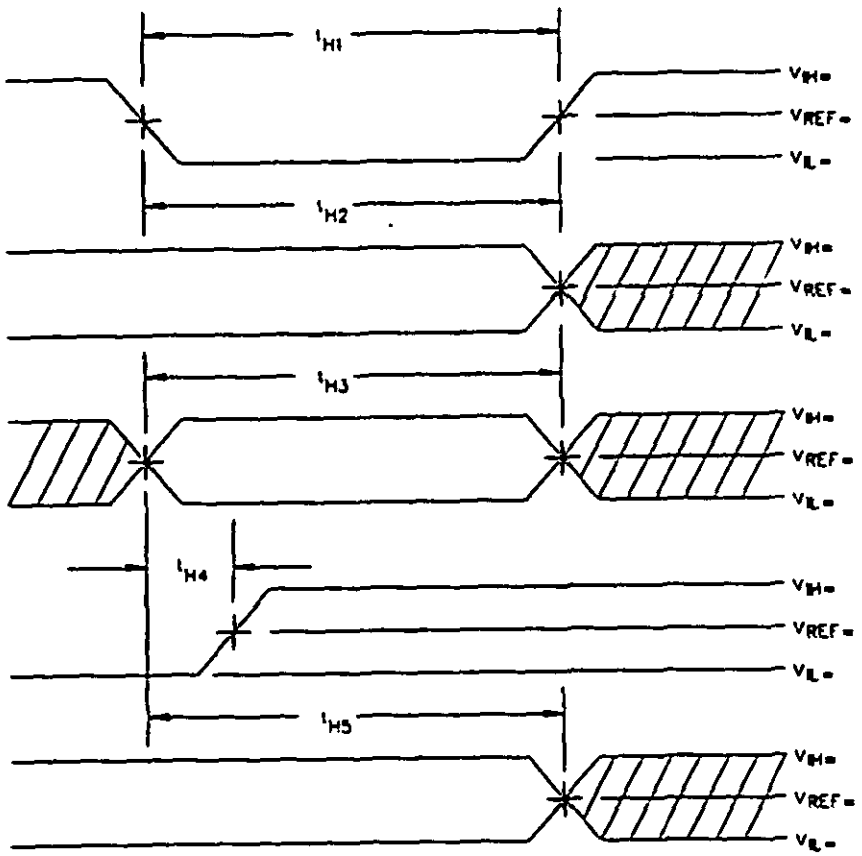

FIGURE 8. Example of input waveforms - Continued.

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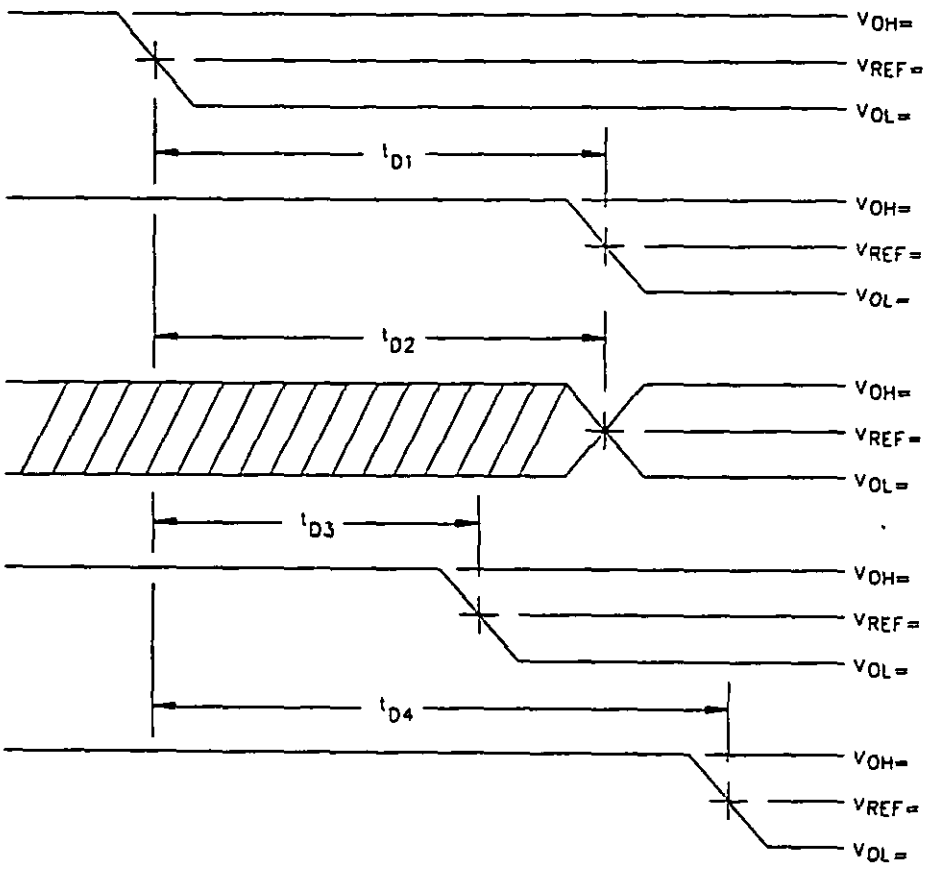

FIGURE 9. Example of output waveforms.

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TEST REQUIREMENTS FOR ANALOG MODULES

10. SCOPE

10.1 Scope. This appendix is a mandatory part of the standard in the preparation of detail specifications for analog modules for the SEM. The information contained herein is intended for compliance. This appendix provides a baseline against which new analog module detail specifications are written and reviewed.

20. APPLICABLE DOCUMENTS

20.1 Government documents.

20.1.1 Standards. The following standard forms a part of this appendix to the extent specified herein. Unless otherwise specified, the issue of this document is that listed in the issue of the Department of Defense Index of Specifications and Standards (DODISS) and supplement thereto, cited in the solicitation.

STANDARD

MILITARY

MIL-STD-202	-	Test Methods for Electronic and Electrical Component Parts.

(Unless otherwise indicated, copies of federal and Military standards are available from the Naval Publications and Forms Center, (ATTN: NPODS), 5801 Tabor Avenue, Philadelphia, PA 19120-5099.)

30. GENERAL REQUIREMENTS

30.1 General requirements. This appendix shall be used when determining which tests shall be included in the detail specification and how these tests shall be implemented and performed.

30.1.1 Types of tests. There are two types of tests performed by the module supplier. These tests are 100 percent (X) tests which are performed on all modules and are generally static tests and sample (S) tests which are performed on 1 percent or a minimum of two modules from each inspection lot and generally include stress and dynamic tests. There are three types of tests performed by the SEM-QAA. These tests are 100 percent (X) tests, sample (S) tests, and qualification (Q) tests. Q tests are generally tests which check the module design such as input capacitance and crosstalk.

30.1.2 Test limits. Test limits shall be as specified in the component's Military specification such as MIL-M-38510 detail specification, SMDs or DESC drawings. When component Military specifications do not exist or do not address a particular parameter, limits shall be as specified in the component vendor's specifications. These limits shall be modified as necessary for special test configurations. When limits are not specified in the Military specification or the vendor's specification, engineering judgement and experimental data shall be used to determine the applicable limits. All tests shall have minimum and maximum limits specified.

30.1.3 Order of testing. The order of testing paragraph shall specify that the isolation tests and stress tests shall be performed first in any sequence of tests. During quality assurance inspection testing, the performance of isolation and stress tests shall be followed by all 100 percent (X) tests as a minimum.

30.1.4 Detail specification title. Detail specifications for analog modules shall indicate in the title that the detail specification covers an analog module.

40. DETAILED REQUIREMENTS

40.1 Detailed requirements. Unless otherwise specified, the following tests shall be performed on all analog modules. Other tests not listed may be added if they are necessary to characterize the module function.

40.1.1 Unused contact and circuit isolation. If the module has unused contacts, this test shall be performed to ensure isolation between used and unused contacts and between individual unused contacts. It shall also be performed to ensure isolation between circuits which have no common connections. No supply voltage shall be applied to the module. Isolation shall be checked using a megohm bridge with the voltage set according to the module working voltage (see table II).

TABLE II. Working voltage versus test voltage.

Module working voltage	Test voltage
0 to 25 V	100 Vdc ±10%
25 to 50 V	200 Vdc ±10%
50 to 100 V	500 Vdc ±10%

The minimum initial limit shall be 10 megohms and the minimum end-of-life limit shall be 1 megohm. This is a stress test but shall be 100 percent tested and one of the first tests run.

40.1.2 Contact-to-contact continuity. If the module has multiple ground contacts or other contacts which are internally tied together, this test shall be performed to ensure that the connections exist. No supply voltage shall be applied to the module. The continuity shall be checked using an ohmmeter. The minimum limits shall be zero-ohm and the maximum limit shall be 1 ohm. This test shall be a 100 percent test. If a tighter limit of 0.1 ohm is required, it may be specified either as a 100 percent test, sample test, or as a qualification test depending on the application.

40.1.3 Frame isolation. This test shall be performed to ensure that the proper isolation exists between the module frame and all the module contacts except the frame ground contact. No supply voltage shall be applied to the module. The isolation shall be checked using a megohm bridge with the bridge voltage set according to table II. The minimum initial limit shall be 10 megohms and the minimum end-of-life limit shall be 1 megohm. This test is a stress test and shall be the first test performed. This shall be a sample test.

40.1.4 Frame continuity. If the module has a frame ground contact, the continuity shall be checked between this contact and the module frame. No supply voltage shall be applied to the module. The continuity shall be checked using an ohmmeter. The minimum limit shall be zero-ohm and the maximum limit shall be 1 ohm. This shall be a sample test.

40.1.5 Power supply current. This test shall be a 100 percent test for modules with a maximum power dissipation greater than 1 watt and a sample test for modules with a maximum power of 1 watt or less. This test shall be performed with no load on the module and the module conditioned to draw maximum supply current. The supply voltage shall be at the maximum value.

40.1.6 Power supply filter capacitor. This test ensures the presence of a decoupling capacitor in the module. It is performed using a capacitance bridge at 1 kHz, 0.3 volt peak maximum, and in the parallel mode. A test frequency of 120 hertz (Hz) shall be used for tantalum capacitors unless other module circuitry is adversely affected. The limit for both shall be plus or minus 30 percent of the nominal capacitance value across all temperatures and through life. This shall be a 100 percent test.

40.1.7 Operating temperature and life test. The module shall be subjected to operating temperature and life tests as specified in MIL-M-28787. The module shall be operated so that maximum allowed power is dissipated by the module. The power supply voltages shall be maximum. The input signal and module loads shall be specified to obtain the maximum allowed power dissipation. The detail specification shall include the necessary test figures.

40.1.8 Vibration test. The module shall be subjected to vibration testing as specified in MIL-M-28787. The required power supplies shall be at nominal voltage plus or minus 10 percent and no signal shall be applied except when necessary to ensure validity of the test. Passive modules shall be operated in the same configuration as for operating temperature. The detail specification shall include the necessary test figure.

40.1.9 Power socket caution. The detail specifications shall contain caution notices of susceptibility to damage for modules containing devices which cannot be protected, by the module design, from removal or insertion into a powered socket.

40.1.10 Output short circuit. Each output shall withstand a short circuit to zero volt potential for not less than 1 second. A caution shall be included in the detail specification for all outputs which are not short circuit protected.

40.2 Parametric tests. Each module shall be tested to the lowest possible functional level. All tests for each type of analog module shall be performed to the maximum extent possible.

40.2.1 Operational amplifiers. The following tests shall be performed on operational amplifier modules when applicable.

40.2.1.1 Input offset voltage (V_{IO}). The supply voltage shall be maximum. The module shall be operated in a circuit similar to that shown on figure 10 (the resistor values may change depending on the characteristics of the operational amplifier) and the output voltage level shall be measured. This shall be a 100 percent test.

40.2.1.2 Average offset voltage temperature sensitivity. This parameter is obtained by calculation from offset voltage readings at the temperature extremes of the module (0 and 60°C for class I modules). The equation is as follows:

$$\text{Offset voltage temperature sensitivity} = \frac{\Delta V_{IO}}{\Delta T}$$

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This shall be a qualification test. It should be noted that the actual offset voltage temperature sensitivity over short temperature ranges within the range of temperature extremes could vary considerably from the average sensitivity obtained with this test. However, due to the difficulty of testing short range sensitivity, it is not recommended as a test unless absolutely necessary.

40.2.1.3 Input offset current (I_{IO}). This parameter is a measure of the difference in bias current required between each input of the operational amplifier. This parameter gives an indication of the effect of different source resistances on the offset voltage. Since this parameter is calculated from the offset voltage readings, the test setup shall be as specified in 40.2.1.1. Input offset current shall be calculated as follows:

$$I_{IO} = \frac{V_{IO}1 - V_{IO}2}{R}$$

This shall be a 100 percent test.

40.2.1.4 Input bias current (I_{IB}). This current is the direct current biasing current required at either input to provide zero output voltage. A typical test circuit is shown on figure 11. The supply voltage shall be maximum. This shall be a 100 percent test.

40.2.1.5 Distortion. This test is a measurement of the output distortion at the maximum output voltage and current which can be supplied. A low frequency sine wave is applied to the input of the operational amplifier of the amplitude which will result in an output equal to the minimum acceptable output voltage swing. The maximum load (minimum resistance) is connected to the output together with a distortion meter. The power supply voltage shall be minimum. This shall be a sample test.

40.2.1.6 Gain accuracy. The purpose of this test is to check the closed loop gain of the operational amplifier which is a function of the source and feedback resistance tolerances. Gross errors such as low operational amplitude gain, open loop gain, low input resistance, or parasitic capacitance would also be discovered with this test. Supply voltage shall be nominal. The operational amplifier shall be programmed for a certain gain using internal resistors. Apply a normal signal at midband frequency and measure the gain. This shall be a 100 percent test.

40.2.1.7 Small signal bandwidth. This test verifies the bandwidth of the operational amplifier. The supply voltage shall be nominal. The operational amplifier shall be programmed for noninverting unity gain. A low level sine wave (100 millivolts root mean square (mVrms)) shall be applied to the input, unless restricted by slew rate, in which case 20 mVrms input may be tolerated. The sine wave frequency shall be set at the minimum bandwidth limit and the module output shall be within 3 decibels (dB) of the input voltage. This shall be a sample test.

40.2.1.8 Phase margin (stability). This test verifies stable operation (no oscillations). Phase margin is the difference in degrees between actual phase shift and the critical phase shift at which oscillations will occur. Therefore, a large phase margin (a 2.5 dB gain equals 45 degrees phase margin) is desirable. This test is performed with the supply voltage set at the normal value. The operational amplifier shall be programmed for a unity gain and a small amplitude sine wave shall be applied to the inputs. While monitoring the gain, increase the frequency and find the maximum gain peaking point. The increase in gain is a function of phase margin. This test could be combined with the bandwidth test. This shall be a sample test. An alternate test method for determining phase margin is to operate the operational amplifier as shown on figure 12 and apply a step function to the input. The overshoot of the output response is also a function of phase margin.

40.2.1.9 Common mode rejection ratio (CMRR). CMRR is the ratio of the differential voltage gain to the common mode voltage gain. The test shall be performed with the supply voltage set at maximum. The operational amplifier shall be operated as shown on figure 13. The CMRR is calculated as follows:

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$$CMRR = 20 \log \left[\frac{e_m}{e_o} \times \frac{100.1\ K\Omega}{0.1\ k\Omega} \right]$$

It should be noted that CMRR degrades with frequency. This shall be a sample test.

40.2.1.10 Noise. Two types of noise which can cause problems in operational amplifiers are broadband or "white" noise and per cycle or "spectral" noise. Within broadband noise, a phenomenon known as "popcorn" noise is associated with operational amplifiers. Popcorn noise consists of spikes occurring randomly and often at long intervals on the output. White noise, on the other hand, appears as random but continuous spikes with only gradual amplitude changes in different frequency bands. Noise generated and observed at a single frequency is per cycle or spectral noise. For all types of noise measurements, the module shall be operated with the supply voltage maximum, the operational amplifiers programmed for maximum gain, and the inputs grounded. The test equipment and environment shall be relatively noise free. These tests shall be either 100 percent tests or sample tests depending on the application.

(a) Broadband. A true root mean square (rms) voltmeter is adequate to measure broadband noise if the bandwidth response need not be limited. If the bandwidth response must be limited, a low noise filter may be inserted before the voltmeter. Special precaution may have to be taken to ensure that the environment and test equipment are as free from noise as possible.

(b) Spectral. An instrument with a narrow band response is required to measure spectral noise. Readings shall be taken at several frequencies in the applicable band.

(c) Popcorn. Popcorn noise can be measured on a fast response storage oscilloscope. A maximum voltage peak is specified and the operational amplifier is observed for some specified length of time (for example, 10 seconds).

40.2.1.11 Life test. In addition to the requirements of MIL-M-28787 for life test, the operational amplifier offset voltage shall be monitored at temperature to ensure that the operational amplifier does not experience out-put latching. Latching is a gradual drifting of the offset voltage toward the positive or negative supply voltage during long operating periods and elevated temperatures. The output voltage shall be measured prior to disconnecting power or reducing the test temperature. This shall be a qualification test.

40.2.1.12 Power supply stress check. This is a maximum stress test and is performed to insure that the module is not damaged by overvoltage. The power supply voltage (for modules operating from plus or minus 15 volts) shall be plus or minus 18 volts or rated absolute maximum minus 2 volts (whichever is higher). The operational amplifier shall be operated in a circuit which measures input offset voltage. The limits shall be 1.5 times the maximum normal offset voltage limits. This shall be a qualification test.

40.2.2 Filters. The following tests shall be performed on filter modules when applicable. Unless otherwise specified, these tests shall apply for passive as well as active filters.

40.2.2.1 Passband ripple. This test measures the gain variation around a nominal value throughout the passband. The nominal gain value should be measured in the middle of the passband and all other points measured with respect to this reference. Supply voltage shall be nominal (active filters only). The filter output shall be loaded with the nominal load and a nominal sine wave applied to the input. Midband gain shall be measured and a slow sweep of the other frequencies shall be made recording the gain. These gain measurements shall be compared to the midband gain and shall be within an applicable tolerance. This may be a 100 percent test or a sample test.

40.2.2.2 Minus 3 dB point. This test defines the beginning of the stopband region. The supply voltage shall be nominal. The filter shall be loaded with a nominal value load and a sine wave of nominal amplitude shall be applied to the input. The frequency shall be adjusted so that the gain is minus 3 dB referenced to the midband gain. The gain will be 0.707 of the midband gain at this frequency. This frequency shall be within the specified tolerances. This shall be a 100 percent test.

40.2.2.3 Stopband attenuation. This test verifies a minimum roll-off slope. Apply nominal supply voltage, load, and input signal to the filter. Pick two points on the roll-off slope and specify minimum attenuation required at these frequencies. This may be a 100 percent test or a sample test.

40.2.2.4 Stopband ripple. This test verifies that the stopband does not contain unacceptable increases in gain. Nominal supply voltage, load, and input signal shall be applied to the filter. Sweep the stopband up to a sufficiently high frequency to ensure attenuation is controlled and specify either a continually decreasing gain or a maximum attenuation figure that all readings must fall below. This test may be a 100 percent test or a sample test.

40.2.2.5 Noise. Noise tests shall only be performed on active filters. Since active filters are basically operational amplifier circuits, the tests shall be performed as specified in 40.2.1.10.

40.2.2.6 Undistorted output voltage. Undistorted output voltage test shall only be performed on active filters. Since active filters are basically operational amplifier circuits, the test shall be performed as specified in 40.2.1.5.

40.2.2.7 Phase shift. Supply voltage, load, and input signals shall be set at nominal values. Using a phase meter, measure the input to output phase shift at mid passband frequency. This shall be a sample test.

40.2.3 Field effect transistor (FET) switches. The following tests shall be performed on FET switch modules. It is assumed that all new FET switches will have built in drives, therefore, driver tests shall also be included in these tests.

40.2.3.1 Switch "ON" resistance. This test measures the direct current (dc) resistance of all paths through the switch. Use a dc power supply to drive current through each channel into an applicable load resistor. The current shall be the maximum rating of the switch. Measure the voltage drop across the load resistor. The difference between this voltage and the input voltage is the voltage drop across the channel. From this voltage and the known current, the resistance can be calculated. Nominal supply voltages shall be used. This shall be a 100 percent test.

40.2.3.2 Switch leakage current. This test measures the leakage through the analog channel when the switch is turned off. With the channels turned off, apply maximum voltage across the channel and measure the leakage current to ground. Supply voltages shall be nominal. This shall be a 100 percent test.

40.2.3.3 Driver logic threshold voltage. Using a dc power supply and load resistor, set up the circuit as described in 40.2.3.1. Apply minimum logic voltage to the driver to turn on the switch. As each channel is enabled, measure the "ON" resistance as specified in 40.2.3.1. This shall be a 100 percent test.

40.2.3.4 Driver logic input current. Using the maximum supply voltages, measure the current into and out of the logic inputs. Specify a zero minimum limit and an applicable maximum limit for high level current and specify both an applicable minimum and maximum limit for low level current. This shall be a 100 percent test.

40.2.3.5 Turn on delay. Set up a direct current power supply and nominal output load on the analog channels. Using a pulse generator with a rise time much faster than the expected delay, pulse each logic input. Observing the input pulse and the switch output simultaneously, measure the turn on time required for the analog output to settle to the required level. This shall be a sample test.

40.2.3.6 Turn off delay. The turn off delay is measured using the same setup as specified in 40.2.3.5 except the turn off is measured. This shall be a sample test.

40.2.3.7 "OFF" analog crosstalk. This test measures the coupling to "OFF" analog channels. Condition the switches so that one channel is "ON" and the remaining channels are "OFF". Load all the "OFF" channel outputs with the minimum load to ground. Load the "ON" channel output with the maximum load. Apply a maximum peak-to-peak voltage square wave to the "ON" channel. Measure the induced voltage on the remaining "OFF" channels. This shall be a qualification test.

40.2.3.8 "ON" analog crosstalk. This test measures coupling to an "ON" analog channel. Tie each end of one channel through a high resistor to ground. Turn this channel "ON". Apply a square wave to the remaining channels and turn them "ON". Measure the induced voltage on the single quiet channel. This shall be a qualification test..

40.2.3.9 Digital crosstalk. This test shall be performed on each address. Connect one bit on the address under test to its "ON" channel logic state. Apply a dc voltage and an applicable load resistor to this analog channel. Connect a binary counter to the other bits. Pulse the counter so that it cycles through all possible address combinations. Monitor the analog output under test and measure the amplitude of any voltage spike which may be present. Repeat for all bits. This shall be a qualification test.

40.2.3.10 Break before make. Step the switch through all possible address combinations using a pulse generator or a binary counter. Apply an input signal of nominal voltage and frequency to the analog channel under nominal load. Observe, using a dual trace oscilloscope, the switching of the output and verify the break before make action. This shall be a qualification test.

40.2.3.11 "OFF" channel impedance. This test checks capacitive coupling through an "OFF" channel. With the channel "OFF", apply a sine wave of maximum voltage and frequency to the analog input. Under minimum load, measure the output voltage. Specify a maximum amplitude. This shall be a 100 percent test.

40.2.3.12 "ON" channel impedance. This test checks parasitic capacitance in the channel. Apply maximum voltage and a maximum frequency sine wave to a channel which is "ON". Measure the attenuation through the channel across the maximum load. This shall be a 100 percent test.

40.2.3.13 Power off switch resistance. This test checks whether the switch is "ON" (low channel resistance) or "OFF" (high channel resistance) when power is removed from the module. Use a dc power supply to drive current through each channel into an applicable load resistor. Measure the voltage across the load to determine if the switch is "ON" or "OFF". The above procedure should be followed with each module supply voltage contact connected either to ground or nominal supply voltage. Initially only one module supply voltage contact at a time shall be grounded, and all combinations shall be checked until finally all supply voltage contacts are grounded. The input voltage to the switch channel shall be chosen so that the combinations of supply voltages will not damage the module. This shall be a qualification test. Note that some field effect transistor (FET) switches have overvoltage protection. If the input voltage exceeds the direct current power supply voltage, a short appears between the input and the power line thus when the power lines are at zero volt the input signal line may be shorted to zero volt.

40.2.3.14 Input clamp diode voltage. The purpose of this test is to ensure the existence of clamp diodes on the inputs of the module. The power supply voltage shall be minimum. The test shall be performed by forcing maximum current through the clamp diode and measuring the voltage across the diode. CAUTION: this test should not be performed on modules which do not have clamp diodes. This shall be a sample test.

40.2.4 Relays. The following tests shall be performed on relays when applicable.

40.2.4.1 Open contact resistance. The open contact resistance of a relay shall be measured using a megohm bridge. The bridge voltage shall be set at 100 Vdc plus or minus 10 percent. For normally open contacts, apply the minimum dropout voltage to the relay coils and make the measurement. For normally closed contacts, energize the relay coil with the maximum pick-up voltage and make the measurement. The minimum limit shall be 10 megohms. The maximum limit shall be infinity. This shall be a 100-percent test.

40.2.4.2 Closed contact resistance. For normally closed contacts, apply the minimum dropout voltage to the coil and force an applicable current through the contacts. The test current shall be the maximum rated contact current for ratings above 100 milliamperes (mA) and a test current of 10 mA maximum for all contacts rated 100 mA or less. Specify the contact resistance and measure the voltage across the contact at the known current to verify the contact resistance. For normally open contacts, the relay shall be energized with a coil voltage equal to the maximum pickup voltage and then the same procedure as for measuring the normally closed contacts shall be followed to verify the contact resistance. These tests shall be 100 percent tests.

40.2.4.3 Pickup voltage. Adjust the applied coil voltage to the maximum allowable operating voltage for a period of 1 to 3 seconds. Gradually reduce the coil voltage to zero. Then gradually increase the coil voltage until the normally open contacts have a resistance of 1 ohm or less. Measure the coil voltage. This shall be a 100 percent test.

40.2.4.4 Dropout voltage. Adjust the applied coil voltage to the maximum allowable operating voltage. Gradually reduce the coil voltage until the normally closed contact resistance is 1 ohm or less. Measure the coil voltage. This shall be a 100 percent test.

40.2.4.5 Diode forward resistance. Using an ohmmeter, measure the forward resistance of the transient suppression diode on the relay. The range of the ohmmeter shall be specified to establish the current through the diode. This shall be a 100 percent test.

40.2.4.6 Coil resistance. Perform test in accordance with MIL-STD-202, method 303. Connect the bridge or other suitable equipment across the coil of the relay so that the suppression diode is reverse biased. Then measure the resistance of the coil. The test current through the coil shall be applied for only a short period of time and shall be as small as practical to prevent coil heating. This shall be a sample test.

40.2.4.7 Dielectric strength. Perform test in accordance with MIL-STD-202, method 301. Voltage shall be 1000 plus or minus 50 volts root mean square (Vrms) applied across the following points of the relay. When the test is performed, the leakage current shall not exceed 1 mA nor shall there be any flashover or evidence of other breakdown.

(a) Between case, frame, or enclosure and open contacts in the energized and unenergized positions.

(b) Between case, frame, or enclosure and coil.

(c) Between all contacts and coil.

(d) Between coils (for dual coil relays only).

(e) Between contact poles.

This shall be a sample test.

40.2.4.8 Insulation resistance. Perform test in accordance with MIL-STD-202, method 302, test condition A. The insulation resistance shall be measured at the same points specified in 40.2.4.7. The minimum limits shall be 1000 megohms between coil and case and 5000 megohms at all other points before the life test. After the life test, the limits shall be minimums of 750 and 1000 megohms, respectively. This shall be a sample test.

40.2.4.9 Operate time. Operate time is measured from the rising edge of the coil energizing voltage to the first point of relay switching as seen by monitoring the closing of the normally open contacts. The relay shall be operated at a minimum of 10 Hz unless the maximum operating speed is less than 10 Hz. The coil voltage shall be a square wave with an amplitude equal to the minimum rated voltage. The operate time measurement does not include contact bounce as shown on figure 14. This shall be a qualification test.

40.2.4.10 Release time. The release time is measured from the falling edge of the coil voltage waveform to the first point of the relay switching as can been seen by monitoring the opening of the normally closed contacts. The setup for release time shall be as specified in 40.2.4.9 (except that the amplitude shall be equal to the maximum rated voltage) and the measurement shall be taken as shown on figure 14. This shall be a qualification test.

40.2.4.11 Contact bounce. Contact bounce is measured at the closure of each set of contacts as can be seen on figure 14. The setup for contact bounce shall be as specified in 40.2.4.9 for operate contact bounce and 40.2.4.10 for release contact bounce. This shall be a qualification test.

40.2.4.12 Overvoltage. The relay shall be energized with maximum coil voltage and the closed contacts shall carry the maximum rated current at the maximum rated voltage. The relay shall remain energized for 72 hours at maximum class temperature. Upon removal of the coil voltage at the end of the 72 hour period, the relay shall meet the class temperature end-of-life limits for release time as performed in 40.2.4.10. This shall be a qualification test.

40.2.4.13 Overload. The overload test shall be performed with the relay at maximum class temperature. The current through the relay contact shall be double the rated current at rated voltage. The relay shall be operated for 100 cycles at the rate of 20 cycles per minute. The coil voltage shall be the maximum rated voltage. Monitor the closed contacts for at least 50 percent of the closure to detect the actual mechanical and electrical switching. Contact resistance tests as specified in 40.2.4.1 and 40.2.4.2 shall be performed following the 100 cycles to verify the test. This shall be a qualification test.

40.2.4.14 Break before make. This test shall be performed only on double throw relays. The relay shall be subjected to 50 cycles at a rate of 20 cycles per minute, switching a current of 0.050 ampere at the rated voltage at maximum class temperature. The coil voltage shall be equal to the maximum pickup voltage. The contacts shall be monitored to ensure that the normally closed contact breaks before the normally open contact makes. This shall be a qualification test.

40.2.4.15 Contact life. Each relay shall be subjected to a minimum of 100,000 cycles at 20 cycles per minute at maximum class temperature. For a general purpose relay, the contact voltage and current shall be at low level for half the relays tested and at rated level for the remainder. The coil voltage shall be the maximum pickup voltage. The contacts shall be monitored for at least 50 percent of each closure. At rated current, a module failure is defined as four failures in any one relay to meet the specified contact resistance requirements during the life test. Following the life test, the following tests shall be performed:

(a) Dielectric strength.

(b) Insulation resistance.

(c) Pickup voltage.

(d) Dropout voltage.

(e) Operate and release times.

(f) Contact bounce.

(g) Coil resistance.

(h) Contact resistance. (Use approximately the same current as used during life test, for example: Do not use a low level test current to measure contact exposed to a high current life test.)

This test shall be a qualification test.

40.2.4.16 Diode inverse current. The diode inverse current test shall be performed as the last test on one module which has not been subjected to the life test. The transient suppression diodes shall be removed from the module and the inverse current measured with the rated voltage applied. This shall be a qualification test.

40.2.5 Power supplies and regulators. The following tests shall be performed on power supplies and regulators when applicable.

40.2.5.1 Load regulation. This test is a measure of the output voltage variance under different load conditions. The load shall be changed from no load (or minimum load) to full load while measuring the output voltage. If there are multiple outputs, all shall be measured as above as well as verifying that a load change on one output has a minimal effect on another output (cross regulation). The input voltage shall be set at a nominal value. This shall be a 100 percent test.

40.2.5.2 Line regulation. This test is a measure of the output voltage variance with a change in input voltage. The input test voltages shall be the worst case minimum and maximum for the source being used. The source may vary as much as plus or minus 20 percent from nominal. The loads shall be set at minimum and at maximum for each input test voltage. At least a portion of these tests shall be 100 percent with the remainder sample tests.

40.2.5.3 Output ripple voltage. This test is a measure of the alternating current (ac) signal which is present in the dc output. Output ripple voltage may be measured over several different frequency ranges. Total ripple would be a wideband (5 to 100 megahertz (MHz)) measurement. Line ripple would be measured with a 10 kHz bandwidth. Converter frequency ripple (if applicable) would be measured over a passband of 10 kHz to 1 MHz. Ripple shall be measured at full load. The total ripple test shall be a 100 percent test. Line and converter ripple tests shall be sample tests.

40.2.5.4 Input power. This test is intended to measure the efficiency of the power supply or regulator. Using a wattmeter which is not limited by nonsinusoidal waveforms, measure the input power at nominal input voltage and maximum load current. This shall be a 100 percent test.

40.2.5.5 Overvoltage threshold. The power supply shall be checked for shut down under output overvoltage conditions. With nominal input voltage and frequency applied to the power supply, apply an overvoltage to the power supply output and check to see that the power supply will shut down. This shall be a sample test.

40.2.5.6 Current limiting and output short circuit current. These tests are a measure of the output current limiting feature. For current limiting, increase the output loading while monitoring the output voltage for a specified drop (or overcurrent BIT for a change in state). Measure the output current at the limiting point. For output short circuit current, measure the output current with the output terminals shorted together. The input voltage shall be nominal. Current limiting shall be a 100 percent test and output short circuit current shall be a sample test.

40.2.5.7 Dynamic regulation. This test is a measure of the ability of a power supply or regulator to return to regulation with rapid changes in output loading. The output loading shall be switched from no load (or a typical load) to full load and the resultant voltage spike and time to regain output regulation shall be measured. The test shall be repeated with a load switching from full load to no load (or a typical load). The maximum rate of the load current (dIo/dt) shall be specified. The input voltage shall be nominal. This regulation of dynamic response is shown on figure 15. This shall be a sample test.

40.2.5.8 Power turn on/turn off response. This test is a measure of the characteristics of the power supply or regulator during application or removal of input power. The time from turn on until the output voltage rises to within regulation limits shall be measured. Output hold up time after power is turned off could also be measured. If there are multiple outputs, it may be required to measure that the outputs come up and go down in a specified sequence or simultaneously. The output shall be measured for the presence of a voltage transient during either turn on or turn off. Adequate time between the on/off sequence shall be provided to allow all transients and turn-on or shut-down sequences to be completed. These tests shall be sample tests.

40.2.6 Capacitors. The following tests shall be performed on capacitor modules when applicable.

40.2.6.1 Dc leakage current. With a current limiting resistor in series with the capacitor, apply maximum rated voltage and measure the leakage current through the capacitor. This test checks the dielectric losses in the capacitor and verifies the rated voltage. This shall be a 100 percent test.

40.2.6.2 Capacitance and dissipation factor. Using a capacitance bridge with the output set at the applicable voltage and frequency, measure the capacitance and dissipation factor of the capacitor. This shall be a 100 percent test.

40.2.6.3 Dielectric strength. Unless otherwise specified by the particular capacitor detail specification, apply 225 percent of the maximum rated voltage for a period of 60 seconds and check the dc leakage current. This current shall not exceed 1 mA. This shall be a sample test.

40.2.7 Transformers. The following tests shall be performed on transformer modules when applicable. Since there is a variety of types of transformers, there may be additional tests which should be performed to characterize the transformer.

40.2.7.1 Transformer ratio. With the input voltage and frequency set at nominal values, measure the ratio of output voltage to input voltage under full load and no load conditions. Two measurement methods could be used. If the test limits are greater than or equal to 1 percent, the output voltage for a given input voltage could be measured with an ac voltmeter, however, if the test limits are less than 1 percent, then a ratio transformer and phase angle voltmeter would have to be used to obtain the required accuracy. This shall be a 100 percent test.

40.2.7.2 Tap accuracy. Using the same setup and measurement conditions specified in 40.2.7.1, measure the ratio of the output voltage across the tap to the input voltage. This shall be a 100 percent test.

40.2.7.3 Phase shift. With the input voltage and output load at nominal values and the input frequency set at midband, measure the phase shift from primary to secondary using a phasemeter. This shall be a 100 percent test.

40.2.7.4 Dc resistance. Using an ohmmeter, measure the resistance of the primary and secondary. This shall be a 100 percent test.

40.2.7.5 Primary magnetizing inductance. With the transformer secondary open, measure the inductance of the primary using an inductance bridge. This shall be a sample test.

40.2.7.6 Leakage inductance reflected to primary. With the transformer secondary shorted, measure the inductance of the primary with an inductance bridge. The ac voltage across the primary should be very small in order that the secondary current will not exceed the transformer rating. This shall be a sample test.

40.2.7.7 Leakage inductance reflected to secondary. This test shall be performed as specified in 40.2.7.6 except that the primary shall be shorted and the inductance of the secondary measured. This shall be a sample test.

40.2.7.8 Primary to secondary capacitance. With the primary winding shorted and the secondary windings shorted, measure the capacitance from primary to secondary using a capacitance bridge set at an applicable frequency. This shall be a sample test.

40.2.7.9 Frequency response. With maximum load on the secondary, apply a sine wave of nominal voltage to the primary. Monitor the secondary and find the upper and lower minus 3 dB frequencies. Measure these frequencies, then, sweep from the lower frequency to the higher frequency and verify that the response is flat plus or minus so many dB. This shall be a sample test.

40.2.7.10 Total harmonic distortion. With maximum input voltage at midband frequency applied to the primary and maximum load across the secondary, measure the harmonic distortion at the secondary with a distortion analyzer. This shall be a sample test.

40.2.7.11 Electromagnetic coupling. This test applies only to modules which have two or more transformers. Apply maximum input signal to one transformer. Place an applicable resistor across the primary of the other transformers. With an ac voltmeter, measure the voltage on the secondary of the other transformers. This shall be a sample test.

40.2.7.12 Core loss. With the secondary open, apply normal operating voltage and frequency to the primary. Using a wattmeter, measure the power consumed in the primary. For signal transformers, an alternate method would be to measure the voltage across the primary, the current through the primary (by measuring the voltage across a series resistor), and compute the wattage from these quantities. This is core loss. This shall be a sample test.

40.2.8 Synchro to digital (S/D) and resolver to digital (R/D) convertors. The following tests shall be performed on S/D and R/D convertor modules when applicable.

40.2.8.1 100 percent (X) tests. The following tests shall be performed on all modules during 25°C acceptance testing. The 100 percent tests shall include the tests specified in 40.1.

(a) Static angular accuracy. The purpose of this test is to determine the accuracy of the conversion under nonrotating conditions. Angle information is input into the converter by a synchro or resolver standard and the output bits are checked. The limits shall be specified by the number of least significant bits (LSB) corresponding to the accuracy required. The tests shall be performed at the frequencies of interest (60 Hz, 400 Hz, and so forth) and at the nominal input voltage level.

(b) Digital output voltage. The digital outputs shall be tested for high and low levels under load. The load shall be as specified by 30.1.3 of appendix D.

(c) Three-state leakage current. The leakage current when the outputs are disabled shall be measured when the outputs are held at high and low levels by external sources. These levels shall be determined by the technology.

(d) Converter busy. The converter busy outputs shall be tested for high and low voltage levels and pulse width.

(e) Secondary outputs. Secondary outputs such as error voltage or velocity voltage shall be functionally tested only if required by system criteria.

(f) Monotonicity. Monotonicity is inherent in a type II converter using the up down counter method. If other methods are used, monotonicity shall be tested.

40.2.8.2 Sample (S) tests. The following tests shall be performed on a sample basis as specified in 30.1.1.

(a) Static angular accuracy. These tests shall be performed as specified in 40.2.8.1(a) except that the input signal voltage levels shall be at the minimum and maximum levels respectively.

(b) Digital input currents. These tests shall be performed as specified in 40.1.1.4 and 40.1.2.3 of appendix D.

(c) Sensitivity. The purpose of this test is to measure the magnitude of angle change required to cause one LSB change in the digital output.

(d) Zero degree crossover. The purpose of this test is to measure the small signal tracking capability of the converter at an angle of zero degrees. An ac modulator shall be applied to the resolver input signals at zero degrees to cause a minimum of plus or minus 10 LSBs about zero degrees. The frequency of the modulation shall be specified. The digitized output signal shall show no oscillation or non-monotonic behavior. This test shall be performed when zero degree crossover is not tested within the settling time test.

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40.2.8.3 Qualification (Q) tests. The following tests shall be performed only during qualification testing.

(a) Insulation resistance. The input signal contacts and reference input contacts shall be connected to the positive terminal of a megohm bridge and the remaining contacts tied to the negative terminal. A minimum voltage of 300 Vdc shall be applied. The resistance measured by the megohm bridge shall be greater than 10 megohms initial and greater than 1 megohm end-of-life. This is a stress test (see 30.1.3).

(b) Power supply sequencing. The purpose of this test is to ensure that there is no degradation of the device due to the sequence of power up or loss of a power supply. The device shall be operated at maximum reference voltage and all outputs loaded. All combinations of power supply turn on sequences shall be tested. The module shall be considered to pass this test if the module passes the remainder of the tests in the sequence. This is a stress test (see 30.1.3).

(c) Common mode voltage. A common ac voltage is applied to all signal inputs and the reference inputs. This voltage shall be the maximum voltage allowed. The module shall be considered to pass this test if the module passes the remainder of the tests in the sequence. This is a stress test (see 30.1.3).

(d) Tracking rate. The purpose of this test is to determine the maximum revolutions per second that the converter can accurately track. This test shall be performed at the minimum and maximum reference signal frequencies. The test can be performed by increasing the revolutions per second of the input angle until the converter busy pulse train of the converter is no longer uniform. The module has then reached its maximum tracking rate.

(e) Settling time. The purpose of this test is to measure the ability of the converter to respond to large step changes in angle position. The step is normally from zero to 179 degrees (output all zeros to all ones except for 180-degree bit). The LSB shall be monitored to determine settling time.

(f) Continuous conversion. The purpose of this test is to verify that the converter continues to track the input even while the output is inhibited. The converter busy pulse train will continue if the converter is tracking.

(g) Noise sensitivity. The purpose of this test is to determine the effect of random noise on the stability of the converter. Inject random noise onto the reference low (RL) line and monitor the LSB. The module shall pass this test if the LSB does not toggle.

(h) Power supply rejection. The purpose of this test is to verify the stability of the output with the presence of ripple on the power supplies. A 1 Vrms sine wave at 1 kHz is injected through a 20 microfarad (μF) blocking capacitor. A 100 ohm series resistor shall be inserted between the power supply and the module. The module shall pass the test if the LSB does not toggle.

(i) Power supply transient amplitude. Monitor the power supply lines while the module is tracking. The positive and negative peaks seen on the power supply lines shall be less than 700 mV.

40.2.9 Analog to digital (A/D) and digital to analog (D/A) converters. The following tests shall be performed on A/D converters and D/A converters. For these tests, one LSB shall be defined as voltage range/2^n where n is the number of digital logic inputs (for D/A) or outputs (for A/D).

40.2.9.1 Digital input current. These tests shall be performed on all digital inputs on converter modules as 100 percent (X) tests.

(a) Digital input current (high level). Supply voltages shall be at the maximum value. The input under test shall be at the maximum high level voltage. All other digital inputs shall be connected to zero volt where feasible in order to check for module shorts. Every digital input shall be tested individually.

(b) Digital input current (low level). Supply voltages shall be at the maximum value. The input under test shall be at zero volts. Every digital input shall be tested individually.

40.2.9.2 Input clamp diode voltage. The purpose of this test is to ensure the existence of clamp diodes where applicable on the digital inputs of the module. Supply voltages shall be minimum. The test shall be performed by forcing maximum current through the clamp diode and measuring the voltage across the diode. This shall be a sample test. CAUTION: This test shall not be performed on modules which do not have clamp diodes.

40.2.9.3 Digital input capacitance. No voltage shall be applied. The capacitance from each digital input to the logic ground contact shall be measured on each input individually. The minimum limit shall be 1 pF and the maximum limit determined by engineering judgement and experimental data. This shall be a qualification test.

40.2.9.4 Input impedance. The input impedance of the analog input of the A/D converter or the reference input of a multiplying D/A converter shall be determined by applying the maximum expected voltage to the input and measuring the input current. This shall be a sample test.

40.2.9.5 D/A converter tests. The following tests shall be performed on D/A converters.

(a) Zero offset error. This test is a measure of the output offset voltage of the module. The digital inputs shall be conditioned for an ideal output of zero volt and the actual output voltage shall be measured. The zero offset error can be expressed in LSB by dividing the output voltage by one LSB. This test shall be performed for each voltage range as a 100 percent test.

(b) Differential linearity. This test determines the step in analog output for a single digital count. The module shall be configured for a voltage output. Testing shall be performed as a minimum at all major carries (digital steps involving a change of state of at least two-thirds of the digital inputs) of one voltage range. The conditioning voltages shall be specified such that any controller with compatible logic can be used to generate the digital patterns. The output voltage shall be measured using a voltmeter. The difference in voltage output at two adjacent digital inputs shall meet the specified limits (where it is not feasible to use a voltmeter, a reference D/A converter output may be compared to the output of the unit under test for the adjacent codes. The step is then one LSB plus the difference of the error voltages). The nominal result for this test is one LSB. Monotonicity is verified (for the tested codes only) by constraining the step to be no less than zero volt. This shall be a 100 percent test.

(c) Absolute accuracy. This test determines the total error of the D/A converter output. The end points for all ranges shall be tested with at least one range tested using digital threshold voltages. The output shall be measured directly with a voltmeter or, where greater accuracy is required, compared to a calibrated reference D/A converter. The absolute accuracy error for any given digital code is the difference between measured output and the ideal output at that code expressed in LSB. If absolute accuracy is specified at plus or minus one-half LSB for all codes, tests for integral linearity error and/or differential error may be deleted, if no further accuracy is lost by the deletion of these tests. This test is a 100 percent test.

(d) Linearity. This test determines the deviation of the output voltage at a particular digital code from the expected voltage at that code based on the end point levels. This expected voltage is obtained by dividing the voltage range between the end points into 2^n -1 equal steps (n is the resolution of the D/A converter). End point errors (gain and offset) can be eliminated from the output voltage either mathematically or by adjustment circuitry capable of reducing end point errors to not more than 0.1 times the linearity limits. Minimum testing shall be for the codes and conditions specified for differential linearity using similar measurement techniques. This shall be a 100 percent test. NOTE: If mathematical methods are used, linearity, differential linearity, zero offset, and absolute accuracy errors may all be determined from a single set of data points.

(e) Settling time. This test determines the time for the analog output to settle within a specified window around the final output following a change in the digital coding. Programming shall be for a full scale change in output or half scale where desirable for bipolar modes. Circuitry to avoid excessive scope recovery time shall be employed. The particular circuit will depend on the speed of the module under test. This shall be a sample test.

(f) Feed through error. This test determines the ac feed through from the reference voltage input to the output of a multiplying D/A converter. A sine wave shall be applied to the reference voltage input with the digital inputs programmed for a zero-volt output. An ac voltmeter shall be used to measure the output. This shall be a sample test.

40.2.9.6 A/D converters. The following tests shall be performed on A/D converters. Where a logic load circuit is required, a standard 5 volt load as specified in appendix D shall be specified. Different loads may be used for other output logic. All codes integral linearity errors of differential linearity errors shall be tested 100 percent for 10-bit or less data converters and all code combinations of the first four MSBs together with the major carries shall be tested for 12-bit or greater converters.

APPENDIX E

(a) Zero offset error. An A/D converter module specification may define the ideal output for a zero-volt input in four different ways. For unipolar devices, the first transition occurs one half or one LSB from zero-volt. For bipolar devices, either a specific digital transition occurs at zero-volt or zero-volt corresponds to a point midway between two transitions. This test determines the actual voltage required to obtain the ideal digital output for zero-volt. For unipolar devices, the voltage level of the first transition shall be measured. The zero offset error is the difference between that level and the ideal level (one-half or one LSB). For bipolar devices, the offset is either the voltage required to cause the transition specified for zero-volt to occur or the average of the voltages at the transition points which ideally lie plus or minus one-half LSB from zero-volt. Clock frequency shall be maximum where not internally controlled. This shall be a 100 percent test.

(b) Absolute accuracy. This test measures the end point accuracy of the A/D converter. The voltage for which the last transition (and the first transition for bipolar modules) occurs shall be measured. The accuracy error is found by comparing the measured voltage to the ideal voltage and can be expressed in LSBs. Clock frequency shall be maximum where not internally controlled. All digital inputs shall be at threshold levels. This shall be a 100 percent test and shall check all ranges.

(c) Linearity. This test determines the deviation of the input voltage for a particular digital transition from the expected voltage based on the end point transitions. The expected voltage is obtained by dividing the voltage difference between the first and last transitions by 2^n -2 (n is the resolution of the A/D converter), yielding the increment size, and adding the appropriate number of increments for the digital code of interest to the first transition voltage. Since worst case linearity errors do not always occur at the major carries (as is usual for D/A converters) only a test of all codes will fully ensure linearity. When abbreviated testing is performed, a note shall be included that linearity is only ensured for the tested codes. Clock frequency shall be maximum where

externally controlled. Linearity errors can be calculated. Refer to the ideal transition voltages or to the code midpoint voltage between the two transition voltages. The method chosen to calculate the module errors shall be specified in the detailed module specification. This shall be a 100 percent test.

(d) Differential linearity. This test determines the range of analog inputs which will result in a given digital output (width of step). This range shall be determined by measuring two adjacent transition levels and finding the difference between them. Nominal step width is one LSB and a minimum limit greater than zero-volt ensures no missing codes (for the tested steps only). Testing shall be performed at all major carries as a minimum. Clock frequency shall be maximum where externally controlled. This shall be a 100 percent test.

(e) Output voltage (high level and low level). The power supply voltage shall be minimum. The analog input to the module under test shall be chosen to force all outputs high for the high level output voltage test and low for the low level output voltage test. The output under test shall be connected to a logic load circuit. This shall be a 100 percent test.

(f) Propagation delay times. This test applies only to A/D converters which have an external clock and do not have a latch on the output contacts. All digital outputs shall be tested. A logic load circuit shall be connected to the output under test. The propagation delay from the clock pulse edge triggering output logic into a valid data state or the output pulse shall be measured using reference timing points based on voltage or percentage values. The reference timing points shall be specified in the detail module specification. This shall be a sample test. Appropriate waveforms to show measurement points shall be included as a separate figure following the test circuit figure.

(g) Three-state outputs. The tests described in appendix D for three-state outputs shall be specified for A/D converter modules containing three-state buffers. These tests shall be 100 percent tests.

(h) Transition uncertainty. Where applicable, the voltage range of uncertainty between output states shall be measured. This uncertainty is caused by noise and may be measured by finding the range of uncertainty of the LSB at the major carry (change in all bits). This shall be a qualification test.

(i) No missing codes. This test determines the presence of all output codes as the input voltage is varied over its full scale range. This test determines only the presence or absence of a code and does not determine value or accuracy. This shall be a 100 percent test.

40.2.10 Digital to synchro (D/S) and digital to resolver (D/R) converters.

40.2.10.1 Ratios. The concept of D/S and D/R converters is based upon ratios of the appropriate line to line voltages. Absolute voltage values of any one line-to-line voltage is of secondary importance. This must be kept in mind when specifying a module. The individual line amplitudes are only important in applications using the outputs individually.

40.2.10.2 Similarity to D/A. The D/S and D/R functions are similar to D/A converters; a digital representation of a signal is converted to its analog equivalent. This leads to the fact that some of the tests for D/A converters are also valid for D/S and D/R converters except that the outputs of interest are ratios rather than a single absolute voltage or current.

40.2.10.3 100 percent (X) tests. The following tests shall be performed on all modules during 25°C acceptance testing. The 100 percent tests shall include the test specified in 40.1.

(a) Maximum output voltage. The purpose of this test is to verify the output voltage to be near a specified level. Examples are 11.8, 26, 6.8, and 90 Vrms line-to-line. For D/S converters, the maximum voltage will appear when the digital inputs represent the following angles:

ϕ = 90 degrees; S1-S3 = maximum.

ϕ = 150 degrees; S2-S3 = maximum.

ϕ = 210 degrees; S2-S1 = maximum.

For D/R converters the maximum voltage will appear when the digital inputs represent the following angles:

ϕ = 90 degrees; sin ϕ = maximum.

ϕ = 0 degrees; cos ϕ = maximum.

The modules shall be at full load. The limits shall reflect tolerances not better than the reference signal supplied.

(b) Output zero noise. The purpose of this test is to maintain module accuracy when the angle data inputs require outputs such that the ratio is a low value over a high value as occurs at 90 degrees for a D/R module. The voltage should be less than minus 50 dB at the carrier frequency.

(c) Static angular accuracy. This test is performed by inputting the digital angle data by some suitable means and then measuring the output using a synchro/resolver bridge. The test shall be performed at all carrier frequencies of interest.

(d) Digital input current. The digital input currents, high level and low level, shall be performed as specified in 40.1.1.4 and 40.1.2.3 of appendix D.

(e) Reference input impedance. The purpose of this test is to determine and control the reference input. The test shall be performed using a series impedance and measuring the resulting voltage division.

40.2.10.4 Sample (S) tests. The following tests shall be performed on a sample basis as specified in 30.1.1.

(a) Power supply ripple rejection. This test shall be performed by injecting a ripple with an amplitude of 1 Vrms at the carrier frequency. Input angles of 0 and 90 degrees shall be used for D/R and 90, 60, and 30 degrees for D/S modules. The modules shall be considered to pass the test if the angular accuracy is as specified at these angles.

(b) Dc offset voltage. The purpose of this test is to ensure minimum dc voltage on the output lines. The test shall be performed with the outputs unloaded.

(c) Scale factor variation. The purpose of this test is to measure the variation of the output amplitude with the digital input angle. Small scale factor variation allows independent use of the outputs. To perform the test, a highly stable reference is required. Perform the test by measuring the line-to-line voltage of each output for each angle being tested. Compute the value for each angle being tested.

$$\frac{V_{measured} - V_{nominal}}{V_{nominal}} = V_{DEV}$$

The average deviation from nominal is

$$\frac{V_{DEVMAX} + V_{DEVMIN}}{2} = V_{AVG}.$$

$$\text{Scale factor variation } \Delta V\% = \frac{V_{DEVMAX} - V_{AVG}}{V_{AVG}} \times 100.$$

$\Delta V\%$ shall be less than the scale factor variation specified.

40.2.10.5 Qualification (Q) tests. The following tests shall be performed only during qualification testing.

(a) Power supply transient amplitude. The purpose of this test is to verify the ability of the module to operate under and suppress the high frequency transients induced during module operation. Monitor the power supply lines while the module is tracking the input digital angle changes. The positive and negative peaks seen on the power supply lines shall be less than 700 mV.

(b) Power supply sequencing. Perform in accordance with 40.2.8.3(b).

40.3 Networks. Network modules shall be specified so that, if possible, each individual component is tested. If the network consists of groups of components interconnected to perform a function, the performance of the function shall be tested.

40.4 Interface. An interface module is defined as any module that provides the necessary link between two or more other circuits. Examples of such circuitry include bus interface and sample/hold modules. These modules shall be specified so that the performance of the function is ensured.

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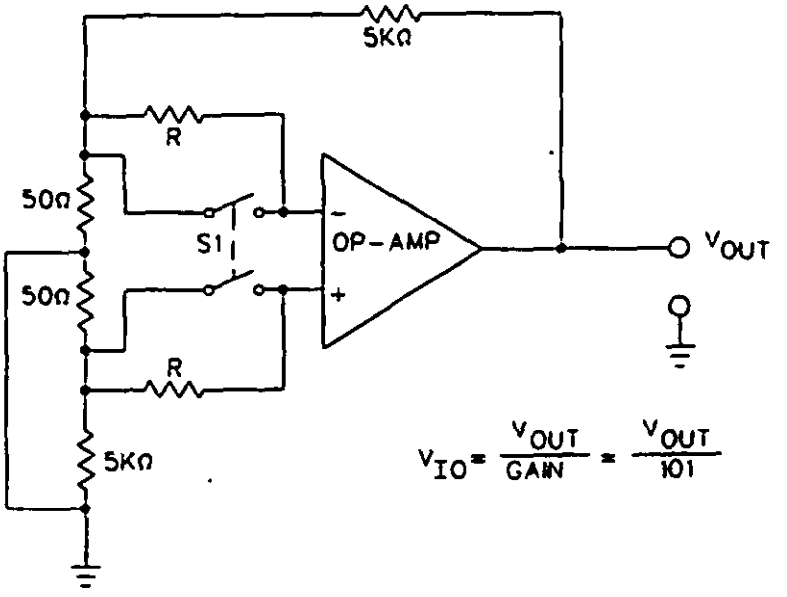

NOTES:
1. This test shall be performed with S1 open ($V_{OUT}1$) for measuring input offset current and with S1 closed ($V_{OUT}2$) for measuring input offset voltage.
2. The resistors from each input to ground shall be matched as closely as possible.
3. For FET input operational amplifiers R greater than or equal 100 kΩ.
4. For bipolar operational amplifiers R equal 10 kΩ.

FIGURE 10. Typical operational amplifier test circuit.

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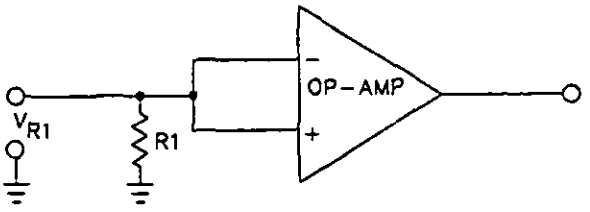


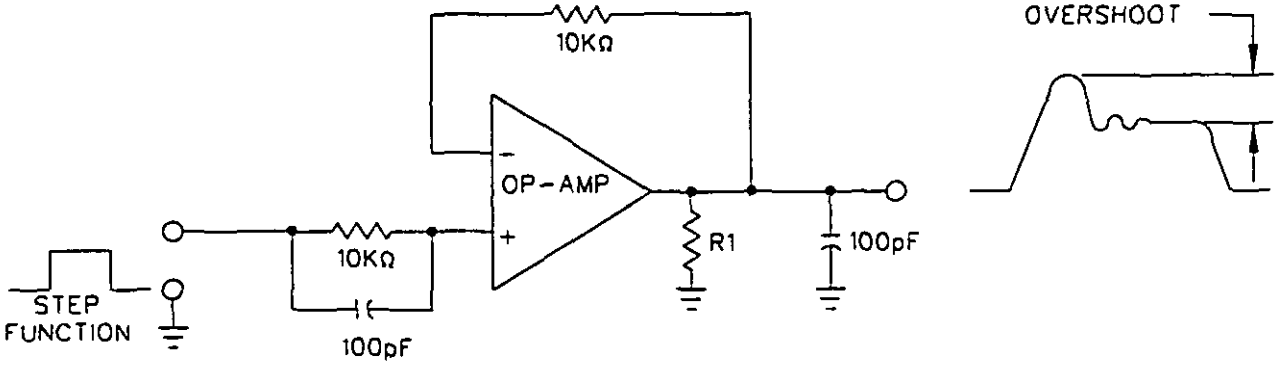
NOTES:

1. Average $I_{IB} = \frac{V_{R1}}{2R1}$ (The value of R1 should be large enough to produce an easily measurable voltage with the expected I_{IB}).

2. This test in conjunction with I_{IO} verifies a maximum

$$I_{IB} = I_{IB}(AVG) + \frac{|I_{IO}|}{2}.$$

FIGURE 11. Typical I_{IB} test circuit.



Note: R1 value depends on the current drive capabilities of the Op Amp.

FIGURE 12. Typical phase margin test circuits.

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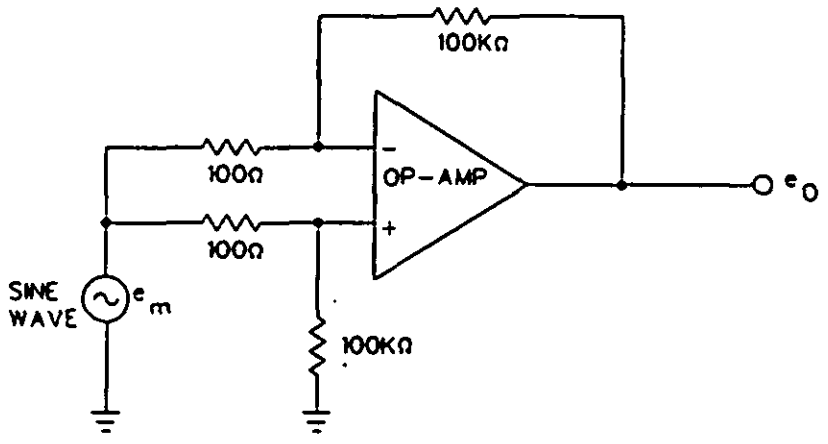

NOTES:

1. The resistors shall be matched to plus or minus 0.1 percent to verify minus 60 dB CMRR.
2. Pick an applicable frequency for e_m.

FIGURE 13. Typical CMRR test circuit.

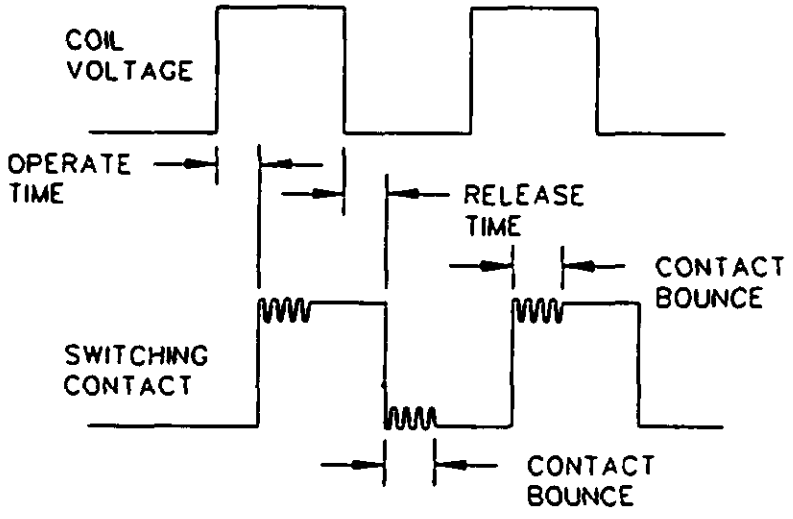

FIGURE 14. Contact switching characteristics.

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1. DOCUMENT NUMBER	2. DOCUMENT TITLE
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3a. NAME OF SUBMITTING ORGANIZATION	4. TYPE OF ORGANIZATION *(Mark one)*
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