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MILITARY STANDARD

PARAMETERS TO BE CONTROLLED

FOR THE SPECIFICATION OF MICROCIRCUITS

FSC 5962

DEPARTMENT OF DEFENSE

WASHINGTON, D. C. 20360

Parameters to be Controlled for the Specification of Microcircuits
MIL-STD-1331

1. This Military Standard was developed by the Department of Defense and the National Aeronautics and Space Administration.

2. This Military Standard is mandatory for use by all Departments and Agencies of the Department of Defense.

3. Recommended corrections, additions, or deletions should be addressed to the Naval Electronic Systems Command, Department of the Navy, Washington, D. C. 20360.

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1. SCOPE

1.1 Scope. This standard describes the parameters required as a minimum for the specification of microcircuits. Parameters, rather than circuits, are considered because circuits vary with the manufacturers involved. Further, circuit designs should be subject to change if improvement results as long as the affected designs are compatible and fully interchangeable. The specific objectives of this document are as follows:

a. To provide the minimum parameters that shall be specified to ensure adequate evaluation of circuit design and performance.
b. To provide maximum commonality of parameters for purposes of test and measurement, within and between major classes of microcircuit types and to allow the recognition of interface problems between types of microcircuits.
c. To provide standard abbreviations, definitions and symbols pertinent to the specification of microcircuits.
d. To promote maximum interchangeability and compatibility between microcircuit types.

2. REFERENCED DOCUMENTS

2.1 The issues of the following documents in effect on the date of invitation for bids form a part of this standard to the extent specified herein.

SPECIFICATION
MILITARY

MIL-M-55565	Microcircuits, Packaging of

STANDARDS
MILITARY

MIL-STD-806	Graphic Symbols For Logic Diagrams
MIL-STD-883	Test Methods and Procedures for Microelectronics
MIL-STD-1313	Microelectronic Terms and Definitions

(Copies of specifications, standards, drawings, and publications required by suppliers in connection with specific procurement functions should be obtained from the procuring activity or as directed by the contracting officer.)

3. DEFINITIONS, ABBREVIATIONS AND SYMBOLS

3.1 For the purpose of this standard, the definitions, abbreviations, and symbols of Appendix A shall apply.

4. REQUIREMENTS

4.1 General. The applicable procurement documents prepared for the procurement of microcircuits shall include, as a minimum, the parameters described herein specified as a function of temperature and any other pertinent conditions as associated with the applicable microcircuit category. The procurement document shall also contain the additional parameters and controls, if any, required for assurance of interchangeability in specific applications. The procurement document shall also identify which parameters are to be tested on a 100 percent basis and which allow sampling. Accept/reject limits for parameter values and acceptable quality levels, where applicable, shall also be included. The terminology and symbols used in the procurement document shall conform to those used herein. The generic term "microcircuit" used in this standard includes all categories of construction as defined in MIL-STD-1313. Where MIL-STD-883 provides test methods for the parameters identified in section 5 or specified in the applicable procurement document, the appropriate test method of MIL-STD-883 shall be used for the measurement or control of those parameters and such use shall be governed by the applicable general requirements of MIL-STD-883.

4.2 Requirements for standardized parameters. In order to best fit the microcircuit user's needs for a standardized set of parameters, the following requirements have been established.

a. All important circuit parameters shall be described.
b. The symbology shall be descriptive of the measured parameters.
c. Test parameters for a given microcircuit type or function shall be specified in such a manner as to be independent of the internal microcircuit construction or the application of the microcircuit.

For logic circuits:

d. Positive current shall be defined as conventional current flow into a device terminal.
e. The limiting terms "min" (minimum) and "max" (maximum) shall be considered to apply to magnitudes only and the sign shall be indicated.
f. V_x shall be considered to be a positive voltage at terminal x with respect to ground or 0 volts. V_{xy} shall be considered to be a positive voltage at terminal x with respect to terminal y.
g. Parameter limits shall be specified under the least favorable appropriate conditions of temperature, biases, supply voltages, signals, and loading within the applicable range of each test condition.

4.3 General items to be controlled. The following items shall be specified for all microcircuit specifications:

a. Storage temperatures (minimum and maximum limits).
b. Lead or Case operating temperature extremes (minimum and maximum limits).
c. Mechanical outline and dimensions
d. Terminal designations
e. Maximum terminal voltage and current (all supplies, inputs, outputs, nodes)
f. Dynamic electrical parameters (see section 5)
g. Static electrical parameters (see section 5)
h. Mechanical and environmental integrity
i. Quality assurance levels and reliability
j. Packaging and packing (refer to MIL-M-55565)
k. Logic diagram, logic equations and truth table (for digital microcircuits) (Logic symbols shall be in accordance with MIL-STD-806.)
l. Complex input and output impedance characteristics when applicable
m. Maximum thermal resistance for the complete microcircuit to the lead or case.
n. Maximum power dissipation per function and for the complete microcircuit.

5. ELECTRICAL PARAMETERS TO BE CONTROLLED

5.1 In all specifications or applicable procurement documents for microcircuits, all applicable electrical parameters of tables I, II, and III shall be specified together with limits and conditions of measurement, and where indicated, the test methods of MIL-STD-883 shall apply. Where "X" appears, the parameter shall be specified, but no MIL-STD-883 test method exists. Standard test methods are being developed.

Table I - Dynamic electrical parameters (Digital microcircuits).

Specify input test conditions: $V_{IH\ min}$, $V_{IH\ max}$, $V_{IL\ min}$, or $V_{IL\ max}$

Parameter	Symbol	Test Method, MIL-STD-883		Remarks
		Gating	Bistable and monostable	
Propagation delay time, low to high level output	t_{PLH}	3003	x	
Propagation delay time, high to low level output	t_{PHL}	3003	x	
Transistion time, high to low level output	t_{THL}	3004	x	
Transition time, low to high level output	t_{TLH}	3004	x	
Power supply current drain vs. frequency		x	x	
Output pulse width (monostable only)				
Terminal capacitance		3012		Where terminal capacitance is regarded as critical to the application.
AC noise margin		3013		Where noise margin is regarded as critical to the application.

NOTE: Forcing conditions which shall be specified (as applicable) for monostable or bistable digital microcircuits are as follows: Asynchronous input, minimum pulse width; Minimum clock pulse width; Clock levels, high and low; Clock repetition rate; Clock level, transition times; Timing relationships of input signals.

Table II - Static electrical parameters (Digital microcircuits).

Specify input test conditions: V_{IH} min, V_{IH} max, V_{IL} min, or V_{IL} max			
Parameter	Symbol	Test Method MIL-STD-883	REMARKS
High level output voltage	V_{OH} max and min	3006	
Low level output voltage	V_{OL} max and min	3007	
High level input current	I_{IH} max and min	3010	
Low level input current	I_{IL} max and min	3009	
High level output current	I_{OH} max and min	x	Measure in conjunction with V_{OH}
Low level output current	I_{OL} max only	x	Measure in conjunction with V_{OL}
Output short circuit current	I_{OS} max and min	3011	
Output leakage current	I_{CEX} max only	x	
Noise margins		3013	Where noise margin is regarded as critical to the application.
Low level supply current drain	I_{CCL}	3005	
High level supply current drain	I_{CCH}	3005	
Breakdown voltage	BV	3008	Where applicable
Where node terminals exist:			
a. High level node current	I_{INH}	3010	At specified V_{INH}
b. Low level node current	I_{INL}	3009	At specified V_{INL}

Table III - Electrical parameters for amplifiers.

		Amplifier Types and Configurations		
		Differential, Video, RF, Gen. Purpose	Operational, Wide Band, IF, Audio Frequency	Audio Frequency, Video, IF, RF, Wide Band, HF, Gen. Purpose
				
Parameters		MIL-STD-883 TEST METHOD		
AC Unbalance	U	X		
Automatic Gain Control Range	AGC	4007	4007	4007
Bandwidth (Small signal)	BW	4004	4004	4004
Common-Mode Input Voltage Range	V_{cmi}	4003	4003	
Common-Mode Output Voltage	V_{cmo}	4003		
Common Mode Rejection Ratio	CM_{rr}	4003	4003	
Common-Mode Voltage Gain	A_{vcm}	4003	4003	
DC Power Dissipation	P_d	4005	4005	4005
Differential Input Impedance	Z_{di}	4004	4004	
Differential Voltage Gain	A_{vd}	4004	4004	
Input Bias Current	I_{ib}	4001	4001	
Input Bias Current Drift	DI_{ib}	4001	4001	
Input Offset Current	I_{io}	4001	4001	
Input Offset Current Drift	DI_{io}	4001	4001	
Input Offset Voltage	V_{io}	4001	4001	
Input Offset Voltage Drift	DV_{io}	4001	4001	
Maximum Output Voltage Swing	V_{om}	4004	4004	4004
Maximum Single-Ended Input Voltage	V_{sim}	X	X	X
Noise Figure	NF	4006	4006	4006
Output Impedance	Z_o	4005	4005	4005
Output Offset Voltage	V_{oo}	X	X	X
Phase Margin	PM		4002	4002
Power Gain	PG		4006	4006
Power Supply Rejection Ratio	PS_{rr}	4003	4003	
Quiescent Input Voltage	V_i			X
Quiescent Output Voltage	V_o			X
Single-Ended Input Impedance	Z_{in}	4004	4004	4004
Single Ended Voltage Gain	A_v	4004	4004	4004
Slew Rate	SL_r		4002	
Total Harmonic Distortion	THD	4004	4004	4004
Transient Response	TR		X	
Maximum Output Swing Bandwidth	BW_{os}			
Overload Recovery Time	t_{OR}			

Custodians:
Army - EL
Navy - EC
Air Force - 17

Review activities:
Army - EL, MU, MI
Navy - AS, OS
Air Force 10, 11, 26, 85
NASA - HQ (KR)

User activities:
Army - ME
Navy - CG
Air Force - 1, 13, 18, 19, 23, 25, 71, 80

Preparing activity:
Navy - EC
(Project 5962-0003)

30.5 Absolute maximum supply voltage. The maximum supply voltage that may be applied without hazard of permanently altering the characteristics of the circuit.

30.6 Asynchronous input minimum pulse width. The minimum pulse width which will assure stable transition of logic levels, according to the truth tables when the asynchronous inputs are returned to their non-controlling level.

30.7 Clock levels, high and low. The clock levels, high and low, are the values (minimum and maximum) of clock voltages, for both high and low levels, which will assure stable transition of logic levels according to the truth table when the clock goes through its required sequence.

30.8 Clock level transition times. The clock level transition times are the transition times (minimum and maximum) of a clock pulse which will assure stable transition of logic levels, according to the truth table, when the clock goes through its required sequence.

30.9 Clock repetition rate. The clock repetition rate is the minimum and maximum rate a clock pulse may repeat logic levels which will assure stable transition of logic levels, according to the truth table, when the clock goes through its required sequence.

30.10 High level input maximum current ($I_{IH\ max}$). The maximum resultant current measured at an input when a specified high level voltage is applied to that input.

30.11 High level input minimum current ($I_{IH\ min}$). The minimum resultant current measured at an input when a specified high level voltage is applied to that input.

30.12 High level node input maximum current ($I_{INH\ max}$). The maximum resultant current measured at an input node with a specified high level voltage applied to that node.

30.13 High level node input minimum current ($I_{INH\ min}$). The minimum resultant current measured at an input node with a specified high level voltage applied to that node.

30.14 High level input maximum voltage ($V_{IH\ max}$). The maximum limit-value High Level Input voltage applied to an input which guarantees operation of the logic element within specification limits.

30.15 High level input minimum voltage ($V_{IH\ min}$). The minimum limit-value High Level Input voltage applied to an input which guarantees operation of the logic element within specification limits.

APPENDIX A

DEFINITIONS, ABBREVIATIONS AND SYMBOLS

10. SCOPE

10.1 The definitions, abbreviations, and symbols used in this appendix are these generally accepted by the electronic industries.

20. ELECTRICAL QUANTITY SYMBOLS

I, i . . . . . current
V, v . . . . . voltage

20.1 Subscript symbols.

20.1.1 Terminals (first subscript)

I . . . . . input
N . . . . . node
O . . . . . output

20.1.2 Logic State (second subscript)

H . . . . . High Level
L . . . . . Low Level

20.2 Defined Value

max . . . . . maximum
min . . . . . minimum

30. DIGITAL MICROCIRCUITS

30.1 Positive logic. The logic is termed positive when logic one is assigned to the HIGH level and logic zero to the LOW level.

30.2 Negative logic. The logic is termed negative when logic zero is assigned to the HIGH level and logic one to the LOW level.

1/ 30.3 LOW level. The LOW level of the two logic levels is that level which has the lesser magnitude.

1/ 30.4 HIGH level. The HIGH level of the two logic levels is that level which has the greater magnitude.

1/ For logic levels which transverse zero volt, the positive and negative levels are defined as the high and low levels respectively.

30.16 High level node input maximum voltage ($V_{INH\ max}$). The maximum limit-value High Level node voltage which guarantees operation of the logic element within specification limits.

30.17 High level node input minimum voltage ($V_{INH\ min}$). The minimum limit-value High Level node voltage which guarantees operation of the logic element within specification limits.

30.18 High level output maximum current ($I_{OH\ max}$). The maximum forced current measured at the output which will guarantee a specified high level output voltage.

30.19 High level output minimum current ($I_{OH\ min}$). The minimum forced current measured at the output which will guarantee a specified high level output voltage.

30.20 High level output maximum voltage ($V_{OH\ max}$). The maximum limit-value of the output voltage in the high level for a specified output current.

30.21 High level output minimum voltage ($V_{OH\ min}$). The minimum limit-value of the output voltage in the high level for a specified output current.

30.22 High level supply current drain (I_{CCH}). The maximum resultant drain current measured at the supply terminal when the output is at a permissible high level voltage.

30.23 Low level input maximum current ($I_{IL\ max}$). The maximum resultant current measured at an input when a specified low level voltage is applied to that input.

30.24 Low level input minimum current ($I_{IL\ min}$). The minimum resultant current measured at an input when a specified low level voltage is applied to that input.

30.25 Low level node input maximum current ($I_{INL\ max}$). The maximum resultant current measured at an input node with a specified low level voltage applied to that node.

30.26 Low level node input minimum current ($I_{INL\ min}$). The minimum resultant current measured at an input node with a specified low level voltage applied to that node.

30.27 Low level input maximum voltage ($V_{IL\ max}$). The maximum limit-value Low Level Input voltage applied to an input which guarantees operation of the logic element within specification limits.

30.28 Low level input minimum voltage ($V_{IL\ min}$). The minimum limit-value Low Level Input voltage applied to an input which guarantees operation of the logic element within specification limits.

30.29 Low level node input maximum voltage ($V_{INL\ max}$). The maximum limit-value Low Level node voltage which guarantees operation of the logic element within specification limits.

30.30 Low level node input minimum voltage ($V_{INL\ min}$). The minimum limit-value Low Level node voltage which guarantees operation of the logic element within specification limits.

30.31 Low level output maximum current ($I_{OL\ max}$). The maximum forced current measured at the output which will guarantee a specified low level output voltage.

30.32 Low level output minimum current ($I_{OL\ min}$). The minimum forced current measured at the output which will guarantee a specified low level output voltage.

30.33 Low level supply current drain (I_{CCL}). The maximum resultant drain current measured at the supply terminal when the output is at a permissible low level voltage.

30.34 Low level output maximum voltage($V_{OL\ max}$). The maximum limit-value of the output voltage in the low level for a specified output current.

30.35 Low level output minimum voltage ($V_{OL\ min}$). The minimum limit-value of the output voltage in the low level for a specified output current.

30.36 Maximum supply voltage ($V_{s\ max}$). The maximum supply voltage that may be applied which will guarantee operation of the logic element within specification limits.

30.37 Minimum supply voltage ($V_{s\ min}$). The minimum supply voltage that may be applied which will guarantee operation of the logic element within specification limits.

30.38 Minimum clock pulse width. The minimum clock pulse width is the smallest pulse width which will assure stable transition of logic levels according to the truth table when the clock goes through the required sequence.

30.39 Noise margin. Noise Margin is defined as the voltage amplitude of extraneous signal which can be algebraically added to the noise-free worst case "input" level before the output voltage deviates from the allowable logic voltage levels. The term "input" is used here to refer to logic input terminals, ground reference terminals or power supply terminals.

30.40 Output leakage maximum current (I_{CEX}). The maximum forced current measured at the collector of an output transistor without a pull-up resistor that will produce a specified high level output voltage.

30.41 Output short circuit current (I_{OS}). The current which flows when an output with a pull-up resistor, which is biased to the output level farthest from ground potential, is short-circuited to ground.

30.42 Propagation delay time, high to low level output (t_{PHL}). The time measured with the specified output changing from the defined high level to the defined low level with respect to the corresponding input transition.

30.43 Propagation delay time, low to high level output (t_{PLH}). The time measured with the specified output changing from the defined low level to the defined high level with respect to the corresponding input transition.

30.44 Pull-up. The establishment of the output voltage in the HIGH level by an internal current sink or source.

30.45 Terminal capacitance. The effective capacitance of each terminal (other than ground) to the ground terminal.

30.46 Timing relationships of input signals (Synchronous and asynchronous and clock). The time relationship which must exist between input signals to insure compliance with the truth table. Times must be specified from positive and negative going edges of the clock pulse.

30.47 Transistion time, high to low level output (t_{THL}). The transition time of the output from 90 percent to 10 percent or 90 percent to a specified value of output voltage with the specified output changing from the defined high level to the defined low level.

30.48 Transition time, low to high level output (t_{TLH}). The transition time of the output from 10 percent to 90 percent or 10 percent to a specified value of output voltage with the specified output changing from the defined low level to the defined high level.

30.49 Truth table. A tabulation relating all output logic levels to all possible combinations of input logic levels for sufficient successive time intervals(t_n, t_{n+1}) to completely characterize the static and dynamic functions of the logic microcircuit, expressed in logic levels (1, 0) or appropriate symbols (that is interrogation mark (?) for an indeterminate level, Qn and $\bar{Q}n$ to express the relationship of successive and complementary outputs). In all specifications for logic microcircuits, the truth table shall be accompanied by a logic equation.

40. LINEAR (ANALOGUE) MICROCIRCUITS

40.1 AC unbalance (U). The Ac unbalance is the difference between the peak values of the AC voltages at the two outputs when the amplifier is operating in the maximum output voltage swing condition.

40.2 Automatic gain control range (AGC). The automatic gain control range is the total change in voltage gain which may be achieved by application of a specified range of DC voltages to the AGC input terminal of the device.

40.3 Balanced amplifier. An amplifier having two inputs and one output is considered balanced when the quiescent DC output voltage is reduced to zero or a specified level. An amplifier having two inputs and two outputs is considered balanced when the difference between the quiescent DC output voltages is reduced to zero or a specified level.

40.4 Bandwidth (small signal) (BW). The bandwidth is the range of frequencies within which the voltage (or current) gain of the amplifier for small signals is not more than 3 db below the value of the midband gain.

40.5 Common-mode input voltage (V_{cm}). The common-mode input voltage is that voltage which is applied simultaneously to both input terminals of the amplifier.

40.6 Common-mode input voltage range (V_{cmi}). The common-mode input voltage range is that range of common-mode voltages which, if exceeded, will cause output distortion, or is that range of common-mode input voltages which may be applied to the input terminals of the device without decreasing the common-mode rejection ratio by more than 6 db.

40.7 Common-mode output voltage (V_{cmo}). The common-mode output voltage is that DC voltage which exists between either output terminal and ground when the difference between the two DC output voltages is reduced to zero or a specified level.

40.8 Common-mode rejection ratio (CM_{rr}). The common-mode rejection ratio is the ratio of the differential open loop gain to the common-mode voltage gain.

40.9 Common-mode voltage gain (A_{vcm}). The common-mode voltage gain is the ratio of the change in voltage with respect to ground of the output terminal (or change in voltage between the output terminals) to the change in common-mode input voltage.

40.10 DC power dissipation (P_d). The DC power dissipation is the total power dissipated in the amplifier with the amplifier biased into its normal operating range and without any output load.

40.11 Differnetial input impedance (Z_{di}). The differential input impedance is the ratio of the change in input voltage to the change in input current seen between the two ungrounded input terminals of the amplifier at the quiescent output DC level.

40.12 Differential input voltage (V_{di}). The differential input voltage is the difference between the instantaneous values of the two voltages applied to the input terminals of an amplifier.

40.13 Differential output voltage (V_{do}). The differential output voltage is the difference between the instantaneous values of the voltages present at the two output terminals when a differential input voltage is applied to the input terminals of the amplifier.

40.14 Differential voltage gain (A_{vd}). The differential voltage gain (open loop) is the ratio of the change in output voltage to the change in differential input voltage in the linear range. For amplifiers having one output terminal, A_{vd} is the ratio of the change in output voltage with respect to ground to the change in differential input voltage.

40.15 Input bias current (I_{ib}). The input bias current is one-half the sum of the separate bias currents entering into the two input terminals of a balanced amplifier, or the bias current entering the input terminal of a single-ended amplifier.

40.16 Input bias current drift (DI_{ib}). The input bias current drift is the ratio of the change in the input bias current, ΔI_{ib}, to the change in circuit temperature, ΔT, for a constant output voltage.

40.17 Input offset current (I_{io}). The input offset current is the difference between the currents entering into the input terminals of a differential input amplifier, or the current entering into the input of a single-ended amplifier, required to force the output voltage to zero or other specified level.

40.18 Input offset current drift (DI_{io}). The input offset current drift is the ratio of the change of input offset current, ΔI_{io}, to the change of circuit temperature, ΔT, for a constant output voltage.

40.19 Input offset voltage (V_{io}). The input offset voltage is that DC voltage which must be applied between the input terminals through equal resistances to force the quiescent DC output to zero or other specified level.

40.20 Input offset voltage drift (DV_{io}). The input offset voltage drift is the ratio of the change of input offset voltage, ΔV_{io}, to the change of circuit temperature, ΔT, for a constant output voltage.

40.21 Maximum output swing bandwidth (MOSW). The maximum output swing bandwidth is the range of frequencies within which the maximum output voltage swing is not more than 3 db below its value measured at the wideband frequency.

40.22 Maximum output voltage swing (V_{om}). The maximum output voltage swing is the maximum peak-to-peak output voltage which can be obtained without waveform clipping when the quiescent DC output voltage is set at a specified reference level.

40.23 Maximum single-ended input voltage (V_{sim}). The maximum single-ended input voltage which if exceeded on any input terminal will cause the total harmonic distortion of the amplifier to exceed the specified maximum value.

40.24 Noise figure (NF). The noise figure is the ratio of the signal-to-noise power ratio at the input to the signal-to-noise power ratio at the output expressed in db.

40.25 Output impedance (Z_o). The output impedance of a differential amplifier is that impedance present between the two output terminals when the amplifier is balanced. The output impedance of a single ended amplifier is that impedance between the output terminal and ground when the amplifier is balanced.

40.26 Output offset voltage (V_{oo}). The output offset voltage is the difference between the DC voltages present at the two output terminals (or at the output terminal and ground for amplifiers with one output) when the two input terminals are grounded.

40.27 Overload recovery time (t_{or}). The time required for an amplifier to recover its ability to perform amplification within stated specification limits after the output voltage amplitude has been distorted by the application of a specified input voltage in excess of rated amplitude.

40.28 Phase margin (PHM). The phase margin is 180 degrees minus the absolute value of the phase shift measured around the loop at that frequency at which the magnitude of the loop gain is unity. The loop is the series path of the device under test and the feedback network which is opened at the inverting terminal. The inverting terminal is loaded down to simulate the load normally presented by the feedback network. Good practice dictates that the phase margin should be at least 45 degrees.

40.29 Power gain (PG). The power gain is the ratio, expressed in db, of the signal power developed at the output(s) of the device to the signal power applied at the input(s). ($db = 10 \log P_o/P_{in}$).

40.30 Power supply rejection ratio (PS_{rr}). The power supply rejection ratio is the ratio of the change in input offset voltage to the corresponding change in one power supply voltage with all remaining power supply voltages held constant.

40.31 Quiescent input voltage (V_i). The quiescent input voltage is the DC voltage present at the input of an amplifier having one input terminal when the input terminal is not connected to any source.

40.32 Quiescent output voltage (V_o). The quiescent output voltage is the DC voltage present at the output terminal when the input is AC grounded through a resistance representing the signal source resistance.

40.33 Single ended input impedance (Z_{in}). The single ended input impedance is the impedance present between one input terminal and ground (with the other input terminal, if any, AC grounded) when the amplifier is balanced.

40.34 Single ended input voltage (V_{si}). The single ended input voltage is that signal voltage which is applied to one input of an amplifier with the other input terminal at signal ground.

40.35 Single ended ouput voltage (V_{so}). The single ended output voltage is the signal voltage present between one output terminal of an amplifier and ground.

40.36 Single-ended voltage gain (A_v). The single ended voltage gain is the ratio of the change in output voltage to the change in single ended input voltage, in the linear range.

40.37 Slew rate (SL_r). The slew rate is the time rate of change of the closed-loop amplifier output voltage for a large step signal input; a large step signal input is the maximum input voltage step for which the amplifier performance remains linear.

40.38 Total harmonic distortion (THD). The total harmonic distortion is the ration, expressed in percent, of the rms voltage of all harmonics present in the output to the total rms voltage of the output for a pure sine wave input. The rms voltages are measured at an output terminal with respect to ground.

40.39 Transient response (TR). The transient response is the closed-loop step function response of the amplifier under small signal conditions.

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- ☐ USER
- ☐ MANUFACTURER
- ☐ OTHER *(Specify)*: _____

b. ADDRESS *(Street, City, State, ZIP Code)*

5. PROBLEM AREAS

a. Paragraph Number and Wording:

b. Recommended Wording:

c. Reason/Rationale for Recommendation:

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7a. NAME OF SUBMITTER *(Last, First, MI)* – Optional

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