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MILITARY STANDARD

TEST POINTS, TEST POINT SELECTION AND INTERFACE REQUIREMENTS FOR EQUIPMENTS MONITORED BY SHIPBOARD ON-LINE AUTOMATIC TEST EQUIPMENT

FSC MISC

DEPARTMENT OF THE NAVY

NAVAL SHIP ENGINEERING CENTER

WASHINGTON, D.C. 20360

Test Points, Test Point Selection and Interface Requirements for Equipments Monitored by Shipboard On- Line Automatic Test Equipment

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1. This Military Standard is mandatory for use by the Department of the Navy.

2. Recommended corrections, additions, or deletions should be addressed to Commander, Naval Ship Engineering Center, Department of the Navy, Washington, D. C. 20360.

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1. SCOPE

1.1 Scope. - This standard establishes the requirements for providing test points in prime equipments for monitoring by on-line automatic test equipment (ATE). It provides criteria for guidance in optimum test point selection. It defines interface and data requirements, a system of test point data generation, and procedures for submission of data disclosing the selections of these test points.

1.1.1 Application. - The requirements of this standard are applicable to the design of equipments intended to be interfaced with an ATE. This standard may also be used for the retrofit of existing equipments for ATE monitoring.

1.1.2 Intent. - It is the intent of this standard to specify the requirements of the procuring activity to achieve the following objectives:

(a) The optimum selection and placement of test points to:
  (1) Continuously monitor the performance of prime equipment.
  (2) Indicate the existence of a failure.
  (3) Facilitate rapid isolation of a failure to the line replaceable unit to effect repair by substitution of a spare, performance of realignment, etc.

(b) The planning and development of an adequate level of test logic design for the prime equipment in order that the ATE can be programmed to provide optimum monitoring of the sensor outputs, and to insure timely delivery of the end article and all of the required test point information.

(c) The definition of the types of test point signals and their dimensions that may be provided for ATE monitoring.

2. REFERENCED DOCUMENTS

2.1 The issues of the following documents in effect on the date of invitation for bids form a part of this standard to the extent specified herein.

GOVERNMENTAL

SPECIFICATION
MIL-T-24309 - Technical Support Plans for Electronic Equipment.

STANDARD
MI L-STD-1309- Definition of Terms for Automatic Electronic Test and Checkout.

PUBLICATION
NAVSHIPS 93820- Handbook for the Prediction of Shipboard and Shore Electronic Equipment Reliability.

(Copies of specifications, standards, drawings, and publications required by suppliers in connection with specific procurement functions should be obtained from the procuring activity or as directed by the contracting of ficer.)

3. DEFINITIONS

3.1 The definitions of MIL-STD-1309 apply. The following definitions are defined as related specifically to this standard.

3.1.1 ATE. - An abbreviation of the term “Automatic Test Equipment.”

3.1.2 Prime equipment. - An equipment or system that is to be monitored by an ATE.

3.1.3 Sensor. - Circuitry and related hardware located within the prime equipment for the purpose of providing a suitable test signal for the ATE, isolating the prime equipment in the event of an ATE failure, and preventing unwanted RFI from being present in the sensor output.

3.1.3.1 Passive sensor. - A sensor requiring no source of power other than the signal being measured.

3.1.3.2 Active sensor. - A sensor requiring a source of power in addition to that of the signal being measured.

3.1.4 ATE test point. - A sensor output which is brought to an accessible location for connection to the ATE.

3.1.5 Circuit test point. - That point considered physically in the prime equipment, exclusive of isolation and sensing circuitry.

3.1.6 Simple test point. - A test point at which the parameter of interest is continuously present.

3.1.7 Complex test point. - A test point at which the parameter of interest is present only when stimulated or activated by means of the ATE program.

3.1.8 Virtual test point. - A point in the prime equipment about which information is known by virtue of processing information from actual ATE test points.

3.1.9 Module. - A physically independent assembly whose boundaries are determined by facile replacement as reflected by the applicable maintenance policy.

3.1.10 Functional entity. - The components within a theoretical boundary which are related to perform a specific function, that is, amplification, gating, filtering, etc.

3.1.11 On-line. - Monitoring and testing in a non-interfering manner while the prime equipment is in normal operation use.

4. GENERAL REQUIREMENTS

4.1 Purposes of test points. - ATE test point signals will be utilized to provide an indication of equipment performance and to permit fault location to the replaceable module or functional entity. They shall be compatible with the system circuitry to minimize the possible losee of performance occasioned by their use. A sufficient number of test points shall be provided to facilitate the location of the most probable type of circuit malfunctions which may be reasonably expected to occur. Consideration shall also be given to the monitoring of non-electrical parameters such as equipment ambient temperature, ventilation, air velocity, etc., if such measurements will materially reduce fault location time or provide advance warning of potential failures.

4.2 Information and performance degradation. - The prime equipment will be monitored while energized and in normal operation, therefore information available at test points shall not be degraded by manipulation of normal operator controls, nor shall there be any degradation of the equipment performance due to the choice of circuit test point location. In the event of a malfunction shorting an ATE test point; damage or performance degradation shall not be sustained by the prime equipment.

4.3 Grounding. - All ATE test point output signals shall be measured relative to a common prime equipment circuit ground which can also be grounded at the ATE. Due consideration shall be given to isolation, decoupling, and multiple and single point ground requirements. A common prime equipment circuit ground connection shall be provided for the ATE.

4.4 Sensor preference. - Passive sensors shall be used in preference to active sensors wherever possible. Where active sensors are used to provide information not obtainable by passive sensors, there shall be a minimal effect on the reliability of the circuit-sensor combination.

4.5 ATE input impedance. - Each ATE test point signal output shall be capable of driving a capacity load of up to 1000 picofarads in parallel with the ATE resistive load of one megohm.

4.6 Sensor calibration. - Sensors requiring calibration, initial or otherwise should be avoided (see 5.7).

4.7 Sensor repeatability. - The ATE test point signal repeatability tolerance (long term) shall be, at most, one-fourth the tolerance of required measurement accuracy.

4.8 Test point output location. - All ATE test points and the prime equipment common circuit ground(s) shall be brought to an accessible multiplepin receptacle(s) mounted on or close to the prime equipment enclosure skin and providing termination suitable for cable connection to the ATE. Connector selection and pin assignment shall maintain integrity of line separation dictated by prime equipment for isolation of cross talk between RF, digital and analog, and d.c. signals.

4.9 Connectors. - Connectors shall conform to the detail or performance specifications for the original design or retrofit of existing prime equipment.

4.10 Shielding. - All sensors shall be designed so that interference caused by electromagnetic radiation is minimized through the use of good design principles and by filtering and shielding where necessary.

Electromagnetic interference requirements in detail or performance specifications for the original design or retrofit of existing prime equipment shall apply with the ATE test points unloaded or connected to the ATE.

4.11 Decoupling .- Adequate decoupling shall exist between the test point and the prime equipment so that degradation of equipment performance or introduction of extraneous signals does not occur before or after connection of the ATE.

4.12 Marking. - All test points terminating in jacks, sockets, or connectors shall be marked in a readily visible fashion, with markings conforming to the requirements specified in the detail or performance specification covering the prime equipment.

5. ATE MEASUREMENT CAPABILITY

5.1 General. - The ATE will have a capability to make the following types of measurements within the limitations specified in 5.2 through 5.6.3:

(a) D.C. voltages.
(b) Pulse parameters.
(c) Time interval.
(d) Frequency.

5.2 D.C. voltage measurements .-

5.2.1 General - The ATE will be capable of measuring d.c. voltages within the range of 0 to plus or minus 10 volts. However, to insure detection and measurement of abnormal voltages when they occur, each d.c. type sensor output shall fall within the range of 250 millivolts minimum to 6.67 volts maximum when monitoring a "normal" prime equipment signal for an overall ATE system accuracy of plus or minus 1 percent; lower voltage down to 50 mv, can be accommodated at reduced accuracy. In special cases where a "normal" sensed signal may vary from a positive value through zero to a negative value (or vice versa), a bipolar ATE measurement capability will be provided and the minimum voltage limit is waived.

5.2.2 ATE voltage ranges. - Zero to plus or minus 1.0 volt, O to plus or minus 3.33 volts, and O to plus or minus 10.0 volts.

5.2.3 ATE resolution of measurement. - One thousand digital increments per voltage range, zero to full scale (2,000 digital increments bipolar).

5.2.4 ATE input impedance. - One megohm resistive.

5.2.5 Modulation. - A.C. ripple or modulation superimposed on the d.c. signal will affect the measurement. A d.c. measurement will be in error by an amount equal to the peak amplitude of the unwanted modulation superimposed on the desired d.c. output and therefore it should be minimized.

5.2.6 Proportionality and off set.- Variation in a d.c. sensor output voltage shall be directly proportional to the variation in prime equipment signal being monitored. A d.c. offset may be present.

5.2.7 Maximum output. - The d.c. sensor output shall not exceed 12 volts in amplitude. This shall include predictable type failures of the prime equipment.

5.3 A.C. voltage measurements. -

5.3.1 Conversion. - Prime equipment a.c. voltages chosen to be monitored shall be converted by the sensor to a proportional d.c. voltage.

5.3.2 Measurement. - After conversion to d.c. by the sensor, the d.c. voltage measurement specifications of 5.2 shall apply.

5.4 Pulse parameter measurements. -

5.4.1 Capability. - The following ATE pulse parameter measurement capability will be provided unless the requirements of 5.4.13 are invoked by the procuring activity:

(a) Risetime (time interval measurement).
(b) Falltime (time interval measurement).

(c) Pulse width (time interval measurement).
(d) Pulse amplitude (voltage amplitude measurement).

5.4.2 Repetitive pulses required. - For the ATE to make a pulse parameter measurement, at least two pulses must occur at the monitored point after the ATE request for measurement. The ATE measurement facility is "enabled" by the first pulse that occurs and then makes the measurement on the next pulse that follows.

5.4.3 Measurement. - Risetime, falltime, and amplitude pulse parameter measurements are made from the approximate 0 percent (0.5 volt at the data converter output) to the 100 percent of pulse amplitude. Overshoot will have a negligible effect on the pulse amplitude measurement if the width of the overshoot does not exceed 10 percent of the total pulse width. Pulse width is measured between the approximate 0.5 volt (the conduction point of silicon semiconductor devices) amplitude levels on the pulse.

5.4.4 Time interval resolution. - The resolution of pulse parameter time interval measurements is in 50 nanosecond increments up to 1.638 milliseconds; 1.0 microsecond increments from 1.638 to 32,767 milliseconds.

5.4.5 Pulse amplitude measurements. - The ATE will measure pulse parameters on positive or negative pulses within the ranges of 1.5 to 6.0 volts in amplitude within an accuracy of plus or minus 1 percent of full scale. A "normal" sensor pulse output shall be within the range of 2.5 to 4.0 volts in amplitude. A sensor peak pulse output amplitude shall not exceed 6.0 volts relative to circuit ground.

5.4.6 Pulse duration. - During a pulse risetime, falltime, or width measurement, the pulse parameter measured must have a duration of more than 50 nanoseconds and less than 32.767 milliseconds. During a pulse amplitude measurement, the pulse must have a minimum duration of 50 nanoseconds, with no maximum limit.

5.4.7 Minimum time interval between pulses .- At least 50 nanoseconds.

5.4.8 Multiple parameter measurements on a single pulse. - More than one type of pulse parameter meas - urement can be made by the ATE on a single ATE test point output from the prime equipment. The ATE load will remain a constant (see 5.4.10).

5.4.9 Waveform integrity .- In order to preserve waveform integrity to the ATE, consideration shall be given to compensate for cable capacitance that may range in value up to 1000 picofarads.

5.4.10 ATE input impedance. - 1.0 megohm resistive loading shunted by the interconnecting cable capaci- tance (up to 1000 picofarads).

5.4.11 Optional ATE input impedance .- With justification ATE input impedance of less than 1.0 megohm will be provided (for example 50 ohms), upon request by the contractor.

5.4.12 Offset. - Sensor outputs for pulse parameter measurement shall not have d.c. offset exceeding 100 millivolts unless prior approval is obtained.

5.4.13 Pulse conversion. - When specifically required by the procuring activity, pulse parameters to be measured shall be converted to a d.c. analog with output in accordance with the requirements of 5.2.

5.5 Time interval measurements. - Unless otherwise specified, time interval measurements shall be as specified in 5.5.1 through 5.5.7.

5.5.1 General. - Time interval measurements can be made by the ATE between successive pulses, sinusoidal, or other type periodic waves that occur in repetitive nature and are available from a single sensor. Time inter- val measurements between pulses on different ATE test point outputs can be made as a special requirement (see 5.7).

5.5.2 Time interval measurement capability. - From 50 nanoseconds minimum to 32.767 milliseconds maximum.

5.5.3 Pulse requirements. - Same as for pulse parameter measurements specified in 5.4.

5.5.4 Sinusoidal or other periodic wave requirements. - The periodic wave shall be centered around a zero voltage axis, 3.0 volts minimum to 12.0 volts maximum peak-to-peak amplitude.

5.5.5 ATE measurement resolution. - The resolution of measurement is in 50 nanosecond increments up to 1.638 milliseconds; 1.0 microsecond increments from 1.638 to 32.767 milliseconds.

5.5.6 Maximum output. - A sensor periodic wave amplitude shall be guarded against rising above plus or minus 6.0 volts relative to circuit ground. Maximum pulse amplitudes are specified in 5.4.

5.5.7 Accuracy. - The ATE resolution accuracy of time interval measurement is shown on figure 1.

5.6 Frequency measurements. - Unless otherwise specified, frequency measurements shall be as specified in 5.6.1 through 5.6.3:

5.6.1 General. - Frequency measurements are obtained by an ATE processor translation of a time interval measurement (see 5. 5). Using this method the frequency of a periodic repetitive type waveform can be obtained by a time interval measurement of a single cycle, which is then converted to a corresponding frequency reading.

5.6.2 Frequency range measurement capability. - Minimum frequency 30 cycles per seond. Maximum frequency 1.0 megacycle.

5.6.3 Accuracy. - The ATE resolution accuracy of frequency measurements is shown on figure 2.

5.7 Special requirements. - If, after a study of test point logic, the contractor believes that adequate fault isolation can be achieved only through the use of sensor calibration, complex test points, special ATE measurement ranges or accuracies, stimulus injection, or comparison of outputs of different sensors, the contractor may petition the procuring activity to grant a waiver of the aforementioned constraints, if it will materially benefit ATE monitoring of the prime equipment. A technical description of the proposed action shall be submitted to the procuring activity for review. The technical description shall contain a functional description and reason for the action. Data such as schematics, block diagrams, and engineering sketches depicting information necessary for an engineering evaluation of the proposed action shall be prepared and submitted as part of the technical descriptions.

5.7.1 Stimulus generator. - The contractor shall submit proposals for stimuli as needed. At the option of procuring activity, the contractor may be required to provide or build into the prime equipment the stimuli required. The procuring activity will provide stimulus control information.

6. TEST POINT SELECTION

6.1 Philosophy .- Circuit test points shall be selected on their ability to detect and isolate faults with a maximum degree of confidence to the lowest level practical, at a minimum cost. Circuit test point placement shall be such that the degree of automatic testing reflects the repair philosophy dictated by physical configuration of the design. Since two types of repair are possible, piece-part and module replacement, it is necessary to approach these problems differently.

6.2 General criteria. - The following general criteria for circuit test point selection shall be applied to both piece-part and modular replacement.

6.2.1 Order of priority. - Priority should be given to the testing of functions that are most important to the operational mission, that are least reliable, or are the least accessible.

6.2.2 Interface monitoring. - A sufficient number of circuit test points shall be provided to cover major prime equipment interface signals to insure information flow to the ATE in the event of major prime equipment failure.

6.2.3 Parameter choice. - The parameter chosen for monitoring at a circuit test point should be the one that most closely represents the performance of the function of the associated module(s) or functional entities.

6.2.4 Fail safe. - The connection to the circuit test point by any sensing circuitry necessary shall be in a fail safe manner whenever possible; the unfeasibility of this, however, is not considered sufficient grounds for not testing a particular function.

6.2.5 Displayed signals. - In general, displayed signals over which a prime equipment operator must maintain constant cognizance may be monitored by ATE.

6.2.6 Simple test points. - Circuit test point selection shall be limited to simple test points except as specified in 5.7.

6.2.6.1 Simple test points in fault isolation. - In fault isolation, the test point shall be simple in the mode in which isolation is performed, except as specified in 5.7.

6.2.7 Use of virtual test points.- Performance monitoring and fault location at a point shall be available from a single sensor. In the event that the sensing circuitry necessary to monitor the key parameter(s) of the signal would degrade the performance of the circuit, would be difficult to install or would seriously degrade the reliability, consideration shall be given to obtaining the information at this test point through ATE evaluation of a group of interrelated test points; such a circuit test point shall be considered to be monitored by a virtual test point.

6.2.7.1 Justification of virtual test points. - The contractor may utilize virtual test points providing he supports their necessity by submission of an engineering analysis. This analysis shall include a written disclosure, text and supporting drawings as follows:

(a) The proposed sensing circuitry shown connected to the module or functional entity in question.
(b) Quantitative analysis showing the performance degradation, if any, incurred by insertion of the sensing circuitry.
(c) A failure rate calculation, made according to NAVSHIPS 93820 or other technique acceptable to the procuring activity showing an appreciable (at least 1.1 times) increase, if any, in failure rate of the module or functional entity when the sensing circuitry is connected and included in the calculation. Interconnecting wires or cabling necessary to bring the sensed parameter to the surface of the cabinet shall be assumed as having a failure rate of zero. The procuring activity retains the option of requiring the use of sensors incurring degraded reliability if deemed important enough for the coverage of the prime equipment.

6.2.8 External power monitoring. - A separate ATE test point, with a d.c. type output, shall be provided to monitor each equipment primary supply voltage obtained from external sources. It shall monitor presence of the voltage, not a switch position.

6.2.9 Mode monitoring. - A separate test point shall be provided to monitor each normal of operation or condition that can be selected by an operator. These test points shall have d.c. binary type "true/false" outputs.

6.3 Modular criteria. - The criteria for circuit test point selection applied to modularized equipments or to modularized portions of equipment shall be as specified in 6.3.1 through 6.3.3.

6.3.1 Level of isolation. - Sufficient test points shall be placed in the equipment to allow ATE fault isolation to each replaceable module.

6.3.2 Isolation precision. - An out of tolerance indication at a test point shall unambiguously imply a failure within the module in question when no other failure indication exists.

6.3.3 Unmonitored modules. - A module may go untested only if the contractor can justify the inability to use an ATE test point with data required in 6.2.7.1, and in addition shows that information concerning the status of the module cannot be determined by other sensors (virtual test point).

6.4 Non-modular criteria. - The criteria for circuit test point selection applied to non-modularized equipment or to non-modularized portions of equipment shall be as specified in 6.4.1 through 6.4.3.

6.4.1 Level of isolation. - The contractor shall define each functional entity in accordance with 3.1.10 by solid lines drawn on the blocked schematic (see appendix). A sufficient number of ATE test points shall be placed in the equipment to allow ATE fault isolation to each functional entity.

6.4.2 Isolation precision. - An out of tolerance indication at a test point shall unambiguously imply a failure within the functional entity in question when no other failure indications exist.

6.4.3 Unmonitored functional entities .- A functional entity may go untested only if the contractor can justify the inability to use an ATE test point with data required in 6.2.7, and in addition shows that information concerning the status of the module cannot be determined by other sensors (virtual test point).

7. DELIVERABLE ITEMS

7.1 Items. - The contractor shall submit for approval the following items (6 copies) to the procuring activity by the dates specified at the guidance meeting, to allow an effective review of the test point selection:

(a) Block diagram(s) and blocked schematic (s) (see apendix).
(b) Power distribution diagram(s) (see appendix).
(c) Design outline (see appendix).
(d) Test logic flow diagram.
(e) Test logic chart(s) (see figure 3).
(f) Test point data sheet(s) (see figure 4).
(g) List of modules or functional entities not covered in (f) above, and supporting documentation as specified in 5.7 and 6.2.7.1.
(h) Other supporting data or information deemed pertinent by the contractor.

7.2 Test point data sheet. - A list of all ATE test points shall be prepared with the following information detailed for each test point (see example, figure 4):

(a) Test point number - A number in a simple alpha-numeric code to be composed by the contractor to identify each ATE test point.
(b) Circuit drawing number - The identification of the circuit drawing which depicts the circuit containing the related circuit test point.
(c) Connector number - The identification of the connector (see 4.8) which contains the sensed information of the ATE test point.
(d) Connector pin number - The identification of the specific pin in the connector which contains the sensed information of the ATE test point.
(e) Module or entity number - The identification number (see appendix for method of establishment) of the module or functional entity which the circuit test point locates or monitors.
(f) Circuit test point - The precise description of the location of the circuit test point within the prime equipment circuitry, that is, junction of R112 and C62.
(g) Parameter measured - The statement of the key parameter, selected as specified in 6.2.3, to be monitored at the circuit test point.
(h) Parameter characteristics - The nominal value(s) and dimensions of the key parameter.
(i) Upper and lower parameter limits - The maximum and minimum values of the key parameter between which the parameter indication is considered “go.”
(j) Test point source impedance - The nominal value of impedance seen by the ATE looking into the connector pin specified in (d) above.
(k) ATE test point signal characteristics - The nominal value(s) and dimensions of the sensor output as it appears at the output connector.
(l) Upper and lower ATE test point limit - The maximum and minimum values of the sensor output between which the signal indicates a “go” condition.
(m) Initial calibration required - A yes or no indication as to whether or not an initial calibration of the sensor is required.
(n) Frequency of calibration - The frequency of calibration required, if any, by the sensor to retain its accuracy.
(o) Remarks and additional information - Any relevant information considered pertinent or necessary.

7.3 Recommended test logic. - A separate test logic chart shall be submitted for each normal mode(s) of prime equipment operation that has a unique selected group of test points to be monitored. Based on the total field of test points selected the contractor shall arrange the test points into a recommended logical hierarchy abstracted from the design outline (see 7.1 (c)) for ATE sequential monitoring. Certain key test points shall be designated as performance monitoring points and shall be kept to a minimum. Performance monitoring test points, whose indications may depend upon indications of other test points, shall be the ones which are capable of monitoring the performance of an entire equipment or a major portion of an equipment. The relationship of performance monitoring test points, external power source test points, equipment mode test points, fault location test points and virtual test points shall be graphically indicated on a test logic chart similar to figure 3. Each test point shall be identified by its test point number.

8. DESIGN REVIEW CONTROL

8.1 Guidance meeting . - After award of the contract, but not more than 90 days thereafter, the contractor shall request and recommended a date for a meeting to be arranged by the procuring activity. The purpose of the meeting will be to arrive at a format and timetable for data submission, and to delineate the particulars of the design review cycle as called out in the contract. This meeting may be part of the over-all guidance meeting called for in MIL-T-24309.

8.1.1 Prepartion for guidance meeting.- The contractor shall prepare and submit to the procuring activity, a skeleton data presentation format depicting the proposed form of data submission in response to section 7 of this standard. This submission should include the information described herein, in addition to other documentation

deemed necessary for the conduct of design review.The submission should precede the meeting date by at least 4 weeks in order to facilitate guidance.

8.2 Preparation and submission of data. - Six copies of all data required by 7.1 shall be submitted to the procuring activity as the information is developed in accordance with a schedule determined at the guidance meeting of 8.1. The contractor shall review the comments submitted on the interim data and make all modifications, deletions and additions required. The final submission shall include all corrections and shall form the final ATE test point data requirements.

9. VERIFICATION

9.1 All parameters required by 7.2 for ATE test points shall be verified by actual measurement on the produced equipment.

Review activities:
Navy-SH,AS,EC,OS

Preparing activity:
Navy-SH
(Project MISC-N492)

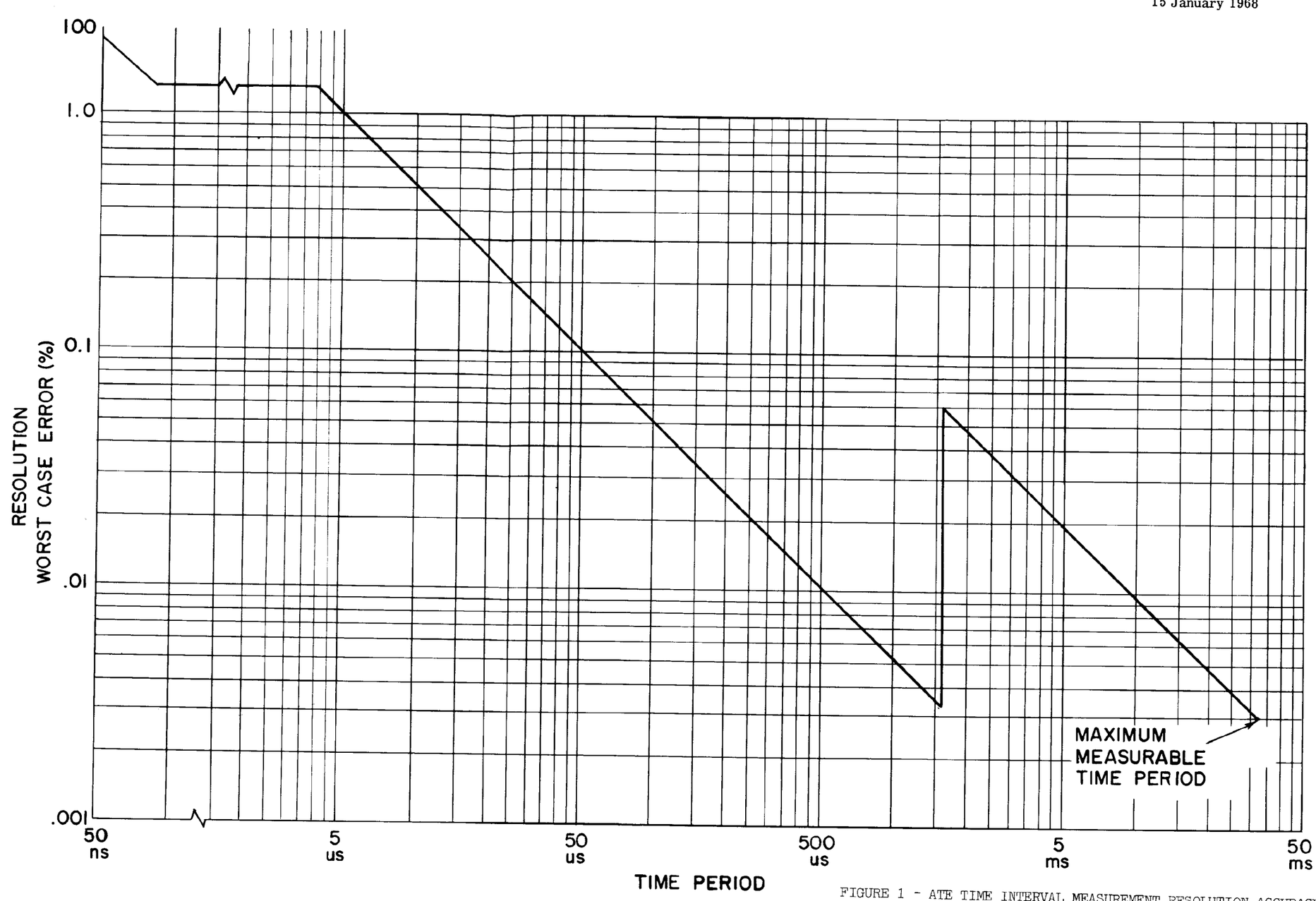


FIGURE 1 - ATE TIME INTERVAL MEASUREMENT RESOLUTION ACCURACY.

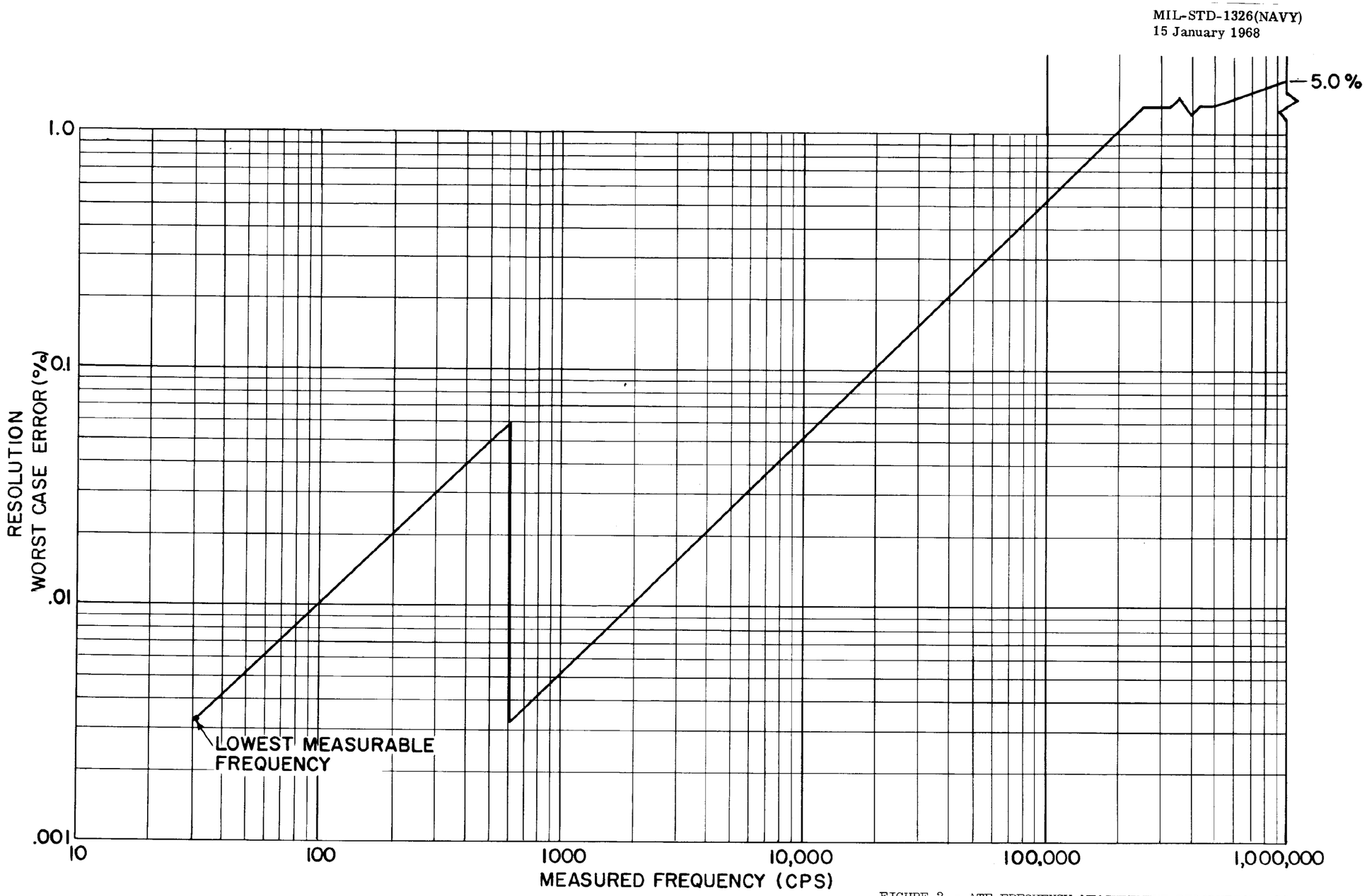


FIGURE 2 - ATE FREQUENCY MEASUREMENT RESOLUTION ACCURACY.

PERFORMANCE Monitoring TEST POINT NUMBER	FAULT ISOLATION TEST POINT NUMBER			REPLACEABLE MODULE OR FUNCTIONAL ENTITY NUMBER	MODE IDENTIFICATION TEST POINTS

FIGURE 3 - TEST LOGIC CHART.

ATE TEST POINT NO.	CIRCUIT DRAWING NO.	CONNECTOR		CIRCUIT LOCATION		PARAMETER MEASURED	CIRCUIT PARAMETER CHARACTERISTICS	CIRCUIT PARAMETER LIMITS		ATE TEST POINT SOURCE IMPEDENCE	ATE TEST POINT SIGNAL CHARACTERISTICS	ATE TEST POINT LIMITS		CALIBRATION REQUIRED		REMARKS AND ADDITIONAL INFORMATION
		CONNECTOR NO.	PIN NO.	MODULE OR ENTITY NO.				UPPER	LOWER			UPPER	LOWER	INITIAL	FREQUENCY	

FIGURE 4 - TEST POINT DATA SHEET.

APPENDIX - DISCLOSURE FORMATS

10. INTRODUCTION

10.1 This appendix describes the formats for a system of diagrams to disclose each level of system design These diagrams shall be integrated, that is, in general each block on one level should be an entire drawing on the next lower level. As an example, if the blocks on cabinet functional drawings are circuits they should be disclosed as schematics at the next lower level; or, if they are assemblies or subassemblies then the next lower level of disclosure would still be block diagrams. Thus the contractor, in this example, would provide one master block diagram, several intermediate block diagrams, and a corresponding number of blocked schematics. For simpler systems the blocked schematics may be sufficient.

10.2 The formats set forth in this appendix are those portions of the U.S. Naval Applied Science Laboratory Design Disclosure Format (DDF) deemed pertinent to this standard and modified to meet its specific needs. These formats shall be utilized by the contractor to enable the procuring activity to effectively analyze, review, and control the test point selection and the ATE interface. At all times, the objective shall be to provide clear, and concise documentation of the required items. Where new or unique situations which are not specifically covered by this standard are encountered, the principles of formating shall be extrapolated by the contractor. In all cases, the procuring activity retains the right of inspection and approval of the final product. The requirements for these disclosure formats will vary with the size and type of equipment. The procuring activity may modify requirements at the guidance meeting to meet the specific needs of a particular equipment. The finalized formats shall be used as inputs for the preparation of, or as appendices to, the prime equipment technical manuals.

20. BLOCK DIAGRAM

20.1 General considerations. -

20.1.1 Layout. - The layout of the block diagrams should be purely functional and should not be compromised in order to keep hardware or functional boundaries square or rectangular. Hardware boundaries and functional boundaries may be distorted as necessary to keep main signal flow generally from left to right and feedback signal flow from right to left. Input signals should appear on the far left of the page, while output signals should appear on the far right of the page. The technical layout should never be distorted solely for artistic balance or to fill up white space.

20.1.1.1 Hardware boundaries. - Heavy long dash-short dash lines are used to define hardware boundaries.

20.1.1.2 Hardware reference designations and nomenclature. - Each assembly or subassembly which has a military nomenclature and reference designation, or other identifying number is labelled with a reference designator (see figure 5), followed by the official nomenclature printed-in the upper left corner of the hardware boundary, or upper left corner of page if circuitry shown represents only a portion of that hardware boundary. If official nomenclature is not assigned, descriptive nomenclature may be used.

20.1.1.3 Functional boundaries. - Each function shall be contained within a thin solid line which defines the functional boundary. On the lowest level of disclosure, the blocked schematic, the solid lines depict functional entities (see 3.1.10). On all higher levels the solid lines depict functional blocks. Therefore every circuit element on the blocked schematic must be enclosed by either a solid line or a heavy long dash-short dash line (see 20.1.1.1).

20.1.1.4 Functional identifier codes and nomenclature. - Each functional block or entity is assigned an identifier code which is printed in the upper left corner of the functional boundary, such that it uniquely identifies each function in the prime equipment. This code may be followed by descriptive nomenclature if it addes further clarification (see figure 6). The identifier code consists of a group of alpha units and a number. The alpha group designates the function of the circuit, while the numeric part of the code differentiates between similar types of functions used more than once in an equipment. A list of sample identifier codes is given in figure 7. This list is provided as a guide and is not to be considered all inclusive. New codes can be generated where the need demands. Piece-parts do not have a code and are identified by reference designators only.

20.1.1.5 Sensors. - Sensors are to be considered as part of the prime equipment. They need be shown only at the most detailed level of disclosure, that is, the blocked schematic and the power distribution diagrams. Sensors shall be separated from the functional circuit elements, and drawn at the top of their respective diagrams, enclosed by a thin solid line. They are not shown connected to the circuit by solid lines, rather, the connection is implied through the use of break symbols for the signal path. To facilitate connection between break symbols, they should be aligned vertically, and the test point number should be indicated at the break symbols. Examples

are shown on figures 8, 9 and 6. Sensors shall be labelled in the upper left corner with their reference designators and descriptive nomenclature.

20.1.1.6 Circuit test points. - Circuit test points shall be drawn as shown on figure 10. Circuit test points shown on blocked schematics shall be drawn at the point of circuit measurement. On higher level block diagrams, circuit test points monitoring the outputs of blocks shall be ties to the signal flow paths between blocks. Circuit test points which provide isolation to a level more detailed than the diagram under consideration need not be shown on the diagram. All circuit test points shall be shown on the blocked schematics.

20.1.1.7 Wrap around schematic information. - Cabinets and other wrap around devices frequently have components such as switches, relays, termination resistors, etc., mounted directly on the cabinet. For purposes of this standard, a wrap around is defined as an enclosure and contiguous elements which remain after complete removal of assemblies, chassis, printed circuit cards or anything else normally removed for maintenance. Wrap around schematic data shall appear on either the detailed block diagram or the power distribution diagram.

20.1.1.8 Coded signal flow. - Signal flow is coded by use of special arrowheads and appropriate annotations. Figure 10 lists the various types of signal flow codes used. These codes are not to be considered all-inclusive. If required, new coded signal flow arrowheads should be generated.

20.1.1.9 Signal names and waveforms. - All input and output signals are to be clearly identified and a complete and accurate description of each shall be given. Signals generated in an assembly which connect to output plugs but are not used are labelled “NOT USED.” Signals of special importance may be identified by using signal name flags pointing to the signal path to be identified. Waveforms at significant points throughout the diagrams may be added if needed for clarity.

20.1.1.10 Adjustments and controls. - Adjustments and controls may be included in the drawing if they enhance the functional understanding of the circuit. They should not be added if the number of controls is large and would tend to complicate the drawing. If the adjustment is a front panel adjustment, accessible with the equipment under normal operation, the symbol and adjustment nomenclature shall be enclosed within a solid light line with the lower right corner darkened. A list of sample symbols is shown on figure 10. This list is provided as a guide, and is not to be considered as all inclusive.

20.1.1.11 Mechanical connection separation techniques. - When multi- section switches, ganged potentiometers, or relays have more than one element or contact set, the sets or elements shall be nomenclature individually but with some common alpha-numeric relationship. It is desirable to graphically align the contact sets vertically or horizontally if possible, but not at the expense of functional flow. Relays and switches will not necessarily have their contact sets operating in the same functional area; often they will function in different circuits. When this occurs, the various sets of contacts and actuating elements are connected by a dashed line to illustrate mechanical linkage. If the elements of these parts are separated so that a long dashed line destroys the clarity of the diagram and must be broken up to preserve functional signal flow, the following techniques is to be used to locate the various parts. At the bottom of figures 8 and 9 two triangles labelled R19 are shown. Directly above these triangles are two identical triangles shown mechanically connected to sections of potentiometer R49. The triangles indicate a mechanical break. The labelling indicates the reference designator of the part. On a complex drawing, other sections of a multi-section part can be quickly found by referring to the bottom of a page and locating other triangles with the same reference designator.

20.1.1.12 Spares information. - Spare relay contacts, connector pins, terminal connectors, switch contact sets, etc., which are available for future use, are not shown on the body of the drawing but listed in tabular form in the note area of the illustration.

20.1.2 Text. - Corresponding to every functional block, functional entity, and module on the diagrams, there shall be an explanatory test (see figure 11). The text shall provide the following information:

(a) Identifier code (functional entities or blocks) or reference designator (modules).
(b) A description of what function(s) it performs.
(c) Timing information, where applicable.
(d) Theory of operation (for unusual circuits).
(e) Logic equations for digital circuits.

Text corresponding to a functional entity or module describes the operation of the circuit parts within. Text corresponding to functional blocks describes their operation in relation to other functional blocks. Modes of operation should be discussed if important.

20.1.2.1 Simplified circuits. - Since all circuits are drawn in their most familiar form, simplified diagrams are not used. However, on occasion, simplified circuits may be used to support the text Of unique circuits with complex interrelation of circuit parts.

20.1.2.2 Identical circuits. - If circuits on the same diagram are identical, the phrase "idential to" may be used rather than repetition of the text description. Similar circuits are discussed by using the phrase “similar to” or “identical to” and noting the exceptions.

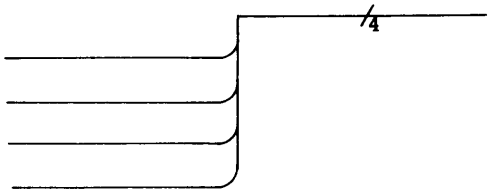
20.2 Master block diagram. -

20.2.1 Purpose. - One master block diagram shall be provided to disclose the overall function of the prime equipment. The purpose of this diagram is to describe the relative operation of each major functional division in order to comprehend the total operation of the equipment and provide access to lower levels of design information.

20.2.2 Layout techniques. - The master block diagram consists of major functional divisions enclosed by light solid lines. These lines are functionally connected by signal path lines, each identified with a descriptive name. Each major block on the diagram represents a major functional division and is identified by a descriptive name and an identifier code. If a functional division is complex, additional blocks may be added within the major block to represent further subdivision.

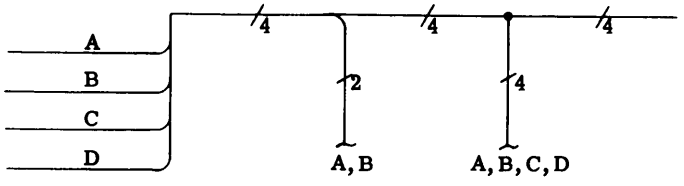
20.2.2.1 Power distribution. - If the equipment is simple enough to be disclosed in sufficient detail on the master block diagram, then the power distribution diagram may be included at the bottom. What is to be contained in the power distribution diagram is specified in 20.6.

20.2.2.2 Interconnection. - Signal lines that contain closely related information may be grouped into one signal line. However, care must be exercised in not grouping signal lines indiscriminately. Signal lines are grouped as follows:



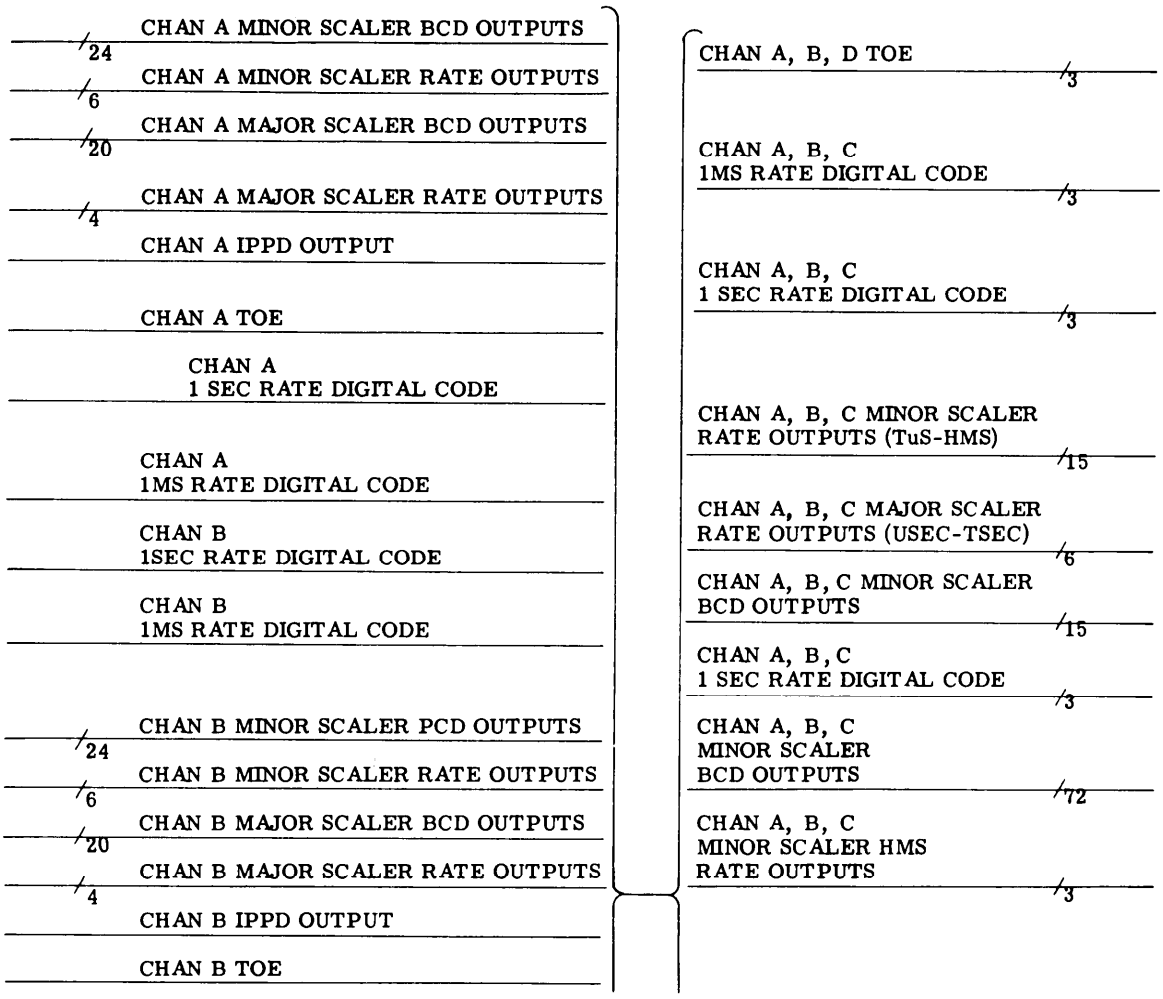
The number of signals being grouped is indicated by means of a slash through the grouped line and a number as shown above. Distribution of the grouped signals is shown by means of a curved breakoff line or a straight line breakoff.

Example:



In the above example, the first distribution uses the curved breakoff indicating only a portion of the grouped signals are being used. The second distribution uses a straight line breakoff indicating all of the grouped signals are used.

To avoid over-crossing of signal lines, a discontinuous interface may be created. All lines approach and leave this interface in a horizontal parallel manner as shown below.



Each signal line is identified with its name and number on each side of the interface to enable one to trace it across this interface.

20.3 Intermediate block diagram. -

20.3.1 Purpose. - When the functional divisions as defined on the master block diagram are sufficiently large, subfunctionalization is sometimes necessary. The intermediate block diagram provides the transition between a major functional division on the master block diagram and the many detailed block diagrams which may be required to describe the functional division.

20.3.2 Layout techniques.- The intermediate block diagram is generated by dividing the functional divison into discrete subfunctions. These subfunctions are interconnected in the same manner as on the master block diagram with complete signal nomenclature and characteristics.

20.4 Detailed block diagrams. -

20.4.1 Purpose. - The purpose of the detailed block diagrams is to depict a major functional division, showing the interrelationships of the functional entities or modules.

20.4.2 Layout techniques. - A detailed block diagram is prepared for each major function defined on the master block diagram. Each detailed block diagram is developed in a manner which makes the performance of the function obvious. In order to achieve this, care must be exercised to ensure the complete disclosure of the function on a single page. If this is not possible, the function is subdivided in such a manner that the first page of a multi-sheet detailed block diagram depicts the overall function, and each additional sheet shows the detail of each of the subfunctions. Each subfunction is shown on the first page as a box with a descriptive name and a function identifier code or hardware nomenclature. All inputs and outputs of each of the subfunctions are shown on both the first page and on the detailed diagram of the subfunction. By using this technique the entire function can be shown on a single page with secondary detail on succeeding pages. For smaller systems or equipments, a detailed block diagram page may cover more than one function and possibly the entire system or equipment.

20.4.2.1 Functionalization within a digital function. - In digital portions of equipments, each major block on the detailed block diagram shall contain the familiar logic diagram. Each of the logic operations being performed is represented by discrete logic symbols. These logic symbols need not be grouped or delineated into discrete functional entities. In general, coded signal lines are not used on logic block diagrams. However, if a coded signal flow line will enhance understanding, it should be used. All signal lines having significance shall be labelled with a descriptive name and logic term.

20.4.2.2 Interconnections. - All functional interconnections between hardware units are shown. All plugs, jacks, and cable numbers which provide the interconnection information between the units, assemblies, etc. are shown. Point-to-point wiring between circuit parts within an assembly need not be shown, but all interconnections between assemblies shall be accounted for. For larger equipments, one detailed block diagram is prepared for each function. The interconnection between these functions shall be shown. To accomplish this, all signals entering or leaving the function associated with a particular detailed block diagram shall be interconnected with functions associated with other detailed block diagrams. All hardware and cabling information between functions shall be shown. When tie-in is to another system or equipment, the signal specification and other pertinent interface considerations shall be included.

20.5 Blocked schematic. -

20.5.1 Purpose. - Blocked schematics represent the most detailed level of design disclosure, presenting all circuit information including component values, all test points, and sensors.

20.5.2 Layout techniques. - One blocked schematic is prepared for each block on the detailed block diagrams. On small equipment, a single blocked schematic may supply sufficient information, eliminating the need for higher level drawings.

20.5.2.1 Power circuits. - Power and power filtering circuits are separated from functional circuits. They are drawn at the bottom of the blocked schematic. B+, grounds, and return lines are now shown connected to the functional circuit by solid lines, but the connection is implied through the use of symbols for supplied power. The connection between a power line from the power circuit to a destination in a functional circuit is made by the break line technique. For piece-part assemblies, the power line is terminated outside the power entity, picked up outside the functional entity to which it is being supplied, and continued to the proper point within the functional entity (see figure 9). For modular assemblies, the power circuits are drawn the same as for piece-part assemblies, but with the functional entity boundaries removed (see figure 8). To facilitate making the connection between break symbols, these symbols shall be aligned vertically and the voltage indicated at the break symbols.

20.5.2.2 Part arrangement. - Circuit parts are arranged so that the circuit appears in its most understandable form, as commonly seen in standard textbooks. A great deal of emphasis should be placed on arranging the circuit parts to enhance functional understanding. Common ground or return points and common power points should not be tied together merely to conserve symbols.

20.5.2.3 Part data. - As much of the following circuit part data as is available is recorded for each part:

(a) Resistors - reference designator, value, wattage, and tolerance.
(b) Capacitors - reference designators, value, voltage, and tolerance.

(c) Coils, motors, and other wire wound devices- reference designators, value, tolerance, and resistance when applicable.
(d) Vacuum tubes, transistors, diodes etc. - reference designator and type designation.

(e) Transformers, matching devices, delay lines or other circuit devices - reference designator,

20.6 Power distribution diagrams. -

20.6.1 Purpose. - The power distribution diagrams shall disclose the complete generation and distribution of power.

20.6.2 Layout techniques. - The number of power distribution diagrams depends on the prime equipment complexity and configuration. Generally, there shall be one diagram for each cabinet, and one diagram showing distribution between cabinets. If there is a prime power cabinet, the generation and distribution within the cabinet should be shown along with the interlocking arrangements and distribution to other cabinets. Depending upon the packaging scheme, the power distribution diagram can be completely blocked schematic in form or partially blocked schematic and partially block diagram. Power supplies and regulators packaged as nomenclature items, and which have separate blocked schematics, are shown in block diagram form. All cable numbers, plug, pin and jack numbers shall be provided. Figure 6 is an example of a power distribution diagram disclosed on one sheet. This example is shown completely in blocked schematic form due to the simplicity of the equipment it represents.

20.6.2.1 Grounding techniques. - The grounding of an equipment is usually as complex as power distribution and, as such, requires equal attention. Since a power distribution diagram is a schematic diagram rather than a wiring diagram, it does not show the routing of wires, but it must show the continuities that exist. Generally, there are four types of grounds that exist in an equipment: (1) circuit common, (2) chassis ground, (3) A-C neutral, and (4) D-C return. Each of these is given a symbol shown on figure 10.

30. DESIGN OUTLINES

30.1 General considerations.-

30.1.1 Layout. - The design outline (figure 12) is a logical model which portrays complex dependency chains in a clear and concise manner. By the use of a few special symbols, the interrelationships are displayed which symbolize the dependency structure of the prime equipment. Design outlines can be prepared to show detailed design or to summarize the overall design of the prime equipment. Generally, a master design outline is prepared to show the overall dependency structure of the functions of the prime equipment, and detailed design outlines to show the dependency structure of the lower level functional entities and modules. It is not expected that design outlines be prepared to indicate circuit piece-part relationships. All design outlines are constructed in a chart form consisting of four areas: (1) headings, (2) specifications and data, (3) operation column, and (4) body (dependency structure). The headings (located at the top of the chart) precisely identify each functional entity/module and its input and output events. The specifications (normally located to the right of the chart) precisely describe the events depicted in the chart body. Data rows (located directly below the headings) provide basic reliability information associated with unmonitored functional entities/modules and a reference to performance data associated with the events. These rows may also include cost, spares data, maintainability data, and other pertinent information. The operation column (located at the left of the chart) identifies all man-machine actions (turn-on, check-out, operations, etc.) required to effect functional utilization of the prime equipment. The body of a design outline symbolically depicts the interrelationships among functional entities/modules, and their associated input and output events.

30.1.1.1 Headings. - The headings list all functional entities/modules and events necessary to completely describe the dependency structure of the design outline. Functional entity entries are identified by means of their identifier codes. Module entries are identified by means of their reference designators. The physical measurement points of all events are identified except during early design phases in which only the signal name is used due to lack of hardware information. In later phases, critical events are identified by listing first their signal names followed by, in parentheses, their test point number. Specifications or descriptions for the event are referenced by a number located in the box created by the intersection of the signal specification row and column headings. When adjacent columns refer to the same event, the event entry can be so placed that it applies to more than one column. The hardware identification of each heading entry is specified at the top of each column. Assigned reference designations are to be used for prime equipment identification. When adjacent columns refer to items in the same assembly, the location identifier can be placed so that it applies to more than one column.

30.1.1.2 Specifications and data. - The specification area of a design outline contains: (1) event specifications or descriptions, and (2) general notes. Each event occurring throughout the body of a design outline is

assigned a unique specification number. This number appears directly below the event entry in the heading. The same specification number also appears in the specification area. Here, the event is precisely specified by use of waveforms, timing diagrams, or other descriptive methods. In this manner complete performance characteristics associated with each event are identified. In addition, reliability information may be provided by means of data rows at the top of the design outline. Additional information can be presented simply by adding more data rows.

30.1.1.2.1 Specification number assignment. - During early design phases when both intermediate and master design outlines are required, specification numbers are assigned sequentially at the intermediate design outline level. The specification numbers are then assigned to the corresponding events on the master design outline. During the later phases when detailed design outlines are introduced, each detailed design outline is assigned a number. Specification numbers are then assigned, in numerical sequence, to each event on the design outline and are prefaced with the assigned number. For example, detailed design outline 1 specification number assignments are 1-1, 1-2, 1-3, etc., detailed design outline 2 assignments are 2-1, 2-2, etc. Distribution events recentered on other detailed design outlines carry the originating specification number.

30.1.1.3 Operation column. - The operation column identifies all actions required to disclose the complete dependency structure at any desired level of coverage. The dependency structure within the body of the design outline is developed according to the procedures specified in the operation column. For purposes of identification the procedures are divided into two basic categories: modal and test. Since the modal procedures are of primary concern these are presented first with the test procedures indented within the modal procedures. The dependency structure associated with each mode and test is identified by means of heavy horizontal lines. The modal procedures are numbered sequentially and the test procedures are assigned capital letters (A, B, C, etc.) sequentially within each modal procedure. The general procedure for the development of the procedure column is as follows:

(a) Determine what the different prime equipment modes are and what switch selections are necessary to obtain them.
(b) Present power turn-on as the first modal procedure. The dependency structure developed in the design outline body will reflect application of power, activation of power supplies and power distribution. Remember to include any test procedures as indented steps.
(c) Next, select the primary mode of operation and develop the complete dependency structure for this mode. Include all steps necessary to exercise all controls relative to this mode either as secondary modal steps or indented test.
(d) Select remaining modes in a logical dependency order and develop dependency structure as specified in 30.1.1.3 (c).

Early in the life cycle, the operation column would consist primarily of mode identification. Later, as more detailed information is known, the operation column would take on more detail. In addition to mode identification, it would include other actions required to develop the dependency structure such as turn-on, check-out, and other unique procedures. In order to maintain continuity between the procedural steps on the master design outline and the many detailed design outlines, the modal and test procedure number assignments made on the master design outline are maintained on the detailed design outlines. This means that the modal step numbers for a given detailed design outline may not be sequential but will reflect the modes in which the depicted function is involved.

30.1.1.4 Body. - The body of a design outline consists of a series of horizontal dependency lines. Each dependency line consists of basic symbols used to relate a functional entity/module or group of functional entities/modules to their associated inputs and outputs. The organization of the dependency lines in the chart body portrays the energy flow through the functional entities/modules depicted on the chart.

30.1.1.4.1 Basic symbols. - The body of a design outline is the mapping of a block diagram configuration. The mapping structure consists of basic symbols used to relate a functional entity/module or a group of functional entities/modules to their associated input and output events. The three basic symbols used in mapping are defined as follows:

Event box:	▭	to represent an action or availability of one or more events resulting from the proper operation of the functional entities/modules associated with the event
Functional entity/module dot:	●	to represent a functional entity/module or a group of functional entities/modules.
Dependency marker:	▲	*to* indicate dependency upon another event.

Three basic types of event boxes are used in mapping. These are: (1) the single event box to represent one unique event, (2) the composite event box which consists of two or more single event boxes to represent multiple events and (3) the contracted event box which consists of a single event box to represent multiple events. Each of these event box types is discussed in more detail in the following paragraphs. Nomenclature in the event box specifies the type of action or availability of the event. Figure 13 lists the various nomenclatures that can appear in the box and their meaning. To assist in determining the accessibility of the events indicated on the design outlines, three distinguishable kinds of backgrounds are used within the event boxes. These backgrounds and their use are:

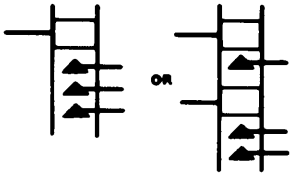
Background		When used
BLACK (with white lettering)	A	Events which may be recognized from outside the equipment. Examples are: ATE monitored front panel lamps, front panel meters, motor running, etc. Notice that this recognition includes events other than those which may be observed by sight.
GRAY (with black lettering)		Events which may be determined or observed only after the equipment enclosure has been opened, and occur at points which are readily accessible.
WHITE	A	Events at points which are difficult to gain access to.

There are several variations of the functional entity/module dot. One such variation is the partial dot (◐) which indicates that the functional entity/module which it represents is only partially involved in producing the corresponding event. Other variations of the functional entity/module dot are described on figure 13. There are also several variations of the dependency marker which are used to describe the relationship between a group of events and an ensuing dependent event. These variations and their use are described in later paragraph

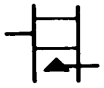
30.1.1.4.2 Basic dependency structure. - A dependency line consists of dependency marker, functional entity/module dots and event boxes connected as follows:

A dependency structure consists of a series of dependency lines. Each dependency line is constructed using the three basic symbols. The simplest dependency line would appear as follows:

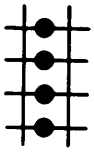
By itself this dependency line has very little meaning except to indicate that the event (▲) is dependent upon the proper operation of the functional entity/module (•) and the availability of some previous event (•). In order to provide meaning to this dependency line the symbols are ordered into one of two types of columns: the event/dependency column and the functional entity/module column. The event/dependency column consists of event boxes and dependent y markers depicted as follows:



The simplest event/dependency column would appear as follows:



The functional entity/module column consists of only functional entities/modules even though these entities/ modules may be depicted more than once. It is indicated as follows:



The simplest form of a functional entity/module column would appear as follows

30.1.2 Mapping rules and techniques. - Experience indicates that the following rules and techniques govern substantially all the basic mapping situations to be encountered. If situations arise which are not covered in the following paragraphs, the contractor should carefully augment the mapping schemes and record such for future use.

30.1.2.1 Simple dependency line (rule 1). - The mapping of a functional entity/module with one input and a single output results in a simple dependency line as follows:

The mapping shows that the output event at ② is dependent upon functional entity/module Z and the input event at ①

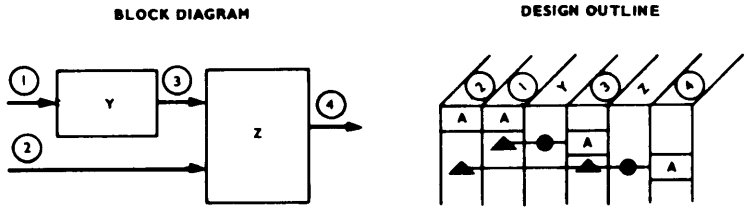
30.1.2.2 Multiple input dependency line (rule 2). - A functional entity/module with more than one input and a single output is mapped as a multiple input dependency line as follows:

The mapping shows that the output event at ③ is dependent upon functional entity/module Z and the input events at ① and ②

30.1.2.3 Multiple output dependency line (rule 3).- A functional entity/module having one input and multiple output is mapped as a multiple output dependency line as follows:

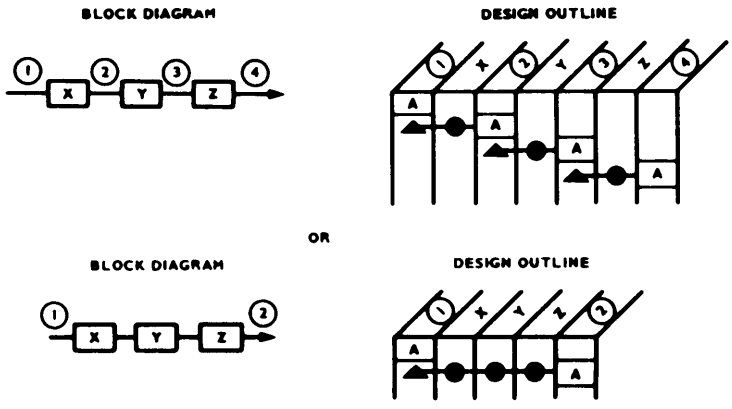
The mapping shows that both outputs at ② and③ are dependent upon functional entity/module Z and the input event at ① .

30.1.2.4 Dependency chain. - A dependency chain consists of a series of interrelated dependency lines. The following example shows a dependency chain consisting of two dependent y lines:

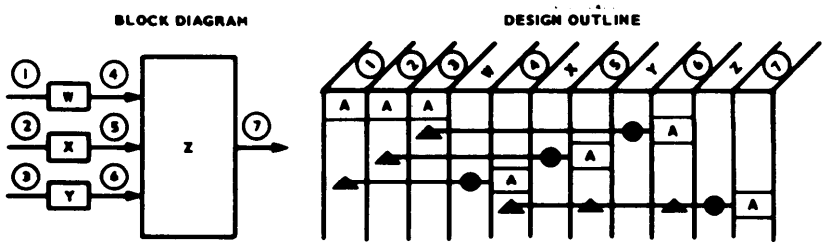


The last dependency line in this examle shows that the output event at ④ is dependent upon functional entity/ module Z and the event ③ and ②

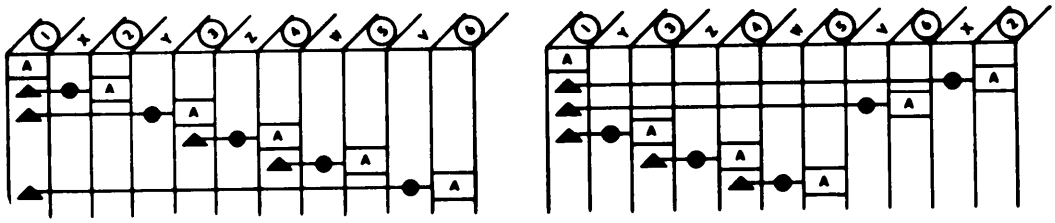
30.1.2.4.1 Serial relationships. - As a rule serial relationships are shown as follows:



30.1.2.4.2 Parallel relationships. - As a rule parallel relationships are shown as follows:

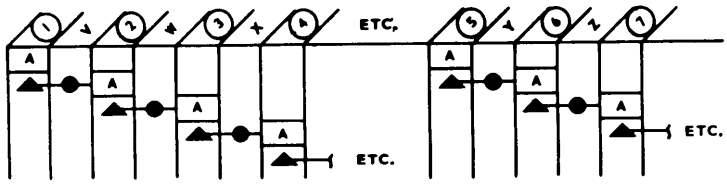


30.1.2.4.3 Serial parallel relationships. - The following example illustrates the preferred manner in mapping serial parallel relationships:



The undesirable presentation erroneously infers by its structural layout that there is one serial dependency chain. The desirable presentation shows clearly by its structural layout that there are three separate parallel dependency chains. It also shows that one of the dependency chains has several serial relationships.

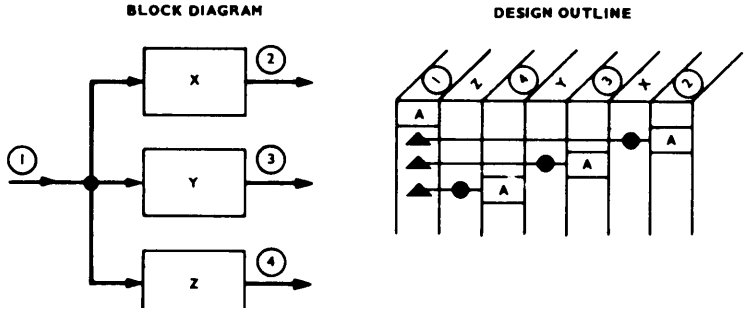
30.1.2.4.4 Horizontal line usage. - Normally, only one dependency line is used per horizontal segment of the chart. However, if height is a problem on a design outline, more than one dependency line may be used if care is exercised. The dependency chains should be separated by ample space to avoid confusion. An example of this technique is as follows:



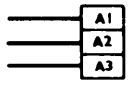
Notice that each dependency chain is easily identifiable.

30.1 .2.4.5 Parallel divergent branches (rule 4). - When a path diverges into a number of path, it is depicted by an event/dependency column using a single event and the appropriate number of dependency marker. This situation is shown as follows:

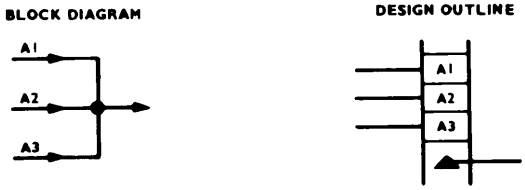
The following example utilizes this rule:



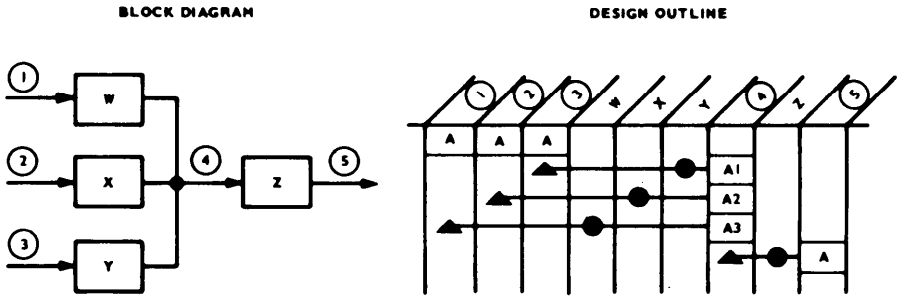
30.1.2.5 Composite event. - A composite event represents an event which is made up of a number of single events. The constituent events may or may not be measured individually. A composite event is constructed in an event/dependency column as follows:



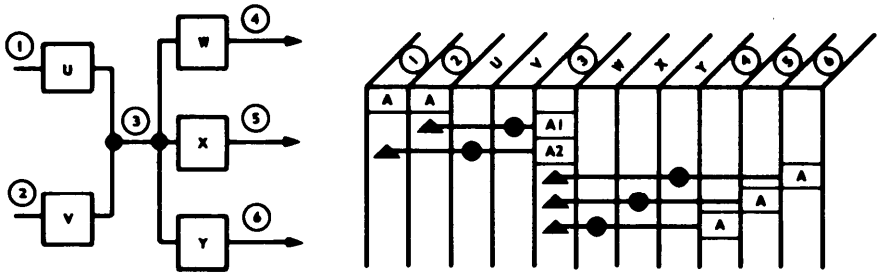
30.1.2.5.1 Parallel convergent branches (rule 5). - When paths converge into a single path, they are depicted by an event/dependency column using a composite event and a single dependency marker. This situation is shown thusly:



The following example illustrates this rule:

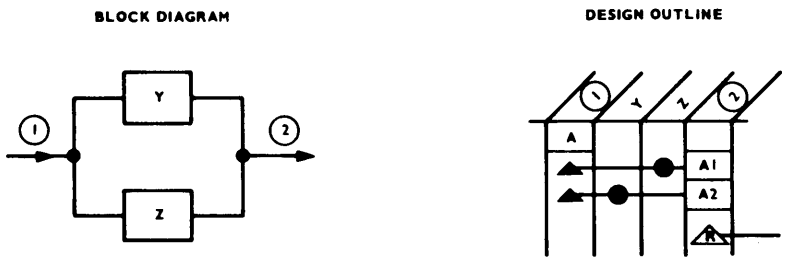


30.1 .2.5.2 Convergent divergent branches. - The following example illustrates a situation in which both divergent and convergent branches exist.



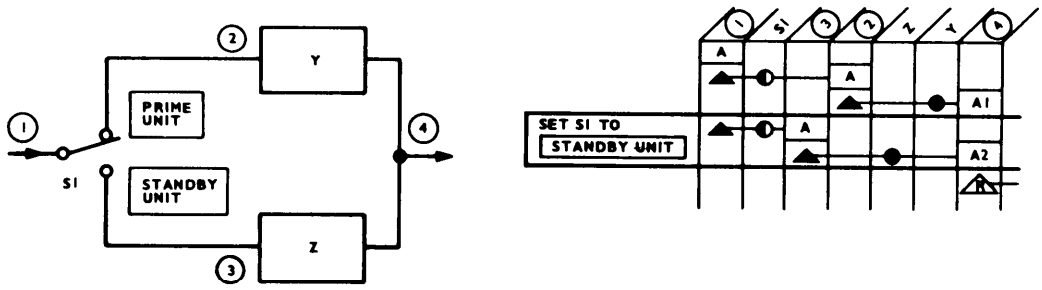
30.1.2.5.3 Redundant - Redundancy is mapped using the composite event and a special dependency marker. The following examples illustrate the mapping of various types of redundancy:

30.1.2.5.3.1 Active redundancy. - Active redundancy is mapped as follows:



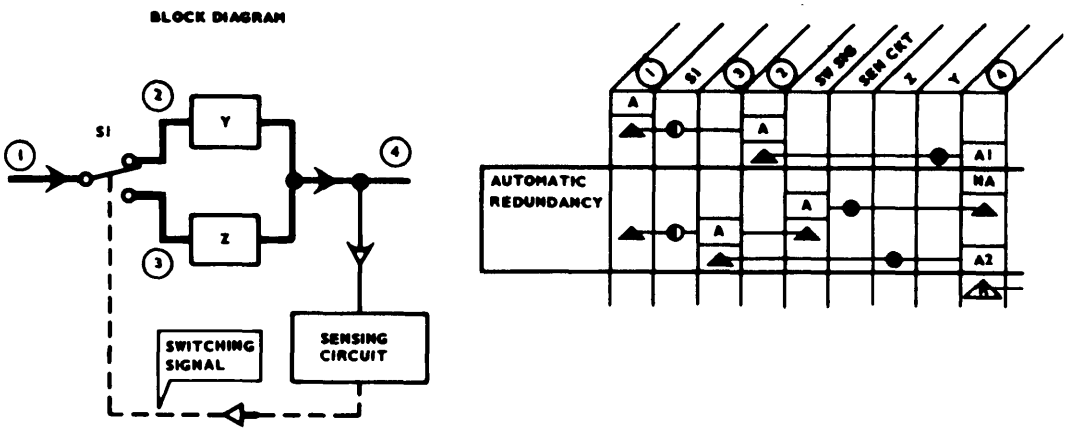
The design outline shows that if the signal at@ is available and either functional entity/module Y or Z is operating the signal at@ will be available. The notation R within the dependency marker denotes a redundant event.

30.1.2.5.3.2 Manually switched redundancy. - Manually switched redundancy is mapped as follows:



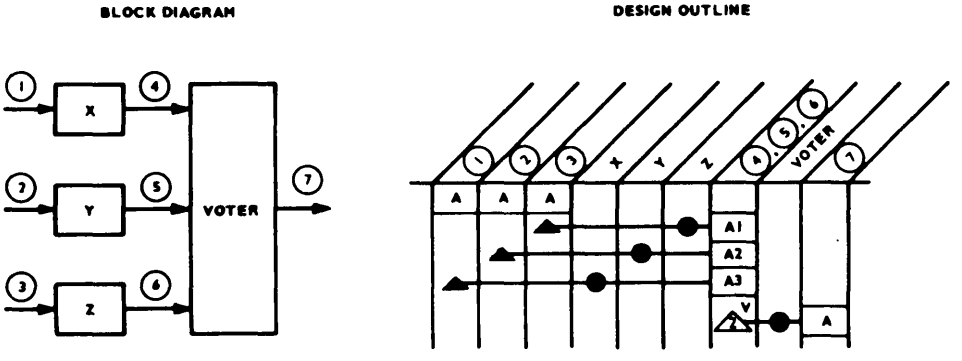
This situation is mapped in the same manner as the active redundancy situation except that the manual operation is specified in the procedure column and outlined with a heavy line along with the associated dependency line.

30.1.2.5.3.3 Automatically switched redundancy. - Automatically switched redundancy is mapped as follows:



The design outline first maps the primary dependency structure. The automatic switching is emphasized by the heavy lines and the notation within the procedure column. The redundant signal is initiated by the use of a signal not available event box (NA) at ④ which generates a switching signal to activate the redundant path,

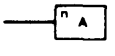
30.1.2.5.4 Voting. - The following example illustrates the mapping of a typical voting situation:



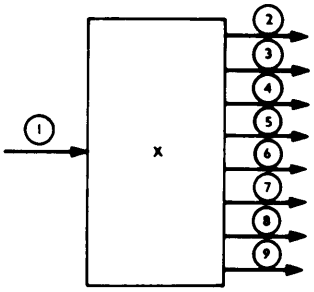
This example illustrates a 2/3 voter. Parallel events at ④, ⑤ and ⑥ are shown as a composite event. The dependency marker under the composite event has special notation as follows: The V denotes that the events are being voted. The 2 within the dependency marker indicates that any two of the three events represented by the composite event are required for the event at ⑦ to occur.

30.1.2.6 Contractions. - In the event space on the design outline becomes limited, several schemes have been devised to allow contractions of events and fuctional entities/modules. The following paragraphs describe the techniques for contractions. It is important to note here that contractions should be used only when absolutely necessary since they tend to obscure the dependency structure details.

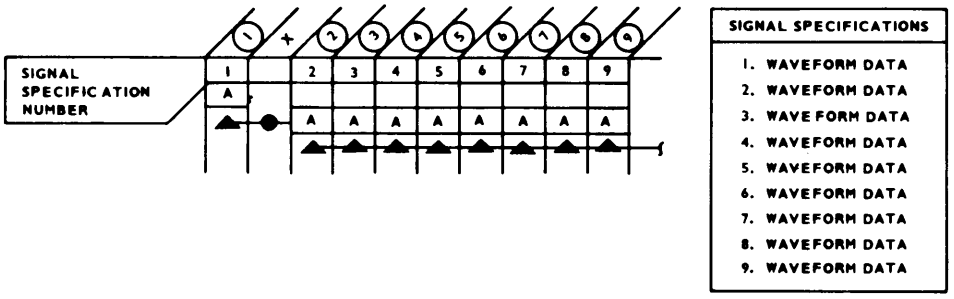
30.1.2.6.1 Contracted event (rule 6).- A contracted event is constructed in an event/dependency column as follows:



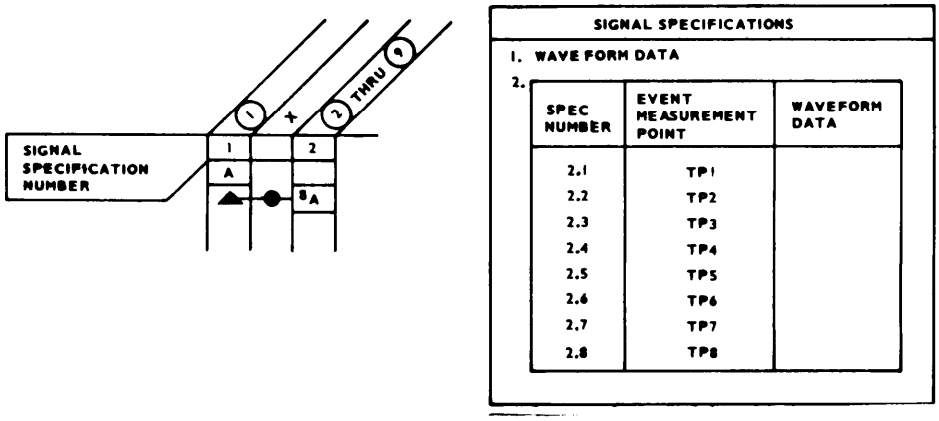
The n in the upper left hand corner of the contracted event indicates the number of events it represents. The following is an example of contracted events. Consider a functional entity/module X with one input and eight outputs. If all eight outputs are required as a unit by many different functional entities/modules on the design outline, it is desirable to contract these outputs into one event entry. The block diagram of functional entity/module X would appear as follows:



The design outline (not contracted) would appear as follows:

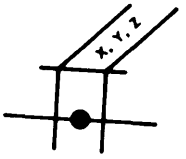


The design outline (contracted) would appear as follows:

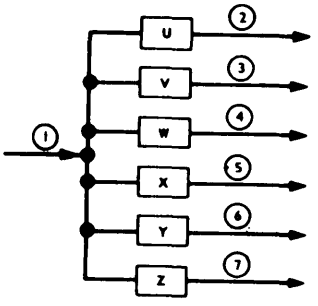


In this example, the eight output events of functional entity/module X are contracted into a single event. The small 8 in the upper left corner of the event box denotes the number of contracted events. Each of the contracted events is assigned a unique specification number as indicated in the signal specification area in the example above. The physical locations of the event measurement points are identified either in the heading or the event measure point column in the signal specifications area. Waveform data is provided for each of the events in the waveform data column in the signal specifications area.

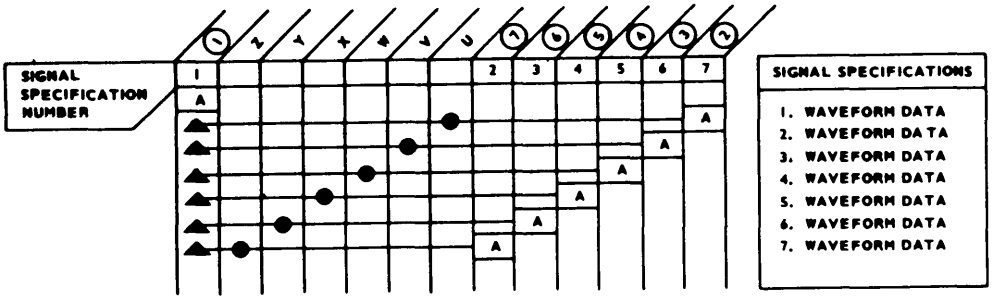
30.1 .2.6.2 Contracted functional entity/module (rule 7). - A contracted functional entity/module represents a number of single functional entities/modules and is constructed as follows:



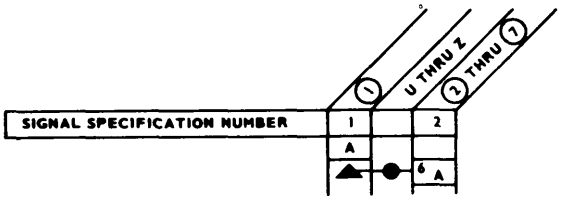
A contracted functional entity/module is identified by noting that more than one functional entity/module is listed in the heading corresponding to the column of which it is a part. The following is an example of contracted functional entities/modules. Consider the case in which a signal is distributed to six separate functional entities/modules. The block diagram would appear as follows:



The design outline (not contracted) would appear as follows:



The design outline (contracted) would appear as follows:



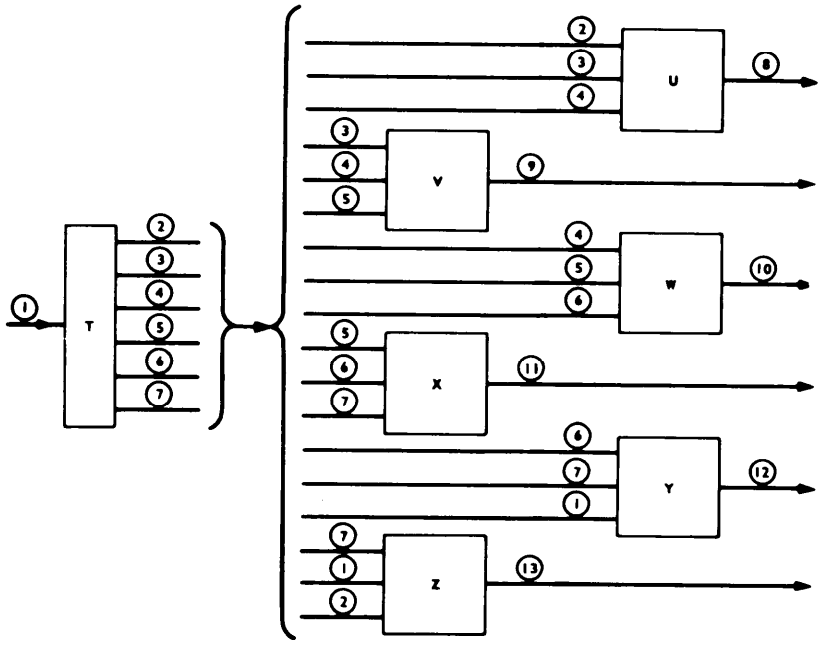
SIGNAL SPECIFICATIONS

1. WAVEFORM DATA
2.

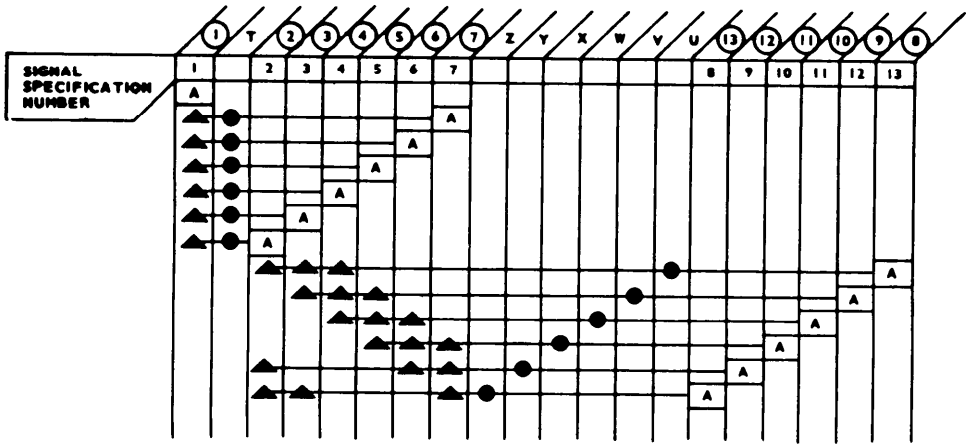
SPEC NUMBER	EVENT MEASUREMENT POINT	WAVEFORM DATA	ASSOCIATED FUNCTIONAL ENTITY / MODULE
2.1	②		U
2.2	③		V
2.3	④		W
2.4	⑤		X
2.5	⑥		Y
2.6	⑦		Z

In this example, the six output events have been contracted into one event entry. In addition, the six functional entities/modules associated with these events have been contracted into one entry. The specification number, measurement point, and waveform data of each contracted event are described in the signal specifications area in the same manner as in the event contractions example. The functional entity/module associated with each event is identified by an additional column in the signal specifications area as shown above.

30.1 .2.6.3 Contracted dependency chains. - The following example illustrates the mapping of a complex configuration resulting in a contracted dependency chain. Consider the case represented, by the following block diagram:

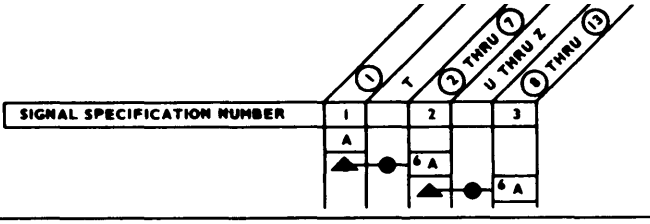


contracted) would appear as follows:



SIGNAL SPECIFICATIONS
1. WAVEFORM DATA
2. WAVEFORM DATA
3. WAVEFORM DATA
4. WAVEFORM DATA
5. WAVEFORM DATA
6. WAVEFORM DATA
7. WAVEFORM DATA
8. WAVEFORM DATA
9. WAVEFORM DATA
10. WAVEFORM DATA
11. WAVEFORM DATA
12. WAVEFORM DATA
13. WAVEFORM DATA

The following design outline (contracted) represents a contracted dependency chain:



SIGNAL SPECIFICATIONS

1. WAVEFORM DATA

2.

SPEC NUMBER	EVENT MEASUREMENT POINT	WAVEFORM DATA	SPEC NUMBER	EVENT MEASUREMENT POINT	WAVEFORM DATA
2.1	(2)		2.4	(5)	
2.2	(3)		2.5	(6)	
2.3	(4)		2.6	(7)	

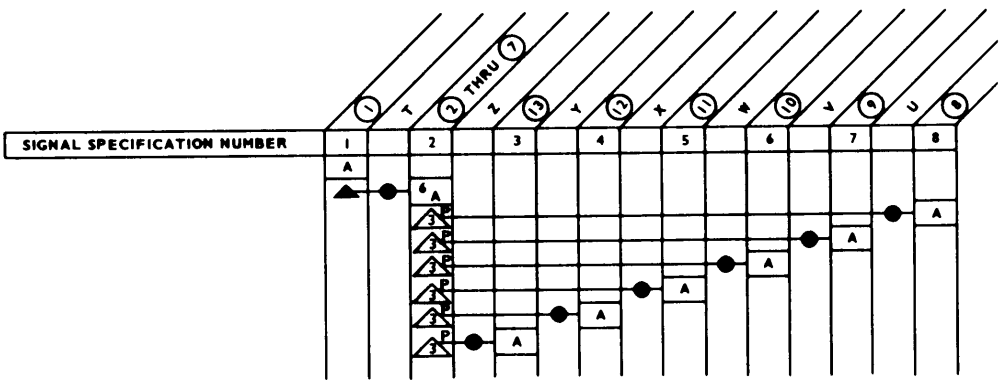
3.

SPEC NUMBER	EVENT MEASUREMENT POINT	WAVEFORM DATA	ASSOCIATED FUNCTIONAL ENTITY / MODULE	REQUIRED INPUT EVENTS
3.1	(8)		U	2.1, 2.2, 2.3
3.2	(9)		V	2.2, 2.3, 2.4
3.3	(10)		W	2.3, 2.4, 2.5
3.4	(11)		X	2.4, 2.5, 2.6
3.5	(12)		Y	2.5, 2.6, 2.1
3.6	(13)		Z	2.6, 2.1, 2.2

In this example, the six output events and their associated functional entities/modules have been contracted. In addition, the six outputs of functional entity/module T have been contracted. The specification number, measurement point, and waveform data associated with the event outputs of functional entity/module T are described in the same manner as in 30.1.2.6.2. The specification number, measurement point, waveform data, and functional entity associated with each of the output events at (8) through (13) are described in the same manner as in 30.1.2.6.2. In addition, the input events associated with each of the output events are tabularized as shown.

30.1.2.6.4 Event/dependency interface for contracted events. - In the situation where several events are mapped from a contracted event, a dependency marker with special notation is used. Two types of special notations are used. The first type relates to particular combinations of events from a contracted event and is shown as follows:

The use of the m and p with the dependency marker indicates that m particular events out of the n contracted events are required to produce the ensuing event. The following example illustrates the use of this type of event/dependency interface. Consider the block diagram of paragraph 30.1 .2.6.3 in which only the inputs of functional entity/module _ are contracted. Assume it is desirable from a disclosure viewpoint to not contract the outputs at (8) through (13); and their associated functional entities/modules. The design outline would appear as follows:



SIGNAL SPECIFICATIONS

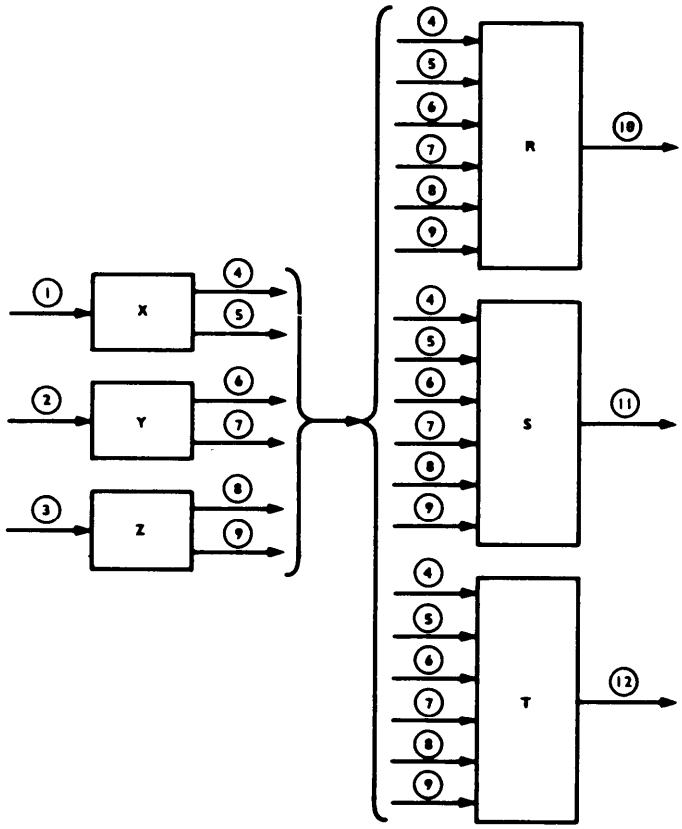
1. WAVEFORM DATA
2.

SPEC NUMBER	EVENT MEASUREMENT POINT	WAVEFORM DATA
2.1	(2)	
2.2	(3)	
2.3	(4)	
2.4	(5)	
2.5	(6)	
2.6	(7)	

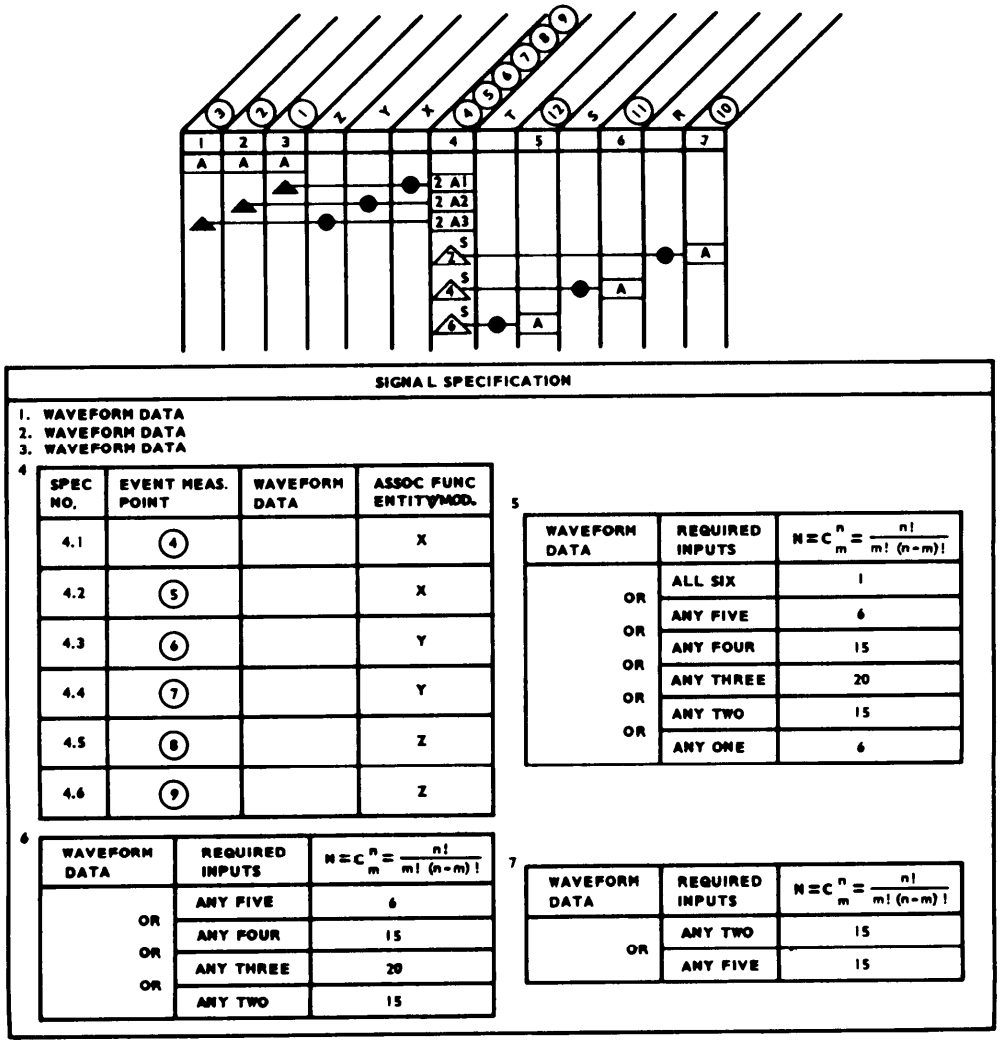
3. WAVEFORM DATA; REQUIRED INPUTS: 2.1, 2.2, 2.3
4. WAVEFORM DATA; REQUIRED INPUTS: 2.2, 2.3, 2.4
5. WAVEFORM DATA; REQUIRED INPUTS: 2.3, 2.4, 2.5
6. WAVEFORM DATA; REQUIRED INPUTS: 2.4, 2.5, 2.6
7. WAVEFORM DATA; REQUIRED INPUTS: 2.5, 2.6, 2.1
8. WAVEFORM DATA; REQUIRED INPUTS: 2.6, 2.1, 2.2

The event/dependency interface for the events at (8) through (13) indicates that three particular events of the contracted six events are required to produce the desired output events. The specifications for these events identify the required three events as shown. The second type of dependency marker notation relates to sets of combinations of events and is shown as follows:

The use of the m and s with the dependency marker indicates that m number of sets of events is requird to produce the ensuing event. A given set is defined as the number of combinations of n events taken m at a time. ($N = C_m^n$).. A different set of combinations is generated for each value of m($m < n$). The following example illustrates the use of the event/dependency interface for sets of combinations. Consider the case represented by the following block diagram:

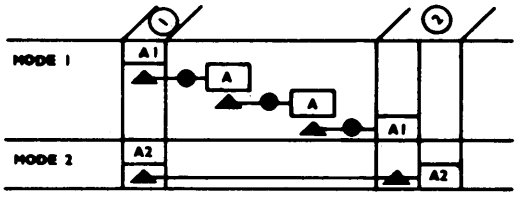


The following design out line represents the functional entities/modules and signal flow between X, Y, Z, and R, S, T.



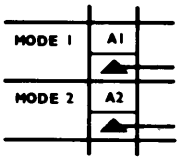
In this example the six signals from X, Y and Z are described by the composite event designated by signal specification number 4. Specification number 5 on the signal specification chart shows that the event at (12) is available when alternative sets of combinations occur. This means that in order for a signal to be available at measurement point 12 a combination of all six events must be available to T or any combination of five events must be available to? or any combination of four, etc. The column at the right indicates the total number of possible combinations for each set. Similarly, signal specification number 6 shows that the event at (11) is vailable when a combination of any five events are available to S and S is functioning properly, or any combination of four or three or two. The column at the right, as before, indicates the total number of possible combinations for any given set.

30.1.2.7 Event commonality.- When a complex dependency chain produces an end availability which proves a group of functional entitles modules good under one mode of operation, it may be proven good under another mode as follows:

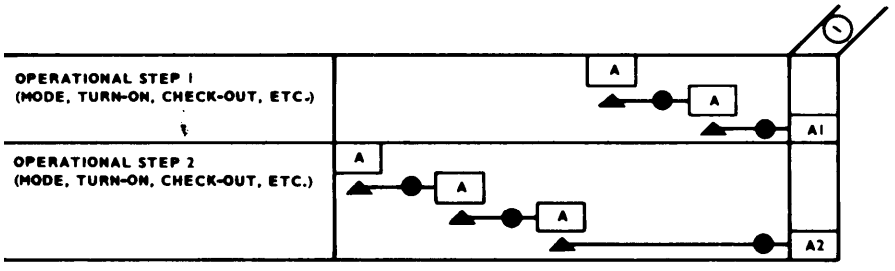


The two end availabilities above (furthest to the right) are measured at the same physical test point but charted in two adjascent columns containing the same signal specification number. The last line is interpreted thusly: If A2 at ① is now available, and if A1 at ② was available during mode 1, then A2 at ② is available for mode 2. This implies that all functional entities/modules required for mode 1 are also necessary for mode 2. This technique eliminates the need for redeveloping the entire dependency chain of mode 1 again for mode 2. A second case occurs when two events of different operational steps occur at the same measurement point but are a result of different dependency chains. The following two examples illustrate this situation:

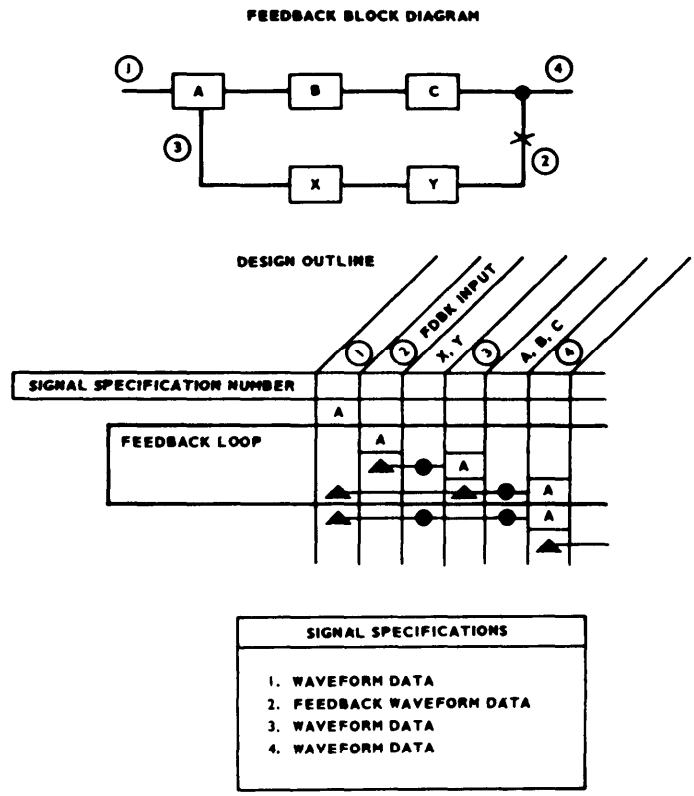
Example 1:



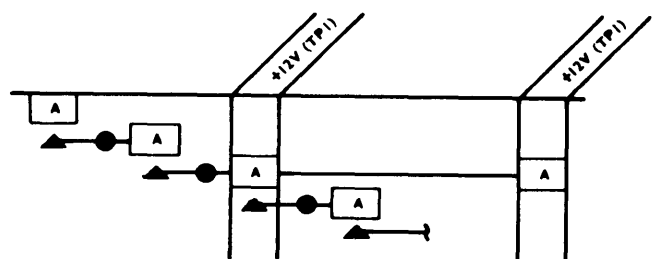
Example 2:



30.1.2.8 Feedback loops. - When the output of a circuit is sent back to appear as part of the input to the circuit, a feedback loop exists. To disclose the functional dependency of such a loop requires that the loop be broken. Under these conditions, the normal (main) input into the loop, plus a proper stimulus inserted at the break, will result in a known output. Breaking the loop allows functional dependency to appear as a simple serial dependency chain. Feedback loops are identified in the procedure column and enclosed in a manner similar to checkout steps (refer to example feedback block diagram and design outline below). The complete dependency structure of the broken loop is then shown within the enclosed area Directly below the enclosed area, the dependency structure of the loop is again shown but with the loop connected as normal. This structure appears as a horizontal line consisting of a dependency mark, a series of dots and an output. In words, the line shows that if the input to the loop is available and all functional entities/modules within the loop are good, then the output of the loop is available. Using this technique, the detailed dependency structure of a feedback loop can be disclosed while also showing how the loop as a whole fits into the general dependency scheme of the design outline when normally connected.



30.1.2.9 Re-entered event. - Occasionally, design outline presentation is enhanced when an event is re-entered. An event is recentered by simply extending the horizontal line, of which it is a part, to the desired point of re-entry and again recording the event. All information associated with the event (heading, signal specification number, etc.) must also be recentered in the appropriate column. An example of event re-entry is as follows:



In this example the +12V occurs in the middle of the design outline and is further involved in the dependency structure. Thus, it is entered where it is first developed in the dependency structure and then recentered for further use.

30.1.2.10 Energized relay events. - When relays are held energized by a path separate from that of the initial energizing path, a variation of a composite event box is used to represent the situation. The resulting dependency chain normally appears as follows:

The first line terminated by an "I" shows the path for initially energizing the relay. The second line terminated by an "H" identifies the holding path.

30.1.2.11 Time delays.- Protective time delays which occur after an operational step is initiated are illustrated by placing a ban of screen shading horizontally across the page immediately after the entry of the time delay device. Time is assumed to begin with the setting of the switch that initiates the step in which the time delay occurs. The length of time delay is indicated within the shaded band. When the time delay is not directly related to the step, special notations may be added within the time delay band - e.g. "2 seconds after motor exceeds 3000 r.p.m."

30.2 Master block diagram. -

30.2.1 Purpose. - One master design outline shall be provided for each system equipment to summarize the logical dependency structure of the entire prime equipment, disclose the relationship between functional entities/modules, and provide detailed specifications for all prime equipment inputs and outputs.

30.2.2 Layout techniques. - The master design outline provides, in symbolic form, the overall dependency structure of a prime equipment. Its content includes the dependency structure of all functional entities/modules as they are defined at this time. The master design outline is divided into four main areas: (1) headings, (2) specifications and data, (3) operation column, and (4) body.

30.2.2.1 Headings. - Column headings list the name and location of all events and functional entities/modules associated with the master design outline. Events include:

(a) Inputs from external equipment.
(b) Internal events.
(c) Output events (terminal events).

30.2.2.2 Specifications and data. - When the master design outline is first generated (detailed design outline not generated yet), all major events appear on the master design outline. However, when the design progresses to the point where the detailed design outline is generated, additional events appearing on the detailed design outline will have developed which do not appear on the master design outline. Since the master design outline is a summary of the detailed design outline, all events should be directly keyed between the two design outlines. To accomplish this, the specification number associated with each event on the detailed design outline must be used for that identical event on the master design outline. Because of the direct keying, the specification numbers on the master design outline may not be sequential from left to right, but will provide a direct reference to the appropriate detailed design outline. The data rows are entered just below the headings. The first row contains numbers which key events to signal specifications normally listed at the right of the diagram. These signal specifications provide precise performance data including timing and voltage data, waveform data, and human factors data where applicable. In the second row, failure rates of subfunctions which go unmonitored. Additional information can be presented simply by adding more data rows.

30.2.2.3 Operation column. - The operation column must identify all modes or operation. It may also display selected procedural actions if so desired. If the design has proceeded to the point where the detailed design outline has been generated, the selected turn-on and check- out step numbers of the master design outline must correspond to those of the detailed design outline.' Necessary actions by personnel to operate the system can be disclosed using work study techniques and keyed to the operation column.

30.2.2.4 Body. - The body of the design outline depicts the dependency structure of the prime equipment. The development of the dependency structure is determined by the procedural actions identified in the procedure column.

30.3 Intermediate design outline. -

30.3.1 Purpose. - Intermediate design outlines shall be provided to insure smooth and comprehensive transition between the many detailed design outline parts and the master design outline when a prime equipment is sufficiently large and complex to warrant these diagrams. The intermediate design outlines provide intermediate level dependency structure coverage linking the detailed design outline parts to the master design outline.

30.3.2 Layout techniques. - The construction of the intermediate design outline is approached in the same manner as the master design outline.

30.4 Detailed design outline. -

30.4.1 Purpose. - The detailed design outline is generated after the design process reaches the point at which most of the circuit details are known. It is an expansion of the master design outline (and intermediate design outlines as necessary) and is directly keyed to them. The detailed design outline discloses the dependency structure of a system-equipment in its most detailed form.

30.4.2 Layout techniques. - Each detailed design outline represents one or more complete functions. It displays the interrelationship among functional entities/modules found on detailed block diagrams and is directly keyed to them. Each detailed design outline is divided into four main areas: (1) headings, (2) specifications and data, (3) operation column, and (4) body.

30.4.2.1 Headings Column headings list the signal name of all critical events and hardware identification of all events. The name, functional code, and hardware identification of functional entities/modules associated with the detailed design outline are also listed. Events include such conditions as:

(a) Availability of signals or power inputs.
(b) Indications that may be observed.
(c) Conditions or states of the prime equipment - i.e., relay energizes, temperature normal, etc.

30.4.2.2 Specifications and data. - The function of these rows is the same as that described under master design outlines.

30.4.2.3 Operation column. - The operation column identifies all modes of operation. It also displays all operational actions which are necessary to provide complete logical design outlines. These actions consist of turn-on and check-out steps. These steps may take the form of making switch selections, providing external stimulus, or running diagnostic programs.

30.4.2.4 Body. - The construction of the body is the same as that described under master design outline.

40. LIST OF SYMBOIS

40.1 Symbols. - The contractor shall supply a list of all codes and symbols used in the disclosure formats.

REFERENCE DESIGNATOR	DESCRIPTION	MIL NOMENCLATURE WHERE APPLICABLE
1A	INTERROGATOR SET CASE	CY-3838/TPX-28
1A1	REAR PANEL	
2	MAIN CHASSIS	
2A1	DIRECTIONAL COUPLER	
2A2	SWR	
2A3	FILAMENT REGULATOR	
3	CODER-SYNCHRONIZER	KY-486/TPX-28
3A1	CLOCK AND SUPPRESSOR	
3A1A1	BOARD	
3A1A2	BOARD	
3A2	INTERROGATION CODER	
3A2A1	BOARD	
3A2A2	BOARD	
3A3	TRIGGER AMPLIFIER AND GTC MIXER	
3A4	TRIGGER COUNTDOWN	
3A5	PULSE COUNTER	
3A6	MODE GATE GENERATOR	
3A7	INTERCONNECTION ASSEMBLY	
4	RADAR TRANSMITTER	T-906/TPX-28
5	RADAR RECEIVER	R-1180/TPX-28
5A1	RF HEAD ASSEMBLY	
5A2	IF/VIDEO AMPLIFIER	
5A2A1	IF AMPLIFIER	
5A2A2	GTC GENERATOR	
5A2A3	VIDEO PROCESSOR	
6	GATING SIGNAL SELECTOR	SA-1021/TPX-28
6A1	BOARD	
6A2	BOARD	
7	POWER SUPPLY (RECTIFIER BOARD AND BRACKET ASSEMBLY)	PP-3656/TPX-28
7A1	12V REGULATOR BOARD	
7A2	25V REGULATOR BOARD	
8	POWER SUPPLY (CENTER BOARD AND BRACKET ASSEMBLY)	PP-3799/TPX-28

FIGURE 5- HARDWARE NOMENCLATURE AND REFERENCE DESIGNATORS, SAMPLE.

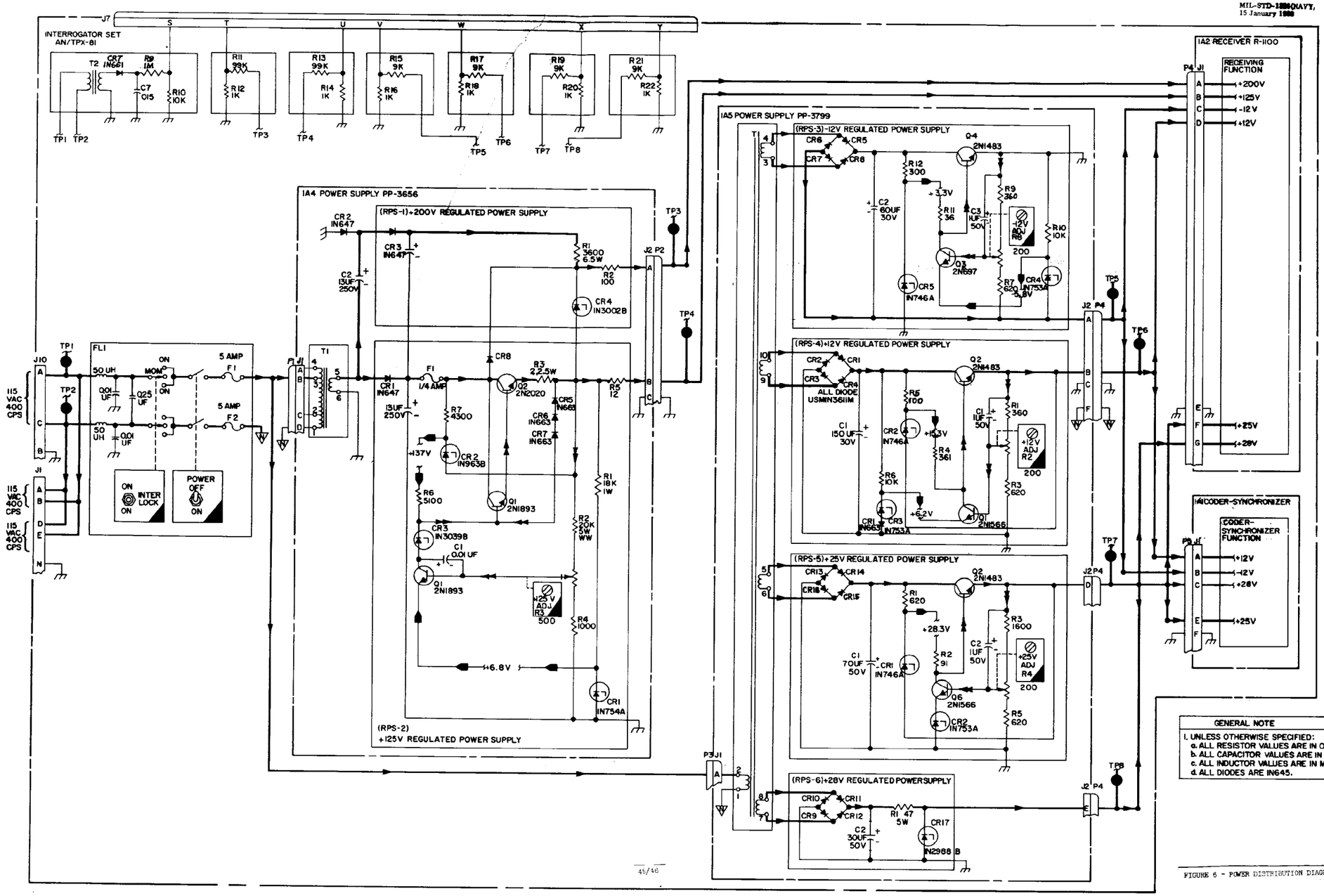
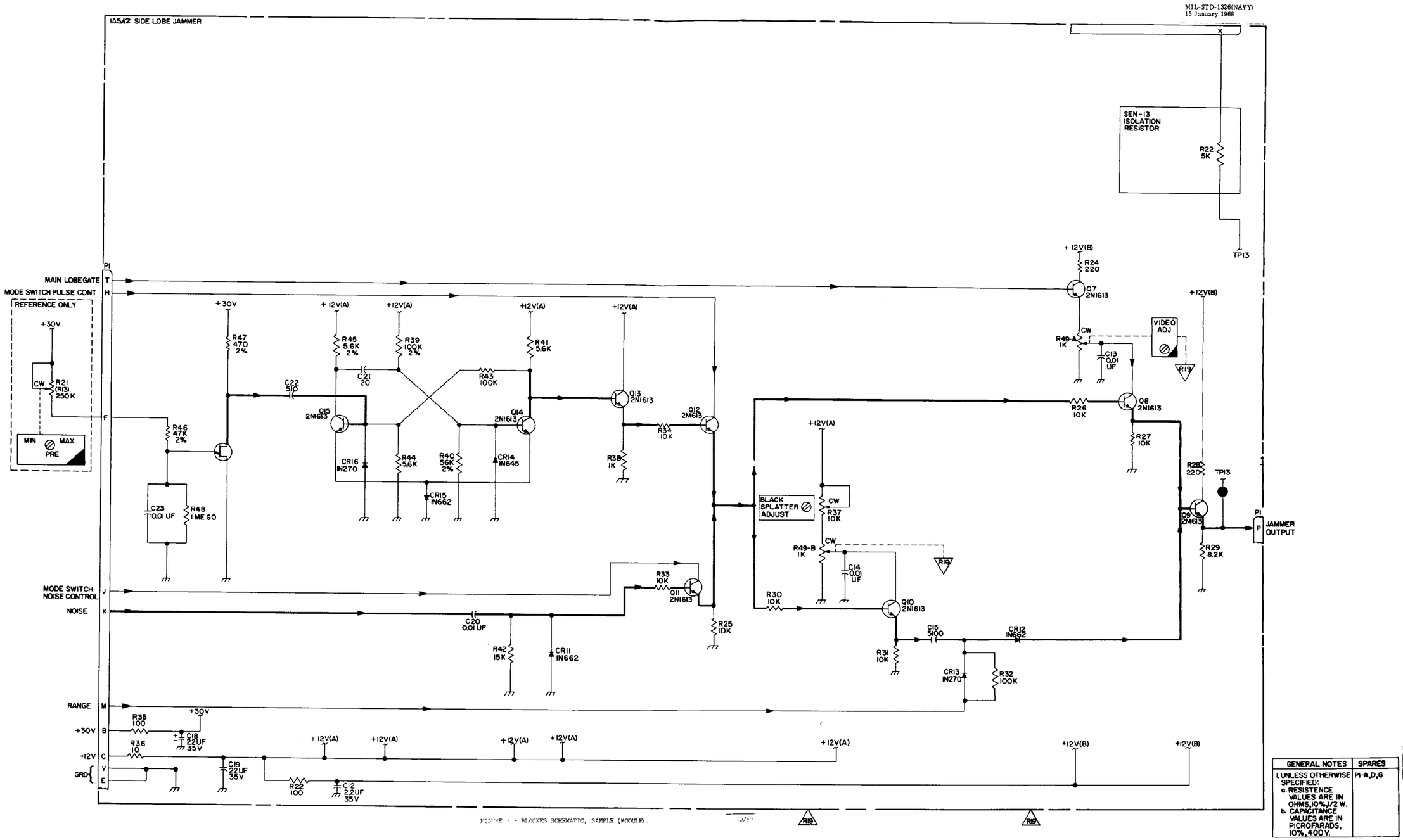


FIGURE 6 - POWER DISTRIBUTION DIAGRAM, SAMPLE

EXPLANATION OF IDENTIFIER CODES		
AMP-1	AMPLIFIER	Within each equipment numeric codes for each alpha code begin at 1. For example, if a given equipment has two amplifiers, one voltage divider, and two diode clamps, code assignments would be as follows: AMP-1 AMP-2 VD-1 CLP-1 CLP-2 If the numeric code agrees with the standard reference designator, it is only incidental.
BMV-1	BISTABLE MULTIVBRATOR	
BO-1	BLOCKING OSCILLATOR	
CA-1	CONTROL AMPLIFIER	
CR-1	CURRENT REGULATOR	
DRV-1	DRIVER	
DSW-1	DELAYED SWITCH	
EF-1	EMITTER FOLLOWER	
GA-1	GATING AMPLIFIER	
GAT-1	GATING CIRCUIT	
GDA-1	GATED DELAY AMPLIFIER	
INV-1	INVERTER	
MMV-1	MONOSTABLE MULTIVBRATOR	
MOD- 1	MODULATOR	
MV-1	MULTIVIBRATOR	
OR-1	“OR” GATE	
OSC-1	OSCILLATOR	
PG-1	PULSE GENERATOR	
SW-l	TRANSISTOR SWITCH	
TC-1	TEMPERATURE COMPENSATOR	
VR-1	VOLTAGE REGULATOR	

FIGURE 7-IDENTIFIER CODES, SAMPLE.

1A542 SIDE LOBE JAMMER



GENERAL NOTES	SPARES
1. UNLESS OTHERWISE SPECIFIED: a. RESISTENCE VALUES ARE IN OHMS, 10%, 1/2 W. b. CAPACITANCE VALUES ARE IN PICROFARADS, 10%, 400 V.	P1-A,D,G

FIGURE . - BLOCKER SCHEMATIC, SAMPLE (MODULE).

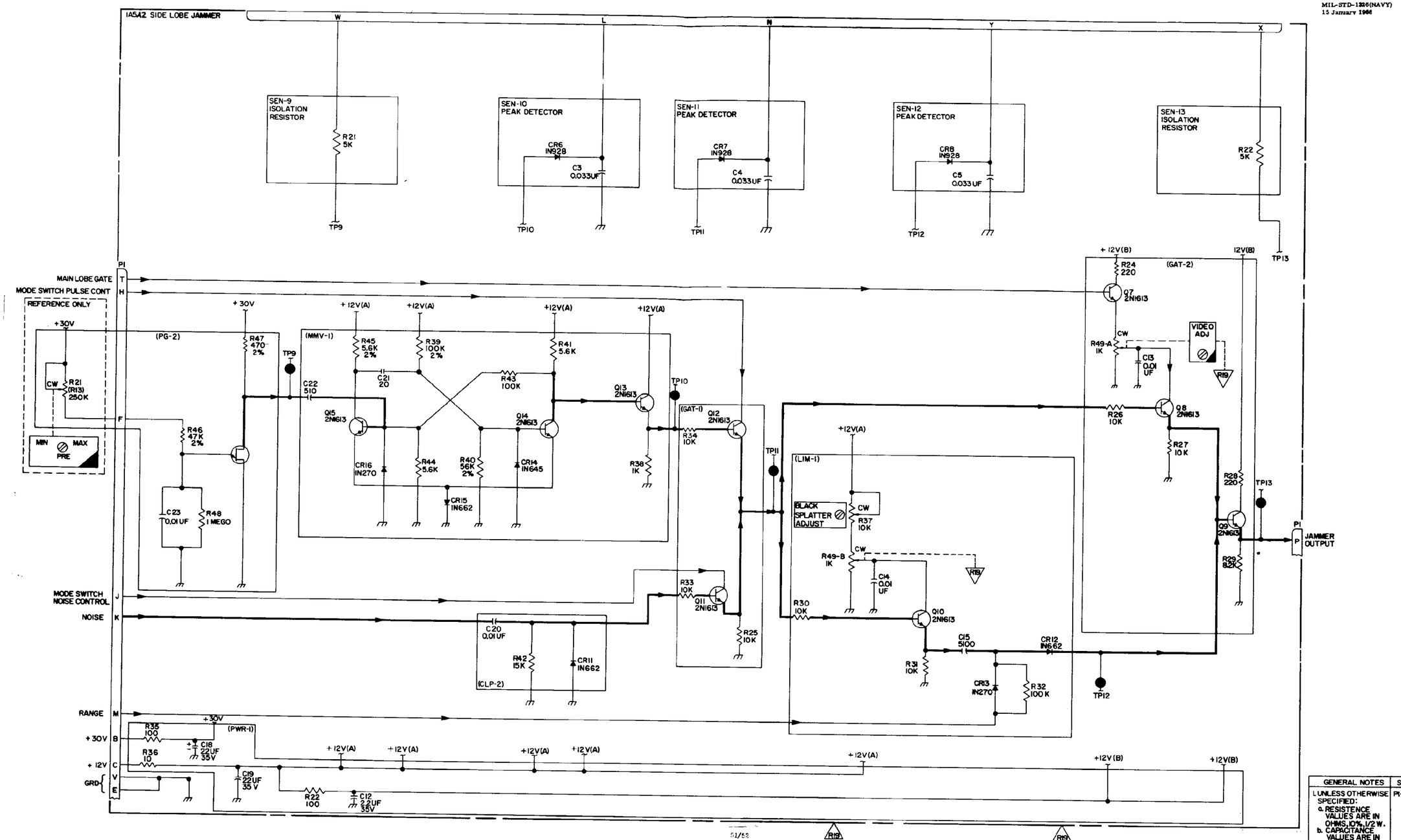


FIGURE 9 - BLOCKED SCHEMATIC, SAMPLE (PTEGR-PART).

GENERAL NOTES	SPARES
1. UNLESS OTHERWISE SPECIFIED: a. RESISTENCE VALUES ARE IN OHMS, 10%, 1/2 W. b. CAPACITANCE VALUES ARE IN PICROFARADS, 10%, 400V.	P1-A,D,G

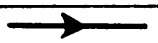
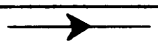
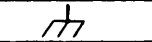
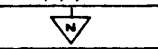
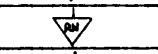
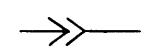
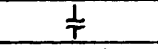
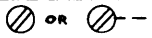
EXPLANATION OF SYMBOLS		
CATEGORY	BASIC SYMBOLS	MEANING OF SYMBOL
SIGNAL CODE SYMBOLS		MAJOR SIGNAL FLOW OR POWER DISTRIBUTION PATH
		SECONDARY FUNCTIONAL FLOW
		MAJOR GATING OR SYNCHRONIZING SIGNAL
		MINOR GATING OR SYNCHRONIZING SIGNAL
		PATH FOR ENERGIZING RELAY
		FEEDBACK PATH (EITHER POSITIVE OR NEGATIVE FEEDBACK)
		SIGNAL PATH USED TO LIGHT AN INDICATOR LAMP, PROVIDE A METER READING, OR ACCOMPLISH SOME OTHER TEST FUNCTION.
		REFERENCE SIGNAL
SYMBOLS USED FOR PURPOSE INDICATED		CIRCUIT COMMON
		CHASSIS GROUND
		UNREGULATED A-C NEUTRAL CONNECTIONS
		REGULATED A-C NEUTRAL CONNECTIONS
		ALL D-C RETURN CONNECTIONS
		THE GENERAL PURPOSE CONNECTOR SYMBOL IS USED ONLY FOR COAXIAL CONNECTIONS.
		TEST POINT
		BREAK SYMBOL
ADJUSTMENTS AND CONTROLS		SCREWDRIVER ADJUSTMENT
		KNOB ADJUSTMENT
		TOGGLE SWITCH

FIGURE 10-EXPLANATION OF SYMBOLS, SAMPLE.

C L P - 2

Clamps noise signal so that the complete signal output is positive with respect to ground.

GAT - 1

Provides means of gating on either noise or pulse jamming. Output is continuous pulses when Q12 is gated on by a continuous +12V. Output is continuous noise when Q11 is gated on by a continuous +12V. Output is groups of pulses when Q12 is gated on at the FM rate. Output is groups of noise pulses when Q11 is gated on at the FM rate.

GAT - 2

Main lobe pulses gate on the noise or pulse signal from GAT - 1. The amplitude of the gating signal is controlled by a front panel adjustment - Video adj R49-A. Capacitor C13 decouples noise.

L I M - 1

Output from GAT - 1 is limited by controlling the level of collector voltage applied to Q10 by front panel adjustment R49-B and Back Splatter Adj R37. C15, CR 13 and R 32 clamps the signal from Q10 to the reference range voltage. CR 12 passes that portion of the clamped signal which is above the output potential of Q8. The proportion of the input is controlled by increasing or decreasing the range voltage. C14 decouples noise.

MNV - 1

Multivibrator is triggered by the trailing edge of each pulse from PG-2. Output is positive square wave pulses with a duration of approximately 5 µsec and a PRF which is the same as that of PG-2.

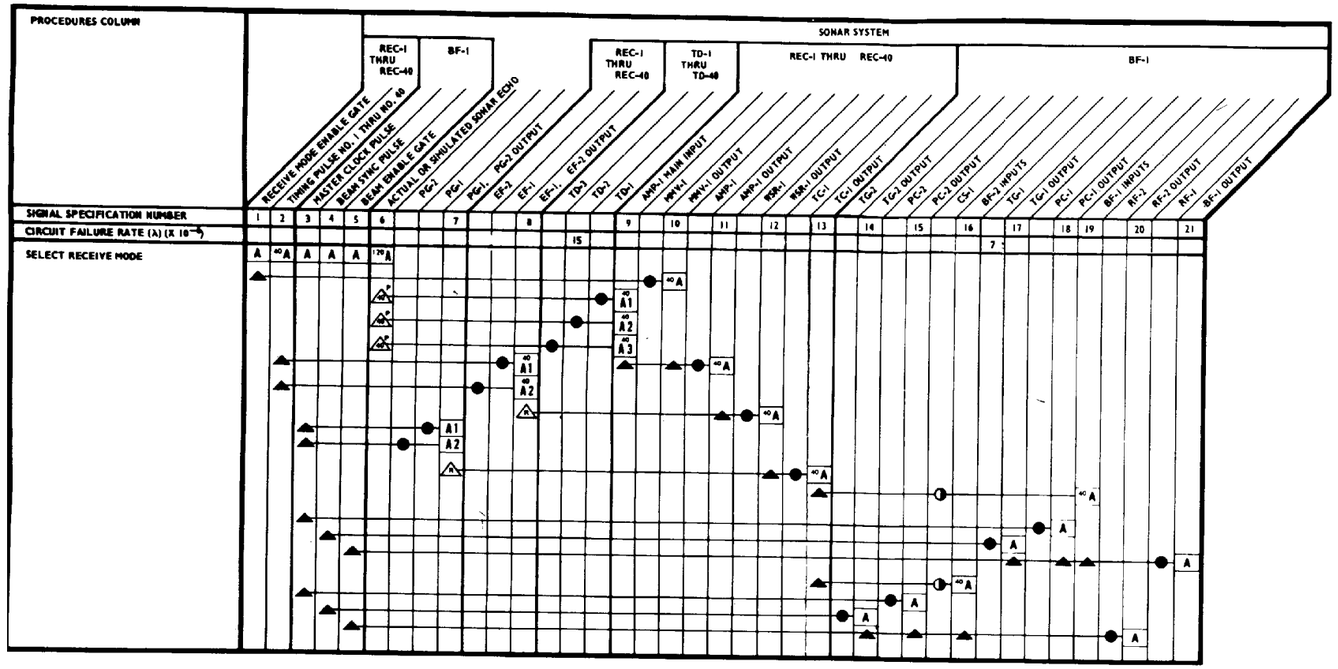
P G - 2

Unijunction transistor relaxation oscillator provides negative pulse output at the frequency of 300 to 3000 cps as controlled by 1A5R21.

PWR-1

Filters provide decoupling for input power.

FIGURE 11- SAMPLE TEST FOR FIGURE 9.



SIGNAL SPECIFICATIONS

1. WAVEFORM DATA
2.

SPEC NO.	ASSOCIATED FUNCTION	EVENT MEASUREMENT POINT	WAVEFORM DATA
2.1 2.2 ⋮ 2.40	REC-1 REC-2 ⋮ REC-40		

3. WAVEFORM DATA
4. WAVEFORM DATA
5. WAVEFORM DATA
6.

SPEC NO.	ASSOCIATED FUNCTION	EVENT MEASUREMENT POINT	WAVEFORM DATA
6.1 6.2 ⋮ 6,120	TD-1 TD-1 ⋮ TD-40		

7. A1, A2: WAVEFORM
8.

A1 AND A2				
SPEC NO.	ASSOCIATED FUNCTION	REQUIRED NPUT	EVENT MEASUREMENT POINT	WAVEFORM DATA
8.1 8.2 ⋮ 8.40	RBC-1 REC-2 ⋮ REC-40	2-1 2-2 ⋮ 2-40		

9.

SPEC NO.	ASSOCIATED FUNCTION	EVENT MEASUREMENT POINT	*EVENT INPUT	REQUIRED INPUT EVENTS	WAVEFORM DATA
9.1	REC-1	TP#	A1	6.1	
			A2	6.2	
			A3	6.3	
			COMPOSITE	6.1-6.3	
9.40	REC-40	TP#	A1	6.118	
			A2	6.119	
			A3	6.120	
			COMPOSITE	6.118-6.120	

*EVENT PORTIONS A1, A2 AND A3 ARE ASSOCIATED WITH TD-1, TD-2 AND TD-3 RESPECTIVELY.

10.

SPEC NO	ASSOCIATED FUNCTION	EVENT MEASUREMENT POINT	WAVEFORM DATA
10.1 10.2 ⋮ 10.40	REC-1 REC-2 ⋮ REC-40		

11.

SPEC NO.	ASSOCIATED FUNCTION	REQUIRED INPUT EVENTS	EVENT MEASUREMENT POINT	WAVEFORM DATA
11.1 11.2 ⋮ 11.40	REC-1 REC-2 ⋮ REC-40	9.1, 10.1 9.2, 10.2 ⋮ 9.40, 10.40		

12.

SPEC NO.	ASSOCIATED FUNCTION	REQUIRED INPUT EVENTS	EVENT MEASUREMENT POINT	WAVEFORM DATA
12.1 12.2 ⋮ 12.40	REC-1 REC-2 ⋮ REC-40	8.1, 11.1 8.2, 11.2 ⋮ 8.40, 11.40		

13.

SPEC NO.	ASSOCIATED FUNCTION	REQUIRED INPUT EVENTS	EVENT MEASUREMENT POINT	WAVEFORM DATA
13.1 13.2 ⋮ 13.40	REC-1 REC-2 ⋮ REC-40	7, 12.1 7, 12.2 ⋮ 7, 12.40		

14. WAVEFORM DATA
15. WAVEFORM DATA
16.

SPEC NO.	EVENT MEASUREMENT POINT	SCHEDULE AND WAVEFORM DATA
16.1 16.2 ⋮ 16.40		

17. WAVEFORM DATA
18. WAVEFORM DATA
19.

SPEC NO.	EVENT MEASUREMENT POINT	SCHEDULE AND WAVEFORM DATA
19.1 19.2 ⋮ 19.40		

20. WAVEFORM DATA
21. WAVEFORM DATA

FIGURE 12 - DESIGN OUTLINE, SAMPLE.

CATEGORY	SYMBOL	EXPLANATION OF DESIGN OUTLINE SYMBOLS
A BOX REPRESENTS AN EVENT SUCH AS THE ARRIVAL OF A VOLTAGE AT A CHECKPOINT, A LIGHT COMING ON, A MOTOR RUNNING, ETC.	A	AVAILABLE OR PERFORMING WITHIN SPECIFICATION
	NA	NOT AVAILABLE
	NM	NOT MEASUREABLE
	REM A	REMAINS AVAILABLE
	NORM	CONDITION DESCRIBED IN EVENT SPECIFICATION IS NORMAL
A BLACK BOX WITH WHITE LETTERING INDICATES THAT THE EVENT CAN BE RECOGNIZED FROM OUTSIDE THE EQUIPMENT ENCLOSURE	EN	RELAY ENERGIZED
LIT	I EN H	RELAY ENERGIZED. I INITIALLY ENERGIZED H HELD ENERGIZED
	D EN	RELAY DE-ENERGIZED
A GRAY BOX WITH BLACK LETTERING INDICATES THAT THE EVENT CAN BE RECOGNIZED OR MEASURED AT A READILY ACCESSIBLE POINT INSIDE THE EQUIPMENT	RUNS UP	MOTOR DRIVES VARIABLE TRANSFORMER TO INCREASE VOLTAGE
	RUNS DOWN	MOTOR DRIVES VARIABLE TRANSFORMER TO DECREASE VOLTAGE
LIT	LOW	TRANSFORMER IS AT LOW LIMIT (LOWEST VOLTAGE OUTPUT)
	OP	TRANSFORMER IS AT OPERATING LEVEL
A WHITE BOX WITH BLACK LETTERING INDICATES THAT THE EVENT CAN BE RECOGNIZED OR MEASURED AT A POINT WHICH IS MORE DIFFICULT TO ACCESS THAN REPRESENTED BY A GRAY BOX OR A BLACK BOX.	LIT	INDICATOR LAMP LIT
LIT	REM LIT	INDICATOR LAMP REMAINS LIT
	OUT	INDICATOR LAMP NOT LIT
	IND	INDICATES DESIRED VALUE WITHIN SPECIFICATIONS
	NO IND	INSTRUMENT NOT INDICATING
	RUNS	MOTOR OR BLOWER RUNS PROPERLY
	CONT RUN	MOTOR OR BLOWER CONTINUES TO RUN
	STOPS	MOTOR OR BLOWER STOPS RUNNING
	ON	STATE OF A DEVICE. (EXAMPLE: ANTENNA BRAKE APPLIED, ETC.)
	OFF	STATE OF A DEVICE. (EXAMPLE: ANTENNA BRAKE NOT APPLIED, BRAKE RELEASED, ETC.)
	ROT	DEVICE ROTATES (EXAMPLE: ANTENNA ROTATES)
	HELD	DEVICE HELD IN PLACE (EXAMPLE: ANTENNA HELD IN PLACE)
	●	REPRESENTS FUNCTIONAL ENTITY THAT MUST BE PERFORMING ITS FUNCTION PROPERLY FOR THE EVENT ON THE SAME LINE TO OCCUR WITHIN SPECIFICATION.
	◐	REPRESENTS FUNCTIONAL ENTITY WHICH IS PARTIALLY PROVEN GOOD IF THE EVENT ON THE SAME LINE OCCURS WITHIN SPECIFICATION. TO PROVE THE FUNCTIONAL ENTITY FULLY GOOD, EVENTS ON AT LEAST TWO DEPENDENCY LINES, OF WHICH THE FUNCTIONAL ENTITY IS A PART, MUST BE OPERATING WITHIN SPECIFICATION.
	◢	REPRESENTS ADJUSTABLE FUNCTIONAL ENTITY.
	●/	REPRESENTS RELAY CONTACT SET THAT PROVIDES CONTINUITY IN THE DE-ENERGIZED STATE.
	/●	REPRESENTS RELAY CONTACT SET THAT PROVIDES CONTINUITY IN THE ENERGIZED STATE.
	▲	INDICATES THAT THE EVENT OR EVENTS DIRECTLY ABOVE THE DEPENDENCY MARKER MUST BE AVAILABLE (AND WITHIN SPEC) FOR THE EVENT ON THE SAME LINE AS THE DEPENDENCY MARKER TO OCCUR (WITHIN SPEC) PROVIDED THE OTHER REPRESENTED FUNCTIONAL ENTITIES ALONG THE LINE ARE PERFORMING PROPERLY.

Figure 13-EXPLANATION OF DESIGN OUTLINE SYMBOL, SAMPLE

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