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DEFINITIONS OF TERMS FOR TEST, MEASUREMENT AND DIAGNOSTIC EQUIPMENT

FSC ATTS

DEPARTMENT OF THE NAVY

NAVAL ELECTRONIC SYSTEMS COMMAND

WASHINGTON, D.C. 20360

Definitions of Terms for Test, Measurement and Diagnostic Equipment (TMDE)
MIL-STD-1309C

1. This Military Standard is approved for use by all Departments and Agencies of the Department of Defense.

2. Recommended corrections, additions, or deletions should be addressed to Commander, Naval Electronic Systems Command, ATTN: 8111, Washington, D.C. 20363.

FOREWORD

Test, measurement, and the use of diagnostic devices are a prerequisite for maintaining operational readiness of equipment used by the three services in the performance of their assigned tasks. In order to improve communications and to facilitate coordination, key words or terms, more commonly used, are defined in this standard.

Not every test, measurement and diagnostic equipment (TMDE) term is listed. Oscilloscope, voltmeter and similar terms, which can be readily found in any standard technical dictionary, have been excluded. This document contains TMDE-related terms selected from the following sources:

DOD-STD-100	- Engineering Drawing Practices (Chap 700-Definitions)
MIL-STD-188	- Military Communications System Technical Standards
MIL-STD-196	- Joint Electronics Type Designation System (Para 3, Definitions)
MIL-STD-280	- Definitions of Item Levels, Item Exchangeability, Models, and Related Terms
MIL-STD-287	- Test Signals for Electronic Tactical Air Navigation Equipment (TACAN)
MIL-STD-415	- Test Provisions for Electronic Systems and Associated Equipment, Design Criteria For
MIL-STD-471	- Maintainability Demonstration
DOD-STD-480	- Configuration Control - Engineering Changes, Deviations, and Waivers (App E, Definitions).
MIL-STD-721	- Definitions of Effectiveness, Terms for Reliability, Maintainability, Human Factors, and Safety
MIL-STD-785	- Reliability Program for Systems and Equipment Development and Production
MIL-STD-883	- Test Methods and Procedures for Microelectronics

MIL-STD-1388-1	- Logistics Support Analyses (App b, Glossary).
MIL-STD-1472	- Human Engineering Design Criteria for Military System, Equipment and Facilities (Para 3, Definitions)
MIL-STD-1552	- Provisioning Technical Documentation, Uniform DOD Requirements for (Para 3, Definitions)
MIL-STD-1561	- Provisioning Procedures, Uniform DOD (Para 3, Definitions)
MIL-STD-2073	- DOD Packaging Data Forms, Instructions for Preparation and Use, (Para 3, Definitions)
MIL-STD-2077	- Test Program Sets, General Requirements for
MIL-E-16400	- Electronic, Interior Communication and Navigation Equipment, Naval Ship and Shore, General Specification For
MIL-T-28800	- Test Equipment for Use with Electrical and Electronic Equipment, General Specification
MIL-S-83490	- Specifications, Types and Forms

Joint Services Automatic Testing

Pamphlets identified by each Services' Number:

(1) Joint Service Automatic Testing (AT) Acquisition Planning Guide (AFSCP/AFLCP 800-38)

(2) Built-In-Test Design Guide (AFSCP/AFLCP 800-39)

(3) Joint Service Weapon System Acquisition Review Guidelines for AT (AFSCP/AFLCP 800-40)

Air Force Manual, "Communications - Electronics Terminology", AFM-11-1, Volume III, 30 March 1970.

Defense Standardization Manual 4120.3M.

Army Regulation No. 750-43. Test, Measurement, and Diagnostic Equipment (including Prognostic Equipment and Calibration Test/Measurement Equipment), Department of the Army, Washington, D.C., 24 July 1975, ch. 1, 22 September 1976.

TM 11-486-11. Electrical Communications Systems, Engineering Definitions and Abbreviations. HQ, Dept. of the Army, August 1963.

NAVAIR INSTRUCTION 5400.67. Certification Program for Navy Air-Launched Guided Weapon Test Systems, Naval Air Systems Command, Washington, D.C., 10 March 1972.

NAVMAT Acquisition Guide

NAVMAT INSTRUCTION 4355.67. Department of the Navy Metrology and Calibration (METCAL) Program, Chief of Naval Material, Washington, D.C. 1973.

NAVORD INSTRUCTION 4855.19. Certification Program for Naval Weapons and Weapon Systems Support Test Systems, Naval Ordinance Systems Command, Washington, D.C. 20360, 11 November 1971.

A Compendium of Authenticated Logistics Terms and Definitions. Air Force Institute of Technology, School of Systems and Logistics, Wright-Patterson AFB, Ohio, Fred Gluck, Editor, 1970.

Anthony Ralston, "Encyclopedia of Computer Science" Petrocelli/Charter, New York, 1st Edition, 1976.

Van Nostrand Scientific Encyclopedia, 5th ED., 1976.

Charles J. Sippl, "Computer Dictionary and Handbook", Howard W. Sams and Co., Inc., Indianapolis, Indiana, 1966.

Martin H. Weik, "Standard Dictionary of Computer and Information Processing", Hayden Book Co., New York, 1969.

ANSI X3.12-1970. American National Standard, Vocabulary for Information Processing. American National Standards Institute, New York, 1970.

IFIP Guide to Concepts and Terms in Data Processing, edited by Ian H. Gould University of London. North-Holland Publishing Company, Amsterdam - London, 1971.

IEEE Standard Dictionary of Electrical and Electronic Terms, approved September 28, 1971, by the American National Standards Institute, IEEE Std-100-1972 - ANSI C42.100-1972.

International Dictionary of Physics and Electronics, 2nd Edition, D. Van Nostrand Company, Inc., Princeton, NJ, 1961.

Modern Dictionary of Electronics by Rudolf F. Graf, Howard W. Sams & Co., The Bobbs-Merrill Co., New York, 4th Edition, 1972.

Electronic Engineer's Handbook, Donald Funk, 1st 15.D. 1975, McGraw-Hill.

Handbook of Components for Electronics, Charles Harper, 1977, McGraw-Hill.

CONTENTS

DEFINITIONS OF TERMS
FOR
TEST, MEASUREMENT AND DIAGNOSTIC EQUIPMENT

1. SCOPE

1.1 Purpose. This standard contains definitions of the most commonly used terms for test, measurement and diagnostic equipment (TMDE).

1.2 For purpose of this standard, the term "Unit Under Test" (UUT) is used to denote any hardware entity under going testing.

2. REFERENCE DOCUMENTS

2.1 General. The following documents of the issue in effect on the date of invitation for bids or request for proposal form a part of this standard to the extent specified herein.

STANDARDS

MILITARY

MIL-STD-1345 (NAVY)	Test Requirements Document Preparation of
MIL-STD-1519 (AF)	Test Requirements Document Preparation of

Other publications.

DA-PAM 700-21	TMDE Register Index and Instruction Parts 1 and 2

3. DEFINITIONS

3.1 The following definitions shall apply to the terms stated.

3.1.1 Abbreviated test language for all systems (ATLAS). A Department of Defense (DOD) directed standard test language (ANSI/IEEE 416-1978, and its official successors) whose major features are; (1) standard testing terminology to reduce erroneous interpretations; and (2) UUT oriented test statements to increase portability (ability to be used with different test equipment configurations).

3.1.2 Absolute error. The magnitude of the error without regard to algebraic sign.

3.1.3 Accelerated life test. A test in which certain factors, such as voltage, temperature, and so forth, are increased or decreased beyond normal operating values to obtain observable deterioration in a reasonable period of time, and thereby afford some measure of the probable life under normal operating conditions or some measure of the durability of the equipment when exposed to the factors being aggravated.

3.1.4 Acceptance test. A test which verifies that the UUT is operating in accordance with the operational specifications.

3.1.5 Access time. The time required under specified conditions to communicate with a storage device, and transfer data to or from that device, including the time required to search for and find the storage location once the command is given.

3.1.6 Accessory. An assembly of a group of parts or an item which is not always required for the operation of a test set or unit as originally designed but serves to extend the functions or capabilities of the test set.

3.1.7 Accumulator. The group of circuits or registers within arithmetic or logic assemblies in which certain operations are performed and the results stored temporarily.

3.1.8 Accuracy. The extent to which a given measurement agrees to a universally accepted standard value.

3.1.9 Accuracy augmentation routine. Test routines using auxiliary test equipment that is more accurate than the automatic test equipment complement, as may be necessary when test accuracy ratios cannot be met otherwise.

3.1.10 Accuracy enhancement. A process which provides accuracies beyond the individual instrument capability by monitoring the instrument performance with another instrument of much greater accuracy over the duration of the test, or by means of software algorithms.

3.1.11 Acquisition time. The time required, after sampling an input voltage, for the hold capacitor to charge to that input voltage change or full scale and remain within a specified tolerance or error band around that input voltage.

3.1.12 Activation. The process of creating a logic value at the location of a fault that differs from the logic value that location would have under the presence of the fault.

3.1.13 Active built-in-test (BIT). A type of BIT which is temporarily disruptive to the prime system operation through the injection of test stimuli into the system.

3.1.14 Active redundancy. That condition where parallel back-up items are operating simultaneously, rather than being switched on when needed.

3.1.15 Active sensor. (1) A sensor requiring a source of power other than the signal being measured. (2) A sensor that provides a signal by stimulating the UUT.

3.1.16 Adapter kit. A kit containing an assortment of cables and adapters for use with test or support equipment.

3.1.17 Address. An identification, represented by a name, label, or number for a register or location in storage. Addresses are also part of an instruction word along with commands, tags, and other symbols.

3.1.18 Adjustment. Changing (by electronic, electrical or physical means) a variable in an item to cause a change in its output characteristics.

3.1.19 Algorithmically generated pattern. An array of digital data automatically generated by a predetermined software routine or program. The pattern may be generated and applied in real time.

3.1.20 Alignment. A sequence of adjustments providing optimum performance characteristics.

3.1.21 Alignment kit. A set of instruments or tools necessary for the adjustment of electrical or mechanical components.

3.1.22 Alignment program. A program used to align instruments and signal paths to known characteristics.

3.1.23 Alphanumeric. A character set that contains both letters and numbers.

3.1.24 Ambiguity delay. A delay model which allows the minimum and maximum propagational delay through an element to be specified. The state of the element between minimum and maximum delay is unknown, and is called the ambiguity region.

3.1.25 Ambiguity group. The group of maintenance replaceable units which may have faults resulting in the same fault signature.

3.1.26 Analog. Data in the form of continuously variable quantities, such as voltage, frequency, current, etc.

3.1.27 Analog computer. A computer which represents variables by existing analogies. Thus, a computer which solves problems by translating existing conditions such as flow, temperature, pressure, angular position or voltage into related mechanical or electrical equivalent quantities as an analog for

the existing phenomenon being investigated. In general, it is a computer which uses an analog for each variable and produces analogs as outputs. Thus, an analog computer measures continuous quantities whereas a digital computer operates on discrete data.

3.1.28 Ancillary equipment. Equipment which is auxiliary or supplementary to an installation. Ancillary equipment usually consists of standard off-the-shelf items such as oscilloscopes and digital multimeters (also called auxiliary equipment).

3.1.29 Aperture delay. The time elapsed from the hold command to when the switch actually opens.

3.1.30 Aperture uncertainty. The time variation from sample to sample of the aperture delay.

3.1.31 Architecture. A method or style of building a system (hardware or software). The construction, frame or structure of that system.

3.1.32 Arithmetic unit. That portion of the hardware of a device by which arithmetic and logical operations are performed.

3.1.33 Assembler. A computer program which translates assembly language mnemonic source statements into binary strings representing machine code operations. It also assigns either relative or absolute memory addresses to resulting instructions and data items.

3.1.34 Assembly level language. A computer language in which machine operations and locations are represented by mnemonic symbols.

3.1.35 ATE bit skew. The maximum time difference between the first and last digital pulse arriving at the ATE interface within the same digital test pattern.

3.1.36 ATE control software. Resident software (executive or operating system) used during execution of a test program to control the testing operations of the ATE. This software is used to execute a test procedure but does not contain any of the stimuli or measurement parameters used in testing the UUT. Where test software and control software are combined in one inseparable program, that program will be treated as test software, not control software.

3.1.37 Automatic calibration. The capability of a test system to automatically check its own accuracy by means of internal standards.

3.1.38 Automatic self-test. Self-test to that degree of fault detection and isolation which can be achieved entirely under computer control, without human intervention.

3.1.39 Automatic test. That performance assessment, fault detection, diagnosis, isolation, and prognosis which is performed with a minimum of reliance on human intervention. This may include BIT.

3.1.40 Automatic test equipment (ATE). Equipment that is designed to automatically conduct analysis of functional or static parameters and to evaluate the degree of UUT performance degradation; and may be used to perform fault isolation of UUT malfunctions. The decision making, control, or evaluative functions are conducted with minimum reliance on human intervention and usually done under computer control.

3.1.41 Automatic test generator (ATG). A generic computer program which automatically generates the test patterns and responses from UUT circuit equivalent inputs.

3.1.42 Automatic test program generator (ATPG). Same as paragraph 3.1.41.

3.1.43 Automatic test system. The composite grouping of equipments, software, and data required to test a unit automatically.

3.1.44 Automatic testing. That discipline which concerns itself with the development, acquisition, and application of automatic test.

3.1.45 Auxiliary equipment. Same as paragraph 3.1.28.

3.1.46 Availability. A measure of the degree to which an item is in operable and committable state at the start of a mission, when the mission is called for at an unknown (random) point in time.

3.1.47 Back driving. The process of forcing a logic level onto the output of a device that differs from the level it is attempting to drive.

3.1.48 Back trace. The process of tracing back from the failure site to the primary inputs and making an input assignment so that a distinguishable test can be produced at the failure site.

3.1.49 Baud rate. The operating number of the bits, handled by a device in a given unit of time, under specified conditions.

3.1.50 Bed of nails interface adapter. A type of interface adapter which uses a series of pogo-pins or nails to make contact with the UUT.

3.1.51 Beginners all-purpose symbolic instruction code (BASIC). A high level language used in ATE computing controllers.

3.1.52 Benchmark. A test point for comparison purposes; in microprocessor-based equipment, a benchmark program is one used to compare aspects of performance among competing systems.

3.1.53 Bidirectional bus. A conductor or group of conductors which transmits and receives digital data on the same line(s).

3.1.54 Binary code. A code in which each element is defined by a series of binary digits. It is based on the mathematical number system of base or radix 2.

3.1.55 Binary digit. A digit that has only two values represented by a "0" for the absence of a pulse; or a "1" for the presence of a pulse.

3.1.56 Binary simulator. A program which establishes a representation of a logic circuit or configuration based upon a computer-directed or processed model of the logic circuit or configuration.

3.1.57 Bit. A contraction of the term binary digit.

3.1.58 Bit per unit time (Bit Rate). Same as paragraph 3.1.49.

3.1.59 Blank. (1) A place of storage where data may be stored (synonymous with "space"). (2) A character used to indicate an output space on a printer in which nothing is printed. (3) A condition of no information at all in a given column of a punched card or in a given location on perforated tape. (4) A period of no data transmission.

3.1.60 Block input. (1) A section of internal storage of a computer, reserved for the receiving and processing of input information (synonymous with "input area"). (2) A block used as an input buffer. (3) A block of machine words considered as a unit and intended to be transferred from an internal storage medium to an external destination.

3.1.61 Block output. (1) A section of internal storage, reserved for storing data which are to be transferred out of the computer. (2) A block used as an output buffer. (3) A block of machine words considered as a unit and intended to be transferred from an internal storage medium to an external destination.

3.1.62 Branch instruction. An instruction in the program that provides a choice between alternative subprograms or subroutines in accordance with the test logic. It is usually based on a program decision.

3.1.63 Breakdown. A disruptive discharge through insulation, involving a sudden and large increase in current due to failure of the insulation under electrostatic stress.

3.1.64 Bridge fault. Short circuits or leakage between adjacent paths (lands, traces) on a printed circuit board (card).

3.1.65 Buffer. An isolating circuit used to avoid reaction of a driven circuit on the corresponding driving circuit.

3.1.66 Building block. A measurement or stimulus device, usually programmable, such as multimeter, power supply, switching unit, frequency meter, installed as an integral part of the test equipment.

3.1.67 Built-in-test (BIT). An integral capability of the mission equipment which provides an on-board, automated test capability to detect, diagnose, or isolate system failures. The fault detection and, possibly, isolation capability is used for periodic or continuous monitoring of a system's operational health, and for observation and, possibly, diagnosis as a prelude to maintenance action.

3.1.68 BIT, active. Same as paragraph 3.1.13.

3.1.69 BIT, continuous. A type of BIT which continually monitors system operation for errors. Examples include parity and other error detecting codes.

3.1.70 BIT equipment. Test and fault-isolation hardware or software designed into the circuitry of a system.

3.1.71 BIT, initiated. A type of BIT which is executed only after the occurrence of an external event such as an action by an operator.

3.1.72 BIT, passive. A type of BIT which is non-disruptive and non-interferring to the prime system.

3.1.73 BIT, periodic. A type of BIT which is initiated at some frequency. An example is BIT software executing during planned processor idle time.

3.1.74 BIT turn-on. A specific type of initiated BIT which is exercised each time power is applied to the unit or system.

3.1.75 Bulk storage. A supplementary large volume memory or storage device.

3.1.76 Burn-in. The operation of items prior to their end application to stabilize their characteristics and identify early failures.

3.1.77 Burst. A pulse train that starts at a prescribed time and continues for a specified duration (or number of pulses).

3.1.78 Bus. A conductor, or group of conductors, which serve as the path for carrying digital control, address, and information signals. Also power distribution between controlling and controlled electronic items.

3.1.79 Byte. (1) A generic term to indicate a measureable portion of consecutive binary digits; for example, an 8-bit or 6-bit type. (2) A group of binary digits usually operated upon as a unit.

3.1.80 Calibration. The comparison of a measurement system or device of unverified accuracy to a measurement system or device of known and greater accuracy, to detect and correct any variation from required performance specifications of the measurement system or device.

3.1.81 Calibration adapter. An interface adapter which may include precision active circuits to aid in ATE self certification, or to verify calibration of ATE instruments or functions, and building blocks.

3.1.82 Calibration interval, period, or cycle. The designated period of time between calibration services. During this time the instrument should remain within specific performance levels, with a specified probability, under normal conditions of handling and use.

3.1.83 Calibration procedure. The specific steps and operations to be followed by activity personnel in the performance of an instrument calibration.

3.1.84 Cam-programmed. (1) A programming technique that uses a rotating shaft, having specifically oriented, eccentric projections which control a series of switches that set up the proper circuits for a test. (2) A cam-follower system used to set positions or values of a shafted instrument for programming instructions to the test system.

3.1.85 Cannot duplicate (CND). A fault indicated by BIT or other monitoring circuitry which cannot be confirmed at the next level of maintenance.

3.1.86 Card field. An area on a computer input card (one or more columns or portion of a column) which is regularly assigned for use as a separate identifiable item.

3.1.87 Card-programmed. The capability of a computer to perform a sequence of tests according to instructions contained in one or a deck of punched cards.

3.1.88 Catastrophic failure. Change in the operating characteristics of an item resulting in considerable degradation of useful performance.

3.1.89 Catastrophic fault. A defect or malfunction in a component, assembly, or system causing a sudden change in its operating characteristics which results in a substantial lack of useful performance of the device or system.

3.1.90 Central integrated test system. An on-line test system which processes, records, or displays at a central location, information gathered by test point data sensors at more than one remotely located equipment or system under test (also called system integrated test system).

3.1.91 Certification. The process of officially authenticating the capability of a test support system to assess accurately the quality of UUTs.

3.1.92 Channel. A single path for transmitting electrical signals, usually in distinction from other parallel paths.

3.1.93 Character. A digit, letter, or special symbol, such as 1, 7, s, ", %, and so forth, or its digital equivalent.

3.1.94 Character density. The number of characters that can be stored per unit area or length.

3.1.95 Check routine. A routine or program designed to provide information about the operational condition of a computer or computer control system. Generally, a check routine is designed to give the operator of the system a high confidence level that the equipment is operating properly (also called check program).

3.1.96 Checkout. A sequence of tests for determining whether or not a device or system is capable of, or is actually performing, a required operation or function.

3.1.97 Checkout equipment. Electric, electronic, optical, mechanical, hydraulic, or pneumatic equipment, either automatic, semiautomatic, or manual, or any combination thereof, which is required to perform the checkout function.

3.1.98 Checkout time. The time required to determine whether designated characteristics of a system are within specified values.

3.1.99 Checkpoint. A place in a routine where a check or recording of data for restart purposes is performed.

3.1.100 Checksum. The sum of every byte contained in an input/output (I/O) record used for assuring integrity of the programmed entry.

3.1.101 Circuit. A conductor, or system of conductors, and active or passive elements through which an electric current is intended to flow to produce a specific electrical or electronic function.

3.1.102 Circuit card tester. An instrument for testing and diagnosing printed circuit cards.

3.1.103 Circuit image. The representation of the functions and interconnections of an electronic circuit in a format compatible with the ATPG system being used.

3.1.104 Circuit load. A device or an electronic circuit which provides a simulation of the normal I/O of the circuit under test.

3.1.105 Circuit malfunction analysis. The logical, systematic examination of circuits and their diagrams to: (a) identify and analyze the probability and consequence of potential malfunctions; and (b) to determine related maintenance and support requirements to investigate effects of failures (allied with failure modes and effects analysis (FMEA)).

3.1.106 Circuit simulator. A computer program which simulates the operation of an electronic circuit. It also analyzes the efficiency of stimulus test patterns on itself.

3.1.107 Clock. A device that generates periodic signals used for synchronization.

3.1.108 Closed loop testing. Testing in which the input stimulus is controlled by the UUT output.

3.1.109 Closed subroutine. A subroutine not stored in the normal program sequence.

3.1.110 Coding. That part of the test program development process where the test sequences are translated into the language of the ATE controller.

3.1.111 Command. An electronic pulse, signal, or set of signals to start, stop, change, or continue some operation.

3.1.112 Common mode noise. Ground currents caused by alternating current power flowing in ground leads.

3.1.113 Common mode noise rejection. The ability to reduce common mode potential in a floating measurement system.

3.1.114 Common mode rejection ratio. The ratio of differential voltage gain to common mode voltage gain, usually expressed in decibels.

3.1.115 Common support equipment. That support equipment which is applicable to several systems, subsystems, or items of equipment.

3.1.116 Common UUT. A UUT that shares an interconnection device or adapter, test program procedure or ATE/TMDE with another UUT.

3.1.117 Comparative test. Comparative tests compare end item signal or characteristic values against a specified tolerance band and present the operator with a go or no-go readout; a "go" for signals within tolerances, and a "no-go" for signals out-of-tolerance.

3.1.118 Comparator. (1) A device capable of comparing a measured value with predetermined limits to determine if the value is within these limits. (2) A device capable of comparing digital signals to determine agreement.

3.1.119 Comparison tester. A device which uses a known good unit (golden unit) as a means for comparing test results with the UUT when both are subjected to the same stimuli.

3.1.120 Compatibility. Design features of a UUT which provide functional, electrical, and mechanical interfacing with the intended ATE and which minimize the use of unique or complex interface devices.

3.1.121 Compiler. A computer program which translates high order language instructions of a computer program into machine language before the instructions are executed (for example, BASIC to machine code).

3.1.122 Compiler-driven simulation. The simulation carried out by translation of the network description into machine executable code. This technique is employed for clocked (synchronous) networks, and primitive blocks.

3.1.123 Comprehensive testability. An overall testability design characteristic which includes both hardware design and test design.

3.1.124 Computer aided design. A software system which aids in prediction of system or circuit performance by projecting output results in response to inputs and circuit configuration.

3.1.125 Computer-guided probe. A fault isolation technique based solely on the good circuit data. The probe algorithm acts as the master instruction operator to probe various integrated circuit pins on the UUT until it derives the final diagnosis and diagnostics.

3.1.126 Computer program. An organized sequence of instructions, commands, and data which cause a machine to automatically execute some desired function.

3.1.127 Computing controller. A device used in an ATE to automatically control the ATE's programmable instruments to perform the programmed tests, then process the resulting test measurements to see if they are in tolerance and, when they are not, to provide fault isolation information.

3.1.128 Concurrent fault simulation. Fault list type simulations during which fault lists, associated with each primitive block, are propagated by using the same elemental evaluator routines used by the failure free simulation. The concurrency consists in the fact that for each primitive scheduled to be evaluated, its failure free behavior is computed first and then its fault list is computed.

3.1.129 Confidence test. (1) A test performed to provide a high degree of certainty that the UUT is operating acceptably. (2) A check of the performance of all test system stimulus and measurement functions, to detect degradation with respect to system specifications, and to inform the system operator.

3.1.130 Contact. (1) A connection between two conductors that permits a current flow path. (2) A part or device that makes or breaks a current path connection.

3.1.131 Continuous BIT. Same as paragraph 3.1.70.

3.1.132 Control panel. That part of ATE which includes the means by which the operator can control the ATE functions.

3.1.133 Control point. A design attribute to enhance testability by enabling, disabling, blocking, resetting an so forth, functions within a system to effect efficient test control.

3.1.134 Control point selector. A device capable of selecting and controlling the proper stimulus, power or load, and applying it to the UUT, in accordance with instructions from the programming device.

3.1.135 Controllability. An attribute of equipment design which defines or describes the extent to which signals of interest may be controlled.

3.1.136 Controller. A hardware interface that accepts instructions from a computer and reformats them to program an instrument or peripheral.

3.1.137 Converter. A device which changes the manner of representing information from one form to another.

3.1.138 Correlation. A portion of certification which establishes the mutual relationships between similar support test systems by comparing test data on specimen hardware or simulators.

3.1.139 Crest factor. The ratio of a signal's peak voltage level either positive or negative (whichever is greater) to its root-mean-square value.

3.1.140 Critical race condition. The nearly concurrent change of two or more lines which may result in any one of two or more stable states being entered.

3.1.141 Cross coupling. The amount of undesired energy appearing in one signal path as a result of coupling from other signal paths.

3.1.142 Crossbar switch/crossbar scanner. An electrical or electronic device having a plurality of "n" vertical paths and "m" horizontal paths, establishing "n" times "m" crosspoints or interconnections for the cross-switching of data circuits consisting of signal data, power, modifiers, or monitors for the purpose of injecting, altering, monitoring, or comparing information for test analyses. The switching may be accomplished by relays, tubes, transistors or diodes under manual or automated control. The scanner scans each sensor point during the measure and compares actions of the test equipment.

3.1.143 Crosstalk. Same as paragraph 3.1.141.

3.1.144 Data link. An information-carrying medium (such as a phone line) by which data between a data-generating device and a data-processing device is transmitted.

3.1.145 Data logger. A system to measure a number of variables and make a written tabulation in a form suitable for computer input.

3.1.146 Data processor. A device which operates on data (such as the computing portion of an ATE's computing controller).

3.1.147 Data reduction. The process of transforming masses of raw data or experimentally obtained data, usually gathered by instrumentation, into useful, ordered or simplified intelligence.

3.1.148 Debug. The process of detecting and removing errors or faults from a computer program or from electronic equipment.

3.1.149 Dedicated switching. The property of a switching matrix which allows each device in a test system to connect to a unique point on the output.

3.1.150 Deductive fault simulator. Fault list type simulator during which fault lists associated with each primitive mode (and internal states, if any) are propagated by performing set operations by using the results of the failure free simulator, executed previously rather than concurrently, as a guideline. For each primitive, there is a deductive routine different from the elemental evaluation routine used by the failure free simulator.

3.1.151 Delay fault. A fault in a digital device such that switching occurs to the proper level but does so outside of a specified time interval.

3.1.152 Delay line. A transmission line or equivalent device designed to delay a signal for a predetermined length of time.

3.1.153 Delay line storage. A storage or memory device consisting of a delay line means for regenerating and reinserting information into the delay line.

3.1.154 Dependent failure. A failure which is caused by the failure of an associated item, distinguished from independent failure.

3.1.155 Dependent fault. A fault which is caused by the failure of an associated element.

3.1.156 Dependent node. A node having one or more incoming branches.

3.1.157 Depot maintenance. Maintenance performed on material requiring major overhaul or a complete rebuild of parts, subassemblies, and end items, including the manufacture of parts, modification, testing, and reclamation as required. Depot maintenance serves to support lower categories of maintenance by providing technical assistance and performing that maintenance beyond their responsibility. Depot maintenance provides stocks or serviceable equipment by using more extensive facilities for repair than are available in lower level maintenance activities.

3.1.158 Design fault. A fault due to inadequate hardware or software design.

3.1.159 Design for testability. A design process or characteristic thereof such that deliberate effort is expended to assure that a product may be thoroughly tested with minimum effort, and that high confidence may be ascribed to test results.

3.1.160 Destructive testing. (1) Prolonged endurance testing of equipment or a specimen until it fails in order to determine service life or design weakness. (2) Testing in which the preparation of the test specimen or the test itself may adversely affect the life expectancy of the UUT or render the sample unfit for its intended use.

3.1.161 Diagnosis. The functions performed and the techniques used in determining and isolating the cause of malfunctions.

3.1.162 Diagnostic accuracy. The percentage of failures correctly diagnosed, based on the possible failure population.

3.1.163 Diagnostic capability. All capabilities associated with the detection and isolation of faults, including built-in test, automatic test systems, and manual test.

3.1.164 Diagnostic flow chart. A test oriented logical description of branching routines used in a test sequence to describe the steps taken to diagnose a failure successfully.

3.1.165 Diagnostic routine. A logical sequence of tests designed to locate a malfunction of the UUT. The software to perform these tests.

3.1.166 Diagnostic test. A test performed for the purpose of isolating a malfunction in the UUT or confirming that there actually is a malfunction.

3.1.167 Digital. The use of data carrying signals that are restricted to either of two voltage levels, corresponding to logic "1" or "0".

3.1.168 Digital circuit simulator. A computer program which (upon being fed a description of a digital circuit) simulates the circuit, then (upon generating or being fed test patterns) analyzes how well the patterns exercise (toggle the nodes in) the circuit.

3.1.169 Digital clock. A series of synchronized pulses that determine the bit times (data rate) of a digital pattern.

3.1.170 Digital computer. A computer in which discrete quantities are represented in digital form and which generally is made to solve mathematical problems by iterative use of the fundamental processes of addition, subtraction, multiplication, and division.

3.1.171 Digital driver. The output stage of a digital data generator.

3.1.172 Digital section. A portion of ATE that includes all of the digital circuitry required for testing units.

3.1.173 Direct memory access. The transfer of data directly from or to computer memory to or from a peripheral.

3.1.174 Don't care state. A portion of primary input or output patterns created for a UUT that are not assigned specific values.

3.1.175 Down time. The period during which a system or device is not operating due to internal failures, scheduled shut down, or servicing.

3.1.176 Dual port. An architechural implementation which allows ATE hardware resource sharing between two ATE interfaces which may be used for testing different UUTs.

3.1.177 Dummy load. A device or any electronic circuit which provides a simulation of the normal input or output of a circuit or a system under test.

3.1.178 Dump. (1) To duplicate the contents of a section of computer memory in another section of the computer system. (2) To remove power from a computer system containing volatile storage data.

3.1.179 Dynamic dumping. The printing of diagnostic information without stopping the program being tested.

3.1.180 Dynamic functional test. A testing sequence performed at or about rated speed usually done by continuously clocking the UUT.

3.1.181 Dynamic test. Any test performed when the UUT or system is in dynamic operation.

3.1.182 Edit. To correct errors or logic or make changes in a test program.

3.1.183 Editor. An interactive software subsystem that allows users to modify test programs directly.

3.1.184 Edge connector. The portion of a circuit board which is used for communication of input, output and power signals between itself and the prime system.

3.1.185 Electrical partitioning. The electrical or electronic separation of system or unit elements for the purpose of enhanced testing.

3.1.186 Electronic knife. A probe used primarily in digital testing to sense direction of current flow to assist isolation to the defective node in a net.

3.1.187 End-to-end run time. The time for a test program to determine that a good UUT is good.

3.1.188 English language programming. A technique of programming which allows the programmer to write programs and routines in English language statements.

3.1.189 English level language. A computer language in English terms which represent multiple binary instructions which can be processed directly by the machine (examples: ATLAS, BASIC, and so forth). Also called High Order Language.

3.1.190 Entry point. One of a set of points in an ATE program where the test conditions are completely stated and are not dependent on previous tests or setups in any way. Such points are the only ones at which it is permissible to begin part of the complete test program.

3.1.191 Equipment path measurement. A measurement of the path impedance in a test system, between the UUT and the stimulus source or response monitor.

3.1.192 Equipment replaceable unit. The lowest assembly or individual part that can be fault detected, isolated, removed, replaced and verified functional at organization level without disassembly of the equipment to which it is attached in consonance with the maintenance concept.

3.1.193 Equipment signature. The special characteristics of an equipment's response to a stimulus or of its electrical, electromagnetic, infrared or acoustical emissions.

3.1.194 Equivalent faults. Two or more faults which create the same response for all possible tests.

3.1.195 Equivalent gate count. A measure of circuit size. The circuit is analyzed as to its gate structure (NAND, NORS, and so forth) and all gates are counted.

3.1.196 Erasable programmable read only memory (EPROM). A solid-state memory device which, after being programmed, can be re-programmed.

3.1.197 Erasable storage. Storage media that may hold information that can be changed.

3.1.198 Error. The deviation of a computed, observed, or measured quantity from the true, specified or theoretically correct value of the quantity.

3.1.199 Error code. Refers to the progressive tolerance allowances made at increasingly higher levels of test where components have the tightest tolerance requirements (for example, incoming inspection) progressing to the widest tolerance band at the system level of test (for the same component).

3.1.200 Error correcting codes. In the transmission of digital data, the use of additional (redundant) bits to permit the detection and correction of errors.

3.1.201 Error detecting codes. In the transmission of digital data, the use of additional (redundant) bits to permit the detection of errors.

3.1.202 Error logging. A function of BIT which saves error data (and system status data at the time of the error) in a local storage for the purpose of diagnosing intermittent faults at the next level of maintenance.

3.1.203 Event directed simulation. The simulation of an element when an event occurs on one of its inputs. (An event is the change in a signal value. An element will only change signal value when one or more of its inputs change values. Hence, a given element need only be simulated when an event occurs on one of its inputs.)

3.1.204 Exact match fault dictionary. A fault dictionary whose use is based on the exact matching of observed fault signatures versus predicted fault signatures from the dictionary.

3.1.205 Executable statement. A test statement which will cause some action to be performed during test run-time.

3.1.206 Executive routine. A master set of coded instructions designed to process and control other sets of coded instructions.

3.1.207 Executive test system. A software module which supervises the execution of the test system monitor and module control software.

3.1.208 Exercise. To operate an equipment in such a manner that it performs all its intended functions to allow observation, testing, measurement and diagnosis of its operational condition.

3.1.209 Exercising diagnostics. Routines which exercise the UUT, causing latent and intermittent failures to occur. These are used as a trouble-shooting aid.

3.1.210 External storage. Information storage off-line in media such as magnetic tape, punched tape, punched cards, or magnetic disc.

3.1.211 Fail-all simulator. All faults simulated one at a time in serial fashion (also known as a sequential simulator).

3.1.212 Fail soft. A non-specific condition of a system that has manifested a number of failures but still provides most of its functional capability.

3.1.213 Failed machine response. The output response of a failed UUT when a stimulus is applied.

3.1.214 Failure. The state of inability of an item to perform its required function. Failure is the functional manifestation of a fault.

3.1.215 Failure analysis. The logical, systematic examination of an item or its diagram(s) to identify and analyze the probability, causes, and consequences of potential and real failures.

3.1.216 Failure, castastrophic. Same as paragraph 3.1.88.

3.1.217 Failure coverage. The ratio of failures detected (by a test program or test procedure) to failure population, expressed as a percentage.

3.1.218 Failure, dependent. Same as paragraph 3.1.154.

3.1.219 Failure, independent. A failure which occurs without being related to the failure of associated items, distinguished from dependent failure.

3.1.220 Failure, intermittent. A failure which occurs randomly in time.

3.1.221 Failure mechanism. The physical, chemical, or other process which results in a failure.

3.1.222 Failure mode. The functional result of a fault.

3.1.223 Failure modes and effects analysis (FMEA). A procedure by which each potential failure mode in a system is analyzed to determine the results or effects thereof on the system and to classify each potential failure mode according to its severity.

3.1.224 Failure, non-critical. Any failure which results in degraded operation requiring special operating techniques or alternative modes of operation which could be tolerated throughout a mission but should be corrected immediately upon completion of mission.

3.1.225 Failure, nonrelevant. Failure to be excluded in interpreting test results or in calculating the value of a reliability characteristic.

3.1.226 Failure, partial. Failure resulting from deviations in characteristics beyond specified limits but not sufficient to cause a complete lack of function.

3.1.227 Failure population. Those failures which are used as a basis for the design and evaluation of tests.

3.1.228 Failure, relevant. Failure to be included in interpreting test results or in calculating the value of a reliability characteristic.

3.1.229 Failure, secondary. Same as paragraph 3.1.212.

3.1.230 Failure, soft. Same as paragraph 3.1.226.

3.1.231 Failure, transient. A temporary failure induced by a momentary or temporary external factor such as input power fluctuation, excessive ambient temperature excursion, electromagnetic interference, or by factors internal to a system.

3.1.232 Failure universe. The totality of failures being considered. If all these failures are detected, then 100% fault coverage has been achieved.

3.1.233 False alarm. A fault indicated by BIT or other monitoring circuitry where no fault exists.

3.1.234 False alarm rate. The number of false alarms per unit time or number of false alarms per BIT alarms expressed as a percentage.

3.1.235 Fault. A physical condition that causes a device, component, or element to fail to perform in a required manner; for example, a short-circuit or a broken wire.

3.1.236 Fault, catastrophic. Same as paragraph 3.1.89.

3.1.237 Fault class. The grouping of equivalent faults.

3.1.238 Fault, delay. Same as paragraph 3.1.151

3.1.239 Fault, design. Same as paragraph 3.1.158.

3.1.240 Fault detection. A process which discovers the existence of faults.

3.1.241 Fault detection time. The extent or duration of time during which the existence of a fault is not known; the elapsed time between fault occurrence and fault indication.

3.1.242 Fault dictionary. A list (usually created automatically by an ATPG system) containing each fault signature and the associated failed item (or one of a group of items) causing the fault signature to be developed by the test program and displayed by the ATE.

3.1.243 Fault, functional. A fault which can be described by a change in the operation of some portion of a system.

3.1.244 Fault, hard. Same as paragraph 3.1.235.

3.1.245 Fault indicator. A device which presents a visual display, audible alarm, or other indication, when a failure or marginal condition exists.

3.1.246 Fault, input. A fault at the input terminals of a UUT or components within the UUT.

3.1.247 Fault insertion. (1) Fault insertion, in the context of simulation, is a transformation which maps the original network (=the good machine) into a new network (=the faulty machine). (2) The process of inserting actual or simulated faults in a UUT for the purpose of demonstrating BIT or test program set (TPS) performance.

3.1.248 Fault, internal. A fault internal to an integrated component or device such as an integrated circuit.

3.1.249 Fault isolation. Isolating the fault in a UUT to the fault resolution level of the item.

3.1.250 Fault isolation time. A component of mean time to repair (MTTR); the time between detection and isolation of a fault.

3.1.251 Fault isolated replacable unit. The replaceable subsystem, assembly, subassembly or component identified through diagnostic testing of a UUT.

3.1.252 Fault latency time. The extent or duration of time during which the existence of a fault is not known; the elapsed time between fault occurrence and fault indication.

3.1.253 Fault list analysis. An analysis of faults prior to fault simulation. (Fault simulation is deduced by the propagation of fault lists on nodes of the primitive building block during a single pass simulation. The fault lists are calculated in Boolean arithmetic where the Boolean operators are specified by the primitive building blocks).

3.1.254 Fault localization. The process designed to identify the location of a fault known to exist within a general area of equipment. Fault localization may be less specific than fault isolation.

3.1.255 Fault masking. Equipment design which prevents complete unique fault isolation.

3.1.256 Fault, nondetectable. A fault that results in a nonrelevant failure.

3.1.257 Fault, open. A fault caused by an electrical separation of normal electronically-connected points.

3.1.258 Fault, out-of-tolerance. A defect or malfunction in a component, assembly or system in which a performance parameter approximates but falls outside the prescribed upper or lower limit for the parameter.

3.1.259 Fault resolution. How well the test program (or test procedure) can pin-point the failed item from among other items in the UUT.

3.1.260 Fault, probable. A hard or soft fault that is most likely to occur, relative to all possible faults within the UUT. It is caused by a component having a high failure rate.

3.1.261 Fault signature. Data developed by the test program and used by the ATE to indicate the ambiguity group.

3.1.262 Fault simulator. A computer program which inserts and studies simulated faults at the nodes of a represented digital circuit being exercised by test stimulus patterns. Also for analog, an analog circuit analysis program which simulates the effect of out-of-tolerance components.

3.1.263 Fault, soft. (1) A fault causing a degraded performance of the UUT. (2) A condition manifested only under certain conditions of UUT operation. When those conditions change the fault disappears.

3.1.264 Fault, stuck. A failure in which the digital signal is permanently held in one of its binary states.

3.1.265 Fault symptom. A measurable or visible abnormality in an equipment parameter.

3.1.266 Fault tolerance. The capacity of a system, or program to continue operation in the presence of specified faults.

3.1.267 Faults, equivalent. Same as paragraph 3.1.194.

3.1.268 Feedback. (1) The return of a portion of the output of a circuit or device to its input. (2) A timing signal used as a self-test feature in an automatic test system to verify that a control instruction has been executed before proceeding to the next control instruction.

3.1.269 Firmware. Hardware components which contain embedded software, such as EPROMS, Programmable Read Only Memory (PROMS), Read Only Memory (ROMS).

3.1.270 Fixed-logic levels. The characteristics of a digital ATE wherein the levels of the digital stimuli provided by the ATE cannot be changed.

3.1.271 Fixed point. A notation or system of arithmetic in which all numeric quantities are expressed by a predetermined number of digits with the decimal point implicitly located at some predetermined position.

3.1.272 Fixed-word length. Property of a storage device in which the capacity for bits in each storage word is fixed.

3.1.273 Flexible switching. Allows each device in a test system to connect to any pin on the output interfaces.

3.1.274 Floating point. A number representation in which the decimal point is automatically shifted and accounted for in order to extend the range of magnitude of numeric values which can be accommodated. The numbers are usually represented as one number multiplied by a base raised to a power.

3.1.275 Foreground or background. The capability to perform test development tasks concurrent with test execution.

3.1.276 Forward trace. The process of creating a sensitized path from the failure site to a primary output.

3.1.277 Functional fault. Same as paragraph 3.1.243.

3.1.278 Functional flowchart. A pictorial representation using programmer symbology to define the sequence of functional testing from initiation through completion.

3.1.279 Functional flow diagram. A diagram that represents the functional relationships among the parts of a system.

3.1.280 Functional item replacement (FIR). A functional module which is replaced at the intermediate maintenance level.

3.1.281 Functional model. A representative network containing several functional blocks of a UUT.

3.1.282 Functional modularity. The splitting of a system into parts or modules based on the function or purpose of these parts.

3.1.283 Functional partitioning. The physical or electrical separation of system or unit elements along interfaces which define and isolate these elements on the basis of function or purpose.

3.1.284 Functional test. A test which determines whether the UUT is functioning properly. The operational environment (such as stimuli and loads) can be either actual or simulated.

3.1.285 Functional test flow chart. A chart showing the sequential flow of the functional test sequences making up the total test.

3.1.286 Gate. A logic primitive element, such as an AND, OR, NAND, NOR, exclusive-OR, buffer or inverter device.

3.1.287 Gate level model. A modeling technique in which equivalents for high-level logic elements are constructed from basic gating elements.

3.1.288 General purpose electronic test equipment (GPETE). Test equipment containing the capability without modification, to generate, modify, or measure a range of parameters of electronic functions required to test two, or more prime equipments or systems of basically different design.

3.1.289 GPETE support item. The complement of equipment, supplemental to GPETE, which is necessary to facilitate a complete test measurement capability. This includes GPETE accessories, GPETE plug-ins and GPETE auxiliary items.

3.1.290 General purpose register. A register that may be used for arithmetic and logical operations, indexing, shifting, input, output, and general storage of temporary data.

3.1.291 General purpose test equipment. Test equipment which is used for the measurement of a range of parameters common to two or more equipments or systems of basically different design.

3.1.292 Global initialization algorithm. An algorithm that exercises all memory elements of a UUT to their limit.

3.1.293 Go/no-go test. A test designed to yield a "test pass" or "go" indication in the absence of faults in a UUT, and a "test fail" or "no-go" indication when fault(s) have been detected.

3.1.294 Good machine response. The output response of a failure-free UUT when a stimulus is applied.

3.1.295 Gray code. A sequence of input patterns in which exactly one bit changes state from one test step to the next.

3.1.296 Ground support equipment. All required external equipment (test equipment, tools, handling, storage, cooling, auxiliary power units, and so forth) which are required to support the operation and maintenance of a system.

3.1.297 Ground support equipment recommendation data. A document which reflects a contractor's recommendations for major items of ground support equipment for a specific end item. This document includes identification of testing requirements and is TMDE recommended to satisfy the requirements.

3.1.298 Guarding. The method by which the virtual common mode noise generator drives the guard connection of a digital multimeter, instead of the low side of the line, thereby reducing offset potential on the low side of a voltage source to be measured.

3.1.299 Guided probe system. A fault-isolating technique, in which the test program causes the ATE display to indicate where the test performer should affix the ATE's diagnostic probe on the UUT. The test program then analyzes the signal sensed by the probe and causes the ATE display to indicate where next to affix the probe. This process continues until the fault has been isolated to the best of the test program's capability.

3.1.300 Hard detect. Failures that can be positively detected.

3.1.301 Hard fault. Same as paragraph 3.1.235.

3.1.302 Hard-line. Any direct electrical connection between UUT and the testing device.

3.1.303 Hardware intensive. Applications in which the function is fixed and the application software or firmware is not expected to change or require a redevelopment of the application function itself, should a change be necessary.

3.1.304 Hardwire. To make permanent connections (such as soldered and wire-wrapped connections) between circuits; as contrasted with quick-disconnect connections (such as plug-in, threaded or twist-lock connections).

3.1.305 High order language. Same as paragraph 3.1.189.

3.1.306 Hold. (1) The function of retaining information in one storage device after transferring it to another device. (2) A designed stop in testing. (3) The function of storing information after it has been sampled (for example, sample and hold analog to digital converter).

3.1.307 Horizontal standardization. An item of test equipment used to perform a test function for several different systems.

3.1.308 Human interface module. Modules used in the test measurement or diagnostic equipment which provide information exchange between the operator and the machine.

3.1.309 Hybrid circuit. A circuit possessing both digital and analog signals.

3.1.310 Identification test. A test used to verify that the item about to be tested is the correct unit to test.

3.1.311 Impossible detects. Failures which can not be detected by any test sequence due to circuit redundancy or lack of test access.

3.1.312 In-circuit test. Tests of individual components within a circuit while guarding out the effects of surrounding components (analog) or over-riding (digital) inputs.

3.1.313 Information retrieval. The methods and procedures for recovering specific information from stored data.

3.1.314 Independent failure. Same as paragraph 3.1.219.

3.1.315 Inherent testability. A hardware testability design characteristic which does not include consideration of test stimulus and response data.

3.1.316 Initial certification only. Certification applied to items of precision measuring equipment (PME) which do not require periodic recalibration. The initial certification is sufficient unless components affecting calibration of the item are replaced.

3.1.317 Initial value. The value of the output of a system or element just prior to the time a stimulus is applied.

3.1.318 Initialize. To place an item into a known state.

3.1.319 Initiated BIT. Same as paragraph 3.1.71.

3.1.320 Input. (1) The path through which information is applied to any device. (2) The means for supplying information to a machine. (3) Information transferred from external storage to the internal storage of the machine. (4) The stimuli of a UUT.

3.1.321 Input fault. Same as paragraph 3.1.246.

3.1.322 Input skew. The application of test patterns one at a time to the input contacts of a digital UUT in order to prevent the ATE's stimulus application method from causing race hazards to occur in the UUT during testing.

3.1.323 Input test vector. A test bit pattern.

3.1.324 Instruction. A set of characters which define an operation, together with one or more addresses (or no address) and which, as a unit, cause the machine to operate accordingly on the indicated quantities. The term "instruction" is preferable to the terms "command" and "order": "command" is reserved for a specific portion of the instruction word or electronic signal; "order" is reserved for the order of the characters (implying sequence) or the order of the interpretation.

3.1.325 Instruction counter. A register in the central processing unit (CPU) that holds the address of the next instruction to be executed.

3.1.326 Instrumentation. All those devices (chemical, electrical, hydraulic, magnetic, mechanical, optical, pneumatic) utilized to test, observe, measure, monitor, alter, generate, record, calibrate, manage, or control physical properties, movements or other characteristics.

3.1.327 Integrated circuit subroutine. A subroutine in an ATPG computer program. The subroutine simulates the function of a particular integrated circuit.

3.1.328 Interface. Those physical and functional characteristics of an item which interoperate with the mateable or matchable characteristics of one or more other items to perform a combined joint operation.

3.1.329 Interface adapter. An item providing electronic, electrical and mechanical compatibility between the UUT and the test equipment.

3.1.330 Interface controller. Enables a computer to transmit and receive digital information for programming an instrument or peripheral.

3.1.331 Interface device. A device used to insure compatibility between UUT and adapter.

3.1.332 Interface testing. A type of on-line testing that requires disruption of the normal operation of the UUT.

3.1.333 Intermediate frequency. A frequency to which a signal is shifted locally as an intermediate step in transmission or reception.

3.1.334 Intermediate maintenance. Maintenance which is the responsibility of and performed by designated maintenance activities for direct support of the using organizations. Its phases normally consist of calibration, repair or replacement of damaged or unservicable parts, components or assemblies; the emergency manufacture of non-available parts and providing technical assistance to using organizations.

3.1.335 Intermittent failure. Same as paragraph 3.1.220.

3.1.336 Internal fault. Same as paragraph 3.1.248.

3.1.337 Internal storage. Storage facilities forming an integral part of the machine.

3.1.338 Interoperability. (1) The ability of systems, units or forces to provide services to and accept services from other systems, units or forces and to use the services so exchanged to enable them to operate effectively together. (2) The condition achieved among communication-electronics equipment when information or services can be exchanged directly and satisfactorily between them and their users. The degree of interoperability should be defined when referring to specific cases.

3.1.339 Interpreter. (1) A computer program which translates, then executes one-at-a-time, each instruction in the program. (2) A device which interprets and prints on a punched card the information punched onto the card.

3.1.340 Inverted-pyramid. Descriptive term characterizing a test or test technique whereby the smallest possible portions of hardware are tested first in the test sequence, and subsequent tests utilize previously verified hardware for execution. Also considered as the practice of using the widest test tolerances at system level testing, and the narrowest test tolerences at component or subassembly testing.

3.1.341 Jump. A programming instruction that conditionally or unconditionally specifies the location of the next instruction and directs the computer to that instruction to alter the normal sequence of the computer.

3.1.342 Keyboard. A device for the inputting of data by key depression which causes the generation of the selected code element.

3.1.343 Knowledge based test. A test based in part on previously acquired and stored information.

3.1.344 Known good board. A fault-free circuit board.

3.1.345 Learn mode testing. The utilization of random test patterns as stimuli for a circuit to produce a change in state at the output.

3.1.346 Level of repair analysis. A technique which establishes (1) whether an item should be repaired or discarded; (2) at what maintenance level, that is, organizational, intermediate, or depot.

3.1.347 Limit. The extreme of the designated range through which the measured value of characteristics may vary and still be considered acceptable.

3.1.348 Line replaceable unit (LRU). An item which is replaced at the organizational maintenance level.

3.1.349 Load. (1) To read information from cards, disc or tape into memory. (2) Building block or adapter providing a simulation of the normal termination characteristics of a UUT. (3) The effect that the test equipment has on UUT or vice versa.

3.1.350 Loading error. The error introduced when data are incorrectly transferred from one medium to another.

3.1.351 Local pin storage. Digital data stored in a memory element such as a shift register or random access memory (RAM) for each pin in a digital device used for clocking out data or reading in data at a predetermined rate.

3.1.352 Logic diagram. (1) A diagram representing the logic elements and their interconnections without necessarily expressing construction or engineering details. (2) A diagram that depicts the two-state device implementation of logic functions with logic symbols and supplementary notations, showing details of signal flow and control, but not necessarily the point-to-point wiring.

3.1.353 Logic value. A digital value of "1" or "0" (high or low state).

3.1.354 Low speed digital. Generating and receiving digital data at the computer recycle rate.

3.1.355 Machine. The CPU of a computer.

3.1.356 Machine code. An operation code that a machine is designed to recognize.

3.1.357 Machine instruction. An instruction that a machine can recognize and execute.

3.1.358 Machine language. The set of instructions in the number system which is intelligible to a specific machine (for example, a computer or class of computers). Such a language may include instructions which define and direct machine operations, and information to be recorded by or acted upon by these machine operations.

3.1.359 Maintainability. A characteristic of design and installation which is expressed as the probability that an item will be retained in or restored to a specified condition within a given period of time, when the maintenance is performed in accordance with prescribed procedures and resources.

3.1.360 Malfunction. Same as paragraph 3.1.235.

3.1.361 Manual check-out. A check-out system which relies completely on manual operation, operator decision, and evaluation of results.

3.1.362 Mask file. A file which is used to determine which measured values at a particular test step are valid or invalid.

3.1.363 Master test program set index. A reference system keyed by UUT identifier that contains a part number description of all the test program set (TPS) elements needed to execute a test program.

3.1.364 Mean time between failures. A measure of reliability giving the average time between failures.

3.1.365 Mean time to repair (MTTR). The arithmetic average of time required to complete a repair activity.

3.1.366 Measurement standard. A measuring instrument or artifact used as a reference to establish and maintain the accuracy of other measuring instruments or artifacts. Measurement standards may be used to calibrate other standards of lesser accuracy or to calibrate test and measuring equipment directly.

3.1.367 Measurement uncertainty. The range over which a measured value is expected to lie with a given probability.

3.1.368 Memory cycle. The time required to read information from memory and replace it.

3.1.369 Metrology. The science of measurement for determination of conformance to technical requirements including the development of standards and systems for absolute and relative measurements.

3.1.370 Minimum access code. A system of coding which minimizes the effect of delays for transfer of data or instructions between storage and other machine units.

3.1.371 Mission equipment. Any item which is a functional part of a system or subsystem and is required to perform mission operations.

3.1.372 Mnemonic code. An assembly level language which utilizes abbreviated terms which are intelligible to a specific processor for translation to machine code.

3.1.373 Mode code. A means by which the bus controller can communicate with the multiplex bus related hardware, in order to assist in the management of information flow.

3.1.374 Modem. A device that converts data from a form which is compatible with data processing equipment to a form that is compatible with transmission facilities and vice-versa.

3.1.375 Modular automatic test equipment (MATE) system. The complete complement of MATE management used in the acquisition of ATE. This includes MATE Standards, procedures, manuals and specifications; MATE Test Program Set; MATE Support Center and its disciplines; MATE hardware, software, human resources, training, technical data and facilities.

3.1.376 Modular software. A program structure implemented as independent functional sections to preclude extensive housekeeping in the accomodation of changes.

3.1.377 Module. A component, or a complete subassembly combined in a single package, that is designed to be removed and replaced easily for maintenance or repair.

3.1.378 Monitor. To check and measure selected parameters of an operating system.

3.1.379 Multiplex terminal. The electronic module necessary to interface the data bus with the subsystems. Terminals may exist as separate LRUs or be contained within the elements of the subsystems.

3.1.380 Multiplexer. A device used to channel an analog signal or digital logic from a selected node to an output.

3.1.381 Multiport ATE. An ATE system which contains more than two functional interfaces and shares a common set of test resources.

3.1.382 Negative test. A test for which the proper response to a stimuli is no response, such as a command deliberately formatted with a syntax error to check the accept or reject circuitry.

3.1.383 Net. A group of (I/O) nodes connected together.

3.1.384 Nibble. A four bit byte.

3.1.385 Node. The I/O of logic gates.

3.1.386 Nominal delay. The time the signals take to propagate through a logic element or even a wire. The effect of an input change to an element on the output will not occur until after the duration of nominal delay.

3.1.387 Noncritical failure. Same as paragraph 3.1.224.

3.1.388 Nondestructive storage. A storage medium from which information can be extracted without being erased.

3.1.389 Nondestructive testing. Testing of a nature which does not impair the usability of the item.

3.1.390 Nondetectable fault. Same as paragraph 3.1.256.

3.1.391 Nonerasable storage. A storage medium in which information cannot be erased.

3.1.392 Noninterference testing. A type of on-line testing that may be carried out during normal operation of the UUT without affecting the operation.

3.1.393 Nonrelevant failure. Same as paragraph 3.1.225.

3.1.394 Nonvolatile storage. A storage device which can retain information in the absence of power.

3.1.395 Normal mode noise. A combination of residual common mode noise and induced system noise.

3.1.396 Normal mode noise rejection. The inherent ability of an instrument to integrate a signal, thereby averaging out and reducing the effective normal mode noise.

3.1.397 Normalize. (1) To adjust the characteristic and fraction of a floating decimal point number thus eliminating leading zeros in the fraction. (2) To adjust a measured parameter to a value acceptable to an instrument or measurement technique.

3.1.398 Null. The condition of minimum output of a circuit as a function of some adjusting device.

3.1.399 Object code. A series of "1s" and "0s" (machine language code) that can be used by a computer directly.

3.1.400 Observability. An attribute of equipment design which defines or describes the extent to which signals of interest may be observed.

3.1.401 Off-line test equipment. Equipment used to perform tests on a UUT with the item removed from its normal operating environment.

3.1.402 Off-line testing. The testing of a UUT with the item removed from its normal operational environment.

3.1.403 On-line calibration. Calibration of ATE hardware through use of existing ATE assets which can be certified as; (1) within calibration; (2) providing test accuracy ratios of at least 10:1.

3.1.404 On-line test equipment. Equipment used to perform tests on a UUT while the item is in its normal operating environment.

3.1.405 On-line testing. The testing of the UUT in its operational environment.

3.1.406 On-off test. A test conducted by repeatedly switching on and off either the signal, power, or lead connected to the UUT while observing the reaction or performance of some parameter of that UUT. A test frequently used to isolate offending equipment while conducting compatibility, interference, or system performance evaluations.

3.1.407 Open fault. Same as paragraph 3.1.257.

3.1.408 Open subroutine. A subroutine that must be relocated and inserted into a routine at each place it is used. Contrast with subroutine, closed.

3.1.409 Operable equipment. Equipment which is operating within its specifications.

3.1.410 Operational assurance, fault isolation. Self-test program used on ATE.

3.1.411 Operational suitability. The degree to which a system can be satisfactorily operated in the field, with consideration being given to availability, safety, human factors, electromagnetic compatibility, logistic supportability, and training requirments.

3.1.412 Operational test and evaluation. Tests of the operational capability of an item, conducted in as realistic an operational environment as possible, then an evaluation of the test results including an estimate of the item's military utility, operational effectiveness and operational suitability. The evaluation is used in deciding whether or not to go into full production of the item.

3.1.413 Operational test progaram (OTP). The test program for a specific UUT or functionally related group of UUTs, in a medium designed for field use with the applicable ATE or TMDE, or both.

3.1.414 OTP instruction. The test program instruction as described in an OTP.

3.1.415 Organizational maintenance. Maintenance which is the responsibility of and performed by using organizations on its assigned equipment. Its phases normally consist of inspecting, servicing, lubricating, adjusting and the replacing of parts, minor assemblies and subassemblies.

3.1.416 Oscillation control. Oscillation control is a mechanism in simulators to inhibit potential and real oscillation which creates high circuit activity by limiting the number of times a signal line can change. A line which changes more than the preset number of times is set to the unknown state. Eventually, the circuit will stabilize with every line that was involved in the oscillating loop set to the unknown state.

3.1.417 Out-of-tolerance fault. Same as paragraph 3.1.258.

3.1.418 Output. (1) Current, voltage, power, pressure, flow, or any other driving force delivered by a circuit or device. (2) Terminals or other places where current, voltage, power, pressure, flow, or any other driving force may be delivered by a circuit or device. (3) In computers, information transferred from internal storage to external storage or other peripheral equipment.

3.1.419 Output interface. The output connection device in ATE that has all analog and digital signals transmitted through it for testing a UUT.

3.1.420 Output termination. To terminate the output of a UUT (such as a radio transmitter or receiver) with a dummy lead to simulate its normal operating environment.

3.1.421 Output test vector. An ordered set of simultaneously observed output values.

3.1.422 Overflow. The condition which arises when the result of an arithmetic operation exceeds the capacity of the storage space allotted in a memory device.

3.1.423 Overload. To exceed the rated capacity of an item.

3.1.424 Over-range. An input to a measuring device which exceeds in magnitude the capability of the selected range of that device.

3.1.425 Overshoot. The amount by which a pulse amplitude exceeds some set reference value after it has changed its state. Also, considered a distortion which occurs after a major pulse transistion.

3.1.426 Packing density. The number of units of useful information contained within a given linear dimension or within a given area.

3.1.427 Parallel fault simulation. The simultaneous simulation of two or more faults by the fault simulation program in an ATPG system.

3.1.428 Parametric tolerance testing. Testing a UUT's ability to function correctly when input parameters (for example, power supply voltages) are varied within specified limits.

3.1.429 Parity bit. An additional bit used in digital data transmission or memory to make the number of "1" bits it contains either odd or even as appropriate for a given application.

3.1.430 Parity check. An internal error self-check to determine whether an odd or even number of bits are present.

3.1.431 Partial failure. Same as paragraph 3.1.226.

3.1.432 Partition. To divide circuitry into easy-to-test sections.

3.1.433 Partitioning. The physical, functional or electrical separation of system or unit elements.

3.1.434 Passive BIT. Same as paragraph 3.1.72.

3.1.435 Passive test. A test conducted upon an un-energized UUT (also called cold test).

3.1.436 Passive sensor. (1) A sensor requiring no source of power other than the signal being measured. (2) A sensor that provides a signal after being stimulated by the UUT.

3.1.437 Patchboard. A device composed of a board containing a matrix of electrical terminals into which short interconnecting cables (patchcords) may be plugged in patterns to establish a selected circuit configuration for specific programs. To change the circuit configuration, one wired-up patchboard is removed and another wired-up patchboard is inserted.

3.1.438 Patchcord. An interconnecting cable for plugging or patching between terminals; commonly employed on patchboard, plugboard, and in maintenance operations.

3.1.439 Path sensitization. A process of creating a sensitized output path for fault-dependent test program generation.

3.1.440 Pattern generator. A procedure which generates input stimuli for a circuit.

3.1.441 Peculiar support equipment. Support equipment which is compatible with only one item.

3.1.442 Percent detect. Same as paragraph 3.1.217.

3.1.443 Performance monitoring. A process of continuously or periodically scanning a selected number of test points on a non-interferring basis to determine if the unit is operating within specified limits.

3.1.444 Performance standards. The established test parameters used to verify the expected performance of a UUT.

3.1.445 Performance test. A test which verifies if the UUT is performing properly.

3.1.446 Performance verification. Performance testing monitored by Government personnel to verify proper performance.

3.1.447 Periodic BIT. Same as paragraph 3.1.73.

3.1.448 Periodic check. A test or series of tests performed at designated intervals to determine if all elements of the UUT or test system are operating within their designated limits.

3.1.449 Personality card. A printed circuit card which is inserted in a test adapter to make the test adapter compatible with the I/O personality of a particular UUT.

3.1.450 Pickoff. A device that senses change to create a signal or to effect some type of control.

3.1.451 Pinboard. A programming or switching device composed of a removable or semipermanent board containing a matrix of holes or jacks into which short pins may be placed in patterns to establish a circuit configuration for specific programs or tests.

3.1.452 Pin electronics. An ATE architectural implementation envisioned to minimize system performance degradation due to cabling and interface constraints by including chip oriented test capability at each interface pin.

3.1.453 Pipeline processing. Pipeline processing refers to a simulation technique which allows new input vectors to be applied to a modeled circuit before the circuit has stabilized from the last input vector. This simulation technique is valuable when used in conjunction with dynamic tests which can exercise UUT's at their operating speeds typically in excess of 1 megahertz. Pipeline processing simulators usually employ a real time concept rather than an arbitrary unit time.

3.1.454 Plugboard. The same as patchboard but use is restricted to punched card machines.

3.1.455 Portability. The ability of test procedures to be used by more than one test equipment configuration.

3.1.456 Possible detect. Possible detect results when the unknown or indeterminate bits of a failed UUT response constitute the only difference from the response of a good UUT.

3.1.457 Postmortem. A routine that causes the information concerning the contents of all internal registers and storage locations to be printed in order to locate a mistake.

3.1.458 Potential fault detection. Same as fault detection except the outputs are such that the good output is "0" or "1" while the fault output is "X" (unknown).

3.1.459 Power or stimuli short test. A power or stimulus input check made to verify that the input is not operating into a short circuit.

3.1.460 Precision. A measure of consistency or repeatability of a set of measurements.

3.1.461 Precision measurement equipment (PME). Test and measurement equipment used to measure, calibrate, gauge, test, inspect, diagnose, or otherwise examine material, supplies, and equipment to determine whether they comply with the established specifications.

3.1.462 Pre-emptive control. An action or function which, by reason of pre-established priority, is able to seize or interrupt the process in progress and perform a process of higher priority.

3.1.463 Preferred items list. A listing of equipment which denotes the equipment considered the most advanced and acceptable, in its family, for military use (DA Pam 700-21).

3.1.464 Presence tests. Actions which verify the presence or absence of signals or characteristics. Such signals or characteristics are those which are not critical to the operating of the item within its tolerances.

3.1.465 Preset. To establish an initial condition or starting state.

3.1.466 Preshoot. A distortion which occurs prior to a major pulse transition.

3.1.467 Preventive maintenance. Tests, measurements, replacements, adjustments, repairs and similar activities carried out with the intention of preventing faults or malfunctions from occurring during subsequent operation. Preventive maintenance is designed to keep hardware and software in proper operating condition and may be performed on a scheduled basis.

3.1.468 Primary failure. Same as paragraph 3.1.219.

3.1.469 Primary I/O. The pins or connections of the UUT which provide only the power or signals necessary for proper operation.

3.1.470 Primitive model. The description of a UUT by primitives. It is actually a microfunctional model, which is one level higher than the gate-level model.

3.1.471 Primitives. The basic blocks or operators used by an ATPG system. There are several levels of primitives used by different ATPG systems. Some systems use combinational gates or Boolean operators only. Other systems include sequential elements such as latches, flip-flops, delay lines, and monostable in their primitive sets. Some systems consider counters, shift registers, ROM, and RAM as primitives. Primitives usually are handled as single blocks by interpretive subroutines.

3.1.472 Printed circuit board. A mounting of electrical components on which most connections are made by conductive circuit paths printed on the board.

3.1.473 Probable fault. Same as paragraph 3.1.260.

3.1.474 Problem oriented language. A language designed for the convenient solution of a given class of problems.

3.1.475 Procedure oriented language. A programming language designed for the convenient expression of procedures used in the solution of a wide class of problems.

3.1.476 Processor/post. A software tool which converts the output of a simulator into ATE source code.

3.1.477 Prognosis. The use of test data in the evaluation of a system or equipment for determining the potential of impending faults.

3.1.478 Programmable driver. A driver which insures (through programmability of voltage levels) compatibility with multi-logic families.

3.1.479 Programmable instrumentation. Test instruments that can be controlled automatically by an external device.

3.1.480 Programmable read only memory (PROM). A solid state memory storage device which is not programmed at the time of manufacture, but once programmed cannot be reprogrammed.

3.1.481 Programmable stimuli. Stimuli that can be controlled in accordance with instructions from a controlling device.

3.1.482 Programmable stimuli-generating instrument. An instrument whose stimuli-generating functions can be automatically controlled.

3.1.483 Programmer. A device having the function of controlling the timing and sequencing operation.

3.1.484 Programmer-comparator. A device which (1) reads commands and data from a sequential program usually on tape or cards. (2) Sets up delays, switching, stimuli, and performs measurements as directed by the program. (3) Compares the results of each measurement with fixed programmed tolerance limits to arrive at a decision.

3.1.485 Programming. The design, the writing, and testing of a program. It involves analyzing the problem, flowcharting, coding, debugging, and documentation.

3.1.486 Programming language. The language in which a computer program is written for processing by a computer.

3.1.487 Prototype. A development or first production model of an item.

3.1.488 Pseudo-code. An arbitrary code, independent of the hardware of a computer, which has the same general form as actual computer code but which must be translated into actual computer code if it is to direct the computer.

3.1.489 Pseudo-instruction. An instruction which resembles the instructions acceptable to the computer but which must be translated into actual computer instructions in order to control the computer.

3.1.490 Pseudo-random patterns. A repeatable sequence of digital patterns that has the appearance of being random.

3.1.491 Punch summary. A tape or card punch operating in conjunction with another machine to punch data which have been summarized or calculated by the other machine.

3.1.492 Quality assurance. Planned and systematic actions necessary to provide adequate confidence that a system or component will perform satisfactorily in service.

3.1.493 Quality assurance software. Computer programs used as test cases, simulators, validation and verification tools to certify the quality of operation or test computer programs.

3.1.494 Quantitative testing. Testing that monitors or measures the specific quantity, level or amplitude of a characteristic to evaluate the operation of an item. The outputs of such tests are presented as finite or quantitative values of the associated characteristics.

3.1.495 Quieting sensitivity. The level of a continuous wave input signal which will reduce the noise output level of a frequency modulation receiver by a specified amount, usually 20 decibels.

3.1.496 Race hazard. Close or simultaneous timing between signals that can result in erratic circuit operation.

3.1.497 Rack and stack. An ATE which relies on system integration of applicable units of test equipment.

3.1.498 Random access. Selection of any test point without regard to a fixed sequence.

3.1.499 Random access memory (RAM). A device that permits individual interrogation of any memory cell in a completely random sequence.

3.1.500 Random access programming. Programming without regard to the sequence required for access to the storage position called for in the program.

3.1.501 Random failure. Any failure whose occurrence is unpredictable in an absolute sense but which is predictable only in a probabilistic or statistical sense.

3.1.502 Range. (1) (Instrument) -- The range of values within which a measuring instrument is capable of measuring or which a generating instrument is capable of generating. (2) (Computing System) -- (a) The set of values that a quantity or function may assume. (b) The difference between the highest and the lowest values that a function may assume.

3.1.503 Rapid access loop. Internal memory machines in which a small section of memory has much faster accessibility than the remainder of the memory.

3.1.504 Read. To acquire information from some form of storage.

3.1.505 Read head. A sensor that converts information stored on punched tape, magnetic tape, magnetic drum, or other storage device, into electrical signals.

3.1.506 Read only memory (ROM). A solid-state memory storage device which is programmed upon manufacture and cannot be reprogrammed.

3.1.507 Readiness test. A test specifically designed to determine whether an equipment or system is operationally suitable for a mission.

3.1.508 Readout. (1) The device used to present output information to the operator, either in real time or as an output of a storage medium. (2) The act of reading, transmitting, displaying information either in real time or from an internal storage medium of an operator or an external storage medium or peripheral equipment.

3.1.509 Real time testing. Testing the UUT at its normal operating frequency and timing.

3.1.510 Recovery time. The time required for a signal to return to its rated value after a sudden change.

3.1.511 Redundant design. Alternate or parallel methods of performing a given test or function that are not necessary for system operation but are utilized when the primary function fails.

3.1.512 Reference quantity. A selected value of a parameter from which departure of similar parameters is measured.

3.1.513 Register. A device capable of storing a specified amount of data, such as one word.

3.1.514 Reliability. The probability that an item will perform its intended function for a specified period of time under stated conditions.

3.1.515 Remote access. Access pertaining to communication with a data processing facility by one or more stations that are distant from that facility.

3.1.516 Remote terminal. A terminal connected to the system by some telecommunication means.

3.1.517 Repair. The location and replacement of faulty parts on an item, including a successful functional test of the item.

3.1.518 Repeatability. The closeness of agreement among repeated measurements of the same variable under the same conditions.

3.1.519 Re-run point. One of a set of planned points in a program. If an error is detected between two such points, it is only necessary to go back to the re-run point in order to re-run the problem. All information pertinent to a re-run is available in standby storage during the whole time from one re-run point to the next.

3.1.520 Reserve. The setting aside of a specific portion of memory for storage area.

3.1.521 Reset. (1) To restore a register or counter to a prescribed state, usually zero. (2) To place a flip-flop in a zero state.

3.1.522 Residual frequency modulation. A measure of short term stability of an oscillator or synthesizer output and is usually expressed in hertz peak to peak.

3.1.523 Resolution. The ability to resolve a fault to the specific faulty item to be replaced.

3.1.524 Response. The reaction of a device to a stimulus.

3.1.525 Response time. The time required for a resulting condition to reach the steady state after variation of an input quantity.

3.1.526 Restart. To go back to a specific planned point in a routine.

3.1.527 Re-test OK (RTOK). The subsequent passing of a previously failed test.

3.1.528 Relevant failure. Same as paragraph 3.1.228.

3.1.529 Rise time. The time interval of the leading (trailing) edge between the instants at which the instantaneous value first reached the specified lower and upper limits (10% and 90%) of programmed or fixed output amplitude.

3.1.530 Rounding. A distortion appearing as a rounded feature and occurring at a point where a change of slope is expected or described.

3.1.531 Routine. (1) A set of coded instructions arranged in proper sequence to direct the machine to perform a desired operation or sequence of operations. (2) A subdivision of a program consisting of two or more instructions that are functionally related.

3.1.532 Run. A single continuous execution of a program or series of programs.

3.1.533 Run time performance verification. A software routine usually associated with third generation ATE which provides software adjustments of stimulus and response prior to test execution to assure test accuracy.

3.1.534 Run time variable. An application program condition in which the stimuli is varied under system control based on a measurement result.

3.1.535 Sampling. Obtaining the value of a variable at regular or irregular intervals.

3.1.536 Scale factor. A number used as a multiplier, chosen so that it will cause a set of quantities to fall within a given range of values.

3.1.537 Scanner. A device that sequentially samples a number of data points.

3.1.538 Schematic. A diagram which shows a symbol for each electrical and electronic part in the circuit and shows the electrical connections between post terminals. The part symbols are arranged in order of signal flow, with the circuit inputs at the left and the circuit outputs at the right.

3.1.539 Search. The scanning of information contained on a storage medium by comparing the information of each field with a predetermined standard until an identity is obtained.

3.1.540 Secondary failure. Same as paragraph 3.1.212.

3.1.541 Segment. Those portions of a test program that must be segmented due to core size limitations of the ATE used.

3.1.542 Self-calibration capability. The ability of an item to automatically monitor and adjust bias levels on itself with little or no operation intervention.

3.1.543 Self-test. A test or series of tests, performed by a device upon itself, which shows whether or not it is operating within designed limits. This includes test programs on computers and ATE performing functional and diagnostic tests.

3.1.544 Self-test adapter. An item used to replace the UUT during the self-test of an ATE.

3.1.545 Self-test capability. The ability of a device to check its own operation, expressed in terms of its ability to detect and possibly isolate faults.

3.1.546 Semi-automatic self-test. Self-test which, in order to achieve a higher level of accuracy or fault isolation than that achievable by automatic self test, requires human intervention to reach inaccessible test points or to employ external test equipment or standards, or both.

3.1.547 Semi-automatic test equipment. Any automatic testing device which requires human participation in the decision making control, or evaluative functions.

3.1.548 Sensitivity. A figure of merit that expresses the ability of a circuit or device to respond to an input quantity.

3.1.549 Sensitized path. A signal path conditioned so that a designated signal may propagate, unaffected by other states, to a primary output.

3.1.550 Sensor. A device that responds to a physical stimulus (such as heat, light, sound, pressure, magnetism, or motion) and transmits a resulting electrical signal for measurement or control.

3.1.551 Sequential access. A system for accessing data where all the data preceding the data of interest must be sequenced through in order to gain access to the data of interest.

3.1.552 Sequential control. Control from a program storage medium which must be read in a fixed order such as a tape (magnetic or punched) or a deck of punched cards.

3.1.553 Sequential programming. The programming of a device by which only one arithmetical or logical operation can be executed at one time.

3.1.554 Service routine. A routine in general support of the operation of a programmable machine (for example, an I/O diagnostic, tracing, or monitoring routine). Synonymous with utility routine.

3.1.555 Service test. A test of an item, system, material or technique conducted under simulated or actual operational conditions to determine whether the specified requirments or characteristics are satisfied.

3.1.556 Set. (1) A collection. (2) To place a storage device into a specified state, usually other than that denoting zero or blank. (3) To place a binary cell into the "1" state.

3.1.557 Shop replaceable assembly (SRA). An item which is designated to be removed or replaced upon failure from a higher level assembly in the shop (intermediate or depot maintenance activity), and is to be tested as a separate entity. Also called FIR.

3.1.558 Shop replaceable unit. Same as paragraph 3.1.557.

3.1.559 Signature analysis. A digital test approach which uses circuit-generated stimulus and synchronization and compresses the response data into a compact signature.

3.1.560 Signature diagnosis. The examination of the electronic signature of an equipment for deviation from known or expected characteristics and consequent determination of the nature and location of malfunctions.

3.1.561 Significance. The value or weight given to a position, or to a digit in a position, in a positional numeration system. In most positional numeration systems, positions are grouped in sequence of significance, usually more significant towards the left.

3.1.562 Simulation. The representation of the behavior of a physical or abstract system by the behavior of another system.

3.1.563 Simulator. (1) A device or program used for test purposes which simulates a desired system or condition to provide proper inputs and terminations for the equipment under test. (2) A software system which predicts output results derived from a UUT functional model and user generated input stimuli.

3.1.564 Skew. Same as paragraph 3.1.322.

3.1.565 Slave. A device that follows an order given by a master remote control.

3.1.566 Slew or slew rate. This is the time interval required for the driver to reach the programmed voltage level. Simply defined as the slope.

3.1.567 Slewing speed. A continuous speed, usually the maximum, at which a rotating device can approach a desired location.

3.1.568 Soft failure. Same as paragraph 3.1.226.

3.1.569 Soft fault. Same as paragraph 3.1.263.

3.1.570 Software. (1) All documentation associated with an ATE. (2) The totality of programs and routines used to extend the capabilities of ATEs.

3.1.571 Software intensive. Functions which are performed more by software than by hardware.

3.1.572 Software source documentation. Design and product specifications, source data flow charts, and descriptive data which shows how an ATE program is designed and operates its programming language, what it produces, and what it was designed for.

3.1.573 Software user documentation. Technical data instructing the operator of the test programs how to load, execute and evaluate the results or products of the programs.

3.1.574 Sort. To arrange data in accordance with a specific order.

3.1.575 Source code. The code in which a program is prepared. Generally a high order language code (such as BASIC, ATLAS, and so forth).

3.1.576 Special purpose electronic test equipment. Signal generating or signal measuring equipment which can only be used to test a specific electronic prime equipment.

3.1.577 Special purpose test equipment. Equipment which can only be used to test a specific prime equipment.

3.1.578 Special test equipment (STE). Equipment developed for the principal purpose of maintaining quality assurance of end items development and production. Some STE may be used for depot repair.

3.1.579 Spike. An asynchronous random pulse of short duration.

3.1.580 Spike analysis. Spike analysis makes use of a mechanism in a simulator with a more accurate timing model to detect a potential spike and set the signal value to unknown or potential error for that time interval.

3.1.581 Standard. Same as paragraph 3.1.366.

3.1.582 Standard test problem. An evaluation of the performance of a system, or any part of it, conducted by setting parameters into the system; the parameters are operated on and the results obtained from system readouts.

3.1.583 Static functional test. A test in which a measurement is made of the outputs of a UUT after, and only after, these outputs have stabilized with respect to a given input stimulus. Further, the measurement and assessment is made only with respect to the specific, overall action or purpose which the UUT is intended to perform or serve.

3.1.584 Static test. A test of a non-signal property (such as direct current voltage and current), of an equipment or of any of its constituent units, performed while the equipment is energized.

3.1.585 Stimulus. Any physical or electrical input applied to a device intended to produce a measurable response.

3.1.586 Storage. Any device into which information can be transferred, held, and later read out.

3.1.587 Storage buffer. A storage device used to compensate for a difference in rate of flow of information or time of occurrence of events when transmitting information from one device to another or within subsections of the same device.

3.1.588 Stuck fault. Same as paragraph 3.1.264.

3.1.589 Subprogram. A part of a larger program which can be converted into machine language independently.

3.1.590 Subroutine. A subprogram that may be used at more than one place in the program (such as, processing different sets of data in a common way).

3.1.591 Supplementary data. Information, text, schematics and logic diagrams necessary for analysis of the TPS and UUT in the event of a problem or anomaly during the testing process. The amount and content of the supplementary data is contingent upon the capability of the ATE to store and display required information automatically.

3.1.592 Support equipment. Equipment required to support the operation and maintenance of equipment.

3.1.593 Support software. Software which aids in preparing, analyzing, editing, and maintaining operational or test computer programs.

3.1.594 Support system. All related facilities, equipment, material, services and personnel required for operation and maintenance of a system, so that it can be considered a self-sufficient unit in its intended operational environment.

3.1.595 Support test system. A measurement system used to assess the quality of material which consists of the following elements: (1) test equipment; (2) ancillary equipment; (3) supporting documentation; (4) physical arrangement; (5) operating environment; and (6) operating personnel.

3.1.596 Switching. The act of manually, mechanically or electrically actuating a device for opening or closing an electrical circuit.

3.1.597 Switching card. A plug-in device which provides the necessary interconnection to the UUT.

3.1.598 Symbolic address. A label chosen to identify a particular word, function or other information in a routine, independent of the location of the information within the routine.

3.1.599 Symbolic logic. Exact reasoning about non-numerical relations using symbols that are efficient in calculation. One type of symbolic logic is Boolean algebra.

3.1.600 System. The composite of equipment, skills and techniques capable of performing or supporting (or both) an operational role.

3.1.601 System integrated test. Centralized monitoring and processing of fault data in one (or more) of the prime avionics equipments.

3.1.602 System life-cycle. Phases through which a system progresses from conception through disposal.

3.1.603 Systematic error. Any slight mismatch between the start channel and the stop channel amplifier rise time or fall times that causes a time error directly proportional to the trigger level error and inversely proportional to the signal slew rate at the trigger point.

3.1.604 Table driven simulator. A table driven simulator operates upon the topology of the circuit, rather than compiled code. The digital circuit is stored as a set of tables indicating the fan-in list, fan-out list, value, type of gate, and so forth.

3.1.605 Tag. A symbol, preferably mnemonic, identifying a specific memory location.

3.1.606 Tape block. A group of frames or tape lines.

3.1.607 Tape transport. A device which moves magnetic or punched tape past the tape reader. Reels for storage of the tape are usually provided.

3.1.608 Technical repair standard. A document which describes the UUT, tells how to test, fault-isolate, repair, and re-test the UUT.

3.1.609 Temporary storage. An area of working storage not reserved for one use only, but used by many sections of a program at different times.

3.1.610 Terminal. A point at which any element may be directly connected to one or more other elements. See paragraph 3.1.516.

3.1.611 Ternary simulator. A program which establishes a representation of a logic circuit or configuration based upon a computer-directed or processed simulation (or both,) of the logic circuit or configuration. Node points and output pins of the simulated circuit or configuration are permitted to take on three values; logical "1", logical "0", or "X" (unknown state) in sequences and along paths in accord with program rules, in order to derive fault-detection and fault isolation information for the logic circuit or configuration represented.

3.1.612 Test. A procedure or action taken to determine under real or simulated conditions the capabilities, limitations, characteristics, effectiveness, reliability or suitability of a material, device, system or method.

3.1.613 Test accuracy ratio. The ratio of measurement accuracy required by the unit to the measurement accuracy provided by the test instrumentation.

3.1.614 Test adapter. Same as paragraph 3.1.329.

3.1.615 Test analysis. The examination of the test results to determine whether the device is in a "go" or "no-go" state or to determine the reasons for or location of a malfunction.

3.1.616 Test bench. Equipment specifically designed to provide a suitable work surface for testing a unit in a particular test setup under controlled conditions.

3.1.617 Test chamber. An enclosure which is specifically designed to provide connectors, adapters, and stimulus for performing a test under a controlled environment.

3.1.618 Test comprehension. The ability of a test program to detect faults, expressed as a percentage of total faults.

3.1.619 Test diagram. An interconnecting diagram of the ATE and UUT interface, depicting the hookup and active signal lines required for enacting a test or group of tests.

3.1.620 Test equipment. Electric, electronic, mechanical, hydraulic, or pneumatic equipment (either automatic, manual, or any combination thereof) which is required to perform the checkout function.

3.1.621 Test fixture. An item providing electronic, electrical, and mechanical compatibility between the UUT and the test equipment. This item is usually associated with manually-controlled test equipment.

3.1.622 Test generation. The process of generating tests or test stimuli.

3.1.623 Test language. A particular test oriented language (BASIC, ATLAS, and so forth) utilizing english mnemonics that are commonly used in testing.

3.1.624 Test, measurement and diagnostic equipment (TMDE). Any system or device used to evaluate the operating condition of a system or equipment to identify or isolate (or both) any actual or potential malfunction.

3.1.625 TMDE register. A listing of TMDE technical descriptions of items for use in determining which proposed or fielded TMDE can be applied to fulfill the TMDE requirements of equipment programs, thus insuring maximum use of in-service assets and elimination of duplicate development or procurement of similar items of TMDE for different system applications (DA Pam 700-21).

3.1.626 Test pattern. (1) The pattern of logic states to be applied to the inputs of a digital UUT by a digital tester (usually automatic). (2) A stimulus design to exercise the UUT transfer function.

3.1.627 Test point. An electrical contact designed into a circuit specifically for the measurement of internal signals so as to increase the testability of the circuit.

3.1.628 Test point selector. A device capable of selecting test points on a UUT in accordance with instructions from the test program.

3.1.629 Test procedure. A document that describes step by step the operations required to test a specific item. A test procedure can be UUT-oriented or test equipment-oriented.

3.1.630 Test program. An aggregate of the test programs peculiar to an ATE or TMDE designed to accomplish the test function of a UUT automatically.

3.1.631 Test program instruction. An element of TPS which provides information required for testing which cannot be conveniently provided by the ATE under control of the test program.

3.1.632 Test program integration. The initial mating of an ATE, a TPS and a UUT to assure functional performance (debug).

3.1.633 Test program set (TPS). The combination of operational test program, operational test program instructions and interconnection device or signal conditioning circuitry that together allow an ATE/TMDE to perform the test necessary to check and diagnose a UUT.

3.1.634 TPS validation. The contractor testing of a UUT using the TPS developed for the UUT in order to validate that the TPS meets its contractual requirements.

3.1.635 TPS verification. The Government testing of a UUT using the TPS developed for the UUT in order to verify that the TPS meets its contractual requirements.

3.1.636 Test programming procedures. Documents which explain in detail the composition of test programs including definitions and logic used to compose the program. These procedures also provide instructions to implement changes in the program.

3.1.637 Test provisions. The capability included in the design for conveniently evaluating the performance of (and locating the faulty item in) a system, subsystem, set, group, unit, assembly, or subassembly.

3.1.638 Test requirement specification. A specification developed to establish contractual requirements for test documentation, TPSs, and test verification and validation.

3.1.639 Test requirements analysis. The examination of test requirements to determine adequacy, range of test stimuli, measurements, method of test (such as manual or automated), and type of test equipment.

3.1.640 Test requirements document. An item specification that contains the required performance characteristics of a UUT and specifies the test conditions, values (and allowable tolerances) of the stimuli, and associated responses needed to indicate a properly operating UUT. See MIL-STD-1345 or MIL-STD-1519.

3.1.641 Test sequence. The order in which tests or test patterns are run.

3.1.642 Test sequence number. Identification of a test sequence.

3.1.643 Test software. Same as paragraph 3.1.630.

3.1.644 Test specification. A document which specifies the values (and allowable tolerances) of the stimuli, and associated responses needed to indicate a properly operating UUT.

3.1.645 Test stand. An equipment specifically designed to provide suitable mountings, connections, and controls for testing electrical, mechanical, or hydraulic equipment as an entire system.

3.1.646 Test support software. Computer programs used to prepare, analyze, and maintain test software.

3.1.647 Test validation. A process in the production of a test program by which the correctness of the program is assured by running it on the ATE together with the UUT.

3.1.648 Test verification. The Government performance of a test in accordance with a test procedure to demonstrate that the test set-up (and the test procedure) covers the test requirements of the UUT.

3.1.649 Testability. A design characteristic which allows the status of a unit to be confidently determined in a timely fashion.

3.1.650 Testability measurement. A measurement of the ease and adequacy of testing derived as a result of demonstration or failed history analysis.

3.1.651 Testability prediction. A prediction of the ease and adequacy of testing developed through use of models or schematics (or both). The prediction is based on parameters (such as fault detection, fault isolation, and MTTR).

3.1.652 Threshold sensitivity. The smallest quantity that can be detected by an electronic item (such as a radio receiver, a measuring instrument, or an automatic control system).

3.1.653 Throughput. The measure of an ATE capability to process workload.

3.1.654 Tolerance. The total permissible deviation of a measurement from a designated value.

3.1.655 Tolerance cone. The specification of tighter test tolerances at the factory which gradually loosen at successive maintenance levels. The use of a tolerance cone tends to reduce CND and RTOK problems.

3.1.656 Traceability. The ability to relate individual measurement results to national standards or nationally accepted measurement systems through an unbroken chain of comparisons.

3.1.657 Traceability life. Historic testing documentation through the life of a unit.

3.1.658 Transient failure. Same as paragraph 3.1.231.

3.1.659 Translator. The general term for a program which converts a computer program from one language to another.

3.1.660 Trunk. A single circuit between two points, both of which are switching centers and individual distribution points.

3.1.661 Turn-on BIT. Same as paragraph 3.1.74.

3.1.662 Undershoot. The amount by which a pulse amplitude exceeds (negatively) some set reference value after it has changed its state. Also, considered a distortion which occurs after a major pulse transition.

3.1.663 Unit delay simulation. A digital logic simulation technique which assumes that the propagation delay time for all primitives is the same.

3.1.664 Unit under test (UUT). Any system, subsystem, group, unit, set, assembly, subassembly, and so forth, undergoing testing.

3.1.665 Unknown state. Most memory elements used in sequential circuits are bistable devices. When the power is turned on, they can assume either one of the two stable states. Because they are normally designed to have a symmetrical configuration, the initial states become unpredictable and are called unknown states. Unknown states can also be the result of critical races or oscillations.

3.1.666 Utility routine. Same as paragraph 3.1.554.

3.1.667 Utility software. Computer programs used for directory manipulation, memory management, disc I/O, test I/O, error message output, interrupt routines, and miscellaneous I/O.

3.1.668 Validation. The contractor's procedure for proving that the deliverable item meets its contractual requirements.

3.1.669 Variable delay simulation. A digital logic simulation technique which allows the user to fix the propagation delay time for each usage of a primitive element.

3.1.670 Verification. The Government's procedure for verifying that the deliverable item meets its contractual requirements.

3.1.671 Vertical standardization. The use of the same test procedure (or TPS) and associated test set-up (or ATE) at several support levels.

3.1.672 Volatile storage. A storage device in which stored data are lost when the applied power is removed.

3.1.673 Wait. A programmed instruction which causes an automatic test system to remain in a given state for a predetermined period.

3.1.674 Waveform digitizer. A third generation measurement instrument which contains sampling analog to digital converters and memory storage. Digitized waveform data is transmitted to a computer for processing by software algorithms (for example, fast fourier analysis).

3.1.675 Weapon replaceable assembly. A generic term which includes replaceable packages of a system installed in the weapon system with the exception of cables, mounting provisions, and fuse boxes or circuit breakers.

3.1.676 Wire data list. Tabular listing indicating point-to-point wire runs and connections of an interface adapter, UUT or other device.

3.1.677 Word. A number of bits, either constant or variable, normally treated as a single item of information by the program.

3.1.678 Word length. The number of bits in a digital word. In a given machine, the number may be constant or variable.

3.1.679 Wrap-around test. Self-test of an ATE system accomplished by connecting the system's stimuli outputs to its response monitor inputs, usually through a self-test adapter.

3.1.680 Write. To introduce information usually into some form of storage or onto some form of output medium.

3.1.681 Zero delay simulation. A digital logic simulation technique which assumes that all circuit devices have no propagation delay.

4. GENERAL REQUIREMENTS

4.1 Not applicable.

5. DETAIL REQUIREMENTS

5.1 Not applicable.

6. NOTES

6.1 Changes from Previous Issue. The extent of changes, deletions, additions, and so forth preclude the annotation of the individual changes from the previous issue of this document.

Preparing Activity:

Navy - EC
(Project ATTS-0002)

Custodians:
Army-CR
Navy-EC
Air Force-99

Review Activities:

Army-MI
Navy-AS, MC
Air Force-11

User Activities:

Army-ME
Navy-CG, OS, SH, YD

APPENDIX A

ACRONYMS

ATE	Automatic Test Equipment
ATG	Automatic Test Generator
ATLAS	Abbreviated Test Language for All Systems
ATPG	Automatic Test Program Generator
BASIC	Beginners All-purpose Symbolic Instruction Code
BIT	Built-In Test
CND	Cannot Duplicate
CPU	Central Processing Unit
EPROM	Erasable Programmable Read Only Memory
FMEA	Failure Modes and Effects Analysis
FIR	Functional Item Replacement
GPETE	General Purpose Electronic Test Equipment
I/O	Input/Output
LRU	Line Replaceable Unit
MATE	Modular Automatic Test Equipment
MTTR	Mean Time To Repair
OTP	Operational Test Program
PME	Precision Measurement Equipment
PROM	Programmable Read Only Memory
RAM	Random Access Memory
ROM	Read Only Memory
RTOK	Re-Test OK
SRA	Shop Replaceable Assembly
STE	Special Test Equipment
TMDE	Test, Measurement and Diagnostic Equipment
TPS	Test Program Set
UUT	Unit Under Test

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