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MILITARY STANDARD

CERTIFICATION REQUIREMENTS FOR JAN SEMICONDUCTOR DEVICES

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FOREWORD

1. This military standard is approved for use by all Departments and Agencies of the Department of Defense.

2. Beneficial comments (recommendations, additions, deletions) and any pertinent data which may be of use in improving this document should be addressed to: NASA Parts Project Office, ATTN: Code 311.A, NASA/Goddard Space Flight Center, Greenbelt, MD 20771, by using the Standardization Document Improvement Proposal (DD Form 1426) appearing at the end of this document or by letter.

3. The purpose of this standard is to establish requirements and criteria for certification (as required by MIL-S-19500). Definite criteria will assure that semiconductors are manufactured under conditions which have been demonstrated to be capable of continuously producing highly reliable products. This is accomplished by evaluating the manufacturer's capability for attaining statistical control of critical parameters and continuous improvement of process capability. Certification and the maintenance thereof is a prerequisite to semiconductor qualification and is performed in advance and independent of acquisition.

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1. SCOPE

1.1 Scope. This standard establishes the minimum requirements for the certification of manufacturing facilities/lines(s) used in fabricating, assembling, and testing high reliability JAN semiconductors in accordance with MIL-S-19500. This includes plant facilities, equipment, materials, personnel training, process controls, testing, and documentation.

2. APPLICABLE DOCUMENTS

2.1 Government documents.

2.1.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DODISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

MILITARY

MIL-S-19500	-	Semiconductor Devices, General Specification for.

STANDARDS

MILITARY

MIL-STD-750	-	Test Methods for Semiconductor Devices.
MIL-STD-1686	-	Electrostatic Discharge Control Program for Protection of Electrical and Electronic Parts, Assemblies and Equipment (Excluding Electrically Initiated Explosive Devices) (Metric).
MIL-STD-45662	-	Calibration Systems Requirements.

HANDBOOKS

MILITARY

DOD-HDBK-263	-	Electrostatic Discharge Control Handbook for Protection of Electrical and Electronic Parts, Assemblies and Equipment (Excluding Electrically Initiated Explosive Devices) Metric.
MIL-HDBK-279	-	Total-Dose Hardness Assurance Guidelines for Semiconductor Devices and Microcircuits.
MIL-HDBK-280	-	Neutron Hardness Assurance Guidelines for Semiconductor Devices and Microcircuits.

(Unless otherwise indicated, copies of federal and military specifications, standards, and handbooks are available from the Standardization Documents Order Desk, Building 4D, 700 Robbins Avenue, Philadelphia, PA 19111-5094.)

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents which are DoD adopted are those listed in the issue of the DODISS cited in the solicitation. Unless otherwise specified, the issues of documents not listed in the DODISS are the issues of the documents cited in the solicitation.

AMERICAN SOCIETY FOR TESTING AND MATERIALS (ASTM)

ASTM F34-76	-	Standard Test Method for Liquid Extraction of Flexible Barrier Materials.
ASTM F42-88	-	Standard Test Method for Conductivity Type of Extrinsic Semiconducting Materials.
ASTM F43-88	-	Standard Test Method for Resistivity of Semiconductor Materials.
ASTM F47-88	-	Standard Test Method for Crystallographic Perfection of Silicon by Preferential Etch Techniques.

ASTM F80-88 - Standard Test Method for Crystallographic Perfection of Epitaxial Deposits of Silicon by Etching Techniques.
ASTM F81-89 - Standard Test Method for Measuring Radial Resistivity Variation on Silicon Slices.
ASTM F120-88 - Standard Practices for Determination of the Concentration of Impurities in Single Crystal Semiconductor Materials by Infrared Absorption Spectroscopy.
ASTM F121-83 - Interstitial Atomic Oxygen Content of Silicon by Infrared Absorption, Test Method for.
ASTM F123-86 - Standard Test Method for Substitutional Atomic Carbon Content of Silicon by Infrared Absorption.
ASTM F416-88 - Standard Test Method for Detection of Oxidation Induced Defects in Polished Silicon Wafers.
ASTM F533-88 - Standard Test Method for Thickness and Thickness Variation of Silicon Slices.
ASTM F613-87 - Standard Test Method for Measuring Diameter of Silicon Slices and Wafers.
ASTM F657-87 - Standard Test Method for Measuring Warp and Total Thickness Variation on Silicon Wafers by Noncontact Scanning.
ASTM F671-89 - Standard Test Method for Measuring Flat Length on Slices of Electronic Materials.
ASTM F673-90 - Standard Test Methods for Measuring Resistivity of Semiconductor Slices or Sheet Resistance of Semiconductor Films with a Noncontact Eddy-Current Gage.
ASTM F847-87 - Standard Test Method for Measuring Crystallographic Orientation of Flats on Single Crystal Silicon Slices and Wafers by X-ray Techniques.

(Application for copies should be addressed to the American Society for Testing and Materials (ASTM), 1916 Race Street, Philadelphia, PA 19103.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

2.3 Order of precedence. In the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. DEFINITIONS

3.1 Definitions. In addition to the definitions specified in MIL-S-19500, the following definitions apply:

3.1.1 Certification. The process by which a qualifying activity or certification team determines on the basis of a survey that a manufacturer's facility(ies)/lines are capable of meeting the applicable requirements so that the manufacturer is eligible to qualify products manufactured on those facilities/lines. The written notification of such eligibility constitutes certification.

3.1.2 Certification team. The Government qualifying activity's designated representative(s) charged with the responsibility of auditing a manufacturer's facility/line.

3.1.3 Facility. Equipment, documentation, and services used to support the manufacture, assembly, testing, and shipping of semiconductors.

3.1.4 Semiconductor technology. A group of semiconductors which are manufactured on the same line using the same materials, procedures, and similar equipment (see MIL-S-19500).

3.1.5 Line. A collection of designated wafer fabrication, assembly, test equipment, and organizational structure used to manufacture semiconductors in accordance with specific process flow.

4. GENERAL REQUIREMENTS

4.1 Requirements. The following requirements are applicable for the certification of product assurance levels for JAN semiconductors as specified in MIL-S-19500. The qualifying activity shall determine the adequacy and compliance to the requirements and shall report their findings and recommendations to the manufacturer.

4.1.1 Pre-audit information submission. The manufacturer shall submit to the qualifying activity the information required in 4.1.1.1 through 4.1.1.13 for review and comment prior to an audit. At least one JAN product, which is intended for manufacture on each line to be certified for each particular process, shall be identified. A pre-audit information letter shall be issued by the qualifying activity to the manufacturer under consideration for certification. Additional items may be requested by the qualifying activity, however, the primary pre-audit information is listed below:

4.1.1.1 Quality assurance program plan. The plan shall be in accordance with and cross-referenced to the applicable paragraphs of MIL-S-19500, appendix D. The manufacturer's flowchart for the line must be complete, current, and accurate, and shall contain as a minimum, the type of information as shown in the example on figure 1 for all processes to be certified.

4.1.1.1.1 Process flowcharts and lot travelers. Process flowcharts (e.g., see figure 1) and lot travelers, as required by the qualifying activity, shall be submitted for wafer fabrication, assembly, screening, and groups A, B, C, D and E (if applicable) tests. The manufacturer's flowchart for each line to be certified must comply with the requirements of MIL-S-19500, appendix D. Lot travelers may be used in lieu of flowcharts if the lot travelers contain the required flowchart information.

4.1.1.2 Calibration information.

4.1.1.2.1 Calibration system description. The system description shall be in accordance with and cross-referenced to MIL-STD-45662 requirements.

4.1.1.2.2 Calibration facilities list. The list shall include names and addresses of all calibration laboratories utilized. The test laboratory must verify that the calibration laboratories utilized are, in fact, capable of performing the required services (see MIL-STD-45662).

4.1.1.3 Test procedures. All test procedures for which laboratory suitability is to be issued by the qualifying activity shall be cross-referenced to the applicable MIL-STD-750 test methods and submitted. If the quality control personnel use a different document(s) than the manufacturing personnel, both sets of documents shall be cross-referenced to the applicable MIL-STD-750 test methods.

4.1.1.4 Testing information. The following test information shall be made available to the qualifying activity:

4.1.1.4.1 Test equipment suitability. The manufacturer shall have a documented system in operation which assures the suitability of equipment and associated calibration standards used for the screening, qualification, and quality conformance inspections.

4.1.1.5 Verification procedure documentation. The manufacturer shall supply, as required by the qualifying activity, the procedures which are used internally to verify that the electrical test programs, switching and special schematics, and burn-in schematics are in accordance with the specification requirements.

4.1.1.6 Audit baseline sheet (design and construction information). Audit baseline sheet shall be current and complete for each line and technology for which the manufacturer is seeking certification. This shall be verified prior to the certification audit (see figure 2).

4.1.1.7 Quality conformance inspection (QCI). A documented QCI procedure shall be submitted which includes a sample selection process and notification of lot failure.

4.1.1.8 Electrostatic discharge (ESD) control. A documented ESD handling and control procedure in accordance with 5.1.11 shall be submitted.

4.1.1.9 Self-audit. A documented self-audit procedure in accordance with MIL-S-19500, appendix D shall be submitted. A guide for a self-audit checklist may be obtained from the qualifying activity.

4.1.1.10 Distributor audits. When applicable, a documented distributor audit procedure in accordance with MIL-S-19500, appendix D shall be submitted. The procedure shall contain provisions for ESD handling, repackaging, storage, and product retest.

4.1.1.11 Current density. For each different product line, facility, or technology to be certified, a current density calculation procedure in accordance with the internal conductors paragraph of MIL-S-19500 shall be submitted.

4.1.1.12 Radiation hardness assurance (RHA) program. When applicable, a documented RHA program plan in accordance with 5.2.18 shall be submitted.

4.1.2 Manufacturer audit. The qualifying activity shall audit the manufacturer's facility(ies) and line(s). The purpose of the audit is to determine that the controls imposed on manufacturing, inspection, and testing of JAN semiconductors are sufficient to assure conformance with the requirements of MIL-S-19500 and this standard.

4.1.2.1 Capability demonstration. Evidence shall be shown to the qualifying activity during the audit that the certification requirements herein are being regularly met in production. The manufacturer shall provide (or make available for review during the audit of each line) representative sample(s), data, and documentation as required.

4.1.2.2 Audit report. The qualifying activity will report the results of the audit to the manufacturer.

4.1.3 Certification. Certification is valid until terminated by written notification from the qualifying activity. Throughout the duration of the certification, the manufacturer is subject to a periodic reaudit approximately every two years and a more frequent review by the qualifying activity or its representatives.

4.1.3.1 Loss of certification. The manufacturer may lose certification for failing to comply with the requirements of MIL-S-19500 or this standard.

4.1.3.2 Reinstatement of certification. Manufacturers may have certification reinstated by successfully completing all the requirements referred to in MIL-S-19500 and this standard, or such portions thereof as the qualifying activity may direct in order to remedy the deficiencies leading to the loss.

5. DETAILED REQUIREMENTS

5.1 System requirements. In addition to section 4, the manufacturer shall document, control, and meet the following:

5.1.1 Documentation. Documents which specify materials, calibration techniques, processing, tests and measurements, controls, and procedures shall be maintained in accordance with appendix D of MIL-S-19500. These documents shall cover all process steps to be certified. The documentation shall be readily available to the operating personnel at all times. It shall be made available to the qualifying activity for the purpose of verifying its existence, coverage, implementation, and adequacy.

5.1.1.1 Lot traveler. A lot traveler shall be used for each lot, sublot, or split. The lot travelers shall include as the minimum: Lot identification, operation, identification of critical equipment when an equipment option is available (JAN S only), quantity in and out, date of operation, PDA (when applicable), and unique operator identification. In addition, the test lot traveler shall be in accordance with MIL-S-19500, appendix D.

5.1.1.1.1 Wafer lot acceptance for JAN S. A form which contains the data required by the "Wafer lot inspection" paragraph of MIL-S-19500 shall be utilized for each wafer lot.

5.1.1.2 Statistical process control (SPC) program. The manufacturer's SPC program per the "Process control charts" paragraph of appendix D of MIL-S-19500, shall be documented and available for review by the qualifying activity during the audit. A planned SPC milestone schedule and progress reporting system shall be developed and made available for review.

5.1.1.2.1 SPC tools. SPC tools, which are used to summarize data and to aid in the SPC analysis of a given manufacturing process, shall be maintained at operations where inspections or measurements are performed (e.g., dimensions, strengths, thicknesses, resistivity). Examples of SPC tools shall include, but are not limited to, the following: Histograms, pareto analyses, scatter plots, check sheets, control charts, cusum charts, and cause and effect diagrams. Where control limits (trends), absolute specification or baselined limits are exceeded, the manufacturer shall document the product disposition and corrective action taken. If absolute specification or baselined limits are exceeded (other than rework allowed by MIL-S-19500), the product must be dispositioned as non-JAN. The records of SPC tools shall be readily available during the audit.

5.1.1.3 Equipment maintenance and calibration. The procedures, records, and calibration facility location for the performance of preventative maintenance and recalibration (including recall cycle) and repairs shall be specified in accordance with MIL-S-19500, appendix D.

5.1.2 Control of incoming materials. Control of incoming materials shall be accomplished using one of the following:

5.1.2.1 Incoming inspection. Methods and procedures used to control inspection, storage, and handling of incoming materials shall be documented. Records shall be provided which verify that materials used in production meet the requirements of the manufacturer's specifications and of the general and detail MIL-S-19500 specifications. As an example the following items shall be covered:

5.1.2.1.1 Substrate. Thickness, flatness, surface orientation, conductivity type, resistivity, visual examination, surface quality after defect etch, and oxygen and carbon content.

5.1.2.1.2 Bond wire. Composition, uniformity, hardness, diameter, elongation, tensile strength, and purity.

5.1.2.1.3 Metal. Composition and purity.

5.1.2.1.4 Package material and lead frames. Dimensions, composition, lead integrity test, material purity, plating, underplating, and tolerances where applicable.

5.1.2.1.5 Chemicals, photoresists, and gases. Composition, purity, and grades.

5.1.2.1.6 Masks. Geometry (lines, gaps, tolerances), pinholes (density, size, distribution), scratches, edge raggedness, and level overlay.

5.1.2.2 Vendor quality system certification. As an alternative to the requirements of 5.1.2.1, the vendor quality system certification may be used to ensure the quality of incoming supplies. This system requires validation of the vendor's quality system, staff capabilities, equipment controls, facilities, and record procedures. This method may replace the semiconductor manufacturer's incoming inspection. It shall consist of, as a minimum, the evaluation of the vendor's inspection data, process control statistics, and calibration records, including a correlation of the vendor's measurements to the semiconductor manufacturer's incoming inspection procedures. Semiconductor manufacturers shall periodically verify the vendor's quality system. This shall include random measurements to verify correlation, periodic vendor facility audits, and receipt of certificate of analysis or certificate of compliance.

All aspects of the program shall be documented, including methods, criteria, and evaluation or audit procedures. Both parties shall maintain records to verify that the incoming material consistently meets the requirements of the semiconductor manufacturer's specifications.

The vendor is defined as all suppliers or manufacturers of incoming supplies to the semiconductor manufacturer. In the case of more than one vendor, for example, a manufacturer and a packager, both must be certified. Supplies include, but are not limited to, package piece parts including bonding wires and preforms, chemicals, masks, gases, and silicon.

If, in the course of audits or monitors, inadequacies are found that jeopardize the efficiency of the program, the semiconductor manufacturer shall revert to incoming inspections until corrective actions are implemented. All materials used prior to the inadequacies being found shall be documented and dispositioned.

5.1.3 Calibration. Calibration shall be in accordance with MIL-STD-45662. Certificates showing traceability to the National Institute of Standards and Technology (NIST) are to be maintained current at the manufacturer's plant and available at the time of audit.

5.1.4 Environmental control. Specify, control, and record the relative humidity, temperature, and particle count for each critical process step (e.g., wafer fabrication, assembly). The procedures and techniques for measuring these environmental parameters and limits shall be documented. The procedures shall contain corrective actions for out-of-tolerance environmental conditions. Particle counts shall be in accordance with the "Control during manufacturing and assembly" paragraph of appendix D of MIL-S-19500.

5.1.5 Deionized water control. Specify, measure, control, and record the purity of water in terms of: Minimum resistivity (control and absolute specifications limits) at 25°C, maximum total organic carbon (TOC), maximum bacteria count, maximum total dissolved silica, maximum particulates, and maximum residue.

5.1.6 Electrical testing for JAN semiconductors.

5.1.6.1 Hardware. All electrical test equipment and fixtures used for testing JAN semiconductors shall be suitable to meet applicable test conditions. Setup, operation, and verification procedures for each operation/equipment shall be made available during the audit. Test equipment shall be verified in accordance with the "Electrical test equipment verification" paragraph of MIL-S-19500.

5.1.6.2 Programs and tapes. Test programs and corresponding tapes shall meet the requirements of the detail semiconductor specifications. A system shall be documented which ensures that, if a specification is revised, the corresponding program(s) and tape(s) are also changed, and that the correct program is used.

5.1.7 Environmental testing for JAN semiconductors. All environmental test equipment and fixtures used for testing JAN semiconductors shall be suitable to meet applicable test conditions. Setup and operation procedures for each operation/equipment shall be made available for determination of adequacy.

5.1.8 Failure analysis. Failure analysis and corrective actions shall be performed and documented in accordance with MIL-S-19500.

5.1.9 Handling of wafers, substrates, and tools. Provisions shall be made for the careful handling of wafers, substrates, tools, fixtures, etc. used in the production cycle to prevent damage and contamination.

5.1.10 Training. Procedures and records of training for operators and inspectors shall be made available for review by the qualifying activity and shall be in accordance with MIL-S-19500, appendix D.

5.1.11 Electrostatic discharge (ESD) control program. The ESD control program procedure shall be documented and implemented in accordance with MIL-S-19500, and appendix D of MIL-S-19500. The ESD control program shall be made available to the qualifying activity.

The ESD control program shall incorporate failure analysis feedback. The manufacturer shall be responsible for assuring that its distributors implement and maintain ESD controls.

Definitions specified in the ESD control program shall be in accordance with MIL-S-19500 and DOD-HDBK-263 as applicable. DOD-HDBK-263 and DOD-STD-1686 are recommended as guides in establishing the ESD control program.

5.2 JANTX and JANTXV line requirements. The following processes shall be documented and controlled, including accept/reject criteria, and are applicable to the certification of a line on which the manufacturer intends to produce any or all levels of JAN semiconductors. Additionally, the manufacturer must meet the requirements of sections 4 and 5.1 of this standard.

5.2.1 Oxidation and deposition. Each combination of materials formed on the substrate or wafer shall be identified and the methods of formation (thermal oxidation, sputtering, etc.) shall be specified. Equipment, thickness, and tolerances shall be specified and controlled.

5.2.2 Patterning. Techniques (photolithography, beam) and materials used to form patterns shall be specified.

5.2.2.1 Photoresist. The following shall be specified: Preparation and evaluation (specific gravity, viscosity, solids residue, definition of line width, pinhole count), storage conditions (temperature, time, type of container), application (humidity control, rpm of spinner, acceleration, spin time), pre-bake and bake (time, temperature, environment), development (cycle times, temperature, chemicals), and removal. If the photoresist thickness is measured, rpm of spinner, acceleration, and spin time need not be specified.

5.2.2.2 Etching. The controls and tolerances on each patterning process shall be specified for each technique (wet chemical etch, dry plasma etch, etc.). For wet etch methods, the etchant information shall include: Composition, grade, concentration, frequency of etchant replacement, temperature, etch rate and uniformity and time of each oxide or metal layer agitation, and method of drying. For dry etch methods the etchant information shall include: Gas composition, chamber pressure, forward RF power, limit on reflection power, electrode temperature, and a procedure for monitoring etch rate uniformity.

5.2.2.3 Alignment and exposure. Contact print parameters shall be specified as: Exposure (uniformity, contact pressure, wavelength, light intensity, time, environment) and visual inspection (magnification, lighting, visual aids). Projection print parameters shall include: Scan, aperture, focus (microns from center allowable), distortion, intensity, uniformity, and wavelength.

5.2.3 In-line epitaxy. Techniques, controls, materials, and equipment used in forming an epitaxial layer on a substrate shall be specified. This shall include temperature, cycle times, sheet resistivity of epitaxial layer, thickness of epitaxial layer, gas flow rates, loading and unloading of wafers (dust removal, wafer placement on susceptor), wafer precleaning, and susceptor and tube cleaning. Instruments used for temperature measurement shall be calibrated.

5.2.4 Structure formation. Techniques and materials used in forming junctions and MOS gates shall be identified.

5.2.4.1 Diffusion. Diffusion temperature measurements including tolerances, profiling techniques, diffusion tube and associated handling hardware cleaning frequency and techniques, flow rate of gases, wafer loading and unloading, storage, calibration of thermocouples, and dopant source (grade, type, etc.) shall be specified when applicable.

5.2.4.2 Ion implantation. Dopant source, power supplies and vacuum equipment, frequency and cleaning techniques of the entire system, and wafer loading and unloading, shall be specified.

5.2.4.3 Test structures (active devices, control wafers, coupons, etc.). Test results shall be made available on critical parameters (e.g., Beta, breakdown voltages, threshold voltages, leakage current, or others as applicable). These results shall show the control or specification limits, frequency of test, and type of record.

5.2.5 Metallization. Equipment for depositing metal, composition of each metal layer, method (vacuum chamber electroplating, sputtering, etc.), heat source (E-beam, filament, etc.), temperature of substrate during deposition, metal thickness and tolerance, deposition rate of metal, motion (stationary, rotary, or planetary), cleaning of chamber, thickness control, weight of melt, and sintering (time, temperature, ambient gas) shall be specified.

5.2.6 CV plotting. The techniques, equipment, frequency of test, test conditions (time, temperature, bias, etc.), and control or specification limits shall be specified as required.

5.2.7 Glassivation. The method of formation (oxidation of silicon, quartz sputtering, etc.), and the materials used shall be identified. The controls for the glassivation layer(s) shall be documented and include temperature, time, thickness, flow rate of gases, motion of wafer during deposition, control of power and frequency, and dopant concentration.

5.2.8 Wafer thinning. Techniques, methods of removal (lapping, etching, etc.), and materials used in reducing wafer thickness shall be specified. Pressure, grit size, speed of rotation, removal of coating, cleaning, front side protection, taper, thickness, tolerances, and other pertinent parameters shall also be specified.

5.2.9 Scribing. Each method (diamond, laser, sawing, etc.) of scribing shall be specified.

5.2.9.1 Diamond. The type of machine, scribing tool, tool point (e.g., heel), tool angle, tool pressure, speed and direction of tool travel, depth of scribe line, orientation of die pattern, use of oxide and metal free channels, and debris removal shall be specified.

5.2.9.2 Laser. The type of equipment, power, beam resolution, depth of scribe line, cleaning, protective overcoat, and pulse rate shall be specified.

5.2.9.3 Sawing. The wafer feed rate limits, wheel thickness, slurry, washing, and kerf depth shall be specified.

5.2.10 Die separation. Each method of die separation to be certified shall be specified. Additionally, the method of storing sorted die shall be specified.

5.2.10.1 Roller. Wafer protection, roller diameter, composition, and cleanliness shall be specified.

5.2.10.2 Sawing. The wafer feed rate limits, wheel thickness, slurry, and washing shall be specified.

5.2.10.3 Anvil. Wafer protection, anvil, pressure, etc., shall be specified as applicable.

5.2.11 Die attach. For each type of device, the die attach material, package type and die orientation shall be specified. Additional requirements such as time, temperature, pressure, scrub, die attach environment, or others as applicable shall be specified.

5.2.12 Interconnect bonding. Techniques (ultrasonic, thermocompression, tape automated bonding, etc.), material (Al, Au, etc.), material size (diameter, width, thickness), and type of interconnect (wire, beam lead, etc.) used in connecting die to package shall be identified. The following shall also be specified, if applicable: Temperature, pressure dwell time, condition of capillary or electrode control, power, loop height, size and thickness/width of bond, and environment.

5.2.13 Internal visual inspection. When specified, the procedures for internal visual inspection of semiconductors shall be documented and shall be in accordance with the applicable MIL-STD-750 test methods.

5.2.14 Sealing. The sealing technique and materials used shall be specified. The following shall also be specified: Pre-seal bake (time, temperature, atmospheric conditions), temperature or power, moisture content of sealing environment, flow rate of gases, profile and welding controls (pressure, power, time, etc.), cleaning, and package orientation.

5.2.15 Marking. The techniques, procedures, and materials used for marking shall be specified.

5.2.16 Foreign material contamination (FMC). Procedures for a FMC control program shall be documented in accordance with MIL-STD-750, method 2069, 2070, 2072 or 2073 (as applicable). The procedures and the results of the required audits and subsequent corrective action(s) shall be made available for the qualifying activity's review. Records shall cover at least the previous three-month period except where not possible (e.g., new certification).

5.2.17 Process monitor programs. Process monitor programs required by the "Process monitor programs" paragraph of MIL-S-19500, shall have provisions for the following:

5.2.17.1 Wire bonding. The manufacturer shall monitor the wire bond strength in accordance with the manufacturer's documented procedure. The frequency of this procedure shall be performed at machine setup as a minimum. At the manufacturer's option, this procedure shall consider shift start and stop, change of operators, spools, packages, wire size, lot size, and other related factors.

5.2.17.2 Die attachment. The manufacturer shall monitor the die attachment integrity in accordance with the manufacturer's documented procedure. This procedure shall be performed at each equipment setup as a minimum. At the manufacturer's option, this procedure shall consider other related factors.

5.2.17.3 Package sealing. The manufacturer shall monitor seal integrity in accordance with the manufacturer's documented procedure. A test plan shall be available for review by the qualifying activity.

5.2.17.4 Lead attach and final lead finish thickness. The manufacturer shall monitor the package lead attach and the final lead finish thickness in accordance with MIL-S-19500. A test plan shall be available for review by the qualifying activity.

5.2.17.5 Inspection by scanning electron microscope (SEM). A SEM program shall be established to ensure adequate process control and coverage of metallization for overlay devices having metal line widths less than 1 mil. SEM evaluation shall be performed at a minimum of once per month per wafer fabrication line.

5.2.18 Radiation hardness assurance (RHA) program. The manufacturer of RHA devices shall have documentation defining the critical factors and the procedures for design, manufacture, inspection, and testing of RHA devices (including RHA test structures). The manufacturer shall consult MIL-HDBK-279 and MIL-HDBK-280, for guidance regarding development of this documentation. This documentation shall be available for review by the qualifying activity.

5.2.18.1 Test structures. The manufacturer's documentation shall define test structures (devices, patterns, or coupons) used to monitor radiation response or processes affecting radiation response. The applications of these structures (sample plan, frequency, type of testing, and acceptance testing) shall be detailed. The correlation in radiation response between the test structures and the semiconductor shall be documented.

5.3 JANS line requirements. In addition to sections 4, 5.1, and 5.2, the manufacturer shall document and demonstrate capability to control the following:

5.3.1 Substrate measurements. Using documented techniques and capable equipment, the manufacturer shall have performed and continue to be capable of performing the measurements specified in table I. If the qualifying activity has reason to doubt the capability of the manufacturer to correctly make these measurements, the qualifying activity may request that additional measurements be made in their presence. The qualifying activity may also request that the substrates, including the recorded measurements, be submitted to the qualifying activity for performance testing in accordance with some or all of the measurements specified in MIL-STD-750 and referenced in table I. An adequate vendor quality system may also be implemented to meet any or all of these measurements.

5.3.2 Pinhole and crack measurements. Demonstrate the method used during production for detecting and measuring the densities and size of pinholes and cracks in a typical oxide layer. Test method 5006 of MIL-STD-750 or an equivalent test shall be used. The qualifying activity may request samples of oxides that have these imperfections identified and measured be submitted for verification in accordance with the aforementioned test methods. The wafer lot reject limits, disposition of reject wafers, and corrective actions shall be specified.

5.3.3 Stability of devices. To assure the stability of each process step in producing devices, the manufacturer shall have documented procedures to show that they have developed and are using tests such as high temperature reverse bias, BV_{CEO}, BV_{DSS}, BV_{GO}, h_{FE}, I_{CBO}, I_{EBO}, V_T, sheet resistivity, or others. The manufacturer may be required to demonstrate these tests to the qualifying activity. Records, such as X-bar or R charts shall be available with parameter limits that show control of the process used for producing devices.

5.3.4 CV plotting. Current CV plots or equivalent in accordance with method 5002 of MIL-STD-750 shall be made available to the qualifying activity. CV plotting may be required to be performed during the audit.

5.3.5 Induced wafer defects. When requested by the qualifying activity, the manufacturer shall demonstrate that the quantity of induced dislocations and other defects are not sufficient to be deleterious to the characteristics of the junctions, oxide layers or other structures built in or on the substrate.

5.3.6 Photoresist pinholes. The test method and the maximum density of pinholes shall be specified for each photoresist type.

5.3.7 Masks. The defect density (size, hard and soft, etc.) allowable on working masks, and cleaning and inspection frequencies shall be specified.

5.3.8 Epitaxy. The stacking fault count allowable of the epi-layer shall be specified and recorded.

5.3.9 Stability of conductors. The tests specified in 5.3.9.1 and 5.3.9.2 are applicable, as a minimum, to manufacturing lines on which devices having any of the following are manufactured:

a. Conductor line widths narrower than 2 microns.

b. Multilevel structures.

c. Conductors other than doped aluminum, gold, titanium tungsten, polysilicon, or nichrome.

As an alternative to the requirements of 5.3.9.1 and 5.3.9.2, data may be presented to the qualifying activity which demonstrates the stability of the metallization and contacts of actual devices from the lines to be certified under temperature and high current density stresses. The qualifying activity shall evaluate the manufacturer's test procedures and results for acceptability.

5.3.9.1 Effect of time and temperature. Data shall be presented to the qualifying activity for each metallization type used on the line(s) to be certified and to demonstrate the stability of contact resistance under accelerated time and temperature conditions. If more than one conductor-contact type is used (e.g., metal-polysilicon, metal-multilayer, polysilicon-silicon, etc.), data shall be presented for each conductor-contact type.

An acceptable test would consist of subjecting the conductor-contact test patterns to a storage temperature of 200°C for 2,000 hours. Unless otherwise specified, each test pattern should contain at least 60 conductor-contacts of each type.

Five test patterns or actual devices from each of five different deposition runs shall be used for the test. The contact resistance shall be measured before and after the temperature stress test and the data shall be recorded. The manufacturer's test plan, procedures, failure criteria, and test results shall be reviewed for acceptability by the qualifying activity.

Equivalent time and temperature tests are allowed when approved by the qualifying activity.

5.3.9.2 Effect of current. Data shall be presented to the qualifying activity for each conductor type and type of deposition system to be certified in order to demonstrate absence of electromigration under current and temperature accelerated test conditions.

Test patterns may be used which contain metallization crossovers, contacts, etc. These test patterns are laid out using design rules (layouts, dimensions, etc.) representative of the worst case design rules used in the production line to be certified.

Five test patterns or actual devices containing each conductor type from five different deposition runs for each metallization equipment type (E-beam, filament, etc.) on the line to be certified shall be tested and the data recorded for review by the qualifying activity. The manufacturer's test plan, procedures, failure criteria, and test results shall be reviewed for acceptability by the qualifying activity.

Equivalent time and temperature tests are allowed when approved by the qualifying activity.

5.3.10 Inspection by scanning electron microscope (SEM). A continuing SEM program shall be established to ensure control over metallization at oxide window edges. This program shall consist of the SEM process monitor in accordance with 5.2.17.5 except that the SEM criteria shall be in accordance with method 2077 of MIL-STD-750. SEM wafer lot acceptance data, when available, may be used instead of this monitor.

SEM photographs shall be presented demonstrating capability of meeting the requirements of method 2077 of MIL-STD-750. The angles from which the photographs are taken shall be varying and they shall be from a minimum of four lots per month manufactured over a period of at least the preceding six months. These photographs should include, as a minimum, views of the deepest oxide step covered by metallization lines. These photographs should confirm that the metallization process meets the SEM requirements of method 2077 of MIL-STD-750. The manufacturer's SEM operator(s), who make assessments in accordance with method 2077 of MIL-STD-750, shall satisfy the following criteria: (1) Demonstrate the ability to attain the required resolution as specified in paragraph 2 of method 2077 of MIL-STD-750; (2) Clearly identify all defects in accordance with the documented library of defects; and (3) Receive training and retraining on a yearly (minimum) basis.

TABLE I. Substrate measurements.

Test	MIL-STD-750 test method (or equivalent) 1/	Maximum tolerance 2/
1. Diameter	5007 (F613)	3-inch wafers: ±20 mils 100 mm wafers: ±0.50 mm 125 mm wafers: ±0.50 mm 150 mm wafers: ±0.50 mm
2. Thickness	5010 (F533)	3-inch wafers: ±25 µm 100 mm wafers: ±25 µm 125 mm wafers: ±25 µm 150 mm wafers: ±25 µm
Thickness variation	5010 (F533, F657)	3-inch wafers: 25 µm 100 mm wafers: 50 µm 125 mm wafers: 50 µm 150 mm wafers: 50 µm
3. Warp	5010 (F657)	3-inch wafers: 40 µm 100 mm wafers: 40 µm 125 mm wafers: 60 µm 150 mm wafers: 75 µm
4. Surface finish 3/ 4/	5006 (F523)	
a. Front side		
(1) Scratches		3, length radius/2
(2) Pits		None
(3) Haze		None
(4) Contamination and particulate		3-inch wafers: 6 100 mm wafers: 10 125 mm wafers: 15 150 mm wafers: 15
(5) Contamination area		None
(6) Edge chips 5/		None
(7) Cracks, crowsfeet 5/		None
(8) Craters		None
(9) Dimples		None
(10) Grooves		None
(11) Mounds		None
(12) Orange peel		None
(13) Saw mark		None
(14) Resistivity striation		6/
b. Back side		
(1) Edge chips 5/	1600	None
(2) Cracks, crowsfeet 5/		None
(3) Contamination area		None

See footnotes at end of table.

TABLE I. Substrate measurements - Continued.

Test	MIL-STD-750 test method (or equivalent) 1/	Maximum tolerance 2/
5. Crystal perfection	5009	
a. Dislocation count	(F47)	500 pits/cm^2
b. Lineage	(F80)	None
c. Slip		None
6. Surface orientation	5004 (F263, method A)	1
7. Primary flat	5007	3 inches 0.750-1.000 inch
a. Length	(F671)	100 mm 30.0-35.0 mm 125 mm 40.0-45.0 mm 150 mm 55.0-60.0 mm
b. Orientation	5004 (F847)	1
8. Secondary flat 7/	5007	
a. Length	(F671)	3 inches 0.380-0.500 inch 100 mm 16.0-20.0 mm 125 mm 25.0-30.0 mm 150 mm 35.0-40.0 mm <100> n-type 180° ±5° from primary <111> n-type 45° ±5° CLW from primary <100> p-type 90° ±5° CLW from primary <111> p-type none
9. Conductivity type	5005 (F42)	n or p
10. Resistivity	5008 (F43, F673)	In accordance with specification
Resistivity gradient	5008 (F81)	
11. Oxygen content	5003 (F120, F121)	In accordance with specification
12. Carbon content	(F120, F123)	1 ppm
13. Crystal growth method		In accordance with specification

1/ ASTM test methods are listed in parentheses to provide a means of establishing equivalency.
2/ Tolerances defined within this table are to be used unless other tolerances are approved by the qualifying activity.
3/ Performed on finished polished wafers to an AQL of 1 percent.
4/ All listed characteristics $\leq$ 2.5 percent.
5/ Cumulative AQL for both front side and back side is 1 percent.
6/ Striations may be visible on low resistivity wafers ($\leq$ 0.020 ohm-cm)
7/ Secondary flat is vendor dependent.

5.3.11 Current density verification. Assumptions for thinning or narrowing shall be verified at initial qualification and upon any major change in design or process that affects worst case current density or upon the request of the qualifying activity.

5.3.12 Control of materials for assembly area. The criteria, sampling requirements, acceptable control limits, and handling which reflect the higher reliability requirements of JANS shall be identified. As a minimum, these requirements shall include:

a. Formation of special inspection lots for critical materials and for packages.

b. Sample assembly of critical items into packages and their acceptability.

5.3.13 Effect of time and temperature on electrical resistance and strength of bonds. Evidence shall be presented to demonstrate the mechanical and electrical integrity of the bonds with respect to such factors as: (1) Flexing of bond wire due to thermal expansion; and (2) Microcracks or microvoids at the wafer interface.

5.3.14 Die attachment. The die strength test shall be performed for both eutectic and adhesive (epoxy, metal-glass) die attach. For eutectic die attach, the die shear strength test shall be performed at the start and finish of operator change, package type change, die size change, and after every two hours of production. This die shear strength test shall be in accordance with method 2017 of MIL-STD-750. Alternatively, for adhesive die attach techniques (e.g., silverglass and epoxy), each lot or sublot die attached on a single machine and processed as a single group through final adhesive cure shall be tested to the die strength test method 2017 of MIL-STD-750 on a randomly selected sample of 0.5 percent of the lot size, or two devices, whichever is greater. In the event that the die shear is less than the value of figure 4, method 2017 of MIL-STD-750, the die attach station and process shall be closed down until tests show that satisfactory operation has been re-established. A procedure for the traceability, recovery, and disposition of all units die attached since the last successful die shear test shall be required. This procedure shall provide for sample size, reject criteria, and disposition of failed lots. This test may be conducted on the same samples used for the wire bond strength test.

5.3.15 Wire bond strength test. The manufacturer's wire bond strength test shall be conducted on each sample in accordance with the requirements of MIL-STD-750, method 2037, test condition A. The manufacturer shall submit the sampling plan to the qualifying activity for approval, which shall include start and completion of shifts, frequency of sampling during the shift, change of operators, spools, packages, wire size, lot size, and other related factors (e.g., bond pull testing two devices approximately every two hours of production). Pull strength data shall be read, recorded, and maintained in accordance with the specified requirements. Data shall include the force (grams) required for failure, the physical location of the point of failure, and the nature of the failure. In the event that any bond strength is less than the pre-seal value given in table I, method 2037 of MIL-STD-750, the bonder shall be inactivated immediately and not returned to production until tests show that satisfactory operation has been re-established. A procedure for the traceability, recovery, and disposition of all units bonded since the last successful bond strength test shall be required. This procedure shall provide for sample size, number of bonds and device to be tested, reject criteria, and disposition of failed lots.

5.3.16 Internal visual inspection. The circuits shall be visually inspected using adequate visual aids, inspection criteria, storage, and equipment. Handling and storage shall be documented in accordance with methods 2069, 2070, 2072 or 2073 of MIL-STD-750 as applicable for the product being inspected.

5.3.17 Internal water vapor levels. Documentation from a test laboratory that has been granted suitability from DESC shall be provided at the time of the audit showing the actual internal water vapor level of devices for a package type for which qualification is desired. These devices shall have been processed and screened on the same line which is being evaluated for JANS certification.

5.3.18 Lid torque test. For glass frit sealed packages, the manufacturer shall document the testing and sampling procedure for lid torque testing in accordance with method 2024 of MIL-STD-883. This procedure shall be available to the qualifying activity for their review.

6. NOTES

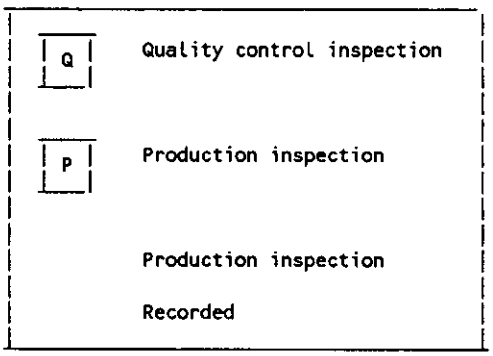
(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory.)

6.1 Intended use. Intended use is for the certification program for MIL-S-19500.

6.2 Subject term (key word) listing.

Process monitor programs

PRODUCT FLOW	OPERATION TITLE	SPECIFICATION NO.
	Substrate inventory	M and SS 341, Q and R 3540
	Issue material/lot form	LIN 4540
	Wafer clean	LIN 4541
	P-oxidation	LIN 4503
	Oxide X_J evaluation	LIN 4504
	Diffusion surface inspec.	LIN 4520
	Resist	M and SS 401
	Apply photoresist	LIN 5504
	Soft bake	LIN 5505
	Mask	Q and R 3560
	Align and expose photores	LIN 5506
	Develop	LIN 5507
	Hard bake	LIN 5540
	Develop inspect	LIN 7820
	Backspin resist	LIN 5531
	Hard bake	LIN 5540
	Develop inspect	LIN 7829, W and R 6555, Q and R 6570



NOTES:
1. Specification revision and dates must be current at the time of audit. This information shall not be placed on the flowchart. However, this information must be made available to the certification team during the audit.
2. This flowchart is not complete and is used as an example to show the type of information which shall be included.

FIGURE 1. Typical process flowchart.

Plant name and address	MIL-S-19500 detail spec(s)	Semiconductor device type(s)	Test report no. 19500-
			Part name (SCR, FET, etc.)
			Date Rev.
			Manufacturer's die designation
Signature of responsible official			

ATTENTION: For any given process, additional information may be required.

SECTION I. WAFER PROCESS SECTION

Revision_____ Date_____

Manufacturer:	
Wafer fab line identification:	Wafer fab flowchart number:
Applicable military detail specification(s):	

A. Process baseline:

1. Device technology (MOSFET, BIPOLAR, etc.):_____

2. Substrate (include tolerances):

   a. Material:_____

   b. Crystal orientation:_____

   c. EPI/NON EPI:_____

   d. Final thickness:_____

   e. Wafer diameter:_____

   f. N or P doped/specify type (min/max thickness)

   g. Life time: Yes_____ No_____

   h. Doping (i.e., gold, platimun, electron irradiation)

FIGURE 2. Design and construction information (semiconductor).

3. Wafer mask:

   a. Wafer mask control document no.:_____

   b. Mask type (emulsion, glass, etc.):_____

4. Wafer surface depositions:

Deposition	Material	Deposition technique	Thickness	
			Min. (A)	Max. (A)
Metallization (front)				
Metalliation (back)				

5. Layout geometry:

   a. Die size (nominal):_____x_ _____ Mils

   b. Die thickness (nominal):_____ Mils

   c. Bond pad size (minimum) _____x_____Mils, or _____Mils diameter

   d. Beuel angle: _____

6. Metallization calculated maximum internal conductor current density_____A/cm^2

7. Photograph of the die surface is attached_____Yes _____No, previously submitted on_____(date)

8. In-line EPI layer: Yes_____ No_____

   a. Reactor type:_____

   b. Silicon source:_____

   c. Impurity source:_____

   d. EPI thickness: Min_____ Max

   e. EPI resistivity limits: Min_____ Max_____

   f. EPI spike count: Max_____

   g. Dislocation:_____

9. Method when wafer purchased with EPI

   Substrate measurements per table I.

FIGURE 2. Design and construction information (semiconductor) - Continued.

10. Passivation 1/, glassivation 2/ and organic 3/ system passivation/glassivation type: Oxide_____ Nitride_____

a. Oxide:

(1) Impurity source:

(2) Impurity concentration and tolerance:

(3) Percent by weight of phosphorous concentration in glassivation: _____

(4) Process temperature: Min_____ Max_____

b. Nitride:

(1) Process temperature: Min_____ Max_____

Level/layer number and identification 4/	Material composition (purity if applicable)	Deposition process	Final thickness		
			Min	Max	Units

c. Organic:

Die protective coating	Mfg:	Cure	MIL Time:	MIL Temp:

11. Processing location(s): 5/

Operation	Plant or building	Address: Street, City, State

1/ Passivation is the silicon oxide, nitride or other insulating material that is grown or deposited directly on the die prior to the deposition of metal.
2/ Glassivation is the top layer(s) of transparent insulating material that covers the active circuit area including metallization, except bonding pads and beam.
3/ Organic carbon compounds used as coatings to protect a die.
4/ List all passivation, conduction, glassivation, and any other levels deposited in the actual order deposited, level number 1 being the one closest to the substrate; each level number only once.
5/ Applicable if wafer operations are performed outside of job location (see section 1, Wafer Process Section).

FIGURE 2. Design and construction information (semiconductor) - Continued.

SECTION II. ASSEMBLY

A. Package materials: (Diodes)

Part	Base material	Underplating and plating			Spec. or dwg. no.
		Material	Thickness Min	Thickness Max	
_____ glass filled Header_____solid					
Die-mount base					
Lid					
Bonding posts					
Glass type for post isolation					
Tubulations					
External leads					
Axial lead thermal resistance: °C/W/cm					

1. Die ohmic contacts (methods and materials):

a. Cathode:

(1) Type contact:_____ (3) Max temp:_____ °C

(2) Materials:_____ (4) Time at max T°:_____ °C

(5) Atmosphere:_____

b. Anode:

(1) Type contact:_____ (3) Max temp:_____ °C

(2) Materials:_____ (4) Time at max T°:_____ °C

(5) Atmosphere:_____

c. Multiple die interconnect: (Pairs, arrays, etc.):

(1) Type contact:_____ (3) Max temp:_____ °C

(2) Materials:_____ (4) Time at max T°:_____ °C

(5) Atmosphere:_____

FIGURE 2. Design and construction information (semiconductor) - Continued.

2. Package sealing technique:

   a. Sealing atmosphere:_____ Moisture content_____ ppm, max

   b. Sealing method:_____

   c. Sealing material:_____

   d. Seal temperature:_____°C

   e. Approximate cavity volume:_____cc

   f. Organic material, if any:_____ Cure cycle: Time____Temp_____ °C

3. Element electrically connected to the case (i.e., cathode):_____

4. Method used to shield die from light:_____

5. Description. The following items are attached:

   a. Photographs or drawing of internal configuration (indicating all multiple die locations and interconnections_____ Yes_____ No, Submitted_____(Date)

   b. Description of unique construction detail not covered above _____Yes _____N/A

6. Die sigulation method (saw/diamond, etc.)

B. Package materials: (Transistors)

Part	Base material	Underplating and plating			Spec. or dwg. no.
		Material	Thickness Min	Thickness Max	
_____ glass filled Header_____solid					
Die-mount base					
Lid					
Bonding posts					
Glass type for post isolation					
Tubulations					
External leads					

FIGURE 2. Design and construction information (semiconductor) - Continued.

1. Die attach:

   (a) Material:_____ (d) Time at max temp._____

   (b) Method:_____ (e) Atmosphere:_____

   (c) Temperature:_____°C

2. Internal wire bonding:

Wire bond	Type of bond	No.	Wire material	Wire diameter	E, B, etc.
Die					
Post					

3. Package sealing technique:

   a. Sealing atmosphere:_____ Moisture content_____ ppm, max

   b. Sealing method:_____

   c. Sealing material:_____

   d. Seal temperature:_____ °C

   e. Approximate cavity volume:_____ cc

   f. Organic material, if any:_____ Cure cycle: Time_____ Temp_____ °C

4. Element electrically connected to the case (i.e., cathode):_____

5. Power at 25°C case temperature:____four watts or higher_____less than four watts

6. Description. The following items are attached:

   a. Photographs or drawing of internal configuration (indicating all multiple die locations and interconnections)_____ Yes_____ No,
   Submitted_____(Date)

   b. Description of unique construction detail not covered above
   _____Yes _____N/A

7. Die singulation method (saw, diamond scribe, sand blast, etc.)

FIGURE 2. Design and construction information (semiconductor) - Continued.

8. Scribe, break, and assembly location(s):

Operation	Plant or building	Address: Street, City, State

FIGURE 2. Design and construction information (semiconductor) - Continued.

CONCLUDING MATERIAL

Custodians:
Army - ER
Navy - EC
Air Force - 17
NASA - NA

Review activities:
Army - AR, MI
Navy - SH
Air Force - 11, 19, 85, 99
DLA - ES

User activities:
Army - SM
Navy - AS, CG, MC, OS

Preparing activity:
NASA - NA

Agent:
DLA - ES

(Project 5961-1257)

STANDARDIZATION DOCUMENT IMPROVEMENT PROPOSAL

INSTRUCTIONS

1. The preparing activity must complete blocks 1, 2, 3, and 8 In block 1, both the document number and revision letter should be given.
2. The submitter of this form must complete blocks 4, 5, 6, and 7.
3. The preparing activity must provide a reply within 30 days from receipt of the form.

NOTE: This form may not be used to request copies of documents, nor to request waivers, or clarification of requirements on current contracts. Comments submitted on this form do not constitute or imply authorization to waive any portion of the referenced document(s) or to amend contractual requirements.

I RECOMMEND A CHANGE:	1. DOCUMENT NUMBER	2. DOCUMENT DATE (YYMMDD)
	MIL-STD-989	1991 November 11

3. DOCUMENT TITLE
Certification Requirements For JAN Semiconductor Devices

4. NATURE OF CHANGE *(Identify paragraph number and include proposed rewrite, if possible. Attach extra sheets as needed.)*

5. REASON FOR RECOMMENDATION

6. SUBMITTER

a. NAME (Last, First, Middle Initial)	b. ORGANIZATION	
c. ADDRESS (Include Zip Code)	d. TELEPHONE (Include Area Code) (1) Commercial (2) AUTOVON (If applicable)	7. DATE SUBMITTED (YYMMDD)

8. PREPARING ACTIVITY

a. NAME	b. TELEPHONE (Include Area Code) (1) Commercial	(2) AUTOVON
NASA/Parts Project Office (NPP))	301-286-8884	
c. ADDRESS (Include Zip Code) NASA Goddard Space Flight Center Code 311.A Greenbelt, MD 20771	IF YOU DO NOT RECEIVE A REPLY WITHIN 45 DAYS, CONTACT: Defense Quality and Standardization Office 5203 Leesburg Pike, Suite 1403, Falls Church, VA 22041-3466 Telephone (703) 756-2340 AUTOVON 289-2340	