Notice of Change

This document and process conversion measures necessary to comply with this revision shall be completed by 30 September 2003

INCH-POUND

MIL-STD-883E
NOTICE 5
7 March 2003

DEPARTMENT OF DEFENSE

TEST METHOD STANDARD
MICROCIRCUITS

TO ALL HOLDERS OF MIL-STD-883E:

1. THE FOLLOWING TEST METHODS OF MIL-STD-883E HAVE BEEN REVISED AND SUPERSEDE THE TEST METHODS LISTED:

NEW METHOD	DATE	SUPERSEDED METHOD	DATE
1019.6	07 March 2003	1019.5	1 December 1997
2019.7	07 March 2003	2019.6	18 December 2000

2. THE FOLLOWING PAGES OF MIL-STD-883E HAVE BEEN REVISED AND SUPERSEDE THE PAGES LISTED:

METHOD	NEW PAGE	DATE	SUPERSEDED PAGE	DATE
---	iii	31 December 1996	iii	REPRINTED WITHOUT CHANGE
---	iv	07 March 2003	iv	18 December 2000
---	v	05 November 1999	v	REPRINTED WITHOUT CHANGE
---	vi	18 December 2000	vi	REPRINTED WITHOUT CHANGE
1014.10	5	14 March 1995	5	REPRINTED WITHOUT CHANGE
	6	07 March 2003	6	14 March 1995
1018.3	1	07 March 2003	1	18 December 2000
	2	18 December 2000	2	REPRINTED WITHOUT CHANGE
2010.10	3	07 March 2003	3	27 July 1990
	4	07 March 2003	4	27 July 1990
	5	07 March 2003	5	27 July 1990
	6	07 March 2003	6	27 July 1990
	39	07 March 2003	39	27 July 1990
	39a	07 March 2003	39a	new page
	39b	07 March 2003	39b	new page
	40	18 December 2000	40	REPRINTED WITHOUT CHANGE
	49	07 March 2003	49	27 July 1990
	50	27 July 1990	50	REPRINTED WITHOUT CHANGE

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3. RETAIN THIS NOTICE AND INSERT BEFORE TABLE OF CONTENTS.

4. Holders of MIL-STD-883E will verify that page changes, additions, and corrections indicated above have been entered. This notice page will be retained as a check sheet. This issuance, together with appended pages, is a separate publication. Each notice is to be retained by stocking points until the military standard is completely revised or canceled.

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CONCLUDING MATERIAL

Custodians:
Army - CR
Navy - EC
Air Force - 11
NASA-NA
DLA - CC

Preparing activity:
DLA - CC

Review activities
Army - AR, MI, SM
Navy - OS, SH, TD, AS, CG, MC
Air Force - 19, 99

(Project 5962-1943)

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FIGURES

FIGURE

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TEST METHODS

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TABLE II. Fixed conditions for test condition A_1.

Volume of package (V) in cm^3	Bomb condition			R_1 Reject limit (atm cc/s He)
	Psia ±2	Minimum exposure time hours (t_1)	Maximum dwell hours (t_2)	
<0.05	75	2	1	5×10^{-8}
≥0.05 - <0.5	75	4	1	5×10^{-8}
≥0.5 - <1.0	45	2	1	1×10^{-7}
≥1.0 - <10.0	45	5	1	5×10^{-8}
≥10.0 - <20.0	45	10	1	5×10^{-8}

3.1.1.2 Test condition A_2, flexible method. Values for bomb pressure exposure time, and dwell time shall be chosen such that actual measured tracer gas leak rate (R_1) readings obtained for the devices under test (if defective) will be greater than the minimum detection sensitivity capability of the mass spectrometer. The devices shall be subjected to a minimum of 2 atmospheres absolute of helium atmosphere. If the chosen dwell time (t_2) is greater than 60 minutes, graphs shall be plotted to determine an R_1 value which will assure overlap with the selected gross leak test condition. The chosen values, in conjunction with the value of the internal volume of the device package to be tested and the maximum equivalent standard leak rate (L) limit (as shown below or as specified in the applicable acquisition document), shall be used to calculate the measured leak rate (R_1) limit using the following formula:

$$R_1 = \frac{LP_E}{P_O}\left(\frac{M_A}{M}\right)^{\frac{1}{2}} \left\{1 - e^{-\left[\frac{LT_1}{VP_0}\left(\frac{M_A}{M}\right)^{\frac{1}{2}}\right]}\right\} e^{-\left[\frac{LT_2}{VP_0}\left(\frac{M_A}{M}\right)^{\frac{1}{2}}\right]}$$

Where:

R_1 = The measured leak rate of tracer gas (He) through the leak in atm cc/s He.
L = The equivalent standard leak rate in atm cc/s air.
P_E = The pressure of exposure in atmospheres absolute.
P_O = The atmospheric pressure in atmospheres absolute. (1)
M_A = The molecular weight of air in grams. (28.7)
M = The molecular weight of the tracer gas (Helium) in grams. (4)
t_1 = The time of exposure to P_E in seconds.
t_2 = The dwell time between release of pressure and leak detection, in seconds.
V = The internal volume of the device package cavity in cubic centimeters.

3.1.1.2.1 Failure criteria. Unless otherwise specified, devices with an internal cavity volume of 0.01 cc or less shall be rejected if the equivalent standard leak rate (L) exceeds 5×10^{-8} atm cc/s air. Devices with an internal cavity volume greater than 0.01 cc and equal to or less than 0.4 cc shall be rejected if the equivalent standard leak rate (L) exceeds 1×10^{-7} atm cc/s air. Devices with an internal cavity volume greater than 0.4 cc shall be rejected if the equivalent standard leak rate (L) exceeds 1×10^{-6} atm cc/s air.

* 3.1.2 Test condition A_4, procedure applicable to the unsealed package method. The fixture and fittings of 2.1a. shall be mounted to the evacuation port of the leak detector. Proof of fixturing integrity shall be verified by sealing a flat surfaced metal plate utilizing the gasket of 2.1 (and grease or fluid of 2.1 if required to obtain seal) and measuring the response of the leak test system. Testing shall be performed by sealing the package(s) to the evacuation port and the package cavity evacuated to 0.1 torr or less. Care shall be taken to prevent contact of grease with package (seal ring not included) to avoid masking leaks. The external portion of the package shall be flooded with Helium gas either by the use of an envelope or a spray gun, at a pressure of 10 psig.

3.1.2.1 Failure criteria. Unless otherwise specified, devices shall be rejected if the measured leak rate (R_1) exceeds 1 x 10^{-8} atm cc/s He.

3.2 Test condition B, radioisotope fine leak test.

3.2.1 Activation parameters. The activation pressure and soak time shall be determined in accordance with the following equation:

$$Q_S = \frac{R}{skT\,\overline{P}\,t} \qquad (1)$$

The parameters of equation (1) are defined as follows:

Q_S = The maximum leak rate allowable, in atm cc/s Kr, for the devices to be tested.

R = Counts per minute above the ambient background after activation if the device leak rate were exactly equal to Q_S. This is the reject count above the background of both the counting equipment and the component, if it has been through prior radioactive leak tests.

s = The specific activity, in microcuries per atmosphere cubic centimeter, of the krypton-85 tracer gas in the activation system.

k = The overall counting efficiency of the scintillation crystal in counts per minute per microcurie of krypton-85 in the internal void of the specific component being evaluated. This factor depends upon component configuration and dimensions of the scintillation crystal. The counting efficiency shall be determined in accordance with 3.2.2.

T = Soak time, in hours, that the devices are to be activated.

$\overline{P}$ = $P_e^{\,2} - P_i^{\,2}$, where P_e is the activation pressure in atmospheres absolute and P_i is the original internal pressure of the devices in atmospheres absolute. The activation pressure (P_e) may be established by specification or if a convenient soak time (T) has been established, the activation pressure (P_e) can be adjusted to satisfy equation (1).

t = Conversion of hours to seconds and is equal to 3,600 seconds per hour.

NOTE: The complete version of equation (1) contains a factor ($P_O^{\,2} - (\Delta P)^2$) in the numerator which is a correction factor for elevation above sea level. P_O is sea level pressure in atmospheres absolute and ΔP is the difference in pressure, in atmospheres between the actual pressure at the test station and sea level pressure. For the purpose of this test method, this factor has been dropped.

METHOD 1018.3

INTERNAL WATER-VAPOR CONTENT

1. PURPOSE. The purpose of this test is to measure the water-vapor content of the atmosphere inside a metal or ceramic hermetically-sealed device. It can be destructive (procedures 1 and 2) or nondestructive (procedure 3).

2. APPARATUS. The apparatus for the internal water-vapor content test shall be as follows for the chosen procedure:

2.1 Procedure 1. (Procedure 1 measures the water-vapor content of the device atmosphere by mass spectrometry.) The apparatus for procedure 1 shall consist of:

a. A mass spectrometer meeting the following equipments:

(1) Spectra range. The mass spectrometer shall be capable of reading a minimum spectra range of 1 to 100 atomic mass units (AMUs).

(2) Detection limit. The mass spectrometer shall be capable of reproducibly detecting the specified moisture content for a given volume package with signal to noise ratio of 20 to 1 (i.e., for a specified limit of 5,000 ppmv, .01 cc, the mass spectrometer shall demonstrate a 250 ppmv minimum detection limit to moisture for a package volume of .01 cc). The smallest volume shall be considered the worst case.

(3) Calibration. The calibration of the mass spectrometer shall be accomplished at the specified moisture limit (±20 percent) using a package simulator which has the capability of generating at least three known volumes of gas ±10 percent on a repetitive basis by means of a continuous sample volume purge of known moisture content ±10 percent. Moisture content shall be established by the standard generation techniques (i.e., 2 pressure, divided flow, or cryogenic method). The dew point analyzer shall be recalibrated a minimum of once per year using equipment traceable to NIST or by a suitable commercial calibration services laboratory using equipment traceable to NIST standards. Calibration records shall be kept on a daily basis. Gas analysis results obtained by this method shall be considered valid only in the moisture range or limit bracketed by at least two (volume or concentration) calibration points (i.e., 5,000 ppmv between .01 -.1 cc or 1,000 – 5,000 ppmv between .01 - .1 cc). A best fit curve shall be used between volume calibration points. Systems not capable of bracketing may use an equivalent procedure as approved by the qualifying activity. Corrections of sensitivity factors deviation greater than 10 percent from the mean between calibration points shall be required.

NOTE: It is recommended that the percentage of water vapor contained in a gas flowing through the gas humidifier be compared to the dewpoint sensor reading for accuracy of the sensor. The following equation may be used to calculate the percent of water vapor contained in a gas flowing through the gas humidifier.

$$\%H_2O = \frac{100(Pvmb)}{68.95\ mb/psi\ Pg + 1.33 mb/mmPa}$$, where

P_v = vapor pressure of water in the GPH based on water temperature in degrees centigrade,
P_g = gauge pressure in psi, and
P_a = atmospheric pressure in mm Hg.

(4) Calibration for other gases. Calibration shall be required for all gases found in concentrations greater than .01 percent by volume. As a minimum, this shall include all gases listed in 3.1c. The applicable gases shall be calibrated at approximately 1 percent concentrations as part of the yearly calibration requirements, with the exception of fluorocarbons, which may use a concentration of approximately 200 ppmv; nitrogen, which may use a concentration of approximately 80 percent or more; helium, which may use a concentration of approximately 10 percent; and oxygen, which may use a concentration of approximately 20 percent. *

(5) Calibration check. The system calibration shall be checked on the day of test prior to any testing. This shall include checking the calibration by in-letting a 5000 ppmv ±20% moisture calibration sample of the required volumes and comparing the result with the calibration sample. The resulting moisture reading shall be within 250 ppmv of the moisture level in the calibration sample. Calibration performed on the day of test prior to any testing may be substituted for the calibration check.

b. A vacuum opening chamber which can contain the device and a vacuum transfer passage connecting the device to the mass spectrometer of 2.1a. The system shall be maintained at a stable temperature equal to or above the device temperature. The fixturing in the vacuum opening chamber shall position the specimen as required by the piercing arrangement of 2.1c, and maintain the device at 100°C ±5°C for a minimum of 10 minutes prior to piercing.

Note: A maximum 5-minute transfer time from prebake to hot insertion into apparatus shall be allowed. If 5 minutes is exceeded, device shall be returned to the prebake oven and the prebake continued until device reaches 100 °C ± 5 °C.

For initial certification of systems or extension of suitability, device temperature on systems using an external fixture shall be characterized by placing a thermocouple into the cavity of a blank device of similar mass, internal volume, construction and size. This shall be a means for proving the device temperature has been maintained at 100 °C ± 5 °C for the minimum ten minutes. This also applies to devices prebaked in an external oven but tested with the external fixture to adjust for any temperature drop during the transfer. These records shall be maintained by the test laboratory.

c. A piercing arrangement functioning within the opening chamber or transfer passage of 2.1b, which can pierce the specimen housing (without breaking the mass spectrometer chamber vacuum and without disturbing the package sealing medium), thus allowing the specimen's internal gases to escape into the chamber and mass spectrometer.

NOTE: A sharp-pointed piercing tool, actuated from outside the chamber wall via a bellows to permit movement, should be used to pierce both metal and ceramic packages. For ceramic packages, the package lid or cover should be locally thinned by abrasion to facilitate localized piercing.

2.2 Procedure 2. (Procedure 2 measures the water-vapor content of the device atmosphere by integrating moisture picked up by a dry carrier gas at 50°C.) The apparatus for procedure 2 shall consist of:

a. An integrating electronic detector and moisture sensor capable of reproducibly detecting a water-vapor content of 300 ±50 ppmv moisture for the package volume being tested. This shall be determined by dividing the absolute sensitivity in micrograms H_20 by the computed weight of the gas in the device under test, and then correcting to ppmv.

b. A piercing chamber or enclosure, connected to the integrating detector of 2.2a, which will contain the device specimen and maintain its temperature at 100°C ±5°C during measurements. The chamber shall position the specimen as required by the piercing arrangement. The piercing mechanism shall open the package in a manner which will allow the contained gas to be purged out by the carrier gas or removed by evacuation. The sensor and connection to the piercing chamber will be maintained at a temperature of 50°C ±2°C.

2.3 Procedure 3. (Procedure 3 measures the water-vapor content of the device atmosphere by measuring the response of a calibrated moisture sensor or an IC chip which is sealed within the device housing, with its electrical terminals available at the package exterior.) The apparatus for procedure 3 shall consist of one of the following:

a. A moisture sensor element and readout instrument capable of detecting a water-vapor content of 300 ±50 ppmv while sensor is mounted inside a sealed device.

METHOD 1019.6

IONIZING RADIATION (TOTAL DOSE) TEST PROCEDURE

* 1. PURPOSE. This test procedure defines the requirements for testing packaged semiconductor integrated circuits for ionizing radiation (total dose) effects from a cobalt-60 (^{60}Co) gamma ray source. The testing includes both standard room temperature irradiation as well as irradiation at elevated temperature. In addition this procedure provides an accelerated annealing test for estimating low dose rate ionizing radiation effects on devices. This annealing test is important for low dose-rate or certain other applications in which devices may exhibit significant time-dependent effects. This procedure addresses only steady state irradiations, and is not applicable to pulse type irradiations. This test may produce severe degradation of the electrical properties of irradiated devices and thus should be considered a destructive test.

1.1 Definitions. Definitions of terms used in this procedure are given below:

a. Ionizing radiation effects. The changes in the electrical parameters of a device or integrated circuit resulting from radiation-induced charge. These are also referred to as total dose effects.

b. In-flux test. Electrical measurements made on devices during irradiation exposure.

c. Not in-flux test. Electrical measurements made on devices at any time other than during irradiation.

d. Remote tests. Electrical measurements made on devices which are physically removed from the radiation location.

e. Time dependent effects. Significant degradation in electrical parameters caused by the growth or annealing or both of radiation-induced trapped charge after irradiation. Similar effects also take place during irradiation.

f. Accelerated annealing test. A procedure utilizing elevated temperature to accelerate time-dependent effects.

* g. Enhanced Low Dose Rate Sensitivity (ELDRS). Used to refer to a part that shows enhanced radiation induced damage at dose rates below 50 rad(Si)/s.

* h. Overtest. A factor that is applied to the specification dose to determine the test dose level that the samples must pass to be acceptable at the specification level. An overtest factor of 1.5 means that the parts must be tested at 1.5 times the specification dose.

* i. Parameter Delta Design Margin (PDDM). A design margin that is applied to the radiation induced change in an electrical parameter. For a PDDM of 2 the change in a parameter at a specified dose from the pre-irradiation value is multiplied by two and added to the post-irradiation value to see if the sample exceeds the post-irradiation parameter limit. For example, if the pre-irradiation value of Ib is 30 nA and the post-irradiation value at 20 krad(Si) is 70 nA (change in Ib is 40 nA), then for a PDDM of 2 the post-irradiation value would be 110 nA (30 nA + 2 X 40 nA). If the allowable post-irradiation limit is 100 nA the part would fail.

* 2. APPARATUS. The apparatus shall consist of the radiation source, electrical test instrumentation, test circuit board(s), cabling, interconnect board or switching system, an appropriate dosimetry measurement system, and an environmental chamber (if required for time-dependent effects measurements or elevated temperature irradiation). Adequate precautions shall be observed to obtain an electrical measurement system with sufficient insulation, ample shielding, satisfactory grounding, and suitable low noise characteristics.

2.1 Radiation source. The radiation source used in the test shall be the uniform field of a ^{60}Co gamma ray source. Uniformity of the radiation field in the volume where devices are irradiated shall be within ±10 percent as measured by the dosimetry system, unless otherwise specified. The intensity of the gamma ray field of the ^{60}Co source shall be known with an uncertainty of no more than ±5 percent. Field uniformity and intensity can be affected by changes in the location of the device with respect to the radiation source and the presence of radiation absorption and scattering materials.

* 2.2 Dosimetry system. An appropriate dosimetry system shall be provided which is capable of carrying out the measurements called for in 3.2. The following American Society for Testing and Materials (ASTM) standards and guidelines or other appropriate standards and guidelines shall be used:

ASTM E 666 - Standard Method for Calculation of Absorbed Dose from Gamma or X Radiation.

ASTM E 668 - Standard Practice for the Application of Thermoluminescence Dosimetry (TLD) Systems for Determining Absorbed Dose in Radiation-Hardness Testing of Electronic Devices.

ASTM E 1249 - Minimizing Dosimetry Errors in Radiation Hardness Testing of Silicon Electronic Devices.

ASTM E 1250 - Standard Method for Application of Ionization Chambers to Assess the Low Energy Gamma Component of Cobalt 60 Irradiators Used in Radiation Hardness Testing of Silicon Electronic Devices.

ASTM E 1275 - Standard Practice for Use of a Radiochromic Film Dosimetry System.

* ASTM F 1892 - Standard Guide for Ionizing Radiation (Total Dose) Effects Testing of Semiconductor Devices.

These industry standards address the conversion of absorbed dose from one material to another, and the proper use of various dosimetry systems. 1/

2.3 Electrical test instruments. All instrumentation used for electrical measurements shall have the stability, accuracy, and resolution required for accurate measurement of the electrical parameters. Any instrumentation required to operate in a radiation environment shall be appropriately shielded.

2.4 Test circuit board(s). Devices to be irradiated shall either be mounted on or connected to circuit boards together with any associated circuitry necessary for device biasing during irradiation or for in-situ measurements. Unless otherwise specified, all device input terminals and any others which may affect the radiation response shall be electrically connected during irradiation, i.e., not left floating. The geometry and materials of the completed board shall allow uniform irradiation of the devices under test. Good design and construction practices shall be used to prevent oscillations, minimize leakage currents, prevent electrical damage, and obtain accurate measurements. Only sockets which are radiation resistant and do not exhibit significant leakages (relative to the devices under test) shall be used to mount devices and associated circuitry to the test board(s). All apparatus used repeatedly in radiation fields shall be checked periodically for physical or electrical degradation. Components which are placed on the test circuit board, other than devices under test, shall be insensitive to the accumulated radiation or they shall be shielded from the radiation. Test fixtures shall be made such that materials will not perturb the uniformity of the radiation field intensity at the devices under test. Leakage current shall be measured out of the radiation field. With no devices installed in the sockets, the test circuit board shall be connected to the test system such that all expected sources of noise and interference are operative. With the maximum specified bias for the test device applied, the leakage current between any two terminals shall not exceed ten percent of the lowest current limit value in the pre-irradiation device specification. Test circuit boards used to bias devices during accelerated annealing must be capable of withstanding the temperature requirements of the accelerated annealing test and shall be checked before and after testing for physical and electrical degradation.

2.5 Cabling. Cables connecting the test circuit boards in the radiation field to the test instrumentation shall be as short as possible. If long cables are necessary, line drivers may be required. The cables shall have low capacitance and low leakage to ground, and low leakage between wires.

2.6 Interconnect or switching system. This system shall be located external to the radiation environment location, and provides the interface between the test instrumentation and the devices under test. It is part of the entire test system and subject to the limitation specified in 2.4 for leakage between terminals.

2.7 The environmental chamber. The environmental chamber for time-dependent effects testing, if required, shall be capable of maintaining the selected accelerated annealing temperature within ±5°C.

* 2.8 The irradiation temperature chamber. The irradiation temperature chamber, if required for elevated temperature irradiation, should be capable of maintaining a circuit under test at 100°C ±5°C while it is being irradiated. The chamber should be capable of raising the temperature of the circuit under test from room temperature to the irradiation temperature within a reasonable time prior to irradiation and cooling the circuit under test from the irradiation temperature to room temperature in less than 20 minutes following irradiation. The irradiation bias shall be maintained during the heating and cooling. The method for raising, maintaining and lowering the temperature of the circuit under test may be by conduction through a heat sink using heating and cooling fluids, by convection using forced hot and cool air, or other means that will achieve the proper results.

1/ Copies may be obtained from the American Society for Testing and Materials, 1916 Race Street, Philadelphia, PA 19103.

3. PROCEDURE. The test devices shall be irradiated and subjected to accelerated annealing testing (if required for time-dependent effects testing) as specified by a test plan. This plan shall specify the device description, irradiation conditions, device bias conditions, dosimetry system, operating conditions, measurement parameters and conditions, and accelerated annealing test conditions (if required).

3.1 Sample selection and handling. Only devices which have passed the electrical specifications as defined in the test plan shall be submitted to radiation testing. Unless otherwise specified, the test samples shall be randomly selected from the parent population and identically packaged. Each part shall be individually identifiable to enable pre- and post-irradiation comparison. For device types which are ESD-sensitive, proper handling techniques shall be used to prevent damage to the devices.

3.2 Burn-in. For some devices, there are differences in the total dose radiation response before and after burn-in. Unless it has been shown by prior characterization or by design that burn-in has negligible effect (parameters remain within post-irradiation specified electrical limits) on the total dose radiation response, then one of the following must be done:

3.2.1 The manufacturer shall subject the radiation samples to the specified burn-in conditions prior to conducting total dose radiation testing or

3.2.2 The manufacturer shall develop a correction factor, (which is acceptable to the parties to the test) taking into account the changes in total dose response resulting from subjecting product to burn-in. The correction factor shall then be used to accept product for total dose response without subjecting the test samples to burn-in.

3.3 Dosimetry measurements. The radiation field intensity at the location of the device under test shall be determined prior to testing by dosimetry or by source decay correction calculations, as appropriate, to assure conformance to test level and uniformity requirements. The dose to the device under test shall be determined one of two ways: (1) by measurement during the irradiation with an appropriate dosimeter, or (2) by correcting a previous dosimetry value for the decay of the ^{60}Co source intensity in the intervening time. Appropriate correction shall be made to convert from the measured or calculated dose in the dosimeter material to the dose in the device under test.

3.4 Lead/Aluminum (Pb/Al) container. Test specimens shall be enclosed in a Pb/Al container to minimize dose enhancement effects caused by low-energy, scattered radiation. A minimum of 1.5 mm Pb, surrounding an inner shield of at least 0.7 mm Al, is required. This Pb/Al container produces an approximate charged particle equilibrium for Si and for TLDs such as CaF_2. The radiation field intensity shall be measured inside the Pb/Al container (1) initially, (2) when the source is changed, or (3) when the orientation or configuration of the source, container, or test-fixture is changed. This measurement shall be performed by placing a dosimeter (e.g., a TLD) in the device-irradiation container at the approximate test-device position. If it can be demonstrated that low energy scattered radiation is small enough that it will not cause dosimetry errors due to dose enhancement, the Pb/Al container may be omitted.

3.5 Radiation level(s). The test devices shall be irradiated to the dose level(s) specified in the test plan within ±10 percent. If multiple irradiations are required for a set of test devices, then the post-irradiation electrical parameter measurements shall be performed after each irradiation.

* 3.6 Radiation dose rate. The radiation dose rate for bipolar and BiCMOS linear or mixed-signal parts used in applications where the maximum dose rate is below 50 rad(Si)/s shall be determined as described in paragraph 3.13 below. Parts used in low dose rate applications, unless they have been demonstrated to not exhibit an ELDRS response shall use Condition C, Condition D, or Condition E.

* Note: Devices that contain both MOS and bipolar devices may require qualification to multiple subconditions to ensure that both ELDRS and traditional MOS effects are evaluated.

3.6.1 Condition A. For condition A (standard condition) the dose rate shall be between 50 and 300 rad(Si)/s [0.5 and 3 Gy(Si)/s] ^{60}Co 2/ The dose rates may be different for each radiation dose level in a series; however, the dose rate shall not vary by more than ±10 percent during each irradiation.

2/ The SI unit for the quantity absorbed dose is the gray, symbol GY. 100 rad = 1 Gy.

3.6.2 Condition B. For condition B, for MOS devices only, if the maximum dose rate is < 50 rad(Si)/s in the intended application, the parties to the test may agree to perform the test at a dose rate ≥ the maximum dose rate of the intended application. Unless the exclusions in 3.12.1b are met, the accelerated annealing test of 3.12.2 shall be performed.

* 3.6.3 Condition C. For condition C, (as an alternative) the test may be performed at the dose rate agreed to by the parties to the test.

* 3.6.4 Condition D. For condition D, for bipolar or BiCMOS linear or mixed-signal circuits only, the parts shall be irradiated at ≤10 mrad(Si)/s unless the specification dose is greater than 25 krad(Si). For radiation levels greater than 25 krad(Si) the total irradiation time shall be ≥ 1000 hours and the dose rate shall be determined from the total dose (including any overtest factors) and the irradiation time.

* 3.6.5 Condition E. For condition E, for bipolar or BiCMOS linear or mixed-signal circuits only, the parts shall be irradiated at between 0.5 and 5 rad(Si)/s if the specification dose is ≤ 50 krad(Si). Condition E applies to elevated temperature irradiation at 100°C ±5°C and does not apply for devices with specification doses >50 krad(Si) unless it can be demonstrated that the elevated temperature irradiation test provides a conservative bound for low dose rate response at a radiation specification level that is above 50 krad(Si).

* 3.7 Temperature requirements. The following requirements shall apply for room temperature and elevated temperature irradiation.

* 3.7.1 Room temperature irradiation. Since radiation effects are temperature dependent, devices under test shall be irradiated in an ambient temperature of 24°C ±6°C as measured at a point in the test chamber in close proximity to the test fixture. The electrical measurements shall be performed in an ambient temperature of 24°C ±6°C. If devices are transported to and from a remote electrical measurement site, the temperature of the test devices shall not be allowed to increase by more than 10°C from the irradiation environment. If any other temperature range is required, it shall be specified.

* 3.7.2 Elevated temperature irradiation. For bipolar or BiCMOS linear or mixed-signal circuits irradiated using Condition E dose rate, devices under test shall be irradiated in an ambient temperature of 100°C ±5°C as measured at a point in the test chamber in close proximity to the test fixture.

3.8 Electrical performance measurements. The electrical parameters to be measured and functional tests to be performed shall be specified in the test plan. As a check on the validity of the measurement system and pre- and post-irradiation data, at least one control sample shall be measured using the operating conditions provided in the governing device specifications. For automatic test equipment, there is no restriction on the test sequence provided that the rise in the device junction temperature is minimized. For manual measurements, the sequence of parameter measurements shall be chosen to allow the shortest possible measurement period. When a series of measurements is made, the tests shall be arranged so that the lowest power dissipation in the device occurs in the earliest measurements and the power dissipation increases with subsequent measurements in the sequence.

The pre- and post-irradiation electrical measurements shall be done on the same measurement system and the same sequence of measurements shall be maintained for each series of electrical measurements of devices in a test sample. Pulse-type measurements of electrical parameters should be used as appropriate to minimize heating and subsequent annealing effects. Devices which will be subjected to the accelerated annealing testing (see 3.12) may be given a pre-irradiation burn-in to eliminate burn-in related failures.

3.9 Test conditions. The use of in-flux or not in-flux testing shall be specified in the test plan. (This may depend on the intended application for which the data are being obtained.) The use of in-flux testing may help to avoid variations introduced by post-irradiation time dependent effects. However, errors may be incurred for the situation where a device is irradiated in-flux with static bias, but where the electrical testing conditions require the use of dynamic bias for a significant fraction of the total irradiation period. Not-in-flux testing generally allows for more comprehensive electrical testing, but can be misleading if significant post-irradiation time dependent effects occur.

3.9.1 In-flux testing. Each test device shall be checked for operation within specifications prior to being irradiated. After the entire system is in place for the in-flux radiation test, it shall be checked for proper interconnections, leakage (see 2.4), and noise level. To assure the proper operation and stability of the test setup, a control device with known parameter values shall be measured at all operational conditions called for in the test plan. This measurement shall be done either before the insertion of test devices or upon completion of the irradiation after removal of the test devices or both.

3.9.2 Remote testing. Unless otherwise specified, the bias shall be removed and the device leads placed in conductive foam (or similarly shorted) during transfer from the irradiation source to a remote tester and back again for further irradiation. This minimizes post-irradiation time dependent effects.

3.9.3 Bias and loading conditions. Bias conditions for test devices during irradiation or accelerated annealing shall be within ±10 percent of those specified by the test plan. The bias applied to the test devices shall be selected to produce the greatest radiation induced damage or the worst-case damage for the intended application, * if known. While maximum voltage is often worst case some bipolar linear device parameters (e.g. input bias current or maximum output load current) exhibit more degradation with 0 V bias. The specified bias shall be maintained on each device in accordance with the test plan. Bias shall be checked immediately before and after irradiation. Care shall be taken in selecting the loading such that the rise in the junction temperature is minimized.

3.10 Post-irradiation procedure. Unless otherwise specified, the following time intervals shall be observed:

a. * The time from the end of an irradiation to the start of electrical measurements shall be a maximum of 1 hour unless Condition D is used, in which case the maximum time shall be 72 hours.

b. * The time to perform the electrical measurements and to return the device for a subsequent irradiation, if any, shall be within two hours of the end of the prior irradiation unless Condition D is used, in which case the maximum time shall be 120 hours.

To minimize time dependent effects, these intervals shall be as short as possible. The sequence of parameter measurements shall be maintained constant throughout the tests series.

3.11 Extended room temperature anneal test. The tests of 3.1 through 3.10 are known to be overly conservative for some devices in a very low dose rate environment (e.g. dose rates characteristic of space missions). The extended room temperature anneal test provides an estimate of the performance of a device in a very low dose rate environment even though the testing is performed at a relatively high dose rate (e.g. 50-300 rad(Si)/s). The procedure involves irradiating the device per steps 3.1 through 3.10 and post-irradiation subjecting the device under test to a room temperature anneal for an appropriate period of time (see 3.11.2c) to allow leakage-related parameters that may have exceeded their pre-irradiation specification to return to within specification. The procedure is known to lead to a higher rate of device acceptance in cases:

a. where device failure when subjected to the tests in 3.1 through 3.10 has been caused by the buildup of trapped positive charge in relatively soft oxides, and

b. where this trapped positive charge anneals at a relatively high rate.

3.11.1 Need to perform an extended room temperature anneal test. The following criteria shall be used to determine whether an extended room temperature anneal test is appropriate:

a. The procedure is appropriate for either MOS or bipolar technology devices.

b. The procedure is appropriate where only parametric failures (as opposed to functional failure) occurs. The parties to the test shall take appropriate steps to determine that the device under test is subject to only parametric failure over the total ionizing dose testing range.

c. The procedure is appropriate where the natural annealing response of the device under test will serve to correct the out-of-specification of any parametric response. Further, the procedure is known to lead to a higher rate of device acceptance in cases where the expected application irradiation dose rate is sufficiently low that ambient temperature annealing of the radiation induced trapped positive charge can lead to a significant improvement of device behavior. Cases where the expected application dose rate is lower than the test dose rate and lower than 0.1 rad(Si)/s should be considered candidates for the application of this procedure. The parties to the test shall take appropriate steps to determine that the technology under test can provide the required annealing response over the total ionizing dose testing range.

3.11.2 Extended room temperature anneal test procedure. If the device fails the irradiation and testing specified in 3.1 through 3.10, an additional room temperature annealing test may be performed as follows:

a. Following the irradiation and testing of 3.1 through 3.10, subject the device under test to a room temperature anneal under worst-case static bias conditions. For information on worst case bias see 3.9.3,

b. The test will be carried out in such a fashion that the case of the device under test will have a temperature within the range 24°C ± 6°C.

c. Where possible, the room temperature anneal should continue for a length of time great enough to allow device parameters that have exceeded their pre-irradiation specification to return to within specification or post-irradiation- parametric limit (PIPL) as established by the manufacturer. However, the time of the room temperature anneal shall not exceed t_{max}, where

$$t_{max} = \frac{D_{spec}}{R_{max}}$$

D_{spec} is the total ionizing dose specification for the part and R_{max} is the maximum dose rate for the intended use.

d. Test the device under test for electrical performance as specified in 3.7 and 3.8. If the device under test passes electrical performance tests following the extended room temperature anneal, this shall be considered acceptable performance for a very low dose rate environment in spite of having previously failed the post-irradiation and electrical tests of 3.1 through 3.10.

3.12 MOS accelerated annealing test. The accelerated annealing test provides an estimate of worst-case degradation of MOS microcircuits in low dose rate environments. The procedure involves heating the device following irradiation at specified temperature, time and bias conditions. An accelerated annealing test (see 3.12.2) shall be performed for cases where time dependent effects (TDE) can cause a device to degrade significantly or fail. Only standard testing shall be performed as specified in 3.1 through 3.10 for cases where TDE are known not to cause significant device degradation or failure (see 3.12.1) or where they do not need to be considered, as specified in 3.12.1.

3.12.1 Need to perform accelerated annealing test. The parties to the test shall take appropriate steps to determine whether accelerated annealing testing is required. The following criteria shall be used:

a. The tests called out in 3.12.2 shall be performed for any device or circuit type that contains MOS circuit elements (i.e., transistors or capacitors).

b. TDE tests may be omitted if:

1. circuits are known not to contain MOS elements by design, or

2. the ionizing dose in the application, if known, is below 5 krad(Si), or

3. the lifetime of the device from the onset of the irradiation in the intended application, if known, is short compared with TDE times, or

4. the test is carried out at the dose rate of the intended application, or

5. the device type or IC technology has been demonstrated via characterization testing not to exhibit TDE changes in device parameters greater than experimental error (or greater than an otherwise specified upper limit) and the variables that affect TDE response are demonstrated to be under control for the specific vendor processes.

   At a minimum, the characterization testing in (5) shall include an assessment of TDE on propagation delay, output drive, and minimum operating voltage parameters. Continuing process control of variables affecting TDE may be demonstrated through lot sample tests of the radiation hardness of MOS test structures.

c. This document provides no guidance on the need to perform accelerated annealing tests on technologies that do not include MOS circuit elements.

3.12.2 Accelerated annealing test procedure. If the device passes the tests in 3.1 through 3.10 or if it passes 3.11 (if that procedure is used) to the total ionizing dose level specified in the test plan or device specification or drawing and the exclusions of 3.12.1 do not apply, the accelerated annealing test shall be conducted as follows:

a. Overtest.

1. Irradiate each test device to an additional 0.5-times the specified dose using the standard test conditions (3.1 through 3.10). Note that no electrical testing is required at this time.

2. The additional 0.5-times irradiation in 3.12.2.a.1may be omitted if it has been demonstrated via characterization testing that:

a. none of the circuit propagation delay, output drive, and minimum operating voltage parameters recover toward their pre-irradiation value greater than experimental accelerated annealing test of 3.12.2.b, and

b. the irradiation biases chosen for irradiation and accelerated annealing tests are worst-case for the response of these parameters during accelerated annealing.

The characterization testing to establish worst-case irradiation and annealing biases shall be performed at the specified level. The testing shall at a minimum include separate exposures under static and dynamic irradiation bias, each followed by worst-case static bias during accelerated annealing according to 3.12.2.b.

b. Accelerated annealing. Heat each device under worst-case static bias conditions in an environmental chamber according to one of the following conditions:

1. At 100°C ±5°C for 168 ±12 hours, or

2. At an alternate temperature and time that has been demonstrated via characterization testing to cause equal or greater change in the parameter(s) of interest, e.g., propagation delay, output drive, and minimum operating voltage, in each test device as that caused by 3.12.2.b.1, or

3. At an alternate temperature and time which will cause trapped hole annealing of >60% and interface state annealing of <10% as determined via characterization testing of NMOS test transistors from the same process. It shall be demonstrated that the radiation response of test transistors represent that of the device under test.

c. Electrical testing. Following the accelerated annealing, the electrical test measurements shall be performed as specified in 3.8 and 3.9.

* 3.13 Test procedure for Bipolar and BiCMOS linear or mixed signal circuits with agreed to dose rates of less than 50 rad(Si)/s. Many bipolar linear parts exhibit ELDRS, which cannot be simulated with a room temperature 50-300 rad(Si)/s irradiation plus elevated temperature anneal, such as that used for MOS parts (see ASTM-F1892 for more technical details). Parts that exhibit ELDRS shall be tested either at the agreed to dose rate, at a prescribed low dose rate to an overtest radiation level, or with an elevated temperature irradiation test that includes a parameter delta design margin.

* Need to perform low dose rate testing.

* a. The low dose rate tests described in 3.13 may be omitted if:

* 1. circuits are known not to contain bipolar transistors by design, or

* 2. circuits are known not to contain any linear circuit functions by design.

* 3. the device type and IC technology have been demonstrated via characterization testing not to exhibit ELDRS in device parameters greater than experimental error (or greater than an otherwise specified upper limit) and the variables that affect ELDRS response are demonstrated to be under control for the specific vendor processes.

* 3.13.1 Low dose rate or elevated temperature irradiation test for bipolar or BiCMOS linear or mixed-signal circuits. All circuits that do not meet the exception of 3.13.a shall be tested using one of the following test conditions.

Note: The test procedures described in paragraphs b. and c. below represent a compromise between the desire for a conservative, worst-case test and the constraints of test cost, schedule and facilities. For this reason, the test procedures may result in a non-conservative test for some kinds of circuits.

* a. Test at the agreed to dose rate. Irradiate each test device at the dose rate described in 3.6.3 Condition C using the standard test conditions (3.1 through 3.10).

* b. Test at a prescribed low dose rate. Irradiate each test device at the dose rate described in 3.6.4 Condition D using the standard test conditions (3.1 through 3.10) with the following additional requirements:

* 1. If the dose rate is $\leq$ 10 mrad(Si)/s, an overtest factor of 1.5 shall be applied to the radiation test level, i.e. the part must pass at a radiation level of 1.5 times the specification dose to be acceptable.

* 2. If the dose rate is greater than 10 mrad(Si)/s, an overtest factor of 2.0 shall be applied to the radiation test level, i.e. the part must pass at a radiation level of 2.0 times the specification dose to be acceptable.

* c. Test at an elevated temperature. Irradiate each test device at the dose rate described in 3.6.5 Condition E using the standard test conditions (3.1 through 3.10) with the following additional requirements:

* 1. The irradiation temperature shall be 100°C ± 5°C using an irradiation test chamber as described in paragraph 2.8. Every effort shall be made to minimize the time at temperature.
* 2. The elevated temperature irradiation test shall only be used for parts with a specification dose of 50 krad(Si) or less.
* 3. All pre and post irradiation electrical measurements shall be made at a temperature of 24°C ±6°C.
* 4. A parameter delta design margin of 3 shall be applied at the specification dose to all critical electrical parameters in the following manner. The change in each electrical parameter shall be calculated for each sample at the specification dose. This change in the parameter shall be multiplied by 3 and added (or subtracted) to the post irradiation parameter value for each sample. This value shall be compared to the allowable degraded value of the parameter to determine whether the sample passes or fails the test.

* 3.14 Test report. As a minimum, the report shall include the device type number, serial number, the manufacturer, package type, controlling specification, date code, and any other identifying numbers given by the manufacturer. The bias circuit, parameter measurement circuits, the layout of the test apparatus with details of distances and materials used, and electrical noise and current leakage of the electrical measurement system for in-flux testing shall be reported using drawings or diagrams as appropriate. Each data sheet shall include the test date, the radiation source used, the bias conditions during irradiation, the ambient temperature around the devices during irradiation and electrical testing, the duration of each irradiation, the time between irradiation and the start of the electrical measurements, the duration of the electrical measurements and the time to the next irradiation when step irradiations are used, the irradiation dose rate, electrical test conditions, dosimetry system and procedures and the radiation test levels. The pre- and post-irradiation data shall be recorded for each part and retained with the parent population data in accordance with the requirements of MIL-PRF-38535 or MIL-PRF-38534. Any anomalous incidents during the test shall be fully documented and reported. The accelerated aging annealing procedure, if used, shall be described. Any other radiation test procedures or test data required for the delivery shall be specified in the device specification, drawing or purchase order.

4. SUMMARY. The following details shall be specified in the applicable acquisition document as required:

a. Device-type number(s), quantity, and governing specifications (see 3.1).

b. Radiation dosimetry requirements (see 3.3).

c. Radiation test levels including dose and dose rate (see 3.5 and 3.6).

d. Irradiation, electrical test and transport temperatures if other than as specified in 3.7.

e. Electrical parameters to be measured and device operating conditions during measurement (see 3.8).

f. Test conditions, i.e., in-flux or not-in-flux type tests (see 3.9).

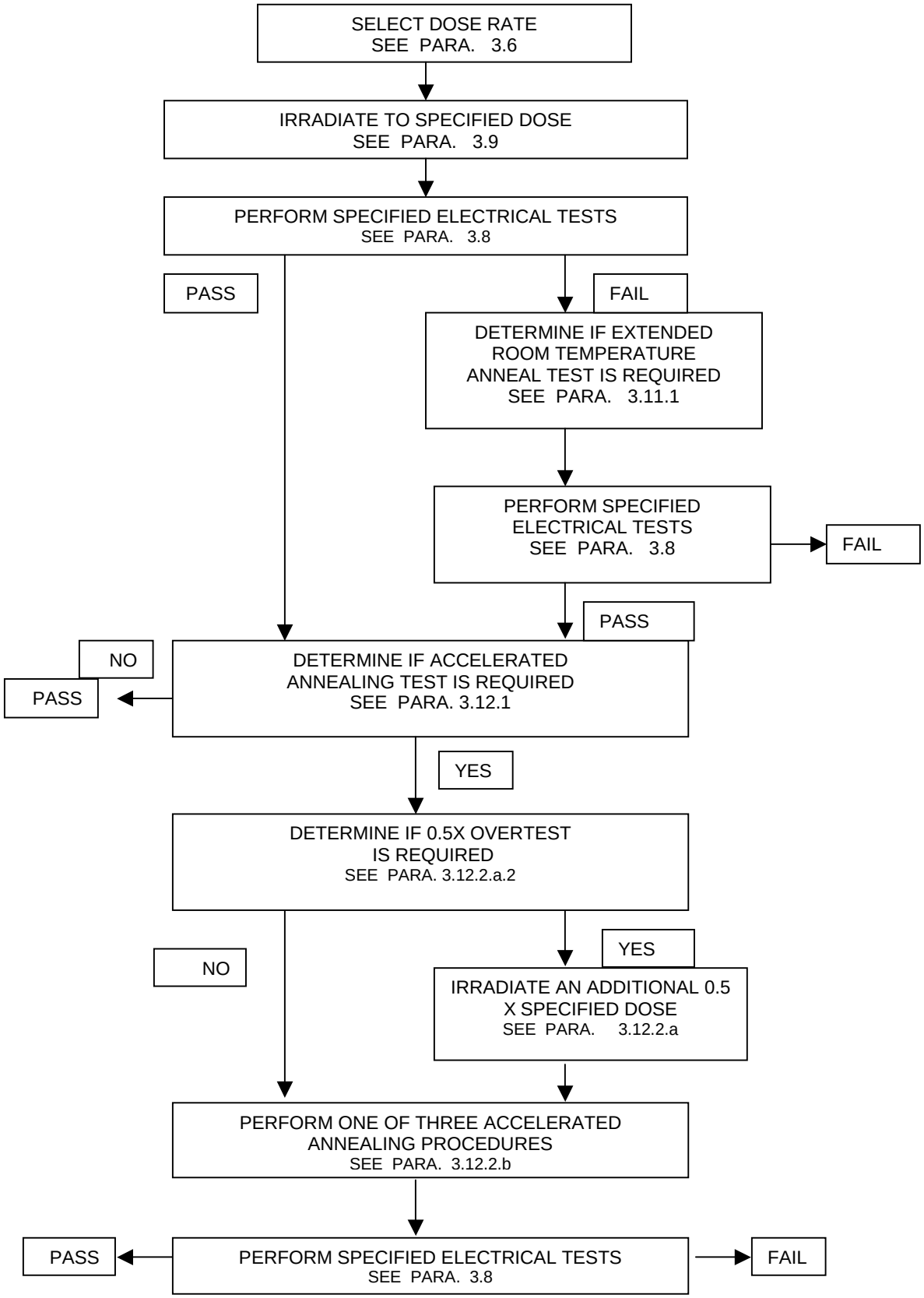
g. Bias conditions for devices during irradiation (see 3.9.3).

h. Time intervals of the post-irradiation measurements (see 3.10).

i. Requirement for extended room temperature anneal test, if required (see 3.11).

j. Requirement for accelerated annealing test, if required (see 3.12).

* k. Documentation required to be delivered with devices (see 3.14).



* Figure 1019-1. Flow diagram for ionizing radiation test procedure for MOS and digital bipolar circuits

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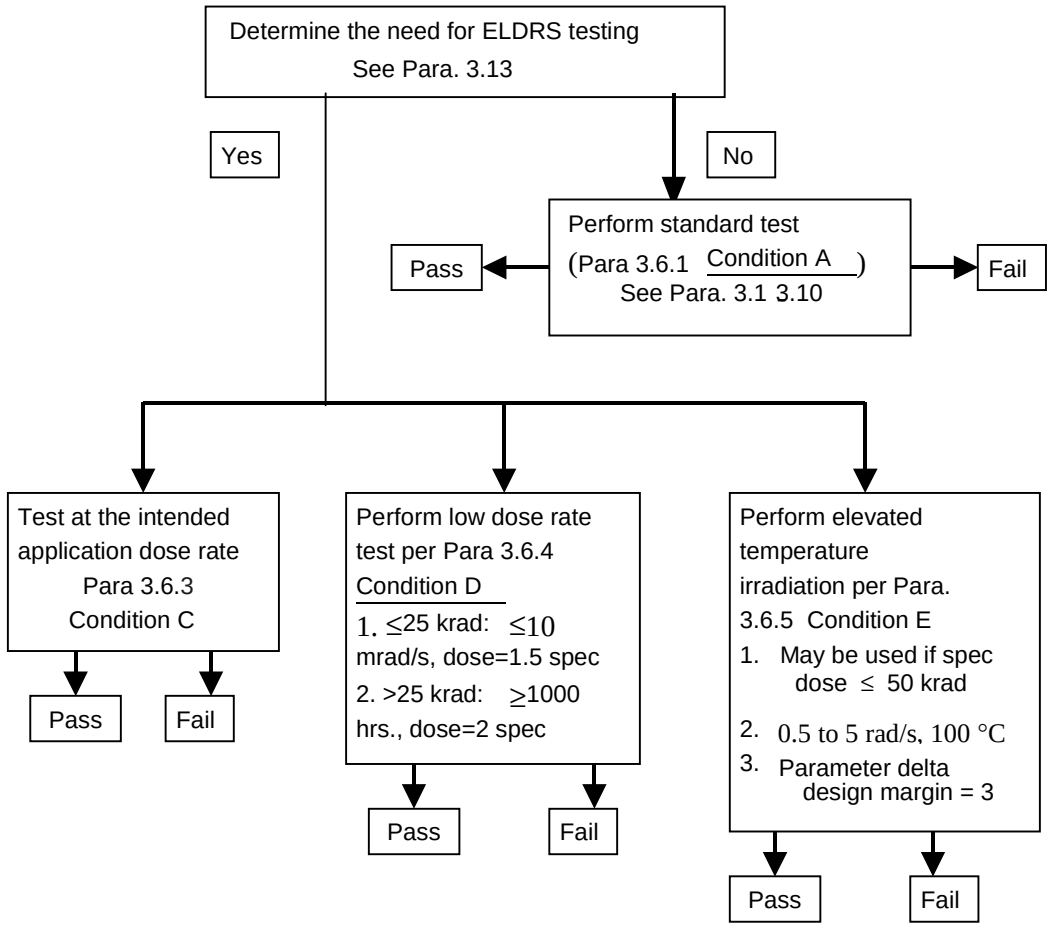

* Figure 1019-2. Flow diagram for Ionizing radiation test procedure for bipolar (or BiCMOS) linear or mixed-signal circuits

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f. Definitions:

(1) Active circuit area. All areas enclosed by the perimeter of functional circuit elements, operating metallization or any connected combinations thereof excluding beam leads.

(2) Coupling (air) bridge. A raised layer of metallization used for interconnection that is isolated from the surface of the element.

(3) Block resistor. A thin film resistor which for purposes of trimming is designed to be much wider than would be dictated by power density requirements and shall be identified in the approved manufacturer's precap visual implementation document.

* (4) Contact Via. The Via where dielectric material is etched away in order to expose the Under Bump Metalization (UBM) on the bond pads or solder bump attach pads.

* (5) Channel. An area lying between the drain and the source of FET structures.

* (6) Controlled environment. Shall be class 1,000, (see 40.8.1.1.7 of appendix A of MIL-PRF-38535), except that the maximum allowable relative humidity shall not exceed 65 percent.

* (7) Crazing. The presence of numerous minute cracks in the referenced material, (e.g., glassivation crazing).

* (8) Detritus. Fragments of original or laser modified resistor material remaining in the kerf.

* (9) Die coat. A thin layer of soft polyimide coating applied to the surface of a semiconductor element that is intended to produce stress relief resulting from encapsulation and to protect the circuit from surface scratches.

* (10) Dielectric isolation. Electrical isolation of one or more elements of a monolithic semiconductor integrated circuit by surrounding the elements with an isolating barrier such as semiconductor oxide.

* (11) Dielectric layer or layers. Dielectric layer or layers deposited on the die surface to protect the redistribution metalization, and to create the contact via for solder bump pad.

* (12) Diffusion tub. A volume (or region) formed in a semiconductor material by a diffusion process (n- or p- type) and isolated from the surrounding semiconductor material by a n-p or p-n junction or by a dielectric material (dielectric isolation, coplanar process, SOS, SOI).

* (13) Foreign material. Any material that is foreign to the microcircuit or package, or any nonforeign material that is displaced from its original or intended position within the microcircuit package.

* (14) Functional circuit elements. Diodes, transistors, crossunders, capacitors, and resistors.

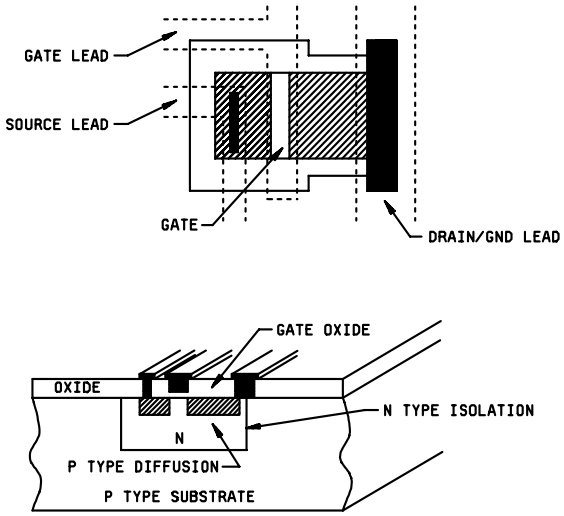

FIGURE 2010-1. P channel MOS transistor.

* (15) Gate oxide. The oxide or other dielectric that separates gate metallization (or other material used for the gate electrode) from the channel of MOS structures (see figure 2010-1).

* (16) Glassivation. The top layer(s) of transparent insulating material that covers the active circuit area, with the exception of bonding pad areas and beam leads.

* (17) Glassivation cracks. Fissures in the glassivation layer.

* (18) Junction line. The outer edge of a passivation step that delineates the boundary between "P" and "N" type semiconductor material. An active junction is any P/N junction intended to conduct current during normal operation of the circuit element, (e.g., collector to base).

* (19) Kerf. That portion of the component area from which material has been removed or modified by trimming or cutting.

* (20) Line of separation. Visible distance or space between two features that are observed not to touch at the magnification in use.

* (21) MESFET. (Metal semiconductor field-effect transistor). A field-effect transistor in which a metal semiconductor rectifying contact is used for the gate electrode. Typically the structure is fabricated in gallium arsenide and the term GaAs MESFET may be used. Both depletion-type and enhancement type devices have been manufactured. The acronyms are D-MESFET, and E-MESFET, respectively.

* (22) Metallization nonadherence. Unintentional separation of material from an underlying substrate excluding air bridges and undercutting by design.

* (23) Multilayered metallization (conductors). Two or more layers of metal or any other material used for interconnections that are not isolated from each other by insulating material. The term "underlying metal" shall refer to any layer below the top layer of metal (see figure 2010-2).

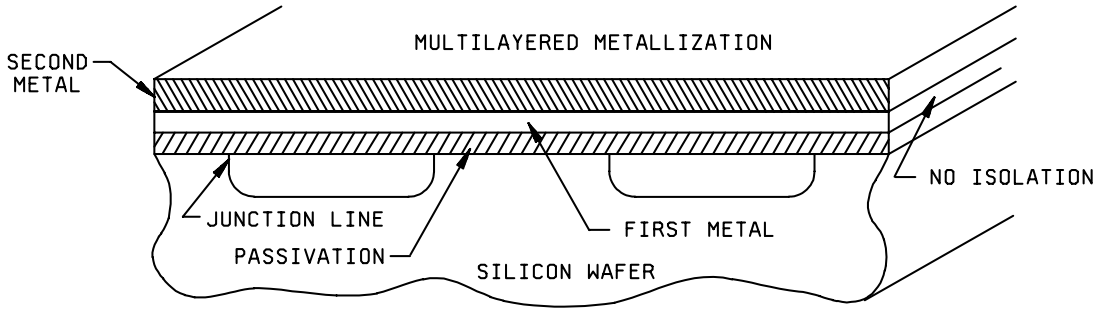

FIGURE 2010-2. Multilayered metallization.

* (24) Multilevel metallization (conductors). Two or more levels of metal or any other material used for interconnections that are isolated from each other by insulating material (also referred to as interlevel dielectric) (see figure 2010-3).

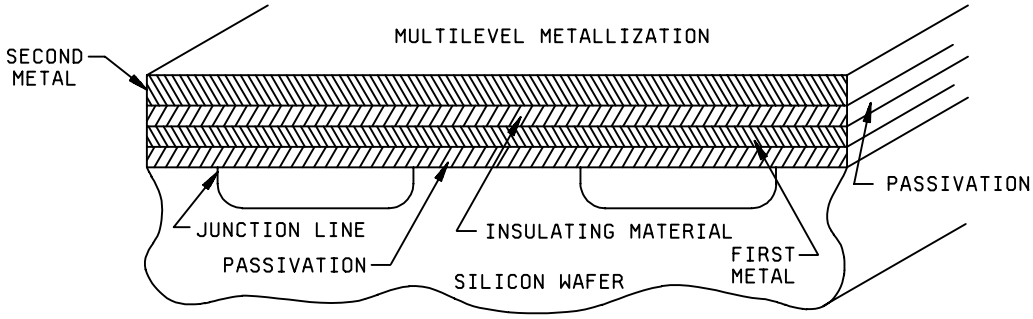

FIGURE 2010-3. Multilevel metallization.

* (25) Narrowest resistor width. The narrowest portion of a given resistor prior to trimming.

* (26) Operating metallization (conductors). Metal or any other material used for interconnection except metallized scribe lines, test patterns, unconnected functional circuit elements, unused bonding pads, and identification markings.

* (27) Original width. The width dimension or distance that would have been present, in the absence of the observed abnormality (e.g., original metal width, original diffusion width, original beam width, etc.).

* (28) Package post. A generic term used to describe the bonding location on the package.

* (29) Passivation. The silicon oxide, nitride or other insulating material that is grown or deposited directly on the die prior to the deposition of metal or between metal levels on multilevel devices.

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* (30) Passivation step. An abrupt change of elevation (level) of the passivation such as a contact window, or operating metallization crossover.

* (31) Peripheral metal. All metal that lies immediately adjacent to or over the scribe grid.

* (32) Redistribution Layer (RDL). Layer added to original wafer/die surface to allow for the redistribution of bond pads into a format more suitable to flip chip.

* (33) Redistribution metalization. The metal deposited on the RDL to create the electrical conductors which connect the original bond pads to the redistributed solder bump pads.

* (34) Shooting metal. Metal (e.g., aluminum, gold) expulsion of various shapes and lengths from under the wire bond at the bonding pad.

* (35) Solder ball. Solder ball or sphere attached to the UBM through the contact via after a re-flow process.

* (36) Solder Bump. Solder that is either electroplated or screened into the photo resist opening. After the photo resist is removed the solder resembles a bump before it is reflowed into ball or sphere.

* (37) Substrate. The supporting structural material into or upon which or both the passivation, metallization and circuit elements are placed.

* (38) Substrate via. A small hole formed through the wafer and metallized, causing electrical connection to be made from the frontside (the side on which the circuitry is formed) to the backside of the wafer.

* (39) Thick film. That conductive/resistive/dielectric system that is a film having greater than 50,000Å thickness.

* (40) Thin film. That conductive/resistive/dielectric system that is a film equal to or less than 50,000Å in thickness.

* (41) Under Bump Metalization (UBM). Metals deposited on top of the aluminum bond pads or on the solder bump pads that enhance wetting and protect against intermetalic reactions between the solder and the original metal on the pads.

* (42) Via metallization. That which connects the metallization of one level to another.

g. Interpretations. Reference herein to "that exhibits" shall be considered satisfied when the visual image or visual appearance of the device under examination indicates a specific condition is present and shall not require confirmation by any other method of testing. When other methods of test are to be used for confirming that a reject condition does not exist, they shall be approved by the acquiring activity. For inspections performed on the range of 75X to 100X, the criteria of 0.1 mil of passivation, separation or metal can be satisfied by a line of separation or a line of metal visible.

h. Foreign material control. The manufacturer shall perform an audit on a weekly basis for (1) the presence of foreign material within incoming piece part lids and bases, and (2) the presence of foreign material on the die surface or within the package of assembled parts.

The audit of assembled parts may be satisfied during routine internal visual inspection. If the presence of foreign material is discovered, the manufacturer shall perform the necessary analysis on a sample of the foreign material on the suspect devices to determine the nature of the material. The manufacturer shall document the results of this investigation and corrective action to eliminate the foreign material and this information will be available to the Government QAR, and the acquiring activity or the qualifying activity, as applicable. A corrective action plan shall be obtained within a maximum of 10 working days of discovery.

The audit of incoming piece part lids and bases shall be performed before parts are assembled, or may be satisfied during routine incoming quality inspection. If the presence of foreign material of a size 1 mil or greater is discovered, the manufacturer will analyze the foreign material to determine its nature and document the results of the analysis. If applicable, these results shall be distributed to the vendor supplying the parts, with the request that the vendor document corrective actions to minimize or eliminate such foreign material. This information will be available to the manufacturer, Government QAR, and the acquiring activity or qualifying activity, as applicable.

Condition A Class level S	Condition B Class level B

h. Bonds where more than 25 percent of the bond is located on die mounting material.

i. Any evidence of repair of conductors by bridging with additional material.

j. Bonds on foreign material.

k. Intermetallic formation extending radially more than 0.1 mil completely around the periphery of that portion of the gold bond located on metal.

3.2.1.5 Rebonding of monolithic devices. Rebonding of monolithic microcircuits, may be done with the following limitations. No device shall be acceptable that exhibits:

a. Rebond over exposed passivation or over metal which shows evidence of peeling. More than one rebond attempt at any design bond location. Rebonds that touch an area of exposed oxide caused by lifted metal.

b. A bond on top of, or partially on top of, another bond, bond wire tail, or residual segment of wire.	b. Bond along side or partially on top of another bond, bond wire tail or residual segment of wire, when the overlap width is greater than 25 percent.

c. Rebond attempts that exceed 10 percent of the total number of bonds in the microcircuit. (e.g., for a 28 lead wire bonded package there are 56 bonds. A bond of one end of a wire shall count as a single attempt. A replacement of a wire bonded at both ends, counts as two rebond attempts.)

NOTE: For class level B only. Bond-offs required to clear the bonder after an unsuccessful first bond attempt are not considered as rebonds provided they can be identified as bond-offs.

d. Missing or extra wires.

* 3.2.1.6 Flip chip solder bump die. No solder bumped die shall be acceptable that exhibit any of the following characteristics (see figure 2010.34A):

a. Missing solder ball from original design position.
b. Solder ball 20% smaller, or larger than design size (nominal).
c. Solder balls bridging.
d. Any attached or embedded foreign material bridging balls, or redistribution metalization.
e. Misaligned solder ball which exposes the UBM on the contact via.
f. Voids in redistribution metalization greater the 50% of the design width.
g. Any redistribution metalization bridging.
h. Any residual unetched UBM bridging balls or redistribution metalization.
i. Mechanical damage to the ball which reduces the original height or diameter more than 20%.
j. Lifting, or peeling of the RDL or dielectric material.

* Note: Minor damage to the solder ball and bump misalignment can be reworked by performing a re-flow/refresh of the solder balls.

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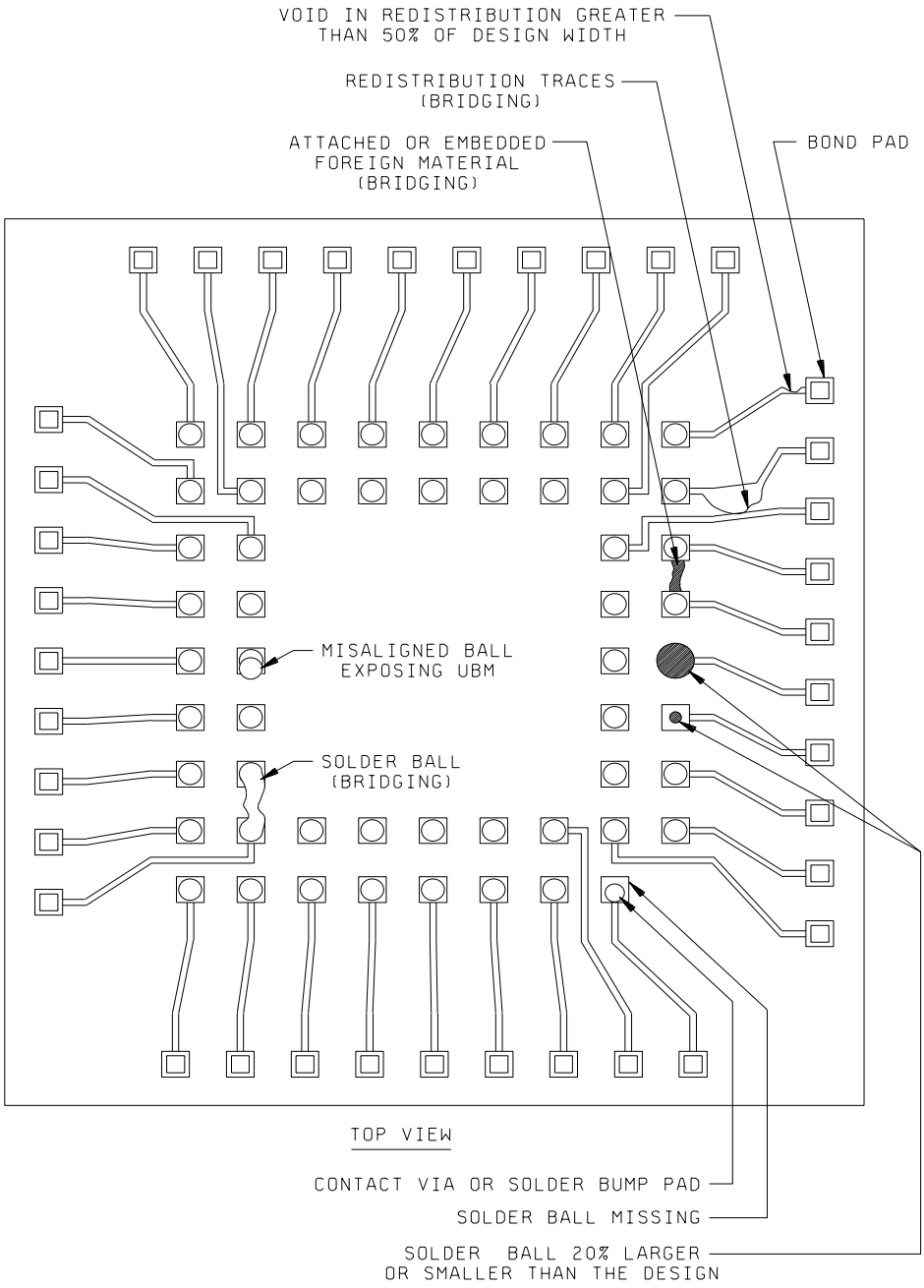

* Figure 2010.34A – FLIP CHIP VISUAL INSPECTION DIAGRAM

New Page

Condition A Class level S	Condition B Class level B

3.2.2 Internal wires. During inspection for the requirements of 3.2.2, each device shall be viewed at any angle necessary to determine full compliance to this specification, without damaging the device. No device shall be acceptable that exhibits:

a. Any wire with a separation of less than two wire diameters to unglassivated operating metal,other bonds, another wire (common wires excluded),other package post, unglassivated die area (except for wires or pads which are at the die or substrate potential), or any portion of the package including the plane of the lid to be attached.	a. Any wire with a separation of less than one wire diameter to unglassivated operating metal, other bonds, another wire (common wires excluded), other package post, unglassivated die area (except for wires or pads which are at the die or substrate potential), or any conductive portion of the package or the plane of the lid to be attached.
NOTE: For condition A only. Within a 5.0 mil radial distance from the perimeter of the bond on the die the separation shall be 1.0 mil minimum.	NOTE: For condition B only. Within a 10.0 mil radial distance from the perimeter of the bond on the die a line of separation must be visible.

NOTE: For SOS devices, exclude the unglassivated insulator areas.

b. Nicks, bends, cuts, crimps, scoring, or neckdown in any wire that reduces the wire diameter by more than 25 percent.

c. Tearing at the junction of the wire and bond.

d. Any wire making a straight line run from a die bonding pad to a package post that has no arc.

Condition A Class level S	Condition B Class level B

3.2.5.1 Foreign material, die coated devices. This inspection and criteria shall be required on all devices that receive a die coat during the assembly process. This inspection will be done after die coat cure. No device shall be acceptable that exhibits:

a. Unattached foreign particles on the surface of the die coat or within the package that is (are) large enough to bridge the narrowest spacing between unglassivated operating material (e.g., metallization, bare semiconductor material, mounting material, bonding wire, etc.). Note: Semiconductor particles shall be considered as foreign material.

b. Partially embedded foreign material with an "unembedded portion" that is large enough to bridge the narrowest spacing between unglassivated operating material (e.g., metallization, bare semiconductor material, mounting material, bonding wire, etc.).

c. Foreign material attached to or embedded in the die coat that appears to bridge unglassivated operating material when viewed from above (e.g., bare semiconductor material, bond pads, bonding wire, mounting material, etc.).

* d. Embedded foreign particles that penetrate the entire thickness of the die coating.

* 3.2.5.1.1 Die coating material. No device shall be accepted that exhibits:

* a. Surface scratches that penetrate the die coating and expose underlying glassivated metal.

* b. Die coating that is lifted or is peeling from the semiconductor surface.

3.2.6 GaAs backside metallization. GaAs inspection shall be performed with low magnification prior to die mounting. (Verification at high magnification is permitted.) With the approval of the acquiring activity, the manufacturer may substitute a sample inspection plan at the wafer level for 100 percent inspection in dice form. The sample inspection plan shall be documented in the manufacturer's baseline documentation and shall be performed to the requirements of test method 5013. No devices shall be acceptable that exhibit the following.

a. Evidence of metal corrosion, lifting, peeling, blistering.

b. Voids or scratches that expose underlying metal or substrate whose cumulative areas are more than 25 percent of the cell area or device area.

NOTE: Absence of gold in the die separation area (saw street) of devices with electroplated backside metallization is not a cause for rejection. Small voids at edges due to die separation are acceptable if they comprise less than 10 percent of the backside area.

c. Any voids or scratches in the substrate via metallization that effects more than 25 percent of the metallization or cause unintended isolation of the metallization path.

d. Underetched vias.

e. Overetched vias.

4. SUMMARY. The following details shall be specified in the applicable acquisition document.

a. Test condition (see 3).

b. Where applicable, any conflicts with approved circuit design topology or construction.

c. Where applicable, gauges, drawings, and photographs that are to be used as standards for operator comparison (see 2).

d. Where applicable, specific magnification (see 3).

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METHOD 2019.7

DIE SHEAR STRENGTH

1. PURPOSE. The purpose of this test is to determine the integrity of materials and procedures used to attach semiconductor die or surface mounted passive elements to package headers or other substrates. This determination is based on a measure of force applied to the die, the type of failure resulting from this application of force (if failure occurs) and the visual appearance of the residual die attach media and substrate/header metallization.

2. APPARATUS. The test equipment shall consist of a load-applying instrument with an accuracy of ±5 percent of full scale or 50 grams, whichever is the greater tolerance. A circular dynamometer with a lever arm or a linear motion force-applying instrument may be used to apply the force required for testing. The test equipment shall have the following capabilities:

* a. A die contact tool which applies a uniform distribution of the force to an edge of the die (see figure 2019-1). A compliant (conforming) material (e.g., nail polish, tape, etc.) may be applied to the face of the contact tool to ensure uniform force distribution on the edge of the die.

b. Provisions to assure that the die contact tool is perpendicular to the die mounting plane of the header or substrate.

c. A rotational capability, relative to the header/substrate holding fixture and the die contact tool, to facilitate line contact on the edge of the die; i.e., the tool applying the force to the die shall contact the die edge from end-to-end (see figure 2019-2).

d. A binocular microscope with magnification capabilities of 10X minimum and lighting which facilitates visual observation of the die and die contact tool interface during testing.

3. PROCEDURE. The test shall be conducted, as defined herein, or to the test conditions specified in the applicable specific acquisition document consistent with the particular part construction. All die strength tests shall be counted and the specific sampling, acceptance, and added sample provisions shall be observed, as applicable.

3.1 Shear strength. A force sufficient to shear the die from its mounting or equal to twice the minimum specified shear strength (figure 2019-4), whichever occurs first, shall be applied to the die using the apparatus of 2 above.

* NOTE: For passive elements only attached at the end terminations, the area used to determine the force applied shall be the total area of the mounting surface of the end terminations. An area between end terminations filled with non-adhering filler shall not be used to determine the force applied. However, any adhering material applied between the end terminations shall be used in the shear calculation. If the area between end terminations contains an adhering material, then the area of the adhering material shall be added to the area of the mounting surfaces of the end terminations and that total area shall be used to determine the force applied.

a. When a linear motion force-applying instrument is used, the direction of the applied force shall be parallel with the plane of the header or substrate and perpendicular to the die being tested.

b. When a circular dynamometer with a lever arm is employed to apply the force required for testing, it shall be pivoted about the lever arm axis and the motion shall be parallel with the plane of the header or substrate and perpendicular to the edge of the die being tested. The contact tooling attached to the lever arm shall be at a proper distance to assure an accurate value of applied force.

c. The die contact tool shall apply a force gradually from zero to a specified value against an edge of the die which most closely approximates a 90° angle with the base of the header or substrate to which it is bonded (see figure 2019-3). For rectangular die, the force shall be applied perpendicular to the longer side of the die. When constrained by package configurations, any available side of the die may be tested if the above options are not available.

d. After initial contact with the die edge and during the application of force, the relative position of the contact tool shall not move vertically such that contact is made with the header/substrate or die attach media. If the tool rides over the die, a new die may be substituted or the die may be repositioned, provided that the requirements of 3.1.c are met.

3.2 Failure criteria. A device which fails any of the following criteria shall constitute a failure.

* NOTE: (See examples for determining DIE AREA following figure 2019-4.)

a. Fails die strength requirements (1.0X) of figure 2019-4.

b. Separation with less than 1.25 times the minimum strength (1.0X) specified in figure 2019-4 and evidence of less than 50 percent adhesion of the die attach medium.

c. Separation with less than 2.0 times the minimum strength (1.0X) specified in figure 2019-4 and evidence of less than 10 percent of adhesion of the die attach medium.

* NOTE: Residual silicon attached in discrete areas of the die attach medium shall be considered as evidence of adhesion. For metal glass die attach, die attach material on the die and on the package base shall be considered as evidence of acceptable adhesion.

3.2.1 Separation categories. When specified, the force required to achieve separation and the category of the separation shall be recorded.

a. Shearing of die with residual silicon remaining.

b. Separation of die from die attach medium.

c. Separation of die and die attach medium from package.

4. SUMMARY. The following details shall be specified in the applicable acquisition document.

a. Minimum die attach strength if other than shown on figure 2019-4.

b. Number of devices to be tested and the acceptance criteria.

c. Requirement for data recording, when applicable (see 3.2.1).

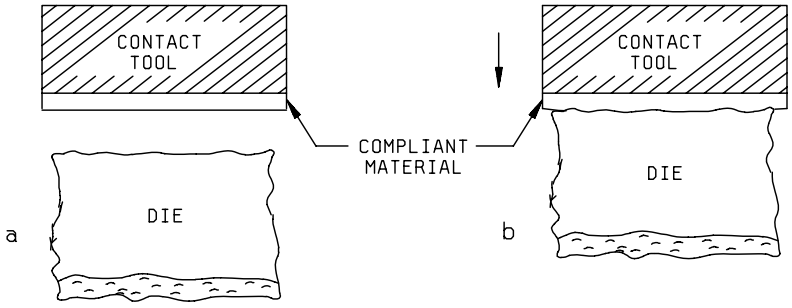


FIGURE 2019-1. Compliant interface on contact tool distributes load to the irregular edge of the die.

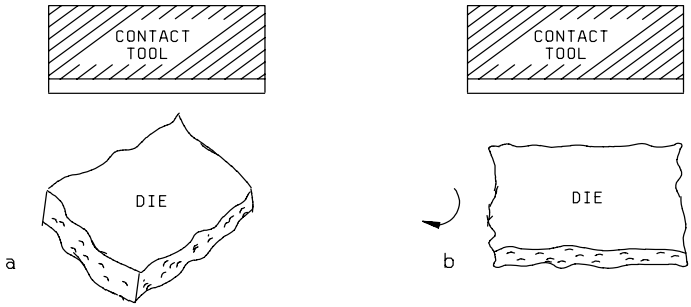


FIGURE 2019-2. Rotate the die contact tool or the device for parallel alignment.

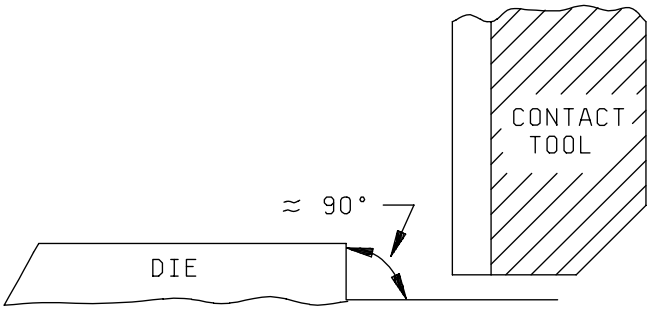
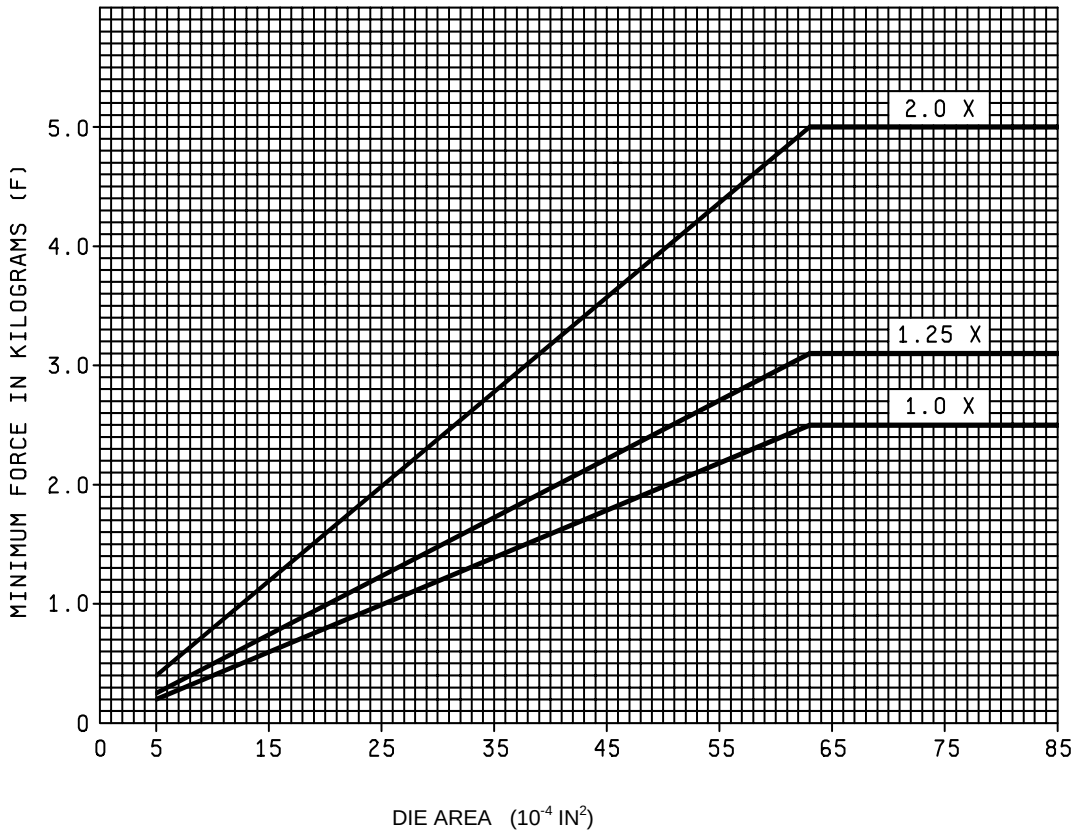


FIGURE 2019-3. The contact tool shall load against that edge of the die which forms an angle ≈ 90° with the header/substrate.



NOTES:

1. All die area larger than 64 x 10^{-4} $(IN)^2$ shall withstand a minimum force of 2.5 kg or a multiple thereof (see 3.2).

* 2. All die area larger than or equal to 5 x 10^{-4} $(IN)^2$ but smaller than or equal to 64 x 10^{-4} $(IN)^2$ shall withstand a minimum force as determined from the chart of Figure 2019.4.

* 3. All die area smaller than 5 x 10^{-4} $(IN)^2$ shall withstand a minimum force (1.0X) of 0.04 kg/10^{-4} $(IN)^2$ or a minimum force (2X) of 0.08 kg/10^{-4} $(IN)^2$.

FIGURE 2019-4. Die shear strength criteria (minimum force versus die attach area).

* Examples of determining die strength requirements based on die area.

* Example 1:

Die Area of device measuring .02 inches by .02 inches.

Die Size = .02 X .02 = .0004 IN^2 = 4 X 10^{-4} (IN^2).

Because die size is less than 5 X 10^{-4} (IN^2) use Note 3 which states the value of minimum force required is 0.04 kg/10^{-4} (IN^2) at (1X), 0.05 kg/10^{-4} (IN^2) at (1.25X), or 0.08 kg/10^{-4} (IN^2) at (2X). Thus the associated minimum forces required are 0.16 kg, 0.20 kg and 0.32 kg, respectively.

* Example 2:

Die Area of device measuring .04 inches by 0.04 inches.

Die Size = .04 X .04 = .0016 IN^2 = 16 X 10^{-4} (IN^2).

Because die size is between 5 X 10^{-4} (IN^2) and 64 X 10^{-4} (IN^2) use Note 2 which states the value of minimum force required is to be determined based on the chart. The values for die size 16 X 10^{-4} (IN^2) are found on the chart by reading 16 on the (10^{-4} IN^2) scale, then finding the coordinating force value on the (F) scale. Doing so provides minimum forces required as .64 kg at (1X), .80 kg at (1.25X), and 1.28 kg at (2X).

* Example 3:

Die Area of device measuring .09 inches by .09 inches.

Die Size = .09 X .09 = .0081 IN^2 = 81 X 10^{-4} (IN^2).

Because die size is larger than 64 X 10^{-4} (IN^2) use Note 1 which states the value of minimum force required is 2.5 kg or a multiple thereof. Therefore, the minimum forces required are 2.5 kg at (1X), 3.125 kg at (1.25X), and 5.0 kg at (2X).

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