This document and process conversion measures necessary to comply with this change shall be completed by 16 March 2020.

INCH - POUND

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16 September 2019
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3 May 2018

DEPARTMENT OF DEFENSE

TEST METHOD STANDARD

TEST PROCEDURES FOR MICROCIRCUITS

PART 5: TEST METHODS 5000-5999

AMSC N/A

FSC 5962

DISTRIBUTION STATEMENT A. Approved for public release. Distribution is unlimited.

FOREWORD

1. This standard is approved for use by all Departments and Agencies of the Department of Defense.

2. This entire standard has been revised. This revision has resulted in many changes to the format, but the most significant one is the splitting the document into parts. See MIL–STD–883 for the change summary.

3. Comment, suggestions, or questions on this document should be addressed to: Commander, Defense Logistics Agency, ATTN: DLA Land and Maritime - VA, P.O. Box 3990, Columbus, OH 43218-3990, or by email to STD883@dla.mil. Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at: https://assist.dla.mil/.

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METHOD NO. TEST PROCEDURES

1. SCOPE

1.1 Purpose. Part 5 of this test method standard establishes uniform test methods for the electrical testing (digital) to determine resistance to deleterious effects of natural elements and conditions surrounding military operations. For the purpose of this standard, the term "devices" includes such items as monolithic, multichip, film and hybrid microcircuits, microcircuit arrays, and the elements from which the circuits and arrays are formed. This standard is intended to apply only to microelectronic devices.

1.2 Numbering system. The test methods are designated by numbers assigned in accordance with the following system:

1.2.1 Classification of tests. The test procedures included in this part of a multipart test method standard are numbered 5001 to 5013 inclusive.

1.2.2 Test method revisions. Revisions are numbered consecutively using a period to separate the test method number and the revision number. For example, 5001.2 designates the second revision of test method 5001.

2. APPLICABLE DOCUMENTS

2.1 General. The documents listed in this section are specified in sections 3, 4, and 5 of this standard. This section does not include documents cited in other sections of this standard or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements documents cited in sections 3, 4, and 5 of this standard, whether or not they are listed.

2.2 Government documents.

2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

MIL-PRF-680	-	Degreasing Solvent, Performance Specification For.
MIL-PRF-19500	-	Semiconductor Devices, General Specification For.
MIL-PRF-38534	-	Hybrid Microcircuits, General Specification For.
MIL-PRF-38535	-	Integrated Circuits (Microcircuits) Manufacturing, General Specification For.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-202	-	Electronic and Electrical Component Parts.
MIL-STD-750	-	Test Methods for Semiconductor Devices.
MIL-STD-1686	-	Electrostatic Discharge Control Program for Protection of Electrical and Electronic Parts, Assemblies and Equipment (Excluding Electrically Initiated Explosive Devices).
MIL-STD-1835	-	Electronic Component Case Outlines.
MIL-STD-1916	-	DOD Preferred Methods for Acceptance of Product.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-217	-	Reliability Prediction of Electronic Equipment.
MIL-HDBK-505	-	Definitions of Item Levels, Item Exchangeability, Models, and Related Terms.
MIL-HDBK-781	-	Reliability Test Methods, Plans, and Environments for Engineering, Development Qualification, and Production .
MIL-HDBK-1331	-	Parameters to be Controlled for the Specification of Microcircuits.

FEDERAL STANDARDS

SAE AMS-STD-595	-	Colors Used in Government Procurement
SAE AMS-STD-595/15102	-	Blue, Gloss
SAE AMS-STD-595/25102	-	Blue, Semi-gloss

OTHER GOVERNMENT DOCUMENTS, DRAWINGS, AND PUBLICATIONS

QML-38534	-	Hybrid Microcircuits, General Specification For.
QML-38535	-	Integrated Circuits (Microcircuits) Manufacturing, General Specification For.

COMMERCIAL ITEM DESCRIPTIONS

A-A-58092	-	Tape, Antiseize, Polytetrafluorethylene.

(Copies of these documents are available online at https://assist.dla.mil.)

2.3 Non-Government publications. The following documents form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

INTERNATIONAL ORGANIZATION FOR STANDARDIZATION (ISO) STANDARDS

ISO 14644-1	-	Cleanrooms and Associated Controlled Environments – Part 1: Classification of Air Cleanliness.
ISO 14644-2	-	Cleanrooms and Associated Controlled Environments – Part 2: Specifications for Testing and Monitoring to Prove Continued Compliance with ISO 14644-1.
ISO /ASTM 51275	-	Standard Practice for Use of a Radiochromic Film Dosimetry System.

(Copies of these documents are available online at https://www.iso.org)

AMERICAN NATIONAL STANDARDS INSTITUTE (ANSI)

ANSI/NCSL Z540.3	-	Requirements for the Calibration of Measuring and Test Equipment, General Requirements.

(Copies of these documents are available online at https://ansi.org)

IPC - ASSOCIATION CONNECTING ELECTRONICS INDUSTRIES (IPC)

IPC J-STD-004	-	Requirements for Soldering Fluxes.
IPC J-STD-005	-	Requirements for Soldering Pastes.
IPC J-STD-006	-	Requirements for Electronic Grade Solder Alloys and Fluxed and Non-fluxed Solid Solders for Electronic Soldering Applications.
IPC J-STD-033	-	Handling, Packing, Shipping and Use of Moisture/Reflow Sensitive Surface Mount Devices.
IPC-T-50	-	Terms and Definitions for Interconnecting and Packaging Electronic Circuits.

(Copies of these documents are available online at https://www.ipc.org)

JEDEC SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC).

JEDEC JESD22-B116	- Wire Bond Shear Test
JEDEC JESD78	- IC Latch-up Test.
JEDEC JESD213	- Common Test Method for Detection Component Surface Finish Material.
JEDEC Standard 12	- Standard for Gate Array Benchmark Set
JEDEC Standard 12-1	- Terms and Definitions for Gate Array Benchmark Set.
JEDEC Standard 12-2	- Standard for Cell-Based Integrated Circuit Benchmark Set.
JEDEC Standard 12-3	- CMOS Gate Array Macrocell Standard.

(Copies of these documents are available online at https://www.jedec.org)

NATIONAL COUNCIL ON RADIAATION PROTECTION AND MEASUREMENT

Report Number 40 - Protection Against Radiation from Brachytherapy Sources
Report Number 102 - Medical X-ray, Electron Beam and Gamma Ray Protection

(Copies of these documents are available online at http://www.NCRPPublications.org)
TECHSTREET THOMPSON REUTERS

TechAmerica EIA-557 - Statistical Process Control Systems.

(Copies of these documents are available online at https://www.techstreet.com)

AMERICAN SOCIETY FOR TESTING AND MATERIALS (ASTM)

ASTM C 177 - Standard Test Method for Steady-State Heat Flux Measurements and Thermal Transmission Properties by Means of the Guarded Hot-Plate Apparatus.
ASTM C 518 - Standard Test Method for Steady-State Heat Flux Measurements and Thermal Transmission Properties by Means of the Heat Flow Meter Apparatus.
ASTM D 150 - Standard Test Methods for A-C Loss Characteristics and Permittivity (Dielectric Constant) of Solid Electrical Insulating Materials.
ASTM D 257 - Standard Test Methods for D-C Resistance or Conductance of Insulating Materials.
ASTM D 877 - Standard Test Methods for Dielectric Breakdown Voltage of Insulating Liquids Using Disk Electrodes.
ASTM D 971 - Interfacial Tension of Oil Against Water by the Ring Method.
ASTM D 1002 - Standard Test Method for Strength Properties of Adhesives in Shear by Tension Loading (Metal-to-Metal).
ASTM D 1120 - Engine Coolant, Boiling Point of.
ASTM D 1331 - Standard Test Methods for Surface and Interfacial Tension of Solutions of Surface-Active Agents.
ASTM D 2109 - Standard Test Methods for Nonvolatile Matter in Halogenated Organic Solvents and their Admixtures.
ASTM D 3574 - Materials, Flexible Cellular-Slab, Bonded, and Molded Uretane Foam.
ASTM D 3850 - Rapid Thermal Degradation of Solid Electrical Insulating Materials by Thermogravimetric Method, Test Method for.
ASTM E 263 - Standard Test Method for Measuring Fast-Neutron Reaction Rates by Radioactivation of Iron.
ASTM E 264 - Standard Test Method for Measuring Fast-Neutron Reaction Rates by Radioactivation of Nickel.
ASTM E 265 - Standard Test Method for Measuring Reaction Rates and Fast-Neutron Fluences by Radioactivation of Sulfur-32.
ASTM E 666 - Standard Practice for Calculating Absorbed Dose from Gamma or X-Radiation.
ASTM E 668 - Standard Practice for Application of Thermoluminescence-Dosimetry (TLD) Systems for Determining Absorbed Dose on Radiation Hardness Testing of Electronic Devices.
ASTM E 720 - Standard Guide for Selection and Use of Neutron Sensors for Determining Neutron Spectra Employed in Radiation-Hardness Testing of Electronics.
ASTM E 721 - Standard Method for Determining Neutron Energy Spectra with Neutron-Activation Foils for Radiation-Hardness Testing of Electronics.
ASTM E 722 - Standard Practice for Characterizing Neutron Energy Fluence Spectra in Terms of an equivalent Monoenergetic Neutron Fluence for Radiation-Hardness Testing of Electronics.

AMERICAN SOCIETY FOR TESTING AND MATERIALS (ASTM) (CONTINUED)

ASTM E 801	-	Standard Practice for Controlling Quality of Radiological Examination of Electronic Devices.
ASTM E 831	-	Standard Test Method for Linear Thermal Expansion of Solid Materials by Thermomechanical Analysis
ASTM E 1249	-	Minimizing Dosimetry Errors in Radiation Hardness Testing of Silicon Electronic Devices.
ASTM E 1250	-	Standard Method for Application of Ionization Chambers to Assess the Low Energy Gamma Component of Cobalt 60 Irradiators Used in Radiation Hardness Testing of Silicon Electronic Devices.
ASTM E 2450	-	Standard Practice for Application of CaF_2(Mn) Thermoluminescence Dosimeters in Mixed Neutron-Photon Environments.
ASTM F 458	-	Standard Practice for Nondestructive Pull Testing of Wire Bonds.
ASTM F 459	-	Standard Test Methods for Measuring Pull Strength of Microelectronic Wire Bonds.
ASTM F 526	-	Standard Test Method for Measuring Dose for Use in Linear Accelerator Pulsed Radiation Effects Tests.
ASTM F 1192	-	Standard Guide for the Measurement of Single Event Phenomena (SEP).
ASTM F 1892	-	Standard Guide for Ionizing Radiation (Total Dose) Effects Testing of Semiconductor Devices.

(Copies of these documents are available online at https://www.astm.org/)

2.4 Order of precedence. Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. DEFINITIONS

3.1 Abbreviations, symbols, and definitions. For the purpose of this standard, the abbreviations, symbols, and definitions specified in MIL-PRF-19500, MIL-PRF-38535, or MIL-HDBK-505 apply. The following definitions also apply:

3.1.1 Microelectronic device. A microcircuit, microcircuit module, or an element of a microcircuit as defined in appendix A of MIL-PRF-38535. For the purposes of this document, each type of microelectronic device will be identified by a unique type, or drawing number.

3.1.2 Mode of failure. The cause for rejection of any failed device or microcircuit as defined in terms of the specific electrical or physical requirement which it failed to meet (i.e., no failure analysis is required to identify the mode of failure, which should be obvious from the rejection criteria of the test method).

3.1.3 Mechanism of failure. The original defect which initiated the microcircuit or device failure or the physical process by which the degradation proceeded to the point of failure, identifying quality defects, internal, structural, or electrical weakness and, where applicable, the nature of externally applied stresses which led to failure.

3.1.4 Absolute maximum ratings. The values specified for ratings, maximum ratings, or absolute maximum ratings are based on the "absolute system" and are not to be exceeded under any measurable or known service or conditions. In testing microelectronic devices, limits may be exceeded in determining device performance or lot quality, provided the test has been determined to be nondestructive and precautions are taken to limit device breakdown and avoid conditions that could cause permanent degradation. These ratings are limiting values beyond which the serviceability of any individual microelectronic integrated circuit may be impaired. It follows that a combination of all the absolute maximum ratings cannot normally be attained simultaneously. Combinations of certain ratings are permissible only if no single maximum rating is exceeded under any service condition. Unless otherwise specified, the voltage, current, and power ratings are based on continuous dc power conditions at free air ambient temperature of 25°C ±3°C. For pulsed or other conditions of operation of a similar nature, the current, voltage, and power dissipation ratings are a function of time and duty cycle. In order not to exceed absolute ratings, the equipment designer has the responsibility of determining an average design value, for each rating, below the absolute value of that rating by a safety factor, so that the absolute values will never be exceeded under any usual conditions of supply-voltage variations, load variations, or manufacturing variations in the equipment itself.

3.1.5 Worst case condition. Worst case condition(s) consists of the simultaneous application of the most adverse (in terms of required function of the device) values (within the stated operating ranges) of bias(es), signal input(s), loading and environment to the device under test. Worst cases for different parameters may be different. If all the applied test conditions are not established at the most adverse values, the term "partial worst case condition" should be used to differentiate and should be accompanied by identification of the departure from worst case. For example, the lowest values of supply voltages, signal input levels, and ambient temperature and the highest value of loading may constitute "worst case conditions" for measurement of the output voltage of a gate. Use of the most adverse values of applied electrical conditions, at room temperature, would then constitute "partial worst case conditions" and should be so identified using a postscript "at room temperature."

3.1.5.1 Accelerated test condition. Accelerated test conditions are defined as test conditions using one or more applied stress levels which exceed the maximum rated operating or storage stress levels but are less than or equal to the "Testing Rating" values.

3.1.6 Static parameters. Static parameters are defined as dc voltages, dc currents, or ratios of dc voltages or dc currents, or both.

3.1.7 Dynamic parameters. Dynamic parameters are defined as those which are rms or time-varying values of voltages or currents, or ratios of rms or time-varying values of voltages or currents, or both.

3.1.8 Switching parameters. Switching parameters are defined as those which are associated with the transition of the output from one level to another or the response to a step input.

3.1.9 Functional tests. Functional tests are defined as those go, no-go tests which sequentially exercise a function (truth) table or in which the device is operated as part of an external circuit and total circuit operation is tested.

3.1.10 Acquiring activity. The acquiring activity is the organizational element of the Government which contracts for articles, supplies, or services; or it may be a contractor or subcontractor when the organizational element of the Government has given specific written authorization to such contractor or subcontractor to serve as agent of the acquiring activity. A contractor or subcontractor serving as agent of the acquiring activity does not have the authority to grant waivers, deviations, or exceptions unless specific written authorization to do so has also been given by the Government organization.

3.1.11 Accuracy. The quality of freedom from error. Accuracy is determined or assured by calibration, or reliance upon calibrated items.

3.1.12 Calibration. Comparison of measurement standard or instrument of known accuracy with another standard, instrument or device to detect, correlate, report or eliminate by adjustment, any variation in the accuracy of the item being compared. Use of calibrated items provide the basis for value traceability of product technical specifications to national standard values. Calibration is an activity related to measurement and test equipment performed in accordance with ANSI/NCSL Z540.3 or equivalent.

3.1.13 Precision. The degree to which an instrument, device, assemblage, test, measurement or process exhibits repeatability. Expressed statistically or through various techniques of Statistical Process Control (SPC). Term is used interchangeably with "repeatability".

3.1.14 Resolution. The smallest unit of readability or indication of known value in an instrument, device or assemblage thereof.

3.1.15 Standard reference material (SRM). A device or artifact recognized and listed by the National Institute of Standards and Technology (NIST) as having known stability and characterization. SRM's used in product testing provide traceability for technical specifications. SRM's do not require calibration when used and stored in accordance with NIST accompanying instructions. They are used as "certified materials".

3.1.16 Tolerance. A documented range over which a specified value may vary.

3.1.17 Test accuracy ratio (TAR). A ratio of the tolerance of the device under test to the accuracy of the related measuring or test instrument or to the accuracy of the correlation device/SRM.

3.1.18 Uncertainty. An expression of the combined errors in a test measurement process. Stated as a range within which the subject quantity is expected to lie. Comprised of many components including: estimates of statistical distribution and results of measurement or engineering analysis. Uncertainty established with a suitable degree of confidence, may be used in assuring or determining product conformance and technical specifications.

3.1.19 Susceptibility. The point at which a device fails to meet the postirradiation end-point electrical parameter limits or fails functionally during radiation exposure (e.g., neutron irradiation).

3.1.20 Class M. Class M is defined as 1.2.1 of MIL-STD-883 basic section compliant product or product built in compliance to Appendix A of MIL-PRF-38535 documented on a Standard Microcircuit Drawing where configuration control is provided by the Government preparing activity. Class M devices are required to use the conditions specified in the test methods herein for class level B product.

3.1.21 Class level B and class level S. 2 class levels are used in this document to define requirements for high reliability military applications (Class level B) and space applications (Class level S). Class level B requirements contained in this document are intended for use for Class Q, Class H, and Class M products, as well as Class B M38510 JAN slash sheet product. Class level B requirements are also intended for use for product claimed as 883 compliant or 1.2.1 compliant for high reliability military applications. Class level S requirements contained in this document are intended for use for Class V, Class K, as well as M38510 Class S JAN slash sheet product. Class level S requirements are also intended for use for product claimed as 883 compliant or 1.2.1 of MIL-STD-883 basic section compliant for space level applications.

3.1.22 Acquisition documents. Acquisition documents consist of the acquisition order or contract, device specification (e.g. SMD's, SCD's) or specifications as applicable.

4. GENERAL REQUIREMENTS

4.1 General. Unless otherwise specified in the individual test method, the general requirements of MIL-STD-883 shall apply.

4.2 Test circuits. The test circuits shown in the test methods of this test method standard are given as examples which may be used for the measurements. They are not necessarily the only test circuits which can be used; however the manufacturer shall demonstrate to the Government that other test circuits which they may desire to use will give results within the desired accuracy of measurement.

4.3 Laboratory suitability. Prior to processing any microcircuit intended for use in any military system or sub-system, the facility performing the test(s) shall be audited by the DLA Land and Maritime, Sourcing and Qualification Division and be granted written laboratory suitability status for each test method to be employed. Processing of any devices by any facility without laboratory suitability status for the test methods used shall render the processed devices nonconforming.

4.4 Method of reference. When applicable, test methods contained herein shall be referenced in the individual specification or specification sheet by specifying the test method number and, the details required in the summary of the applicable test method shall be listed. To avoid the necessity for changing documents that refer to test methods of this standard, the revision number should not be used when referencing test methods. (For example: Use 4001 versus 4001.2.)

5. DETAILED REQUIREMENTS

This section is not applicable to this standard.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory.)

6.1 Intended use. The intended use of this test method standard is to establish appropriate conditions for testing semiconductor devices to give test results that simulate the actual service conditions existing in the field. This test method standard has been prepared to provide uniform test methods, controls, and procedures for determining with predictability the suitability of such devices within military, aerospace and special application equipment.

6.2 International standardization agreement. Certain provisions of this test method standard are the subject of international standardization agreement. When amendment, revision, or cancellation of this test method standard is proposed which will affect or violate the international agreement concerned, the preparing activity will take appropriate reconciliation action through international standardization channels, including departmental standardization offices, if required.

6.3 Subject term (key word) listing

Destructive tests
Environmental tests
Laboratory suitability
Non–destructive tests

6.4 Supersession data The main body and five parts (–1 through –5) of this revision of MIL-STD-883 replace superseded MIL–STD–883K

METHOD 5001

PARAMETER MEAN VALUE CONTROL

1. PURPOSE. The purpose of this method is to define a technique for assuring a conformance to a maximum or minimum mean of a parameter measured in any test method listed in section 3000 and 4000 of this standard. This method is not intended for general application to acquisitions where it is important only to assure that device parameters are between specified limits. It is intended for use only where it is necessary to control the average or mean value for a given parameter throughout a lot of shipment of devices. When this method is employed, it is expected that the specified group of devices tested will be packaged for shipment as a group together with the required data. It is also expected that some provisions will be required for special marking of devices subjected to this method to identify that they have met the selection criteria involved and that they are therefore not directly interchangeable with identical devices which have not been controlled or selected in this manner.

2. APPARATUS. For distribution control, it is desirable for the measuring equipment to have data logging capability in addition to the capabilities listed in section 3000 and 4000. The data shall be recorded and analyzed to compute the average value of a group of microelectronic devices. The size of the group shall be specified in the applicable acquisition document.

3. PROCEDURE. Microelectronic devices shall be separated into groups. Each group will be tested in accordance with the specified test method. The reading from each device will be recorded. When all devices in the group have been tested, the recorded data shall be averaged (or the mean value computed) and compared against a maximum or minimum limit specified in the applicable acquisition document.

4. SUMMARY. The following details must be specified in the applicable acquisition document:

a. Absolute maximum and minimum limits.

b. Maximum or minimum limits on the average or mean.

c. Group size.

d. Requirements for data logging, special marking, and special provisions for group packaging and shipment, where applicable.

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METHOD 5002.1

PARAMETER DISTRIBUTION CONTROL

1. PURPOSE. The purpose of this method is to define a technique for assuring a normal distribution for any test method listed in the 3000 or 4000 series of this standard. This method is not intended for general application to acquisitions where it is important only to assure that device parameters are between specified limits. It is intended for use only where it is necessary to control the distribution of parameter values within the specified group. When this method is employed, it is expected that the specified group of devices tested will be packaged for shipment as a group together with the required data. It is also expected that some provisions will be required for special marking of devices subjected to this method to identify that they have met the selection criteria involved and that they are therefore not directly interchangeable with identical devices which have not been controlled or selected in this manner.

2. APPARATUS. For distribution control, it is desirable for the measuring equipment, in addition to the capabilities listed in section 3000 and 4000, to have the capability of rejecting and counting the devices above or below the specified extreme limits, and to also separate and count the devices that fall above or below the sigma limits. If the equipment does not have this capability, the units shall be read to the specified parameter conditions and the data recorded. Identification of units to the data shall also be required. Data analysis and unit separation shall be hand performed in the case where automatic equipment is not used.

3. PROCEDURE. Microelectronic devices shall be separated into groups. Each group will be tested, in accordance with the specific method for the maximum and minimum limits specified in the applicable acquisition document. All failures will be removed from the original group. The remaining units will be tested for the following: Not less than 12 percent but not greater than 18 percent of units tested will fall below the mean -1& limit. Not greater than 18 percent but not less than 12 percent of units tested will fall above the mean +1& limit.

4. SUMMARY. The following details must be specified in the applicable acquisition document:

a. Absolute maximum and minimum limits.

b. Mean value.

c. +1& and -1& value.

d. Group size.

e. Requirements for data logging, special markings, and special provisions for packaging and shipment, where applicable.

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METHOD 5003

FAILURE ANALYSIS PROCEDURES FOR MICROCIRCUITS

1. PURPOSE. Failure analysis is a post mortem examination of failed devices employing, as required, electrical measurements and many of the advanced analytical techniques of physics, metallurgy, and chemistry in order to verify the reported failure and identify the mode or mechanism of failure as applicable. The failure analysis procedure (as indicated by test condition letter) shall be sufficient to yield adequate conclusions, for determination of cause or relevancy of failure or for initiation of corrective action in production processing, device design, test or application to eliminate the cause or prevent recurrence of the failure mode or mechanism reported.

1.1 Data requirements. When required by the applicable acquisition document the failure analyst shall receive, with the failed part, the following information:

a. Test conditions: This shall include the type of test or application, the in-service time (when available), temperature, and other stress conditions under which the device failed.

b. System conditions: This shall include the exact location of failure in the equipment, date, test and inspection or both, at which defect was first noted, any unusual environmental conditions and all related system anomalies noted at time of removal of the failed unit. The equipment symptoms shall also be recorded.

c. General device information: This shall include part type numbers and serial numbers (when applicable), date code, and other identifying information, and size of production or inspection lot (when applicable).

2. APPARATUS. The apparatus required for failure analysis includes electrical test equipment capable of complete electrical characterization of the device types being analyzed, micromanipulators capable of point-to-point probing on the surface of device dies or substrates, as required, and microscopes capable of making the observations at the magnifications indicated in the detailed procedures for the specified test condition. In addition, special analytical equipment for bright field, dark field and phase contrast microscopy, metallographic sectioning, and angle lapping are required for the test condition C. Special analytical equipment for test condition D are as detailed in the procedure and shall be available only as required for each specific device analysis at that level. Apparatus for x-ray radiography, hermeticity test, and other specific test methods shall be as detailed in the referenced method. Cleaning agents, chemicals for etching, staining, oxide, or metallization removal shall be available as required.

3. PROCEDURE. Failure analysis shall be performed in accordance with the specified test condition letter (see 4).

3.1. Test condition A. Failure verification. This represents a minimal diagnosis, comprised of the electrical verification of the failure including external and internal photographic recording of the suspected mode or mechanism of failure. The following steps (see 3.1.1 through 3.1.5) shall be performed in the sequence indicated and the results included in the failure analysis report. The sequence may be modified or additional tests performed when justified by an analysis of the results of previous steps in the sequence.

3.1.1 External examination. This shall include an optical examination at a magnification of 30X minimum of:

a. The condition of the leads, plating, soldered, or welded regions.

b. Condition of external package material, seals, marking, and other failures as warranted.

Photographic records shall be made at suitable magnification of any unusual features.

3.1.2 Electrical verification procedures. This shall include the measurement of all electrical parameters in the applicable acquisition document.

3.1.3 Additional electrical tests. These shall be performed specifically for the determination of opens and shorts:

a. Threshold test. Determine the forward characteristic obtained for each pin to substrate and compare to the device schematic and structure. Excessive forward voltage drop may indicate an open or an abnormally high resistance current path.

b. Case isolation. (For metal packages or those with metal lids or headers only.) Apply a voltage between the package and the external leads. Current flow determines the presence of shorts-to-case.

c. As an alternative to a. and b. above, suitable electrical tests may be made to determine that no opens, shorts, or abnormal characteristics exist between pairs of pins, pins and die or substrate, or pins and device package.

3.1.4 Internal examination. The lid of the failed device shall be carefully removed and an optical examination made of the internal device construction at a minimum magnification of 30X. A color photograph, at suitable magnification to show sufficient detail, shall be taken of any anomalous regions which may be related to the device failure.

3.1.5 Information obtainable. The following is a partial list of failure modes and mechanisms which may be identified using test condition A:

a. Overstress conditions resulting from device abuse, transients, or inadequate power supply regulation, evidenced as open or shorted leads, and other metallization problems, such as flashover between contacts with the circuit.

b. Excessive leakage currents indicating degraded junctions.

c. Resistance changes.

d. Degradation of time response or frequency dependent parameters.

e. Opens and shorted leads or metallization land areas.

f. Undercut metals.

g. Intermetallic formation.

h. Poor bond placement and lead dress.

i. Thin metal at oxide steps.

j. Migration of metal.

k. Oxide contamination - discoloration.

l. Oxide defects, cracks, pinholes.

m. Mask misregistration.

n. Reactions at metal/semiconductor contact areas.

o. Degradation of lead at lead frame.

p. Shorts through the oxide or dielectric.

q. Missing or peeling metals.

r. Corroded metals within package.

s. Cracked die or substrate.

3.2 Test condition B. This is a more extensive procedure which supplements test condition A with x-ray radiography, seal testing, additional electrical measurements, package cleaning, vacuum baking, and probing procedures to aid in confirmation of suspected modes and mechanisms. The following steps shall be performed in the sequence indicated and the results included in the failure analysis report. The sequence may be modified or additional tests performed when justified by an analysis of the results of previous steps in the sequence.

3.2.1 External examination. This shall include an optional examination at a magnification of 30X minimum of:

a. The conditions of leads, platings, soldered, or welded regions.

b. Condition of external package material, seals, markings, and other features as warranted.

Photographic records shall be taken at suitable magnification of any unusual features.

3.2.2 Electrical verification procedures. This shall include the measurement of all electrical parameters in the applicable acquisition document.

3.2.3 Additional electrical tests. In addition to the threshold and case isolation tests, this section provides for curve tracer pin to pin measurements and other nonstandard measurements which allow electrical characterization of significant physical properties.

a. Threshold test. Determine the forward characteristic obtained for each pin to substrate and compare to the device schematic and structure. Excessive forward voltage drop may indicate an open or abnormally high resistance in the current path.

b. Case isolation. (For metal packages or those with metal lids or headers only.) Applying a voltage between the package and the external leads. Current flow determines the presence of shorts-to-case.

c. Pin-to-pin two and three terminal electrical measurements utilizing a transistor curve tracer, electrometer, picoammeter, capacitance bridge, and oscilloscope, as required, shall be performed and results recorded for lead combinations involving the defective portion of the microcircuit. Gain, transfer, input versus output, forward and reverse junction characteristics, shall be observed and interpreted. Resulting characteristics may be compared to those obtained from a good unit, and differences interpreted for their relation to the device failure.

3.2.4 X-ray radiography. A film record is required of the failed device taken normal to the top surface of the device, and where applicable, additional views shall be recorded. This shall be performed when open or shorted leads, or the presence of foreign material inside the device package are indicated from electrical verification of failure or there is evidence of excessive temperature connected with the device failures.

3.2.5 Fine and gross seal testing. This shall be performed in accordance with method 1014 of this standard.

3.2.6 External package cleaning. When there is evidence of contamination on the package exterior, the device shall be immersed in standard degreasing agents followed by boiling deionized water. After drying in clean nitrogen, critical parameters in the applicable acquisition document shall be remeasured in accordance with 3.2.1 above.

3.2.7 Internal examination. The lid of the failed device shall be carefully removed and an optical examination made of the internal device construction, at a minimum magnification of 30X. A color photograph, at suitable magnification to show sufficient detail, shall be taken of any anomalous regions which may be related to the device failure. Where there is evidence of foreign material inside the device package, it shall be removed using a stream of dry compressed inert gas or appropriate solvents. The relationship of the foreign material to device failure (if any) shall be noted and if possible, the nature of the material shall be determined.

3.2.8 Electrical verification procedures. Critical parameters of the individual specification shall be remeasured and recorded.

3.2.9 Vacuum bake. This shall be performed at the suggested condition 10^{-5} torr, 150°C to 250°C for 2 hours noting any change in leakage current, as a result of baking, using a microammeter.

3.2.10 Electrical verification procedures. Critical parameters of the individual specification shall be remeasured and recorded.

3.2.11 Multipoint probe. A multipoint probe shall be used as applicable to probe active regions of the device to further localize the cause of failure. A curve tracer shall be used to measure resistors, the presence of localized shorts and opens, breakdown voltages, and transistor gain parameters. A microammeter shall be used for measuring leakage currents, and where applicable, a capacitance bridge shall be employed for the determination of other junction properties. It may be necessary to open metallization stripes to isolate components.

3.2.12 Information obtainable. The procedures of test condition B can result in the following information in addition to that outlined in 3.1.5:

a. Hermeticity problems.

b. Radiographically determined defects such as poor wire dress, loose bonds, open bonds, voids in die or substrate mount, presence of foreign materials.

c. Further definition of failed device region.

d. Stability of surface parameters.

e. Quality of junctions, diffusions and elements.

3.3 Test condition C. In this procedure additional metallographic analysis techniques are provided to supplement the analysis accomplished in test condition B, and shall be performed after completion of the full procedure of test condition B. In test condition C, one of the procedures (see 3.3.1, 3.3.2, and 3.3.3) shall be selected as appropriate and the steps shall be followed in the sequences indicated. The sequence may be modified or additional tests performed when justified by the analysis of the results of previous steps in the sequence.

3.3.1 Total device cross section. This procedure shall be used where there are indications of defects in the package, die or substrate, bonds, seals, or structural elements. The following steps shall be performed:

a. Mount the device in the appropriate orientation for cross sectioning procedures.

b. Section to reveal desired feature(s) and stain where applicable.

c. Employ bright field, dark field, or polarized light photomicrography at suitable magnification.

d. Make photographic record of defective regions or features pertinent to the mode or mechanism of failure.

3.3.2 Oxide defect analysis. This procedure shall be used where there are indication of oxide (or other dielectric) structural anomalies or contamination within or under the oxide or where it is necessary to determine the specific location and structure of such defects. The following steps shall be performed:

a. Remove bonds to die or substrate and remove metallized interconnection layer(s).

b. Observe the oxide using interferometric or phase contrast photomicrography at suitable magnification and make appropriate photographic record.

c. Observe and probe semiconductor contact (window or cut) areas as applicable, recording appropriate electrical characteristics.

d. Mount the die or substrate in the appropriate orientation for sectioning (angle or cross) procedures, cut or lap to reveal desired features and stain where applicable.

e. Make photographic record at suitable magnification.

3.3.3 Diffusion defect analysis. This procedure shall be used where there are indications of diffusion imperfections, diffusion of contact metal into the semiconductor, structural defects in the semiconductor or anomalies in junction geometries. The following steps shall be performed:

a. Remove bonds to die or substrate and remove metallized interconnection layer(s).

b. Remove oxide or other dielectric passivation layer.

c. Probe contact regions recording appropriate electrical characteristics.

d. Stain surface to delineate junctions.

e. Mount the die or substrate in the appropriate orientation for cross sectioning or angle lapping, as applicable.

f. Cut or lap as required to expose significant features and stain junctions (may involve successive lap and stain operations to approach specific defect).

g. Make photographic record at suitable magnification of significant features and record pertinent electrical probing results.

3.3.4 Information obtainable. Failure analysis in accordance with test condition C provides additional capability for detecting or defining the following types of defects:

a. Oxide or dielectric imperfections.

b. Oxide or dielectric thicknesses.

c. Diffusion imperfections.

d. Junction geometries.

e. Intermetallic phase formation.

f. Voids at the bond/metallization interface.

g. Diffusion of contact metal into the semiconductor or substrate.

h. Migration of metals across, through, or under the oxide or dielectric.

i. Voids in die or substrate mount.

3.4 Optional measurements. The purpose of failure analysis is to obtain sufficient information to initiate corrective action in device design, production, test, or application. It may be necessary to obtain more detailed information than can be acquired in test conditions A, B, or C on the nature of contaminants or phases observed, concentrations, dimensions of submicroscopic features, etc. The selection and use of a number or less conventional analytical techniques by highly qualified personnel can provide this more extensive or fundamental knowledge of the precise chemical, physical, or electrical mechanisms of failure. The decision as to which techniques are appropriate and the point in the analytical sequence of test conditions A, B, or C at which they should be employed is contingent on the nature of information desired and previous results obtained from the specified analytical procedures, and must be left to the discretion of the analyst. Any of the following techniques may therefore be introduced into a failure analysis sequence at the appropriate point provided precautions are taken to avoid destruction of the evidence of failure which may be observed in subsequent procedures. Where multiple samples of the same type of device or failure exist, it shall be permissible to subdivide the quantity of devices and employ destructive techniques in parallel with the specified test condition provided all samples have been exposed to electrical verification tests and internal examination (see 3.1.1 through 3.1.3 and 3.2.1 through 3.2.5) prior to any of the optional measurements. When any of these optional measurements are employed, they shall be listed in the failure analysis report including the details of the method applied, conditions of test and results.

a. Residual gas analysis. When device surface contamination is indicated as a possible cause of failure, the lid of an unopened device shall be punctured and the internal gaseous ambient analyzed for the type and concentration of volatile products. This information then supplements electrical leakage current measurements and hermeticity tests.

b. Surface profilometer measurement. A mechanical determination of surface topography variations can be made using this type of instrument. This records the vertical motion of a stylus moved across the surface of the device. This information can be used to quantitatively determine oxide, dielectric, or metal thicknesses.

c. Photoscanning. A device, with leads and interconnections intact, after being opened, can be scanned with a small diameter beam of light which generates photovoltages in active p-n junctions. This generated photovoltage which is dependent on many physical junction properties indicates the presence of surface channels or inversion layers or both, caused by contamination on, in, or under the passivating oxide layer. It is also possible to locate certain regions of enhanced high field multiplication, mask misregistration, imperfect diffusions, as well as other device imperfections involving junction properties.

d. Infrared scanning. An IR detector, sampling infrared radiation from various points of the surface of an operating microcircuit, can detect the location of hot spots and other thermal abnormalities.

e. Scanning electron microscopy and electron beam microanalysis. The scanning electron microscope, employing an electron beam with a diameter on the order of a few hundred angstroms, is the most effective means of attaining device structural information without the need for special sample preparation procedures. The scanning electron microscope can perform chemical analysis, such as the microanalyzer, by incorporating a nondispersive x-ray detector. An electron beam microanalyzer can be used for x-ray spectrochemical analysis of micron sized volumes of material. Several other device structural properties are determinable through detection and display of back-scattered primary electrons and secondary electrons. These instruments are most generally used for:

(1) Determination of surface potential variations using secondary electron scanning microscopy. The small size of the electron beam coupled with the properties of secondary electrons result in the ability to examine physical defects with much higher resolution and depth of field than light microscopy.

(2) Analysis of micron sized defects such as oxide pin-holed, metallization grain structure.

(3) Determination of products of solid state reactions, such as diffusion, precipitation, and intermetallic formation.

(4) Corrosion product identification.

f. Electron microscopy. An examination at extremely high magnification of the structure of failed metallization and bulk materials is best accomplished using electron microscopy.

g. Special test structures. Often the amount of reacted material on a failed circuit is too small to allow definitive determination of chemical and structural properties. In addition, it is often necessary to reproduce the failure in a controlled experimental manner for verification of the mechanism of failure. Special test structures may be fabricated with variations in geometry and materials permitting study of the mechanism without extraneous influences. This is most advantageous when information is desired concerning the basic failure mechanism(s).

4. SUMMARY. The following details must be specified in the applicable acquisition document:

a. Test condition letter (see 3.) for test conditions A, B, or C and where applicable, optional measurements (see 3.4), identifying the specific procedures to be applied and details as to their option application.

b. Any special measurements not described in the applicable test condition.

c. Requirements for data recording and reporting including instructions as to disposition of original data, photographs, radiographs, etc.

d. Physical and electrical specifications and limits for the device being analyzed.

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METHOD 5004.13

SCREENING PROCEDURES

1. PURPOSE. This method establishes screening procedures for total lot screening of microelectronics to assist in achieving levels of quality and reliability commensurate with the intended application. It must be used in conjunction with other documentation such as appendix A of MIL-PRF-38535 or an applicable device specification to establish the design, material, performance, control, and documentation requirements which are needed to achieve prescribed levels of device quality and reliability. In recognition of the fact that the level of screening has a direct impact on the cost of the product as well as its quality and reliability, two standard levels of screening are provided to coincide with two device classes or levels of product assurance. Since it is not possible to prescribe an absolute level of quality or reliability which would result from a particular screening level or to make a precise value judgment on the cost of a failure in an anticipated application, two levels have been arbitrarily chosen. The method provides flexibility in the choice of conditions and stress levels to allow the screens to be further tailored to a particular source, product, or application based on user experience. The user is cautioned to collect experience data so that a legitimate value judgment can be made with regard to specification of screening levels. Selection of a level better than that required for the specific product and application will, of course, result in unnecessary expense and a level less than that required will result in an unwarranted risk that reliability and other requirements will not be met. In the absence of specific experience data, the class B screening level is recommended for general applications. Guidance in selecting screening levels or predicting the anticipated reliability for microcircuits may be obtained from MIL-HDBK-217 Military Standardization Handbook Reliability Prediction.

NOTE: Reference to method 5004 on a stand-alone basis (not indicating compliance or noncompliance to 883) requires full compliance to 1.2.1 of this standard.(See 1.2.2)

2. APPARATUS. Suitable electrical measurement equipment necessary to determine compliance with applicable acquisition documents and other apparatus as required in the referenced test methods.

3. PROCEDURE.

3.1 Screening procedures for microcircuits. Screening of microcircuits shall be conducted as described in Table I, Screen Tests 1 through 19, and in the sequence shown except where variations in sequence are specifically allowed herein. This provision does not preclude the performance of additional tests or inspection which may be required for specific devices or which may be desirable to optimize results of screening; however, any such special test inspections shall be subjected to the requirements of A.3.4.3 of appendix A of MIL-PRF-38535. Any burn-in in addition to that specified is only permitted when documented in the lot records, and any failures shall be counted in applicable PDA calculations. Where end-point or post-test measurements are required as part of any given test method used in the screening procedure and where such posttest measurements are duplicated in the interim (post burn-in) or final electrical tests that follow, such measurements need not be duplicated and need be performed only as part of the interim (post burn-in) or final electrical tests. Devices which pass screening requirements of a higher reliability level shall be considered to meet the screening requirements of all lower levels. In no case shall screening to a lower level than that specified be permitted. Microcircuits which are contained in packages which have an inner seal or cavity perimeter of 2 inches or more in total length or which have a package mass of 5 grams or more may be treated in accordance with 3.2 as an alternative to Screen Test 5.

Qualified manufacturers list (QML) manufacturers who are certified and qualified to MIL-PRF-38535 or who have been granted transitional certification to MIL-PRF-38535 may modify the class level B screening table (Table I) as specified in the applicable device specification or drawing and as permitted in 1.2 of MIL-STD-883 provided the modification is contained in the manufacturers quality management (QM) plan and the "Q" or "QML" certification mark, is marked on the devices. For contractor prepared drawings, with specific references to individual test methods of MIL-STD-883 (e.g., method 1010, method 2001, etc.); these test methods may not be modified by a QML manufacturer without the knowledge and approval of the acquiring activity.

3.2 Constant acceleration procedure for large packages (see Table 1, Screen Test 5). Microcircuits which are contained in packages which have an inner seal or cavity perimeter of 2 inches or more in total length or have a package mass of 5 grams or more may be treated in accordance with provisions below as an alternate to the procedure of Table 1, Screen Test 5.

Delete test condition E and replace with test conditions as specified in the applicable device specification. Unless otherwise specified in the acquisition document, the stress level for large, monolithic microcircuit packages shall not be reduced below test condition D. If the stress level specified is below condition D, the manufacturer must have data to justify this reduction and this data must be maintained and available for review by the preparing or acquiring activity. The minimum stress level allowed is condition A.

3.3 Alternate procedures to method 2010 internal visual for microcircuits. Alternate procedures may be used on an optional basis on any microcircuit, provided that the conditions and limits of the alternate procedures are submitted to, and approved by the preparing activity, or the acquiring activity.

3.3.1 Alternate procedures.

Alternate 1: The deletions and the changes stated in 3.3.1a are allowable for class level B product only if the requirements of 3.3.1b and 3.3.1c are imposed and any of the following conditions exists.

1. Minimum horizontal geometry is less than 3 micrometers (μm).
2. Interconnects consisting of two or more levels.
3. Opaque materials mask design features.

a. For inspection of each microcircuit die, delete the inspection criteria of 3.1.1, 3.1.2, 3.1.3, 3.1.4, 3.1.5, 3.1.6, 3.1.7, and 3.2.5 of condition B of method 2010 and for use in conjunction with alternate procedures add 3.1.1.1, 3.1.1.2, 3.1.1.6, 3.1.3, 3.1.4, and 3.2.5 to the low magnification inspection of method 2010.

b. Temperature cycling (Screen Test 4). The minimum total number of temperature cycles shall be 10.

(1) The manufacturer shall perform a high magnification visual inspection on a small sample of devices (e.g., 5(0)) to monitor the process. This inspection may be performed at wafer level.

c. Special electrical screening tests shall be applied to each microcircuit die at the wafer, individual die (chip) or packaged microcircuit level in accordance with the requirements of 3.3.2 of MIL-STD-883, method 5004. The conditions and limits of the electrical tests (in Table III format) shall be submitted to the preparing activity for approval and subsequently maintained on file with the qualifying activity. These special screens are in addition to the required electrical parametric tests which the device must pass and shall be designed to screen out devices with defects that were not inspected to the full criteria of Screen Test 3 (internal visual). Due to the nature of these tests, they are not to be repeated as part of the qualification and quality conformance procedures in accordance with method 5005.

Alternate 2: The requirements and conditions for use of this alternate are contained in appendix A of this method. This option applies to both class level B and class level S microcircuits.

TABLE I. Screening procedure for hermetic classes Q, V and non-hermetic class Y microcircuits

Screening Tests	MIL-STD-883, test method (TM) and conditions		
	Class Q (class level B)	Class V (class level S)	Class Y (class level S)
1. Wafer lot acceptance test	QM plan (see H.3.2.1.4) 1/	QM plan (see H.3.2.1.4) 1/ or TM 5007 of MIL-STD-883 (all lots)	QM plan (see H.3.2.1.4) 1/ or TM 5007 of MIL-STD-883 (all lots)
2. Nondestructive bond pull (NDBP) test 2/		TM 2023	TM 2023
3. Internal visual inspection 3/	TM 2010, condition B	TM 2010, condition A	TM 2010, condition A
4. Temperature cycling 4/	TM 1010, condition C, 10 cycles minimum	TM 1010, condition C, 10 cycles minimum	TM 1010, condition C, 10 cycles minimum
5. Constant acceleration 5/	TM 2001, condition E (minimum), Y1 orientation only	TM 2001, condition E (minimum), Y1 orientation only	TM 2001, condition E (minimum), Y1 orientation only
6. Visual inspection 6/	100%	100%	100%
7. Particle Impact Noise Detection (PIND) test 7/ 8/		TM 2020, test condition A on each device	TM 2020, test condition A on each device
8. Serialization 9/	In accordance with device specification (100%)	In accordance with device specification (100%)	In accordance with device specification (100%)
9. Pre burn-in (Interim) electrical parameters test 10/	In accordance with device specification 11/	In accordance with device specification 12/	In accordance with device specification 12/
10. Burn-in test: 10/ 13/ 14/	TM 1015 160 hours at +125°C minimum	TM 1015 240 hours at 125°C, condition D 15/	TM 1015 240 hours at 125°C , condition D 15/
11. Post burn-in (Interim) electrical parameters test 10/		In accordance with device specification 12/	In accordance with device specification 12/
12. Reverse bias burn-in test (Static burn-in) 13/ 14/ 16/		TM 1015, Condition A or C; 144 hours at +125°C or 72 hours at +150°C minimum	TM 1015, Condition A or C; 144 hours at +125°C or 72 hours at +150°C minimum
13. Post burn-in (Interim-reverse bias) electrical parameters test 10/		In accordance with device specification 12/	In accordance with device specification 12/

See footnotes at end of table.

TABLE I. Screening procedure for hermetic classes Q, V and non-hermetic class Y microcircuits - Continued.

Screening Tests	MIL-STD-883, test method (TM) and conditions		
	Class Q (class level B)	Class V (class level S)	Class Y (class level S)
14. Percent defective allowable (PDA) calculation 17/	5 percent PDA (all lots)	5 percent PDA, 3 percent PDA for functional parameters at 25°C (all lots)	5 percent PDA, 3 percent PDA for functional parameters at 25°C (all lots)
15. Final electrical tests 18/ (see table III) a. Static test : (1) at 25°C (2) Maximum and Minimum operating temperature b. Dynamic or functional test : 19/ (1) at 25°C (2) Maximum and Minimum operating temperature c. Switching test : (1) at 25°C (2) Maximum and Minimum operated temperature	In accordance with applicable device specification (see group A test)	In accordance with applicable device specification (see group A test)	In accordance with applicable device specification (see group A test)
16. Seal test 20/ a. Fine leak b. Gross leak	TM 1014	TM 1014	Not applicable
17. Radiographic (X-ray) and/or C-SAM test 21/		X-ray: TM 2012, Two views; C-SAM TM 2030	X-ray: TM 2012, Two views; C-SAM TM 2030
18. External visual inspection 22/ 23/	TM 2009	TM 2009	TM 2009
19. Qualification or quality conformance inspection/TCI test sample selection	24/	24/	24/
20. Radiation dose rate induced latch-up test 25/	TM 1020	TM 1020	TM 1020

See footnotes on next three pages.

Note: The screening and QCI/TCI tables from MIL-PRF-38535 and MIL-STD-883 Test Methods 5004 and 5005 have been combined for consistency. MIL-PRF-38535 shall reflect this change as well. Manufacturers shall document in their QM plan the screening and QCI/TCI requirements to either MIL-PRF-38535 or MIL-STD-883.

TABLE I. Screening procedure for hermetic classes Q, V and non-hermetic class Y microcircuits - Continued.

1/ Testing per manufacturer's QM plan. See paragraph H.3.2.1.4 of MIL-PRF-38535 or TM 5007 of MIL-STD-883.

2/ For flip chip packages Nondestructive bond pull (NDBP) test is not required.

3/ Unless otherwise specified, at the manufacturer's option for test samples selection of group B, bond strength test (method 5005) may be randomly selected prior to or following internal visual (method 5004), prior to sealing provided all other specification requirements are satisfied (e.g., bond strength requirements shall apply to each inspection lot, bond failures shall be counted even if the bond would have failed internal visual exam), and unsealed microcircuits awaiting further processing shall be stored in a dry, inert, controlled environment until sealed. Test method 2010 applies in full except when method 5004, alternate 1 or alternate 2 (appendix A) is in effect (see 3.3 method 5004 of MIL-STD-883). For gallium arsenide (GaAs) devices only, TM 5013 of MIL-STD-883 shall be used. For flip chip devices, both internal visual and C-SAM inspection (such as prior to bump attach to die and after bump attach to substrate and underfill cured etc.) shall be performed in accordance with TM 2010 and TM 2030.

4/ For devices with solder terminations, Temperature cycling test may be performed without balls and columns upon approval of Package Integrity Demonstration test Plan (PIDTP) and QM plan.

5/ All microcircuits shall be subjected to constant acceleration. For microcircuits which are contained in packages that have an inner seal or cavity perimeter of 2 inches or more in total length or have a package mass of 5 grams or more may be tested by replacing test condition E with condition D or with test conditions as specified in the applicable device specification. Unless otherwise specified in the acquisition document, the stress level for large, monolithic microcircuit packages shall not be reduced below test condition D. If the stress level specified is below condition D, the manufacturer must have data to justify this reduction and this deviation shall be specified in the QM plan, and data available for review by the preparing or acquiring activity. The minimum stress level allowed in this case is condition A. For flip chip devices, Constant acceleration test is not required.

6/ At the manufacturer's option, external visual inspection for catastrophic failures may be conducted after each of the thermal/mechanical screens, after the sequence or after seal test. Catastrophic failures are defined as missing leads, broken packages, or lids off.

7/ See paragraph A.4.6.3 of appendix A and paragraph B.4.1 of appendix B of MIL-PRF-38535. The PIND test may be performed in any sequence after temperature cycling test and prior to post burn-in (interim) electrical parameters test.

8/ For device without a cavity or for flip chip devices with underfill, PIND test is not applicable.

9/ Class V or class Y (class level S) devices shall be serialized prior to the first recorded electrical measurement in screening. Class Q (class level B) microcircuits shall be serialized if delta calculations or matching characteristics are a requirement of the device specification. Each microcircuit shall be assigned a unique serial number in order to trace the data back to an individual device within the inspection lot which shall, in turn, be traceable to the wafer lot from which the device originated.

10/ Interim (pre and post burn-in) electrical testing shall be performed when specified, to remove defective devices prior to further testing or to provide a basis for application of percent defective allowable (PDA) criteria when PDA is specified (Ref: Screen Test 14: PDA calculation, and footnote 17 herein). If no device specification or drawing exists, subgroups tested shall at least meet those of the most similar device specification or standard microcircuit drawing (SMD). This test need not include all specified device parameters, but shall include those measurements that are most sensitive to the time and temperature effects of burn-in and the most effective in removing electrically defective devices.

11/ When specified in the applicable device specification, 100 percent of the devices shall be tested and the results recorded for those parameters requiring delta calculations.

TABLE I. Screening procedure for hermetic classes Q, V and non-hermetic class Y microcircuits - Continued.

12/ For class V and class Y (class level S) microcircuit devices, delta measurements shall be performed. The specific delta parameters shall be as defined in the applicable device specification. Pre burn-in and post burn-in interim electrical parameters shall be read and recorded when delta measurements have been specified as part of post burn-in electrical measurements, 100 percent of the devices shall be tested and the results shall be recorded for those parameters requiring delta calculations.

13/ Burn-in shall be performed on all QML microcircuits, except as modified in accordance with SMD section 4.2, or above their maximum rated operating temperature (for devices to be delivered as wafer or die, burn-in of packaged samples from the wafer lot shall be performed to a quantity accept level of 10(0)). For microcircuits whose maximum operating temperature is stated in terms of ambient temperature (T_A), Table I of TM 1015 of MIL-STD-883 applies. For microcircuits whose maximum operating temperature is stated in terms of case temperature (T_C), and where the ambient temperature would cause T_J to exceed +175°C, the ambient operating temperature may be reduced during burn-in from +125°C to a value that will demonstrate a T_J between +175°C and +200°C and T_C equal to or greater than +125°C without changing the test duration. Data supporting this reduction shall be documented in the QM plan and shall be available to the acquiring and qualifying activities upon request. For devices with solder terminations, burn-in test may be performed before solder balls/columns have been attached to the packages.

14/ When test condition F of method 1015 for temperature accelerated screening is used for either burn-in or reverse bias burn-in , it shall be used for both. Also, when devices have aluminum/gold metallurgical systems (at either the die pad or package post), the constant acceleration test shall be performed after burn-in and before completion of the final electrical tests (e.g., to allow completion of time limited tests but that sufficient 100 percent electrical testing to verify continuity of all bonds is accomplished subsequent to constant acceleration).

15/ Where applicable, dynamic burn-in test shall be performed, and test condition F of method 1015 and temperature accelerated test requirement shall not apply. For class V or class Y (class level S), burn-in test shall be performed in accordance with TM 1015 of MIL-STD-883, on each device for 240 total hours at +125°C. For a specific device type, the burn-in duration may be reduced from 240 to 160 hours if three consecutive production lots of identical parts, from three different wafer lots pass percent defective allowable (PDA) requirements after completing 240 hours of burn-in. Sufficient analysis (not necessarily failure analysis) of all failures occurring during the run of the three consecutive burn-in lots shall not reveal a systematic pattern of failure indicating an inherent reliability problem which would require that burn-in be performed for a longer time. The manufacturer's burn-in procedures shall contain corrective action plans, approved by the qualifying activities for dealing with lot failures.

16/ The reverse bias burn-in is a requirement only when specified in the applicable device specification and is recommended only for a certain MOS, linear or other microcircuits where surface sensitivity may be a concern. When reverse bias burn-in is not required, interim post burn-in electrical parameter measurements shall be omitted. The order of performing the burn-in test and the reverse bias burn-in test may be inverted. Static burn-in may be substituted for high temperature reverse bias burn-in based on device technology and must be approved by the QA. Moreover, burn-in time-temperature regression Table I of TM 1015 of MIL-STD-883 can be used for determination of reverse bias burn-in time and temperature.

TABLE I. Screening procedure for hermetic classes Q, V and non-hermetic class Y microcircuits - Continued.

17/ The percent defective allowable (PDA) shall be 5 percent or one device, whichever is greater. This PDA shall be based, as a minimum, on failures from group A, subgroup 1 plus deltas (in all cases where delta parameters are specified) with the parameters, deltas and any additional subgroups (or subgroups tested in lieu of A-1) subject to the PDA as specified in the applicable device specification or drawing. If no device specification or drawing exists, subgroups tested shall at least meet those of the most similar device specification or Standard Microcircuit Drawing. In addition, for class V or class Y (class level S) the PDA shall be 3 percent (or one device, whichever is greater) based on failures from functional parameters measured at room temperature. For class level S screening where an additional reverse bias burn-in is required, the PDA shall be based on the results of both burn-in tests combined. The verified failures after burn-in divided by the total number of devices submitted in the lot or sublot for burn-in shall be used to determine the percent defective for that lot, or sublot and the lot or sublot shall be accepted or rejected based on the PDA for the applicable device class. Lots and sublots may be resubmitted for burn-in one time only and may be resubmitted only when the percent defective does not exceed twice the specified PDA (10 percent) or 2 devices, whichever is greater. This test need not include all specified device parameters, but shall include those measurements that are most sensitive to and effective in removing electrically defective devices (see A.4.6.1.1 and A.4.6.1.2 of MIL-PRF-38535).

18/ Final electrical testing of microcircuits shall assure that the microcircuits tested meet the electrical requirements of the device specification and shall include the tests of Table III, group A, subgroups 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, and 11, unless otherwise specified in the device specification. For solder termination devices, ball grid array (BGA) packages electrical test shall be performed across the full military temperature range after attachment of the solder balls on the package, and for Column Grid Array (CGA) packages, electrical test shall be performed across the full military temperature range before attachment of the solder columns on the package. After column attach, electrical test shall be performed at 25°C (Group A, subgroup 1) as a minimum to verify that no electrical/mechanical damage has been introduced due to the column attach process.

19/ Functional tests shall be conducted at input test conditions as follows: $V_{IH} = V_{IH}(min) +20$ percent, -0 percent; $V_{IL} = V_{IL}(max) +0$ percent, -50 percent; as specified in the most similar military detail specification. Devices may be tested using any input voltage within this input voltage range but shall be guaranteed to $V_{IH}(min)$ and $V_{IL}(max)$.

CAUTION: To avoid test correlation problems, the test system noise (e.g., testers, handlers, etc.) should be verified to assure that $V_{IH}(min)$ and $V_{IL}(max)$ requirements are not violated at the device terminals.

20/ The fine and gross leak seal tests shall be performed separately or together, between constant acceleration and external visual inspection test. For class level S and class level B devices, all device lots (sublots) having any physical processing steps (e.g., lead shearing, lead forming, solder dipping to the glass seal, change of, or rework to, the lead finish, etc.) performed following seal or external visual inspection shall be retested for hermeticity and visual defects. This shall be accomplished by performing, and passing, as a minimum, a sample seal test (method TM 1014) using an acceptance criteria of a quantity (accept number) of 116(0), and an external visual inspection (method TM 2009) on the entire inspection lot (sublot). For devices with leads that are not glass-sealed and that have a lead pitch less than or equal to 1.27 mm (0.050 inch), the sample seal test shall be performed using an acceptance criteria of a quantity (accept number) of 15(0). If the sample fails the acceptance criteria specified, all devices in the inspection lot represented by the sample shall be subjected to the fine and gross seal tests and all devices that fail shall be removed from the lot for final acceptance. For class level S devices, with the approval of the qualifying activity, an additional room temperature electrical test may be performed subsequent to seal, but before external visual, if the devices are installed in individual carriers during electrical test.

21/ The radiographic and/or C-SAM screening test may be performed in any sequence after serialization. Only one view is required for flat packages and leadless chip carriers having lead (terminal) metal on four sides. For flip chip technology, only C-SAM inspection is required. C-SAM inspection may be performed in any sequence after underfill cure for flip chip technology. For additional requirements for this test, see appendix B paragraph B.4.1 of MIL-PRF-38535.

TABLE I. Screening procedure for hermetic classes Q, V and non-hermetic class Y microcircuits - Continued.

22/ External visual inspection shall be performed on the lot any time after radiographic test and prior to shipment, and all shippable samples shall have external visual inspection at least subsequent to qualification or quality conformance inspection testing.

23/ The manufacturer shall inspect the devices 100 percent or on a sample basis using a quantity/accept number of 116(0). If one or more rejects occur in this sample, the manufacturer may double the sample size with no additional failures allowed or inspect the remaining devices 100 percent for the failed criteria and remove the failed devices from the lot. If the double sample also has one or more failures, the manufacturer shall be required to 100 percent inspect the remaining devices in the lot for the failed criteria. Re-inspection magnification shall be no less than that used for the original inspection for the failed criteria.

24/ Samples shall be randomly selected from the assembled inspection lot for testing in accordance with the specific device class and lot requirements of Group A, B, C, D, E and applicable appendices of MIL-PRF-38535 or TM 5005 of MIL-STD-883; after the specified screen requirements herein Table I or TM 5004 have been satisfactorily completed.

25/ Radiation dose rate induced latch-up screen test shall be conducted when specified in purchase order or contract. Dose rate induced latch-up screen test is not required when radiation induced latch-up is verified to be not possible such as SOI, SOS and dielectrically isolated technology devices. If radiation dose rate induced latch-up screen test is required, it may be performed at any screening operation step after seal test, at the manufacturer's option. Test conditions, temperature, and the electrical parameters to be measured pre, post, and during the test shall be in accordance with the device specification. The PDA for each inspection lot for class V or class Y (class level S) sublot submitted for radiation latch-up test shall be 5 percent or one device, whichever is greater.

3.3.2 Description of special electrical screening tests. The special electrical screens shall consist of a series of electrical tests each of which can be categorized as either a voltage stress test or a low level leakage test.

3.3.2.1 Voltage stress tests. The purpose of voltage stress tests is to eliminate those failure mechanisms which are voltage sensitive. These tests shall be designed such that each circuit element (including metallization runs) within the microcircuit is stressed by an applied voltage which approaches or exceeds (under current limited conditions) the breakdown voltage of the circuit element under test. For those elements which cannot be placed in a reverse bias mode, the applied voltage must be equal to or greater than 120 percent of the normal operating voltage. Any device which exhibits abnormal leakage currents at the specified applied voltage conditions shall be rejected. The number of stress tests being performed will vary from a few for a simple gate to many for MSI or LSI functions.

3.3.2.2 Low level leakage tests. The purpose of the low level leakage tests (which must be performed after the voltage stress tests) is to eliminate any device that exhibits abnormal leakage. Since leakage currents can be measured only at the device terminals, the test conditions and limits will vary depending upon the type of device being tested and the function of the terminal under test (V_{CC}, input, output, etc.). However, there may be cases where this test cannot be performed, i.e., input terminals which are forwarded biased junctions or resistive networks. But, since these types of circuits are generally very sensitive to leakage currents, the device would fail parametrically if abnormal leakage currents were present. For all other cases, where these measurements can be made, the tests shall be designed as described below:

a. For inputs which can be reverse biased, measure the input leakage at each input terminal at a voltage level which is equal to one-half the maximum rated input voltage for that device with the supply terminal grounded. The maximum allowable input leakage shall be established as shown in 3.3.2.2.1. Inputs shall be tested individually with all other input terminals grounded.

b. For outputs which can be reverse biased, measure the output leakage at each output terminal at a voltage which is equal to the device's maximum rated input voltage with the supply terminal grounded (if possible). The maximum allowable output leakage limit shall be established as shown in 3.3.2.2.1. The input terminals shall be all grounded (if the supply terminal is grounded) or if the supply terminal is not grounded, the input terminals should be in such a state that the output terminal under test is in the reverse biased mode. All outputs shall be tested.

c. Measure the supply terminal leakage current at a voltage which is equal to 80 percent of the voltage required to forward-bias a single PN junction on the device under test. The maximum allowable supply terminal leakage shall be established as shown in 3.3.2.2.1.

3.3.2.2.1 Establishing maximum leakage current limits. The maximum allowable leakage current shall be the upper 3 sigma value as established through an empirical evaluation of three or more production lots which are representative of current production. Any process change which results in a substantial shift in the leakage distribution shall be cause for recalculation and resubmission of this limit. The low current sensitivity of the test system shall be no higher than 20 percent of the expected mean value of the distribution.

3.4 Substitution of test methods and sequence.

3.4.1 Stabilization bake. Molybdenum-gold multilayered conductors shall be subject to stabilization bake in accordance with method 1008, condition C immediately before performing internal visual inspection Screen Test 3.

3.4.2 Accelerated testing. When test condition F of method 1015 for temperature/time accelerated screening is used for either burn-in (Screen Test 10) or reverse bias burn-in (Screen Test 12), it shall be used for both. Also, when devices have aluminum/gold metallurgical systems (at either the die pad or package post), the constant acceleration test (Screen Test 5) shall be performed after burn-in and before completion of the final electrical tests (Screen Test 15) (i.e., to allow completion of time limited tests but that sufficient 100 percent electrical testing to verify continuity of all bonds is accomplished subsequent to constant acceleration).

3.5 Electrical measurements.

3.5.1 Interim (pre and post burn-in) electrical parameters. Interim (pre and post burn-in) electrical testing shall be performed when specified, to remove defective devices prior to further testing or to provide a basis for application of percent defective allowable (PDA) criteria when a PDA is specified. The PDA shall be 5 percent or one device, whichever is greater. This PDA shall be based, as a minimum, on failures from group A, subgroup 1 plus deltas (in all cases where delta parameters are specified) with the parameters, deltas and any additional subgroups (or subgroups tested in lieu of A-1) subject to the PDA as specified in the applicable device specification or drawing. If no device specification or drawing exists, subgroups tested shall at least meet those of the most similar device specification or Standard Microcircuit Drawing. In addition, for class level S the PDA shall be 3 percent (or one device, whichever is greater) based on failures from functional parameters measured at room temperature. For class level S screening where an additional reverse bias burn-in is required, the PDA shall be based on the results of both burn-in tests combined. The verified failures after burn-in divided by the total number of devices submitted in the lot or sublot for burn-in shall be used to determine the percent defective for that lot, or sublot and the lot or sublot shall be accepted or rejected based on the PDA for the applicable device class. Lots and sublots may be resubmitted for burn-in one time only and may be resubmitted only when the percent defective does not exceed twice the specified PDA, or 20 percent whichever is greater. This test need not include all specified device parameters, but shall include those measurements that are most sensitive to and effective in removing electrically defective devices.

3.5.2 Final electrical measurements. Final electrical testing of microcircuits shall assure that the microcircuits tested meet the electrical requirements of the applicable device specification or drawing and shall include, as a minimum, all parameters, limits, and conditions of test which are specifically identified in the device specification or drawing as final electrical test requirements. Final electrical test requirements that are duplicated in interim (post burn-in) electrical test (Screen Test 15) need not be repeated as final electrical tests.

3.5.3 Radiation latch-up screen. Latch-up screen shall be conducted when specified in purchase order or contract. Test conditions, temperature, and the electrical parameters to be measured pre, post, and during the test shall be in accordance with the specified device specification. The PDA for each inspection lot or class level S sublot submitted for radiation latch-up test shall be 5 percent or one device, whichever is greater.

3.6 Test results. When required by the applicable device specification or drawing, test results shall be recorded and maintained in accordance with the general requirements of 4.2 of this standard and A.4.7 of appendix A of MIL-PRF-38535.

3.7 Failure analysis. When required by the applicable device specification, failure analysis of devices rejected during any test in the screening sequence shall be accomplished in accordance with method 5003, test condition A of this standard.

3.8 Defective devices. All devices that fail any test criteria in the screening sequence shall be removed from the lot at the time of observation or immediately at the conclusion of the test in which the failures was observed. Once rejected and verified as a device failure, no device may be retested for acceptance.

4. SUMMARY. The following details shall be specified:

a. Procedure paragraph if other than 3.1, and device class.

b. Sequence of test, test method, test condition, limit, cycles, temperature, axis, etc., when not specified, or if other than specified (see 3).

c. Interim (pre and post burn-in) electrical parameters (see 3.5.1).

d. Burn-in test condition (see Screen Test 10) and burn-in test circuit.

e. Delta parameter measurements or provisions for PDA including procedures for traceability where applicable (see 3.5.1).

f. Final electrical measurements (see 3.5.2).

g. Constant acceleration level (see 3.2).

h. Requirements for data recording and reporting, where applicable (see 3.6).

i. Requirement for failure analysis (see 3.7).

APPENDIX A

PURPOSE:

This appendix addresses two problems. First, Test Method 2010 visual criteria for wafer fab induced defects is unsuitable for complex wafer process technologies, as in most cases the defects themselves cannot be seen through 200X magnification. Secondly, no current alternate suitably addresses defect control of complex wafer fab technologies. Section 20 of this document describes the conditions under which this procedure is invoked. This document implements a new technique for controlling and eliminating wafer fab induced defects, while preserving and extending the intent of the original Test Method 2010 visual criteria.

The essence of this procedure revolves around the concept that it is a manufacturer's responsibility to define and document its approach to defect reduction and control in a manner that is acceptable to the manufacturer and their qualifying activity, as specified in section 30 of this document. This includes an understanding of the reliability impact of wafer fab process-induced defects. It is expected that considerable dialogue will occur between a manufacturer and the qualifying activity, resulting in mutually agreeable defect control procedures. This document is deliberately non-specific regarding metrics such as defect sizes, defect densities, correlation and risks to allow adaptability for different process technologies, different manufacturing control methods and continuous improvement. The procedures are specified in this document with the intent that metrics and their values will be made more specific via dialogue between a manufacturer and its qualifying activity.

Defect characterization is addressed in section 40 of this document. A key element in this section is understanding the effects of process defects on final product reliability. This understanding can be achieved in many ways, including: experimentation, review of pertinent literature and certain semiconductor traditions. The depth and scope of any characterization will be determined by a manufacturer and its qualifying activity.

The concept of demonstration is discussed in many sections of this document. The methods for demonstrating defect understanding have been made as diverse as possible to allow flexibility.

As described in section 90 of this document, results of defect characterization must be documented as well as the methods for monitoring and controlling defect levels. The effectiveness of any screens that are used (in-line or end-of-line) must also be documented. The ultimate requirements for demonstration and documentation will be determined between a manufacturer and its qualifying activity. The qualifying activity will be concerned with maintenance of institutional knowledge and the level to which a manufacturer understands: defect generation, control, reduction, prevention and the effects of defects on product reliability.

This document makes the underlying assumption that a manufacturer will undertake efforts to continuously improve defect levels (i.e. reduce these levels) in its wafer fabrication processes. As part of this assumption, it is expected that the inspections, as outlined in section 50 of this document, will be used to acquire information for defect level reduction. The intent is not to create inspections which "inspect in" quality, though screens of this nature may be a part of a manufacturer's integrated defect control system. Rather, it is intended to provide an effective means of defect prevention, control and reducing defects generated by the wafer process. Ideally, the manufacturer is striving to continually improve its control systems.

Sections 60, 70 and 80 of this document deal with excursion containment, yield analysis and a system for unexpected failure.

This document makes extensive use of examples and attachments to illustrate key points and ways in which these points could be implemented. The examples are intended to be no more than examples, illustrating how the items in this procedure might be performed in a given instance. They are not intended to specify the way items must be done. A glossary of terms is provided in section 100 of this document.

APPENDIX A

INTRODUCTION:

The evolution and progress in semiconductor fabrication technology require that new quality assurance methodologies be employed which are applicable to small geometry and multiple metallization microcircuits. Removal of ineffective visual inspections require an effective foreign material and defect control program early in the manufacturing process. It is the intent of this procedure to define the key elements of such a program. It is the responsibility of each manufacturer to define and document his approach to manufacturing defect reduction and control. This program shall be approved by the qualifying activity.

The goal of this procedure is to assure that defects induced during the wafer fabrication process shall be minimized to such an extent as to avoid non-conformance of product to device specifications or premature termination of its useful life. It is expected that killer defects (as defined by the manufacturer) will not be found in the delivered product. It is expected that critical defects (as defined by the manufacturer) will be controlled to meet the intended product life.

10. SCOPE:

10.1 This procedure may be conducted for complex technology microcircuits when any of the following conditions exist:

a. Minimum horizontal geometries are equal to or less than 1.5 μm final dimension of any current carrying conductors on the wafer, or

b. Interconnects (eg. metal, polysilicon) conducting current consist of three or more levels and the number of logical gates exceeds 4000.

c. Opaque materials mask design features and either or both conditions A or B apply.

10.2 This procedure may be subject to review by the acquiring activity.

10.3 Any manufacturer required to be compliant with this procedure for complex microcircuits may extend it to other devices (optional devices) that do not meet the conditions as specified in 10.1, conditions a through c herein. Extension applies only if those optional devices are manufactured primarily on the same wafer process line to most of the same process baseline (the majority of the fab equipment and process baseline used to fabricate required product as defined in 10.1, conditions a through c, is also used on extension product). All elements of the processes that are different for the extension products must meet the requirements herein.

10.4 This procedure allows for the removal, modification or reduction of inspections and screens, as a result of process improvements. For such changes, the process (and/or sub-process) must be sufficiently characterized to permit such action. Data supporting these changes must be made available to the qualifying activity upon request.

10.5 This procedure is applicable only to wafer fabrication related defects. When using this procedure the manufacturer is exempt from sections 3.1.1 (except as noted below), 3.1.2, 3.1.4, 3.1.5, 3.1.6 and 3.1.7 of conditions A and B of test method 2010. Assembly induced defects (ie: scribe damage, probe damage, bond integrity, die surface scratches and foreign material) shall be inspected at low power (30X to 60X) only, in accordance with sections 3.1.1.1, 3.1.1.6, 3.1.3 and 3.2.5 of test method 2010, conditions A and B as applicable.

10.6 This procedure does not override the requirements of any other government specifications, unless otherwise specified herein.

APPENDIX A

20. APPLICABLE DOCUMENTS. (This section is not applicable to this document.)

30. QUALIFYING ACTIVITY APPROVAL:

30.1 The manufacturer's implementation of this procedure shall be validated (audited) by the qualifying activity. The qualifying activity will issue a letter of suitability to the supplier, prior to delivery of compliant product. The letter of suitability shall specify exactly what is covered (eg: description of wafer fab line, including: location, process baseline, optional devices and technologies, etc.)

30.2 The qualifying activity shall recognize the need for auditor expertise in semiconductor wafer fabrication in order to validate a line to the requirements herein. Expertise in semiconductor wafer fabrication consists of: an understanding of wafer fabrication process flow, wafer fabrication process and measurement tools, wafer fabrication process chemistry and physics, reliability physics and defect generation and control.

40. CHARACTERIZATION OF DEFECTS AND SCREENING EFFECTIVENESS:

40.1 Products built using this procedure must have the process characterized to determine "non-critical" defects, "critical" defects and "killer" defects and to understand their impact on reliability. The characterization must consider interactive effects to the extent they have a reasonable probability of occurrence (eg: contact resistance change as affected by contact critical dimension variations interacting with dielectric film thickness variations). Defect characterization must identify categories of known defects (see 40.3), the source of each defect type (to the extent necessary to insure adequate defect control) and their population (ie: random, variation from die to die within a wafer, variation from wafer to wafer within a lot, variation from lot to lot, variation with date of manufacturer).

40.2 Methods and techniques for evaluating defect impact on reliability may include but are not limited to: designed experimentation, failure modes and effects analysis (FMEA), characterization data, analysis of field failures, analysis of unexpected failures at a manufacturer, historically available data such as public literature and proprietary information, existing reliability data, device/ process modeling, etc. It is not necessary to understand the reliability impact of each and every defect or defect combination(s); rather, the repeatable reliability performance of the delivered product must be understood in the context of defects likely to be present in the wafer process line at the time of fabrication.

40.3 Categories of defects must include the following, as a minimum (unless these defects do not occur because of process capability or other fundamental reasons):

DEFECTS:	EXAMPLES/TYPES/CONSIDERATIONS:
- Particles:	Size and composition of particles for affected mask levels and source(s) of variation.
- Conductive Traces:	Size, incidence and impact of imperfections (ie: scratches, voids, cracks, etc.). Shorting potential (ie: extrusions, hillocks, stringers, bridging, etc.). Most vulnerable areas where current carrying density violations may occur.
- Metal Corrosion:	Corrosion or corrosive elements present in metallization.
- Film Delam:	Delamination, poor adherence, excessive stress or coefficient of thermal expansion mismatches.

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DEFECTS:	EXAMPLES/TYPES/CONSIDERATIONS:
- Misalign:	Contact, via, poly/diff. alignment. Acceptable versus unacceptable alignment matching.
- Diffusion Pattern Violation:	Bridging between wells, width reduction (resistors) and enlargement.
- Dielectric Film Faults:	Blown contacts/via's, holes, cracking, active junction line exposure, excessive thickness variations.
- Die Surface Protection Faults:	Cracks, pinholes, scratches, voids, cornerholes, peeling/lifting, blistering, bond pad clearance.
- Diffusion,isolation defects,trenches, guard rings,other techniques:	Voids, notches in pattern diffusion, overlaps of diffusion, contact windows tub-to-tub connections (except by design), etc.
- Film Resistor Flaws:	Scratches, voids, potential bridging, non-adherence, corrosion, alignment, overlap between resistors and conductive traces, step coverage thinning, composition (color) changes.
- Laser Trimmed Film Resistor Flaws:	Kerf width, detritus, current carrying violations (resistor width).
- Foreign Material:	Foreign to process step/ structure (chemical stains, photoresist, ink, stains, liquid droplets).

Note: See appropriate category figures in TM 2010 Conditions A and B

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40.3.1 The following metallization concerns need to be addressed by the manufacturer in the process control procedures used to demonstrate metal integrity.

a. Silicon consumption

b. Junction spiking

c. Silicon precipitates (nodules)

d. Copper nucleation

e. Nonplanarity

f. Undercutting

g. Notching

h. Tunneling

i. Cusping

40.4 Defect characterization must identify and quantify non-critical defects, critical defects, and killer defects at each mask level and establish action limits at the appropriate inspection steps. If 100% in-line or end-of-line production screens are used to remove a specific defect, action limits and inspections may not be required at the affected mask level. Characterization must determine the major sources of variations and the impact of defect attributes (ie: size, mass, composition and quantity). Characterization must comprehend the effects of defects on the mask level being characterized and their impact on subsequent mask levels, up to and including the final product. Characterization must encompass defect behavior at worse case allowable processing locations (eg: worse case physical location for critical defect generation), at worse case boundary conditions (ie: thickness, temperature, gas flow, etc.) and to worse case design rules. See Attachment #1: Example of Defect Characterization.

40.5 In accordance with the results of defect characterization, the action limits for defects must be less than the level at which the defects are known to adversely affect the reliability and performance of the device (the use of process "safety margins" must be invoked, eg: if an aluminum line with a 25% notch is known to shorten the life of the device, then margin limits for the notching must be accounted for, that is, the allowable notch limit must be less than 25%). By definition, any observation of a killer defect (one or more) exceeds its action limit.

40.6 The results of the defect characterization shall be used to establish inspection sampling requirements (ie: sample sizes and sampling frequency) and analytical techniques for in-line and end-of-line process inspections (see section 50).

40.7 The manufacturer shall establish a process baseline and put the process under formal change control after defect characterization has been completed and in-line and end-of-line inspection steps are implemented. Any changes that adversely affect the defects require re-characterization of the defects (eg #1: changing fabrication gowns may affect particulate generation and must be determined if they are equivalent or better than gowns used when the original defect characterization was completed, if better no further action, if worse, re-characterization of the line. eg #2: a change in HCl (hydrochloric acid) chemical supplier requires comparative analysis of new supplier to old supplier, relative to trace impurities, followed by an engineering evaluation to validate the impact on product. Discovery of excessive, new impurities that could not be proven benign would require re-characterization before the new supplier could be used).

40.8 Any manufacturers' imposed in-line or end-of-line screens must demonstrate their effectiveness in eliminating killer and critical defects in excess of their allowable action limit(s).

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40.9 Any new defects that surface as a result of excursion containment, yield analysis, customer returns, inspection procedures, (etc.) must be characterized in accordance with specifications in section 40.

50. INSPECTION AND TEST SYSTEM:

50.1 Control and reduction of defects will result from an inspection and test system, employing process and product monitors and screens. The inspection and test system is incorporated throughout the wafer fab process flow (in-line and/or end-of-line). It is expected that an inspection and test system will prevent killer defects from appearing in the delivered product. See Attachment #2: Example of an Inspection and Test System.

50.2 Inspection and test procedures shall form an integrated approach that in total controls and reduces defects. The procedure shall consider the following criteria where applicable:

50.2.1 The supplier shall define and implement inspection and test procedures at appropriate points to monitor killer and critical defects (as identified in section 40).

50.2.2 The inspection and test procedures shall consist of sampling plans which recognize the sources of defects and their variance (ie: random, variation from die to die within a wafer, variation from wafer to wafer within a lot, variation from lot to lot, variation with date of manufacturer). Sample plans shall be consistent with statistical practices (distributional form and alpha/beta risks). The population to be sampled must be homogeneous.

Examples of homogeneity considerations include:

Lots that have been split or otherwise altered for rework are not considered homogeneous, unless otherwise demonstrated, and therefore require independent sampling of the non-homogeneous (reworked) population. If different pieces of processing equipment are used at the same process step (mask level), for the same purpose (eg: use of multiple wafer steppers on the same wafer lot), these tools must demonstrate the killer and critical defect characteristics are statistically comparable, for a given wafer lot to be considered a homogeneous population.

50.2.3 Inspections and tests must consider, but are not limited to worst case locations (as identified in Section 40). Examples Include: 1) At an LPCVD operation, the defect characterization might determine particles to be consistently higher on wafers at, or near, the door end of the tube, sampling at LPCVD must comprehend inspection at this location. While characterizing metal bridging, one location on the die might appear consistently more prone to bridging than other die locations, sampling criteria should include inspections at this location.

50.2.4 Inspection and test procedures must make use of "look backs". A look back inspection examines the current process step and one or more preceding process steps. This procedure allows for inspection/test of telescoping effects (magnifies or enhances the defect) and/or defects decorated by subsequent processing. This technique allows for additional opportunities to inspect/test for killer and critical defects in preceding layers.

Examples Include: 1) While inspecting field oxidation it is possible to look back at pattern definitions in previous levels. 2) A defect is known to be more obvious after a subsequent LTO deposition (the defect size telescopes), therefore an inspection at LTO could effectively look back at the previous operation which generate a defect.

50.2.5 Inspection and test procedures must define action limits and the appropriate data to be recorded. Data recording shall recognize the need for wafer, lot, or product disposition and corrective action (eg: data may need to be classified by machine number, tool, wafer lot, operator, etc.). These types of data and action limits are derived from the defect characterization (as identified in section 40) and shall take into account relevant attributes of defects (ie: size, color, mass, composition, density). Action limits shall comprehend safety margins (as specified in section 40).

50.2.6 As a result of defect characterization (see section 40), non-critical defects shall be monitored, unless the non-critical defect has been proven not to have any influence on the finished product, regardless of incidence or defect density. This is required to address situations when:

a. Non-critical defects may mask detection of killer and critical defects (eg: a change in color obscures visual observation of a killer or critical defect).

b. A non-critical defect becomes critical as a result of increased defect density (eg: due to an increase of non-critical defects, a chain is formed, creating a critical defect).

c. An inconsistency between the incidence of non-critical and critical defects, signaling a change in the process that must be explained.

50.3 Any in-line or end-of-line screens shall be defined, implemented and documented when used in lieu of, or to supplement inspections/tests for killer and critical defects. The population to be screened must also be defined and documented (eg: wafers, die, portions of wafers, wafer lots, etc.). These procedures shall only include those screens proven to be effective, per requirements in section 40. Records of screening results must be maintained (accept/ reject data).

50.4 The Analytical tools and product, process reliability and equipment monitors must have sufficient capability to measure defect attributes as defined in section 40. This includes changes in critical defect density (eg: if defect characterization indicates a 0.1 μm particle is a critical defect at a given mask level, the inspection procedure must be capable of detecting and quantifying the incidence of particles this size and larger). See attachment #3: Analytical tools.

60. EXCURSION CONTAINMENT FOR MATERIAL EXCEEDING ACTION LIMITS:

60.1 The manufacturer shall confirm that the action limit has been exceeded. This may be accomplished by: record review, reinspection, increased sampling, higher magnification visual, etc.

60.2 If the condition is confirmed, the manufacturer shall identify and act upon affected material (ie: single wafer, multiple wafers, whole lot, batches of lots, whole line).

60.3 The manufacturer shall perform analysis on affected material and establish a disposition strategy (ie: root cause analysis, scrap, screen, rework, etc.).

60.4 The manufacturer shall implement appropriate short term/long term corrective action (ie: screens, process change, equipment change, design rule change, etc.)

70. YIELD ANALYSIS:

70.1 The manufacturer shall establish a yield analysis system as a monitor point to confirm effectiveness of inspections and tests. Particular attention should be given to those lots that exhibit abnormal variation from expected yields, as defined by the manufacturer.

70.2 Yield analysis should include root cause analysis to determine and drive process improvements.

70.3 The manufacturer shall coordinate the yield analysis system with a formal material review board (MRB), or other approved disposition authority, to drive corrective action for "excursion" material (killer or critical defect escapes).

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80. SYSTEM FOR UNEXPECTED FAILURE:

80.1 The manufacturer shall establish a system to analyze field returns. Determine root cause of failure and drive action for: identification, containment, disposition, notification and corrective action.

80.2 The manufacturer shall implement a system to capture and contain killer or critical defect escapes originating in wafer fabrication but found elsewhere in the factory (ie: sort, assembly, test, etc.) and implement corrective action.

80.3 The manufacturer shall review unexpected failures through a formal material review board (MRB), or other approved disposition authority, that brings together the expertise to identify and contain the discrepant product (killer or critical defects), to notify internal and external customers, as needed and to implement corrective action. The circumstances for convening an MRB must be defined.

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90. DOCUMENTATION AND DATA REQUIREMENTS:

90.1 The results of defect characterization, assessment of effectiveness of screening methods, sampling and inspection methodologies, procedures and systems for controlling changes shall be made available to the qualifying activity, upon request.

90.2 Inspection and screening procedures must be placed under formal document and change control. Data records must be maintained and made available to the qualifying activity, upon request. Data retention must be maintained in accordance with the procurement specifications.

90.3 Excursion containment procedures must be documented and placed under document control. When appropriate, records of root cause analysis, containment, disposition and corrective action (via an MRB or other approved disposition authority) must be maintained and made available to the qualifying activity, upon request. Varying degrees of formality are essential to any manufacturer's line; therefore, disposition authority may range from the responsible individual to a formal MRB and documentation may range from initialing a lot traveler to a formal MRB report. The manufacturer shall have prescribed guidelines for the various methods allowable for disposition action and documentation (eg: if product deviation is within certain spec or action limits, the line engineer may have disposition authority; if these limits are exceeded, some higher disposition authority may be required). Records must be retained in accordance with the procurement specifications.

100. DEFINITIONS:

(Note: The definitions herein are applicable to this procedure only)

Action limits -Numerical limits for defect densities, counts, or other metrics used to trigger a response. This response may involve: investigation, root cause analysis, disposition and corrective action.

Alignment - Also known as "overlay" or "registration". The proper placement of one photolithography layer atop a preceding layer.

Blown contact - A phenomena most often associated with the wet etching of contacts. The etch proceeds laterally at a rate much greater than is expected or desirable. Typically, the lateral etching is non-uniform with respect to the desired contact profile.

Cornerholes - A process phenomena associated with narrow gaps between lines of topography. In particular, where those lines form an angle of approximately 90 degrees (form a "corner"). A cornerhole is formed when photoresist cannot cover the severe topography generated by structures like these, allowing a subsequent etch to remove film in the gap between the lines.

Critical Defects - Defects known or suspected to cause premature failure but only under certain conditions that have a small probability of occurrence or any defect that cannot be proven as non-critical.

Defect escapes - Lots, wafers or die which contain defects that unintentionally get through a manufacturer's inspection and test system.

DI (DI water) - De-ionized water. Used for wafer cleaning.

Discrepant material - any material determined to be unsuitable for its destined form, fit or function, as specified by the MRB or other disposition authority.

Elements of the process - Any fundamental piece (building block) of the wafer fab process or process step (eg: thermal ramp rates, etch rates, recipe' steps, incoming raw materials, etc.). This includes quantifiable/ measurable chemical and physical phenomena of the wafer fab process.

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End-of-line - The steps after wafer fabrication and initial testing (electrical test, wafer sort). This includes most of what is commonly referred to as "assembly/test".

Excursion containment - Efforts undertaken to find, limit and segregate discrepant material.

Homogeneous - The state in which every wafer in a lot has received the exact same processing, including: correlated equipment (as specified in appendix A of MIL-PRF-38535), same recipes, same operations and same materials. This does not include metrology or inspection steps.

ILD - Inter-layer dielectric. Typically refers to the layer separating different conductor material layers but is occasionally used to describe the layer between first metal and the underlying layers.

In-line - The process steps that comprise wafer fabrication from initial starting material through and including initial test (electrical test and sort).

Inspection - Any procedure designed to detect or measure defects. Depending on the equipment or procedure, the quantity or types of defects may or may not be measurable; depending on the inspection, defects may or may not be removed. These procedures may utilize visual detection (human or automated), laser surface scatter, in-situ particle detectors, etc.

Interconnects - Any structures on the wafer surface used for electrical connection from one device (or portion of a device) to another. These structures are typically made of polysilicon or metal.

Killer defect - A defect that has a high probability of causing failure, under any condition, at some given point in a products intended life.

Letter of suitability - A formal written document from the qualifying activity stating the manufacturer has sufficient capability and competency to implement/execute the subject procedure.

Look-back inspection - An inspection that is capable of detecting defects not only at the current process layer but also at some number of preceding process layers. Ideally, this inspection allows for differentiation between defects at the current process layer and those of preceding ones.

LPCVD - Low-pressure chemical vapor deposition.

LTO - Low-temperature oxidation or low-temperature oxide.

LYA - Low-yield analysis. A method for determining the reason for yield loss by analyzing low-yielding material.

Mask level - A structure (electrical, physical and/or chemical) on, in, above or below a wafer substrate, achieved or modified by various sequential physical or chemical processes, such as: oxidation, diffusion, etch, film deposition, implant, etc.

Material review board (MRB) - A group of individuals who have sufficient expertise and are duly authorized by the facility to disposition discrepant or non-conforming material.

Monitor - Inspections or tests performed on a sampled population.

Non-critical defect - A defect that has been demonstrated not to cause premature failure, regardless of defect density, defect placement on the die or defect size.

PM - Preventive maintenance procedure.

Poly - Polycrystalline silicon.

Process baseline - An approved set of instructions, conditions and procedures for wafer fabrication.

Product - Material resulting from the output of a wafer fab process that is ultimately destined for delivery to a customer.

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Screens - 100% of a population (dice or wafers) is inspected or tested and all material containing targeted defects are rejected.

Sub-process - Any number of related process steps leading to an outcome on the wafer. Examples would include poly interconnect formation (comprised of poly deposition, poly layer lithography, poly etch and resist strip) and contact formation (dielectric deposition, contact layer lithography, contact etch and resist strip).

Telescoping defects - Defects which increase in visibility, due to an apparent increase in size, as wafers are processed through subsequent operations. The increase is a function of the defect being decorated by etches or films, the defect acting as a nucleation site for subsequent depositions or by the defect creating non-uniform regions in a film or oxide.

Test - 1) Evaluate (ie: stress and measure) reliability, quality and performance; 2) ensure the defects present do not affect reliability, quality or performance.

Unexpected failures - Failures that are not detected, or cannot be predicted, using the manufacturer's standard in-line inspection and containment plans.

Wafer process - The materials, equipment, operations and environment necessary to manufacture a product or family of products. This includes all potential sources of defect generation.

Yield analysis - The analysis of die yields to determine failure modes and defect mechanisms. This can entail analyzing low yielding material, average yielding material or high yielding material or combinations of these items. This type of analysis can be used to validate in-line monitors.

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EXAMPLE 1 - QUALITY SCENARIO:

A defect characterization has been performed on an LPCVD operation. The primary defect mechanism was found to be particles. These particles were quantified using a laser surface-scanning tool. The results show that the particles fell into three size distributions: 1) <0.3 microns randomly distributed from wafer to wafer and within a wafer, 2) about 1.0 microns with a higher density near the pump end of the deposition tube, and 3) greater than 6.0 microns that appeared heavily on some wafers but did not appear at all on others. The defects in the 1.0 micron or less categories were found to be relatively small, dark particles when viewed with an optical microscope. The larger particles (>6 microns) appeared as large, black particles that appeared to be on the wafer surface. A compositional analysis of particles from the three distributions showed that the first two types (<0.3 microns and about 1.0 microns) were composed of Si and O, essentially the same composition as the deposited film. The large particles were composed of primarily Fe and Ni.

Wafers containing defects from the smaller size distributions were processed through the subsequent patterning operations. The 1.0 micron particles were observed to have an affect on the subsequent pattern when they occurred adjacent to the patterned lines. The <0.3 micron particles had no observable effect. Both defects were characterized using optical microscopes and an automated pattern inspection system. After resist strip, the 1.0 micron particles were gone, with only their effects on the patterning operation being visible. The <0.3 micron defects were still observable after resist strip. After a subsequent LTO deposition, the <0.3 micron particles appeared to "telescope" in size to about 1 micron due to the conformal nature of the LTO film. The "telescoped" particles had a noticeable effect on the next patterning operation. Observation of both particle types using an SEM (scanning electron microscope) showed that the 1.0 micron particles appeared to be incorporated into the film, whereas the <0.3 micron particles appeared to be under the film. This was consistent with the defect behavior observed during subsequent processing.

The signal from the large particles suggested contamination from a stainless steel source. Observation of the defect with an SEM showed that the defects were on top of the deposited film. The defects were found to be coming from the unload arm of the LPCVD system. The unload arm was occasionally striking another piece of the load/unload assembly, generating metal particles each time it did this.

The characterization of particle defects from this LPCVD operation resulted in the following monitoring plan: 1) The alignment of the unload arm was found to be most affected by the preventive maintenance procedure performed on the load/unload assembly once each week. As a result, a bare silicon particle monitor is run after each PM, before any product wafers can be run on the system. The monitor is set to look for 6 micron and larger particles with the expectation that no such particles should be present if the unloader is working properly. 2) The source of the 1.0 micron particles is unknown. What is known is that these defects are always worse near the pump-end of the tube. As a result, the monitor for this particle source is run at the pump end of the tube, with a door end monitor run simultaneously as a "control". Different action limits exist for each monitor. 3) The small particles were found to be very difficult to monitor at the LPCVD operation since they fell into the "noise" caused by limitations in the particle detection equipment. However, they are easily monitored in a "look-back" fashion after the subsequent patterning operation using the automated pattern inspection system. As a result, this defect is monitored at the post-patterning inspection step with action limits initiating feedback to the LPCVD operation.

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EXAMPLE 2 - RELIABILITY SCENARIO:

Characterization of particles at a gate oxide preclean operation showed that the particles contributed by the operation tend to be small (0.2 microns) and vary in concentration from 0.02 d/cm^2 to 0.8 d/cm^2 depending on how heavily the station is utilized. Defect density increased as the number of wafers processed through the station increased.

Wafers from this operation were selected such that some of them had low defect densities (approximately 0.3 d/cm^2) and the remainder had high defect densities (approximately 0.8 d/cm^2). These wafers were processed through the line and the die from these wafers subjected to high voltage stress testing. The results of the tests were that the low and moderate defect density groups showed levels of gate leakage consistent with the historical process baseline. The high defect density die show gate leakage that was 3 times that of the historical baseline and resulted in barely acceptable failure rates.

As a result of this characterization, a particle monitor was implemented at gate oxide preclean with an upper limit of 0.6 d/cm^2 to allow some safety margin from the gate leakage problems seen at 0.8 d/cm^2. However, due to resource limitations, this monitor can only be run once every shift (approximately every 12 hours). It is likely that the movement of material in the line will lead to the station occasionally exceeding its control limits between monitors. A second preclean station is scheduled to be installed in about three months. This station will provide enough capacity to prevent wafer-volume related out-of-control particle conditions at the gate preclean operation. In order to ensure that no material with bad gate oxide is shipped during the interim period (before the new station comes on-line), a manufacturer imposed screen (high-voltage stress test) is used on all material processed between a failing monitor and the last known good monitor at this operation.

In order to show that the screen is effective, particle monitors are processed through the station with every lot of wafers. This test is done for a period of time sufficient to yield multiple lots at various defect densities. Die from each of these lots are processed through the high-voltage screen. The results show that the screen is 100 percent effective at detecting the lots with defect densities greater that 0.6 d/cm^2. The results show a solid correlation between gate oxide preclean defect densities and gate oxide leakage levels. The screen is then used to augment station particle level data and remains in place until the second station is installed and qualified.

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EXAMPLE OF DEFECT DETECTION FOR KEY PROCESS STEPS:

PROCESS STEP MONITOR	PRODUCT MONITOR	EQUIPMENT MONITOR	RELIABILITY
Wafer start	Incoming Si QA	NA	NA
EPI	Laser surface particle scan.	Gas flow/pressure, chamber temp	NA
Start Oxide	Oxide thickness, laser surface particle scan.	Tube temp profile, CV, thermocouple cal, gas flows, tube particle checks using laser surface scan.	Oxide integrity test wafers
Patterning/Well Implant	UV light particle insp, optical pattern insp, e-test parametrics.	Exposure dose, reticle/ pellicle inspection, stepper stage checks implant dose processor and voltage calibration, DI water resistivity. Particle checks of stepper, implanter, coat/develop tracks using laser surface particle scan.	LYA
Active Region Patterning/Gate Oxide (no 2010 equiv.)	Alignment check, optical inspection, automated pattern inspection, UV light and laser surface particle inspections, in-line SEM CD measurement, e-test parametrics.	Exposure dose, reticle/ pellicle inspections, stepper stage checks, tube temp profile, CV thermo-couple cal, gas flows, DI water resistivity. Particle checks of stepper, diffusion tube, coat/develop tracks using laser surface particle scan.	Oxide integrity test wafers, comb/serpentine test structures, LYA.
Poly Dep/Patterning	Alignment check, optical and automated pattern inspection, laser surface particle inspections, in-line SEM CD measurement, e-test parametrics.	Dep tube pump/vent speed, MFC calibration, gas flows, pressures, temperature. Expose dose, reticle/pellicle checks, stepper stage checks. DI water resistivity. Particle checks on poly tube, stepper and coat/develop tracks using laser surface particle scan.	Comb/serpentine test structures, buried contact check, LYA.

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PROCESS STEP MONITOR	PRODUCT MONITOR	EQUIPMENT MONITOR	RELIABILITY
Patterning/ S/D Implant	Alignment check, optical pattern inspection, UV light or laser surface particle inspections. E-test parametrics.	Exposure dose, reticle/ pellicle inspection, stepper stage checks. implant dose processor and voltage calibration, DI water resistivity. Particle checks of stepper, implanter, coat/develop tracks using laser surface particle scan.	LYA.
ILD 1/Patterning	Alignment check, auto-mated pattern inspection, UV light and laser surface particle inspection, e-test parametrics. In-line SEM CD measure.	Exposure dose, reticle/ pellicle inspection, stepper stage checks. ILD deposition system temp/pressure. MFC calibration, gas flows. DI water resistivity. Particle checks on stepper, coat/develop tracks and ILD deposition system.	Refractive index. % phosphorus. Film integrity tests (break-down, etc.). LYA.
Metal 1/Patterning	Alignment check, auto-mated pattern inspection, laser surface particle inspection, metal resistivity/specularity, In-line SEM CD measurement and electrical CD measure, e-test parametrics.	Expose dose, reticle/ pellicle inspection, stepper stage checks. Metal dep thickness, RGA of dep system, gas flows, pressures, pump/vent rate checks, metal resistivity/ specularity. Particle checks on metal dep system, stepper and coat/develop tracks using laser surface scan.	Contact chains, Metal-to-poly contact, Metal-to-diff contacts, electromigration monitors, metal CDs (at end of line), step coverage. LYA.
ILD 2/Patterning.	Similar to ILD1.	Similar to ILD1.	Similar to ILD1.
Metal 2/Patterning	Similar to Metal 1	Similar to Metal 1	Similar to Metal 1 with addition of Via chains, Metal 2-to-Metal 1 contact.
Glassivation/ Bond pads	Coarse alignment check, optical inspection of bond pads to ensure clearing and of passivation for cornerholes.	Glassivation thickness, phos content, temp, pressure and flows. Exposure dose, stepper stage parameters. Part-icle checks on all equip.	Acid bath for glass integrity. Acoustic micro-scopy.

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ATTACHMENT 2 (Continued)

Backside prep/ Chrome/Gold Dep/ E-test/Sort	Post-tape visual, post-grind visual, post-detape visual (all optical). Warpage check, thickness check. Chrome/gold thickness checks, visual for backside appearance post-dep. Post-sort visual (optical).	Grind rate check, grind pressure check. Evaporator pressure/leak rate checks, RGA, power and gas flows. Warpage and thickness checks on test wafers.	Warpage and thickness checks. Die cracking and adhesion monitors at assembly.

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ANALYTICAL TOOLS/MONITORS AND SCREENS

Analytical tools may include, but are not limited to the following:

a. Oblique light, very low magnification

b. Optical microscope

c. Laser scattering (or equivalent)

d. Automated pattern inspection

e. Alignment measurement tool (automated, high-resolution)

f. Non-destructive S.E.M.

g. Wafer mapping

Broad Use of Tools for Inspections (tools may include but are not limited to):

Oblique Light, visual inspection: A quick and gross visual inspection at very low mag (1X to 20X) using a light source projected onto the wafer and tilting the wafer to detect large particles. This is an inspection step used in-line at various key process steps.

Optical microscope: Looks for defects that are detectable optically (eg: metal stringers, large particles, visible foreign material, visible resist imperfections such as drips, visible voids and cracks, visible misalignment, etc.). This tool is used at different magnifications, at beginning and/or end of key process steps (200X optical sampling in-line for a selected key process step and 800X optical check at the end of a key process step and before proceeding to the next key process step).

Laser scanning (or equivalent): Used to detect any anomalous surface defects (eg: very fine particles that may not be detected by optical microscopy). May be used in numerous process steps and is particularly important early in the process to control telescoping defects.

Automated Pattern recognition: Used to verify integrity of two dimensional geometries (detects anomalies such as: voids and cracks in the metal, metal bridging, diffusion and poly faults or any other abnormalities in an expected pattern).

Automated high resolution alignment measurement tool: Used for inter-level registration at very fine tolerances (on the order of 0.1 μm). This tool is used to align very fine critical geometries undetectable by conventional high power optical registration tools.

Non-destructive S.E.M: In-line product monitor used for very high power visual examination of critical process steps (critical dimension, step coverage, metal thinning, etc.).

Wafer mapping: An analytical technique using data from various inspection tools (eg: automated pattern recognition tools, laser scanning tools, e-test results) for defect characterization and partitioning.

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Product, Process and Reliability Monitors/Screens

These monitors/screens incorporate inspections/tests which may include but are not limited to):

In-line electrical test (E-test): This monitor is used to measure electrical characteristics of transistor elements (sheet resistance, doping levels and other transistor parametrics), contact chains, metallization structures (line width, thickness, resistance) and via structures. Parametric failures detectable by e-test may be indicative of an unacceptable incidence of killer or critical defects.

Test structures: Special structures used to detect killer or critical defects (eg: serpentine structures used to detect metal continuity such as voids, comb structures for bridge detection and to verify field oxide isolation integrity, electromigration structures to verify metal integrity and step coverage and inter-layer dielectric structures to verify e-field integrity).

Periodic reliability studies: Intended to verify design life margins of the technology.

Yield Analysis: Used to validate effectiveness of in-line monitors by a closed loop feedback system that detects the effects of killer or critical defect escapes not caught in-line. Actions may include: scrapping lot, root cause analysis and correction, lot screening, etc. (see section 70).

Other monitors: Used to measure key process elements. Examples may include but are not limited to:

a. Metal reflectivity and resistivity (to check metal irregularities such as: hillocks formations, step thinning, changes in granularity, voiding, etc.).

b. Ionic contamination.

c. Refractive index for interlayer dielectric thickness measurements.

d. Post wafer probe visual inspection. A monitor performed on randomly selected post probe wafer(s) beginning with visual high power inspection and may be followed by subsequent detailed analysis (S.E.M., EDX, layer strip-back, etc.). This is used to confirm the effectiveness of in-line monitors.

e. Acid bath (used for quick detection/ decoration of glassivation defects, cracks and holes) or acoustic microscopy (to measure glassivation integrity).

Equipment Monitors (equipment monitors may include but are not limited to):

Particle checks: Performed on process equipment such as: etch, metal deposition, implant, diffusion, dielectric deposition, photoresist material and application. Particles of sufficient size and density may lead to killer or critical defects (metal bites, dielectric holes, poly/ diffusion geometry changes, etc.).

Residual Gas Analysis: Used to monitor gas integrity of key process equipment (eg: metal deposition equipment to control corrosion).

Photolithography exposure equipment: Used to verify critical parameters and controls for photolithography operation (pre-alignment checks, stage accuracy, machine alignment accuracy using reference patterns, lens distortion check, alignment accuracy, wafer chuck flatness measurement, lens focus check, reticle rotation, etc.)

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METHOD 5005.17

QUALIFICATION AND QUALITY CONFORMANCE PROCEDURES

1. PURPOSE. This method establishes qualification and quality conformance inspection procedures for microelectronics to assure that the device and lot quality conforms with the requirements of the applicable acquisition document. The full requirements of groups A, B, C, D, and E tests and inspections are intended for use in initial device qualification, requalification in the event of product or process change, and periodic testing for retention of qualification. Groups A and B tests and inspections are required for quality conformance inspection on individual inspection lots as a condition for acceptance for delivery. Groups C and D tests are required for quality conformance inspection on a periodic basis as a condition for acceptance for delivery. Group E tests are qualification and quality conformance procedures to be utilized only for radiation hardness assurance levels as specified in Table V. In general, it is intended that the device class level to which qualification or quality conformance inspection is conducted would be the same device class level to which screening procedures (in accordance with method 5004) are conducted. However, it is permissible for qualification or quality conformance procedures to be specified at a higher quality level (in no case shall a lower level be permitted) to reduce the potential percent-defective. It is also permissible to specify tightened inspection criteria for individual subgroups where experience indicates justifiable concern for specific quality problems.

NOTE: Reference to method 5005 on a stand-alone basis (not indicating compliance or noncompliance to 883) requires full compliance to 1.2.1 of this standard (see 1.2.2 of this standard).

2. APPARATUS. Suitable electrical measurement equipment necessary to determine compliance with the requirements of the applicable acquisition document and other apparatus as required in the referenced test methods.

3. PROCEDURE. The procedure contained in 3.1, 3.2, or 3.3, as applicable to the microcircuit type and class, shall apply for all qualifications and quality conformance inspection requirements. Subgroups within a group of tests may be performed in any sequence but individual tests within a subgroup (except group B, subgroup 2) shall be performed in the sequence indicated for groups B, C, D, and E tests. Where end-point electrical measurements are required for subgroups in groups B, C, D, and E testing, they shall be as specified in the applicable device specification or drawing. Where end-point measurements are required but no parameters have been identified in the acquisition document for that purpose, the final electrical parameters specified for 100 percent screening shall be used as end-point measurements. Microcircuits which are contained in packages which have an inner seal or cavity perimeter of 2 inches or more in total length or have a package mass of 5 grams or more may be treated in accordance with the optional provisions below, where applicable.

Constant acceleration. Delete test condition E and replace with test condition as specified in the applicable device specification or drawing. Unless otherwise specified, the stress level for large monolithic microcircuit packages shall not be reduced below test condition D. If the stress level specified is below condition D, the manufacturer must have data to justify this reduction and this data must be maintained and available for review by the preparing or acquiring activity. The minimum stress level allowed is condition A.

Qualification and quality conformance inspection requirements for radiation hardness assured devices are in addition to the normal classes level S and level B requirements. Those requirements for each of the specified radiation levels (M, D, P, L, R, F, G and H) are detailed in Table V.

Qualified manufacturers list (QML) manufacturers' who are certified and qualified to MIL-PRF-38535 or who have been granted transitional certification to MIL-PRF-38535 may modify the class level B tables (Tables I, II Class B, III, and IV) as specified in the applicable device specification or Standard Microcircuit Drawing and as permitted in 1.2 of MIL-STD-883 provided the modification is contained in the manufacturer's Quality Management (QM) plan and the "Q" or "QML" certification mark is marked on the devices. For contractor prepared drawings with specific references to individual test methods of MIL-STD-883 (e.g., method 1010, method 2002, etc.); these test methods may not be modified by a QML manufacturer without the knowledge and approval of the acquiring activity.

3.1 Qualification procedure for class level S microcircuits.

3.1.1 Qualification for class level S QML-38535 listing. Qualification testing for class level S microcircuits shall be in accordance with appendix A of MIL-PRF-38535.

3.1.2 Steady-state life test. In the case of multiple sublots contained in the class level S inspection lot, the sample size number shall be selected from the sublots in the nearest whole number of devices proportionately to the number of devices in each sublot. Where this results in less than 10 samples from any sublot, additional samples shall be selected from that sublot(s) to provide a minimum of 10 samples from each sublot. Any sublot which exhibits more than one failure shall be rejected from the inspection lot.

3.2 Quality conformance inspection procedures for class level S microcircuits. Each class level S quality conformance inspection lot shall be assembled in accordance with the class level S requirements of appendix A of MIL-PRF-38535. Quality conformance testing shall be in accordance with Tables I, II Class S, and IV.

3.2.1 Notification of nonconformance. Whenever any of the following occurs, the qualifying activity shall be immediately notified:

a. The number of failures in a single subgroup of Table II exceeds the acceptance number on two successive lots (applicable to Class S only) subgroups 2b, 2c, 2d, 5, and 6).

b. The number of failures for the resubmitted sample in accordance with A.4.3.3.1 of appendix A of MIL-PRF-38535 exceeds the acceptance number on two successive lots on the following Table II subgroups: (applicable to Class Q only) 1, 2a, 2b, 2d, and 4.

c. For a given device type withdrawal from quality conformance testing for any reason on two successive lots.

d. Following initial notification, the manufacturer shall provide the qualifying agency or its designated representative with data which indicates the reason(s) for the reported nonconformance, contributing factors, and proposed corrective action.

e. Two successive lots failing group E testing, or 10 percent or more of the lots requiring the add-on sampling procedure.

In the absence of timely compliance with the above, or corrective action acceptable to the qualifying activity, action may be taken to remove the product from the class level S QML-38535.

3.3 Qualification and quality conformance inspection procedures for class level B microcircuits. Qualification or quality conformance inspection for microcircuits shall be conducted as described in the groups A, B, C, D, and E tests of Tables I, II, III, IV, and V herein and as specified in the applicable device specification. For quality conformance inspection, each inspection lot (sublot) shall pass groups A, B and (when applicable) E test (or be accepted in accordance with 3.5 herein), and the periodic group C and D tests shall be in accordance with appendix A of MIL-PRF-38535.

3.4 Acceptance procedure. Acceptance numbers, provisions for resubmission, and criteria for acceptance or rejection of lots shall be as specified herein and in the applicable device specification or drawing.

3.5 Sample selection. Samples shall be randomly selected from the assembled inspection lot in accordance with appendix A of MIL-PRF-38535 (and in accordance with Table V herein for group E) after the specified screen requirements of method 5004 have been satisfactorily completed. Where use of electrical rejects is permitted, unless otherwise specified, they need not have been subjected to the temperature/ time exposure of burn-in.

3.5.1 Alternate group A testing. Alternate procedures for performing group A inspection on each inspection lot or sublot may be used at the manufacturer's option provided that the qualifying activity has previously approved the alternate procedure and flow being used by the manufacturer. A different operator shall check the entire test setup and verify the use of the correct test program prior to testing the group A sample.

3.5.1.1 Inspection lot sample selection. When this option is used, test samples for each individual group A subgroup shall be randomly selected from the inspection lot after 100 percent screening of that subgroup (or subgroups, in the event that multiple subgroups are tested at the same temperature in sequence with the same test program). All devices in the inspection lot or sublot shall be available for selection as a test sample and a fully random sample shall be selected from the total population of devices.

3.5.1.2 Concurrent sample selection. When this option is used, test samples from each individual group A subgroup(s) shall be randomly selected concurrent with the 100 percent screening of that subgroup(s) and tested subsequent to screening each individual device of that subgroup(s). When this option is used, the following requirements apply:

a. A documented verification methodology and operating procedure shall be set up to assure the integrity of the total test system, that the product is being tested with correct test conditions and that all required screening and group A testing is being performed.

b. The group A samples shall be sorted out separately from the balance of the lot and the sample size verified. If because of higher than expected yield loss, the number of samples tested are less than the required sample size, (116 units), then additional samples shall be randomly selected and tested.

c. Each group A reject shall be sorted out separately.

d. All screening rejects shall be segregated from the acceptable product and the physical count verified against the test system attribute data.

e. When sorting (e.g., speed or power) is completed during the final electrical screening, each individual device type screened shall have a full group A sample selected and tested.

f. For small lots, where the lot size is less than the required sample size (116 units) each device in the lot shall be double tested (i.e., 100 percent screening and 100 percent group A).

TABLE I. Group A (electrical tests). 1/

Subgroups	Tests	MIL-STD-883 test method and conditions Minimum sample size quantity (accept no.) 2/ 3/ 4/ 5/		
		Class Q (class level B)	Class V 6/ (class level S)	Class Y 6/ (class level S)
1	Static tests at +25°C	116(0) or 100 percent/ 0 sample	116(0) or 100 percent/ 0 sample	116(0) or 100 percent/ 0 sample
2	Static tests at maximum rated operating temperature			
3	Static tests at minimum rated operating temperature			
4	Dynamic tests at +25°C	116(0) or 100 percent/ 0 sample	116(0) or 100 percent/ 0 sample	116(0) or 100 percent/ 0 sample
5	Dynamic tests at maximum rated operating temperature			
6	Dynamic tests at minimum rated operating temperature			
7	Functional tests at +25°C	116(0) or 100 percent/ 0 sample	116(0) or 100 percent/ 0 sample	116(0) or 100 percent/ 0 sample
8A	Functional tests at maximum rated operating temperature			
8B	Functional tests at minimum rated operating temperature			
9	Switching tests at +25°C	116(0) or 100 percent/ 0 sample	116(0) or 100 percent/ 0 sample	116(0) or 100 percent/ 0 sample
10	Switching tests at maximum rated operating temperature			
11	Switching tests at minimum rated operating temperature			

1/ The specific parameters to be included for tests in each subgroup shall be as specified in the applicable acquisition document. Where no parameters have been identified in a particular subgroup or test within a subgroup, no group A testing is required for that subgroup or test to satisfy group A requirements.

2/ At the manufacturer's option, the applicable tests required for group A testing (see 1/ herein) may be conducted individually or combined into sets of tests, subgroups (as defined in Table I), or sets of subgroups. However, the manufacturer shall pre-designate these groupings prior to group A testing. Unless otherwise specified, the individual tests, subgroups, or sets of tests/subgroups may be performed in any sequence.

3/ The sample plan (quantity and accept number) for each test, subgroup, or set of tests/subgroups as pre-designated in 2/ herein, shall be 116/0.

4/ A greater sample size may be used at the manufacturer's option; however, the accept number shall remain at zero. When the (sub)lot size is less than the required sample size, each and every device in the (sub)lot shall be inspected and all failed devices removed from the (sub)lot for final acceptance of that test, subgroup, or set of tests/subgroups, as applicable. For those lots having a quantity of less than 116 devices, the test shall be imposed on a 100 percent basis with zero failure.

5/ If any device in the sample fails any parameter in the test, subgroup, or set of tests/subgroups being sampled, each and every additional device in the (sub)lot represented by the sample shall be tested on the same test set-up for all parameters in that test, subgroup, or set of tests/subgroups for which the sample was selected, and all failed devices shall be removed from the (sub)lot for final acceptance of that test, subgroup, or set of tests/subgroups, as applicable. For device class V or class Y (class level S), if the testing results in a percent defective allowable (PDA) greater than 5 percent, the (sub)lot shall be rejected, except that for (sub)lots previously unscreened to the tests that caused failure of this percent defective, the (sub)lot may be accepted by resubmission and passing the failed individual tests, subgroups, or set of tests/subgroups, as applicable, using a 116/0 sample.

6/ For class V and class Y, group A electrical tests additional requirements see paragraph B.4.3 appendix B of MIL-PRF-38535.

TABLE II. Group B tests (Mechanical and environmental test).

Subgroups 1/	Group B tests for QML microcircuits (MIL-PRF-38535)			Group B tests for class level B and S microcircuits (TM 5005 of MIL-STD-883)	
	Class Q	Class V	Class Y	Class level B	Class level S
Subgroup 1	Resistance to solvents 2/ TM 2015 3(0)	Resistance to solvents 2/ TM 2015 3(0)	Resistance to solvents 2/ TM 2015 3(0)		a. Physical dimensions 3/ TM 2016 2(0) b. Internal water vapor content TM 1018 3(0) 3/ 4/ 5/ (5,000 ppm maximum water content at 100°C.)
Subgroup 2 6/	a. Bond strength 7/ TM 2011 22(0) (1) Thermo compression - Test condition C or D (2) Ultrasonic - Test condition C or D (3) Beam lead – Test condition H b. Die shear test or substrate attach strength or stud pull test including passive elements TM 2019 or TM 2027 3(0) c. Flip chip pull off test TM 2031 or TM 2011 2(0) d. Flip chip die shear strength test or substrate attach strength test (test perform post underfill cure) TM 2019 or TM 2027 3(0)	a. Bond strength 7/ TM 2011 22(0) (1) Thermo compression - Test condition C or D (2) Ultrasonic - Test condition C or D (3) Beam lead – Test condition H b. Die shear test or substrate attach strength or stud pull test including passive elements TM 2019 or TM 2027 3(0) c. Flip chip pull off test TM 2031 or TM 2011 2(0) d. Flip chip die shear strength test or substrate attach strength test (test perform post underfill cure) TM 2019 or TM 2027 3(0)	a. Bond strength 7/ TM 2011 22(0) (1) Thermo compression - Test condition C or D (2) Ultrasonic Test condition C or D (3) Beam lead Test condition H b. Die shear test or substrate attach strength or stud pull test including passive elements TM 2019 or TM 2027 3(0) c. Flip chip pull off test TM 2031 or TM 2011 2(0) d. Flip chip die shear strength test or substrate attach strength test (test perform post underfill cure) TM 2019 or TM 2027 3(0)	a. Resistance to solvents 2/ TM 2015 3(0)	a. Resistance to solvents 2/ TM 2015 3(0) b. Internal visual and mechanical TM 2013, TM 2014 2(0) c. Bond strength 7/ TM 2011 22(0) (1) Thermo compression - Test condition C or D (2) Ultrasonic - Test condition C or D (3) Beam lead - Test condition H d. Die shear test or substrate attach strength or stud pull test including passive elements TM 2019 or TM 2027 3(0) e. Flip chip pull off test TM 2031 or TM 2011 2(0) f. Flip chip die shear strength test or substrate attach strength test (test perform post underfill cure) TM 2019 or TM 2027 3(0)

TABLE II. Group B tests (Mechanical and environmental test). – Continued.

Subgroups 1/	Group B tests for QML microcircuits (MIL-PRF-38535)			Group B tests for class level B and S microcircuits (TM 5005 of MIL-STD-883)	
	Class Q	Class V	Class Y	Class level B	Class level S
Subgroup 3 sample size 22(0) (22 leads from 3 devices) 8/	Solderability TM 2003 solder temperature +245°C ±5°C	Solderability TM 2003 solder temperature +245°C ±5°C	Solderability TM 2003 solder temperature +245°C ±5°C	Solderability TM 2003 solder temperature +245°C ±5°C	Solderability TM 2003 solder temperature +245°C ±5°C
Subgroup 4 sample size 45(0) 3/		For BGA/CGA packages: (i) Ball shear test for BGA package - JESD22-B117 (45 balls from 2 devices minimum) (ii) Solder column pull test for CGA package – TM 2038 (45 columns from 2 devices minimum)	For BGA/CGA packages: (i) Ball shear test for BGA package - JESD22-B117 (45 balls from 2 devices minimum) (ii) Solder column pull test for CGA package - TM 2038 (45 columns from 2 devices minimum)		a. Lead integrity TM 2004 9/ (Test condition B2, lead fatigue) b. Seal test TM 1014 as applicable (1) Fine leak (2) Gross leak c. Lid torque TM 2024 10/ as applicable d. For BGA/CGA packages: (i) Ball shear test for BGA package - JESD22-B117 (45 balls from 2 devices minimum) (ii) Solder column pull test for CGA package – TM 2038 (45 columns from 2 devices minimum)

TABLE II. Group B tests (Mechanical and environmental test). – Continued.

Subgroups 1/	Group B tests for QML microcircuits (MIL-PRF-38535)			Group B tests for class level B and S microcircuits (TM 5005 of MIL-STD-883)	
	Class Q	Class V	Class Y	Class level B	Class level S
Subgroup 5				a. Bond strength TM 2011 15(0) 11/ (1) Thermo compression - Test condition C or D (2) Ultrasonic - condition C or D (4) Beam lead - condition H b. Die shear test or substrate attach strength or stud pull test including passive elements TM 2019 or TM 2027 3(0) c. Flip chip pull off test TM 2031 or TM 2011 2(0) d. Flip chip die shear strength test or substrate attach strength test (test perform post underfill cure) TM 2019 or TM 2027 3(0)	sample size 45(0) a. End-point electrical parameters 12/ - As specified in the applicable device specification b. Steady state life test 13/TM 1005 Test condition C, D or E c. End-point electrical parameters 12/ - As specified in the applicable device specification
Subgroup 6 Sample size 15(0) 14/					a. Temperature cycling TM 1010, condition C, 100 cycles minimum b. Constant acceleration TM 2001, condition E, Y_1 orientation only c. Seal test TM 1014 (1) Fine leak (2) Gross leak d. End-point electrical parameters - As specified in the applicable device specification.

Note: The screening and QCI/TCI tables from MIL-PRF-38535 and MIL-STD-883 Test Methods 5004 and 5005 have been combined for consistency. MIL-PRF-38535 shall reflect this change as well. Manufacturers shall document in their QM plan the screening and QCI/TCI requirements to either MIL-PRF-38535 or MIL-STD-883.

TABLE II. Group B tests (Mechanical and environmental test). – Continued.

1/ Electrical reject devices from the same inspection lot may be used for all subgroups when end-point measurements are not required provided that the rejects are processed identically to the inspection lot through pre burn-in electrical and provided the rejects are exposed to the full temperature/ time exposure of burn-in. Group B test shall be performed on each inspection lot as a condition for lot acceptance for delivery. Group B test shall be performed on each qualified package type and lead finish.

2/ Resistance to solvents testing required only on devices using inks or paints as a marking medium. For devices with solder terminations, Resistance to solvents test shall be performed with balls/columns.

3/ Not required for qualification or quality conformance inspections where group D inspection is being performed on samples from the same inspection lot. For devices with solder terminations, Physical dimension test shall be performed with balls/columns.

4/ This test is required only, if it is a glass-frit-sealed package. Unless handling precautions for beryllia packages are available and followed TM 1018, procedure 3 shall be used (see group D, subgroup 6 of Table V). For class Y non-hermetic microcircuits devices internal water vapor content test is not applicable.

5/ Test three devices; if one fail, test two additional devices with no failures. At the manufacturer's option, if the initial test sample (e.g., 3 or 5 devices) fails, a second complete sample may be tested at an alternate laboratory that has been granted current suitability status by the qualifying activity. If this sample passes, the lot shall be accepted provided the devices and data from both submissions is submitted to the qualifying activity along with five additional devices from the same lot. If sample size (accept number) of 5(1) is used to pass the lot, the manufacturer shall evaluate their product to determine the reason for the failure and whether the lot is at risk.

6/ For all devices, except flip chip, the die shear test or substrate attach strength or stud pull test including passive elements shall be performed per TM 2019 or TM 2027, as applicable. For flip chip devices, flip chip pull off test shall be performed per TM 2031 or TM 2011. Flip chip die shear test or substrate attach strength test shall be performed after underfill is cured per TM 2019 or TM 2027. If the flip chip device uses passive elements the substrate attach strength or stud pull test shall also be performed per TM 2019 or TM 2027. For solder termination devices, subgroup 2 test may be performed without balls and columns attached.

7/ Unless otherwise specified, the sample size number for condition C or D is the number of bond pulls selected from a minimum number of 4 devices, and for condition H is the number of dice (not bonds) (see TM 2011).

8/ All devices submitted for solderability test shall be in the lead finish that will be on the shipped product and which has been through the temperature/time exposure of burn-in except for devices which have been hot solder dipped or undergone tin-lead fusing after burn-in. The sample size number applies to the number of leads inspected except in no case shall less than 3 (three) devices be used to provide the number of leads required. For BGA/CGA packages, solderability test shall be verified after solder ball or solder column attachment processes per TM 2003. For CGA packages, solder temperature shall be maintained in accordance with table 1 of TM 2003.

9/ The sample size number of 45 for lead integrity shall be based on the number of leads or terminals tested and shall be taken from a minimum of 3 devices. All devices required for the lead integrity test shall pass the seal test and lid torque test, if applicable, (see 10/) in order to meet the requirements of subgroup 4. For pin grid array leads and rigid leads, use TM 2028. For leaded chip carrier packages, use condition B1. For leadless chip carrier packages only, use test condition D and a sample size number of 15 based on the number of pads tested taken from 3 devices minimum. Seal test (subgroup 4b) need to be performed only on packages having leads exiting through a glass seal. For LGA/BGA/CGA packages, TM 2004 does not apply.

10/ Lid torque test shall apply only to packages which use a glass-frit-seal to lead frame, lead or package body (e.g., wherever frit seal establishes hermeticity or package integrity). Device packages with lid/heat sink attached on the back side of a flip chip die require a lid shear or lid torque test. Manufacturers shall submit test procedures for lid shear test for approval of QA. Lid torque test shall be performed in accordance with TM 2024.

11/ Test samples for bond strength may, at the manufacturer's option, unless otherwise specified, be randomly selected prior to or following internal visual (PRESEAL) inspection specified in Table IA of MIL-PRF-38535 or TM 5004, prior to sealing provided all other specifications requirements are satisfied (e.g., bond strength requirements shall apply to each inspection lot, bond strength samples shall be counted even if the bond would have failed internal visual exam). Unless otherwise specified, the sample size number for condition C or D is the number of bond pulls selected from a minimum number of 4 devices, and for condition F or H is the number of dice (not bonds) (see TM 2011).

12/ Read and record group A subgroups 1, 2 and 3.

13/ The alternate removal-of-bias provisions of 3.3.1 of TM 1005 shall not apply for test temperature above 125°C.

14/ For devices with solder terminations, Temperature cycling and Constant acceleration test may be performed without balls/columns attachment.

TABLE III. Group C life tests.

Subgroup	Tests	MIL-STD-883 test method and conditions Minimum sample size quantity (accept no.)		
		Class Q (class level B) 1/	Class V (class level S) 1/ 2/	Class Y (class level S) 1/ 2/
Subgroup 1	a. Steady-state life test	a. TM 1005 45(0) 1000 hours at 125°C	a. TM 1005 45(0) 1000 hours at 125°C	a. TM 1005 45(0) 1000 hours at 125°C
	b. End-point electrical parameters	b. As specified in the applicable device procurement specification	b. As specified in the applicable device procurement specification	b. As specified in the applicable device procurement specification

1/ Life test may be performed on a quantity (accept) criteria of 22(0) for 2000 hours at 125°C or equivalent per TM 1005 to attain 44,000 device hours. For lots greater than 200, actual devices shall be used. For lots less than or equal to 200, the number of actual devices shall be the greater of 5 devices or 10 percent of the lot, and the SEC shall supplement actual devices to result in a sample of 22 unless acceptable group C data from the same lot of SEC is available for the previous 3 months. The SEC shall have been produced under equivalent conditions as the production lot and as close in time as feasible, but not to exceed a 3-months period.

2/ Group C life tests shall be performed on the initial production lot of actual devices from each wafer lot, in accordance with Table IV herein. Group C life tests are not required to be performed on subsequent production lots when all the following conditions are met:

(a) Subsequent production lots utilize die from the same wafer lot as the initial production lot.

(b) Wafers or die remaining from the initial production lot are to be stored in dry nitrogen or equivalent controlled storage, and in covered containers.

(c) No major changes to the assembly processes have occurred since the group C test was performed on the wafer lot.

Note: For ASICs, a sample size of 5 actual devices may be used with the balance being made up of the SEC.

TABLE IV. Group D tests (Package related test).

Subgroups test	Tests 1/	MIL-STD-883 test method and conditions		
		Class Q (class level B)	Class V (class level S)	Class Y (class level S)
Subgroup 1 sample size 15(0) 2/	Physical dimensions	TM 2016	TM 2016	TM 2016
Subgroup 2 sample size 45(0) 2/ 3/	a. Lead/terminal integrity test	Where applicable a. TM 2004 condition B2 (lead fatigue) or applicable for the package technology style	Where applicable a. TM 2004 condition B2 (lead fatigue) or applicable for the package technology style	Where applicable a. TM 2004 condition B2 (lead fatigue) or applicable for the package technology style
	b. Seal test 4/ (1) Fine leak (2) Gross leak	b. TM 1014 Test condition as applicable	b. TM 1014 Test condition as applicable	b. 5/
	c. For BGA/CGA packages	c. BGA/CGA packages	c. BGA/CGA packages	c. BGA/CGA packages
	(i) Ball shear test for BGA package	(i) For BGA package - JESD22-B117 (45 balls from 2 devices minimum)	(i) For BGA package - JESD22-B117 (45 balls from 2 devices minimum)	(i) For BGA package - JESD22-B117 (45 balls from 2 devices minimum)
	(ii) Solder column pull test for CGA package	(ii) For CGA package - TM 2038 (45 columns from 2 devices minimum)	(ii) For CGA package - TM 2038 (45 columns from 2 devices minimum)	(ii) For CGA package - TM 2038 (45 columns from 2 devices minimum)
Subgroup 3 sample size 15(0) 6/ 7/	a. Thermal shock	a. TM 1011 Test condition B, 15 cycles minimum	a. TM 1011 Test condition B, 15 cycles minimum	a. TM 1011 Test condition B, 15 cycles minimum
	b. Temperature cycling	b. TM 1010 Test condition C, 100 cycles minimum	b. TM 1010 Test condition C, 100 cycles minimum	b. TM 1010 Test condition C, 100 cycles minimum
	c. Moisture resistance	c. TM 1004 8/	c. TM 1004 8/	c. HAST in accordance with JESD22-A118, condition B
	d. Visual examination	d. In accordance with visual criteria of TM 1004 or TM 1010	d. In accordance with visual criteria of TM 1004 or TM 1010	d. In accordance with visual criteria of TM 1004 or TM 1010
	e. Seal test 9/ (1) Fine leak (2) Gross leak	e. TM 1014 test condition as applicable	e. TM 1014 test condition as applicable	e. 5/
	f. End-point electrical parameters 10/	f. As specified in the applicable device	f. As specified in the applicable device	f. As specified in the applicable device

TABLE IV. Group D tests (Package related test). - Continued.

Subgroups	Test 1/	MIL-STD-883 test method and conditions		
		Class Q (class level B)	Class V (class level S)	Class Y (class level S)
Subgroup 4 sample size 15(0) 6/ 7/	a. Mechanical shock	a. TM 2002 condition B minimum	a. TM 2002 condition B minimum	a.TM 2002 condition B minimum
	b. Vibration, variable frequency	b. TM 2007 condition A minimum	b. TM 2007 condition A minimum	b.TM 2007 condition A minimum
	c. Constant acceleration 11/	c. TM 2001 Test condition E, Y1 orientation only	c. TM 2001 Test condition E, Y1 orientation only	c.TM 2001 Test condition E, Y1 orientation only
	d. Seal test (1) Fine leak (2) Gross leak	d. TM 1014 condition as applicable	d. TM 1014 condition as applicable	d. 5/
	e. Visual examination	e. In accordance with visual criteria of TM 2007	e. In accordance with visual criteria of TM 2007	e. In accordance with visual criteria of TM 2007
	f. End-point electrical parameters	f. As specified in the applicable device specification	f. As specified in the applicable device specification	f. As specified in the applicable device specification
Subgroup 5 sample size 15(0) 2/	a. Salt atmosphere	a. TM 1009 Test condition A minimum	a. TM 1009 Test condition A minimum	a. TM 1009 Test condition A minimum
	b. Visual examination	b. In accordance with visual criteria of TM 1009	b. In accordance with visual criteria of TM 1009	b. In accordance with visual criteria of TM 1009
	c. Seal 9/ (1) Fine leak (2) Gross leak	c. TM 1014 condition as applicable	c. TM 1014 condition as applicable	c. 5/
Subgroup 6 2/ 12/	Internal water vapor test (cavity packages)	TM 1018 3(0) 5,000 ppm maximum water content at 100°C	TM 1018 3(0) 5,000 ppm maximum water content at 100°C	5/
Subgroup 7 sample size 15(0) 2/ 13/ 14/	Adhesion of lead finish	Where applicable TM 2025	Where applicable TM 2025	Where applicable TM 2025

TABLE IV. Group D tests (Package related test). - Continued.

Subgroups	Test 1/	MIL-STD-883 test method and conditions		
		Class Q (class level B)	Class V (class level S)	Class Y (class level S)
Subgroup 8 sample size 5(0) 2/	Lid torque 15/	Where applicable TM 2024	Where applicable TM 2024	Where applicable TM 2024
Subgroup 9 sample size 3(0) (3 leads minimum) 16/	a. Soldering heat b. Seal (1) Fine leak (2) Gross leak c. External Visual examination d. End-point electrical	Where applicable a. TM 2036 b. TM 1014 condition as applicable c. TM 2009 d. As specified in the applicable device specification	Where applicable a. TM 2036 b. TM 1014 condition as applicable c. TM 2009 d. As specified in the applicable device specification	Where applicable a. TM 2036 b. 5/ c. TM 2009 d. As specified in the applicable device specification

Note: The screening and QCI/TCI tables from MIL-PRF-38535 and MIL-STD-883 Test Methods 5004 and 5005 have been combined for consistency. MIL-PRF-38535 shall reflect this change as well. Manufacturers shall document in their QM plan the screening and QCI/TCI requirements to either MIL-PRF-38535 or MIL-STD-883.

1/ In-line monitor data may be substituted for subgroups D1, D2, D6, D7, and D8 upon approval by the qualifying activity. The monitors shall be performed by package type and to the specified subgroup test method(s). The monitor sample shall be taken at a point where no further parameter change occurs, using a sample size and frequency of equal or greater severity than specified in the particular subgroup. The in-line monitor data shall be traceable back to the specific inspection lot(s) represented (accepted or rejected) by the data.

2/ Electrical reject devices from that same inspection lot may be used for samples. For devices with solder terminations, subgroups 1, 2, 5 and 8 tests shall be performed with balls and columns.

3/ The sample size number of 45, C = 0 for lead integrity shall be based on the number of leads or terminals tested and shall be taken from a minimum of 3 devices. All devices required for the lead integrity test shall pass the seal test if applicable (see 4/) in order to meet the requirements of subgroup 2. For leaded chip carrier packages, use condition B1. For pin grid array leads and rigid leads, use TM 2028. For leadless chip carrier packages only, use test condition D and a sample size number of 15 (C = 0) based on the number of pads tested taken from 3 devices minimum. For LGA/BGA/CGA packages, TM 2004 does not apply.

4/ Seal test (subgroup 2b) need be performed only on packages having leads exiting through a glass seal.

5/ This test is not applicable for class Y non-hermetic microcircuits devices.

6/ Devices used in subgroup 3, "Thermal and Moisture Resistance" may be used in subgroup 4, "Mechanical".

TABLE IV. Group D tests (Package related test). - Continued.

7/ For devices with solder terminations, subgroups 3 and 4 tests may be performed without balls and columns.

8/ Lead bend stress initial conditioning is not required for leadless chip carrier packages or BGA/CGA packages. For fine pitch packages (≤ 25 mil pitch) using a nonconductive tie bar, preconditioning shall be required on 3 devices only prior to the moisture resistance test with no subsequent electrical test required on these 3 devices. The remaining 12 devices from the sample of 15 devices do not require preconditioning but shall be subjected to the required endpoint electrical tests.

9/ After completion of the required visual examinations and prior to submittal to TM 1014 seal tests, the devices may have the corrosion by-products removed by using a bristle brush.

10/ At the manufacturer's option, end-point electrical parameters may be performed after moisture resistance and prior to seal test.

11/ For flip chip packages Constant acceleration test is not required.

12/ Test three devices; if one fails, test two additional devices with no failures. At the manufacturer's option, if the initial test sample (e.g., 3 or 5 devices) fails a second complete sample may be tested at an alternate laboratory that has been issued suitability by the qualifying activity. If this sample passes the lot shall be accepted provided the devices and data from both submissions is submitted to the qualifying activity along with 5 additional devices from the same lot. If sample size (accept number) of 5(1) is used to pass the lot, the manufacturer shall evaluate his product to determine the reason for the failure and whether the lot is at risk.

13/ The adhesion of lead finish test shall not apply for leadless chip carrier, land grid array (LGA), ball grid array (BGA), and column grid array (CGA) packages.

14/ Sample size number 15 leads from 3 devices minimum are based on number of leads with zero failure.

15/ Lid torque test shall apply only to packages which use a glass-frit-seal to lead frame, lead or package body (e.g., wherever frit seal establishes hermeticity or package integrity). Device packages with lid/heat sink attached on the back side of a flip chip die require a lid shear or lid torque test. Manufacturers shall submit test procedures for lid shear test for approval of QA. Lid torque test shall be performed in accordance with TM 2024.

16/ This test is performed at qualification/re-qualification of design changes which may affect this test. The manufacturer shall determine, for each package, the applicable conditions from TM 2036 that are appropriate for the mounting conditions, and assure by testing, or through their assembly processes, that the part is subjected to an equivalent time/temperature stress.

TABLE V. Group E (RHA) TCI/QCI test for class Q, class V and class Y.

Subgroups	Tests 1/ 2/	MIL-STD-883 test method and conditions Minimum sample size quantity (accept no.)		
		Class Q (class level B)	Class V (class level S)	Class Y (class level S)
Subgroup 1 3/ 4/	Neutron irradiation test (Displacement Damage test)			
	a. Qualification test	a.TM 1017 at 25°C 2(0) devices/wafer or 5(0) devices/wafer lot or 11(0) devices/inspection lot 5/	a.TM 1017 at 25°C 2(0) devices/wafer or 11(0) devices/wafer lot 6/	a.TM 1017 at 25°C 2(0) devices/wafer or 11(0) devices/wafer lot 6/
	b. QCI/TCI test	b. TM 1017 at 25°C 2(0) devices/wafer or 5(0) devices/wafer lot or 11(0) devices/inspection lot 5/	b. TM 1017 at 25°C 2(0) devices/wafer or 11(0) devices/wafer lot 6/	b. TM 1017 at 25°C 2(0) devices/wafer or 11(0) devices/wafer lot 6/
	c. Endpoint electrical parameters test	c. As specified in accordance with device specification	c. As specified in accordance with device specification	c. As specified in accordance with device specification
Subgroup 2 3/ 7/ 9/ 10/	Total ionization dose (TID)			
	a. Qualification test	a. TM 1019 at 25°C maximum supply voltage 2(0) devices/wafer or 5(0) devices/wafer lot or 22(0) devices/inspection lot 8/	a.TM 1019 at 25°C maximum supply voltage 2(0) devices/wafer or 22(0) devices/wafer lot or 1(0) devices/wafer + 4(0) SEC or test structures/ wafer or 5(0)devices/wafer lot + 4(0) SEC or test structures/ wafer	a.TM 1019 at 25°C maximum supply voltage 2(0) devices/wafer or 22(0) devices/wafer lot or 1(0) devices/wafer + 4(0) SEC or test structures/ wafer or 5(0)devices/wafer lot + 4(0) SEC or test structures/ wafer
	b. QCI/TCI test	b. TM 1019 at 25°C maximum supply voltage 2(0) devices/wafer or 5(0) devices/wafer lot or 22(0) devices/inspection lot 8/	b.TM 1019 at 25°C maximum supply voltage 2(0) devices/wafer or 22(0) devices/wafer lot or 1(0) devices/wafer + 4(0) SEC or test structures/ wafer or 5(0)devices/wafer lot + 4(0) SEC or test structures/ wafer	b.TM 1019 at 25°C maximum supply voltage 2(0) devices/wafer or 22(0) devices/wafer lot or 1(0) devices/wafer + 4(0) SEC or test structures/ wafer or 5(0)devices/wafer lot + 4(0) SEC or test structures/ wafer
	c. Endpoint electrical parameters test	c. As specified in accordance with device specification	c. As specified in accordance with device specification	c. As specified in accordance with device specification

TABLE V. Group E (RHA) TCI/QCI test for class Q, class V and class Y. – continued.

Subgroups	Tests 1/ 2/	MIL-STD-883 test method and conditions Minimum sample size quantity (accept no.)		
		Class Q (class level B)	Class V (class level S)	Class Y (class level S)
Subgroup 3 11/	a. Dose rate upset test (Transient irradiation test	a. For Digital TM 1021 For Linear TM1023 (temperature at 25°C) 2(0) devices/wafer or 11(0)devices/inspection lot 5/	a. For Digital TM1021 For Linear TM1023 (temperature at 25°C) 2(0) devices/wafer or 11(0) devices/wafer lot 6/	a. For Digital TM1021 For Linear TM1023 (temperature at 25°C) 2(0) devices/wafer or 11(0) devices/wafer lot 6/
	b. End point electrical parameters test	b. As specified in accordance with device specification	b. As specified in accordance with device specification	b. As specified in accordance with device specification
Subgroup 4 12/	Radiation dose rate induced latch-up test	TM 1020 As specified in the device specification	TM 1020 As specified in the device specification	TM 1020 As specified in the device specification
Subgroup 5 13/	Single event effects (SEE) test		ASTM F-1192 or JESD57 4(0) devices or As specified in the device specification	ASTM F-1192 or JESD57 4(0) devices or As specified in the device specification

Note: The screening and QCI/TCI tables from MIL-PRF-38535 and MIL-STD-883 Test Methods 5004 and 5005 have been combined for consistency. MIL-PRF-38535 shall reflect this change as well. Manufacturers shall document in their QM plan the screening and QCI/TCI requirements to either MIL-PRF-38535 or MIL-STD-883.

1/ Group E tests may be performed prior to device screening. Parts used for one subgroup test may not be used for other subgroups but may be used for higher levels in the same subgroup. End point electrical parameters as specified in accordance with device specification.

2/ For devices with solder terminations, group E subgroups test may be performed without balls and columns.

3/ The radiation hardness assurance capability level (RHACL)/radiation assurance in the SPEC level is the ratio of the capability level to the specification level of devices fluence. Subgroups shall be invoked when the radiation hardness assurance capability level (RHACL) specification requirements of > 10 are not met. For an example, if RHACL/SPEC ratio is > 10 then this test may not be required, but if the RHACL/SPEC ratio falls within > 1 and ≤ 10 then the subgroup test is required.

4/ This test is to be conducted only when specified in the purchase order or contract. Neutron irradiation test (Displacement damage test) is not required for MOS devices unless bipolar elements are included by design.

TABLE V. Group E (RHA) TCI/QCI test for class Q, class V and class Y. – continued.

5/ In accordance with inspection lot. If one part fails, seven additional parts may be added to the test sample with no additional failures allowed, 18(1).

6/ In accordance with wafer lot. If one part fails, seven additional parts may be added to the test sample with no additional failures allowed, 18(1).

7/ Parts used for one subgroup test may not be used for other subgroups, but may be used for higher levels in the same subgroup. For subgroup 2, total dose exposure shall not be considered cumulative unless testing is performed within the time limits of the test method.

8/ In accordance with inspection lot. If one part fails, 16 additional parts may be added to the test sample with no additional failures allowed, 38(1).

9/ Traceability to the specific wafer is required.

10/ In accordance with wafer for device types with greater than or equal to 4,000 equivalent transistors/chip selected from the wafer. The manufacturer shall define and document sampling procedures. The test structures shall be randomly selected from the wafer. An X-ray source may be used on test structures at the wafer level provided correlation has been established between the X-ray and the Cobalt-60 source and shall be documented in the QM plan.

11/ Radiation dose rate upset (Transient irradiation test) test shall be conducted during qualification on first QCI when specified in purchase order or contract.

12/ Radiation dose rate induced latch-up screen test shall be conducted when specified in purchase order or contract. Dose rate induced latch-up screen test is not required when radiation induced latch-up is verified to be not possible such as SOI, SOS and dielectrically isolated technology devices. If radiation dose rate induced latch-up screen test is required, shall be performed screening operation after seal. Test conditions, temperature, and the electrical parameters to be measured pre, post, and during the test in accordance with the specified device specification. The PDA for each inspection lot for class V or class Y (class level S) devices sublot, screened, shall be 5 percent or one device, whichever is greater.

13/ When single event effects (SEE) testing is specified in the purchase order or contract, the SEE test shall be performed during initial qualification and after any design or process change that may affect SEE response. Destructive SEE (SEB and SEGR) testing shall be performed accordance with JEDEC standard JESD57.

3.5.2 Alternate group B inspection for class level B. At the manufacturer's option, (class level B only), group B inspection shall be performed on any inspection lot of each qualified package type and lead finish from each different week of sealing. Different inspection lots may be used for each subgroup. After this alternate group B inspection is successfully completed, all other device types manufactured on the same assembly line using the same package type and lead finish sealed in the same week may be accepted without further group B testing. A manufacturer shall not accept inspection lots containing devices of a particular package type and lead finish until after the successful completion of group B testing for that package type and lead finish for each week of seal.

3.5.2.1 Nonconformance for the alternate group B inspection. When a failure has occurred in group B using the alternate group B procedure, samples from three additional inspection lots of the same package type, lead finish, and week of seal as the failed package shall be tested to the failed subgroup(s). If all three inspection lots pass, then all devices manufactured on the same assembly line using the same package type and lead finish and sealed in the same week may be accepted for group B inspection. If one or more of the three additional inspection lot fail, then no inspection lot containing devices manufactured on the same assembly line using the same package type and lead finish sealed in the same week shall be accepted for group B inspection until each inspection lot has been subjected to and passed the failed subgroup(s).

3.5.3 Group E samples. At the manufacturer's option (but subject to the criteria defined by 3.5.3.1, 3.5.3.2, and 3.5.3.3), group E samples need not be subjected to all the screening tests of method 5004, but shall be assembled in a group D qualified package and, as a minimum, pass group A, subgroups 1 and 7, electrical tests at 25°C prior to irradiation.

3.5.3.1 Group E tests shall be performed on samples that have been exposed to burn-in, or

3.5.3.2 As an alternative, the requirement of 3.5.3.1 can be waived if previous testing has shown that burn-in produces negligible changes in the device total dose response, or

3.5.3.3 As an alternative, the Group E tests can be performed on samples which have not received burn-in if the results of the Group E tests are corrected for the changes in total dose response which would have been caused by burn-in. This correction shall be carried out in a manner acceptable to the parties to the test.

3.6 Disposition of samples. Disposition of sample devices used in groups A, B, C, D, and E testing shall be in accordance with the applicable device specification.

3.7 Substitution of test methods and sequence.

3.7.1 Accelerated qualification or quality conformance testing for class level B. When the accelerated temperature/time test conditions of condition F of method 1005 are used for any operating life or steady state reverse bias subgroups on a given sample for purposes of qualification or quality conformance inspection, the accelerated temperature/time test conditions shall be used for all of those named subgroups. When these accelerated test conditions are used for burn-in screening test (test condition F of method 1015) or stabilization bake (any test temperature above the specified maximum rated junction temperature for devices with aluminum/ gold metallurgical systems) for any inspection lot, it shall be mandatory that they also be used for the operating life, and steady-state reverse bias tests of method 5005, as applicable, or qualification or quality conformance inspection. Qualification and quality conformance inspection may be performed using accelerated conditions on inspection lots that have been screened using normal test conditions.

3.8 Data reporting. When required by the applicable acquisition document, the following data shall be made available for each lot submitted for qualification or quality conformance inspection:

a. Results of each subgroup test conducted, initial, and any resubmission.

b. Number of devices rejected.

c. Failure mode of each rejected device and, for class S, the associated mechanism for catastrophic failures of each rejected device.

d. Number of additional samples added, when applicable.

e. Resubmitted lots, identification and history.

f. Read and record variables data on all specified electrical parameter measurements in group B.

4. SUMMARY. The following details shall be specified in the applicable device specification:

   a. Device class and procedure paragraph if other than 3.

   b. Sequence of test, sample size, test method, and test condition where not specified, or if other than specified.

   c. Test condition, cycles, temperatures, axis, etc., where not specified, or if other than specified (see 3).

   d. Acceptance procedure (see 3.3) and quantity (accept number) or sample size number and acceptance number, if other than specified (see 3).

   e. Electrical parameters for group A.

   f. Electrical parameters for groups B, C, D, and E end point measurements, where applicable.

   g. Requirements for failure analysis (see 3.8).

   h. Requirements for data recording and reporting if other than specified in 3.8.

   i. Restriction on resubmission of failed lots (see 3.4), where applicable.

   j. Steady-state life test circuits, where not specified or if other than specified (see subgroup 1 of Table III and subgroup 5 of Table II (Class S).

   k. Parameters on which delta measurements are required.

METHOD 5006

LIMIT TESTING

1. PURPOSE. This method provides means for establishing or evaluating the maximum capabilities of microelectronic devices, including such capabilities as absolute maximum ratings (from which safe design limits may be derived), maximum stresses which may be applied in screening or testing without causing degradation, and sensitivity to particular screening or testing without causing degradation, and sensitivity to particular screening or testing stresses and the associated modes or mechanisms of failure. Since this is a relatively expensive and time consuming procedure, it is not intended for general application to all device acquisitions. It should however be extremely useful in evaluating the capabilities of new device types or devices which have experienced significant modifications in design, materials or processes which might be expected to alter their stress tolerance or primary modes and mechanisms of failure. It should also be useful in providing information vital to quality and reliability assurance in high reliability programs or in acquisition extending over significant periods of time where test results can be used to provide corrective action in device design, processing or testing.

1.1 Destructive testing. All limit testing accomplished in accordance with this method is considered destructive and devices shall be removed from their respective lot.

1.2 Parameter measurements. Electrical measurement shall be performed to remove defective devices after each stress step unless otherwise specified herein or in the applicable acquisition document. These measurements need not include all device parameters, but shall include sufficient measurements to detect all electrically defective devices. When delta parameter measurements are required they shall be specified in the applicable acquisition document.

2. APPARATUS. The apparatus for this test shall include equipment specified in the referenced test methods as applicable and electrical measurement equipment necessary to determine device performance.

3. PROCEDURE. Limit testing shall be conducted in accordance with the procedure contained in 3.1 and 3.2 using samples sizes as designated in table I.

TABLE I. Sample sizes for limit testing.

Limit test	Sample size
Thermal evaluation	5
Extended thermal shock	10
Step-stress mechanical shock	10
Step-stress constant acceleration	10
Step-stress operational life	10
Constant high stress operational life	10
Step-stress storage life	10
Total devices	65

3.1 Test condition A. Procedure for monolithic and multichip microcircuits. Limit testing shall be conducted as described in 3.1.1 through 3.1.7 in the sequence shown, unless otherwise specified (see 4.). Failure analysis of all devices failing limit tests shall be performed in accordance with method 5003, test condition B, unless otherwise specified in the applicable acquisition document. Limit testing may be discontinued prior to completing the test when 50 percent of the test sample has failed that specific test.

3.1.1 Thermal evaluation. This test shall be performed in accordance with method 1012, test condition B. With maximum power applied, the complete temperature gradient of the active chip area shall be recorded. This data shall be analyzed to determine that no areas of abnormally high operating temperatures are present as a result of improper design or processing. The thermal resistance at the maximum operating temperature of the device shall be determined using test condition C or method 1012.

3.1.2 Extended thermal shock. The purpose of this testing is to establish the resistance of the device to thermal fatigue effects. The device shall be subjected to a minimum of 100 cycles of thermal shock, in accordance with method 1011. This test shall be conducted in the following sequence:

Step	Cycles	Test condition
1	15	C
2	15	D
3	70	F

Parameter measurements (see 1.2) shall be made at the completion of 15, 30, 40, 70, and 100 cycles, and the number of failures after each of these cycles shall be recorded.

3.1.2.1 Temperature cycling. When specified in the applicable acquisition document, temperature cycling method 1010 may be substituted for the thermal shock test in 3.1.2. This test shall be conducted in the following sequence:

Step	Cycles	Test condition
1	20	B
2	20	C
3	20	D

Parameter measurements (see 1.2) shall be made at the completion of each step, and the number of failures for each of these steps shall be recorded.

3.1.3 Step-stress mechanical shock. The purpose of this test is to establish the mechanical integrity of the device. The device shall be subjected to mechanical shock in accordance with method 2002 and the following step-stress sequence:

Step	Test condition	Plane	No. of shocks
1	B	Y_1	5
2	C	Y_1	5
3	E	Y_1	5
4	F	Y_1	5
5	G	Y_1	5

Electrical parameter measurements (see 1.2) shall be made after each step, and the number of failures incurred at each step shall be recorded.

3.1.4 Step-stress constant acceleration. The purpose of this testing is to establish the mechanical integrity of the device. The device shall be subjected to a constant acceleration in accordance with method 2001 and the following step-stress sequence:

Step	Test condition	Plane
1	E	Y_2, X_1, Z_1, Y_1
2	F	Y_2, X_1, Z_1, Y_1
3	G	Y_2, X_1, Z_1, Y_1
4	H	Y_2, X_1, Z_1, Y_1

Electrical parameter measurements (see 1.2) shall be made after each plane, and the number of failures incurred shall be recorded.

3.1.5 Step-stress operational life. The purpose of this test is to establish the operational stress levels that will accelerate predominant failure mechanisms so that meaningful failures can be generated in a relatively short period of time. The results of the testing will also be utilized to evaluate the safety factors built into the device, to establish the safe constant operational stress conditions, and to improve through corrective action(s) the reliability of the device. Electrical parameter measurements shall be made after each stress level and the number of failures incurred in each step shall be recorded.

3.1.6 Constant high-stress operational life. The purpose of this test is to induce meaningful operational failures in a relatively short period of time and to compare the results of this testing with the results obtained from the step-stress operational life. The stress level to be applied and intervals to intermediate electrical measurements shall be determined on the basis of the results obtained in the step-stress tests (see 3.1.5). Electrical parameter measurements shall be made after each specified time interval and the number of failures shall be recorded.

3.1.7 Step-stress storage life. The purpose of this test is to establish the storage stress levels that will accelerate predominant failure mechanisms so that meaningful failures can be generated in a relatively short period of time. The storage temperatures and the step duration shall be established prior to initiation of testing. The results of the testing will be utilized to evaluate the maximum limits of device resistance to failure at high temperature. Electrical parameter measurements shall be made after each stress level and the number of failures incurred at each level shall be recorded.

3.2 Test condition B. Procedure for film and hybrid microcircuits. Limit test shall be conducted in accordance with table I and as described in 3.1.1 through 3.1.7 except that the specified test condition may be changed. When test condition or stress levels are changed, they shall be established prior to the initiation of test. Failure analysis of all devices failing limit tests shall be performed in accordance with method 5003, test condition B, unless otherwise specified in the applicable acquisition document. Unless otherwise specified in the applicable acquisition document, limit testing in any test may be discontinued after 50 percent of test sample has failed that specific test.

3.3 Test plan. When required by the applicable acquisition document, the specific procedures for conducting limit testing shall be submitted as a "Limit Test Plan" for approval by the acquiring activity prior to the initiation of testing. This plan shall include the following as a minimum:

a. Activity responsible for performing the test.

b. Device types to be subjected to limit testing and criteria for their selection.

c. Failure criteria including electrical parameters to be measured.

d. Testing schedule.

e. Description of testing equipment.

f. Test condition if other than specified.

g. Data recording and reporting formats.

h. Data analysis procedures.

4. SUMMARY. The following details shall be specified in the applicable acquisition document:

a. Test condition letter (see 3.1 and 3.2).

b. Test sequence and sample quantities if other than specified (see 3.1 and 3.2).

c. Failure analysis procedures and test condition, if other than specified (see 3.1 and 3.2).

d. For test condition B, the test conditions and stress levels, where applicable (see 3.2).

e. Percent failure for test termination, if other than specified (see 3.1 and 3.2).

f. Requirements for Limit Test Plan and data reporting (see 3.3).

METHOD 5007.8

WAFER LOT ACCEPTANCE

1. PURPOSE. This method establishes the requirements for the lot acceptance testing of microcircuit wafers intended for class level S use.

2. APPARATUS. The apparatus used shall be in accordance with the apparatus requirements of the methods specified in the conditions column of table I.

3. PROCEDURE. The performance of the wafer lot acceptance tests shall be in accordance with the conditions specified in table I. If a lot fails a test under the sampling plan, as an alternative to rejecting the entire lot, the manufacturer may elect to test each wafer in the lot for that parameter(s). All wafers successfully passing the test(s) shall be considered the lot for the remainder of the tests. All wafers failing any test shall be removed from the lot. Data obtained from all tests shall be recorded. The sequence of the tests in table I does not have to be adhered to, however, the tests must be performed at the point in the processing (if specified) required in the conditions column of table I. Where limits are based on tolerances about an "approved design nominal", the nominal shall be stated in the maintenance plan submitted for approval to the qualifying or acquiring activity. Where table I limits are based on tolerances about the "mean", the mean shall be determined initially on measurements from a minimum of five lots and the mean shall be stated in the maintenance plan submitted for approval to the qualifying or acquiring activity. In no case shall the "design nominal" or "mean" exceed the absolute limits specified in table I.

4. SUMMARY. The following detail shall be specified in the applicable device specification:

Requirements or limits if other than those on table I.

TABLE I. Wafer lot acceptance tests.

Test	Conditions 1/	Limits 3/	Sampling plan
1. Wafer thickness	Measurement shall be performed after final lap or polish. All readings shall be recorded. 2/	Maximum deviation of ±2 mil from approved design nominal 6 mil minimum.	Two wafers per lot. Reject lot if any measurement exceeds limits or revert to test of each wafer.
2. Metallization thickness	All readings shall be recorded. Sheet resistance measurements with a QA approved correlation curve to metallization thickness is an allowed alternate method of measurement.	The conductor metal shall be 8KA minimum, 5KA minimum for lower levels. The metallization thickness shall be adequate to satisfy the current density requirements of MIL-PRF-38535 with a minimum 20% additional margin. For technologies less than 500 nm, the minimum metallization thickness shall be as defined by the supplier. The supplier must still provide objective evidence to show compliance to current density/electromigration and all other design and reliability requirements of MIL-PRF-38535.	One wafer (or monitor) per lot. Reject lot if measurement exceeds limits or revert to test of each wafer.
3. Thermal stability (applicable to: All linear; all MOS; all bipolar digital operating at 10 V or more)	Record V_{FB} or V_T. May be replaced by an in-line monitor, with approval from the Qualifying Activity.	a. ΔV_{FB} or ΔV_T $\leq$0.75, normalized to an oxide thickness of 1000Å for bipolar digital devices operating at 10 volts or greater and all bipolar linear devices not containing MOS transistor(s). The monitor shall have an oxide and shall be metallized with the lot.	One wafer (or monitor) per lot. Reject lot if measurement exceeds limits or revert to test of each wafer.

See footnotes at end of table.

TABLE I. Wafer lot acceptance tests - Continued.

Test	Conditions 1/	Limits 3/	Sampling plan
3. Thermal stability (applicable to: All linear; all MOS; all bipolar digital operating at 10 V or more)	Record VFB or V_T.	b. ΔV_{FB} or Δ_{VT} $\leq$1.0 V,normalized to an oxide thickness of 1,000Å for bipolar linear devices that operate above 5 V and containing MOS transistor(s), and digital devices that operate above 10 V and containing MOS structures. The V_{FB} limit shall not be exceeded by the sum of the absolute values of the MOS oxide transistors and the metallization Δ. The monitor(s) shall be oxidized and metallized with the lot. Separate monitors may be used for this test. c. ΔV_{FB} or V_T $\leq$0.4 V, normalized to an oxide thickness of 1,000Å for MOS devices. A monitor consisting of a gate oxide metallized with the lot shall be used.	One wafer (or monitor) per lot. Reject lot if measurement exceeds limits or revert to test of each wafer.
4. SEM	MIL-STD-883, method 2018.	MIL-STD-883, method 2018.	MIL-STD-883, method 2018. Lot acceptance basis.
5. Glassivation thickness	All readings shall be recorded.	As specified in MIL-PRF-38535, Paragraph A.3.5.8.	One wafer (or monitor) per lot. Reject lot if any measurement exceeds limits or revert to test of each wafer.

See footnotes at end of table.

TABLE I. Wafer lot acceptance tests - Continued.

Test	Conditions 1/	Limits 3/	Sampling plan
6. Gold backing thickness (when applicable)	All readings shall be recorded. A sheet resistance measurement with a correlation curve to thickness is an allowed method of measurement.	In accordance with approved design nominal thickness and tolerance.	One wafer (or monitor) per lot. Reject lot if any measurement exceeds limits or revert to test of each wafer.

1/ The manufacturer shall have documented procedures for performing each required test. These procedures shall be made available to the qualifying activity or acquiring activity upon request.

2/ This test is not required when the finished wafer design thickness is greater than 10 mil.

3/ Approved design nominal values or tolerances shall be documented in the manufacturer's baseline documentation.

METHOD 5008.9

TEST PROCEDURES FOR HYBRID AND MULTICHIP MICROCIRCUITS

Method 5008 is canceled effective 1 June 1993. It is superseded by MIL-PRF-38534. For Federal Stock classes other than 5962, the following paragraphs of MIL-PRF-38534 are provided to replace method 5008.

Superseded method 5008	MIL-PRF-38534	Requirement
3.2 Element evaluation	C.3 Element evaluation	Element evaluation
3.3 Process control	C.4 Process control	Process control
3.4 Device screening	C.5 Device screening	Screening
3.5 Quality conformance evaluation	C.6 Conformance Inspection and Periodic Inspection	QCI

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METHOD 5009.1

DESTRUCTIVE PHYSICAL ANALYSIS

1. PURPOSE. The purpose of this test is to describe requirements for performance of destructive physical analysis (DPA) for the applicable device class, for sampling, preparation, procedures, accept/reject criteria, disposition of rejected lots and documentation. While this test method may be used by a microcircuit manufacturer, it is intended that these procedures be actually performed by the contractor, subcontractor, or independent testing lab.

1.1 Definitions.

a. Defects. Any nonconformance from specified requirements for form, fit, function, or workmanship.

b. Destructive physical analysis. The process of disassembling, testing, and inspecting a device for the purpose of determining conformance with applicable design and process requirements.

c. Lot related defect. A defect, attributable to a variance in design or the manufacturing, test or inspection process, that may be repetitive (e.g., mask defects, metallization thickness, bond strength insulation resistance and separation between metallization runs, wires or wires and die edge).

d. Screenable defects. A defect for which an effective nondestructive screening test or inspection is available or can be developed.

2. APPARATUS. The apparatus shall consist of suitable equipment to perform each specified DPA test.

3. PROCEDURE. The organization (contractor, subcontractor, or independent test lab) conducting the DPA test should contact the manufacturer of the product and supply a list of test methods that are to be used during the DPA test. The manufacturer can then advice the DPA test organization if there are any significant changes to those test methods that are allowed as modification options within MIL-STD-883, MIL-PRF-38535 or under the manufacturer's approved program plan.

3.1 Sample selection. A random sample shall be selected from the inspection lot in accordance with table I, unless otherwise specified.

TABLE I. Sample selection.

Monolithic microcircuits	Two devices or 1 percent of the inspection lot, whichever is greater, to a maximum of 5 total devices, unless otherwise specified, (see 3.1.1 and 4a).
Hybrid or multichip microcircuits	Two devices or 1 percent of the inspection lot, whichever is greater, to a maximum of 5 total devices, unless otherwise specified, (see 3.1.1 and 4a).

3.1.1 Combining sample. Where an inspection lot is comprised of more than one device type covered by a single device specification or drawing, the sample selected shall be proportionately divided from the device types in order to assure a representative sampling, and not less than one, of each device type in the DPA sample.

3.2 DPA report. A DPA report shall be prepared for each inspection lot tested and submitted to the acquiring or qualifying activity. The report shall consist of the following:

a. DPA summary sheet.

b. DPA checklist.

c. DPA test data sheet.

d. Photographs.

e. Other data or analysis supporting findings.

3.2.1 DPA checklist. A checklist shall be used to record all attribute data from the applicable test.

3.2.2 DPA test data sheet. A test data sheet shall be used to record the variable data from the applicable test and any electrical test specified.

NOTE: No provisions have been included herein for electrical testing since all devices shall have already passed the specified electrical tests; however, electrical tests may be required for follow-up analysis of a physical discrepancy.

3.2.3 DPA summary sheet. A summary sheet shall be used to summarize the DPA test results, analysis supporting findings, provide other essential data and indicate disposition of lot.

3.3 General requirements.

3.3.1 DPA evaluation. The results of all tests and examinations performed on DPA sample items shall be analyzed by qualified technical personnel to determine disposition and corrective action, as applicable, of the lot from which the samples were taken.

3.3.2 Photographs. Photographs shall be made at sufficient magnification and with enough views to clearly document significant details of the parts construction. When SEM or optical microscopes are used to evaluate a device, photographs shall be made to document discrepant or worst case features.

3.3.2.1 Photograph requirements. A minimum of two photographs will normally be required to document baseline characteristics of an opened part prior to performance of any destructive tests. These shall be supplemented with other photographs as required to record observed defects or anomalies. Microscopy techniques such as color, dark field, phase contrast, interference contrast, etc., shall be used as necessary to enhance image clarity. When SEM examination is performed the DPA report shall include, as a minimum, view(s) of significant features of the die, a photograph of the worst case oxide step and a photograph of the worst case metallization. Each photograph shall be labeled or otherwise identified with the DPA report number, and, if applicable, the part number, serial number, lot date code, and the magnification (and viewing angle for SEM photographs) used.

3.3.3 Retention of DPA reports. The original copy of all DPA reports shall be retained by the performing organization and a copy submitted to the acquiring or qualifying activity.

3.3.4 Sectioned samples. When performed techniques similar to those used to prepare sectioned metallurgical and mineralogical specimens for optical examination are generally applicable to the preparation of DPA samples. The device to be examined is first potted in a suitable plastic (or mounting by other suitable means). It is then cut or rough ground to the desired section plane. This is followed by fine grinding, polish and sometimes an etch to bring out the necessary detail. Care shall be taken to ensure that damage is not introduced during any of these operations (in particular, during potting cure, cutting, and rough grinding).

3.3.5 SEM samples. The microcircuits shall be prepared for SEM examination in accordance with method 2018 of MIL-STD-883, "Notes on SEM examination of Microelectronic Parts". Other types of parts shall be prepared for SEM by using standard laboratory techniques for mounting and coating, taking care that anomalies are not introduced by the coating.

3.3.6 Baseline design documentation. Each DPA procedure should be referenced to a baseline photograph, sketch, or drawing showing the general configurations of the device to be examined, which includes critical dimensions, location of constituent parts and details of any pertinent materials or processes. The baseline documentation shall be current so as to show any approved changes in the configuration.

3.4 Microcircuits (monolithic) procedure. The purpose is to verify external and internal physical configuration and that the devices were not damaged during sealing or any other processing step(s). To verify that the devices have met the requirements for radiography, seal, external visual, internal water vapor analysis, internal visual, baseline, bond strength, and contamination control.

3.4.1 External visual. Record identification marking. Examine parts, at 10X minimum magnification for configuration and defects in seal, plating, or glass feed through in accordance with method 2009 of MIL-STD-883.

3.4.2 Radiography. When specified, radiography shall be in accordance with MIL-STD-883, method 2012. Radiograph shall be required before delidding to examine cavity devices for loose particles, die attach, and to determine internal clearances. It is also useful as an aid in locating delidding and sectioning cuts and to nondestructively investigate suspected defects.

3.4.3 Seal. A fine and gross leak seal test shall be performed on all DPA samples in accordance with MIL-STD-883, method 1014. Record both fine and gross leak rates.

3.4.4 Internal water vapor analysis. When specified, internal water vapor analysis shall be performed in accordance with method 1018.

3.4.5 Internal visual. De-cap all samples using appropriate method (see 3.6) taking care not to introduce contamination during the de-cap process. Examine all devices in accordance with MIL-STD-883, method 2010, test condition A or B or appendix A of method 5004 (alternate 2) as applicable, and methods 2013 and 2014.

3.4.6 Baseline configuration. During external and internal visual all devices shall be evaluated for conformance with the baseline design documentation (see 3.3.6) and other specified requirements. Variance from requirements shall be reported as defects.

3.4.7 Bond strength. Perform bond strength tests in accordance with MIL-STD-883, method 2011, test condition D. Pull all wires on at least two devices. Record the force at which the wire breaks or bond lifts and the location of the break.

3.4.8 SEM. Prepare the samples for SEM evaluation and conduct this inspection in accordance with MIL-STD-883, method 2018. If any of the wire bonds lifted during the bond strength tests, these shall be included in the SEM inspection to determine the nature of the bond to chip interface at the point of rupture.

3.4.9 Die shear. Die shear tests shall be performed on at least two samples in accordance with MIL-STD-883, method 2019. Record the die force required to separate the die from substrate and the interface appearance in terms of areas affected in the break.

3.4.10 Evaluation criteria. The inspection lot shall be considered suspect if devices exhibit any defects when inspected or tested to the criteria listed below. Each defect shall be photographed (when applicable), measured, and described in the DPA report. In the absence of defects or based on a decision by the responsible parts authority that any observed anomalies do not constitute rejectable defects, the lot may be considered acceptable for use (see 3.7.1 for disposition of suspect lots).

INSPECTION REQUIREMENT	MIL-STD-883 EVALUATION CRITERIA
External visual	Method 2009
Radiography	Method 2012
Seal	Method 1014
Internal water vapor	Method 1018
Internal visual	Method 2010 test condition A or B or alternate 2 of Method 5004 as applicable, 2013 and 2014
Bond strength	Method 2011
SEM	Method 2018
Die shear	Method 2019
Configuration	Baseline design documentation

3.5 Microcircuits hybrid and multichip procedure. The purpose is to verify external and internal physical configuration. To verify that devices met the requirements for radiography, PIND, seal, external Visual, gas analysis, internal visual, baseline, bond strength, and contamination control. These devices are normally custom and will depend on contractor drawings, therefore, the DPA procedure for a hybrid or multichip microcircuit shall be tailored to evaluate the features specified and the overall configuration as defined by the applicable hybrid or multichip drawing.

3.5.1 External visual. Conduct external visual examination on all samples to determine conformance with MIL-STD-883, method 2009, and the applicable device specification.

3.5.2 Radiography. When specified, radiography shall be in accordance with MIL-STD-883, method 2012. Radiography shall be required before delidding to examine cavity devices for loose particles, die attach, improper interconnecting wires, and to determine internal clearances. It is also useful as an aid in locating delidding and sectioning cuts and to nondestructively investigate suspected defects.

3.5.3 Particle impact noise detection test (PIND). A PIND test shall be performed on all DPA samples in accordance with MIL-STD-883, method 2020, condition A or B.

3.5.4 Seal. A fine and gross leak seal test shall be performed on all DPA samples in accordance with MIL-STD-883, method 1014. Record both fine and gross leak rates.

3.5.5 Internal water vapor analysis. When specified, internal water vapor analysis shall be performed in accordance with method 1018.

3.5.6 Internal visual. De-cap all devices (see 3.6) and perform internal visual inspection in accordance with MIL-STD-883, method 2017, and the applicable device design data.

3.5.7 Baseline configuration. Evaluate configuration and workmanship of each sample for compliance with the requirements of the applicable device specifications and drawings or baseline design documentations (see 3.3.6). Report variances as defects.

3.5.8 Bond strength. Perform bond strength tests in accordance with MIL-STD-883, method 2011. Pull all wires on at least two devices. Record the force at which the wire breaks or bond lifts and location of the break.

3.5.9 SEM. Prepare the samples for SEM evaluation and conduct this inspection on the microcircuits and other expanded contact chips in accordance with MIL-STD-883, method 2018. If any of the wire bonds lifted during the bond strength test, these shall be included in the SEM inspection to determine the nature of the bond to chip interface at the point of rupture.

3.5.10 Die shear. Die shear tests shall be performed on at least two samples in accordance with MIL-STD-883, method 2019. Record the die force required to separate the die from substrate and the interface appearance in terms of area affected in the break. Test a representative sample of each chip type in each package under test. Samples of each other chip type such as resistors and capacitors shall also be tested for shear strength in accordance with the requirements of the applicable specification, and the force required to separate the active and passive components from the substrate shall be recorded.

3.5.11 Evaluation criteria. The lot shall be considered suspect if parts exhibit any defects when inspected or tested to the criteria listed below. Each defect shall be photographed, measured, and described in the DPA report. In the absence of defects or based on a decision by the responsible parts authority that any observed anomalies do not constitute rejectable defects, the lot may be considered acceptable for use (see 3.7.1 for disposition of suspect lots).

INSPECTION REQUIREMENT	MIL-STD-883 EVALUATION CRITERIA, Sample Size
External visual	Method 2009
Radiography	Method 2012
PIND	Method 2020
Seal	Method 1014
Internal water vapor	Method 1018
Internal visual	Methods 2017, 2010 test condition A or B or alternate 2 of Method 5004 as applicable; 2013 and 2014
Bond strength	Method 2011
SEM	Method 2018
Die shear	Method 2019
Configuration	Baseline design documentation

3.6 Delidding procedures. The devices shall be delidded using one of the procedures below or other suitable means. Caution should be exercised to preclude damage to the device or the generation of internal contamination as the result of delidding.

3.6.1 Solder seals. Do not reflow the solder. After these cans are opened, the interior shall be examined for excess solder or flux. Reflowing the solder seal will destroy the evidence. To open, grind can just above the header until it is thin enough to be cut with a sharp instrument.

3.6.2 TO-5 type enclosures. Semiconductors, microcircuits, and other devices are often packaged on TO-5 type enclosure that can be quickly opened using a commercial device known as a "Head Remover, Silicon" or, more commonly, as a TO-5 can opener. This device can be modified to accept various lid heights and a metal guide bar may be added over the cutting wheel to maintain minimum clearance between the TO-5 flange and the cutting wheel.

3.6.3 Flange welded enclosures. Grind off flange until can is thin enough to be cut with a sharp instrument.

3.6.4 Tubulated enclosures. Before opening, file or dry grind into the crimp to ensure that it has properly engaged the conductor. Note whether the number and placement of the crimps are normal and check for over crimping. Free the center conductor from the crimp before removing the device cover by using a can opener or grinder.

3.6.5 Solder sealed flat-pack or DIP. Hold the sample flat against a dry Buehler grinding wheel (180 grit paper) until the lid becomes thin enough to make the cavity indentation visible. Clean the sample, then puncture the lid with a sharp instrument and peel it off.

3.6.6 Ceramic flat-pack.

a. Preferred method. Pass an oxygen/butane flame over the lid of the sample while the part is under light pressure from the blades of a delidding vise. Each pass of the torch should last two or three seconds and the vise should be tightened slightly between passes. Two or four passes are normally required. The blades of the delidding vise should be positioned above the leads and not at the ends of the sample.

b. Alternate method. Hold the sample firmly by its lower body (this may require careful bending of the leads). Place the point of a sharp blade on the seal line above the lead frame and strike the blade lightly with a small hammer. Continue this process around the package circumference until the seal fractures to release the lid.

NOTE: The "flat-pack delidding vise" referred to in 3.6.6 is a special fixture which can be assembled or may be acquired from a commercial source.

3.6.7 Dual-in-line package.

a. Preferred method. This technique is suitable for all types of ceramic packages, including those types where the lid seal is formed at the lead frame interface. Position the package between the knife blades of a delidding vise contacting the seal region. The physical condition of the seal regions (i.e., the determination of the optimum package sides exhibiting the maximum seal glass dimensional length) to be clamped between the parallel cutters, will generally dictate the orientation. Apply sufficient pressure to just hold the package in place. Heat the package lid for approximately 5 seconds with a oxygen/butane microflame torch, remove the heat and slowly increase pressure on the package seal. Repeat the heat/pressure sequence until the entire lid, intact, is sheared off at the seal.

b. Alternate method. Place abrasive paper (e.g., Buehler emery paper or equivalent) on a flat surface. Abrade the package lid by repeated strokes across the paper. The sample may optionally be placed in a fixture containing a mounted dual-in-line socket for ease in handling. Continue abrading, with frequent visual checks, until the lid is almost completely gone. Remove the remainder of the lid over the cavity by attaching a piece of tape and lifting off.

3.7 Failure criteria. The inspection lot shall be considered suspect if the devices exhibit any defect when inspected or tested to the criteria in 3.4 or 3.5. Each defect shall be photographed, measured, and described in the DPA report.

3.7.1 Disposition of suspect lots. Inspection lots which are found to have one or more defects as the result of evaluation of a DPA sample shall be: a. subjected to resampling if the results of the first sample were inconclusive, b. screened, c. scrapped, or d. returned to supplier, as applicable.

3.7.2 Resampling. In the event that results of the initial DPA sample are inconclusive, a second DPA sample may be selected in accordance with 3.1 except that the sample size shall be determined by the cognizant authority for the parts and approved by the acquiring or qualifying activity on the basis of the type of defect that is being investigated and the number of devices remaining in the inspection lot. Final disposition shall be made of the inspection lot after completion of the evaluation of the second sample.

3.7.3 Rescreened lots. Inspection lots which are found to have parts with screenable defects may be subjected to 100 percent nondestructive screening tests to eliminate the nonconforming items. After completion of screening the remaining devices may be accepted for shipment.

3.7.4 Retention of samples. When requested, all DPA samples shall be submitted to the acquiring activity or qualifying activity along with the DPA report.

4. SUMMARY. The following details shall be specified in the applicable acquisition document.

a. DPA sample size if different than specified in 3.1.

b. Radiography requirement (see 3.4.2 and 3.5.2).

c. Disposition of suspect lots and DPA samples if different than specified (see 3).

d. Any additional requirements for tests or for documentation in DPA report (see 3.2)

e. Electrical test requirement, if applicable.

f. Die shear strength for resistor and capacitor chips (see 3.5.10).

g. Internal water vapor requirement (see 3.4.4 and 3.5.5).

h. A manufacturer listing of defects, if applicable (see 3.4.5).

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METHOD 5010.4

TEST PROCEDURES FOR COMPLEX MONOLITHIC MICROCIRCUITS

1. PURPOSE. This method establishes screening, qualification, and quality conformance requirements for the testing of complex monolithic microcircuits to assist in achieving the following levels of quality (class level B and S) and reliability commensurate with the intended application. Complex monolithic microcircuits are defined as monolithic devices that contain a minimum of 4,500 transistors. It shall be used in conjunction with other documentation such as appendix A of MIL-PRF-38535 and an applicable device specification or drawing to establish the design, material, performance, control, and documentation requirements which are needed to achieve prescribed levels of device quality and reliability.

2. APPARATUS. Suitable measurement equipments necessary to determine compliance with applicable acquisition documents and other apparatus as required in the referenced test methods.

3. PROCEDURE. The procedures defined herein, including appendix I and II, outline the requirements and testing necessary to certify and qualify a complex microcircuit design, fabrication, assembly and testing facility. It illustrates the concept of generic qualification through the use of standard evaluation circuits and process monitors.

3.1 Test procedures for complex monolithic microcircuits. Complex monolithic microcircuits shall be tested as described herein, and in the device specification or drawing.

3.1.1 Precedence. Unless otherwise specified in the device specification or drawing, the test requirements and conditions shall be given herein.

3.1.2 Electrostatic discharge sensitivity. Electrostatic discharge sensitivity testing, marking, and handling shall be in accordance with appendix A of MIL-PRF-38535.

3.1.3 Failure analysis. When required by the applicable device specification failure analysis of devices rejected during any test in the screening sequence shall be accomplished in accordance with method 5003, test condition A.

3.1.4 Failure analysis class level S. Class level S devices shall be analyzed in accordance with method 5003, test condition B to identify the cause for failed lots and burn-in failures in accordance with appendix A of MIL-PRF-38535, A.4.3.3.1, and A.4.6.1.2.1. The documented results shall only be reported to the qualifying or acquiring activity when specifically requested.

3.1.5 Class requirements. Within tables having a class column, only those test and inspections or subgroups identified with "B" are applicable to class level B. All apply to class level S.

3.1.6 Radiation. When required by the applicable device specification or drawing, qualification, and quality conformance inspection requirements for radiation hardness assured devices are in addition to the normal class level S and B requirements. These requirements for each specified radiation levels (M, D, P, L, R, F, G and H) are detailed in table VIII herein.

3.2 Element evaluation.

3.2.1 General.

3.2.1.1 Element. Herein "element" refers to materials for device assembly. Before device assembly, element characteristics shall be evaluated and verified to assure their compatibility with element specifications, device requirements, and manufacturing procedures (see table I). Also, characteristics which cannot be verified after manufacturing but could cause function failure shall be evaluated and verified before assembly.

TABLE I. Element evaluation summary.

Element	Paragraph	Requirement
Microcircuit wafer	3.2.2	Appendix II (herein)
Package	3.2.3	Table II (herein)

3.2.1.2 Element evaluation requirements. Element evaluation may be performed at either the element supplier or device manufacturing facility up to the point where the element must undergo processing or assembly prior to testing. If element evaluation is performed by the supplier, then the device manufacturer must obtain a summary of the results for verification, and record retention.

3.2.2 Microcircuit wafer evaluation.

3.2.2.1 Definition. Diffused wafers used and evaluated shall, as a minimum, be complete with interconnect layers and glassivation from material that was homogeneously processed through wafer fabrication.

3.2.2.2 General. For the purpose of microcircuit wafer evaluation and wafer lot acceptance, measurement of the process monitor (PM), verifying that the identified parameters are within process limits, will be required from each wafer lot in accordance with appendix II wafer lot acceptance herein. Each die from each diffused wafer lot shall be electrically tested prior to assembly in accordance with the manufacturer's in-house documentation.

3.2.3 Package evaluation. Each package type shall be evaluated and characterized in accordance with table II herein prior to use. Finite element analyses techniques may be used. Packages used for complex monolithic microcircuits and fabricated to this test method shall be tested as follows:

3.2.3.1 Definition. Package used and evaluated shall consist of the same element specifications, materials, and finish; and homogeneously processed through device assembly.

3.2.3.2 Incoming inspection.

a. From the initial package inspection lot, a randomly selected sample shall be subjected to package evaluation (see table II). Additionally, subgroup 3 testing shall be accomplished using sealed packages. A die may be attached. Subgroups 2, 3, and 4 apply to cases only.

b. Additionally, subgroups 1, 2, and 3 of table II shall be accomplished for each subsequent acquisition.

c. For solderability (subgroup 2), lead integrity (subgroup 3), and metal package isolation (subgroup 4) defined within table II, a quantity (accept number) of 15 (0) shall apply to the number of terminals or leads tested. The leads shall be randomly selected from the three packages.

TABLE II. Package evaluation requirements.

Subgroup	Class levels		Test	MIL-STD-883		Quantity (accept number)	Reference paragraph
	S	B		Method	Condition		
1	X	X	Physical dimensions	2016		15 (0)	3.2.3.3
2	X	X	Solderability	2003	Solderability temperature 245 ±5°C	3 (0) 1/	
3	X	X	Thermal shock or Temperature cycle	1011 1010	C C (20 cycles)	3 (0)	
	X	X	High temperature bake	1008	2 hours at 150°C	3 (0)	
	X	X	Lead integrity	2004 2028	B2 (lead fatigue) D (leadless chip carriers) B1 (leaded chip carrier packages) (Pin grid array leads and rigid leads)	3 (0) 1/	
	X	X	Seal	1014	D Sealed cases	3 (0)	
4	X	X	Metal package isolation	1003	600 V dc, 100 nA maximum	3 (0) 1/	3.2.3.4
5	X	X	Insulation	1003	2/	3 (0)	
6	X	X	Conductor	MIL-STD- 202 method 307	2/	3 (0)	
7	X	X	Thermal characterization	1012		3/	

1/ A quantity (accept number) of 15 (0) shall apply to the number of terminals or leads to be tested. The leads shall be randomly selected from three packages minimum.
2/ Selected from three packages minimum. Conditions as specified by acquisition document and Appendix A of MIL-PRF-38535.
3/ Required on all package types prior to initial use.

3.2.3.3 Subgroup 1. Separately verify case and cover dimensional compliance with the device specification or drawing.

3.2.3.4 Subgroup 4. For metal cases with leads separated by an insulator, measure insulation resistance between the metal body of the case and the leads that are isolated from the case. This test does not apply to nonmetallic cases.

3.3 Manufacturing control.

3.3.1 Process control requirements. Line control as detailed below is required.

3.3.1.1 Wafer fabrication controls. Wafer fabrication shall be controlled in accordance with the manufacturer's fabrication baseline and documented procedures of the fabrication process.

3.3.1.2 Assembly controls. Assembly controls shall be in accordance with the manufacturer's assembly baseline and documented assembly procedures and additions herein

3.3.2 Design/layout system control. Design/layout controls shall be implemented using appendix I as a guide.

3.3.3 Testing controls. Documentation of testing controls shall meet the requirements of MIL-PRF-38535, appendix A.

3.3.3.1 Test vectors. The manufacturing-level logic test vectors shall be graded for fault coverage using a fault simulator. The resulting fault coverage shall be reported in the device specification or drawing. Fault coverage shall be based on the detectable equivalence classes of single, permanent, stuck at zero, and stuck at one faults on all logic lines of a structural logic model. The logic model shall be expressed in terms of gate-level primitives or simple atomic functions (such as flip-flops). Large, regular structures such as RAMs and ROMs shall not be modeled at the gate level; rather, documentation shall be provided to show that these structures are tested using appropriate procedures (such as, galloping patterns for a RAM).

3.3.3.2 Built-in-test/build-in-redundancy. When specified in the device specification or drawing, the following shall apply.

3.3.3.2.1 Probe/bond sites. The device shall contain probe/bond sites to allow testing using the full set of test vectors specified in the device specification or drawing.

3.3.3.2.2 Built-in redundancy for yield enhancement. Where built-in redundancy is used to provide yield enhancement, testing shall be included to provide a statistic which represents the amount of alternate element selection utilized.

3.3.3.2.3 Built-in redundancy using self test and fix. Where built-in redundancy is provided in the form of self test and fix, the circuitry will be capable of interrogation to determine the level of redundancy remaining on the device.

3.3.4 Quality controls. The product assurance program plan shall be in accordance with MIL-PRF-38535, appendix A.

3.3.4.1 Process monitor. Process control and stability of dc parameters must be demonstrated through the use of the manufacturer's process monitor (PM). The PM is to be designed so that the dc process parameters may be measured in wafer form. The PM may also be packaged so as to permit biasing of those circuits for measurement. The PM design must be submitted to the qualifying activity for approval prior to qualification and must contain as a minimum the structures outlined in table I of appendix II herein.

3.3.4.1.1 Process monitors for other technology devices. An adequate set of PM's applicable for other technology devices shall be generated to assure that applicable failure mechanisms are detected and submitted for approval by the qualifying activity.

3.3.4.2 Qualification device. A qualification device shall be used to demonstrate process stability and reliability. The qualification device, either a standard evaluation circuit (SEC) or an actual device (worst case design) shall be submitted to the qualifying activity for approval and as such contain the basic information as detailed herein. The qualification device shall be fabricated with the same process and designed to the same design rules that will produce any device in the technology to be qualified. The qualification device design shall be configured in such a manner so as to evaluate the reliability of the underlayer designs (e.g., diffusion) and evaluate the worst case design rule conditions on the personalization layers. The design should utilize cell libraries as well as test structures which will detect metal to metal shorting or opening, high via resistance and dielectric pinholes during reliability life testing, where applicable. The following structures are suggested:

Parameter	Structure
Functionality and performance	Large functional block (ALU), ring oscillator
Contact resistance/electromigration	Contact strings
Hot electrons/holes	Short channel devices
Oxide breakdown voltage	Capacitors
Resistance (electromigration test)	Metal stripes

3.4 Screening procedures for microcircuits. Screening of microcircuits shall be conducted as described in 3.4 through 3.4.13 and table III herein. This provision does not preclude the performance of additional tests or inspection which may be required for specific devices or which may be desirable to optimize results of screening; however, any such special test inspection shall be subjected to the requirements of appendix A of MIL-PRF-38535, A.4.3.4 and A.4.3.7. Sampling inspections shall not be an acceptable substitute for any specified screening test. Any burn-in, in addition to that specified, is only permitted when documented in the lot records, and any failures shall be counted in applicable PDA calculations. Where end point or post test measurements are required as part of any given test method used in the screening procedure and where such post-test measurements are duplicated in the interim (post burn-in) or final electrical tests that follow, such measurements need not be duplicated and need to be performed only as part of the interim (post burn-in) or final electrical tests. Devices which pass screening requirements of a higher reliability level shall be considered to meet the screening requirements of all lower levels. In no case shall screening to a lower level than that specified be permitted.

3.4.1 General.

a. Devices that fail any test or inspection criteria in the screening sequence shall be removed from the lot at the time of observation or immediately at the conclusion of the test in which the failure was observed. Once rejected and verified as a device failure, no device may be retested for acceptance. Unless otherwise specified in the device specification or drawings, electrical rejects may be used to satisfy sample selection requirements for qualification and quality conformance inspection in accordance with 3.5.

b. Device screening shall be performed in the sequence shown in table III except where variations in sequence are specifically allowed herein.

TABLE III. Device screening.

Screen	Class level S		Class level B		Reference paragraph
	Method	Reqmt	Method	Reqmt	
Wafer lot acceptance	5010 appendix II and 5007	All lots	5010 appendix II	All lots	
Nondestructive bond pull	2023	100%			
Internal visual	2010, test condition A	100%	2010, test condition B	100%	3.4.2
Stabilization bake. No end point measurements required					3.4.3
Temperature cycling or thermal shock	1010, test condition C	100%	1010, test condition C 1011, test condition A	100% 100%	3.4.5
Constant acceleration	2001, test condition E (min) Y1 orientation only	100%	2001, test condition E (min) Y1 orientation only	100%	3.4.6
Visual inspection		100%		100%	
Particle impact noise detection (PIND)	2020, test condition A	100%			3.4.7
Serialization		100%			
Interim (pre-burn-in) electrical parameters	In accordance with applicable device specification	100%	In accordance with applicable device specification	100%	3.4.9.1
Burn-in test	1015 240 hours at 125°C minimum	100%	1015 160 hours at 125°C minimum	100%	3.4.10
Interim (post-burn-in) electrical parameters	In accordance with applicable device specification	100%		Optional	3.4.9.1
Reverse bias burn-in	1015; test condition A or C, 72 hours at 150° minimum.	100%			

TABLE III. Device screening -Continued.

Screen	Class level S		Class level B		Reference paragraph
	Method	Reqmt.	Method	Reqmt.	
Interim (post-burn-in) electrical parameters	In accordance with applicable device specification	100%	In accordance with applicable device specification	100%	3.4.9.1
Percent defective allowable (PDA) calculation	5 percent (subgroup 1, table IV) 3 percent functional parameters at 25°C (subgroup 7 table IV)	All lots	5 percent (subgroup 1, table IV)	All lots	3.4.9.1
Final electrical test	In accordance with applicable device specification		In accordance with applicable device specification		3.4.11
a. Static tests		100%		100%	
(1) 25°C (subgroup 1, table IV)		100%		100%	
(2) Maximum and minimum rated operating temp. (subgroup 2, 3, (table IV)		100%		100%	
b. Dynamic or functional tests					
(1) 25°C (subgroup 4, or 7, table IV)		100%		100%	
(2) Minimum and maximum rated operating temp. (subgroup 5 and 6, or 8, table IV)		100%		100%	
c. Switching tests at 25°C (subgroup 9,) table IV)		100%		100%	

TABLE III. Device screening - Continued.

Screen	Class level S		Class level B		Reference paragraph
	Method	Reqmt.	Method	Reqmt.	
Seal Fine Gross	1014	100%	1014	100%	3.4.8
Radiographic	2012 two views	100%			3.4.12
Qualification or quality conformance inspection test sample selection	See 3.5		See 3.5		
External visual	2009	100%	2009	100%	3.4.13

3.4.2 Internal visual inspection. Internal visual inspection shall be performed to the requirements of method 2010, condition A for class level S devices and condition B for class level B devices. Devices awaiting preseal inspection, or other accepted, unsealed devices awaiting further processing shall be stored in a dry, inert, controlled environment until sealed.

Unless otherwise specified, at the manufacturer's option, test samples for group B, bond strength may be randomly selected prior to or following internal visual, prior to sealing provided all other specification requirements are satisfied (e.g., bond strength requirements shall apply to each inspection lot, bond failures shall be counted even if the bond would have failed internal visual exam).

The alternate procedure of 3.4.2.1 shall be used when any of the following criteria are met:

a. Minimum horizontal geometry is less than three microns.

b. Metallization consists of two or more levels.

c. Opaque materials mask design features.

3.4.2.1 Alternate procedures for class level B microcircuits. Alternate procedures may be used on an optional basis on any microcircuit, provided that the conditions and limits of the alternate procedures are submitted to, and approved by the preparing activity, or the acquiring activity.

3.4.2.1.1 Alternate procedures. The deletions and the changes stated herein are allowable only if the requirements of alternate 1 or alternate 2 are met.

Alternate 1: The deletions and the changes stated in 3.4.2.1.1a. are allowable for complex monolithic microcircuits for class level B product only if the requirements of 3.4.2.1.1.b and 3.4.2.1.1.c are imposed and any of the following conditions exists.

1. Minimum horizontal geometry is less than 3 micrometers (μm).
2. Interconnects consisting of two or more levels.
3. Opaque materials mask design features.

a. For inspection of each microcircuit die, delete the inspection criteria of 3.1.1, 3.1.2, 3.1.3, 3.1.4, 3.1.5, 3.1.6, 3.1.7, and 3.2.5 of condition B of method 2010 and for use in conjunction with alternate procedures, add 3.1.1.1, 3.1.1.2, 3.1.1.6, 3.1.3, 3.1.4, and 3.2.5 to the low magnification inspection of method 2010.

b. Temperature cycling (3.4.5). The minimum total number of temperature cycles shall be 50. The manufacturer may reduce the number of temperature cycles from 50 to the 10 required as part of normal screening based upon data justifying the reduction in temperature cycles approved by the preparing activity and an approved plan which shall include the following criteria:

(1) Reduction of test must be considered separately for each wafer fabrication line and each die family.

(2) The manufacturer shall demonstrate that the wafer fabrication line that produces product which will involve reduction of temperature cycles is capable and in process control.

(3) The manufacturer shall perform a high magnification visual inspection on a small sample of devices (e.g., 5(0)) to monitor the process. This inspection may be performed at wafer level.

c. Special electrical screening tests shall be applied to each microcircuit die at the wafer, individual die (chip) and packaged, or both, microcircuit level in accordance with the requirements of MIL-STD-883, method 5004, 3.3.2. The conditions and limits of the electrical tests (in table III format) shall be submitted to the preparing activity for approval and subsequently maintained on file with the qualifying activity. These special screens are in addition to the required electrical parametric tests which the device must pass and shall be designed to screen out devices with defects that were not inspected to the full criteria of 3.4.3 (internal visual). Due to the nature of these tests, they are not to be repeated as part of the qualification and quality conformance procedures.

Alternate 2: The requirements and conditions for use of this alternate are contained in appendix A of method 5004. This option applies to both class level B and class level S microcircuits.

3.4.3 Stabilization bake. Stabilization bake is not required for class level S or class level B product unless specified in the device specification or drawing.

3.4.4 Visual inspection for damage. The manufacturer may inspect for damage after each screening step. Damaged devices shall be removed from the lot.

3.4.5 Temperature cycling or thermal shock. All devices shall be subjected to the requirements of temperature cycling or thermal shock. The device specifications or drawing shall specify which screen shall be employed. Temperature cycling shall be in accordance with MIL-STD-883, method 1010, condition C minimum. For class level B, this test may be replaced with thermal shock in accordance with MIL-STD- 883, method 1011, condition A minimum.

3.4.6 Constant acceleration. All devices shall be subjected to constant acceleration, in the Y_1 axis only, in accordance with MIL-STD-883, method 2001, condition E (minimum). Microcircuits which are contained in packages which have an inner seal or cavity perimeter of two inches or more in total length or have a package mass of five grams or more may be treated in accordance with provisions below as an alternate to this procedure. Delete test condition E and replace with test condition D. Unless otherwise specified, the stress level for large, monolithic microcircuit packages shall not be reduced below condition D. If the stress level specified is below condition D, the manufacture shall have data to justify this reduction and this data must be maintained and available for review by the preparing or acquiring activity. The minimum stress level allowed is condition A.

3.4.7 Particle impact noise detection test (PIND). Testing to be performed in accordance with appendix A of MIL-PRF-38535, A.4.6.3. The PIND test may be performed in any sequence after temperature cycling and prior to final electrical test.

3.4.8 Seal (fine and gross leak) testing. For class level S devices seal testing may be performed in any sequence between the final electrical test and external visual, but it shall be performed after all shearing and forming operations on the terminals. For class level B devices, fine and gross seal test shall be performed separate or together in any sequence and order between 3.4.7 and 3.4.13 and they shall be performed after all shearing and forming operations on the terminals. When the 100 percent seal screen cannot be performed following all shearing or forming operations (i.e., flat packs, brazed lead packages, and chip carriers) the seal screen shall be done 100 percent prior to those shearing and forming operations and a sample test using sample size number of 45 (C = 0) shall be performed on each inspection lot following these operations to verify integrity. For devices with leads that are not glass-sealed and that have a lead pitch less than or equal to 1.27 mm (0.050 inch), the sample seal test shall be performed using an acceptance criteria of a quantity (accept number) of 15 (0). If sample fails the sample acceptance criteria, all devices in the inspection lot represented by the sample tested shall be subjected to and pass 100 percent fine and gross leak seal screens.

3.4.9 Electrical measurements.

3.4.9.1 Interim (pre- and post-burn-in) electrical parameters. Interim (pre- and post-burn-in) electrical testing shall be performed when specified, to remove defective devices prior to further testing or to provide a basis for application of percent defective allowable (PDA) criteria when a PDA is specified. The PDA shall be 5 percent or one device, whichever is greater. This PDA shall be based, as a minimum, on failures from group A, subgroup 1 plus deltas (in cases where delta parameters are specified) with the parameters, deltas, and any additional subgroups (or subgroups tested in lieu of A-1) subject to the PDA as specified in the applicable device specification or drawing. If no device specification or drawing exists, subgroups tested shall at least meet those of the most similar device specification or Standard Microcircuit Drawing. In addition, for class level S the PDA shall be 3 percent (or one device, whichever is greater) based on failures from functional parameters measured at room temperature. For class level S screening, where an additional reverse bias burn-in is required, the PDA shall be based on the results of both burn-in tests combined. The verified failures after burn-in divided by the total number of devices submitted in the lot or sublot for burn-in shall be used to determine the percent defective for that lot, or sublot and the lot or sublot shall be accepted or rejected based on the PDA for the applicable device class. Lots and sublots may be resubmitted for burn-in one time only and may be resubmitted only when the percent defective does not exceed twice the specified PDA, or 20 percent, whichever is greater.

3.4.9.2 Pattern failures. Pattern failure criteria may be used as an option for class level B, provided that:

a. Inspection lot size is less than 500 devices.

b. Pre burn-in electrical testing is done.

3.4.9.2.1 Pattern failures criteria. A maximum number of pattern failures (failures of the same part type when the failures are caused by the same basic failure mechanism) shall apply as specified in the acquisition document. If not otherwise specified, the maximum allowable pattern failures shall be five. Accountability shall include burn-in through final electrical test.

3.4.9.2.2 Pattern failure resubmission. When the number of pattern failures exceeds the specified limits, the inspection lot shall be rejected. At the manufacturer's option, the rejected lot may be resubmitted to burn-in one time provided:

a. The cause of the failure has been evaluated and determined.

b. Appropriate and effective corrective action has been completed to reject all devices affected by the failure cause.

c. Appropriate preventive action has been initiated.

3.4.10 Burn-in. Device burn-in shall be performed in accordance with the requirements of method 1015 conditions A, B, C, D, or E. Regardless of power level, devices shall be able to be burned-in at their maximum rated operating temperature. For devices whose maximum operating temperature is stated in terms of ambient temperature, T_A, table I of method 1015 applies. For devices whose maximum operating temperature is stated in terms of case temperature, T_C, and where the ambient temperature would cause T_J to exceed 200°C for class level B or 175°C for class level S, the ambient operating temperature may be reduced during burn-in from 125°C to a value that will demonstrate a T_J between 175°C and 200°C (for both class levels S and B) and T_C equal to or greater than 125°C without changing the test duration. Data supporting this reduction shall be available to the acquiring and qualifying activities upon request.

3.4.11 Final electrical measurements. Final electrical testing of microcircuits shall assure that the microcircuits tested meet the electrical requirements of the applicable device specification or drawing and shall include, as a minimum, the tests of group A, subgroups 1, 2, 3, 4 or 7, 5 and 6, or 8, and 9.

3.4.12 Radiographic. The radiographic screen may be performed in any sequence after PIND test and before external visual inspection. Only one view is required for flat packages and leadless chip carriers having lead (terminal) metal on four sides.

3.4.13 External visual inspection. All devices shall be inspected in accordance with MIL-STD-883, method 2009, prior to acceptance for shipment

3.5 Qualification and quality conformance procedures. Qualification and quality conformance shall be performed in accordance with A.4.4 qualification procedures and A.4.5 quality conformance inspection of appendix A of MIL-PRF-38535 except as modified herein. The qualification device shall be used for QCI testing in accordance with 3.5.3 herein, as well as for qualifying the process line. Life testing requirements shall follow the same criteria as burn-in (3.4.10 herein) for reduced temperature.

3.5.1 Qualification testing. Initial product process qualification shall be in accordance with MIL-STD-883 method 5005. Change to qualified product shall be addressed in accordance with MIL-STD-883, method 5005 and appendix A of MIL-PRF-38535, A.3.4.2. The SEC shall be used for group D inspection whenever practical; where the SEC cannot be used, another die may be used (for gate arrays, 60 percent or greater utilization required). Utilizing the qualification device the process monitor, the manufacturer shall demonstrate:

a. Process control and stability.

b. Process/device reliability.

c. Design and simulation control.

3.5.1.1 Detailed qualification test plan. The manufacturer shall submit to the qualifying activity for approval a detailed qualification test plan to assure conformance to 3.5.1 herein. The test plan shall, as a minimum, define test groups, subgroups, conditions, and sampling plans in accordance with method 5005, as well as the tests to carry out 3.5.1.2, 3.5.1.3, and 3.5.1.4.

3.5.1.2 Database test. For qualification, at least five PM's per wafer (located in accordance with appendix II) shall be measured to ensure the establishment of a statistically valid database on which a decision can be made as to whether the manufacturer's process is stable and under control.

3.5.1.3 Qualification device design and test plan. Qualification device design and test plan to be used to qualify the manufacturing line shall be submitted to the qualifying activity for approval. The design must meet the minimum requirements of 3.3.4.2 herein. The test plan must include life test requirements. If a SEC is used as the qualification device, data demonstrating process reliability from lots processed within 12 months of qualification and that an on-going SEC program is in effect shall be submitted for qualifying activity review.

3.5.1.4 Design and simulation verification. Design and simulation verification shall be accomplished as follows:

a. Design rule check (DRC) verification. DRC software shall be run on a design which contains known design rule violations.

b. Electrical rule check (ERC) verification. ERC software shall be run on a design which contains known electrical rule violations (e.g., fan-out violations).

c. Layout versus schematic (LVS) check.

d. Correct by construction. If the manufacturers' design methodology is based on a "correct by construction" approach, distinct DRC, ERC, and LVS software is unnecessary and a, b, and c above do not apply. However, the manufacturer shall provide suitable data to demonstrate the correct performance of "correct by construction" software.

e. Computer aided design (CAD) system control shall be in accordance with appendix I herein.

3.5.2 Quality conformance inspection. This procedure, as applicable to the microcircuit type and class, shall apply for all quality conformance inspection requirements. Subgroups within a group of tests may be performed in any sequence but individual tests within a subgroup (except group B, subgroup 2) shall be performed in the sequence indicated for groups B, C, D, and E tests herein. Where end-point electrical measurements are required for subgroups in groups B, C, D, and E testing herein, they shall be as specified in the applicable device specification or drawing. Where end-point measurements are required but no parameters have been identified in the acquisition document for this purpose, the final electrical parameters specified for 100 percent screening shall be used as end-point measurements. Electrical reject devices from the same inspection lot may be used for all subgroups when end-point measurements are not required.

3.5.2.1 Radiation hardness. Quality conformance inspection requirements for radiation hardness assured devices are in addition to the normal class level S and B requirements. Those requirements are detailed in table VIII (group E) herein. The radiation levels (M, D, P, L, R, F, G and H) are defined in appendix A of MIL-PRF-38535.

3.5.2.2 Quality conformance inspection. For class level B quality conformance inspection, each inspection lot (sublot) shall pass groups A, B, and E (when applicable) tests or be accepted in accordance with 3.5.3 herein and the periodic group C and D tests shall be in accordance with appendix A of MIL-PRF-38535. End point electrical parameters shall be as specified in 3.5.2.3 herein. For class level S, each QCI inspection lot shall be assembled in accordance with the class level S requirements of appendix A of MIL-PRF-38535. Quality conformance testing for class level S shall be in accordance with tables IV, V, VI, and VII herein.

3.5.2.3 End point electrical parameters. Where intermediate and end point electrical measurements are required for subgroups B, C, D, and E testing, they shall be as specified in the applicable device specification or drawing where required and when end point parameters have not been identified, group A, subgroup 1, 2, 3, 4 or 7, and 9 shall be used for end point measurements.

3.5.2.4 Constant acceleration. Constant acceleration shall be performed in accordance with method 2001, test condition E for all applicable subgroups except as allowed in accordance with 3.4.6, herein.

3.5.3 Quality conformance testing. Conformance testing shall be performed through the use of the identified quality conformance vehicles.

Quality conformance test		Quality conformance vehicle	Frequency
Table IV	Group A	Actual device	Each inspection lot
Table V	Group B	Actual device	Each inspection lot
Table VI	Group C	SEC or actual device	3 months
Table VII	Group D	SEC or actual device	6 months
Table VIII	Group E	Actual device	See MIL-PRF-38535. appendix A

3.5.3.1 Alternate group A method. The alternate group A method below may be used provided that:

a. Inspection lot size is less than 500 devices.

b. Final electrical test shall assure that the electrical requirements of the device specification or drawing are met and shall include the tests of group A, subgroups 1, 2, 3, 4 or 7, 5 and 6 or 8, 9, as a minimum.

c. All test software and procedures are under document control.

3.5.3.1.1 In-line verification testing.

a. For each test set up (and operator for manual testing), production runs correlation unit to assure that the accuracy requirements of MIL-STD-883 4.5.2 are being met.

b. Testing is performed using the verified set up.

c. At the completion of testing utilizing the verified set up (not to exceed 8 hours and at the change of operators) a separate party (QA or QA designate) then verifies the production testing by:

(1) Checking visually to verify that the correct fixture, equipment, software, and procedure(s) were used.

(2) Actual testing of controlled known good device utilizing the fixtures, set ups, software and procedures that were used by production. Variables data for all required group A tests shall be read and recorded for the controlled unit. This data shall be maintained with the lot.

(3) The verifying party shall stamp or sign the lot traveler to attest that the above data meets the test requirements and that all of the above items were performed and were found to be acceptable.

(4) Failure of the verification test shall require, as a minimum, engineering to perform a detailed review of hardware/software/set up and parts. If engineering locates the problem, a one time only 100 percent retest to all group A requirements for all devices that were under consideration for acceptance shall be required. If the engineering review does not locate the problem, the verification unit shall undergo failure analysis before retesting the lot.

(a) If failure analysis locates the problem, the entire group of devices being considered for acceptance at the time of the failure may be retested for appropriate subgroup(s) acceptance one time only by repeating this group A method.

(b) If the failure analysis does not specifically locate the problem, the lot may be considered for acceptance one time only by 100 percent retesting of all the devices of the group A requirements and by repeating this group A method.

TABLE IV. Group A electrical test. 1/

Subgroup	Parameters 2/ 3/ 4/ 5/	Quantity/ acceptance number
1	Static test at +25°C	116/0
2	Static tests at maximum rated operating temperature	116/0
3	Static tests at minimum rated operating temperature	116/0
4	Dynamic test at +25°C	116/0
5	Dynamic tests at maximum rated operating temperature	116/0
6	Dynamic tests at minimum rated operating temperature	116/0
7	Functional test at +25°C	116/0
8	Functional tests at maximum and minimum rated operating temperatures	116/0
9	Switching tests at +25°C	116/0
10	Switching tests at maximum rated operating temperature	116/0
11	Switching tests at minimum rated operating temperature	116/0

1/ The specific parameters to be included for tests in each subgroup shall be as specified in the applicable acquisition document. Where no parameters have been identified in a particular subgroup or test within a subgroup, no group A testing is required for that subgroup or test to satisfy group A requirements.

2/ At the manufacturer's option, the applicable tests required for group A testing (see 1/) may be conducted individually or combined into sets of tests, subgroups (as defined in table I), or sets of subgroups. However, the manufacturer shall predesignate these groupings prior to group A testing. Unless otherwise specified, the individual tests, subgroups, or sets of tests/subgroups may be performed in any sequence.

3/ The sample plan (quantity and accept number) for each test, subgroup, or set of tests/subgroups as predesignated in 2/ above, shall be 116/0.

4/ A greater sample size may be used at the manufacturer's option; however, the accept number shall remain at zero. When the (sub)lot size is less than the required sample size, each and every device in the (sub)lot shall be inspected and all failed devices removed from the (sub)lot for final acceptance of that test, subgroup, or set of tests/subgroups, as applicable.

5/ If any device in the sample fails any parameter in the test, subgroup, or set of tests/subgroups being sampled, each and every additional device in the (sub)lot represented by the sample shall be tested on the same test set-up for all parameters in that test, subgroup, or set of tests/subgroups for which the sample was selected, and all failed devices shall be removed from the (sub)lot for final acceptance of that test, subgroup, or set of tests/subgroups, as applicable. For class level S only, if this testing results in a percent defective greater than 5 percent, the (sub)lot shall be rejected, except that for (sub)lots previously unscreened to the tests that caused failure of this percent defective, the (sub)lot may be accepted by resubmission and passing the failed individual tests, subgroups, or set of tests/subgroups, as applicable, using a 116/0 sample.

TABLE V. Group B testing.

Subgroup	Class level		Test	MIL-STD-883		quantity/(accept number) or sample size number, accept number	Referenced paragraph
	S	B		Method	Condition		
1	X	X	Physical dimensions	2016		2 (0)	
2	X		Particle impact noise detection test	2020	A or B	15 (0)	3.4.7
3	X	X	Resistance to solvents	2015		3 (0)	
4	X	X	Internal visual and mechanical	2014		1 (0)	3.4.2
5	X	X	Bond strength a. Thermocompression b. Ultrasonic or wedge c. Flip-chip d. Beam lead	2011	 C or D C or D F H	2 (0)	
6	X	X	Die shear strength or substrate attach strength	2019 or 2027		2 (0)	
7	X	X	Solderability	2003	Solder temperature 245°C ±5°C	1 (0)	
8	X	X	Seal a. Fine b. Gross	1014		Sample size number = 15 C = 0	3.4.8

TABLE VI. Group C testing.

Subgroup	Class levels		Test	MIL-STD-883		Sample size number, accept number	Referenced paragraph
	S	B		Method	Condition		
1	X	X	External	2009		Sample size number = 15	3.4.13
	X	X	Temperature cycling	1010	C 100 cycles minimum	C = 0	3.4.5
	X	X	Mechanical shock or constant acceleration	2002 2001	B, Y1 axis E, Y1 axis		3.4.6
	X	X	Seal (fine and gross)	1014			3.4.8
	X		Radiographic	2012	Y axis		3.4.12
	X	X	Visual examination		In accordance with visual criteria of method 1010.		
	X	X	End point electrical		As specified in accordance with device specification		3.5.2.3
2	X	X	Steady-state life test	1005	1,000 hours at +125°C minimum	Sample size number = 22 C = 0	3.5.2.3
			End point electrical		As specified in accordance with device specification		

TABLE VII. Group D testing.

Subgroup	Class		Test	MIL-STD-883		Quantity/ accept number	Referenced paragraph
	S	B		Method	Condition		
1	X	X	Internal water vapor content 5000 PPM maximum water content at +100°C	1018		3 devices (0 failures) or 5 devices (1 failure)	
2	X	X	Moisture resistance	1004		5 (0)	
3	X	X	Salt atmosphere	1009		5 (0)	

TABLE VIII. Group E (radiation hardness assurance tests). 1/

Test	MIL-STD-883		Class level S		Class level B	
	Method	Condition	Quantity/ accept number	Notes	Quantity/ accept number	Notes
Subgroup 1 2/						
Neutron irradiation	1017	+25°C				
a. Qualification			a. 11 (0)	3/	a. 11 (0)	4/
b. QCI			b. 11 (0)	3/	b. 11 (0)	4/
Endpoint electrical parameters		As specified in accordance with device specification				
Subgroup 2 5/						
Steady-state total dose irradiation	1019	+25°C Maximum supply voltage				
a. Qualification			a.	a.	a. 22 (0)	7/
b. QCI			4 (0)	6/	b. 22 (0)	7/
Endpoint electrical parameters		As specified in accordance with device specification	2 (0) b. 4 (0) 2 (0)	8/ b. 6/ 8/		

1/ Parts used for one subgroup test may not be used for other subgroups but may be used for higher levels in the same subgroup. Total exposure shall not be considered cumulative unless testing is performed within the time limits of the test method.

2/ Waive neutron test for MOS IC devices except where neutron susceptibility is less than 10^{13} neutrons/cm^2 (e.g., charge coupled devices, BICMOS, ect.). Where testing is required, the limit for neutron fluence shall be $2x10^{12}$ neutrons/cm^2.

3/ Per wafer lot. If one part fails, seven additional parts may be added to the test sample with no additional failures allowed, 18(1).

4/ Per inspection lot. If one part fails, seven additional parts may be added to the test sample with no additional failures allowed, 18(1).

5/ Class level B devices shall be inspected using either the class level B quantity/accept number criteria as specified, or by using the class level S criteria on each wafer.

6/ Per wafer for device types with less than or equal to 4,000 equivalent transistors/chip selected from the wafer at a radius approximately equal to two-thirds of the wafer radius, and spaced uniformly around this radius.

7/ Per inspection lot. If one part fails, 16 additional parts may be added to the test sample with no additional failures allowed, 38(1).

8/ Per wafer for device types with greater than 4,000 equivalent transistor/chip selected from the wafer at a radius approximately equal to two-thirds of the wafer radius and spaced uniformly around this radius.

3.6 Disposition of samples. Disposition of sample devices in groups A, B, C, D, and E testing shall be in accordance with the applicable device specification.

3.7 Substitution of test methods and sequence.

3.7.1 Accelerated qualification or quality conformance testing for class level B. When the accelerated temperature/time test conditions of condition F of method 1005 are used for any operating life or steady-state reverse bias subgroups on a given sample for purposes of qualification or quality conformance inspection, the accelerated temperature/time test conditions shall be used for all those named subgroups. When these accelerated test conditions are used for burn-in screening test (test condition F of method 1015) or stabilization bake for devices with aluminum/gold metallurgical systems (any test temperature above the specified maximum rated junction temperature) for any inspection lot, it shall be mandatory that they also be used for the operating life, and steady-state reverse bias tests of method 5005, or herein as applicable, or qualification or quality conformance inspection. Qualification and quality conformance inspection may be performed using accelerated conditions on inspection lots that have been screened using normal test conditions.

3.8 Test results. Unless otherwise specified, test results that are required by the applicable acquisition document shall be reported in accordance with the general requirements of appendix A of MIL-PRF-38535 (see A.4.7).

4. SUMMARY. The following details shall be specified in the applicable device specification:

   a. Procedure paragraph if other than 3.1, and device class.

   b. Sequence of test, sample size, test method, and test condition where not specified, or if other than specified.

   c. Test condition, limit, cycles, temperatures, axis, etc., where not specified, or if other than specified (see 3).

   d. Acceptance procedure or sample size and acceptance number, if other than specified.

   e. Initial and interim (pre and post burn-in) electrical parameters for group A.

   f. Electrical parameters for groups B, C, D, and E end point measurements, where applicable.

   g. Burn-in test conditions (see table III) and burn-in test circuit.

   h. Delta parameter measurements or provisions for PDA including procedures for traceability or provisions for pattern failure limits including accountable parameters, test conditions, and procedures for traceability, where applicable.

   i. Final electrical measurements.

   j. Constant acceleration level.

   k. Requirements for failure analysis.

   l. Requirements for data recording and reporting if other than specified in 3.8.

   m. Restriction or resubmission of failed lots where applicable.

   n. Steady-state life test circuits, where not specified or if other than specified.

   o. Parameters on which delta measurements are required.

   p. Wafer travelers shall be used to record completion of each requirement of 3.4.2.1.1.

APPENDIX I

COMPUTER AIDED DESIGN (CAD)

10. SCOPE.

10.1 Scope. Additional line certification requirements. This appendix defines additional line certification requirements. The answers to the questions in this appendix shall be provided to the qualifying activity for approval. The manufacturer shall have the following additional information on file and available for review.

a. Design/layout rules as a manufacturer's controlled document.

b. A list of the cells in the manufacturer's cell library, cell performance data, and simulation verification data, if applicable.

c. Process monitor design used by the manufacturer.

d. Standard evaluation circuit implementation used by the manufacturer for qualification and qualification conformance inspection (QCI).

e. JEDEC benchmark macro set (see JEDEC standards 12, 12-1, 12-2, and 12-3), delay simulation data, if applicable.

f. A list of the software packages (including names and current version) used by the manufacturer in the circuit design process.

g. Design rule check (DRC) verification. DRC software shall be run on a design which contains known design rule violations.

h. Electrical rule check (ERC) verification. ERC software shall be run on a design which contains known electrical rule violations.

i. Layout versus schematic (LVS) checker.

j. If the manufacturer's design methodology is based on the "correct by construction" approach, distinct DRC, ERC, and LVS software is unnecessary and may not exist. In this case, the provisions of g., h., and i. do not apply. Instead, the manufacturer will provide suitable example data to demonstrate the correct performance of "correct by construction" software.

10.2 Functional delay simulation. To be retained by manufacturer; simulation to be derived from each final application specific electrical design and layout (i.e., post-routed design). Simulation will be done using actual delays and parasitics computed from the placement and layout of the device as it will be fabricated. Actual delays shall include the contribution associated with the delay through the gate, as well as the contribution due to actual metal capacitance and device loading on the output(s). Using these actual delays, the application specific integrated circuit (ASIC) designer shall insure that there are no timing violations remaining in the circuit. Such timing violations shall include, but not be limited to, setup, hold, critical delay path, and circuit race conditions due to variations in process, temperature and supply voltage. Simulation at the two worst case extremes (temperature, process, radiation (if applicable) and supply voltage) shall be identical with respect to circuit operation (final state of each signal in each clock cycle must be identical).

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10.3 Layout verification. The manufacturer shall retain the results of full mask level design rule checks, electrical rule checks, and connectivity checks (see 10.1) for each application specific design. Rule checking will encompass the rules set provided under 10.1 herein. The manufacturer will explain any rules not checked and all error reports produced by the checker. The LVS checker will ensure that the layout matches exactly the schematic simulated by the ASIC designer. Final layout verification results will not be required if the manufacturer's design methodology is "correct by construction." In this case, the manufacturer will explain the methodology and rules used, as well as any rules not checked and all error reports which were not corrected during construction of design.

10.4 Power routing simulation. To be retained by manufacturer; derived from each final application specific electrical design and layout. The worst case simulation of power buses shall show that at no time shall the localized bus current density exceed specification for allowable current density of the power bus material. In addition, at no point in the power bus shall voltage levels exceed design goals for IR drop values from the respective supply. Power routing simulation must be based upon actual placement of cells within the array. Such a simulation may be driven by Monte Carlo methods, or in conjunction with a digital simulator using the selected set of test vectors.

10.5 Cell design and simulation qualification. Cell design and simulation qualification shall be accomplished in a two step procedure consisting of:

a. Parameter verification/simulation verification, and

b. Functional verification.

A chip or set of chips, called the cell test chip set, shall be designed to provide access to a set of cells to test performance characteristics. The cell test chip set design must be submitted to the qualifying activity for approval prior to use. The cell test chip shall include as a minimum:

Description

Inverter

4-input NAND

2-input AND into 3-input NOR

D latch with active low reset

JK flip-flop with active low reset

TTL input buffer

CMOS input buffer

Output buffer

Three-state I/O buffer with pull-up

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The intent is to get a representative cross section of cell types (i.e., combinational, sequential, input, output). Chains shall be formed (when necessary to avoid rise and fall time measurement problems) and actual performance data over the full operating range shall be taken (a provision to extract for multiplexing and I/O buffer delay shall be included). Delay versus metal wire length and fanout for the above cells shall be determined. The actual performance data shall be submitted to the qualifying activity along with computer program simulation results. The actual performance data must be within the limits predicted by the simulation. If multipliers are used to extrapolate performance at the temperature extremes, such multipliers shall be verified as well.

In addition, for the above cells, a set of pins shall be provided on the test chip for observability. This will enable verification of functionality of the cells. (Note: Inputs and outputs may be multiplexed).

10.6 CAD routing and post routing simulation. A chip or set of chips shall be submitted for approval and used to qualify the manufacturer's ability to perform routing and to accurately predict post routing performance. The manufacturer must submit to the qualifying activity:

a. The actual measured performance data for each function over temperature and voltage.

b. The computer simulation performance prediction.

The two results will remain on file and the actual measured performances must fall between the simulation extremes.

20. APPLICABLE DOCUMENTS. (This section is not applicable to this document.)

30. CERTIFICATION QUESTIONS.

30.1 Cell libraries.

a. Who is the source for your cell libraries?

Own organization?

Work station vendors?

Outside commercial vendors?

Universities?

b. What verification or certification is done for cell libraries, including those obtained from outside organizations? Are macrocells implemented in silicon and verified for functionality and performance limits via actual hardware test? Is only software simulation performed?

c. How are cell libraries controlled (e.g., level of documentation, maintenance and revisions, specifications, additions)?

d. Provide company-approved cell library.

e. Identify those implemented and tested in silicon.

f. Is a designer allowed to tailor a macrocell or "roll his own" for a certain application? If so, how is the resulting macro tested to insure there are no problems?

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30.2 Design process.

a. Who does and who approves the various levels of design?

Requirements definition? Detail function definition? Detail design (e.g., gate level design)? Layout and mask generation?

b. What automatic aids are used for refinement from each design level to the next?

c. What automatic aids are used for verifying the refinement at each level (e.g., automatic checking of layout versus schematic)?

d. How is automatic placement and routing software verified and certified for use?

30.3 Simulation.

a. What simulators are used for:

Process simulation (e.g., SUPREME-II)?

Circuit simulation (e.g., SPICE, SCEPTRE)?

Gate level simulation (e.g., LASAR HITS)?

Switch level simulation?

Behavior/function simulation?

Dynamic timing analysis (to include actual delays due to placement and routing?

b. How are the above simulators verified? Are benchmarks used, and if so, what are these benchmarks?

c. Are the simulation results periodically checked against actual silicon test data (to complete the loop)?

30.4 Test.

a. What test tools are used for:

Automatic test vector generation?

Fault simulation?

Insertion of design-for-testability/built-in-test features? (And are they integrated with the design process?)

b. Who is responsible for test generation:

Foundry?

Customer?

Designer?

c. If test vectors are not generated by the foundry, are the submitted vectors evaluated by the foundry to determine the percentage of faults detected?

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30.5 Design rule checking.

a. Are design constraints enforced by the customers or management, such as:

Synchronous designs only?

Use of an approved set of cells/macrocells only?

Conservative use of electrical and switching limits?

Is the designer able to obtain waivers?

b. What design rule checkers (DRCs) are used for:

Physical rule checks (e.g., minimum spacing)?

Electrical rule checks (e.g., max current density, fanout restrictions)? Timing rule checks (e.g., worst-case timing paths)? Logical rule checks (e.g., unclocked feedback paths)?

c. Is each design subjected to the above DRCs?

d. How can the DRC software be shown to "work as advertised?"

e. If "correct by construction" techniques are used, what procedure is used, how is "correctness" assured?

30.6 Software control.

a. What are the sources of design and test software?

Own organization?

Workstation vendors?

Outside commercial vendors?

Universities?

b. How is design and test software approved and controlled:

Frequency of major/minor revision?

Trouble reports?

Regression testing?

c. What commercial CAD/CAE work stations or packages are used (e.g., MENTOR, Daisy, Silvar-Lisco)? Are modifications to any of the software packages permitted?

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30.7 How is interface with foundries and customers, or both done?

Data formats?

Media (e.g., magtapes, modems, DDN/Arpanet)?

Qualification of foundry via test chips?

Are evaluation chips available for customers to assess performance?

30.8 Who tests the chips?

At wafer level?

After packaging?

Burn-in?

Life testing?

What automatic test equipment types are used?

30.9 Masks.

a. What are the procedures for mask making, inspection, verification, and repair?

b. Is the design transferred to the fab house via an actual mask set or via software?

c. If design transfer is via software, what are the procedures used to verify the mask design?

30.10 Wafer acceptance.

a. What wafer inspection/accept-reject criteria are currently used (i.e., how is process control/stability demonstrated)?

b. Which of the following process control indicators are used?

Kerf test structure measurements? (What structures are in the kerf; how many kerf sites are measured; what data are taken; tolerances allowed?)

Drop-ins: (What does the drop-in design consist of? How many drop-ins per wafer? Allowed parameter tolerances?)

Visual test structures?

c. How is high magnification inspection being accomplished? Are voltage stress tests used in lieu of some of the high mag inspections?

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30.11 Reliability evaluation.

a. How is the reliability of the process proven? It is done via:

Standard evaluation chips (SECs) or reliability evaluation chips?

Test dice with specialized/optimized test structures?

b. If such vehicles do not exist, how is the processing shown to be free of reliability hazards?

c. How can the power buses be guaranteed to be within current density specifications at all times and under all conditions?

d. For CMOS technology, how is a latch-up free process assured?

e. For bipolar technology, is any radiation hardness characterization done?

30.12 Documentation.

a. What are the procedures for certifying and controlling the configuration of software?

b. What are the procedures outlining in detail the process flows for computer-aided design/manufacture/engineering/test (CAD/M/E/T)?

c. If neither of above is available, when will they be available?

APPENDIX II

WAFER LOT ACCEPTANCE

10. SCOPE.

10.1 Scope. This appendix establishes the requirement for wafer lot acceptance of microcircuit wafers intended for class level B and level S use. The performance of each wafer shall be evaluated individually and independently of the performance of other wafers in the lot. This wafer lot acceptance procedure is based on fabrication specification adherence (in accordance with appendix A of MIL-PRF-38535 and the manufacturer's documented fabrication procedures), physical testing, and electrical testing of suitable process monitors (PM's).

This method can be used only on a fabrication line that has Appendix A of MIL-PRF-38535 certification or control and has successfully instituted the required checks. Wafers failing any process specification (with the exception of acceptable rework instances) shall be removed from further processing.

This method is restricted to a well characterized and baselined process. By characterized, it is meant that a fabrication line has been adequately described in relation to the capabilities of the process. Baselined refers to the existence of a well defined process parameter target value with associated variances (based on characterization data) against which the actual wafer to wafer process data is measured to determine acceptability.

A collection of test structures which can provide the parametric data as well as additional yield indicators is referred to as a "process monitor" (PM). A statistically valid number of PM's shall be provided on each wafer. The PM may be either stepped onto every wafer in dedicated drop-in die locations, incorporated into kerf locations, or located on each die, such that they can be probed at the conclusion of processing up to and including final metallization and passivation (glassivation). Table I presents a minimum listing of structures which make up a PM. The manufacturer shall see PM parametric limits as called for by design rules and process rules, or both. Probe pads shall be designed to conform to the 2 x N (NIST) dimensions.

20. APPLICABLE DOCUMENTS. (This section is not applicable to this document.)

30. APPARATUS. Suitable electrical measurement equipment necessary to determine compliance with applicable acquisition documents and other apparatus as required in the referenced test methods.

40. PROCEDURE. There are three phases to wafer acceptance:

a. Processing to the manufacturer's fabrication baseline and documented fabrication procedures.

b. Visual/SEM inspection.

c. PM evaluation.

Wafers failing any test (with the exception of acceptable rework instances in accordance with appendix A of MIL-PRF-38535) shall be removed from the lot.

APPENDIX II

TABLE I. Minimum suggested set of structures used in a PM. 1/

N-channel transistors for measuring threshold voltages (minimum and maximum geometries)
P-channel transistors for measuring threshold voltages (minimum and maximum geometries)
Field threshold device(s)
Leakage current structures
Sheet resistance measurement structures
N-channel gain structures (KN)
P-channel gain structures (Kp)
Oxide breakdown structures (gates, intermetal, and field)
Contact chains (to be sufficient length to allow accurate measurement of the contact resistance typically found on a device, with diagnostic procedures to isolate failures)
Metal to poly
Metal 1 to metal 2 via resistance (where applicable)
Metal to diffusion
SEM step coverage checking structures for metal step coverage analysis
Alignment verniers
Functional circuits (e.g., ring oscillator, delay chains, etc.

1/ Appropriate structures for other technologies shall be developed.

APPENDIX II

40.1 Processing. Table II presents a minimum checkpoint list for wafer processing. If certain parameter values are proprietary, they may be presented in normalized or other specialized form.

TABLE II. In-process check points.

Process step	Inspection
Incoming material inspection	Water, wafers, chemicals, gasses
Photolithography	Spin speed, thickness, critical dimension measurements, alignment, post development visual inspection (100X)
Oxidation	Index of refraction, flatband, and threshold voltage shifts, thicknesses
Diffusion	Resistivity
Ion implant	Resistivity, range, species
Deposition	Thickness, resistivity, index of refraction
Etching	Critical dimension measurements, etch rates, end point detection
SEM	Step coverage (all metallization layers)

40.2 Visual/SEM inspection. Visual inspection of photo resist (PR) patterns, alignment verniers, and critical dimension measurements shall be made after each PR develop/bake operation. Following every etch and every ion implant, PR mask stripped wafers shall be inspected for proper PR removal, damage, or other defects, and defective wafers removed from the lot for scrap or for rework.

In-line nondestructive SEM inspection in accordance with MIL-STD-883, method 2018, shall be performed on each wafer lot. One wafer from each metallization level shall be randomly selected for inspection. SEM inspection for each level may be reduced to a weekly basis for each fabrication process when five consecutive lots pass inspection for the given level. If a metallization level fails the weekly inspection, then lot by lot inspection shall be required until five consecutive lots again pass. Wafers failing to meet the requirements of the test method shall be removed from processing. Wafer lot acceptance shall be in accordance with table IV herein.

APPENDIX II

40.3 PM evaluation. PM structures shall be submitted for approval. Wafer acceptance will be made on a wafer by wafer basis depending upon the information derived from PM room temperature testing in accordance with table III. If drop-in PM's are utilized, each wafer shall have at least 5 PM's; one shall be stepped in the center and the others in each of the quadrants. For kerf PM's and PM's on individual die, the five probed PM's shall be located in the center and in each of the quadrants. Quadrant PM's shall lie at least two-thirds of a radius away from the wafer center. Wafer acceptance will be governed by table III.

TABLE III. PM evaluation.

PM type	Number within PM specification limits	Less than 3 out of 5
Drop-in		Reject
Kerf		Reject
Each die		Reject

40.4 Lot acceptance. Acceptance requirements are as defined in table IV.

TABLE IV. Wafer lot acceptance requirements.

Requirement	Condition	Acceptance
Line certified	MIL-PRF-38535 Appendix A	Control to specification
Lot traveler check points	MIL-PRF-38535 Appendix A	100 percent in specification for lot acceptance
PM test data	Every wafer	75 percent of wafers in lot pass PM evaluation, otherwise reject.
Visual inspection	Every wafer	Wafer by wafer
SEM inspection	MIL-STD-883 Method 2018	Method 2018 criteria

APPENDIX II

40.5 Test results. When required by the applicable document, the following test results shall be made available for each lot submitted for qualification or quality conformance.

a. Results of each test conducted; initial and any resubmission.

b. Number of wafers rejected.

c. Failure analysis data and failure mode of each rejected SEC and the associated mechanism for catastrophic failures for each rejected device.

d. Number of reworked wafers and reason for rework.

e. Read and record data of PM electric parameter measurements.

40.6 Defective devices. All wafers that fail any test criteria shall be removed at the time of observation or immediately at the conclusion of the test in which the failure was observed. Once rejected and verified as a failure, no wafer may be retested for acceptance.

METHOD 5011.7

EVALUATION AND ACCEPTANCE PROCEDURES FOR POLYMERIC MATERIALS

1. PURPOSE. This method establishes the minimum inspection procedures and acceptance criteria for polymeric materials used in microcircuit applications. These materials shall be classified in two types as follows:

a. Type I being electrically conductive.

b. Type II being electrically insulative.

1.1 The user may elect to supplement Quality Conformance Inspection (QCI) test data or Qualification Testing data as a substitute where applicable for user Certification Testing.

2. APPARATUS. Suitable measurement equipment necessary to determine compliance with the requirements of the applicable acquisition document and other apparatus as required in the referenced test methods.

3. PROCEDURES.

3.1 Material acquisition specification. The microcircuit manufacturer shall prepare an acquisition specification describing the detailed electrical, mechanical, chemical, and thermal requirements for the polymeric material to be acquired. The requirements shall not be less than those imposed by this method, but may be increased to reflect the specific parameters of a particular material or the requirements of a particular application.

3.2 Certificate of compliance. The material supplier shall provide upon the users request a certificate of compliance for each polymeric material order. This certificate shall contain the actual test data for the supplier's testing as prescribed in this document.

3.3 Evaluation procedures. Evaluation procedures for polymeric materials shall be performed as specified in 3.4.1 through 3.5.13 for the type of material being tested.

3.4 Properties of uncured materials.

3.4.1 Materials. The components of a polymeric material and/or system shall be examined in accordance with table I and 3.8.1 and shall be uniform in consistency and free of lumps or foreign matter when examined in film, liquid or other acceptable form. Any filler shall remain uniformly dispersed and suspended during the required pot life (see 3.8.3). The electrically conductive fillers used in type I materials shall be gold, silver, alloys of gold or silver, or other precious metals.

3.4.1.1 Encapsulating compounds Encapsulating compounds are liquidous material and are to be tested in accordance with the requirements in Table I.

3.4.1.2 Molding compounds. Molding compounds as used in microelectronic devices are normally solidous material and are to be tested in accordance with MIL-PRF-38535, Appendix H Tables H-IB and H-IIB.

3.4.2 Viscosity. The viscosity of paste materials shall be determined in accordance with 3.8.2. The viscosity, including an acceptable range, shall be specified in the material acquisition document.

3.4.3 Pot life. The pot life when required shall be determined in accordance with 3.8.3 and shall be a minimum of 1 hour. The polymeric material shall be used within the pot life period after removal from the container, after mixing, or after thawing to room temperature in the case of premixed frozen polymers.

3.4.4 Shelf life. The shelf life, defined as the time that the polymeric material continues to meet the requirements of this specification shall be determined in accordance with 3.8.4. This shelf life shall be a minimum of 12 months at -40°C or below for one component system and a minimum of 12 months at room temperature (32°C maximum) for two component systems unless the supplier certifies for some other period of time. For class K devices, no polymeric material shall be used after the expiration date. Materials in class H devices may be requalified once, with acquiring activity and qualifying activity approval. Encapsulants shall have a minimum shelf life of 6 months.

TABLE I. Requirements

Test or Condition	Test Method Paragraph	Adhesives				α Absorbers				Film Dielectrics 1/				Particle Getters			
		Supplier		User		Supplier		User		Supplier		User		Supplier		User	
		A	C	A	C	A	C	A	C	A	C	A	C	A	C	A	C
Materials (3.4.1)	3.8.1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
Viscosity (3.4.2)	3.8.2	X	X			X	X			X	X						
Pot Life (3.4.3)	3.8.3	X	X			X	X			X	X						
Shelf Life (3.4.4)	3.8.4		X				X				X				X		
Thermogravimetric analysis (3.5.2)	3.8.5	X	X			X	X				X			X	X		
Outgassed materials (3.5.3)	3.8.6				X				X				X				X
Ionic impurities(3.5.4)	3.8.7	X	X			X	X				X				X		
Bond strength (3.5.5)	3.8.8	X 2/	X				X										
Coefficient of linear thermal expansion (3.5.6)	3.8.9		X														
Thermal conductivity (3.5.7)	3.8.10		X														
Volume resistivity (3.5.8)	3.8.11		X														
Type 1 materials		X 2/	X														
Type 2 materials			X			X	X			X	X						
Dielectric constant (3.5.9)	3.8.12		X								X						
Dissipation factor (3.5.10)	3.8.13		X								X						
Sequential test environment (3.5.11)	3.8.14				X				X				X				
Density (3.5.12)	3.8.15																
Mechanical integrity (3.5.13)	3.8.16																X
Operating life test (3.5.14)	3.8.17																X

A= Performed at acceptance testing.
C= Performed at certification testing.

1/ Film dielectrics are defined as polymeric materials that are used in film form to act as either interlayer dielectrics, passivation layers, and/or circuit support films.
2/ Required at 25ºC test condition only. No high temperature storage required.

TABLE I. Requirements (Continued)

Test or Condition	Test Method Paragraph	Dessicants				Junction Coatings				T-Wave Absorbers				Encapsulating Compounds			
		Supplier		User		Supplier		User		Supplier		User		Supplier		User	
		A	C	A	C	A	C	A	C	A	C	A	C	A	C	A	C
Materials (3.4.1)	3.8.1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
Viscosity (3.4.2)	3.8.2														X		
Pot Life (3.4.3)	3.8.3																
Shelf Life (3.4.4)	3.8.4		X				X								X		
Thermogravimetric analysis (3.5.2)	3.8.5	X	X			X	X								X		
Outgassed materials (3.5.3)	3.8.6				X				X				X				
Ionic impurities(3.5.4)	3.8.7	X	X				X							X	X		
Bond strength (3.5.5)	3.8.8													X	X		
Coefficient of linear thermal expansion (3.5.6)	3.8.9														X		
Thermal conductivity (3.5.7)	3.8.10														X		
Volume resistivity (3.5.8)	3.8.11														X		
Type 1 materials																	
Type 2 materials						X	X								X		
Dielectric constant (3.5.9)	3.8.12														X		
Dissipation factor (3.5.10)	3.8.13														X		
Sequential test environment (3.5.11)	3.8.14				X				X								
Density (3.5.12)	3.8.15									X	X	X	X				
Mechanical integrity (3.5.13)	3.8.16																
Operating life test (3.5.14)	3.8.17				X												X

A= Performed at acceptance testing.
C= Performed at certification testing.

3.5 Properties of cured polymer materials.

3.5.1 Curing of polymer materials. The material must be capable of meeting the requirements of this document when cured according to the supplier's instructions. The cure schedule for supplier tests shall be identical for all tests and shall be reported. The cure schedule for the user tests shall be the minimum cure schedule plus, as a minimum, the pre-seal bake specified in the user's assembly document and shall be reported. Deviation from the suppliers recommended cure schedule will require verification by the user of the materials performance.

3.5.2 Thermogravimetric analysis (TGA).

3.5.2.1 Thermal stability. The thermal stability of the cured material shall be determined in accordance with 3.8.5. Unless otherwise noted, the weight loss at 200°C shall be less than or equal to 1.0 percent of the cured material weight. Equivalent standard, i.e., "classical analytical techniques" are acceptable.

3.5.2.2 Filler content. Polymeric materials using a filler to promote properties such as electrical and thermal conductivity shall be tested in accordance with 3.8.5 to determine the inorganic filler content. For acceptance testing, the percent filler content shall not differ from the filler content in the certified materials by more than ±2 percent.

3.5.3 Outgassed materials. Outgassing of the cured material shall be determined in accordance with 3.8.6. Outgassed moisture, as determined in 3.8.6.1, shall be less than or equal to 5,000 ppmv (0.5 percent V/V) for 3 packages (0 failures) or 5 packages (1 failure). Other gaseous species present in quantities greater than or equal to 100 ppmv (0.01 percent V/V) shall be reported in ppmv or percent V/V. The data obtained in 3.8.6.2 shall also be reported in the same manner but for information only. The outgassing of the cured getter shall be determined in accordance with 3.8.6. The vapor content of the package with getter shall not exceed 2000 ppmv after 24 hours at 150°C and 3000 ppmv after 1000 hours at 150°C.

3.5.4 Ionic impurities. The ionic impurity content shall be determined in accordance with 3.8.7 and shall meet the requirements specified in table II. Ionic content analysis shall be in triplicate for certification and single analysis for acceptance testing. Failure at acceptance shall require the passing of two additional samples.

TABLE II. Ionic impurity requirements.

Total ionic content specific electrical conductance)	≤ 4.50 millisiemens/meter
Hydrogen (pH)	4.0 ≤ pH ≤ 9.0
Chloride	≤ 200 ppm
Sodium	≤ 50 ppm
Potassium	≤ 50 ppm
Flouride	≤ 50 ppm

Other ions present in quantities > 5 ppm shall be reported in ppm.

3.5.5 Bond strength. The bond strength of a polymeric material shall be determined in accordance with 3.8.8 at 25°C, and 25°C after 1,000 hours at 150°C. The bond strength shall meet as a minimum the 1.0X requirement specified in figure 2019-4 of method 2019 of MIL-STD-883 at each test condition. The manufacturer should test to shear or until twice the minimum 1.0X shear force is reached.

3.5.6 Coefficient of linear thermal expansion. The coefficient of linear thermal expansion shall be determined from -65°C to 150°C in accordance with 3.8.9. The coefficient of linear thermal expansion shall be ±10% of the value required in the users material specification or purchase order. This requirement shall apply to the material as it is configured for actual use. This requirement shall not apply to glass supported polymeric films.

3.5.7 Thermal conductivity. The thermal conductivity shall be determined at 121°C ±5°C in accordance with 3.8.10. The thermal conductivity shall be greater than or equal to 1.5 watt/meter-K for type I polymers and greater than or equal to .15 watt/meter-K for type II polymers.

3.5.8 Volume resistivity. The volume resistivity shall be determined in accordance with 3.8.11. The volume resistivity of conductive materials at 25°C, at 60°C, at 150°C, and at 25°C after 1,000 hours at 150°C shall be less than or equal to 5.0 microhm-meter for silver-filled polymers and less than or equal to 15.0 microhm-meter for gold-filled polymers. The volume resistivity of insulative materials shall be greater than or equal to 0.1 teraohm-meter at 25°C and greater than or equal to 1.0 megohm-meter at 125°C.

3.5.9 Dielectric constant. The dielectric constant of insulative polymeric materials shall be determined in accordance with 3.8.12 and shall be less than or equal to 6.0 at both 1 kHz and 1 MHz for this type of polymer but shall be less than or equal to 3.5 at 1 kHz and 1 MHz for materials used for dielectric layers.

3.5.10 Dissipation factor. The dissipation factor of insulative polymers shall be determined in accordance with 3.8.13 and shall be less than or equal to 0.03 at 1 kHz and less than or equal to 0.05 at 1 MHz.

3.5.11 Sequential test environment. The polymeric material shall withstand exposure to the test conditions specified in 3.8.14. After exposure to the complete sequence of environmental conditions, the test specimens shall show no evidence of mechanical degradation. For adhesives the measured bond strength of components shall meet as a minimum the 1.0X requirement specified on figure 2019-4 of method 2019 of MIL-STD-883.

3.5.12 Density. The density of microwave or RF absorbing materials shall be tested in accordance with 3.8.15. The acceptable value shall be that which is within ±10% of the value required on the user's material specification or purchase order.

3.5.13 Mechanical integrity. Particle getter integrity shall be verified after different levels of environmental stress.

3.5.13.1 Getter integrity (short term). When tested in accordance with 3.8.16.1 all samples shall pass the criteria for PIND as defined in MIL-STD-883 method 2020.

3.5.13.2 Getter integrity (long term). When tested in accordance with 3.8.16.2 all samples shall pass the criteria for PIND as defined in MIL-STD-883, method 2020, both initially and after storage at 150°C for 1,000 hours. The salted particles shall remain attached to the getter material in the original position with no attachment and reattachment when viewed at 30X to 60X magnification.

3.5.13.3 Getter integrity (vibration). When tested in accordance with 3.8.16.3 the sample shall pass PIND as defined in MIL-STD-883, method 2020, the salted particles shall remain attached to the getter material in the original position, with no detachment and re-attachment when viewed at 30X to 60X.

3.5.14 Operating life. When tested in accordance with 3.8.17, the comparison between initial and post test electrical data shall not indicate parametric shifts, which are unique to the test group containing getter material.

3.6 Responsibility for testing. The manufacturer and user are responsible for the performance of all tests as specified in table I herein.

NOTE: The Government reserves the right to perform any of the inspections set forth in the specification where such inspections are deemed necessary to assure that supplies and services conform to prescribed requirements.

3.6.1 Test equipment and testing facilities. Test and measuring equipment and testing facilities of sufficient accuracy, quality and quantity to permit performance of the required testing shall be established and maintained by the manufacturer and user. The establishment and maintenance of a calibration system to control the accuracy of the measuring and test equipment shall be in accordance with ANSI/NCSL Z540.3 or similar specification approved by the qualifying activity. The supplier and user may utilize a commercial laboratory acceptable to the qualifying activity for performing the required certification and acceptance testing.

3.6.2 Testing conditions. Unless otherwise specified herein, all testing shall be performed in accordance with the test conditions specified in the "general requirements" of the MIL-STD-883.

3.7 Classification of testing. The test requirements specified herein are classified as certification testing and acceptance testing.

3.7.1 Certification testing. Certification testing shall be performed on the initial lot of material and for any major changes to the material thereafter and consist of all tests to determine conformance with all requirements specified herein. To insure that both the polymeric material and the processes employing the material are controlled, both the supplier and the user of the material shall be responsible for performance of the tests as designated in table I.

3.7.1.1 Sample size. The number of samples to be subjected to each testing procedure shall be as specified in the individual test methods.

3.7.1.2 Failures. Failure of any polymeric material to meet the testing requirements shall be cause for refusal to grant certification approval.

3.7.1.3 Retention of data. The data generated for certification shall be retained for a period of 5 years or until a recertification is performed, whichever is greater.

3.7.2 Acceptance testing. Acceptance tests shall be performed on each lot and shall consist of tests as specified in table I.

3.7.2.1 Test lot. A test lot shall consist of all polymeric material manufactured under the same batch number, i.e., a batch number identifies those materials whose constituents can be traced to a single lot of raw materials.

3.7.2.2 Sample size. The number of samples to be subjected to each testing procedure shall be as specified in the individual test methods.

3.7.2.3 Failures. Failure of the samples to meet the testing requirements of a specific test shall be cause for rejection of the lot.

3.7.2.4 Retention of data. The data generated for acceptance testing shall be retained for a period of 5 years.

3.8 Methods of examination and test. The following test criteria and analytical protocols shall be documented and approved by the qualifying activity prior to material certification.

3.8.1 Materials. The polymeric components or system or both shall be examined visually at a minimum magnification of 30X to ensure conformance with the requirements of 3.4.1.

3.8.2 Viscosity. The material user and supplier shall define a mutually acceptable method for verifying the viscosity of fluid or paste materials. The supplier shall use the same method in performing the required certification and acceptance testing.

3.8.3 Pot life. The parameters to be used in the measurement of pot life (e.g., viscosity change, skin-over, loss of bond strength, etc.) are generally material dependent. The material supplier and user shall select the procedure to be used in establishing and testing the pot life.

3.8.4 Shelf life. Where applicable, an unopened container of material shall be stored under the condition specified in 3.4.4. As a minimum, the test methods and requirements specified in table III shall be used to establish the shelf life.

TABLE III. Shelf Life Determination.

Property	Requirement	Test method	Application/condition
Materials	3.4.1	3.8.1	All polymeric materials
Pot life	3.4.3	3.8.3	Adhesives; α Absorbers; Junction coatings; Dielectrics
Bond strength	3.5.5	3.8.8	Adhesives; α Absorbers; Junction coatings; 25°C only
Volume resistivity 1/	3.5.8	3.8.11	Adhesives, type I, 25°C only

1/ To be determined for materials where electrical conductivity is a design parameter.

3.8.5 Thermogravimetric analysis (TGA). The thermal stability of the polymeric system and it's filler content (if any) shall be determined by testing samples of the cured system (see 3.5.1) in nitrogen using suitable TGA equipment or in accordance with ASTM D3850. Single point analyses are acceptable, however if the first sample fails, then two additional analyses must be performed. The average value of the three samples must then meet or exceed the minimum requirements.

3.8.5.1 Thermal stability. The thermal stability of the polymeric material shall be determined by heating the specimens from room temperature to not less than 210°C, at a heating rate between 10°C/minute and 20°C/minute, in a nitrogen atmosphere with 20-30 milliliter/minute nitrogen flow. The weight loss at 200°C shall be determined.

3.8.5.2 Filler content. The filler content of polymeric materials using a filler to promote properties such as electrical or thermal conductivity shall be determined by heating the specimen from room temperature to 600°C, at a heating rate between 10°C/minute and 20°C/minute, in an air atmosphere with 20-30 milliliter/minute air flow. The temperature shall be maintained at 600°C until constant weight is obtained. It is permitted to perform 3.8.5.1, followed by heating from 210°C to 600°C as detailed above. The filler content shall be reported as weight percent of the cured specimen.

3.8.6 Outgassed materials. Ten test specimens shall be prepared using gold- or nickel-plated Kovar or ceramic packages, (dielectric materials may be prepared using aluminum coated silicon as the substrate). (The use of "leadless" packages is permitted to reduce moisture contributions due to package construction). The material shall be cured using the minimum cure schedule and shall receive the minimum pre-seal bake specified in the assembly document(s) (see 3.5.1). After a pre-seal bake, the packages shall be hermetically sealed. Only those packages that meet the fine and gross leak test requirements of test method 1014 shall be submitted for moisture content analysis. If less than 10 test specimens remain after hermetically testing, the failed packages shall be replaced by additional hermetical packages processed and tested in the same manner as the original group.

3.8.6.1 Testing for short term outgassing of moisture and other gaseous species. Five packages containing polymer prepared in accordance with 3.8.6 shall be heated in accordance with MIL-STD-883, method 1008, 24 hours at 150°C. The packages shall then be immediately (less than or equal to 5 minutes) inserted into the ambient gas analysis apparatus. The packages shall be subjected to ambient gas analysis in accordance with MIL-STD-883, method 1018, procedure 1. In addition to moisture, other gaseous species present in quantities greater than or equal to 100 ppmv (0.01 percent V/V) shall be reported in ppmv or percent V/V. This test shall meet the requirements of 3.5.3.

NOTE: From the 5 packages prepared in accordance with MIL-STD-883, method 1008, only 3 packages are required to be subjected to the ambient gas analysis testing and the pass criteria of 3 packages (0 failures) shall apply (see 3.5.3). However, in the event of a failure, the testing of the remaining 2 packages shall be required in order to pass with the criteria of 5 packages (1 failure).

All polymeric materials tested shall have quantities of material equivalent in mass and exposed surface area to that of the intended application. Gold plated Kovar tabs and alumina blanks may be used as facsimile device elements. Several polymeric materials of different application may be tested in combination with each other in this test, however their combined moisture content shall not exceed 5,000 ppmv.

3.8.6.2 Testing for long term outgassing of moisture and other gaseous species. Provided that the moisture requirement of 3.5.3 has been met by packages tested in 3.8.6.1, the remaining five devices containing polymer from the group prepared in accordance with 3.8.6 shall be heated in accordance with MIL-STD-883, method 1008 for 1,000 hours at 150°C. The packages shall then be immediately (less than or equal to 5 minutes) inserted into the ambient gas analysis apparatus. The packages shall be subjected to ambient gas analysis in accordance with MIL-STD-883, method 1018, procedure 1. In addition to moisture, other gaseous species present in quantities greater than or equal to 100 ppmv (0.01 percent V/V) shall be reported in ppmv or percent V/V.

3.8.7 Ionic impurities. A water-extract analysis shall be performed to determine the level of ionic contamination in the cured polymeric material. The total ion content (specific electrical conductance) and the specific ionic content for the hydrogen (pH), chloride, sodium, fluoride and potassium ions shall be measured. Other ions present in quantities > 5 ppm shall also be reported in ppm. The methods of analysis submitted in the following paragraphs are suggested techniques. Alternate methods of analysis may be selected where it can be shown that the techniques are equivalent and the method of analysis is approved by the qualifying activity.

3.8.7.1 Sample preparation. Adequate material shall be cured to obtain 3 gram samples of polymer following grinding, for final preparation. The material shall be cured on teflon or other inert surface in a forced draft oven. When possible the cured specimen shall be removed from the curing substrate and ground to 60-100 mesh particles; polymeric film samples less than or equal to 0.025 cm thick shall be cured and cut into less than or equal to 0.25 cm^2 samples; gels or low modulus materials may be cast directly into the flat bottom of the sample flask for the extraction. Smaller sample sizes may be selected where it can be shown that the accuracy of the test method has not changed.

3.8.7.2 Extraction procedure. 3 grams (equivalent resin) of the ground or cut equivalent polymer shall be added to a cleaned; tarred, 250-ml flasks made of pyrex, or equivalent. The weight of the cured material in each flask shall be recorded to the nearest milligram. 150.0 grams of deionized water with a measured specific conductance less than or equal to 0.1 millisiemens/meter (specific resistivity greater than or equal to 1.0 megohm-centimeter) shall be added to the flask. A blank shall be prepared by adding 150.0 grams of the deionized water and a boiling chip to a second 250-ml flask. The flasks shall be refluxed for 20 hours.

NOTE: 1.0 mho = 1.0 siemens; 1.0 mho/cm = 100.0 siemens/meter.

3.8.7.3 Measurement of ionic content.

3.8.7.3.1 Total ionic content. The total extractable ionic content shall be determined by measuring the specific electrical conductance of the water-extract samples and the blank using a conductivity meter with an immersion conductivity cell having a cell constant of 0.01/centimeter (alternatively 0.1 cm^{-1} to adjust for proper analysis of the solution). The total ionic content, in millisiemens/meter, shall be obtained by subtracting the specific conductance of the blank from the specific conductance of the samples.

3.8.7.3.2 Hydrogen ion content (pH). The pH of the water extract shall be determined using a pH meter with a standard combination electrode.

3.8.7.3.3 Specific ion analysis. Specific ion analysis of the water extract shall be conducted using ion chromatography or a demonstrated equivalent. The ion concentrations in the extract shall be converted to the sample extractable concentrations by multiplying the ratio of the deionized water weight (W) to polymer sample weight (S); that is, by (W/S). The chloride, sodium, fluoride and potassium ion levels and all other ions detected in quantities > 5 ppm shall be reported in ppm.

3.8.8 Bond strength. The bond strength of the polymeric material shall be determined in accordance with 3.8.8.1, 3.8.8.2 or 3.8.8.3 below. As a minimum, five elements shall be tested to failure at the following conditions:

a. At 25°C.

b. At 25°C after 1,000 hours at 150°C in an air or nitrogen ambient.

The average bond strength at each test condition shall be determined in kilograms (force).

3.8.8.1 Bond strength. The bond strength shall be determined in accordance with method 2019 of MIL-STD-883. A gold-metallized substrate or a gold- or nickel-plated package shall be used as the bonding surface for bond strength testing.

3.8.8.1.1 Type I materials. Suppliers shall use 0.08 inch-square (0.2 centimeter-square) gold-plated Kovar tabs.

3.8.8.1.2 Type II materials. Suppliers shall use 0.08 inch-square (0.2 centimeter-square) alumina chips.

3.8.8.2 Bond strength. The bond strength may be determined in accordance with ASTM D1002 as an alternative to test method 2019. If ASTM D1002 is used, the results must be correlated to assure that the bond strength of the adhesive is shown to be equivalent to the Method 2019 failure criteria.

3.8.8.3 Molding compounds or encapsulants. Molding compounds or encapsulants shall be tested in accordance with MIL-STD-883, test method 1034.

3.8.9 Coefficient of linear thermal expansion. The coefficient of linear thermal expansion shall be determined in accordance with ASTM E831 over the temperature range of -65°C to 150°C. The glass transition temperature, coefficients, and temperature ranges corresponding to different slopes of the curve shall be noted.

3.8.10 Thermal conductivity. The thermal conductivity, in watt/meter-K, shall be determined at 121°C ±5°C in accordance with ASTM C177 or ASTM C518.

NOTE: 1 cal/cm-s-k = 418.4 W/m-K.

3.8.11 Volume resistivity.

3.8.11.1 Type I polymers.

3.8.11.1.1 Paste materials. Test specimens shall be prepared using a standard 1 inch x 3 inch glass slide. A jig capable of holding this slide, with two scribed lines 100 mil apart and parallel to the length, shall be the guide for applying two strips of transparent tape. There shall be no wrinkles or bubbles in the tape. The slide shall be cleaned with alcohol and air dried. A drop of the type I material shall be placed between the two strips of tape. Using a single edge razor blade maintaining a 30° angle between the slide surface and the razor blade, the material shall be squeezed between the tape strips. The length of the applied strip shall be at least 2.5 inches. The tape shall be removed, and the material shall be cured according to 3.5.1. After cure, the test specimens shall be allowed to cool to room temperature.

3.8.11.1.2 Film materials. Test specimens shall be prepared using a standard 1 inch x 3 inch glass slide. The slide shall be cleaned with alcohol and air dried. A thin strip of the uncured film approximately 100 mil wide and at least 2.5 inches long shall be placed on the glass slide. The film shall be covered with a strip of copper foil or Teflon film and a second 1 inch x 3 inch glass slide shall be placed over the foil or Teflon film. Sufficient force (weight, clip, etc.), shall be applied to the assembly to compress the material during cure. The material shall be cured according to 3.5.1. After cure, the test specimen shall be allowed to cool to room temperature, and the top slide and foil or Teflon shall be removed. The exact width and thickness of each polymer strip shall be measured with a precision caliper and micrometer respectively. These measurements, after conversion to the appropriate units, shall be used to calculate the volume resistivity using the formula given in 3.8.11.1.3.

3.8.11.1.3 Resistance measurements. Resistance measurements shall be made using a milliohm meter in conjunction with a special four-point probe test fixture. (This fixture can be made of an acrylic material with four spring-loaded contacts. The contacts must be set into the acrylic so that the current contacts are 2 inches apart, the voltage contacts are between the two current contacts, and the voltage contacts are separated from each current contact by 0.5 inch.) The four-point probe fixture shall be placed on the strip of conductive polymer and contact between each probe and the material shall be ensured. The measured resistance shall be recorded in ohms, and the resistivity shall be determined from the following formula:

$$P = \frac{R\,(w\,x\,t)}{l}$$

Where:

P = resistivity, ohm-m

R = measured resistance, ohms

w = width, (100 mil = 2.54 mm)

t = thickness, (micrometer reading of the material plus glass side) minus (micrometer reading of the glass slide)

l = length between inner pair of probes, (1 inch = 25.4 mm)

A minimum of three specimens shall be tested at 25°C, at 60°C, at 150°C, and at 25°C after 1,000 hours at 150°C in an air or nitrogen ambient. The same specimens may be used for each test.

3.8.11.2 Type II polymer materials. Type II materials shall be tested in accordance with ASTM D257 at temperatures of 25°C and 125°C.

3.8.12 Dielectric constant. The dielectric constant of type II materials shall be determined as required in the user's material specification in accordance with ASTM D150 at frequencies of 1 kHz and 1 MHz at room temperature.

3.8.13 Dissipation factor. The dissipation factor of type II materials shall be determined as required in the user's material specification in accordance with ASTM D150 at frequencies of 1 kHz and 1 MHz at room temperature.

3.8.14 Sequential test environment. Testing shall be performed using either 3.8.14.1 or 3.8.14.2.

3.8.14.1 Sequential test environment. A minimum of five test specimens shall be subjected to the environmental conditions specified below. Specimens shall be prepared using the largest component/substrate/package combinations representative of end-use applications in backing material, attach surface, and size. Component types include resistor, capacitor, integrated circuit, and discrete semiconductor elements. Two components of each type shall be attached to the substrate with the adhesive (type I or II) proposed for use with that component type. The test specimens shall be subjected to the following environmental conditions in the sequence given:

a. Thermal shock (MIL-STD-883, method 1011, condition C, 15 cycles).

b. Temperature cycling (MIL-STD-883, method 1010, condition C, 100 cycles).

c. Mechanical shock (MIL-STD-883, method 2002, condition B, Y1 only).

d. Variable frequency vibration (MIL-STD-883, method 2007, condition A, Y1 only).

e. Constant acceleration (MIL-STD-883, method 2001, condition B, Y1 only).

3.8.14.2 Alternate sequential testing. Alternatively, testing in accordance with Qualification Testing (QML sequences in accordance with MIL-PRF-38534, using maximum baseline limits may be performed. The user is still required to satisfy the requirements of 3.8.14.1 by completing the necessary supplemental testing, i.e., thermal shock and vibration.

Following the environmental exposures of 3.8.14.1 or 3.8.14.2, the test specimens shall be examined for possible degradation in accordance with MIL-STD-883, method 2017. For adhesives, one of each type of component from each sample shall be evaluated for die shear strength in accordance with MIL-STD-883, method 2019 and shall meet the strength requirements of figure 2019-4.

3.8.15 Density. The density of materials used as RF or microwave absorbers shall be determine in accordance with principles outlined in ASTM D 3574, paragraphs 9-14. Those RF absorbers that are foamed in-place are to be foamed, cured, and cut to form the free standing material for this analysis.

3.8.16 Mechanical integrity.

3.8.16.1 Getter integrity - short term. Samples shall be prepared using hermetically sealed packages representative of the maximum size and type which will incorporate the use of getter material. These samples will contain only "salted" particles and getter material. The getter material shall be applied to the package in the location and approximate volume as specified for a normal production part. The getter material coverage area shall be measured and recorded. The particles to be salted shall consist of the following unless otherwise agreed upon by the user and the qualifying activity.

(1) Solder balls: 3-6 mils in diameter - 2 pieces required.

(2) Aluminum ribbon: Approximate dimensions of 2 mil thick by 5 mil wide by 10 mils long - 1 required. A piece of aluminum wire 2-6 mils in diameter may be substituted for the ribbon.

(3) Gold wire: 1 mil diameter by 15-20 mils in length - 1 piece required. Getter material application and cure shall take place in the sequence normally followed for production parts. The samples shall be processed through the same environmental conditioning steps as a qualified production part. The samples shall be subjected to PIND test in accordance with MIL-STD-883, method 2020, condition A or B, which shall be repeated three time for a total of four cycles to verify the integrity of the getter material. During all PIND testing the samples shall be mounted on the tester such that the shock pulses integral with the test shall be in the direction most likely to dislodge the particles from the getter material. A minimum of three samples shall be evaluated and all shall pass the defined PIND criteria.

3.8.16.2 Getter integrity - long term. All of the conditions and requirements of 3.8.16.1 apply, except that the samples either newly prepared or as received from the short term test, shall be stored at 150°C for 1,000 hours.

The samples shall then be subjected to mechanical shock in accordance with MIL-STD-883, method 2002, condition B, in the Y_2 direction. Following mechanical shock the samples shall be PIND tested as specified above.

Following PIND, the samples shall be delidded and a visual inspection shall be performed to verify the following:

a. Determine if particles have separated from the getter material or have fallen into the package.

b. Determine if getter coverage has spread or bled out.

c. Check for any evidence of peeling from inside and/or getter becoming separated from package.

3.8.16.3 Vibration. Samples shall be prepared as in 3.8.16.1 except that the lid shall be attached in such a manner that it may be removed for visual inspection. After particle salting and immobilization as in 3.8.16.1, visual inspection shall be done to verify entrapment of the salted particles. Location of the particles in the getter material shall be recorded for future reference.

The lid shall then be reattached to the package securely enough to withstand the testing that follows. After PIND testing in accordance with MIL-STD-883, method 2020, the samples shall be subjected to vibration in accordance with MIL-STD-883, method 2007, condition A or B. At the end of this test, the lids shall be removed from the package by whatever method is required. Location of the "salted" particles in the getter material shall be noted and compared with the location prior to vibration. Particles other than the original "salted" particles shall be ignored. A minimum of three samples shall be submitted for evaluation and all shall pass the defined PIND criteria initially and after vibration.

3.8.17 Operating life test. Ten electrically functioning samples shall be fabricated using hermetically sealed devices which have been processed through the same steps as a normally qualified production part as specified by the user's assembly drawing. If agreed upon by the user and the qualifying activity, standard evaluation circuits may be substituted. All the samples shall meet the PIND test requirements in accordance with MIL-STD-883, method 2020, condition A or B. The samples shall be subjected to the life test in accordance with MIL-STD-883, method 1005, condition A, for 1,000 hours at 125°C. Electrical parameters shall be measured and recorded for the units initially and at the completion of the life test. Data taken from the samples shall be reviewed for evidence of device degradation due to the presence of getter material.

NOTE: Qualification test data may be used to satisfy this requirement with qualifying activity approval.

3.9 Test deviation. Additional, reduced or alternate testing, as may be dictated by the uniqueness of particular material and manufacturing construction techniques can be required or authorized by the qualifying activity provided the manufacturer submits data to support test deviation.

4. SUMMARY. As a minimum, acquisition documents shall specify the following information:

a. Title, number, and revision letter of acquisition specification.

b. Size and number of containers required.

c. Manufacturer's product designation.

d. Request for test data.

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METHOD 5012.1

FAULT COVERAGE MEASUREMENT FOR DIGITAL MICROCIRCUITS

1. PURPOSE. This test procedure specifies the methods by which fault coverage is reported for a test program applied to a microcircuit herein referred to as the device under test (DUT). This procedure describes requirements governing the development of the logic model of the DUT, the assumed fault model and fault universe, fault classing, fault simulation, and fault coverage reporting. This procedure provides a consistent means of reporting fault coverage regardless of the specific logic and fault simulator used. Three procedures for fault simulation are described in this procedure: Full fault simulation and two fault sampling procedures. The applicable acquisition document shall specify a minimum required level of fault coverage and, optionally, specify the procedure to be used to determine the fault coverage. A fault simulation report shall be provided that states the fault coverage obtained, as well as documenting assumptions, approximations, and procedures used. Where any technique detailed in this procedure is inapplicable to some aspect of the logic model, or inconsistent with the functionality of the available fault simulator and simulation postprocessing tools, it is sufficient that the user of this procedure employ an equivalent or comparable technique and note the discrepancy in the fault simulation report. Microcircuits may be tested by nontraditional methods of control or observation, such as power supply current monitoring or the addition of test points that are available by means of special test modes. Fault coverage based on such techniques shall be considered valid if substantiating analysis or references are provided in the fault simulation report.

1.1 Terms. Terms and abbreviations not defined elsewhere in the text of this test procedure are defined in this section.

a. Automatic test equipment (ATE). The apparatus with which the actual DUT will be tested. ATE includes the ability to apply a test vector sequence (see 1.1l).

b. Broadside application. A method of applying a test vector sequence where input stimuli change only at the beginning of a simulation cycle or ATE cycle and all changes on primary inputs of the DUT are assumed to be simultaneous. Nonbroadside application occurs when test vectors are conditioned by additional timing information such as delay (with respect to other primary inputs), return-to-zero, return-to-one, and surround-by- complement.

c. Detection. An error at an observable primary output of a logic model caused by the existence of a logic fault. A hard detection is where an observable output value in the fault-free logic model is distinctly different from the corresponding output value in the faulty logic model. An example of a hard detection is where the fault-free logic model's output value is 0 and the faulty logic model's output value is 1, or where the fault-free logic model's output value is 1 and the faulty logic model's output value is 0. If the high-impedance state (Z) can be sensed by the ATE, then a hard detection can involve the Z state as well. A potential detection is an error where the fault-free output is 0 or 1 and the faulty output value is unknown (X), or Z if Z cannot be sensed by the ATE.

d. Established test algorithm. An algorithm, procedure, or test vector sequence, that when applied to a logic component or logic partition has a known fault coverage or test effectiveness. This fault coverage or test effectiveness is denoted herein as the established fault coverage or established test effectiveness for the established test algorithm. For example, an established test algorithm for a RAM may be a published memory test algorithm, such as GALPAT, that has been shown by experience to detect essentially all RAM failures and therefore is assessed an established test effectiveness of 100 percent. An ALU may be tested by means of a precomputed test vector sequence for which fault coverage has been previously determined. More than one established test algorithm may exist for a logic component or logic partition, each with a different established fault coverage or test effectiveness.

e. Failure hierarchy: Failure mechanism, physical failure, logical fault, error. The failure hierarchy relates physical defects and their causes to fault simulators and observable effects. A failure mechanism is the actual cause of physical failure; an example is electromigration of aluminum in a microcircuit. A physical failure (or simply failure) is the actual physical defect caused by a failure mechanism; an example is an open metal line. A logical fault (or simply fault) is a logical abstraction of the immediate effect of a failure; an example is "stuck- at-one" behavior of a logic gate input in the presence of an open metal line. An error is a difference between the behavior of a fault-free and faulty DUT at one or more observable primary outputs of the DUT.

f. Fault coverage. For a logic model of a DUT, a fault universe for the logic model of the DUT, and a given test vector sequence, fault coverage is the fraction obtained by dividing the number of faults contained in the fault universe that are detected by the test vector sequence by the total number of faults contained in the fault universe. Fault coverage is also stated as a percentage. In this test procedure, fault coverage is understood to be based on the detectable fault equivalence classes (see 3.3). Rounding of fault coverage fractions or percentages shall be "toward zero," not "to nearest." For example, if 9,499 faults are detected out of 10,000 faults simulated, the fault coverage is 94.99 percent; if this value is to be rounded to two significant digits, the result shall be reported as 94 percent, not 95 percent.

g. Logic line, node. Logic lines are the connections between components in a logic model, through which logic signals flow. Logic lines are the idealized "wires" in a logic model. A set of connected logic lines is a node.

h. Logic: Combinational and sequential. Combinational digital logic contains only components that do not possess memory, and in which there are no feedback paths. Sequential digital logic contains at least one component that contains memory, or at least one feedback path, or both. For example, a flip-flop is a component that contains memory, and cross-coupled logic gates introduce feedback paths.

i. Macro. A logic modeling convention representing a model contained within another model. A macro boundary does not necessarily imply the existence of a physical boundary in the logic model. A main model is a logic model that is not contained within a larger model. Macros may be nested (that is, a macro may contain submacros).

j. Primary inputs, primary outputs. Primary inputs to a logic model represent the logic lines of a DUT that are driven by the ATE's drivers and thus are directly controllable test points. Primary outputs from a logic model represent the logic lines of the DUT that are sensed by the ATE's comparators and thus are directly observable test points. The inputs to the "main model" of the logic model of the DUT are the primary inputs, and the outputs from the main model are the primary outputs. Internal nodes that can be driven or sensed by means of special test modes shall be considered to be control or observation test points.

k. Test effectiveness. A measure similar to fault coverage, but used in lieu of fault coverage in cases where physical failures cannot be modeled accurately as logical faults. For example, many RAM and PLA failures cannot be idealized conveniently in the same way as gate-level failures. However, established test algorithms may be used to detect essentially all likely physical failures in such structures.

l. Test vector sequence. The (ordered) sequence of stimuli (applied to a logic model of a DUT) or stimulus/response values (applied to, and compared for, the actual DUT by the ATE).

m. Undetectable and detectable faults. An undetectable fault is defined herein as a logical fault for which no test vector sequence exists that can cause at least one hard detection or potential detection (see 1.1c). Otherwise (that is, some test vector sequence exists that causes at least one hard detection, or potential detection, or both), the fault is defined herein to be a detectable fault (see 3.3.3).

2. APPARATUS.

2.1 Logic simulator. Implementation of this test procedure requires the use of a facility capable of simulating the behavior of fault-free digital logic in response to a test vector sequence; this capability is herein referred to as logic simulation.

In order to simulate sequential digital logic, the simulator must support simulation of a minimum of four logic states: zero (0), one (1), high-impedance (Z), and unknown (X). In order to simulate combinational digital logic only, the simulator must support simulation of a minimum of two logic states: 0 and 1.

At the start of logic simulation of a logic model of a DUT containing sequential logic, the state of every logic line and component containing memory shall be X; any other initial condition, including explicit initialization of any line or memory element to 0 or 1, shall be documented and justified in the fault simulation report.

In order to simulate wired connections or bus structures, the simulator must be capable of resolving signal conflicts introduced by such structures. Otherwise, modeling workarounds shall be permitted to eliminate such structures from the logic model (see 3.1.2).

In order to simulate sequential digital logic, the simulator must support event- directed simulation. As a minimum, unit-delay logic components must be supported.

Simulation of combinational-only logic, or simulation of sequential logic in special cases (such as combinational logic extracted from a scannable sequential logic model) can be based on nonevent-directed simulation, such as levelized, zero-delay, or compiled-code methods. The fault simulation report shall describe why the selected method is equivalent to the more general event-directed method.

2.2 Fault simulator. In addition to the capability to simulate the fault-free digital logic, the capability is also required to simulate the effect of single, permanent, stuck-at-zero and stuck-at-one faults on the behavior of the logic; this capability is herein referred to as fault simulation. Fault simulation shall reflect the limitations of the target ATE (see 3.4.1). It is not necessary that the fault simulator directly support the requirements of this test procedure in the areas of hard versus potential detections, fault universe selection, and fault classing. However, the capability must exist, at least indirectly, to report fault coverage in accordance with this procedure. Where approximations arise (for example, where fault classing compensates for a different method of fault universe selection) such differences shall be documented in the fault simulation report, and it shall be shown that the approximations do not increase the fault coverage obtained.

3. PROCEDURE.

3.1 Logic model.

3.1.1 Level of modeling. The DUT shall be described in terms of a logic model composed of components and connections between components. Primary inputs to the logic model are assumed to be outputs of an imaginary component (representing the ATE's drivers), and primary outputs of the logic model are assumed to be inputs to an imaginary component (representing the ATE's comparators). Some logic simulators require that the ATE drivers and comparators be modeled explicitly; however, these components shall not be considered to be part of the logic model of the DUT.

3.1.2 Logic lines and nodes (see 1.1g). All fan-out from a node in a logic model is ideal, that is, fan-out branches associated with a node emanate from a single point driven by a fan-out origin. All fan-in to a node in a logic model is ideal; that is, multiple fan-in branches in a node drive a single line. Figure 1 shows a node that includes fan-in branches, a fan-out origin, and fan-out branches. Because fan-in and fan-out generally are not ideal in actual circuit layout, the actual topology of the circuit should be modeled, if it is known, by appropriately adding single-input noninverting buffers to the logic model. Modeling workarounds may be used to eliminate fan-in to a node. This may be required if the simulator does not directly model wired connections or bus structures. Some simulators may permit internal fan-in, but require that bidirectional pins to a DUT be modeled as separate input and output functions.

3.1.3 G-logic and B-logic partitions. Simple components of the logic model (logic primitives such as AND, OR, NAND, NOR, XOR, buffers, or flip-flops; generally the indivisible primitives understood by a simulator) are herein referred to as gate logic (G-logic). Complex components of the logic model (such as RAM, ROM, or PLA primitive components, and behavioral models - relatively complex functions that are treated as "black boxes" for the purpose of fault simulation) are referred to herein as block logic (B-logic).

For the purpose of fault simulation, the logic model shall be divided into nonoverlapping logic partitions; however, the entire logic model may consist of a single logic partition. The logic partitions contain components and their associated lines; although lines may span partitions, no component is contained in more than one partition. A G-logic partition contains only G-logic; any other logic partition is a B-logic partition.

A logic partition consisting of G-logic, or B-logic, or G-logic and B-logic that, as a unit, is testable using an established testing algorithm, with known fault coverage or test effectiveness, may be treated as a single B-logic partition.

3.1.4 Model hierarchy. The logic model may be hierarchical (that is, consisting of macro building blocks), or flat (that is, a single level of hierarchy with no macro building blocks). Hierarchy does not impose structures on lines; for example, there is no implied fan-out origin at a macro input or output. Macros that correspond to physical partitions in a model shall use additional buffers (or an equivalent method) to enforce adherence to the actual DUT's fan-out.

3.1.5 Fractions of transistors. The fraction of transistors comprising each G-logic and B-logic partition, with respect to the total count of transistors in the DUT, shall be determined or closely estimated; the total sum of the transistor fractions shall equal 1. Where the actual transistor counts are not available, estimates may be made on the basis of gate counts or microcircuit area; the assumptions and calculations supporting such estimates shall be documented in the fault simulation report. The transistor fractions shall be used in order to weight the fault coverage measured for each individual logic partition (see 3.5).

3.2 Fault model.

3.2.1 G-logic. The fault model for G-logic shall be permanent stuck-at-zero and stuck-at-one faults on logic lines. Only single stuck-at faults are considered in calculating fault coverage.

3.2.2 B-logic. No explicit fault model is assumed for B-logic components. However, an established test algorithm shall be applied to each B-logic component or logic partition. If a B-logic partition contains logic lines or G-logic components, or both, justification shall be provided in the fault simulation report as to how the established test algorithm that is applied to the B-logic partition detects faults associated with the logic lines and G-logic components.

3.2.2.1 Built-in self-test. A special case of B-logic is a partition that includes a linear-feedback shift register (LFSR) that performs signature analysis for compression of output error data. Table I lists penalty values for different LFSR degrees. If the LFSR implements a primitive GF(2) polynomial of degree "k", where there is at least one flip-flop stage between inputs to a multiple-input LFSR, then the following procedure shall be used in order to determine a lower bound on the established fault coverage of the logic partition:

Step 1: Excluding the LFSR, but including any stimulus generation logic considered to be part of the logic partition, determine the fault coverage of the logic partition by fault simulation without signature analysis; denote this fault coverage by C.

Step 2: Reference table I. For a given degree "k" obtain the penalty value "p". The established fault coverage of the logic partition using a LFSR of degree "k" shall be reported as (1-p)C. That is, a penalty of (100p) percent is incurred in assessing the effectiveness of signature analysis if the actual effectiveness is not determined.

3.3 Fault universe selection and fault equivalence classing. Fault coverage shall be reported in terms of equivalence classes of the detectable faults. This section describes the selection of the initial fault universe, the partitioning or collapsing of the initial fault universe into fault equivalence classes, and the removal of undetectable faults in order to form the detectable fault universe. These three stages constitute the fault simulation reporting requirements; however, it is generally more efficient to obtain the set of faults that represent the fault equivalence classes directly without explicitly generating the initial fault universe.

3.3.1 Initial fault universe. The initial fault universe shall consist of single, permanent, stuck-at-zero and stuck-at-one faults on every logic line (not simply on every logic node) in the G-logic partitions of the logic model. A bus, which is a node with multiple driving lines, shall be considered, for the purpose of fault universe generation, to be a multiple-input, single-output logic gate. The initial fault universe shall include stuck-at-zero and stuck-at-one faults on each fan-in and fan-out branch and the fan-out origin of the bus (see figure 1).

The fault universe does not explicitly contain any faults within B-logic partitions. However, all faults associated with inputs and outputs of B-logic components either are contained in a G-logic partition or shall be shown to be considered by established test algorithms that are applied to the B-logic partitions.

No faults shall be added or removed by considering or not considering logic model hierarchy. No extra faults shall be associated with any primary input or output line, macro input or output line, or logic line that spans logic partitions where the logic partitions do not correspond to a physical boundary. No more than one stuck-at-zero and one stuck-at-one fault per logic line shall be contained in the initial fault universe.

3.3.2 Fault equivalence classes. The initial fault universe shall be partitioned or collapsed into fault equivalence classes for reporting purposes. The fault equivalence classes shall be chosen such that all faults in a fault equivalence class cause apparently identical erroneous behavior with respect to the observable outputs of the logic model. One fault from each fault equivalence class shall be selected to represent the fault class for reporting purposes; these faults shall be called the representative faults.

For the purpose of implementing this test procedure it is sufficient to apply simple rules to identify structurally-dependent equivalence classes. An acceptable method for selecting the representative faults for the initial fault universe consists of listing all single, permanent, stuck-at faults as specified in table II. Any other fault equivalencing procedure used shall be documented in the fault simulation report. If a bus node exhibits wired-AND or wired-OR behavior in the applicable circuit technology, then faults associated with that bus shall be collapsed in accordance with the AND or OR fault equivalencing rules, respectively. Otherwise, no collapsing of faults associated with a bus shall be performed.

3.3.3 Detectable fault universe. Fault coverage shall be based on the detectable fault universe. Undetectable faults shall be permitted to be dropped from the set of representative faults; the remaining set of representative faults comprises the detectable fault universe. In order for a fault to be declared as undetectable, documentation shall be provided in the fault simulation report as to why there does not exist any test vector sequence capable of guaranteeing that the fault will cause an error at an observable primary output (see 1.1m.). Any fault not documented in the fault simulation report as being undetectable shall be considered detectable for the purpose of calculating fault coverage.

3.4 Fault simulation.

3.4.1 Automatic test equipment limitations. Fault coverage reported for the logic model of a DUT shall reflect the limitations of the target ATE. Two common cases are:

a. Fault detection during fault simulation shall occur only at times where the ATE will be capable of sensing the primary outputs of the DUT; there must be a one-to-one correspondence between simulator compares and ATE compares. For example, if fault coverage for a test vector sequence is obtained using broadside fault simulation (where fault detection occurs after every change of input stimuli, including clock signals), then it is not correct to claim the same fault coverage on the ATE if the test vectors are reformatted into cycles where a clock signal is pulsed during each cycle and compares occur only at the end of each cycle.

b. If the ATE cannot sense the Z output state (either directly or by multiple passes), then the reported fault coverage shall not include detections involving the Z state. That is, an output value of Z shall be considered to be equivalent to an output value of X.

   Any differences in format or timing of the test vector sequence, between that used by the fault simulator and that applied by the ATE, shall be documented in the fault simulation report and it shall be shown that fault coverage achieved on the ATE is not lower than the reported fault coverage.

3.4.2 G-logic.

3.4.2.1 Hard detections and potential detections. Fault coverage for G-logic shall include only faults detected by hard detections. Potential detections shall not be considered directly in calculating the fault coverage. No number of potential detections of a fault shall imply that the fault would be detected.

Some potential detections can be converted into hard detections for the purpose of calculating fault coverage. If it can be shown that a fault is only potentially detected by fault simulation but is in fact detectable by the ATE by a difference not involving an X value, then upon documenting those conditions in the fault simulation report that fault shall be considered to be detected as a hard detection and the fault coverage shall be adjusted accordingly.

Faults associated with three-state buffer enable signal lines can cause X states to occur on nodes with fan-in branches, or erroneous Z states to occur on three-state primary outputs that may be untestable on some ATE. These faults may then be detectable only as potential detections, but may be unconvertible into hard detections. In such cases, it is permissible for the fault simulation report to state separately the fraction of the undetected faults that are due to such faults.

3.4.2.2 Fault simulation procedures. The preferred method of fault simulation for G-logic is to simulate the effect of each representative fault in the G-logic. However, this may not be practical in some cases due to the large number of representative faults, or because of limitations of the logic models or simulation tools. In such cases fault sampling procedures may be used. When fault sampling is used, either the acquisition document shall specify the method of obtaining a random sample of faults or the fault simulation report shall describe the method used. In either case, the complete random sample of faults shall be obtained before beginning the fault simulation procedure involving a random sample of faults.

Use of any fault simulation procedure other than fault simulation procedure 1 (see 3.4.2.2.1) shall be documented and justified in the fault simulation report.

In this section, it is assumed that the representative faults declared to be undetectable have been removed from the set of faults to be simulated.

3.4.2.2.1 Fault simulation procedure 1. Simulate each representative fault in a G-logic partition. The procedure used shall be equivalent to the following:

Step 1: Denote by "n" the total number of representative faults in the G-logic partition.

Step 2: Fault simulate each representative fault. Denote by "d" the number of hard detections.

Step 3: Fault coverage for the G-logic partition is given by d/n.

3.4.2.2.2 Fault simulation procedure 2. Obtain lower bound on actual fault coverage in a G-logic partition using fixed sample size (see table III). The procedure used shall be equivalent to the following:

Step 1: Select a value for the penalty parameter "r" (r = 0.01 to 0.05). The corresponding value of "n" in table III is the size of the random sample of representative faults.

Step 2: Fault simulate each of the "n" representative faults. Denote by "d" the number of hard detections.

Step 3: The lower bound on the fault coverage is given by "d/n-r".

3.4.2.2.3 Fault simulation procedure 3. Accept/reject lower bound on fault coverage in a G-logic partition using fixed sample size (see table IV). The procedure used shall be equivalent to the following:

Step 1: Denote by "F" the minimum required value for fault coverage. From table IV obtain the minimum required sample size, denoted by "n".

Step 2: Fault-simulate each of the "n" representative faults, and denote by "d" the number of hard detections.

Step 3: If "d" is less than "n" (that is, any faults are undetected), then conclude that the fault coverage is less than "F." Otherwise (that is, all sampled faults are detected), conclude that the fault coverage is greater than or equal to "F".

3.4.3 B-logic. Fault coverage shall be measured indirectly for each B-logic partition. For a given B-logic partition, the established fault coverage or test effectiveness shall be reported for that B-logic partition only if it is shown that: (a) the test vector sequence applied to the DUT applies the established test algorithm to the B-logic partition, and (b) the resulting critical output values from the B-logic partition are made observable at the primary outputs. Otherwise, the fault coverage for that B-logic partition shall be reported as 0 percent. For each B-logic partition tested in this way, the established test algorithm, proof of its successful application, and the established fault coverage or test effectiveness shall be documented in the fault simulation report.

3.5 Fault coverage calculation. Let "m" denote the number of logic partitions in the logic model for the DUT. For the i^{th} logic partition, let "F_i" denote its fault coverage (measured in accordance with 3.4), and let "T_i" denote its transistor fraction (measured in accordance with 3.1.5). The fault coverage "F" for the logic model for the DUT shall be calculated as:

$$F = F_1 T_2 + F_2 T_2 + \ldots + F_m T_m$$

If fault simulation procedure 1 is performed for each G-logic partition in the logic model of a DUT, then the fault coverage for the logic model of a DUT shall be reported as:

"F of all detectable equivalence classes of single, permanent, stuck-at-zero and stuck-at-one faults on the logic lines of the logic model as measured by MIL-STD- 883, test method 5012."

If fault simulation procedure 2 or 3 is performed for any G-logic partition, then the fault coverage for the logic model of a DUT shall be reported as:

"No less than F of all detectable equivalence classes of single, permanent, stuck-at-zero and stuck-at-one faults on the logic lines of the logic model, with 95 percent confidence, as measured by MIL-STD-883, test method 5012."

The confidence level of 95 percent shall be identified if any fault simulation procedure other than procedure 1 was performed for any G-logic partition.

4. SUMMARY. The following details shall be specified in the applicable acquisition document:

a. Minimum required level of fault coverage and method of obtaining fault coverage.

b. If a fault sampling method is permitted, guidance on selection of the random sample of faults.

c. Guidelines, restrictions, or requirements for test algorithms for B-Logic types.

d. The fault simulation report shall provide:

(1) Statement of the overall fault coverage. If there are undetectable faults due to three-state enable signal lines, then, optionally, fault coverage based on those potential detections may be reported separately.

(2) Description of logic partitions.

(3) Description of test algorithms applied to B-logic. For each B-logic partition tested in this way the established test algorithm, proof of its successful application, and description of its established fault coverage or test effectiveness (including classes of faults detected) shall be documented.

(4) Justification for any initial condition, other than X, for any logic line or memory element.

(5) Justification for any approximations used, including estimates of fault coverages, transistor fractions, and counts of undetectable faults.

(6) Description of any fault equivalencing procedure used in lieu of the procedure defined by table II.

(7) Justification for declaring any fault to be undetectable.

(8) In the event that the test vector sequence is formatted differently between the ATE and the fault simulator, justification that fault coverage achieved on the ATE is not lower than the reported fault coverage.

(9) Justification of the use of fault simulation procedure 2 or 3 rather than fault simulation procedure 1.

(10) When fault sampling is used, description of the method of obtaining a random sample of faults.

(11) In the event that the fault simulation procedure used is not obviously equivalent to fault simulation procedure 1, 2, or 3, justification as to why it yields equivalent results.

(12) In the event that a test technique or design-for-testability approach is used that provides additional control or observation test points beyond those provided by the DUT's primary inputs and primary outputs (see 1.1j), justification that the stated fault coverage is valid.

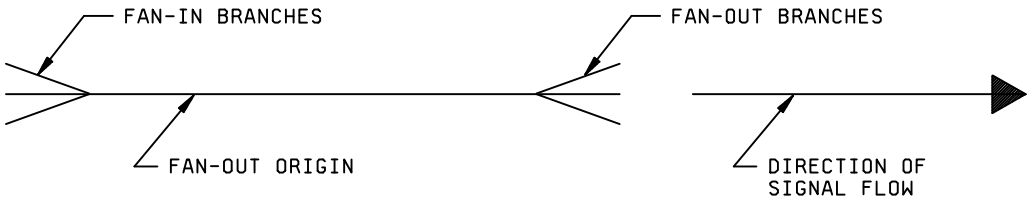

FIGURE 1. Node consisting of fan-in branches, a fan-out origin, and fan-out branches.

TABLE I. Penalty values, P, for LFSR signature analyzers implementing primitive polynomial of degree k.

K	p
k < 8	1.0
k = (8...15)	0.05
k = (16...23)	0.01
k > 23	0.0

TABLE II. Representative faults for the fault equivalence classes.

Stuck-at faults	Type of logic line in logic model
s-a-1	Every input of multiple-input AND or NAND gates
s-a-0	Every input of multiple-input OR or NOR gates
s-a-0, s-a-1	Every input of multiple-input components that are not AND, OR, NAND, or NOR gates
s-a-0, s-a-1	Every logic line that is a fan-out origin
s-a-0, s-a-1	Every logic line that is a primary output

Note: "s-a-0" is stuck-at-zero and "s-a-1" is stuck-at-one.

TABLE III. Sample sizes used to obtain lower bound on fault coverage using fault simulation procedure 2.

r	n
0.01	6860
0.015	3070
0.02	1740
0.03	790
0.04	450
0.05	290

NOTE: "n" is the minimum sample size required for a chosen penalty "r".

TABLE IV. Sample sizes used to accept/reject lower bound on fault coverage using fault simulation procedure 3.

F	n	F'
50.0%	5	87.1%
55.0%	6	89.1%
60.0%	6	89.1%
65.0%	7	90.6%
70.0%	9	92.6%
75.0%	11	93.9%
76.0%	11	93.9%
77.0%	12	94.4%
78.0%	13	94.8%
79.0%	13	94.8%
80.0%	14	95.2%
81.0%	15	95.5%
82.0%	16	95.8%
83.0%	17	96.0%
84.0%	18	96.2%
85.0%	19	96.4%
86.0%	20	96.6%
87.0%	22	96.9%
88.0%	24	97.2%
89.0%	26	97.4%
90.0%	29	97.6%
91.0%	32	97.9%
92.0%	36	98.1%
93.0%	42	98.4%
94.0%	49	98.6%
95.0%	59	98.8%
96.0%	74	99.1%
97.0%	99	99.3%
98.0%	149	99.5%
99.0%	299	99.8%

NOTE: For a given minimum required fault coverage "F" simulate "n" faults. If all faults are detected, then conclude that the actual fault coverage is greater than or equal to "F". Otherwise, conclude that the actual fault coverage is less than "F." The column labeled "F'" shows the actual fault coverage that has a 50 percent probability of acceptance.

METHOD 5013.1

WAFER FABRICATION CONTROL AND WAFER ACCEPTANCE PROCEDURES FOR PROCESSED GaAs WAFERS

1. PURPOSE. This method specifies wafer fabrication control and wafer acceptance requirements for GaAs monolithic microcircuits for application in class level B or class level S microcircuits. It shall be used in conjunction with other documents such as MIL-PRF-38535, MIL-PRF-38534 and an applicable device specification or drawing to establish the design, material, performance, control, and documentation requirements.

2. APPARATUS. The apparatus required for this test method includes metallurgical microscopes capable of up to 1,000X magnification, a scanning electron microscope (SEM), electrical test equipment suitable for the measurement of process monitor (PM) test structures and other apparatus as required to determine conformance to the requirements of this test method.

3. PROCEDURE. The procedures defined herein specify the wafer fabrication controls and wafer acceptance tests necessary for the production of GaAs wafers compliant to the requirements of this test method.

3.1 Precedence. Unless otherwise specified in the device specification or drawing, the test requirements and conditions shall be as given herein.

3.2 Wafer fabrication line controls.

3.2.1 Process baseline. The use of this test method is restricted to a well characterized (controlled) and baselined process. By "characterized" it is meant that the fabrication line has been adequately documented in relation to the capabilities of the process. "Baselined" refers to the existence of a well defined process parameter target value with associated variances (based on characterization data) against which the actual wafer to wafer process data is measured to determine acceptability. The manufacturer shall submit process baseline documentation as specified herein to the acquiring activity for approval.

3.2.2 Statistical process control. The manufacturers shall have implemented statistical process control (SPC) for the wafer fabrication line in accordance with the requirements of TechAmerica EIA-557.

3.2.2.1 Alternate visual inspection procedure for class level B microcircuits. A sample plan for visual inspection in accordance with 3.1 of test method 2010 may be implemented in lieu of 100 percent visual inspection for processes controlled by the SPC program. The sample size for inspection shall be identified in the baseline process documentation.

3.2.3 Incoming material evaluation. Incoming material evaluation shall be performed as documented in the process baseline to assure compatibility with wafer fabrication specifications and manufacturing procedures.

3.2.4 Electrostatic discharge sensitivity. The manufacturer shall develop and implement an ESD control program for the wafer fabrication area.

3.2.5 Failure analysis. When required by the applicable device specification or drawing, failure analysis shall be performed on wafers rejected at in-process or acceptance testing.

3.3 Wafer acceptance tests.

3.3.1 General. This wafer lot acceptance procedure is based on wafer visual inspection and electrical testing of suitable process monitors (PMs), see table I. The performance of each wafer shall be evaluated individually. Process monitor measurements, verifying that the identified baseline parameters are within process limits, will be required from each wafer lot in accordance with 3.3.2 herein.

3.3.1.1 Process monitor (PM). A process monitor (PM) is a collection of test structures which provide data for the purposes of process control and determining wafer acceptability. PMs may be either stepped into every wafer in dedicated drop-in locations, incorporated into kerf locations, located on each die, or combinations of these, such that they can be probed at the conclusion of processing up to and including final front-side metallization and passivation (glassivation) where applicable. PM structures, tests and acceptance limits shall be recorded in the baseline document. A suggested list is shown in table I.

3.3.2 PM evaluation. Wafer acceptance will be made on a wafer by wafer basis upon the information derived from PM room temperature testing, which may be performed at any time during the manufacturing cycle. If drop-in PMs are utilized each wafer shall have a sufficient number of PMs stepped in the center of each of the quadrants to assure the integrity of the wafer acceptance procedure and the baseline SPC program. For kerf PMs and for PMs on individual die, the probed PMs shall be located in the center of the wafer and in each of the quadrants. Quadrant PMs shall lie at least one-half of the distance to the wafer edge away from the wafer center.

3.3.3 Visual/SEM inspection. Inspection via visual microscopy or SEM shall be performed at critical process steps during wafer fabrication. When the process flow includes substrate via processing, the backside features shall be visually inspected to the criteria specified in test method 2010. Inspections may include patterns, alignment verniers, and critical dimension measurements. Defective wafers shall be removed from the lot for scrap or for rework. Inspection operations, sampling plans and acceptance criteria shall be documented in the process baseline.

3.3.4 Test results. When required by the device specification or drawing or for qualification, the following test results shall be made available for each wafer lot submitted.

a. Results of each test conducted; initial and any resubmissions.

b. Number of wafers accepted/rejected per lot.

c. Number of reworked wafers and reason for rework.

d. Measurements and records of the data for all specified PM electrical parameters.

3.3.5 Defective wafers. All wafers that fail any test criteria shall be removed at the time of observation or immediately at the conclusion of the test in which the failure was observed. Rejected wafers may be subjected to approved rework operations as detailed in the baseline document. Once rejected and verified as an unreworkable failure, no wafer may be retested for acceptance. Rejected wafers processed in accordance with approved rework procedures shall be resubmitted to all applicable inspections at the point of rejection and must be found acceptable prior to continuing processing.

3.3.6 Element evaluation. When specified, upon completion of wafer acceptance based on the baseline SPC program and PM measurement results, 100 percent static/RF testing at 25°C shall be performed on each individual die. Failures shall be identified and removed from the lot when the die are separated from the wafer.

TABLE I. Test structures for use in a PM.

1.	N-channel transistors for measuring transistor parameters.
2.	P-channel transistors for measuring transistor parameters.
3.	Sheet resistance.
4.	E-mode transistor parameters.
5.	D-mode transistor parameters.
6.	Isolation.
7.	Contact resistance (via/ohmics).
8.	Step coverage.
9.	Alignment verniers.
10.	Line width.
11.	Diode parameters.
12.	Backgating.
13.	Doping profile structure.
14.	FATFET.
15.	Thin film resistor characteristics.
16.	Capacitance value measurements.

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CONCLUDING MATERIAL

Custodians:
Army - CR
Navy - EC
Air Force – 85
NASA – NA
DLA – CC

Preparing activity:
DLA – CC

(Project 5962-2019-009)

Review activities:
Army - AR, EA, MI, SM
Navy – AS, CG, MC, SH
Air Force – 03, 19

NOTE: The activities listed above were interested in this document as of the date of this document. Since organizations and responsibilities can change, you should verify the currency of the information above using the ASSIST Online database at https://assist.dla.mil/.