This document and process conversion measures necessary to comply with this change shall be completed by 16 March 2020.

INCH - POUND

MIL-STD-883-4
16 September 2019
SUPERSEDING
MIL-STD-883K
w/CHANGE 3
3 May 2018

DEPARTMENT OF DEFENSE

TEST METHOD STANDARD

ELECTRICAL TESTS (LINEAR) FOR MICROCIRCUITS

PART 4: TEST METHODS 4000-4999

AMSC N/A

FSC 5962

FOREWORD

1. This standard is approved for use by all Departments and Agencies of the Department of Defense.

2. This entire standard has been revised. This revision has resulted in many changes to the format, but the most significant one is the splitting the document into parts. See MIL–STD–883 for the change summary.

3. Comment, suggestions, or questions on this document should be addressed to: Commander, Defense Logistics Agency, ATTN: DLA Land and Maritime - VA, P.O. Box 3990, Columbus, OH 43218-3990, or by email to STD883@dla.mil. Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at: https://assist.dla.mil.

CONTENTS

ELECTRICAL TESTS (LINEAR)

1. SCOPE

1.1 Purpose. Part 3 of this test method standard establishes uniform test methods for the electrical testing (digital) to determine resistance to deleterious effects of natural elements and conditions surrounding military operations. For the purpose of this standard, the term "devices" includes such items as monolithic, multichip, film and hybrid microcircuits, microcircuit arrays, and the elements from which the circuits and arrays are formed. This standard is intended to apply only to microelectronic devices.

1.2 Numbering system. The test methods are designated by numbers assigned in accordance with the following system:

1.2.1 Classification of tests. The electrical test methods included in this part of a multipart test method standard are numbered 4001 to 4007 inclusive.

1.2.2 Test method revisions. Revisions are numbered consecutively using a period to separate the test method number and the revision number. For example, 4001.2 designates the second revision of test method 4001.

2. APPLICABLE DOCUMENTS

2.1 General. The documents listed in this section are specified in sections 3, 4, and 5 of this standard. This section does not include documents cited in other sections of this standard or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements documents cited in sections 3, 4, and 5 of this standard, whether or not they are listed.

2.2 Government documents.

2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

MIL-PRF-680	-	Degreasing Solvent, Performance Specification For.
MIL-PRF-19500	-	Semiconductor Devices, General Specification For.
MIL-PRF-38534	-	Hybrid Microcircuits, General Specification For.
MIL-PRF-38535	-	Integrated Circuits (Microcircuits) Manufacturing, General Specification For.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-202	-	Electronic and Electrical Component Parts.
MIL-STD-750	-	Test Methods for Semiconductor Devices.
MIL-STD-1686	-	Electrostatic Discharge Control Program for Protection of Electrical and Electronic Parts, Assemblies and Equipment (Excluding Electrically Initiated Explosive Devices).
MIL-STD-1835	-	Electronic Component Case Outlines.
MIL-STD-1916	-	DOD Preferred Methods for Acceptance of Product.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-217	-	Reliability Prediction of Electronic Equipment.
MIL-HDBK-505	-	Definitions of Item Levels, Item Exchangeability, Models, and Related Terms.
MIL-HDBK-781	-	Reliability Test Methods, Plans, and Environments for Engineering, Development Qualification, and Production .
MIL-HDBK-1331	-	Parameters to be Controlled for the Specification of Microcircuits.

FEDERAL STANDARDS

SAE AMS-STD-595	-	Colors Used in Government Procurement
SAE AMS-STD-595/15102	-	Blue, Gloss
SAE AMS-STD-595/25102	-	Blue, Semi-gloss

OTHER GOVERNMENT DOCUMENTS, DRAWINGS, AND PUBLICATIONS

QML-38534	-	Hybrid Microcircuits, General Specification For.
QML-38535	-	Integrated Circuits (Microcircuits) Manufacturing, General Specification For.

COMMERCIAL ITEM DESCRIPTIONS

A-A-58092	-	Tape, Antiseize, Polytetrafluorethylene.

(Copies of these documents are available online at https://assist.dla.mil.)

2.3 Non-Government publications. The following documents form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

INTERNATIONAL ORGANIZATION FOR STANDARDIZATION (ISO) STANDARDS

ISO 14644-1	-	Cleanrooms and Associated Controlled Environments – Part 1: Classification of Air Cleanliness.
ISO 14644-2	-	Cleanrooms and Associated Controlled Environments – Part 2: Specifications for Testing and Monitoring to Prove Continued Compliance with ISO 14644-1.
ISO /ASTM 51275	-	Standard Practice for Use of a Radiochromic Film Dosimetry System.

(Copies of these documents are available online at https://www.iso.org)

AMERICAN NATIONAL STANDARDS INSTITUTE (ANSI)

ANSI/NCSL Z540.3	-	Requirements for the Calibration of Measuring and Test Equipment, General Requirements.

(Copies of these documents are available online at https://ansi.org)

IPC - ASSOCIATION CONNECTING ELECTRONICS INDUSTRIES (IPC)

IPC J-STD-004	-	Requirements for Soldering Fluxes.
IPC J-STD-005	-	Requirements for Soldering Pastes.
IPC J-STD-006	-	Requirements for Electronic Grade Solder Alloys and Fluxed and Non-fluxed Solid Solders for Electronic Soldering Applications.
IPC J-STD-033	-	Handling, Packing, Shipping and Use of Moisture/Reflow Sensitive Surface Mount Devices.
IPC-T-50	-	Terms and Definitions for Interconnecting and Packaging Electronic Circuits.

(Copies of these documents are available online at https://www.ipc.org)

JEDEC SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC).

JEDEC JESD22-B116	- Wire Bond Shear Test
JEDEC JESD78	- IC Latch-up Test.
JEDEC JESD213	- Common Test Method for Detection Component Surface Finish Material.
JEDEC Standard 12	- Standard for Gate Array Benchmark Set
JEDEC Standard 12-1	- Terms and Definitions for Gate Array Benchmark Set.
JEDEC Standard 12-2	- Standard for Cell-Based Integrated Circuit Benchmark Set.
JEDEC Standard 12-3	- CMOS Gate Array Macrocell Standard.

(Copies of these documents are available online at https://www.jedec.org)

NATIONAL COUNCIL ON RADIAATION PROTECTION AND MEASUREMENT

Report Number 40	-	Protection Against Radiation from Brachytherapy Sources
Report Number 102	-	Medical X-ray, Electron Beam and Gamma Ray Protection

(Copies of these documents are available online at http://www.NCRPPublications.org)

TECHSTREET THOMPSON REUTERS

TechAmerica EIA-557	-	Statistical Process Control Systems.

(Copies of these documents are available online at https://www.techstreet.com)

AMERICAN SOCIETY FOR TESTING AND MATERIALS (ASTM)

ASTM C 177	-	Standard Test Method for Steady-State Heat Flux Measurements and Thermal Transmission Properties by Means of the Guarded Hot-Plate Apparatus.
ASTM C 518	-	Standard Test Method for Steady-State Heat Flux Measurements and Thermal Transmission Properties by Means of the Heat Flow Meter Apparatus.
ASTM D 150	-	Standard Test Methods for A-C Loss Characteristics and Permittivity (Dielectric Constant) of Solid Electrical Insulating Materials.
ASTM D 257	-	Standard Test Methods for D-C Resistance or Conductance of Insulating Materials.
ASTM D 877	-	Standard Test Methods for Dielectric Breakdown Voltage of Insulating Liquids Using Disk Electrodes.
ASTM D 971	-	Interfacial Tension of Oil Against Water by the Ring Method.
ASTM D 1002	-	Standard Test Method for Strength Properties of Adhesives in Shear by Tension Loading (Metal-to-Metal).
ASTM D 1120	-	Engine Coolant, Boiling Point of.
ASTM D 1331	-	Standard Test Methods for Surface and Interfacial Tension of Solutions of Surface-Active Agents.
ASTM D 2109	-	Standard Test Methods for Nonvolatile Matter in Halogenated Organic Solvents and their Admixtures.
ASTM D 3574	-	Materials, Flexible Cellular-Slab, Bonded, and Molded Uretane Foam.
ASTM D 3850	-	Rapid Thermal Degradation of Solid Electrical Insulating Materials by Thermogravimetric Method, Test Method for.
ASTM E 263	-	Standard Test Method for Measuring Fast-Neutron Reaction Rates by Radioactivation of Iron.
ASTM E 264	-	Standard Test Method for Measuring Fast-Neutron Reaction Rates by Radioactivation of Nickel.
ASTM E 265	-	Standard Test Method for Measuring Reaction Rates and Fast-Neutron Fluences by Radioactivation of Sulfur-32.
ASTM E 666	-	Standard Practice for Calculating Absorbed Dose from Gamma or X-Radiation.
ASTM E 668	-	Standard Practice for Application of Thermoluminescence-Dosimetry (TLD) Systems for Determining Absorbed Dose on Radiation Hardness Testing of Electronic Devices.
ASTM E 720	-	Standard Guide for Selection and Use of Neutron Sensors for Determining Neutron Spectra Employed in Radiation-Hardness Testing of Electronics.
ASTM E 721	-	Standard Method for Determining Neutron Energy Spectra with Neutron-Activation Foils for Radiation-Hardness Testing of Electronics.
ASTM E 722	-	Standard Practice for Characterizing Neutron Energy Fluence Spectra in Terms of an equivalent Monoenergetic Neutron Fluence for Radiation-Hardness Testing of Electronics.

AMERICAN SOCIETY FOR TESTING AND MATERIALS (ASTM) (CONTINUED)

ASTM E 801	-	Standard Practice for Controlling Quality of Radiological Examination of Electronic Devices.
ASTM E 831	-	Standard Test Method for Linear Thermal Expansion of Solid Materials by Thermomechanical Analysis
ASTM E 1249	-	Minimizing Dosimetry Errors in Radiation Hardness Testing of Silicon Electronic Devices.
ASTM E 1250	-	Standard Method for Application of Ionization Chambers to Assess the Low Energy Gamma Component of Cobalt 60 Irradiators Used in Radiation Hardness Testing of Silicon Electronic Devices.
ASTM E 2450	-	Standard Practice for Application of CaF_2(Mn) Thermoluminescence Dosimeters in Mixed Neutron-Photon Environments.
ASTM F 458	-	Standard Practice for Nondestructive Pull Testing of Wire Bonds.
ASTM F 459	-	Standard Test Methods for Measuring Pull Strength of Microelectronic Wire Bonds.
ASTM F 526	-	Standard Test Method for Measuring Dose for Use in Linear Accelerator Pulsed Radiation Effects Tests.
ASTM F 1192	-	Standard Guide for the Measurement of Single Event Phenomena (SEP).
ASTM F 1892	-	Standard Guide for Ionizing Radiation (Total Dose) Effects Testing of Semiconductor Devices.

(Copies of these documents are available online at https://www.astm.org/)

2.4 Order of precedence. Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. DEFINITIONS

3.1 Abbreviations, symbols, and definitions. For the purpose of this standard, the abbreviations, symbols, and definitions specified in MIL-PRF-19500, MIL-PRF-38535, or MIL-HDBK-505 apply. The following definitions also apply:

3.1.1 Microelectronic device. A microcircuit, microcircuit module, or an element of a microcircuit as defined in appendix A of MIL-PRF-38535. For the purposes of this document, each type of microelectronic device will be identified by a unique type, or drawing number.

3.1.2 Mode of failure. The cause for rejection of any failed device or microcircuit as defined in terms of the specific electrical or physical requirement which it failed to meet (i.e., no failure analysis is required to identify the mode of failure, which should be obvious from the rejection criteria of the test method).

3.1.3 Mechanism of failure. The original defect which initiated the microcircuit or device failure or the physical process by which the degradation proceeded to the point of failure, identifying quality defects, internal, structural, or electrical weakness and, where applicable, the nature of externally applied stresses which led to failure.

3.1.4 Absolute maximum ratings. The values specified for ratings, maximum ratings, or absolute maximum ratings are based on the "absolute system" and are not to be exceeded under any measurable or known service or conditions. In testing microelectronic devices, limits may be exceeded in determining device performance or lot quality, provided the test has been determined to be nondestructive and precautions are taken to limit device breakdown and avoid conditions that could cause permanent degradation. These ratings are limiting values beyond which the serviceability of any individual microelectronic integrated circuit may be impaired. It follows that a combination of all the absolute maximum ratings cannot normally be attained simultaneously. Combinations of certain ratings are permissible only if no single maximum rating is exceeded under any service condition. Unless otherwise specified, the voltage, current, and power ratings are based on continuous dc power conditions at free air ambient temperature of 25°C ±3°C. For pulsed or other conditions of operation of a similar nature, the current, voltage, and power dissipation ratings are a function of time and duty cycle. In order not to exceed absolute ratings, the equipment designer has the responsibility of determining an average design value, for each rating, below the absolute value of that rating by a safety factor, so that the absolute values will never be exceeded under any usual conditions of supply-voltage variations, load variations, or manufacturing variations in the equipment itself.

3.1.5 Worst case condition. Worst case condition(s) consists of the simultaneous application of the most adverse (in terms of required function of the device) values (within the stated operating ranges) of bias(es), signal input(s), loading and environment to the device under test. Worst cases for different parameters may be different. If all the applied test conditions are not established at the most adverse values, the term "partial worst case condition" should be used to differentiate and should be accompanied by identification of the departure from worst case. For example, the lowest values of supply voltages, signal input levels, and ambient temperature and the highest value of loading may constitute "worst case conditions" for measurement of the output voltage of a gate. Use of the most adverse values of applied electrical conditions, at room temperature, would then constitute "partial worst case conditions" and should be so identified using a postscript "at room temperature."

3.1.5.1 Accelerated test condition. Accelerated test conditions are defined as test conditions using one or more applied stress levels which exceed the maximum rated operating or storage stress levels but are less than or equal to the "Testing Rating" values.

3.1.6 Static parameters. Static parameters are defined as dc voltages, dc currents, or ratios of dc voltages or dc currents, or both.

3.1.7 Dynamic parameters. Dynamic parameters are defined as those which are rms or time-varying values of voltages or currents, or ratios of rms or time-varying values of voltages or currents, or both.

3.1.8 Switching parameters. Switching parameters are defined as those which are associated with the transition of the output from one level to another or the response to a step input.

3.1.9 Functional tests. Functional tests are defined as those go, no-go tests which sequentially exercise a function (truth) table or in which the device is operated as part of an external circuit and total circuit operation is tested.

3.1.10 Acquiring activity. The acquiring activity is the organizational element of the Government which contracts for articles, supplies, or services; or it may be a contractor or subcontractor when the organizational element of the Government has given specific written authorization to such contractor or subcontractor to serve as agent of the acquiring activity. A contractor or subcontractor serving as agent of the acquiring activity does not have the authority to grant waivers, deviations, or exceptions unless specific written authorization to do so has also been given by the Government organization.

3.1.11 Accuracy. The quality of freedom from error. Accuracy is determined or assured by calibration, or reliance upon calibrated items.

3.1.12 Calibration. Comparison of measurement standard or instrument of known accuracy with another standard, instrument or device to detect, correlate, report or eliminate by adjustment, any variation in the accuracy of the item being compared. Use of calibrated items provide the basis for value traceability of product technical specifications to national standard values. Calibration is an activity related to measurement and test equipment performed in accordance with ANSI/NCSL Z540.3 or equivalent.

3.1.13 Precision. The degree to which an instrument, device, assemblage, test, measurement or process exhibits repeatability. Expressed statistically or through various techniques of Statistical Process Control (SPC). Term is used interchangeably with "repeatability".

3.1.14 Resolution. The smallest unit of readability or indication of known value in an instrument, device or assemblage thereof.

3.1.15 Standard reference material (SRM). A device or artifact recognized and listed by the National Institute of Standards and Technology (NIST) as having known stability and characterization. SRM's used in product testing provide traceability for technical specifications. SRM's do not require calibration when used and stored in accordance with NIST accompanying instructions. They are used as "certified materials".

3.1.16 Tolerance. A documented range over which a specified value may vary.

3.1.17 Test accuracy ratio (TAR). A ratio of the tolerance of the device under test to the accuracy of the related measuring or test instrument or to the accuracy of the correlation device/SRM.

3.1.18 Uncertainty. An expression of the combined errors in a test measurement process. Stated as a range within which the subject quantity is expected to lie. Comprised of many components including: estimates of statistical distribution and results of measurement or engineering analysis. Uncertainty established with a suitable degree of confidence, may be used in assuring or determining product conformance and technical specifications.

3.1.19 Susceptibility. The point at which a device fails to meet the postirradiation end-point electrical parameter limits or fails functionally during radiation exposure (e.g., neutron irradiation).

3.1.20 Class M. Class M is defined as 1.2.1 of MIL-STD-883 basic compliant product or product built in compliance to Appendix A of MIL-PRF-38535 documented on a Standard Microcircuit Drawing where configuration control is provided by the Government preparing activity. Class M devices are required to use the conditions specified in the test methods herein for class level B product.

3.1.21 Class level B and class level S. 2 class levels are used in this document to define requirements for high reliability military applications (Class level B) and space applications (Class level S). Class level B requirements contained in this document are intended for use for Class Q, Class H, and Class M products, as well as Class B M38510 JAN slash sheet product. Class level B requirements are also intended for use for product claimed as 883 compliant or 1.2.1 compliant for high reliability military applications. Class level S requirements contained in this document are intended for use for Class V, Class K, as well as M38510 Class S JAN slash sheet product. Class level S requirements are also intended for use for product claimed as 883 compliant or 1.2.1 of MIL-STD-883 basic compliant for space level applications.

3.1.22 Acquisition documents. Acquisition documents consist of the acquisition order or contract, device specification (e.g. SMD's, SCD's) or specifications as applicable.

4. GENERAL REQUIREMENTS

4.1 General. Unless otherwise specified in the individual test method, the general requirements of MIL-STD-883 shall apply.

4.2 Test circuits. The test circuits shown in the test methods of this test method standard are given as examples which may be used for the measurements. They are not necessarily the only test circuits which can be used; however the manufacturer shall demonstrate to the Government that other test circuits which they may desire to use will give results within the desired accuracy of measurement.

4.3 Laboratory suitability. Prior to processing any microcircuit intended for use in any military system or sub-system, the facility performing the test(s) shall be audited by the DLA Land and Maritime, Sourcing and Qualification Division and be granted written laboratory suitability status for each test method to be employed. Processing of any devices by any facility without laboratory suitability status for the test methods used shall render the processed devices nonconforming.

4.4 Method of reference. When applicable, test methods contained herein shall be referenced in the individual specification or specification sheet by specifying the test method number and, the details required in the summary of the applicable test method shall be listed. To avoid the necessity for changing documents that refer to test methods of this standard, the revision number should not be used when referencing test methods. (For example: Use 4001 versus 4001.2.)

5. DETAILED REQUIREMENTS

This section is not applicable to this standard.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory.)

6.1 Intended use. The intended use of this test method standard is to establish appropriate conditions for testing semiconductor devices to give test results that simulate the actual service conditions existing in the field. This test method standard has been prepared to provide uniform test methods, controls, and procedures for determining with predictability the suitability of such devices within military, aerospace and special application equipment.

6.2 International standardization agreement. Certain provisions of this test method standard are the subject of international standardization agreement. When amendment, revision, or cancellation of this test method standard is proposed which will affect or violate the international agreement concerned, the preparing activity will take appropriate reconciliation action through international standardization channels, including departmental standardization offices, if required.

6.3 Subject term (key word) listing

Destructive tests
Environmental tests
Laboratory suitability
Non–destructive tests

6.4 Supersession data The main body and five parts (–1 through –5) of this revision of MIL-STD-883 replace superseded MIL–STD–883K

METHOD 4001.1

INPUT OFFSET VOLTAGE AND CURRENT AND BIAS CURRENT

1. PURPOSE. This method establishes the means for measuring input bias current and the offset in voltage and current at the input of a linear amplifier with differential inputs. Offset voltage may also be pertinent in some single input amplifiers. Input bias current will also be measured in this procedure.

1.1 Definitions. The following definitions shall apply for the purpose of this test method.

1.1.1 Input offset voltage (V_{IO}). That dc voltage which must be applied between the input terminals through two equal resistances to force the quiescent dc output to zero or other specified level V_{QO}, generated by V_{QI}.

1.1.2 Input offset voltage drift (DV_{IO}). Input offset voltage drift is the ratio of the change of input offset voltage to the change of the circuit temperature.

$$DV_{IO} = \frac{\Delta V_{IO}}{\Delta T}$$

1.1.3 Input offset current (I_{IO}). The input offset current is the difference between the input bias currents entering into the input terminals of a differential input amplifier required to force the output voltage to zero or other specified level (V_{QO}).

1.1.4 Input offset current drift (DI_{IO}). The input offset current drift is the ratio of the change of input offset current to the change of circuit temperature.

$$DI_{IO} = \frac{\Delta I_{IO}}{\Delta T}$$

1.1.5 Input bias current (I_{IB}). The input bias currents are the separate currents entering into the two input terminals of a balanced amplifier, specified as $+I_{IB}$ and $-I_{IB}$. The bias current in a single ended amplifier is defined as I_{IB}.

1.1.6 Input offset voltage adjust ($\pm V_{IO\ adj}$). Bias adjustment which produces maximum offset at the output.

2. APPARATUS. The apparatus shall consist of appropriate test equipment capable of measuring specified parameters and an appropriate test fixture with standard input, output, and feedback resistances.

3. PROCEDURE. The test figures show the connections for the various test conditions. An op amp null loop test figure is also shown as an alternate test setup. R_2 shall be no larger than the nominal input impedance nor less than a value which will load the amplifier (10 x Z_{OUT}). Let R_2/R_1 = 100 or 0.1 x (open loop gain), whichever is smaller. Recommended stabilization and power supply decoupling circuitry shall be added. R_3 shall be no larger than the nominal input impedance. For methods using the null loop circuit, assume all switches (relays) normally closed.

3.1 Input offset voltage.

3.1.1 Differential input amplifier. The test setup is shown on figure 4001-1. Input offset voltage $V_{IO} = (R_1/R_2)(E_O - V_{QI})$. Switches S_1 and S_2 are closed for this test.

3.1.2 Single ended inverting amplifier. The test setup is shown on figure 4001-2. Input offset voltage $V_{IO} = (R_1/R_2)(E_O - V_{QI})$. Switch S is closed for this test.

3.1.3 Single ended noninverting amplifier. The test figure is shown on figure 4001-3. $V_{IO} = (R_1/R_2)(E_O - V_{QI})$. Switch S is closed for this test.

3.1.4 Differential input amplifier. This is an alternative method using the null loop circuit of figure 4001-4, in which all switches are closed. Set V_C to zero. Measure E_O. $V_{IO} = (R_1/R_2)(E_O)$.

3.2 Input offset current. This has a meaning for differential input amplifiers only.

3.2.1 Differential input amplifier. The test figure is shown on figure 4001-1. Measure E_{01} with S_1 and S_2 closed, measure E_{02} with S_1 and S_2 open.

$$I_{IO} = \frac{R_1}{R_2}\left(\frac{E_{01} - E_{02}}{R_3}\right)$$

3.2.2 Differential input amplifier using null loop. The test setup is shown on figure 4001-4, S_1 and S_4 are closed, set
$V_C = 0$. Measure E_{01} as in 3.1.4. Open S_2 and S_3 and measure E_{02}.

$$I_{IO} = \frac{R_1}{R_2}\left(\frac{E_{02} - E_{01}}{R_3}\right)$$

3.3 Input bias current.

3.3.1 Differential input amplifier. The test figure is shown on figure 4001-1. Measure E_{01} with S_1 and S_2 closed, measure E_{02} with S_1 closed and S_2 open. Measure E_{03} with S_1 open and S_2 closed.

$$I_{IB+} = \frac{R_1}{R_2}\left(\frac{E_{01} - E_{02}}{R_3}\right)$$

$$I_{IB-} = \frac{R_1}{R_2}\left(\frac{E_{01} - E_{03}}{R_3}\right)$$

3.3.2 Single ended inverting amplifier. The test figure is shown on figure 4001-2. Measure E_{01} with S closed, measure E_{02} with S open.

$$I_{IB} = \frac{R_1}{R_2}\left(\frac{E_{01} - E_{02}}{R_3}\right)$$

3.3.3 Single ended noninverting amplifier. The test figure is shown on figure 4001-3. Measure E_{01} with S closed. Measure E_{02} with S open.

$$I_{IB} = \frac{R_1}{R_2}\left(\frac{E_{01} - E_{02}}{R_3}\right)$$

3.3.4 Differential input amplifier using null loop. The test setup is shown on figure 4001-4. Set V_C to zero with S_1 and S_4 closed. Measure E_{01} with S_2 closed and S_3 closed. Measure E_{02} wth S_2 open and S_3 closed. Measure E_{03} with S_2 closed and S_3 open.

$$I_{IB+} = \frac{R_1}{R_2}\left(\frac{E_{03} - E_{01}}{R_3}\right)$$

$$I_{IB-} = \frac{R_1}{R_2}\left(\frac{E_{02} - E_{01}}{R_3}\right)$$

3.4 Input offset voltage drift. Measurement of V_{IO1} is made at temperature T_1 in accordance with 3.1 and a second measurement at T_2 of V_{I02} is made at the second temperature.

$$DV_{IO} = \frac{V_{IO2} - V_{IO1}}{T_2 - T_1}$$

3.5 Input offset current drift. Measurement of I_{I01} is made at temperature T_1 and I_{I02} at temperature T_2 in accordance with 3.2.

$$DI_{IO} = \frac{I_{IO2} - I_{IO1}}{T_2 - T_1}$$

3.6 Adjustment for input offset voltage. Use the value of E_0 for 3.1.4. Measure E_{01} with the offset null voltage (V_{ON}) set to the positive extreme.

$$V_{IO\,Adj}(+) = (E_O - E_{01})\frac{R_1}{R_2}$$

Measure E_{02} with the offset null voltage (V_{ON}) set to the negative extreme:

$$V_{IO\,Adj}(-) = (E_O - E_{02})\frac{R_1}{R_2}$$

NOTE: V_{ON} may be implemented using a combination of resistors to obtain the proper voltage across the offset null terminals. This determination shall be based on the device under test (DUT) specifications.

4. SUMMARY. The following details shall be specified in the applicable acquisition document for specified values of R_1, R_2, and R_3, R_4, R_5, R_L, and $\pm V_{CC}$ of the nulling amplifier.

a. V_{IO} maximum.

b. DV_{IO} maximum at specified temperature(s).

c. I_{IO} maximum when applicable.

d. DI_{IO} maximum, when applicable at specified temperature(s).

e. I_{IB+} and I_{IB-} maximum at specified temperature(s).

f. V_{QI} and V_{QO}, when applicable, at specified temperature(s).

g. $\pm V_{IO\,Adj}$ at specified temparature(s).

h. Test temperature(s). Unless otherwise specified, all parameters shall be measured at the minimum and maximum specified operating temperature and at +25°C ambient.

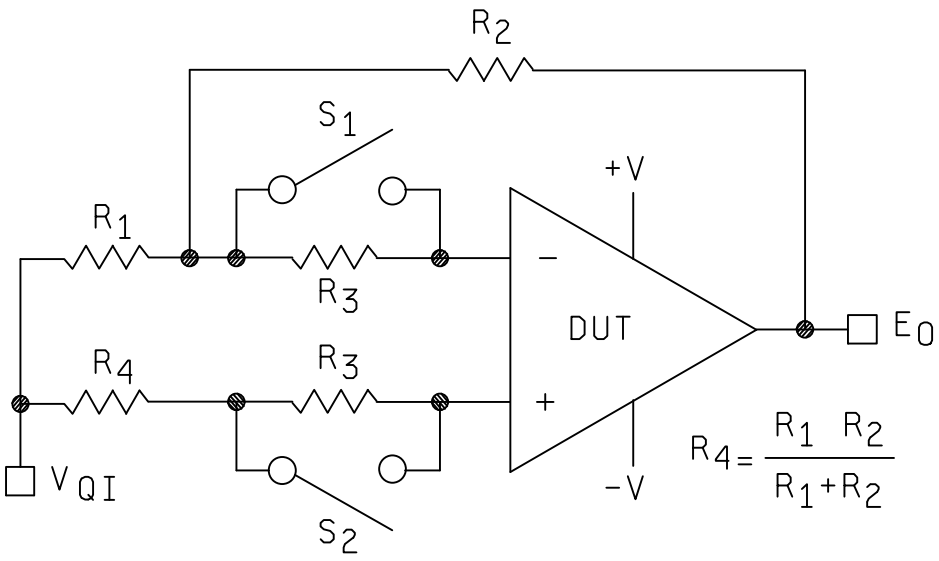

FIGURE 4001-1. Differential input amplifier.

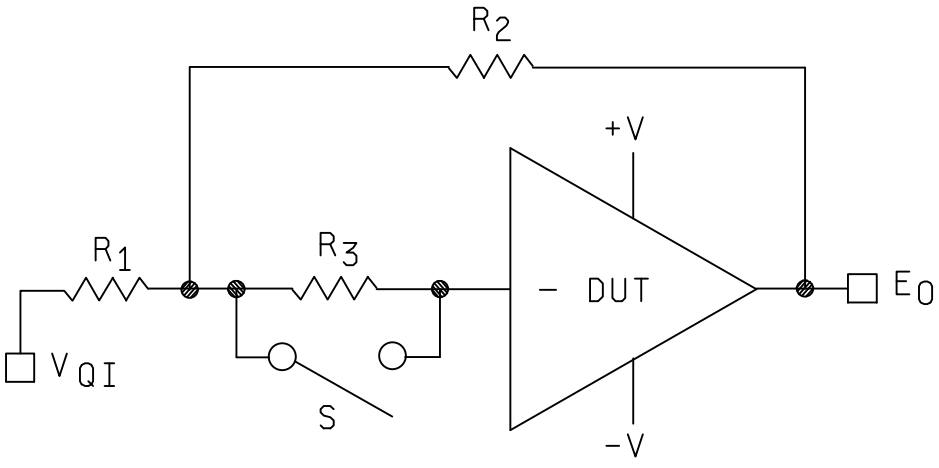

FIGURE 4001-2. Single ended inverting amplifier.

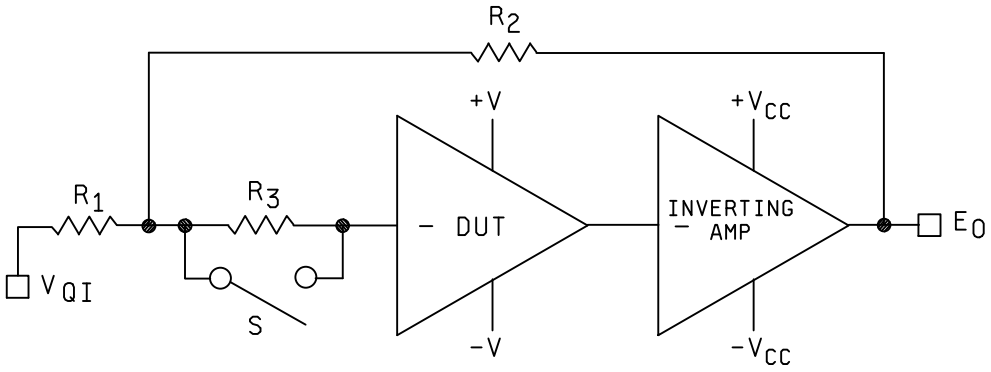

FIGURE 4001-3. Single ended noninverting amplifier.

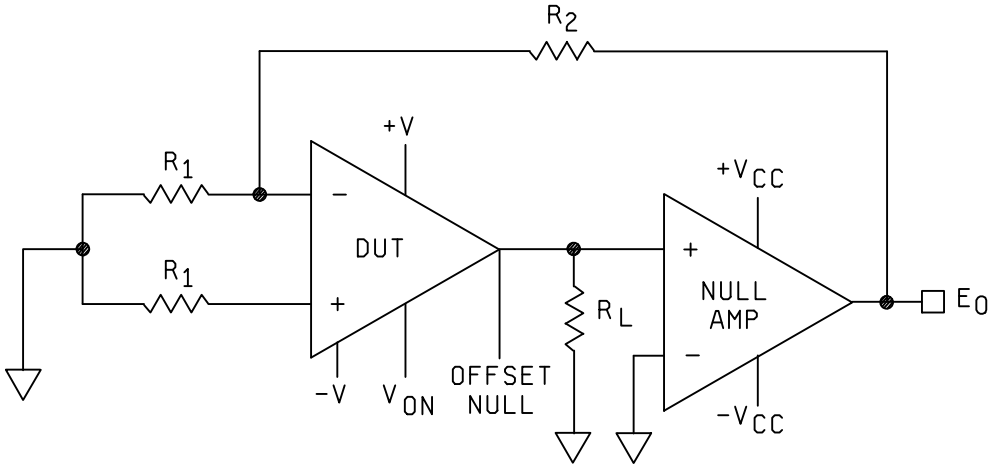

FIGURE 4001-4. Differential input amplifier using null loop.

This page intentionally left blank

METHOD 4002.1

PHASE MARGIN AND SLEW RATE MEASUREMENTS

1. PURPOSE. This method establishes the means for measuring the stability and slew rate of a linear amplifier intended to be used with feedback.

1.1 Definitions. The following definitions shall apply for the purpose of this test method.

1.1.1 Phase margin. The phase margin is 180° minus the absolute value of the phase shift measured around the loop at that frequency at which the magnitude of the loop gain is unity. The loop is the series path of the device under test and the feedback network which is opened at the inverting terminal. The inverting terminal is loaded down to simulate the load normally presented by the feedback network. Good practice dictates that the phase margin should be at least 45°.

1.1.2 Peaking. If a closed loop gain versus frequency plot is made, peaking is the amount by which the gain may increase over its nominal value just before it falls off. 3 dB of peaking will result from a phase margin of 45°. Thus, it is desirable to keep the peaking less than 3 dB.

1.1.3 Slew rate. Slew rate is the time rate of change of the closed-loop amplifier output voltage under large signal conditions (i.e., the maximum ac input voltage for which the amplifier performance remains linear). Stabilization networks will affect the slew rate and therefore these must be included in the measurement.

2. APPARATUS. The apparatus shall consist of appropriate test equipment capable of measuring specified parameters and appropriate test fixture with standard input, output, and feedback resistances.

3. PROCEDURE. The test figures show the connections for the various test conditions. Recommended stabilization networks should be added to compensate for the degree of feedback in the test. The circuit under test should have adequate power supply decoupling added. For differential output devices, the measurements described in 3.1 through 3.2.1 below, as applicable, shall be repeated for the other output using the same test figure except an oscilloscope shall be connected to the other output.

3.1 Phase margin. The test shall be setup as on figure 4002-1 for a gain of 1 noninverting. This is the maximum feedback case. R_2 and R_1 shall be the same value and shall be low compared to the amplifier input impedance. Figure 4002-2 shows the amplitude of the envelope of the output E_O. The peaking shall be less than 3 dB (1.414 times the flat band voltage) to indicate a 45° phase margin minimum. The circuit of figure 4002-3 shall be used for single ended inverting amplifiers (where no positive input terminal is brought out) or where the test is to be run at closed loop gains greater than 1. Closed loop gain = R_2/R_1. In the case of closed loop gains greater than one, the peaking shall be less than 3 dB.

3.2 Pulsed slew rate. Figure 4002-1 or 4002-3 is the test figure for this test. Values of R_2 and R_1 shall be the same values as those used in the phase margin test. Stabilization networks shall also be the same. The pulse amplitude V_1 shall be such that E_0 is the maximum large signal value for the amplifier. With the pulse V_1 having a rise and fall time much faster than the specified slew rate for the amplifier, the rise and fall time for the amplifier shall be measured and shall be within specified limits (see 4). The test shall be repeated for both polarities of V_1.

4. SUMMARY. The following details shall be specified in the applicable acquisition document for specified values of R_1, R_2, and V_1.

a. Maximum peaking.

b. Maximum rise time for E_0 positive pulses.

c. Maximum fall time for E_0 positive pulses.

d. Maximum rise time for E_0 negative pulses.

e. Maximum fall time for E_0 negative pulses.

f. Test temperature(s). Unless otherwise specified, all parameters shall be measured at the minimum and maximum specified ambient operating temperatures and at 25°C ambient.

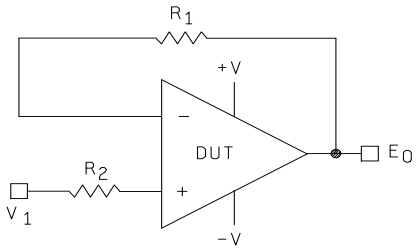

FIGURE 4002-1. Test setup noninverting amplifier.

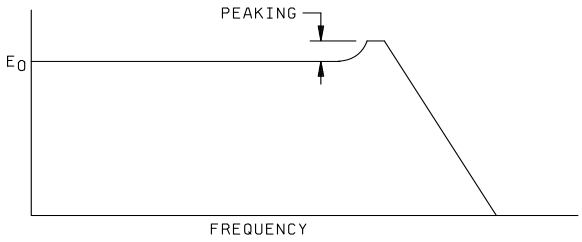

FIGURE 4002-2. Amplitude of E_o.

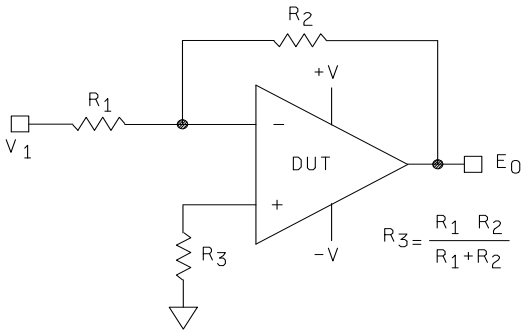

FIGURE 4002-3. Test setup single ended inverting amplifier.

This page intentionally left blank

METHOD 4003.2

COMMON MODE INPUT VOLTAGE RANGE
COMMON MODE REJECTION RATIO
SUPPLY VOLTAGE REJECTION RATIO

1. PURPOSE. This method establishes the means for measuring common mode input voltage range, common mode rejection ratio, and supply voltage rejection ratio.

1.1 Definitions. The following definitions shall apply for the purpose of this test method.

1.1.1 Common mode input voltage range (V_{CM}). The common mode input voltage range is that range of common mode input voltages which, if exceeded, will cause the amplifier to distort or is that range of voltage which may be applied to the input terminals of the device without decreasing the common mode rejection ratio (CMRR) by more than 6 dB.

1.1.2 Common mode rejection ratio (CMRR). The common mode rejection ratio is the ratio of the differential open loop gain, A_D, to the common mode voltage gain, A_C.

$$CMRR = \frac{A_D}{A_C}$$

CMRR is usually expressed in decibels:

$$CMRR = 20 \log \frac{A_D}{A_C}$$

Common mode rejection ratio can also be expressed as the ratio of change in offset voltage to the change in common mode voltage.

$$CMRR = 20 \log \frac{\Delta V_{IO}}{\Delta V_{CM}}$$

1.1.3 Power supply rejection ratio (PSRR). The power supply rejection ratio is the ratio of the change in input offset voltage ΔV_{IO}, to the corresponding change in one power supply voltage with all remaining power supply voltage(s) held constant.

$$+PSRR = \frac{\Delta V_{IO}}{\Delta V_{CC}} \qquad V_{BB} = constant$$

$$-PSRR = \frac{\Delta V_{IO}}{\Delta V_{BB}} \qquad V_{CC} = constant$$

$$PSRR = \frac{\Delta V_O}{A_D \, \Delta V_{CC}}$$

2. APPARATUS. The apparatus shall consist of appropriate test equipment capable of measuring specified parameters and an appropriate test fixture with standard input, output, and feedback resistances.

3. PROCEDURE. The test figures show the connections for the various test conditions. Assume all switches normally closed. The feedback resistance, R_2 for figure 4003-1, shall be no larger than the nominal input impedance nor less than a value which will load the amplifier (100 x Z_{OUT}). Specified stabilization and power supply decoupling shall be added where applicable.

3.1 Common mode input voltage range.

3.1.1 Differential input amplifier. This test shall be an implied measurement. The maximum common mode input voltage specified for the amplifier shall be used in making the common mode rejection ratio test of 3.2.

3.2 Common mode rejection ratio.

$$CMRR = \left| \frac{A_D}{A_C} \right|$$

where A_D = differential gain, and A_C = common-mode gain.

3.2.1 Differential input amplifier using null loop. The test figure is shown on figure 4003-1, all switches are closed. Raise V+, V-, and V_C to V_{CM} volts above nominal (i.e., if V+ = 15, V- = -15, V_C = 0, V_{CM} = 10, then set V+ = 25, V- = -5, and V_C = 10). Measure E_{01}. Lower V+, V-, and V_C to V_{CM} volts below nominal. Measure E_{02}.

$$CMRR = 20 \log \frac{R_1}{R_2} \frac{(E_{01} - E_{02})}{\Delta V_{CM}}$$

3.3 Power supply rejection ratio.

3.3.1 Differential input amplifier. The power supply shall be adjusted for a value equal to the average of the maximum and minimum allowable supply voltage. The signal generator connected to the power supply under test shall be adjusted such that the voltage input at the amplifier under test swings between maximum and minimum specified values. Then:

$$PSRR = 20 \log \frac{R_1}{R_2} \frac{(\Delta V_O)}{\Delta V_{CC}}$$

where: ΔV_0 = Change in output voltage (peak)
ΔV_{CC} = Change in supply voltage (peak)

The frequency used shall be as specified.

3.3.2 Differential input amplifier using null loop. The test figure is shown on figure 4003-1. Set V_C to zero. For +PSRR set V- to constant voltage and set V+ to minimum value and measure E_{01}; set the V+ supplies to maximum values and measure E_{02} .

$$+PSRR = 20 \log \frac{R_1}{R_2} \frac{(E_{02} - E_{01})}{DV_{CC}}$$

where DV_{CC} is the total change in power supply voltage (if the supplies vary from +5 to +20 V, DV_{CC} = 20 - 5 = 15 V). For -PSRR repeat the above measures with V+ supply held constant and V- varied between the minimum and the maximum value, measure E_{03} and E_{04} respectively.

$$-PSRR = 20 \log \frac{R_1}{R_2} \frac{(E_{04} - E_{03})}{DV_{CC}}$$

4. SUMMARY. The following details shall be specified in the applicable acquisition document for specified values of C_1, C_2, R_1, R_2, R_L, and $\pm V_{CC}$ for the nulling amplifier.

a. V_{CM} at specified temperature(s).

b. CMRR at specified temperature(s). V_I signal frequency when applicable.

c. PSRR, when applicable, at specified temperature(s).

d. Test temperature(s). Unless otherwise specified, all parameters shall be measured at the minimum and maximum specified ambient operating temperature and at 25°C ambient.

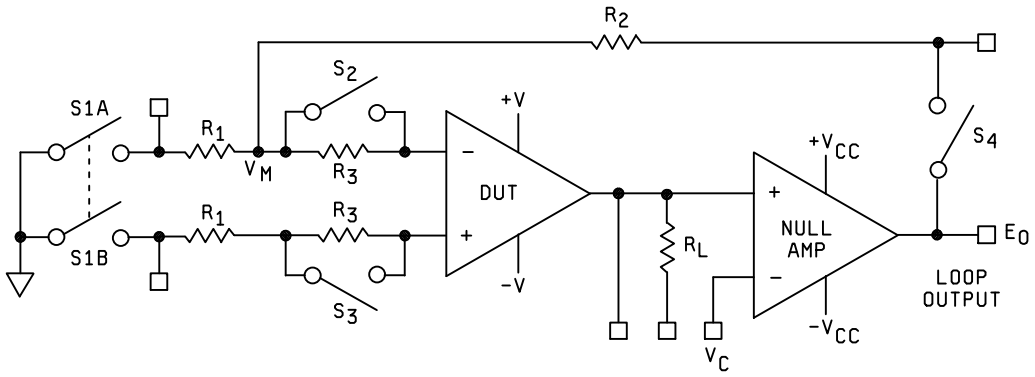

FIGURE 4003-1. Differential input amplifier using null loop.

METHOD 4004.2

OPEN LOOP PERFORMANCE

1. PURPOSE. The purpose of this test procedure is to measure gain, bandwidth, distortion, dynamic range, and input impedance. Gain, dynamic range, and distortion are combined into a large signal test where the distortion measurement will indicate either lack of dynamic range or inherent distortion.

1.1 Definitions. The following definitions shall apply for the purpose of this test method.

1.1.1 Maximum output voltage swing (V_{OP}). The maximum output voltage swing is the maximum peak-to-peak output voltage which can be obtained without waveform clipping when the quiescent dc output voltage is set at a specified reference level. The swing levels are denoted by $+V_{OP}$ and $-V_{OP}$.

1.1.2 Single ended input impedance (Z_{IN}). The single ended input impedance is the ratio of the change in input voltage to the change in input current seen between either input and ground with the other input terminal ac grounded. In case of single input amplifiers, it is the impedance between that terminal and ground. It is measured at the quiescent output dc level.

1.1.3 Differential input impedance (Z_{DI}). The differential input impedance is the ratio of the change in input voltage to the change in input current seen between the two ungrounded input terminals of the amplifier at the quiescent output dc level.

1.1.4 Voltage gain (A_{VS}). The voltage gain (open loop) is the ratio of the output voltage swing to the single ended or differential input voltage, required to drive the output to either swing limit.

1.1.5 Bandwidth, open loop (BW_{01}). The open loop bandwidth is the range of frequencies within which the open-loop voltage gain of the amplifier is not more than 3 dB below the value of the midband open loop gain.

1.1.6 Distortion. The total ratio of the RMS sum of all harmonics to the total RMS voltage at the output for a pure sine wave input.

1.1.7 Unity gain bandwidth (GBW): The unity gain bandwidth is the frequency at which the output voltage is equal to the input voltage.

2. APPARATUS. The apparatus shall consist of appropriate test equipment capable of measuring specified parameters and an appropriate test fixture with standard input, output, and feedback resistances.

3. PROCEDURE. The test figures show the connections for the various test conditions. A differential input is shown, but if a single ended inverting amplifier is under test, the components shown at the positive input terminal shall not be used. If a noninverting amplifier is under test, it shall be necessary to either use fixed bias instead of the dc feedback or to use an inverting gain of one amplifier in the feedback path. For differential output devices, the measurements described in 3.1, 3.2, 3.3, and 3.4 below, as applicable, shall be repeated for the other output using the same test figure except that the measuring equipment shall be connected to the other output.

3.1 Open loop gain using the null loop. The test figure is shown on figure 4004-3. The load resistor R_L is grounded. Set V_C to -10 V and measure E_{01}. Set V_C to +10 V and measure E_{02}.

$$A_{VS} = \frac{R_2}{R_1} \quad \frac{20}{E_{02} - E_{01}}$$

3.2 Distortion. Under the conditions of 3.1, read the distortion on the distortion meter or the voltage at the output of the rejection filter if that is used.

3.3 Maximum output voltage swing. The test figure is shown on figure 4004-3. Set V_C equal to zero. Switches S_1 - S_4 are closed. For $+V_{OP}$ apply a V_1 equal to the positive supply voltage $+V_{OP} = V_2$. For $-V_{OP}$ apply a V_1 equal to the negative supply voltage $-V_{OP} = V_2$.

3.4 Bandwidth. Establish the amplitude of V_2 within the linear region of the device under test at a frequency specified for the measurement of A_D. Increase the frequency, while maintaining the amplifier of V_1 constant, until V_2 reduces to 0.707 of the original value (3 dB down). This frequency shall be measured as the bandwidth for the device under test. The test figure is shown on figure 4004-1.

3.5 Input impedance. This will be specified as a minimum value and shall be measured by observing that the output voltage V_2 does not drop more than 6 dB (2:1 in voltage) when the switch S is opened. This test shall be performed at the specified frequency with a specific amplitude of V_2 within the linear region. R_2 shall be given as the value of the minimum input impedance. The test figure is shown on figure 4004-1.

3.6 Unity gain bandwidth. Increase the frequency of e_I (starting at 100 kHz) until $e_0 = e_I$. The frequency at which this occurs is GBW. The test figure is shown on figure 4004-4. Set the input voltage V_1 to the required device voltage.

4. SUMMARY. The following details shall be specified in the applicable acquisition document for specified values of R_1, R_2, C, $\pm V_{CC}$ for the nulling amplifier, R_3 and R_L.

a. V_{OP}, at specified temperature(s).

b. Z_{IN} (minimum), at specified temperature(s) and frequency.

c. Z_{DI}, where applicable, at specified temperature(s) and frequency.

d. A_{VS}, where applicable, at specified temperature(s) and frequency.

e. A_V, at specified temperature(s) and frequency.

f. BW_{01}, at specified temperature(s).

g. Distortion (%), at specified temperature(s).

h. V_{QI}, when applicable, at specified temperature(s).

i. GBW, at specified temperatures.

j. Test temperature(s). Unless otherwise specified, all parameters shall be measured at the minimum and maximum specified ambient operating temperatures and at 25°C ambient.

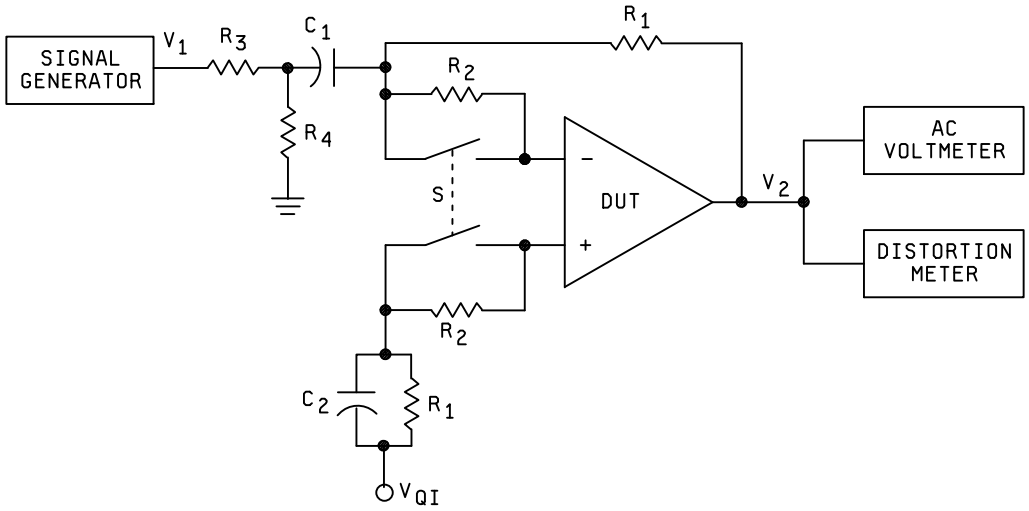

FIGURE 4004-1. Test figure for bandwidth and input impedance.

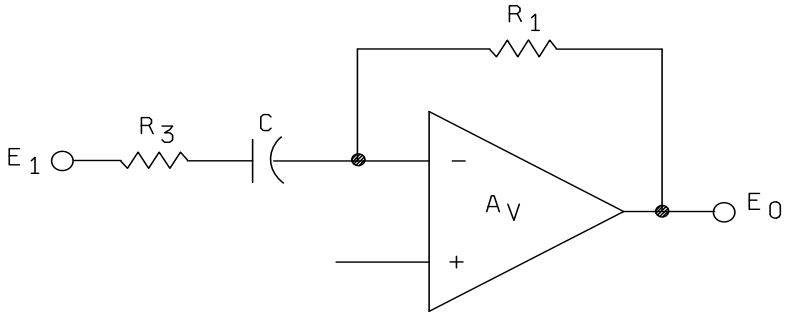

FIGURE 4004-2. Transfer function circuit.

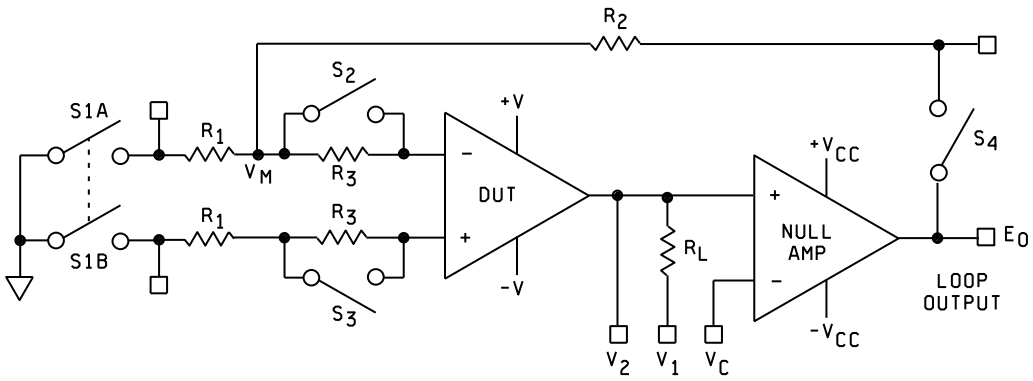

FIGURE 4004-3. Test setup for open loop gain, distortion and maximum output voltage swing.

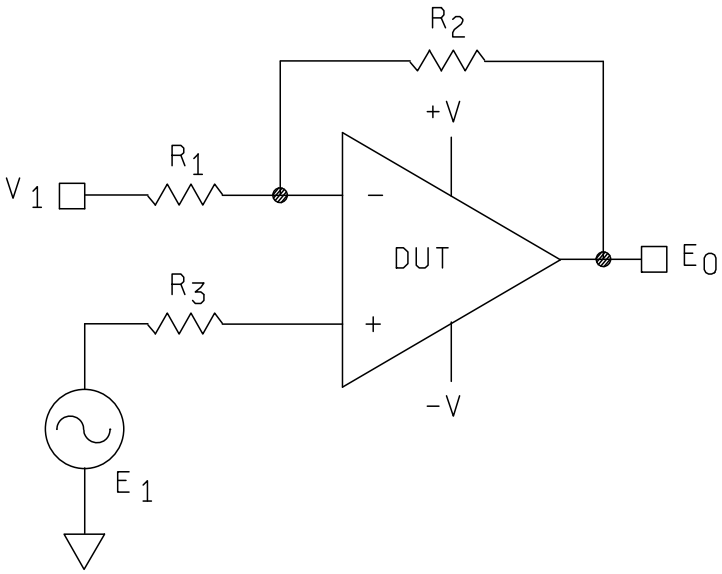

FIGURE 4004-4. Test setup for unity gain bandwidth.

METHOD 4005.1

OUTPUT PERFORMANCE

1. PURPOSE. This method establishes the means for measuring the power dissipation and output impedance.

1.1 Definitions. The following definitions shall apply for the purpose of this test method.

1.1.1 Output impedance (Z_0). The output impedance is the impedance between the output terminal and ground. It is measured at a specific quiescent dc output voltage and with no ac feedback around the amplifier.

1.1.2 Power dissipation (P_D). The power dissipation is the total power dissipated in the amplifier with the amplifier biased into its normal operating range and without any output load.

2. APPARATUS. The apparatus shall consist of appropriate test equipment capable of measuring specified parameters and an appropriate test fixture with standard input, output, and feedback resistances.

3. PROCEDURE. The test figure shown will be used for all three tests. R_1 should be no larger than the nominal input impedance nor less than a value which will load the amplifier (100 x Z_{OUT}). 2 ⦸ f R_1C_1 shall be at least 10 A_D where A_D is the open loop gain and f is the test frequency. C_2 should be at least 10/2 ⦸ f R_2 and R_2 should be about equal to the nominal amplifier Z_0.

3.1 Power dissipation. For this test, the signal generator is off. Measure the positive supply voltage and current V_{CC} and I_C and the negative supply voltage and current V_{EE} and I_E. The power dissipation $P_D = V_{CC}\ I_C + V_{EE}\ I_E$.

3.2 Output impedance. For this test, the signal generator frequency is set to a specified value and the level is set to a specified V_2. V_0 is read on the ac voltmeter. The output impedance is then equal to:

$$Z_O = \frac{V_O \ R_2}{V_2 \ - \ V_0}$$

An alternate measurement would be to make R_2 equal to the maximum acceptable value of Z_0 and require that V_0 be no greater than $V_2/2$. For differential output devices, this measurement shall be repeated for the other output using the same test figure except that the measuring equipment shall be connected to the other output.

4. SUMMARY. The following details shall be specified in the applicable acquisition document for specified values of R_1, R_2, C_1, and C_2.

a. Z_0 limits at the specified frequency.

b. P_D maximum.

c. V_2 where applicable.

d. V_{QI} where applicable at the specified temperature(s).

e. Test temperature(s). Unless otherwise specified, all parameters shall be measured at the minimum and maximum specified operating temperature and at 25°C ambient.

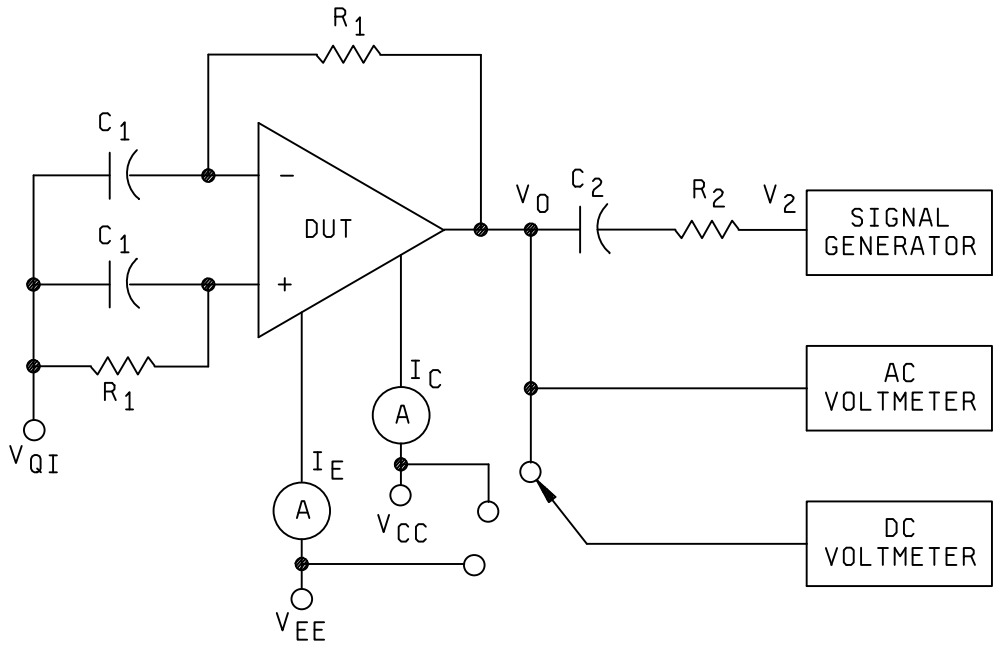

FIGURE 4005-1. Test setup-output performance.

METHOD 4006.2

POWER GAIN AND NOISE FIGURE

1. PURPOSE. The purpose of this test procedure is to measure small signal power gain and the noise figure of an amplifier.

1.1. Definition. The following definitions shall apply for the purpose of this test method.

1.1.1 Power gain (PG). The power gain is the ratio, expressed in dB, of the signal power developed at the output of the amplifier to the signal power applied to the input.

$$PG = 10 \log \frac{P_{OUT}}{P_{IN}}$$

1.1.2 Noise factor (F). The noise factor is the ratio of the signal-to-noise power ratio at the input to the signal-to-noise power ratio at the output.

$$F = \frac{\frac{P_{IN}}{N_{PIN}}}{\frac{P_{OUT}}{N_{POUT}}}$$

Where: P_{IN} = input signal power

P_{OUT} = output signal power

N_{PIN} = input noise power

N_{POUT} = output noise power

1.1.3 Noise figure (NF). The noise figure (NF) is the noise factor (F) expressed in dB.

$$NF = 10 \log F = 10 \log \frac{P_{IN} / N_{PIN}}{P_{OUT} / N_{POUT}}$$

The above expression for NF can be written in terms of voltage since the signal and its associated noise work into the same load.

$$NF = 2o \log \frac{\frac{V_{IN}}{N_{IN}}}{\frac{V_{OUT}}{N_{OUT}}} = 20 \log \frac{V_{IN}}{N_{IN}} - 20 \log \frac{V_{OUT}}{N_{OUT}}$$

Where: V_{IN} = signal voltage IN

V_{OUT} = signal voltage OUT

N_{IN} = noise voltage IN

N_{OUT} = noise voltage OUT

2. APPARATUS. The apparatus shall consist of appropriate test equipment capable of measuring specified parameters and an appropriate test fixture with standard input, output, and feedback resistances.

3. PROCEDURE. The test figures show the connections for the various test conditions. The signal frequency, where applicable, shall be a specified value within the defined bandwidth of the amplifier.

3.1 Power gain. Figure 4006-1 is used for this test. Unless otherwise specified, R_2 shall be equal to the nominal output impedance of the device under test. If the input resistance (R_I) of the device under test is much greater than the source resistance (R_G), unless otherwise specified, a resistor (R) which makes $V_I = 1/2\ V_G$ should be added in series with R_G. The specified ac signal V_G at the specified frequency is applied to the inputs of the amplifier under test. V_I and V_L are recorded. Then:

$$PG(db) = 10 \log \frac{V_L^2}{V_I (V_G - V_I)} x \frac{R_G}{R_2}$$

If the series resistor (R) has been added, then:

$$PG(db) = 10 \log \frac{V_L^2}{V_I (V_G - V_I)} x \frac{R_G'}{R_2}$$

Where: $R_G' = R_G + R$

3.2 Power gain (insertion method). If the input resistance (R_I) to the device under test is known, the power gain can be measured by this procedure. On figure 4006-2 with switch S in position 1, and the attenuator set to zero insertion loss, a reference level is established on the oscilloscope. The switch is then moved to position 2, switching in the circuit under test, and the attenuation increased until the output is brought to the previous reference level. The voltage insertion gain of the circuit under test equals attenuator setting in dB. The power gain is then calculated from the following expression:

$$PG(dB) = (Attenuator\ reading) + 20 \log \frac{R_I (R_G + R_2)}{R_2 (R_G + R_I)}$$

where: R_2 equals the nominal output impedance of the circuit under test.

R_G equals the source resistance.

R_I equals the input impedance of the circuit under test, unless otherwise specified.

The accuracy of this measurement is dependent upon the accuracy of the attenuator.

3.3. Noise figure. Figure 4006-3 is used for this test. The input noise voltage shall be calculated from the following expression:

$$N_{IN} = \sqrt{4KT\Delta f \pm R_G}$$

where: K = Boltzmann's constant (1.38 x 10^{-23} joules/°K)
T = Temperature (°K)
Δf = Noise bandwidth
R_G = Source resistance

The input signal level is then set to ten times (20 dB) N_{IN}. R_X is now adjusted so that the ac voltmeter reads 10 dB on some convenient scale. The input signal V_G is then reduced to zero and the reduction in dB on the output recorded. The noise figure NF is obtained by subtracting this drop in dB from 20 dB. The error in this measurement can be calculated from the following expression:

$$Error\ (dB) = 10 \log \left[\left(\frac{V_{OUT}}{N_{OUT}} \right)^2 + 1 \right] - 20 \log \frac{V_{OUT}}{N_{OUT}}$$

It should be noted that the error will always be in a direction to indicate a lower noise figure than the true noise figure.

3.4 Noise figure, alternate method. In this test, a diode noise generator, as shown on figure 4006-4, is used to measure the noise figure. In this test, with switches S_1 and S_2 in position 1 and the source resistance (R_S) adjusted to a specified value, a reference voltage is read on the ac voltmeter. The switches S_1 and S_2 are then moved to position 2 and the diode source current (I) increased until the previous reference level is read on the ac voltmeter. Using the value of I and R_S, the noise figure is determined for the following expression:

NF = 10 Log 20 IR_S

The accuracy of this technique is established by the accuracy of the 3 dB pad and the current meter in the noise diode circuit.

3.5 Noise factor. The noise factor can be determined from the following expression:

NF = 10 Log F

In this expression, NF is in dB and F is a numeric.

4. SUMMARY. The following details shall be specified in the applicable acquisition document for specified values of R_2 and R_G:

a. PG, at specified temperature(s) and frequency, and R_2.

b. NF, at specified temperature(s) and frequency.

c. F, at specified temperature(s) and frequency.

d. Test temperature(s). Unless otherwise specified, all parameters shall be measured at the minimum and maximum specified ambient operating temperatures and at 25°C ambient.

e. Noise bandwidth (Δf) (see 3.3).

f. R_S (see 3.4).

g. R and R_2, when applicable (see 3.1).

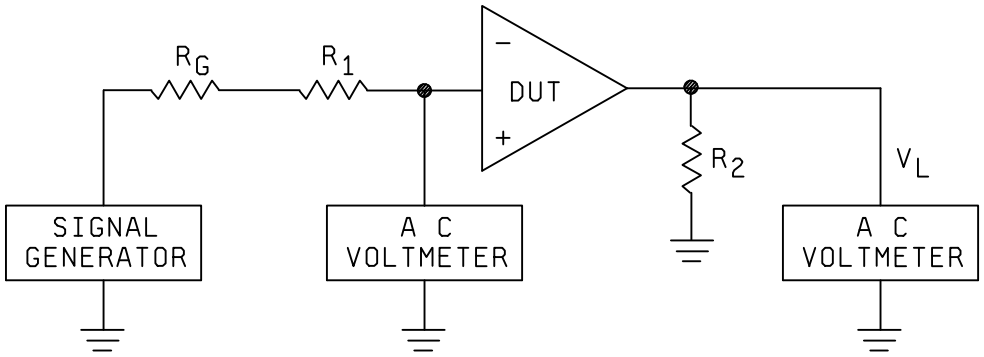

FIGURE 4006-1. Power gain test circuit.

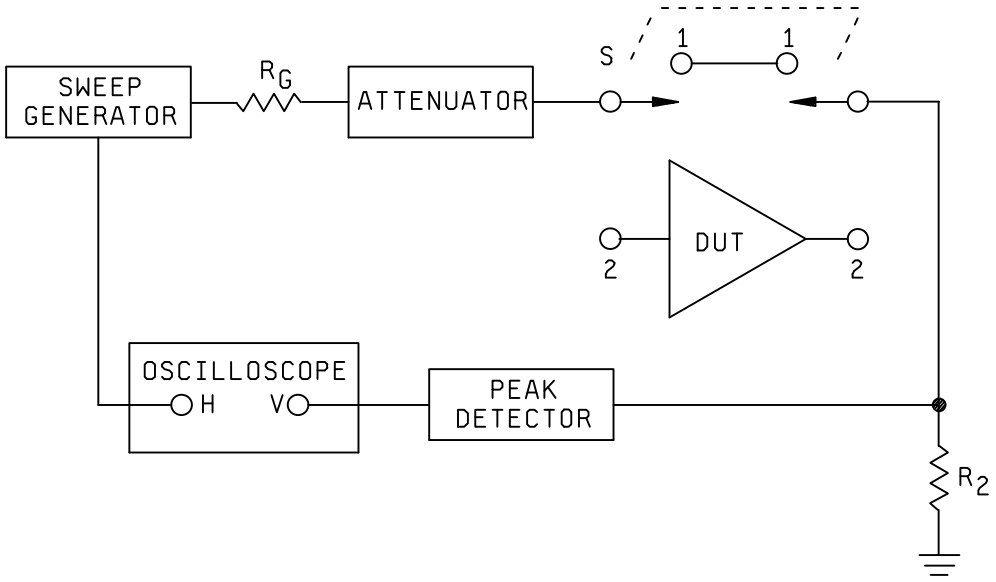

FIGURE 4006-2. Power gain test circuit (insertion method).

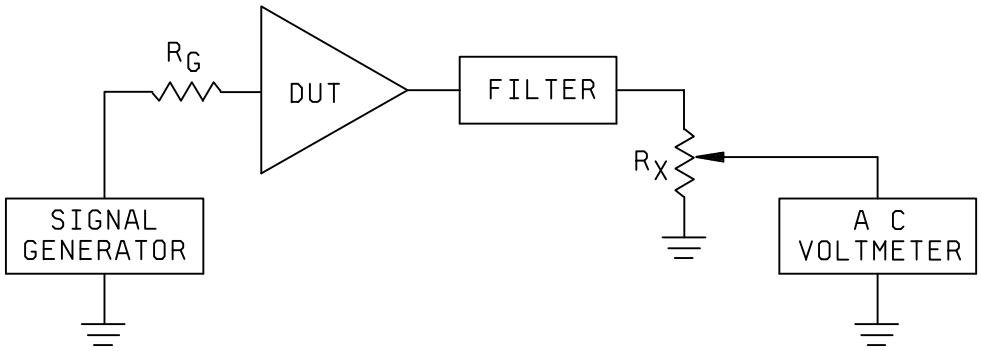

FIGURE 4006-3. Noise figure test circuit.

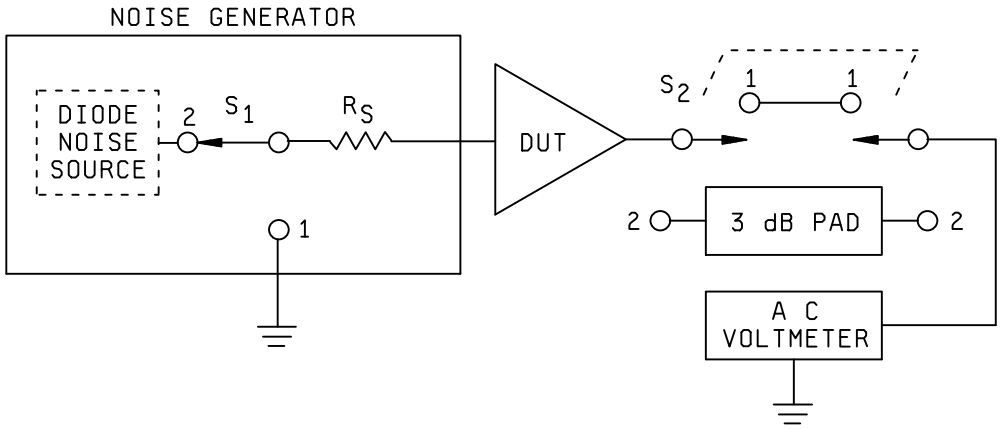

FIGURE 4006-4. Noise figure (double power technique).

This page intentionally left blank

METHOD 4007

AUTOMATIC GAIN CONTROL RANGE

1. PURPOSE. This method establishes the means for measuring the automatic gain control range of a linear amplifier.

1.1 Definitions. The following definition shall apply for the purpose of this test method.

1.1.1 Automatic gain control range (AGC). The AGC range is the total change in voltage gain which may be achieved by application of a specified range of dc voltages to the AGC input terminal of the device.

$$AGC = 20 \log \frac{A_v \ \max}{A_v \ \min}$$

2. APPARATUS. The apparatus shall consist of a sweep generator, voltage source, resistors, capacitors, an ac voltmeter, and a distortion analyzer.

2.1 Sweep generator. The sweep generator must cover the frequency range of the amplifier under test. It shall have an adjustable output level which is flat over the sweep range. It shall be capable of single frequency operation.

2.2 Voltage source. The voltage source shall be capable of supplying the specified AGC voltages to the test circuit. The voltage source shall be free of noise or ripple at its outputs.

2.3 Capacitors and resistors. The capacitors and resistors shall be within 1 per cent or better of the specified values and stable over the test temperature range.

2.4 AC voltmeter. The ac voltmeter shall be capable of measuring the amplifier output voltage without loading and shall have a frequency range that will cover the amplifier under test.

2.5 Distortion analyzer. The distortion analyzer or meter shall be usable over the passband of the amplifier and shall not load the amplifier.

3. PROCEDURE. The test circuit shown on figure 4007-1 shall be used for this test. R_L and C_1 shall be selected to properly load and decouple the circuit, respectively. The AGC voltage is set for maximum gain. The input signal is applied (constant frequency) and increased until the output exhibits maximum allowable distortion. The generator is swept over the prescribed range and the bandwidth noted.

The AGC voltage is varied over the specified range and the reduction in gain is measured. The above measurements are repeated and the bandwidth and signal handling capability recorded.

4. SUMMARY. The following details shall be specified in the applicable acquisition document for specified values of C_1 and R_L.

a. AGC range.

b. Test frequency range.

c. Increase in bandwidth over the AGC range.

d. Maximum reduction in output impedance, where applicable.

e. Minimum reduction in input signal capability, where applicable.

f. Any other variations when applicable, such as power variation, overloading, limitations as to linearity of gain response versus AGC voltage, etc.

g. Test temperature(s). Unless otherwise specified, all parameters shall be measured at the minimum and maximum specified ambient operating temperature and at 25°C ambient.

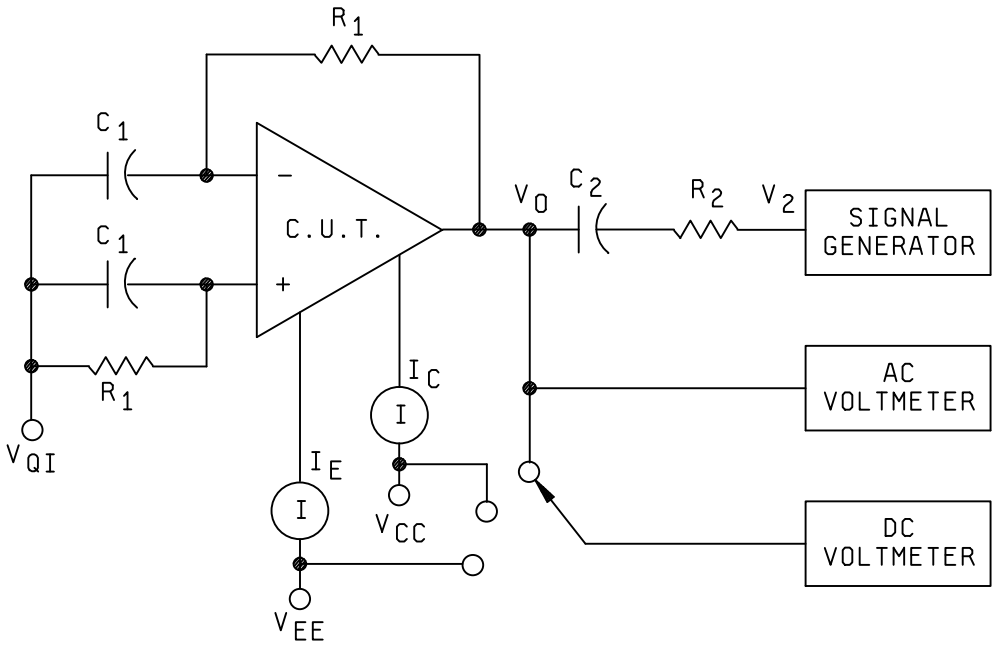

FIGURE 4007-1. AGC test circuit.

This page intentionally left blank

CONCLUDING MATERIAL

Custodians:
Army - CR
Navy - EC
Air Force – 85
NASA – NA
DLA – CC

Preparing activity:
DLA – CC

(Project 5962-2019-008)

Review activities:
Army - AR, EA, MI, SM
Navy – AS, CG, MC, SH
Air Force – 03, 19

NOTE: The activities listed above were interested in this document as of the date of this document. Since organizations and responsibilities can change, you should verify the currency of the information above using the ASSIST Online database at https://assist.dla.mil/.