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MIL-STD-883-2
16 September 2019
SUPERSEDING
MIL-STD-883K
w/CHANGE 3
3 May 2018

DEPARTMENT OF DEFENSE

TEST METHOD STANDARD

MECHANICAL TEST METHODS FOR MICROCIRCUITS

PART 2: TEST METHODS 2000-2999

AMSC N/A

FSC 5962

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FOREWORD

1. This standard is approved for use by all Departments and Agencies of the Department of Defense.

2. This entire standard has been revised. This revision has resulted in many changes to the format, but the most significant one is the splitting the document into parts. See MIL–STD–883 for the change summary.

3. Comment, suggestions, or questions on this document should be addressed to: Commander, Defense Logistics Agency, ATTN: DLA Land and Maritime - VA, P.O. Box 3990, Columbus, OH 43218-3990, or by email to STD883@dla.mil. Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at: https://assist.dla.mil.

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MECHANICAL TESTS

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1. SCOPE

1.1 Purpose. Part 2 of this test method standard establishes uniform test methods for the mechanical testing to determine resistance to deleterious effects of natural elements and conditions surrounding military operations. For the purpose of this standard, the term "devices" includes such items as monolithic, multichip, film and hybrid microcircuits, microcircuit arrays, and the elements from which the circuits and arrays are formed. This standard is intended to apply only to microelectronic devices.

1.2 Numbering system. The test methods are designated by numbers assigned in accordance with the following system:

1.2.1 Classification of tests. The mechanical test methods included in this part of a multipart test method standard are numbered 2001 to 2038 inclusive.

1.2.2 Test method revisions. Revisions are numbered consecutively using a period to separate the test method number and the revision number. For example, 2001.2 designates the second revision of test method 2001.

2. APPLICABLE DOCUMENTS

2.1 General. The documents listed in this section are specified in sections 3, 4, and 5 of this standard. This section does not include documents cited in other sections of this standard or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements documents cited in sections 3, 4, and 5 of this standard, whether or not they are listed.

2.2 Government documents.

2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

MIL-PRF-680 - Degreasing Solvent, Performance Specification For.
MIL-PRF-19500 - Semiconductor Devices, General Specification For.
MIL-PRF-38534 - Hybrid Microcircuits, General Specification For.
MIL-PRF-38535 - Integrated Circuits (Microcircuits) Manufacturing, General Specification For.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-202 - Electronic and Electrical Component Parts.
MIL-STD-750 - Test Methods for Semiconductor Devices.
MIL-STD-1686 - Electrostatic Discharge Control Program for Protection of Electrical and Electronic Parts, Assemblies and Equipment (Excluding Electrically Initiated Explosive Devices).
MIL-STD-1835 - Electronic Component Case Outlines.
MIL-STD-1916 - DOD Preferred Methods for Acceptance of Product.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-217 - Reliability Prediction of Electronic Equipment.
MIL-HDBK-505 - Definitions of Item Levels, Item Exchangeability, Models, and Related Terms.
MIL-HDBK-781 - Reliability Test Methods, Plans, and Environments for Engineering, Development Qualification, and Production .
MIL-HDBK-1331 - Parameters to be Controlled for the Specification of Microcircuits.

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FEDERAL STANDARDS

SAE AMS-STD-595	-	Colors Used in Government Procurement
SAE AMS-STD-595/15102	-	Blue, Gloss
SAE AMS-STD-595/25102	-	Blue, Semi-gloss

OTHER GOVERNMENT DOCUMENTS, DRAWINGS, AND PUBLICATIONS

QML-38534	-	Hybrid Microcircuits, General Specification For.
QML-38535	-	Integrated Circuits (Microcircuits) Manufacturing, General Specification For.

COMMERCIAL ITEM DESCRIPTIONS

A-A-58092	-	Tape, Antiseize, Polytetrafluorethylene.

(Copies of these documents are available online at https://quicksearch.dla.mil.)

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2.3 Non-Government publications. The following documents form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

INTERNATIONAL ORGANIZATION FOR STANDARDIZATION (ISO) STANDARDS

ISO 14644-1	-	Cleanrooms and Associated Controlled Environments – Part 1: Classification of Air Cleanliness.
ISO 14644-2	-	Cleanrooms and Associated Controlled Environments – Part 2: Specifications for Testing and Monitoring to Prove Continued Compliance with ISO 14644-1.
ISO /ASTM 51275	-	Standard Practice for Use of a Radiochromic Film Dosimetry System.

(Copies of these documents are available online at https://www.iso.org)

AMERICAN NATIONAL STANDARDS INSTITUTE (ANSI)

ANSI/NCSL Z540.3	-	Requirements for the Calibration of Measuring and Test Equipment, General Requirements.

(Copies of these documents are available online at https://ansi.org)

IPC - ASSOCIATION CONNECTING ELECTRONICS INDUSTRIES (IPC)

IPC J-STD-004	-	Requirements for Soldering Fluxes.
IPC J-STD-005	-	Requirements for Soldering Pastes.
IPC J-STD-006	-	Requirements for Electronic Grade Solder Alloys and Fluxed and Non-fluxed Solid Solders for Electronic Soldering Applications.
IPC J-STD-033	-	Handling, Packing, Shipping and Use of Moisture/Reflow Sensitive Surface Mount Devices.
IPC-T-50	-	Terms and Definitions for Interconnecting and Packaging Electronic Circuits.

(Copies of these documents are available online at https://www.ipc.org)

JEDEC SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC).

JEDEC JESD22-B116	-	Wire Bond Shear Test
JEDEC JESD78	-	IC Latch-up Test.
JEDEC JESD213	-	Common Test Method for Detection Component Surface Finish Material.
JEDEC Standard 12	-	Standard for Gate Array Benchmark Set
JEDEC Standard 12-1	-	Terms and Definitions for Gate Array Benchmark Set.
JEDEC Standard 12-2	-	Standard for Cell-Based Integrated Circuit Benchmark Set.
JEDEC Standard 12-3	-	CMOS Gate Array Macrocell Standard.

(Copies of these documents are available online at https://www.jedec.org)

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NATIONAL COUNCIL ON RADIAATION PROTECTION AND MEASUREMENT

Report Number 40	-	Protection Against Radiation from Brachytherapy Sources
Report Number 102	-	Medical X-ray, Electron Beam and Gamma Ray Protection

(Copies of these documents are available online at http://www.NCRPPublications.org)
TECHSTREET THOMPSON REUTERS

TechAmerica EIA-557	-	Statistical Process Control Systems.

(Copies of these documents are available online at https://www.techstreet.com)

AMERICAN SOCIETY FOR TESTING AND MATERIALS (ASTM)

ASTM C 177	-	Standard Test Method for Steady-State Heat Flux Measurements and Thermal Transmission Properties by Means of the Guarded Hot-Plate Apparatus.
ASTM C 518	-	Standard Test Method for Steady-State Heat Flux Measurements and Thermal Transmission Properties by Means of the Heat Flow Meter Apparatus.
ASTM D 150	-	Standard Test Methods for A-C Loss Characteristics and Permittivity (Dielectric Constant) of Solid Electrical Insulating Materials.
ASTM D 257	-	Standard Test Methods for D-C Resistance or Conductance of Insulating Materials.
ASTM D 877	-	Standard Test Methods for Dielectric Breakdown Voltage of Insulating Liquids Using Disk Electrodes.
ASTM D 971	-	Interfacial Tension of Oil Against Water by the Ring Method.
ASTM D 1002	-	Standard Test Method for Strength Properties of Adhesives in Shear by Tension Loading (Metal-to-Metal).
ASTM D 1120	-	Engine Coolant, Boiling Point of.
ASTM D 1331	-	Standard Test Methods for Surface and Interfacial Tension of Solutions of Surface-Active Agents.
ASTM D 2109	-	Standard Test Methods for Nonvolatile Matter in Halogenated Organic Solvents and their Admixtures.
ASTM D 3574	-	Materials, Flexible Cellular-Slab, Bonded, and Molded Uretane Foam.
ASTM D 3850	-	Rapid Thermal Degradation of Solid Electrical Insulating Materials by Thermogravimetric Method, Test Method for.
ASTM E 263	-	Standard Test Method for Measuring Fast-Neutron Reaction Rates by Radioactivation of Iron.
ASTM E 264	-	Standard Test Method for Measuring Fast-Neutron Reaction Rates by Radioactivation of Nickel.
ASTM E 265	-	Standard Test Method for Measuring Reaction Rates and Fast-Neutron Fluences by Radioactivation of Sulfur-32.
ASTM E 666	-	Standard Practice for Calculating Absorbed Dose from Gamma or X-Radiation.
ASTM E 668	-	Standard Practice for Application of Thermoluminescence-Dosimetry (TLD) Systems for Determining Absorbed Dose on Radiation Hardness Testing of Electronic Devices.
ASTM E 720	-	Standard Guide for Selection and Use of Neutron Sensors for Determining Neutron Spectra Employed in Radiation-Hardness Testing of Electronics.
ASTM E 721	-	Standard Method for Determining Neutron Energy Spectra with Neutron-Activation Foils for Radiation-Hardness Testing of Electronics.
ASTM E 722	-	Standard Practice for Characterizing Neutron Energy Fluence Spectra in Terms of an equivalent Monoenergetic Neutron Fluence for Radiation-Hardness Testing of Electronics.

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AMERICAN SOCIETY FOR TESTING AND MATERIALS (ASTM) (CONTINUED)

ASTM E 801	-	Standard Practice for Controlling Quality of Radiological Examination of Electronic Devices.
ASTM E 831	-	Standard Test Method for Linear Thermal Expansion of Solid Materials by Thermomechanical Analysis
ASTM E 1249	-	Minimizing Dosimetry Errors in Radiation Hardness Testing of Silicon Electronic Devices.
ASTM E 1250	-	Standard Method for Application of Ionization Chambers to Assess the Low Energy Gamma Component of Cobalt 60 Irradiators Used in Radiation Hardness Testing of Silicon Electronic Devices.
ASTM E 2450	-	Standard Practice for Application of CaF_2(Mn) Thermoluminescence Dosimeters in Mixed Neutron-Photon Environments.
ASTM F 458	-	Standard Practice for Nondestructive Pull Testing of Wire Bonds.
ASTM F 459	-	Standard Test Methods for Measuring Pull Strength of Microelectronic Wire Bonds.
ASTM F 526	-	Standard Test Method for Measuring Dose for Use in Linear Accelerator Pulsed Radiation Effects Tests.
ASTM F 1192	-	Standard Guide for the Measurement of Single Event Phenomena (SEP).
ASTM F 1892	-	Standard Guide for Ionizing Radiation (Total Dose) Effects Testing of Semiconductor Devices.

(Copies of these documents are available online at https://www.astm.org/)

2.4 Order of precedence. Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. DEFINITIONS

3.1 Abbreviations, symbols, and definitions. For the purpose of this standard, the abbreviations, symbols, and definitions specified in MIL-PRF-19500, MIL-PRF-38535, or MIL-HDBK-505 apply. The following definitions also apply:

3.1.1 Microelectronic device. A microcircuit, microcircuit module, or an element of a microcircuit as defined in appendix A of MIL-PRF-38535. For the purposes of this document, each type of microelectronic device will be identified by a unique type, or drawing number.

3.1.2 Mode of failure. The cause for rejection of any failed device or microcircuit as defined in terms of the specific electrical or physical requirement which it failed to meet (i.e., no failure analysis is required to identify the mode of failure, which should be obvious from the rejection criteria of the test method).

3.1.3 Mechanism of failure. The original defect which initiated the microcircuit or device failure or the physical process by which the degradation proceeded to the point of failure, identifying quality defects, internal, structural, or electrical weakness and, where applicable, the nature of externally applied stresses which led to failure.

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3.1.4 Absolute maximum ratings. The values specified for ratings, maximum ratings, or absolute maximum ratings are based on the "absolute system" and are not to be exceeded under any measurable or known service or conditions. In testing microelectronic devices, limits may be exceeded in determining device performance or lot quality, provided the test has been determined to be nondestructive and precautions are taken to limit device breakdown and avoid conditions that could cause permanent degradation. These ratings are limiting values beyond which the serviceability of any individual microelectronic integrated circuit may be impaired. It follows that a combination of all the absolute maximum ratings cannot normally be attained simultaneously. Combinations of certain ratings are permissible only if no single maximum rating is exceeded under any service condition. Unless otherwise specified, the voltage, current, and power ratings are based on continuous dc power conditions at free air ambient temperature of 25°C ±3°C. For pulsed or other conditions of operation of a similar nature, the current, voltage, and power dissipation ratings are a function of time and duty cycle. In order not to exceed absolute ratings, the equipment designer has the responsibility of determining an average design value, for each rating, below the absolute value of that rating by a safety factor, so that the absolute values will never be exceeded under any usual conditions of supply-voltage variations, load variations, or manufacturing variations in the equipment itself.

3.1.5 Worst case condition. Worst case condition(s) consists of the simultaneous application of the most adverse (in terms of required function of the device) values (within the stated operating ranges) of bias(es), signal input(s), loading and environment to the device under test. Worst cases for different parameters may be different. If all the applied test conditions are not established at the most adverse values, the term "partial worst case condition" should be used to differentiate and should be accompanied by identification of the departure from worst case. For example, the lowest values of supply voltages, signal input levels, and ambient temperature and the highest value of loading may constitute "worst case conditions" for measurement of the output voltage of a gate. Use of the most adverse values of applied electrical conditions, at room temperature, would then constitute "partial worst case conditions" and should be so identified using a postscript "at room temperature."

3.1.5.1 Accelerated test condition. Accelerated test conditions are defined as test conditions using one or more applied stress levels which exceed the maximum rated operating or storage stress levels but are less than or equal to the "Testing Rating" values.

3.1.6 Static parameters. Static parameters are defined as dc voltages, dc currents, or ratios of dc voltages or dc currents, or both.

3.1.7 Dynamic parameters. Dynamic parameters are defined as those which are rms or time-varying values of voltages or currents, or ratios of rms or time-varying values of voltages or currents, or both.

3.1.8 Switching parameters. Switching parameters are defined as those which are associated with the transition of the output from one level to another or the response to a step input.

3.1.9 Functional tests. Functional tests are defined as those go, no-go tests which sequentially exercise a function (truth) table or in which the device is operated as part of an external circuit and total circuit operation is tested.

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3.1.10 Acquiring activity. The acquiring activity is the organizational element of the Government which contracts for articles, supplies, or services; or it may be a contractor or subcontractor when the organizational element of the Government has given specific written authorization to such contractor or subcontractor to serve as agent of the acquiring activity. A contractor or subcontractor serving as agent of the acquiring activity does not have the authority to grant waivers, deviations, or exceptions unless specific written authorization to do so has also been given by the Government organization.

3.1.11 Accuracy. The quality of freedom from error. Accuracy is determined or assured by calibration, or reliance upon calibrated items.

3.1.12 Calibration. Comparison of measurement standard or instrument of known accuracy with another standard, instrument or device to detect, correlate, report or eliminate by adjustment, any variation in the accuracy of the item being compared. Use of calibrated items provide the basis for value traceability of product technical specifications to national standard values. Calibration is an activity related to measurement and test equipment performed in accordance with ANSI/NCSL Z540.3 or equivalent.

3.1.13 Precision. The degree to which an instrument, device, assemblage, test, measurement or process exhibits repeatability. Expressed statistically or through various techniques of Statistical Process Control (SPC). Term is used interchangeably with "repeatability".

3.1.14 Resolution. The smallest unit of readability or indication of known value in an instrument, device or assemblage thereof.

3.1.15 Standard reference material (SRM). A device or artifact recognized and listed by the National Institute of Standards and Technology (NIST) as having known stability and characterization. SRM's used in product testing provide traceability for technical specifications. SRM's do not require calibration when used and stored in accordance with NIST accompanying instructions. They are used as "certified materials".

3.1.16 Tolerance. A documented range over which a specified value may vary.

3.1.17 Test accuracy ratio (TAR). A ratio of the tolerance of the device under test to the accuracy of the related measuring or test instrument or to the accuracy of the correlation device/SRM.

3.1.18 Uncertainty. An expression of the combined errors in a test measurement process. Stated as a range within which the subject quantity is expected to lie. Comprised of many components including: estimates of statistical distribution and results of measurement or engineering analysis. Uncertainty established with a suitable degree of confidence, may be used in assuring or determining product conformance and technical specifications.

3.1.19 Susceptibility. The point at which a device fails to meet the postirradiation end-point electrical parameter limits or fails functionally during radiation exposure (e.g., neutron irradiation).

3.1.20 Class M. Class M is defined as 1.2.1 of MIL-STD-883 basic compliant product or product built in compliance to Appendix A of MIL-PRF-38535 documented on a Standard Microcircuit Drawing where configuration control is provided by the Government preparing activity. Class M devices are required to use the conditions specified in the test methods herein for class level B product.

3.1.21 Class level B and class level S. 2 class levels are used in this document to define requirements for high reliability military applications (Class level B) and space applications (Class level S). Class level B requirements contained in this document are intended for use for Class Q, Class H, and Class M products, as well as Class B M38510 JAN slash sheet product. Class level B requirements are also intended for use for product claimed as 883 compliant or 1.2.1 compliant for high reliability military applications. Class level S requirements contained in this document are intended for use for Class V, Class K, as well as M38510 Class S JAN slash sheet product. Class level S requirements are also intended for use for product claimed as 883 compliant or 1.2.1 of MIL-STD-883 basic compliant for space level applications.

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3.1.22 Acquisition documents. Acquisition documents consist of the acquisition order or contract, device specification (e.g. SMD's, SCD's) or specifications as applicable.

4. GENERAL REQUIREMENTS

4.1 General. Unless otherwise specified in the individual test method, the general requirements of MIL-STD-883 shall apply.

4.2 Test circuits. The test circuits shown in the test methods of this test method standard are given as examples which may be used for the measurements. They are not necessarily the only test circuits which can be used; however the manufacturer shall demonstrate to the Government that other test circuits which they may desire to use will give results within the desired accuracy of measurement.

4.3 Destructive tests. Unless otherwise demonstrated, the test methods listed in table I shall be classified as destructive. MIL-STD-883 covers the necessary actions needed to reclassify a test method as non-destructive.

TABLE I. Destructive tests.

Test method number	Test
2003	Solderability
2004	Lead Intergrity
2007	Vibration, variable frequency
2011	Bond strength
2014	Internal visual and mechanical
2018	Scanning electron microscope (SEM) inspection of metalization
2019	Die shear strength
2024	Lid torque for glass-frit-sealed packages
2025	Adhesion of lead finish
2038	Solder column package destructive lead pull test

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4.4 Non–destructive tests. Unless otherwise demonstrated, the test methods listed in table II shall be classified as nondestructive.

TABLE II. Non-destructive tests.

Test method number	Test
2009	External visual
2010	Internal visual (monolithic)
2012	Radiography
2015	Resistance to solvents
2016	Physical dimensions
2020	Particle impact noise detection test
2023	Nondestructive bond pull

4.5 Laboratory suitability. Prior to processing any microcircuit intended for use in any military system or sub-system, the facility performing the test(s) shall be audited by the DLA Land and Maritime, Sourcing and Qualification Division and be granted written laboratory suitability status for each test method to be employed. Processing of any devices by any facility without laboratory suitability status for the test methods used shall render the processed devices nonconforming.

4.6 Method of reference. When applicable, test methods contained herein shall be referenced in the individual specification or specification sheet by specifying the test method number and, the details required in the summary of the applicable test method shall be listed. To avoid the necessity for changing documents that refer to test methods of this standard, the revision number should not be used when referencing test methods. (For example: Use 1001 versus 1001.2.)

5. DETAILED REQUIREMENTS

This section is not applicable to this standard.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory.)

6.1 Intended use. The intended use of this test method standard is to establish appropriate conditions for testing semiconductor devices to give test results that simulate the actual service conditions existing in the field. This test method standard has been prepared to provide uniform test methods, controls, and procedures for determining with predictability the suitability of such devices within military, aerospace and special application equipment.

6.2 International standardization agreement. Certain provisions of this test method standard are the subject of international standardization agreement. When amendment, revision, or cancellation of this test method standard is proposed which will affect or violate the international agreement concerned, the preparing activity will take appropriate reconciliation action through international standardization channels, including departmental standardization offices, if required.

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6.3 Subject term (key word) listing

Destructive tests
Environmental tests
Laboratory suitability
Non–destructive tests

6.4 Supersession data The main body and five parts (–1 through –5) of this revision of MIL-STD-883 replace superseded MIL–STD–883K

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METHOD 2001.4

CONSTANT ACCELERATION

1. PURPOSE. This test is used to determine the effects of constant acceleration on microelectronic devices. It is an accelerated test designed to indicate types of structural and mechanical weaknesses not necessarily detected in shock and vibration tests. It may be used as a high stress test to determine the mechanical limits of the package, internal metallization and lead system, die or substrate attachment, and other elements of the microelectronic device. By establishing proper stress levels, it may also be employed as an in-line 100 percent screen to detect and eliminate devices with lower than nominal mechanical strengths in any of the structural elements.

2. APPARATUS. Constant acceleration tests shall be made on an apparatus capable of applying the specified acceleration for the required time.

3. PROCEDURE. The device shall be restrained by its case, or by normal mountings, and the leads or cables secured. Unless otherwise specified, a constant acceleration of the value specified shall then be applied to the device for 1 minute minimum in each of the orientations X_1, X_2, Y_1,Y_2, Z_1, and Z_2 (see note 1). For devices with internal elements mounted with the major seating plan perpendicular to the Y axis, the Y_1 orientation shall be defined as that one in which the element tends to be removed from its mount. Unless otherwise specified, test condition E shall apply. Note: The “Stress level(s)” are absolute minimums with no lower tolerances. The spin radius shall be from the center of the rotor to the 1st point of element attachment. See Figure 2001-1.

Note 1: Dual cavity devices may require multiple spins with the device orientation reversed to properly stress the device.

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Test condition	Stress level (g)
A	5,000
B	10,000
C	15,000
D	20,000
E	30,000
F	50,000
G	75,000
H	100,000
J	125,000

4. SUMMARY. The following details shall be specified in the applicable acquisition document:

   a. Amount of acceleration to be applied, in gravity units (g) if other than test condition E (see 3).

   b. When required, measurements to be made after test.

   c. Any variations in duration or limitations to orientation (e.g., Y_1 only) (see 3).

   d. Sequence of orientations, if other than as specified (see 3).

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g = acceleration to be applied in gravity units

ω = revolutions per minute

r = radius in inches (center of rotor to the 1st point of element attachment)

$g = 2.8416 \times 10^{-5} r\omega^2$ or g force = Radius in inches x RPM^2 x 2.8416×10^{-5}
$\omega = (g/2.8416 \times 10^{-5} r)^{1/2}$ or $RPM = (g\ force/Radius\ in\ inches \times 2.8416 \times 10^{-5})^{1/2}$
$r = g/(2.8416 \times 10^{-5} \omega^2)$ or Radius = g force/(RPM^2 x 2.8416×10^{-5})

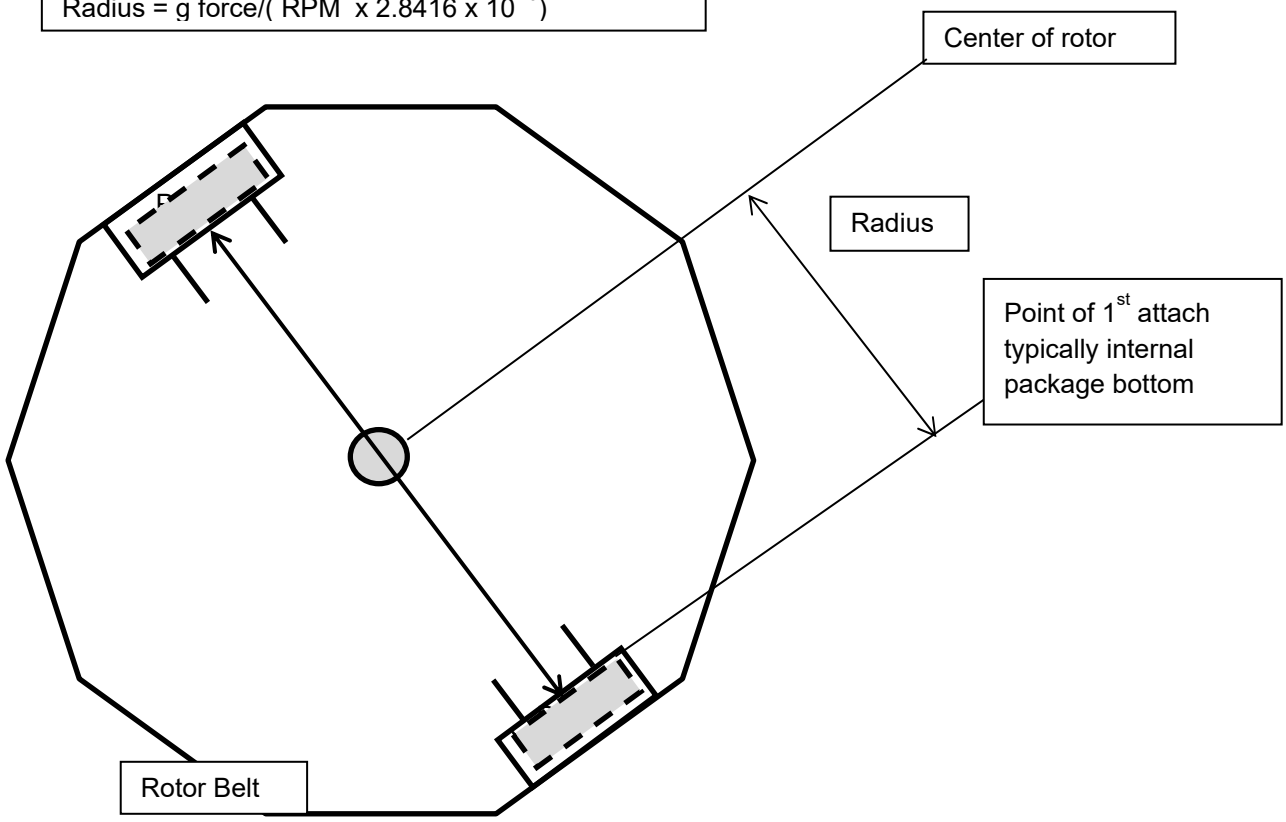

FIGURE 2001-1.Center of Rotation

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METHOD 2002.5

MECHANICAL SHOCK

1. PURPOSE. The shock test is intended to determine the suitability of the devices for use in electronic equipment which may be subjected to moderately severe shocks as a result of suddenly applied forces or abrupt changes in motion produced by rough handling, transportation, or field operation. Shocks of this type may disturb operating characteristics or cause damage similar to that resulting from excessive vibration, particularly if the shock pulses are repetitive.

2. APPARATUS. The shock-testing apparatus shall be capable of providing shock pulses of 500 to 30,000 g (peak) as specified with a pulse duration between 0.1 and 1.0 millisecond, to the body of the device. The acceleration pulse shall be a half-sine waveform with an allowable distortion not greater than ±20 percent of the specified peak acceleration, and shall be measured by a transducer and optional electronic filter with a cut-off frequency of at least 5 times the fundamental frequency of the shock pulse. The pulse duration shall be measured between the points at 10 percent of the peak acceleration during rise time and at 10 percent of the peak acceleration during decay time. Absolute tolerances of the pulse duration shall be the greater of ±0.1 millisecond or ±30 percent of the specified duration.

3. PROCEDURE. The shock-testing apparatus shall be mounted on a sturdy laboratory table or equivalent base and leveled before use. The device shall be rigidly mounted or restrained by its case with suitable protection for the leads. Means may be provided to prevent the shock from being repeated due to "bounce" in the apparatus. Unless otherwise specified, the device shall be subject to 5 shock pulses of the peak (g) level specified in the selected test condition and for the pulse duration specified in each of the orientations X_1, X_2, Y_2, Y_1, Z_1, and Z_2. For devices with internal elements mounted with the major plane perpendicular to the Y axis, the Y_1 orientation shall be defined as that one in which the element tends to be removed from its mount. Unless otherwise specified, test condition B shall apply. Note: The “g level (peak) limits are absolute minimums with no lower tolerances.

Test condition	g level (peak)	Duration of pulse (ms)
A	500	1.0
B	1,500	0.5
C	3,000	0.3
D	5,000	0.3
E	10,000	0.2
F	20,000	0.2
G	30,000	0.12

CAUTIION: If this test is performed using a potting compound type test fixture (e.g., waterglass/sodium silicate) the facility performing the test shall assure that this procedure/material does not mask fine/gross leakers.

3.1 Examination. After completion of the test, an external visual examination of the marking shall be performed without magnification or with a viewer having a magnification no greater than 3X and a visual examination of the case, leads, or seals shall be performed at a magnification between 10X and 20X. This examination and any additional specified measurements and examination shall be made after completion of the final cycle or upon completion of a group, sequence, or subgroup of tests which include this test.

3.2 Failure criteria. After subjection to the test, failure of any specified measurements or examination (see 3 and 4), evidence of defects or damage to the case, leads, or seals, or illegible markings shall be considered a failure. Damage to marking caused by fixturing or handling during tests shall not be cause for device rejection.

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4. SUMMARY. The following details shall be specified in the applicable acquisition document:

   a. Test condition, if other than test condition B (see 3).
   b. Number and direction of shock pulses, if other than specified (see 3).
   c. Electrical-load conditions, if applicable (see 3).
   d. When required, measurement made after test (see 3 and 3.1).
   e. When required, measurement during test.

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METHOD 2003.13

SOLDERABILITY

1. PURPOSE. The purpose of this test method is to provide a referee condition for the evaluation of the solderability of terminations (including leads up to 0.125 inch in diameter) that will be assembled using tin lead eutectic solder. This evaluation is made on the basis of the ability of these terminations to be wetted and to produce a suitable fillet when coated by tin lead eutectic solder. These procedures will test whether the packaging materials and processes used during the manufacturing operations produce a device that can be successfully soldered to the next level assembly using tin lead eutectic solder. A preconditioning test is included in this test method, which degrades the termination finish to provide a guard band against marginal finishes.

1.1 Terms and definitions. The definition of terms shall be in accordance with the following:

1.1.1 Solderability. The property of a metal to be wetted by molten solder.

1.1.2 Wetting. The formation of a relatively uniform, smooth and unbroken film of solder, adherent to the surface of the base metal tested.

1.1.3 Nonwetting. A condition whereby a surface has contacted molten solder, but the solder has not adhered to all of the surface, leaving the surface base metal partially or totally exposed. See Figure 2003-1.

1.1.4 Pinholes. Holes occurring as imperfections that penetrate entirely through the solder layer. See Figure 2003-2.

1.1.5 Dewetting. A condition that results when molten solder has coated a surface and then receded leaving irregularly shaped mounds of solder separated by areas covered with a thin solder film, and where the base metal is not exposed. See Figure 2003-3.

1.1.6 Foreign material. Particles of material located on, but different from, the lead material or coating.

1.1.7 DIP. Dual In-line Package.

1.1.8 TO. Transistor Outline.

1.1.9 PGA. Pin Grid Array.

1.1.10 QFP. Quad Flat Pack.

1.1.11 LCC. Leadless Chip Carrier.

1.1.12 LGA. Land Grid Array.

1.1.13 QFN. Quad Flat No-lead.

2. APPARATUS.

2.1 Solder pot. A thermostatically controlled static solder vessel of sufficient size to contain at least two pounds of solder. The solder shall be static during the dipping procedure. The apparatus shall be capable of maintaining the solder at the temperature specified in 4.4.1.2

2.2 Dipping mechanism. A dipping mechanism capable of controlling the rates of immersion and emersion of the terminations and providing a dwell time (total time at the required depth) in the solder bath as specified in 4.4.1.2. It is also capable of orienting and dipping the device to meet the dipping requirements. The specimen holder shall be designed to minimize the trapping of flux.

2.3 Ceramic substrate. A thin unmetallized ceramic substrate with a thickness range of 0.025 inch to 0.035 inch (used for testing of ball grid arrays).

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2.4 Metallized substrate. A substrate made of glass-reinforced epoxy (e.g., FR-4) with metallized pads (e.g., Electroless Nickel Immersion Gold). The pad diameter shall be at least 0.010 inch larger than the column diameter (used for testing of column grid arrays).

2.5 Screen print stencil. A metal (or other acceptable material, such as plastic) stencil with pad geometry openings appropriate for the device being tested. Alternative dispense systems may be used that do not use a stencil or squeegee (e.g., jet printing). Unless otherwise agreed upon between vendor and user, the nominal stencil thickness shall be 0.004 inch (for lead pitch < 0.020 inch),
0.006 inch (for lead pitch ≥ 0.020 inch and up to 0.025 inch), and 0.008 inch (for lead pitch > 0.025 inch).

2.6 Squeegee. A rubber, plastic, or metal tool used to print the solder paste. This is not applicable if alternative dispense systems (e.g., jet printing) are used.

2.7 Base fixture. A fixture designed to hold the substrate and aid in the alignment of the screen print stencil.

2.8 Reflow equipment. A forced-convection reflow oven or equivalent reflow system capable of achieving the recommended reflow profile.

2.9 Cutting equipment. A system capable of cutting the columns without excessive burrs and without damaging the columns (e.g., diamond wire saw).

2.10 Optical equipment. A stereo optical system capable of providing a minimum magnification of 10x.

2.11 Lighting equipment. A lighting system that will provide a uniform, non-glare, non-directional illumination of the device.

2.12 Steamaging equipment. A non-corrodible container and cover of sufficient size to allow the placement of devices inside the vessel. The devices shall be placed such that the lowest portion of the device is a minimum of 1.5 inches above the surface of the water. A suitable method of supporting the devices shall be improvised using non-contaminating material. The apparatus shall be capable of having the specified temperature verified.

2.12.1 Cleaning of the system. The apparatus shall be drained and cleaned at least once per month or prior to use. A more frequent cleaning cycle may be necessary as indicated by resistivity, visual, or general cleanliness of the water. No contaminating solvents shall be used.

2.13 High-temperature bake equipment. A bake oven of sufficient size and capable of continuously maintaining 150°C ± 5°C temperature control shall be used.

3. MATERIALS. All chemicals shall be of commercial grade or better. Fresh solvents shall be used as often as is necessary to preclude contamination.

3.1 Flux. The flux shall be a standard activated rosin flux having a composition of 25% ± 0.5% by weight of Colophony (rosin) and 0.15% ± 0.01% by weight diethylamine hydrochloride (CAS 660-68-4), in 74.85% ± 0.05% by weight of isopropyl alcohol. Z. When specified by the procuring activity low activity fluxes labeled conforming to ROL0, ROL1, or RMA may be substituted.

3.2 Solder. The solder shall conform to type Sn63Pb37, Sn60Pb40, or equivalent.

3.3 Solder paste. The solder paste shall be Sn60Pb40, Sn63Pb37, or equivalent, with mesh size of -325/+500, flux type ROL1. The solder paste shall meet the storage and shelf life requirements of the manufacturer's specification.

3.4 Cleaning solution. Solutions used for flux removal shall be compatible with the device and the metallized substrate.

3.5 Isopropyl alcohol. Commercial grade isopropyl alcohol or better shall be used.

3.6 Water. The water to be used for steamaging purposes shall be either distilled or deionized.

WARNING: These materials may involve substances that are flammable, toxic to eyes, skin, or respiratory tract, or present a serious burn potential. Eye and skin protection should be used. Heat resistant gloves should be used when handling hot objects.

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4. PROCEDURE. The test procedure shall be performed on the number of terminations specified in the acquisition document. If no number is specified then the sample size shall be 22(0). The test may be performed just prior to packaging for storage or shipment, immediately upon removal from the manufacturer's protective packaging, or as a qualification or quality conformance test. The samples shall have the lead finish that is to be supplied to the customer. (e.g if gold and solder finish are supplied, both finishes shall be tested). The sample shall be selected at random using at least 3 different devices. During handling, special care shall be exercised to prevent the surfaces being tested from being abraded or contaminated by grease, perspiration, or abnormal atmospheres. The test procedure shall consist of the following operations:

a. Proper preparation of the specimens (see 4.1), if applicable.
b. Preconditioning of all specimens (see 4.2).
c. Solderability test (see 4.4).
d. Examination and evaluation of the tested portions of the terminations upon completion of the solder dip process (see 4.5).

4.1 Preparation of terminations. No wiping, cleaning, scraping, or abrasive cleaning of the terminations shall be performed prior to testing. Any special preparation of the terminations, such as bending or reorientation prior to the test, shall be specified in the acquisition document.

4.2. Preconditioning categories. The preconditioning categories shall be as follows:

a. Category A – All device finishes, which have no gold or tin content specified (Steamage for 1 hour ± 5 min)
b. Category B – Column grid arrays (Steamage for 4 hours ± 10 min)
c. Category C – For all other device finishes, including gold (Steamage for 8 hours ± 15 min)
d. Category D – For LGAs (Dry-bake for 4 hours ± 15 min)

4.2.1 Steamaging. (Catagories A, B,and C) Prior to the application of the flux and subsequent solder dips, specimens shall be subjected to aging by exposure of the surfaces to be tested to water vapor (see 4.2) in the apparatus specified in 2.12. The water vapor temperature at the device lead level shall be in accordance with table I. Aging may be interrupted once for 10 minutes maximum. The devices shall be removed from the test apparatus upon completion of the specified test period.

4.2.1.1 Drying and storage procedures. Upon removal of test specimens from the steamaging apparatus following preconditioning, the devices shall be dried (if applicable) using one of these two procedures:

a. Bake at 100ºC maximum for no more than 1 hour in a dry atmosphere (dry nitrogen atmosphere is recommended).
b. Air dry at ambient temperature for a minimum of 15 minutes.

TABLE I. Altitude versus steam temperature (see 4.2.1).

Altitude (feet)	Steam Temperature (+/-3°C)
0 - 1,000	93
1,001 - 2,000	92
2,001 - 3,000	91
3,001 - 4,000	90
4,001 - 5,000	89
5,001 - 6,000	88
Greater than 6,000	87

4.2.2 Dry-bake. (Category D) Prior to the application of the flux and subsequent solder dips, specimens shall be subjected to aging by exposure of the surfaces to be tested to high temperature (see 4.2) in the apparatus specified in 2.13. Aging may be interrupted once for 10 minutes maximum. The devices shall be removed from the test apparatus upon completion of the specified test period.

4.3 Post preconditioning requirements. If solderability test cannot be performed within 2 hours after preconditioning, then devices shall be stored in a desiccant jar or dry nitrogen cabinet. Test must be performed within 72 hours after removal from the preconditioning equipment.

4.4 Solderability test. The test method shall be as follows.

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Test A – For Dip and Look Test
Test B – For Ball Grid Array (BGA) Surface Mount Simulation Test
Test C – For Column Grid Array (CGA) Surface Mount Simulation Test

4.4.1 Dip and look. Dip and look test shall be performed on the following devices:

a. Leaded through hole mount (e.g., DIP, TO can, PGA)
b. Leaded surface mount (e.g., J-lead, QFP)
c. Leadless surface mount (e.g., LCC, LGA, QFN)

4.4.1.1 Application of flux. The terminations to be tested shall be immersed in flux maintained at room ambient temperature. The critical area of the terminations to be tested shall be immersed in the flux for 5 to 10 seconds, and shall be drained for 5 to 20 seconds prior to dipping in the solder pot. The flux shall be covered when not in use and discarded a minimum of once a day. Any obvious droplets of flux clinging to the termination may be removed by blotting.

4.4.1.1.1 Leaded and leadless surface mount devices. Perform the test on the terminations on one side of the device at a time. The fluxing and solder dipping operations shall be performed sequentially on the terminations of the side under test.

4.4.1.1.2 All other devices. The terminations shall be immersed to the seating plane or to within 0.050 inch of the body of the device under test.

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4.4.1.2 Solder dip. The dross and burned flux shall be skimmed from the surface of the molten solder prior to testing. A wave solder pot may be used for this purpose, but the solder shall be static during the dipping procedure (skimming may not be required in wave or flow pots). The molten solder shall be at a uniform temperature of 245°C ± 5°C (473°F ± 9°F). The device shall be attached to a dipping mechanism (see 2.2) and the flux covered terminations immersed once (except for the possible duplicate immersion of corner terminations on leadless surface mount devices) in the molten solder.

The test specimen shall not be suspended above the hot solder pot for longer than 7 seconds. The immersion and emersion rates shall be 1.0 inch per second ± 0.250 inch per second. The dwell time in the solder shall be 5 seconds ± 0.5 second. The dwell time for terminations greater than or equal to 0.040 inch in diameter shall be 7 seconds ± 0.5 second. After the dipping process, the device shall be allowed to cool in air. Residual flux shall be removed from the terminations by dipping the devices in isopropyl alcohol or other suitable solvent. If necessary, a clean soft cloth, cotton swab, or equivalent, moistened with clean isopropyl alcohol or other suitable solvent, may be used to remove all remaining flux.

4.4.1.2.1 Solder dipping of gold plated terminations. Gold plated terminations shall be cycled twice in flux and solder using one or two solder pots. The first immersion is to scavenge the gold on the terminations. It is recommended that a separate solder pot be used for gold plated devices. In any case, the user of this test should use two separate pots, a sufficiently large pot, or monitor closely the contamination level of a single small pot to assure that the test is performed as intended.

4.4.1.2.2 Immersion angle. Unless otherwise specified, the terminations shall be immersed to the solder surface as follows:

a. Leaded through hole mount (e.g., DIP, TO can, PGA) 90°
b. Leaded surface mount (e.g., J-lead, QFP) 20° to 45° (or 90°)
c. Leadless surface mount (e.g., LCC, LGA, QFN) 20° to 45°

4.4.1.2.3 Solder bath contaminants. The manufacturer shall have a system to verify that the solder bath does not exceed the contaminant levels specified in table II.

TABLE II. Maximum limits of solder bath contaminant (see 4.4.1.2.3).

Contaminant	Contaminant percentage limit
Copper	0.300
Gold	0.200
Cadmium	0.005
Zinc	0.005
Aluminum	0.006
Antimony	0.500
Iron	0.020
Arsenic	0.030
Bismuth	0.250
Silver	0.100
Nickel	0.010

NOTE: The total copper, gold, cadmium, zinc, and aluminum contaminants shall not exceed 0.4 percent.

4.4.2 BGA/CGA Surface mount simulation. Surface mount simulation test shall be performed on ball and column grid arrays only.

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4.4.2.1 Ball grid arrays.

a. Place the ceramic substrate onto the base fixture. Place the screen print stencil on the substrate.
b. Apply the solder paste uniformly across the screen print stencil to fill the array pattern using the squeegee.
c. Slowly remove the stencil off the substrate to avoid smearing the paste print. Verify a paste print is equivalent in geometry to the terminal of the device to be tested.
d. Gently press the device down to allow the solder balls to make contact with the solder paste.
e. Place the substrate in the oven and reflow. The reflow profiles shall be per table III, based on the reflow method used.
f. After reflow, allow the ceramic substrate to cool before handling.
g. Slowly remove the device from the substrate. The solder balls may adhere slightly to the substrate due to flux residue.
h. After cooling, clean the device and substrate in the cleaning solution.

4.4.2.2. Column grid arrays.

i. Place the metallized substrate and screen print stencil onto the base fixture.
ii. Place a sufficient amount of solder paste on the screen print stencil. Print the terminal pattern onto the substrate by wiping paste over the stencil/screen in one smooth motion using the squeegee.
iii. Carefully remove the screen print stencil and verify complete coverage of the metallized pads.
iv. Carefully place the solder columns into the printed solder paste.
v. Carefully remove the device and substrate together from the base fixture.
vi. Verify proper alignment with a microscope, use 10x-30x magnification.
vii. Reflow the device and substrate. The reflow profile shall be per table III, based on the reflow method used.
viii. After cooling, clean the device and substrate in the cleaning solution.
ix. Using the cutting equipment, cut the device from the substrate using care to preserve the solder joints at the interface with the substrate.

TABLE III. Reflow parameter requirements.

Method	Peak Temperature (°C)	Time (above 183˚C)
Vapor Phase Reflow	215 - 219	30 - 90 seconds
IR/Convection Reflow	200 - 230	60 - 120 seconds
Oven	215 - 230	2 - 5 minutes (until reflow is assured)

Note: TABLE III reflow parameter values are for solderability testing purposes only and are not related to moisture sensitivity level reflow test parameters. These reflow parameters refer to measurements taken on the device body.

4.5. Examination of terminations. All flux is to be removed prior to visual inspection of the terminal surface.

For devices that were dip and look tested, the dipped portion of the terminations shall be examined using a magnification of 10-15x. Dipped portions of fine-pitch devices (pitch ≤ 0.020 inch) shall be examined at 30x. Verification of failures may be accomplished with higher magnifications up to 60x. The customer/equipment manufacturer of the device may establish a critical portion of the termination within the dipped area. The customer/equipment manufacturer has the option to accept solderability defects outside their established critical area. The customer/equipment manufacturer has the option of cleaning devices to remove carbonate/sulfate deposits caused by exposure of the devices to the steamaging or cleaning process. The customer/equipment manufacturer shall assure that the cleaning process does not adversely affect the physical, mechanical, electrical, or reliability performance of the devices. This cleaning process shall be fully documented. For leaded devices only, the cut portions of the lead which expose lead ends shall not be used for examination and evaluation of the solder coverage of the termination.

For column grid arrays, the number of columns specified in the procurement document shall be randomly selected for examination. Columns which are not within the perimeter of the pad shall be excluded from the selection process. The solder fillets (on the metallized substrate) shall be examined at 15x to 30x magnification. Verification of failures may be accomplished with higher magnifications up to 60x.

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4.5.1 Critical area for dip and look tested devices. Examples of critical areas for some devices are discussed below.

a. Dual-in line. From the termination tip to 0.020 inch above the seating plane, except, devices where the leads exit from the bottom of the device, shall be from the termination tip to the seating plane. Unplated (trim) areas are excluded. See figure 2003-4.
b. Gull wing. All surfaces of the termination at or below the top of the foot, excluding the top of the foot. Unplated (trim) areas are excluded. See Figure 2003-5.
c. J-lead. The narrow portion of the termination below the transition from the termination shoulder. Only the three visible surfaces are to be included. The termination tip is excluded. See Figure 2003-6.
d. L-lead. The bottom of the termination and one times the lead thickness up the side of the termination. Termination edges are excluded. See Figure 2003-7.
e. Passive (rectangular). The bottom of the termination and side of the termination up to the top, excluding the top. See Figure 2003-8.
f. Leadless chip carrier. The bottom of the termination and $^{2}/_{3}$ of the height of the connecting metallized surface. See Figure 2003-9.
g. QFN. The bottom of the termination and exposed pad. See Figure 2003-10.
h. Other devices. 0.050 inch from the body and extending away from the body to the end of the lead or for a distance of 1 inch, whichever is shorter.

If the seating plane is not defined, the critical area shall extend from the termination tip to within 0.040 inch of the lead/device interface. For top brazed and bottom brazed flat pack devices, the critical area shall extend from the termination tip to within 0.070 inch of the lead/device interface.

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4.5.2 Criteria for acceptance. The criteria for acceptance solderability shall be as follows:

4.5.2.1 For all devices, except ball and column grid arrays:

a. The dipped portion of the terminations is at least 95% covered by a continuous new solder coating.
b. Pinholes, nonwetting, or dewetting do not exceed 5% of the total area.
c. For leadless terminations and elements having solder attachment terminations, there shall be no solder bridging between any termination area and any other metallization not connected to it by design. In the event that the solder dipping causes bridging, the test shall not be considered a failure provided that a local application of heat (e.g., gas, soldering iron, or re-dipping) results in solder pullback and no wetting of the dielectric area as indicated by microscopic examination.
d. For devices with exposed pad (e.g., QFN), the exposed pad surfaces shall exhibit a continuous solder coating free from defects for a minimum of 80% of the critical area of those surfaces.
e. Wetting angle shall be less than or equal to 90 degrees.

4.5.2.2 For ball grid arrays:

a. Each solder ball shall “take in” the solder paste deposit producing a uniform and smooth surface with no more than 5% dewetting or non-wetting.
b. The solder balls shall be wetted in a consistent and unified manner.

4.5.2.3 For column grid arrays:

a. Each column fillet shall exhibit evidence of good wetting for at least 50% of the column circumference.
b. Wetting angles (θ) shall be less than or equal to 90°, as shown in Figure 2003-11.

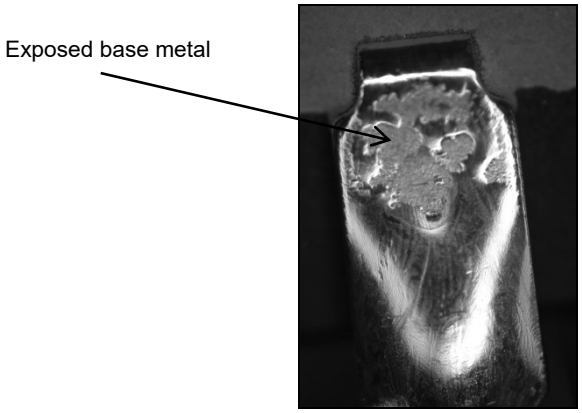

FIGURE 2003-1. Non-wetting.

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FIGURE 2003-2. Pinholes.

FIGURE 2003-3. Dewetting.

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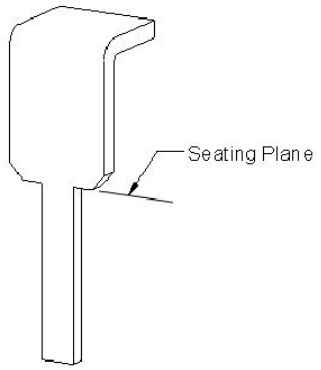

FIGURE 2003-4. Critical area for dual-in line devices.

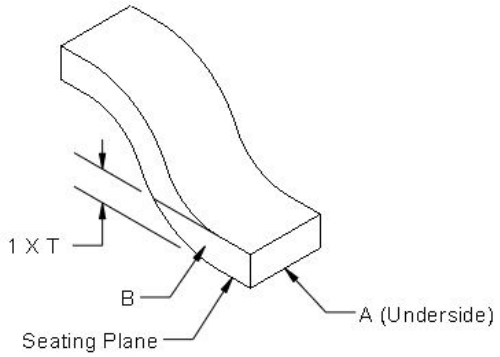

FIGURE 2003-5. Critical area for gull wing devices. Critical area = “A” (up to 1x Lead Thickness) and edges “B”.

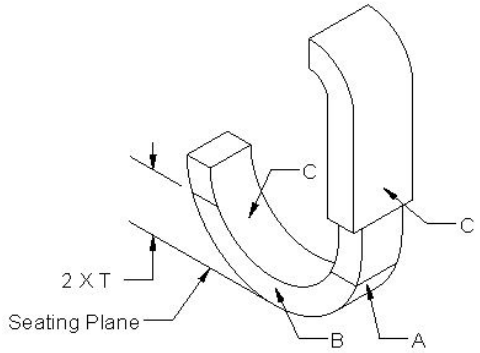

FIGURE 2003-6. Critical area for J-lead devices. Critical area = “A” (equal to 2x Lead Thickness) and edges “B” within the 2xT zone. Surface “C” is excluded.

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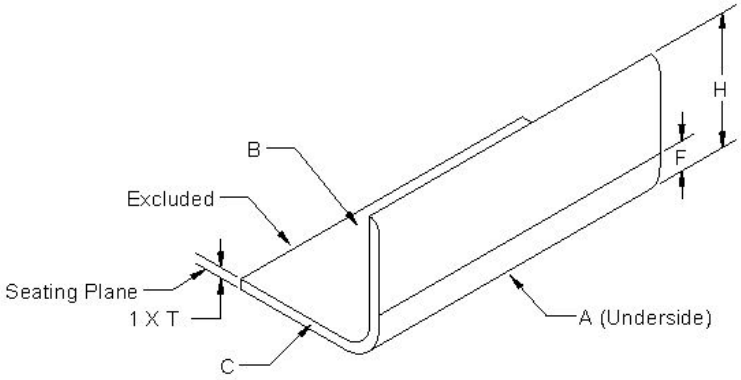

FIGURE 2003-7. Critical area for L-lead devices. Critical area = “A” (equal to 1x Lead Thickness). Surfaces “B” and “C” are excluded.

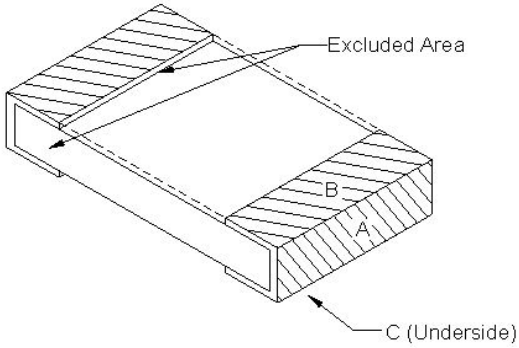

FIGURE 2003-8. Critical area for passive devices (rectangular). Critical area = “A” and “B”. Surface “C” is excluded.

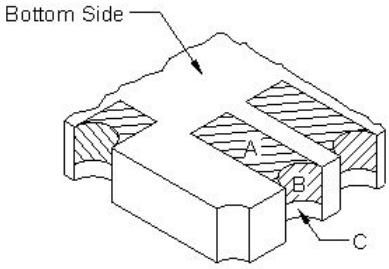

FIGURE 2003-9. Critical area for leadless chip carriers. Critical area = “A” and $^{2}/_{3}$ of “B”. Surface “C” is excluded.

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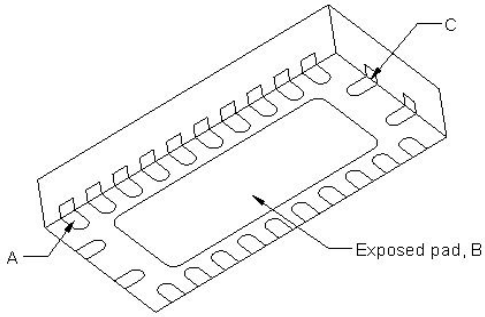
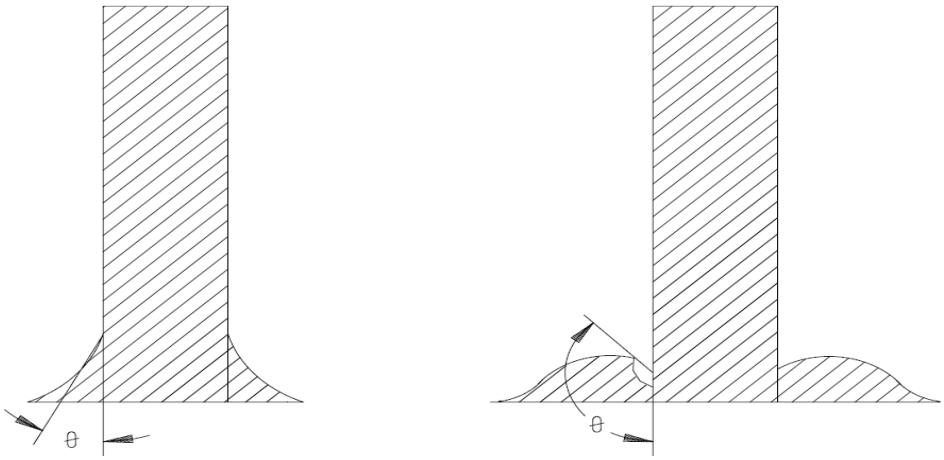


FIGURE 2003-10. Critical area for QFNs. Critical area = “A” and “B”. Surface “C” is excluded.



Acceptable <90 degrees

Reject ≥ 90 degrees

FIGURE 2003-11. Acceptable wetting angle for column grid arrays.

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5. SUMMARY. The following details shall be specified in the applicable procurement document:

a. The number of terminations of each device to be tested, if other than 22(0).

b. The number of devices used for the test, if other than 3.

c. Special preparation of the terminations, if applicable.

d. Depth of immersion if other than specified.

e. Angle of immersion, if other than specified.

f. Solder composition, flux, and temperature, if other than those specified in this document.

g. Measurements after test, where applicable.

h. For ball and column grid arrays:

1. Screen print stencil thickness, if other than specified.

2. Solder paste, if other than specified.

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METHOD 2004.7

LEAD INTEGRITY

1. PURPOSE. This method provides various tests for determining the integrity of microelectronic device leads (terminals), welds, and seals. Test condition A provides for straight tensile loading. Test condition A1 provides testing the solder or braze material lead attach on packages with brazed leads. Test condition B_1 provides for application of bending stresses to determine integrity of leads and seals. Test condition B_2 employs multiple application of bending stresses primarily to determine the resistance of the leads to metal fatigue under repeated bending. Test conditions C_1 and C_2 provide for application of torque or twisting stresses to device leads or studs, respectively, to determine integrity of leads and seals. Test condition D provides for application of peel and tensile stresses to determine integrity of terminal adhesion and plating of leadless packages. Test condition E provides for application of a bend test to determine integrity of plating for flexible and semi-flexible leads. It is recommended that test condition A, B1, B2 and C1 be followed by a seal test in accordance with method 1014 to determine any effect of the stresses applied on the seal as well as on the leads (terminals).

Note: This test method does not apply to ball grid array (BGA) or column grid array (CGA) devices.

2. APPARATUS. See applicable test condition.

3. DEFINITIONS.

a. Arc. An arc is defined as the movement of the case, without torsion, to a position perpendicular to the pull axis and return to normal. All arcs on a single lead shall be made in the same direction and in the same plane without lead restriction.

b. Bending Cycle. A bending cycle is one bend of a lead from a reference position (e.g. 0 Deg), to a defined arc and then back to the original reference to original position (e.g. 0 Deg).

c. Flexible Lead. A rectangular lead is considered flexible if it's section modules is less than or equal to that of an equivalent rectangular lead with a cross section of 0.15 x 0.51 mm (.006 x .020 inch). Round leads less than or equal to 0.51 mm (.020 inch) in diameter shall be considered flexible even if the lead is not intended to be bent as these leads may be subject to routine handling disturbances.

d. Rigid Lead or terminal. A rectangular lead or terminal shall be considered rigid if it's section modules is greater than that of an equivalent rectangular lead with a cross section of 0.15 x 0.51 mm (.006 x .020 inch) and is not intended to be bent or formed in it's end use application. Round leads greater than 0.51 mm (.020 inch) diameter that are not intended to be bent or formed in their end use application shall be considered rigid.

e. Section modules. Section modulus is defined as $bh^2/6$ (width x thickness $^2/6$) for rectangular leads, and 0.098 (φb1)3 or $.098D^3$ for round leads (see MIL-STD-1835). A rectangular lead with a cross section of .006 x .020 has a section modules of 1.2x10-7. A round lead with a .020 inch diameter has a section modules of 7.8x10-7.

f. Semi-flexible Lead. A rectangular lead is considered semi-flexible if it's section modules is greater than that of an equivalent rectangular lead with a cross section of 0.15 x 0.51 mm (.006 x .020 inch) and is intended to be bent or formed in it's end use application Round leads greater than 0.51 mm (.020 inch) diameter that are intended to be bent or formed in their end use application shall be considered semi-flexible.

4. GENERAL PROCEDURE APPLICABLE TO ALL TEST CONDITIONS. The device shall be subjected to the stresses described in the specified test condition and the specified end-point measurements and inspections shall be made except for initial conditioning or unless otherwise specified. Unless otherwise specified, the sample size series sampling shall apply to the leads, terminals, studs or pads chosen from a minimum of 3 devices.

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5. SUMMARY. The following details and those required by the specific test condition shall be specified in the applicable acquisition document:

a. Test condition letter.

b. Number and selection of leads (terminals), if different from above.

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TEST CONDITION A - TENSION

1. PURPOSE. This test is designed to check the capabilities of the device leads, welds, and seals to withstand a straight pull.

2. APPARATUS. The tension test requires suitable clamps and fixtures for securing the device and attaching the specified weight without lead restriction. Equivalent linear pull test equipment may be used.

3. PROCEDURE. A tension of 0.227 kg (8 ounces), unless otherwise specified, shall be applied, without shock, to each lead or terminal to be tested in a direction parallel to the axis of the lead or terminal and maintained for 30 seconds minimum. The tension shall be applied as close to the end of the lead (terminal) as practicable.

3.1 Failure criteria When examined using magnification between 10X and 20X after removal of stress, any complete breakage (e.g. separation of the lead from the body) or loosening of the lead at the glass/ceramic seal that has caused a method 1014 seal failure shall be considered a failure. When a seal test in accordance with method 1014 is conducted as a post test measurement following the lead integrity test(s), meniscus cracks shall not be cause for rejection of devices which pass the seal test.

4. SUMMARY. The following details shall be specified in the applicable acquisition document:

a. Weight to be attached to lead, if other than .227 kg (8 ounces) (see 3).

b. Length of time weight is to be attached, if other than 30 seconds (see 3).

TEST CONDITION A_1 – LEAD BRAZE INTEGRITY

1. PURPOSE. This test is for packages with brazed leads and is intended to test the lead to package attach integrity. This test applies to both flat package and dual in-line package construction.

2. APPARATUS. The lead braze integrity test requires suitable clamps and fixtures for securing the device and attaching the specified weight without lead restriction. Equivalent linear pull test equipment may be used.

3. PROCEDURE. A tension of 0.227 kg (8 ounces), unless otherwise specified, shall be applied, without shock, to each lead or terminal to be tested in a direction perpendicular to the lead attach surface (i.e. force wants to peel lead out or off the attach medium). The force shall be maintained for 30 seconds minimum. The weight shall be applied as close to the end of the lead (terminal) as practicable.

3.1 Failure criteria When examined using magnification between 10X and 20X after removal of stress, any evidence of lead fracture of the solder/braze connection or disconnection of the lead from the package shall be considered a failure.

4. SUMMARY. The following details shall be specified in the applicable acquisition document:

a. Weight to be attached to lead, if other than .227 kg (8 ounces) (see 3).

b. Length of time weight is to be attached, if other than 30 seconds (see 3).

TEST CONDITION B_1 - BENDING STRESS

1. PURPOSE. This test is designed to check the capability of the leads, lead welds, and seals of the devices to withstand stresses to the leads and seals which might reasonably be expected to occur from actual handling and assembly of the devices in application, or to precondition the leads with a moderate bending stress prior to environmental testing.

2. APPARATUS. Attaching devices, clamps, supports, or other suitable hardware necessary to apply the bending stress through the specified bend angle.

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3. PROCEDURE. Each lead or terminal to be tested shall be subjected to a force as specified in 3.1 through 3.5, as applicable. Any number or all of the leads of the device may be tested simultaneously. Rows of leads may be tested one row at a time. Each lead shall be tested in one direction and returned to the approximate original position. All arcs shall be made in the same plane without lead restriction.

3.1 Direction of bends. Test leads shall be bent in the least rigid direction. If there is no least rigid direction, they may be bent in any direction. No lead shall be bent so as to interfere with another lead. If interference is unavoidable, the test lead shall be bent in the opposite direction to the angle specified and returned to its approximate original position.

3.2 Procedure for pre-formed leads. When normally straight leads are supplied in a pre-formed condition (including the staggered lead dual-in- line configuration), the lead forming operation shall be considered an acceptable bending stress in place of that specified, provided the lead forming has been done after lead plating and the forming is at least as severe in permanent lead deformation as the specified bending.

3.3 Procedure for flexible and semi-flexible leads (e.g., flat packs and axial-lead metal-can devices).

3.3.1 Flexible leads. Flexible leads shall be bent through an arc of at least 45° measured at the lead extremities, unless otherwise specified.

3.3.2 Semi-flexible leads. Semi-flexible leads shall be bent through an arc of at least 30° measured at the lead extremities unless otherwise specified.

3.4 Procedure for dual-in-line and pin grid array package leads.

3.4.1 Dual-in-line (platform, side brazed, bathtub) package leads are leads normally aligned in parallel at a 90° angle from the bottom of the package during insertion. Dual-in-line package leads shall be bent inward through an angle sufficient to cause the lead to retain a permanent bend (i.e., after stress removal) of at least 15°. For configuration 1 and 2, the angle of bend shall be measured from the lead extremities to the first bend (see figure 2004-1), for configuration 3, the angle of bend shall be measured from the lead extremities to the seating plane (see figure 2004-1).

3.4.2 Pin grid array packages shall have the leads required for testing from the outside row of leads on opposite sides bent through an angle sufficient to cause the lead to retain a permanent bend (i.e., after stress removal) of at least 15°. The angle of bend shall be 15° from normal and the bend shall be made at the approximate seating plane.

3.5 Procedure for rigid leads or terminals. Unless otherwise specified in the package acquisition document, devices with rigid leads or terminals shall be bent through an angle of at least 10° to cause a permanent bend (i.e. after stress removal).

Note: Rigid leads or terminals shall be reviewed by the acquiring device manufacturer to determine if a lead integrity test adds value based on the purpose of this test condition.

3.6 Failure criteria. When examined using magnification between 10X and 20X after removal of the stress, any complete breakage (e.g. separation of the lead from the body) or loosening of the lead at the glass/ceramic seal that has caused a method 1014 seal failure shall be considered a failure. When a seal test in accordance with method 1014 is conducted as a post test measurement following the lead integrity test(s), glass meniscus cracks shall not be cause for rejection of devices which pass the seal test.

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4. SUMMARY. The following details shall be specified in the applicable acquisition document:

   a. Bending arc, if other than that specified.

   b. Procedure, if other than that specified.

   c. Number and selection of leads and procedure for identification, if other than that specified.

   d. Post test measurements, if applicable (see 3.6)

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TEST CONDITION B_2 - LEAD FATIGUE

1. PURPOSE. This test is designed to check the resistance of the leads to metal fatigue.

2. APPARATUS. Attaching devices, clamps, supports, or other suitable hardware necessary to apply a repeated bending stress through the specified bend angle.

3. PROCEDURE. Each lead or terminal to be tested shall be subjected to a force as specified in 3.1 through 3.7, as applicable. Each lead shall be tested in the same direction through the specified arc in one direction and returned to the approximate original position. All arcs shall be made in the same plane without lead restriction. A test cycle shall be completed in 2 to 5 seconds. For devices with rectangular or ribbon leads, the plane of the arcs shall be perpendicular to the flat plane of the lead. The test shall not be applied to end leads of packages where its application will apply primarily torsion forces at the lead seal.

3.1 Direction of bends. Test leads shall be bent in the least rigid direction. If there is no least rigid direction, they may be bent in any direction. No lead shall be bent so as to interfere with another lead. If interference is unavoidable, the test lead shall be bent in the opposite direction to the angle specified and returned to its normal position.

3.2 Procedure for pre-formed leads. When normally straight leads are supplied in a pre-formed condition (including the staggered lead dual-in- line configuration), the lead forming operation shall be considered an acceptable lead fatigue test in place of that specified, provided the lead forming has been done after lead plating and the forming is at least as severe in permanent lead deformation as the specified bending.

3.3 Procedure for packages with Flexible leads. For flexible rectangular leads or round leads, the test force shall be 0.085kg ±0.009 kg (3oz ±0.3 ounces). Each lead shall be tested for three 90° ±5° arcs, unless otherwise specified.

3.4 Procedure for packages with Semi-flexible leads. For semi-flexible rectangle leads or round leads, the test force shall be 0.229kg ±0.014 kg (8oz ±0.5 ounces). Each lead shall be tested for three 90° ±5° arcs, unless otherwise specified.

3.5 Procedure for dual-in-line and pin grid array package leads.

3.5.1 Dual-in-line (platform, side brazed, bathtub) package leads are leads normally aligned in parallel at a 90° angle from the bottom of the package during insertion. Dual-in-line package leads shall be bent three times inward through an angle sufficient to cause the lead to retain a permanent bend (i.e., after stress removal) of at least 15°. For configuration 1 and 2, the angle of bend shall be measured from the lead extremities to the first bend (see figure 2004-1), for configuration 3, the angle of bend shall be measured from the lead extremities to the seating plane (see figure 2004-1).

3.5.2 Pin grid array packages shall have the leads required for testing from the outside row of leads on opposite sides bent three times through an angle sufficient to cause the lead to retain a permanent bend (i.e., after stress removal) of at least 15°. The angle of bend shall be 15° from normal and the bend shall be made at the approximate seating plane. At the completion of the initial bend, the leads shall be returned to their approximate original position.

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3.6 Optional procedure for Semi-Flexible and Flexible leads. As an option for all lead sizes, a force as determined by the following formula, unless otherwise specified, shall be applied to each lead to be tested for 90 degrees ±5 degree arcs of the device. All other conditions of section 3.3. and 3.4 shall apply. The test weight shall be calculated as follows: Weight = (area in square inches) x 2.1 % x (UTS in psi) x 453.6 grams/lb. Where UTS in psi is the ultimate tensile strength (UTS) for a particular material. Typical value for kovar, alloy 42 and copper materials are listed below. The UTS for other materials can be found in vendor data sheets. The result shall be rounded to the nearest whole number.

Material	UTS in psi
Kovar	75000
Alloy 42	71000
Copper 101	43,500
Copper 110	31,900

3.7 Procedure for rigid leads or terminals. Testing of rigid leads or terminals is not required.

3.8 Failure criteria. When examined using magnification between 10X and 20X after removal of stress, any complete breakage (e.g. separation of the lead from the body) shall be considered a failure.

4. SUMMARY. The following details shall be specified in the applicable acquisition document:

a. Force to be applied to the lead, if other than above (see 3).

b. Number of cycles, if other than above (see 3).

c. Maximum bend angle, if other than above (see 3).

d. Number and selection of leads (terminals), if different from above.

e. Post test measurements, if applicable (see 3.8)

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TEST CONDITION C_1 - LEAD TORQUE

1. PURPOSE. This test is designed to check device leads (or terminals) and seals for their resistance to twisting motions.

2. APPARATUS. The torque test requires suitable clamps and fixtures, and a torsion wrench or other suitable method of applying the specified torque without lead restriction.

3. PROCEDURE. The appropriate procedure of 3.1 or 3.2 for the device under test shall be used.

3.1 Procedure for devices with circular cross-section terminals or leads. The device body shall be rigidly held and the specified torque shall be applied for 15 seconds minimum to the lead (terminal) to be tested, without shock, about the axis of the lead (terminal).

3.2 Procedure for devices with rectangular cross-section terminals or leads. The device body shall be rigidly held and a torque of 1.45 ±.145 kg-mm (2.0 ±0.2 ounce-inch) unless otherwise specified, shall be applied to the lead (terminal) at a distance of 3.05 ±0.76 mm (0.12 ±0.03 inch) from the device body or at the end of the lead if it is shorter than 3.05 mm (0.12 inch). The torque shall be applied about the axis of the lead once in each direction (clockwise and counterclockwise). When devices have leads which are formed close to the body, the torque may be applied 3.05 ±0.76 mm (0.12 ±0.03 inch) from the form. For device leads which twist noticeably when less than the specified torque is applied, the twist shall be continued until the twist angle reaches 30° ±10° or the specified torque is achieved, whichever condition occurs first. The lead shall then be restored to its original position.

3.3 Failure criteria. When examined using magnification between 10X and 20X after removal of the stress, any complete breakage (e.g. separation of the lead from the body) or loosening of the lead at the glass/ceramic seal that has caused a method 1014 seal failure shall be considered a device failure. When a seal test in accordance with method 1014 is conducted as a post test measurement following the lead integrity test(s), meniscus cracks shall not be cause for rejection of devices which pass the seal test.

4. SUMMARY. The following details shall be specified in the applicable acquisition document:

a. Torque to be applied for circular cross-section leads (see 3.1).

b. Duration of torque application for circular cross-section leads, if other than 15 seconds minimum (see 3.1).

c. Torque to be applied for rectangular cross-section leads, if other than 1.45 ±0.145 kg-mm (2.0 ±0.2 ounce-inch) (see 3.2).

d. See general summary above.

e. Post test measurements, if applicable (see 3.3)

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TEST CONDITION C_2 - STUD TORQUE

1. PURPOSE. This test is designed to check the resistance of the device with threaded mounting stud to the stress caused by tightening the device when mounting.

2. APPARATUS. The torque test requires suitable clamps and fixtures, and a torsion wrench or suitable method of applying the specified torque.

3. PROCEDURE. The device shall be clamped by its body or flange. A flat steel washer of a thickness equal to six thread pitches of the stud being tested and a new class 2 fit steel nut shall be assembled in that order on the stud, with all parts clean and dry. The specified torque shall be applied without shock to the nut for the specified period of time. The nut and washer shall then be disassembled from the device, and the device then examined for compliance with the requirements.

3.1 Failure criteria. The device shall be considered a failure if any of the following occurs:

a. The stud breaks or is elongated greater than one-half of the thread pitch.

b. It fails the specified post-test end point measurements.

c. There is evidence of thread stripping or deformation of the mounting seat.

4. SUMMARY. The following details shall be specified in the applicable acquisition document:

a. The amount of torque to be applied (see 3).

b. Length of time torque is to be applied (see 3).

c. Measurements to be made after test (see 3).

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TEST CONDITION D - SOLDER PAD ADHESION FOR LEADLESS CHIP CARRIER AND SIMILAR DEVICES

1. PURPOSE. This test is designed to check the capabilities of the device solder pads to withstand a delamination (peel) stress of specified tension and time.

2. APPARATUS. Equipment for 10X magnification, suitable clamps and fixtures for securing the device and applying the specified tension/time conditions to wires soldered to the device solder pads. Equivalent linear pull test equipment may be used.

3. PROCEDURE. Unless otherwise specified, a delamination (peel) stress test shall be applied to randomly selected solder pads from each device selected for test. Further, unless otherwise specified, the sampling shall be Sample Size Number = 15, c = 0 based on the number of solder pads tested, chosen from a minimum of three devices. Preparation and testing of devices shall be in accordance with figure 2004-2 of this method and as follows.

a. Pretinned soft annealed solid copper wire of a gauge (diameter) nearest, but not exceeding that of the nominal solder pad width, shall be soldered using Sn60A or Pb40A or Sn63A or Pb37A of IPC J-STD-006 (previously known as Sn60 or Sn63 solder in accordance with QQ-S-571) to each solder pad to be tested in a manner such that the wire is bonded over the entire solder pad length and terminates at the package edge (see figure 2004-2). The unsoldered portion of the wire shall be bent perpendicular to the bond plane prior to attachment. Caution should be taken to assure that the solder pad metallization is not damaged during the soldering or the wire bending operation.

b. Unless otherwise specified, a minimum tension of 8 ounces (2.22 N) shall be applied, without shock, to each solder pad to be tested in a direction perpendicular to the solder pad surface and maintained for 30 seconds minimum.

3.1 Failure criteria. When examined, using 10X magnification, after removal of the tension stress, the appearance of any delamination involving constituent solder pad interfaces shall be considered an adhesion failure of the solder pad. Separation of the solder pad from the device is an obvious (without visual magnification) adhesion failure. Separation of the wire from the solder fillet (leaving the solder pad intact) or wire breakage is considered a test procedure failure.

4. SUMMARY. The following details shall be specified in the applicable acquisition document:

a. Sampling criteria, if other than specified (see 3.0).

b. Failure criteria, if other than specified (see 3.1).

c. Tension to be applied in this test if other than 8 ounces (2.22 N).

d. Length of time tension is to be applied if other than 30 seconds.

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TEST CONDITION E – LEAD PLATING INTEGRITY

1. PURPOSE. This test is designed to check the lead plating of flexible and semi-flexible leads which might reasonably be expected to occur from a lead form operation.

Note: Additional plating adhesion accept/reject criteria may be flowed down by the specified plating specifications.

2. APPARATUS. Attaching devices, clamps, supports, or other suitable hardware necessary to apply the bending stress through the specified bend angle.

3. PROCEDURE. Each flexible or semi-flexible lead to be tested shall be subjected to a 90° bend. Any number or all of the leads of the test device may be bent 90° simultaneously. Each lead shall be bent 90° in one direction in the same plane without lead restriction. Leads may be bent 90° by performing a lead form operation.

3.1 Direction of bend. Test leads shall be bent in the normal lead form configuration.

3.2 Procedure for pre-formed leads. When normally straight leads are supplied in a pre-formed condition, then this test condition shall not apply.

3.3 Procedure for flexible and semi-flexible leads (e.g., flat packs and axial-lead metal-can devices).

3.3.1 Flexible leads. Flexible leads shall be bent in the middle of the lead through an arc of at least 90°, unless otherwise specified.

3.3.2 Semi-flexible leads. Semi-flexible leads shall be bent in the middle of the lead through an arc of at least 90°, unless otherwise specified.

3.4 Failure criteria. When examined using magnification between 10X and 20X after removal of the stress, any cracking of the lead plating which results in flaking, peeling or blistering or the crack can be peeled back with a sharp instrument (i.e. knife) shall be rejected.

4. SUMMARY. The following details shall be specified in the applicable acquisition document:

a.. Bending arc, if other than that specified.

b. Procedure, if other than that specified.

c. Number and selection of leads and procedure for identification, if other than that specified.

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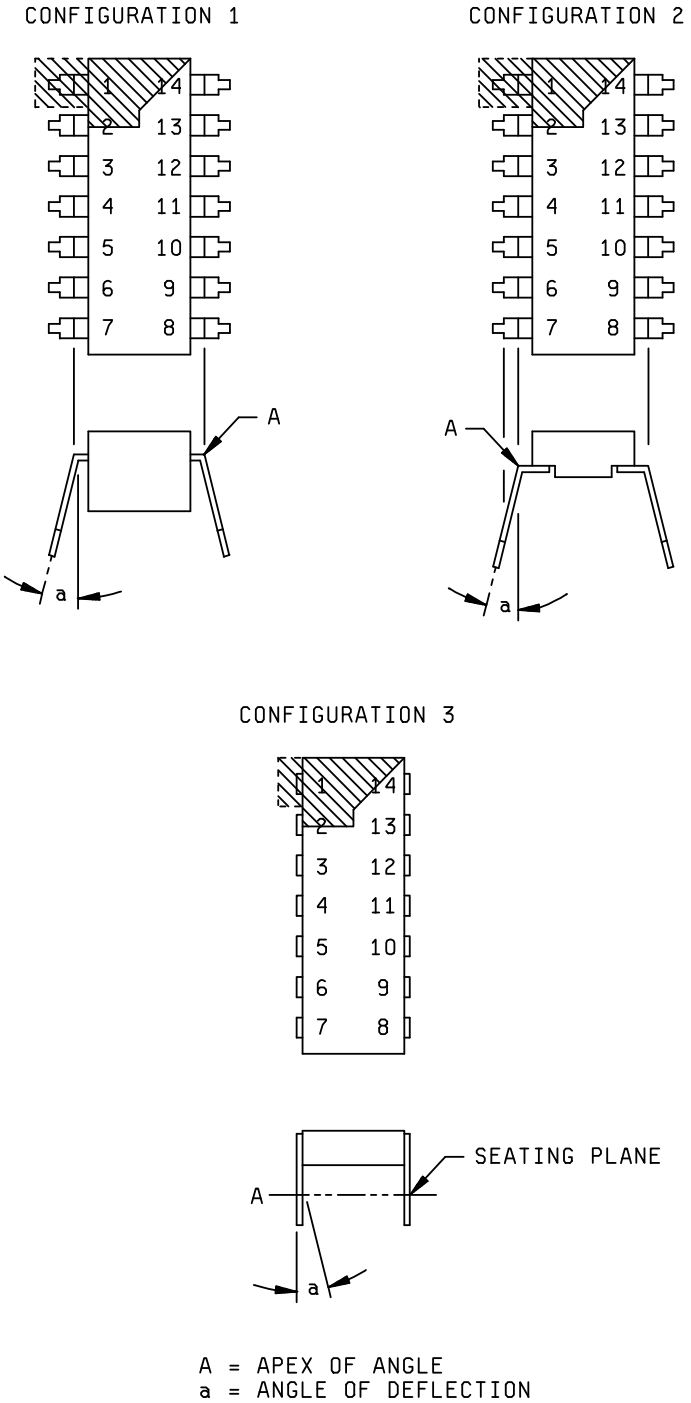

FIGURE 2004-1 Angle of bend for dual-in-line package configurations.

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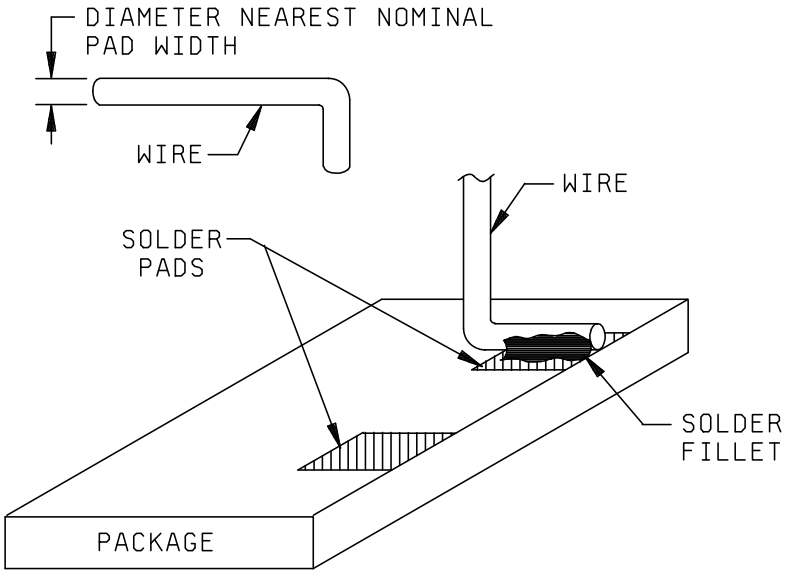

MATERIALS

Flux: Flux type symbol “A” or “B” (flux type “L0” or “L1”) in accordance with IPC J-STD-004 (previously designated as Type R or RMA only, in accordance with MIL-F-14256).

Solder: Sn60A or Pb40A or Sn63A or Pb37A in accordance with IPC J-STD-006 (previously designated as Sn 60 or Sn 63 in accordance with QQ-S-571).

Wire: Soft annealed solid copper.

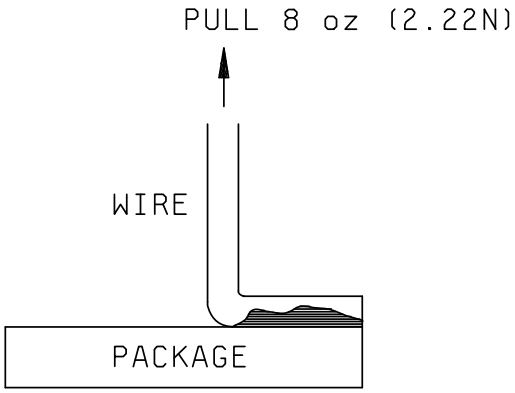

FIGURE 2004-2 Solder pad adhesion.

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METHOD 2005.2

VIBRATION FATIGUE

1. PURPOSE. The purpose of this test is to determine the effect on the device of vibration in the frequency range specified.

2. APPARATUS. Apparatus for this test shall include equipment capable of providing the sustained vibration within the specified levels and the necessary optical and electrical equipment to conduct post-test measurements.

3. PROCEDURE. The device shall be rigidly fastened on the vibration platform and the leads or cables adequately secured. The device shall be vibrated with a constant amplitude simple harmonic motion having a peak acceleration corresponding to the specified test condition. For test condition A, constant amplitude harmonic motion in the range of 60 ±20 Hz having an amplitude of 0.06 inch double amplitude (total excursion) shall be acceptable as an alternative to the specified peak acceleration. The vibration shall be applied for 32 ±8 hours minimum, in each of the orientations X, Y, and Z for a total of 96 hours, minimum. When specified, devices with an internal cavity containing parts or elements subject to possible movement or breakage during vibration shall be further examined by radiographic examination in accordance with method 2012 or by delidding or opening and internal visual examination at 30X magnification to reveal damage or dislocation. Where this test is performed as part of a group or subgroup of tests, the post-test measurements or inspections need not be performed specifically at the conclusion of this test, but may be performed once at the conclusion of the group or subgroup.

Test condition	Peak acceleration, g
A	20
B	50
C	70

3.1 Examination. After completion of the test, an external visual examination of the marking shall be performed without magnification or with a viewer having a magnification no greater than 3X and a visual examination of the case, leads, or seals shall be performed at a magnification between 10X and 20X. This examination and any additional specified measurements and examination shall be made after completion of the final cycle or upon completion of a group, sequence, or subgroup of tests which include this test.

3.2 Failure criteria. After subjection to the test, failure of any specified measurement or examination (see 3 and 4), evidence of defects or damage to the case, leads, or seals, or illegible markings shall be considered a failure. Damage to marking caused by fixturing or handling during tests shall not be cause for device rejection.

3.3 Test frequency and amplitude. For test condition A, B, or C, the double amplitude and frequency used shall result in the application of the peak accelerations of 20, 50, or 70 g's. Peak acceleration may be computed using the following equation:

$$g = \frac{A\,(F)^2}{(2)\,(386)}$$

Where: A = double amplitude in inches.
F = frequency in radians/second.

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4. SUMMARY. The following details shall be specified in the applicable acquisition document:

   a. Test condition (see 3).

   b. Test frequency and test double amplitude (see 3 and 3.3), if other than specified.

   c. Test time and specimen orientation, if other than specified (see 3).

   d. Measurements after test (see 3 and 3.1).

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METHOD 2006.1

VIBRATION NOISE

1. PURPOSE. The purpose of this test is to measure the amount of electrical noise produced by the device under vibration.

2. APPARATUS. Apparatus for this test shall include equipment capable of providing the required variable frequency vibration at the specified levels, a calibrated high impedance voltmeter for noise measurement during test and the necessary optical and electronic equipment for post-test measurements.

3. PROCEDURE. The device and its leads shall be rigidly fastened on the vibration platform and the leads or cables adequately secured. The device shall be vibrated with simple harmonic motion having either an amplitude of 0.06 inch double amplitude (maximum total excursion) or a constant peak acceleration of 20 g minimum. The vibration frequency shall be varied approximately logarithmically between 20 and 2,000 Hz. The entire frequency range shall be traversed in not less than 4 minutes for each cycle. This cycle shall be performed once in each of the orientations X, Y, and Z (total of 3 times), so that the motion shall be applied for a total period of approximately 12 minutes. The specified voltages and currents shall be applied in the test circuit. The maximum noise-output voltage across the specified load resistance during traverse, shall be measured with an average-responding root-mean-square (rms) calibrated high impedance voltmeter. The meter shall measure, with an error of not more than 3 percent, the rms value of a sine-wave voltage at 2,000 Hz. The characteristic of the meter over a bandwidth of 20 to 2,000 Hz shall be ±1 decibel (dB) of the value at 2,000 Hz, with an attenuation rate below 20 and above 20,000 Hz of 6 ±2 dB per octave. The maximum inherent noise in the circuit shall be at least 10 dB below the specified noise-output voltage. When specified, devices with an internal cavity containing parts or elements subject to possible movement or breakage during vibration shall be further examined by radiographic examination in accordance with method 2012 or by delidding or opening and internal visual examination at 30X magnification to reveal damage or dislocation. Where this test is performed as part of a group or subgroup of tests, the post-test measurements or inspections need not be performed specifically at the conclusion of this test, but may be performed once at the conclusion of the group or subgroup.

3.1 Examination. After completion of the test, an external visual examination of the marking shall be performed without magnification or with a viewer having a magnification no greater than 3X and a visual examination of the case, leads, or seals shall be performed at a magnification between 10X and 20X. This examination and any additional specified measurements and examination shall be made after completion of the final cycle or upon completion of a group, sequence, or subgroup of tests which include this test.

3.2 Failure criteria. After subjection to the test, failure of any specified measurement or examination (see 3 and 4), evidence of defects or damage to the case, leads, or seals, or illegible markings shall be considered a failure. Damage to marking caused by fixturing or handling during tests shall not be cause for device rejection.

4. SUMMARY. The following details shall be specified in the applicable acquisition document:

a. Test condition (see 3).

b. Test voltages and currents (see 3). Unless otherwise specified, these shall be the nominal operating voltages and currents for the device.

c. Load resistance (see 3). Unless otherwise specified, this shall be the maximum rated operating load of the device.

d. Measurements after test (see 3 and 3.1).

e. Noise-output voltage limit (see 3).

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METHOD 2007.3

VIBRATION, VARIABLE FREQUENCY

1. PURPOSE. The variable frequency vibration test is performed for the purpose of determining the effect on component parts of vibration in the specified frequency range. This is a destructive test.

2. APPARATUS. Apparatus for this test shall include equipment capable of providing the required variable frequency vibration at the specified levels and the necessary optical and electrical equipment for post-test measurements.

3. PROCEDURE. The device shall be rigidly fastened on the vibration platform and the leads or cables adequately secured. The device shall be vibrated with simple harmonic motion having either a peak to peak amplitude of 0.06 inch (±10 percent) or a peak acceleration of the specified test condition A, B, or C (+20 percent, -0 percent g). Test conditions shall be amplitude controlled below the crossover frequency and g level controlled above. The vibration frequency shall be varied approximately logarithmically between 20 and 2,000 Hz. The entire frequency range of 20 to 2,000 Hz and return to 20 Hz shall be traversed in not less than 4 minutes. This cycle shall be performed 4 times in each of the orientations X, Y, and Z (total of 12 times), so that the motion shall be applied for a total period of not less than 48 minutes. When specified, devices with an internal cavity containing parts or elements subject to possible movement or breakage during vibration shall be further examined by radiographic examination in accordance with method 2012 or by delidding or opening and internal visual examination at 30X magnification to reveal damage or dislocation. Where this test is performed as part of a group or subgroup of tests, the post-test measurements or inspections need not be performed specifically at the conclusion of this test, but may be performed once at the conclusion of the group or subgroup.

Test condition	Peak acceleration, g
A	20
B	50
C	70

CAUTION: If this test is performed using a potting compound type test fixture (e.g., waterglass/sodium silicate) the facility performing the test shall assure that this procedure/material does not mask fine/gross leakers.

3.1 Examination. After completion of the test, an external visual examination of the marking shall be performed without magnification or with a viewer having a magnification no greater than 3X and a visual examination of the case, leads, or seals shall be performed at a magnification between 10X and 20X. This examination and any additional specified measurements and examination shall be made after completion of the final cycle or upon completion of a group, sequence, or subgroup of tests which include this test.

3.2 Failure criteria. After subjection to the test, failure of any specified measurement or examination (see 3 and 4), evidence of defects or damage to the case, leads, or seals, or illegible markings shall be considered a failure. Damage to marking caused by fixturing or handling during tests shall not be cause for device rejection.

4. SUMMARY. The following details shall be specified in the applicable acquisition document:

a. Test condition (see 3).

b. Measurements after test (see 3 and 3.1).

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METHOD 2008.1

VISUAL AND MECHANICAL

Method 2008 is canceled effective 15 November 1974. It is superseded by methods 2014, 2015, and 2016. Test condition A of method 2008 is superseded by method 2016. Test condition B, except for 3.2.1 (Marking), is superseded by method 2014. Paragraph 3.2.1 is superseded by method 2015.

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METHOD 2009.14

EXTERNAL VISUAL

1. PURPOSE. The purpose of this test method is to verify the workmanship of packaged devices. This test method shall also be utilized to inspect for damage due to handling, assembly, and/or test of the packaged device. This examination is normally employed at outgoing inspection within the device manufacturer's facility, or as an incoming inspection of the assembled device.

2. APPARATUS. Equipment used in this test shall be capable of demonstrating device conformance to the applicable requirements. Equipment shall include optical devices capable of magnification of at least 1.5X to 10X, with a relatively large and accessible field of view.

3. PROCEDURE

3.1 Magnification. Devices shall be examined at 1.5X to 10X magnification. Devices may be examined anywhere in the range of 1.5X to 10X; however, acceptable product must be capable of passing all criteria when examined at 10X magnification. Individual glass seals (see 3.3.9) shall be examined at 7X to 10X magnification.

3.2 Foreign material. When foreign material is present, and its adherence is in question, the device may be subjected to a clean filtered gas stream (vacuum or expulsion) of approximately 20 psig.

3.3 Failure criteria. Devices shall fail if they exhibit any of the following:

3.3.1 General

a. Illegible marking, or marking content or placement not in accordance with the applicable specification.

b. Presence of any secondary coating material that visually obscures a seal area(s) (i.e., any hermetic interface).

c. Evidence of any nonconformance with the detail drawing or applicable procurement document, or absence of any required feature.

3.3.2 Foreign/displaced material

a. Braze material flow, or other foreign material (i.e., contamination or corrosion) that reduces the isolation between leads or between braze pads to less than 50% of the lead separation (pad separation for brazed leads) but in no case less than the case outline minimum.

b. Leads or terminals with foreign material such as paint or other adherent deposits affecting 5% or greater of the lead surface area.

3.3.3 Construction defects

a. Protrusions on the bottom (mounting) surface of the package that extend beyond the seating plane.

b. Protrusions (excluding glass run-out) on any other package surface that exceed the lead thickness in height (leaded packages).

c. Protrusions on the lid or cover, or extending beyond the surface plane of solder pads, that exceed 25% of the terminal width in height (leadless packages).

d. Metallization not intended by design between solder pads, between elements of thermal patterns and/or between seal ring or lid to metallized castellations that reduce the isolation to less than 50% of pad separation (leadless packages).

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3.3.4 Package Body/Lid Finish

a. Defective finish (peeling, flaking, pitting, blistering, or corrosion). Discoloration that does not exhibit these conditions is acceptable.

b. Scratches, mars, or indentations, either due to damage or processing, that expose base metal. Exposed underplate is acceptable.

3.3.5 Leads

a. Broken leads.

b. Leads or terminals that are not intact or aligned in their normal location, free of sharp or unspecified lead bends, or twisted more than 20° from the normal lead plane.

c. Leads with pits and/or depressions that exceed 25% of the width (diameter for round leads) and are greater than 50% of the lead thickness in depth.

d. Leads with burrs exceeding a height greater than 50% of the lead thickness.

e. Lead misalignment to the braze pad to the extent that less than 75% of the lead braze section is brazed to the pad.

f. Metallization (including solder lead finish) in which the isolation between leads or between lead and other package metallization is reduced to less than 50% of lead separation (pad separation for brazed leads) but in no case less than the case outline minimum.

g. Braze material that increases the lead dimensions to greater than 1.5 times the lead thickness above the design maximum between the seating plane and the ceramic body or that increases the lead dimensions to greater than the design maximum below the seating plane.

h. Scratches that expose base metal over more than 5% of the lead surface area. Exposed base metal on the cut lead ends is acceptable and does not count in the 5%.

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3.3.6 Ball/column grid array leads.

a. Nonconformance with any design criteria (see 3.3.1.c herein).

b. Solder columns / solder balls alignment.
i. Solder column base is misaligned such that the column is not within the perimeter of the pad.
ii. Solder column tip misalignment that does not meet drawing requirements (typically < 100 µm).
iii. Solder ball misalignment that does not meet drawing requirements.

c. Broken, twisted or damaged solder columns/spheres. Damaged columns/spheres (scored, gouged) that fail to meet final dimensional requirements.

d. Solder column bends or misalignments that do not meet the drawing design criteria.

e. Solder columns/spheres containing any void, hole, pit, gouge or depression greater than 15% of the column/sphere diameter or volume. For voids, holes, pits less than 15% of the diameter or volume, the cumulative total shall be less than half of the column/sphere diameter.

f. Solder columns/spheres containing cracks.

g. Columns/spheres with burrs or bumps exceeding 20% of the column/sphere diameter.

h. Columns/spheres that exhibit peeling, flaking, or blistering.

i. Solder fillet height which is less than half the column diameter for more than 25% of the column circumference.

j. For copper reinforced columns that exhibit any of the following:

i. Copper ribbon delamination exceeding 25% around the column circumference.
ii. Columns with copper wire having copper exposed more than five percent of the column surface area. Exposed (cut) copper on the free end of the column is acceptable.

k. Discoloration of columns/spheres due to corrosion, crusting, or residual flux (there should be a consistent shiny solder appearance). Evidence of flux residue, stains, rust, or signs of corrosion that can be seen at 3 to 10X magnification.

l. Foreign material, discoloration, or adherent deposits within 0.5 mm of the free end of the column.

m. Solder columns/spheres that do not meet requirements for device co-planarity/uniformity of the drawing design criteria (typically < 150 µm).

o. Pad dewetting/non-wetting greater than 5% of the pad surface area.

3.3.7 Package body/lid - leaded devices (See Figure 2009-1).

a. Broken packages or cracks in the packages. Surface scratches shall not be cause for failure except where they violate other criteria stated herein for marking, finish, etc.

b. Any chipping (chip in place/chipout) dimension that exceeds 0.060 inch in any direction on the surface and has a depth that exceeds 25% of the thickness of the affected package element (e.g., cover, base, or wall).

c. External lead metallization stripe forming a conductor to a brazed lead that exhibits voids greater than 25% of the conductor width.

d. Evidence of cracks, delamination, separation, or voiding on any multilayer ceramic package.

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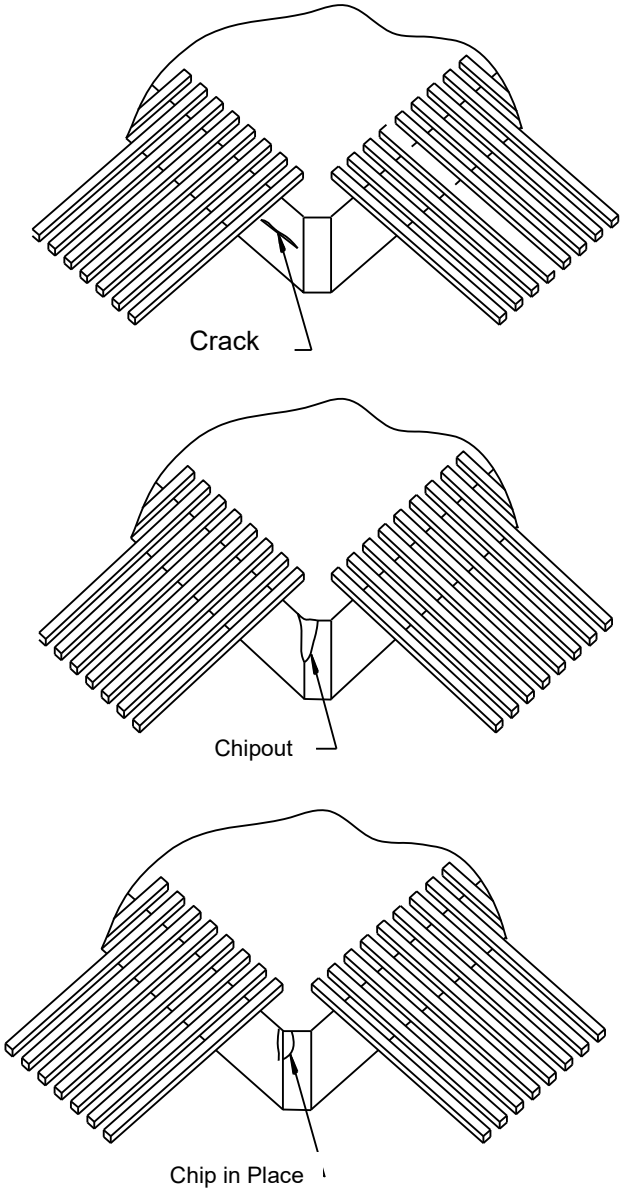

Note: Chipping vs Cracks.

i Cracks are lines of material separation that have one or both terminations in a direction which could be conceived as possibly extending further without limit or in the direction of package structures as it extends.

ii. Chipping is a line of material separation that has both terminations directed towards an edge of the package with no conceivable path for extension beyond the edge.

iii. Chipout is chipping that is so extensive as to have caused the removal of package material.

iv. Chip in Place is chipping that has not cause the removal of material, but forms the semicircular pattern defining a section of material.

FIGURE 2009-1 Cracks Vs Chipping.

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3.3.8 Package body/lid - leadless devices (See Figure 2009-1).

a. Ceramic chipping (chip in place /chipout) that dimensionally exceed 50% of the distance between terminals in any direction on the affected surface (edge or corner), and exceed a depth of 25% of the thickness of the affected package element (e.g., cover, lid, base, or wall).

b. Evidence of cracks, delamination, separation, or voiding on any package element.

c. Castellation to solder pad misalignment. The metal in the castellation, exclusive of the angular ring, shall be within the visually extended boundaries of the solder pad (see Figure 2009-2).

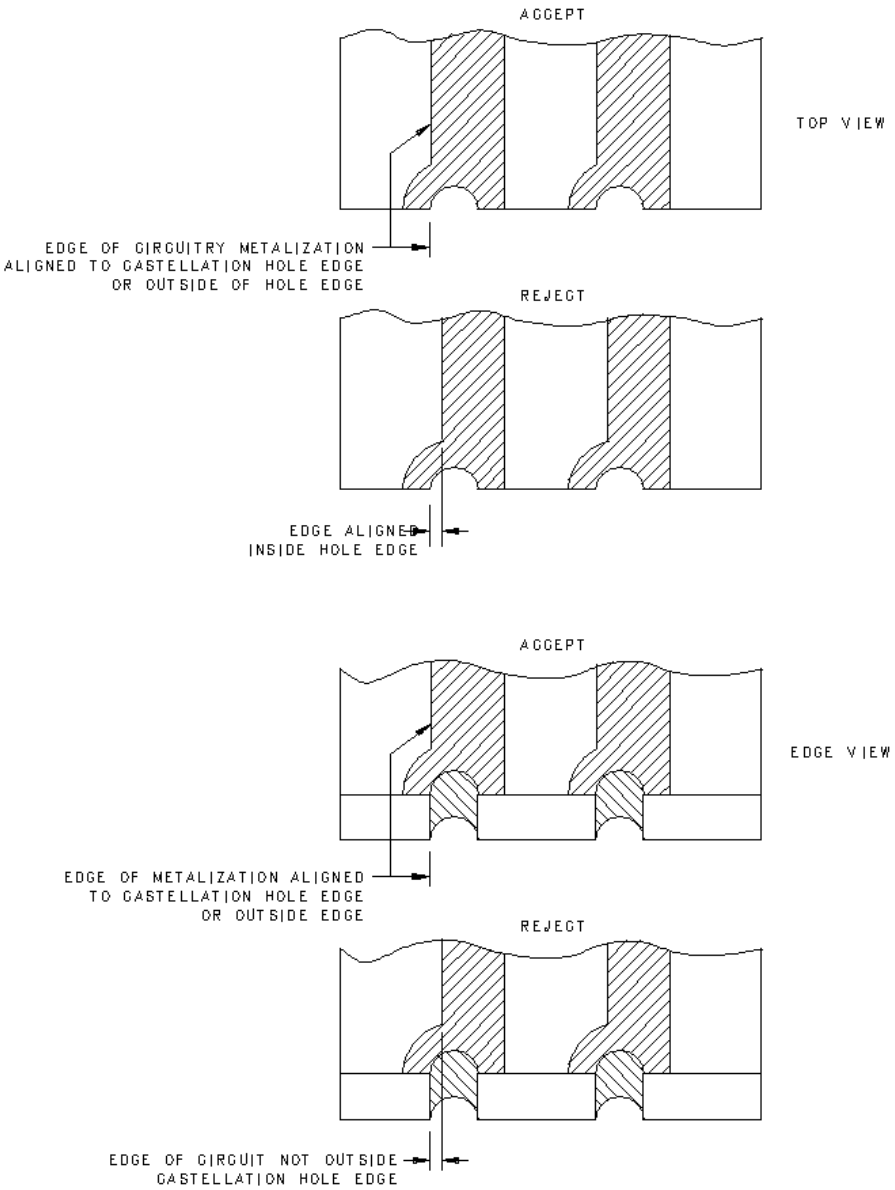

FIGURE 2009-2 Castellation to solder pad misalignment.

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d. Castellation configuration not in accordance with the following (see Figure 2009-3). The castellation shall be roughly concave, confined by a 3-dimensional space traversing all castellated ceramic layers at the package edge. The surface of the castellation may be irregular. The “3-dimensional space" has these dimensions:

1. Minimum width >1/3 package terminal pad width.

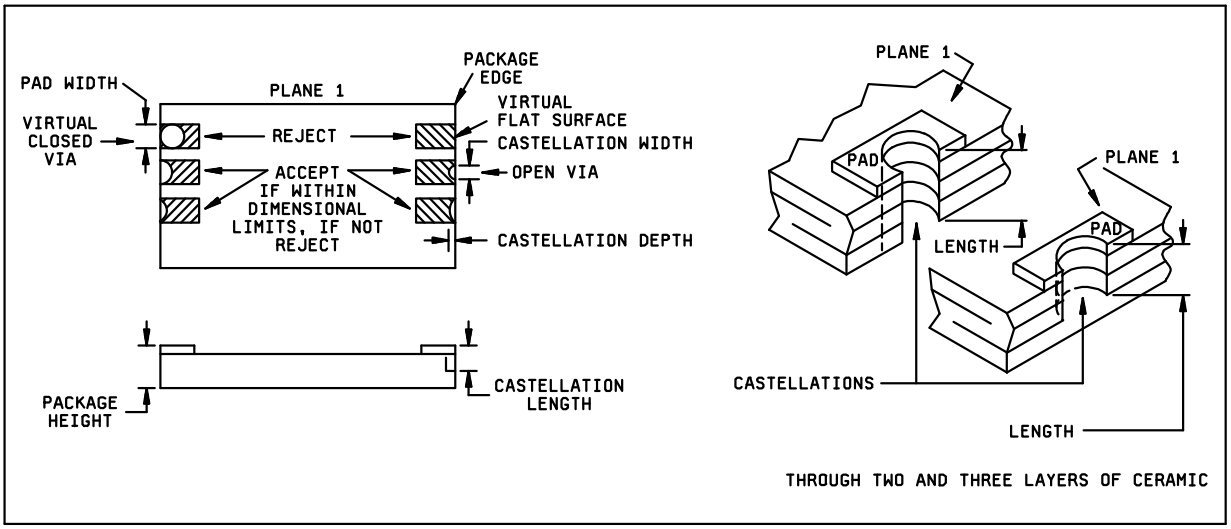
2. Minimum depth > 1/2 castellation minimum width.

3. Length = as designed (see Figure 2009-3).

4. Maximum width ≤ package terminal pad width.

5. Maximum depth ≤ 1/2 castellation maximum width.

These dimensions are an attempt to ensure with some reasonableness that the castellations are not viewed, in the extreme sense, as virtual flat surfaces on the package edge and are not virtual closed vias (holes).



NOTE: Ceramic layers shift, edges are rough after punching, plating buildup is not smooth etc., all of these combine during package manufacture to make the castellation measurement difficult. Therefore, in the event of conflicts in determining castellation acceptance, direct contact measurement shall be made using the limits specified in MIL-STD-1835.

FIGURE 2009-3 Castellation requirements.

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3.3.9 Glass seals.

a. Crazing of the glass seal surface (see Figure 2009-4).

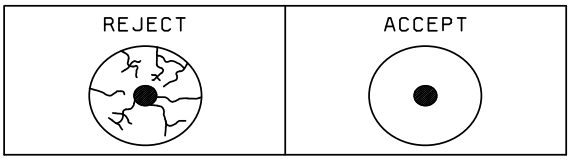

FIGURE 2009-4 Crazed glass surface.

b. Any single circumferential crack (or overlapping crack) that does not lie completely within a single quadrant (i.e., extends beyond 90° arc or rotation about the lead), and extends beyond or is located in the region beyond the midpoint of distance from the lead to the case (see Figure 2009-5).

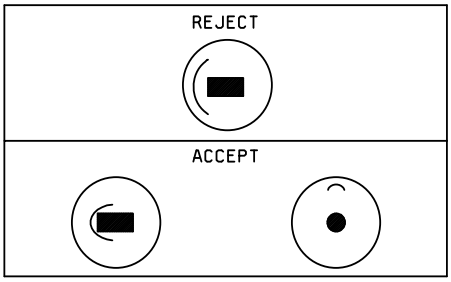

FIGURE 2009-5. Circumferential cracks.

c. Radial cracks that exhibit the following:

1. Cracks that do not originate at the lead (see Figures 2009-6a and 2009-6b).

2. Three or more cracks that extend beyond the midpoints of distance from the lead to the case (see Figure 2009-6c).

3. Two cracks that extend beyond the midpoint of the distance from the lead to the case and that lie within the same quadrant (see Figure 2009-6d).

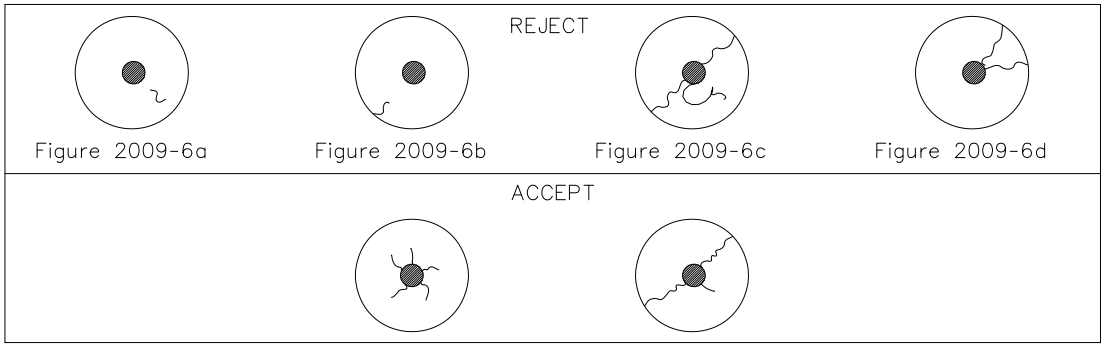

FIGURE 2009-6 Radial Cracks.

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d. Any chip-out that penetrates the sealing glass deeper than the glass meniscus plane. The glass meniscus is defined as that area of glass that wicks up the lead or terminal. Exposed base metal as a result of meniscus chip outs is acceptable, provided that the exposed area is no deeper than 0.010 inch (see Figure 2009-7).

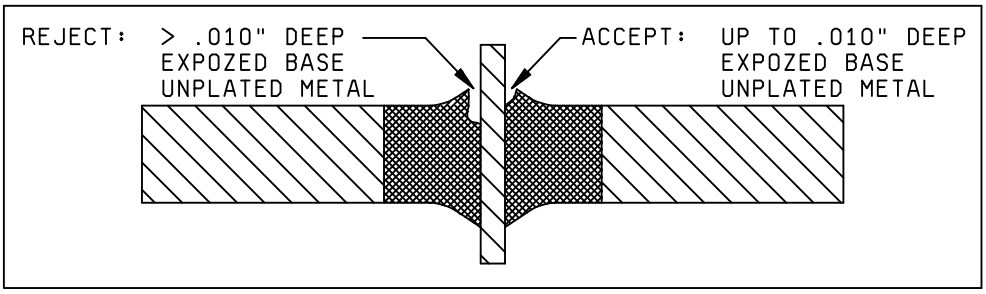

FIGURE 2009-7 Chip-outs.

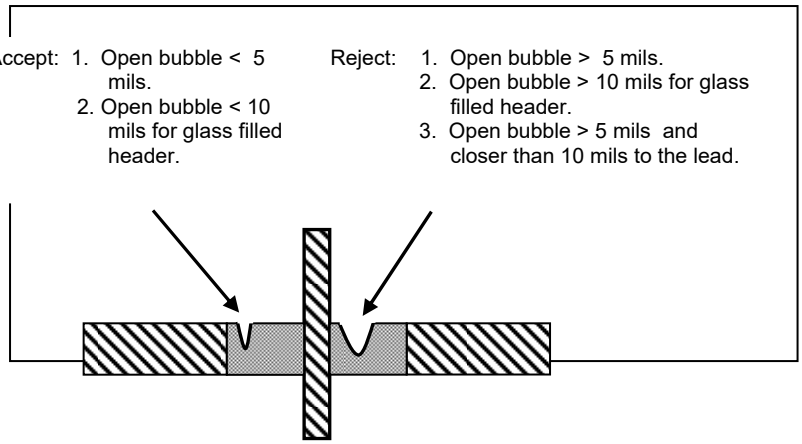

FIGURE 2009-8a Surface bubbles.

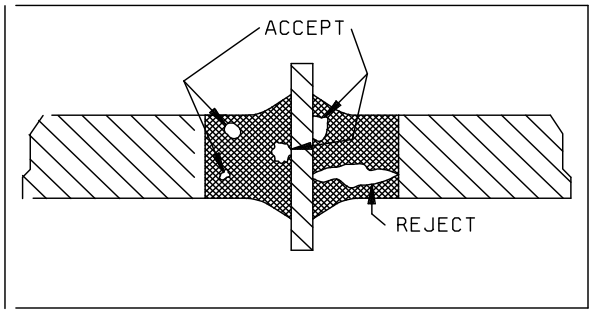

FIGURE 2009-8b Subsurface bubbles.

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e. Surface bubbles that exceed the following:

1. Open bubbles in the glass seal that exceed 5 mils in diameter (see Figure 2009-8a). For packages with a glass-filled header (i.e., TO-5), open bubbles that exceed 10 mils diameter, or an open bubble that exceeds 5 mils diameter situated closer than 10 mils to a lead.

2. Open bubbles in strings or clusters that exceed 2/3 of the distance between the lead and the package wall.

f. Subsurface bubbles that exceed the following:

1. Large bubbles or voids that exceed 1/3 of the glass sealing area (see Figure 2009-8a).

2. Single bubble or void that is larger than 2/3 of the distance between the lead and the package wall at the site of inclusion (see Figures 2009-8b and 2009-8c).

3. Two bubbles in a line totaling more than 2/3 distance from pin to case (see Figure 2009-8c).

4. Interconnecting bubbles greater than 2/3 the distance between pin and case (see Figure 2009-8d).

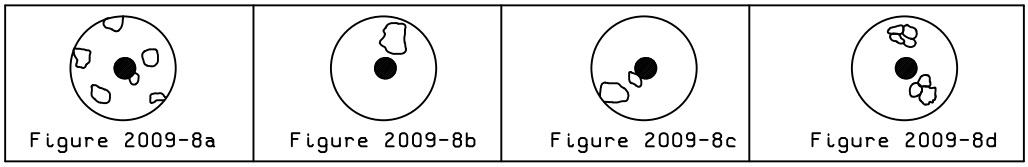

FIGURE 2009-9 Subsurface bubbles.

g. Reentrant seals that exhibit non-uniform wicking (i.e., negative meniscus) at the lead and/or body interface (see Figure 2009-10).

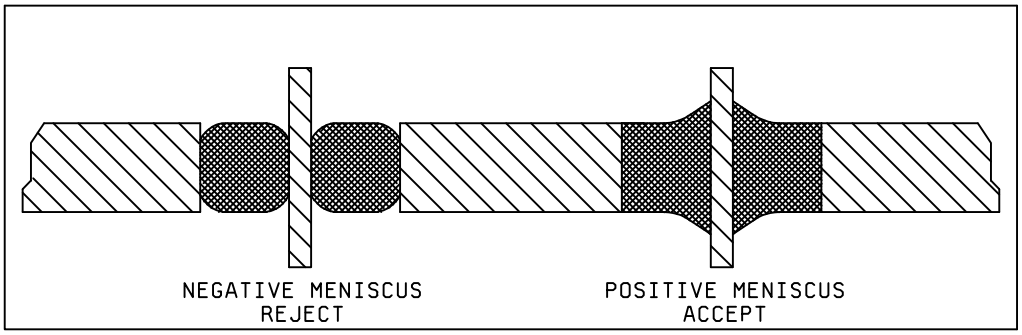

FIGURE 2009-10 Reentrant seals.

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4. SUMMARY. The following details shall be specified in the applicable acquisition document:

   a. Requirements for markings and the lead (terminal), or pin identification.

   b. Any additional detailed requirements for materials, design, construction, and workmanship.

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METHOD 2010.14

INTERNAL VISUAL (MONOLITHIC)

1. PURPOSE. The purpose of this test is to check the internal materials, construction, and workmanship of microcircuits for compliance with the requirements of the applicable acquisition document. This test will normally be used prior to capping or encapsulation on a 100 percent inspection basis to detect and eliminate devices with internal defects that could lead to device failure in normal applications. It may also be employed on a sampling basis prior to capping to determine the effectiveness of the manufacturer's quality control and handling procedures for microelectronic devices. Furthermore, the criteria of this test method will be used during destructive physical analysis (DPA) following the procedures outlined in test method 5009, "Destructive Physical Analysis". Test condition A and B provide a rigorous and detailed procedure for internal visual inspection of high reliability microcircuits as specified in the screening requirements of test method 5004. For condition B product the alternate screening procedure (alternate 1) documented in test method 5004 may be used by the manufacturer as an option to internal visual inspection as specified. For condition A or B product, the alternate screening procedure (alternate 2) documented in test method 5004 may be used by the manufacture as an option to internal visual inspection as specified.

2. APPARATUS. The apparatus for this test shall include optical equipment capable of the specified magnification and any visual standards (gauges, drawings, photographs, etc.) necessary to perform an effective examination and enable the operator to make objective decisions as to the acceptability of the device being examined. Adequate fixturing shall be provided for handling devices during examination to promote efficient operation without inflicting damage to the units.

2.1 GaAs device requirements. GaAs devices shall be inspected to all applicable criteria as listed herein. GaAs microwave devices shall also have additional specific criteria as listed and the applicable high power magnification for individual features of GaAs microwave devices shall be selected from the following table.

TABLE I. GaAs microwave device high magnification requirements.

Feature Dimensions	Magnification range
> 5 microns	75 - 150x
1 - 5 microns	150 - 400x
< 1 micron	400 - 1000x

2.2 Silicon-on-Sapphire (SOS) device requirements. SOS devices shall be inspected to all applicable criteria specified herein, except where noted. The sapphire portions of the die shall be considered "nonconductive and nonoperational material".

3. PROCEDURE.

a. General. The device shall be examined within the specified magnification range to determine compliance with the requirements of the applicable acquisition document and the criteria of the specified test condition.

The inspections and criteria in this method shall be required inspections for all devices and locations to which they are applicable. Where the criterion is intended for a specific device process or technology, it has been indicated.

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b. Sequence of inspection. The order in which criteria are presented is not a required order of examination and may be varied at the discretion of the manufacturer.

When inverted die mounting techniques are employed, the inspection criteria contained herein that cannot be performed after mounting shall be conducted prior to attachment of the die. Devices that fail any test criteria herein are defective devices and shall be rejected and removed at the time of observation.

Visual criteria may be inspected as follows:

(1) Prior to die attachment without re-examination after die attachment; 3.1.1.2, 3.1.1.5, 3.1.1.7, 3.1.2, 3.1.4 e and f, 3.1.5, 3.1.6 a-f, 3.2.6.

(2) Prior to bonding without re-examination after bonding; 3.2.3.

(3) For condition B only; the following criteria may be inspected prior to die attachment at high power, plus low power after die attachment, provided a high magnification sample to sample size number = 45 accept number C = 0 is performed at precap inspection; 3.1.1.1, 3.1.1.3, 3.1.1.4, 3.1.1.6, 3.1.3, 3.1.4 a-d and g-o, 3.1.6 g and h, 3.1.7. If the sample fails the entire lot shall be reinspected at high magnification for the failed criteria.

c. Inspection control. In all cases except die at incoming inspection, examination prior to final preseal inspection shall be performed under the same quality program that is required at the final preseal inspection station. Care shall be exercised after inspections in accordance with 3b, to insure that defects created during subsequent handling will be detected and rejected at final preseal inspection. During the time interval between visual inspection and preparation for sealing, devices shall be stored in a controlled environment. Devices examined to condition A shall be inspected and prepared for sealing in a Class 5 controlled environment and devices examined to condition B criteria shall be inspected and prepared for sealing in a Class 8 controlled environment (see A.4.8.1.1.7 of appendix A of MIL-PRF-38535), except that the maximum allowable relative humidity in either environment shall not exceed 65 percent. Devices shall be in covered containers when transferred from one controlled environment to another.

d. Magnification. "High magnification" inspection shall be performed perpendicular to the die surface with the device under illumination perpendicular to the die surface. "Low magnification" inspection shall be performed with a metallurgical or stereomicroscope with the device under suitable illumination. Low magnification may be performed at an angle other than 90° to the die surface to facilitate the inspection. The inspection criteria of 3.2.1 may be examined at "high magnification" at the manufacturer's option.

e. Reinspection. When inspection for product acceptance is conducted subsequent to the manufacturer's inspection, the additional inspection may be performed at any magnification specified by the applicable test condition, unless a specific magnification is required by the acquisition document. When suspected defects or deficiencies are noted, additional inspection may be performed at magnifications needed to evaluate or resolve the suspect items.

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f. Definitions:

(1) Active circuit area. All areas enclosed by the perimeter of functional circuit elements, operating metallization or any connected combinations thereof excluding beam leads.

(2) Coupling (air) bridge. A raised layer of metallization used for interconnection that is isolated from the surface of the element.

(3) Block resistor. A thin film resistor which for purposes of trimming is designed to be much wider than would be dictated by power density requirements and shall be identified in the approved manufacturer's precap visual implementation document.

(4) Contact Via. The Via where dielectric material is etched away in order to expose the Under Bump Metalization (UBM) on the bond pads or solder bump attach pads.

(5) Channel. An area lying between the drain and the source of FET structures.

(6) Controlled environment (Clean Room). An environment maintained for humidity and atmospheric particle count in accordance with ISO 14644-1. A Class 5 controlled environment has no more than 100 (0.5 µm or greater) particles/cubic-feet or air, a Class 6 controlled environment has no more than 1,000 (0.5 µm or greater) particles/cubic-foot of air, and a Class 8 controlled environment has no more than 100,000 (0.5 µm or greater) particles/cubic-foot of air, except that the maximum allowable relative humidity shall not exceed 65 percent.

(7) Crazing. The presence of numerous minute cracks in the referenced material, (e.g., glassivation crazing).

(8) Detritus. Fragments of original or laser modified resistor material remaining in the kerf.

(9) Die Coat. A thin layer of soft polyimide coating applied to the surface of a semiconductor element that is intended to produce stress relief resulting from encapsulation and to protect the circuit from surface scratches.

(10) Dielectric isolation. Electrical isolation of one or more elements of a monolithic semiconductor integrated circuit by surrounding the elements with an isolating barrier such as semiconductor oxide.

(11) Dielectric layer or layers. Dielectric layer or layers deposited on the die surface to protect the redistribution metalization, and to create the contact via for solder bump pad.

(12) Diffusion tub. A volume (or region) formed in a semiconductor material by a diffusion process (n- or p-type) and isolated from the surrounding semiconductor material by a n-p or p-n junction or by a dielectric material (dielectric isolation, coplanar process, SOS, SOI).

(13) Foreign material. Any material that is foreign to the microcircuit or package, or any nonforeign material that is displaced from its original or intended position within the microcircuit package.

(14) Functional circuit elements. Diodes, transistors, crossunders, capacitors, and resistors.

(15) Gate oxide. The oxide or other dielectric that separates gate metallization (or other material used for the gate electrode) from the channel of MOS structures (see figure 2010-1).

(16) Glassivation. The top layer(s) of transparent insulating material that covers the active circuit area, with the exception of bonding pad areas and beam leads.

(17) Glassivation cracks. Fissures in the glassivation layer.

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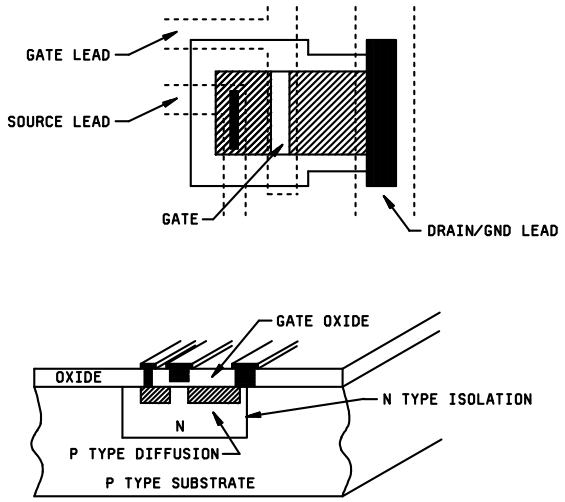

FIGURE 2010-1. P channel MOS transistor.

(18) Junction line. The outer edge of a passivation step that delineates the boundary between "P" and "N" type semiconductor material. An active junction is any P/N junction intended to conduct current during normal operation of the circuit element, (e.g., collector to base).

(19) Kerf. That portion of the component area from which material has been removed or modified by trimming or cutting.

(20) Line of separation. Visible distance or space between two features that are observed not to touch at the magnification in use.

(21) MESFET. (Metal semiconductor field-effect transistor). A field-effect transistor in which a metal semiconductor rectifying contact is used for the gate electrode. Typically the structure is fabricated in gallium arsenide and the term GaAs MESFET may be used. Both depletion-type and enhancement type devices have been manufactured. The acronyms are D-MESFET, and E-MESFET, respectively.

(22) Metallization nonadherence. Unintentional separation of material from an underlying substrate excluding air bridges and undercutting by design.

(23) Multilayered metallization (conductors). Two or more layers of metal or any other material used for interconnections that are not isolated from each other by insulating material. The term "underlying metal" shall refer to any layer below the top layer of metal (see figure 2010-2).

(24) Multilevel metallization (conductors). Two or more levels of metal or any other material used for interconnections that are isolated from each other by insulating material (also referred to as interlevel dielectric) (see figure 2010-3).

(25) Narrowest resistor width. The narrowest portion of a given resistor prior to trimming.

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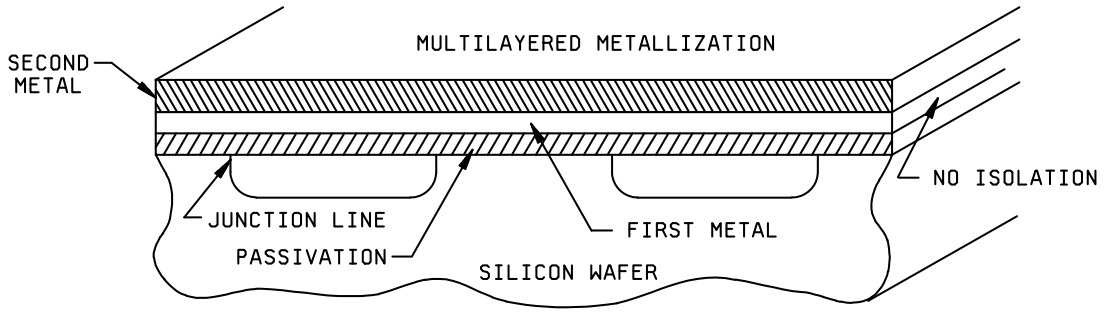

FIGURE 2010-2. Multilayered metallization.

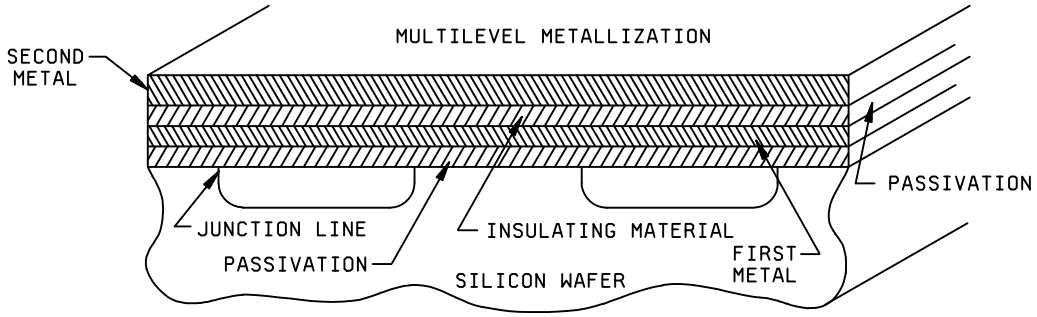

FIGURE 2010-3. Multilevel metallization.

(26) Operating metallization (conductors). Metal or any other material used for interconnection except metallized scribe lines, test patterns, unconnected functional circuit elements, unused bonding pads, and identification markings.

(27) Original width. The width dimension or distance that would have been present, in the absence of the observed abnormality (e.g., original metal width, original diffusion width, original beam width, etc.).

(28) Package post. A generic term used to describe the bonding location on the package.

(29) Passivation. The silicon oxide, nitride or other insulating material that is grown or deposited directly on the die prior to the deposition of metal or between metal levels on multilevel devices.

(30) Passivation step. An abrupt change of elevation (level) of the passivation such as a contact window, or operating metallization crossover.

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(31) Peripheral metal. All metal that lies immediately adjacent to or over the scribe grid.

(32) Redistribution Layer (RDL). Layer added to original wafer/die surface to allow for the redistribution of bond pads into a format more suitable to flip chip.

(33) Redistribution metalization. The metal deposited on the RDL to create the electrical conductors which connect the original bond pads to the distributed solder bump pads.

(34) Shooting metal. Metal (e.g., aluminum, gold) expulsion of various shapes and lengths from under the wire bond at the bonding pad.

(35) Solder ball. Solder ball or sphere attached to the UBM through the contact via after a re-flow process.

(36) Solder Bump. Solder that is either electroplated or screened into the photo resist opening. After the photo resist is removed the solder resembles a bump before it is reflowed into ball or sphere.

(37) Substrate. The supporting structural material into or upon which or both the passivation, metallization and circuit elements are placed.

(38) Substrate via. A small hole formed through the wafer and metallized, causing electrical connection to be made from the frontside (the side on which the circuitry is formed) to the backside of the wafer.

(39) Thick film. That conductive/resistive/dielectric system that is a film having greater than 50,000Å thickness.

(40) Thin film. That conductive/resistive/dielectric system that is a film equal to or less than 50,000Å in thickness.

(41) Under Bump Metalization (UBM). Metals deposited on top of the aluminum bond pads or on the solder bump pads that enhance wetting and protect against intermetalic reactions between the solder and the original metal on the pads.

(42) Via metallization. That which connects the metallization of one level to another.

g. Interpretations. Reference herein to "that exhibits" shall be considered satisfied when the visual image or visual appearance of the device under examination indicates a specific condition is present and shall not require confirmation by any other method of testing. When other methods of test are to be used for confirming that a reject condition does not exist, they shall be approved by the acquiring activity. For inspections performed on the range of 75X to 100X, the criteria of 0.1 mil of passivation, separation or metal can be satisfied by a line of separation or a line of metal visible.

h. Foreign material control. The manufacturer shall perform an audit on a weekly basis for (1) the presence of foreign material within incoming piece part lids and bases, and (2) the presence of foreign material on the die surface or within the package of assembled parts.

The audit of assembled parts may be satisfied during routine internal visual inspection. If the presence of foreign material is discovered, the manufacturer shall perform the necessary analysis on a sample of the foreign material on the suspect devices to determine the nature of the material. The manufacturer shall document the results of this investigation and corrective action to eliminate the foreign material and this information will be available to the Government QAR, and the acquiring activity or the qualifying activity, as applicable. A corrective action plan shall be obtained within a maximum of 10 working days of discovery.

The audit of incoming piece part lids and bases shall be performed before parts are assembled, or may be satisfied during routine incoming quality inspection. If the presence of foreign material of a size 1 mil or greater is discovered, the manufacturer will analyze the foreign material to determine its nature and document the results of the analysis. If applicable, these results shall be distributed to the vendor supplying the parts, with the request that the vendor document corrective actions to minimize or eliminate such foreign material. This information will be available to the manufacturer, Government QAR, and the acquiring activity or qualifying activity, as applicable.

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NOTE: The piece part audit requirements can be replaced by a piece part cleaning process, approved by the qualifying activity, that is always performed either prior to or during the assembly process and these piece parts are stored in a controlled environment until they are used.

The intent of these procedures is to require investigation and resolution of foreign material problems that do not have an effective screening or detection methodology but that could cause degradation and eventual failure of the device function. Repetitive findings without obvious improvements require escalation to Director of Manufacturing and Director of Quality Assurance to continue processing.

Condition A Class level S	Condition B Class level B

3.1 High power inspection. Internal visual examination as required in 3.1.1 through 3.1.3 shall be conducted on each microcircuit. In addition, the applicable criteria contained in 3.1.4 through 3.1.7 shall be used for the appropriate microcircuit area where glassivation, dielectric isolation or film resistors are used.

NOTE: Unless otherwise specified, for flip chip product the criteria of 3.1 shall apply only to top circuit side inspection. After die mounting, only criteria in 3.1.3i shall apply.

The high magnification inspection shall be within the range of 100X to 200X.	The high magnification inspection shall be within the range of 75X to 150X.

For high magnification inspection of GaAs microwave devices, see table I herein. Also, for < 1 micron features, the manufacturer may implement a sample inspection plan which shall be documented in the manufacturer's internal procedure and approved by the qualifying activity.

3.1.1 Metallization defects. No device shall be acceptable that exhibits the following defects in the operating metallization.

3.1.1.1 Metallization scratches:

a. Scratch in the metallization excluding bonding pads and beam leads that leaves less than 50 percent of the original metal width undisturbed (see figure 2010-4).	a. Scratch in the metallization, excluding bonding pads and beam leads, that exposes underlying passivation anywhere along its length and leaves less than 50 percent of the original metal width undisturbed (see figure 2010-5).

NOTE: For GaAs microwave devices, scratches in the gate stripe or gate insertion metallization.

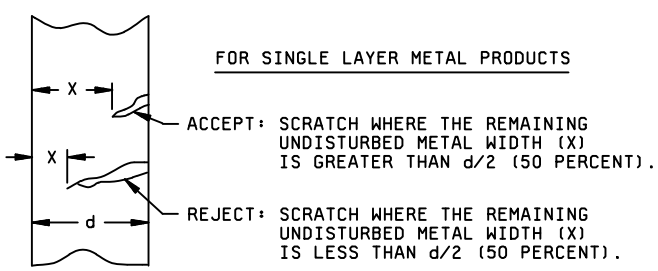

FIGURE 2010-4. Metallization scratch criteria for class level S.

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Condition A
Class level S

Condition B
Class level B

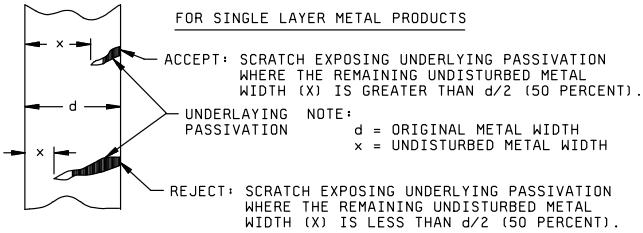
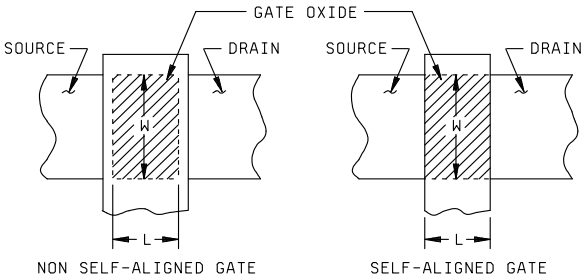


FIGURE 2010-5. Metallization scratch criteria for class level B.

b. For condition A, see 3.1.1.1a above.

b. For condition B only. Scratch that completely crosses a metallization path and damages the surface of the surrounding passivation, glassivation, or substrate on either side (for MOS devices, the path shall be the (L) dimension) (see figure 2010-6).



NOTE: When standard metallization scratch criterion is applied to the gate area, the dimensions (W) and (L) shall be considered as the original channel width and length respectively.

FIGURE 2010-6. MOS scratch criteria.

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Condition A
Class level S

Condition B
Class level B

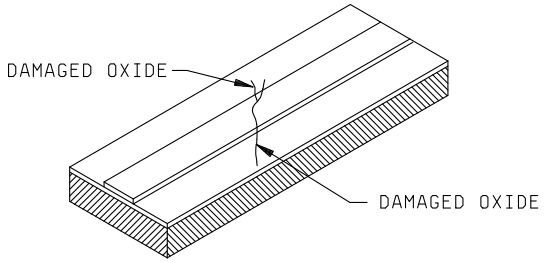

FIGURE 2010-6. MOS scratch criteria - Continued.

c. Scratch in multilayered metallization, excluding bonding pads and beam leads that exposes underlying metal or passivation anywhere along its length and leaves less than 75 percent of the original metal width undisturbed (see figure 2010-7).

c. Scratch in multilayered metallization, excluding bond pads and beam leads that exposes the underlying metal anywhere along its length and leaves less than 25 percent of the original metal width undisturbed (see figure 2010-8).

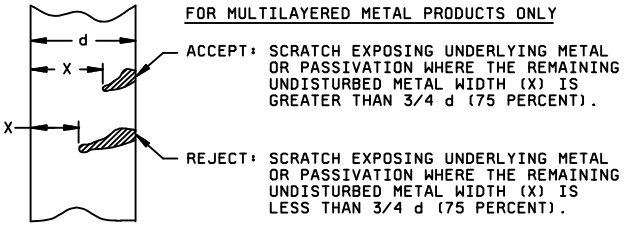

FIGURE 2010-7. Scratch criteria for class level S.

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Condition A
Class level S

Condition B
Class level B

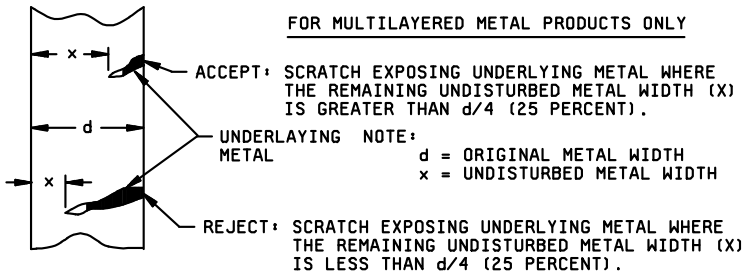

FIGURE 2010-8 Scratch criteria for class level B.

NOTE: For condition B only. Criteria 3.1.1.1a, b, and c can be excluded for peripheral power or ground metallization where parallel paths exist such that an open at the scratch would not cause an unintended isolation of the metallization path.

d. Scratch in the metallization over a passivation step that leaves less than 75 percent of the original metal width at the step undisturbed.

NOTE: For condition B only. Criteria 3.1.1.1a, b, c, and d can be excluded for the last 25 percent of the linear length of the contact cut and all metal beyond, on the termination end(s) of the metallization runs. In these cases there shall be at least 50 percent of the contact opening area covered by metallization and at least a continuous 40 percent of the contact opening perimeter covered by undisturbed metallization (see figure 2010-9).

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Condition A
Class level S

Condition B
Class level B

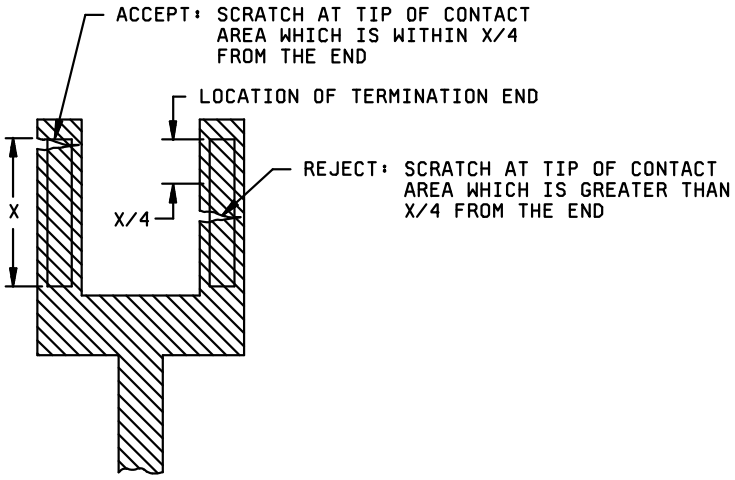

FIGURE 2010-9. Termination ends.

e. Scratch in the metallization, over the gate oxide (applicable to MOS structures only) (see figure 2010-10).

e. Scratch in the metallization, over the gate oxide, that exposes underlying passivation and leaves less than 50 percent of the length or width of the metallization between source and drain diffusion undisturbed (applicable to MOS structures only) (see figure 2010-11).

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Condition A
Class level S

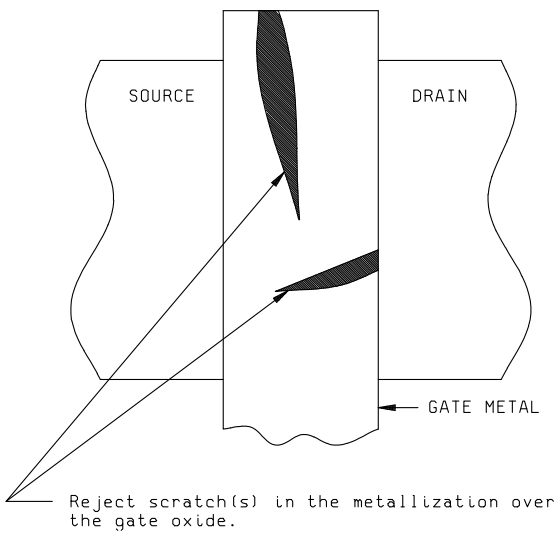

FIGURE 2010-10. MOS scratch criteria for class level S.

Condition B
Class level B

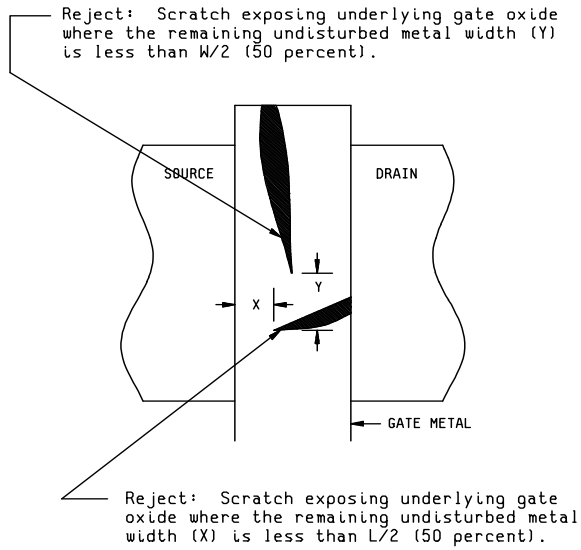

FIGURE 2010-11. MOS scratch criteria for class level B.

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Condition A Class level S	Condition B Class level B
f. Scratch in the metallization that exposes the dielectric material of a thin film capacitor or crossover. (Not applicable to air bridges.)	
g. Scratch in the bonding pad or fillet area that reduces the metallization path width connecting the bond to the interconnecting metallization to less than 50 percent of the narrowest entering interconnect metallization stripe width. If two or more stripes enter a bonding pad, each shall be considered separately.	g. Scratch in the bonding pad or fillet area that exposes underlying passivation or substrate and reduces the metallization path width connecting the bond to the interconnecting metallization to less than 50 percent of the narrowest entering interconnect metallization stripe width. If two or more stripes enter a bonding pad, each shall be considered separately.

h. Scratch(es) (probe mark(s), etc.) in the bonding pad area that exposes underlying passivation, or substrate, and leaves less than 75 percent of the unglassivated metallization area undisturbed.

i. For GaAs devices only, any tears, peeling, gaps, and lateral displacement of metal.

3.1.1.2 Metallization voids;

a. Void(s) in the metallization that leaves less than 75 percent of the original metal width undisturbed (see figure 2010-12).	a. Void(s) in the metallization that leaves less than 50 percent of the original metal width undisturbed (see figure 2010-13).

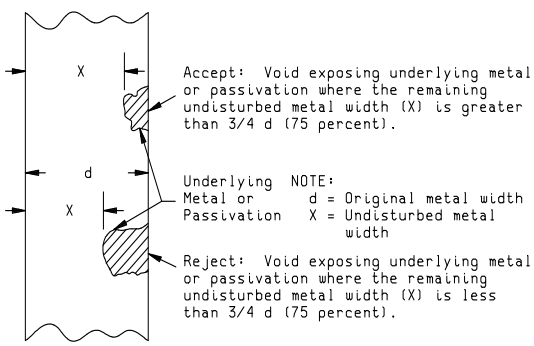

FIGURE 2010-12. Void criteria for class level S.

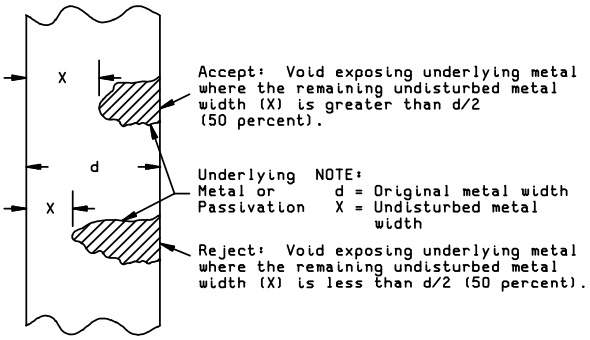

FIGURE 2010-13. Void criteria for class level B.

NOTE: For condition B only. Criteria can be excluded for peripheral power or ground metallization where parallel paths exist so that an open at the void(s) would not cause an unintended isolation of the metallization path.

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Condition A Class level S	Condition B Class level B

b. Void(s) in the metallization over a passivation step that leaves less than 75 percent of the original metal width at the step undisturbed.

NOTE: For condition B only. Criteria of 3.1.1.2a and b can be excluded for the last 25 percent of the linear length of the contact cut and all metal beyond on the termination end(s) of metallization runs. In these cases there shall be at least 50 percent of the contact opening perimeter covered by undisturbed metallization (see figure 2010-14).

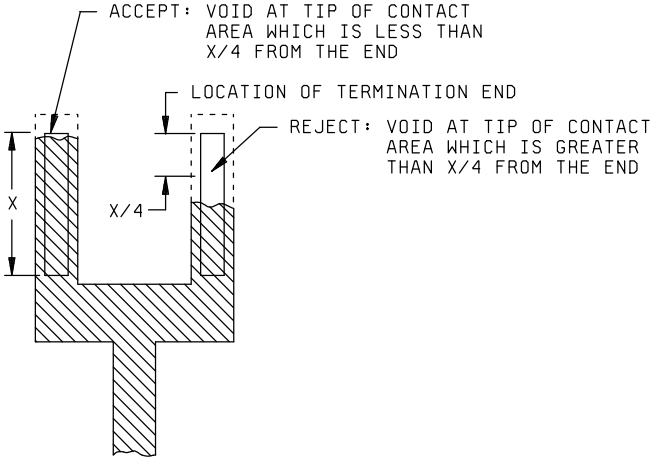

FIGURE 2010-14. Termination ends.

c. Void(s) in the metallization over the gate oxide that leaves less than 75 percent of the metallization length (L) or width (W) between source and drain diffusions undisturbed (applicable to MOS structures only) (see figure 2010-15).

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Condition A Class level S	Condition B Class level B
d. Void(s) that leave less than 75 percent of the metallization area over the gate oxide undisturbed (applicable to MOS structures only).	d. Void(s) that leave less than 60 percent of the metallization area over the gate oxide undisturbed (applicable to MOS structures only).

e. Void(s) that leaves less than 75 percent of the metallization width coincident with the source or drain diffusion junction line undisturbed (applicable to MOS structures only) (see figure 2010-15).

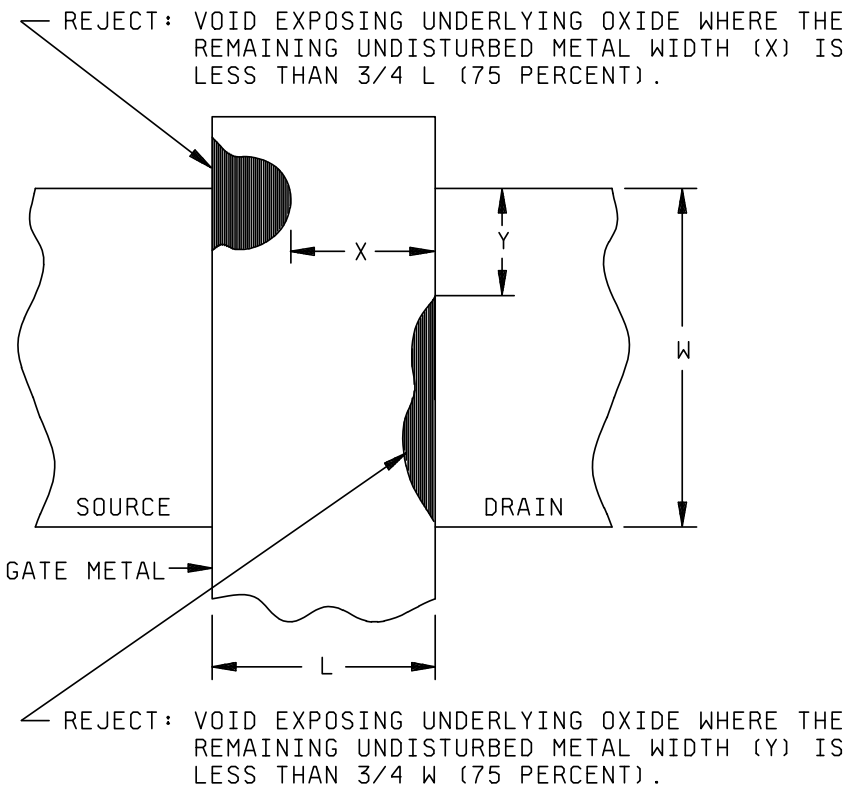

FIGURE 2010-15. MOS void criteria.

f. Void(s) in the bonding pad area that leaves less than 75 percent of its original unglassivated metallization area undisturbed (see figure 2010-16).

g. Void(s) in the bonding pad or fillet area that reduces the metallization path width connecting the bond to the interconnecting metallization to less than 75 percent of the narrowest entering metallization stripe width. If two or more stripes enter a bonding pad,each shall be considered separately. (see figure 2010-16).	g. Void(s) in the bonding pad or fillet area that reduces the metallization path width connecting the bond to the interconnecting metallization to less than 50 percent of the narrowest entering metallization stripe width. If two or more stripes enter a bonding pad, each shall be considered separately (see figure 2010-16).

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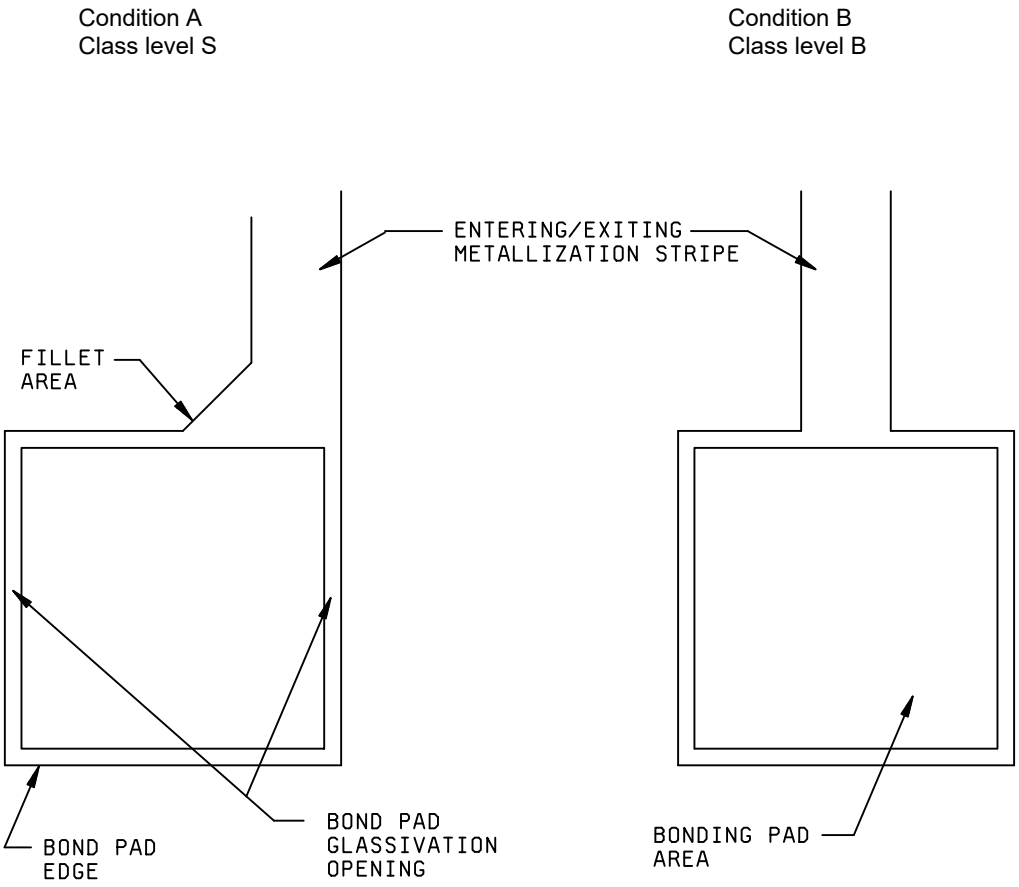

FIGURE 2010-16. Bond pad terminology.

NOTE: When a fillet area exists, it is to be considered as part of the entering/exiting metallization stripe.

h. Void(s) in the metallization area of a thin film capacitor that leave less than 75 percent of the designed metallization area.

i. For GaAs microwave devices only, voids in the gate stripe.

3.1.1.3 Metallization corrosion. Any metallization corrosion. Metallization having any localized discolored area shall be closely examined and rejected, unless it is demonstrated to be a harmless film, glassivation interface, or other obscuring effect.

3.1.1.4 Metallization nonadherence. Any metallization lifting, peeling, or blistering.

3.1.1.5 Metallization probing. Criteria contained in 3.1.1.1 shall apply as limitations on probing damage.

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Condition A Class level S	Condition B Class level B

3.1.1.6 Metallization bridging.

NOTE: For SOS devices, exclude the insulator scribe lines.

a. Any metallization bridging where the separation between metallization paths is reduced to less than 50 percent of the original design.

b. Any metal that is displaced, as a result of bonding, from its original position on the bonding pad (shooting metal) greater than 1.0 mils or that reduces the separation between unglassivated operating metallization or scribe line and the bonding pad to less than 0.25 mils or 50 percent design separation, whichever is less.

a. Any metallization bridging where a line of separation is not visible between metallization paths.

NOTE: For GaAs microwave devices, metallization bridging across spacings of less than 1 μm shall be inspected only in accordance with 3.2 and table I at 400X to 1,000X. If a clear line of separation is not discernible, device functional testing at the wafer level shall suffice.

b. Any metal that is displaced, as a result of bonding, from its original position on the bonding pad (shooting metal) that reduces the separation between unglassivated operating metallization or scribe line and the bonding pad such that a line of separation is not visible.

3.1.1.7 Metallization alignment.

a. Contact window that has less than 75 percent of its area covered by metallization.

b. Contact window that has less than a continuous 50 percent of its perimeter covered by metallization.

a. Contact window that has less than 50 percent of its area covered by metallization.

b. Contact window that has less than 40 percent of its perimeter covered by metallization.

c. Contact window that has less than 75 percent of its perimeter on two adjacent sides covered by metallization (applicable to MOS structures only).

NOTE: When, by design, metal is completely contained in a contact window or does not cover the entire contact perimeter, criteria 3.1.1.7a, b, or c can be deleted, provided the design criteria is satisfied.

d. A metallization path not intended to cover a contact window that is not separated from the contact window by a line of separation.

e. Any exposure of the gate oxide (i.e., oxide not covered by gate electrode in the area between source and drain diffusions, applicable to MOS structures only) (see figure 2010-17).

3.1.1.8 Via hole metallization. For GaAs devices only,

a. Overetched via hole or misaligned via visible around the pad.

b. Poor adhesion (lifting, peeling or blistering).

c. Any cracks originating at the via hole.

d. Evidence of bulging metal over a via hole.

e. Evidence of solder coming up through via hole pad, when die is mounted on a carrier.

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Condition A	Condition B
Class level S	Class level B

3.1.1.9 Coupling (air) bridge defects "high magnification". For GaAs devices only. No element shall be acceptable that exhibits:

a. A void in the coupling (air) bridge metallization that leaves less than 75 percent of the original metallization width undisturbed. (see figure 2010-17A).

b. Nodules or bumps that are greater, in any dimension, than the original coupling (air) bridge metallization width. (See figure 2010-17A)

c. Coupling (air) bridge that contacts underlying operating metallization. (See figure 2010-17A)

d. Attached, conductive foreign material that is greater, in any dimensions, than 50% of the original coupling (air) bridge metallization width.

e. No visible separation between the coupling (air) bridge and the underlying operating metallization.

NOTE: This criterion is not applicable when an insulating material is used between the coupling (air) bridge and the underlying metallization. (See figure 2010-17A)

f. Coupling (air) bridge metallization overhang over adjacent operating metallization, not intended by design, that does not exhibit a visible separation. (See figure 2010-17A)

g. Mechanical damage to a coupling (air) bridge that results in depression (lowering) of coupling (air) bridge metallization over underlying operating metallization.

NOTE: Air bridges which are depressed, over operating metallization, due to normal backside processing are not considered mechanically damaged. A visual line of separation still applies in accordance with 3.1.1.9e.

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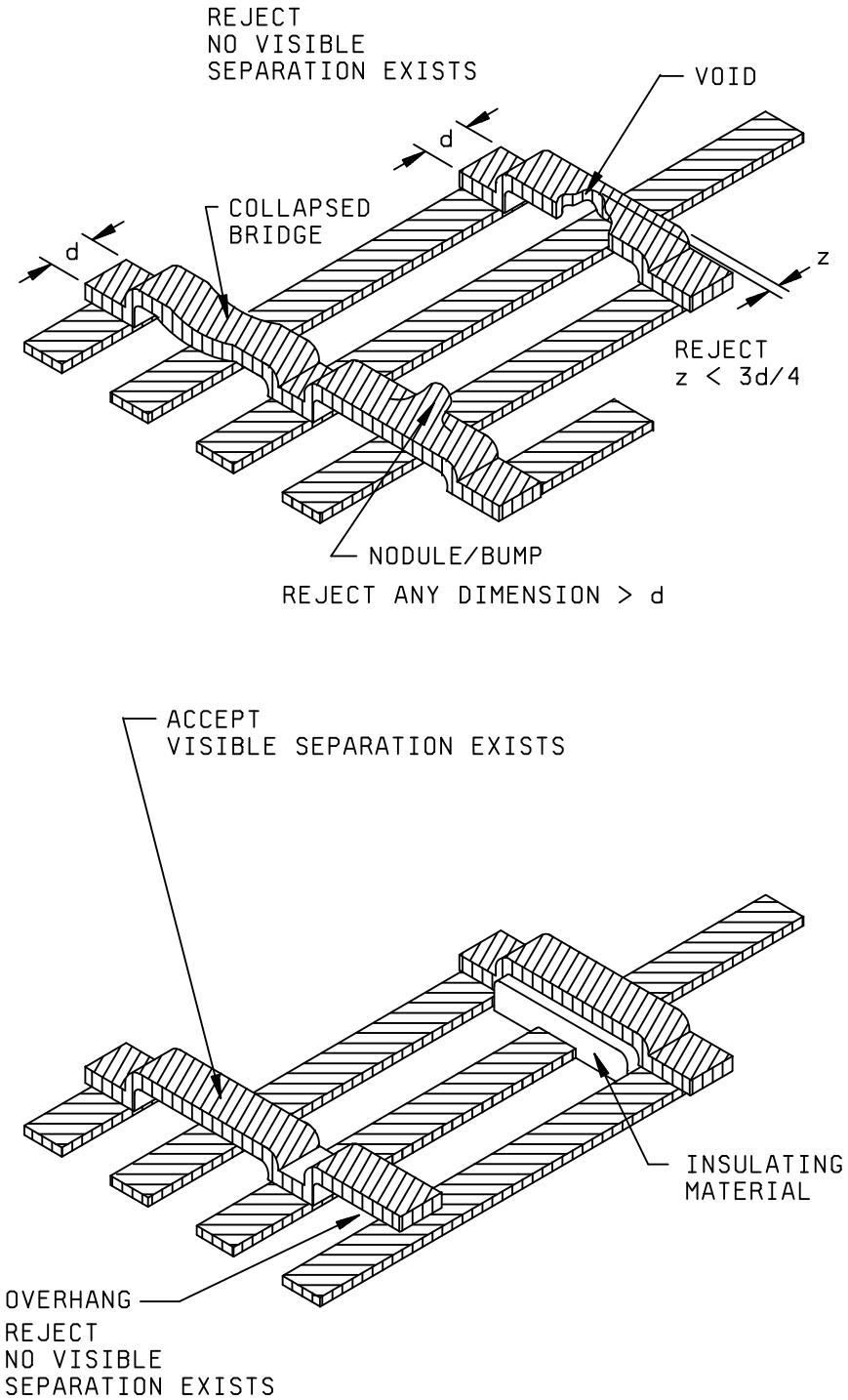

FIGURE 2010-17A. Class level S and Class level B coupling (air) bridge criteria.

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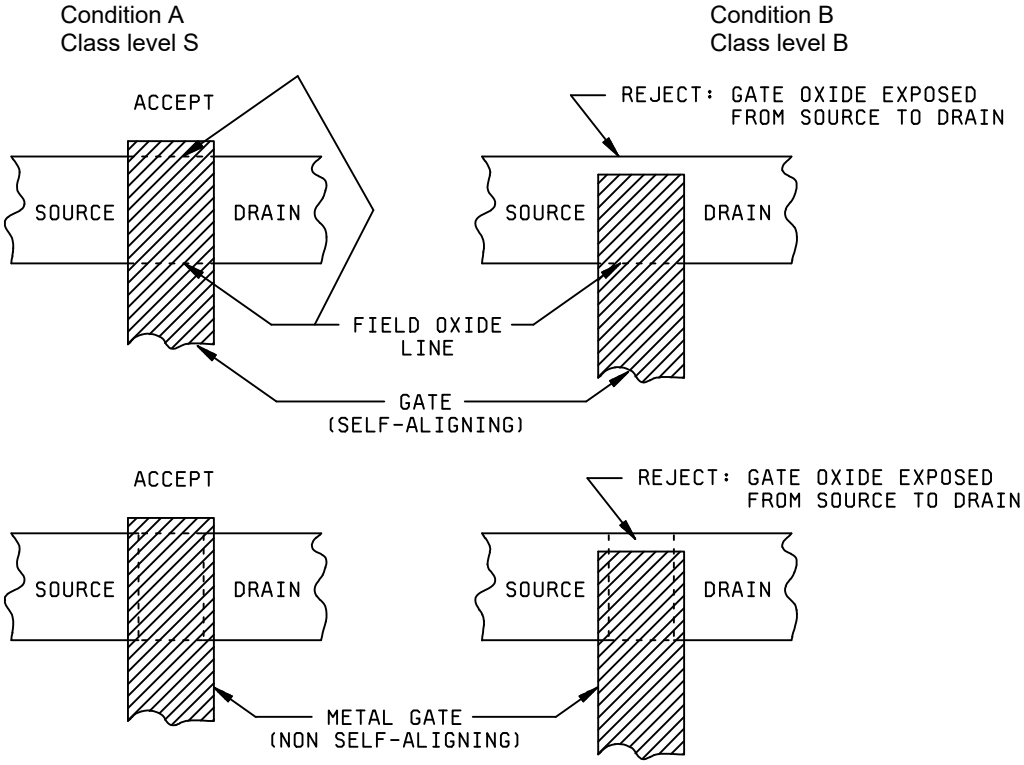

FIGURE 2010-17. MOS gate alignment.

h. For MOS structures containing a diffused guard ring, gate metallization not coincident with or not extending over the diffused guard ring (see figure 2010-18).

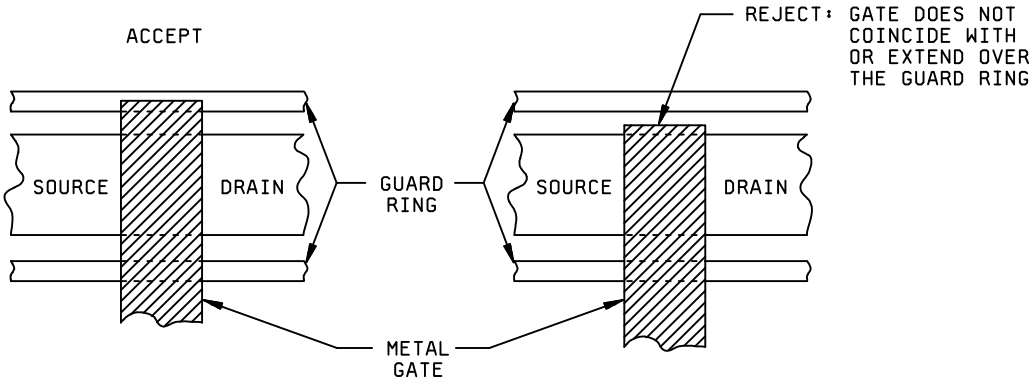

FIGURE 2010-18. MOS gate alignment.

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Condition A Class level S	Condition B Class level B

3.1.2 Diffusion and passivation layer faults. No devices shall be acceptable that exhibits the following:

3.1.2.1 Diffusion faults.

a. Diffusion fault that allows bridging between diffused areas (see figure 2010-19).

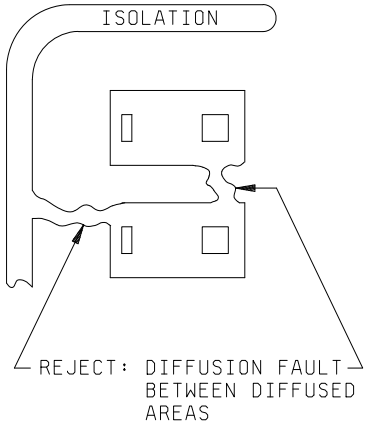

FIGURE 2010-19. Diffusion faults.

b. Any isolation diffusion that is discontinuous (except isolation walls around unused areas or unused bonding pads) or any other diffused area with less than 25 percent (50 percent for resistors) of the original diffusion width remaining (see figure 2010-20).

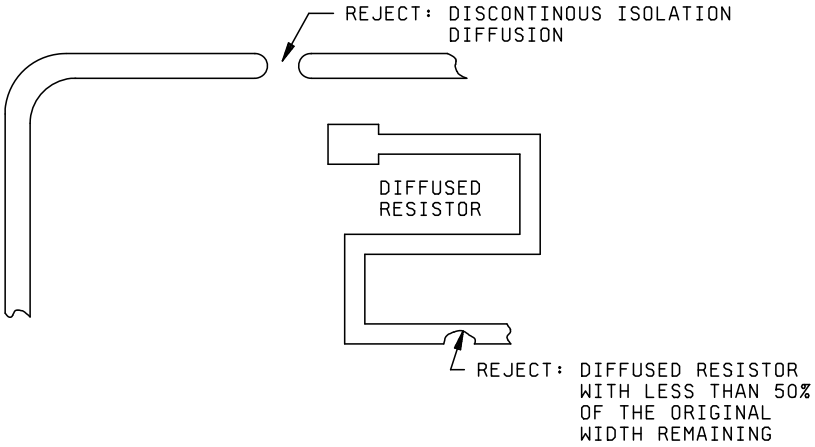

FIGURE 2010-20. Diffusion faults.

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Condition A Class level S	Condition B Class level B

3.1.2.2 Passivation faults.

NOTE: For SOS devices, exclude defects between first-level conductive interconnect (metallization, polysilicon, ect.) and sapphire areas of the die, where no active circuit elements are present.

a. Either multiple lines or a complete absence of passivation visible at the edge and continuing under the metallization unless by design for GaAs devices. Multiple lines indicate that the fault can have sufficient depth to penetrate down to bare semiconductor material.

NOTE: The multiple line criteria can be excluded when a second passivation layer is applied in a separate operation prior to metallization deposition or for bond pads located in isolated tubs.

NOTE: For condition B only. Should the absence of glassivation in the defect area or the characteristics of the glassivation present allow verification of the presence or absence of passivation by color or color comparisons respectively, then these techniques may be used (see figure 2010-21).

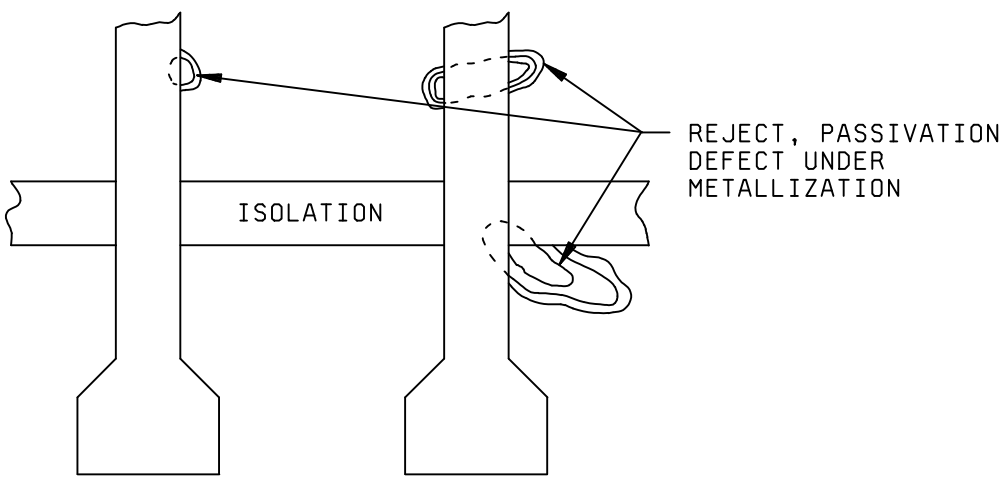

FIGURE 2010-21. Passivation faults.

b. Active junction line not covered by passivation, unless by design.

c. Contact window that extends across a junction line, unless by design.

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Condition A Class level S	Condition B Class level B

3.1.3 Scribing and die defects. No device shall be acceptable that exhibits:

a. Less than 0.25 mil of passivation visible between operating metallization or bond periphery and bare semiconductor material (see figure 2010-22).	a. No line of separation between operating metallization or bond periphery and bare semiconductor material (see figure 2010-22).

NOTE: For GaAs devices only, less than 0.1 mil of substrate visible between operating metallization or bond periphery and edge of the die.

NOTE: Criteria can be excluded for beam leads and peripheral metallization including bonding pads where the metallization is at the same potential as the substrate.

NOTE: Does not apply to SOS devices.

b. A chipout or crack in the active circuit area (see figures 2010-22 and 2010-38). In addition for GaAs a chipout into or underneath the functional metallization, e.g., bond pads, capacitors, peripheral metallization, etc., but excluding test structures of the device.

NOTE: Criteria can be excluded for peripheral metallization that is at the same potential as the substrate. At least 50 percent undisturbed metallization width shall remain at the chipout.

c. A crack that exceeds 3.0 mils in length, or comes closer than 0.25 mils to any operating metallization (except for substrate potential peripheral metal) or functional circuit element (see figure 2010-22).	c. A crack that exceed 5.0 mils in length, or that does not exhibit a line of separation to any operating metallization (except for substrate potential peripheral metal) or function circuit element (see figure 2010-22).
d. For condition A only. Semicircular crack(s) terminating at the die edge, whose chord is long enough to bridge the narrowest spacing between unglassivated operating material (e.g.,metallization, bare semiconductor material, mounting material, bonding wire, etc.) (see figure 2010-22).	d. No condition B.

.

e. Exposed semiconductor material extending over the passivation edge at the point of the beam lead exit from the die (applicable to beam lead structures only) (see figure 2010-38).

f. Die having attached portions of the active circuit area of another die.

g. A crack that exceeds 1.0 mil in length inside the scribe line (or semiconductor material edge for beam lead devices) that points toward operating metallization or functional circuit elements (see figure 2010-22).

h. A crack that comes closer than 0.5 mil to operating beam lead metallization (see figure 2010-38).

NOTE: Criteria of 3.1.3c and h can be excluded for beam lead devices where the chipout or crack does not extend into the semiconductor material.

NOTE: Criteria of 3.1.3e and h do not apply to GaAs devices.

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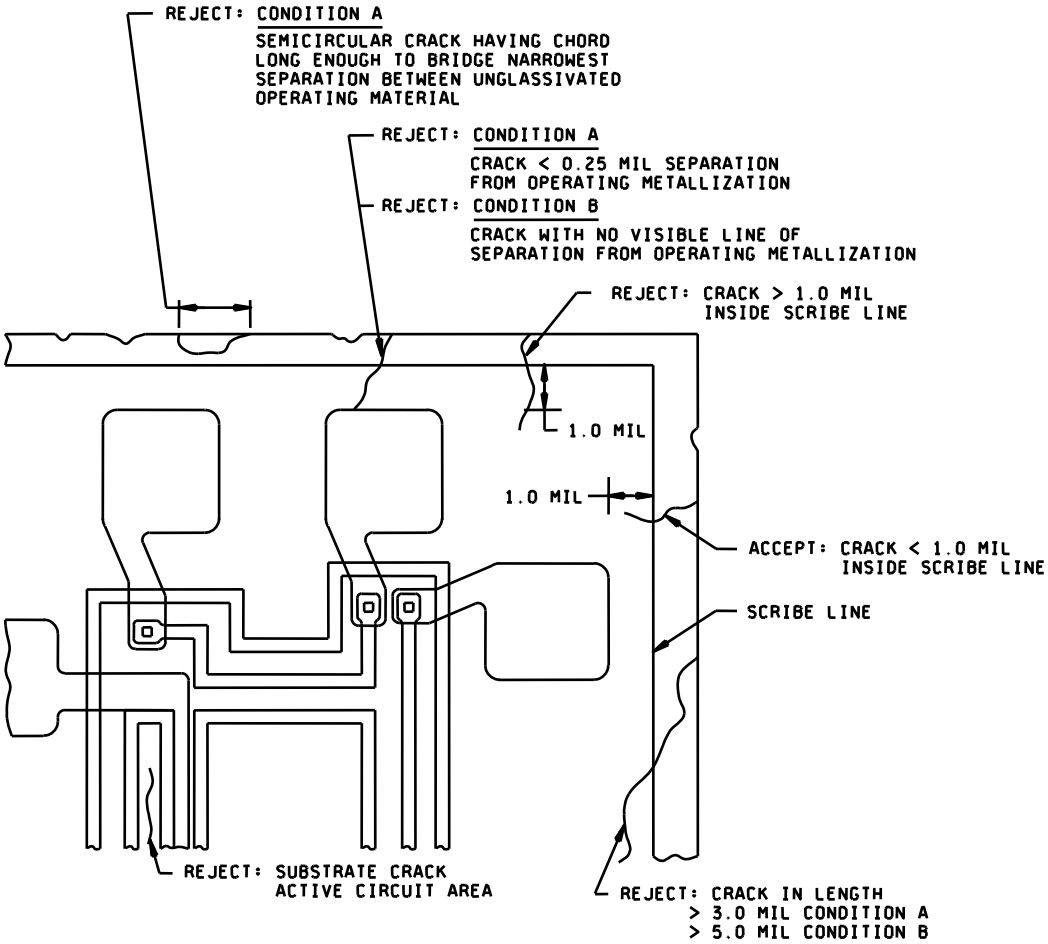

FIGURE 2010-22 Scribing and die defects.

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Condition A Class level S	Condition B Class level B

i. For flip chip, cracks, or chipouts in the substrate material that extends beyond 50 percent of substrate thickness or a crack greater than 5.0 mils in length in the substrate material (see figure 2010-23).

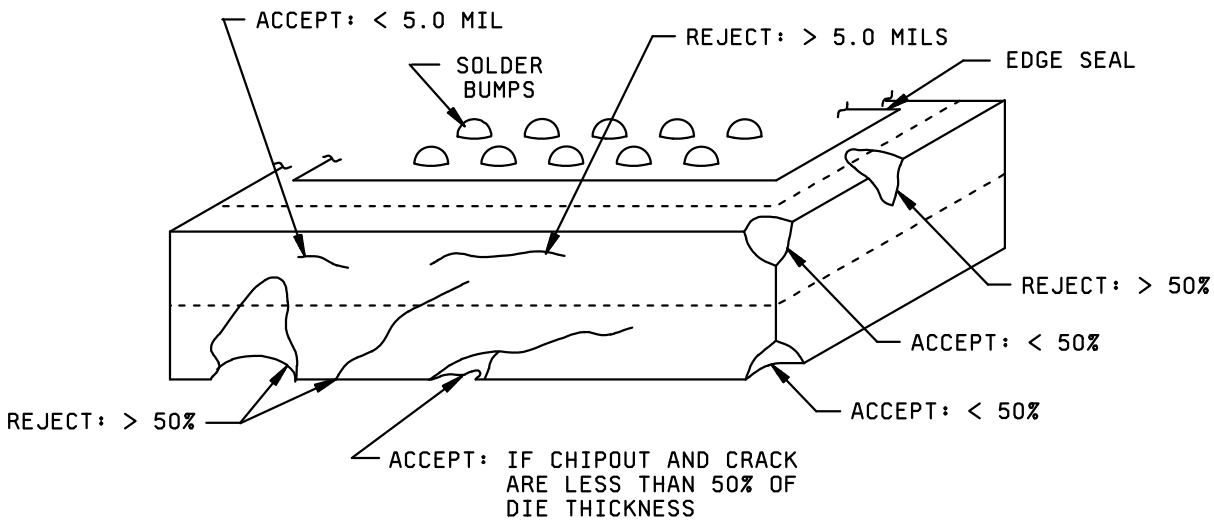

FIGURE 2010-23. Scribing and die defects.

j. Any blistering, peeling, delamination, corrosion, or other gross defects in glassivation, metal, interlevel dielectrics or other layers.

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Condition A Class level S	Condition B Class level B

3.1.4 Glassivation defects. No device shall be acceptable that exhibits (see figure 2010-24):

NOTE: For condition B only. Criteria of 3.1.4 can be excluded when the defect(s) is due to laser trimming. In this case, the defects outside the kerf due to laser trimming shall not be more than one half the remaining resistor width and shall leave a primary resistor path free of glassivation defects, equal to or greater than one half times the narrowest resistor width.

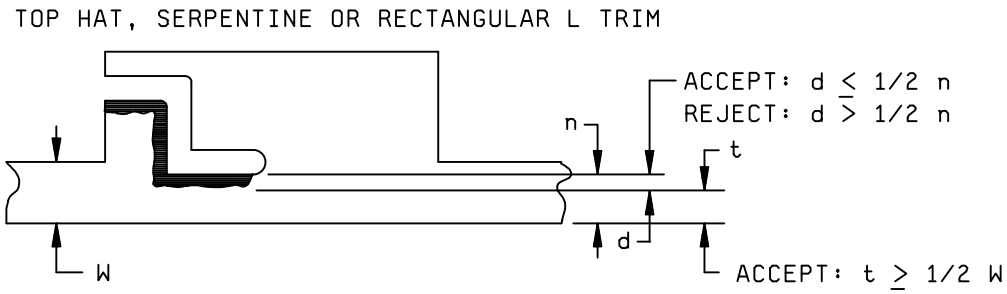

FIGURE 2010-24. Laser trimmed glassivation defects.

a. Glass crazing or glass damage that prohibits the detection of visual criteria contained herein.

b. Any lifting or peeling of the glassivation in the active areas or which extends more than 1.0 mil distance from the designed periphery of the glassivation.

c. A glassivation void that exposes two or more active metallization paths, except by design.

d. Unglassivated areas greater than 5.0 mils in any dimension, unless by design.

e. Unglassivated areas at the edge of bonding pad exposing bare semiconductor material, except by design.

f. Glassivation covering more than 25 percent of the designed open contact bonding area.

g. Crazing over a film resistor.

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Condition A Class level S	Condition B Class level B

h. Scratch(es) in the glassivation that disturbs metal and bridges metallization paths.

i. Crack(s) (not crazing) in the glassivation that forms a closed loop over adjacent metallization paths.

j. Glassivation void(s) that exposes any portion of a thin film resistor or fusible link except where the glassivation is opened by design.

k. For GaAs devices, voids in the glassivation that extends over the gate channel of the FET.

l. For GaAs devices, scratches in the glassivation over the gate channel of the FET.

m. For GaAs devices, scratches in the glassivation over the gate insertion of the FET.

n. For GaAs devices, cracks in the glassivation which are more than 1.0 mil inside the scribe line, or are more than 50 percent of the distance between the scribe line and any functional or active element (e.g., capacitor, resistor, FET) and which point toward any functional or active element unless the crack terminates at a device feature (e.g., transmission line or dc line).

3.1.5 Dielectric isolation. No device shall be acceptable that exhibits:

a. A discontinuous isolation line (typically a black line) around each diffusion tub containing functional circuit elements (see figure 2010-25).

b. Absence of a continuous isolation line between any adjacent tubs, containing functional circuit elements (see figure 2010-25).

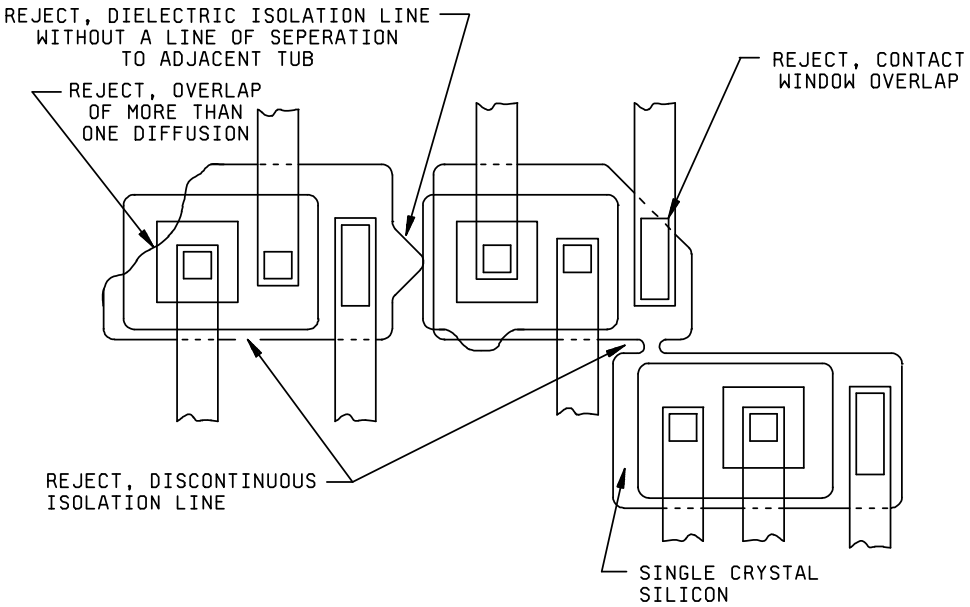

FIGURE 2010-25. Dielectric isolation defects.

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Condition A Class level S	Condition B Class level B

c. A diffused area which overlaps dielectric isolation material and does not exhibit a line of separation to an adjacent tub, or an overlap of more than one diffusion area into the dielectric isolation material (see figure 2010-25).

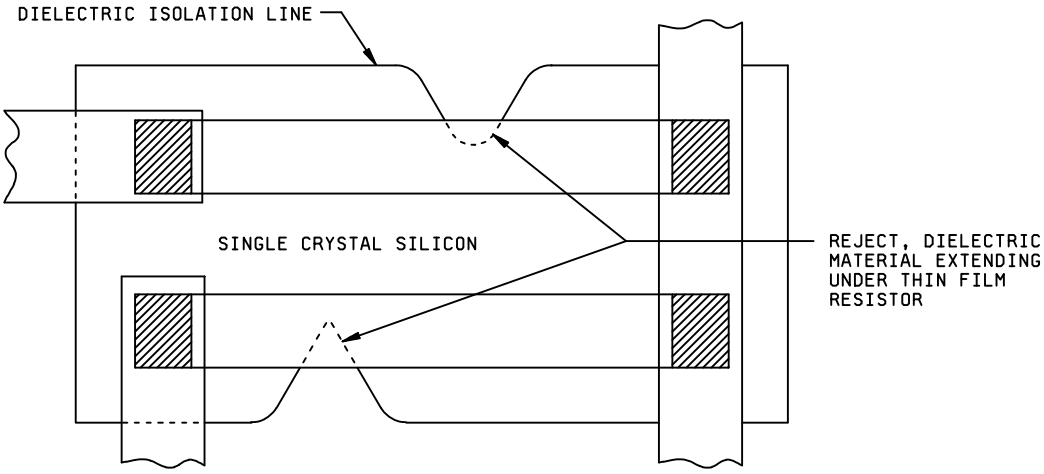

FIGURE 2010-26. Dielectric isolation defects.

d. A contact window that touches or overlaps dielectric material, except by design.

NOTE: Metallization scratch and void defects over a dielectric isolation step shall be rejected in accordance with criteria contained in 3.1.1.1d and 3.1.1.2b.

3.1.6 Film resistor. Rejection shall be based on defects found within the actively used portions of the film resistor. Metallization defect criteria of 3.1.1 shall apply as applicable. No device shall be acceptable that exhibits:

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Condition A Class level S	Condition B Class level B

a. Any misalignment between the conductor/resistor in which the actual width X of the overlap is less than 50 percent of the original resistor width.

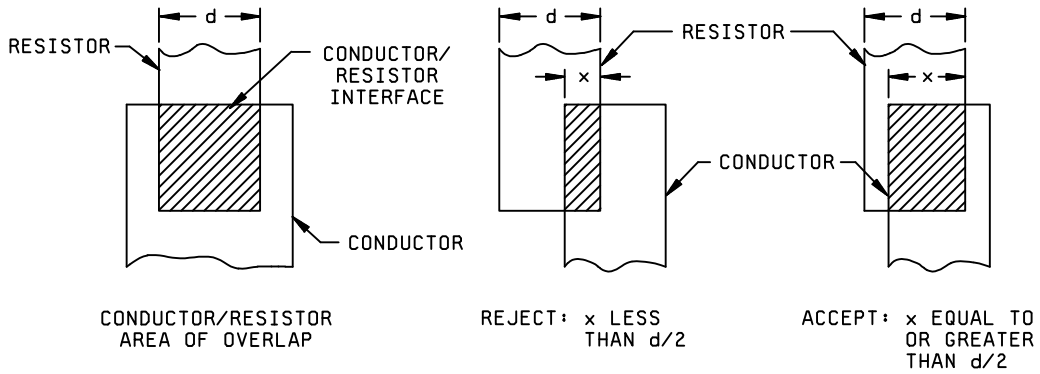

FIGURE 2010-27. Film resistor contact area.

b. No visible line of contact overlap between the metallization and film resistor (see figure 2010-28).

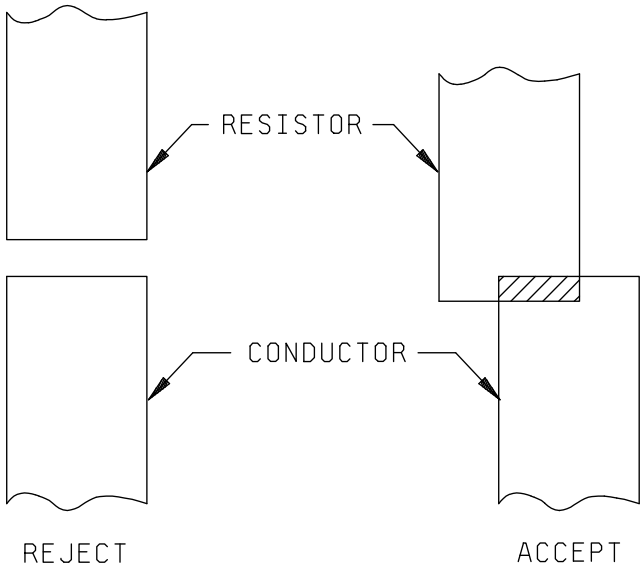

FIGURE 2010-28. Film resistor contact area.

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Condition A Class level S	Condition B Class level B

c. Void or necking down that leaves less than 75 percent of the film resistor width undisturbed at a terminal.

d. Inactive resistor inadvertently connected to two separate points on an active circuit.

e. Separation between any two resistors or a resistor and a metallization path that is less than 0.25 mil, or 50 percent of the design separation, whichever is less.

f. Any thin film resistor that crosses a substrate irregularity (e.g., dielectric isolation line, oxide/diffusion step, etc.) (see figure 2010-26).

NOTE: This criteria does not apply to square isolated islands of single crystal silicon in the polysilicon area.

g. Any resistor width reduced to less than one half the narrowest resistor width, resulting from voids or scratches or a combination thereof (see figure 2010-29).

NOTE: Maximum allowable current density requirements shall not be exceeded.

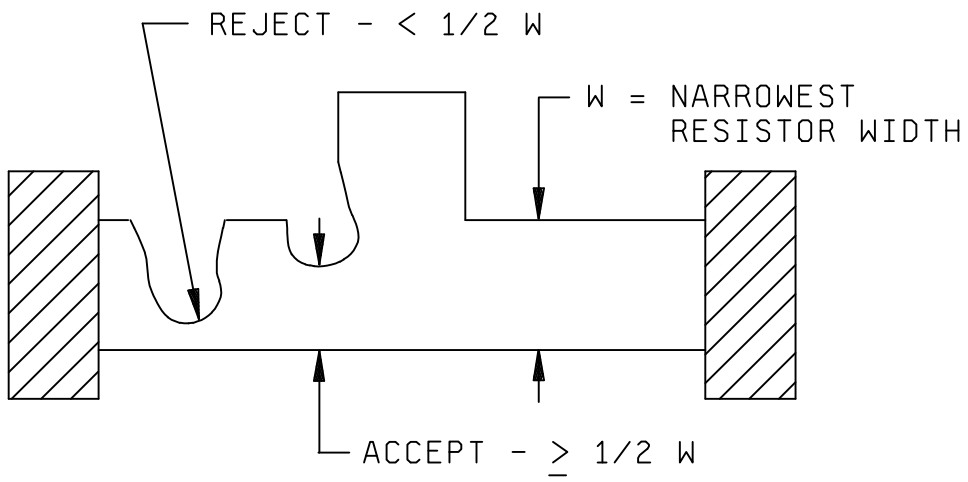

FIGURE 2010-29. Scratch and void criteria for untrimmed resistors.

h. Any sharp change in color of resistor material within 0.1 mil of the resistor/connector termination.

3.1.7 Laser-trimmed thin-film resistors. Rejection shall be based on defects found within the actively used portions of the film resistor. No device shall be acceptable that exhibits:

a. A kerf less than 0.1 mil in width, unless by design.

NOTE: Criteria does not apply for edge trimming.

b. A kerf containing particles of detritus.

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Condition A Class level S	Condition B Class level B

c. A kerf containing untrimmed resistor material, unless that material is continuous across the kerf, and is undisturbed for a width greater than one-half times the narrowest resistor width, unless by design (see figure 2010-30).

NOTE: Maximum allowable current density requirements shall not be exceeded.

Top hat trim

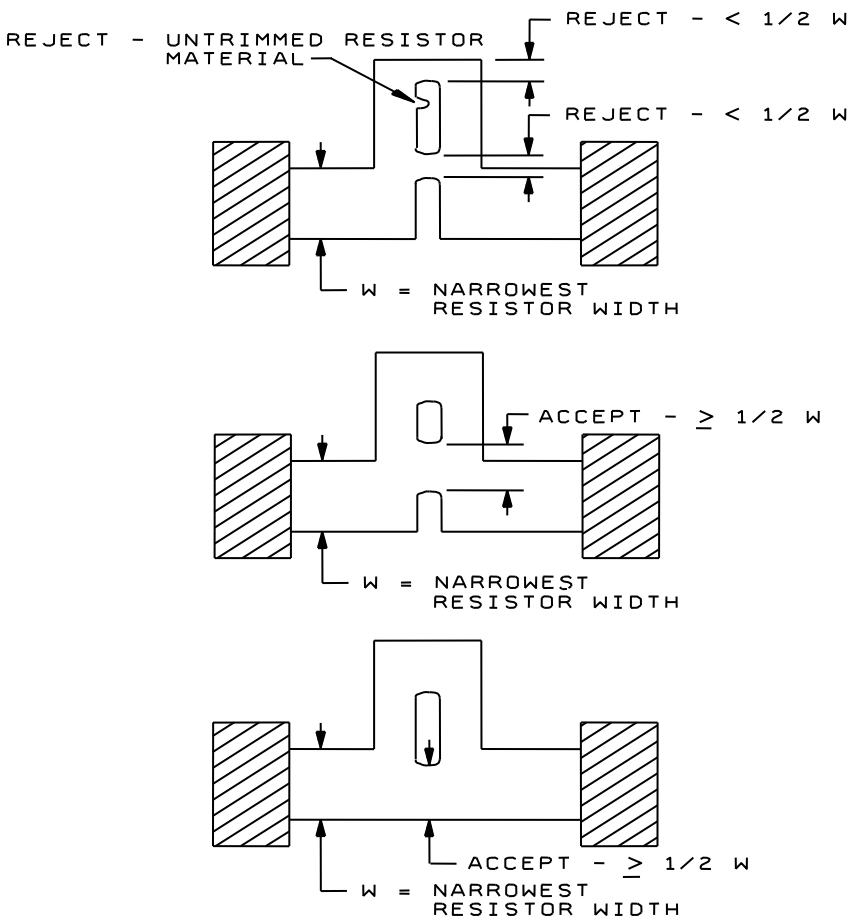

FIGURE 2010-30. Resistor Criteria.

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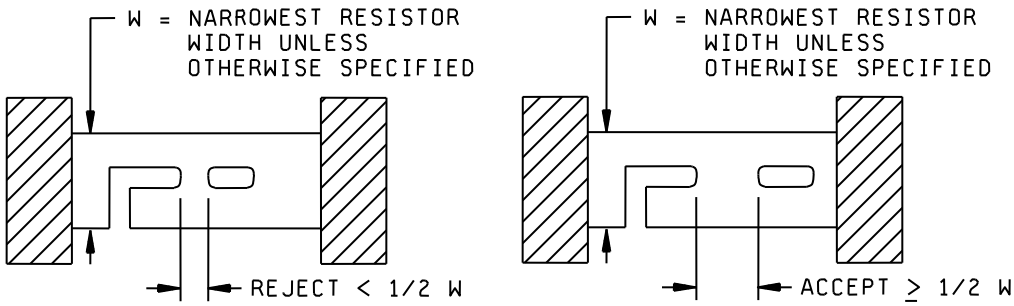
Condition A
Class level S

Condition B
Class level B



Rectangular L trim

FIGURE 2010-30. Resistor Criteria - Continued.

d. Resistor width that has been reduced by trimming to less than one-half the narrowest resistor width, including voids, scratches, or a combination thereof, in the trim area (see figure 2010-31).

NOTE: Trimming of more than 50 percent of a given resistor shunt link is acceptable by design providing that the last shunt link of the resistor adder network is not trimmed greater than 50 percent. All trimmable resistor shunt links shall be defined on the design layout drawing.

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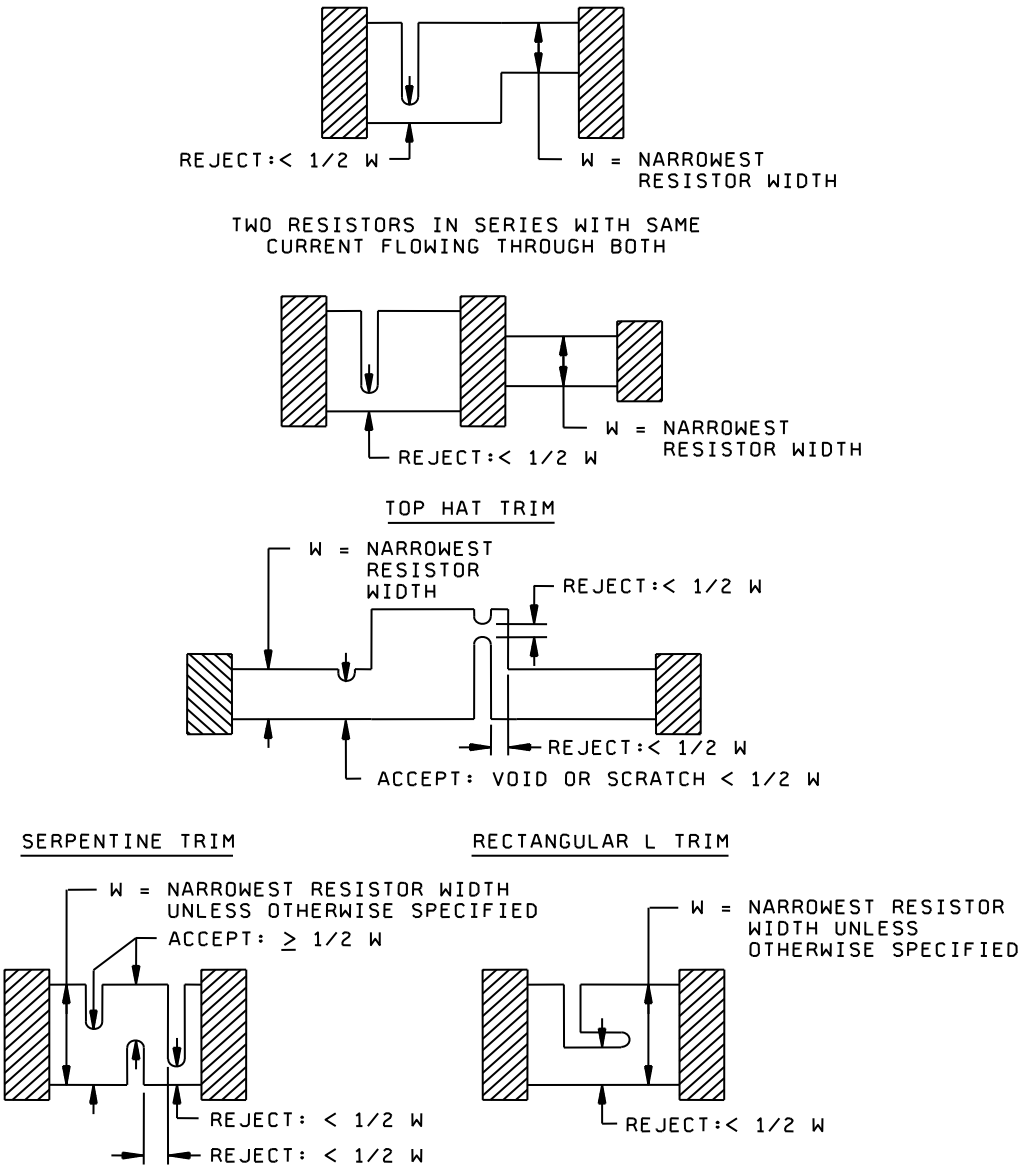

FIGURE 2010-31. Scratch, void and trim criteria for resistors.

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Condition A Class level S	Condition B Class level B

e. Trim path into the metallization except block resistors.

NOTE: This criteria can be excluded for trim paths into terminator ends of metallization runs. Conductors or resistors may be trimmed open for link trims or by design.

f. Trim for block resistors which extends into the metallization (excluding bonding pads) more than 25 percent of the original metal width (see figure 2010-32).

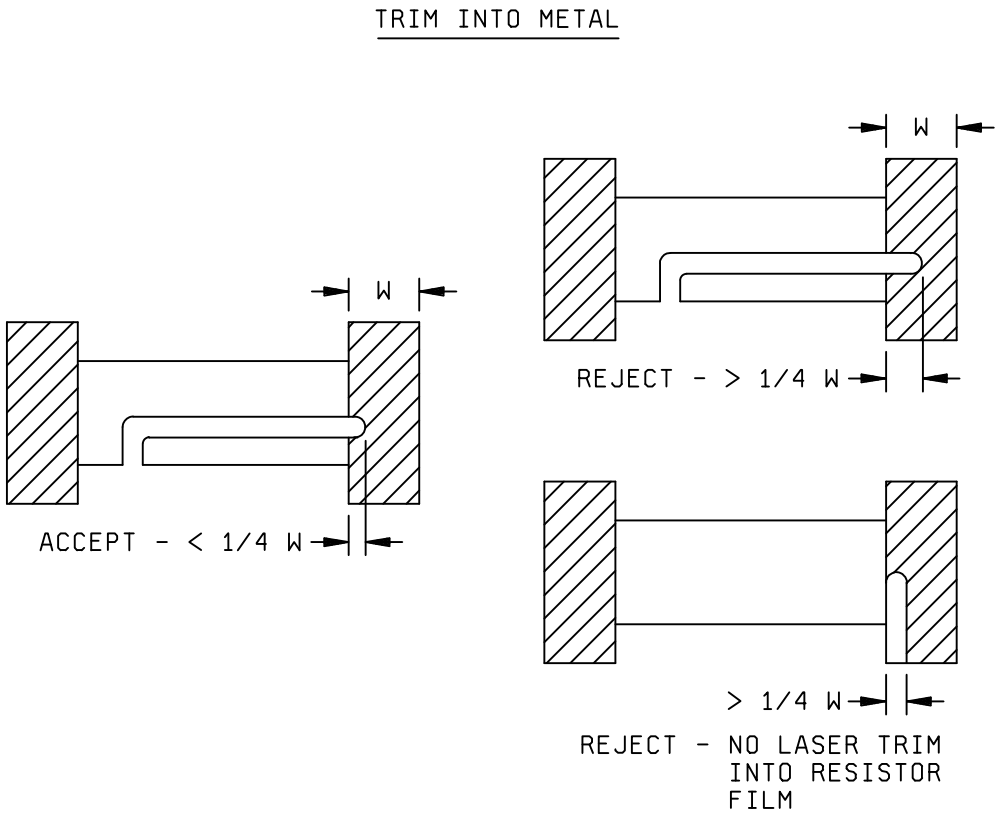

FIGURE 2010-32. Block resistor criteria.

g. Pits into the silicon dioxide in the kerf which do not exhibit a line of separation between the pit and the resistor material.

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Condition A Class level S	Condition B Class level B

3.2 Low power inspection. Internal visual examination as required in 3.2.1 through 3.2.3 shall be conducted on each microcircuit at low magnification range of 30X to 60X. In addition, the applicable criteria contained in 3.2.4 shall be applicable where beam lead assembly technology is used and 3.2.5 shall be inspected at both high and low power as indicated, high power magnification shall be same as 3.1, subject to conditions in 3b.

3.2.1 Lower power wire bond inspection. This inspection and criteria shall be required inspection for the bond type (s) and location(s) to which they are applicable when viewed from above (see figure 2010-33).

NOTE: The criteria applicable for bonds (called "wedgebonds" or "bonds") in this test method refers to the fully or partially deformed area including the tool impression shown as "L and W" in figure. The criteria applicable for "bond tails" (or "tails") in this test method refers to resulting length of bonding wire extending beyond the bond shown as "T" in figure 2010-33. Tail is not part of bond.

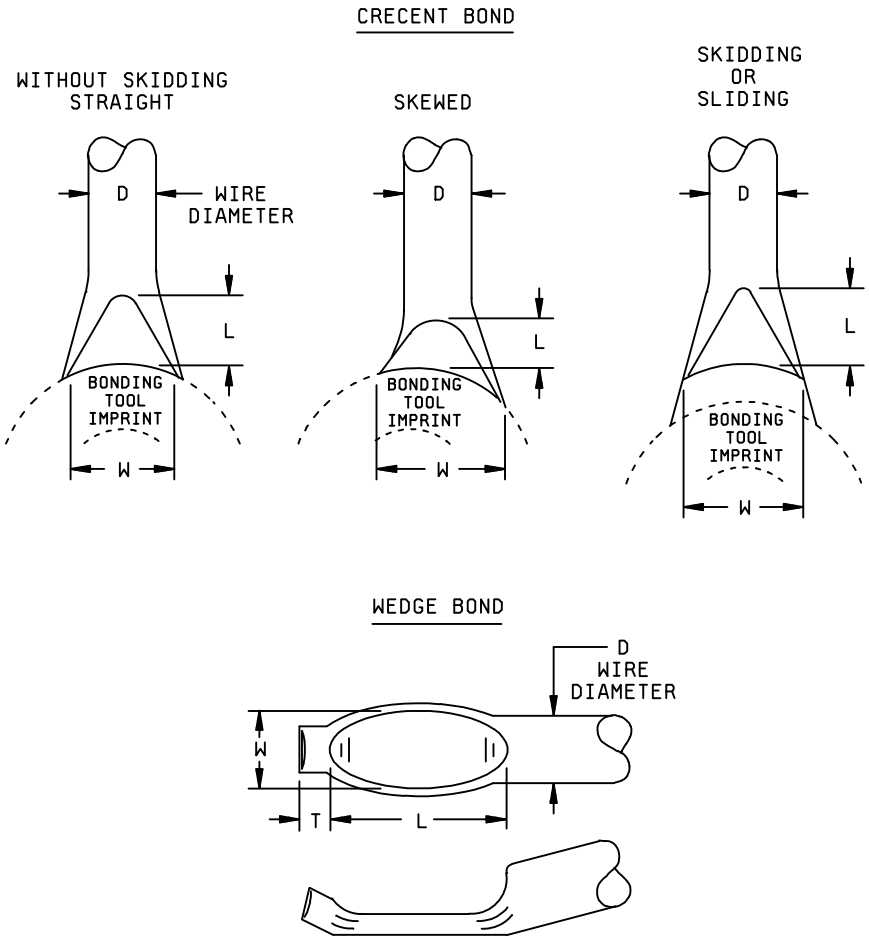

FIGURE 2010-33. Bond dimensions.

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Condition A Class level S	Condition B Class level B

3.2.1.1 Gold ball bonds. No devices shall be acceptable that exhibits:

a. Gold ball bonds on the die or package post wherein the ball bond diameter is less than 2.0 times or greater than 5.0 times the wire diameter.

b. Gold ball bonds where the wire exit is not completely within the periphery of the ball.

c. Gold ball bonds where the wire center exit is not within the boundaries of the unglassivated bonding pad area.

3.2.1.2 Wedge bonds. No device shall be acceptable that exhibits:

a. Ultrasonic wedge bonds on the die or package post that are less than 1.2 times or more than 3.0 times the wire diameter in width, or less than 1.5 times or more than 6.0 times the wire diameter in length.

b. Thermosonic wedge bonds on the die or package post that are less than 1.5 times or more than 3.0 times the wire diameter in width or are less than 1.5 times or more than 6.0 times the wire diameter in length.

c. Bond width less than 1.0 times the wire diameter for aluminum wires 2.0 mils or greater in diameter.

d. Wedge bonds where the tool impression does not cover the entire width of the wire.

3.2.1.3 Tailless bonds (crescent, terminating capillary bond). No device shall be acceptable that exhibits:

a. Tailless bonds on the die or package post that are less than 1.2 times or more than 5.0 times the wire diameter in width, or are less than 0.5 times or more than 3.0 times the wire diameter in length.

b. Tailless bonds where tool impression does not cover the entire width of the wire.

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Condition A Class level S	Condition B Class level B

3.2.1.4 General (gold ball, wedge, and tailless). As viewed from above, no device shall be acceptable the exhibits (see figure 2010-16):

a. Bonds on the die where less than 75 percent of the bond is within the unglassivated bonding pad area.	a. Bonds on the die where less than 50 percent of the bond is within the unglassivated bonding pad area.

b. Bond tails that do not exhibit a line of separation between the tail and unglassivated metallization, another wire, wire bond, or wire bond tail, excluding common conductors and pads.

c. Bond tails extending over glassivated metallization where the glass exhibits evidence of crazing or cracking that extends under the tail, excluding common conductors.

d. Wire bond tails: Tails that exceed 2 wire diameters in length on die or on post.

e. Bonds that are not completely within the boundaries of the package post. For glass sealed packages, bonds not within 20 mils of the end of post.

f. Bonds (excluding bond tails) placed so that the horizontal distance between the bond and glassivated or unglassivated noncommon metallization, scribe lines, another bonding wire or bond is less than .25 mils.	f. Bonds (excluding bond tails) placed so that the horizontal distance between the bond and glassivated or unglassivated noncommon metallization, scribe lines, another bonding wire or bond does not exhibit a visible line of separation.

NOTE: When by design, there are multiple bonds on a common bonding pad or post they may not reduce the width of an adjacent bond by more than 25 percent.

NOTE: For SOS devices, exclude the insulator scribe lines.

g. Bonds (excluding tails) placed such that less than 2.0 mils of bond periphery (on glassivated or unglassivated areas) is exposed to an undisturbed die metallization connecting path to/from the entering/exiting metallization stripe (see figure 2010-34).

NOTE 1: When bond tails prevent visibility of the connecting path and the metallization immediately adjacent to the bond tail is disturbed, the device shall be unacceptable.

NOTE 2: When a fillet area exists, it is to be considered as part of the entering/exiting metallization stripe.

NOTE 3: This criteria is in addition to the bond placement criteria in 3.2.1.4a.

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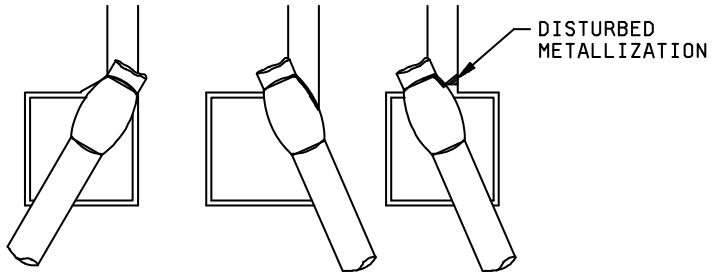
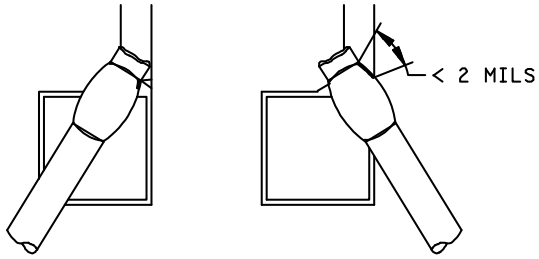
Condition A
Class level S

Condition B
Class level B

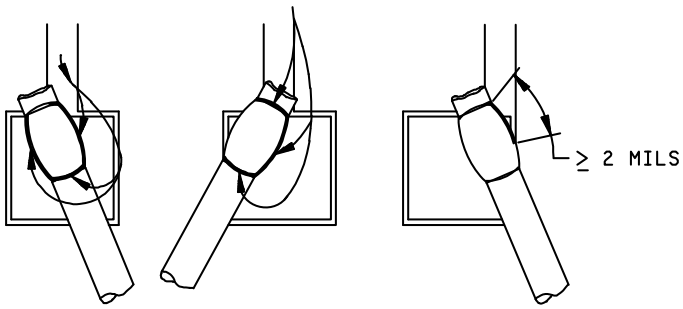
Reject: Bond (excluding tails) placed, such that less than 2.0 mils of bond periphery (on glassivated or unglassivated areas) is exposed by an undisturbed die metallization connecting path to/from the entering/exiting metallization stripe.



Reject: When bond tails prevent visibility of the connecting path to the bond periphery and the metallization immediately adjacent to the bond tail is disturbed.



Accept: Bonds (excluding tails) placed, such that there is 2.0 mils or greater of bond periphery (on glassivated or unglassivated areas) exposed by an undisturbed die metallization connecting path to/from the entering/exiting metallization stripe.



Arrows demonstrate the connecting path to the bond periphery.

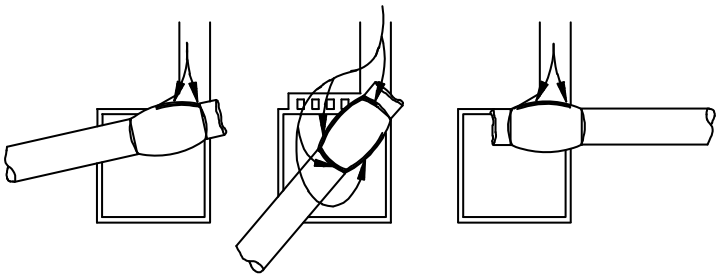


FIGURE 2010-34. Bonds at entering/exiting metallization stripe.

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Condition A Class level S	Condition B Class level B

h. Bonds where more than 25 percent of the bond is located on die mounting material.

i. Any evidence of repair of conductors by bridging with additional material.

j. Bonds on foreign material.

k. Intermetallic formation extending radially more than 0.1 mil completely around the periphery of that portion of the gold bond located on metal.

3.2.1.5 Rebonding of monolithic devices. Rebonding of monolithic microcircuits, may be done with the following limitations. No device shall be acceptable that exhibits:

a. Rebond over exposed passivation or over metal which shows evidence of peeling. More than one rebond attempt at any design bond location. Rebonds that touch an area of exposed oxide caused by lifted metal.

b. A bond on top of, or partially on top of, another bond, bond wire tail, or residual segment of wire.

b. Bond along side or partially on top of another bond, bond wire tail or residual segment of wire, when the overlap width is greater than 25 percent.

c. Rebond attempts that exceed 10 percent of the total number of bonds in the microcircuit. (e.g., for a 28 lead wire bonded package there are 56 bonds. A bond of one end of a wire shall count as a single attempt. A replacement of a wire bonded at both ends, counts as two rebond attempts.)

NOTE: For class level B only. Bond-offs required toclear the bonder after an unsuccessful first bond attempt are not considered as rebonds provided they can be identified as bond-offs.

d. Missing or extra wires.

3.2.1.6 Flip chip solder bump die. No solder bumped die shall be acceptable that exhibit any of the following characteristics (see figure 2010-34A):

a. missing solder ball from original design position.
b. Solder ball 20% smaller, or larger than design size (nominal).
c. Solder balls bridging.
d. Any attached or embedded foreign material bridging balls, or redistribution metalization.
e. Misaligned solder ball which exposes the UBM on the contact via.
f. Voids in redistribution metalization greater than 50% of the design width.
g. Any redistribution metalization bridging.
h. Any residual unetched UBM bridging balls or redistribution metalization.
i. Mechanical damage to the ball which reduces the original height or diameter more than 20%.
j. Lifting, or peeling or the RDL or dielectric material.

Note: Minor damage to the solder ball and bump misalignment can be reworked by performing a re-flow/refresh of the solder balls.

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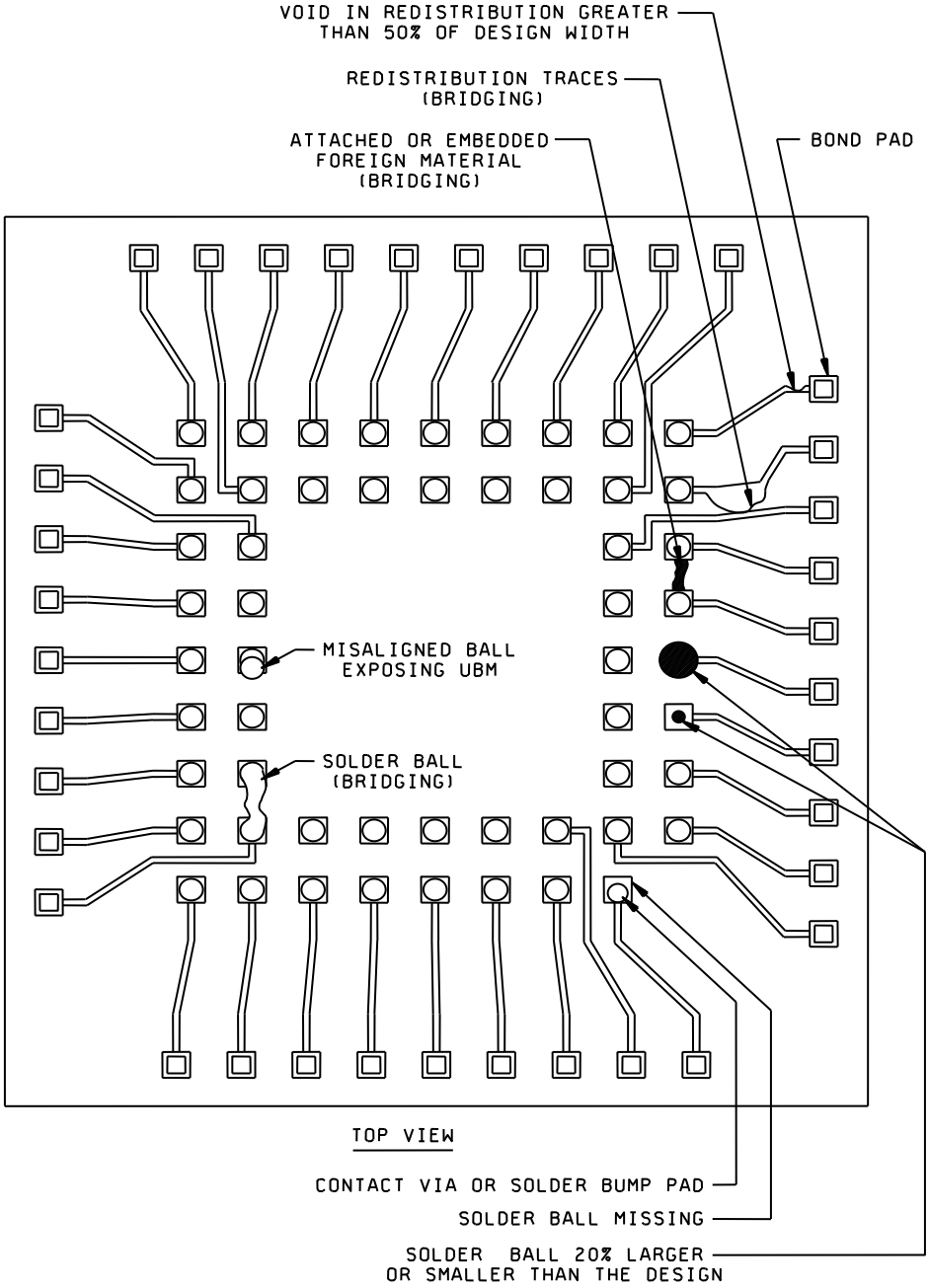

Figure 2010.34A – FLIP CHIP VISUAL INSPECTION DIAGRAM

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Condition A Class level S	Condition B Class level B

3.2.2 Internal wires. During inspection for the requirements of 3.2.2, each device shall be viewed at any angle necessary to determine full compliance to this specification, without damaging the device. No device shall be acceptable that exhibits:

a. Any wire with a separation of less than two wire diameters to unglassivated operating metal,other bonds, another wire (common wires excluded) other package post, unglassivated die area (except for wires or pads which are at the die or substrate potential), or any portion of the package including the plane of the lid to be attached.	a. Any wire with a separation of less than one wire diameter to unglassivated operating metal, other bonds, another wire (common wires excluded), other package post, unglassivated die area (except for wires or pads which are at the die or substrate potential), or any conductive portion of the package or the plane of the lid to be attached.
NOTE: For condition A only. Within a 5.0 mil radial distance from the perimeter of the bond on the die the separation shall be 1.0 mil minimum.	NOTE: For condition B only. Within a10.0 mil radial distance from the perimeter of the bond on the die a line of separation must be visible.

NOTE: For SOS devices, exclude the unglassivated insulator areas.

b. Nicks, bends, cuts, crimps, scoring, or neckdown in any wire that reduces the wire diameter by more than 25 percent.

c. Tearing at the junction of the wire and bond.

d. Any wire making a straight line run from a die bonding pad to a package post that has no arc.

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Condition A Class level S	Condition B Class level B
e. Wire(s) crossing wire(s) when viewed from, above (excluding common conductors) except in multitiered packages, where the crossing occurs within the boundary of the lower wire bond tier(s) being crossed or packages with down bond(s). In these situations,the wires that cross are acceptable if they maintain a minimum clearance of two wire diameters (see figure 2010-35). NOTE: No bond wire shall cross more than one other bond wire and there shall be no more than 4 crossovers or crossovers involving more than 10 percent of the total number of wires, whichever is greater for any single package cavity.	e. Wire(s) crossing wire(s) when viewed from above, (excluding common conductors) except that wires crossing wires bonded to package posts that are at difference heights, or wires bonded into the package cavity that cross are acceptable if they maintain a minimum clearance of two wire diameters (e.g., multitiered packages or packages with down bond chips).

f. Wire(s) not in accordance with bonding diagram.

3.2.3 Die mounting.

3.2.3.1 Die mounting eutectic. No device shall be acceptable that exhibits:

a. Die mounting material buildup that extends onto the top surface or extends vertically above the top surface of the die.

b. Die mounting material (eutectic wetting) not visible around at least two complete sides or 75 percent of the die perimeter, except for transparent die.

c. Transparent die with less than 50 percent of the area bonded.

d. Flaking of the die mounting material.

e. Balling or buildup of the die mounting material that does not exhibit a minimum of 50 percent peripheral fillet when viewed from above or the accumulation of die mounting material is such that the height of the accumulation is greater than the longest base dimension or the accumulation necks down at any point (see figure 2010-36).

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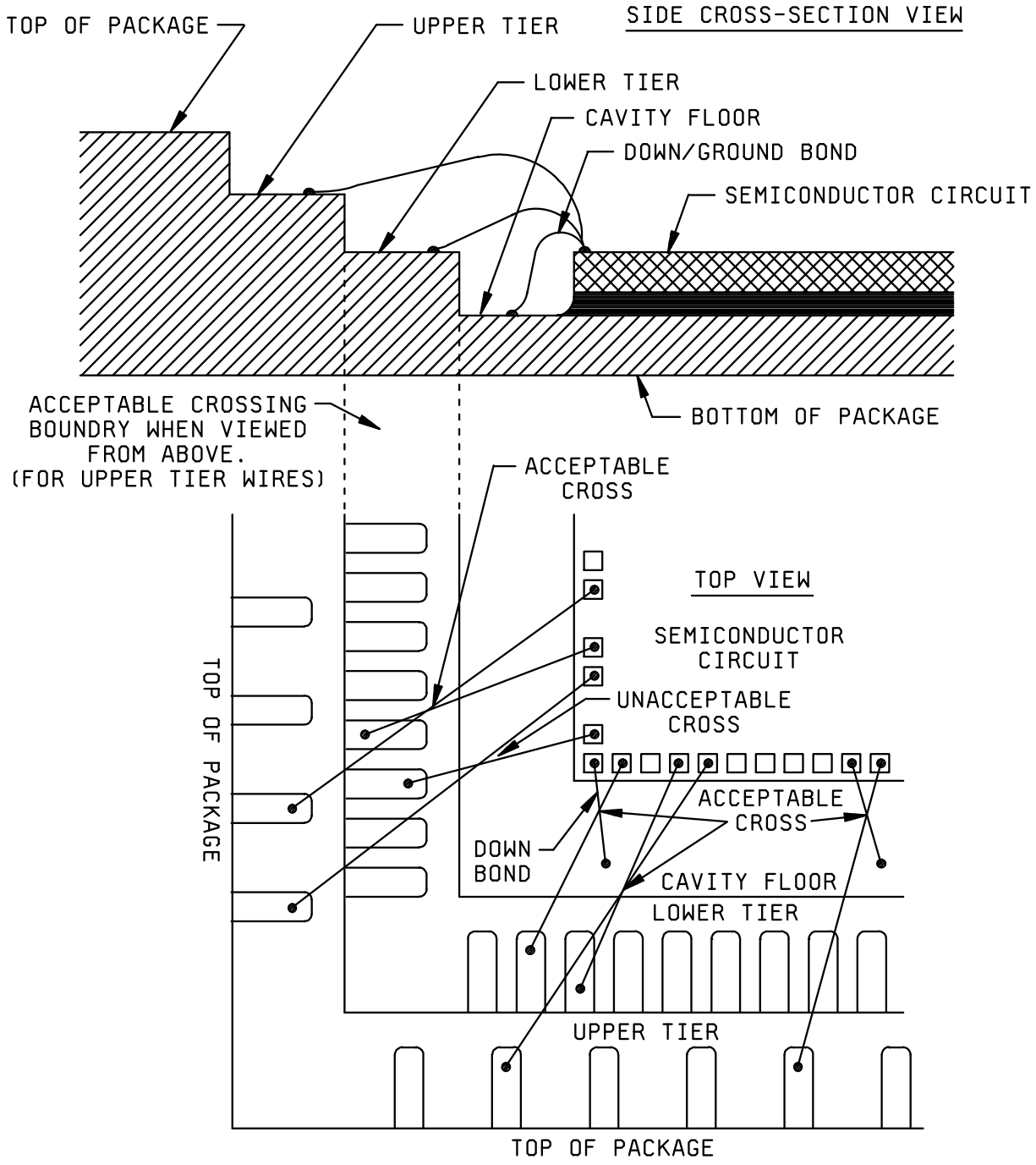

FIGURE 2010-35. Class level S criteria for wire(s) crossing wire(s).

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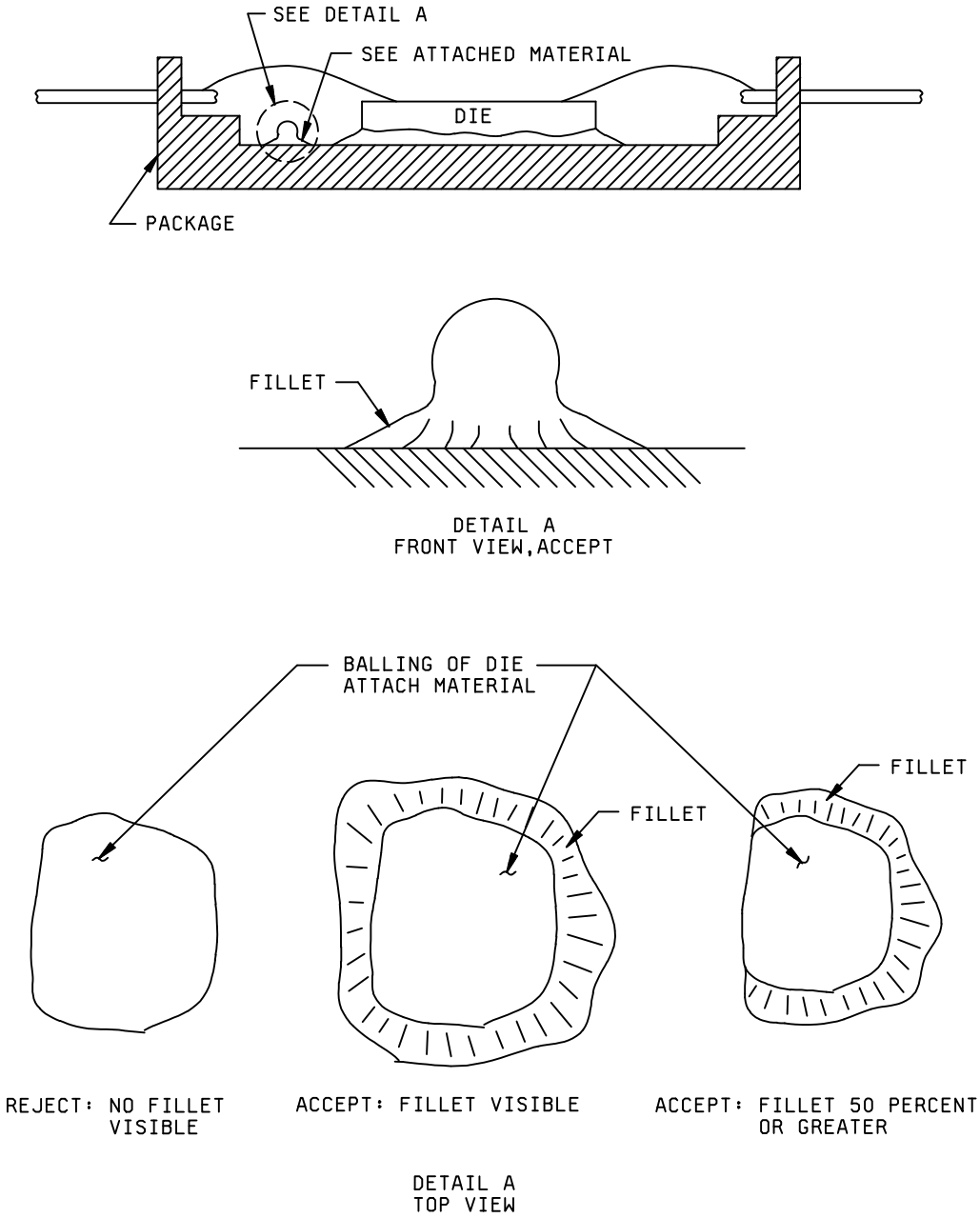

FIGURE 2010-36. Balling of die attach material.

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Condition A Class level S	Condition B Class level B

3.2.3.2 Die mounting noneutectic. No device shall be acceptable that exhibits:

a. Adhesive material immediately adjacent to the die that extends onto or vertically above the top surface of the die.

b. Adhesive fillet not visible along 75 percent of each side of the die.

c. Any flaking, peeling, or lifting of the adhesive material.

d. Separation, cracks, or fissures greater than or equal to 2 mils in width in the adhesive at the cavity wall or cavity floor.

e. Crazing in the adhesive.

f. Adhesive that bridges package posts or is on the post bond area.

g. Any adhesive material that is connected to the fillet or conductive cavity (e.g. metal package base or metallized floor of ceramic package), and extends up the cavity wall to within 1.0 mil of the package post.

h. Transparent die with less than 50 percent of the area bonded.

3.2.3.3 Die orientation. No device shall be acceptable that exhibits:

a. Die not located or oriented in accordance with the applicable assembly drawing.

b. Die that appears to be obviously tilted (i.e., more than 10 degrees) with respect to the package cavity.

3.2.4 Beam lead construction.

3.2.4.1 Bonds. This inspection criteria shall apply to the completed bond area made, using either direct tool contact or a compliant intermediate layer. No device shall be acceptable that exhibits:

a. Bonds where the tool impression does not completely cross the entire beam width.

b. Bonds on thin film substrate metal where the tool impression increases the beam lead width less than 15 percent (10 percent for compliant bonds) or greater than 75 percent of the undeformed beam width.

c. Bonds where the tool impression length is less than 1.0 mil (see figure 2010-37).

d. Bonding tool impression less than 1.0 mil from the die edge (see figure 2010-37).

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Condition A Class level S	Condition B Class level B

e. Effective bonded area less than 50 percent of that which would be possible for an exactly aligned beam (see figure 2010-37).

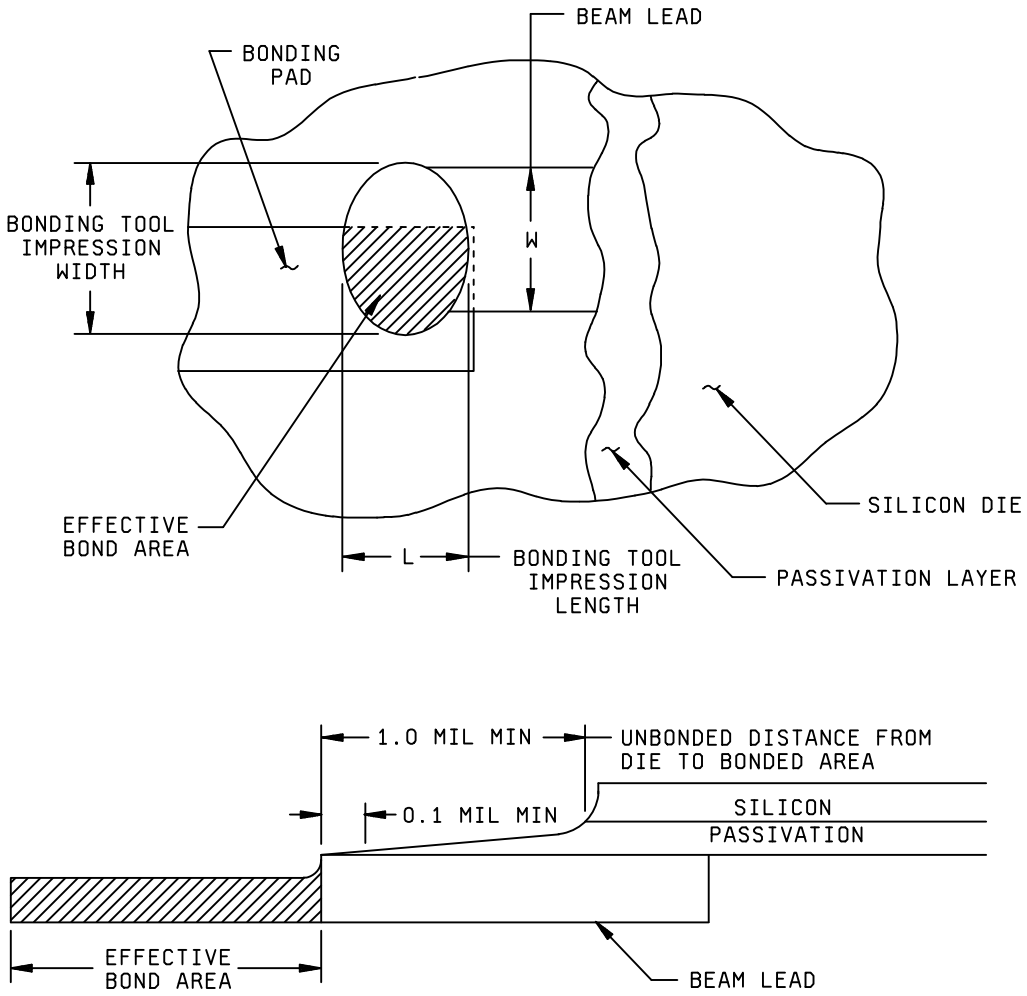

FIGURE 2010-37. Beam lead bond area and location.

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Condition A Class level S	Condition B Class level B

f. Cracks or tears in the effective bonded area of the beam greater than 50 percent of the original beam width.

g. Bonds placed so that the separation between bonds and between bonds and operating metallization not connected to them is less than 0.1 mil.

h. Bonds lifting or peeling.

3.2.4.2 Beam leads. No device shall be acceptable that exhibits the following:

a. Voids, nicks, depressions, or scratches that leave less than 50 percent of the beam width undisturbed.

b. Beam separation from the die.

c. Missing or partially fabricated beam leads unless by design.

d. Beam leads that are not bonded.

e. Bonded area closer than 0.1 mil to the edge of the passivation layer.

f. Less than 0.1 mil passivation layer between the die and the beam visible at both edges of the beam (see figure 2010-37 and 2010-38).

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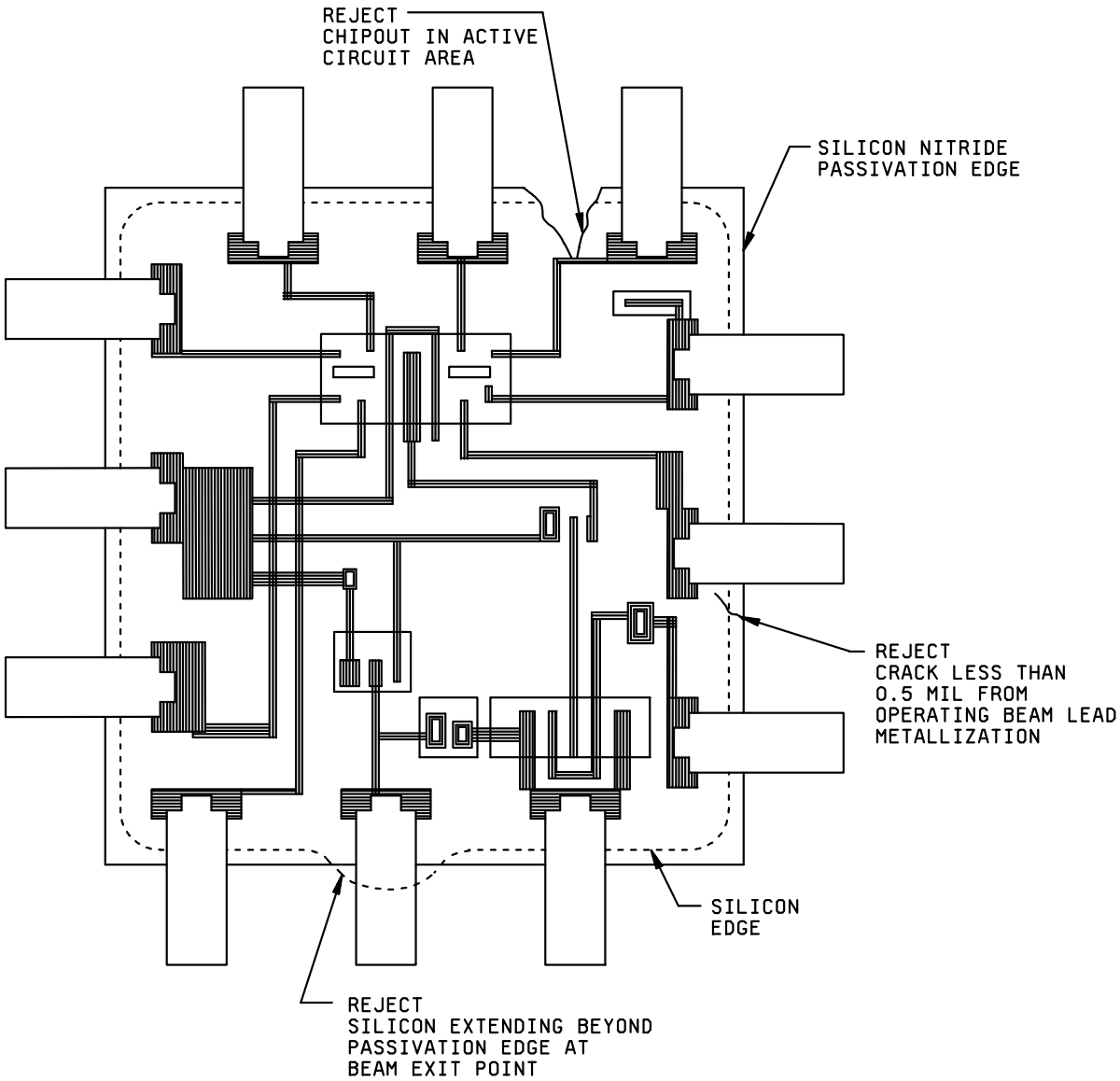

FIGURE 2010-38. Beam lead die faults.

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Condition A Class level S	Condition B Class level B

3.2.5 Foreign material. Die inspections shall be at high magnification. Package and lid inspections shall be at low magnification. Die criteria may be examined at high magnification prior to die mounting provided they are re-examined at low magnification during preseal inspection. No device shall be acceptable that exhibits:

NOTE: Foreign material may be removed, if possible, by subjecting the device to a nominal gas blow (less than 25 psig). After this gas blow off at inspection, all wire bonded devices shall be inspected/reinspected for possible wire damage. Use of a higher psig value is permitted provided that the manufacturer has characterized the process and has data to assure that no damage is done to the wire bonds. This data shall be available upon request to the preparing or acquiring activities.

a. Foreign particle(s) on the surface of the die that is (are) large enough to bridge the narrowest spacing between unglassivated operating material (e.g., metallization, bare semiconductor material, mounting material, bonding wire, etc.).

b. Foreign particle(s) other than on the surface of the die within the package or on the lid or cap that is (are) large enough to bridge the narrowest spacing between unglassivated operating materials and are not the following: Semiconductor material, glass splatter, gold imperfections in the die attach area, gold eutectic material or package ceramic material.

NOTE: As an alternative to 100 percent visual inspection of lids or caps, the lids or caps may be subjected to a suitable cleaning process and quality verification, approved by the qualifying activity. The lids or caps shall subsequently be held in a controlled environment until capping or preparation for seal.

c. Foreign material attached to or embedded in the die surface that appears to bridge the active circuit elements including metallization unless verified as only attached but not embedded by high power dark field illumination.

d. Liquid droplets, chemical stains, ink, or photoresist on the die surface that appear to bridge any combination of unglassivated metallization or bare semiconductor material areas.

e. A particle of gold eutectic material, package ceramic material or semiconductor material, not attached to the die, large enough to bridge the narrowest spacing between unglassivated operating materials, that does not exhibit a minimum of 50 percent cumulative peripheral fillet or whose height is greater than the longest base dimension.

NOTE 1: This criteria shall not be cause for rejection when the assembly process contains a gas blow (less than 60 psig) after die attach and again (less than 25 psig) after wire bond provided rejectable materials (not attached and large enough to bridge) have been removed from the cavity.

NOTE 2: Gold imperfections in the die attach area that do not interfere with proper die attachment, sealing glass splatter (provided it does not suggest inadequately controlled process and does not interfere with the die attach area) or internal glass run out from frit seal (provided it is confined to package walls and does not interfere with the die attach area) are not rejectable.

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Condition A Class level S	Condition B Class level B

3.2.5.1 Foreign material, die coated devices. This inspection and criteria shall be required on all devices that receive a die coat during the assembly process. This inspection will be done after die coat cure. No device shall be acceptable that exhibits:

a. Unattached foreign particles on the surface of the die coat or within the package that is (are) large enough to bridge the narrowest spacing between unglassivated operating material (e.g., metallization, bare semiconductor material, mounting material, bonding wire, etc.). Note: Semiconductor particles shall be considered as foreign material.

b. Partially embedded foreign material with an "unembedded portion" that is large enough to bridge the narrowest spacing between unglassivated operating material (e.g., metallization, bare semiconductor material, mounting material, bonding wire, etc.).

c. Foreign material attached to or embedded in the die coat that appears to bridge unglassivated operating material when viewed from above (e.g., bare semiconductor material, bond pads, bonding wire, mounting material, etc.).

d. Embedded foreign particles that penetrate the entire thickness of the die coating.

3.2.5.1.1 Die coating material. No device shall be accepted that exhibits:

a. Surface scratches that penetrate the die coating and expose underlying glassivated metal.

b. Die coating that is lifted or is peeling from the semiconductor surface.

3.2.6 GaAs backside metallization. GaAs inspection shall be performed with low magnification prior to die mounting. (Verification at high magnification is permitted.) With the approval of the acquiring activity, the manufacturer may substitute a sample inspection plan at the wafer level for 100 percent inspection in dice form. The sample inspection plan shall be documented in the manufacturer's baseline documentation and shall be performed to the requirements of test method 5013. No devices shall be acceptable that exhibit the following.

a. Evidence of metal corrosion, lifting, peeling, blistering.

b. Voids or scratches that expose underlying metal or substrate whose cumulative areas are more than 25 percent of the cell area or device area.

NOTE: Absence of gold in the die separation area (saw street) of devices with electroplated backside metallization is not a cause for rejection. Small voids at edges due to die separation are acceptable if they comprise less than 10 percent of the backside area.

c. Any voids or scratches in the substrate via metallization that effects more than 25 percent of the metallization or cause unintended isolation of the metallization path.

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4. SUMMARY. The following details shall be specified in the applicable acquisition document.

   a. Test condition (see 3).

   b. Where applicable, any conflicts with approved circuit design topology or construction.

   c. Where applicable, gauges, drawings, and photographs that are to be used as standards for operator comparison (see 2).

   d. Where applicable, specific magnification (see 3).

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METHOD 2011.10

BOND STRENGTH (DESTRUCTIVE BOND PULL TEST)

1. PURPOSE. The purpose of this test is to measure bond strengths, evaluate bond strength distributions, or determine compliance with specified bond strength requirements of the applicable acquisition document. This test may be applied to the wire-to-die bond, wire-to-substrate bond, or the wire-to-package lead bond inside the package of wire-connected microelectronic devices bonded by soldering, thermocompression, ultrasonic, or related techniques. It may also be applied to bonds external to the device such as those from device terminals-to-substrate or wiring board or to internal bonds between die and substrate in non-wire-bonded device configurations such as beam lead or flip chip devices.

2. APPARATUS. The apparatus for this test shall consist of suitable equipment for applying the specified stress to the bond, lead wire or terminal as required in the specified test condition. A calibrated measurement and indication of the applied stress in grams force (gf) shall be provided by equipment capable of measuring stresses up to twice the specified minimum limit value, with an accuracy of ±5 percent or ±0.3 gf, whichever is the greater tolerance.

3. PROCEDURE. The test shall be conducted using the test condition specified in the applicable acquisition document consistent with the particular device construction. All bond pulls shall be counted and the specified sampling, acceptance, and added sample provisions shall be observed, as applicable. Unless otherwise specified, for conditions A, C, and D, the sample size number specified for the bond strength test shall determine the minimum sample size in terms of the minimum number of bond pulls to be accomplished rather than the number of complete devices in the sample, except that the required number of bond pulls shall be randomly selected from a minimum of 4 devices. Bond pulls in accordance with test conditions D, F, G, and H, while involving two or more bonds shall count as a single pull for bond strength and sample size number purposes. Unless otherwise specified, for conditions F, G, and H the sample size number specified shall determine the number of die to be tested (not bonds). For hybrid or multichip devices (all conditions), a minimum of 4 die or use all die if four are not available on a minimum of 2 completed devices shall be used. Where there is any adhesive, encapsulant or other material under, on or surrounding the die such as to increase the apparent bond strength, the bond strength test shall be performed prior to application. The stress required to achieve bond failure shall be observed and the physical location of the point of failure shall be recorded as being in one of the listed categories (see 3.2.1).

When flip chip or beam-lead chips are bonded to substrates other than those in completed devices, the following conditions shall apply:

a. The sample of chips for this test shall be taken at random from the same chip population as that used in the completed devices that they are intended to represent.

b. The chips for this test shall be bonded on the same bonding apparatus as the completed devices, during the time period within which the completed devices are bonded.

c. The test chip substrates shall be processed, metallized, and handled identically with the completed device substrates, during the same time period within which the completed device substrates are processed.

3.1 Test conditions:

3.1.1 Test condition A - Bond peel. This test is normally employed for bonds external to the device package. The lead or terminal and the device package shall be gripped or clamped in such a manner that a peeling stress is exerted with the specified angle between the lead or terminal and the board or substrate. Unless otherwise specified, an angle of 90 degrees shall be used. When a failure occurs, the force causing the failure and the failure category shall be recorded.

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3.1.2 Test condition C - Wire pull (single bond). This test is normally employed for internal bonds at the die or substrate and the lead frame of microelectronic devices. The wire connecting the die or substrate shall be cut so as to provide two ends accessible for pull test. In the case of short wire runs, it may be necessary to cut the wire close to one termination in order to allow pull test at the opposite termination. The wire shall be gripped in a suitable device and simple pulling action applied to the wire or to the device (with the wire clamped) in such a manner that the force is applied approximately normal to the surface of the die or substrate. When a failure occurs, the force causing the failure and the failure category shall be recorded.

3.1.3 Test condition D - Wire pull (double bond). This procedure is identical to that of test condition C, except that the pull is applied by inserting a hook under the lead wire (attached to die, substrate or header or both ends) with the device clamped and hook contacting the wire between midspan and loop apex, without causing adverse wire deformation (for forward wedge and ball bonding, this would be between midspan and the die edge: for reverse bonding, this would be between midspan and the package edge) and the pulling force is applied in a perpendicular direction to the die or substrate surface. See Figure 2011-1. When a failure occurs, the force causing the failure and the failure category shall be recorded. The minimum bond strength shall be taken from table I. Figure 2011-2 may be used for wire diameters not specified in table I. For wire diameter or equivalent cross section >0.005 inch, where a hook will not fit under the wire, a suitable clamp can be used in lieu of a hook.

3.1.4 Test condition F - Bond shear (flip chip). This test is normally employed for internal bonds between a semiconductor die and a substrate to which it is attached in a face-bonded configuration. It may also be used to test the bonds between a substrate and an intermediate carrier or secondary substrate to which the die is mounted. A suitable tool or wedge shall be brought in contact with the die (or carrier) at a point just above the primary substrate and a force applied perpendicular to one edge of the die (or carrier) and parallel to the primary substrate, to cause bond failure by shear. When a failure occurs, the force at the time of failure, and the failure category shall be recorded.

3.1.5 Test condition G – Push-off test (beam lead). This test is normally employed for process control and is used on a sample of semiconductor die bonded to a specially prepared substrate. Therefore, it cannot be used for random sampling of production or inspection lots. A metallized substrate containing a hole shall be employed. The hole appropriately centered, shall be sufficiently large to provide clearance for a push tool, but not large enough to interfere with the bonding areas. The push tool shall be sufficiently large to minimize device cracking during testing, but not large enough to contact the beam leads in the anchor bond area. Proceed with push-off tests as follows: The substrate shall be rigidly held and the push tool inserted through the hole. The contact of the push tool to the silicon device shall be made without appreciable impact (less than 0.01 inch/minute (0.254 mm/minute) and forced against the underside of the bonded device at a constant rate. When failure occurs, the force at the time of failure, and the failure category shall be recorded.

3.1.6 Test condition H – Pull-off test (beam lead). This test is normally employed on a sample basis on beam lead devices which have been bonded down on a ceramic or other suitable substrate. The calibrated pull-off apparatus (see 2) shall include a pull-off rod (for instance, a current loop of nichrome or Kovar wire) to make connection with a hard setting adhesive material (for instance, heat sensitive polyvinyl acetate resin glue) on the back (top side) of the beam lead die. The substrate shall be rigidly installed in the pull-off fixture and the pull-off rod shall make firm mechanical connection to the adhesive material. The device shall be pulled within 5 degrees of the normal to at least the calculated force (see 3.2), or until the die is at 2.54 mm (0.10 inch) above the substrate. When a failure occurs, the force at the time of failure, the calculated force limit, and the failure category shall be recorded.

3.1.7 Wire Ball Bond Shear. Procedure in accordance with JEDEC JESD22-B116 Wire Bond Shear Test Method.

3.2 Failure criteria. Any bond pull which results in separation under an applied stress less than that indicated in table I as the required minimum bond strength for the indicated test condition, composition, and construction shall constitute a failure.

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3.2.1 Failure category. Failure categories are as follows: When specified, the stress required to achieve separation and the category of separation or failure shall be recorded.

a. For internal wire bonds:

(a-0) Wire broken or missing prior to test.

(a-1) Wire break at neckdown point (reduction of cross section due to bonding process).

(a-2) Wire break at point other than neckdown.

(a-3) Failure in bond (interface between wire and metallization) at die.

(a-4) Failure in bond (interface between wire and metallization) at substrate, package post, or other than die.

(a-5) Lifted metallization from die.

(a-6) Lifted metallization from substrate or package post.

(a-7) Fracture of die.

(a-8) Fracture of substrate.

(a-9) Break in wire at neckdown on the substrate or package post.

b. For external bonds connecting device to wiring board or substrate:

(b-1) Lead or terminal break at deformation point (weld affected region).

(b-2) Lead or terminal break at point not affected by bonding process.

(b-3) Failure in bond interface (in solder or at point of weld interface between lead or terminal and the board or substrate conductor to which the bond was made).

(b-4) Conductor lifted from board or substrate.

(b-5) Fracture within board or substrate.

c. For flip-chip configurations:

(c-1) Failure in the bond material or pedestal, if applicable.

(c-2) Fracture of die (or carrier) or substrate (removal of portion of die or substrate immediately under the bond).

(c-3) Lifted metallization (separation of metallization or bonding pedestal from die (or carrier) or substrate.

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d. For beam lead devices:

(d-1) Silicon broken.

(d-2) Beam lifting on silicon.

(d-3) Beam broken at bond.

(d-4) Beam broken at edge of silicon.

(d-5) Beam broken between bond and edge of silicon.

(d-6) Bond lifted.

(d-7) Lifted metallization (separation of metallization) from die, separation of bonding pad.

(d-8) Lifted metallization.

NOTE: RF/microwave hybrids that require extremely flat loops which may cause erroneous wire pull data may use the following formula to determine the proper wire pull value.

$V_1 = V_2 \sin \Theta$

Where: V_1 = New value to pull test.
V_2 = Table I value for size wire tested.
Θ = Greatest calculated wire loop angle (Figure 2011-3).

Also, RF/microwave hybrids that contain wires that cannot be accessed with a pull hook must be duplicated on a test coupon in such a way to allow hook access for purposes of pull testing. These wires are to be bonded at the same time the production hybrids are bonded using the same setup, operator, and schedule. The test coupon wires are to be pull tested in lieu of the tuning or inaccessible wires on the production hybrid. Failures on the test coupon shall be considered as failures to production units and appropriate action is to be taken in accordance with the applicable specification (Figure 2011-4).

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TABLE I. Minimum bond strength.

Test condition	Wire composition and diameter 1/	Construction 2/	Minimum bond strength (grams force)	
			Pre seal	Post seal and any other processing and screening when applicable
A	---	---	Given in applicable document	Given in applicable document
C or D	AL 0.0007 in AU 0.0007 in	Wire	1.5 2.0	1.0 1.5
C or D	AL 0.0010 in AU 0.0010 in	Wire	2.5 3.0	1.5 2.5
C or D	AL 0.00125 in AU 0.00125 in	Wire	Same bond strength limits as the 0.0013 in wire	
C or D	AL 0.0013 in AU 0.0013 in	Wire	3.0 4.0	2.0 3.0
C or D	AL 0.0015 in AU 0.0015 in	Wire	4.0 5.0	2.5 4.0
C or D	AL 0.0030 in AU 0.0030 in	Wire	12.0 15.0	8.0 12.0
F	Any	Flip-clip	5 grams-force x number of bonds (bumps)	
G or H	Any	Beam lead	30 grams force in accordance with linear millimeter of nominal undeformed (before bonding) beam width. 3/	

1/ For wire diameters not specified, use the curve of figure 2011-2 to determine the bond pull limit.
2/ For ribbon wire, use the equivalent round wire diameter which gives the same Cross-sectional area as the ribbon wire being tested.
3/ For condition G or H, the bond strength shall be determined by dividing the breaking force by the total of the nominal beam widths before bonding.

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4. SUMMARY. The following details shall be specified in the applicable acquisition document:

a. Test condition letter (see 3).

b. Minimum bond strength if other than specified in 3.2 or details of required strength distributions if applicable.

c. Sample size number and accept number or number and selection of bond pulls to be tested on each device, and number of devices, if other than 4.

d. For test condition A, angle of bond peel if other than 90°, and bond strength limit (see 3.2).

e. Requirement for reporting of separation forces and failure categories, when applicable (see 3.2.1).

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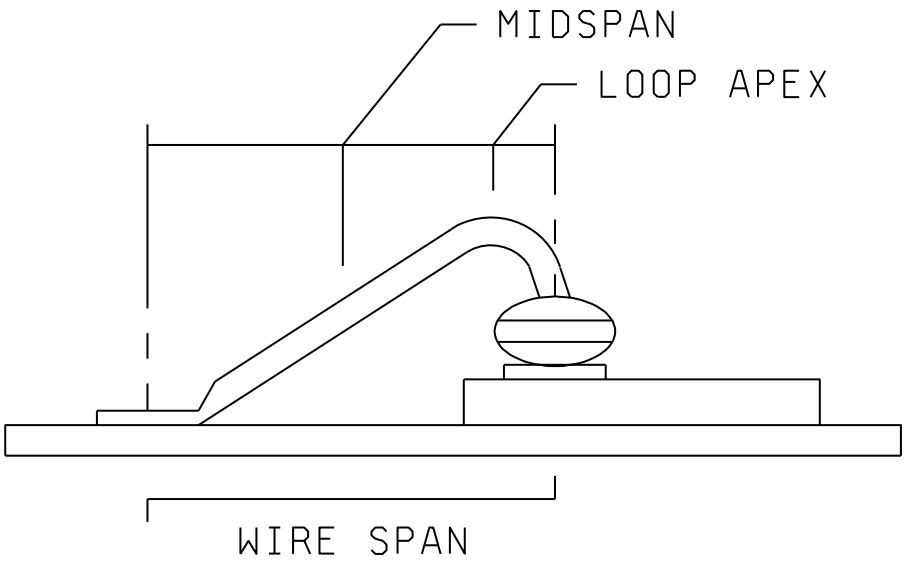

Figure 2011-1. Bond pull hook placement location.

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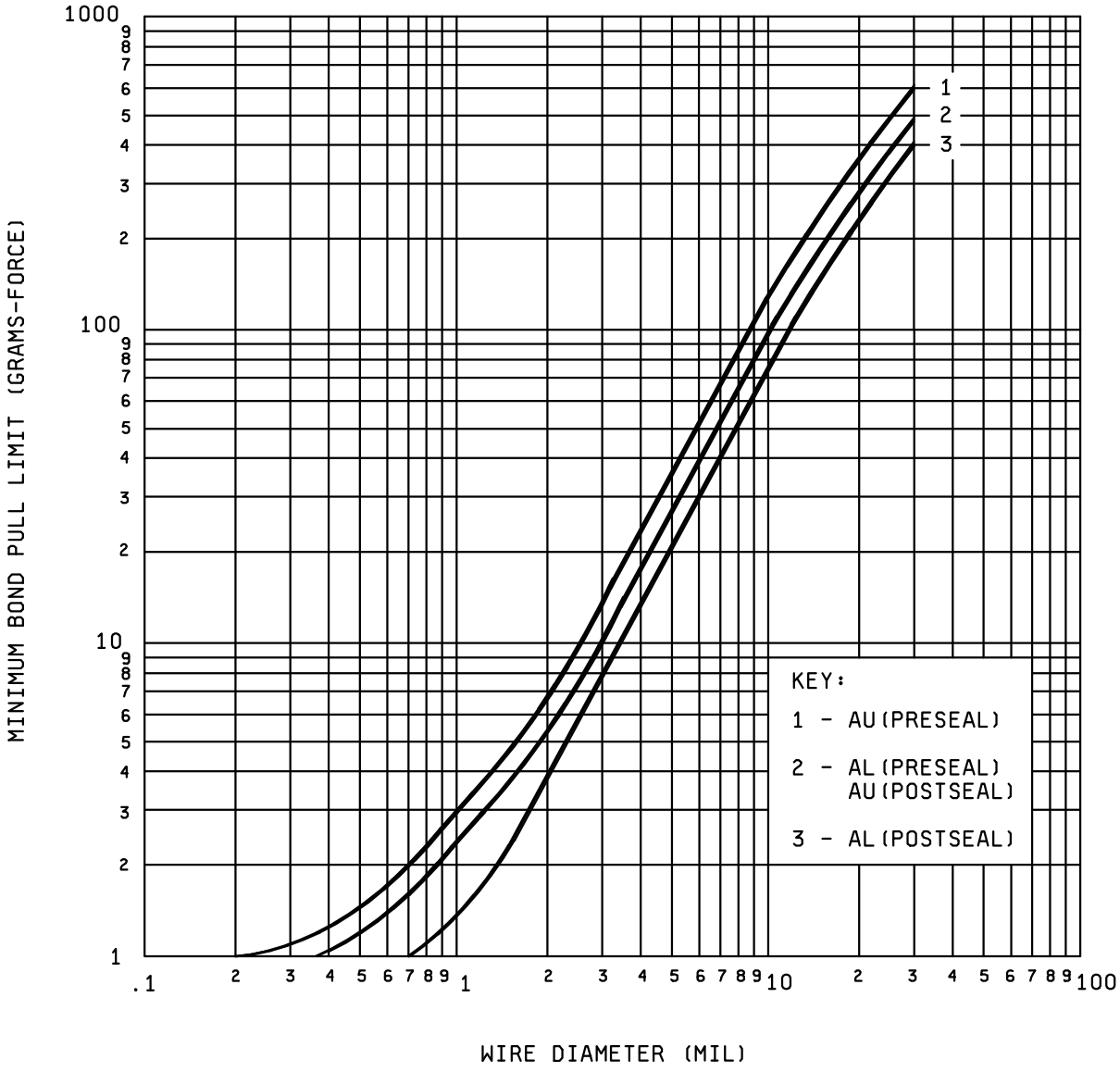

NOTE: The minimum bond strength should be taken from table I. Figure 2011-2 may be used for wire diameters not specified in table I.

FIGURE 2011-2. Minimum bond pull limits.

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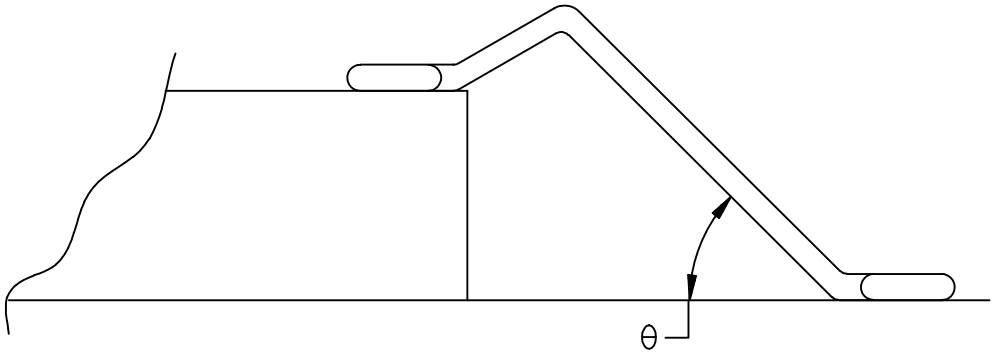

FIGURE 2011-3. Wire loop angle.

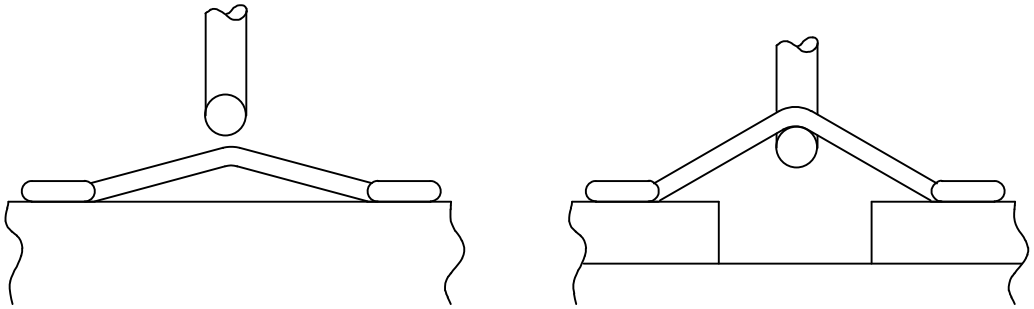

FIGURE 2011-4. Flat loop wire pull testing.

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METHOD 2012.11

RADIOGRAPHY

1. PURPOSE. The purpose of this examination is to nondestructively detect defects within the sealed case, especially those resulting from the sealing process, and internal defects such as foreign objects, improper interconnecting wires, and voids in the die attach material or in the glass when glass seals are used. It establishes methods, criteria, and standards for radiographic examination of semiconductor and hybrid devices.

NOTE: For certain device types, opacity of the construction materials (packages or internal attachment) may effectively prevent radiographic identification of certain types of defects from some or all possible viewing angles. This factor should be considered in relation to the design of each device when application of this test method is specified.

1.1 Definitions. A more complete listing of definitions related to radiography can be found in ASTM E 1316.

1.1.1 Device Under Test (DUT). The microelectronic device (monolithic or hybrid) that is the subject of the radiographic examination.

1.1.2 Digital radiography. For purposes of this test method, digital radiography is defined as a radiographic examination using x-ray as the source whereby the image is translated into digital data that is passed through an information processing algorithm to be transferred to a viewing media such as a display or monitor. It differs from film radiography, which is a direct transfer of the image onto film.

1.1.3 DUT lot. Multiple devices, all of the same type, that have been manufactured in a single production run and sequentially being tested as a group.

1.1.4 Dynamic Radiography. The acquisition of images in a continuous, full volumetric fashion where the DUT is placed in motion by a manipulation system to view multiple areas, axes and depths. (This is also referred to as real-time radiography.) Dynamic radiography generally results in a higher radiation dose to the DUT than static radiography due to longer exposure times.

1.1.5 Image Quality Indicator (IQI). A device manufactured with known conditions to be used to judge image quality. IQI's shall conform to ASTM E 801. An IQI is a standard used for the purpose of qualifying/calibrating the apparatus. An IQI has built-in physical properties that can be used to adjust system parameters for best imaging results.

1.1.6 Qualified Test Personnel. An individual trained on the apparatus being used for radiography, and who is qualified to image or inspect. Personnel involved in acquisition or interpretation of radiographic images shall have training in radiographic imaging procedures and techniques so that defects revealed by this method can be validly interpreted and compared with applicable standards. Training shall be specific to the radiographic system (film or digital) as well as DUT design and failure criteria. The company employing the test personnel shall have a documented training program and will qualify test personnel internally.

1.1.7 Radiation Parameters. The radiation source related variables that can affect the examination outcome for the selected system configuration. Examples are source energy, collimation and intensity, focal spot size, filter in the X-ray beam, range of source to object distance, range of object to detector distance, and source to detector distance.

1.1.8 Real Time Radiography. See 1.1.4, Dynamic Radiography.

1.1.9 Representative Quality Indicator (RQI). Similar to an IQI, an RQI is a device manufactured with known conditions to be used as a representative object for the DUT. RQI's shall conform to ASTM E 1817. An RQI is a device manufactured for the purpose of qualifying/calibrating the apparatus. An RQI has built-in physical properties that can be used to adjust system parameters for best imaging results.

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1.1.10 Static Radiography. The acquisition of images where the DUT is at rest, or fixed in location, resulting in a single distinct image about a predetermined area, axis, and depth.

1.1.11 System Performance Quality Parameters. The features of a radiographic image that determine its usefulness in detecting defects. These features include unsharpness, contrast, noise, signal and bad pixels.

1.1.12 Computed Radiography (CR). A two-step radiological imaging process; first, a storage phosphor imaging plate is exposed to penetrating radiation; second, the luminescence from the plate's photo stimulate-able luminescent phosphor is detected, digitized, and presented via an image display monitor. CR is a film replacement technology. Computed Radiography is not recommended for this method due to inherent artifacts present in the imaging plates that will appear as extraneous matter in the DUT.

1.1.13 Computed Tomography (CT). A radiological imaging process that provides an image of a selected plane in an object to the relative exclusion of structures that lies outside the plane of interest. CT is used to generate a three-dimensional image of an object from a large series of two-dimensional radiographic images taken around a single axis of rotation.

1.1.14 Lp/mm . Abbreviation for line pairs per millimeter

2. APPARATUS.

2.1 Apparatus – Film Based Radiography. The apparatus and material for this test shall include:

2.1.1 Radiographic x-ray source. A radiographic x-ray source with a sufficient voltage range to meet contrast requirements for the inspection of the DUT as defined in paragraph 3.4.1, when used in conjunction with the film required in

2.1.2 The focal distance shall be adequate to resolve a separation of 0.0508 mm (0.002 inch) between two solid objects. A line pair gauge with 20 line pairs per millimeter can be used to verify this resolution.

2.1.2 Radiographic viewer. Film systems meeting Class 1, film type B (or better) requirements of Radiographic viewer. The film viewer used shall have the following minimum capability:

a. Luminance - Film viewer shall have a minimum transmitted light (luminance) of 10000 cd/m^2 for film densities of 2.5 optical density or less.

   NOTE: Film viewers may be tested for luminance using Figure 1 of ASTM E 1742.

b. The viewer shall be located in an area with subdued background lighting, which does not result in glare on the viewing screen. Background ambient light levels shall not exceed 3 foot candles (illuminance) at the surface of the film viewer.

c. Color of light used to illuminate the radiograph shall be white, color temperature of 5000-6250K.

2.1.3 Light Meter.

a. Luminance. Calibrated light meters used to test film viewer transmitted light shall measure luminance in candelas per meters squared (cd/m^2).

b. Illuminance. Calibrated light meters used to test ambient background light shall measure illuminance in foot candles.

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2.1.4 Magnifiers. 10X to 40X.

2.1.5 Holding fixtures. Holding fixtures may be used if they are capable of holding devices in the required positions without interfering with the accuracy or ease of image interpretation.

2.1.6 Film holder. A 1.6 mm (0.0625 inch) minimum lead-topped table or lead-backed film holders to prevent back scatter of radiation.

2.1.7 Electrostatic Discharge (ESD). The system and any holding fixtures used shall be ESD safe and used in compliance with applicable ESD protocol. (Note: Film can be placed in an ESD bag to maintain path to ground.)

2.1.8 Radiographic standards.

2.1.9 Quality Indicators. Image Quality Indicators (IQI) or Representative Quality Indicators (RQI) meeting the requirements of ASTM E 801 or ASTM E 1817 are required.

2.1.10 Filters. Filters may be used to harden the x-ray beam to reduce radiation dose. ASTM E 1161 may be consulted for further guidance on filter selection.

2.2 Apparatus – Digital Radiography. The apparatus and material for this test shall include:

2.2.1 Radiographic equipment. The equipment used in this examination will have sufficient voltage, focal spot, and resolution to provide an image of the DUT in accordance with paragraph 3.4.1.

NOTE: Computed radiography is not an acceptable radiographic method for electronic components.

2.2.2 Radiographic parameters. Radiographic parameters of the digital x–ray apparatus shall provide appropriate image quality such that all defects specified in paragraphs 3.10 and 3.11 for particular package types are readily apparent.

2.2.3 Radiographic display monitor. An image display monitor that has the following capability shall be used.

a. Brightness: The minimum brightness at maximum Digital Driving Level (DDL) shall be 170 cd/m^2 (luminance),

b. Contrast: The minimum contrast as determined by the ratio of the screen brightness at the maximum DDL compared to the screen brightness at the minimum DDL shall be 250:1,

c. High Contrast Resolution: The image display monitor shall be capable of displaying linear patterns of alternating pixels at full contrast (0% and 100% DDL) in both the horizontal and vertical directions without aliasing at the display center and each of the four corners,

d. Low Contrast Resolution: The image display monitor shall be capable of discriminating the horizontal and vertical low contrast 1% modulation patterns (50% and 51% DDL) at the display center and each of the four corners.

e. Flicker and Distortion: The image display monitor shall be free of screen flicker or discernible geometric distortion.

f. Small Contrast Change: The image display monitor shall be capable of displaying a 5% DDL block against a 0% DDL background while simultaneously displaying a 95% DDL block against a 100% background in a manner clearly perceptible to the user.

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2.2.3.1 Image Display Monitor Test Pattern. A test pattern shall be used for verifying that the image display monitor meets the requirements of 2.2.3. The test pattern shall automatically adjust to the image display monitor's resolution and aspect ratio. Alternatively, an image file (lossless file type) may be used. When an image file is used to confirm 2.2.3 c & d, it shall be displayed at 1:1 (100%). If the image as displayed at 1:1 is smaller than the display monitor, the image shall be moved around the monitor display area to meet the location requirements of 2.2.3 c & d. The SMPTE RP 133 test pattern meets the requirements for this verification.

2.2.3.2 Image viewing area. The image viewing area shall be an area with subdued background lighting and shall be arranged to preclude reflective glare from the surface of the image display monitor. Subdued lighting, rather than total darkness, is required in the image viewing room.

a. Background Ambient Light Level. Background ambient light levels shall not exceed 3 foot candles (illuminance) at the image display monitor used for image analysis and final disposition. Ambient light levels shall be measured at the surface of the image display monitor with the monitor off.

2.2.4 Light Meter.

a. Luminance. Calibrated light meters used to test image display monitors for brightness and contrast shall measure luminance in candelas per meters squared (cd/m^2).

b. Illuminance. Calibrated light meters used to test ambient background light shall measure illuminance in foot candles.

2.2.5 Holding fixtures. Holding fixtures may be used if they are capable of holding devices in the required positions without interfering with the accuracy or ease of image interpretation.

2.2.6 Electrostatic Discharge (ESD). The system and any holding fixtures used shall be ESD safe and used in compliance with applicable ESD protocol.

2.2.7 Quality Indicators. Image Quality Indicators (IQI) or Representative Quality Indicators (RQI) meeting the requirements of ASTM E 801 or ASTM E 1817.

2.2.8 Line Pair Gauge. A Line Pair Gauge with a minimum line pair spacing of 20 line pairs per mm shall be used to judge the quality of the system output.

2.2.9 Filters. Filters may be used to harden the x-ray beam to reduce radiation dose. ASTM E 1161 may be consulted for further guidance on filter selection.

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3. PROCEDURE. The X-ray exposure factors; voltage, current, exposure time and magnification settings shall be selected or adjusted as necessary to obtain satisfactory exposures and achieve maximum image details within the sensitivity requirements for the device or defect features the radiographic test is directed toward.

NOTE: For certain device types, opacity of the construction materials (packages or internal attachment) may effectively prevent radiographic identification of certain types of defects from some or all possible viewing angles. If the best attempt to obtain a clear image results in the inability of the radiographer to clearly see some or all of the reject-able criteria, this shall be noted as an exception on the inspection report and certificate of compliance.

3.1 Mounting and views. The devices shall be mounted in the holding fixture so that the devices are not damaged or contaminated and are in the proper plane as specified. The devices may be mounted in any type of fixture and masking may be employed to isolate multiple specimens provided the fixtures or masking material do not block the view from X-ray source to the film or detector of any portion of the body of the device.

3.1.1 Views. When the required view(s) show internal feature(s) that require a different viewing axis for verification and disposition of a failure mode specified in this test method, then additional views (either Z or X direction) shall be taken as record of the disposition.

3.1.1.1 Flat packages, dual-in-line packages, hybrid packages, and single ended cylindrical devices. Flat packages, dual-in-line packages, hybrid packages, and single ended cylindrical devices, unless otherwise specified, shall have one view taken with the X-rays penetrating in the Y direction as defined on figures 1 and 2 of MIL-STD-883, GENERAL REQUIREMENTS. The die/cavity interface shall be positioned in such a manner relative to the film or detector to avoid image distortion.

3.1.1.2 Stud-mounted and cylindrical axial lead devices. Stud-mounted and cylindrical axial lead devices, unless otherwise specified, shall have one view taken with the X-rays penetrating in the X direction as defined in figures 1 and 2 of MIL-STD-883, GENERAL REQUIREMENTS. The die/cavity interface shall be positioned in such a manner relative to the film or detector to avoid image distortion”

3.1.1.3 Additional views. When required, additional views may be used to resolve internal features.

3.2 Image Quality Indictors. Image Quality Indicators in accordance with ASTM E 801 shall be used. As an alternative, Representative Quality Indicators in accordance with ASTM E 1817 may be used.

3.2.1 Film. IQIs or RQIs bracketing the film density of the area of interest, and prescribed in the DUT Specific Technique (see 3.4.1), shall be positioned at the outer edges of the film, in opposite corners, and shall not block the view from X-ray source to the film of any portion of the body of the device.

3.2.2 Digital. Prior to performing imaging on a DUT Lot, the radiographic examination system shall be sampled using the IQIs or RQIs prescribed in the DUT Specific Technique (see 3.4.1). These images collected prior to the DUT Lot imaging shall be saved for comparison with images of the same IQIs or RQIs taken following the DUT Lot imaging. Grayscale values of the IQI/RQI images collected post-DUT Lot imaging shall be within ±15% of the grayscale values of the reference image collected prior to DUT Lot imaging and all features of interest in the IQI or RQI shall be visible in the images collected before and after DUT Lot imaging. If the IQI/RQI images collected before and after DUT Lot imaging do not meet these requirements, it shall be presumed that the radiographic examination system conditions have been altered from the pre-DUT Lot imaging set up and the DUT Lot imaging shall be performed again after proper adjustments are made.

3.2.2.1 DPA/FA IQI/RQI Samples. Post inspection images of IQI or RQI is not required, however, when the imaging equipment is shut down for any reason (e.g., end of shift), additional IQI or RQI images shall be captured prior to continuing inspections.

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3.3 Radiographs and marking.

3.3.1 Radiographs/Radiographic Images. Procedures and techniques developed from the DUT specific technique (see 3.4.1) shall be used for radiographic exposure/imaging.

3.3.1.1 Film. The radiographic film shall be in a film holder backed with a minimum of 1/16 inch lead or the holder shall be placed on the lead topped table. The film shall be identified using techniques that print the following information, either photographically, or created as an image using lead numbers or other means on the radiograph:

a. Device manufacturer's name or code identification number.

b. Device type or Part or Identifying Number.

c. Production lot number or date code or inspection lot number.

d. Radiographic film view number.

e. Date.

f. Device serial or cross reference numbers, when applicable.

g. X-ray laboratory identification, if other than device manufacturer

3.3.1.2 Digital. Images shall be acquired using static radiography, unless dynamic (real-time) radiography is specified in the contract. Images shall be maintained and stored for archive in an electronic data file format that does not reduce the resolution or bit depth of the original image (loss-less file type). The following information shall be permanently associated with the archived image file. This may be achieved by annotating the image with the information, by including all information in the file name, or by including a reference text file with image file correlation.

a. Device manufacturer's name or code identification number.

b. Device type or Part or Identifying Number.

c. Production lot number or date code or inspection lot number.

d. Radiographic view (axis).

e. Date.

f. Device serial or cross reference numbers, when applicable.

g. X-ray laboratory identification, if other than device manufacturer.

3.3.2 Serialized devices. When device serialization is required, each device shall be readily identified by a serial number. When multiple devices are radiographed in a single image, they shall be arranged in consecutive, increasing serial order. When a device is missing, the blank space shall contain either the serial number or other X-ray opaque object to readily identify and correlate X-ray data. When large skips occur within serialized devices, the serial number of the last device before the skip and the first device after the skip may be used in place of the multiple opaque objects.

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3.3.3 Special device marking. When specified (see 4.c), the devices that have been X-rayed and found acceptable shall be identified with a blue dot on the external case. The blue dot shall be approximately 1.6 mm (0.0625 inch) in diameter. The color selected from FED-STD-595 shall be any shade between 15102-15123 or 25102-25109. The dot shall be placed so that it is readily visible but shall not obliterate other device marking.

3.4 Test Plans. A technique for each DUT lot will be generated to ensure repeatability of the examination.

3.4.1 DUT Specific Technique. The DUT specific technique shall be generated to address the unique qualities for that device type, and how that device type is subjected to the radiographic examination, including all information needed to perform a repeatable examination. The DUT Specific Technique shall reference internal operating procedures, if applicable, and acceptance criteria used in the inspection. The plan shall include:

a. The specific device or devices to be examined by manufacturer and part number,

b. Radiographic system (apparatus) used and support equipment, such as the IQIs/RQIs used to bracket the DUT.

c. DUT views (axes). When necessary a drawing, sketch or photograph of the DUT showing the radiation beam axis position(s) of the detector for each and all variations of the DUT orientation and x-ray beam angle.

3.4.1.1 Test Parameters. For each view, the following parameters shall be defined: kV, Current/Power, the IQI(s) selected representing the grayscale value of the area(s) interest of the DUT or the RQI associated with the DUT. For film radiography, set up geometry and exposure time shall be recorded. For digital radiography, parameters can vary with the selected test equipment. The tester shall define those parameters for the particular test set being used. Examples of required parameters include focal spot size, frame averaging, s, set up geometry and geometric magnification, detector settings (e.g., frames per second, gain, binning, etc.) and image evaluation settings (e.g., digital zoom, window width/window level, image enhancement, etc.), as applicable to the selected apparatus. Radiographs/radiographic images shall be made for each view required (see 3.1.1).

a. Film. The DUT Specific Technique shall define test parameters such that the resulting radiographs achieve resolution sufficient to resolve a wire 0.0254 mm (0.001 inch) in diameter, a bead 0.0508 mm (0.002 inch) in diameter, exhibit less than 10 percent distortion and an “H” and “D” film density between 1.0 and 2.5 in the area of interest of the device image and the IQI.

b. Digital. The X-ray exposure factors and image file resolution shall be selected to resolve a wire 0.0254 mm (0.001 inch) in diameter, a bead 0.0508 mm (0.002 inch) in diameter, a separation of 0.0508 mm (0.002 inch) between two solid objects and shall result in an image with a minimum pixel value of 15% of the bit depth range and maximum pixel value of 90% of the saturation limit of the detector. The flow chart presented in Figure 2012-1 provides a suggested method of determining appropriate test parameter selection. One image shall be taken of the overall component. If that image meets the resolution requirements, no further images are required. If that image does not meet the resolution requirements, additional images of higher geometric magnification shall be collected, providing full coverage of the device area (i.e., overlapping views), at the lowest geometric magnification which meets the resolution requirements, unless otherwise specified.

NOTE: For both film and digital radiography, multiple exposure factors and test parameter settings may be required to be able to fully inspect the DUT.

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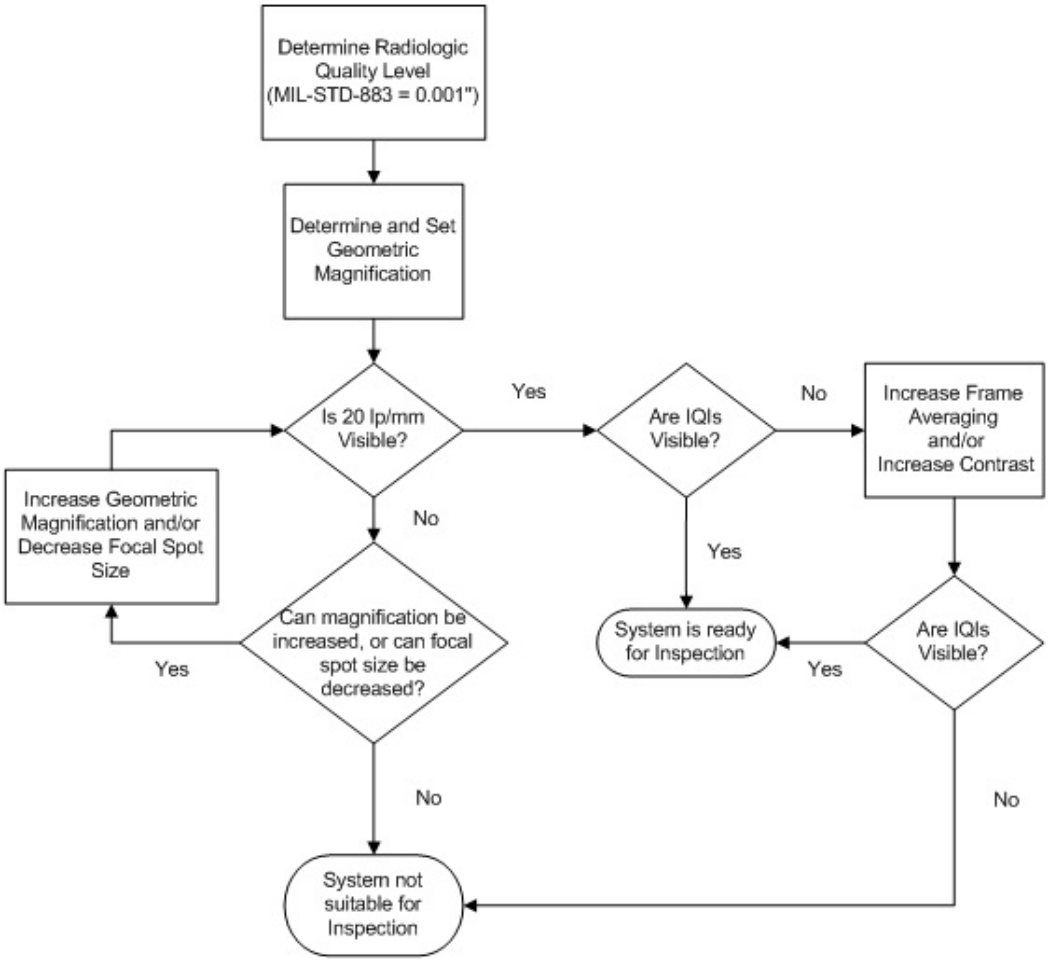

FIGURE 2012-1. Appropriate test parameter selection.

3.4.1.2 Further required details. When applicable, the following items are part of the DUT Specific Test Plan.

a. Film specific requirements. Part masking; added radiation source collimation; allowable range of radiation energy and x-ray beam current, and the focal spot size for each view; beam filtration; examination geometry and coverage of each view; all system settings that can be changed by the operator to affect the outcome of the radiographic examination such as film processing variables.

b. Digital specific requirements. Classification of the DUT into zones for radiographic examination, detector field of view; all system and software settings that can be changed by the operator to affect the outcome of the radiographic examination such as display settings and image processor variables; and the recording media and image file format.

3.4.2 ESD Precautions. ESD precautions shall be maintained at all times during handling and inspection, as appropriate for the ESD sensitivity of the DUT.

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3.4.3 Radiation Dose Control. Semiconductor materials may be sensitive to radiation. Precautions should always be taken to minimize radiation dose; however, precautions shall always be taken to minimize dose when devices are designated as radiation sensitive. Precautions may include, but are not limited to, minimizing exposure time, maximizing distance from the x-ray source, employing filtering or shielding and minimizing the number of devices placed in the cabinet during exposure. When dose characterization of the equipment is to be performed, it should mimic all conditions the DUT will be subjected to, including any shielding techniques employed for reducing secondary exposure. Secondary radiation dose to devices outside or adjacent to the DUT must be recognized and considered when calculating total dose during x-ray equipment characterization. ASTM E 1161 may be consulted for processing techniques.

3.5 Film Processing and Image Processing/Enhancement.

3.5.1 Film Processing. The radiographic film manufacturer's recommended procedure shall be used to develop the exposed film, and film shall be processed so that it is free of processing defects such as fingerprints, scratches, fogging, chemical spots, blemishes, etc.

3.5.2 Digital Image Evaluation. Image evaluation adjustments for image zoom, window width and level settings (contrast and brightness) and any image processing/enhancement shall be performed in a manner consistent with the DUT Specific Technique and shall not reduce the ability to identify required features in the image of the DUT and IQIs/RQIs.

a. Window Width (Contrast) and Level (Brightness). The initial image evaluation window width and level settings shall be documented in the DUT specific technique, either with quantitative values or by defined viewing presets. This includes any multiple window width and level values or viewing presets required due to changes in the DUT thickness or material.

b. Image processing (i.e., enhancement filters). Image processing used for final product acceptance shall be verified by adequately displaying the pertinent features of the DUT and IQI/RQI and shall be documented on the approved DUT specific radiographic examination technique.

   Since some image processing filters can increase image noise and/or generate artifacts, the image interpreter may remove the filter for the purpose of evaluating whether an indication is false, relevant or non-relevant, however, initial image review shall be performed with the filter applied when required by the DUT specific technique.

c. Digital Magnification (Image Zoom). Digital magnification shall be based on the minimum size of the feature of interest, and the size and resolution of the image display monitor. Images shall not be inspected at less than 100% display size, as reduction of image size below 100% results in loss of displayed data due to pixilation. For the purpose of making measurements or a correct disposition, the image may be digitally magnified beyond that specified in the DUT specific technique.

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3.6 Qualified Personnel. The radiographic examination shall be performed only by Qualified Test Personnel as defined in paragraph 1.2.f, following the test procedures provided in the DUT Specific Technique; or performed by someone who is both under the control and supervision of Qualified Test Personnel and is trained on the apparatus being used. The following minimum vision requirements shall apply for personnel evaluating radiographic images:

a. Distant vision shall equal at least 20/30 Snellen in at least one eye, corrected or uncorrected.

b. Near vision shall equal at least 20/25 Snellen at 16 inches (±1 inch) in at least one eye, corrected or uncorrected or such that the operator can read Jaeger No. 1 at a distance of not less than 12 inches in at least one eye.

c. Vision tests shall be performed by an oculist, optometrist, or other professionally recognized personnel at least once a year. Personnel authorized to conduct radiographic tests shall be required to pass the vision tests specified in 3.6 a and b.

3.7 Safety. The premises and equipment shall present no hazards to the safety of personnel or property. NCRP 49, NCRP 116 and NCRP 151 may be used as guides to ensure that radiographic procedures are performed so that personnel shall not receive a radiation dosage exceeding the maximum permitted by city, state, or national codes.

3.8 Interpretation of radiographs/radiographic images. Utilizing the equipment specified herein, radiographs shall be inspected to determine that each device conforms to this standard and defective devices shall be rejected.

3.8.1 Film. Viewing masks may be used when necessary. Any radiograph not clearly illustrating the features in the radiographic quality standards is not acceptable and another radiograph of the devices shall be taken. Inspection shall be performed at a magnification between 10X and 40X.

3.8.2 Digital. Geometric magnification for image collection shall be determined as specified in 3.4.1.1.b. Magnification at the time of inspection is dependent on the spatial resolution of the detector. Inspection magnification may be achieved through a combination of geometric magnification and increasing image display size, until image pixilation occurs or IQI/line pair resolution is lost. Images shall not be inspected at less than 100% display size, as reduction of image size below 100% results in loss of displayed data due to pixilation. All images shall contain a feature of known dimension, from which displayed magnification can be calculated; examples include gold bond wires, the overall package (if dimensions are recorded) or marker bars inserted using calibrated imaging software.

3.9 Reports of records.

3.9.1 Reports of inspection. For class S devices, or when specified for other device classes, the manufacturer shall furnish inspection reports with each shipment of devices. The report shall describe the results of the radiographic inspection, and list the purchase order number or equivalent identification, the PIN, the date code, the quantity inspected, the quantity rejected, and the date of test and which devices utilize the note in 3.10.2.1. For each rejected device, the PIN, the serial number, when applicable, and the cause for rejection shall be listed.

3.9.2 Radiograph submission.

3.9.2.1 Film. Photographic reproduction of complete radiographs may be submitted as long as image quality is not reduced from the original radiograph, but artistic renditions are not acceptable.

3.9.2.2 Digital. An archive of data from each radiographic examination shall be kept and stored in a proper repository for the period specified. The archive shall include the DUT Specific Technique, a complete set of radiographic images of the DUT and IQI/RQIs, and the signed examination reports and/or tabulated results. Data file format is to follow the guidance of 3.3.1.2. It is the responsibility of the radiography service provider to ensure that adequate controls are in place to maintain the fidelity of identifying information and of the original images.

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3.9.3 Radiograph and report retention. When specified, the manufacturer shall retain a set of the radiographs and a copy of the inspection report. These shall be retained for the period specified.

3.10 Examination and acceptance criteria for monolithic devices.

3.10.1 Device construction. Acceptable devices shall be of the specified design and construction with regard to the characteristics discernible through radiographic examination. Devices that deviate significantly from the specified construction shall be rejected.

3.10.2 Individual device defects. The individual device examination shall include, but not be limited to, inspection for foreign particles, solder or weld "splash", build-up of bonding material, proper shape and placement of lead wires or whiskers, bond of lead or whisker to semiconductor element and lead or whisker to terminal post, semiconductor metallization pattern, and mounting of semiconductor element. Any device for which the radiograph reveals any of the following defects shall be rejected:

3.10.2.1 Presence of extraneous matter. Extraneous matter (foreign particles) shall include, but not be limited to:

a. Any foreign particle, lose or attached, greater than 0.025 mm (0.001 inch) (see figure 2012-2), or of any lesser size which is sufficient to bridge non-connected conducting elements of the semiconductor device.

b. Any wire tail extending beyond its normal end by more than two wire diameters at the semiconductor die pad or by more than four wire diameters at the semiconductor package post (see figure 2012-2).

c. Any burr on a post (header lead) greater than 0.08 mm (0.003 inch) in its major dimension or of such configuration that it may break away.

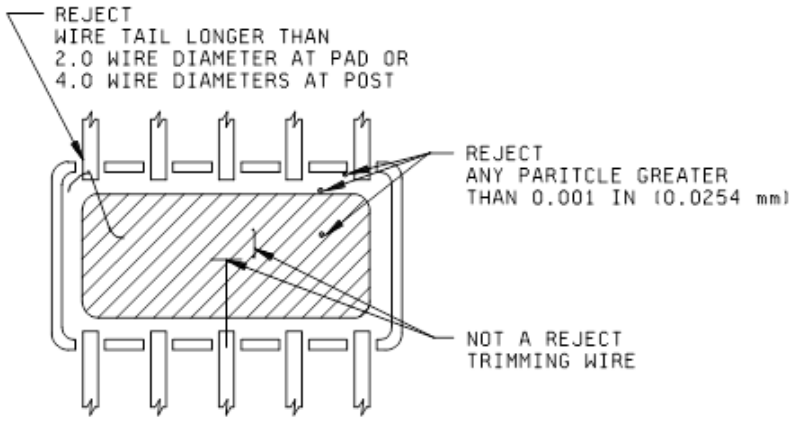

FIGURE 2012-2. Extraneous matter.

d. Excessive semiconductor element bonding material build-up:

(1) A semiconductor element shall be mounted and bonded so that it is not tilted more than 10° from the normal mounting surface. The bonding agent that accumulates around the perimeter of the semiconductor element whether or not it touches the side of the semiconductor element shall not accumulate to a thickness greater than the height of the semiconductor element (see figures 2012-3 and 2012-4), or any lead or post, or be separated from the main bonding material area (see figure 2012-10).

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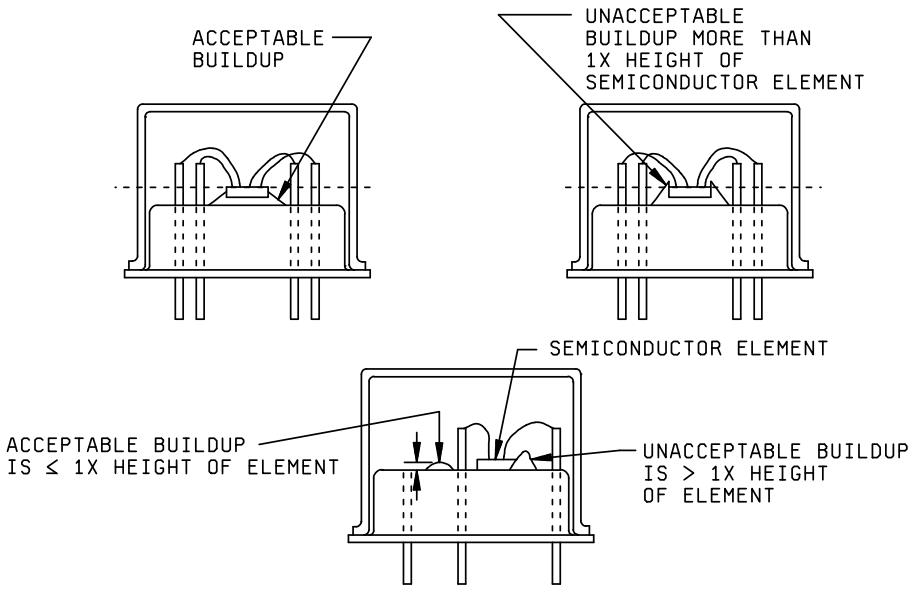

FIGURE 2012-3. Acceptable and unacceptable bonding material build-up.

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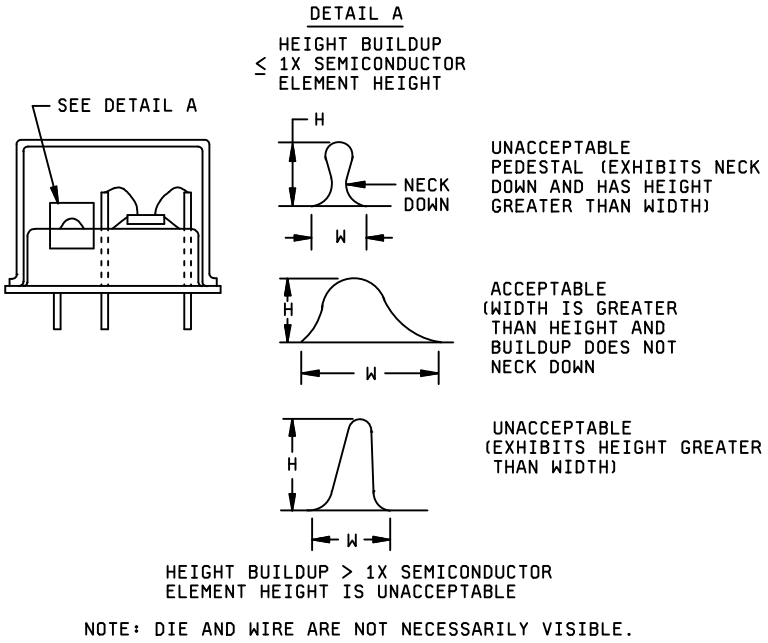

FIGURE 2012-4. Extraneous bonding material build-up.

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(2) There shall be no visible extraneous material 0.025 mm (0.001 inch) or larger in the major dimension inside the semiconductor device. Loose bonding material will be considered extraneous material. Excessive (but not loose) bonding material will not be considered extraneous unless it fails to meet the requirements of 3.10.2.1.d.(1) or unless the accumulation of bonding material is such that the height of the accumulation is greater than the width of its base or that the accumulation necks down at any point (see figures 2012-3 and 2012-4).

NOTE: Devices with suspect foreign particles or extraneous material (in accordance with 3.10.2.1a and 3.10.2.1d(2) may be verified as acceptable provided the following conditions are met:

i. A visual inspection of the die attach area at 30X to 60X shall have been conducted prior to die attach sufficient to assure there are no anomalies in the die attach area which could interfere with effective die attach.

ii. The precap inspection shall have been conducted 100 percent to condition A of method 2010 of MIL-STD-883 and the devices shall have been inspected and prepared for sealing in a class 100 environment.

iii. All devices with X-ray defects to other criteria of 3.10 shall have been removed from the lot.

iv. Serialized devices with less than 5 suspect foreign particles and extraneous material shall be vibrated and shocked in accordance with PIND method 2020, condition A with the detector off.

v. A second X-ray examination of the failed view of the serialized devices after the PIND vibration/shock shall be conducted and each individual device shall be compared to its previous X-ray record.

vi. Any evidence of the suspect particle(s) having moved or having disappeared from their original location shall cause the device to be rejected. If the particle(s) exhibit no evidence of movement, the device may be accepted.

vii. The manufacturer doing the reinspection for suspect foreign particles or extraneous material shall implement a process monitor visual inspection of the cavity of the reinspected devices to assure that accepted devices do not have actual rejectable foreign particles or extraneous material (see 3.2.3.1a, 3.2.3.1d, and 3.2.3.1e, 3.2.3.2a, 3.2.3.2c, 3.2.3.2f, 3.2.3.2g, 3.2.3.2h, and 3.2.5 of method 2010). If any reinspected device fails the process monitor visual inspection, then all reinspected devices in the lot that have been inspected are subject to disposition. Corrective action, when appropriate, must be instituted. A procedure is required for the traceability, recovery, and disposition of all reinspected units accepted since the last successful monitor. The records for this monitor shall include identification of all lots which are reinspected to this note, identification of those lots which are monitored by this visual inspection, sample size, frequency of sampling, results of the visual inspections, and the package types reinspected.

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viii. In the case of a failed monitor, the records must identify all lots affected, their final disposition and a rationale for their disposition. Additionally, for a failed monitor, the records must also contain a description of any instituted corrective action together with its rationale. Records of this type shall be made available to the qualifying activity upon request.

e. Gold flaking on the header or posts or anywhere inside the case.

f. Extraneous ball bonds anywhere inside case, except for attached bond residue when rebonding is allowed.

3.10.2.2 Unacceptable construction. In the examination of devices, the following aspects shall be considered unacceptable construction and devices that exhibit any of the following defects shall be rejected.

a. Voids: When radiographing devices, certain types of mounting do not give true representations of voids. When such devices are inspected, the mounting shall be noted on the inspection report (see figure 2012-5).

1. Contact area voids in excess of one-half of the total contact area.

2. A single void which traverses either the length or width of the semiconductor element and exceeds 10 percent of the total intended contact area.

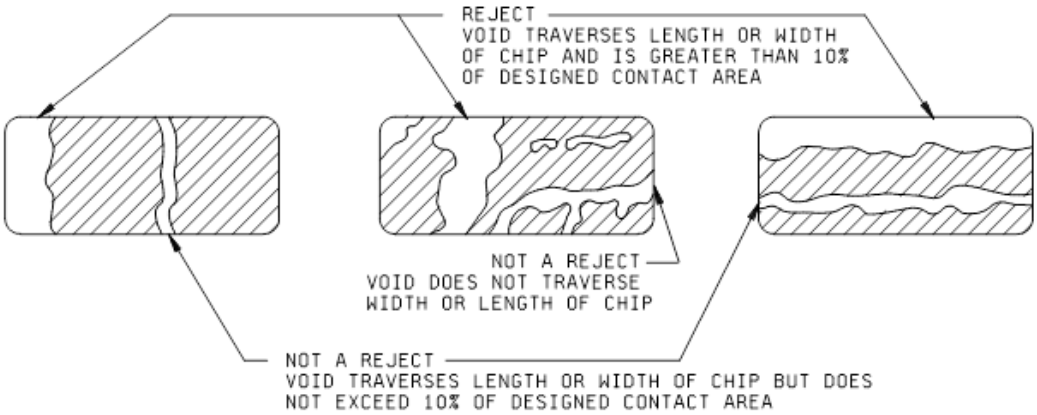

FIGURE 2012-5. Voids.

b. Wires present, other than those connecting specific areas of the semiconductor element to the external leads. Device designs calling for the use of such wires including jumper wires necessary to trim load resistors are acceptable (see figure 2012-2).

c. Cracks, splits, or chips of the electrical elements.

d. Excessive undercutting of the electrical elements (X and Z plane only, see figure 2012-6).

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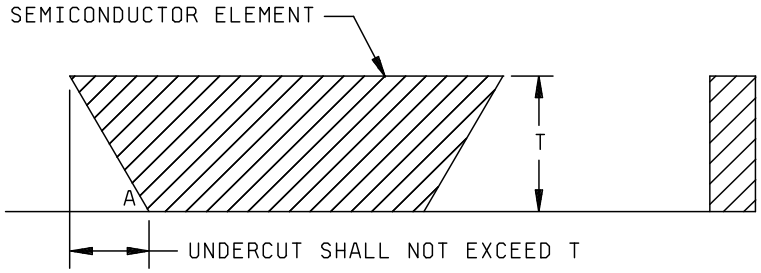

NOTE: Angle A shall be greater than 45°.

FIGURE 2012-6. Undercutting.

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e. Defective seal: Any device wherein the integral lid seal is not continuous or is reduced from its designed sealing width by more than 75 percent. Width reduction to less than 75% may be the result of either a single void or a combination of voids in the same width area (see figure 2012-7). Expulsion resulting from the final sealing operation is not considered extraneous material as long as it can be established that it is continuous, uniform and attached to the parent material and does not exhibit a ball, splash or tear-drop configuration (i.e., where the base support least dimension is smaller than the dimension it is supposed to support).

f. Inadequate clearance: Acceptable devices shall have adequate internal clearance to assure that the elements cannot contact one another or the case. No crossover shall be allowed except as permitted by 3.2.2e of method 2010 (condition A). Depending upon the case type, devices shall be rejected for the following conditions:

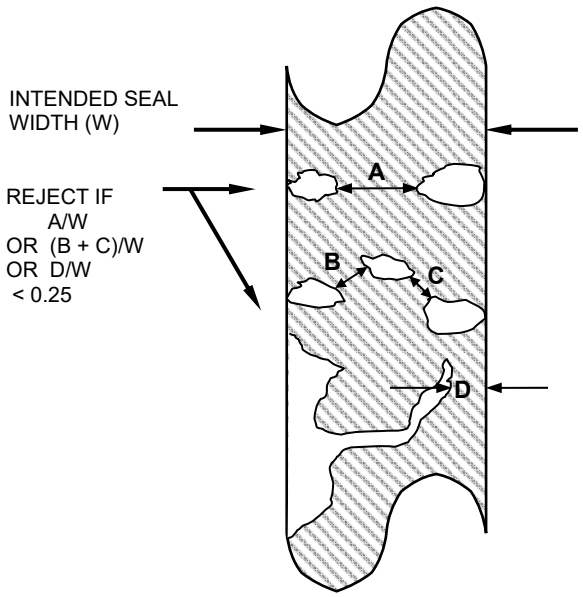

FIGURE 2012-7. Lid seal voids and rejection criterion.

NOTE: Any of the following criteria for bond wires shall not apply, if the wires are not visible In the X-ray.

1. Flat pack and dual-in-line (see figure 2012-8).

i. Any lead wire that appears to touch or cross another lead wire or bond, (Y plane only).

ii. Any lead wire that deviates from a straight line from bond to external lead and appears to be within 0.05 mm (.002 inch) of another bond or lead wire (Y plane only).

iii. Lead wires that do not deviate from a straight line from bond to external lead and appear to touch another wire or bond, excluding common wires, (Y plane only).

iv. Any lead wire that touches or comes within 0.05 mm (0.002 inch) of the case or external lead to which it is not attached (X and Y plane).

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v. Any bond that is less than 0.025 mm (0.001 inch) (excluding bonds connected by a common conductor) from another bond (Y plane only).

vi. Any wire making a straight line run from die bonding pad to package post that has no arc.

vii. Lead wires that sag below an imaginary plane across the top of the die bond (X plane only) except by design.

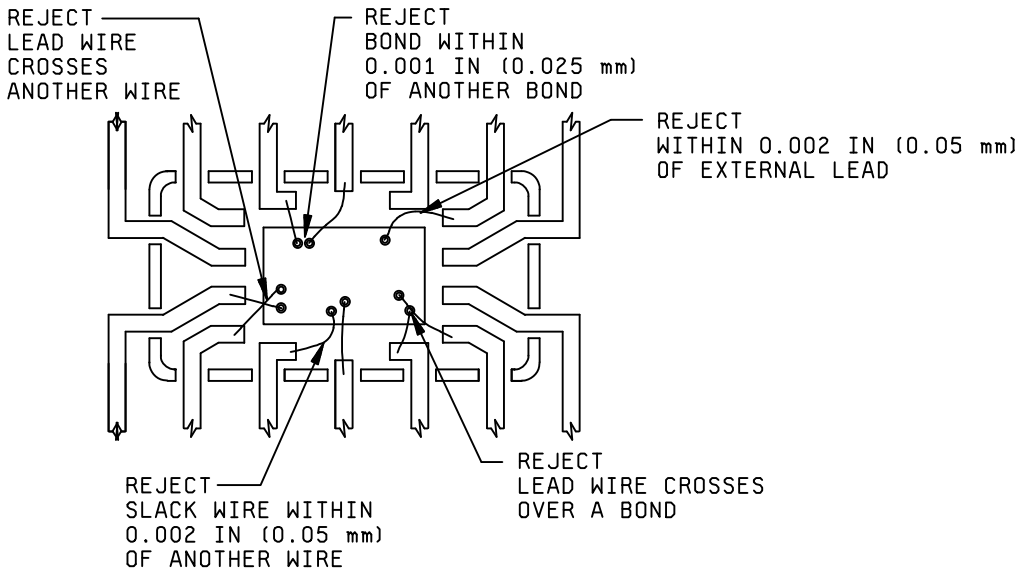

FIGURE 2012-8. Clearance in dual-in-line or flat pack type device.

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2. Round or "box" transistor type (see figure 2012-9).

   i. Any lead wire that touches or comes within 0.05 mm (0.002 inch) of the case or external lead to which it is not attached (X and Y plane).

   ii. Lead wires that sag below an imaginary plane across the top of the die bond (X plane only) except by design.

   iii. Any lead wire that appears to touch or cross another lead wire or bond (Y plane only).

   iv. Any lead wire that deviates from a straight line from bond to external lead and appears to touch or to be within 0.05 mm (0.002 inch) of another wire or bond (Y plane only).

   v. Any bond that is less than 0.025 mm (0.001 inch) (excluding bonds connected by a common conductor) from another bond (Y plane only).

   vi. Any wire making a straight line run from die bonding pad to package post that has no arc, unless specifically designed in this manner (e.g., clips or rigid connecting leads).

   vii. Any internal post that is bent more than 10° from the vertical (or intended design position) or is not uniform in length and construction or comes closer than one post diameter to another post.

   viii. Where a low profile case (such as TO-46) is used, any post which comes closer to the top of the case than 20 percent of the total inside dimension between the header and the top of the case. In devices which have the semiconductor element vertical to the header, any device where the semiconductor element comes closer than 0.05 mm (0.002 inch) to the header or to any part of the case.

   ix. Any case which does not have a header design incorporating a header edge or other feature (e.g., a "splash ring") to prevent solder or weld splash from entering the interior of the case.

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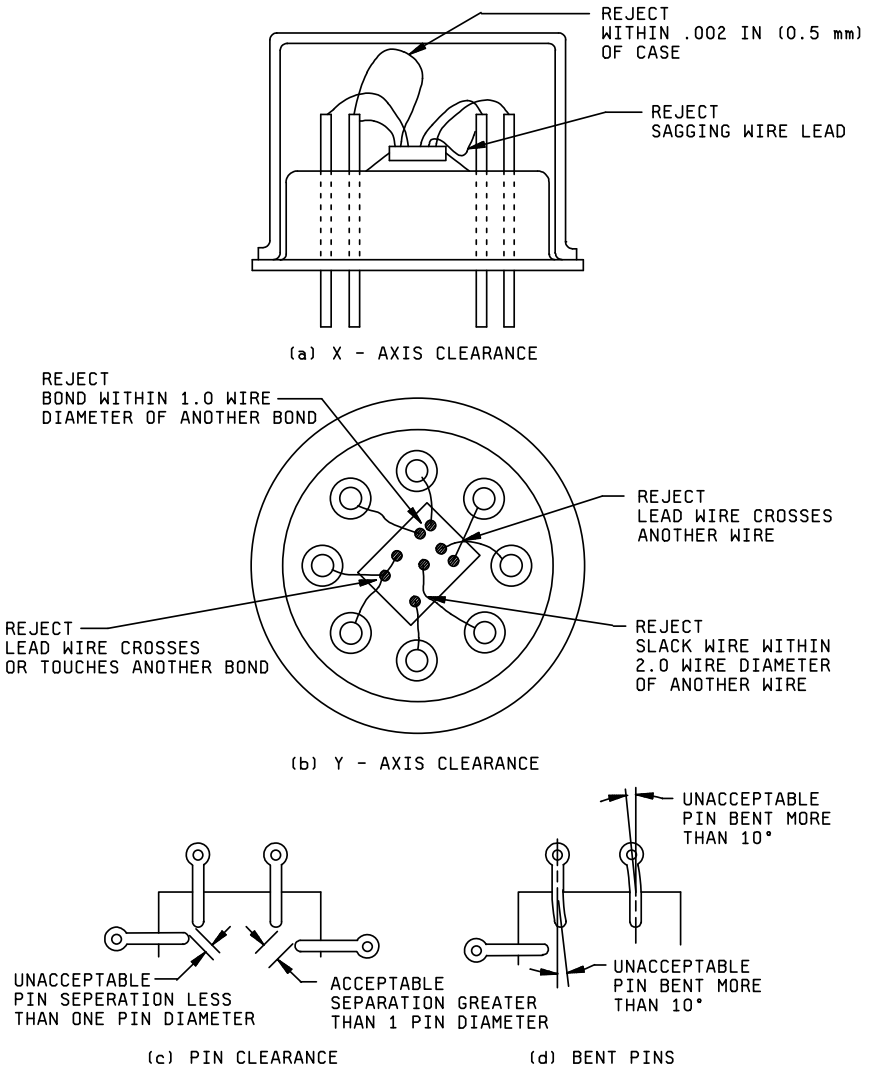

FIGURE 2012-9. Clearance in round or box transistor type device.

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3. Cylindrical axial lead type (see figure 2012-11).

i. Whisker to case distance less than one-half of the diameter of the external lead wire.

ii. Distance from case to semiconductor die or to any eutectic bonding material less than 0.05 mm (0.002 inch).

iii. Whisker tilted more than 5° in any direction from the device lead axis or deformed to the extent that it touches itself.

iv. C and S shaped whisker with air gap between any two points on it less than twice the diameter or thickness of the whisker wire. On diodes with whiskers metallurgically bonded to the post and to the die, the whisker may be deformed to the extent that it touches itself if the minimum whisker clearance zone specified in figure 2012-11 (a) is maintained.

v. Whiskerless construction device with anode and cathode lead connections displaced more than 0.25 mm (0.01 inch) with respect to the central axis of the device.

vi. Semiconductor element mounting tilted more than 15° from normal to the main axis of the device.

vii. Die hanging over edge of header or pedestal more than 10 percent of the die area.

viii. Less than 75 percent of the semiconductor element base area is bonded to the mounting surface.

ix. Voids in the welds, from any edge, between the leads and the heat sink slugs greater than 15 percent of the lead wire diameter. Any voids whatever in the central part of the area that should be welded.

x. Devices with package deformities such as, body glass cracks, incomplete seals (voids, position glass, etc.), die chip outs and severe misalignment of S and C shaped whisker connections to die or post.

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3.11 Examination and acceptance criteria for hybrid devices.

3.11.1 Device construction. Acceptable devices shall be of the specified design and construction with regard to the characteristics discernible through radiographic examination. Devices that deviate significantly from the specified construction shall be rejected.

3.11.2 Individual device defects. The individual device examination shall include, but not be limited to, extraneous matter, location and orientation of elements, cracks in the substrate that exceed 0.127 mm (0.005 inch) in length or point toward active metallization, adhesive build-up, solder splashes, placement of wires, voids in the lid seal (this may not apply to power hybrid devices), and improper wetting between the substrate(s) and the package. Any device for which the radiograph reveals any of the following defects shall be rejected:

3.11.2.1 Presence of extraneous matter (foreign particles).

a. Unattached foreign material greater than 0.025 mm (0.001 inch), or of any lesser size which is sufficient to bridge metallization or nonconnected conducting elements, that appears to be on the surface of the die, component, substrate, or within the package.

b. Attached foreign material that bridges metallization paths, package leads, lead to package metallization, functional circuit elements, junctions, or any combination thereof.

NOTE: Attached or unattached material may be verified by comparing two identical views with a mild mechanical shock, such as PIND test, between the two views.

c. Wire tails or extra wires which make contact with any metallization not connected to the wire, or which exceed four wire diameters in length at the substrate pad or package post, or two wire diameters at the top of a die or component.

d. Any evidence of solder, alloy, or conductive adhesive that appears to bridge noncommon metallization (i.e., wire(s), bonding post, active metallization or any combination thereof) not intended by design.

e. Gold flaking on the bonding post or anywhere inside the case.

3.11.2.2 Unacceptable construction.

a. Voids in substrate or component attachment medium.

1. Contact area voids in excess of one-half of the total contact area.

2. A single void which traverses either the length or width of the substrate or semiconductor element and whose area exceeds 10 percent of the total intended contact area.

NOTE: To obtain, and/or verify substrate attachment the use of a thermal resistance analyzer, which measures the thermal characteristics (heat dissipation), is strongly recommended.

b. Wires present, other than those connecting specific areas as per the drawing, except wires designated as tuning devices on the bonding diagram, and except where bond-offs are allowed.

c. Improper component placement.

d. Cracks, splits, or chips in the component or substrate which enter the active circuit area.

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e. Voids in the lid seal in which the seal is not continuous or is reduced from its design sealing width by more than 75 percent.

NOTE: Sealing voids may not be detectable within power hybrid packages.

f. Inadequate clearance.

1. Any wire that comes closer than 0.025 mm (0.001 inch) to another wire (excluding common wires) within a spherical radial distance from the bond perimeter of 0.127 mm (0.005 inch) for ball bonds, or 0.254 mm (0.010 inch) for ultrasonic and thermocompression wedge bonds.
NOTE: Insulated wires defined in the device specification/drawing are excluded from this criteria.

2. Excessive loop or sag in any wire so that it comes closer than two wire diameters to another wire, package post, unglassivated operating metallization, die, or portion of a package after a spherical radial distance from the bond perimeter of 0.127 mm (0.005 inch) for ball bonds or 0.254 mm (0.010 inch) for ultrasonic and thermocompression wedge bonds.

NOTE: Insulated wires defined in the device specification/drawing are excluded from these criteria.

3. Missing or extra wire(s) or ribbon(s) not in conformance with the bonding diagram except those wire(s) or ribbon(s) designated as microwave tuning devices on the bonding diagram.

NOTE: Extra wires added for statistical process control lot or lot sample bond strength/process machine/operator evaluation in accordance with MIL-PRF-38534 is excluded from this criteria.

4. Any wire that has no arc and makes a straight line run from die bonding pad to package post.

5. Wires crossing wires except common conductors or as allowed in 3.2.2e of method 2010 (condition A).

6. Excessive height in any component or wire loop such that it is closer than 0.127 mm (0.005 inch) to the lid when installed.

7. Any wires which are broken.
NOTE: Wire bond tails, as defined by method 2017, are excluded from this criteria.

8. Excessive sag where the wire lies on the substrate for a distance greater than 1/2 the distance between the edge of the substrate bonding pad and the chip to which the wire is bonded, or comes closer than 0.025 mm (0.001 inch) to runout of any conductive epoxy which mounts the chip.

9. Bonds placed so that the wire exiting from the bond crosses over another bond, except for common bonds.

NOTE: For RF/microwave devices, bonds placed so that the wire exiting from a bond crosses over another bond, except by design, in which case the clearance shall be two wire diameters minimum (common bonds are excluded from this criteria).

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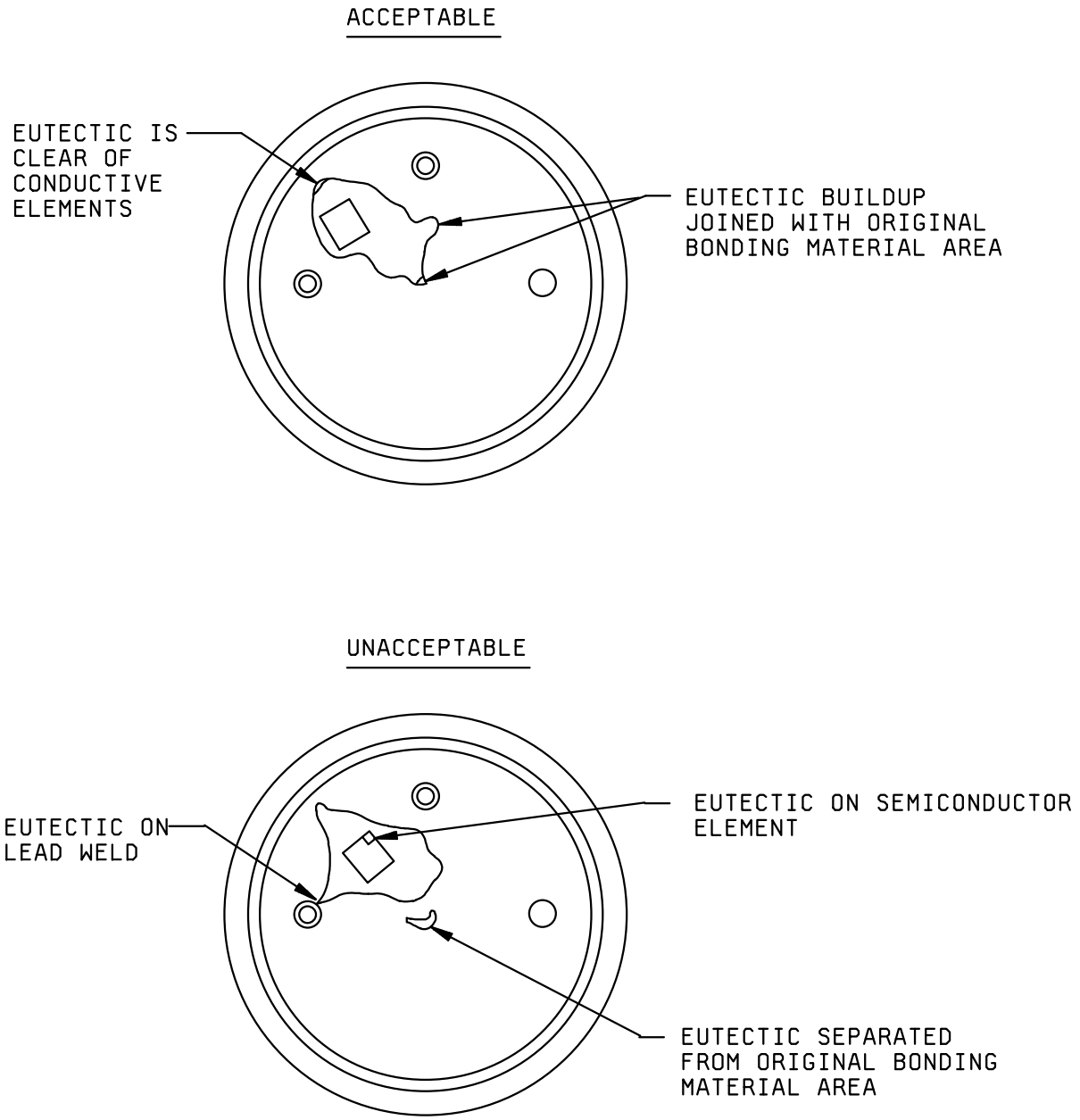

FIGURE 2012-10. Acceptable and unacceptable excess material.

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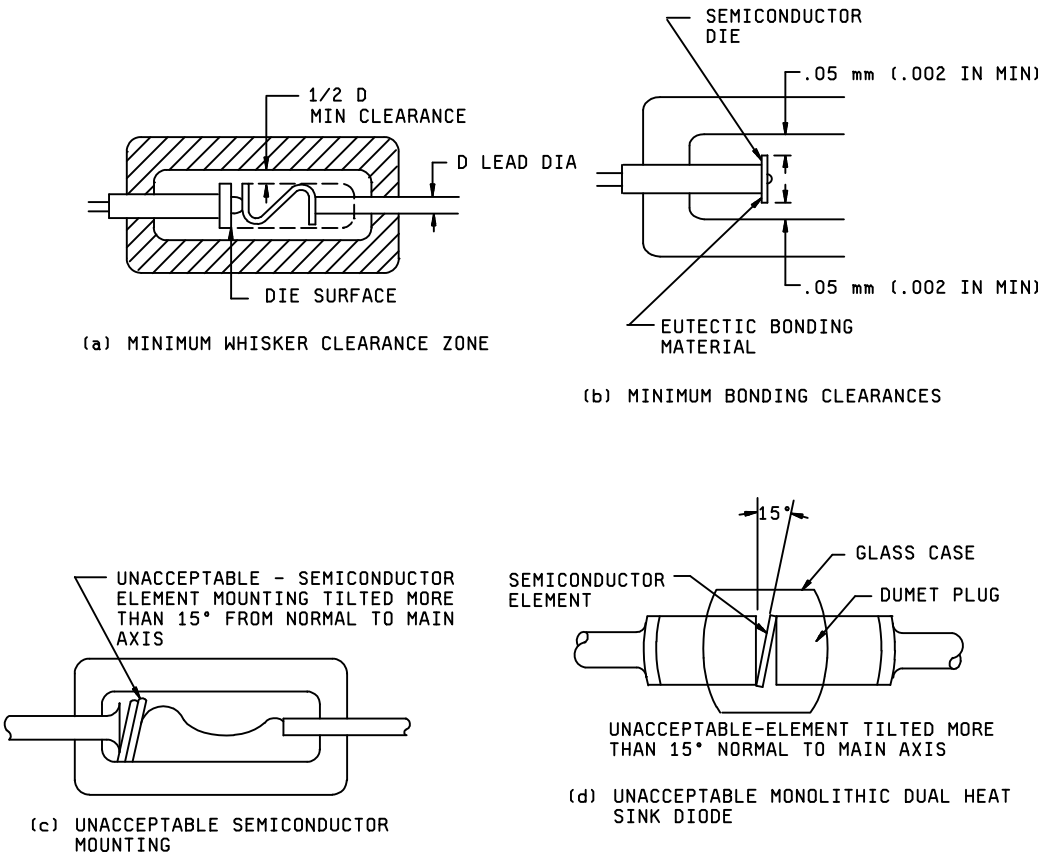

FIGURE 2012-11. Clearance in cylindrical axial lead type device.

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4. SUMMARY. The following details shall be specified in the applicable acquisition document:

4.1 Film.

a. Number of views, if other than indicated in 3.1.1.

b. Radiograph submission, if applicable (see 3.9.2).

c. Marking, if other than indicated in 3.3 and marking of samples to indicate they have been radiographed, if required (see 3.3.3).

d. Defects to be sought in the samples and criteria for acceptance or rejection, if other than indicated in 3.10 or 3.11.

e. Radiograph and report retention, if applicable (see 3.9.3).

f. Test reports when required for class level B.

4.2 Digital.

a. Number of views, if other than indicated in 3.1.1. Any requirements that cause a need for differing angle of axis, depth of view, or area of vision from those required by Film Radiography.

b. Radiograph submission, if applicable (see 3.9.2).

c. Marking, if other than indicated in 3.3 and marking of samples to indicate they have been radiographed, if required (see 3.3.3).

d. Defects to be sought in the samples and criteria for acceptance or rejection, if other than indicated in 3.10 or 3.11.

e. Radiograph and report retention, if applicable (see 3.9.3).

f. Test reports when required for class level B.

g. If Dynamic (Real Time) Radiography will be used.

h. Archiving requirements including software, recording media, image handling, and records retention period not in accordance to those specified herein.

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FEDERAL STANDARDS

Required standards:

FED-STD-595/15102 – 15123	Blue, Gloss
FED-STD-595/25102 – 25109	Blue, Semi-gloss

(Copies of these documents are available online at http://quicksearch.dla.mil.)

AMERICAN SOCIETY FOR TESTING AND MATERIALS (ASTM)

Required standards:

ASTM E 801	Standard Practice for Controlling Quality of Radiological Examination of Electronic Devices.
ASTM E 1817	Practice for Controlling Quality of Radiological Examinations by Using Representative Quality

Recommended for reference only:

ASTM E 94	Standard Guide for Radiographic Examination
ASTM E 1000	Standard Guide for Radiography.
ASTM E 1161	Standard Practice for Radiologic Examination of Semiconductors and Electronic Components
ASTM E 1255	Standard Practice for Radioscopy.
ASTM E 1316	Standard Terminology for Nondestructive Examinations
ASTM E 1411	Standard Practice for Qualification of Radioscopic Systems.
ASTM E 1742	Standard Practice for Radiographic Examination
ASTM E 1815	Standard Test Method for Classification of Film Systems for Industrial Radiography
ASTM E 2002	Standard Practice for Determining Total Unsharpness in Radiology.
ASTM E 2597	Standard Practice for Manufacturing Characterization of Digital Detector Arrays
ASTM E 2698	Standard Practice for Radiological Examination Using Digital Detector Arrays
ASTM E 2736	Standard Guide for Digital Detector Array Radiology.
ASTM E 2737	Standard Practice for Digital Detector Array Performance Evaluation and Long Term Stability.

(Copies of these documents are available online at https://www.astm.org or from the American Society for Testing and Materials, P O Box C700, 100 Barr Harbor Drive, West Conshohocken, PA 19428-2959.)

SOCIETY OF MOTION PICTURE AND TELEVISION ENGINEERS® (SMPTE®)

Recommended for reference only:

SMPTE RP 133	Specifications for Medical Diagnostic Imaging Test Pattern for Television Monitors and Hard-Copy Recording Cameras

(Copies of this document is available online at https://www.smpte.org or from the Society of Motion Picture and Television Engineers, 3 Barker Ave., 5th Floor, White Plains, NY 10601)

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NATIONAL COUNCIL ON RADIATION PROTECTION AND MEASUREMENTS (NCRP)

Recommended for reference only:

NCRP 49	Structural Shielding Design and Evaluation for Medical Use of X-Rays and Gamma-Rays up to 10 MeV
NCRP 116	Limitation of Exposure to Ionizing Radiation (Supersedes NCRP Report No. 91)
NCRP 151	Structural Shielding Design and Evaluation for Megavoltage X- and Gamma-Ray Radiotherapy Facilities

(Copies of these documents are available online at http://www.ncrponline.org or from the National Council on Radiation Protection and Measurements, NCRP Publications, 7910 Woodmont Avenue, Suite 400, Bethesda, MD 20814-3095)

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METHOD 2013.1

INTERNAL VISUAL INSPECTION FOR DPA

1. PURPOSE. This is an internal visual inspection for use in destructive physical analysis (DPA) procedures. The purpose of this destructive test is to examine devices opened for post test evaluation to verify that there is no evidence of defects or damage resulting from prior testing.

2. APPARATUS. The apparatus required for the performance of this test shall include binocular normal-incident illumination microscopes capable of 30X to 60X and 75X to 150X magnification with both light and dark field illumination, and any visual or mechanical standards to be used for measurements or comparison.

3. PROCEDURE. The device shall be opened using a technique which does not damage or contaminate the internal structure or in any way impair the ability to observe defects in the devices or the effects of preceding test exposures. The device(s) shall be examined microscopically at 30X to 60X for particles other than those produced by opening. After examination for particles is complete, the opened device(s) shall be blown off with a nominal gas blow (approximately 20 psig) to remove unattached material from the delidding process. The device shall then be microscopically examined to determine the existence of other visual defects as described in 3.1 and 3.2.

3.1 Low magnification defects (30X to 60X). No device shall be acceptable that exhibits the following defects:

a. Improper substrate or bonding post plating material.

b. Improper bond wire material or size.

c. Metallic contamination or foreign material (see method 2010).

d. Lifted or broken wires.

e. Lifted, cracked, or broken die/substrate.

f. Improper die mounting (see method 2010).

g. Excessive lead wire loop or sag (see method 2010).

h. Improper bond technique and size (see method 2010).

i. Improper assembly die location and orientation as compared to the applicable assembly drawing.

j. Particles (see method 2010) other than those introduced during opening.

3.2 High magnification defects (75X to 150X). No device shall be acceptable that exhibits the following defects:

a. Metallization voids, corrosion, peeling, lifting, blistering, or scratches (see method 2010).

b. Bond intermetallics extending radially more than 0.1 mil beyond the bond periphery in any direction.

c. Improper die or substrate metallization design layout topography or identification.

d. Die cracks (see method 2010).

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4. SUMMARY. The following details shall be specified in the applicable acquisition document:

   a. Where applicable, gauges, drawings, or photographs to be used as standards for the operator comparison (see 2).

   b. Any applicable requirements for materials, design, or construction.

   c. Requirement for photographic record, if applicable, and disposition of the photographs.

   d. Where applicable, any additions or modifications to the specified procedure and criteria.

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METHOD 2014

INTERNAL VISUAL AND MECHANICAL

1. PURPOSE. The purpose of this examination is to verify that internal materials, design and construction are in accordance with the applicable acquisition document. This test is destructive and would normally be employed on a sampling basis in qualification or quality conformance inspection of a specific device type to demonstrate compliance with the acquisition document and to reveal any undocumented changes to the part type.

2. APPARATUS. Equipment used in this examination shall be capable of demonstrating conformance to the requirements of the applicable acquisition document and shall include optical equipment capable of magnification sufficient to verify all structural features of the devices.

3. PROCEDURE. The device shall be examined under a sufficient magnification to verify that all the internal materials, design and construction are in accordance with the requirements of the applicable design documentation or other specific requirements (see 4). Specimens of constructions which do not contain an internal cavity (e.g., encapsulated or embedded devices) or those which would experience destruction of internal features of interest as a result of opening, may be obtained by interception during manufacturing prior to encapsulation. Specimens of constructions with an internal cavity shall be selected from devices which have completed all manufacturing operations and they shall be delidded or opened or both taking care to minimize damage to the areas to be inspected. When specified by the applicable acquisition document, the interception procedure may be used to obtain specimens of constructions with an internal cavity.

3.1 Photographs of die topography and intraconnection pattern. When specified, an enlarged color photograph or transparency shall be made showing the topography of elements formed on the die or substrate and the metallization pattern. This photograph shall be at a minimum magnification of 80X except that if this results in a photograph larger than 8 inches x 10 inches, the magnification may be reduced to accommodate an 8 inches x 10 inches view.

3.2 Failure criteria. Devices which fail to meet the detailed requirements for materials, design and construction shall constitute a failure.

4. SUMMARY. The following details shall be specified in the applicable acquisition document:

a. Any applicable requirements for materials, design and construction.

b. Allowance for interception procedure of internal cavity devices, when applicable (see 3).

c. Requirement for photographic record, if applicable (see 3.1), and disposition of photographs.

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METHOD 2015.14

RESISTANCE TO SOLVENTS

1. PURPOSE. The purpose of this test is to verify that the markings will not become illegible on the component parts when subjected to solvents. The solvents will not cause deleterious, mechanical or electrical damage, or deterioration of the materials or finishes.

1.1 Formulation of solvents. The formulation of solvents herein is considered typical and representative of the desired stringency as far as the usual coatings and markings are concerned. Many available solvents which could be used are either not sufficiently active, too stringent, or even dangerous to humans when in direct contact or when the fumes are inhaled.

1.2 Check for conflicts. When this test is referenced, care should be exercised to assure that conflicting requirements, as far as the properties of the specified finishes and markings are concerned, are not invoked.

2. MATERIALS.

2.1 Solvent solutions. The solvent solutions used in this test shall consist of the following: 1/

a. At 20-30°C a mixture consisting of the following:

(1) One part by volume of an aliphatic alcohol and/or aliphatic ester, USP grade or better.

(2) Three parts by volume of mineral spirits in accordance with MIL-PRF-680, type II, previously designated as TT-T-291, type II, grade A, or three parts by volume of a mixture of 80 percent by volume of kerosene and 20 percent by volume of ethylbenzene.

b. A semiaqueous or nonaqueous based organic solvent e.g., a terpene or heterocyclic compound. 2/

c. This solvent has been deleted. When a suitable replacement for this solvent has been found, it will be added as solution c.

d. At 63°C to 70°C, a mixture consisting of the following: 1/

(1) 42 parts by volume of deionized water.

(2) 1 part by volume of propylene glycol monomethyl ether.

(3) 1 part by volume of monoethanolamine or equivalent inorganic base to achieve the same pH.

2.1.1 Solvent solutions, safety aspects. Solvent solutions listed in a through d above exhibit some potential for health and safety hazards. The following safety precautions should be observed:

a. Avoid contact with eyes.

b. Avoid prolonged contact with skin.

c. Provide adequate ventilation.

d. Avoid open flame.

e. Avoid contact with very hot surfaces.

1/ Normal safety precautions for handling these solutions (e.g., same as those for diluted ammonium hydroxide) based on OSHA rules for Monoethanolamine or other precautionary measures with regard to flash point, toxicity, etc.

2/ Or any EPA demonstrated equivalent. When using EPA approved alternative solutions for test, the device manufacturer should consider the recommended temperature for cleaning specified by the solvent supplier.

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2.2 Vessel. The vessel shall be a container made of inert material, and of sufficient size to permit complete immersion of the specimens in the solvent solutions specified in 2.1.

2.3 Brush. The brush shall be a toothbrush with a handle made of a nonreactive material. The brush shall have at least three long rows of hard (or firm) bristles, the free ends of which shall lie substantially in the same plane. The toothbrush shall be used exclusively with a single solvent and when there is any evidence of softening, bending, wear, or loss of bristles, it shall be discarded.

3. PROCEDURE. The specimens subjected to this test shall be divided into three equal groups. Each group shall be individually subjected to one of the following procedures:

Note: Metal lidded leadless chip carrier (LCC) packages shall be preconditioned by immersing the specimens in room temperature flux type symbols “A” or “B” (flux types “LO” or “L1”) in accordance with IPC J-STD-004 previously designated as RMA flux in accordance with MIL-F-14256, for 5 to 10 seconds. The specimens shall then be subjected to an ambient temperature of 215 °C ±5°C for 60 seconds +5, -0 seconds. After the preconditioning, each device lid shall be cleaned with isopropyl alcohol.

a. The first group shall be subjected to the solvent solution as specified in 2.1a maintained at a temperature of 25°C ±5°C.

b. The second group shall be subjected to the solvent solution as specified in 2.1b maintained at a suitable temperature.

c. This solution has been deleted, (see 2.1c).

d. The fourth group shall be subjected to the solvent solution as specified in 2.1d maintained at a temperature of 63°C to 70°C.

The specimens and the bristle portion of the brush shall be completely immersed for 1 minute minimum in the specified solution contained in the vessel specified in 2.2. Immediately following emersion, the specimen shall be brushed with normal hand pressure (approximately 2 to 3 ounces) for 10 strokes on the portion of the specimen where marking has been applied, with the brush specified in 2.3. Immediately after brushing, the above procedure shall be repeated two additional times, for a total of three immersions followed by brushings. The brush stroke shall be directed in a forward direction, across the surface of the specimen being tested. After completion of the third immersion and brushing, devices shall be rinsed and all surfaces air blown dry. After 5 minutes, the specimens shall be examined to determine the extent, if any, of deterioration that was incurred.

3.1 Optional procedure for the fourth group. The test specimens shall be located on a test surface of known area which is located 15 ±2.5 centimeters (6 ±1 inches) below a spray nozzle(s) which discharges 0.6 ±0.02 liters/minute (0.139 gpm) of solution (2.1d) per 6.5 square centimeters (1 in^2)surface area at a pressure of 140 ±30 kilopascal (20 ±5 psi). The specimens shall be subjected to this spray for a period of 10 minutes minimum. After removal and within 5 minutes the specimens shall be examined in accordance with 3.1.1. The specimens may be rinsed with clear water and air blow dried prior to examination.

3.1.1 Failure criteria. After subjection to the test, evidence of damage to the device and any specified markings which are missing in whole or in part, faded, smeared, blurred, or shifted (dislodged) to the extent that they cannot be readily identified from a distance of at least 15.0 cm (6 inches) with normal room lighting and without the aid of magnification or with a viewer having a magnification no greater than 3X shall constitute a failure.

4. SUMMARY. The following detail shall be specified in the individual specification: The number of specimens to be tested (see 3).

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METHOD 2016

PHYSICAL DIMENSIONS

1. PURPOSE. The purpose of this examination is to verify that the external physical dimensions of the device are in accordance with the applicable acquisition document.

2. APPARATUS. Equipment used in this examination shall include micrometers, calipers, gauges, contour projectors, or other measuring equipment capable of determining the actual device dimensions specified in the applicable acquisition document.

3. PROCEDURE. Unless otherwise specified, the physical dimensions on the case outline drawing shall be measured.

3.1 Failure criteria. Any device which exhibits a dimension or dimensions outside the specified tolerances or limits shall constitute a failure.

4. SUMMARY. The following detail shall be specified in the applicable acquisition document:

External dimensions which are capable of physically describing the device (see 3). Dimensions to be considered shall include case outline dimensions; special lead shapes (e.g., required bend positions, angles of bend), where applicable; dimensions of any projecting or indented features used for coding of lead arrangement, automatic handling and similar purpose; and any other information which affects the installed size or orientation of the device in normal applications.

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METHOD 2017.13

INTERNAL VISUAL (HYBRID)

1. PURPOSE. The purpose of this test is to visually inspect the internal materials, construction, and workmanship of hybrid, multichip and multichip module microcircuits.

1.1 Scope. This test is for both Class H (Class level B) and Class K (Class level S) quality levels, Surface Acoustic Wave (SAW) and hybrid/multichip/multichip module microcircuits. The following types of microcircuits may be inspected:

a. Passive thin and thick film networks.

b. Active thin and thick film circuits.

c. Multiple circuits, including combinations, stacking or other interconnections of 1.1.a and 1.1.b.

This test is performed on microelectronic devices after completion of all assembly operations, prior to seal, encapsulation, or final acceptance on a 100 percent inspection basis (or as specified in controlling documents) to detect and eliminate devices with one or more internal defects. It may also be employed as an in-process inspection on a sampling basis to determine the effectiveness of the manufacturing processes and handling procedures.

2. APPARATUS. The apparatus for this test shall include optical equipment capable of the specified magnification(s) and visual standards/aids (gages, drawings, photographs, etc.) necessary to perform an effective examination and enable the operator to make objective decisions as to the acceptability of the device being examined. Fixtures, if needed, shall be provided for handling devices during examination to promote efficient operation without inflicting damage to the units.

3. PROCEDURE.

a. General. The device shall be examined in a suitable sequence of observations within the specified magnification range to determine compliance with the specified test condition. Devices may be examined at any magnification within the specified range for each criterion. However, the product must be capable of passing each criterion at all magnifications within that criterions specified range. The inspection criteria shall include all criteria of this test method and the applicable test methods referenced in paragraph 3.1.1. For Class H hybrids, the inspection criteria of 3.1.1 may be performed prior to element attachment, at the option of the manufacturer. For Class K hybrids, the inspection criteria of 3.1.1 shall be employed following element attachment and wirebonding, or at final preseal inspection.

b. Sequence of inspection. The order in which criteria are presented is not the required order of examination and may be varied. Where obscuring mounting techniques (e.g., beam lead devices, stacked substrates, components mounting in holes or cutaways, flip chip devices, packaged devices) are employed, the inspection criteria contained herein that cannot be performed after mounting shall be conducted prior to mounting the element or substrate. However, unless obscuring mounting techniques (e.g., beam lead devices, stacked substrates, components mounting in holes or cutaways, flip chip devices, packaged devices) are employed, only in these cases, the obscured details shall be compliant to section 3.1 at the last operation before the details become obscured.

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c. Inspection control. In all cases, examination prior to final preseal inspection shall be performed under the same quality program that is required at the final preseal inspection station. Care shall be exercised after inspections (see 3.b), to ensure that defects created during subsequent handling will be detected and rejected at final preseal inspection. Devices examined to 3.1 criteria shall be inspected and prepared for sealing in a 100,000 (0.5 µm or greater) particles/cubic foot controlled environment (class 8 of ISO 14644-1) for Class H and 100 (0.5 µm or greater) particles/cubic foot controlled environment (class 5 of ISO 14644-1) for Class K, except that the allowable relative humidity shall be less than 65 percent. During the time interval between internal visual inspection and preparation for sealing, devices shall be stored in a 1000 (0.5 µm or greater) particles/cubic foot controlled environment (class 6 of ISO 14644-1). Devices shall be in covered containers when transferred from one controlled environment to another.

d. Re-inspection. When inspection for product acceptance or quality verification of the visual requirements herein is conducted subsequent to the manufacturer's successful inspection, the additional inspection may be performed at any magnification specified by the applicable test condition, unless a specific magnification is required by the acquisition document. Where sample inspection is used rather than 100 percent re-inspection, the sampling plans of MIL-PRF-38534 or Appendix A of MIL-PRF-38535 shall apply.

e. Exclusions. Where conditional exclusions have been allowed, specific instruction as to the location and conditions for which the exclusion can be applied shall be documented in the assembly inspection drawing.

f. Definitions.

(1) Active circuit area includes all areas of functional circuit elements, operating metallization or connected combinations thereof excluding beam leads.

(2) Add-on substrate is a supporting structural material into and/or upon which glassivation, metallization and circuit elements are placed and the entire assembly is in turn placed on, and attached to the main substrate.

(3) Adhesive is a polymeric mixture that bonds elements together. It may be filled with conductive or non-conductive particles.

(4) Attachment media is defined as the material used to effect the attachment of an element to an underlying surface (e.g., adhesive, solder, braze, or other eutectic material system).

(5) Bonding site is a metallized area on a substrate or element intended for a wire or ribbon interconnecting bond.

(6) Cold solder joint is defined as a solder joint whose appearance is "grainy" or "dull". Where a "grainy" or "dull" appearance is characteristic of certain solder materials (e.g., AuSn, etc.), this criteria shall not be rejectable for these materials.

(7) Compound bond is one bond, of any type on top of another bond of any type on an element. For example, ball on top of a ball.

(8) Conductive attach is the process and materials used for the attachment that also provides an electrical contact or thermal dissipation path (e.g., solder, eutectic, conductive epoxy).

(9) Crack is a separation in the mounting material that is measurable in length, width and depth. It is not pullback of the fillet or shrinkage due to the curing process.

(10) Dendrites form in fern-like or snowflake-like patterns growing along a surface (x-y plane) rather than outward from it. The growth mechanism for dendrites requires some type of moisture capable of dissolving the metal (e.g., tin) into a solution of metal ions which are then redistributed by electromigration in the presence of an electromagnetic field.

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(11) Dielectric attach is the process and materials used for attachment that does not provide electrical contact or thermal dissipation considerations.

(12) Edge metallization is the metallization that electrically connects the metallization from the top surface to the opposite side of the substrate; also called wrap around metallization.

(13) Element is a constituent of a hybrid microcircuit; such as integral deposited or screened passive elements, substrates, discrete or integrated electronic parts including dice, chips and other micro-components; also mechanical piece parts as cases and covers; all contributing to the operation of a hybrid microcircuit.

(14) Electrically common is satisfied when two or more conductive surfaces or interconnects are of equal DC voltage/signal potential.

(15) End terminated or wrap around elements are those elements which have electrical connections on the ends (sides) and/or bottom of their bodies.

(16) Eutectic is a mixture of two or more metals in such proportion that their combined melting point is the lowest attainable. At the eutectic, the solidus and liquidus temperatures on the equilibrium phase diagram are the same. For example: AuSi eutectic M.P. = 363 C.

(17) Fissure is a hair-line fracture that does not have significant measurable dimension. For example; a fissure may be several mils in length but would not have a measurable width or depth.

(18) Foreign material is defined as any material that is foreign to the microcircuit or any non-foreign material that is displaced from its original or intended position within the microcircuit package. Conductive foreign material is defined as any substance that appears opaque under those conditions of lighting and magnification used in routine visual inspection. Particles shall be considered embedded in glassivation when there is evidence of color fringing around the periphery of the particle.

(19) Glassivation is the top layer(s) of transparent insulating material that covers the active area including metallization, except bonding pads and beam leads.

(20) Insulating layer is a dielectric layer used to isolate single or multilevel conductive and resistive material or to protect top level conductive and resistive material.

(21) Intermetallics (Purple Plague) is one of several gold-aluminum compounds formed when bonding gold to aluminum and activated by re-exposure to moisture and high temperature (>340°C). Purple plague is purplish in color and is very brittle, potentially leading to time-based failure of the bonds. Its growth is highly enhanced by the presence of silicon to form ternary compounds.

(22) Mechanical strength tests are tests, such as Mechanical Shock or Constant Acceleration, which demonstrate adequate attachment process and materials.

(23) Non-monometallic compound bond consists of two lead bonds, made of dissimilar metals, which are stacked one on top of the other (i.e., the interface between the two lead bonds are made up of dissimilar metals such as an aluminum lead bond stacked on top of a gold lead bond or vice-versa).

(24) Operating metallization (conductors) is all metal or any other material used for interconnections except metallized scribe lines, test patterns, unconnected functional circuit elements, unused bonding pads and identification markings.

(25) Original design separation is the separation dimension or distance that is intended by design.

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(26) Original width is the width dimension or distance that is intended by design (i.e., original metal width, original diffusion width, original beam width, etc.).

(27) Passivation is the silicon oxide, nitride, or other insulating material that is grown or deposited directly on the die prior to the deposition of the final metal layers.

(28) Reinforcement Bond is a ball placed on the heel of a tailless or crescent bond intended to reinforce the initial bond. A reinforcement bond is a type of compound bond.

(29) Security Bond is also known as a reinforcement bond.

(30) Separation barrier is non-conductive adhesive deposited between end terminations and is designed to improve the strength of the element attach and separate the conductive adhesive applied to the end terminations.

(31) Surface Acoustic Wave (SAW) element is a planar element fabricated typically using thin film manufacturing techniques on various substrate materials. Size varies as a function of frequency and design features include interdigitated fingers.

(32) String is a filamentary run-out or whisker of polymer material.

(33) Substrate is the supporting structural material into and/or upon which the passivation, metallization, and circuit elements are placed.

(34) Tuning is the adjustment of signals from an RF/Microwave circuit by altering lines or pads; adding, deleting or manipulating wires/ribbons; and/or changing resistance, inductance or capacitance values to meet specific electrical specifications.

(35) Through hole metallization is the metallization that electrically connects the metallization on the top surface of the substrate to the opposite surface of the substrate.

(36) Thermocompression bond is a wirebond interconnect formed using heat and pressure.

(37) Thermosonic bond is a wirebond interconnect formed using heat, pressure and ultrasonic energy.

(38) Ultrasonic bond is a bond formed with pressure and ultrasonic energy with no added heat.

(39) Unused component or unused deposited element is one not connected to a circuit or connected to a circuit path at one and only one point. A connection may be made by design or by visual anomaly.

(40) Void is any region in a material (interconnects, bonding sites, etc.) where an underlying material is exposed and it was not caused by a scratch.

(41) Visible line is defined as 0.5 mil at 60X magnification.

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(42) Whisker is a spontaneous columnar or cylindrical filament, usually of monocrystalline metal, emanating from the surface of a finish.

NOTE: For the purpose of this document, whiskers have the following characteristics:

- An aspect ratio (length/width) greater than 2
- Can be kinked, bent, or twisted
- Usually have a uniform cross-section shape
- May have striations along the length of the column and or rings around the circumference of the column
- Length of 10 microns or more. Features less than 10 microns may be deemed important for research but are not considered significant for this test method.

(43) Whisker Length is the straight line distance from the point of emergence of the whisker to the distant point on the whisker (i.e., the radius of a sphere containing the whisker with its center located at the point of emergence.

g. Interpretations. References herein to "that exhibits" shall be considered satisfied when the visual image or visual appearance of the device under examination indicates a specific condition is present and shall not require confirmation by any other method of testing. When other methods of test are to be used to confirm that a reject condition does not exist, they shall be approved by the acquiring activity.

h. Foreign material control. The manufacturer shall perform an audit on a weekly basis for the presence of foreign material on the die surface, or within the package. This audit may be satisfied during routine internal visual inspection. If the presence of any type of foreign material/contamination is discovered, the manufacturer shall perform the necessary analysis to determine the nature of the foreign material. The manufacturer shall document the results of the investigation and corrective actions taken. The intent of this procedure is to require investigation and resolution of foreign material/contamination problems which do not have effective screening or detection methodology, but that could cause degradation and eventual failure of the device function. Repetitive findings without obvious improvements require escalation to Director of Manufacturing and Director of Quality before processing.

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3.1 Examination. Internal visual examination as required in 3.1.1 through 3.1.9 shall be conducted on each SAW, hybrid/multichip microcircuit, or microwave hybrid microcircuit. The magnifications required for each inspection shall be those identified in the particular test method used (i.e., 2010, 2017, or 2032 of MIL-STD-883 and 2069, 2070, 2072, or 2073 of MIL-STD-750).

3.1.1 Active and passive elements. All integrated circuit elements shall be examined in accordance with MIL-STD-883, method 2010.

Method 2010; Paragraph 3.1.1: Metallization defects.

Method 2010; Paragraph 3.1.2: Diffusion and passivation layer(s) faults.

Method 2010; Paragraph 3.1.3: Scribing and die defects.

Method 2010; Paragraph 3.2.5: Foreign material.

Method 2010; Paragraph 3.1.4: Glassivation defects.

Method 2010; Paragraph 3.1.6: Film resistors defects.

Method 2010; Paragraph 3.1.7: Laser trimmed film resistor defects.

Method 2010; Paragraph 3.2.1.6: Flip chip solder bump die.

Transistor, diode, power MOS FET and microwave transistor elements shall be examined in accordance with the identified paragraphs of MIL-STD-750, methods 2069, 2070, 2072 and 2073 as indicated in table I. below. Passive elements (including substrates) shall be examined in accordance with MIL-STD-883, method 2032.

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Table I. Element test method paragraph references.

Visual Inspection	MIL-STD-750 Method 2069 Pre-cap Visual Power MOSFET's	MIL-STD-750 Method 2070 Pre-cap Visual Microwave Discrete and Multichip Transistors	MIL-STD-750 Method 2072 Internal Visual Transistor Pre-cap Inspection	MIL-STD-750 Method 2073 Internal Inspection for die (semiconductor diodes)	MIL-STD-883 Method 2010 Internal Visual Monolithic
Die Metallization Defects	3.4.1, 3.4.2, 3.4.3, 3.4.4, 3.4.5, 3.4.6	3.2.1, 3.3	4.1.1	4.1.1	3.1.1
Diffusion and Passivation Layer(s)	3.4.7	3.8, 3.9.4, 3.9.5	4.1.2	4.1.1	3.1.2
Scribing and Die Defects	3.4.8	3.4	4.1.3	4.1.1	3.1.3
Glassivation	3.4.9	3.2.2	4.1.7	N/A	3.1.4
Foreign Material	3.3.1	3.6.1	4.1.6	4.3	3.2.5

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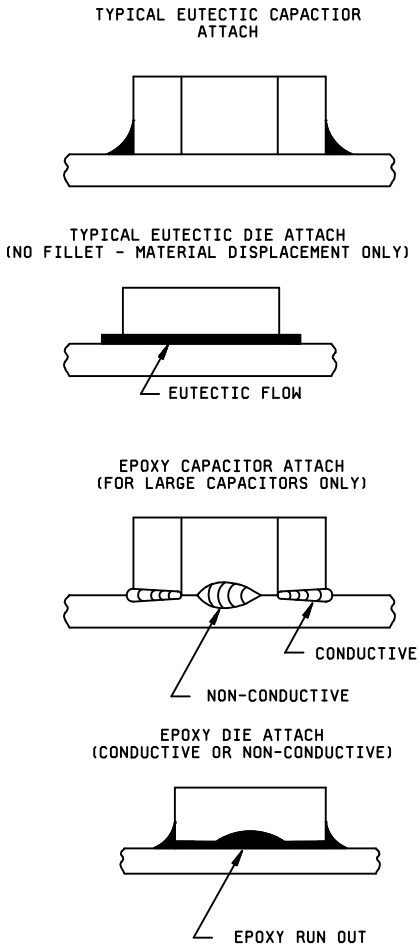
3.1.2 Element attachment (assembly), "magnification 10X to 60X". Figures 2017-1 and 2017-2 are example visual representations of attachment media types.

NOTE: Rejection criteria are not to be derived from these examples but rather from the specific criteria paragraphs that follow.



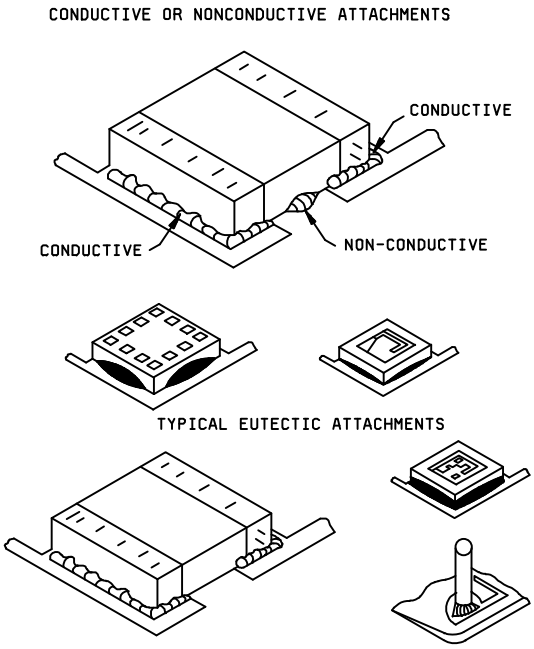


FIGURE 2017-1. Element attachments. (Side view)

FIGURE 2017-2. Element attachments. (Tilted view)

NOTE: Ultrasonic Inspection (TM 2030) or Radiography (TM 2012) may be used to verify attachment in lieu of visual criteria. If so the maximum void acceptance criteria specified in TM 2012 or TM 2030 shall not be exceeded.

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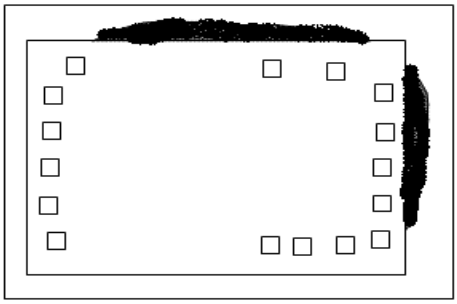
3.1.2.1 Element mounting adhesive. No device shall be acceptable that exhibits:

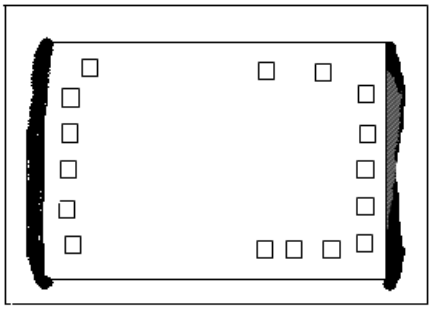
NOTE: The criteria of paragraph 3.1.2.1.a and b shall not apply when attachment adhesive is applied directly to more than 75 percent of the element attach area by use of a controlled process (such as utilizing preforms, screen printing or automated dispense).

a. For non-end terminated elements, attachment adhesives not visible around at least 50 percent of the element's perimeter unless it is continuous on two full nonadjacent sides of the element (see Figures 2017-3 and 4).



Reject less than 50% of perimeter

Figure 2017-3



Minimum Accept two full non-adjacent sides

Figure 2017-4

b. Glass substrates or transparent die, when viewed from the top or bottom, which exhibits attach area coverage less than 75 percent.

NOTE: This criterion may be employed in lieu of 3.1.2.1.a.

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c. End terminated elements that do not have adhesive attachment to bonding pads that is visible around at least 75 percent of each end termination (see Figures 2017-5, 2017-6 and 2017-7).

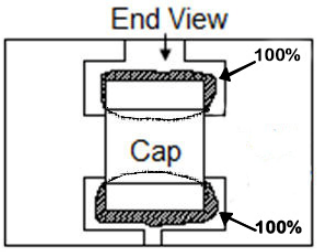

Figure 2017-5

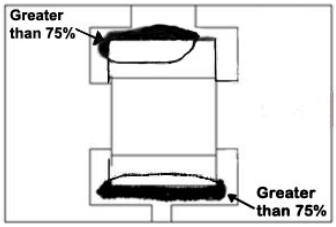

Figure 2017-6

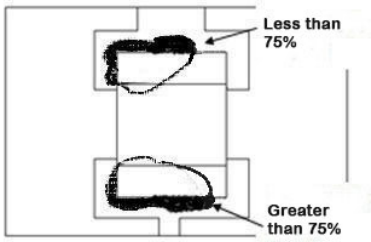

Figure 2017-7

d. Evidence of conductive adhesive under the body of the element that reduces the spacing between attached metallization by more than 50% as viewed from the side (this applies whether or not staking adhesive is used).

NOTE: For end terminated elements with added staking adhesive designed as a separation barrier the staking material must clearly attach to the body of the element. (see Figure 2017-8).

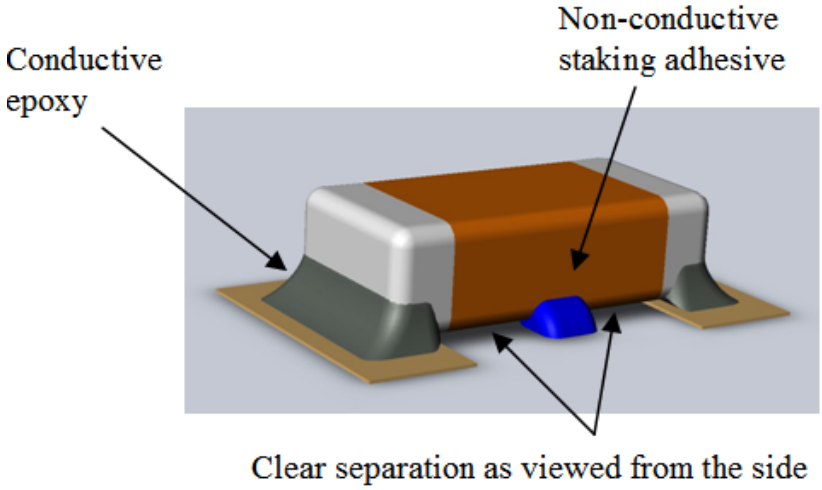

Figure 2017-8. Example of end terminated elements with staking.

e. Flaking, peeling, or lifting of the attachment adhesive material.

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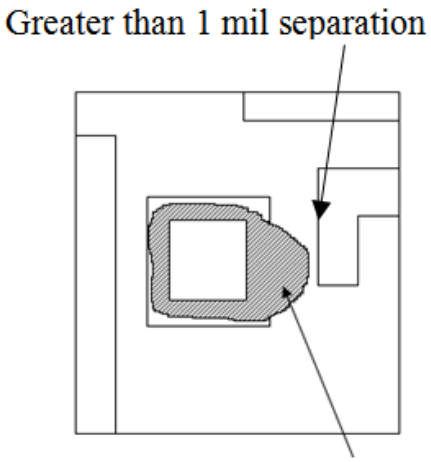
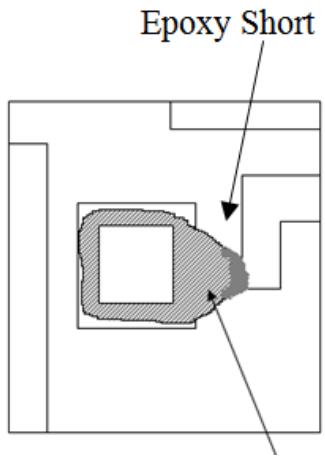
f. Die mounting adhesive that extends onto the top surface or extends vertically above the top surface of the die.

g. Conductive attachment adhesive or resin which comes closer than 1.0 mil to any functional metallization or element which is not electrically common (see Figure 2017-9 and 10).



Accept adhesive or resin not shorted

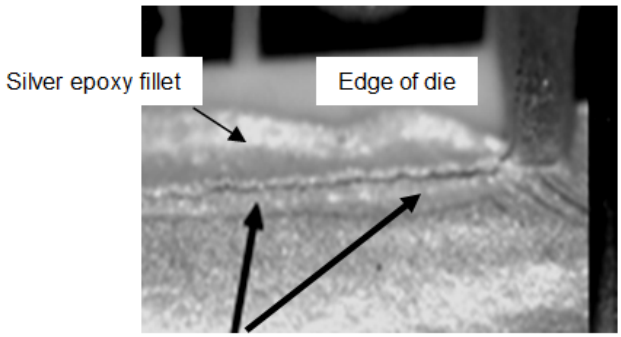
Figure 2017-9



Reject adhesive or resin short

Figure 2017-10

h. Any crack in the surface of the attachment adhesive greater than 5.0 mils in length or 10 percent of the contact periphery (see Figure 2017-11).



Reject crack in the mounting material

Figure 2017-11

NOTE: Irregularities such as fissures or pullback at the edges of the adhesive are not considered cracks (see Figure 2017-11a).

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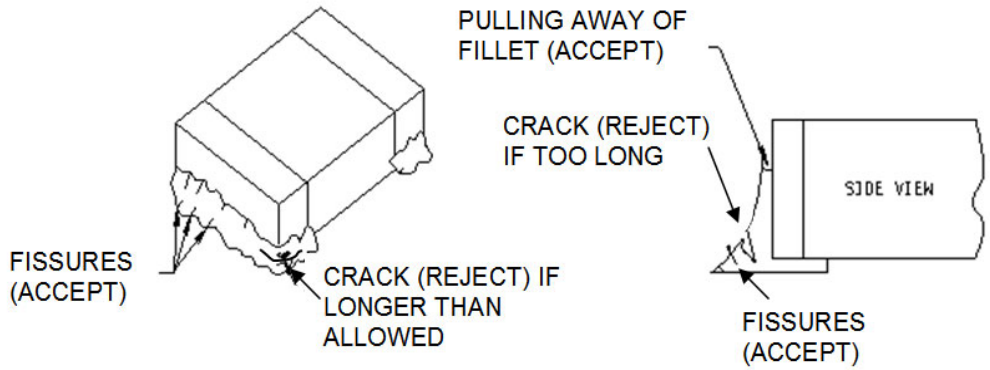

Figure 2017-11a.

i. Adhesive strings where the diameter of the string at the point of attachment is less than 50 percent of the maximum length of the string (see Figure 2017-11b).

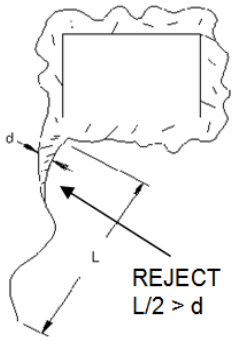

FIGURE 2017-11b. Adhesive String Criteria.

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3.1.2.2 Element mounting eutectic and solder. No device shall be acceptable that exhibits:

NOTE: As a guide and for further information about solder related defects refer to IPC-STD-610 Class 3.

a. Die mounting material buildup that extends onto the top surface, or extends vertically above the top surface of the die, or comes closer than 1.0 mil to any functional metallization or element which is not electrically common.

b. Die mounting attachment material not visible around at least 50 percent of the element's perimeter unless it is continuous on two full nonadjacent sides of the element; except for transparent die (refer to section 3.1.2.1.a).

c. Glass substrates or transparent die, when viewed from the bottom, which exhibits an attach area less than 75 percent.

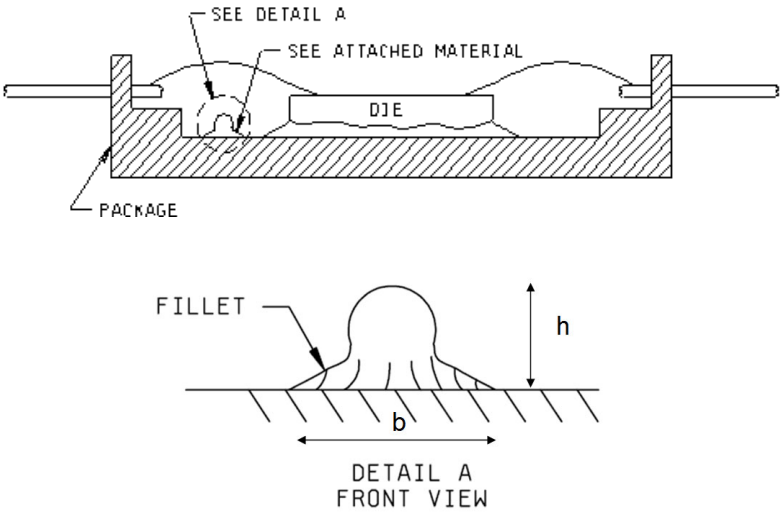
d. Cold solder joint.

e. Fractured solder connections.

f. Solder bridging except by design.

g. Flaking of the eutectic or solder mounting material.

h. Balling of the eutectic or solder mount material that does not exhibit a minimum of 50 percent peripheral fillet when viewed from above or the accumulation of material is such that the height of the accumulation is greater than the longest base dimension or the accumulation necks down at any point (see figure 2017-12 a & b).



Reject if h>b

Figure 2017-12a.

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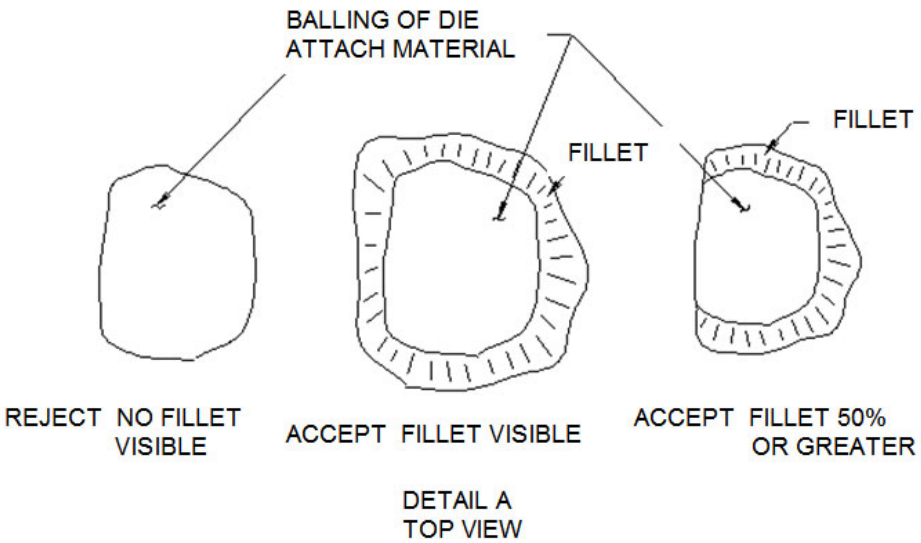
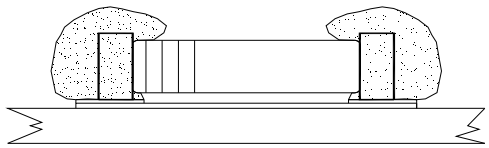


Figure 2017-12b.

i. Solder or eutectic material that extends beyond the intended attach pad or extends above the top plane of the element. (see Figure 2017-13 a and b)



Reject: Build-up of the solder or eutectic attach material above the top plane of the element

Figure 2017-13a.

Acceptable fillet

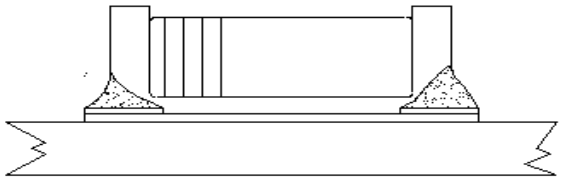


Figure 2017-13b.

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3.1.3 Substrate mounting. No device shall be acceptable that exhibits:

a. Substrate attachment material not visible around at least 50 percent of the element's perimeter unless it is continuous on two full nonadjacent sides of the element, except for transparent die (refer to section 3.1.2.1.a).

NOTE: The criteria of paragraph 3.1.3.a shall not apply when attachment media is applied directly to more than 75 percent of the substrate attach area by use of a method such as preforms or printing.

b. Conductive attachment media which comes closer than 1.0 mil to any functional metallization (e.g. post) or element which is not electrically common.

c. Conductive attachment media buildup that extends onto the top substrate surface and comes closer than 1.0 mil to any element or conductor which is not electrically common.

3.1.4 Element orientation. No device shall be acceptable that exhibits:

a. Element not located or oriented in accordance with the applicable assembly drawing of the device, which would affect the device performance or reliability.

NOTE: Elements whose bond and electrical configuration is symmetrical may be rotated unless otherwise stated in the assembly drawings. (see Figure 2017-14)

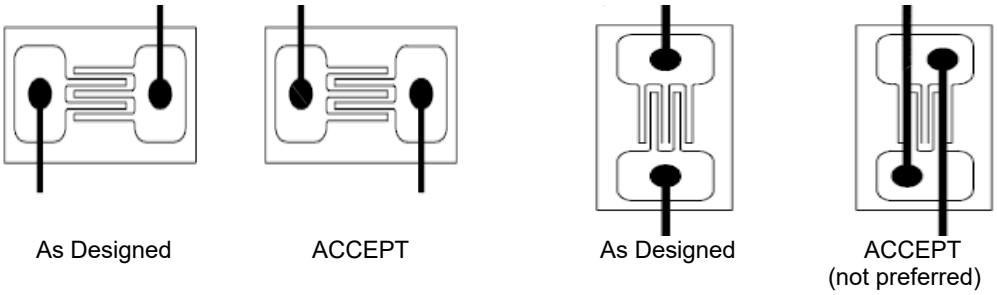

Figure 2017-14. Acceptable Symmetrical Element Orientation.

b. Elements that overhang the edge of the substrate.

c. Clearance less than 1.0 mil between any un-insulated portion of the element and any non-common conductive surface.

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3.1.5 Bond inspection, magnification 30X to 60X. This inspection and criteria shall be the required inspection for the bond type(s) and location(s) to which they are applicable when viewed from above.

Note: Wire tail shall not be considered part of the bond when determining physical bond dimensions.

3.1.5.1 Ball bonds. No device shall be acceptable that exhibits:

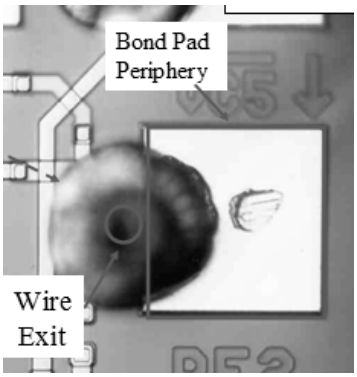
a. Ball bond diameter less than 2.0 times or greater than 5.0 times the wire diameter.

b. Ball bonds where the wire exit is not completely within the periphery of the ball (see Figure 2017-15a).

Reject wire exit not within periphery of ball

Figure 2017-15a.

c. Ball bonds where the wire center exit is not within the boundaries of the bonding site (see Figure 2017-15b).



Reject: wire center exit not within boundary of bond pad.
Additionally, reject because ball is shorted to adjacent metal run.

Figure 2017-15b.

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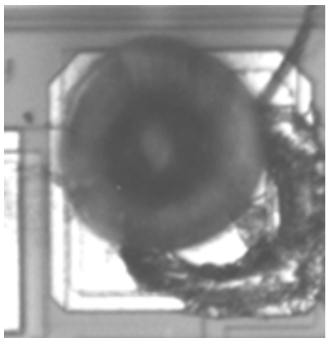
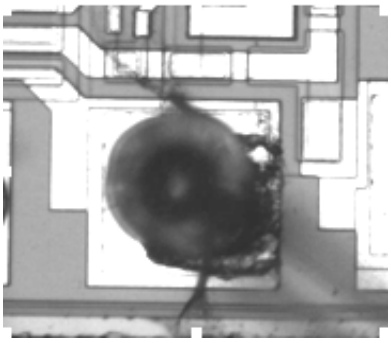
d. Ball bonds where the ball is placed on more than 50% disturbed metal (see Figure 2017-15 c and d).



Accept
ball on <50% disturbed metal

Figure 2017-15c.



Reject
ball on >50% disturbed metal

Figure 2017-15d.

3.1.5.2 Tailless bond (crescent). No device shall be acceptable that exhibits:

NOTE: The dimensions of an acceptable gold crescent or tailless bond are shown in Figure 2017-16a.

a. Tailless bonds that are less than 1.2 times or greater than 5.0 times the wire diameter in width (see Figure 2017-16b).

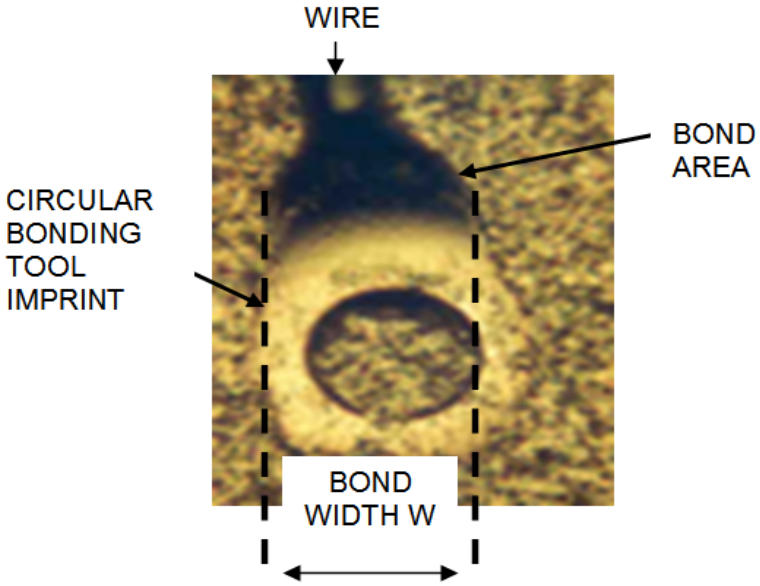


Figure 2017-16a. Tailless (crescent) Bond Dimensions.

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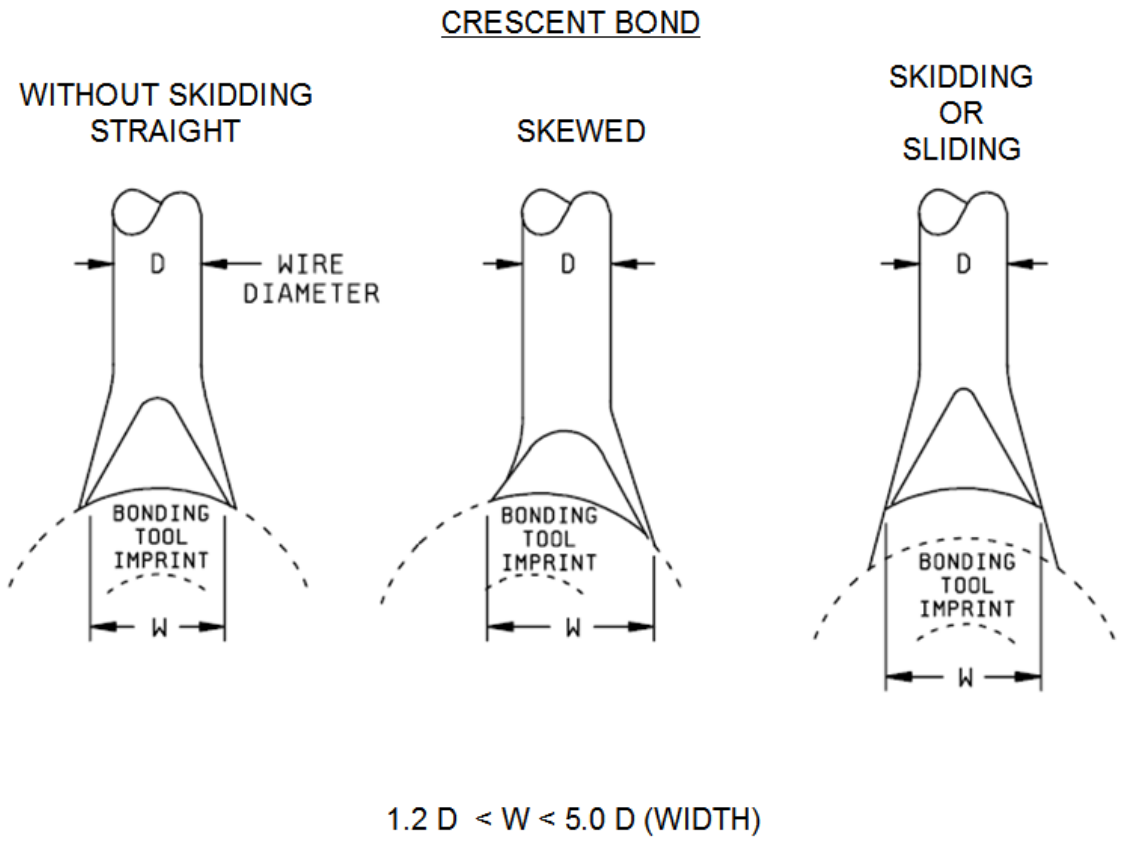

Figure 2017-16b. Tailless Bond Criteria.

b. A tailless bond of a gold wire bonded on the aluminum pads of a die.

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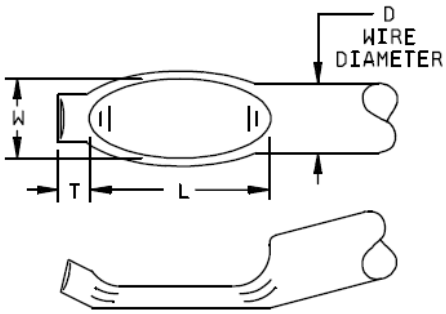
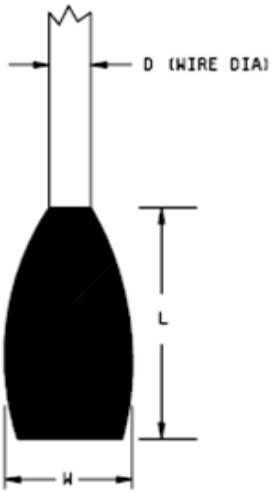
3.1.5.3 Wire wedge bonds. No device shall be acceptable that exhibits:

a. Fine wire criteria (4 mils or less wire diameter): Ultrasonic, thermosonic and thermocompression bonds that are less than 1.2 times or greater than 2.0 times the wire diameter in width or less than 0.5 times the wire diameter in length or no evidence of tool impression (see Figure 2017-16a).

b. Heavy wire criteria (greater than 4 mils diameter): Ultrasonic aluminum bonds that are less than 1.0 times or greater than 2.0 times the wire diameter in width or less than 0.5 times the wire diameter in length or no evidence of tool impression.



Wedge Bond
First bond (with tail)



Wedge Bond
Second bond (no tail)

Figure 2017-16a. Bond Dimensions.

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3.1.5.4 Compound bonds including reinforcement/security bonds (ball on crescent). No device shall be acceptable that exhibits the following:

NOTE: For both compound bonds and reinforcement bonds; broken or lifted bonds as a result of electrical troubleshooting or tuning shall be considered rework and shall not apply to the 10 percent repair limitation.

a. More than one bond on top of original bond including a second ball bond on top of a reinforcement ball.

b. Where the contact area of the second bond is less than 75 percent of the bond area of the original bottom bond.

c. Non-monometallic compound bond (i.e., between dissimilar metals) excluding the bond pad metallization.

d. One reinforcement bond used to secure two common wires (see Figure 2017-17).

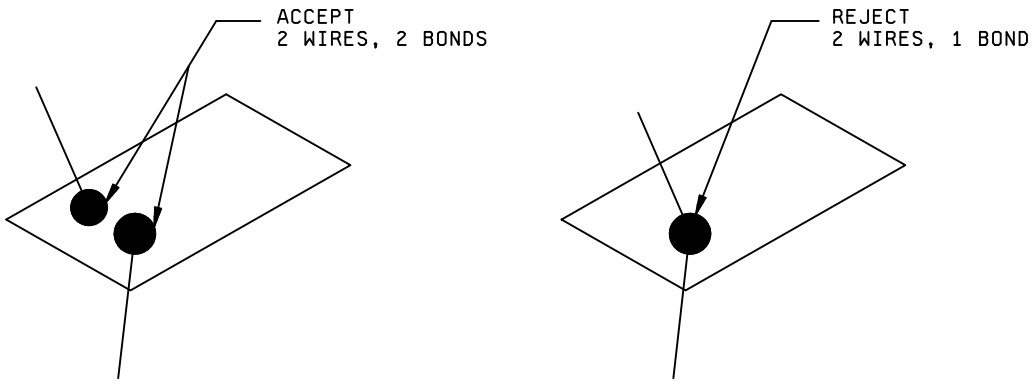

FIGURE 2017-17. One bond to secure two common wires.

3.1.5.5 Beam lead. This inspection and criteria shall apply to the completed bond area made using direct tool contact. No device shall be acceptable that exhibits:

a. Bonds which do not exhibit 75 percent bond/weld impression(s) across the width of the beam lead.

NOTE: Gaps between bonds/welds on the beam lead caused by the natural footprint of a bond/weld tip (i.e., split tip, tool on a gap welder, etc.), are acceptable provided the total of all gaps does not exceed 25 percent of the beam lead width.

b. Complete or partial beam separation from the die.

c. Bonds on the substrate where the tool impression is not visible on the beam.

d. Beam lead width increased by greater than 50 percent of the original beam width.

e. Bonding tool impression less than 1.0 mil from the die edge (see Figure 2017-18a).

f. An absence of visible separation between the bond and the edge of the passivation layer (see Figure 2017-18a).

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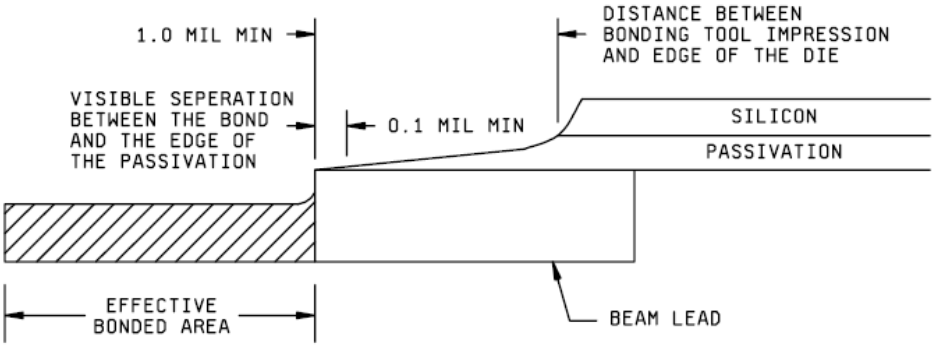

Figure 2017-18a. Beam lead area and location (side view).

g. Bonds where the tool impression length is less than 1.0 mil (see Figure 2017-18b).

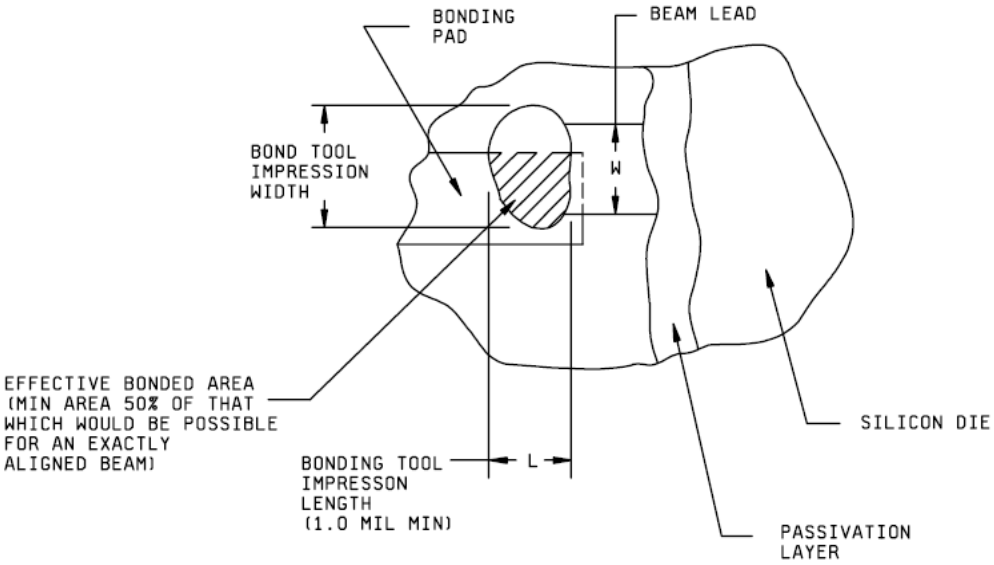

Figure 2017-18b. Beam lead area and location (top down view).

h. Effective bonded area less than 50 percent of that which would be possible for an exactly aligned beam (see Figure 2017-18b).

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i. Any tears in the beam lead between the bond junction nearest the die body and the die or in the bonded area of the beam lead within a distance equal to 50 percent the beam width (see Figure 2017-19).

j. An absence of visible separation between a beam lead and non-electrically common metallization. This criteria applies for both glassivated and unglassivated metallization.

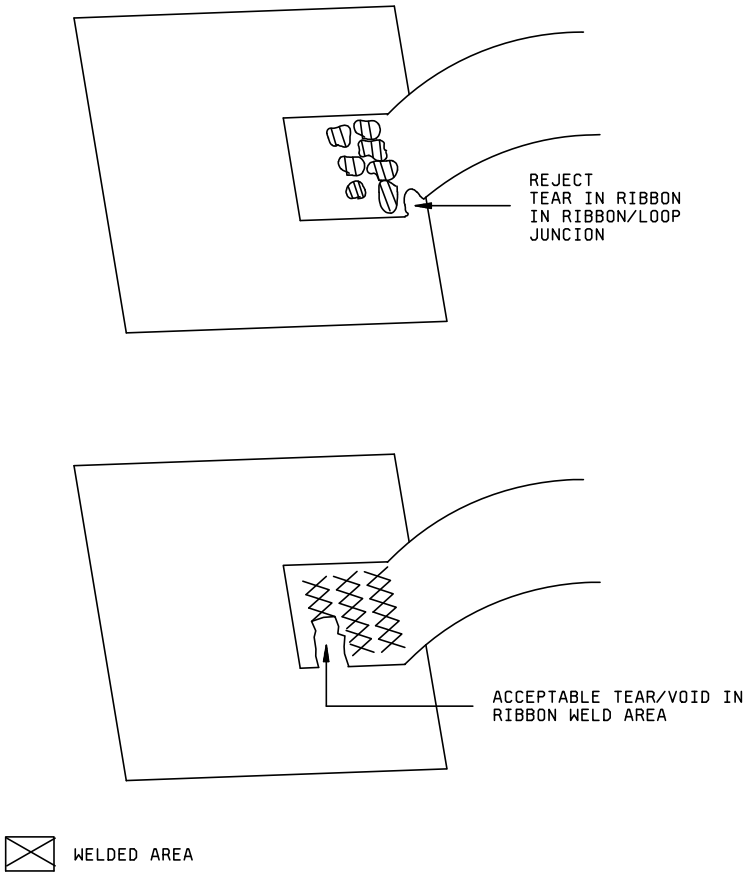

FIGURE 2017-19. Accept/Reject tears or voids in beam lead/ribbon weld area.

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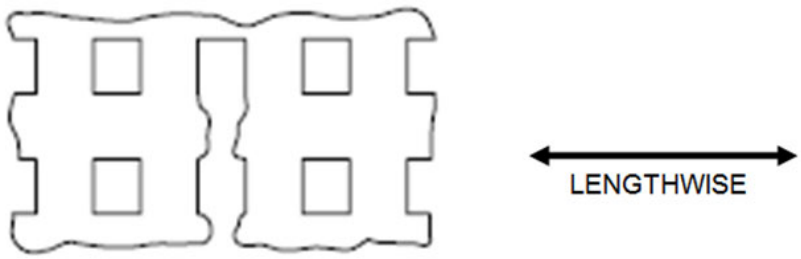
3.1.5.6 Mesh bonding. No device shall be acceptable that exhibits the following:

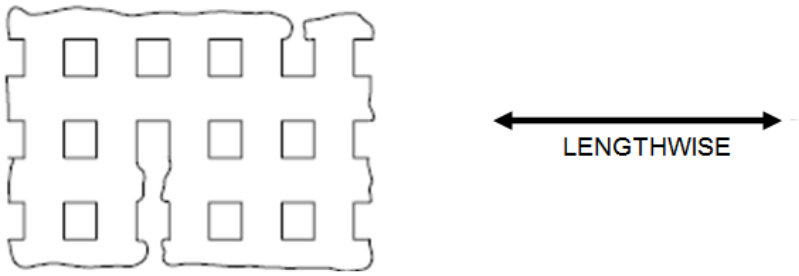
a. Less than 50 percent of the bond is on substrate metallization.

b. The number of continuous strands along the mesh is less than 50 percent of lengthwise strands through each section (see Figure 2017-20a).



Reject
Less than half of the lengthwise strands are continuous
(2 of 3 strands are discontinuous)

Figure 2017-20a. Criteria for strands along the mesh.



Accept
2 (half) or more of the lengthwise strands are continuous through each section

Figure 2017-20b. Criteria for strands along the mesh.

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c. Less than one continuous conducting path(s) through a bond (see figure 2017-20c).

d. Class K: Less than two continuous conducting path(s) through a bond (see Figure 2017-20c).

REJECT: NO CONTINUOUS PATH THROUGH THE MESH BETWEEN BONDS

ACCEPT: AT LEAST ONE CONTINUOUS PATH THROUGH THE MESH BETWEEN BONDS

REJECT FOR CLASS K

FIGURE 2017-20c. Criteria for continuous conducting paths.

3.1.5.7 Ribbon bonds. No device shall be acceptable that exhibits the following:

a. Any tears in the ribbon at the junction between the ribbon loop and bond/weld (see Figure 2017-19).

b. Bonds which do not exhibit 75 percent bond/weld impression(s) across the width of the ribbon overlapping underlying metallization.

NOTE: Gaps between welds on the ribbon caused by the natural footprint of a weld tip (i.e., split tip tool on parallel gap welder, etc.) are acceptable provided the total of all gaps do not exceed 25 percent of the ribbon width.

c. Effective bonded area less than 50 percent of that which would be possible for an exactly aligned ribbon.

d. Bond tails longer than one ribbon width or 10.0 mils, whichever is less, or bridging adjacent metallization.

e. The unbonded end of a ribbon bond tuning stub longer than one ribbon width or 10.0 mils, whichever is less, which is not secured by polymer adhesive.

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3.1.5.8 General. No device shall be acceptable that exhibits:

a. Bonds on the die where less than 50 percent of the bond is within the unglassivated bonding site.

NOTE: For Class K, monometallic bonds on the die where less than 50 percent of the bond is within the unglassivated bonding site. Bimetallic bonds on the die where less than 75 percent of the bond is within the unglassivated bonding site, except where due to geometry, and if by design, the bonding pad is smaller than the bond, then the criteria shall be 50%.

b. Any metal that is displaced as a result of bonding from its original position on the bonding pad (shooting metal) that reduces the separation between unglassivated operation metallization or scribe line to less than 1 mil or 50 percent design separation, whichever is less.

c. Bonds on the package post or substrate that are not completely within the bonding site.

NOTE: For cases where the substrate bonding site is smaller than 1.5 times the minimum bond size, bonds on the substrate where less than 50 percent of the bond is within the bonding site.

d. Bonds placed so that the wire exiting from a bond crosses over another bond, except by design, in which case the clearance shall be 2.0 wire diameters minimum (common bonds are excluded from this criteria).

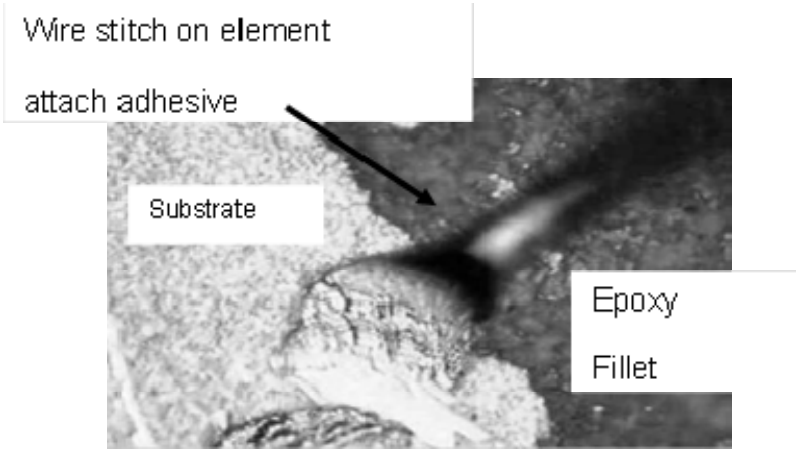
e. An absence of a visible line of separation between non-electrically common bonds.

f. An absence of a visible line of separation between a bond and non-electrically common metallization. This criteria applies to both glassivated and unglassivated metallization.

g. Wire bond tails that extend over or make contact with any non-common, unglassivated active metal.

h. Wire bond tails that exceed two wire diameters in length at the bonding pad or four wire diameters in length at the package post.

i. Bonds on element attach adhesive or on contaminated or foreign material (see figure 2017-20d).



Reject: Bond on element attach adhesive

Figure 2017-20d.

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j. Any lifted or peeling bond.

k. Intermetallic formation extending completely around the metallic interface of any bond between dissimilar metals.

l. Wedge, crescent or ball bonds at the point where metallization exits from the bonding pad that do not exhibit a line of undisturbed metal visible between the periphery of the bond and at least one side of the entering metallization stripe.

NOTE: Criteria of 3.1.5.8 (l) can be excluded when the entering conductor is >2 mils in width and the bond pad dimension on the entering conductor side is >3.5 mils.

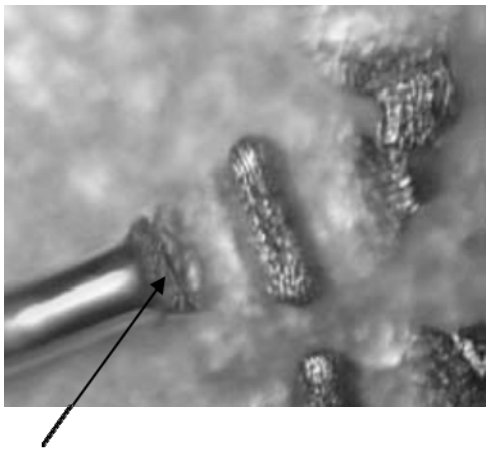
NOTE: For Class H only, the requirements for a visual line of metal can be satisfied when an acceptable wire tail obscures the area of concern, provided the following condition exists. Bond is located more than 0.1 mils from the intersecting line of the entering metallization stripe and the bonding pad and there is no visual evidence of disturbed pad metallization at the bond and wire tail interface.

NOTE: Criteria 3.1.5.8 (l) is not applicable to interdigitated (Lange) couplers or when the interface between a thermosonic/ultrasonic (i.e., non-thermocompression) bond and underlying metal is monometallic.

m. Polymeric adhesive which may be material or residue as evidenced by discoloration within 5.0 mils of the outer periphery of a wire bond.

n. Polymeric adhesive anywhere on a bond wire unless by design.

o. Tearing or cracks at the junction of the wire and bond (see figure 2017-20e). The junction is the line of deformation of the wire at the bonding site.



Reject bond is cracked at the heel.

Figure 2017-20e.

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3.1.6 Internal leads (e.g., wires, ribbons, beams, wire loops, ribbon loops, beams, etc.), "magnification 10X to 60X". No device shall be acceptable that exhibits:

a. Within the first 5.0 mils of wire from the die surface for ball bonds, or 10.0 mils for wedge bonds, any wire that comes closer than 1.0 mil to any non-common conductive surface (e.g., unglassivated operating metallization, unpassivated edge of conductive die). After 5 mils, or 10 mils for wedge bonds, the clearance shall be 2 wire diameters.

   NOTE: Insulated wires and electrically common wires are excluded from these criteria.

b. Nicks, cuts, crimps, scoring, or neckdown in any lead that reduces the lead diameter/width by more than 25 percent.

c. Missing or extra lead(s) not in conformance with bonding diagram.

   NOTE: Leads designated for tuning on the bonding diagram are excluded.

d. Any lead making a straight line run from bond to bond that has no arc, unless specifically allowed by the bonding diagram.

e. Wire(s) crossing wire(s) with a separation of less than 2 lead widths. Common or insulated conductors and insulated wires are excluded.

f. Complete or partial separation of the lead from the body of the element.

g. Excessive loop height such that the wire would contact the lid when it is installed.

3.1.7 Screw tabs and through hole mounting, magnification 3X to 10X. No device shall be acceptable that exhibits:

a. Misaligned tabs.

b. Missing or broken tabs.

c. Cracks emanating from mounting holes.

d. Loose substrates.

e. Missing or loose screws.

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3.1.8 Connector and feedthrough center contact soldering, magnification 10X to 30X. No device shall be acceptable that exhibits:

a. Less than 50 percent of center contact overlaps onto metallized pattern (see Figure 2017-21).

b. Center contact to substrate protrudes over onto circuit less than 1 diameter of a round pin or the width of a flat pin (see Figure 2017-22).

c. Voids in solder (see Figure 2017-23a).

d. Cracked solder joint (see Figure 2017-23b).

e. Poor adhesion, insufficient and un-smooth fillet, of solder to center line contact or substrate (see Figure 2017-23b).

f. Insufficient or excess solder (see Figures 2017-23c through 2017-23e).

g. Less than full coverage of solder along the length of the center contact and the metallization.

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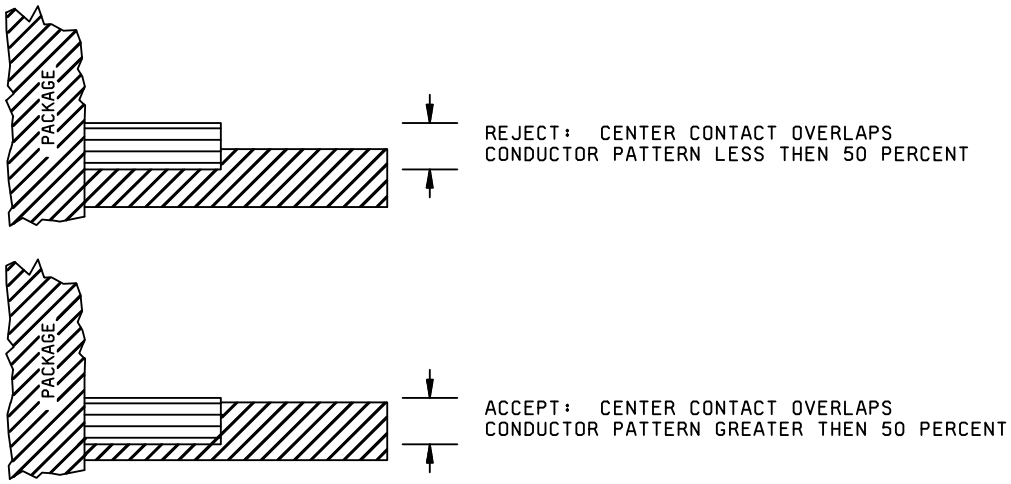

FIGURE 2017-21. Center contact orientations to substrate.

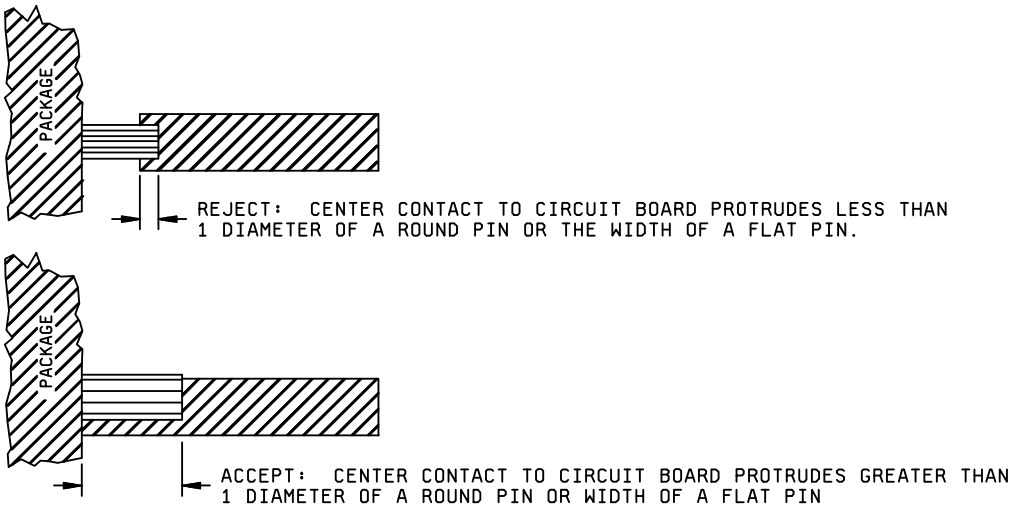

FIGURE 2017-22. Center Contact overlap to substrate.

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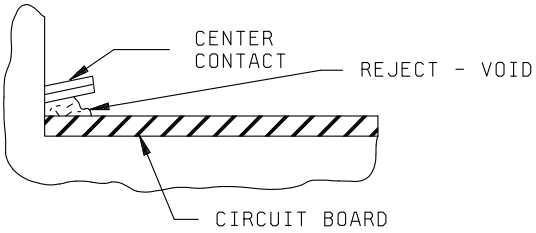

FIGURE 2017-23a. Void criteria.

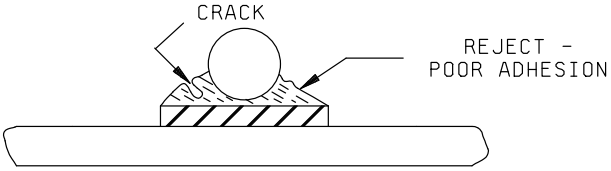

FIGURE 2017-23b. Crack/adhesion criteria.

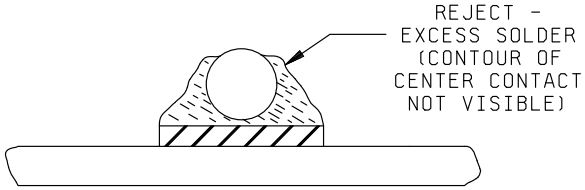

FIGURE 2017-23c. Excess solder criteria.

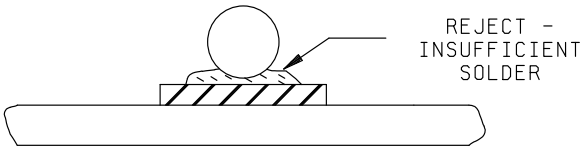

FIGURE 2017-23d. Insufficient solder criteria.

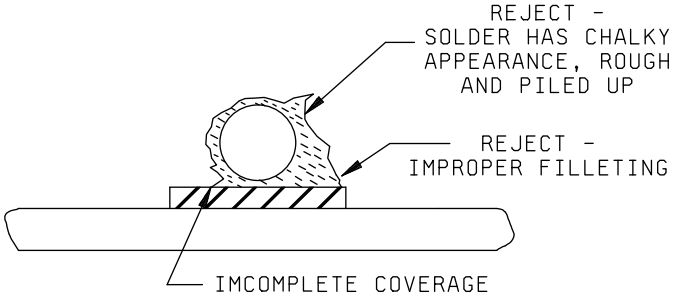

FIGURE 2017-23e. Solder criteria.

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3.1.9 Package conditions, "magnification 10X to 60X". No device will be acceptable that exhibits:

a. Unattached foreign material within the package or on the seal flange.

NOTE: All foreign material shall be considered to be unattached unless otherwise verified to be attached. Verification of attachments of foreign material whose longest dimensions are greater than 75 percent of the closest unglassivated conductive spacing shall be accomplished by a light touch with an appropriate mechanical device (i.e., needle, probe, pick, etc.). Verification of attachments of smaller material can be satisfied by suitable cleaning process approved by the acquiring or qualifying activity. All foreign material or particles may be removed, if possible, with a nominal gas blow (approximately 20 psig).

NOTE: Semiconductor chips shall be considered foreign particles.

b. Attached foreign material that bridges metallization paths, two package leads, lead to package metallization, functional circuit elements, junctions, or any combination thereof.

c. Liquid droplets or any chemical stain that bridges any combination of unglassivated or unpassivated active circuit areas.

d. Physical damage or contamination (eutectic or polymer material) that prevents adequate sealing of the seal surface.

e. Presence of any residual flux.

NOTE: Use 10X to 15X magnification.

f. Foreign material in melt that does not exhibit a fillet.

NOTE: As a guide, and for further information about package related defects, refer to JESD9.

4. SUMMARY. The following details shall be specified in the applicable acquisition document:

a. Test condition (see 3).

b. Where applicable, gages, drawings and photographs that are to be used as standards for operator comparison (see 2).

c. Where applicable, specific magnification if other than that specified.

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METHOD 2018.6

SCANNING ELECTRON MICROSCOPE (SEM) INSPECTIONS

1. PURPOSE. This method provides a means of judging the quality and acceptability of device interconnect metallization on non-planar oxide integrated circuit wafers or dice. SEM inspection is not required on planar oxide interconnect technology such as chemical mechanical polish (CMP) processes. It addresses the specific metallization defects that are batch process orientated and which can best be identified utilizing this method. Conversely, this method should not be used as a test method for workmanship and other type defects best identified using method 2010.

Samples submitted to SEM shall not be shipped as functional devices unless it has been shown that the device structure, in combination with the equipment operating conditions, is nondestructive.

1.1 Definitions.

1.1.1 Barrier adhesion metal. The lower layer of multi-layer metal system deposited to provide a sound mechanical bond to silicon/silicon oxide surfaces or to provide a diffusion barrier of a metal into an undesired area such as aluminum into a contact window.

1.1.2 Cross-sectional plane. An imaginary plane drawn perpendicular to current flow and which spans the entire width of the metallization stripe as illustrated in figure 2018-1. Metallization stripes over topographical variations (e.g., passivation steps, cross-overs, bird's head), which are nonperpendicular to current flow, are projected onto cross-sectional planes for purposes of calculating cross-sectional area reductions.

1.1.3 Destructive SEM. The use of specific equipment parameters and techniques that result in unacceptable levels of radiation damage or contamination of the inspected semiconductor structure.

1.1.4 Directional edge. A directional edge (see figure 2018-2) is typically the edge(s) of a rectangular contact window over which metallization may be deposited for the purpose of carrying current into, through, or out of the contact window for device operation. It should be noted that contact geometry, site of concern, or both may vary and if so, the directional edge concept should be modified accordingly.

1.1.5 General metallization (conductors). The metallization at all locations including metallization (stripes) in the actual contact window regions with the exception being at areas of topographical variation (e.g., passivation steps, bird's head, cross-overs).

1.1.6 Glassivation. Glassivation is the top layer(s) of transparent insulating material that covers the active circuit area (including metallization), except bonding pads and beam leads.

1.1.7 Interconnection. The metal deposited into a via to provide an electrical conduction path between isolated metal layers.

1.1.8 Major current-carrying directional edge. The directional edge(s) which is designed to provide a path for the flow of current into, through, or out of a contact window or other area(s) of concern (see figure 2018-2).

1.1.9 Multi-layer metallization (conductors). Two or more layers of metal used for electrical conduction that are not isolated from each other by a grown or deposited insulating material. The term "underlying metal" shall refer to any layer below the top layer of metal.

1.1.10 Multi-level metallization (conductors). A single layer or a multi-layer of metal shall represent a single level of metallization. A combination of such levels, isolated from each other by a grown or deposited layer of insulating material, shall comprise the multi-level metallization interconnection system. The use of vias to selectively connect portions of such level combinations through the isolation shall not effect this definition.

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1.1.11 Nondestructive SEM. The use of specific equipment parameters and techniques that result in negligible radiation damage, contamination, or both of the inspected semiconductor structure (see 3.10 and 3.11).

1.1.12 Passivation. The silicon oxide, nitride or other insulating material that is grown or deposited on the die prior to metallization.

1.1.13 Passivation steps. The vertical or sloped surface resulting from topographical variations of the wafer surface (e.g., contact windows, diffusion cuts, vias, etc.).

1.1.14 Via. The opening in the insulating layer to provide a means for deposition of metal to interconnect layers of metal.

1.1.15 Wafer lot. A wafer lot consists of microcircuit wafers formed into a lot at the start of wafer fabrication for homogeneous processing as a group and assigned a unique identifier or code to provide traceability and maintain lot integrity throughout the fabrication process.

2. APPARATUS. The apparatus for this inspection shall be a scanning electron microscope (SEM) having resolution of 250Å or less as measured on the photograph at use conditions and a variable magnification of 1,000X to 20,000X or greater. The apparatus shall be such that the specimen can be tilted to a viewing angle (see figure 2018-3) between 0° and 85°, and can be rotated through 360°.

2.1 Calibration. The magnification shall be within ±10 percent of the nominal value when compared with National Institute of Standards and Technology standard 484 or an equivalent at the magnification(s) used for inspection. The resolution shall be 250Å or less as verified with National Institute of Standards and Technology standard SRM-2069 or equivalent. Magnification and resolution verification shall be performed on a frequency defined by the manufacturer based on statistical data for his SEM equipment.

2.2 Operating personnel. Personnel who perform SEM inspection shall have received adequate training in equipment operation and interpretation of the images and resulting photographs prior to attempting certification for metallization inspection. Procedures for certification of SEM operators for metallization inspection shall be documented and made available for review upon request to the qualifying activity, or when applicable, a designated representative of the acquiring activity. This shall include provisions for recertification procedures once a year as a minimum.

Operator certifications and recertifications shall be documented and made available for review upon request to the qualifying activity, or when applicable, a designated representative of the acquiring activity.

2.3 Procedures. There shall be written procedures for metallization inspection. These procedures shall be documented and made available for review upon request to the qualifying activity, or when applicable, a designated representative of the acquiring activity.

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3. PROCEDURE.

3.1 Sample selection. Statistical sampling techniques are not practical here because of the large sample size that would be required. The wafer sampling requirements defined in table I, taken in conjunction with specific dice locations within the sampled wafers, minimize test sample size while maintaining confidence in test integrity. These dice are in typical or worst case positions for the metallization configuration.

Note: When die or packaged parts are to be evaluated for wafer lot acceptance and the requirements for wafer selection per Table I cannot be met, the following sample size shall be utilized:

a. If the die/packaged part is from a known homogeneous wafer lot (traceability specific to the wafer or wafer lot and objective evidence is available for verification), then the sample size shall be 8 devices randomly selected from the population.

b. If the die/packaged part is from a non-homogeneous wafer lot (traceability is unknown or no objective evidence is available for verification), then the sample size shall be 22 devices randomly selected from the population.

Die area submitted for SEM evaluation shall not have been or be located immediately adjacent to the wafers edge, and they shall be sufficiently free of smearing, so that the required inspection can be conducted in an area of undisturbed metallization. Acceptance of the interconnect metallization shall be based on examination of selected die area, using either a single wafer acceptance basis or a wafer lot acceptance basis.

Reference to die or dice within this test method implies the evaluation of a complete function or device. When approved by the qualifying activity, this requirement may be satisfied by the evaluation of a special SEM test vehicle existing within the scribe line (kerf), within each die, or within a special process drop in.

3.1.1 Sampling conditions. This sampling condition applies to devices which have glassivation over the metallization. Steps 1 and 2, which follow, both apply when acceptance is on a wafer lot acceptance basis. Step 2 applies only when acceptance is on a single wafer acceptance basis.

3.1.1.1 Step 1: Wafer selection. From each lot to be examined on a wafer lot acceptance basis, wafers shall be selected as defined by table I. If more than one wafer lot is processed through the metallization operation at one time, each wafer lot shall be grouped as defined by table I and a separate set of wafers shall be selected for each wafer lot being examined on a wafer lot acceptance basis.

3.1.1.2 Step 2: Dice selection. When a wafer is to be evaluated (for acceptance on a single wafer acceptance basis, or with one or more other wafers on a wafer lot acceptance basis), one of the following sampling conditions may be used at the manufacturer's option:

3.1.1.2.1 Sampling quadrants. Immediately following the dicing operation (e.g., scribe and break, saw, etch) and before relative die location on the wafer is lost, four dice shall be selected. The positions of these dice shall be approximately two-thirds of the radius (as measured from the center) of the wafer and approximately 90° apart. The glassivation shall then be removed from the dice using a suitable etchant process(es) (see 3.3) followed by SEM examination.

3.1.1.2.2 Sampling segment, prior to glassivation. This sampling condition may be used only if the subsequent wafer fabrication processing temperature is lower than 450°C (723K) and the width of the interconnect metallization is 3 microns or more. The use of this method with higher temperatures or smaller linewidths may be acceptable when correlation data, which shows there is no difference between this procedure and the normal etchback procedure, is submitted to and approved by the qualifying activity.

Two segments shall be separated from the opposite side of each wafer (i.e., subsequent to metallization and etching but prior to glassivation). These segments shall be detached along a chord approximately one-third of the wafer radius in from the edge of the wafer. One die approximately 1.5 cm from each end along the chord of each segment (i.e., four dice) shall be subjected to SEM examination.

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3.1.1.2.3 Sampling segment, after glassivation. After completion of all processing steps and prior to dicing, two segments shall be separated from opposite sides of each wafer. These segments shall be detached along a chord approximately one-third of the wafer radius in from the edge of the wafer. One die approximately 1.5 cm from each end along the chord of each segment (i.e., four dice) shall be subjected to SEM examination after the glassivation has been removed using a suitable etchant process(es) (see 3.3).

3.1.1.2.4 Sampling whole wafers, prior to glassivation. This sampling condition may be used only if the subsequent wafer fabrication processing temperature is lower than 450°C (723K) and the width of the interconnect metallization is 3 microns or more. The use of this method with higher temperatures or smaller linewidths may be acceptable when correlation data, which shows there is no difference between this procedure and the normal etchback procedure, is submitted to and approved by the qualifying activity.

After completion of the metallization and etching steps and specimen preparation operation, if applicable (see 3.3), the complete wafer shall be placed into the SEM equipment and four die approximately two-thirds of the radius (as measured from the center) of the wafer and approximately 90° apart shall be inspected.

No die or contiguous die from the inspected wafer shall be shipped as a functional device unless it is shown that the examination is nondestructive (see 3.10 and 3.11).

3.1.1.2.5 Sampling whole wafers, after glassivation. This condition is destructive. The complete wafer shall be subjected to the specimen preparation operation, if applicable (see 3.3), and then placed into the SEM equipment. Four die approximately two-thirds of the radius (as measured from the center) of the wafer and approximately 90° apart shall be inspected.

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TABLE I. Wafer sampling procedures for various metallization chamber configurations.

Metallization chamber configuration 1/ 2/	Number of wafer lots in chamber 3/	Required number of samples per wafer lot		Sampling plans per wafer lot
		Evaporation	Sputtering	
Projected plane view of the Wafer-holder is a circle. Wafer-holder is stationary or "wobbulates"	1 4/	5	2	Four from near the periphery of the wafer-holder and 90° apart. One from the center of holder. See figure 4.
	2	3, 4, or 5	2	See figure 4.
	3	3 or 4	2	See figure 4.
	4	3	2	See figure 4.
Wafer-holder is symmetrical (i.e., circular, square, etc.). Deposition source(s) is above or below the wafer-holder. Wafer-holder rotates about its center during deposition.	1, 2, 3, or 4 4/	2	2	For each wafer lot, one from the periphery of the wafer-holder, and one from close proximity to the center of rotation. See figure 4. 5/
Planetary system. One or more symmetrical wafer-holders (planets) rotate about their own axes while simultaneously revolving about the center of the chamber. Deposition source(s) is above or below the wafer-holders.	1, 2, 3, or 4 per planet 4/	2	2	For each wafer lot, one from near the periphery of a planet and one from near the center of the same planet. See figure 4. 6/
Continuous feed. Wafers are continuously inserted into deposition chamber through a separate pump down of an airlock (25 wafer nominal load)	1 1/	2	2	Two randomly selected wafers from each wafer lot.

1/ In this case, a wafer lot shall be defined as a batch of wafers which have received together those common processes which determine the slope and thickness of the passivation steps on these wafers.
2/ If a wafer-holder has only one circular row, or if only one row is used on a multi-rowed wafer-holder; the total number of specified sample wafers shall be taken from that row.
3/ If there is more than one wafer lot in a metallization chamber, each wafer lot shall be grouped approximately in a separate sector within the wafer-holder. A sector is an area of the circular wafer-holder bounded by two radii and the subtended arc; quadrants and semicircles are used as examples on figure 4.
4/ If the wafer lot size exceeds the loading capacity of the metallization system each processed sub-lot will be sampled as if it was a unique lot.
5/ When evaluation data shows that there is no relationship between SEM results and the physical location of the wafers during the metallization process. It shall be permissible to substitute two randomly selected wafers from each wafer lot. This analysis shall be repeated after each major equipment repair.
6/ Sample wafers need be selected from only one planet if all wafer lots contained in the chamber are included in that planet. Otherwise, sample wafers of the wafer lot(s) not included in that planet, shall be selected from another planet(s).

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3.1.2 Sampling Destructive Physical Analysis (DPA) evaluation. Finished product, wafers, or die may be subjected to the test conditions and criteria defined within this test method for the purpose of a DPA evaluation.

3.2 Lot control during SEM examination. After dice selection for SEM examination, the manufacturer may elect either of two options:

3.2.1 Option 1. The manufacturer may continue normal processing of the lot with the risk of later recall and rejection of product if SEM inspection, when performed, shows defective metallization. If this option is elected, positive control and recall of processed material shall be demonstrated by the manufacturer by having adequate traceability documentation.

3.2.2 Option 2. Prior to any further processing, the manufacturer may store the dice or wafers in a suitable environment until SEM examination has been completed and approval for further processing has been granted.

3.3 Specimen preparation. When applicable, glassivation shall be removed from the dice using an etching process that does not damage the underlying metallization to be inspected (e.g., chemical or plasma etch). Specimens shall be mounted for examination in a manner appropriate to the apparatus used for examination. Suitable caution shall be exercised so as not to obscure features to be examined.

Specimens may be examined without any surface coating if adequate resolution and signal-to-noise levels are obtained. If the specimens need to be coated, they shall be coated with no more than 100Å of a thin vapor-deposited or sputtered film of a suitable conductive material (e.g., Au). The coating deposition process shall be controlled such that no artifacts are introduced by the coating.

3.4 Specimen examination, general requirements. The general requirements for SEM examination of general metallization and passivation step coverage are specified below in terms of directional edge, magnification, viewing angle, and viewing direction.

3.4.1 Directional edge. All four directional edges of every type of passivation step (contact window or other type of passivation step) shall be examined on each specimen (see table II).

3.4.2 Magnification. The magnification used for examination of general metallization and passivation steps shall be within the range defined by table II.

3.4.3 Viewing angle. Specimens shall be viewed at whatever angle is appropriate to accurately assess the quality of the metallization. Contact windows, metal thickness, lack of adhesion, and etching defects are typically viewed at the angles of 0° to 85° (see figure 2018-3).

3.4.4 Viewing direction. Specimens shall be viewed in an appropriate direction to accurately assess the quality of the metallization. This inspection shall include examination of metallization at the edges of contact windows and other types of passivation steps (see 3.4) in any direction that provides clear views of each edge and that best displays any defects at the passivation step. This may mean that the viewing angle is perpendicular to an edge, or in parallel with an edge, or at some oblique angle to an edge, whichever best resolves any question of defects at the passivation step (see figure 2018-5).

3.5 Specimen examination detail requirements. Examination shall be as specified herein and summarized in table II. The specimen examination shall be documented in accordance with 3.8.

3.5.1 General metallization. At low magnification, inspect at least 25 percent or 10,000 square mils, whichever is less, of the general metallization on each die for defects such as lifting, peeling, blistering, and voiding. Inspection shall be performed for each layer of each level of metallization.

3.5.1.1 Multi-layer and multi-level metal interconnection systems. Each layer of each metallization level that is deposited shall be examined. The current- carrying layer(s) shall be examined with the SEM after removal of the glassivation layer (if applicable) with a suitable etchant (see 3.3).

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3.5.1.2 Barrier/adhesion layers. The examination of barrier/adhesion layers designed to conduct less than 10% of the total current is not required as this is considered a non-conduction layer.

3.5.1.2.1 Barrier/adhesion layer as a conductor. The barrier/adhesion layer shall be considered as a conductor (considering the layer thickness and relative conductivity) provided that the following conditions are satisfied: At least ten percent of the current is designed to be carried by this layer; and this layer is used in the current density calculations. When this occurs the barrier/ adhesion layer and/or the principal conducting layer shall satisfy all of the step coverage requirements collectively as baselined by the manufacturer. Specimen examination shall be in accordance with 3.5 and the accept/reject criteria as defined in 3.7.1. The barrier/adhesion layer(s) shall be examined using either the SEM or optical microscope. The following methods may be used to examine these barrier/adhesion layers:

3.5.1.2.1.1 The Etchback procedure. This involves the stripping of each successive unique layer of metal by selective etching, with suitable etchants, layer by layer, to enable the examination of each layer. Typically, each successive layer of metal will be stripped in sequence to expose the next underlying layer for examination. Successive layer removal on a single die area may be impractical. In this case the wafer area or additional die (dice) immediately adjacent on the slice to the original die area shall be stripped to meet the requirement that all unique layers shall be exposed and examined.

3.5.1.2.1.2 In-line procedure. The wafer(s) shall be inspected for the defined accept/reject criteria immediately after being processed through each unique deposition and corresponding etching operation.

3.5.2 Passivation steps. Inspect the metallization at all types of passivation steps in accordance with the requirements of 3.5.1.1 and table II.

TABLE II. Examination procedure for specimens.

Device type	Area of examination	Examination	Minimum-maximum magnification	Photographic documentation 1/
Integrated circuit devices	Passivation steps (contact windows and other types of passivation steps) 2/	At least one of each type of passivation step present	5,000X to 50,000X	Two of the worst case passivation steps
	General metallization 2/	25 percent	1,000X to 6,000X	Worst case general metallization

1/ See 3.8 (an additional photograph may be required).
2/ See 3.7 for accept/reject criteria.

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3.6 Acceptance requirements.

3.6.1 Single wafer acceptance basis. The metallization on a single wafer shall be judged acceptable only if all the sampled areas or dice from that wafer are acceptable.

3.6.2 Wafer lot acceptance basis. An entire wafer lot shall be judged acceptable only when all the sampled areas or dice from all sample wafers are acceptable. If a wafer lot is rejected in accordance with this paragraph each wafer from that wafer lot may be individually examined; acceptance shall then be in accordance with 3.6.1.

3.7 Accept/reject criteria. Rejection of dice shall be based on batch process defects and not random defects such as scratches, smeared metallization, tooling marks, etc. In the event that the presence of such random defects obscures the detailed features being examined, an additional adjacent sample shall be inspected. Illustrations of typical defects are shown in figures 2018-6 through 2018-22.

3.7.1 General metallization. Any evidence of poor metallization adhesion shall be unacceptable. Any defects (see figure 2018-18 and 2018-20), such as voids, cracks, separations, depressions, notches, or tunnels, which singly or in combination reduce the cross-sectional area of the general metallization stripe by more than 50 percent shall be unacceptable. Two specific cases of general metallization are specified below:

3.7.1.1 Conductor stripes. In the examination of the other metal layers for the specific case of conductor stripes (exclusive of the contact window area), a defect consuming 100 percent of the thickness of the barrier/adhesion stripe shall be acceptable provided that the defect does not extend more than 50 percent across the width of the metallization stripe (see figure 2018-22).

3.7.1.2 Barrier layers in contact window areas. No defects of any kind in a barrier layer which would bring the overlying metal layer in contact with the semiconductor material surface shall be permitted.

3.7.1.3 Overlying adhesion layers. For the metal layer(s) above the principal conducting layer, a defect consuming 100 percent of the thickness of the adhesion stripe shall be acceptable provided that the defect does not extend more than 50 percent across the width of the metallization stripe.

3.7.2 Passivation steps. Metallization over a passivation step shall be unacceptable if any combination of defects (see figure 2018-23) or thinning of the metal reduces the cross-sectional area of the metallization stripe along any cross-sectional plane in a major current-carrying direction to less than 50 percent of the cross-sectional area of the stripe. A minimum of 20 percent total metallization coverage (barrier metal inclusive, see figure 2018-24) in the primary current carrying direction will be allowed for metallization over a passivation step when the structure involved is a circular or multisided via or contact structure and there is sufficient wrap-around metal (>10 percent of incoming metal line width) to allow for current flow to all sides of the via or contact. The metallization must meet the current density requirements of MIL-PRF-38535. In cases where an absence of visible edge or a smooth transition or taper clearly reveals effective coverage, a cross-section will be performed to verify metal coverage.

3.7.2.1 Nonrejectable cross-sectional area. In the event that the metallization cross-sectional area at a particular directional edge profile is less than as allowed in 3.7.2. This shall not be cause for rejection if the following two conditions occur:

3.7.2.1.1 Condition 1. It is determined that the directional edge profile from which metal is absent does not occur in the major current-carrying directional edge. Such determination shall be made either by scanning all passivation steps of this type on the remainder of the die, or by the examination of a topographical map supplied by the manufacturer which shows the metal interconnect pattern.

3.7.2.1.2 Condition 2. Acceptance shall be on a single wafer basis only.

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3.7.2.2 Nonrejectable, noncovered directional edge. For passivation steps to be acceptable, all directional edges shall be covered with metallization and be acceptable to the requirements of 3.7.2.1, unless by design. In the event that a directional edge profile of a particular type of passivation step is not covered with metallization, this shall not be cause for rejection if the following two conditions occur:

3.7.2.2.1 Condition 1. It is determined that the directional edge profile from which metal is absent does not occur in the major current-carrying directional edge. Such determination shall be made either by scanning all passivation steps of this type on the remainder of the die, or by the examination of a topographical map supplied by the manufacturer which shows the metal interconnect pattern.

3.7.2.2.2 Condition 2. None of the other specimens from the sampled wafers representing the lot exhibit a directional edge profile from which metal is absent in the major current-carrying directional edge.

NOTE: If both 3.7.2.2.1 and 3.7.2.2.2 are satisfied, a wafer lot acceptance basis shall be used. However, if only 3.7.2.2.1 is satisfied, a single wafer acceptance basis shall be used.

3.7.3 Verification of potential rejects. At the option of the manufacturer, it shall be permissible to subject the specimen, or an adjacent sample that exhibits the same reject mode, to a verification test. Given below are some examples of suitable verification tests:

3.7.3.1 Cross-sectioning. A passivated sample shall be cleaved or lapped down to bisect the area of concern. The sample may then be subjected to an etchant that will remove the interconnecting metallization at the inspection surface (i.e., approximately perpendicular to the die surface). Specimens may be examined without any special surface coating if surface charging is not a significant problem and adequate resolution and signal-to-noise levels are obtained. If the specimens are coated, they shall be coated with a thin vapor-deposited or sputtered film of a suitable conductive material (i.e., 100Å gold). The coating deposition processes shall be controlled such that no artifacts are introduced by the coating. The sample shall be prepared (see 3.3) and examined in the SEM for interconnect metallization thickness or percentage coverage at the passivation step, or any other relevant parameter. Note: This cross-sectioning technique is not conclusive for hairline microcracks as they are not adequately filled by the passivation material.

3.7.3.1.1 Dimensional errors. Care must be taken to ensure that the cross-section is close to the center of a contact in order to avoid dimensional errors due to the rounding of the contact corners.

3.7.3.2 Surface etchback. The unpassivated sample surface is subjected to a chemical etch which removes the interconnection metallization from the surface of the die at a known controlled rate. The etching is stopped when the required metal thickness has been removed. The sample is then prepared (see 3.3) and examined within the SEM for residual metal at the passivation step/contact window interface. Photographic evidence shall then be taken of the sample(s) to support the acceptance or rejection of the material.

3.7.3.3 Topographical integration. A graphical representation of the worst case cross-sectional area is drawn to scale on appropriate graph paper from comprehensive photographs taken eucentrically about the directional edge. The cross-sectional area is then graphically integrated. This technique is useful for evaluating metallization with irregular surface topography.

3.8 Specimen documentation requirements. A minimum of three photographs of each level of metallization inspected per lot shall be taken and retained for a minimum of five years after performance of the inspection. Two photographs shall be of worst case passivation steps and the third photograph of worst case general metallization. If any photograph shows an apparent defect within the field of view, another photograph shall be taken to certify the extent of the apparent defect (see table II).

NOTE: Alternate methods of image storage (e.g., video disk or video tape) shall be acceptable with the prior approval of the qualifying activity.

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3.8.1 Required information. The following information shall be traceable to each photograph:

a. Date of SEM photograph.

b. Device or circuit identification (type or part number).

c. Area of photographic documentation.

d. Electron beam accelerating voltage.

e. Magnification.

f. Manufacturer.

g. Manufacturer's lot identification number.

h. Record of calculated/measured percentage step coverage.

i. SEM operator or inspector's identification.

j. Viewing angle.

3.9 Disposition of inspected specimens. SEM samples and contiguous die shall not be shipped as functional devices unless nondestructive SEM conditions and requirements are met (see 3.10). In order to be considered nondestructive, suitable life-test data (see 3.11) shall be submitted for approval to the qualifying activity to substantiate the nondestructive aspects of the test (e.g., radiation hardness degradation-RHD). Additionally, all of the conditions in 3.10 and 3.11 must be satisfied.

3.10 Nondestructive SEM conditions. For nondestructive SEM, the following conditions shall apply:

3.10.1 Equipment conditions.

a. The accelerating voltage shall be within the 0.5 kV to 2.0 kV range.

b. The absorbed specimen current (as measured with a Faraday cup) shall be less than 500 pA.

c. Total scan time for each test site on the wafer shall not exceed ten minutes.

d. Resolution for metal inspection shall be in accordance with 2 above at the accelerating voltage of 3.10.1a. When used for other in-line nondestructive SEM evaluations (e.g., photoresist, critical dimension (cd) inspection, etc.) the resolution shall be sufficient to clearly verify the measurement.

3.10.2 Wafer conditions.

a. The wafer lot shall satisfy the thermal stability criteria defined within MIL-STD-883, method 5007, table I.

b. Weekly monitoring of particle counts shall be conducted in the SEM inspection area. The particle count limits shall be less than or equivalent to the specified wafer fab limits.

c. The wafer shall be clean and free of any surface coating.

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3.11 Required data for nondestructive SEM validation. Data demonstrating that the method is nondestructive as defined in A.4.3.2.2 of Appendix A of MIL-PRF-38535 shall be submitted to the qualifying activity following the procedure detailed in 3.11.1 through 3.11.3.

3.11.1 Sample conditioning. Expose a sufficient number of devices to the following conditions to yield a quantity of life test samples that meet a quantity (accept number) of 45(0) for each validation sample:

a. Sample A: Expose at the worst case SEM operating conditions (i.e., accelerating voltage, absorbed specimen current and tilt) and normal SEM metallization inspection procedure for a duration of 10 ± 1 minutes.

b. Sample B: Expose at the worst case SEM operating conditions and normal SEM metallization inspection procedure for an increased duration of 30 ± 3 minutes.

c. Sample C: (Optional at the discretion of the manufacturer.) Control group without any SEM exposure.

3.11.2 Procedure. Process test groups through all normal screening steps to complete post burn-in electricals, serialize test samples, and complete 3.11.2a through 3.11.2d.

a. Data log variables on all 25°C dc parameters and record attributes data for all other group A electrical test parameters, conditions and limits specified in the device specification or drawing (i.e., complete group A, not only specified life test endpoints).

b. Place test samples, including the control group if applicable, on life test in accordance with method 1005 at 125°C minimum for 1630 hours or equivalent (130°C for 1,135 hours, 135°C for 800 hours, 140°C for 565 hours, 145°C for 405 hours, 150°C for 295 hours, 155°C for 215 hours, 160°C for 155 hours, 165°C for 115 hours, 170°C for 85 hours, 175°C for 65 hours) with cooldown under bias using test condition C.

c. Repeat 3.11.2a for post life test endpoints.

d. Provide qualifying activity with one set of test results for each sample in terms of variables and attributes data on pre and post life test endpoints plus analysis of mean and standard deviation of variables data and indication of any devices which failed any group A test parameters.

3.11.3 Criteria for validating SEM as nondestructive. If sample A passes single duration and sample B passes triple duration SEM exposure and life test without failing any device specification or drawing parameters, conditions and limits (or delta parameter requirements when they are specified), the SEM procedure shall be validated as nondestructive for the process flow represented by the sample devices and for other devices from the same process flow. With the approval of the qualifying activity, this SEM nondestructive qualification may be performed on appropriate process monitor structures or standard evaluation circuits (SEC's) which represent the process flow.

4. SUMMARY. The following details may be specified in the applicable acquisition document:

4.1 Detail 1. Single wafer acceptance basis when required by the acquiring activity.

4.2 Detail 2. Requirements for photographic documentation (number and kind) if other than as specified in 3.8.

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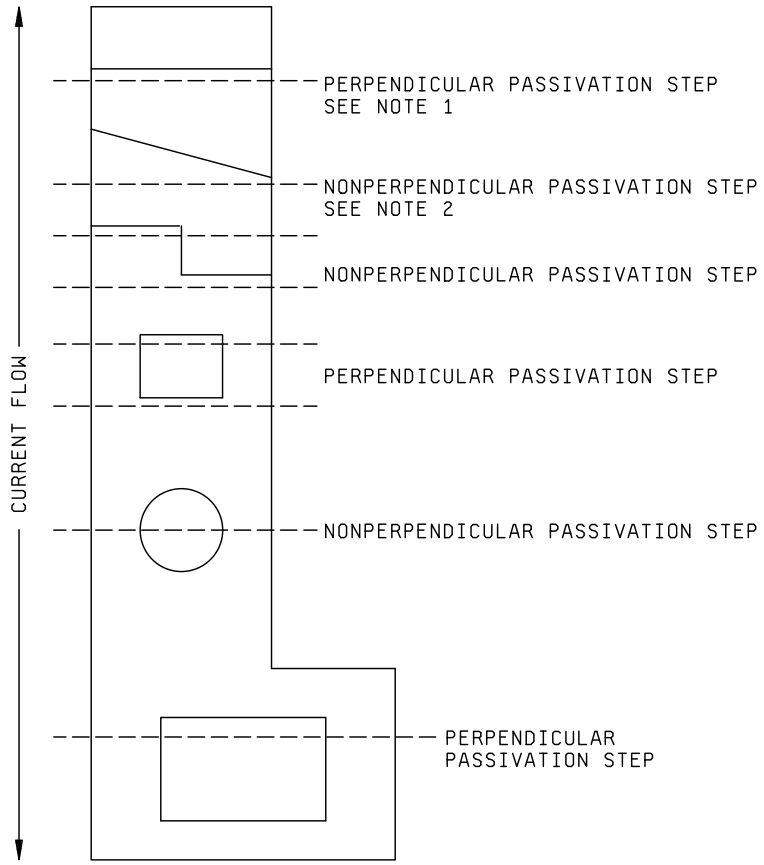

A

NOTES:

1. Cross-sectional planes are denoted by dashed lines.
2. All passivation steps nonperpendicular to current flow must be projected onto cross-sectional planes perpendicular to current flow for purpose of cross-sectional area calculations.
3. The purpose of this cross-sectional plane illustration is two-fold:

   To provide a consistent and convenient means to facilitate the calculation of the appropriate cross-sectional area.

   To insure that the cross-sectional area of the metallization in a major current carrying direction is reduced to no more than 50 percent (30 percent when appropriate) for the topographical variation under consideration.

FIGURE 2018-1. Cross-sectional planes at various passivation steps.

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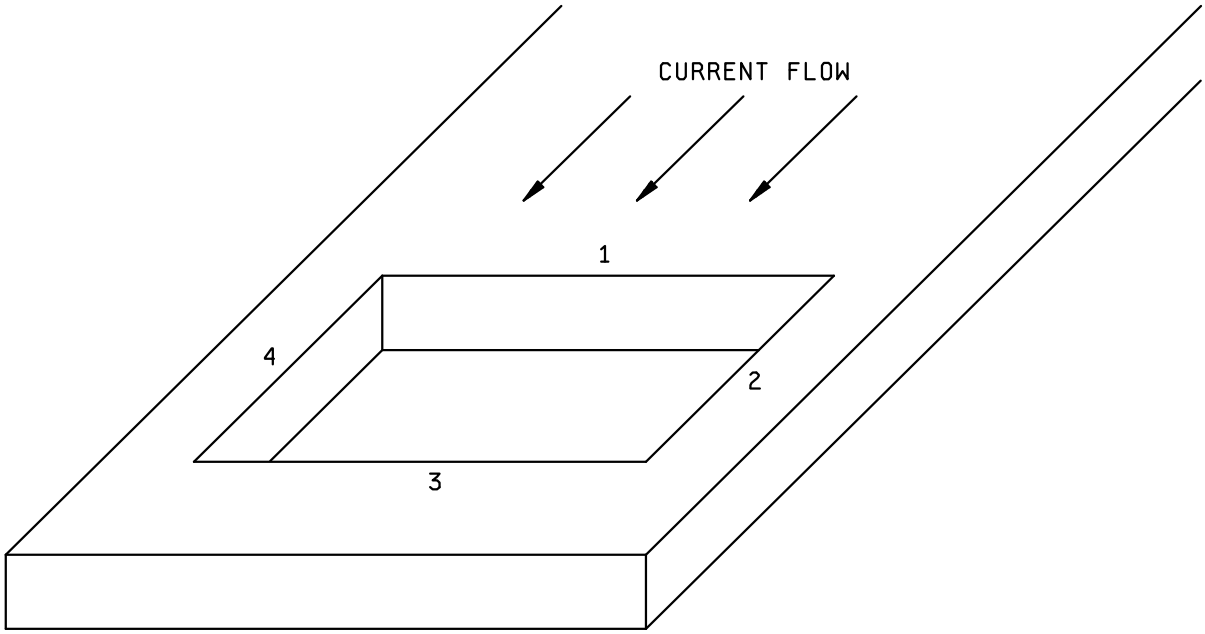

NOTES:
1. 1, 2, 3, and 4 are directional edges.
2. 1 is a major current carrying edge.

FIGURE 2018-2. Directional edge.

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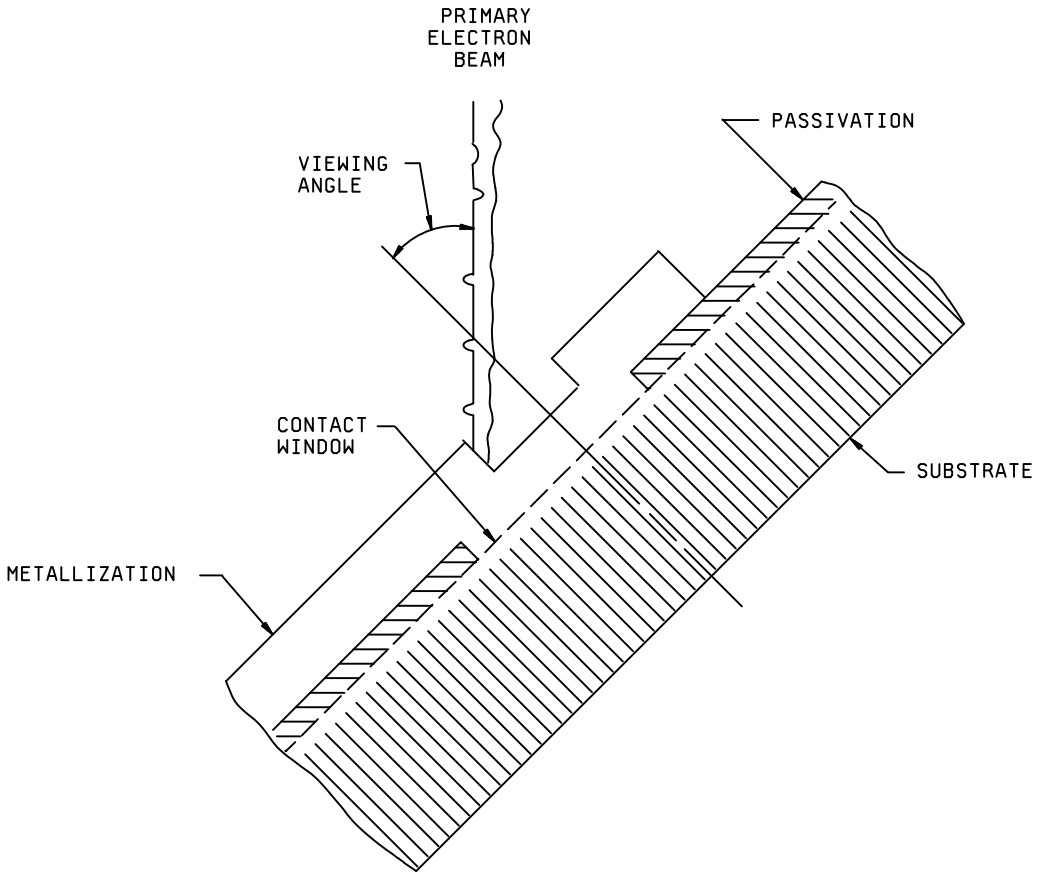

FIGURE 2018-3. Viewing angle.

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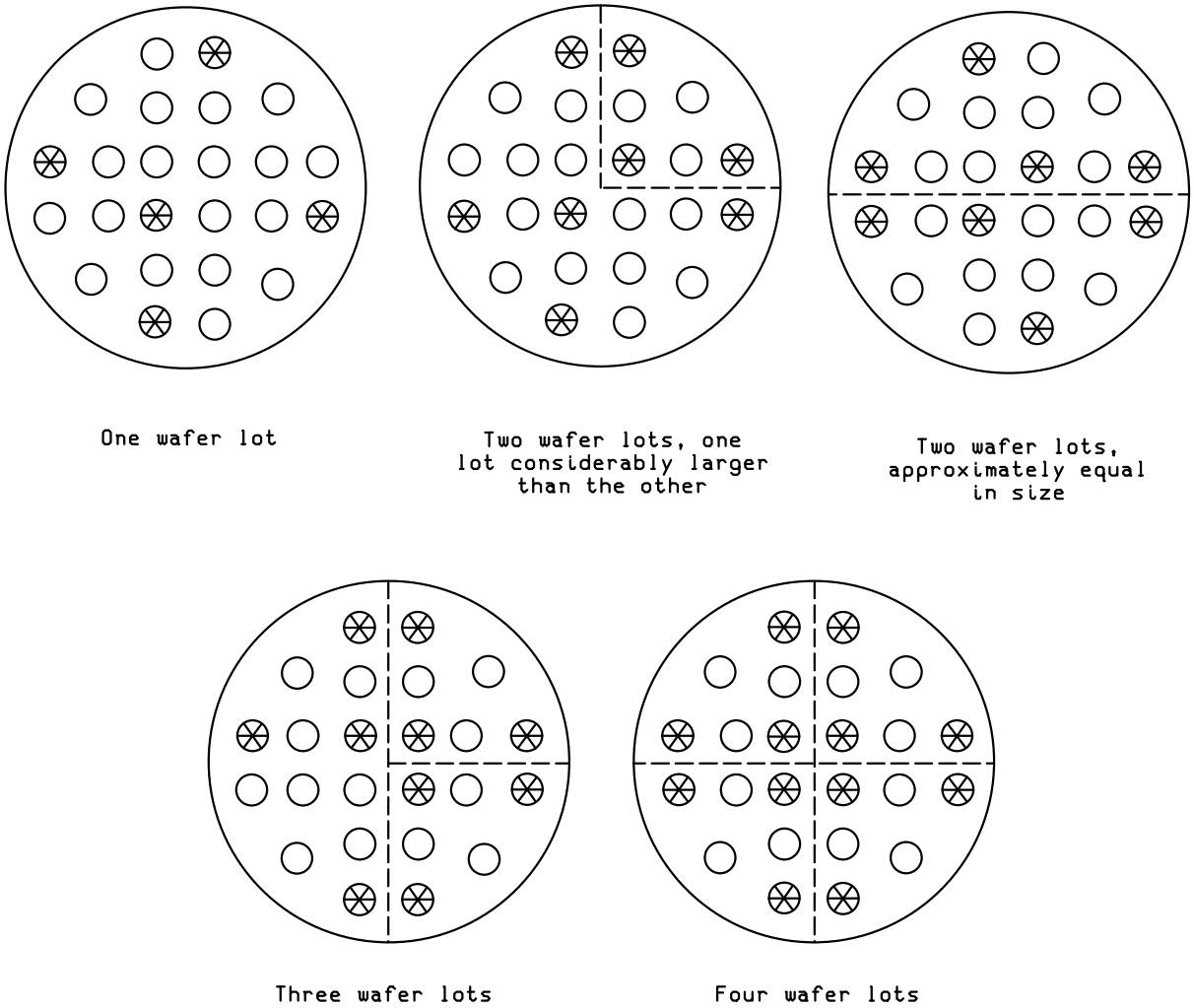

STATIONARY (EVAPORATION) WAFER-HOLDER SYSTEM

FIGURE 2018-4. Wafer sampling procedures (see table I).

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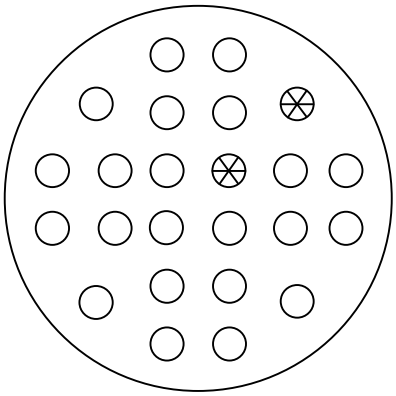
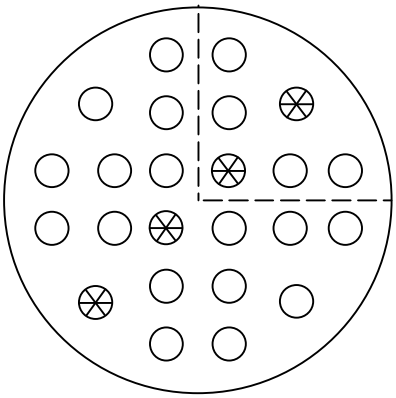
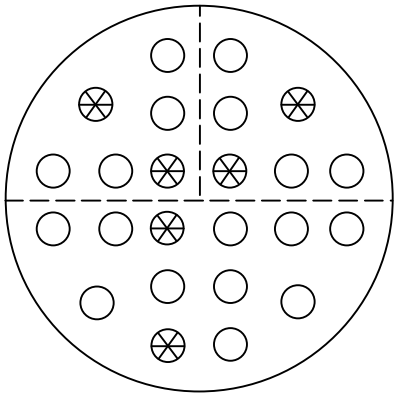


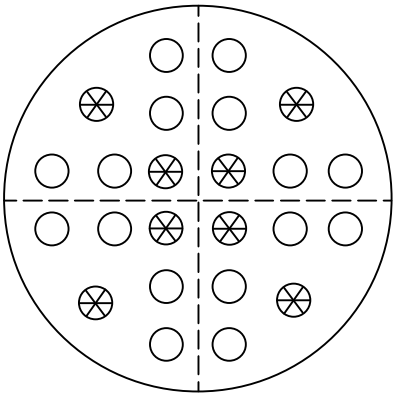
One wafer lot



Two wafer lots



Three wafer lots



Four wafer lots

ROTATING STATIONARY (SPUTTERING) PLANETARY OR CONTINUOUS FEED WAFER-HOLDER SYSTEM

FIGURE 2018-4. Wafer sampling procedures (see table I) - Continued.

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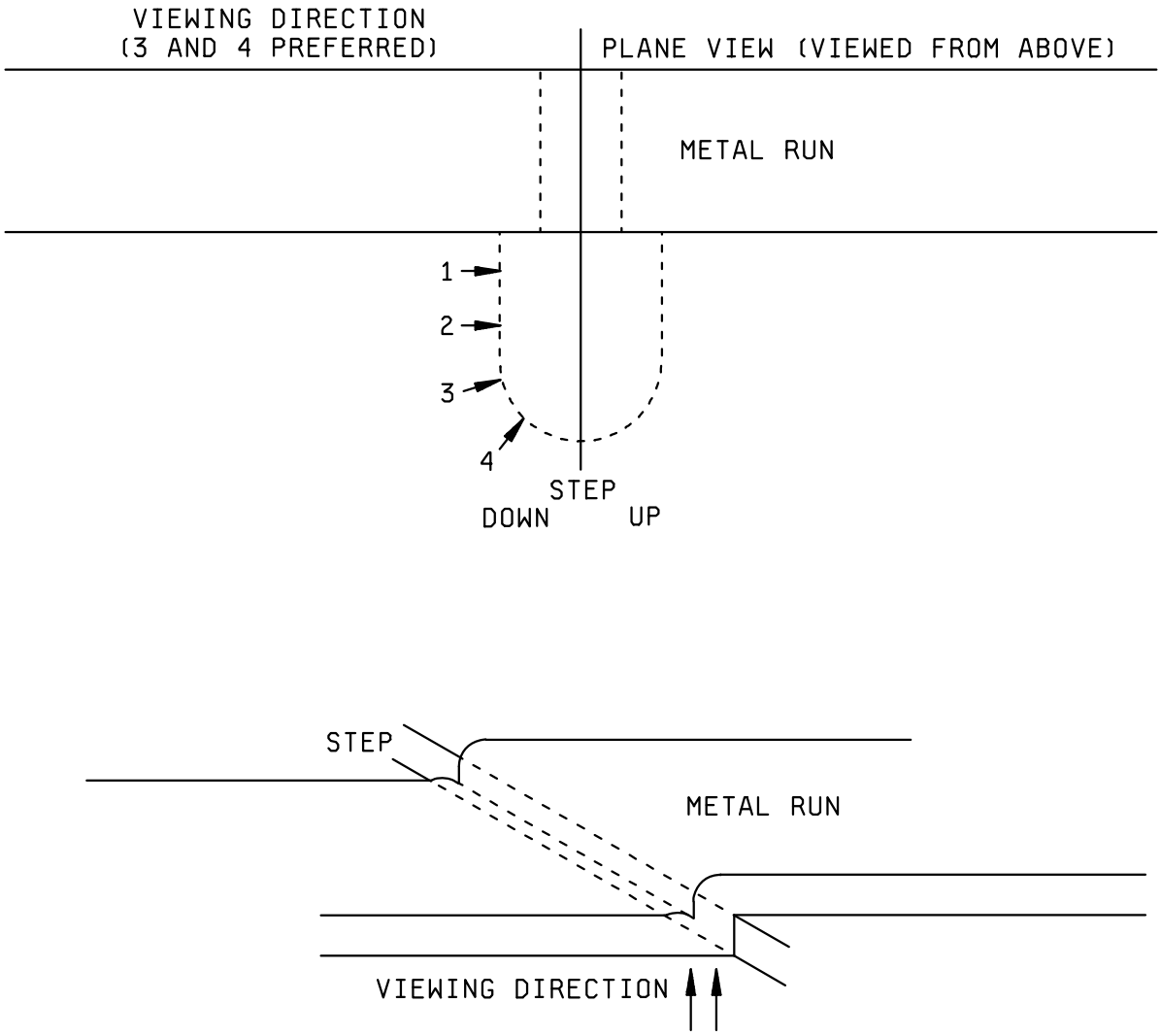

FIGURE 2018-5. Viewing direction.

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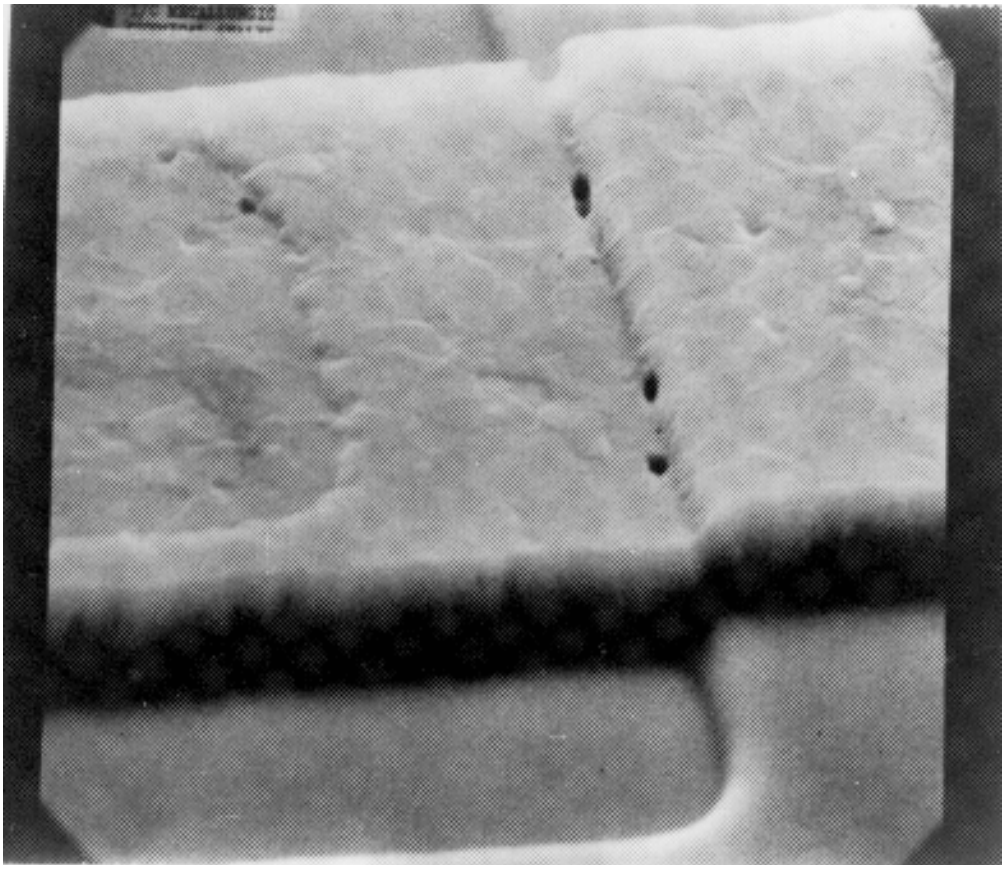

FIGURE 2018-6. (3,400X).
Voiding at passivation step (accept).

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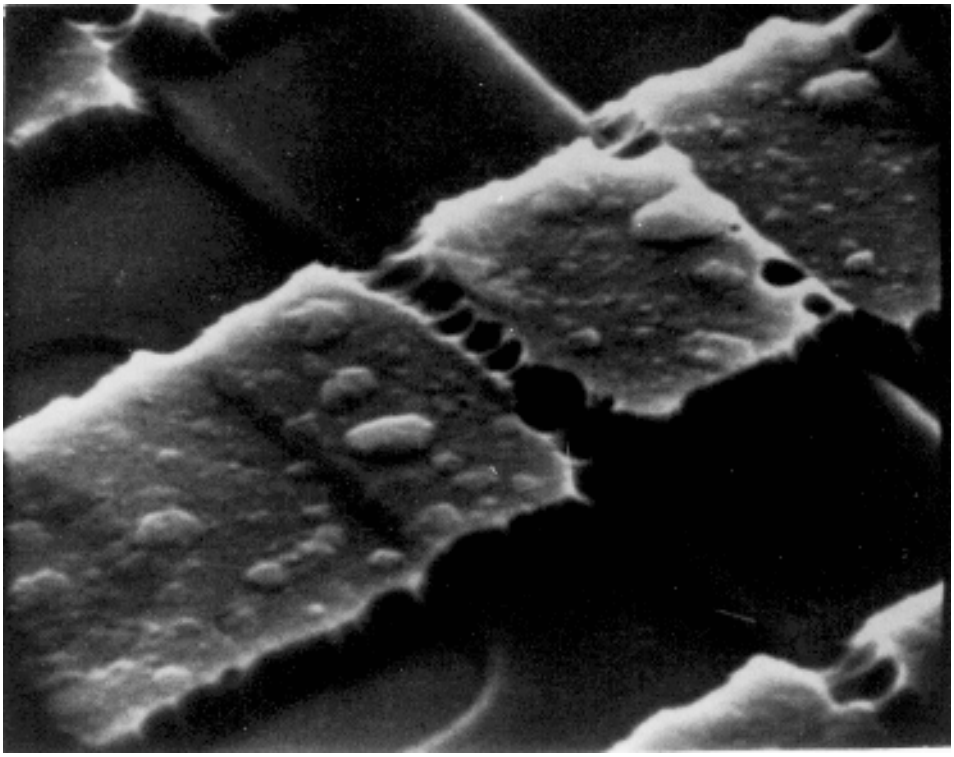

FIGURE 2018-7. 5,000X.
Voiding at passivation step (reject).

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NOTE: Tunnel does not extend to surface of metal; does not reduce cross-sectional area more than 50 percent.

FIGURE 2018-8. (10,000X).
Tunnel/cave at passivation step (accept).

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FIGURE 2018-9. 5,000X.
Tunnel/cave at passivation step (reject).

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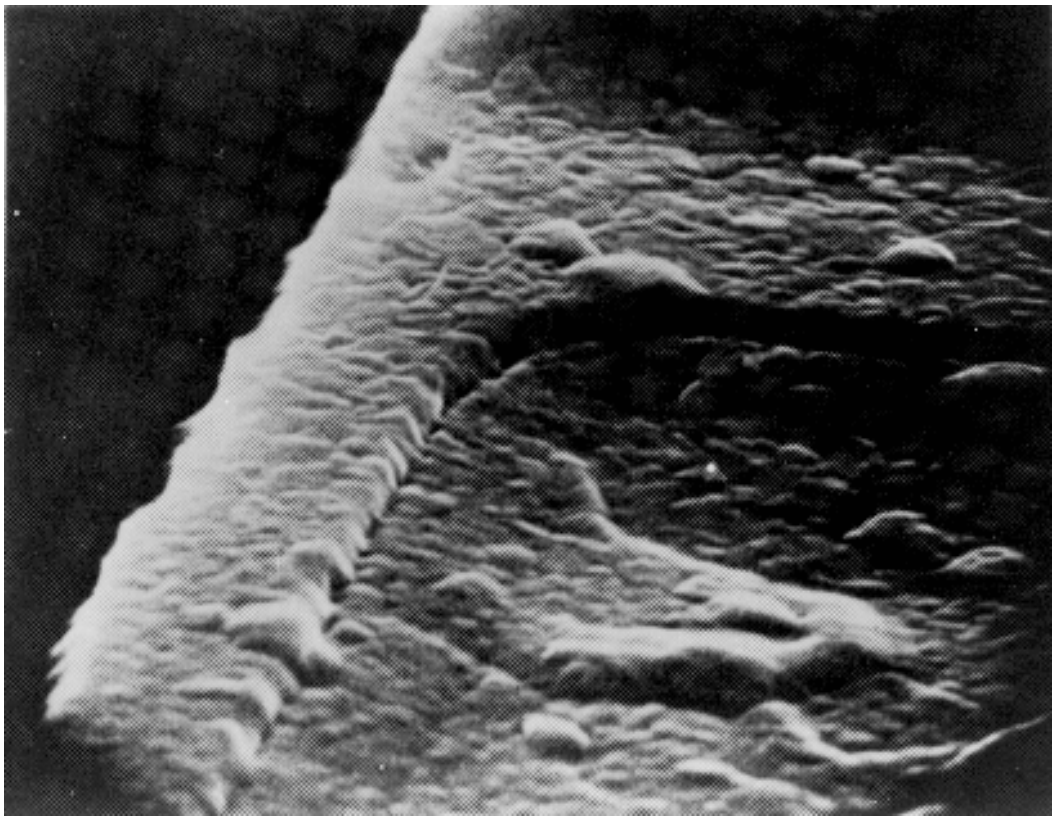

FIGURE 2018-10. (10,000X).
Separation of metallization at
passivation step (base contact) (accept).

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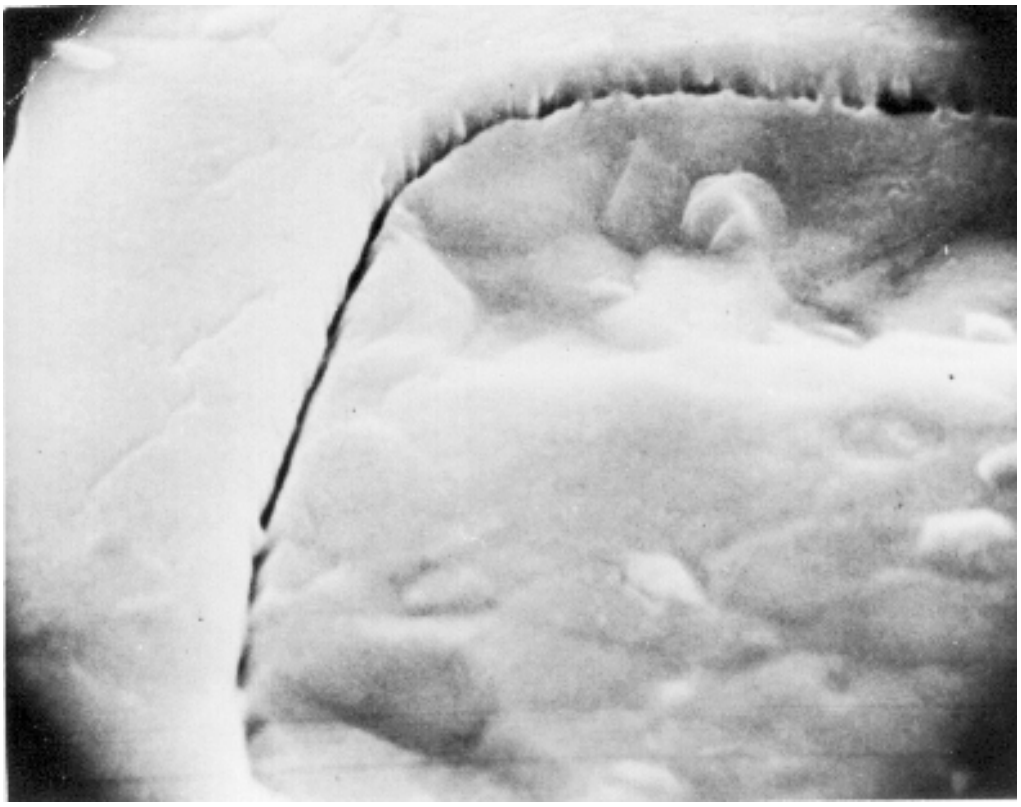

FIGURE 2018-11. 7,000X.
Separation of metallization at
passivation step (base contact) (reject).

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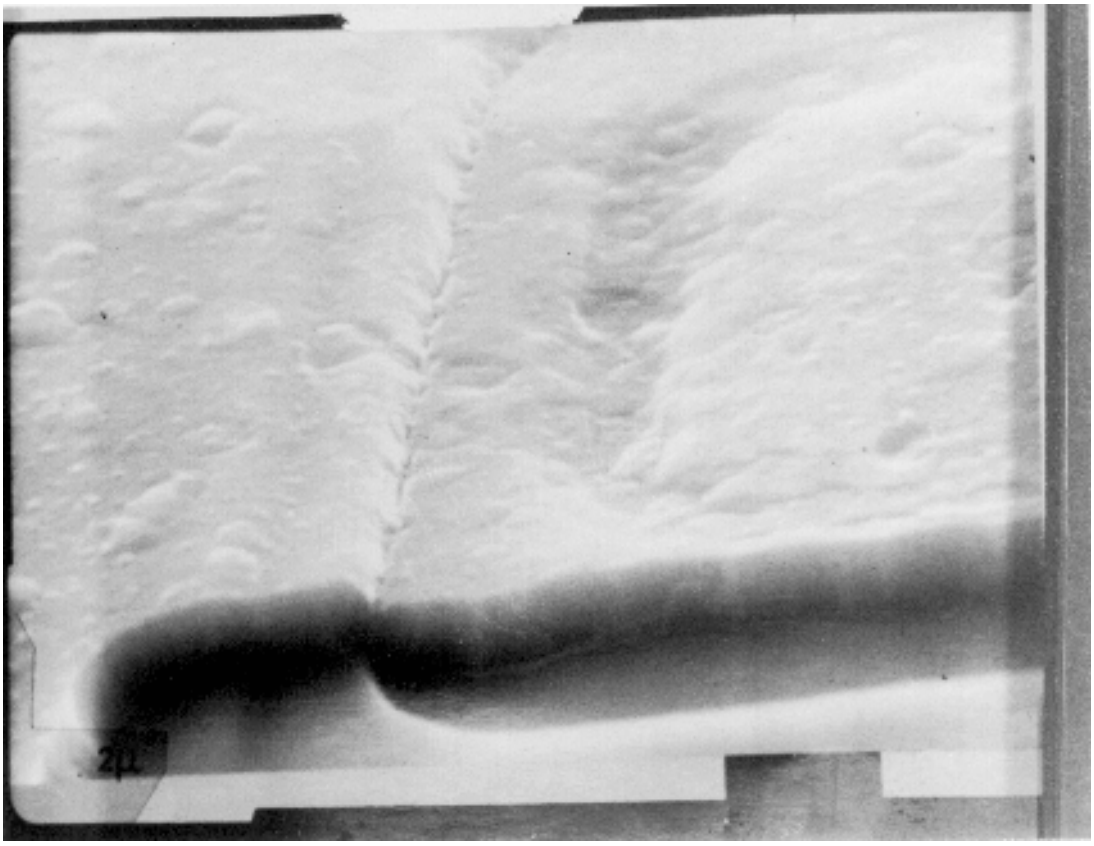

FIGURE 2018-12. (6,000X).
Crack-like defect at passivation step (accept).

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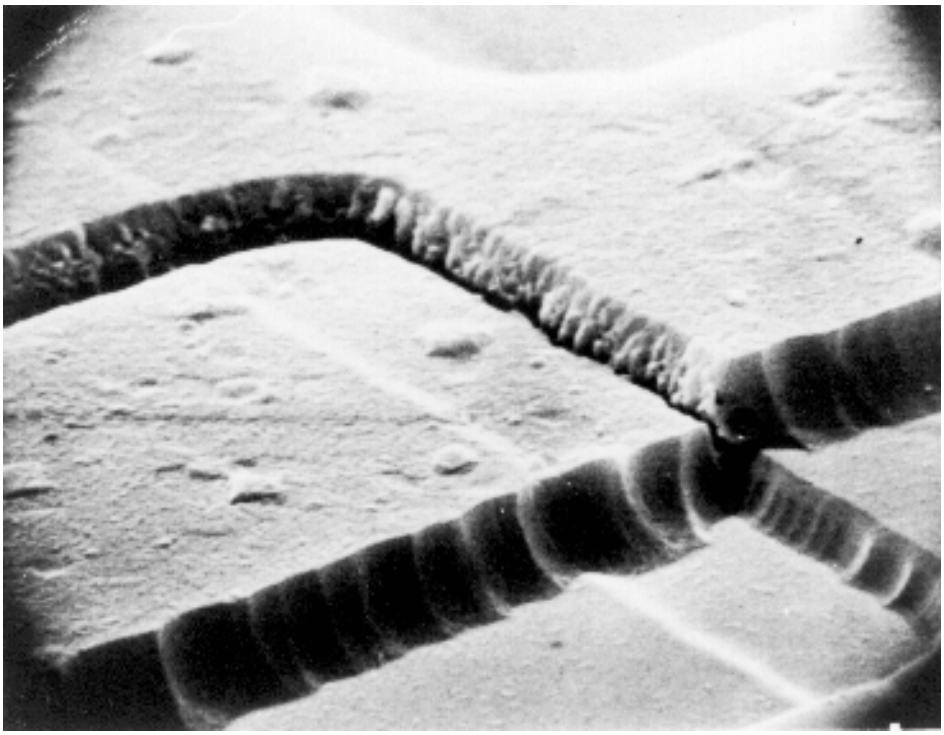

FIGURE 2018-13. 6,000X.
Crack-like defect at passivation step (reject).

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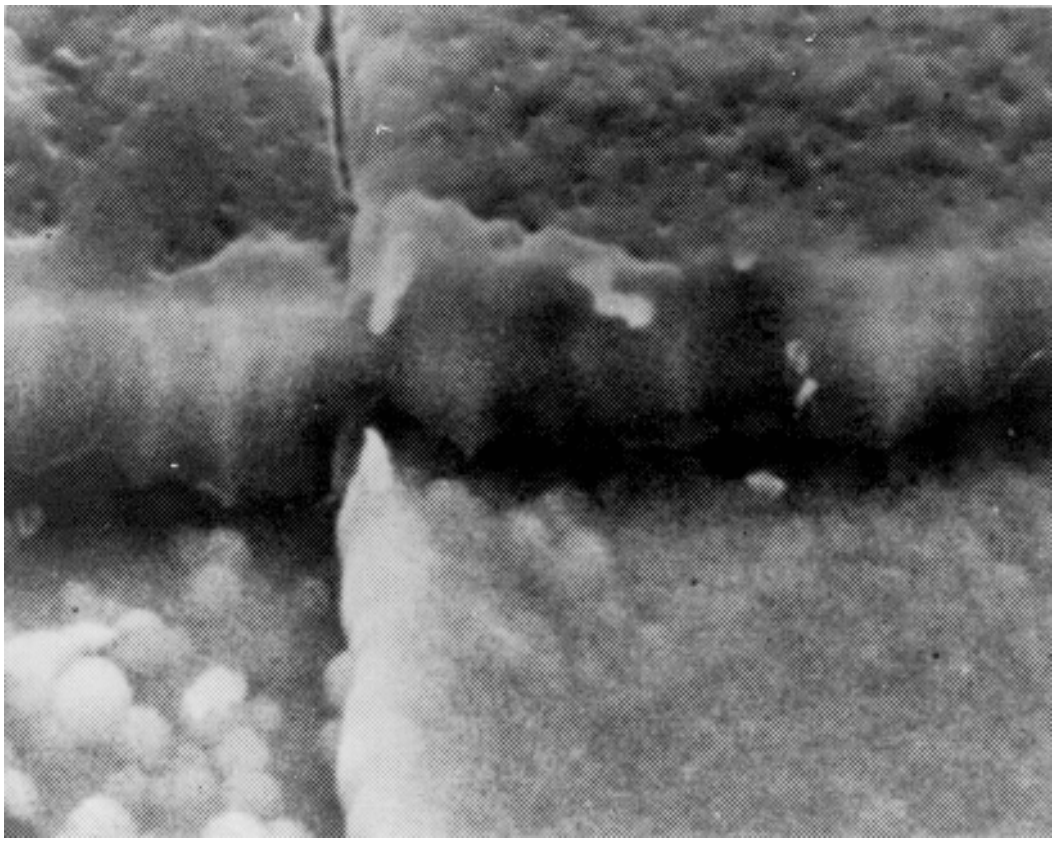

FIGURE 2018-14. (7,200X).
Thinning at passivation step with more than 50 percent of cross-sectional area remaining at step (multi-level metal) (accept).

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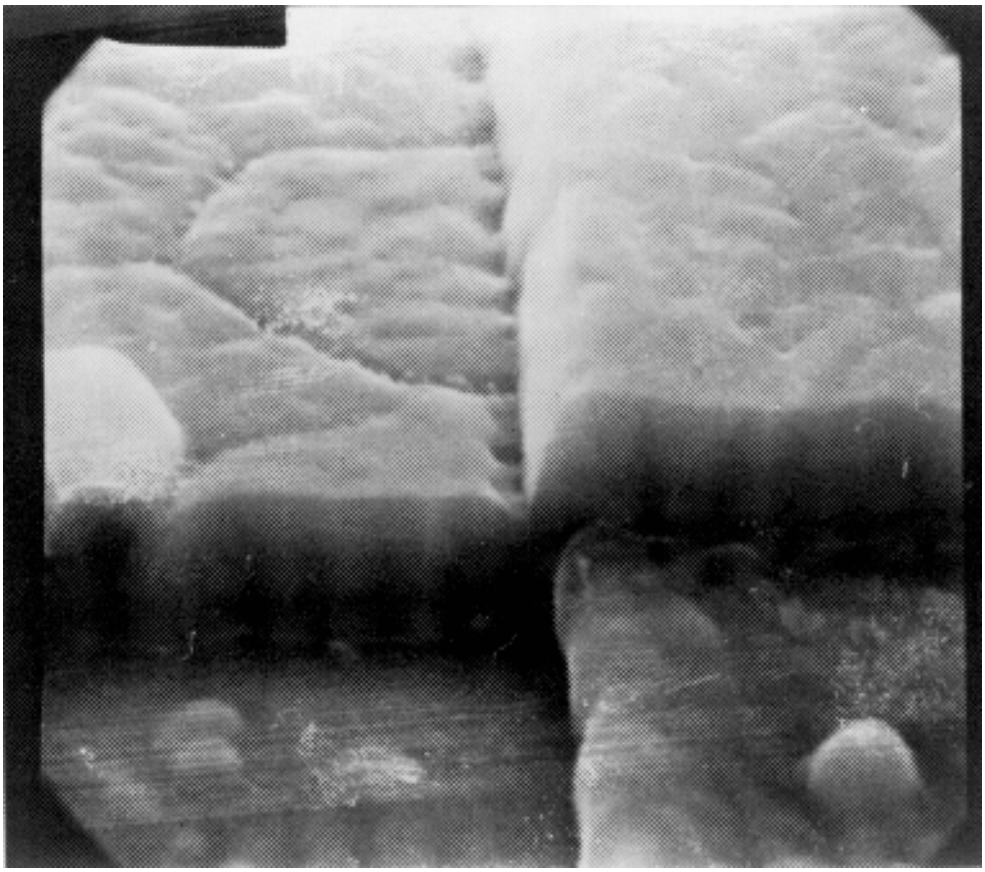

FIGURE 2018-15. 7,200X.
Thinning at passivation step with less than 50 percent of cross-sectional area remaining at step (multi-level metal) (reject).

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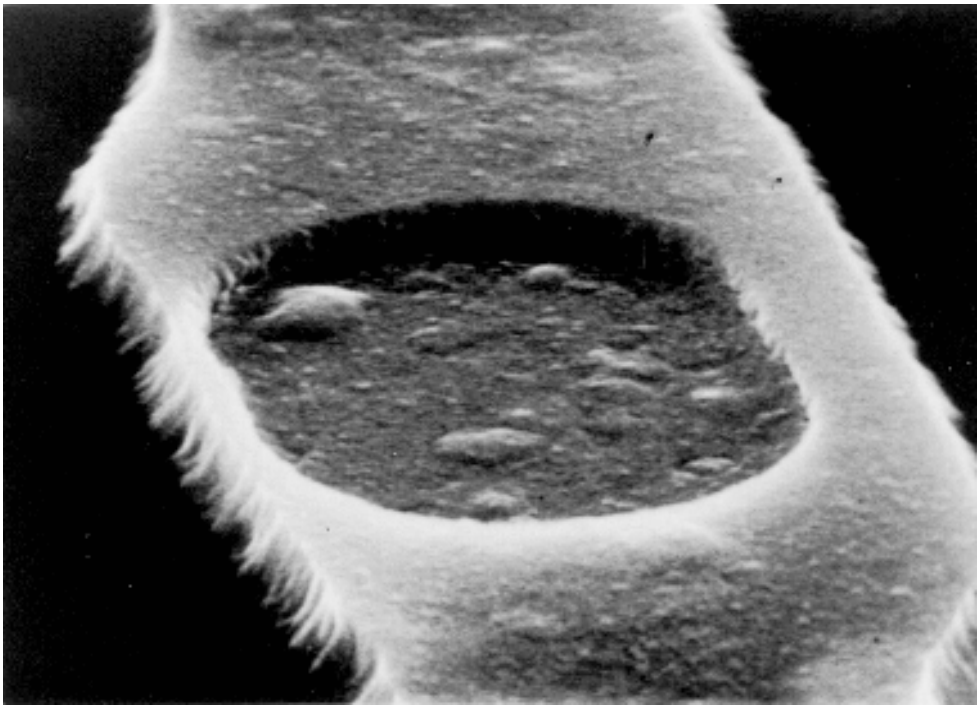

FIGURE 2018-16. (6,000X).
Steep passivation step (MOS) (accept).

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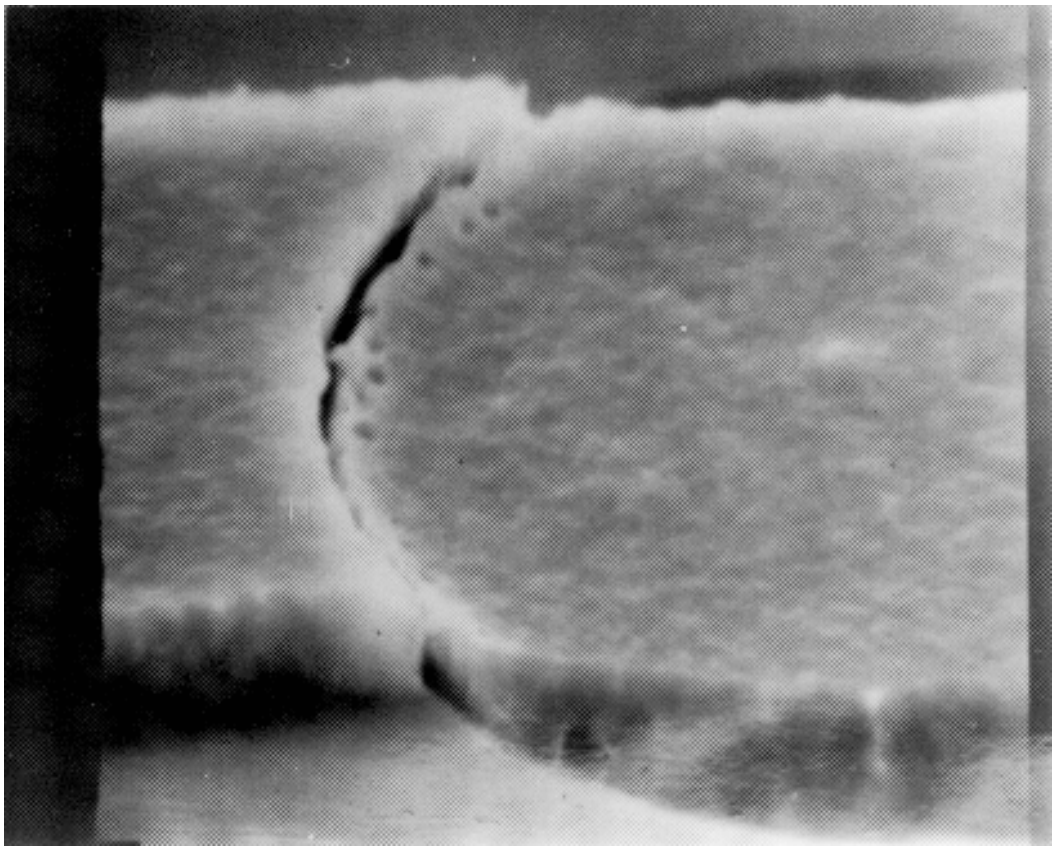

FIGURE 2018-17. 9,500X.
Steep passivation step (MOS) (reject).

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FIGURE 2018-18. (5,000X).
Peeling or lifting general metallization
in contact window area (reject).

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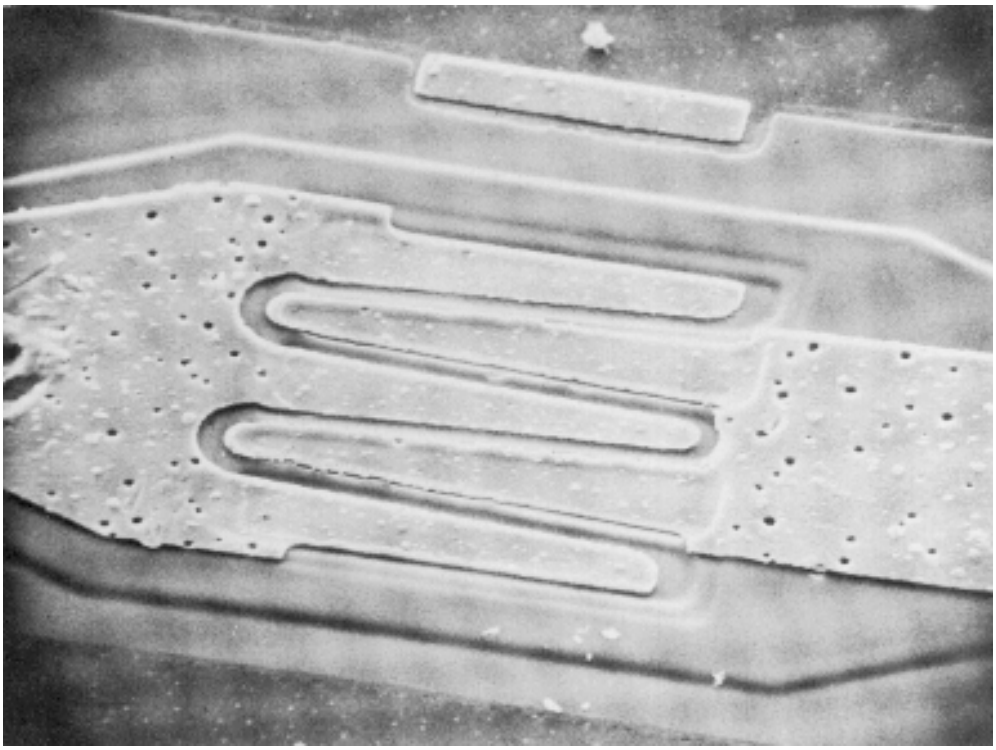

FIGURE 2018-19. 10,000X.
General metallization voids (accept).

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FIGURE 2018-20. (5,000X).
General metallization voids (reject).

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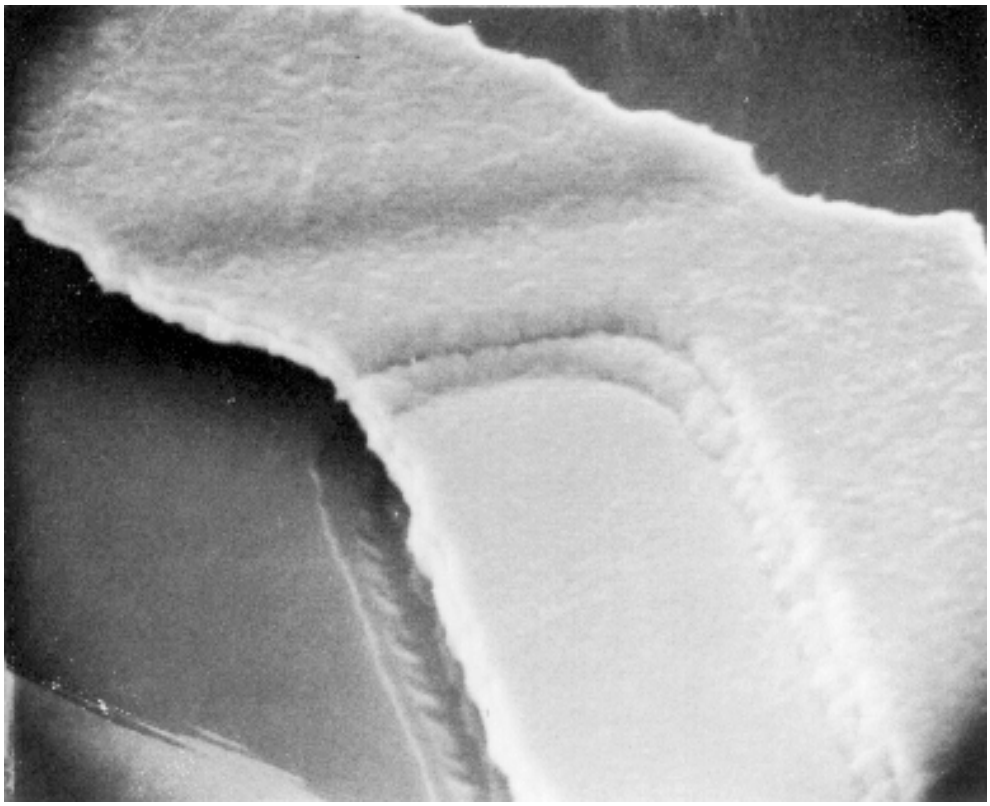

FIGURE 2018-21. 5,000X.
Etch-back/undercut type of notch at
passivation step (multi-layered metal) (accept).

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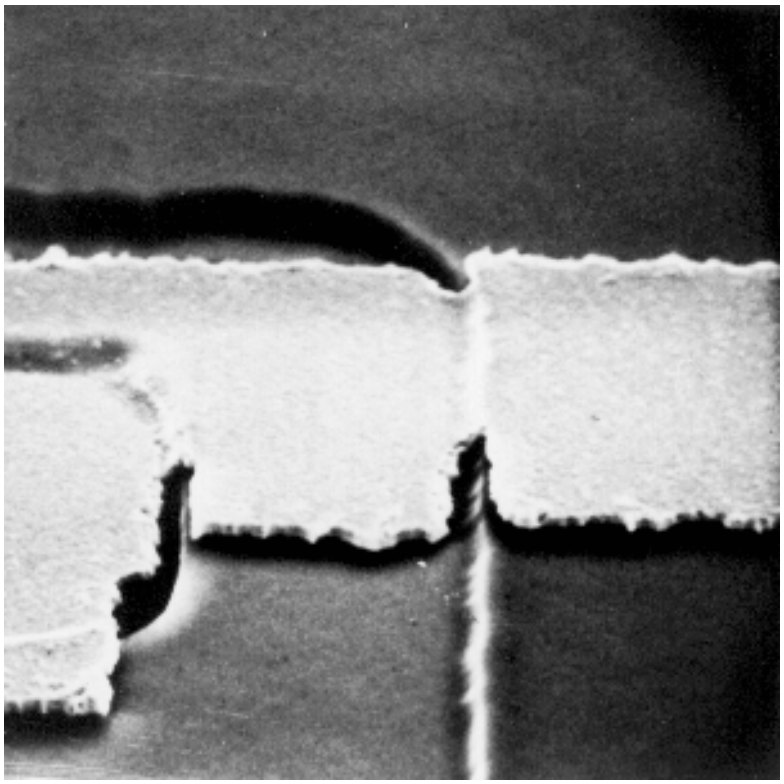

FIGURE 2018-22. (5,000X).
Barrier or adhesion layer etch-back/undercut type of notch at passivation step (multi-layered metal) (accept).

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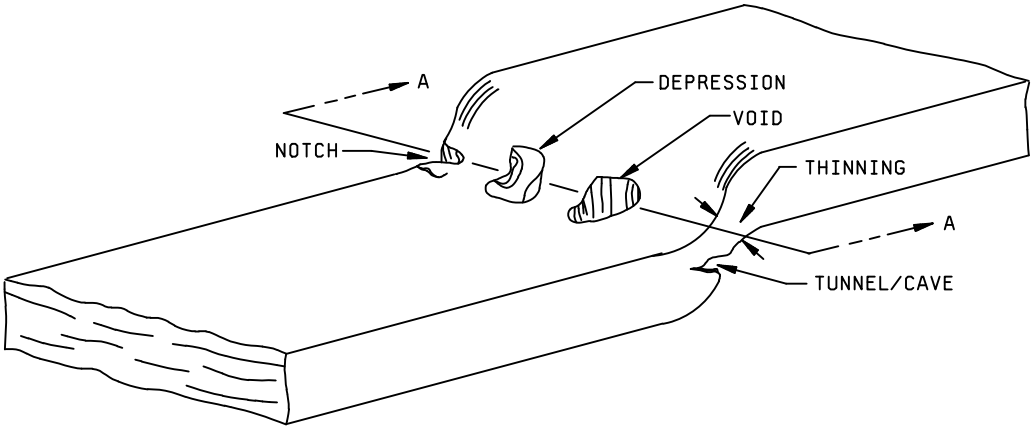
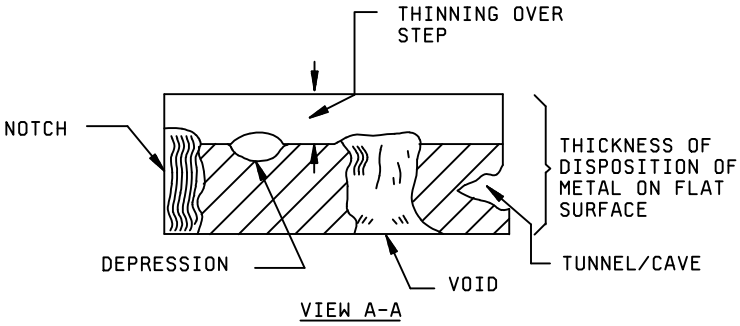


METALLIZATION AT PASSIVATION
STEP SHOWING TYPICAL DEFECTS



CROSS-SECTION AREA (ENLARGED) OF METALLIZATION
AT PASSIVE STEP SHOWN ABOVE

FIGURE 2018-23. Concept of reduction of cross-sectional area of metallization as accept/reject criteria(any combination of defects and thinning over a step which reduces the cross-sectional area of the metal to less than the percentage defined within 3.7.2 of metal cross-sectional area as deposited on the flat surface) is cause for rejection.

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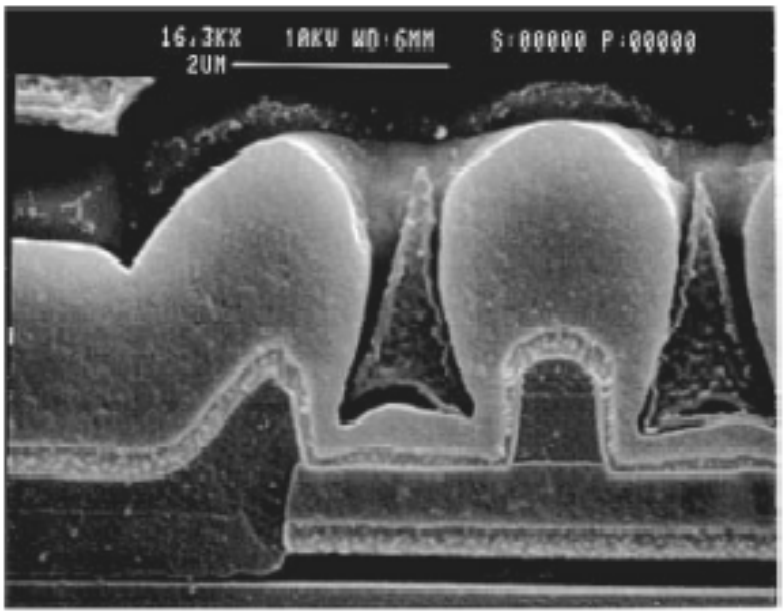

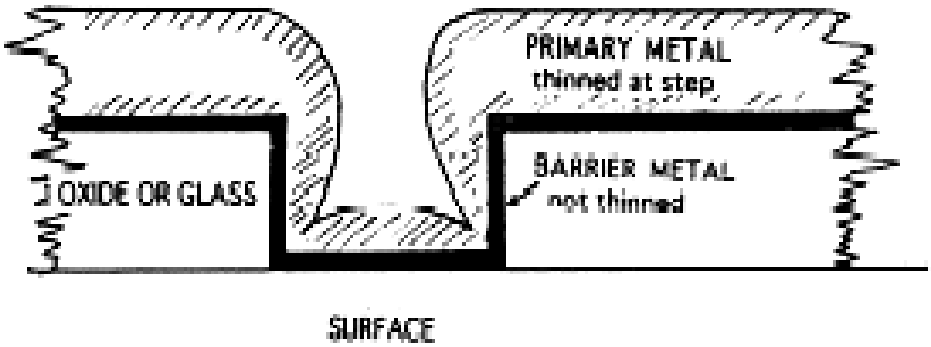

Figure 2018.24 20% metallization coverage (barrier metal inclusive)

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APPENDIX A

Metal integrity alternate to SEM inspection

10. PURPOSE. Metal integrity is achieved through a system of designing and building in quality and reliability. It is not practical or cost effective to rely solely on end-of-line testing to ensure metal integrity. This procedure provides a system for designing, building, and monitoring a metal system that withstands the operating conditions of the device for the specified lifetime.

20. SCOPE.

20.1 Utilization of this method provides an alternate to the requirements defined in TM2018. This procedure must be used in conjunction with the requirements of alternate 2 of TM5004, paragraph 3.3.1 as it applies to metallization.

20.2 This procedure describes a method by which metal integrity is assured through a combination of design rules and techniques, process development, manufacturing controls and end-of-line screening and reliability testing.

20.2.1 Design controls.

a. Reliability rules.

b. Layout rules.

c. Rules checking.

d. Process development.

20.2.2 Manufacturing controls. Statistical control of the manufacturing process and equipment defect and foreign material control.

20.2.3 Reliability testing. Accelerated tests.

30. DEFINITIONS.

Lifetime. The mean time to failure of a technology at operating conditions defined to be normal. The mean time to failure is measured on a large sample of devices stressed at temperatures and current densities well above the normal operating conditions and extrapolated to normal operating temperature and current density.

Current density. The maximum allowable current density calculated as described in appendix A of MIL-PRF-38535.

Specification limits. Minimum or maximum boundaries for the value of a measured parameter. Material whose measured values are beyond these boundaries must be reviewed and dispositioned.

Worst case operating conditions. Conditions of current and temperature at which a device would normally operate, that would result in the greatest likelihood of failure.

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APPENDIX A

40. REQUIREMENTS.

40.1 Design controls. Design includes device design and process development. Device design includes all steps and supporting systems needed to translate a functional description for a device into a pattern generating data base. Process development includes selection of materials, tooling, and process conditions that may significantly affect metal integrity. The design process is a major consideration in establishing metal integrity.

40.1.1 A manufacturer's design system must include controlled, documented rules based on the manufacturer's processing capabilities. These rules shall specify feature size and spacing requirements, taking into account size changes that occur during processing. Manufacturers shall be able to justify their rules based on expected process variations. In addition, documented reliability rules shall exist which establish the electrical characteristics for each technology, taking into account processing materials, tolerances and limitations. The manufacturer shall have a system for checking designs for rule violations, and a system for correcting violations. Design rules shall consider the maximum current density (calculated as described in appendix A of MIL-PRF-38535) which shall be determined using worst case operating conditions and taking into consideration current crowding at contacts and vias. The manufacturer shall ensure that worst case processing conditions (such as alignment, metal thickness, line width, and contact/via size) do not result in violation of current density. Current density for a technology shall be at a level such that there is sufficient margin to ensure that failure will not result from electromigration in the specified lifetime of the device.

40.1.2 Process development. The manufacturer's design must take into consideration known levels of defects in the process. The process developed by the manufacturer must produce metallization that has the electrical and mechanical properties consistent with the design rules of 40.1.1, and reliability goals for the technology. Mechanical stress in the metal after final processing shall be understood. The manufacturer shall demonstrate, with results from appropriate designed experiments, that the desired electrical and mechanical properties have been achieved, and that the interaction of other process parameters on metal integrity parameters (minimum list in 40.2) is understood. The initial process specification limits shall be chosen such that metal integrity parameters are within the capability of the process. The manufacturer shall have a change control system in place such that new or changed processes are not put into production without the appropriate reliability evaluation.

40.2 Manufacturing controls. The manufacturer shall establish manufacturing controls in order to achieve uniformly good quality and reliability in their metal system, and to assure that the product is being manufactured according to the assumptions made during design. The manufacturer shall determine which parameters are critical to metal integrity and control those parameters in accordance with TechAmerica EIA-557. The manufacturer shall be able to demonstrate control of metal thicknesses, step coverage and cross-sectional areas, metal line width, contact and via sizes, contact and via resistance, and sheet resistance as a minimum, and show that they are being controlled to limits that are consistent with the way the metal system was designed. Specification limits shall be established for these parameters. In addition, defects that threaten metal integrity must be controlled in accordance with the alternate visual procedure (alternate 2) in appendix A of TM5004.

40.3 Reliability testing. While it is desirable to design in and build in reliability rather than to achieve reliability by screening finished product, there is valuable information to be gained from screening and reliability testing. Screening test such as burn-in not only eliminate the weaker parts in a population, but also provide information on failure mechanisms which can be used to improve design, materials, processes, or electrical test. Similarly, accelerated testing is used to speed up failure mechanisms likely to occur under normal operating conditions of a device. These failure mechanisms can then be analyzed to provide a basis for improvement. Accelerated test that a manufacturer may use to this end include but are not limited to electromigration testing, life testing, temperature-humidity-bias testing, and temperature cycling. Structures used in accelerated test must be typical of the technology represented. Failure mechanisms experienced during accelerated testing must be typical of those experienced during normal use of the device.

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40.3.1 Reliability evaluating. The manufacturer must have in place a system for evaluating the reliability of the metal system. The system shall enable the manufacturer to determine the probability of failure in a given lifetime. The lifetime and failure rate data of the metal system associated with a given technology shall be made available to the customer. The manufacturer's systematically collected data must indicate that there is a high probability of meeting the specified lifetimes and/or failure rates.

50. DOCUMENTATION.

NOTE: Certain information considered proprietary may only be available under non-disclosure agreement.

50.1 The manufacturer must have available for customer review controlled reliability rules, layout rules, and current density for each technology for which this procedure is used. In addition, the manufacturer must have available for review the method by which the above rules are checked and verified.

50.2 The manufacturer shall be able to demonstrate the manufacturing controls and system for disposition of out of control occurrences that are in place to control the processes determined critical to metal integrity.

50.3 The manufacturer must have available for customer review any testing performed to evaluate the reliability of the metal system.

50.4 The manufacturer shall specify the metal lifetime to the customer upon request.

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METHOD 2019.10

DIE SHEAR STRENGTH

1. PURPOSE. The purpose of this test is to determine the integrity of materials and procedures used to attach semiconductor die or surface mounted passive elements to package headers or other substrates. This determination is based on a measure of force applied to the die, the type of failure resulting from this application of force (if failure occurs) and the visual appearance of the residual die attach media and substrate/header metallization.

2. APPARATUS. The test equipment shall consist of a load-applying instrument with an accuracy of ±5 percent of full scale or 50 grams, whichever is the greater tolerance. A circular dynamometer with a lever arm or a linear motion force- applying instrument may be used to apply the force required for testing. The test equipment shall have the following capabilities:

a. A die contact tool which applies a uniform distribution of the force to an edge of the die (see figure 2019-1). A compliant (conforming) material (e.g., nail polish, tape, etc.) may be applied to the face of the contact tool to ensue uniform force distribution on the edge of the die.

b. Provisions to assure that the die contact tool is perpendicular to the die mounting plane of the header or substrate.

c. A rotational capability, relative to the header/substrate holding fixture and the die contact tool, to facilitate line contact on the edge of the die; i.e., the tool applying the force to the die shall contact the die edge from end-to-end (see figure 2019-2).

d. A binocular microscope with magnification capabilities of 10X minimum and lighting which facilitates visual observation of the die and die contact tool interface during testing.

3. PROCEDURE. The test shall be conducted, as defined herein, or to the test conditions specified in the applicable specific acquisition document consistent with the particular part construction. All die strength tests shall be counted and the specific sampling, acceptance, and added sample provisions shall be observed, as applicable.

3.1 Shear strength. A force sufficient to shear the die from its mounting or equal to twice the minimum specified shear strength (figure 2019-4), whichever occurs first, shall be applied to the die using the apparatus of 2 above.

NOTE: For passive elements only attached at the end terminations, the area used to determine the force applied shall be the total area of the mounting surface of the end terminations. An area between end terminations filled with non-adhering filler shall not be used to determine the force applied. However, any adhering material applied between the end terminations shall be used in the shear calculation. If the area between end terminations contains an adhering material, then the area of the adhering material shall be added to the area of the mounting surfaces of the end terminations and that total area shall be used to determine the force applied.

a. When a linear motion force-applying instrument is used, the direction of the applied force shall be parallel with the plane of the header or substrate and perpendicular to the die being tested.

b. When a circular dynamometer with a lever arm is employed to apply the force required for testing, it shall be pivoted about the lever arm axis and the motion shall be parallel with the plane of the header or substrate and perpendicular to the edge of the die being tested. The contact tooling attached to the lever arm shall be at a proper distance to assure an accurate value of applied force.

c. The die contact tool shall apply a force gradually from zero to a specified value against an edge of the die which most closely approximates a 90° angle with the base of the header or substrate to which it is bonded (see figure 2019-3). For rectangular die, the force shall be applied perpendicular to the longer side of the die. When constrained by package configurations, any available side of the die may be tested if the above options are not available.

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d. After initial contact with the die edge and during the application of force, the relative position of the contact tool shall not move vertically such that contact is made with the header/substrate or die attach media. If the tool rides over the die, a new die may be substituted or the die may be repositioned, provided that the requirements of 3.1.c are met.

3.2 Failure criteria. A device which fails any of the following criteria shall constitute a failure.

NOTE: (See examples for determining DIE AREA following figure 2019-4.)

3.2.1 Epoxy attach.

a. Fails die strength requirements (1.0X) of Figure 2019-4.

b. Separation occurs with a strength greater than the minimum (1.0X) specified in Figure 2019-4, but with less than 2.0 times that strength and evidence that less than 75 percent of the die to substrate contact area contained attach medium coverage. Evidence of adhesion will be in the form of attach medium to the intended area on the substrate, the element or combination of both.

NOTE: Residual element material (silicon or other) attached in discrete areas of the die attach medium shall be considered as evidenced of adhesion.

3.2.2 Eutectic, solder, and other attach.

a. Fails die strength requirements (1.0X) of Figure 2019-4.

b. Separation occurs with a strength greater than or equal to the minimum (1.0X) specified in Figure 2019-4, but with less than 1.25 times that strength and evidence that less than 50 percent of the die to substrate contact area contained attach medium coverage. Evidence of adhesion will be in the form of attach medium to the intended area on the substrate, the element or combination of both.

c. Separation occurs with a strength greater than or equal to the 1.25X specified in Figure 2019-4, but with less than 2.0 times that strength and evidence that less than 10 percent of the die to substrate contact area contained attach medium coverage. Evidence of adhesion will be in the form of attach medium to the intended area on the substrate, the element or combination of both

NOTE: Residual element material (silicon or other) attached in discrete areas of the die attach medium shall be considered as evidence of adhesion. For metal glass die attach, die attach material on the die and on the package base shall be considered as evidence of acceptable adhesion.

3.2.3 Separation categories. When specified, the force required to achieve separation and the category of the separation shall be recorded.

a. Shearing of die with residual silicon remaining.

b. Separation of die from die attach medium.

c. Separation of die and die attach medium from package.

4. SUMMARY. The following details shall be specified in the applicable acquisition document.

a. Minimum die attach strength if other than shown on figure 2019-4.

b. Number of devices to be tested and the acceptance criteria.

c. Requirement for data recording, when applicable (see 3.2.1).

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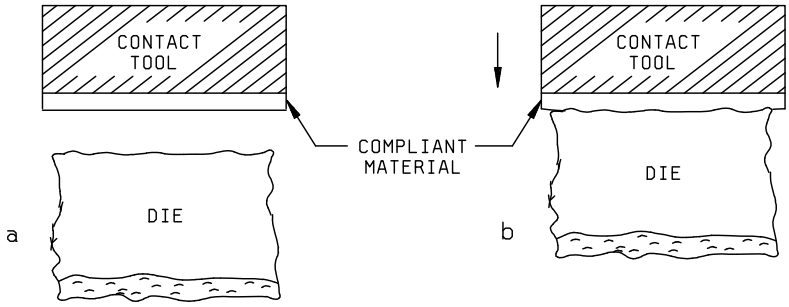

FIGURE 2019-1. Compliant interface on contact tool distributes load to the irregular edge of the die.

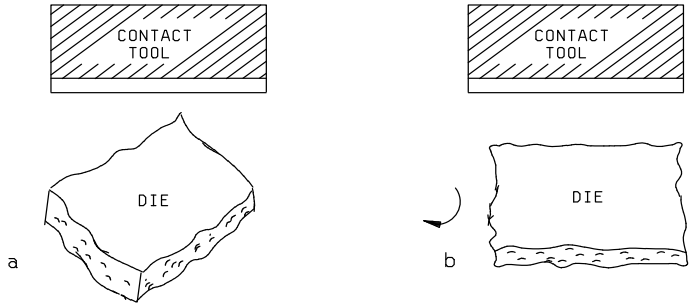

FIGURE 2019-2. Rotate the die contact tool or the device for parallel alignment.

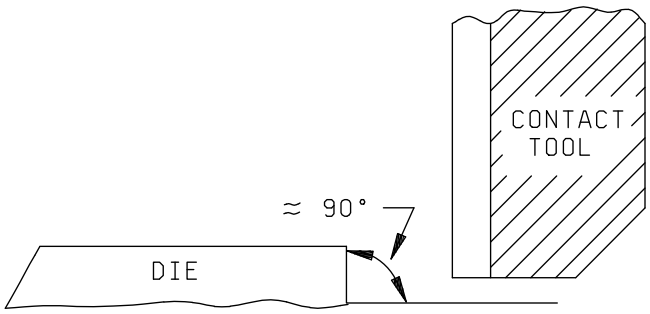

FIGURE 2019-3. The contact tool shall load against that edge of the die which forms an angle ≈ 90° with the header/substrate.

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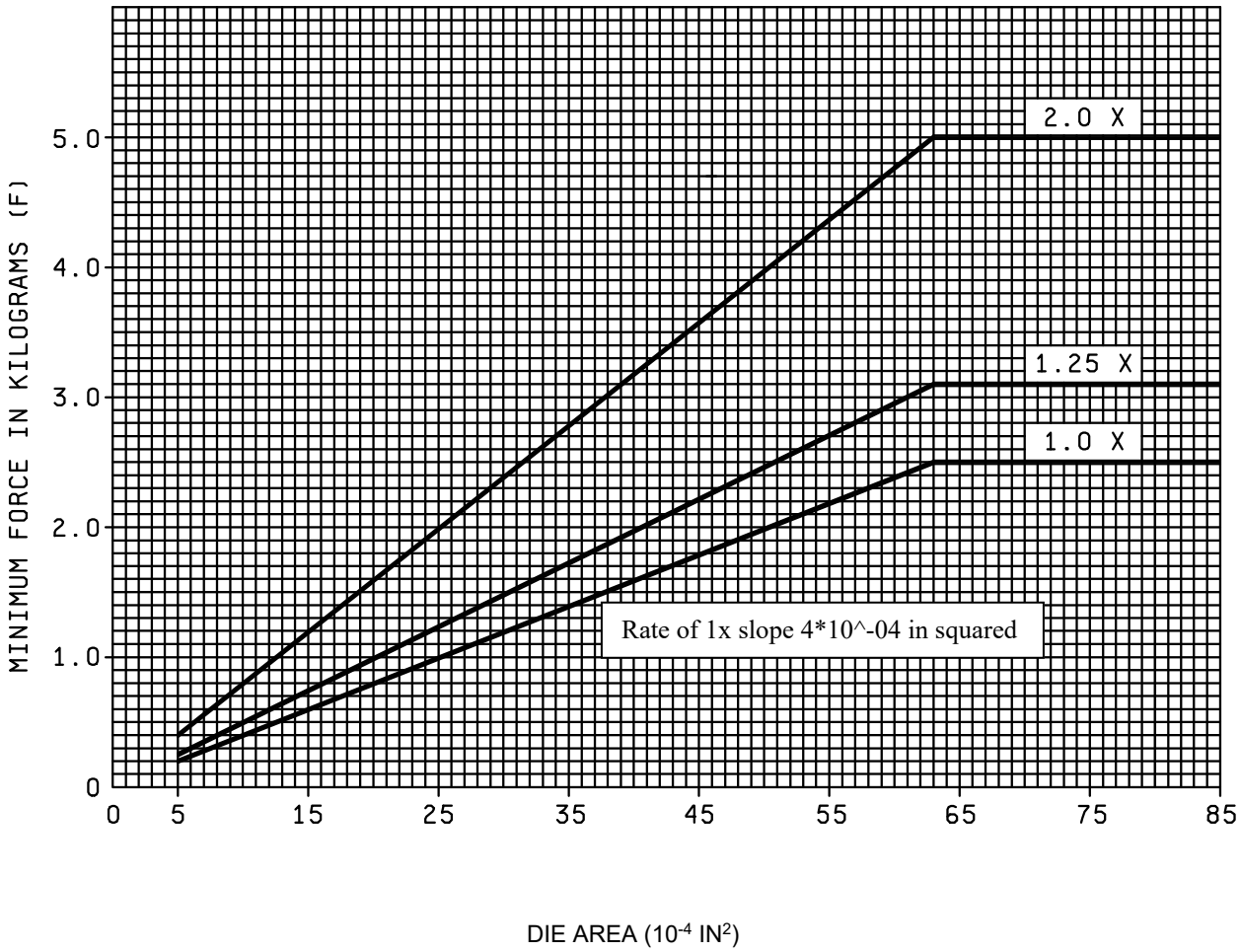

NOTES:

1. All die area larger than 64 x 10^{-4} $(IN)^2$ shall withstand a minimum force of (1.0X) of 2.5 kg or a minimum force (2.0X) of 5.0 kg (see 3.2).

2. All die area larger than or equal to 5 x 10^{-4} $(IN)^2$ but smaller than or equal to 64 x 10^{-4} $(IN)^2$ shall withstand a minimum force as determined from the chart of Figure 2019.4. The chart is based on a force of 0.04 kg for every one ten-thousandth (10-4) square inch at (1X) level. Similarly, the required minimum force is 0.05 kg for every 10-4 IN2 at (1.25X) level and is 0.08 kg for every 10-4 IN2 at (2X) level.

3. All die area smaller than 5 x 10-4 (IN)2 shall withstand a minimum force (1.0X) of 0.04 kg or a minimum force (2X) of 0.08 kg.

4. (1X) and (2X) values apply to all attach methods, (1.25X) values apply to all attach methods except epoxy attach.

FIGURE 2019-4. Die shear strength criteria (minimum force versus die attach area).

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Examples of determining die strength requirements based on die area.

Example 1:

Die Area of device measuring .02 inches by .02 inches.

Die Size = .02 X .02 = .0004 IN^2 = 4 X 10^{-4} (IN^2).

Because die size is less than 5 X 10^{-4} (IN^2) use Note 3 which states the value of minimum force required is 0.04 kg/10^{-4} (IN^2) at (1X), 0.05 kg/10^{-4} (IN^2) at (1.25X), or 0.08 kg/10^{-4} (IN^2) at (2X). Thus the associated minimum forces required are 0.16 kg, 0.20 kg and 0.32 kg, respectively.

Example 2:

Die Area of device measuring .04 inches by ~~0~~.04 inches.

Die Size = .04 X .04 = .0016 IN^2 = 16 X 10^{-4} (IN^2).

Because die size is between 5 X 10^{-4} (IN^2) and 64 X 10^{-4} (IN^2) use Note 2 which states the value of minimum force required is to be determined based on the chart. The values for die size 16 X 10^{-4} (IN^2) are found on the chart by reading 16 on the (10^{-4} IN^2) scale, then finding the coordinating force value on the (F) scale. Doing so provides minimum forces required as .64 kg at (1X), .80 kg at (1.25X), and 1.28 kg at (2X).

Alternately: The chart is based on using .04 kg/10^{-4} (IN^2) at (1X), .05 kg/10^{-4} (IN^2) at (1.25X), and .08 kg/10^{-4} (IN^2) at (2X). Thus: the minimum forces required are 16 X .04 = .64 kg (1X), 16 X .05 = .80 kg (1.25X), and 16 X .08 = 1.28 kg (2X).

Example 3:

Die Area of device measuring .09 inches by .09 inches.

Die Size = .09 X .09 = .0081 IN^2 = 81 X 10^{-4} (IN^2).

Because die size is larger than 64 X 10^{-4} (IN^2) use Note 1 which states the value of minimum force required is 2.5 kg or a multiple thereof. Therefore, the minimum forces required are 2.5 kg at (1X), 3.125 kg at (1.25X), and 5.0 kg at (2X).

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METHOD 2020.9

PARTICLE IMPACT NOISE DETECTION TEST

1. PURPOSE. The purpose of this test is to detect loose particles inside a device cavity. The test provides a nondestructive means of identifying those devices containing particles of sufficient mass that, upon impact with the case, excite the transducer.

2. APPARATUS. The equipment required for the particle impact noise detection (PIND) test shall consist of the following (or equivalent):

a. A threshold detector to detect particle noise voltage exceeding a preset threshold of the absolute value of 15 ±1 millivolt peak reference to system ground.

b. A vibration shaker and driver assembly capable of providing essentially sinusoidal motion to the device under test (DUT) at:

(1) Condition A: 20 g peak at 40 to 250 Hz.

(2) Condition B: 10 g peak at 60 Hz minimum.

c. PIND transducer, calibrated to a peak sensitivity of -77.5 ±3 dB in regards to one volt per microbar at a point within the frequency of 150 to 160 kHz.

d. A sensitivity test unit (STU) (see figure 2020-1) for periodic assessment of the PIND system performance. The STU shall consist of a transducer with the same tolerances as the PIND transducer and a circuit to excite the transducer with a 250 microvolt ±20 percent pulse. The STU shall produce a pulse of about 20 mV peak on the oscilloscope when the transducer is coupled to the PIND transducer with attachment medium.

e. PIND electronics, consisting of an amplifier with a gain of 60 ±2 dB centered at the frequency of peak sensitivity of the PIND transducer. The noise at the output of the amplifier shall not exceed 10 mV peak.

f. Attachment medium. The attachment medium used to attach the DUT to the PIND transducer shall be the same attachment medium as used for the STU test.

g. Shock mechanism or tool capable of imparting shock pulses of 1,000 ±200 g peak to the DUT. The duration of the main shock shall not exceed 100 μs. If an integral co-test shock system is used the shaker vibration may be interrupted or perturbed for period of time not to exceed 250 ms from initiation of the last shock pulse in the sequence. The co-test duration shall be measured at the 50 ±5 percent point.

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3. PROCEDURES.

3.1 Test equipment setup. Shaker drive frequency and amplitude shall be adjusted to the specified conditions based on cavity size of the DUT (for condition A, see table 1 herein). The shock pulse shall be adjusted to provide 1,000 ±200 g peak to the DUT.

3.2 Test equipment checkout. The test equipment checkout shall be performed a minimum of one time per operation shift. Failure of the system to meet checkout requirements shall require retest of all devices tested subsequent to the last successful system checkout.

3.2.1 Shaker drive system checkout. The drive system shall achieve the shaker frequency and the shaker amplitude specified. The drive system shall be calibrated so that the frequency settings are within ±8 percent and the amplitude vibration setting are within ±10 percent of the nominal values. If a visual displacement monitor is affixed to the transducer, it may be used for amplitudes between 0.04 and 0.12 inch (1.02 and 3.05 mm). An accelerometer may be used over the entire range of amplitudes and shall be used below amplitudes of 0.040 inch (1.02 mm).

3.2.2 Detection system checkout. With the shaker deenergized, the STU transducer shall be mounted face-to-face and coaxial with the PIND transducer using the attachment medium used for testing the devices. The STU shall be activated several times to verify low level signal pulse visual and threshold detection on the oscilloscope. Not every application of the STU will produce the required amplitude. All pulses which are greater than 20 mV shall activate the detector.

3.2.3 System noise verification. System noise will appear as a fairly constant band and must not exceed 20 millivolts peak to peak when observed for a period of 30 to 60 seconds.

3.3 Test sequence. The following sequence of operations (a through i) constitute one test cycle or run.

a. 3 pre-test shocks.

b. Vibration 3 ±1 seconds.

c. 3 co-test shocks.

d. Vibration 3 ±1 seconds.

e. 3 co-test shocks.

f. Vibration 3 ±1 seconds.

g. 3 co-test shocks.

h. Vibration 3 ±1 seconds.

i. Accept or reject.

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3.3.1 Mounting requirements. Special precautions (e.g., in mounting, grounding of DUT leads, or grounding of test operator) shall be taken as necessary to prevent electrostatic damage to the DUT.

Batch or bulk testing is prohibited.

Most part types will mount directly to the transducer via the attachment medium. Parts shall be mounted with the largest flat surface against the transducer at the center or axis of the transducer for maximum sensitivity. The DUT shall be placed such that the geometric center of the surface contacting the transducer is centrally located on the transducer to within approximately 2 mm of the transducer surface's geometric center. Where more than one large surface exists, the one that is the thinnest in section or has the most uniform thickness shall be mounted toward the transducer, e.g., flat packs are mounted top down against the transducer. Small axial-lead, right circular cylindrical parts are mounted with their axis horizontal and the side of the cylinder against the transducer. Parts with unusual shapes may require special fixtures. Such fixtures shall have the following properties:

(1) Low mass.

(2) High acoustic transmission (aluminum alloy 7075 works well).

(3) Full transducer surface contact, especially at the center.

(4) Maximum practical surface contact with test part.

(5) No moving parts.

(6) Suitable for attachment medium mounting.

3.3.2 Test monitoring. Each test cycle (see 3.3) shall be continuously monitored, except for the period during co-test shocks and 250 ms maximum after the shocks. Particle indications can occur in any one or combinations of the three detection systems as follows:

a. Visual indication of high frequency spikes which exceed the normal constant background white noise level.

b. Audio indication of clicks, pops, or rattling which is different from the constant background noise present with no DUT on the transducer.

c. Threshold detection shall be indicated by the lighting of a lamp or by deflection of the secondary oscilloscope trace.

3.4 Failure criteria. Any noise bursts as detected by any of the three detection systems exclusive of background noise, except those caused by the shock blows, during the monitoring periods shall be cause for rejection of the device. Rejects shall not be retested except for retest of all devices in the event of test system failure. If additional cycles of testing on a lot are specified, the entire test procedure (equipment setup and checkout mounting, vibration, and co-shocking) shall be repeated for each retest cycle. Reject devices from each test cycle shall be removed from the lot and shall not be retested in subsequent lot testing.

3.5 Screening lot acceptance. Unless otherwise specified, the inspection lot (or sublot) to be screened for lot acceptance shall be submitted to 100 percent PIND testing a maximum of five times in accordance with condition A herein. PIND prescreening shall not be performed. The lot may be accepted on any of the five runs if the percentage of defective devices in that run is less than 1 percent and the cumulative number of defective devices does not exceed 25 percent. All defective devices shall be removed after each run. Resubmission is not allowed.

Note: If the lot count is 100 devices or fewer, or reaches 100 devices or fewer following a run, then no failures are allowed for any subsequent runs to be acceptable.

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TABLE I. Package Height vs.Test Frequency for 20g Acceleration (condition A).

Note: The shaker drive test frequency (F) for condition A (see 3.1) is determined by the package internal cavity height using the following formula:

$$F = \sqrt{20 / [(D) X (0.0511)]}$$

where: D = Average internal package height (in inches).
20 is a constant in this application and is equal to sinusoidal acceleration of 20g.
F is the shaker drive test frequency (in Hz)

Note: The use of this formula is to be limited to frequencies in the range of 40 - 150 Hz and should not be used for package heights giving frequencies outside this range unless a frequency outside this range is approved by the acquiring activity.

Based on the formula above, the following table is generated to show some typical values:

Average Internal Cavity Height (D)			Test Frequency
Mils	mm	inches	Hz
18	.46	0.018	147
30	0.76	0.030	114
40	1.02	0.040	99
50	1.27	0.050	88
60	1.52	0.060	81
70	1.78	0.070	75
80	2.03	0.080	70
90	2.29	0.090	66
100	2.54	0.100	63
110	2.79	0.110	60
250	6.35	0.250	40

Note: The approximate average internal package height (D) shall be measured from the floor of the package cavity or the top of the major substrate for hybrid or multi-chip assemblies and shall exclude the thickness of the die mounted inside the package.

Example calculation: Assume an average internal cavity height of 70 Mils.

$$F = \sqrt{20 / [(D) X (0.0511)]}$$

D = 70 Mils converted to inches = .070 inches.

$$F = \sqrt{20 / [(.070) X (0.0511)]} = \sqrt{20 / [.00358]} = \sqrt{5586} = 75 \text{ Hz}$$

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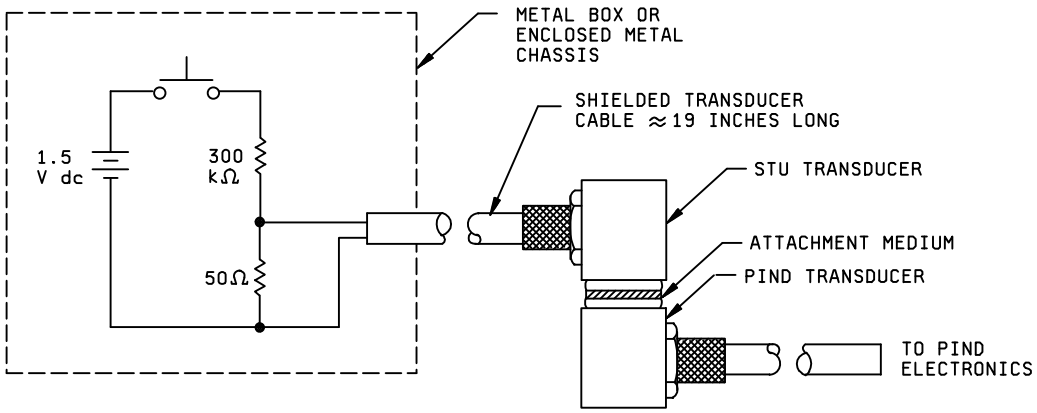
4. SUMMARY. The following details shall be specified in the applicable acquisition document:

a. Test condition letter A or B.

b. Lot acceptance/rejection criteria (if other than specified in 3.5).

c. The number of test cycles, if other than one.

d. Pre-test shock level and co-test shock level, if other than specified.



NOTES:
1. Pushbutton switch: Mechanically quiet, fast make, gold contacts. E.G. T2 SM4 microswitch.
2. Resistance tolerance 5 percent noninductive.
3. Voltage source can be a standard dry cell.
4. The coupled transducers must be coaxial during test.
5. Voltage output to STU transducer 250 microvolts, ±20 percent.

FIGURE 2020-1 Typical sensitivity test unit.

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METHOD 2021.3

GLASSIVATION LAYER INTEGRITY

1. PURPOSE. The purpose of this test is to assess the structural quality of deposited dielectric films (e.g., CVD, sputtered or electron beam evaporated glass or nitride, etc.) over aluminum metallized semiconductor devices or microcircuits. The test is directed at identifying process and materials related glass layer defects which result in localized contamination buildup and loss of the advantage given to properly glassivated devices in terms of electromigration behavior at elevated temperature and current density. This is a destructive test.

2. APPARATUS. The apparatus for this test shall consist of suitable sample handling and chemical etching facilities as required for personnel safety. Standard optical microscopes such as those employed in method 2010 shall be used for device inspection. Standard A.C.S. Reagent Grade chemicals shall be used as etchant materials.

3. PROCEDURE. Unless otherwise specified, this test shall be applied to devices which have been through the complete assembly cycle including final package seal. Packaged devices shall be mechanically delidded with minimum thermal stresses applied. Unless otherwise specified, the test sample shall consist of a minimum of one device selected randomly from the inspection lot. One of the following etching procedures shall be used.

3.1 Procedure A. Delidded sample devices shall be completely immersed in the following aluminum etch:

40 Volumes H_3PO_4 (85%)

19 Volumes H_20

4 Volumes HNO_3 (70%)

This solution shall be maintained at a temperature of 50°C ±5°C.

Devices shall be examined during the etching procedure with an optical system, such as a monocular, binocular or stereomicroscope compatible with observation of the immersed samples. Devices shall be etched for twice the amount of time required to completely remove aluminum metallization from exposed bonding pads.

Properly etched devices shall be removed from the heated solution, rinsed in distilled water, and blown dry with compressed air or other suitable gas streams.

Final optical inspection after etching and drying shall be performed at a magnification of 100X minimum.

3.2 Procedure B. Delidded sample devices shall be completely immersed for 20 to 30 minutes at room temperature in the following aluminum etch:

5 Volumes $HN0_3$ (70%)

80 Volumes H_3P0_4 (85%)

5 Volumes Acetic Acid

10 Volumes Deionized Water

NOTE: The use of a commercial equivalent (e.g., Mity Etch 2) is acceptable.

Properly etched devices shall be removed from the solution, rinsed in distilled water, and blown dry with compressed air or other suitable gas streams.

Final optical inspection after etching and drying shall be performed at a magnification of 100X minimum.

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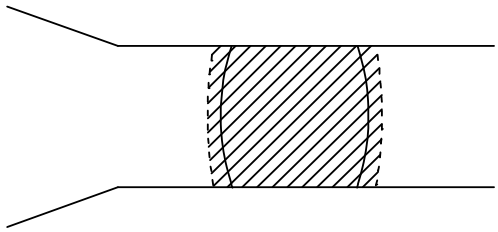

FIGURE 2021-1. Category A - missing glassivation over aluminum.

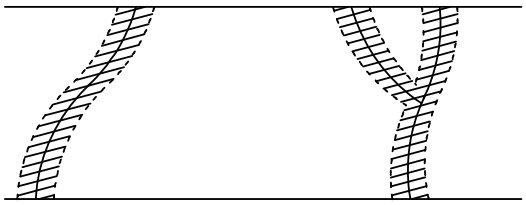

FIGURE 2021-2. Category B - cracks in glass over aluminum.

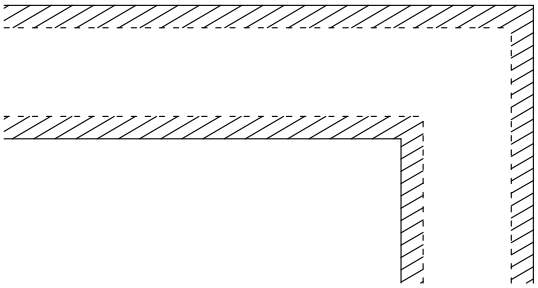

FIGURE 2021-3. Category C - cracks in glass or improper glass coverage along edge of aluminum.

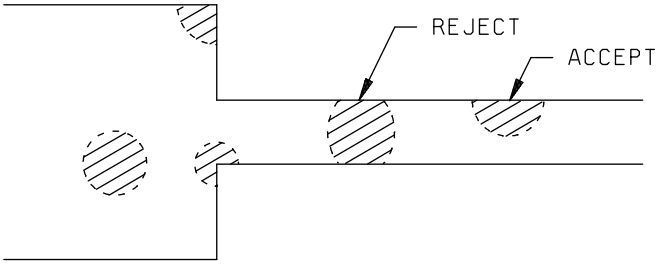

FIGURE 2021-4. Category D - pinholes in glass on top surface and edges of aluminum.

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3.2.1 Failure criteria. Lot rejection shall be based on the appearance of etched aluminum, as shown on figures 2021-1 to 2021-7, at any location other than along the edges immediately adjacent to intentionally unglassed areas (e.g., bonding pads, die edge, scribe line, etc.) (see 4). This criteria shall be applied only to the interconnect levels which exceed a calculated current density of 2×10^5 A/cm^2. Category C and D defects, shown on figures 2021-3, -4, -6, and -7 shall not be a cause for rejection unless aluminum is completely removed from the entire width of the conductor stripe. Etched aluminum is determined by changes in the reflecting properties or transparent appearance of areas normally covered with glassivated aluminum.

Failures shall be recorded in terms of the number of devices tested (if other than one) and the number of failures by failure category as defined below:

4. SUMMARY. The following details shall be specified in the applicable acquisition document:

a. When applicable, any intentional omission of glass over the aluminum metallization layer (see 3.1).

b. If applicable, specific magnification requirements other than as stated in 3.

c. Sample size if other than one (see 3).

d. If applicable, special reporting requirements (see 3.1).

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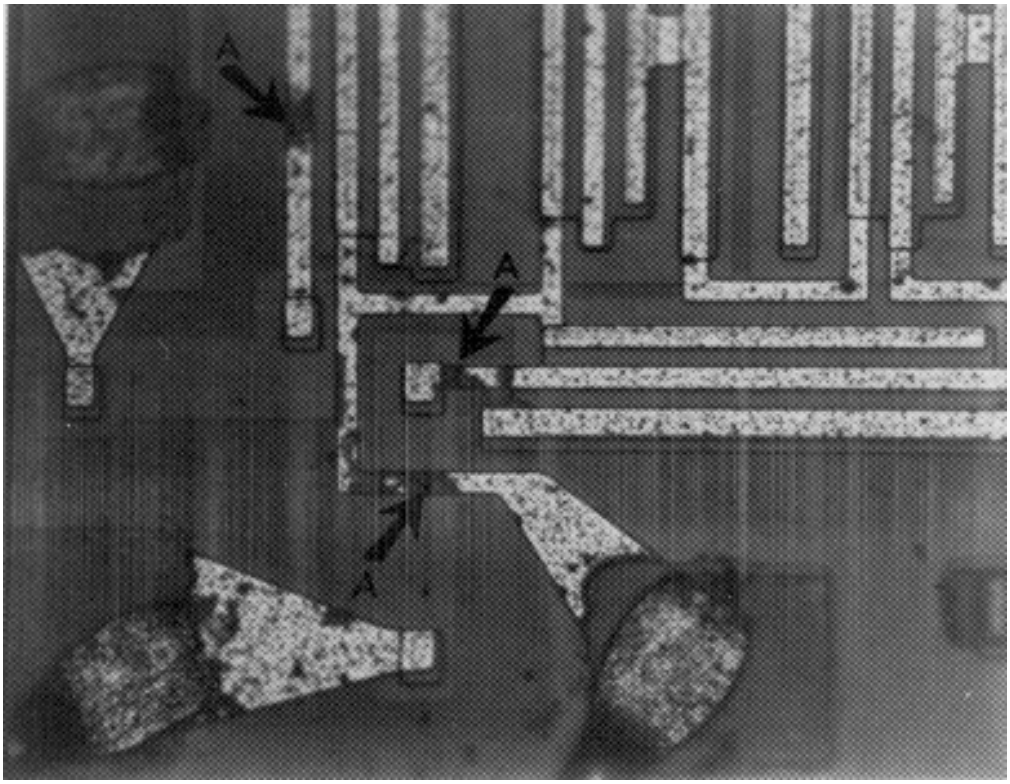

FIGURE 2021-5. Etched device exhibiting failure category A missing glass over aluminum.

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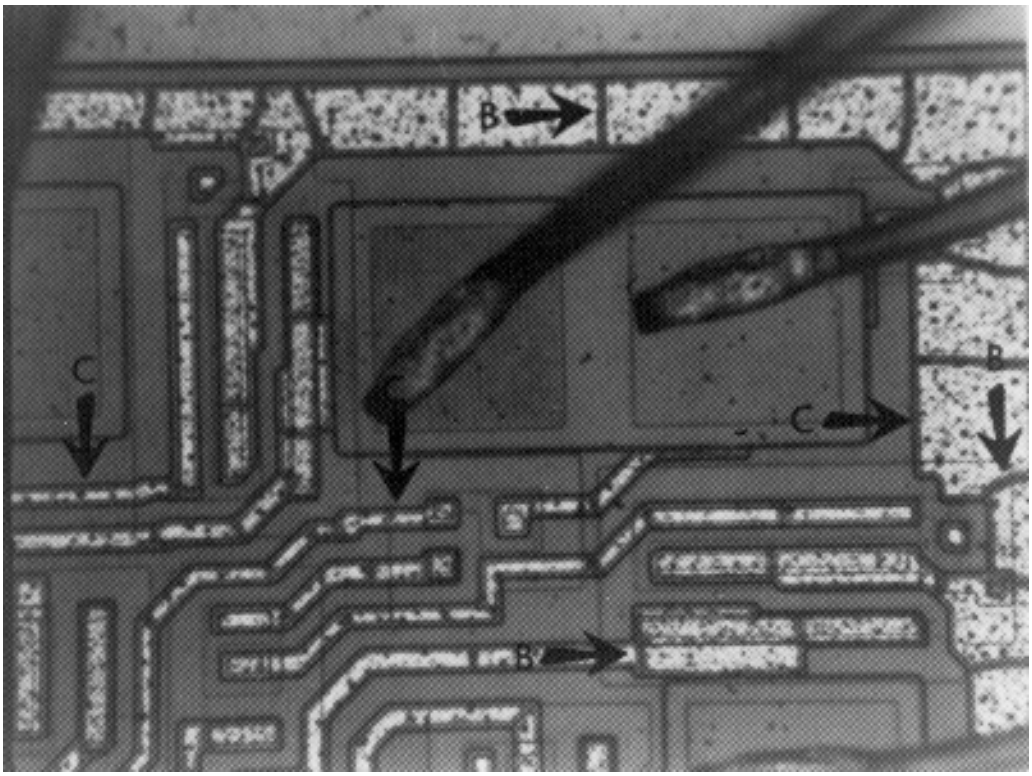

FIGURE 2021-6. Etched device exhibiting failure categories,
B - Cracks in glass over aluminum,
C - Cracks in glass or improper glass,
coverage along edge of aluminum.

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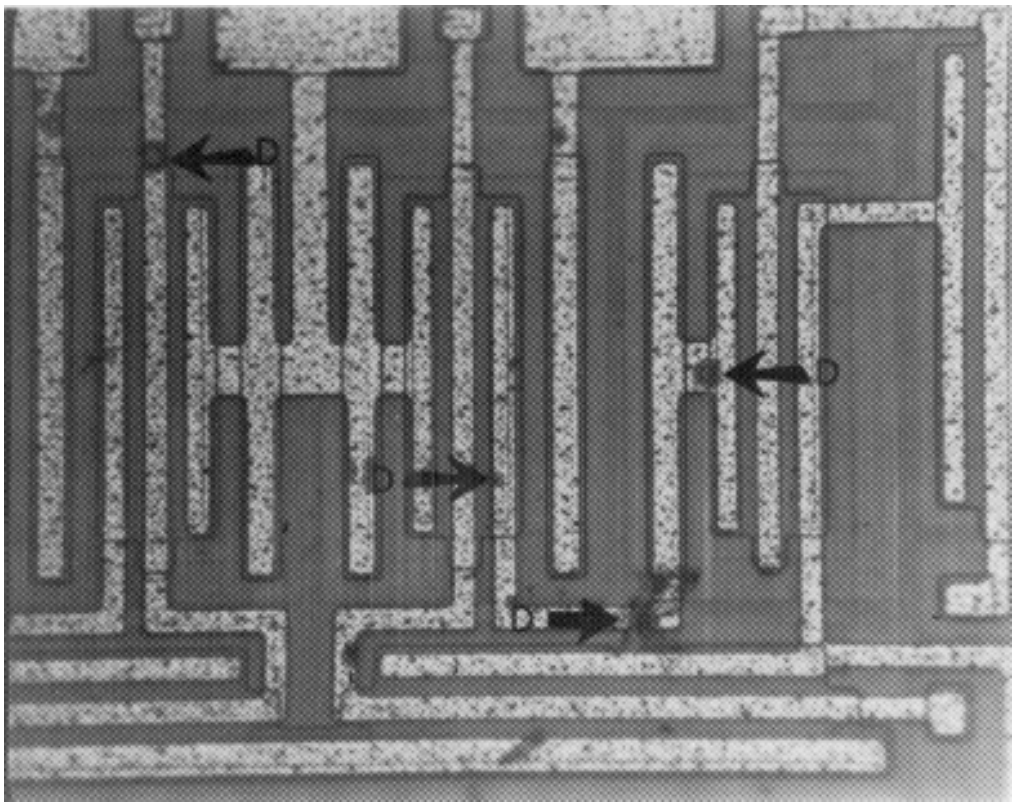

FIGURE 2021-7. Etched device exhibiting category D defects pinholes in glass over aluminum.

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METHOD 2022.3

WETTING BALANCE SOLDERABILITY

1. PURPOSE. The purpose of this test method is to determine the solderability of all ribbon leads up to 0.050 inch (1.27 mm) in width and up to 0.025 inch (0.64 mm) in thickness which are normally joined by a soldering operation and used on microelectronic devices. This determination is made on the basis of the wetting time and wetting force curve produced by the specimen while under test.

These processes will verify that the treatment used in the manufacturing process to facilitate soldering is satisfactory and that it has been applied to the required portion of the part which is designated to accommodate a solder connection.

2. APPARATUS.

2.1 Solder meniscus force measuring device (wetting balance). A solder meniscus force measuring device (wetting balance) which includes a temperature- controlled solder pot containing approximately 750 grams of solder shall be used. This apparatus shall be capable of maintaining the solder at the temperature specified in 3.4. The meniscograph apparatus also includes a strip chart recorder which records the force curve for the device tested.

2.2 Dipping device. A mechanical dipping device is incorporated in the Meniscograph, and is preset to produce an immersion and emersion rate as specified in 3.4. The specimen dwell time is operator controlled to the time specified in 3.4.

2.3 Container and cover. A noncorrodable container of sufficient size to allow the suspension of the specimens 1.5 inches (38.10 mm) above the boiling distilled or deionized water shall be used. (A 2,000 ml beaker is one size that has been used satisfactorily for smaller components.) The cover shall be of one or more noncorrodable plates and shall be capable of covering approximately .875 of the open area of the container so that a more constant temperature may be obtained. A suitable noncorrodable method of suspending the specimens shall be improvised. Perforations or slots in the plates are permitted for this purpose.

2.4 Materials.

2.4.1 Flux. The flux shall conform to flux type symbol “A” (flux type “L0”) of IPC J-STD-004 (previously designated as type “R” of MIL-F-14256).

2.4.2 Solder. The solder shall conform to type Sn63A or Pb37A (previously designated as Sn63 in QQ-S-571) or type Sn60A or Pb40A (previously designated as Sn60 in QQ-S-571).

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3. PROCEDURE. The test procedure shall be performed on the number of terminations specified in the applicable acquisition document. During handling, care shall be exercised to prevent the surface to be tested from being abraded or contaminated by grease, perspirants, etc. The test procedure shall consist of the following operations:

a. Proper preparation of the terminations (see 3.1), if applicable.

b. Aging of all specimens (see 3.2).

c. Application of flux and immersion of the terminations into molten solder (see 3.3 and 3.4).

d. Examination and evaluation of the recordings upon completion of the solder-dip process (see 3.5).

3.1 Preparation of terminations. No wiping, cleaning, scraping, or abrasive cleaning of the terminations shall be performed. Any special preparation of the terminations, such as bending or reorientation prior to the test, shall be specified in the applicable acquisition document.

3.2 Aging. Prior to the application of the flux and subsequent solder dips, all specimens assigned to this test shall be subjected to aging by exposure of the surfaces to be tested to steam in the container specified in 2.3. The specimens shall be suspended so that no portion of the specimen is less than 1.5 inches (38.10 mm) above the boiling distilled or deionized water with the cover specified in 2.3 in place for 4 to 8 hours. In effect while the manufacturer may accept on the basis of 4 hours aging, the customer/user shall be able to reject on the basis of results after 8 hours aging. Means of suspension shall be a nonmetallic holder. If necessary, additional hot distilled water may be gradually added in small quantities so that the water will continue to boil and the temperature will remain essentially constant.

3.3 Application of flux. Flux, type R shall be used (see 2.4.1). Terminations shall be immersed in the flux, which is at room ambient temperature, to the minimum depth necessary to cover the surface to be tested. Unless otherwise specified in the applicable acquisition document, terminations shall be immersed to 0.16 inch (4 mm) from end of lead. The surface to be tested shall be immersed in the flux for a period of from 5 to 10 seconds.

3.4 Solder dip. The dross and burned flux shall be skimmed from the surface of the molten solder specified in 2.4.2. The molten solder shall be maintained at a uniform temperature of 245 ±5°C. The surface of the molten solder shall be skimmed again just prior to immersing the terminations in the solder. The part shall be attached to a dipping device (see 2.2) and the flux-covered terminations immersed once in the molten solder to the same depth specified in 3.3. The immersion and emersion rates shall be 1 ±.25 inches (25.40 ±6.35 mm) per second and the dwell time in the solder bath shall be 5 ±0.5 seconds.

3.5 Evaluation of resultant meniscograph curves from testing of microelectronic leads. The criteria for acceptable solderability during the evaluation of the recordings are:

a. That the recorded signal trace crosses the zero balance point at or before 0.59 seconds of test time.

b. That the recorded signal trace reaches two-thirds of its maximum value in 1 second or less of test time (see figure 2022-1).

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4. SUMMARY. The following details must be specified in the applicable acquisition document:

a. The number of terminations of each part to be tested (see 3).

b. Special preparation of the terminations, if applicable (see 3.1).

c. Depth of immersion if other than 0.16 inch (4 mm) (see 3.3).

d. Solder dip if other than specified in 3.4.

e. Evaluation of meniscograph curves if other than specified in 3.5.

f. Solder composition, flux, and temperature if other than those specified in 2.4 and 3.4.

g. Number of cycles, if other than one. Where more than one cycle is specified to test the resistance of the device to heat as encountered in multiple solderings, the examinations and measurements required shall be made at the end of the first cycle and again at the end of the total number of cycles applied. Failure of the device on any examination and measurement at either the one-cycle or the end-point shall constitute failure to meet this requirement.

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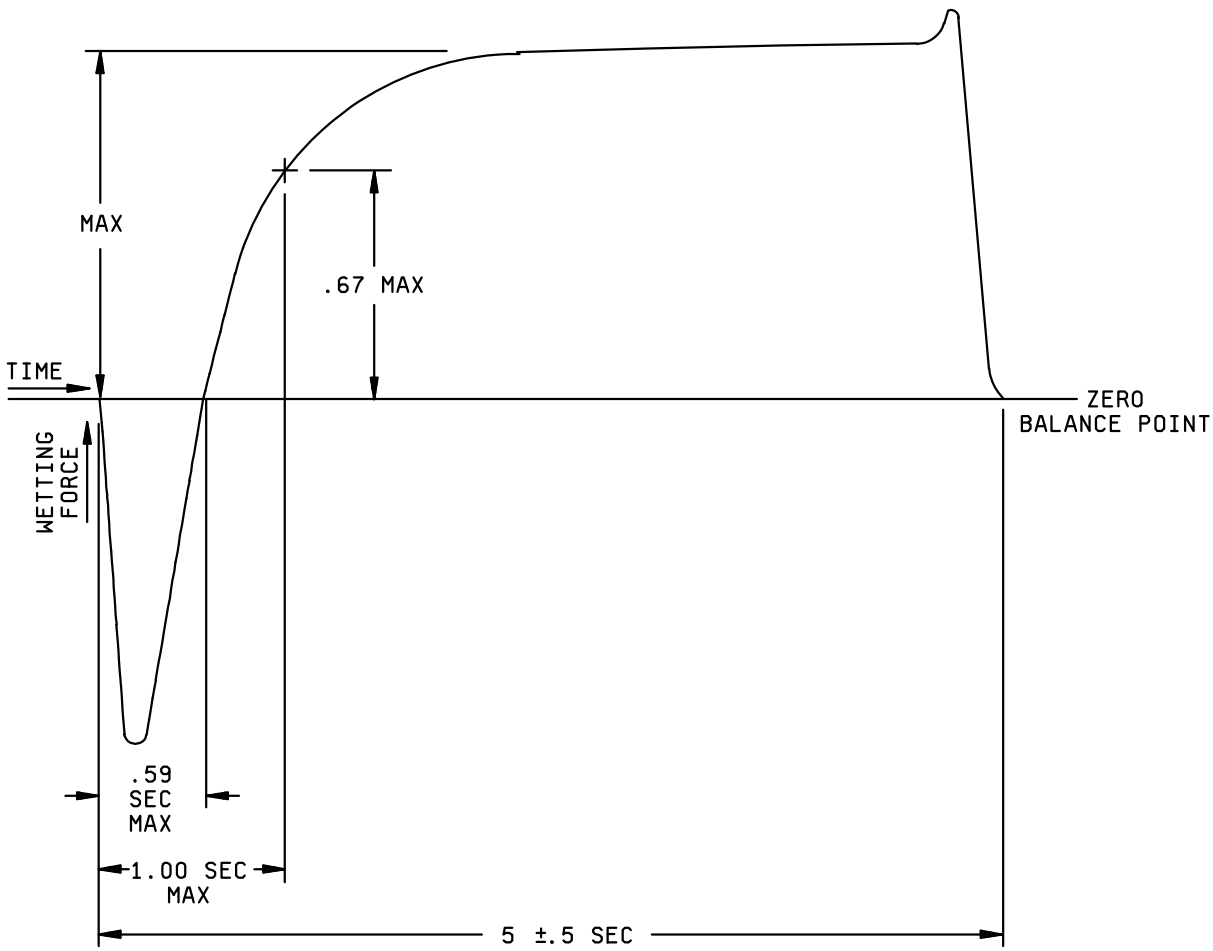

FIGURE 2022-1. Wetting balance curve evaluation criteria.

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METHOD 2023.7

NONDESTRUCTIVE BOND PULL

1. PURPOSE. The purpose of this method is to reveal nonacceptable wire bonds while avoiding damage to acceptable wire bonds. This procedure is applicable for all bonds made by either ultrasonic or thermal compression techniques, except those larger than 0.005 inch diameter (or equivalent cross section area) that do not have sufficient clearance to permit use of a hook.

The alternate procedure defined in 3.2 may be used for devices with packages having 84 or more external terminations and with nominal bonding wire pitch at the package post of less than or equal to 12 mils.

2. APPARATUS. The apparatus of this test shall consist of suitable equipment for applying the specified stress to the bond, lead wire or terminal as required in the specified test condition. A calibrated measurement and indication of the applied stress in grams force (gf) shall be provided by equipment capable of measuring stresses up to twice the specified limit value, with an accuracy of ±5 percent or ±0.3 gf, whichever is greater.

a. The diameter of the wire used to make the hook utilized to apply force to the interconnect wire shall be as follows:

Wire diameter	Hook diameter (x wire dia)
≤ 0.002 inch	2.0 x min
> 0.002 inch - ≤ 0.005 inch	1.5 x min
> 0.005 inch	1.0 x min

For ribbon wire, use the equivalent round wire diameter which gives the same cross sectional area as the ribbon wire being tested. Flat portion of hook (horizontal) shall be ≥1.25 x the diameter of the wire being tested.

b. The hook shall be smooth and free of defects which could compromise the test results or damage the wire being pulled.

c. Travel speed of the hook shall be controlled to that impact loading as the hook initially contacts the wire shall be no more than 20 percent of the specified nondestructive bond pull force.

d. Final hook placement shall be accomplished under observation at 15X minimum magnification. A microscope with a zoom capability may be used for indexing the hook.

e. The fixturing which holds the package shall allow positioning the hook for optimum force application to the wire.

f. An indicator shall either (1) measure the force required to cause failure of the interconnect; or (2) provide visual indication that the predetermined load has been applied.

g. The hook shall be in a fixed position which restricts motion along a straight line between each bond, so that it will not rise to the highest point which could result in a test for only one bond (e.g., as for a ball bond).

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3. PROCEDURE. The test shall be conducted as specified in the applicable acquisition document, as a sample or as a screen, and shall be consistent with the particular bond materials and construction. All bond wires in each device shall be pulled and counted, and the specified sampling, acceptance, and added sample provisions shall be observed, as applicable. Where there is any adhesive, encapsulant or other material under, on, or surrounding the wire such as to increase the apparent bond strength, the test shall be performed prior to the application of the material.

a. Set the rate of force application.

b. Mount the specimen to be tested and set the lifting mechanism to apply the specified force for the appropriate wire size and material.

c. The device shall be rotated and positioned such that the hook contacts the wire between midspan and loop apex without causing adverse wire deformation (for forward wedge and ball bonding, this would be between midspan and die edge; for reverse bonding, this would be between midspan and package edge) and the pulling force is applied in a perpendicular direction to the die or substrate surface. See Figure 2023-1.

d. The lifting mechanism shall be actuated to stress the wire bond such that the specified stress is applied with minimum impact loading and with no overshoot greater than specified accuracy of the indicator at any time during the bond pull. The dwell time of maximum force application shall be a maximum of one second.

e. Observe whether the bond breaks.

f. If the bond breaks, reject the device and proceed to the next device, unless rework is acceptable. If so, record the identification of the broken bond and the device containing the bond. If rework is permitted, all bonds shall be tested prior to any bond rework and reworked bonds shall be tested.

g. If no bonds on the device break, accept the device as satisfactory.

h. Repeat a through g for all bonds to be tested.

i. Record the total number of wires or wire bonds that fail when subjected to the predetermined stress.

j. Record the number of devices that failed the test.

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3.1 Failure criteria. Any bond pull which results in separation (of bonds at the bond interface or breakage of the wire or interconnect anywhere along the entire span including bond heels) at an applied stress less than the specified stress for the applicable material and construction shall constitute a failure. Unless otherwise specified, the applied nondestructive pull stress shall be 80 percent of the preseal minimum bond strengths for the applicable material, size and construction given in table I of method 2011 or figure 2011-2 of method 2011. Table I herein lists pull force values for commonly used wire sizes.

NOTE: RF/microwave hybrids that require extremely flat loops which may cause erroneous wire pull data may use the following formula to determine the proper wire pull value.

$V_1 = V_2 \sin \theta$

Where: V_1 = New value to pull test.
V_2 = Table I value for size wire tested.
θ = Greatest calculated wire loop angle (figure 2023-2).

Also, RF/microwave hybrids that contain tuning wires (designated wires that will alter RF performance when moved) or wires that cannot be accessed with a pull hook must be simulated on a test coupon in such a way to allow hook access for purposes of pull testing. These wires are to be bonded at the same time the production hybrids are bonded using the same setup, operator, schedule, and elements (electrical rejects may be used). The test coupon wires are to be pull tested in lieu of the tuning or inaccessible wires on the production hybrid. Failures on the test coupon shall be considered as failures to production units and appropriate action is to be taken in accordance with the applicable specification (figure 2023-3).

TABLE I. Nondestructive pull forces.

AL and AU wire diameter (inches)	Pull force (gf) AL	Pull force (gf) AU
0.0007	1.2	1.6
0.0010	2.0	2.4
0.00125	2.5	3.2
0.0013	2.5	3.2
0.0015	3.0	4.0
0.0030	9.5	12.0

NOTES:
1. Nondestructive pull force values for wire sizes not specified shall be 80 percent of the preseal pull forces for aluminum or gold wire given in method 2011.
2. Tolerances shall be ±0.3 gf for pull forces up to 6 gf and ±5 percent for pull forces above 6 gf.
3. Any bond subjected to a nondestructive pull force exceeding the specified pull force and the positive tolerance shall be eliminated and not counted toward the PDA failures.

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3.2 Alternative procedure. This alternate procedure may be used where 100 percent non-destructive bond pull cannot be performed because of high pin count (greater than or equal to 84 terminals) and small bonding wire pitch at the package post (less than or equal to 12 mils).

3.2.1 In-process controls. In order for a manufacturer to use the alternate procedure, a SPC program shall be implemented for the wire bond operation in accordance with TechAmerica EIA-557, Statistical Process Control Systems. Any change in the various effects shown to be significant by the characterization with respect to wire bond strength shall require a re-characterization of the wire bonding process for the changed effect(s) on wire bond integrity. For QML, the SPC program and the requirements listed herein shall be approved by the qualifying activity and may be subject to an audit at any time by the government qualification activity. For Non-Jan devices, the SPC program and the requirements listed herein are subject to review by the government agency responsible for the acquisition or their designee. All statistical evaluation, characterizations, and designed experiments shall be available for review.

3.2.1.1 Applicable incoming materials. Applicable incoming materials including wafer pad metallization targets, package bonding post, and bonding wire shall have their critical characteristics determined and made requirements for acceptance using either incoming inspection or vendor SPC data. Critical characteristics shall include possible sources of material contamination (e.g. excessive carbon content in aluminum wire). Also, the applicable incoming inspection requirements of MIL-PRF-38535 or MIL-PRF-38534 shall apply.

3.2.1.2 Applicable manufacturing processes. Applicable manufacturing processes including bond pad metal disposition, glassivation etch, and worst case package seal excursion shall have their critical characteristics determined and placed under SPC control. Also, the process control requirements of the applicable general specification shall apply for these operations including contamination controls, preventative maintenance procedures and schedules, and complete removal of glassivation from the bonding pad.

3.2.1.3 For packages with gold plated posts. For packages with gold plated posts, the device manufacturer shall perform a bake test on one device from each incoming package lot. This test shall evaluate for basic plating or contamination anomalies of the package post. The package shall be wire bonded post-to-post. The wire bonded package shall be baked at 300 degrees Celsius for 1 hour in either air or inert atmosphere. Bond strength shall then be tested in accordance with MIL-STD-883, method 2011, using a sample size number = 45, C = 0 on the number of wires pulled. If any bond strength failure is determined to be package plating or contamination related then the package lot shall not be used for this alternative unless the defect can be effectively screened and the package lot resampled to a tightened sample size number = 76, C = 0 for the number of wires pulled.

3.2.1.4 An active foreign material control program. An active foreign material control program shall be in accordance with MIL-STD-883, method 2010 or method 2017. A procedure and system for storing and handling wafers, packages, related piece parts, and unsealed devices that will prevent contamination through package seal including face masks, lint free gloves, restrictions on particle generating make-up, hair covers, and cleanroom gowns.

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3.2.1.5 A 100 percent pre-bond visual inspection procedure. A 100 percent pre-bond visual inspection procedure of the die pads and package post shall be documented. The visual inspection shall be performed at 100-200X in an ISO 14644-1, Class 5 environment. Cleaning to remove rejectable contamination is allowed. No device shall exhibit evidence of the following criteria:

a. Glassivation on the designed open contact area of the bond pads.

b. Chemical, film, photoresist or liquid contamination on the pads or posts.

c. Particulate and /or foreign material contamination on the pads or the critical bond area of the posts greater than 0.25 mils in diameter.

d. Die pads and package posts that do not meet all applicable requirements of MIL-STD-883, method 2010, condition A or method 2017.

NOTE: 100 percent pre-bond visual inspection may be waived by the qualifying activity provided a 100 percent pre-clean of pads and posts is performed, and all pads and posts for five (5) randomly selected devices pass the inspection criteria. Precleaning may also be waived by the qualifying activity if historical data demonstrates the cleaning is unnecessary. No cleaning is allowed during sample inspection. A 100 percent pre-clean and sample inspection of 5(0) may be repeated a maximum of two times. Rejection of the sample after the second pre-clean shall result in a 100 percent pre-bond inspection of the lot in accordance with 3.2.1.5. An investigation of the rejects in the lot and sample shall be required and corrective action, as necessary shall be instituted. Until then, 100 percent pre-bond inspection is required. Once the effectiveness of any corrective action has been determined, the 100 percent pre-bond inspection may be eliminated.

3.2.1.6 Bonding machine parameters. Bonding machine parameters (e.g., temperatures, pressure, timing, fixtures, wire size, wire material, height settings, etc.) must be defined for each die/package combination. The bonding equipment parameters ranges shall be optimized by designed experiments. The experiments shall consider variations in bonding wire geometry (e.g., loop height, wire length, shelf height, etc.). The experiments shall establish the predicted strength and tolerance of the bonding operation. The allowable performance ranges of the bonding parameters determined by controlled experiments shall be documented. Equipment parameter changes outside the allowable limits must be evaluated and documented as to still meeting the predicted wire pull strength and tolerance.

Note: ASTM Standards F 458 and F 459 may be used as guideline documents.

3.2.1.7 Process capability study. After the wirebond process has been demonstrated to be in a condition of stability and statistical control, a process capability study shall demonstrate that the probability of any device failing the minimum post-seal bond strength is P <.0001. The probability must meet the accumulative probability at the device level and not at the individual wire level. The distributional form of the post-seal bond strengths shall be statistically evaluated for conformance to the selected sampling distribution (e.g., Gaussian, lognormal, Wiebull, etc.). The capability study sample size shall be sufficient to detect a shift in the distribution of the worst case package/die combination to a 100 parts per million level. The beta risk to the consumer shall be .001 or less. (See Appendix A for normal distribution example.) The process capability study shall be performed periodically. The capability study may be accomplished by characterizing the wire pull strengths of one or more worst case package/die combinations. Selection of the worst case package/die combinations should consider wire geometry, number of wires, pads and post sizes, etc. The characterization results from worst case package/die combinations must be readily extended to all devices.

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3.2.1.8 Control limits and action procedures. The results of the evaluations in 3.2.1.6 and 3.2.1.7 shall be used in determining control limits and action procedures for the wire bond operation. A destructive wire bond strength sampling plan for each wire bonder shall include start and completion of each assembly lot, frequency of sampling the assembly lot, and changes in operators (manual wire bonding only), wire spools, package lots, or setup conditions. The bond strength data shall include the force required for failure, the physical location of failure, and the nature of the failure. Electrical rejects from the same wafer lot may be used for the destructive wire bond pulls. In the event that bond wire strengths are outside the predicted values for the wire, or class of wires with similar geometry, the bonder shall be inactivated immediately and not returned to production until tests show that the operation is back under statistical control. A procedure for the traceability, recovery, and disposition of all units bonded since the last successful bond strength test is required.

3.2.1.9 Time and temperature characterization. Initially, a time and temperature characterization shall be performed for each major type of wire bond metallurgical interface (e.g., gold/aluminum, etc.) to determine the electrical and mechanical integrity of the wire bonds with respect to such factors as; flexing of wire bonds due to thermal expansion, and microcracks or microvoids at the metallurgical interface. Evidence from the characterization shall demonstrate that the integrity of the bonds is sufficient for a device to function over its expected life. Life usage conditions shall exceed 50,000 cycles from a 0 - 85 degree Celsius temperature range at the bonds. Time and temperature degradation factors for accelerated testing must be justified against these minimal life usage conditions.

3.2.1.10 Wire bond integrity. If pre-burn-in, interim and post burn-in electrical failures (opens/shorts), qualification, or quality conformance inspection failures indicate questionable wire bond integrity then an analysis is required to verify the bond integrity. If any bond is confirmed to be defective; the applicable inspection lot or sublot will be rejected, an evaluation performed to determine the cause of the bond failure, corrective actions implemented based on the evaluation, and disposition of other affected inspection lots or sublots. The failure analysis and corrective actions will be retained and made available to the qualifying activity upon request.

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3.2.2 Lot acceptance procedure. Each assembly lot shall receive a post-seal bond wire integrity acceptance test. A separate assembly lot acceptance test is required for each wire bonder, and for any changes in setup conditions, wire spool, package lot, or wafer lot, unless such differences have been demonstrated to be statistically insignificant. A post-seal destructive wire bond sampling and test plan with the following minimum requirements shall be documented.

a. More than one device shall be subjected to the acceptance test. Electrical, non-wire bond related visual, or package seal rejects may be used for the post-seal wire bond test.

b. The destructive wire pulls shall be evaluated in meeting the post-seal bond strength limits in MIL-STD-883, Method 2011, or as established in 3.2.1.7. The assembly lot shall be accepted if the wire bond strengths meet the requirements of sections c, d, and e below.

c. All wires or a minimum of 50 randomly selected wires shall be pulled from each sampled device. The post-seal bond strength distribution(s) must demonstrate that the wire bond process is in statistical control, has not changed with respect to the distribution characterized for a one-sided lower control limit, and no single destructive pull is less than the specified post-seal bond strength limit. The sample size shall be sufficient to demonstrate that the statistical distribution of all wires pulled has not changed with respect to central tendency or dispersion in such a way as to violate a $p < .0001$ at the device level. The beta risk to the consumer shall be .01 or less. The method of statistical analysis shall be documented and approved by the qualifying activity.

d. A minimum of 8 wires shall be evaluated from each sampled device to represent the worst case wires as determined to potentially violate the lower specification limit. Their wire pull strengths shall be within the predicted tolerances established in 3.2.1.6. Any wire pull strengths outside the predicted tolerance in the characterized distribution shall require evaluation as to the cause of the out of control condition, and additional worst case wires shall be pulled to determine whether the wire bond strength distribution meets a probability at the wire level of $P < 1-[.9999^{**}(1/n)]$ (n = number of bonding wires in the package). The lot is rejected if this criteria is not met.

e. If any bond fails the acceptance criteria, a documented action plan shall be followed to determine the cause of the failure. Wire bond failures verified as non-bond related shall be documented, and additional post-seal wire bond pulls shall be conducted to demonstrate statistical control as described in 3.2.2.1.c and d. If a failure is verified as bond integrity related (e.g., contamination on wire, glassivation on the bonding pad, etc.), all devices within the applicable assembly lot shall be rejected. Wire bonding shall be suspended on the applicable bonding equipment until a failure analysis, MIL-STD-883, method 5003, of the failed bond is performed and corrective action is implemented and recorded.

4. SUMMARY. The following details shall be specified in the applicable acquisition document:

a. The applied lifting force if other than as specified in 3.1.

b. The sampling, acceptance, or screening requirements.

c. The percent defective allowable (PDA) as applied to the number of failures with respect to the number of wires tested.

d. The requirements for reporting of failure categories, when applicable.

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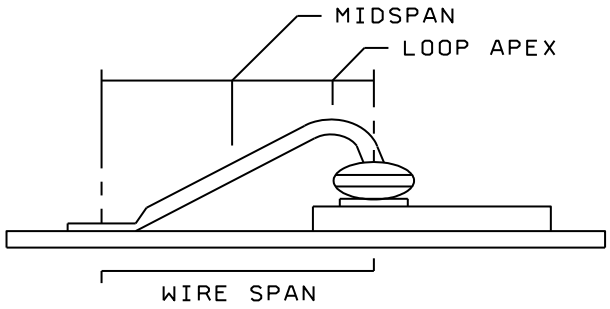

Figure 2023-1. Bond pull hook placement location.

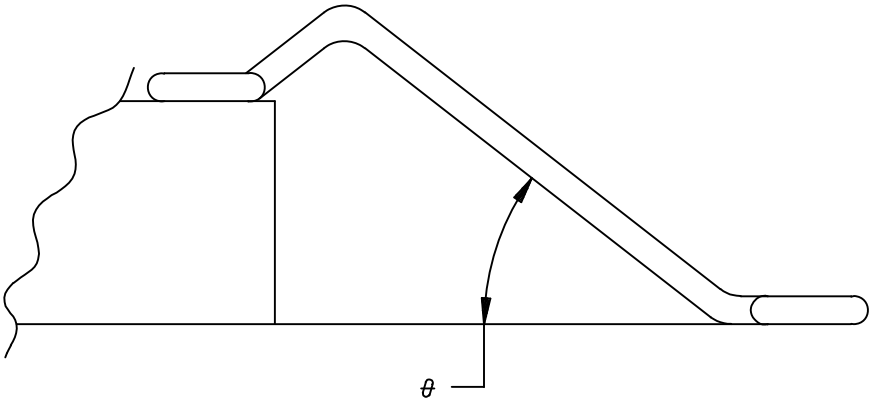

FIGURE 2023-2. Wire loop angle.

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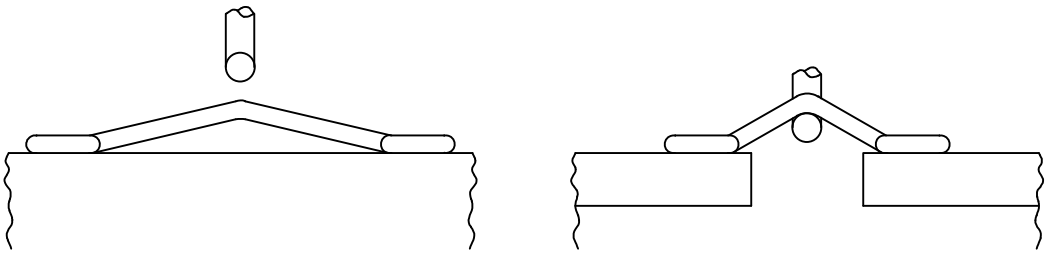

FIGURE 2023-3. Flat loop wire pull testing.

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APPENDIX A

Capability Study Example

The worst case die/package combination for the example product line is a 100 wire package with the smallest die. The worst case die/package combination is based on the characterized worst case wire geometry and number of bonding wires. A post seal bond pull of 2 grams or less is considered unacceptable for 1.25 mil diameter aluminum wire. The proposed military standard requires a failure rate of no greater than 100 parts per million.

The distribution of bond pulls across devices is examined for each wire length. A statistical test is done for normality and in this example there is no reason to reject the assumption of normality. The worst case wire length in terms of variability and closeness to the specification of 2 grams is identified. The mean of this worst case distribution is found to be 4.26 grams with a standard deviation of .5 grams.

Thus, for this distribution the 2 gram specification is 4.52 standard deviations away [(4.26-2)/(.5)] and corresponds to a ppm level of approximately 3.1. If the distribution was to shift to the 100 ppm level such that 2 grams corresponds to 100 ppm (i.e., the 2 gram spec is now only 3.719 standard deviations below the mean), a shift of about .8 sigma [4.52-3.719] from the present bond pull mean of 4.26 would be required. This information is used to determine the number of devices needed for the capability study.

The following table can be used where the data is normally distributed:

Sigma shift to 100 ppm level	Devices needed
0.4	140
0.5	90
0.6	62
0.7	46
0.8	35
0.9	28
1.0	22
1.1	19
1.2	16
1.3	13
1.4	11
1.5 or greater	10

n = [(Z_alpha + Z_beta)**2]/(d**2)

d = standard deviation shift = 0.8

alpha = 0.05 ; Z_alpha = -1.645

beta = 0.001 ; Z_beta = -3.09

[see Diamond, 1989, Practical Experiment Designs, pages 45-47]

Therefore, n = [(1.645 + 3.09)**2]/(.8)**2 = 22.42/.64 = 35. Thirty five devices are used in this capability study.

Using the standard bonding process, the 35 devices (each having 100 wires) are submitted to package seal, and post-seal bond strength measured.

For each wire position a mean and standard deviation is calculated across the 35 devices.

mean = xbar
standard deviation = sd

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The distributions are evaluated and show no significant departure from normality.

The lower spec limit is determined: Here a lower bond pull of 2 grams.

APPENDIX A

For each wire position a "Z" is calculated:

Z = (xbar - LSL) / sd

For each wire position a probability of wire failure is determined by finding the probability of being below the Z value. Use of normal probability tables are utilized in this example because of the distributions being normally distributed. For this example there will be 100 values.

The probability of device failure is calculated by summing the 100 p values for failure of a wire position.

P(Device Failure) = Summation of P(failure of wire position)

= 0.00005 for this example or 50 parts per million

For this example it has been demonstrated that the probability of any device failing the minimum post-seal bond strength is less than 0.0001.

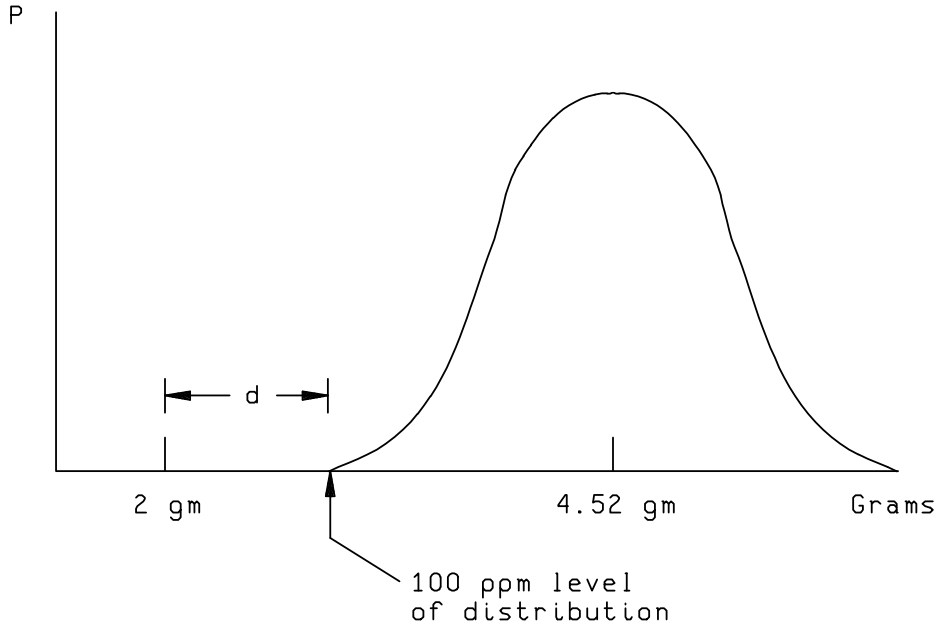

FIGURE 2023-4. Bond strength versus probability.

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METHOD 2024.2

LID TORQUE FOR GLASS-FRIT-SEALED PACKAGES

1. PURPOSE. The purpose of this test is to determine the shear strength of the seal of glass-frit-sealed microelectronic packages. This is a destructive test.

2. APPARATUS. The test equipment shall consist of suitable fixed or adjustable clamps and fixtures to secure devices while applying a torque to the seal area. The torque mechanism and holding fixtures should provide adequate support to the base and lid (especially for flat packs, chip carrier packages, or other thin profile packages) to assure that the torque is applied predominantly to the seal area without significant bending, warping or displacement of the package being tested. A torsion wrench or torque-applying mechanism capable of applying a torque of at least 12.8 newton meter (114 in-lbf) with a gauge capable of measuring the force with an accuracy and precision of ±5 percent of the reading or ±0.2 newton meter, whichever is greater, shall be used to apply torque to the lid. For smaller seal area packages a torsion wrench or torque-applying mechanism with sufficient capacity to separate the package and with an accuracy and precision of ±5 percent of the reading or ±0.2 newton meter whichever is greater, may be used to allow for a more accurate reading. The torque mechanism shall have a peak indicator for retaining the maximum stress applied or other equivalent stress recording system.

3. PROCEDURE. The device shall be held by the device body and torque applied to the lid of the device or vice versa. The lid torque fixtures shall be placed to assure that it only applies torque to the side area of the package lid, base, or spacer. Contact to the sealing glass should be avoided. The lid torque fixture may touch the package leads but not in such a way that significant torque is transferred directly through the leads. The torque shall be applied gradually and smoothly until package separation occurs, or the reaching of the 12.8 newton meter torque limit. The torque required for package separation or the reaching of the 12.8 newton meter torque limit shall be recorded. The torque shall be applied such that the axis of rotation is perpendicular to the sealing plane and the axis of rotation shall be located at the geometric center of the sealing area (see figure 2024-2).

3.1 Separate glass seals. For packages with more than one glass-frit-seal (e.g., separate glass-frit-seals for the lid and the lead frame), each seal shall be torqued and rated separately against the failure criteria. A failure of either seal shall constitute failure of the test. Alternatively, the two seals may be simultaneously stressed by holding only the lid and base and applying the torque specified for the larger seal area.

3.2 Failure criteria. Failure criteria are based on not achieving the designated torque without breakage or lid separation. The designated torque is a function of the device seal area, as illustrated in Figure 2024-1. A device where package separation or breakage occurs at a torque value less than specified in table I shall constitute a failure. If the entire package (lid, seal, and base) breaks in a direction normal to the plane of the applied torque (i.e., showing evidence of improperly applied torque) with parts of lid and base still fused together, the package may be discarded without counting as a failure and a replacement sample substituted to complete the required testing.

4. SUMMARY. The following details shall be specified in the applicable acquisition document:

a. The minimum torque if other than the value specified in table I.

b. Number of devices to be tested.

c. Requirement for data recording where applicable.

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TABLE I. Minimum torque limits versus design seal area.

Design seal area (cm2)	Torque		
	Newton meter (N-m)	Inch-pounds force (in-lbf)	Meter-grams force (m-gf)
<0.22	0.5	4	50
0.221-0.32	0.7	6	70
0.321-0.47	1.0	9	100
0.471-0.65	1.7	15	170
0.651-0.85	2.5	22	250
0.851-1.08	3.4	30	350
1.081-1.41	4.4	39	450
1.411-1.73	5.9	52	600
1.731-2.05	7.4	65	750
2.051-2.50	8.8	78	900
2.501-3.00	10.8	96	1100
>3.00	12.8	114	1300

Various units are presented for the convenience of those using conventional torque wrenches scaled in metric or English system units. All values have been rounded off from the direct conversion values beginning with N-m and are acceptable for use in quality conformance and qualification inspection.

1 m-gf = 0.009807 N-m
1 in-lbf = 0.1130 N-m

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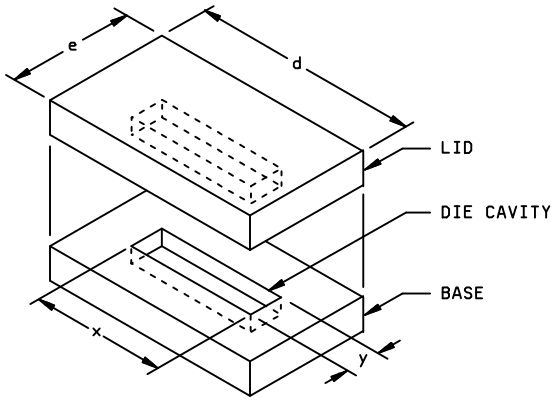
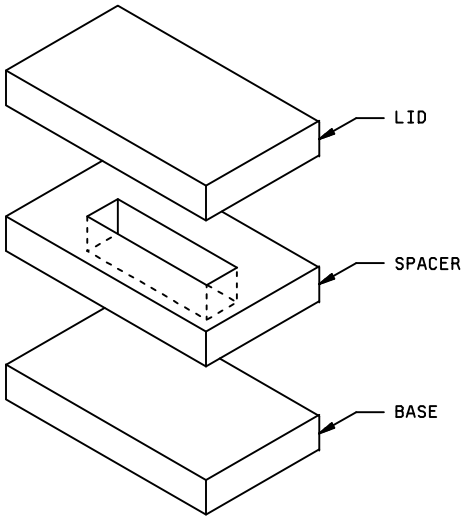


a. TWO PIECE PACKAGE

Seal area = ed - xy

If the cavities in the lid and base are not equal, the area "XY" shall be determined from the larger of the cavities in the lid or base.



b. THREE PIECE PACKAGE

FIGURE 2024-1. Design seal area.

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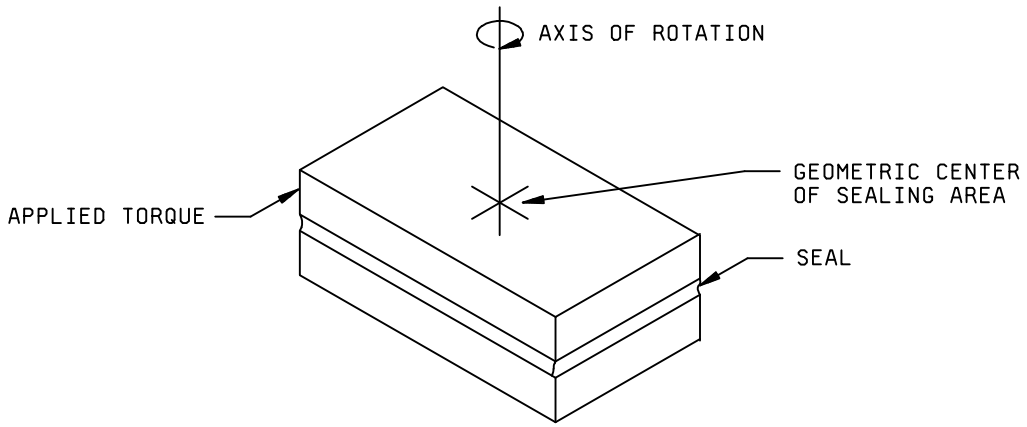

FIGURE 2024-2. Application of torque.

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METHOD 2025.4

ADHESION OF LEAD FINISH

1. PURPOSE. This destructive test is intended to determine the integrity of all primary and undercoat lead finishes.

2. APPARATUS. This test requires suitable clamps and hardware necessary to apply the bending stress through the specified bend angle. Optical equipment capable of magnification of 10X to 20X.

3. PROCEDURE. Unless otherwise specified, the bend stress shall be applied to randomly selected leads from each device selected for test and shall be performed after application of the primary finish and after sealing. Unless otherwise specified, the sampling shall be sample size number = 15, C = 0 based on the number of leads tested chosen from a minimum of three devices. The leads shall be bent in the least rigid direction. If there is no least rigid direction, they may be bent in any direction. The coated lead shall be bent repeatedly in the same direction (or plane) through an angle of at least 90° at a radius of less than four times the lead thickness or diameter at approximately the mid point of the lead lengths until fracture (i.e., lead breaks off) of the base metal occurs.

3.1 Failure criteria. No cracking, flaking, peeling, blistering, loosening, or detachment of the coating(s) at the interface(s) shall result from probing the bend/break area with a sharp instrument. Cracks in the base metal shall not be considered a failure unless accompanied by cracking, flaking, peeling, blistering, loosening, or detachment of the primary coating(s) or undercoating(s).

NOTE: In tin lead or heavy tin coatings, the failure criteria listed should not be confused with shearing and tearing associated with fatigue fractures and slip-planes which develop into cracks and result in rupture.

4. SUMMARY. The following details shall be specified in the applicable acquisition document:

a. Sampling criteria, if other than specified (see 3).

b. Failure criteria, if other than specified (see 3.1).

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METHOD 2026

RANDOM VIBRATION

1. PURPOSE. This test is conducted for the purpose of determining the ability of the microcircuit; to withstand the dynamic stress exerted by random vibration applied between upper and lower frequency limits to simulate the vibration experienced in various service-field environments. Random vibration is more characteristic of modern-field environments produced by missiles, high-thrust jets, and rocket engines. In these types of environments, the random vibration provides a more realistic test. For design purposes, however, a swept frequency sinusoidal test may yield more pertinent design information.

2. APPARATUS.

2.1 Vibration system. The vibration system, consisting of the vibration machine, together with its auxiliary equipment shall be capable of generating a random vibration for which the magnitude has a gaussian (normal) amplitude distribution, except that the acceleration magnitudes of the peak values may be limited to a minimum of three times the rms (three-sigma (α) limits). The machine shall be capable of being equalized so that the magnitude of its spectral-density curve will be between specified limits (for example, see figures 2026-1 and -2). When the test item, or a substitute equivalent mass, is appropriately secured to the vibration machine. The equalization of an electrodynamic vibration machine system is the adjustment of the gain of the electrical amplifier and control system so that the ratio of the output-vibration amplitude to the input-signal amplitude is of a constant value (or given values) throughout the required frequency spectrum.

2.1.1 Control and analysis of vibration.

a. Spectral-density curves. The output of the vibration machine shall be presented graphically as power-spectral density versus frequency. 1/ The spectral-density values shall be within +40 and -30 percent (±1.5 dB) of the specified values between a lower-specified frequency and 1,000 Hz, and within +100 and -50 percent (±3 dB) of the specified values between 1,000 and an upper-specified frequency (2,000 Hz). A filter bandwidth will be a maximum of one-third-octave or a frequency of 25 Hz, whichever is greater.

1/ Power-spectral density is the mean-square value of an oscillation passed by a narrow-band filter per unit-filter bandwidth. For this application it is expressed as G^2/f where G^2/f is the mean-square value of acceleration expressed in gravitational units per number of cycles of filter bandwidth. The spectral-density curves are usually plotted either on a logarithmic scale, or in units of decibels (dB). The number of decibels is defined by the equation:

$$dB = 10 \log \frac{G^2 / f}{G_r^{\,2} / f} = 20 \log \frac{G / \sqrt{f}}{G_r / \sqrt{f}}$$

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The rms value of acceleration within a frequency band between f_1 and f_2 is:

$$G_{rms} = \left[\int_{f_1}^{f_2} G^2 / f \, df \right]^{1/2}$$

where $G_r{}^2/f$ is a given reference value of power-spectral density, usually the maximum specified value.

b. Distribution curves. A probability density-distribution curve may be obtained and compared with a gaussian-distribution curve. The experimentally-obtained curve should not differ from the gaussian curve by more than ±10 percent of the maximum value.

2.2 Monitoring. Monitoring involves measurements of the vibration excitation and of the test-item performance. When specified, the device shall be monitored during the test. The details of the monitoring circuit, including the method and points of connection to the specimen, shall be specified.

2.2.1 Vibration input. The vibration magnitude shall be monitored on a vibration machine, on mounting fixtures, at locations that are as-near as practical to the device mounting points. When the vibration input is measured at more than one point, the minimum input vibration shall be made to correspond to the specified test curve (see figures 2026-1 and 2026-2). For massive test-items and fixtures, and for large-force exciters or multiple-vibration exciters, the input-control value may be an average of the average magnitudes of three or more inputs. Accelerations in the transverse direction, measured at the test-item attachment points, shall be limited to 100 percent of the applied vibration.

3. PROCEDURE. The device(s) shall be rigidly fastened on the vibration platform and the leads adequately secured. The vibration machine shall then be operated and equalized or compensated to deliver the required random frequencies and intensities conforming to the curves specified in test condition I, figure 2026-1 or test condition II, figure 2026-2. The device(s) shall be subjected to a random vibration specified by the test condition letter (see tables I and II) for a duration of 15 minutes in each of the orientations X, Y, and Z. Where this test is performed as part of a group or subgroup of tests, the post-test measurements or inspections need not be performed specifically at the conclusion of this test.

3.1 Examination. After completion of the test, an external visual examination of the marking shall be performed without magnification or with a viewer having a magnification no greater than 3X and a visual examination of the case, leads, or seals shall be performed at a magnification between 10X and 20X. This examination and any additional specified measurements and examination shall be made after completion of the final cycle or upon completion of a group, sequence, or subgroup of tests which include this test.

3.2 Failure criteria. After subjection to the test, failure of any specified measurement or examination (see 3 and 4), evidence of defects or damage to the case, leads, or seals, or illegible markings shall be considered a failure. Damage to marking caused by fixturing or handling during tests shall not be cause for device rejection.

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4. SUMMARY. The following details shall be specified in the applicable acquisition document:

a. Test condition (see 3).

b. Measurements after test (see 3 and 3.1).

c. Test condition I or II and letter (A-K).

d. Test duration if other than specified.

e. Requirement for test to be conducted with device powered up, when applicable.

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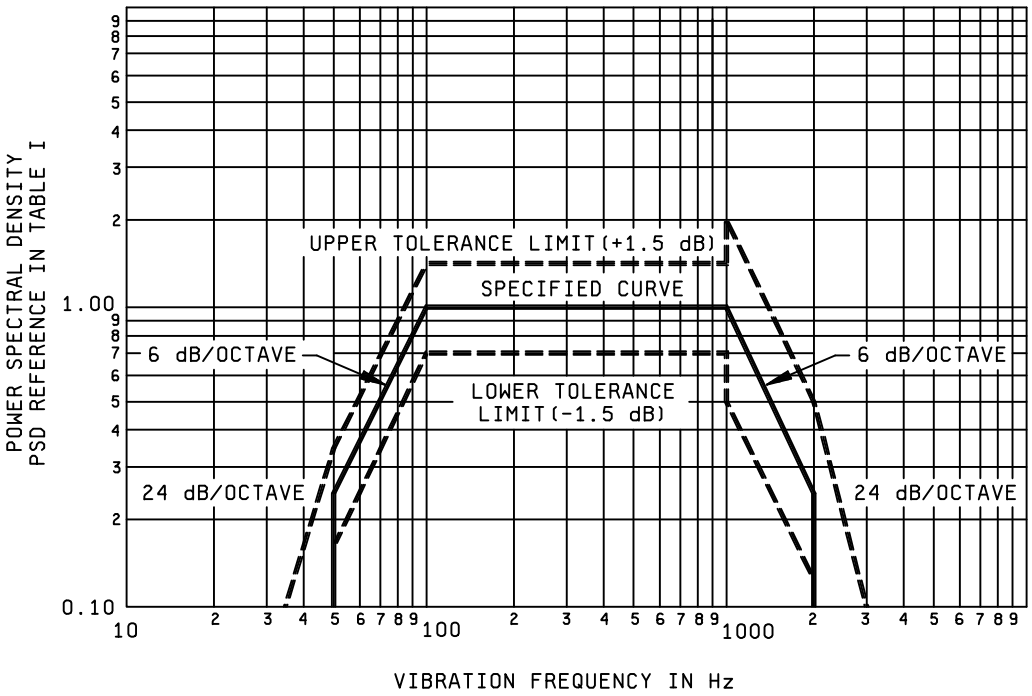

FIGURE 2026-1. Test condition I, random vibration test-curve envelope (see table I).

TABLE I. Values for test condition I. 1/

Characteristics		
Test condition letter	Power spectral density	Overall rms G
A	.02	5.2
B	.04	7.3
C	.06	9.0
D	.1	11.6
E	.2	16.4
F	.3	20.0
G	.4	23.1
H	.6	28.4
J	1.0	36.6
K	1.5	44.8

1/ For duration of test, see 4.

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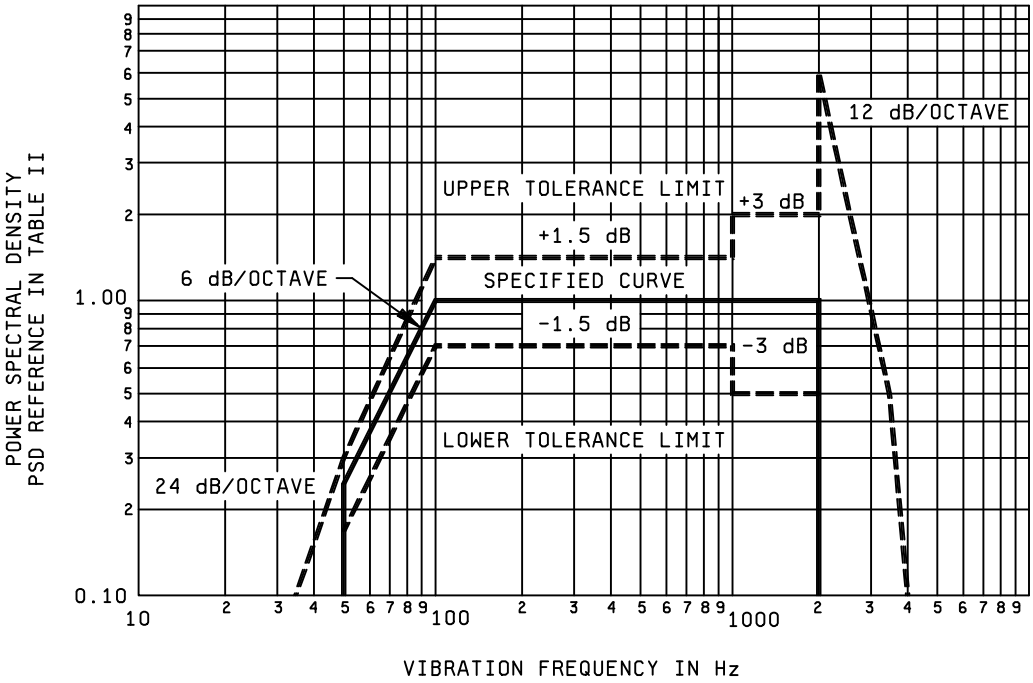

FIGURE 2026-2. Test condition II, random vibration test-curve envelope (see table II).

TABLE II. Values for test condition II. 1/

Characteristics		
Test condition letter	Power spectral density	Overall rms G
A	.02	5.9
B	.04	8.3
C	.06	10.2
D	.1	13.2
E	.2	18.7
F	.3	22.8
G	.4	26.4
H	.6	32.3
J	1.0	41.7
K	1.5	51.1

1/ For duration of test, see 4.

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METHOD 2027.2

SUBSTRATE ATTACH STRENGTH

1. PURPOSE. The purpose of this test is to determine the strength of the element attachment system when subjected to force in the Y1 axis. This method is applicable to semiconductor die attached to headers or substrates by means of organic materials. Uses include material evaluations and process control.

2. APPARATUS. The test equipment shall consist of a tensile strength tester capable of applying a force equal to 1,000 psi (6895 kpa) times the area of the largest die to be tested with an accuracy of ±5 percent or 1.75 ounces (50 gm) force, whichever is less. The test equipment shall have the following capabilities.

a. A range of replaceable die contact tools such that each contacting surface shall be 60 to 100 percent of the area of the die under test.

b. Provision to assure that the die contact tool is held perpendicular to the die mounting plane of the header or substrate.

c. A rotational capability between the die contact tool and the header/ substrate holding fixture.

3. PROCEDURE. The test shall be conducted by placing a small amount of a quick setting adhesive on the contacting tool which is then attached to the die surface (figure 2027-1). After sufficient adhesive curing the sample is subjected to a vertical pull force as defined herein.

3.1 Force applied. A force sufficient to lift the die from its mounting or equal to twice the minimum specified tensile strength (figure 2027-2) whichever occurs first, shall be applied to the die using the apparatus of 2 above.

3.2 Failure criteria. If the separation occurs between the die surface and the die contacting tool at less than twice the minimum specified tensile strength, the particular die pull test will not be counted in the sample as either passing or failing. When this occurs, the DUT may either be retested or replaced with a substitute device to be tested in its place. The following criteria constitute a failure when the die is lifted from the header/substrate:

a. Separation at less than the minimum die tensile strength (1.0X) as shown on figure 2027-2).

b. Separation at less than 200 percent of the minimum die attach strength (2.0X) as shown on figure 2027-2 and no evidence of attachment at the interface between the die attach medium and the die or header/substrate.

3.2.1 Recording. When specified, the force required to achieve separation will be recorded with the failure category.

4. SUMMARY. The following details shall be specified in the applicable acquisition document:

a. Minimum die pull strength if other than that shown on figure 2027-2.

b. Number of die to be tested and the acceptance number.

c. Requirements for data recording.

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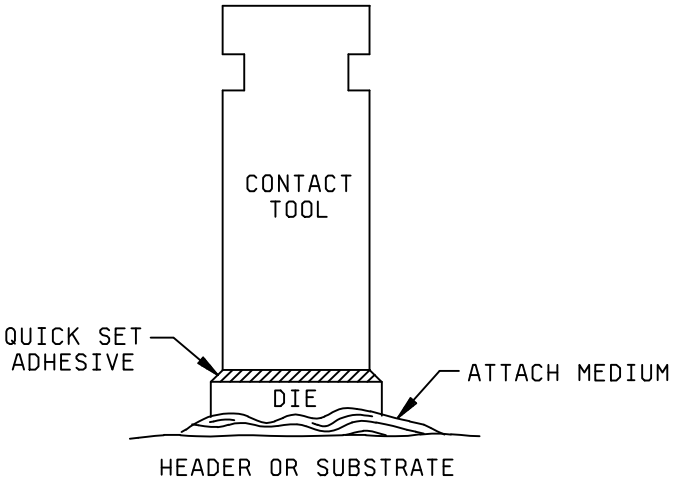

FIGURE 2027-1. Die contact tool adhered to die top surface prior to lift off.

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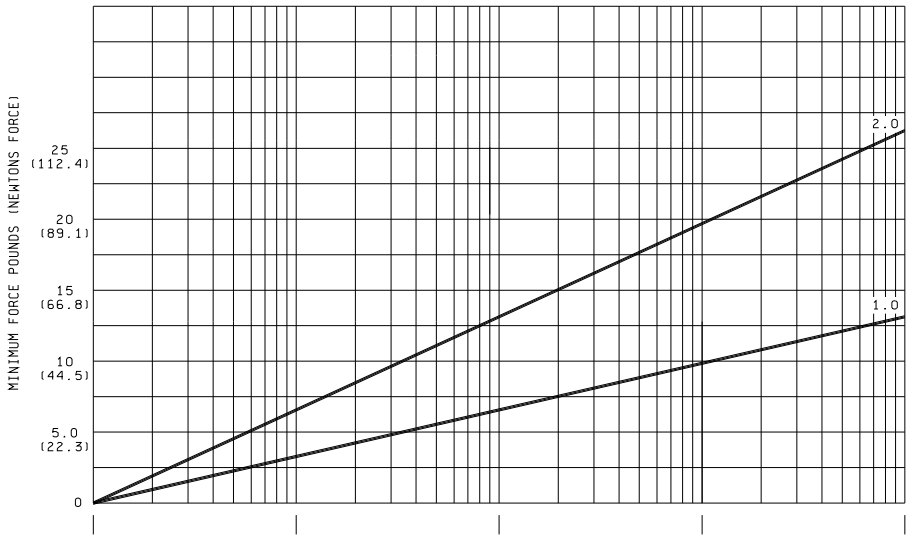

1×10^{-4} sq in	1×10^{-3} sq in	1×10^{-2} sq in	1×10^{-1} sq in	1 sq in
100 sq mils	1,000 sq mils	10,000 sq mils	100,000 sq mils	1,000,000 sq mils
6.5×10^{-4} sq cm	6.5×10^{-3} sq cm	6.5×10^{-2} sq cm	6.5×10^{-1} sq cm	6.5 sq cm

NOTE: The X-axis is a log scale and intermediate points not shown must be calculated based on the formulas,

(1.0 X: y = 3.32 log x + 13.3, 2.0 X: y = 6.63 log x + 26.6) not extrapolated from the graph.

Sample 1: English calculation:

Assume a die measurement of 0.25 inches by 0.25 inches.

x = 0.25 in times 0.25 in = 0.0625 sq in.

Then y = 3.32 log x + 13.3

= 3.32 log (0.0625) + 13.3

= 3.32 (-1.204) + 13.3

= - 4.0 + 13.3

= 9.3

Hence: X = 9.3 lbs and 2X = 18.6 lbs

Sample 2: Metric calculation:

Assume a die measurement of 0.8 cm by 0.8 cm.

x = 0.8 cm times 0.8 cm = 0.64 sq cm

Then y(in pounds) = 3.32 log x(in sqin) +13.3

Because 1 pound = 4.45 newtons, and 1 sq in = 6.45 sq cm, then $y_{newtons}$ = 4.45 times y_{pounds} and $x_{sqin} = x_{sqcm}/6.45$

Thus: $y_{newtons} = 4.45\ [3.32 \log (x_{sqcm}/6.45) + 13.3] = 14.8 \log x_{sqcm} + 47.2$

Or $y_{newtons}$ = 14.8 log (0.64 sq cm) + 47.2

= 14.8 (-0.194) + 47.2

= -2.9 + 47.2

= 44.3 Newtons

Hence X = 44.3 newtons and 2X = 88.6 newtons

FIGURE 2027-2. Die attach strength criteria (minimum force versus die attach area).

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METHOD 2028.4

PIN-GRID PACKAGE DESTRUCTIVE LEAD PULL TEST

1. PURPOSE. This method provides a test for determining the integrity of pin-grid type package leads by measuring the capability of the package leads to withstand an axial force.

2. APPARATUS. The apparatus for this test shall consist of suitable equipment for supplying the specified stress to the package lead. A calibrated measurement and indication of the applied stress in grams-force (gf) shall be provided by equipment capable of measuring stresses up to twice the specified minimum limit value, with an accuracy of ±5 percent or ±0.25 kgf, whichever is greater.

3. PROCEDURE. The stress shall be applied to the leads to be tested randomly selected from a minimum of 3 devices prior to start of the test. Tension only shall be applied, without shock, to each lead to be tested in a direction parallel to the axis of the lead. The tension shall be increased until the minimum acceptable pull strength is reached or upon separation of the lead from the braze pad. The tension shall be applied as close to the end of the lead as possible.

3.1 Failure criteria. The minimum acceptable lead pull strength shall be 1.70×10^7 grams-force per square inch of cross-sectional lead area (e.g., the minimum pull strength of a lead with an average cross-sectional area of 2.5×10^{-4} in^2 will be 4.3 kgf.)

4. SUMMARY. The following details shall be specified in the applicable acquisition document:

a. Number and selection of leads, if different from above.

b. Measured lead pull strength and minimum required pull strength, if different from above.

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METHOD 2029.1

CERAMIC CHIP CARRIER BOND STRENGTH (DESTRUCTIVE PUSH TEST)

1. PURPOSE. The purpose of this test method is to measure strengths of bonds external to leadless microelectronic packages (e.g., solder bonds from chip carrier terminals to substrate or wiring board).

2. APPARATUS. The apparatus for this test method shall consist of suitable equipment for applying the specified stress to the device terminals. A calibrated measurement and indication of the applied stress in grams force (gf) shall be provided by equipment capable of measuring stresses up to twice the specified limit value, with an accuracy of ±5 percent or ±0.25 gf, whichever is the greater tolerance.

3. PROCEDURE. The test shall be conducted using the following test procedure. All push tests shall be counted and the specified sampling, acceptance, and added sample provisions shall be observed, as applicable. A minimum of 4 chip carriers (or use all chip carriers if 4 are not available) on each of a minimum of 2 completed substrates or wiring boards shall be used. Where there is any adhesive, encapsulant, or other material under, on, or surrounding the chip carrier such as to increase the apparent bond strength, the bond strength test shall be performed prior to application.

3.1 Test samples. When packages are bonded to substrates or wiring boards other than those in completed devices, the following conditions shall apply:

a. The sample of packages for this test shall be taken at random from the same chip carrier population as that used in the completed devices that they are intended to represent.

b. The packages for this test shall be bonded on the same bonding apparatus as the completed devices, during the time period within which the completed devices are bonded.

c. The test package substrates shall be processed and handled identically with the completed device substrates, during the same time period within which the completed device substrates are processed.

3.1.1 Sample preparation. Substrates must be prepared as follows:

a. A roughly circular area comprising 50 percent, +5 percent, -0 percent of the bonded side of each package to be tested shall be exposed by either end-mill drilling of the test substrate or other suitable means. If it is not possible to expose the ceramic in this manner, the packages shall be bonded onto test substrates into which the proper hole(s) and hole size(s) has (have) been manufactured, providing all other conditions of 3.1 have been met.

b. Suitable support must be provided for the test substrate so that there is a minimum of flexure of the substrate during the test. This support, if necessary, may be provided by bonding the substrate to a rigid metal plate having a hole pattern matching that of the test substrate.

c. A cylindrical rigid metal test post must be prepared for each hole size, which will be inserted through the support plate and test substrate holes. The post will be used to transmit the specified stress from the stress-source equipment to the exposed package surface. The diameter of the post shall be 85 percent (+5 percent, -0 percent) of the corresponding test hole diameter. The length of the post shall be sufficient to extend 1 inch (+100 percent, -0 percent) from the open end of the test hole when the post is inserted completely into the hole.

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3.2 Testing. The test shall be performed in the following manner:

a. A single package shall be pushed during each test sequence.

b. A layer of teflon tape in accordance with A-A-58092 or equivalent shall be placed between the exposed chip carrier surface and the test post prior to testing.

c. Insert test post into test hole. The contact of the test post to the ceramic chip carrier shall be made without appreciable impact (≤0.1 inch/minute). With the stressing element of the test equipment traveling at a constant rate of 0.02 ±1 percent inch/second, apply sufficient force to chip carrier (through test post) to break all chip carrier to substrate bonds on at least three edges of chip carrier under test. When failure occurs, the force at the time of failure and the failure category shall be recorded. Any test resulting in the fracturing of either the chip carrier or test substrate shall be considered unacceptable. The data from the test shall be discarded, and the test performed again.

3.3 Failure criteria. Any push test which results in separation with a bond strength of less than 30 kg-force per linear inch (1180 g-force per linear mm) of solder pad width shall constitute a failure. The bond strength shall be determined by dividing the separating force by the total of the solder pad widths as measured on the substrate at the package edge, in a direction parallel to the package edge.

3.3.1 Failure category. Failure categories are as follows. When specified, the stress required to achieve separation and the predominant category of separation shall be recorded.

a. Device fracture.

b. Failure in package-bond interface.

c. Terminal break at point not affected by bonding process.

d. Failure in bond-substrate conductor interface.

e. Conductor lifted from board or substrate.

f. Fracture within board or substrate.

4. SUMMARY. The following details shall be specified in the applicable acquisition document.

a. Minimum bond strength if other than specified in 3.3 or details of required strength distributions if applicable.

b. Sample size number and accept number and selection and number of devices to be tested on each substrate, if other than 4.

c. Requirement for reporting of separation forces and failure categories, when applicable (see 3.3.1).

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METHOD 2030.2

ULTRASONIC INSPECTION OF DIE ATTACH

1. PURPOSE. The purpose of this examination is to nondestructively detect unbonded regions, delaminations and/or voids in the die attach material and at interfaces within devices through the measurement of acoustic continuity. It establishes methods and criteria for ultrasonic inspection of devices.

For certain device structures or die attach materials, a dramatic distinction between well-bonded and poorly bonded conditions may be difficult to achieve. This factor should be considered in relation to the design of each device when application of this test method is specified.

2. DEFINITIONS.

2.1 The term "die attach interface" as used in this test method refers to the entire bulk area between the die and the substrate to which it is bonded. For die attach interfaces, this includes the interface between the die attach material and the die, the interface between the die attach material and the substrate, plus the die attach material itself.

2.2 The term “bulk material” as used in this test method refers to the entire thickness within a specific layer of material. For die attach, the attachment material by itself is considered a bulk material.

2.3 The term “ultrasonic inspection” as used in this test method refers to high frequency ultrasonic visualization (imaging) which produces a gray or color scale output such as may be provided by ultrasonic scanning (US) or acoustic microscope (AM) techniques. The most common mode utilized for die attach inspection is an X-Y plane scan at specified depth(s) in Z, which is commonly referred to as C-Scan or C-mode imaging. Other ultrasonic techniques may also be utilized to obtain the die attach integrity data.

2.4 The term “reflected” as used in this test method refers to the change in direction of an ultrasound wave front at an interface between two different media so that the wave front returns via the medium from which it originated.

2.5 The term “reflection mode” as used in this test method refers to an ultrasonic scan or acoustic microscope that uses one transducer as both the pulser and receiver. (This is also known as a pulse/echo system.)

2.6 The term “transmitted” as used in this test method refers to the propagation of an ultrasound wave through a media or an interface between media that allows it to continue through the structure.

2.7 The term “transmission mode” as used in this test method refers to an ultrasonic scan or an acoustic microscope that transmits ultrasound completely through the sample from a sending transducer to a receiver on the opposite side.

3. APPARATUS. The apparatus and materials for this test shall include:

3.1 Ultrasonic inspection equipment: The ultrasonic inspection equipment shall have a test frequency sufficient to penetrate to the die attach material interface. In the case that the opening of a sealed hermetic or non-hermetic device with a known air cavity is undesirable, the ultrasonic equipment shall be capable of detecting an acoustic signal that enters the top and bottom or back of a package and is reflected by or transmitted through to the desired material interface. The test frequencies and focal distances shall be adequate to achieve a resolution capable of detecting voids as small as 0.0254 mm (0.001 inch) in diameter, when inspecting through the die is desired, but this may not be feasible due to the construction of the device. In such cases, the test frequency and focal distance shall be chosen to ensure penetration down to the desired material interface with the achievable resolution being a secondary consideration.

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3.2 Output device: A hard copy gray or color scale recording unit or other direct recording device (computer storage) shall be used to produce an image for analysis (manual or automated). The dynamic range of the output image shall be at least 256 discernible colors or levels of gray scale. The appropriate gray/color scale shall be included in each image. The image, hard copy or digital, shall be large enough to achieve a resolution capable of detecting a void as small as 0.0254 mm (0.001 inches) in diameter, when inspecting through the die, or the best feasible resolution for that application.

3.3 Holding tank: A holding tank for containing the coupling fluid and locating fixtures (as needed) to ensure accurate and repeatable placement of the devices inspected. The holding tank, locating fixtures and any auxiliary supporting hardware shall be constructed of materials that will be unaffected by corrosion or other reactivity in the presence off the coupling fluid.

3.4 Ultrasonic detector: Reflection mode imaging shall be used when the opening of a sealed, hermetic device is undesirable. For inspection of the die attach interfaces within a sealed device, as an example, it shall be capable of detecting an acoustic signal which enters the back or bottom of the package and is reflected by the material interface(s). The reflection and/or transmission modes of imaging shall be used when inspecting a non-hermetic or the opening of a sealed hermetic device is allowable.

4. PROCEDURE. The ultrasonic inspection instrument shall be selected or adjusted as necessary to obtain satisfactory images and achieve maximum image details within the sensitivity requirements for the device or defect features the test is directed toward. In the case of reflection mode or transmission mode images, care must be exercised to insure that the ultrasound penetrates and is sensitive to the entire die attach interface or bulk material area of interest

4.1 Mounting and handling. The devices shall be mounted in the holding tank so that the devices are not damaged or contaminated and are in the proper plane for inspection. The devices may be mounted in any type of fixture providing the fixtures do not block the view from the ultrasonic transducer to any portion of the body of the device in the region of interest. The coupling fluid in the holding tank shall be distilled water or other suitable noncorrosive liquid. The devices shall remain in the coupling fluid for as short a time as possible. Subsequent to the ultrasound inspection, proper cleaning and drying of the samples are required. Refer to IPC J-STD-033 for the recommended bake out times and procedures to remove any ingressed moisture within a non-hermetic surface mount devices.

4.2 Views. All devices, shall have at least one image view made with the ultrasound penetrating the device in a direction perpendicular to the plane of the material interfaces, and for which there is acoustic continuity from the device exterior surface to the die attach interface(s) (Note: Generally, the Z-axis direction with the die attach parallel to the X-Y plane). For devices with no sealed air gap above the die (unlidded or non-hermetic devices), an image view made with the ultrasound directed from (reflected) or through (transmitted) the surface of the die to the material interface(s) may be specified (see figure 2030-1 for examples).

4.3 Recording and marking. The ultrasonic image shall be printed using paper and with at least a resolution of 300 data elements per inch nominal or stored in a digital file format by the equipment. The image shall be identified by unambiguously marking the paper on which the image is printed or stored within the digital file format with, but not limited to the following information:

4.3.1 Device manufacturer's name or code identification number.

4.3.2 Device type or part number.

4.3.3 Production lot number or date code or inspection lot number.

4.3.4 Ultrasonic image view number and date.

4.3.5 Device serial or cross reference numbers, where applicable.

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4.3.6 Ultrasonic laboratory identification, if other than device manufacturer.

4.3.7 Mounting material utilized for the die attachment, if known.

4.4 Recording with nonprint techniques. The use of documentation techniques, other than paper recording techniques is permitted (e.g., computer records, digital data files) provided that the equipment is capable of storing results of at least equal quality when compared to printed recording techniques, and all requirements specified herein, except those pertaining to the actual paper recording. If possible, the digital file name should incorporate a unique device identifier, such as a serial number, as part of the file name.

4.5 Serialized devices. When device serialization is required, each device shall be readily identified by a serial number.

4.6 Set up verification. When imaging lidded (sealed) devices, one open lid device of the same type and construction should be available to set up the equipment. The device may be a scrapped, nonoperational device or a known set up sample with known voids which will be used to identify internal landmarks and insure the equipment is properly operating.

4.7 Tests. Ultrasonic frequency gate settings, receiver attenuation, and other equipment settings shall be selected to achieve the resolution desired for the type of inspection being accomplished, in the example of die attach a resolution of 0.0254 mm (0.001 inch) in diameter, when inspecting through the die. Optimize the ultrasonic signal reflected from the material interface of interest, and distinguish image features with as great a contrast as possible. Ultrasonic images shall be made for each view required.

4.8 Operating personnel. Personnel who will perform ultrasonic inspection shall have training in ultrasonic imaging procedures and techniques so that defects revealed by this method can be validly interpreted and compared with applicable standards.

4.9 Interpretation of ultrasonic images. Ultrasonic images shall be inspected to determine that each device conforms to this standard and defective devices shall be rejected. Interpretation of the image shall be made under moderate light level conditions without a glare on the recording paper's surface or the display monitor. The image shall be viewed at an appropriate magnification to determine acceptance as specified herein. Automated percentage void or bond area calculations can be utilized instead of visual analysis upon confirming that the automated method is at least equal to the accuracy of the visual method (see figure 2030-2 for example of automated method).

4.10 Reports of records.

4.10.1 Reports of inspection. When specified, the manufacturer shall furnish inspection reports with each shipment of devices. The report shall describe the results of the ultrasonic inspection, and list the purchase order number or equivalent identification, the part number, the date code, the quantity inspected, the quantity rejected, and the date of test. For each rejected device, the part number, the serial number when applicable, and the cause for rejection shall be listed.

4.10.2 Ultrasonic image and report retention. When specified, the manufacturer shall retain a set of the ultrasonic images and a copy of the inspection report. These shall be retained for the period specified by the procuring activity in the acquisition document.

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4.11 Examination and acceptance criteria for die attach. In the examination of devices, the following aspects shall be considered unacceptable die attach interface, and devices that exhibit any of the following defects shall be rejected. If heat transfer is a concern, defects directly under the “hot” regions of the attach interface may be an issue and should be evaluated further with reliability testing.

4.12 Voids and Unbonded Area. When imaging devices ultrasonically, certain types of mounting material may not give true representation of voids; therefore the mounting material shall be noted on the inspection report, when known.

4.12. 1 Total of voids in excess of 50 percent of the total intended interface region (see figure 2030-3).

4.12.2 A single void in excess of 15 percent of the total intended interface region (see figure 2030-3).

4.12.3 A single corner void in excess of 10 percent of the total intended interface region (see figure 2030-3).

4.12.4 When the interface region of interest is divided into four equal quadrants by bisecting both pairs of opposite edges, any quadrant exhibiting interface region voids in excess of 70 percent of the intended interface quadrant region (see figure 2030-3).

In case of dispute, the percent of voiding shall be determined by actual measurement from the digital image using percentage void and bond image analysis functions with at least two threshold levels, i.e. B&W.

5. SUMMARY. The following details shall be specified in the applicable acquisition document:

5.1 Number of views, if other than indicated in 4.2.

5.2 Image marking, if other than indicated in 4.3 or marking of samples to indicate they have been ultrasonically imaged, if required.

5.3 Defects to be sought in the samples and criteria for acceptance or rejection, if other than indicated in 4.12.

5.4 Image and report retention per 4.10.2, if applicable.

5.5 Test reports, if other than indicated in 4.10.1.

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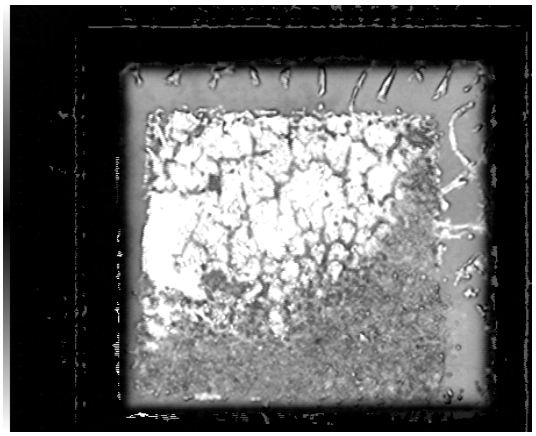
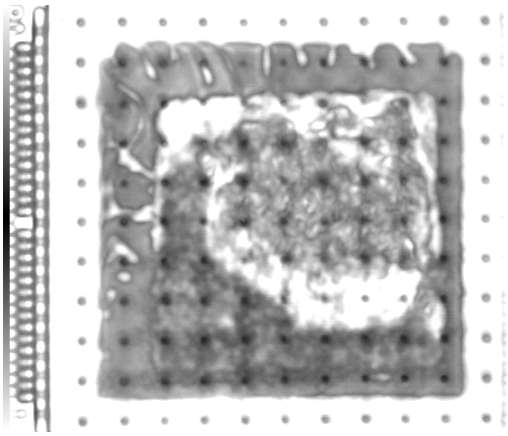
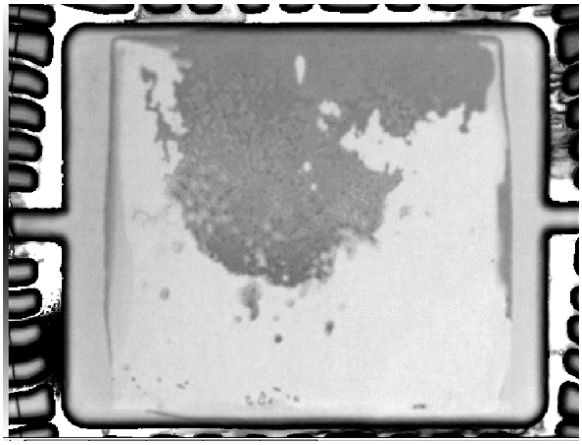


Example 2030-1a: Unlidded device reflection mode image through the die to die attach interface.



Example 2030-1b: Unlidded device reflection mode image through substrate side to die attach interface.



Example 2030-1c: Non-hermetic device reflection mode image through substrate side to die attach interface (see figure 2030-2 for example automated method analysis).

FIGURE 2030-1. Example Reflection Mode Grayscale Images of Die Attach Interface.

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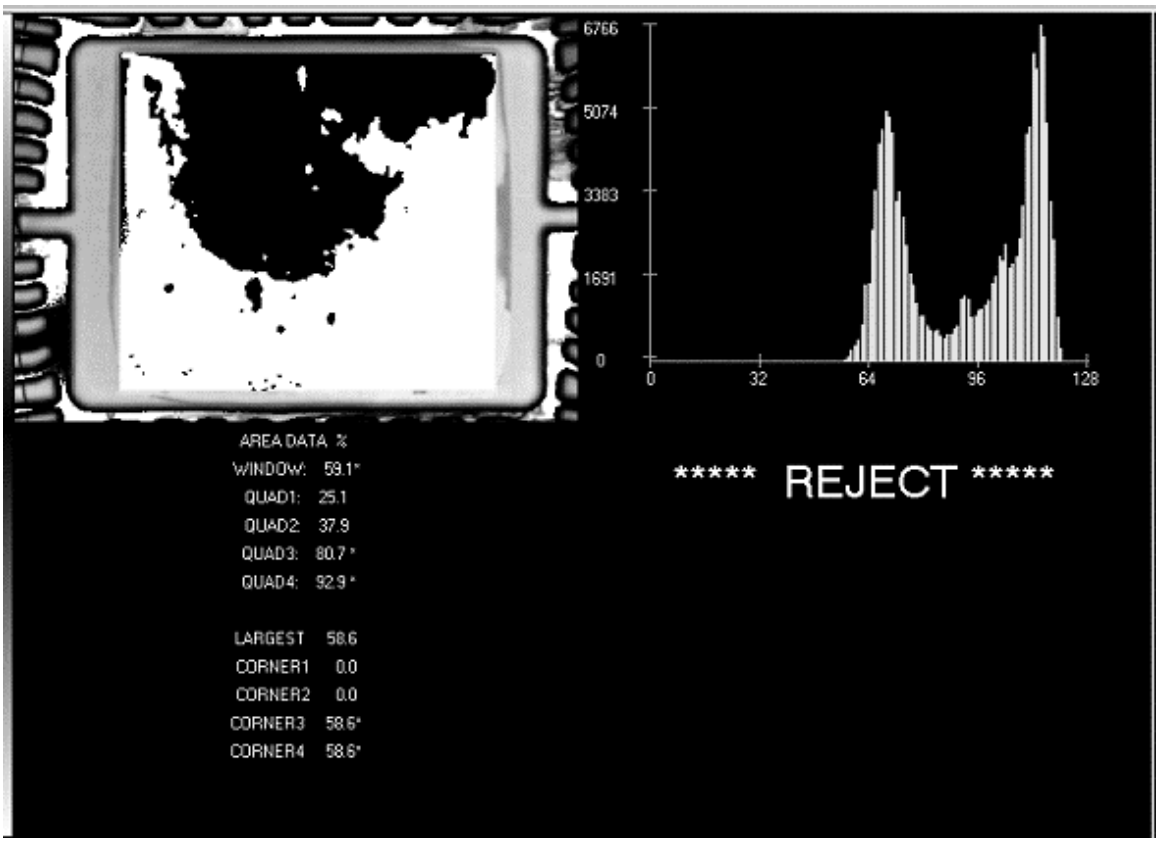

FIGURE 2030-2. Example Automated Method Analysis Report for Die Attach Interface.

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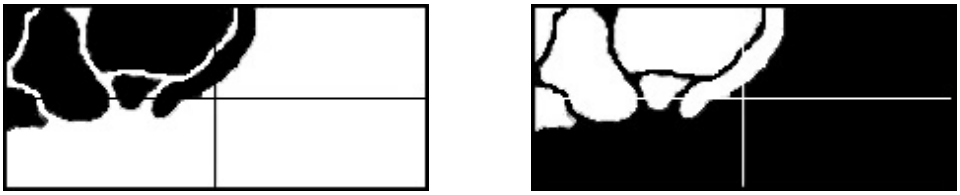
Typical Transmission Mode Image Analysis
(Two threshold levels – B&W)

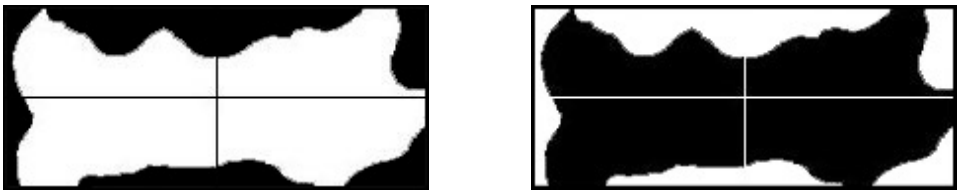
Typical Reflection Mode Image Analysis
(Two threshold levels – B&W)

Reject: Single void larger than 15 percent (%) of total intended interface.
Reject: Corner void larger than 10 percent (%) of total intended interface.

Accept: No single void larger than 15 percent (%) of total intended interface.
Accept: Corner void of area less than 10 percent (%) of total intended interface.



Reject: Quadrant more than 70 percent (%) unbonded.



Accept: All quadrants less than 70 percent (%) unbonded.

= Void or Unbonded area

= Void or Unbonded area

FIGURE 2030-3. Void criteria for die attach material interface inspection.

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METHOD 2031.1

FLIP-CHIP PULL-OFF TEST

1. PURPOSE. The purpose of this test is to measure the strength of internal bonds between a semiconductor die and a substrate to which it is attached in a face-bond configuration.

2. APPARATUS. The apparatus for this test shall consist of suitable equipment for applying the specified stress to the bonds. A calibrated measurement and indication of the applied stress in grams force (gf) shall be provided by equipment capable of measuring stresses up to twice the specified minimum limit value, with an accuracy of ±5 percent or ±0.25 gf, whichever is the greater tolerance.

3. PROCEDURE. The test shall be conducted using the following procedure. All die pulls shall be counted and the specified sampling, acceptance, and added sample provisions shall be observed, as applicable. The sample size number and accept number specified shall determine the number of die to be tested (not bonds). For hybrid or multichip devices, a minimum of 4 die or all die if four are not available on a minimum of 2 completed devices shall be used. All pull tests shall be performed prior to the application of encapsulants, adhesive, or any material which may increase the apparent bond strength.

When flip chips are bonded to substrates other than those in completed devices, the following conditions shall apply:

a. The sample of chips for this test shall be taken at random from the same chip population as that used in the completed devices that they are intended to represent.

b. The chips for this test shall be bonded on the same bonding apparatus as the completed devices, during the time period within which the completed devices are bonded.

c. The test chip substrates shall be processed, metallized, and handled identically with the completed device substrates, during the same time period within which the completed device substrates are processed.

3.1 Testing. The calibrated pull-off apparatus (see 2) shall include a pull-off rod (for instance, a current loop of nichrome or Kovar wire) having a cross-sectional area of 75 percent, +3 percent, -5 percent of the chip surface area. The rod shall make connection with a hard setting adhesive material (for instance, a cyanoacrylate or other adhesive possessing high tensile strength) on the back of the flip chip. The substrate shall be rigidly installed in the pull-off fixture and the pull-off rod shall make firm mechanical connection to the adhesive material. The die shall be pulled without shock, within 5° of the normal at a rate of 500 grams ±100 grams per second, until the die separates from the substrate. When a failure occurs, the force at the time of failure, the calculated force limit, and the failure category shall be recorded.

3.2 Failure criteria. Any flip-chip pull which results in separation under an applied stress less than 500 kg/in^2 x average solder bump area (in^2) x number of solder bumps shall constitute a failure.

3.2.1 Failure category. Failure categories are as follows: When specified, the stress required to achieve separation and the predominant category of separation or failure shall be recorded.

a. Silicon broken.

b. Lifted metallization from chip.

c. Separation at bond-chip interface.

d. Failure within bond.

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e. Separation at bond-substrate interface.

f. Lifted metallization from substrate.

g. Substrate broken.

4. SUMMARY. The following details shall be specified in the applicable acquisition document.

a. Minimum bond strength if other than specified in 3.2 or details of required strength distributions if applicable.

b. Sample size number and accept number and selection and the number of die to be tested, if other than 4

c. Requirement for reporting of separation forces and failure categories, when applicable (see 3.2.1).

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METHOD 2032.3

VISUAL INSPECTION OF PASSIVE ELEMENTS

1. PURPOSE. The purpose of this test is to inspect passive elements used for microelectronic applications, including RF/microwave, for the visual defects described herein. This test can be performed at the unmounted element level, or prior to sealing or encapsulation, on a 100 percent inspection basis, to detect and eliminate elements with visual defects that could lead to failure in normal application. It may also be performed on a sample inspection basis at the unmounted element level, or prior to sealing or encapsulation, to determine the effectiveness of the manufacturer's quality control and handling procedures for passive elements. The inspection criteria define the visual requirements for class H and class K elements (classes of passive elements refer to screening requirements of MIL-PRF-38534).

2. APPARATUS. The apparatus for this test shall include optical equipment capable of the specified magnification(s) and any visual standards (drawings, photographs, etc.) necessary to perform effective inspection and to enable the operator to make objective decisions as to the acceptability of the element being inspected. Adequate fixturing shall be provided for handling elements during inspection to promote efficient operation without inflicting damage to them.

3. PROCEDURE.

a. General. The element shall be inspected in a suitable sequence of observations within the specified magnification ranges to determine compliance with class H or class K visual requirements. If a specified visual inspection requirement is in conflict with element design, topology or construction, it shall be documented and specifically approved by the acquiring activity. Inspection for all of the visual defect criteria in this test shall be performed on all elements to which they are applicable. Where a criterion is intended for a specific element type, process, or technology, it has been so indicated.

b. Sequence of inspection. The order in which criteria are presented is not a required order of inspection and may be varied at the discretion of the manufacturer.

c. Inspection control. In all cases, inspections prior to the final pre-seal inspection shall be performed under the same quality program that is required at final pre-seal inspection. Care shall be exercised after unmounted element inspection to prevent any handling induced defects from occurring and to insure that defects created during such handling will be detected and rejected at final pre-seal inspection. If an element is electrostatic discharge (ESD) sensitive, then appropriate precautions shall be taken.

d. Inspection environment. Inspection of unmounted elements shall be conducted in a Class 8 controlled environment (see paragraph 3.i (7)), except that the maximum allowable relative humidity shall not exceed 65 percent. Final pre-seal visual inspection shall be conducted in a Class 8 controlled environment for class H and a Class 5 controlled environment for class K. During the time interval between final pre-seal visual inspection and preparation for sealing, mounted elements shall be placed in a Class 6 controlled environment. Both mounted and unmounted elements shall be in covered containers when transported from one controlled environment to another.

e. Magnification. "High magnification" inspection shall be performed perpendicular to the element with illumination normal to the element surface. Other angles at which the inspection can be performed, and at which the element can be illuminated, may be used at the option of the manufacturer if the visual presentation is the same as used in the originally specified conditions. "Low magnification" inspection shall be performed with either a monocular, binocular, or stereo microscope with the element under suitable illumination, tilted at an angle not greater than 30° from the perpendicular. The magnification ranges to be used for inspection are specified at the start of each section and are called out at the start of each major criteria grouping.

f. Reinspection. When inspection for product acceptance or quality verification of the visual requirements herein is conducted subsequent to the manufacturer's successful inspection, the additional inspection shall be performed at the magnification specified herein, unless a specific magnification is required by the acquisition document.

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g. Exclusions. Where conditional exclusions have been allowed, specific instruction as to the location and conditions for which the exclusion can be applied shall be documented in the assembly drawing.

h. Format and conventions. For ease of understanding and comparison, visual criteria are presented side-by-side in a columnar format. Class H criterion are presented in the left column and class K criterion are presented in the right column. When there are differences, the applicable parts of the class H criterion are underlined, for ease of comparison and clarity, and the differences only are shown in the class K column. When there are similarities, the phrase "same as class H" is used with no underlining of the class H criterion. If a requirement is not applicable to either product class, this is indicated by "N/A." A note in the class H column is applicable to class K unless otherwise specified in the class K column. A note in the class K column is applicable to class K only. Two kinds of notes are used herein, regular notes (NOTE:) and precautionary notes (PRECAUTIONARY NOTE:). A regular note is a integral part of a criterion. A precautionary note is not an integral part of the criterion but serves to alert the user to a requirement of the General Specification for Hybrids, MIL-PRF-38534. The phrases "except by design," "intended by design," "by design," or "unless otherwise specified by design" require that the element drawing be referenced to determine intent. For inspections performed at 100X, the criteria of "0.1 mil of passivation, separation, or metal" is satisfied by a "line of passivation, separation, or metal." Reference herein to "that exhibits" is satisfied when the visual image or visual appearance of the element under examination indicates a specific condition is present that does not require confirmation by any other method of testing. When other methods of test are used to confirm that a defect does not exist, they shall be approved by the acquiring activity. In the figures, cross-hatched areas represent metallization, blank areas represent resistor material and shaded areas represent exposed underlying material. The letters "x", "y", or "z" represent the dimension of interest and the letter "d" represents the original dimension. Most figures show the reject condition only.

i. Definitions:

(1) Active circuit area is all functional circuitry, operating metallization, or any connected combinations of these. In the case of resistors, it includes all resistor material that forms a continuous path between two metallized areas (usually bonding pads).

(2) Block resistor is a solid, rectangular shaped resistor, which, for purposes of trimming, is designed to be much wider than would be dictated by power density requirements and shall be identified in the approved manufacturer's precap visual implementation document.

(3) Bonding pad is a metallized area (usually located along the periphery of the element) at which an electrical connection is to be made by the user of the element.

(4) Bridging is complete connection between circuit features not intended to be connected.

(5) Conductive substrate is one that can conduct electricity. Copper or doped silicon, for example, are conductive substrates. Alumina and quartz, for example, are nonconductive (insulating) substrates.

(6) Contact window is an opening (usually square) through the oxide (or insulating) layer for the purpose of allowing contact by deposited material to the substrate.

(7) Controlled environment (Clean Room) is one that maintains the humidity and particle count in the working atmosphere below specified limits, as defined by ISO 14644-1. A Class 5 controlled environment has no more than100 (0.5 µm or greater) particles/cubic foot of air, a Class 6 controlled environment has no more than 1,000 (0.5 µm or greater) particles/cubic foot of air, and a Class 8 controlled environment has no more than 100,000 (0.5 µm or greater) particles/cubic foot of air. The maximum allowable relative humidity shall not exceed 65 percent.

(8) Corrosion is the gradual wearing away of metal, usually by chemical action, with the subsequent production of a corrosion product.

(9) Crazing is the presence of numerous, minute, interconnected surface cracks.

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(10) Crossover is the transverse crossing of metallization paths, without mutual electrical contact, achieved by the deposition of an insulating layer between the metallization paths in the area of crossing.

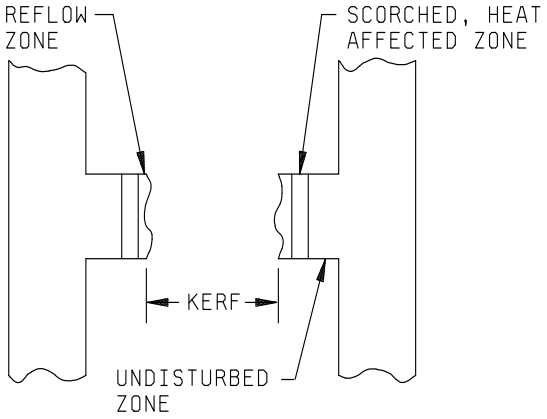
(11) Detritus is fragments of original or trim-modified resistor or conductor material.

(12) Dielectric is an insulating material that does not conduct electricity but may be able to sustain an electric field. It can be used in crossovers, as a passivation or a glassivation, or in capacitors.

(13) Foreign material is any material that is foreign to the element or any non-foreign material that is displaced from its original or intended position in the element. It is considered attached when it cannot be removed by a nominal gas blow (approximately 20 psig) or by an approved cleaning process. Conductive foreign material is any substance that appears opaque under those conditions of lighting and magnification used in routine visual inspection. Particles are considered to be embedded in glassivation when there is evidence of color fringing around the periphery of the particle.

(14) Glassivation is the top layer(s) of transparent insulating material that covers the active circuit area, including metallization, but not bonding pads. Crazing is the presence of numerous minute cracks in the glassivation. Cracks are fissures in the glassivation layer resulting from stress release or poor adhesion. The cracks can form loops over metallized areas.

(15) Kerf is the clear area in a trimmed resistor resulting from the removal of resistor material by the trimming operation. In laser trimming, the Kerf is bounded by the reflow zone (which is characterized by adherent, melted resistor material), the scorched heat-affected zone (which is characterized by discoloration of the resistor film without alteration of its physical form), and the undisturbed zone.



(16) Mar is a surface disturbance such as an indentation or a buff mark.

(17) Metallization, multilevel (conductors) is alternate layers of metallization, or other material used for interconnection, that are isolated from each other by a grown or deposited insulating material. The term "overlaying metallization" refers to any metallization layer on top of the insulating material.

(18) Metallization, multilayered (conductors) is two or more layers of metallization, or other material used for interconnection, that are not isolated from each other by a grown or deposited insulating material. The term "underlying metallization" refers to any metallization layer below the top layer of metallization.

(19) Metallization, operating (conductors) is all metallization (gold, aluminum, or other material) used for interconnection. Bonding pads are considered to be operating metallization. Alignment markers, test patterns, and identification markings are not considered to be operating metallization.

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(20) Narrowest resistor width is the narrowest portion of a given resistor prior to trimming; however, the narrowest resistor width for a block resistor may be specified in the approved manufacturer's design documentation.

(21) Neck-down is tapering of a resistor line at a metallization interface. Resistor material taper is typically equal on both sides of the line and is less abrupt than a void.

(22) Nicking (partial cut) is incomplete or inadvertent trimming of a resistor adjacent to the one being trimmed or of the next ladder rung of the same resistor.

(23) Nonplanar element is one that is essentially three-dimensional.

(24) Original separation is the separation dimension or space that is intended by design.

(25) Original width is the width dimension that is intended by design.

(26) Oxide defect is an irregularly shaped defect in the oxide characterized by two or three colored fringes at its edges.

(27) Passivation is the silicon oxide, silicon nitride, or other insulating material, that is grown or deposited directly on the element prior to the deposition of metal.

(28) Passivation step is a change in thickness of the passivation layer by design.

(29) Passive elements are planar resistors, capacitors, inductors, and patterned substrates (both single-layer and multilayer), and nonplanar chip capacitors, chip resistors, chip inductors, and transformers.

(30) Patterned substrate is a substrate on which conductors and components, such as resistors or capacitors, are formed using thick or thin film manufacturing techniques.

(31) Planar element is one that is essentially two-dimensional with all points in a common plane.

(32) Protrusion is a jutting-out of a circuit feature. Protrusion is typically caused by a photolithographic or screening defect.

(33) Resistor ladder is a resistor structure resembling a ladder in appearance that can be trimmed in incremental steps. A coarse ladder structure is one in which trimming of a rung results in a large incremental resistance change (one that can cause an out-of-tolerance condition to occur). A fine ladder structure is one in which trimming of a rung results in a small incremental resistance change (one that can not cause an out-of-tolerance condition to occur).

(34) Resistor ladder rung is that portion of a resistor ladder structure intended to be laser trimmed to result in an incremental change in resistance.

(35) Resistor loop is a resistor structure resembling a loop in appearance that can be trimmed. A coarse loop structure is one in which trimming results in a large resistance change (one that can cause an out-of-tolerance condition to occur). A fine loop structure is one in which trimming results in a small resistance change (one that cannot cause an out-of-tolerance condition to occur).

(36) Resistor material, self-passivating is one on which a conformal insulating layer can be thermally grown (such as tantalum nitride on which tantalum pentoxide is grown).

(37) Scorching is discoloration of laser trimmed thin film resistor material without alteration of its physical form.

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(38) Scratch, metallization is any cut, including probe marks, in the surface of the metallization. A mar on the metallization surface is not considered to be a scratch.

(39) Scratch, resistor is any cut in the resistor film. A mar on the resistor surface is not considered to be a scratch.

(40) Sidebar is that portion of a resistor ladder structure to which rungs are attached. Sidebars are not intended to be laser trimmed.

(41) Substrate is the supporting structural material into or upon which, or both, functional circuits are formed.

(42) Surface Acoustic Wave (SAW) element is a planar element fabricated typically using thin film manufacturing techniques on various substrate materials. Size varies as a function of frequency and design features include interdigitated fingers.

(43) Terminal is a metal area used to provide an electrical access point to functional circuitry.

(44) Thick film is conductive, resistive or dielectric material screen printed onto a substrate and fired at temperature to fuse into its final form.

(45) Thin film is conductive, resistive or dielectric material, usually less than 50,000Å in thickness that is deposited onto a substrate by vacuum evaporation, sputtering, or other means.

(46) Underlying material is any layer of material below the top-layer metallization. This includes metallization, resistor, passivation or insulating layers, or the substrate itself.

(47) Via is an opening in the insulating material in which a vertical conductive electrical connection from one metallization layer to another is made.

(48) Vitrification is conversion into glass or a glassy substance by heat and fusion.

(49) Void, metallization is any missing metallization where the underlying material is visible (exposed). Voids typically are caused by photolithographic, screen, or mask related defects, not by scratches.

(50) Void, resistor is any missing resistor material where the underlying material is visible (exposed). Voids typically are caused by photolithographic, screen, or mask related defects, not by scratches.

(51) Wraparound conductor is one which extends around the edge of the substrate by design.

(52) Coupling (air) bridge is a raised layer of metallization used for interconnection that is isolated from the surface of the element by an air gap or other insulating material.

(53) Pit is a depression produced in a substrate surface typically by non-uniform deposition of metallization or by non-uniform processing such as excessively powered laser trim pulses.

(54) Substrate, hard is the inorganic, rigid material into or upon which or both, functional circuits are formed. Typical materials are alumina and silicon.

(55) Blister, metallization is a hollow bump that can be flattened.

(56) Nodule, metallization is a solid bump that cannot be flattened.

(57) Substrate plug via is a cylinder-like volume in the substrate material filled with conductive material which makes electrical connection from contact areas on the top surface to the back surface of the substrate.

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(58) Whisker is a spontaneous columnar or cylindrical filament, usually of monocrystalline metal, emanating from the surface of a finish. Whiskers are not to be confused with dendrites. Whiskers have the following characteristics:

a. An aspect ratio (length/width) greater than 2.
b. Can be kinked, bent, or twisted.
c. Usually have a uniform cross-sectional shape.
d. May have striations along the length of the column and/or rings around the circumference of the column.
e. Length of 10 microns or more. Features less than 10 microns may be deemed important for research but are not considered significant for this test method.

(59) Dendrites are fern-like growths on the surface of a material. They can form as a result of electromigration of an ionic species produced during solidification.

(60) Probe marks are scratches on the bond pads made by probes during electrical measurements.

3.1. Thin film resistor element planar inspection (Including patterned substrates, discrete resistor elements, or other planar thin film element inspection). Inspection for visual defects described in this section shall be conducted on each thin film passive element. The "high magnification" inspection shall be within the range of 100X to 200X for both class H and class K. The "low magnification" inspection shall be within the range of 30X to 60X for both class H and class K. When inspection is performed prior to mounting, then elements utilizing ceramic or glass type substrates, without backside metallization, shall be inspected using backlighting for conditions of hair-line voiding or bridging. Patterned substrates that have geometries of 2.0 mils or greater shall be inspected at 10X to 60X magnification.

3.1.1. Operating metallization defects "high magnification". No element shall be acceptable that exhibits:

NOTE: The metallization defect criteria contained in this section apply to operating metallization only.

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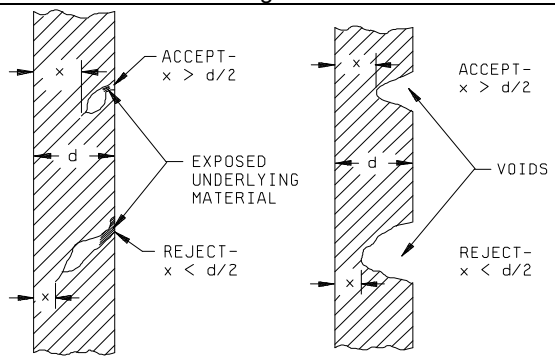
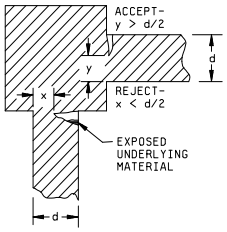
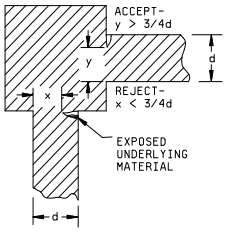
3.1.1.1. Metallization scratches and voids. No element shall be acceptable that exhibits:

Class H	Class K	Figures
a. A scratch, probe mark, or void in the metallization, excluding bonding pads, that both exposes underlying material anywhere along its length and leaves less than 50 percent of the original metallization width undisturbed (see 2032-1h). NOTE: Underlying material does not have to be exposed along the full length of the scratch.	a. Same as Class H.	 FIGURE 2032-1h
b. Scratch, probe mark, or void in the bonding pad area that both exposes underlying material and reduces the metallization path width, where it enters the bonding pad, and leaves less than 50 percent of its original metallization width. If two or more metallization paths enter a bonding pad, each shall be considered separately (see figure 2032-2h).	b. Less than 75 percent (see figure 2032-2k).	 FIGURE 2032-2h  FIGURE 2032-2k
c. Scratch that completely crosses the metallization path and damages the surface of the surrounding passivation, glassivation, or substrate on either side.	c. Same as Class H.	No figure supplied.
d. Scratches, probe marks, or voids in the bonding pad area that expose underlying material over greater than 25 percent of the original unglassivated metallization area. NOTE: For RF/microwave elements on nonconductive substrates, a void created in the bonding pad area as a result of wire bond removal for performance optimization or tuning, is not rejectable provided that the void remains entirely visible.	d. Same as Class H.	No figure supplied.

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3.1.1.2. Metallization corrosion. No element shall be acceptable that exhibits:

Class H	Class K	Figures
a. Any metallization corrosion. NOTE: Metallization having any localized discolored area shall be closely examined and rejected unless it is demonstrated to be a harmless film, glassivation interface, or other obscuring effect.	a. Same as class H.	No figure supplied.

3.1.1.3 Metallization adherence. No element shall be acceptable that exhibits:

Class H	Class K	Figures
a. Any metallization lifting, peeling, or blistering. NOTE: Nodules are acceptable. In order to determine if a bump in the metallization is a blister or a nodule, attempt to flatten the bump with a nonmetallic instrument. If the bump flattens, then it is a blister. NOTE: These criteria are not applicable to undercutting or separation induced anomalies (for example, metallization lifting due to scribe and break or diamond sawing) since these are not indicative of adhesion problems.	a. Same as Class H.	No figure supplied.

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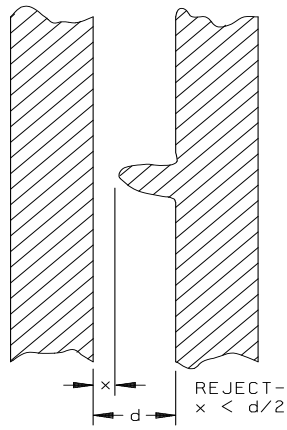
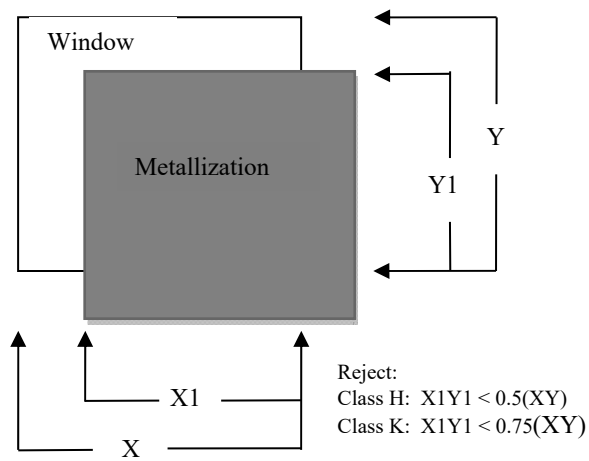
3.1.1.4. Metallization protrusion. No element shall be acceptable that exhibits:

Class H	Class K	Figures
a. Protrusion of metallization that reduces the original separation between adjacent operating metallization by greater than 50 percent (see figure 2032-3h).	a. Same as class H.	 FIGURE 2032-3h

3.1.1.5. Metallization alignment. No element shall be acceptable that exhibits:

Class H	Class K	Figures
a. A contact window that has less than 50 percent of its area covered by metallization (see figure 2032-4h).	a. 75 percent of its area (see figure 2032-4k).	 FIGURE 2032-4h & 2032-4k
b. Metallization path not intended to cover a contact window that is separated from the window by less than 0.1 mil unless by design.	b. Same as Class H.	No figure supplied.

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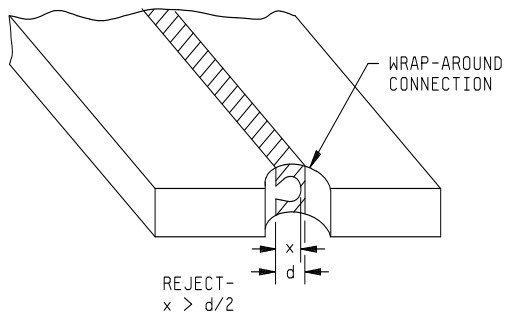
3.1.1.6. Metallized through-hole defects, "high magnification". No element shall be acceptable that exhibits:

Class H	Class K	Figures
a. Through-hole metallization that is not vertically continuous or that does not cover at least a continuous 50 percent of the inside, circumferential surface area unless by design.	a. Same as Class H.	No figure supplied.

3.1.1.7. Wrap-around connection defects, "high magnification". No element shall be acceptable that exhibits:

Class H	Class K	Figures
a. Unmetallized area in the edges of wrap-around connections greater than 50 percent of the largest dimension of the edge metallization (see figure 2032-5h).	a. Same as Class H.	 FIGURE 2032-5h

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3.1.1.8. Substrate plug via defects, “low magnification”. When inspected from each side of the substrate, no element shall be acceptable that exhibits:

NOTE: These are minimum requirements. Via flatness and other requirements shall be in accordance with the applicable detail drawings. The via fill may consist of thick film metallization.

Class H	Class K	Figures
a. A complete void through the via.	a. Same as Class H.	See figure 2032-6h.
b. Any lifting, peeling, or blistering of the via metallization.	b. Same as Class H.	See figure 2032-6h.
c. Via fill less than 75% of the total surface area of the via plug and less than 75% of the substrate thickness.	c. Same as Class H.	See figure 2032-6h.

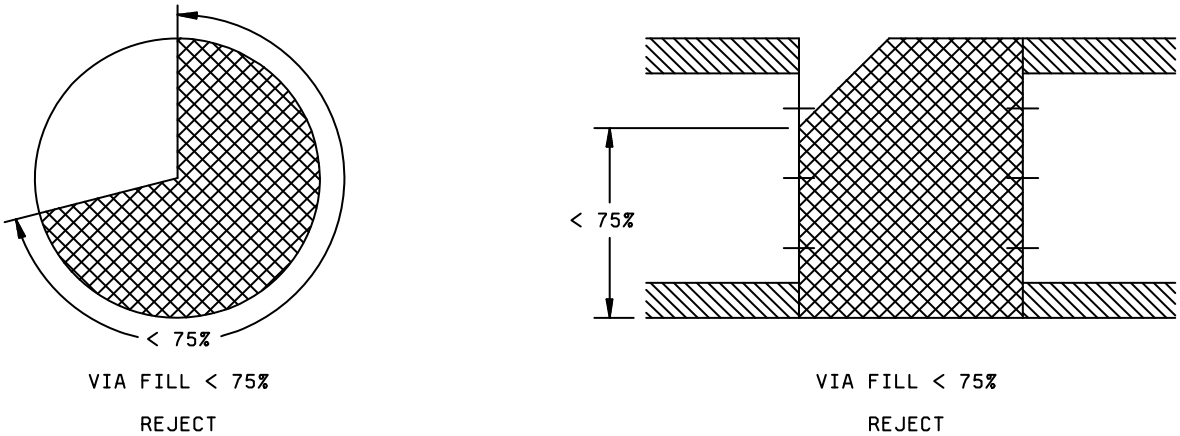

FIGURE 2032-6h. Classes H and K via plug fill criteria.

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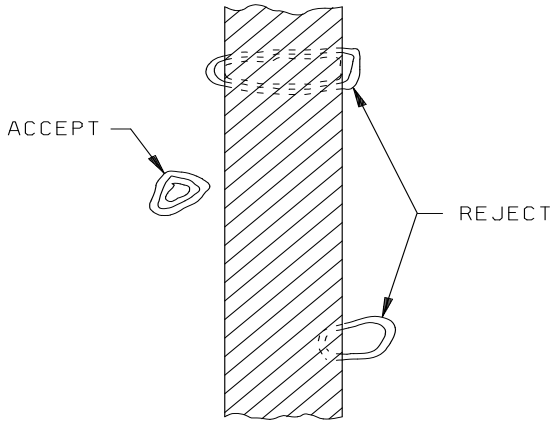
3.1.2. Passivation defects "high magnification". No element shall be acceptable that exhibits:

Class H	Class K	Figures
a. Either multiple lines (color fringing) or a complete absence of passivation visible at the edge and continuing under the metallization (see figure 2032-7h). A passivation defect that exhibits a line of separation from the metallization is acceptable. NOTE: These criteria apply to conductive substrate elements only. NOTE: Double or triple lines at the edge of the passivation defect indicate it can have sufficient depth to penetrate down to the bare substrate.	a. Same as class H.	 FIGURE 2032-7h

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3.1.3. Glassivation defects, "high magnification". No device shall be acceptable that exhibits:

Class H	Class K	Figures
a. Glass crazing or damage that prohibits the detection of visual criteria contained herein.	a. Same as Class H.	No figure supplied.
b. Any lifting or peeling of the glassivation. NOTE: Lifting or peeling of the glassivation is acceptable when it does not extend more than 1.0 mil from the designed periphery of the glassivation, provided that the only exposure of metallization is of adjacent bonding pads or of metallization leading from those pads.	b. Same as Class H.	No figure supplied.
c. A void in the glassivation that exposes two or more adjacent operating metallization paths, excluding bonding pad cutouts, unless by design.	c. Same as Class H.	No figure supplied.
d. Unglassivated non-active circuit areas greater than 5.0 mils in any dimension, unless by design.	d. Same as Class H.	No figure supplied.
e. Unglassivated areas at the edge of a bonding pad exposing the conductive substrate.	e. Same as Class H.	No figure supplied.

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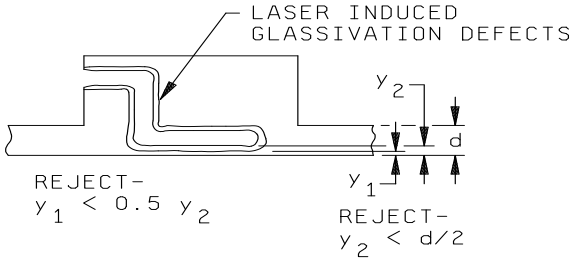
3.1.3. Glassivation defects, "high magnification" - Continued.

Class H	Class K	Figures
f. Glassivation covering more than 25 percent of a bonding pad area.	f. Same as Class H.	No figure supplied.
g. Crazing in glassivation over a resistor.	g. Same as Class H.	No figure supplied.
h. Misalignment of the glassivation that results in incomplete coverage of a resistor, unless by design.	h. Same as Class H.	No figure supplied.
i. Glassivation scratches or voids that expose any portion of a resistor or fusible link except for polycrystalline silicon links where the glassivation is opened by design.	i. Same as Class H.	No figure supplied.
j. Scratches in the glassivation that disturb metallization and bridge metallization paths.	j. Same as Class H.	No figure supplied.
k. Cracks (not crazing) in the glassivation that form a closed loop over adjacent metallization paths.	k. Same as Class H.	No figure supplied.
NOTE: Criteria of 3.1.3a-k can be excluded when the defects are due to laser trimming. In this case, the defects outside the kerf due to laser trimming shall not be more than one half the remaining resistor width, and shall leave a primary resistor path free of glassivation defects, equal to or greater than 50 percent of the narrowest resistor width, (see figure 2032-8h).	NOTE: Same as Class H.	 FIGURE 2032-8h

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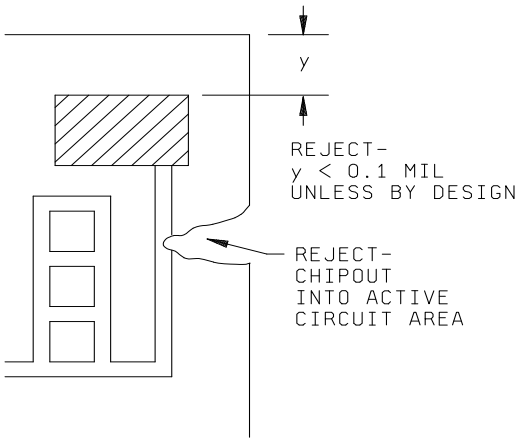
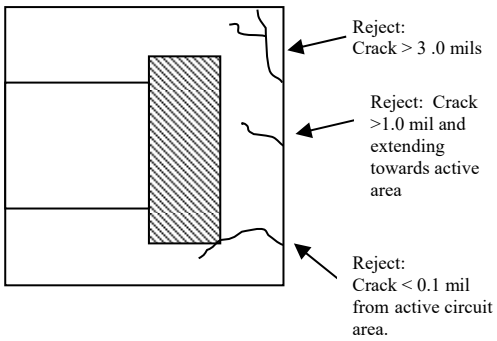
3.1.4. Substrate defects "high magnification". No element shall be acceptable that exhibits:

Class H	Class K	Figures
a. Less than 0.1 mil of separation between the operating metallization and the edge of the element unless by design (see figure 2032-9h). NOTE: For elements containing wrap-around conductors or for bonding pads of RF/microwave elements that are coincident with the element edge (as documented on the design drawing), this criteria does not apply. When bond pad metallization is coincident with the element edge, a minimum separation of 1.0 mil shall exist between the bonding pad metallization at the element edge and any non-common conductive surface.	a. Same as Class H.	 FIGURE 2032-9h
b. A chipout that extends into the active circuit area (see figure 2032-9h).	b. Same as class H.	See figure 2032-9h.
c. Any crack that exceeds 3.0 mils in length (see figure 2032-10h). NOTE: For fused quartz or glass substrates, no cracking is allowed.	c. Same as Class H.	 FIGURE 2032-10h
d. Any crack that does not exhibit 0.1 mil of separation from any active circuit area or operating metallization (see figure 2032-10h).	d. 0.25 mil (see figure 2032-10h).	See figure 2032-10h.
e. Any crack exceeding 1.0 mil in length extending from the element edge directly towards the active circuit area or operating metallization (see figure 2032-10h).	e. Same as class H.	See figure 2032-10h.

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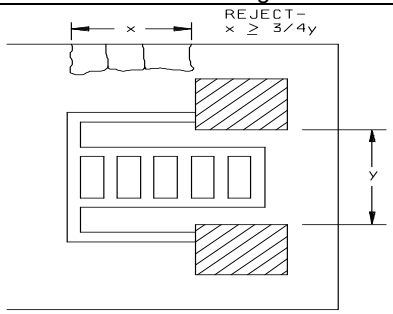
3.1.4. Substrate defects "high magnification" - Continued.

Class H	Class K	Figures
f. Not applicable.	f. Semicircular crack or combination of cracks along the element edge whose total length is equal to or greater than 75 percent of the narrowest separation between any two bonding pads (see figure 2032-11k).	 FIGURE 2032-11k
g. An attached portion of an active circuit area from an adjacent element.	g. Same as Class H.	No figure supplied.
h. Any crack that does not originate at an edge.	h. Same as Class H.	No figure supplied.
i. Holes through the substrate, unless by design.	i. Same as Class H.	No figure supplied.

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3.1.5 Foreign material defects "low magnification". No element shall be acceptable that exhibits:

Class H	Class K	Figures
a. For mounted and unmounted elements, unattached foreign material on the surface of the element. NOTE: All foreign material shall be considered to be unattached unless otherwise verified to be attached. Verification of attachments of foreign material whose longest dimensions are greater than 75 percent of the closest unglassivated conductive spacing shall be accomplished by a light touch with an appropriate mechanical device (i.e., needle, probe, pick, etc.). Verification of attachments of smaller material can be satisfied by suitable cleaning process approved by the acquiring or qualifying activity. All foreign material or particles may be removed, if possible, with a nominal gas blow (approximately 20 psig). NOTE: Semiconductor particles are considered to be foreign material.	a. Same as class H.	No figure supplied.

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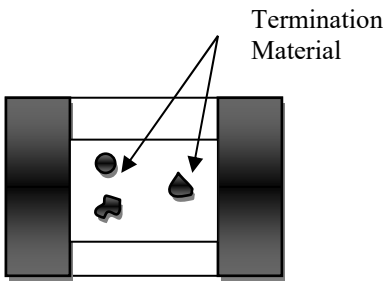
3.1.5 Foreign material defects "low magnification" - Continued.

Class H	Class K	Figures
b. Attached foreign material that bridges metallization paths, two package leads, lead to package metallization, functional circuit elements, junctions, or any combination thereof.	b. Same as class H.	No figure supplied.
c. Liquid droplets, ink drops, or chemical stains that appear to bridge any unglassivated or unpassivated active circuit areas.	c. Same as class H.	No figure supplied.
d. Attached foreign material that covers greater than 25 percent of a bonding pad area.	d. Same as class H.	No figure supplied.
e. Termination material splattered throughout the resistor, substrate, passivation, or glassivation (see figure 2032-12h). Reject for termination material greater than 10 mils in any direction. Reject for 5 or more areas between 3 and 10 mils in any direction.	d. Same as class H.	 FIGURE 2032-12h

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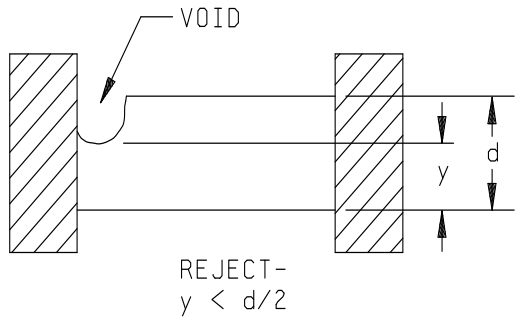
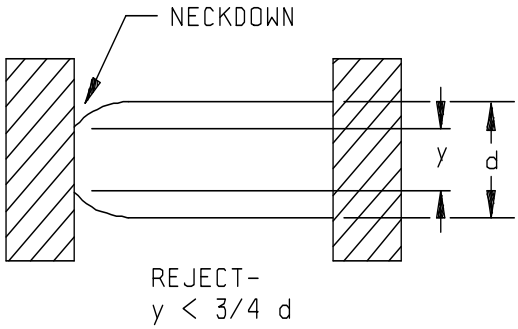
3.1.6 Thin film resistor defects, "high magnification". No element shall be acceptable that exhibits:

Class H	Class K	Figures
a. Voids at the terminal that reduces the resistor width to less than 50 percent of the original resistor width (see figure 2032-13h).	a. Same as Class H.	 FIGURE 2032-13h
b. Neckdown at the terminal that reduces the resistor width to less than 75 percent of the original resistor width (see figure 2032-14h).	b. Same as Class H.	 FIGURE 2032-14h
c. Any sharp (clearly defined) color change within 0.1 mil of the terminal. NOTE: A sharp color change close to the terminal usually indicates an abrupt reduction of resistor film thickness. This color change usually occurs in a straight line parallel to the terminal. A gradual color change, or a non-uniform or mottled color anywhere in the resistor, is not cause for rejection.	c. Same as Class H.	No figure supplied.

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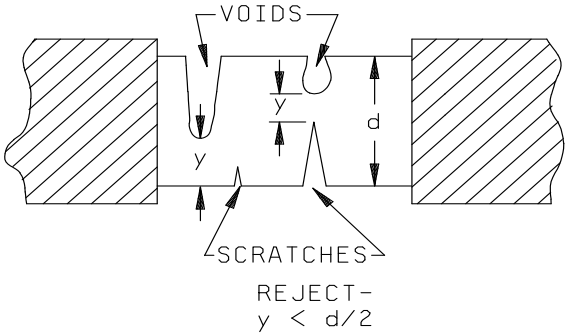
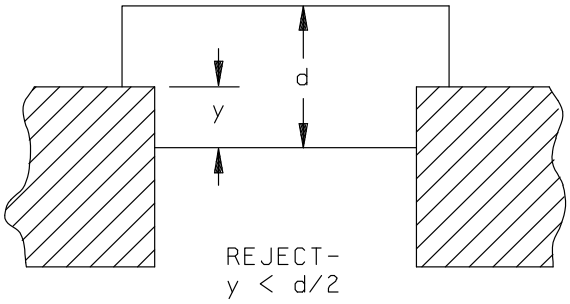
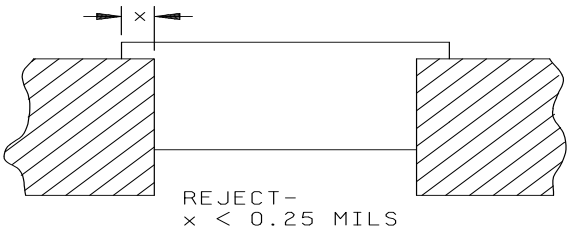
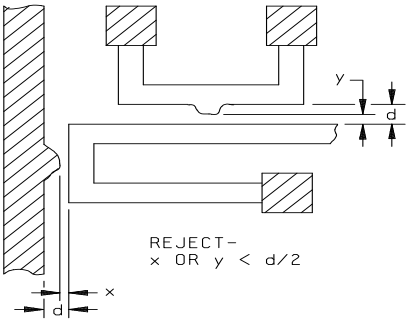
3.1.6 Thin film resistor defects, "high magnification" - Continued.

Class H	Class K	Figures
d. Any resistor film lifting, peeling or blistering.	d. Same as class H.	No figure supplied.
e. Reduction of resistor width, resulting from voids, scratches, or a laser trim kerf or a combination of these, that leaves less than 50 percent of the narrowest resistor width (see figure 2032-15h). PRECAUTIONARY NOTE: The maximum allowable current density requirement shall not be exceeded.	e. Same as class H.	 FIGURE 2032-15h
f. Contact overlap between the metallization and the resistor in which the width dimension "y" is less than 50 percent of the original resistor width (see figure 2032-16h).	f. Same as Class H.	 FIGURE 2032-16h
g. Contact overlap between the metallization and the resistor in which the length dimension "x" is less than 0.25 mil (see figure 2032-17h).	g. Same as class H.	 FIGURE 2032-17h
h. More than a 50 percent reduction of the original separation, between any two different resistors, or a resistor and metallization not associated with it (see figure 2032-18h).	h. Same as class H.	 FIGURE 2032-18h

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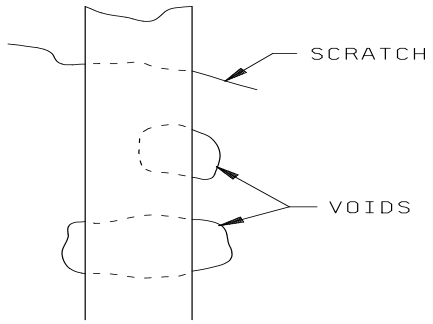
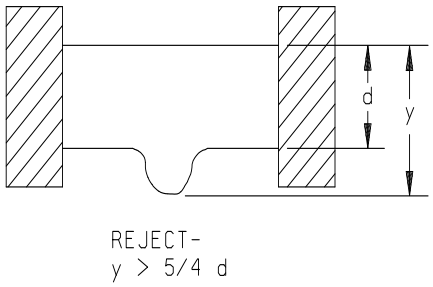
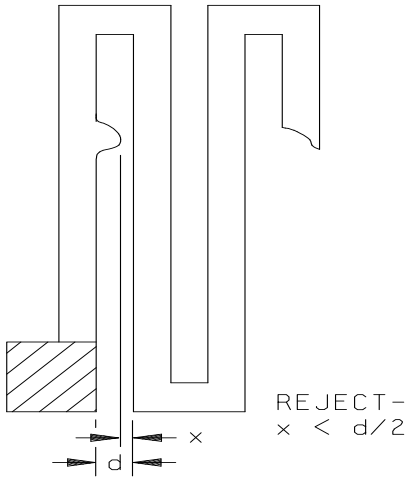
3.1.6. Thin film resistor defects, "high magnification" - Continued.

Class H	Class K	Figures
i. Any resistor that crosses a substrate irregularity (such as a void or scratch) (see figure 2032-19h). NOTE: This criterion is applicable to conductive substrates only.	i. Same as class H.	 FIGURE 2032-19h
j. Any increase in resistor width of a block resistor greater than 25 percent of the original resistor width (see figure 2032-20h).	j. Same as class H.	 FIGURE 2032-20h
k. Protruding resistor material within the same resistor structure that reduces the original separation to less than 50 percent (see figure 2032-21h). NOTE: This criterion applies to protrusion of resistor material resulting from a photo-lithographic defect.	k. Same as class H.	 FIGURE 2032-21h

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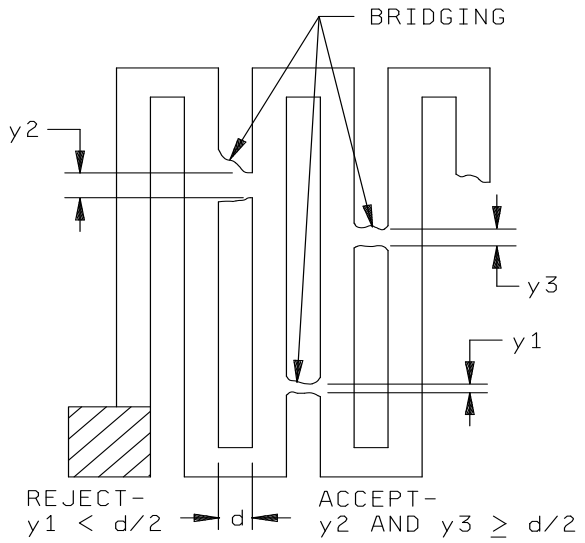
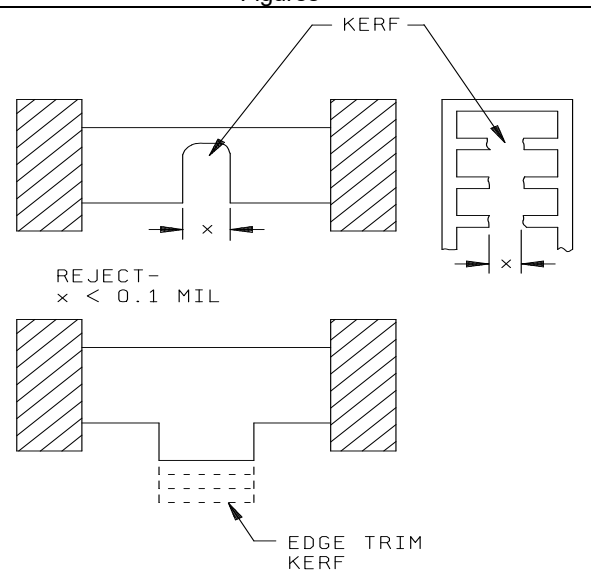
3.1.6 Thin film resistor defects, "high magnification" - Continued.

Class H	Class K	Figures
l. Bridging within the same resistor pattern where the width of the bridge is less than 50 percent of the narrowest line being bridged (see figure 2032-22h).	l. Same as class H.	 FIGURE 2032-22h

3.1.7 Laser trimmed thin film resistor defects, "high magnification". No element shall be acceptable that exhibits:

NOTE: The laser trim defect criteria contained in this section apply to active resistor areas only.

Class H	Class K	Figures
a. A Kerf width less than 0.1 mil (see figure 2032-23h). NOTE: This does not apply to edge trimming.	a. Same as class H.	 FIGURE 2032-23h

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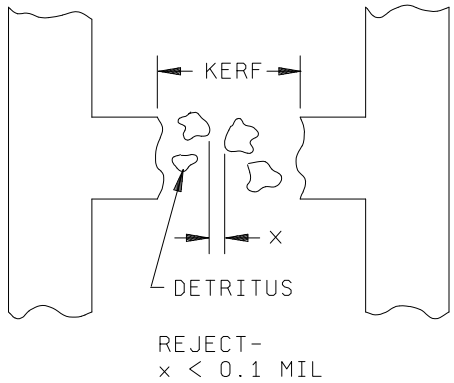
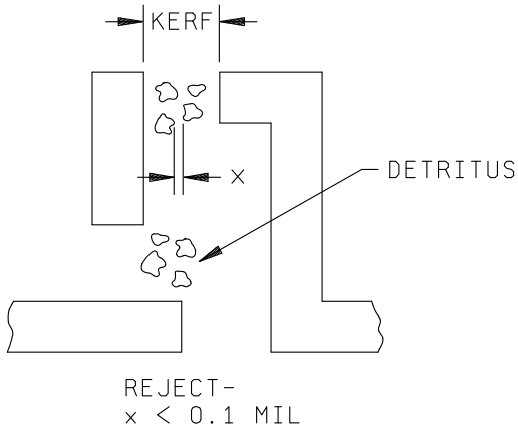
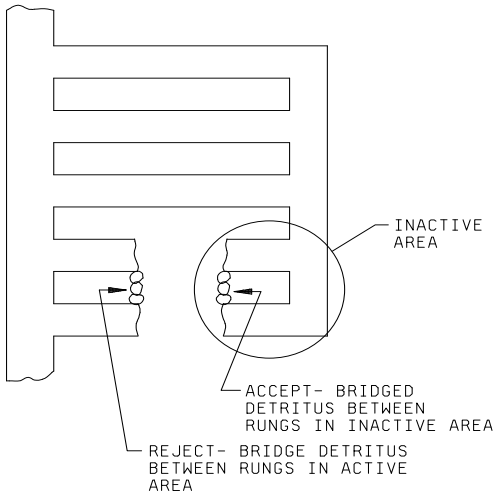
3.1.7 Laser trimmed thin film resistor defects, "high magnification" - Continued.

Class H	Class K	Figures
b. A Kerf containing particles of detritus. NOTE: For resistor materials that are self-passivating (such as tantalum nitride), detritus in the Kerf is allowed provided that a clear path of at least 0.1 mil in width exists in the Kerf. Such detritus shall be attached. Verification of attachment shall be accomplished using the techniques described in 3.1.5 (see figure 2032-24h). NOTE: This does not apply to edge trimming.	b. Same as class H.	 FIGURE 2032-24h
NOTE: In the case of a resistor loop made with self-passivating resistor material which is similar in configuration to the one shown in figure 2032-25h, there shall be at least one Kerf that contains a clear path of at least 0.1 mils in width, otherwise, the element shall be rejected.	Same as class H.	 FIGURE 2032-25h
c. Bridging of detritus between rungs in the active area of a resistor ladder structure (see figure 2032-26h). NOTE: Bridging of detritus in inactive areas is acceptable.	c. Same as class H.	 FIGURE 2032-26h

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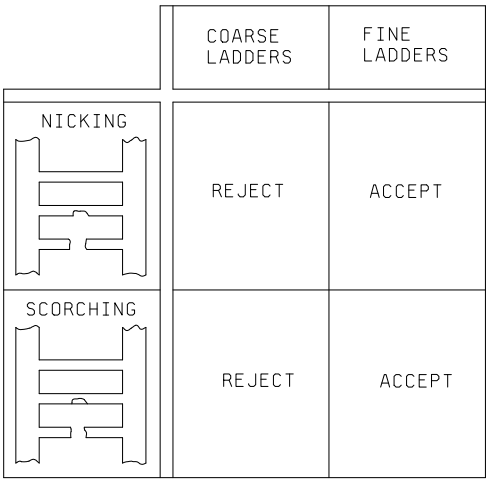
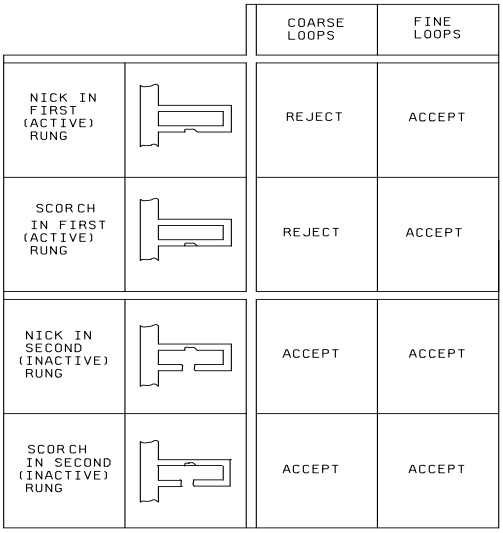
3.1.7 Laser trimmed thin film resistor defects, "high magnification" - Continued.

Class H	Class K	Figures
d. No nicking or scorching is allowed except as permitted below. NOTE: This does not apply to rungs in a fine resistor ladder structure (see figure 2032-27h). NOTE: See 3.i.(33) for a definition of coarse and fine resistor ladder structures. The element drawing must be referenced to determine if a given resistor ladder structure is coarse or fine.	d. Same as class H.	 FIGURE 2032-27h
d. (Continued.) NOTE: This criterion does not apply to the second rung of a resistor loop since the second rung is inactive. This criterion does not apply to a fine loop or to a resistor structure that is comprised of fine loops (see figure 2032-28h). NOTE: See 3.i.(35) for a definition of coarse and fine resistor loop structures. The element drawing must be referenced to determine if a given resistor loop structure is coarse or fine.	d. Same as Class H.	 FIGURE 2032-28h

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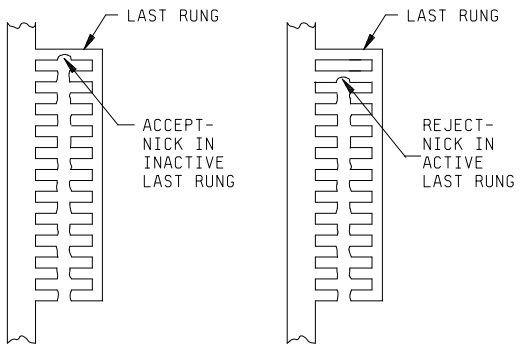
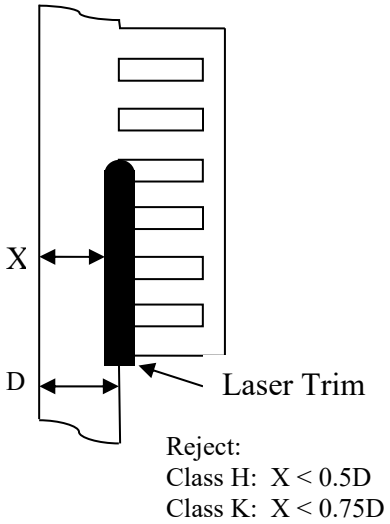
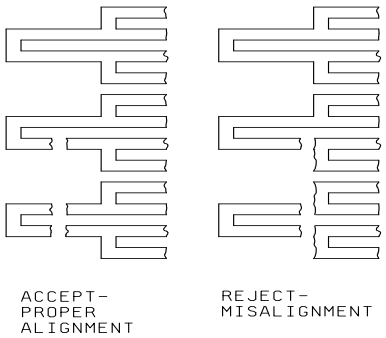
3.1.7. Laser trimmed thin film resistor defects, "high magnification" - Continued.

Class H	Class K	Figures
d. (Continued.) NOTE: This criterion does not apply to the last rung of a resistor coarse ladder if the last rung is inactive (see figure 2032-29h).	d. Same as class H.	 FIGURE 2032-29h
e. A Kerf or scorch which extends into a resistor ladder sidebar is acceptable as long as there is 50% of the line undisturbed (see figure 2032-30h).	e. 75% for class K (see figure 2032-30k).	 FIGURE 2032-30h & 2032-30k
f. Kerf or scorch misalignment which extends into resistor loop (see figure 2032-31h).	f. Same as class H.	 FIGURE 2032-31h

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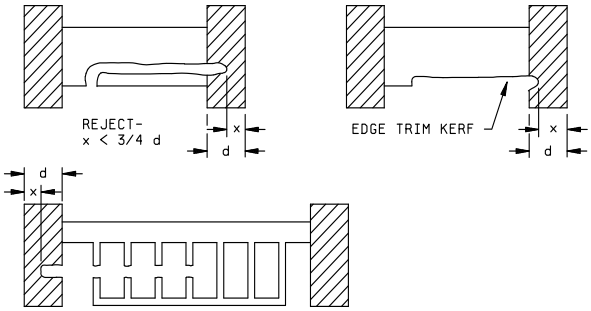
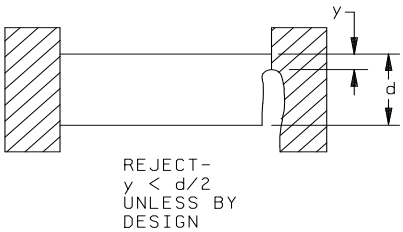
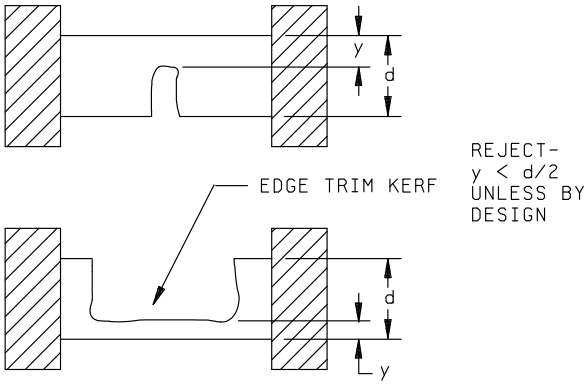
3.1.7 Laser trimmed thin film resistor defects, "high magnification" - Continued.

Class H	Class K	Figures
g. A Kerf which extends into metallization and leaves less than 75 percent of the metallization width undisturbed (see figure 2032-32h). NOTE: Opening a metallization link by design is acceptable.	g. Same as class H.	 FIGURE 2032-32h
h. A Kerf in a resistor, at the interface of the resistor material with the metallization, that leaves less than 50 percent of the original resistor width, unless by design. PRECAUTIONARY NOTE: The maximum allowable current density requirement shall not be exceeded. (see figure 2032-33h).	h. Same as class H.	 FIGURE 2032-33h
i. A Kerf in a resistor that leaves less than 50 percent of the original resistor width, unless by design. PRECAUTIONARY NOTE: The maximum allowable current density requirement shall not be exceeded (see figure 2032-34h).	i. Same as class H.	 FIGURE 2032-34h

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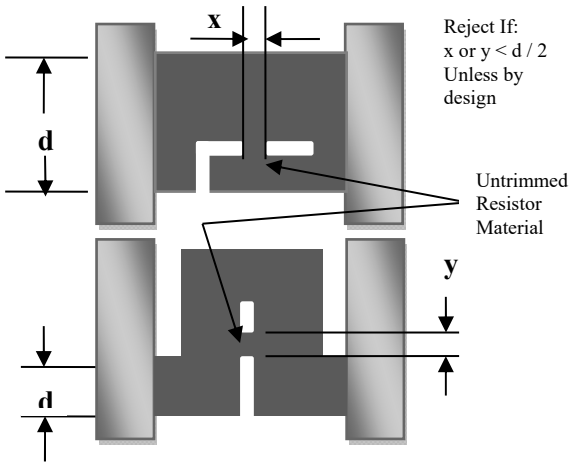
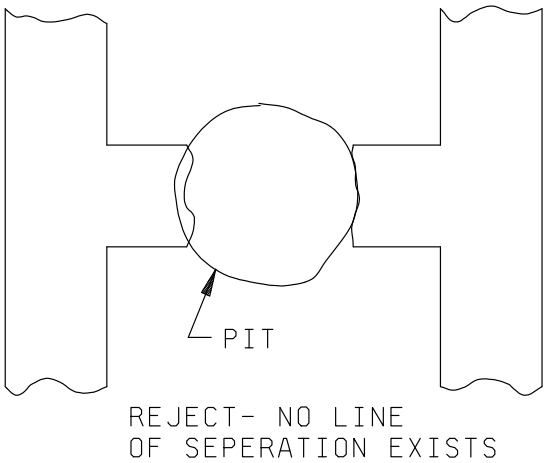
3.1.7. Laser trimmed thin film resistor defects, "high magnification" - Continued.

Class H	Class K	Figures
j. A floating Kerf in a resistor that leaves less than 50 percent of the narrowest resistor width unless by design (see figure 2032-35h). NOTE: A floating Kerf (one that is completely contained within the resistor) must meet this criterion. PRECAUTIONARY NOTE: The maximum allowable current density requirement shall not be exceeded.	j. Same as class H.	 FIGURE 2032-35h
k. Pits into the silicon dioxide of conductive substrate elements in the Kerf which does not show a line of separation between the pit and the resistor material (see figure 2032-36h).	k. Same as class H.	 FIGURE 2032-36h

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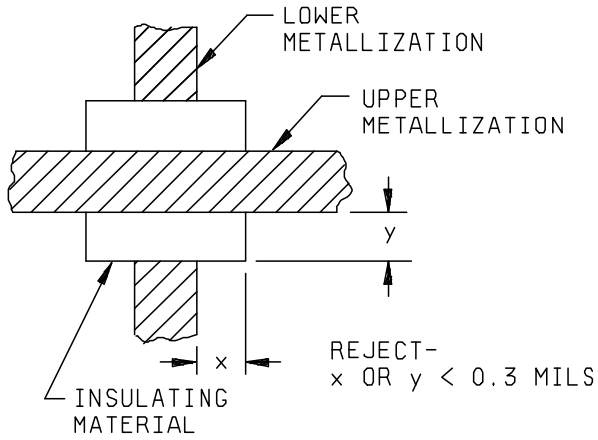
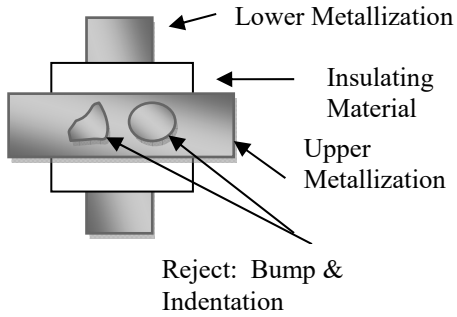
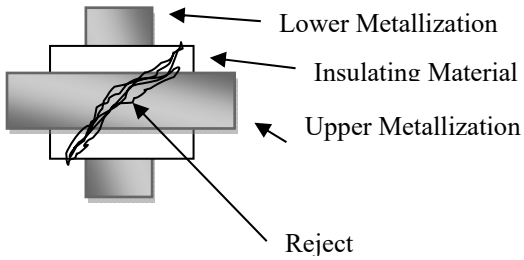
3.1.8. Multilevel thin film defects, "high magnification". No element shall be acceptable that exhibits:

Class H	Class K	Figures
a. Insulating material that does not extend beyond the width of the upper and lower metallization by 0.3 mil minimum (see figure 2032-37h).	a. Same as class H.	 FIGURE 2032-37h
b. Voids in the insulating material.	b. Same as class H.	No figure supplied.
c. A bump or indentation in the upper (overlaying) metallization at the intersection of the upper and lower metallization (see figure 2032-38h). NOTE: This criteria is not applicable to coupling (air) bridges. NOTE: There could be a problem with the insulating material.	c. Same as class H.	 FIGURE 2032-38h
d. Scratch that completely crosses the metallization and damages the insulating material surface on either side (see figure 2032-39h).	d. Same as class H.	 FIGURE 2032-39h

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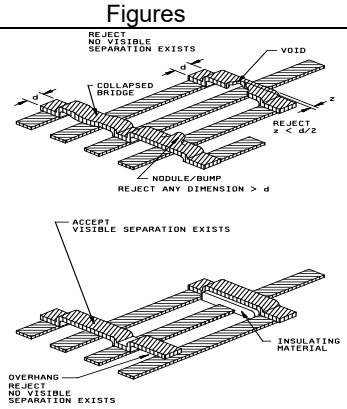
3.1.9 Coupling (air) bridge defects, "high magnification". No element shall be acceptable that exhibits:

Class H	Class K	Figures
a. A void in the coupling (air) bridge metallization that leaves less than 50 percent of the original metallization width undisturbed. (See figure 2032-40h).	a. Same as class H.	 FIGURE 2032-40h
b. Nodules or bumps that are greater, in any dimension, than the original coupling (air) bridge metallization width. (See figure 2032-40h).	b. Same as class H.	See figure 2032-40h.
c. Coupling (air) bridge that contacts underlying operating metallization. (See figure 2032-40h).	c. Same as class H.	See figure 2032-40h.
d. Attached, conductive foreign material that is greater, in any dimension, than 50 percent of the original coupling (air) bridge metallization width.	d. Same as class H.	No figure supplied.
e. No visible separation between the coupling (air) bridge and the underlying operating metallization. NOTE: This criterion is not applicable when an insulating material is used between the coupling (air) bridge and the underlying metallization. (See figure 2032-40h).	e. Same as class H.	See figure 2032-40h.
f. Coupling (air) bridge metallization overhang over adjacent operating metallization, not intended by design, that does not exhibit a visible separation. (See figure 2032-40h).	f. Same as class H.	See figure 2032-40h.

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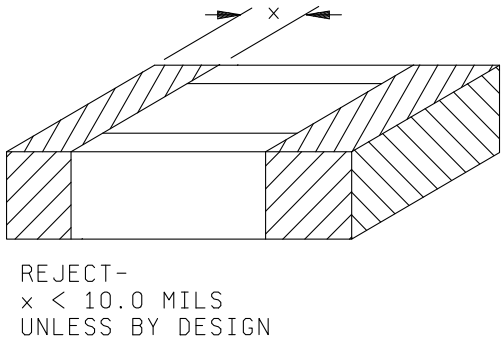
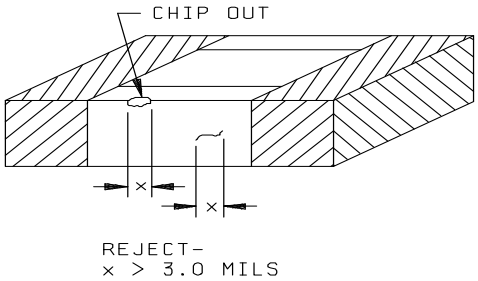
3.1.9 Coupling (air) bridge defects, "high magnification" - Continued.

Class H	Class K	Figures
g. Mechanical damage to a coupling (air) bridge that results in depression (lowering) of coupling (air) bridge metallization over underlying operating metallization.	g. Same as class H.	No figure supplied.

3.1.10. Additional criteria for thin film nonplanar resistor defects “low magnification”. The thin film resistor element planar inspection criteria, also applies to thin film nonplanar resistors. The "low magnification" inspection shall be within the range of 10X to 60X. No element shall be acceptable that exhibits:

Class H	Class K	Figures
a. Metallized termination width less than 10.0 mils unless by design (see figure 2032-41h).	a. Same as class H.	 FIGURE 2032-41h
b. A crack, chipout or void in the substrate greater than 3.0 mils in any direction (see figure 2032-42h).	b. Same as class H.	 FIGURE 2032-42h
c. Build-up of termination material on metallized termination areas greater than 3.0 mils high for weldable metallized terminations or 8.0 mils high for solderable metallized terminations (see figure 2032-43h). Note: Whiskers are not acceptable (See definitions, section 3i).	c. Same as class H.	 FIGURE 2032-43h

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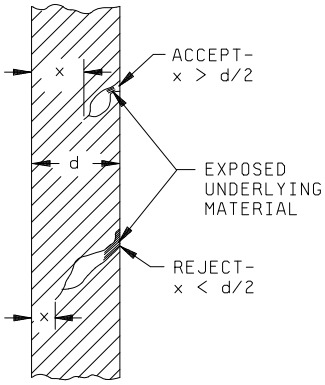
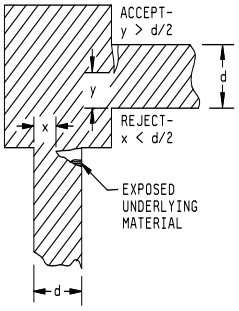
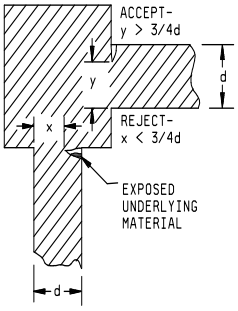
3.2. Thick film resistor element planar inspection (Including patterned substrates, discrete resistor elements, or other planar thick film element inspection). Inspection for visual defects described in this section shall be conducted on each thick film passive element. All inspection shall be performed at "low magnification" within the range of 10X to 60X magnification for both class H and class K.

3.2.1. Operating metallization defects "low magnification". No element shall be acceptable that exhibits:

NOTE: The metallization defect criteria contained in this section apply to operating metallization only.

3.2.1.1. Metallization scratches and voids. No element shall be acceptable that exhibits:

Class H	Class K	Figures
a. A scratch, probe mark, or void in the metallization, excluding bonding pads, that both exposes underlying material anywhere along its length and leaves less than 50 percent of the original metallization width undisturbed (see figure 2032-44h). NOTE: Underlying material does not have to be exposed along the full length of the scratch.	a. Same as Class H.	 FIGURE 2032-44h
b. Scratch, probe mark, or void in the bonding pad area that both exposes underlying material and reduces the metallization path width, where it enters the bonding pad, to less than 50 percent its original metallization width. If two or more metallization paths enter a bonding pad, each shall be considered separately (see figure 2032-45h).	b. Less than 75 percent (see figure 2032-45k).	 FIGURE 2032-45h  FIGURE 2032-45k
c. Scratch, probe marks, or voids in the bonding pad area that expose underlying material over more than 25 percent of the original metallization area.	c. Same as class H	No figure supplied.

3.2.1.2. Metallization corrosion. No element shall be acceptable that exhibits:

Class H	Class K	Figures
a. Any metallization corrosion.	a. Same as class H.	No figure supplied.

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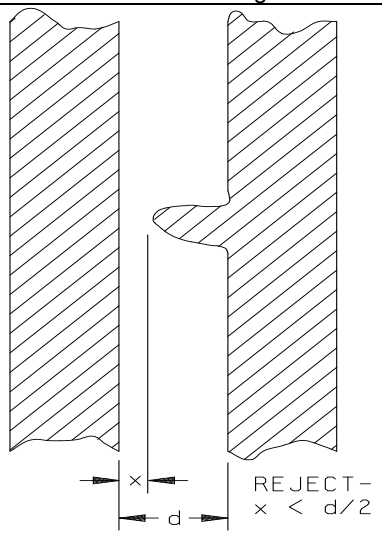
3.2.1.3. Metallization adherence. No element shall be acceptable that exhibits:

Class H	Class K	Figures
a. Any metallization lifting, peeling, or blistering. NOTE: Nodules are acceptable. In order to determine if a bump in the metallization is a blister or a nodule, attempt to flatten the bump with a nonmetallic instrument. If the bump flattens, then it is a blister. NOTE: These criteria are not applicable to separation induced anomalies (for example, metallization lifting due to scribe and break or diamond sawing) since these are not indicative of adhesion problems.	a. Same as class H.	No figure supplied.

3.2.1.4. Metallization protrusion. No element shall be acceptable that exhibits:

Class H	Class K	Figures
a. More than 50 percent reduction of the original design separation, between any protruding metallization and adjacent metallization paths (see figure 2032-46h).	a. Same as class H.	 FIGURE 2032-46h

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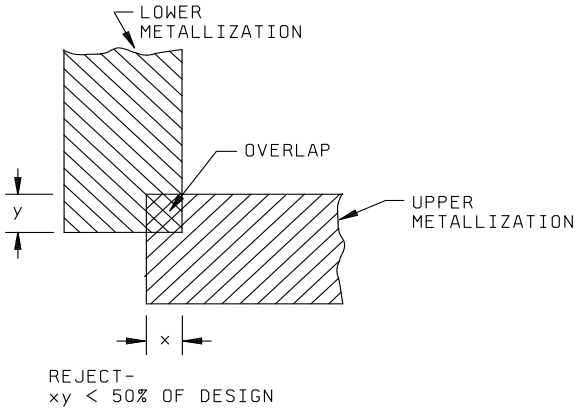
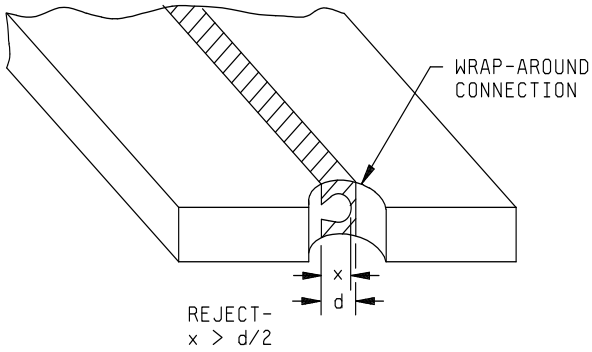
3.2.1.5. Metallization overlap. No element shall be acceptable that exhibits:

Class H	Class K	Figures
a. Contact overlap between the upper and lower metallization that is less than 50 percent of the designed contact overlap area (see figure 2032-47h). NOTE: The overlap area is that area in which the upper metallization actually contacts the lower metallization.	a. Same as class H.	 FIGURE 2032-47h

3.2.1.6. Metallized through-hole defects, "low magnification". No element shall be acceptable that exhibits:

Class H	Class K	Figures
a. Through-hole metallization that is not vertically continuous or that does not cover at least a continuous 50 percent of the inside, circumferential surface area unless by design.	a. Same as class H.	No figure supplied.

3.2.1.7. Wrap-around connection defects, "low magnification". No element shall be acceptable that exhibits:

Class H	Class K	Figures
a. Unmetallized area in the edges of wrap-around connections greater than 50 percent of the largest dimension of the edge metallization (see figure 2032-48h).	a. Same as class H.	 FIGURE 2032-48h

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3.2.1.8. Substrate plug via defects, “low magnification”. When inspected from each side of the substrate, no element shall be acceptable that exhibits:

NOTE: These are minimum requirements. Via flatness and other requirements shall be in accordance with the applicable detail drawings.

Class H	Class K	Figures
a. A complete void through the via.	a. Same as Class H.	See figure 2032-49.
b. Any lifting, peeling, or blistering of the via metallization.	b. Same as Class H.	See figure 2032-49.
c. Via fill less than 75% of the total surface area of the via plug and less than 75% of the substrate thickness.	c. Same as Class H.	See figure 2032-49.

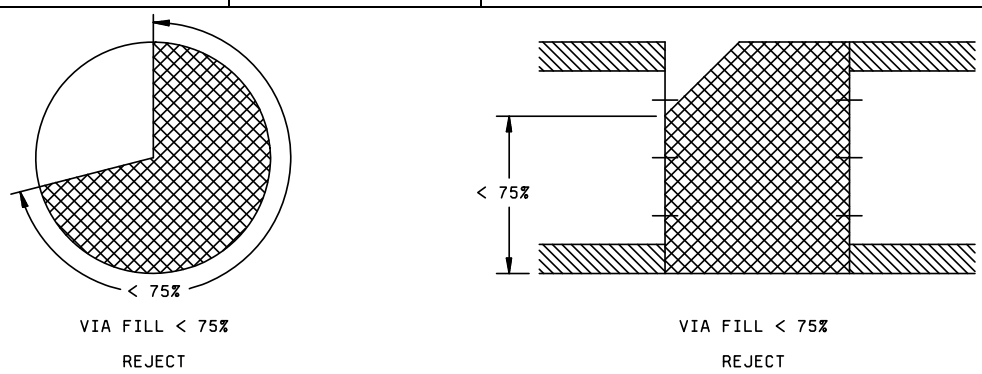

FIGURE 2032-49. Classes H and K via plug fill criteria

3.2.2. Substrate defects, "low magnification". No element shall be acceptable that exhibits:

Class H	Class K	Figures
a. Less than 1.0 mil separation between the operating metallization and the edge of the element unless by design and necessary for element function (see figure 2032-50h). NOTE: This criterion does not apply to substrates designed for wraparound conductors. NOTE: This criterion does not apply to elements that are to be mounted on substrates (e.g., planar chip resistors).	a. Same as class H.	No figure supplied.

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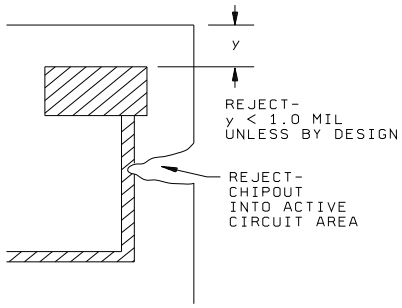
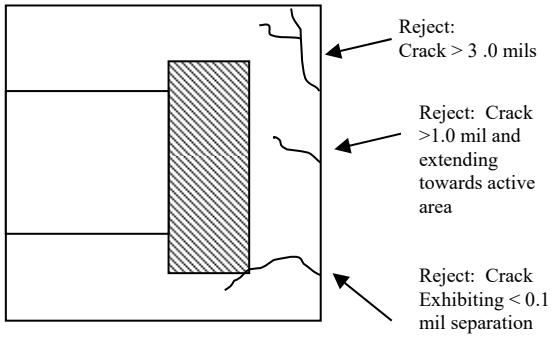
3.2.2. Substrate defects, "low magnification" - Continued.

Class H	Class K	Figures
b. A chipout that extends into the active circuit area (see figure 2032-50h).	b. Same as class H.	 FIGURE 2032-50h
c. Any crack that exceeds 3.0 mils in length (see figure 2032-51h). NOTE: For fused quart or crystalline substrates, no cracking is allowed.	c. Same as Class H.	 FIGURE 2032-51H
d. Any crack that does not exhibit 1.0 mil of separation from any active circuit area or operating metallization (see figure 2032-51h).	d. Same as class H.	See figure 2032-51h.
e. Any crack exceeding 1.0 mil in length extending from the element edge directly towards the active circuit area or operating metallization (see figure 2032-51h).	e. Same as class H.	See figure 2032-51h.

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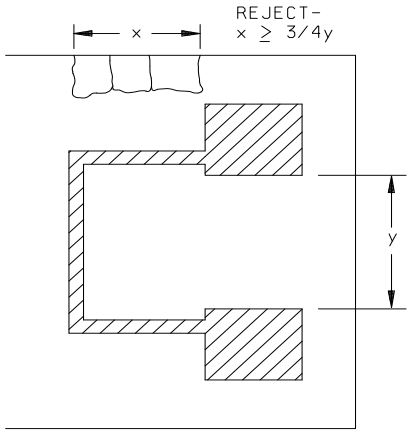
3.2.2. Substrate defects, "low magnification" - Continued.

Class H	Class K	Figures
f. Not applicable.	f. Semicircular cracks that are combined along the element edge whose total length is equal to or greater than 75 percent of the narrowest separation between any two bonding pads (see figure2032-52k).	 FIGURE 2032-52k
g. An attached portion of a circuit area from an adjacent element.	g. Same as class H.	No figure supplied.
h. Any crack that does not originate at an edge.	h. Same as class H.	No figure supplied.
i. Holes through the substrate, unless by design.	i. Same as class H.	No figure supplied.
j. Patterned substrates having a section broken out around a substrate mounting hole (intended for substrate-to-post attachment) that is greater than 25 percent of the mounting hole circumference.	j. Same as class H.	No figure supplied.

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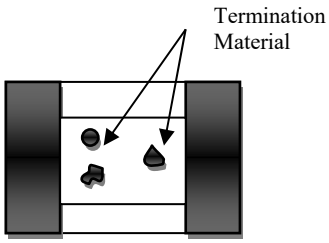
3.2.3. Foreign material defects "low magnification". No element shall be acceptable that exhibits:

Class H	Class K	Figures
a. For mounted and unmounted elements, unattached foreign material on the surface of the element. NOTE: All foreign material shall be considered to be unattached unless otherwise verified to be attached. Verification of attachments of foreign material whose longest dimensions are greater than 75 percent of the closest unglassivated conductive spacing shall be accomplished by a light touch with an appropriate mechanical device (i.e., needle, probe, pick, etc.). Verification of attachments of smaller material can be satisfied by suitable cleaning process approved by the acquiring or qualifying activity. All foreign material or particles may be removed, if possible, with a nominal gas blow (approximately 20 psig). NOTE: Semiconductor particles are considered to be foreign material.	a. Same as class H.	No figure supplied.
b. Attached foreign material that bridges metallization paths, two package leads, lead to package metallization, functional circuit elements, junctions., or any combination thereof.	b. Same as class H.	No figure supplied.
c. Liquid droplets, ink drops, or chemical stains that appear to bridge any unglassivated or unpassivated active circuit areas.	c. Same as class H.	No figure supplied.
d. Attached foreign material that covers greater than 25 percent of a bonding pad area.	d. Same as class H.	No figure supplied.
e. Termination material splattered throughout the resistor, substrate, passivation, or glassivation (see figure 2032-53h). Reject for termination material greater than 10 mils in any direction. Reject for 5 or more areas between 3 and 10 mils in any direction.	e. Same as class H.	 FIGURE 2032-53h

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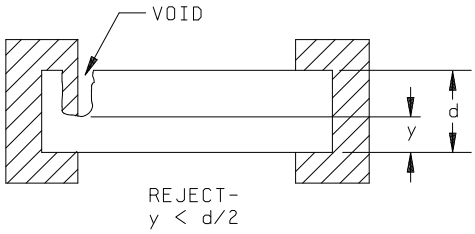
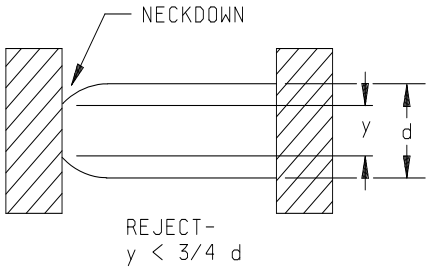
3.2.4. Thick film resistor defects, "low magnification". No element shall be acceptable that exhibits:

Class H	Class K	Figures
a. A reduction of the resistor at the terminal due to voids to less than 50 percent of the original resistor width (see figure 2032-54h).	a. Same as Class H.	 FIGURE 2032-54h
b. Reduction of the resistor at the terminal, due to neckdown less than 75 percent, to the original resistor width (see figure 2032-55h).	b. Same as Class H.	 FIGURE 2032-55h
c. Any resistor film lifting, peeling, or blistering.	c. Same as class H.	No figure supplied.
d. Crack in the resistor greater than 1.0 mil in length. NOTE: Irregularities such as fissures in resistor material that are created during firing, and that do not expose the underlying material, are not considered to be cracks.	d. Same as class H.	No figure supplied.
e. Evidence of resistor repair by overprinting or any other means.	e. Same as class H.	No figure supplied.
f. Separation between any two resistors that is less than 50 percent of the original separation.	f. Same as class H.	No figure supplied.
g. Separation between any resistor and conductor combination that is less than 50 percent of the original separation.	g. Same as class H.	No figure supplied.
h. Increase in resistor width greater than 25 percent of the original design width.	h. Same as class H.	No figure supplied.

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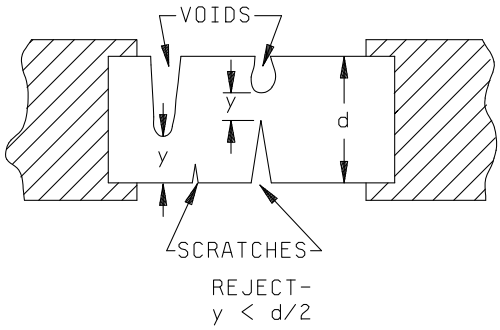
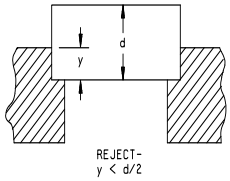
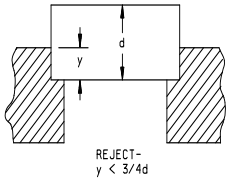
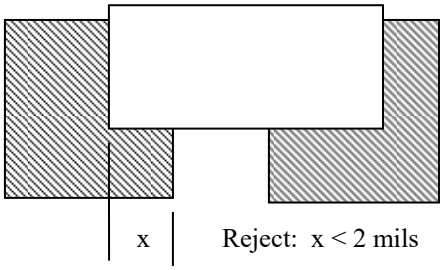
3.2.4. Thick film resistor defects, "low magnification" - Continued.

Class H	Class K	Figures
i. Resistor material that is closer than 1.0 mil to the edge of the substrate.	i. Same as class H.	No figure supplied.
j. Reduction of resistor width resulting from voids, scratches, or chipouts, or a combination of these, that leaves less than 50 percent of the narrowest resistor width (see figure 2032-56h). PRECAUTIONARY NOTE: The maximum allowable current density requirement shall not be exceeded.	j. Same as class H.	 FIGURE 2032-56h
k. Contact overlap between the metallization and the resistor in which the actual width dimension "y" is less than 50 percent of the original resistor width (see figure 2032-57h).	k. Less than 75 percent (see figure 2032-49k).	 FIGURE 2032-57h  FIGURE 2032-57k
l. Contact overlap between the metallization and the resistor in which the length dimension "x" is less than 2.0 mils (see figure 2032-58h).	l. Same as class H.	 FIGURE 2032-58h
m. Voids, misalignment, lifting, or peeling of glassivation that results in less than 90 percent coverage of the resistor area, unless by design.	m. Same as class H.	No figure supplied.
n. Crazing of glassivation over a resistor.	n. Same as class H.	No figure supplied.

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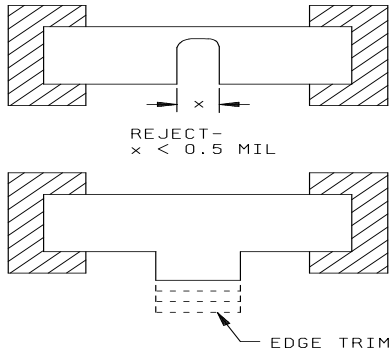
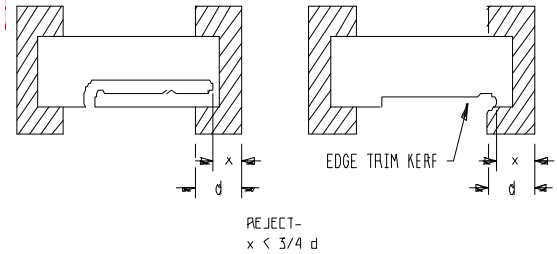
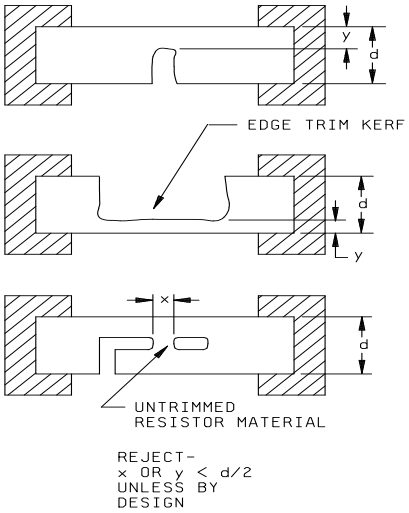
3.2.5. Trimmed thick film resistor defects, "low magnification". No element shall be acceptable that exhibits:

NOTE: The trim defect criteria contained in this section apply to active resistor areas only.

Class H	Class K	Figures
a. A Kerf width less than 0.5 mil (see figure 2032-59h). NOTE: This does not apply to edge trimming.	a. Same as class H.	 FIGURE 2032-59h
b. A Kerf containing detritus.	b. Same as class H.	No figure supplied.
c. A Kerf which extends into metallization and leaves less than 75 percent of the metallization width undisturbed (see figure 2032-60h). NOTE: Opening a metallization link by design is acceptable.	c. Same as class H.	 FIGURE 2032-60h
d. A Kerf or floating Kerf that leaves less than 50 percent of the original width of a resistor, unless by design (see figure 2032-61h). PRECAUTIONARY NOTE: The maximum allowable current density requirement shall not be exceeded. NOTE: A floating Kerf in a resistor that leaves less than 50 percent of the narrowest resistor width unless by design.	d. Same as class H.	 FIGURE 2032-61h
e. A trim that does not originate from the edge of the resistor.	e. Same as class H.	No figure supplied.

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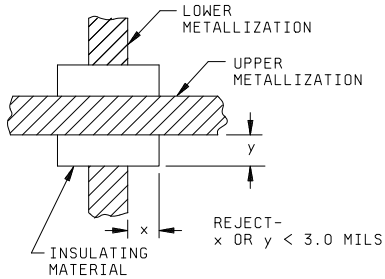
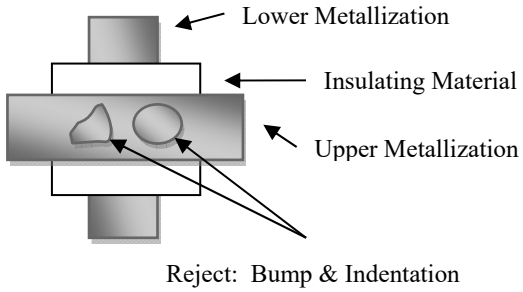
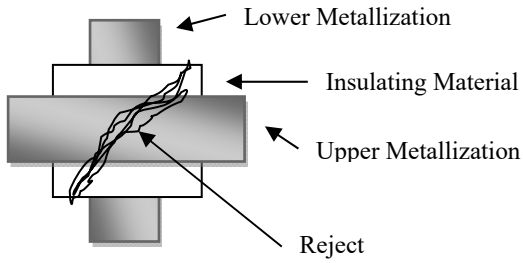
3.2.6. Multilevel thick film defects, "low magnification". No element shall be acceptable that exhibits:

Class H	Class K	Figures
a. Any insulating material that does not extend beyond the width of the upper and lower metallization by 3.0 mils minimum (see figure 2032-62h).	a. Same as class H.	 FIGURE 2032-62h
b. Voids in the insulating material that expose underlying metallization. NOTE: Voids caused by burn outs are not acceptable.	b. Same as class H.	No figure supplied.
c. Vias that are less than 50 percent of the original design area.	c. Same as class H.	No figure supplied.
d. A bump or indentation in the upper (overlaying) metallization at the intersection of the upper and lower metallization (see figure 2032-63h). NOTE: This criteria is not applicable to coupling (air) bridges. NOTE: There could be a problem with the insulating material.	d. Same as class H.	 FIGURE 2032-63h
e. Scratch that completely crosses the metallization and damages the insulating material surface on either side (see figure 2032-64h).	e. Same as class H.	 FIGURE 2032-64h

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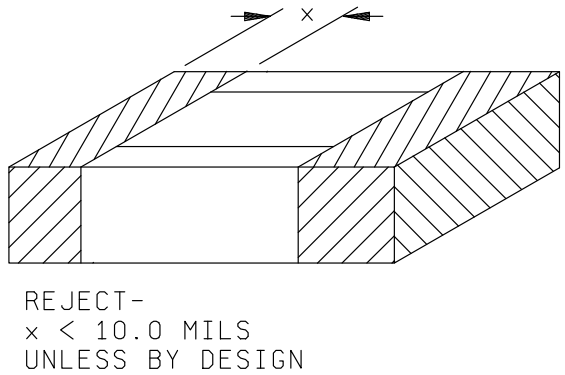
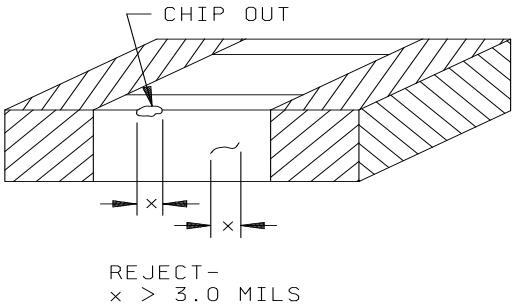
3.2.7. Additional criteria for thick film nonplanar resistor defects “low magnification”. The thick film resistor element planar inspection criteria, also applies to thick film nonplanar resistors. The "low magnification" inspection shall be within the range of 10X to 60X. No element shall be acceptable that exhibits:

Class H	Class K	Figures
a. Metallized termination width less than 10.0 mils unless by design (see figure 2032-65h).	a. Same as class H.	 FIGURE 2032-65h
b. A crack, chipout or void in the substrate greater than 3.0 mils in any direction (see figure 2032-66h).	b. Same as class H.	 FIGURE 2032-66h
c. Build-up of termination material on metallized termination areas greater than 3.0 mils high for weldable metallized terminations or 8.0 mils high for solderable metallized terminations (see figure 2032-67h). Note: Whiskers are not acceptable (See definitions, section 3i).	c. Same as class H.	 FIGURE 2032-67h

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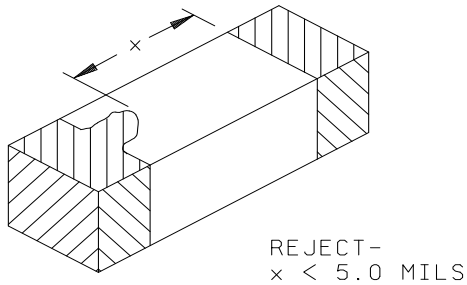
3.3. Capacitor inspection. Inspection for visual defects described in this section shall be conducted on each capacitor device. The "high magnification" inspection shall be within the range of 100X to 200X for both class H and class K. The "low magnification" inspection shall be within the range of 10X to 60X for both class H and class K.

3.3.1. Common nonplanar capacitor defects, "low magnification". No element shall be acceptable that exhibits:

Class H	Class K	Figures
a. Peeling or lifting of any metallization.	a. Same as class H.	No figure supplied.
b. Protrusion between metallization terminals that leaves less than 5.0 mils separation see figure 2032-68h).	b. Same as class H.	 FIGURE 2032-68h
c. Lifting, blistering, or peeling of insulation.	c. Same as class H.	No figure supplied.
d. Voids in metallized terminals that expose underlying material over greater than 25 percent of any side of the metallized terminal area.	d. Same as class H.	No figure supplied.
e. Marking shall be legible and complete.	e. Same as class H.	No figure supplied.
f. Lips, flared edges, or irregular shapes shall not exceed specified limits and tolerances.	f. Same as class H.	No figure supplied.
g. There shall be no fused dust or excess material on external surface that prevents a chip from lying flat, or protrude more that 0.003” or 0.08mm out of the surface.	g. Same as class H.	No figure supplied.
h. When compared to a flat surface, the clearance or warpage at the center of the chip shall be less than 5% of the length dimension.	h. Same as class H.	No figure supplied.

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3.3.2. Common foreign material capacitor defects, "low magnification". No element shall be acceptable that exhibits:

Class H	Class K	Figures
a. For mounted and unmounted elements, unattached foreign material on the surface of the element. NOTE: All foreign material shall be considered to be unattached unless otherwise verified to be attached. Verification of attachments of foreign material whose longest dimensions are greater than 75 percent of the closest unglassivated conductive spacing shall be accomplished by a light touch with an appropriate mechanical device (i.e., needle, probe, pick, etc.). Verification of attachments of smaller material can be satisfied by suitable cleaning process approved by the acquiring or qualifying activity. All foreign material or particles may be removed, if possible, with a nominal gas blow (approximately 20 psig). NOTE: Semiconductor particles are considered to be foreign material.	a. Same as class H.	No figure supplied.
b. Attached foreign material that bridges metallization paths, two package leads, lead to package metallization, functional circuit elements, junctions, or any combination thereof.	b. Same as class H.	No figure supplied.
c. Liquid droplets, ink drops, or any chemical stain that appear to bridge any unglassivated metallization or unpassivated active circuit areas.	c. Same as class H.	No figure supplied.
d. Attached foreign material that covers more than 25 percent of a bonding pad area.	d. Same as class H.	No figure supplied.

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3.3.3. Thick film capacitors and those overlay capacitors used in GaAs microwave devices, "low magnification". No element shall be acceptable that exhibits:

Class H	Class K	Figures
a. Scratches that expose an underlying material.	a. Same as class H.	No figure supplied.
b. Any peeling or lifting of the metallization.	b. Same as class H.	No figure supplied.
c. Excess top metal which extend beyond the capacitor bottom metal.	c. Same as class H.	No figure supplied.
d. Voids in the capacitor bottom metal which extend under the capacitor top metal.	d. Same as class H.	No figure supplied.
e. Voids in the top metallization which leaves less than 75% of the metallization area undisturbed.	e. Same as class H.	No figure supplied.

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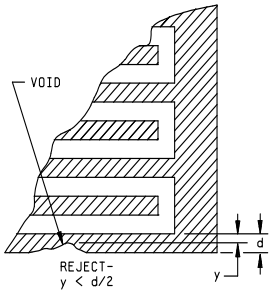
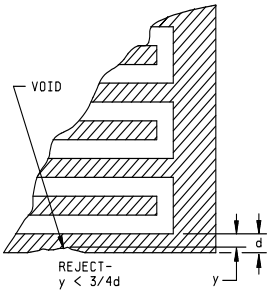
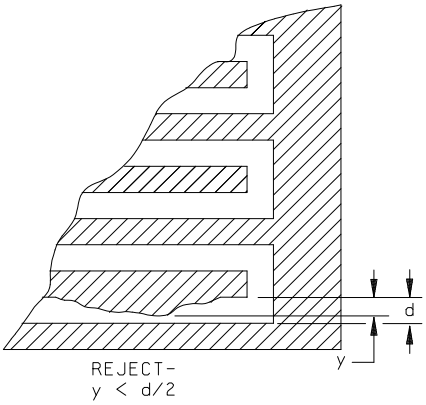
3.3.4. Thin film capacitors devices (this includes silicon dioxide and silicon nitride capacitors), "low magnification". No element shall be acceptable that exhibits:

Class H	Class K	Figures
a. A scratch in the metallization, other than in the bonding pad area, that exposes the dielectric material.	a. Same as class H.	No figure supplied.
b. A void(s) in metallization, other than in the bonding pad area, that reduces the metallization to an extent greater than an area equivalent to 25 percent of the capacitor metallization.	b. Same as class H.	No figure supplied.
c. For interdigitated capacitors only, void(s) in the metallization that leaves less than 50 percent of the original metallization width undisturbed (see figure 2032-69h).	c. Less than 75 percent (see figure 2032-69k).	 FIGURE 2032-69h  FIGURE 2032-69k
d. For interdigitated capacitors, a protrusion of metallization that reduces the original separation by greater than 50 percent (see figure 2032-70h).	d. Same as class H.	 FIGURE 2032-70h
e. A bump or indentation in the overlaying metallization.	e. Same as class H.	No figure supplied.
f. Scratch that completely crosses metallization and disturbs the surface on either side.	f. Same as class H.	No figure supplied.

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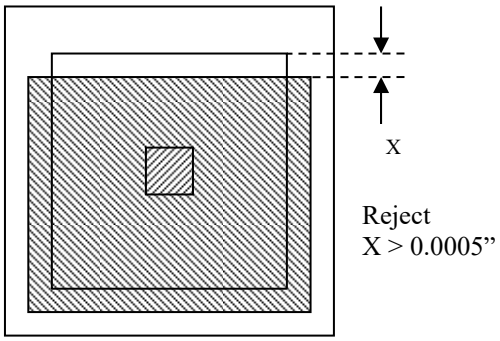
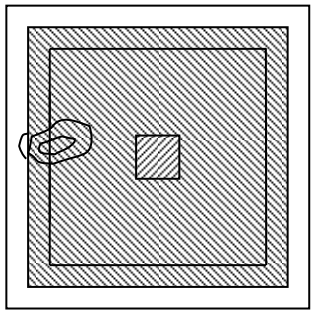
3.3.4. Thin film capacitors devices (this includes silicon dioxide and silicon nitride capacitors), "low magnification" - Continued.

Class H	Class K	Figures
g. Scratch or probe marks in the bond pad area that exposes underlying material over more than 25% of the bond pad.	g. Same as class H.	No figure supplied.
h. Void(s) in the bond pad area that expose underlying material over more than 25% of the bond pad.	h. Same as class H.	No figure supplied.
i. Metallization corrosion.	i. Same as Class H. Note: Metallization having localized discolored areas should be closely examined.	No figure supplied.
j. Dielectric exposure on either side of the contact window greater than 0.0005" due to metallization misalignment (2032-71h).	j. Same as class H.	 FIGURE 2032-71h
k. Protrusion of metallization that reduces the original separation between operating metallizations by greater than 50%.	k. Same as class H.	No figure supplied.
l. Either multiple lines (color fringing) or a complete absence of passivation visible at the edge and containing under the metallization (2032-72h)	l. Same as class H.	 FIGURE 2032-72h

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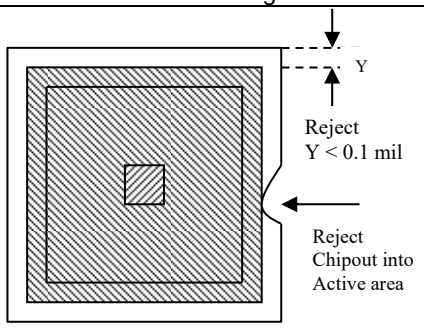
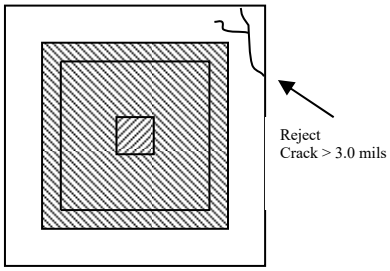
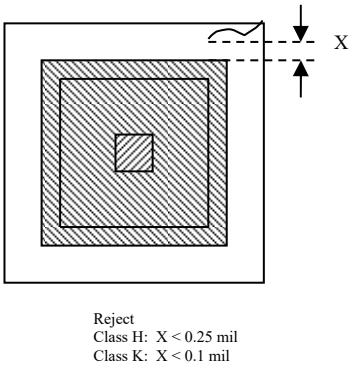
3.3.4. Thin film capacitors devices (this includes silicon dioxide and silicon nitride capacitors), "low magnification" - Continued.

Class H	Class K	Figures
m. Less than 0.1 mil of passivation visible between the operating metallization and the edge of the substrate (2032-73h).	m. Same as class H.	 FIGURE 2032-73h
n. A chipout that extends into the active circuit area.	n. Same as class H.	See figure 2032-73h.
o. A crack that exceeds 3.0 mils in length (2032-74h).	o. Same as class H.	 FIGURE 2032-74h
p. A crack that does not exhibit 0.25 mil of separation from an active circuit area or operating metallization (2032-75h).	p. Exhibits 0.1 mil (2032-75k).	 FIGURE 2032-75h & 2032-75k

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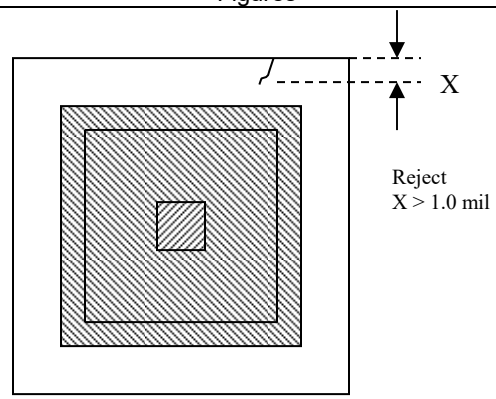
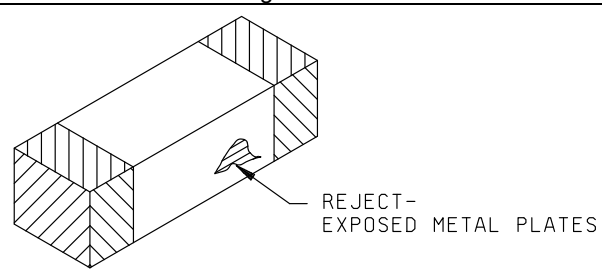
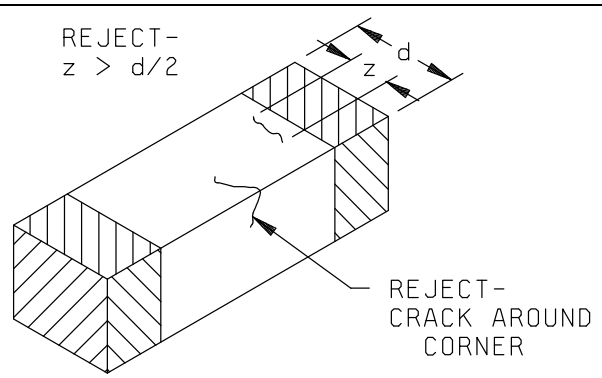
3.3.4. Thin film capacitors devices (this includes silicon dioxide and silicon nitride capacitors), "low magnification" - Continued.

Class H	Class K	Figures
q. A crack greater than 1.0 mil in length extending from the edge directly towards the active circuit area (2032-76h).	q. Same as class H.	 FIGURE 2032-76h
r. A crack that does not originate at an edge.	r. Same as class H.	No figure supplied.

3.3.5. Ceramic chip capacitor defects, “low magnification”. No element shall be acceptable that exhibits:

Class H	Class K	Figures
a. Crack, chip or void in the body that exposes metal plates, (see figure 2032-77h).	b. Crack, chip or void in the body.	 FIGURE 2032-77h
b. Crack that is greater than 50 percent of the width of the unmetallized sides, top, or bottom, or that extends around a corner (see figure 2032-78h). Note: Striations are unacceptable.	b. Crack. NOTE: No cracks are allowed.	 FIGURE 2032-78h.

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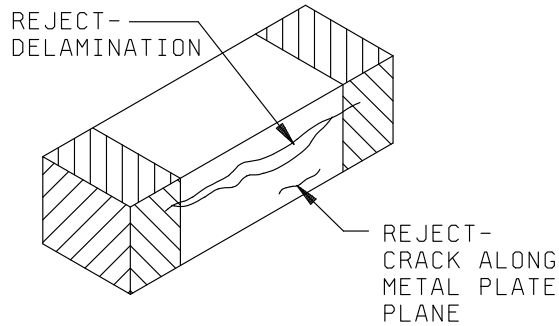
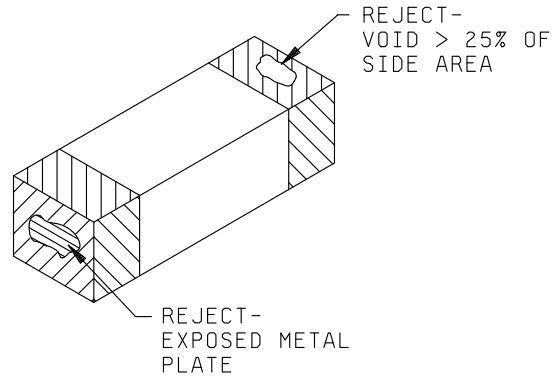
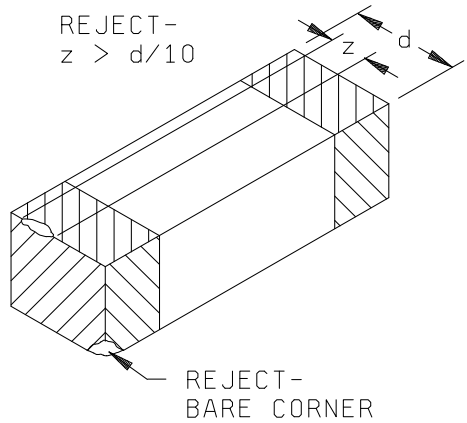
3.3.5. Ceramic chip capacitor defects, “low magnification” - Continued.

Class H	Class K	Figures
c. Evidence of separation (delamination) of metal plates or cracks along the plane of the metal plates (see figure 2032-79h). Note: Narrow grooves or channel less than 1.0 mil wide that exhibit a glass-like appearance and do not expose metal plates are acceptable.	c. Delamination. NOTE: No delamination is allowed.	 FIGURE 2032-79h. Class H delamination criteria.
d. Crack or void in the metallization that exposes metal plates, or voids that are greater than 25 percent of the area of the metallized terminal (see figure 2032-80h).	d. Same as class H.	 FIGURE 2032-80h. Class H termination defect criteria.
e. Void in the metallized edges of the element that are greater than 10 percent of the metallized edge dimension, or bare corners of metallized terminals (see figure 2032-81h). NOTE: This criterion is applicable to solder attached elements only.	e. Same as class H.	 FIGURE 2032-81h. Class H metallized edge defect criteria.
f. Attached foreign material on the body that covers an area greater than 5.0 mils square on any side.	f. Same as class H.	No figure supplied.

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3.3.6. Tantalum chip capacitor defects, “low magnification”. No element shall be acceptable that exhibits:

Class H	Class K	Figures
a. Flaking or peeling of the encapsulant that exposes any underlying material.	a. Same as class H.	No figure supplied.
b. A metallized terminal that is less than 90 percent free of encapsulant material.	b. Same as class H.	No figure supplied.
c. Less than 50 percent continuous metallized terminal weld area without cracks. For capacitors with riser wires, a riser wire connection with less than 25 percent continuous weld area.	c. Same as class H.	No figure supplied.
d. Metallized terminal containing residue from the welding operation that is not firmly attached metallurgically to the anode cap.	d. Same as class H.	No figure supplied.
e. Metallized terminal not aligned as shown in the applicable drawing.	e. Same as class H.	No figure supplied.
f. Encapsulant preventing the metallized terminal from resting on the substrate bonding pads when the capacitor is in the bonding position except where the metallized terminal electrical contact is made by alternate means.	f. Same as class H.	No figure supplied.
g. Lifting, blistering or peeling of metallized terminal encapsulant.	g. Same as class H.	No figure supplied.

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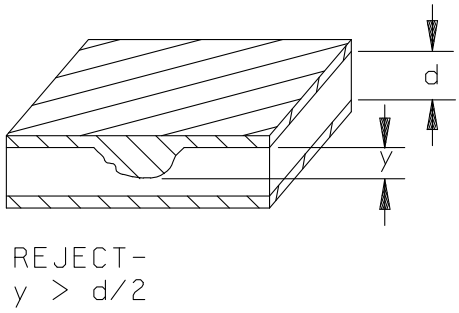
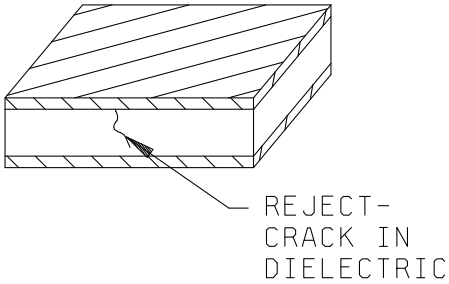
3.3.7. Parallel plate chip capacitor defects, “low magnification”. No element shall be acceptable that exhibits:

Class H	Class K	Figures
a. Metallization that extends greater than 50 percent around the edge of the capacitor (see figure 2032-82h).	a. Same as class H.	 FIGURE 2032-82h. Class H metallization extension criterion.
b. Evidence of cracks in the dielectric body (see figure 2032-83h).	a. Same as class H.	 FIGURE 2032-83h. Class H crack in dielectric criterion.

3.4. Inductor and Transformer Inspection. Inspection for visual defects described in this section shall be conducted on each inductor and transformer device. The "high magnification" inspection shall be within the range of 100X to 200X for both class H and class K. The "low magnification" inspection shall be within the range of 10X to 60X for both class H and class K.

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3.4.1. Common foreign material inductor and transformer defects, "low magnification". No element shall be acceptable that exhibits:

Class H	Class K	Figures
a. For mounted and unmounted elements, unattached foreign material on the surface of the element. NOTE: All foreign material shall be considered to be unattached unless otherwise verified to be attached. Verification of attachments of foreign material whose longest dimensions are greater than 75 percent of the closest unglassivated conductive spacing shall be accomplished by a light touch with an appropriate mechanical device (i.e., needle, probe, pick, etc.). Verification of attachments of smaller material can be satisfied by suitable cleaning process approved by the acquiring or qualifying activity. All foreign material or particles may be removed, if possible, with a nominal gas blow (approximately 20 psig). NOTE: Semiconductor particles are considered to be foreign material.	a. Same as class H.	No figure supplied.
b. Attached foreign material that bridges metallization paths, two package leads, lead to package metallization, functional circuit elements, junctions, or any combination thereof.	b. Same as class H.	No figure supplied.
c. Liquid droplets, ink drops, or any chemical stain that appear to bridge any unglassivated metallization or unpassivated active circuit areas.	c. Same as class H.	No figure supplied.
d. Attached foreign material that covers more than 25 percent of a bonding pad or attachment area.	d. Same as class H.	No figure supplied.

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3.4.2. Inductor and transformer defects, "low magnification". No element shall be acceptable that exhibits:

Class H	Class K	Figures
a. Peeling, lifting, flaking, chipping, cracking, crazing, or blistering of winding metallization, insulation, or protective coating.	a. Same as class H.	No figure supplied.
b. Evidence of shorts between adjacent turns or windings. This includes evidence of arcing or flashover.	b. Same as class H.	No figure supplied.
c. Cracks or exposure of bare magnetic core material. Exposed bare magnetic core material is acceptable if by design.	c. Same as class H.	No figure supplied.
d. Pits or voids in the core insulation greater than 5.0 mils area that expose the magnetic core material.	d. Same as class H.	No figure supplied.
e. Separation less than 5.0 mils between wire termination points of the same or adjacent windings.	e. Same as class H.	No figure supplied.
f. Missing polarity identification unless by design.	f. Same as class H.	No figure supplied.
g. Operating metallization and multilevel thick film defects as described in 3.2.1 and 3.2.5 herein.	g. Same as class H.	No figure supplied.
h. Leakage of filling material.	h. Same as class H	No figure supplied.
i. Evidence of physical damage such as cracks, bursting, or bulging of the case.	i. Same as class H	No figure supplied.
j. Corrosion which could affect the mechanical or electrical operation.	j. Same as class H	No figure supplied.

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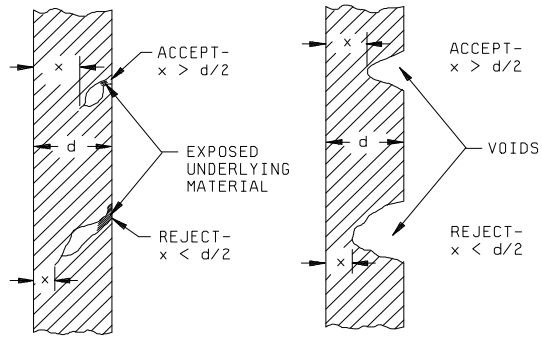
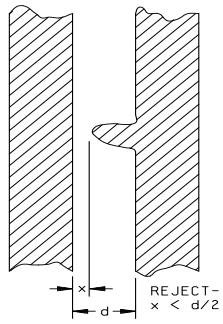
3.5. Surface acoustic wave (SAW) element inspection. Inspection for visual defects described in this section shall be conducted on each SAW element. When inspection is performed prior to mounting, then SAW elements may be inspected using backlighting. All inspection shall be performed at "low magnification" within the range of 10X to 60X for both class H and class K.

3.5.1. Operating metallization defects "low magnification". No element shall be acceptable that exhibits:

3.5.1.1. Metallization voids and scratches. No element shall be acceptable that exhibits:

Class H	Class K	Figures
a. A scratch or void in the metallization, that both exposes under-lying material anywhere along its length and leaves less than 50 percent of the original metallization width undisturbed (see figure 2032-84h). NOTE: Underlying material does not have to be exposed along the full length of the scratch.	a. Same as Class H.	 FIGURE 2032-84h

3.5.1.2. Metallization bridging and protrusions. No element shall be acceptable that exhibits:

Class H	Class K	Figures
a. Metallization protrusions or bridging that reduces the original separation between adjacent operating metallization by greater than 50 percent (see figure 2032-85h).	a. Same as class H.	 FIGURE 2032-85h

3.5.1.3. Metallization corrosion. No element shall be acceptable that exhibits:

Class H	Class K	Figures
a. Any metallization corrosion.	a. Same as class H.	No figure supplied.

3.5.1.4. Metallization adherence. No element shall be acceptable that exhibits:

Class H	Class K	Figures
a. Any metallization lifting, peeling or blistering.	a. Same as class H.	No figure supplied.

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3.5.2. Substrate material defects "low magnification". No element shall be acceptable that exhibits:

Class H	Class K	Figures
a. Any crack that exceeds 3.0 mils in length.	a. Same as class H.	No figure supplied.
b. Any crack that is within 0.1 mil of any active circuit area or operating metallization.	b. Same as class H.	No figure supplied.
c. Any crack exceeding 1.0 mil in length extending from the element edge directly toward the active circuit area or operating metallization.	c. Same as class H.	No figure supplied.
d. Any chipout touching the active area.	d. Same as class H.	No figure supplied.

3.5.3. Foreign material defects "low magnification". No element shall be acceptable that exhibits:

Class H	Class K	Figures
a. For mounted and unmounted elements, unattached foreign material on the surface of the element. NOTE: All foreign material shall be considered to be unattached unless otherwise verified to be attached. Verification of attachments of foreign material whose longest dimensions are greater than 75 percent of the closest unglassivated conductive spacing shall be accomplished by a light touch with an appropriate mechanical device (i.e., needle, probe, pick, etc.). Verification of attachments of smaller material can be satisfied by suitable cleaning process approved by the acquiring or qualifying activity. All foreign material or particles may be removed, if possible, with a nominal gas blow (approximately 20 psig).	a. Same as class H.	No figure supplied.
b. Liquid droplets, ink drops, or chemical stains that appear to bridge unglassivated metallization or unpassivated active circuit areas.	b. Same as class H.	No figure supplied.

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3.5.3. Foreign material defects "low magnification" - Continued.

Class H	Class K	Figures
c. Attached foreign material that covers greater than 25 percent of a bonding pad area.	c. Same as class H.	No figure supplied.
d. Attached foreign material that bridges metallization paths, two package leads, lead to package metallization, functional circuit elements, junctions, or any combination thereof.	d. Same as class H.	No figure supplied.

4. SUMMARY. The following details shall be specified in the applicable acquisition document:

a. Class H or class K visual requirements.

b. Where applicable, any conflicts with element design, topology or construction (see 3).

c. Where applicable, gauges, drawings and photographs that are to be used as standards for operator comparison (see 2).

d. Where applicable, magnifications other than those specified (see 3).

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METHOD 2035

ULTRASONIC INSPECTION OF TAB BONDS

1. PURPOSE. The purpose of this method is to detect unbonded and insufficiently bonded sites in TAB (Tape automated bonding) devices in the open package condition, through the measurement of bond area by means of Scanning Laser Acoustic Microscope (SLAM) techniques. It establishes methods and criteria for ultrasonic inspection of these TAB semiconductor devices.

NOTES:

1. For various metallurgical constitutions, absolute strengths expressed as pull strengths per unit area of bond differ. A scalar equivalency must be established for each alloy and process, to relate bond area to anticipated bond strength.

2. The term TAB bond in this document refers to one of the multiplicity of bonds, inner lead (ILB) or outer lead (OLB) formed by a tape automated bonding (TAB) process. In the case of ILB, it refers to that area of the device defined by the intersection of the beam lead, the semiconductor bonding pad area, and the contact outline of the thermode or fixture performing the bond, in the horizontal plane, and refers to all interfaces within that area between the semiconductor die surface and the beam lead. In the case of OLB, it refers to that area of the device defined by the intersection of the beam lead, the substrate bonding pad area, and contact outline of thermode or fixture performing the bond, in the horizontal plane, and refers to all interfaces within that area between the substrate surface and the beam lead.

3. The terms ultrasonic inspection and SLAM as used in this document refer to the process and instrument performing high frequency ultrasonic inspection and produce grey-scale images of the internal features of devices by means of scanning laser acoustic microscopy, and by which bond area measurement may be performed.

2. APPARATUS. The apparatus and materials for this evaluation shall include:

a. Ultrasonic imaging equipment of the scanning laser acoustic microscope type, of frequency and resolution sufficient to penetrate the bond area and render an image which discloses the size and shape of the bond area with a linear dimensional allowance no greater than 20 percent of a bond dimension. Frequency is dictated by consideration of the wavelength of sound in the materials and the limit of resolution. Whereas lower frequencies have been used for inspection of larger scale device types, the present size of TAB sites requires frequencies of from one hundred to several hundred megahertz.

b. A visual output/storage device. A method of producing, displaying, and storing a scale image of adequate grey-scale range (minimum of 64 levels) shall be used. Such device may include a grey-scale printer/plotter, or preferably CRT display with an image digitizer capable of rendering images in digital code for bulk media storage and retrieval, and algorithmic processing and evaluation. The images so stored shall be suitable for manual, or preferably, automated analysis. The output devices shall be capable of producing and storing the images to a spatial and grey-scale resolution at least equal to the resolution of their acquisition by the ultrasonic imaging equipment. The output/storage device must be capable of presenting, storing, and retrieving image label information.

3. PROCEDURE. The equipment used shall be adjusted as necessary to obtain satisfactory images of good contrast to achieve maximum image detail within the sensitivity requirements of the bond type being examined. The appropriate operator methodology will be used to insure adequate positioning and insonification (irradiation by ultrasound) of the device for purposes of producing its image. Additional protocols will be followed as required. The normal intrinsic strength of the bond metallurgy shall be known and established, and the metallurgy of the devices to be tested should be qualified as in agreement with that strength.

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3.1 Calibration of the instrument. When specified, at least one device of the type and construction to be tested shall be available to set up the ultrasonic inspection equipment and peripherals. The device may be a scape non-operational device with TAB bonded leads which will be used to identify device landmarks and ensure the equipment is properly functional.

3.2 Labeling and identifying. The devices tested and the image records made of them shall be labeled in a standard format to include the following information:

a. Device manufacturer's name or code identification number.

b. Device type or part number.

c. Production lot number and/or inspection date code lot number.

d. Ultrasonic image view number and date; to include description or code for the region or bond number (s) viewed.

e. Device serial/cross reference number if applicable.

f. Ultrasonic operator identification.

3.3 Serialized devices. When device serialization is required, each device shall be readily identifiable by a serial number, and this serial number must be included in a form readable in the stored image. In the event of a skipped piece in the serialization, a blank space representing the skipped piece, and labeled with its serial number should appear in the storage medium. In the event of a large contiguous range of skipped pieces, a similar blank space advising of the range of pieces skipped should appear in the storage medium in place of the large physical space of the many skips.

3.4 Data back-up. When required, data back-up shall be specified from a choice of multiple floppy disk, multiple track data tape, or a video format tape, or other options having sufficient volume, resolution, speed, and reliability to suit the requirements for storage and labeling.

3.5 Mounting. The devices shall be mounted for ultrasonic inspection in a fixture which insures correct positioning in all dimensions, and adequately safeguards the potentially fragile bonds from mechanical contact with any substance other than the coupling fluid. Positioning thereafter must continue in a fashion which continues the above condition, and furthermore exposes each inspected bond area to the correct acoustic environment and portion of the instrumental field.

3.6 Angle of insonification. The angle of insonification must be specified by prior analysis, and if the mounting fixture is goniometrically agile it must be set to the correct angle by adjustment or selection.

3.7 Conditions of operation. Adjustments, selections, options, and settings used in the performance of the ultrasonic inspection must be recorded if they are of a nature critical to the proper operation of equipment; not to be recorded are those casual adjustments which are done as an obvious matter of course, and the performance of which are guided by such rules as trimming for maximum, minimum, or optimum, and which are not controlled by calibrated interfaces.

3.8 Operating personnel. Operating personnel shall have a basic familiarity of the nature of sound and the use of ultrasonic instruments in the inspection of devices. They shall be specifically trained and certified in the operation of the ultrasound and peripheral equipment used so that defects revealed by the method can be validly interpreted and compared with applicable standards.

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3.9 Reports of inspection. For class S devices, or when specified for other device classes, the manufacturer shall furnish
inspection reports with each shipment of devices. The report shall describe the results from the ultrasonic inspection, and list the purchase order number, or equivalent identification, the part number, the date code, the quantity inspected, the quantity rejected, and the date of the test. For each rejected device, the part number, the serial number when applicable, and the cause for rejection shall be listed.

3.10 Acoustic micrograph and report retention. When specified, the manufacturer shall retain a set of the ultrasonic images and a copy of the inspection report, for the period specified.

3.11 Examination and acceptance criteria. Once the manufacturer has established the total bond area to be sought, based upon studies of the device to be bonded, and the inclusion of a prudent excess margin, then the following shall be considered the minimum bond area percentage:

a. In the case of solder bonds of lead-tin alloys a bond area percentage of 75 percent of the total bond area shall be considered minimum.

b. In the case of gold-tin eutectic and gold-gold thermocompression, a bond area percentage of 50 percent of the total bond area shall be considered minimum, except in the case of lead misalignment; when lead misalignment is a contributing factor a bond area percentage of 75 percent shall be considered minimum.

In the examination of devices, the following aspects shall be considered unacceptable bonding, and devices which exhibit any of the following defects shall be rejected:

a. A bond having a total bond area less than the minimum bond area. The failure may be caused by any reason, including lateral or longitudinal misalignment.

b. A bond meeting the minimum bond area, but with this area being discontinuous so that no single bonded area meets or exceeds the minimum bond area.

4. SUMMARY. The following details shall be specified in the applicable acquisition document:

a. Number of views to be taken by SLAM inspection of each piece or bonding site, in accordance with 3.10, if other than one view.

b. Markings of devices, or labeling of images, if other than in accordance with 3.2, or special markings of devices to indicate that they have been ultrasonically imaged, if required.

c. Defects to be sought in the devices, and criteria for acceptance or rejection, if other than in 3.11.

d. Image and report retention when applicable (see 3.10).

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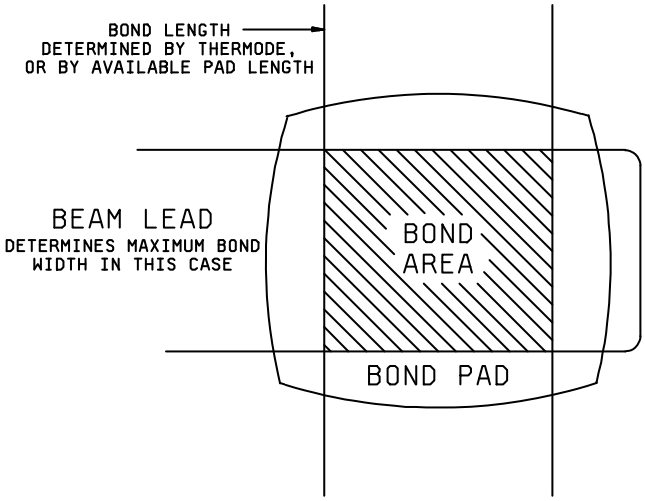

FIGURE 2035-1. Bond area.

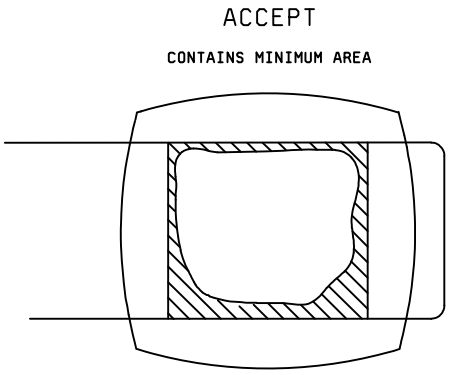

FIGURE 2035-2. Acceptable bond area.

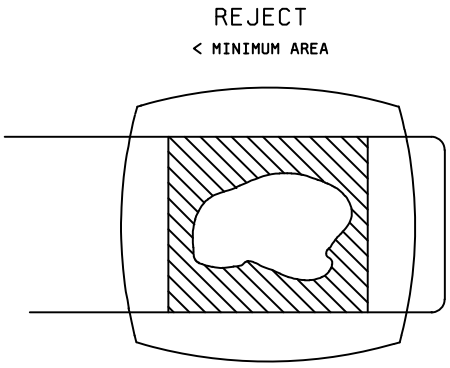

FIGURE 2035-3. Rejectable bond area.

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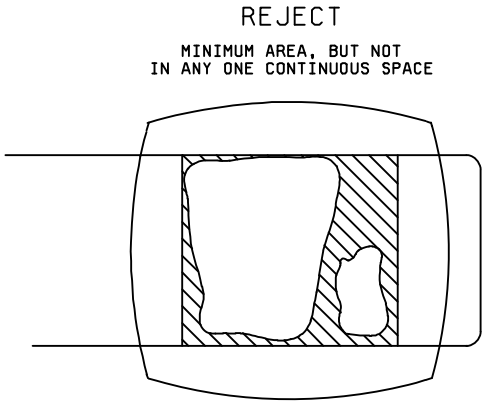

FIGURE 2035-4. Rejectable discontinuous bond area.

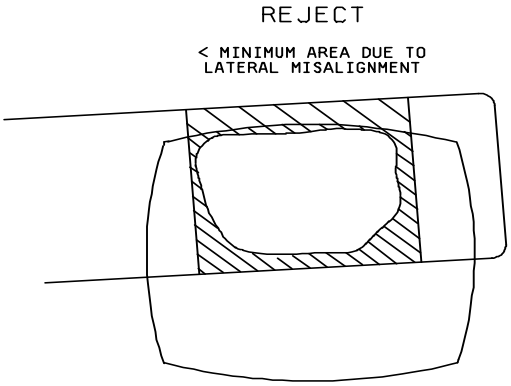

FIGURE 2035-5. Lateral misaligned bond area.

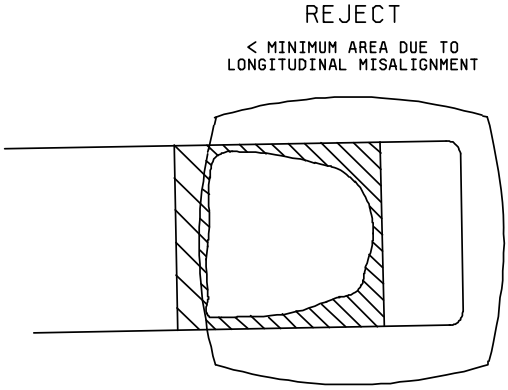

FIGURE 2035-6. Longitudinal misaligned bond area.

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METHOD 2036.1

RESISTANCE TO SOLDERING HEAT

1. PURPOSE. This test method is performed to determine whether termination leads and other component parts can withstand the effects of the heat to which they will be subjected during the soldering process (solder iron, solder dip, solder wave, or solder reflow). The heat can be either conducted heat through the termination into the component part, or radiant heat from the solder bath when in close proximity to the body of the component part, or both. The solder dip method is used as a reasonably close simulation of the conditions encountered in wave soldering, in regard to radiated and conducted heat. This test also is intended to evaluate the impact of reflow techniques to which components may be exposed. The heat of soldering can cause solder reflow which may affect the electrical characteristics of the component part and may cause mechanical damage to the materials making up the part, such as loosening of terminations or windings, softening of insulation, opening of solder seals, and weakening of mechanical joints.

2. APPARATUS.

2.1 Solder pot. A static solder pot, of sufficient size to accommodate the mounting board and the immersion of its terminations to the depth specified for the solder dip (without touching the bottom of the pot), shall be used. This apparatus shall be capable of maintaining the solder at the temperature specified. The solder bath temperature shall be measured in the center of the pot at a depth of at least 0.500 inch (12.7 mm), but no deeper than 1 inch (25.4 mm) below the surface of the solder.

2.2 Heat sinks or shielding. The use of heat sinks or shielding is prohibited except when it is a part of the component. When applicable, heat sinks or shielding shall be specified in the individual specification, including all of the details, such as materials, dimensions, method of attachment, and location of the necessary protection.

2.3 Fixtures. Fixtures, when required, shall be made of a non-solderable material designed so that they will make minimum contact (i.e., minimum heat sink) with the component. Further, they shall not place undue stress on the component when fixtured.

2.4 Mounting board. A mounting board, in accordance with NEMA grade FR-4 of IPC-4101 (e.g. glass epoxy material, IPC-4101/21, IPC-4101/26, IPC-4101/82, IPC-4101/83, IPC-4101/92, IPC-4101/93, IPC-4101-95, IPC-4101/97 and IPC4101/98), 9 square inches (e.g. 3 x 3, 1 x 9, etc.), minimum area, 0.062 inch ±0.0075 inch (1.57 mm ±0.191 mm) thick, shall be used, unless otherwise specified. Component lead holes shall be drilled such that the diametrical clearance between the hole and component terminals shall not exceed 0.015 inch (0.38 mm). Metal eyelets or feed-throughs shall not be used. Surface mount boards, when specified in the individual specification, shall have pads of sufficient size and number to accommodate the component being tested.

2.5 Solder iron. A solder iron, capable of maintaining a temperature of 350 °C ±10 °C, under thermal load, shall be used.

2.6 Reflow chambers. The reflow chambers or equivalent (Vapor Phase Reflow (VPR) chamber, Infrared Reflow (IRR) oven, air circulating oven, etc.) shall be of sufficient size to accommodate the mounting board and components to be tested. The chamber shall be capable of generating the specified heating rate, temperatures and environments.

2.7 Temperature measurement. Low mass thermocouples that do not affect the heating rate of the sample shall be used. A temperature recording device is recommended. The equipment shall be capable of maintaining an accuracy of ±1 °C at the temperature range of interest.

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3. MATERIALS.

3.1 Solder. The solder or solder paste shall be tin-lead alloy with a nominal tin content of 50 percent to 70 percent in accordance with IPC J-STD-006, “Requirements for Electronic Grade Solder Alloys and Fluxed and Non-Fluxed Solid Solders for Electronic Soldering Applications” or IPC J-STD-005, “Requirements for Soldering Pastes”. When specified in the individual specification, other solders can be used provided they are molten at the specified temperature.

3.2 Flux. When flux is used, it shall conform to type A of IPC J-STD-004, “Requirements for Soldering Fluxes”, or as specified in the individual specification.

3.3 VPR fluid. A perfluorocarbon fluid that has a boiling point of 215 °C shall be used.

4. PROCEDURE. The procedures described below in paragraph 4.4.1 through 4.4.6 are the default tests procedures. At the manufacturer’s option, other test setups/procedures may be used provided it can be shown that they provide an equivalent stress. In the absence of equivalent procedures, the specified procedures shall be followed.

4.1 Special preparation of specimens. Any special preparation of specimens prior to testing shall be as specified in the individual specification. This could include specific instructions such as bending or any other relocation of terminations, cleaning, application of flux, pre-tinning, or attachment of heat sinks or protective shielding, prior to test.

4.2 Preparation of solder bath. The molten solder shall be agitated to assure that the temperature is uniform. The surface of the solder shall be kept clean and bright.

4.3 Application of flux. When flux is used, the terminations to be tested shall be immersed in the flux, which is at room ambient temperature, to the depth specified for the solder dip. The duration of the immersion shall be from 5 seconds (s) to 10 seconds.

4.4 Test conditions. Unless otherwise specified in the individual specification, the test shall be performed on all solder terminations attached to the component part (see FIGURE 2036-1 for examples). There are six types of soldering techniques covered by these test conditions. The test conditions are outlined below and in TABLE 2036-I.

Test condition A: Solder iron - Hand soldering of solder cups, through hole components, tab and post terminations, and solder eyelet terminations.

Test condition B: Solder dip - Simulates hot solder dipping (tinning) of leaded components.

Test condition C: Wave solder - Simulates wave solder of topside board mount product.

Test condition D: Wave solder - Simulates wave solder of bottom-side board mount product.

Test condition H: VPR – VPR environment without preheat.

Test conditions I, J, K: Infrared/Convection reflow - Simulates IRR, natural convection, and forced air convection reflow environments (see TABLE 2036-1 for temperature requirements).

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4.4.1 Test condition A: Solder iron.

a. When testing a solder cup, tab and post termination, or solder eyelet termination, the applicable wire size, properly prepared for the solder termination, shall be attached in the appropriate manner.

b. When testing a board mount component, the component shall be placed on a mounting board (See 2.4).

c. When specified, the components shall be fluxed (See 4.3).

d. Unless otherwise specified, a solder iron in accordance with 2.5 shall be used.

e. The solder iron shall be heated to 350 °C ±10 °C and applied to the termination for a duration of 4 seconds to 5 seconds as specified in TABLE 2036-I. The solder and iron shall be applied to the area of the assembly closest to the component body that the product is likely to experience. For surface mount components, the iron shall be placed on the pad only.

f. Remove the iron and allow the component to cool and stabilize at room ambient conditions. If flux was used, the component shall be cleaned using an appropriate cleaning solution.

4.4.2 Test condition B: Solder dip.

a. Place the component in an appropriate fixture (See 2.3).

b. When specified, the leads shall be fluxed (See 4.3).

c. Remove the dross from the solder pot surface.

d. Unless otherwise specified, terminations shall be immersed to within 0.050 inch (1.27 mm) of the component body in accordance with TABLE 2036-1. Terminations shall be immersed simultaneously, if the geometry of the component permits.

e. After the solder dip, the component shall be allowed to cool and stabilize at room ambient conditions. If flux was used, the component shall be cleaned using an appropriate cleaning solution.

4.4.3 Test condition C: Wave solder - topside board mount component.

a. The component under test shall be mounted on a mounting board or fixture (See 2.3 or 2.4). Through-hole mounted components shall have their terminals inserted into the termination holes. Surface mount components shall be placed on top of the board (see FIGURE 2036-1 for mounting examples).

b. When specified, the leads shall be fluxed (See 4.3).

c. Remove the dross from the solder pot surface.

d The components, mounted on the board, shall be preheated and immersed in the solder pot so that the bottom of the board floats on the molten solder in accordance with TABLE 2036-1.

e. The test specimen is not to be held against the surface of the molten solder.

f. After the float, the components shall be allowed to cool and stabilize at room ambient conditions. If flux was used, the components shall be cleaned using an appropriate cleaning solution.

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4.4.4 Test condition D: Wave solder – bottom side board mount product.

a. Place the component in an appropriate fixture (See 2.3).

b. When specified, the terminations shall be fluxed (See 4.3).

c. The component shall be preheated and fully immersed in the solder bath in accordance with TABLE 2036-I.

d. After the immersion, the component shall be allowed to cool and stabilize at room ambient conditions. If flux was used, the component shall be cleaned using an appropriate cleaning solution.

4.4.5 Test condition H: Vapor phase reflow soldering.

a. Components shall be mounted on a mounting board or fixture (See 2.3 or 2.4). Through-hole mounted components shall have their terminals inserted into the termination holes. Surface mount components shall be placed on top of the board.

b. A test chamber shall be used which is large enough to suspend the mounting board or fixture without touching the sides or solution (See 2.6). The VPR fluid shall be placed in the test chamber and shall be heated until it is boiling. The solution shall be allowed to boil for 5 minutes prior to suspending the mounting board or fixture.

c. The specific combination of temperature, duration of exposure, and number of heats shall be as specified in TABLE 2036-I.

d. After chamber equalization, the mounting board or fixture shall be suspended into the vapor in a horizontal plane. The mounting board or fixture shall not touch the solution.

e. After the heat, the component shall be allowed to cool and stabilize at room ambient conditions. If a solder paste was used, the component shall be cleaned using an appropriate solution.

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4.4.6 Test conditions I, J, K: Infrared / convection reflow soldering.

a. Components shall be mounted on a mounting board or fixture (See 2.3 or 2.4). Through-hole mounted components shall have their terminals inserted into the termination holes. Surface mount components shall be placed on top of the board.

b. A test chamber as specified in 2.6 shall be used.

c. A low mass thermocouple shall be attached tightly to the component at an appropriate position away from the edges.

d. The mounting board or fixture shall be placed into the test chamber and the temperature of the component ramped at a rate of 1 °C/s to 4 °C/s, as measured by the thermocouple. The mounting board or fixture shall be above 183 °C for 90 seconds to 120 seconds and held at the final temperature and time designated by the test condition. The mounting board or fixture shall then be allowed to cool to room ambient temperature. This constitutes one heat cycle in accordance with TABLE 2036-1.

5. EXAMINATIONS AND MEASUREMENTS. Examinations and measurements are to be made before and after the test, as specified in the individual specification.

6. SUMMARY. The following details are to be specified in the individual specification:

a. The use of heat sinks or shielding is prohibited except when they are part of the component (see 2.2).

b. Mounting board, if different from that specified (see 2.4).

c. Solder, if different from that specified (see 3.1).

d. Flux, if applicable and if different from that specified (see 3.2, 4.1, and 4.3).

e. Solder terminations that are not to be tested, if applicable (see 4.4).

f. Special preparation of specimens if applicable (see 4.1).

g. Depth of immersion in the molten solder, if different from that specified (see 4.4.2).

h. Test condition letter (see 4.4).

i. Cooling time prior to final examinations and measurements (see 4.4 and 5).

j. Examinations and measurements before and after test, as applicable (see 5).

k. Method of internal inspection, if required (see 5).

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TABLE 2036-1: Test conditions.

Test Condition	Solder Technique simulation	Temperature (°C)	Time (s) (at temp.)	Temperature ramp / immersion and / emersion rate	Number of heat cycles
A	Solder iron	350 ± 10 (solder iron temp)	4 - 5		1
B	Dip	260 ± 5 (solder temp)	10 ± 1	25 ± 6 mm/s	1
C	Wave: Topside	260 ± 5 (solder temp)	10 ± 1	Preheat 1 °C/s-4 °C/s to within 100 °C of solder temp. 25 mm/s ± 6 mm/s	1
D	Wave: Bottom-side	260 ± 5 (solder temp)	10 ± 1	Preheat 1 °C/s-4 °C/s to within 100 °C of solder temp. 25 mm/s ± 6 mm/s	1
H	Vapor phase reflow	215 ± 5 (vapor temp)	60 ± 5		1
I	IR/convection reflow	215 ± 5 (component temp)	30 ± 5	1 °C/s-4 °C/s; time above 183 °C, 90 s – 120 s	3
J	IR/convection reflow	235 ± 5 (component temp)	30 ± 5	1 °C/s-4 °C/s; time above 183 °C, 90 s – 120 s	3
K	IR/convection reflow	250 ± 5 (component temp)	30 ± 5	1 °C/s-4 °C/s; time above 183 °C, 90 s – 120 s	3

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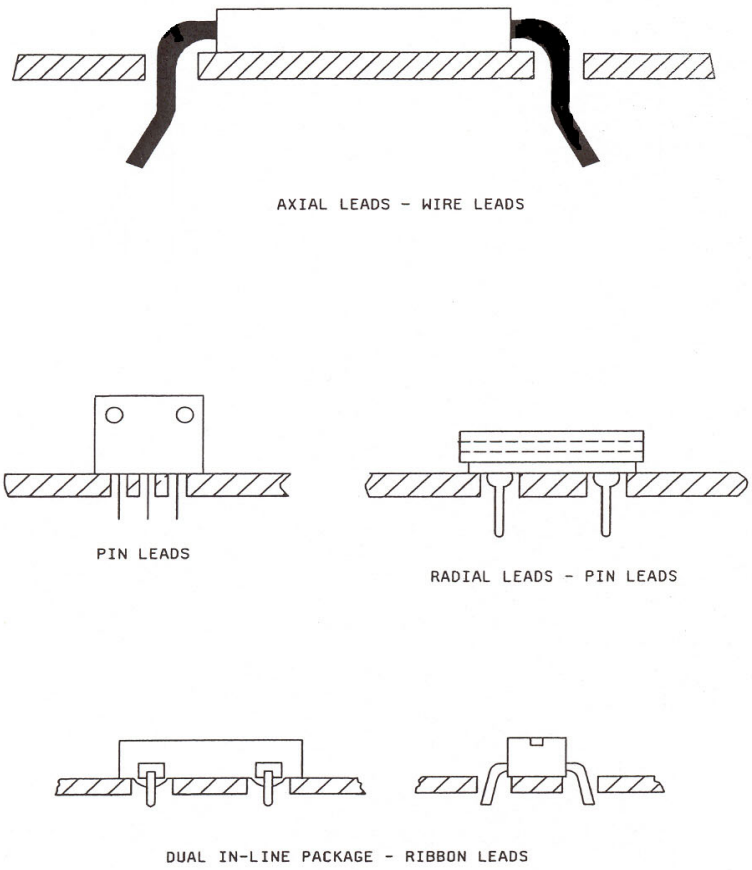

FIGURE 2036-1 Component lead and mounting examples.

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METHOD 2037

X-RAY FLUORESCENCE (XRF) SCAN FOR TIN (Sn)-LEAD (Pb) CONTENT ANALYSIS

1. PURPOSE. The purpose of this test is to verify that the amount of Lead (Pb) in Tin-Lead (Sn-Pb) alloys and electroplated finishes contain at least 3 weight percent (wt%) Lead by using X-Ray Fluorescence (XRF). This test method also establishes the XRF scan locations, and sampling plans for various package styles.

2. APPLICABLE DOCUMENTS. The following document forms a part of this document to the extent specified herein. Unless otherwise specified, the issue of this document is that cited in the solicitation or contract.

2.1 Government documents.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-1916 DOD Preferred Methods for Acceptance of Product.

(Copies of thIs document are available online at http://quicksearch.dla.mil.)

2.2 Non-government publications

JEDEC SOLID STATE TECHNOLGY ASSOCIATION

JEDEC JESD213 Standard Test Method Utilizing X-ray Fluorescence (XRF) for Analyzing Component Finishes and Solder Alloys to Determine Tin (SN) - Lead (Pb) Content.

(Copies of this document are available online at http://www.jedec.org or from the JEDEC Solid State Technology Association, 3103 North 10th Street, Suite 240 South, Arlington, VA 22201-2107.)

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3. APPARATUS.

3.1. XRF Instrument. The XRF instrument shall be capable of qualitatively identifying the metals present in a complex sample and providing quantitative accuracy sufficient to insure at least 3 wt% Lead (Pb).

3.1.1 X-ray detector. A peltier cooled pin diode detector, or similar detector with increased spatial resolution, is the preferred apparatus. A proportional counter detector, or a capillary optic collimated XRF instrument may be used if it can meet the test requirements. (Requirements are based on alignment, focusing, scan area, and spatial resolution. For guidance on these requirements refer to JEDEC JESD213.) The detector used shall be able to quantify lead (Pb) with ± 2 wt% accuracy when operated in the range from 0 to 10 wt%, and in combination with interfering energy lines from elements such as bismuth (Bi). The excitation voltage for the X-rays shall be a minimum of 40 KeV to support detection of higher energy lines.

3.1.2 Positioning fixture. Positioning fixtures or sample trays shall be made of materials that do not interfere with the accuracy of the analysis, e.g., commercially pure aluminum.

3.2 Verification standard. For tin-lead alloys, a tin-lead composition standard with a lead content of 3.0 wt% is required. This Sn-Pb standard shall be a cast alloy sample made from high purity tin and lead. The value for the standard shall be traceable to values provided by the National Institute of Standards and Technology (NIST). If surface finish thickness is a concern, a foil standard of ≥ 99.9 wt% tin of a specified thickness consistent with component design is required.

Note: For guidance on traceability to values for NIST Standard Reference Materials or other certified reference materials, refer to the NIST Policy on Traceability at http://ts.nist.gov/traceability.

4. PROCEDURE.

4.1 Verification. The equipment calibration shall be verified at the beginning of each work shift by measuring the Tin-Lead (Sn-Pb) verification standard. If surface finish thickness is a concern, the foil verification standard shall be read over a substrate similar to the sample. The result must agree with the assigned value for the verification standard after taking into account the uncertainty of the assigned value and the laboratory's uncertainty. (i.e., if a 3.0 wt% Lead (Pb) verification standard has a tolerance of ±10%, the allowable range would be 2.7 to 3.3 wt% Lead (Pb).) It may be useful to implement a control chart to monitor this comparison.

4.2 Sampling plans. Sample size shall be a minimum of five (5) components per plating lot. Visually inspect the surfaces on each sample at 30X to determine the homogeneity of the surfaces. Homogeneous surface devices require measurement of one spot per sample surface. For heterogeneous surface devices, each visually distinct surface requires a separate scan.

4.2.1 Sample surfaces. A sample will typically have multiple surfaces that have been made as separate processes and assembled together; for example, metal leads, can, and lid for a TO type package. Each of the separate component metal surfaces requires a separate scan.

4.2.2. Alternate sampling. Alternate sampling may be use if specified by the contract, or as specified in a statistically based sampling plan derived from MIL-STD-1916. The testing facility shall justify any other sampling plan such as needing to determine the number of spot location measurements required per sample to ensure a high level of confidence is obtained. This determination shall be based upon the equipment used for testing, manufacturing processes, materials used and geometry of the component being tested (see section 4.3 of JEDEC JESD213 for guidance.)

4.3 Measurements. Each sample shall be measured independently. Scanning multiple samples under the X-ray beam at one time is not acceptable. The samples should be measured on a flat surface, when possible. For non-flat or rounded surfaces, the sample must be measured at the center to prevent extending beyond the sample edge. Caution should be exercised to prevent X-ray beam scatter by measuring on non-flat surfaces.

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4.3.1 Capillary optic collimated XRF instruments. Scanning or other averaging to 15 square mil area, or the maximum available area if less than 15 square mils, shall be performed when using a capillary optic collimated XRF instrument.

4.4 Scan Locations and Guidance:

4.4.1 Scan Locations. Figures 2037-1 to 2037-9 show typical scan locations for the most common package styles. Each visually identifiable component metal surface requires a separate scan, for example, metal device leads, cans, and lids for a TO type package all require individual scans. Flat surfaces provide the greatest measurement accuracy. Sharp edges, highly curved surfaces, and locations that will mix responses from dissimilar materials will result in lower accuracy. For non-flat or rounded surfaces, the sample must be measured at the center to prevent extending beyond the sample edge. Caution should be exercised to prevent X-ray beam scatter by avoiding measurements on non-flat surfaces.

4.4.1.1 Scan Locations on Device Leads: Leaded devices shall be measured as closely as practical to the device body, with care to exclude the body material. A second location away from the device body shall also be measured.

4.4.1.2 Scan Locations on Large or Rounded Surfaces: Devices with varied geometry shall be measured at each different plane. In all cases, the X-ray spot or beam size shall be small enough to remain within the area under test with a guard band area approximating the beam diameter. Large pad devices shall be scanned in one location with adequate scan size to meet accuracy and reproducibility requirements, rather than scanning the entire surface (see Figure 2037-1).

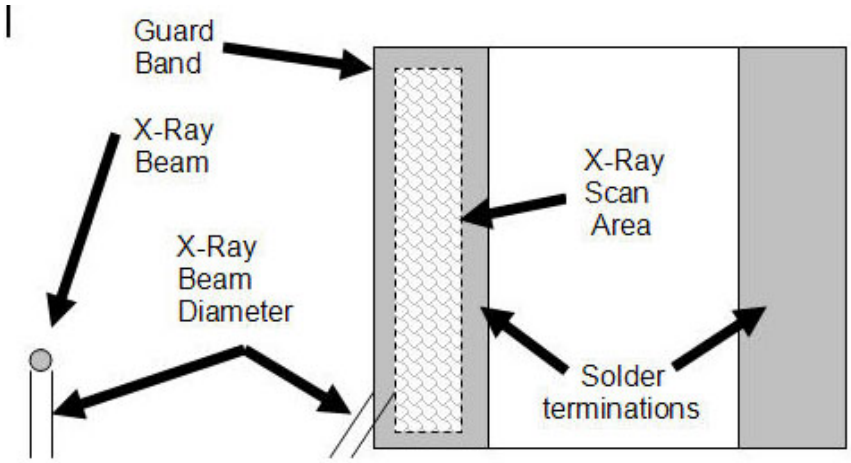

FIGURE 2037-1. Typical Scan Location on Flat Surface Mounted Devices.

4.5 Acceptance Criteria. For Tin (Sn) and Lead (Pb) containing samples the lot shall pass if each of the measured readings are ≥ 3.0 wt% Lead (Pb) unless a greater percentage of Lead (Pb) is specified in the contract or acquisition document. These minimums shall be adjusted to account for the equipment accuracy established per a Gauge Reproducibility and Repeatability study (i.e., if the equipment has an established accuracy of ±20%, then the required minimum is 3.6 wt% Lead (Pb).) One rejected sample shall be cause of rejection for the entire sample lot. A failed lot shall remain rejected, or be reworked, or be evaluated per 4.5.1.

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4.5.1 Alternate Acceptance Method. For a lot that fails the XRF analysis per paragraph 4.5, and that lot is not rejected or reworked, then the alternate acceptance of the XRF materials analysis shall be conducted. This also applies to a lot when segregation of the Lead (Pb) and Tin (Sn) is suspected.

4.5.1.1 The composition shall be confirmed by cross-section and Scanning Electron Microscopy-Energy Dispersive Spectroscopy (SEM-EDS) measurements. Because SEM-EDS does not penetrate as deeply as XRF, measurements shall be taken at the solder surface, in the middle of the cross-section, and at the interface with the substrate. Samples confirmed by SEM-EDS to have <3.0 wt% Pb (Lead) at any scan location shall be considered rejections.

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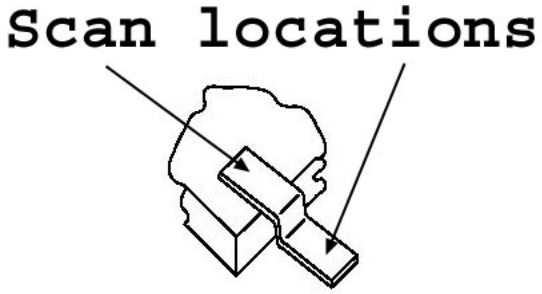

FIGURE 2037-2. Scan Locations on Gull-Wing Lead.

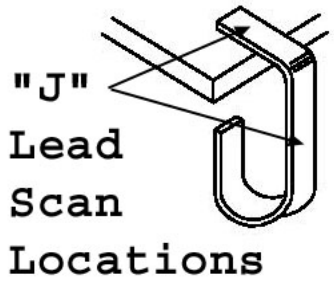

FIGURE 2037-3. Scan Locations on J-Style lead.

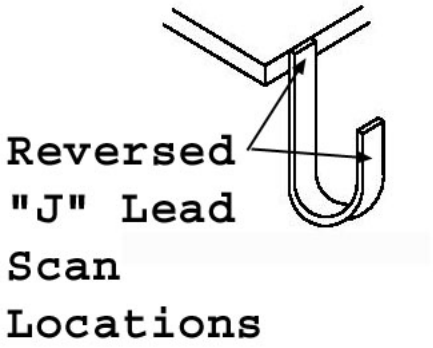

FIGURE 2037-4. Scan Locations on Reversed J-Style lead.

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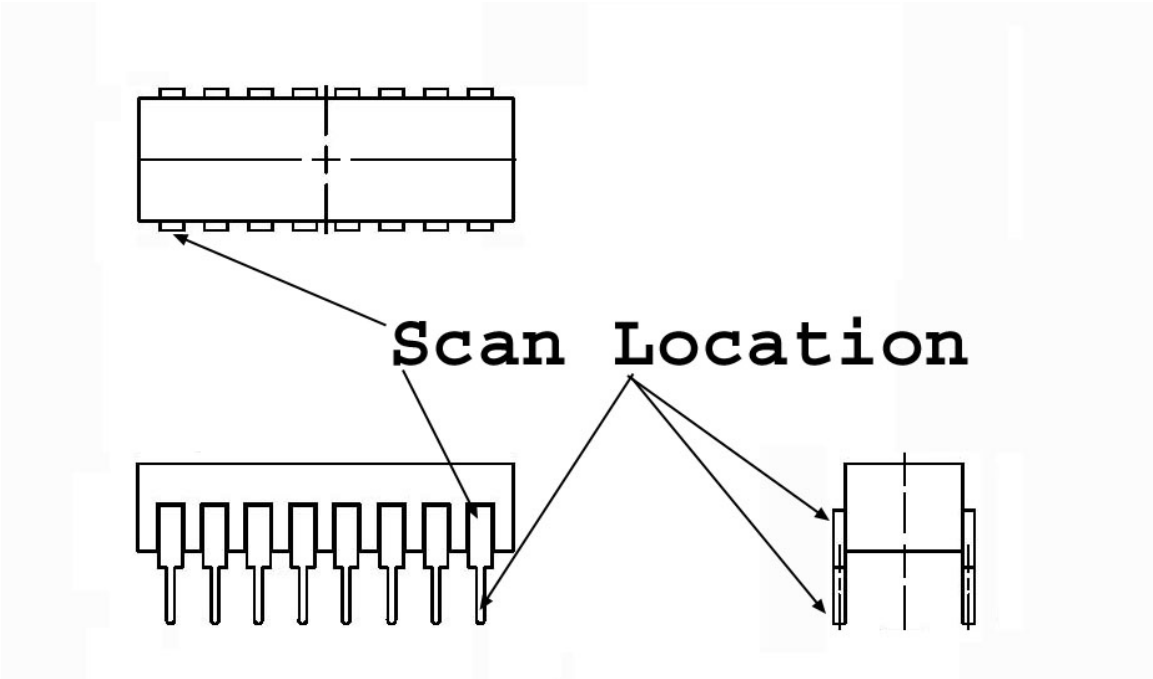

FIGURE 2037-5. Scan Locations on Dual In-Line Package.

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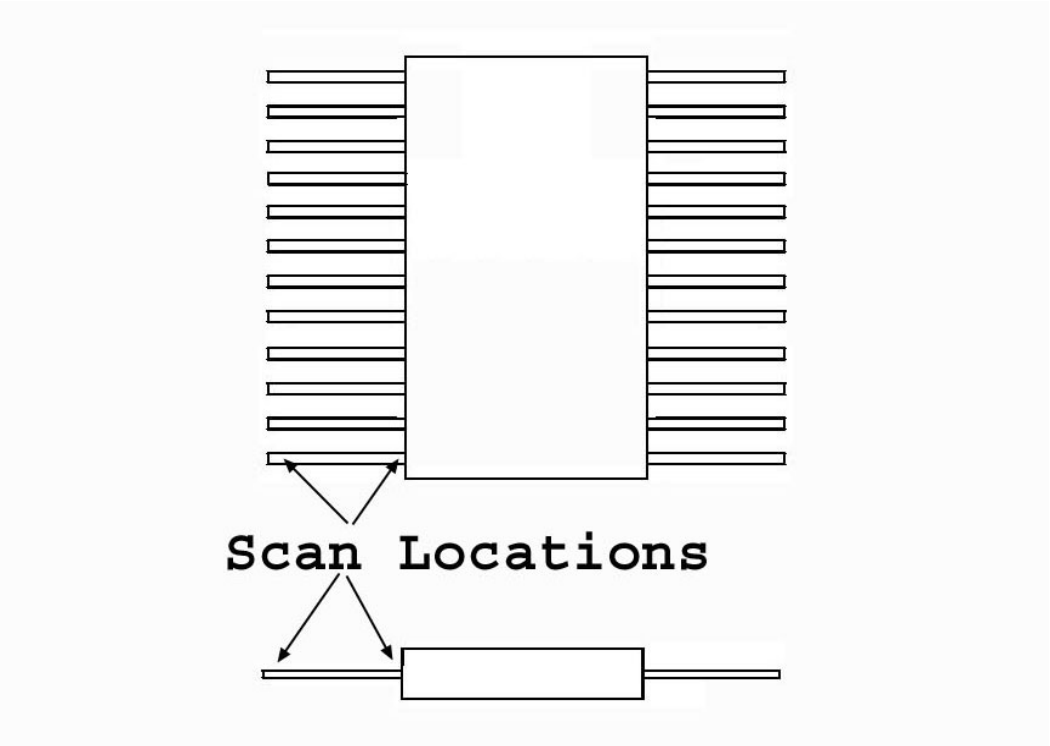

FIGURE 2037-6. Scan Locations on Flat Pack Package.

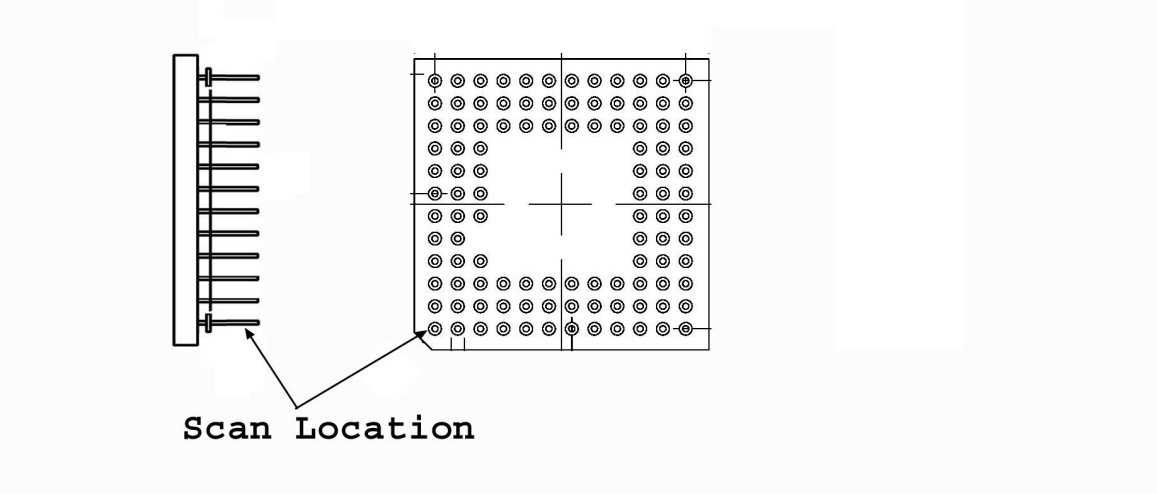

FIGURE 2037-7. Scan Locations on Pin Grid Array Package.

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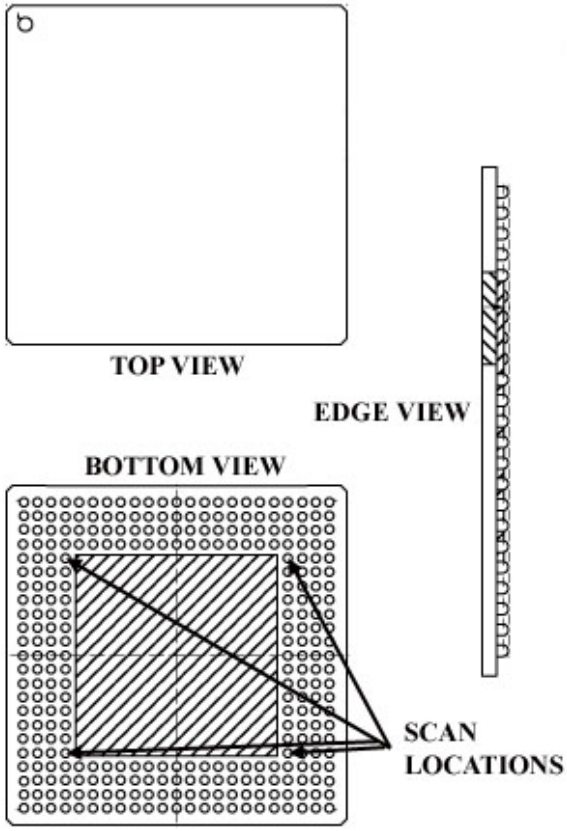

FIGURE 2037-8. Scan Locations on Ball Grid Array Package 1.

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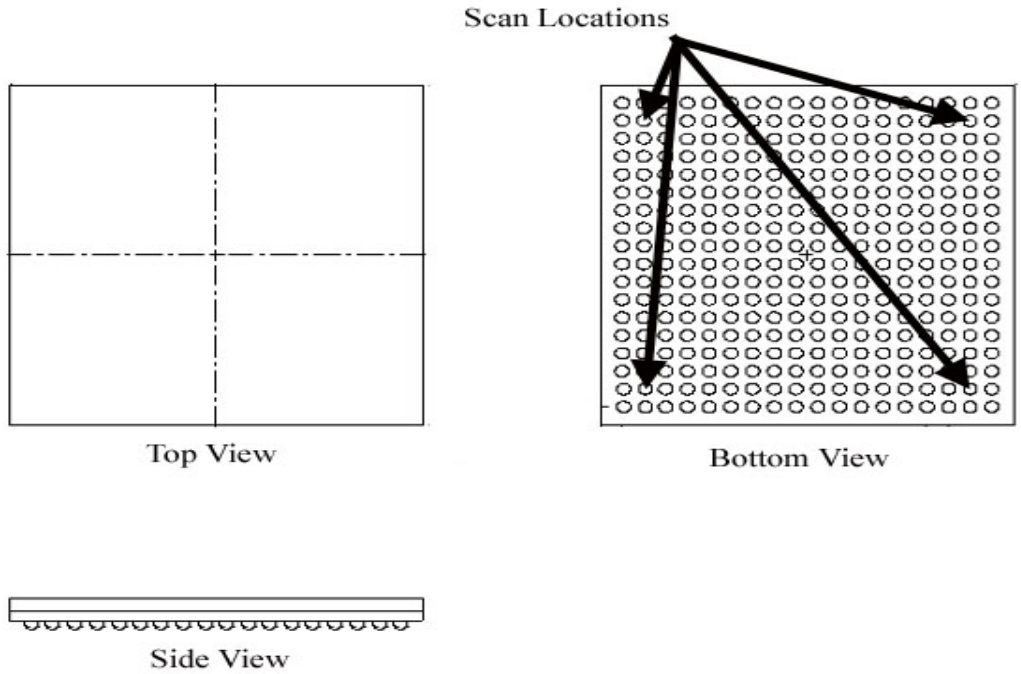

FIGURE 2037-9. Scan Locations on Ball Grid Array Package 2.

NOTE: On Ball Grid Array packages with ball diameters ranging from 0.5 to 0.65 mm, with rounded surfaces, an accurate quantitative analysis is challenging even with a capillary optic XRF, and is more difficult with mechanically collimated XRF. A rounded surface with 0.5 mm diameter is below the size recommended suitable for mechanically collimated XRF, per JEDEC JESD213, Table 1.

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5. SUMMARY. The following details shall be specified in the applicable acquisition document:

a. Sampling plan if other than five (5) components per plating lot.

b. Surfaces and surface locations to be scanned for the type of component sampled.

c. When an alternate acceptance method is used.

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METHOD 2038

SOLDER COLUMN PACKAGE DESTRUCTIVE LEAD PULL TEST

1. PURPOSE. This method provides a test for determining the integrity of solder column type package leads by measuring the capability of the package column to withstand an axial force.

2. APPARATUS. The apparatus for this test shall consist of suitable equipment for applying the specified stress to the package column. A calibrated measurement and indication of the applied stress in grams-force (gf) shall be provided by equipment capable of measuring stresses up to twice the specified minimum limit value, with an accuracy of ±5 percent.

3. PROCEDURE. Tension only shall be applied, without shock, to each lead to be tested in a direction parallel to the axis of the lead. The tension shall be increased until the minimum acceptable pull strength is reached or upon separation of the lead from the package. The tension shall be applied as close to the end of the lead as possible, gripped on no more than half of the column length.

3.1 Pull Rate. Pull rate should not exceed 1.0 inch/minute.

3.2 Failure criteria. The minimum acceptable lead pull strength shall be 2,810 grams-force per square mm of cross-sectional lead area. For typical column diameters, minimum lead pull strengths are defined in table I below.

TABLE I. Minimum lead pull strength.

Column Diameter	Minimum Lead Pull Strength
0.55 mm (0.022 in)	670 grams-force
0.51 mm (0.020 in)	575 grams-force
0.41 mm (0.016 in)	370 grams-force
0.33 mm (0.013 in)	240 grams-force

3.3 Failure category. Failure categories are as follows:

a. Column failure, where failure occurs through the core of the solder column.

b. Pad/column joint failure, where failure occurs at the pad/column attach joint.

c. Pad failure, where failure occurs when the pad is separated from the package.

4. SUMMARY. The following details shall be specified in the applicable acquisition document:

a. Number of leads tested.

b. Measured lead pull strength for each lead tested.

c Failure category for each lead tested.

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CONCLUDING MATERIAL

Custodians:
Army - CR
Navy - EC
Air Force – 85
NASA – NA
DLA – CC

Preparing activity:
DLA – CC

(Project 5962-2019-006)

Review activities:
Army - AR, EA, MI, SM
Navy – AS, CG, MC, SH
Air Force – 03, 19

NOTE: The activities listed above were interested in this document as of the date of this document. Since organizations and responsibilities can change, you should verify the currency of the information above using the ASSIST Online database at https://assist.dla.mil.