NOTICE OF CHANGE

MIL-STD-750D
NOTICE 3
29 February 2000

The documentation and process conversion measures necessary to comply with this Notice shall be completed by 29 August 2000.

DEPARTMENT OF DEFENSE

TEST METHOD STANDARD FOR SEMICONDUCTOR DEVICES

TO ALL HOLDERS OF MIL-STD-750D:

1. THE FOLLOWING PAGES OF MIL-STD-750D HAVE BEEN REVISED AND SUPERSEDE THE PAGES LISTED:

METHOD	NEW PAGE	DATE	SUPERSEDED PAGE	DATE
---	5	28 February 2000	5	Reprinted Without Change
---	6	29 February 2000	6	28 February 1995
---	15	29 February 2000	15	23 February 1996
---	16	29 February 2000	16	23 February 1996
---	17	29 February 2000	17	Reprinted Without Change
---	18	29 February 2000	18	23 February 1996
---	19/20	29 February 2000	19/20	23 February 1996

2. THE FOLLOWING TEST METHODS OF MIL-STD-750D HAVE BEEN REVISED AND SUPERSEDE THE TEST METHOD LISTED:

METHOD	DATE	SUPERSEDED METHOD	DATE
2037.1	29 February 2000	2037	28 February 1995
2052.3	29 February 2000	2052.2	28 February 1995
2070.2	29 February 2000	2070.1	28 February 1995
2075. 1	29 February 2000	2075	28 February 1995
3101.3	29 February 2000	3101.2	28 February 1995
4016.4	29 February 2000	4016.3	28 February 1995
5001.2	29 February 2000	5001.1	28 February 1995

3. THE FOLLOWING NEW METHODS HAVE BEEN ADDED:

METHOD	TITLE	DATE
1080	Single Event Gate Rupture and Drain Burnout Test	29 February 2000
2102	DPA for Wire Bonded Devices	29 February 2000

4. RETAIN THIS NOTICE AND INSERT BEFORE TABLE OF CONTENTS.

5. Holders of MIL-STD-750D will verify that page changes and additions indicated above have been entered. This notice page will be retained as a check sheet. This issuance, together with appended pages, is a separate publication. Each notice is to be retained by stocking points until the military standard is completely revised or canceled.

Custodians:
Army - CR
Navy - EC
Air Force - 11
NASA – NA
DLA-CC

Review activities:
Army - AR, MI
Navy - AS, CG, MC, SH
Air Force – 19, 99

Preparing activity:
DLA - CC

(Project 5961-1881)

4. GENERAL REQUIREMENTS

4.1 Test conditions. Unless otherwise specified herein or in the individual specification, all measurements and tests shall be made at thermal equilibrium at an ambient temperature of 25°C ±3°C, and at ambient atmospheric pressure and relative humidity and the specified test condition C (at environmentally elevated and reduced temperatures) shall have a tolerance of ±3 percent or 3°C, whichever is greater. Whenever these conditions must be closely controlled in order to obtain reproducible results, the referee conditions shall be as follows: temperature 25°C±1°C, relative humidity 50 ±5 percent, and atmospheric pressure from 650 to 800 millimeters of mercury. For mechanical test methods, 2000 series, the ambient temperature may be 25°C ±10°C, unless otherwise specified in the detail test method.

4.1.1 Permissible temperature variation in environmental chambers. When chambers are used, specimens under test shall be located only within the working area defined as follows:

a. Temperature variation within working area: The controls for the chamber shall be capable of maintaining the temperature of any single reference point within the working area within ±2°C or ±4 percent, whichever is greater.

b. Space variation within working area: Chambers shall be so constructed that, at any given time, the temperature of any point within the working area shall not deviate more than ±3°C or ±3 percent, whichever is greater, from the reference point, except for the immediate vicinity of specimens generating heat.

c. Chambers with specified minimum temperatures (such as those used in burn-in and life tests): When test requirements involve a specified minimum test temperature, the controls and chamber construction shall be such that the temperature of any point within the working area shall not deviate more than +8°C, -0°C; or +8 percent, -0 percent, whichever is greater, from the specified minimum temperature, except for the immediate vicinity of the specimens generating heat.

4.1.2 Electrical test frequency. Unless otherwise specified, the electrical test frequency shall be 1,000 ±25 Hertz (Hz).

4.1.3 Accuracy. The specified limits are for absolute (true) values, obtained with the specified (nominal) test conditions. Proper allowance shall be made for measurement errors (including those due to deviations from nominal test conditions) in establishing the working limits to be used for the measured values, so that the true values of the device parameters (as they would be under nominal test conditions) are within the specified limits.

The following electrical test tolerances and precautions, unless otherwise specified in the applicable acquisition document, shall be maintained for all device measurements to which they apply (3000, 4000 series and other specified electrical measurements). Wherever test conditions are specified in the applicable acquisition document to a precision tighter than the tolerances indicated below, the specified conditions shall apply and take precedence over these general requirements.

a. Bias conditions shall be held to within 3 percent of the specified value.

b. Such properties as input pulse characteristics, repetition rates, and frequencies shall be held to within 10 percent. Nominal values should be chosen so that ±10 percent variation (or the actual test equipment variation, if less than 10 percent) does not affect the accuracy or validity of the measurement of the specified value.

c. Voltages applied in breakdown testing shall be held within 1 percent of specified value.

d. Resistive loads shall be ±5 percent tolerance.

e. Capacitive loads shall be ⌖10 percent or ⌖1 picofarad (pF) tolerance, whichever is greater.

f. Inductive loads shall be ⌖10 percent or ⌖5 microhenries (mH) tolerance, whichever is greater.

g. Static parameters shall be measured to within 1 percent.

h. Switching parameters shall be measured to within 5 percent or 1 nanosecond (ns), whichever is greater.

4.1.3.1 Test methods and circuits. Unless otherwise stated in the specific test method, the methods and circuits shown are given as the basic measurement method. They are not necessarily the only method or circuit which can be used, but the manufacturer shall demonstrate to the acquiring activity that alternate methods or circuits which he may desire to use are equivalent and give results within the desired accuracy of measurement (see 4.1.3).

* 4.1.4 Calibration requirements. Calibration and certification procedures shall be provided in accordance with ANSI/NCSL-Z540-1-1994 for plant standards and instruments used to measure or control production processes and semiconductor devices under test. For those measurements that are not traceable to the National Institute of Standards and Technology (NIST), correlation samples shall be maintained and used as the basis of proving acceptability when such proof is required. In addition, the following requirements shall apply:

a. The accuracy of a calibrating instrument shall be at least four times greater than that of the item being calibrated, unless the item being calibrated is state of the art equipment, which may be near or equal in accuracy to the state of the art calibrating equipment, in which case the four time requirement does not apply. However, the instrument shall be calibrated to correlate with standards established by the NIST.

b. Except in those cases where the NIST recommends a longer period and concurrence is obtained from the qualifying activity, calibration intervals for plant electrical standards shall not exceed one year, and for plant mechanical standards shall not exceed two years.

4.2 Orientations:

X is the orientation of a device with the main axis of the device normal to the direction of the accelerating force, and the major cross section parallel to the direction of the accelerating force.

Y is the orientation of a device with the main axis of the device parallel to the direction of the accelerating force, and the principal base toward (Y_1), or away from (Y_2), the point of application of the accelerating force.

Z is the orientation of a device with the main axis and the major cross section of the device normal to the direction of the accelerating force. Z is 90° of X.

NOTE: For case configurations, other than those shown on figures 1 and 2, the orientation of the device shall be as specified in the individual specification.

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METHOD 1080

SINGLE-EVENT BURNOUT AND SINGLE-EVENT GATE RUPTURE TEST METHOD

1. Purpose. The purpose of this test method is to describe the procedure for conducting heavy ion irradiation of power MOSFETs. This test method establishes a procedure for characterization and for verification (acceptance or qualification) of discrete power MOSFETs for single-event burnout (SEB) and single-event gate rupture (SEGR). In principle, this test method may be applicable to testing where neutrons, protons, or other light particles are used.

1.1 Definitions. The following symbols and terms shall apply for the purpose of this test method:

a. Cross-sectional area: Calculated as the number of events per unit fluence.

b. DUT: Device under test.

c. Fluence: The ion flux integrated over the time required for the run, expressed as ions/cm^2.

d. Flux: The number of ions passing through a one cm^2 area perpendicular to the ion beam per unit of time, expressed as ions/$cm^2 \bullet s$.

e. I_{DS}: The measured drain-to-source current (amps).

f. I_{GS}: The measured gate-to-source current (amps).

g. Linear energy transfer (LET): The amount of energy transferred per unit length as the ion travels through a material, expressed as MeV/(mg/cm^2) in this test method.

h. Single-event burnout (SEB): A single-ion-induced condition that causes a localized high-current state resulting in a catastrophic device failure characterized by an increase in drain current that exceeds the manufacturer's rated leakage current at the drain electrode.

i. Single-event gate rupture (SEGR): A single-ion-induced condition that causes a localized defect in the gate dielectric resulting in a catastrophic device failure, characterized by an increase in gate current that exceeds the manufacturer's rated leakage current at the gate electrode.

j. SEB circumvention: A technique used to prevent the device from catastrophically failing during an SEB event.

k. SEB cross-sectional area: Calculated as the number of SEB events per unit fluence.

l. SEGR cross-sectional area: Calculated as the reciprocal of the fluence required to induce the SEGR event.

m. SEGR post gate-stress test: After the heavy ion irradiation, a test is conducted to verify the gate integrity by applying the maximum specified V_{GS}.

n. Threshold LET: The minimum LET required to cause a single-ion-induced failure under the specified bias conditions.

o. V_{DS}: The applied drain-to-source voltage (volts).

p. V_{GS}: The applied gate-to-source voltage (volts).

q. V_{TH}: The value of V_{GS} where the inversion layer is formed and the device turns on.

1.2 Applicable documents. The following documents form part of this test method. The most current revision of these documents shall take precedence over those cited.

EIA/JESD57 - Test Procedures for the Measurement of Single-Event Effects in Semiconductor Devices from Heavy Ion Irradiation.

ASTM F-1192 - Standard Guide for the Measurement of Single-Event Phenomena from Heavy Ion Irradiation of Semiconductor Devices.

1.3 Device handling. Special care shall be taken to ensure that the devices are not damaged before testing. Since the lids are removed before irradiation, extra precautions shall be taken to protect the exposed die. Otherwise, devices shall be handled in accordance with standard operating procedures to protect against damage and electrostatic discharge. Use of anti-static foams, grounding straps, and other precautions is recommended.

NOTE: Some power MOSFETs may require voltages that exceed 500 volts and voltages in excess of 32 volts can present a safety hazard. Safety precautions shall be taken to ensure safe operation of all equipment and personnel. Note that conformal coatings may interfere with the test, changing the penetration depth of the ion as well as degrading the ion energy. The effect of conformal coatings shall be evaluated. Conformal coatings, such as polyamide, should be chemically removed before testing.

2. Apparatus. The apparatus required for SEB/SEGR testing consists of a heavy ion source, a vacuum chamber system, DUT test instrumentation, test circuit board(s), cabling, switching system (if required), an x-y-z stage system (if required), and dosimetry measurement instrumentation. Precautions shall be taken to obtain an electrical measurement system with sufficient insulation, shielding, and grounding to measure a gate current, I_{GS}, of 10 nA or less (measurement resolution).

2.1 Heavy ion source. The heavy ion source shall be a cyclotron, Van de Graaff accelerator, or other suitable source. The heavy ion source shall be capable of providing an average ion flux up to 100,000 ions/cm^2•s. The average beam uniformity should be maintained within ±15 percent over the die area unless otherwise specified. The ion beam energy shall provide sufficient ion penetration depth to induce the SEGR response or as agreed to by both parties to the test. Note that the accelerator design determines the maximum ion beam energy; and, therefore, some accelerators may be inadequate to perform a worst-case test condition. Also, note that some accelerators are rf-type machines (e.g. cyclotrons) and may have higher instantaneous fluxes.

2.2 Vacuum chamber system. The chamber shall have a test circuit board mounting frame and cable feed-through. The vacuum chamber system should be capable of accepting an x-y-z stage mechanism. The pumping system shall be capable of evacuating the vacuum chamber below1.3 x 10^{-1} Pa (10^{-3} torr). Precautions shall be taken to ensure that any component placed in the vacuum chamber does not interfere with the vacuum system. Note that certain materials can out-gas, affecting the vacuum quality. Also note that some capacitors (e.g., electrolytic capacitors) can explode, fail, or out-gas when placed in a vacuum.

2.3 Test instrumentation. Standard electrical test instruments capable of establishing the required test conditions and measuring the required electrical parameters shall be used. Note that many power MOSFETs may require operating voltages in excess of 32 volts and safety precautions shall be followed to ensure safe operation of all equipment and personnel."

2.3.1 SEB instrumentation. Test instrumentation to bias and monitor the DUT may consist of one or more of the following types of instruments:

a. Power supply.

b. Ammeter.

c. Voltmeter.

d. Counter.

e. Oscilloscope.

2.3.2 SEGR instrumentation. Test instrumentation to bias and monitor the DUT may consist of one or more of the following types of instruments:

a. Power supply.

b. Ammeter.

c. Voltmeter.

2.4 Test circuit board. The test circuit board contains the test socket, delidded DUT, any additional wiring, and any auxiliary components. The test board provides a mounting surface and interface between the test instrumentation and the DUT, applying V_{GS} and V_{DS}, while monitoring I_{GS} and I_{DS}. Figure 1 shows a representative test circuit and figure 2 shows a typical SEB circumvention and monitoring technique. Any auxiliary components, such as the resistors, capacitors, or current probes, shall be included in the final test circuit. Any accepted SEB circumvention and monitoring technique is acceptable. The test board can have multiple test sockets to minimize the time required to vent and evacuate the vacuum chamber. The test socket, in which the DUT is inserted, is mounted in such a way that the DUT surface shall be perpendicular (nominally within ±5°C) to the heavy ion beam. The DUT is delidded prior to testing, and the entire die shall be irradiated.

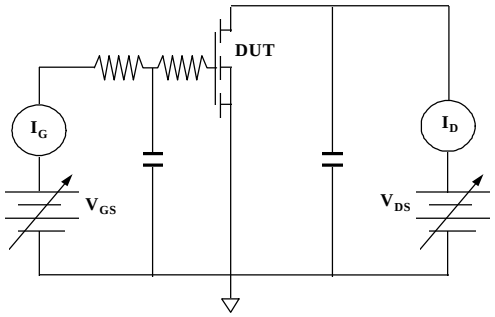


FIGURE 1080-1. Basic SEB/SEGR test circuit.

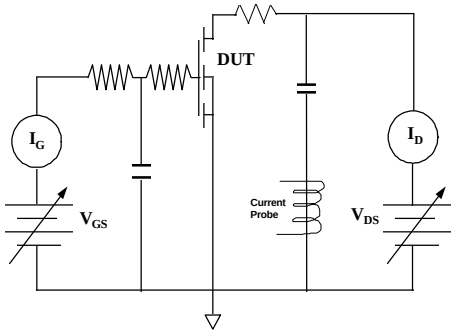


FIGURE 1080-2. SEB circumvention and monitoring circuit.

2.5 Cabling. Cables are typically used to connect the test circuit board, located in the vacuum chamber, to the test instrumentation, normally placed outside the vacuum chamber. The cable length shall be minimized to prevent interference with the desired measurement. However, the actual cable length is dictated by the size of the vacuum chamber, the spatial location of the test board with respect to the cabling feed-throughs, and the minimum distance from the cabling feed-throughs to the DUT test instrumentation. Observation of SEB pulses shall be performed using properly terminated shielded cables to minimize reflections and other signal/noise interference.

2.6 Switching system. A switching system can be used when multiple devices are placed on the test board. The switching system shall provide electrical isolation between the gate and drain electrodes of the various test devices on the test board. Inclusion of a switching system shall not interfere with the electrical measurement system, as specified in 2.

2.7 X-Y-Z stage system. If multiple devices are placed on the test board, an x-y-z stage system can be used to provide a mechanical mechanism to move the device into and out of the heavy ion beam.

2.8 Dosimetry system. The dosimetry system shall be used to determine the ion beam energy, LET, average ion beam flux, fluence, and average ion beam uniformity. Note that many facilities provide this dosimetry system.

3. SEB/SEGR prediction. To assist in the preparation of the test plan and the selection of initial bias conditions, an appropriate SEB/SEGR prediction method may be utilized to predict the SEB/SEGR failure thresholds. The preferred prediction method is to use previous measurements on similar device types. Test personnel should use these predicted failure thresholds to help verify that the SEGR and SEB test measurements are valid. If a significant difference (nominally greater than a ±30 percent deviation from the predicted response) is observed, the test personnel should verify the test setup including the ion specie, ion energy, bias conditions, and device type. These predictions can help to develop the overall test plan.

3.1 SEB prediction. Currently, there are not any accurate prediction models available for SEB. Predictions based upon previously obtained SEB data are helpful, but, due to the nature of the failure mechanism, cannot be used to accurately predict SEB.

3.2 SEGR prediction. Predictions of SEGR can be made from previous SEGR data or calculated using currently accepted models. If previous test results are unavailable or the device layout, design, or process has been modified, then SEGR failure thresholds can be predicted using an empirical prediction method or an analytical prediction method.

3.2.1 SEGR empirical prediction. The empirical prediction method uses an empirically derived equation to predict the SEGR failure threshold of the oxide capacitor when V_{DS} = 0 volts, as expressed by Equation (1).

$$V_{GS} = \frac{(E_{OX\_BR})(T_{OX})}{\left(1 + \frac{LET}{53}\right)}$$

Where: E_{OX_BR} is the breakdown field strength of the oxide (V/cm),
T_{OX} is the thickness of the gate oxide dielectric (cm), and

LET_PEAK is the maximum LET value of the given ion species in MeV/mg/cm2.

An approximation of the substrate response for the case when V_{DS} is biased can be obtained by using an expanded form of equation 1. This expanded equation is expressed by equation (2).

$$V_{GS} = (0.84)(1 - e^{-\frac{LET}{17}})(V_{DS}) - \frac{(E_{OX\_BR})(T_{OX})}{\left(1 + \frac{LET}{53}\right)}$$

Where: E_{OX_BR} is the breakdown field strength of the oxide (V/cm),
T_{OX} is the thickness of the gate oxide dielectric (cm), and
LET is the linear energy transfer in (MeV/mg/cm2).
LET PEAK is the maximum LET value of the given ion species in MeV/mg/cm2

3.2.2 SEGR analytical prediction. Analytical predictions can be obtained using sophisticated numerical simulations to predict the SEGR failure threshold response. Additional information concerning these predictions can be found in the literature.

4. Characterization tests. Characterization testing is that testing required to obtain an SEB cross-sectional area curve, an SEGR cross-sectional area curve, or an SEGR failure threshold curve. Data points are taken to describe the response of the discrete MOSFET as a function of V_{GS} and/or V_{DS} over the operating range of the device and/or over a range of LET values. Characterization testing should be conducted initially to define the worst-case operating conditions of the device or to identify the sensitive die area. Additional characterization testing may be required after process and/or design changes have been made to the device. Characterization tests are useful for establishing the conditions for subsequent verification tests. Characterization testing does not have to be performed as a part of the verification testing unless fabrication changes have been made that might invalidate the initial technology characterization. Note that angling the die surface away from the plane where the ion beam is perpendicular to the die surface to produce an effective LET is invalid and shall not be used. It has been reported that the ion energy can influence the measured SEGR failure thresholds, suggesting that the ion energy shall be considered when a worst-case test condition is specified. The maximum allowable V_{DS} bias increment for a DUT shall be no more than 10 percent of the device's rated drain voltage. The maximum allowable V_{GS} bias increment for a DUT shall be no more than 5 volts. Smaller V_{DS} and V_{GS} bias increments are recommended. Also, note that increasing the DUT's operating temperature has been demonstrated to increase the LET threshold for SEB but not for SEGR, indicating that lower operating temperatures are a worst-case test condition.

4.1 SEB characterization**.** Characterization requires that an SEB circumvention method be utilized. SEB characterization produces a cross-sectional area curve as a function of LET for a fixed V_{DS} and V_{GS}. SEB is not sensitive to changes in the gate bias, V_{GS}. The V_{GS} bias shall be sufficient to bias the DUT in an "off" state (a few volts below V_{TH}), allowing for total dose effects that may reduce the V_{TH}. Multiple SEB cross-sectional area curves may be required, expressing different operating conditions for V_{DS}. Note that p-channel devices have not been demonstrated to be sensitive to SEB.

4.1.1 SEB cross-sectional area If specified as a test requirement and if SEB is observed, one of the many reported techniques can be used to circumvent catastrophic SEB failure, such as a current-limiting resistor placed between the drain stiffening capacitor and the drain electrode. Then, to obtain an SEB error count, a current probe (Tektronix CT-2, sense resistor, or other suitable current probe) shall be inserted between the source electrode and ground. Using this setup, an SEB event will produce current pulses. SEB occurrence can be monitored using an electronic oscilloscope to record the shape of the SEB pulse(s), if required, and a pulse counter to record the number of SEB occurrences. A point on the SEB cross-sectional area curve is then obtained by dividing the number of SEB events by the fluence for that given test condition. The SEB cross sectional curve is subsequently found by finding points at several different LET values. After the DUTs have been delidded and the chamber evacuated, apply the specified V_{GS} and V_{DS} bias condition; and irradiate the DUT to the specified fluence level (typical ranges are between 10^5 and 10^7 ions/cm^2). If SEB occurs, record the event by incrementing the counter. The flux shall be adjusted so that the number of SEB events is no more than 100 events per second. When the desired fluence is achieved, the beam is shuttered; and the total number of SEB events are recorded. This process is continued, selecting different ions to obtain the required LET values. Repeat this process for the specified samples and conditions.

4.2 SEGR characterization. SEGR characterization may produce three unique curves: an SEGR cross-sectional area curve as a function of LET for a fixed V_{GS} and V_{DS} bias condition, an SEGR threshold curve of V_{GS} as a function of V_{DS} for a fixed LET value, or an SEGR threshold curve of V_{DS} as a function of LET at a fixed V_{GS}. Multiple SEGR cross sectional area curves may be required to express different V_{DS} and V_{GS} conditions. Multiple SEGR threshold curves may be required to express different V_{GS}, V_{DS}, or LET conditions. SEGR characterization may be performed in conjunction with SEGR verification.

4.2.1 SEGR cross-sectional area. If specified in the test requirements and if SEGR occurs, an SEGR cross-sectional area curve can be obtained. However, SEGR cannot be circumvented. Hence, to obtain an SEGR cross-sectional area curve requires the destruction of numerous devices. For a given device, the ion irradiation would be terminated upon detection of SEGR. One point on the SEGR cross-sectional area curve can be obtained by dividing one SEGR event by the measured fluence to induce that event. After the DUTs have been delidded and the chamber evacuated, apply the specified V_{GS} and V_{DS} bias condition; and irradiate the DUT to the specified fluence level. If SEGR occurs, immediately terminate the exposure; and record the accumulated fluence. Note that the ion flux can be lowered to obtain a more accurate fluence. If the maximum fluence is achieved and the DUT passes the post gate-stress test, a new test condition or a new DUT is selected. If SEGR occurs, a new DUT is selected. Apply the new test condition (incrementing V_{GS}, V_{DS}, or changing the ion specie). This process is repeated until the desired curve is obtained. Repeat this process to obtain the required curves. Note that characterization results in device failure and only represents a single data point for that device. For the special case where the applied dc field across the gate dielectric is less than 1 MV/cm, the procedure to obtain a cross-sectional area curve should be modified as follows:

a. An incremental fluence should be set at one-third of the die area or less;

b. After each irradiation step, a post gate-stress test shall be performed to verify device functionality;

c. If SEGR is not detected, continue irradiation steps until SEGR occurs or until the maximum accumulated fluence is obtained; and

d. Select new device and bias condition and repeat test procedure until the desired curve is obtained.

4.2.2 SEGR post gate-stress test. If the gate bias is small (typically V_{GS} < 10 volts) during irradiation, SEGR may or may not produce a catastrophic failure until sufficient gate bias is applied. If an insufficient gate bias is applied, SEGR may only produce a latent defect site. Therefore, after the irradiation, a post gate-stress test shall be performed on each test device. The post gate-stress test shall apply a gate bias equal to the maximum operating gate voltage (nominally ±10 percent) or as specified.

5. Verification tests. Verification testing requires the irradiation of the DUT to specified test conditions (e.g. gate bias, drain bias, ion species, ion energy, ion LET, ion range, ion flux, and ion fluence). Verification testing is useful for hardness assurance and qualification testing of discrete power MOSFETs to determine their suitability at the specified test conditions. These tests use a "pass"/"no pass" criterion and can be destructive. Note that angling the die surface away from the plane where the ion beam is perpendicular to that surface to produce an effective LET is invalid and shall not be used to conduct these tests. It has been reported that the ion energy can influence the measured SEGR failure thresholds, suggesting that the ion energy should be considered to achieve a worst-case test condition. Also, note that increasing the DUT's operating temperature has been demonstrated to increase the LET threshold for SEB but not for SEGR, indicating that lower operating temperatures are a worst-case test condition.

5.1 SEB verification tests. For SEB verification, a sufficiently large capacitance is placed at the drain electrode to produce catastrophic failure. Note that no circumvention techniques are used in this test. After the DUTs have been delidded and the chamber evacuated, apply the specified V_{GS} and V_{DS} bias condition and irradiate the DUT to the specified fluence level. If failure occurs, the exposure can be terminated. Record SEB results. Repeat for the specified samples and conditions.

5.2 SEGR verification tests. For SEGR verification, this test is a two-step process. After DUTs have been delidded and the chamber evacuated, apply the specified VGS and VDS bias condition and irradiate the DUT to the specified fluence. If failure occurs, the exposure can be terminated. The second step requires a post gate-stress test to be performed after irradiation, if the gate bias during irradiation was less that the maximum operating gate voltage. Record SEGR result. Repeat for the specified samples and conditions.

6. SEB/SEGR test procedure. The test plan should document the proper steps to be followed before, during, and after heavy ion irradiation. Sufficient samples shall be obtained to conduct the test. Samples with conformal coatings, such as polyamide, should be chemically removed before testing. SEB and SEGR both can result in catastrophic failure that produces large leakage currents, destroying the device. In SEB testing, a capacitance sufficient to hold the bias voltage within ±10 percent may be required to induce damage during an SEB event. For characterization testing, SEB can be circumvented and recorded producing an SEB event count, which then can be used to produce a point on the cross-sectional area curve. To help select the proper biases, an SEB/SEGR prediction shall be made. The required ion specie is selected and the ion beam energy shall be tuned and verified using the dosimetry system. The test circuit board, cabling, and instrumentation shall be connected and its operation verified. Before irradiation, test devices shall be delidded and inserted into the test board. The drain and gate currents, I_{GS} and I_{DS}, shall be monitored before, during, and after the irradiation(s), as well as during the post gate-stress test, to verify the condition of the DUT. After completion of the test run, the results of the test shall be recorded and documented.

6.1 Test plan. A test plan shall be devised that supports each test. The test plan shall be used as a guide for the procedures and decisions during irradiation. The test plan shall be developed, and the following conditions shall be outlined.

6.1.1 Ion specie and energy. The test plan shall identify the ion specie and an appropriate energy to perform the test. Selection of a specific ion specie and its energy determines the LET value. Obtaining a range of LET values requires using different ion species at different energies. Note that using angles to modulate the LET value is unacceptable. Selection of a different ion specie and energy by test personnel requires verification that the ion LET and its range meet the test requirements. Verification can be made using the TRIM code or other suitable simulation codes for the given device material. Also, note that the energy of the ion beam has been shown to influence the SEGR failure thresholds. Therefore, determination of the worst-case test condition can require multiple irradiations with the same ion at different energies.

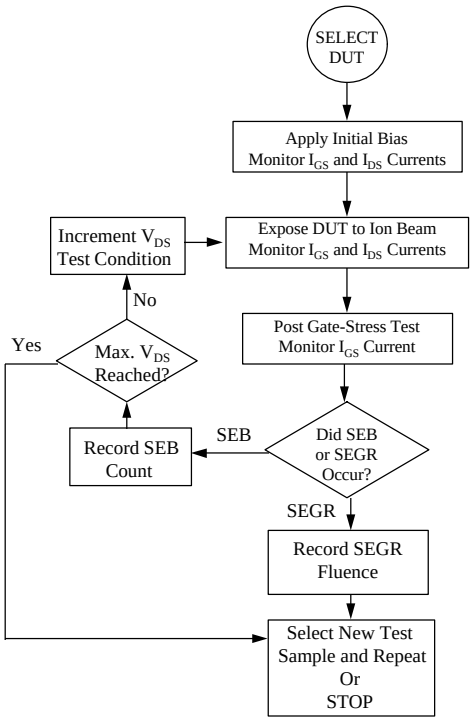
6.1.2 Device information. The test plan shall provide a description of the devices to be tested and the number of test samples required for each test. The test plan shall identify the device type, acceptance lot, and other critical information. Devices shall be marked for traceability so that lids can be removed. Identification markers should be placed on the flange and not on the lid. Only devices that have passed the pre-electrical tests shall undergo heavy ion testing. Test samples shall be randomly selected from the parent population. The number of samples shall be specified to meet the test requirements. For the purposes of verification testing, a representative sample should be selected from the lot.

6.1.3 Electrical parameters. The test plan shall specify the electrical parameters to be measured before and after irradiation.

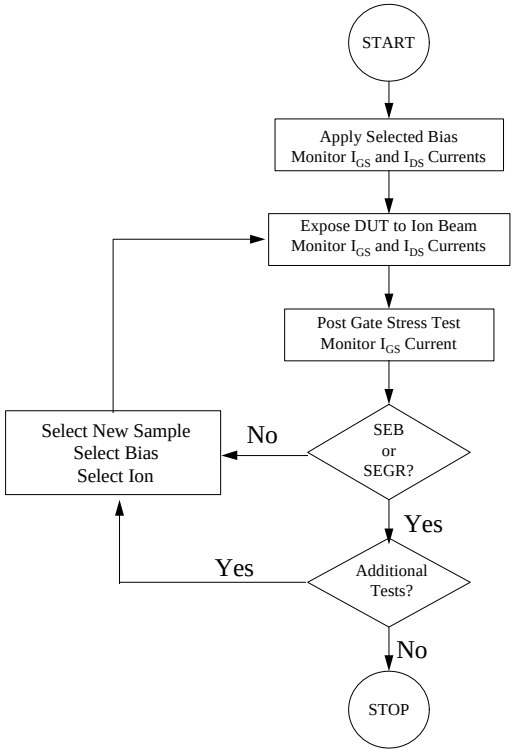
6.1.4 Test configuration. The test plan shall specify the bias and exposure conditions for each test sample. The test plan shall specify the case temperature of the DUT if it is required to be set at other than the room ambient temperature.

6.1.5 Test sequence. The test plan should specify a test sequence similar to figure 1080-3. For characterization testing, the test plan shall define an initial bias condition and the bias increment. The V_{DS} bias increment shall not exceed 10 percent of the device's rated drain breakdown voltage. For verification testing, the test plan shall define the specified biases, the minimum number of samples that shall be tested at each bias, and the handling of the devices after testing. Any additional electrical tests shall be specified and any special handling requirements shall be specified.

6.1.6 SEB/SEGR detection. The test plan shall specify the procedure to monitor the drain and gate currents, I_{GS} and I_{DS}, before, during, and after the irradiation(s). In addition, the gate and drain currents shall be monitored during the post gate-stress test to verify that the DUT was not damaged during the previous irradiation.



Characterization flowchart sample.



Verification flowchart sample.

FIGURE 1080-3. Test plan flowcharts.

6.1.7 Data recording. The test plan shall specify the necessary parameters that shall be recorded during the test.

6.1.8 Reporting requirements. The test plan shall specify the test documentation as required by 7 herein.

6.2 Radiation test procedure. The test plan shall be used as a guide to perform the radiation test. A typical SEB/SEGR test procedure is given here as an example.

a. Test personnel shall specify the selected ion specie and energy to the facility operators as defined in the SEGR/SEB test plan specifying the desired flux, fluence, LET, range, and beam uniformity. Dosimetry shall be performed to verify that the ion beam characteristics are as specified.

b. The SEGR/SEB test board shall be mounted in the test fixture mounting frame. All necessary test cables shall be connected to the test board and vacuum feed-through inside the vacuum chamber.

c. The test instrumentation shall be set up as close as possible to the vacuum chamber. All necessary test cables shall be connected to the test hardware and vacuum feed-through outside the vacuum chamber.

d. When the test system is set up, the operation of the test system shall be verified for continuity and operation. Note that a quick check can be performed by applying a V_{GS} and V_{DS} and verifying the presence of these voltages with a voltmeter.

e. After test system verification is completed, ground all electrodes; and insert the devices for test. Handling of devices shall be in accordance with normal ESD practices. If lids were not removed before placement on the test board, remove the device lids. To verify that the devices were not damaged during the delidding process or insertion into the test board, a simple electrical check of I_{GS} and I_{DS} should be performed.

f. After device verification is completed, the device to be tested shall be aligned to the ion beam. With the beam shuttered and the DUT biases set at 0 volts, perform an alignment of the DUT to the ion beam. Note that some facilities provide a laser alignment system for this task.

g. When positional alignment is complete, turn off any lighting systems and laser systems in the vacuum chamber. Apply the selected bias conditions to the DUT; and begin monitoring the gate and drain leakage currents, I_{GS} and I_{DS}. Note that excitation by lights or laser may produce photocurrents which may interfere with the measurements.

h. When ready, open the ion beam shutter, exposing the DUT to the heavy ion beam. Note that most facilities include instrumentation to monitor the ion beam characteristics monitoring the average flux, fluence, and beam uniformity which should be recorded. When the desired fluence level is achieved, shutter the ion beam, terminating the irradiation.

   (1) If performing an SEB characterization test, the test circuit shall include an appropriate circumvention technique and a current-sensing circuit. The number of current pulses for each irradiation shall be recorded (see 4.1).

   (2) If performing an SEGR characterization test, the ion beam shall be shuttered immediately following the detection of SEGR- any significant gate current change. The ion fluence at failure shall be recorded. Note that detection of SEGR may require the test personnel to make a judgment concerning the SEGR status of the device.

   (3) If performing an SEGR or SEB verification test, the gate and drain leakage currents, I_{GS} and I_{DS}, shall be monitored. If a current change is recorded (typically, a flag can be set, e.g. an $I_{GS} > 10^{-7}$ amps), document the observed conditions.

i. After the ion beam is shuttered, a post gate-stress test shall be performed. During the post gate-stress test (the rated gate voltage is applied), the gate current shall be monitored. If a current change is detected (typically, a flag can be set, e.g. an $I_{GS} > 10^{-7}$ amps), document any observed conditions.

j. Upon completion of the post gate-stress test, record all pertinent test data. Record run number, ion specie, ion energy, range, LET, average flux, fluence, and test conditions (V_{GS}, V_{DS}). Record any changes in the drain or gate currents (I_{GS} and I_{DS}) before, during, and after the ion irradiation. Record any changes in the drain and gate currents, I_{GS} and I_{DS}, during the post gate-stress test. Determine the status of the test run. If the test is a characterization test, increment the test condition or select new device as required. Repeat test procedure. If the test is a verification, select next device and test conditions. Repeat test procedure.

7. Data formatting reporting. Test data/test reports shall be maintained and shall include the following information:

   a. Device type, identification marker, lot identification, and date code.

   b. Test date and test personnel names.

   c. Facility, accelerator type, identification of ion, energy, average flux, LET, range in device material, and fluence.

   d. Schematic of test circuit or test board.

   e. Dosimetry output of each ion beam used.

   f. Bias condition of each exposure run.

   g. Record of observed SEGR or SEB (current changes).

   h. Device case temperature (only if required at other than room ambient)

METHOD 2037.1

BOND STRENGTH (DESTRUCTIVE BOND PULL TEST)

1. PURPOSE. The purpose of this test is to measure bond strengths, evaluate bond strength distributions, or determine compliance with specified bond strength requirements of the applicable acquisition document. This test may be applied to the wire-to-die bond, wire-to-substrate bond, or the wire-to-package lead bond inside the package of wire-connected microelectronic devices bonded by soldering, thermocompression, ultrasonic, or related techniques. It may also be applied to bonds external to the device such as those from device terminals-to-substrate or wiring board or to internal bonds between die and substrate in non-wire-bonded device configurations such as beam lead or flip chip devices.

2. APPARATUS. The apparatus for this test shall consist of suitable equipment for applying the specified stress to the bond, lead wire or terminal as required in the specified test condition. A calibrated measurement and indication of the applied stress in grams force (gf) shall be provided by equipment capable of measuring stresses up to twice the specified minimum limit value, with an accuracy of ±5 percent or ±0.25 gf, whichever is the greater tolerance.

3. PROCEDURE. The test shall be conducted using the test condition specified in the applicable acquisition document consistent with the particular device construction. All bond pulls shall be counted and the specified sampling, acceptance, and added sample provisions shall be observed, as applicable. Unless otherwise specified, for conditions A, C, and D, the sample size number specified for the bond strength test shall determine the minimum sample size in terms of the minimum number of bond pulls to be accomplished rather than the number of complete devices in the sample, except that the required number of bond pulls shall be randomly selected from a minimum of 4 devices. Bond pulls in accordance with test conditions D, F, G, and H, while involving two or more bonds shall count as a single pull for bond strength and sample size number purposes. Unless otherwise specified, for conditions F, G, and H the sample size number specified shall determine the number of die to be tested (not bonds). For multichip devices (all conditions), a minimum of 4 die or use all die if four are not available on a minimum of 2 completed devices shall be used. Where there is any adhesive, encapsulant or other material under, on or surrounding the die such as to increase the apparent bond strength, the bond strength test shall be performed prior to application.

When flip chip or beam-lead chips are bonded to substrates other than those in completed devices, the following conditions shall apply:

a. The sample of chips for this test shall be taken at random from the same chip population as that used in the completed devices that they are intended to represent.

b. The chips for this test shall be bonded on the same bonding apparatus as the completed devices, during the time period within which the completed devices are bonded.

c. The test chip substrates shall be processed, metallized, and handled identically with the completed device substrates, during the same time period within which the completed device substrates are processed.

3.1 Test conditions:

3.1.1 Test condition A - Bond peel. This test is normally employed for bonds external to the device package. The lead or terminal and the device package shall be gripped or clamped in such a manner that a peeling stress is exerted with the specified angle between the lead or terminal and the board or substrate. Unless otherwise specified, an angle of 90 degrees shall be used. When a failure occurs, the force causing the failure and the failure category shall be recorded.

3.1.2 Test condition C - Wire pull (single bond). This test is normally employed for internal bonds at the die or substrate and the lead frame of microelectronic devices. The wire connecting the die or substrate shall be cut so as to provide two ends accessible for pull test. In the case of short wire runs, it may be necessary to cut the wire close to one termination in order to allow pull test at the opposite termination. The wire shall be gripped in a suitable device and simple pulling action applied to the wire or to the device (with the wire clamped) in such a manner that the force is applied approximately normal to the surface of the die or substrate. When a failure occurs, the force causing the failure and the failure category shall be recorded.

3.1.3 Test condition D - Wire pull (double bond). This procedure is identical to that of test condition C, except that the pull is applied by inserting a hook under the lead wire (attached to die, substrate or header or both ends) with the device clamped and the pulling force applied approximately in the center of the wire in a direction approximately normal to the die or substrate surface or approximately normal to a straight line between the bonds. When a failure occurs, the force causing the failure and the failure category shall be recorded. The minimum bond strength shall be taken from table I. Figure 2037.1-1 may be used for wire diameters not specified in table I. For wire diameter or equivalent cross section >0.005 inch, where a hook will not fit under the wire, a suitable clamp can be used in lieu of a hook.

3.1.4 Test condition F - Bond shear (flip chip). This test is normally employed for internal bonds between a semiconductor die and a substrate to which it is attached in a face-bonded configuration. It may also be used to test the bonds between a substrate and an intermediate carrier or secondary substrate to which the die is mounted. A suitable tool or wedge shall be brought in contact with the die (or carrier) at a point just above the primary substrate and a force applied perpendicular to one edge of the die (or carrier) and parallel to the primary substrate, to cause bond failure by shear. When a failure occurs, the force at the time of failure, and the failure category shall be recorded.

3.1.5 Test condition G - Push-off test (beam lead). This test is normally employed for process control and is used on a sample of semiconductor die bonded to a specially prepared substrate. Therefore, it cannot be used for random sampling of production or inspection lots. A metallized substrate containing a hole shall be employed. The hole appropriately centered, shall be sufficiently large to provide clearance for a push tool, but not large enough to interfere with the bonding areas. The push tool shall be sufficiently large to minimize device cracking during testing, but not large enough to contact the beam leads in the anchor bond area. Proceed with push-off tests as follows: The substrate shall be rigidly held and the push tool inserted through the hole. The contact of the push tool to the silicon device shall be made without appreciable impact (less than 0.01 inch/minute (0.254 mm/minute) and forced against the underside of the bonded device at a constant rate. When failure occurs, the force at the time of failure, and the failure category shall be recorded.

3.1.6 Test condition H - Pull-off test (beam lead). This test is normally employed on a sample basis on beam lead devices which have been bonded down on a ceramic or other suitable substrate. The calibrated pull-off apparatus (see 2) shall include a pull-off rod (for instance, a current loop of nichrome or Kovar wire) to make connection with a hard setting adhesive material (for instance, heat sensitive polyvinyl acetate resin glue) on the back (top side) of the beam lead die. The substrate shall be rigidly installed in the pull-off fixture and the pull-off rod shall make firm mechanical connection to the adhesive material. The device shall be pulled within 5 degrees of the normal to at least the calculated force (see 3.2), or until the die is at 2.54 mm (0.10 inch) above the substrate. When a failure occurs, the force at the time of failure, the calculated force limit, and the failure category shall be recorded.

3.2 Failure criteria. Any bond pull which results in separation under an applied stress less than that indicated in table I as the required minimum bond strength for the indicated test condition, composition, and construction shall constitute a failure.

3.2.1 Failure category. Failure categories are as follows: When specified, the stress required to achieve separation and the category of separation or failure shall be recorded.

a. For internal wire bonds:

(a-1) Wire break at neckdown point (reduction of cross section due to bonding process).

(a-2) Wire break at point other than neckdown.

(a-3) Failure in bond (interface between wire and metallization) at die.

(a-4) Failure in bond (interface between wire and metallization) at substrate, package post, or other than die.

(a-5) Lifted metallization from die.

(a-6) Lifted metallization from substrate or package post.

(a-7) Fracture of die.

(a-8) Fracture of substrate.

b. For external bonds connecting device to wiring board or substrate:

(b-1) Lead or terminal break at deformation point (weld affected region).

(b-2) Lead or terminal break at point not affected by bonding process.

(b-3) Failure in bond interface (in solder or at point of weld interface between lead or terminal and the board or substrate conductor to which the bond was made).

(b-4) Conductor lifted from board or substrate.

(b-5) Fracture within board or substrate.

c. For flip-chip configurations:

(c-1) Failure in the bond material or pedestal, if applicable.

(c-2) Fracture of die (or carrier) or substrate (removal of portion of die or substrate immediately under the bond).

(c-3) Lifted metallization (separation of metallization or bonding pedestal from die (or carrier) or substrate.

d. For beam lead devices:

(d-1) Silicon broken.

(d-2) Beam lifting on silicon.

(d-3) Beam broken at bond.

(d-4) Beam broken at edge of silicon.

(d-5) Beam broken between bond and edge of silicon.

(d-6) Bond lifted.

(d-7) Lifted metallization (separation of metallization) from die, separation of bonding pad.

(d-8) Lifted metallization.

NOTE: RF/microwave that require extremely flat loops which may cause erroneous wire pull data may use the following formula to determine the proper wire pull value.

$V_1 = V_2 \sin \theta$

Where: V_1 = New value to pull test.
V_2 = Table I value for size wire tested.
θ = Greatest calculated wire loop angle (figure 2037.1-2).

Also, RF/microwave that contain wires that cannot be accessed with a pull hook must be duplicated on a test coupon in such a way to allow hook access for purposes of pull testing. These wires are to be bonded at the same time the production devices are bonded using the same setup, operator, and schedule. The test wires are to be pull tested in lieu of the tuning or inaccessible wires on the production devices. Failures on the test coupon shall be considered as failures to production units and appropriate action is to be taken in accordance with the applicable specification (figure 2037.1-3).

TABLE I. Minimum bond strength.

Test condition	Wire composition and diameter 1/	Construction 2/	Minimum bond strength (grams force)	
			Pre seal	Post seal and any other processing and screening when applicable
A	---	---	Given in applicable document	Given in applicable document
C or D	AL 0.0007 in AU 0.0007 in	Wire	1.5 2.0	1.0 1.5
C or D	AL 0.0010 in AU 0.0010 in	Wire	2.5 3.0	1.5 2.5
C or D	AL 0.00125 in AU 0.00125 in	Wire	Same bond strength limits as the 0.0013 in wire	
C or D	AL 0.0013 in AU 0.0013 in	Wire	3.0 4.0	2.0 3.0
C or D	AL 0.0015 in AU 0.0015 in	Wire	4.0 5.0	2.5 4.0
C or D	AL 0.0030 in AU 0.0030 in	Wire	12.0 15.0	8.0 12.0
F	Any	Flip-clip	5 grams-force x number of bonds (bumps)	
G or H	Any	Beam lead	30 grams force in accordance with linear millimeter of nominal undeformed (before bonding) beam width. 3/	

1/ For wire diameters not specified, use the curve of figure 2037.1-1 to determine the bond pull limit.
2/ For ribbon wire, use the equivalent round wire diameter which gives the same cross-sectional area as the ribbon wire being tested.
3/ For condition G or H, the bond strength shall be determined by dividing the breaking force by the total of the nominal beam widths before bonding.

4. SUMMARY. The following details shall be specified in the applicable acquisition document:

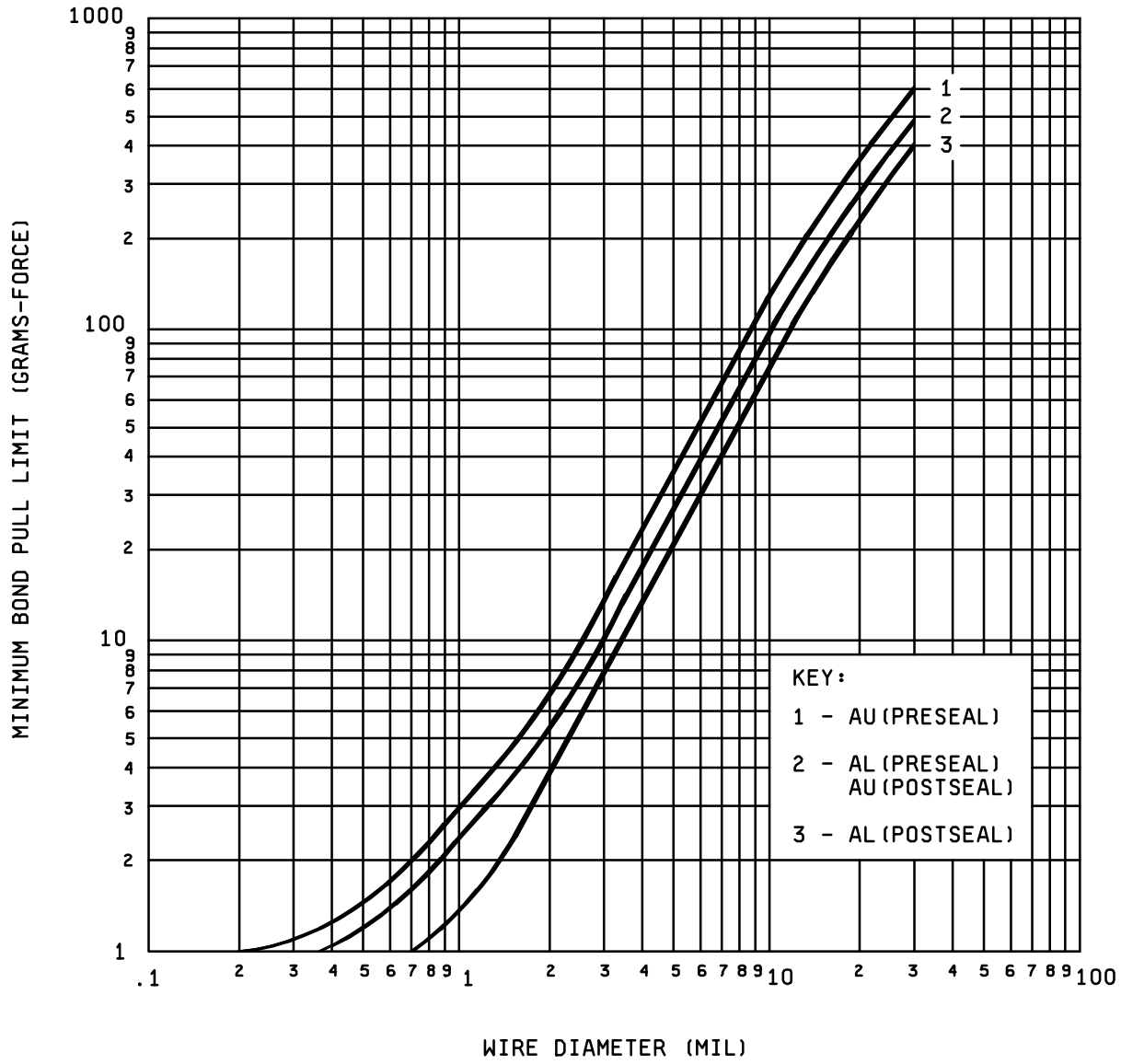
a. Test condition letter (see 3).

b. Minimum bond strength if other than specified in 3.2 or details of required strength distributions if applicable.

c. Sample size number and accept number or number and selection of bond pulls to be tested on each device, and number of devices, if other than 4.

d. For test condition A, angle of bond peel if other than 90°, and bond strength limit (see 3.2).

e. Requirement for reporting of separation forces and failure categories, when applicable (see 3.2.1).



NOTE: The minimum bond strength should be taken from table I. Figure 2037.1-1 may be used for wire diameters not specified in table I.

FIGURE 2037.1-1 Minimum bond pull limits.

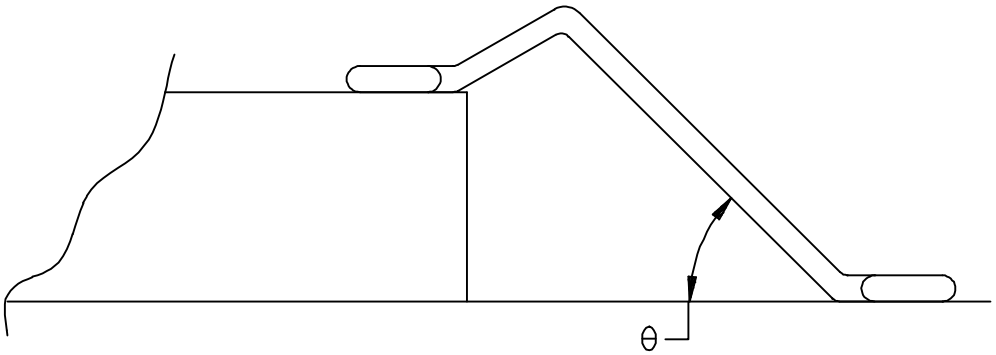


FIGURE 2037.1-2 Wire loop angle.

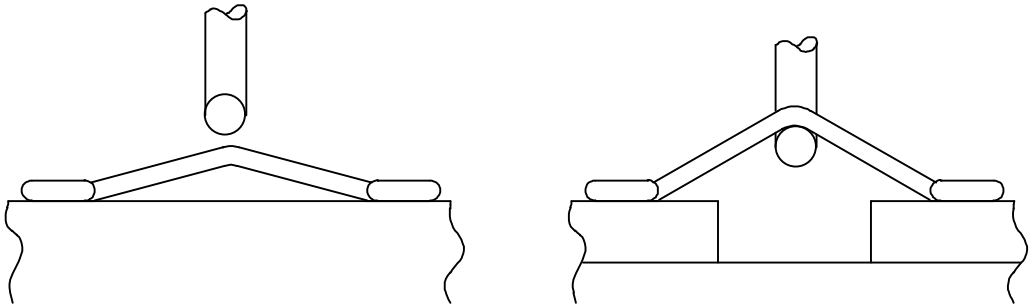


FIGURE 2037.1-3 Flat loop wire pull testing.

METHOD 2052.3

PARTICLE IMPACT NOISE DETECTION (PIND) TEST

1. Purpose. The purpose of this test is to detect loose particles inside a device cavity. The test provides a nondestructive means of identifying those devices containing particles of sufficient mass that, upon impact with the case, excite the transducer.

2. Apparatus. The equipment required for the PIND test shall consist of the following (or equivalent):

a. A threshold detector to detect particle noise voltage exceeding a preset threshold of the absolute value of 20 ±1 mV peak reference to system ground.

b. A vibration shaker and driver assembly capable of providing essentially sinusoidal motion to the DUT at:

(1) Condition A: 20 g's peak at 40 to 250 Hz.

(2) Condition B: 10 g's peak at 60 Hz minimum.

c. PIND transducer, calibrated to a peak sensitivity of -77.5 ±3 dB in regards to one volt per microbar at a point within the frequency of 150 to 160 kHz.

d. A sensitivity test unit (STU) (see figure 2052-1) for periodic assessment of the PIND system performance. The STU shall consist of a transducer with the same tolerances as the PIND transducer and a circuit to excite the transducer with a 250 microvolt ±20 percent pulse. The STU shall produce a pulse of about 20 mV peak on the oscilloscope when the transducer is coupled to the PIND transducer with attachment medium.

e. PIND electronics, consisting of an amplifier with a gain of 60 ±2 dB centered at the frequency of peak sensitivity of the PIND transducer. The noise at the output of the amplifier shall not exceed 10 mV peak.

f. Attachment medium. The attachment medium used to attach the device under test (DUT) to the PIND transducer shall be the same attachment medium as used for the STU test.

g. Shock mechanism or tool capable of imparting shock pulses of 1,000 ±200 g's peak to the DUT. The duration of the main shock shall not exceed 100 μs. If an integral co-test shock system is used the shaker vibration may be interrupted or perturbed for period of time not to exceed 250 ms from initiation of the last shock pulse in the sequence. The co-test duration shall be measured at the 50 ±5 percent point.

3. Procedures.

*3.1 Test equipment setup. Shaker drive frequency and amplitude shall be adjusted to the specified conditions based on cavity size of the DUT (see figure 2052-2). For packages smaller than 40 Mils (1.02 mm), the following formula shall be used to calculate the shaker drive frequency:

$G = 0.0511 \times F^2 \times D$ where G = acceleration in gravity units
F = frequency in Hz
D = displacement pk-pk in inches (cavity size)

The approximate average internal package height shall be measured from the floor of the package cavity or the top of the major substrate for applicable assemblies and shall exclude the thickness of the die mounted inside the package. The shock pulse shall be adjusted to provide 1,000 ±200 g's peak to the DUT.

3.2 Test equipment checkout. The test equipment checkout shall be performed a minimum of one time per operation shift. Failure of the system to meet checkout requirements shall require retest of all devices tested subsequent to the last successful system checkout.

3.2.1 Shaker drive system checkout. The drive system shall achieve the shaker frequency and the shaker amplitude specified. The drive system shall be calibrated so that the frequency settings are within ±8 percent and the amplitude vibration setting are within ±10 percent of the nominal values. If a visual displacement monitor is affixed to the transducer, it may be used for amplitudes between .04 and .12 inch (1.02 and 3.05 mm). An accelerometer may be used over the entire range of amplitudes and shall be used below amplitudes of .040 inch (1.02 mm).

3.2.2 Detection system checkout. With the shaker deenergized, the STU transducer shall be mounted face-to-face and coaxial with the PIND transducer using the attachment medium used for testing the devices, prior to attaching any special fixtures. The STU shall be activated several times to verify low level signal pulse visual and threshold detection on the oscilloscope. Not every application of the STU will produce the required amplitude. All pulses which are greater than 20 mV shall activate the detector.

3.2.3 System noise verification. System noise will appear as a fairly constant band and must not exceed 20 mV peak to peak when observed for a period of 30 to 60 seconds.

3.3 Test sequence. The following sequence of operations (a. through i.) constitute one test cycle or run.

a. Three pre-test shocks.

b. Vibration 3±1 seconds.

c. Three co-test shocks.

d. Vibration 3±1 seconds.

e. Three co-test shocks.

f. Vibration 3±1 seconds.

g. Three co-test shocks.

h. Vibration 3±1 seconds.

i. Accept or reject.

*3.3.1 Mounting requirements. Special precautions (e.g., in mounting, grounding of DUT leads, or grounding of test operator) shall be taken as necessary to prevent electrostatic damage to the DUT. Batch testing is prohibited.

Most part types will mount directly to the transducer via the attachment medium. Parts shall be mounted with the thinnest walled surface against the transducer at the center or axis of the transducer for maximum sensitivity. An alternate mounting method, that optimizes the capture rate, can be used. In any case, the procedure shall be documented and approved by Qualifying Activity. Centering is critical and a reasonable tolerance shall be exercised and documented for each package family. Parts with unusual shapes may require special fixtures. Such fixtures shall have the following properties:

(1) Low mass.
(2) High acoustic transmission (aluminum alloy 7075 works well).
(3) Full transducer surface contact, especially at the center.
(4) Maximum practical surface contact with test part.
(5) No moving parts.
(6) Suitable for attachment medium mounting.

3.3.2 Test monitoring. Each test cycle (see 3.3) shall be continuously monitored, except for the period during co-test shocks and 250 ms maximum after the shocks. Particle indications can occur in one or any combination of the three detection systems as follows:

a. Visual indication of high frequency spikes which exceed the normal constant background white noise level.

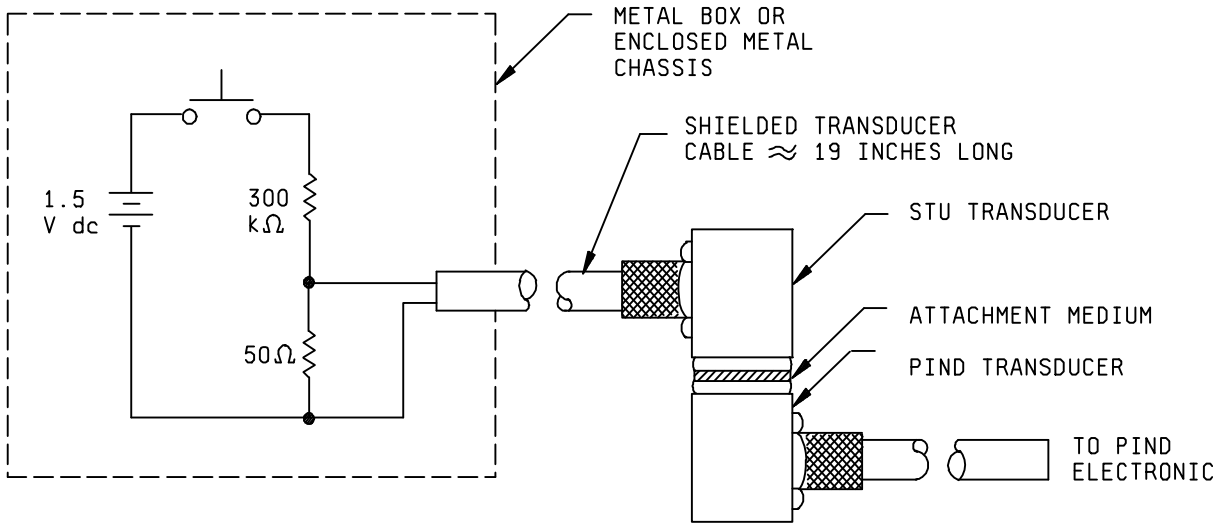
b. Audio indication of clicks, pops, or rattling which is different from the constant background noise present with no DUT on the transducer.

c. Threshold detection shall be indicated by the lighting of a lamp or by deflection of the secondary oscilloscope trace.

3.4 Failure criteria. Any noise bursts as detected by any of the three detection systems exclusive of background noise, except those caused by the shock blows, during the monitoring periods shall be cause for rejection of the device. Rejects shall not be retested except for retest of all devices in the event of test system failure. If additional cycles of testing on a lot are specified, the entire test procedure (equipment setup and checkout mounting, vibration, and co-shocking) shall be repeated for each retest cycle. Reject devices from each test cycle shall be removed from the lot and shall not be retested in subsequent lot testing.

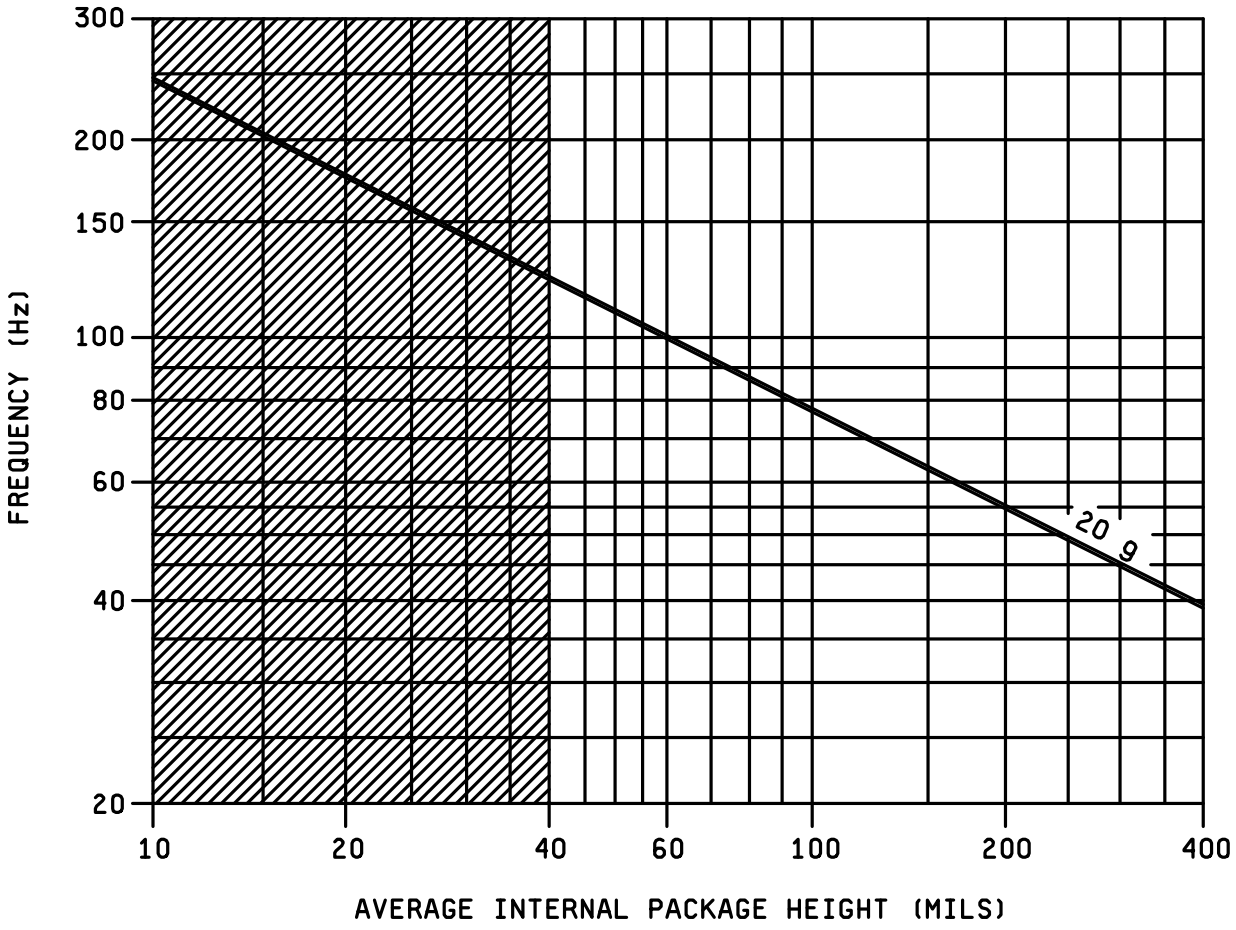
4. Summary. The following details shall be specified in the applicable detail specification:

a. Test condition letter A or B.
b. Lot acceptance/rejection criteria (if applicable).
c. The number of test cycles, if other than one.
d. Pre-test shock level and co-test shock level, if other than specified.



NOTES:
Pushbutton switch: Mechanically quiet, fast make, gold contacts. E.G. T2 SM4 microswitch.
Resistance tolerance five percent noninductive.
Voltage source can be a standard dry cell.
The coupled transducers must be coaxial during test.
Voltage output to STU transducer 250 microvolts, ±20 percent.

FIGURE 2052-1. Typical STU.



NOTE: Formula applies to shaded area (see 3.1)

Figure 2052-2. Package height versus test frequency for 20 g's acceleration.

METHOD 2070.2

PRE-CAP VISUAL
MICROWAVE DISCRETE AND MULTICHIP TRANSISTORS

1. Purpose. The purpose of this inspection is to verify the construction and quality of workmanship in wafer, wafer dc testing, die inspection, and assembly processes to the point of pre-cap inspection. These various inspections and tests are intended to detect and remove transistor die with defects that could lead to device failure during application and to verify compliance with the requirements of the applicable detail specification.

2. Apparatus. The apparatus for this inspection shall consist of the following:

a. Optical equipment capable of the specified magnifications, and both normal incident and darkfield lighting.

b. Adequate fixturing for handling the devices being inspected without causing damage.

c. Adequate covered storage and transportation containers to protect devices from mechanical damage and environmental contamination.

d. Any visual standards (e.g., drawings, photographs) necessary to enable the inspector to make objective decisions as to the acceptability of devices being inspected.

*2.1 Microwave Devices. GaAs devices shall be inspected to all applicable criteria as listed herein. GaAs microwave devices shall also have additional specific criteria as listed and the applicable high power magnification for individual features of GaAs microwave devices shall be selected from the following table."

Table I GaAs microwave device high magnification requirements

Feature Dimensions	Magnification Range
> 5 microns	75 - 150X
1 - 5 microns	150 - 400X
< 1 micron	400 - 1000X

3. Procedure.

*3.1 General. The devices shall be examined in a suitable sequence of observations with the specified magnification range to determine compliance with the requirements of this document and the applicable detail specification.

a. Sequence of inspection. The order in which criteria are presented is not a required order of inspection and may be varied at the discretion of the manufacturer.

b. Inspection control. Within the time interval between visual inspection and preparation for sealing, devices shall be stored in a controlled environment (an environment in which air-borne particles and relative humidity are controlled). The use of a positive pressure inert gas environment, such as dry nitrogen, shall satisfy the requirement of storing in a controlled environment. Unless a cleaning operation is performed prior to sealing, devices inspected in accordance with this specification shall be inspected in a class 100,000 environment in accordance with FED-STD-209. The maximum allowable relative humidity shall not exceed 05 percent. Devices shall be in clean covered containers when transferred through any uncontrolled environment.

c. Magnification. High magnification inspection shall be performed perpendicular to the die surface with normal incident or darkfield illumination as required. Low magnification inspection shall be performed with either a monocular, binocular, or stereo microscope and the inspection performed with any appropriate angle, with the device under suitable illumination. High magnification may be used to verify a discrepancy which has first been noted at low magnification.

(1) High magnification inspection shall be performed within the range of 00X to 200X.

(2) Low magnification shall be performed within the range of 30X to 00X.

d. General reject criteria: Unless otherwise specified, reject if the defect is present in 25 percent of any one cell or in 10 percent of the entire die.

e. Figures 2070-5 through 2070-9 illustrate different geometries used in fabricating microwave discrete transistors.

*3.2 Wafer inspection. Not applicable

3.2.1 Metallization inspection. Unless otherwise specified, the 25 percent of a cell and 10 percent of a die reject conditions apply). No die shall be acceptable which exhibits any of the following defects:

a. Metallization misalignment so that there is less than 75 percent coverage of the ohmic contact windows.

b. Contact window that has less than a continuous 50 percent of its perimeter covered by metallization. NOTE: Metal coverage is not required at the far dielectric steps of the end base contacts under base metal finger tips.

c. Metal must cover 50 percent of the contact that lies over the enhancement area.

d. Metallization bridging, between two normally unconnected metallization paths, which reduces the design separation to less than 50 percent or 0.1 mil whichever is less.

e. Metallization corrosion. Any metallization which shows evidence of corrosion.

f. Metallization adherence. Any metallization which has lifted, peeled, or blistered.

g. Exception: Do not reject for missing or defective run around metal (run around metal is nonactive metal used for probing purposes with multicell devices).

3.2.2 Glassivation and silicon nitride defects. (Unless otherwise specified, the 25 percent of a cell and 10 percent of a die reject conditions apply). No die shall be acceptable which exhibits any of the following defects:

a. Glass crazing that prohibits the detection of voids or scratches during subsequent inspection or that covers more than 25 percent of the die area.

b. Any glassivation which has delaminated.

c. Two or more adjacent active metallization paths which are not covered by glassivation, except by design.

d. Unglassivated areas at the edge of bonding pads which expose silicon.

e. Glassivation which covers more than 25 percent of the designed bonding pad area.

f. Glass crazing covering more than 25 percent of the die area.

g. Glass cracks which form closed loops over adjacent metallization paths.

3.3 Die metallization defects (high magnification). No die shall be acceptable which exhibits any of the following defects.

3.3.1 Metallization scratches and voids exposing underlying material (see figure 2070-1). Unless otherwise specified, the 25 percent of a cell and 10 percent of a die conditions apply.

a. A scratch or void that severs the innermost metallized guard ring.

b. Any die containing a void in the metallization at the bonding pad covering more than 25 percent of the pad area (see figure 2070-1).

c. For all devices with expanded contacts. A scratch whether or not underlying material is exposed or a void, which leaves less than 50 percent undisturbed metal width in the metal connecting the pad and the contact regions.

d. For expanded contacts with more than 10 contact regions. A scratch or void extending across more than 50 percent of the first half of any contact region (beginning at the bonding area) in more than 10 percent of the contact regions.

e. For expanded contacts with less than 10 contact regions. A scratch or void in the contact area which isolates more than 10 percent of the contact regions.

f. Metallization probing. Criteria contained in 3.3.1b shall apply as limitation on probing damage.

3.4 Scribing and die defects (high magnification). No device shall be acceptable which exhibits any of the following defects (see figure 2070-2):

a. Unless by design, less than 0.1 mil passivation visible between active metallization or bond pad periphery and the edge of the die.

b. Any chip-out or crack in the active area.

c. Any crack which exceeds 2.0 mils in length beyond the scribe grid or line that points toward active metallization or an active area.

d. Any chip-out that extends to within 1.0 mil of an active area or to within 50 percent of the design spacing, whichever is less.

e. Any crack or chip-out that extends under any active metallization.

f. Reject if more than 25 percent of a depletion ring is missing. A depletion ring encompasses an individual cell. An annular ring encompasses the entire die. A true annular ring will be the same color as the emitter.

3.5 Bonding inspection (low magnification). This inspection and criteria shall be the required inspection for the bond types and locations to which they are applicable when viewed from above (see figures 2070-3 and 2070-4). (Wire tail is not considered part of the bond when determining physical bond dimensions.) No device shall be acceptable which exhibits any of the following defects.

3.5.1 Gold ball bonds

a. Gold ball bonds where the ball bond diameter is less than 2.0 times or greater than 5.0 times the bonding wire diameter.
b. Gold ball bonds where the wire exit is not completely within the periphery of the ball.
c. Gold ball bonds where the exiting wire is not within boundaries of the bonding pad.
d. Any visible intermetallic formation at the periphery of any gold ball bond.

3.5.2 Wedge bonds.

a. Aluminum wire: Ultrasonic/thermasonic wedge bonds that are less than 1.2 times or greater than 3.0 times the wire diameter in width, or less than 1.5 times or greater than 3.0 times the wire diameter in length.

b. Gold wire: Ultrasonic/thermasonic wedge bonds that are less than 1.0 times or greater than 3.0 times the wire diameter in width, or less than 0.5 times or greater than 3.0 times the wire diameter in length.

c. Thermocompression wedge bonds that are less than 1.2 times or greater than 3.0 times the wire diameter in width or are less than 0.5 times or greater than 3.0 times the wire diameter in length.

3.5.3 Tailless bonds (crescent).

a. Tailless bonds that are less than 1.2 times or greater than 5.0 times the wire diameter in width, or are less than 0.5 times or greater 3.0 times the wire diameter in length.

b. Tailless bonds where the bond impression does not cover the entire width of the wire.

3.5.4 General (gold ball, wedge, and tailless). As viewed from above, no device shall be acceptable which exhibits any of the following defects:

a. Bonds on the die where less than 50 percent of the bond is within the unglassivated bonding pad area.

b. Wire bond tails that extend over and make contact with any metallization not covered by glassivation and not connected to the wire.

c. Wire bond tails that exceed two wire diameters in length at the die bonding pad or four wire diameters in length at the package or post.

d. Bonds on the package post that are not bonded entirely on the flat surface of the post top.

e. A bond on top of another bond, bond wire tail, or residual segment of lead wire. An ultrasonic wedge bond alongside a previous bond where the observable width of the first bond is reduced less than .25 mil is considered acceptable.

f. Bonds placed so that the separation between bond and adjacent unglassivated die metallization not connected to it is less than 1.0 mil, except if the glass does not exhibit cracking, the separation may be 0.1 mil.

g. Rebonding shall be permitted with the following limitations:

(1) No scratched, open, or discontinuous metallization paths or conductor patterns shall be repaired by bridging with or addition of bonding wire or ribbon.

(2) All rebonds shall be placed on at least 50 percent undisturbed metal (excluding probe marks that do not expose oxide) and no more than one rebond attempt at any design bond location shall be permitted at any pad or post and no rebonds shall touch an area of exposed oxide caused by lifting metal.

(3) The total number of rebond attempts shall be limited to a maximum of 10 percent of the total number of bonds in the device. The 10 percent limit on rebonds may be interpreted as the nearest whole number of bonds in the device. A bond shall be defined as a wire to post or wire to bond pad. Bond-offs required to clear the bonder after an unsuccessful first bond attempt need not be considered as rebonds provided they can be identified as bond-offs by being made physically away from normal bond areas. The initial bond attempt need not be visible. A replacement of one wire at one end or an unsuccessful bond attempt at one end of the wire counts as one rebond; a replacement of wire bonded at both ends, or an unsuccessful bond attempt of a wire already bonded at the other end, counts as two rebonds.

h. Gold bonds where less than 50 percent of the bond is located within an area that is free of eutectic melt. The blush area shall not be considered part of the eutectic melt (The blush area is defined as the area where a color change can be seen but not a change in surface texture).

3.5.5 Internal lead wires. This inspection and criteria shall be required inspection for the locations to which they are applicable when viewed from above. No device shall be acceptable that exhibits any of the following defects:

a. Any wire that comes closer than one wire diameter to unglassivated operating metallization, another wire (common wires excluded), package post, unpassivated die area of opposite polarity, or any portion of the package of opposite polarity including the plane of the lid to be attached (except by design, but in no case should the separation be less than .25 mil). (Within a 5.0 mil spherical radial distance from the perimeter of the bond on the die surface, the separation shall be greater than 1.0 mil.)

b. Nicks, tears, bends, cuts, crimps, scoring, or neckdown in any wire that reduces the wire diameter by more than 25 percent, except in bond deformation area.

c. Missing or extra lead wires.

d. Bond lifting or tearing at interface of pad and wire.

e. Any wire which runs from die bonding pad to package post and has no arc or stress relief.

f. Wires which cross other wires, except common connectors, except by design, in which case the clearance shall be 1.0 mil minimum.

g. Wires not in accordance with bonding diagram (unless allowed in design documentation, for tuning purposes).

h. Kinked wires (an unintended sharp bend) with an interior angle of less than 90° or twisted wires to an extent that stress marks appear.

i. Wire (ball bonded devices) not within 10° of the perpendicular to the surface of the chip for a distance of greater than 0.5 mil before bending toward the package post or other termination point.

3.6 Package conditions (low magnification). No device shall be acceptable which exhibits any of the following defects.

3.6.1 Foreign material on die surface. All foreign material or particles may be blown off with a nominal gas blow (approximately 20 psi (138 kPa)) or removed with a soft camel hair brush. The device shall then be inspected for the following criteria:

a. Loosely attached conductive particles (conductive particles which are attached by less than one-half of their largest dimension) that are large enough to bridge the narrowest unglassivated active metal spacing (silicon chips or any opaque material shall be included as conductive particles).

b. Liquid droplets, chemical stains, or photoresist on the die surface that bridge any combination of unglassivated metallization or bare silicon areas, except for unused cells.

c. Ink on the surface of the die that covers more than 25 percent of a bonding pad area (or interferes with bonding) or that bridges any combination of unglassivated metallization or bare silicon areas, except for unused cells.

d. Any entrapped opaque material which appears to extend over metallization.

3.6.2 Die mounting.

a. Die to header mounting material which is not visible around at least three sides or 75 percent of the die perimeter. Wetting criteria is not required if the devices pass an approved die attached evaluation test.

b. Any balling of the die mounting material which does not exhibit a fillet when viewed from above.

c. Any flaking of the die mounting material.

d. Any die mounting material which extends onto the die surface beyond the scribe zone and comes closer than 0.5 mil to any active area or metallization, or extends vertically above the top surface of the die and interferes with bonding.

3.6.3 Die orientation.

a. A die which is not oriented or located in accordance with the applicable assembly drawing of the device.

b. Die is visibly tipped or tilted (more than 10°) with respect to the die attach surface.

3.6.4 Internal package defects (applicable to headers, bases, caps, and lids). As an alternative to 100 percent visual inspection, the lids or caps may be subjected to a suitable cleaning process and quality verification procedure approved by the qualifying activity, provided the lids or caps are subsequently held in a controlled environment until capping or preparation for seal.

a. Any header or post plating which is blistered.

b. Any conductive particle which is attached by less than one-half of the longest dimension.

c. For isolated heat sink packages:

(1) Any defect or abnormality causing the designed isolating paths between the metal islands to be reduced to less than 50 percent of the design separation or reduced to 0.2 mil, whichever is less.

(2) A crack in the substrate.

3.6.5 Carrier defects ((e.g., BeO, alumina) substrate).

a. Any chip-out in the carrier material.

b. Carrier metallization which is smeared or is obviously not uniform in metallization design pattern to the extent that there is less than 50 percent of the original design separation, or 0.5 mil whichever is less, between operating pads, paths, lid mounting metallization, edges, or any combination thereof.

c. Any crack in the BeO or operating metallization that would affect hermetic seal or die mounting metallization. (Tooling marks or cold form interface lines are not cracks and are not cause for rejection.)

d. Any metallization lifting, peeling, or blistering (on the carrier surface).

e. Any attached conductive foreign material which bridges any combination of metallization paths, leads, or active circuit elements.

f. A scratch or void in the metallization which exposes the substrate anywhere along its length and leaves less than 75 percent of the original metal width undisturbed. NOTE: Occasionally package metallization is intentionally burnished or scratched, in areas which require wire bond attachment, to improve surface bondability; such conditions are not cause for rejection. Burnished or scratched areas must satisfy the criteria of 3.0.4b.

g. Excessive scratches in carrier metallization due to abuse in handling or processing.

h. Any staple, bridge, or clip with solder joint which exhibits less than 50 percent wetting around the section that is attached to the package.

i. Any header posts which are not perpendicular within 10° of the horizontal plane of the header.

j. Any lead attach eutectic or solder which extends across greater than 50 percent of the design separation gap between metallization pads.

3.7 Capacitor defects (high magnification).

a. Scratches through the metal that extend the length of the metal and expose underlying oxide.

b. Any metallization peeling (except due to bond tail pull).

c. Any metallization which shows evidence of corrosion.

d. Cracks in the silicon that point toward the metal and are within 1 mil of the metal (except for ground bar portion).

e. Chip-outs within 0.5 mil of the metal (except for ground bar portion).

f. Metal that has been gouged or probed over 20 percent of a bonding pad area and exposes underlying oxide.

g. Mounting material which is not visible around at least three sides or 75 percent of the capacitor perimeter. Wetting criteria is not required if the devices pass an approved capacitor attach evaluation test. (This inspection is to be performed at low magnification.)

NOTE: Multiple bonding is allowable for tuning purposes, however initial bond wire shall be completely removed before rebonding and must be in accordance with design documentation.

3.8 Alignment (This applies to 25 percent of any one cell or 10 percent of any die). Reject any diffusion line which touches another diffusion line, except for contact enhancements, which can touch an active area of the same type. Emitter contacts can touch emitter base junction but cannot cross. Base contacts must engage 50 percent or more of the contact enhancement.

NOTE: Contacts are not diffused.

3.9 Resistors (criteria applies to 25 percent of any one cell or 10 percent of any die.

Process level	Defect	Reject
NICR resistor	Pinched	Resistor is less than 90 percent of its intended design width.
	Undercutting	Resistor is less than 75 percent of its intended design width.
	Bridging or excess NICR	Bridging between discrete resistor pattern.
Diffused resistors	Oxide defects Poor definitions	No visible opening.
	Misalignment	Contacting less than 90 percent of its intended design width.
	Undercutting	Resistor less than 75 percent of its intended design width.
	Over etched	Resistor is greater than 125 percent of its intended design width.
Poly SI resistor	Pinched	Resistor is less than 90 percent of its intended design width.
Poly SI resistor	Undercut	Resistor is less than 75 percent of its intended design width.
	Bridging or excess poly SI	Bridging between discrete resistor pattern.
	Misalignment	Contacting less than 75 percent of the design separation.

Reject if 25 percent of any one cell or 10 percent of any die exhibits burned or missing resistors.

3.9.1 NICR resistor. Thin film deposited and patterned usually connecting emitter fingers to emitter feed metal to control current. It can also be used as a passive element in RF IC's.

3.9.2 Poly SI resistors (bevel). Thin film of poly SI is deposited, doped, and patterned usually connecting emitter fingers to emitter feed metal to control current. It can also be used as passive elements in RF IC's.

3.9.3 Diffused resistors (contact appearance). A diffused area connecting emitter fingers to emitter feed metal used to control current.

3.9.4 Contacts and diffusion defects (contacts are not diffused). Reject if contacts are less than 50 percent of design on 10 percent of the die. Reject any die that has a discontinuous implant or diffusion line effecting more than 10 percent of the die. A discontinuous line is a line that wanders but does not close on itself. Reject any die where an implant or diffusion fault bridges between two diffuse areas, any two metallized stripes of any combination not intended by design. This must effect greater than 10 percent of the die. Reject any implant or diffused area that is less than 50 percent of design.

3.9.5 Passivation or oxide defects. This applies to 25 percent of a cell and 10 percent of the die. Reject any active junction not covered by passivation or glassivation. Reject for absence of passivation or oxide visible at the edge and continuing under the metallization causing a short between the metal and the underlying material (unless by design). Reject for passivation or oxide defects that allows bridging between any two metallized stripes.

4. Summary. The following details shall be specified in the applicable detail specification:

a. Exceptions or additions to the inspection method.

b. Where applicable, any conflicts with approved circuit design topology or construction.

c. Where applicable, gauges, drawings, and photographs that are to be used as standards for operator comparison.

d. When applicable, specific magnification.

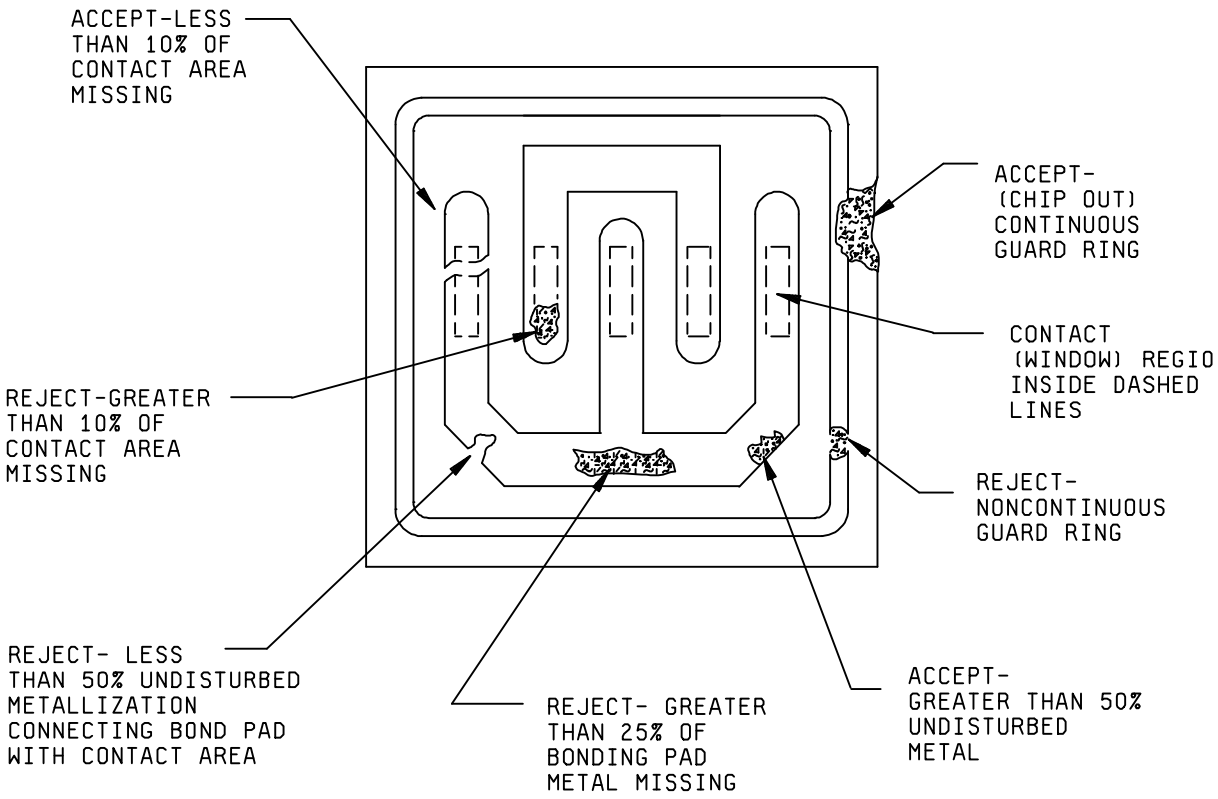
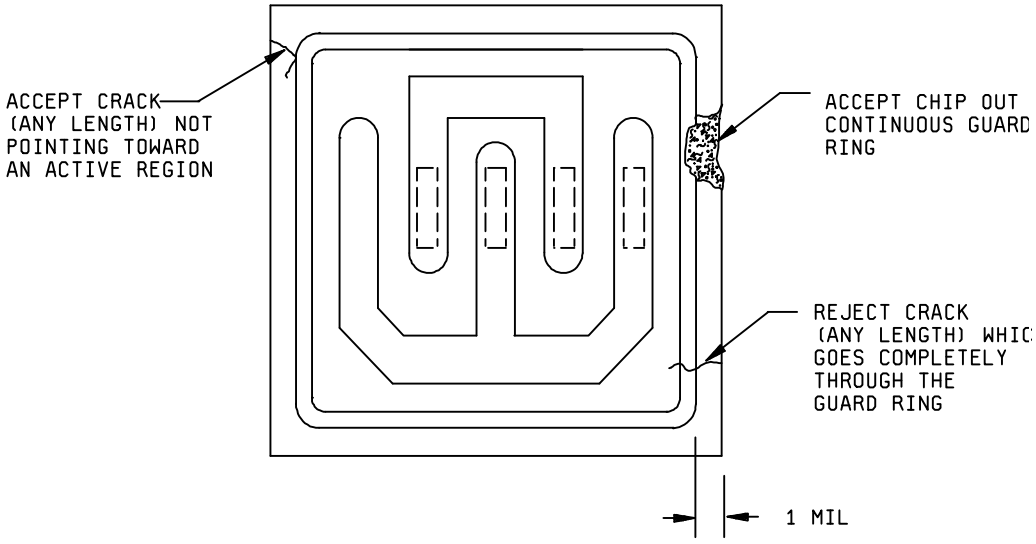
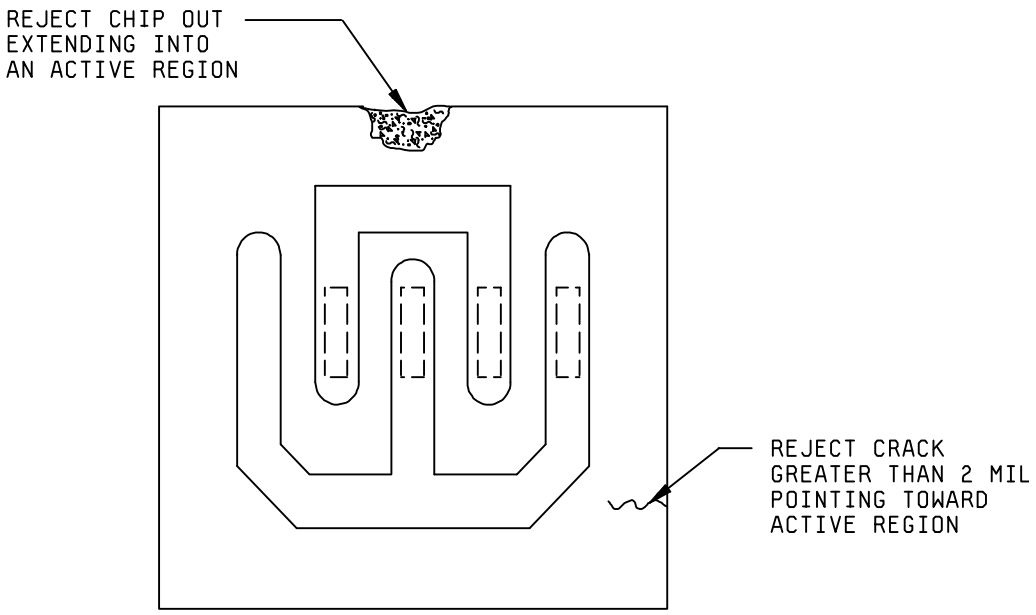


FIGURE 2070-1. Metallization scratches and voids (expanded contact).

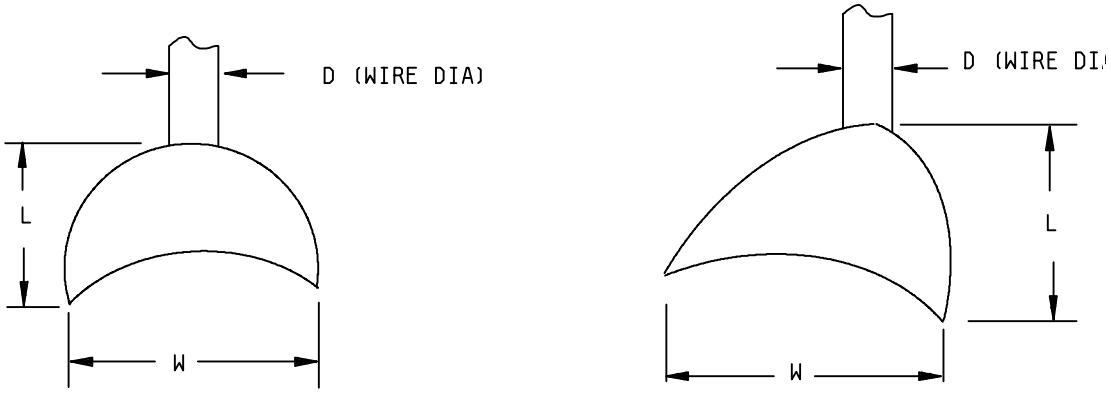


Die with guard ring.



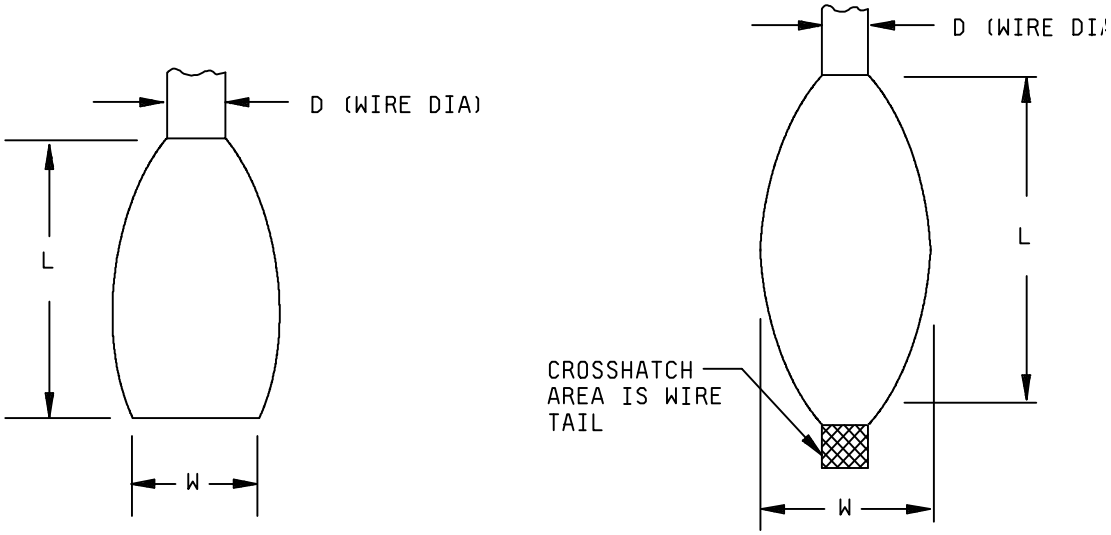
Die without guard ring.

FIGURE 2070-2. Cracks and chips.



Tailless or crescent.

NOTES:
1.2 D ≤ W ≤ 5.0 D (width)
0.5 D ≤ L ≤ 3.0 D (length)



Wedge.

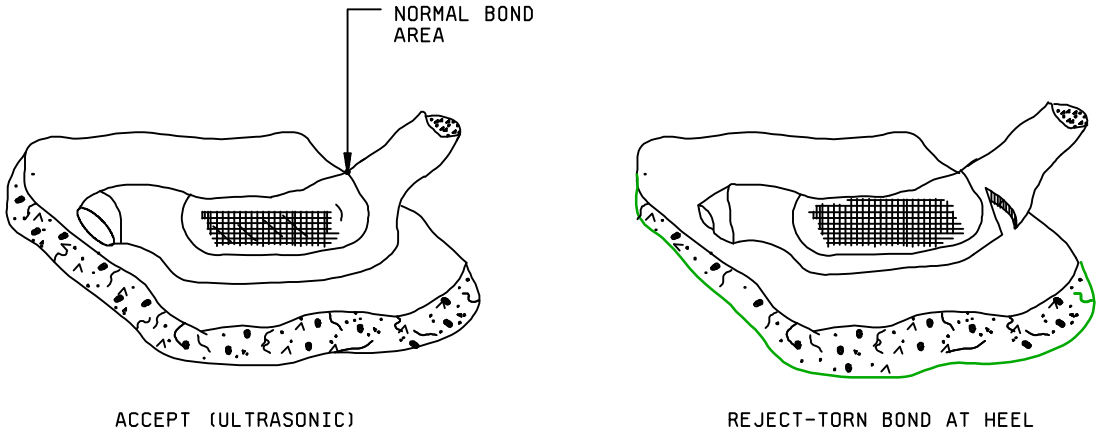
Ultrasonic

NOTES:
1. 1.0 D ≤ W ≤ 3.0 D (width)
2. 1.5 D ≤ L ≤ 5.0 D (length)

Thermocompression

NOTES:
1. 1.2 D ≤ W ≤ 3.0 D (width)
2. 1.5 D ≤ L ≤ 5.0 D (length)

FIGURE 2070-3. Bond dimensions.



REJECT-BOND LIFTED

FIGURE 2070-4. Lifted/torn bonds.

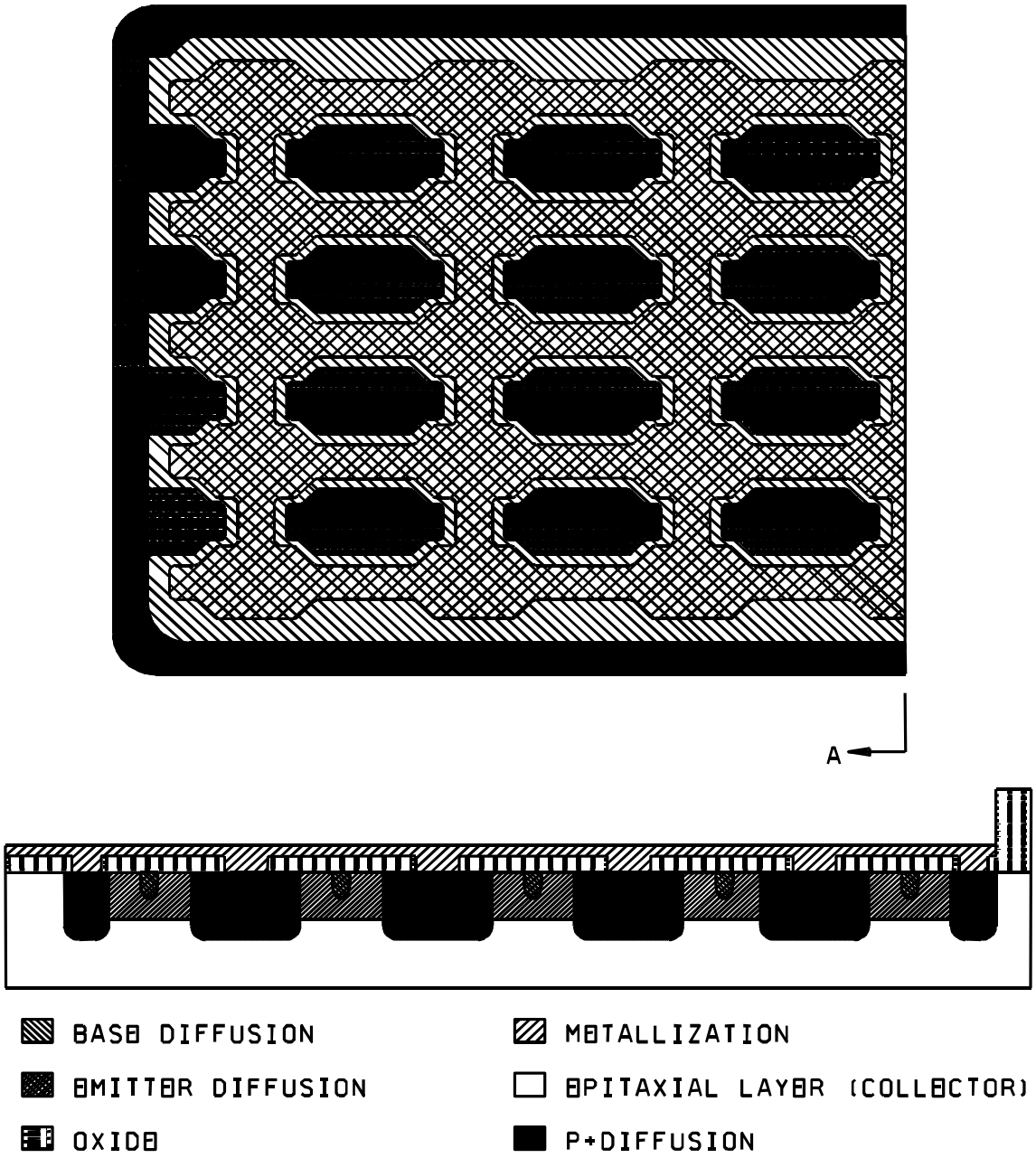


FIGURE 2070-5. Mesh geometry.

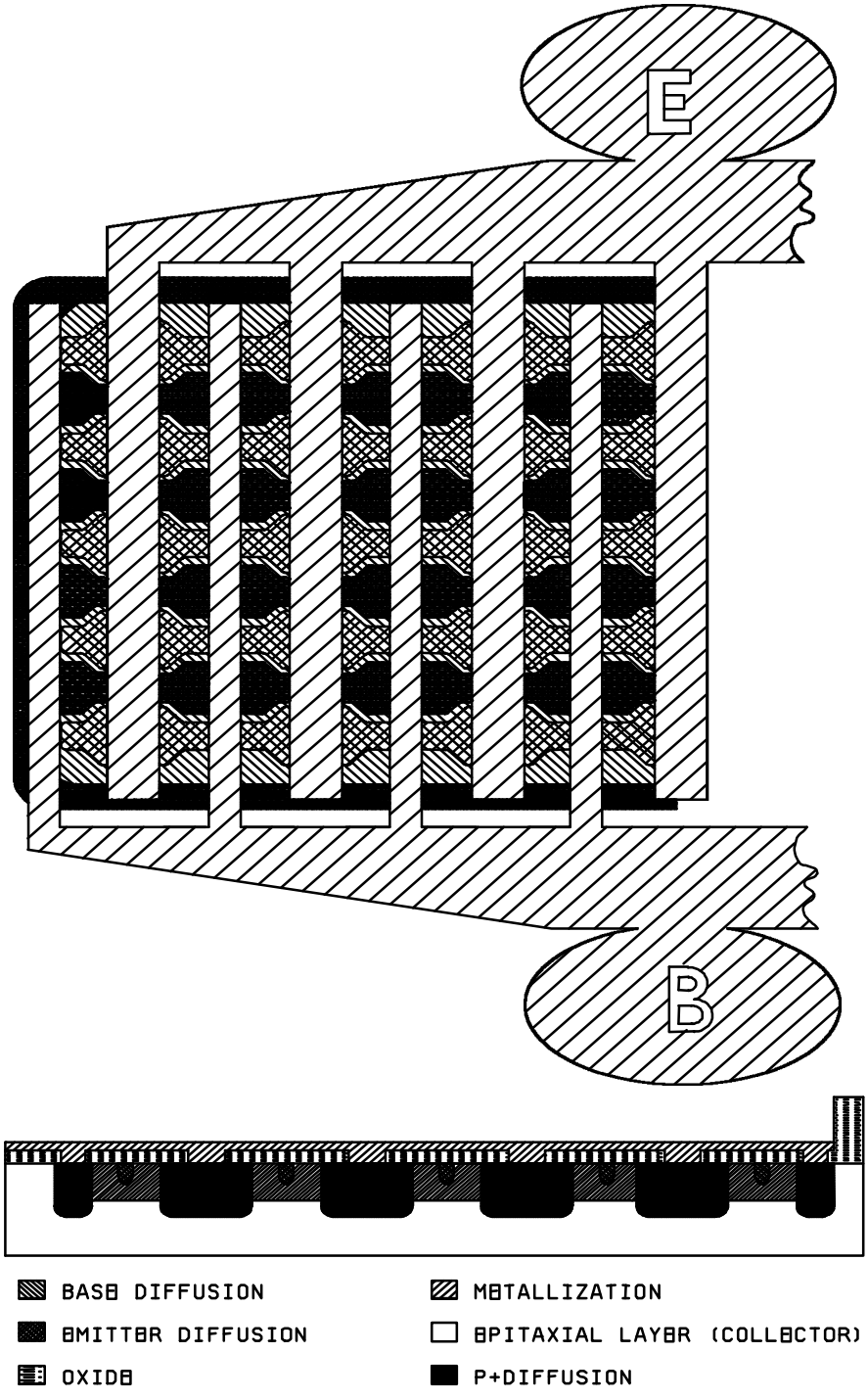


FIGURE 2070-5. Mesh geometry - Continued.

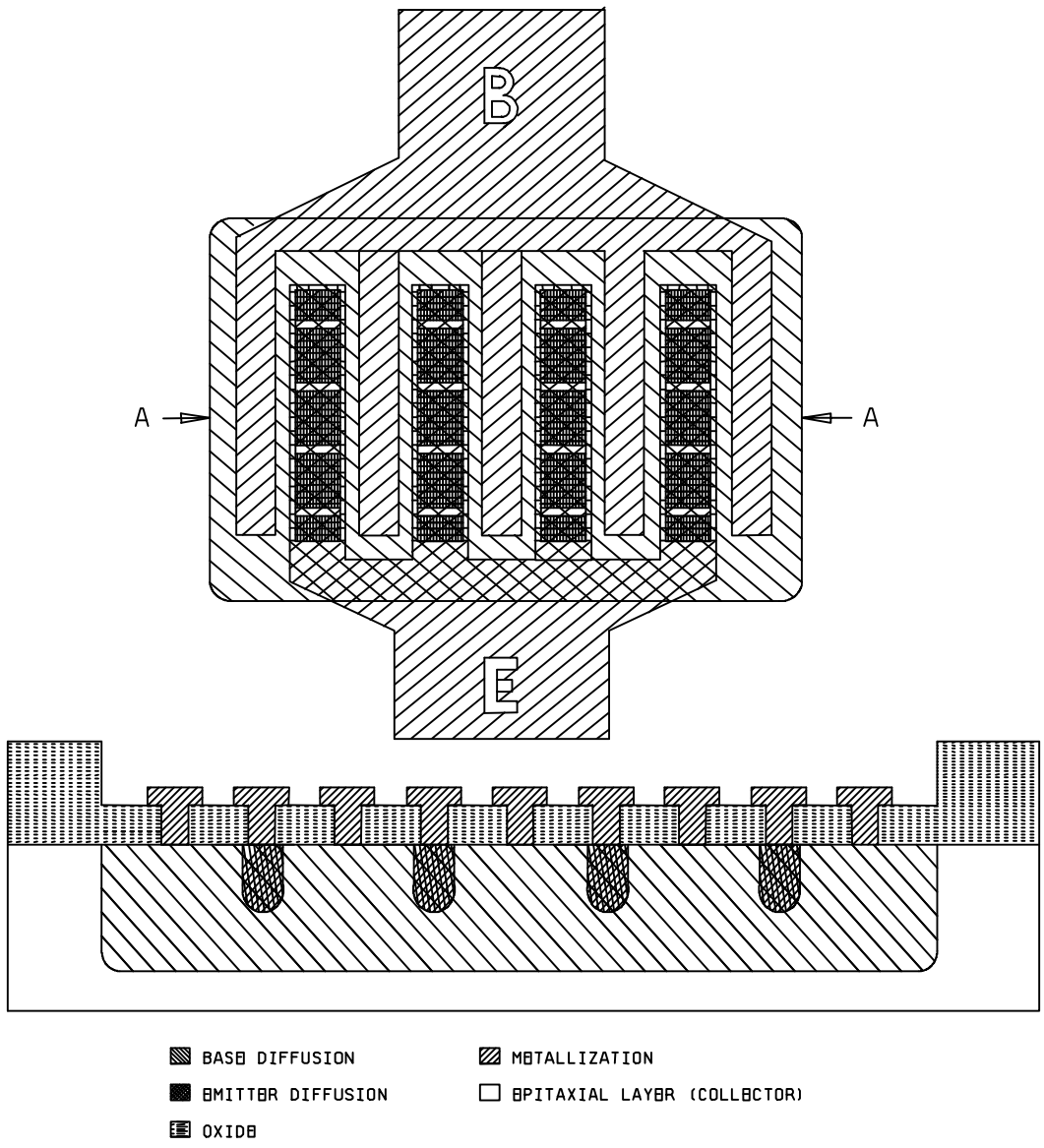


FIGURE 2070-6. Interdigitated geometry.

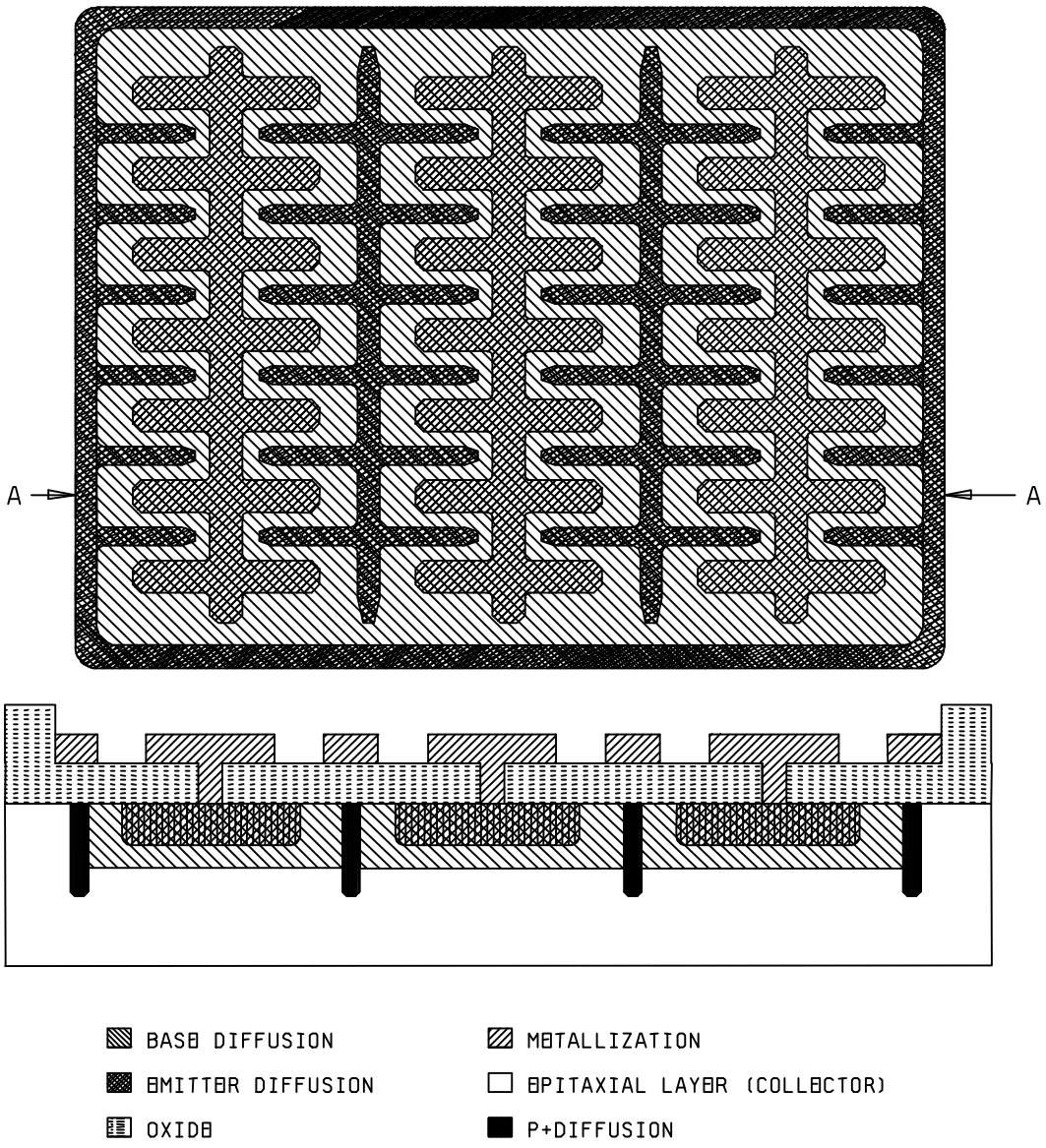


FIGURE 2070-7. Spine geometry.

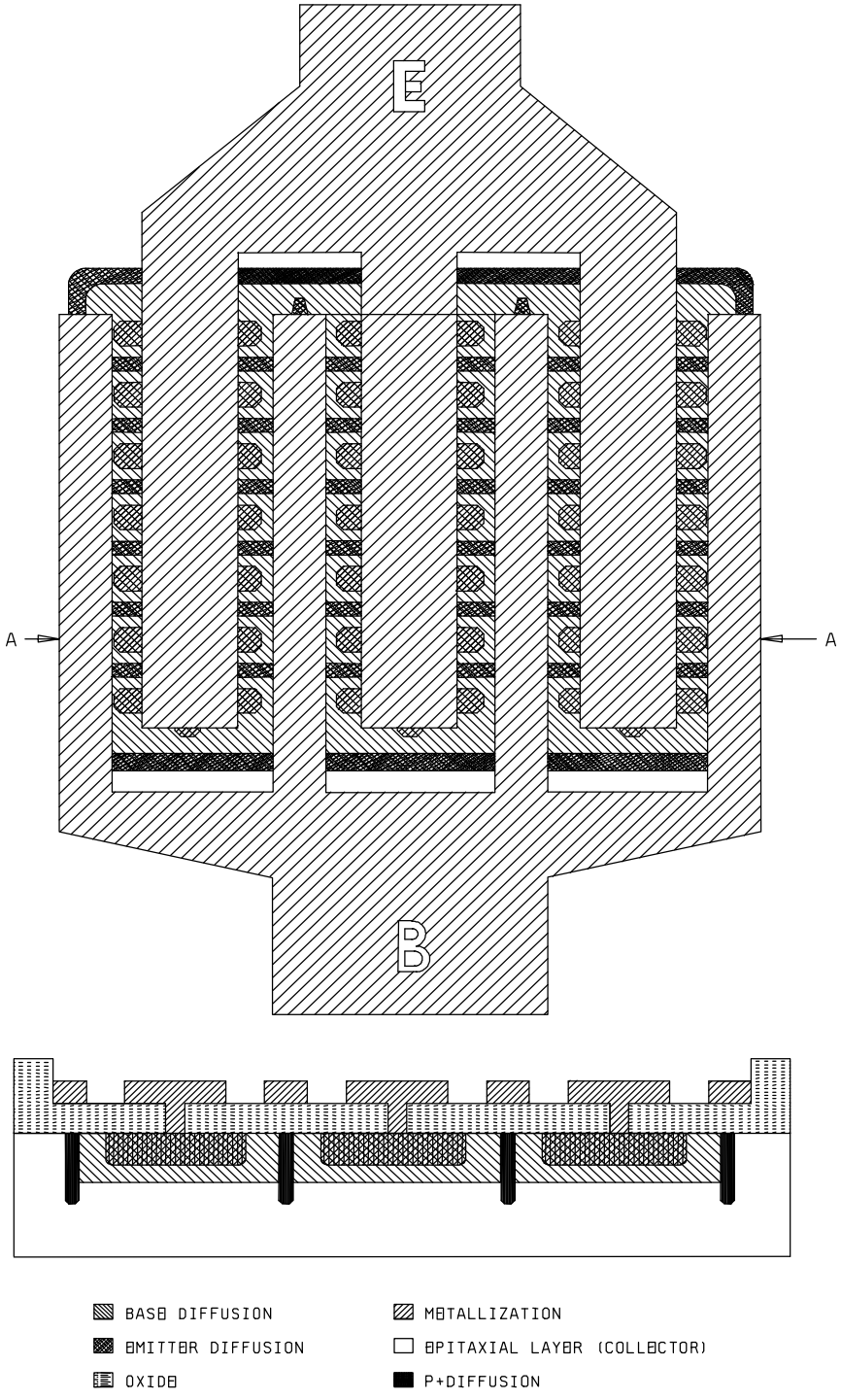


FIGURE 2070-7. Spine geometry - Continued.

METHOD 2075.1

DECAP INTERNAL VISUAL DESIGN VERIFICATION

1. Purpose. The purpose of this examination is to verify that design and construction are the same as those documented in the qualified design report and for which qualification approval has been granted. This test is destructive and would normally be employed on a sampling basis during qualification or quality conformance inspection of a specific device type.

2. Apparatus. Equipment used in this examination shall be capable of demonstrating conformance to the requirements of the applicable acquisition document and shall include optical equipment with sufficient magnification to verify all structural features of the devices.

3. Procedure. Devices shall be selected at random from the inspection lot and examined using sufficient magnification to verify that design and construction are in accordance with the requirements of the applicable design documentation or other specific requirements (see 4.). Specimens of constructions which do not contain an internal cavity (e.g., sealed or embedded devices) or those which would experience destruction of internal features of interest as a result of opening, may be obtained from manufacturing prior to sealing. Specimens of constructions with an internal cavity shall be selected from devices which have completed all manufacturing operations and they shall be delidded or opened taking care to minimize damage to the areas to be inspected. When specified by the applicable detail specification, specimens of constructions with an internal cavity may be obtained from manufacturing prior to sealing.

*3.1 Photographs of die topography and intraconnection pattern. When specified, a color photograph or transparency shall be made showing the topography of elements formed on the die or substrate and the metallization pattern. This photograph shall be at a minimum magnification of 80X except that if this results in a photograph larger than 3.5 x 4.5 inches (88.90 x 114.30 mm), the magnification may be reduced to accommodate the 3.5 x 4.5 inches (88.90 x 114.30 mm) view. In addition, a color photograph for all qualifications reports and design changes is required. The photograph shall be submitted with the 36D form.

3.2 Failure criteria. Devices which fail to meet the detailed requirements for design and construction shall constitute a failure.

4. Summary. The following conditions shall be specified in the detail specification:

a. Any applicable requirements for design and construction.

b. Allowance for obtaining internal cavity devices prior to encapsulation (see 3.).

c. Requirement for photographic record, if applicable (see 3.1), and disposition of photographs.

d. Sample size.

METHOD 2102

DESTRUCTIVE PHYSICAL ANALYSIS FOR WIRE BONDED DEVICES

1. PURPOSE. This method describes procedures and evaluation guidelines for the destructive physical analysis (DPA) of wire bonded semiconductor devices. It is intended to provide techniques for determining compliance with construction requirements, as well as evaluating processes, consistency, and workmanship with respect to MIL-PRF-19500 requirements.

2. SCOPE. This method covers all hermetically sealed, wire bonded device types.

3. REQUIREMENTS

3.1 Apparatus. Equipment requirements shall be as specified in the various test methods for each procedure listed. Equipment for delidding will vary from package to package and may be custom built or provided commercially.

3.2 Sampling. Sampling for DPA shall be specified in the applicable detail specification or acquisition procedure requirements, by contract. If no quantity is given, 3 parts shall be used. If internal water vapor (RGA) is to be performed in 4.9, this sample shall be separate. Parts used for DPA testing must pass group A, subgroup 2 testing as a minimum.

3.3 Applicable inspections. MIL-PRF-19500, the applicable detail specification, the reliability level and any purchase order requirements determine if a listed inspection is applicable. In the event of a conflict the following order of precedence shall be applied; a) purchase order, b) detail specification, c) MIL-PRF-19500, and d) individual test methods. The actual revisions of the specifications referenced within shall be determine from the date code unless superseded by the purchased order or the detail specification. For the purpose of investigation, higher magnifications than specified or alternate equipment may be used, however the report shall clearly indicate whether the observed phenomena was a violation when inspected at the prescribed inspection magnification, at the time of manufacture. The term "when specified" is used herein to identify tests specified in MIL-PRF-19500 which do not apply to all quality levels. These tests are to be performed only on device types which require them as part of the manufacturing process.

4. PROCEDURE. Unless otherwise stated, inspections shall be performed in the order specified.

4.1 Device identification. If unique serial numbers do not already exist identifying each device, they shall be assigned to the sample devices. Serial number identity of all samples and parts of samples shall be maintained throughout the complete analytical process.

4.2 External visual. Perform visual in accordance with MIL-STD-750, method 2071.

4.3 Record markings. The report shall include all markings on the device such as part number, manufacturer, date code, and serial number.

4.4 Electrical test. Group A, subgroup 2 reverse leakage and "On" parameters shall be read and recorded. If read and record data traceable to each individual sample has been previously taken and submitted with the samples, this testing need not be repeated. Sustaining voltage and thermal tests are not to be attempted by the DPA lab since special test circuits or equipment may be required to prevent device damage.

4.5 Hermeticity. Perform gross leak testing in accordance with MIL-STD-750, method 1071, and the associated detail specification. Fine leak shall be performed if RGA is required in 4.10.

4.6 Radiographic Inspection. (When specified) perform radiographic inspection in accordance with MIL-STD-750, method 2076.

4.7 PIND. (When specified) perform particle impact noise detection test in accordance with MIL-STD-750, method 2052, condition A or B. Devices failing PIND shall have particle capture, particle dimensional analysis, and particle element (chemical) analysis performed.

4.8 Decapsulation. Delidding may be performed by any method, however, since delidding techniques require a level of skill and special equipment in good condition to prevent damage to internal components, any internal damage or anomalies observed shall be cause to review the delidding technique used and the potential for the damage or anomaly to have been caused by the delidding process. The decapsulation process used shall be detailed in the DPA report.

4.8.1 Photographs. Two magnified photographs shall be taken with a magnification such that in the first one little more than both ends of all wires are visible (or would be visible if an opaque coating used were not present) and in the second the chip fills the field of view to the maximum possible.

4.8.2 Design verification. Perform design verification in accordance with MIL-STD-750, method 2075.

a. If a design base line exists, the DPA samples shall be compared to that baseline. Differences shall be documented but may not be rejectable if the difference only involves one or more of the following:

(1) The linear or rotational position of the chip.

(2) The position of the wire bonds within the same wire bonding terminal or pad.

(3) The length of the wires.

Violations of the specified internal visual requirements (when specified) take precedence over the above allowances.

b. If no prior baseline exists, the construction details may be requested from the manufacturers design group. Manufacturers shall not be required to provide details unless such agreements were made in advance of purchase.

4.9 Conformal coating removal. (If applicable) Chemicals used to remove compliant coatings must be compatible with remaining materials of interest. Procedures and materials shall be documented and shall be indicated in the DPA report. It is encouraged that a chemical recommendation be obtained from the manufacturer of the device when the manufacturer is not performing the DPA. Additional photos shall be taken in accordance with 4.8.1 following coating removal, and 4.10 shall be repeated.

4.10 Internal visual (when specified). When specified, perform internal visual in accordance with MIL-STD-750, method 2072 for transistors, method 2069 for MOSFETS or method 2073 for diode elements. In the event that foreign material (loose or attached) is found:

a. Identify the elements contained in that material using Energy Dispersive Spectroscopy (EDS) or other suitable techniques.

b. If the material contains corrosive ions such as chlorine:

(1) Select three additional devices from the lot.

(2) Establish the presence of moisture within the package using internal water vapor (RGA), method 2018 of MIL-STD-883, dew point method 1018 of MIL-STD-750 or other suitable means.

(3) If the moisture level passes, the presence of free ions is acceptable.

(4) Data from any DPA performed by or directed by the OEM that shows defects to this test method shall be shared with the manufacturer.

4.11 Bond strength. Perform bond pull in accordance with MIL-STD-750, method 2037.

4.12 SEM. (When specified) perform SEM examination as required in accordance with the detail specification and MIL-STD-750, method 2077.

4.13 Die shear. Perform die shear in accordance with MIL-STD-750, method 2017 unless specified otherwise in the detail drawing.

5. DATA RECORDING AND REPORTING

5.1 Data recording. The data taken at each step of the analysis shall be permanently recorded. The data sheet shall be referenced as an outline for the testing flow. This data shall identify the test method used for each step, the results obtained for each sample device at each step, the identity of the person performing each step, and the date on which each step was accomplished. Photographs, additional comment sheets, and any data taken by agencies other than the DPA lab shall be clearly identified to maintain traceability to each sample device.

5.2 Report. The analysis report shall identify the part number, lot number, manufacturer and source of the sample devices. The report shall include the one of all data generated during the analysis. A separate summary of any noncomformances or anomalous conditions found shall be included. The reporting laboratory may include comments or recommendations to the requesting agency if they deem this appropriate.

5.2.1 Sample retention. All samples, along with one copy of the final DPA report shall be stored and available for review for a minimum of five years from the date of the report.

5.3 Acceptance. This test method only specifies the procedures to be used in DPA. Fitness for use of the devices represented by the analyzed sample must be determined by the agency requesting the DPA. Acceptance or rejection of the lot shall be as contractually agreed between the manufacturer and the procuring activity.

6. SUMMARY. The following details shall be specified by the agency requesting the DPA:

a. The acquisition document to which the lot was acquired.

b. Sample size, if different than specified.

c. Any tests to be added to, or deleted from those specified in this test method.

METHOD 3101.3

THERMAL IMPEDANCE (RESPONSE) TESTING OF DIODES

1. Purpose. The purpose of this test is to determine the thermal performance of diode devices. This can be done in two ways, steady-state thermal impedance or thermal transient testing. Steady state thermal impedance (referred to as thermal resistance) determines the overall thermal performance of devices. A production-oriented screening process, referred to as thermal transient testing, is a subset of thermal impedance testing and determines the ability of the diode chip-to-header interface to transfer heat from the chip to the header, and is a measure of the thermal quality of the die attachment. It is relevant to designs which use headers, or heat conducting plugs, with mass and thermal conductivity allowing effective discrimination of poor die attachments. This is particularly true with power devices. The method can be applied to rectifier diodes, transient voltage suppressors, power zener diodes, and some zener, signal and switching diodes. This method is intended for production monitoring, incoming inspection, and pre-burn in screening applications. Some zener constructions, particularly when used with small junction area designs, cool too rapidly (from a heating current) to provide accurate measurement when forward (diode) current is used for this test. For such devices, a method is provided to apply currents in the zener direction and make a measurement much closer to the termination of the heating current. In this way, no minority carriers are involved and inductive effects are minimized due to lower test current. This may be considered a lab measurement because cable lengths in an ATE may prevent accurate measurements so close to cessation of the heating current. This laboratory method is intended on initial zener device design verification for correlation to forward direction thermal impedance testing (such as with ATE) prior to establishing a production test limit. Correlation assurance must be provided in the forward production monitoring that thermal impedance in the reverse direction (zener) must not exceed the specified limit. If this zener test method exceeds the forward method by 10 percent or more, production monitoring (with an ATE in the forward direction) will require a lower limit, for some devices, than that required by the more accurate lab method (see 5.1).

1.1 Background and scope for thermal transient testing. Steady-state thermal response (transient thermal impedance) of semiconductor devices are sensitive to the presence of these voids in the die attachment material between the semiconductor chip and package since voids impede the flow of heat from the chip to the substrate (package). Due to the difference in the thermal time constants of the chip and package, the measurement of transient thermal response can be made more sensitive to the presence of voids than can the measurement of steady-state thermal response. This is because the chip thermal time constant is generally several orders of magnitude shorter than that of the package. Thus, the heating power pulse width can be selected so that only the chip and the chip-to-substrate interface are heated during the pulse by using a pulse width somewhat greater than the chip thermal time constant but less than that of the substrate. Heating power pulse widths ranging from 1 to 400 ms for various package designs have been found to satisfy this criterion. This enables the detection of voids to be greatly enhanced, with the added advantage of not having to heat sink the DUT. Thus, the transient thermal impedance or thermal response techniques are less time-consuming than the measurement of thermal resistance for use as a manufacturing screen, process control, or incoming inspection measure for die attachment integrity evaluation.

2. Definitions. The following symbols and terminology shall apply for the purpose of this test method in the forward direction: (When using the zener method, see NOTES below):

a. V_F: The forward biased junction voltage of the DUT used for junction temperature sensing.
NOTE: When using the zener method, delete “forward” and use “zener” bias.
V_{Fi}: The initial V_F value before application of heating power.
V_{Ff}: The final V_F value after application of heating power.

b. ΔV_F The change in the TSP, V_F, due to the application of heating power to the DUT.

c. I_H: The current applied to the DUT during the heating time in order to cause power dissipation.

d. V_H: The heating voltage resulting from the application of I_H to the DUT.

e. P_H: The heating power pulse magnitude; product of V_H and I_H.

f. t_H: The duration of P_H applied to the DUT.

g. I_M: The measurement current used to forward bias the temperature sensing diode junction for measurement of V_F.

NOTE: When using the zener, delete “forward” and use “zener” bias.

h. t_{MD}: Measurement delay time is defined as the time from the start of heating power (P_H) removal to the start of the final V_F measurement time, referred to as t_{SW}.

i. t_{SW}: Sample window time during which final V_F measurement is made. The value of t_{SW} should be small; it can approach zero if an oscilloscope is used for manual measurements.

j. VTC: Voltage-temperature coefficient of V_F with respect to T_J at a fixed value of I_M; in mV/°C.

k. K: Thermal calibration factor equal to the reciprocal of VTC; in °C/mV.

l. CU: The comparison unit, consisting of ΔV_F divided by V_H, that is used to normalize the transient thermal response for variations in power dissipation; in units of mV/V.

m. T_J: The DUT junction temperature.

n. ΔT_J: The change in T_J caused by the application of P_H for a time equal to t_H.

o. $Z_{\theta JX}$: Thermal impedance from device junction to a time defined reference point; in units of °C/W.

p. $Z_{\theta JC}$: Thermal impedance from device junction to a point on the outside surface of the case immediately adjacent to the device chip measured using time equal time constant of device; in units of °C/W.

q. $R_{\theta JX}$: Thermal resistance from device junction to a defined reference point; in units of °C/W.

$R_{\theta JC}$: Thermal resistance from device junction to a point on the outside surface of the case immediately adjacent to the device chip; in units of °C/W.

$R_{\theta JA}$: Thermal resistance from device junction to an ambient (world); in units of °C/W.

*r. TSP: The temperature sensitive parameter of V_F or V_Z.

*s. V_Z: The zener voltage. (Also see note 1.)

NOTES: 1. When using the zener method, the following changes shall further apply to the definitions whenever they appear in the text.

Letter symbols: I_F becomes I_Z
V_F becomes V_{ZL}
V_H becomes V_{ZH}
V_{Fi} becomes V_{ZLi}
V_{Ff} becomes V_{ZLf}
ΔV_F becomes ΔV_{ZL}
wording: “forward” bias becomes “reverse” bias

2. ΔV_F, K, and CU parameter values will be substantially different when using the zener method (as

compared to the forward biased method). Some difference will be observed between zeners with different nominal voltages.

3. Apparatus. The apparatus required for this test shall include the following, configured as shown on figure 3101-1, as applicable to the specified test procedure:

a. A constant current source capable of adjustment to the desired value of I_H and able to supply the V_H value required by the DUT. The current source should be able to maintain the desired current to within ±2 percent during the entire length of heating time.

b. A constant current source to supply I_M with sufficient voltage compliance to turn the TSP junction fully on.

c. An electronic switch capable of switching between the heating period conditions and measurement conditions in a time frame short enough to avoid DUT cooling during the transition; this typically requires switching in the microsecond or tens of microseconds range.

d. A voltage measurement circuit capable of accurately making the V_{Ff} measurement within the time frame with millivolt resolution.

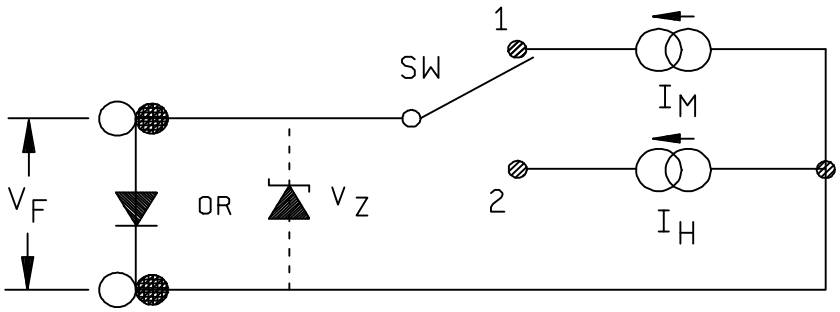
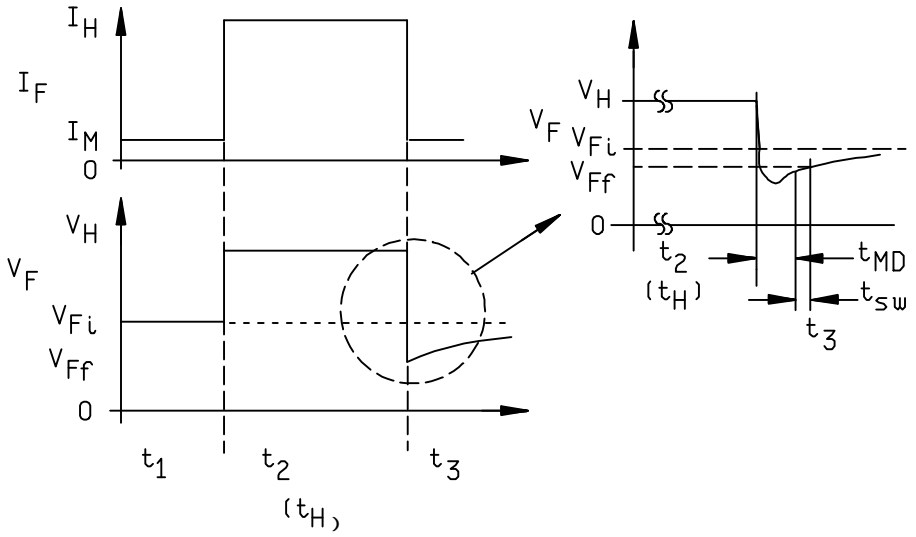


FIGURE 3101-1. Thermal impedance testing setup for diodes.

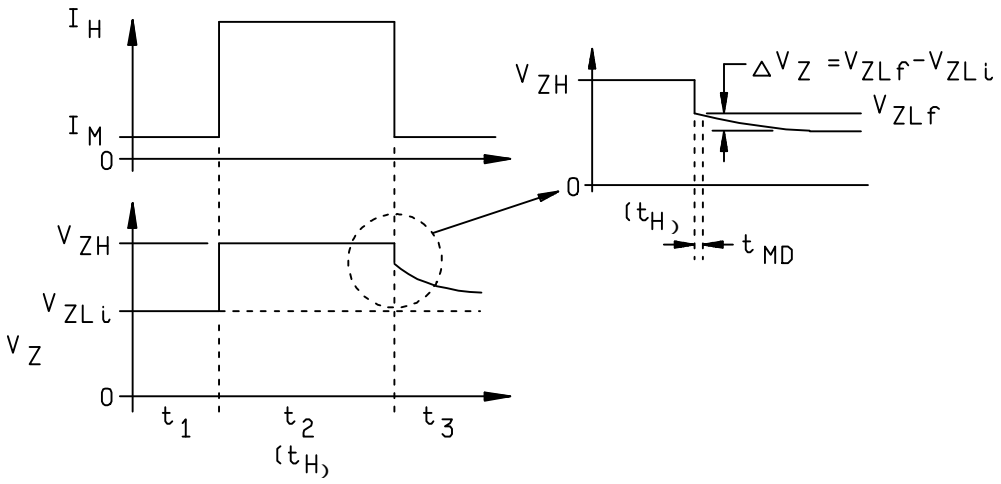
4. Test operation.

4.1 General description. The test begins with the adjustment of I_M and I_H to the desired values. The value of I_H is usually at least 50 times greater than the value of I_M. Then with the electronic switch in position 1, the value of V_{Fi} is measured. The switch is then moved to position 2 for a length of time equal to t_H and the value of V_H is measured. Finally, at the conclusion of t_H, the switch is again moved to position 1 and the V_{Ff} value is measured within a time period defined by t_{MD} (or $t_{MD} + t_{SW}$, depending on the definitions stated previously). The two current sources are then turned off at the completion of the test.



Forward biased method

FIGURE 3101-2a. Thermal impedance testing waveforms.



Zener biased method

FIGURE 3101-2b. Thermal impedance testing waveforms - Continued.

4.2 Notes.

a. Some test equipment may provide a ΔV_F directly instead of V_{Fi} and V_{Ff}; this is an acceptable alternative. Record the value of ΔV_F.

b. Some test equipment may provide $Z_{\theta JX}$ directly instead of V_{Fi} and V_{Ff} for thermal resistance calculations; this is an acceptable alternative. Record the value of $Z_{\theta JX}$.

c. Alternative waveforms, as may be generated by ATE using the general principles of this method, may be used upon approval of the qualifying activity.

*d. The zener biased method in Fig 3101-2b illustrates a positive TSP when the zener is in avalanche breakdown. It is also possible to portray a negative TSP for low voltage zeners when they are in the field-emmission or tunneling mode. A near-zero TSP can also result from these two off-setting factors of a specific operating current that must be avoided by changing to a higher or lower current. Also see paragraph 6 for TSP.

5. Acceptance limit.

5.1 General discussion. Variations in diode characteristics from one manufacturer to another cause difficulty in establishing a single acceptance limit for all diodes tested to a given specification. Ideally, a single acceptance limit value for ΔV_F would be the simplest approach. However, different design, materials, and processes can alter the resultant ΔV_F value for a given set of test conditions. Listed below are several different approaches to defining acceptance limits. The ΔV_F limit is the simplest approach and is usually selected for screening purposes. 5.3 through 5.6 require increasingly greater detail or effort. In some examples, absolute thermal impedance limits are required for correlation to surge performance such as for zeners. In such examples, setting a limit for zener diode construction with the forward biased (usual ATE) method requires prior evaluation of $Z_{\theta JX}$ (and $R_{\theta JX}$, when desired) by the zener biased method. If the zener method result is more than 10 percent higher, the limit shall be based on the more accurate zener biased measurement. In such case, if it is desired to use the forward biased method, the limit (of ΔV_F, $Z_{\theta JX}$, or $R_{\theta JX}$) shall be reduced by the extent (percentage) difference between the two methods.

5.2 ΔV_F limit. A single ΔV_F limit is practical if the K factor and V_H values for all diodes tested to a given specification are nearly identical. Since these values may be different for different manufacturers, the use of different limits is likely to more accurately achieve the desired intent. (A lower limit does not indicate a better die bond when comparing different product sources.) The diode specifications would list the following test conditions and measurement parameters:

I_H (in A)

t_H (in ms)

I_M (in mA)

t_{MD} (in µs)

t_{SW} (in µs)

ΔV_F (maximum limit value, in mV)

5.3 ΔT_J limit. (Much more involved than ΔV , but useful for examining questionable devices.) Since ΔT_J is the product of K (in accordance with 6.) and ΔV_F, this approach is the same as defining a maximum acceptable junction temperature rise for a given set of test conditions.

5.4 CU limit. (Slightly more involved than ΔT_J.) The ΔT_J limit approach described above does not take into account potential power dissipation variations between devices. The V_H value can vary, depending on chip design and size, thus causing the power dissipation during the heating time to be different from device to device. This variation will be small within a lot of devices produced by a single manufacturer but may be large between manufacturers. A CU limit value takes into account variations in power dissipation due to differences in V_H by dividing the ΔV_F value by V_H.

5.5 (K•CU) limit. (Slightly more involved but provides greater detail.) This is a combinational approach that takes into account both K factor and power dissipation variations between devices.

5.6 $Z_{\theta JX}$ limit. (For full characterization; not required for screening purposes, but preferred if the proper ATE is available.) The thermal impedance approach uses an absolute magnitude value specification that overcomes the problems associated with the other approaches. Thermal impedance is time dependent and is calculated as follows:

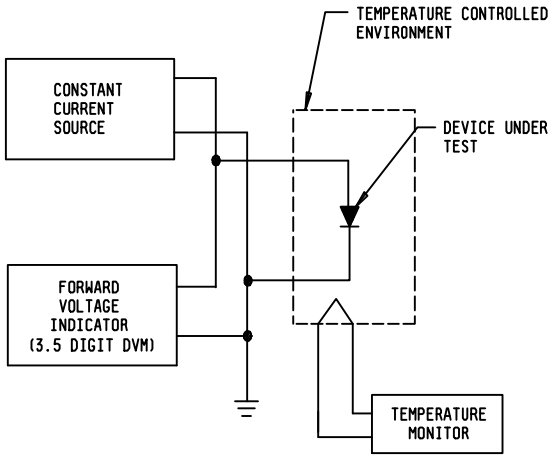
$$Z_{\Theta JX} = \frac{\Delta T_J}{P_D} = \left| \frac{(K)(\Delta V_F)}{(I_H)(V_H)} \right| {}^{O}\text{C/W}$$

5.7 $R_{\theta JX}$ limit. (For thermal resistance specification testing.) The thermal resistance to some defined point, such as the case, is an absolute magnitude value specification used for equilibrium conditions. The t_H heating time must therefore be extended to appreciably longer times (typically 20 to 50 seconds). In the example of $R_{\theta JC}$ measurements, the case must be carefully stabilized and monitored in temperature which requires an infinite heat sink for optimum results. The ΔT_J is the difference in junction temperature to the case temperature for the example of $R_{\theta JC}$.

$$R_{\Theta JX} = \frac{\Delta T_J}{P_D} = \left| \frac{(K)(\Delta V_F)}{(I_H)(V_H)} \right| {}^{O}\text{C/W}$$

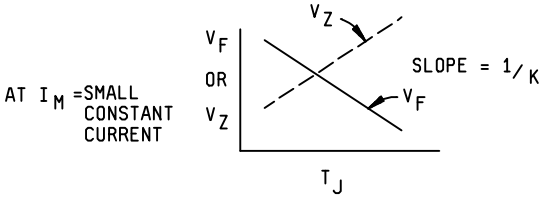
5.8 General comment for thermal transient testing. One potential problem in using the thermal transient testing approach lies in trying to make accurate enough measurements with sufficient resolution to distinguish between acceptable and nonacceptable diodes. As the diode-under-test current handling capability increases, the thermal impedance under transient conditions will become a very small value. This raises the potential for rejecting good devices and accepting bad ones. Higher I_H values must be used in this case.

*6. Measurement of the TSP V_F (or V_Z). The calibration of V_F versus T_J is accomplished by monitoring V_F for the required value of I_M as the environmental temperature (and thus the DUT temperature), and is varied by external heating. It is not required if the acceptance limit is ΔV_F (see 5.2), but is relevant to the other acceptance criteria (see 5.3 through 5.6). The magnitude of I_M shall be chosen so that V_F is a linearly decreasing function over the normal T_J range of the device. I_M must be large enough to ensure that the diode junction is turned on but not large enough to cause significant self-heating. An example of the measurement method and resulting calibration curve is shown on figure 3101-3.



Step 1: Measure V_{F1} at T_{J1} using I_M
Step 2: Measure V_{F2} at T_{J2} using I_M

Step 3: $K = \left| \frac{T_{J2} - T_{J1}}{V_{F2} - V_{F1}} \right| °C / mV$



I_M: must be large enough to overcome surface leakage effects but small enough not to cause significant self-heating.
*When using the zener direction, the I_M may also require adjustment to avoid a near zero TSP where the avalanche breakdown effects are offset by tunneling or field emission. (See 4.2, note d.)

T_J: is externally applied: (e.g., via oven, liquid) environment.

FIGURE 3101-3. Example curve of V_F versus T_J.

A calibration factor K (which is the reciprocal of the slope of the curve on figure 3101-3) can be defined as:

$$K = \left| \frac{T_{J2} - T_{J1}}{V_{F2} - V_{F1}} \right| \ ^{\circ}C/mV$$

*It has been found experimentally that the K-factor variation for all devices within a given device type class is small. The usual procedure is to perform a K factor calibration on a 10 to 12 piece sample from a device lot and determine the average K and standard deviation (σ). If σ is less than or equal to three percent of the average value of K, then the average value of K can be used for all devices within the lot. If σ is greater than three percent of the average value of K, then all the devices in the lot shall be calibrated and the individual values of K shall be used in determining device acceptance. As an alternative to using individual values of K, the manufacture may establish internal limits unique to their product that ensures atypical product removal from the population (lot-to-lot and within-the-lot). The manufacture shall use statistic techniques to establish the limits to the satisfaction of the government.

7. Establishment of test conditions and acceptance limits. Thermal resistance measurements require that I_H be equal to the required value stated in the device specifications, typically at rated current or higher. Values for t_H, t_{MD}, and heat sink conditions are also taken from the device specifications. The steps shown below are primarily for thermal transient testing and thermal characterization purposes.

The following steps describe how to set up the test conditions and determine the acceptance limits for implementing the transient thermal test for die attachment evaluation using the apparatus and definitions stated above.

7.1 Initial device testing procedure. The following steps describe in detail how to set up the apparatus described previously for proper testing of various diodes. Since this procedure thermally characterizes the diode out to a point in heating time required to ensure heat propagation into the case (i.e., the $R_{\theta JX}$ condition), an appropriate heat sink should be used or the case temperature should be monitored.

Step 1: From a 20 to 25 piece sample, pick any one diode to start the setup process. Set up the test apparatus as follows:

I_H = 1.0 A	(Or some other desired value near the DUTs normal operating current: typically higher for power diodes, and lower for zener diodes, when measured in the zener direction.)
t_H = 10-50 ms	Unless otherwise specified, for most devices rated up to 15 W power dissipation.
50 - 100 ms	Unless otherwise specified, for most devices rated up to 200 W power dissipation.
≥ 250 ms	For steady state thermal resistance measurement. The pulse must be shown to correlate to steady state conditions before it can be substituted for steady state condition.
*t_{MD} = 100 μs max	A larger value may be required on power devices with inductive package elements which generate nonthermal electrical transients; unless otherwise specified, this would be observed in the t_3 region of figure 3101-2.
I_M = 10 mA	(Or some nominal value approximately two percent, or less, of I_H.)

Step 2: Insert device into the apparatus test fixture and initiate a test. (For best results, a test fixture that offers some form of heat sinking would be desirable. Heat sinking is not needed if either the power dissipation during the test is well within the diode's free-air rating or the maximum heating time is limited to less than that required for the heat to propagate through the case.)

*Step 3: If ΔV_F is in the 15 to 80 mV range, or ΔV_{ZL} is equivalent to the same ΔT_J, then proceed to the next step. This range approximately corresponds to a junction temperature change of roughly +10°C to +50°C and is sufficient for initial comparison purposes.

If ΔV_F is less than 15 mV, return to step 1 and increase heating power into device by increasing I_H.

If ΔV_F is greater than 80 mV, approximately corresponding to a junction temperature change greater than +50°C, it would probably be desirable to reduce the heating power by returning to step 1 and reducing I_H.

NOTE: The test equipment shall be capable of resolving ΔV_F to within five percent. If not, the higher value of ΔV_F must be selected until the five percent tolerance is met. Two different devices can have the same junction temperature rise even when P_H is different, due to widely differing V_H. Within a given lot, however, a higher V_H is more likely to result in a higher junction temperature rise. For such examples, this screen can be more accurately accomplished using the CU value. As defined in 2., CU provides a comparison unit that takes into account different device V_H values for a given I_H test condition.

*Step 4: Test each of the sample devices and record the data detailed in 8.1.

*Step 5: Select out the devices with the highest and lowest values of CU or $Z_{\theta JX}$ and put the remaining devices aside.

The ΔV_F values can be used instead of CU or $Z_{\theta JX}$ if the measured values of V_H are very tightly grouped around the average value.

Step 6: Using the devices from step 5, collect and plot the heating curve data for the two devices in a manner similar to the examples shown on figure 3101-4.

*Step 7: Interpretation of the heating curves is the next step. Realizing that the thermal characteristics of identical chips should be the same if the heating time (t_H) is less than or equal to the thermal time constant of the chip, the two curves should start out the same for the low values of t_H. Non identical chips (thinner or smaller in cross section) will have completely different curves, even at the smaller values of t_H. As the value of t_H is increased, thereby exceeding the chip thermal constant, heat will have propagated through the chip into the die attachment region. Since the heating curve devices of step 5 were specifically chosen for their difference, the curves of figure 3101-4 diverge after t_H reaches a value where the die attachment variance has an affect on the device junction temperature. Increasing t_H further will probably result in a flattening of the curve as the heating propagates in the device package. If the device package has little thermal mass and is not well mounted to a good heat sink, the curve will not flatten very much, but will show a definite change in slope.

Step 8: Using the heating curve, select the appropriate value of t_H to correspond to the inflection point in the transition region between heat in the chip and heat in the package.

If there are several different elements in the heat flow path: Chip, die attachment, substrate, substrate attach, and package for example in a hybrid, there will be several plateaus and transitions in the heating curve. Appropriate selection of t_H will optimize evaluation sensitivity to other attachment areas.

Step 9: Return to the apparatus and set t_H equal to the value determined from step 8.

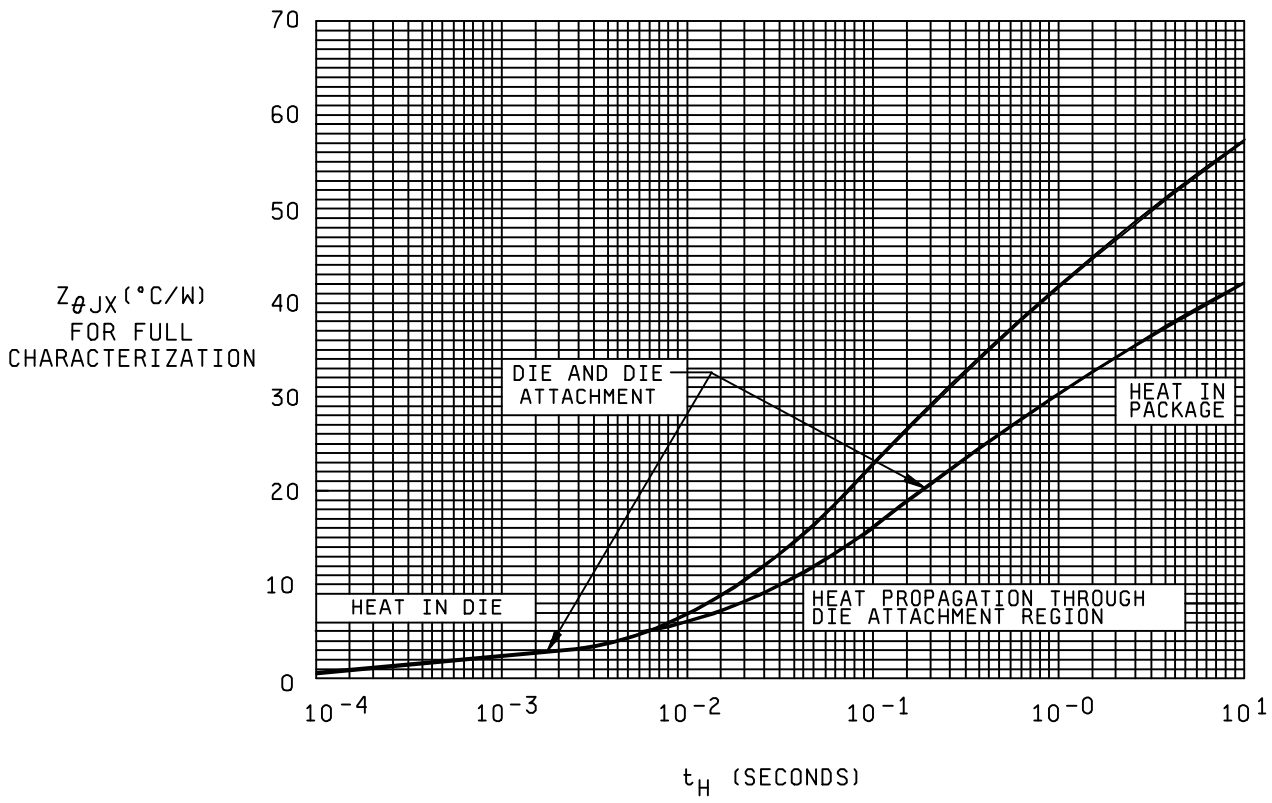


FIGURE 3101-4. Heating curves for two extreme devices.

Step 10: Because the selected value of t_H is much less than that for thermal equilibrium, it is possible to significantly increase the heating power without degrading or destroying the device. The increased power dissipation within the DUT will result in higher ΔV_F or CU values that will make determination of acceptable and nonacceptable devices much easier.

Step 11: The pass/fail limit, the cut-off point between acceptable and nonacceptable devices, can be established in a variety of ways:

a. Correlation to other die attachment evaluation methods, such as die shear and x-ray, while these two methods have little actual value from a thermal point of view, they do represent standardization methods as described in various military standards.

*b. Maximum allowable junction temperature variations between devices, since the relationship between ΔT_J and ΔV_F is about 0.5°C/mV for forward bias testing, or a measurable equivalent for zener direction testing, the junction temperature spread between devices can be easily determined. The T_J predicts reliability. Conversely, the T_J spread necessary to meet the reliability projections can be translated to a ΔV_F or CU value for pass/fail criteria.

To fully utilize this approach, it will be necessary to calibrate the devices for the exact value of the T_J to V_F characteristic. The characteristic's slope, commonly referred to as K factor, is easily measured on a sample basis using a voltmeter, environmental chamber, temperature indicator, and a power supply setup as described in 6. A simple set of equations yield the junction temperature once K and ΔV_F are known:

$$\Delta T_J = (K)\ (\Delta V_F)$$

$$T_J = T_A + \Delta T_J$$

Where T_A is the ambient or reference temperature. For thermal transient test conditions, this temperature is usually equivalent to lead temperature (T_L) for axial lead devices or case temperature (T_C) for case mounted devices.

*c. Statistically from a 20 to 25 device sample the distribution of ΔV_F or CU values should be a normal one with defective devices out of the normal range. Figure 3101-5 shows a ΔV_F distribution for a sample lot of diodes. NOTE: The left-hand side of the histogram envelope is fairly well defined but the other side is greatly skewed to the right. This comes about because the left-hand side is constrained by the absolutely best heat flow that can be obtained with a given chip assembly material and process unless a test method error is introduced. The other side has no such constraints because there is no limit as to how poorly a chip is mounted.

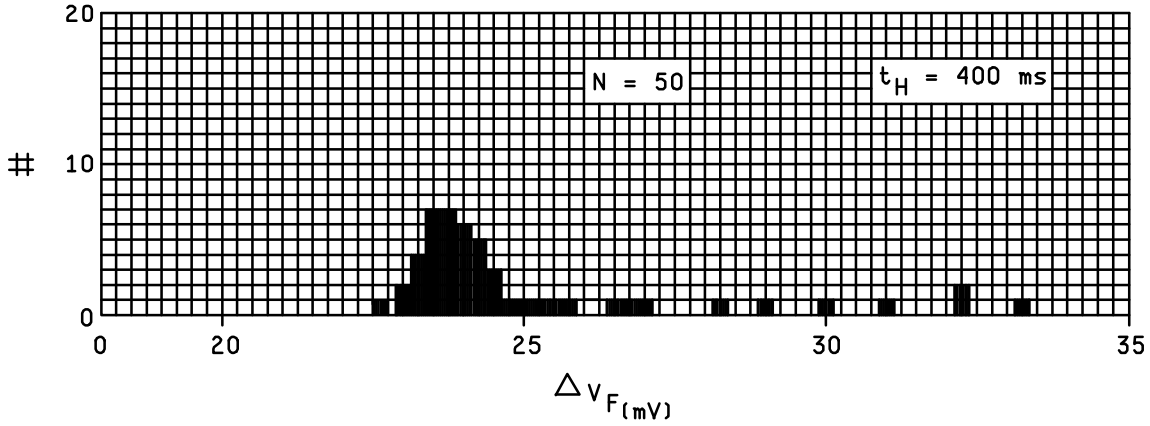


FIGURE 3101-5. Typical ΔV_F distribution.

The usual rule of thumb in setting the maximum limit for ΔV_F , CU, or $Z_{\theta JX}$ is to use the distribution average value and three standard deviations (σ). For example:

$$| (\Delta V_F) | = \overline{\Delta V_F} + X \sigma$$

high
limit

$$| (CU) | = \overline{CU} + X \sigma$$

high
limit

$$| (Z_{\theta JX}) | = \overline{Z_{\theta JX}} + X \sigma$$

high
limit

Where X = 3 in most cases and $\overline{\Delta V_F}$, $\overline{\Delta CU}$, and $\overline{\Delta Z_{\theta JX}}$ are the average distribution values.

The statistical data required is obtained by testing 25 or more devices under the conditions of step 11.

The maximum limit determined from this approach should be correlated to the diode's specified thermal resistance. This will ensure that the ΔV_F or CU limits do not pass diodes that would fail the thermal resistance or transient thermal impedance requirements.

*Step 12: Once the test conditions and pass/fail limit have been determined, it is necessary only to record this information for future testing requirements of the same device in the same package. It is also recommended that a minimum limit is established to ensure a test method error or other anomaly is investigated.

*Step 13: After the pass/fail limits are established, there shall be verification they correllate to good and bad bonded devices or the electrical properties such as surge.

The steps listed hereto are conveniently summarized in table 3101-I.

*TABLE 3101-I. Summary of test procedure steps.

General description		Steps	Comments
A	Initial setup	1 through 4	Approximate instrument settings to find variations among devices in 10 to 15 piece sample.
B	Heating curve generation	5 through 6	Using highest and lowest reading devices, generate heating curves.
C	Heating curve interpretation	7 through 9	Heating curve is used to find more appropriate value for t_H corresponding to heat in the die attachment area (for some other desired interface in the heat flow path).
D	Final setup	10	Heating power applied during t_H is increased in order to improve measurement sensitivity to variations among devices.
E	Pass-fail determination	11 through 12	A variety of methods is available such as JESD 34 for setting the fail limit; the statistical approach is the fastest and easiest to implement.
F	Verification	13	Mechanical / Electrical Correllation

7.2 Routine device thermal transient testing procedure. Once the proper control settings have been determined for a particular device type from a given manufacturing process or vendor, repeated testing of that device type simply requires that the same test conditions be used as previously determined.

New device types or the same devices manufactured with a different process will require a repeat of 7.1 for proper thermal transient test conditions.

8. Test conditions and measurements to be specified and recorded.

8.1 Thermal transient and equilibrium measurements.

8.1.1 Test conditions. Specify the following test conditions:

a. I_M measuring current ___ mA

b. I_H heating current ___ A

c. t_H heating time ___ ms

d. t_{MD} measurement time delay ___µs

e. t_{SW} sample window time ___ µs

8.1.2 Data. Record the following data:

a. V_{Fi} initial forward voltage ___V

b. V_H heating voltage ___V

c. V_{Ff} final forward voltage ___V

(NOTE: Some test equipment may provide a ΔV_F instead of V_{Fi} and V_{Ff}; this is an acceptable alternative. Record the value of ΔV_F.

Some test equipment may provide direct display of calculated CU or $Z_{\theta JX}$ this is an acceptable alternative. Record the value of CU or $Z_{\theta JX}$.

8.2 K factor calibration. (Optional for criteria 8.3a or 8.3b, mandatory for 8.3c, 8.3d, or 8.3e.)

8.3 Test conditions. Specify the following test conditions:

a. I_M current magnitude ___mA

b. Initial junction temperature ___°C

c. Initial V_F voltage ___mV

d. Final junction temperature ___°C

e. Final V_F voltage ___mV

8.4 K factor. Calculate K factor in accordance with the following equation:

$$K = \left| \frac{T_{J2} - T_{J1}}{V_{F2} - V_{F1}} \right| \ ^\circ C/mV$$

K factor ___°C/mV

8.5 Specification limit calculations. One or more of the following should be measured or calculated, as called for on the device specification (see 5.1):

ΔV_F ___mV

CU ___mV/V

ΔT_J ___°C

K•CU ___°C/V

$Z_{\theta JX}$ ___°C/W

$R_{\theta JX}$ ___°C/W

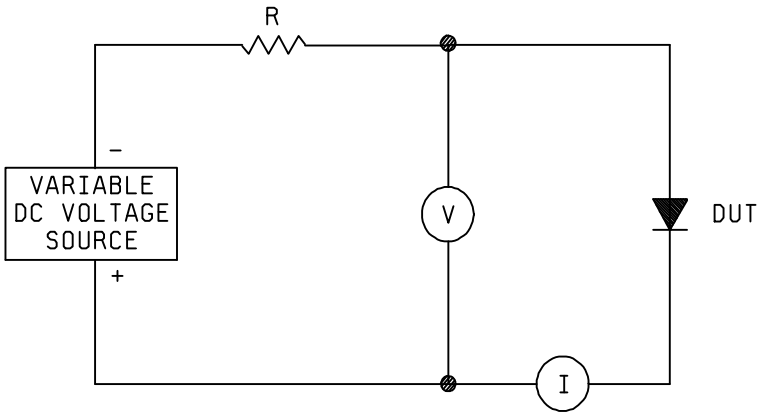
METHOD 4016.4

REVERSE CURRENT LEAKAGE

1. Purpose. The purpose of this test is to measure the reverse current leakage through a device at a specified reverse voltage using a dc method or an ac method, as applicable.

2. DC method.

2.1 Test circuit. See figure 4016-1.



NOTE: To assure accurate measurement of reverse leakage current, the voltage drop across the ammeter shall be subtracted from the measured value of reverse voltage. Resistor (R) shall be chosen to limit the current flow in the event the device goes into reverse breakdown.

FIGURE 4016-1. Test circuit for reverse current leakage (dc method).

2.2 Procedure.

2.2.1 Reverse current. The dc voltage shall be adjusted to the specified value by voltmeter (V) and the reverse current (I_R) shall be measured by current meter (I).

3. AC method.

3.1 Test circuit. See figure 4016-2.

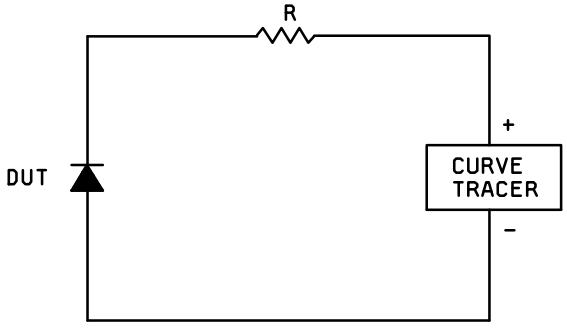


FIGURE 4016-2. Test circuit for reverse current leakage (ac method).

*Note: The resistor R is a selectable value within the curve tracer.

3.2 Procedure.

3.2.1 Reverse current. A Tektronix 576-curve tracer or equivalent shall be used to apply voltage in the reverse direction only. The curve tracer supply shall be adjusted to obtain the specified peak reverse voltage across the device. Current and voltage shall be measured on the curve tracer.

4. Summary. The following conditions shall be specified in the detail specification:

a. DC or ac method.

b. Test voltage (dc method) or peak reverse voltage (ac method).

c. Thermal resistance of minimum heat dissipater on which device is mounted in °C/W (where applicable).

*d. Thermal equilibrium or pulse condition such as specified in EIA-320-A. (If pulse test is not specified, thermal equilibrium dc test method correlation will be applicable. This may include pulse measurement intended to correlate to steady-state dc measurement as described in EIA-320-A.)

METHOD 5001.2

WAFER LOT ACCEPTANCE TESTING

*The content of this test method has been transferred to MIL-PRF-19500, APPENDIX D.