

The documentation and process conversion measures necessary to comply with this Notice shall be completed by 19 May 94.

NOTICE OF  
CHANGE

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MIL-STD-750C  
NOTICE 8  
19 November 1993

MILITARY STANDARD

TEST METHODS FOR SEMICONDUCTOR DEVICES

TO ALL HOLDERS OF MIL-STD-750C:

1. THE FOLLOWING PAGES OF MIL-STD-750C HAVE BEEN REVISED AND SUPERSEDE THE PAGES LISTED:

METHOD	NEW PAGE	DATE	SUPERSEDED PAGE	DATE
---	5	30 April 1992	5	REPRINTED WITHOUT CHANGE
---	5a	19 November 1993	5a	30 April 1992
---	13	19 November 1993	13	30 June 1993
---	14	19 November 1993	14	30 June 1993
---	15	19 November 1993	15	30 June 1993
---	16	19 November 1993	16	30 June 1993
---	17/18	19 November 1993	17/18	30 June 1993
2072.5	1	19 November 1993	1	30 April 1992
2072.5	2	30 April 1992	2	REPRINTED WITHOUT CHANGE
2076.2	5	19 November 1993	5	30 June 1993
2076.2	6	19 November 1993	6	30 June 1993

2. THE FOLLOWING TEST METHODS OF MIL-STD-750C HAVE BEEN REVISED AND SUPERSEDE THE TEST METHOD LISTED:

METHOD	DATE	SUPERSEDED METHOD	DATE
1039.4	19 November 1993	1039.3	30 August 1992
1042.3	19 November 1993	1042.2	30 August 1992
3101.1	19 November 1993	3101	30 April 1991
3477.1	19 November 1993	3477	30 August 1992
4031.3	19 November 1993	4031.2	30 April 1991

3. THE FOLLOWING NEW METHODS HAVE BEEN ADDED:

NEW METHOD	TITLE	DATE
3105	Measurement Method for Thermal Resistance of a Bridge Rectifier Assembly.	19 November 1993
4023	Scope Display.	19 November 1993

4. RETAIN THIS NOTICE AND INSERT BEFORE TABLE OF CONTENTS.

5. Holders of MIL-STD-750C will verify that page changes and additions indicated above have been entered. This notice page will be retained as a check sheet. This issuance, together with appended pages, is a separate publication. Each notice is to be retained by stocking points until the military standard is completely revised or canceled.

MIL-STD-750C  
NOTICE 8

CONCLUDING MATERIAL

Custodians:

Army - ER  
Navy - EC  
Air Force - 17  
NASA - NA

Review activities:

Army - AR, MI  
Navy - SH  
Air Force - 19, 85, 99  
DLA - ES

User activities:

Navy - AS, CG, MC, OS  
Air Force - 13

Preparing activity:

Navy - EC

Agent:

DLA - ES

(Project 5961-1336)

MIL-STD-750C  
NOTICE 8

## 4. GENERAL REQUIREMENTS

4.1 Test conditions. Unless otherwise specified herein or in the individual specification, all measurements and tests shall be made at thermal equilibrium at an ambient temperature of  $25 \pm 3^\circ\text{C}$  and at ambient atmospheric pressure and relative humidity and the specified test condition C (at environmentally elevated and reduced temperatures) shall have a tolerance of  $\pm 3$  percent or  $3^\circ\text{C}$ , whichever is greater. Whenever these conditions must be closely controlled in order to obtain reproducible results, the referee conditions shall be as follows: temperature  $25 \pm 1^\circ\text{C}$ , relative humidity  $50 \pm 5$  percent, and atmospheric pressure from 650 to 800 millimeters of mercury.

4.1.1 Permissible temperature variation in environmental chambers. When chambers are used, specimens under test shall be located only within the working area defined as follows:

- a. Temperature variation within working area: The controls for the chamber shall be capable of maintaining the temperature of any single reference point within the working area within  $\pm 2^\circ\text{C}$  or  $\pm 4$  percent, whichever is greater.
- b. Space variation within working area: Chambers shall be so constructed that, at any given time, the temperature of any point within the working area shall not deviate more than  $\pm 3^\circ\text{C}$  or  $\pm 3$  percent, whichever is greater, from the reference point, except for the immediate vicinity of specimens generating heat.
- c. Chambers with specified minimum temperatures (e.g., burn-in, life test, etc.): When test requirements involve a specified minimum test temperature, the controls and chamber construction shall be such that the temperature of any point within the working area shall not deviate more than  $+8, -0^\circ\text{C}$ ; or  $+8, -0$  percent, whichever is greater, from the specified minimum temperature, except for the immediate vicinity of the specimens generating heat.

4.1.2 Electrical test frequency. Unless otherwise specified, the electrical test frequency shall be  $1,000 \pm 25$  Hertz (Hz).

4.1.3 Accuracy. The specified limits are for absolute (true) values, obtained with the specified (nominal) test conditions. Proper allowance shall be made for measurement errors (including those due to deviations from nominal test conditions) in establishing the working limits to be used for the measured values, so that the true values of the device parameters (as they would be under nominal test conditions) are within the specified limits.

The following electrical test tolerances and precautions, unless otherwise specified in the applicable acquisition document, shall be maintained for all device measurements to which they apply (3000, 4000 series and other specified electrical measurements). Wherever test conditions are specified in the applicable acquisition document to a precision tighter than the tolerances indicated below, the specified conditions shall apply and take precedence over these general requirements.

- a. Bias conditions shall be held to within 3 percent of the specified value.

MIL-STD-750C  
NOTICE 8

- b. Input pulse characteristics, repetition rates, frequencies, etc., shall be held to within 10 percent. Nominal values should be chosen so that  $\pm 10$  percent variation (or the actual test equipment variation, if less than 10 percent) does not affect the accuracy or validity of the measurement of the specified value.
- c. Voltages applied in breakdown testing shall be held within 1 percent of specified value.
- d. Resistive loads shall be  $\pm 5$  percent tolerance.
- e. Capacitive loads shall be  $\pm 10$  percent or  $\pm 1$  picofarad tolerance, whichever is greater.
- f. Inductive loads shall be  $\pm 10$  percent or  $\pm 5$  microhenries tolerance, whichever is greater.
- g. Static parameters shall be measured to within 1 percent.
- h. Switching parameters shall be measured to within 5 percent or 1 nanosecond, whichever is greater.

4.1.3.1 Test methods and circuits. Unless otherwise stated in the specific test method, the methods and circuits shown are given as the basic measurement method. They are not necessarily the only method or circuit which can be used, but the manufacturer shall demonstrate to the acquiring activity that alternate methods or circuits which he may desire to use are equivalent and give results within the desired accuracy of measurement (see 4.1.3).

4.1.4 Calibration requirements. Calibration and certification procedures shall be provided in accordance with MIL-STD-45662 for plant standards and instruments used to measure or control production processes and semiconductor devices under test. For those measurements that are not traceable to the National Institute of Standards and Technology (NIST), correlation samples shall be maintained and used as the basis of proving acceptability when such proof is required. In addition, the following requirements shall apply:

- a. The accuracy of a calibrating instrument shall be at least four times greater than that of the item being calibrated, unless the item being calibrated is state of the art equipment, which may be near or equal in accuracy to the state of the art calibrating equipment, in which case the five time requirement does not apply. However, the instrument shall be calibrated to correlate with standards established by the National Bureau of Standards (NBS).
- b. Except in those cases where the National Institute of Standards and Technology (NIST) recommends a longer period and concurrence is obtained from the qualifying activity, calibration intervals for plant electrical standards shall not exceed one year, and for plant mechanical standards shall not exceed two years.

MIL-STD-750C  
NOTICE 8

## Numerical index of test methods

Method no.	Title
<u>Environmental tests (1000 series).</u>	
1001.1	Barometric pressure (reduced).
1011	Immersion.
1015	Steady-state primary photocurrent irradiation procedure (electron beam).
1016	Insulation resistance.
1017.1	Neutron irradiation.
1019.3	Steady-state total dose irradiation procedure.
1020.2	Electrostatic discharge sensitivity classification.
1021.1	Moisture resistance.
1022.4	Resistance to solvents.
1026.5	Steady-state operation life.
1027.3	Steady-state operation life (LTPD).
1031.5	High-temperature life (nonoperating).
1032.2	High-temperature (nonoperating) life (LTPD).
1036.3	Intermittent operation life.
1037.2	Intermittent operation life (LTPD).
1038.2	Burn-in (for diodes, rectifiers, and zeners).
*1039.4	Burn-in (for transistors).
1040	Burn-in (for thyristors (controlled rectifiers)).
1041.3	Salt atmosphere (corrosion).
*1042.3	Burn-in and life test for power MOSFET's or insulated gate bipolar transistors (IGBT).
1046.2	Salt spray (corrosion).
1048	Blocking life.
1049	Blocking life (LTPD).
1051.5	Temperature cycling (air to air).
1054.1	Potted environment stress test.
1055.1	Monitored mission temperature cycle.
1056.5	Thermal shock (liquid to liquid).
1061.1	Temperature measurement, case and stud.
1066.1	Dew point.
1071.6	Hermetic seal.
1018	Internal water-vapor content.
<u>Mechanical characteristics tests (2000 series).</u>	
2005.2	Axial lead tensile test.
2006	Constant acceleration.
2016.2	Shock.
2017.2	Die attach integrity.
2026.8	Solderability.
2031.2	Soldering heat.
2036.3	Terminal strength.
2037	Bond strength.
2046.1	Vibration fatigue.
2051.1	Vibration noise.
2052.2	Particle impact noise detection test.
2056	Vibration, variable frequency.
2057.1	Vibration, variable frequency (monitored).
2066	Physical dimensions.
2068	External visual for nontransparent, glass-encased, double plug, noncavity, axial leaded diodes.
2069	Pre-cap visual, power MOSFET's.
2070.1	Pre-cap visual microwave discrete and multichip transistors.
2071.2	Visual and mechanical examination.
*2072.5	Internal visual transistor (pre-cap) inspection.

MIL-STD-750C  
NOTICE 8

## Numerical index of test methods - Continued.

Method no.	Title
<u>Mechanical characteristics tests (2000 series) - Continued.</u>	
2073	Visual inspection for die (semiconductor diode).
2074.2	Internal visual inspection (discrete semiconductor diodes).
2075	Decap internal visual design verification.
*2076.2	Radiography.
2077.2	Scanning electron microscope (SEM) inspection of metallization.
2081	Forward instability, shock (FIST).
2082	Backward instability, vibration (BIST).
<u>Electrical characteristics tests for bipolar transistors (3000 series).</u>	
3001.1	Breakdown voltage, collector to base.
3005.1	Burnout by pulsing.
3011.2	Breakdown voltage, collector to emitter.
3015	Drift.
3020	Floating potential.
3026.1	Breakdown voltage, emitter to base.
3030	Collector to emitter voltage.
3036.1	Collector to base cutoff current.
3041.1	Collector to emitter cutoff current.
3051	Safe operating area (continuous dc).
3052	Safe operating area (pulsed).
3053	Safe operating area (switching).
3061.1	Emitter to base cutoff current.
3066.1	Base emitter voltage (saturated or nonsaturated).
3071	Saturation voltage and resistance.
3076.1	Forward-current transfer ratio.
3086.1	Static input resistance.
3092.1	Static transconductance.
<u>Circuit-performance and thermal resistance measurements (3100 series).</u>	
*3101.1	Thermal impedance testing of diodes.
3103	Thermal impedance measurements for insulated gate bipolar transistors.
3104	Thermal impedance measurements of GaAs MOSFET's (constant current forward-biased gate voltage method).
*3105	Measurements method for thermal resistance of a bridge rectifier assembly
3126	Thermal resistance (collector-cutoff-current method).
3131.2	Thermal impedance measurements for bipolar transistors (delta base-emitter method).
3132	Thermal resistance (dc forward voltage drop, emitter base continuous method).
3136	Thermal resistance (forward voltage drop, collector to base, diode method).
3141	Thermal response time.
3146.1	Thermal time constant.
3151	Thermal resistance, general.
3161	Thermal impedance measurements for vertical power MOSFET's (delta source-drain voltage method).
3181	Thermal resistance for thyristors.
<u>Low frequency tests (3200 series).</u>	
3201.1	Small-signal short-circuit input impedance.
3206.1	Small-signal short-circuit forward-current transfer ratio.
3211	Small-signal open-circuit reverse-voltage transfer ratio.
3216	Small-signal open-circuit output admittance.

MIL-STD-750C  
NOTICE 8

## Numerical index of test methods - Continued.

Method no.	Title
<u>Low frequency tests (3200 series) - Continued</u>	
3221	Small-signal short-circuit input admittance.
3231	Small-signal short-circuit output admittance.
3236	Open circuit output capacitance.
3240.1	Input capacitance (output open-circuited or short-circuited).
3241	Direct interterminal capacitance.
3246.1	Noise figure.
3251.1	Pulse response.
3255	Large signal power gain.
3256	Small signal power gain.
3261.1	Extrapolated unity gain frequency.
3266	Real part of small-signal short circuit input impedance.
<u>High frequency tests (3300 series)</u>	
3301	Small-signal short-circuit forward-current transfer-ratio cutoff frequency.
3306.3	Small-signal short-circuit forward-current transfer ratio.
3311	Maximum frequency of oscillation.
3320	Power output, RF power gain, and collector efficiency.
<u>Electrical characteristics tests for MOS field-effect transistors (3400 series)</u>	
3401.1	Breakdown voltage, gate to source.
3403.1	Gate to source voltage or current.
3404	MOSFET threshold voltage.
3405.1	Drain to source on-state voltage.
3407.1	Breakdown voltage, drain to source.
3411.1	Gate reverse current.
3413.1	Drain current.
3415.1	Drain reverse current.
3421.1	Static drain to source on-state resistance.
3423	Small-signal, drain to source on-state resistance.
3431	Small-signal, common-source, short-circuit, input capacitance.
3433	Small-signal, common-source, short-circuit, reverse-transfer capacitance.
3453	Small-signal, common-source, short-circuit, output admittance.
3455	Small-signal, common-source, short-circuit, forward transadmittance.
3457	Small-signal, common-source, short-circuit, reverse transfer admittance.
3459	Pulse response (FET).
3461	Small-signal, common-source, short-circuit, input admittance.
3469	Repetitive unclamped inductive switching.
3470.2	Single pulse unclamped inductive switching.
3471.1	Gate charge.
3472.2	Switching time test.
3473.1	Reverse recovery time ( $t_{rr}$ ) and recovered charge ( $Q_{rr}$ ) for power MOSFET body diode and for fast, ultra-fast power rectifiers.
3474.1	Safe operating area (SOA) for power MOSFET's or insulated gate bipolar transistors (IGBT).
3475.1	Forward transconductance (pulsed dc method) for power MOSFET's or insulated gate bipolar transistors (IGBT).
3476	Commutating diode for safe operating area test procedure for measuring $dv/dt$ during reverse recovery of power MOSFET transistors or insulated gate bipolar transistors (IGBT).
*3477.1	Measurement of total switching losses of an insulated gate bipolar transistor (IGBT).

MIL-STD-750C  
NOTICE 8

## Numerical index of test methods - Continued.

Method no.	Title
<u>Electrical characteristics tests for MOS field-effect transistors (3400 series) - Continued</u>	
3478.1	Power transistor electrical dose rate test method.
3479	Short circuit withstand time.
3490	Clamped inductive switching safe operating area for MOS gate power transistors.
<u>Electrical characteristics tests for Gallium Arsenide transistors (3500 series)</u>	
3501	Breakdown voltage, drain to source.
3575	Forward transconductance.
3505	Associated gain.
<u>Electrical characteristics tests for diodes (4000 class).</u>	
4001.1	Capacitance.
4011.4	Forward voltage (source-drain diode).
4016.3	Reverse current leakage.
4021.2	Breakdown voltage (diodes).
4022	Breakdown voltage (voltage regulators and voltage-reference diodes).
*4023	Scope display.
4026.2	Forward recovery voltage and time.
*4031.3	Reverse recovery time.
4036.1	"Q" for voltage variable capacitance diodes.
4041.2	Rectification efficiency.
4046.1	Reverse current, average.
4051.3	Small-signal reverse breakdown voltage impedance.
4056.2	Small-signal forward impedance.
4061.1	Stored charge.
4066.3	Surge current.
4071.1	Temperature coefficient of breakdown voltage.
4076.1	Saturation current.
4081.2	Thermal resistance of lead mounted diodes (forward voltage, switching method).
<u>Electrical characteristics tests for microwave diodes (4100 series)</u>	
4101.3	Conversion loss.
4102	Microwave diode capacitance.
4106	Detector power efficiency.
4111.1	Figure of merit (current sensitivity).
4116.1	Intermediate frequency (IF) impedance.
4121.2	Output noise ratio.
4126.2	Overall noise figure and noise figure of the IF amplifier.
4131.1	Video resistance.
4136.1	Standing wave ratio.
4141.1	Burnout by repetitive pulsing.
4146.1	Burnout by single pulse.
4151	Rectified microwave diode current.



MIL-STD-750C  
NOTICE 8

## Numerical index of test methods - Continued.

Method no.	Title
<u>Electrical characteristics tests for thyristors (controlled rectifiers) (4200 series)</u>	
4201.2	Holding current.
4206.1	Forward blocking current.
4211.1	Reverse blocking current.
4216	Pulse response.
4219	Reverse gate current.
4221.1	Gate-trigger voltage or gate-trigger current.
4223	Gate-controlled turn-on time.
4224	Circuit-commutated turn-off time.
4225	Gate-controlled turn-off time.
4226.1	Forward "on" voltage.
4231.2	Exponential rate of voltage rise.
<u>Electrical characteristics tests for tunnel diodes (4300 series)</u>	
4301	Junction capacitance.
4306.1	Static characteristics of tunnel diodes.
4316	Series inductance.
4321	Negative resistance.
4326	Series resistance.
4331	Switching time.
<u>High reliability space application tests (5000 class)</u>	
5001.1	Wafer lot acceptance testing.
5002	Capacitance-voltage measurements to determine oxide quality.
5010	Clean room and workstation airborne particle classification and measurement.

MIL-STD-750C  
NOTICE 8

## METHOD 1039.4

## BURN-IN (FOR TRANSISTORS)

1. Purpose. This test is performed to eliminate marginal devices or those with defects resulting from manufacturing aberrations that are evidenced as time and stress dependent failures. Without the burn-in, these defective devices would be expected to result in early lifetime failures under normal use conditions. It is the intent of this test to operate the semiconductor device at specified conditions to reveal electrical failure modes that are time and stress dependent.

2. Procedure. The semiconductor device shall be subjected to the burn-in at the temperature and for the time specified herein. Preburn-in measurements shall be made as applicable. The failure criteria shall be as specified.

2.1 Mounting. Devices with leads projecting from the body shall be mounted by their leads at least 1/4-inch (6.4 mm) from the seating plane. Devices with studs or case shall be mounted by the stud or case, unless otherwise specified.

2.1.1 Test condition A, steady-state reverse bias. The transistor primary blocking junction, as specified, shall be reverse biased for 48 hours minimum, except PNP bipolar transistors shall be 24 hours, at the ambient temperature specified (normally 150°C) and at 80 percent of its maximum rated collector-base voltage. For bipolar transistors, the  $V_{CB}$  bias is not to exceed the maximum collector-emitter voltage rating. For field-effect transistors (signal or low power), the gate to source voltage, with drain to source shorted, shall be as specified. At the end of the high-temperature test time, specified herein, the ambient temperature shall be lowered. The test voltage shall be maintained on the devices until  $T_C = 30^\circ\text{C} \pm 5^\circ\text{C}$  is attained. After room ambient temperature has been established, the bias voltage shall be removed. After removal of the bias voltage, no other voltage shall be applied to the device before taking the post burn-in reverse-current measurement(s). After burn-in voltage is removed, post burn-in measurements shall be completed within 24 hours, unless otherwise specified. If measurements cannot be performed within the specified time, the devices shall be subjected to the same test conditions for a minimum of 24 additional hours before post test measurements are performed.

2.1.2 Test condition B, steady-state power. All devices shall be operated at the maximum rated power related to the test temperature for 160 hours minimum at the specified test conditions (excluding microwave).

- a. For bipolar transistors, the temperature and power shall be specified. Unless otherwise specified, the temperature shall be as follows:  
 $T_A = 30^\circ\text{C} \pm 5^\circ\text{C}$  for small signal, switching, and medium power devices intended for printed circuit board mounting;  $T_J =$  maximum rated temperature,  $+0^\circ\text{C}$ ,  $-25^\circ\text{C}$ , for devices intended for chassis or heat sink mounting. Case temperature burn-in at maximum ratings (typically  $T_C = 100^\circ\text{C}$ ) may be substituted on the chassis or heat sink mounted devices at the supplier's option. If the voltage conditions specified herein cause the safe operating area rating to be exceeded, then the voltage shall be decreased until the safe operating area rating is met while maintaining the full rated power condition. For microwave bipolar transistors, the temperature, voltage, and current shall be as specified in the detail specification.
- b. For unijunction and field-effect (signal and low power) transistors, the temperature, voltage, and current shall be as specified.
- c. Post burn-in measurements shall be as specified.
- d. Post burn-in readings shall be taken within 96 hours, unless otherwise specified. If measurements cannot be performed within the specified time, the devices shall be subjected to the same test conditions for a minimum of 24 additional hours before post test measurements are performed.

MIL-STD-750C  
NOTICE 8

3. Summary. Test condition letter and the following conditions shall be specified in the detail specification:

3.1 Test condition A:

- a. Junction to be reverse biased (see 2.1.1).
- b. Gate to source voltage for field-effect transistors (see 2.1.1).
- c. Test temperature (see 2.1.1).
- d. Test time for field-effect transistors (see 2.1.1).
- e. Voltage for post burn-in reverse current measurement (see 2.1.1).
- f. Time for completion of post burn-in measurements, if other than 24 hours (see 2.1.1).
- g. Criteria for failure (see 2.).

3.2 Test condition B:

- a. Test temperature, if other than as specified in 2.1.2.
- b. Test conditions (see 2.1.2).
- c. Power for bipolar transistors (see 2.1.2).
- d. Voltage and current for unijunction and field-effect transistors (see 2.1.2).
- e. Preburn-in and post burn-in measurements (see 2.1.2).
- f. Time for completion of post burn-in measurements, if other than as specified in 2.1.2.
- g. Criteria for failure (see 2.).

MIL-STD-750C  
NOTICE 8

## METHOD 1042.3

BURN-IN AND LIFE TEST FOR POWER MOSFET's OR  
INSULATED GATE BIPOLAR TRANSISTORS (IGBT)

1. Purpose. Test conditions A, B, and C are performed to eliminate marginal devices or those with defects resulting from manufacturing aberrations that are evidenced as time and stress failures under normal use conditions. Test condition D is performed to eliminate marginal lots with manufacturing defects. For the IGBT, replace the drain and source MOSFET designations with collector and emitter IGBT designations, D = C and S = E.

2. Procedure. The semiconductor device shall be subjected to the burn-in at the temperature and for the time specified herein. Preburn-in measurements shall be made as applicable. The failure criteria shall be as specified.

2.1.1 Test condition A, steady-state reverse bias. All devices shall be operated at 80 percent of the maximum rated drain to source voltage at the specified test temperature for 160 hours minimum, at the specified test conditions. The drain to source voltage, with gate to source shorted, shall be as specified. At the end of the high-temperature test time, specified herein, the ambient temperature shall be lowered. The burn-in voltage shall be maintained on the devices until  $T_C = 30^\circ\text{C} \pm 5^\circ\text{C}$  is attained. The interruption of bias for up to one minute for the purpose of moving devices to cool down positions separate from the chamber within which life testing was performed shall not be considered removal of bias.

After removal of the burn-in voltage, no other voltage shall be applied to the device before taking the post burn-in reverse current measurement(s). After burn-in voltage is removed, post burn-in measurements shall be completed within 96 hours, unless otherwise specified. (See figure 1042-1.) Unless otherwise specified, the burn-in temperature shall be  $T_A = 150^\circ\text{C}$ . The  $V_{DS}$  burn-in voltage shall be as follows. For IGBT devices, burn-in temperature shall be  $T_J = 150^\circ\text{C} - 15^\circ\text{C}$  to  $+0^\circ\text{C}$ , and test time shall be 96 hours minimum.

If $V_{(BR)DSS}$ is 20 V	$V_{DS}$ shall be 16 V
30 V	24 V
40 V	32 V
60 V	48 V
80 V	64 V
90 V	72 V
100 V	80 V
120 V	96 V
150 V	120 V
170 V	136 V
200 V	160 V
240 V	192 V
350 V	280 V
400 V	320 V
450 V	360 V
500 V	400 V
600 V	480 V

$V_{(BR)DSS}$  voltages in between shall revert to the next lower  $V_{DS}$  burn-in voltage.

2.1.1.1 Temperature accelerated test details. In an accelerated test devices are subjected to bias conditions at a temperature exceeding the maximum rated junction temperature. The maximum ambient temperature for MOSFETs is  $175^\circ\text{C}$  for a minimum of 48 hours. It is recommended that an adequate sample of devices be exposed to the high temperature while measuring the voltage(s) and current(s) of the devices to assure that the applied stresses do not induce damaging overstress. An adequate sample which has completed the accelerated test should also be subjected to a 1,000 hour steady state reverse bias at standard test conditions to assure the devices have not been deleteriously affected. Details of the accelerated test will be found in the detail and/or general specification.

Supersedes method 1042.2 of Notice 5

Method 1042.3  
19 November 1993

MIL-STD-750C  
NOTICE 8

2.1.2 Test condition B, steady-state gate bias. All devices shall be operated at 80 percent of the maximum rated gate to source voltage at the specified temperature for a minimum of 48 hours. (See figure 1042-2.) For MOS power transistors, the temperature and voltage shall be as specified. Unless otherwise specified, the temperature ( $T_A$ ) shall be 150°C.

If maximum rated $V_{GS}$ is 10 V	Burn-in voltage ( $V_{GS}$ ) shall be 8 V
15 V	12 V
20 V	16 V
30 V	24 V
40 V	32 V

$V_{GS}$  voltages in between shall revert to the next lower voltage.

2.1.3 Test condition C, steady-state power. All devices shall be operated at the maximum junction temperature +0°C, -24°C by means of applying power to the device while maintaining an ambient temperature of 25°C +10°C, -5°C. The junction temperature shall be verified by means of measuring junction temperature using the change in body diode voltage drop or calculated by applying the following equations:

$$T_J = R_{\theta JA} \times P_D + T_A \quad \text{Not heat sink used}$$

$$T_J = R_{\theta JC} \times P_D + T_C \quad \text{Heat sink used}$$

$T_C$  = Temperature of case

$T_A$  = Ambient air temperature

$T_S$  = Temperature of heat sink

$$P_D = V_{DS} \times I_D$$

$V_{DS}$  = Drain-source voltage

$I_D$  = Drain-source current

Note: The power indicated by the safe operating curve shall not be exceeded.

2.1.4 Test condition D, intermittent power. 1/ All devices shall be subjected to the number of cycles as specified. A cycle shall consist of applying power to the device for the time necessary to achieve a 100°C +15°C, -10°C minimum rise in junction temperature followed by an off period for the time necessary for the junction to cool. Forced air cooling is permitted during the off period only.

The power level, power-on time, and heat sink used, if any, shall be chosen to ensure that at the end of the heating cycle, the case temperature is not more than 15°C below the junction temperature. The rise in junction temperature during the on period shall be verified by means of measuring junction temperature using the change in body diode voltage drop or calculated by applying the following equations.

$$\Delta T_J = P_T R_{\theta JA} (1 - \text{Exp} - t/T_p) \text{ where } P_T = V_{DS} I_D$$

$T_p$  = thermal time constant of device package, and the heat sink used.

$t$  = heating time,  $R_{\theta JA}$  = thermal resistance junction to ambient, for the period of heating time specified, of the device and any necessary heat sink used.

This test is intended to allow the case temperature to rise and fall appreciably as the junction is heated and cooled; thus, it is not appropriate to use a large heat sink or a high power short pulse.

1/ This test condition is destructive.

MIL-STD-750C  
NOTICE 8

3. Summary. Test condition letter and the following details shall be specified in the individual specification.

3.1 Test condition A.

- a. Drain to source voltage for MOS power field-effect transistors ( $V_{DS}$ ) (see 2.1.1).
- b. Test temperature, if other than specified in 2.1.1.
- c. Test time, if other than specified in 2.1.1.
- d. Voltage for post burn-in reverse current measurement (see 2.1.1).
- e. Criteria for failure.

3.2 Test condition B.

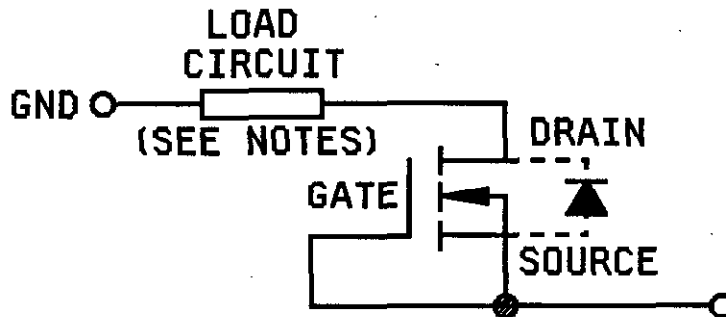
- a. Test temperature, if other than as specified in 2.1.2.
- b. Test conditions (see 2.1.2).
- c. Voltage for MOS power field-effect transistors (see 2.1.2).
- d. Preburn-in and post burn-in measurements.
- e. Criteria for failure.

3.3 Test condition C.

- a. Ambient temperature and thermal resistance (see 2.1.3).
- b. Voltage and current, if other than specified in 2.1.3.
- c. Preburn-in and post burn-in measurements.
- d. Total test time (see 2.1.3).
- e. Criteria for failure.

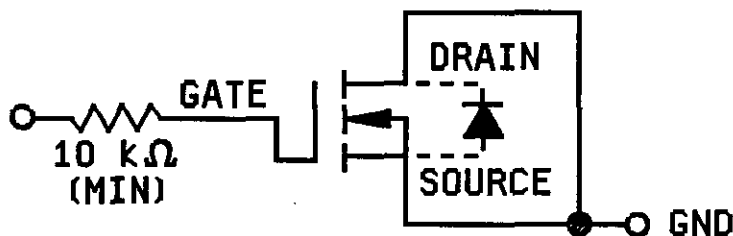
3.4 Test condition D.

- a. Ambient temperature (if one is desired) and thermal resistance (see 2.1.4).
- b. Voltage and current, if other than specified in 2.1.4.
- c. Pretest and post test measurements.
- d. Number of cycles (see 2.1.4).
- e. Criteria for failure.
- f. Minimum heating time.

MIL-STD-750C  
NOTICE 8

## NOTES:

1. The load circuit shall be selected or designed to ensure that the voltage across the load circuit of each acceptable device shall not exceed 10 percent of the specified test voltage. The load circuit may be a resistor, fuse, or circuit which:
  - a. Protects the power supply.
  - b. Isolates the defective devices from the other devices under test.
  - c. Insures a minimum of 98 percent of the specified test voltage is applied across the DUT.
2. If the circuit does not maintain bias on a failed device, then means must be provided to identify that device.

FIGURE 1042-1. High temperature reverse bias test circuit.FIGURE 1042-2. High temperature gate bias circuit.

MIL-STD-750C  
NOTICE 8

## METHOD 2072.5

## INTERNAL VISUAL TRANSISTOR (PRE-CAP) INSPECTION

1. Purpose. The purpose of this inspection is to verify the construction and workmanship of bipolar transistors, field effect transistors, discrete monolithic, multichip, and multijunction devices excluding microwave and selected RF devices. This test will be performed prior to capping or encapsulation to detect those devices with internal defects that could lead to failures in normal application and verify compliance with the requirements of the applicable detail specification.

2. Apparatus. The apparatus for this inspection shall consist of the following.

2.1 Optical equipment capable of the specified magnifications.

2.2 Light sources of sufficient intensity to adequately illuminate the devices being inspected.

2.3 Adequate fixturing for handling the devices being inspected without causing damage.

2.4 Adequate covered storage and transportation containers to protect devices from mechanical damage and environmental contamination.

2.5 Any visual standards (drawings and photographs) necessary to enable the inspector to make objective decisions as to the acceptability of the devices being examined.

3. Definitions.

3.1 Glassivation. The top layer of transparent insulating material that covers the active circuit area metallization, but excluding bonding pads.

3.2 Passivation. Silicon oxide, nitride, or other insulating material that is grown or deposited directly on the die prior to the deposition of any metal.

4. Procedure.

4.1 General. The device shall be examined in a suitable sequence of observations within the specified magnification range to determine compliance with the requirements of the applicable detail specification and the criteria of the specified test condition. If a specified visual inspection requirement is in conflict with the topology or construction of a specific device design, alternate inspection criteria may be included in the detail specification. Any alternate inspection criteria contained in the detail specification shall take precedence over the criteria of this test method. Any criteria of this test method intended for a specific device process or technology has been indicated. Where applicable, unused cells shall not be subjected to internal visual criteria.

a. Sequence of inspection. The order in which criteria are presented is not a required order of examination and may be varied at the discretion of the manufacturer. Visual criteria specified in 4.1.1, 4.1.2, 4.1.3, and 4.1.7, may be examined prior to die attachment with reexamination at low or high magnification after die attachment for these criteria. Visual criteria specified in 4.1.6.2 and 4.1.6.3 may be examined prior to lead wire bonding without reexamination after bonding.

b. Inspection control. Within the time interval between visual inspection and preparation for sealing, devices shall be stored in a controlled environment (one which controls airborne particle count and relative humidity). The use of an inert gas environment, such as dry nitrogen shall satisfy the requirements for storing in a controlled environment. Devices examined in accordance with this test method shall be inspected and stored in a class 100,000 environment, in accordance with FED-STD-209, except that the maximum allowable relative humidity shall not exceed 65 percent.



MIL-STD-750C  
NOTICE 8

If devices are subjected to a high temperature bake (>100°C) immediately prior to sealing, the humidity control is not required. Devices shall be in covered containers when transferred from one controlled environment to another, unless a cleaning operation is performed prior to sealing.

- c. Magnification. High magnification inspection shall be performed perpendicular to the die surface with normal incident illumination. Low magnification inspection shall be performed with either a monocular, binocular, or stereo microscope, and the inspection performed within any appropriate angle, with the device under suitable illumination. The inspection criteria of 4.1.4 and 4.1.6.1 may be examined at "high magnification" at the manufacturer's option. High power magnification may be used to verify a discrepancy noted at a low power.

TABLE I. Die magnification requirements.

* Chip size	High magnification	Low magnification
30 mils or less	100 to 200X	30 to 50X
31 to 60 mils	75 to 150X	30 to 50X
61 to 150 mils	35 to 120X	10 to 30X
greater than 150 mils	25 to 75X	10 to 30X

\* Length of shortest dimension.

- d. Reinspection. When inspection for product acceptance or quality verification of the visual requirements herein is conducted subsequent to the manufacturer's successful inspection, the additional inspection may be performed at any magnification specified herein, unless a specific magnification is required by the detail specification. If sampling is used rather than 100 percent reinspection, reevaluation of lot quality in accordance with the "Reevaluation of lot quality" of MIL-S-19500 shall be used.
- e. Exclusions. If conditional exclusions have been allowed, specific instruction as to the location and conditions for which the exclusion can be applied shall be documented in the assembly inspection drawing.

4.1.1 Die metallization defects (high magnification). A die which exhibits any of the following defects shall be rejected.

4.1.1.1 Metallization, scratches, and voids exposing underlying material (see figure 2072-1).

- a. A scratch or void that severs the innermost metallized guard ring.
- b. Any die containing a void in the metallization at the bonding pad covering more than 25 percent of the pad area.

MIL-STD-750C  
NOTICE 8

- a. Flat pack and dual-in-line (see figure 2076-5).
1. Any lead wire that appears to touch or cross another lead wire or bond (Y plane only).
  2. Any lead wire that deviates from a straight line from bond to external lead and appears to be within 0.002 inch (0.0508 mm) of another bond (Y plane only).
  3. Lead wires that do not deviate from a straight line from bond to external lead and appear to touch another wire or bond (Y plane only).
  4. Any lead wire that touches or is less than 0.002 inch (0.0504 mm) from the case or external lead to which it is not attached (X and Y plane).
  5. Any bond that is less than 0.001 inch (0.0254 mm) (excluding bonds connected by a common conductor) from another bond (Y plane only).
  6. Any wire making a straight line run (with no arc) from die bonding pad to package post.
- b. Round or "box" transistor type (see figure 2076-6).
1. Any lead wire that touches or is less than 0.002 inch (0.0504 mm) from the case or external lead to which it is not attached (X and Y plane).
  2. Lead wires that stay below an imaginary plane across the top of the bond (X plane only).
  3. Any lead wire that appears to touch or cross another lead wire or bond (Y plane only) if bonded to different electrical elements.
  4. Any lead wire that deviates from a straight line from bond to external lead appears to touch or to be within 0.002 inch (0.0504 mm) of another wire or bond (Y plane only).
  5. Any bond that is less than 0.001 inch (0.0254 mm) (excluding bonds connected by a common conductor) from another bond (Y plane only).
  6. Any wire making a straight line run (with no arc) from die bonding pad to package post, unless specifically designed in this manner (e.g., clips, rigid connecting leads, or heavy power leads).
  7. Any internal post that is bent more than 10 degrees from the vertical (or intended design position) or is not uniform in length and construction or comes closer than one post diameter to another post.
  8. Any post in a low profile case (such as a TO-46) which comes closer to the top of the case than 20 percent of the total inside dimension between the header and the top of the case. Any device in which the semiconductor element is vertical to the header, and comes closer than 0.002 inch (0.0508 mm) to the header or to any part of the case.

MIL-STD-750C  
NOTICE 8

c. Axial lead type (see figure 2076-7).

1. Whisker embedded with glass body wall.
2. Whisker tilted more than 5 degrees in any direction from the device lead axis or deformed to the extent that it touches itself.
3. Either half of an S or C bend whisker that is compressed so that any dimension is reduced to less than 50% of its design value. On diodes with whiskers metallurgically bonded to the post and to the die, the whisker may be deformed to the extent that it touches itself, if the minimum whisker clearance zone specified in figure 2076-7a, is maintained for metal packages.
4. Whiskerless construction device with plug displacement distance more than one-fourth of the diameter of the plug with respect to the central axis of the device.
5. Semiconductor element mounting tilted more than 15 degrees from normal to the main axis of the device.
6. Die hanging over edge of header or pedestal more than 20 percent of the die contact area by design.
7. Less than 75 percent of the semiconductor element base area is bonded to the mounting surface.
8. Voids in the welds which reduce the lead to plug connection by more than 25 percent of the total weld area.
9. Devices with package deformities such as, body glass cracks, incomplete seals (voids, position of glass, etc.), die chip outs, and severe misalignment of S- and C-shaped whisker connections to die or post that exceed the limits of the applicable visual inspection requirements.

3.9.3 Encapsulated non-cavity assemblies of discrete devices. External to the individual devices, the encapsulating material shall be examined and rejected for the following defects.

3.9.3.1 Extraneous material. Extraneous matter of any shape with any dimension exceeding 0.020 inches. Also, any two adjacent particles of such matter with total dimensions exceeding 0.030 inches.

4. Summary. The following conditions shall be specified in the applicable detail specification.

- a. Number of views, if other than indicated in 3.1.1 and 3.1.1.1.
- b. Radiograph submission, if applicable (see 3.8.2).
- c. Marking, if other than indicated in 3.3 and marking of samples to indicate they have been radiographed, if required (see 3.3.3).
- d. Sample defects and criteria for acceptance or rejection, if other than indicated in 3.9.
- e. Radiograph and report retention, if applicable (see 3.8.3).
- f. Test reports when required.

MIL-STD-750C  
NOTICE 8

## METHOD 3101.1

## THERMAL IMPEDANCE TESTING OF DIODES

1. Purpose. The purpose of this test is to determine the thermal performance of diode devices. This can be done in two ways, steady-state thermal impedance and/or thermal transient testing. Steady-state thermal impedance (referred to as thermal resistance) determines the overall thermal performance of devices. A production-oriented screening process, referred to as thermal transient testing, is a subset of thermal impedance testing and determines the ability of the diode chip-to-header interface to transfer heat from the chip to the header, and is a measure of the thermal quality of the die attachment. It is relevant to designs which use headers, or heat conducting plugs, with mass and thermal conductivity allowing effective discrimination of poor die attachments. This is particularly true with power devices. The method can be applied to rectifier diodes, transient voltage suppressers, power zener diodes, and some zener, signal and switching diodes. This method is intended for production monitoring, incoming inspection, and pre-burn in screening applications.

1.1 Background and scope for thermal transient testing. Steady-state thermal response (thermal resistance) and thermal transient response (related to and often called thermal impedance or thermal transient impedance) of semiconductor devices are sensitive to the presence of these voids in the die attachment material between the semiconductor chip and package since voids impede the flow of heat from the chip to the substrate (package). Due to the difference in the thermal time constants of the chip and package, the measurement of transient thermal response can be made more sensitive to the presence of voids than can the measurement of steady-state thermal response. This is because the chip thermal time constant is generally several orders of magnitude shorter than that of the package. Thus, the heating power pulse width can be selected so that only the chip and the chip-to-substrate interface are heated during the pulse by using a pulse width somewhat greater than the chip thermal time constant but less than that of the substrate. Heating power pulse widths ranging from 1 to 400 milliseconds for various package designs have been found to satisfy this criterion. This enables the detection of voids to be greatly enhanced, with the added advantage of not having to heatsink the device under test. Thus, the transient thermal response technique is less time-consuming than the measurement of thermal resistance for use as a manufacturing screen, process control, or incoming inspection measure for die attachment integrity evaluation.

2. Definitions. The following symbols and terminology shall apply for the purpose of this test method.

- a.  $V_F$  The forward biased junction voltage of the device-under-test (DUT) used for junction temperature sensing.
  - $V_{Fi}$  The initial  $V_F$  value before application of heating power.
  - $V_{Ff}$  The final  $V_F$  value after application of heating power.
- b.  $\Delta V_F$  The change in the temperature sensitive parameter,  $V_F$ , due to the application of heating power to the DUT.
- c.  $I_H$  The current applied to the DUT during the heating time in order to cause power dissipation.
- d.  $V_H$  The heating voltage resulting from the application of  $I_H$  to the DUT.
- e.  $P_H$  The heating power pulse magnitude; product of  $V_H$  and  $I_H$ .
- f.  $t_H$  The duration of  $P_H$  applied to the DUT.
- g.  $I_M$  The measurement current used to forward bias the temperature sensing diode junction for measurement of  $V_F$ .

MIL-STD-750C  
NOTICE 8

- h.  $t_{MD}$  Measurement delay time is defined as the time from the start of heating power ( $P_H$ ) removal to the start of the final  $V_F$  measurement time, referred to as  $t_{SW}$ .
- i.  $t_{SW}$  Sample window time during which final  $V_F$  measurement is made. The value of  $t_{SW}$  should be small; it can approach zero if an oscilloscope is used for manual measurements.
- j. VTC Voltage-temperature coefficient of  $V_F$  with respect to  $T_J$  at a fixed value of  $I_H$ ; in  $mV/^\circ C$ .
- k. K Thermal calibration factor equal to the reciprocal of VTC; in  $^\circ C/mV$ .
- l. CU The comparison unit, consisting of  $\Delta V_F$  divided by  $V_H$ , that is used to normalize the transient thermal response for variations in power dissipation; in units of  $mV/V$ .
- m.  $T_J$  The device-under-test junction temperature.
- n.  $\Delta T_J$  The change in  $T_J$  caused by the application of  $P_H$  for a time equal to  $t_H$ .
- o.  $Z_{\Theta JX}$  Thermal impedance from device junction to a time defined reference point; in units of  $^\circ C/W$ .  
 $Z_{\Theta JC}$  Thermal impedance from device junction to a point on the outside surface of the case immediately adjacent to the device chip measured using time equal time constant of device; in units of  $^\circ C/W$ .
- p.  $R_{\Theta JX}$  Thermal resistance from device junction to a defined reference point; in units of  $^\circ C/W$ . Also shown as  $\Theta_{JX}$  in publications.  
 $R_{\Theta JC}$  Thermal resistance from device junction to a point on the outside surface of the case immediately adjacent to the device chip; in units of  $^\circ C/W$ . Also shown as  $\Theta_{JC}$  in publications.  
 $R_{\Theta JA}$  Thermal resistance from device junction to a ambient (world); in units of  $^\circ C/W$ . Also shown as  $\Theta_{JA}$  in publications.

3. Apparatus. The apparatus required for this test shall include the following, configured as shown on figure 3101-1, as applicable to the specified test procedure:

3.1 A constant current source capable of adjustment to the desired value of  $I_H$  and able to supply the  $V_H$  value required by the DUT. The current source should be able to maintain the desired current to within  $\pm 2\%$  during the entire length of heating time.

3.2 A constant current source to supply  $I_H$  with sufficient voltage compliance to turn the TSP junction fully on.

3.3 An electronic switch capable of switching between the heating period conditions and measurement conditions in a time frame short enough to avoid DUT cooling during the transition; this typically requires switching in the microsecond or tens of microseconds range.

MIL-STD-750C  
NOTICE 8

3.4 A voltage measurement circuit capable of accurately making the  $V_{Ff}$  measurement within the time frame with millivolt resolution.

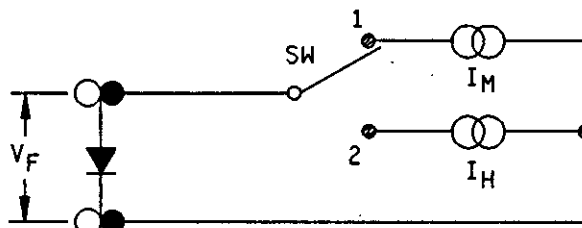


FIGURE 3101-1. Thermal impedance testing setup for diodes.

#### 4. Test operation.

4.1 General description. The test begins with the adjustment of  $I_M$  and  $I_H$  to the desired values. The value of  $I_H$  is usually at least 50 times greater than the value of  $I_M$ . Then with the electronic switch in position 1, the value of  $V_{Fi}$  is measured. The switch is then moved to position 2 for a length of time equal to  $t_H$  and the value of  $V_H$  is measured. Finally, at the conclusion of  $t_H$ , the switch is again moved to position 1 and the  $V_{Ff}$  value is measured within a time period defined by  $t_{MD}$  (or  $t_{MD}$  plus  $t_{SW}$ , depending on the definitions stated previously). The two current sources are then turned off at the completion of the test.

The voltage and current waveforms for all three time periods of the test are shown below on figure 3101-2.

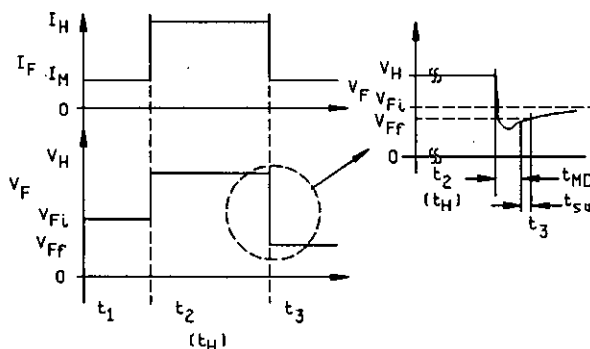


FIGURE 3101-2. Thermal impedance testing waveforms.

METHOD 3101.1

MIL-STD-750C  
NOTICE 84.2 Notes.

4.2.1 Some test equipment may provide a  $\Delta V_F$  directly instead of  $V_{Fi}$  and  $V_{Ff}$ ; this is an acceptable alternative. Record the value of  $\Delta V_F$ .

4.2.2 Some test equipment may provide a  $\Theta_{jx}$  directly instead of  $V_{Fi}$  and  $V_{Ff}$  for thermal resistance calculations; this is an acceptable alternative. Record the value of  $\Theta_{jx}$ .

4.2.3 Alternative waveforms, as may be generated by automatic test equipment using the general principles of this method, may be used upon approval of the qualifying activity.

5. Acceptance Limit.

5.1 General discussion. Variations in diode characteristics from one manufacturer to another cause difficulty in establishing a single acceptance limit for all diodes tested to a given specification. Ideally, a single acceptance limit value for  $\Delta V_F$  would be the simplest approach. However, different design, materials, and processes can alter the resultant  $\Delta V_F$  value for a given set of test conditions. Listed below are several different approaches to defining acceptance limits. The  $\Delta V_F$  limit is the simplest approach and is usually selected for screening purposes. 5.3 through 5.6 require increasingly greater detail or effort.

5.2  $\Delta V_F$  Limit. A single  $\Delta V_F$  limit is practical if the K factor and  $V_H$  values for all diodes tested to a given specification are nearly identical. Since these values may be different for different manufacturers, the use of different limits is likely to more accurately achieve the desired intent. (A lower limit does not indicate a better die bond when comparing different product sources.) 34e diode specifications would list the following test conditions and measurement parameters:

$I_H$  (in A)

$t_H$  (in ms)

$I_M$  (in mA)

$t_{HD}$  (in  $\mu s$ )

$t_{SW}$  (in  $\mu s$ )

$\Delta V_F$  (maximum limit value, in mV)

5.3  $\Delta T_J$  Limit. (Much more involved than  $\Delta V_F$  but useful for examining questionable devices.)

Since  $\Delta T_J$  is the product of K (in accordance with 6.) and  $\Delta V_F$ , this approach is the same as defining a maximum acceptable junction temperature rise for a given set of test conditions.

5.4 CU Limit. (Slightly more involved than  $\Delta T_J$ .)

The  $\Delta T_J$  limit approach described above does not take into account potential power dissipation variations between devices. The  $V_H$  value can vary, depending on chip design and size, thus causing the power dissipation during the heating time to be different from device to device. This variation will be small within a lot of devices produced by a single manufacturer but may be large between manufacturers. A CU limit value takes into account variations in power dissipation due to differences in  $V_H$  by dividing the  $\Delta V_F$  value by  $V_H$ .

MIL-STD-750C  
NOTICE 8

## 5.5 (K.CU) Limit. (Slightly more involved but provides greater detail.)

This is a combinational approach that takes into account both K factor and power dissipation variations between devices.

5.6  $Z_{\theta JX}$  Limit. (For full characterization; not needed for screening purposes.)

The thermal impedance approach uses an absolute magnitude value specification that overcomes the problems associated with the other approaches. Thermal impedance is time dependant and is calculated as follows:

$$Z_{\theta JX} = \frac{\Delta T_J}{P_D} = \frac{|(K)(\Delta V_F)|}{|(I_H)(V_H)|}$$

5.7  $R_{\theta JX}$  Limit. (For thermal resistance specification testing.)

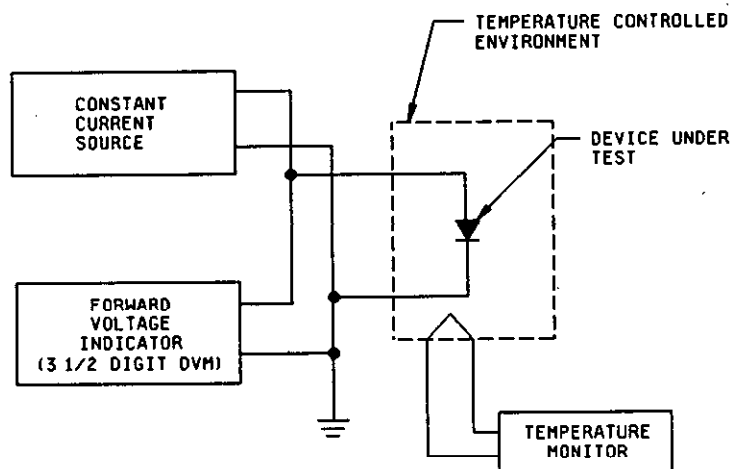
The thermal resistance to some defined point, such as the case, is an absolute magnitude value specification used for equilibrium conditions. The  $t_h$  heating time must therefore be extended to appreciably longer times (typically 20 to 50 seconds). In the example of  $R_{\theta JC}$  measurements, the case must be carefully stabilized and monitored in temperature which requires an infinite heat sink for optimum results. The  $\Delta T_J$  is the difference in junction temperature to the case temperature for the example of  $R_{\theta JC}$ .

$$R_{\theta JX} = \frac{\Delta T_J}{P_D} = \frac{|(K)(\Delta V_F)|}{|(I_H)(V_H)|} \text{ } ^\circ\text{C/W}$$

5.8 General comment for thermal transient testing. One potential problem in using the thermal transient testing approach lies in trying to make accurate enough measurements with sufficient resolution to distinguish between acceptable and nonacceptable diodes. As the diode-under-test current handling capability increases, the thermal impedance under transient conditions will become a very small value. This raises the potential for rejecting good devices and accepting bad ones. Higher  $I_H$  values must be used in this case.

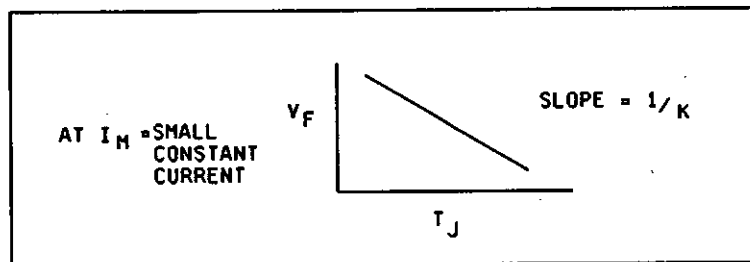
6. Measurement of the temperature sensitive parameter  $V_F$ . The calibration of  $V_F$  versus  $T_J$  is accomplished by monitoring  $V_{SD}$  for the required value of  $I_M$  as the environmental temperature (and thus the DUT temperature), and is varied by external heating. It is not required if the acceptance limit is  $\Delta V_F$  (see 5.2), but is relevant to the other acceptance criteria (see 5.3 through 5.6). The magnitude of  $I_M$  shall be chosen so that  $V_F$  is a linearly decreasing function over the normal  $T_J$  range of the device.  $I_M$  must be large enough to ensure that the diode junction is turned on but not large enough to cause significant self-heating. An example of the measurement method and resulting calibration curve is shown on figure 3101-3.



MIL-STD-750C  
NOTICE 8

Step 1: Measure  $V_{F1}$  at  $T_{J1}$  using  $I_M$   
 Step 2: Measure  $V_{F2}$  at  $T_{J2}$  using  $I_M$

Step 3: 
$$K = \frac{|T_{J2} - T_{J1}|}{|V_{F2} - V_{F1}|} \text{ } ^\circ\text{C/mV}$$



$I_M$  must be large enough to overcome surface leakage effects but small enough not to cause significant self-heating.

$T_J$  is externally applied - via oven, liquid, etc. - environment.

FIGURE 3101-3. Example curve of  $V_F$  versus  $T_J$ .

A calibration factor  $K$  (which is the reciprocal of the slope of the curve on figure 3101-3) can be defined as:

$$K = \frac{|T_{J2} - T_{J1}|}{|V_{F2} - V_{F1}|} \text{ } ^\circ\text{C/mV}$$

It has been found experimentally that the  $K$ -factor variation for all devices within a given device type class is small. The usual procedure is to perform a  $K$  factor calibration on a 10 to 12 piece sample from a device lot and determine the average  $K$  and standard deviation ( $\sigma$ ). If  $\sigma$  is less than or equal to 3 percent of the average value of  $K$ , then the average value of  $K$  can be used for all devices within the lot. If  $\sigma$  is greater than 3 percent of the average value of  $K$ , then all the devices in the lot shall be calibrated and the individual values of  $K$  shall be used in determining device acceptance.

MIL-STD-750C  
NOTICE 8

7. Establishment of test conditions and acceptance limits. Thermal resistance measurements require that  $I_H$  be equal to the required value stated in the device specifications, typically at rated current or higher. Values for  $t_H$ ,  $t_{MD}$ , and heat sink conditions are also taken from the device specifications. The steps shown below are primarily for thermal transient testing and thermal characterization purposes.

The following steps describe how to set up the test conditions and determine the acceptance limits for implementing the transient thermal test for die attachment evaluation using the apparatus and definitions of above.

7.1 Initial device testing procedure. The following steps describe in detail how to set up the apparatus described previously for proper testing of various diodes. Since this procedure thermally characterizes the diode out to a point in heating time required to ensure heat propagation into the case (i.e., the  $\Theta_{JX}$  condition), an appropriate heat sink should be used or the case temperature should be monitored.

Step 1: From a 20 to 25 piece sample, pick any one diode to start the setup process. Set up the test apparatus as follows:

- $I_H = 1.0 \text{ A}$  (Or some other desired value near the device-under-test's (DUTs) normal operating current.)
- $t_H = 10\text{-}50 \text{ ms}$  (for most devices rated up to 15 W power dissipation), unless otherwise specified.
- 50 - 250 ms (for most devices rated up to 200 W power dissipation), unless otherwise specified.
- $\geq 250 \text{ ms}$  for steady state thermal resistance measurement. The pulse must be shown to correlate to steady state conditions before it can be substituted for steady state condition.
- $t_{MD} = 100 \mu\text{s max}$  (larger value may be required on power devices with magnetic package elements which generate nonthermally induced transients; this would be observed in the  $t_3$  region of figure 3101-2) unless otherwise specified.
- $I_M = 10 \text{ mA}$  (Or some nominal value approximately 1/50, or less, of  $I_H$ .)

Step 2: Insert device into the apparatus test fixture and initiate a test. (For best results, a test fixture that offers some form of heat sinking would be desirable. Heat sinking is not needed if either the power dissipation during the test is well within the diode's free-air rating or the maximum heating time is limited to less than that required for the heat to propagate through the case.)

Step 3: If  $\Delta V_F$  is in the 5 to 80 mV range, then proceed to the next step. This range approximately corresponds to a junction temperature change of roughly 10°C to 20°C and is sufficient for initial comparison purposes.

If  $\Delta V_F$  is less than 5 mV, return to step 1 and increase heating power into device by increasing  $I_H$ .

If  $\Delta V_F$  is greater than 80 mV, approximately corresponding to a junction temperature change greater than 40°C, it would probably be desirable to reduce the heating power by returning to step 1 and reducing  $I_H$ .

NOTE: The test equipment shall be capable of resolving  $\Delta V_F$  to within 5 percent. If not, a higher value of  $\Delta V_F$  must be selected until the 5 percent tolerance is met.

MIL-STD-750C  
NOTICE 8

Note that two different devices can have the same junction temperature rise even when  $P_H$  is different, due to widely differing  $V_H$ . Within a given lot, however, a higher  $V_H$  is more likely to result in a higher junction temperature rise. For such examples this screen can be more accurately accomplished using the CU value. As defined in 2., CU provides a comparison unit that takes into account different device  $V_H$  values for a given  $I_H$  test condition.

Step 4: Test each of the sample devices and record the  $\Delta V_F$  and CU data.

Step 5: Select out the devices with the highest and lowest values of CU and put the remaining devices aside.

The  $\Delta V_F$  values can be used instead of CU if the measured values of  $V_H$  are very tightly grouped around the average value.

Step 6: Using the devices from step 5, collect and plot the heating curve data for the two devices in a manner similar to the examples shown on figure 3101-4.

Step 7: Interpretation of the heating curves is the next step. Realizing that the thermal characteristics of identical chips should be the same if the heating time ( $t_H$ ) is less than or equal to the thermal time constant of the chip, the two curves should start out the same for the low values of  $t_H$ . Nonidentical chips (thinner or smaller in cross section) will have completely different curves, even at the smaller values of  $t_H$ . As the value of  $t_H$  is increased, thereby overcoming the chip thermal constant, heat will have propagated through the chip into the die attachment region. Since the heating curve devices of step 5 were specifically chosen for their difference, the curves of figure 3101-4 diverge after  $t_H$  reaches a value where the die attachment variance has an affect on the device junction temperature. Increasing  $t_H$  further will probably result in a flattening of the curve as the heating propagates in the device package. If the device package has little thermal mass and is not well mounted to a good heat sink, the curve will not flatten very much, but will show a definite change in slope.

Step 8: Using the heating curve, select the appropriate value of  $t_H$  to correspond to the inflection point in the transition region between heat in the chip and heat in the package.

If there are several different elements in the heat flow path: chip, die attachment, substrate, substrate attach, and package for example in a hybrid: there will be several plateaus and transitions in the heating curve. Appropriate selection of  $t_H$  will optimize evaluation sensitivity to other attachment areas.

Step 9: Return to the apparatus and set  $t_H$  equal to the value determined from step 8.

MIL-STD-750C  
NOTICE 8

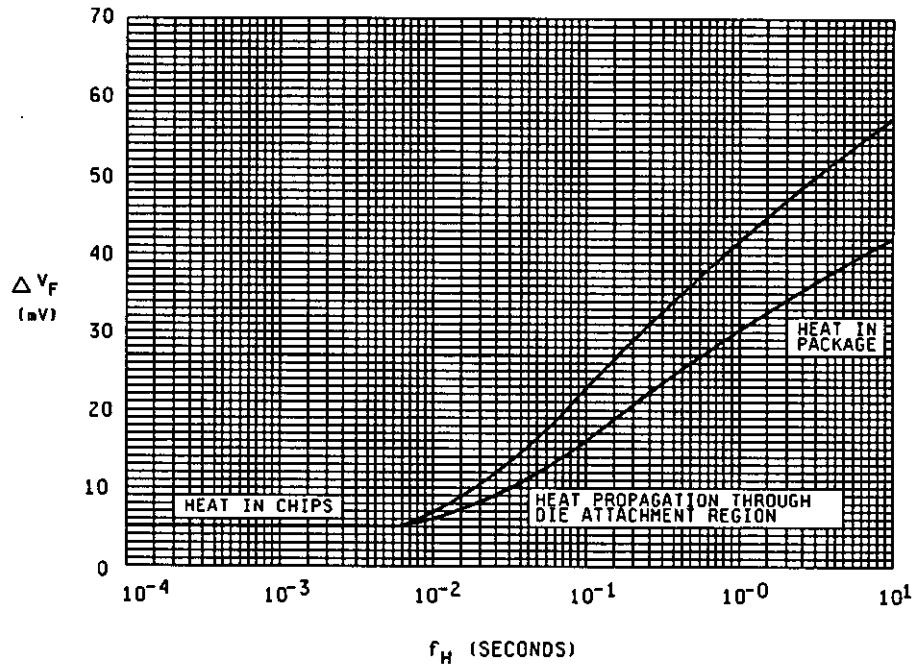


FIGURE 3101-4. Heating curves for two extreme devices.

METHOD 3101.1

MIL-STD-750C  
NOTICE 8

- Step 10: Because the selected value of  $t_H$  is much less than that for thermal equilibrium, it is possible to significantly increase the heating power without degrading or destroying the device. The increased power dissipation within the device under test will result in higher  $\Delta V_F$  and/or CU values that will make determination of acceptable and nonacceptable devices much easier.
- Step 11: The pass/fail limit, the cut-off point between acceptable and nonacceptable devices, can be established in a variety of ways:

- a. Correlation to other die attachment evaluation methods, such as die shear and/or X-ray, while these two methods have little actual value from a thermal point of view, they do represent standardization methods as described in MIL-STD specifications.
- b. Maximum allowable junction temperature variations between devices, since the relationship between  $\Delta T_J$  and  $\Delta V_F$  and is about  $0.5^\circ\text{C}/\text{mV}$ , the junction temperature spread between devices can be easily determined. The  $T_J$  predicts reliability. Conversely, the  $T_J$  spread necessary to meet the reliability projections can be translated to a  $\Delta V_F$  and/or CU value for pass/fail criteria.

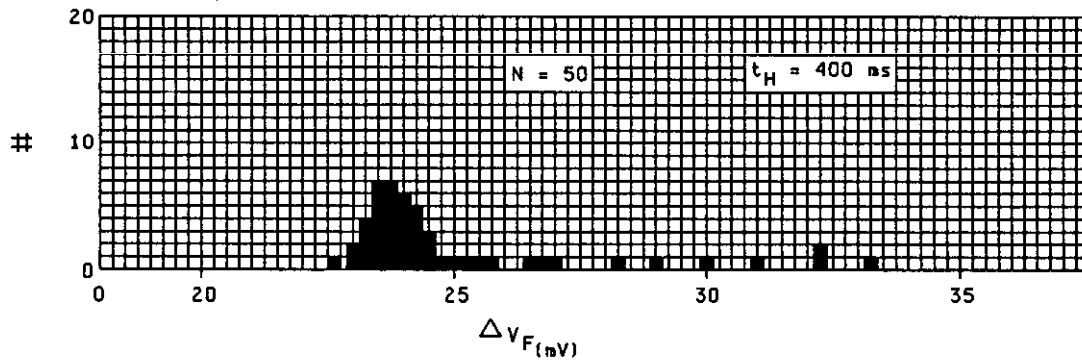
To fully utilize this approach, it will be necessary to calibrate the devices for the exact value of the  $T_J - V_F$  characteristic. The characteristic's slope, commonly referred to as K factor, is easily measured on a sample basis using a voltmeter, environmental chamber, temperature indicator, and a power supply setup for forcing, temperature indicator and a power supply setup as described in 6. A simple set of equations yield the junction temperature once K and  $\Delta V_F$  are known:

$$\Delta T_J = (K) (\Delta V_F)$$

$$T_J = T_A + \Delta T_J$$

Where  $T_A$  is the ambient or reference temperature. For thermal transient test conditions, this temperature is usually equivalent to lead temperature ( $T_L$ ) for axial lead devices or case temperature ( $T_C$ ) for case mounted devices.

- c. Statistically from a 20 to 25 device sample; the distribution of  $\Delta V_F$  or CU values should be a normal one with defective devices out of the normal range. Figure 3101-5 shows a  $\Delta V_F$  distribution for a sample lot of diodes. Note that the left-hand side of the histogram envelope is fairly well defined but the other side is greatly skewed to the right. This comes about because the left-hand side is constrained by the absolutely best heat flow that can be obtained with a given chip assembly material and process. The other side has no such constraints because there is no limit as to how poorly a chip is mounted.

MIL-STD-750C  
NOTICE 8FIGURE 3101-5. Typical  $\Delta V_F$  distribution.

The usual rule of thumb in setting the maximum limit for  $\Delta V_F$  or CU is to use the distribution average value and one standard deviation ( $\sigma$ ): i.e.:

$$(\Delta V_F) \Big|_{\substack{\text{high} \\ \text{limit}}} = \Delta V_F + X \sigma$$

$$(CU) \Big|_{\substack{\text{high} \\ \text{limit}}} = CU + X \sigma$$

Where  $X = 3$  in most cases.

The statistical data required is obtained by testing 25 or more devices under the conditions of step 11.

The maximum limit determined from this approach should be correlated to the diode's specified thermal resistance. This will insure that the  $\Delta V_F$  or CU limits do not pass diodes that would fail the thermal resistance requirement.

Step 12: Once the test conditions and pass/fail limit have been determined, it is necessary only to record this information for future testing requirements of the same device in the same package.

MIL-STD-750C  
NOTICE 8

The steps listed hereto are conveniently summarized on figure 3101-6.

General description		Steps	Comments
A	Initial setup	1 through 4	Approximate instrument settings to find variations among devices in 10 to 15 piece sample.
B	Heating curve generation	5 through 6	Using highest and lowest reading devices, generate heating curves.
C	Heating curve interpretation	7 through 9	Heating curve is used to find more appropriate value for $t_H$ corresponding to heat in the die attachment area (or some other desired interface in the heat flow path).
D	Final setup	10	Heating power applied during $t_H$ is increased in order to improve measurement sensitivity to variations among devices.
E	Pass-fail determination	11 through 12	A variety of methods is available for setting the fail limit; the statistical approach is the fastest and easiest to implement.

FIGURE 3101-6. Summary of test procedure steps.

7.2 Routine device thermal transient testing procedure. Once the proper control settings have been determined for a particular device type from a given manufacturing process or vendor, repeated testing of that device type simply requires that the same test conditions be used as previously determined.

New device types or the same devices manufactured with a different process will require a repeat of 7.1 for proper thermal transient test conditions.

8. Test conditions and measurements to be specified and recorded.

8.1 Thermal transient and equilibrium measurements.

8.1.1 Specify the following test conditions:

- a.  $I_M$  measuring current \_\_\_\_\_ mA
- b.  $I_H$  heating current \_\_\_\_\_ A
- c.  $t_H$  heating time \_\_\_\_\_ ms
- d.  $t_{MD}$  measurement time delay \_\_\_\_\_  $\mu$ s
- e.  $t_{SW}$  sample window time \_\_\_\_\_  $\mu$ s

METHOD 3101.1

MIL-STD-750C  
NOTICE 8

## 8.1.2 Record the following data:

- a.  $V_{Fi}$  initial forward voltage \_\_\_\_\_ V
- b.  $V_H$  heating voltage \_\_\_\_\_ V
- c.  $V_{Ff}$  final forward voltage \_\_\_\_\_ V

(Note: Some test equipment may provide a  $\Delta V_F$  instead of  $V_{Fi}$  and  $V_{Ff}$ ; this is an acceptable alternative. Record the value of  $\Delta V_F$ .)

Some test equipment may provide direct display of calculated CU and/or  $\Theta_{JX}$ ; this is an acceptable alternative. Record the value of CU and/or  $\Theta_{JX}$ .)

8.2 K factor calibration. (Optional for criteria 8.3a or 8.3b, mandatory for 8.3c, d, or e.)

## 8.2.1 Specify the following test conditions:

- a.  $I_M$  current magnitude \_\_\_\_\_ mA
- b. Initial junction temperature \_\_\_\_\_ °C
- c. Initial  $V_F$  voltage \_\_\_\_\_ mV
- d. Final junction temperature \_\_\_\_\_ °C
- e. Final  $V_F$  voltage \_\_\_\_\_ mV

## 8.2.2 Calculate K factor in accordance with the following equation:

$$K = \frac{|T_{J1} - T_{J2}|}{|V_{F1} - V_{F2}|} \text{ } ^\circ\text{C/mV}$$

- a. K factor \_\_\_\_\_ °C/mV

8.3 Specification limit calculations. One or more of the following should be measured and/or calculated, as called for on the device specification (see 5.1);

- a.  $\Delta V_F$  \_\_\_\_\_ mV
- b. CU \_\_\_\_\_ mV/V
- c.  $\Delta T_J$  \_\_\_\_\_ °C
- d.  $K \cdot CU$  \_\_\_\_\_ °C/V
- e.  $Z_{\Theta JX}$  \_\_\_\_\_ °C/W
- f.  $\Theta_{JX}$  \_\_\_\_\_ °C/W



MIL-STD-750C  
NOTICE 8

## METHOD 3105

MEASUREMENT METHOD FOR THERMAL RESISTANCE  
OF A BRIDGE RECTIFIER ASSEMBLY

1. Purpose. This method describes a means to cause current to flow alternately through the legs of a single-phase or three-phase bridge assembly under condition to make it feasible to determine its effective thermal resistance. The bridge is operated under steady-state  $I_0$  conditions and the current in each leg is interrupted while readings are taken from which to calculate thermal resistance.

2. Definitions. The following symbols and terminology shall apply for the purposes of this test method:

a. $V_F$ - - - - -	The forward-biased junction voltage of the device under test (DUT) used for junction temperature sensing. For a bridge, this applies to individual legs (i.e., one ac to one dc terminal).
b. $V_{F1}$ - - - - -	The forward voltage at room temperature at $I_{REF}$ .
c. $V_{F2}$ - - - - -	The forward voltage at $I_{REF}$ and 100°C above that at $V_{F1}$ .
d. $V_{F3}$ - - - - -	The initial $V_F$ value at $I_{REF}$ before the application of heating power, with the device at rated case temperature.
e. $V_{F4}$ - - - - -	The final $V_F$ value at $I_{REF}$ after stabilization of temperatures due to the application of rated current at rated case temperature.
f. $\Delta V_F$ - - - - -	The change in the temperature sensitive parameter $V_F$ , due to the application of heating power to the DUT, in volts.
g. $V_{FH}$ - - - - -	The maximum forward voltage resulting from the application of $I_0$ to the DUT.
h. $I_0$ - - - - -	The rated average current applied to the DUT.
i. $I_{REF}$ - - - - -	The measurement current used to forward-bias the temperature sensing diode junction for measurement of $V_F$ .
j. TCVF - - - - -	Voltage-temperature coefficient of $V_F$ with respect to $T_J$ at a fixed value of $I_{REF}$ , in V/°C.
k. $T_J$ - - - - -	The DUT junction temperature.
l. $\Delta T_J$ - - - - -	The change in $T_J$ caused by the application of $I_0$ .
m. TSP - - - - -	The temperature-sensitive parameter ( $V_F$ ).
n. $T_N$ - - - - -	Reference case temperature for measuring $V_N$ , when N = 1, 2, 3, or 4.
o. $R_{thJX}$ - - - - -	Thermal resistance from device junction to a defined reference point (e.g. lead or ambient), in units of °C/W.
p. $R_{thJC}$ - - - - -	Thermal resistance from device junction to a defined reference point on the outside surface of the case, in units of °C/W.
q. $t_{F4}$ - - - - -	Step trace time.
r. $V_{AC}$ - - - - -	Bridge input AC voltage per leg.

MIL-STD-750C  
NOTICE 8

3. Test circuit. The apparatus required for this test shall include the following, configured as shown on figures 1 and 2.

- a. A source of 60 hertz, single or three phase sine wave (AC) capable of being adjusted to the desired value of  $I_0$  and able to supply the  $V_{FH}$  value required by the DUT. The current source should be able to maintain the desired current to within  $\pm 2$  percent during the entire time needed for temperature stabilization and measurements.
- b. A constant-current source to supply  $I_{REF}$  with sufficient compliance voltage range to turn on fully the junction of the diode leg being measured.
- c. Anti-parallel fast recovery rectifier diodes with ratings exceeding  $I_0$ , to provide isolation of the high-current source from  $I_{REF}$  during commutation of  $I_0$  between legs.
- d. A voltage measurement circuit capable of accurately making the  $V_F$  measurements within the available time interval (when the anti-parallel diodes are not conducting), with millivolt resolution.

4. Procedure. Refer to figures 1 and 2, test circuits for single- and three-phase bridges.

- a. With  $S_1$  open, and DUT at  $20^\circ\text{C}$  to  $30^\circ\text{C}$  (temperature  $T_1$ ), read  $V_{F1}$  of each leg at current  $I_{REF}$ . Elevate the device temperature to  $100^\circ\text{C}$  above temperature  $T_1$  (temperature  $T_2$ ). Allow the device to stabilize until the junction temperature is at  $T_2$ . Read  $V_{F2}$  of each leg at  $I_{REF}$  current. Compute the TCVF of each leg as follows:

$$\text{TCVF} = (V_{F1} - V_{F2}) / 100^\circ\text{C}$$

$$V_{F2} \text{ computed at } T_1 + (100^\circ\text{C})$$

Compute the expected  $V_{F2A}$  at  $T_j = \text{maximum rated}$  as follows:

$$V_{F2A} = V_{F1} - [(\text{TCVF}) \times (T_{J\text{max}} - T_1)]$$

$$V_{F2A} \text{ computed at } T_{J\text{max}}$$

Determine the average TCVF and the standard deviation of the TCVF from the readings on each leg. If the standard deviation is less than or equal to 3 percent of the average value of TCVF, TCVF may be used for all devices. If the standard deviation is greater than 3 percent of the average value of TCVF, then the individual values of TCVF shall be used in determining the performance of the bridge.

- b. With the device held at  $T_3$ , at or below rated case temperature of  $I_0$ , close  $S_1$  and read  $V_{F3}$  for each leg.
- c. After closing  $S_1$ , adjust the power source and/or the load resistor to obtain the maximum rated  $I_0$  (either  $I_{01}$  or  $I_{02}$ , depending on the rated  $T_c$  selected) and readjust the case temperature to the chosen rated value. Allow the device to achieve stable junction temperatures (see note 1).
- d. Measure  $V_{F4}$  (see figure 3) for each leg at the same reference current ( $\pm 1\%$ ) as in steps a and b. (The instrumentation used to measure  $V_{F4}$  must have sufficient resolution to read it within 2 mV or 2%).

NOTE: If  $V_{F3}$  for the leg is greater than  $V_{F2}$ ,  $T_j$  is less than  $T_{J\text{max}}$ .

- e. Measure  $V_{FH}$  for each leg.

MIL-STD-750C  
NOTICE 8

f. Compute thermal resistance as follows:

1. Compute  $\Delta V_F = V_{F4} - V_{F3}$  for each leg.

2. Compute

$$\Delta T_J = \frac{\Delta V_F}{TCVF}, \text{ see note 1.}$$

3. Compute  $R_{thJC}$  of the full bridge;

$$R_{thJC} = \frac{\Delta T_{JC}}{I_O \times 2V_{FH}}, \text{ where } \Delta T_J \text{ is the average of all legs. } V_{FH} \text{ is the average of all legs and } I_O \text{ is the rectified output current of the full bridge. See notes 2, 3, and 4.}$$

## NOTES:

1. If, under power, the case is held to  $T_4$ , slightly above  $T_3$ , a corrected  $\Delta T_J$  ( $\Delta T_{J(corr)}$ ) =  $\Delta T_{JC} - (T_4 - T_3)$  should be used for step f.2.
2. Step f.3 gives  $R_{th}$  for the bridge. The average per-leg  $R_{th}$  for a single-phase bridge is four times the value; six times for a three-phase bridge (see note 3).
3. If desired,  $R_{th}$  of individual legs may be computed from the individual values of  $\Delta T_{JC}$  and  $V_{FH}$ .
4. The power dissipated  $I_O \times 2V_{FH}$  is a reasonable approximation.

5. Test condition to be specified.

$I_O$  \_\_\_\_\_

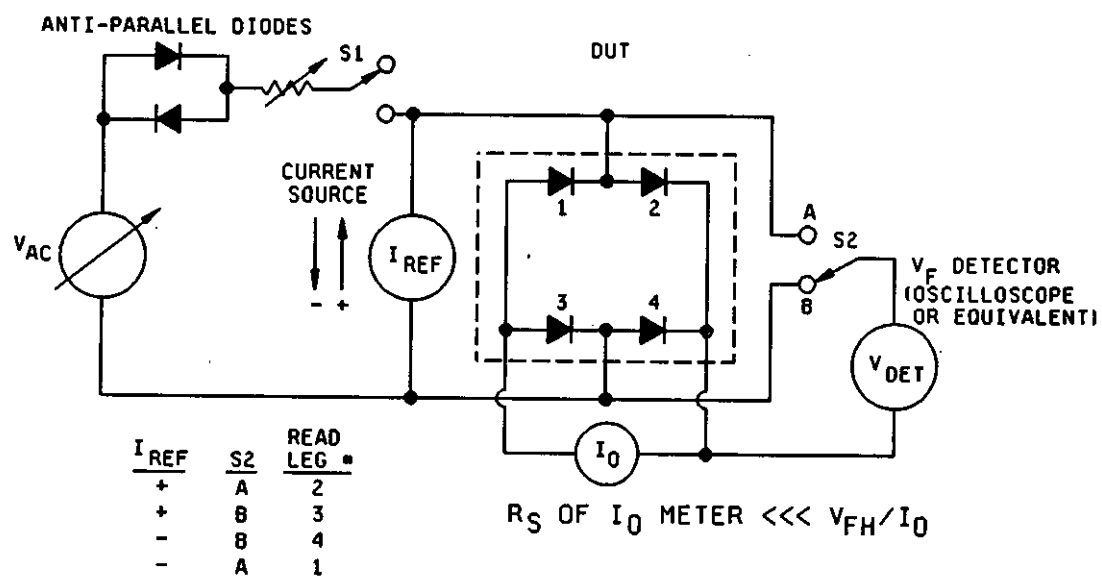
$T_C$  \_\_\_\_\_

$I_{REF}$  \_\_\_\_\_

Frequency (if other than 60 Hz) \_\_\_\_\_

6. Characteristics to be determined:

Steady state thermal resistance. Junction to case (unless otherwise specified): \_\_\_\_\_ °C/W.

MIL-STD-750C  
NOTICE 8

NOTE: All voltage measurements shall be made using leads Kelvin - connected directly to the bridge terminals

FIGURE 1. Single phase bridge.

MIL-STD-750C  
NOTICE 8

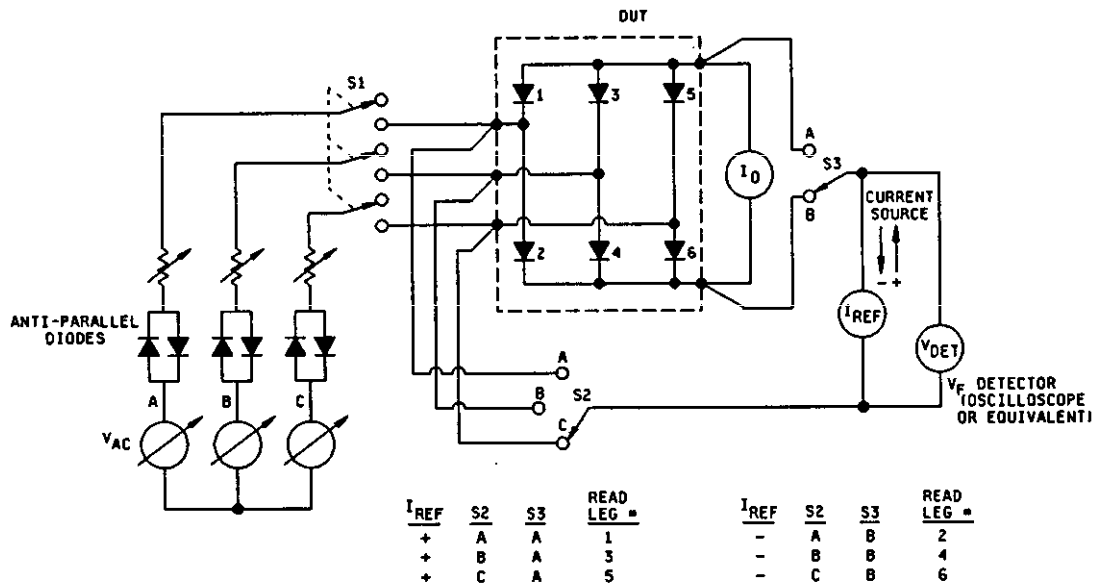
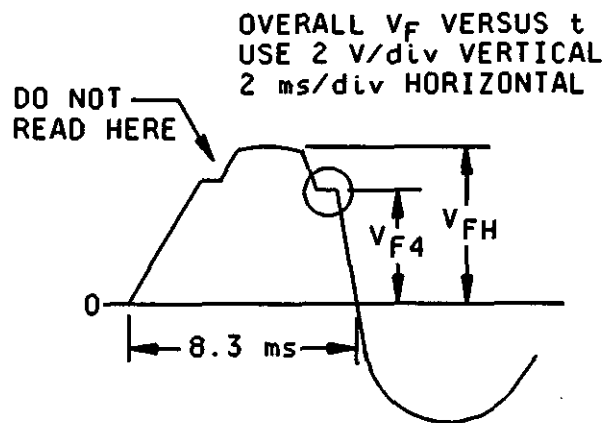


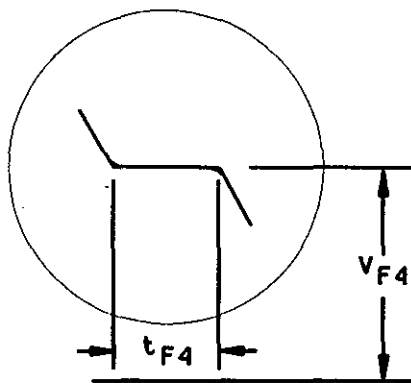
FIGURE 2. Three phase bridge.

MIL-STD-750C  
NOTICE 8

NOTE:  $V_{F4}$  "step trace" is provided when anti-parallel diodes in circuit briefly commutate off (I AC passes through zero during each cooling cycle of individual bridge legs under AC test conditions).

OSCILLOSCOPE DISPLAYS

EXPANDED AND CHOPPED  
 $V_F$  VERSUS  $t$ . USE 5 OR  
10 mV/div VERTICAL,  
20 OR 50  $\mu$ s/div HORIZONTAL



## NOTES:

1. Polarity shown applies when  $I_{REF}$  is positive. The trace is inverted when  $I_{REF}$  is negative.
2.  $V_{AC}$  is adjusted so that the  $V_{F4}$  step ( $t_{F4}$ ) shown in figure 3 is  $100\mu$ s  $\pm$  50 $\mu$ s and is clearly defined. A typical  $V_{AC}$  might be 10 volts peak. Bridges with parasitic inductive components must adjust  $V_{AC}$  so that after the inductive ringing settles. The  $V_{F4}$  step in figure 3 ( $t_{F4}$ ) is  $100\mu$ s  $\pm$  50 $\mu$ s.

FIGURE 3. Oscilloscope displays.

MIL-STD-750C  
NOTICE 8

## METHOD 3477.1

MEASUREMENT OF INSULATED GATE BIPOLAR TRANSISTOR (IGBT)  
TOTAL SWITCHING LOSSES AND SWITCHING TIMES

1. Purpose. This method defines the basic test circuitry and waveform definitions by which to measure the total switching losses of an insulated gate bipolar transistor (IGBT).

2. Scope. This method applies only to measurements of IGBT devices without an integral diode.

3. Definitions.

- a.  $V_{(BR)CES}$  Collector/emitter breakdown voltage.
- b.  $I_{CE}$  Test current.
- c.  $V_{GE}$  Gate to emitter voltage.
- d.  $R_G$  Gate drive series resistance
- e.  $V_{CL}$  Clamp voltage (80 percent rated  $V_{(BR)CES}$ ).
- f.  $t_0$  Time point where  $V_{GE}$  is at 10 percent of the specified gate drive.
- g.  $t_1$  Time point where  $i_{CE} = 5$  percent  $I_{CE}$  (max).
- h.  $t_2$  Time point where  $v_{CE} = 5$  percent  $V_{CL}$  when  $v_{CE}$  decreasing.
- i.  $t_3$  Time point where  $v_{CE} = 5$  percent  $V_{CL}$  when  $v_{CE}$  increasing.
- j.  $t_4$   $t_3 + 5 \mu s$ .
- k.  $t_{d(on)}$  Turn on delay time.
- l.  $t_r$  Rise time.
- m.  $t_{d(off)}$  Turn off delay time.
- n.  $t_f$  Fall time.
- o.  $W_{ON}$  Turn on switching losses.
- p.  $W_{OFF}$  Turn off switching losses.
- q.  $W_{TOT}$  Total switching losses.
- r.  $T_j$  Semiconductor junction temperature.
- s.  $V_G$  Gate drive voltage.

4. Circuitry. Figure 3477-1 shows the basic test circuit. The circuit has to satisfy two fundamental requirements.

- a. The circuit reflects the losses that are attributed to the IGBT only and is independent from those due to other circuit components, like the freewheeling diode.

MIL-STD-750C  
NOTICE 8

- b. The operation of the circuit shown on figure 3477-1 is as follows:

The driver IGBT builds the test current in the inductor. When it is turned off, current flows in the zener. At this point, the switching time and switching energy test begins, by turning on and off the device under test (DUT). In its switching, the DUT will see the test current that is flowing into the inductor and the voltage across the zener, without any reverse recovery component from a freewheeling diode. This test can exercise the IGBT to its full voltage and current without any spurious effect due to diode reverse recovery.

Input drive duty cycles should be chosen such that  $T_j$  is not affected. Control of  $T_j$  is best done using external methods.

5. Method. Figure 3477-2 shows the DUT current and voltage waveforms and test points.

- 5.1 Energy loss during turn on. During turn on, the energy loss is defined as follows:

$$(1) W_{on} = \int_{t_1}^{t_2} i_{CE} \cdot v_{CE} dt \text{ joules/pulse}$$

Refer to figure 3477-2 for  $t_1$  and  $t_2$

- 5.2 Energy loss during turn off. During turn off, the energy loss is defined as follows:

$$(2) W_{off} = \int_{t_3}^{t_4} i_{CE} \cdot v_{CE} dt \text{ joules/pulse}$$

Refer to figure 3477-2 for  $t_3$  and  $t_4$

- 5.3 Total switching loss. The total switching loss is the sum of equations (1) and (2).

$$(3) W_{TOT} = W_{ON} + W_{OFF} \text{ joules/pulse}$$

- 5.4 Switching time measurements. Switching time measurements while not the preferred method of delineating between devices may be determined using the rules below and as seen in figure 3477-2.

- |                 |  |
|-----------------|--|
| a. $t_{d(on)}$  | The interval measured from the 10% point of the rising input pulse $V_g$ and the 10% rise of the output current $I_C$ .          |
| b. $t_r$        | The interval measured from the 10% to the 90% point of the rising output current $I_C$ .   |
| c. $t_{d(off)}$ | The interval measured from the 90% point of the falling input pulse $V_g$ to the 90% point of the falling output current $I_C$ . |
| d. $t_f$        | The interval measured from the 90% to the 10% point of the falling output current $I_C$ .  |



MIL-STD-750C  
NOTICE 8

6. Equipment. A modern high speed digitizing system is recommended. The measurement of  $W_{ON}$  or  $W_{OFF}$  is accomplished by accessing the output  $V(t)$  and  $I(t)$  waveforms, digitizing them, and transmitting the data to a computer where  $W_{ON}$  or  $W_{OFF}$  is calculated and the results displayed. Two factors of importance must be considered.

- a. Sample spacing must be short relative to transition times for accurate and repeatable results.
- b. The relative  $V(t)$ ,  $I(t)$  channel delay must be known and accounted for in the computer program that does the point by point multiplication and summation that determines either  $W_{ON}$  or  $W_{OFF}$  (see figure 3477-2).

7. Specifications.

- |             |                         |       |             |
|-------------|-------------------------|-------|-------------|
| a. $V_{CL}$ | Clamp voltage           | _____ | V           |
| b. $I_{CE}$ | Maximum test current    | _____ | A           |
| c. $V_{GE}$ | Gate to emitter voltage | _____ | V           |
| d. $R_G$    | Gate resistance         | _____ | $\Omega$    |
| e. $T_j$    | Junction temperature    | _____ | $^{\circ}C$ |

MIL-STD-750C  
NOTICE 8

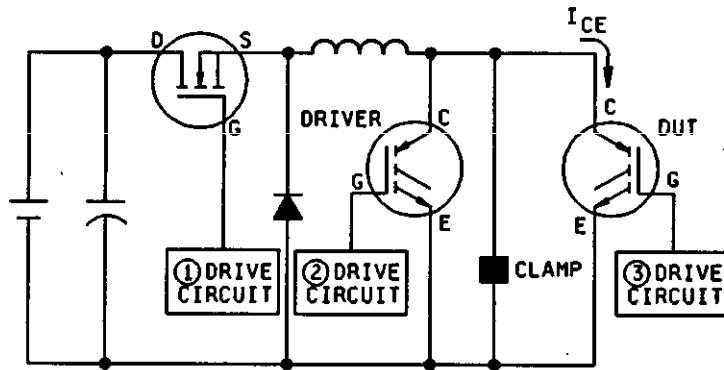


FIGURE 3477-1. Test circuit.

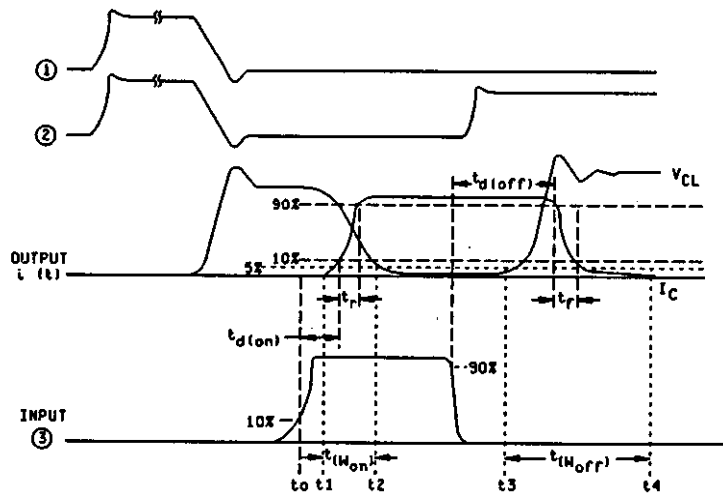


FIGURE 3477-2. Typical clamped inductive waveforms.

MIL-STD-750C  
NOTICE 8

METHOD 4023

SCOPE DISPLAY

1. Purpose. The purpose of this test is to define criteria for inspection of the dynamic reverse characteristics of rectifiers, switching, and zener diodes when viewed on a curve tracer. This inspection criteria may not be applicable to specific rectifier designs where the device is not intended to be driven into avalanche breakdown, or where the detail specification has not provided for this inspection.

2. Scope.

2.1 All devices requiring stable or sharp and stable breakdown characteristics. NOTE: Since low voltage zeners do not inherently have, and some other devices may not have a "sharp" breakdown, specific exceptions in requirements are also provided herein.

2.2 For condition A, stable (only) types, figures 3 through 11 shall apply.

2.3 For condition B, sharp and stable types, figures 2 through 11 shall apply. The ideal sharp and stable trace is one which exhibits a single horizontal line up to the point of breakdown, then transitions vertically to form a 90 degree angle while maintaining the single line (see figure 1). Deviations from this ideal, which are not specifically allowed in this method or detail, specification shall be cause for rejection of the device under test. The following depictions (figures 2 through 11) have been compiled to describe commonly observed faults. Tolerances from acceptable devices have been assigned when applicable.

3.0 Procedures

3.1 The curve tracer presentation shall be configured so that the horizontal axis shall be calibrated in volts per division and the vertical axis shall be calibrated in amps per division (or fractions thereof). The vertical and horizontal axis of the curve tracer presentation will be graduated into 8 or 10 divisions, each representing a precalibrated increment of current or voltage.

3.2 A series load resistor shall be used to limit the device reverse current and prevent device damage. This typical resistance should be approximately one quarter or more of the device resistance at the breakdown specification, when the curve trace set-up permits. Example: A device to be observed at  $I_{BR}$  of 100  $\mu A$  which is specified to be 400 volts minimum, would have a series resistance chosen according to the following:

$$R \geq 0.25 (400 / 0.0001), \text{ therefore} \\ R \geq 1 \text{ Megohm}$$

The curve tracer peak voltage ( $V_{CT}$ ) may also require limitation, particularly if the series load resistance described cannot be achieved. See figure 1 and 3.5 for typical load line relationships to assure safe reverse current monitoring.

3.3 The trace should occur in the first and third quadrant of the display and be slowly adjusted from zero volts to attain the specified current with the maximum amount of resolution for determination of trace characteristics. The dut shall be held under breakdown conditions for at least one second to ensure freedom from intermittent instability for breakdown drift. NOTE: All figures herein are shown in the first quadrant.

3.4 The vertical and horizontal sensitivity shall be adjusted on the curve tracer to provide a rendition of the complete trace to the specified current. Horizontal and vertical sensitivity shall be adjusted to provide a trace occupying no less than 50 percent of the available screen.

MIL-STD-750C  
NOTICE 8

3.5 The curve trace voltage shall not be simply set at a predetermined value and snapped on instantaneously. This may be done only if the product to be tested is known to have a sufficiently narrow breakdown voltage ( $V_{BR}$ ) range with a predetermined series (load line) resistor setting (refer to paragraph 3.2) and described below, to assure that the device will not be overpowered. This is typically the case for zener diodes prescreened on  $V_Z$  (or  $V_{BR}$ ). The peak open circuit supply voltage of the curve tracer ( $V_{CT}$ ) may then be adjusted such that the  $V_{CT}$  setting can provide no more current ( $I_{BR}$  or  $I_Z$ ) than that required for avalanche breakdown, taking into account the series load resistance "R" in figure 1. Unless otherwise specified, these relationships may be calculated by:

$$I_{BR} = \frac{V_{CT} - V_{BR}}{R}, \text{ AND } V_{CT} = I_{BR}R + V_{BR}$$

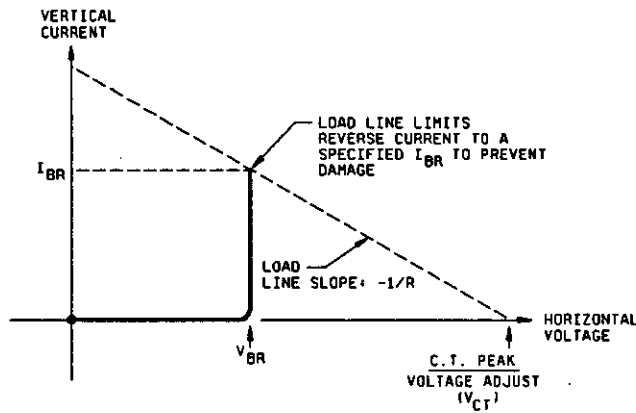
The resistance "R" may be determined by:

$$R = \frac{V_{CT} - V_{BR}}{I_{BR}}$$

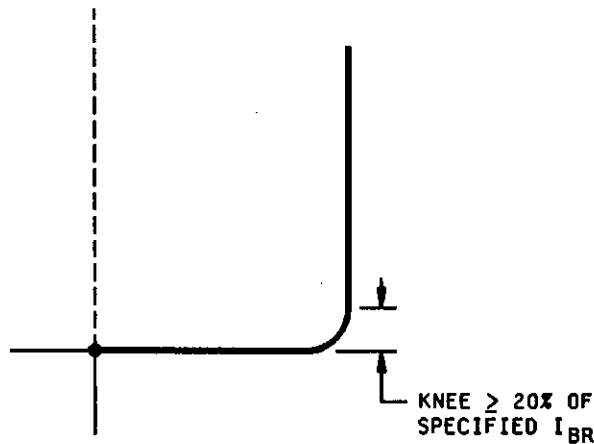
The  $V_{BR}$  (or  $V_Z$ ) utilized in this equation should be the minimum expected so as to always maximize the R value selected.

3.6 Allowance for deviation from the desired characteristics described in this method or detail specification must be granted by the qualifying activity. If a particular rejectable trace described is expected in a manufacturer's normal process, it must be identified and explained during device conformance/qualification. Devices exhibiting the exceptional trace characteristic must be present in the conformance/qualification lot to establish reliability.

4. Summary. The following condition shall be specified in the detail specification: Test condition to be used.

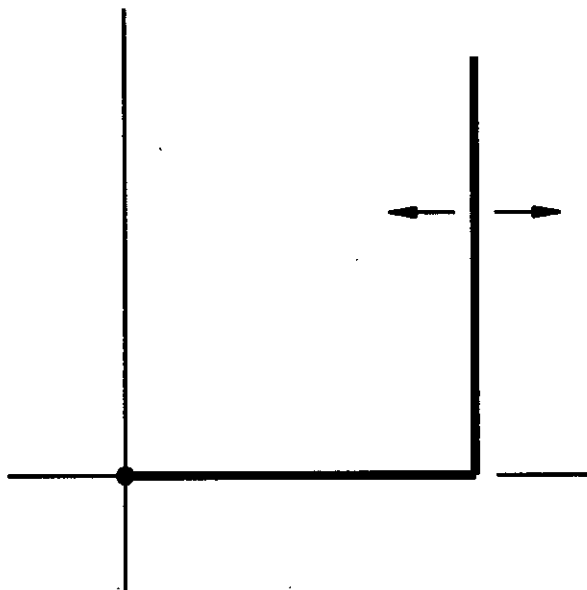
MIL-STD-750C  
NOTICE 8

This ideal trace exhibits none of the characteristics described on the figures below. Also, illustrated are the basic curve tracer adjustments and relation for a safe maximum operating current ( $I_{BR}$ ) with the series load resistor ( $R$ ) versus peak open circuit voltage ( $V_{CT}$ ) and device breakdown voltage ( $V_{BR}$ ).

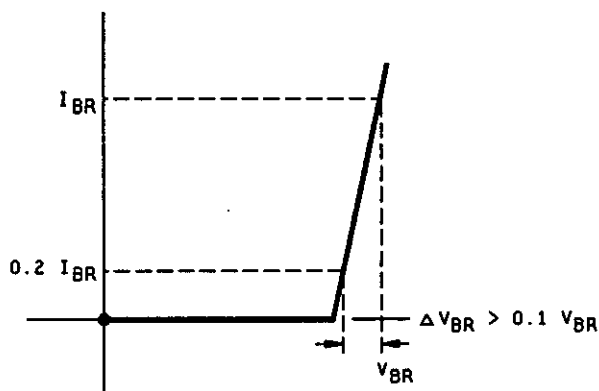
FIGURE 1. Ideal reverse.

The knee area is the area in which the trace transitions from the horizontal to the vertical. Unless otherwise specified, this area should not require more than 10% of the total horizontal voltage component being viewed, or more than 20% of the specified  $I_{BR}$ . Not applicable to fast, ultrafast, and schottky rectifiers or low voltage zeners < 10 volts.

FIGURE 2. Soft knee

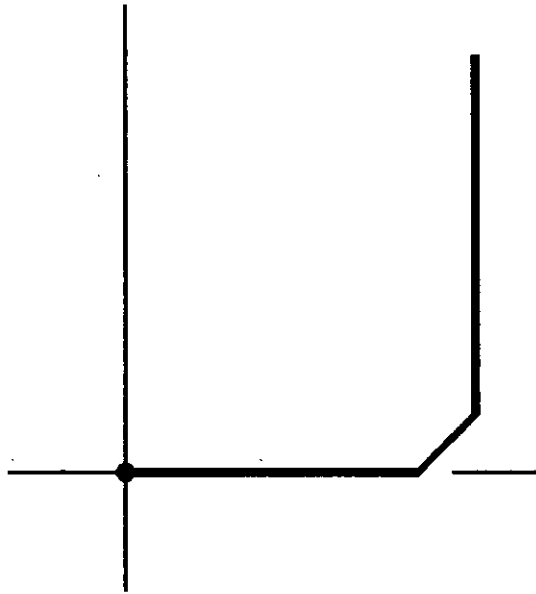
MIL-STD-750C  
NOTICE 8

The vertical component of the trace should remain stable in the horizontal axis. An undesirable drift is defined as greater than 10% increase or 2% decrease in actual breakdown voltage up to 1500 volts. If over 1500 volts, the allowable drift should separately specified.

FIGURE 3. Drift.

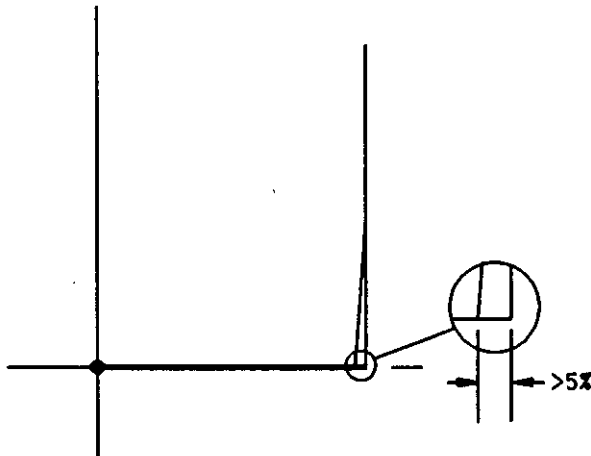
The slope shall be less than 10 percent of  $V_{BR}$  when viewed between 20 percent to 100 percent of the specified  $I_{BR}$  or  $I_Z$ . Low voltage zeners below 5.5 volts are in exception to this requirement; also other devices, as may be specified.

FIGURE 4. Slope.

MIL-STD-750C  
NOTICE 8

The double break occurs the area in which the trace transitions from the horizontal to the vertical. Unless otherwise specified, this area should not occupy more than 10 percent of the total horizontal voltage component being viewed, or more than 20 percent of the specified  $I_{BR}$  or  $I_{TT}$ . This requirement is not applicable to ultrafast or schottky rectifiers, and low voltage zeners  $\leq 10$  volts.

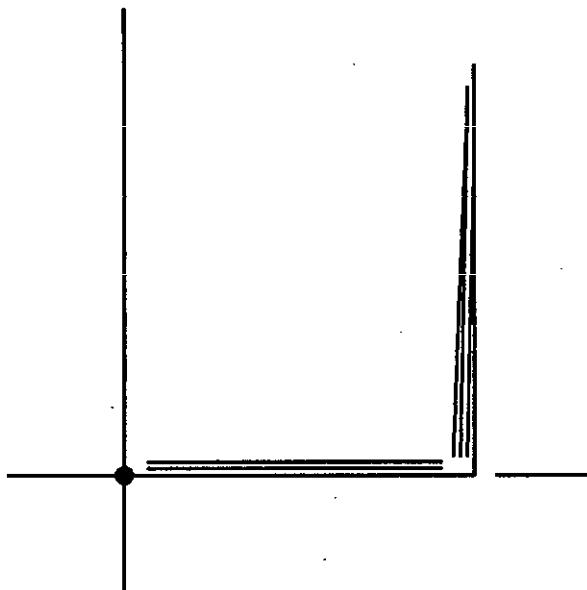
FIGURE 5. Double break (reject criteria for sharp knee devices).



For rectifiers and zeners the region at the knee may display a secondary trace no more than 5 percent of the total voltage of the device under test (see detail).

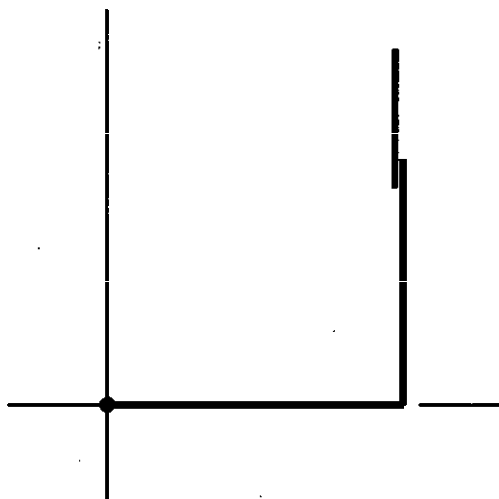
FIGURE 6. Double trace.

MIL-STD-750C  
NOTICE 8



Any jittery movement of the trace in any direction, not caused by power line voltage fluctuations, must not occur.

FIGURE 7. Unstable (jitter).

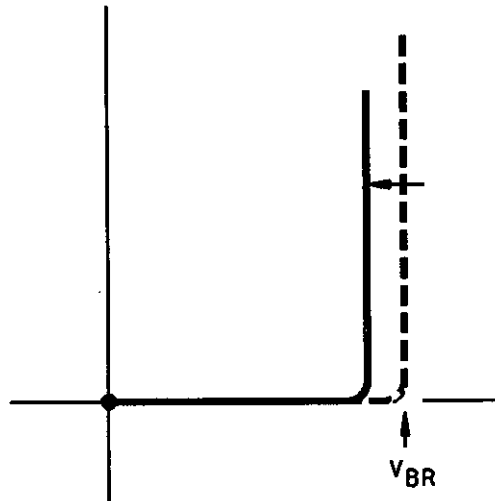


The vertical component must not depart from a single vertical line, except as allowed on figures 5 and 6.

FIGURE 8. Discontinuity.

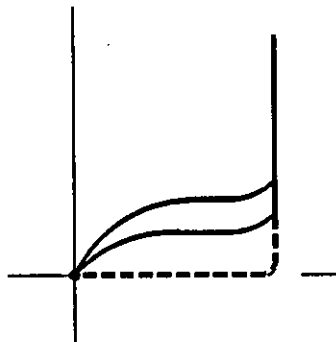


MIL-STD-750C  
NOTICE 8



The vertical component must not decrease its value abruptly by 2% or more of  $V_{BR}$ .

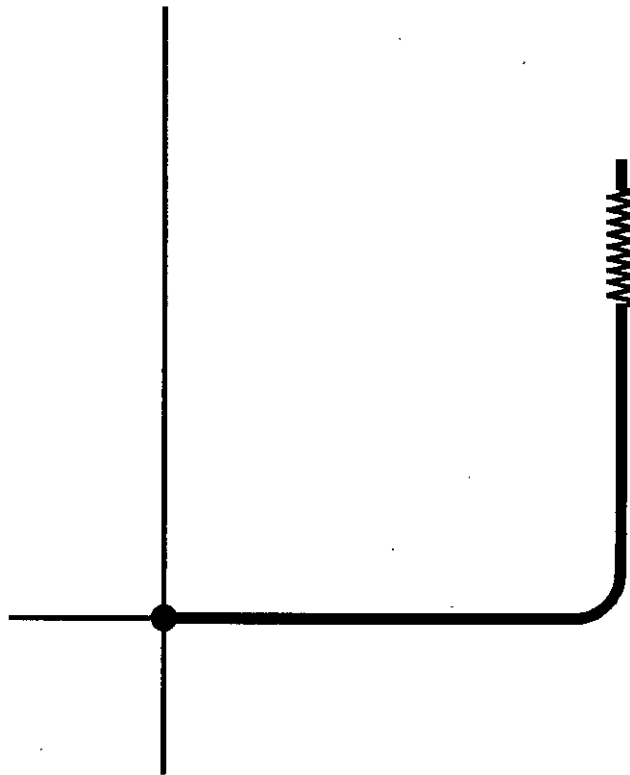
FIGURE 9. Snap back - collapsing  $V_{BR}$ .



Leakage current (vertical) must not degrade from an initial value.

FIGURE 10. Floater.

MIL-STD-750C  
NOTICE 8



Instability (arcing) appearing at or near the specified  $I_{BR}$  region on the vertical trace (such as may be coincident with visible sparking activity within the device die region) must not be present. Noise at or near the knee is permissible, such as typically observed on avalanche-zener devices.

FIGURE 11. Arcing.

MIL-STD-750C  
NOTICE 8

## METHOD 4031.3

## REVERSE RECOVERY CHARACTERISTICS

1. Purpose. The purpose of this test is to measure the reverse recovery time and other specified recovery characteristics related to signal, switching, and rectifier diodes by observing the reverse transient current versus time when switching from a specified forward current to a reverse biased state in a specified manner.

2. General guide for selecting appropriate condition. Four conditions are given to include recommended practice for the range of diodes considered. A general guide for selecting the appropriate condition letter is:

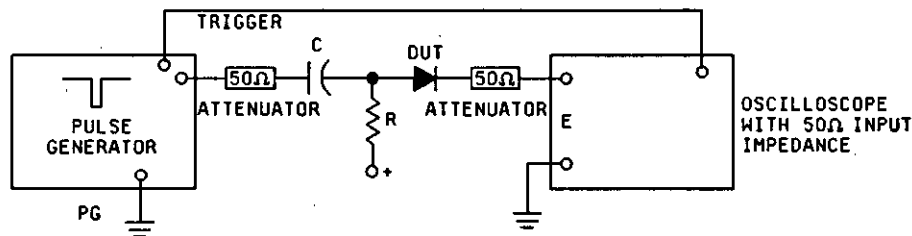
- a. Signal diodes with reverse recovery time less than 6 ns.
- b. Low to medium current rectifiers with maximum specified recovery times of 50 to 3,000 ns.
- c. High current rectifiers with maximum specified recovery times of 350 ns or greater.
- d. Ultra-fast rectifiers, particularly on new specifications.

Further, detailed guidance is given under each condition below.

2. Test condition A. This condition is particularly relevant to low-current, signal diodes faster than 6 ns and tested at 10 mA. However, it is practicable for measurements up to 20 ns and 100 mA.

2.1 Circuit notes for condition A.

- a. Rise time of the reverse voltage pulse across a noninductive calibration resistor in place of the DUT shall be less than one-fifth of the recovery time of the DUT, for greatest accuracy.
- b. Oscilloscope rise time shall be less than one-fifth of device recovery time, for greatest accuracy.
- c. Proper coaxial networks and terminations shall be employed to ensure against error-producing pulse reflections.
- d.  $R > 10 R_L$
- e.  $R_L = Z_{PG} + Z_{SCOPE} = 100 \text{ ohms}$ , unless otherwise specified.
- f.  $C > 10 PW \div RL$
- g.  $PW > 2 \times \text{maximum specified } t_{rr}$  (see figure 1.)

MIL-STD-750C  
NOTICE 8FIGURE 1. Test circuit for condition A.

NOTE: The test circuit shall comply with the test conditions as stated under 2.1.

PW = Pulse width of reverse voltage pulse (see figure 2).

$R_L$  = Load resistance

$C$  = Coupling capacitance

2.2 Procedure for condition A. The specified forward current shall be adjusted by resistor R and the + supply. Voltage E, developed across the 50 ohm oscilloscope input impedance shall be measured. Specified forward current shall be calculated by the expression  $I_F = E/50$ . The time duration of  $I_F$  shall be at least 10 times the device recovery time. The oscilloscope trace deflection above zero reference shall be adjusted by the oscilloscope vertical sensitivity to produce an amplitude of 2 cm minimum vertical deflection. Adjustment of the reverse transient current ( $I_{RM}$ ) shall be made by varying the pulse generator output, observing the voltage E across the 50 ohm oscilloscope input impedance, and calculating  $I_{RM}$  by the expression  $I = E/50$ . When reverse bias voltage  $V_R$  is specified, and  $I_{RM}$  is not, the DUT shall be replaced with a shorting bar and  $I_{RM}$  shall be calculated by the expression  $V_R/50$  (see figure 2.)

2.3 Summary for condition A. The following conditions shall be specified in the detail specification:

- a. Forward current,  $I_F$ .
- b. Reverse current  $I_{RM}$  (preferred), or reverse voltage (optional alternative).
- c. Load resistance, if other than 100 ohms. (this is the sum of  $Z_{PG}$  and  $Z_{SCOPE}$ ).
- d. Ambient temperature in °C.
- e. Generator impedance, if other than 50 ohms.
- f. Recovery current measuring point,  $i_{R(REC)}$ , if different from 10 percent of  $I_{RM}$ .

The following measurement shall be made:  $t_{rr}$  (see figure 2).

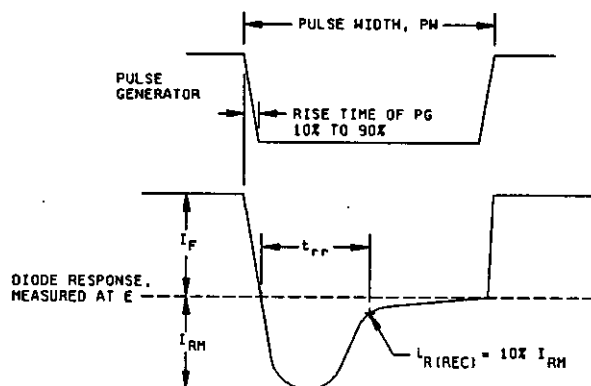
MIL-STD-750C  
NOTICE 8

FIGURE 2. Response pulse waveforms for condition A.

3. Test condition B. (See suggested conditions, B1, B2, etc. below). This condition is particularly relevant to medium current (axial and similar) types of standard and fast rectifiers with maximum specified recovery times between 50 and 3,000 ns that measured at peak forward currents greater than 100 mA and less than or equal to 1.0 ampere. It is readily adapted to lower test currents. This test is also appropriate for devices with recovery times less than 50 ns that are measured at peak forward currents of 1A or less; below 25 ns, or at higher current, particular care must be used to achieve low loop inductance and low circuit rise times to achieve acceptable repeatability.

This condition differs from condition D in that the reverse current ( $I_{RM}$ ) is limited by the test circuit, not by the DUT.

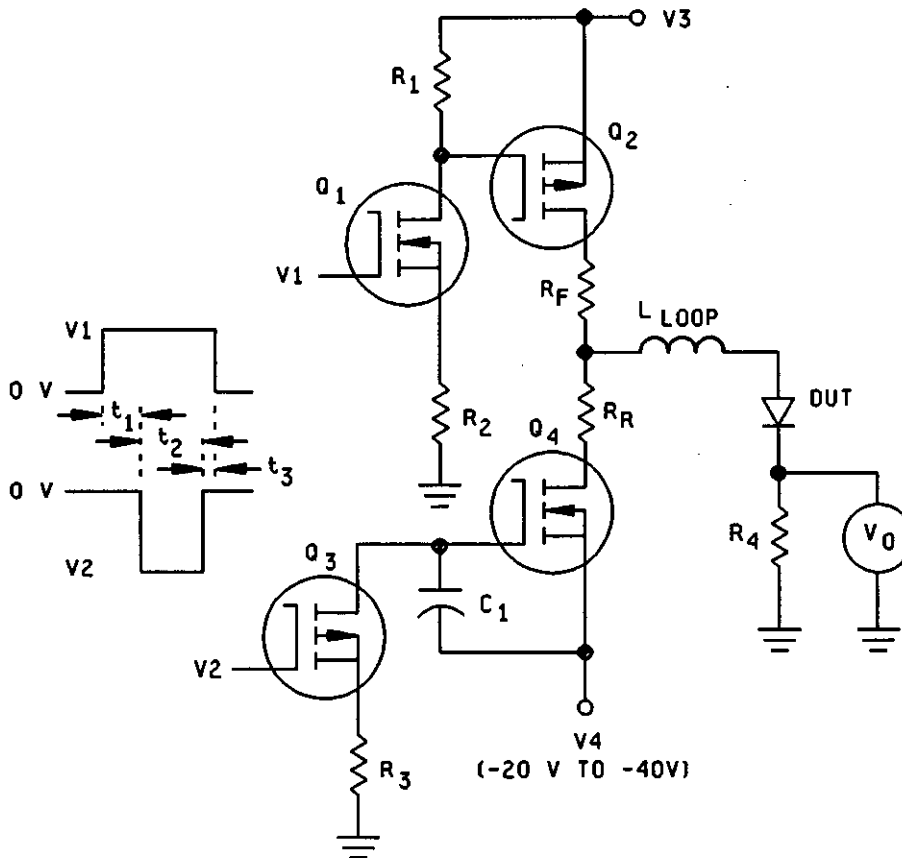
Designation (condition)		B1	B2	B3	B4	B5
Test current, (amperes) see figure 4	$I_F$	0.5	0.5	1.0	1.0	0.01
	$I_{RM}$	1.0	0.5	1.0	1.0	0.01
	$i_{R(REC)}$	0.25	0.1	0.5	0.1	0.005
Circuit resistor.* (ohms)	$R_F$	33	33	50	50	1200
	$R_R$	9	9	15	15	200
	$R_4$	1.00	1.00	1.00	1.00	10.0

\* Preferred nominal resistance values are shown; modification of  $R_F$  and  $R_R$  may be needed to achieve the rise time of 3.1a and the  $I_{RM}$  specified.

MIL-STD-750C  
NOTICE 8

3.1 Circuit notes for condition B. The timing and test circuit of figure 3A is a guide to that needed. An equivalent circuit may be used. Figure 3B shows a suggested configuration for  $R_4$ . Duty factor shall be 5 percent maximum.

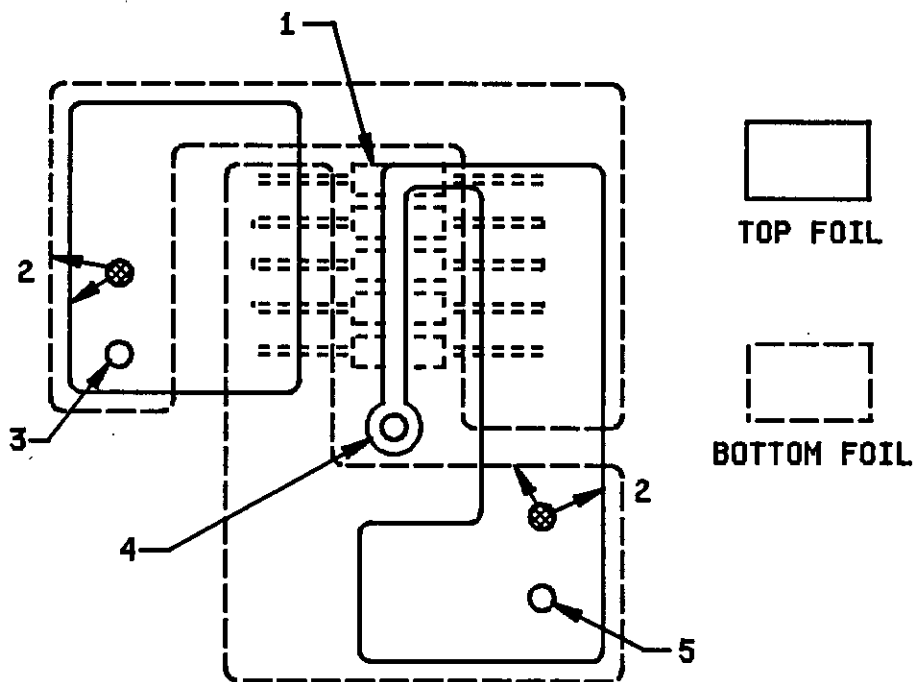
- The rise time of the reverse voltage pulse across a noninductive calibration resistor in place of DUT shall be less than one-fifth the recovery time of the DUT.
- The oscilloscope rise time shall be less than one-half of the pulse generator rise time.



$V_3$  and  $R_F$  control forward current  $I_F$ .  
 $V_4$  and  $R_R$  control reverse current  $I_{RM}$ .  
 $t_{rr(max)}$  is the longest to be measured.  
 $t_{rr(min)}$  is the shortest expected.  
 $Q_1$  and  $Q_4 = \text{IRF530}$   
 $Q_2$  and  $Q_3 = \text{RFP12P08}$

$t_1 > 5 t_{rr(max)}$   
 $t_2 > t_{rr}$   
 $t_3 > 0$   
 $L_1/R_4 < t_{rr(min)}/10$   
 $L_1$  is the self induction of  $R_4$

FIGURE 3A. Test circuit for condition B.

MIL-STD-750C  
NOTICE 8

## NOTES:

1. Resistor assembly  $R_4$  is made from ten 1 ohm, 1/4 W metal film resistors, 5 on top and 5 on the bottom foils. The center of resistor bodies are not shown, and leads are shown dotted so that conducting foils may be more clearly shown. Bottom resistor current flow L to R ( $\rightarrow$ ) is opposite to top current flow R to L ( $\leftarrow$ ), providing magnetic field cancellation. Sense lead to the center conductor of the probe jack exits at right angle to resistor axes and is located between the top and bottom resistor layers.
2. Cross hatched circular areas show the connections between those top and bottom foil regions indicated by arrows.
3. To ground of circuit and probe.
4. To center conductor of miniature probe jack.
5. to cathode of DUT.

FIGURE 3B. Suggested board layout for low  $L_1/R_4$  for condition B.

3.2 Procedure for condition B. Specified forward current ( $I_F$ ) shall be adjusted by varying positive voltage,  $V_3$ . Reverse current ( $I_{RM}$ ) shall be controlled by varying the negative voltage,  $V_4$  (see figure 4). With the DUT in place the circuit must be capable of higher than specified  $I_{RM}$ ; the circuit, and not the diode, must limit  $I_{RM}$ .

MIL-STD-750C  
NOTICE 8

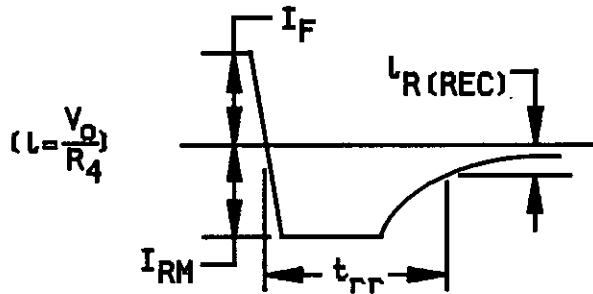


FIGURE 4. Current through DUT (condition B).

3.3 Summary for condition B. The following conditions shall be specified in the detail specification:

- a. Test condition (B1, B2, etc., - see 3.) If not in table, specify c, d, and e.
- b. Ambient temperature, if other than 25°C.
- c. Forward current,  $I_F$ .
- d. Reverse current,  $I_{RM}$ .
- e. Load resistances  $R_F$  and  $R_R$ .
- f. Recovery measuring point,  $i_{R(REC)}$ .

NOTE: Specify c through f only if not a condition designation in 3e.

The following measurement shall be made:  $t_{rr}$  (see figure 4).

4. Test condition C. This test is intended for high current rectifiers with reverse recovery times equal to or greater than 350 ns and test at peak forward currents greater than 10 amperes.

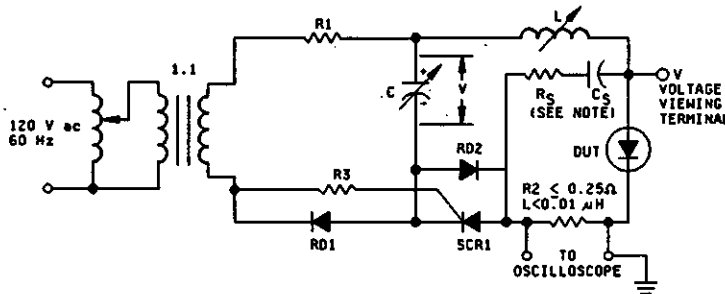


FIGURE 5. Circuit for measuring reverse recovery characteristics (condition C).



MIL-STD-750C  
NOTICE 84.1 Circuit notes for condition C.

- a. The circuit is designed to simulate the commutation duty encountered in power rectifier diode circuits while also keeping average power dissipation low to minimize the need for thermal management.
- b. The resistance of the C.L. and DUT loop ( $R_2$  and parasitics) is small, e.g.,  $2\pi\sqrt{L/C} \gg R$  so the test current will essentially be sinusoidal, possessing a width of  $\pi\sqrt{LC}$ ; a  $di/dt$  of  $V/L$  and a peak value of  $V\sqrt{L/C}$ . The peak voltage across the capacitor shall be as small as practicable to achieve the desired test conditions. The effects of reverse voltage magnitude on the test device recovery characteristics are neglected.
- c. The minimum forward current pulse time ( $t_p$ ) shall be at least 5 times the recovery time ( $t_{rr}$ ) of the DUT so that the  $di/dt$  will be linear and of the same value before and after current reversal.
- d. The oscilloscope rise time shall be less than one-fifth of  $t_a$  or  $t_b$  (see figure 6), whichever is less.
- e. The inductance of the current viewing resistor shall be extremely low, e.g., 0.01 microhenry. Abrupt recovery rectifiers (figure 6) can cause current oscillations which may be reduced by using a lower inductance current viewing resistor and by properly terminating the oscilloscope cable. A current transformer 1/ with suitable rise time may be substituted for the current viewing resistor. Rectifier diode RD2 provides a very low inductance path around SCR1 if the reverse recovery time of SCR1 is shorter than that of the DUT. An external SCR triggering source may be required to achieve stable triggering.
- f. A slight oscillation may appear on the waveform following device recovery. This may be reduced by reducing the current viewing resistor's inductance, or properly terminating the viewing cable. The oscillation, however, does not affect the test results.
- g.  $D_2$  and its circuit branch should provide a very low inductance path 2 around the SCR if the reverse recovery time of the SCR is shorter than that of the DUT.
- h.  $R_3$  must be sufficiently large such that the SCR triggers only after the capacitor, C, has had ample time to charge to its desired value. If stable triggering or ample charging is a problem, a momentary pushbutton switch may be inserted in line with  $R_3$  to provide triggering. A pulse transformer technique is also acceptable in the triggering circuit.

4.2 Procedure for condition C. C, L, and V are adjusted to obtain the specified test current  $di/dt$  and magnitude,  $I_{FM}$ . The recovery time for rectifier diodes is defined as  $t_{rr} = t_a + t_b$  (see figure 6)  $t_a$  is measured from the instant of current reversal to the instant that current reaches its peak reverse value  $I_{RM(REC)}$  and  $t_b$  is measured from  $I_{RM(REC)}$  to the instant the straight line connecting  $I_{RM(REC)}$  and  $0.25 I_{RM(REC)}$  intercepts the zero current axis. The recovery time for devices with abrupt recovery characteristics is defined in the same manner except  $t_b$  is measured from  $I_{RM(REC)}$  to the instant the test current waveform intercepts the zero current axis, if applicable.

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1/ Pearson Electronics, Inc. or equivalent types.

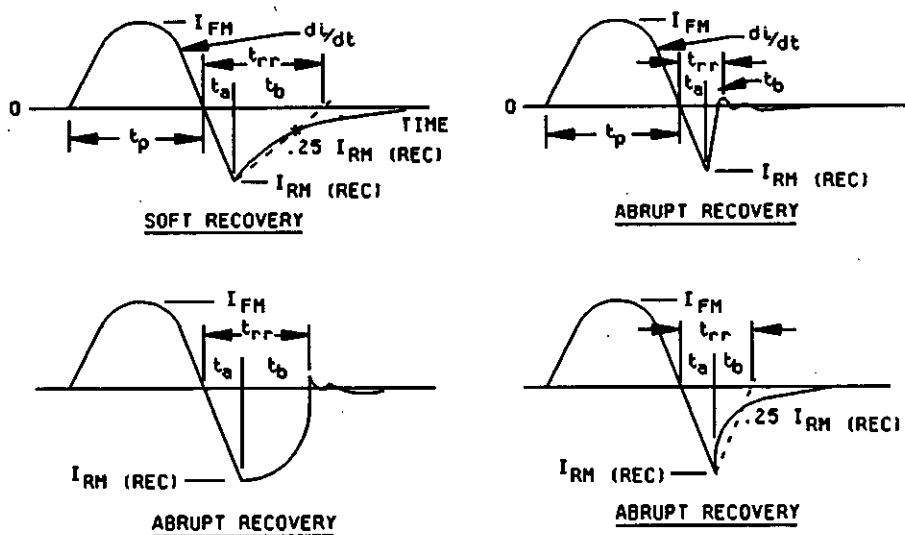
MIL-STD-750C  
NOTICE 8

FIGURE 6. Test current waveforms for various types of rectifier diodes under test in the circuit for measuring reverse recovery characteristics.

4.3 Summary for condition C. The following conditions shall be specified in the detail specification:

- a. Case temperature in °C.
- b. Test repetition rate, in Hz.
- c. Peak forward current,  $I_{FM}$ , in amperes.
- d. Rate of decrease of forward current,  $di/dt$ , in A/ $\mu$ s.
- e. Minimum test current pulse width,  $t_p$ , in microseconds. (Duty cycle shall be  $\leq 1\%$ ).

The following characteristics shall be specified for measurement in the detail specification as required:

- a. Reverse recovery time (defined as  $t_{rr} = t_a + t_b$ ),  $t_a$ ,  $t_b$ .
- b. Reverse recovery current,  $I_{RM}(REC)$ , in amperes.

MIL-STD-750C  
NOTICE 8

5. Test condition D. (See suggested conditions, D1, D2, D3, etc. below.) This condition is intended for ultra-fast medium current rectifiers (axial and case mount, or equivalent styles) measured at  $I_F \geq 1A$  and with reverse recovery time  $\leq 100$  ns. With good engineering practice, condition D can adequately measure  $t_{rr}$  down to about 10 ns; it can also utilize  $I_F$  up to at least 10 A.

Device ratings		Designation (condition)	Values for testing	
$I_0$ or $I_F$ (AV) (A)	$t_{rr}$ (ns)		$I_F$ (A)	di/dt (A/ $\mu$ )
1 to 4	> 65 to 100	D1	2	100
to 20	> 65 to 100	D2	6	100
over 20	> 65 to 100	D3	10	100
1 to 4	$\leq 65$	D4	2	200
to 20	$\leq 65$	D5	6	200
over 20*	$\leq 65$	D6	10	200

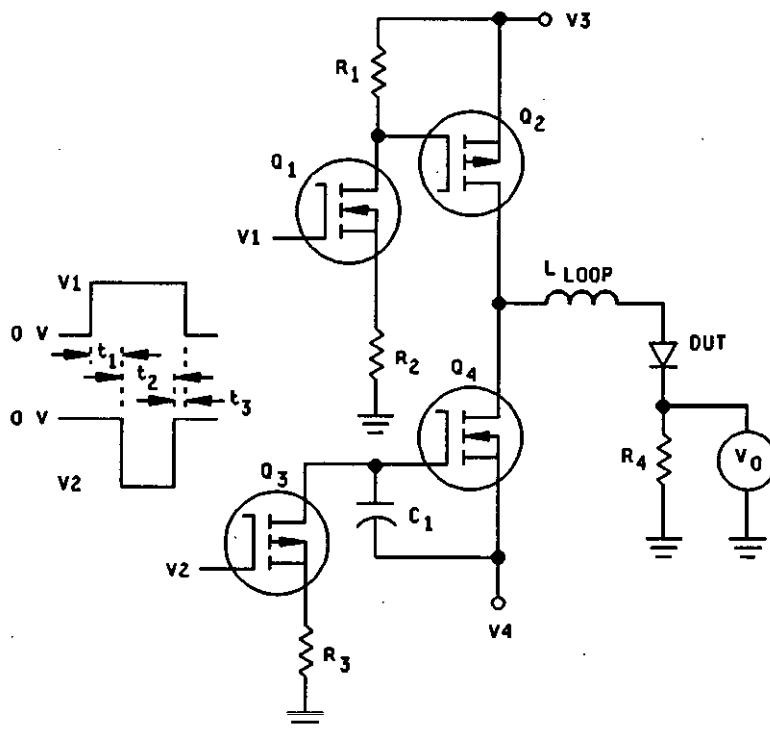
\* For devices with substantially higher rated current it is desirable to use test condition for  $I_F$  close to rated current, and higher values of di/dt.

5.1 Test circuit. Refer to figures 7 and 8 for timing and circuit details. Equivalent circuits may be used. The forward current generator consisting of  $Q_1$ ,  $Q_2$ ,  $R_1$ , and  $R_2$  may be replaced with any functionally equivalent circuit. Likewise, the current-ramp generator consisting of  $Q_3$ ,  $Q_4$ ,  $R_3$ , and  $C_1$ . The duty factor shall be  $\leq 5$  percent.

- This method presumes that good engineering practice will be employed in the construction of the test circuit, e.g., short leads, good ground plane, minimum inductance of the measuring loop and minimum self-inductance ( $L_1$ ) of the current sampling resistor ( $R_4$ ). Also, appropriate high speed generators and instruments must be used.
- The measuring-loop inductance ( $L_{LOOP}$ , see figure 7) represents the net effect of all inductive elements, whether lumped or distributed, e.g., bonding wires, test fixture, circuit board foil, inductance of energy storage capacitors, etc. The value of  $L_{LOOP}$  should be 100 nH or less. The reason for controlling this circuit parameter is that it, combined with diode characteristics including  $C_T$ , determines the value of  $t_b$ .
- The turn-off reverse-voltage overshoot shall not be allowed to exceed the device rated breakdown voltage. Ringing and overshoot may become a problem with  $R_{LOOP} < 2\sqrt{L/C}$ ; where  $L = L_{LOOP}$ . That is another reason for minimizing  $L_{LOOP}$ .
- Regarding breakdown voltage,  $-V_b$  should be kept as low as practicable, especially when test low voltage devices. A value of approximately 30 volts is recommended.

MIL-STD-750C  
NOTICE 8

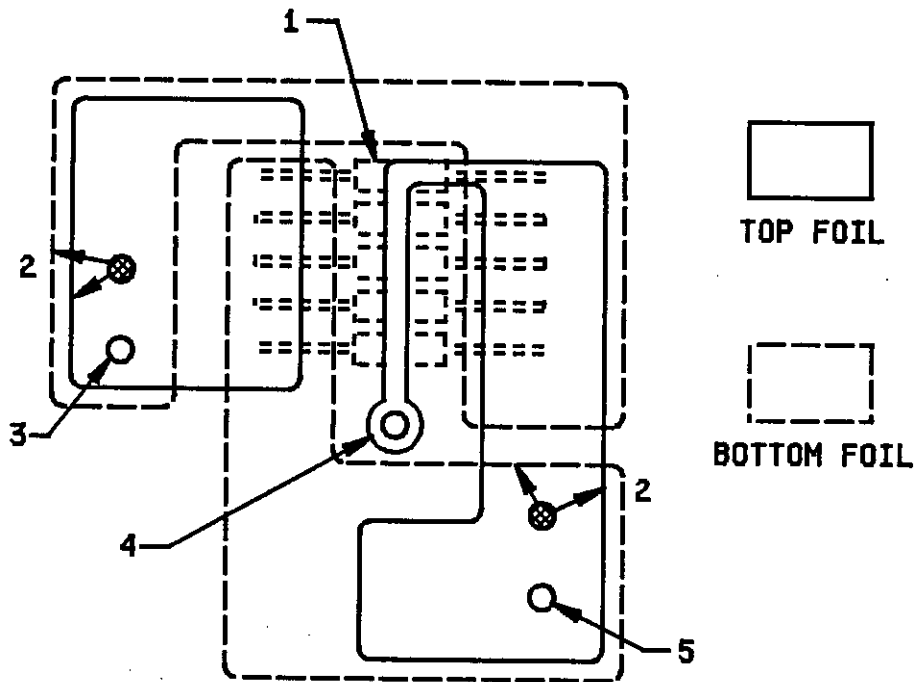
- e. The self-inductance of the current-sample resistor  $R_4$  (see figure 4031-8) must be kept low relative to  $t_a$  because the observed values of  $t_a$  and  $I_{RM}$  increase with increasing self-inductance. Since the value of  $R_4$  is not specified, the recommended maximum inductance is expressed as a time constant ( $L_1/R_4$ ) with a maximum value of  $t_a$  (minimum)/10, where  $t_a$  (minimum) is the lowest  $t_a$  value expected. This ratio was chosen as a practical compromise and would yield an observed  $t_a$  which is 10 percent high ( $\Delta t_a = L_1/R_4$ ). The  $I_{RM}$  error is a function of the  $L_1/R_4$  time constant and  $di/dt$ . For a  $di/dt$  of  $100 \text{ A}/\mu\text{s}$  the observed  $I_{RM}$  would also be 10 percent high.  $\Delta I_{RM} = L_1/R_4 \text{ di}/dt$ .
- f. The  $di/dt$  of  $100 \text{ A}/\mu\text{s}$  was chosen so as to provide reasonably high signal levels and still not introduce the large  $I_{RM}$  errors caused by higher  $di/dt$ . Higher values of  $di/dt$ , without large errors, can be achieved with lower  $L_1/R_4$ .



$V_1$  amplitude controls forward current ( $I_F$ ).  
 $V_2$  amplitude controls  $di/dt$   
 $t_a(\text{max})$  is the longest  $t_a$  to be measured.  
 $t_a(\text{min})$  is the shortest  $t_a$  to be measured.  
 $Q_1$  and  $Q_4 = \text{IRF530}$   
 $Q_2$  and  $Q_3 = \text{RFP12P08}$

$t_1 > 5 t_a(\text{max})$   
 $t_2 > t_{rr}$   
 $t_3 > 0$   
 $L_1/R_4 < t_a(\text{min})/10$   
 $L_1$  is the self induction of  $R_4$

FIGURE 7.  $t_{rr}$  test circuit for condition D.

MIL-STD-750C  
NOTICE 8

## NOTES:

1. Resistor assembly  $R_p$  is made from ten 1 ohm, 1/4 W metal film resistors, 5 on top and t on the bottom foils. The center of resistor bodies are not shown, and leads are shown dotted so that conducting foils may be more clearly shown. Bottom resistor current flow L or R ( $\leftrightarrow$ ) is opposite to top resistor current flow R to L ( $\leftarrow$ ), providing magnetic field cancellation. Sense lead to the center conductor of the probe jack exits at right angle to resistor axes and is located between the top and bottom resistor layers.
2. Crosses hatched circular areas show the connections between those top and bottom foil regions indicated by arrows.
3. To ground of circuit and probe.
4. To center conductor of miniature probe jack.
5. To cathode of DUT.

FIGURE 8. Suggest board layout for low  $L_1/R_L$  for condition D.

MIL-STD-750C  
NOTICE 8

5.2 Procedure for condition D. Adjust  $V_1$  for the specified forward current,  $I_F$ . Adjust  $-V_2$  for the specified  $di/dt$ . (See figures 7 and 9)

5.3 Summary for Condition D. The following conditions shall be specified:

- Designation (condition, - see 5.). If another is desired, d and e must be specified.
- $-V_R$ , reverse ramp power supply voltage.
- $T_C$ , case temperature, if other than 25°C.
- $I_F$ , .25 (min) of the continuous rated current is the suggested alternative (see 5.3a.).
- $di/dt$ , 100 A/ $\mu$ s is the suggested alternative (see 5.3a.).

The following characteristics shall be specified for measurement:

- Reverse recovery time,  $t_{rr}$  (see figure 9). Alternative terminating points may be specified, e.g., the first zero crossing, when applicable, or an unextrapolated 0.25  $I_{RM(REC)}$ .
- $I_{RM(REC)}$  (see figure 9).

NOTE: An additional measurement,  $t_a$  may be made if desired to compute  $t_b = t_{rr} - t_a$ , and the recovery softness factor,  $RSF = t_b/t_a$ .

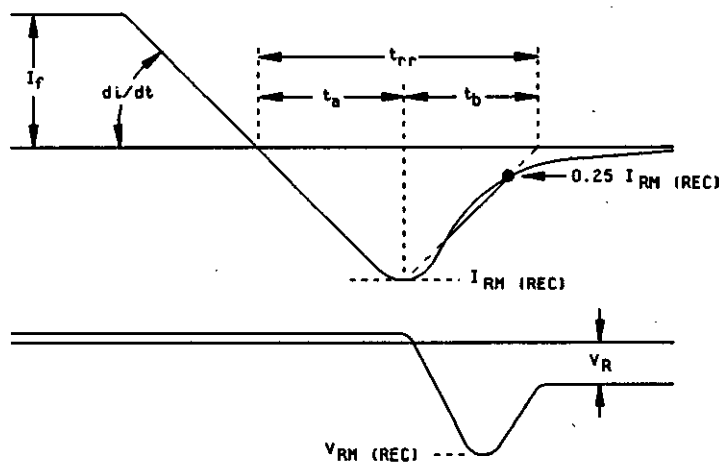


FIGURE 9. Generalized reverse recovery waveforms for condition D.