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The documentation and process conversion measured necessary to comply with this revision shall be completed by 10 December 2018.

INCH–POUND

MIL–STD–750–5
w/CHANGE 1
10 August 2018
SUPERSEDING
MIL–STD–750–5
3 January 2012
(see 6.4)

DEPARTMENT OF DEFENSE

TEST METHOD STANDARD

HIGH RELIABILITY SPACE APPLICATION TEST METHODS FOR SEMICONDUCTOR DEVICES

PART 5: TEST METHODS 5000 THROUGH 5999

AMSC N/A

FSC 5961

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FOREWORD

1. This standard is approved for use by all Departments and Agencies of the Department of Defense.

2. This subpart standard establishes uniform test methods for high reliability space applications.

3. Comments, suggestions, or questions on this document should be addressed to: Commander, Defense Logistics Agency, DLA Land and Maritime, ATTN: VAC, P.O. Box 3990, Columbus, OH 43218–3990, or emailed to 750.TestMethods@dla.mil. Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at https://assist.dla.mil.

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SUMMARY OF CHANGE 1 MODIFICATIONS

1. Paragraph 1.3 has been modified to comply with current format requirements.
2. Paragraph 2.2.1 has been modified to comply with current format requirements.
3. Paragraph 2.3 has been modified to comply with current format requirements. Documents that have been canceled that were referenced in this test method standard have been removed. Documents not referenced in this test method standard have been removed.
4. Paragraph 3.2 has been modified to remove acronyms not used in this test method standard.
5. Paragraph 6.4 has been modified.
6. Paragraph 6.5 has been added.
7. Test method 5010, paragraph 3.2, deleted canceled reference document.
8. The following modifications to MIL–STD–750–5 have been made:

Paragraph	Modification
1.3	Changed.
2.2.1	Changed.
2.3	Changed.
3.2	Changed.
6.4	Changed.
6.5	Added.

Test method	Paragraph	Modification
5010	3.2	Changed

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CONTENTS

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1. SCOPE

1.1 Purpose. Part 5 of this test method standard establishes uniform test methods for the basic high reliability space application testing of semiconductor devices to determine resistance to deleterious effects of natural elements and conditions surrounding military operations. For the purpose of this standard, the term "devices" includes such items as transistors, diodes, voltage regulators, rectifiers, tunnel diodes, and other related parts. This part of a multipart test method standard is intended to apply only to semiconductor devices.

1.2 Numbering system. The test methods are designated by numbers assigned in accordance with the following system:

1.2.1 Classification of tests. The high reliability space application test methods included in this part are numbered 5000 to 5999 inclusive.

1.2.2 Test method revisions. Revisions are numbered consecutively using a period to separate the test method number and the revision number. For example, 5001.2 designates the second revision of test method 5001.

1.3 Method of reference. When applicable, test methods contained herein should be referenced in the individual specification or specification sheet by specifying the test method number of this test method standard, and the details required in the summary of the applicable method should be listed. To avoid the necessity for changing documents that refer to the test methods of this standard, the revision number should not be used when referencing test methods. (For example: Use 5001 versus 5001.2.)

2. APPLICABLE DOCUMENTS

2.1 General. The documents listed in this section are specified in sections 3, 4, 5, and the individual test methods of this standard. This section does not include documents cited in other sections of this standard or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements documents cited in sections 3, 4, 5 and the individual test methods of this standard, whether or not they are listed.

2.2 Government documents.

2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

MIL–PRF–19500 – Semiconductor Devices, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL–STD–750 – Test Methods For Semiconductor Devices.

(Copies of these documents are available online at http://quicksearch.dla.mil.)

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2.3 Non-Government publications. The following documents form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

ASME INTERNATIONAL (ASME)

ASME Y14.38	–	Abbreviations and Acronyms for Use on Drawings and Related Documents.

(Copies of these documents are available online at http://www.asme.org.)

ASTM INTERNATIONAL (ASTM)

ASTM F25	–	Standard Test Method for Sizing and Counting Airborne Particulate Contamination in Cleanrooms and Other Dust-Controlled Areas.
ASTM F50	–	Standard Practice for Continuous Sizing and Counting of Airborne Particles in Dust-Controlled Areas and Clean Rooms Using Instruments Capable of Detecting Single Sub-Micrometre and Larger Particles.

(Copies of these documents are available online at http://www.astm.org.)

2.4 Order of precedence. Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein (except for related applicable specification sheet, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. DEFINITIONS

3.1 Abbreviations, symbols, and definitions. For the purposes of this part of the test method standard, the acronyms, symbols, and definitions specified in MIL–PRF–19500, ASME Y14.38, and herein shall apply.

3.2 Acronyms used in this standard. Acronyms used in this part of the test method standard are defined as follows:

a.	Å	–	Angstrom.
b.	C/V	–	Capacitance–voltage.
c.	DVM	–	Digital voltmeter.
d.	MOS	–	Metal oxide semiconductor.
e.	pF	–	Picofarad.
f.	V_{FB}	–	Forward bias voltage.

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4. GENERAL REQUIREMENTS

4.1 General. Unless otherwise specified in the individual test method, the general requirements of MIL–STD–750 shall apply.

4.2 Test circuits. The test circuits shown in the test methods of this test method standard are given as examples which may be used for the measurements. They are not necessarily the only test circuits which can be used; however the manufacturer shall demonstrate to the Government that other test circuits which they may desire to use will give results within the desired accuracy of measurement. Circuits are shown for PNP transistors in one circuit configuration only. They may readily be adapted for NPN devices and for other circuit configurations.

4.3 Laboratory suitability. Prior to processing any semiconductor devices intended for use in any military system or sub-system, the facility performing the test(s) shall be audited by the DLA Land and Maritime, Sourcing and Qualification Division and be granted written Laboratory Suitability status for each test method to be employed. Processing of any devices by any facility without Laboratory Suitability status for the test methods used shall render the processed devices nonconforming.

5. DETAILED REQUIREMENTS

This section is not applicable to this standard.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory.)

6.1 Intended use. The intended use of this test method standard is to establish appropriate conditions for testing semiconductor devices to give test results that simulate the actual service conditions existing in the field. This test method standard has been prepared to provide uniform test methods, controls, and procedures for determining with predictability the suitability of such devices within military, aerospace and special application equipment.

6.2 International standardization agreement. Certain provisions of this test method standard are the subject of international standardization agreement. When amendment, revision, or cancellation of this test method standard is proposed which will affect or violate the international agreement concerned, the preparing activity will take appropriate reconciliation action through international standardization channels, including departmental standardization offices, if required.

6.3 Subject term (key word) listing.

Airborne particle classification
Capacitance voltage measurements
High reliability tests
Laboratory suitability

6.4 Supersession data. The main body (MIL–STD–750) and five parts (MIL–STD–750–1 through –5) of this revision replace the superseded MIL–STD–750E.

6.5 Change notations. The margins of this standard are marked with vertical lines to indicate modifications generated by this change. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations.

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METHOD 5001.2

WAFER LOT ACCEPTANCE TESTING

The content of this test method has been transferred to MIL–PRF–19500, appendix D.

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METHOD 5002

CAPACITANCE VOLTAGE MEASUREMENTS TO DETERMINE OXIDE QUALITY

1. Purpose. The purpose of this test method is to determine the quality of an oxide layer as indicated by capacitance-voltage (C/V) measurements of a metal-oxide semiconductor capacitor. The overall shape and position of the initial C/V curve can be interpreted in terms of the charge density, and to a certain extent charge type, at the oxide-semiconductor interface. By applying an appropriate bias while heating the sample to a moderate temperature (e.g., +200°C), the mobile ion contamination level of the sample oxide may be determined.

2. Apparatus/materials. Capacitance-voltage plotting system complete with heated/cooled stage and probe (Princeton Applied Research Model 410, MSI Electronics Model 868 or equivalent). A C/V plotter may be constructed from the following components (see figure 5002–1 for equipment setup).

2.1 Manual setup.

a. L-C meter (Boonton 72B or equivalent).

b. X-Y recorder (HP 7035B or equivalent).

c. DC voltmeter (Systron Donner 7050 or equivalent).

d. DC power supply, 0 to 100 volts.

e. Heated/cooled stage (Thermochuck TP-36 or equivalent).

f. Probe in micromanipulator.

2.2 Automatic C/V plotter. (CSM-16 or equivalent).

3. Suggested procedure.

3.1 Sample preparation.

a. The sample is typically a silicon wafer on which has been grown the oxide to be measured, or wafers with known clean oxide which is exposed to a furnace at temperature to measure the furnace cleanliness. An array of metal dots on the surface of the oxide provides the top electrodes of the metal-oxide semiconductor capacitors. The metal may either have been deposited through a shadow mask to form the dots, or it may have been deposited uniformly over the oxide surface and then etched into the dot pattern by photolithographic techniques. Cleanliness of the metal deposition is paramount. Contamination introduced during metal deposition is as catastrophic to the oxide quality as is contamination introduced during oxide growth. The metal shall have been annealed, except in cases where the method is being used to investigate the effectiveness of annealing.

   NOTE: This test method also may be used to determine metal deposition system cleanliness when used with oxide samples known to be contamination free.

b. The minimum dot size should be such that the capacitance of the MOS capacitor is greater than 20 pF.

c. The oxide thickness is typically 1,100 Å. Reduced sensitivity results from oxide thickness greater than 2,000 Å.

d. The backside of the sample shall have the oxide removed to expose the silicon. The backside may have metal, such as aluminum or gold deposited on it.

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3.2 C/V plot (at room temperature).

a. Place the wafer on the heated/cooled stage. Use vacuum to hold the wafer firmly in place.

b. Zero the capacitance meter as necessary, place the paper in X-Y plotter and set up the voltage source for the desired range.

c. Select the capacitor dot to be measured and carefully lower the probe to contact it.

d. Lower the pen on the X-Y plotter and sweep the voltage over the desired range so a C/V trace for an N-type substrate or P-type substrate, similar to that shown on figure 5002–2, is obtained.

NOTE: If an anomalous trace is obtained, it may be because the capacitor is leaking or shorted. In this case, another dot should be selected.

3.3 Mobile ion drift.

a. Use the capacitor dot measured in 3.2.

b. With the probe making good contact, apply a positive bias of 10_{10} v/cm to the capacitor dot. (For a 1,000 Å thick oxide, this is a 10-volt bias.) A different voltage is acceptable, if the manufacturer can demonstrate effectiveness.

c. Heat the sample to +300°C ±5°C with the bias applied. Hold at this temperature for 3 minutes (different times may be acceptable if the manufacturer can demonstrate effectiveness).

d. With the bias still applied, cool the sample to room temperature (the heating/cooling cycle can be automatically programmed if the Thermochuck system is used).

NOTE: Be certain that the probe does not lose contact with the capacitor dot during the heat/cool cycle. If it should, the test is invalid and should be repeated.

e. Lower the pen on the X-Y plotter and sweep the voltage over the range necessary to obtain a C/V trace similar to that obtained in 3.2.d. The trace may be displaced on the voltage scale from the original trace, but should be parallel to the original trace. Label this trace as the (+) trace.

f. Apply a negative bias of the same magnitude selected in 3.3.b to the capacitor dot and repeat steps 3.3.c and 3.3.d.

g. Lower the pen on the X-Y plotter and sweep the voltage over the range again. This trace may be displaced from the two previous traces and should be labeled as the (–) trace.

h. An automatic system that performs equivalent functions may be substituted for steps 3.3.b and 3.3.g.

3.4 Interpretation.

a. Determine the V_{FB} (voltage difference between original trace and bias trace, taken at 90 percent capacitance level (see figure 5002–2).

b. Determine the mobile ion contamination concentration (For mobile ion density versus voltage shift (V_{FB}) (see figure 5002–3)), N_O, as follows:

$$N_o = \left| \frac{\varepsilon 0 \ K_{ox} \ \Delta \ V_{FB}}{q \ t_{ox}} \right|$$

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Where:

$\varepsilon 0$ = permittivity of free space (8.85×10^{-12} coulomb volt^{-1} m^{-1}).

K_{ox} = dielectric constant of the oxide (3.8 for silicon dioxide).

q = the charge on an electron (1.6×10^{-19} coulomb).

t_{ox} = oxide thickness (in meters).

Example:

ΔV_{FB} (measured from C/V curves similar to those shown on figure 5002–2) = 1.4 V.

t_{ox} (measured on wafer prior to metal deposition) = 950 Å.

$$N_o = \left| \frac{(8.85 \times 10^{-12})\ (3.8)\ (3.14)}{(1.6 \times 10^{-19}\ (950 \times 10^{-10})} \right| \begin{array}{l} = 3.1 \times 10^{15}/\text{meter}^2 \\ = 3.1 \times 10^{11}/\text{cm}^2 \end{array} \Bigg|$$

So, the mobile ion contamination level is 3.1×10^{11} mobile ions per square centimeter in this example.

c. Considerably more information concerning the oxide and the semiconductor substrate can be obtained from interpretation of the C/V trace.

4. Summary.

4.1 Calibration. The voltage scale calibration of the X-Y plotter should be checked against the DVM during set up. Other instruments should be calibrated at regular intervals.

4.2 Accuracy. The voltage accuracy obtainable is ±0.1 volt and the ΔV_{FB} accuracy obtainable is ±0.2 volt. The practical lower limit of detectability of mobile ion contamination is on the order of $2 \times 10^{11}/\text{cm}^2$.

4.3 Documentation. Record results in appropriate control document.

Reference:

Whelon, N.V., "Graphical Relation Between Surface Parameters of Silicon, to be Used in Connections with MOS Capacitance Measurements", Phillips Res. Apt., 620-630 (1965).

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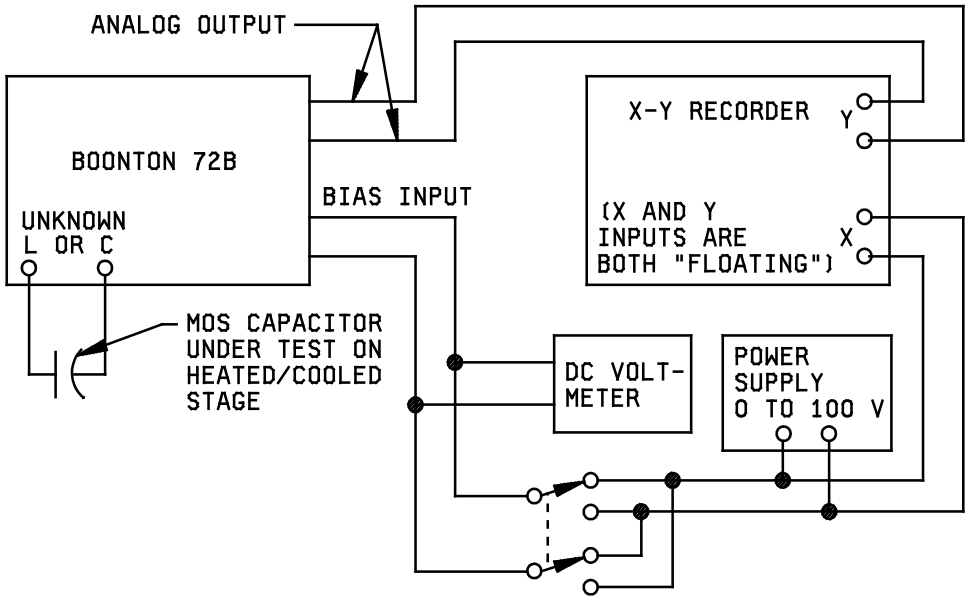

FIGURE 5002–1. Diagram of equipment set-up for measuring relationship of metal-insulator-semiconductor structures.

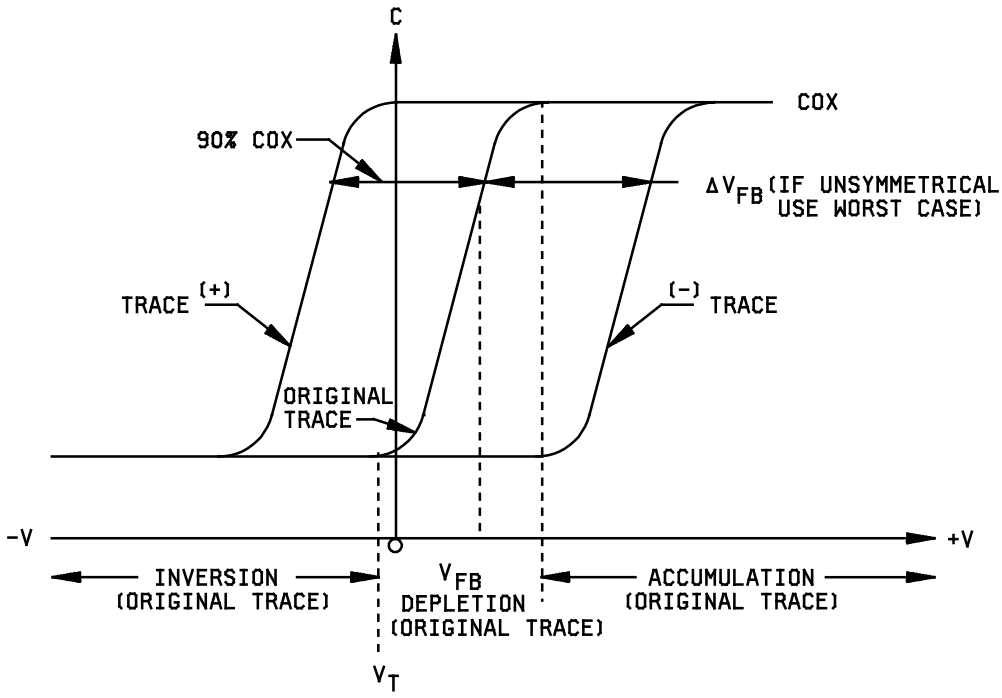

FIGURE 5002–2. Capacitance–voltage traces.

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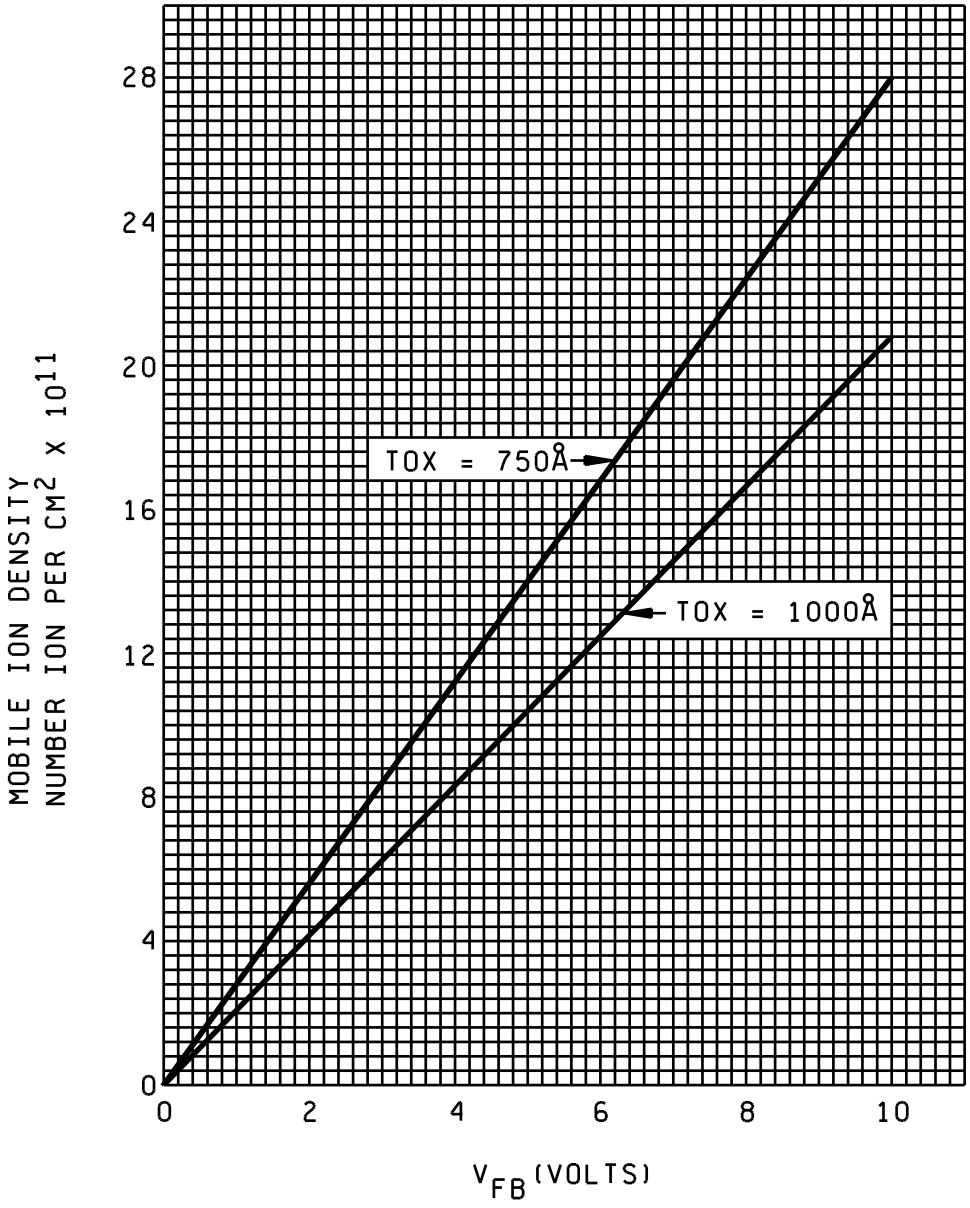

FIGURE 5002–3. Mobile ion density versus voltage shift (V_{FB}).

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METHOD 5010.2

CLEAN ROOM AND WORKSTATION AIRBORNE PARTICLE CLASSIFICATION AND MEASUREMENT

1. Purpose. This test method provides a classification system for, and means of measuring, air cleanliness. It is intended to be used in conjunction with the environmental controls specified in MIL–PRF–19500.

2. Air cleanliness classes. There are three classes defined by this method. Classifications are based upon particle count with a maximum allowable number of particles per unit volume 0.5 micron or larger, and 5.0 microns and larger. Particle counts are to be taken during normal work activity periods and at a location which will yield the particle count of the air as it approaches the work location.

2.1 Class 100 (3.5). Particle counts must not exceed a total of 100 particles per cubic foot (3.5 particles per liter) of a size of 0.5 micron or larger.

2.2 Class 1,000 (35). Particle counts must not exceed a total of 1,000 particles per cubic foot (35 particles per liter) of a size of 0.5 micron or larger of 7 particles per cubic foot (0.25 particles per liter) of a size 5.0 microns and larger.

2.3 Class 10,000 (350). Particle counts must not exceed a total of 10,000 particles per cubic foot (350 particles per liter) of a size of 0.5 micron or larger or 65 particles per cubic foot (2.3 particles per liter) of a size of 5.0 microns and larger.

2.4 Class 100,000 (3,500). Particle counts must not exceed a total of 100,000 particles per cubic foot (3,500 particles per liter) of a size of 0.5 micron or larger or 700 particles per cubic foot (25 particles per liter) of a size of 5.0 microns and larger.

3. Particle counting methods. For proof of meeting the requirements of the class of clean room or clean work station, one or more of the following particle counting methods shall be employed on the site of use.

3.1 Particle sizes 0.5 micron and larger. The equipment to be used must employ the light scattering measurement principle as specified in ASTM F50.

3.2 Particle sizes 5.0 micron and larger. A microscopic counting of particles collected on a membrane filter, through which a sample of the air to be measured has been drawn, may be used in lieu of the light scattering measurement principle as specified in ASTM F25.

4. Monitoring techniques. Appropriate equipment shall be selected and monitoring routines established to measure the air cleanliness levels under normal use conditions.

5. Items to be specified. The general specification shall specify the following information:

a. The class of the workstation or clean room.

b. The frequency of test. Unless otherwise specified, this frequency shall be, at a minimum, once per month per working shift.

c. The locations within the clean environment to be monitored.

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CONCLUDING MATERIAL

Custodians:
Army – CR
Navy – EC
Air Force – 85
NASA – NA
DLA – CC

Review activities:
Army – AR, MI, SM
Navy – AS, CG, MC, SH
Air Force – 19
Other – NRO

Preparing activity:
DLA – CC

Project: 5961–2018–037

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