MILITARY STANDARD

PRINTED WIRING FOR

ELECTRONIC EQUIPMENT

TO ALL HOLDERS OF MIL-STD-275E:

1. THE FOLLOWING PAGES OF MIL-STD-275E HAVE BEEN REVISED AND SUPERSEDE THE PAGES LISTED:

NEW PAGE	DATE	SUPERSEDED PAGE	DATE
5	31 December 1984	5	REPRINTED WITHOUT CHANGE
6	8 July 1986	6	31 December 1984
17	8 July 1986	17	31 December 1984
18	8 July 1986	18	31 December 1984
19	8 July 1986	19	31 December 1984
20	31 December 1984	20	REPRINTED WITHOUT CHANGE
21	8 July 1986	21	31 December 1984
22	31 December 1984	22	REPRINTED WITHOUT CHANGE
23	31 December 1984	23	REPRINTED WITHOUT CHANGE
24	8 July 1986	24	31 December 1984
27	8 July 1986	27	31 December 1984
28	8 July 1986	28	31 December 1984
31	8 July 1986	31	31 December 1984
32	31 December 1984	32	REPRINTED WITHOUT CHANGE
41	8 July 1986	41	31 December 1984
42	31 December 1984	42	REPRINTED WITHOUT CHANGE

2. RETAIN THIS NOTICE AND INSERT BEFORE TABLE OF CONTENTS.

3. Holders of MIL-STD-275E will verify that page changes and additions indicated above have been entered. This notice page will be retained as a check sheet. This issuance, together with appended pages, is a separate publication. Each notice is to be retained by stocking points until the military standard is completely revised or canceled.

Custodians:
Army - ER
Navy - EC
Air Force - 17

Review activities:
Army - AR, EA, MI
Navy - AS, OS, SH
Air Force - 11, 16, 19, 85, 99
DLA - ES
NSA/S512

User activities:
Navy - CG, MC

Preparing activity:
Navy - EC

Agent:
DLA - ES

(Project 5999-0176)

4. GENERAL REQUIREMENTS

4.1 Design features. The design features of the printed-wiring boards shall be in accordance with this standard. Quality conformance test circuitry shall also be included on the production master. Quality conformance test circuitry shall be included on each panel and shall be in accordance with figure 1 and 5.9. Test circuitry shall be not more than 0.5 inch (13 mm) and shall be not less than 0.25 inch (6.4 mm) from the edge of the printed board, and represents all the manufacturing processes such as drilling, plating, etching, fusing, ground/voltage/thermal/mechanical planes or cores, separately fabricated layers, permanent coatings (solder mask) and so forth.

4.2 Documentation. Requirements for drawing content may be satisfied by direct delineation on the drawing or by reference to other documents which are part of the engineering drawing set (see figure 2).

4.2.1 Reference designations. Reference designations of components to be mounted on printed-wiring boards, when specified on the master drawing or the printed-wiring assembly drawing, shall be in accordance with IEEE-STD-200.

4.2.2 Deviation request and approval. When a deviation to this standard is necessary, or has been granted in the initial contract design description, the contractor (before proceeding further) shall furnish each proposed master drawing, or a detailed deviation request to the Government Agency concerned for approval with justification for the deviation. If approved, all deviations granted shall be documented on the master drawing.

4.2.3 Government furnished master drawings. Any deviation from this standard or drawing shall have been recorded on the Government approved master drawing or a Government approved deviations list. When new or additional deviations from this standard or drawing are necessary, the contractor (before processing further) shall furnish one copy of each proposed master drawing being revised, or a detailed deviation request to the Government Agency concerned for approval with justification for the deviation. If approved, all deviations granted shall be documented on the master drawing or the Government approved deviations list.

4.2.4 Conflicts. In the event of any conflict between the approved master drawing supplemented by an approved deviation list, if applicable, and the requirements of this standard, the approved master drawing and deviations list shall take precedence.

4.3 Master drawing. The master drawing shall be prepared in accordance with DOD-STD-100, shall include all appropriate detail board requirements (see section 5), and the following:

a. The type, size, and shape of the printed-wiring board.
b. The size, location, and tolerance of all holes therein.
c. Etchback allowances, when required or permitted.
d. Location of traceability marking.
e. Dielectric separation between layers.
f. Shape and arrangement of both conductors and nonconductor patterns defined on each layer of the printed-wiring board. Copies of the production masters or copies of the artwork may be used to define these patterns.
g. Separate views of each conductor layer.
h. Any and all pattern features not controlled by the hole sizes and locations shall be dimensioned either specifically, or by reference to the grid system (see n).
i. Processing allowances that were used in the design of the printed-wiring board (see 5.1.1, 5.1.4, 5.2.1.2, 5.2.2, and 5.2.2.6).
j. All notes either included on the first sheet(s) of the master drawing or by specifying the location of the notes on the first sheet.
k. Conductor layers numbered consecutively starting with the component side as layer 1. If there are no conductors or lands on the component side, the next layer shall be layer 1. For assemblies with components on both sides, the most densely populated side shall be layer 1.

l. Identification marking (see 5.8).
m. Size, shape, and location of reference designation and legend markings, if required (see h).
n. A modular grid system to identify all holes, test points, lands, and overall board dimensions with modular units of length of 0.100, 0.050, 0.025, or other multiples of 0.005 inch in that order of preference. For design where the majority component locations are metric-based (SI), the basic modular units of length shall be 2.0, 1.0, 0.5, or other multiples of 0.1 mm in that order of preference. The grid system shall be applied in the X and Y axes of the Cartesian coordinates. The grid shall not be reproduced on the master drawing, but may be indicated using grid scales or X, Y control dimensions (see figure 3).
o. Dimensions for critical pattern features which may effect circuit performance because of distributed inductance or capacitance effects within the tolerance required for circuit performance.
p. All terms used on the master drawing shall be in conformance with the definitions of ANSI/IPC-T-50 or ANSI Y14.5 (see 3.1 and 2.2).
q. Deviations to this standard (see 4.2.2).
r. Minimum line width and spacing of the finished printed-wiring board.
s. Maximum rated voltage (maximum voltage between the two nonconnected adjacent conductors with the greatest potential difference) for type 3 boards only.
t. Plating and coating material(s) and thickness(es).
u. Identification of test points required by the design (see 5.1.8).
v. Applicable fabrication specification with date(s), revision letter, and amendment number.

When continuation sheets of a drawing are used for conductor pattern definition, they need not be prepared on standard drawing forms provided standard sheet sizes are used with standard continuation sheet title blocks in accordance with ANSI Y14.1 located in the lower right corner of each sheet. Numeric form of end product descriptions shall be in accordance with IPC-D-350.

4.3.1 Hole location tolerance. Unless otherwise specified, the location of holes shall be dimensioned and toleranced with respect to single or secondary grid systems. Each distinctive hole pattern (such as, plated-through holes, tooling holes, mounting holes, windows, access holes, and so forth), may require separate consideration or specification of tolerance. Producibility considerations are presented in table VI.

4.3.2 Processing allowances. The processing allowances which were considered in the design and artwork preparation for the printed-wiring board shall be documented and defined on the master drawing in either note form or by reference to another drawing which contains artwork requirements or specifications. This information shall be expressed in terms of the maximum variation between the end-product conductor widths and spacings and what may appear on the artwork; the minimum land, in reference to the drilled or plated hole and what may appear on the artwork; or any other feature conditions considered in the design where the variation between end-product and artwork configuration play a role in the producibility of the printed-wiring board.

4.3.3 Datums. There shall be a minimum of two datum features to establish the mutually perpendicular datum reference frame for each board. These datums shall be established by at least two holes, points, symbols, or other datum features, but not edges. Critical design features may require the use of more than one set of datum references. The master drawing shall establish the relationship and acceptable tolerance between all datum features. All datum features shall be located on grid or establish grid criterion, as defined on the master drawing, and should be on or within the outline of the printed-wiring boards.

5.7.5 Bow and twist. Unless otherwise specified on the master drawing, the maximum allowable bow and twist shall be 1.5 percent.

5.8 Detail board marking requirements. Individual printed-wiring boards and quality conformance test circuitry shall be identified in accordance with the master drawing and MIL-STD-130. Provisions shall be made in the design for locating the traceability and date markings that are additionally required by the fabrication specification. The methods and materials for marking shall be specified on the master drawing. If ESD marking is required at the board level, it shall be specified on the master drawing. Marking shall be of a contrasting color to the background.

5.9 Quality conformance testing circuitry. The quality conformance test circuitry, comprised of the coupons shown on figure 1, shall be a part of every panel used to produce printed-wiring boards that are designed to this standard. The minimum number of coupons per panel and the requirements for positioning will be in accordance with table V. Coupons A, B, and F shall be positioned in accordance with 4.1 and figure 17. All other coupons may be positioned at optional locations. All coupons required shall be shown on the master drawing, artwork, and production master.

TABLE V. Conformance test circuitry.

Coupon type	Type 1 board	Type 2 board	Type 3 board
A Microsection	Not required	Three per panel. Opposite corners location fixed by artwork (see figure 17). Location of third optional.	Three per panel. Opposite corners location fixed by artwork (see figure 17). Location of third optional.
B Microsection	Twice per panel opposite corners location fixed by artwork (see figure 17).	Three per panel. Opposite corners location fixed by artwork (see figure 17). Location of third optional.	Three per panel. Opposite corners location fixed by artwork (see figure 17). Location of third optional.
C Plating	Once per panel location optional pattern defined by artwork	Once per panel location optional pattern defined by artwork	Once per panel location optional pattern defined by artwork
E 1/ Insulation resistance	Once per panel location optional pattern defined by artwork	Once per panel location optional pattern defined by artwork	Once per panel location optional pattern defined by artwork
F 2/ Registration	Not required	Not required	Twice per panel opposite corners location fixed by artwork (see figure 1)
J Solder mask	When required, once per panel with solder mask location optional pattern fixed by artwork	When required, once per panel with solder mask location optional pattern fixed by artwork	When required, once per panel with solder mask location optional pattern fixed by artwork

1/ If the panel has solder mask, the E coupon shall be covered with the solder mask. Clearances of 0.010 ±0.005 should be provided for all surface lands.
2/ Registration coupons are optional and may be used in lieu of microsection evaluation for registration.

6. DETAIL PART MOUNTING REQUIREMENTS

6.1 Approved methods of attachment. Component leads shall pass through lead component holes and be attached or the component terminals or leads shall be surface mounted to the land pattern. Part attachment shall be described on the assembly drawing following the methods specified in 6.1.2 through 6.1.5.4. General mounting requirements shall be as specified in 6.1.1.

6.1.1 Unclinched leads. Unless otherwise specified, unclinched leads (either straight or partially bent for retention) shall be soldered in component holes or eyelets in accordance with IPC-S-815. If no clinching requirements are specified on the assembly drawing, unclinched lead termination shall apply.

6.1.1.1 In unsupported holes. Lead tip projection shall be required to extend from 0.020 inch (0.51 mm) minimum to 0.060 inch (1.5 mm) maximum from the surface of the foil.

6.1.1.2 In plated-through or eyeletted holes. The lead shall be required to extend at least to the surface of the plating or rim of the eyelet and extend no more than 0.060 inch (1.5 mm) from the plating surface or eyelet. The straight-through leads on connectors shall extend from -.009 to +.076 inch from the plating surface or eyelet.

6.1.2 Clinched leads. When maximum mechanical retention of a lead or terminal is required by design, the lead or terminal shall be clinched. The component holes may be plated-through holes, unsupported holes, or eyeletted holes. Clinching requirements shall be defined on the assembly drawing. The lead end shall not extend beyond the edge of its land or its electrically connected conductor pattern in violation of the minimum spacing requirement. Partial clinching of leads for part retention shall be considered under the requirements of 6.1.1.

6.1.3 Surface terminated ribbon leads. Flat-wire ribbon leads may be attached to lands on the printed-wiring board. Connections shall be made by soldering only. The contact area between any lead and land shall be not less than a square having each side equal to the nominal width of the lead (see figure 9). Minimum conductor spacing indicated in 5.1.4 shall be maintained. Attachment details may be conveyed by an assembly drawing reference to IPC-S-815 (see figure 18). For additional mounting notes and considerations see 6.2.11.

6.1.4 Surface terminated round leads. With prior approval by the government acquiring activity, designs may stipulate that parts shall be attached with their round leads soldered to surface terminals (lands) without first passing through a hole. The lands shall be designed with proper shape and spacing to comply with proper soldering techniques (see IPC-S-815).

6.1.5 Standoff terminals, eyelets, or fasteners.

6.1.5.1 Component attachment to standoffs. Component attachment to standoff terminals, shall be defined on the assembly drawing and meet the requirements of IPC-S-815. Placement of terminals shall be specified to suit each application.

6.1.5.2 Attachment of standoffs to boards. A terminal of the funnel flanged type shall be specified wherever the flange must be soldered for electrical connection to a land. The included angle of such flange shall be between 35 and 120 degrees.

6.1.5.3 Eyelets. Eyelet applications used in design shall be in compliance with the following:

Attachment requirements - Interfacial connections shall not be made with eyelets. Eyelets installed at an electrically functional land shall be required to be of the funnel flange type.

6.1.5.4 Fastening hardware. The installed location and installation orientation shall be prescribed on the assembly drawing for any fastening devices such as rivets, machine screws, washers, inserts, nuts, and bracketing. Precautions such as the specification of tightening torque values shall be provided wherever general assembly practices might be inadequate or detrimental to the board assembly's structure or functioning.

6.2 Electrical part mounting. The following are requirements the designer shall consider and detail on the assembly drawing in specific notes or illustrations. All such electrical parts, hereafter referred to as components, shall also be selected so as to withstand the vibration, mechanical shock, humidity, and other environmental conditions the design must endure when the components are installed in accordance with 6.2.1 through 6.2.14.

6.2.1 One side only. Parts shall be mounted on only one side of the printed-wiring board assembly whenever possible.

6.2.2 Accessibility. Lands and terminals shall be located and spaced so that the terminations of each component are not obscured by any other component, or by any other permanently installed parts. Each component shall be capable of being removed from the assembly without having to remove any other component.

6.2.3 Design envelope. Unless otherwise detailed on the assembly drawing, the board edge is regarded as the extreme perimeter of the assembly, beyond which no portion of a component is allowed to extend. The designer shall prescribe the design envelope with due respect for maximum part body dimensions and the mounting provisions dictated by the board and assembly documentation.

6.2.4 Over conductive areas. No parts shall be mounted in direct contact with external conductor areas unless required for thermal dissipation. If design limitations require placement of parts over conductive areas, the part shall be mounted so that subsequent insulating coating will cover the conductive area under the part or conductive areas under parts shall be insulated or protected against moisture entrapment by applying conformal coating or a cured resin coating by laminating low-flow prepreg material in accordance with MIL-P-13949, or by solder masking over the area prior to mounting the part.

6.2.5 Thermal transfer. Components, which for thermal reasons require extensive surface contact with the board or with a heat sink mounted on the board, shall be protected from processing solutions at the conductive interface. To prevent risk of entrapment, compatible materials and methods shall be specified to seal the interface from entry of corrosive and conductive contaminants.

NOTE: Even totally nonmetallic interfaces that are prone to entrap fluids can have adverse effects on the fabricator's ability to pass required cleanliness tests.

6.2.6 Components dissipating one or more watts. Design for heat dissipation of components shall insure that the maximum allowable temperature of the board material is not exceeded under operating conditions specified in 5.6. Heat dissipation may be accomplished by requiring a gap between board and component, using a clamp or thermal mounting plate, or attaching a compatible, thermally conductive material working in conjunction with a thermal bus plane to the component.

6.2.7 Stress relief bends. Lands and terminals shall be located by design so that components can be mounted or provided with stress relief bends in such a manner that the leads cannot overstress the part lead interface when subjected to the anticipated environments of temperature, vibration, and shock of MIL-P-28809. The lead length for stress relief and lead bend radius shall be in accordance with figure 19. Where lead bending cannot be in accordance with figure 19 in order to achieve design goals, the bends shall be detailed on the assembly drawing.

6.2.8 Mechanical support. All parts weighing 0.25 ounce (7.1 g) or more per lead (.04-inch diameter) shall be supported by clamps or other specified means which will insure that the soldered joints and leads are not relied upon for mechanical strength.

6.2.9 Axial-leaded parts. Axial-leaded parts shall be mounted as specified on the approved assembly drawing and mounted so that a portion of the body is as close to the printed-wiring board as possible. The leads shall be shaped in accordance with 6.2.7. This does not apply to parts mounted on standoff terminals (see 6.1.5.1).

5.2.9.1 Perpendicular mounting. Axial-leaded components weighing less than 0.50 ounce (14 g) may be mounted on the assembly using perpendicular mounting criteria. The assembly drawing shall prescribe a minimum of 0.015 inch (0.38 mm) space between the end of the component body (or the lead-weld) and the board. Unless otherwise noted on the assembly drawing, components required to be perpendicularly mounted shall be installed with their major axis within ±15 degrees of a right angle with board surface. The maximum vertical height from the board surface shall be 0.55 inch (14 mm) (see figure 20).

6.2.10 Nonaxial-leaded parts. Nonaxial-leaded parts shall be mounted with the surface from which the lead projects a minimum of 0.010 inch (0.25 mm) above the printed-wiring board surface. Dimensioning of the required spacing under these components is generally not required unless the component package design could result in an assembly error. For thermal considerations see 6.2.5 and 6.2.6.

6.2.11 Multiple-leaded components. Multiple-leaded components (components with three or more leads), except multiple leaded components mounted to thermal planes or heat sinks, shall be mounted in such a manner that components are spaced off the board to facilitate cleaning, provide electrical isolation, and to prevent moisture traps. The necessary gap may be prescribed as an exceptional fabrication requirement by identifying the subject component and prescribing the required underbody clearance dimension, or the gap may be achieved by virtue of the component's own standoff features. Unless otherwise specified, a clearance of 0.010 inch (0.25 mm) minimum applies.

6.2.11.1 Spacers. Special spacers (such as feet, ribs, or projections) with minimal contact may be prescribed to go under the component, provided they will not impair soldering or the assembly's performance.

6.2.11.2 Sealing. The need for a gap between component body and board may be avoided by requiring the interface under the component to be sealed with adhesive or a combination of adhesive and insulation material, which is compatible with the board, parts, and conformal coating. This option exists only if all lead terminations are external to the seal. Repairability shall not be precluded by the method or material selection.

6.2.12 Surface mounted components. The requirements and considerations of 6.2.4 apply to this class of components. Space for cleaning shall be provided to reduce entrapment.

6.2.12.1 Flat-pack types with ribbon leads. Lead forming is a major design consideration and shall be detailed on the assembly drawing to provide for lead stress relief, fit to the land pattern, underbody clearance for cleaning, and any designed-in provisions for thermal transfer (see figure 18 and 6.1.3).

6.2.12.2 Chip carrier types. Leadless components may be attached to the surface of a land. The component shall be attached to the land of the printed-wiring board in a way that provides sufficient space under the body of the component to facilitate cleaning. Land pattern design shall facilitate adequate solder fillets between the conductor pattern and the component.

6.2.12.3 End-cap discrete components. End-cap discrete resistor and capacitor components and similar leadless end-cap discrete components shall be mounted to printed wiring or printed circuitry. The devices shall not be stacked nor shall they bridge spacing between other parts or components, such as terminals or other properly-mounted components.

6.2.12.4 Surface mounting of flattened round leaded components. Components with axial leads of round cross-sections shall be utilized for surface mounting only if the leads are coined or flattened for positive receding. For flattened round leads with original diameter of 0.025 inch (0.635 mm) or greater, the flattened thickness shall be 70 percent of the original diameter, minimum. For leads with an original diameter less than the 0.025 inch (0.635 mm), the flattened thickness shall be 50 percent of the original diameter, minimum. The body of a planar mounted axial leaded component should be spaced away from the board to facilitate cleaning.

6.2.13 Two-part connectors (plug and receptacle). Two-part connectors containing male and female quick disconnect electrical contacts and integral aligning hardware to assure proper mating of the contacts shall be specified as the only means to integrate plug-in printed-wiring assemblies. Their attachment and mounting methods are subject to the design concerns of 6.1, 6.2.3, and 6.2.4. Board connectors may be uniquely keyed in such a manner only insertion of the proper assembly is possible.

6.2.13.1 Wires. Use of hard wiring directly to plug in connector mounted printed-wiring board assemblies shall not be permitted. Plug in assemblies shall have all external electrical connections accomplished through the use of two-part connectors.

6.2.14 Jumper wires. Jumper wires may be used on types 1, 2, or 3 printed-wiring board assemblies. Jumper wires shall be terminated in holes or standoffs. They may also be terminated on lands with prior approval of the government acquiring activity. Jumper wires shall be considered a component. Jumper wires shall be as short as practicable and shall not be applied over or under other replaceable components (including jumper wires). Jumper wires must be permanently fixed to the printed-wiring board at intervals not to exceed 1 inch. Jumper wires less than 0.50 inch in length whose path does not pass over conductive areas and does not violate the spacing requirements (see 5.1.4) may be uninsulated. Insulation, when required, or jumper wires shall be compatible with the conformal coating.

6.3 Conformal coating. The design criteria contained in this standard are predicated on the requirement that end item assemblies shall be conformally coated. Solder mask shall not be used in lieu of conformal coating.

6.3.1 Coating area. Printed-wiring assemblies shall be conformally coated with a coating material that conforms to MIL-I-46058. The coating shall be applied to both sides of the cleaned printed-wiring assembly including the part leads. The type of conformal coating shall be listed on the assembly drawing.

6.3.1.1 Surfaces to be free of coating. Surfaces specified on the approved assembly drawing to be free of conformal coating shall be suitably masked and protected from coating, coating residues, and masking residues. The masking material used shall have no deleterious effects on the printed-wiring boards. Printed-wiring assemblies having adjustable components shall not have the adjustable portion covered with coating. Electrical and mechanical mating surfaces, such as probe points, screw threads, bearing surfaces (e.g., card guides), and so forth shall not be coated.

6.3.2 Cleaning agents. Cleaning agents and techniques shall have no deleterious effects on any part of the printed-wiring assembly.

6.3.3 Compatibility. The conformal coating shall be compatible with all parts of the printed-wiring assembly.

6.3.4 Thickness. The thickness of the conformal coating shall be as follows for the type specified, when measured on a flat unencumbered surface:

a. Types ER, UR, and AR: 0.003 ±0.002 inch (0.08 ±0.05 mm).
b. Type SR: 0.005 ±0.003 inch (0.13 ±0.08 mm).
c. Type XY: 0.0005 to 0.002 inch (0.10 to 0.05 mm).

6.3.5 Electrical performance. Printed-wiring assemblies shall be constructed, adequately masked, or otherwise protected in such a manner that application of conformal coating does not degrade the electrical performance of the assembly.

6.3.6 Buffer material. If component(s) on the printed-wiring assembly are made of brittle material (glass or ceramic), they shall be protected against breakage by a buffer material before applying the conformal coating to the assembly. The buffer material shall be a thin, pliant material such as polyvinylidene fluoride, polyethylene terephthalate, or silicon rubber, and be nonreactive with the conformal coating material and all parts of the printed-wiring assembly. The buffer material shall be fungus resistant and flame retardant, and clear or transparent, so markings on the components are visible.

6.3.6.1 When required. When conformal coating types SR, XY, UR, and AR are used, buffer material is not required. Buffer material will be required for type ER.

NOTE: Board designers are cautioned to consider that buffer material may be needed when allocating space and location for components to be mounted on printed-wiring boards covered by this standard.

6.4 Support. All printed-wiring assemblies shall be supported within a maximum of 1 inch (25.4 mm) of the edges on at least two opposite sides. Support shall be sufficient to prevent fracture or loosening of the foil or breakage of the parts or part leads resulting from flexing of the printed-wiring boards.

6.5 Detailed assembly markings. Completed printed-wiring assemblies shall be marked in accordance with the assembly drawing and MIL-STD-130 with their full identification. Printed-wiring assemblies which contain electrostatic discharge sensitive devices shall be marked in accordance with DOD-STD-1686. The marking shall be etched or applied by the use of a permanent ink which will withstand assembly processing. Additional markings if required shall be specified on the assembly drawing.

APPENDIX

10. SCOPE

10.1 Purpose. This appendix is for guidance to the designer of printed-wiring boards.

20. DESIGN CONSIDERATIONS

20.1 Design process tolerances and allowances. The data in table IV shall serve as a guide concerning the tolerances and allowances used in the design process. Due to tolerance buildup, the tradeoffs involved in arriving at the permissible limits for each particular tolerance for a particular design should be recognized. This data is intended to show the increasing difficulty of producing boards with tighter tolerances, but does not express the limits attainable or permissible for any single aspect of board design. This data shall not be interpreted as end item board requirements.

20.2 Board dimensions. Extreme length-to-width ratios should be avoided.

20.3 Dimensional stability. While MIL-P-13949 limits the allowable dimensional change of the thin laminate, consideration must be given to the fact that during processing, the thin laminate may either expand or contract within these limits, and in addition, the change may vary across different portions of the board. The result may be misregistration, and bow and twist beyond that which would be expected from a simple dimensional change.

20.4 Dielectric constant and dissipation factor. When designing circuits which depend on stable dielectric properties, consideration should be given to the fact that MIL-P-13949 sets forth only a maximum for these values and that some materials which meet the thin laminate specifications will have values 15 percent lower than the specification requirement.

20.5 Surface preparation of large conductive areas. The adhesion of prepregs and other polymers, such as solder mask to large conductive areas, may be improved through the use of special materials and surface preparations. The use of adhesion promoters, such as oxide treatments and double treated copper may improve the bonding of type 3 printed-wiring boards. A protective chemical treatment may be required to prevent a reaction between the copper surface and the polymer coating.

20.6 High voltage factors (considerations):

a. Encapsulate with void-free potting materials, well bonded to all surfaces.
b. Avoid sharp projections.
c. Arrange conductors so that high and low voltage groups are separate from one another.
d. Provide rounded corners on electrical conductors and ground planes next to energized circuits.
e. In ac circuits, check adjacent conductors for instantaneous voltage differences between them.
f. Conformal coating should consist of at least three separate layers, with each layer applied at right angles to the previous layer.
g. Solder terminations on the printed-wiring board must be smooth and even with no projections from the component lead or solder spikes.
h. Standoff terminal connections must be solder balled. The radius of the solder ball should be at least 1/6 of the spacing between the solder ball and adjacent high voltage circuit or ground plane. When large spacings are involved, the solder ball should be at least .125 inch (3.1 mm) in diameter.

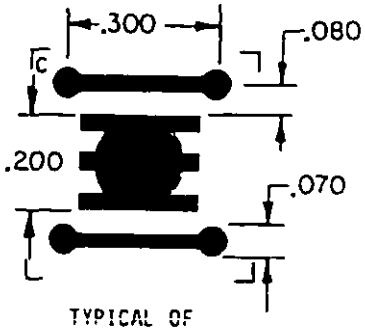
APPENDIX

TABLE VI. Composite board design guidance.

	Preferred	Standard	Reduced producibility
Number of conductor layers (maximum 1/)	6	12	20
Thickness of total board (maximum) (inch)	0.100(2.54)	0.150(3.81)	0.200(5.08)
Board thickness tolerance	±10% of above nominal	or 0.007(0.18),	whichever is greater
Thickness of dielectric (minimum)	0.008(0.20)	0.006(0.15)	0.004(0.10)
Minimum conductor width (or figure 4 value, whichever is greater)			
Internal	0.015(0.38)	0.010(0.25)	0.004(0.10)
External	0.020(0.51)	0.015(0.38)	0.004(0.10)
Conductor width tolerance			
Unplated 2 oz/ft$_2$	+0.004(0.10) -0.006(0.15)	+0.002(0.05) -0.005(0.13)	+0.001(0.025) -0.003(0.08)
Unplated 1 oz/ft^2	+0.002(0.05) -0.003(0.08)	+0.001(0.025) -0.002(0.05)	+0.001(0.025) -0.001(0.025)
Protective plated (metallic etch resist over 2 oz/ft$_2$ copper)	+0.008(0.20) -0.006(0.15)	+0.004(0.10) -0.006(0.10)	+0.002(0.05) -0.004(0.05)
Minimum conductor spacing (or table I, whichever is greater)	0.020(0.51)	0.010(025)	0.005(0.13)
Annular ring plated-through hole (minimum)			
Internal	0.008(0.20)	0.005(0.13)	0.002(0.05)
External	0.010(0.25)	0.008(0.20)	0.005(0.13) 2/
Feature location tolerance (master pattern, material movement, and registration			
Longest board dimension 12" or less	0.008(0.20)	0.007(0.18)	0.006(0.15)
Longest board dimension over 12"	0.010(0.25)	0.009(0.23)	0.008(0.20)
Master pattern accuracy			
Longest board dimension 12" or less	0.004(0.10)	0.003(0.08)	0.002(0.05)
Longest board dimension over 12"	0.005(0.13)	0.004(0.10)	0.003(0.08)
Feature size tolerance	±0.003(0.08)	±0.002(0.05)	±0.001(0.025)
Board thickness to plated hole diameter (maximum)	3:1	4:1	5:1
Hole location tolerance			
Longest board dimension 12" or less	0.005(0.13)	0.003(0.08)	0.002(0.05) 3/
Longest board dimension over 12"	0.007(0.18)	0.005(0.13)	0.003(0.08) 3/
Unplated hole diameter tolerance (unilateral)			
Up to 0.032(0.81)	0.004(0.10)	0.003(0.08)	0.002(0.05)
0.033(0.84)-0.063(1.61)	0.006(0.15)	0.004(0.10)	0.002(0.05)
0.064(1.63)-0.188(4.77)	0.008(0.20)	0.006(0.15)	0.004(0.10)

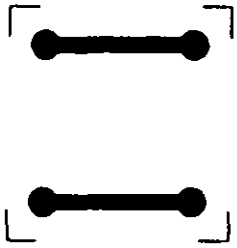
See footnotes at the end of table.

COUPON "C"

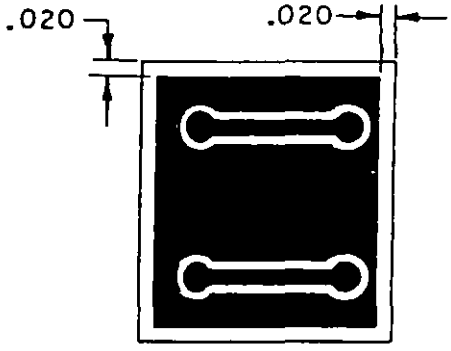


TYPICAL OF
SURFACE
LAYERS
TYPE 1, 2, 3
BOARDS

See Note 12



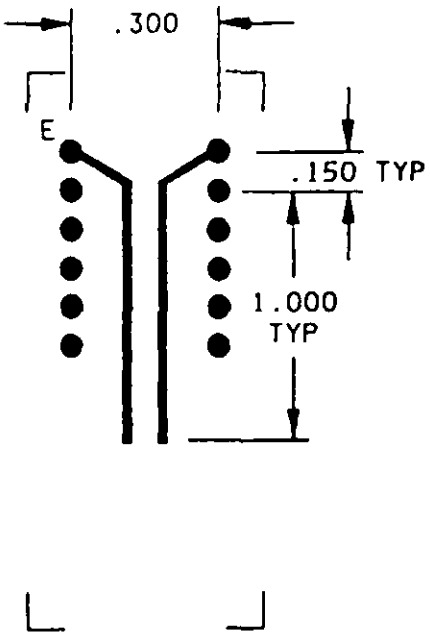
TYPICAL OF
INTERNAL
CIRCUIT
LAYERS
TYPE 3
BOARDS



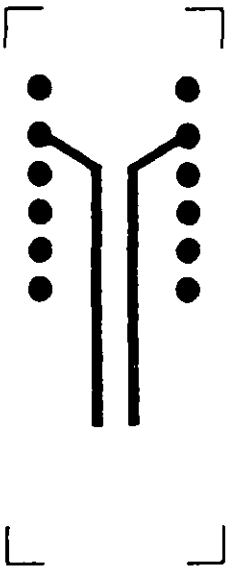
TYPICAL OF
INTERNAL
PLANE
LAYERS
TYPE 3
BOARDS

FIGURE 1. Quality conformance test circuitry.

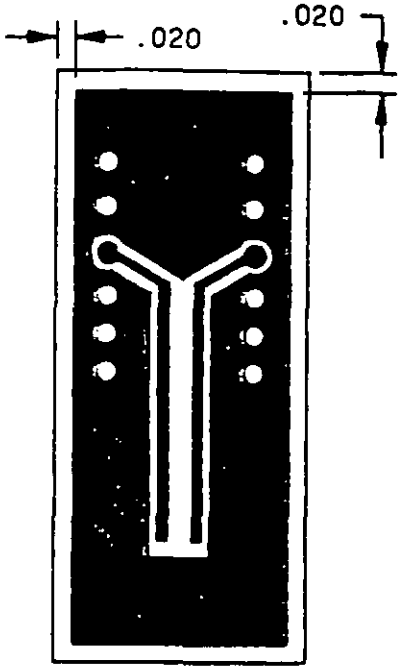
COUPON "E"



LAYER 1 OF
TYPE 1, 2,
AND 3 BOARDS



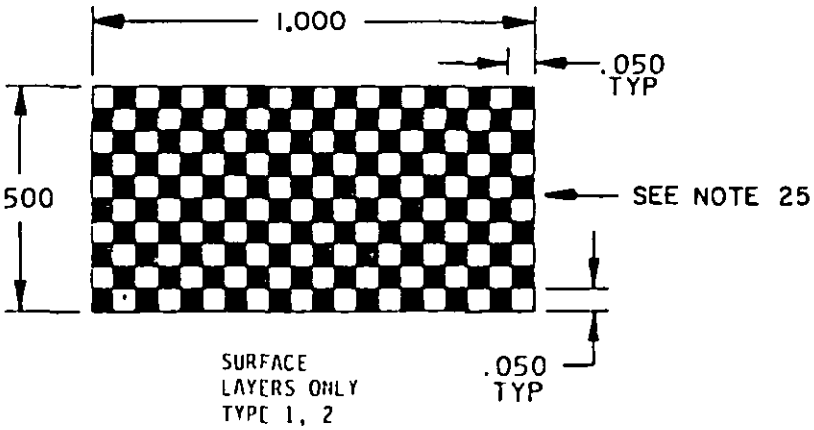
LAYER 2 OF
TYPE 2 AND
3 BOARDS
TYPICAL OF
INTERNAL
CIRCUIT
LAYERS



TYPICAL OF
INTERNAL
PLANES OF
TYPE 3
BOARDS

See Notes 8, 11, and 12.

COUPON "J"



SURFACE
LAYERS ONLY
TYPE 1, 2
AND 3 BOARDS

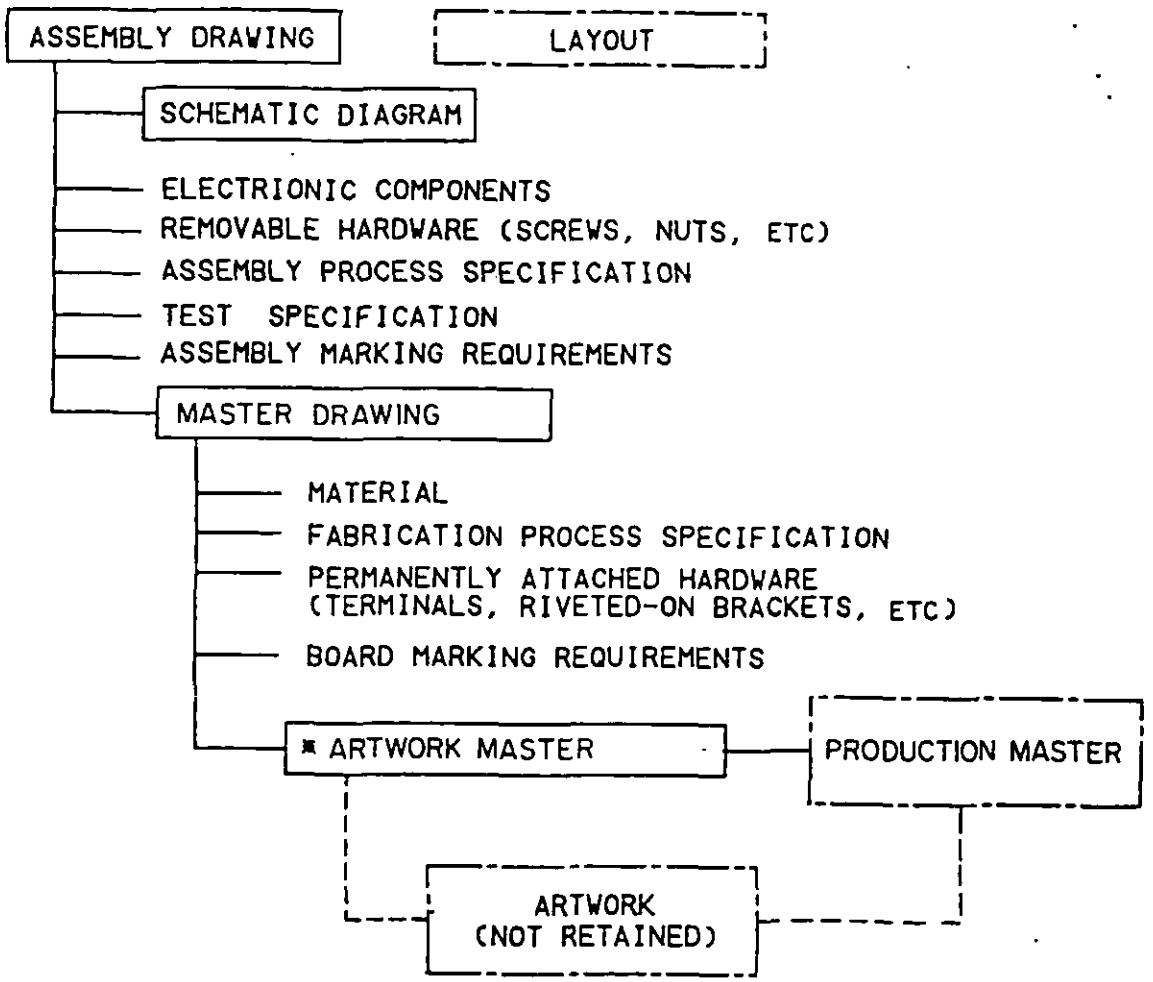
See Notes 12 and 16.

Inches	mm
.020	0.51
.050	1.27
.070	1.78
.080	2.03
.150	3.81
.200	5.08
.300	7.62
.500	12.70
1.000	25.40

FIGURE 1. Quality conformance test circuitry - Continued.

NOTES:
1. Test coupons are to be identified with the following:
   a. FSCM of board manufacturers.
   b. Part number and revision letter of master drawing.
   c. Board traceability.
   d. Lot number.
2. Dimensions are in inches.
3. Metric equivalents are given for general information only.
4. Unless otherwise specified, all conductors shall be .020 inch (0.51 mm) ±.003 (0.08 mm) wide.
5. Unless otherwise specified, the tolerances shall meet the requirements of this specification.
6. Unless otherwise specified, the minimum land dimension shall be .070 inch (1.78 mm) ±.005 inch (0.13 mm) and may represent the land shape used on the associated board. Holes in the land areas shall be the diameter of the smallest component hole in the associated board (see note 10).
7. Coupons for surface layers or internal layers shall be representative of the type of circuitry on the associated layer. Any layer with large copper planes shall use the appropriate plane coupon where applicable on the layer that is being represented by the coupon.
8. The lengths of coupons E and F are dependent upon the number of layers in the panel.
9. Intentionally left blank.
10. For coupons A and B, the minimum land dimension and shape shall be that used on the associated board. The hole shall be the maximum used in this minimum land dimension.
11. For coupon E, a pair of holes, and the conductor width and spacing shall be .025 ±.005 inch.
12. The quality conformance test circuitry may be segmented; however, coupons A, B, and F, when required, must be joined together. Coupons C, E, and J may be arranged to optimize board layout. All test coupons illustrated when required must appear on each panel. The number of layers must be identical to the associated board.
13. Etched letters on coupons are for identification purposes only.
14. The number of layers shown in these test coupons are for illustration purposes only. Conductor layer number 1 shall be the first layer on the component side, and all other conductor layers shall be counted consecutively downward through the laminated board to the bottom conductor layer which is the solder side.
15. For coupon F, the design is optional, provided the coupon defines the relationship of the features on each conductor layer to the board datum. For examples of coupons used for registration evaluation of type 3 boards.
16. Coupon J is only required on board surfaces to be solder mask coated.
17. Spacing between coupons may be modified to accommodate tooling holes used for automatic and/or multiple mounting microsectioning equipment.
18. The land dimension should represent the smallest land used for a component hole or via hole in the associated board.
19. The holes in the lands should be the diameter of the smallest component hole or via hole in the assocated board.
20. The inside diameter of the circular lands should be design dimension minus 2 x .002 inch. (Additional allowances may be made for the etch allowance used in the associated board.)
21. The clearance hole in the planes used for the specific layer evaluation should be design dimension minus 2 x .002 inch. All other clearances should be a minimum of design dimension plus 2 x .002 inch. (Additional allowances may be made for the etch allowances used in the associated board.)
22. The conductor dimensions should be representative of the associated board.
23. The coupon may be reduced or extended to accommodate the number of layers in a type 3 board.
24. If continuity exists between commonly number lands, the board does not meet the minimum annular ring requirement of 0.002 inch.
25. Dark areas represent metal.

FIGURE 1. Quality conformance test circuitry - Continued.



* Includes circuit and silk screen masters.

FIGURE 2. Block diagram depicting typical printed-wiring drawing relationships.

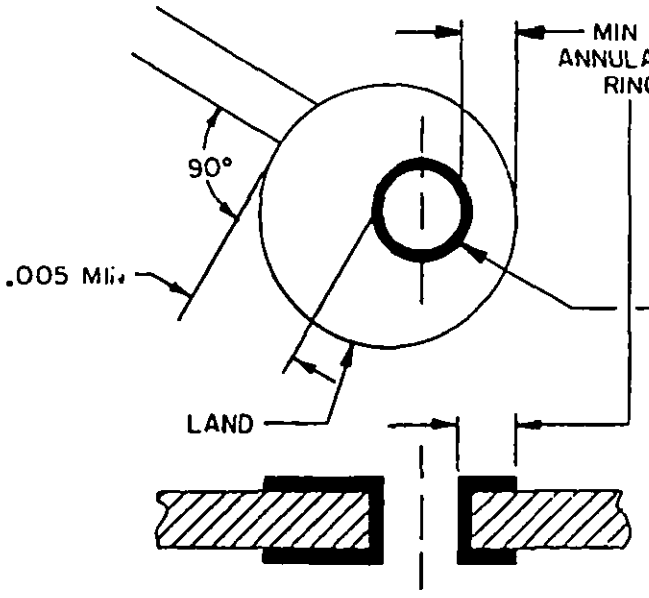


FIGURE 11. Minimum annular ring. (External) Type 2 or 3 boards.

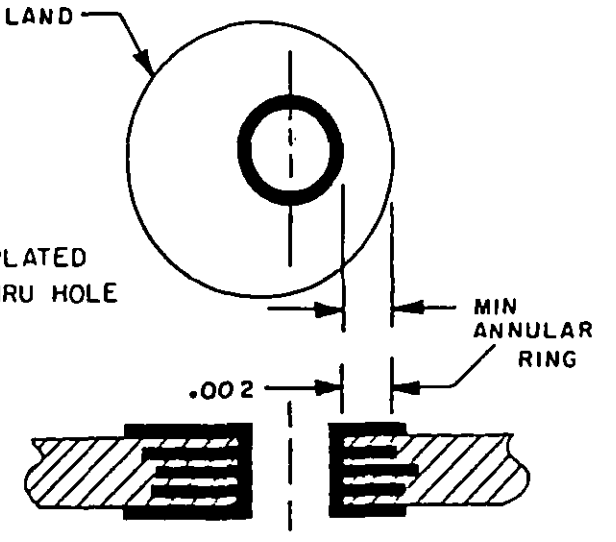
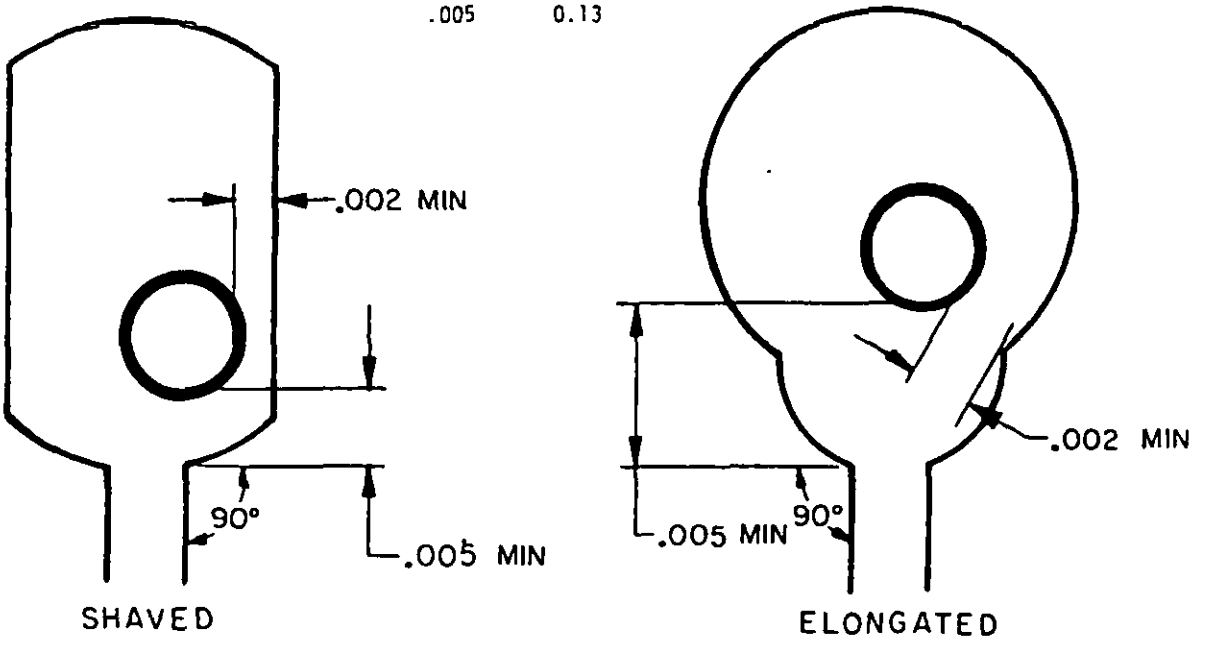


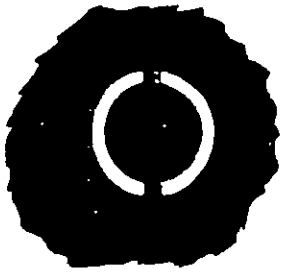
FIGURE 12. Minimum annular ring. (Internal) Type 3 boards.

Inches	mm
.002	0.05
.005	0.13



NOTES:
1. Dimensions are in inches.
2. Metric equivalents are given for general information only.
3. Radii are permissible at the junction of lands and conductors.

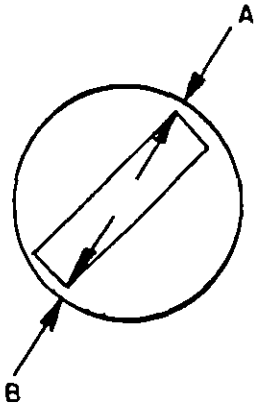
FIGURE 13. Examples of minimum annular ring dimensions. (External)



TERMINAL AREA BEFORE DRILLING

TERMINAL AREA AFTER DRILLING

FIGURE 14. Ground plane lands (typical).



	Plated-through hole	Unsupported hole
A + B =	.028 Inch (0.71 mm) MAX	.020 Inch (0.51 mm) MAX
	.006 Inch (0.15 mm) MIN	.006 Inch (0.15 mm) MIN

FIGURE 15. Hole diameter for flat lead.