INCH-POUND
MIL-STD-202-219
11 September 2017

DEPARTMENT OF DEFENSE

TEST METHOD STANDARD

METHOD 219, SHEAR STRESS

AMSC N/A

FSC 59GP

FOREWORD

1. This standard is approved for use by all Departments and Agencies of the Department of Defense.

2. Comments, suggestions, or questions on this document should be emailed to std202@dla.mil or addressed to: Commander, Defense Logistics Agency, DLA Land and Maritime, ATTN: VAT, P.O. Box 3990, Columbus, OH 43218–3990. Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at https://assist.dla.mil .

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METHOD 219
SHEAR STRESS

1. SCOPE

1.1 Purpose. The purpose of this test is to determine the integrity of materials and procedures used to attach surface mounted chip components to package headers or other substrates. This determination is based on a measure of force applied to the chip components, the type of failure resulting from this application of force (if failure occurs) and the visual appearance of the residual die attach media and substrate/header metallization.

2. APPLICABLE DOCUMENTS

This section not applicable to this standard.

3. DEFINTIONS

This section not applicable to this standard.

4. GENERAL REQUIREMENTS

4.1 Mounting. The chip component shall be mounted on a FR4 or ceramic substrate board. The test board material shall be such that it shall not be the cause of, nor contribute to, any failure of a chip component in any of the tests for which it may be used. A test board shall be prepared with metallized surface land areas of proper spacing to permit mounting of chips by soldering the terminations of the chips to the test board land areas. Unless otherwise specified, the dimensions of the test card are optional. The metallization material shall be compatible with the bonding technique to be employed and the material used on the chip termination. Epoxy adhesives, if applicable shall be limited to the terminations only. The method of chip mounting for the different termination materials shall be as follows:

a. Solderable terminations. Specimens shall be mounted on a test board by soldering the chip terminations directly to the test board metallized land areas in accordance with the following:

(1) Solder and soldering flux shall be of such a quality as to enable the chip specimens to meet all the requirements of the individual specification and shall be applied to the terminations of each chip.

(2) All specimens shall be placed across the metallized land areas of the test board with contact between the chip terminations and board land areas only. The use of adhesive to keep chips in place during mounting operation is allowable.

(3) Only ambient air cooling shall be used.

b. Palladium/silver alloy terminations. Specimens shall be attached to the substrate with a conductive adhesive. The conductive adhesive shall be cured at a minimum temperature of +150°C. The minimum curing time shall be 30 minutes.

c. Gold terminations. Specimens may be mechanically attached to the substrate with a non-conductive adhesive. The specimens shall then be electrically connected using wire bonds between the termination and the test board metalized lands. Alternately, specimens may be attached to the substrate with a conductive adhesive. The conductive adhesive shall be cured at a minimum temperature of +150°C. The minimum curing time shall be 30 minutes.

4.2 Procedure. The specified force shall be applied to the side of the component being tested (see figure 1). The applied force shall be parallel with the plane of the test board and perpendicular to the side of the component. The force shall be applied gradually as not to apply a shock to the component.

4.3 Duration of force. The duration of the applied force shall be 60 seconds ±1 second.

4.4 Magnitude of force applied.

Part Size 1/	Force (Kg)
> 1210	1.8
≥ 0603 and ≤ 1210	1.0
≥ 0201 and ≤ 603	0.5
≤ 0201	0.1

1/ The part size identifies the shape and nominal size of the chip component body. Actual dimensions shall be as specified in the individual specification.

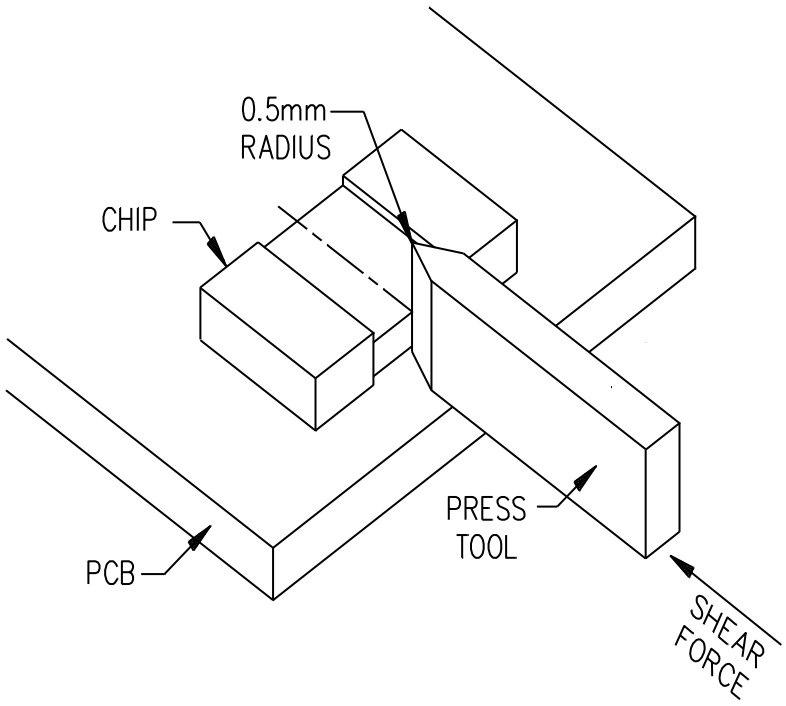

FIGURE 1. Shear Stress.

5. DETAILED REQUIREMENTS

5.1 Examination after test. The chip specimen shall be visually inspected for mechanical damage to the chip body, terminals, and body/terminal junction.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory.)

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Army - AR, AT, AV, CR4, MI, SM, TE
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NSA - NS

Preparing activity:
DLA - CC

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