MILITARY SPECIFICATION

TEST SET, ADAPTER GROUP, OF-65/ASM

This specification is approved for use by the Naval Air Systems Command, Department of the Navy, and is available for use by all Departments and Agencies of the Department of Defense.

1. SCOPE.

1.1 Scope. This specification establishes the requirements for manufacture and acceptance of the Test Set Adapter Group OF-65/ASM critical item, referred to herein as the TSAG.

2. APPLICABLE DOCUMENTS.

2.1 Government documents.

2.1.1 Specifications and standards. Unless otherwise specified, the following specifications and standards of the issue listed in that issue of the Department of Defense Index of Specifications and Standards (DoDISS) specified in the solicitation, form a part of this specification to the extent specified herein.

SPECIFICATIONS

MILITARY

MIL-T-18303	Test Procedures, Preproduction, Acceptance, and Life for Aircraft Electronic Equipment, format for.

Beneficial comments (recommendations, additions, deletions) and any pertinent data which may be of use in improving this document should be addressed to: Commanding Officer, Naval Air Engineering Center, Engineering Specifications and Standards Department (ESSD), Code 93, Lakehurst, NJ 08733, by using the self-addressed Standardization Document Improvement Proposal (DD Form 1426) appearing at the end of this document, or by letter.

FSC 7035

MIL-T-21200	Test Equipment for Use with Electronic and Electrical Equipment, General Specification for.

STANDARDS

FEDERAL

FED-STD-102	Preservation, Packaging, and Packing Levels.

MILITARY

MIL-STD-108	Definitions of and Basic Requirements for Enclosures for Electric and Electronic Equipment.
MIL-STD-109	Quality Assurance Terms and Definitions.
MIL-STD-129	Marking for Shipment and Storage.
MIL-STD-130	Identification Marking of U.S. Military Property.
MIL-STD-454	Standard General Requirements for Electronic Equipment.
MIL-STD-810	Environmental Test Methods.
MIL-STD-831	Test Reports, Preparation of.
MIL-STD-1695	Environments, Working, Minimum Standards for.
MIL-STD-45662	Calibration Systems Requirements.

2.1 Other Government documents, drawings, and publications. The following other Government documents, drawings, and publications form a part of this specification to the extent specified herein.

DOCUMENTS

Naval Air Systems Command
(Code Ident 30003)

WS-6536	Procedures and Requirements for Preparation and Soldering of Electrical Connections.

Federal Cataloging Handbook

H4	Federal Supply Code for Manufacturers, United States and Canada.

CODE OF FEDERAL REGULATIONS (CFR)

49 CRF Parts 171-178	Transportation.

(Application for copies should be addressed to the Superintendent of Documents, Government Printing Office, Washington, D.C. 20402.)

NAVAIR 16-50 BAC-2-13	Technical Manual, Computer Memory Loader-Verifier Test Set AN/ASM-607(V) (Series) AN/ASM-607A(V) (Series).

(Application for copies should be addressed to Commander (Code 3655), Naval Weapons Center, China Lake, CA 93555.)

DRAWINGS

Naval Air Systems Command
(Code Ident 30003)

1164AS616	Test Requirements Document for Circuit Card Assembly Test Card.
1164AS617	Test Requirements Specification for Circuit Card Assembly Test Card.
1164AS222	Assembly, Adapter Group, Test Set (U1).

(Copies of specifications, standards, drawings, and publications required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting officer.)

2.1.3 Order of precedence. In the event of a conflict between the text of this specification and the references cited herein, the text of this specification shall take precedence.

3. REQUIREMENTS.

3.1 Item description. The TSAG is a lightweight portable adapter kit used to convert an AN/ASM-607(V) Computer Memory Loader-Verifier (MLV) Test Set into a configuration to test another MLV. The software routines required to perform the executive functions of the MLV are stored in the programmable read only memory in the MLV. The software routines required to perform the TSAG function are stored in the tape transport unit in the MLV and loaded into the random access memory in the MLV as required.

3.1.1 Government furnished property. When specified in the contract or purchase order, the Government will furnish two MLV's and one copy of NAVAIR 16-50 BAC 2-13 (see 6.2.1).

3.1.2 First article. When specified, a sample shall be subjected to first article inspection (see 4.4 and 6.3).

3.2 Characteristics.

3.2.1 Performance.

3.2.1.1 Interface pin definition. The function and location of each signal on the output of the TSAG A1 test card shall be as specified in Appendix A.

3.2.1.2 Functional requirements. The functional requirements for the TSAG A1 test card shall be in accordance with the command address word as specified in Appendix B and on Drawings 1164AS616 and 1164AS617.

3.2.1.3 Individual acceptance tests. Individual acceptance tests shall be performed on all TSAG's in accordance with 4.6.2.

3.3 Design and construction. The design, construction, materials, and finish of the TSAG shall conform to the requirements specified herein and as specified in MIL-T-21200. If not specified in MIL-T-21200, the details of design, construction, materials, and finish shall be such as to ascertain that the TSAG will meet the requirements specified herein. Acceptance or approval of any such details shall not be construed as a guarantee of acceptance of the finished TSAG.

3.3.1 Production drawings. The TSAG shall be fabricated and assembled in accordance with the drawings, parts lists, and other documents listed on Drawing 1164AS222.

3.3.2 Interchangeability. The equipment shall meet the applicable interchangeability requirements as specified in MIL-T-21200.

3.3.3 Materials. All materials used in the construction of the TSAG shall be in accordance with MIL-STD-454, Requirement 3, Flammable Materials; Requirement 4, Fungus-Inert Materials; Requirement 15, Ferrous Alloys, Corrosion Resistance; and Requirement 16, Dissimilar Metals.

3.3.4 Standards of manufacture. The TSAG shall be manufactured, inspected, and tested under conditions and procedures as specified herein.

3.3.4.1 Special working environment. The contractor shall provide adequate facilities for the fabrication, assembly, and inspection of the item to be manufactured in accordance with this specification. Unless otherwise specified in the contract or purchase order (see 6.2.1), the minimum standards for working environments of MIL-STD-1695 shall apply to the facility where final assembly, test, and delivery of the TSAG is accomplished.

3.3.4.2 Soldering. Procedures for the preparation and soldering of electrical connections shall be in accordance with WS-6536.

3.4 Environmental requirements.

3.4.1 High temperature. The TSAG shall show no detrimental effects and shall meet the performance requirements of 3.2.1 after exposure to a high temperature environment of +55 degrees Celsius (^{o}C) for a period of 48 hours minimum (see 4.6.3.1).

3.4.2 Low temperature. The TSAG shall show no detrimental effects and shall meet the performance requirements of 3.2.1 after exposure to a low temperature environment of -40^{o}C for a period of 24 hours minimum (see 4.6.3.2).

3.4.3 Shock. The TSAG shall show no detrimental effects and shall meet the performance requirements of 3.2.1 after subjection to the shock tests of MIL-STD-810 (see 4.6.3.3).

3.4.4 Watertight. The TSAG shall show no detrimental effects and shall meet the performance requirements of 3.2.1 after exposure to the watertight tests of MIL-STD-108 (see 4.6.3.4)

3.4.5 Salt fog The TSAG shall show no detrimental effects and shall meet the performance requirements of 3.2.1 following exposure to a salt fog environment (see 4.6.3.5).

3.4.6 Dust (fine sand). The TSAG shall show no detrimental effects and shall meet the performance requirements of 3.2.1 following exposure to a dust (fine sand) environment (see 4.6.3.6).

3.5. Identification and marking. The TSAG shall be identified and marked in accordance with MIL-STD-130. Marking shall include, but not be limited to, the following:

a. The number and date of this specification.

b. NAVAIR code identification number, 30003.

c. Manufacturer's name and symbol or code identification from Federal Cataloging Handbook H4.

d. A unique serial number.

3.6 Workmanship. The TSAG, including all parts and accessories, shall be constructed and finished in a manner that will ensure compliance with all the requirements of this specification and the referenced drawings. Fabrication and assembly practices shall be in accordance with MIL-STD-454, Requirement 9.

4. QUALITY ASSURANCE PROVISIONS.

4.1 Responsibility for inspection. Unless otherwise specified in the contract or purchase order (see 6.2.1), the contractor is responsible for the performance of all inspection requirements as specified herein. Except as otherwise specified in the contract or purchase order, the contractor may use his own or any other facilities suitable for the performance of the inspection requirements specified herein, unless disapproved by the Government. The Government reserves the right to perform any of the inspections set forth in this specification where such inspections are deemed necessary to ensure that supplies and services conform to prescribed requirements.

4.2 Classification of inspections. The inspection requirements specified herein are classified as follows:

a. First article inspection (see 4.4).

b. Quality conformance inspection (see 4.5).

4.3 Test conditions.

4.3.1 Test equipment.

4.3.1.1 Calibration and maintenance. Unless otherwise specified herein, all test equipment shall be calibrated and maintained in accordance with MIL-STD-45662.

4.3.1.2 Test equipment accuracy. All test equipment used in the performance of the specified electrical tests shall have an accuracy greater than one-fifth the tolerance for the variable to be measured.

4.3.1.3 Test facility environment. Unless otherwise specified herein, tests shall be performed under the following conditions:

a. Temperature: Ambient, between +18°C and +35°C.

b. Altitude: Elevation of test facility.

c. Relative humidity: Ambient (shall be not greater than 95 percent relative.)

4.3.2 Test documentation.

4.3.2.1 Test procedures. When specified in the contract or purchase order (see 6.2.1), detailed test procedures conforming to the applicable requirements of this specification and MIL-T-18303 shall be prepared for procuring activity review prior to commencement of testing (see 6.2.2).

4.3.2.2 Test plan. When specified in the contract or purchase order (see 6.2.1), a detailed test plan shall be prepared for procuring activity review prior to commencement of testing (see 6.2.2).

4.3.2.3 Test reports. When specified in the contract or purchase order (see 6.2.1), test reports shall be prepared in accordance with MIL-STD-831 (see 6.2.2). The reports shall contain the quantitative results of each examination, test, or measurement specified.

4.3.2.4 Certification. The contractor shall have available for the Government representative, written certification accompanied by objective quality evidence (as defined in MIL-STD-109), that the components used as a part of the TSAG meet the applicable requirements.

4.4 First article inspection. When specified in the contract or purchase order, the contractor shall furnish a first article of two TSAG's to the testing activity designated in the contract or purchase order for first article inspection and approval (see 6.3). First article approval is valid only on the contract under which it is granted, unless specifically extended by the procuring activity to other contracts. The first article shall be manufactured using the same methods, materials, processes, and procedures proposed for production. Any production prior to approval of the first article shall be at the risk of the contractor.

4.4.1 First article inspection sequence. The first article sample of two TSAG's shall be subjected to the inspections of Table I in the sequence shown.

4.4.2 First article acceptance and rejection criteria. Failure of any TSAG to pass any of the first article inspections specified herein shall cause rejection of the first article sample.

TABLE I. First article inspection.

Inspection	Requirement paragraph	Method paragraph
Visual and mechanical	3.3, 3.5, 3.6	4.6.1, 4.6.4, 4.6.5
Performance tests	3.2.1.1, 3.2.1.2	4.6.1
High temperature	3.4.1	4.6.3.1
Low temperature	3.4.2	4.6.3.2
Shock	3.4.3	4.6.3.3
Watertight	3.4.4	4.6.3.4
Salt fog	3.4.5	4.6.3.5
Dust (fine sand)	3.4.6	4.6.3.6
Performance tests	3.2.1.1, 3.2.1.2	4.6.1
Individual acceptance tests	3.2.1.3	4.6.2

4.4.3 Disposition of first article sample. Disposition of first article samples shall be in accordance with the contract or purchase order (see 6.2.1).

4.5 Quality conformance inspections. All TSAG's offered for acceptance shall be subjected to the quality conformance inspections and in the sequence specified in Table II. Any TSAG that fails to meet the requirements of Table II shall be rejected.

TABLE II. Quality conformance inspection.

Inspection	Requirement paragraph	Method paragraph
Visual and mechanical	3.3, 3.5, 3.6	4.6.1, 4.6.4, 4.6.5
Performance tests	3.2.1.1, 3.2.1.2	4.6.1
Individual acceptance tests	3.2.1.3	4.6.2

4.6 Methods of inspection.

4.6.1 Performance tests. The TSAG A1 test card shall be tested for conformance to 3.2.1.1 and 3.2.1.2.

4.6.2 Individual acceptance test. The following individual acceptance tests shall be performed in accordance with NAVAIR 16-50 BAC 2-13 (see 3.2.1.3):

a. TSAG circuit card test.

b. MLV-to-MLV test.

4.6.3 Environmental tests. The environmental tests specified in 4.6.3.1 through 4.6.3.6 shall be performed with the TSAG components secured in the transit case. The case cover shall be installed and latched.

4.6.3.1 High temperature. The TSAG shall be subjected to the high temperature test of MIL-STD-810, Method 501.1, Procedure I, except that the high temperature shall be +55°C, and Steps 4 and 5 shall not be performed. Following exposure, the TSAG shall be subjected to and pass the examinations and tests of 4.5 (see 3.4.1).

4.6.3.2 Low temperature. The TSAG shall be subjected to the low temperature test of MIL-STD-810, Method 502.1, Procedure I, except that the low temperature shall be -40°C, and Steps 4 and 5 shall not be performed. Following exposure, the TSAG shall be subjected to and pass the examinations and tests of 4.5 (see 3.4.2).

4.6.3.3 Shock. The TSAG shall be subjected to the shock test of MIL-STD-810, Method 516.2, Procedure II, except that the total number of drops shall be 14. Following exposure, the TSAG shall be subjected to and pass the examinations and tests of 4.5 (see 3.4.3).

4.6.3.4 Watertight. The TSAG shall be subjected to the watertight test of MIL-STD-108. Following exposure, the TSAG shall be subjected to and pass the examinations and tests of 4.5 (see 3.4.4).

4.6.3.5 Salt fog. The TSAG shall be subjected to the salt fog test of MIL-STD-810, Method 509.1, Procedure I, using a 20-percent salt solution. Following exposure, the TSAG shall be subjected to and pass the examinations and tests of 4.5 (see 3.4.5).

4.6.3.6 Dust (fine sand). The TSAG shall be subjected to the dust (fine sand) test of MIL-STD-810, Method 510.1, Procedure I. Following exposure, the TSAG shall be subjected to and pass the examinations and tests of 4.5 (see 3.4.6).

4.6.4 Visual examination. The TSAG shall be examined to verify that marking and workmanship meet the requirements of 3.3, 3.5, and 3.6.

4.6.5 Packaging, packing, and marking. Examination shall be made to ensure that packaging, packing, and marking conform to the requirements of Section 5.

5. PACKAGING.

5.1 Preservation and packaging. Preservation and packaging shall be Level C in accordance with FED-STD-102.

5.1.1 Level C. Unless otherwise specified in the conteact or purchase order (see 6.2.1), the TSAG shall be preserved and packaged in a manner to prevent deterioration and damage during shipment from the supply source to the first receiving activity in accordance with 49 CFR Parts 171-178.

5.2 Packing.

5.2.1 Level C. Unless otherwise specified in the contract or purchase order (see 6.2.1), the TSAG shall be packed in a manner which will afford adequate protection against damage during direct shipment from the supply source to the first receiving activity in accordance with 49 CFR Parts 171-178.

5.3 Marking. In addition to any special markings specified in the contract or purchase order, the unit package, intermediate packages, and shipping containers shall be marked in accordance with MIL-STD-129 (see 6.2.1).

6. NOTES.

6.1 Intended use. The TSAG is intended for use in converting an MLV into a diagnostic MLV which will be used to test another MLV.

6.2 Ordering data.

6.2.1 Acquisition requirements. Acquisition documents should specify the following:

a. Number, title, and date of this specification.

b. Government furnished property (see 3.1.1).

c. First article inspections (see 3.1.2 and 4.4).

d. Special working environment, if other than specified in 3.3.4.1.

e. Responsibility for inspection and inspection facilities, if other than specified in 4.1.

f. Detailed test procedures, if required (see 4.3.2.1).

g. Detailed test plan, if required (see 4.3.2.2).

h. Test reports, if required (see 4.3.2.3).

i. Disposition of first article (see 4.4.3).

j. Preservation and packaging, if other than specified in 5.1.

k. Packing, if other than specified in 5.2.

l. Marking, if other than specified in 5.3.

6.2.2 Data requirements. When this specification is used in an acquisition which incorporates a DD Form 1423, Contract Data Requirements List (CDRL), the data requirements identified below shall be developed as specified by an approved Data Item Description (DD Form 1664) and delivered in accordance with the approved CDRL incorporated into the contract. When the provisions of DAR 7-104.9(n) (2) are invoked and the DD Form 1423 is not used, the data specified below shall be delivered by the contractor in accordance with the contract or purchase order requirements. Deliverable data required by this specification is cited in the following paragraphs:

Paragraph no.	Data requirement title	Applicable DID no.	Option
4.3.2.1	Test Procedures	UDI-T-21347	---
4.3.2.2	Test Plan	DI-T-5204	---
4.3.2.3	Test Reports	DI-T-2072	---

(Data item descriptions related to this specification, and identified in Section 6 will be approved and listed as such in DOD 5000.19L., Vol. II, AMSDL. Copies of data item descriptions required by the contractor in connection with specific acquisition functions should be obtained from the Naval Publications and Forms Center or as directed by the contracting officer.)

6.3 First article. When a first article inspection is required, the item will be tested and should be a first article sample as specified in 4.4. The first article should consist of two units. The contracting officer should include specific instructions in acquisition documents regarding arrangements for examination, test approval of the document's first article.

Preparing activity:
Navy (AS)
(Project No. 7035-N007)

APPENDIX A

PIN DEFINITION LIST

10 SCOPE.

10.1 Scope. This appendix identifies the function and location of each signal on the output of the Test Set Adapter Group (TSAG) test card circuit card assembly (A1). This appendix is a mandatory part of the specification. The information contained herein is intended for compliance.

20 APPLICABLE DOCUMENTS.

This section is not applicable to this document.

TEST CARD CONNECTOR AND PIN NUMBER	SIGNAL NAME	INPUT/ OUTPUT	SOURCE/ DESTINATION	SOURCE/ DESTINATION CONNECTOR/ PIN NUMBER	FUNCTION	LOGIC LEVELS
P1-3	DBØ (LSB)	Input	CPU - S	P1-3	DBØ-DB7 are the output data lines from the CPU board. Data is valid whenever the CPU is performing an output operation or a memory write operation and the signal /WR is a logic "0". For an output operation this data should be latched on the leading edge of /CAWENB True data.	"1" = 2.4V-5.0V "0" = 0.0V-0.4V
P1-4	DB1	Input	CPU - S	P1-4		
P1-5	DB2	Input	CPU - S	P1-5		
P1 6	DB3	Input	CPU - S	P1-6		
P1-7	DB4	Input	CPU - S	P1-7		
P1-8	DB5	Input	CPU - S	P1-8		
P1-9	DB6	Input	CPU - S	P1-9		
P-10	DB7 (MSB)	Input	CPU - S	P1-10		
P1-14	/WR	Input	CPU - S	P1-14	This is the write signal from the CPU Board When a logic "0", DBØ-DB7 are stable for a memory write or an output operation	"1" = 2.4V-5.0V "0" = 0.0V-0.4V
P2-44	/CEØ	Input	Memory - S	P2-44	/CEØ and /CE1 are caw enable signals generated on the memory board. /CEØ will be a logic "0" for the following condition $/CE\emptyset = \overline{(OUT \cdot WR) + INP \cdot \overline{BA3} \cdot \overline{BA4}}$ /CE1 will be a logic "0" for the following condition $/CE1 = \overline{(OUT \cdot WR) + INP \cdot \overline{BA3} \cdot \overline{BA4}}$	"1" = 2.4V-5.0V "0" = 0.0V-0.4V
P2-45	/CE1	Input	Memory - S	P2-45		

TEST CARD CONNECTOR AND PIN NUMBER	SIGNAL NAME	INPUT/ OUTPUT	SOURCE/ DESTINATION	SOURCE/ DESTINATION CONNECTOR/ PIN NUMBER	FUNCTION	LOGIC LEVELS
					Both of the signals will go to a logic "0" for an output or an input operation if the BA3 and BA4 bits are the right address value. An input operation should use these signals to gate input data onto the DI bus. An output operation should use the leading edge of these signals to latch up output data from the DB bus	
P2 36	DIØ (LSB)	Output	CPU - D	P2-36	These are input data lines for external data into the CPU. External data is enabled onto the DI lines with the signals /CEØ - /CE3. Data is put on these lines whenever a memory read or an input operation is being performed. True data.	"1" = 2.4V-5.0V "0" = 0V-0.4V
P2-37	DI1	Output	CPU - D	P2-37		
P2-38	DI2	Output	CPU - D	P2-38		
P2-39	DI3	Output	CPU - D	P2-39		
P2-40	DI4	Output	CPU - D	P2-40		
P2-41	DI5	Output	CPU - D	P2-41		
P2-42	DI6	Output	CPU - D	P2-42		
P2-43	DI7 (MSB)	Output	CPU - D	P2-43		
P2-34	2MHZ	Input	CPU - S	P2-34	2MHZ Frequency, TTL level system clock. Same as Ø2 from the CPU board.	"1" = 2.4V-5.0V "0" = 0V-0.4V

TEST CARD CONNECTOR AND PIN NUMBER	SIGNAL NAME	INPUT/ OUTPUT	SOURCE/ DESTINATION	SOURCE/ DESTINATION CONNECTOR/ PIN NUMBER	FUNCTION	LOGIC LEVELS
P2-11	BAØ (LSB)	Input	CPU - S	P2-11	Address lines from the CPU board On the I/O card slot, they are used to decode the command address works (CAWS) in conjunction with the signals /CEØ and /CE1 The generated CAWS are used to either latch output data, to gate input data, or to generate command pulses. True data.	"1" = 2.4V-5.0V "0" = 0V-0.4V
P2-12	BA1	Input	CPU - S	P2-12		
P2-13	BA2	Input	CPU - S	P2-13		
P2-14	BA3	Input	CPU - S	P2-14		
P2-15	BA4	Input	CPU - S	P2-15		
P2-16	BA5	Input	CPU - S	P2-16		
P2-17	BA6	Input	CPU - S	P2-17		
P2-18	BA7 (MSB)	Input	CPU - S	P2-18		
P1-15	MCREADY	Output	CPU - D	P1-15	MCREADY is the ready input to the CPU board It is an open-collector driven signal To put the 8080 microporcessor into a wait state, this signal should be pulled to a logic "0" on the rising edge of the Ø2 signal. To release the 8080 microprocessor from a wait state, this signal should be put to a logic "1" on the rising edge of the Ø2 signal.	"1" = 2.4V-5.0V "0" = 0.0V-0.4V
P2-8	OUT	Input	CPU - S	P2-8	The OUT signal from the CPU board is a status bit sent out in the 8080 status word. When it is a logic "1" it indicates that the address bus	"1" = 2 4V-5.0V "0" = 0.0V-0.4V

TEST CARD CONNECTOR AND PIN NUMBER	SIGNAL NAME	INPUT/ OUTPUT	SOURCE/ DESTINATION	SOURCE/ DESTINATION CONNECTOR/ PIN NUMBER	FUNCTION	LOGIC LEVELS
					contains the address of an output device and the DB bus will contain the output data when /WR is a logic "0"	
P1-29	/INTR3	Output	CPU - D	P1-29	/INTR3 is an interrupt request to the interrupt circuitry on the CPU board. When it goes to a logic "0", the interrupt request is active. This signal should be latched and held until the signal /INTA1 releases the request /INTR3 is 3rd in interrupt priority	"1" = 2.4V-5.0V "0" = 0.0V-0.4V
P2-27	/INTA1	Input	CPU - S	P2-27	/INTA1 is an interrupt acknowledge signal generated by the CPU board at the end of an interrupt cycle to clear an interrupt request at its origin. The logic "0" level should be used to clear the latch where the interrupt request is stored.	"1" = 2.4V-5.0V "0" = 0.0V-0.4V

TEST CARD CONNECTOR AND PIN NUMBER	SIGNAL NAME	INPUT/ OUTPUT	SOURCE/ DESTINATION	SOURCE/ DESTINATION CONNECTOR/ PIN NUMBER	FUNCTION	LOGIC LEVELS
P1-46	-12Vdc	Input	Heatsink Assembly-S	NA	-12Vdc	NA
P1-45	+12Vdc	Input	Heatsink Assembly-S	NA	+12Vdc	NA
P1-1	+5V	Input	+5V P S Assembly-S	NA	+5Vdc	NA
P1-2	+5V	Input	+5V P S. Assembly-S	NA	+5Vdc	NA
P1-34	+5V	Input	+5V P S Assembly-S	NA	+5Vdc	NA
P1-35	+5V	Input	+5V P S. Assembly-S	NA	+5Vdc	NA
P2-32	GND	Input	System Ground - S	NA	Ground	NA
P2-33	GND	Input	System Ground - S	NA	Ground	NA
P2-65	GND	Input	System Ground - S	NA	Ground	NA
P2-66	GND	Input	System Ground - S	NA	Ground	NA

TEST CARD CONNECTOR AND PIN NUMBER	SIGNAL NAME	INPUT/ OUTPUT	SOURCE/ DESTINATION	SOURCE/ DESTINATION CONNECTOR/ PIN NUMBER	FUNCTION	LOGIC LEVELS
P1-11	/TMEMENB	INPUT	MLV under test, CPU board - S	P1-12	/TMEMENB is the /MEMENB signal generated on the CPU board of the MLV under test. It is a logic "0" whenever the MLV under test is performing a memory operation from 4000_{16} - $5FFF_{16}$. At all other times it is a logic "1"	"1" = 2.4V-5.0V "0" = 0.0V-0.4V
P1-12	/TCAWENB	INPUT	MLV under test, CPU board-S	P1-13	/TCAWENB is the /CAWENB signal generated on the CPU board of the MLV under test. It is a logic "0" whenever the MLV under test is performing an input or an output operation. It is a logic "0" whenever the INP bit of the status word is a logic "1", or whenever the OUT bit of the status word is a logic "1" and the /WR signal is a logic "0" on the CPU board in the MLV under test.	"1" = 2.4V-5.0V "0" = 0.0V-0.4V
P1-13	/TWR	INPUT	MLV under test, CPU board-S	P1-14	/TWR is the /WR signal generated on the CPU board of the MLV under test. It is a logic "0" whenever the 8080 microprocessor is sending out stable data on the DB lines for either a memory write operation or an output operation.	"1" = 2.4V-5.0V "0" = 0.0V-0.4V

TEST CARD CONNECTOR AND PIN NUMBER	SIGNAL NAME	INPUT/ OUTPUT	SOURCE/ DESTINATION	SOURCE/ DESTINATION CONNECTOR/ PIN NUMBER	FUNCTION	LOGIC LEVELS
P1-16 P1-17 P1-18 P1-19	TICHANA TICHANB TICHANC TICHAND	Input or Output	MLV under test, Memory board-S, Tape Unit - D	MLV under test, Memory board P2-3,4,5,6 Tape Unit J1-T,X,W,V	TICHANA-TICHAND are the ICHANA-ICHAND lines from the tape unit in the MLV under test. These are the data in lines to the tape unit. If TDISABLE is set to a logic "1", TICHANA-TICHAND will be the I channel data sent from the tape interface on the memory board of the MLV under test to the tape unit of the MLV under test. If TDISABLE is set to a logic "0", the test card in the diagnostic MLV will be able to send data on these lines to the tape unit in the MLV under test.	"1" = 2.4V-5.0V "0" = 0.0V-0.4V
P1-28	TICLOCK	Input or Output	MLV under test, Memory board-S, tape unit - D	MLV under test, Memory board P1-52, tape unit J1-R	TICLOCK is the ICLOCK line from the tape interface on the memory board in the MLV under test to the tape unit in the MLV under test It is a symmetrical 10KHZ waveform that is used in conjunction with sending data to the tape unit 25 µsec prior to the falling edge of TICLOCK the data on TICHANA-TICHAND must be stable and remain stable until 25 µsec after the falling edge of TICLOCK. If TDISABLE is a logic "1", TICLOCK will be the wave form sent from the tape interface on the memory board of the MLV under test to the tape unit in the MLV under test If TDISABLE is a logic "0", the test card in the diagnostic MLV will be able to send a TICLOCK signal to the tape unit in the MLV under test.	"1" = 2.4V-5.0V "0" = 0.0V-0.4V

TEST CARD CONNECTOR AND PIN NUMBER	SIGNAL NAME	INPUT/ OUTPUT	SOURCE/ DESTINATION	SOURCE/ DESTINATION CONNECTOR/ PIN NUMBER	FUNCTION	LOGIC LEVELS
P2-26	TDISABLE	Output	MLV under test, Memory board - D	MLV under test, Memory board, P2-2	TDISABLE is the DISABLE signal sent to the tape interface on the memory board in the MLV under test. If it is a logic "0", all of the tape interface outputs on the memory board in the MLV under test will go to a high impedance output state. If it is a logic "1" all of the tape interface outputs on that board will be enabled. The outputs affected are as follows: TICHANA TICHANB TICHANC TICHAND TICLOCK TCNBL TCWRITE TCMOVE TCSPEED TCDIR	"1" = 2.4V-5.0V "0" = 0.0V-0.4V
P2-62	TCNBL	Input/ Output	MLV under test, Memory card-S, tape unit-D	MLV under test, Memory card P1-53, tape unit 21-E	TCNBL is the CNBL signal from the tape interface on the Memory board in the MLV under test to the tape unit in the MLV under test. If it is a logic "0", it will disable the tape unit. If it is a logic "1", it will enable the tape unit. If TDISABLE is set to a logic "1", TCNBL will be the signal sent from the tape interface on the memory board in the MLV under test to the tape unit in the MLV under test. If TDISABLE is a logic "0", the	"1" = 2.4V-5.0V "0" = 0.0V-0.4V

TEST CARD CONECTOR AND PIN NUMBER	SIGNAL NAME	INPUT/ OUTPUT	SOURCE/ DESTINATION	SOURCE/ DESTINATION CONNECTOR/ PIN NUMBER	FUNCTION	LOGIC LEVELS
					test card in the diagnostic MLV will be able to send the TCNBL signal to the tape unit in the MLV under test.	
P1-21	TCWRITE	Input/ Output	MLV under test, Memory Board - S, tape unit - D	MLV under test, Memory board P2-1, tape unit J1-M	TCWRITE is the CWRITE signal sent from the tape interface on the memory board in the MLV under test to the tape unit in the MLV under test. If it is a logic "0", it will set the tape unit into a read mode. If it is a logic "1", it will set the tape unit into a write mode. If TDISABLE is set to a logic "1", TCWRITE will be the signal sent from the tape interface on the memory board in the MLV under test to the tape unit in the MLV under test. If TDISABLE is set to a logic "0", the test card in the diagnostic MLV will be able to send the TCWRITE signal to the tape unit in the MLV under test.	"1" = 2.4V-5.0V "0" = 0.0V-0.4V
P1-20	TCMOVE	Input/ Output	MLV under test, Memory Board - S, Tape Unit - D	MLV under test, Memory P1-56 Board, Tape J1-P Unit	TCMOVE is the CMOVE signal sent from the tape interface on the memory board in the MLV under test to the tape unit in the MLV under test. If it is a logic "0", it will stop the motion of the tape. If it is a logic "1" it will start the tape moving. If TDISABLE is set to a logic "1" TCMOVE will be the signal sent from the tape interface on the memory board	"1" = 2.4V-5.0V "0" = 0.0V-0.4V

TEST CARD CONNECTOR AND PIN NUMBER	SIGNAL NAME	INPUT/ OUTPUT	SOURCE/ DESTINATION	SOURCE/ DESTINATION CONNECTOR/ PIN NUMBER	FUNCTION	LOGIC LEVELS
					In the MLV under test to the tape unit in the MLV under test If TDISABLE is set to a logic "0", the test card in the diagnostic MLV will be able to send the TCMOVE signal to the tape unit in the MLV under test	
P2-63	TCDIR	Input/ Output	MLV under test, Memory Board - S, Tape Unit - D	MLV under test, Memory Board P1-54, Tape Unit J1-E	TCDIR is the CDIR signal sent from the tape interface on the memory board in the MLV under test to the tape unit in the MLV under test If it is a logic "0" it will cause tape unit to run in the reverse direction If it is a logic "1", it will cause the tape unit to run in the forward direction. This signal must be preset to a value before TCMOVE is set to a logic "1" if TDISABLE is set to a logic "1", TCDIR will be the signal sent from the tape interface on the memory board in the MLV under test to the tape unit in the MLV under test. If TDISABLE is set to a logic "0", the test card in the diagnostic MLV will be able to send the TCDIR signal to the tape unit in the MLV under test.	"1" = 2.4V-5.0V "0" = 0.0V-0.4V
P2-64	TCSPEED	Input/ Output	MLV under test, Memory Board - S, Tape Unit D	MLV under test, Memory Board P1-55, Tape Unit J1-D	TCSPEED is the CSPEED signal sent from the tape interface on the memory board in the MLV under test to the tape unit in the MLV under test. If it is a	"1" = 2.4V-5.0V "0" = 0.0V-0.4V

TEST CARD CONNECTOR AND PIN NUMBER	SIGNAL NAME	INPUT/ OUTPUT	SOURCE/ DESTINATION	SOURCE/ DESTINATION CONNECTOR/ PIN NUMBER	FUNCTION	LOGIC LEVELS
					logic "0" it will set the tape unit into a low speed mode. If it is a logic "1", it will set the tape unit into a high speed mode. If TDISABLE is set to a logic "1", TCSPEED will be the signal sent from the tape interface on the memory board in the MLV under test to the tape unit in the MLV under test. If TDISABLE's set for a logic "0", the test card in the diagnostic MLV will be able to send the TCSPEED signal to the tape unit in the MLV under test	
P2-47	TSBOT	Input	MLV under test, Tape Unit - S	MLV under test, Tape Unit J1-C	TSBOT is the SBOT signal sent from the tape unit in the MLV under test to the tape interface on the memory board in the MLV under test It is a logic "1" when the tape unit is at the beginning of tape position and it is a logic "0" for all other tape positions.	"1" = 2.4V-5.0V "0" = 0.0V-0.4V
P2-48	TSEOT	Input	MLV under test, Tape Unit - S	MLV under test, Tape Unit J1-F	TSEOT is the SEOT signal sent from the tape unit in the MLV under test to the tape interface on the memory board in the MLV under test It is a logic "1" when the tape unit is at the end of tape position. It is a logic "0" for all other tape positions.	"1" = 2.4V-5.0V "0" = 0.0V-0.4V

TEST CARD CONNECTOR AND PIN NUMBER	SIGNAL NAME	INPUT/ OUTPUT	SOURCE/ DESTINATION	SOURCE/ DESTINATION CONNECTOR/ PIN NUMBER	FUNCTION	LOGIC LEVELS
P2-49	TSSTOP	Input	MLV under test, Tape Unit - S	MLV under test, Tape Unit J1-K	TSSTOP is the SSTOP signal sent from the tape unit in the MLV under test to the tape interface on the memory board in the MLV under test It is a logic "1" whenever the tape speed of the tape unit is less than 10% of full speed It is a logic "0" for all other speeds	"1" = 2 4V-5.0V "0" = 0.0V-0.4V
P2-50	TSRUN	Input	MLV under test, Tape Unit - S	MLV under test, Tape Unit J1-L	TSRUN is the SRUN signal sent from the tape unit in the MLV under test to the tape interface on the memory board in the MLV under test It is a logic "1" whenever the tape speed of the tape unit is greater than 90% of full speed It is a logic "0" for all other speeds	"1" = 2.4V-5.0V "0" = 0 0V-0.4V
P2-51	TSNBL	Input	MLV under test, Tape Unit - S	MLV under test, Tape Unit J1-M	TSNBL is the SNBL signal sent from the tape unit in the MLV under test to the tape interface on the memory board in the MLV under test It is a logic "1" whenever a valid CNBL sequence has been sent to the tape unit, the power in to the tape unit is greater than 100 volts, and the tape interlock circuitry is functional.	"1" = 2.4V-5.0V "0" = 0.0V-0.4V

TEST CARD CONNECTOR AND PIN NUMBER	SIGNAL NAME	INPUT/ OUTPUT	SOURCE/ DESTINATION	SOURCE/ DESTINATION CONNECTOR/ PIN NUMBER	FUNCTION	LOGIC LEVELS
P2-52	TBSBLOCK	Input	MLV under test, Tape Unit - S	MLV under test, Tape Unit - J1-D	TBSBLOCK is the BSBLOCK signal sent from the tape unit in the MLV under test to the tape interface on the memory board in the MLV under test. It is a logic "1" whenever the tape unit is reading valid data off of the tape. It is a logic "0" for interrecord gaps, blank tape, for high speed operation, or for rewind operation	"1" = 2.4V-5.0V "0" = 0.0V-0.4V
P2-58	TBOCHANA	Input	MLV under test, Memory board - S	P1-58	TBOCHANA-TBOCHAND are the OCHANA-OCHAND lines from the tape unit in the MLV under test. These are the data out lines from the tape unit to the tape interface in the memory board in the MLV under test The signal TOCLOCK must be used to synchronize external devices to the output data rate of the tape unit	"1" = 2.4V-5.0V "0" = 0.0V-0.4V
P2-59	TBOCHANB	Input	"	P1-59		
P2-60	TBOCHANC	Input	"	P1-60		
P2-61	TBOCHAND	Input	"	P1-61		
P1-40	TOCLOCK	Input	MLV under test, Memory board - S	P1-62	TOCLOCK is the OCLOCK signal from the tape unit in the MLV under test to the tape interface in the memory board in the MLV under test It is a non-symmetrical timing signal with a PRT of 100±25 µsec and a logic "1" pulse width of 1-3 sec It is used to sychronize external devices to the output data rate of the tape unit. On the rising edge, the data TBOCHANA-TBOCHAND will change, and should be latched on the falling edge of TOCLOCK.	"1" = 2.4V-5.0V "0" = 0.0V-0.4V

TEST CARD CONNECTOR AND PIN NUMBER	SIGNAL NAME	INPUT/ OUTPUT	SOURCE/ DESTINATION	SOURCE/ DESTINATION CONNECTOR/ PIN NUMBER	FUNCTION	LOGIC LEVELS
P1-30	TDB0	Input	MLV under test CPU Board	P1-3	TDB0-TDB7 are the D30-D37 signals from the CPU board of the MLV under test. Data on these lines are valid whenever that CPU is performing an output operation or a memory write operation and the signal /TWR is a logic "0". The outputs are also active whenever /TDBENB is a logic "0" or whenever /TDBDIS is a logic "0".	"1" = 2.4V-5.0V "0" = 0.0V-0.4V
P1-31	TDB1	Input	MLV under test, CPU Board	P1-4		
P1-32	TDB2	Input	MLV under test, CPU Board	P1-5		
P1-33	TDB3	Input	MLV under test, CPU Board	P1-6		
P1-36	TDB4	Input	MLV under test, CPU Board	P1-7		
P1-37	TDB5	Input	MLV under test, CPU Board	P1-8		
P1-38	TDB6	Input	MLV under test, CPU Board	P1-9		
P1-39	TDB7	Input	MLV under test, CPU Board	P1-10		

TEST CARD CONNECTOR AND PIN NUMBER	SIGNAL NAME	INPUT/ OUTPUT	SOURCE/ DESTINATION	SOURCE/ DESTINATION CONNECTOR/ PIN NUMBER	FUNCTION	LOGIC LEVELS
P1-41	TDIØ	Input	MLV under test, CPU Board - S	P2-36	TDIØ-TDI7 are the DIØ-DI7 signal lines from the CPU board in the MLV under test. These are input data lines for external data into the CPU. External data is enabled onto these lines with the signals CEØ, CE1, CE2, and CE3. Data is enabled onto these lines whenever a memory read or an input operation is being performed.	"1" = 2.4V-5.0V "0" = 0.0V-0.4V
P1-42	TDI1	Input	"	P2-37		
P1-43	TDI2	Input	"	P2-38		
P1-44	TDI3	Input	"	P2-39		
P1-47	TDI4	Input	"	P2-40		
P1-48	TDI5	Input	"	P2-41		
P1-49	TDI6	Input	"	P2-42		
P1-50	TDI7	Input	"	P2-43		

TEST CARD CONNECTOR AND PIN NUMBER	SIGNAL NAME *	INPUT/ OUTPUT	SOURCE/ DESTINATION	SOURCE/ DESTINATION CONNECTOR/ PIN NUMBER	FUNCTION	LOGIC LEVELS
P1-51	TBAØ	Input/ Output	MLV under test, CPU 5 Board Memory - D Board	P2-11	TBAØ-TBA15 are the BAØ-BA15 signal lines from the CPU board in the MLV under test. These lines provide the address information that specify an address in a memory operation or specify an I/O device in an I/O operation.	"1" = 2.4V-5.0V "0" = 0.0V-0.4V
P1-52	TBA1	"	"	P2-12		
P1-53	TBA2	"	"	P2-13		
P1-54	TBA3	"	"	P2-14		
P1-55	TBA4	"	"	P2-15		
P1-56	TBA5	"	"	P2-16		
P1-57	TBA6	"	"	P2-17		
P1-58	TBA7	"	"	P2-18		
P1-59	TBA8	"	"	P2-19		
P1-60	TBA9	"	"	P2-20		
P1-61	TBA10	"	"	P2-21		
P1-62	TBA11	"	"	P2-22		
P1-63	TBA12	"	"	P2-23		
P1-64	TBA13	"	"	P2-24		
P1-65	TBA14	"	"	P2-25		
P1-66	TBA15	"	"	P2-26		

TEST CARD CONNECTOR AND PIN NUMBER	SIGNAL NAME	INPUT/ OUTPUT	SOURCE/ DESTINATION	SOURCE/ DESTINATION CONNECTOR/ PIN NUMBER	FUNCTION	LOGIC LEVELS
P2-2	TDMADØ	Output	MLV under Test, CPU Board - D	P2-57	TDMADØ-TDMAD7 are the DMADØ-DMAD7 signal lines on the CPU board in the MLV under test. This data is gated onto the DI bus whenever /TMEMDIS is a logic "0" or the MLV under test is executing an IN 56, or the internal signal IMDIS is a logic "1". This data is gated onto the DB bus whenever the signal /TDBDIS is a logic "0", or whenever the MLV under test is in a HALT state and/TDBENB is a logic "1".	"1" = 2.4V-5.0V "0" = 0.0V-0.4V
P2-3	TDMAD1	"	"	P2-58		
P2-4	TDMAD2	"	"	P2-59		
P2-5	TDMAD3	"	"	P2-60		
P2-6	TDMAD4	"	"	P2-61		
P2-7	TDMAD5	"	"	P2-62		
P2-9	TDMAD6	"	"	P2-63		
P2-10	TDMAD7	"	"	P2-64		
P1-22	/TRESIN	Output	MLV under test, CPU Board - D	P1-18	/TRESIN is the /RESIN pulse that goes to the CPU board on the MLV under test. When it is a logic "0" the 8080 program counter and the interrupt request signals are cleared and the 8080 INTE and HLDA signals are reset. When it is a logic "1" it starts the 8080 operating. Must be an open collector signal.	"1" = 2.4V-5.0V "0" = 0.0V-0.4V

TEST CARD CONNECTOR AND PIN NUMBER	SIGNAL NAME	INPUT/ OUTPUT	SOURCE/ DESTINATION	SOURCE/ DESTINATION CONNECTOR/ PIN NUMBER	FUNCTION	LOGIC LEVELS
P1-25	/TWAIT	Input	MLV under test, CPU Board - S	P2-45	/TWAIT is the /WAIT signal from the CPU board in the MLV under test When it is a logic "0", it indicates that the 8080 microprocessor is in a wait state	"1" = 2.4V-5.0V "0" = 0.0V-0.4V
P1-24	/TPWRGOOD	Input	MLV under test, CPU Board - S	P2-29	/TPWRGOOD is the /PWRGOOD signal from the CPU board in the MLV under test When it is a logic "1", it indicates that the power in the MLV under test is about to fail or has failed	"1" = 2.4V-5.0V "0" = 0.0V-0.4V
P1-26	ID1	Output	NA	NA	Identification pin 1 of the I/O board. This pin will identify that the board is part of the MLV series of boards This pin will have a 8.25Kohm resistance to ground	NA
P1-27	ID2	Output	NA	NA	Identification pin 2 of the I/O board. This pin will identify the board as being the test card assembly of the test set adapter group. This pin will have a 2 61Kohm resistance to ground.	NA

TEST CARD CONNECTOR AND PIN NUMBER	SIGNAL NAME	INPUT/ OUTPUT	SOURCE/ DESTINATION	SOURCE/ DESTINATION CONNECTOR/ PIN NUMBER	FUNCTION	LOGIC LEVELS
P1-25	TSYNC	Input	MLV under test, CPU Board - S	P2-48	TSYNC is the sync signal output from the CPU board in the MLV under test. This is a synchronizing signal from the 8080 microprocessor. The logic "1" value identifies the beginning of every machine cycle. It is triggered by the low to high transition of Ø2.	"1" = 2.4V-5.0V "0" = 0.0V-0.4V
P2-19	/TØ2	Input	MLV under test, CPU Board - S	P2-47	/TØ2 is the /Ø2 signal output from the CPU board in the MLV under test This is a TTL level 2MHZ system clock.	"1" = 2.4V-5.0V "0" = 0.0V-0.4V
P2-20	TMCREADY	Output	MLV under test, CPU Boaro - D	P1-15	TMCREADY is the MCREADY signal line to the CPU board in the MLV under test. This is an externally generated READY signal to the 8080 microprocessor and it must be synchronized to the rising edge of Ø2 (the falling edge of /TO2). It is used to synchronize the 8080 CPU with slower memory or I/O devices. When it is a logic "1", it indicates that valid memory or input data is available to the 8080 CPU from an external device. When it is a logic "0", it indicates that external data is not ready and the 8080 CPU will go into a wait state.	"1" = 2.4V-5.0V "0" = 0.0V-0.4V

TEST CARD CONNECTOR AND PIN NUMBER	SIGNAL NAME	INPUT/ OUTPUT	SOURCE/ DESTINATION	SOURCE/ DESTINATION CONNECTOR/ PIN NUMBER	FUNCTION	LOGIC LEVELS
P2-21	/THOLDR	Output	MLV under test CPU Board - D	P1-57	/THOLDR is the /HOLDR signal to the CPU board in the MLV under test. When it is set to a logic "0", it will cause the 8080 microprocessor to enter into a HOLD state. This will cause the 8080 microprocessor to put all its address lines and output data lines into a high impedance state and to set HLDA to a logic "1". When it is set to a logic "1", it will cause the 8080 microprocessor to exit the HOLD state	"1" = 2.4V-5.0V "0" = 0.0V-0.4V
P2-22	/TMEMDIS	Output	MLV under test, CPU Board - D	P1-25	/TMEMDIS is the /MEMDIS signal to the CPU board in the MLV under test. It is primarily used for diagnostics When it is a logic "0", it disables the memory and enables the TDMA data lines onto the DI bus of the CPU board	"1" = 2.4V-5.0V "0" = 0 0V-0.4V
P2-23	/TDIENB	Output	MLV under test, CPU Board - D	P1-50	/TDIENB is the /DIENB signal sent to the CPU board in the MLV under test. When it is a logic "0", it will enable the DI bus onto the 8080 data bus.	"1" = 2.4V-5 0V "0" = 0 0V-0.4V

TEST CARD CONNECTOR AND PIN NUMBER	SIGNAL NAME	INPUT/ OUTPUT	SOURCE/ DESTINATION	SOURCE/ DESTINATION CONNECTOR/ PIN NUMBER	FUNCTION	LOGIC LEVELS
P2-24	/TDBDIS	Output	MLV under test, CPU Board - D	P1-51	/TDBDIS is the /DBDIS signal sent to the CPU board in the MLV under test. When it is a logic "0", it will enable the TDMA data onto the DB bus and if the signal /TDBENB is a logic "1", it will make the outputs of the DB buffers go to a high impedance state	"1" = 2.4V-5.0V "0" = 0.0V-0 4V
P2-25	/TADRDIS	Output	MLV under test, CPU Board - D	P1-28	/TADRDIS is the /ADRDIS signal sent to the CPU board in the MLV under test When it is a logic "0", it will make the outputs of the address buffers go to a high impedance state.	"1" = 2 4V-5.0V "0" = 0 0V-0.4V
P2-28	/TMCINTR	Output	MLV under test, CPU Board - D	P1-21	/TMCINTR is the /MCINTR signal sent to the CPU board in the MLV under test. When it is set to a logic "0" and back to a logic "1", it will set an interrupt request to the 8080 microprocessor	"1" = 2.4V-5.0V "0" = 0.0V-0.4V
P2-29	/TDMAWR	Output	MLV under test, CPU Board - D	P1-16	/TDMAWR is the /DMAWR signal sent to the CPU board in the MLV under test. This signal has no effect when the signal /TDBDIS is set to a logic "1" When /TDBDIS is a logic "0", setting /TDMAWR to a logic "1" will cause the system WR signal to go to a logic "0". Setting it to a logic "0" will cause the system WR signal to go to a logic "1".	"1" = 2.4V-5.0V "0" = 0.0V-0.4V

TEST CARD CONNECTOR AND PIN NUMBER	SIGNAL NAME	INPUT/ OUTPUT	SOURCE/ DESTINATION	SOURCE/ DESTINATION CONNECTOR/ PIN NUMBER	FUNCTION	LOGIC LEVELS
P2-30	/TMCSTB	Output	MLV under test, CPU Board - D	P1-20	/TMCSTB is the /MCSTB signal sent to the CPU board in the MLV under test This is an externally generated status strobe signal generated by putting it to a logic "0" and then back to a logic "1" (pulse duration must be greater than 100 μsec) It is used to latch the status word from the DB data lines MEMACV, INP, OUT, AND IMDIS form the status word	"1" = 2.4V-5 0V "0" = 0.0V-0 4V
P2-31	/TSTATDIS	Output	MLV under test, CPU Board - D	P2-51	/TSTATDIS is the /STATDIS signal sent to the CPU board in the MLV under test. When this is set to a logic "0", it causes the outputs of the status word latch to go to a high impedance state. The externally generated signals TMEMACV, TINP, TIMDIS AND TOUT can be sent into the status bus of the MLV under test	"1" = 2.4V-5 0V "0" = 0.0V-0 4V
P2-46	/TDBENB	Output	MLV under test, CPU Board - D	P2-52	/TDBENB is the /DBENB signal sent to the CPU board in the MLV under test When it is set to a logic "0" it will enable the DB buffer on the CPU board.	"1" = 2.4V-5.0V "0" = 0 0V-0.4V

TEST CARD CONNECTOR AND PIN NUMBER	SIGNAL NAME	INPUT/ OUTPUT	SOURCE/ DESTINATION	SOURCE/ DESTINATION CONNECTOR/ PIN NUMBER	FUNCTION	LOGIC LEVELS
P2-53	/THLDA	Input	MLV under test, CPU Board - S	P2-56	/THLDA is the /HLDA signal sent from the CPU board in the MLV under test. This is the hold acknowledge signal from the 8080 microprocessor. When it is a logic "0", the 8080 microprocessor is in a HOLD state and all the address and data outputs are a high impedance	"1" = 2.4V-5.0V "0" = 0.0V-0.4V
P2-54	TMEMACV	Input/ Output	MLV under test, CPU Board	P2-49	TMEMACV is the MEMACV signal from the CPU board in the MLV under test. A logic "1" indicates that memory is to be enabled for a memory read or write operation When /TSTATDIS is a logic "0" an externally generated /TMEMACV signal may be put on this line.	"1" = 2 4V-5.0V "0" = 0.0V-0.4V
P2-55	TINP	Input/ Output	MLV under test, CPU Board	P2-50	TINP is the INP signal from the CPU board in the MLV under test A logic "1" indicates that the 8080 microprocessor is going to do an input operation When /TSTATDIS is a logic "0" an externally generated /TINP signal may be put on this line	"1" = 2.4V-5.0V "0" = 0 0V-0.4V
P2-56	TIMDIS	Input/ Output	MLV under test, CPU Board	P2-4	TIMDIS is the IMDIS signal from the CPU board in the MLV under test A logic "1" disables the memory and enables the DMAD data bus to the DI bus. It goes to a logic "1" while the 8080 microprocessor is processing an	"1" = 2.4V-5.0V "0" = 0.0V-0.4V

TEST CARD CONNECTOR AND PIN NUMBER	SIGNAL NAME	INPUT/ OUTPUT	SOURCE/ DESTINATION	SOURCE/ DESTINATION CONNECTOR/ PIN NUMBER	FUNCTION	LOGIC LEVELS
					Interrupt When /TSTATDIS is a logic "0" an externally generated /TIMDIS signal may be put on this line.	
P2-57	TOUT	Input/ Output	MLV under test, CPU Board	P2-8	TOUT is the OUT signal from the CPU board in the MLV under test A logic "1" indicates that the 8080 microprocessor is going to do a data output operation When /TSTATDIS is a logic "0" an externally generated /TOUT signal may be put on this line	"1" = 2 4V-5 0V "0" = 0.0V-0 4V
P2-1	I/O CON1	Input/ Output	Diagnostic MLV, Spare 1 Board	P2-1	I/O CON1 is a connecting I/O signal path between the I/O board and the spare 1 and spare 2 boards It is currently not used	'1" = 2.4V-5 0V "0" = 0 0V-0 4V
			Spare 2 Board	P2-1		
P2-35	I/O CON2	Input/ Output	Diagnostic MLV, Spare 1 Board	P2-35	I/O CON2 is a connecting I/O signal path between the I/O board and the Spare 1 and Spare 2 boards. It is currently not used.	"1" = 2.4V-5.0V "0" = 0.0V-0.4V
			Spare 2 Board	P2-35		

APPENDIX B

COMMAND ADDRESS WORD LIST

10 SCOPE.

10.1 Scope. This appendix specifies the functional requirements of the Test Set Adapter Group (TSAG) test card circuit card assembly (A1). This appendix is a mandatory part of this specification. The information contained herein is intended for compliance.

20 APPLICABLE DOCUMENTS.

This section is not applicable to this document.

CAW 00

In/Out IN

Description Reads MLV DB bus, positive logic levels

Bit Functions:

LSB B0 DBØ

B1 DB1

B2 DB2

B3 DB3

B4 DB4

B5 DB5

B6 DB6

MSB B7 DB7

Additional Notes

CAW 01

In/Out IN

Description READS MLV DI BUS, positive logic levels

Bit Functions:

LSB B0 DIØ

B1 DI1

B2 DI2

B3 DI3

B4 DI4

B5 DI5

B6 DI6

MSB B7 DI7

Additional Notes:

CAW 02

In/Out IN

Description READS THE FOUR BIT STATUS BUS AND READY BITS FOR THE TAPE INTERFACE

Bit Functions:

B0	Single Read Ready	1 = ready
B1	Pack Read Ready	1 = ready
B2	Write Ready	1 = ready
B3	X	
B4	MEMACV	(+) logic
B5	INP	(+) logic
B6	IMDIS	(+) logic
B7	OUT	(+) logic

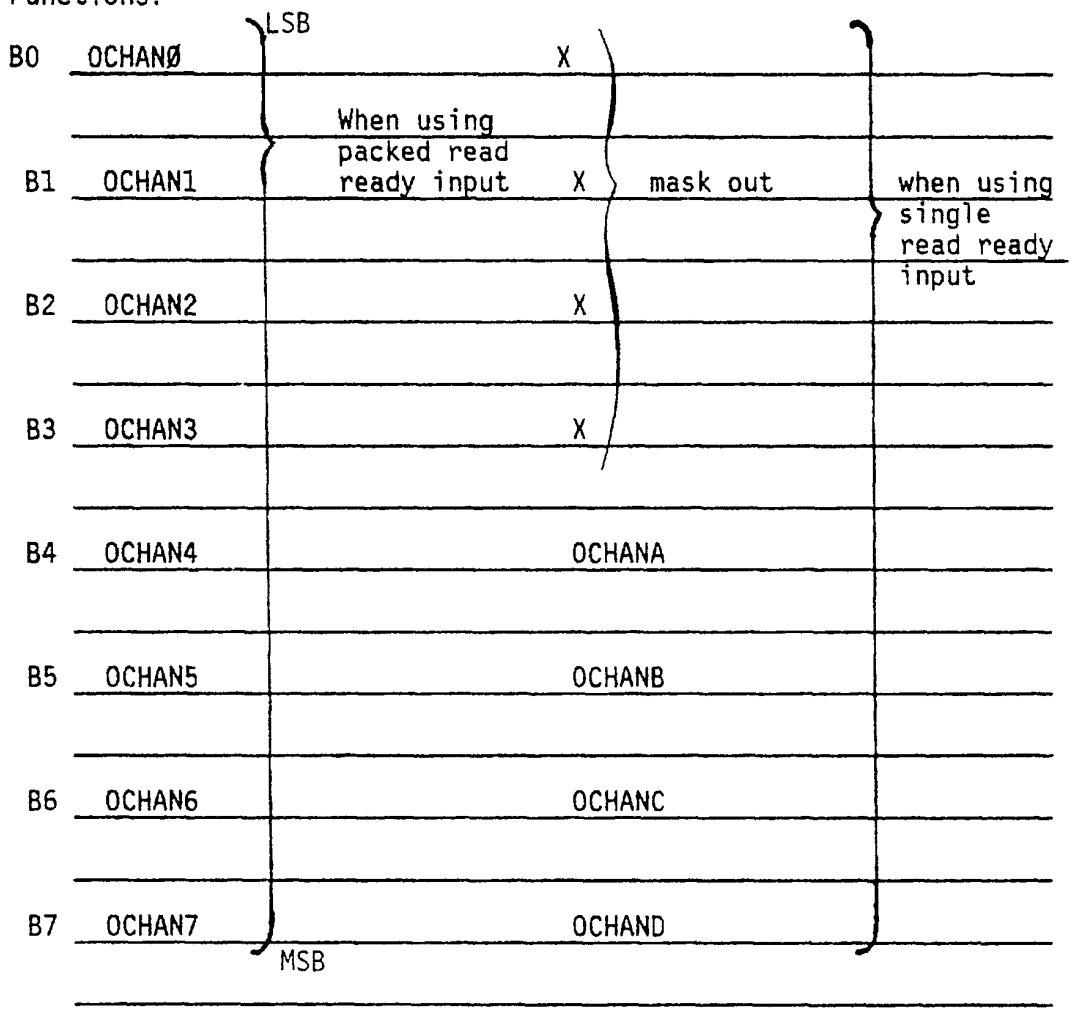
Additional Notes. X = don't care condition

CAW 03

In/Out IN

Description READS DATA FROM THE TAPE UNIT, POSITIVE LOGIC LEVELS

Bit Functions:



Additional Notes: X = don't care condition

CAW 04

In/Out IN

Description READS TAPE UNIT STATUS WORD AND HOLDA SIGNAL

Bit Functions:

LSB B0	SBOT	1 - beginning of tape
B1	SEOT	1 - end of tape
B2	SSTOP	1 - stopped
B3	SRUN	1 - running
B4	SNBL	1 - enabled
B5	BSBLOCK	1 - in data block
B6	/HOLDA	0 - in hold state
MSB B7	X	input must be masked out when reading data. (floating input)

Additional Notes. X = don't care condition

CAW 05

In/Out OUT

Description SENDS OUT LS 8 BITS OF ADDRESS BUS, POSITIVE LOGIC LEVELS

Bit Functions:

LSB B0 BAØ

B1 BA1

B2 BA2

B3 BA3

B4 BA4

B5 BA5

B6 BA6

MSB B7 BA7

Additional Notes: Outputs go to a high impedance-state on turn-on. Bit 1 of out 08 must be set to a one to enable outputs

CAW 06

In/Out OUT

Description SENDS OUT MS 8 bits of address bus, positive logic levels

Bit Functions:

LSB B0 BA8

B1 BA9

B2 BA10

B3 BA11

B4 BA12

B5 BA13

B6 BA14

MSB B7 BA15

Additional Notes Outputs go to a high impedance state on power turn-on. Bit 2 of out 08 must be set to a one to enable outputs.

CAW 07

In/Out OUT

Description SENDS OUT DMADØ-DMAD7 TO MLV, POSITIVE LOGIC LEVELS

Bit Functions:

LSB B0 DMADØ

B1 DMAD1

B2 DMAD2

B3 DMAD3

B4 DMAD4

B5 DMAD5

B6 DMAD6

MSB B7 DMAD7

Additional Notes:

CAW 08

In/Out OUT

Description CONTROLS THE TRI-STATE OUTPUTS TO THE MLV UNDER TEST.

ALL OUTPUTS GO TO A LOGIC "0" WHEN POWER IS TURNED ON TO THE TEST CARD

Bit Functions:

B0 X

B1 "1" Enables BA0 - BA7 outputs

B2 "1" Enables BA8 - BA15 outputs

B3 "1" Enables CNBL, CDIR, CSPEED, CMOVE, CWRITE, & ICLOCK OUTPUTS

B4 "1" Enables MFMACV, INP, IMDIS, AND OUT OUTPUTS

B5 "1" ENABLES ICHANA-ICHAND

B6 X

B7 X

Additional Notes. X = don't care condition

CAW 09

In/Out OUT

Description OUTPUT CONTROL

Bit Functions:

B0 0 = MCREADY stays at a "1", 1 = single step cycle execution

B1 /HOLDR, "1" = Hold Request

B2 /MEMDIS, "1" = Disable Memory

B3 /DIENB "1" = Enable DI Buffer

B4 /DBDIS, "1" = Disable DB Buffer

B5 /ADRDIS, "1" = Disable Address Buffer

B6 /DISABLE, "1" = Disable Tape Unit Control Buffer

B7 /MCINTR, "1" = Interrupt Request

Additional Notes: On power turn-on, all outputs are set to a logic "0"

For single step cycle execution, see /CAW (25)

CAW DA

In/Out IN

Description Reads ICHANA - ICHAND (data sent by the MLV tape interface to the tape unit) and status and control signals from the MLV under test

Bit Functions:

B0 ICHANA + logic

B1 ICHANB + logic

B2 ICHANC + logic

B3 ICHAND + logic

B4 /WAIT - logic, wait = 0

B5 /PWRGOOD - logic, PWR GOOD = 0

B6 /MEMENB - logic 0 = memory enabled from 4000_{16} to $5FFF_{16}$

B7 /CAWENB - logic, 0 = CAW ENB

Additional Notes:

CAW OB

In/Out

Description NOT USED

Bit Functions:

B0

B1

B2

B3

B4

B5

B6

B7

Additional Notes.

CAW 0C

In/Out OUTPUT

Description SENDS OUT A 8 BIT WORD TO THE TAPE UNIT, POSITIVE LOGIC LEVELS

Bit Functions:

B0 ICHAN0

B1 ICHAN1

B2 ICHAN2

B3 ICHAN3

B4 ICHAN4

B5 ICHAN5

B6 ICHAN6

B7 ICHAN7

Additional Notes. BØ - B7 outputs go to a high impedance output on power turn-on. Bit 5 of out 08 must be set to a one to enable outputs. Disable must be set to a zero before these outputs can be enabled

CAW 0D

In/Out OUT

Description SENDS CONTROL WORD TO MLV

Bit Functions:

LSB B0 DMAWR, "1" = Write Pulse Active

B1 MCSTSTB, "1" = Strobe Pulse Active

B2 STATDIS, "1" = Status Bus Disabled

B3 DBENB, "1" = DB Bus Enabled

B4 MEMACV "1" = Memory Active

B5 INP "1" = Input Operation

B6 IMDIS "1" = Interrupt, Memory Disabled

MSB B7 OUT "1" = Output Operation

Additional Notes: Outputs BØ-B3 are set to a logic "0" on power turn-on. Outputs B4-B7 are set to a high impedance state on turn-on To enable their outputs, bit 4 of OUT (08) must be set to a logic "1"

CAW .0E

In/Out IN

Description READS CONTROL WORD SENT BY MLV TO TAPE UNIT

Bit Functions:

LSB B0	CNBL	1-enable tape unit
B1	CDIR	1-forward
B2	CSPEED	1-high speed
B3	CMOVE	1-move tape
B4	CWRITE	1-write
B5	ICLOCK	Write clock, 10KHZ rate
B6	X	Floating inputs, must be masked out
B7	X	

Additional Notes

CAW 0F

In/Out OUT

Description OUTPUTS CONTROL WORD TO TAPE UNIT AND TAPE INTERFACE

Bit Functions:

B0 CNBL 1 - enable

B1 CDIR 1 - forward

B2 CSPEED 1 - high speed

B3 CMOVE 1 - move

B4 CWRITE 1 - write

B5 1 - Reset ICLOCK, 0 - Turn ICLOCK ON

B6 X not used

B7 X not used

Additional Notes: Bit 3 of out 08 must be set to a "1" to enable the following outputs: CNBL, CDIR, CSPEED, CMOVE, CWRITE, ICLOCK

X = don't care condition

These outputs go to a high impedance state on power turn-on. Disable must be set to a zero before these outputs can be enabled.

CAW 20

In/Out IN

Description LOOKS AT THE ID IDENTIFICATION OF THE CARD AND A STATUS SIGNAL FROM THE MLV UNDER TEST.

Bit Functions:

B0 /WR "0" = Write Pulse Active

B1 "0"

B2 X

B3 X

B4 "0"

B5 "1" Card I/D Word

B6 "0"

B7 "0"

Additional Notes X = don't care condition

CAW 21

In/Out IN

Description READS THE STATUS WORD FROM THE MLV UNDER TEST

Bit Functions:

B0	INTA	"1" = Interrupt Acknowledge
B1	/WO	"0" = Write or Output Operation
B2	STACK	"1" = Stack Operation
B3	HLTA	"1" = Halt Acknowledge
B4	OUT	"1" = Output Operation
B5	M1	"1" = Fetch Cycle Execution
B6	INP	"1" = Input Operation
B7	MEMR	"1" = Memory Read Operation

Additional Notes:

CAW 22

In/Out

Description NOT USED

Bit Functions.

B0

B1

B2

B3

B4

B5

B6

B7

Additional Notes.

CAW 23

In/Out IN

Description READS THE ADDRESS LINES ON THE MLV UNDER TEST, POSITIVE LOGIC LEVELS

Bit Functions:

B0 BAØ

B1 BA1

B2 BA2

B3 BA3

B4 BA4

B5 BA5

B6 BA6

B7 BA7

Additional Notes:

CAW 24

In/Out IN

Description READS THE ADDRESS LINES ON THE MLV UNDER TEST, POSITIVE LOGIC LEVELS

Bit Functions:

B0 BA8

B1 BA9

B2 BA10

B3 BA11

B4 BA12

B5 BA13

B6 BA14

B7 BA15

Additional Notes:

CAW 25

In/Out OUT

Description SINGLE STEP CYCLE EXECUTION CONTROL FOR THE MLV UNDER TEST

Bit Functions:

B0 1 = Single Step

B1 X

B2 X

B3 X

B4 X

B5 X

B6 X

B7 X

Additional Notes: EACH TIME AN OUT 25 IS EXECUTED WITH BIT Ø SET TO A "1", THE MLV UNDER TEST WILL EXECUTE A SINGLE CYCLE STEP

X = don't care condition.

CAW 26

In/Out OUT

Description SETS /RESIN TO A ZERO

Bit Functions:

B0 X

B1 X

B2 X

B3 X

B4 X

B5 X

B6 X

B7 X

Additional Notes. X = don't care condition

CAW 27

In/Out OUT

Description SETS /RESIN TO A ONE

Bit Functions:

B0 X

B1 X

B2 X

B3 X

B4 X

B5 X

B6 X

B7 X

Additional Notes: X = don't care condition

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STANDARDIZATION DOCUMENT IMPROVEMENT PROPOSAL

(See Instructions – Reverse Side)

1 DOCUMENT NUMBER	2 DOCUMENT TITLE
MIL-T-85284(AS)	Test Set, Adapter Group, OF-65/ASM

3a. NAME OF SUBMITTING ORGANIZATION	4 TYPE OF ORGANIZATION *(Mark one)*
	☐ VENDOR
b ADDRESS *(Street, City, State, ZIP Code)*	☐ USER
	☐ MANUFACTURER
	☐ OTHER *(Specify)* _____

5 PROBLEM AREAS

a. Paragraph Number and Wording

b Recommended Wording

c Reason/Rationale for Recommendation

6 REMARKS

7a. NAME OF SUBMITTER *(Last First, MI)* – Optional	b WORK TELEPHONE NUMBER *(Include Area Code)* – Optional
c MAILING ADDRESS *(Street City, State, ZIP Code)* – Optional	8 DATE OF SUBMISSION *(YYMMDD)*

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