MILITARY SPECIFICATION

TURRET SUBSYSTEM, UNIVERSAL (UTS), FOR ARMAMENT SUBSYSTEM, HELICOPTER, 20MM: M97EI AND M97E2, LOGIC CONTROL UNIT ASSEMBLY FOR

This specification is approved for use by the U.S. Army Armament Research and Development Command, and is available for use by all Departments and Agencies of the Department of Defense.

1. SCOPE

1.1 Scope. This specification covers requirements, quality assurance provisions or Logic Control Unit, Gun, for Armament Subsystem Helicopter, 20MM: M97EI and M97E2.

2. APPLICABLE DOCUMENTS

2.1 Government documents.

2.1.1 Specifications and standards. Unless otherwise specified (see 6.2), the following specifications and standards of the issue listed in that issue of the Department of Defense Index of Specifications and Standards (DoDISS) specified in the solicitation, form a part of this specification to the extent specified herein.

SPECIFICATIONS

MILITARY

MIL-B-5087	Bonding, Electrical and Lighting Protection, for Aerospace Systems
MIL-W-63150	Weapons and Support Material, Standard Quality Assurance Provisions for.

Beneficial comments (recommendations, additions, deletions) and any pertinent data which may be of use in improving this document should be addressed to: Commander, US Army Armament Research and Development Command, Attn. DRDAR-QA, Dover, New Jersey 07801 by using the self-addressed Standardization Document Improvement Proposal (DD Form 1426) appearing at the end of this document or by letter.

STANDARDS

MILITARY

MIL-STD-105	-	Sampling procedures and Tables for Inspection by Attributes.
MIL-STD-109	-	Quality Assurance Terms and Definitions.
MIL-STD-704	-	Electric Power, Aircraft Characteristics and Utilization of.
MIL-STD-810	-	Environmental Test Methods.

2.1.2 Other Government documents, drawings, and publications. The following other Government documents, drawings, and publications form a part of this specification to the extent specified herein.

DRAWINGS

US ARMY RESEARCH AND DEVELOPMENT COMMAND (ARRADCOM)

PRODUCT

11830922	-	Logic Control Unit Assembly

PACKAGING

P11830922	-	Logic Control Unit Assembly

AMERICAN SOCIETY FOR TESTING AND MATERIALS (ASTM)

ASTM B117	-	Method of Salt Spray (Fog) Testing.

(Application for copies should be addressed to: American Society for Testing Materials, 1916 Race Street, Philadelphia, PA 19103.)

(Copies of specifications, standards, drawings, and publications required by suppliers in connection with specified procurement functions should be obtained from the procuring activity or as directed by the contracting officer.)

2.1.3 Order of precedence. In the event of a conflict between the test. of this specification and the reference cited herein, the text of this specification shall take precedence.

3. REQUIREMENTS

3.1 Item definition. The logic control unit (LCU) as defined by Drawing 11830922 shall be configured for use in an AH-IS helicopter equipped with XM97E1 20 mm Armament Subsystem. The control is a totally enclosed box that contains the required circuitry to translate signals from the aircraft Into appropriate signals for turrent subsystem control and safe weapon firing sequences. The following functions shall be performed by the LCU:

a. Convert resolver signals into appropriate inputs for the air craft Stabilization Control Augmentation System (SCAS) and also provide a control signal to enable the SCAS.

b. Sense an out-of-coincidence. condition between the turrent and sighting station and also provide the necessary signals to drive the turrent back in alignment with the sighting station.

c. Sense an angular difference (in azimuth or elevation) between the turrent and sighting station in excess of 1.5 degrees and provide a gun firing interrupt signal until the turrent and sight are in alignment.

d. Limit the down elevation travel of the turret subsystem to 4.5 degrees while the system is in the ground mode and to provide a logic signal indicating this condition.

e. Provide gun firing interrupt whenever +18 volts direct current (Vdc) or -18 Vdc is not supplied externally.

f. Provide +15 Vdc, -15 Vdc, +5 Vdc to supply the electronics contained within the LCU.

g. Provide the system with a 28 Vdc signal indicating that the 20MM Armament Subsystem is selected on the LCU control switch.

3.1.1 Major components list. The major components shall be as specified in Table I.

TABLE I. Major component list.

Component	Ref. Des.	Drawing
Case	--	11830531
Component Assembly, Power Supply and SCAS	A1	11830441

Component Assembly, Torque Command	A2	11830988
Component Assembly, Depression Limit	A4	11830798
Component Assembly Coincidence Sensor	A5	11830724
Component Assembly Interconnection	A6	11830797

3.1.2 Government furnished property list. See 6.2c.

3.1.3 Electrical power supply. The LCU shall operate from power sources with characteristics conforming to MIL-STD-704. The power supplies for all acceptance tests shall be as specified in Table II.

TABLE II. Electrical power.

Pin	Function	Input Power
J2-e	115 Vac	115 Vac (±5%), 400 Hz (±5%), 200 mA
J2-f	115 Vac Return	115 Vac Return
J2-h	28 Vdc	28 (+0.5, -0) Vdc, Current of 1.5 amps
J2-g	Return for all dc and 26 Vac supplies	Ground
J2-U	26 Vac	26 Vac (±5%), 400 Hz (±5%), 8mA

3.1.3.1 Ground. When the LCU is installed in the helicopter, the enclosures mounting provisions shall be electrically bonded in accordance with MIL-B-5087.

3.2 Material. Materials shall be in accordance with applicable drawings, specifications, and standards.

3.3 Assembly. The Logic Control Unit Assembly shall comply with all requirements specified on Drawing (Dwg) 11830922, all associated drawings, and with all requirements specified in applicable specifications, and standards.

3.4 Interchangeability. All parts having the same part number shall be completely interchangeable with each other and with like parts of other manufacture with respect to installation and performance. Parts joined together by welding, brazing or riveting shall be interchangeable as assemblies. Interchangeability shall be in accordance with MIL-STD-454, Requirement 7.

3.5 First article inspection. This specification contains technical provision for first article inspection. Requirements for the submission of first article by the contractor shall be as specified in the contract ancf 4.4.

3.6 Characteristics.

3.6.1 Performance. The LCU shall comply with the performance requirements specified herin, when tested as specified in 4.5, 4.6 and 4.7.

3.6.1.1 Electronic characteristics. The LCU electronic characteristics shall be as specified in Table III.

TABLE III. Electronic characteristics.

Connector Pin	Function	Characteristics	
		Voltage	Current
J1-A	Gunner Q-Signal Input	0-10 Vac 400 Hz	Differential amplifier, A5AR1, inverting input via relay contacts and 348 kilohms.
JI-B	Gunner Q-Signal Return	Return See J1-A	Return
J1-C	Chassis Ground		
J1-D	Elevation Servo Error Output	0-3 Vac 400 Hz	Into a minimum load of 200 kilohms.
J1-E	Elevation Servo Error Return	Return	Low level return
J1-F	Yaw Output Voltage Return	Return	Low level return
JI-G	Azimuth Demod Input	O to +3 Vdc	Current into a single ended inverting amplifier through a 10 kilohms resistance.
J1-H	Elevation Demod Input	O to +3 Vdc	Same as J1-G

TABLE III. Electronic characteristics (continued)

Connector Pin	Function	Characteristics	
		Voltage	Current
J1-J	Forcing Function of V_x Signal output	0-10 Vac	Into a minimum load of 200 kilohms.
J1-K	Forcing Function or V_x Signal Return		Low level return
J1-L	Azimuth Interlock Output	O or 20 Vdc ±15% through RTL impedance	N/A
J1-M	Elevation Interlock Output	O or 28 Vdc ±10% through a 1OK +10% resistance	N/A
JI-R	Gun Drive Relay Return	Through wire to J2-n	Current not to exceed 1 ampere
J1-S	Pilot Q Signal Return		Same as J1-B
J1-T	Pilot Q Signal Input		Same as J1-A
J1-U	V_x Signal Input	0 to 10 Vac 400 Hz	Differential amplifier input AIAR1 via lOOK and inverting input of A5AR1 via 511 kilohms ±5% in parallel with a 0.01-microfarad capacitor to Pin J1-e
J1-V	Elevation Error Input	0 to 10Vac 400 Hz	Differential amplifier A4AR4 inverting input via 100 kilohms in addition to a 0.01-microfarad capacitor to J1-W
J1-W	Elevation Error Input Return	Return See J1-V	Return
J1-X	Yaw Signal Output	0 to 10Vac 400 Hz	Minimum of 10-kilohm load to ground

TABLE III. Electronic characteristics (continued)

Connector Pin	Function	Characterlstics	
		Voltage	Current
J1-Y	Roll Signal Output		Similar to J1-X
J1-Z	Roll Signal Return	Return, see JI-Y	Low level return
J1-a	Pitch Signal output		Similar to J1-X
J1-b	Pitch Signal Return	Return, see J1-a	Low level return
J1-c	TSU Q Signal Input	0-10 Vac 400 H3	Similar to J1-A
J1-d	TSU Q Signal Return	Return, see J1-c	Similar to J1-B
J1-e	V_x Signal Input Return	Return, see J1-4	Differential amplifier non-inverting input AIAR1 via 100 kilohms and non-inverting input of A5AR1 via 511 kilohms in addition to an 18 kilohms ±5% in parallel with a .01-microfarad capacitor to pin J1-U
J1-f	V_z Signal Input Return	Return, See J1-j	Differential amplifier A1AR2 inverting input via 100 kilohms
J1-g	V_y Signal Input	0 to 10 Vac 400 Hz	Differential amplifier AIAR1 inverting input via 100 kilohms
J1-h	'y Signal Input Return	Return, see J1-g	Return
J1-j	V_z Signal Input	o to 8 Vac 400 Hz	Differential amplifier A1AR2 non-inverting input via 100 kilohms and single ended amplifier A4AR5 inverting input via 100K and a set of normally open relay contacts controlled by J2-J.

TABLE III. Electronic characteristics (continued)

Connector Pin	Function	Characteristics	
		Voltage	Current
J2-A	Track Signal Input	0 or 28 Vdc input	25 mA (relay current) open circuit when J2 B or C = 28 Vdc
J2-B	Pilot Signal Input	0 or 28 Vdc input	50 mA (relay current)
J2-C	Tow Mode Input	0 or 28 Vdc input	50 mA (relay current)
J2-D	+18 Vdc Input	+18 Vdc input	1 mA
J2-E	-18 Vdc Input	-18 Vdc input	1 mA
J2-R	20mm Weapon Select Signal output	O or 28 Vdc	100 mA
J2-U	26 Vac Reference Input	See Table II	See Table 11
J2-X	SCAS Enable Output	0 or 28 Vdc	100 MA maximum
J2-Z	Firing Voltage Signal Input	0 to 28 Vdc	2 mA
J2-b	Gunner Stow Interrupt Input	0 Vdc to 28 Vdc through 10 kilohms into 1 kilohm to ground or 2K to -10 Vdc	
J2-e	115 Vac Input	Refer to Table II	See Table II
J2-f	115 Vac Input Return	Refer to Table 11 (see J2-e)	See Table II
J2-g	28 Vdc Return	Refer to Table II (see J2-h)	See Table II

TABLE III. Electronic characteristics (continued)

connector Pin	Function	Characteristics	
		Voltage	Current
J2-h	28 Vdc Power	Refer to Table II	See Table II
J2-i	Fixed Fwd Input	0 or 28 Vdc	25 mA maximum (relay current)
J2-j	Depression limit Enable	0 or 28 Vdc	25 mA maximum (relay current)
J2-n	Ground Circuit Closure Gun Power Relay	N.A.	Continuity through wire to J1-R
J2-p	Chassis Ground		
J2-q	Chassis Ground		
J2-r	Interlocked Trigger, Ground Circuit Closure	28 Vdc	Relay A2k1 current

TABLE III. Electronic characteristics (continued)

Connector Pin	Function	Characteristics
J3-A(1)	+15 Vdc Test Point	Direct connection to +15 Vdc internal power supply.
J3-B	-15 Vdc Test Point	Direct connection to -15 Vdc internal power supply.
J3-C	Chassis Ground	
J3-D	Depression Limit Condition Signal	+15 Vdc through 10K in normal mode, -15 Vdc through 20 kilohms when in depression limit with J1-j at 1.0 Vac in phase with J2-U.
J3-E	Selected Control Mode (Gunner, Pilot, TSU) Test Point	Voltage same as voltage on J1-A when J2-A, B, and C = 0 Vdc
		Voltage same as voltage on J1-T when J2-B or C = 28 Vdc
		Voltage same as voltage on J1-c when J2-A = 28 Vdc and both J2-B and C = O Vdc
J3-J	Ground Circuit Closure, Gun Power Relay	Continuity through wire to J2-n and J1 -R
J3-K	900 Error Detector Voltage	Voltage across DS1 0.0 ± 0.5 Vdc = unlit 1.6±0.5 Vdc = lit
J3-L	Gunner Stow Interupt Test Point	Parallel with J2-b
J3-P	5 Vdc Test Point	Direct connection to +5 Vdc internal power supply
J3-R	Depression Limit Output to Test Set	Parallel with J1-D

Note 1. J3 is a test connector for system checkout with a test set.

TABLE III. Electronic characteristics (continued)

Connector Pin	Function	Characteristlcs
J3-S	Fire Volts Signal Output to Test Set	Parallel with J2-Z
J3-T	SCAS Enable Output to Test Set	Parallel with J2-X
J3-U	Azimuth 1 1/2° Output to Test Set	0 Vdc when J1-G is greater than ±445 mVdc
		20 Vdc ±0.5 Vdc when J1-G is less than +220 mVdc
J3-V	T1 Transformer Secondary to Test Point	26 Vac 400 Hz
J3-W	Yaw Output to Test Set	Parallel with J1-X
J3-X	Pitch Output to Test Set	Parallel with J1-a
J3-Y	Roll Output to Test Set	Parallel with J1-Y
J3-a	Az 1 1/2° In-put, Test Point	Parallel with J1-G
J3-b	El 1 1/2° Irt-put, Test Point	Parallel with J1-H
J3-c	28 Vdc Input Power Test Point	Parallel with J2-h

3.6.1.2 SCAS component assembly. With the inputs in 3.1.3, the SCAS tnterface circuitry shall exhbit the characteristics as described in the following subparagraphs.

3.6.1 .2.1 SCAS circuit. The following outputs shall occure when the specified inputs are supplied.

Input	Voltage	Output Phase Relationships
a. V_x= 10 Vrms at Pin J1-U	2.15 Vac	+5% in phase with V_x input, ±10 mVDC offset, at Pin J1-a; with V_z input at 0 Vac
V_x Return at Pin J1-e		Return at Pin J1-b
b. V_z= 8V rms at Pin J1-j	4.25 Vac	±5% out of phase with V_z input, ±10 mVdc offset, at Pin J1-a; with V_x input at 0 Vac.
V_z Return at Pin J1-f		V_z Return at Pin J1-b
co V_y = 10V rms at Pin J1-g	4.64 Vac	+5% in phase with V_y input, +10 mVdc offset, at Pins JlyX and J1-Y
V_y Return at Pin J1-h		Return at J1-Z (for J1-Y) J1-X return to chassis ground
d. 28Vdc, J2-h	28 Vdc at J2-R	Note: Weapon select switch, S1, at 20 mm position

3.6.1.3 Torque command component assembly. With input power as specified in 3.1.3 and with the additional inputs described in 3.6.1.3.1, the following outputs shall occur as defined in 3.6.1 .3.2 and 3.6.1.3.3.

3.6.1.3.1 Stabilized Control Augmentation System (SCAS) command signal. When a fire volts pulse train (applied at J2-Z) and an interlocked trigger signal are present (relay A2kl energized), a 28(+2) Vdc signal shall be on J2-X and test connector pin J3-T.

3.6.1.3.2 SCAS output time delays. When the fire volts pulse (a square wave test pulse train of 0 to 28 Vdc amplitude, pulse width of 40 ms, and pulse period of 80 ms) is applied (at J2-Z) and then, the interlocked trigger signal is applied (relay A2kl is energized by grounding Pin J2-r), the output at Pin J2-X shall rise to 28 (±2) Vdc after a delay of 50 (±30) ms. When the interlocked trigger signal is removed (Pin J2-r disconnected from ground, the

output at Pin J2-X shall remain at 28 (±2) Vdc for 350 (±100) ms before returning to 0 (±0.5) Vdc. When the interlocked trigger signal is applied first, and then, the fire volts pulse train is applied, the output at Pin J2-X shall rise to 28 (±2) Vdc following a maximum delay of 6 ms after the beginntng of the second fire volts input pulse. When the fire volts input pulses are removed, the output shall remain for 350 (±100) ms after start of the last input pulse.

3.6.1.3.3 SCAS circuitry with low frequency pulse input. The output at Pin J2-X shall change from 28 (±2) Vdc to 0(±0.5) Vdc if the period between the fire volts pulse input increases beyond 165 milliseconds.

3.6.1.4 Depression limit component assembly. With input power as specified i n3.1.3 and with the additional inputs described below, the following outputs shall occur.

3.6.1.4.1 Depression limit circuit, no-limit mode. When the following inputs are applied, outputs shall occur as specified below:

Input		output
0.5 V rms, 400 Hz, in phase with 26 Vac at Pin J2-U With return to Pin J1-V	applied at Pin J1-V	Voltage at Pin J1-D shall be equal to the input ±7%.
0.5 V rms, 400 Hz, 1800 out of phase with 26 Vac input at Pin J2-U With return to Pin J1-W	applied at Pin J1-V	Voltage at Pin J1-D shall be equal to the input ±7%.

When either of the above two inputs are applied and 1.5 V rms is applied at Pin J1-j, either in-phase or 180 degrees out of phase, with a 26 Vac input at Pin J2-U and the return to Pin J2-g, there shall be no effect on the output at Pin J1-D.

3.6.1 .4.2 Depression limit circuit, limit mode. When 28 (+0.5 -O) Vdc is applied to PinJ2-j with return to Pin J2-g, the following outputs shall occur when the specified inputs are applied.

Input		output
a. At V signal input Pin J1-j with return at Pin J2-g (28 Vdc return) and	apply 1.5 V rms 180 degrees out of phase with the 26 Vac input at Pin J2-U ±7%.	Voltage at Pin J1-D shall be equal to the input at Pin J1-V
at Evaluation error signal input Pin J1-V with return to Pin J1-W	apply 0.5 V rms, 400 Hz	

Input		Output
b. Vary the input at Pin J1-j (with return to Pin J2-g) and with 0.5 V rms 400 Hz (1800 out of phase with 26 Vac input at J2-U) at Pin J1-V (with return to Pin J1-11)	At the point where output becomes as specified, the input at J1-j shall be 0.820 ±10% V rms in phase Vith the 26 Vac input at Pin J2-U	Voltage at Pin J1-D shall be 0.0 ±30 millivolts.

3.6.1.4.3 One and one-half degree azimuth error detector. With the initial conditions as specified below, the outputs shall be in accordance with 3.6.1.4.3.1 and 3.6.1.4.3.2.

a. Input power as specified in 3.1.3

b. +18 Vdc ±10 percent at Pin J2-D

c. -18 Vdc ±10 Percent at Pin J2-E

d. 7(+0, -1 V) rms, 400 Hz (±5 percent) at Pin J1-A, in phase with the 26 Vac applied to Pin J2-U, with return to Pin J1-B

e. 28 (+0.5, -O) Vdc through a 10,000 ohm (±5 percent) 0.25 watt resistor to Pin J2-b

3.6.1 .4.3.1 Output for azimuth error detector. With the initial conditions of 3.6.1.4.3 plus the inputs given below, the outputs shall be:

Input	Output
28 (±0.5, -O) Vdc at Pin J2-j, and 5 V rms (±5%) at Pin J1-j, 1800 out of phase with the 26 Vac applied at Pin J2-U, with return to Pin J1-f	20 Vdc (±15%) at PinJ1-L
A positive or negative polarity d-c voltage at Pin J1-G which is increased in level from zero until J1-L changes to a O Vdc level. The voltage on J1-G shall be between 222 to 445 mVdc with either of the polarity applied to J1-G	Voltage at Pin J1-L changes from 20 Vdc (±15%) to 0(±0.4) Vdc

3.6.1.4.3.2 Output of J1-L. The output of J1-L shall be O (+ 4) Vdc when the inputs of 3.6.1 .4.3 occur and if any one or more of the following conditions occur:

a. 0 Vdc on J1-G, 28 Vdc on J2-j, and 1 Vac on J1-j in phase with J2-U

b. 0 Vdc on J2-D

c. 0 Vdc on J2-E

d. 0 Vac on J1-A

e. 0 Vdc on J2-b.

3.6.1.4.4 One and one-half degree elevation error detector. With input power as specified in 3.1.3 and O Vdc (±0.200) on J1-H, the output at J1-H shall be 28 (±1.0) Vdc (open circuit, i.e., no load at J1-H). When J1-H input is increased in either dc polarity, the output at J1-M shall change from 28 Vdc to O (±0.4) Vdc prior to a maximum of 445 millivolts dc.

3.6.1.5 Coincidence sensor component assembly. With the inputs as specified below, the events described in the following subparagraphs shall occur.

a. Input power as specified in paragraph 3.1.3.

b. +18 Vdc (±10 percent) at Pin J2-D.

c. -18 Vdc (±10 percent) at Pin J2-E.

d. 28 (+0.5, -0) Vdc through a 10,000 ohm O.25 watt (±5 percent) resistor at Pin J2-b.

3.6.1 .5.1 Gunner Q-signal, in-phase. When the input at Pin JI-A (with return to Pin J1-B) is 7 (+0, -1) V rms, 400 Hz ±5 percent in phase with the 26 Vac signal input at Pin J2-U, the following outputs shall occur:

a. 20 Vdc (±15 percent) at Pin J1-L.

b. The resistance between Pin J1-J and Pin J1-U shall be less than 5 milliohms.

c. The light-emitting diode (LED) DS1 shall be off.

3.6.1 .5.2 Gunner Q-signal, in-phase and low voltage. When the input signal is applied at Pin J1-A as specified in 3.6.1.5.1 except that the amplitude is decreased to a threshold causing the output at Pin J1-L to change from 20 (±13%) Vdc to O (±1) Vdc, the following shall occur:

a. The threshold level at the input, Pin J1-A, shall be 4.75 (21) V rms.

b. The resistance between Pin J1-J and Pin J1-U shall be less than 5 milliohms.

c. The LED DSI shall be off.

3.6.1.5.3 Gunner Q-signal, out-of-phase. When the input at Pin J1-A is as specified in 3.6.1.5.1, except that the amplitude is decreased to zero and then-increased out of phase with the 26 Vac at Pin J2-U from zero to 7 V rms, the following outputs shall occur during the out-of-phase condition:

a. Zero (±1) Vdc at Pin J1-L.

b. The LED DSI shall be on.

The voltage at Pin J1-J shall be 7.31 (±10%) Vat, 400 Hz in phase with J2-U.

d. The resistance between Pin J1-J and Pin J1-U shall be 560K ohms (±5 percent).

3.6. 1.5.4 Pilot Q-signal. With 28.0 (+0.5, -O) Vdc applied to Pin J2-B, the voltages specified in 3.6.1.5 applied, and voltage applied to Pin J1-T instead of Pin J1-A; the characteristics as defined in 3.6.1 .5.1 through 3.6.1.5.3 shall occur.

3.6.1 .5.5 TSU Q-signal. With 28.0 (+0.5, -O) Vdc applied to Pin J2-A, the voltages specified in 3.6.1.5 applied, and voltage applied to Pin J1-C instead of Pin J1-A; the characteristics as defined in 3.6.1 .5.1 through 3.6.1.5.3 shall occur.

3.6.1.5.6 Tow mode. With 28.0 (+0.5, -O) Vdc applied to Pin J1-C, the voltages specified in 3.6.1.5 applied, and voltage applied to Pin J1-T instead of Pin J1-A; the characteristics as defined in 3.6.1 .5.1 through 3.6.1 .5.3 shall occur.

3.6.1.5.7 Low voltage on +18V suplies. When the input at Pin J1-A is as specified in 3.6.1.5.1, the output at Pin J1-L shall change for 20 Vdc (±15%) to zero (±1) Vdc when either, or both, of the following events occur:

a. The +18 Vdc input at Pin J2-D decreases below +3 Vdc.

b. The -18 Vdc at Pin J2-E rises above -3 Vdc.

3.6.1.5.8 Fixed forward mode. When 28.0 (+0.5, -O) Vdc is applied to Pin J2-i in conjunction with the following inputs, the outputs specified in the following subparagraphs shall occur.

3.6.1.5.8.1 V in-phase. When 10 (+0, -1) V rms, 400 Hz (±5 Percent) in-phase with the 26 Vac Input at Pin J2-U is applied to Pin JT-U (with return to Pin J1-e), the outputs specified in 3.6.1 .5.1 shall occur.

3.6.1 .5.8.2 V_x signal, in-phase and low voltage. When the input at,pin J1-U is applied as specified In 3.6.1.5.8.1, except that the amplitude is decreased to a threshold causing the output at Pin J1-L to change from 20 Vdc (±15 percent) to zero (±1) Vdc, the following shall occur:

a. The threshold level at the input shall be 6.97 (±1.4) V rms.

b. The output characteristics shall be the same as those specified in 3.6.1.5.2.

3.6.1.5.8.3 V_x out-of-phase. When the input at Pin J1-U is as specified in 3.6.1.5.8.2, except that the amplutude is decreased to zero and then increased (out-of-phase with the 26 Vdc reference) from zero to 10 V rms, the outputs as specified in 3.6.1.5.3 shall occur during the out-of-phase condition.

3.6.1 .5.8.4 Low voltage on +18 V su plies. When the input at PinJ1-U is as specified in 3.6.1.5.8.1, the output as J1-L shall not change when either, or both, the +18 Vdc or the -18 Vdc supplies decrease in magnitude to zero Vdc. The output at Pin J1-L shall remain at 20 Vdc ±15 percent.

3.6.1.6 Elapsed time meter. The LCU shall include a meter that provides a readout in hours of the time that 115 Vac has been supplied.

3.6.1.7 Proof test (first article inspection only). Logic Control Unit Assemblies shall operate when assembled to an accepted Universal Turret Subsystem (UTS).

3.7 Design and construction.

3.7.1 Production drawings. The LCU shall be fabricated and assembled in accordance with the associated drawings, parts lists and other documents listed on Drawing 11830922.

3.7.2 Standards of manufacture. The LCU shall be manufactured to met the requrements of the applicable drawings.

3.8 Environmental Requirements.

3.8.1 Temperature. The operating temperature of the LCU shall be from -65°F to +120°F and non-operating temperature shall be from -65°F to +160°F.

3.8.2 Altitude. The operating altitude of the LCU shall be from sea level to 50,000 feet.

3.8.3 Temperature - altitude combination. The LCU shall meet the requirements of MIL-L-5400 paragraph 3.2.24.4.

3.8.4 Humidity. The LCU shall withstand the effects of humidity up to 100 percent, including conditions where in condensation takes place in and on the LCU. The LCU shall withstand the above conditions during operating and non-operating conditions.

3.8.5 Vibration. The LCU shall meet the requirements of MIL-E-5400 paragraph 3.2.24.5.1.3 except as modified by drawing.

3.8.6 Shock. The LCU shall meet the requirements of MIL-E-5400 paragraph 3.2.24.6.

3.8.7 Sand and dust. The LCU shall withstand, in both an operating and nonoperating condition, exposure to sand and dust particles.

3.8.8 Fungus. The LCU shall withstand, in both an operating and non-operating condition, exposure to fungus drowth as encountered in tropical climates.

3.8.9 Salt fog. The LCU shall withstand in both an operating and nonoperating condition, exposure to salt-see atmospheres.

3.9 Workmanship. Workmanship and finish shall be in accordance with MIL-STD-454, Requirement 7. Finished items and parts shall not exhibit faulty material and processing such as seams, laminations, cracks, visible steps, sharp edges, nicks, scratches, burrs, foreign matter, deformations, and missing operations which may affect serviceability, operation, or safety.

4. QUALITY ASSURANCE PROVISIONS

4.1 Responsibility for inspection and standard quality assurance provisions. Unless otherwise specified herein or in the contract, the provisions of MIL-W-63150 shall apply and are hereby made a part of this detail specification.

4.1.1 Certification provisions. The certification provisions of MIL-W-63150 shall apply.

4.2. Quality assurance terms and definitions. Quality assurance terms and definitions used, herein are in accordance with MIL-STD-109.

4.3 Classification of inspections. Inspections shall be classified as follows:

a. First article inspection.

b. Quality conformance inspection.

4.4 First article inspection.

4.4.1 Submission. The contractor shall submit a first article sample as designated by the Contracting Officer for evaluation in accordance with the provisions of 4.4.2. The first article sample shall consist of the following items in sample quantities as indicated.

Part Description	Drawing	Quantity
Logic Control Unit Assembly	11830922	5
Component Assembly, Power supply and Clearing	11830441	5
Component Assembly, Torque Command	11830988	5
Case, Logic Control Unit	11830531	5
Component Assembly Coincidence Sensor	11830724	5
Component Assembly Interconnection	11830797	5
Component Assembly, Depression Limit	11830798	5

4.4.2 Inspection to be performed. See Table IV.

4.4.3 Rejection. If any assembly, component, or test specimen fails to comply with any of the applicable requirements, the first article sample shall be rejected. The Government reserves the right to terminate its inspection upon any failure of any assembly, component, or test specimen in the sample that fails to comply with any of the stated requirements.

TABLE IV. First article inspection

CLASSIFICATION OF DEFECTS OF TESTS

PARAGRAPH	TITLE		SHEET 1 OF 2		DRAWING NUMBER
	Logic Control Unit Assembly and Components				See Below
					NEXT HIGHER ASSEMBLY
CATEGORY	EXAMINATION OR TEST	NO. OF SAMPLE UNITS	AQL OR 100%	REQUIREMENT PARAGRAPH	PARAGRAPH REFERENCE /INSPECTION METHOD
	Logic Control Unit Assembly (Dwg 11830922)				
	Examination for defects	5		3.3	4.5.2.1
	Interchangeability	3		3.4	4.7
	Proof Test	3		3.6.1.7	4.8
	Component Assembly, Power Supply and Clearing (Dwg 11830441)				
	Examination for defects	5		3.3	4.5.2.2
	Component Assembly, Torque Command (Dwg 11830988)				
	Examination for defects	5		3.3	4.5.2.3
	Case, Logic Control Unit (Dwg 11830531)				
	Examination for defects	5		3.3	4.5.2.4
	Component Assembly, Coincidence Sensor (Dwg 11830724)				
	Examination for defects	5		3.3	4.5.2.5

NOTES:

DRDAR-QA Form 160 Jul 77

TABLE IV. First article inspection

CLASSIFICATION OF DEFECTS & TESTS

PARAGRAPH	TITLE		SHEET 2 OF 2		DRAWING NUMBER
	Logic Control Unit Assembly and Components				See Below
					NEXT HIGHER ASSEMBLY
CATEGORY	EXAMINATION OR TEST	NO. OF SAMPLE UNITS	AQL OR 100%	REQUIREMENT PARAGRAPH	PARAGRAPH REFERENCE /INSPECTION METHOD
	Component Assembly, Interconnection (Dwg 11830797)				
	Examination for defects	5		3.3	4.5.2.6
	Component Assembly, Depression Limit (Dwg 11830798)				
	Examination for defects	5		3.3	4.5.2.7

NOTES:

DRDAR-QA Form 160 Jul 77

4.5 Quality conformance inspection.

4.5.1 Inspection lot formation. The term "inspection lot" is defined as a homogeneous collection of units of product from which a representative sample-is drawn or which is inspected-100 percent to determine conformance with applicable requirements. Units of product selected fro inspection shall represent only the inspection lot from which drawn and shall not be construed to represent any prior or subsequent quantities presented for inspection. Homogeneity shall be considered to exist provided the inspection lot has been produced by one manufacturer in one unchanged process, using the same materials and methods, in accordance with the same drawings, same drawing revisions, same specifications and same specification revisions, and complies with the provisions for submission of product as specified in MIL-STD-105. All material submitted for inspection in accordance with this specification shall comply with the homogeneity criteria specified herein, regardless of the type of inspection procedure which is being applied to determine conformance with requirements.

4.5.2 Examination. The examinations listed in this specification for Classification of Defects shall be performed on inspection lots as defineD in 4.4.1 of this specification. Equipment necessary for the performance of the inspections listed shall be in accordance with 4.5.4.

a. Sampling plans. Unless otherwise specified in the Classification of Defects and Test Tables, sampling plans and procedures for major and minor defects shall be in accordance with MIL-STD-105, Inspection Level II.

4.5.3 Testing. Testing is described in the First Article and Quality Conformance Inspection tables.

4.5.4 Inspection equipment. The inspection equipment required to perform the inspections and tests prescribed in this specification is identified in the "Paragraph Reference/Inspection method" column in the tables starting with paragraph 4.5.2.1, and the test method paragraphs (See 4.6). The contractor shall submit for approval inspection equipment designs in accordance with the terms of the contract. See 6.3 herein.

4.6 Methods of inspection. Any assembly which fails to comply with the specified requirements or evidences degradation of its operational performance shall be classed defective. Test equipment and procedures shall be satisfactory to the Contracting Officer. (See 4.5.4).

4.6.1 Electrical requiarements. The part or assembly shall be subjected to the electrical tests in order to determine conformance to the electrical characteristics specified on the applicable drawing. Test equipment and

4.6.2 Environmental Tests (First article only). The part or assembly shall be subjected to the environmental tests in order to determine conformance to the environmental characteristics specified on the applicable drawing. Test equipment and procedures shall be satisfactory to the contracting agency. If any part or assembly fails to comply with any specified environmental requirement, it shall be classed defective and rejected.

QUALITY CONFORMANCE INSPECTION

CLASSIFICATION OF DEFECTS & TESTS

PARAGRAPH	TITLE		SHEET 1 OF 1		DRAWING NUMBER 11830922
4.5.2.1	Logic Control Unit Assembly				NEXT HIGHER ASSEMBLY ---
CATEGORY	EXAMINATION OR TEST	NO. OF SAMPLE UNITS	AQL OR 100%	REQUIREMENT PARAGRAPH	PARAGRAPH REFERENCE /INSPECTION METHOD
Critical	None defined				
Major					
101	Solder workmanship unsatisfactory		100%	3.3	Visual
102	Wiring workmanship unsatisfactory		100%	3.3	Visual
103	Wire marking improper or missing		100%	3.3	Visual
104	Part or assembly damaged		100%	3.3	Visual
105	Part or assembly missing		100%	3.3	Visual
106	Part or assembly incorrectly assembled		100%	3.3	Visual
107	Performance	a	--	3.6	4.6
Minor					
201	Identification plate separating from surface		1.50%	3.3	Manual
202	Identification plate lettering misleading, unidentifiable or missing		1.50%	3.3	Visual-Manual
203	Exposed surface unprotected (Note 8)		1.50%	3.3	Visual
204	Solder connections not insulated (Note 5)		1.50%	3.3	Visual
205	Silicone compound missing from specified surface		1.50%	3.3	Visual
206	Poor workmanship		2.50%	3.9	Visual

NOTES:

a: Three samples; accept if none fail, reject on one failure.

QUALITY CONFORMANCE INSPECTION

CLASSIFICATION OF DEFECTS & TESTS

PARAGRAPH	TITLE		SHEET 1 OF 1		DRAWING NUMBER
4.5.2.2	Component Assembly, Power Supply and Clearing				11830441
					NEXT HIGHER ASSEMBLY 11830922
CATEGORY	EXAMINATION OR TEST	NO. OF SAMPLE UNITS	AQL OR 100%	REQUIREMENT PARAGRAPH	PARAGRAPH REFERENCE /INSPECTION METHOD
Critical	None defined				
Major					
101	Moisture present on assembly		0.65%	3.3	Visual
102	Moisture protection missing		0.65%	3.3	Visual
103	Solder workmanship poor		0.65%	3.3	Visual
104	Part missing		0.65%	3.3	Visual
105	Assembly damaged		0.65%	3.3	Visual
Minor					
201	Marking misleading, unidentifiable or missing		1.50%	3.3	Visual
202	Fillet missing		1.50%	3.3	Visual
203	Compound on prohibited areas		1.50%	3.3	Visual
204	Poor workmanship		2.50%	3.9	Visual

NOTES:

QUALITY CONFORMANCE INSPECTION

CLASSIFICATION OF DEFECTS & TESTS

MIL-T-63536(AR)

PARAGRAPH	TITLE		SHEET 1 OF 1		DRAWING NUMBER
4.5.2.3	Component Assembly, Torque Command				11830998
					NEXT HIGHER ASSEMBLY 11830922
CATEGORY	EXAMINATION OR TEST	NO. OF SAMPLE UNITS	AQL OR 100%	REQUIREMENT PARAGRAPH	PARAGRAPH REFERENCE /INSPECTION METHOD
Critical	None defined				
Major					
101	Moisture present on assembly		0.65%	3.3	Visual
102	Moisture protection missing		0.65%	3.3	Visual
103	Solder workmanship poor		0.65%	3.3	Visual
104	Part missing		0.65%	3.3	Visual
105	Assembly damaged		0.65%	3.3	Visual
Minor					
201	Marking misleading, unidentifiable or missing		1.50%	3.3	Visual
202	Fillet missing		1.50%	3.3	Visual
203	Compound on prohibited area		1.50%	3.3	Visual
204	Poor workmanship		2.50%	3.9	Visual

NOTES:

DRDAR-QA Form 160 Jul 77

QUALITY CONFORMANCE INSPECTION

CLASSIFICATION OF DEFECTS & TESTS

PARAGRAPH	TITLE		SHEET 1 OF 1		DRAWING NUMBER
4.5.2.4	Case, Logic Control Unit				11830531
					NEXT HIGHER ASSEMBLY 11830922
CATEGORY	EXAMINATION OR TEST	NO. OF SAMPLE UNITS	AQL OR 100%	REQUIREMENT PARAGRAPH	PARAGRAPH REFERENCE /INSPECTION METHOD
Critical	None defined				
Major					
101	Welding workmanship unsatisfactory		0.65%	3.3	Visual
102	Brazing workmanship unsatisfactory		0.65%	3.3	Visual
103	Part missing		0.65%	3.3	Visual
104	Assembly damaged		0.65%	3.3	Visual
Minor					
201	Specified areas not flush after brazing		1.50%	3.3	Visual
202	Protective finish damaged		1.50%	3.3	Visual
203	Primer or final coating present on prohibited areas		1.50%	3.3	Visual
204	Notched tangs not removed		1.50%	3.3	Visual
205	Primer missing from inserts		2.50%	3.9	Visual

NOTES:

QUALITY CONFORMANCE INSPECTION

CLASSIFICATION OF DEFECTS & TESTS

PARAGRAPH	TITLE		SHEET 1 OF 1		DRAWING NUMBER
4.5.2.5	Component Assembly, Coincidence Sensor				11830724
					NEXT HIGHER ASSEMBLY 11830922
CATEGORY	EXAMINATION OR TEST	NO. OF SAMPLE UNITS	AQL OR 100%	REQUIREMENT PARAGRAPH	PARAGRAPH REFERENCE /INSPECTION METHOD
Critical	None defined				
Major					
101	Moisture present on assembly		0.65%	3.3	Visual
102	Moisture protection missing		0.65%	3.3	Visual
103	Solder workmanship poor		0.65%	3.3	Visual
104	Part missing		0.65%	3.3	Visual
105	Assembly damaged		0.65%	3.3	Visual
Minor					
201	Marking misleading, unidentifiable or missing		1.50%	3.3	Visual
202	Fillet missing		1.50%	3.3	Visual
203	Compound on prohibited area		1.50%	3.3	Visual
204	Poor workmanship		2.50%	3.9	Visual

NOTES:

DRDAR-QA Form 160 Jul 77

QUALITY CONFORMANCE INSPECTION

CLASSIFICATION OF DEFECTS & TESTS

PARAGRAPH	TITLE		SHEET 1 OF 1		DRAWING NUMBER 11830797
4.5.2.6	Component Assembly, Interconnection				NEXT HIGHER ASSEMBLY 11830922
CATEGORY	EXAMINATION OR TEST	NO. OF SAMPLE UNITS	AQL OR 100%	REQUIREMENT PARAGRAPH	PARAGRAPH REFERENCE /INSPECTION METHOD
Critical	None defined				
Major					
101	Moisture present on assembly		0.65%	3.3	Visual
102	Moisture protection missing		0.65%	3.3	Visual
103	Solder workmanship poor		0.65%	3.3	Visual
104	Part missing		0.65%	3.3	Visual
105	Assembly damaged		0.65%	3.3	Visual
Minor					
201	Part incorrectly assembled (including wiring)		1.50%	3.3	Visual
202	Marking misleading, unidentifiable or missing		1.50%	3.3	Visual
203	Compound on prohibited surfaces		1.50%	3.3	Visual
204.	Poor workmanship		2.50%	3.9	Visual

NOTES:

CLASSIFICATION OF DEFECTS & TESTS

PARAGRAPH	TITLE		SHEET 1 OF 1		DRAWING NUMBER 11830798
4.5.2.7	Component Assembly, Depression Limit				NEXT HIGHER ASSEMBLY 11830922
CATEGORY	EXAMINATION OR TEST	NO. OF SAMPLE UNITS	AQL OR 100%	REQUIREMENT PARAGRAPH	PARAGRAPH REFERENCE /INSPECTION METHOD
Critical	None defined				
Major					
101	Moisture present on assembly		0.65%	3.3	Visual
102	Moisture protection missing		0.65%	3.3	Visual
103	Solder workmanship poor		0.65%	3.3	Visual
104	Part missing		0.65%	3.3	Visual
105	Assembly damaged		0.65%	3.3	Visual
Minor					
201	Marking misleading, unidentifiable or missing		1.50%	3.3	Visual
202	Fillet missing		1.50%	3.3	Visual
203	Compound on prohibited area		1.50%	3.3	Visual
204	Poor workmanship		2.50%	3.9	Visual

NOTES:

4.6.2.1 Temperature. A high temperature test shall be performed in accordance with MIL-STD-810, Method 501.1. Procedure H, and a low temperature test shall be performed in accordance with MIL-STD-810, Method 502.1, Procedure I. The minimum temperature during the low temperature test shall be -65°F, and the maximum temperature during the high temperature test shall be +160°C.

4.6.2.2 Altitude. A low pressure altitude test shaLl be performed in accordance with MIL-STD-810, Method 500.1, Procedure I.

4.6.2.3 Temperature - altitude combination. A temperature - altitude test shall be performed in accordance with MIL-STD-810C, Method 504.1, Procedure I and equipment category 5.

4.6.2.4 Humidity. A humidity test shall be performed in accordance with MIL-STD-810, 507.1, Procedure I.

4.6.2.5 Vibration. A vibration test shall be performed in accordance with MIL-STD-810, Method 514.2, Procedure I, Equipment Category C, except use 0.3 inch double Amplitude from 5 to 40 cps or ±3 g acceleration, whichever is less, and use 0.036 inch double amplitude from 40 cps to 73 cps and ±10 g from 73 Cps to 500 Cps.

4.6.2.6 Shock. A shock test shall be performed in accordance with MIL-STD-810, Method 516.2, Procedure I.

4.6.2.7 Sand and dust. A dust test shall be performed in accordance with MIL-STD-810, Method 510.1, Procedure I.

4.6.2.8 Fungus. A fungus test shall be performed in accordance with MIL-STD-810, 508.1, Procedure I.

4.6.2.9 Salt spray test. Samples shall be selected from each protective o finished lot and subject to the salt spray test in accordance with the procedures specified-in ASTM B 117. Unless otherwise specified on the applicable drawing, the minimum exposure time shall be one and one half (1 1/2) hours using a 5% sodium chloride solution. Rejection shall be in accordance with the applicable protective finish specification.

4.6.3 Electronic performance inspection methods and procedures. The logic control assembly shall be tested for compliance with specified electronic, test points, feed-through winding, power outputs, input/output relationships, adjustments, fire voltage output load, and power supply fail safe. Any assembly which fails to comply with the specified performance characteristic requirements or evidences degradation of its operational performance shall be classed defective. Test equipment and procedures shall be satisfactory to the contracting officer.

4.6.3.1 Inspection conditions. Unless otherwise specified, the performance requirements specified for the LCU, Drawing 11830922, shall be verified using the following test conditions:

a. Input power as specified in the requirement for electrical power supply.

b. Temperature of 70° + 20°F.

c. Measurements will be made using approved functional inspection equipment and/or standard commercial measuring equipment (see 4.5.4).

Note: Details such as inputs/outputs, signal levels, pin connections, etc., for the tests specified below are in the referenced Section 3 paragraph. This information is a pertinent part of each test specified.

4.6.3.2 SCAS circuit. Verify that the outputs defined in the specified requirement of the SCAS circuit occur when the specified inputs are supplied.

4.6.3.3 SCAS command signal input. With Items a and b present as specified below, verify the output defined in the specified requirement of the SCAS Command signal input.

a. Fire volts pulse train — Input at Pin J2-Z
Amplitude: 28 V
Pulse duration: 2 ms
Pulse period: 82 ms

b. Interlocked trigger signal Input at Pin J2-r: 0 Vdc (Ground)

4.6.3.4 SCAS output time delays. Using the fire volts pulse and the interlocked trigger signal, verify that the SCAS output time delays at Pin J2-X are as specified in the specified requirement of the SCAS output time delays.

4.6.3.5 SCAS circuitry with low frequency pulse input. Increase the time period between the fire volts pulse input In accordance with the specified requirement for the SCAS circuitry with low frequency pulse input and verify the specified output voltage change at Pin J2-X.

4.6.3.6 Depression limit circuit, no-limit mode. Using the inputs defined in the specified requirement for depression limit circuit, no-limit mode, verify the specified output voltages at Pin JI-D.

4.6.3.7 Depression limit circuit, limit mode. Using the inputs defined in the specified requirement for depression limit circuit, limit mode, verify the specified output voltages at Pin JI-D.

4.6.3.8 One and one-half degree azimuth error detector. Using the initial conditions defined In the specified requirement of one and one-half degree azimuth eror detector and with the inputs of output for azimuth error detector and output of J1-L applied, verify the specified output voltages at Pin JI-L.

4.6.3.9 One and one-half degree elevation error detector. Using the inputs defined in the specified requirement of one and one-half degree elevation error detector, verify the specified output voltages at Pin J1-M.

4.6.3.10 Gunner Q-signal, in-phase. Using the initial conditions of the specified requirements for coincidence sensor component assembly and with the inputs fo the gunner Q-signal, in-phase applied, verify the outputs specified in a, b, and c of the gunner Q-signal, in-phase.

4.6.3.11 Gunner Q-signal, in-phase and low voltage. Using the initial conditions of the specified requirements for coincidence sensor component assembly and with the input at Pin J1-A in accordance with the gunner Q-signal, in-phase and low voltage, verify the outputs specified in a, b, and c of the gunner Q-signal, in-phase and low voltage.

4.6.3.12 Gunner Q-signal, out-of-phase. Using the initial conditions of the specified requirements for coincidence sensor component assembly and the input at Pin J1-A in accordance with the gunner Q-signal, out-of-phase, verify the outputs specified in a, b, c, and d of the gunner Q-signal, out-of-phase.

4.6.3.13 Pilot Q-signal. Using the initial conditions of the specified requirements for coincidence sensor component assembly and with the inputs defined in the specified requirements of pilot Q-signal applied, verify the characteristics specified in the gunner Q-signal, in-phase; in phase and low voltage and out-of-phase.

4.6.3.14 TSU Q-signal. Using the initial conditions of the specified requirements for coincidence sensor component assembly and with the inputs defined in the specified requirements of the TSU Q-signal applied, verify the characteristics specified in 4.6.3.13.

4.6.3.15 Tow mode. Using the initial conditions of the specified requirements for coincidence sensor component assembly and with the inputs defined in the specified requirements for the tow mode applied, verify the characteristics specified in 4.6.3.13.

4.6.3.16 Low voltage on +18 V supplies. Using the initial conditions of the specified requirements coincidence sensor component assembly and with the inputs defined in the specified requirement of low voltage on ±18V supplies applied, verify the specified output voltage change at Pin J1-L.

4.6.3.17 V_x in-phase. Using the conditions and inputs defined in the specified requirements for coincidence sensor component assembly, fixed forward mode and V_x in-phase, verify the outputs specified in the gunner requirement of Q-signal, in-phase.

4.6.3.18 Vxsignal, in-phase and low voltage. Using the conditions and inputs defined in the specified requirements for coincidence sensor component assembly, fixed forward mode, and the V_x signal, in-phase and low voltage, verify the outputs specified in a and b of this last requirement.

4.6.3.19 Vxout-of-phase. Using the conditions and inputs defined in the specified requirements for coincidence sensor component assembly, fixed forward mode, and V_x out-of-phase, verify that the outputs specified in the requirements of gunner Q-signal, out-of-phase occur during the out-of-phase condition.

4.6.3.20 Low voltage on + 18 V supplies. Using the conditions and inputs defined in the specified requirements for coincidence sensor component assembly, fixed forward mode, and low voltage on ±18V supplies, verify that the output voltage at Pin J1-L does not change.

4.6.3.21 Elapsed time meter. Verify that the elapsed time meter advances one hour when the power to the LCU has been applied for one hour.

3.6.3.22 Workmanship. The requirements of workmanship shall be verified by continuous inspection of all parts and assemblies to assure conformance to high quality workmanship.

4.7 Interchangeability testing. Any assembly which fails to comply with the specified requirements or evidences degradation of its operational performance shall be classed defective. Test equipment and procedures shall be satisfactory to the contracting officer (see 4.564).

4.7.1 Logic control assembly. A sample of three control assemblies rondomly selected, shall be tested for interchangeability using the test method specified in 4.7.3. Control assemblies taken for interchangeability testing shall have been found satisfactory in all other examinations and tests. The three control assemblies shall comply with the applicable specification functioning requirements of 4.6.3 before and after the interchange of parts. It shall be the responsibility of the agency responsible for the test to inform the contracting officer by letter or other methods satisfactory to the contracting officer, when selective assembly has become necessary. Statement shall contain, as a minimum, contractor's name and FSCM, contract number, parts involved in the selective fit, conditions of parts and tationale for action taken. No hand refinement of parts shall be permissible without approval by the contracting officer. No malfunctions shall be allowed in the functioning tests. Failure of a control assembly in the interchangeability test shall cause retest or rejection of the first article.

At the discretion of the Government representative, an interchangeability retest may be allowed. Failure during the retest shall cause rejection of the first article. A sample of six control assemblies from each retest shall be tested using the same procedures described above.

4.7.2 Repair parts. At least two parts of concurrent repair parts shall be subjected to the interchangeability test specified in 4.7.3. Failure of any part to meet the interchangeability requirements shall be cause for rejection, subject to reconditioning and further test. A sample consisting of double the number of parts used in the original test shall be tested using the test methods specified above.

4.7.3 Test method of interchangeability. Control assemblies shall be tested by disassembling and then reassembling the parts specified below. Parts shall be disassembled from the control and identical parts placed together and mixed. Any commercial part (screws, pins, etc.) rendered unserviceable by disassembly shall be replaced without penalty to the interchangeability test.

List of Interchangeable Parts

Component	Drawing
Logic Control Unit Assembly	11830922
Component Assembly, Power Supply and Clearing	11830441
Component Assembly, Torque Command	11830988
Case, Logic Control Unit	11830531
Component Assembly, Coincidence Sensor	11830724
Component Assembly, Interconnection	11830797
Component Assembly, Depression Limit	11830798

4.7.4 Repair parts. Concurrent repair parts shall be tested by disassembling two control assemblies previously tested in 4.7.3 and then reassembling them using the concurrent repair parts. No hand refinement of parts will be allowed, and the assembled control assemblies shall operate and function as intened. This test may be performed independently of the control assembly interchangeability testing specified in 4.7.1 and at more frequent intervals using accepted drive assemblies taken from current production.

4.8 Proof test (first article inspection only). When specified in the contract (see 6.2) three Logic Control Unit Assemblies shall be forwarded to the site specified by the contracting agency and assembled to an accepted Universal Turret Subsystem (UTS). The Logic Control Unit Assemblies shall function in accordance to the intent of the design and with no evidence of malfunction. When approved by the contracting agency, this test may be performed at the aircraft system level.

5. PACKAGING

5.1 Preservation, packaging, packing and marking. The logic control assemblies shall be prepared, packaged, packed and marked in accordance with the requirements of the Preservation and Packaging Data for Drawing P11830922 for the level of protection specified in the contract. (See 6.2.)

5.1.1 Spare parts or replacement parts. Spare parts or replacement parts shall be cleaned, perserved, packaged and packed as specified in the contract or order.

6. NOTES

6.1 Intended use. The logic control assembly covered by this specification is intended for use with gun, automatic, 20mm: M197 on Armament Subsystem, Helicopter, 20mn, M97E1 and M97E2.

6.2 Ordering data. Procurement documents shall specify the following:

6.2.1 Acquisition requirements.

a. Title, number and date of this specification.

b. Quantity required and delivery schedules.

c. Serialization requirements, if applicable.

d. Quality Conformance Inspection, if other than specified in Section 4 of this specification.

e. First Article sample requirements, if other than specified in Section 4 of this specification.

f. Packaging requirements, if other than specified in Section 5 of this specification.

g. Certified test reports and certificates of conformance for each lot or shipment of product.

6.2.2 Contract data requirements. Contract data requirements for inspection equipment design shall conform to Data Item Description DI-R-1714, Tailored.

6.3 Submission of inspection equipment design for approval. See MIL-w-63150 equipment designs shall be submitted as required to: Commander, ARRADCOM, ATTN: DRDAR-QAF-1, Dover, NJ 07801. Request letter of submittal should state contractor, contract number, specification number, item nomenclature, and classification of defects and test paragraphs.

6.4 Submission of results of contractor-conducted examinations and tests. Unless otherwise specified by the Contracting Officer, the contractor shall forward requested records of examinations or tests to: Commander, ARRADCOM, ATTN: DRDAR-QAF-S, Dover, NJ 07801.

Custodian:
Army-AR

Preparing activity:
Army-AR

Project 1005-A617

STANDARDIZATION DOCUMENT IMPROVEMENT PROPOSAL

INSTRUCTIONS: This form is provided to solicit beneficial comments which may improve this document and enhance its use. DoD contractors, government activities, manufacturers, vendors, or other prospective users of the document are invited to submit comments to the government. Fold on lines on reverse side, staple in corner, and send to preparing activity. Attach any pertinent data which may be of use in improving this document. If there are additional papers, attach to form and place both in an envelope addressed to preparing activity. A response will be provided to the submitter, when name and address is provided, within 30 days indicating that the 1426 was received and when any appropriate action on it will be completed.

NOTE: This form shall not be used to submit requests for waivers, deviations or clarification of specification requirements on current contracts. Comments submitted on this form do not constitute or imply authorization to waive any portion of the referenced document(s) or to amend contractual requirements.

DOCUMENT IDENTIFIER *(Number)* AND TITLE

MIL-T-63536 (AR) TURRET SUBSYSTEM

NAME OF ORGANIZATION AND ADDRESS OF SUBMITTER

☐ VENDOR ☐ USER ☐ MANUFACTURER

1. ☐ HAS ANY PART OF THE DOCUMENT CREATED PROBLEMS OR REQUIRED INTERPRETATION IN PROCUREMENT USE? ☐ IS ANY PART OF IT TOO RIGID, RESTRICTIVE, LOOSE OR AMBIGUOUS? PLEASE EXPLAIN BELOW.

A. GIVE PARAGRAPH NUMBER AND WORDING

B. RECOMMENDED WORDING CHANGE

C. REASON FOR RECOMMENDED CHANGE(S)

2. REMARKS

SUBMITTED BY *(Printed or typed name and address — Optional)*

TELEPHONE NO.

DATE

DD FORM 1 OCT 76 1426

EDITION OF 1 JAN 72 WILL BE USED UNTIL EXHAUSTED.

FOLD

DEPARTMENT OF THE ARMY

OFFICIAL BUSINESS
PENALTY FOR PRIVATE USE $300

NO POSTAGE NECESSARY IF MAILED IN THE UNITED STATES

BUSINESS REPLY CARD

FIRST CLASS PERMIT NO. 12062 WASHINGTON D. C.

POSTAGE WILL BE PAID BY THE DEPARTMENT OF THE ARMY

Commander
US ARMY ARMAMENT RESEARCH & DEVELOPMENT COMMAND
ATTN:: DRDAR-QAF
DOVER, NJ 07801

FOLD

NOTICE
OF VALIDATION

INCH-POUND

MIL-T-63536(AR)
NOTICE 1
12 October 1990

MILITARY SPECIFICATION

Turret Subsystem, Universal (UTS), For Armament Subsystem, Helicopter, 20MM, M97E1 & M97E2, Logic Control Unit Assembly For

MIL-T-63536(AR) dated, 27 Dec 1981, has been reviewed and determined to be valid for use in acquisition.

Preparing actifity:
Army - AR

ANSMC N/A FSC 1005

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.