INCH-POUND

MIL-T-48467C(AR)
01 May 1995
(see 6.4)

MILITARY SPECIFICATION

TEST SET, FIELD

This specification is approved for use by the U.S. Army Armament, Research, Development and Engineering Center (ARDEC) and is available for use by all Departments and Agencies of the Department of Defense.

1. SCOPE

1.1 Scope. This specification establishes the requirements and quality assurance provisions for the Test Set, Field, M21 Computer, 11733200.

2. APPLICABLE DOCUMENTS

2.1 Government documents.

2.1.1 Specifications, standards and handbooks. The following specifications, standards and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents shall be those listed in the issue of the Department of Defense Index of Specifications and Standards (DODISS) and supplement thereto, cited in the solicitation (see 6.2).

SPECIFICATIONS

MILITARY

MIL-F-13926 - Fire Control Materiel, General Specification Governing the Manufacture and Inspection of
MIL-I-45607 - Inspection Equipment; Acquisition, Maintenance, and Disposition of

Beneficial comments (recommendations, additions, deletions) and any pertinent data which may be of use to improving this document should be addressed to: Commander, U.S. Army ARDEC, ATTN: AMSTA-AR-EDE-S, Picatinny Arsenal, New Jersey 07806-5000 by using the Standardization Document Improvement Proposal (DD Form 1426) appearing at the end of this document or by letter.

AMSC N/A

FSC 1240

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

STANDARDS

MILITARY

MIL-STD-100	- Engineering Drawing Practices
MIL-STD-454	- Standard General Requirements for Electronic Equipment
MIL-STD-810	- Environmental Test Methods
MIL-STD-2000	- Standard Requirements for Soldered Electrical and Electronic Assemblies
MIL-STD-2073-1	- Procedures for Development and Application of Packaging Requirements

(Unless otherwise indicated, copies of federal and military specifications, standards and handbooks are available from: DODSSP - Customer service, Standardization Documents Order Desk, 700 Robbins Avenue, Bldg 4D, Philadelphia, PA 19111-5094.)

2.1.2 Other Government documents, drawings and publications. The following other Government documents, drawings and publications form a part of this document to the extent specified herein. Unless otherwise specified, the issue shall be those in effect on date of the solicitation.

U.S. Army Armament Research Development and Engineering Center (ARDEC)

DRAWINGS

11733200	- Test Set, Field

(Copies of Government drawings required by contractors in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this document and the references cited herein (except for related associated detail specifications, specification sheets or MS standards), the text of this document shall take precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained (See contract provisions for additional precedence criteria).

3. REQUIREMENTS

3.1 Fabrication. The field test set, herein referred to as the assembly, shall be manufactured in accordance with Drawing 11733200 and drawings pertaining thereto and, when assembled, shall meet the requirements of this specification.

3.1.1 Function. The assembly shall provide complete test facilities to fault isolate errors in the computer and Gunner's Control Unit (GCU).

3.1.2 General specifications. (see 4.6.3)

3.1.2.1 Manufacture and inspection. The following provisions of MIL-F-13926 apply:

a. Dimensions and tolerances
b. Effect of protective coating on dimensions (Inorganic type coatings)
c. Part identification and marking
d. Workmanship (including applicable portions of MIL-STD-2000 and MIL-STD-454, Requirement 9)

3.1.2.2 Standards of Manufacture.

3.1.2.2.1 Assembly and Soldering. The requirements of MIL-STD-2000 shall apply, as a minimum.

3.1.2.2.2 Interchangeability. The assembly shall be manufactured in accordance with interchangeability requirements as specified in MIL-STD-100.

3.1.3 Ambient conditions. Standard ambient conditions shall be as follows:

a.	Temperature	73° ± 18°F
b.	Relative humidity	50 percent ±30 percent
c.	Atmospheric pressure	28.5 + 2.0 −3.0 in. Hg.

3.2 First article. When specified in the contract or purchase order (see 6.2), the contractor shall furnish sample units for first article inspection and approval (see 4.4).

3.3 Performance. Unless otherwise specified, the assembly shall meet the performance requirements specified herein under standard ambient conditions of 3.1.3.

a.	Input power and signals	See Table I
b.	Loads	See Figure 1

TABLE I. Input power and signals.

Item	Parameter	Characteristics	Connection	Return
1.0	INPUT POWER			
1.1	24V dc ±2.4V dc	Ripple contents 200 mv max Supply: 5 amps min	J6-A	J6-B and J6-C
2.0	SIGNALS 1/			
2.1	5.000 ±0.002 V rms	400 Hz ±1 Hz phase 1 (Ph 1)	J1-52	J1-50
2.2	Variable V rms	From 0 to 3.000V rms 400 ±1 Hz Ph 1	J1-17	J1-50
2.3	Variable dc	From +1.6 to +2.4V dc	J4-44 with J1-48 J1-56 J1-60 and J1-64 Jumpered to J4-44	J1-50
2.4	Variable dc	From +11.5 to +13.5V dc	J3-78	J1-50
2.5	Variable dc	From -9.7 to -10.3V dc	J4-41	J1-50
2.6	Variable V rms	From 0 to 4.000V rms 400 ± 1 Hz Ph 2	J4-2	J1-50
2.7	Variable V rms	0 to 3.000V rms 400 ± 1 Hz Ph 2	J4-3	J1-50
2.8	Variable V rms	0 to 3.000V rms 400 ± 1 Hz Ph 2	J4-33	J1-50
2.9	Variable V rms	0 to 4.000V rms 400 ± 1 Hz Ph 2	J4-36	J1-50
2.10	Variable V rms	0 to 3.000V rms 400 ± 1 Hz Ph 1	J4-4	J1-50
2.11	Variable V rms	0 to 3.000V rms 400 ± 1 Hz Ph 1	J4-5	J1-50
2.12	Variable V rms	0 to 10.0V rms 400 ± 1 Hz Ph 1 or Ph 2	J3-79	J1-50
2.13	Variable V dc	15.0 to -15.0V dc	J3-80	J1-50
2.14	Variable V dc	15.0 to -15.0V dc	J3-81	J1-50
2.15	Variable V rms	0 to 7.000V rms 400 Hz ± 1 Hz Ph 1 or Ph 2	J3-34	J3-40
2.16	Variable V rms	0 to 10.000V rms 400 Hz ± 1 Hz Ph 1	J3-36	J3-40
2.17	Variable V rms	0 to 7.000V rms 400 Hz ± 1 Hz Ph 1 or Ph 2	J3-63	J3-40

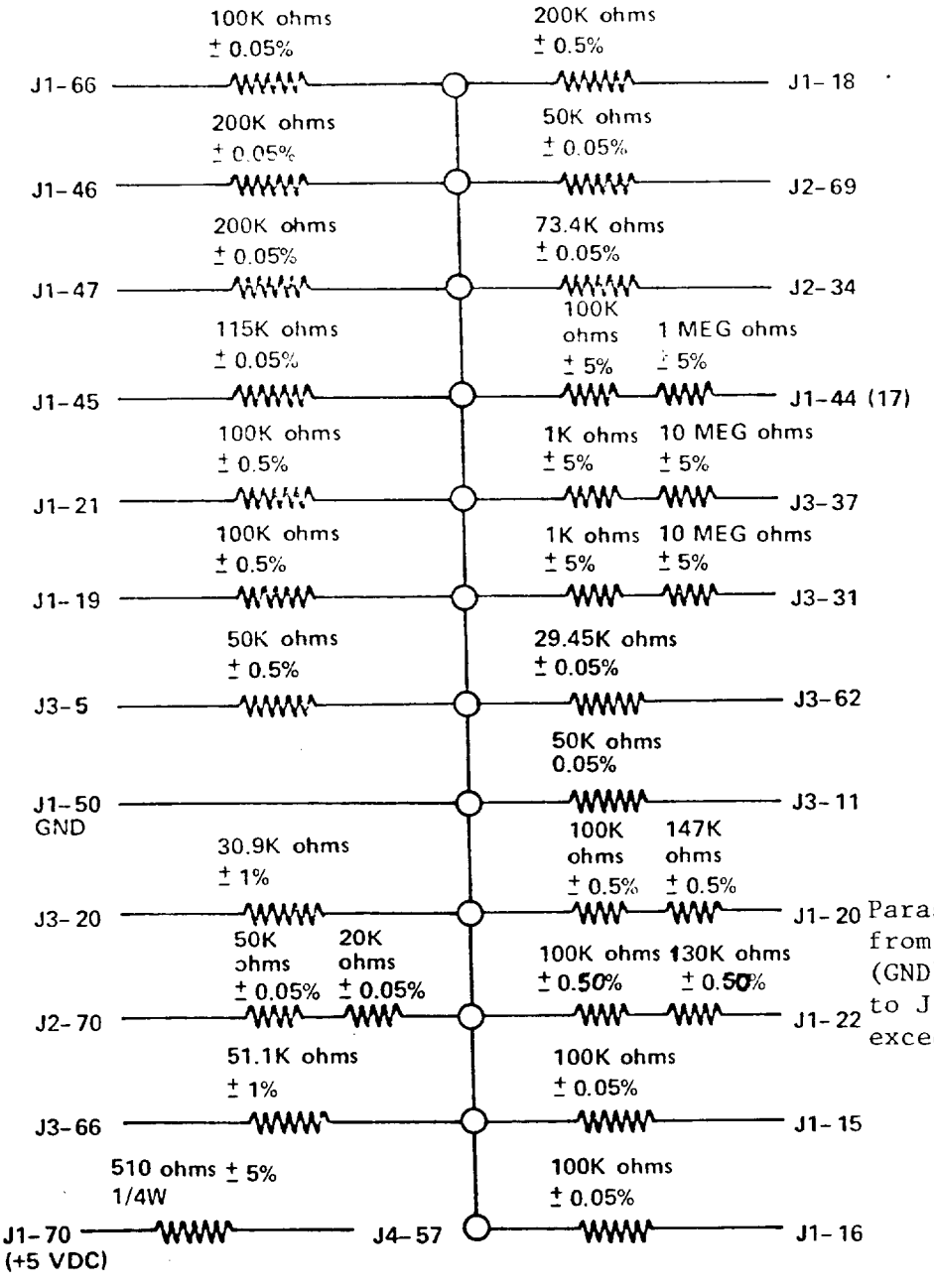
TABLE I. Input power and signals. - Continued

Item	Parameter	Characteristics	Connection	Return
2.18	Variable V rms	0 to 10.000V rms 400 Hz ± 1 Hz Ph 1 or Ph 2	J3-64	J3-40
2.19	Variable V dc	12.0 to -12.0V dc	J3-17	J3-41
2.20	Variable V dc	12.0 to -12.0V dc	J3-18	J3-41
2.21	Variable V rms	0 to 3.000V rms 400 ± 1 Hz Ph 1	J3-7	J1-50
2.22	Variable V rms	0 to 3.000V rms 400 ± 1 Hz Ph 1	J3-1	J1-50
2.23	Variable V rms	0 to 3.000V rms 400 ± 1 Hz Ph 1	J4-69	J1-50
2.24	Variable dc	-5.000 to 5.000V dc	J4-21	J1-50
2.25	-15.000V dc (Logic 0 Level)	-15.000 ± 0.030V dc applied through a 51K ±5% ohm, 1/8W resistor	J1-23, 24, 34, 35 J4-19 and as specified	J1-50
2.26	Variable V rms	0 to 5.000V rms 400 Hz ± 1 Hz Ph 1	Vin (Figure 3)	J3-40 or J1-50
2.27	Variable V rms	0 to 5.000V rms 400 Hz ± 1 Hz Ph 2	Vin (Figure 3)	J3-40 or J1-50
2.28	Variable V rms	0 to 5.000V rms 400 Hz ± 1 Hz Ph 1	Vin (Figure 3)	J3-40 or J1-50
2.29	Variable V rms	0 to 5.000V rms 400 Hz ± 1 Hz Ph 2	Vin (Figure 3)	J3-40 or J1-50
2.30	Variable dc	-15.00 to 15.00V dc	J5-18, 20, 22, 44	J1-50
2.31	Variable dc	-1.00 to 1.00V dc	J5-15, 16, 46, 47	J1-50
2.32	Variable dc	-10.00 to 10.00	J5-45	J1-50
2.33	Variable dc	-2.000 to 2.000V dc	Vin (Figure 4)	J1-50 or J3-40
2.34	±15.00V dc Square wave	±0.5V dc 400 Hz ±1 Hz Ph 1	MR1 (Figure 4)	J1-50
2.35	Variable dc	0 to +12.00V dc	J5-2, 4, 19, 21, 65, 81, 85	J1-50
2.36	Variable dc	0 to +2.000V dc	J5-66	J1-50
2.37	-15.000V dc	±0.030V dc	J1-57, J3-59, J2-50, 68	J1-50
2.38	15.000V dc	±0.030V dc	J1-49, J2-7, 8, 56, J3-58 and applied as specified	J1-50
2.39	5.000V dc	±0.030V dc	J1-70, J3-60, J2-75	J1-50

TABLE I. Input power and signals. - Continued

Item	Parameter	Characteristics	Connection	Return
2.40	24.000V dc	±0.050V dc	J1-72, J2-24, J3-25	J1-50
2.41	Variable dc	0 to -2.000V dc	J2-67	J1-50
2.42	5.000 ±0.005 V rms	400 ± 1 Hz, Ph 1	J1-53, J3-21, 43, 57	J1-50
2.43	5.000 ±0.005 V rms	400 ± 1 Hz, Ph 2	J3-22, 44, 67	J1-50
2.44	115.0 V rms	±11.5V rms, 400 ± 1 Hz	J3-33	J1-50
2.45	Variable V rms	0 to 5.000V rms 400 ± 1 Hz Ph 1 or Ph 2	J1-54	J1-50
2.46	Variable V rms	0 to 5.000V rms 400 ± 1 Hz Ph 1 or Ph 2	J4-67	J1-50
2.47	Logic Gnd (Logic 0 Level)	0.20 ± 0.20V dc	Applied as Specified	J1-50
2.48	+5V Logic (Logic 1 Level)	3.40 ± 1.40V dc	Applied as Specified	J1-50
2.49	Ground (Logic 1 Level)	0.000 ± 0.030V dc	Applied as Specified	J1-50
2.50	-15.000V dc (Logic 0 Level)	-15.000 ± 0.030V dc applied through a 20K ohm ±5% 1/8W resistor	Applied as Specified	J1-50

1/ The item 2.1 signal source is the input reference, Ph 1. All other signal sources designated Ph 1 are "in-phase" with the item 2.1 voltage. All signal sources designated Ph 2 are 180 degrees "out-of-phase" with the item 2.1 voltage.



Parasitic capacitance from J1-20 to J1-50 (GND) or from J1-22 to J1-50 shall not exceed 1000 pF.

FIGURE 1. Electrical Loads.

3.3.1 Continuity. With no power or signals applied, direct continuity (resistance equal to 1.0 ohm or less) shall exist between connector pins specified in Table II (see 4.6.1.1).

TABLE II. Continuity requirements.

Item	From	To	Item	From	To
1	J1-01	J1-02	19	J1-50	J1-59
		J1-03	(Cont.)	"	J1-61
2	J1-05	J1-06		"	J1-83
		J1-67			J2-1
		J1-68			J2-13
3	J1-64	J1-65			J2-33
4	J1-15	J1-46			J2-38
5	J1-16	J1-47			J2-83
6	J2-43	J2-57			J3-2
7	J3-07	J3-09			J3-4
8	J3-01	J3-03			J3-6
9	J5-01	J5-03			J3-8
		J5-60			J3-10
10	J5-17	J5-48			J3-23
11	J5-49	J5-64			J3-26
12	J5-53	J5-80			J3-40
13	J5-54	J5-84			J3-41
14	J1-4	J3-35			J3-52
15	J1-84	J3-56			J3-61
16	J1-85	J2-74			J3-83
17	J3-30	J3-38			J4-51
18	J5-7	J5-8			J4-52
		J5-9			J4-83
		J5-10			J5-5
		J5-11			J5-50
		J5-12			J5-51
		J5-13			J5-58
		J5-14			J5-59
19	J1-50	J1-51			J5-61
		J1-58			

3.3.2 Resistance. With no power, loads or signals applied, and switches set to the positions specified, perform paragraphs a and b.

a. The resistance between connector pins shall be as specified in Table III-A.

b. With the PHASE switch rotated from positions 1 through 5, the resistance shall be as specified in Table III-B.

TABLE III-A. Resistance requirements.

Item	From	To	Resistance, (Ohms)
1	J2-43, 57	J1-05	12.00 ± 0.6
2	J2-47	J2-43, 57	100K ± 1K
3	J2-47	J1-05	100K ± 1K
4	J3-17	J3-18	49.9 ± 1.0
5	J3-34	J5-1	374 ± 19
6	J3-36	J5-1	374 ± 19
7	J3-63	J5-1	374 ± 19
8	J3-64	J5-1	374 ± 19
9	J2-49	J2-52	3970 ± 2

Switch	Position
POWER	OFF
UNIT SELECT	GCU
AMMO TEST	APDS
POTENTIOMETER TEST	ALT
COMPUTER TEST SELECT	1
COMPUTER PHASE	1
CONTINUITY	OFF

TABLE III-B. Resistance requirements.

ITEM NO.	FTS PHASE SWITCH POSITIONS	RANGE (K OHMS) LOWER LIMIT	RANGE (K OHMS) UPPER LIMIT
1	1	99	101
2	2	0	0.001
3	3	99	101
4	4	0	0.001
5	5	99	101

POWER	OFF
UNIT SELECT	GCU
AMMO TEST	APDS
POTENTIOMETER TEST	ALT
COMPUTER TEST SELECT	1
CONTINUITY	OFF

3.3.3 Power, unit select, lamp test switches, and incorrect setup test. With item 1.1 of Table I connected to power connector J6; with the POWER switch set to ON and the UNIT SELECT placed in the COMPUTER position, the CONTINUITY switch set to OFF, the POWER lamp shall be illuminated (see 4.6.1.3).

a. With the LAMP TEST switch pressed, the COMPUTER TEST CARD MALFUNCTION lamps A1 through A10, COMPUTER OK, INCORRECT SETUP, and TEST IN PROGRESS shall illuminate.

b. With the UNIT SELECT switch placed in GCU position, the POWER lamp shall illuminate. With the LAMP TEST switch pressed, the GUNNERS CONTROL TEST indicators shall illuminate.

c. With the UNIT SELECT switch placed in the COMPUTER position and the TEST SELECT and PHASE switches set to the positions as indicated in Table IV, the INCORRECT SETUP indicators shall illuminate or extinguish as specified in Table IV.

d. Unless otherwise noted, the item 1.1 of Table I voltages shall be applied to the power connector J6, the loads, as specified in Figure 1 shall be applied, and the CONTINUITY switch shall be set to OFF.

TABLE IV. Incorrect setup logic.

Item	TEST SELECT Position	PHASE Position	INCORRECT SETUP Indication
1	1	1	OFF
2	2	1	OFF
3	3	1	OFF
4	4	1	OFF
5	5	1	OFF
6	6	1	ON
7	6	2	ON
8	5	2	ON
9	4	2	OFF
10	3	2	ON
11	2	2	ON
12	1	2	ON
13	1	3	ON
14	2	3	ON
15	3	3	ON
16	4	3	OFF
17	5	3	ON
18	6	3	ON
19	6	4	ON
20	5	4	ON

TABLE IV. Incorrect setup logic. (cont.)

Item	TEST SELECT Position	PHASE Position	INCORRECT SETUP Indication
21	4	4	OFF
22	3	4	ON
23	2	4	ON
24	1	4	ON
25	1	5	ON
26	2	5	ON
27	3	5	ON
28	4	5	OFF
29	5	5	ON
30	6	5	ON

3.3.4 Prime power forms. With the POWER switch set to ON, UNIT TEST set to COMPUTER, TEST SELECT and PHASE switches set to position 1, the output voltage: (see 4.6.1.4)

a. At J5-48 and J5-17 shall be plus 15.000 ± 0.030V dc (referenced to J1-50).

b. At J5-56 shall be minus 15.000 ± 0.030V dc (referenced to J1-50).

c. At J5-70 shall be plus 5.00 ± 0.05V dc (referenced to J2-13).

d. At J1-1, 2, 3 shall be plus 23.7 ± 2.4V dc (referenced to J1-05).

e. At J5-1, 3, and 60 shall be plus 23.7 ± 2.4V dc (referenced to J5-05).

f. At J5-52 shall be plus 7.071 ± 0.024V dc (referenced to J1-50).

g. At J5-55 shall be minus 7.070 ± 0.030V dc (referenced to J1-50).

3.3.5 Test initiate switch and timing signal logic. With the POWER switch set to ON, the UNIT SELECT switch set to the COMPUTER position, the TEST SELECT and PHASE switches set to 1 and the TEST INITIATIVE switch pressed and released, the TEST IN PROGRESS indicator shall illuminate for 25.6 ± 3.3 seconds and the A2 CARD MALFUNCTION indicator shall illuminate after 25.6 ± 3.3 seconds (see 4.6.1.5).

3.3.6 Reference signal characteristics. With the POWER switch set to ON, the UNIT SELECT switch set to the COMPUTER position, the TEST SELECT switch in position 1, the PHASE switch in position 2 and the signal source item 2.1 of Table I connected to J1-52: (see 4.6.1.6)

a. The output voltage measured across J1-44 shall be 1.836 ± 0.005V rms Ph 1 measured to J1-50.

b. The output voltage measured across J1-45 shall be minus 6.992 ± 0.150V dc measured to J1-50.

3.3.7 A1 and A2 card fail logic. With the POWER switch set to ON, the UNIT SELECT switch set to COMPUTER, and the TEST SELECT and PHASE switches set to position 1, a logical "0" level of item 2.47 of Table I applied to J4-57, item 2.45 of Table I adjusted to 5.000 ± 0.005V rms and applied as specified, item 2.1 of Table I adjusted to 5.000 ± 0.002V rms Ph. 1 and applied as specified, item 2.3 of Table I applied to J4-44 (with J1-48, J1-56, J1-60 and J1-64 jumpered to J4-44) and item 2.4 of Table I applied to J3-78.

a. With the variable dc input at J4-44 adjusted to +2.359 ± 0.005V dc and the variable dc input at J3-78 adjusted to +12.469 ± 0.005V dc, the A1 CARD MALFUNCTION indicator shall illuminate and all other indicators shall extinguish.

b. With the variable dc input at J3-78 adjusted to the values specified for each item of Table V, the corresponding CARD MALFUNCTION indicators shall illuminate.

c. With the input to J3-78 adjusted to +12.469 ± 0.005V dc, the input to J4-44 adjusted to +2.023 ± 0.005V dc and the logic "0" level removed from J4-57, the A2 and A4 CARD MALFUNCTION indicators shall illuminate.

d. With the variable dc input at J4-44 adjusted to the values specified for each item of Table VI, the corresponding CARD MALFUNCTION indicators shall illuminate.

TABLE V. A1 and A2 card fail logic (+13V REG comparator).

Item	Input (J3-78)	CARD MALFUNCTION Indicator
1	+11.682 ± 0.153V dc	A2
2	+11.749 ± 0.145V dc	A1
3	+13.271 ± 0.168V dc	A2
4	+13.202 ± 0.159V dc	A1

TABLE VI. A1 and A2 card fail logic (comp. power comparator).

Item	Input (J4-44, etc...)	CARD MALFUNCTION Indicator
1	+1.696 ± 0.002V dc	A1
2	+1.830 ± 0.002V dc	A2, A4
3	+2.356 ± 0.002V dc	A1
4	+2.219 ± 0.002V dc	A2, A4

3.3.8 Computer -10 volt/AC REF 2 comparator logic. With the POWER switch set to ON, the UNIT SELECT switch set to COMPUTER, the PHASE and TEST SELECT switches set to position 1 and 4 respectively, a logical "0" level of item 2.47 of Table I applied to J4-57, item 2.1 of Table I adjusted to 5.000 ± 0.002V rms Ph. 1 and applied as specified, item 2.3 of Table I adjusted to 2.023 ± 0.005V dc and applied as specified, item 2.4 of Table I adjusted to 12.469 ± 0.005V dc and applied as specified, a logical level of -15V dc, item 2.25 applied to J1-23, J1-24, J1-34 and J1-3 and items 2.5 and 2.45 of Table I applied to J4-41 and J1-54 respectively.

a. With item 2.5 of Table I adjusted to -10.000 ± 0.010V dc and item 2.45 of Table I adjusted to 5.000 ± 0.005V rms, the A4 CARD MALFUNCTION indicator shall extinguish and the A5, A7 and A9 CARD MALFUNCTION indicators shall illuminate.

b. With the variable dc input at J4-41 adjusted to the values specified for each item of Table VII, the corresponding CARD MALFUNCTION indicators shall illuminate.

c. With the variable ac input at J1-54 adjusted to the values specified for each item of Table VIII, the corresponding CARD MALFUNCTION indicators shall illuminate.

TABLE VII. Computer - 10V comparator logic.

Item	Input (J4-41)	CARD MALFUNCTION Indicator
1	- 9.751 ± 0.003V dc	A4
2	- 9.860 ± 0.003V dc	A5, A7, A9
3	-10.253 ± 0.003V dc	A4
4	-10.132 ± 0.003V dc	A5, A7, A9
5	-10.000 ± 0.010V dc	A5, A7, A9

TABLE VIII. Computer AC REF 2 comparator logic.

Item	Input (J1-23)	CARD MALFUNCTION Indicator
1	1.000 ± 0.002V dc	A4
2	5.000 ± 0.005V dc	A5, A7, A9
3	9.000 ± 0.010V dc	A4
4	5.000 ± 0.005V dc	A5, A7, A9

3.3.9 Ammo select/MT comparator logic. With the POWER switch set to ON, the UNIT SELECT switch set to COMPUTER, the PHASE switch set to position 1, item 2.1 of Table I adjusted to 5.000 ± 0.002V rms and applied as specified, item 2.3 of Table I adjusted to +2.023 ± 0.005V dc and applied as specified, item 2.4 of Table I adjusted to +12.967 ± 0.026V dc and applied as specified, item 2.45 of Table I adjusted to 5.000 ± 0.005V rms and applied as specified, item 2.5 of Table I adjusted to -10.000 ± 0.010V dc and applied as specified, and the inputs of Table IX established in any item number order, the corresponding CARD MALFUNCTION indicators shall illuminate for each position of the TEST SELECT switch specified (see 4.6.1.9).

TABLE IX. Ammo select/MT comparator logic.

Item	TEST SELECT Position	Inputs J2-14 1/	J2-15 1/	J2-16 1/	J2-17 1/	J2-18 1/	J2-19 1/	J1-23 2/	J1-24 2/	J1-34 2/	J1-35 2/	J4-19 3/	CARD MALFUNCTION Indicator
1	1	0	OPEN	OPEN	OPEN	0	OPEN	1	0	0	0	0	A5, A9
2	3	OPEN	0	OPEN	OPEN	0	OPEN	0	1	0	0	0	A5, A9
3	4	OPEN	OPEN	0	OPEN	OPEN	0	0	0	1	0	0	A5, A9
4	4	OPEN	OPEN	0	0	0	OPEN	0	0	1	0	0	A5, A7, A9
5	5	OPEN	OPEN	0PEN	0	OPEN	0	0	0	0	1	1	A5, A9
6	5	OPEN	OPEN	OPEN	0	0	0	0	0	0	1	0	A5, A7, A9
7	1	OPEN	OPEN	OPEN	OPEN	0	OPEN	1	0	0	0	0	A5, A7, A9
8	1	0	OPEN	OPEN	OPEN	0	OPEN	1	0	0	0	0	A5, A9
9	1	0	OPEN	OPEN	OPEN	0	OPEN	1	1	0	0	0	A7
10	1	0	OPEN	OPEN	OPEN	0	OPEN	1	0	1	0	0	A7
11	1	0	OPEN	OPEN	OPEN	0	OPEN	1	0	0	1	0	A7
12	3	OPEN	0	OPEN	OPEN	0	OPEN	0	1	0	1	0	A7
13	3	OPEN	0	OPEN	OPEN	0	OPEN	0	1	1	0	0	A7
14	3	OPEN	0	OPEN	OPEN	0	OPEN	0	1	0	0	0	A5, A9
15	3	OPEN	0	OPEN	OPEN	0	OPEN	1	1	0	0	0	A7
16	4	OPEN	0	OPEN	OPEN	0	OPEN	1	0	1	0	0	A7
17	4	OPEN	OPEN	0	OPEN	OPEN	0	0	1	1	0	0	A7

TABLE IX. Ammo select/MT comparator logic. (Cont.)

Item	TEST SELECT Position	Inputs J2-14 1/	J2-15 1/	J2-16 1/	J2-17 1/	J2-18 1/	J2-19 1/	J1-23 2/	J1-24 2/	J1-34 2/	J1-35 2/	J4-19 3/	CARD MALFUNCTION Indicator
18	4	OPEN	OPEN	0	OPEN	OPEN	0	0	0	1	0	0	A5, A9
19	4	OPEN	OPEN	0	OPEN	OPEN	0	0	0	1	1	0	A7
20	5	OPEN	OPEN	OPEN	O	OPEN	0	0	0	1	1	0	A7
21	5	OPEN	OPEN	OPEN	0	OPEN	0	0	1	0	1	0	A7
22	5	OPEN	OPEN	OPEN	0	OPEN	0	1	0	0	1	0	A7

1/ A "0" indicates that a logic "0" level of item 2.47 of Table I is applied and an "OPEN" indicates no connection or a high-impedance open-collector input.
2/ A "0" indicates that a logic "0" level of item 2.25 of Table I is applied and a "1" indicates that a logic "1" level of item 2.49 of Table I is applied.
3/ A "0" indicates that -15.000 ± 0.030V dc of item 2.37 of Table I is applied and a "1" indicates that +15.000 ± 0.030V dc of item 2.38 of Table I is applied through a 51K ohms ±5%, 1/8W resistor.

3.3.10 -Epsilon comparator logic. With the POWER switch set to ON, the UNIT SELECT switch set to COMPUTER, the PHASE and TEST SELECT switches set to positions 1 and 4 respectively, a logic "1" level of item 2.49 of Table I applied to J1-34, a logic "0" level of item 2.47 of Table I applied to J2-16 and J2-19, item 2.25 of Table I applied to J1-23, 24, 35 and J4-19, and the variable input voltages of Table X applied as specified: (see 4.6.1.10)

a. With the variable ac input at J4-2 adjusted as specified on Table X, the COMPUTER OK indicator shall illuminate.

b. With the variable ac input J4-2 adjusted to the values as specified for each item of Table XI, the corresponding CARD MALFUNCTION indicators shall illuminate.

TABLE X. -Epsilon comparator logic inputs.

Table I Reference	Connection	Return	Initial Voltage Adjustment
2.1	J1-52	J1-50	5.000 ± 0.005V rms, Ph 1
2.3	J4-44	J4-83	2.023 ± 0.005V dc
2.4	J3-78	J1-50	12.469 ± 0.005V dc
2.5	J4-41	J1-50	-10.000 ± 0.010V dc
2.6	J4-2	J1-50	2.333 ± 0.005V rms, Ph 2
2.7	J4-3	J1-50	2.301 ± 0.005V rms, Ph 2
2.23	J4-69	J1-50	2.218 ± 0.005V rms, Ph 1
2.24	J4-21	J1-50	4.020 ± 0.005V dc
2.45	J1-54	J1-50	5.000 ± 0.005V rms, Ph 2
2.46	J4-67	J1-50	2.335 ± 0.005V rms, Ph 2

TABLE XI. -Epsilon comparator logic.

Item	Input (J4-2)	CARD MALFUNCTION Indicator
1	2.395 ± 0.002V rms	A5
2	2.356 ± 0.002V rms	COMPUTER OK
3	2.275 ± 0.002V rms	A5
4	2.313 ± 0.002V rms	COMPUTER OK
5	2.333 ± 0.005V rms	COMPUTER OK

3.3.11 Eta comparator logic. With the input conditions established as specified in 3.3.10, and the variable ac input at J4-3 adjusted to the values as specified for each item of Table XII, the corresponding CARD MALFUNCTION indicators shall illuminate (see 4.6.1.11).

TABLE XII. Eta comparator logic.

Item	Input (J4-69)	CARD MALFUNCTION Indicator
1	2.365 ± 0.002V rms	A5
2	2.322 ± 0.002V rms	COMPUTER OK
3	2.243 ± 0.002V rms	A5
4	2.280 ± 0.002V rms	COMPUTER OK

3.3.12 $(W - K_W V_W) T_F$ comparator logic. With the same input conditions established as specified in 3.3.10, and the variable ac input at J4-3 adjusted to 2.353 ± 0.016V rms, the A5 CARD MALFUNCTION shall illuminate, and: (see 4.6.1.12)

a. With the variable ac input at J4-69 adjusted to the values as specified for each item of Table XIII, the corresponding CARD MALFUNCTION indicators shall illuminate.

b. With the variable ac inputs at J4-3 and J4-69 readjusted to 2.301 ± 0.005V rms and 2.218 ± 0.005V rms, respectively, the COMPUTER OK indicator shall illuminate.

TABLE XIII. $(W - K_W V_W) T_F$ comparator logic.

Item	Input (J4-69)	CARD MALFUNCTION Indicator
1	2.276 ± 0.002V rms	A4
2	2.238 ± 0.002V rms	A5
3	2.156 ± 0.002V rms	A4
4	2.195 ± 0.002V rms	A5

3.3.13 V_W comparator logic. With the same input conditions established as specified in 3.3.10, and the variable dc input at J4-21 adjusted to the values specified for each item of Table XIV, the corresponding CARD MALFUNCTION indicators shall illuminate (see 4.6.1.13).

TABLE XIV. V_W comparator logic.

Item	Input (J4-21)	CARD MALFUNCTION Indicator
1	+4.274 ± 0.002V dc	A9
2	+4.152 ± 0.002V dc	COMPUTER OK
3	+3.748 ± 0.002V dc	A9
4	+3.876 ± 0.002V dc	COMPUTER OK
5	+4.020 ± 0.005V dc	COMPUTER OK

3.3.14 CRS1/CRS2 comparator logic. With the same input conditions established as specified in 3.3.10: (see 4.6.1.14)

a. With a logic "0" level of item 2.47 of Table I applied to J3-76, the A8 CARD MALFUNCTION indicator shall illuminate.

b. With the variable ac inputs of items 2.21 and 2.22 of Table I applied to J3-7 and J3-1, respectively, and the input to J3-7 adjusted to 2.000 ± 0.005V rms and the input to J3-1 adjusted to 2.042 ± 0.005V rms, the A8 CARD MALFUNCTION indicator shall illuminate.

c. With the variable ac input to J3-1 adjusted to the values as specified for each item of Table XV the corresponding CARD MALFUNCTION indicators shall illuminate.

TABLE XV. CRS1/CRS2 comparator logic.

Item	Input (J3-1)	CARD MALFUNCTION Indicator
1	2.142 ± 0.002V rms	A6
2	2.101 ± 0.002V rms	A8
3	1.946 ± 0.002V rms	A6
4	1.983 ± 0.002V rms	A8

3.3.15 E FDBK/D FDBK comparator logic. With the same input conditions established as specified in 3.3.10, and a logic "1" level of item 2.48 of Table I applied to J3-76: (see 4.6.1.15)

a. When the variable ac inputs of items 2.8 and 2.9 of Table I applied to J4-33 and J4-36 and adjusted to 2.500 ± 0.005 and 3.660 ± 0.008V rms, respectively, the COMPUTER OK indicator shall illuminate.

b. With the variable ac input to J4-33 adjusted to the values as specified for each item of Table XVI, the corresponding CARD MALFUNCTION indicators shall illuminate.

c. With the variable ac input to J4-36 adjusted to the values as specified for each item of Table XVII, the corresponding CARD MALFUNCTION indicators shall illuminate.

TABLE XVI. E FDBK/D FDBK comparator logic (-E FDBK INPUT).

Item	Input (J4-33)	CARD MALFUNCTION Indicator
1	2.561 ± 0.002V rms	A6
2	2.523 ± 0.002V rms	COMPUTER OK
3	2.434 ± 0.002V rms	A6
4	2.473 ± 0.002V rms	COMPUTER OK
5	2.500 ± 0.005V rms	COMPUTER OK

TABLE XVII. E FDBK/D FDBK comparator logic (D FDBK INPUT).

Item	Input (J4-36)	CARD MALFUNCTION Indicator
1	3.758 ± 0.002V rms	A6
2	3.698 ± 0.002V rms	COMPUTER OK
3	3.569 ± 0.002V rms	A6
4	3.627 ± 0.002V rms	COMPUTER OK

3.3.16 D PWR AMP/E PWR AMP 1/E PWR AMP 2 comparator logic. With the same input conditions established as specified in 3.3.10, item 2.8 of Table I adjusted to 2.500 ± 0.005V rms and applied as specified, and items 2.12, 2.13 and 2.14 of Table I applied to J3-79, 80 and 81, respectively: (see 4.6.1.16)

a. With the variable ac input to J3-79 adjusted at 0.000 ± 0.005V rms and the variable dc inputs to J3-80 and 81 adjusted to 0.000 ± 0.005V dc, the A6 CARD MALFUNCTION indicator shall illuminate.

b. With the variable dc input to J3-80 adjusted to the values specified for each item of Table XVIII the corresponding CARD MALFUNCTION indicator shall illuminate.

c. With the variable dc input to J3-81 adjusted to the values as specified for each item of Table XIX, the corresponding CARD MALFUNCTION indicators shall illuminate.

d. With the variable ac input to J3-79 adjusted to the values specified in Table XX, the corresponding CARD MALFUNCTION indicators shall illuminate.

TABLE XVIII. E PWR AMP 1 comparator logic.

Item	Input (J3-80)	CARD MALFUNCTION Indicator
1	+14.218 ± 0.003V dc	A3, A6
2	+10.748 ± 0.003V dc	A6
3	-13.416 ± 0.003V dc	A3, A6
4	-10.689 ± 0.003V dc	A6
5	+ 0.000 ± 0.005V dc	A6

TABLE XIX. E PWR AMP 2 comparator logic.

Item	Input (J3-81)	CARD MALFUNCTION Indicator
1	+13.426 ± 0.003V dc	A3, A6
2	+10.679 ± 0.003V dc	A6
3	-14.208 ± 0.003V dc	A3, A6
4	-10.758 ± 0.003V dc	A6
5	+ 0.000 ± 0.005V dc	A6

TABLE XX. D PWR AMP comparator logic.

Item	Input 1/ (J3-79)	CARD MALFUNCTION Indicator
1	+10.031 ± 0.003V rms	A3, A6
2	+ 7.720 ± 0.003V rms	A6
3	- 9.491 ± 0.003V rms	A3, A6
4	- 7.662 ± 0.003V rms	A6
5	+ 0.000 ± 0.005V rms	A6

1/ A plus (+) sign indicates that the ac input is in-phase with AC REF 1 and a negative (-) sign indicates in-phase with AC REF 2.

3.3.17 E/-D comparator logic. With the input conditions established as specified in 3.3.10, item 2.8 of Table I adjusted to 2.500 ± 0.005V rms and applied as specified, item 2.13 of Table I adjusted to +14.152 ± 0.014V dc and applied as specified, and items 2.10 and 2.11 of Table I applied to J4-4 and J4-5, respectively: (see 4.6.1.17)

a. With the variable ac inputs to J4-4 and 5 adjusted to 2.514 ± 0.005V rms at the A3 and A6 CARD MALFUNCTION indicators shall illuminate.

b. With the variable ac input to J4-4 and 5 adjusted to the values specified for each item in Table XXI, the corresponding CARD MALFUNCTION indicators shall illuminate.

c. With the variable ac input to J4-5 adjusted to the values specified for each item in Table XXII, the corresponding CARD MALFUNCTION indicators shall illuminate.

d. With the variable ac inputs to J4-4 and 5 adjusted to 0.000 ± 0.005V rms the A3 and A6 CARD MALFUNCTION indicators shall illuminate.

TABLE XXI. E comparator logic.

Item	Input (J4-4)	CARD MALFUNCTION Indicator
1	2.575 ± 0.002V rms	A6
2	2.539 ± 0.002V rms	A3, A6
3	2.449 ± 0.002V rms	A6
4	2.486 ± 0.002V rms	A3, A6
5	2.514 ± 0.005V rms	A3, A6

TABLE XXII. -D comparator logic.

Item	Input (J4-5)	CARD MALFUNCTION Indicator
1	2.579 ± 0.002V rms	A6
2	2.541 ± 0.002V rms	A3, A6
3	2.453 ± 0.002V rms	A6
4	2.490 ± 0.002V rms	A3, A6
5	2.514 ± 0.005V rms	A3, A6

3.3.18 System units OK logic. With the input conditions established as specified in 3.3.10, the COMPUTER OK indicator shall illuminate and with the input conditions of Table XXIII established, in any item order, the corresponding CARD MALFUNCTION indicator shall illuminate (see 4.6.1.18).

TABLE XXIII. System units OK logic.

Item	Inputs 1/								CARD MALFUNCTION Indicator
	J1-7	J1-8	J1-9	J1-10	J1-11	J1-12	J1-63	J4-57	
1	0	0	-	-	-	-	-	0	A8
2	0	-	0	-	-	-	-	0	A8
3	0	-	-	0	-	-	-	0	A8
4	0	-	-	-	0	-	-	0	A8
5	0	-	-	-	-	0	-	0	A8
6	0	-	-	-	-	-	0	0	A8
7	0	-	-	-	-	-	-	0	COMPUTER OK
8	-	-	-	-	-	-	-	0	COMPUTER OK

1/ A "0" indicates that the logic "0" level of item 2.47 of Table I is applied and the "-" indicates that the input is open circuited or a high-impedance open-collector type input.

3.3.19 OUM1/OUM2 comparator logic. With the input conditions established as specified in 3.3.10, item 2.8 of Table I adjusted to 2.500 ± 0.005V rms and applied as specified, item 2.13 of Table I adjusted to +14.152 ± 0.014V dc and applied as specified, and items 2.12, 2.19 and 2.10 of Table I applied to J3-79, J3-17 and J3-18, respectively (see 4.6.1.19).

a. With the variable ac input to J3-79 adjusted to 0.000 ± 0.050V rms and the variable dc inputs to J3-17 and J3-18 and adjusted to 0.000 ± 0.050V dc, the A3 and A6 CARD MALFUNCTION indicators shall illuminate.

b. With the variable dc input to J3-17 adjusted to the values specified for each item in Table XXIV, the corresponding CARD MALFUNCTION indicators shall illuminate.

c. With the variable dc input to J3-18 adjusted to the values specified for each item in Table XXV, the corresponding CARD MALFUNCTION indicators shall illuminate.

d. With the variable ac input to J3-79 adjusted to 9,990 ± 0.010V rms in-phase with AC Ref 1, the A6 CARD MALFUNCTION indicator shall extinguish and the A3 shall illuminate.

e. With the variable dc input to J3-18 adjusted to +10.686 ± 0.010V dc, the A3 and A6 CARD MALFUNCTION indicators shall illuminate.

f. With the variable ac input to J3-79 adjusted to 0.000 ± 0.005V rms and the variable dc input to J3-18 adjusted to 0.000 ± 0.005V dc, the A3 and A6 CARD MALFUNCTION indicators shall illuminate.

TABLE XXIV. OUM1 comparator logic.

Item	Input (J3-17)	CARD MALFUNCTION Indicator
1	+10.786 ± 0.003V dc	A6
2	+ 8.575 ± 0.003V dc	A3, A6
3	-11.412 ± 0.003V dc	A6
4	- 8.641 ± 0.003V dc	A3, A6
5	+ 0.000 ± 0.050V dc	A3, A6

TABLE XXV. OUM2 comparator logic.

Item	Input (J3-18)	CARD MALFUNCTION Indicator
1	+10.786 ± 0.003V dc	A6
2	+ 8.575 ± 0.003V dc	A3, A6
3	-11.412 ± 0.003V dc	A6
4	- 8.641 ± 0.003V dc	A3, A6
5	+ 0.000 ± 0.050V dc	A3, A6

3.3.20 DMTR1/DMTR2 comparator logic. With the input conditions established as specified in 3.3.10, item 2.8 of Table I adjusted to 2.500 ± 0.005V rms and applied as specified, item 2.12 of Table I adjusted to 9.990 ± 0.010V rms in phase with AC Ref 1 and applied as specified, item 2.13 of Table I adjusted to 0.000 ± 0.005V dc and applied to J3-80, and items 2.14, 2.15 and 2.16 of Table I applied to J3-81, 34, and 36, respectively: (see 4.6.1.20)

a. With the variable dc input to J3-81 adjusted to 0.000 ± 0.005V dc and the variable ac input to J3-34 and 36 adjusted to 0.000 ± 0.005V rms, the A3 and A6 CARD MALFUNCTION indicators shall illuminate.

b. With the input to J3-81 adjusted to +13.302 ± 0.010V dc, the A6 CARD MALFUNCTION indicator shall extinguish and the A3 shall illuminate.

c. With the input to J3-81 to 0.000 ± 0.005V dc, the A3 and A6 CARD MALFUNCTION indicators shall illuminate.

d. With the variable ac input to J3-34 adjusted to the values specified for each item of Table XXVI, the corresponding CARD MALFUNCTION indicators shall illuminate.

e. With the variable ac input to J3-36 adjusted to 9.400 ± 0.010V rms in-phase with AC Ref 1, the A6 CARD MALFUNCTION indicator shall illuminate and the A3 shall extinguish.

f. With the input to J3-36 adjusted to 0.000 ± 0.005V rms, the A3 and A6 CARD MALFUNCTION indicators shall illuminate.

g. With the input to J3-34 adjusted to 6.743 ± 0.003V rms, in-phase with AC Ref and the input to J3-81 adjusted to +13.002 ± 0.010V dc, the A3 and A6 CARD MALFUNCTION indicators shall illuminate.

h. With the input to J3-81 and J3-34 adjusted to 0.000 ± 0.005V rms, respectively, the A3 and A6 CARD MALFUNCTION indicators shall illuminate.

TABLE XXVI. DMTR1 comparator logic.

Item	Input 1/ (J3-34)	CARD MALFUNCTION Indicator
1	+6.743 ± 0.003V rms	A6
2	+5.051 ± 0.003V rms	A3, A6
3	-6.372 ± 0.003V rms	A6
4	-5.025 ± 0.003V rms	A3, A6
5	0.000 ± 0.005V rms	A3, A6

1/ A plus (+) sign indicates that the ac input is in-phase with AC Ref 1 and a negative (-) sign indicates in-phase with AC Ref 2.

3.3.21 LMTR1/LMTR2/D_L comparator logic. With the input conditions established as specified in 3.3.10, a logic "1" level of item 2.48 of Table I applied to J3-68 and items 2.17, 2.18, and 2.46 of Table I applied to J3-63, 64, and J4-67, respectively: (see 4.6.1.21)

a. With the variable ac inputs to J3-63 and 64 adjusted to 0.000 ± 0.005V rms and the variable ac input to J4-67 adjusted to the values specified for each item of Table XXVII, the corresponding CARD MALFUNCTION indicators shall illuminate.

b. With the variable ac input to J3-63 adjusted to the values specified for each item of Table XXVIII, the corresponding CARD MALFUNCTION indicators shall illuminate.

c. With the variable ac input to J3-64 adjusted to 9.400 ± 0.010V rms, in-phase with AC Ref 1, the A10 CARD MALFUNCTION indicator shall illuminate.

d. With the input to J3-64 adjusted to 0.000 ± 0.005V rms, the COMPUTER OK indicator shall illuminate.

TABLE XXVII. D_L comparator logic.

Item	Input (J4-67)	CARD MALFUNCTION Indicator
1	-2.335 ± 0.005V rms	COMPUTER OK
2	-2.423 ± 0.002V rms	A10
3	-2.376 ± 0.002V rms	COMPUTER OK
4	-2.250 ± 0.002V rms	A10
5	-2.297 ± 0.002V rms	COMPUTER OK
6	-2.335 ± 0.005V rms	COMPUTER OK

TABLE XXVIII. LMTR1 comparator logic.

Item	Input (J3-63)	CARD MALFUNCTION Indicator
1	+6.492 ± 0.003V rms	A10
2	+5.319 ± 0.003V rms	COMPUTER OK
3	-6.133 ± 0.003V rms	A10
4	-5.279 ± 0.003V rms	COMPUTER OK
5	0.000 ± 0.005V rms	COMPUTER OK

3.3.22 Phase outputs. With the POWER switch set to ON, the UNIT SELECT switch set to COMPUTER, the PHASE switch set to position "1" and the TEST SELECT switch set to position 4 and item 2.1 of Table I applied between J1-52 and J1-50, item 2.2 of Table I applied between J1-17 and J1-50 and adjusted to 2.737 ± 0.003V rms, item 2.21 of Table I applied between J3-7 and J1-50 and adjusted to 2.500 ± 0.010V rms and item 2.22 of Table I applied

between J3-1 and J1-50 and adjusted to 2.500 ± 0.010V rms and with the electrical output loads specified in Figure 1 applied to the pins specified and with returns all connected to J1-50 (GND); the output voltage measured at the specified output terminals for each of the 5 PHASE switch positions shall be in accordance with Table XXIX (see 4.6.1.22).

TABLE XXIX. Phase output voltages.

Item	PHASE Position	Output Terminal Connection	Output Voltage 1/ (V dc)
1	1	J1-45	0.000 ± 0.005
2	1	J2-34	0.000 ± 0.005
3	1	J2-69	0.000 ± 0.005
4	1	J3-20	0.000 ± 0.005
5	1	J2-70	0.000 ± 0.005
6	2	J1-45	-6.990 ± 0.152
7	2	J2-34	+0.092 ± 0.002
8	2	J2-69	+4.753 ± 0.009
9	2	J3-20	0.000 ± 0.005
10	2	J2-70	+5.321 ± 0.009
11	3	J1-45	0.000 ± 0.005
12	3	J2-34	0.000 ± 0.005
13	3	J2-69	+4.753 ± 0.009
14	3	J3-20	0.000 ± 0.005
15	3	J2-70	+5.321 ± 0.009
16	4	J1-45	0.000 ± 0.005
17	4	J2-34	0.092 ± 0.002
18	4	J2-69	+4.753 ± 0.009
19	4	J3-20	0.000 ± 0.005
20	4	J2-70	+5.321 ± 0.009
21	5	J1-45	0.000 ± 0.005
22	5	J2-34	0.000 ± 0.005
23	5	J2-69	+4.753 ± 0.009
24	5	J3-20	+8.325 ± 0.037
25	5	J2-70	+5.321 ± 0.009
26	1 2/	J1-44	+1.942 ± 0.006
27	1	J1-18	5/
28	1	J1-19	5/
29	1	J1-21	5/
30	1	J1-46	5/
31	1	J1-47	5/
32	1	J1-66	5/
33	1	J1-20	5/
34	1	J1-22	5/
35	1	J3-5	-2.270 ± 0.016
36	1	J3-11	-2.498 ± 0.017
37	1	J3-66	5/

TABLE XXIX. Phase output voltages. - (Cont.)

Item	PHASE Position	Output Terminal Connection	Output Voltage 1/ (V dc)
38	1	J3-39	5/
39	2 3/	J1-44	+1.835 ± 0.005
40	2	J1-18	+1.531 ± 0.013
41	2	J1-19	+1.940 ± 0.011
42	2	J1-21	+1.963 ± 0.011
43	2	J1-46	-1.530 ± 0.023
44	2	J1-47	-0.740 ± 0.013
45	2	J1-66	+1.642 ± 0.019
46	2	J1-20	+0.856 + 0.013 - 0.138
47	2	J1-22	+0.816 + 0.012 - 0.112
48	2	J3-5	-0.283 ± 0.038
49	2	J3-11	-2.498 ± 0.017
50	2	J3-66	5/
51	2	J3-39	5/
52	3 4/	J1-44	+2.049 ± 0.010
53	3	J1-18	5/
54	3	J1-19	5/
55	3	J1-21	+3.300 ± 0.023
56	3	J1-46	-1.526 ± 0.027
57	3	J1-47	-0.739 ± 0.014
58	3	J1-66	-1.641 ± 0.020
59	3	J1-20	5/
60	3	J1-22	5/
61	3	J3-5	-1.066 ± 0.034
62	3	J3-11	-2.498 ± 0.017
63	3	J3-66	5/
64	3	J3-39	5/
65	4 2/	J1-44	+1.941 ± 0.017
66	4	J1-18	5/
67	4	J1-19	5/
68	4	J1-21	5/
69	4	J1-46	5/
70	4	J1-47	5/
71	4	J1-66	5/
72	4	J1-20	5/
73	4	J1-22	5/
74	4	J3-5	-2.272 ± 0.018
75	4	J3-11	-2.498 ± 0.017
76	4	J3-66	5/
77	4	J3-39	5/
78	5	J1-44	+1.940 ± 0.008
79	5	J1-18	5/

TABLE XXIX. Phase output voltages. - (Cont.)

Item	PHASE Position	Output Terminal Connection	Output Voltage 1/ (V dc)
80	5	J1-19	5/
81	5	J1-21	5/
82	5	J1-46	5/
83	5	J1-47	5/
84	5	J1-66	5/
85	5	J1-20	5/
86	5	J1-22	5/
87	5	J3-5	-2.273 ± 0.019
88	5	J3-11	-2.500 ± 0.027
89	5	J3-66	-3.895 ± 0.026
90	5	J3-39	+5.000 ± 0.007

1/ Items 1 through 25 represent dc voltages. Items 26 through 90 are ac voltages where "+" indicates in-phase with AC Ref 1 and "-" indicates 180 degrees out-of-phase with AC Ref 1.
2/ Item 2.2 of Table I is applied and adjusted to 2.737 ± 0.003V rms.
3/ Item 2.2 of Table I is applied and adjusted to 2.585 ± 0.003V rms.
4/ Item 2.2 of Table I is applied and adjusted to 2.877 ± 0.003V rms.
5/ The voltage value shall be 0.018V rms maximum.

3.3.23 Computer lead-lock test logic. With POWER switch set to ON, UNIT SELECT switch set to COMPUTER, PHASE and TEST SELECT switches set to position 4, a logic "1" level of item 2.49 of Table I applied to J1-34, a logic "0" level of item 2.47 of Table I applied to J2-16 and J2-19, a logic "0" level of item 2.25 of Table I applied to J1-23, 24, 35 and J4-19 and the variable input voltages of Table XXX applied as specified: (see 4.6.1.23)

a. With the TEST INITIATE switch momentarily pressed, the COMPUTER OK indicator shall illuminate after 25.6 ± 3.3 seconds.

b. With the variable ac input of item 2.23 of Table I adjusted to the values specified for each item of Table XXXI and the TEST INITIATE switch momentarily depressed, corresponding CARD MALFUNCTION indicator shall illuminate after 25.6 ± 3.3 seconds.

c. With the TEST INITIATE switch momentarily depressed, the waveform voltages shown on Figure 2 shall appear at J2-66.

d. With the PHASE switch set to position 5 and the variable ac input of item 2.46 of Table I adjusted to 0.322 ± 0.005V rms, PH 2 and item 2.23 applied and adjusted to the values specified for each item of Table XXXII and the TEST INITIATE switch momentarily depressed, the corresponding CARD MALFUNCTION indicator shall illuminate after 25.6 ± 3.3 seconds.

TABLE XXX. Computer lead-lock test logic requirements.

Table I Item	Connector	Return	Adjustments 1/
2.1	J1-52	J1-50	5.000 ± 0.005V rms, Ph 1
2.3	J4-44, et al	J4-83	2.023 ± 0.005V dc
2.4	J3-78	J1-67	12.469 ± 0.005V dc
2.5	J4-41	J1-50	-10.000 ± 0.005V dc
2.6	J4-2	J1-50	2.622 ± 0.005V rms, Ph 2
2.7	J4-3	J1-50	0.096 ± 0.005V rms, Ph 2
2.23	J4-69	J1-50	1.440 ± 0.005V rms, Ph 1
2.24	J4-21	J1-50	4.020 ± 0.005V dc
2.45	J1-54	J1-50	5.000 ± 0.005V rms, Ph 2
2.46	J4-67	J1-50	0.148 ± 0.005V rms, Ph 2

1/ Ph 2 is 180° out of phase from Ph 1 where Ph 1 is in phase with AC Ref 1.

TABLE XXXI. Computer lead-lock logic phase 4.

Item	Input (J4-69)	CARD MALFUNCTION Indicator
1	+1.440 ± 0.005V rms	COMPUTER OK
2	+1.500 ± 0.002V rms	A4
3	+1.465 ± 0.002V rms	COMPUTER OK
4	+1.384 ± 0.002V rms	A4
5	+1.418 ± 0.002V rms	COMPUTER OK

TABLE XXXII. Computer lead-lock logic phase 5.

Item	Input (J4-69)	CARD MALFUNCTION Indicator
1	+1.113 ± 0.005V rms	A5
2	+1.208 ± 0.016V rms	A4
3	+1.186 ± 0.015V rms	A5
4	+1.026 ± 0.016V rms	A4
5	+1.045 ± 0.014V rms	A5

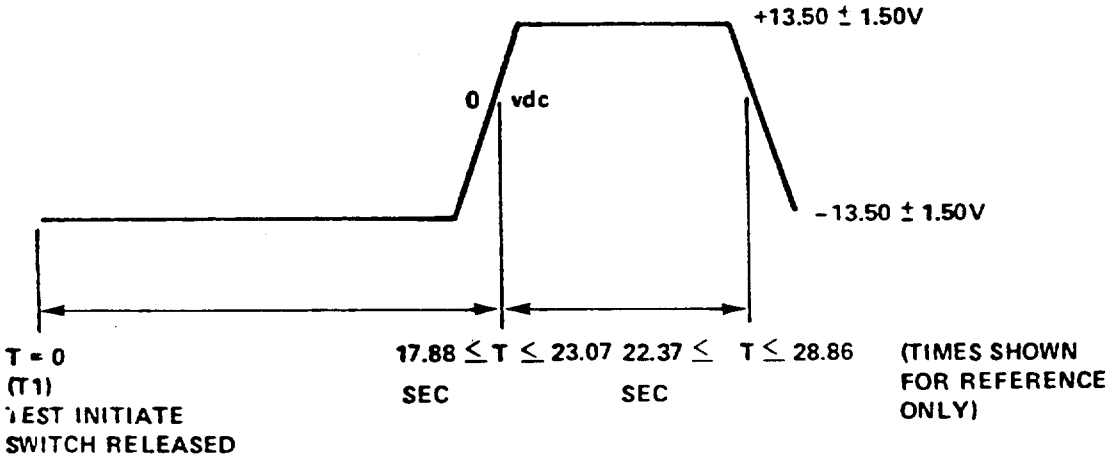


FIGURE 2. Computer Lead-Lock Signal at J2-66.

3.3.24 Computer Phase 2 and 3 fail logic. With POWER switch set ON, UNIT SELECT switch set to COMPUTER, TEST SELECT switch set to position 4 and PHASE switch set to position 2, a logic "1" level of item 2.49 of Table I applied to J1-34, a logic "0" level of item 2.47 of Table I applied to J2-16, J2-19, a logic "0" level of item 2.25 of Table I applied to J1-23, 24, 35, and J4-19, and the variable input voltages of Table XXXIII applied as specified: (see 4.6.1.24)

a. With the input conditions of Table XXXIV established, in any item order, the corresponding CARD MALFUNCTION indicator shall illuminate.

b. With the variable input voltages of TABLE XXXV applied as specified, the PHASE switch set to position 3, and the input conditions of Table XXXVI established, in any item number order, the corresponding CARD MALFUNCTION indicators shall illuminate.

TABLE XXXIII. Computer phase 2 and 3 fail logic requirements.

Table I Item	Connector	Return	Initial Voltage 1/ Adjustment
2.1	J1-52	J1-50	5.000 ± 0.005V rms, Ph 1
2.3	J4-44, etal	J4-83	2.023 ± 0.005V dc
2.4	J3-78	J1-67	12.469 ± 0.005V dc
2.5	J4-41	J1-50	-10.000 ± 0.005V dc
2.6	J4-2	J1-50	2.240 ± 0.005V rms, Ph 2
2.7	J4-3	J1-50	0.780 ± 0.005V rms, Ph 2
2.17	J3-63	J3-40	0.000 ± 0.500V rms, Ph 1
2.18	J3-64	J3-40	6.492 ± 0.003V rms, Ph 1
2.23	J4-69	J1-50	0.697 ± 0.005V rms, Ph 1
2.24	J4-21	J1-50	4.020 ± 0.005V dc
2.45	J1-54	J1-50	5.000 ± 0.005V rms, Ph 2
2.46	J4-67	J1-50	1.532 ± 0.005V rms, Ph 2

1/ Ph 2 is 180° out of phase from Ph 1 where Ph 1 is in phase with AC Ref 1.

TABLE XXXIV. Phase 2 logic.

Item	Inputs 1/ J1-14	J3-68	J3-70	J3-71	J3-72	J3-73	J3-74	J3-75	J3-76	CARD MALFUNCTION Indicator
1	0	1	0	0	0	0	0	0	1	COMPUTER OK
2	0	1	0	0	1	0	0	0	1	A8
3	0	1	1	0	0	0	0	0	1	A8
4	0	1	0	1	0	0	0	0	1	A8
5	0	1	0	0	0	1	0	0	1	A8
6	0	1	0	0	0	0	1	0	1	A8
7	0	1	0	0	0	0	0	1	1	A8
8	1	1	0	0	0	0	0	0	1	A9
9	0	1	0	0	0	0	0	0	0	A8
10	0	0	0	0	0	0	0	0	1	A10

1/ A "O" indicates that the logic "0" level of item 2.47 of Table I is applied and a "1" indicates that the logic "1" level of item 2.48 of Table I is applied.

TABLE XXXV. Computer phase 3 fail logic requirements.

Table I Item	Connector	Return	Initial Voltage 1/ Adjustment
2.1	J1-52	J1-50	5.000 ± 0.005V rms, Ph 1
2.3	J4-44, et al	J4-83	2.023 ± 0.005V dc
2.4	J3-78	J1-67	12.469 ± 0.005V dc
2.5	J4-41	J1-50	-10.000 ± 0.005V dc
2.6	J4-2	J1-50	2.270 ± 0.005V rms, Ph 2
2.7	J4-3	J1-50	0.504 ± 0.005V rms, Ph 2
2.17	J3-63	J3-40	0.000 ± 0.500V rms, Ph 1
2.18	J3-64	J3-40	6.492 ± 0.003V rms, Ph 1
2.23	J4-69	J1-50	0.420 ± 0.005V rms, Ph 1
2.24	J4-21	J1-50	-4.020 ± 0.005V dc
2.45	J1-54	J1-50	5.000 ± 0.005V rms, Ph 2
2.46	J4-67	J1-50	0.036 ± 0.005V rms, Ph 2

1/ Ph 2 is 180° out of phase from Ph 1 where Ph 1 is in phase with AC Ref 1.

TABLE XXXVI. Phase 3 logic.

Item	Inputs 1/ J1-14	J3-68	J3-70	J3-71	J3-72	J3-73	J3-74	J3-75	J3-76	CARD MALFUNCTION Indicator
1	0	1	0	0	0	0	0	0	1	A8, A9
2	1	1	0	0	0	0	0	0	1	A8
3	1	1	0	0	1	0	0	0	0	COMPUTER OK
4	1	0	0	0	1	0	0	0	0	A10
5	1	1	0	0	1	0	0	0	0	COMPUTER OK

1/ A logic "0" indicates that the logic "0" level of item 2.47 of Table I is applied and a "1" indicates that the logic "1" level of item 2.48 of Table I is applied.

3.3.25 Computer feedback simulator circuits.

3.3.25.1 D feedback in output. With the POWER switch set to ON, the UNIT SELECT switch set to COMPUTER, the PHASE and TEST SELECT switches set to positions 1 and 4, respectively, and the feedback load circuit of Figure 3 connected between J3-37 and J3-36, and J3-34 connected to J1-50 (GND), the D Feedback shall provide the following outputs: (see 4.6.1.25.1)

a. When 4.700 ± 0.010V rms, 400 Hz ± 1 Hz, phase 1 (item 2.26 of Table I) is applied to Vin of Figure 3 (return to ground of J1-50) and S1 is closed, the output at J3-37 shall increase to 4.700 + 0.104V rms, 400 Hz ± 1 Hz, phase 1. When S1 is opened, the output voltage at J3-37 shall decrease to 0.000 ± 0.050V rms within 42 ± 16 seconds.

b. When S1 is opened and voltage is applied to Vin of Figure 3 adjusted to 4.700 ± 0.010V rms, 400 Hz ± 1 Hz phase 2 (item 2.27 of Table I) closure of S1 shall cause the output voltage of J3-37 to increase to 4.700 ± 0.104V rms, 400 Hz ± 1 Hz phase 2. When S1 of Figure 3 is opened, the output voltage at J3-37 shall decrease to 0.000 ± 0.050V rms within 42 ± 16 seconds.

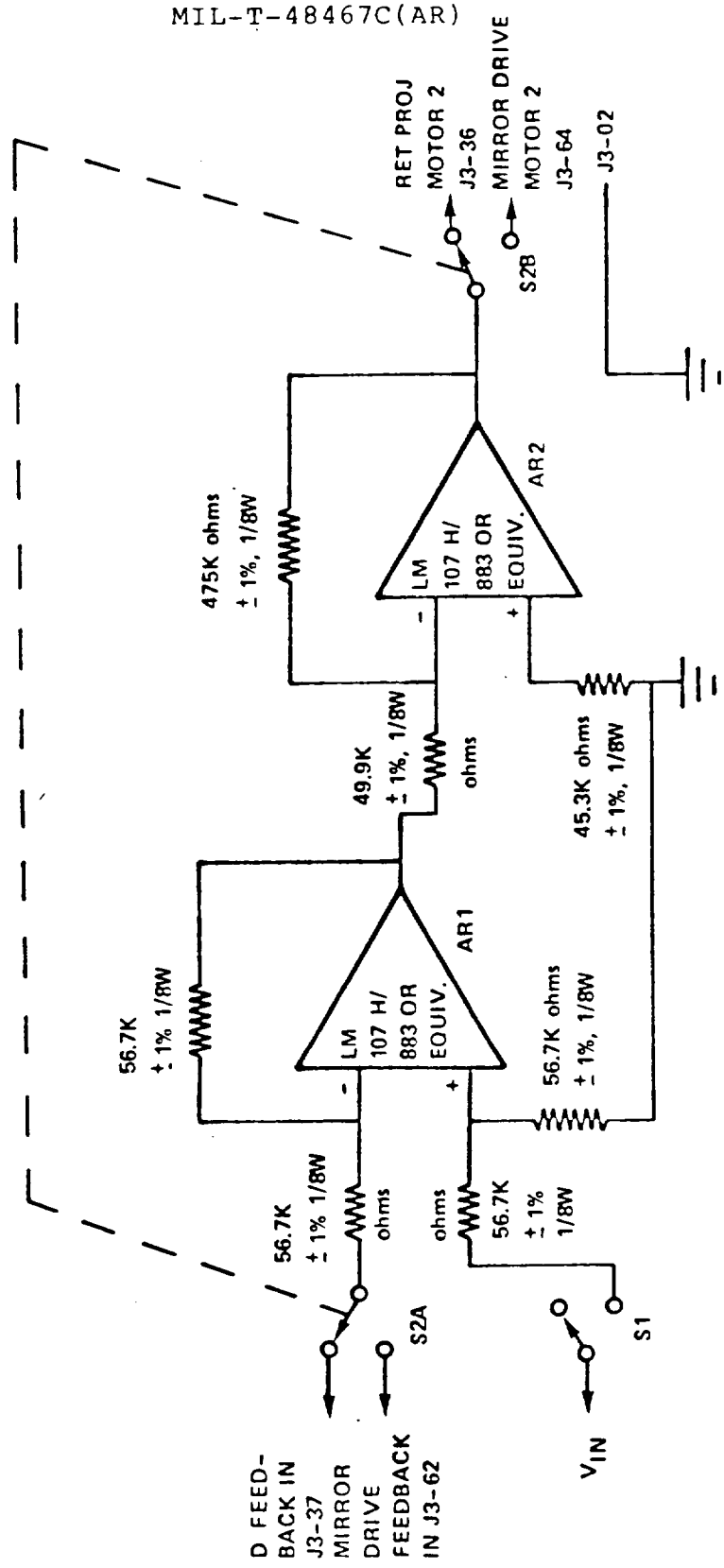


FIGURE 3. D Fdbk (IN) and DL Fdbk (IN) Feedback Load Circuit.

3.3.25.2 D_L feedback in output. With the input conditions established as specified in 3.3.25.1, and with the feedback circuit of Figure 3 connected between J3-62 and J3-64, with J3-63 connected to J1-50 (GND), the D_L Feedback shall provide the following outputs: (see 4.6.1.25.2)

a. With 4.700 ± 0.010V rms, 400 Hz ± 1 Hz, phase 1 (item 2.28 of Table I) applied to Vin of Figure 3 (return to J1-50), with S1 open the output voltage at J3-63 shall increase to 4.700 ± 0.104V rms, 400 Hz ± 1 Hz, phase 1 with the closure of S1. With S1 opened, the output voltage at J3-64 shall decrease to 0.000 ± 0.050V rms within 8.3 ± 3.2 seconds.

b. With 4.700 ± 0.010V rms, phase 2 (item 2.29 of Table I) applied to Vin of Figure 2 (return to J1-50), with S1 open the output voltage of J3-64 shall increase to 4.700 ± 0.104V rms, 400 Hz ± 1 Hz, phase 2 with the closure of S1. With S1 opened, the output voltage at J3-64 shall decrease to 0.000 ± 0.050V rms within 8.3 ± 3.2 seconds.

3.3.25.3 -E feedback in output. With the input conditions established as specified in 3.3.25.1 and with the feedback circuit of Figure 4 connected between J3-31 and J3-37, with J3-18 connected to J1-50 (GND), the -E Feedback shall provide the following outputs: (see 4.6.1.25.3)

a. With 2.000 ± 0.010V dc (item 2.33 of Table I) applied to Vin of Figure 4, (return to J1-50), with S1 open the output voltage at J3-31 shall increase to 2.000 ± 0.021V rms, 400 Hz ± 1 Hz, phase 1 with the closure of S1. With S1 opened, the output voltage at J3-31 shall decrease to 0.000 ± 0.050V rms within 40 ± 13 seconds.

b. With -2.000 ± 0.010V dc (item 2.33 of Table I) applied to Vin of Figure 4, (return to J1-50), with S1 open the output voltage at J3-31 shall increase to 2.000 ± 0.021V rms, 400 Hz ± 1 Hz, phase 2 with the closure S1. With S1 opened, the output voltage at J3-31 shall decrease to 0.000 ± 0.050V rms within 40 ± 13 seconds.

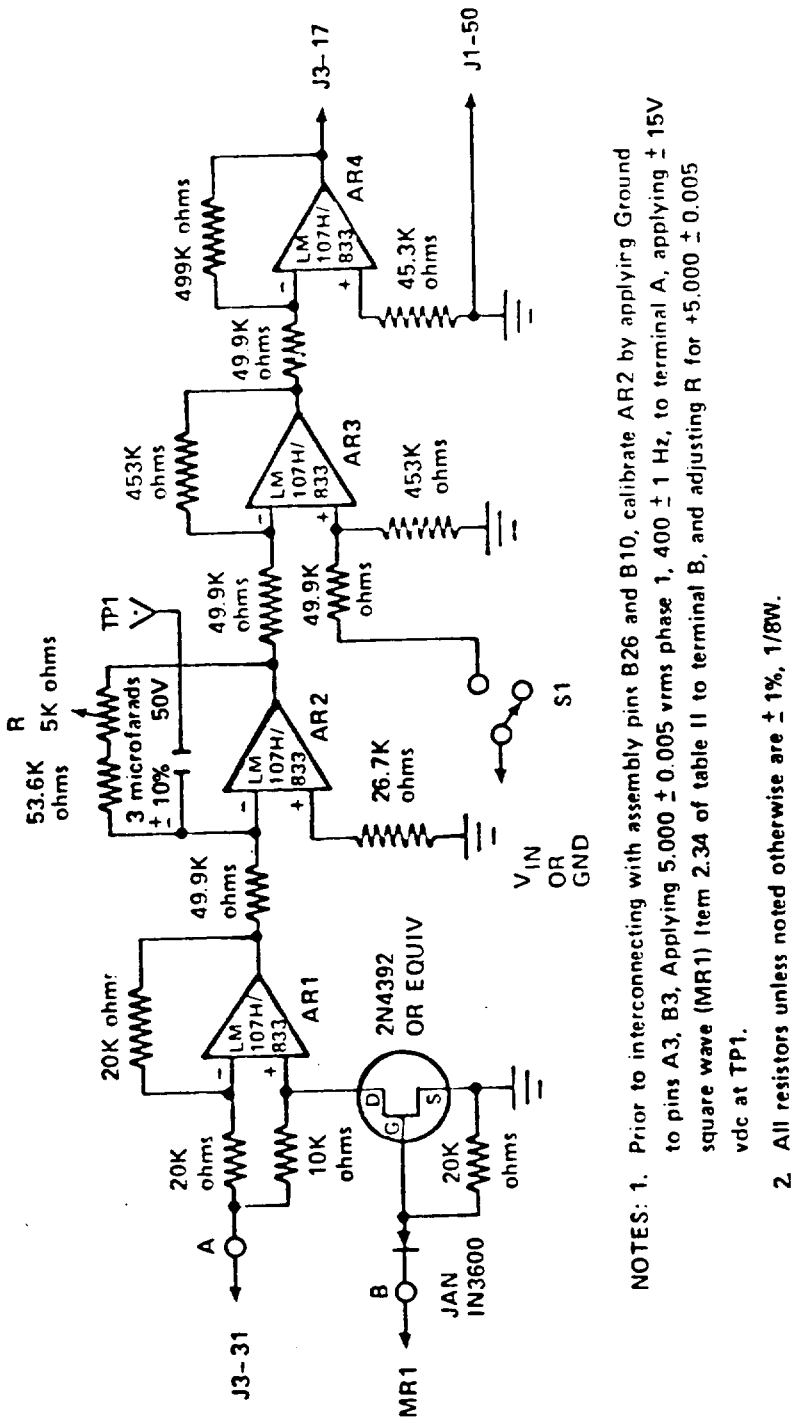


FIGURE 4. E Fdbk (IN) Feedback Load Circuit, Pre-connection Calibration Requirements, and Interconnection Provisions

3.3.25.4 Phases 2, 3 and 5 feedback simulator outputs. With the input conditions established as specified in 3.3.25.3, with the PHASE switch placed in positions 2, 3 and 5 for each phase, the output voltage shall be as specified in Table XXXVII (see 4.6.1.25.4).

TABLE XXVII. Simulator feedback outputs.

Item	Output Connector 1/	Phase to 2		Phase to 3		Phase to 5	
		Output Voltage, V rms	Phase	Output Voltage, V rms	Phase	Output Voltage, V rms	Phase
1	J3-37	1.178 ± 0.019	Ph 2	0.681 ± 0.013	Ph 2	0.227 ± 0.005	Ph 1
2	J3-31	0.681 ± 0.013	Ph 1	1.178 ± 0.019	Ph 2	1.504 ± 0.023	Ph 2
3	J3-62	1.279 ± 0.015	Ph 1	0.847 ± 0.010	Ph 1	0.189 ± 0.004	Ph 2

1/ Return to J1-50

3.3.26 Computer mode selection logic. With the POWER switch set to ON, the UNIT SELECT switch set to COMPUTER, the TEST SELECT switch set to position 4; with the PHASE switch set to positions 1 through 5, the output voltages shall be as specified in Table XXXVIII (see 4.6.1.26).

3.3.27 AMMO select logic. With the POWER switch set to ON, the UNIT SELECT switch set to COMPUTER, the TEST SELECT and TEST INITIATE switches set as specified in Table XXXIX the PHASE switch set to position 1, the AMMO select logic output voltages (return to J1-50) shall be as specified in Table XXXIX (see 4.6.1.27).

3.3.28 GCU A10 card. With the POWER switch set to ON, the UNIT SELECT switch set to GCU, the CONTINUITY switch set to OFF and the AMMO TEST switch set as specified in Table XL and with the input conditions established, in any item order, as specified in Table XL, the corresponding AMMO TEST/STATUS indicator shall illuminate (see 4.6.1.28).

3.3.28.1 GCU potentiometer test circuit. With the POWER switch set to ON, the UNIT SELECT switch set to GCU, the input voltages applied in accordance with item 2.30 of Table I to J5-18 20, 22 and 44, with item 2.31 of Table I applied to J5-15, 16, 46, and 47 and with item 2.32 of Table I applied to J5-45: (see 4.6.1.28.1)

a. With the POTENTIOMETER TEST switch set to ALT and the input voltage to J5-22 varied from minus 15.00 ± 0.050 to plus 15.00 ± 0.050V dc; the CONTINUITY TEST meter shall deflect fully left to right (-100 ± 5 microamps to +100 ± 5 microamps).

b. With the POTENTIOMETER TEST switch set on AIR TEMP and the input voltage to J5-20 varied from minus 15.00 ± 0.050 to plus 15.00 ± 0.050V dc; the CONTINUITY TEST meter shall deflect fully from left to right (-100 ± 5 microamps to +100 ± 5 microamps).

c. With the POTENTIOMETER TEST switch set to MAN RANGE and the CONTINUITY switch set to OFF and the input voltage to J5-44 varied from minus 6.98 ± 0.050 to plus 6.98 ± 0.050V dc; the CONTINUITY TEST meter shall deflect fully from left to right (-100 ± 5 microamps to +100 ± 5 microamps).

d. With the POTENTIOMETER TEST switch set on the REMAINING TUBE LIFE and the input voltage to J5-18 varied from minus 15.00 ± 0.050 to plus 15.00 ± 0.050V dc; the CONTINUITY TEST meter shall deflect fully from left to right, (-100 ± 5 microamps to +100 ± 5 microamps).

e. With the POTENTIOMETER TEST switch set to AZ ZERO and the input voltage to J5-16 varied from minus 1.00 ± 0.050 to plus 1.00 ± 0.050V dc; the CONTINUITY TEST meter shall

deflect fully from left to right (-100 ± 5 microamps to +100 ± 5 microamps).

f. With the POTENTIOMETER TEST switch set on EL ZERO and the input voltage to J5-15 varied from minus 1.00 ± 0.050 to plus 1.00 ± 0.050V dc; the CONTINUITY TEST meter shall deflect fully from left to right (-100 ± 5 microamps to +100 ± 5 microamps).

g. With the POTENTIOMETER TEST switch set to AZ COMMON ZERO and the input voltage to J5-47 varied from minus 1.00 ± 0.050 to plus 1.00 ± 0.050V dc, the CONTINUITY TEST meter shall deflect fully from left to right (-100 ± 5 microamps to +100 ± 5 microamps).

h. With the POTENTIOMETER TEST switch set on EL COMMON ZERO and the input voltage to J5-46 varied from minus 1.00 ± 0.050 to plus 1.00 ± 0.050V dc; the CONTINUITY TEST meter shall deflect fully from left to right (-100 ± 5 microamps to +100 ± 5 microamps).

i. With the POTENTIOMETER TEST switch set on CROSSWIND and the input voltage to J5-45 varied from minus 10.00 ± 0.050 to plus 10.00 ± 0.050V dc; the CONTINUITY TEST meter shall deflect fully from left to right (-100 ± 5 microamps to +100 ± 5 microamps).

3.3.29 A14 board load simulator outputs. With the POWER switch set to ON: (see 4.6.1.29)

a. The output voltage at J2-54 shall be minus 9.275 ± 0.090V dc (return to J1-50).

b. The output voltage at J2-53 shall be 3.345 ± 0.058V dc (return to J2-50).

TABLE XXXVIII. Computer mode selection logic.

Item	Signal 1/	Output At	FTS PHASE Position 1 (V dc)	2 (V dc)	3 (V dc)	4 (V dc)	5 (V dc)
1	BIT	J1-39	14.00 ± 0.20	-15.00 ± 0.20	-15.00 ± 0.20	-15.00 ± 0.20	-15.00 ± 0.20
2	BIT BAR	J1-62	-14.50 ± 0.20	14.00 ± 0.20	13.70 ± 0.40	14.00 ± 0.20	13.70 ± 0.40
3	MT	J2-5	-14.50 ± 0.20	-14.50 ± 0.20	13.70 ± 0.40	14.00 ± 0.20	13.70 ± 0.40
4	MT BAR	J2-6	14.00 ± 0.20	14.00 ± 0.20	-15.00 ± 0.20	-15.00 ± 0.20	-15.00 ± 0.20
5	BS	J1-42	-14.50 ± 0.20	-14.50 ± 0.20	13.70 ± 0.40	-14.20 ± 0.20	-13.00 ± 0.20
6	BS BAR	J1-43	14.00 ± 0.20	14.00 ± 0.20	-15.00 ± 0.20	14.00 ± 0.20	13.70 ± 0.40
7	MW	J1-40	-15.00 ± 0.20	14.00 ± 0.20	-15.00 ± 0.20	14.00 ± 0.20	-15.00 ± 0.20
8	MW BAR	J1-41	14.00 ± 0.20	-14.50 ± 0.20	13.70 ± 0.40	-14.20 ± 0.20	13.70 ± 0.40
9	STAB	J2-72	-14.50 ± 0.20	14.00 ± 0.20	13.70 ± 0.40	-14.20 ± 0.20	13.70 ± 0.40
10	SIGNLD	J2-55	OPEN	OPEN	OPEN	15.00 ± 0.20	15.00 ± 0.20
11	NP10R2	J3-55	0.00 ± 0.40	0.00 ± 0.40	3.90 ± 1.50	3.90 ± 1.50	3.90 ± 1.50
12	NP5LA	J1-69	3.90 ± 1.50	3.90 ± 1.50	3.90 ± 1.50	3.90 ± 1.50	0.00 ± 0.40

1/ Return to J1-50

TABLE XXXIX. Ammo select logic outputs.

ITEM	OUTPUT CONNECTION	FTS TEST INITIATE PUSH BUTTON	TEST SELECT POSITION 1/ 1	2	3	4	5	SIGNAL
1	J2-9	NORMAL	OPEN	OPEN	OPEN	OPEN	OPEN	N.APDS
2	J2-9	DEPRESSED	OPEN	0.0 ± 0.005	OPEN	OPEN	OPEN	N.APDS
3	J2-10	NORMAL	OPEN	OPEN	OPEN	OPEN	OPEN	N.HEAT
4	J2-10	DEPRESSED	OPEN	OPEN	0.0 ± 0.005	OPEN	OPEN	N.HEAT
5	J1-33	NORMAL	0.0 ± 0.005	-15.0 ± 0.2	0.0 ± 0.005	0.0 ± 0.005	0.0 ± 0.005	AS6...
6	J1-33	DEPRESSED	0.0 ± 0.005	-15.0 ± 0.2	0.0 ± 0.005	0.0 ± 0.005	0.0 ± 0.005	AS6...
7	J1-28	NORMAL	-15.0 ± 0.2	-15.0 ± 0.2	-0.5 ± 0.2	-15.0 ± 0.2	-15.0 ± 0.2	AS2...
8	J1-28	DEPRESSED	-15.0 ± 0.2	-15.0 ± 0.2	-0.5 ± 0.2	-15.0 ± 0.2	-15.0 ± 0.2	AS2...
9	J2-11	NORMAL	OPEN	OPEN	OPEN	OPEN	OPEN	HEPBAR
10	J2-11	DEPRESSED	OPEN	OPEN	OPEN	0.0 ± 0.005	OPEN	HEPBAR
11	J2-12	NORMAL	OPEN	OPEN	OPEN	OPEN	OPEN	N.FSDS
12	J2-12	DEPRESSED	OPEN	OPEN	OPEN	OPEN	0.0 ± 0.005	N.FSDS

1/ Readings in V dc with return to J1-50

TABLE XL. GCU A10 card ammo/status select logic.

Item	AMMO TEST	Inputs 1/ J5-28	J5-33	J5-39	J5-40	J5-41	J5-42	J5-43	J5-62	J5-69 2/	AMMO TEST INDICATION	STATUS INDICATION
1	APDS	0	1	-	-	-	-	-	-	-	APDS M.392	-
2	APDS	0	0	-	-	-	-	-	-	-	APDS M728	-
3	HEAT	1	0	-	-	-	-	-	-	-	HEAT M456	-
4	HEP/WP	0	0	-	-	-	-	-	-	-	HEP/WP	-
5	FSDS	0	0	-	-	-	-	-	-	-	FSDS	-
6	-	-	-	0	-	-	-	-	1	-	-	SELF TEST SYSTEM
7	-	-	-	1	-	-	-	-	0	-	-	SELF TEST NORMAL
8	-	-	-	-	-	-	0	1	-	-	-	MODE BORESIGHT
9	-	-	-	-	-	-	1	0	-	-	-	MODE NORMAL
10	-	-	-	-	1	0	-	-	-	-	-	WIND MAN
11	-	-	-	-	0	1	-	-	-	-	-	WIND AUTO
12	-	-	-	-	-	-	-	-	-	1	-	RANGE LRF
13	-	-	-	-	-	-	-	-	-	0	-	RANGE MAN

1/ A "0" indicates a logic "0" level of item 2.50 of Table I is applied, a "1" indicates that a logic "1" level of item 2.49 of Table I is applied and a "-" indicates a "don't care" condition.
2/ A "0" indicates a logic "0" level of item 2.47 of Table I is applied and a "1" indicates that a logic "1" level of item 2.48 of Table I is applied.

3.3.30 GCU continuity test circuits. With the POWER switch set to ON, the UNIT SELECT switch set to GCU, the POTENTIOMETER TEST switch set to CON TEST, the input voltages applied in accordance with item 2.35 of Table I to J5-2, 4, 19, 21, 65, 81, and 85, with item 2.36 of Table I applied to J5-66 and with pins J5-6, 67, and 68 interconnected with pin J5-61: (see 4.6.1.30)

a. With the CONTINUITY switch set to 1, and the input voltage at J5-66 adjusted to the values specified for each item in Table XLI, there shall be a corresponding CONTINUITY TEST meter deflection.

b. With the CONTINUITY switch set to 2 and the input voltage at J5-2, 4, 19, 21, 65, 81, and 85 set to 11.80 ± 0.05 volts, the CONTINUITY TEST meter shall deflect +50 ± 25 microamps.

c. With the CONTINUITY switch set to 3, pin J5-44 shall be ground (0.000 ± 0.005V dc).

d. With the CONTINUITY switch set to 3 and -15.000 ± 0.030V dc (item 2.25 of Table I) applied through a 301 Kohm (1/8 watt, 1%) resistor to pin J5-72, the CONTINUITY TEST meter shall indicate +50 ± 25 microamps.

e. With the CONTINUITY switch set to 4 and -15.000 ± 0.030V dc (item 2.25 of Table I) applied through a 402 Kohm (1/8 watt, 1%) resistor to pin J5-44, the CONTINUITY TEST meter shall indicate +50 ± 25 microamps.

f. With the CONTINUITY switch set to 5 and the LAMP TEST switch pressed and held, pins J5-7, 8, 9, 10, 11, 12, 13, and 14 shall be ground (0.000 ± 0.005V dc).

g. With the CONTINUITY switch set to 6 and the LAMP TEST switch pressed and held, pin J5-63 shall be ground (0.000 ± 0.005V dc).

TABLE XLI. GCU test continuity comparator logic.

Item	Input (J5-66)	CARD MALFUNCTION Indication (Microamperes)
1	+1.005 ± 0.005V dc	+50 ± 25
2	+1.083 ± 0.001V dc	0 ± 25
3	+1.045 ± 0.001V dc	+50 ± 25
4	+0.935 ± 0.001V dc	0 ± 25
5	+0.965 ± 0.001V dc	+50 ± 25

3.3.31 Computer continuity test circuits. With the POWER switch set to ON, the UNIT SELECT switch set to COMPUTER, the PHASE switch set to position 5, the input voltages applied in accordance with item 2.37 of Table I to J1-57, J3-59, J2-50 and 68, with item 2.38 of Table I applied to J1-49, J2-7, 8, 56 and J3-58, with item 2.39 of Table I applied to J1-70, J3-60 and J2-75, with item 2.40 of Table I applied to J1-72, J2-24 and J3-25, with item 2.41 of Table I applied to J2-67, with item 2.42 of Table I applied to J1-53, J3-21, 43 and 57, with item 2.43 of Table I applied to J3-22, 44, and 67, and with pins J2-25, 45, 46, 48, 51, 71, J3-19, 32, 65, and 69 interconnected with pin J1-50: (see 4.6.1.31)

a. With the CONTINUITY switch set to 1, the CONTINUITY TEST meter shall deflect +50 ± 25 microamps.

b. With the CONTINUITY switch set to 2 and the variable input voltage at J2-67 adjusted to -1.590 ± 0.015V dc, the CONTINUITY TEST meter shall indicate +50 ± 25 microamps.

c. With the CONTINUITY switch set to 3, the CONTINUITY TEST meter shall indicate +50 ± 25 microamps.

d. With the CONTINUITY switch set to 4 and item 2.44 of Table I applied to J3-33, the CONTINUITY TEST meter shall indicate +50 ± 25 microamps.

3.3.32 Ammo test switch outputs. With the POWER switch set to ON, the output voltages at J5-23, 24, 34, and 35 shall be as specified in Table XLII for each AMMO TEST switch position specified (see 4.6.1.32).

TABLE XLII. AMMO TEST switch outputs.

AMMO TEST Switch Item	Position	Output Voltages (V dc) J5-23	J5-24	J5-34	J5-35
1	APDS	0.0 ± 0.005	-15.0 ± 0.15	-15.0 ± 0.15	-15.0 ± 0.15
2	HEAT	-15.0 ± 0.15	0.0 ± 0.005	-15.0 ± 0.15	-15.0 ± 0.15
3	HEP/WP	-15.0 ± 0.15	-15.0 ± 0.15	0.0 ± 0.005	-15.0 ± 0.15
4	FSDS	-15.0 ± 0.15	-15.0 ± 0.15	-15.0 ± 0.15	0.0 ± 0.005

3.4 Environmental conditions. The assembly shall meet the requirements of 3.3 after being subjected to the environmental conditions specified herein.

3.4.1 Temperature. The assembly shall be capable of operating as specified herein over the operating temperature range of +40°F to 100°F and shall not be damaged when subjected to storage conditions ranging from -65°F to 160°F (see 4.6.2.1 and 4.6.2.2).

3.4.2 Vibration. The assembly shall be capable of operating as specified herein after withstanding exposure under the conditions of 3.1.3 to a sinusoidal vibration displacement of .03 inch double amplitude, 10 - 55 Hz in accordance with Figure 5. Duration of exposure shall be not less than 80 minutes in each of three mutually perpendicular axes (see 4.6.2.3).

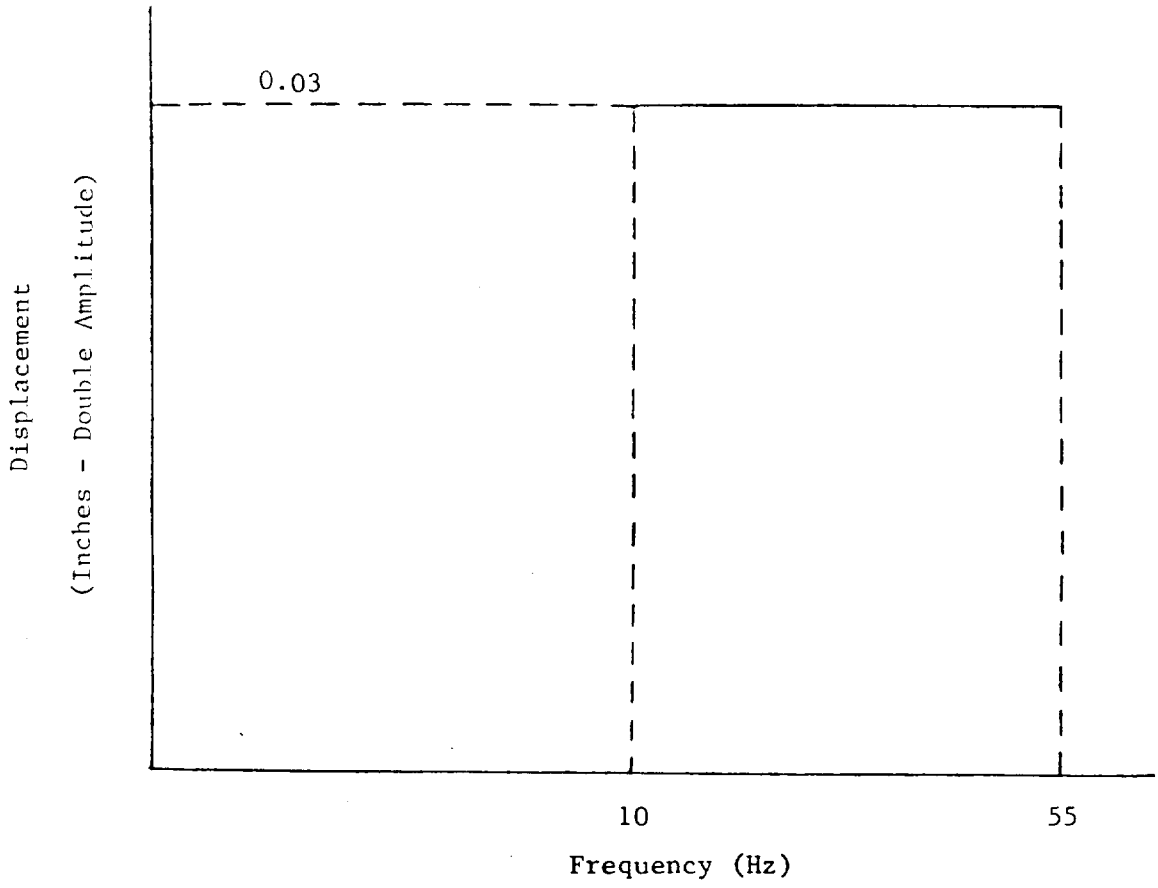


FIGURE 5. Vibration Curve.

3.4.3 Shock. The assembly shall be capable of operating as specified herein after withstanding exposure under the conditions of 3.1.3 to half sine wave shock pulses of 40 ± 4 gravity units (g's) for a duration of 18 ± 3 milliseconds (msec) in accordance with Figure 6. The assembly shall withstand 3 shock pulses applied in both directions along three mutually perpendicular axes (18 shocks). In addition, the assembly shall be capable of withstanding three half sine wave shock pulses of 100.0 ± 10.0 g's for a duration of 1.5 ± 0.2 msec applied in each direction along three mutually perpendicular axes (see 4.6.2.4).

A = 40 g's
D = 18 msec

A = 100 g's
D = 1.5 msec

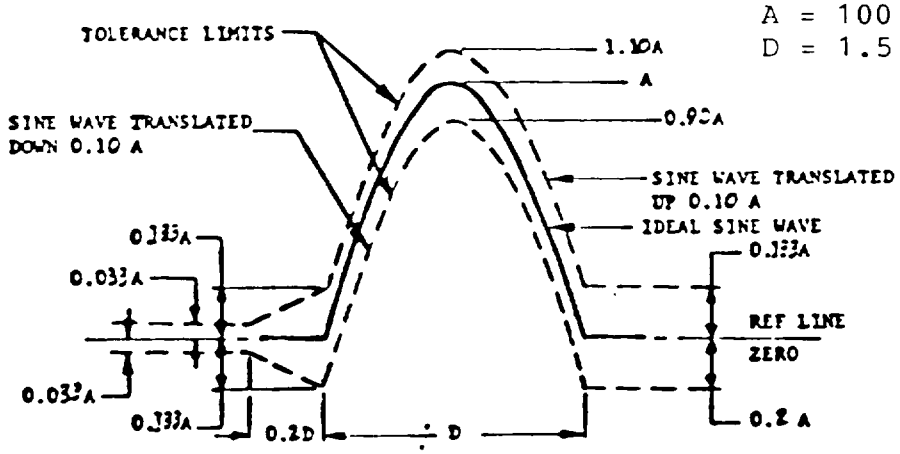


FIGURE 6. Shock Pulse.

3.4.4 Temperature cycling. The assembly shall be capable of operating as specified herein after withstanding exposure to temperature cycling and soaking between the temperatures of -25°F and 140°F in accordance with Figure 7 (see 4.6.2.5).

4. QUALITY ASSURANCE PROVISIONS

4.1 Responsibility for inspection. Unless otherwise specified in the contract or purchase order, the contractor is responsible for performance of all inspection requirements (examinations and tests) as specified herein. Except as otherwise specified in the contract or purchase order, the contractor may use his own or any other facilities suitable for the performance of the inspection requirements specified herein, unless disapproved by the Government. The Government reserves the right to perform any of the inspections set forth in this specification where such inspections are deemed necessary to ensure supplies and services conform to prescribed requirements.

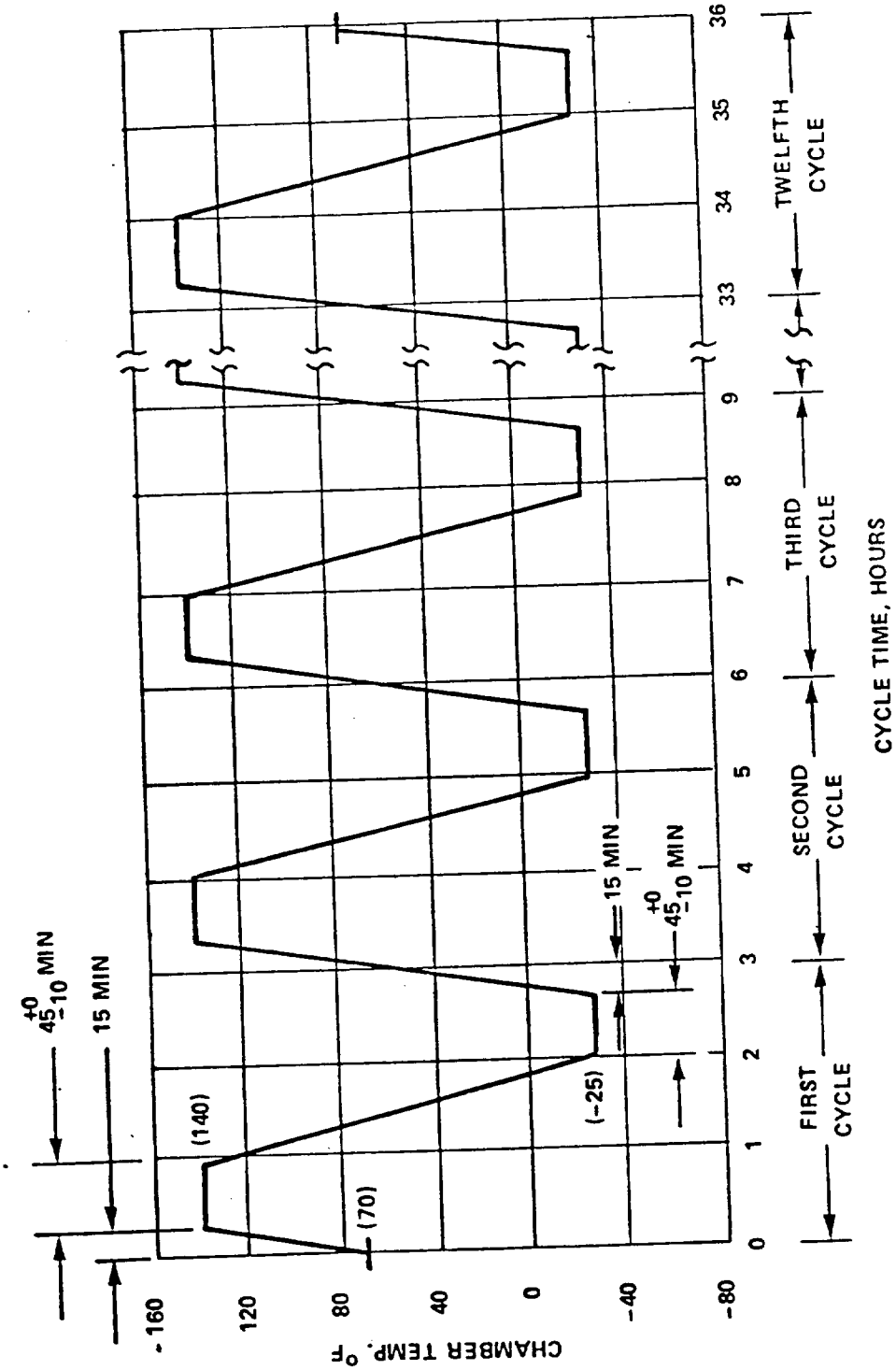


FIGURE 7. Temperature Cycling.

4.1.1 Responsibility for compliance. All items shall meet all requirements of sections 3 and 5. The inspection set forth in this specification shall become part of the contractor's overall inspection system or quality program. The absence of any inspection requirements in the specification shall not relieve the contractor of the responsibility of ensuring that all products or supplies submitted to the Government for acceptance comply with all requirements of the contract. Sampling inspection, as part of manufacturing operations, is an acceptable practice to ascertain conformance to requirements, however, this does not authorize submission of known defective material, either indicated or actual, nor does it commit the Government to accept defective material.

4.1.2 Inspection equipment. Unless otherwise specified in the contract, the contractor shall supply, maintain and calibrate inspection equipment in accordance with the provisions of MIL-I-45607 and by standard commercial practice. Contractor inspection equipment designs shall be submitted for Government approval as specified in the contract (see 6.5).

4.2 Classification of inspections. The inspection requirements specified herein are classified as follows:

a. First article inspection (see 4.4).
b. Quality conformance inspection (see 4.5 and 6.8).

4.3 Inspection conditions. Unless otherwise specified, all inspections shall be performed in accordance with the quality assurance provisions of MIL-F-13926 and the conditions of 3.1.3.

4.4 First article inspection. The requirements for first article approval and the designation of responsibility for first article inspection to either the Government or the contractor shall be specified in the contract (see 6.3).

4.4.1 Sample. The contractor shall submit a first article sample as designated by the Contracting Officer for evaluation in accordance with the provisions of 4.4.2. The first article sample shall consist of two assemblies.

4.4.2 Inspection. Two assemblies shall be subjected to the examinations and tests specified in Tables XLIII, XLIV, and XLV. Examinations 301 and 302 of Table XLV shall be performed first.

TABLE XLIII. Performance tests.

Item	Characteristic	Requirement	Test Procedure
101	Continuity	3.3.1	4.6.1.1
102	Resistance	3.3.2	4.6.1.2
103	POWER, UNIT SELECT, LAMP TEST switches and INCORRECT SETUP test	3.3.3	4.6.1.3
104	Prime power forms	3.3.4	4.6.1.4
105	TEST INITIATE switch and timing signal logic	3.3.5	4.6.1.5
106	Reference signal characteristic	3.3.6	4.6.1.6
107	A1 and A2 card fail logic	3.3.7	4.6.1.7
108	Computer -10 volt/AC REF 2 comparator logic	3.3.8	4.6.1.8
109	Ammo Select/MT comparator logic	3.3.9	4.6.1.9
110	-Epsilon comparator logic	3.3.10	4.6.1.10
111	Eta comparator logic	3.3.11	4.6.1.11
112	$(W-K_WV_W)T_F$ comparator logic	3.3.12	4.6.1.12
113	V_W comparator logic	3.3.13	4.6.1.13
114	CRS1/CRS2 comparator logic	3.3.14	4.6.1.14
115	E FDBK/D FDBK comparator logic	3.3.15	4.6.1.15
116	D PWR AMP/E PWR AMP 1/E PWR AMP 1/E comparator logic	3.3.16	4.6.1.16
117	E/-D comparator logic	3.3.17	4.6.1.17
118	System units OK logic	3.3.18	4.6.1.18
119	OUM1/OUM2 comparator logic	3.3.19	4.6.1.19
120	DMTR1/DMTR2 comparator logic	3.3.20	4.6.1.20
121	LMTR1/LMTR2/D_L comparator logic	3.3.21	4.6.1.21
122	Phase outputs	3.3.22	4.6.1.22
123	Computer lead-lock test logic	3.3.23	4.6.1.23
124	Computer phase 2 and 3 fail logic	3.3.24	4.6.1.24
125	D feedback in output	3.3.25.1	4.6.1.25.1
126	D_L feedback in output	3.3.25.2	4.6.1.25.2
127	-E feedback in output	3.3.25.3	4.6.1.25.3
128	Phases 2, 3 and 5 feedback simulator outputs	3.3.25.4	4.6.1.25.4
129	Computer mode selection logic	3.3.26	4.6.1.26
130	AMMO select logic	3.3.27	4.6.1.27
131	GCU A10 card	3.3.28	4.6.1.28
132	GCU potentiometer test circuit	3.3.28.1	4.6.1.28.1
133	A14 board load simulator outputs	3.3.29	4.6.1.29
134	GCU continuity test circuits	3.3.30	4.6.1.30
135	Computer continuity test circuits	3.3.31	4.6.1.31
136	AMMO test switch outputs	3.3.32	4.6.1.32

TABLE XLIV. First article environmental tests.

Item	Characteristic	Requirement	Test Procedure
201	High Temperature	3.4.1	4.6.2.1
202	Low Temperature	3.4.1	4.6.2.2
203	Vibration A	3.4.2	4.6.2.3.1
204	Shock	3.4.3	4.6.2.4
205	Temperature Cycling	3.4.4	4.6.2.5

TABLE XLV. Examination control examinations.

Item	Characteristic	Requirement	Test Procedure
301	Fabrication	3.1	Applicable drawings-Visual
302	General specifications	3.1.2	4.6.3 - Visual
303	Packaging inspection	5.1	4.6.4 - Visual

4.4.3 Failure. Failure of any assembly to meet any requirement shall be cause for refusal to grant first article approval. The Government reserves the right to terminate first article inspection upon any failure of any assembly to comply with any stated requirement.

4.4.4 Responsibility. The contractor, whether or not responsible, shall inspect the sample for conformance to all contractual requirements and shall submit a record of this inspection with the sample and certificates of conformance for materials. The Government reserves the right to witness inspections performed by the contractor.

4.5 Quality conformance inspection.

4.5.1 Performance inspection.

4.5.1.1 Performance sample and examinations. Each assembly in every lot shall be subjected to the examinations and tests in Table XLIII and shall be examined visually for completeness, improper assembly and evidence of poor workmanship per items 301 and 302 of Table XLV. The conditions of 3.1.3 apply.

4.5.1.2 Acceptance. Where any one assembly fails to meet any specified requirement, the defective assembly shall be removed from the lot and resubmitted only after all defects have been corrected.

4.5.2 Examination control inspection.

4.5.2.1 Examination control sample and examinations. One assembly, as a control sample, shall be selected at random by the Government representative from each 100 assemblies produced and shall be subjected to the examinations in Table XLV.

4.5.2.2 Acceptance. Where any assembly fails to meet any specified requirement, the lot shall be rejected. Rejected lots shall be resubmitted for reinspection only after all assemblies are re-examined or retested and all defective assemblies are removed or defects corrected.

4.5.3 Environmental control inspection.

4.5.3.1 Environmental control sample and examinations. One assembly, as a control sample, shall be selected at random by the Government representative from each 50 assemblies produced or from each month's production, whichever occurs first. The assembly shall be subjected to all of the tests of Table XLVI in the order listed. Combining of tests is not permitted.

TABLE XLVI. Environmental control examinations.

Item	Characteristic	Requirement	Test Procedure
401	High Temperature	3.4.1	4.6.2.1
402	Low Temperature	3.4.1	4.6.2.2
403	Vibration B	3.4.2	4.6.2.3.2
404	Shock	3.4.3	4.6.2.4
405	Temperature Cycling	3.4.4	4.6.2.5

4.5.3.2 Acceptance. Where any one assembly fails to meet any specified requirement, the lot shall be rejected. Rejected lots shall be resubmitted for reinspection only after all assemblies are re-examined or retested and all defective assemblies are removed or defects corrected.

4.6 Methods of inspection.

4.6.1 Performance tests.

4.6.1.1 Continuity. The outputs shall be measured and verified to comply with the requirements of paragraph 3.3.1.

4.6.1.2 Resistance. With the switches set as specified in paragraph 3.3.2, the outputs shall be measured and verified to comply with the requirements of paragraph 3.3.2.

4.6.1.3 Power, unit select, lamp test switches, and incorrect setup test. Apply the power form and switch settings per paragraph 3.3.3, verify the lamp indications meet the requirements of paragraph 3.3.3.

4.6.1.4 Prime power forms. Apply the power form and switch settings per paragraph 3.3.4. The outputs shall be measured and verified to comply with the requirements of paragraph 3.3.4.

4.6.1.5 Test initiate switch and timing signal logic. Apply the power form and switch settings per paragraph 3.3.5. Verify the lamp indications meet the requirements of paragraph 3.3.5.

4.6.1.6 Reference signal characteristics. Apply the power form and switch settings per paragraph 3.3.6. The outputs shall be measured and verified to comply with the requirements of 3.3.6.

4.6.1.7 A1 and A2 card fail logic. Apply the power form, input signals, and switch settings as per paragraph 3.3.7. The lamp indications and output voltage signals shall comply with the requirements of 3.3.7.

4.6.1.8 Computer -10 volt/AC Ref 2 comparator logic. Apply the power form, input signals, and switch settings per paragraph 3.3.8. The lamp indications and output voltage signals shall comply with the requirements of 3.3.8.

4.6.1.9 Ammo select/MT comparator logic. Apply the power form, input signals, and switch settings per paragraph 3.3.9. Verify the lamp indications meet the requirements of paragraph 3.3.9.

4.6.1.10 -Epsilon comparator logic. Apply the power form, input signals, and switch settings per paragraph 3.3.10. The lamp indications and output voltage signals shall comply with the requirements of 3.3.10.

4.6.1.11 Eta comparator logic. Apply the power form, input signals, and switch settings per paragraph 3.3.11. The lamp indications and output voltage signals shall comply with the requirements of 3.3.11.

4.6.1.12 $(W-K_W V_W)\ T_F$ comparator logic. Apply the power form, input signals, and switch settings per paragraph 3.3.12. The lamp indications and output voltage signals shall comply with the requirements of 3.3.12.

4.6.1.13 V_W comparator logic. Apply the power form, input signals, and switch settings as per paragraph 3.3.13. The lamp indications and output voltage signals shall comply with the requirements of 3.3.13.

4.6.1.14 CRS1/CRS2 comparator logic. Apply the power form, input signals, and switch settings per paragraph 3.3.14. The lamp indications and output voltage signals shall comply with the requirements of 3.3.14.

4.6.1.15 E FDBK/D FDBK. Apply the power form, input signals, and switch settings per paragraph 3.3.15. The lamp indications and output voltage signals shall comply with the requirements of 3.3.15.

4.6.1.16 D PWR AMP/E PWR AMP1/E PWR AMP2. Apply the power form, input signals, and switch settings per paragraph 3.3.16. The lamp indications and output voltage signals shall comply with the requirements of 3.3.16.

4.6.1.17 E/-D comparator logic. Apply the power form, input signals, and switch settings per paragraph 3.3.17. The lamp indications and output voltage signals shall comply with the requirements of 3.3.17.

4.6.1.18 System units OK logic. Apply the power form, input signals, and switch settings per paragraph 3.3.18. Verify the lamp indications meet the requirements of paragraph 3.3.18.

4.6.1.19 OUM1/OUM2 comparator logic. Apply the power form, input signals, and switch settings per paragraph 3.3.19. The lamp indications and output voltage signals shall comply with the requirements of 3.3.19.

4.6.1.20 DMTR1/DMTR2 comparator logic. Apply the power form, input signals, and switch settings per paragraph 3.3.20. The lamp indications and output voltage signals shall comply with the requirements of 3.3.20.

4.6.1.21 LMTR1/LMTR2/D_L comparator logic. Apply the power form, input signals, and switch settings per paragraph 3.3.21. The lamp indications and output voltage signals shall comply with the requirements of 3.3.21.

4.6.1.22 Phase outputs. Apply the power form, input signals, and switch settings per paragraph 3.3.22. The outputs shall be measured and verified to comply with the requirements of 3.3.22.

4.6.1.23 Computer lead-lock test logic. Apply the power form, input signals, and switch settings per paragraph 3.3.23. The lamp indications and output voltage signals shall comply with the requirements of 3.3.23.

4.6.1.24 Computer Phase 2 and 3 fail logic. Apply the power form, input signals, and switch settings per paragraph 3.3.24. The lamp indications and output voltage signals shall comply with the requirements of 3.3.24.

4.6.1.25 Computer feedback simulator circuit.

4.6.1.25.1 D feedback in outputs. Apply the power forms, input signals, interconnections, switch settings per paragraph 3.3.25.1. The outputs shall be measured and verified to comply with the requirements of paragraph 3.3.25.1.

4.6.1.25.2 D_I feedback in output. Apply the power forms, input signals, interconnections, switch settings per paragraph 3.3.25.2. The outputs shall be measured and verified to comply with the requirements of paragraph 3.3.25.2.

4.6.1.25.3 -E feedback in output. Apply the power forms, input signals, interconnections, switch settings per paragraph 3.3.25.3. The outputs shall be measured and verified to comply with the requirements of paragraph 3.3.25.3.

4.6.1.25.4 Phases 2, 3 and 5 feedback simulator outputs. Apply the power forms, input signals, interconnections, switch settings per paragraph 3.3.25.4. The outputs shall be measured and verified to comply with the requirements of paragraph 3.3.25.4.

4.6.1.26 Computer mode selection logic. Apply the power form and switch settings per paragraph 3.3.26. The outputs shall be measured and verified to comply with the requirements of paragraph 3.3.26.

4.6.1.27 AMMO select logic. Apply the power form and switch settings per paragraph 3.3.27. The outputs shall be measured and verified to comply with the requirements of paragraph 3.3.27.

4.6.1.28 GCU A10 card. Apply the power form and switch settings per paragraph 3.3.28. Verify the lamp indications meet the requirements of paragraph 3.3.28.

4.6.1.28.1 GCU potentiometer test circuit. Apply the power form and switch settings per paragraph 3.3.28.1. The outputs shall be measured and verified to comply with the requirements of paragraph 3.3.28.1.

4.6.1.29 A14 board load simulator outputs. Apply the power form and switch settings per paragraph 3.3.29. The outputs shall be measured and verified to comply with the requirements of paragraph 3.3.29.

4.6.1.30 GCU continuity test circuits. Apply the power form, input signals, interconnections, and switch settings per paragraph 3.3.30. The outputs shall be measured and verified to comply with the requirements of paragraph 3.3.30.

4.6.1.31 Computer continuity test circuit. Apply the power form, input signals, interconnections, and switch settings per paragraph 3.3.31. The outputs shall be measured and verified to comply with the requirements of paragraph 3.3.31.

4.6.1.32 AMMO test switch outputs. Apply the power form, input signals, and switch positions as specified in paragraph 3.3.32. The outputs shall be measured and verified to comply with the requirements of paragraph 3.3.32.

4.6.2 Environmental conditions.

4.6.2.1 High temperature. Subject the assembly to the high temperature test specified in MIL-STD-810, Method 501, except storage temperature shall be 160°F for 48 hours. At the conclusion of the storage temperature test, stabilize the assembly at 100°F and subject it to the performance tests of Table XLIII. After testing, return the assembly to room temperature and subject it to the performance tests of Table XLIII.

4.6.2.2 Low temperature. Subject the assembly to the low temperature test specified in MIL-STD-810, Method 502. Maintain the temperature at -65°F for a period of 12 hours minimum. At the conclusion of the storage temperature test, stabilize the assembly at +40°F and subject it to the performance tests of Table XLIII. After testing, return the assembly to room temperature and subject the assembly to the performance tests of Table XLIII.

4.6.2.3 Vibration. Vibration A as specified in 4.6.2.3.1 shall be conducted only for first article inspection. Vibration B as specified in 4.6.2.4.2 shall be conducted only for quality conformance inspection.

4.6.2.3.1 Vibration A. Mount the assembly in a suitable vibration fixture and subject the assembly to the vibration test specified in MIL-STD-810, Method 514, General Procedures, with a double amplitude of 0.03 inch and a frequency range from 10 to 55 Hz and back to 10 Hz. The vibration amplitude shall have a tolerance of ±10%. The tolerance of the vibration frequency shall be ±2%, or ±1/2 Hz for frequencies below 25 Hz. Vibration sweeps shall be conducted with the duration of exposure not less than 80 minutes in each of three mutually perpendicular axes. At the conclusion of this test, subject the assembly to the performance tests in Table XLIII.

4.6.2.3.2 Vibration B. This test shall be conducted as in 4.6.2.3.1 except that the period of vibration shall be not less than 15 minutes in each axis.

4.6.2.4 Shock. Mount the assembly in a suitable shock fixture and subject it to the functional shock test for ground equipment specified in MIL-STD-810, Method 516, for a total of

three half sine wave shock pulses in both directions along three mutually perpendicular axes (18 shocks). Peak amplitude shall be 40 ± 4 g's with a time duration of 18 ± 3 msec in accordance with Figure 6. At the conclusion of this test, subject the assembly to the performance tests of Table XLIII. Repeat this test with peak amplitude of 100.0 ± 10.0 g's with a time duration of 1.5 ± 0.2 msec in accordance with Figure 6.

4.6.2.5 Temperature cycling. With power and loads of Table I applied, subject the assembly to the temperature profile specified in Figure 7. At the conclusion of this test, subject the assembly to the performance tests of Table XLIII.

4.6.3 General specifications. Verification of precedence or inspections required shall be performed by examination, visually or through the use of standard measuring equipment, in accordance with MIL-F-13926 and MIL-STD-454, requirement 9, or as applicable.

4.6.4 Packaging inspection. The sampling and inspection of the preservation, packaging, packing and container marking shall be in accordance with MIL-STD-2073-1.

5. PACKAGING

5.1 Packaging, packing and marking. Packaging, packing and marking shall be in accordance with MIL-STD-2073-1. The level of protection shall be specified in the procurement documents (see 4.5.5, 6.2 and 6.7).

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory.)

6.1 Intended use. The Test Set, Field in conjunction with the Computer PN 11732400 and the Gunner's Control Unit PN 11732854, is used in the field to test the subsystems of the M21 Computer PN 11732979, which is part of the M60A3 Tank Fire Control System.

6.2 Acquisition requirements. Acquisition documents must specify the following:

a. Title, number and date of this specification.

b. Issue of DODISS to be cited in the solicitation, and if required, the specific issue of individual documents referenced (see 2.1).

c. Inspection provisions for first article (see 6.3).

d. Applicable levels of preservation packaging, packing and container marking (see 5.1 and 6.7).

6.3 First article. The contracting officer should provide specific guidance to offerors for the submission of a first article sample to be tested as specified in 4.4.2. The contracting officer should also include specific instruction in acquisition documents regarding arrangements for examinations, approval of first article test results, and disposition of first articles. Invitations for bids should provide that the Government reserves the right to waive the requirement for samples for first article inspection to those bidders offering a product which has been previously acquired or tested by the Government, and that bidders offering such products, who wish to rely on such production or test, must furnish evidence with the bid that prior Government approval is presently appropriate for the pending contract. Bidders should not submit alternate bids unless specifically requested to do so in the solicitation.

6.4 Supersession. Previous revisions of MIL-T-48467(AR) were for the U.S. Army Armament, Research, Development, and Engineering Center's internal use only, and were not forwarded to the Naval Publications and Form Center for publication.

6.5 Submission of contractor inspection equipment designs for approval. Submit copies of designs as required to: Commander, U.S. Army ARDEC, ATTN: SMCAR-QAF-I, Picatinny Arsenal, NJ 07806-5000. This address will be specified on the Contract Data Requirements List, DD Form 1423 in the contract.

6.6 Drawings. Drawings listed in Section 2 of this specification under the heading U.S. Army Armament, Research, Development and Engineering Center (ARDEC) may also include drawings prepared by, and identified as U.S. Army Armament, Research and Development Command (ARRADCOM), Frankford Arsenal, Rock Island Arsenal or Picatinny Arsenal. Technical data originally prepared by these activities is now under cognizance of ARDEC.

6.7 Levels of packaging. The following definitions describe the three levels of packaging in accordance with MIL-STD-2073-1.

a. Level A - Adequate protection for indeterminate storage and worldwide distribution.

b. Level B - Adequate protection for known shipment conditions and storage conditions normally not exceeding one year.

c. Level C - Adequate protection for shipment to a known site for immediate use.

6.8 Alternative quality conformance provisions. Alternative quality conformance procedures, methods, or equipment, such as statistical process control, tool control, other types of sampling procedures, etc., may be used by the contractor when they provide,

as a minimum, the level of quality assurance required by the provisions specified herein. Prior to applying such alternative procedures, methods, or equipment, the contractor shall describe them in a written proposal submitted to the Government for evaluation. When required, the contractor shall demonstrate that the effectiveness of each proposed alternative is equal to or better than the specified quality assurance provision(s) herein. In cases of dispute as to whether the contractor's proposed alternative(s) provides equivalent assurance, the provisions of this specification shall apply. All approved alternative provisions shall be specifically incorporated into the contractor's quality program or detailed inspection system, as applicable. Unless otherwise specified in the contract, proposed alternative quality conformance provisions will be submitted by the contractor for evaluation by the Government technical activity.

6.9 Subject (key word) listing.

Fire Control
Tank, M60A3
Logic functions
Simulator functions

Custodian:
Army-AR

Preparing activity:
Army-AR

(Project 1240-0004)

STANDARDIZATION DOCUMENT IMPROVEMENT PROPOSAL

INSTRUCTIONS

1. The preparing activity must complete blocks 1, 2, 3, and 8. In block 1, both the document number and revision letter should be given.
2. The submitter of this form must complete blocks 4, 5, 6, and 7.
3. The preparing activity must provide a reply within 30 days from receipt of the form.

NOTE: This form may not be used to request copies of documents, nor to request waivers, or clarification of requirements on current contracts. Comments submitted on this form do not constitute or imply authorization to waive any portion of the referenced document(s) or to amend contractual requirements.

I RECOMMEND A CHANGE:	1. DOCUMENT NUMBER	2. DOCUMENT DATE (YYMMDD)
	MIL-T-48467C(AR)	950501

3. DOCUMENT TITLE: TEST SET, FIELD

4. NATURE OF CHANGE (*Identify paragraph number and include proposed rewrite, if possible. Attach extra sheets if needed.*)

5. REASON FOR RECOMMENDATION

6. SUBMITTER

a. NAME (*Last, First, Middle Initial*)	b. ORGANIZATION	
c. ADDRESS (*Include Zip Code*)	d. TELEPHONE (*Include Area Code*) (1) Commercial (2) AUTOVON (*If applicable*)	7. DATE SUBMITTED (YYMMDD)

8. PREPARING ACTIVITY

a. NAME	b. TELEPHONE (*Include Area Code*)	
U.S. ARMY ARDEC STANDARDIZATION OFFICE	(1) Commercial 201-724-6629	(2) AUTOVON DSN-880-6629
c. ADDRESS (*Include Zip Code*) ATTN: AMSTA-AR-EDE-S PICATINNY ARSENAL, NJ 07806-5000	IF YOU DO NOT RECEIVE A REPLY WITHIN 45 DAYS, CONTACT: Defense Quality and Standardization Office 5203 Leesburg Pike, Suite 1403, Falls Church, VA 22041-3466 Telephone (703) 756-2340 AUTOVON 289-2340	