The documentation and process conversion measures necessary to comply with this revision shall be completed by 15 January 1995

INCH-POUND

MIL-S-19500J
15 April 1994
SUPERSEDING
MIL-S-19500H
30 April 1990

MILITARY SPECIFICATION

SEMICONDUCTOR DEVICES,

GENERAL SPECIFICATION FOR

This specification is approved for use by all Departments and Agencies of the Department of Defense.

## 1. SCOPE

* 1.1 Scope. This specification establishes the general requirements for semiconductor devices. Detail requirements and characteristics are specified in the detail specification. Four levels of product assurance requirements for encapsulated devices are provided for in this specification, differentiated by the prefixes JAN, JANTX, JANTXV, and JANS (see table Ia). Seven radiation hardness assurance (RHA) levels are provided for JANTXV and JANS product assurance levels (see table Ib). These are designated by the letters M, D, L, R, F, G, and H following the product assurance identifier portion of the prefix. Two levels of product assurance requirements for unencapsulated devices are provided for in this specification, differentiated by the prefixes JANHC and JANKC. A parts per million (PPM) quality system is used for documenting and reporting the average outgoing quality of discrete semiconductor devices supplied to this specification, except for devices which are inactive for new design. Statistical process control (SPC) techniques are required in the manufacturing process to minimize variation in production of discrete semiconductor devices supplied to the requirements of this specification.

* 1.2 Identification. The identification for semiconductor devices furnished under this specification shall be formulated as follows:

| JAN | A | XN | YYYY | ZZ |
|---|---|---|---|---|
| Product assurance level and JAN brand (see 1.2.1) | Alpha identification for JANKC and JANHC only (see appendix H 30.1) | Component designation (see 1.2.2) | Identification number (see 1.2.3) | Suffix letters (see 1.2.4) |

* Beneficial comments (recommendations, additions, deletions) and any pertinent data which may be of use in improving this document should be addressed to: Commander, Defense Electronics Supply Center, ATTN: DESC-ELDT, 1507 Wilmington Pike, Dayton, OH 45444-5765, using the Standardization Document Improvement Proposal (DD Form 1426) appearing at the end of this document or by letter.

AMSC N/A
FSC 5961

* 1.2.1 Prefix. The following prefixes shall be used as applicable (see tables Ia and Ib).

| Product assurance portion of the basic prefix for encapsulated devices | | | | |
|---|---|---|---|---|
| Radiation designators | JAN | JANTX | JANTXV | JANS |
| M | N/A | N/A | JANTXVM | JANSM |
| D | N/A | N/A | JANTXVD | JANSD |
| L | N/A | N/A | JANTXVL | JANSL |
| R | N/A | N/A | JANTXVR | JANSR |
| F | N/A | N/A | JANTXVF | JANSF |
| G | N/A | N/A | JANTXVG | JANSG |
| H | N/A | N/A | JANTXVH | JANSH |

| Product assurance portion of the basic prefix for unencapsulated devices | | |
|---|---|---|
| Radiation designators | JANHC | JANKC |
| M | JANHCM | JANKCM |
| D | JANHCD | JANKCD |
| L | JANHCL | JANKCL |
| R | JANHCR | JANKCR |
| F | JANHCF | JANKCF |
| G | JANHCG | JANKCG |
| H | JANHCH | JANKCH |

* 1.2.1.1 Level of product assurance. The levels of product assurance (listed above) for encapsulated devices from the lowest level to the highest level shall be JAN, JANTX, JANTXV, and JANS. A higher assurance level product is substitutable for a lower assurance level product.

* 1.2.1.1.1 Devices substitutions. A device of a higher product assurance level may be substitute for the same basic part number device of a lower product assurance level. Product assurance levels, in descending order of assurance are: JANS, JANTXV, JANTX, and JAN. RHA devices tested to a higher total dose requirement may be substituted for the same basic part number device with a lower total dose requirement (see table Ib). For axial leaded diodes, where the same part number both with, and without a dash one (-1) suffix, the dash one device is considered to be a higher assurance level and may be substituted for the non-dash one part. For those devices selected to voltage tolerances (e.g., zener diodes, transient voltage suppressors) the tighter tolerance device may be substituted for one of more relaxed tolerance. Nondash one devices are inactive for new design (whenever dash-one devices exist) and dash-one devices shall be used in lieu of nondash-one devices. JANTX'P' devices are substitutable for JANTX devices and JANTXV'P' devices are substitutable for JANTXV devices. Devices having suffix letters L or S or no lead length designator, may be substituted for each other in applications where the alternate lead length will fit.

1.2.1.2 Unencapsulated devices. Two levels of unencapsulated devices designated JANHC and JANKC are available. The requirements and quality conformance inspection (QCI) are as specified in appendix H. Information on a specific device will be as specified in the associated detail specification for that device.

1.2.2 Component designation. Semiconductor devices are identified by the prefix "XN". An "X" will usually be a number that is one less than the number of active element terminations.

1.2.3 Identification number. It is recommended that each type of semiconductor device intended for standardization be assigned an identification, serially, by the Joint Electron Device Engineering Council, a council sponsored by the Electronic Industries Association (EIA) and the National Electrical Manufacturers Association. The assignment will provide the component designation the identification number.

* 1.2.4 Suffix letters. The following suffix letters may be incorporated in the military type number as applicable.

| | |
|---|---|
| A, B, C, etc. (except L, M, P, R, S, U) | Indicates a modified version which is substitutable for the basic numbered (nonsuffix) device. |
| M | Indicates matching of specified parameters of separate devices. |
| R | Indicates reverse polarity packaging of the basic numbered device. |
| L or S | Indicates that the terminal leads are longer or shorter, respectively, than those of the basic numbered device. |
| U | Indicates unleaded or surface mounted devices. |
| P | Indicates particle impact noise detection (PIND) screened devices (for JANTX and JANTXV only). |
| UR | Indicates unleaded or surface mounted (round end cap diodes). |
| US | Indicates unleaded or surface mounted (square end cap diodes). |

Suffix letter(s) except for P suffix, shall be used and marked on the device only when specific device types are covered by the applicable associated detail specification requiring the suffix letters (see 3.7.3 and 3.7.6.1).

2. APPLICABLE DOCUMENTS

2.1 Government documents.

2.1.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DODISS) and supplement thereto, cited in the solicitation (see 6.2).

*SPECIFICATION*

MILITARY

MIL-S-19491 - Semiconductor Devices, Packaging of.

STANDARDS

FEDERAL

FED-STD-H28 - Screw-Thread Standards for Federal Services.

MILITARY

MIL-STD-750 - Test Methods for Semiconductor Devices.
MIL-STD-45662 - Calibration Systems Requirements.

(Unless otherwise indicated, copies of federal and military specifications, standards, and handbooks are available from the Defense Printing Service Detachment Offices, Building 40 (Customer Service), 700 Robbins Avenue, Philadelphia, PA 19111-5094.)

2.1.2 Other Government documents, drawings, and publications. The following other Government documents, drawings, and publications form a part of this document to the extent specified herein. Unless otherwise specified, the issues are those cited in the solicitation.

| | | |
|---|---|---|
| DLAM 8200 | - | Procurement Quality Assurance Support Manual for Defense Contract Administration Services. |
| NAVSHIPS 0967-LP-190-4010 | - | Electronic Equipment PAV-1A, -2A, and -3A Manufacture Designating Symbols for Navy Type Numbers and Plates for, TM. |

* 2.2 Non-Government publications. The following documents form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents which are DoD adopted shall be those listed in the issue of the DODISS cited in the solicitation. Unless otherwise specified, the issues of documents not listed in the DODISS are the issues of the documents cited in the solicitation (see 6.2).

ELECTRONIC INDUSTRIES ASSOCIATION (EIA)

| | | |
|---|---|---|
| EIA-554 | - | Assessment of Outgoing Nonconforming Levels in Part Per Million (PPM) (DOD adopted). |
| EIA-557 | - | Statistical Process Control Systems. |
| JEDEC Publication 108 | - | Distributor Requirements for Handling Electrostatic Discharge Sensitive (ESDS) Devices. |
| JEDEC Publication 109 | - | General Requirement for Distributors. |
| JEDEC Publication 114 | - | Analysis of Component PIND Test Failures. |

(Application for copies should be addressed to the Electronic Industries Association, 2001 Pennsylvania Avenue, Washington, DC 20006.)

(Non-Government standards and other publications are normally available from the organizations which prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

2.3 Order of precedence. In the event of a conflict between the text of this document and the references cited herein the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

## 3. REQUIREMENTS

* 3.1 General requirements. The individual device requirements shall be as specified herein and in accordance with the applicable associated detail specification. The general requirements of referenced documents shall also apply. Only devices or die listed or approved for listing on the Qualified Products List (QPL) which are inspected for and meet all the requirements of the applicable associated detail specification for the applicable product assurance level shall be marked and delivered as JAN, JANTX, JANTXV, JANTXVM, JANTXVD, JANTXVL, JANTXVR, JANTXVF, JANTXVG, JANTXVH, JANS, JANSM, JANSD, JANSL, JANSR, JANSF, JANSG, or JANSH devices, JANHC or JANKC dies. Government source inspection shall be required (see 4.1.1). Unless otherwise specified, all JANTXV requirements apply to JANTXVM, JANTXVD, JANTXVL, JANTXVR, JANTXVF, JANTXVG, and JANTXVH devices and all JANS requirements apply to JANSM, JANSD, JANSL, JANSR, JANSF, JANSG, and JANSH devices.

* 3.2 Conflicting requirements. Nothing in this document or the documents referenced herein supersedes applicable laws or regulations unless a specific exemption has been obtained. In the event of conflict between the requirements of this specification and the requirements contained in the associated detail specification or other referenced documents, the following order of precedence shall apply:

First: The associated detail specification.

Second: This specification.

Third: Applicable documents as specified in 2.0.

Fourth: Other Government, industry, and manufacturer specifications, standards, and data sheets.

* 3.2.1 Reference to associated detail specification. For purposes of this specification, when the term "specified" is used without reference to a specific document, the intended reference is to the associated detail specification.

3.3 Qualification. Devices furnished under this specification shall be products which have been listed on or approved for listing on the QPL (see 4.5).

* 3.3.1 Certification of conformance and acquisition traceability. Manufacturers who offer the products as described in this specification shall provide written certification signed by the company or corporate official who has management responsibility for the production of the products, (1) that the product being supplied has been manufactured and tested in accordance with this specification and conforms to all of the requirements as specified herein, (2) that all products are as described on the certificate which accompanies the shipment. The responsible official may, by documented authorization, designate other responsible individuals to sign the certificate, but the responsibility for conformance to the facts shall rest with the responsible official. The certification shall be confirmed by documentation to the Government or to users with Government contracts or subcontracts, regardless of whether the products are acquired directly from the manufacturer or from another source such as a distributor. When other sources are involved, their acquisition certification shall be in addition to the certificates of conformance and acquisition traceability provided by the manufacturer and previous distributors. In no case shall the manufacturer's certificate be altered or show signs of alteration. The certificate shall include the following information:

a. Manufacturer documentation:

(1) Manufacturer's name and address.

(2) Customer's or distributor's name and address.

(3) Device type, product assurance level, and detail specification number.

(4) Lot identification code (including assembly plant code).

(5) Inspection date and latest reinspection date.

(6) Quantity of devices in shipment from manufacturer.

(7) Statement certifying product conformance and traceability.

(8) Signature and date of transaction.

(9) International standardization agreement (ISA) country's quality conformance mark.

b. Distributor documentation for each distributor:

(1) Distributor's name and address.

(2) Name and address of customer.

(3) Quantity of devices in shipment.

(4) Latest reinspection date, if applicable.

(5) Certification that this shipment is a part of the shipment covered by the manufacturer's documentation, and an attached copy of the manufacturer's original certification.

(6) Signature and date of transaction.

(7) Authorized dealers and distributors have handled the products in accordance with the requirements of JEDEC publications 108 and 109.

* 3.3.2 Qualification to RHA levels. Qualification to an RHA level shall consist of qualification to the appropriate product assurance level (JANTXV or JANS) plus group D inspections and tests (see table VI). RHA levels are defined in table Ib.

* 3.4 Product assurance requirements. Devices furnished under this specification shall comply with the applicable quality assurance provisions of section 4 herein, and shall be prepared for delivery in accordance with section 5. Quality assurance related to semiconductor sensitivity to electrostatic discharge (ESD) damage is provided for in this specification by categorizing semiconductors into three ESDS classes (classes 1, 2, and 3). In addition, seven RHA levels (M, D, L, R, F, G, and H) are provided for those semiconductors qualified to the radiation hardness levels as specified in 4.7.7. Product assurance requirements are summarized in tables Ia and Ib.

3.4.1 Requirements summary. Tables Ia and Ib summarize the product assurance and RHA levels and requirements. To offer any of the product assurance levels as specified in tables Ia or Ib, the manufacturer must use wafers that have been manufactured in its own United States wafer facility.

3.4.2 Product assurance program. As a precondition to manufacturer certification and device qualification, as applicable, the device manufacturer shall establish and implement a product assurance program as defined in appendix D. The manufacturer shall also submit a program plan for approval as specified in appendix D (see 30.1.2) and shall provide for a manufacturer facility survey by the qualifying activity. The product assurance program and program plan shall be subject to periodic review and audit by the Government to assure implementation, compliance, and extension on a 2-year basis by the qualifying activity.

3.4.2.1 Changes to the program documentation. After a manufacturer receives approval of its product assurance program, no changes in product design, material, process, or control shall be implemented without a concurrent change in the program documentation.

3.4.2.2 Manufacturer certification requirements for all product assurance levels. Manufacturers of semiconductor devices shall meet the requirements of 3.4.2 and also shall meet certification requirements for the specific production line or manufacturing and testing facility (or specified portions thereof). Certification requirements shall be as specified in section 40 of appendix D herein. When the qualifying activity determines on the basis of a manufacturer survey (see 3.4.2) that the manufacturer is eligible to qualify the product, the manufacturer shall receive written notification of such eligibility which shall specify the technologies and the associated facilities within the manufacturing locations that are certified. Certification is normally valid for 2 years and can only be terminated by written notification from the qualifying activity. During the duration of the certification, the manufacturer is subject to a periodic review by the qualifying activity or its representatives. Certification will not normally be extended beyond the 2-year period without a re-audit of the manufacturer's facility for compliance with this specification.

3.4.2.2.1 Certification audits. After initial certification, a certification audit team will periodically examine the manufacturer's facilities and equipment, review the processes and techniques, and audit the implementation of the product assurance program plan and records. The date, location, time of audit, and extent of participation of supplier personnel required to accomplish the task will be established on a schedule that is mutually acceptable to the qualifying activity or its representative and the manufacturer. On completion of the audit, the manufacturer will be provided an audit critique and will subsequently be provided with a written report of the results of such an audit. A schedule for correction of any significant deficiencies will be required and will subsequently be reviewed for completeness, adequacy, and timeliness of committed closure actions.

3.4.2.2.2 Loss of certification. Loss of certification for any certified line shall result in removal from the QPL of all applicable devices. The manufacturer may lose certification for failing to:

a. Have any semiconductor device from the certified line listed on the QPL within 2 years after date of certification.

b. Comply with the requirements of this specification.

c. Allow the certification team access to the operations and documentation as required by section 40 of appendix D.

3.4.2.2.3 Reinstatement of certification. Manufacturers may have certification reinstated by successfully completing all the requirements referred to in this specification, or portions thereof as directed by the qualifying activity in order to remedy the deficiencies and assure compliance with certification requirements.

* 3.4.3 Change of qualified product. After qualification, the manufacturer shall notify the qualifying activity prior to the release and shipment (for JANS prior to line implementation except for evaluation samples) of product which undergoes any change in the product or product assurance program which affects performance, quality, appearance, reliability, or interchangeability. Changes in design, materials, or processes for any device must be processed in accordance with established change control procedures for all affected documents (see 30.1.1.5 and 30.1.2 of appendix D). Such notification shall include a thorough description of the proposed change and a suggested test plan designed to demonstrate that the change will not adversely affect performance, quality, reliability, or interchangeability and that the changed product will continue to meet the specification requirements. The qualifying activity will review the proposed change and test plan and advise the manufacturer of the testing required to obtain approval of the proposed change. The completed test results shall be submitted to the qualifying activity for review and the manufacturer shall be notified of approval or disapproval. After approval of the design change, all product inventory of the old design must be submitted to QCI within 6 months, unless authorization is extended by the qualifying agency. Unless the design change has been required to correct or eliminate a verified design defect, finished devices manufactured to the previously approved design which are in inventory or in process of testing (i.e., inspection lot identification code assigned) will remain qualified only until that inventory is depleted. The previously approved design will not remain qualified if the design change has been required to correct or eliminate a verified design defect. Changes representative of those that are subject to this requirement are those shown in table Ic.

* 3.4.3.1 Allowable alternate design, materials, and construction. Only one device design is allowed for JANTX and JANTXV per manufacturer. For JANS devices, only one design is allowed per manufacturer, and it may differ from the design of other product assurance levels. For radiation hardened devices of all levels, only one design is allowed, and it may differ from the design of nonradiation hardened devices. With the approval of the qualifying activity (see 3.4.3), design material and construction alternatives for qualified device types may be allowed only for a limited time. An alternate design submitted for approval must be definitive of all pertinent construction features. Particular design features are not interchangeable between approved designs. A single inspection lot or sublot, in the case of lots made up of sublots of structurally identical devices, shall contain only one approved design, material and construction so that homogeneity is preserved within a given lot identification code and device type. The qualifying activity shall be notified of the first lot incorporating the change and the last lot of the present existing design and effective date codes for each. If the existing design is to be maintained, the manufacturer shall justify the retention, subject to approval by the qualifying activity. The qualifying activity may periodically identify specific alternate designs by device type and detail specification and request justification for continued retention of that specific alternate design.

3.4.4 Government source inspection. Government source inspection and acceptance in accordance with table Ia and appendix D is required on all "JAN" branded semiconductors delivered to this specification. The inspection shall be performed by the designated Government agency (see 4.1.1).

* 3.4.5 PPM quality levels. The quality of lots that have been subjected to and have passed the 100 percent screening inspections of table II (or unscreened devices at the option of the manufacturer) shall be established and maintained in accordance with 4.7.4.1 and EIA-554. Individual PPM levels for PPM-2 shall be computed for table III, subgroups 2, 3, and 4 and be reported individually for each subgroup. The sum of these shall be reported as the overall PPM-5 defect level. Data collection must begin by 30 July 1991, for subgroups 2, 3, and 4. Data reporting shall be available upon request.

3.5 Terms, definitions, abbreviations, and symbols. For the purpose of common understanding, usage, preparation of associated detail specifications, and the recording of data, the terms, definitions, abbreviations, and symbols contained herein, in the appendixes, referenced documents, and in the associated detail specifications shall apply.

3.6 Design, construction, and materials. Design, construction, and materials for devices furnished under this specification shall be as specified herein or as specified in the associated detail specification.

3.6.1 Package. All packaged devices supplied under this specification shall be hermetically sealed in glass, metal, or ceramic (or combinations of these) packages. No organic or polymeric material shall be used as a package or package seal.

* 3.6.1.1 Moisture content. The moisture content of the sealing environment shall be controlled. The internal moisture content of device packages with an internal cavity greater than .01 cc shall not exceed 5,000 PPM when tested in accordance with method 1018 at +100°C. All manufacturers shall exercise package internal moisture content monitors at key locations in the manufacturing flow. The internal water-vapor content test may be performed at the option of the manufacturers. When the internal water-vapor content test is performed, the samples shall have been subjected to screen 3 of table II, or equivalent; not required for devices which are inactive for new design.

3.6.1.2 Oxygen content. All power devices with soft solder die attach shall have the internal oxygen content of the sealing environment controlled. The internal oxygen content of the device package shall not exceed 2,000 PPM at +100°C. The internal oxygen content test may be performed at the option of the manufacturers. When the internal content test is performed, the samples shall have been subjected to screen 3 of table II or equivalent; not required for devices which are inactive for new design.

* 3.6.2 Fungus-resistant material. External parts of the semiconductor device shall be inherently nonnutrient to fungus.

* 3.6.3 Metals. Internal surfaces shall be capable of resisting progressive degradation within a hermetically sealed package. External metal surfaces shall be corrosion resistant or shall be plated or treated to resist corrosion. Device package material shall be free of burrs and other potential particle contamination.

3.6.4 Screw threads. Standard screw threads listed in FED-STD-H28 shall be required for all semiconductor devices where screw threads are a mechanical requirement of the device.

* 3.6.5 Internal conductors. Internal conductors which are in thermal contact with a substrate along their entire lengths (such as metallization strips, contact areas, and bonding interfaces) shall be designed so that no properly fabricated conductor shall experience, at device maximum rated current, a current density in excess of the values shown below for the applicable conductor material including allowances for worst case conductor composition, cross-sectional area, normal production tolerances on design dimensions, and actual thickness at critical areas, such as, steps in the elevation or contact windows:

| Conductor material | Maximum allowable continuous current density (RMS for pulse applications) |
|---|---|
| Aluminum (99.99 percent pure or doped) without glassivation | $2 \times 10^5$ amps/cm$^2$ |
| Aluminum (99.99 percent pure or doped) with glassivation | $5 \times 10^5$ amps/cm$^2$ |
| Gold | $6 \times 10^5$ amps/cm$^2$ |
| All other (unless otherwise specified) | $2 \times 10^5$ amps/cm$^2$ |

3.6.5.1 Wire bonds. Thermocompression wedge bonds shall not be utilized when aluminum wire is used.

3.6.5.2 Die mounting. Pure glass shall not be used for device die mounting.

3.6.6 Silicon transistor metallization protective coating. All silicon transistors with "maximum rating" of less than 4 watts at $T_C$ of +25°C, shall have an inorganic transparent protective overlay material on the active metallization (excluding the bonding pads). For JANS devices, the minimum deposited glassivation thickness shall be 6,000 Å of $SiO_2$ or 2,000 Å of $Si_3N_4$. The glassivation shall cover all electrical conductors on the chip except the bonding pads. For JANS devices, a minimum of 0.050 mm (2 mils) distance shall be maintained between all uncoated conducting paths, except where the functional performance parameters of the device require closer spacing.

* 3.6.7 Material restrictions. The external surface of package, header, or flange shall be finished and not have any depression or cavity, unless it is part of the original design. External parts, elements, or coatings shall not blister, crack, (excluding glass meniscus), outgas, soften, flow, or exhibit defects that adversely affect storage, operation, or environmental capabilities of semiconductor devices. Organic or polymeric materials shall not be used external to the package to increase size or dimensions. For JAN, JANTX, and JANTXV the use of silicone or organic material inside the packages, shall be approved by the qualifying activity. Desiccants shall not be used. For JANTX, JANTXV, or JANS devices, silicone or organic materials may be used. For JANS devices, silicone or organic materials may only be used when specified by the associated detail specification. For JANTX, JANTXV, or JANS, the qualifying activity shall evaluate processing conditions of the materials before granting approval. Polymer impregnations (backfill, etc.) of the packages shall not be permitted.

* WARNING: Packages containing beryllium oxide (BeO) shall be marked in accordance with 3.7.3.2 and shall not be ground, machined, sandblasted, or subjected to any mechanical operation which will produce dust containing any beryllium compound. Packages containing any beryllium compound shall not be subjected to any chemical process (etching, etc.) which will produce fumes containing beryllium or its' compounds.

* 3.6.7.1 Organic materials and silicones. If organic materials and silicones are used inside the package, approval of the qualifying activity shall be required and the following information shall be provided to the qualifying activity for approval consideration:

a. Identification of the specific material(s) and manufacturer(s).

b. Details of the application cure cycle, preseal bake, seal, and any other special processing required. (Maximum curing temperature shall not be exceeded after curing).

c. A brush shall not be used to apply organic material or silicone. Any wire bonded device with an excessive buildup of organic material or silicones beyond a normal fillet under the heel of the bond wire is prohibited.

d. Five randomly selected devices shall be provided for moisture content and contamination analysis.

* 3.6.8 Metallurgical bond for JANS axial diodes. All JANS diodes (excluding Schottky barrier and point contact ultra high frequency (UHF) devices) shall be metallurgically bonded at the interface of any mechanical connection within the assembly of the device (see 30.14.3 of appendix A for axial lead diodes).

3.6.9 Requirements for JANS transistor structure.

3.6.9.1 Metallization thickness. The minimum metallization thickness shall be 8,000 A.

* 3.6.9.2 Internal wire size. The internal wire diameter shall be .0009 inch (0.023 mm) minimum for aluminum and .0007 inch (.018 mm) minimum for gold wire.

3.7 Marking.

3.7.1 Marking on each device. The following marking shall be placed on each encapsulated semiconductor device and shall be legible at time of shipment.

a. Polarity marking, when applicable (see 3.7.5).

b. Type designation (see 3.7.6).

c. Product assurance level. The P suffix (when applicable, see 3.7.3).

d. ISA country's quality conformance mark (when applicable, see 3.7.6.1).

e. Manufacturer's name, trademark, or identification (see 3.7.10) and/or manufacturer's designating symbol (see 3.7.7).

f. Lot identification code and code of assembly plant (see 3.7.8 and 3.7.8.1).

g. Serial number, if applicable (see 3.7.9).

h. "1N" portion of the Part or Identifying Number (PIN) of an axial leaded or surface mount glass diode.

i. Electrostatic discharge sensitivity (ESDS) identifier (see 3.7.3.1).

j. Country of origin (see 3.7.8.2).

k. Special marking (see 3.7.3). Beryllium oxide identifier (see 3.7.3.2).

The maximum marking commensurate with device size and the above order of precedence shall apply.

3.7.2 Marking on initial container (unit package). All device marking, except for polarity and serial numbers, shall also appear on the unit package used as the initial protection for delivery.

3.7.3 Special marking. If any special marking is used, it shall in no way interfere with or obscure the marking required in 3.7.1. The "P" suffix marking for PIND testing (see 1.2.4 and 3.7.6.1) may follow the type number or be marked any place on the device within the marking area.

* 3.7.3.1 ESDS identifier. When a device's ESDS class is determined by the ESDS classification test (see 4.5.2.1 and 4.5.2.2), the devices represented by the test shall be marked as follows:

a. Class 1: 1,999 V and below - $\Delta$ - single equilateral triangle outline or solid (still acceptable as pin one designator).

b. Class 2: 2,000 V to 3,999 V - $\Delta\Delta$ - double equilateral triangle outline or solid (still acceptable as pin one designator).

c. Class 3: 4,000 V to 15,999 V - no designator.

* d. Nonsensitive: Above 15,999 V - no designator.

3.7.3.2 Beryllium oxide package identifier. If a semiconductor package contains beryllium oxide (beryllia), the device shall be marked with the designation 'BeO'.

* 3.7.4 Marking legibility. Marking shall remain legible after all tests. Marking damage caused by mechanical fixturing shall not be cause for lot rejection. Devices having damaged markings shall be remarked prior to shipment to insure legibility.

3.7.5 Polarity marking of unidirectional diodes and thyristors. The polarity shall be indicated by one of the following methods.

3.7.5.1 Diodes.

a. A diode graphic symbol or arrow with the arrow pointing toward the cathode terminal for forward bias.

b. A single contrasting color band or a minimum of three contrasting color dots spaced around the periphery on the cathode end may be used.

c. An ESD identifier may be used to indicate polarity for sensitive devices.

3.7.5.2 Thyristors. A graphic symbol for a thyristor with the arrow pointing toward the cathode terminal (for stud-mounted thyristors only).

3.7.6 Type designation. Each semiconductor device shall be marked with the type designation which shall be formulated as shown in 1.2.

* 3.7.6.1 JAN branded prefix. The type number of all semiconductor devices acquired to and meeting the requirements of this specification and the applicable associated detail specification shall bear the applicable prefix (if manufactured in the U.S.). See 1.2.1 for available prefixes. In the case of small size semiconductor devices, the abbreviated prefix J, JX, JV, JVM, JVD, JVL, JVR, JVG, JVF, JVH, JS, JSM, JSD, JSL, JSR, JVF, JVG, or JSH may be used.

* 3.7.6.1.1 The JAN brand registered U.S. Government certification mark. The JAN brand is a registered U.S. Government certification mark as number 504860 by the U.S. Patent Office, and its application shall constitute certification by the manufacturer that all tests of the applicable associated detail specification and this specification have been satisfactorily completed; that verifiable test data will be retained in files for not less than 5 years; and that within the specified time period, test data will be made available for on-site review by Government representatives upon request. In the event that a lot fails to pass inspection, the manufacturer shall remove or obliterate within 30 days the JAN or J prefix from the sample tested and also from all devices represented by the sample.

* 3.7.6.1.2 ISA certification mark. For product totally manufactured outside the U.S. under a ratified ISA, the quality conformance certification mark of the country in which the product was manufactured shall be used in place of the JAN brand, except when the JAN certification mark is actually a part of the military PIN. Then the ISA certification mark shall be marked on the device in addition to the JAN prefix.

* 3.7.6.1.3 Purchase order requirements. The JAN brand or the abbreviations shall not be used on any semiconductor device acquired under contracts which permit or require any changes to this specification or the applicable associated detail specification, except for:

a. Lead length.

b. Finish.

c. PIND testing. PIND screening to requirements beyond those specified herein may be performed only when imposed by the acquisition document upon the component manufacturer. A new PIN will be created in accordance with 1.2.4 and 3.7.3. Devices which pass such screens may be JAN branded or may retain the JAN brand if already marked. All devices failing such screens shall not be JAN branded or, if already marked shall have the JAN brand removed or the device destroyed.

d. Lead forming. The forming of leads shall not be performed except for specific customer purchase orders where the lot is controlled throughout processing by specific lot travelers. The bend shall not be closer than .050 inch (1.27 mm) to the glass seal. If lead forming is performed, a hermeticity test shall be performed in accordance with table II, screen 7.

* 3.7.6.2 RHA designator. The letters M, D, L, R, F, G, and H following the JV or JS portion of the JAN prefix indicate the level of RHA. Parts which do not have an RHA designator either have not been tested for, or have not passed RHA testing.

* 3.7.7 Manufacturer's designating symbol. The manufacturer's designating symbol (NAVSHIPS 0967-LP-190-4010) shall be as listed in the QPL and assigned by the qualifying activity. The symbol shall be used only by the manufacturer to whom it has been assigned and only on those devices manufactured at that manufacturer's plant. In the case of small devices, the manufacturer's designating symbol may be abbreviated by omitting the first "C" in the series of letters.

3.7.8 Lot identification code. Semiconductor devices shall be marked by a code indicating the last week of sealing for the inspection lot accumulation period. The first two numbers in the code shall be the last two digits of the number of the year. The third and fourth numbers shall be two digits indicating the calendar week of the year. When the number of the week is a single digit, it shall be preceded by a zero. Reading from left to right or top to bottom, the code number shall designate the year and week. When more than one lot of a device type sealed within the same 6-week period is submitted for QCI, a lot identification suffix letter shall be chosen, consisting of a single capital letter, and shall appear on each semiconductor device immediately following the date code. This letter shall be chosen by the manufacturer so that each inspection lot is uniquely identified by the lot identification code and by the lot identification suffix letter, if one is required. In addition, for JANS, each device shall be traceable to a wafer lot.

3.7.8.1 Code for assembly plants. If the devices are assembled at an assembly plant other than the basic plant, the lot identification code shall include a single letter which uniquely identifies the plant or country where the assembly plant is located. When the full name of the country of assembly in which the device is assembled is marked on the device, the letter code is not required. This assembly plant designator shall appear immediately preceding and adjacent to the date code. The assembly plant designators will be listed with the addresses in the QPL.

* 3.7.8.2 Country of origin. Country of origin if other than USA, determination and markings for semiconductor devices made in a foreign country shall be in accordance with United States Customs rulings.

3.7.9 Serialization. JANS devices and, when specified, other device levels shall be marked with a unique serial number assigned consecutively within the inspection lot. JANS devices shall be marked with the serial number prior to the first electrical test in screening, and inspection lot records shall be maintained to provide traceability from the serial number to the specific wafer inspection lot from which the devices originated. For small devices with insufficient area for serialization, metal lead or body tags may be used.

* 3.7.10 Manufacturer's name, abbreviation, or trademark. At the manufacturer's option, devices supplied to this specification may be marked with the device manufacturer's name, abbreviation, or trademark in place of the designating symbol described in 3.7.7, except for a manufacturer with multiple facility locations. The identification of the equipment manufacturer may appear on the device only if the equipment manufacturer is also the device manufacturer. The name or trademark of only the original manufacturer shall appear on the device or initial container. Rebranding shall not be permitted.

3.7.11 Marking option. Except for serialization, the manufacturer has the option of marking the entire lot or only the sample devices prior to inspection. If the manufacturer exercises the option to mark only the sample devices, the procedure shall be as follows:

a. The sample devices shall be marked prior to performance of quality conformance or qualification inspection.

* b. At the completion of inspection, the marking of the sample devices shall be inspected for conformance with the requirements of 3.7.1 and 3.7.4.

c. The inspection lot represented by a conforming inspection sample shall then be marked and any specified visual and mechanical inspection performed.

d. The marking materials and processing applied to the inspection lot shall be to the same specification as those used for the inspection sample.

* 3.8 Workmanship. Semiconductor devices shall be manufactured and processed in a careful and workmanlike manner, in accordance with good design and sound engineering practice, and to the requirements of this specification.

3.8.1 Lead finish. The finish system on all external leads or terminals shall conform to one of the combinations listed in table Id and to the thickness and composition requirements of table Ie. The finish system shall also conform to the requirements of 3.8.1.2 and 3.8.1.4 where applicable. Lead finish requirements are not applicable to specifications which are inactive for new design.

3.8.1.1 Package element (other than lead or terminal) finish. External metallic package elements other than leads and terminals (e.g., lids, covers, bases, and seal rings) shall meet the applicable environmental requirements without additional finishing of the base materials or else they shall be finished so they meet those requirements using a finish system conforming to one of the combinations listed in table If, and conforming to the thickness and composition requirements of table Ie. The finish system shall also conform to the requirements of 3.8.1.2 and 3.8.1.4.

3.8.1.2 Hot solder dip. The hot solder dip shall be homogeneous and shall be applied as follows:

* a. All outlines with hot solder dip over compliant coating. The hot solder dip shall extend to within 0.05 inch (1.27 mm) of the seating plate (minimum). For leadless chip carrier devices, the hot solder dip shall cover a minimum of 95 percent of the metallized side castellation or notch and metallized areas above and below the notch, except the index feature if not connected to the castellation. Terminal area intended for device mounting shall be completely covered as required by MIL-STD-750 solderability test. For stud mount the solder shall extend .050 inch minimum below the terminal hole.

b. All outlines with hot solder dip over base metal, or noncompliant coating (which are subject to corrosion resulting in lead degradation). The solder shall extend to the glass seal or point of emergence of the metallized contact or lead through the package wall. If solder is applied up to the seal, a hermeticity test (method 1071, sample size (116 devices, c = 0)) shall subsequently be performed and passed. An external visual examination (method 2068, sample size (116 devices, c = 0)) may be performed in lieu of the hermeticity test for non-transparent glass encased double plug noncavity axial lead diodes. Alternately, the hot solder dip may extend to within 0.05 inch (1.27 mm) of the seating plane (minimum), provided a salt atmosphere test method 1041 sample plan 22 devices, c = 0 subsequently be performed and passed. For leadless chip carrier devices, the hot solder dip shall completely cover the metallized side castellation or notch an metallized areas above and below the notch, except the index feature if not connected to the castellation.

3.8.1.3 Silver. The lead may be solid silver or the lead finish may be silver clad or silver plated. The silver shall be a minimum of 99.7 percent pure. Silver cladding thickness shall be a minimum of 250 microinches (6.35 $\mu$m). A matte or semi-bright plated finish is allowed. The silver plating thickness shall be a minimum of 100 microinches (2.54 $\mu$m) and a maximum of 425 microinches (10.80 $\mu$m). Silver plating as a final finish, shall not be used directly over copper.

* 3.8.1.4 Tin and tin-lead plate. Pure tin finish shall not be used on any internal or external package or lead surface. Lead finish shall not use pure tin. Tin-lead plate shall contain three percent lead as a minimum (see table Ie). Pure tin finish (including pure tin undercoating) shall be prohibited. For JAN level, pure tin is acceptable in accordance with table Ie. herein.

3.8.2 Rework provisions. All rework permitted on devices manufactured under this specification shall be accomplished in accordance with procedures and safeguards documented in accordance with appendix D and available for review by the qualifying or acquiring activity. No delidding or package opening for rework shall be permitted except disc packages. Unless otherwise specified, allowable rework of sealed package includes recleaning of any device or portion thereof, rebranding to correct defective marking and lead straightening (provided the reworked devices meet the requirements for conditions of leads). For discrete semiconductor wafers, rework (i.e., the strip and redeposition of a layer in order to correct a nonconformance to a specification limit) is not allowed. Additional etch to correct a nonconformance to a specification limit, photoresist strip and recoat, or processing to continue or finish incomplete processing, strip and redeposit of non-junction passivation and backside metallization is considered acceptable rework. However, investigative and correction action shall be performed. For JANS additional deposition of oxidation, passivation, or any interconnect layers (e.g., polysilicon, aluminum, etc.), and any assembly rework operation prior to package seal is not allowed. After replating of the package or leads, all JANS, JANTXV, and JANTX devices shall be subjected to and pass as a 100 percent screen, the final electrical test requirements of screen 13 of table II for the device class (excluding calculation of delta limits) and the hermetic seal requirements of screen 7 of table II. Solder-dip rework shall be in accordance with 3.8.1.2. Subsequent screening of lot testing may be used to satisfy these requirements. Lots shall not exceed two reworks for any process (e.g., chemical stripping to achieve solderability).

3.9 Location of manufacturer.

3.9.1 Location of manufacturer for JANS and JANTXV types. For JANS and JANTXV devices, wafer processing, device assembly, 100 percent screening test, (except clear glass JANTXV diodes) and groups A, B, C, D, and E inspections shall be performed in the U.S.A. or its territories, using wafers processed in their own United States manufacturing facility (see 3.9.2). However, 100 percent screening (table II) for JANTXV types may be performed in those countries that have ratified an ISA with the U.S.A. (e.g., NATO STANAG no. 4093 or DoDI 2045).

3.9.2 Location of manufacturer for JAN, JANTX, and clear glass diode, JANTXV types. Provided the requirements of Foreign Plant Qualification Provisions (see appendix E) are satisfied, JAN and JANTX devices and clear glass JANTXV diodes may be assembled in a foreign country provided that the foreign assembly plant is technically controlled by basic facility with quality assurance procedures controlled and approved by the qualifying activity and the basic plant, and provided that all wafer fabrication, 100 percent screening tests and groups A, B, C, D, and E inspections are performed in the U.S.A. at the basic plant, except for step 2 of table II, high temperature life (stabilization bake), which may be performed at the foreign assembly plant. However, 100 percent screening may be performed in any country that has an ISA with the U.S.A. (e.g., NATO STANAG no. 4093 or DoDI 2045).

3.10 Waivers and letters of interpretation and policy letters. Waivers, letters of interpretation, and policy letters shall be approved in writing by the preparing activity. All waivers, letters of interpretation, and policy letters applicable to MIL-S-19500, associated detail specification, or MIL-STD-750 written prior to the current date of that particular document are null and void. All subsequent waivers, letters of interpretation, and policy letters written are valid only until the next document action (This is not intended to void 4.4.1).

4. QUALITY ASSURANCE PROVISIONS

4.1 Responsibility for inspection. The manufacturer is responsible for the performance of all inspection requirements as specified herein, and in the detail specification. The manufacturer may use his own or other suitable facilities (which have been approved and granted laboratory suitability by the qualifying activity for the performance of the inspection requirements specified herein). The Government or acquiring activity reserves the right to witness or perform any of these inspections set forth herein or in the detail specification and to audit the data resulting from the manufacturer's performance of these inspections. The responsible Government inspection agency shall be given adequate notification prior to the initiation of all tests. If a manufacturer elects to eliminate or reduce a QCI step or 100 percent screen operation by substituting a process monitor or SPC procedure (when approved by the preparing activity and the qualifying activity), the manufacturer is only relieved of the responsibility of performing the QCI or 100 percent screen operation. However, the manufacturer is still responsible for providing product which meets all of the performance, quality, and reliability requirements herein.

* 4.1.1 Government source inspection. Government source inspection shall be required as a condition for the use of a JAN brand on all semiconductor devices acquired to and meeting the requirements of this specification and the applicable detail specification. Government source inspection shall apply to qualification, QCI, and screening. The Government representative shall inform the manufacturer to the extent of inspection that will be exercised upon notification that a QCI is intended and the date on which inspection will begin. In the event of limited inspection resources, the Government source inspector shall arrange the schedule for the performance of inspections, surveillance, audit, or reviews so as to maximize the effectiveness of the inspection function.

* 4.1.1.1 Government source inspection for JANS. For each JANS lot, Government personnel (and other Government designated representatives when required by contract) shall perform surveillance and monitoring functions related to inspections, assembly, and wafer fabrication from wafer lot acceptance through shipment of the completed product. The inspection requirements shall be performed or witnessed by the representatives at designated manufacturing and test steps as noted in the manufacturing/inspection flow chart. Adequate inspection stations shall be provided for the Government representatives. These designated manufacturing and test steps as a minimum shall include the following:

a. Surveillance of wafer lot acceptance, when applicable.

b. Visual examinations at die inspection and at pre-seal.

c. Surveillance of in-process die shear test.

d. Surveillance of in-process bond strength test.

e. Surveillance of burn-in board checkout for continuity.

f. Surveillance of examination required by the last four requirements of subgroup 3 of table IVa.

g. Surveillance of radiation tests when required by table VI.

h. Final audit of documentation on each lot.

i. Right to witness and analyze scanning electron microscope (SEM) photography of applicable wafers.

j. Surveillance of failure analysis, DPA activities and the results and corrective actions related thereto.

k. Surveillance of ESDS classification tests.

4.1.1.2 Government source inspection for JAN, JANTX, and JANTXV devices. For JAN, JANTX, and JANTXV lots, Government personnel, and other Government designated representatives, will perform surveillance and monitoring functions related to screening and QCIs, assembly and processing steps back to the wafer fabrication line. These surveillance and monitoring functions are reflected in the procedures of section III, part 5 of DLAM 8200.

4.1.1.3 Government source inspection for suppliers. The supplier (whether manufacturer, distributor, dealer, stocker, etc.) shall have an inventory control system for JAN branded devices which documents and maintains traceability by quantity accumulated and distributed on each device lot or partial lot (i.e., as identified by common PIN, inspection lot identification code, and manufacturer) to the original manufacturer or (where intermediate transaction(s) is involved) to the previous supplier(s)). All suppliers of JAN semiconductors shall be prepared to provide to any customer, when required by acquisition document, copies of the actual records of processing or a certification as to the origin and their own transactions and handling of semiconductors ordered from them including copies of the actual records of processing or certification(s) from their supplier(s). Any supplier of JAN semiconductors shall make details of their inventory control system and traceability documentation available to an authorized Government representative for inspection (acceptance) upon request.

4.1.1.4 Government source inspection at a test facility other than the device manufacturer. The provisions of 4.1.1 shall apply, however, upon notification from the manufacturer it shall become the responsibility of the test facility to notify the Government representative and schedule an inspection.

4.1.1.5 Government source inspection at facilities other than the device manufacturer. Government source inspection for JAN branded devices, which are acquired from sources other than the device manufacturer, shall be required upon request for the purpose of verifying shipment integrity with regards to traceability documentation. Traceability documentation shall, as a minimum, include the requirements specified in 3.3.1 herein and other related lot records. The frequency of Government source inspection may vary in accordance with need determined by the Government. The facility shall have an inventory control system for JAN branded devices which is acceptable to the Government representative.

4.2 Procedure for lots held by manufacturers for more than 36 months. Semiconductors held by manufacturers or distributors for a period exceeding 36 months from the date of the last inspection for solderability or date of solder dip shall be demonstrated to be solderable in accordance with table IVa, group B, subgroup 2 (JANS) or table IVb, group B, subgroup 1 (JAN, JANTX, and JANTXV). The devices shall retain the original inspection lot identification code and an updated certificate shall accompany all shipments of devices to the Government or its contractors or subcontractors. Records of reinspection shall be maintained as specified in appendix D. The requirements for group A reinspection have been deleted.

4.2.1 Reinspection procedure for lots held by device distributors. Reinspection requirements may be satisfied by one of the following procedures:

a. Upon mutual agreement between the device manufacturer and distributor, the entire lot or a random sample, large enough to satisfy the reinspection requirements, may be returned to the device manufacturer by the distributor. Devices held and being represented by the submission of a random sample must be retained by the distributor until an updated certificate of conformance and acquisition traceability with certified reinspection date included is received from the device manufacturer. An updated certificate shall accompany all shipments of devices to the Government or its contractors or subcontractors. In the case of lot failure, when only a sample has been returned to the device manufacturer, the total represented lot must be returned for the required 100 percent inspection and screening. Quantity or price adjustments shall be a matter of agreement between the device manufacturer and the distributor.

b. When procedure 4.2 or 4.2.1a above is accomplished by a device manufacturer from inventory received from any one distributor and a lot failure has not occurred, the device manufacturer may choose to update all other distributors' certification documents for the same device type and lot inspection code. These updated documents shall contain the certified reinspection date. In case of lot failure occurring during procedure 4.2.1a, this paragraph does not apply and, therefore, each distributor must follow procedure 4.2.1a.

4.3 Classification. The examination and testing of semiconductor devices shall be classified as follows:

a. Qualification inspection (see 4.5.1).

b. Screening (see 4.6).

c. QCI (see 4.7).

* 4.3.1 Formation of inspection lots. The product shall be assembled into an identifiable inspection lot or collection of inspection sublots. Each lot shall be identified by a unique lot identification code (see 3.7.8).

4.3.1.1 JAN, JANTX, and JANTXV inspection lot. The total number of devices that the manufacturer submits at any one time for qualification or QCI shall constitute an inspection lot. The maximum small inspection lot size shall be 500 devices. The inspection lot is submitted to determine compliance with the requirements of the detail specification. Each inspection lot shall consist of devices of a single device type or consist of a collection of sublots of structurally identical devices contained on one or more detail specifications manufactured on the same production line(s) within a single plant through final seal by the same production technique and to the same device design with the same material requirements and sealed within the same 6-week period. Lot identification shall be maintained from the time the lot is assembled to the time it is accepted or rejected.

4.3.1.1.1 Inspection sublot. An inspection sublot shall consist of a single device type contained on a single detail specification manufactured on the same production line(s) through final seal by the same fabrication technique and to the same device design with the same material requirements and within the same 6-week period.

4.3.1.2 JANS inspection lot.

4.3.1.2.1 Wafer lot. A wafer lot shall consist of only semiconductor wafers subjected to each and every process step of masking, etching, deposition, diffusion, metallization, etc. as a group. Each wafer lot shall be assigned a unique identifier which provides traceability to all wafer processing steps. Wafer lot records shall identify all JANS device inspection lots formed from the wafer lot.

* 4.3.1.2.2 Wafer lot acceptance. Wafer lot acceptance is required for selected die designs such as overlay structure devices and devices with metallization path to bond pad crossing any junction covered by passivation or glassivation where the bonding pad is not on the active area of the device. This acceptance shall be performed in accordance with method 5001 of MIL-STD-750 for each of these lots.

4.3.1.2.3 Device inspection lot. The total number of devices that the manufacturer submits at any one time for JANS qualification or QCI shall constitute a device inspection lot and shall conform to the following criteria:

a. Small lots shall not exceed 500 pieces. Sampling inspection for large or small lots shall be in accordance with table IVa.

b. All devices shall be of a single device type.

c. All devices shall be from a single wafer lot.

d. All devices shall be assembled on the same production line with the same technique from die attach through final seal, within 21 working days not to exceed 31 calendar days.

4.3.1.3 Structurally identical device types. Structurally identical device types are devices manufactured on the same production line(s) through final seal, by the same fabrication technique within the same package family and to the same device design with the same material requirements and differ only electrically. Examples of such structurally identical device types are as follows:

a. Rectifiers, diodes, or thyristors grouped into different voltage ratings.

b. Transistors grouped for gain limits and voltage ratings.

c. Power MOSFETs grouped for $r_{DS}(on)$ and voltage ratings. Power MOSFETs of the same voltage types with identical design rules (field termination and cell density) and which differ only in die size are considered structural identical. Initially, groups B and C shall be performed on the largest die size available within each structurally identical voltage grouping. The die sizes which receive groups B and C inspection shall be rotated on a periodic basis thus assuring that all die sizes receive groups B and C inspection.

* 4.3.2 Traceability. All devices delivered to this specification shall be so identified (see 3.7.1 and 3.3.1) and documented that they shall be traceable through the lot identification code and inspection lot records. In addition, JANS devices shall have a lot control system from wafer processing through screening which provides wafer lot identification operation (machine), date of operation, operator(s) identification, quantity, and serial numbers (after step 8 of table II) of devices processed. This traceability data shall be maintained for 5 years.

* 4.3.3 Disposal of samples. Devices subjected to destructive tests or which fail any test shall not be shipped. Sample devices from lots which have passed QCI and which have been subjected to mechanical or environmental tests specified in groups B and C inspection and not classified as destructive, may be shipped provided each of the devices subsequently passes group A, subgroup 2 inspection.

4.3.3.1 Destructive tests. Unless otherwise demonstrated, the following MIL-STD-750 tests are classified as destructive:

| Method number | Test |
|---|---|
| 1017 | Neutron irradiation |
| 1019 | Steady state total dose irradiation |
| 1020 | ESDS classification |
| 1021 | Moisture resistance |
| 1036, 1037 | Intermittent operation life |

| Method number | Test |
|---|---|
| 1041 | Salt atmosphere |
| 1042 (condition D) | Burn-in/life test for power MOSFETs |
| 1046 | Salt spray |
| 1056 | Thermal shock (glass strain) |
| 2017 | Die shear test |
| 2031 | Soldering heat |
| 2036 | Terminal strength |
| 2037 | Post seal bond strength |
| 2075 | Decap internal visual design verification |
| 2077 | SEM |

All other mechanical or environmental tests (other than those listed in 4.3.3.2) shall be considered destructive initially, but may subsequently be considered nondestructive upon accumulation of sufficient data to indicate that the test is nondestructive. The accumulation of data from five repetitions of the specified test on the same sample of product, without significant evidence of cumulative degradation in any device in the sample, is considered sufficient evidence that the test is nondestructive for the device of that manufacturer. Any test specified as a 100 percent screen shall be considered nondestructive for the stress level and duration or number of cycles applied as a screen.

4.3.3.2 Nondestructive tests. Unless otherwise demonstrated, the following MIL-STD-750 tests are classified as nondestructive:

| Method number | Test |
|---|---|
| 1001 | Barometric pressure |
| 1022 | Resistance to solvents |
| 1026, 1027 | Steady-state life |
| 1031, 1032 | High temperature life (nonoperating) |
| 1038, 1039, 1040 | Burn-in screen |
| 1042 (conditions A, B, and C) | Burn-in/life test for power MOSFETs |
| 1051 (100 cycles or less) | Thermal shock (temperature cycling) |
| 1071 | Hermetic seal tests |
| 2006 | Constant acceleration |
| 2016 | Shock |
| 2026 | Solderability (If the original lead finish is unchanged and if the maximum allowable number of reworks is not exceeded.) |
| 2052 | PIND test |
| 2056 | Vibration, variable frequency |

| Method number | Test |
|---|---|
| 2066 | Physical dimensions |
| 2069, 2070, 2072, 2073, 2074 | Internal visual (pre-cap) |
| 2071 | External visual |
| 2076 | Radiographic inspection |
| 2081 | Forward instability shock test (FIST) |
| 2082 | Backward instability shock test (BIST) |
| 3101 | Thermal impedance testing of diodes |
| 3103 | Thermal impedance measurements for IGBTs |
| 3104 | Thermal impedance measurements for GaAs |
| 3051, 3052, 3053 (with limited supply voltage) | Safe operating area (SOA) (condition A for method 3053) |
| 3131 | Thermal resistance (emitter to base forward voltage, emitter-only switching method) |
| 4066 | Surge current |
| 4081 | Thermal resistance of lead mounted diode (forward voltage, switching method) |

When the junction temperature exceeds the device maximum rated junction temperature for any operation or test (including electrical stress test), these tests shall be considered destructive except under transient surge or nonrepetitive fault conditions or approved accelerated screening when, it may be desirable to allow the junction temperature to exceed the rated junction temperature. The feasibility shall be determined on a part by part basis and in the case where it is allowed adequate sample testing shall be performed to provide the proper reliability safeguards.

4.3.4 Resubmitted lots.

* 4.3.4.1 Resubmitted lots of JANS. Resubmitted lots shall be kept separate from new lots and shall be clearly identified as resubmitted lots. Any failed lot for group B, subgroups 1, 2, 3, 4, 5, 6, and group C may be resubmitted one time only, for the failed subgroup, at double the original sample sized with zero failures. Lots which fail group B, bond strength, die shear, decap internal visual and SEM (when applicable) shall not be resubmitted. For group A, 4.3.4.2 shall apply. With the approval of the qualifying activity die shear failures (when determined to be die attach failure mode) may be considered to be screenable utilizing the applicable thermal impedance methods.

* 4.3.4.2 Resubmitted lots of JANTXV, JANTX, and JAN. Resubmitted lots shall be kept separate from new lots and shall be clearly identified as resubmitted lots. When any lot submitted for qualification or QCI fails any applicable subgroup requirement of groups A (for A-2, A-3, and A-4, see footnote 3 of table III), B, C, or E tests, it may be resubmitted once for that particular subgroup at double the original sample size with zero failures. A second submission, using double the original sample size with zero failures, may only be performed if it is determined by analysis of all the failed devices, that the failure mechanism is due to a defect that can be effectively removed by rescreening the entire lot, and that rescreening has been performed.

* 4.3.4.3 Resubmitted lots of JANSM, JANSD, JANSL, JANSR, JANSF, JANSG, JANSH, JANTXVM, JANTXVD, JANTXVL, JANTXVR, JANTXVF, JANTXVG, and JANTXVH. Lots which fail group D tests may be resubmitted if failure analysis indicates that the defective parts can be effectively removed by screening the entire lot (100 percent) and sample retesting to group D requirements.

4.4 Conditions and methods of test. Conditions and methods of test shall be in accordance with MIL-STD-750. The general requirements of MIL-STD-750 apply as specified.

4.4.1 Alternative test methods. Other test methods or circuits may be substituted for those specified in MIL-STD-750 provided it is demonstrated to and approved by the qualifying activity that such a substitution in no way relaxes the requirements of this specification. The schematic wiring diagram of the test equipment shall be made available for checking by the qualifying activity. Control and calibration of the test equipment shall be established and documented in accordance with MIL-STD-45662.

* 4.4.2 Procedure in case of test equipment failure or human error. If it is determined through an engineering evaluation that a failed device is the result of test equiment failure of human error, a replacement device from the same inspection lot may be added to the sample. Documentation of the event and subsequent follow-up shall be in accordance with appendix D. The replacement device shall be subjected to all those tests to which the discarded device was subjected prior to its failure and to any remaining specified tests to which the discarded device was not subjected prior to its failure. Failures occurring as a result of operator error, prior to the start of testing, may be replaced by the manufacturer without notifying the cognizant Government quality representative but shall be noted on the lot history. Any ESD failures shall be counted as rejects and not be attributed to equipment/operator error for screening, group A, and end-point electrical tests of MIL-STD-750.

* 4.4.2.1 Device manufacturer imposed tests. Any manufacturer imposed test(s) (e.g., gross and fine leak) conducted prior to any qualification or QCI, are to be reported in the qualification report and are performed on all subsequent lots until requalified. These records shall be made available for review by the qualifying activity. If any manufacturer imposed tests detect a problem, the manufacturer shall submit all devices in the lot to those tests to eliminate rejects and shall take steps to determine and eliminate the cause of failure (e.g., rough handling which has produced gross leaks).

4.4.3 Standard mixer diodes and holders. The manufacturer of UHF and microwave mixer diodes shall establish and maintain standard mixer diodes and standard mixer holders for use in qualification and quality conformance testing of UHF and microwave mixer diodes. These standards shall be calibrated at least once in each successive 12-month period or prior to use if over 12 months, at a laboratory acceptable to the Government.

4.4.4 Electrical test equipment verification. The manufacturer shall define and utilize a method (e.g., correlation samples, diagnostic routines, etc.) to verify the measurement and operation characteristics of the electrical test equipment when in use. In the event of verification of failure, the manufacturer shall utilize a procedure which will determine the requirements for traceability, recovery, and when retesting is required of all units tested since the last successful verification.

4.5 Qualification inspection.

* 4.5.1 Qualification inspection. Qualification inspection shall be performed at a facility approved by the qualifying activity and shall be conducted in accordance with the procedures described herein and appendix D. Application for qualification inspection shall be submitted on DESC form 190 and shall include a proposed test plan, design and construction form 360, and engineering evaluation as applicable. Qualification of a particular device type to a given product assurance level may be extended by the qualifying activity to any other product assurance level provided all the groups A, B, C, D, and E requirements of the other level have been met and provided that suitable approved screening facilities are available for the other tests and stress levels. In addition, the requirements of 3.4.2.2 (3.6.8 and 4.3.1.2 for JANS) shall be met.

* Group D is required for each inspection lot of RHA types as specified in the detail specification. Qualification for RHA shall be for a specific semiconductor die and package type.

An alternate qualification procedure for RHA devices for levels M, L, and D only, are available for devices with demonstrated RHA. These devices must be submitted for qualification inspection and QCI, if process or design changes affecting RHA are made. QPL-19500 provides a footnote for devices not requiring RHA qualification or QCI testing.

* 4.5.2 Inspection routine. For qualification, devices shall be subjected to screening tests (see 4.6), inspections specified in groups A, B, C, and E for the applicable product assurance level, and group D to the applicable RHA level. All samples subjected to groups B, C, D, and E must have been chosen from a lot which has passed the requirements for group A except as modified in 4.7.3. The following conditions apply:

a. The required sample plan from a sublot of each device type submitted except for series of devices which shall be the sample plan of the highest and the lowest voltage types or as the qualifying activity requires, shall be tested for each group A subgroup.

b. A sample from one sublot shall be tested for each group B subgroup. A sample device from each sublot (each device type) shall be submitted to the design verification examination.

c. A sample from one sublot shall be tested for each group C subgroup. At the option of the manufacturer, devices from table IVb, subgroup 3, may be continued on in group C, subgroup 6, to achieve 1,000 hours or 6,000 cycles total, or separate samples may be used.

d. When group D (RHA) qualification extension is granted, the radiation facility shall be approved by the qualifying activity. A sample from a sublot of each device type shall be tested for each group D subgroup.

* e. Devices which are constructed using braided leads may be processed through table II screening and qualification high temperature testing prior to the addition of leads. Qualification testing requiring load current conduction will require that leads be attached.

4.5.2.1 Qualification to ESDS classes. Initial qualification to an ESDS class or requalification after redesign shall consist of qualification to the appropriate quality and reliability level plus ESDS classification in accordance with method 1020 of MIL-STD-750.

ESDS classification levels are defined as follows:

| ESDS class designator | Prior designation category | Marking | Electrostatic voltage |
|---|---|---|---|
| 1 | A | ▲ | 0 - 1,999 V |
| 2 | B | ▲ ▲ | 2,000 - 3,999 V |
| 3 | | | 4,000 - 15,999 V |
| Nonsensitive | | | > 15,999 V |

a. Although little variation due to case outline is expected, if a device type is available in more than one package type or case outline, ESDS testing and classification shall be applied to at least that one package type shown by experience to be worst case for ESDS. ESDS classification test results shall be submitted to DESC-ELST for all associated detail specifications for listing on the QPL. Specifications using structurally identical die designs may be classified with data from previously classified types. Any dissimilar designs within a associated detail specification shall have ESDS classifications for each structurally identical grouping.

b. All power bi-polar transistors and rectifiers except schottkys are considered to be at least class 3 by design. Schottky case mounted rectifiers may be marked class 3, upon successful completion of a 2 ampere reverse energy test. Other schottky rectifier package configurations may be designated class 3, if they pass a reverse energy test which has been demonstrated to correlate with class 3 classification.

c. All zeners, (voltage reference and voltage regulators) and transient suppressors are considered non-sensitive by design.

* 4.5.2.2 ESDS. ESDS classification testing shall be done in accordance with method 1020 of MIL-STD-750 and the applicable associated detail specification (see 3.7.3.1). Devices shall be handled in accordance with the manufacturer's in-house control documentation. Devices that are clasified class 3 or nonsensitive, are not required to be handled as ESD sensitive, and manufacturer's in-house control documentation plan is not required. Handling shall begin at lead clip or wire bond (e.g., for packages which do not have a lead shorting bar or do not have leads shorted together). A model ESD control program is available upon request from the qualifying activity and may be used as a guideline document. Further guidance for device handling is available in the EIA JEDEC 108 document.

* 4.5.2.3 SPC program. The manufacturer shall use SPC techniques in the manufacturing process for parts covered by this specification. The SPC program shall be in accordance with all the requirements of EIA-557. The SPC program shall be documented and maintained as part of the overall reliability assurance program as specified in appendix D. A minimum program shall include training, definition of critical operations, installation of statistical control techniques, and a control action system. A planned SPC milestone schedule and progress reporting system shall be developed and made available for review. This SPC program plan and milestone shall be maintained as part of the overall product assurance program plan as specified in appendix D.

4.5.2.4 Process monitor programs. Process monitor programs shall be established as referenced below, for processes performed by the manufacturer. A fully implemented and approved SPC program (in accordance with 4.5.2.3) may replace all or portions of the process monitor programs with the approval of the qualifying activity. These programs shall be documented and made available to the certification team for review. The implementing procedures shall provide for frequency, sample size, reject criteria, allowable rework, and disposition of failed product/lots. Investigative and corrective actions shall be established which address noted deficiencies. With the exception of the particle detection monitor, a procedure is required for the traceability, recovery, and disposition of all units monitored since the last successful test. As with all monitors, the particle detection procedure shall provide for continual process improvement. Records of these monitors shall be available to any (Government or military user) audit team for review. As a minimum, the process monitors shall include the following, or equivalent as approved by the qualifying activity:

a. Die attachment (see appendix D, 40.1.4).

b. Wire bond (see appendix D, 40.1.5).

c. Glass-to-lead seals on clear glass diodes (see appendix D, 40.1.13).

d. Lid seal (see 3.6.1.1, 3.6.1.2) and (see appendix D, 40.1.7).

e. Particle contamination (see appendix D, 40.1.14).

f. Applications of final lead finish (see 3.8.1).

4.5.2.5 Qualification by extension. Qualification of a structurally identical device or series of devices from the same or different associated detail specifications may be extended from a previously fully qualified device provided the following information and data are supplied to the qualifying activity:

a. Previously qualified device type, associated detail specification number, and qualification reference number.

b. Design and construction information on devices covered under different associated detail specifications.

c. Samples of structurally identical devices with certification that these samples are structurally identical to the previously qualified device.

d. Group A variables data on an sample plan of each structurally identical device type except for series of devices which shall be the sample plan of the highest and the lowest voltage types or as the qualifying activity requires, or as specified in associated detail specifications covering groups of devices. Test samples of selected devices in a group or portion of a group shall be from the same inspection lot.

e. Results and variables data for each structurally identical device on all group B and C electrical tests not specified in group A, including tests at temperature extremes.

f. All results and variables data on group B and C tests as follows:

(1) Data on any tests are not required by the qualified device.

(2) Data that is the result of tests performed at stress levels greater than those required for the qualified device.

(3) Data for any tests requiring more exacting limits than those found for the qualified device.

g. Items 4.5.2.5d through 4.5.2.5f shall not be required if the qualifying activity can be assured that the previously fully qualified device at least meets all of the conditions and requirements for the proposed structurally identical device type, except for device type marking.

4.5.3 End points. End-point electrical measurements shall be measured and recorded as applicable (e.g., if delta's are required) starting and after completion of all specified tests in the subgroups of groups B, C, and D. Pre-test end point failures shall be replaced by acceptable devices.

4.5.4 Variables data. Group A variables data and the pre-test and post-test group B, C, and D end point variables data shall be included in the test report.

4.5.5 Data submitted. Data for all tests shall be recorded in sufficient detail to verify the test procedures and conditions applied.

4.5.6 Selection of samples. All samples shall be randomly selected from the qualification inspection lot. Sample selection for group D testing shall be in accordance with table VI and shall be from each wafer or from each inspection lot, as appropriate.

4.5.7 Identification of samples. The authorized Government quality assurance representative may, at his option, mark or authorize the marking of each sample to be subjected to qualification testing in order to distinguish these devices from those not intended for qualification inspection.

4.5.8 Lot release. The lot from which the qualification samples are selected may be offered for delivery under contract after qualification approval has been granted provided screening and quality conformance requirements are satisfied.

* 4.5.9 Retention of qualification. To retain qualification, the manufacturer shall forward a report at 12-month intervals to the qualifying activity. The qualifying activity shall establish the initial reporting date. The report shall consist of a summary of the results of all tests performed for QCI (groups A, B, C, and D) including the number and mode of any subgroup failures. The summary shall include results of all QCI tests performed on completed lots during the 12-month period. If the summary of the test results indicates nonconformance with specification requirements (see 4.7.1 and 4.7.3) and corrective action acceptable to the qualifying activity has not been taken, action shall be taken to remove the failing product from the QPL. The results of tests of all reworked lots shall be identified and accounted for. Failure to submit the report within 60 days after the end of each 12-month period shall result in loss of qualification for the product.

4.5.9.1 Nonproduction. In the event that no production occurred during the reporting period, a report shall be submitted certifying that the company still has the capabilities and facilities necessary to produce the item. If, during three consecutive reporting periods, there has been no production of a device type or a package type using similar process technology (examples are N (or P) channel field-effect transistors (FETs) or small signal NPN (or PNP) bipolar transistors), the manufacturer shall be required to submit a representative product to appropriate testing in accordance with the qualification inspection requirements.

4.5.9.2 Retention of JANS qualification. For JANS qualification retention, the requirements of 4.5.9 above and the following are required:

a. A list which identifies by device type the total number of lots completing QCI and identifies the device types for which there was no qualification conformance inspection during the reporting period.

b. Information regarding failed lots, including lots withdrawn or scheduled for resubmission, that includes:

   (1) Lot identification code and PIN(s) of the failed lots.

   (2) The percent defective due to burn-in screen.

   (3) The results of group A, B, and C testing (i.e., pass or fail).

c. Summary of parts fallout (see 4.9.1.1).

d. Summary of failure analysis reports (see 4.6.5).

e. Certification that the design and construction of each qualified device is identical to that for which qualification approval was granted.

f. Certification that the manufacturer still has the capabilities and facilities necessary to manufacture devices for which no quality conformance inspection has been performed.

4.5.9.3 PPM quality level verification. The contractor shall provide documentation upon request to the qualifying activity pertaining to PPM-1. Levels as defined in 3.4.5, 4.7.4.1, 4.9.2, and 4.9.3.

4.6 Screening. All JANS, JANTXV, and JANTX semiconductor devices (100 percent) shall have been subjected to and passed, all the applicable screening tests (as specified in table II) in the sequence shown and the applicable percent defective allowed (PDA) for the type of semiconductor and product assurance level (device class) specified. Devices which fail any test criteria in the screening, shall be identified and controlled until removal from the lot at the option of the manufacturer, the rejects may continue processing. The lot records shall identify the point of failure and the actual PDA (as applicable). Any rejected devices shall be removed from the lot prior to shipment. Except for JANS, the conditioning and screening tests performed as standard production tests need not be repeated when these are predesignated and acceptable to the Government as being equal to or more severe than specified herein provided the relative process conditioning sequence is maintained. All tests, preconditioning and screening operations which were performed on the devices submitted for qualification inspections specified herein shall be performed on all devices subsequently submitted for QCIs (see 4.7).

* 4.6.1 PDA. Selected electrical parameters shall be designated in the associated detail specification as interim and end-point measurements for the 100 percent burn-in of screen 12 of table II. These parameters may also be compared to determine whether the change during burn-in (delta) is indicative of a lot stability problem. All burn-in pre-conditioning failures (on additional burn-in added prior to screen 12) shall be counted as part of the PDA in screen 13. When these parameters are specified, the quantity in the lot which fail these parameters or associated delta limits shall not exceed 10 percent. If the percent defective exceeds 20 percent, the lot shall not be acceptable for any level (see 4.6.6).

4.6.2 Notification for JANS. The responsible Government inspection agency shall be given adequate notification of the schedule for internal visual inspection and for the start of the remaining screening tests.

4.6.3 JANTX and JANTXV product. The procedure for testing and screening for JANTXV and JANTX devices shall be in accordance with tables II, III, IVb, V, figure 1, and as specified in the applicable associated detail specification.

4.6.3.1 Alternate procedure for screening of JANTX and JANTXV types. JAN types may be processed and marked as JANTX and JANTXV types by the original part manufacturer on his own qualified product provided the following procedures are satisfied:

a. All devices to be proposed for JANTXV processing (except clear glass JANTXV diodes which shall be subjected to internal visual inspection before printing or marking) must have been subjected to and passed JANTXV internal visual 100 percent screening prior to seal.

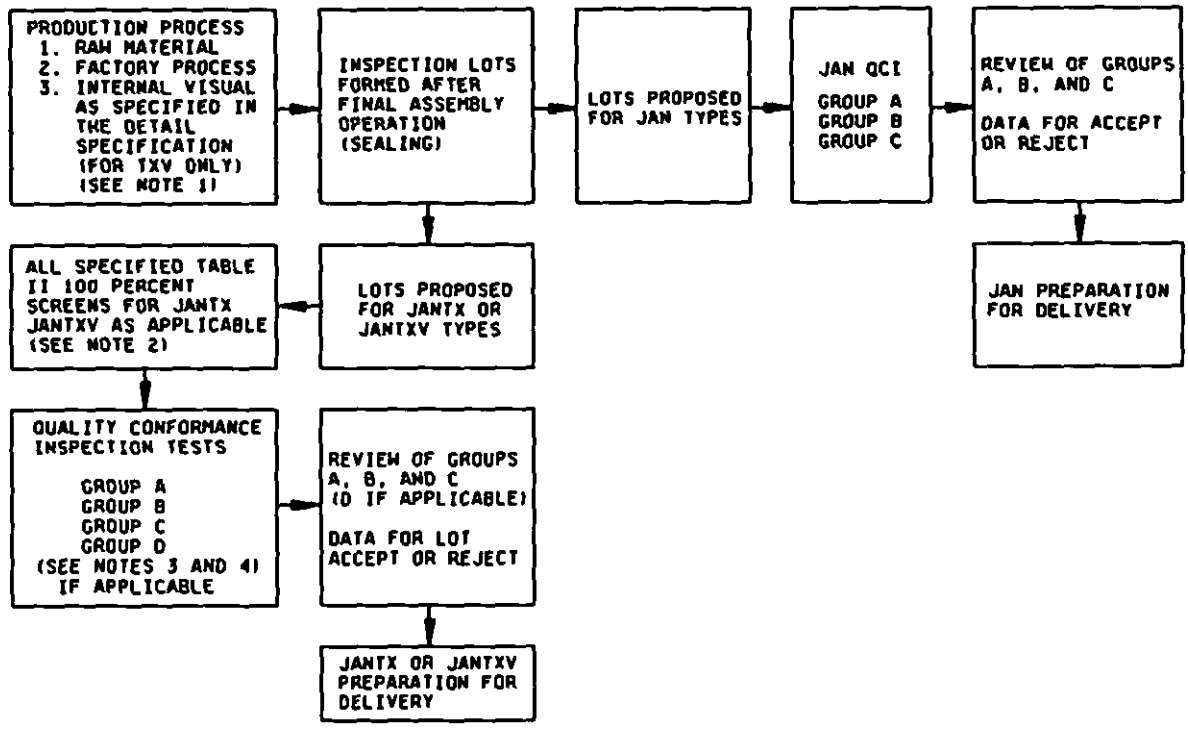
b. Groups A, B, and C inspection shall have met the JANTX and JANTXV level requirements in accordance with tables III, IVb, V, figure 2, and the applicable associated detail specification.

c. Screening shall be conducted in accordance with table II, figure 2, and the applicable associated detail specification. All units failing these tests shall be removed from the lot and the quantity removed shall be noted in the lot history.

* d. A sample of the screened devices shall be submitted to and pass the requirements of group A-1 and A-2 inspection (table III) (table IVb, subgroup 1) subsequent to the 100 percent screening (of the lot or separate portions thereof) as specified in 4.6.3.1c, as shown on figure 2.

4.6.3.2 JANTX and JANTXV pre and post burn-in electrical measurements. Alternate methods to variables recording may be used to determine delta end point requirements of JANTX and JANTXV burn-in provided the qualifying activity has granted written approval. When alternate methods to variables recording are used to determine delta end point requirements, devices shall be separated into groups, each of which shall have maximum and minimum limits on the variable parameter(s). The difference in parameter limits for any group shall not exceed the delta requirements for the variable parameter(s).

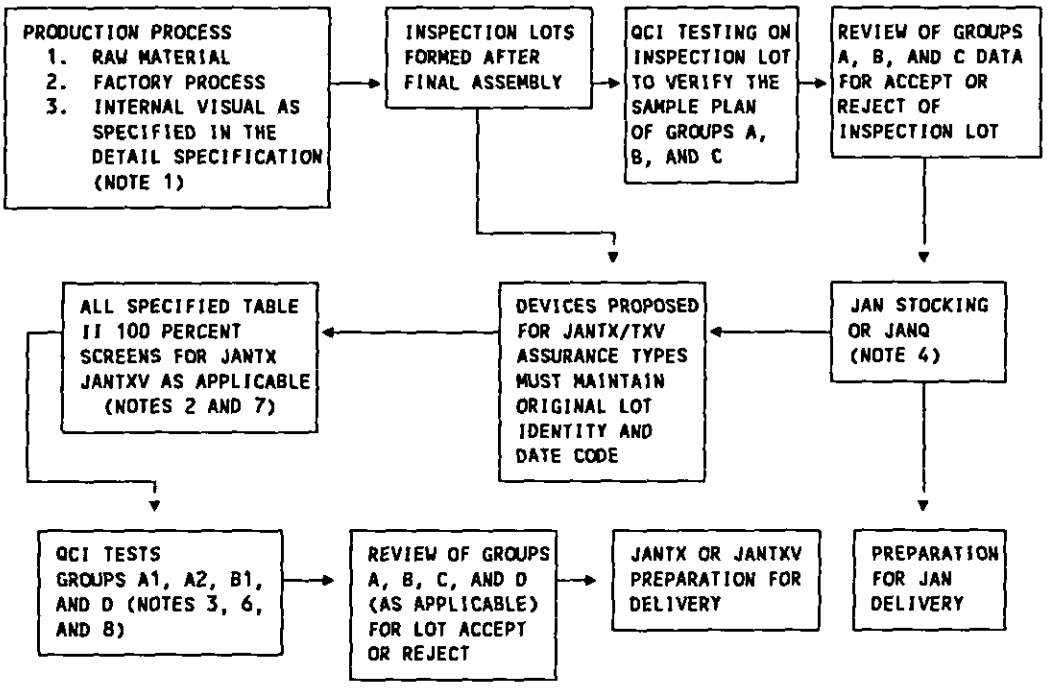
4.6.3.3 Alternate procedures for qualification and QCI where JAN is not covered by the associated detail specification. When the JAN quality level is not included in the associated detail specification, or at the option of the manufacturer, the alternate flow (see figure 2) may be used for qualification and QCI. The lot used shall be marked in accordance with 3.7.1, except the "JAN" designating symbol shall be replaced by the letter "Q". These samples shall not be shipped unless they are submitted to the flow that the lot was submitted to. In lieu of submitting the sample to the flow, the manufacturer, at his option, may keep the samples for reinspection as required in 4.2.




NOTES:

1. All products to be proposed for JANTXV processing must have been subjected to and passed JANTXV internal visual 100 percent screening at this step (except for clear glass JANTXV diodes which shall be subjected to internal visual inspection prior to painting and marking).
2. Order of the tests shall be performed as specified in table II.
3. Group D inspection may be performed at any point following the production process.
4. When the product being screened is processed as partial lots, each partial lot after the initial lot must receive groups A1, A2, and B1. When a partial lot fails at any inspection, the partial lot, may be reworked and resubmitted for the failed inspection step only. This reinspection will not affect any other partial lots in the inspection lot.

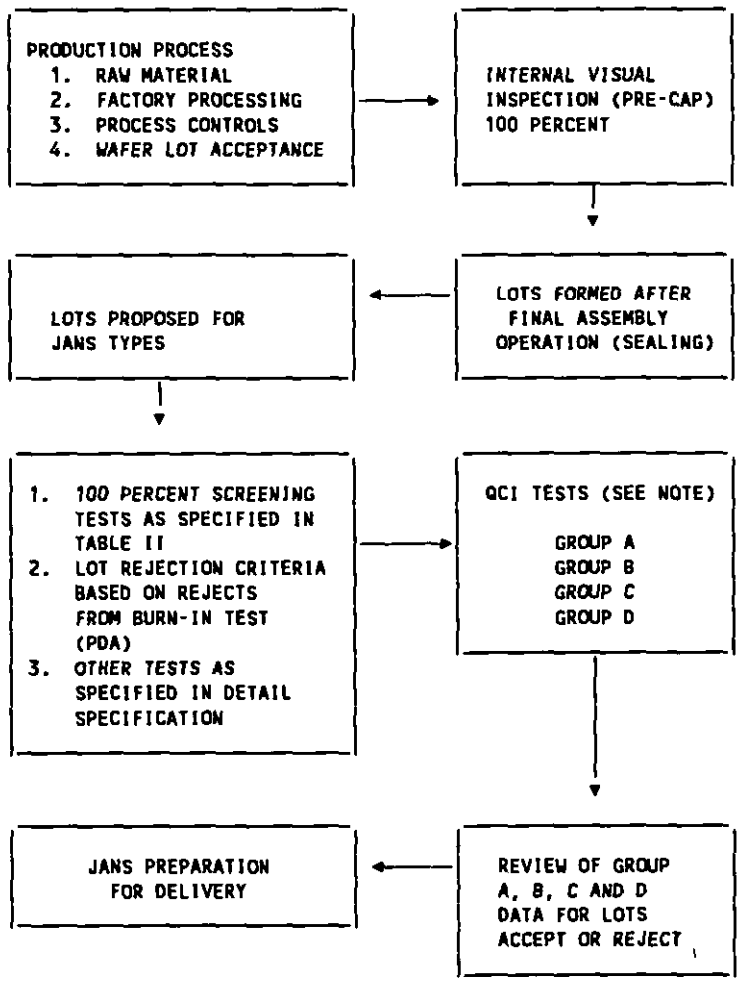
FIGURE 1. Order of procedure diagram for JAN, JANTX, and JANTXV device types (see 4.6.3).




NOTES:

1. All product proposed for JANTXV processing must have been subjected to and passed JANTXV internal visual 100 percent screening in accordance with table II herein at this step (except for clear glass JANTXV diodes which shall be subjected to internal visual prior to body paint or mark).
2. The order of all screening tests shall be performed as specified in table II.
3. B1 may be performed simultaneously with A. Steam age is not required for solderability testing at this step only.
4. JANQ product must be screened and receive the appropriate QCI testing prior to shipping (see 4.6.3.3).
5. Parallel processing of JANTX/TXV material with the JAN inspection lot is allowed.
6. If a JAN inspection lot is not processed in parallel with the material designated for JANTX and JANTXV, all group A, B, C, and D testing must be performed on a JANTX or JANTXV inspection lot.
7. Groups A, B, C, and D testing for lot acceptance may be initiated immediately prior to screen 1 or between screens 11 and 12.
8. When product being screened is processed as partial lots, each partial lot must receive this inspection step. Group B1 must be performed at this step. When a partial lot fails at any inspection step, the partial lot may be reworked and resubmitted for the failed inspection step only. This reinspection will not affect any other partial lots in the inspection lot.

FIGURE 2. Alternate order of procedure diagram for JAN, JANTX, and JANTXV device types (see 4.6.3.1).




NOTES:
1. Group D testing may be performed at any point following the production process (see 4.7.7).
2. Groups B, C, and D testing for lot acceptance may be initiated immediately prior to screen 15.

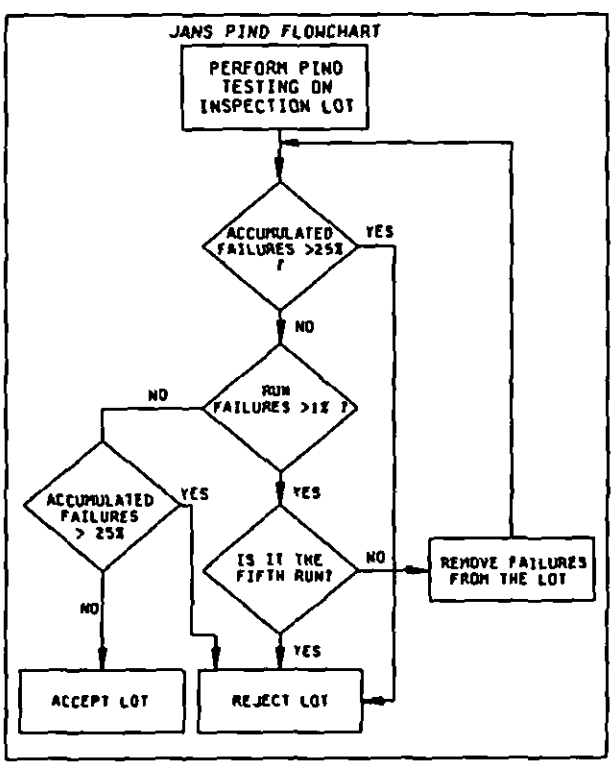
FIGURE 3. Order of procedure diagram for JANS.

4.6.3.4 PIND screened JANTX and JANTXV devices. When specified by the purchase order, JANTX and JANTXV devices may be PIND tested. This testing may be performed during 100 percent processing or following lot acceptance. The inspection lot, or portion or a lot, shall be submitted to PIND testing in accordance with MIL-STD-750, method 2052, test condition A or B, one pass minimum. Rejects shall be removed and JAN brand removed. Rejects shall not be used for any product assurance level. Accepted devices shall be marked with a "P" following the type number or any place on the device within the marking area.

4.6.4 JANS product. The procedure for testing and screening of JANS devices shall be in accordance with tables II, III, IVa, V, figure 3, and the applicable associated detail specification.

4.6.4.1 Burn-in acceptance criteria. The PDA for each inspection lot submitted to burn-in and interim (post burn-in) electrical parameters shall be 5 percent (for each burn-in) on all failures in steps 11 and 13a. Delta limits shall be defined in the associated detail specification. When the PDA applies to delta limits, the delta parameter values measured after burn-in (100 percent screening test) shall be compared with delta parameter values measured prior to that burn-in. Unless otherwise specified, lots which exceed the 5 percent PDA may be resubmitted one time only to the burn-in operation failed. The PDA shall be 3 percent on the resubmitted lot to each failed burn-in (delta endpoint parameter failures). If the combined burn-in PDA's for the first submission exceeds 20 percent or either of the resubmitted burn-in exceed the 3 percent PDA, the entire lot shall be unacceptable for any quality level."

4.6.4.2 PIND test for JANS devices. The inspection lot (or sublots) shall be submitted to 100 percent PIND testing a maximum of five times in accordance with method 2052 of MIL-STD-750, test condition A. PIND prescreening shall not be performed. The lot may be accepted on any of the five runs if the percentage of defective devices is less than one percent (zero failures allowed for lots of less than 50 devices). All defective devices shall be removed after each run. Lots which do not meet the one percent PDA on the fifth run, or exceed 25 percent defectives cumulative, shall be rejected and resubmission is not allowed. These parts shall not be shipped as any other product assurance level. When calculating numbers of allowed failures using percentages, fractional values shall be increased to the next whole integer.



4.6.4.3 Lead forming. When lead forming is specified for JANS devices in flat packs, it shall be followed by 100 percent fine and gross seal tests and external visual examination.

4.6.4.4 Burn-in socket verification for JANS. The electrical continuity between each device and the socket shall be verified prior to initiating burn-in (see MIL-STD-750 for details).

4.6.5 Failure analysis for JANS. Catastrophic failures (opens, shorts, and nonfunctional devices) that occur during JANS screening shall be failure analyzed to the extent required to allow identification of the cause of failure. This information shall be retained and presented to the qualifying activity, when requested, for review and determination if a failure trend is developing that needs corrective action.

4.6.6 Lots resubmitted for burn-in. Unless otherwise specified, lots may be resubmitted for burn-in one time only and may be resubmitted only when the observed percentage of defectives does not exceed twice the specified PDA or 20 percent whichever is greater. Resubmitted lots shall contain only parts which were in the original lot. Resubmitted lots shall be kept separate from new lots and shall be inspected for all specified characteristics using a tightened inspection PDA of 3 percent. If the percent defective for the resubmitted lot exceeds the tightened inspection PDA, the entire resubmitted lot shall be unacceptable for any quality level.

* 4.7 QCI. QCI shall be conducted in accordance with the requirements of groups A, B, and C for the specified product assurance level, and group D to the applicable RHA level. If a lot is withdrawn in a state of failing to meet quality conformance requirements and is not resubmitted, it shall be considered a failed lot and reported as such. Each lot shall be subjected to group A and B inspection. Successful completion of group C quality conformance for a given product assurance level shall satisfy the group C requirements for the tested level or any product assurance level and devices represented by the structurally identical group. The grouping of structurally identical devices shall be as agreed between the manufacturer and the qualifying activity. JANS devices shall not be used to represent the other product assurance levels. If a manufacturer elects to eliminate a QCI step or 100 percent screen operation substituting either a process monitor or SPC procedures (when approved by the preparing activity and qualifying activity), the manufacturer is only relieved of the responsibility of performing the QCI or 100 percent screen operation. The manufacturer still bears full liability for any failure that may result if these tests are performed at a later time.

4.7.1 Corrective action. If 3 of 10 consecutive lots or if 2 successive lots of a device type or structurally identical types are rejected for the same failure mechanism corrective action shall be initiated by the manufacturer and submitted in the retention report (see 4.5.8). Failure to initiate corrective action may result in removal of products from the qualified product list.

4.7.2 Notification for JANS. The responsible Government inspection agency shall be given adequate notification before the start of QCI for JANS lots.

4.7.3 Nonconformance. Lots which fail subgroup requirements of group A, B, or C may be resubmitted in accordance with the provisions of 4.3.4 (4.3.4.3 for group D). However, if the lot is not resubmitted or fails resubmission, the lot shall not be shipped and the JAN marking shall be removed within 30 days.

Samples from subsequent lots of the device types in the structurally identical device grouping represented by a failed group C inspection in the case of group C failures, shall then be subjected to all the tests in the subgroup in which the failure occurred, on a lot-by-lot basis until three successive lots pass the failed subgroup. The testing may then return to periodic testing. A device type which fails a group C inspection shall not be accepted until the device type which failed, successfully completes the failed group C subgroup(s). Other device types from the same qualified group represented by the failed device type may be accepted provided group C inspection requirements have been satisfied for those device types. A device type which fails a group D inspection may not be certified as an RHA device at the level tested, but may be used as a non-RHA device or certified at another (lower) level if the device meets the lower level requirements.

4.7.4 Group A inspection. Group A inspection shall be performed on each inspection lot and shall consist of visual and mechanical inspection and electrical tests as specified in table III and the associated detail specification. Group A inspection may be performed in any order. If an inspection lot is made up of a collection of sublots, each sublot shall pass group A inspection as specified. Devices which have received PIND screening in accordance with 3.7.6.1 may not be considered as candidates for this inspection unless the entire inspection lot has seen the same screening.

* 4.7.4.1 Group A, subgroup 2, 3, and 4 tests (PPM categories). Data collected from the tests of subgroup 2, 3, and 4 shall be used for subsequent PPM calculations in accordance with EIA-554. PPM calculations shall be based on the results of the first submission and shall be based on the semiconductor grouping defined as structurally identical (see 4.3.1.3), or as defined in 4.9.3 and PPM calculation, shall not use data on resubmitted lots. Calculation and data exclusion shall be in accordance with EIA-554, method B. Larger samples may be inspected by the contractor in order to calculate PPM, however rejection of the lot shall be based only on subgroup sample testing.

* 4.7.5 Group B inspection. Group B inspection shall be performed on each inspection lot. Group B shall be in accordance with table IVa or IVb as applicable, and the associated detail specification. Testing of one device type sublot in any subgroup shall be considered as complying with the requirements for that subgroup for all types in the lot. Different device types may be used for each subgroup. All inspections except for life tests shall be applied only to completed and fully marked devices (see 4.6.3.3) from lots which have been subjected to and passed the group A requirements. When the final lead finish is solder, or any plating prone to oxidation at high temperature, the samples for life tests (groups B3 and B6 for JX and JV, and groups B4 and B5 for JANS) may be pulled prior to the application of final lead finish. Tests within a subgroup shall be performed in the order specified. When the lead finish is tin plated the storage life test samples may be cleaned prior to the electrical end-point testing. An evaluation shall be performed on all catastrophic failures to determine the failure mode. Appropriate corrective action shall be performed as a result of the evaluation. All tests within a subgroup shall be performed in the order specified except table IVa, subgroup 2, and table IVb, subgroup 1.

4.7.5.1 Rejected lots. Lots with an unscreenable failure mode shall be rejected. Devices which have received PIND screening in accordance with 3.7.6.1 may not be considered as candidates for this inspection unless the entire inspection lot has seen the same screening.

4.7.5.2 Lots shipped prior to group B completion. No lots shall be shipped prior to completion of group B without the approval of the qualifying activity.

* 4.7.6 Group C inspection. Group C inspection shall be in accordance with table V and shall include those tests specified which are performed periodically at 1 year intervals on at least one device type from each structurally identical device grouping (from the same or different associated detail specification) in which the manufacturer has qualified device types. This inspection shall be applied only to completed and fully marked devices (see 4.6.3.3) from lots which have been subjected to and passed the group A requirements. When the final lead finish is solder, the life test subgroup may be pulled prior to the application of final lead finish. All tests within a subgroup shall be performed in the order specified. When the lead finish is tin plated, the storage life test samples may be cleaned prior to the electrical end-point testing. An evaluation shall be performed on all catastrophic failures to determine the failure mode. Appropriate corrective action shall be performed as a result of the evaluation. Lots with an unscreenable failure mode shall be rejected. Devices which have received PIND screening in accordance with 3.7.6.1 may not be used to qualify the next group C inspection periods unless all devices intended for manufacturing during that period will receive as a minimum the same screening.

4.7.6.1 Group C sample selection. Samples for subgroups in group C shall be chosen at random from the first lot submitted for QCIs during the specified group C inspection interval. Testing of one device type for each subgroup shall be considered as complying with the requirements for that subgroup for all types represented (see 4.7.6) from the same line. A different device type(s) shall be tested at each successive inspection interval until all structurally identical device types qualified on the same or different associated detail specifications from the same qualified line have been tested, except power MOSFETs grouped by the same voltage as described in 4.3.1.3. When none of the inspection lots passing group A of the first lot submitted contain the device type which is due to be tested, the samples for inspection shall be chosen from those types in the inspection lots being tested which have not been used for the longest time for group C inspection. Successful completion of group C inspection period starting with date code of the inspection lot submitted. Groups A and B shall also be completed on the group C inspection lot date code period to the coverage being valid.

4.7.6.2 Lots shipped prior to group C completion. No lots shall be shipped prior to completion of group C without the approval of the qualifying activity.

* 4.7.7 Group D inspection. Group D inspection shall be performed in accordance with table VI and the requirements of the associated detail specification. A device type which fails a group D inspection may not be certified as an RHA device at the level test, but may be used as a non RHA device or certified at another (lower) level if the device meets the lower level requirements. At the manufacturer's option, group D samples need not be subjected to all the screening tests, but shall be assembled in its qualified package and as a minimum, pass group A, subgroup 2 prior to irradiation. QCI is not required for a special group of moderately hard semiconductor devices for JANTXV, levels M and D. These devices are so noted in QPL-19500. Devices which have received PIND screening in accordance with 3.7.6.1, may not be considered as candidates for this inspection unless the entire inspection lot has been subjected to the same screening.

* 4.7.8 Group B, C, D, and E end points. Post test end points specified in the associated detail specification shall be measured for each device of the sample after completion of all specified tests in the subgroups. Except as specified or otherwise required, all life test (operation, storage, blocking, etc.) end point measurements shall be performed within 96 hours after sample units have been subjected to and removed from required tests. All other end-point test measurements shall be made within 168 hours, or as specified. Additional measurements may be made at the discretion of the manufacturer.

4.7.9 Inspection of packaging. The sampling and inspection of the preservation, packing, container and unit package marking shall be in accordance with the requirements of MIL-S-19491.

4.7.10 Group E inspection. Group E is a workmanship, ruggedness, and design verification inspection. Group E testing need only be performed when the testing requirements have been added to the associated detail specification. The results of group E testing shall be submitted to the qualifying activity (by all QPL manufacturers prior to the implementation of the associated detail specification or prior to shipment of product, as applicable). Product redesigns may be subjected to group E testing as required by the qualifying activity.

4.7.10.1 Group E testing requirements. Group E shall be performed in accordance with table VII herein and the associated detail specification. All tests within a subgroup shall be performed in the order specified. An evaluation shall be performed on all failures to determine if the failure mode is the result of a latent (time dependent) defect, workmanship, or design weakness. Appropriate corrective action shall be performed and approved by the qualifying activity.

4.7.10.2 Alternate group E testing procedures. Manufacturers may use internal design verification and/or ongoing reliability assessment programs in lieu of group E, subgroups 1 and 2 only, provided this testing is equivalent to or more stressful than group E and is performed using the same design and construction on file at DESC-ELST. This alternate testing must be approved by the preparing activity and the qualifying activity.

4.8 Inspection during manufacture.

4.8.1 Control of critical processes. Die attach and bonding operations shall be monitored in accordance with requirements of 4.5.2.4 process monitor program and appendix D.

4.9 Data recording (all quality levels). The results of all qualification, screening (attribute data), quality conformance tests (attributes or variable data) and inspections, and required failure analysis shall be recorded and maintained for at least five years in accordance with appendix D. Group A (read and record) need not be recorded for every QCI, however it shall be required upon request from DESC-ELST. The qualifying activity may request read and record data be performed on all selected and/or designated lots just prior to an audit and then may examine that data during the audit. The internal documentation or test tapes shall be available at any time. The product assurance program plan, qualification test reports, and periodic summary report (see 4.5.8) shall be submitted to the qualifying activity. The disposition of all lots or samples submitted for wafer lot acceptance, screening (when PDA is specified), QCI, or qualification shall be fully documented. Lots which fail any specified requirement shall be recorded as failed lots whether resubmitted or withdrawn. Disposition of resubmitted lots shall likewise be recorded so that a complete history for every lot tested from initial submission to final disposition including all failures, resubmissions, and withdrawals. For JANS devices, one copy of all attributes data, specified in table VIII, shall be available to the customer. Screening and QCI attributes and variable data shall be available for purchase and shipped to the acquiring activity if ordered on the purchase order.

4.9.1 JANS electrical test data retention. Unless otherwise specified in the associated detail specification, all electrical measurements performed on devices during screening tests and lot acceptance testing shall be recorded. The manufacturer shall retain a master data record for a minimum of 5 years following completion of QCI.

4.9.1.1 Summary of parts fallout. A summary of the JANS parts fallout during screening tests shall be prepared by the manufacturer and text in the lot listing record. This summary shall be prepared from the screening data as specified in 4.6 and shall state the number of times that each test parameter has failed, the quantity and serial numbers of devices that failed one or more test parameters. The summary shall also identify all catastrophic failures and the failure mode (open, short, mechanical damage, etc.).

4.9.1.2 Lot rejection report. If any lot is rejected for failure to meet the wafer lot acceptance or quality conformance requirements, a detailed report shall be prepared and submitted to the qualifying activity. The report shall include in detail the results of each test performed and the specific cause of lot rejection. Photographs shall be included where clarification is required (see 40.1.9 of appendix D).

4.9.1.3 Other data. Copies of radiographs for JANS devices shall be retained for 5 years.

4.9.2 PPM quality level verification. The contractor is responsible for establishing a quality system to verify the PPM defect level of lots that are subjected to subgroup tests of the group A inspections. The PPM defect level shall be based on a 6-month moving average. The contractor shall verify and report annually each month's PPM categories (i.e., PPM-2, PPM-5, and the individual group A subgroups in PPM-2). In the event that the contractor (component manufacture) meets or exceeds 100 PPM for PPM-2 groupings (see 4.9.3) the manufacturer shall identify the problem device type(s) and problem subgroup which caused the grouping to exceed 100 PPM.

4.9.3 PPM semiconductor groupings. In the event that a device type or structurally identical device types are of insufficient volume for PPM reporting, manufacturers may their its own groupings with the following guidelines:

a. Similar package styles.

b. Similar construction, materials, and processing.

4.9.4 Preservation of lot identity. During all screening, inspection, and marking operations, each lot and sublot shall be kept segregated, secure, and traceable.

4.9.4.1 Security of completed devices. Marked devices which have passed all screening and quality conformance requirements shall be retained in a secure area prior to shipment or delivery. Device inventory shall be controlled by device type, quantity, product assurance level, and transaction date. Provision shall be made for surveillance by Government representatives. This requirement applies to the manufacturer and distributors.

TABLE Ia. Product assurance requirements.

| | Requirement | Reference | JANS | JANSM JANSD JANSL JANSR JANSF JANSG JANSH | JANTXV | JANTXVM JANTXVD JANTXVL JANTXVR JANTXVF JANTXVG JANTXVH | JANTX | JAN | JANHC JANKC |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | (X = Required) | | | | |
| | Qualification: | 4.5 | | | | | | | |
| | a. Product assurance program and survey | 3.4.2 and appendix D | X | X | X | X | X | X | X |
| | b. Manufacturer certification | 3.4.2.2 and appendix D | X | X | X | X | X | X | X |
| | c. Inspection and testing | 4.5 and 4.6 | X | X | X | X | X | X | X |
| | d. Group E | Table VII | X | X | X | X | X | X | |
| | Inspection lot | 4.3.1.1 and 4.3.1.2 | X | X | X | X | X | X | |
| | Traceability | 4.3.1.4 | X | X | X | X | X | X | X |
| | Government source inspection | 3.4.4 | X | X | X | X | X | X | X |
| | Inspection during manufacture | 4.8 | X | X | | | | | |
| * | Process monitors | 4.5.2.4 and appendix D | X | X | X | X | X | X | X |
| | Screening | 4.6 and table II | X | X | X | X | X | | |
| | QCI: | | | | | | | | |
| | a. Group A (each lot) | 4.7.4 and table III | X | X | X | X | X | X | |
| | b. Group B (each lot) | 4.7.5 table IVa | X | X | | | | | |
| | | table IVb | | | X | X | X | X | |
| * | c. Group C (every 12 months) | 4.7.6 and table V | X | X | X | X | X | X | |
| | d. Group D (each lot) | 4.7.7 and table VI | | X | | X | | | |
| | Appendix H | | | | | | | | X |

* TABLE Ib. RHA levels and requirements. 1/

| Radiation level | | | Product assurance level | |
|---|---|---|---|---|
| RHA Designation | Total ionizing dose (RAD(Si)) 2/ | Neutron fluence ($N/Cm^2$) 3/ | JANTXV See table VI | JANS See table VI |
| M | $3 \times 10^3$ | | | |
| D | $1 \times 10^4$ | | | |
| L | $5 \times 10^4$ | | | |
| R | $1 \times 10^5$ | | | |
| F | $3 \times 10^5$ | | | |
| G | $6 \times 10^5$ | | | |
| H | $1 \times 10^6$ | | | |

1/ See 3.4.
2/ Test in accordance with MIL-STD-750, method 1019.
* 3/ Test in accordance with MIL-STD-750, method 1017, unless otherwise specified in the detail specification, the minimum neutron fluence shall be $2 \times 10^{12}$ $N/cm^2$.

TABLE Ic. Testing guidelines for changes to a qualified product. 1/ 2/ 3/ 4/ 5/ 6/ 7/

| | Changes (see 3.4.3 herein) | Testing, MIL-STD-750, (All electrical parameters as specified in associated detail specifications) | Samples to be submitted to qualifying activity |
|---|---|---|---|
| a. | Doping material source<br>Concentration<br>Process technique | GRP A and C-6 deltas (variables only when deltas are required) | C-6 (2 samples) |
| b. | Die structure/topography | Same as a | C-6 (2 samples) |
| c. | Mask changes affecting die size or active element | Variable GRP A, B-2, and C6, if new die area is smaller/larger in the applicable package than previously qualified | B-2 (2 samples) |
| | Wafer diameter | GRP A and C-6 | C-6 (2 samples) |
| | Final die thickness | GRP B-2 and B-4 | B-2 (2 samples) |
| d. | Passivation/glassivation or die coating | GRP A and C-6 | C-6 (2 samples) |
| e. | Metallization changes. Anything that effects density for Schottkys and composition of layers | GRP A, B-2, B-4, and C-6 | B-2 (2 samples) |
| f. | Die attach method | B-2 and C-3 | C-3 (2 samples) |

See footnotes at end of table.

TABLE Ic. Testing guidelines for changes to a qualified product 1/ 2/ 3/ 4/ 5/ 6/ 7/ - Continued.

| Changes (see 3.4.3 herein) | | Testing, MIL-STD-750, (all electrical parameters as specified in associated detail specifications) | Samples to be submitted to qualifying activity |
|---|---|---|---|
| g. | Bond process | B-4 and C-3 | C-3 (2 samples) |
| h. | Bond wire material, doping dimensions | B-4 and C-3 | C-3 (2 samples) |
| i. | Package or lid structure | B-1, B-2, and C-3 | C-3 (2 samples) |
| | Package or lid material | B-1, B-2, and C-3 | C-3 (2 samples) |
| | Package or lid dimension | B-1, B-2, and C-3 | C-3 (2 samples) |
| j. | Sealing technique | B-1, B-2, and C-3 | C-3 (2 samples) |
| k. | Sealing environment | B-1, B-2, and C-3 | C-3 (2 samples) |
| l. | Implementation of test methods | Notify qualifying activity (may involve test demonstration) | As required |
| m. | Changes in flow chart | Same as l | As required |
| n. | Fab move | Quality conformance test report (summary data) group A (read and record) | One test sample each subgroup (B and C) |
| o. | Assembly move | Same as L | Same as L |
| p. | Test facility move | Notify qualifying activity | As required |
| q. | Scribe/die separation | B-2 and C-3 | B-2 (2 samples) |
| r. | Qualification/QCI procedures | Notify qualifying activity | As required |

1/ Acceptable supporting data may be submitted to reduce or eliminate required testing.

2/ When variable data is required for applicable groups A and C testing, data histograms providing acceptable parameter data summaries may be submitted in place of variables.

3/ If changes involve more than one device type from the same certified line, contact the qualifying activity to determine appropriate selection of device type(s) to be selected for testing.

4/ The qualifying activity may add or reduce testing if warranted by detail specification requirements or unique design or process circumstances after notification of the manufacturer.

5/ All groups and subgroups referenced herein apply to JANTX and JANTXV only. Test requirements for sample submittals for design changes to JANS level qualified product are to be determined by the qualifying activity.

6/ Additional testing and evaluation in accordance with group E to establish confidence in the proposed change shall be performed as required by the qualifying activity (see 4.5.1).

7/ New die design requires full qualification.

* TABLE Id. Lead finish systems.

| Finish | Applied over | | | | Required underplate 1/ | | |
|---|---|---|---|---|---|---|---|
| | Base metal | Silver plate | Gold plate | Tin plate | Electroplated nickel | Electroless nickel | None 2/ |
| Hot solder dip 3/ | X | | | | | | X |
| Hot solder dip 3/ | | | | | | | X |
| Hot solder dip 3/ | | | | | X | | |
| Hot solder dip 3/ | | | | | | X | |
| Hot solder dip 3/ | | | | X | | | X |
| Hot solder dip 3/ | | | | X | X | | |
| Hot solder dip 3/ | | | | X | | X | |
| Hot solder dip 3/ | | | X | | X | | |
| Hot solder dip 3/ | | | X | | | X | |
| Hot solder dip 3/ | | X | | | X | | |
| Hot solder dip 3/ | | X | | | | X | |
| Tin plate | X | | | | | | X |
| Tin plate | | | | | | | X |
| Tin plate | | | | | X | | |
| Tin plate | | | | | | X | |
| Tin-lead plate | X | | | | | | X |
| Tin-lead plate | | | | | | | X |
| Tin-lead plate | | | | | X | | |
| Tin-lead plate | | | | | | X | |
| Tin-lead plate | | | | X | X | | |
| Tin-lead plate | | | | X | | X | |
| Gold plate 4/ | X | | | | | | X |
| Gold plate | | | | | X | | |
| Gold plate | | | | | | X | |
| Silver plate 5/ | X | | | | | | X |
| Silver plate | | | | | X | | |
| Silver plate | | | | | | X | |

1/ Underplate is the coating that the solder will wet and adhere to.
2/ May include activation systems such as immersion plating of silver or tin.
3/ Hot solder dip shall be applied in accordance with 3.8.1.2.
4/ Gold plating shall not be used directly over copper.
5/ Silver plating shall not be used directly over copper, however, silver cladding directly over copper is acceptable.

TABLE Ie. Coating thickness and composition requirements.

| Coating | Thickness (microinch/micrometer) | | Coating composition requirements |
|---|---|---|---|
| | Minimum 1/ | Maximum 2/ | |
| Hot solder dip (for round leads) 3/ | 60/1.52 | NS | The solder bath shall have a nominal composition of Sn60 or Sn63. 4/ |
| Hot solder dip (for all shapes other than round leads) 3/ 5/ | 200/5.08 | NS | The solder bath shall have a nominal composition of Sn60 or Sn63. 4/ |
| Tin plate (as plated) 6/ | 300/7.62 | NS | Shall contain no more than 0.12 percent by weight co-deposited organic material measured as elemental carbon. 7/ |
| * Tin-lead plate (as plated) 6/ | 200/5.08 | NS | Shall consist of 3 to 50 percent by weight lead (balance nominally tin) homogeneously co-deposited. Shall contain no more than 0.12 percent by weight co-deposited organic material measured as elemental carbon. 7/ |
| * Tin dipping 6/ | 100/2.54 | | |
| Gold plate | 10/.254 | 225/5.72 | Shall contain a minimum of 99.7 percent gold. Only cobalt shall be used as the hardener. |
| Silver plate | 100/2.54 | 425/10.8 | 99.7 percent silver minimum. |
| Nickel plate (electro-plate) | 50/1.27 | 350/8.89 | The introduction of organic addition agents to nickel bath is prohibited. Up to 40 percent by weight cobalt is permitted as a co-deposit. |
| Nickel plate (electroless) | 50/1.27 | 250/6.35 | The introduction of organic addition agents to nickel bath is prohibited. |
| Nickel cladding | 50/1.27 | 350/8.89 | |

1/ Package elements having noncompliant coatings are permitted provided they are subsequently hot solder dipped in accordance with 3.8.1.2b.
2/ NS = not specified.
3/ See 3.8.1.2.
4/ As measured to the center of the flat.
* 5/ See 3.8.1.4. For threaded stud packages only, the minimum coating thickness shall be 100 µm/ 0.54 µm.
6/ The maximum carbon content (and minimum lead content in tin-lead plate) shall be determined by the manufacturer on at least a quarterly basis. The determination of carbon and lead content may be made by any accepted analytical technique (e.g., for carbon: pyrolysis, infrared detection (using an IR212, IR244 infrared detector or equivalent); for lead: x-ray fluorescence, emission spectroscopy) so long as the assay reflects the actual content in the total deposited finish.
7/ The solder Sn concentration in the pot may range between 50 percent Sn to 70 percent Sn.
8/ Maximum nickel applies only to lead material.

* TABLE If. Package element (other than leads/terminals) finish systems.

| Finish | Applied over | | Required underplate | | | |
|---|---|---|---|---|---|---|
| | Gold plate | Tin plate | Electroplated nickel | Electroless nickel 1/ | Nickel cladding 1/ | None |
| Tin plate | | | | | | X |
| Tin plate | | | X | | | |
| Tin plate | | | | X | | |
| Tin plate | | | | | X | |
| Tin-lead plate | | | | | | X |
| Tin-lead plate | | | X | | | |
| Tin-lead plate | | | | X | | |
| Tin-lead plate | | | | | X | |
| Tin-lead plate | | X | | | | X |
| Tin-lead plate | | X | X | | | |
| Tin-lead plate | | X | | X | | |
| Tin-lead plate | | X | | | X | |
| Gold plate | | | X | | | |
| Gold plate | | | | X | | |
| Gold plate | | | | | X | |
| Silver plate | | | X | | | |
| Silver plate | | | | X | | |
| Silver plate | | | | | X | |
| Electroplated nickel 1/ | | | | | | X |
| Electroless nickel 1/ | | | | | | X |
| Nickel cladding 1/ | | | | | | X |

1/ Combinations of electroplated nickel and electroless nickel and nickel cladding are permitted.

TABLE II. Screening requirements.

| Screen | MIL-STD-750 method | Condition | JANS requirements | JANTXV requirements | JANTX requirements |
|---|---|---|---|---|---|
| 1a. Die visual for diodes 1/ | 2073 | Die form prior to assembly | 100 percent | When specified | N/A |
| 1b. Internal visual (pre-cap) inspection | | | 100 percent | 100 percent | N/A |
| For diodes | 2074 | | | | |
| For POWERFETs | 2069 | | | | |
| For microwave transistors | 2070 | | | | |
| For transistors | 2072 | | | | |
| 2. High temperature life Nonoperating life (stabilization bake) | 1032 | $T_{STG} \leq +175°C$ t = as specified | optional | optional | optional |
| 3a. Temperature cycling | 1051 | No dwell is required at +25°C. Test condition C, or maximum storage temperature, whichever is less, 20 cycles, t(extremes) ≥ 10 minutes. | 100 percent | 100 percent | 100 percent |
| 3b. Surge (as specified) 2/ | 4066 | Condition B, as specified | 100 percent | 100 percent | 100 percent |
| 3c. Thermal response 2/ (as specified) | | As specified | 100 percent | 100 percent | 100 percent |
| Transistors, POWERFETs | 3161 | | | | |
| Bipolar | 3131 | | | | |
| Diodes | 3101 | | | | |
| IGBT | 3103 | | | | |
| GaAs FET | 3104 | | | | |
| 4. Constant acceleration | 2006 | $Y_1$ direction at 20,000 G min except at 10,000 G minimum for devices with power rating of ≥ ten watts at $T_C$ = +25°C. The 1 minute hold time requirement shall not apply. | 100 percent except not required for metallurgically bond diodes | Optional 3/ | Optional 3/ |

See footnotes at end of table.

TABLE II. Screening requirements - Continued.

| Screen | MIL-STD-750 method | Condition | JANS requirements | JANTXV requirements | JANTX requirements |
|---|---|---|---|---|---|
| 5. PIND 4/ | 2052 | Condition A. | 100 percent see 4.6.4.2 | | |
| 6. Instability shock test (axial lead diodes only) 5/ | | | | | |
| a. FIST | 2081 | | 100 percent | | |
| b. BIST | 2082 | | 100 percent | | |
| 7. Hermetic seal 6/ | | | | | |
| a. Fine | 1071 | Omit for double plug diodes. Test condition G or H, maximum leak rate = $5x10^{-8}$ atm cc/s except $5x10^{-7}$ atm cc/s for devices with internal cavity > 0.3 cc. Maximum leak rate = $5x10^{-6}$ atm cc/s for cavities 3-40 cc. | optional | 100 7/ percent | 100 7/ percent |
| b. Gross | | | | 100 7/ percent | 100 7/ percent |
| 8. Serialization | | See 3.7.9. | 100 percent | | |
| 9. Interim electrical parameters | | As specified. | 100 percent (Read and record) | For case mounted rectifiers as specified | For case mounted rectifiers as specified |
| 10. High temperature reverse bias (HTRB) | | | | | |
| a. For transistors | 1039 | Test condition A. 80 percent (minimum) of rated $V_{CB}$ (bipolar), $V_{GS}$(FET) or $V_{DS}$(FET), as applicable. | 100 percent | 100 percent | 100 percent |

See footnotes at end of table.

TABLE II. Screening requirements - Continued.

| Screen | MIL-STD-750 method | Condition | JANS requirements | JANTXV requirements | JANTX requirements |
|---|---|---|---|---|---|
| 10. High temperature reverse bias (HTRB) - Continued | | | | | |
| b. For Powerfets | 1042 | Test condition B. 80 percent (minimum) of rated $V_{GS}$. | 100 percent | 100 percent | 100 percent |
| c. For diodes and rectifiers | 1038 | c. Test condition A. Diodes (not required for LEDs, case mounted rectifiers and zeners) 80 percent minimum of rated $V_R$ or $V_{RWM}$ when dc conditions are specified. 95 - 100 percent of $V_{RWM}$, when half sine condition is specified. | 100 percent | 100 percent | 100 percent |
| 11. Interim electrical and delta parameters for PDA (see 4.6.1) for JANTX and JANTXV and 4.6.4.1 for JANS | | As specified but including all delta parameters as a minimum. When HTRB is performed leakage current shall be measured on each device before any other specified parametric test is made. | 100 percent (Measure all specified parameters within 16 hours after removal of applied voltage in HTRB. Record those parameters which have a delta limit.)(See screen 13.) | 100 percent (Measure all specified parameters within 24 hours after removal of applied voltage in HTRB. Record those parameters which have a delta limit.)(See screen 13.) | 100 percent (Measure all specified parameters within 24 hours after removal of applied voltage in HTRB. Record those parameters which have a delta limit.) (See screen 13.) |
| 12. Burn-in | | As specified. | 100 percent | 100 percent | 100 percent |
| a. For bipolar transistors | 1039 | a. Test condition B. | 240 hours (minimum) | 160 hours (minimum) | 160 hours (minimum) |
| * b. For Powerfets | 1042 | b. Test condition A. | 240 hours (minimum) | 160 hours 8/ (minimum) | 160 hours 8/ (minimum) |

See footnotes at end of table.

TABLE II. Screening requirements - Continued.

| Screen | MIL-STD-750 method | Condition | JANS requirements | JANTXV requirements | JANTX requirements |
|---|---|---|---|---|---|
| 12. Burn-in - Continued | | As specified. | 100 percent | 100 percent | 100 percent |
| * c. For diodes, zeners, and rectifiers | 1038 | c. Test condition B. | 240 hours (minimum) | 96 hours (minimum) | 96 hours (minimum) |
| For case mount rectifiers | | Condition A, JANTX and JANTXV only. | N/A | 48 hours (minimum) | 48 hours (minimum) |
| * | | Condition B, for JANS | 240 hours (minimum) | N/A | N/A |
| d. For thyristors 10/ | 1040 | | 240 hours (minimum) | 96 hours (minimum) | 96 hours (minimum) |
| 13. Final electrical test (see 4.6 and 4.6.5) | | As specified. | 100 percent | 100 percent | 100 percent |
| a. Interim electrical and delta parameters for PDA (see 4.6.1 or 4.6.4.1) | | | Interim electrical and delta parameters as a minimum. (Read and record.) | Interim electrical and delta parameters as a minimum. (Read and record.) (See 4.6.3.2.) | Interim electrical and delta parameters as a minimum. (Read and record.) (See 4.6.3.2.) |
| b. Other electrical parameters 13/ | | | Group A, subgroups 2 and 3. | Group A, subgroup 2. | Group A, subgroup 2. |
| 14. Hermetic seal 6/ a. Fine b. Gross | 1071 | (Same as 7 above) 11/ | 100 percent | optional 7/ | optional 7/ |

See footnotes at end of table.

TABLE II. Screening requirements - Continued.

| Screen | MIL-STD-750 method | Condition | JANS requirements | JANTXV requirements | JANTX requirements |
|---|---|---|---|---|---|
| 15. Radiography | 2076 | 12/ | 100 percent | | |
| 16. External visual examination | 2071 | To be performed after complete marking and prior to lot acceptance | 100 percent | | |

1/ Visual inspection (method 2074) on clear glass diodes shall be performed any time prior to screen 8.
* 2/ Shall be performed any time before screen 13. Surge shall precede thermal response when both tests are performed. Surge and thermal impedance are applicable only when specified in the screening table of the detail specification.
3/ Constant acceleration shall be performed on gold bond devices.
4/ PIND is not applicable to any device with external and internal pressure contacts (die to electrical contacts) optical coupled isolators, and double plug diodes. PIND screening may be performed any time after screen 4 when imposed by contract or purchase order (see 3.7.6.1).
5/ Omit BIST and FIST tests for double plug or case-mounted diodes. Omit FIST test for temperature compensated referenced diodes.
* 6/ Non-transparent glass encased double plug noncavity axial lead diodes only may use method 2068 in lieu of 1071.
7/ Fine and gross seal leak test for JANTX and JANTXV shall be performed in either screen 7 or screen 14.
* 8/ Optional accelerated HTRB for POWERFETs in accordance with method 1042, condition A, shall be 48 hours minimum at $T_A$ = +175°C minimum. Initial use of this option is contingent upon subsequent completion of a one time 1,000 hour qualification in accordance with method 1042, and as specified on group E of the individual detail specification, condition A to be submitted with the initial qualification report.
* 9/ For JANS only, zener diodes shall be subjected to high temperature reverse bias at 80 - 85 percent of nominal $V_Z$ for $V_Z$ > 10 V. Omit test for devices with $V_Z \leq 10$ V. For JANS case mounted rectifiers condition A is required.
10/ For JANTX and JANTXV levels full wave-blocking test shall replace power burn-in for all thyristors.
11/ Hermetic seal screens for JANS may be performed in any order following final electrical test. Glass diodes shall not be painted until after seal tests. When hermetic seal testing is performed in screen 7 it does not have to be performed again in screen 14 for double plug diode construction.
12/ The radiographic screen for JANS may be performed in any sequence after screen 8.
13/ Tests previously performed 100 percent (i.e., surge, thermal impedance) need not be repeated in screen 13.

TABLE III. Group A inspection.

| Subgroups | JANS 1/ sample plan (n/c) | JAN, JANTX, JANTXV sample plan 1/ |
|---|---|---|
| Subgroup 1<br><br>Visual and mechanical inspection (MIL-STD-750, method 2071) | 15 devices<br>c = 0 | 45 devices<br>c = 0 |
| Subgroup 2 (PPM-2)<br><br>DC (static) tests at +25°C | 116 devices<br>c = 0 | 116 devices 2/<br>c = 0 |
| Subgroup 3 (PPM-2)<br><br>DC (static) tests at maximum rated and minimum rated operating temperatures | 2/ 3/ | 116 devices 2/<br>c = 0 |
| Subgroup 4 (PPM-2)<br><br>Dynamic tests at +25°C | | 116 devices 2/<br>c = 0 |
| Subgroup 5<br><br>Safe operating area test (for power transistors only):<br>a. DC<br>b. Clamped inductive<br>c. Unclamped inductive<br><br>End-point electrical measurement | 4/<br>45 devices<br>c = 0 | 45 devices<br>c = 0 |
| Subgroup 6<br><br>Surge current (for diodes/rectifiers only)<br>End-point electrical measurements | | 22 devices<br>c = 0 |
| Subgroup 7<br><br>Selected static and dynamic tests | | 22 devices<br>c = 0 |

1/ The specific parameters to be included for tests in each subgroup shall be as specified in the applicable associated detail specification. Where no parameters have been specified in a particular subgroup or test within a subgroup, no group A testing is required for that subgroup or test to satisfy group A requirements. A single sample may be used for all subgroup testing. These tests are considered nondestructive and devices may be shipped.

2/ If a device in the sample fails one or more test(s) in the subgroup(s) being sampled, each device in the (sub)lot represented by the sample may be screened for the test(s) for which the sample failed. An alternate temperature electrical screen necessary to remove the failure mode may be used after an Engineering evaluation is performed. A second sample shall be tested to the failed parameter. If the second sample fails, the same subgroup 100 percent rescreen of the failed subgroup shall be performed or the lot shall be rejected.

3/ All devices required by the specified sample plan shall be subjected to subgroups 2, 3, and 4 combined.

4/ All devices required by the specified sample plan shall be randomly selected from the devices subjected to subgroups 2, 3, and 4, and shall be subjected to subgroups 5, 6, and 7 combined.

TABLE IVa. Group B inspections for JANS devices.

| Inspections | MIL-STD-750 method | MIL-STD-750 condition | Qualification and large lot quality conformance inspection sample plan | Small lot QCI n/c |
|---|---|---|---|---|
| Subgroup 1 1/ | | | 22 devices c = 0 | 8 devices c = 0 |
| Physical dimensions | 2066 | Dimensions in accordance with case outline specified. | | |
| * Subgroup 2 1/ | | Separate samples may be used for each test. | 15 leads c = 0 | 6 leads c = 0 |
| Solderability | 2026 | The sample plan applies to the number of leads inspected. A minimum of 3 devices shall be tested. | | |
| Resistance to solvents | 1022 | Not required if marking is etched into the device. | 15 devices c = 0 | 15 devices c = 0 |
| Subgroup 3 | | | 22 devices c = 0 | 6 devices c = 0 |
| Temperature cycling (air-to-air) * (except for axial lead glass diodes) | 1051 | No dwell is required at +25°C. Test condition C, (100 cycles) or maximum storage temperature which-ever is less. | | |
| Thermal shock (liquid-to-liquid) (For axial lead glass diodes only) | 1056 | 25 cycles, condition A | | |
| Surge | 4066 | As specified. | | |
| Hermetic seal 2/ | 1071 | | | |
| a. Fine | | Not required for double plug diodes. Test condition G or H, maximum leak rate = $5 \times 10^{-8}$ atm cc/s, except $5 \times 10^{-7}$ atm cc/s for devices with internal cavity > 0.3 cc. Maximum leak rate = $5 \times 10^{-6}$ atm cc/s for cavities 3-40cc | | |
| b. Gross | | | | |
| Electrical measurements | | As specified. | | |

See footnotes at end of table.

TABLE IVa. Group B inspections for JANS devices - Continued.

| Inspections | MIL-STD-750 method | MIL-STD-750 condition | Qualification and large lot quality conformance inspection sample plan | Small lot QCI n/c |
|---|---|---|---|---|
| Subgroup 3 - Continued | | | | |
| Decap-internal visual (design verification) 3/ | 2075 | Visual criteria in accordance with qualified design and internal visual precap criteria. | 6 devices c = 0 | |
| Bond strength (wire or clip bonded devices only) | 2037 | | 22 wires or 11 devices c = 0 (Whichever requires the smaller number of devices) | |
| SEM (when specified) 4/ | 2077 | | 6 devices c = 0 | |
| Die shear (excluding axial leaded devices) | 2017 | The same number of devices used for bond strength will also be used for die shear (minimum of six die) | | |
| Subgroup 4 | | | 22 devices c = 0 | 8 devices c = 0 |
| Intermittent operation life | 1037 | 2,000 cycles | | |
| | 1042 | As specified. Condition D. | | |
| Electrical measurements | | Thermal response and other electrical measurements as specified. | | |
| Subgroup 5 | | | 22 devices c = 0 | 12 devices c = 0 |
| Accelerated steady-state operation life | | Bias conditions as specified. | | |
| Eutectic die attached semiconductors | 1027 | $T_J$ = +275°C minimum (for 96 hours minimum) | | |
| Soft solder die attached power semiconductors | 1027 | $T_J$ = +225°C minimum (for 168 hours minimum) | | |
| Electrical measurements | | As specified | | |

See footnotes at end of table.

TABLE IVa. Group B inspections for JANS devices - Continued.

| Inspections | MIL-STD-750 method | MIL-STD-750 condition | Qualification and large lot quality conformance inspection sample plan | Small lot QCI n/c |
|---|---|---|---|---|
| Subgroup 5 - Continued | | | | |
| Schottky diodes | 1038 | $T_J$ = rated $T_J$ maximum (for 240 hours minimum) | | |
| Electrical measurements | | As specified | | |
| Accelerated steady-state reverse bias power MOSFETS | 1042 | Condition A, $V_{DS}$ = rated, $T_A$ = +175°C, t = 120 hours and as specified | | |
| Electrical measurements | | As specified | | |
| Accelerated steady-state gate stress power MOSFETS | 1042 | Condition B, $V_{GS}$ = rated, $T_A$ = +175°C, t = 24 hours | | |
| Electrical measurements | | As specified | | |
| Bond strength (Al-Au die-interconnect only) | 2037 | As specified. Bond strength samples shall have passed accelerated steady-state operation life. | 20 wires c = 0 | 20 wires c = 0 |
| Subgroup 6 | | | 22 devices c = 0 | 8 devices c = 0 |
| Thermal resistance | | As specified. | | |
| Diodes | 3101 | | | |
| Transistors (bipolar) | 3131 | | | |
| Transistors (POWERFETS) | 3161 | | | |
| Thyristors | 3181 | | | |
| IGBT | 3103 | | | |
| GaAs FET | 3104 | | | |

1/ Electrical reject devices from the same inspection lot, may be used for all subgroups, when electrical end-point measurements are not required. Other non-catastrophic rejected devices (i.e., PIND, X-ray) may be utilized for all subgroups. For subgroups with end-point measurements, the devices shall be screened to table II through block 13.

2/ Non-transparent glass encased double plug noncavity axial lead diodes only may use method 2068 in lieu of 1071.

3/ Verification of metallurgical bond as defined in 30.14 of appendix A in its entirety shall be documented.

4/ This test may be performed at any time prior to lot formation.

TABLE IVb. Group B inspections for JAN, JANTX, and JANTXV devices.

| Inspections | MIL-STD-750 | | Sample plan | Small lot quality conformance inspection n/c |
|---|---|---|---|---|
| | Method | Condition | | |
| Subgroup 1 1/ | | | 15 leads c = 0 | 4 leads c = 0 |
| Solderability | 2026 | Separate samples may be used for each test. The sample plan applies to the number of leads inspected. A minimum of 3 devices shall be tested. | | |
| Resistance to solvents | 1022 | Not required if marking is etched into the device | | |
| Subgroup 2 | | | 22 devices c = 0 | 6 devices c = 0 |
| Temperature cycling (air-to-air) except for axial lead glass diode | 1051 | No dwell is required at +25°C. Test condition C, or maximum storage temperature whichever is less, (45 cycles, including screening) | | |
| Thermal shock (liquid-to-liquid) (For axial lead glass diodes only) | 1056 | 10 cycles, condition A | | |
| Surge | 4066 | As specified. | | |
| Hermetic seal 2/ | | | | |
| a. Fine leak | 1071 | Not required for double plug diode. Test condition G or H, maximum leak rate = $5 \times 10^{-8}$ atm cc/s, except $5 \times 10^{-7}$ atm cc/s for devices with internal cavity > 0.3 cc. Maximum leak rate = $5 \times 10^{-6}$ atm cc/s for cavities 3-40 cc | | |
| b. Gross leak | | | | |
| Electrical measurements 3/ | | As specified. | | |
| Subgroup 3 4/ | | | 45 devices c = 0 | 12 devices c = 0 |
| Steady-state-operation life or intermittent operation life 5/ | 1027 | Bias conditions as specified, 340 hours (minimum) | | |
| | 1037 | 2,000 cycles (minimum) | | |
| | 1042 | Condition D, 2,000 cycles (minimum) | | |
| Electrical measurements | | As specified. | | |
| Bond strength (wire or clip bonded devices only) | 2037 | The sample shall include a minimum of 3 devices and shall include all wire sizes. | 11 wires c = 0 | 11 wires c = 0 |

See footnotes at end of table.

TABLE IVb. Group B inspections for JAN, JANTX, and JANTXV devices - Continued.

| Inspections | MIL-STD-750 | | Sample plan | Small lot quality conformance inspection n/c |
|---|---|---|---|---|
| | Method | Condition | | |
| Subgroup 4 1/ | | | 1 device c = 0 | 1 device c = 0 |
| Decap internal visual (design verification) | 2075 | Visual criteria in accordance with qualified design. | | |
| SEM (when specified) | 2077 | | 6 devices c = 0 | 6 devices c = 0 |
| Subgroup 5 | | | 15 devices c = 0 | 6 devices c = 0 |
| Thermal resistance: | | As specified. Thermal resistance may be performed on group E frequency whenever 100 percent thermal impedance is performed. | | |
| Diodes | 3101 or 4081 | | | |
| Transistors (bipolar) | 3131 | | | |
| Transistors (POWERFETS) | 3161 | | | |
| Thyristors | 3181 | | | |
| IGBT | 3103 | | | |
| GaAs FET | 3104 | | | |
| Subgroup 6 6/ | | | 32 devices c = 0 | 12 devices c = 0 |
| High-temperature life (nonoperating) | 1032 | 340 hours minimum, $T_{STG(max)} = T_A$ | | |
| Electrical measurements | | As specified. | | |

1/ Electrical reject devices from the same inspection lot, may be used for all subgroups when electrical end-point measurements are not required. Other non-catastrophic rejected devices (i.e., PIND, X-ray) may be utilized for all subgroups. For subgroups with end-point measurements, the devices shall be screened to table II through block 13.

2/ Non-transparent glass encased double plug noncavity axial lead diodes only may use method 2068 in lieu of 1071. This test may be performed after electrical measurements.

3/ Unless otherwise specified, omit delta parameters limits for low current gain ($h_{fe}$) and leakage measurements included in end-point measurements.

4/ If a given inspection lot undergoing group B inspection has been selected to satisfy group C inspection requirements, the 340-hour or 2,000 cycle life tests may be continued on test to 1,000 hours or 6,000 cycles, as applicable, in order to satisfy the group C life test requirements and bond pull may be performed after group C life test. End-point measurements shall be performed or either group B, subgroup 3 (340 hours or 2,000 cycles, as applicable) to satisfy group B lot acceptance or group C, subgroup 6 (1,000 hours or 6,000 cycles, as applicable) to satisfy group B and C lot acceptance. If group B, subgroup 3, is to be continued to group C, bond strength test may be performed after group C, subgroup 6.

5/ Intermittent operation life shall be performed on all case mounted devices.

6/ Not required for power MOSFETs.

TABLE V. Group C periodic inspections (all quality levels).

| Inspections | MIL-STD-750 | | Sample plan | Small lot quality conformance inspection n/c |
|---|---|---|---|---|
| | Method | Condition | | |
| Subgroup 1 | | | 15 devices c = 0 | 6 devices c = 0 |
| Physical dimensions 1/ (Not required for JANS) | 2066 | Dimensions in accordance with case outline specified | | |
| Subgroup 2 | | | 22 devices c = 0 | 6 devices c = 0 |
| Thermal shock (glass strain) | 1056 | Test condition A, except test condition B for devices with power rating of > 10 watts at $T_C$ = +25°C. | | |
| Terminal strength | 2036 | As specified. | | |
| Hermetic seal 2/ | | | | |
| a. Fine leak | 1071 | Not required for double plug diodes. Test condition G or H, maximum, leak rate = $5 \times 10^{-8}$ atm cc/s, except $5 \times 10^{-7}$ atm cc/s for devices with internal cavity > 0.3 cc. Maximum leak rate = $5 \times 10^{-6}$ atm cc/s for cavities 3-40 cc. | | |
| b. Gross leak | | | | |
| Moisture resistance | 1021 | Omit initial conditioning. | | |
| Electrical measurements | | As specified. | | |
| Subgroup 3 | | Not required for disc packages or metallurgically bonded double plug devices, or stud packaged devices. | 22 devices c = 0 | 6 devices c = 0 |
| Shock | 2016 | Nonoperating, 1500 g's, 0.5 ms, 5 blows in each orientation: X1, Y1, and Z1 (Y1 only for axial glass diodes). | | |
| Vibration, variable frequency | 2056 | | | |
| Constant acceleration 3/ | 2006 | 1 minute minimum in each orientation, X1, Y1, and Z1 at 20,000 g's minimum, except at 10,000 g's minimum for devices with power rating of ≥ 15 watts. $T_C$ = +25°C. | | |
| Electrical measurements | | As specified. | | |

See footnotes at the end of table.

TABLE V. Group C periodic inspections (all quality levels) - Continued.

| Inspections | MIL-STD-750 | | Sampling plan | Small lot quality conformance inspection n/c |
|---|---|---|---|---|
| | Method | Condition | | |
| Subgroup 4<br><br>Salt atmosphere (corrosion)<br>1/ | 1041 | | 15 devices<br>c = 0 | 6 devices<br>c = 0 |
| Subgroup 5<br><br>Not applicable | | | | |
| Subgroup 6 4/ 5/ 6/<br><br>Steady-state-operation life or<br>Intermittent operation life or<br>Blocking life<br><br>Electrical measurements | <br><br>1026<br><br>1037<br>1042<br>1048<br><br> | Not required for disc packages.<br><br>1,000 hours minimum at maximum operating junction temperature<br>6,000 cycles minimum<br>Conditions D, 6,000 cycles minimum<br><br>As specified. | 22 devices<br>c = 0 | 12 devices<br>c = 0 |

1/ Electrical reject devices from the same inspection lot, may be used for all subgroups when electrical end-point measurements are not required. Other non-catastrophic rejected devices (i.e., PIND, X-ray) may be utilized for all subgroups. For subgroups with end-point measurements, the devices shall be screened to table II through block 13.

2/ Non-transparent glass encased double plug noncavity axial lead diodes only may use method 2068 in lieu of 1071. This test may be performed after electrical measurements.

3/ Not applicable to any devices with external and internal pressure contacts (die to electrical contacts), optional coupled isolators, and double plug diodes.

4/ If a given inspection lot undergoing group B inspection has been selected to satisfy group C inspection requirements, the 340-hour or 2,000 cycles life tests may be continued on test to 1,000 hours or 6,000 cycles, as applicable, in order to satisfy the group C life test requirements. End-point measurements shall be performed on either table IVa, group B, subgroup 4, or table IVb group B, subgroup 3 (340 hours or 2,000 cycles, as applicable) to satisfy group B (table IVa or table IVb) lot acceptance or group C, subgroup 6 (1,000 hours or 6,000 cycles, as applicable) to satisfy group B and C lot acceptance.

5/ Intermittent operation life shall be performed on all case mounted devices.

6/ The sample size may be increased and the test time decreased so long as the devices are stressed for a total of 22,000 device hours minimum, and the actual time or test is at least 340 hours.

TABLE VI. Group D (RHA tests). 1/

| Test | MIL-STD-750 | | JANS | | JANTXV | |
|---|---|---|---|---|---|---|
| | Method | Condition | Quantity/ accept number | Notes | Quantity/ accept number | Notes |
| Subgroup 1 2/ | | | | | | |
| Neutron irradiation | 1017 | +25°C | | | | |
| a. Qualification | | | (a) 11(0) | 3/ | (a) 11(0) | 4/ |
| b. QCI | | | (b) 11(0) | 3/ | (b) 11(0) | 4/ |
| End-point electrical parameters | | As specified in accordance with associated detail specification. | | | | |
| Subgroup 2 5/ | | | | | | |
| Steady-state total dose irradiation | 1019 | +25°C<br>Maximum supply voltage. | | | | |
| a. Qualification | | | (a) 4(0)<br>2(0) | (a) 6/<br>8/ | (a) 22(0) | 7/ |
| b. QCI | | | (b) 4(0)<br>2(0) | (b) 6/<br>8/ | (b) 22(0) | 7/ |
| End-point electrical parameters | | As specified in accordance with associated detail specification. | | | | |
| Subgroup 3 9/ | | | | | | |
| Power transistor electrical dose rate test | 3478 | +25°C | 11(0) | 3/ | 11(0) | 4/ |
| End-point electrical parameters | | As specified in accordance with associated detail specification. | | | | |

1/ Parts used for one subgroup test may not be used for other subgroups but may be used for higher levels in the same subgroup. Total exposure shall not be considered cumulative unless testing is performed within the time limits of the test method. Group D tests may be performed prior to device screening (see 4.7.7).

2/ Waive neutron tests for MOS devices unless by design, bipolar elements are an integral part of the device function.

3/ In accordance with wafer lot. If one part fails, seven additional parts may be added to the test sample with no additional failures allowed, 18 devices, c = 1.

4/ In accordance with inspection lot. If one part fails, seven additional parts may be added to the test sample with no additional failures allowed, 18 devices, c = 1.

5/ JANTXV devices shall be inspected using either the JANTXV quantity/accept number criteria as specified, or by using the JANS criteria on each wafer.

6/ For device types with greater than or equal to 4,000 die per wafer, selected from the wafer at a radius approximately equal to two-thirds of the wafer radius, and spaced uniformly around this radius.

7/ In accordance with inspection lot. If one part fails, 16 additional parts may be added to the test sample with no additional failures allowed, 38 devices, c = 1. For devices which require more than one bias, the sample size shall be 22 (0) for each bias.

8/ For device types with less than or equal to 4,000 die per wafer, selected from the wafer at a radius approximately equal to two-thirds of the wafer radius and spaced uniformly around this radius.

9/ Upset testing during qualification on first QCI shall be conducted when specified in purchase order or contract. When specified, the same devices may be tested in more than one subgroup.

TABLE VII. Group E inspections (all quality levels) for qualification only.

| Inspections | MIL-STD-750 | | Sampling plan |
|---|---|---|---|
| | Method | Condition | |
| Subgroup 1 | | | |
| Thermal shock and/or Electrical measurements | 1056 | 100 cycles or as specified | As specified |
| Temperature cycling Electrical measurements | 1051 | 500 cycles minimum or as specified. | |
| Subgroup 2 | | As specified. | |
| Intermittent operating life | 1037 | | As specified |
| Life test | 1042 | | |
| Electrical measurements or | | | |
| Steady-state operating life | 1026 | | |
| Electrical measurements or | | | |
| Blocking life | 1048 | | |
| Electrical measurements | | | |
| Subgroup 3 As specified | | As specified. | As specified |
| Destructive physical analysis | 2101 2102 | | |
| Subgroup 4 | | As specified. | 22 devices c = 0 |
| Thermal resistance | | | |
| Transistors, | | | |
| POWERFETs | 3161 | | |
| Bipolar | 3131 | | |
| Diodes | 3101 or 4081 | | |
| IGBT | 3103 | | |
| GaAs FET | 3104 | | |
| Subgroup 5 | | As specified. | 15 devices c = 0 |
| Barometric pressure (reduced) (required only on all devices with rated voltage > 200 V) | 1001 | | |

TABLE VIII. Data requirements for JANS devices.

| Data | |
|---|---|
| Wafer lot acceptance (see 4.3.1.2.1) | 1. SEM photographs (when applicable) |
| Screening (see 4.6) | 2. Electrical data |
| | 3. Radiographs |
| | 4. Screening data |
| Quality conformance (see 4.7) | 5. Electrical data |
| | 6. SEM photographs (when applicable) |
| | 7. Bond pull limits (when applicable) |
| | 8. Lot rejection report |
| | 9. QCI data (groups A, B, C, and D) |

5. PACKAGING

* 5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-S-19491, for direct Government sales only.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory.)

6.1 Acquisition requirements. Acquisition documents should specify the following:

a. Type designation (see 1.2).

b. Number of the applicable associated detail specifications (see 3.2 and supplement 1 of this document). For additional information of type designations not included in supplement 1, contact the Defense Electronics Supply Center, DESC-EL, Dayton, OH 45444.

c. Lead formation, length, finish, if other than that specified, or when a choice is required by the device application.

d. Data requirements when applicable (see 3.3, 4.1.1.3, and 4.9).

e. Specify point of shipment (facility other than the device manufacturer, see 4.1.1.1.5).

f. PIND screening when required (see 3.7.6.1 and 1.2.4).

g. Date code and specification revision letter shall not be restricted by the acquisition documents.

6.2 Supersession information. Devices covered by this specification are substitutable for the manufacturer's and user's PIN's. This information in no way implies that manufacturer's PINs are suitable as a substitute for the military PIN.

Supersession and cross reference data.

| Military PIN | Manufacturer's CAGE code | Manufacturer's and user's PIN |
|---|---|---|
| | | |

6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time set for opening of bids, qualified for inclusion in QPL, whether or not such products have actually been so listed by that date. The attention of the suppliers is called to this requirement, and manufacturers are urged to arrange to have the products that they propose to offer to the federal Government tested for qualification, in order that they may be eligible to be awarded contracts for the products covered by this specification. The activity responsible for the qualification products list is the Defense Electronics Supply Center, Dayton, OH 45444. Application for qualification tests shall be submitted on DESC Form 190 and shall include a proposed test plan, design and construction, DESC Form 360 and engineering evaluation as applicable.

6.4 Associated detail specification. Since this specification covers the general requirements and tests for semiconductor devices, the details of performance of the semiconductor device must be as specified in the associated detail specification. Attention of engineers preparing the associated detail specification is invited to the items listed below which should be covered in the associated detail specification:

a. Identification (see 1.2).

b. Design, construction, and material (see 3.6).

c. The marking to be omitted if any (see 3.7). The order of preference for marking is as listed in 3.7.1.

d. Classification of inspection.

(1) Examination and tests to be performed under qualification inspection.

(2) Examination and tests to be performed under QCI.

(3) Examination and tests to be performed under screening inspection.

e. End-point measurements to be made for group B, C, D, and E inspections (see 4.7.8).

f. Product assurance levels covered.

g. Device level and screening procedure if other than table II.

h. Sequence of test, test method, test condition, limit, cycles, temperature, axis, etc., when not specified, or if other than specified herein.

i. Interim (pre- and post-burn-in) electrical parameters.

j. Burn-in test condition and burn-in test circuit.

k. Delta parameter measurements or provisions for POA including procedures for traceability, where applicable.

l. Final electrical measurements.

m. Requirements for data recording and reporting, where applicable.

6.4.1 MIL-STD-750 details. In addition to the items as specified in 6.5, the applicable details required by MIL-STD-750 should be listed in the associated detail specification.

6.5 Associated detail specifications issued but not having a QPL source. See QPL 19500 note.

6.6 ISAs. Certain provisions of this specification are the subject of international standardization agreement. When amendment, revision, or cancellation of this specification is proposed which will affect or violate the international agreement concerned, the preparing activity will take appropriate reconciliation action through international standardization channels including departmental standardization offices, if required.

6.7 Subject term (key word) listing.

Thryistors
Radiation designators
Unencapsulated devices
Beryllium oxide
ISA
PIND
Rectifiers
Radiography
Neutron irradiation

6.8 Changes from previous issue. The margins of this specification are marked with asterisks to indicate where changes (additions, modifications, corrections, deletions) from the previous issue were made. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations and relationship to the last previous issue.

APPENDIX A

DEFINITIONS

10. SCOPE

10.1 Scope. This appendix contains the definitions of terms used with semiconductor devices. This appendix is a mandatory part of the specification. The information contained herein is intended for compliance.

20. APPLICABLE DOCUMENTS. This section is not applicable to this appendix.

30. SEMICONDUCTOR COMMON DEFINITIONS

30.1 Absolute maximum ratings. The values specified for "ratings", "maximum ratings", or "absolute maximum ratings" are based on the "absolute system" and unless otherwise required for a specific test method are not to be exceeded under any service or test conditions. These ratings are limiting values beyond which the serviceability of any individual semiconductor device may be impaired. Unless otherwise specified, the voltage, current, and power ratings are based on continuous dc power conditions at free air ambient temperature of +25°C. For pulsed or other conditions or operation of similar nature, the current, voltage, and power dissipation ratings are a function of time and duty cycle. In order not to exceed absolute ratings, the equipment designer has the responsibility of determining an average design value, for each rating, below the absolute value of that rating by a safety factor, so that the absolute values will never be exceeded under any usual conditions of supply-voltage variation, load variation, or manufacturing variation in the equipment itself.

30.2 Ambient temperature. Ambient temperature is the air temperature measured below a semiconductor device, in an environment of substantially uniform temperature, cooled only by natural air convection and not materially affected by reflective and radiant surfaces.

30.3 Anode. The electrode from which the forward current flows within the device.

30.4 Blocking. A term describing the state of a semiconductor device or junction which eventually prevents the flow of current.

30.5 Breakdown voltage. The breakdown voltage is the maximum instantaneous voltage, including repetitive and nonrepetitive transients, which can be applied across a junction in the reverse direction without an external means (circuit) of limiting the current. It is also the instantaneous value of reverse voltage at which a transition commences from a region of high small-signal impedance to a region of substantially lower small-signal impedance.

30.6 Case mount. A type of package (outline) which provides a method of readily attaching one surface of the semiconductor device to a heat dissipator to achieve thermal management of the case temperature (example: TO-3, DO-4).

30.7 Case temperature. Case temperature is that temperature measured at a specified point on the case of a semiconductor device.

30.8 Cathode. The electrode to which the forward current flows within the device.

30.9 Characteristic. An inherent and measurable property of a device. Such a property may be electrical, mechanical, thermal, hydraulic, electromagnetic, or nuclear, and can be expressed as a value for stated or recognized conditions. A characteristic may also be a set of related values usually shown in graphical form.

30.10 Constant current source. A current source shall be considered constant if halving the generator impedance does not produce a change in the parameter being measured that is greater than the required precision of the measurement.

30.11 Constant voltage source. A voltage source shall be considered constant if doubling the generator impedance does not produce a change in the parameter being measured that is greater than the required precision of the measurement.

30.12 Disc type. A type of package (outline) for very high power devices which provides two parallel surfaces for mounting into a specialized heat dissipator capable of applying a specified compressive force to the device.

30.13 Forward bias. The bias which tends to produce current flow in the forward direction (p type semiconductor region at a positive potential relative to n type region).

* 30.14 Metallurgical bond, diode construction, and thermal matching. Metallurgical bonds as used in JAN-brand semiconductor devices will be identified by one of the following categories. The listing of the three types of metallurgical bonds is for clarification and may not necessarily be listed in order of merit.

30.14.1 Double plug construction. Double plug construction is one where the terminal plugs have equal nominal diameters and are in direct contact with the metallization materials of the semiconductor die; the use of a point contact whisker or other wire conductors is not allowed.

30.14.2 Dash-one construction. Dash-one diodes shall be of double plug construction utilizing high temperature metallurgical bonding between both sides of the silicon die and terminal pins.

* 30.14.3 Category I metallurgical bond. A category I metallurgical bond is formed when the bond between the semiconductor element (silicon, germanium, etc.) and the package consists of a phase which melts during the bonding process and which includes in the solidified melt both a portion of the semiconductor element and a portion of the metallization layer which is on the package mounting surface. Category I bonds between adjacent semiconductor elements (as in stacks) shall include portions of both semiconductor elements in the solidified melt. Category I metallurgical bonds are typically required for all axial leaded diodes, equal to and greater than 1 watt or 1 amp, unless otherwise specified in the detail specification.

30.14.4 Category II metallurgical bond. A category II metallurgical bond is formed utilizing a brazing or soldering alloy which melts during the bonding process and bonds to a metallization layer on each of the surfaces being joined. Dissolution of the semiconductor element or any of the wetted surface layers is not required.

30.14.5 Category III metallurgical bond. A category III metallurgical bond is formed when the surfaces to be bonded are brought together under conditions of temperature and pressure such that a diffusion bond is formed between the outermost metallization layer of the elements being joined. This bond is characterized by having species from both sides of the original interface diffused across the interface without any molten phase having been present.

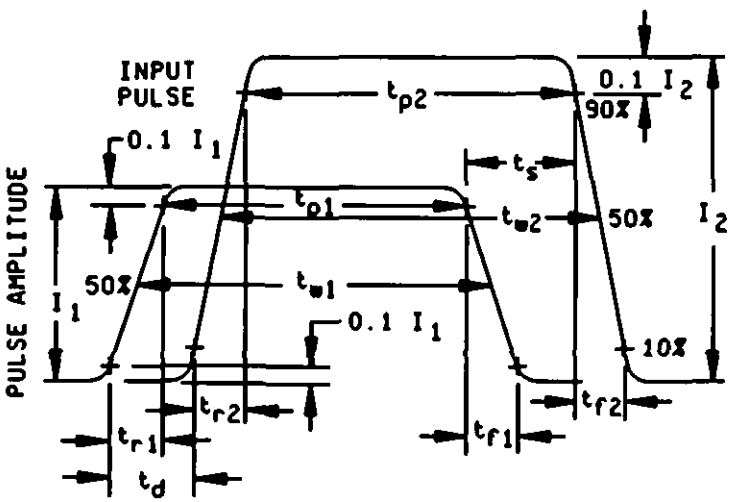
30.14.6 Non-cavity double plug diode. Double plug construction where the package glass is in intimate contact with the semiconductor die isolating the anode and cathode regions, and insuring immunity from particle related failures. Voids may be present provided isolation (to prevent arcing) and particle immunity are insured.

* 30.14.7 Thermally matched axial leaded diodes. Diode construction within the coefficients of thermal expansion of the die, plug, and package materials shall be thermally matched such that the diodes are immune to intermittent opens by design. Axial-leaded diode designs which comply with this definition must utilize tungsten or molybdenum plugs.

* 30.14.8 Metallurgically bonded-thermally matched-noncavity-double plug construction. Axial-leaded diodes meeting this definition must be of double plug construction utilizing tungsten or molybdenum plugs. Both sides of the diode chip (die) must be bonded to the corresponding plug by a category I metallurgical bond. The package must be thermally matched, non-cavity construction (see 30.14.1 through 30.14.7). The plate silver bottom contact design is not permitted.

30.15 Noise figure. At a selected input frequency, the noise figure is the ratio of the total noise power per unit bandwidth (at a corresponding output frequency) delivered to the output termination, to the portion thereof contributed at the input frequency by the input termination, whose noise temperature is standard (293°K) at all frequencies.

30.16 Open circuit. A circuit shall be considered as open circuited if halving the magnitude of the terminating impedance does not produce a change in the parameter being measured greater than the specified accuracy of the measurement.




$t_r$ = Pulse rise time.

$t_d$ = Pulse delay time.

$t_p$ = Pulse time.

$t_s$ = Pulse storage time.

$t_f$ = Pulse fall time.

$t_w$ = Pulse average time.

I = Pulse amplitude.

NOTES:
1. Subscript 2 denotes output.
2. Subscript 1 denotes input.

FIGURE 4. Pulse measurements.

30.17 Package type. A package type is a package which has the same case outline, configuration, materials (including bonding, wire, or ribbon and die attach) piece parts (excluding preforms which differ only in size) and assembly processes.

30.18 Pulse. A pulse is a flow of electrical energy of short duration. See figure 4 for illustrations of the characteristics defined in 30.19 to 30.24, inclusive.

30.19 Pulse average time. The average pulse time of a pulse is the time duration from a point on the leading edge which is 50 percent of the maximum amplitude to a point on the trailing edge which is 50 percent of the maximum amplitude.

30.20 Pulse delay time. The delay time of a pulse is the time interval from a point at which the leading edge of the input pulse has risen to 10 percent of its maximum amplitude to a point at which the leading edge of the output pulse has risen to 10 percent of its maximum amplitude.

30.21 Pulse fall time. The fall time of a pulse is that time duration during which the amplitude of its trailing edge is decreasing from 90 to 10 percent of the maximum amplitude.

30.22 Pulse rise time. The rise time of a pulse is that time duration during which the amplitude of its leading edge is increasing from 10 to 90 percent of the maximum amplitude.

30.23 Pulse storage time. The storage time of a pulse is the time interval from a point 10 percent down from the maximum amplitude on the trailing edge of the input pulse to a point 10 percent down from the maximum amplitude on the trailing edge of the output pulse.

30.24 Pulse time. The pulse time of a pulse is the time interval from the point on the leading edge which is 90 percent of the maximum amplitude, to the point on the trailing edge which is 90 percent of the maximum amplitude.

30.25 Radiation failures. A radiation failure is defined at the lowest radiation level when either any device parameter exceeds its specified post irradiation parameter limits (PIPL) or the device fails any functional test in accordance with stated test conditions.

* 30.26 Radiation hardness assurance (RHA). That portion of product assurance testing that assures that parts meet the radiation response characteristics as specified in this specification and the detail specification.

30.27 Rating. The nominal value of any electrical, thermal, mechanical, or environmental quantity assigned to define the operating conditions under which a component, machine, apparatus, electronic device, etc. is expected to give satisfactory service.

30.28 Reverse bias. The bias which tends to produce current flow in the reverse direction (n type semiconductor region at a positive potential relative to the p type region).

30.29 Semiconductor diode. A semiconductor device having two terminals and exhibiting a nonlinear voltage-current characteristic.

30.30 Semiconductor junction. A region of transition between semiconductor regions of different electrical properties (e.g., n-n+, p-n, p-p+ semiconductors) or between a metal and a semiconductor.

30.31 Short circuit. A circuit shall be considered short-circuited if doubling the magnitude of the terminating impedance does not produce a change in the parameter being measured that is greater than the specified accuracy of the measurement.

30.32 Small signal. A signal shall be considered small if doubling its magnitude does not produce a change in the parameter being measured that is greater than the specified accuracy of the measurement.

30.33 Storage temperature. Storage temperature is a temperature at which the device may be stored without any power being applied.

30.34 Temperature coefficient. The ratio of the change in a parameter to the change in temperature.

30.35 Thermal compression bond. A bond achieved when pressure and temperature are present regardless of how the temperature rise was achieved except without ultrasonic assist.

30.36 Thermal equilibrium. Thermal equilibrium is reached when doubling the test time interval does not produce a change, due to thermal effects, in the parameter being measured that is greater than the specified accuracy of the measurement.

30.37 Thermal resistance. Thermal resistance is the temperature rise, per unit power dissipation, of a junction above the temperature of a stated external reference point under conditions of thermal equilibrium.

30.38 Thyristor. A BISTable semiconductor device that comprises three or more junctions and can be switched from the off state or on state to the opposite state.

30.39 Transistor. An active semiconductor device capable of providing power amplification and having three or more terminals.

30.40 Expanded metallization. Expanded metallization is metallization that increases in area (example, metal line to bond pad area) (see figure 5).

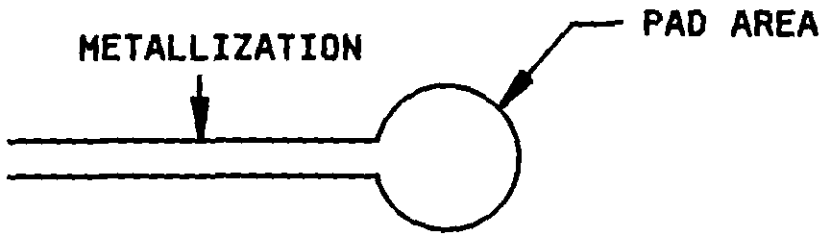



FIGURE 5. Example of expanded metallization.

30.41 Impulse waveform. A pulse with a defined virtual front and impulse duration for either a voltage or current amplitude of unidirectional polarity.

30.42 Virtual front duration. The pulse time as defined by 1.67 times time for voltage to increase from 30 percent to 90 percent of crest (peak value) or 1.25 times time for current to increase from 10 percent to 90 percent of crest.

30.43 Impulse duration. The time required for an impulse waveform to decay to 50 percent of the peak value measured from the start of the virtual front duration of zero crossover.

30.44 Line. A collection of similar water fabrication flows, or similar package assembly flows used to manufacture semiconductors in accordance with a specified process flow.

40. TRANSISTORS

40.1 Junction transistor, multijunction types.

40.1.1 Base. A region which lies between an emitter and collector of a transistor and into which minority carriers are injected.

40.1.2 Collector. A region through which a primary flow of charge carriers leaves the base.

40.1.3 Cutoff current. The cutoff current is the measured value of dc current when a transistor is reverse biased by a voltage less than the breakdown voltage.

40.1.4 Emitter. A region from which charge carriers that are minority carriers in the base are injected into the base.

40.1.5 Junction, collector. A semiconductor junction, normally biased in the reverse direction, the current through which can be controlled by the introduction of minority carriers into the base.

40.1.6 Junction, emitter. A semiconductor junction normally biased in the forward direction to inject minority carriers into the base.

40.1.7 Saturation. A base current and a collector current condition resulting in a forward-biased collector junction.

40.2 Unijunction transistors.

40.2.1 Peak point. The point on the emitter current-voltage characteristic corresponding to the lowest current at which the change in emitter base voltage with respect to emitter current equals zero.

40.2.2 Unijunction transistor. A three-terminal semiconductor device having one junction and a stable negative-resistance characteristic over a wide temperature range.

40.2.3 Valley point. The point on the emitter current-voltage characteristic corresponding to the second lowest current at which the change in emitter base voltage with respect to emitter current equals zero.

40.3 Field-effect transistors (FET).

40.3.1 Depletion-mode operation. The operation of a FET such that changing the gate to source voltage from zero to a finite value decreases the magnitude of the drain current.

40.3.2 Depletion-type-FET. A FET having appreciable channel conductivity for zero gate to source voltage. The channel conductivity may be increased or decreased according to the polarity of the applied gate to source voltage.

40.3.3 Drain. A region into which majority carriers flow from the channel.

40.3.4 Enhancement-mode operation. The operation of a FET such that changing the gate to source voltage from zero to a finite value increases the magnitude of the drain current.

40.3.5 Enhancement-mode FET. A FET having substantially zero channel conductivity for zero gate to source voltage. The channel conductivity may be increased by the application of a gate to source voltage of appropriate polarity.

40.3.6 FET. A transistor in which the conduction is due entirely to the flow of majority carriers through a conduction channel controlled by an electric field arising from a voltage applied between the gate and source terminals.

40.3.7 Gate. The electrode associated with the region in which the electric field due to the control voltage is effective.

40.3.8 Insulated-gate FET. A FET having one or more gate electrodes which are electrically insulated from the channel.

40.3.9 Junction-gate FET. A FET that uses one or more gate regions to form p-n junction(s) with the channel.

40.3.10 MOSFET. An insulated gate FET in which the insulating layer between each gate electrode and the channel is oxide material.

40.3.11 N-channel FET. A FET that has an n type conduction channel.

40.3.12 P-channel FET. A FET that has a p type conduction channel.

40.3.13 Source. A region from which majority carriers flow into the channel.

40.4 Insulated-gate-bipolar-transistor.

50. DIODES AND RECTIFIERS

50.1 Signal diodes and rectifier diodes.

50.1.1 Semiconductor rectifier diode. A device having an asymmetrical voltage-current characteristic used for rectification.

50.1.2 Semiconductor signal diode. A device having an asymmetrical voltage-current characteristic and used for signal detection.

50.2 Microwave diodes.

50.2.1 Detector diode. A device which converts rf energy into dc or video output.

50.2.2 Gunn diode. A microwave diode that exhibits negative resistance arising from the bulk negative differential conductivity occurring in several compound semiconductors such as gallium arsenide, and that operates at a frequency determined by the transit time of charge bunches formed by this negative differential conductivity.

50.2.3 IMPATT diode (Impact, avalanche and transit time diode). A semiconductor microwave diode that, when its junction is biased into avalanche, exhibits a negative resistance over a frequency range determined by the transit time of charge carriers through the depletion region.

50.2.4 LSA diode (limited space-charge accumulation diode). A microwave diode similar to the Gunn diode except that it achieves higher output power at frequencies, determined by the microwave cavity, that are several times greater than the transit-time frequency by avoiding the formation of charge bunches or domains.

50.2.5 Matched pair. A pair of diodes identical in outline dimensions and with matched electrical characteristics. The two diodes may both be forward polarity,or one forward and one reverse polarity, or both reverse polarity.

50.2.6 Microwave diode. A two terminal device that is responsive in the microwave region of the electromagnetic spectrum, commonly regarded as extending from 1 to 300 GHz.

50.2.7 Mixer diode. A microwave diode that combines rf signals at two frequencies to generate an rf signal at a third frequency.

50.2.8 TRAPATT diode (trapped plasma avalanche transit time diode). A microwave diode that, when its junction is biased into avalanche, exhibits a negative resistance at frequencies below the transit time frequency range of the diode due to generation and dissipation of trapped electron-hole plasma resulting from the intimate interaction between the diode and a multiresonant microwave cavity.

50.3 Tunnel diodes.

50.3.1 Tunnel diodes. A device in which quantum-mechanical tunneling leads to a region of negative slope in the forward direction of the current-voltage characteristic.

50.3.2 Backward diode. A device in which quantum-mechanical tunneling leads to a current-voltage characteristic with a reverse current greater than the forward current, for equal and opposite applied voltages.

50.4 Voltage-regulator and voltage-reference diodes.

50.4.1 Voltage-reference diode. A diode which is normally biased to operate in the breakdown region of its voltage-current characteristic and which develops across its terminals a reference voltage of specified accuracy, when biased to operate throughout a specified current and temperature range.

50.4.2 Voltage-regulator diode. A diode which is normally biased to operate in the breakdown region of its voltage-current characteristic and which develops across its terminals an essentially constant voltage throughout a specified current range.

50.5 Current-regulator diodes.

50.5.1 Current-regulator diode. A diode which limits current to an essentially constant value over a specified voltage range.

50.6 Varactor diodes.

50.6.1 Varactor diode. A two terminal semiconductor device in which use is made of the property that its capacitance varies with the applied voltage.

50.6.2 Tuning diode. A varactor diode used for rf tuning including functions such as automatic frequency control (AFC) and automatic fine tuning (AFT).

50.7 Transient voltage suppressors.

50.7.1 Varistor. A transient voltage suppressor that is a nonlinear resistor with symmetrical characteristics.

50.7.2 Avalanche-junction. A transient voltage suppressor that is a semiconductor diode that can operate in either the forward or reverse direction of its voltage-current characteristic to limit voltage transients.

50.7.3 Clamping voltage. The voltage in a region of low differential resistance that serves to limit the transient voltage across the device terminals.

50.7.4 Clamping factor. The ratio of clamping voltage to breakdown voltage.

50.7.5 Peak impulse current. The peak current for a series of essentially identical impulses.

50.7.6 Standby current. The dc current through a transient voltage suppressor at rated standoff voltage.

50.7.7 Repetitive peak pulse power. The peak power dissipation resulting from the peak impulse current $I_{pp}$.

50.7.8 Response time. The time interval between the point on the impulse waveform at which the amplitude exceeds the clamping voltage level and the peak of the voltage overshoot.

50.7.9 Voltage overshoot. The excess voltage over the clamping voltage that occurs when a current impulse having short virtual front duration is applied.

50.7.10 Forward surge current. The peak current for a single impulse for forward biased diode.

50.7.11 Working peak voltage. The peak voltage, excluding all transient voltage, usually referred to as standoff voltage.

60. CLASSES OF THYRISTORS

60.1 Thyristor. A bistable semiconductor device that comprises three or more junctions and can be switched between conducting and nonconducting status.

60.1.1 Bidirectional diode thyristor. A two terminal thyristor having substantially the same switching behavior in the first and third quadrants of the principal voltage-current characteristic.

60.1.2 Bidirectional triode thyristor. An n-gate or p-gate thyristor having substantially the same switching behavior in the first and third quadrants of the principal voltage-current characteristic.

60.1.3 N-gate thyristor. A three-terminal thyristor in which the gate terminal is connected to the n-region adjacent to the region to which the anode terminal is connected and that is normally switched to the on-state by applying a negative signal between gate and anode terminals.

60.1.4 P-gate thyristor. A three-terminal thyristor in which the gate terminal is connected to the p-region adjacent to the region to which the cathode terminal is connected and that is normally switched to the on-state by applying a positive signal between gate and cathode terminals.

60.1.5 Reverse blocking diode thyristor. A two-terminal thyristor that switches only for positive anode to cathode voltages and exhibits a reverse blocking state for negative anode to cathode voltages.

60.1.6 Reverse blocking triode thyristor. An n-gate or p-gate thyristor that switches only for positive anode to cathode voltages and exhibits a reverse blocking state for negative anode to cathode voltages.

60.1.7 Reverse conducting diode thyristor. A two terminal thyristor that switches only for positive anode to cathode voltages and conducts large currents at negative anode to cathode voltages comparable in magnitude to the on-state voltage.

60.1.8 Reverse conducting triode thyristor. An n-gate or p-gate thyristor that switches only for positive anode to cathode voltages and conducts large currents at negative anode to cathode voltages comparable in magnitude to the on-state voltages.

60.1.9 Turn off thyristor. A thyristor that can be switched between conducting and nonconducting states by applying control signals of appropriate polarities to the gate terminal, with the ratio of triggering power to triggered power appreciably less than one.

60.2 Physical structure terms.

60.2.1 Gate. An electrode connected to one of the semiconductor regions for introducing control current.

60.2.2 Main terminals. The two terminals through which the principal current flows.

60.3 Electrical characteristic and rating terms.

60.3.1 Anode to cathode voltage-current characteristic (anode characteristic). A function, usually represented graphically, relating the anode to cathode voltage to the principal current, with gate current where applicable, as a parameter.

60.3.2 Breakover point. Any point on the principal voltage-current characteristic for which the differential resistance is zero and where the principal voltage reaches a maximum value.

60.3.3 Negative differential resistance region. Any portion of the principal voltage-current characteristic in the switching quadrant within which the differential resistance is negative.

60.3.4 Off impedance. The differential impedance between the terminals through which the principal current flows when the thyristor is in the off state.

60.3.5 Off state. The condition of a thyristor corresponding to the high resistance low current portion of the principal voltage-current characteristic between the origin and the breakover point in the switching quadrant.

60.3.6 On impedance. The differential impedance between the terminals through which the principal current flows when the thyristor is in the on state.

60.3.7 On state. The condition of a thyristor corresponding to the low resistance, low voltage portion of the principal voltage-current characteristic in the switching quadrant.

60.3.8 Principal current. A generic term for the current through the device excluding gate current.

60.3.9 Principal voltage. The voltage between the main terminals.

60.3.10 Principal voltage-current characteristic (principal characteristic). A function, usually represented graphically, relating the principal voltage to the principal current, with gate current where applicable, as a parameter.

60.3.11 Reverse blocking impedance. The differential impedance between the two terminals through which the principal current flows when the thyristor is in the reverse blocking state at a stated operating point.

60.3.12 Reverse blocking state. The condition of a reverse blocking thyristor corresponding to the portion of the anode to cathode voltage-current characteristic for which the reverse currents are of lower magnitude than the reverse breakdown current.

60.3.13 Switching quadrant. A quadrant of the principal voltage-current characteristic in which a device is intended to switch between an off state and an on state.

70. OPTOELECTRONIC DEVICES

70.1 Optoelectronic device. A device that is responsive to or that emits or modifies electromagnetic radiation in the visible, infrared, or ultraviolet spectral regions; or a device that utilizes such electromagnetic radiation for its internal operation.

70.1.1 Conversion efficiency. The ratio of maximum available power output resulting from photovoltaic operation to total incident radiant flux.

70.1.2 Dark condition. The condition attained when the electrical parameter under consideration approaches a value which cannot be altered by further irradiation shielding.

70.1.3 Dark current. The current that flows through a photosensitive device in the dark condition.

70.1.4 Light current. The current that flows through a photosensitive device when it is exposed to radiant energy.

70.1.5 Photoconductive diode. A photodiode that is intended to be used as a photoconductive transducer.

70.1.6 Photocurrent. The difference in magnitude between light current and dark current.

70.1.7 Photodiode. A diode that is intended to be responsive to radiant energy.

70.1.8 Photodiode, avalanche. A photodiode that is intended to take advantage of avalanche multiplication of photocurrent.

70.1.9 Photoemitter. A device that emits electromagnetic radiation in the visible, infrared, or ultraviolet spectral regions.

70.1.10 Photosensitive device. A device that is responsive to electromagnetic radiation in the visible, infrared, or ultraviolet spectral regions.

70.1.11 Photothyristor. A thyristor that is intended to be responsive to radiant energy for controlling its operation as a thyristor.

70.1.12 Phototransistor. A transistor that is intended to be responsive to radiant energy.

70.1.13 Photovoltaic diode. A photodiode that is intended to generate a terminal voltage in response to radiant energy.

70.2 Photoemitting devices.

70.2.1 Avalanche luminescent diode. A light emitting diode that emits luminous energy when a controlled reverse current in the breakdown region is applied.

70.2.2 Infrared emitting diode. A diode capable of emitting radiant energy in the infrared region of the spectrum resulting from the recombination of electrons and holes.

70.2.3 Light emitting diode. A diode capable of emitting luminous energy resulting from the recombination of electrons and holes.

70.2.4 Radiant efficiency. The ratio of the total radiant flux emitted to the total input power.

70.3 Opto-couplers.

70.3.1 Photodarlington coupler. An opto-coupler in which the photo-sensitive element is a darlington connected phototransistor.

70.3.2 Photodiode coupler. An opto-coupler in which the photosensitive element is a photodiode.

70.3.3 Photothyristor coupler. An opto-coupler in which the photosensitive element is a photothyristor.

70.3.4 Phototransistor coupler. An opto-coupler in which the photosensitive element is a phototransistor.

80. ELECTRICAL AND ENVIRONMENTAL STRESS SCREENING.

a. Electrical stressing near maximum rating of semiconductor devices is performed to remove devices within a given lot which are subject to early life failures due to improper processing.

b. Determine if wear-out mechanisms are present in a given lot which will shorten the time to failure (life tests).

80.1 Power burn-in. A generic term describing a screening test which operates the device by internally dissipating sufficient power to significantly heat the device junction for a specified time.

80.1.1 Rectifying ac power burn-in. Power burn-in whereby junction heating is accomplished through the alternate application every half cycle of forward current and reverse voltage.

80.1.2 Steady-state dc power burn-in. Power burn-in whereby junction heating is accomplished through the application of steady-state forward current, reverse current, or forward power for diodes (including rectifiers), zeners, and transistor respectively.

80.2 High temperature reverse bias. A generic term describing a screening test which applies a blocking voltage and is normally performed at $T_A$ = +150°C through the external application of heat.

80.2.1 Steady-state dc high temperature reverse bias. High temperature reverse bias which applies steady-state dc blocking voltage.

80.2.2 Half-wave high temperature reverse bias. High temperature reverse bias which applies half-wave blocking voltage.

80.2.3 Full-wave high temperature blocking bias. High temperature reverse bias which applies full-wave blocking voltage; sometimes applicable to symmetrical thyristors or transient voltage suppressors.

80.3 Operating life. A generic term describing a sample test which operates and internally heats a device junction for an extended time to verify lot integrity. This is generally an extension of power burn-in.

80.3.1 Rectifying ac operating life. Operating life whereby heating is accomplished through the alternate application of forward current and reverse voltage.

80.3.2 Steady-state dc operating life. Operating life whereby heating is accomplished through the application of steady-state forward current, reverse current, or forward power for diodes (including rectifiers), zeners, and transistors respectively.

80.3.3 Intermittent operating life. Operating life whereby $T_J$ and $T_C$ is cycled through a specified temperature range by a heating current or power and a cooling period, when current or power is removed.

80.3.3.1 Rectifying ac intermittent operating life. Intermittent operating life whereby the device is subjected to forward current and reverse voltage, during the heating period.

80.3.3.2 DC intermittent operating life. Intermittent operating life whereby the device is subjected to steady-state forward current or equivalent half sine forward current, during the heating period. This test is also known as power cycling or thermal fatigue.

80.4 Blocking life. A generic term describing a sample test which applies a blocking voltage and is normally performed at a specified high ambient or case temperature through the external application of heat.

80.4.1 Steady-state dc blocking life. Blocking life which applies steady-state dc blocking voltage.

80.4.2 Half-wave blocking life. Blocking life which applies half-wave blocking voltage.

80.4.3 Full-wave blocking life. Blocking life which applies full-wave blocking voltage.

80.5 Temperature cycling (air to air). Temperature cycling at device's case temperature through a specified range by the external heating and cooling of the device in an air to air environment.

80.6 Thermal shock (liquid to liquid). Thermal shock cycling at device's case temperature through a specified range by the external heating and cooling of the device in a liquid to liquid environment.

80.7 Thermal response. Thermal response for the purpose of this specification is the application of an electrical stress sufficient to pass heat through the interface of dissimilar materials, primarily to determine the quality of attachment by measuring the electrical characteristics of the temperature sensitive parameter.

* 80.8 Surge. Surge is the application of a high peak current ten times (minimum) the device average current maximum rating applied for a short pulse width appropriate to determine processing defects (e.g., wire bond integrity, micro cracks, and bond voids).

APPENDIX B

ABBREVIATIONS AND SYMBOLS

10. SCOPE

10.1 Scope. This appendix covers the abbreviations and symbols for use with semiconductor devices. This appendix is a mandatory part of the specification. The information contained herein is intended for compliance.

20. APPLICABLE DOCUMENTS. This section is not applicable to this appendix.

30. SEMICONDUCTOR, GENERAL

30.1 Definitions.

| | |
|---|---|
| ACF | Automatic frequency control |
| AFT | Automatic fine tuning |
| BIST | Backward instability shock test |
| ESD | Electrostatic discharge |
| ESDS | Electrostatic discharge sensitive |
| FET | Field-effect transistor |
| FIST | Forward instability shock test |
| GaAs | Gallium arsenide |
| HTRB | High temperature reverse bias |
| IGBT | Insulated gate bipolar transistor |
| IMPATT | Impact, avalanche, and transit time diode |
| LSA | Limited space-charge accumulation |
| MOSFETS | Metal oxide semiconductor field-effect transistors |
| OEM | Original equipment manufacturer |
| PDA | Percent defective allowed |
| PIN | Part or identifying number |
| PIND | Particle impact noise detector |
| PIPL | Post-irradiation parameter limits |
| PPM | Parts per million |
| QCI | Quality conformance inspection |
| QPL | Qualified products list |
| RHA | Radiation hardness assurance |
| RHAPM | Radiation hardness assurance part managers |

| | | |
|---|---|---|
| | RMS | *Root means square* |
| | SEM | Scanning electron microscope |
| | SOA | Safe operating area |
| | SPC | Statistical process control |
| | TP | True position |
| | *TRAPATT* | Trapped *plasma avalanche transit time diode* |
| | UHF | Ultra high frequency |

30.1 Symbols.

| | Old symbol | |
|---|---|---|
| | F | Spot noise figure (NF) |
| | F | Average noise figure |
| | $R_{\Theta}$ | Thermal resistance ($\Theta$) |
| | $R_{\Theta CA}$ | Thermal resistance, case to ambient |
| | $R_{\Theta JA}$ | Thermal resistance, junction ($\Theta_{J-A}$) to ambient |
| | $R_{\Theta JC}$ | Thermal resistance, junction ($\Theta_{J-C}$) to case |
| | $R_{\Theta JL}$ | Thermal resistance, junction to lead |
| | $R_{\Theta JR}$ | Thermal resistance, junction to reference |
| | $T_A$ | Ambient or free air temperature |
| | $T_C$ | Case temperature |
| * | TEC | End cap temperature |
| | $T_J$ | Junction temperature |
| * | TL | Lead temperature |
| | $T_{op}$ | Operating temperature |
| | $T_{STG}$ | Storage temperature |
| | $t_d$ | Delay time |
| | $t_f$ | Fall time |
| | $t_{off}$ | Turn off time |
| | $t_{on}$ | Turn on time |
| | $t_p$ | Pulse time |
| | $t_r$ | Rise time |

| | |
|---|---|
| $t_s$ | Storage time |
| $t_w$ | Pulse average time |
| $V_{(BR)}$ | Breakdown voltage (BV) |

40. TRANSISTORS

40.1 Junction transistors, multijunction types.

| | |
|---|---|
| $C_{ibo}$, $C_{ieo}$ | Input capacitance, (common base, common emitter) collector open circuited for ac |
| $C_{ibs}$, $C_{ies}$ | Input capacitance, (common base, common emitter) collector short-circuited to reference terminal for ac |
| $C_{obo}$, $C_{oeo}$ | Output capacitance, (common base, common emitter) input open circuited to ac |
| $C_{obs}$, $C_{oes}$ | Output capacitance, (common base, common emitter) input short-circuited to reference terminal for ac |
| $f_{hfb}$, $f_{hfc}$, $f_{hfe}$ | Small signal, short-circuit forward current transfer ratio cutoff frequency (common base, common collector, common emitter) |
| $f_{max}$ | Maximum frequency of oscillation |
| $f_T$ | Extrapolated unity gain frequency |
| $g_{MB}$, $g_{MC}$, $g_{ME}$ | Static transconductance (common base, common collector, common emitter) |
| $g_{mb}$, $g_{mc}$, $g_{me}$ | Small signal transconductance (common base, common collector, common emitter) |
| $G_{pB}$, $G_{pC}$, $G_{pE}$ | Large signal insertion power gain (common base, common collector, common emitter) |
| $G_{pb}$, $G_{pc}$, $G_{pe}$ | Small signal insertion power gain (common base, common collector, common emitter) |
| $h_{FB}$, $h_{FC}$, $h_{FE}$ | Static forward current transfer ratio (common base, common collector, common emitter) |
| $h_{fb}$, $h_{fc}$, $h_{fe}$ | Small signal short circuit forward current transfer ratio (common base, common collector, common emitter) |
| $\lvert h_{fe} \rvert$ | Magnitude of common emitter small signal short circuit forward current transfer ratio |
| $h_{IB}$, $h_{IC}$, $h_{IE}$ | Static input resistance (common base, common collector, common emitter) |
| $h_{ib}$, $h_{ic}$, $h_{ie}$ | Small signal short circuit input impedance (common base, common collector, common emitter) |
| $h_{ob}$, $h_{oc}$, $h_{oe}$ | Small signal open circuit output admittance (common base, common collector, common emitter) |

APPENDIX B

| | |
|---|---|
| $h_{rb}$, $h_{rc}$, $h_{re}$ | Small signal open circuit reverse voltage transfer ratio (common base, common collector, common emitter) |
| $I_B$ | Base current (dc) |
| $I_C$ | Collector current (dc) |
| $I_E$ | Emitter current (dc) |
| $i_B$ | Base current (instantaneous total value) |
| $i_C$ | Collector current (instantaneous total value) |
| $i_E$ | Emitter current (instantaneous total value) |
| $I_{CBO}$ | Collector cutoff current (dc) emitter open |
| $I_{CEO}$ | Collector cutoff current (dc) base open |
| $I_{CER}$ | Collector cutoff current (dc) with specified resistance between base and emitter |
| $I_{CES}$ | Collector cutoff current (dc) base short circuited to emitter |
| $I_{CEV}$ | Collector cutoff current (dc) with specified voltage between base and emitter |
| $I_{CEX}$ | Collector cutoff current (dc) with specified circuit between base and emitter |
| $I_{EBO}$ | Emitter cutoff current (dc) collector open |
| $I_{ECS}$ | Emitter cutoff current (dc) base short-circuited to collector |
| $I_S$ | Collector efficiency |
| $P_C$ | Collector power dissipation |
| $P_T$ | Total power dissipation, all terminals |
| $R_B$ | External base resistance |
| $r_b$ | Base spreading resistance |
| $r_{b'cc}$ | Collector-base time constant |
| $R_C$ | External collector resistance |
| $r_{CE(sat)}$ | Collector to emitter saturation resistance |
| $R_E$ | External emitter resistance |
| $r_{iep}$ | Small signal short circuit parallel input resistance (common emitter) |
| $t_c$ | $t_{OFF}$ crossover time (the time interval during which the collector voltage decreases from 10 percent of its peak off-state value and the collector current decreases to 10 percent of its peak on state value) |

APPENDIX B

| | |
|---|---|
| $V_{BB}$ | Base supply voltage |
| $V_{BE}$ | Base to emitter voltage (dc) |
| $V_{BE(sat)}$ | Base to emitter saturation voltage |
| $V_{(BR)CBO}$ | Breakdown voltage collector to base, emitter open |
| $V_{(BR)CEO}$ | Breakdown voltage collector to emitter, base open |
| $V_{(BR)CER}$ | Breakdown voltage collector to emitter, with specified resistance between base and emitter |
| $V_{(BR)CES}$ | Breakdown voltage collector to emitter, with base short-circuited to emitter |
| $V_{(BR)CEX}$ | Breakdown voltage collector to emitter, with specified circuit between base and emitter |
| $V_{(BR)EBO}$ | Breakdown voltage emitter to base, collector open |
| $V_{CB}$ | Collector to base voltage (dc) |
| $V_{CBF}$ | DC open circuit voltage (floating potential) between the collector and base, with the emitter biased in the reverse direction with respect to the base |
| $V_{CBO}$ | Collector to base voltage (static), emitter open |
| $V_{CC}$ | Collector supply voltage |
| $V_{CE}$ | Collector to emitter voltage (dc) |
| $V_{ce}$ | Collector to emitter voltage (rms) |
| $v_{ce}$ | Collector to emitter voltage (instantaneous) |
| $V_{CE(sat)}$ | Collector to emitter saturation voltage |
| $V_{CEO}$ | Collector to emitter voltage (static) base open |
| $V_{CEO(sus)}$ | Breakdown voltage, collector to emitter, sustained |
| $V_{CER}$ | Collector to emitter voltage (dc), with specified resistance between base and emitter |
| $V_{CES}$ | Collector to emitter voltage (dc), base short-circuited to emitter |
| $V_{EB}$ | Emitter to base voltage (dc) |
| $V_{eb}$ | Emitter to base voltage (rms) |
| $v_{eb}$ | Emitter to base voltage (instantaneous) |
| $V_{EBF}$ | DC open circuit voltage (floating potential) between the emitter and base, with the collector biased in the reverse direction with respect to the base |

| | |
|---|---|
| $V_{(BR)CEV}$ | Breakdown voltage collector to emitter, with specified voltage between base and emitter |
| $V_{EBO}$ | Emitter to base voltage (static) collector open |
| $V_{EC}$ | Emitter to collector voltage (dc) |
| $V_{ECF}$ | DC open circuit voltage (floating potential) between the emitter and collector, with the base biased in the reverse direction with respect to the collector |
| $V_{EE}$ | Emitter supply voltage |
| $V_{RT}$ | Reach through voltage |

40.2 FETs.

| | |
|---|---|
| $b_{is}$ | Small-signal, common-source, short-circuit, input susceptance |
| $b_{os}$ | Small-signal, common-source, short-circuit, output susceptance |
| $b_{fs}$ | Small-signal, common-source, short-circuit, forward transfer susceptance |
| $b_{rs}$ | Small-signal, common-source, short-circuit, reverse transfer susceptance |
| $C_{ds}$ | Small-signal drain to source capacitance |
| $C_{du}$ | Small-signal drain to substrate capacitance |
| $C_{iss}$ | Small-signal, common-source, short-circuit, input capacitance |
| $C_{oss}$ | Small-signal, common-source, short-circuit, output capacitance |
| $C_{rss}$ | Small-signal, common-source, short-circuit, reverse transfer capacitance |
| D, d | Drain terminal |
| $E_{AR}$ | Repetitive avalanche energy capability |
| $E_{AS}$ | Single pulse avalanche energy capability |
| G, g | Gate terminal |
| $g_{fs}$ | Small-signal, common-source, short-circuit, forward transfer conductance |
| $g_{is}$ | Small-signal, common-source, short-circuit, input conductance |
| $g_{os}$ | Small-signal, common-source, short-circuit, output conductance |
| $G_{pg}$ | Small-signal, common-gate insertion power gain |
| $G_{ps}$ | Small-signal, common-source insertion power gain |
| $g_{rs}$ | Small-signal, common-source, short-circuit, reverse transfer conductance |

| | |
|---|---|
| $G_{tg}$ | Small-signal, common-gate, transducer power gain |
| $G_{ts}$ | Small-signal, common-source transducer power gain |
| $I_D$ | Drain current |
| $I_{AR}$ | Rated avalanche current (repetitive and nonrepetitive) |
| $I_{D(on)}$ | On-state drain current |
| $I_{D(off)}$ | Drain cutoff current |
| $I_{DSS}$ | Zero-gate-voltage drain current |
| $I_G$ | Gate current |
| $I_{GF}$ | Forward gate current |
| $I_{GR}$ | Reverse gate current |
| $I_{GSS}$ | Reverse gate current with all other terminals short-circuited to source (junction-gate) |
| $I_{GSSF}$ | Forward gate current with all other terminals short-circuited to source (insulated-gate) |
| $I_{GSSR}$ | Reverse gate current with all other terminals short-circuited to source (insulated-gate) |
| $I_S$ | Source current through drain diode (forward biased $V_{SD}$) |
| $I_{S(off)}$ | Source cutoff current |
| $I_{SDS}$ | Zero-gate-voltage source current |
| $I_{(ISO)}$ | Source pin to case isolation current |
| $Q_g(th)$ | Gate charge that must be supplied to reach minimum specified gate-source threshold voltage |
| $Q_{g(on)}$ | Gate charge that must be supplied to reach the gate-source voltage specified for the device $r_{DS(on)}$ measurement |
| $Q_{gm(on)}$ | Gate charge that must be supplied to the device to reach the maximum rated gate-source voltage |
| $Q_{gs}$ | Charge required by $C_{GS}$ to reach a specified $I_D$ |
| $Q_{gd}$ | Charge supplied to the drain from the gate to change the drain voltage under constant drain current conditions |
| $r_{ds(on)}$ | Small-signal, drain to source on-state resistance |
| $r_{DS(on)}$ | Static drain to source on-state resistance |
| S, s | Source terminal |
| $t_{d(off)}$ | Turn-off delay time |
| $t_{d(on)}$ | Turn-on delay time |

| | |
|---|---|
| U, u | Substrate (bulk) (terminal, when substrate is externally terminated) |
| $V_{(BR)GSS}$ | Gate to source breakdown voltage, all other terminals short-circuited to source (junction-gate) |
| $V_{(BR)DSS}$ | Drain to source breakdown voltage, all other terminals short-circuited to source (junction-gate) |
| $V_{(BR)GSSF}$ | Forward gate to source breakdown voltage |
| $V_{(BR)GSSR}$ | Reverse gate to source breakdown voltage |
| $V_{DD}$ | Drain supply voltage |
| $V_{DG}$ | Drain to gate voltage |
| $V_{DS}$ | Drain to source voltage |
| $V_{DS(on)}$ | On-state drain to source voltage |
| $V_{DU}$ | Drain to substrate voltage |
| $V_{GG}$ | Gate supply voltage |
| $V_{GP}$ | Gate plateau voltage |
| $V_{GS}$ | Gate to source voltage |
| $V_{GSF}$ | Forward gate to source voltage |
| $V_{GSR}$ | Reverse gate to source voltage |
| $V_{GS(off)}$ | Gate to source cutoff voltage |
| $V_{GS(th)}$ | Gate to source threshold voltage |
| $V_{GU}$ | Gate to substrate voltage |
| $V_{ISO}$ | Source pin to case isolation voltage |
| $V_{SS}$ | Source supply voltage |
| $V_{SU}$ | Source to substrate voltage |
| $y_{fs}$ | Magnitude of small-signal common-source short-circuit forward transfer admittance |
| $y_{is}$ | Magnitude of small-signal common-source short-circuit input admittance |
| $y_{rs}$ | Magnitude of small-signal common-source short-circuit reverse transfer admittance |

40.3 Unijunction transistors.

| | |
|---|---|
| $I_{B2(mod)}$ | Interbase modulated current |
| $I_{EB2O}$ | Emitter reverse current |
| $I_P$ | Peak point current |
| $I_V$ | Valley point current |

| | |
|---|---|
| $r_{BB}$ | Interbase resistance |
| $V_{B2B1}$ | Interbase voltage |
| $V_{EB1(sat)}$ | Emitter saturation voltage |
| $V_{OB1}$ | Base - 1 peak voltage |
| $V_p$ | Peak point voltage |
| $V_v$ | Valley point voltage |
| $\eta$ | Intrinsic standoff ratio |

50. DIODES AND RECTIFIERS

50.1 Diodes and rectifiers.

| | |
|---|---|
| $C_J$ | Junction capacitance |
| $I_{F(RMS)}$, $I_f$, $I_F$, $I_{F(AV)}$, $i_F$, $I_{FM}$ | Forward current |
| $I_{FSM}$ | Forward current, surge peak |
| $I_{F(OV)}$ | Forward current, overload |
| $I_O$ | Average forward current, 180° conduction angle, 60 Hz, half sine wave |
| $I_{R(RMS)}$, $I_r$, $I_R$, $I_{R(AV)}$, $i_R$, $I_{RM}$ | Reverse current |
| $i_{R(REC)}$, $I_{RM(REC)}$ | Reverse recovery current |
| $I_{RRM}$ | Reverse current, repetitive peak |
| $I_{RSM}$ | Reverse current, surge peak |
| $P_F$, $P_{F(AV)}$, $P_F$, $P_{FM}$ | Forward power dissipation |
| $P_R$, $P_{R(AV)}$, $P_R$, $P_{RM}$ | Reverse power dissipation |
| $Q_S$ | Stored charge |
| $t_{fr}$ | Forward recovery time |
| $t_{rr}$ | Reverse recovery time |
| $V_{(BR)}$, $v_{(BR)}$ | Breakdown voltage (dc, instantaneous total value) |
| $V_{F(RMS)}$, $V_f$, $V_F$, $V_{F(AV)}$, $v_F$, $V_{FM}$ | Forward voltage |
| $V_{R(RMS)}$, $V_r$, $V_R$, $V_{r(AV)}$, $v_R$, $V_{RM}$ | Reverse voltage |
| $V_{RWM}$ | Working peak reverse voltage |
| $V_{RRM}$ | Repetitive peak reverse voltage |
| $V_{RSM}$ | Nonrepetitive peak reverse voltage |

APPENDIX B

50.1.1 Letter symbol table (diodes and rectifiers).

| | Total RMS value | RMS value of alternating component | DC value no alternating component | DC value with alternating component | Instantaneous total value | Maximum (peak) total value |
|---|---|---|---|---|---|---|
| Forward current | $I_{F(RMS)}$ | $I_f$ | $I_F$ | $I_{F(AV)}$ | $i_F$ | $I_{FM}$ |
| Forward current, average, 180° conduction angle 60 Hz, half sine wave | | | | $I_O$ | | |
| Forward current, repetitive peak | | | | | | $I_{FRM}$ |
| Forward current, surge peak | | | | | | $I_{FSM}$ |
| Forward current, overload | | | | | | $I_{F(OV)}$ |
| Reverse current | $I_{R(RMS)}$ | $I_f$ | $I_R$ | $I_{R(AV)}$ | $i_R$ | $I_{RM}$ |
| Reverse recovery current | | | | | $i_{R(REC)}$ | $I_{RM(REC)}$ |
| Forward power dissipation | | | $P_F$ | $P_{F(AV)}$ | $P_F$ | $P_{FM}$ |
| Reverse power dissipation | | | $P_R$ | $P_{R(AV)}$ | $P_R$ | $P_{RM}$ |
| Forward voltage | $V_{F(RMS)}$ | $V_f$ | $V_F$ | $V_{F(AV)}$ | $V_F$ | $V_{FM}$ |
| Reverse voltage | $V_{R(RMS)}$ | $V_r$ | $V_R$ | $V_{R(AV)}$ | $V_R$ | $R_{RM}$ |
| Reverse voltage working peak | | | | | | $V_{RWM}$ |
| Reverse voltage repetitive peak | | | | | | $V_{RRM}$ |
| Reverse voltage nonrepetitive peak | | | | | | $V_{RRM}$ |
| Breakdown voltage | | | $V_{(BR)}$ | | $V_{(BR)}$ | |

50.2 Microwave diodes.

| | |
|---|---|
| $F_o$ | Overall average noise figure (of a mixer diode) |
| $F_{os}$ | Standard overall average noise figure (of a mixer diode) |
| $L_c$ | Conversion loss |
| M | *Figure of merit (of a detector diode)* |
| $N_r$ | Output noise ratio |
| TSS | Tangential signal sensitivity |
| VSWR | Voltage standing wave ratio |
| $z_{if}$ | Impedance, intermediate-frequency |
| $z_{rf}$ | Impedance, radio-frequency |
| $z_m$ | *Impedance, modulator-frequency load* |
| $z_v$ | Video impedance |

50.3 Tunnel diodes and backward diodes.

| | |
|---|---|
| $I_I$ | Inflection point current |
| $I_P$ | Peak point current |
| $I_V$ | Valley point current |
| $r_i$ | Dynamic resistance at inflection point |
| $V_{PP}$ | *Projected peak point voltage* |
| $V_I$ | Inflection point voltage |
| $V_P$ | Peak point voltage |
| $V_V$ | Valley point voltage |

50.4 Voltage regulator and voltage reference diodes.

| | |
|---|---|
| $I_F$ | Forward current, dc |
| $I_R$ | *Reverse current, dc* |
| $I_Z$, $I_{ZK}$, $I_{ZM}$, $I_{ZSM}$ | Regulator current, reference current (dc, dc near breakdown knee, dc maximum rated current, dc maximum rated surge current) |
| $V_F$ | *Forward voltage, dc* |
| $V_R$ | Reverse voltage, dc |
| $V_Z$, $V_{ZM}$ | Regulator voltage, reference voltage (dc, dc at maximum rated current) |
| $z_z$, $z_{zk}$, $z_{zm}$ | *Regulator impedance, reference impedance (small-signal, at $I_Z$, at $I_{ZK}$, at $I_{ZM}$)* |
| $\alpha_{VZ}$ | Temperature coefficient of regulator voltage, temperature coefficient of reference voltage |

50.5 Current regulator diodes.

| | |
|---|---|
| $I_L$ | Limiting current |
| $I_S$ | Regulator current |
| $V_K$ | Knee voltage |
| $V_L$ | Limiting voltage |
| $\Delta I_S$ | Regulator current variation |
| $V_S$ | Regulator voltage |
| $z_k$ | Knee impedance |
| $z_s$ | Regulator impedance |
| $\alpha_{IS}$ | Temperature coefficient of regulator current |

50.6 Varactor diodes.

| | |
|---|---|
| $C_c$ | Case capacitance |
| $C_j$ | Junction capacitance |
| $C_t$ | Total capacitance |
| $\frac{C_{t1}}{C_{t2}}$ | Capacitance ratio |
| $f_{co}$ | Cut-off frequency |
| $L_s$ | Series inductance |
| Q | Figure of merit |
| $r_s$ | Series resistance, small-signal |
| $\alpha_C$ | Temperature coefficient of capacitance |
| $\eta$ | Efficiency |

50.7 Transient voltage suppressors.

| | |
|---|---|
| CF | Clamping factor |
| $I_D$ | Standby current |
| $I_{FS}$ | Forward surge current |
| $I_{FSM}$ | Rated forward surge current |
| $I_{PP}$ | Peak impulse current |
| $I_{PPM}$ | Rated peak impulse current |
| $I_S$ | Surge peak transient current |
| $I_{SM}$ | Rated surge peak transient current |

| | |
|---|---|
| $P_{(AV)}$ | Average power dissipation |
| $P_{M(AV)}$ | Rated average power dissipation |
| $P_{PP}$ | Repetitive peak pulse power dissipation |
| $P_{PPM}$ | Rated repetitive peak pulse power dissipation |
| $t_{os}$ | Overshoot duration |
| $t_{res}$ | Response time |
| $V_{(BR)}$ | Breakdown voltage |
| $V_C$ | Clamping voltage |
| $V_W$ | Working peak voltage, also standoff voltage |
| $V_{WM(RMS)}$ | Working rms voltage |
| $V_{WM}$ | Rated working peak voltage |
| $V_{CS}$ | Voltage overshoot |
| $\alpha V_{(BR)}$ | Temperature coefficient of breakdown voltage |

60. THYRISTORS

| | |
|---|---|
| dv/dt | Critical rate of rise of off-state voltage |
| $I_{(BO)}$, $i_{(BO)}$ | Breakover current |
| $I_{(BR)}$, $i_{(BR)}$ | Reverse breakdown current (of a reverse-blocking thyristor) |
| $I_{D(RMS)}$, $I_D$, $I_{D(AV)}$, $i_D$, $I_{DM}$ | Off-state current |
| $I_{DRM}$ | Repetitive peak off-state current |
| $I_G$, $I_{G(AV)}$, $i_G$, $I_{GM}$ | Gate current |
| $I_{GD}$, $i_{GD}$, $I_{GDM}$ | Gate nontrigger current |
| $I_{GQ}$, $i_{GQ}$, $I_{GQM}$ | Gate turn-off current (of a turn-off thyristor) |
| $I_{GT}$, $i_{GT}$, $I_{GTM}$ | Gate trigger current |
| $I_H$, $i_H$ | Holding current |
| $I_L$, $i_L$ | Latching current |
| $I_{R(RSM)}$, $I_R$, $I_{R(AV)}$, $i_R$, $I_{RM}$ | Reverse current (of a reverse-blocking or reverse-conducting thyristor) |
| $I_{RRM}$ | Repetitive peak reverse current (of a reverse-blocking thyristor) |
| $I_{RSM}$ | Nonrepetitive peak reverse current (of a reverse-blocking thyristor) |
| $I_{T(RMS)}$, $I_T$, $I_{T(AV)}$, $i_T$, $I_{TM}$ | On-state current |
| $I_{TRM}$ | Repetitive peak on-state current |

| | |
|---|---|
| $I_{TSM}$ | Nonrepetitive peak on-state current |
| $P_G$, $P_{G(AV)}$, $P_G$, $P_{GM}$ | Gate power dissipation |
| $P_R$, $P_{R(AV)}$, $P_R$, $P_{RM}$ | Reverse power dissipation |
| $t_{gd}$ | Gate-controlled delay time |
| $t_{gq}$ | Gate-controlled turn-off time (of a turn-off thyristor) |
| $t_{gt}$ | Gate-controlled turn-on time |
| $t_q$ | Circuit-commutated turn-off time |
| $V_{(BO)}$, $v_{(BO)}$ | Breakover voltage |
| $V_{(BR)}$, $v_{(BR)}$ | Reverse breakdown voltage (of a reverse-blocking thyristor) |
| $V_{D(RMS)}$, $V_D$, $V_{D(AV)}$, $v_D$, $V_{DM}$ | Off-state voltage |
| $V_{DRM}$ | Repetitive peak off-state voltage |
| $V_{DSM}$ | Nonrepetitive peak off-state voltage |
| $V_{DWM}$ | Working peak off-state voltage |
| $V_G$, $V_{G(AV)}$, $v_G$, $V_{GM}$ | Gate voltage |
| $V_{GD}$, $v_{GD}$, $V_{GDM}$ | Gate nontrigger voltage |
| $V_{GQ}$, $v_{GQ}$, $V_{GQM}$ | Gate turn-off voltage (of a turn-off thyristor) |
| $V_{GT}$, $v_{GT}$, $V_{GTM}$ | Gate trigger voltage (of a reverse-blocking thyristor |
| $V_{RRM}$ | Repetitive peak reverse voltage (of a reverse-blocking thyristor) |
| $V_{RSM}$ | Nonrepetitive peak reverse voltage (of a reverse-blocking thyristor) |
| $V_{RWM}$ | Working peak reverse voltage (of a reverse-blocking thyristor) |
| $V_{T(RMS)}$, $V_T$, $V_{T(AV)}$, $v_T$, $V_{TM}$ | On-state voltage |
| $V_{T(MIN)}$ | Minimum on-state voltage |

60.1.1 Letter symbol table (thyristors).

| | Total RMS value | DC value no alternating component | DC value with alternating component | Instantaneous total value | Maximum (peak) total value |
|---|---|---|---|---|---|
| On state current | $I_{T(RMS)}$ | $I_T$ | $I_{T(AV)}$ | $i_T$ | $I_{TM}$ |
| Repetitive peak, on-state current | | | | | $I_{TRM}$ |
| Surge (nonrepetitive) on-state current | | | | | $I_{TSM}$ |
| Overload on-state current | | | | | $I_{T(OV)}$ |
| Breakover current | | $I_{(BO)}$ | | $i_{(BO)}$ | |
| Off-state current | $I_{D(RMS)}$ | $I_D$ | $I_{D(AV)}$ | $i_D$ | $I_{DM}$ |
| Repetitive peak, off-state current | | | | | $I_{DRM}$ |
| Reverse current | $I_{R(RMS)}$ | $I_R$ | $I_{R(AV)}$ | $i_R$ | $I_{RM}$ |
| Repetitive peak, reverse current | | | | | $I_{RRM}$ |
| Reverse breakdown current | | $I_{(BR)R}$ | | $i_{(BR)R}$ | |
| On-state voltage | $V_{T(RMS)}$ | $V_T$ | $V_{T(AV)}$ | $v_T$ | $V_{TM}$ |
| Breakover voltage | | $V_{(BO)}$ | | $v_{(BO)}$ | |
| Off-state voltage | $V_{D(RMS)}$ | $V_D$ | $V_{D(AV)}$ | $v_D$ | $V_{DM}$ |
| Minimum on-state voltage | | $V_{T(MIN)}$ | | | |
| Working peak, off-state voltage | | | | | $V_{DWM}$ |
| Repetitive peak, off-state voltage | | | | | $V_{DRM}$ |

60.1.1 Letter symbol table (thyristors) - Continued.

| | Total RMS value | DC value no alternating component | DC value with alternating component | Instantaneous total value | Maximum (peak) total value |
|---|---|---|---|---|---|
| Nonrepetitive, off-state voltage | | | | | $V_{DSM}$ |
| Reverse voltage | $V_{R(RMS)}$ | $V_R$ | $V_{R(AV)}$ | $v_R$ | $V_{RM}$ |
| Working peak, reverse voltage | | | | | $V_{RWM}$ |
| Repetitive peak, reverse voltage | | | | | $V_{RRM}$ |
| Nonrepetitive peak, reverse voltage | | | | | $V_{RSM}$ |
| Reverse breakdown voltage | | $V_{(BR)R}$ | | $v_{(BR)R}$ | |
| Holding current | | $I_H$ | | $i_H$ | |
| Latching current | | $I_L$ | | $i_L$ | |
| Gate current | | $I_G$ | $I_{G(AV)}$ | $i_G$ | $I_{GM}$ |
| Gate trigger current | | $I_{GT}$ | | $i_{GT}$ | $I_{GTM}$ |
| Gate nontrigger current | | $I_{GD}$ | | $i_{GD}$ | $I_{GDM}$ |
| Gate turn-off current | | $I_{GQ}$ | | $i_{GQ}$ | $I_{GQM}$ |
| Gate voltage | | $V_G$ | $V_{G(AV)}$ | $v_G$ | $V_{GM}$ |
| Gate trigger voltage | | $V_{GT}$ | | $v_{GT}$ | $V_{GTM}$ |
| Gate nontrigger current | | $V_{GD}$ | | $v_{GD}$ | $V_{GDM}$ |
| Gate turn-off voltage | | $V_{GQ}$ | | $v_{GQ}$ | $V_{GQM}$ |
| Gate power dissipation | | $P_G$ | $P_{G(AV)}$ | $p_G$ | $P_{GM}$ |

## 70. OPTOELECTRONIC DEVICES

| | |
|---|---|
| $Q$, ($Q_e$) | *Radiant energy* |
| $Q$, ($Q_v$) | Luminous energy |
| $t_d$ | Delay time |
| $t_f$ | Fall time |
| $t_{off}$ | Turn-off time |
| $t_{on}$ | Turn-on time |
| $t_r$ | Rise time |
| $t_s$ | Storage time |
| $\tau$ | Time constant |
| $\phi$ | Luminous flux, radiant flux |

### 70.1 Photosensitive devices.

| | |
|---|---|
| $A_D$ | *Area, detector* |
| $E$ | Illuminance (illumination); irradiance |
| $f_{mod}$ | Modulation frequency |
| $I_n$ | Detector noise |
| $I_S$, $I_s$ | Detector signal current (dc; rms value of ac component) |
| $P_n$ | Noise equivalent power |
| $V_n$ | Detector noise voltage |
| $V_S$, $V_s$ | Detector signal voltage (dc; rms value of ac component) |
| $\mu f$ | Noise equivalent bandwidth |

### 70.2 Photoemitting devices.

| | |
|---|---|
| $I$ | Luminous intensity; radiant intensity |
| $L$ | *Luminance; radiance* |
| $t_f$ | Radiant-pulse fall time |
| $t_r$ | Radiant-pulse rise time |
| $w$ | Luminous density; radiant density |
| $\Delta\lambda$ | Spectral bandwidth |
| $\lambda_p$ | Peak wavelength |

70.3 Optocouplers (photocouplers, opto-isolators).

| | |
|---|---|
| $C_{io}$ | Input-to-output internal capacitance; transcapacitance |
| $h_F$ | Current transfer ratio |
| $I_{IO}$ | DC input-to-output current; isolation current |
| $r_{IO}$ | Isolation resistance |
| $V_{IO}$ | DC input-to-output voltage; isolation voltage |

APPENDIX C

STATISTICAL SAMPLING AND LIFE TEST PROCEDURES

10. SCOPE

10.1 Scope. This appendix contains statistical sampling and life test procedures used with semiconductor devices. This appendix is a mandatory part of the specification. The information contained herein is intended for compliance.

20. APPLICABLE DOCUMENTS

20.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DODISS) and supplement thereto, cited in the solicitation (see 6.1).

HANDBOOK

MILITARY

MIL-HDBK-H53-1 - Guide for Attribute Lot Sampling Inspection and MIL-STD-105.

(Unless otherwise indicated, copies of federal and military specifications, standards, and handbooks are available from the Defense Printing Service Detachment Office, Bldg. 4D (Customer Service), 700 Robbins Avenue, Philadelphia, PA 19111-5094.)

20.2 Order of precedence. In the event of a conflict between the text of this document and the references cited herein (except for related associated detail specifications, specification sheets, or MS standards), the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

30. GENERAL

30.1 Definitions. The following definitions shall apply for all statistical sampling procedures:

a. Sample plan series. The sample plan series is defined as the following decreasing series of sample plan values: 50, 30, 20, 15, 10, 7, 5, 3, 2, 1.5, 1, 0.7, 0.5, 0.3, 0.2, 0.15, and 0.1.

b. Tightened inspection. Tightened inspection is defined as inspection performed using the next sample plan value in the sample plan series lower than that specified.

c. Acceptance number (c). The acceptance number is defined as an integral number associated with the selected sample size which determines the maximum number of defectives permitted for that sample size.

d. Rejection number (r). Rejection number is defined as one plus the acceptance number.

30.2 Symbols. The following symbols shall apply for all statistical sampling procedures:

a. c - Acceptance number

b. r - Rejection number

c. n - Sample size

40. STATISTICAL SAMPLING PROCEDURES AND TABLE

40.1 General. Statistical sampling shall be conducted using the sample plan method herein. The sample plan method as specified herein is a double sample plan which provides a high degree of assurance that a lot having a proportion defective equal to or greater than the specified sample plan value will not be accepted. The choice of any one procedure is optional. The procedures specified herein are suitable for all qualification or quality conformance requirements, but are not suitable if the objective of the inspection is to determine that the proportion defective in the lot represented is greater than the specified sample plan value since the assurance for that purpose is normally only 10 percent (see 6.4).

40.1.1 Selection of samples. Samples shall be randomly selected from the inspection lot or inspection sublots (For an explanation of random sampling, see MIL-HDBK-53-1, section 13).

40.1.1.1 Identification of samples for quality conformance tests. The authorized Government quality assurance representative may, at his option, mark or authorize the marking of each sample to be subjected to qualification or QCI in order to distinguish these units from those not intended for Government conformance inspection (see 3.7.3).

40.1.1.2 Small lots. Small lots shall not exceed 500 pieces.

40.1.2 Failures. Failure of a unit for one or more tests of a subgroup shall be charged as a single failure.

40.2 Single-lot sampling method. QCI information (sample sizes and number of observed defectives) shall be accumulated from a single inspection lot to demonstrate conformance to the individual subgroup criteria.

40.2.1 Sample size. The sample size for each subgroup shall be determined from table IX and shall meet the specified sample plan. The manufacturer may, at his option, select a sample size greater than that required; however, the number of failures permitted shall not exceed the acceptance number associated with the required sample size in table IX.

40.2.2 Acceptance procedure. For the first sampling, an acceptance number shall be chosen and the associated number of sampling devices for the specified sample plan selected and tested (see 40.2.1). If the observed number of defectives from the first sample is less than or equal to the preselected acceptance number, the lot shall be accepted. If the observed number of defectives exceeds the preselected acceptance number, an additional sample may be chosen such that the total sample complies with 40.2.3.

40.2.3 Additional sample. The manufacturer may add an additional quantity to the initial sample, but this may be done only once for any subgroup and the added samples shall be subjected to all the tests within the subgroup. The total sample size (initial and added samples) shall be determined by a new acceptance number selected from table IX.

40.2.4 Multiple criteria. Except where otherwise specified, when a subgroup contains more than one acceptance criterion, the entire sample for a subgroup shall be used for all criteria within the subgroup. In table IX, the acceptance number shall be that one associated with the largest sample size in the appropriate sample plan column which is less than or equal to the sample size used.

40.2.5 One-hundred percent inspection. Inspection of 100 percent of the lot shall be allowed, at the option of the manufacturer for any or all subgroups other than those which are considered "destructive." The maximum observed percent defective for the inspection lot shall not exceed the specified sample plan value. Devices that fail any test shall be removed from the lot.

40.2.6 Disposition of failed lot. A lot that fails QCI may, at the option of the manufacturer, be screened for defectives or reworked and resubmitted for reinspection (see 4.3.4).

50. LIFE TEST

50.1 General. Life tests shall be conducted in accordance with the procedures in this section. Life tests performed on devices at or within their maximum ratings shall be considered nondestructive. If a lot is made up of a collection of sublots, each sublot shall pass all applicable electrical end-points as specified.

50.2 Selection of samples. Samples for life tests shall be selected at random from the inspection lot (see 40.1.1). The sample size for a 1,000-hour test shall be chosen by the manufacturer from table IX from the column under the specified $\lambda$. The acceptance number shall be the one associated with the particular sample size chosen.

APPENDIX C

50.3 Failures. A semiconductor device which exceeds one or more of the end-point limits specified for life test at any specified or other reading interval shall be considered a failure and shall not be considered acceptable at any subsequent reading interval. For the purpose of computing device hours, the test-time hours credited to a failed device shall not exceed the test time associated with the last measurement time that the device was observed to be within the specified end-point limits. If the sample size fails, the test may be terminated at the discretion of the manufacturer.

50.4 Life-test time and sample size. When a lambda ($\lambda$) is specified, the life-test time shall be 1,000 hours initially. Once a lot has passed the 1,000-hour tests, life tests with minimums of 340 hours and maximums of 2,000 hours may be initiated for new lots provided that 180 days have not elapsed since a 1,000-hour life tests on the same device type on the same structurally identical group (see 4.7.6). If 180 days have elapsed, the new lot shall pass a 1,000-hour life test. The sample size for a life-test time other than 1,000 hours shall be chosen according to the relationship of inverse proportionality between test time and sample size, such that the total unit test hours accumulated (sample sizes multiplied by test hours) equal the amount that would have been chosen for the 1,000-hour life test, had it been performed. The acceptance number shall also be determined from the sample size associated with the same 1,000-hour test, had it been performed. The lot shall be accepted if the number of failures at the end of the test period does not exceed the acceptance number.

50.5 Procedure to be used if number of observed failures exceeds the acceptance number. In the event that the number of failures observed on life test exceeds the acceptance number, the manufacturer shall choose one of the following options: (1) discontinue the life test, screen or rework, and resubmit in accordance with 40.2.6, (2) add additional samples in accordance with 50.5.1, or (3) extend the test time to 1,000 hour in accordance with 50.5.2, if a test time less than 1,000 hours was originally chosen. Only one of these options shall be used for a given submission, and this option shall be used only once.

50.5.1 Additional samples. When this option is chosen, a new total sample size (initial plus added) shall be chosen by the manufacturer from table IX from the column under the specified $\lambda$. A quantity of additional units sufficient to increase the sample to the newly chosen total sample size shall be selected from the lot. A new acceptance number shall be determined and shall be the one associated with the new total sample size chosen. The added sample shall be subjected to the same life-test conditions and time period as the initial sample. If the total observed number of defectives (initial plus added) does not exceed the acceptance number for the total sample, the lot shall be accepted. If the observed number of defectives exceeds this acceptance number, the lot shall not be accepted but may be resubmitted (see 40.2.6).

50.5.2 Extension of life-test period. If a life-test time period less than 1,000 hours is being used and the number of failures observed in the initial sample exceeds the acceptance number, the manufacturer may in lieu of adding additional samples, choose to extend the test time of the entire initial sample to 1,000 hours and determine a new acceptance number from table IX. The new acceptance number shall be that one associated with the largest sample size in the specified column which is less than or equal to the sample size on test. A device which is a failure at the initial reading interval shall not be considered acceptable at the 1,000-hour reading interval. If the observed number of defectives at 1,000 hours does not exceed the new acceptance number, the lot shall be accepted. If the observed number of defectives exceeds this acceptance number, the lot shall not be accepted, but may be resubmitted (see 40.2.6).

50.5.3 Failure of life test. If a lot fails to meet life-test requirements (including submission in accordance with 40.2.6, if elected) such that it is eliminated or withdrawn from further quality conformance inspection consideration, then a 1,000-hour life test shall be required for the failed subgroup until three successive lots have passed. If group B or C (table IV or V) does not require 1,000-hour testing, then the specified life test, if other than 1,000 hours, shall be required for three successive lots.

TABLE IX. Sample plans. 1/ 2/
Minimum size of sample to be tested to assure, with a 90 percent confidence, that a lot having percent-defective equal to the specified sample plan will not be accepted (single sample).

| Maximum percent defective or A | 50 | 30 | 20 | 15 | 10 | 7 | 5 | 3 | 2 | 1.5 | 1 | 0.7 | 0.5 | 0.3 | 0.2 | 0.15 | 0.1 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Acceptance number (c) (r = c + 1) | Minimum sample sizes (For device-hours required for life test, multiply by 1,000) | | | | | | | | | | | | | | | | |
| 0 | 5 (1.03) | 8 (0.64) | 11 (0.46) | 15 (0.34) | 22 (0.23) | 32 (0.16) | 45 (0.11) | 76 (0.07) | 116 (0.04) | 153 (0.03) | 231 (0.02) | 328 (0.02) | 461 (0.01) | 767 (0.007) | 1152 (0.005) | 1534 (0.003) | 2303 (0.002) |
| 1 | 8 (4.4) | 13 (2.7) | 18 (2.0) | 25 (1.4) | 38 (0.94) | 55 (0.65) | 77 (0.46) | 129 (0.28) | 195 (0.18) | 258 (0.14) | 390 (0.09) | 555 (0.06) | 778 (0.045) | 1296 (0.027) | 1946 (0.018) | 2592 (0.013) | 3891 (0.009) |

1/ Sample sizes are based upon the Poisson exponential binomial limit.
2/ The minimum quality (approximate AQL required to accept on the average) 19 of 20 lots is shown in parentheses for information only.

APPENDIX D

PRODUCT ASSURANCE PROGRAM AND MANUFACTURING
CERTIFICATION REQUIREMENTS

10. SCOPE

10.1 Scope. This appendix contains details of the product assurance program requirements and manufacturing certification requirements for JAN, JANTX, JANTXV, and JANS for semiconductor devices. This appendix is a mandatory part of the specification. The information contained herein is intended for compliance.

20. APPLICABLE DOCUMENTS. This section is not applicable to this appendix.

30. PRODUCT ASSURANCE PROGRAM

* 30.1 Product assurance program general requirements. The product assurance program shall assure that the design, processing, assembly, inspection, and testing of semiconductor devices comply with this specification and the applicable detail specification. It shall be the responsibility of the manufacturer to maintain the documentation and control the product assurance program as described herein. The program documentation shall be under documentation systems with revision letters, release dates, and approval signature, and shall include, as a minimum, the manufacturer's flow charts and those documents required in 30.1.1. Personnel performing quality functions shall have sufficient well-defined responsibility, authority, and the organizational freedom to identify and evaluate quality problems and to initiate, recommend, or provide solutions. The test programs and setups used to sort, classify, and test for MIL-S-19500 requirements are required to be traceable through each companies document control system to insure the correct revision was used when testing MIL-S-19500 devices. Devices or lots which fail any specification or internal tests procedures and requirements above and beyond the specification, except electrical selections, are not suitable for any JAN level. Lots failing electrical selections for any JAN level which 1) are above and beyond the military specification, and 2) are intended to select a portion of a lot having greater reliability than the overall average reliability of the lot other than through statistical methods are not suitable for any JAN level.

30.1.1 Design, processing, manufacturing, and testing documentation. The manufacturer shall utilize documented instructions (e.g., internal specifications, traceability documents, or lot traveler detailing the manufacturer's minimum requirements) covering as a minimum these areas:

a. Personnel training (see 30.1.1.1).

b. Inspection of incoming materials, utilities, and work in process (see 30.1.1.2).

c. Quality operations (see 30.1.1.3).

d. Design, processing, manufacturing, equipment, and materials documentation (see 30.1.1.4).

e. Design, material, and process change control (see 30.1.1.5).

f. Test equipment maintenance and calibration procedures (see 30.1.1.6).

g. Failure and defect analysis and data feedback (see 30.1.1.7).

h. Corrective action and evaluation (see 30.1.1.8).

i. Incoming, in-process, and outgoing inventory control (see 30.1.1.9).

j. Product lot identification (see 30.1.1.10).

k. ESD handling control program (see 30.1.1.11).

l. Conversion of military specification requirements and methods into manufacturer's internal instructions (see 30.1.1.12).

30.1.1.1 Personnel training. Work training practices shall be established and utilized in acquiring and maintaining job skills as required in critical work areas. As a minimum the critical work area shall include a through o of 30.1.1.4.

30.1.1.2 Inspection of incoming materials and utilities, and work-in process. Inspection operations shall be documented as to type of inspection, sampling and test procedures, acceptance-rejection criteria, and frequency of use. Records of inspection operations shall cover the tests or inspections made, the materials group (lot, batch, etc.) inspected, the controlling documentation, the date of completion of inspection, the amount of material tested, and acceptance, rejection or other final disposition of the material. Devices which fail any specification or internal tests procedures and requirements above and beyond the specification are not suitable (except electrical selections) for any JAN level. Lots failing electrical selections for any JAN level which 1) are above and beyond the military specification and 2) are intended to select a portion of a lot having greater reliability than the overall average reliability of the lot are not suitable for any JAN level.

30.1.1.3 Quality operations. Quality operations shall be documented as to type, procedures, rating criteria, action criteria (including disposition of product processed during periods of out-of-control conditions), equipment, records, and frequency of use.

30.1.1.4 Design, processing, manufacturing, equipment, and materials documentation. Device design, processing, manufacturing equipment and materials shall be documented in drawings, standards, specifications, or other appropriate media which shall cover the requirements and tolerances for all aspects of design and manufacture including equipment test and prove-in, materials acquisition and handling, design-verification testing and processing steps. As a minimum requirement, documentation shall exist for the following items:

a. Incoming materials control (wafers, packages, wire, water purification, etc.).

b. Materials preparation (lapping, polishing, etching, cleaning, etc.).

c. Masking, photoresist, and mask registration.

d. Epitaxy, diffusion and ion implantation.

e. Oxidation or passivation.

f. Metallization and film deposition.

g. Junction etch, silicon reflow.

h. Die attachment.

i. Bonding.

j. Rework.

k. Sealing.

l. Cleanliness and atmosphere control in critical work areas (see 40.1.10).

m. Screening operations.

n. QCI testing.

o. Design and construction.

30.1.1.5 Design, material, and process change control. The methods and procedures for implementation and control of changes in device design, material and processing, shall be documented and maintained. Records shall be maintained for 5 years minimum covering the initial documentation and all changes with the date each change in design, materials, or processing becomes effective.

30.1.1.6 Test equipment maintenance and calibration procedures. Maintenance and calibration procedures and the frequency of scheduled actions, for gauges and test equipment, shall be documented and in accordance with the requirements of MIL-STD-45662. Equipment maintenance and calibration records shall be maintained.

30.1.1.7 Failure and defect analysis and feedback. The procedures for identification, handling, and analysis of failed or defective devices and for dissemination of analysis data shall be documented.

30.1.1.8 Corrective action and evaluation. The procedures and responsibility for decisions regarding the necessity for corrective action as a result of failure or defect analysis, and for evaluation and approval of proposed corrective actions shall be documented.

30.1.1.9 Incoming, in-process, and outgoing inventory control. The methods and procedures which are used to control storage and handling of incoming materials, work in-process, and warehoused and outgoing product in order to (a) achieve such factors as age control of limited-life materials; and (b) prevent inadvertent mixing of conforming and nonconforming materials, work, finished product, resubmitted lots, or customer returns shall be documented.

30.1.1.10 Product lot identification. Records shall be documented and maintained and shall be capable of identifying for each production and QCI lot (as applicable) of finished product, these items as a minimum.

a. The QCI tests performed on the lot, and their results.

b. The serial numbers (when applicable) of all devices in the lot.

c. The date of submission and completion of QCI of the lot.

d. Identification of lot.

e. The pertinent detail specification under which inspection was performed.

f. Final disposition of the lot (withdrawn, not accepted, accepted).

* 30.1.1.11 ESD handling control program. The ESD handling control program documentation for devices marked class 1 or 2 shall be under document control. This includes methods, equipment and materials, training, packaging, handling, and procedures for handling ESD sensitive devices.

30.1.1.12 Conversion of military specification requirements and methods into manufacturer's internal instructions. The procedure by which customer requirements, as expressed in specifications, purchase orders, etc., are converted into working instructions for the manufacturer's personnel shall be documented.

30.1.2 Program plan. The program plan shall be established and maintained by the manufacturer in accordance with 3.4.2 and shall be delivered to the qualifying activity for review prior to a survey, as a basis for manufacturer approval. It shall serve to demonstrate to the qualifying activity that the manufacturer's understanding of a complete product assurance program, as exemplified by his documentation system, is adequate to assure compliance of his product with the applicable specifications and quality standards. If the product assurance program exemplified is applied consistently to all products intended to be submitted for QCI under this specification, only one program plan is required. Differences in the program plan for different product categories (i.e., power transistors, rectifiers and thyristors, small signal diodes, small signal transistors, FETs, power regulators, small signal regulators, optoelectronics, etc.) shall be stated and explained in the program plan, or separate program plans prepared for such different product categories. Proprietary documents shall be clearly identified by category in the program plan. Proprietary documents need not be furnished with the product assurance plan. All documents shall be made available for review to the Government audit team upon request during an audit. The program plan shall contain, as a minimum, these items and they shall be available for review on site.

a. Functional block organizational chart (see 30.1.2.1).

b. Manufacturing flow chart (see 30.1.2.2).

c. Examples of design, material, equipment, visual standards, and processing instructions (see 30.1.2.3).

d. Examples of records (see 30.1.2.4).

e. Examples of design, material and process change control documents (see 30.1.1.5).

f. Examples of failure and defect analysis and feedback documents (see 30.1.1.7).

g. Examples of corrective action and evaluation documents (see 30.1.1.8).

h. Manufacturer's internal audit activities (see 30.1.2.5).

i. Manufacturer's SPC program plan and milestone.

30.1.2.1 Functional block organization chart. This chart shall show, in functional block-diagram form, the lines of authority and responsibility (both line and staff) for origination, approval, and implementation of the several aspects of the product assurance program. Names of incumbents are not required in this chart.

30.1.2.2 Manufacturing flow chart. This chart shall show, in flow chart form, the manufacturing sequence typical of the product category under consideration, including inspection and process-control stations. If desired, a separate chart may be used for quality assurance operations. Insofar as practical, each manufacturing flow chart station shall be keyed to the pertinent exemplary documents included in the program plan, to facilitate understanding of the interrelationships of the various documents.

30.1.2.3 Examples of design, material, equipment, visual standards, and process instructions. An example of each type of design, material, equipment, visual standard, and process instruction used in the manufacture of semiconductor devices intended to be submitted for acceptance inspection under this specification shall be included in the program plan. These may be either dummies or actual working documents, but shall in either event show the form of the pertinent document. Blank forms shall not be included.

30.1.2.4 Examples of records. Examples of records, complying with the requirements of 30.1.2.3 for instructions, shall be included in the program plan. Blank forms shall not be included.

30.1.2.5 Manufacturer's internal audit activities. The manufacturer's internal audit activity which identifies key review areas, their frequency of audit, and the corrective action system to be employed when variations from approved procedures or specification requirements are identified.

* 30.1.2.6 PPM customer feedback program. The manufacturer shall establish a feedback loop (with all military customers who request participation), to improve repeatability of tests and establish PPM correlation with customer incoming inspection.

APPENDIX D

40. MANUFACTURING CERTIFICATION REQUIREMENTS

40.1 Operations requiring certification. In addition to the requirements of section 30, the following manufacturing testing and inspection operations and controls require certification by the qualifying activity prior to the qualification of JAN, JANTX, JANTXV, and JANS:

a. Incoming inspection.

b. Control during manufacturing and assembly.

c. Wafer lot inspection (JANS only).

d. Die mounting.

e. Wire bonding or interconnection.

f. Preseal visual (JANTXV and JANS only), except clear glass diodes shall be post seal visual.

g. Sealing.

h. Testing.

* 40.1.1 Manufacturing certification documentation. The manufacturer shall submit a flow chart traveler and design and construction form 36D for each line to be certified to the qualifying activity prior to certification team visit. The flow chart shall identify all wafer fab and assembly operations, inspections, testing, quality verification points, and the point where all materials or subassemblies enter the flow. The chart will identify all documents pertaining to the inspection of materials, the production processes, the production environments, and production controls which were used. The documents will be identified by name and number, and revision in effect at the time of supplier certification or changes approved thereafter. Flow chart shall be kept current and complete for all lines and technologies. The documentation shall be readily available to the operating personnel at all times. It shall be made available to the qualifying activity for the purpose of verifying its existence, coverage, implementation, and adequacy.

40.1.1.1 Changes to certification documentation. Manufacturers shall notify the qualifying activity of any changes in the process listed in 3.4.3. Changes of certified process other than those in 3.4.3 shall be traceable through the document control system and be available to the audit team during an audit.

40.1.1.2 Process control charts. Process control charts shall be maintained during the manufacture semiconductors. The charts shall contain information such as: process step, lot number or date, mean, actual limits, and absolute limits and range. Where absolute limits are exceeded, the manufacturer shall document the corrective action taken.

40.1.2 Incoming, in-process, and outgoing inventory control. The methods and procedures shall be documented which are used to control storage and handling of incoming materials, work in-process, and warehoused and outgoing product in order to (a) achieve such factors as age control of limited-life materials, and (b) prevent inadvertent mixing of conforming and nonconforming materials, work, or finished product. Tests and inspections performed by the manufacturers on acquired materials and supplies shall include verification of chemical, physical, and functional characteristics required by manufacturer drawings and specifications. Procedures shall be prepared and maintained for controlling the receipt of acquired materials and supplies. The procedures shall provide for the following:

a. Withholding received materials or supplies from use pending completion of the reinspections or tests, or the receipt of necessary reports.

b. Segregation and identification of nonconforming materials and supplies from conforming materials and supplies and removal of nonconforming subassemblies and parts.

c. Identification and control of limited-life materials and supplies.

d. Identification and control of raw materials.

e. Assurance that the required tests reports, certifications, etc., have been received.

f. Clear identification of materials released from receiving inspection and test to clearly indicate acceptance or rejection status of material pending review action.

g. The supplier (whether manufacturer, distributor, dealer, stocker, etc.) shall have an inventory control system (see 4.1.1.3).

40.1.3 Wafer lot inspection (JANS only). The methods and procedures which are used to specify sample size, criteria for control of the wafer thickness, cleanliness, junction and surface preparation, metal deposition and thickness, etching, and alloying shall be documented. Records shall be maintained to show the results of all wafer lots submitted for inspection.

40.1.4 Die mount. The type of die mounting method, die material, die mounting material, package material, and mounting configuration shall be documented. The time, temperature, pressure, scrubbing, cleanliness, and environment shall also be specified.

* 40.1.4.1 Die-to-header strength. The manufacturer shall monitor the die attach integrity for all silicon transistors in accordance with test method 2017 or thermal response methods 3101, 3161, 3131, 3103, and 3104 of MIL-STD-750 using the manufacturer's documented procedure. This procedure shall be performed at each equipment set up as a minimum for JANTX and JANTXV and may, at the manufacturers option, consider other related factors. This test shall be conducted on a minimum of two devices from each die attach station at the start and finish of operator change, package type change, die size change and after every two hours of production for JANS. A different method of process control may be implemented, with the approval of the qualifying activity, if an appropriate thermal response method is performed in 100% screening.

In the event that the die shear is less than the value of table I of method 2017, or the test leaves less than 75 percent silicon remaining of die-to-header bond surface, the output of the die attach station shall not be used until tests show that satisfactory operation has been re-established. A procedure for the traceability, recovery, and disposition of all units bonded since the last successful die attach integrity test is required. This procedure shall provide for sample size, reject criteria, and disposition of failed lots. This test may be conducted on the same samples used for the wire bond strength test.

40.1.5 Wire bonding or interconnection. The bonding techniques, type of bond wire, and lead material used in connecting the die to the package leads shall be documented and comply with this specification and the applicable detail specifications. The temperature, pressure, dwell time, control of condition of capillary or electrode, ultrasonic power, composition of metals, lead dress, thickness to width ratio of bond, and environment shall be specified.

40.1.5.1 Bond strength. The manufacturer shall monitor the wire bond strength in accordance with test method 2037 of MIL-STD-750 using the manufacturer's documented procedure. This procedure shall be performed at each equipment setup as a minimum for JANTX and JANTXV and may, at the manufacturer's option consider change of operators, lot size, shift start and stop, and other related factors.

As a minimum for JANS each operator/wire bonding station shall have two device samples taken at the start and end of each shift, after each two hours of production, and after changing operators, spools, shifts, packages, wire size, and maintenance of equipment. When more than one lot is processed for JANS in a two-hour period, samples shall be tested from each lot. Pull strength data shall be read and recorded and shall be control charted and maintained in accordance with the specified requirements. Data shall include the force, in grams, required for failure, the physical location of the point of failure, and the nature of the failure. In event that any bond strength is less than the pre-seal value given in table I, method 2037, of MIL-STD-750, the bonder shall be inactivated immediately and not returned to production until tests show that satisfactory operation has been re-established. When the system at the die surface is bimetallic and the lead wires are less than 5 mils in diameter, the lead shall be pulled to destruction and if the chip bond lifts before the wire breaks, the lot shall be rejected. A procedure for the traceability, recovery, and disposition of all units bonded since the last successful bond strength test is required. This procedure shall provide for sample size, number of bonds and device to be tested, reject criteria, and disposition of failed lots.

40.1.6 Internal visual inspection (JANS and JANTXV only). Visual inspection procedures shall specify inspection criteria, the use of visual aids, and shall comply with the requirements of methods 2069, 2070, 2072 or 2073 (die visual), and 2074 of MIL-STD-750.

40.1.6.1 Handling of inspected devices. Devices which have been inspected shall be protected from the time of inspection to final seal in such a manner that they will not be exposed to an environment worse than that in which internal visual inspection was performed.

40.1.7 Sealing. The type of seals, sealing materials and methods used in production shall be documented. Sealing variables such as pre-seal bake, moisture content of the sealing environment, time, temperature, flow rate of gases, profile and welding controls, etc., shall also be documented (see 3.6.1, 3.6.1.1, and 3.6.1.2).

40.1.8 Screening, test, and inspection equipment. The equipment for screening, testing and inspection, and the procedures delineating their use, shall be evaluated during certification.

40.1.9 Failure and defect analysis and feedback. The procedures for identification, handling, and analysis of failed or defective devices and for dissemination of analysis data shall be documented, including the procedure for informing the qualifying activity of analysis results, when applicable. Records of failed or defective devices shall be maintained and shall cover the source from which each device was received, the test or operation during which failure occurred or defects were observed and prior testing or screening history of the device, the date of receipt, and the disposition of the device. Records of failure and defect analyses shall cover the nature of the reported failure or defect (failure or defect mode), verification of the failure or defect, the nature of any device discrepancies which were found during analysis (failure or defect mechanism), assignment of the failure - activating cause if possible, the date of completion of the analysis, identification of the group performing the analysis, disposition of the device after analysis, and the distribution of the record. The record shall also treat the relationship of observed failure or defect modes in related lots or devices, and, where applicable, corrective action taken as a result of the findings.

40.1.10 Control during manufacturing and assembly. The relative humidity, temperature, and particle count for each critical process step (e.g., wafer fabrication, assembly) shall be specified, controlled, and recorded. The procedures and techniques for measuring these environmental parameters and limits shall be documented. The procedures shall contain corrective actions for out-of-tolerance environmental conditions. Unsealed parts shall be handled in such a way as to minimize the introduction of foreign material into the sealed cavity. The purity of water shall be specified, measured, controlled, and recorded in terms of minimum resistivity at +25°C (resistivity meters and cells shall be calibrated), maximum total solids, maximum organic impurities, and maximum bacteria count.

40.1.10.1 Particle count measurements. Particle count measurements in the clean room and clean work station areas shall be in accordance with test method 5010 of MIL-STD-750.

40.1.10.2 JANS, JANTXV, and JANTX critical wafer fabrication areas. JANS, JANTXV, and JANTX wafer production fabrication areas shall be maintained in class 100,000 maximum until a wafer probe or a wafer saw or background operation is performed. Wafers shall be kept in particle free, covered, protective carriers throughout the fabrication process. They shall be exposed only to class 1000 or better when outside the carriers, during the following critical steps:

a. Immediately after cleaning and prior to exposure to a high temperature process (e.g., diffusion, thermal oxidation, silox reflow).

b. Immediately after cleaning and prior to photoresist deposition.

For the purpose of this class 1000 restriction: A cleaning requires exposure of wafers to a cleaning liquid, and not just a pressurized gas blow off. Handling in class 100,000 is allowed outside the carriers for processing immediately before and during a cleaning operation, and during and after photoresist deposition. This requirement does not apply to large geometry devices where the distance between any two features is greater than 0.0015 inches (0.038 mm).

* 40.1.10.3 Pre-seal visual inspection for JANS and JANTXV. Pre-seal visual inspection for JANS shall be performed under class 100 laminar flow hoods. For JANTXV this inspection shall be conducted under class 1,000 laminar flow hoods. After pre-seal inspection, devices shall be maintained under the same environmental conditions as at pre-seal except over bake until final seal.

40.1.11 Electrical stability of devices. Procedures, techniques, and data to prove that the devices are electrically stable shall be evaluated.

40.1.12 Maintenance of certification. The manufacturer shall maintain materials control during wafer fabrication, assembly, and test in accordance with the procedures and plans approved by the certification team. Using the process flow charts as a baseline, the certified line shall be monitored periodically by the certification team or its representatives. This audit is to assure that the line is still in certified condition, and that all process and process control changes are properly documented and implemented.

40.1.13 Clear glass diode visual inspection. In addition to the requirements of 40.1.6, the manufacturer shall monitor the lead-to-glass seal following final plating operation for all JANTX, JANTXV, and JANS clear glass diodes constructed with borated seal, using the manufacturer's documented procedure. The procedures shall specify criteria and visual aids and shall be capable of detecting significant loss of glass-to-lead seal.

40.1.14 Particle detection monitorial program. The manufacturer shall establish a particle detection monitoring program which assesses the source of particle contamination of sealed cavity devices on an individual manufacturing line basis. The monitor shall use the test set-up as specified in method 2052 of MIL-STD-750. JEDEC Publication 114, "Guidelines for Particle Impact Noise Detection (PIND) Testing, Operator Training, and Certification" may be used as a guideline. This monitor is applicable to all metal or ceramic cavity package outlines, unless otherwise exempt herein. This monitor shall be performed at the assembly location, or locations, to ensure the most effective feedback loop for corrective action.

50. SELF-AUDIT REQUIREMENTS

50.1 Self-audit requirements. This portion of appendix D contains details for implementation of the minimum requirements to be used in the manufacturer's self-audit program. The intent of this self-audit program is to assure continued conformance to military specification requirements.

60. DEFINITIONS

60.1 Self-audit. The performance of periodic surveys and reviews by the device manufacturer's designated personnel to evaluate compliance to military specifications.

60.2 Audit checklist. A form listing specific items which are to be audited.

70. GENERAL

70.1 Self-audit program. The manufacturer shall establish an independent self-audit program under the direction of the quality organization to assess the effectiveness of the manufacturer's compliance to all applicable specifications. The manufacturer's self-audit program which identifies key review areas, their frequency of audit, and the corrective action system to be employed when variations from the approved procedures or specification requirements are identified shall be included in the program plan. The self-audit program shall, as a minimum, incorporate the following requirements.

70.1.1 Correction of deficiencies. A system to identify and correct any deficiencies (e.g., processing and testing) or deviations from the specification requirements.

70.1.2 Deviation from critical documents. Provide for review of all deviations from critical documents, such as, baseline(s), flow chart(s), traveler(s), QCI procedures, etc.

70.1.3 Training and retention of auditors. Specify the selection and training/retraining requirements for auditors.

70.1.4 Self-audit schedule and frequency. Specify the self-audit frequencies and require that a schedule be established and adhered to.

70.2 Self-audit representatives. The quality assurance representatives or designated appointees shall perform all self-audits. The designated auditors shall be independent from the area being audited. If the use of any independent auditor is not practical, then as a minimum, another individual should be assigned to participate in the audit or review the results with the auditor from the area. The auditors shall be trained in the area to be audited, in the applicable military specification requirement and provided with an appropriate checklist for annotating deficiencies. Prior to the audit, the assigned auditor(s) shall review the previous audit checklist to assure corrective actions have been implemented and are sufficient to correct the deficiencies.

70.3 Audit deficiencies. All audit deficiencies shall be documented on the appropriate forms and a copy submitted to the department head for corrective action(s). All corrective actions shall be agreed to by the quality organization or Material Review Board.

70.4 Audit follow up. All audit reports will be filed and maintained by the quality organization. The quality organization shall establish a procedure to follow up on all audit deficiencies to assure that the corrective actions have been implemented in a timely manner. A system (e.g., Management Review) shall also be established to review the acceptability and timeliness of all corrective actions and to determine if any deficiencies have repeated since the last required self-audit. If any deficiencies have occurred two or more times in the predetermined time period, additional corrective actions shall be taken to assure immediate correction of the problem and the qualifying activity shall be notified. The self-audit team shall also perform a 6-month follow-up verification of corrective actions covering all deficiencies found during the qualifying activity audit and annual self-audit to assure corrective actions are adequate and maintained.

70.5 Audit schedules and frequencies. The original audit frequency shall be established with a schedule by the quality organization but in no case exceed 1 year for each area, unless authorized by the qualifying activity. A self-audit shall be conducted and corrective actions completed prior to the initial qualifying activity audit. Changes to the frequency of audit due to being consistently above or below average performance on the self-audit shall require approval of the qualifying activity.

* 70.6 Self-audit report. The manufacturer shall submit a comprehensive initial self audit report. Subsequent reports shall be kept on file by the manufacturer. The self-audit report shall be signed by the quality assurance representative responsible for its overall success or failure. The manufacturer shall keep the self-audit report on file for a minimum of 4 years. The manufacturer shall make available to the qualifying activity, during reaudits, the self-audit report, deficiencies, and corrective actions taken. The qualifying activity may modify the frequency of the self-audit or require additional testing based on the self-audit report. A successful self-audit program can be used by the qualifying activity to extend the reaudit interval or reduce the audit time duration. If the qualifying activity determines the self-audit program is ineffective and unacceptable, certification approval will be withheld.

70.7 Self-audit areas. The self-audit will be performed to assure conformance to the checklist and military specification in at least the following areas:

Areas

| | |
|---|---|
| Calibration and preventive maintenance | DI water controls |
| Fabrication | Training |
| Assembly operations | Failure analysis |
| Electrical test | Qualification/QCI system |
| Test methods | Document control |
| Environmental control | Design change control |
| Incoming inspection | |
| Inventory control and traceability | |

70.8 Self-audit checklist. The audit checklist shall be prepared by the quality organization and maintained under document control. The checklist shall assure that the quality assurance system is adequate and followed by all personnel in each area.

* 70.9 Authorized distributors and suppliers responsibilities. All manufacturers shall audit their authorized distributors in accordance with their internal quality program (program plan). As a minimum, the quality plan shall establish and report the following:

1. Frequency of audits (frequency may vary or be adjusted between authorized distributors based on history.

2. Any nonconformance (particularly attention to authorized alterations or misrepresentations of the following:

   a. The date code

   b. The C of C

   c. The quantities in a lot

   d. The part marking (color coding)

   e. Unauthorized testing or value added processing

   f. Putting returns back into inventory

3. The sales function and/or any other procedure or service the distributor is authorized to perform.

APPENDIX E

PROVISIONS GOVERNING THE QUALIFICATION OF SEMICONDUCTORS
ASSEMBLED AT A FOREIGN PLANT OR A DOMESTIC CONTRACTED PLANT

10. SCOPE

* 10.1 Scope. The following procedures in section 40 will be used when a company having qualification under MIL-S-19500 of a semiconductor device produced at a plant in the United States, desires to perform certain assembly operations at a plant in a foreign country. The following procedures in section 50 will be used when a company desires to perform certain assembly operations at a domestic contracted plant to qualify the device as totally manufactured domestically. These requirements are based on 4-105.6 of Defense Standardization Manual 4120.3-M and do not apply to extension of qualification from a foreign manufacturing plant to a U.S. plant. This appendix is a mandatory part of the specification. The information contained herein is intended for compliance.

* 10.2 Eligibility. To be eligible for qualification of a foreign-assembled device, a U.S. manufacturer must first qualify that device as totally manufactured at the basic plant. Domestic contracted plants shall comply with all manufacturer certification requirements of 3.4.2.2 herein prior to qualification tests and QPL listing.

* 10.2.1 Foreign plant audits. The qualifying activity reserves the right to audit the foreign assembly plant with a minimum notice. The basic plant site shall be responsible to facilitate all qualifying activity site visits. Any refusal to allow such a site visit may result in an immediate de-certification and QPL removal. All qualifying activity's expenses to issue certification or reaudit to maintain certification to the foreign plant(s) shall be borne by the foreign plant and/or basic plant. Furthermore, the basic plant and/or foreign plant shall be responsible for any established fees to cover the cost of product qualification.

* 10.2.1.1 Foreign plant audit compliance. As of the date of this specification, no new qualification extensions will be granted, until the plant has requested a certification audit for their foreign plant. All basic plants shall have requested a certification audit and agreed to bear cost/expense per 10.2.1, within two years from the date of this specification, or their qualification will be removed, from their foreign plant.

20. APPLICABLE DOCUMENTS. DLAM 8200: Procurement quality assurance support manual for defense contract administration services.

30. DEFINITIONS

* 30.1 Basic plant. The plant, in the United States, where wafer processing, die diffusion, inspection of all wafers or chips (dice) are performed. The basic plant has full responsibility for device performance, quality assurance, and reliability. The basic plant's logo or CAGE code shall appear on the finished product.

* 30.2 Foreign assembly plant (owned by basic plant). A plant, owned by the basic plant, (or in accordance with 30.2.1), in a foreign country at which die attachment, lead bonding, and final seal are performed. The address of the approved foreign assembly plants shall be included on the QPL. No foreign assembled devices shall be JAN branded until approval for such listing has been granted, except as provided in 3.7.11 for first lot test samples.

* 30.2.1 Foreign contracted assembly plant (not owned by basic plant). Effective immediately, qualification listing to contracted (unowned) foreign plants shall expire on the implementation date of this specification by written QPL removal letters from the qualifying activity. Effective immediately, contracted foreign assembly shall be prohibited unless otherwise specified in the detail specification as follows "foreign contracted assembly is allowed." This clause will only be used on a case by case basis (i.e., to prevent a zero source situation.)

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* 30.3 Domestic contracted assembly plant (unowned by basic plant). A plant, in the United States, that has been certified by the qualifying activity to perform die attach, lead bonding, and final seal operations for case outlines shown in appendix F herein. Qualification of (domestic contracted) assembled devices will be the responsibility of the basic plant. The address of the domestic contracted assembly plant shall be included on the QPL. QPL manufacturers may offer their services as domestic contracted assembly plants for any package style they are certified for.

40. QUALIFICATION EXTENSION PROVISIONS

* 40.1 Conditions for extension. When a company has qualified a device that is produced at a basic plant and subsequently desires to do die attachment, lead bonding, and sealing at a foreign owned assembly plant, qualification may be extended under the following conditions:

a. Offshore operations are limited to the processes listed above. Cleaning (i.e., alcohol or deionized water) which does not alter or further process the die/wafer is permitted.

b. All device wafers or chips must be completely processed and inspected in the basic plant. A complete die includes, as a minimum, all steps of appendix D, 30.1.1.4 through g. However, acquisition of raw silicon wafers with expitaxial deposition from offshore sources for use in the domestic facility is permitted. (Formed junction material is prohibited from any acquisition.) Off shore die separation (i.e., scribe and break, saw through, laser scribe) are permitted. However, junction alteration (i.e., leveling) is prohibited. (Leveling is the removal of silicon, oxide, or metal from an exposed junction by the means of an acid or caustic etch). Removal of loose silicon particles or organic contamination with simple nonisotrophic chemical (i.e., alcohol and the deionized water) is permitted.

* c. All quality control operations, procedures, and standards at the foreign plant must be under the control of the basic plant's quality assurance manager or employee, who has been trained at the basic plant on all operations to be used at the foreign assembly plant. All such operations, procedures, and standards must be maintained on site in the foreign assembly plant at all times while JAN products are being assembled.

All quality control operations, procedures, and standards at the foreign plant must be approved by the basic plant and certified by the qualifying activity. No changes in any of the related operations can be changed without approval from the basic plant.

d. Devices assembled by foreign assembly plants must have a coding on each device to identify the assembly plant (see 3.7.8.1).

e. After assembly, the devices intended to become JAN shall be returned to the basic plant for screening and QCI prior to delivery, except as defined by 3.9.1 and 3.9.2.

40.2 Material to be submitted. The following information concerning the manufacturing and quality control operations of a company utilizing a foreign assembly plant shall be furnished to the qualifying activity:

a. Organization charts showing management, quality control, and production relationships between the basic plant and the assembly plant.

b. Detailed flow charts of all semiconductor device process operations and inspections performed at the foreign assembly plant and at the basic plant. The charts shall identify the documents detailing the various manufacturing and inspection operations. The qualifying activity may request copies of any document associated with the flow charts if necessary to clarify the charts. Proprietary documents are to be identified. They need not be furnished, but shall be made available for review at the basic plant by authorized representatives of the qualifying activity.

c. Lists of production facilities used in die bonding and lead attachment, and test facilities which are used on the assembly line for both the basic plant and for the foreign assembly plant, using figures 6 and 7. The operation and inspection numbers from the flow charts shall be shown on these lists.

d. Photographs showing exterior and interior views of the foreign assembly plant.

* e. Quality conformance test data from the first production lot for each of the package styles manufactured at the assembly plant, compiled in the manufacturer's standard report format. The report shall contain MIL-S-19500 group A variables data, group B and C summary data and end-points after life tests.

* f. If a package style has already been approved at a facility, domestic QPL listings may be extended by submitting a formal request which includes device types to be extended along with applicable test report numbers, showing package style was previously approved at test location.

g. Ten tested and fully marked samples for each detail specification and package type. The samples shall be labeled to identify the test subgroup.

h. A statement by a responsible company official showing the corporate or other degree of ownership and control of the assembly plant by the basic plant.

i. A copy of a survey report by a responsible official of the basic plant, verifying that the assembly plant has been found acceptable and that all the information and material furnished to the qualifying activity is complete and accurate.

40.3 Retention of product extension approval. To retain qualification approval of a device that is assembled at a foreign plant, qualification shall be maintained for that device manufactured at the basic plant. The retention of qualification requirements of MIL-S-19500 are applicable to both the foreign plant and the basic plant.

40.4 Nonapproved plants. Products assembled at any plant location other than the ones approved for listing on the QPL are not in accordance with the qualification terms specified herein and, therefore, are not considered qualified products and may not be marked or sold as such.

* 50. DOMESTIC CONTRACTED ASSEMBLY PROVISIONS

* 50.1 Domestic contracted assembly selection. The basic plant shall request the use of third party assembly and receive approval from the qualifying activity. The domestic contracted party assembly plant shall meet all assembly related requirements and quality assurance provisions as specified herein. The basic plant shall submit to the qualifying activity a domestic contracted management plan that demonstrates how the requirements and quality assurance provisions of this specification will be managed at the domestic contracted assembly plant.

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* 50.2 Domestic contracted management plan. The information contained in this plan shall be a part of the basic plant's existing product assurance program plan. The following areas shall be addressed:

a. General basic plant requirements for selecting and approving a domestic contracted assembly plant.

b. Traceability from wafer lot through production lot to inspection lot date code as defined by the basic plant.

c. Process controls and capability based on statistical evaluation system and control methods.

d. Self audit program of third party plant.

e. Failure/defect analysis and feedback/corrective action system. This system shall include production inspections and process error corrections that take place on the assembly line.

* 50.2.1 Documentation. Conversion of basic plant documentation to domestic contracted assembly plant documentation shall be addressed in the basic plant's management plan. The domestic contracted assembler shall convert the basic plant(s) requirements into an internal documentation control system of flow charts, travelers, change control, and product inventory controls and shall be capable of ensuring product traceability.

* 50.3 Approval of domestic contracted assembly. The certification requirements specified herein are intended for manufacturers who intend to engage the services of a domestic contracted assembly plant. Certification is granted to the basic plant on the basis of a certification audit. Domestic contracted assembly plants will receive assembly suitability based on the certification audit and on the demonstrated capabilities to assemble case outline families shown in appendix F herein, as a minimum. (The contracted assembly plants shall be certified by the qualifying activity.)

* 50.4 Domestic contracted retention of assembly suitability. Approved domestic contracted assembly plants shall report nonconformances in parts per million (PPM) using PPM-4, hermetic nonconformance, as described by EIA-554. The domestic contracted assembly plant shall report annually using calculation and data exclusion options of method B of EIA-554. The report shall show a six-month moving average for each month of the reporting period.

APPENDIX E

List of production facilities

Name of firm:
Plant address:

Date:
Specification no:
Amendment no:

| Operation | Operation number if applicable | Equipment description | Manufacturer | Type or model number | Number in use |
|---|---|---|---|---|---|
| | | | | | |

FIGURE 6. List of production facilities.

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List of production facilities

Name of firm:
Plant address:

Date:
Specification no:
Amendment no:

| Production test | Equipment | Manufacturer | Type or model | Serial or inventory number | Description and use (included dimensions, measuring device, and controls, as applicable) | Equipment limits (include multiple ranges) | Accuracy |
|---|---|---|---|---|---|---|---|
| | | | | | | | |

FIGURE 7. List of production facilities.

APPENDIX F

CASE OUTLINES

10. SCOPE

10.1 Scope. This appendix details the rules for dimensioning popular case outlines used with discrete semiconductor devices. This appendix is a mandatory part of the specification. The information contained herein is intended for compliance.

20. APPLICABLE DOCUMENT. This section is not applicable to this appendix.

30. GENERAL

30.1 Definitions. The following definitions apply to this appendix.

30.1.1 Seating plane. The reference plane which designates the interface between the package and the surface on which it is mounted.

30.1.2 Body. That part of the package exclusive of electrical terminals, studs, or leads.

30.1.3 Terminal. That part of the package used in making an electrical, mechanical, or thermal connection. Examples of terminals are flexible leads, rigid leads, studs, and cases which serve as electrical connections.

30.1.4 Visual index. A referenced mark, chamfer, notch, tab, flat, extended terminal, or groove which identifies the number one terminal position.

40. CASE OUTLINE PRESENTATION

40.1 Outline identification. Outlines included in this appendix shall be identified by a letter, a dash, then a number-suffix combination. The letter T shall be used to designate transistor and thyristor outlines and D for diode outlines. Numbers shall be assigned sequentially within each group to designate a family of outlines. One suffix letter shall be added to designate one of a family of outlines (e.g., T-1A, T-1B, D-1A, and D-2B).

40.2 Dimensioning symbols. The symbols for dimensioning case outlines shall be as listed below.

| | |
|---|---|
| BD | Body diameter. |
| BL | Body length. |
| BW | Body width. |
| CD | Largest diameter of body (case diameter). |
| CH | Distance from seating plane to top of body (case height). |
| ECT | End cap thickness. |
| F | Overall dimension of flange or hexagon zone including any fillet. |
| $F_1$ | Dimension of a flange or hexagon zone excluding any fillet. |
| FL | Longest dimension between seating plane and center of hole in the lug of a terminal (flag length). |
| FW | Major cross section dimension of a terminal (flag width). |
| HD | Header diameter. |

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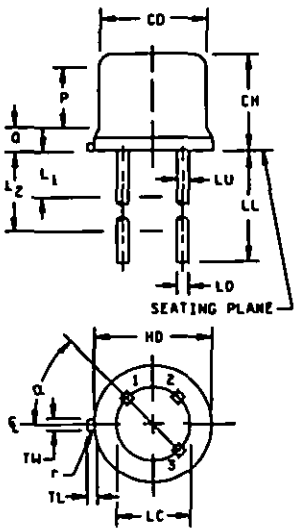
| | |
|---|---|
| HF | Distance across flats dimension of a hexagon (hexagon flats). |
| HR | Curve radii associated with body (header radius). |
| HR2 | Curve radii associated with body (header radius). |
| HT | Header thickness. |
| LC | Diameter of the circle upon which the terminal positions are located (lead circle). |
| LD | Diameter of round (wire) terminals (lead diameter). |
| LL | Overall terminal length (lead length). |
| $L_1$ | Length of uncontrolled cross section of terminal. |
| LS | Largest dimension, excluding terminals, on the major axis of a noncircular body. |
| MHD | Diameter of mounting holes (mounting hole diameter). |
| MHS | Distance between centers of two mounting holes (mounting hole spacing). |
| OAH | Over all height from seating plane. |
| P | Length of controlled zone of body. |
| PS | Linear distance between two terminal centers (pin spacing). |
| Q | Other dimensions. |
| SD | Pitch diameter in accordance with FED-STD-H28 (stud diameter). |
| SL | Overall length of stud. |
| SU | Length of incomplete or undercut threads (stud undercut). |
| TL | Length of visual index (tab length). |
| TW | Width of visual index (tab width). |
| UD | Diameter of thread relief zone (undercut diameter). |
| c | Minor cross section dimension of a terminal. |
| r | Index tab radii. |
| S | Miscellaneous dimensions of terminal flat relative to terminal hole. |
| $\phi$T | Diameter of hole in terminal. |
| $\alpha$ | Index datum angle to first terminal position on each pin circle. |
| $\beta$ | Angular spacing between adjacent terminal positions. |

NOTE: Subscript numbers may be included when more than one dimension is specified for a given symbol (e.g.F1, HR2).

40.3 Outline number. The outline numbers shall be as listed below:

| Outline number | Similar to JEDEC number | Figure number | Page number |
|---|---|---|---|
| T-1A (3 - 1.5" leads, number 3 connected to case) | TO-205AA(TO-5) | 8 | 110 |
| T-1B (3 - 1.5" leads, all isolated from case) | TO-205AA(TO-5) | 8 | 110 |
| T-1C (3 - .5 leads, number 3 connected to case) | TO-205AD(TO-39) | 8 | 110 |
| T-1D (3 - .5" leads, all isolated from case) | TO-205AD(TO-39) | 8 | 110 |
| T-1E (3 - .5" leads, number 3 connected to case) low profile | TO-205AF(TO-39) | 8 | 110 |
| T-2A (3 - .5" leads, number 3 connected to case) | TO-206AA(TO-18) | 9 | 111-112 |
| T-2B (3 - .5" leads, number 3 connected to case) | TO-206AB(TO-46) | 9 | 111-112 |
| T-3A (4 - .5" leads, number 4 connected to case) | TO-206AF(TO-72) | 10 | 113-114 |
| T-4A (40 mil diameter leads) | TO-204AA(TO-3) | 11 | 115-116 |
| T-4B (50 mil diameter leads) | TO-204AD(TO-3) | 11 | 115-116 |
| T-4C (60 mil diameter leads) | TO-204AE(TO-3) | 11 | 115-116 |
| T-5A (30 mil diameter leads) | TO-213AA(TO-66) | 12 | 117-118 |
| T-6A (120° lead orientation, number 3 connected to case) | TO-210AA(TO-59) | 13 | 119-121 |
| T-6B (90° lead orientation, all isolated from case) | TO-210AA(TO-59) | 13 | 119-121 |
| T-6C (120° lead orientation, number 3 isolated from case) | TO-210AA(TO-59) | 13 | 119-121 |
| T-7A (lead number 3 connected to case) | TO-210AC(TO-61) | 14 | 122-123 |
| T-7B (all leads isolated from case) | TO-210AC(TO-61) | 14 | 122-123 |

APPENDIX F




| Inches | mm | Inches | mm |
|---|---|---|---|
| .010 | 0.25 | .180 | 4.57 |
| .016 | 0.41 | .200 | 5.08 |
| .019 | 0.48 | .240 | 6.10 |
| .021 | 0.53 | .250 | 6.35 |
| .028 | 0.71 | .260 | 6.60 |
| .029 | 0.74 | .305 | 7.75 |
| .034 | 0.86 | .335 | 8.51 |
| .040 | 1.02 | .370 | 9.40 |
| .045 | 1.14 | .500 | 12.70 |
| .050 | 1.27 | .750 | 19.05 |
| .100 | 2.54 | 1.500 | 38.10 |
| .160 | 4.06 | 1.750 | 44.45 |

| Symbol | T-1A | | T-1B | | T-1C | | T-1D | | T-1E | | Note |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | |
| CD | .305 | .335 | .305 | .335 | .305 | .335 | .305 | .335 | .305 | .335 | |
| CH | .240 | .260 | .240 | .260 | .240 | .260 | .240 | .260 | .160 | .180 | |
| HD | .335 | .370 | .335 | .370 | .335 | .370 | .335 | .370 | .335 | .370 | |
| LC | .200 TP | | .200 TP | | .200 TP | | .200 TP | | .200 TP | | 6 |
| LD | .016 | .021 | .016 | .021 | .016 | .021 | .016 | .021 | .016 | .021 | 7 |
| LL | 1.500 | 1.750 | 1.500 | 1.750 | .500 | .750 | .500 | .750 | .500 | .750 | 7 |
| LU | .016 | .019 | .016 | .019 | .016 | .019 | .016 | .019 | .016 | .019 | 7 |
| $L_1$ | | .050 | | .050 | | .050 | | .050 | | .050 | 7 |
| $L_2$ | .250 | | .250 | | .250 | | .250 | | .250 | | 7 |
| TL | .029 | .045 | .029 | .045 | .029 | .045 | .029 | .045 | .029 | .045 | 3 |
| TW | .028 | .034 | .028 | .034 | .028 | .034 | .028 | .034 | .028 | .034 | 10 |
| P | .100 | | .100 | | .100 | | .100 | | .100 | | 5 |
| Q | | .040 | | .040 | | .040 | | .040 | | .040 | 4 |
| r | | .010 | | .010 | | .010 | | .010 | | .010 | 11 |
| $\alpha$ | 45° | TP | 45° | TP | 45° | TP | 45° | TP | 45° | TP | 6 |
| Notes | 1,2,8,9 | | 1,2,8 | | 1,2,8,9 | | 1,2,8 | | 1,2,8,9 | | |

NOTES:

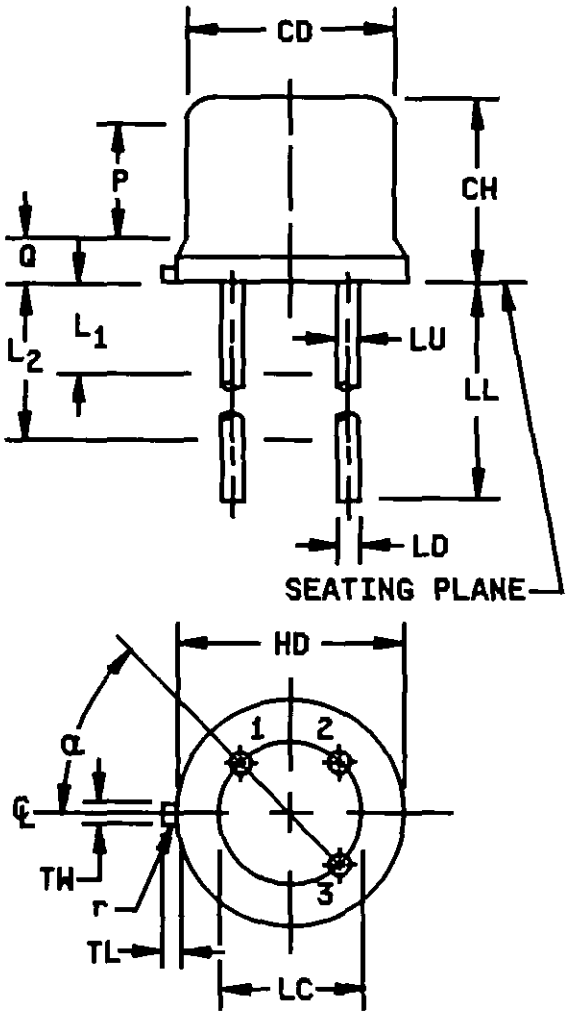
1. Dimensions are in inches.
2. Metric equivalents are given for general information only.
3. Symbol TL is measured from HD maximum.
4. Details of outline in this zone are optional.
5. Symbol CD shall not vary more than .010 (0.25 mm) in zone P. This zone is controlled for automatic handling.
6. Leads at gauge plane .054 inch (1.37 mm) +.001 inch (0.03 mm) -.000 inch (0.00 mm) below seating plane shall be within .007 inch (0.18 mm) radius of true position (TP) relative to tab. Device may be measured by direct methods or by gauge.
7. Symbol LD applies between $L_1$ and $L_2$. *Dimension LD applies between $L_2$ and LL minimum.* Lead diameter shall not exceed .042 inch (1.07 mm) within $L_1$ and beyond LL minimum.
8. Lead designation, depending on device type, shall be as follows:

| Lead number | Bipolar transistor | FET | Thyristor |
|---|---|---|---|
| 1 | Emitter | Source | Cathode |
| 2 | Base | Gate | Gate |
| 3 | Collector | Drain | Anode |

9. Lead number three is electrically connected to case.
10. Beyond r maximum, TW shall be held for a minimum length of .011 inch (0.28 mm).
11. *Symbol r applied to both inside corners of tab.*

FIGURE 8. Physical dimensions of T-1 family. (Similar to TO-5, TO-39)

| Symbol | T-2A | | T-2B | | Note |
|---|---|---|---|---|---|
| | Min | Max | Min | Max | |
| CD | .178 | .195 | .178 | .195 | |
| CH | .170 | .210 | .240 | .260 | |
| HD | .209 | .230 | .209 | .230 | |
| LC | .100 TP | | .100 TP | | 6 |
| LD | .016 | .021 | .016 | .021 | 7 |
| LL | .500 | .750 | .500 | .750 | 7 |
| LU | .016 | .019 | .016 | .019 | 7 |
| $L_1$ | | .050 | | .050 | 7 |
| $L_2$ | .250 | | .250 | | 7 |
| TL | .028 | .048 | .028 | .048 | 3 |
| TW | .036 | .046 | .036 | .046 | 10 |
| P | .100 | | | | |
| Q | | .040 | | .040 | 4 |
| r | | .007 | | .007 | 11 |
| $\alpha$ | 45° TP | | 45° TP | | 6 |
| Notes | 1, 2, 8, 9 | | 1, 2, 8, 9 | | |




| Inches | mm | Inches | mm |
|---|---|---|---|
| .007 | 0.18 | .170 | 4.43 |
| .016 | 0.41 | .178 | 4.52 |
| .019 | 0.48 | .195 | 4.95 |
| .021 | 0.53 | .209 | 5.31 |
| .028 | 0.71 | .210 | 5.33 |
| .036 | 0.91 | .230 | 5.84 |
| .040 | 1.02 | .240 | 6.10 |
| .046 | 1.17 | .250 | 6.35 |
| .048 | 1.22 | .260 | 6.60 |
| .050 | 1.27 | .500 | 12.70 |
| .100 | 2.54 | .750 | 19.05 |

FIGURE 9. Physical dimensions of T-2 family. (Similar to TO-18, TO-46)

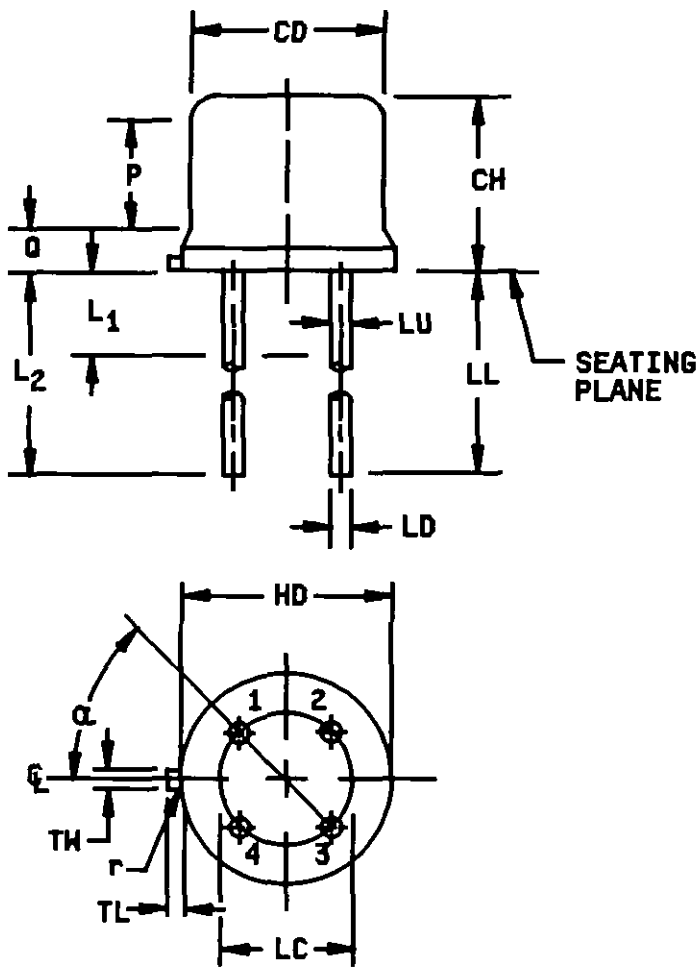
NOTES:
1. Dimensions are in inches.
2. Metric equivalents are given for general information only.
3. Symbol TL is measured from HD maximum.
4. Details of outline in this zone are optional.
5. Symbol CD shall not vary more than .010 inch (0.25 mm) in zone P. This zone is controlled for automatic handling.
6. Leads at gauge plane .054 inch (1.37 mm) +.001 inch (0.03 mm) -.000 inch (0.00 mm) below seating plane shall be within .007 inch (0.18 mm) radius of TP relative to tab. Device may be measured by direct methods or by gauge.
7. Symbol LU applies between $L_1$ and $L_2$. Dimension LD applies between $L_2$ and LL minimum. Lead diameter shall not exceed .042 inch (1.07 mm) within $L_1$ and beyond LL minimum.
8. Lead designation, depending on device type, shall be as follows:

| Lead number | Bipolar transistor | FET | Thyristor |
|---|---|---|---|
| 1 | Emitter | Gate | Cathode |
| 2 | Base | Source | Gate |
| 3 | Collector | Drain | Anode |

9. Lead number three is electrically connected to case.
10. Beyond r maximum, TW shall be held for a minimum length of .011 inch (0.28 mm).
11. Symbol r applied to both inside corners of tab.

FIGURE 9. Physical dimensions of T-2 family (Similar to TO-18, TO-46) - Continued.

| Symbol | T-3A | | Note |
|---|---|---|---|
| | Min | Max | |
| CD | .178 | .195 | |
| CH | .170 | .210 | |
| HD | .209 | .230 | |
| LC | .100 TP | | 6 |
| LD | .016 | .021 | 7 |
| LL | .500 | .750 | 7 |
| LU | .016 | .019 | 7 |
| $L_1$ | --- | .050 | 7 |
| $L_2$ | .250 | --- | 7 |
| TL | .028 | .048 | 3 |
| TW | .036 | .046 | 10 |
| P | .100 | --- | |
| Q | --- | .040 | 4 |
| r | --- | .007 | 11 |
| α | 45° TP | | 6 |
| Notes | 1, 2, 8, 9 | | |




| Inches | mm | Inches | mm |
|---|---|---|---|
| .007 | 0.18 | .100 | 2.54 |
| .016 | 0.41 | .170 | 4.32 |
| .019 | 0.48 | .178 | 4.52 |
| .021 | 0.53 | .195 | 4.95 |
| .028 | 0.71 | .209 | 5.31 |
| .036 | 0.91 | .210 | 5.33 |
| .040 | 1.02 | .230 | 5.84 |
| .046 | 1.17 | .250 | 6.35 |
| .048 | 1.22 | .500 | 12.70 |
| .050 | 1.27 | .750 | 19.05 |

FIGURE 10. Physical dimensions of T-3 family. (Similar to TO-72)

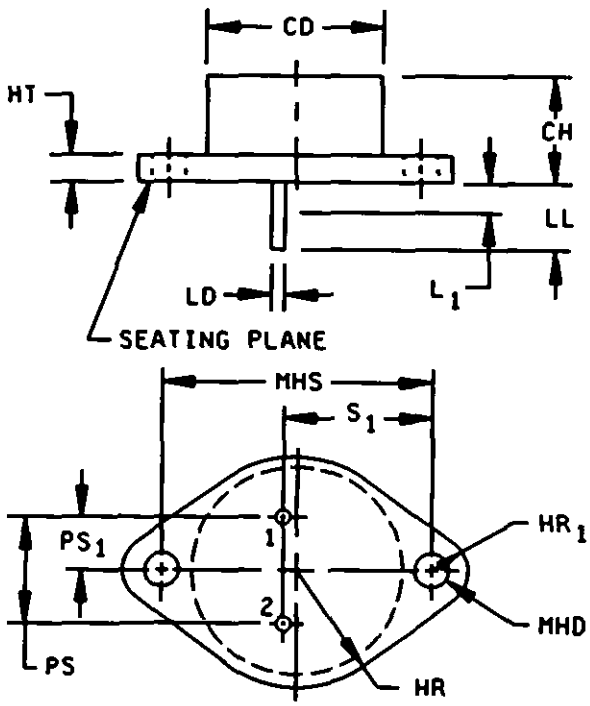
NOTES:
1. Dimensions are in inches.
2. Metric equivalents are given for general information only.
3. Symbol TL is measured from HD maximum.
4. Details of outline in this zone are optional.
5. Symbol CD shall not vary more than .010 inch (0.25 mm) in zone P. This zone is controlled for automatic handling.
6. Leads at gauge plane .054 inch (1.37 mm) +.001 inch (0.03 mm) -.000 inch (0.00 mm) below seating plane shall be within .007 inch (0.18 mm) radius of TP relative to tab. Device may be measured by direct methods or by gauge.
7. Symbol LU applies between $L_1$ and $L_2$. Dimension LD applies between $L_2$ and LL minimum. Lead diameter shall not exceed .042 inch (1.07 mm) within $L_1$ and beyond LL minimum.
8. Lead designation, depending on device type, shall be as follows:

| Lead number | Bipolar transistor | FET |
|---|---|---|
| 1 | Emitter | Gate |
| 2 | Base | Source |
| 3 | Collector | Drain |
| 4 | Case | Case |

9. Lead number three is electrically connected to case.
10. Beyond r maximum, TW shall be held for a minimum length of .011 inch (0.28 mm).
11. Symbol r applied to both inside corners of tab.

FIGURE 10. Physical dimensions of T-3 family (Similar to TO-72) - Continued.

| Inches | mm | Inches | mm | Inches | mm |
|---|---|---|---|---|---|
| .038 | 0.97 | .135 | 3.43 | .440 | 11.18 |
| .043 | 1.09 | .151 | 3.84 | .495 | 12.57 |
| .048 | 1.22 | .188 | 4.78 | .500 | 12.70 |
| .050 | 1.27 | .205 | 5.21 | .525 | 13.34 |
| .053 | 1.35 | .225 | 5.72 | .875 | 22.22 |
| .058 | 1.47 | .250 | 6.35 | 1.177 | 29.90 |
| .060 | 1.52 | .312 | 7.92 | 1.197 | 30.40 |
| .063 | 1.60 | .360 | 9.14 | 1.51 | 38.4 |
| .131 | 3.33 | .420 | 10.67 | 1.65 | 41.9 |




NOTES: (for table on next page)
1. Dimensions are in inches.
2. Metric equivalents are given for general information only.
3. These dimensions should be measured at points .050 inch (1.27 mm) +.005 inch (0.13 mm) -.000 inch (0.00 mm) below seating plane. When gauge is not used, measurement will be made at the seating plane.
4. Two places.
5. The seating plane of the header shall be flat within .001 inch (0.03 mm) concave to .004 inch (0.10 mm) convex inside a .930 inch (23.62 mm) diameter circle on the center of the header and flat within .001 inch (0.03 mm) concave to .006 inch (0.15 mm) convex overall.
6. Lead diameter shall not exceed twice LD within $L_1$.
7. Lead designation, depending on device type, shall be as follows:

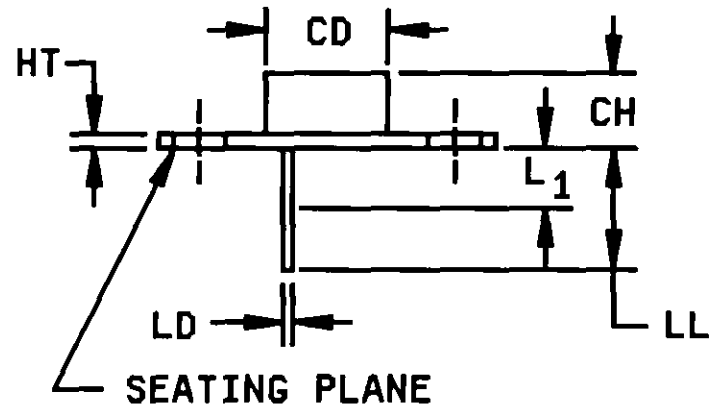
| Lead number | Bipolar transistor | FET |
|---|---|---|
| 1 | Emitter | Source |
| 2 | Base | Gate |
| Case | Collector | Drain |

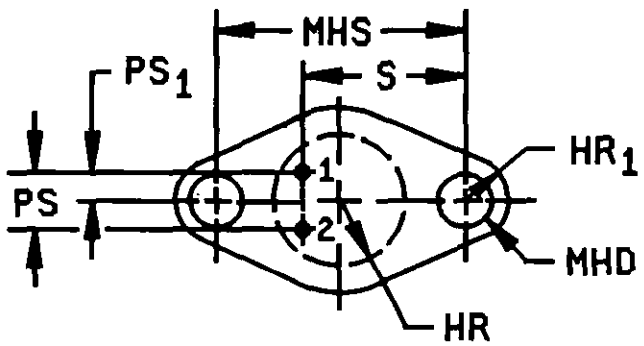
FIGURE 11. Physical dimensions of T-4 family. (Similar to TO-3)

| Symbol | T-4A | | T-4B | | T-4C | | Note |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| CD | | .875 | | .875 | | .875 | |
| CH | .250 | .360 | .250 | .360 | .250 | .360 | |
| HR | .495 | .525 | .495 | .525 | .495 | .525 | 4 |
| $HR_1$ | .131 | .188 | .131 | .188 | .131 | .188 | 4 |
| HT | .060 | .135 | .060 | .135 | .060 | .135 | |
| LD | .038 | .043 | .048 | .053 | .058 | .063 | 4, 6 |
| LL | .312 | .500 | .312 | .500 | .312 | .500 | |
| $L_1$ | | .050 | | .050 | | .050 | 6 |
| MHD | .151 | 1.65 | 1.51 | 1.65 | .151 | 1.65 | 4 |
| MHS | 1.177 | 1.197 | 1.177 | 1.197 | 1.177 | 1.197 | |
| PS | .420 | .440 | .420 | .440 | .420 | .440 | 3 |
| $PS_1$ | .205 | .225 | .205 | .225 | .205 | .225 | 3 |
| $S_1$ | .655 | .675 | .655 | .675 | .655 | .675 | |
| Notes | 1, 2, 5, 7 | | 1, 2, 5, 7 | | 1, 2, 5, 7 | | |

FIGURE 11. Physical dimensions of T-4 family (Similar to TO-3) - Continued.

| Symbol | T-5A | | Note |
|---|---|---|---|
| | Min | Max | |
| CD | | .620 | |
| CH | .250 | .340 | |
| HR | | .350 | 4 |
| HT | .050 | .075 | |
| $HR_1$ | .115 | .145 | 4 |
| LD | .028 | .034 | 4, 6 |
| LL | .360 | .500 | |
| $L_1$ | | .050 | 6 |
| MHD | .142 | .152 | 4 |
| MHS | .958 | .962 | |
| PS | .190 | .210 | 3 |
| PS1 | .093 | .107 | 3 |
| S | .570 | .590 | |
| Notes | 1, 2, 5, 7 | | |




| Inches | mm | Inches | mm |
|---|---|---|---|
| .028 | 0.71 | .250 | 6.35 |
| .034 | 0.86 | .340 | 8.64 |
| .050 | 1.27 | .350 | 8.89 |
| .075 | 1.91 | .360 | 9.14 |
| .093 | 2.36 | .470 | 11.94 |
| .107 | 2.72 | .500 | 12.70 |
| .115 | 2.92 | .570 | 14.48 |
| .142 | 3.61 | .590 | 14.99 |
| .145 | 3.68 | .620 | 15.75 |
| .152 | 3.86 | .958 | 24.33 |
| .190 | 4.83 | .962 | 24.43 |
| .210 | 5.33 | | |

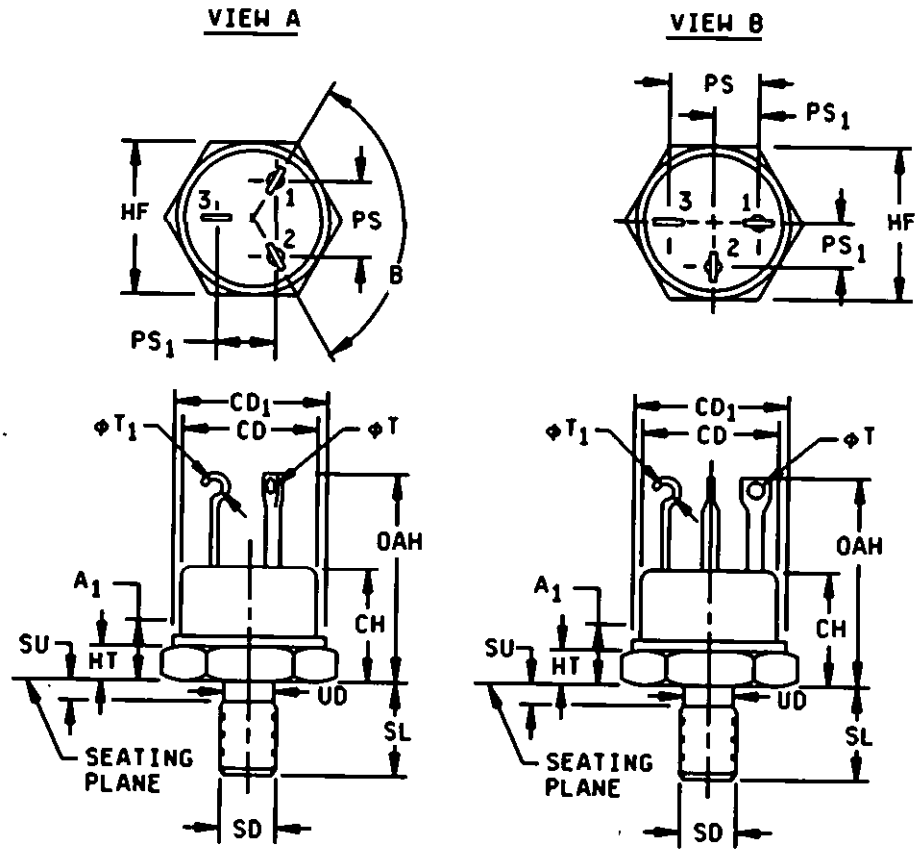
FIGURE 12. Physical dimensions of T-5 family. (Similar to TO-66)

*NOTES:*

1. Dimensions are in inches.
2. Metric equivalents are given for general information only.
3. These dimensions should be measured at points .050 inch (1.27 mm) +.005 inch (0.13 mm) -.000 inch (0.00 mm) below seating plane. When gauge is not used, measurement will be made at the seating plane.
4. Two places.
5. The seating plane of the header shall be flat within .001 inch (0.03 mm) concave to .004 inch (0.10 mm) convex inside a .930 inch (23.62 mm) diameter circle on the center of the header and flat within .001 inch (0.03 mm) concave to .006 inch (0.15 mm) convex overall.
6. Lead diameter shall not exceed twice LD within $L_1$.
7. Lead designation, depending on device type, shall be as follows:

| Lead number | Bipolar transistor | FET |
|---|---|---|
| 1 | Emitter | Source |
| 2 | Base | Gate |
| Case | Collector | Drain |

FIGURE 12. Physical dimensions of T-5 family (Similar to TO-66) - Continued.




| Inches | mm | Inches | mm | Inches | mm |
|---|---|---|---|---|---|
| .040 | 1.02 | .150 | 3.81 | .320 | 8.13 |
| .045 | 1.14 | .155 | 3.94 | .380 | 9.65 |
| .065 | 1.65 | .165 | 4.19 | .400 | 10.16 |
| .070 | 1.78 | .185 | 4.70 | .424 | 10.77 |
| .078 | 1.98 | .189 | 4.80 | .437 | 11.10 |
| .090 | 2.29 | .190 | 4.83 | .455 | 11.56 |
| .110 | 2.79 | .215 | 5.46 | .468 | 11.89 |
| .125 | 3.18 | .250 | 6.35 | .570 | 14.48 |
| | | .318 | 8.08 | .763 | 19.38 |

FIGURE 13. Physical dimensions of T-6 family. (Similar to TO-59)

| Symbol | T-6A | | T-6B | | T-6C | | Note |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| CD | .380 | .437 | .380 | .437 | .380 | .437 | 9 |
| $CD_1$ | .318 | .380 | .318 | .380 | .318 | .380 | |
| CH | .320 | .468 | .320 | .468 | .320 | .468 | |
| HF | .424 | .437 | .424 | .437 | .424 | .437 | |
| HT | .090 | .150 | .090 | .150 | .090 | .150 | |
| OAH | .570 | .763 | .570 | .763 | .570 | .763 | |
| PS | .185 | .215 | .185 | .215 | .125 | .165 | |
| $PS_1$ | .090 | .110 | .090 | .110 | .090 | .110 | |
| SD | .190-32 UNF-2A | | .190-32 UNF-2A | | .190-32 UNF-2A | | 6 |
| SL | .400 | .455 | .400 | .455 | .400 | .455 | |
| UD | .155 | .189 | .155 | .189 | .155 | .189 | |
| SU | | .078 | | .078 | | .078 | |
| $\phi T$ | .040 | .065 | .040 | .065 | .040 | .065 | |
| $\phi T_1$ | .045 | .070 | .045 | .070 | .045 | .070 | |
| $A_1$ | | .250 | | .250 | | .250 | |
| B | 120° Nom | | 90° Nom | | 120° Nom | | |
| Notes | 1, 2, 3, 4, 5, 7, 10, 11 | | 1, 2, 3, 4, 5, 8, 10 | | 1, 2, 3, 4, 5, 7, 10 | | |

FIGURE 13. Physical dimensions of T-6 family (Similar to TO-59) - Continued.

NOTES:
1. Dimensions are in inches.
2. Metric equivalents are given for general information only.
3. Terminal three may be flattened and pierced, or hook type.
4. Orientation of terminals in relation to hexagon is not controlled.
5. Chamfer or undercut on one or both ends of hexagon is optional.
6. Threads shall meet the requirements of FED-STD-H28.
7. View 'A' applicable.
8. View 'B' applicable.
9. Symbol $CD_1$ shall not exceed actual HF.
10. Lead designation, depending on device type, shall be as follows:

| Lead number | Bipolar transistor |
|---|---|
| 1 | Emitter |
| 2 | Base |
| 3 | Collector |

11. Lead number three is electrically connected to case.

FIGURE 13. Physical dimensions of T-6 family (Similar to TO-59) - Continued.

| Symbol | T-7A | | T-7B | | Note |
|---|---|---|---|---|---|
| | Min | Max | Min | Max | |
| CD | .610 | .687 | .610 | .687 | 8 |
| $CD_1$ | .570 | .610 | .570 | .610 | |
| CH | .325 | .460 | .325 | .460 | |
| HF | .667 | .687 | .667 | .687 | 7 |
| HT | .090 | .150 | .090 | .150 | |
| OAH | .640 | .875 | .640 | .875 | |
| PS | .340 | .415 | .340 | .415 | |
| $PS_1$ | .170 | .213 | .170 | .213 | |
| SD | .250-28 UNF-2A | | .250-28 UNF-2A | | 6 |
| SL | .422 | .455 | .422 | .455 | |
| SU | | .090 | | .090 | |
| $\phi T$ | .047 | .072 | .047 | .072 | |
| $\phi T_1$ | .046 | .077 | .046 | .077 | |
| UD | .220 | .249 | .220 | .249 | |
| $A_1$ | | .270 | | .270 | |
| Notes | 1, 2, 3, 4, 5, 9, 10 | | 1, 2, 3, 4, 5, 9, 10 | | 6 |

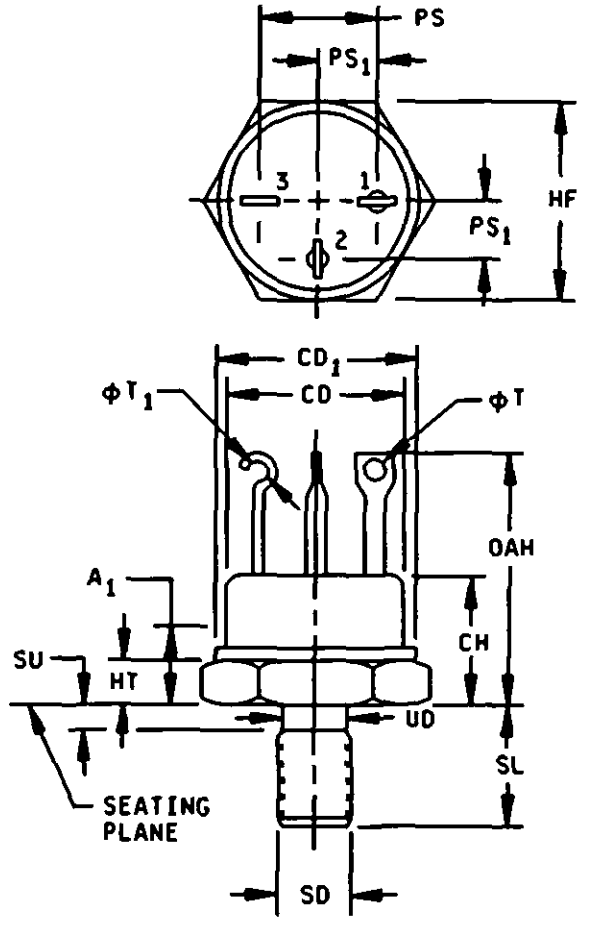



FIGURE 14. Physical dimensions of T-7 family. (Similar to TO-61)

| Inches | mm | Inches | mm |
|---|---|---|---|
| .046 | 1.17 | .325 | 8.26 |
| .047 | 1.19 | .340 | 8.64 |
| .072 | 1.83 | .415 | 10.54 |
| .077 | 1.96 | .422 | 10.72 |
| .090 | 2.29 | .455 | 11.56 |
| .150 | 3.81 | .460 | 11.68 |
| .170 | 4.32 | .570 | 14.48 |
| .213 | 5.41 | .610 | 15.49 |
| .220 | 5.59 | .640 | 16.26 |
| .249 | 6.32 | .667 | 16.94 |
| .250 | 6.35 | .687 | 17.45 |
| .270 | 6.86 | .875 | 22.23 |

NOTES:
1. Dimensions are in inches.
2. Metric equivalents are given for general information only.
3. Terminal three may be flattened and pierced or hook type.
4. Orientation of terminals in relation to hexagon is not controlled.
5. Chamfer or undercut on one or both ends of hexagon is optional.
6. Threads shall meet the requirements of FED-STD-H28.
7. Three places.
8. Symbol CD1 shall not exceed actual HF.
9. Lead designation, depending on device type, shall be as follows:

| Lead number | Bipolar transistor |
|---|---|
| 1 | Emitter |
| 2 | Base |
| 3 | Collector |

10. Lead number three is electrically connected to case.

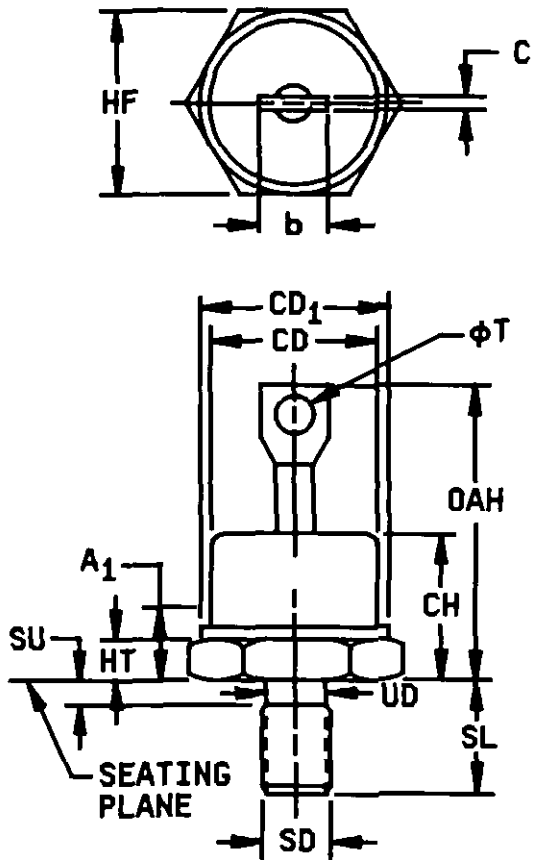
FIGURE 14. Physical dimensions of T-7 family (Similar to TO-61) - Continued.

APPENDIX F

| Outline number | Similar to JEDEC number | Figure number | Page number |
|---|---|---|---|
| D-1A (anode to stud) | DO-203AA(DO-4) | 15 | 125 |
| D-1B (cathode to stud) | DO-203AA(DO-4) | 15 | 125 |
| D-2A (anode to stud) | DO-203AB(DO-5) | 16 | 126 |
| D-2B (cathode to stud) | DO-203AB(DO-5) | 16 | 126 |
| D-3A (20 mil leads) | DO-204AA(DO-7) | 17 | 127 |
| D-3B (20 mil leads) | DO-204AB(DO-14) | 17 | 127 |
| D-3C (20 mil leads) | DO-204AA(DO-35) | 17 | 127 |
| D-3D (30 mil leads) | | 17 | 127 |
| D-3E (40 mil leads) | | 17 | 127 |
| D-4A | DO-205AA (DO-8) | 18 | 128-129 |
| D-4B | DO-205AB (DO-9) | 18 | 128-129 |
| D-4C | DO-205AC (DO-30) | 18 | 128-129 |
| D-4D | DO-205AD | 18 | 128-129 |
| TO-254 (40 mil diameter leads) | TO-254 | 19 | 130 |
| TO-257 (40 mil diameter leads) | TO-257 | 20 | 131 |
| TO-258 (60 mil diameter leads) | TO-258 | 21 | 132 |
| D-5A | Surface mount | 22 | 133 |
| D-5B | Surface mount | 22 | 133 |
| D-5C | Surface mount | 22 | 133 |
| D-5D | Surface mount | 22 | 133 |
| DO-213AA | Surface mount | 23 | 134 |
| DO-213AB | Surface mount | 23 | 134 |
| C-3 | Surface mount | 24 | 135 |
| C-4 | Surface mount | 25 | 136 |
| C-6 | Surface mount | 26 | 137 |

APPENDIX F

| Symbol | D-1A | | D-1B | | Note |
|---|---|---|---|---|---|
| | Min | Max | Min | Max | |
| CD | | .505 | | .505 | |
| $CD_1$ | .265 | .424 | .265 | .424 | 8 |
| CH | .300 | .405 | .300 | .405 | |
| HF | .424 | .437 | .424 | .437 | |
| HT | .075 | .175 | .075 | .175 | |
| OAH | .600 | .800 | .600 | .800 | |
| SD | .190-32 UNF-2A | | .190-32 UNF-2 | | 5 |
| SL | .422 | .453 | .422 | .453 | |
| SU | | .078 | | .078 | |
| UD | .163 | .189 | .163 | .189 | |
| ϕT | .060 | .103 | .060 | .103 | |
| $A_1$ | | .250 | | .250 | |
| b | | .250 | | .250 | |
| C | .018 | .065 | .018 | .065 | |
| Notes | 1,2,3,4,6 | | 1,2,3,4,7 | | |

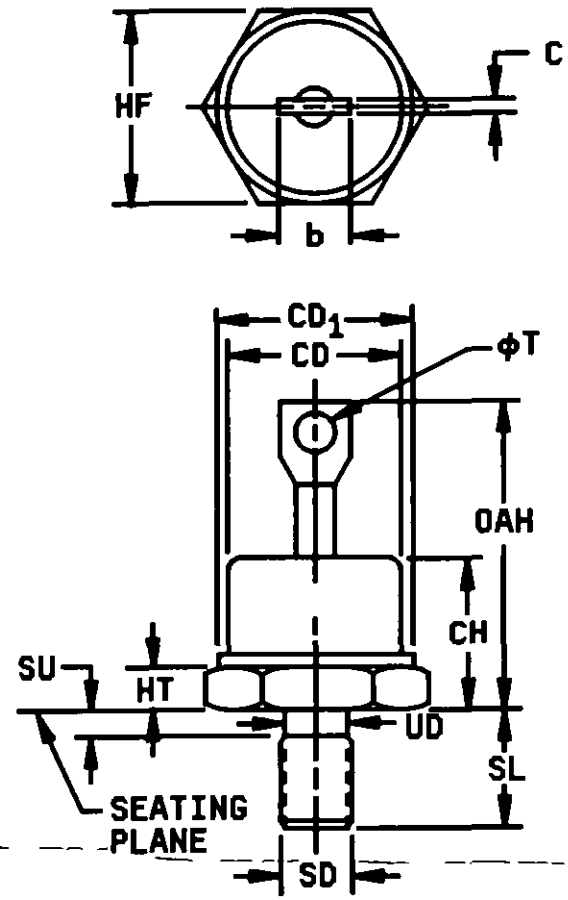



| Inches | mm | Inches | mm |
|---|---|---|---|
| .018 | 0.46 | .265 | 6.73 |
| .060 | 1.52 | .300 | 7.62 |
| .065 | 1.65 | .405 | 10.29 |
| .075 | 1.91 | .422 | 10.72 |
| .078 | 1.98 | .424 | 10.77 |
| .103 | 2.62 | .437 | 11.10 |
| .163 | 4.14 | .453 | 11.51 |
| .175 | 4.45 | .505 | 12.83 |
| .189 | 4.80 | .600 | 15.24 |
| .190 | 4.83 | .800 | 20.32 |
| .250 | 6.35 | | |

NOTES:
1. Dimensions are in inches.
2. Metric equivalents are given for general information only.
3. Orientation of terminals in relation to hexagon is not controlled.
4. Chamfer or undercut on one or both ends of hexagon is optional.
5. Threads shall meet the requirements of FED-STD-H28.
6. Anode shall be electrically connected to stud.
7. Cathode shall be electrically connected to stud.
8. $CD_1$ shall not exceed HF.

FIGURE 15. Physical dimensions of D-1 family. (Similar to DO-4)

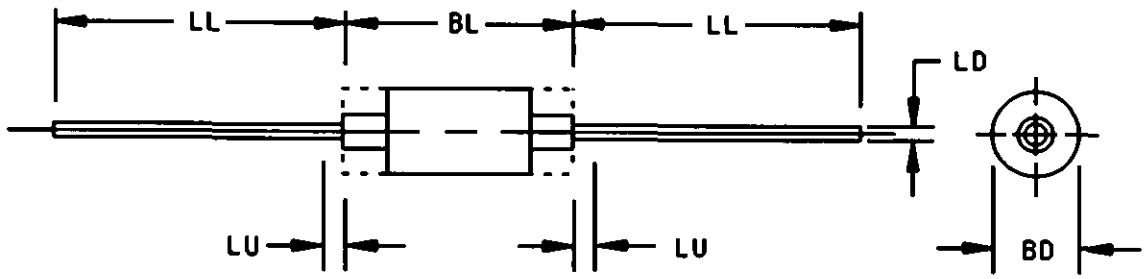
| Symbol | D-2A | | D-2B | | Note |
|---|---|---|---|---|---|
| | Min | Max | Min | Max | |
| CD | | .794 | | .794 | |
| $CD_1$ | | .667 | | .667 | 8 |
| CH | | .450 | | .450 | |
| HF | .667 | .687 | .667 | .687 | |
| OAH | .750 | 1.000 | .750 | 1.000 | |
| SD | .250-28 UNF-2A | | .250-28 UNF-2A | | 5 |
| SL | .422 | .453 | .422 | .453 | |
| SU | | .090 | | .090 | |
| UD | .220 | .249 | .220 | .249 | |
| b | .250 | .375 | .250 | .375 | |
| c | .030 | .080 | .030 | .080 | |
| HT | .115 | .200 | .115 | .200 | |
| ϕT | .140 | .175 | .140 | .175 | |
| Notes | 1, 2, 3, 4, 6 | | 1, 2, 3, 4, 7 | | |




| Inches | mm | Inches | mm |
|---|---|---|---|
| .030 | 0.76 | .375 | 9.53 |
| .080 | 2.03 | .422 | 10.72 |
| .090 | 2.29 | .450 | 11.43 |
| .115 | 2.92 | .453 | 11.51 |
| .140 | 3.56 | .667 | 16.94 |
| .175 | 4.45 | .687 | 17.45 |
| .200 | 5.08 | .750 | 19.05 |
| .220 | 5.59 | .794 | 20.17 |
| .249 | 6.32 | 1.000 | 25.40 |
| .250 | 6.35 | | |

NOTES:
1. Dimensions are in inches.
2. Metric equivalents are given for general information only.
3. Orientation of terminals in relation-to-hexagon is not controlled.
4. Chamfer or undercut on one or both ends of hexagon is optional.
5. Threads shall meet the requirements of FED-STD-H28.
6. Anode shall be electrically connected to stud.
7. Cathode shall be electrically connected to stud.
8. $CD_1$ shall not exceed HF.

FIGURE 16. Physical dimensions of D-2 family. (Similar to DO-5)

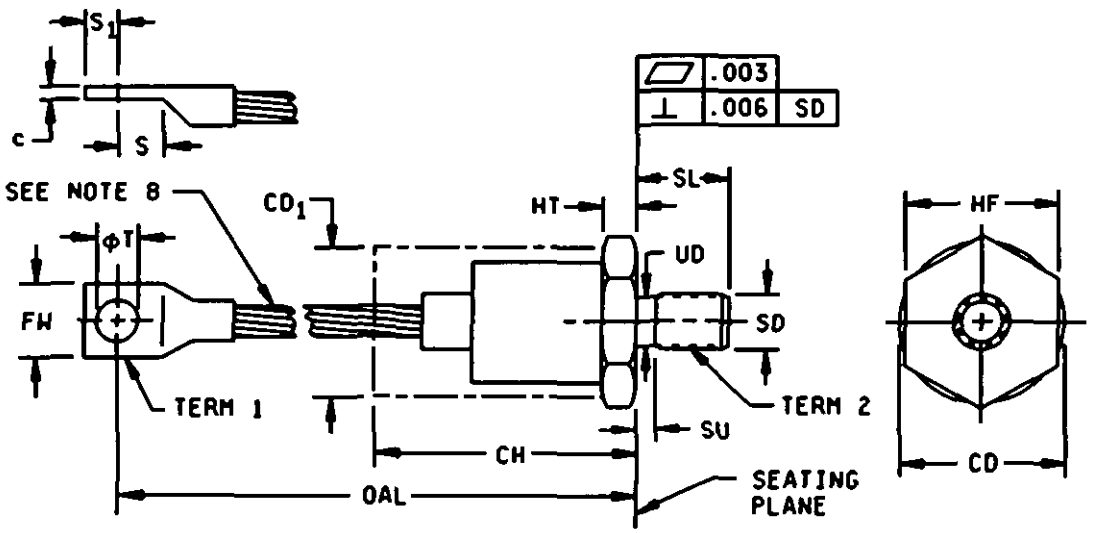



| Symbol | D-3A | | D-3B | | D-3C | | D-3D | | D-3E | | Note |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | |
| BD | .085 | .107 | .108 | .130 | .055 | .090 | .060 | .110 | .115 | .185 | 3 |
| BL | .230 | .300 | .230 | .300 | .120 | .200 | .125 | .215 | .130 | .195 | |
| LD | .018 | .022 | .018 | .022 | .018 | .022 | .027 | .032 | .036 | .042 | |
| LL | 1.000 | 1.500 | 1.000 | 1.500 | 1.000 | 1.500 | .800 | 1.300 | .900 | 1.300 | |
| LU | | .050 | | .050 | | .050 | | .050 | | .030 | 4 |
| Notes | 1, 2 | | 1, 2 | | 1, 2 | | 1, 2 | | 1, 2 | | |

| Inches | mm | Inches | mm | Inches | mm |
|---|---|---|---|---|---|
| .018 | 0.46 | .085 | 2.16 | .195 | 4.95 |
| .022 | 0.56 | .090 | 2.29 | .200 | 5.08 |
| .027 | 0.69 | .107 | 2.72 | .215 | 5.46 |
| .030 | 0.76 | .108 | 2.74 | .230 | 5.84 |
| .032 | 0.81 | .110 | 2.79 | .300 | 7.62 |
| .036 | 0.91 | .115 | 2.92 | .800 | 20.32 |
| .042 | 1.07 | .120 | 3.05 | .900 | 22.86 |
| .050 | 1.27 | .125 | 3.18 | 1.000 | 25.40 |
| .055 | 1.40 | .130 | 3.30 | 1.300 | 33.02 |
| .060 | 1.52 | .185 | 4.70 | 1.500 | 38.10 |

NOTES:
1. Dimensions are in inches.
2. Metric equivalents are given for general information only.
3. Symbol BD shall be measured at the largest diameter.
4. Within $L_1$ lead diameter may vary to allow for flash, lead finish build-up, and minor irregularities other than heat slugs.

FIGURE 17. Physical dimensions of D-3 family. (Similar to DO-7, DO-41, DO-35)




| Inches | mm | Inches | mm | Inches | mm | Inches | mm |
|---|---|---|---|---|---|---|---|
| .050 | 1.27 | .310 | 7.87 | .645 | 16.38 | 1.250 | 31.75 |
| .063 | 1.60 | .312 | 7.92 | .650 | 16.51 | 1.443 | 36.65 |
| .100 | 2.54 | .350 | 8.89 | .660 | 16.76 | 1.460 | 37.08 |
| .105 | 2.67 | .374 | 9.50 | .735 | 18.67 | 1.647 | 41.83 |
| .110 | 2.79 | .375 | 9.53 | .749 | 19.02 | 1.688 | 42.88 |
| .125 | 3.18 | .395 | 10.03 | .750 | 19.05 | 1.949 | 49.50 |
| .156 | 3.96 | .420 | 10.67 | .755 | 19.18 | 2.500 | 63.50 |
| .172 | 4.37 | .425 | 10.80 | .793 | 20.14 | 3.250 | 82.55 |
| .187 | 4.75 | .437 | 11.10 | .828 | 21.03 | 3.50 | 88.9 |
| .230 | 5.84 | .499 | 12.67 | 1.000 | 25.40 | 3.875 | 98.42 |
| .250 | 6.35 | .500 | 12.70 | 1.031 | 26.19 | 4.185 | 106.30 |
| .265 | 6.73 | .520 | 13.21 | 1.063 | 27.00 | 5.000 | 127.00 |
| .270 | 6.86 | .530 | 13.46 | 1.100 | 27.94 | 5.150 | 130.81 |
| .300 | 7.62 | .605 | 15.37 | 1.212 | 30.78 | 6.000 | 152.40 |
| | | .630 | 16.00 | 1.227 | 31.17 | 9.457 | 240.21 |
| | | | | | | 9.70 | 246.4 |

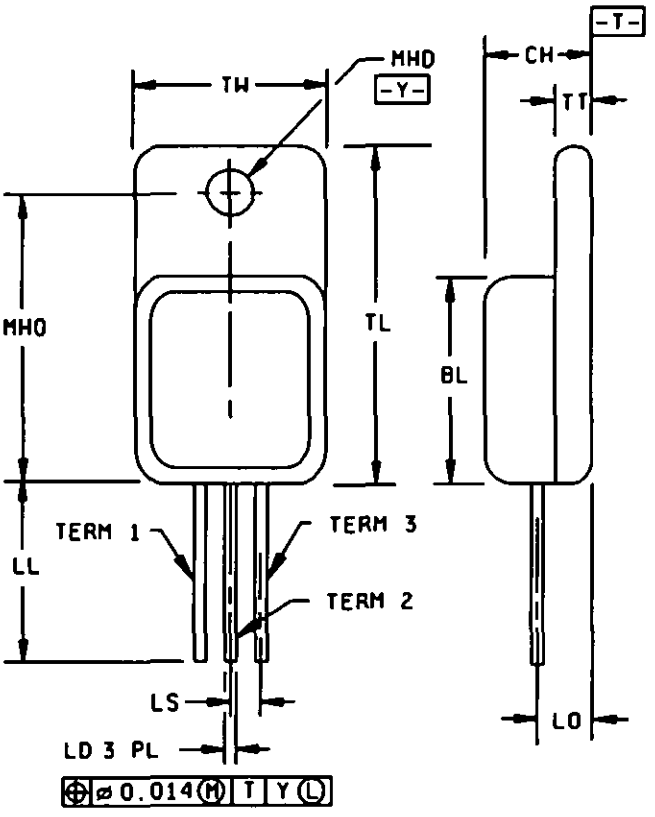
FIGURE 18. Physical dimensions of D-4 family. (Similar to DO-8)

| Symbol | Variations (all dimensions shown in inches) | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | D-4AA | | Note | D-4AB | | Note | D-4AC | | Note | D-4AD | | Note |
| | Min | Max | | Min | Max | | Min | Max | | Min | Max | |
| CH | | 2.500 | 4 | | 3.250 | 4 | | 2.500 | 4 | | 3.50 | 4 |
| FW | .437 | .650 | 7 | .530 | .755 | 5 | .437 | .650 | 7 | .735 | 1.000 | |
| HF | 1.031 | 1.063 | | 1.212 | 1.250 | | 1.031 | 1.063 | | 1.647 | 1.688 | |
| HT | .125 | .500 | 5 | .250 | .630 | 4 | .187 | .500 | 4 | | .630 | 5 |
| OAL | 3.875 | 5.150 | | 5.000 | 6.000 | | 4.185 | 5.150 | | 9.457 | 9.70 | |
| S | .300 | | 8 | .375 | | 8 | .312 | | 8 | .520 | | 8 |
| SD | .375-24 UNF-2A | | 9 | .750-16 UNF-2A | | 9 | .500-20 UNF-2A | | 9 | .750-16 UNF-2A | | |
| $S_1$ | .270 | | 8 | .300 | | 8 | .270 | | 8 | .300 | | 8 |
| SL | .605 | .645 | | .793 | .828 | | | .828 | | 1.00 | 1.100 | 4 |
| SU | | .105 | | | .156 | | .605 | .125 | | | .156 | |
| UD | .312 | .374 | | .660 | .749 | | .425 | .499 | | .660 | .750 | |
| c | .050 | .110 | | .063 | .172 | | .050 | .110 | | .100 | .230 | |
| CD | | 1.063 | 4 | | 1.250 | | | 1.063 | 4 | | 1.460 | |
| $CD_1$ | | 1.227 | | | 1.443 | | | 1.227 | | | 1.949 | |
| $\phi T$ | .250 | .310 | | .265 | .350 | | .250 | .310 | | .395 | .420 | |
| Note | 1, 2, 5, 7 | | | 1, 2, 5, 7 | | | 1, 2, 5, 7 | | | 1, 2, 5, 7 | | |

NOTES:
1. Dimensions are in inches.
2. Metric equivalents are for general information only.
3. Dimensioning and tolerancing in accordance with ANSI Y14.5M-1982.
4. The body of the device with the exception of the hexagon and flexible lead extensions lies within cylinder defined by $CD_1$ and CH, $CD_1$ not to exceed actual HF.
5. Chamfer or undercut on one or both ends of hexagonal base is optional.
6. Flexible lead.
7. Contour and orientation of terminal lug are optional. Square or radius on end of terminal is optional.
8. Minimum flat.
9. Symbol SD is pitch diameter of coated threads, reference: Unified screw threads, ANSI B1.1-1982.

FIGURE 18. Physical dimensions of D-4 family (Similar to DO-8) - Continued.

| Symbol | AA | |
|---|---|---|
| | Min | Max |
| BL | .535 | .545 |
| CH | .249 | .260 |
| LD | .035 | .045 |
| LL | 0.500 | 0.750 |
| LO | .150 BSC | |
| LS | .150 BSC | |
| MHD | .665 | .685 |
| MHO | .139 | .149 |
| TL | .790 | .800 |
| TT | .040 | .050 |
| TW | .535 | .545 |

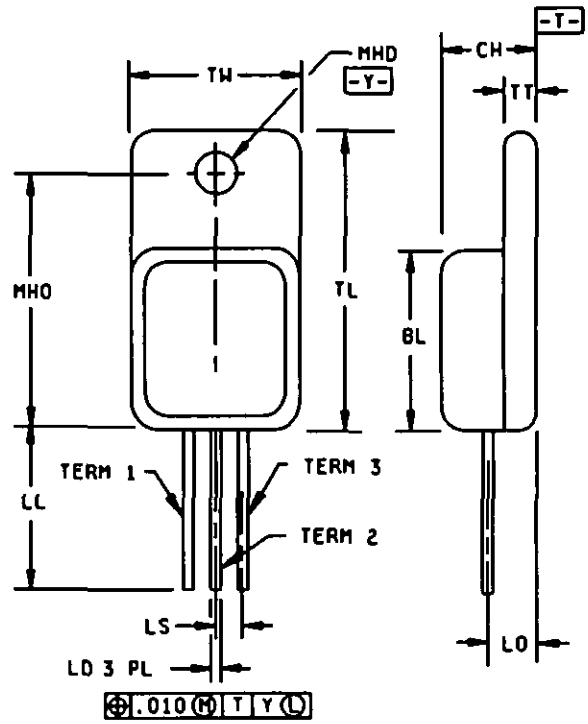



| Inches | mm | Inches | mm |
|---|---|---|---|
| .035 | 0.89 | .535 | 13.59 |
| .040 | 1.02 | .545 | 13.84 |
| .045 | 1.14 | .665 | 16.89 |
| .050 | 1.27 | .685 | 17.40 |
| .139 | 3.53 | .790 | 20.07 |
| .149 | 3.78 | .800 | 20.32 |
| .150 | 3.81 | 1.195 | 30.35 |
| .249 | 6.32 | 1.235 | 31.37 |
| .260 | 6.60 | | |

NOTES:
1. Dimensions are in inches.
2. Metric equivalents are given for general information only.
3. Refer to applicable symbol list.
4. Dimensioning and tolerancing in accordance with ANSI Y14.5M-1982.
5. Included in dimensions D and E.
6. Methods used for electrical isolation of the terminals feedthroughs shall employ materials that contain a minimum of 90 percent $AL_2O_3$ (ceramic).

FIGURE 19. Physical dimensions of TO-254.

| Symbol | AA | |
|---|---|---|
| | Min | Max |
| BL | .410 | .430 |
| CH | .190 | .200 |
| LD | .025 | .035 |
| LL | .500 | .750 |
| LS | .100 BSC | |
| MHD | .140 | .150 |
| MHO | .527 | .537 |
| TL | .645 | .665 |
| TT | .035 | .045 |
| TW | .410 | .420 |

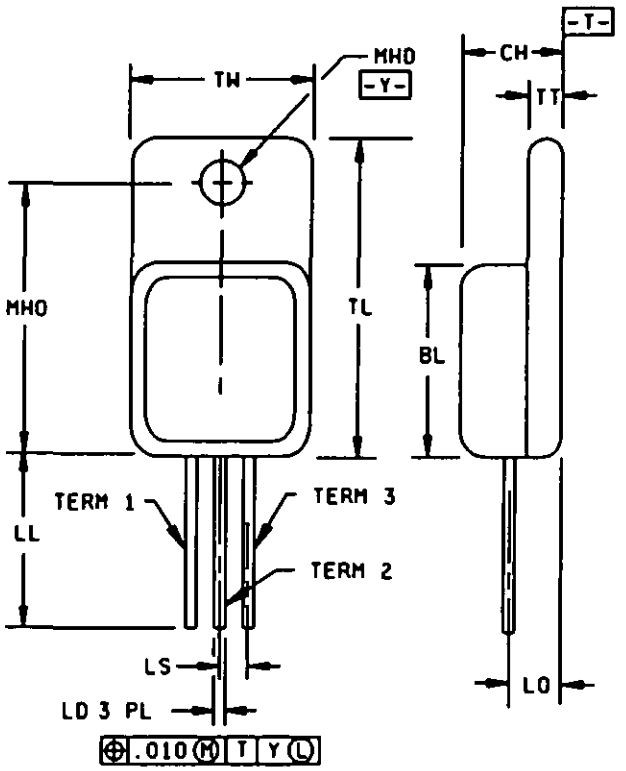



| Inches | mm | Inches | mm |
|---|---|---|---|
| .025 | 0.64 | .410 | 10.41 |
| .035 | 0.89 | .430 | 10.92 |
| .045 | 1.14 | .500 | 12.70 |
| .100 | 2.54 | .527 | 13.39 |
| .140 | 3.56 | .537 | 13.63 |
| .150 | 3.81 | .645 | 16.38 |
| .190 | 4.83 | .665 | 16.89 |
| .200 | 5.08 | .750 | 19.05 |

NOTES:
1. Dimensions are in inches.
2. Metric equivalents are given for general information only.
3. Methods used for electrical isolation of the terminals feedthroughs shall employ materials that contain a minimum of 90 percent $AL_2O_3$ (ceramic).

FIGURE 20. Physical dimensions of TO-257.

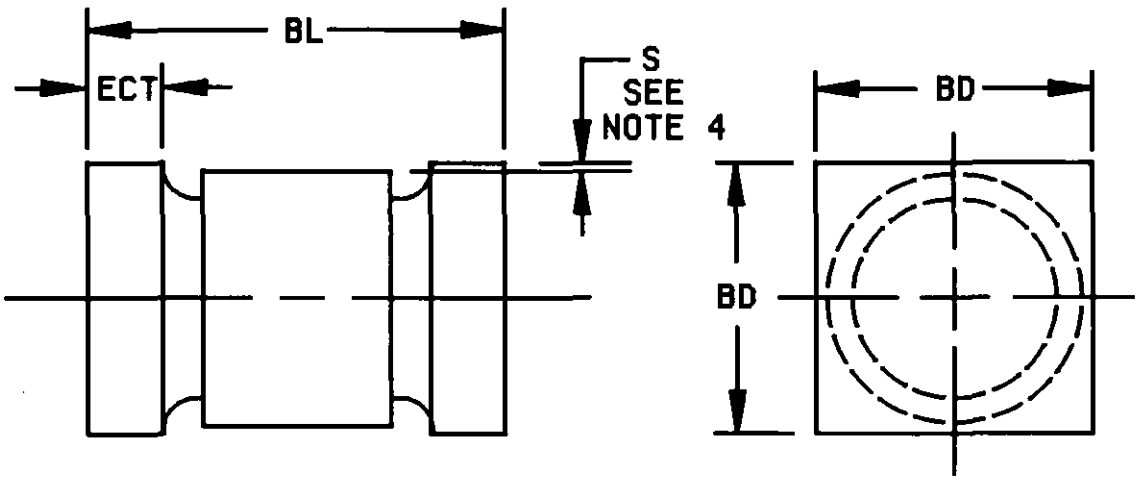
| Symbol | AA | |
|---|---|---|
| | Min | Max |
| BL | .530 | .550 |
| CH | .240 | .270 |
| LD | .055 | .065 |
| LL | .500 | .750 |
| LS | .200 BSC | |
| MHD | .155 | .165 |
| MHO | .697 | .707 |
| TL | .815 | .835 |
| TT | .035 | .045 |
| TW | .685 | .695 |




| Inches | mm | Inches | mm |
|---|---|---|---|
| .035 | 0.89 | .530 | 13.46 |
| .045 | 1.14 | .550 | 13.97 |
| .055 | 1.40 | .685 | 17.40 |
| .065 | 1.65 | .695 | 17.65 |
| .155 | 3.94 | .697 | 17.70 |
| .165 | 4.19 | .707 | 17.96 |
| .200 | 5.08 | .750 | 19.05 |
| .240 | 6.10 | .815 | 20.70 |
| .270 | 6.86 | .835 | 21.21 |
| .500 | 12.70 | | |

NOTES:
1. Dimensions are in inches.
2. Metric equivalents are given for general information only.
3. Included in dimension E and E.
4. Methods used for electrical isolation of the terminals feedthroughs shall employ materials that contain a minimum of 90 percent $AL_2O_3$ (ceramic).

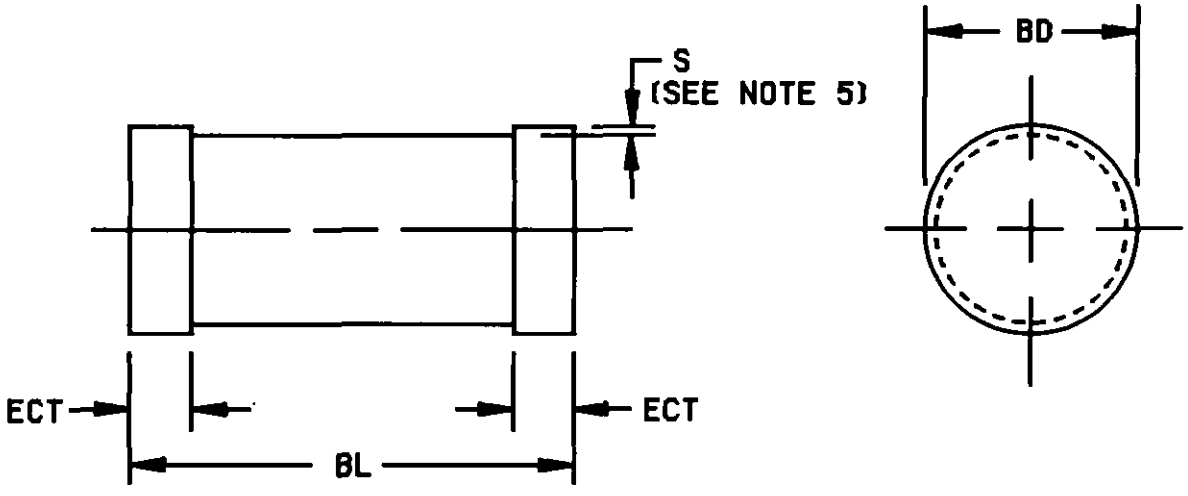
FIGURE 21. Physical dimensions of TO-258.




| Symbol | D-5A | | D-5B | | D-5C | | D-5D | |
|---|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | Min | Max |
| BL | .168 (4.27) | .200 (5.08) | .200 (5.08) | .225 (5.72) | .205 (5.21) | .245 (6.22) | .165 (4.19) | .195 (4.95) |
| BD | .091 (2.31) | .103 (2.62) | .137 (3.48) | .148 (3.76) | .183 (4.65) | .202 (5.13) | .070 (1.78) | .085 (2.16) |
| ECT | .019 (0.48) | .028 (0.71) | .019 (0.48) | .028 (0.71) | .019 (0.48) | .028 (0.71) | .019 (0.48) | .028 (0.71) |
| S | .003 (0.08) | | .003 (0.08) | | .003 (0.08) | | .003 (0.08) | |

NOTES:
1. Dimensions are in inches.
2. Metric equivalents are for general information only.
3. Dimensions are pre-solder dip.
4. Minimum clearance of glass body to mounting surface on all orientations.
5. Cathode marking to be either a color band or four dots spaced 90° apart.

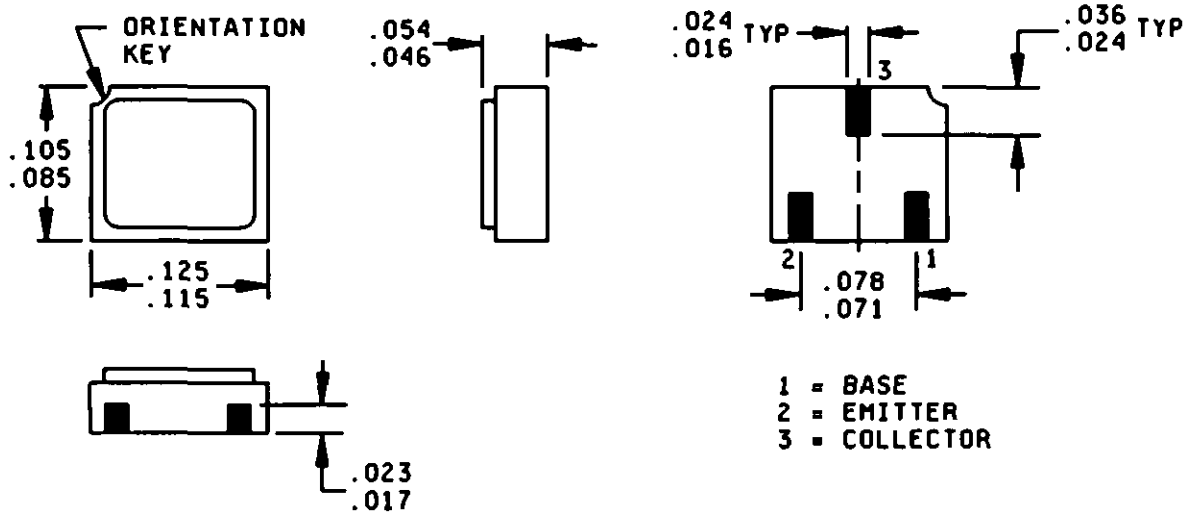
FIGURE 22. Physical dimensions of D5 surface mount family, square end surface mount.




| Symbol | Dimensions | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | DO-213AA | | | | DO-213AB | | | |
| | Inches | | Millimeters | | Inches | | Millimeters | |
| | Min | Max | Min | Max | Min | Max | Min | Max |
| BL | .130 | .146 | 3.30 | 3.70 | .189 | .205 | 4.80 | 5.20 |
| BD | .063 | .067 | 1.60 | 1.70 | .094 | .105 | 2.39 | 2.66 |
| ECT | .016 | .022 | 0.41 | 0.55 | .016 | .022 | 0.41 | 0.55 |
| S | .001 min | | 0.03 min | | .001 min | | 0.03 min | |

NOTES:
1. Dimensions are in inches.
2. Metric equivalents are given for general information only.
3. Dimensions are pre-solder dip.
4. Cathode marking to be either a color band or four dots spaced 90° apart.
5. Minimum clearance of glass body to mounting surface on all orientations.

FIGURE 23. Physical dimensions of DO-213 family, round end surface mount.

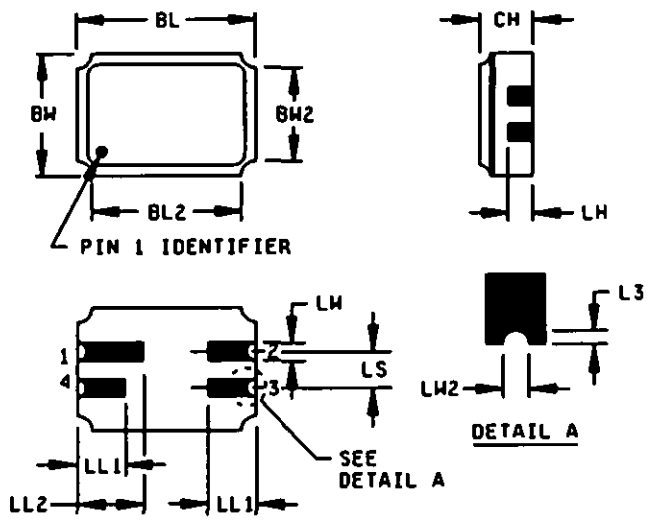



| Inches | mm | Inches | mm |
|---|---|---|---|
| .016 | 0.41 | .071 | 1.80 |
| .017 | 0.43 | .078 | 1.98 |
| .023 | 0.58 | .085 | 2.16 |
| .024 | 0.61 | .105 | 2.67 |
| .036 | 0.91 | .115 | 2.92 |
| .046 | 1.17 | .125 | 3.18 |
| .054 | 1.37 | | |

NOTES:
1. Dimensions are in inches.
2. Metric equivalents are given for general information only.

FIGURE 24. Physical dimensions, surface mount C-3.

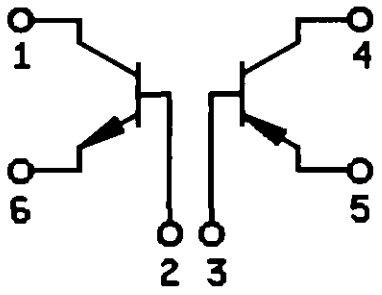
| Symbol | Dimensions | | | |
|---|---|---|---|---|
| | Inches | | Millimeters | |
| | Min | Max | Min | Max |
| BL | .215 | .225 | 5.46 | 5.71 |
| BL2 | | .225 | | 5.71 |
| BW | .145 | .155 | 3.68 | 3.93 |
| BW2 | | .155 | | 3.93 |
| CH | .061 | .075 | 1.55 | 1.90 |
| L3 | .003 | .007 | 0.08 | 0.18 |
| LH | .029 | .044 | 0.74 | 1.12 |
| LL1 | .032 | .048 | 0.81 | 1.22 |
| LL2 | .072 | .088 | 1.83 | 2.23 |
| LS | .045 | .055 | 1.14 | 1.39 |
| LW | .022 | .028 | 0.56 | 0.71 |
| LW2 | .006 | .022 | 0.15 | 0.56 |

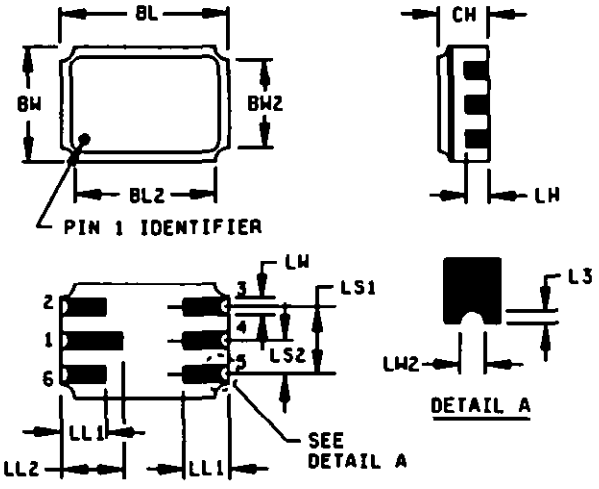



| Pin no. | Transistor | MOSFET | Optocoupler |
|---|---|---|---|
| 1 | Collector | Substrate | Collector |
| 2 | Emitter | Source | Cathode |
| 3 | Base | Gate | Anode |
| 4 | N/C | Drain | Emitter |

NOTES:
1. Dimensions are in inches.
2. Metric equivalents are given for general information only.
3. The coplanarity deviation of all terminal contact points, as defined by the device seating plane, shall not exceed .006 inch (0.15 mm) for solder dipped leadless chip carriers.

FIGURE 25. Physical dimensions of surface mount C-4.




| Symbol | Dimensions | | | |
|---|---|---|---|---|
| | Inches | | Millimeters | |
| | Min | Max | Min | Max |
| BL | .240 | .250 | 6.10 | 6.35 |
| BL2 | --- | .250 | --- | 6.35 |
| BW | .165 | .175 | 4.19 | 4.44 |
| BW2 | | .175 | | 4.44 |
| CH | .066 | .080 | 1.68 | 2.03 |
| L3 | .003 | .007 | 0.08 | 0.18 |
| LH | .026 | .034 | 0.66 | 0.86 |
| LL1 | .060 | .070 | 1.52 | 1.78 |
| LL2 | .082 | .098 | 2.08 | 2.49 |
| LS1 | .095 | .105 | 1.14 | 2.67 |
| LS2 | .045 | .055 | 1.14 | 1.39 |
| LW | .022 | .028 | 0.56 | 0.71 |
| LW2 | .006 | .022 | 0.15 | 0.56 |

| Pin no. | Transistor | MOSFET | Optocoupler |
|---|---|---|---|
| 1 | Collector no. 1 | Drain no. 1 | Anode |
| 2 | Base no. 1 | Gate no. 1 | N/C |
| 3 | Base no. 2 | Gate no. 2 | Collector |
| 4 | Collector no. 2 | Drain no. 2 | Base |
| 5 | Emitter no. 2 | Source no. 2 | Emitter |
| 6 | Emitter no. 1 | Source no. 1 | Cathode |

NOTES:
1. Dimensions are in inches.
2. Metric equivalents are given for general information only.
3. The coplanarity deviation of all terminal contact points, as defined by the device seating plane, shall not exceed .006 inch (0.15 mm) for solder dipped leadless chip carriers.

FIGURE 26. Physical dimensions of surface mount C-6.

APPENDIX G

CERTIFICATION REQUIREMENTS FOR RADIATION HARDNESS
ASSURED SEMICONDUCTOR DEVICES

10. Scope. Requirements for line certification of radiation hardness assured (RHA) semiconductor devices. This appendix is a mandatory part of the specification. The information contained herein is intended for compliance.

20. APPLICABLE DOCUMENT

20.1 Government documents. The following documents form a part of this appendix to the extent specified herein.

HANDBOOKS

MILITARY

| | | |
|---|---|---|
| MIL-HDBK-279 | - | Total Dose Hardness Assurance Guidelines for Semiconductor Devices. |
| MIL-HDBK-280 | - | Neutron Radiation Hardness Assurance Guidelines for Semiconductor Devices and Microcircuits. |

(Copies of the handbooks required by contractors in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

30. RADIATION HARDNESS PROGRAM

30.1 RHA program. The manufacturer shall establish, implement, and maintain a RHA assurance program. The program shall demonstrate and assure that design, manufacture, inspection, and testing of semiconductor devices are adequate to assure compliance with standard, reference documents, and the detail specification for RHA devices. If radiation testing is conducted outside of the manufacturer's facility, it shall be the responsibility of the manufacturer to assure that radiation testing and the associated documents follow the requirements specified herein.

The RHA tasks include but are not limited to:

a. Designation of a RHA manager or a project engineer.

b. Development of a RHA program plan.

c. Development of the RHA design, processing, assembly, testing, and inspection requirements.

d. Development of RHA records.

30.2 RHA management. The manufacturer shall identify a person or persons whose responsibility is to implement, control, and coordinate all activities associated with the manufacturing of RHA semiconductor devices.

30.3 RHA program plan. The manufacturer shall develop and document a RHA program plan for semiconductor devices which details the tasks to be performed and identifies responsibilities for assuring the tasks are carried out. The program plan shall contain, as a minimum these items:

a. Definition of the responsibilities of the RHA management.

b. Identification of RHA critical factors in design, layout, wafer processing, and assembly of the semiconductor devices.

c. Preparation of manufacturing flow charts showing electrical and radiation testing, quality verification points, and all the documents associated with RHA.

d. Preparation of detailed radiation test procedures to meet the specified RHA requirements.

e. RHA records to be maintained.

30.4 RHA design, processing, assembly, testing, and equipment instructions. Device design, processing, assembly, testing, and equipment related to RHA shall include the following items as applicable.

a. Critical layout rules.

b. Circuit design factors.

c. Critical processes.

d. Assembly, packaging, and handling critical to radiation hardness.

30.5 Change control, quality control, training, and calibration instructions for RHA. The manufacturer shall have in effect documented instructions covering as a minimum these areas:

a. Procedure for implementation and control of changes in device design, material, and processing which may affect hardness of the device and for making the information available to the certifying activity.

b. RHA quality control and quality assurance operations related to procedures, equipment, action criteria, records, and frequency of use.

c. Training and certification of personnel engaged in radiation testing.

d. The calibration and maintenance procedures of radiation facilities, dosimetry, and equipment used in radiation testing.

e. Traceability of radiation dosimetric devices to National Institute of Standards and Technology (NIST).

30.6 Radiation test procedure. The manufacturer shall document a detailed radiation test procedure which complies with the radiation requirements in accordance with group D of MIL-S-19500, and in accordance with associated detail specifications. Guidelines on radiation testing are provided in MIL-HDBK-279 and MIL-HDBK-280.

30.6.1 Ionizing radiation test procedure. Ionizing radiation test procedure shall be conducted in accordance with test method 1019 of MIL-STD-750. The procedure shall include:

a. Assembly of the dice using the same procedure of die attach, wire bonding, and packaging method specified for the certified line. Manufacturer shall have available procedures for qualifying each package type.

b. Conducting pre- and post-electrical test in accordance with the associated detailed specification using a certified test program.

c. The manufacturer shall maintain a table or graph showing a monthly correction for the Cobalt-60 source decay and the radiation time required to achieve the specified total dose at the device location. The calibration of the source should be traceable to the NIST.

30.6.2 Neutron irradiation test procedure. Neutron irradiation test procedure shall follow the requirements in test method 1017 of MIL-STD-750.

30.7 RHA records. The RHA records listed below shall be maintained and be submitted upon request for the review by the certification audit team. Those records shall be retained for a minimum of five years after performance of the inspection. As a minimum, the following records shall be maintained:

a. Records of radiation testing on wafer and wafer lot for JANS or inspection lot for JANTX and JANTXV. The records shall include the information on the test procedure and test results as specified in test methods 1017 and 1019 of MIL-STD-750.

b. Records of failed devices shall identify the device type, the wafer and the wafer lot for JANS or inspection lot for JANTX and JANTXV, and the disposition of the parts. The failed devices shall be data logged and this log shall be made available to the audit team.

c. The manufacturer shall document his RHA control procedure. As a minimum, group D for MIL-S-19500 post irradiation electrical parameter shall be read and recorded every six months on representative product from the certified line.

d. Records shall document the initial design, material, processing, and assembly and all changes affecting the hardness of the semiconductor device. Letters of approval by DESC to the above changes shall be maintained.

e. Records shall cover the scheduled calibration interval for each equipment item, the dates of completion of actual calibration and certification.

f. A traceability system shall be maintained such that RHA semiconductor devices can be traced to a specific wafer for JANS and inspection lot for JANTX and JANTXV, as applicable.

g. Records of personnel training.

30.8 Marking. The manufacturer shall show the procedure which assures that only those parts from the wafer for JANS, or from the inspection lot for JANTX and JANTXV which passed the specified radiation level, are marked by the corresponding RHA letter designator.

40 RADIATION HARDNESS ASSURANCE PART MANAGER PROGRAM

40.1 Radiation hardness assurance part manager (RHAPM). A certified company (e.g., original equipment manufacturer (OEM)) who establishes a relationship with a component manufacturer for the sole purpose of developing RHA semiconductors and has the responsibility to ensure compliancy of all manufacturing and testing procedures. The certified company shall be listed on the QPL as the manufacturer for the semiconductor device specified. The RHAPM is responsible for setting up a control system to ensure all requirements of the general and detailed device specifications are met.

40.1.1 Eligibility of participants. To be eligible to qualify a RHA part, a specification for the part must exist. Associated detail specifications are controlled and modified by DESC-ELDT. Participants shall be certified on the basis of a facilities survey.

40.1.1.1 Preparation of the detailed device specification. After the parts selection and prior to a third party agreement with a device manufacturer, the RHAPM must notify DESC-ELDT of his intent and request that a detailed device specification number be assigned. This can be accomplished in writing or by submitting to DESC through the Military Parts Control Advisory Group (MPCAG) on a DD Form 2052 Non-standard Parts Approval Request. In the justification section of this form the RHAPM will indicate a willingness to prepare the JAN detailed specification. After the applicable parts control procedures have been followed DESC-ELDT will assign a JAN detailed specification number or revision letter. The RHAPM will prepare the preliminary draft and submit it to DESC-ELDT. This preliminary draft does not have to be complete. It may have blank tables, figures, and it may be group D only, but it must be in the correct JAN detailed device specification format. A copy of this format is available from any of the technology representatives within DESC-ELDT (see figure 26).

40.1.1.2 Participants preparation for certification. All participants shall comply with the RHAPM management plan and all applicable requirements as specified in 3.4 and 40.3.1 herein. Qualification of RHA devices shall comply with the provisions in 4.5 herein. QCI shall comply with the provisions of 4.7 and 40.3.1 herein.

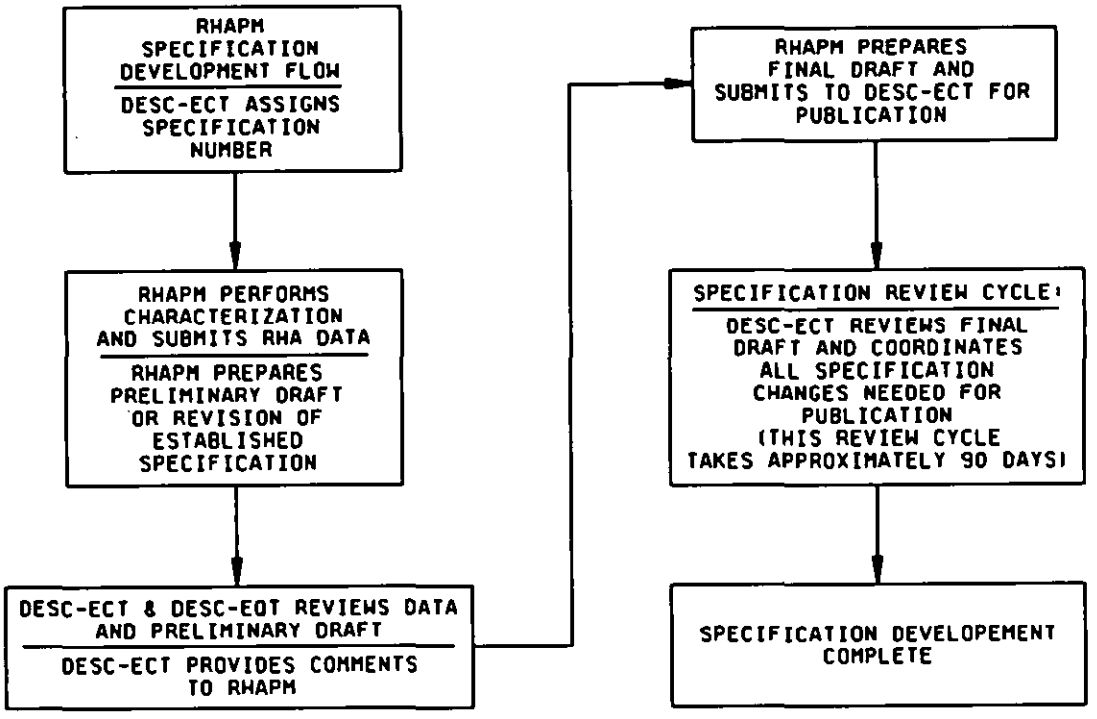



FIGURE 27. Specification development flow.

40.2 RHAPM product assurance requirements. The RHAPM product assurance program shall assure that the design, processing, assembly, inspection and testing of semiconductor devices comply with this specification and the applicable detailed specification. This program shall not require ownership of all manufacturing and testing facilities and establishes additional requirements for the sole purpose of developing a standard RHA product. As a minimum the RHAPM shall document the relationship as follows:

a. Individual responsibilities.

b. Product reliability.

c. Product quality.

d. Traceability.

e. Individual liability.

f. Data support.

g. Part marking.

h. Lot integrity of RHA product.

i. Testing (e.g., certified and qualified to MIL-S-19500).

A RHAPM must maintain an active working relationship with the device manufacturer, the Defense Electronics Supply Center (DESC), and the Systems Program Office (SPO). These relationships will constitute a partnership between the RHAPM, the device manufacturer, and the Government to insure the availability of high reliable standard RHA product to be used in more than one Department of Defense (DoD) system.

40.2.1 Management review. The RHAPM product assurance program shall be reviewed at appropriate intervals by responsible management to ensure RHA performance, product reliability, and the effectiveness of the established program. Records of management review shall be maintained covering the following minimum areas:

a. RHA design (when needed).

b. RHA baselines.

c. RHA characterization.

d. Process change control.

e. RHA testing (MIL-STD-750 test methods).

f. RHA Test laboratory suitability (ELST).

g. Development of detailed device specifications (ELDT).

40.2.2 Management plan. The management plan shall be established in accordance with 3.4.2 herein and submitted to the qualifying activity prior to a survey. It shall serve as a basis to demonstrate to the qualifying activity that the RHAPM has an understanding of a complete RHA product assurance program. As exemplified by its documentation system, is adequate to assure compliance of its product with the applicable specifications and quality standards. The management plan shall contain, as a minimum, these items and they shall be available for review at all sites:

a. Functional block diagrams.

b. Manufacturing flow charts by technology.

c. Examples of documentation as required by 40.2 herein.

d. Examples of records as required by 40.2 herein.

e. Examples of internal and device manufacturer audit activities.

f. Examples of ppm/spc monitoring.

40.3 Certification requirements. Only RHAPM certified companies may develop RHA products listed on part II of the QPL (QPL-19500).

40.3.1 RHAPM certification. Before an OEM can be considered as a RHAPM, he must demonstrate the capability to control and manage radiation hardened product. This can be accomplished through a pre-certification review and certification audit (see figure 27).

40.3.1.1 Pre-certification review. The pre-certification review of the OEM's management plan shall address the following:

a. The interface between the RHAPM and the third parties.

b. The availability of RHA product to other programs.

c. Methods for procurement, storage and delivery.

Upon completion of this review the OEM shall receive a authorization to pursue certification as a RHAPM. After receiving authorization the potential RHAPM has one year to establish a qualification plan and develop third party relationships with subcontractors.

40.3.1.2 RHAPM certification and laboratory suitability. After the third party relationships have been established the qualifications branch (DESC-ELST) must be notified and qualification milestones, certifications, and laboratory suitabilities, must be established. Laboratory suitability shall be obtained from DESC-ELS for all facilities designated to perform RHA characterization and QCI. A list of laboratories being used shall be submitted to DESC-ELS. It will be the responsibility of the RHAPM to insure each RHA test facility maintains suitability. The RHAPM will be responsible for the QCI. QCI shall be part of the RHA baseline and shall be performed as specified in the general and detailed specifications.

40.3.1.2.1 Characterization. The RHAPM must be responsible for the performance of all RHA characterization. This includes all known and testable radiation effects. As a minimum characterization shall include the following test methods:

a. Neutron Irradiation (MIL-STD-750, test method 1017).

b. Ionizing Radiation (MIL-STD-750, TOTAL DOSE test method 1019).

c. Dose Rate Burnout (MIL-STD-750, test method 3478).

d. Single Event Effects - Gate Rupture (JEDEC standard XXXX).

All characterization shall be to the device capability (not the system capability) under worst case conditions for the device technology and design. Data will be to functional failure or to a level of irradiation which best represents the product capability. From this data, endpoint electrical parameter limits shall be established. The detailed device specification shall represent these limits in the appropriate test tables.

40.3.1.2.2 Baselines. The RHAPM shall establish the RHA baseline and insure the device manufacturer maintains the manufacturing controls in accordance with this baseline. Any changes to the baseline must be coordinated through the RHAPM and reported to the qualifying activity (DESC-ELST).

40.3.1.2.3 QPL. In order to be listed as a source, on the QPL, the RHAPM must receive from DESC the following:

a. Certification: wafer fabrication, assembly, and test.

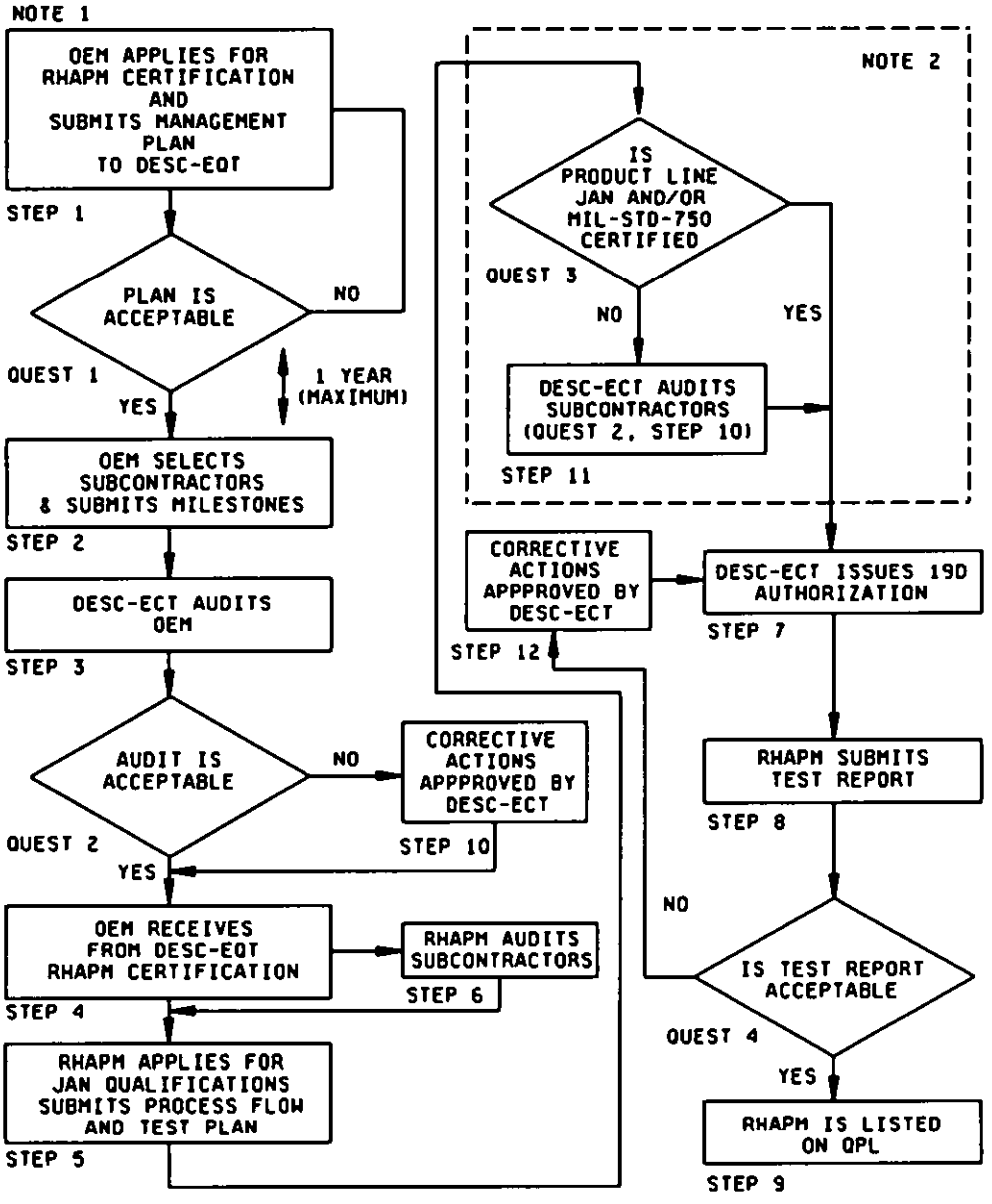
b. Suitability: test laboratories and radiation facilities.

40.3.1.3 Retention for RHAPM. This listing requires that the RHAPM shall maintain the following documentation:

a. Annual retention reports.

b. Self-audits.

c. Annual recertification/resuitability (class S).




NOTES:

1. The product development flow is as follows:

   Step 1. OEM applies for certification as a RHAPM. At this point DESC-ELST will request a management plan (see 40.2.2 herein) be formulated and presented to the certifying activity (DESC-ELST and DESC-ELDT).

FIGURE 28. Product development flow.

NOTES - Continued

Question 1. The certifying activity will review the management plan. When all problem areas have been resolved the OEM may be considered as a potential RHAPM. Upon acceptance of the management plan the potential RHAPM will have up to 1 year to accomplish step 2 herein.

Step 2. The potential RHAPM establishes relationships with subcontractors and submits a detailed outline of these relationships (see 40.1.1.2 herein) to the certifying activity for review. This outline must include qualification milestones.

Step 3. The certifying activity reviews potential RHAPM's product assurance program, management plan and verifies by auditing the potential RHAPM's procedures to insure compliance to MIL-S-19500 and all of appendix G.

Question 2. After reviewing all audit data the certifying activity will issue RHAPM certification. If there are any unresolved issues step 10 must be completed before certification can be issued.

Step 4. DESC-ELST issues RHAPM certification (see 40.3 herein). The RHAPM's management plan is implemented.

Step 5. Product line, RHA characterization, lab and device manufacturer are selected. The RHAPM is responsible for maintaining compliance to MIL-STD-750 and MIL-S-19500 by it's subcontractors. It is also the RHAPM's responsibility to insure that it's subcontractors procedures and documentation meet the baseline established within the RHAPM's management plan (see 40.2 and 40.3 herein).

Step 6. RHAPM will prepare preliminary draft specification for submission to DESC-ELDT. After the detailed device specification has been approved and dated the RHAPM applies for device qualification (see 40.1.1.1 and figure 26). This application must include a process flow and test report.

Question 3. Before a 19D authorization (step 7) can be issued all device fabrication and assembly must be JAN and/or MIL-STD-750 certified and all test facilities must have received suitability from DESC-ELS. If not Step 11 must be completed.

Step 7. DESC-ELST issued 19D authorization. This qualification test notification (DESC Form 19D) outlines the product to be tested, testing to be performed, sample sizes, and test locations.

Step 8. The qualification data test report is submitted to DESC-ELST for evaluation and review.

Question 4. If all qualification data is in accordance with MIL-S-19500, the detailed device specification, and the RHAPM's management plan QPL listing is authorized. If not Step 12 must be completed.

Step 9. The RHAPM is listed in the MIL-S-19500 QPL as the source of supply for the JAN RHA device.

Steps 10 and 12. If questions 2 and 4 are "NO", DESC-ELST will evaluate proposed corrective actions. These corrective actions must be implemented and approved before the next step can be accomplished.

Step 11. All subcontractors must be certified or have received from DESC-ELS laboratory suitability (see 40.3). If the answer to Question 3 is "NO", DESC-ELST must perform an audit of the facility in question. Any deficiencies requiring corrective action must be implemented and approved prior to granting manufacturer certification or laboratory suitability (see question 2 and step 10).

2. Question 3 may be answered at any time within the certification process, but if the answer is "NO" step 11, question 2 and step 10 must be accomplished before qualification testing can be authorized.

FIGURE 28. Product development flow - Continued.

APPENDIX H

DISCRETE SEMICONDUCTOR DIE/CHIP LOT ACCEPTANCE

10. SCOPE

10.1 Scope. The purpose of this appendix is to establish minimum standards for screening, qualification, and sample testing of JANHC and JANKC unencapsulated discrete semiconductor devices (die/chips) for use in military hybrids. Except for chips qualified under the provisions of 40.3.2, JANHC and JANKC qualification is only valid if the manufacturer maintains QPL status for the packaged device. In the event of conflict between this general specification and the associated detail specification, the detail specification shall govern. This appendix is a mandatory part of the specification. The information herein is intended for compliance.

20. APPLICABLE DOCUMENTS. This section is not applicable to this appendix.

30. DEFINITIONS

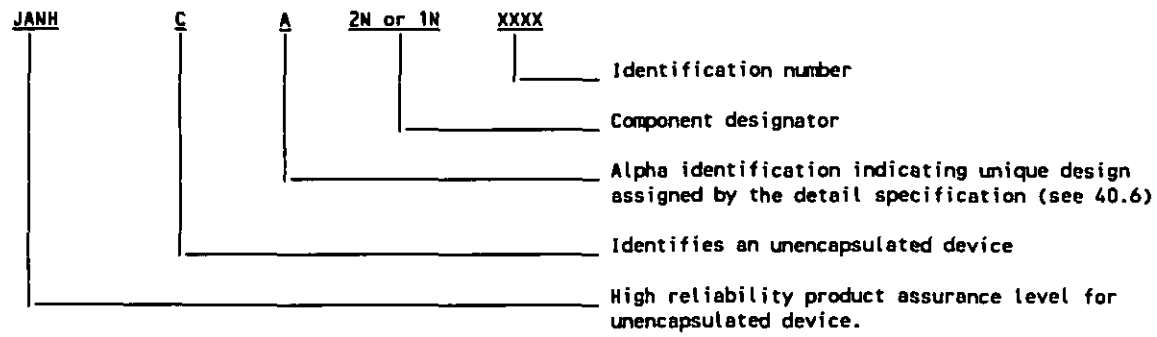
30.1 Definitions.

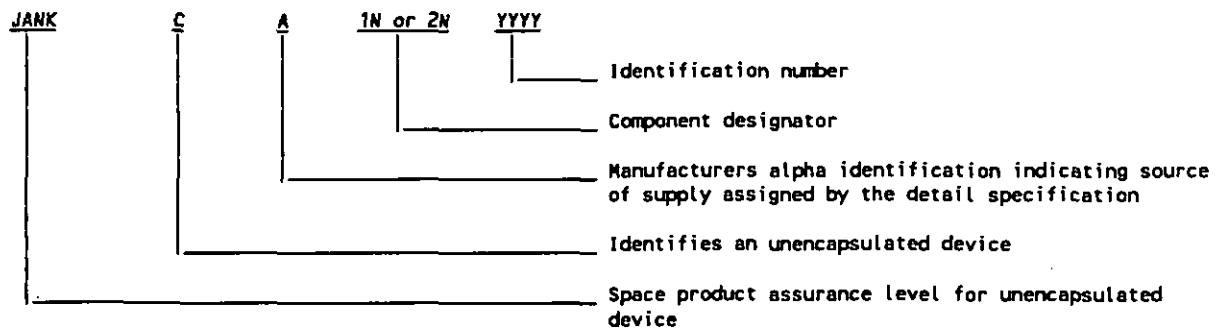
Date code: Seal week of the QCI packaged samples.

Die/chips: Unencapsulated discrete semiconductors. The term chip is interchangeable with the term die.

Manufacturer: Original wafer fabricator.

Identification: The designations JANHCA2NXXXX or JANKCA1NYYYY applies to die supplied to this specification.



APPENDIX H

Wafer lot: A wafer lot shall consist of only semiconductor wafers subjected to each and every process step of masking, etching, deposition, diffusion, metallization, etc. as a group. Each wafer lot shall be assigned a unique identifier which provides traceability to all wafer processing steps. If any portion of the lot is subjected to rework of masking, etching, deposition, diffusion, or related processes, that portion shall be re-identified with a different wafer lot number with identification maintained back to the original lot. Wafer lot records shall identify all JANHC and JANKC device inspection lots formed from the wafer lot.

Inspection lot: An inspection lot shall consist of all dice from a single wafer lot which are submitted for QCI at one time (see 4.2). The inspection lot may consist of a collection of sublots of different PINs. Only one QCI is required for each inspection lot, but each sublot must meet the requirements of table X, step 1 for JANHC and table XI, step 1 for JANKC.

40. REQUIREMENTS

40.1 General. Semiconductor die shall conform to the requirements contained herein.

40.2 Screening. Semiconductor die shall be 100 percent screened in accordance with 50.2 prior to qualification, QCI, and shipment.

40.3 Qualification. Qualification must be performed by the original wafer manufacturer. JANHC qualification will only be granted to a manufacturer who has a MIL-S-19500 qualified facility. JANKC qualifications will only be granted to a manufacturer who has been MIL-S-19500 qualified to manufacture JANS products.

40.3.1 Qualification requirements. Manufacturers who are on the QPL for a JANTX or higher level for a PIN will be granted qualification for the JANHC chip of the same PIN upon successful completion of QCI on the first lot of JANHC devices. Manufacturers who are on the QPL for the JANS packaged devices, will be granted qualification to the JANKC and JANHC of the same PIN upon completion of QCI on the first lot of JANKC devices.

40.3.2 Alternate qualification requirements. Manufacturers who are not on the QPL for the packaged device, but are JANS qualified, will be granted qualification of a JANHC or JANKC part when the requirements of 40.3.2a through 40.3.2f are met.

a. The manufacturer must have QPL on a device of similar function and technology. For the purpose of this specification, examples of functions are: signal transistor, zener diode, power transistor, darlington, transient suppressor, or their identifiable circuit function. The term technology will include: DMOS, VMOS, diffused junction, alloy junction, JFET, and all other pertinent technological descriptions of the device design.

b. Qualification testing for JANHC shall consist of QCI testing in accordance with table X and periodic testing as required by 50.3.5 and table XII.

c. Qualification testing for JANKC shall consist of QCI testing in accordance with table XI and table XII.

d. Sample devices to be tested for qualification under this option will be assembled in packages which are thermally equivalent to the device package shown on the applicable detail specification.

* e. The dices are manufactured on JANS qualified wafer fab line.

f. Manufacturers seeking qualification under this option shall submit Form 360 showing the die/package combination which is proposed for qualification and QCI testing and data substantiating compliance with the requirements of 40.3.2a and 40.3.2d above.

40.4 Quality assurance provisions. QCI shall be performed on each inspection lot subsequent to qualification.

40.4.1 JANHC and JANKC assembly. When a portion of a wafer lot intended for JANHC is assembled, tested, and accepted through QCI as JANTX or higher devices, the remainder of the wafer lot shall be qualified for JANHC without further QCI testing. When a portion of a wafer lot intended for JANKC is assembled, tested, and accepted through QCI as JANS devices, the remainder of the wafer lot shall be qualified for JANKC without further QCI testing. This applies only if the following conditions are met: All PDA requirements of table II, step 11, and step 13a were met on the first submission; the group A sample plan of subgroups 2, 3, and 4 passed on the first submission; the JANC die is identical to the packaged die in all respects; and the assembled lot contains only dice from the JANHC or JANKC intended wafer lot. While awaiting the results of the assembled QCI lot, the remaining portion of the wafer lot intended for JANHC or JANKC shall be stored in accordance with 50.4.

40.4.2 Alternate flow. When no dice from JANHC or JANKC inspection lot are assembled as JAN branded packaged devices, devices, or the JANHC and JANKC dice are configured differently from the dice in the JAN branded packaged devices (e.g., different metallization), then QCI of the JANHC and JANKC inspection lot in accordance with 50.3 is required.

40.4.3 JANHC multiple sublots. When the JANHC die lot is divided into multiple sublots which differ only in the metallization schemes, samples from all sublots must conform to step 1 of table X and 50.3.2 through 50.3.4 herein. Conformance to the requirements of 50.3 herein may be demonstrated with a sample from a single sublot.

40.5 Performance characteristics. The electrical performance characteristics of semiconductor die shall be as specified in the associated detail specification.

40.6 Design and construction. The design, construction, and physical dimensions of the semiconductor die shall be in accordance with the requirements of MIL-S-19500 and with 40.6.1 through 40.6.3 and shall be identical to the qualified die except that metallization may be varied to suit various bonding and die attach methods. A completed form 360 and die topography, including dimensions, pad locations, and metallization descriptions (die map)shall be submitted to the qualifying activity prior to qualification. A unique design identifier as part of the PIN shall be assigned based on any of the following differences:

a. Die size, height, width, and length.

b. Bond pad size.

c. Bond pad location.

d. Bond pad metal.

e. Backside metal.

40.6.1 Bonding pad. The bonding pad size, location, and electrical function shall be in accordance with the applicable associated detail specification. The minimum bond pad dimensions shall be 3 mils unless approved by the qualifying activity.

40.6.1.1 Metallization integrity. The bonding pads shall be metallized and suitable for bonding as specified in the associated detail specification and shall meet the requirements of 50.3.2.

40.6.2 Backing material. The backing material shall be as described in the associated detail specification, and meet the requirements of 50.3.4.

40.6.3 Glassivation. Glassivation requirements of 3.6.6 of MIL-S-19500 apply.

APPENDIX H

50. QUALITY ASSURANCE PROVISIONS

50.1 General. The screening and QCI (see 40.2 and 40.4) of semiconductor die shall be performed at a qualified domestic facility.

50.1.1 Responsibility for inspection. The supplier shall be responsible for the performance of all inspection requirements as specified herein and in the associated detail specification.

50.1.2 Retention of records. The supplier shall maintain adequate records of all examinations, inspections, and tests accomplished in accordance with the requirements specified herein and in the associated detail specification. Records, including variables data, shall be retained in accordance with 4.9 of MIL-S-19500.

50.2 Screening. The die/chip screening shall be performed prior to QCI of 50.3 and shall consist of the following.

50.2.1 Electrical probe test. Probe tests shall be performed on 100 percent of the semiconductor die. Test limits and conditions shall be chosen by the supplier to demonstrate that there is compliance with all the electrical characteristics specified by the associated detail specification. This allows the supplier to assign test values or test details which differ from the associated detail specification requirements.

50.2.2 Visual inspection. All QCI samples shall be visually inspected in die form prior to submittal for assembly of the quality conformance testing samples. The remainder of the inspection lot shall be 100 percent visually inspected at any time prior to shipment. All visual inspections shall be performed in accordance with the applicable methods specified in MIL-STD-750.

50.2.3 JANKC wafer lot inspection. For JANKC, wafer lot inspection requirements of 4.3.1.2.2 of MIL-S-19500 shall apply.

50.3 Quality conformance inspection.

TABLE X. Electrical sampling for JANHC.

| Step | Inspection | Associated detail specification reference | Sample plan |
|---|---|---|---|
| 1. | Electrical tests 1/ 2/ | Group A, subgroups 2, 3, 4, and 7 | n = 10, c = 0 |
| 2. | Burn-in | Step 12 of JANTX screening table | |
| 3. | End-points 2/ | Group A, subgroup 2 | n = 10, c = 0 |

1/ MIL-S-19500, group A table. Group A test conditions and limits shall be as specified in the associated detail specification.
2/ Data from steps 1 and 3 shall be read and recorded.

TABLE XI. Electrical sampling for JANKC.

| Step | Inspection | Associated detail specification reference (JANS) | Sample plan |
|---|---|---|---|
| 1. | Electrical tests 1/ 3/ | Group A, subgroups 2, 3, 4, 5, 6, and 7 | n = 10, c = 0 |
| 2. | HTRB | Step 10 of screening table | |
| 3. | DC test 2/ 3/ | Step 11 of screening table | n = 10, c = 0 |
| 4. | Burn-in | Step 12 of screening table | |
| 5. | End-points and delta 2/ 3/ calculation | Step 13 of screening table | n = 10, c = 0 |

1/ MIL-S-19500, group A table. Group A test conditions and limits shall be as specified in the associated detail specification.
2/ Deltas shall be required when specified in the screening table of the applicable associated detail specification.
3/ Data steps 1, 3, and 5 shall be read and recorded.

TABLE XII. Periodic tests and continuation of JANKC QCI.

| Step | Inspection | Associated detail specification reference | Sample plan |
|---|---|---|---|
| 1-1 | Temperature cycling | Group B, subgroup 3 (S level) | |
| 1-2 | Surge | Group B, subgroup 3 (S level) | |
| 1-3 | Electrical measurements | Group A, subgroups 2, 3, 4, and 7 | n = 10, c = 0 |
| 2 | Thermal resistance | Group B, subgroup 6 | n = 10, c = 0 |
| 3-1 | Operating life 1/ | Step 12 of screening table. (S level) t = 1,000 hours | n = 10, c = 0 |
| 3-2 | Electrical measurements at 1,000 hours | Step 13 of screening table. (S level) 2/ | n = 10, c = 0 |

1/ Devices from step 4 of table X may be continued to 1,000 hours to fulfill this requirement.
2/ Omit $Z_{\theta JX}$.

TABLE XIII. Storage life verification tests. 1/

| Inspection |
|---|
| a. Electrical tests at +25°C, group A, subgroup 2, n = 10, c = 0 |
| b. Bond pull (see 50.3.2) 1/ n = 10, c = 0 |
| c. Die shear (see 50.3.4) 1/ n = 5, c = 0 |

1/ Separate samples may be used for steps b and c.

If the devices pass the above criteria, then the lot has passed the storage life verification tests.

* 50.3.1 Packaged sample tests. A random sample shall be selected from each inspection lot. The manufacturer may, at his option, perform evaluation of the wafer lot prior to submitting for QCI. The evaluation samples may not be used for any QCI requirements or test. For JANKC, at least 2 die from each wafer and at least 10 die from each wafer lot shall be selected, to build the packaged samples.

50.3.1.1 Pre-cap visual. A pre-cap visual inspection in accordance with the applicable methods specified in MIL-STD-750 shall be performed to remove assembly induced defects.

50.3.1.2 Packaged sample identification. The packaged sample shall be marked or labeled in accordance with the following priority:

a. Serial numbers, if required for delta measurement unit identification.

b. Device PIN.

c. Inspection lot number or date code.

50.3.1.3 Sample acceptance. The specified sample size shall be processed through the test sequence specified in table X for JANHC and tables XI and XII for JANKC. If the test sample fails the criteria of the applicable table, the lot shall be rejected. If a failure is attributed to packaging or handling defects, ESD, equipment malfunction, or operator error, these samples shall be verified by visual inspection or failure analysis. Upon verification of such defects, the test sample may be replaced in accordance with 4.4.2 of MIL-S-19500. In addition, all quality conformance inspections lots must complete the tests of 50.3.2 through 50.3.4.

50.3.2 Bond pull. Wire bond pull shall be performed according to MIL-STD-750, method 2037, condition A. Wire bond samples must have been baked to any of the conditions listed in table XIV. Five devices minimum with 10 wires shall be tested with zero rejects allowed. If one reject is found, resubmittal is allowed using 10 devices minimum and 20 wires with zero rejects. Failures which are not related to the integrity of the die do not constitute failure of the lot and such failures may be replaced with additional packaged devices and resubmitted for bond pull after verification. It is permissible, but not required, to use *devices from tables X and XI.*

* 50.3.3 Temperature cycling. Temperature cycling shall be performed in accordance with MIL-STD-750, method 1051, condition C. Sample size shall be 10 pieces. Failure criteria shall be group A, subgroup 2, with zero rejects allowed. If one reject is found, resubmittal is allowed using double the sample size with zero rejects. Failures which are not related to the integrity of the die do not constitute failure of the lot and such failures may be replaced with additional packaged devices and resubmitted for temperature cycling after verification. It is permissible, but not required, to use devices from table X or table XI.

* 50.3.4 Die shear. Die shear shall be performed in accordance with MIL-STD-750, method 2017, condition A. Five samples that have completed table X or table XI (unless the test is for table XIII verification testing) and temperature cycling, shall be tested with zero rejects. If one reject is found, resubmittal is allowed using 10 devices with zero rejects. Assembly related failures which are not related to the integrity of the die do not constitute failure of the lot and such failures may be replaced with additional packaged devices and resubmitted for die shear after verification.

50.3.5 Chip qualification. Chips qualified under the optional procedure of 40.3.2 must successfully complete the periodic testing shown in table XII as required by 4.7.6 of MIL-S-19500. For the purpose of this appendix, the requirement stating that the devices be fully marked shall be waived and the requirements of 50.3.1.2 herein shall apply.

50.3.5.1 Periodic testing. All devices tested to table XII requirements shall have passed step 1 of table X. Devices which have been subjected to table X or table XI testing can be used for table XII testing.

50.3.5.2 Separate samples. Separate samples may be used for test groupings 1-1 through 1-3, 2, and 3-1 through 3-2 in table XII. Samples for each test group must be tested sequentially within the group.

50.4 Storage. Prior to acceptance, dice shall be stored in a dry nitrogen atmosphere. After lot acceptance, the inspection lot die may be stored in dry nitrogen or other inert atmosphere. When storage time exceeds 36 months after QCI completion, a sample shall be assembled and tested as specified in table XIII. The manufacturer may submit an alternate procedure for storage of semiconductor die for approval by the qualifying agency.

60. PACKAGING

60.1 Packaging. All semiconductor die shall be packaged in individually lidded containers. For ESD sensitive devices (classes I and II) conductive or anti-static containers shall be required with an external conductive field shielding barrier. Stacking of containers without lids shall not be allowed. The supplier may submit an alternate procedure for packaging of die for approval by the using activity. Protective packaging of ESD shall be mandatory.

60.2 Container marking. The following information shall be marked on each container of semiconductor die:

a. Type designation.

b. Applicable detail specification number.

c. Manufacturer's logo or designation symbol.

d. Lot identification code.

e. Quantity.

f. ESD symbol, in accordance with 3.7.3.1 of MIL-S-19500 herein.

g. Date code.

h. Verification date code (see 60.2.1).

60.2.1 Date code for verification. Lots that had storage life verification tests in accordance with table XIII shall have a second date code identifying the date of the verification tests. This date code will be followed by the suffix letter V (identifying verification).

60.3 Certificate of conformance. The certificate of conformance shall be in accordance with 3.3.1 of MIL-S-19500.

TABLE XIV. Age-time and temperature.

| Condition | Minimal time | Temperature 1/ |
|---|---|---|
| A | 1 hour | 300°C |
| B | 2.5 hours | 275°C |
| C | 8 hours | 250°C |
| D | 25 hours | 225°C |
| E | 90 hours | 200°C |
| F | 400 hours | 175°C |

1/ +10°C, -5°C.

APPENDIX H

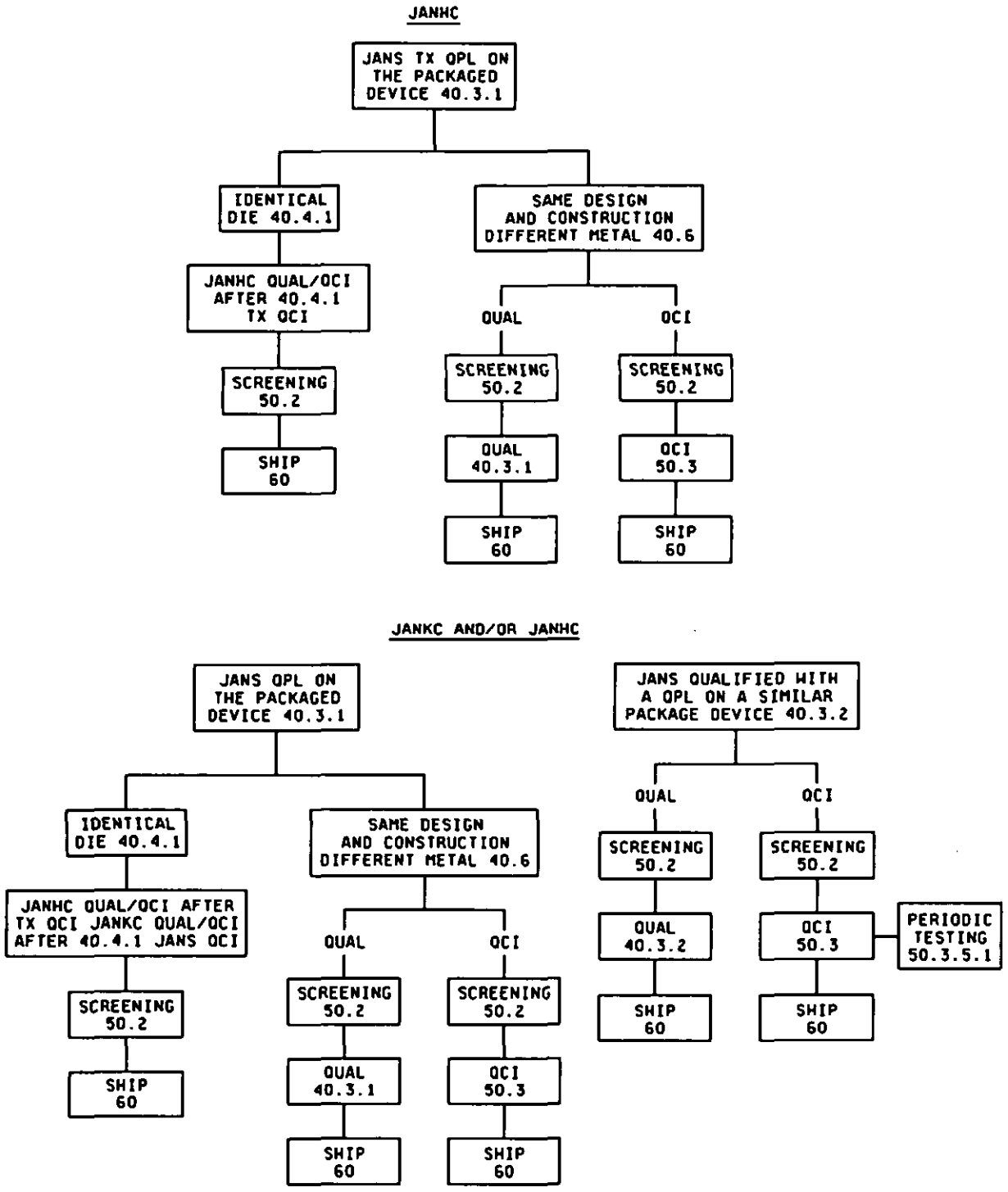



FIGURE 29. MIL-S-19500 appendix H flowchart.

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CONCLUDING MATERIAL

Custodians:
Army - ER
Navy - EC
Air Force - 17
NASA - NA
International interest (see 6.6)

Review activities:
Army - AR, MI, SM
Navy - AS, MC, CG
Air Force - 13, 19, 85, 99
DLA - ES

Preparing activity:
Navy - EC

Agent:
DLA - ES

(Project 5961-1438)

# STANDARDIZATION DOCUMENT IMPROVEMENT PROPOSAL

**INSTRUCTIONS**

1. The preparing activity must complete blocks 1, 2, 3, and 8. In block 1, both the document number and revision letter should be given.
2. The submitter of this form must complete blocks 4, 5, 6, and 7.
3. The preparing activity must provide a reply within 30 days from receipt of the form.

NOTE: This form may not be used to request copies of documents, nor to request waivers, or clarification of requirements on current contracts. Comments submitted on this form do not constitute or imply authorization to waive any portion of the referenced document(s) or to amend contractual requirements.

| I RECOMMEND A CHANGE: | 1. DOCUMENT NUMBER<br>MIL-S-19500J | 2. DOCUMENT DATE (YYMMDD)<br>94-04-15 |
|---|---|---|

3. DOCUMENT TITLE
SEMICONDUCTOR DEVICES, GENERAL SPECIFICATION FOR

4. NATURE OF CHANGE (Identify paragraph number and include proposed rewrite, if possible. Attach extra sheets as needed.)

5. REASON FOR RECOMMENDATION

6. SUBMITTER

| a. NAME (Last, First, Middle Initial) | b. ORGANIZATION | |
|---|---|---|
| c. ADDRESS (Include Zip Code) | d. TELEPHONE (Include Area Code)<br>(1) Commercial<br>(2) AUTOVON<br>(If applicable) | 7. DATE SUBMITTED<br>(YYMMDD) |

8. PREPARING ACTIVITY

| a. NAME Alan Barone | b. TELEPHONE (Include Area Code)<br>(1) Commercial: 513-296-6048<br>(2) AUTOVON: 986-6048 |
|---|---|
| c. ADDRESS (Include Zip Code)<br>Defense Electronics Supply Center<br>Attn: DESC-ELDT<br>Dayton, Ohio 45444-5765 | IF YOU DO NOT RECEIVE A REPLY WITHIN 45 DAYS, CONTACT:<br>Defense Quality and Standardization Office<br>5203 Leesburg Pike, Suite 1403, Falls Church, VA 22041-3466<br>Telephone (703) 756-2340 AUTOVON 289-2340 |