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SUPERSEDING
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12 August 1971

MILITARY SPECIFICATION

DATA ANALYSIS PROGRAMMING GROUP

AN/AYA-8B

This specification has been approved by the
Naval Air Systems Command, Department of the Navy

1. SCOPE

1.1 Scope - The equipment * covered by this specification shall allow communication between Computer C P-901/ASQ-114 and the computer driven peripheral equipments.

1.2 Classification - The equipment covered by this specification shall consist of the following items:

Type Designation	Applicable Paragraph
Data Amlysis Logic Unit MX-8023A/AYA-8 (Logic Unit 1)	3.5.1
Data Analysis Logic Unit MX-8024A/AYA-8 (Logic Unit 2)	3.5.2
Data Analysis Logic Unit MX-8034/AYA-8 (Logic Unit 3)	3.5.3
Data Analysis Logic Unit MX-9360/AYA-8B (Logic Unit 4)	3.5.4
Control-Indicator C-7627(P)/AYA-8 (Universal Keyset) (3 per system)	3.5.5
Control-Indicator C-7629/AYA-8 (Pilot's Keyset)	3.5.5
Control-Indicator C-7628/AYA-8 (Ordnance Panel)	3.5.5
Electrical Test Panel SB-3152/AYA-8 (Armament/Ordnance Test Panel)	3.5.5

1.3 Associated Equipment - This equipment shall operate with the associated equipment listed in 6.7. Magnetic Tape Transport RD-319A/AYA-8 is identified as a part of Data Analysis Programming Group AN/AYA-8B but is supplied separately and is covered by a separate specification. Therefore it is treated as an associated equipment and listed in 6.7.

* Data Analysis Programming Group AN/AYA-8B is commonly referred to as Data Processing System or DPS.

2. APPLICABLE DOCUMENTS

2.1 General. - The following documents form a part of this specification to the extent specified herein. Listed are the issues of the documents in effect for the previous procurement. However, in lieu of the issue listed, the contractor shall use the latest issue in effect of these documents where feasible. If the use of the latest issue will affect design performance, or interchangeability of any replaceable part, then the issue of the document listed below shall be used.

SPECIFICATIONS

Military

MIL-C-3608A 22 March 1969	Connectors, Coaxial Radio Frequency Series BNC and Associated Fittings, General Specification for Use
MIL-E-5400H 1 June 1965	Electronic Equipment, Aircraft, General Specifications for
MIL-T-5422E 15 Nov 1961	Testing, Environmental, Aircraft Electronic Equipment
MIL-F-5591B 19 Nov 1963	Fasteners, Panel
MIL-I-6181D 25 Nov 1959	Interference Control Requirements, Aircraft Equipment
MIL-C-6781B 13 Sept 1960	Control Panel, Aircraft Equipment, Racker Console Mounted
MIL-M-7793C 14 Aug 1961	Meter, Time Totalizing
MIL-E-17555F 5 Mar 1965	Electronic and Electrical Equipment and Associated Repair Parts, Preparation for Delivery of
MIL-T-18303A 1 May 1963	Test Procedures: Preproduction and Inspection, for Aircraft Electronic Equipment, Format for
MIL-N-18307C 1 Oct 1958	Nomenclature and Nameplates for Aeronautical Electronic and Associated Equipment
MIL-S-19500D 11 May 1964	Semiconductor Devices, General Specification for
MIL-P-23377A 30 Sept 1964	Primer Coating; Epoxy-Polyamide, Chemical and Solvent Resistant
MIL-F-25173A 23 Nov 1959	Fasteners, Control Panel, Aircraft Equipment
MIL-C-26482D 10 May 1966	Connector, Electric, Circular, Miniature, Quick Disconnect
MIL-C-81511 15 Mar 1967	Connectors, Electrical, Circular, High Density, Quick Disconnect, Environment Resisting, General Specifications for

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AR-34 26 Mar 1969	Failure Classification for Reliability Testing, General Requirements for
WR-101 Part I -28 Feb 1966 Part II -3 Mar 1966	Weapon Requirements for Advanced ASW Electronic Systems Part I - Electromagnetic Control Requirements for Advanced ASW Avionics Systems Part II - Selection and Testing of Microelectronic Circuits for Advanced ASW Avionic Systems
WS-8506 15 Dec 1966	Requirements for Digital Computer Program Documentation

STANDARDS

Military

MIL-STD-454C 15 Oct 1970	Standard General Requirements for Electronic Equipment
MIL-STD-470 21 Mar 1966	Maintainability Program Requirements (for Systems and Equipment)
MIL-STD-471 15 Feb 1966	Maintainability Demonstration
MIL-STD-701E 30 Dec 1964	Preferred and Guidance List of Semiconductor Devices
MIL-STD-704A 9 August 1966	Electric Power, Aircraft Characteristics and Utilization of
MIL-STD-781A 10 Dec 1965	Reliability Tests, Exponential Distribution
MIL-STD-785 30 June 1965	Requirements for Reliability Program (for System and Equipment)
MIL-STD-794 10 Mar 1965	Parts and Equipment, Procedures for Packaging and Packing of
MS-17322C	Meter, Time Totalizing, 115Volt -400 Cycle
MS-25212C 25 Aug 1960	Control Panel, Console Type, Aircraft Equipment, Basic Dimensions
MS-25213A 25 Aug 1960	Control Panel, Aircraft Equipment, Typical Installation
FED-STD-595 1 Mar 1956	Color

Naval Air Systems Command

EI-515A	Avionics Installation Instructions for Data Analysis Programming Group AN/AYA-8B

2.1.1 Availability of Documents -When requesting specifications, standards, drawings, and publications, refer to both title and number. Copies of this specification and applicable specifications required by contractors in connection with specific procurement functions may be obtained upon application to the Commanding Officer, Publications and Forms Center (NPFC 1032), Code 105, 5801 Tabor Avenue, Philadelphia, Pennsylvania 19120.

3. REQUIREMENTS

3.1 Preproduction - The specification makes provision for preproduction testing.

3.2 Parts and Materials - In the selection of parts and materials, fulfillment of major design objectives shall be the prime consideration. In so doing the following shall govern:

(1) Microelectronic devices shall conform to requirements specified in WR-101, Part II.

(2) Other parts and materials requirements shall conform to Specification MIL-E-5400.

(3) Nonrepairable subassemblies, as outlined in Specification MIL-E-5400, shall be used when practicable. The general size of the subassembly and the amount of circuitry to be included therein shall be approved by the procuring activity. Nonrepairable subassemblies must be reliable.

(4) When previously produced models of this equipment did not use repairable subassemblies, the design shall not be changed to employ nonrepairable assemblies without the approval of the procuring activity.

3.2.1 Nonstandard Parts and Materials Approval - Approval for the use of nonstandard parts and materials (including electron tubes, transistors and diodes) other than microelectronic devices shall be obtained as outlined in Specification MIL-E-5400. Microelectronic devices shall be approved as outlined in WR-101, Part II, Amendment 1.

3.2.2 Electron Devices - Transistors and diodes shall be chosen and applied as outlined in Specification MIL-S-19500 and MIL-STD-701.

3.2.3 Maintenance Modules - The electronic portions of the equipment shall be divided into maintenance modules as defined in 3.3.7.2.1.

3.3 Design and Construction - The equipment shall conform with all the applicable requirement specification MIL-E-5400 for design, construction and workmanship, except as otherwise specified herrein

*3.3.1 Total Weight - The total weight of the DPS equipment shall be minimum consistent with good design and shall not exceed 776 pounds.

3.3.2 Reliability

3.3.2.1 Reliability Program - The contractor shall establish and conduct a reliability program in accordance with MIL-STD-785.

3.3.2.2 Operational Stability - The equipment shall operate with satisfactory performance for the life of the equipment without the necessity for readjustment of any control, which are inaccessible to the operator during normal use.

3.3.2.3 Operating Life - The equipment shall have a total operating life of 50,000 hours with reasonable servicing and replacement of parts. Parts requiring scheduled replacement and the replacement interval shall be specified by the contractor.

3.3.2.4 Specified Mean-Time-Between-Failures (MTBF) - The specified Mean-Time-Between-Failures (MTBF) for tiheb respective units of Data Analysis Programming Group AN/AYA-8B when tested and accepted as outlined under the requirements of 4.4.3 shall be as follows:

Logic Unit 1	800 hours
Logic Unit 2	800 hours
Logic Unit 3	800 hours
Logic Unit 4	600 hours **
Universal Keyset	110 hours
Pilot's Keyset	440 hours
Ordnance Panel	270 hours
Armament/Ordnance Test Panel	930 hours

**(The Drum subassembly of the Magnetic Drum Memory requiring depot maintenance shall have an MTBF of 1500 hours or greater.)

3.3.2,5 Time Totalizing Meter - The equipment shall contain time totalizing meters in accordance with Specification MIL-M-7793. A time totalizing meter type MS-17322-6A shall be included in each separate item, except panels and keysets. Logic Unit 4 shall have two meters. In Logic Unit 4 a separate meter shall be supplied for the Magnetic Drum Memory subassembly of the Drum Auxillary Memory Subunit.

3. 3.3 Cablimg and Connections

3.3.3.1 Cables - The equipment shall provide for the use of cables in accordance with specification WR- 101, Part 1.

3.3.3.2 Interconnection Cabling - The equipment shall be capable of satisfactory operation using external wiring in accordance with the applicable requirements of Specification WR-101 Part 1, except as modified herein, and the detailed requirements of EI-515. External cables and that portion of the connectors attached to the cables shall not be supplied as part of the equipment.

3.3.3.2.1 Twisted Pair Cable - Twisted pair cable shall be in accordance with EI-515. In twisted pair transmission neither lead shall be grounded on the receiving end.

3.3.3.2.2 Triaxial Cable - All triaxial cable shall be Amphenol 421-033 or equivalent in accordance with EI-515. In triaxial signal transmissions the inner shield shall be grounded on the transmitting end only.

3.3.3 .2.3 Single Wire Cable - In signal wire transmissions the reference lead supplied by the signal source shall not be grounded on the receiving end.

3.3.3 .2.4 Number of Wires per Terminal - Attachment of wires and leads shall be in accordance with Requirement 5 of MIL-STD-454 except that the number of wires per terminal shall be limited only to the extent that no wires shall be wrapped on another wire.

3.3.3.3 Connectors - The equipment shall use external connectors in accordance with the requirements of Installation Instructions EI-515. Triaxial connectors shall be hermetically sealed triaxial BNC type receptacles conforming to the requirements outlined in paragraph 3 of MIL-C-3608 except that the part shall have an additional contact between the inner and outer contact. Protective locking caps in accordance with 3.4.6 of MIL-C-81511 will not be required.

3.3.4 Control Panels - All rack or console mounted control panels shall conform to the applicable requirements of Specification MIL-C-6781 except that edge-lighting shall not be required. The configuration of all control panels must be approved by the procuring activity prior to preproduction testing.

3.3.5 Interchangeability - The equipment shall meet the interchangeability requirements of Specification MIL-E-5400.

3.3.6 Interference Control - The equipment shall conform with all of the requirements of WR-101, Part I for design, construction and workmanship, except as specified herein. A Control Plan will be prepared in accordance with WR-101, Part I.

3.3.7 Maintainability

3.3.7.1 Maintainability Program - The contractor shall establish and conduct a maintainability program in accordance with MIL-STD-470 and MIL-STD-471 Method 2. All maintenance actions shall be capable of being performed by a technician with a comprehensive ability level as follows:

(1) Civilian Education - High school graduate or equivalent.

(2) Technical Training - Navy, Class A technicians school appropriate to the maintenance task

(3) Experience - Two (2) years of technical experience in addition to technical training.

3.3.7.2 Maintainability Definitions - The following definitions shall apply to the terminology as used in this specification.

3.3.7.2.1 Maintenance Module - A maintenance module shall be defined as the least complex segment of each part of the DPS which is capable of being removed and reinserted within the DPS through the use of a connector or captive mounting bolts/screws rather than by soldering (brazing) or welding.

3.3.7.2.1.1 Maintenance Module Requirements

(1) A module shall be packaged in such form that it can be plugged into and removed from its subunit (functional group of maintenance modules) or assembly without the use of special tools.

(2) A maximum of 46 different modules shall be used in Logic Units 1, 2, 3 and 4, exclusive of their power supplies and the Magnetic Drum Memory Subassembly.

3.3.7.2.2 Subunit - A subunit is a functional group of maintenance modules. Each subunit containing its associated maintenance modules shall be either a single plug-in, removable assembly, or due to size or packaging limitations, a number of plug-in, removable assemblies.

3.3.7.2.3 Subunit Types - The types of subunits shall be as specified herein.

3.3.7.3 Maintainability Requirements

3.3.7.3.1 Maintainability Philosophy - To provide for increased system effectiveness, maintainability y shall receive equal considerate ion with such factors as cost, physical parameters, and reliability. The maintenance philosophy for avionics equipment is that of fault isolation to and repair by replacement of individual modules without removing the units from the operational environment in the aircraft. Where feasible, fault isolation shall be computer initiated utilizing a diagnostic program. Where not feasible, equipments shall provide self-test features and readily accessible test points to accommodate standard test equipment affording fault isolation to the individual replaceable module.

3.3.7.3.2 Fault Detection and Isolation

3.3.3.2.1 Operator Methods

Three methods of fault detection and isolation for each subunit of the DPS (excluding power supplies and Maintenance Control Panels) and associated peripherals shall be provided:

(1) Integration Test

(2) System Test Program

(3) Maintenance Control Panel Tests

The associated peripherals shall be defined as the external devices to which the subunit interface. The associated peripherals for the DPS subunits are defined as follows: TACCO Tray, Sensor Station 3 Control Tray, Universal Keysets, Pilot Keyset, Ordnance Panel, ARO Display, Armament/Ordnance Test Panel, Magnetic Tape Transport, TACCO and Sensor Station 3 Multipurpose Displays, Pilot Display, Auxiliary Display, and Omega.

3.3.7.3.2.2 Integration Tests

The Integration Tests shall utilize the computer, the Maintenance Control Panel and the subunit external test points for the detection of malfunctions in the communication paths between equipments. The Integration Tests shall consist of a series of short programs or subroutines, operator initiated, interspersed by manual checks to exercise all communication paths between the computer, DPS, and associated peripherals. The Integration Test snail be used primarily during the initial integration of a given equipment into the total system and will therefore require a high degree of operator training.

The contractor shall provide Integration Test Specifications for each subunit (excluding power supplies) of the DPS.

The Integration Test Specifications shall be submitted to the Procuring Agency for approval.

3.3.7.3.2.3 System Test Program

The System Test Program shall utilize the computer for on-line fault detection and isolation of the DPS subunits and associated peripherals. The System Test program shall be divided into the following sections:

(1) System GO/NO-GO Tests (SYGNOG)

(2) Diagnostic Test

3.3.7.3.2.3.1 System GO/NO-Go Tests (SYGNOG)

The SYGNOG tests shall utilize the computer for a GO/NO-GO check of each subunit. The SYGNOG test shall test every logic element of the subunit in so far as possible. The only limitations imposed on the test will be those required for safety. The operator shall be the initiator of the test and will be available for visual monitoring of faults (which the computer cannot detect) and the activating of those computer inputs which require manual operation. The contractor shall provide a SYGNOG test specification for each subunit of the DPS.

The SYGNOG test shall be documented in accordance with WS-8506. The primary purpose of the SYGNOG test shall be to detect the presence of faults and reform the operator of operational readiness of the subunit under test. The SYGNOG test for each DPS subunit shall include the associated peripheral to which the DPS subunit interfaces.

The SYGNOG test documentation shall be submitted to the Procuring Agent y for approval.

3.3.7.3.2.3.2 Diagnostic Tests

The Diagnostic Program shall utilize the computer to diagnose equipment malfunctions for each subunit of the DPS (excluding power supply and Maintenance Control - Panel subunits). The Diagnostic Program shall be capable of delineating any subunit failure to such a level that any further isolation and replacement of the failed module may be accomplished in 15 minutes or less for 50% of such failures and in 30 minutes or less for 95% of such failures. To the extent permitted by the characteristics of the subunit, the Diagnostic Program shall satisfy the following requirements:

(1) Comprehensive - Every logical element shall be tested in all of its functions within the limits of the Diagnostic Hardware constraint.

(2) Automatic - Operator intervention shall be held to a minimum. To satisfy this requirement, test loops should be included in the design of those subunits which receive data from and transmit data to the computer. The Test Loops shall permit the computer to selectively monitor the performance of the logic elements in the subunit for the purposes of fault detection and isolation. The criterion to be used in the design of the Test Loops is as follows: The amount of hardware for the Test Loops shall not exceed 15% of the total hardware for the unit. A computer input channel shall be assigned to Logic Unit 3 for monitoring of the test loops by the Diagnostic Programs. The Diagnostic specifications module for each subunit of the DPS shall include the peripheral equipment to which it interfaces.

The Diagnostic Program specifications for each subunit of the DPS shall be in accordance with WS-8506 and shall be submitted to the Procuring Agent y for approval.

3.3.7.3.2.4 Maintenance Control Panel Tests

The Maintenance Control Panel Test shall provide the Off-Line maintenance capability for the DPS. Maintenance Control Panel Tests shall provide an example of detailed operating procedures for the Maintenance Control Panel, test description for each subunit, library of normal operation codes, test codes, and test point waveforms for the normal operation in order to provide a functional check of each subunit. The goal of the MCP tests shall be to provide sufficient documentation to enable a Maintenance Technician to analyze the problem and formulate his own detailed detection and isolation procedures. The contractor shall provide a Maintenance Control Panel test for each subunit (excluding power supplies and the Maintenance Control Panel Subunit) of the DPS. (The MCP is used as a tool to test the Logic Unit proper, but has no self-test capability.) The tests shall include Universal Keysets, Pilot Keyset, Ordnance Panel, TACCO Control Tray, Sensor Control Tray, Armament/Ordnance Panel and Magnetic Tape Transport in addition to all logic subunits except Power Supplies. The use of the peripheral equipments not listed herein may be used as an aid to the technician for the purpose of monitoring outputs and stimulating inputs to each DPS subunit as needed. The Maintenance Control Panel tests shall be included as part of the Organizational Maintenance Instruction Manuals for each Logic Unit and shall be validated and approved as such.

3.3.7.3.3 Test Point Requirement - Any test points required shall accommodate general purpose test equipment, i. e. , multimeter or oscilloscope probes. In the event test points cannot accommodate standard probes, use of adapters will be permitted. These adapters are to be provided with and secured to the unit.

3.3.7.3.4 Special Support Equipment (SSE) - There shall be no special support equipment for support of the equipment except as expressly authorized by the procuring activity.

3.3.8 Nomenclature and Nameplates - Nomenclature assignment and nameplate approval for equipment identification shall be in accordance with Specification MIL-N-18307.

3.3.9 Standard Conditions - The following conditions shall be used to establish normal performance characteristics under standard conditions and for making laboratory bench tests.

Temperature	Room ambient (25°C ±5°C)
Altitude	Normal Ground
Vibration	None
Humidity	Room ambient up to 90% relative humidity
Input Power Voltage	115 ±l.0 VAC, 3 phase 400 Hz ±1%

3.3.10 Service Conditions - The equipment shall operate satisfactorily under any of the environmental service conditions or reasonable combination of these conditions as specified in Specification MIL-E-5400 for Class 1AX equipment, except as modified herein.

3.3.10.1 Vibration - The equipment shall operate satisfactorily when subjected to the vibration requirements of MIL-E-5400 Curve I from 5 to 32 Hz and ±2 g from 32 to 500 Hz.

3.3.10.2 Attitude - The equipment shall operate satisfactorily in all attitudes and orientations within ±90° of its normal mounting orientation.

3.3.10.3 Fungus Treatment - Equipments shall be fungus-proofed by selection of parts and materials that are non-nutrient for fungus, or the parts and materials shall be so treated prior to their use in the equipment that over-all spraying of the equipment is not necessary.

3.3.10.4 Explosion Proofing Not required.

3.3. 10.5 Temperature - The equipment shall operate as specified herein from -25°C to and including +55°C. The equipment shall also operate as specified for tests above +55°C per MIL-T-5422 except for the Drum Auxiliary Memory Subunit (DAMS) of Logic Unit 4 which shall not be required to meet the DAMS error rate requirements. However, no damage or degradation shall occur to the DAMS during high temperature MIL-T-5422 tests. From below -25°C to -54°C the equipment shall not be required to meet specification performance requirements; however, no damage or degradation shall occur to the equipment within the -25°C to -54°C limits.

3.3.10.6 Altitude - The equipment shall operate satisfactorily up to a maximum altitude of 15,000 feet.

3.3.11 Warm-Up Time - The time required for the equipment to warm up prior to operation shall be kept to a minimum and shall not exceed 0.5 minutes from 0° to and ineluding +55°C and 5 minutes from less than 0°C to and including -25 ‘C.

3.3.12 Power

3.3.12.1 Primary Input Power Requirements - The equipment shall meet all applicable requirements of MIL-STD-704 and shall give specified performance from the following power sources with characteristics as defined in MIL-STD-704 having limits as modified herein. The equipment shall operate within the bounds of limits 2 and 3 of Figure 3 of MIL-STD-704 except that the lower limit of curve 3 shall not fall below 80 volts. Operational malfunction may occur when the input voltage exceeds the above limits but remains within limits 1 and 4 of Figure 3 of MIL-STD-704. However, no damage shall be suffered by the equipment under transient conditions defined herein. Normal operation shall autoctmatically be resumed upon return of the input voltage to levels within limits 2 and 3 as modified herein. The power required shall not exceed the following specified amounts.

(1) AC Power (Three-Phase) 115/200 V, Category B

Logic Unit 1	588 VA
Logic Unit 2	609 VA
Logic Unit 3	609 VA
Logic Unit 4	810 VA
Universal Keyset	24 VA
Pilot’s Keyset	24 VA
Ordnance Panel	---
Armament/Ordnance Test Panel	78 VA

(2) AC Power (Single Phase) 115 V, Category B

Logic Unit 1	30.5 VA
Logic Unit 2	30.5 VA
Logic” Unit 3	30.5 VA
Logic Unit 4	30.5 VA
Universal Keyset (es)	77 VA
Pilot’s Keyset	50 VA
Ordnance Panel	22 VA
Armament/Ordnance Test Panel	----

3.3.12.1.1 AC Power - The equipment shall operate on an input voltage of 115 volts, line to neutral, 200 volts line to line, three phase 400 Hz as described in MIL-STD-704 Category B mode of operation except as modified herein.

3.3.12.1.2 AC Over Voltage - The input voltage transients shall remain within limits 1 and 2 of MIL-STD-704, Figure 3, for normal and abnormal operating conditions.

3.3.12.1.3 AC Under Voltage - The input voltage transients shall remain within limits 3 (as modified herein) and 4 of MIL-STD-704, Figure 3, for normal and abnormal operating conditons.

3.3.12.1.4 Loss Of Power - No damage shall result from accidental or deliberate stoppage of electrical power to the equipment regardless of the time in its operating cycle that such a stoppage should occur, and regardless of the time interval that elapses before power is restored.

3.3.12.1.5 DC Power - The use of 28 Volts DC aircraft power is specifically prohibited, except where specified as a requirement.

3.3.12.2 Power Supply Subunit - Each unit of the system shall have a power supply subunit which shall meet the requirements of MIL-STD-704, as modified herein.

3.3.12.2.1 Power Control Switch - A power control switch for activating and deactivating each power supply shall be supplied, except for keysets and panels.

3.3.12.2.2 Overload Protection - The power supply shall be protected from external overload conditions including short circuiting.

3.3.12.2.3 Over Voltage Protection - The power supply shall provide over voltage protection to the DPS under both normal and abnormal operation conditions. When normal operation is affected by an over voltage condition, indication of such a condition shall be provided.

3.3.12.2.4 Under Voltage Protection - The power supply shall provide under voltage protection to the DPS for both normal and abnormal operating conditions. When norrmal operation is affected by an under voltage condition, indication of such a condition shall be provided.

3.3.12.2.5 Power Supply Output Conditions (Excluding the Magnetic Drum Memory)

Voltage	Regulation	DPS Operating Limits
+5 VDC	±5%	± 1 10%
-10 VDC	±5%	± 10%

3.3.12.2.6 Normal Operation - The equipment shall operate under normal electric-system operation of MIL-STD-704, Section 6 except as specified herein.

3.3.12.2.7 Protective Devices - Circuit breakers shall be used in lieu of fuses whenever possible. All circuit breakers shall be accessible without removing equipment from racks. Fuses, if used, shall be of types and ratings readily available from Navy supply,

3.3.12.2.8 Overtemperature Sensor - Each logic unit power supply excluding the Magnetic Drum Memory Subassembly power supply shall contain thermal sensing circuitry to detect the maximum safe operating temperature and provide a signal to the aircraft power distribution system. The overtemperature signal shall be used by the airframe contractor to provide a warning to the TACCO Station operator that the respective Logic Unit is operating beyond the upper design thermal limit. The logic unit shall not automatically shut down as a result of the overtemperature sensor.

3.3.13 Special Support Equipment - Self-test features shall be such as to obviate the need for any Special Support Equipment for preflight, post-flight checks of fault isolation. There shall be no special support equipment for support of the equipment except as expressly authorized by the government.

3.3.14 Adjustments - In order to decrease the complexity of the maintenance tasks, the equipment should be designed to require no periodic adjustments, alignment or calibration. If adjustments are mandatory, they shall be capable of being made in the aircraft using simple tools and/or General and Standard Test Equipment.

3.4 Performance - Unless otherwise specified, values set forth to establish the requirements for satisfactory performance apply to performance under both standard and extreme service conditions. When reduced performance under the extreme conditions is acceptable, tolerances or values setting forth acceptable variations from the performance under standard conditions will be specified herein.

3.4.1 Description of System - The DPS shall be comprised of one each of Logic Units 1, 2, 3 and 4, three Universal Keysets, one Pilot's Keyset, one Armament/Ordnance Test Panel and one Ordnance Panel. (Refer to 1.3 regarding Magnetic Tape Transport.)

3.4. 1.1 Computer Input/Output - The subunits, which are assigned to a Computer Input and/or Output Channel will communicate with the computer in a 30 bit (max) parallel mode over the Input and/or Output Channel. The Input/Output Unit of the computer shall provide computer control of and communications with peripheral equipment. Up to 16 channels of input and 16 channels of output shall be provided in the Input/Output Unit. Each channel shall provide parallel data transfer for up to 30 data bits. Each group of four input channels and the corresponding group of four output channels shall have access to an assigned 32,768 word memory group, with selectability to other 32,768 word groups of a maximum 131,072 word memory by back panel wire change. In the delivered configuration, the four output data channels from each of the four output registers shall be bussed into one 30-twisted-pair cable. Each of these output groups shall be provided with control lines for four peripherals. Thus the output configuration will provide four data output channels from the 1/0 unit with control lines for a total of 16 peripherals.

Each of the computer I/O unit I/O groups contains a time-shared output register, input selection circuits, local I/O control and priority circuits.

Since the Output Register in an 1/0 group is time-shared by up to four Output peripherals, the 30 data lines emanating from the register are common to the four output peripherals, i. e. , an I/O group transmits the data to the four output peripherals over a single 30-twisted-pair cable and the control lines for the four Output peripherals determine which peripheral is to sample the data. The control lines for the four channels are independent. Subunits which communicate with the same I/O group have been assigned to the same logic unit. This permits a logic unit to buffer all incoming computer data with a single group of 30 input amplifiers. (Input amplifiers are defined in Appendix 11.)

Logic Units 2, 3, and 4 each require three computer output channels. Logic Unit 1 contains two subunits which are assigned a computer output channel. As indicated, a computer 1/0 group is capable of servicing up to four output peripherals, and since none of the logic units require more than three output channels, each logic unit shall make the 30 data lines from the computer 1/0 subunit available for "bussing" to one additional output peripheral. The data lines from the computer shall remain available for "bussing" regardless of the number of subunits removed from the logic unit.

3.4.1.1,1 A failure in Logic Unit 4 electronics shall not preclude normal operation of computer charnels O through 11 used in the aircraft with Logic Units 1, 2, and 3.

3.4.1.2 Maintenance Control Panel - Each logic unit shall contain a Maintenance Control Panel (MCP), which shall, as a minimum, provide the maintenance operator with the capability of monitoring the data and control lines associated with any computer input or output peripheral contained in the logic unit, and of operating anyone computer input or output peripheral contained within the logic unit off-line from the computer in either single step or continuous mode operation. The MCP shall also provide any additional maintenance functions described in the detailed requirements for the Logic Unit.

NOTE

Since the Maintenance Control Panels for the four logic units are nearly identical, only one detailed descriptions given for an MCP. (See MCP section for Logic Unit 1, 3.5.1.4.9.)

3.4.1.3 Power Control Panel - All subunits of each logic unit, except the MCP/MCPL subunits and the MTL subunit shall have on/off switches located on the power control panel. All MCP/MCPL subunits and the MTL subunit shall decontrolled by the master power on/off switch for the logic unit. Operation of the subunit switches shall be defined as an abnormal operating condition for the DPS.

3.4.1.4 Logic Units - Each of the four logic units is comprised of a number of subunits (functional groups of modules). Two criteria were used in the grouping of the subunits into logic units.

(1) Computer Input/Output Channel Assignment

(2) Functional Relationship

3.4.2 Logic Unit 1 Subunits - Logic Unit 1 shall contain the following subunits:

	No. Required
Digital Input Multiplexer	1
Digital Output Multiplexer	1
TACCO Tray Logic	1
Universal Keyset Logic	3
Pilot Key set/CRT Tray/Oral Panel Logic	3
Status Logic	1
Sono Receiver Logic	1
Auxiliary Readout (ARO) Display Interface Logic	1
Maintenance Control Panel/Logic	1
Power Supply	1

3.4.3 Logic Unit 2 Subunits - Logic Unit 2 shall contain the following subunits:

	No. Required
Magnetic Tape Control Logic	1
Armament: Ordnance Input Interface	1
Armament Output Interface	1
Ordnance Output Interface	1
Navigation Multiplexer	1
Maintenance Control Panel/Logic	1
Power Supply	1

3.4.4 Logic Unit 3 Subunits - Logic Unit 3 shall contain the following subunits:

	No. Required
Multi-Purpose Display (MPD) Interface	2
Pilot Display Interface	1
Function Generator	1
Master Timing Logic	1
Maintenance Control Panel,' Logic	1
Power Supply	1

3.4.5 Logic Unit 4 Subunits - Logic Unit 4 shall contain the following subunits:

	No. Required
Data Multiplexer Subunit	1
Auxiliary Display Logic	1
Drum Auxiliary Memory Subunit	1
Maintenance Control Panel/Logic	1
Spare Computer Channel Subunit	1
Power Supply	1

3.4.6 Keysets and Panels - Included in the system shall be the following separate items:

	No. Required
Universal Keysets	3
Pilot Keyset	1
Ordnance Panel	1
Armament 'Ordnance Test Panel	1

3.4.7 Logic Unit 1 Functions - The subunits of Logic Unit 1 shall perform the following system functions in conjunction with other equipments.

(1) Digital Input Multiplexer - The Digital Input Multiplexer permits one computer input channel to service up to 16 input peripheral equipments.

(2) Digital Output Multiplexer - The Digital Output Multiplexer permits one computer output channel to service up to 16 output peripheral equipments.

(3) TACCO Tray Logic - The TACCO Tray and TACCO Tray Logic allow the Tactical Coordinator (TACCO) to enter information into and receive information from the computer. This information transfer, in conjunction with the data presented on the TACCO MPD, permits the TACCO to prosecute the tactical situation.

(4) Universal Keyset Logic - A Universal Keyset Logic and a Universal Keyset allow a sensor operator to enter information into and receive information from the computer.

(5) Pilot Keyset Logic- The Pilot Keyset Logic and Pilot's Keyset allow the pilot to enter information into and receive information from the computer.

(6) CRT Tray Logic - The CRT Tray Logic and CRT Tray permit the operator to enter information into and receive information from the computer.

(7) Ordnance Panel Logic - The Ordnance Panel Logic and Ordnance Panel permit the operator to enter information into and receive information from the computer.

(8) Status Logic - The Status Logic provides for the transmission of status data from several aircraft systems to the computer. The status logic also provides for transmission of data from the computer to the navigation system.

(9) Sono Receiver Logic - All acoustic processors in the P-3C system receive their signals from the ARR-72 Sonobuoy Receiver. The ARR Sonobuoy Receiver consists of 31 fixed tuned receivers, each providing an audio signal output. These 31 outputs are sent to the switching matrix, the function of which is to switch 20 or less of them to 20 acoustic processing channels. Manual channel selection is accomplished through the use of nine remote Control/Indicator Panels. These nine panels serve 18 of the 20 processing channels. The other two channels have no manual control. Each half panel contains a thumbwheel capable of selecting one of 31 receivers, a decimal readout to indicate which receiver is selected, an "AGC" indicator for that receiver, and a Manual/Auto mode lamp. The SRL provides an integrated Computer/Manual tuning mode for the 31 receivers used in this system. This will allow the following operating modes:

(a) Computer control of the ARR-72 Switching Matrix with indication of channel status given to the operator.

(b) Direct operator control of the Switching Matrix with indication of the channel status given to the computer.

Additional control shall provide both computer selection of either mode, and manual overrides to force the SRL to mode (b) above. An additional requirement is to make it possible for the computer to monitor all RF activity within the ARR-72 spectrum. This allows the computer to select RF channels prior to launch, and to monitor sonobuoy operation (light-off) immediately after launch.

The logic provides logical signals so that the 20 acoustic processing channels may be switched to the desired RF channels. Additionally, one output channel is provided for the TACCO. The Light Off Detector Logic serves to provide logical signals to the matrix in order to call up the desired RF level (AGC) signal.

(10) Auxiliary Readout (ARO) Display Interface Logic - The ARO Display Interface Logic provides the interface between the computer and Auxiliary Readout Displays. The Auxiliary Readout Display provides a means for displaying computer generated tableau information on a Charactron-type display. One ARO is located at the TACCO Station and the other ARO is at the NAV/COM operator station.

3.4.8 Logic Unit 2 Functions - The subunits of Unit 2 shall perform the following system functions :

(1) Digital Magnetic Tape Subsystem (DMTSS) - The Digital Magnetic Tape Subsystem shall provide rapid retrieval of supplemental programs required during the mission, such as classification programs; and rapid interchange of operational programs with systems tests, integration tests, and diagnostic programs. The subsystem shall also record in-flight data (events) for use in post-flight data reduction and analysis.

The Digital Magnetic Tape Subsystem shall consist of a Magnetic Tape Subunit and a Magnetic Tape Transport.

(2) Armament/Ordnance Input Logic - The Armament/Ordnance Input Logic shall transmit to the computer an Armament Status Word which notifies the computer of ' the Armament and Ordnance System Status or Change of Status, i. e. ,

(a) Readiness of Search and Kill Store Weapons

(b) Change in Status of these Search and Kill Store Weapons

(c) Recognition and transmission of an error or malfunction in the Subsystem operation,

(d) Launch indication of Search and Kill Store Weapons.

(3) Armament Output Logic - The Armament Output Logic shall provide the capability for the computer program to select, arm, and release torpedoes, conventional and nuclear depth charges, rockets and mines, either individually or in salvo.

(4) Ordnance Output Logic - The Ordnance Output Logic shall provide the capability for the computer program to select and launch sonobuoys, explosive sound sources, and smoke markers at the appropriate time with the required accuracy and launch rates.

(5) Navigation Multiplexer (NM) - The NM provides an interface between the Inertial Platform and the Doppler to the computer.

3.4.9 Logic Unit 3 Functions - The subunits of Logic Unit 3 shall perform the following system functions:

(1) Multipurpose Display (MPD) Logic -The MPD Logic shall display tactical data, and comes under computer control in such away that the tactical plot of the ASW situation may be presented on the MPD. Furthermore, Scan Converted Radar data may bepresented on the MPD in conjunction with the tactical plot. The second Scan Converter is provided for future sensor equipments.

(2) Pilot Display Interface Logic -The Pilot Display interface Logic, under computer command, shall provide timing, control, deflection and video signals to control the presentation of tactical data on the Pilot Display. The tactical data shall consist of the aircraft symbol with track vector, fly-to-points, vectors, circles, flashing symbols, tabular information and the entire alphanumeric repertoire as required.

(3) Function Generator Logic - The Function Generator shall accept digital inputs that describe ellipses, circles and straight lines, process this data and generate the appropriate analog sine wave and unblank signal outputs to a CRT display system so as to cause ellipses, circles or straight lines to be displayed.

(4) Master Timing Logic - The Master Timing Logic (MTL) shall provide the timing and control signal necessary to "'line-lock" (sync) all display operations to the aircraft's 400 Hz power source. The MTL shall receive signals from MPD 1 Logic and MPD 2 Logic; and transmit signals to the MPD 1, MPD 1 Logic, MPD 2, MPD 2 Logic, Radar Interface Unit, Spare Scan Converter, Pilot Display Logic and Low Light Level TV.

3.4.10 Logic Unit 4 Functions - The subunits of Logic Unit 4 shall perform the following system functions:

(1) Data Multiplexer Subunit - The eight channel Data Multiplexer Subunit (DMS) is a digital interface unit capable of servicing eight peripheral equipments (one at a time) with input/output channel capability from a single computer channel.

(2) Auxiliary Display Logic - The Auxiliary Display Control Logic (ADL) under computer command (via DMS Output Charnel 2) shall provide timing, control deflection and video signals to control the presentation of functional data on a display at Sensor Stations 1and 2.

(3) Drum Auxiliary Memory Subunit - The Drum Auxiliary Memory Subunit (DAMS) shall provide rapid access and transfer of computer program segments. The DAMS shall also provide for rapid storage of computer data for purposes such as program recovery. The DAMS shall be functionally independent of all other subunits of Logic Unit 4 with the exception of the Maintenance Control Panel Subunit.

(4) Spare Computer Channel Subunit - Logic Unit 4 shall provide for an interface designated as Spare Computer Channel. Logic Unit 4 shall provide one input and one output connector compatible with full computer I/O capability for the spare channel.

3.4.11 Keyset and Panel Functions - The functions of the remaining items of the DPS are as follows:

3.4.11.1 Universal Keyset - The Universal Keyset shall contain data entry and readout devices.

3.4. 11.2 Pilot Keyset - The Pilot's Keyset shall contain 35 momentary Switches. This Keysetshall redesigned to communicate with the computer via the Keyset Logic and the Digital Input and Output Multiplexers.

3.4. 11.3 Ordnance Panel - The Ordnance Panel displays computer command information to the Ordnance operator concerning Search Stores, i.e. , Bin and Chute number and Status information.

3.4.11.4 Armament/Ordnance Test Panel - The panel shall provide an operator with a means of monitoring the performance of the Armament/Ordnance Logics.

3.5 Detail Requirements

3.5.1 Data Analysis Logic Unit MX-8023A/AYA-8 (Logic Unit 1)

3.5, 1.1 Function - See 3.4.7

3.5. 1.2 Form Factor - Refer to illustration in EI-515, Avionics Installation Instructions for Data Analysis Programming Group AN/AYA-8B.

3.5. 1.3 Weight - The total weight of Logic Units 1, 2, 3 and 4 shall not exceed 680 pounds.

3.5. 1.4 Contents - See 3.4.2

3.5. 1.4.1 Digital Input Multiplexer

3. 5.1.4.1.1 Functional Description - The computer is capable of servicing 16 input peripheral equipments which utilize the normal input data transfer. The DPS contains more than 16 input peripherals;-however, the rate and priority of the data to many of the the peripherals do not demand real time access to the computer memory: i.e. , many of the peripherals can communicate with the computer via a buffer unit. In the DPS, this common input buffer is termed the Digital Input Multiplexer (DIM). Figure 2 is a functional flow diagram for the DIM. Figure 3 is a timing diagram.

3.5.1.4.1.2 General Description - The DIM shall provide the capability of transmitting up to 12 data bits from each of the 16 input peripherals to the computer via a single computer input channel. The operation of the DIM shall be independent of the Digital Output Multiplexer (DOM) except for test loops.

3.5.1.4.1.3 Operating Requirements

3.5.1.4.1.3.1 Data Transfer - Peripheral Equipment to Computer via Digital Input Multiplexer - An input peripheral equipment which communicates with the computer via the DIM shall be able to transmit one 12-bit word to the computer by following the control line sequence given below:

(1) A peripheral equipment places its data on the 12 data lines to the DIM.

(2) The peripheral equipment sets the Enter line to the DIM to indicate that it has data ready for transmission.

(3) The DIM detects the Enter signal.

(4) The DIM places the 12 data bits from the peripheral equipment and 4 address bits on the computer data lines.

(5) The DIM sets the Input Data Request line to indicate that it has data ready for transmission to the computer except for channel 11 where it raises an Interrupt.

(6) The computer 1/0 subunit detects the Input Data Request.

(7) The computer samples the 16 data lines, at its convenience.

(8) The computer sets the Input Acknowledge line indicating that it has sampled the data.

(9) The DIM drops the data lines and the Input Data Request line.

(10) The DIM sets the Channel Input Acknowledge line to the peripheral equipment indicating that ‘the computer has sampled the data lines.

(11) The peripheral equipment drops the data at its convenience. The DIM shall not transmit any further data from this peripheral equipment to the computer until the equipment drops and then sets its Enter line indicating new data.

3.5.1.4.1.3.2 Timing, Priority and Initialization

(1) Since the peripheral equipments, which communicate with the computer via the DIM, operate independently of each other, a number of equipments may raise their Enter lines (indicating data is ready for transmission to the computer) simultaneously. The DIM shall sequentially scan the Enter lines from the peripheral equipments, stopping and entering the data from the first peripheral equipment with its Enter line set. The trailing edge of the Input Acknowledge shall start the DIM scanning again: the scan shall commence at the Enter line of the next peripheral equipment in the normal scan sequence. The order in which the DIM scans the peripheral equipments is designated by the channel numbers assigned to the equipments. There shall be no priority in the DIM, except for channel 11; if a number of peripheral equipments simultaneously set their Enter lines, the peripheral equipment serviced first by the DIM shall depend on the position of the scanner; e.g. , if peripheral equipments 1, 2, and 8 simultaneously set their Enter lines and the scanner normally scans sequentially from channel O through 15 and the scanner is at channel 6, the data from channel 8 shall be entered first and then channels 1 and 2 shall be serviced in that order before 8 can be serviced again. Upon receipt of a channel 11 Enter, the DIM shall complete the transmission of any channel being processed and then transmit channel 11 data.

(2) The time required for the DIM to scan all the Enter lines from the 16 peripheral equipments, when none of the Enter lines is set, shall not exceed 64 micro-seconds,

(3) The time between the detection of an active Enter line by the scanner and the raising of the Input Data Request line to the computer shall not exceed six micro-seconds,

(4) The DIM shall be self-initializing; i.e. , when power is applied to the DIM, no spurious data shall be transmitted to the computer and the DIM shall be ready for normal operation.

3.5. 1.4.1.4 Test Loops

3.5. 1.4.1.4.1 In-Flight Performance Monitoring Channels - Two of the channels of the DIM shall be designated as test channels. The setting of the Enter and Data lines for these channels shall be controlled by the computer program via the DOM. The DIM shall scan the Enter lines and transmit the data from these channels the same as it would for any other peripheral equipment. This loop operation, computer to DOM to DIM to computer, shall permit the computer program to monitor automatically the performance of the DOM and DIM. The test loops shall be utilized for in-flight performance monitoring and diagnostic programs.

3. 5.1.4.1.5 Interface Requirements - Refer to Figure 2, the functional flow diagram for the DIM.

3. 5.1,4.1.5.1 Format of Input Word to Computer from Digital Input Multiplexer - Refer to the format shown in Figure 1.

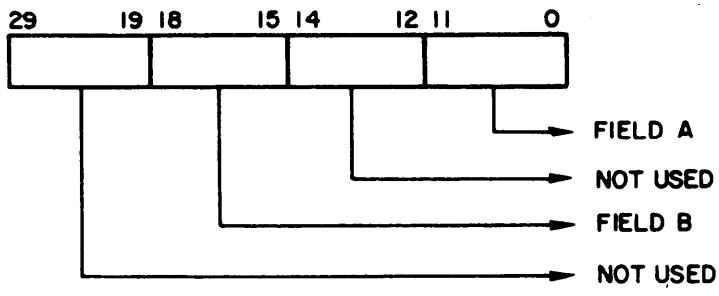


Figure 1. Format of Input Word to Computer from Digital Input Multiplexer

(1) Field A - represents the data bits from the peripheral equipment being serviced by the DIM.

(2) Field B - represents the address of the peripheral equipment selected by the DIM. The functional flow diagram (Figure 2) indicates the DIM channel assignments for the peripheral equipments.

3.5.1.4.1.5.2 Digital Input Multiplexer to Computer - Communications between the computer and the DIM shall be in accordance with Appendix I. Data transfer is accomplished by the Input Data Request/Input Acknowledge scheme.

3.5.1.4.1.5.3 Digital Input Multiplexer to Maintenance Control Panel - Communications between the Maintenance Control Panel and the DIM shall be in accordance with 3.5.1.4.9.

3.5.1.4.1.5.4 Peripheral Equipments Contained Within Logic Unit 1 and Digital Input Multiplexer.

3.5.1.4.1.5.4.1 Signal Characteristics

(1) logical "1" = +5 ± 1.5 volts
logical "0" = 0 ± 1/2 -0.0 volts

(2) Enter - The Enter line from a peripheral equipment shall change from a logical "1" to a logical "0" when new data is available. The Enter line shall remain stable for a minimum of 20 milliseconds or until a Channel Input Acknowledge signal is recieved from the DIM.

(3) Data - All data lines from a peripheral equipment shall remain stable for a minimum of 20 milliseconds or until a Channel Input Acknowledge is received by the equipment.

(4) Channel Input Acknowledge - The DIM shall transmit a Channel Input Acknowledge signal to the peripheral when the data from the peripheral equipment has been received by the computer. The Channel Input Acknowledge signal shall be a logical "1" signal of 2.2 microseconds minimum duration. The Channel Input Acknowledge signal indicates to the peripheral equipment that it may drop its Enter line at its convenience. The TACCO, Universal Keysets and Pilot/CRT/ORD Keysets shall not require an Input Acknowledge to reset their Enters.

3.5.1.4.1.5.5 Peripheral Equipments External to Logic Unit 1 (Channels 12, 13, 14, and 15) and Digital Input Multiplexer.

3.5. 1.4.1.5.5.1 Signal Characteristics

(1) logical "l" = 0 ± 1/2 -0.0 volt
logical "0" = 4 ±1 volts

(2) All signals between the DIM and the external peripheral equipments shall be transmitted over twisted pair cables.

(3) Enter - Same as 3.5.1.4.1.5.4.1 (2)

(4) Data - The data lines from an external peripheral equipment shall be stable at least one microsecond before the Enter line is set and shall remain stable until a Channel Input Acknowledge signal is received from the DIM, The selective enabling of data from an external peripheral equipment for transmission to the computer shall be performed in the DIM and hence no Data Enable signal shall be required for the data to be transmitted from the external peripheral equipment to the DIM.

(6) Channel Input Acknowledge - Same as 3.5.1 .4.1.5.4.1 (4).

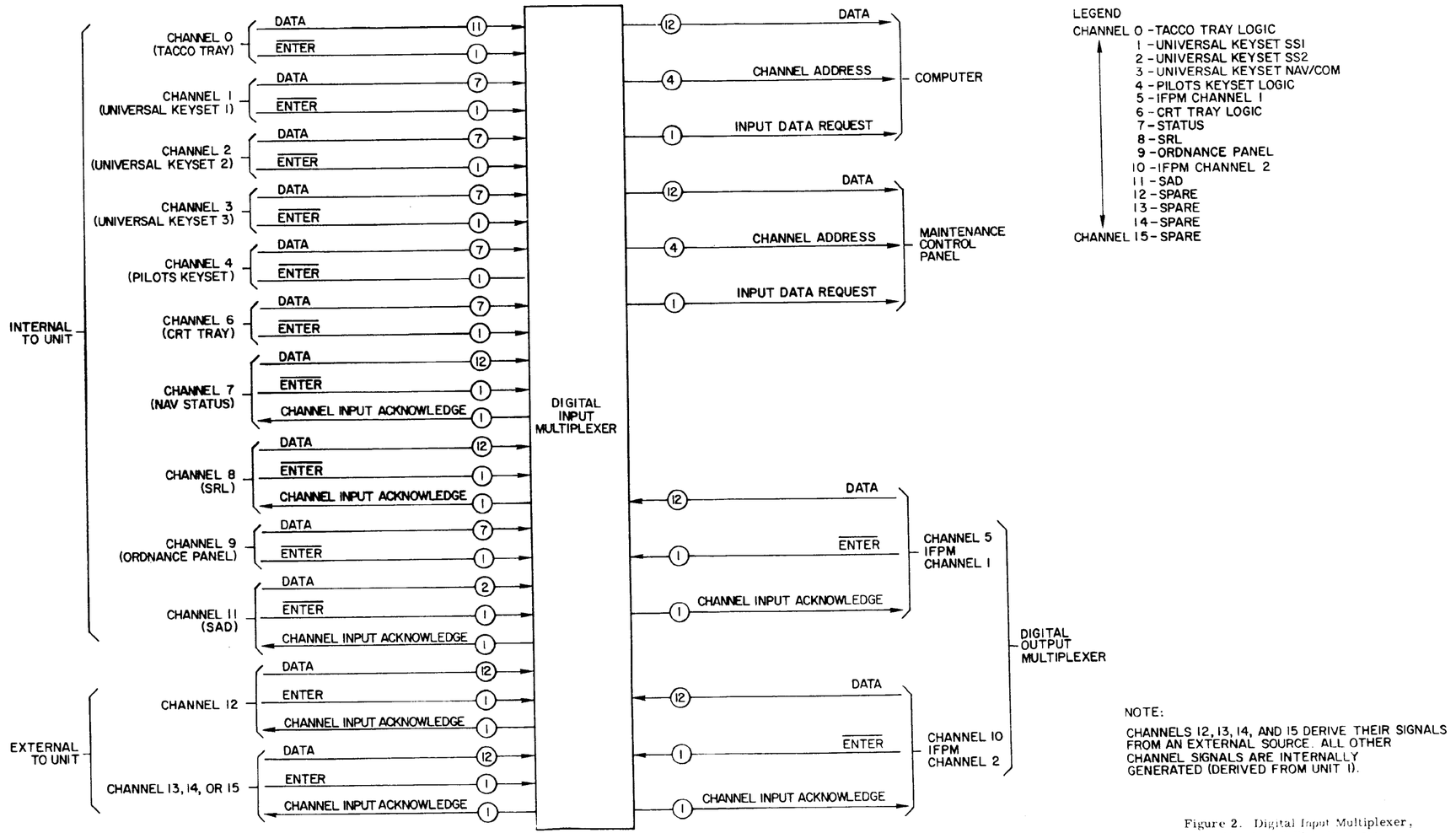


Figure 2. Digital Input Multiplexer, Functional Flow Diagram

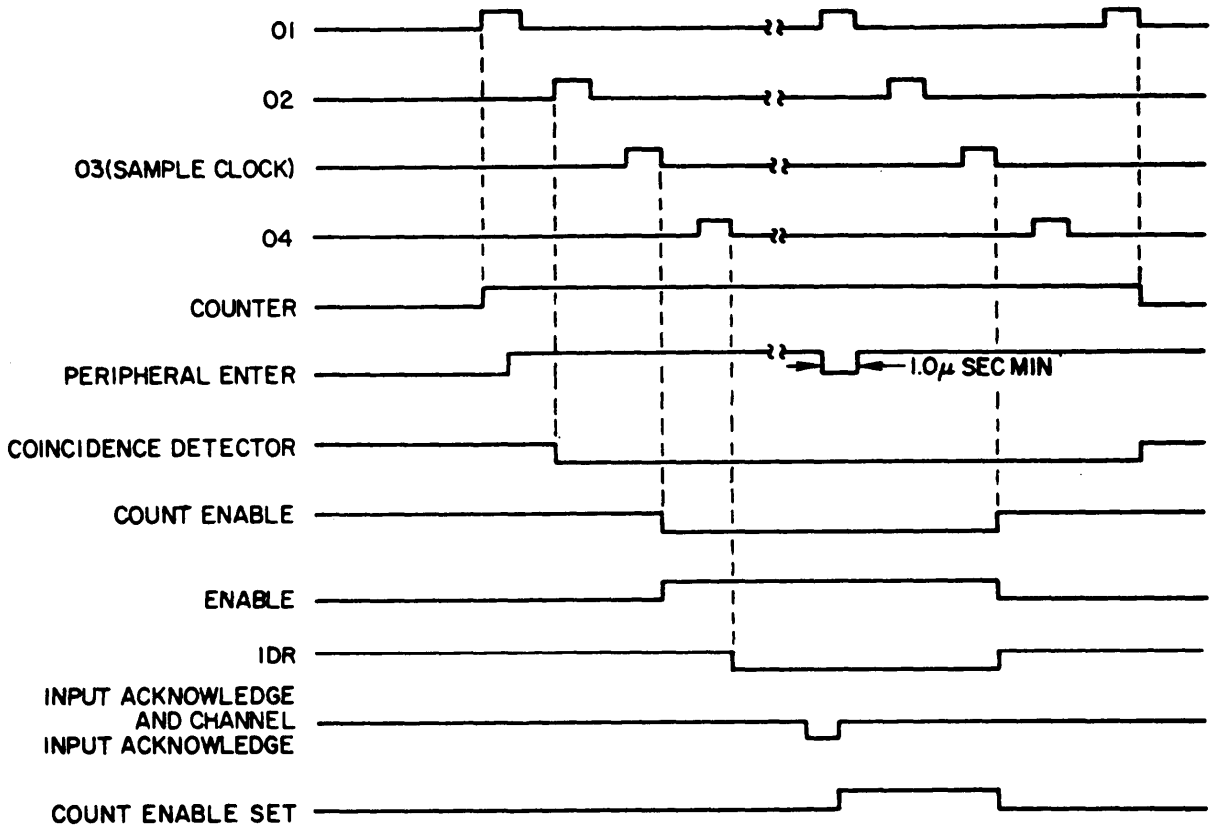


Figure 3. Digital Input Multiplexer, Timing Diagram

3.5.1.4.2 Digital Output Multiplexer

3.5.1.4.2.1 Functional Description - The Computer is capable of servicing 16 output peripheral equipments which utilize the normal output data transfer. The DPS contains more than 16 output peripherals; however, the rate and priority of the data from many of these peripherals do not demand realtime access to the computer memory; i.e., many of the output peripherals can communicate with the computer via a buffer unit. In the DPS, this common output buffer is termed the Digital Output Multiplexer (DOM). Figure 5 is a functional flow diagram for the DOM.

3.5.1.4.2.2 General Description - The DOM shall provide the capability of transmitting up to 12 data bits from the computer to each of 16 output peripherals via a single computer output channel. The operation of the DOM shall be independent of the DIM except for test loops.

3.5.1.4.2.3 Operating Requirements

3.5.1.4.2.3.1 Data Transfer - Computer to Peripheral Equipment via Digital Output Multiplexer - The computer shall be able to output one 12-bit data word to one of the 16 peripheral equipments by following the control sequence given below:

(1) The computer program initiates a normal output buffer for the channel assigned to the DOM.

(2) The DOM sets the Output Data Request line indicating that it is in a condition to accept data.

(3) The computer 1/0 subunit detects the Output Data Request.

(4) The computer, at its convenience, places 12 data bits and 4 address bits (identifying the peripheral equipment to receive the data) on 16 computer data lines.

(5) The DOM transmits the 12 data bits to each of the 16 peripheral units.

(6) The computer sets the Output Acknowledge line, indicating that the data is ready for sampling.

(7) The Digital Output Multiplexer decodes the address and transmits the Output Acknowledge signal to the peripheral equipment specified by the address code.

(8) The peripheral equipment, upon receipt of the Output Acknowledge signal from the DOM, samples the 12 data lines.

(9) The Computer drops the Output Acknowledge.

(10) The DOM drops the Output Acknowledge to the peripheral equipment, indicating that the period for sampling the data is terminated.

3.5.1.4.2.3.2 Timing - The DOM shall be capable of processing one computer output word every 10 microseconds.

3.5.1.4.2.4 Test Loops

3.5.1.4.2.4.1 In-Flight Performance Monitoring Channels - Two of the channels (5 and 10) of the DOM shall be designated as test channels. When the computer program addresses these channels, the 12 data bits accompanying the test channel addresses shall be stored in the DOM. When the data is stable, the DOM shall set the Enter line of the DIM channel corresponding to the test channel addressed by the computer; i.e. , if the computer transmits data to channel 5, the DOM shall set the Enter line and transmit the stored data on the DIM channel 5 input data lines; the Enter line and data shall be reset when a Channel Input Acknowledge signal is received from the DIM: the same procedure shall be followed for DOM channel 10. This loop operation, computer to DOM to DIM to computer, shall permit the computer program to monitor automatically the performance of the DOM and DIM. The test loops shall be utilized for in-flight performance monitoring and diagnostic programs.

3.5.1.4.2.5 Interface Requirements - Refer to Figure 5, the functional flow diagram for the DOM.

3.5.1.4.2.5.1 Format of Output Word to Digital Output Multiplexer from Computer - Refer to Figure 4.

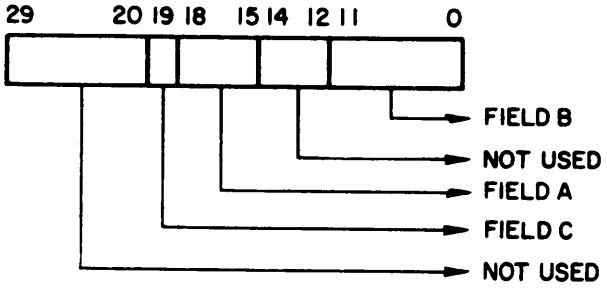


Figure 4. Format of Output Word to Digital Output Multiplexer from Computer

(1) Field A - Represents the address of the peripheral equipment which shall receive the channel Output Acknowledge indicating that the peripheral equipment should sample the data lines from the DOM.

(2) Field B - Represents the data for the peripheral equipment,

(3) Field C - A general clear to all DIM-DOM internal charnels.

3.5.1.4.2,5.2 Computer to Digital Output Multiplexer via Maintenance Control Panel - Communications between the Computer and the DOM shall be in accordance with Appendix I and the Maintenance Control Panel description in 3.5.1.4.9.

3.5.1.4.2.5,3 Peripheral Equipments Contained Within Logic Unit 1 and Digital Output Multiplexer

3.5.1.4.2.5.3.1 Signal Characteristics

(1) logical “0” = 0.0=0.5-0.0 volts
logical “1” = +5 ± 1.5 volts

(2) Channel Output Acknowledge Signal - The DOM shall transmit a Channel Output Acknowledge signal to a peripheral equipment when bits 15 - 18 of an output word from the computer contain the binary equivalent of the ‘peripheral equipment channel address. The channel addresses for each of the peripheral equipments are shown in the functional flow diagram for the DOM (Figure 5). The Channel Output Acknowledge shall be a logical “l” signal of 2.2 microsecond minimum duration.

(3) Data - The DOM shall transmit the data received from the Computer to each of the 16 peripheral equiments. The data lines to the peripheral equipments shall have the same timing as that specified for normal output in Appendix 1.

3.5. 1,4.2.5.4 Peripheral Equipments External to Logic Unit 1 and the Digital Output Multiplexer

3.5. 1.4.2.5.4.1 Signal Characteristics

(1) logical "1"= 0.0+0.5-0. Volt
logical “0” = +4 ± 1 Volts

(2) All signals between the DOM and the external peripheral equipments shall be transmitted over twisted pair cables.

(3) Channel Output Acknowledge - Same as 3.5.1 .4.2.5.3.1 (2).

(4) Data -Same as 3.5.l.4.2.5.3.l (3).

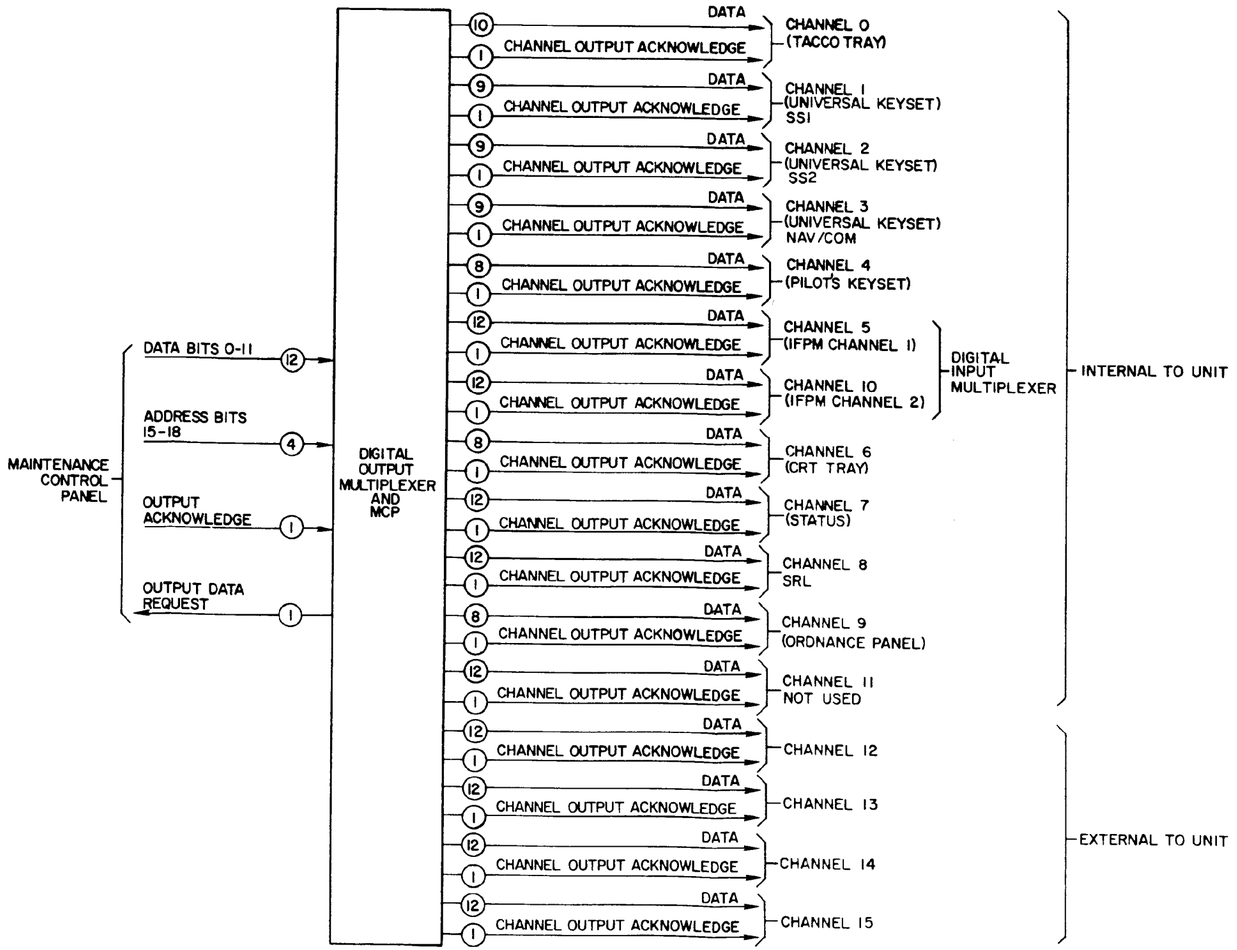


Figure 5. Digital Output Multiplexer, Functional Flow Diagram

3.5.1.4.3 TACCO Tray Logic

3.5.1.4.3.1 Functional Description - The TACCO Tray Logic (TTL) is an interface unit between the TACCO Tray and the computer (via the Digital Input/Output Multiplexer). The TACCO Tray will be a physical part of the MPD Display Console, located at the TACCO Station. The TACCO Tray provides the operator with the controls needed to execute the tactical situation. Using the controls on the Tray, the TACCO can utilize the DPS and computer to:

(1) Communicate with the sensor operators.

(2) Control the display of data from the sensor operators and the major subsystems on the MPD Display at the TACCO station.

(3) Initiate computer implemented functions which affect the operation of the Navigation, Communication, Sensor, Armament, and Ordnance subsystems.

Figure 8 is a functional flow diagram for the TTL.

3.5.1.4.3.2 General Description - The TACCO Tray Logic shall provide:

(1) The encoding and transmission of data from the TACCO Tray to the computer.

(2) The decoding and storage of data from the computer to the TACCO Tray.

3.5.1.4.3.3 operating Requirements - The TTL shall detect the depression of any switch on the tray and transmit a code identifying the depressed switch to the computer via the DIM. The operator will not have two switches depressed at the same time. The TTL shall interpret the computer output word received from the DOM and perform one of the following operations:

(1) Store the four bits of the computer word which specify the combination of function messages to be illuminated on the Matrix A Readout switches and the Matrix Select A switch to be lit. This four bit code shall be supplied to the TACCO Tray.

(2) Store the four bits of the computer word which specify the combination of function messages to be illuminated on the Matrix B Readout switches and the Matrix Select B switch to be lit. This four bit code shall be supplied to the TACCO Tray.

(3) Store the four bits of the computer word which specify the combination of function messages to be illuminated on the Matrix C Readout switches and the Matrix Select C switch to be lit. This four bit code shall be supplied to the TACCO Tray.

(4) Set or reset one of the 36 flip-flops. Each flip-flop shall control the illumination of the colored backfground (message 12) on one of the Matrix A, B, and C Readout switches. An output from each of the flip-flops shall be supplied to the TACCO Tray.

(5) Reset the 12 flip-flops which control the illumination of the colored background (message 12) on the Matrix A Readout switches.

(6) Reset the 12 flip-flops which control the illumination of the colored background (message 12) on the Matrix B Readout switches.

(7) Reset the 12 flip-flops which control the illumination of the coolered background (message 12) on the Matrix C Readout switches.

(8) Set or reset one of 44 flip-flops. Each flip-flop shall control the illumination of the colored background on one of the 44 computer lit Monofunction switches. An output from each of the flip-flops shall be supplied to the TACCO Tray.

(9) Reset 24 of the flip-flops which control the illumination of a colored background on 24 of the Monofunction switches.

(10) Reset the 20 flip-flops not covered in (9). Each flip-flop controls the illumination of a colored background on a Monofunction switch.

(11) Enable one of the test loops contained in the TTL.

The TTL shall be self-initializing; i.e. , when power is applied to the TTL, no spurious data shall be transmitted to the DIM and the TTL shall be ready for normal operation.

3.5.1.4.3.4 Test Loops - Test loops shall be designed into the TTL. The test loops shall permit the computer program to exercise the TTL and monitor the performance for possible logic malfunctions. The test loops shall be comprehensive; i.e. , they shall exercise every logic element in the TTL in all of its functions insofar as possible. The test loops shall be utilized for in-flight performance monitoring (IFPM) and diagnostic programs.

3.5.1.4.3.5 Interface Requirements - Refer to the functional flow diagram for the TTL Subunit (Figure 8).

3.5.1.4.3.5.1 Format of Input Word to Digital Input Multiplexer from TACCO Tray Logic - Refer to Figure 6.

(1) Field A - Identifies the switch group transmitting the data.

BIT	10	9	8	
	0	0	0	- self encoding keyboard or (30) Monofunction switch data
	0	0	1	- (38) Monofunction switch data
	0	1	0	- Matrix Select switch data
	1	0	0	- Matrix data

(2) Field B - Identifies test loop operation data; i. e, , if bit 7 is a logical “l”, the data contained in the remainder of the input word to the computer is not the result of a switch depression on the TACCO Tray but is due to test loop operation of the TTL by the computer program.

(3) Field C - Distinguishes self-encoding keyboard data from the Monofunction data in the switch group, identified by Field A being binary zero. Keyboard data is identified by a logical “1” in this position.

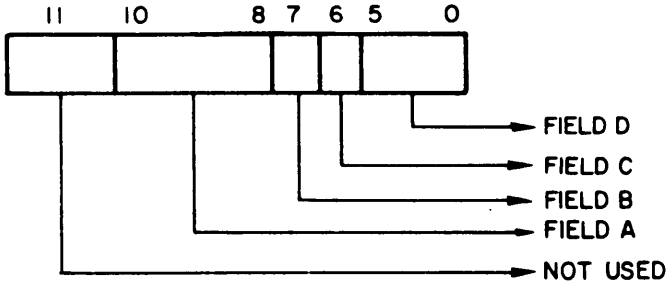


Figure 6. Format of Input Word to Digital Input Multiplexer from TACCO Tray Logic

(4) Field D- Identifies the switch or key depressed in the witch group or it contains the data resulting from test loop operation.

NOTE

Bits 0-10 of the input word to the DIM will constitute bits 0-10 of the input word to the computer from the DIM .

3.5.1.4.3.5.2 Format of Output Word to TACCO Tray Logic from Digital Output Multiplexer - Refer to Figure 7.

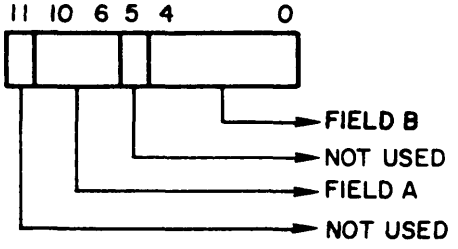


Figure 7. Format of Output Word to TACCO Tray Logic from Digital Output Multiplexer

(1) Field A- Indicates which of the following operations is to be performed:

(a) The flip-flop specified by Field B shallbe set or reset. The flip-flop may control the lighting of a colored background on a Monofunctionor Matrix switch, or the flip-f lop may control the enabling of a test loop.

(b) Reset a group of flip-flops. The flip-flop may control the illumination of colored backgrounds on the Matrix A or Matrix B or Matrix C switches or Monofunction switch group 1 or 2,

(c) Bits 0-3 of Field B constitute a message combination selection code for Matrix A, or B, or C and shall be stored in the appropriate register.

(2) Field B - Depending upon the Field A code, this field shall indicate one of the following:

(a) The flip-flop to be set or reset

(b) The Matrix message combination selection code

3.5.1.4.3.5.3 TACCO Tray Logic to Digital Input Multiplexer - Communications between the TTL and DIM shall be in accordance with 3.5.1.4.1.

3.5.1.4.3.5.4 Digital Output Multiplexer to TACCO Tray Logic - Communications between the DOM and the TTL shall be in accordance with 3.5.1.4.2.

3.5.1.4,3.5.5 Clock Signal from Maintenance Control Panel Logic to TACCO Tray Logic - A 10 millisecond clock signal for the TTL shall be generated in the MCPL.

3.5.1.4.3.5.6 Data Bits 0-4 from Maintenance Control Panel Logic to TACCO Tray Logic - Computer output data bits 0-4 shall be buffered in the MCPL.

3.5.1.4.3.5.7 TACCO Tray to TACCO Tray Logic

3.5.1.4.3.5.7.1 Signal Characteristics

(1) logical "1"= 0.0+0.5-0.0 Volt
logical “0” = open

(2) Switch Common - The switches and keyboard on the TACCO Tray are wired as four groups. The Matrix Readout switches constitute one group, the Matrix Select a second and the 68 Monofunction switches are divided into two groups. One group has 38 of the Monofunction switches, the other has 30 Monofunction switches in addition to the Keyboard data. Four switch common lines, one for each group, are provided to the TTL by the TACCO Tray. Whenever a switch or key is depressed in a group, the switch common makes a transition from logical “l” to logical “O”. The switch common will remain a logical “0” until the operator releases the switch (a minimum of 50 milliseconds). Up to 10 milliseconds of contact bounce noise may be present on both the leading and trailing edges of the signal.

(3) Keyboard Enter - The TACCO Tray will provide one keyboard enter (or data strobe) line to the TTL. The line will make the transition from logical “0” to logical “l” whenever a key is depressed. The signal will remain for a minimum of 50 milliseconds. Up to 10 milliseconds of contact bounce noise may be present on both the leading and trailing edges of the signal.

(4) Monofunction, Matrix Readout and Matrix Select Switches - The TACCO Tray will supply one switch line to the TTL for each of the 68 Monofunction, 6 Matrix Readout, and 36 Matrix Select switches. A switch line will make the transition from logical “O” to logical “1” whenever the associated switch is depressed. The signal will remain a logical “1” until the switch is released (a minimum of 50 milliseconds). Up to 10 milliseconds of contact bounce noise may be present on both the leading and trailing edges of the signal.

(5) Keyboard Data - The TACCO Tray will supply six encoded switch lines to the TTL for the keyboard. Whenever a key is depressed, the six-bit code identifying the depressed key is presented on these lines. The code remains for a minimum of 50 milliseconds. Up to 10 milliseconds of contact bounce noise may accompany the leading and trailing edges of the code on the signal lines.

(6) Ground - All signals between the TTL and TACCO Tray shall be referenced to the TTL signal return and the TTL signal shall be isolated from TACCO chassis and airframe ground.

3.5.1.4.3.5.8 TACCO Tray Logic to TACCO Tray

3.5.1.4.3.5.8.1 Signal Characteristics

(1) logical “1” = 3-6 volts, Drive = 2 MA
logical "0"= 0.0+0.5-0.0 Volts

(2) Matrix A, B, C, Background Illumination - The TTL shall supply a background illumination control line to the TACCO Tray for each of the 36 Matrix Readout switches. When a line is in the logical “l” state, message 12 (the colored background) will be illuminated on the associated Matrix Readout switch. A logical “0” on the line will not illuminate message 12. The logical state of an illumination control line shall be under computer program control.

(3) Monofunction Background - The TTL shall supply a background illumination control line to the TACCO Tray for each of the 44 computer lit Monofunction switches. When a line is in the logical “1” state, the colored background on the switch will be illuminated. A logical “0” on the line will not illuminate the colored background. The logical state of an illumination control line shall be under computer program control.

(4) Selection of the Function Messages to be Displayed on the Matrix Readout Switches -The TTL shall supply four message combination selection lines to the TACCO Tray for each of the three Matrix Readout groups. The four-bit code on each set of selection lines will determine the combination of function messages (or program" modules) to be-displayed on the associated Matrix Readout switch group. The four bit code will also cause that Matrix Select switch with a legend describing the combination of function messages currently being displayed on the Matrix Readout switch group to be illuminated with a colored background.

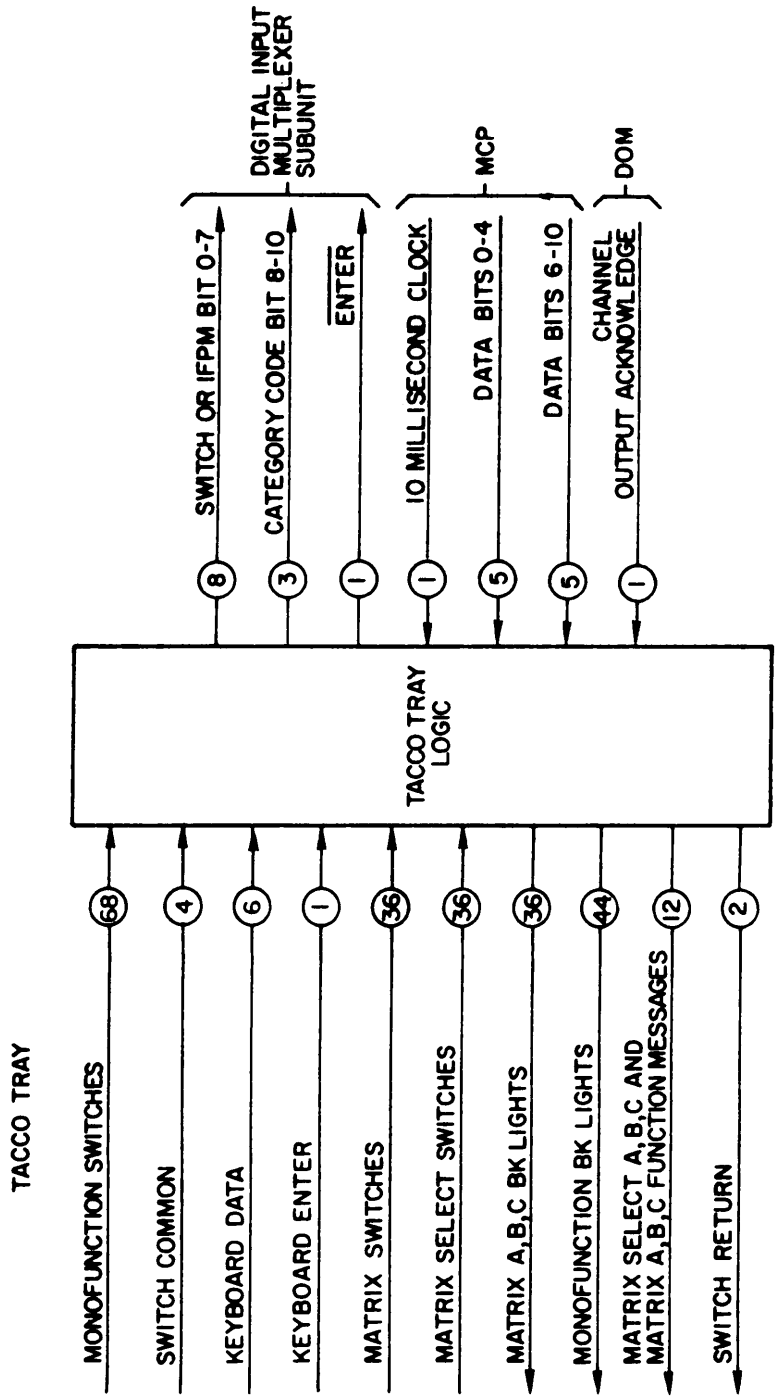


Figure 8. TACCO Tray Logic, Functional Flow Diagram

3.5.1.4.4 Universal Keyset Logic

3.5.1.4.4.1 Functional Description -The Universal Keyset Logic (UKL) is an interface unit between a Universal Keyset and the computer (via the Digital Input/Output Multiplexer). There will be three Universal Keysets in the DPS. The Navigation/Communication operator has a Universal Keyset at his disposal. Each of the two Acoustic Sensor Operators (Sensor Stations 1 and 2) has a Universal Keyset at his station. A Universal Keyset and Universal Keyset Logic permit an operator to enter information into and receive information from the computer program. Figure 11 shows the location of switches on the Universal Keyset. Figure 12 is a functional flow diagram of the Universal Keyset Logic.

3.5.1.4.4.1.1 Operation of Universal Key set and Universal Key set Logic in Conjunction with Computer Program - The switches on the Universal Keyset may be divided into four categories of operation:

(1) Matrix Readout Switches - The Matrix Readout switches are Shelly Readout Switches ROS -500 or equivalent. A Readout switch combines the features of a push-button momentary action switch and a rear projection readout device. The switch is mounted on the Projection Readout (PRO) in such a way that the switch may be actuated by depressing the viewing screen of the PRO. For the Universal Keyset application, each PRO may display up to nine messages; eight will be function messages and one message will be a colored background.

(2) Matrix Select Switches - The Matrix Select switches control the illumination of function messages on the Matrix Readout switches. The Matrix Select switches are physically operated as independent momentary action switches. Each Matrix Select controls the illumination of one combination or group of function messages on the Matrix Readout switches. The function messages in each of the eight combinations are related and when considered collectively, they form a Function Group. The Function Group or combination of function messages, which will be displayed by the depression of a Matrix Select, is described by the switch legend. When a Matrix Select switch is depressed, the UKL will detect the depression of the switch and transmit a code identifying the depressed switch to the computer via the DIM. The code indicates to the computer program what Function Group is to be displayed on the Matrix Readout switches. The computer program will respond by transmitting a word to the UKL via the DOM. The word will contain an identifier code and respond by transmitting a word to the UKL via the DOM. The word will contain an identifier code and the 4-bit code which specifies the particular combination of function messages to be displayed on the Matrix Readout switches and the Matrix Select switch to be lit, Once a Matrix Select switch is depressed, the function messages associated with the switch are displayed until another Matrix Select switch is selected.

Depression of a Matrix Readout switch will result in the computer implementing the function currently being displayed on the viewing screen of the switch. The computer program may display the colored background message on any of the Matrix switches at the same time that any one of the function messages is being displayed. The computer program will utilize this lighting capability to indicate when a function is active; i.e. , a function message displayed against an opaque background for a non-active or momentary function; a function message displayed against a colored background for an active function. The computer may illuminate or extinguish the colored background on a particular Matrix switch by transmitting an appropriately coded output word to the UKL via the DOM. Depending upon the coded word, the UKL will either set or reset the flip-flop which controls the illumination of the PRO.

(3) Keyboard - The switches labeled 20 through 28 represent numerics 1 through 9 respectively and switch 29 represents numeric 0. Using the keyboard, the operator may enter up to a 3-digit number into the computer program. Projection Readouts 7 through 9 are used by the operator to verify the number. The depression of a numeric switch results in the computer receiving an input word, identifying the depressed switch from the UKL via the DIM. The computer program will respond by transmitting a word to the UKL via the DOM. The word will cause the display of the numeric on PRO 9. If another numeric switch is depressed, the computer will transmit two successive output words which will cause the first numeric depressed to be displayed on PRO 8 and the numeric, currently depressed, to be displayed on PRO 9. Similarly, if another numeric is depressed, the computer will output three words which will cause the first numeric to be displayed on PRO 7, the second on PRO 8 and the third on PRO 9. If more than three numerics are depressed

in succession, PRO's 7 through 9 will display the last three numeric switches depressed. The numerics will be displayed on the PRO's until the operator indicates to the computer, by use of the keyboard control switches (30-32), that the number is to be processed or ignored. If the operator has only entered one or two numerics prior to the depression of a keyboard control switch, the computer program will consider the more significant numeric(s) to be zero(es).

(4) Monofunction Switches - The switches labeled 17 through 19 and 30 through 37 are termed Monofunction switches. Each of the Monofunction switches represents one and only one function. Depression of one of these switches results in the computer implementing the function indicated by the legend on the depressed switch. The computer program may provide colored background lighting for all the Monofunction switches with the exception of switches 30 - 32. The ccmputer program will utilize this lighting capability to indicate when a function is active; i.e. , a colored background indicates an active function. The computer may illuminate or extinguish a colored background on each of four Monofunction switches by transmitting an appropriately coded output word to the UKL via the DOM. Depending upon the coded word, the UKL will selectively set or reset each of four flip-flops; each flip-flop controls the illumination of one of the Monofunction switches

The Projection Readout Devices (PRO's) 1 through 6 are used to display amplifying information or cueing type messages to the operator. The message on each of the PRO's is selected by the computer program. The program may select a message to be displayed on a PRO by transmitting an output word to the UKL via the DOM. The word will identify the PRO and. contain the 4-bit message select code. The UKL will store the message select code.

3.5.1.4.4.2 General Description - The UKL shall provide:

(1) The encoding and transmission of data from a Universal Keyset to the computer.

(2) The decoding and storage of data from the computer to the Universal Keyset.

3.5.1.4.4.3 Operating Requirements - The UKL shall detect the depression of any switch on the Universal Keyset and transmit a code identifying the depressed switch to the computer via the DIM. The operator shall not have two switches depressed at the same time.

The UKL shall interpret the computer output word received from the DOM and perform one of the following operations:

(1) Store the four bits of the computer word which specify the combination of function messages to be displayed on the Matrix Readout switches and the Matrix Select switch to be lit. This four bit code shall be supplied to the Universal Keyset.

(2) Store the four bits of the computer word which specify the message to be displayed on one of the PRO's, in the appropriate storage location. There shall be a distinct storage location for each of the nine PRO's. The nine sets of four bit selection code lines shall - be supplied to the Universal Keyset.

(3) Selectively set or reset each of four flip-flops. Each flip-flop controls the illumination of a colored background on a computer lit Monofunction switch. An output from each of the flip-flops shall be supplied to the Universal Keyset.

(4) Selectively set or reset each of four flip-flops. Each flip-flop controls the illumination of a colored background on a computer lit Monofunction switch not controlled by (3). An output from each of the flip-flops shall be supplied to the Universal Key set.

(5) Selectively set or reset each of four flip-flops. Each flip-flop controls the illumination of a colored background message on a Matrix Readout switch. An output from each of the flip-flops shall be supplied to the Universal Keyset.

(6) Selectively set or reset each of four flip-flops. Each flip-flop controls the illumination of a colored background message on a Matrix Readout switch not controlled by (5). An output from each of the flip-flops shall be supplied to the Universal Keyset.

(7) Reset the storage registers for PRO's 7-9.

(8) Enable one of the test loops contained in the UKL.

Each UKL shall be self initializing; i.e. , when power is applied to a UKL, no spurious data shall be transmitted to the DIM and the UKL shall be ready for normal operation.

3.5.1.4.4.4 Test Loops - Test Loops shall be designed into each UKL. The test loops shall permit the computer program to exercise a UKL and monitor the performance for possible logic malfunctions. The test loops shall be comprehensive: i. e. , the test loops shall exercise every logic element in a UKL in all of its functions insofar as possible. The test loop shall be utilized for in-flight performance monitoring (IFPM) and diagnostic programs.

3.5.1.4.4.5 Interface Requirements - Refer to the functional flow diagram for the UKL Subunit, Figure 12.

3.5.1.4.4.5.1 Format of Input Word to Digital Input Multiplexer from Universal Keyset Logic - Refer to Figure 9.

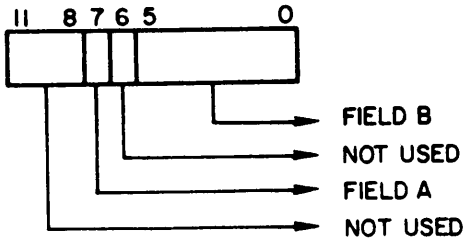


Figure 9. Format of Input Word to Digital Input Multiplexer from Universal Keyset Logic

(1) Field A - Identifies test loop operation data, i.e. , if bit 7 is a logical "l", the data contained in the remainder of the input word to the computer is not the result of a switch depression on the Universal Keyset but is due to test loop operation of the UKL by the computer program.

(2) Field B - Identifies the switch depressed or contains the data resulting from test loop operation.

NOTE

Bits 0-5 and 7 of the input word to the DIM form bits 0-5 and 7 of the input word from the DIM to the computer.

3.5.1.4.4.5.2 Format of Output Word to Universal Keyset from the Digital Output Multiplexer - Refer to Figure 10.

(1) Field A - Specifies which one of the following operations is to be performed.

(a) Field C is a message combination selection code for the Matrix Readout switches and shall be stored in the appropriate register.

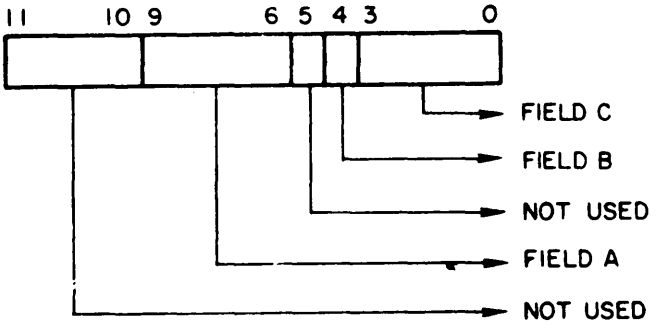


Figure 10. Format of Outcut Word to Universal Keyset from Digital Output Multiplexer

(a) Field C is a message selection code for a particular PRO and shall be in the storage location allotted to that PRO. There are nine Field A codes required for this purpose.

(c) Field C contains illumination control data for a particular group of four computer Monofunction switches and shall be stored in the appropriate register. There are two Field A codes required for this purpose since there is a total of eight computer lit Monofunction switches.

(d) Field C contains data for the illumination control of the colored background messages on a particular group of four Matrix Switches and shall be stored in the appropriate register. There are two Field A codes required for this purpose since there is a total of eight Matrix switches.

(e) Reset the storage flip-flops for PRO's 7-9.

In addition to one of the operations described above, Field A shall enable or disable (depending upon Field B) one of the test loops in the UKL.

(2) Field B - A logical "l" shall enable the test loop specified by Field A. A logical "0" shall disable the test loop specified by Field A; this bit is stored in the same register as the Field C bits.

(3) Field C- The interpretation and storage location of Field C depends upon Field A.

3.5.1.4.4.5.3 Universal Keyset Logic to Digital Input Multiplexer - Communications between the UKL and the DIM shall be In accordance with 3.5.1.4.1.

3.5.1.4.4.5.4 Digital Output Multiplexer to Universal Keyset Logic - Communications between the UKL and the DOM shall be in accordance with 3.5.1.4.2.

3.5.1.4.4.5.5 Clock Signal From Maintenance Control Panel Logic to Universal Keyset Logic- - A 10 millisecond clock signal for the UKL shall be generated in the MCPL.

3.5.1.4.4.5.6 Enter Signal from Universal Keyset Logic to Digital Input Multiplexer - An Enter signal shall be generated within the UKL when the subunit has data for transmission to the computer. This Enter signal shall be transmitted to the DIM.

3.5.1.4.4.5.7 Universal Keyset to Universal Keyset Logic

3.5.1.4.4.5.7.1 Signal Characteristics

(1) logical "1"= 0+0.5-0.0volt
logical “0” = open

(2) Switch Common- The switches on a Universal Keyset shall be wired as one group. A switch common line shall be provided for the group. Whenever a switchis depressed, the switch common shall make a transition from logical "1" to logical “0”. The switch common signal shall remain a logical “O” until the operator releases the switch (a minimum of 50 milliseconds). Up to 10 milliseconds of contact bounce noise may be present on both the leading and trailing edges of the signal.

(3) Matrix, Matrix Select, Keyboard, and Monofunction Switch - A Universal Keyset shall supply one switch line to the UKL for each of the 8 Matrix, 8 Matrix-Select, 10 Keyboard, and 11 Monofunction switches. A switch line shall make the transition from logical “O” to logical “l” whenever the associated switch is depressed. The signal shall remain a logical “l” until the switch is released (a minimum of 50 milliseconds). Up to 10 milliseconds of contact bounce noise may be present on both the leading and trailing edges of the signal.

(4) Ground - All signals between the UKL and the Universal Keyset shall be referenced to the UKL signal return. The UKL signal return shall be isolated from the Keyset chassis and air frame ground.

3.5.1.4.4.5.8 Universal Keyset Logic to Universal Keyset

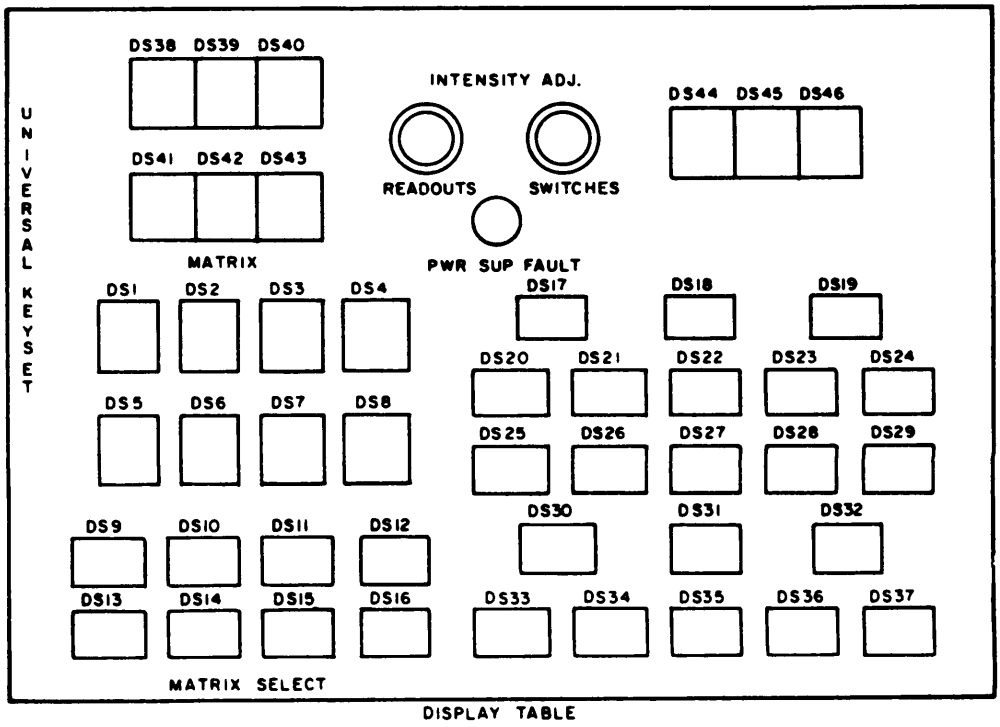
3.5.1.4.4.5.8.1 Signal Characteristics

(1) logical “1” = 3 - 6 volts, Drive = 2 MA maximum
logical “0” = 0+0.5-0.0volt

(2) Message Selection Codes for PRO’s 1 through 9- The UKL shall supply four message selection code lines to the Universal Keyset for each of PRO’s 1 through 9. The four bit code on each set of select lines shall determine the message to be displayed on the associated PRO.

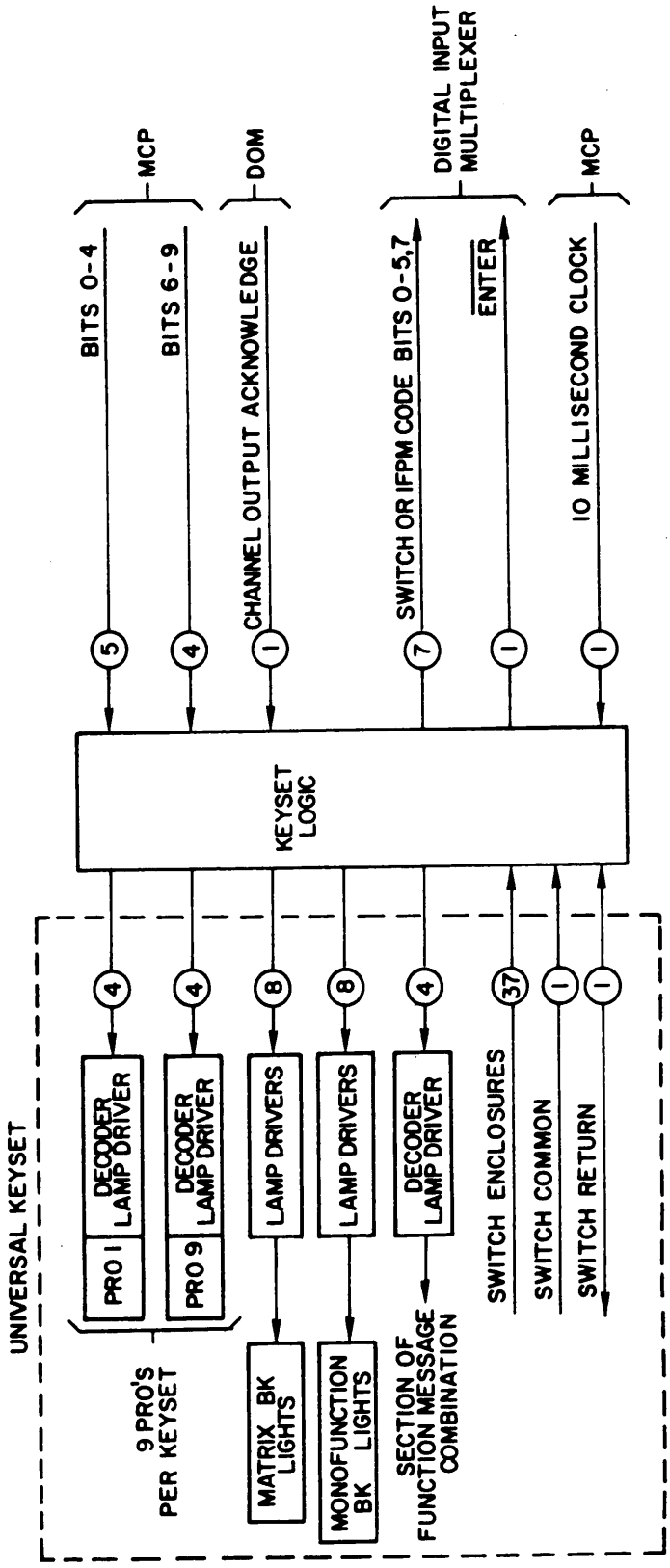
(3) Selection of Function Messages to be Displayed on Matrix Readout Switches - The UKL shall supply four message combination selection lines to the Universal Keyset. The four bit code shall determine the combination of function messages to be displayed on the Matrix Readout switches. The four bit code shall also cause that Matrix Select switch with a legend describing the combination of function messages currently being displayed on the Matrix Readout switches, to be illuminated with a colored background.

(4) Monofunction and Matrix Background Illumination - The UKL shall supply a background illumination control line to the Universal Keyset for each of the eight Matrix and eight computer lit Monofunction switches. When a line is in the logical “1” state, the colored background on the switch shall be illuminated. A logical “O” on the line shall not illuminate the colored background. The logical state of an illumination control line shall be under computer program control.



NOTE:
1. DS9-37 ARE NORMALLY ILLUMINATED GREEN
2. DS1-17, 33-46 ARE COMPUTER LIT

Figure 11. Universal Keyset Front Panel Layout



3.5.1.4.5 Pilot Keyset/CRT Tray/Ordnance Panel Logic

3.5.1.4.5.1 Functional Description - The name is derived from the use of three logically identical subunits to interface the three devices (Pilot Keyset, CRT Tray, Ordnance Panel). The Pilot Keyset and Pilot Keyset Logic permit the Pilot to:

(1) Control the presentation of information on the Pilot CRT Display

(2) Enter navigation stabilization information into the computer

(3) Drop Smokes via the computer and DPS

(4) Enter information on visual contacts

(5) Drop Weapons via the computer and DPS

The CRT Tray and CRT Tray Logic permit the Sensor Station 3 operator to control the presentation of sensor and computer data on the CRT Display and to enter sensor information into the computer program.

The Ordnance Panel and Ordnance Panel Logic enable the computer program to transmit commands to the Ordnance Operator. Illustrations of the Pilot Keyset and Ordnance Panel front panels are shown in Figures 17 and 18. Figures 19, 20 and 21 are functional flow diagrams of the Pilot Keyset, CRT Tray and Ordnance Panel Logic Subunits.

3,5. 1.4.5.1.1 Operation of Pilot Keyset and Pilot Keyset Logic in Conjunction With Computer Program - The switches on the Pilot Keyset may be divided into two categories of operation.

(1) Monofunction Switches - Switches 1 through 23 and 33 through 35 are termed Monofunction switches. The computer may illuminate a colored background on each of Monofunction switches 1 through 16. The operation of these switches is similar to the operation of the Monofunction switches on a Universal Keyset.

(2) Keyboard - Switches 23 through 31 represent numerics 1 to 9 respectively and switch 32 represents O. The operation of the keyboard is similar to the operation of the keyboard on a Universal Keyset. The only difference is that the three digit number to be processed by the computer program is displayed on the CRT Display and not on PRO's for verification by the operator.

3.5. 1.4.5.1.2 Operation of Ordnance Panel and Ordnance Panel Logic in Conjunction With Computer Program

(1) Switches - The operation of the three switches on the Ordnance Panel is similar to the operation of Monofunction switches on a Universal Keyset.

(2) Projection Readout Devices - Two of the PRO's on the Panel are used to indicate the bin associated with the sonobuoy; the other two PRO's indicate the chute into which, or in which, the sonobuoy is loaded. The message on each PRO is selected by the computer program. The program may select a message to be displayed on a PRO by transmitting an output word to the Ordnance Panel Logic via the DOM. The word will identify the PRO and contain the four bit message select code. The Ordnance Panel Logic will store the message select code.

(3) Status Readout - The Status Readouts specify whether the sonobuoy is to be taken from the bin and loaded into the chute or the sonobuoy is in the chute and is to be unloaded and replaced in the bin. The program may select the Status Readout message to be illuminated by transmitting an output word to the Ordnance Panel Logic via the DOM. The word will contain an identifier and the four-bit message selection code.

3.5.1.4.5.2 General Description - The Pilot Keyset/CRT Tray/Ordnance Panel Logic Subunit (hereafter referred to as Logic Subunit) shall provide:

(1) The encoding and transmission of data from the Pilot Keyset or the CRT Tray or the Ordnance Panel to the computer.

(2) The decoding and storage of data from the computer to the Pilot Keyset or the CRT Tray or the Ordnance Panel.

3.5.1.4.5.3 Operating Requirements - The Logic Subunit shall detect the depression of any switch on the associated device (Pilot Keyset or CRT Tray or Ordnance Panel) and transmit a code identifying the depressed switch to the computer via the DIM. The operator shall not have two switches depressed at the same time.

The Logic Subunit shall interpret the computer output word received from the DOM and perform one of the following operations:

(1) Selectively store bits 0 - 4 of the output word in one of five storage registers

(2) Reset the five storage registers

(3) Enable one of the test loops contained in the Logic Subunit

Each Logic Subunit shall be self initializing; i. e. , when power s applied to the Logic Subunit, no spurious data shall be transmitted to the DIM and the Logic Subunit shall be ready for normal operation.

3.5.1.4.5.4 Test Loops - Test loops shall be designed into each Logic Subunit. The test loops shall permit the computer program to exercise the Logic Subunit and monitor the performance for possible logic malfunctions. The test loops shall be comprehensive; i. e. , the test loops shall exercise every logic element in the Logic Subunit in all of its functions insofar as possible. The test loops shall be utilized for in-flight performance monitoring (IFPM) and diagnostic programs.

3.5.1.4.5.5 Interface Requirements - Refer to the functional flow diagrams for the Pilot Keyset, CRT Tray and Ordnance Panel Logic Subunits (Figures 19, 20 and 21).

3.5.1.4.5.5.1 Format of Input Word to Digital Input Multiplexer from Pilot Keyset or CRT Tray or Ordnance Panel Logic Subunit - Refer to Figure 13.

(1) Field A - Identifies test loop operation data; i.e. , if bit 7 is a logical “l”, the data contained in the remainder of the input word is not the result of a switch depression but is due to test loop operation of the Logic Subunit by the computer program.

(2) Field B - Identifies the switch depressed or contains the data resulting from test loop operation.

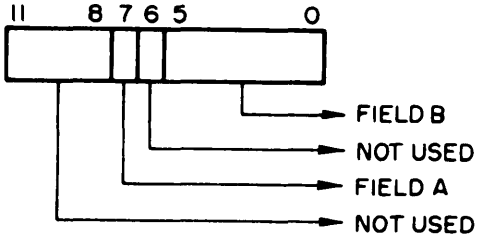


Figure 13. Format of Input Word to Digital Input Multiplexer from Pilot Keyset, CRT Tray; or Ordnance Panel Logic Subunit

3.5.1.4.5.5.2 Format of Output Word to Pilot Keyset Logic from Digital Output Multiplexer - Refer to Figure 14.

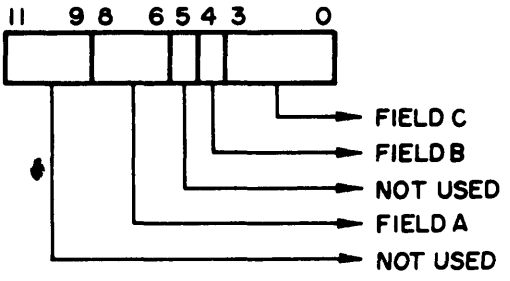


Figure 14. Format of Output Word to Pilot Keyset Logic from Digital Output Multiplexer

(1) Field A- Specifies which one of the following operations is to be performed.

(a) Field C contains illumination control data a for a particular group of four computer lit monofunction switches and shall be stored in the appropriate register. There are four Field A codes required for this purpose since there is a total of 16 computer lit Monofunction switches.

(b) Field C shall be stored in the spare storage register (fifth register). This register shall be utilized only in test loop operation.

(c) Reset all five storage registers.

In addition to one of the operations described above, Field A shall enable or disable (depending upon Field B) one of the test loops in the Logic Subunit.

(2) Field B - a logical "1" shall enable the test loop specified by Field A. A logical "0''shall disable the test loop specified by Field A. This bit is stored in the same register as the Field C bits.

(3) Field C - The interpretation and storage location of Field C depends upon Field A.

3.5.1 .4.5.5,3 Format of Output Word to CRT Tray Logic from Digital Output Multiplexer - Refer to Figure 15.

(1) Field A- Specifies which one of the following operations is to be performed.

(a) Field C is a message combination selection code for the Matrix Readout switches and shall be stored in the appropriate register.

(b) Field C contains illumination control data for a particular group of four computer lit Monofunction switches and shall be stored in the appropriate register. There are two Field A codes required for this purpose since there is a total of eight computer lit Monofunction switches.

(c) Field C contains data for the illumination control of the colored background messages on a particular group of four Matrix Readout switches and shall be stored in the appropriate register. There are two Field A codes required for this purpose since there is a total of eight Matrix Readout switches.

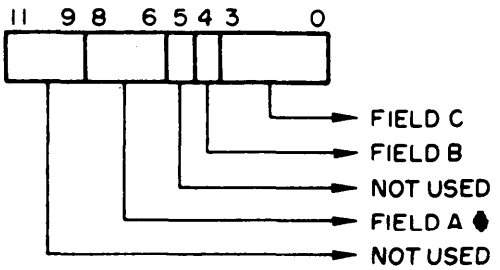


Figure 15. Format of Output Word to CRT Tray Logic from Digital Output Multiplexer

(d) Reset all five storage registers.

In addition to one of the operations described above, Field A shall also enable or disable (depending upon Field B) one of the test loops in the Logic Subunit.

(2) Field B - A logical "l" shall enable the test loop specified by Field A. A logical "O" shall disable the test loop specified by Field B. This bit is stored in the same register as the Field C bits.

(3) Field C - The interpretation and storage location of Field C depends upon Field A.

3.5.1.4.5.5.4 Format of Output Word to Ordnance Panel Logic from Digital Output Multiplexer - Refer to Figure 16.

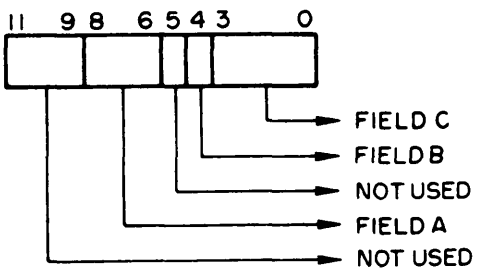


Figure 16. For mat of Output Word to Ordnance Panel Logic from Digital Output Multiplexer

(1) Field A - Specifies which one of the following operations is to be performed.

(a) Field C is a message selection code for one of the four PRO's and shall be stored in the storage register allotted to that PRO. There are four Field A codes required for this purpose.

(b) Field C is the message selection data for the Status Readout and Alert Signals and shall be stored in the appropriate register.

(c) Reset all five storage registers.

In addition to the operations described above, Field A shall enable or disable one of the test loops in the Logic Subunit,

(2) Field B - a logical "l" shall enable the test loop specified by Field A. A logical "0" shall disable the test loop specified by Field A. This bit is stored in the same register as the Field C bits.

(3) Field C - 'The interpretation and storage location of Field C depends upon Field A.

3.5.1.4.5.5.5 Logic Subunit to Digital Input Multiplexer - Communication between a Logic Subunit and the DIM shall be in accordance with 3.5. 1.4.1

3.5.1.4.5.5.6 Digital Output Multiplexer to Logic Subunit - Communications between a Logic Subunit and the DOM shall be in accordance with 3.5.1.4.2.

3.5.1.4.5.5.7 Clock Signal from Maintenance Control Panel Logic to Logic Subunit - A 10 millisecond clock signal for the Logic Subunit shall be generated within the MCPL.

3.5.1.4.5.5.8 Enter Signal from Logic Subunit to Digital Input Multiplexer - An Enter signal shall be generated within the Logic Subunit when the subunit has data for transmission to the computer. This Enter signal shall be transmitted to the DIM.

3.5.1.4.5.5.9 Pilot Keyset or CRT Tray or Ordnance Panel to Logic Subunit

3.5.1.4.5.5.9.1 Signal Characteristics

(1) logical "1" = 0.0+0.5-0-Volt
logical "0" = open

(2) Switch Common - The switches on a device (Pilot Keyset or CRT Tray or Ordnance Panel) are wired as one group. A switch common line for the group shall be provided by the device to the Logic Subunit. The switch common shall make a transition from logical "1" to logical "O" whenever a switch is depressed. The switch common signal shall remain a logical "O" until the operator releases the switch (a minimum of 50 milliseconds). Up to 10 milliseconds of contact bounce noise may be present on both the leading and trailing edges of the signal.

(3) Switch Line - The device shall supply one switch line to the Logic Subunit for each switch it contains. A switch line shall make the transition from logical "O" to logical "1" whenever the associated switch is depressed. The signal shall remain a logical "l" until the switch is released (a minimum of 50 milliseconds). Up to 10 milliseconds of contact bounce may be present on both the leading and trailing edges of the signal.

(4) Ground - All signals between the Pilot Keyset, CRT Tray, Ordnance Panel and the Logic Subunit shall be referenced to the Logic Subunit signal return. The Logic Subunit signal return shall be isolated from the CRT Tray, Pilot Keyset and Ordnance Panel Logic chassis and airframe ground.

3.5.1.4.5.5.10 Logic Subunit to Pilot Keyset

3.5.1.4.5.5.10.1 Signal Characteristics

(1) logical "1" = 3-6 volts, Drive = 2 MA maximum
logical "0" = 0.0+0.5-0.0 volt

(2) Monofunction Background Illumination - The Logic Subunits shall supply a background illumination control line to the Pilot Keyset for each of the computer lit Monofunction switches. When a line is in the logical "l" state, the colored background on the switch will be illuminated. A logical "O" on the line will not illuminate the colored background. The logical state of an illumination control line shall be under computer program control.

3.5.1.4.5.5.11 Logic Subunit to CRT Tray

3.5.1.4.5.5.11.1 Signal Characteristics

(1) logical "1"= 3 - 6 volts, Drive = 2 MA maximum
logical "0" = 0.0+0.5-0.0volt

(2) Selection of Function Messages to be Displayed on Matrix Readout Switches - The Logic Subunit shall supply four message combination selection lines to the CRT Tray. The four bit code shall determine the combination of function messages to be displayed on the Matrix Readout switches. The four bit code shall also cause the Matrix Select switch whose legend describes the combination of function messages currently being displayed on the Matrix Read-out switches to be illuminated with a colored background.

(3) Monofunction and Matrix Background Illumination - The Universal Keyset Logic shall supply a background illumination control line to the Universal Keyset for each of the eight Matrix and eight computer lit Monofunction switches. When a line is in the logical "l" state, the colored background on the switch shall be illuminated. A logical "O" on the line shall not illuminate the colored background. The logical state of an illumination control line shall be under computer program control.

3.5.1.4.5.5.12 Logic Subunit to Ordnance Panel and Aircraft System

3.5.1.4.5.5.12.1 Signal Characteristics

(1) logical "1" = 3 - 6 volts Drive = 2 MA maximum
logical "0" = 0.0+0.5-0.0 volt

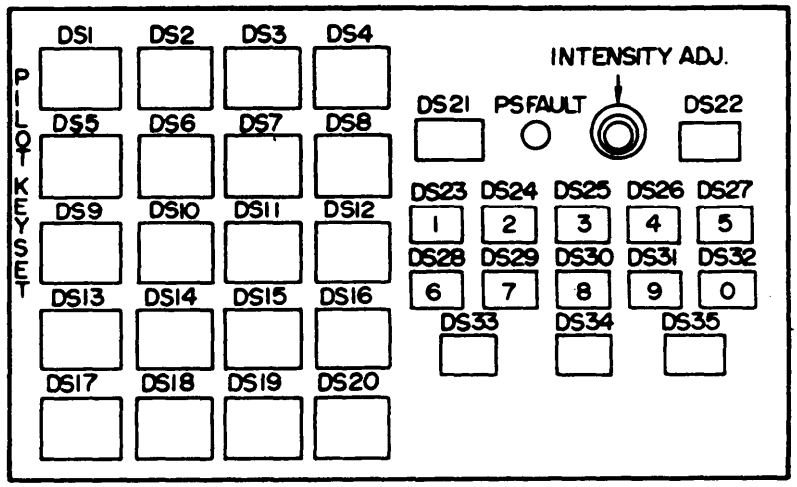
(2) Message Selection Codes for Four PRO's - The Logic Subunit shall supply four message selection code lines to the Ordnance Panel for each of the four PRO's. The four bit code on each set of selectior lines shall determine the message to be displayed on the associated PRO.

(3) Message Selection Data for Status Readout and Alert Signals - The Logic Subunit shall supply three message selection data lines to the Status Readout. The three bits shall determine the Status Indicator or alert indicator to be illuminated.

(4) The Logic Unit shall provide 100 MA, +12. O volts unregulated d-c power and a ground reference to the aircraft system for the operation of alert indicator interface circuits.

NOTE

The alert signal is not located on the Ordnance Panel.

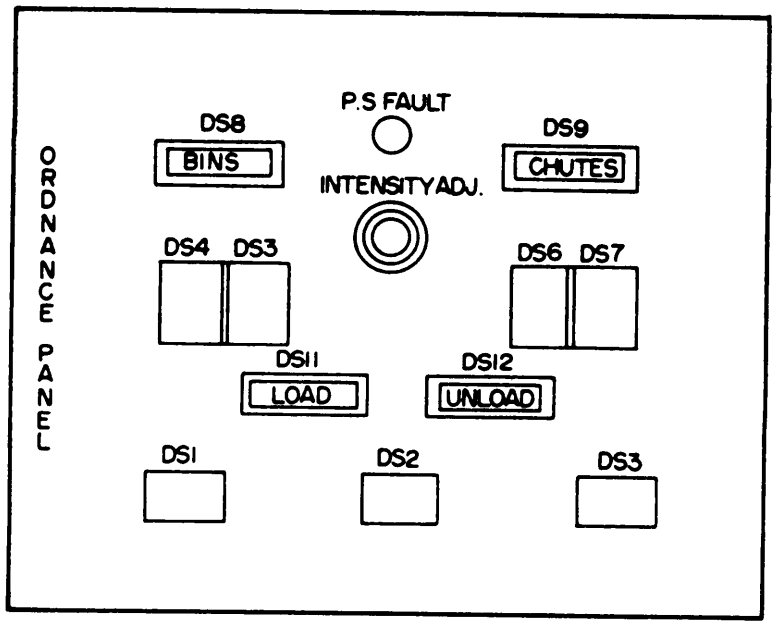


NOTE 1- S1 THRU S35 ARE NORMALLY ILLUMINATED GREEN. STATUS CONTROL SWITCHES S1 – S16 WILL CHANGE FROM GREEN TO AMBER.

2- LEGENDS ARE WHITE CHARACTERS ON OPAQUE (BLACK) BACKGROUND.

3- DS1 – DS16 ARE COMPUTER LIT.

Figure 17. Pilot Keyset Front Panel Layout



NOTE:
1. DS1-3, 8 & 9 ARE NORMALLY ILLUMINATED GREEN
2. DS4-7, 11 & 12 ARE COMPUTER LIT.

Figure 18. Ordnance Panel Front Panel Layout

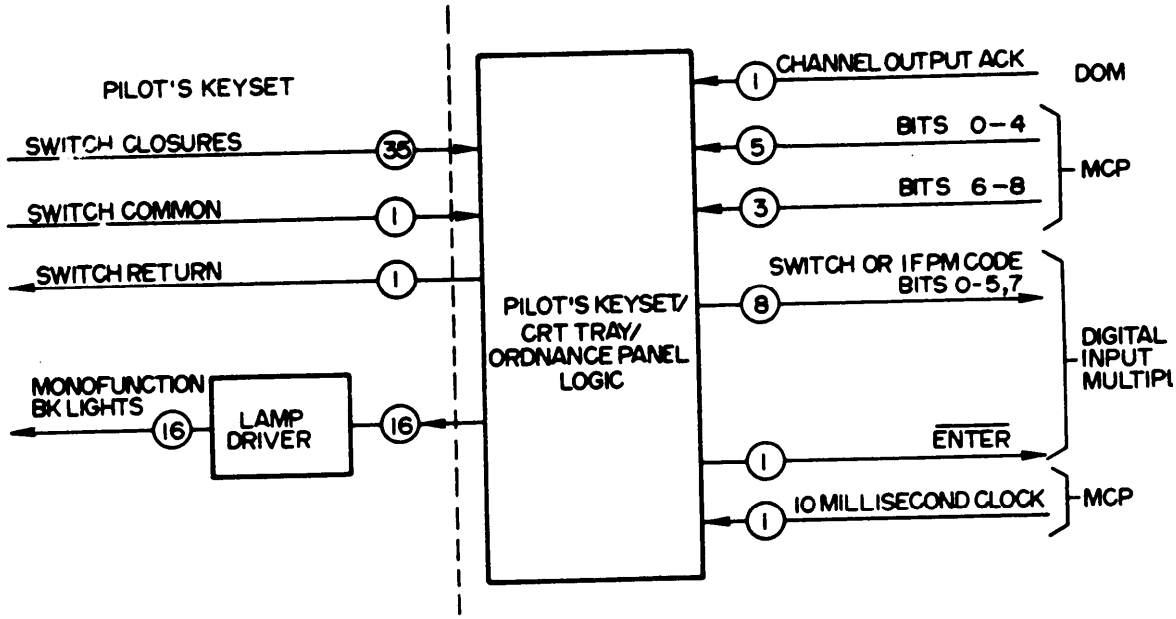


Figure 19. Pilot Keyset Logic, Functional Flow Diagram

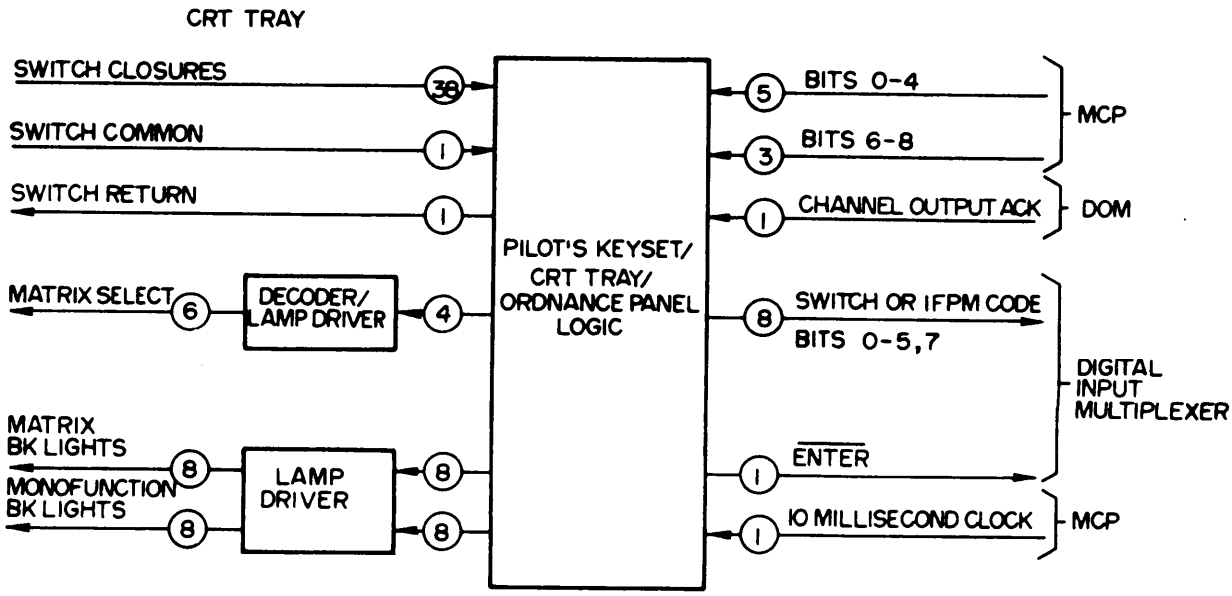


Figure 20. CRT Tray Logic, Functional Flow Diagram

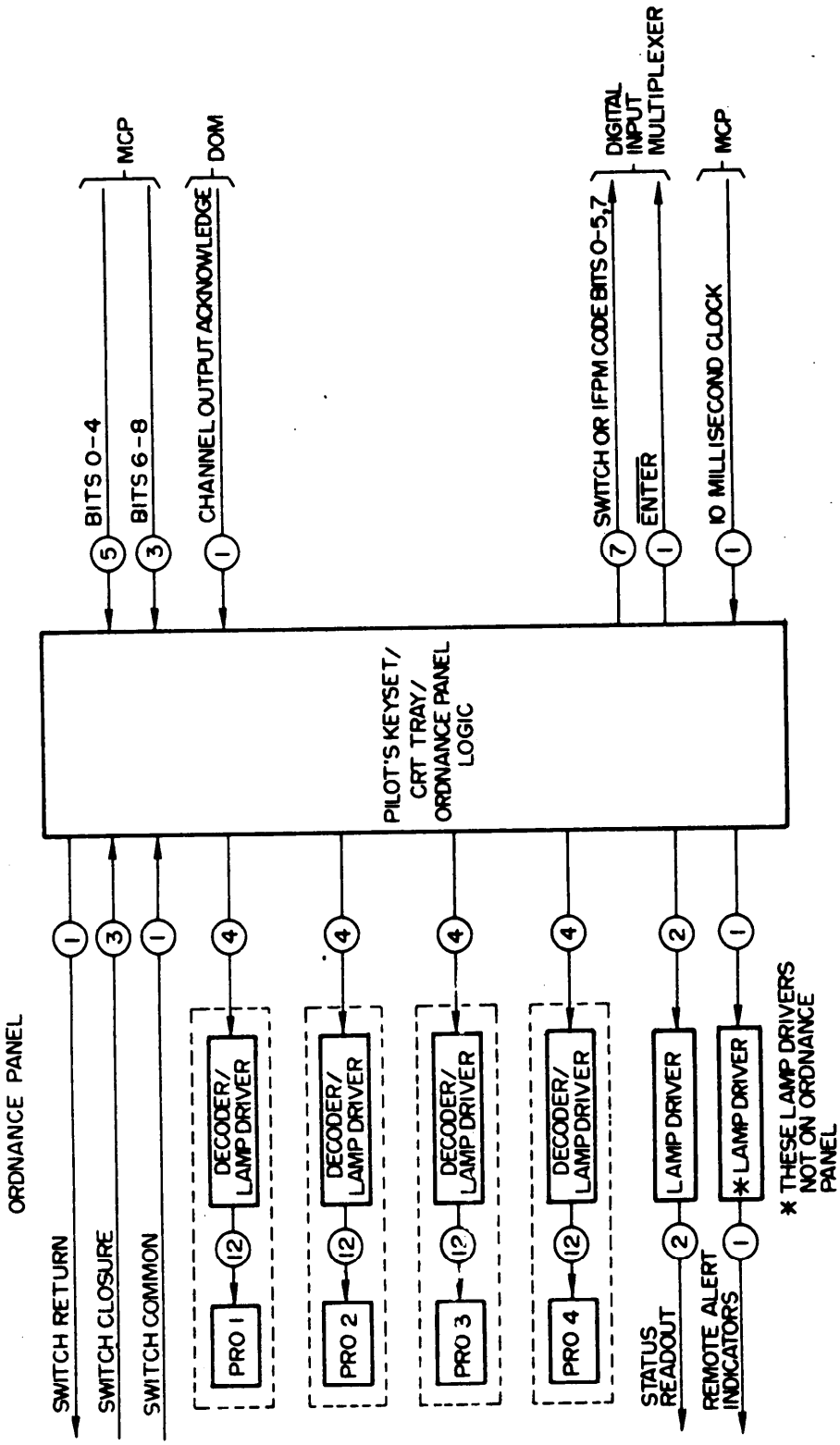


Figure 21. Ordnance Panel Logic, Functional Flow Diagram

3.5.1.4.6 Status Logic Subunit

3.5.1.4.6.1 Factional Description - The Status Logic subunit will transmit status information from the Navigation Sensors, Sonobuoy Receiver, Submarine Anomaly Detector and Camera System to the computer. The Status Logic Subunit will receive status information from the computer for the Navigation System. Figure 23 is a functional flow diagram of the Status Logic Subunit.

3.5.1.4.6.2 General Description - The Status Logic Subunit shall monitor status information from the following equipments:

(1) Navigation System

(2) Submarine Anomaly Detector (SAD)

(3) Sonobuoy Receiver

(4) Camera

The Status Logic Subunit shall transmit the status information to the computer whenever there is a change in the status information or when requested by the computer program. The Status Logic Subunit shall provide for expanding the monitoring to status information from other equipments.

The Status Logic Subunit shall also provide decoding and storage for status information from the computer (via the DOM) to the Navigation system.

3.5.1.4.6.3 Operating Requirements - Refer to the functional flow diagram (Figure 23).

3.5.1.4.6;3.1 Status Information to Computer via Digital Input Multiplexer The Status Logic Subunit shall utilize two DIM channels to transmit the status information to the computer.

The Status Logic Subunit shall be capable of receiving one SAD, twenty-one Navigation System (general) Status lines, one Camera System, ten Sonobuoy Receivers, two SUS system Status lines, one Drop Hold Status Line, one computer Track Status line and two Spare Status lines. This status data shall be transmitted to the computer over one of the two DIM channels assigned to the Logic Subunit. Since the DIM may transmit a maximum of 12 data bits to the computer, the status information shall be transmitted as six distinct *data* words to the computer via the DIM channel. Bit position coding shall be utilized in forming these data words; i.e. , *the* voltage level on each status line shall be represented by the logic level of a bit in one of the input data words. The status data shall be organized into the data words as defined in the word formats.

In addition to transmitting the status words to the computer, the Status Logic Subunit shall store each of the six words to serve as the criterion for detecting a change in status information. The Status Logic Subunit shall continue to compare each of *the* stored data words (representing the status information on which the computer program is operating) with the information on the status lines to detect a change in status. Whenever a status change is detected, the new data word(s) shall be transmitted to the computer and stored in the Status Logic Subunit.

The status data from the Submarine Anomaly Detector (SAD) shall be transmitted to the computer utilizing the second DIM channel assigned to the Status Logic Subunit. The Status Logic Subunit shall receive one SAD Status line. The status data from the system shall be transmitted as a single input word to the computer. In addition to transmitting the status word to the computer, the Status Logic Subunit shall store the word to serve as the criterion for detecting *a* change in status. The Status Logic Subunit shall continually compare the stored status word with the information on the status lines to detect *a change in* status. Whenever a status change is detected, the new data word shall be transmitted to the computer and stored in the Status Logic Subunit.

3.5.1.4.6.3.2 Timing for Input Data Words

(1) If a single status word changes (indicated by a permanent change in voltage on one or more of the status' lines associated with the word), the Status Logic Subunit shall raise the appropriate Enter line to the DIM and have status data available within 50 microseconds after the status change.

(2) If a number of the status words change simultaneously, the Enter line for the first status word shall be raised within 50 microseconds after the change. The Enter line associated with each succeeding word shall be raised within 100 microseconds after the trailing edge of the Channel Input Acknowledge signal for the previous word.

3.5.1.4.6.3.3 Status Information From Computer via Digital Output Multiplexer - The Status Logic Subunit shall interpret the output word received from the DOM to perform one of the following operations:

(1) Transmit any combination of the 1 to 5 status words, to the computer via the DIM. When more than one word is requested, the words shall be transmitted in succession to the computer. The order of transmission of the words is not significant.

(2) Store 10 status bits for the Navigation System. The 10 status bits are supplied as 10 lines to the Navigation System. Six lines shall drive relays and four lines shall drive line receivers,

3.5.1.4.6.3.4 Self Initialization - The equipment shall be self-initializing. When power is applied to the Status Logic subunit, no spurious data shall be transmitted to the computer and the subunit shall be ready for normal operation. When DC voltages and data to the subunit have stabilized, the subunit shall transmit either an interrupt on Channel 11 followed by five normal input status words to the computer via DIM Channel 7 (status words 1 through 5), or, five status words with no channel 11 interrupt.

3.5.1.4.6.4 Interface Requirements - Refer to the functional flow diagram for the Status Logic Subunit (Figure 23).

3.5.1.4.6.4.1 Format of Input Word to Digital Input Multiplexer from Status Logic for SAD Status Channel - Refer to Figure 22.

3.5.1.4.6.4.2 Format of Input Words to Digital Input -Multiplexer from Status Loic - The five status words to the Digital Input Multiplexer from the Status Logic are shown in Figures 24 through 28.

3.5.1.4.6.4.3 Format of Output Words from the Digital Output Multiplexer to the Status Logic Subunit - The Output Words are shown in Figures 29, 30 and 31.

3.5.1.4.6.4.4 Status Logic Subunit to Digital Input Multiplexer - Communications between the Logic Subunit and the DIM shall be in accordance with 3.5.1.4.1.

3.5. 1.4.6.4.5 Digital Output Multiplexer to Status Logic Subunit - Communications between the Status Logic Subunit and the DOM shall be in accordance with 3.5.1.4.2.

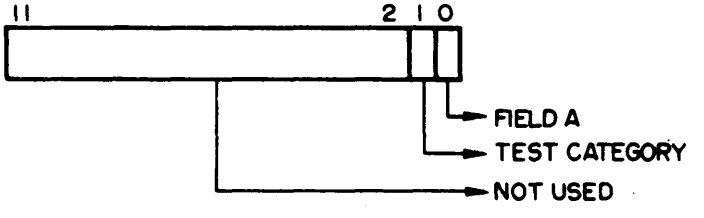


Figure 22. Format of Input Word to Digital Input Multiplexer from Status Logic for SAD Status Channel

3.5.1.4.6.4.6 Status Lines to Status Logic Subunit

3.5.1.4.6.4.6.1 Signal Characteristics

3.5.1.4.6.4.6.1.1 Status Word 1

(1) logical ''1"= 0.5-0.0Volt
logical "0" =4±1Volts

(2) The signals shall be transmitted over a twisted pair cable via data line drivers as per WR-101 Part II.

3.5.1.4.6.4.6.1.2 Status Word 2 to 5 and SAD

(1) logical "1" = 0.0+0.5-0.0Volt
logical ''0''=Open

(2) Twisted Pairs - The signals shall be transmitted over a twisted pair cable, one of which is the DPS signal return. This signal return shall not be tied to any other component.

(3) Up to 15 milliseconds of contact bounce noise may accompany a transition of any of the lines.

3.5.1.4.6.4.7 Status Lines from Status Logic Subunit to Navigation System

3.5.1.4.6.4.7.1 Signal Characteristics

3.5.1.4.6.4.7.1.1 Doppler

(1) logical "1" 0+0.5-0.0. Volt
logical "0" = 4 ± 1 Volts

(2) The signals shall be transmitted over a twisted pair cable via data line drivers per WR-101 Part II.

3.5.1.4.6.4.7.1.2 Other than Doppler

(1) logical "1" 0+0.5 - 0.0 Volt, Drive =250 MA
logical "0" Effectively Open

(2) The relays shall use the 12 V supplied by the DPS. This voltage shall not be tied to any other component.

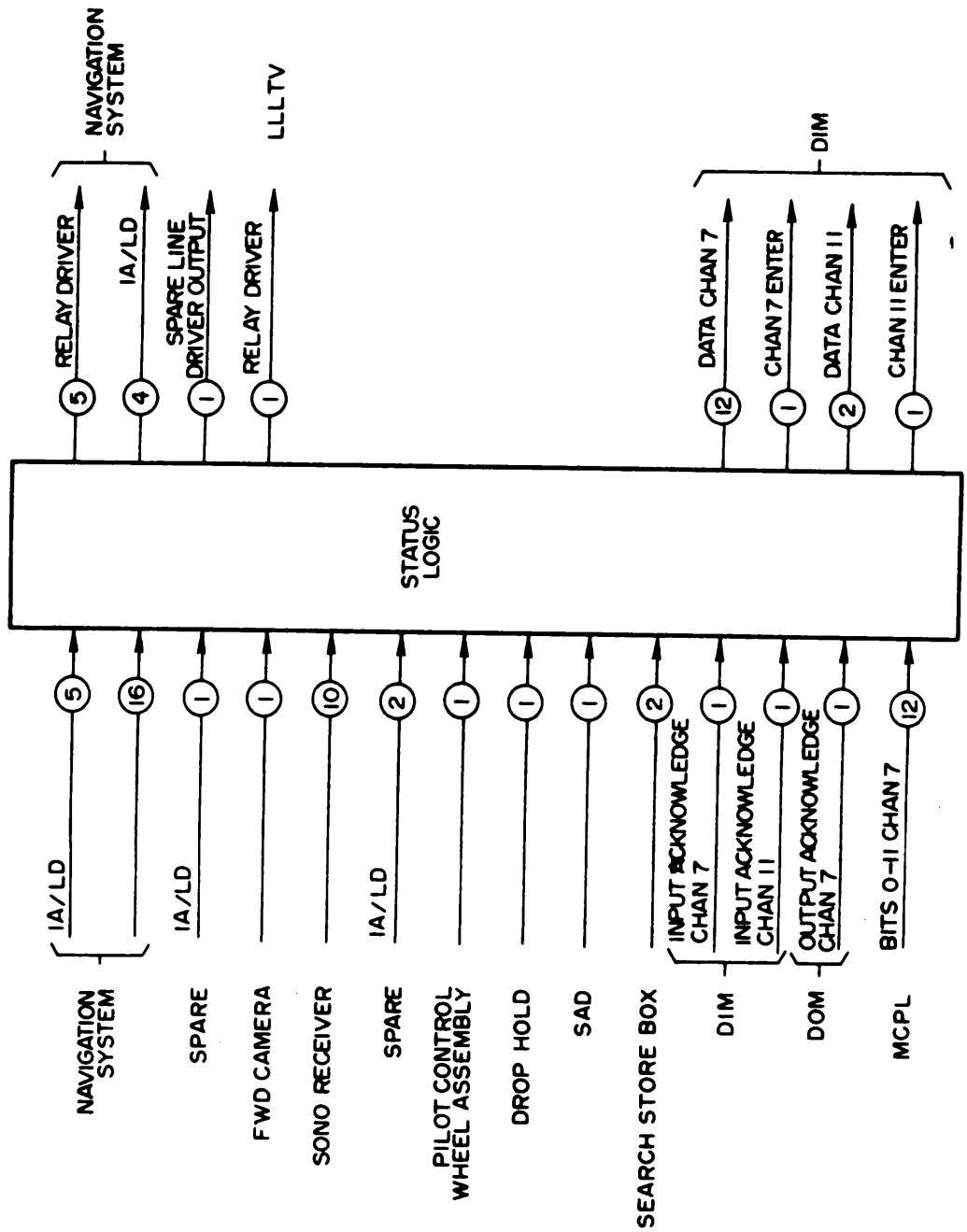


Figure 23. Status Logic Functional Flow Diagram

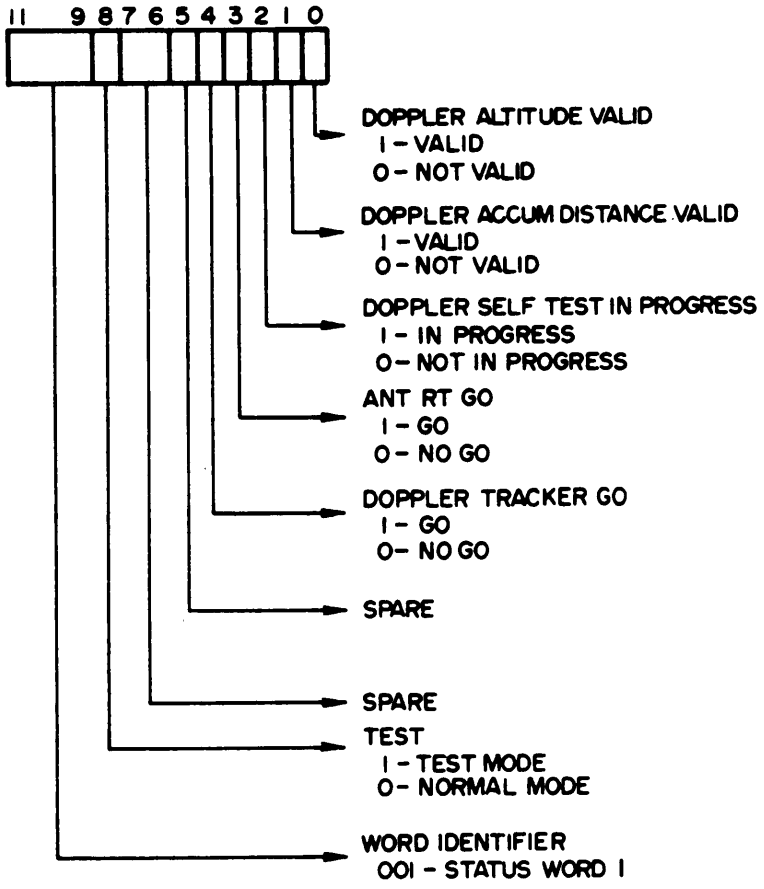


Figure 24. Format of Status Word 1 to Digital Input Multiplexer from Status Logic

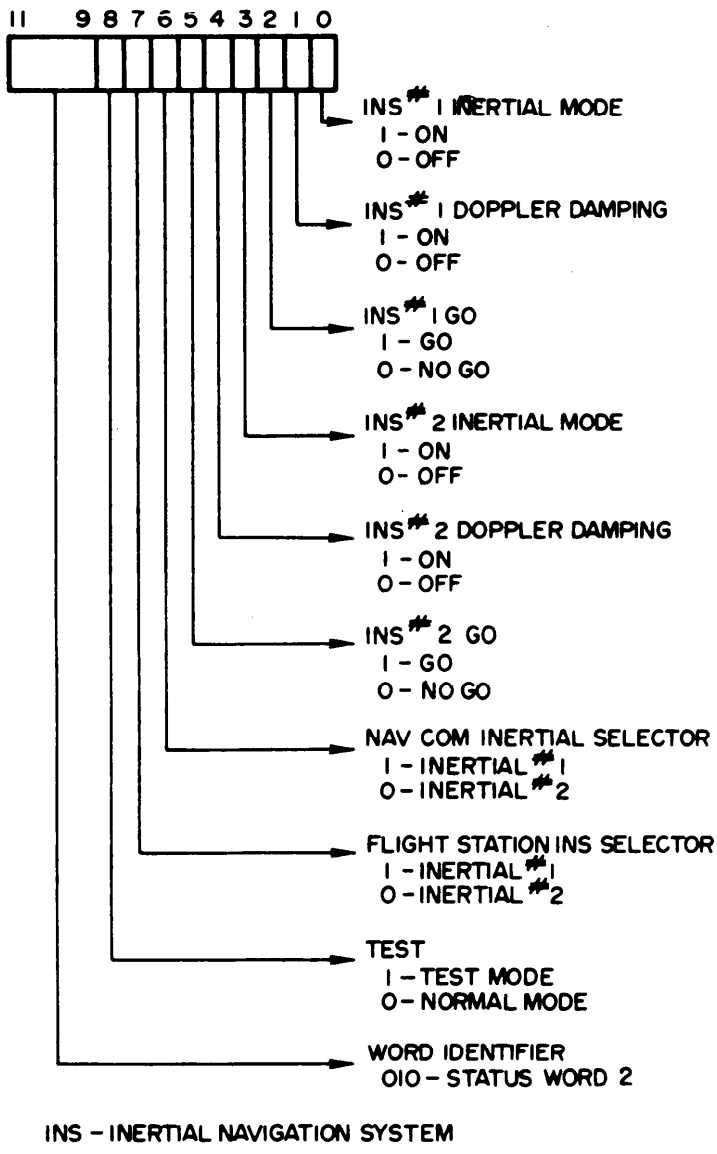


Figure 25. Format of Status Word 2 to Digital Input Multiplexer from Status Logic

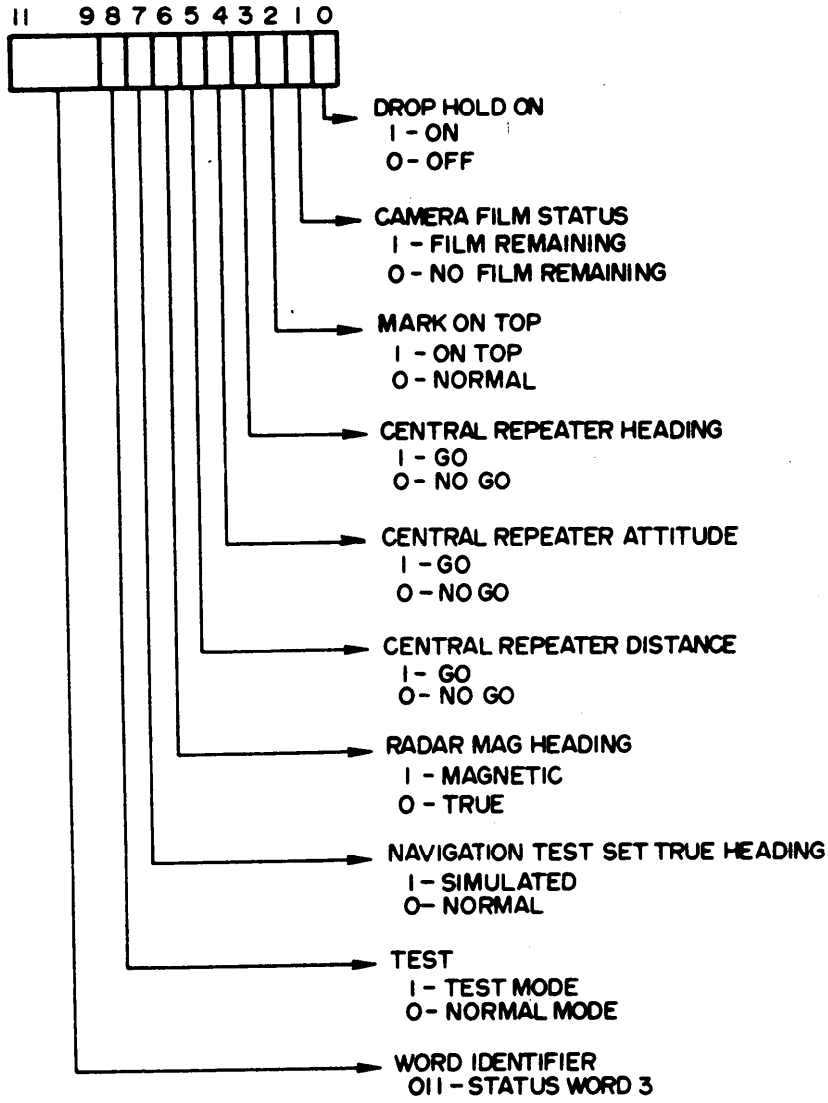


Figure 26. Format of Status Word 3 to Digital Input Multiplexer from Status Logic

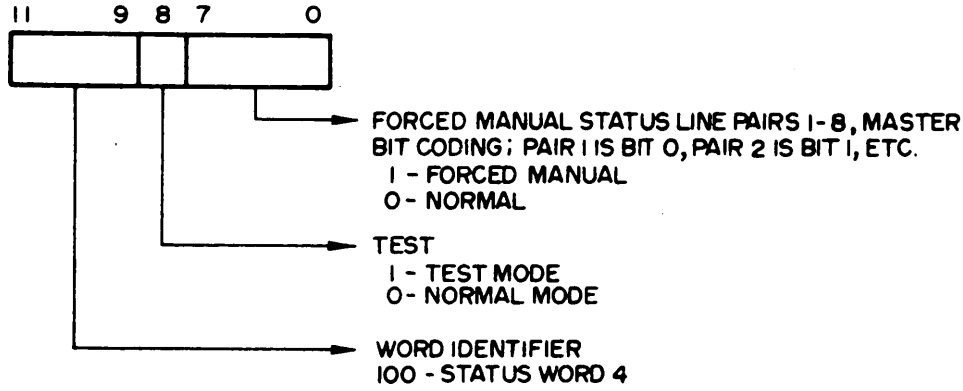


Figure 27. Format of Status Word 4 to Digital Input Multiplexer from Status Logic

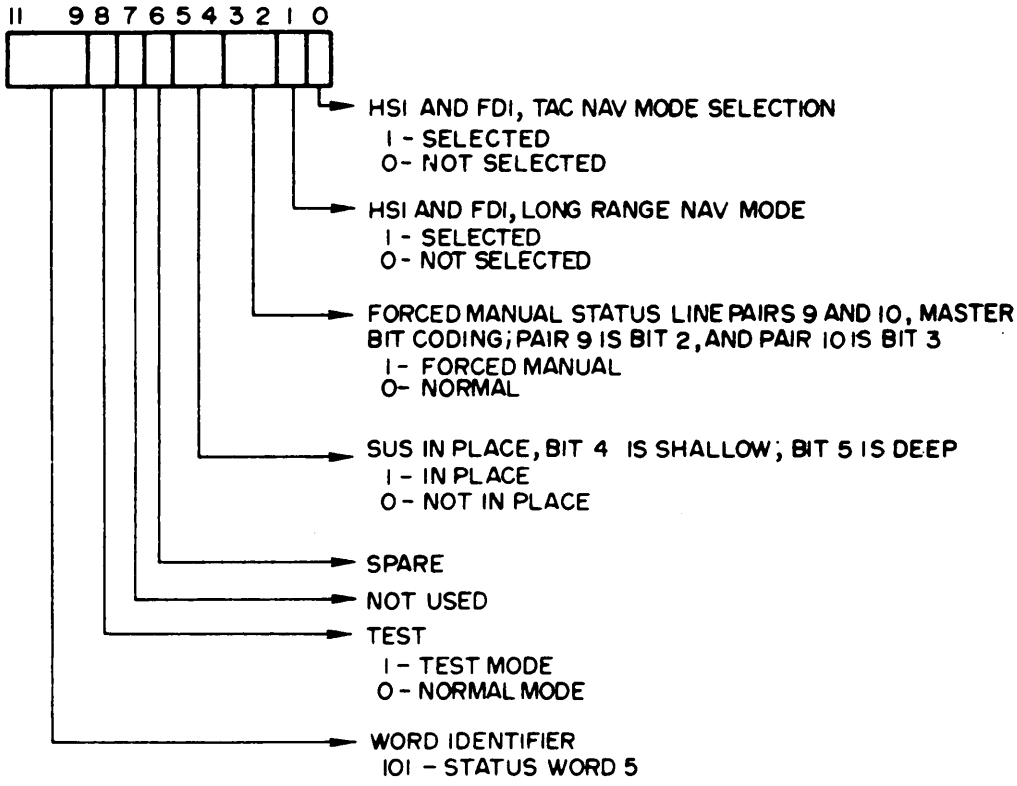


Figure 28. Format of Status Word 5 to Digital Input Multiplexer from Status Logic

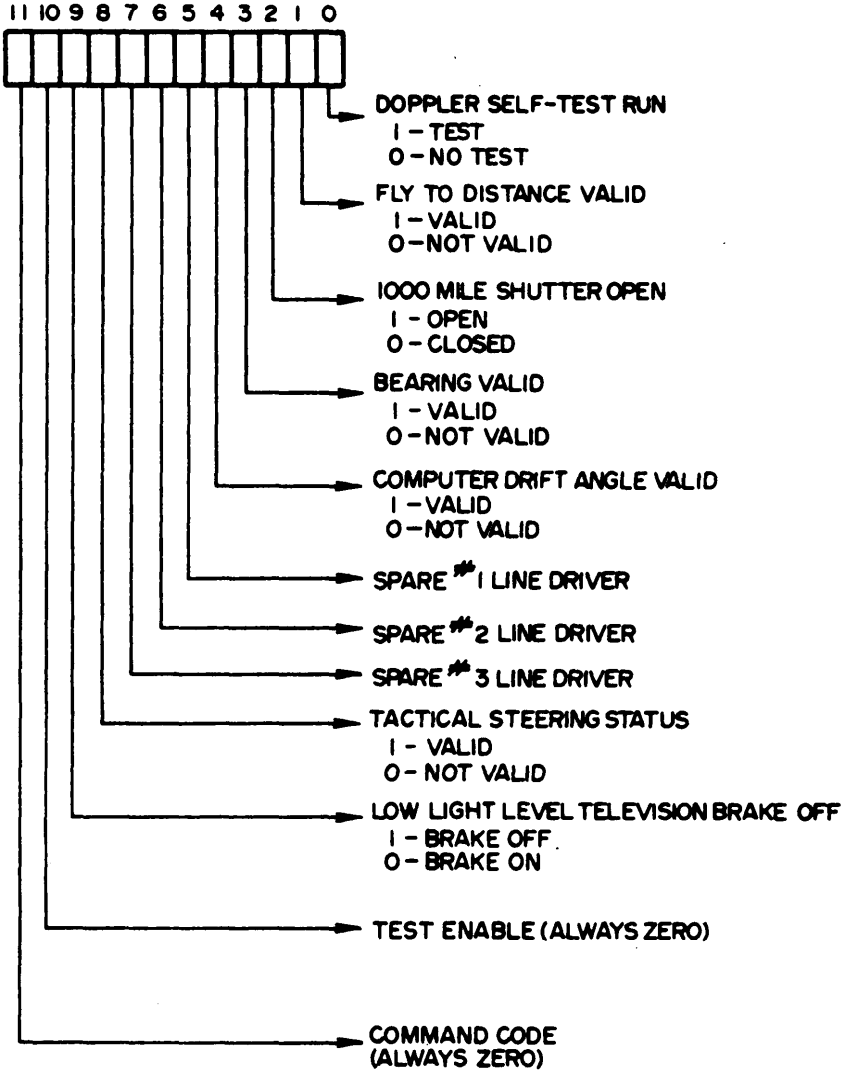


Figure 29. Format of Output Word 1 (Normal) from Digital Output Multiplexer to Status Logic Subunit

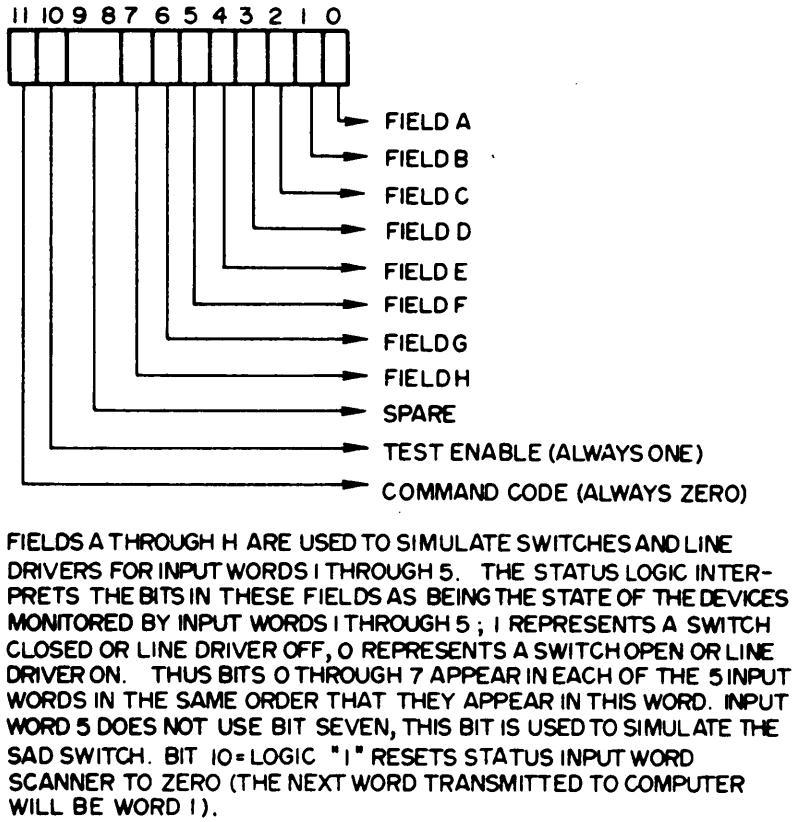
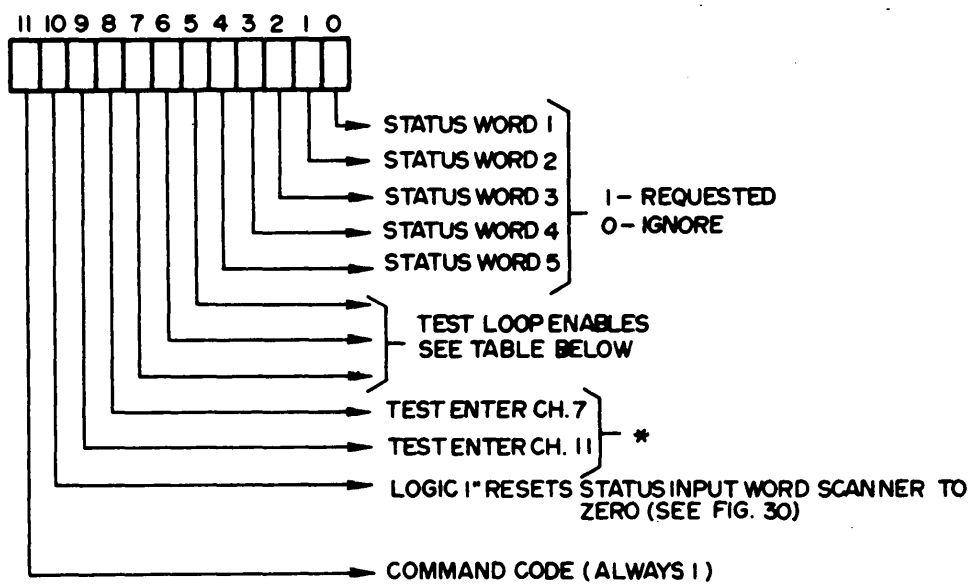


Figure 30. Format of Output Word 1 (Test) from Digital Output Multiplexer to Status Logic Subunit



* THESE LINES ARE USED TO RAISE ENTERS TO THE TWO DIM CHANNELS ASSIGNED TO THE STATUS LOGIC. THEY ARE USED TO ISOLATE MALFUNCTIONS DURING DIAGNOSTIC TESTING.
1 – ENTER, 0 – NO ENTER.

OUTPUT STATUS WORD 2 TEST LOOP ENABLES

7 6 5	TEST LOOP	
0 0 0	#0	SIMULATE ALL OPEN SWITCHES AND OFF LINE DRIVERS TO STATUS LOGIC (INCLUDING SAD LINE).
0 0 1	#1	SIMULATE ALL CLOSED SWITCHES TO STATUS LOGIC (INCLUDING SAD LINE).
0 1 0	#2	SIMULATE INDIVIDUAL CONTROL OF SWITCHES AND LINE DRIVERS TO THE STATUS LOGIC. (INCLUDING SAD LINE).
0 1 1	#3	NOT USED.
1 0 0	#4	DIAGNOSTIC INPUT WORDS USED TO ISOLATE MAL-FUNCTIONS BY TRANSMITTING SELECTED DATA TO THE COMPUTER. THE LOGIC IS DESIGNED TO ENABLE TEST LOOP 2 WHENEVER BIT 7 IS SET.
1 0 1	#5	
1 1 0	#6	
1 1 1	#7	

Figure 31. Format of Output Status Word 2 (Normal) from Digital Output Multiplexer to Status Logic Subunit

3.5.1.4.7 Sono Receiver Logic

3.5.1.4.7.1 Functional Description- All acoustic processors in the system receive their signals from the AN/ARR-72 sonobuoy receiver. The AN/ARR-72 is a 31 Channel, VHF, fixed tuned FM receiver. There are 19 processor and 1 Light Off Detector (LOD) channels that use sonobuoy data. These 20 channels can independently select any one of the 31 outputs from the RF receivers. Control for channel selection is accomplished in a 31 x 20 solid state matrix located in the Audio Matrix portion of the sonobuoy receiver. There are two modes of control as follows:

(1) Computer control via the SRL portion of the DPS.

(2) Manual control by acoustic sensor station operators.

The Sono Receiver Logic (SRL) shall upon command from the computer, provide channel selection control for all processor channels (20). In addition, when commanded by the computer, the SRL shall provide mode of operation control to the Sonobuoy Receiver group, allowing either Manual channel selection from the receiver control indicator panels or Auto channel selection.

The SRL shall be capable of monitoring Sonobuoy mode of operation, either Manual or Auto, and the RF channel selected for each processor and transmitting this information to the computer.

The SRL shall be capable of monitoring RF Level data from the Sonobuoy Receiver group and transmitting this data to the computer.

Upon receipt of a Forced Manual command from the Sonobuoy Receiver group, the SRL shall remove computer commanded control data from the receiver group but shall continue to monitor both mode and channel selection in the Sono Receiver. All computer commands shall be withheld from the Sono Receiver until such time as the Forced Manual control signal is removed.

The receiver group control mode is to be by processor paws, i.e., Auto, Manual or Forced Manual Mode can be established for any pre-determined pair of processor channels without affecting the mode of any other processor channels.

3.5.1.4.7.2 Operating Requirements

3.5.1.4.7.2.1 Computer Interface - The SRL shall function as *a* computer input-output interface device. Because of its low data rate, all data to and from the computer shall be via the Digital Input/Output Multiplexer.

3.5.1.4.7.2.1.1 Output - Data output from the computer via the Digital Output Multiplexer (DOM) shall determine the following functions:

(1) Selection of tuning mode, either manual or computer (automatic) *for* Sonobuoy Receiver, Processor channel pairs.

(2) Selection of RF receivers (1 through 31) for application to acoustic processor channels.

(3) Selection of acoustic processor channel to which RF receiver selection codes are to be applied.

(4) Selection of SRL input data to the computer.

NOTE

For purposes of this discussion, control of the Light Off Detector (LOD) channel in the receiver group will be treated as any other processor channel unless otherwise noted.

NOTE

To insure minimum receiver select time during computer LOD and select operations, components used to filter and delay manual select inputs to the SRL shall not have any effect on the automatic select data.

3.5.1.4.7.2.1.2 Input - Input data to the computer shall be transferred via the DIM. It is selected in (4) above, and is of three types:

(1) Manual Turning Data - This information is required to cor - relate acoustic processor data with operating sonobuoys whenever the associated AN/ARR-72 receiver is in the Manual mode.

(2) RF Carrier Level Data - This information is required to select clear RF channels prior to sonobuoy launch and to confirm buoy operation following launch.

(3) Operating Mode - Computer selected Auto or Manual mode status or Forced Manual mode status shall be passed through the SRL. The Forced Manual Mode indi- cation also interfaces with the Status Logic.

NOTE

The Manual tuning data and operating modes (1) and (3) above are monitored through the same gates that are used for In- Flight Performance Monitoring (IFPM).

3.5.1.4.7.2.2 Receiver Interface - See Figures 32 through 34.

3.5.1.4.7.2.2.1 Sono Receiver Logic Outputs - The SRL shall output to the receiver group the following:

(1) Six-bit parallel output in BCD format to each of 20 processor channels, for channel selection control with data described in 3.5.1.4.7.2.1.1.

(2) One Auto/Manual Select line for each group of two six-bit parallel outputs.

(3) One RF Request line via twisted wire pair per Figure 35. Timing of the RF request pulse shall be concurrent with strobing of the Channel Select Storage Register

3.5.1.4.7.2.2.2 Sono Receiver Logic Inputs - The SRL shall accept the following from the receiver:

(1) Two-bit parallel twisted pair inputs representative of RF carrier level.

(2) Twenty sets of six-bit parallel Selection codes in BCD format from the receiver group for purposes of manual charnel selection.

(3) One bit parallel twisted pair input from the receiver, indi - eating completion of the A-D conversion function in the LOD Loop. This bit to be interpreted as LOD valid.

(4) Ten Forced Manual Mode indicator lines (one for each pair of processor channels). This line shall be at O V when the Forced Manual Mode is in effect.

3.5.1.4.7.2.2.3 Form of Data Transmission - Channel selection data between the SRL and the receiver shall be in BCD Format. Data on the control lines shall be at a continuous and uninterrupted level changing only upon receipt of proper command from the computer or upon input from manual control. Channel selection data shall be stored in the SRL in the Auto Mode.

3.5.1.4.7.2.2.4 Logic Levels - All logic levels at the Sono Receiver/SRL Interface shall comply with Figure 36.

3.5.1.4.7.2.2.5 Turning Data Indication - It is a systems requirement that the sensor station operator be able to monitor the computer select channel when in the Auto mode. This is accomplished by PRO devices that are part of the sonobuoy receiver group control indicator panels. These PRO's are connected in parallel with the receiver group input and hence in parallel with the SRL output. The combination receiver input, and PRO input collectively form an ORing circuit capable of being driven from the SRL or the maintenance control panel. See Figure 33 for typical interface.

3.5.1.4.7.2.2.6 Sono Receiver Logic Output Drive Capability

(1) Output drivers shall be capable of supplying to external loads no more than 25 microampere.

(2) Output driver circuits shall be capable of accepting from external sources, a maximum of 5 ma.

3.5.1.4.7.2.2.7 Sono Receiver Logic Input Gate Capability - Input gates shall require a maximum of 2 ma from external sources.

3.5.1.4.7.2.2.8 Light Off Detector Interface - The SRL Sonobuoy subunit shall receive an input from the receiver group that is descriptive of RF level information. The input will consist of three parallel bits. 'IWO bits will define RF carrier level, the third bit will indicate when level information from the receiver is valid, and is designated as an LOD Valid. Upon receipt of an LOD Valid signal from the AN/ARR-72 receiver, the RF level data shall be transmitted to the computer.

3.5.1.4.7.2.2.9 Mode Select Drivers - For each of the ten pairs of data line output groups from a subunit to the receiver there shall be one line for establishing Auto/Manual Mode control for the associated pair of processor channels. This line shall provide a 521.5 volt level to the processor pair control indicator panel in the Manual mode of operation. It shall provide 0.0 + 0.5- 0.0V to the processor control indicator panel when the Auto mode of operation is desired.

3.5.1.4.7.2.2.10 Manual Mode Output - When any pair of channels is in the Computer Selected Manual mode, the circuitry shall be so arranged that the stored SRL data associated with that pair is inhibited, thereby allowing each of the output data lines to be controlled, on a line by line basis, by the Manual Selectors in the receiver group.

3.5.1.4.7.3 Test Modes - All testing shall be performed using data and control signals from the Maintenance Control Panel described in 3.5.1.4.9.

3.5.1.4.7.3.1 IFPM - In-flight performance monitoring capability shall be provided in the SRL to the extent that any loss of functional capability may be detected and processed by the computer as a malfunction.

3.5.1.4.7.4 Interface Requirements

3.5.1.4.7.4.1 Output Data Transfer - The SRL shall receive data from the computer via the Digital Output Multiplexer (DOM). Communications between the SRL and the DOM shall be in accordance with 3.5.1.4.2.

3.5.1.4.7.4.1.1 Output Word Formats - The output word formats are shown in Figures 37 through 40. Detailed descriptions are given in the following paragraphs.

3.5.1.4.7.4.1.1,1 Receiver/Processor Select (See Figure 37) - This word, received from the DOM, provides control data relative to the processor channel to be switched and the RF receiver to be applied to that processor channel.

(1) Bit 11- Interrogate bit and for this word is always set to O.

(2) Bits 10 through 6- identify the processor channel to be switched. only octal codes 00 through 23 are legal for these bit positions. These codes correspond to processors decimal 0 through 19 respectively.

(3) Bits 5 through 0 - identify the RF channel applied to the processor. Only BCD codes 01 through 31 are legal for these bit positions. These BCD codes correspond to receivers decimal 1 through 31 respectively.

Upon receipt of octal code 23, an RF request shall be sent to the LOD section of the AN/ARR-72 receiver, indicating that RF level data is being requested.

3.5.1.4.7.4.1.1.2 Mode Select (Auto/Manual) (See Figure 38) - This word, received from the DOM, provides control data relative to the Mode of operation, either Auto or Manual, for 10 pairs of processors.

(1) Bit 11 -Interrogate bit and for this word is always set to 0.

(2) Bits 10 through 6- Identify the groups of processor pairs to be mode controlled. There are two groups of five processor pairs. Only octal codes 24 and 25 are legal for these bit positions. Octal code 24 identifies processor pair group 1. Octal code 25 identifies processor pair group 2.

(3) Bit 5- Not used in this word to convey data and is designated as spare.

(4) Bits 4 through 0 - Provide, by master bit, control data concerning the mode (Auto or Manual) for each of processor pairs 1 through 10. A bit set to logical “O” dictates the Auto mode and a bit set to logical” 1“ dictates the Manual mode. If bits 10 through 6 equal octal 24, then bit 4 corresponds to pair 9 and bits 3 through 0 correspond to pairs 4 through 1 respec - tively. If bits 10 through 6 equal octal 25, then bit 4 corresponds to pair 10 and bits 3 through O correspond to pairs 8 through 5 respectively. Mode control data is provided for all processor pairs in a group at one time.

3.5.1.4.7.4.1.1.3 Processor/Receiver Status Request (See Figure 39) - This word, from the DOM, is used to request information concerning the receiver channel that is applied to various processor charnels.

(1) Bit 11- Interrogate bit and for this word is always set to 1.

(2) Bits 10 through 6- Define the processor channel of interest. Only octal codes 00 through 23 are legal for these bit positions. These octal codes correspond to processors decimal 0 through 19 respectively.

(3) Bits 5 through 0 - not used in this word and are designated as spare.

3.5.1.4.7.4.1.1.4 Mode Status Request (See Figure 40) - This word, from the DOM, is used to request information concerning the mode of operation of processor channel pairs.

(1) Bit 11- Interrogate bit and for this word is always set to 1.

(2) Bits 10 through 6 - identify the groups of processor pairs to be mode monitored. There are two groups of five processor pairs. Only octal codes 24 and 25 are legal for these bit positions. Octal code 24 selects group 1 of the processor pairs. Octal code 25 selects group 2 of the processor pairs.

(3) Bits 5 through 0 - Not used in this word and are designated as spare.

In response to this instruction, all channels in any one group are to be monitored simultaneously.

3.51.4.7.4.2 Input Data Transfer - The SRL shall transmit data to the computer via the DIM. Communications between the SRL and the DIM shall be in accordance with 3.5.1.4.1.

3.5.1.4.7.4.2.1 Input Word Formats - The input word formats are shown in Figures 42 and 43. Detailed descriptions are given in the following paragraphs.

3.5.1.4.7.4.2.1.1 Processor Status (See Figure 41) - This word provides to the DIM, monitoring data relative to the RF receiver channel selected for any of the processor channels.

(1) Bit 11- RF Monitor bit and is always set to 0.

(2) Bits 10 through 6- identify the processor channel being monitored. Only octal codes 00 through 23 are legal for this word.

These octal codes correspond to processor channels decimal O through 19 respectively.

(3) Bits 5 through O - identify the RF channel applied to the processor channel. Only BCD codes 01 through 31 are legal for these bit positions. These BCD codes correspond to receiver channels decimal 1 through 31 respectively.

3.5.1.4.7.4.2.1.2 RF Level Status (See Figure 42) - This word provides to the DIM, monitoring data relative to RF carrier level on any 1 of 31 VHF sonobuoy frequencies.

(1) Bit 11- RF Monitor bit and for this word is always set to 1.

(2) Bits 10 through 8- Designated as spare and are not used to convey data.

(3) Bits 7 and 6- Provide the indication of RF level.

(4) Bits 5 through 0 - Identify the RF channel being monitored. Only BCD codes 01 through 31 are legal for these bit positions. These codes correspond to RF channels decimal 1 through 31 respectively.

3.5.1.4.7.4.2.1.3 Mode Status (See Figure 43) - This word provides to the DIM, monitoring data relative to the Auto/Manual mode of operation of processor channel pairs.

(1) Bit 11- RF Monitor bit and for this word is always set to O.

(2) Bits 10 through 6 - Identify which group of Mode monitor lines is being monitored. There are two groups of five Mode monitor lines. Group 1 is associated with the four processor pairs at Sensor Station 1 and the processor pair at Sensor Station 3. Group 2 is associated with the four processor pairs at Sensor Station 2, the LOD, and TACCO station. Only octal codes 24 and 25 are legal for these bit positions. Octal code 24 identifies Mode monitor group 1. Octal code 25 identifies Mode monitor group 2.

(3) Bit 5- Not used and is designated as spare.

(4) Bits 4 through 0- Provide, by master bit, data concerning the Mode (Auto or Manual) of each of the processor pairs 1 through 10. A bit set to logical "O" dictates the Auto Mode and a bit set to logical "1" indicates the Manual Mode. If bits 10 through 6 equal octal 24, then bit 4 corresponds to pair 9 and "bits 3 through 0 correspond to pairs 4 through 1 respectively. If bits 10 through 6 equal octal 25, then bit 4 corresponds to pair 10 and bits 3 through 0 correspond to pairs 8 through 5 respectively. The Mode status of all processor pairs in a group is provided at one time.

3.5.1.4.7.5 Channel Numbering and Grouping

3.5.1.4.7.5.1 Grouping by Pairs - It shall be a requirement that the SRL provide for control and monitoring of 20 channels, arranged in groups of two, with each group having arias-sociated Auto/Manual Select line output to the associated receiver group, processor pair, and a Forced Manual input line from the receiver group processor pair.

3.5.1.4.7.5.2 Channel Numbering Scheme - The output channels to the sono receiver shall be numbered O through 19 and shall be arranged in successively numbered pairs; i. e, , channels O and 1 form pair 1, channels 2 and 3 form pair 2, etc.

3.5.1.4.7.5.3 Mode Control and Monitor Groups

(1) Group 1 shall consist. of output channel pairs 1 through 4 and 9 (output charnels O through 7, 16 and 17).

(2) Group 2 shall consist of output channel pairs 5 through 8 and 10 (output charnels 8 through 15, 18 and 19).

.

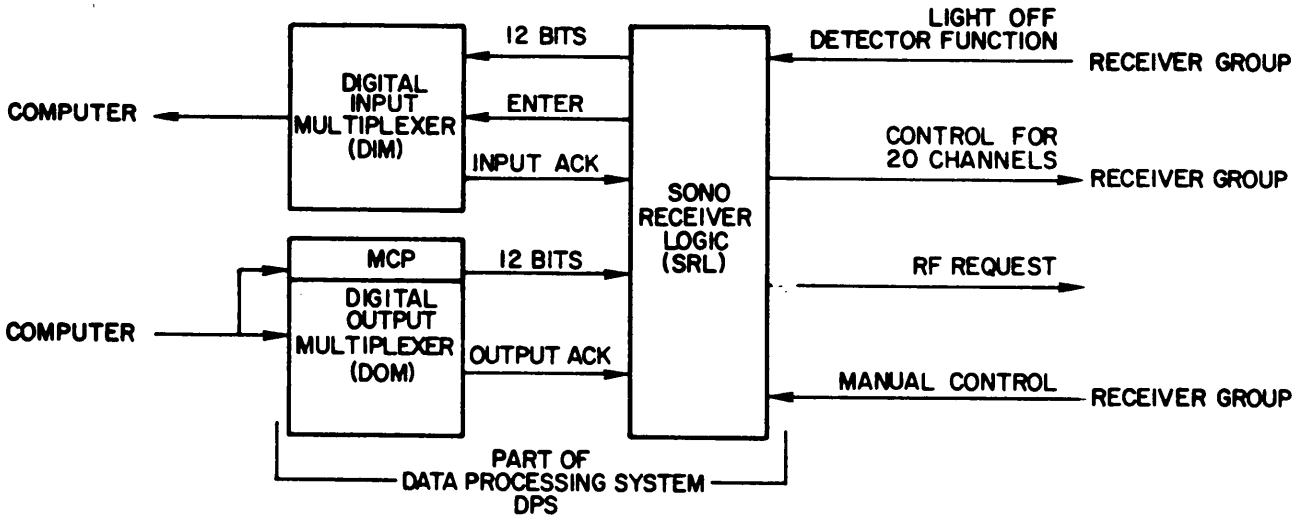


Figure 32. Sonobuoy Receiver Logic Input/Output Interface, Block Diagram

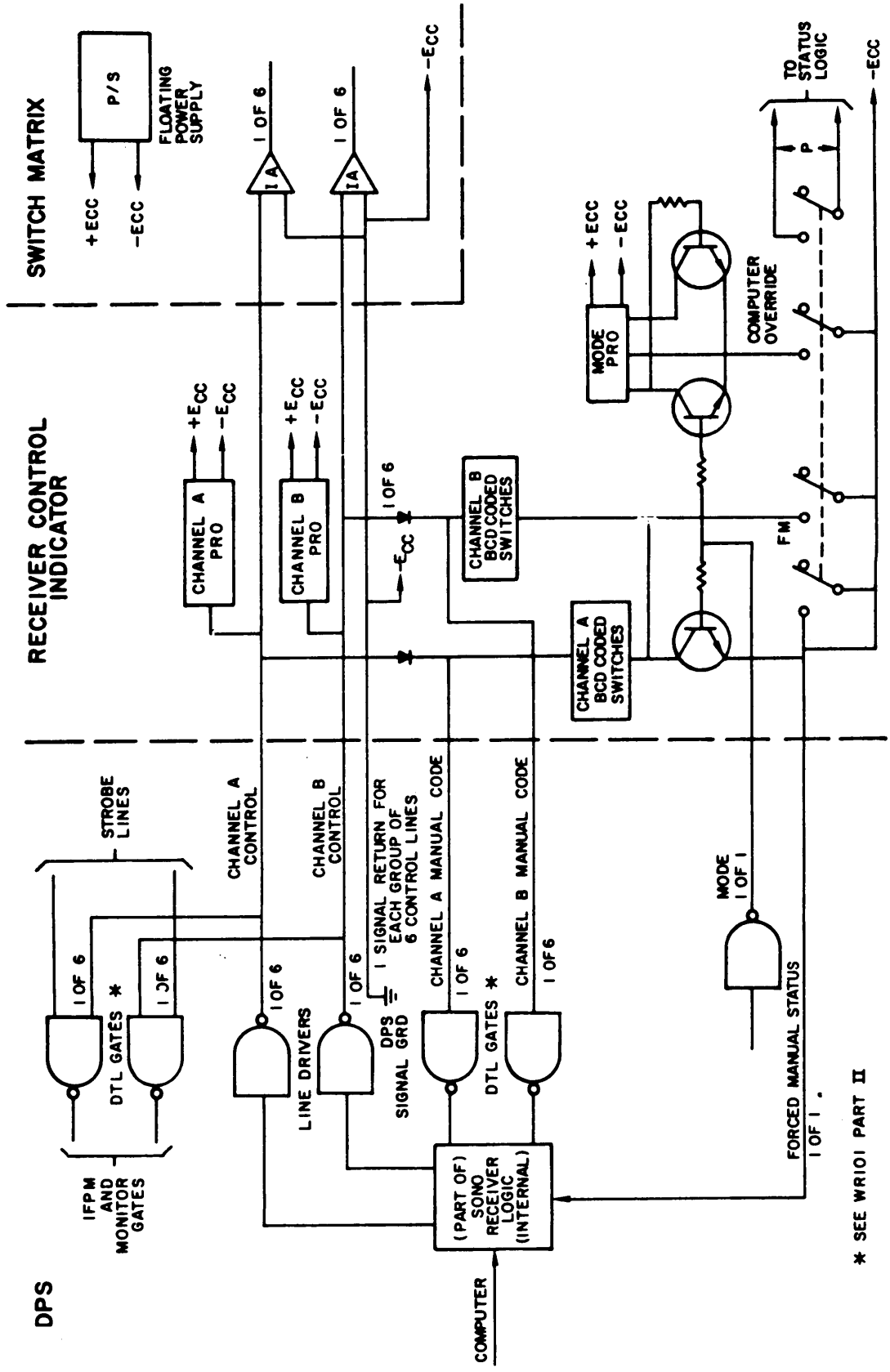


Figure 33. Sonobuoy Receiver Logic/Sonobuoy Receiver Interface Detail for Two-Channel Control

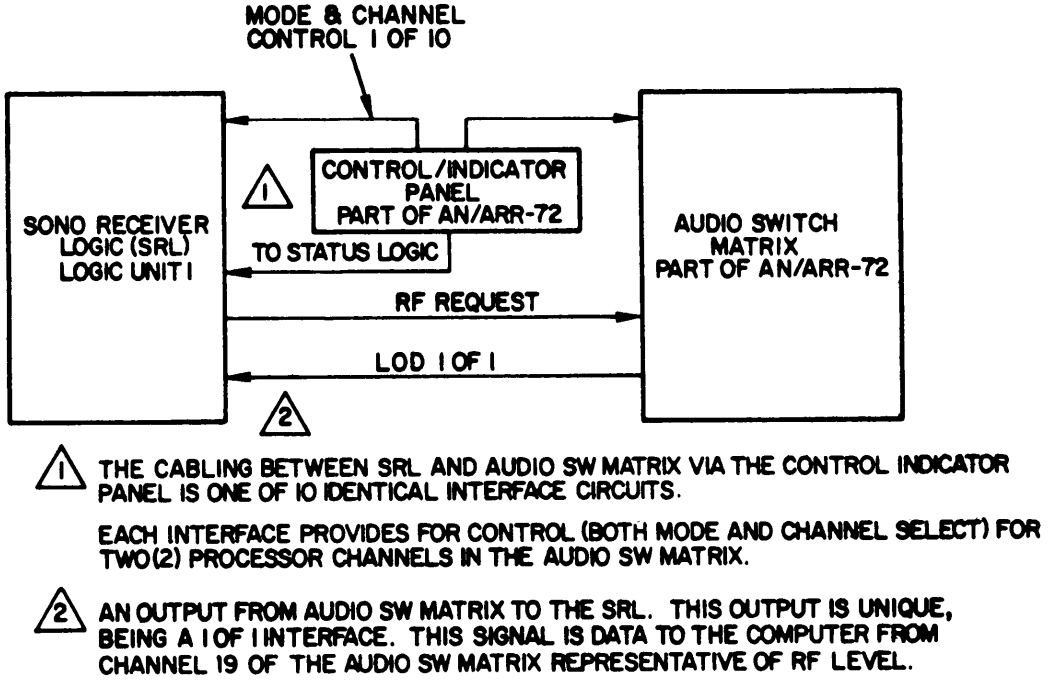


Figure 34. Sonobuoy Receiver Logic/Sonobuoy Receiver Interface

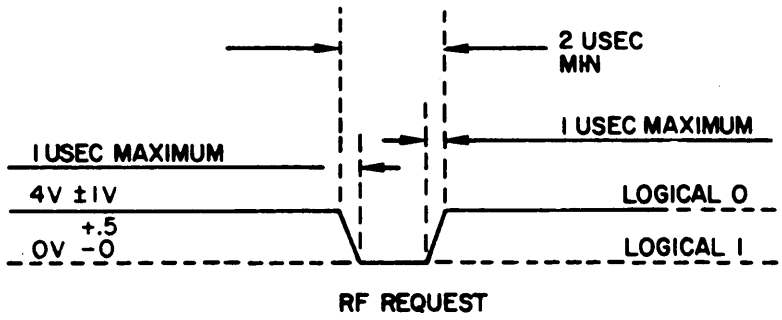


Figure 35. RF Request

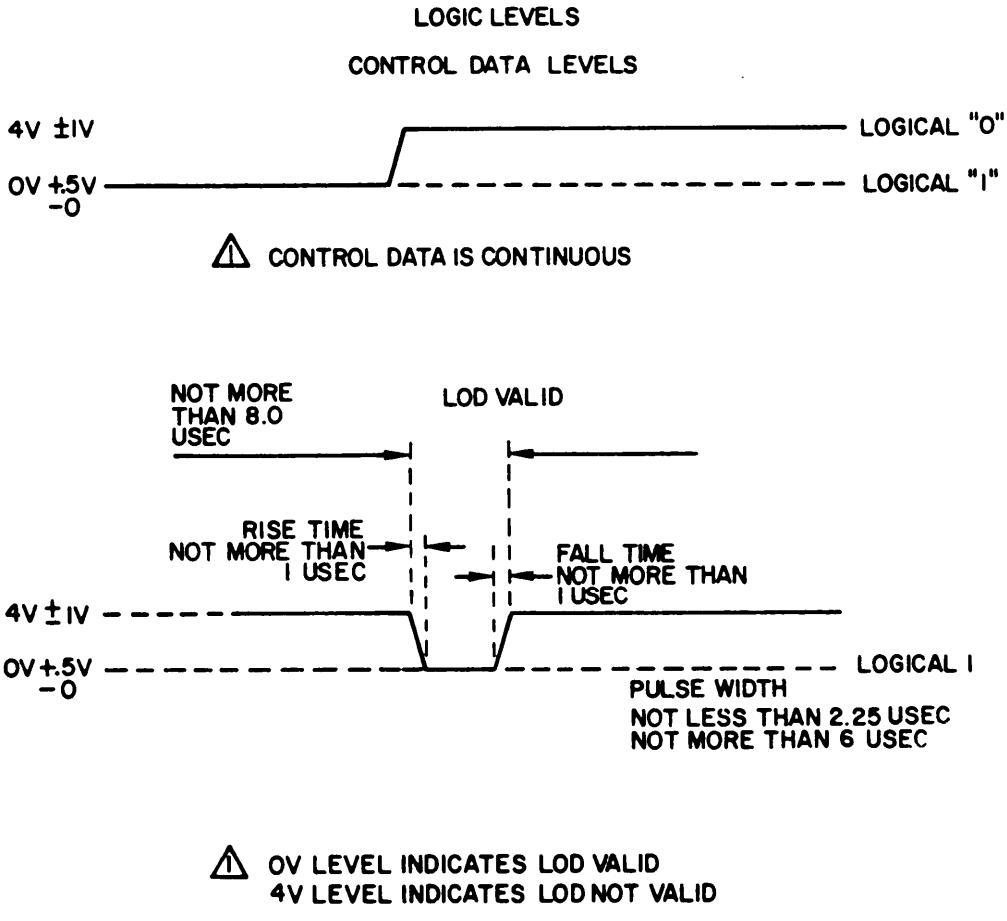


Figure 36: Sonobuoy Receiver Logic/Sonobuoy Receiver Interface Logic Levels

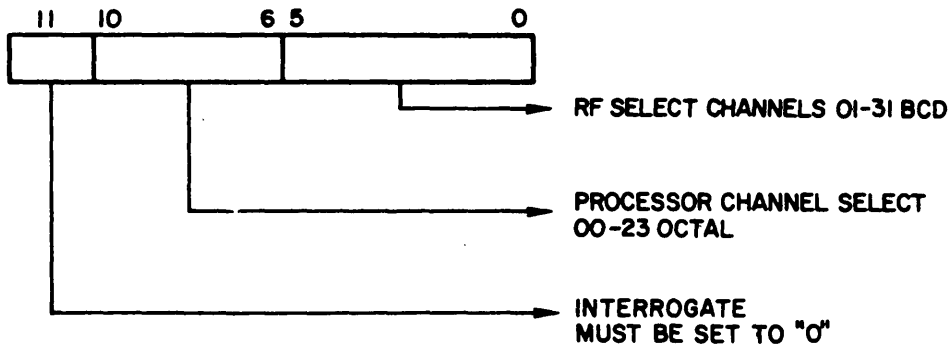


Figure 37. Format of Receiver/Processor Select Output Word to Sonobuoy Receiver Logic from Digital Output Multiplexer

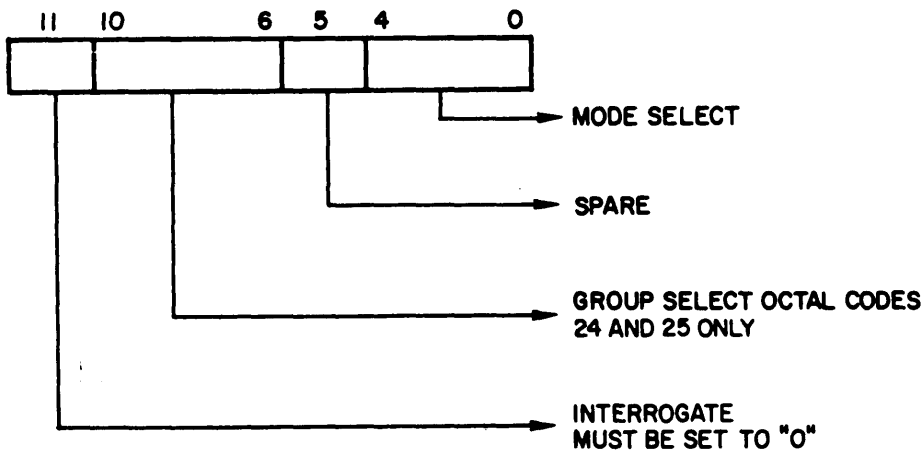


Figure 38. Format of Mode Select (Auto/Manual) Output Word to Sonobuoylteceiver Logic from Digital Output Multiplexer

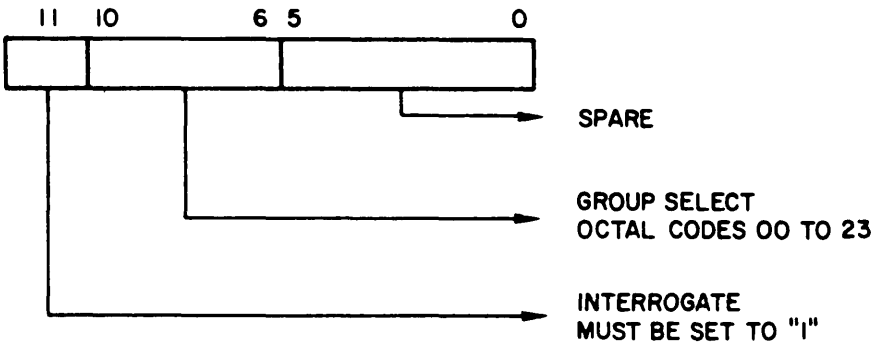


Figure 39. Format of Processor/RF Channel Status Request Output Word to Sonobuoy Receiver Logic from Digital Output Multiplexer

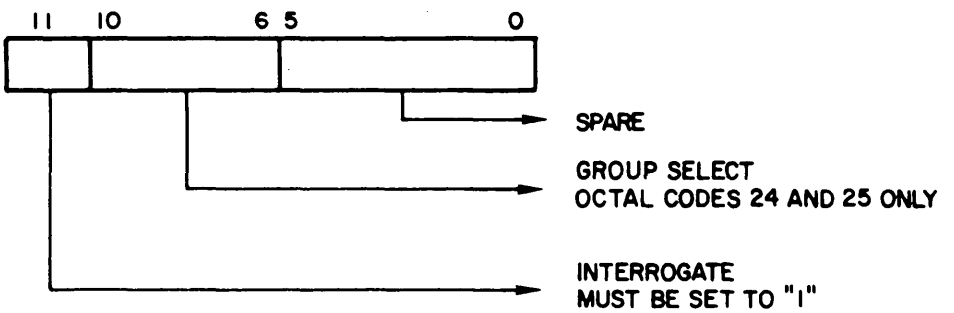


Figure 40'. Format of Mode Status Request Output Word to Sonobuoy Receiver Logic from Digital Output Multiplexer

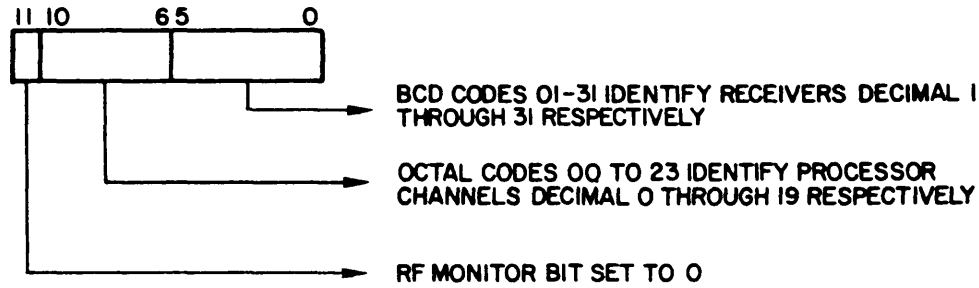


Figure 41. Format of Processor Status Input Word to Digital Input Multiplexer from, Sonobuoy Receiver Logic

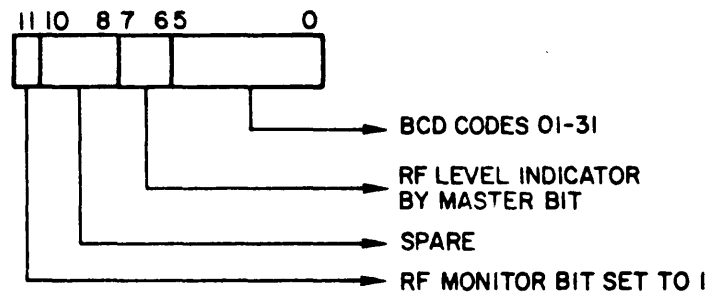


Figure 42. Format of RF Level Status (LOD) Input Word to Digital Input Multiplexer from Sonobuoy Receiver Logic

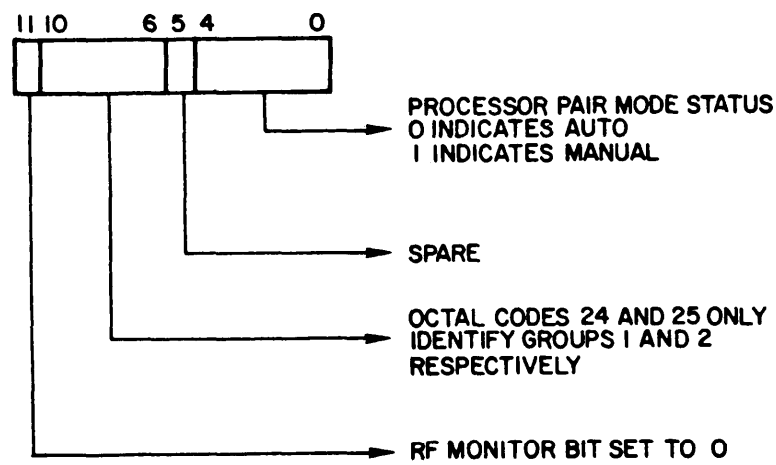


Figure 43. Format of Mode Status Input Word to Digital Input Multiplexer from Sonobuoy Receiver Logic

3.5.1.4.8 Auxiliary Readout Display (ARO) Logic

3.5.1.4.8.1 Functional Description - The ARO Logic Subunit shall be designed to accept computer generated digital information and convert it to a form suitable for driving two five-inch ARO "CHARACTRON" displays for the purpose of presenting alphanumeric tableaux to the Tactical Coordinator and NAVCOM operators as shown in Figure 45. Figure 46 is a functional flow diagram of the ARO Logic.

3.5.1.4.8.2 General Description - The ARO Logic Subunit receives signals from the digital computer through the Maintenance Control Panel, converts and controls the data for the correct formatting and timing and transmits the proper signals to the ARO Display for presentation on the CRT screens. Each computer data word contains the information to print two alphanumeric characters on each ARO display screen. Each character requires six binary bits. The ARO Display Logic provides for the positioning of the characters on the ARO. The available display positions are to be 20 rows of 20 characters, or 400 total characters per ARO display.

3.5.1.4.8.3 Operating Requirements

3.5.1.4.8.3.1 Interface - Provide the interface for the transfer of digital information from the Computer via the Maintenance Control Panel to the ARO Displays. The ARO Logic Subunit also provides data to the computer for test purposes.

3.5.1.4.8.3.2 Storage - Provide storage of received digital character information while the information is being displayed by the ARO Displays.

3.5.1.4.8.3.3 Signal Generator - The ARO Logic shall provide the ARO Display with character selection, deflection and unblank signals.

3.5.1.4.8.3.4 Modes of Operation - The ARO Logic shall provide capability of three modes of operation by the setting of the ARO Mode switch located on the Maintenance Control Panel.

3.5.1.4.8.3.4.1 On Line Mode - With the ARO Mode switch in the "On Line" Position, the ARO Logic shall be under the control of the computer. The timing of the data transfer, and the "page" or frame information is under control of the logic. Operations performed by the logic are: receiving data from the computer, providing information to the ARO Displays for displaying a character, advancing the position counters and upon receipt of an End of Data command resetting the position counters and stopping operation to wait for a 33.3 Hz line sync signal.

3.5.1.4.8.3.4.2 Test 1- With the ARO Mode switch in the "Test 1" position the 20 x 20 character test pattern shown in Figure 47 shall be presented on both ARO Displays. This pattern is used to set the ARO Deflection and Reference gain controls, and as a check of the logic in the ARO Logic Subunit and of the ARO Displays.

3.5.1.4.8.3.4.3 Test 2 - With the ARO Mode switch in the "Test 2" position, the matrix test pattern shown in Figure 48 shall be presented in the upper left hand corner of the 20 x 20 Matrix on both ARO Displays. This pattern is used for a logic check of the Subunit and the setting of the selection gain and centering controls on the ARO Displays.

3.5.1.4.8.4 Interface Requirements

3.5.1.4.8.4.1 General

3.5.1.4.8.4.1.1 Maintenance Control Panel

3.5.1.4.8.4.1.1.1 Computer Signals - The ARO Logic Subunit receives 24-bit parallel binary words from the computer through the Maintenance Control Panel. Output data transfer is accomplished by the Output Data Request/Output Acknowledge scheme. The ARO Logic shall transmit up to 30 bits of information via the Input Data Request/Input Acknowledge scheme, to the computer. These Input/Output schemes are explained in Appendix 1.

3.5.1.4.8.4.1.1.2 Operate Mode Switch - The Operate Mode switch transmits data to the ARO Logic Subunit to inform the Subunit which mode has been selected.

3.5.1.4.8.4.1.2 Master Timing - The ARO Logic Subunit derives a 33.3 Hz frame sync signal from the 100 Hz clock generated by the MCPL. Initial output data requests for each frame are a direct result of this frame sync signal.

3.5.1.4.8.4.1.3 ARO Displays - The ARO Logic Subunit transfers a 6-bit selection and a 10-bit position parallel binary word together with a single unblank signal to each of the ARO Displays.

3.5.1.4.8.4.2 Interface Circuits - All signals shown in the ARO Logic functional flow diagram, Figure 46, that have the symbol “TP” labelled on the line are transmitted via twisted pair cables. The number inside the circle denotes the quantity of twisted pair signals entering or leaving the subunit. All “TP” output lines from the subunit shall be driven by the line driver circuit as specified in WR-101, Part II. All “TP” input lines shall use the input amplifier circuit specified in Appendix 11,

3.5.1.4.8.4.3 Output Signal Characteristics

3.5.1.4.8.4.3.1 Deflection - Ten parallel data bits to each ARO (logical “O” = + 4 + 1 volts, logical “l” = 0.0 + 0.5 -0.0 volts) over twisted pair cables. Reference (00) position is upper left corner of ARO Display screen.

3.5.1.4.8.4.3.2 Character Selection - Six parallel data bits to each ARO (logical “0” = + 4 ± 1 volts, logical “l” = 0.0 + 0.5 -0.0 volts) over twisted pair cables. Figure 49 illustrates the octal code for character selection as transmitted to the ARO Displays.

3.5.1.4.8.4.3.3 Unblank - One signal to each ARO (logical “0” = + 4 ± 1 volts, logical “l” = 0.0 + 0.5 -0.0 volts) over twisted pair cables.

3.5.1.4.8.4.3.4 Output Data Request - One signal to the computer (logical “O” = + 4 ± 1 volts, logical “1” = 0.0 + 0.5 - 0.0 volts).

3.5.1.4.8.4.3.5 Input Data and Input Data Request - Thirty data lines plus one control line shall be used for transmittal of diagnostic information to the computer. A logical “O” = + 4 ± 1 volts, alogical “1” = 0.0 + 0.5 - 0. 0 volts.

3.5.1.4.8.4.3.6 Test Indicator - One line to each ARO which is the ARO ground when the ARO Test Mode switch is in one of the two test positions, and “open” when the ARO Test Mode switch is in the "On Line” position. These lines shall be transmitted via the MCP.

3.5.1.4.8.4.4 Input Signal Characteristics

3.5.1.4.8.4.4.1 Data -24 parallel data bits from the Maintenance Control Panel (logical “0” = 0.0 +0.5-0.0 volts, logical “1” = + 5 ± 1.5 volts).

3.5.1.4.8.4.4.2 Output Acknowledge - One signal from the computer via the Maintenance Control Panel (logical “0” = 0.0 + 0.5 - 0.0 volts, logical “1” = + 5 ± 1.5 volts).

3.5.1.4.8.4.4.3 Switch Signals - Signals from the ARO Mode switch located on the Maintenance Control Panel (logical “0” = open switch contact, logical “1” = 0 volts).

3.5.1.4.8.4.4.4 100 Hz Clock - A square wave signal originating from the MCPL. This signal is derived from the 400 Hz power source, and therefore has a tolerance of ± 10%.

3.5.1.4.8.4.4.5 ARO Ground - The ARO ground line from each ARO Display shall be used to control the illumination of the Test Indicators on the ARO Displays when the ARO Test Mode switch is in either of the test positions. These grounds shall be isolated at the MCP from the DPS.

3.5.1.4.8.4.5 Word Formats

3.5.1.4.8.4.5.1 Output Word Formats - The format for the word transferred from the computer to the ARO Logic Subunit via the Maintenance Control Panel shall be as shown in Figure 44.

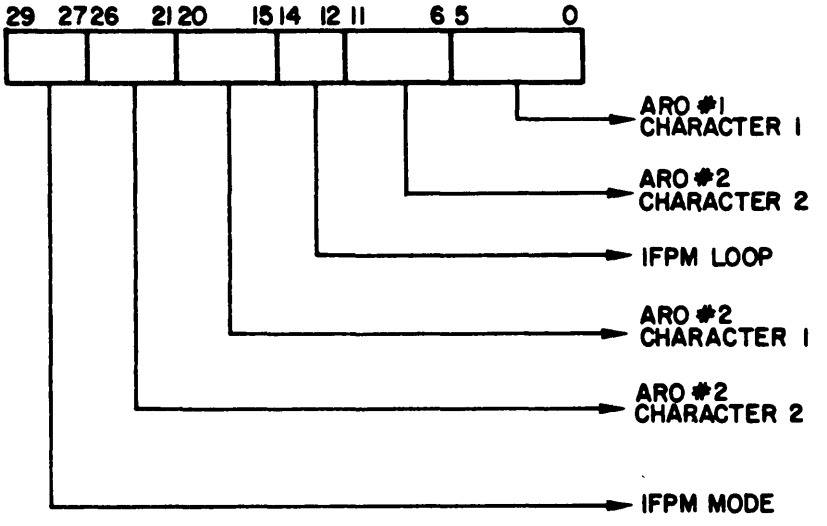


Figure 44. Format of Output Word from Computer to ARO Logic via Maintenance Control Panel

The six-bit character codes for displayed symbols shall be in conformance with Figure 49 in which the six-bit character code is presented in octal form.

3.5.1.4.8.4.5.2 Input Word Formats - The ARO Logic Subunit shall transmit up to 30-bit words to the computer.

3.5.1.4.8.5 Operation

3.5.1.4.8.5.1 Transfer Data - In the On Line mode of operation, data is transferred from the computer to the ARO Logic. The ARO Logic, on sensing the presence of an Output Acknowledge signal, loads the computer word into the input registers and initiates the display sequence. In the test modes, an internally generated acknowledge signal is substituted for the computer Output Acknowledge signal.

3.5.1.4.8.5.2 Display Character (Refer to Figures 50, 51 and 52) - Upon receipt of an Output Acknowledge, a 40 microsecond settling time delay is initiated. At the end of this delay , an unblinking signal is sent to each display unless a Blank Code (36) has been detected. The start of the unblank time initiates a delay of 16 microseconds. At the end of this time the unblinking signals are reset to a logical “O”, the horizontal position is advanced one step to the right, and the contents of the input register’s Character 2 codes are sat to the ARO Display selection circuits. This again initiates the 40 microsecond settling time delay. At the end of this delay, an unblinking signal is sent to each display unless a Blank Code (36) has been received. The start of unblank time initiates two more delays, one of 12 microseconds, and one of 16. At the end of the 12 microsecond delay, if the character is not the twentieth in the row, an Output Data Request is sent to the computer. At the end of the 16 microsecond delay, the unblank is reset, the horizontal position advanced, and the input register is cleared. If the character was the twentieth in the row, the 12 microsecond delay is changed to 140 microseconds before initiating the Output Data Request. The 16 microsecond delay still resets the unblinking signals, but it also clears the horizontal position counter (reset to the left side) and advances the vertical position one step downward.

3.5.1.4.8.5.3 End of Data Command - An End of Data Command shall be used to terminate a sequence of characters on the ARO's. This code (41) shall be interpreted as an EOD only if received in Character 1 of ARO 1; if received in any other character position-, the character associated with code 41 shall be displayed. Upon receipt of this code, further requests for data shall be inhibited until receipt of the next 33 Hz sync, all character codes shall be set to octal code 44, and the X and Y position registers shall each be set to octal code 11. The Output Data Request shall be raised upon receipt of the 33.3 Hz sync; however, the character selection and X and Y positioning registers shall not be cleared until receipt of the associated Output Acknowledge from the computer. A time of 160 microseconds minimum prior to unblank shall be allowed for positioning of the beam starting character position upon receipt of this Output Acknowledge signal. Normal timing operations as shown in Figures 50, 51 and 52 resume subsequent to the receipt of this first word.

3.5.1.4.8.5.4 Test 1 Mode - With the ARO Mode switch in the Test 1 position the computer signals are disconnected, and an internally generated Acknowledge signal and character data are substituted. The End of Data Command sensing gate is disabled so the counters will go to 400 before terminating and wait for the 33.3 Hz sync signal.

3.5.1.4.8.5.5 Test 2 Mode - All of the operational characteristics of Test 1, above, apply to this test mode. However, special gates do not allow the characters to be unblanked unless they are in the upper left hand 8 x 8 positions of the 20 x 20 character array. Also, the data inputs to the input register are such that the 8 x 8 array is arranged in the same sequence as the CHARACTRON matrix. This sequence is terminated at the beginning of the ninth line instead of after the 400th character.

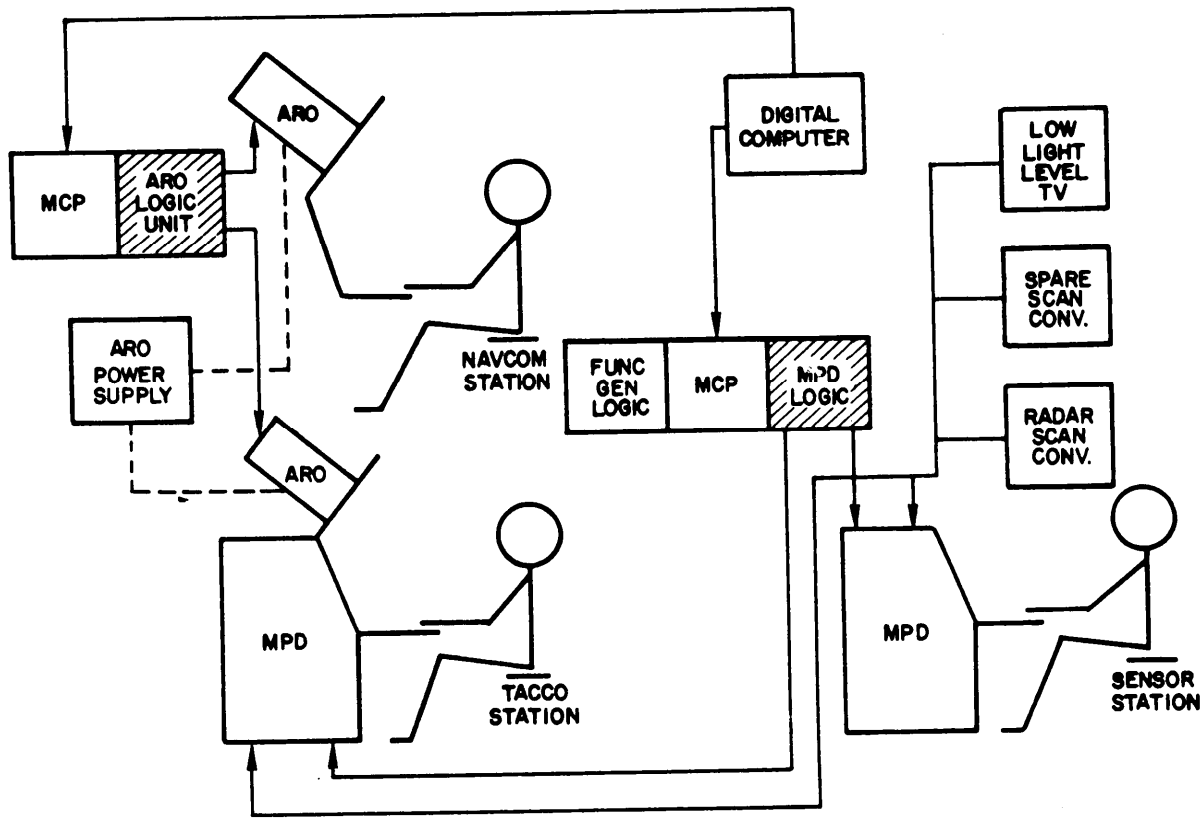


Figure 45. Interconnection of MPD and ARO Logic Subunits

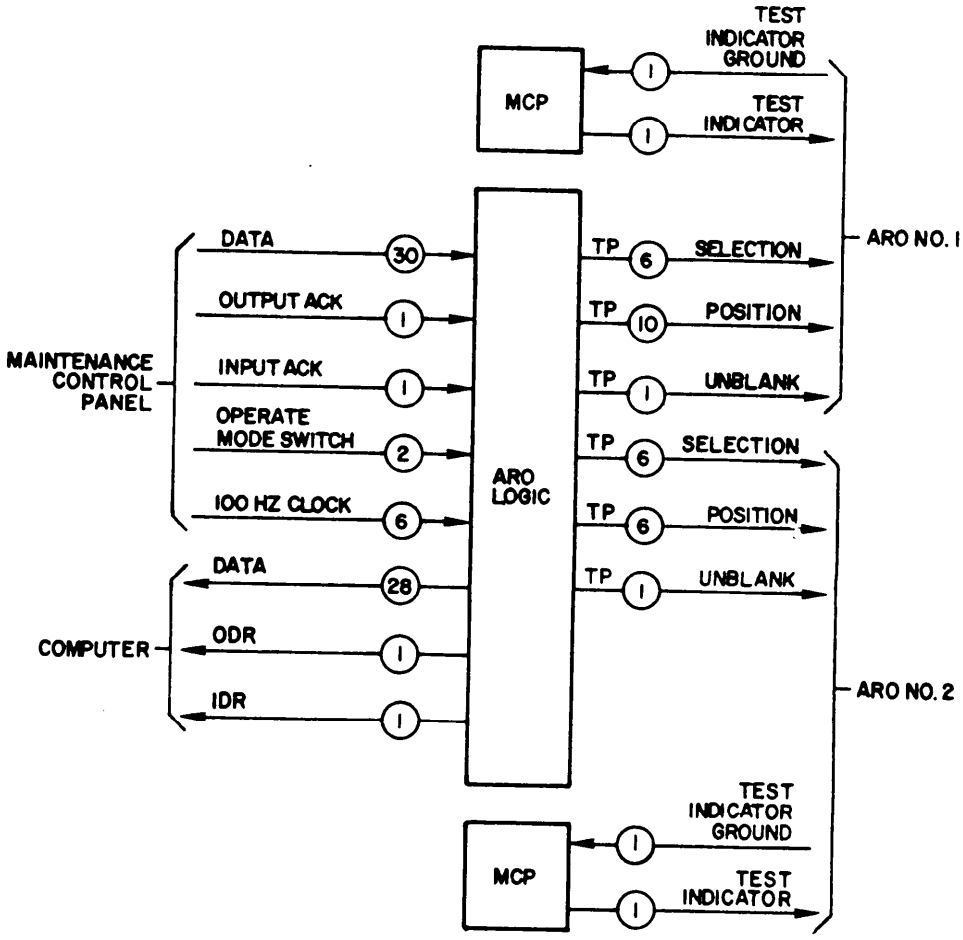


Figure 46. ARO Logic Subunit, Functional Flow Diagram

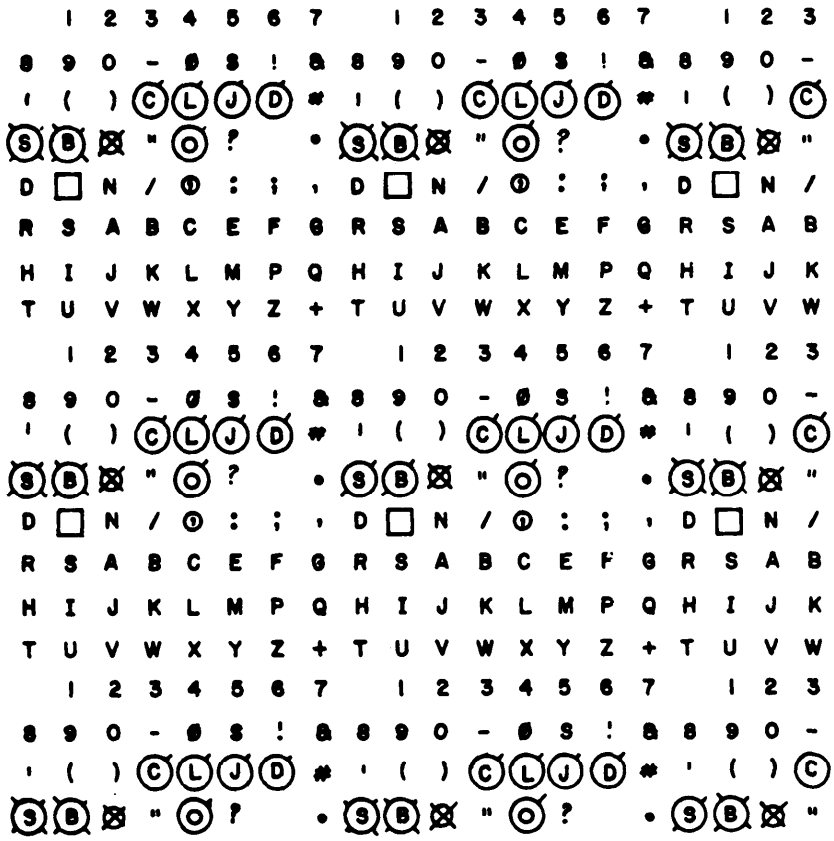


Figure 47. ARO Test 1 Format (20 x 20 Matrix)

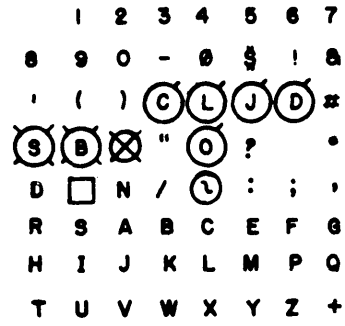


Figure 48. ARO Test 2 Format (8 x 8 Matrix)

CODE	CHARACTER
00	BLANK
01	1
02	2
03	3
04	4
05	5
06	6
07	7
10	8
11	9
12	0
13	-
14	Ø
15	S
16	!
17	@
20	' **
21	(
22	)
23	C
24	L

CODE	CHARACTER
25	J
26	D
27	#
30	S
31	B
32	⊠
33	"
34	◎
35	?
36	BLANK
37	.
40	D
41	□ *
42	N
43	/
44	2
45	:
46	;
47	,
50	R
51	S

CODE	CHARACTER
52	A
53	B
54	C
55	E
56	F
57	G
60	H
61	I
62	J
63	K
64	L
65	M
66	P
67	Q
70	T
71	U
72	V
73	W
74	X
75	T
76	Z
77	+

* END OF DATA IF CODE 41 IS RECEIVED IN ARO 1 CHARACTER 1

** APOSTROPHE

Figure 49. ARO Character Matrix Symbols and Octal Codes

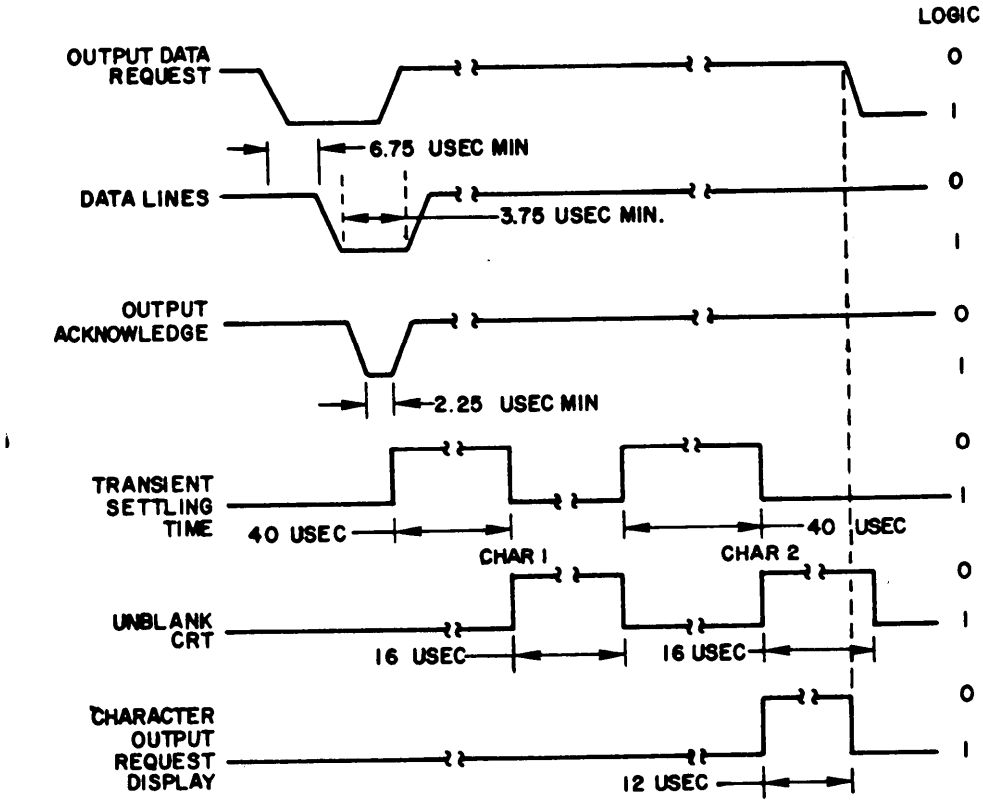


Figure 50. ARO Character to Character Timing

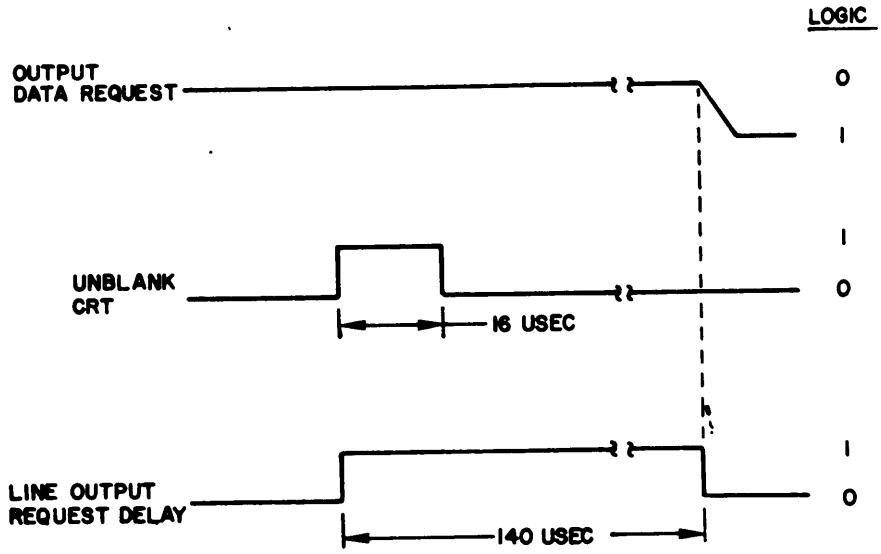


Figure 51. ARO Line to Line Timing

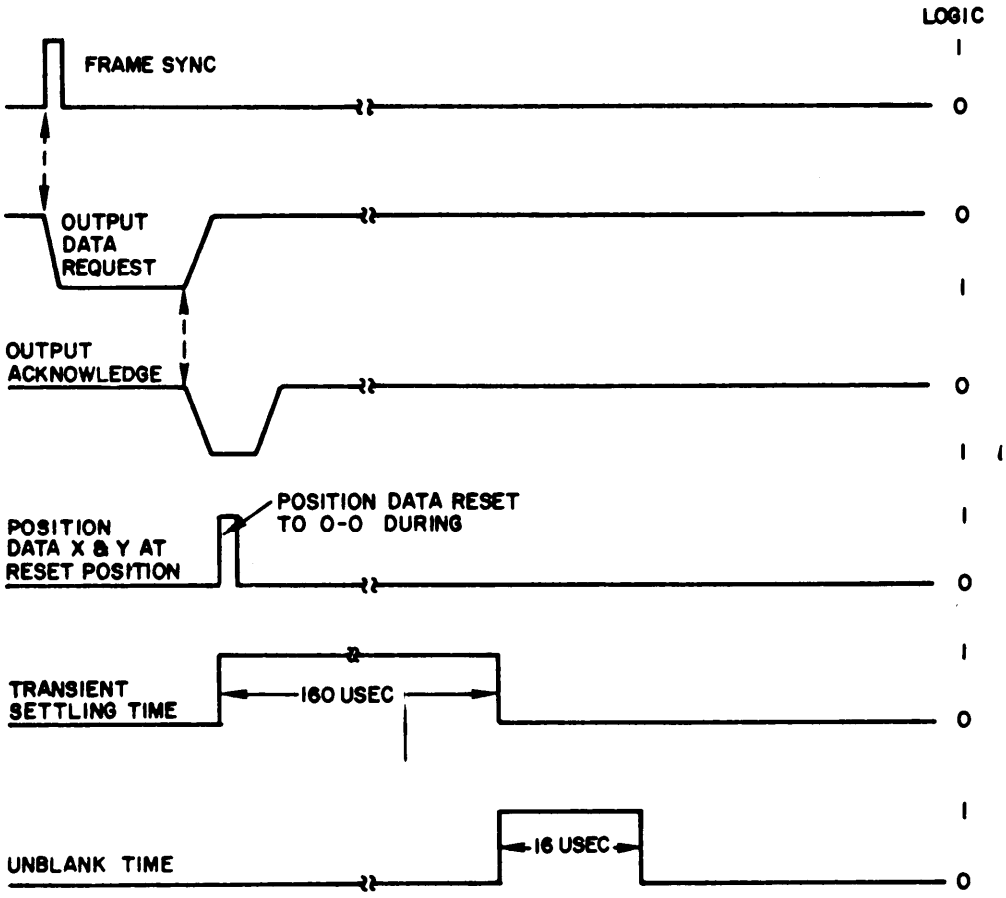


Figure 52. ARO Frame to **Frame** Timing

3.5.1.4.9 Maintenance Control Panel Subunit

NOTE

Since the Maintenance Control Panels for the four Logic Units are nearly identical, the following paragraphs will serve as a description of the MCP's for all four units.

3.5.1.4.9.1 Functional Description -The output register inan I/O subunit of the computer is time shared by up to four output peripherals. The 30 datelines emanating from the register are common to the four output peripherals; i.e., a computer 1/0 subunit transmits the data to the four output peripherals over a single 30 twisted pair cable, and the control lines for the four output peripherals determine which peripheral is to sample the data; the control lines for the four channels are independent. Subunits which communicate with the same I/O subunit have been assigned to the same logic unit. This permits a logic unit to buffer all incoming computer data with a single group of 30 input amplifiers.

In the four logic units there are three subunits, each of which requires a computer output channel. (Logic Unit 1 has only two subunits.) As indicated, a computer I/O subunit is capable of servicing up to four output peripherals. Since none of the logic units requires more than three output channels, each logic unit shall make the 30 data lines from the computer 1/0 subunit available for "bussing" to one additional output peripheral. The data lines from the computer shall remain available for "bussing" regardless of the number of subunits removed from the logic unit. In addition to the subunits, which satisfy an operational system requirement, the Maintenance Control Panel Logic shall provide for the buffering of the data lines to the internal subunits and the "bussing" of the data lines to the external peripherals. The Maintenance Control Panel shall also provide maintenance features for the subunits.

3.5.1.4.9.2 General Description - The Maintenance Control Panel subunit shall provide the following capabilities:

(1) Buffer the 30 data lines from the computer to the subunits of each logic unit.

(2) Provide the 30 data lines from the computer for "bussing" to other peripherals. The data lines from the computer shall remain available for "bussing" regardless of the number of subunits removed from the logic unit.

(3) Selectively monitor the data and control lines associated with any computer input peripheral contained in the logic unit. The monitoring shall be in the form of indicator lamps. -

(4) Without affecting the operation of the other peripherals, operate any one computer input peripheral contained in the logic unit off-line from the computer; i.e. , disable the input control lines which originate at the computer and allow the operator to simulate the control signals. The operator shall be able to select either single step or continuous mode of simulated operation. The single step mode shall allow the operator to transmit a single control signal of minimum duration each time a particular switch is depressed. If the continuous mode is selected, a control signal of minimum duration shall be transmitted each time the input peripheral raises the associated control line.

(5) Monitor the data and control lines associated with any computer output peripheral contained in the logic unit. The monitoring of the Output Data Request and External Function Request signals shall be in the form of indicator lamps and scope probe test points. The monitoring of the Output Acknowledge, External Function, and data lines from the computer shall be in the form of indicator lamps and scope probe test points.

(6) Without affecting the operation of the other peripherals, operate any one computer output peripheral contained in the logic unit off-line from the computer, i.e., disable the data and output control lines which originate at the computer (Output Acknowledge or

External Function) and allow the operator to simulate these data and control signals. The operator shall be able to select either single step or continuous mode of simulated operation. The single step mode shall allow the operator to transmit a single control signal of minimum duration (Output Acknowledge or External Function) each time a particular switch is depressed. If the continuous mode is selected, a control signal of minimum duration shall be transmitted each time the output peripheral raises the associated control line (Output Data Request or External Function Request). A switch/indicator shall be provided for each data bit of the computer word which can be simulated by the operator. If the operator wishes a particular data bit to be a logical "l", he may depress the switch/indicator associated with the data bit; the indicator will light, verifying that the bit is in the logical "1" state. The data bit shall continue to be transmitted as a logical "1" until the operator depresses the Clear switch. The Clear switch shall reset all data bits to the logical "O" state.

(7) Provide any additional maintenance functions described in the detailed requirements for the logic unit, or which may be needed to accomplish the Maintenance Control Panel Tests.

3.5.1.4.9.3 Interface Requirements

3.5.1.4.9.3.1 Input

3.5.1.4.9.3.1.1 Subunit to Maintenance Control Panel Logic- Each subunit shall vers for all input control and data lines. In addition, the input data and control lines (prior to the control and data line drivers) shall be provided by the subunits to the MCPL for monitoring. Monitoring shall be in the form of indicators.

All input communications to the computer shall be in accordance with Appendix 1.

3.5.1.4.9.3.1.2 Computer to Maintenance Control Panel Logic - The MCPL shall provide the input amplifiers for Input Acknowledge and Interrupt Enable for each subunit which is assigned an input channel. Data shall be provided to each subunit for both control lines.

3.5.1.4.9.3.2 output

3.5.1.4.9.3.2.1 Maintenance Control Panel Logic to Subunits - The MCPL shall provide to each subunit, buffered (with input amplifiers) data signals for the output control and data *lines* associated with that subunit. (Input amplifiers are described in Appendix II.)

In the off-line or maintenance mode, the MCPL shall provide to the selected subunit, the data and control lines which simulate the signals supplied by the computer. (Simulated control line signals shall be approximately the same pulse width as computer control line signals.)

3.5.1.4.9.3.2.2 Computer to Maintenance Control Panel Logic - Signal levels between the computer and the MCPL shall be in accordance with Appendix 1. All output communications between the computer and each subunit hall be via the MCPL.

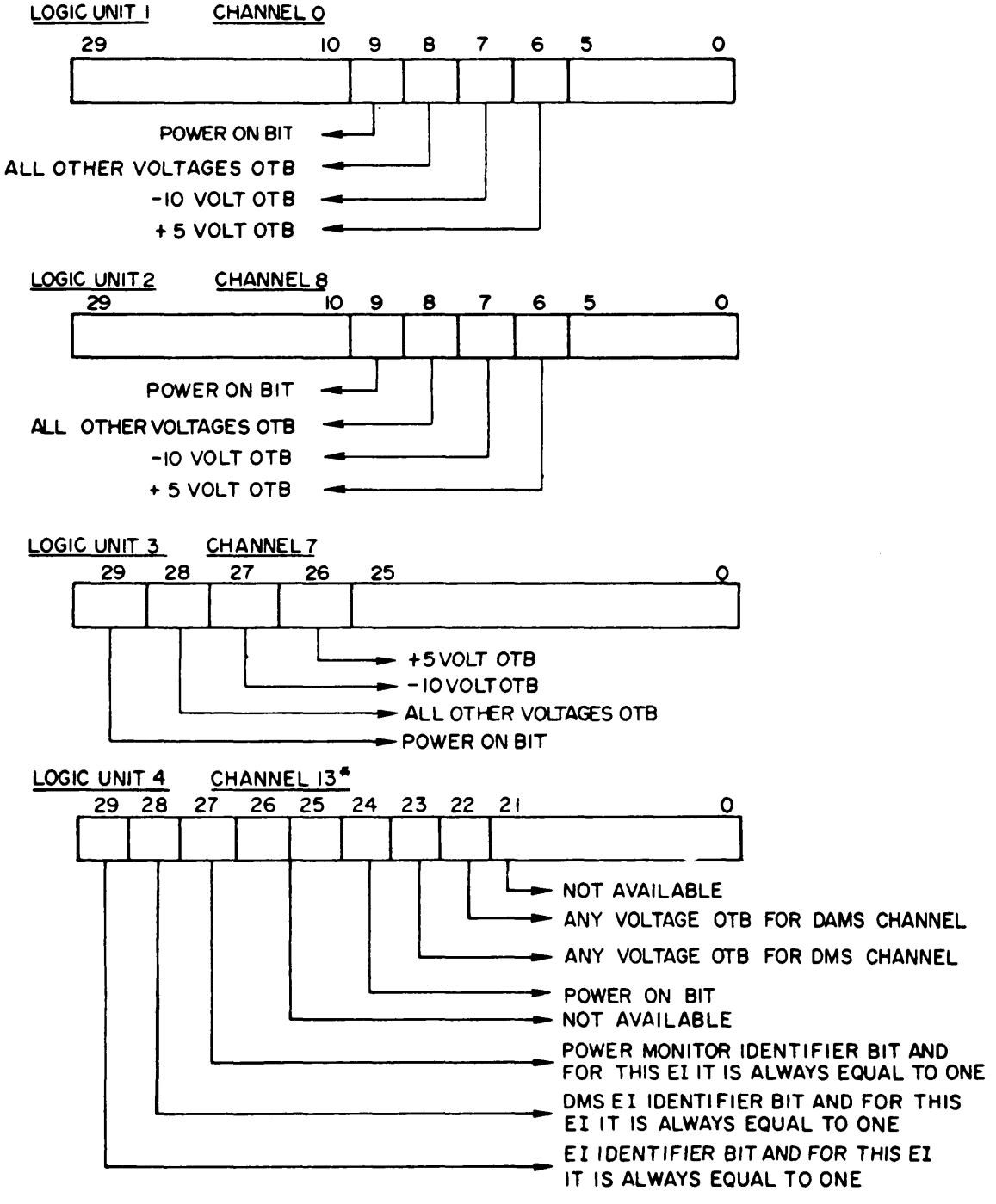
3.5.1 .4.9.3.3 Power Monitor - The MCPL shall monitor the output voltages from the power supply. When power is out-of-tolerance, not due to input power out-of-tolerance, a Power Valid word shall be transmitted to the computer using an interrupt. This word small be sent with every change of status.

3.5.1.4.9.3.3.1 Power Monitor Word Formats - The power monitoring word formats for the four logic units are shown in Figure 53.

3.5.1.4.9.3.3.2 Computer Channel Assignments

Logic Unit 1 - Channel 0
Logic Unit 2 - Channel 8
Logic Unit 3 - Channel 7
Logic Unit 4 - Channel 13

3.5.1.4.10 Power Supply Subunit Logic Unit 1 shall contain a Power Supply Subunit as described in 3.3.12.2.



THE "POWER-ON" BIT WILL BE A "1" FOR THE REPORT MADE WHEN POWER IS FIRST APPLIED AND WILL BE A ZERO FOR SUCCEEDING REPORTS

OTB MEANS OUT OF TOLERANCE BIT
LOGICAL "1" = IN TOLERANCE
LOGICAL "0" = OUT OF TOLERANCE

* THE LOGIC UNIT 4 POWER MONITOR WORD SHALL BE SENT AS A DATA MULTIPLEXER STATUS EI, PARAGRAPH 3.5.4.4.1.3.1(5)

Figure 53. Power Monitor Word Formats

3.5.2 Data Analysis Logic Unit MX-8024A/AYA-8 (Logic Unit 2)

3.5.2.1 Function: See 3.4.8.

3.5.2.2 Form Factor: Refer to illustration in EI-515, Avionics Installation Instructions for Data Analysis Programming Group AN/AYA-8B.

3.5.2.3 Weight: see 3.5.1.3.

3.5.2.4 Contents: See 3.4.3.

3.5.2.4.1 Magnetic Tape Control Subunit

3.5.2.4.1.1 Functional Description - The Magnetic Tape Control (MTC) provides the computer with acessto, and control up to Magnetic Tape Transports (MTT). The MTC converts the 30-bit computer words into a form acceptable to the MTT, and interprets the instructions issued by the computer. The MTC converts the MTT characters into 30-bit words acceptable to the computer, and notifies the computer of certain specified occurrences (Interrupts) which affect subsystem operation.

The Digital Magnetic Tape Subsystem (DMTSS) shall be capable of operating at 75 inches per second under program control.

Figure 56 is a Functional Flow Diagram of the MTC. Figure 57 is a block diagram of the DMTSS.

3.5.2.4.1.2 General Description - The MTC shall be used to disassemble the computer word, during output operations, into 6-bit characters and to reassemble the 6-bit characters into computer words, during input operations. The MTC shall also be used to store the "Identifier word" during a search operation and perform the search operation compare.

3.5.2.4.1.3 Operating Requirements

3.5.2.4.1.3.1 Word Arrangement - The MTC shall handle four types of computer words:

(1) Data Words

(2) Function Words

(3) Identifier Words

(4) Status Words

3.5.2.4.1.3.1.1 Data Word - The Data word (input or output) is arranged in groups of 6-bit characters as shown in Figure 54.

During an output operation the MTC stores the Data word in its assembly - disassembly register. When the MTC is ready for an output transfer, it disassembles the

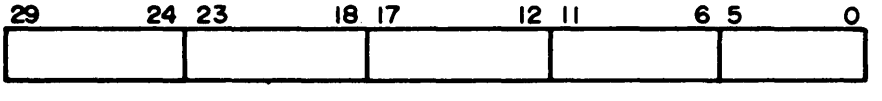


Figure 54. Format for Data Word between Computer and Magnetic Tape Control .

30-bit word into 6-bit characters and transfers these MTC characters (one at a time) to the MTT. During input operations the MTC assembles the 6-bit characters received (one at a time) from the MTT into a 30-bit computer word.

3.5.2.4.1.3.1.2 Function Word - The Function word contains the operating instructions. The Function Code (FC) is contained in bits 27 -24. The MTC on receiving a Function word, decodes the lower 4 bits (FC). The decoded finction Code sets the operating mode for the MTC. The MTC uses the Function Code to direct the operation of the tape transport. The Function word is always accompanied by an External Function signal which differentiates the Function word from a Data word.

NOTE

A Function word will be required before any operation is initiated.

Bits 17 and 18 are used to select any one of the possible MTT's Transport select for this operation is by bit position rather than binary code. Bits 20 and 21 select density while bit 19 selects lateral parity format.

3.5.2.4.1.3. 1.3 Identifier Word - The Identifier word is a full length computer word which immediately follows a Search-Read Function word; it is arranged in groups of 6-bit characters as shown in Figure 55.

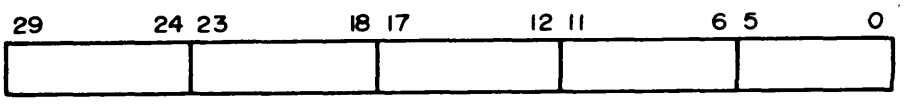


Figure 55. Identifier Word from Computer to Magnetic Tape Control

The Identifier word may contain any bit configuration except that bits 24 through 27 may not be zeros simultaneously. It is sent to the MTC accompanied by an External Function signal. The Identifier word is stored in the MTC assembly-disassembly register and compared with each 30-bit Search word. The comparison is accomplished by the MTC search comparison circuit.

3.5.2.4.1.3.1.4 Status Word - The Status word contains the error information generated by the MTC and status conditions of the selected MTT. When the MTC has accumulated all error and status information, it sends an External Interrupt signal to the computer. A normal input transfer of the Status word is then initiated.

3.5.2.4.1.3.2 Control Operation

3.5.2.4.1.3.2.1 Parity - The MTC will provide both lateral and longitudinal parity generation and detection.

3.5.2.4.1.3.2.1.1 Lateral Parity - During a write operation a Lateral Parity bit shall be added to each six-bit character according to the format specified by the Function word and the resultant seven bits recorded as one frame. Either odd (total number of “1‘s” in a frame is odd) or even (total number of “1 ‘s” in a frame is even) Lateral Parity must be specified by the Function word. If the MTC detects a frame whose Lateral Parity does not agree with that specified, during a read type operation or during the post-write check of the record type operation, a Lateral Parity Error shall be generated. The parity former shall also detect an all zero character and record the following codes for the specified parity.

		Tape Track						
		1	2	4	8	A	B	C
Odd	Parity	O	0	0	0	0	0	1
Even	Parity	O	0	0	0	1	0	1

3.5.2.4.1.3.2.1.2 Longitudinal Parity - During a write operation a Longitudinal Even Parity bit shall degenerated by the MTC for each tape track and shall be recorded after the last frame of the record. If the MTC detects an error in this parity during a read type operation or during the post-write check of the record type operation, a Longitudinal Parity Error shall be generated.

3.5.2.4.1.3.2.2 Computer Word - Tape Track Formats - The correspondence between computer word data and the tape track storage of that data is defined in Figure 58.

3.5.2.4.1.3.2.3 Load Point, Tape Marks, Gaps and Density Control - The MTC during output, shall determine the delay to allow for a gap of 3-1/2 inches beyond the load point marker (before the first record is written). The End of File mark, the Inter-record Gap, and the Write Density are also controlled by the MTC.

3.5.2.4.1.3.2.4 Tape Transport Control - The MTC shall transfer signals based on the Function Code to the selected MTT and monitor the return signals from the MTT to determine the control sequence. The MTC shall use the Transport Select bits to provide the necessary enable to select the desired MTT.

3.5.2.4.1.3.2.5 Character Count - The MTC shall count the character transfers on read and record operations and generate an error if one occurs.

3.5.2.4.1.3.2.6 MTT Timing - During output, the MTC shall monitor transport status and provide the delay to initiate writing 3-1/2 inches beyond the load point marker before the first record is written. The MTC shall also provide the delays necessary to record at the normal Inter -record Gap of 3/4 inch or the extended Inter-record Gap of 3-1/2 inches. During input and output the MTC shall monitor the End of Tape marker and if no data is received from the MTT for a time corresponding to approximately 10 inches of tape after the end of tape, the MTC shall terminate the instruction and indicate “EOT” to the computer. No new forward tape motion instructions will be initiated by the MTC. Prior to the stopping of tape motion, the MTC shall provide timing and control signals that define the time at which the current instruction is complete, so that the computer may repeat the current instruction without stopping the tape motion. This shall be designated as the Repeat Instruction Request Time. While the Function Code must remain identical, the density select and parity select may be changed with the Repeat Instruction.

3.5.2.4.1.3.2.7 Character Loop Gate - The MTC shall provide a character loop gate that makes it possible to bypass the MTT on the Loop Instruction.

3.5.2.4.1.3.3 Function Repertoire Operation

3.5.2.4.1.3.3.1 Function Code Description - Four bit positions (27 through 24) of the Function word form the Function Code. The following describes the functions required.

Function Code Octal	Binary 27 26 25 24 MSB	
00	0 0 0 0	Master Clear - This instruction has priority over all others and shall terminate all others in process, including Rewind. The Master Clear places the DMTSS in the idle state and a Status Word with Interrupt is sent to the computer.

Octal	Binary 27 26 25 24 MSB	
01	0 0 0 1	Rewind - The selected MTT shall rewind the tape to load point. The Status Word with Interrupt shall be sent to the computer after the MTC initiates the rewind, not at the completion of the rewind.
02	0 0 1 0	Status Report - The status of the selected MTT shall be stored in the status register and a Status word with Interrupt shall be sent to the computer. No tape movement shall occur.
03	0 0 1 1	Write - The selected MTT shall write in the forward direction at the bit packing density specified by the Function word. At completion of the instruction a Status word with Interrupt shall be sent to the computer.
04	0 1 0 0	Write Extended Record Gap - The selected MTT shall write in the forward direction at the bit packing density specified by the Function word. The Interrecord Gap shall be increased from the normal 3/4 of an inch to 3-1/2 inches; at completion, a Status word with Interrupt shall be sent to the computer.
05	0 1 0 1	Write Tape Mark - The selected MTT shall write in the forward direction the fixed format tape mark adding a normal record gap. At completion of the Instruction a Status word with Interrupt shall be sent to the computer.
06	0 1 1 0	Write Tape Mark - Extended Record Gap - The selected MTT shall write in the forward direction the fixed format tape mark. The Interrecord Gap shall be increased from the normal 3/4 inches to 3-1/2 inches. At completion a Status word with Interrupt shall be sent to the computer.
07	0 1 1 1	Backspace Record - The selected MTT shall move the tape in the reverse direction to the next Interrecord Gap. The tape shall be properly positioned in the Interrecord Gap for reading or writing. At completion a Status word with Interrupt shall be sent to the computer.
10	1 0 0 0	Search File Reverse - Read Record Forward - The selected MTT shall search in the reverse direction for a compare *or* "find" condition between the Identifier word and the first word in the record. (Last word read reverse). When a "find" is made, the record is read in the forward direction. The search shall be terminated by an error condition *or* tape mark; at completion a Status word with Interrupt shall be sent to the computer.
11	1 0 0 1	Backspace File - The selected MTT shall move the tape in the reverse direction to the Interrecord Gap beyond the next tape mark. At completion a Status word with Interrupt shall be sent to the computer.
12	1 0 1 0	Read Record Reverse - The selected MTT shall read one record in the reverse direct ion. Character order within each computer word shall be in correct order. At completion a Status word with Interrupt shall be sent to the computer.
13	1 0 1 1	Space Record - The selected MTT shall move the tape in the forward direction to the next Interrecord Gap. The tape shall be properly positioned in the Interrecord Gap for reading or writing. At completion a Status word with Interrupt shall be sent to the computer.

Octal	Binary 27 26 25 24 MSB	
		Search File Forward- The selected MTT shall search in the forward direction for a compare or "find" condition between the Identifier word and the first word in the block. When a "find" is made, the record is read in the forward direction. The search shall be terminated by an error condition or tape mark. At completion a Status word with Interrupt shall be sent to the computer.
15	1 1 0 1	Space File - The selected MTT shall move the tape in the forward direction to the Interrecord Gap beyond the next tape mark. At completion a Status word with Interrupt shall be sent to the computer.
16	1 1 1 0	Read Record Forward - The selected MTT shall read one record in the forward direction. At completion a Status word with Interrupt shall be sent to the computer.
17	1 1 1 1	Loop - This instruction shall test the data transfer paths of the MTC.

One word shall be requested by the MTC and shall be stored in the word registers. The word shall be transferred back to the computer and then also shall be transferred through the MTC data paths and again stored in the word registers. The word shall then again be transferred to the computer.

NOTE

The Repeat Instruction mode is applicable to all Function Codes except Loop, Status Report, Rewind, Search, and Master Clear.

3.5.2.4.1.3.3.2 Operation - The Operation Code is located in bits 27 to 24 of the Instruction word. Legal operation codes exist for the five basic operations of Read, Search-Read, Write, Space and Rewind. Operation Codes except Rewind, Master Clear, Status Report, and Loop must be supplemented by Parity and Density codes, placed in bit locations 19 through 21 respectively of the Instruction word. All instructions except Master Clear, Status Report, and Loop must include a Tape Transport select bit located in bit positions 17 or 18.

3.5.2.4.1.3.3.2.1 Master Clear - The DMTSS shall perform a Master Clear, whenever the power is applied, whenever the Channel Reset switch on the MCP is operated with the MTC in the Off-Line Mode and whenever the Master Clear Function Code is received via the External Function command word. The Master Clear shall have the following properties.

(1) The Master Clear shall be accepted by the DMTSS at any time.

(2) The Master Clear shall be followed by a Status word Interrupt.

(3) Master Clear shall stop all tape motion, including a rewinding tape, and shall place the DMTSS in the Idle state.

(4) The DMTSS shall accept an External Function command word any time after a Master Clear provided that the Interrupt has been acknowledged.

3.5.2.4.1.3.3.2.2 Rewind - The selected MTT shall rewind the tape and position the load point at the load point sensor. The Status Interrupt shall be presented upon initiation of the rewind and not upon completion of the rewind.

3.5.2.4.1.3.3.2.3 Status Report - The MTC shall transmit to the computer the stored status report of the selected MTT via the Interrupt control line and 30 data bits.

3.5.2.4.1.3.3.2.4 Write Function - The MTT can be programmed to write forward one record at 200, 555.5 or 800 bits per inch using either odd or even Lateral Parity.

3.5.2.4.1.3.3.2.4.1 Write Function Operation - When the MTC detects a Write Function, it shall cause the selected transport to move the tape forward at 75 inches per second and record an Interrecord Gap. A signal is then placed on the computer Output Data Request line. The computer will then respond with the first data word. The MTC shall disassemble each word into five 6-bit characters, generate a Lateral Parity bit, and transfer the seven-bits to the selected transport for recording on tape according to the density selected. When the recorded frame passes over the read head, it is checked for Lateral Parity. If a Lateral Parity error is detected, upon completion of the function, a Parity Error is transmitted to the computer. If no error occurs during recording, the process will continue until the computer no longer acknowledges the Output Data Request within the time allotted for another word to be disassembled and written. The above procedure shall be repeated until the end of the first record; since the data is written on the tape in the form of records, a new External Function will be required for each record written.

3.5.2.4.1.3.3.2.4.2 Write Function Conditions - Conditions that may occur during a Write Function and shall be indicated by an External Interrupt and a Status word are as follows:

(1) Normal Completion

(2) Rewinding

(3) End of Tape Warning

(4) Low Tape Warning

(5) Write Lockout

(6) Illegal Instruction

(7) Improper Frame Count

(8) Fault

(9) Lateral Parity Error

(lo) Longitudinal Parity Error

(11) Timing Error

(12) Illegal Operation

3.5.2.4.1.3.3.2.4.3 Write Function Termination - The Write Function word will be followed by at least one Data word. (If no Data words are transferred, an Output Timing Error shall be generated.) Each Data word to be written in a record must be received by the MTC within a predetermined amount of time such that the spacing between the corresponding bits of adjacent characters within the record shall be a nominal distance of 200, 555.5 and 800 characters per inch at 75 inches per second. Otherwise the MTC shall assume an “End of Write. ” Longitudinal Parity shall then be written after an appropriate delay and the recording process terminated. Tape motion shall be stopped after part of the IRG is written on the tape. The MTC shall place a “Normal Completion” or appropriate Error Status word on the computer input lines and send an External Interrupt to the computer. Data received after the termination but before a new Function word shall be considered an Output Timing Error and shall not be recorded.

3.5.2.4.1.3.3.2.5 Write XIRG - The selected MTT shall record an Extended Interrecord Gap of 3-1/2 inches instead of the normal 3/4 inch IRG preceding a normal Write portion of the operation. If no data is transferred from the computer for recording, the XIRG will be on the tape and an Output Timing Error shall be generated. The Status word sent to the computer shall contain MTC status and all error indications detected in a Normal Write Operation.

3.5.2.4.1.3.3.2.6 Write Tape Mark - The selected MTT shall write a fixed format Tape Mark. The Tape Mark shall be a special one-frame record with one frame of Longitudinal Parity using "Even" Lateral Parity. The special one-frame record consists of "0's''in tape tracks A, B, and C and "l's" in tape tracks 1, 2, 4, and 8. A Status word with External Interrupt shall be sent to the computer upon completion of the Write Tape Mark function.

3.5.2.4.1.3.3.2.7 Write Tape Mark, XIRG - The selected MTT shall record an Extended Interrecord Gap of 3-1/2 inches instead of the normal 3/4 inch IRG preceding the normal Write Tape Mark operation. The Tape Mark which is written is identical to the Write Tape Mark in normal operation.

3.5.2.4.1.3.3.2.8 Backspace Record - The selected MTT shall move the tape in the reverse direction to the next IRG (back one record). The tape shall be properly positioned in the IRG for reading or writing. If the tape was at Load Point when the Back Space instruction was given, an Illegal Operation shall be generated and noted in the Status word. The Status word with External Interrupt shall be sent to the computer upon completion of the Back Space function.

3.5.2.4.1.3.3.2.9 Search File Reverse - Read Record Forward - The MTC shall search the tape in the reverse direction and compare the first word of each record with an Identifier word, which is transmitted from the computer to the MTC (with the characters in correct order) by a one word output buffer. When a compare occurs, the *'Found" record is transmitted in the forward direction to the computer as a Normal Read.

NOTE

In a Forward Search the first word encountered in each record is the first word of the record. In a Backward Search the last word encountered in each record is the first word of the record. (This is the same word encountered in the Forward Search with the characters in the same order).

3.5.2.4.1.3.3.2.9.1 Search File Reverse Operation - The function that specified a Search File Reverse Operation, will be followed by an Identifier word, of 30 bits, which may be any configuration of bits except that data bits 24 through 27 may not be zero simultaneously. The Search portion of the Search File Reverse Operation compares the first word of the record with the Identifier word. If a find is not made, the MTC shall move on to the next record and compare the first word of that record with the Identifier word. This process will continue until a find is made, an error occurs, the search is terminated, or a Tape Mark occurs. When a find is made, the MTC shall perform a Forward Read Tape operation, which shall be the same as a normal Forward Read operation. The Read operation shall begin with the Identifier word, with the characters in the correct order, then continue until the end of the record.

3.5.2.4.1.3.3.2.9.2 Search File Reverse Conditions - Conditions which may occur during a Back Search File function shall be indicated by an External Interrupt. These conditions are identical to the Search File conditions.

3.5.2.4.1.3.3.2.9.3 Search File Reverse Termination - If the MTC does not receive the Search word from the computer before it starts searching a record, an Output Timing Error shall be generated. The Search File Reverse operation shall be terminated whenever a Parity or Timing Error is generated. A Tape Mark and a "Normal Completion" shall also terminate the Search File Reverse operation. When the tape motion is stopped due to an error, the tape shall be positioned in the IRG after the record in which the error occurred.

3.5.2.4.1.3.3.2.10 Backspace File - The selected MTT shall move the tape in the reverse direction to the Interrecord Gap beyond the next tape mark. At completion a Status word with Interrupt shall be sent to the computer.

3.5.2.4.1.3.3.2.11 Read Record Reverse - The selected MTT shall read one record in the reverse direction. Character order within each computer word shall be in the correct order. At completion a Status word with Interrupt shall be sent to the computer.

3.5.2.4.1.3.3.2.12 Search File Forward - The selected MTT shall read records from the tape in the forward direction and compare the first word of each tape record with an Identifier word, which is transmitted from the computer to the M'TC by a one-word output buffer. When a compare occurs, that Found record shall be transmitted to the computer as in a Normal Read.

3.5.2.4.1.3.3.2.12.1 Search File Operation - The Function that specified a Search File will be followed by an Identifier word, of 30-bits, which may be any configuration of bits except that bits 24 through 27 may not be zero simultaneously. The Search portion OF the Search File operation compares the first word of the record with the ldentifier word. If a find is not made, the MTC shall move on to the next record and compare the first word of that record with the Identifier word. This process shall continue until a find is made, an error occurs, the search is terminated or a tape mark occurs. When a find is made. the MTC shall perform a Read Type operation, which shall be the same as a Normal Read operation. The Read operation shall begin with the Identifier word and continue until the end of the record.

3.5.2.4.1.3.3.2.12.2 Search File Conditions - Conditions which may occur during a Search File function shall be indiceted by an External Interrupt. These conditions are identical to the read conditions.

3.5.2.4.1.3.3.2.12.3 Search File Termination - If the MTC does not receive the Identifier word from the computer before it starts searching a record, an Output Timing Error shall be generated. The Search File operation shall be terminated whenever a parity or timing error is generated. A Tape Mark and a Normal Completion shall also terminate the Search File operation. When the tape motion is stopped due to an error, the tape shall be positioned in the IRG after the records in which the error occurred.

3.5.2.4.1.3.3.2.13 Space File - The MTC shall cause the selected transport to move the tape in the Forward direction to the IRG beyond the next Tape Mark and shall send a normal completion Status Code to the computer when the function is complete.

3.5.2.4.1.3.3.2.14 Read Function - The MTC can be programmed to read in the forward direction only one record at a time.

3.5.2.4.1.3.3.2.14.1 Read Function Operation - To read from a selected tape, the program will issue a Read Function for each record; however, the computer may stop accepting data at any point within the record, or accept none of the information. The computer must sample the input lines and acknowledge each input Data Request within a specified time for each density, or words will be lost. If the computer fails to sample the input lines and acknowledge the Input Data Request within this allotted time, an Input Timing Error shall occur and the MTC shall cease the transfer of data to the computer for the remainder of the record. Following detection of "End of Record", the MTC shall set the Input Timing Error Status word on the input lines and generate an External Interrupt to the computer.

3.5.2.4.1.3.3.2.14.2 Read Function Condition - Conditions that may occur during a Read Function shall be Indicated by an External Interrupt. They are as follows:

(1) Normal Completion

(2) Rewinding

(3) End of File

(4) End of Tape Warning

(5) Load Point

(6) Low Tape Warning

(7) Illegal Instruction

(8) Illegal Operation

(9) Improper Frame Count

(10) Fault

(11) Lateral Parity Error

(12) Longitudinal Parity Error

(13) Timing Error

3.5.2.4.1.3.3.2.14.3 Read Function Termination - The MTC after sensing the End of Record shall place a Status word on the input lines and generate an External Interrupt to the computer. The Status word shall contain either Normal Completion or all Error indications encountered during the read operation.

3.5.2.4.1.3.3.2.15 Loop - This instruction shall test the data transfer paths of the MTC. One word shall be requested by the MTC. The word shall be stored in the MTC word registers and transferred back to the computer from storage. The word shall then be routed through the MTC data paths (bypassing the data line drivers and input amplifiers) and back to the word register. It shall then be transferred back to the computer. (The computer receives two words back). At completion a Status word with Interrupt shall be sent to the computer.

3.5.2.4.1.3.3.3 Interrupts - The MTC shall be provided with the facility for interrupting computer operation for any of several reasons. These include normal answers to Function commands to notify the computer of the completion of that Function, Equipment Status, and Error Codes to indicate faults which will affect subsystem operation. The computer shall be interrupted after the completion of every operation performed by the MTC. The MTC shall place the Status word on the channel input lines and raise the External Interrupt Line. The bit structure of the Status word will enable the computer program to determine the status of the MTC and whether or not the requested operation was successfully completed. Any such Interrupt sent to the computer must be acknowledged by the computer before another External Function with an Instruction word, other than a Master Char, will be accepted by the MTC. A description of each Interrupt follows: (Appendix I contains a detailed description of the computer interrupt schemes).

3.5.2.4.1.3.3.3.1 Status Word Format

Bit Location	Function
0	Normal Completion
1	Rewinding
2	End of File
3	End of Tape Warning
4	Load Point
5	Low Tape Warning
6	Write Lockout
7	Illegal Instruction
8	Illegal Operation
9	Improper Frame Count

Bit Location	Function
10	Fault
11	Lateral Parity Error
12	Longitudinal Parity Error
13	Timing Error
14	Master Clear
15	No Compare

3.5.2.4.1.3.3.3.2 Normal Completion - This Status shall be indicated when the operation was completed with all conditions "normal" for the instruction performed. A Status condition of Normal Completion shall make it unnecessary for the computer program to examine any other Status bits. Normal Completion shall be reset if any Status condition not normal for that instruction exists. Normal Completion shall be reset under the following combinations of Instruction and Status: Rewind Instructions and specified tape transport not rewinding (except at load point); not a Rewind Instruction and rewinding; End of File Status and not a Write Tape Mark or Space File or Backspace File Instruction; and a Write Tape Mark Instruction and not an End of File Status.

3.5.2.4.1.3.3.3.3 Rewinding - This Status bit shall indicate that the selected transport is rewinding.

3.5.2.4.1.3.3.3.4 End of File - This Status bit shall indicate that the MTC detected a tape mark.

3.5.2.4.1.3.3.3.5 End of Tape Warning - This Status bit shall be set when the end of tape marker passes its sensor in the forward direction only.

3.5.2.4.1.3.3.6 Load Point - This Status bit shall indicate that the selected MTT is at the load point.

3.5.2.4.1.3.3.3.7 Low Tape Warning - This Status bit shall indicate that the tape is past the variable low tape warning point.

3.5.2.4.1,3.3.3.8 Write Lockout - This Status bit shall indicate that the selected MTT does not have a write permit ring in the tape reel.

3.5.2 .4.1.3.3.3.9 Illegal Instruction - This Status bit shall indicate that no packing density is specified or that no address or multiple MTT addresses are specified.

3.5.2.4.1.3.3.3.10 Illegal Operation - This Status bit shall indicate that a combination or normal instructions and normal conditions exist that together are illegal, i.e. , reverse direction at load point and forward directional end of tape.

3.5.2.4.1.3.3.3.11 Improper Frame Count - This Status bit shall indicate that the character counter in the MTC did not process an integral number of 30-bit words.

3.5.2.4.1.3.3.3.12 Fault - This Status bit shall indicate a condition that requires manual intervention at the MTT or MTC. The conditions are MTT not ready, MTT Select Not Answered, or Write Instruction and no Write Permit Ring.

3.5.2.4.1.3.3.3.13 Lateral Parity Error - This Status bit shall indicate a Lateral Parity Error.

3.5.2.4.1.3.3.3.14 Longitudinal Parity Error - This Status bit shall indicate a Longitudinal Parity Error.

3.5.2.4.1.3.3.3.15 Timing Error - This Status bit shall indicate a Timing Error in the computer MTC interface. If the computer does not send at least one word in a Write operation, if the computer does not accept the Data word on a Read operation before the next word must-be transferred, or if the computer does not send the Identifier word on search before data is received from the MTT, the Timing Error Status bit shall be set.

3.5.2.4.1.3.3.3.16 Master Clear - This Status bit shall indicate that a Master Clear function has been performed.

3.5.2.4.1.3.3.3.17 No Compare - This Status bit shall indicate that the data sent through the data paths in the loop instruction is not identical to the data received from the data paths.

3.5.2.4.1.3.3.4 Interrecord Gap (IRG) - Normal Interrecord Gap shall be a nominal 3/4 inch in length. Actual length is 0.75 inch + 0.157 inch -0.125 inch.

3.5.2.4.1.3.3.4.1 Extended Interrecord Gap (XIRG) - The Extended Interrecord Gap shall be a nominal 3-1/2 inches in length. Actual length is 3.4 inch l 0.90 inch.

3.5.2.4.1.3.3.5 Density Designator - Bits 20 and 21 of all Function Codes except Rewind shall indicate the density at which the data was recorded.

3.5.2.4.1.3.3.5.1 Low Density - 200 bits per inch shall be indicated by “0’s’’inbit positions 20 and 21.

3.5.2.4.1.3.3.5.2 Medium Density - 555.5 bits per inch shall redesignated by a “l” in bit position 20 and a “O” in bit position 21.

3.5.2.4.1.3.3.5.3 High Density - 800 bits per inch shall redesignated by a "1"in bit positions 20 and 21.

3.5.2.4.1.3.3.6 Lateral Parity Designator - Bit position 19 designates the Lateral Parity. A “1’’select so odd parity(total number of “1's’’in a frame is odd). A “0’’s elects even parity (total number of “1 ‘s” in a frame is even).

3.5.2.4.1.3.3.7 Tape Format - Refer to Figure 59.

3.5.2.4.1.4 Interface Requirements

3.5.2.4.1.4.1 Computer/DMTSS - Communications between the DMTSS and the computer shall be via the Maintenance Control Panel Logic and in accordance with Appendix I and Maintenance Control Panel (3.5.2.4.6). The following lines will originate at the computer (via the MCPL) and terminate at the MTC.

(1) 1 Interrupt Enable

(2) 1 External Function

(3) 1 Input Acknowledge

(4) 1 Output Acknowledge

(5) 30 Output Data Lines

The following lines will originate at the MTC and terminate at the computer:

(1) 30 Input Data Lines

(2) 1 Output Data Request

(3) 1 Input Data Request

(4) 1 Interrupt

(5) 1 External Function Request

3.5.2.4.1.4.2 Magnetic Tape Control to Magnetic Tape Transport

3.5.2.4.1.4.2.1 General

(1) All communications between the MTC and the MTT shall be via twisted pairs and data line driver/input amplifier combination, specified in Appendix II, unless otherwise noted.

(2) A logical "l" shall be 0 + 0.5 -0.0 volts and a logical "O" shall be 4 ± 1 volts, unless otherwise noted.

(3) The MTT shall gate all signals with the select line, unless otherwise noted.

3.5.2.4.1.4.2.2 Seven Data Lines - Seven Data lines, indicating the information to be written on the taps, shall be transmitted to all MT'I"s.

3.5.2.4.1.4.2.3 Data Strobe - A Data Strobe line, indicating valid data to the MTT shall be transmitted to all MTT's. The Data Strobe shall be a 2.0 microsecond (min.) pulse; the data lines shall remain stable for the duration of the pulse and for 2 microseconds (min.) after the Data Strobe pulse.

3.5.2.4.1.4.2.4 Select Line - One Select line shall be transmitted to each MTT indicating the computer selection to the MTT. The Select line shall be a logical "l" as long as the MTT is selected.

3.5.2.4.1.4.2.5 Forward - A Forward line, indicating to the MTT that it shall move the tape in the forward direction, shall be transmitted to all MTT's. The Forward line shall be logical "l" as long as the tape is to travel in the forward direction.

3.5.2.4.1.4.2.6 Reverse - A Reverse line, indicating to the MTT that it shall move the tape in the reverse direction, shall be transmitted to all MTT's. The Reverse line shall be a logical "l" as long as the tape is to travel in the reverse direction.

3.5.2.4.1.4.2.7 Rewind - A Rewind signal, indicating to the MTT that it shall rewind the tape to the load point, shall be transmitted to all MTT's. The Rewind signal shall be a logical "l" for 2.0 microseconds (min.).

3.5.2.4.1.4.2.8 Read - A Read line, indicating to the MTT that it shall read data from the tape, shall be transmitted to all MTT's. The Read line shall be a logical "1" as long as the MTT is to read data.

3.5.2.4.1.4.2.9 Write - A Write line, indicating to the MTT that it shall write data onto the tape, shall be transmitted to all MTT's. The Write line shall be logical "l" as long as the MTT is to write data.

3.5.2.4.1.4.2.10 Write Reset - A Write Reset signal, indicating to the MTT that it shall reset its write register, shall be transmitted to all MTT's. The Write Reset signal shall be a logical "l" for 2.0 microseconds (min.).

3.5.2.4.1.4.2.11 Three Packing Density - Three Packing Density lines, indicating to the MTT a packing density of 800, 555.5, or 200 bits per inch, shall be transmitted to all MTT's. Only one Packing Density line shall be a logical "l" at any one time; however, the chosen Packing Density line shall remain a logical "1" for as long as the function being performed is active.

3.5.2.4.1.4.2.12 Two Address Lines- Two Address lines, indicating that the address of given MTT is to be as manually selected from Logic Unit 2 shall be transmitted to each MTT. Only one Address line shall be a logical "1" at any one time and shall remain active until some manual intervention occurs.

3.5.2.4.1.4.2.13 Interlock - Two interlock lines shall be provided to the MTT. Continuity shall exist between the two lines only while MTC power is turned on and the MTC subassembly which provides motion commands to the MTT is in its normal operating position.

3.5.2.4.1.4.2.14 MTT Test Enables (Five Lines) - When an 'MTT Test Enable Line is a logic "1" that test mode shall be enabled.

3.5.2.4.1.4.3 Magnetic Tape Transport to Magnetic Tape Control

3.5.2.4.1.4.3.1 General

(1) All communications between the MTT and the MTC shall be via twisted pairs and data line driver/input amplifier combinations, unless otherwise noted. (See Appendix II for Input Amplifier Specifications.)

(2) A logical "1" shall be 0 +0.5 -0.0 volts and a logical "0" shall be plus 4 ±1 volts, unless otherwise noted.

(3) The MTC shall gate all signals with the select line, unless otherwise noted.

3.5.2.4.1.4.3.2 Seven Data Lines - Seven Data lines, indicating the information read from the tape, shall be transmitted from each MTT to the MTC.

3.5.2.4.1.4.3.3 Data Strobe - A Data Strobe line, indicating valid data to the MTC, shall be transmitted from each MTT to the MTC. The Data Strobe shall be a 2.0 microsecond (min.) pulse; the data lines shall remain stable for the duration of pulse and for 2 microseconds after the Data Strobe pulse.

3.5.2.4.1.4.3.4 Select Acknowledge - One Select Acknowledge line, indicating that the MTT has recognized the Select Line, shall be transmitted from each MTT to the MTC. The Select Acknowledge line shall be a logical "1" as long as the MTT is selected. If two cables are used for the MTC/MTT interface, the Select signal and the Select Acknowledge signal shall not be in the same cable.

3.5.2.4.1.4.3.5 Load Point - One Load Point line, indicating that the tape is at the load point, shall be transmitted from each MTT to the MTC. The Load Point line shall be a logical "1" as long as the "tape is at load point. The MTC shall not gate this signal line with the Select line except when used for Satus Word.

3.5.2.4.1.4.3.6 End of tape Warning - One End of Tape Warning, indicating that the tape marker has passed the end of tape sensor, shall be transmitted from each MTT to the MTC.

3.5.2.4.1.4.3.7 Ready - One Ready line, indicating that the MTT is not in a fault condition, shall be transmitted from each MTT to the MTC. The Ready line shall be a logical "1" as long as the MTT is in the Ready condition. The MTC shall not gate this signal line with the Select line except when used for Status Word.

3.5.2.4.1.4.3.8 Rewinding - One Rewinding line, indicating that the tape is rewinding shall be transmitted from each MTT to the MTC. The Rewinding line shall be a logical "1" as long as the MTT is rewinding tape.

3.5.2.4.1.4.3.9 Write Lockout - One Write Lockout line, indicating that the tape supply reel does not contain a write permit ring, shall be transmitted from each MTT to the MTC. The Write Lockout line shall be a logical "1" as long as the supply reel does not contain a write permit ring. The MTC shall not gate this signal line with the Select line except when used for Status Word.

3.5.2.4.1.4.3.10 Low Tape - One Low Tape line indicating that the tape is at a point in the 100 to 1000 feet remaining range, shall be transmitted from each MTT to the MTC. The Low Tape line shall be a logical "1" as long as the tape remaining is less than the preset amount.

3.5.2.4.1.4.3.11 Tape Remaining - Two Tape Remaining lines, indicating the amount of tape remaining from 0 to 2400 feet, shall be transmitted from each MTT to the MTC. These two lines shall provide an analog voltage to drive a calibrated 0 to 1 ma meter. The MTC shall not gate this signal with the Select line.

3.5.2.4.1.5 Test Functions - The following functions shall be included in the Maintenance Control Panel of Logic Unit 2 to be used in conduction with the DMTSS.

3.5.2.4.1.5.1 DMTSS Test - A maintenance (or Off-Line) mode of operation shall be provided that shall permit complete subsystem testing of the DMTSS independent of the computer. It shall be possible to manually enter a 30-bit Instruction word from the MC P to the MTC. If the MTC normally requires a data word following the Instruction, the Instruction is placed in a special set of switches on the MCP and the data word is placed in the MCP data register. In addition to the normal repertoire of Instructions listed in the Function Code description, the Instruction word shall include a word count in bit positions 0-8 to specify the number of times a word is to be written or read. A Timing Error (peculiar to the Off- Line mode) shall be generated if the record which has been read has fewer or more words than the specified count.

It shall be possible to perform all of the instructions of the MTC repertoire from the MC P with the options of Single Instruction, Repeat Instruction or Repeat Instrue - tion with Halt on Error. The MC P shall also include a Cycle Mode. In this mode of operation, the MTT shall read forward from an end of file until the next end of file is reached and then read reverse to the initial end of file. The same options of Single Instruction, Repeat Instruction or Repeat Instruction with Halt on Error shall be possible. If the MCP operating mode selection switch is in the normal or On-Line mode, actuation of any of the MCP switches used for maintenance shall not have any effect on DMTSS operation.

3.5.2.4.1.5.2 MTC Test - A maintenance mode of operation shall be provided that shall pemit testing of the MTC independent of the computer and the MTT. It shall be possible to single step, by means of manual execution of MTC test mode operations, the control logic and data transfers of the MTC through the logic steps associated with all of the instructions of the DMTSS repertoire. The loop gates shall be active in this mode to bypass the MTT and the source of data shall be the MCP.

3.5.2.4.1.5.3 MTT Test - A maintenance mode of operation shall be provided that shall allow the MTC to control the MTT independent of the computer. This mode of operation shall make it possible to write or read continuously with an End of Tape terminating the operation in the forward direction. It shall also be possible to select sequences of Forward-Stop operation, Reverse- Stop operation and Forward Stop Reverse operation with the drive command times and stop times determined by selection switches on the MCP. The selectable drive command and stop times shall be 5, 10, and 320 milliseconds. Test points shall be provided that will permit oscilloscope synchronizing and display of drive commands and internal test signals.

3.5.2.4.1.5.4 MTT Display and Selection - Logic Unit 2 shall include a continuous display of the three MTT status conditions of Ready, Load Point and Write Lockout. It shall include two calibrated meter displays of tape remaining from O to 2400 feet.

3.5.2.4.1.5.5 MTT Address Selection - Logic Unit 2 shall include one two-position Address switch to change the address selection of the MTT.

3.5.2.4.1.6 Detailed Description of the Operation of DMTSS

3.5.2.4.1.6.1 Idle State - In the idle state the MTC will contain the Status information of the previously executed instruction. If the MCP is in the normal or On-Line mode, the MTC

will send an External Function Request to the computer (the Output Data Request is kept low at this time). When the computer responds with an External Function line, the Function word on the corn- , puter output lines will be transferred to the instruction storage register in the MTC and the status storage of the MTC will be cleared or initialized unless the instruction was an 02 (Status Report). For any Function Code the MTC will select the MTT specified by bits 17-18 of the Function word to insure that the MTT status is appropriate for the operation to be performed. The Function word address bits will be compared with the Address Selection switch of the MC P. If the Function word does not specify an existing MTT or specifies more than one, the Illegal Instruction Status condition will be set and the Normal Completion Status condition reset provided that the Instruction requires the selection of an MTT.

For any Function Code except the codes specifying a Rewind, Satus Report, Master Clear or Loop Instruction where the packing density is not specified, the Illegal Instruction condition will be set and the Normal Completion Status condition reset. If the selected MTT does not respond with a select acknowledge and ready signal, the Fault Satus condition will be set and the Normal Completion condition reset. If the Function Code specifies a Write operation and the MTT Satus is Write Lockout, the Fault Status and Write Lockout conditions will be set and the Normal Completion Status condition reset. If the Function Code specifies a Reverse Direction command and the MTT Status is Load Point, the Illegal Operation Status condition will be set and the Normal Completion Status condition reset.

For any Function Code except the codes specifying the Status Report or Rewind Instruction, if the MTT Status is Rewinding, the Normal Completion Status condition will be reset. If the Function Code specifies a Rewind Instruction and the MTT does not respond with a Rewinding Status within four to ten microseconds, the Normal Completion Status condition will be reset. When in the idle state if the Normal Completion Status condition is reset for any reason, the MTC will not proceed with the instruction and no direction command will be sent to the MTT. If the Interrupt Enable from the computer is a logical ‘1” the MTC will send an Interrupt to the computer and transfer all Status information to the computer input data lines. If the Interrupt Enable from the computer is a logic “0”, the MTC will revert to the idle state; however, the Status signals will still be available for Status Report function.

3.5.2.4.1.6.2 Write Function - When a Write class of Instruction, Write or Write Extended Interrecord Gap, is received by the MTC and the idle state is normal, the MTC will send an Output Data Request to the computer. At the same time, the MTC will send Forward, Write, and Read commands to the MTT and initiate the start time delays.

If the MTT is at load point, a delay time corresponding to a nominal 3-1/2 inch distance between the load point marker leading edge and the first character of the record will be timed. If the MTT is not at load point, the MTC will time a start distance determined by the Instruction (normal or extended interrecord gap) and the original Status. The MTC is now ready to write the Data words one frame (character plus designated parity bit) at a time on the tape at the specified density.

If the computer has not responded to the Output Data Request with an Output Acknowledge indicating there is a Data word on the computer output line to be written within the gap time, the MTC will set the Timing Error Status condition and reset the Normal Completion Status. If the computer does respond to the Output Data Request, the MTC will transfer the word into storage and request the second word from the computer. The MTC will have requested and received at least one and possibly two words from the computer before the MTT is ready to write the first character on tape. The MTC will count and transfer the characters to be written. When a full word has been written (five characters) an Output Data Request is sent to the computer.

The timing of Output Data Requests from the MTC will now be determined by the density at which data is being written on the tape. The process will continue until the computer does not respond to an Output Data Request within the time allowed to write a word on tape at the requested density. The MTC will recognize a no data condition and will time a

delay corresponding to a three-character spacing and then send a Write Reset command to the MTT to Write the longitudinal parity bits on the tape. The MTC will then time a delay corresponding to the "write to read" head spacing. If the instruction has resulted in a Normal Completion, i.e. , no Lateral or Longitudinal Parity Error, and no End of Tape Warning, the MTC will send an External Function Request to the computer and wait while the MTC times the' Repeat Instruction Request time (300 µs). If the computer does not respond with an External Function line during the Repeat Instruction Request time, the MTC will terminate its External Function Request and wait an additional 16 microseconds for the External Function command. If no External Function command is received, the MTC will initiate the Stop Timing and terminate the Forward and Read commands to the MTT. If the Interrupt Enable from the computer is a logical "1", the MTC will send an Interrupt to the computer and transfer the Status word. When the Interrupt is acknowledged and the MTC has completed the stop time, the MTC will terminate the Write signal and return to the idle state. If the computer responds to the External Function Request during the Repeat Instruction Request time, or during the following 16 microseconds, the MTC will set a Continue Condition Status, examine the new word for a change in Parity, or Density, send an Interrupt to the computer, and transfer the Status word.

The MTC will sense the Continue condition and time a delay corresponding to the specified Interrecord Gap distance without stopping tape motion. During this time the MTC will complete its function as described above and bypass the idle state to initiate another Write operation. From this point the operation will continue as if the Instruction originally proceeded from the idle state.

If the End of Tape Warning is sensed, the MTC will perform the Instruction for a time approximately equal to 10 inches of tape for data before terminating the Instruction and sending an Interrupt to the computer. If an Instruction is completed within the 10 inch segment of tape following the End of Tape Warning, no new Forward Instruction will be executed.

If the Instruction has resulted in a Normal Completion, the MTC sets EFR for the Repeat Instruction Request time. If the computer does not respond with an EF during the Repeat Instruction Request time, the MTC resets the EFR and waits approximately 16 microseconds for a late E F from the computer. If there is no EF from the computer during this time, the MTC initiates the Stop Timing. At this time if the Interrupt Enable is logical "1", the MTC sets the Interrupt line and transfers the Status word. If Interrupt Enable is a logical "0", the MTC stores the fact that an Interrupt is needed and waits for the Interrupt Enable to become a logical "l" at which time an Interrupt is sent.

If the Instruction has resulted in a Normal Completion and the computer does respond with an E F during the Repeat Instruction Request time, the MTC will send an Interrupt at the completion of the Repeat Instruction Request time if the Interrupt Enable is a logical "1". If the Interrupt Enable is a logical "0", no Interrupt is sent and the MTC enters the Instruction.

If the Instruction results in something other than a Normal Completion, the MTC will not send an EFR during the Repeat Instruction Request time. At the end of this time an Interrupt is sent to the computer if the Interrupt Enable line is a logic "1". If the Interrupt Enable line is a logic "O", the fact that an Interrupt is needed is stored and the Interrupt is sent when the Interrupt Enable line becomes a logical "1".

3.5.2.4.1.6.3 Read Function - When a Read class of Instruction, Read Record Forward or Read Record Reverse, is received by the MTC and the idle state is normal, the MTC will send the appropriate direction command and read control signal to the MTT. The MTC will perform the Instruction for the first character from the MTT. If the End of Tape Warning is sensed, the MTC will wait for a time equal to ten inches of tape before terminating the Read and sending an Interrupt to the computer. If the Instruction is completed within the 10 inches of tape following the End of Tape Warning, no new forward motion Instruction will be executed. The first character from the MTT will be checked for proper parity and transferred to storage. The MTC will then initiate a delay time determined by the packing density and tape speed and wait for the next character from the MTT. If the second character is not received within the specified time, the first character may have been the Longitudinal Parity Character in a Read Reverse or a Tape Mark. The MTC will initiate the delay time again and wait for the second character. If the first and second characters were Tape Marks, no more data will be received and the End of File Status condition will be set if both characters are

decoded as Tape Marks (0001111) or if one is decoded as a Tape Mark and the other has a single bit error. If the second character is received within the second delay time and is followed by a third within one delay time, the first character will be discarded since it was the Longitudinal Parity character. The process *of* waiting for characters, checking parity and transferring the characters to storage will continue with the MTC counting the characters received. When five characters have been received, the MTC will set a full condition. The MTC will send an Input Data Request to the computer, transfer the Data word, and wait for an Input Acknowledge. If the computer responds within the word transfer time determined by the packing density, the MTC will reset the Full Condition. The MTC will set the Full Condition when five more characters have been received and the process will continue until no more data is received from the MTT or until the computer does not respond to the Input Data Request within the word transfer time. If the computer does not respond, the MTC will set the Timing Error Status condition and drop its Input Data Request. In either event the MTC will continue its operation until no more data characters are received from the MTT. If the instruction has resulted in a normal completion, the MTC will send an External Function Request to the computer and wait while the MTC times the Repeat Instruction Request time. If the computer does not respond with an External Function command during the Repeat Instruction Request time, the MTC will terminate its External Function Request and wait an additional 16 microseconds for the External Function command. If no External Function is received, the MTC will initiate the stop timing and terminate the Forward or Reverse command to the MTT. During this time the MTC will place the Status word on the data lines and send an Interrupt to the computer. If the Interrupt Enable from the computer is a logical “1”, the MTC will wait for an Input Acknowledge. When the Interrupt is acknowledged and the MTC has completed the stop time, the MTC will return to the idle state. If the computer responds to the External Function Request during the Repeat Instruction Request time or during the following 16 microseconds, the MTC will set a Continue condition, place the Status word on the input data lines, and send an Interrupt to the computer. The MTC will sense the Continue condition and initiate the new Instruction without stopping tape motion. During this time the MTC will complete its function as described above and bypass the idle state to initiate another Read operation. From this point the operation will continue as if the Instructions originally proceeded from the idle state.

If the Instruction is a Read Reverse, the MTC will assemble the characters in the correct order.

If the Instruction has resulted in a Normal Completion, the MTC sets EFR for the Repeat Instruction Request time. If the computer does not respond with an EF during the Repeat Instruction Request time, the MTC resets EFR and waits approximately 16 microseconds for a late E F from the computer. If there is no EF from the computer during this time, the MTC initiates the Stop Timing. At this time if the Interrupt Enable is logical “1”, the MTC sets the Interrupt line and transfers the Status word. If the Interrupt Enable is a logical “0”, the MTC stores the fact that an Interrupt is needed and waits for the Interrupt Enable to become a logical “1” at which time an Interrupt is sent.

If the instruction has resulted in a Normal Completion and the computer does respond with an E F during the Repeat Instruction Request time, the MTC will send an Interrupt at the completion of the Repeat Instruction Request time if the Interrupt Enable is a logical “1”. If the Interrupt Enable is a logical “O”; no Interrupt is sent and the MTC enters the instruction.

If the Instruction results in something other than a Normal Completion, the MTC will not send an EFR during the Repeat Instruction Request time. At the end *of* this time an Interrupt is sent to the computer if the Interrupt Enable line is a logical ‘1”. If the Interrupt Enable line is a logical “O”, the fact that an Interrupt is needed is stored and the Interrupt is sent when the Interrupt Enable line becomes a logical *’1”.

3.5.2.4.1.6.4 Search File Forward - When the Search File Forward instruction is received and the idle state is normal, the MTC will send an External Function Request to the computer and set the MTC full condition. At the same time, the MTC will initiate the same functions that are performed in the Read operation. If the computer does not respond with an External Function Line indicating the Identifier word is on the computer output lines before the MTC receives the first data character from the MTC, the MTC will set the Timing Error Status condition and terminate its External Function Request. The MTC will then wait until the MTC stops receiving data from the MTT, send an Interrupt to the computer and transfer the Status information to the computer. If the computer does

respond with an External Function line, the Identifier word will be transferred into MTC storage and as the first word is received, it will be compared character by character with the Identifier word. If the five characters compare, the operation will become identical to the Read operation and the record will be transferred to the computer. If the first word does not compare, the MTC will wait until the first word of the following record is received and make the comparison again. The operation will continue if Normal Completion is not reset until a Find is made or until an End of File is reached.

3.5.2.4.1.6.5 Search File Reverse - Read Record Forward - This Instruction will duplicate the Search File Forward Instruction except the direction command to the MTT will be Reverse and the MTC will make the comparison with the last word read in each record with the characters in the correct order. When a Find is made, the MTC will stop the MTT and the MTC will initiate a Read Record Forward Instruction.

3.5.2.4.1.6.6 Loop Instruction - When the Loop Instruction is received by the MTC in the idle state (except that no MTT will be selected) the MTC will send an Output Data Request to the computer and when the computer responds with an Output Acknowledge the MTC will transfer the Data word into its data storage register. The MTC will then send an Input Data Request to the computer and transfer the Data word to the computer input lines. When the computer responds with an Input Acknowledge, the MTC will form the selected parity for each character, transfer the characters through the data loop paths which bypass the line drivers and input amplifiers thereby bypassing the MTT's, check the characters for Lateral Parity and compare the characters with the correct ones stored in the word register. The MTC will then send an Input Data Request to the computer and transfer the re-assembled word to the computer input lines. When the computer responds with an Input Acknowledge, the MTC will send an InTerrupt to the computer and transfer the status information to the computer input lines.

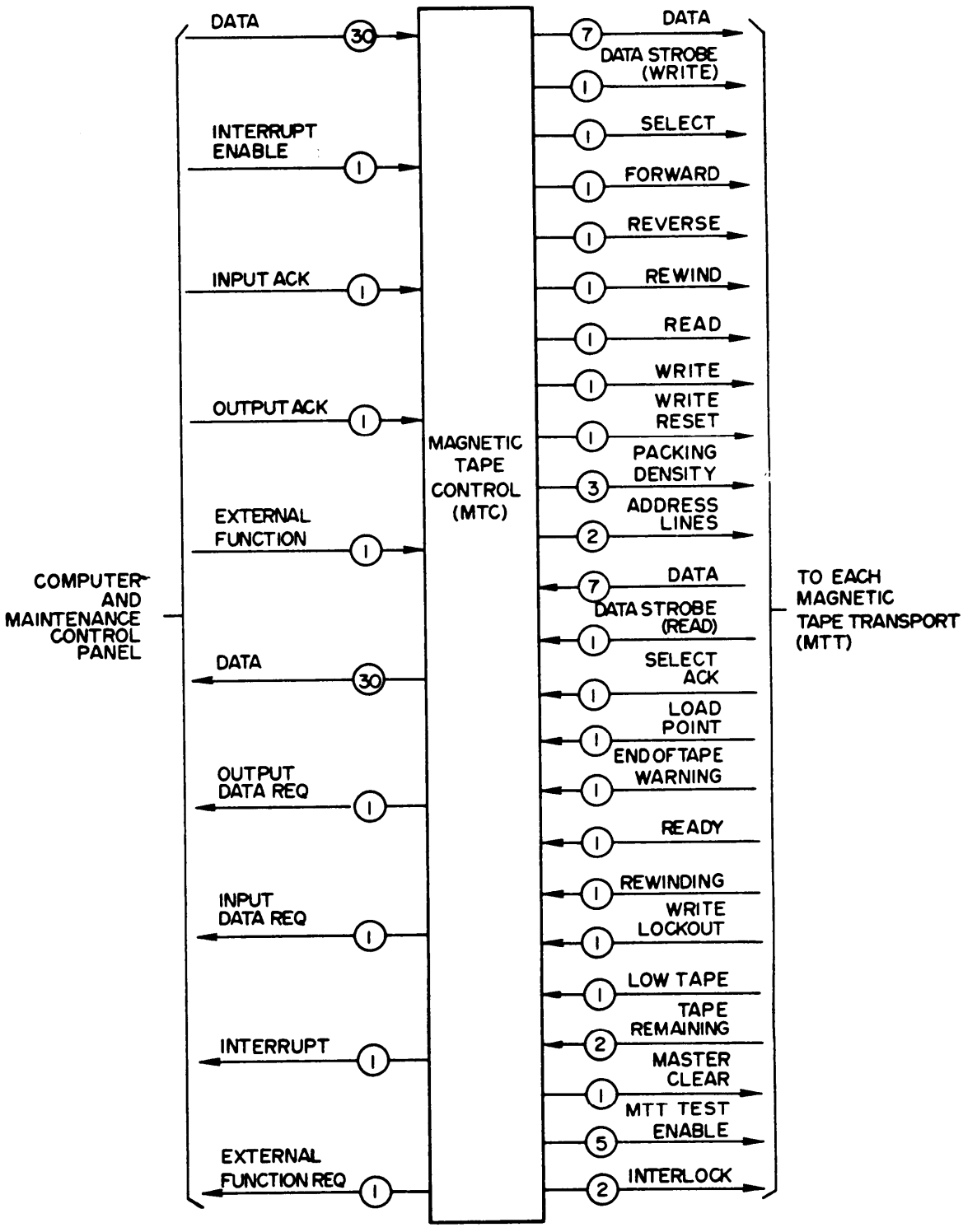


Figure 56. Magnetic Tape Control, Functional Flow Diagram

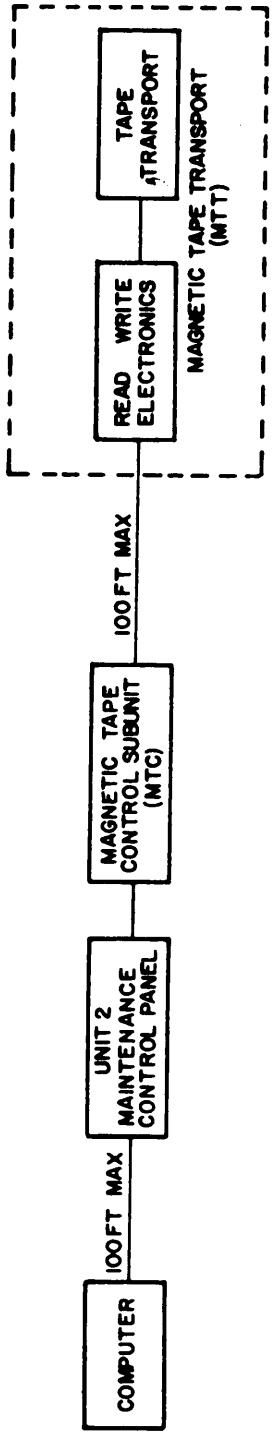


Figure 57. Digital Magnetic Tape Subsystem, Block Diagram

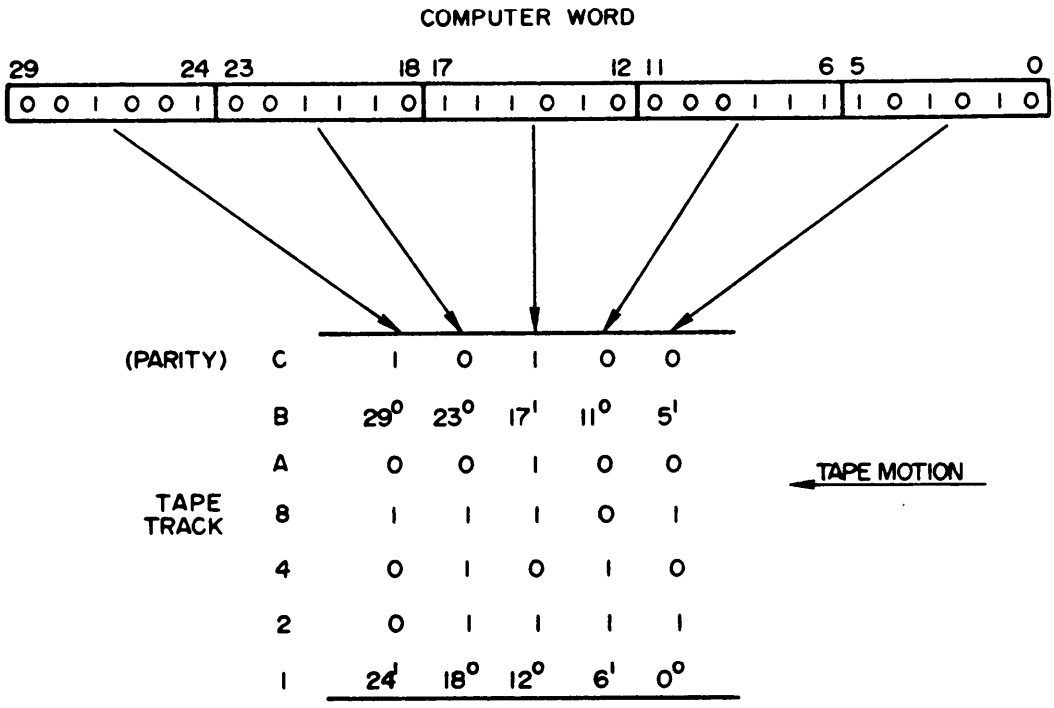


Figure 58. Correspondence Between Computer Word and Tape Track Storage of that Data

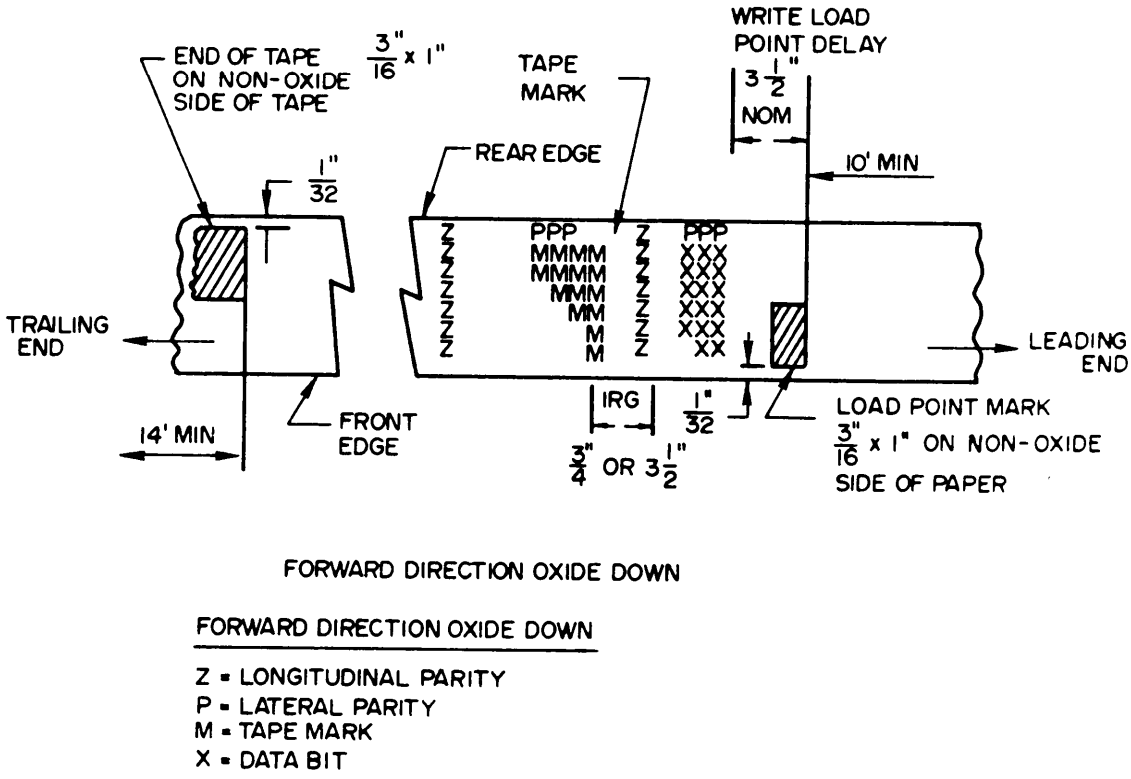


Figure 59. Tape Format

3.5.2.4.2 Navigation Multiplexer

3.5.2.4.2.1 Functional Description - The Navigation Multiplexer (NM) is an interface unit between the computer and two inertial platforms and doppler navigation equipment.

Figure 60 is a functional flow diagram of the navigation multiplexer.

3.5.2.4.2.2- General Description - The NM shall have the capability of transmitting data bits from the inertial platforms and the doppler navigation equipment to the computer. Each inertial platform and doppler navigation equipment shall use a single serial line for data to the NM.

3.5.2.4.2.3 Operating Requirements

3.5.2.4.2.3.1 Data Transfer - A peripheral equipment which communicates with the computer via the NM shall be able to transmit one data word to the computer by following the control line sequence given below.

(1) The computer requests the information required by using its Normal Output Function (Output Acknowledge).

(2) The NM generates the select line for that function and starts the clock.

(3) The peripheral sends the data to the NM using the 22 clock bits from the NM.

(4) The NM places the data bits from the peripheral equipment on the computer data lines.

(5) The NM sets the Input Data Request Line to indicate that it has data ready for transmission to the computer.

(6) The Computer 1/0 Subunit detects the Input Data Request.

(7) The computer samples the data lines, at its convenience.

(8) The computer sets the Input Acknowledge Line indicating that it has sampled the data.

(9) The NM drops the Input Data Request.

3.5.2.4.2.3.2 Timing, Priority and Initialization

(1) The computer selects the peripheral unit and function to be transmitted.

(2) The NM shall be self-initializing, i.e. , when power is applied to the NM, no spurious data shall be transmitted to the computer and the NM shall be ready for normal operation.

3.5.2.4.2.3.2.1 Navigation Word Sampling - Each word shall be sampled at random times but not more often than once every 30 milliseconds.

3.5.2.4.2.4 Test Loops

3.5.2.4.2.4.1 In- Flight Performance Monitoring - The NM shall be capable of loop operation. This loop operation, Computer to NM and NM to computer, shall permit the computer program to monitor automatically the performance of the NM. The test loops shall be utilized for in-flight performance monitoring and diagnostic programs.

3.5.2.4.2.5 Interface Requirements - Refer to the NM functional flow diagram, Figure 60.

3.5.2.4.2.5.1 Computer Interface

3.5.2.4.2.5.1.1 Format of Output Word from Computer to Navigation Multiplexer - The format of the output word is shown in Figure 61.

3.5.2.4.2.5.1.2 Format of Input Word to Computer from Navigation Multiplexer - The Navigation formats of the input words to the computer from the Navigation Multiplexer are shown in Figures 62 through 65.

3.5.2.4.2.5.1.3 Signal Characteristics -All communications between the NM and the computer shall be via twisted pairs and data line driver/input amplifier combinations. Input amplifiers are defined in Appendix II.

3.5.2.4.2.5.2 Peripheral Interface

3.5.2.4.2.5.2.1 Formats of Input Words to Navigation Multiplexer from Peripheral Equipment - The formats of the input words from the Navigation Equipment to the Navigation Multiplexer are shown in the following tabulation:

CLOCK PULSE NUMBER	V_{NORTH}	V_{EAST}	TRUE HEADING	DIST ALONG HEADING	DIST ACROSS HEADING	ALTITUDE
1	0	0	0	0	0	0
2	0	0	0	0	1	1
3	0	0	0	1	0	1
4	0	0	0	OVE	S	0
5	0	0	1	MSB	OVE	0
6	0	1	0		MSB	0
7	1	0	0			0
8	S	S	MSB			0
9	MSB	MSB				MSB
10						
11						
12						
13						
14						
15						
16						
17						
18						
19						
20						
21						
22	LSB	LSB	LSB	LSB	LSB	LSB

OVE = Overflow

MSB = Most Significant Bit

LSB = Least Significant Bit

Signal Characteristics -Refer to Figure 66.

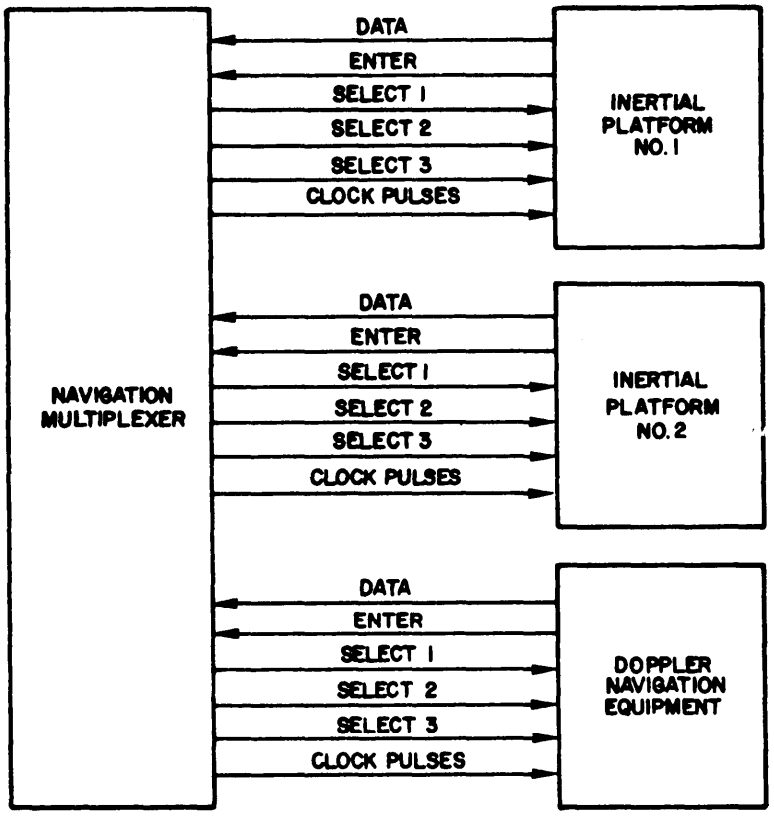


Figure 60. Navigation Multiplexer, Functional Flow Diagram

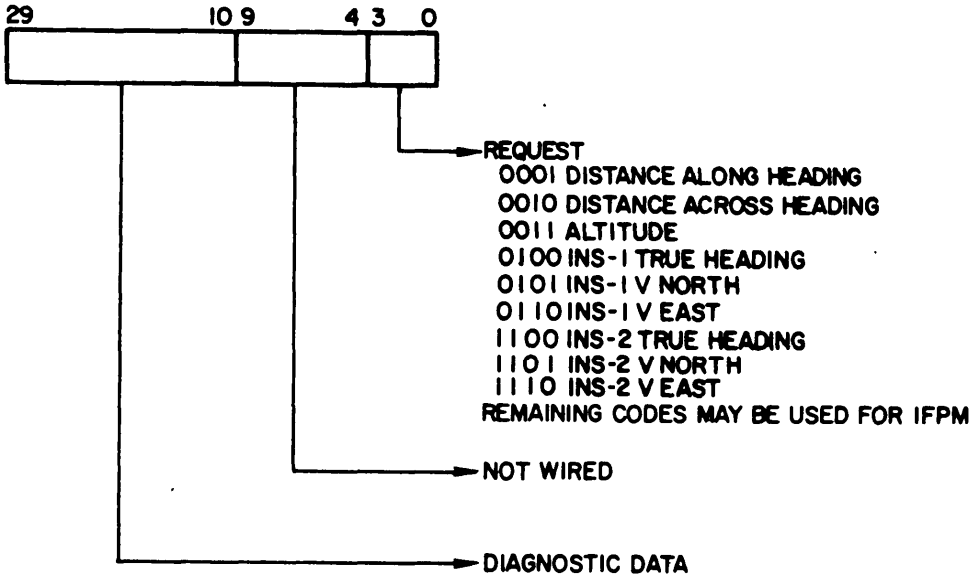


Figure 61. Format of Output Word From Computer to Navigation Multiplexer

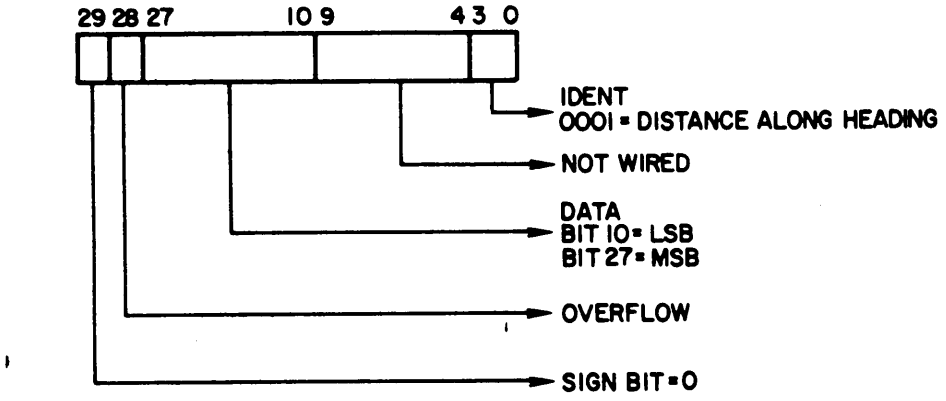


Figure 62. Format of Input Word (Distance Along Heading) to Computer from Navigation Multiplexer

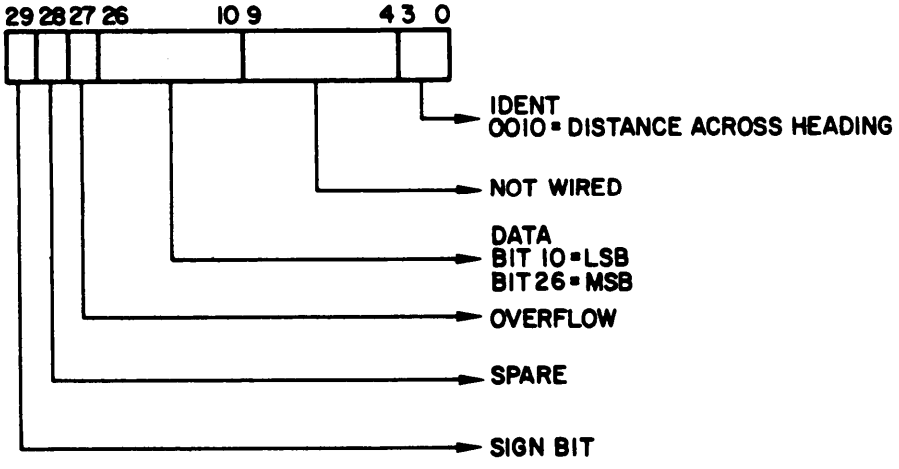


Figure 63. Format of Input Word (Distance Across Heading) to Navigation Multiplexer from Computer

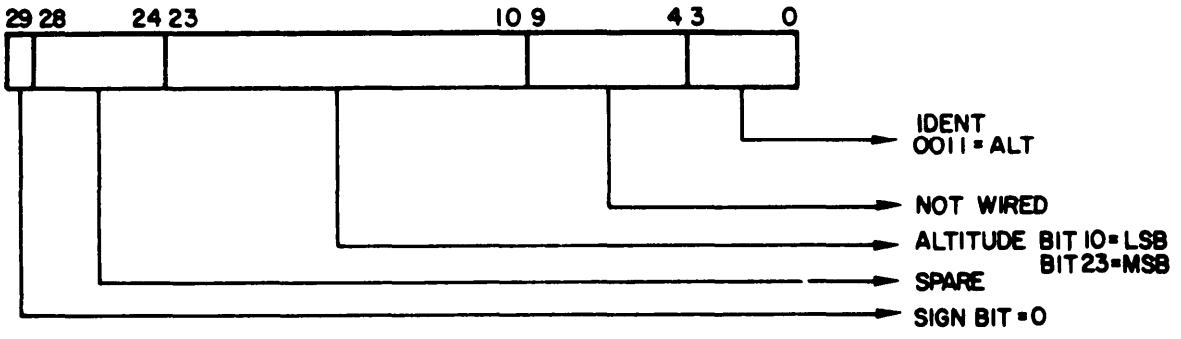


Figure 84. Format of Input Word (Altitude) to Computer from Navigation Multiplexer

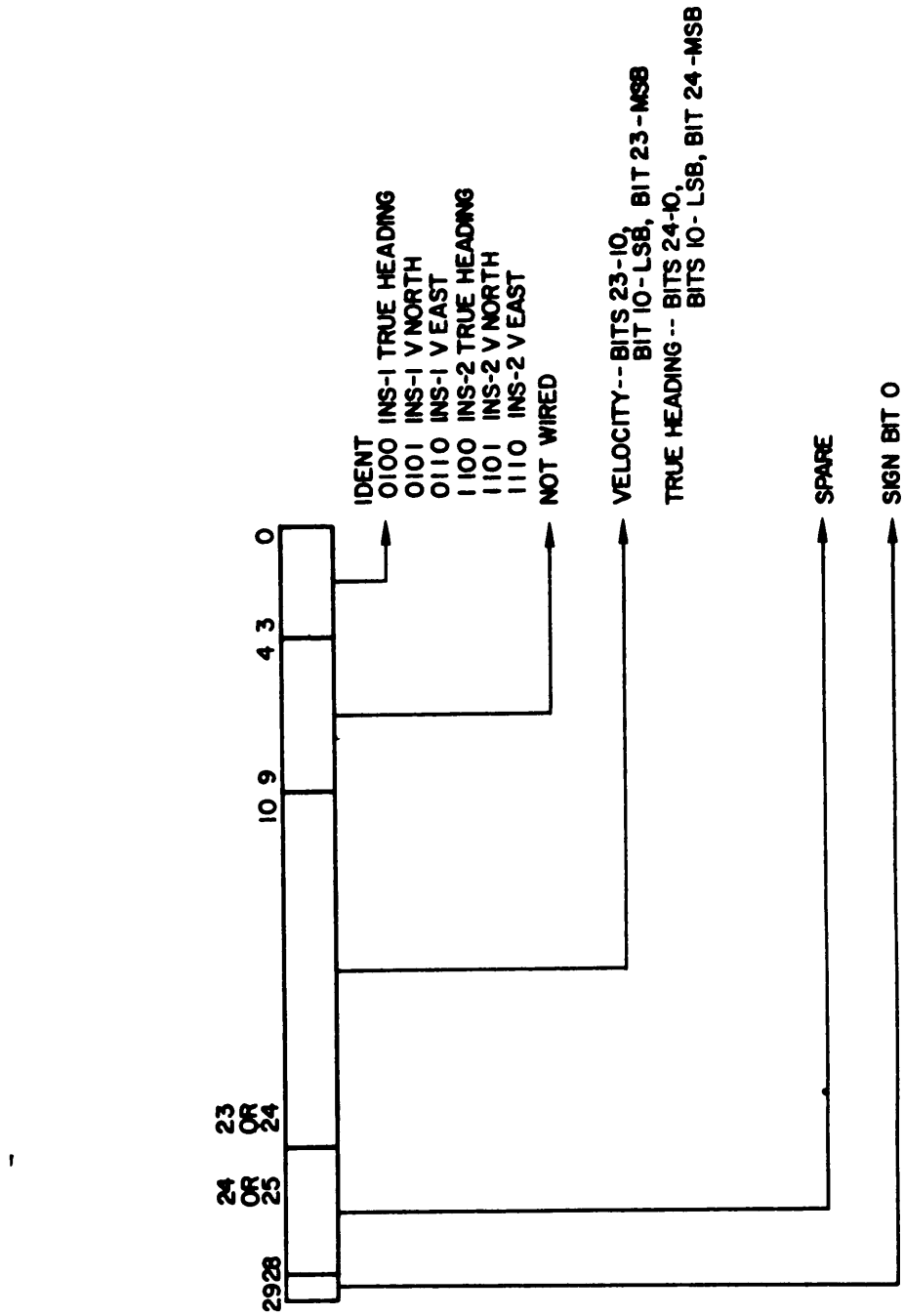


Figure 65. Format of Input Word (INS 1 and 2 Velocity and True Heading) to Computer from Navigation Multiplexer

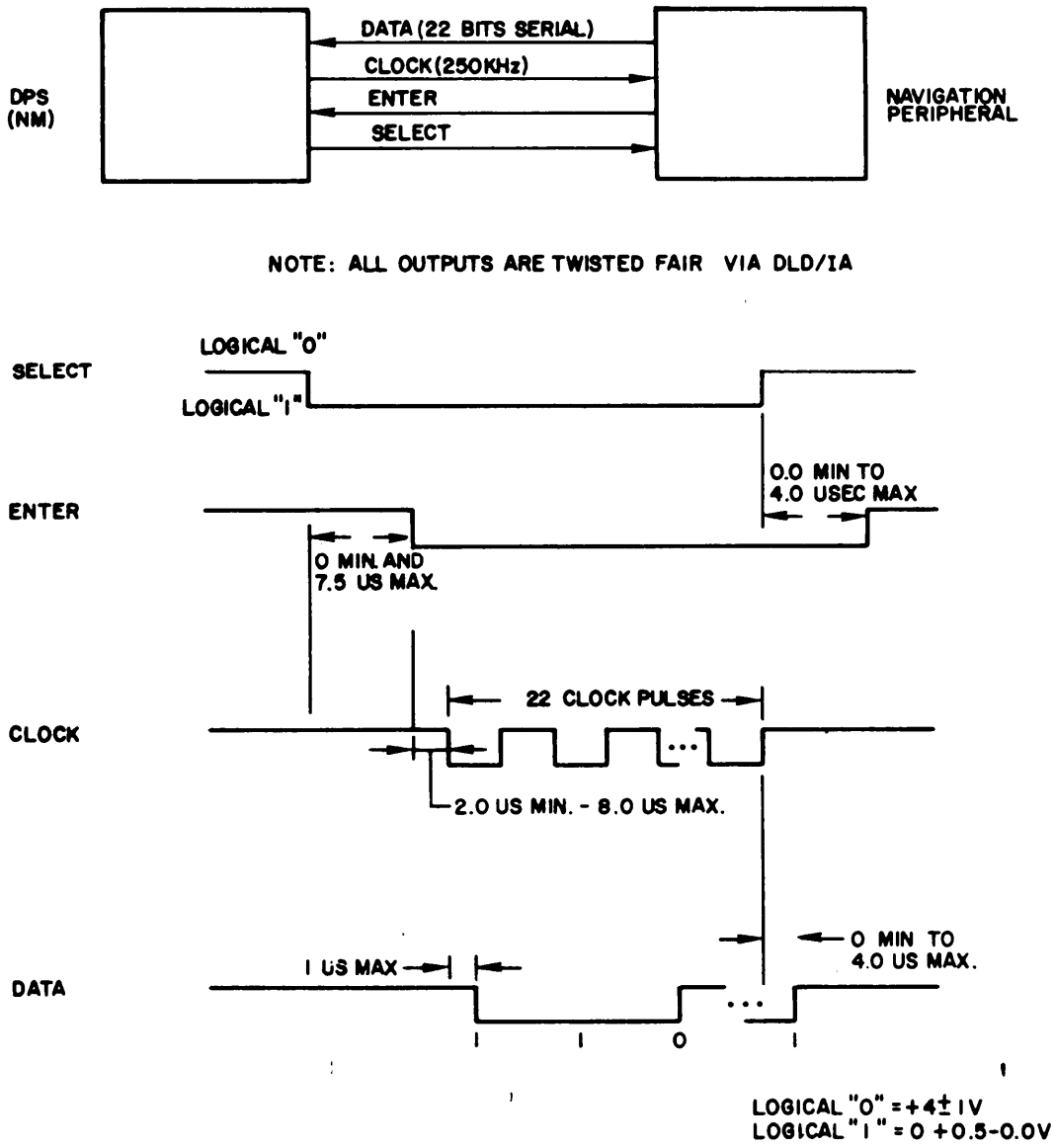


Figure 66. Signal Characteristics for Data Transfer between Navigation Multiplexer and Navigation Equipment

3.5.2.4.3 Armament/Ordnance Input Logic (AOIL)

3.5.2.4.3.1 Functional Description

3.5.2.4.3.1.1 Aircraft Armament System - The Aircraft Armament System controls the following:

(1) Ten Wing Weapon Stations

(2) Eight Bomb Bay Weapon Stations

Weapon Stations are loaded before a flight and cannot be changed or reloaded during a flight. A weapon must be armed prior to launching. Weapon arming is not selective (i. e. , all weapons are armed or disarmed at either the wing or bomb bay station at once) and may be one of three types - Nose arm, Tail arm, or Nose and Tail arm. Two outboard wing weapon stations on either side can carry single rocket launchers or rocket pods. The four rockets in a pod may be launched one at a time (Rocket Single) or in rapid succession (Rocket Ripple).

3.5.2.4.3.1.2 Aircraft Armament System - The Aircraft Ordnance configuration consists of the following:

(1) 48 fixed sonobuoy launcher tubes (SLT) (“A” size). Twenty-four of these tubes may be breech loaded or unloaded in flight. All 48 chutes are unpressurized.

(2) Three pressurized sonobuoy launchers (“A” size).

(3) Two circular rotating SUS dispensers with 39 SUS capacity each. One will contain Deep SUS, the other Shallow SUS.

(4) Total “A” size stowage is 112. Forty-eight will be carried in the chutes and an additional 64 in cabin bins.

(5) “B” chute (free fall).

All chutes, with the exception of the “B” chute, will have the capability for automatically setting sonobuoy life and depth.

For any pressurized launcher the bottom aircraft door for the launcher must be closed prior to loading, and opened prior to launching (by the computer). A top door (which is manually operated) must be closed prior to launching.

3.5.2.4.3.1.3 Interface Logic - The Armament and Ordnance Output Logics (AOL and OOL) are the interface subunits between the computer and the Aircraft Armament and Ordnance Systems. These interface logics allow the computer to exercise control over the aircraft systems and will be described in later sections.

The Armament/Ordnance Input Logic (AOIL) allows the computer to receive station and switch position information from the Aircraft Armament Ordnance Systems. The AOIL also receives error and inhibit signals from the AOL and the OOL. Status information includes “stores-in-place” for the 18 Weapon Stations, and the 2 SUS launchers. (A store is considered to be a weapon--torpedo, rocket, depth charge, mine, bomb--when referring to the Armament System and a sonobuoy, BUSS or SUS when referring to the Ordnance System). In addition, status information includes door status (doors fully open or not fully open) for the bomb bay door, the three pressurized sonobuoy launcher doors; and manual switch status for the Search Power, Master Arm, Manual Weapon Release, Kill Store Manual Mode and Manual Torpedo Preset Switches. Chute Status is determined by an interrogate command and selection of one of 51 launchers.

The AOIL informs the computer of a depression of either the Pilot's or Co-Pilot’s Weapon Release switch. Error information received from the error detection circuitry of the AOL and OOL is also transmitted by the AOIL to the computer.

Figure 67 is a functional flow diagram of the AOIL.

3.5.2.4.3.2 General Description - The AOIL shall perform the following functions:

(1) Enter to the computer up to six types of error information received from the OOL and the AOL.

(2) Detect a depression of the Pilot/Co-Pilot's Manual Weapon Release switches and enter this information to the computer.

(3) Enter to the computer the status of the following items, upon detection of change of status or upon computer interrogation:

(a) Ten Wing Weapon Stations

(b) Eight Bomb Bay Weapon Stations

(c) Two SUS Away

(d) Three Pressurized Doors

(e) Bomb Bay Door

(f) Three Bomb Bay Special Weapon Rack Locks

(g) Three Special Weapon Select Monitors

(h) Manual Torpedo Preset Monitor

(i) Search Power Switch

(j) Master Arm Switch

(k) Kill Store Manual Mode Switch

(4) Enter to the computer the SLT Status upon computer request.

3.5.2.4.3.3 Operating Requirements - The function of the AOIL shall be to inform the computer of the status of the Aircraft Armament and Ordnance Systems. The required information to be transmitted to the computer has been detailed in 3.5.2.4.3.2. Status and switch information shall be transmitted from the Aircraft Armament and Ordnance systems to the AOIL. In addition, the computer shall have the capability to request that one or more status words (to be explained below) be entered. This shall be accomplished by a computer command to the OOL, which shall then decode and transmit this information to the AOIL. Error information (i.e. , information from the error detection circuitry of the AOL and OOL) shall be sent to the AOIL from the AOL and OOL, and entered to the computer by the AOIL.

Of the various inputs, some are considered to be asynchronous and, therefore, may be grouped together into one computer word. A total of seven groupings (or individual words) have been defined (Figure 68 through 76). These input words can occur simultaneously; therefore, provisions must be made for sequentially scanning the various words for entry. If all input words were active at the same time, the AOIL shall insure that all the words would be entered within 10 milliseconds plus any delay incurred for the computer to respond to the Input Data Request and Interrupt. In addition, error and Pilot/Co-Pilot Weapon Release information (Figures 69 and 70) shall be entered with the Interrupt control link; the remaining five input words (Figures 72 through 76) shall utilize the Input Data Request.

3.5.2.4.3.4 Interface Requirements

3.5.2.4.3.4.1 Word Formats - The AOIL Word Formats are given in Figures 68 through 76.

3.5.2.4.3.4.2 Signal Characteristics- Unless otherwise noted, signal levels external to Logic Unit 2 are defined as follows:

Logical “0” = +4 ±1 volts

Logical “1” = 0.0 +0. 5-0.0 volts

3.5.2.4.3.4.3 Armament/Ordnance Input Logic to Computer - Communications between the AOIL and the computer shall be in accordance with Appendix 1. The AOIL shall provide control line drivers for Interrupt and Input Data Request and data line drivers for bits 0 through 9 and 12 through 14.

3.5.2.4.3.4.4 Armament /Ordnance Input Logic to Maintenance Control Panel Subunit - The AOIL shall provide to the MCPL the input control and dat a lines for monitoring.

3.5.2.4.3.4.5 Maintenance Control Panel Subunit to Armament/Ordnance Input Logic - The MCPL shall provide the input amplifiers for the Input Acknowledge and External Interrupt Enable for the AOIL. Data only shall be available to the AOIL.

3.5.2.4.3.4.6 Ordnance Output Logic to Armament/Ordnance Input Logic

3.5.2.4.3.4.6.1 Error Signals - As indicated previously, the OOL and AOL shall have error detection circuitry. Each Output Logic shall have the ability to detect three different types of errors. The interpretation of the error types will be found in 3.5.2 .4.4.4.5.1 and 3.5.2.4.5.4.5.1. For the present, errors will be referred to only by error type numbers.

Three error signals and an inhibit signal shall be transferred from the OOL to the AOIL. The inhibit signal shall be a logical "1" (inhibited) during the time when the External Function Request is a logical “0”. The External Function Request shall be a logical “O” for a time period between one microsecond and one millisecond if the computer output command was an Interrogate command, and 130 ±10% milliseconds for any other computer command (see 3.5.2.4.5. 3). The AOIL shall not enter any error information to the computer during the time that the inhibit is a logical “l”; therefore, any error signal occurring during this time must be stored until the inhibit becomes a logical “O”.

The Type I error signal shall be a logical “l” for 2.2 microseconds (min.). The trailing edge of this pulse shall occur during the time that the inhibit signal is a logical “1”. The Type II error signal shall be a logical “1” for an indefinite length of time. The Type III error signal shall be a logical “1” (low) for a maximum of 260 ±10% milliseconds, and shall occur during the time that the inhibit signal is a logical “1”. Following an SLT Status command, the Type III error signal may be a logical “1” for an indefinite period of time.

3.5.2.4.3.4.6.2 Interrogates - The computer shall be able to request that the AOIL enter one or more (up to five) status words. This interrogation is used primarily for initialization and system’s recovery (temporary loss of power). Four of these words (Wing Status, Bomb Bay Status, Pressurized Sono/SUS Status and Manual Switch/Door Satus) shall also be entered upon change of status.

The computer shall request the interrogation of these five words by transmitting an Interrogate command (3. 5. 2.4.5.4.1 and Figure 84) to the OOL. The OOL shall decode the computer command and transmit interrogate signals (a logical “1” for O. 5 microseconds min.) to the AOIL. Since the computer can simultaneously request any combination of the five status words, the AOIL shall store the interrogate commands until each individual word has been entered.

3.5.2.4.3.4.7.1 Error Signals - As with the OOL, the AOL shall also transmit three error signals and an inhibit signal (for these three errors) to the AOIL. In this case the inhibit signal shall be a logical “1” (inhibited) during the time when the Output Data Request is a logical “O”. (The Output Data Request is a logical “O” for 640 ±10% milliseconds if the computer output command was a Rocket Launch Command, and is 130 ±10% milliseconds for any other computer command.

(See 3.5.2.4.4.3.1.) The AOIL shall not enter any error information to the computer during the time the inhibit is a logical "1"; therefore, any error signal occurring during this time must be stored until the inhibit becomes a logical "0".

The Type IV error signal shall be a logical "l" for O. 5 microseconds min. The trailing edge of this pulse shall occur during the time the inhibit signal is a logical "l". The Type V error signal shall be a logical "1" for an indefinite length of time. The Type VI error signal shall be a logical "1" for a maximum of 640 ±10% milliseconds, and shall occur during the time the inhibit signal is a logical "1".

3.5.2.4.3.4.8 Aircraft Armament/Ordnance System to Armament/Ordnance Input Logic

3.5.2.4.3.4.8.1 Signal Characteristics - Signals from the Aircraft Armament and Ordnance systems to the AOIL are derived from switch or relay contacts. Up to 15 milliseconds of "switch bounce" can be anticipated on make and break. Unless otherwise noted, signal levels are defined as follows:

Logical "0" = open circuit-greater than 100 K.

Logical "1" = DPS ground - less than 10 ohms.

All input signals to the AOIL from the Armament/Ordnance Systems shall be switch or relay closures relative to DPS signal return (ground). These input signals shall originate in one of the following interconnection boxes:

(1) Search Store interconnection box

(2) Forward Armament interconnection box

(3) Aft Armament interconnection box

Each of these interconnection boxes shall provide an input connector to the AOIL. The DPS signal return shall not be used in the interconnection box or ARM/ORD system for any other purpose except to be fed back to the AOIL as a logical "1" via a switch or relay closure.

The DPS signal return shall not be used for any other purpose in the interconnection box or sent to any other ARM/ORD system equipments.

3.5.2.4.3.4.8.2 Momentary Switches - The only momentary switches with which the AOIL must interface are the Pilot's and Co- Pilot's Weapon Release Switches. These two switches are wired in parallel and only one line shall be sent to the AOIL. When either the Pilot or Co- Pilot depresses his Weapon Release switch, the Pilot'/Co-Pilot's Weapon Release switch signal line will go from a logical "O" to a logical "1". The AOIL shall generate an Enter to the computer only upon depression of either the Pilot' s/Co- Pilot's Weapon Release Switch.

3.5.2.4.3.4.8.3 Manually Operated Alternate Action Switches - The AOIL shall interface with the following manually operated alternate action switches:

(1) Search Power Switch

(2) Master Arm Switch

(3) Kill Store Manual Mode Switch

(4) Special Weapon Station Select (three signals)

(5) Torpedo Preset Station/Auto Select Switch

Each of these switches shall have a signal line to the AOIL; the Special Weapon Station Select switch has three signal lines. When the switch is operated a second time the line will go from a logical "1" to a logical "0". The AOIL shall generate an Enter to the computer upon either transition.

3.5.2.4.3.4.8.4 System Operated Alternate Action Switches - A system operated alternate action switch is one that is controlled by some action of the aircraft , such as a door opening, which activates a limit switch or a store (search or weapon) being released or loaded and activating a "Stores-in-Place" switch. This type of switch includes the following:

(1) Bomb Bay Door Switch

(2) Ten Wing Weapon Station Stores-in- Place Switches (Detection only on Release)

(3) Eight Bomb Bay Weapon Station Stores-in- Place Switches (Detection on Release)

(4) Three Pressurized Sonobuoy Launcher Door Switches

(5) Two SUS Away Switches

(6) Three Bomb Bay Rack Locked Switches

These switches have the same characteristics as the manually operated alternate action switches and again the AOIL shall generate an Enter to the computer upon either transition except as indicated above.

3.5.2.4.34.8.5 SLT Stores-in-Place Status - The Interrogate Monitor line is used to verify the stores inventory, i.e., that there is a Sore-in-Place where the computer program indicates there should be one. When the computer interrogates the Interrogate Monitor line to the AOIL, it appears as shown in Figure 90 (3.5.2.4. 5). When a Store has been selected and a store is in place, the Interrogate Monitor line will go to a logical "1"; when a Store has been selected but there is no Store in Place, the Interrogate Monitor line will go to a logical "O".

3.5.2.4.3.4.8.6 Aircraft Armament System Signals to Armament/Ordnance Input Logic (Kill Stores) (Summary) - "Input Signals" from the armament kill stores and controls to the DPS are listed below:

(1) Kill stores-in-Place Monitor - (18 signals) - Ground indicates Store is in place. Otherwise open circuit. There is no Store-in-Place signal for individual rockets or bullpup AGM-12/B.

(2) Bomb Bay Rack Unlock - (3 signals) - Ground when unlocked. Otherwise open circuit.

(3) Master Arm Monitor - Ground when master arm switch is on. Otherwise open circuit.

(4) Kill Stores Manual Mode Monitor - Ground when armament kill stores selection is in auto mode. Open circuit for manual mode.

(5) Manual Torpedo Preset Monitor - Open circuit when weapon station manually selected on torpedo preset panel. Ground for auto mode.

(6) Kill Store Release Command - Ground for weapon release. Otherwise open circuit.

(7) Bomb Bay Door Open Monitor - Open when bomb bay door closed or partially open. Ground circuit when bomb bay door fully open.

(8) Special Weapon Select Monitor - (3 signals) - Ground when weapon selected; otherwise open circuit.

3.5.2.4.3.4.8.7 Aircraft Armament Search Stores Signals to Armament/Ordnance Input Logic (Summary) - "Input Signals'' from the armament search stores and controls to the DPS are listed below:

(1) SUS Away Deep - Ground when SUS drop has started.

(2) SUS Away (Shallow) - Ground when SUS drop has started.

(3) Interrogate Monitor (1 signal) - Open circuit when store not in place. Ground when in place.

(4) Search Power Monitor - Ground when search power switch on pilot's armament panel is in "on" position. Otherwise, open circuit.

(5) Pressurized Door Monitor - (3 signals) - Ground when door open. Open circuit when door closed or not fully open.

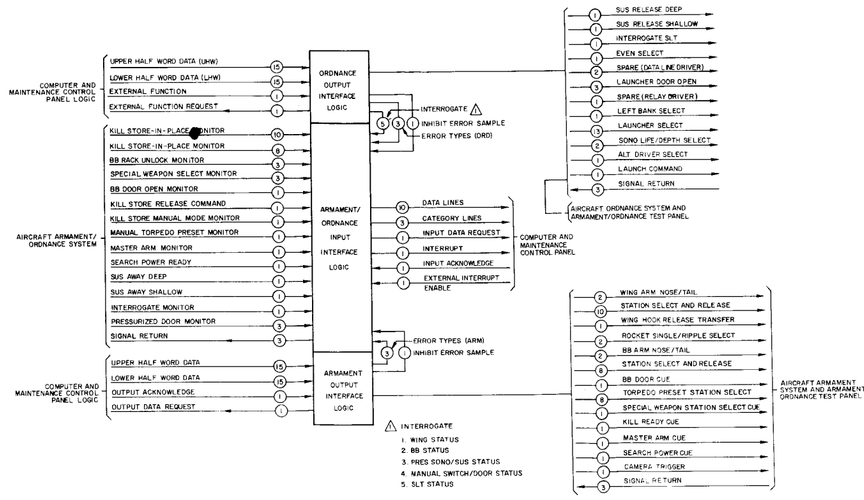


Figure 67. Armament/Ordnance Input Logic, Armament Output Logic and Ordnance Output Logic, Pictorial Flow Diagram.

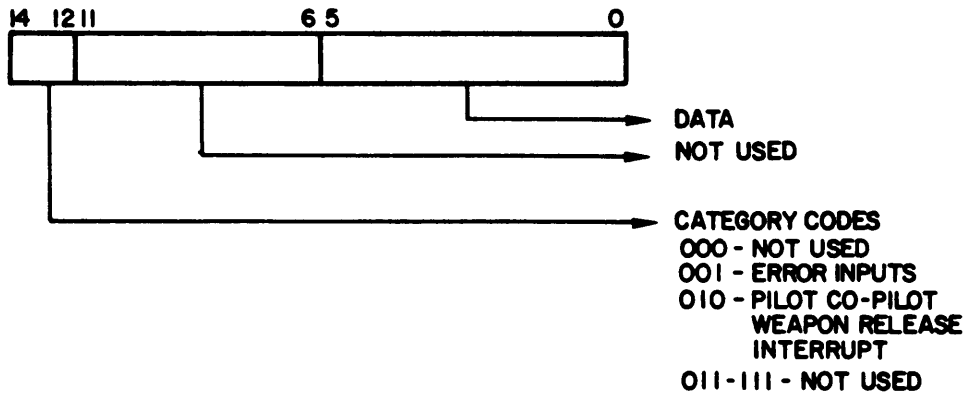


Figure 68. Armament/Ordnance Computer Input Word Format (Interrupt Inputs)

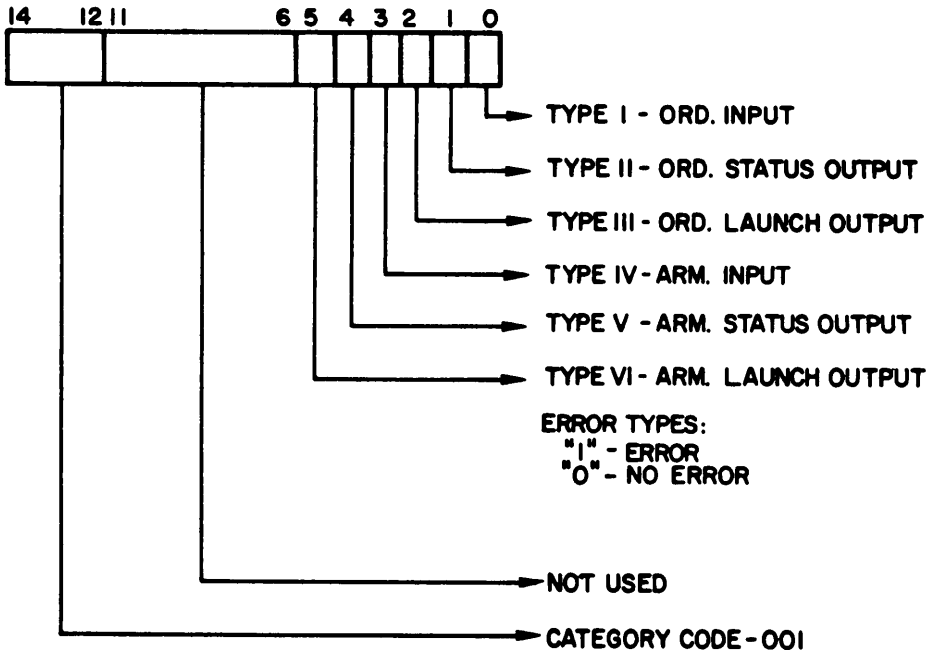


Figure 69. Armament/Ordnance Computer Input Formats (Error Interrupts)

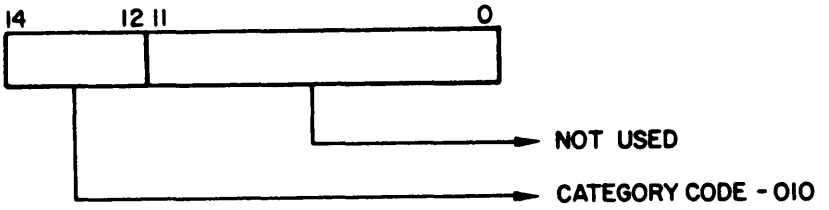


Figure 70. Armament/Ordnance Computer Input Word Format (Pilot/Co-Pilot Weapon Release Interrupt)

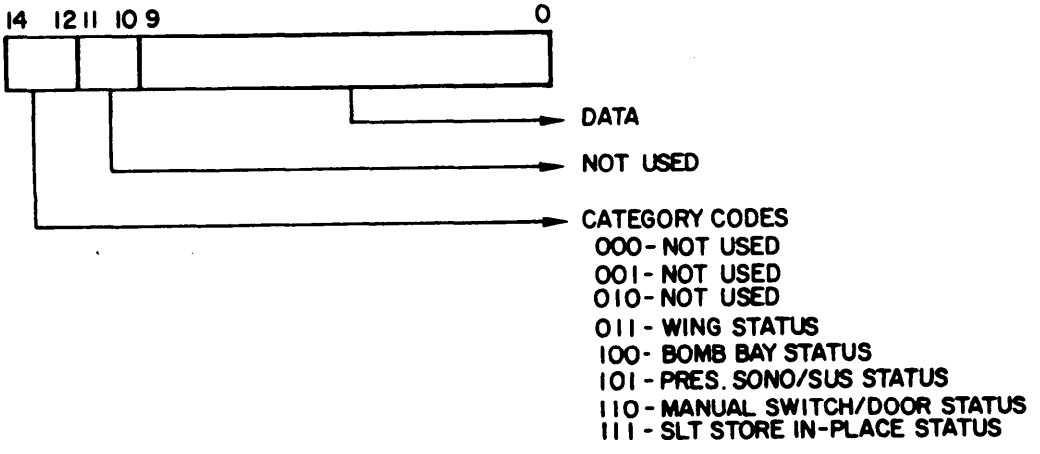


Figure 71. Armament/Ordnace Computer Input Word Format (Normal Inputs)

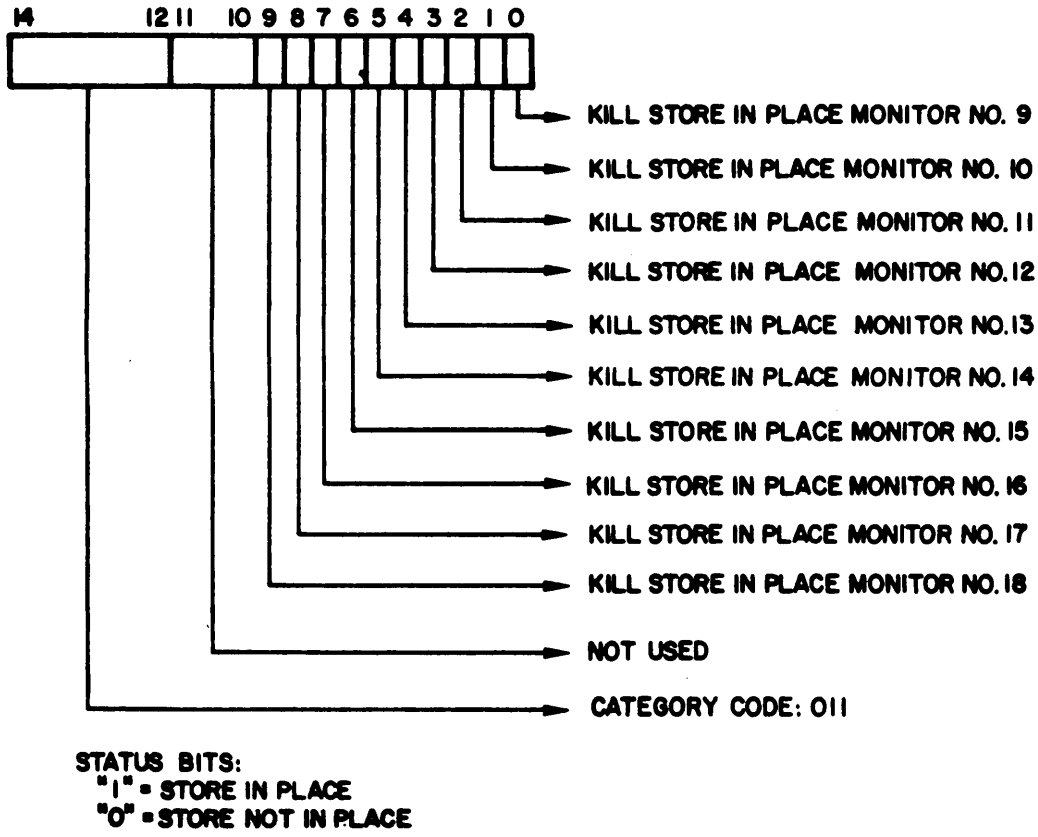


Figure 72. Armament/Ordance Computer Input Word Format (Wing Statue)

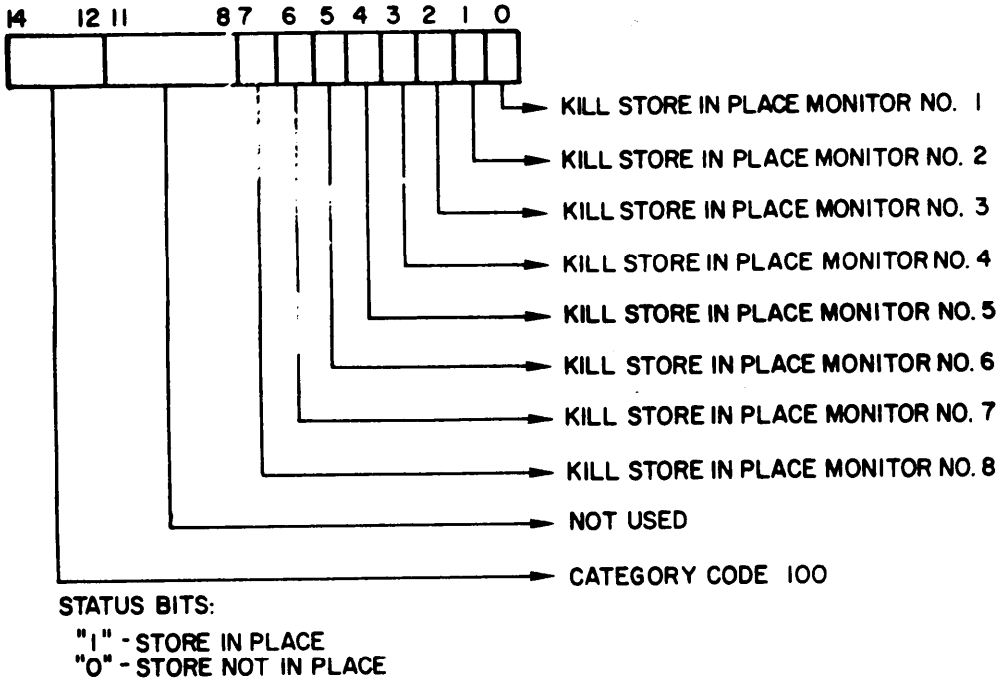


Figure 73. Armament/Ordnance Computer Input Word Format (Bomb Bay Status)

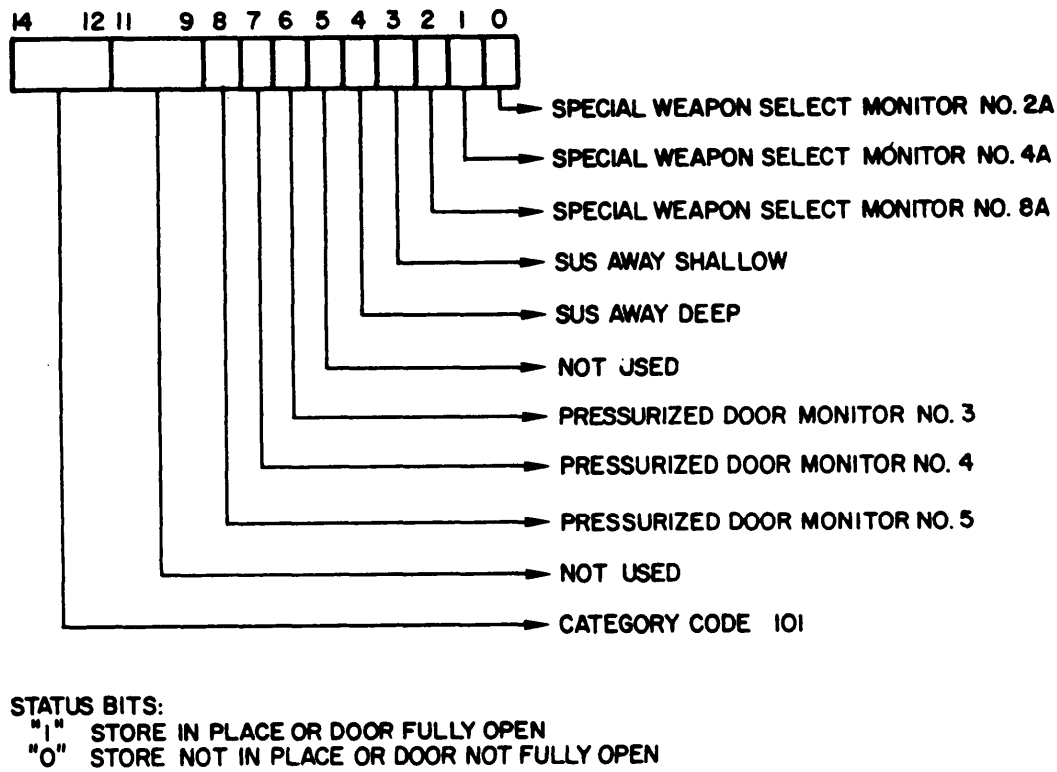


Figure 74. Armament/Ordnance Computer Input Word Format (Pres. Sono/SUS Station/Special Weapon Select)

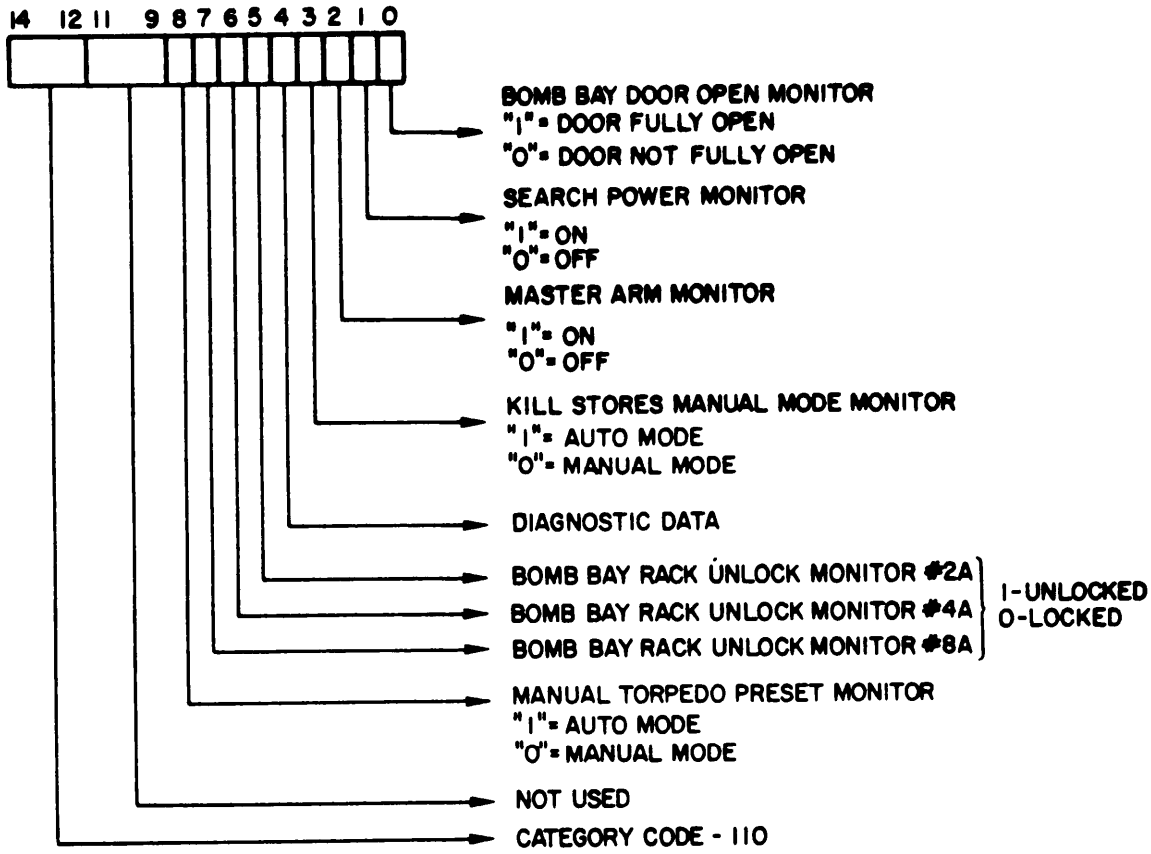


Figure 75. Armament/Ordnance Computer Input Word Format (Manual Switch/Door Status/Rack Locked)

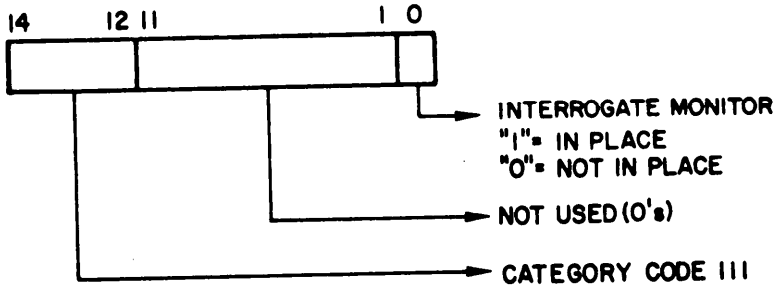


Figure 76. Armament/Ordnance Computer Input Word Format (SLT Store in Place)

3.5.2.4.4 Armament Output Logic

3.5.2.4.4.1 Functional Description - The Armament Output Logic (AOL) is the interface between the computer and the Aircraft Armament System. The AOL shall receive and decode commands from the computer and transmit commands to the Aircraft Armament System. The AOL shall allow the computer to control the arming, rocket selection, and selection and launching of the weapon stations.

Figure 67 is a Functional Flow Diagram of the AOL. Figure 77 is a timing diagram.

3.5.2.4.4.2 General Description - The AOL shall perform the following functions:

(1) Upon computer command: arm nose, arm tail, arm nose and tall, or disarm for either wing or bomb bay weapon stations independently.

(2) Upon computer command select rocket ripple, rocket single, or hook transfer controls.

(3) Upon computer command select one of 18 weapon stations for either weapon release or rocket launch.

(4) Detect and transmit to the AOIL the following errors:

(a) Input word structure is improper (i.e. , upper and lower half words not identical or bits in the Ordnance Category Field and the Armament Category Field simultaneously).

(b) Redundant status logic not in agreement.

(c) Redundant launch logic not in agreement.

(5) Camera trigger signal supplied simultaneously with the weapon release signal.

(6) Provides the necessary cueing signals.

(7) Torpedo preset weapon station select.

3.5.2.4.4.3 Operating Retirements

3.5.2.4.4.3.1 General - Because of the critical nature of the Armament System precautions shall be taken to guard against erroneous operation.

(1) The computer shall transmit a 30-bit command to the AOL utilizing the Output Acknowledge with the constraint that bits 0 - 14 must be identical to bits 15-29.

(2) Bits 12-14 and 27-29 shall be used for Armament and/or IFPM Category codes and bits 8-,11 and 23 - 26 shall be used for Ordnance and/or IFPM Category codes. The Armament Category field and the Ordnance Category field shall not contain bits simultaneously.

(3) The Armament Category codes shall be minimum distance 2 codes except that the remaining codes may be used for test modes.

(4) The AOL shall be comprised of redundant logic sections, each operating on one half of the computer output word. No action shall be performed unless both logic sections agree. In addition, no single error, either logic malfunction or comuter error (i.e. . one bit) shall cause an erroneous launch operation.

(5) The AOL shall terminate all normal Launch Commands after 130 ±10% milliseconds and all Rocket Launch Commands after 640 ±10% milliseconds.

(6) The AOL shall not accept a command from the computer (i. e. , the AOL shall not raise the Output Data Request) during the period the AOL is exercising a Launch Command or within 130 ±10% milliseconds after receipt of a Rocket Select or Arm Command.

(7) The AOL shall be self-initializing after any power interruption, (i. e. , the AOL shall insure that no output command shall be high for more than one millisecond due to the random setting of flip-flops caused by the power interruption).

(8) Removal of the AOL subunit shall cause the Aircraft Armament system to revert to a reset state (i.e. , all Weapon Stations disarmed, Rocket Clear, and no Launch Commands).

(9) The AOL shall detect and transmit to the AOIL the errors described in 3.5.2.4.4.2 (4).

3.5.2.4.4.4 Interface Requirements

3.5.2.4.4.4.1 Word Formats - The AOL Word Formats are shown in Figures through 82.

3.5.2.4.4.4.2 Signal Characteristics - Unless otherwise noted, signal levels external to Logic Unit 2 are defined as follows:

Logical “0” = +4 ±1 volts

Logical “1” = 0.0 +0.5 -0. 0 volts

3.5.2.4.4.4.3 Maintenance Control Panel Subunit to Armament Output Logic - Communications between the computer and the AOL shall be via the MC PL and in accordance with Appendix I and 3.5.2.4.6. The MCPL shall provide the input amplifiers for Output Acknowledge and data bits 0 hrough 29. “Data” shall be available to the AOL.

3.5.2.4.4.4.4 Armament Output Logic to Maintenance Control Panel Subunit - The AOL shall provide the MCPL the input control and data lines for monitoring.

3.5.2.4.4.4.5 Armament Output Logic to Armament/Ordnance Input Logic

3.5.2.4.4.5.1 Error Signals - The AOL shall be capable of detecting and transmitting to the AOIL the three types of errors indicated in 3.5.2.4.4.2(4). In addition, an inhibit signal shall be transferred from the AOL to the AOIL. The inhibit signal shall be a logical “1” during the time the Output Data Request is a logical “O” (see 3.5.2 .4.4.3.1 (6)).

The Type IV error signal (indicating an input word structure is improper -- see 3. 5.2.4.4.2 (4) (a)) shall be a logical “1” for 0.5 microsecond (minimum): the trailing edge of this pulse shall occur during the time the inhibit signal is a logical “1”. Therefore, data comparison for a Type IV error shall be done during the time the Output Acknowledge is a logical “1”.

The Type V error signal (indicating the redundant status logic is not in agreement (see 3. 5.2.4.4.2 (4) (b)) shall be a logical “l” for an indefinite length of time. Data comparison of the Armament Status registers shall be done continuously and the Type V error signal shall be transmitted to the AOIL any time the registers do not agree.

The Type VI error signal (indicating the redundant launch logic is not in agreement (see 3.5.2 .4.4.2 (4) (c)) shall be a logical “1” for a maximum of 640 ±10% milliseconds, and shall occur during the time the inhibit signal is a logical “l”. Data comparison of the Armament Launch Register shall be done during the time the registers are active.

3.5.2.4.4.4.6 Armament Output Logic to Aircraft Armament System

3.5.2.4.4.4.6.1 Signal Characteristics - Unless otherwise noted, all output drivers shall interface with a circuit in the Aircraft Armament System similar to that shown in Figure 83. In this case a logical "l" shall be 0 + 1.5 -0.0 volts and a logical "0" shall be 12 ±1 volts.

All output signals from the AOL to the Armament/Ordnance systems shall be relay drivers capable of driving a diode damped inductive load of not more than 250 ma. The output signals shall originate in the DPS and terminate in one of the following interconnection boxes:

(1) Search Store Interconnection Box.

(2) Forward Armament Interconnection Box.

(3) Aft Armament Interconnection Box.

Each of these interconnection boxes shall Provide an Output connector to the DPS. The DPS Armament/Ordnance Test Panel shall provide the positive voltage to operate the isolation relays in the three interconnection boxes. This voltage shall be used only for the relays to which the DPS interfaces. The relays shall be activated when the two series drivers in the DPS are turned on to provide a return path for the DPS positive power supply through the isolation relay in the interconnection box, to the DPS ground. By this means the DPS can remain isolated from the ARM/ORD ground and aircraft 28 VDC transient conditions.

3.5.2.4.4.4.6.2 Weapon Select and Launch Commands - The AOL shall, upon computer command, select and launch a weapon from one of 18 weapon stations. The selection and launch are accomplished simultaneously by selecting one of 18 lines. The output signal (logical "1") for a normal launch command (i.e. , Rockets Single or Ripple have not previously been selected) shall be 130 milliseconds ±10% in duration. If Rockets Single or Rockets Ripple have previously been selected, the launch command (in this case Rocket Launch) shall be 640 milliseconds ±10% in duration.

3.5.2.4.4.4.6.3 Armament Auxiliary Functions

3.5.2.4.4.4.6.3.1 Arm Commands - Arm commands shall be transmitted via four signals from the AOL to the Aircraft Armament System. These signals, Arm Nose (Bomb Bay), Arm Tail (Bomb Bay), Arm Nose (Wing) and Arm Tail (Wing), shall be a logical "l" as long as the specified function is to be active. Two signals arm the wing stations (nose and tail) and the other two signals arm the bomb bay stations (nose and tail).

3.5.2.4.4.4.6.3.2 Rocket/Mines/Torpedoes Commands - Three commands will be transmitted via three signals from the AOL to the Aircraft Armament System. These are the Wing Hook Release Transfer, Rocket Single/Rocket Ripple Select command. If Mines or Torpedoes, which are connected to the Aircraft Weapon Station Hook, are to be released, a Wing Hook Release Transfer signal is required (logical "1" level), as well as a Release/Station Select and Release signal. If a Rocket Pod is mounted on the Hook, the Wing Hook Release Transfer signal must be logical "O". To release a Single Rocket, a logical "1" is required on the Rocket Single Select line. To activate the Rocket Ripple function requires a logical "1" on the Rocket Ripple Select Line.

3.5.2.4.4.4.6.4 Armament Output Logic to Armament System (Kill Stores) Sognals (Summary) - "Output Signals" from the DPS to the armament kill stores and controls are listed below. Each relay driver-in the DPS must be able to furnish a ground for a 250 milliampere 12 volt load.

(1) Station select and Release (Fire) -18 relays (one for each station). Each line furnishes a ground for one of 18 relays. Function used for both dropping stores and firing rockets. Must follow items (2), (4), (5), (6), (7), (8) and (13) by at least 130 milliseconds ±10%. Must follow item (12) by at least 3 seconds. (Note 3 seconds is a program function.)

(2) Wing Hook Release Transfer - (1 relay)

When active, this function transfers power to release hooks for dropping store (mines, bombs, torpedoes, etc.). Function remains inactive when firing rocket single or rocket ripple.

(3) Camera Trigger - (1 relay)

Function active simultaneous with release of any Kill Store.

(4) Rocket Ripple Select - (1 relay)

When function is active, all rockets in the launching pod at the selected station will fire.

(5) Wing Arm Nose - (1 relay)

Function arms nose of any store released from a wing station (not bomb bay).

(6) Wing Arm Tail - (1 relay)

Function arms tail of any store released from bomb bay (not (not bomb bay).

(7) Bomb Bay Arm Nose - (1 relay)

Function arms nose of any store released from bomb bay (not wing).

(8) Bomb Bay Arm Tail - (1 relay)

Function arms tail of any store released from bomb bay (not wing) .

(9) Master Arm Cue - (1 relay)

Function illuminates an indicator lamp on the pilot's armament panel. (Indicator lamp requests pilot to move master arm switch to other position to supply or remove armament power).

(10) Bomb Bay Door Cue - (1 relay)

Function illuminates an indicator lamp on the pilot's armament panel. (Indicator lamp requests pilot to move bomb bay door switch to other position to open or close bomb bay doors).

(11) Kill Ready Cue - (1 relay)

Function illuminates an indicator lamp on the pilot's armament panel. (This cue tells the pilot that all preparations for dropping a kill store have been completed and store may be released.)

(12) Torpedo Preset Station Select - (8 relays)

When Sation Select switch on torpedo preset panel is set to "auto" this function connects the torpedo preset panel with the torpedo that the computer has selected to drop. the torpedo will then be set to the depth and mode as set on the torpedo preset panel.

(13) Rocket Single Select - (1 relay)

Function switches power to rocket firing bus.

(14) Special Weapon Sation Select Cue - (1 relay)

Function illuminates an indicator lamp on pilot's armament panel. (Indicator lamp requests pilot to select special weapon station.)

(15) Search Power Cue - (1 relay)

Lights an indicator lamp on pilot's armament panel. This lamp requests pilot to put Ssarch Power switch in other position.

S.5.2.4.4.4.7 Armament Output Logic to Armament/Ordnance Test Panel - Each output line from the AOL to the Aircraft Armament System shall also be transmitted to an externally located Armament/Ordnance Test Panel. This Test Panel shall contain one indicator lamp for each function except cue signals and shall be arranged such that when the function is active the indicator lamp is illuminated. The Test Panel is discussed in detail in 3.5.2 .4.4.5 and 3.5.5.

3.5.2.4.4.5 Armament/Ordnance Test Panel

3.5.2.4.4.5.1 Functional Description - The Armament/Ordnance Test Panel shall provide an operator with a means of monitoring the performance of the AOL and OOL. The test Panel shall be used during System Test and Integration Tests to verify the operation of the control logics. Indicator lamps shall be provided for each output function of both logics except cue signals.

3.5.2.4.4.5.2 General Description - The Armament/Ordnance Test Panel shall perform the following functions:

(1) Display the results of each output function of the AOL, such that the indicator shall be illuminated when the function is active exclusive of cues.

(2) Display the result of each output function of the OOL, such that the indicator shall be illuminated when the function is active.

3.5.2.4.4.5.3 Interface Requirements

3.5.2.4.4.5.3.1 General - The Armament/Ordnance Test Panel shall provide one indicator light for each output (to the aircraft systems) of the AOL and OOL except cue signals. A power switch (not shown in the diagram) shall be provided to disable all indicator lamps such that when the Power switch is off, no power will be drawn from the input lines to the lamps. In addition, a lamp test circuit (not shown in diagram) shall be provided to test the indicator lamps in such a manner that no interaction shall occur between input signals when the lamp test is used.

The Armament/Ordnance Test Panel shall provide the +12.0 volt power to operate the ARM/ORD isolation relays in the three ARM/ORD interconnection boxes. This power shall not be switched from the front of the test panel and shall remain active as long as input power is applied from the aircraft power distribution system.

The Armament/Ordnance Test Panel shall serve as a junction box and distribute the signals to the Aft-Interconnection Box and the Search Stores Interconnection Box. The outputs of the AOL to the FWD-Interconnection Box shall be wired directly from Logic Unit 2 and not the Armament/Ordnance Test Panel. All inputs from the three ARM/ORD Interconnection Boxes shall be wired directly to Logic Unit 2.

3.5.2.4.4.5.3.2 Input Singals - Input signals from the Armament and Ordnance Output logics shall be the same signals which are transmitted to the aircraft system.

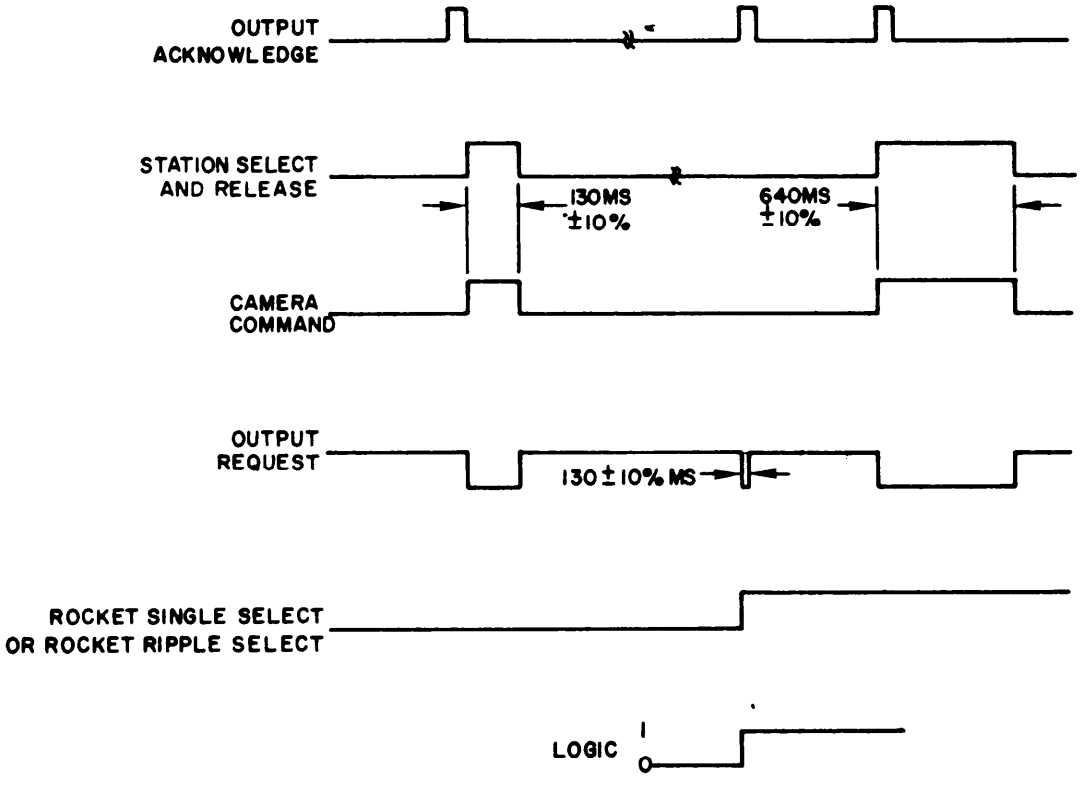


Figure 77. Armament Output Logic Timing Diagram

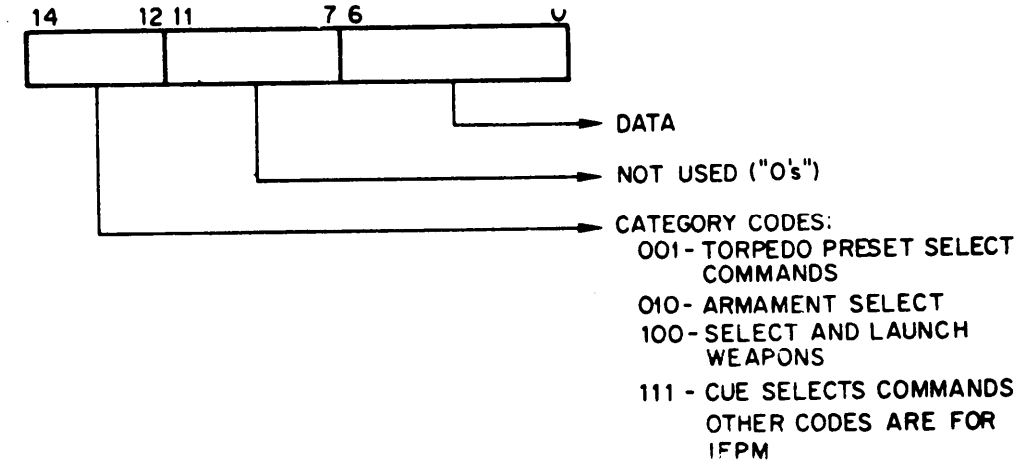


Figure 78. Format for Armament Output Logic Normal Armament Output Command Word

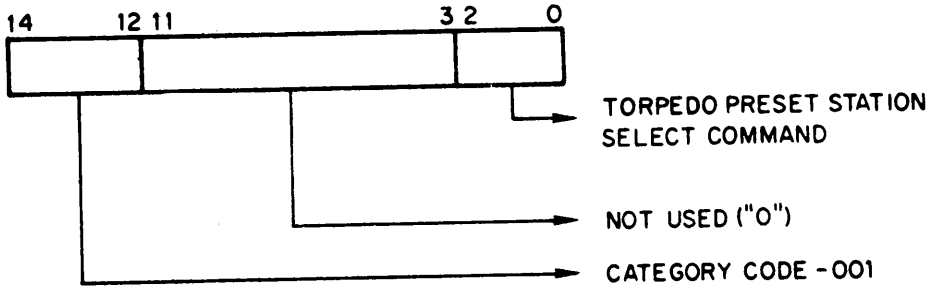


Figure 79. Format for Armament Output Logic Torpedo Preset Select CMDS Word

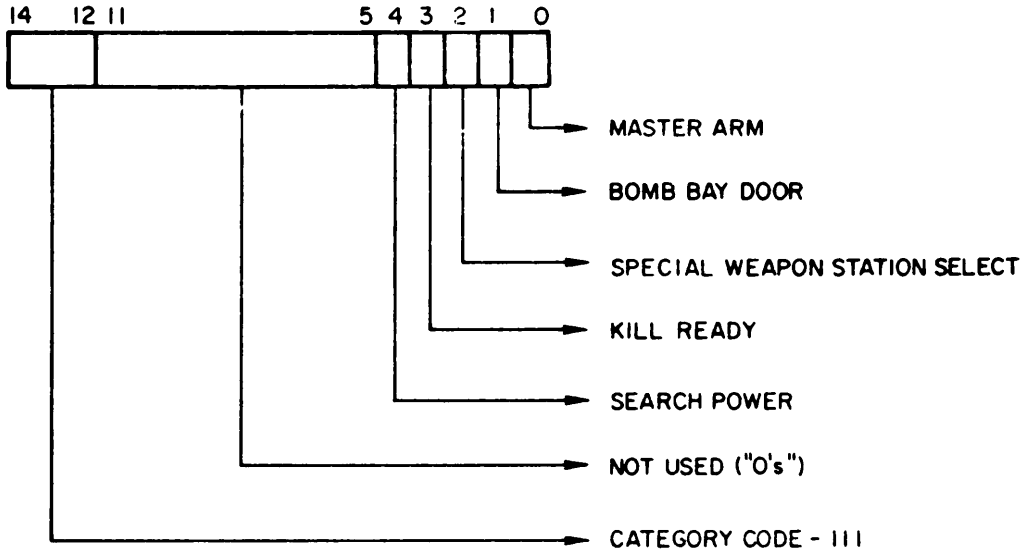


Figure 80. Format for Armament Output Logic Cue Select CMDS Word

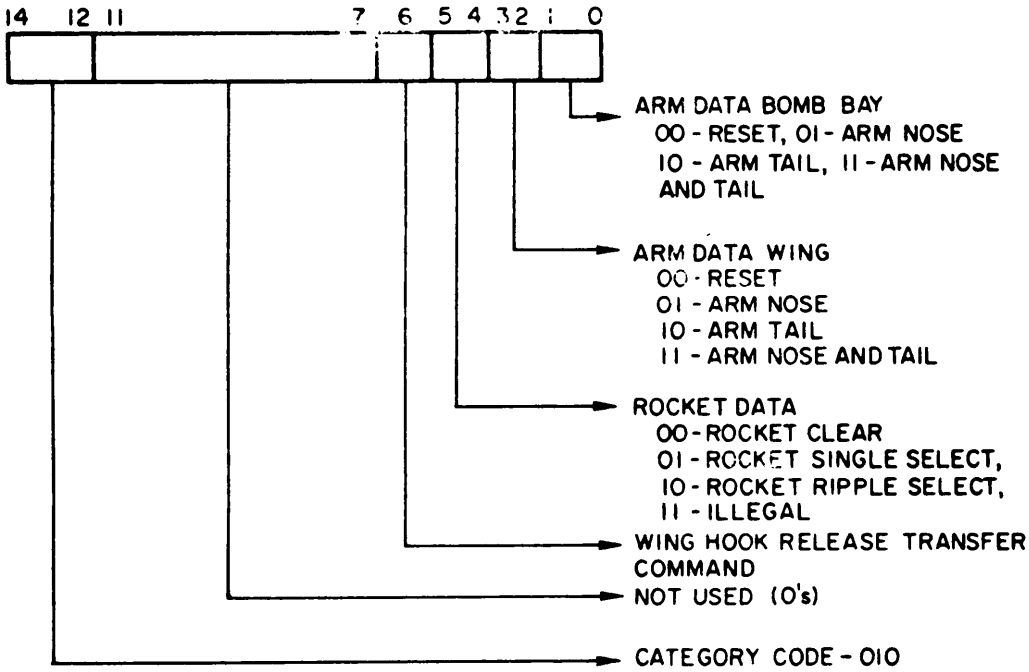


Figure 81. Format for Armament Output Logic Armament Select Commands

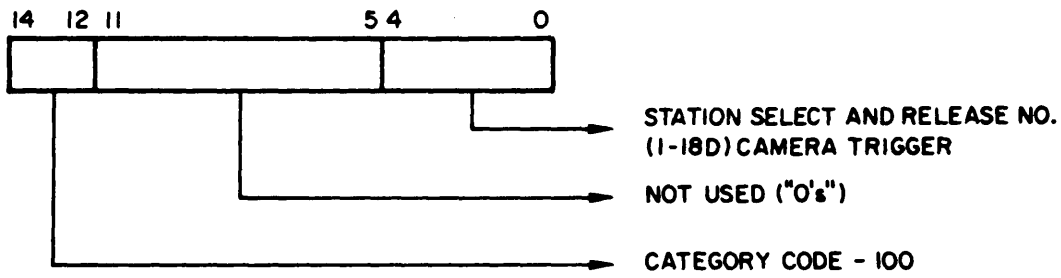


Figure 82. Format for Armament Output Logic Select and Launch Weapon and Camera Trigger Command Word

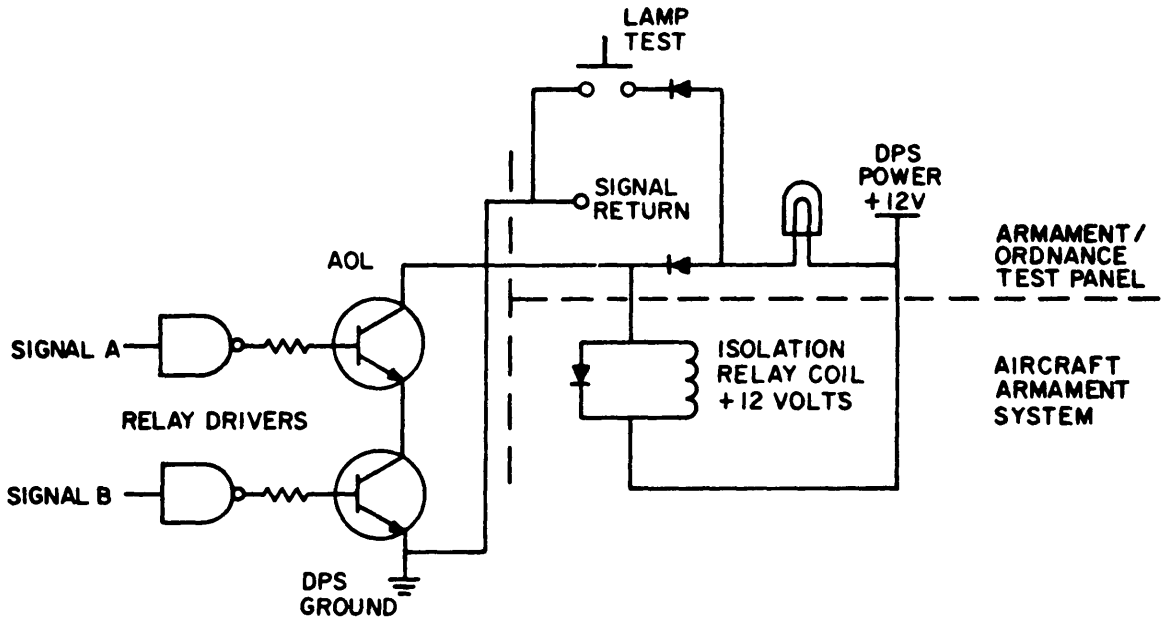


Figure 83. Armament Output Logic/Armament Ordnance Test Panel/Aircraft Armament System Interface

3.5.2.4.5 Ordnance Output Logic

3.5.2.4.5.1 Functional Description - The Ordnance Output Logic (OOL) is the interface between the computer and the Aircraft Ordnance System. The OOL shall receive and decode commands from the computer and transmit commands to the Aircraft Ordnance System. The OOL shall allow the computer to select and launch sonobuoys from either the non-pressurized or the three pressurized launchers, select and launch SUS, select sonobuoy depth and life, control the pressurized launcher doors, and interrogate the SLT Status, the SUS Away Status and the Wing and Bomb Bay Weapon Station Status via the AOIL.

Figure 67 is a Functional Flow Diagram for the Ordnance Output Logic .

3.5.2.4.5.2 General Description - The OOL shall perform the following functions:

(1) Upon computer command interrogate the AOIL for up to five status words.

(2) Upon computer command select and launch SUS Shallow, SUS Deep, or SUS Shallow and Deep.

(3) Upon computer command selectively open and close the three pressurized doors.

(4) Upon computer command select Sonobuoy Hydrophore Depth (shallow or deep).

(5) Upon computer command select Sonobuoy Life (long or short).

(6) Upon computer command interrogate the SLT to verify Stores-in-Place.

(7) Upon computer command select and launch from one of three pyrotechnic pressurized sonobuoy launchers.

(8) Upon computer command select and launch from one of 48 pyrotechnic, non- pressurized sonobuoy launchers.

(9) Detect and transmit to the AOIL the following errors:

(a) Input word structure is improper (i. e., upper and lower half words not identical or bits in the Ordnance Category Field and the Armament Category Field simultaneously).

(b) Redundant status logic not in agreement.

(c) Redundant launch logic not in agreement.

3.5.2.4.5.3 Operating Requirements - Because of the critical nature of the Ordnance system, precautions shall be taken to guard against erroneous launch operation.

(1) The computer shall transmit a 30-bit command to the OOL utilizing the External Function with the constraint that bits 0-14 must be identical to bits 15-29.

(2) Bits 12-14, and 27-29 shall be used for Armament and/or IFPM Category codes and bits 8-11 and 23-26 shall be used for Ordnance and/or IFPM Category codes. The Armament Category field and the Ordnance Category field shall not contain bits simultaneously.

(3) The Ordnance Category codes shall be minimum distance 2 except for codes used for test modes.

(4) The OOL shall be comprised of redundant logic sections each operating on one-half of the computer output word. No launch action shall be performed unless both logic sections agree. In addition. no single error, either logic malfunction or computer error (i. e. , one bit), shall cause an erroneous launch operation.

(5) The OOL shall terminate SUS Launch Commands after 130 ±10% milliseconds and SLT Select and Launch Commands after 260 ±10% milliseconds.

(6) The OOL shall not accept a command from the computer (i. e., the OOL shall not raise the External Function Request) during the period the OOL is exercising a Launch Command or within 130 ±10% milliseconds after receipt of a Select Command (door, buoy life or depth, or SLT select), or within 1 microsecond through 1 millisecond after receipt of an AOIL Interrogate Command.

(7) The OOL shall be self-initializing after any power interruption (i. e. , the OOL shall insure that no output command shall be high for more than 1 millisecond due to the random setting of flip-flops caused by the power interruption).

(8) Removal of the OOL subunit shall cause the Aircraft Ordnance System to revert to a reset state (i. e. , no SUS selected, all doors closed, and no Launch Commands).

(9) The OOL shall detect and transmit to the AOIL the errors described in 3.5.2.4.5.2 (9).

3.5.2.4.5.4 Interface Requirements

3.5.2.4.5.4.1 Word Formats - The OOL Word Formats are shown in Figures 84 through 88.

3.5.2.4.5.4.2 Signal Characteristics - Unless otherwise noted, signal levels external to Logic Unit 2 are defined as follows:

Logical “0” = +4 ±1 volts

Logical “1” = 0.0 +0.5 -0.0 volts

3.5.2.4.5.4.3 Maintenance Control Panel Subunit to Ordnance Output Logic - Communications between the computer and the OOL shall be via the MCPL and in accordance with Appendix I and 3.5,2.4.6. The MCPL shall provide the input amplifiers for External Function and data bits O through 29. Data shall be available to the OOL. Input amplifiers are specified in Appendix II.

3.5.2.4.5.4.4 Ordnance Output Logic to Maintenance Control Panel Subunit - The OOL shall provide to the MCPL the input control and data lines for monitoring.

3.5.2.4.5.4.5 Ordnance Output Logic to Armament/Ordnance Input Logic

3.5.2.4.5.4.5.1 Error Signals - The OOL shall be capable of detecting and transmitting to the AOIL the three types of errors indicated in 3. 5.2.4.5.2 (9). In addition, an inhibit signal shall be transferred from the OOL to the AOIL. The inhibit signal shall be a logical “1” during the time the External Function Request is a logical “0”. (See 3. 5.2.4.5.3 (6).)

The Type I error signal (indicating an input word structure is improper (see 3. 5.2.4.5.2 (9) (a)) shall be a logical “1” for O. 5 microseconds (min.): the trailing edge of this pulse shall occur during the time the inhibit signal is a logical “1”. Therefore, data comparison for a Type I error shall be done during the time the External Function is a logical “l”.

The Type II error signal (indicating the redundant status logic is not in agreement (see 3. 5.2.4.5.2 (9) (b)) shall be a logical “1” for an indefinite length of time. Data comparison of the Ordnance-Status registers shall be done continuously and the Type II error signal shall be transmitted to the AOIL any time the registers do not agree.

The Type III error signal (indicating the redundant launch logic is not in agreement (see 3.5.2 .4.5.2 (9) (c)) shall be a logical "l" for a maximum of 260 ±10% milliseconds, and shall occur during the time the inhibit signal is a logical "1". Data comparison of the Ordnance Launch Register shall be done during the time the Registers are active. Following an SLT Status Command, the Type III error signal may be a logical "1" for an indefinite period of time.

3.5.2.4.5.4.5.2 Interrogate signals - The computer may request that the AOIL enter one or more (up to five) status words. The computer requests the interrogation of these words (Wing status, Bomb Bay Status, Pressurized Sono/SUS Status, Manual Switch/Door Status, and SLT Status) by transmitting an Interrogate Command (see Figure 84) to the OOL. The OOL shall decode the computer command and transmit 0.5 microsecond (min.) logical "1" interrogate signal to the AOIL.

The SLT Status Interrogate Command shall terminate the SLT interrogate sequence as described in 3.5.2.4.5.4.6.2.2.

3.5.2.4.5.4.6 Ordnance Output Logic to Aircraft Ordnance System

3.5.2.4.5.4.6.1 Signal Characteristics - Unless otherwise noted all output drivers shall interface with a circuit in the Aircraft Ordnance System similar to that shown in Figure 89. In this case a logical "l" is O +1.5 -0.0 volts and a logical "O" is 12 l 1 volts.

All output signals from the OOL to the Armament/Ordnance Systems shall be relay drivers capable of driving a diode damped inductive load of not more than 250 ma. The output signals shall originate in the DPS and terminate in one of the following interconnection boxes:

(1) Search Store interconnection box

(2) Forward Armament interconnection box

(3) Aft Armament interconnection box

Each of these interconnection boxes shall provide an output connector to the DPS. The DPS Armament Ordnance Test Panel shall provide the positive voltage to operate the isolation relays in the three interconnection boxes. This voltage shall be used only for the relays to which the DPS interfaces. The relays shall be activated when the two series drivers in the DPS are turned on to provide a return path for the DPS positive power supply through the isolation relay in the interconnection box, to the DPS ground. By this means the DPS can remain isolated from the ARM/ORD ground and aircraft +28 VDC transient conditions.

3.5.2.4.5.4.6.2 Sonobuoy Launchers

3.5.2.4.5.4.6.2.1 Select and Launch Commands - The OOL shall, upon computer command, select and launch one of 51 sonobuoys from the cartridge ejected sonobuoy launcher system.

The selection of a particular launcher in the SLT is accomplished by relays. Once a launcher is selected, the launching is accomplished by a Silicon Controlled Rectifier (SCR). Figures 90, 91 and 92 show timing and wiring diagrams for the SLT select and launch functions.

The Launcher System is divided into two groups of 27 and 24 launchers designated Bank I and Bank II. Each Bank contains 13 four-pole relays. One pole from each relay is common to one SCR. Both Banks share the same two SCR's. Each relay controls two launchers, but one SCR selects only one of the two. In actual operation the SCR, Bank, and Relay select functions are as shown in Figures 90 and 91. The SCR select shall be delayed 130 milliseconds ±10% to provide for relay stabilization prior to the actual launch command.

By use of alternate selection lines (for Bank and Even/Odd selection) all critical paths are redundant. This reduces the number of buoys unavailable for launch to 4 out of 5, assuming a single driver failure.

The alternate driver select line controls a relay which simply reverses the outputs of the Bank select final drivers. This is reflected in the alternate coding shown in the OOL word formats.

The output signals to provide these functions are:

(1) One Launcher Command

(2) One Left Bank select signal

(3) One alternate Driver select signal

(4) Thirteen Relay select signals

(5) One Even select signal

(6) One Interrogate SLT signal (to be explained in 3.5.2.4.5.4.6.2.2).

(7) Spares 1, 2 and 3

All output lines (except spares 2 and 3) shall have the characteristics of 3.5.2.4.5.4.6.1. All select commands shall be 260 ±10% milliseconds in duration except as noted in Figure 91.

Spare 2 and 3 lines shall be driven by standard data line drivers. The Launch Command Signal from the OOL shall have the same timing as the spare 2 and 3 lines, but shall be driven by a standard relay driver. All signals shall be triggered as shown in Figure 91.'

3.5.2.4.5.4.6.2.2 Interrogate - An interrogation mode shall be provided to allow computer confirmation of pre-flight loading information and check out of the relay selection logic prior to and after a buoy launch command. The computer shall be able to verify the presence of a buoy by transmitting a word which is identical to the launch command with the exception of two category codes. A Schmitt Trigger in the aircraft ordnance system shall detect the presence or absence of the 0.1 ohm cartridge load. The equivalent circuit for the interrogate mode is shown in Figure 92.

For SLT interrogation mode, two computer commands are required. The first command establishes the relay selection matrix with a category code octal 04 to the OOL. The relay matrix remains in the selected condition until the computer issues an SLT interrogate command category code octal 01 to the AOIL via the OOL. The relay matrix is not reset until the completion of the AOIL interrogation command, or transmission of an SLT Launch Command. The two redundant SCR select lines shall not be actuated for the interrogate mode.

3.5.2.4.5.4.6.2.3 Ordnance Select - Sono Depth and Sono Life shall be transmitted via signals to the Aircraft Ordnance System. Decoding will be done in the aircraft system. These signals shall be a logical "1" as long as the specified function is to be active. These functions will be selected prior to launching a sonobuoy. The OOL shall consider these functions to be status type functions (i. e. , the OOL shall store this information until the computer outputs revised data.)

3.5.2.4.5.4.6.2.4 Door Commands - The OOL shall, upon computer command, open or close any of the three pressurized sonobuoy launcher doors. The door opening signals shall be a logical "l" as long as the specified function is to be active. The OOL shall consider these functions to be status type functions and therefore to be stored until the computer outputs revised data.

3.5.2.4.5.4.6.3 SUS Launchers

3.5.2.4.5.4.6.3.1 Selection - The OOL shall upon computer command select and launch either SUS Deep or SUS Shallow. The output signals shall be a logical "1" for 130 milliseconds ±10%

3.5.2.4.5.4.6.3.2 Launch Commands - The OOL shall upon computer command launch the selected SUS(s). The SUS launch commands (see Figure 87) shall be a 130 ±10% milliseconds pulse.

3.5.2.4.5.4.7 Ordnance Output Logic to Aircraft Ordnance System - Search Stores Signals (Summary) - Output Signals" from the DPS to the armament search stores and controls are listed below. Each relay driver in the DPS must be able to furnish a ground for a 250 milliampere relay coil 12 volts.

(1) Launcher Select - (13 relays)

Function actuates one of 13 relays. One of the four poles on the selected relay is furnished firing power through SCR driver select and relay bank select functions.

(2) Spares 2 and 3

(3) Launch Command- (l relay)

Function initiates launch action

(4) Left Bank Select - (1 relay)

Relayed, function supplies firing power for one bank of sonobuoys. Active, function supplies firing power for the other bank.

(5) Spare 1 - (1 relay)

(6) Interrogate SLT - (1 relay)

Function activated for sonobuoy- in-place interrogation.

(7) SUS Release Deep (1 relay)

Actuate deep SUS release relay.

(8) SUS Release Shallow (1 relay)

Actuate shallow SUS release relay.

(9) Sonobuoy Life Select (1 relay)

When function is active, sonobuoy is set at long life; otherwise, sonobuoy will remain set to short life.

(10) Sonobuoy Depth Select (1 relay)

When function is active, sonobuoy depth is set to shallow upon being launched. Otherwise, sonobuoy will remain set to deep.

(11) Launcher Door Open Command (3 relays)

Function opens selected pressurized sonobuoy chute door.

(12) Alternate Driver Select (1 relay)

Function reverses action of Bank Select Relay.

(13) Even Select (1 relay)

Inactive, function selects odd chutes. Active, function selects even chutes.

3.5.2.4.5.4.8 Ordnance Output Logic to Armament/Ordnance Test Panel - Each output line from the OOL to the Aircraft Ordnance system shall also be transmitted to an externally located Armament/Ordnance Test Panel. This Test Panel shall contain one indicator lamp for each function and shall be arranged such that when the function is active the indicator lamp is illuminated. The Armament/Ordnance Test Panel is discussed in detail in 3.5.2.4.4.5 and 3.5.5.

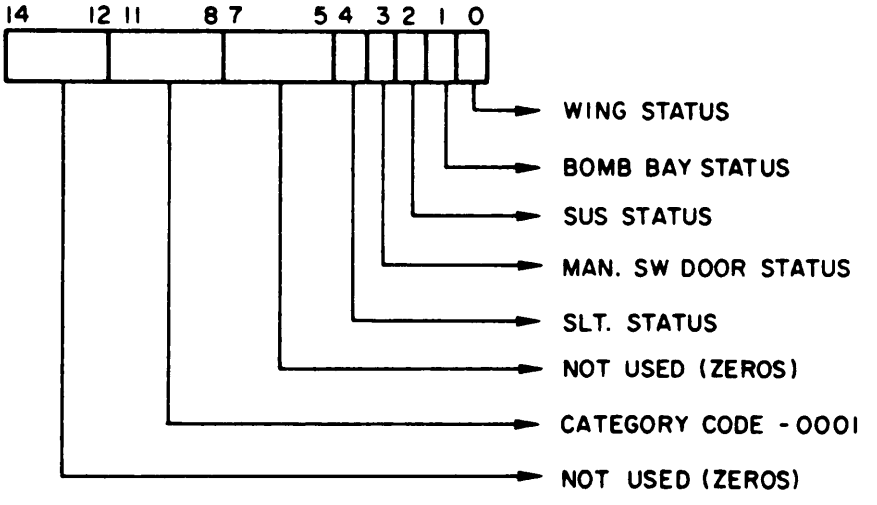


Figure 84. Format for Ordnance Output Logic Interrogate Word Format

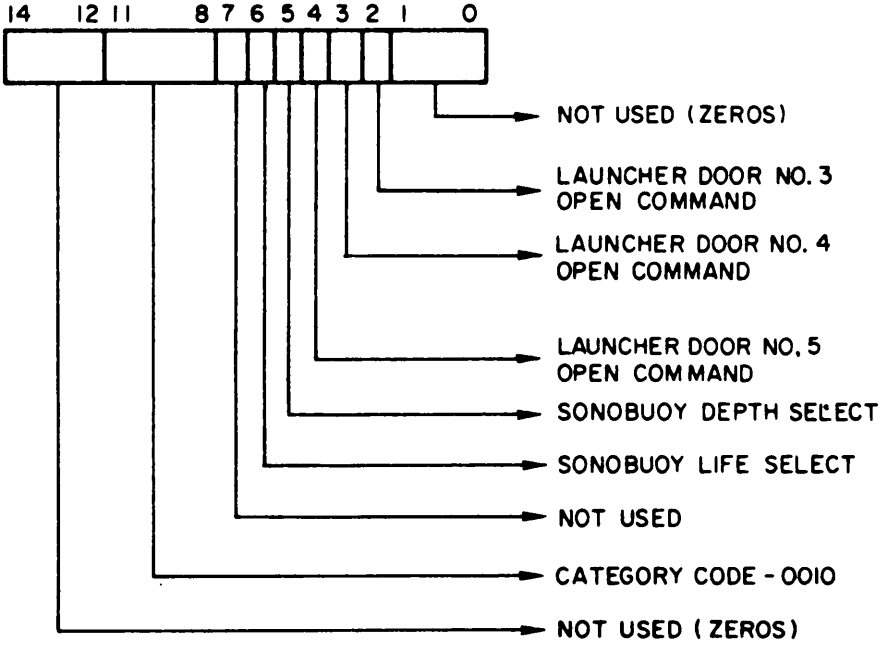


Figure 85. Format for Ordnance Output Logic Ordnance Select Word

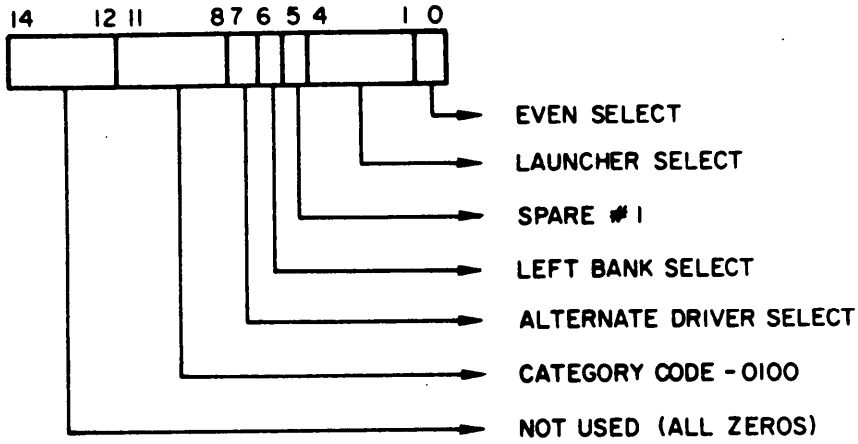


Figure 86. Format for Ordnance Output Logic SLT Status Word

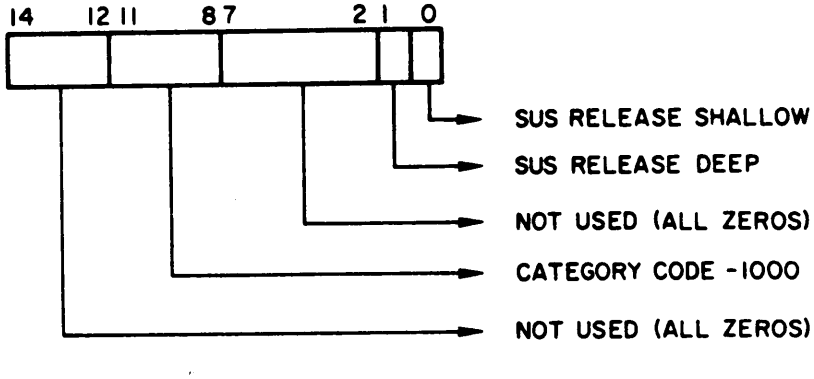


Figure 87. Format for Ordnance Output Logic SUS Launch Word

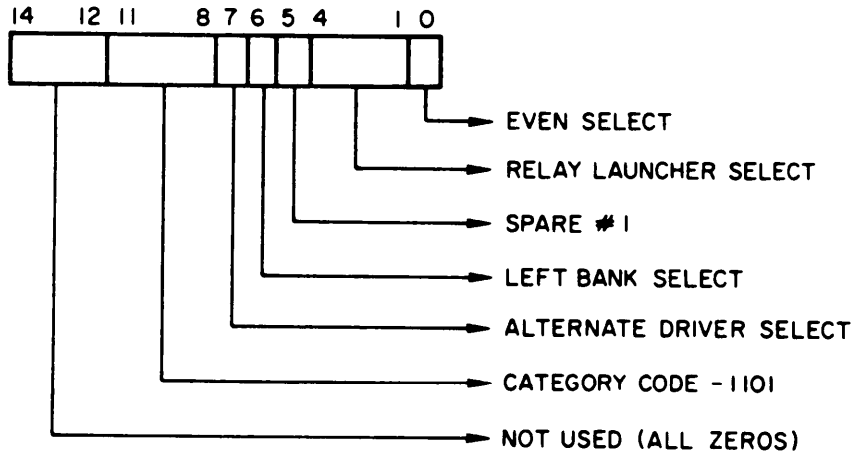


Figure 88. Format for Ordnance Output Logic SLT Select and Launch Word

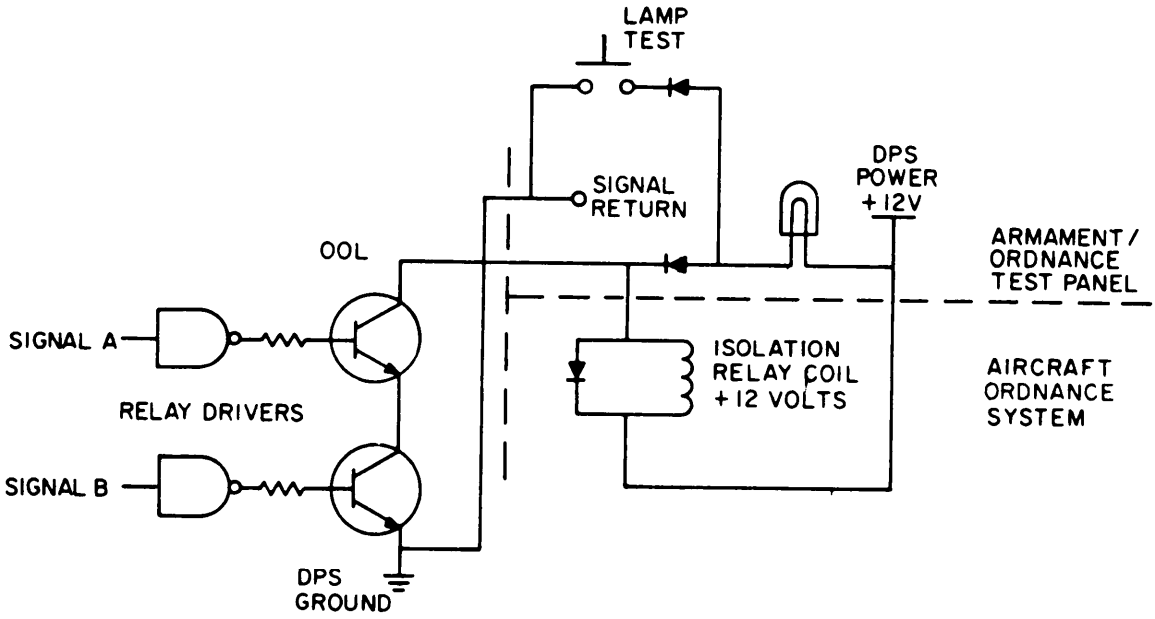


Figure 89. Ordnance Output Logic/Armament Ordnance Test Panel Aircraft Ordnance System Interface

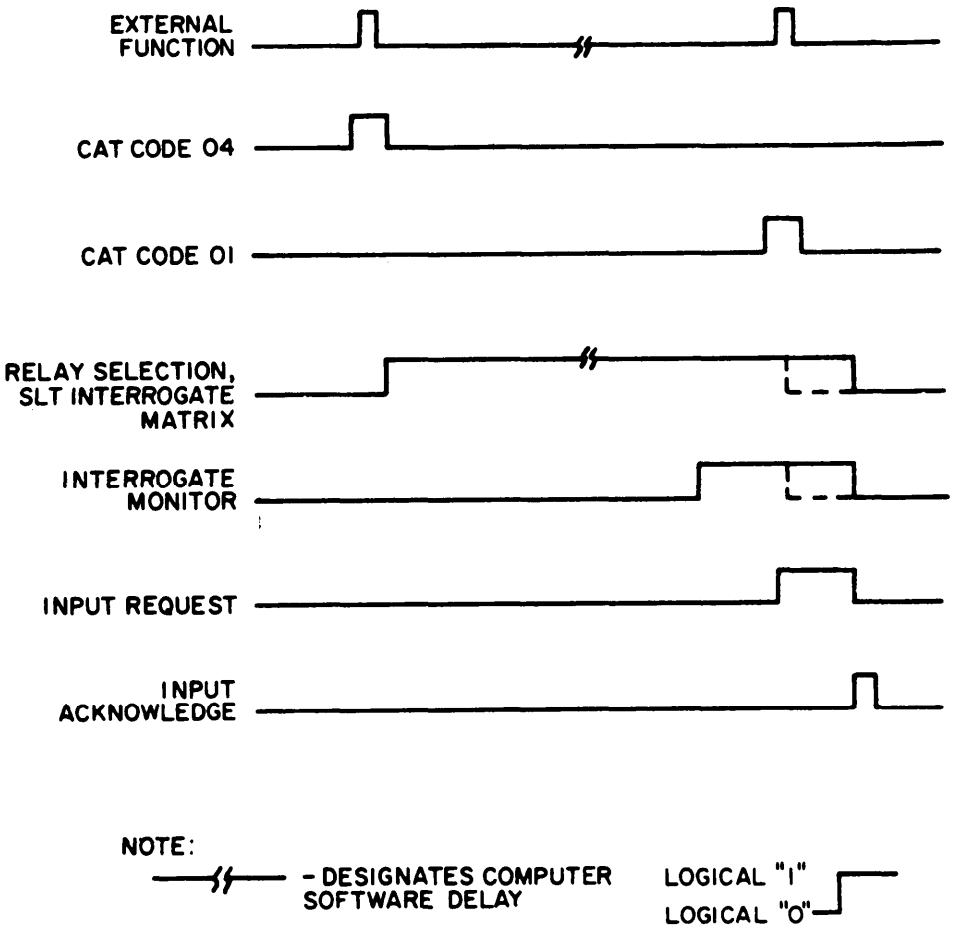


Figure **90.** Ordnance Output Logic SLT Interrogate Timing Diagram

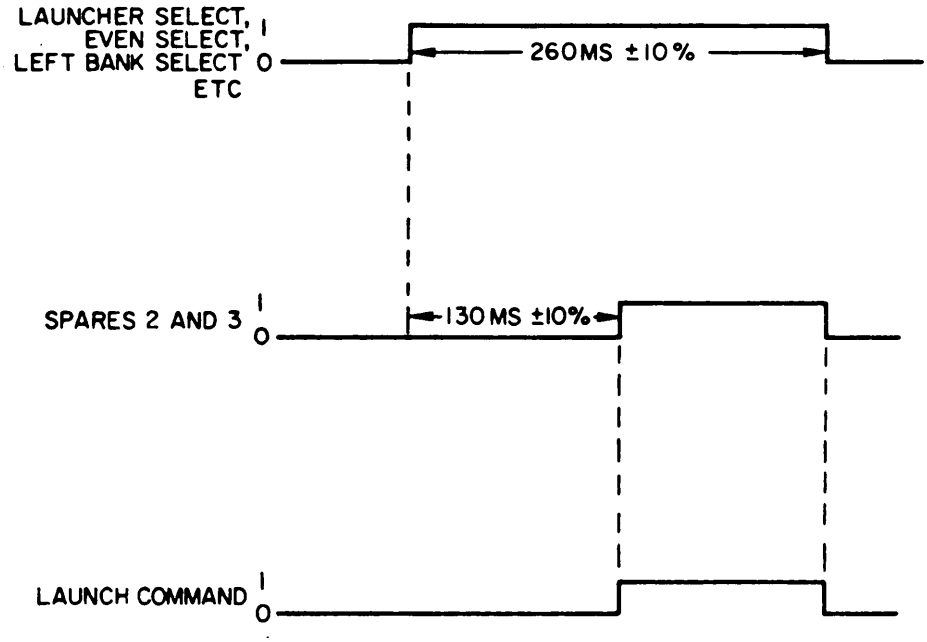


Figure 91. Ordnance Output Logic SLT Select and Launch Timing

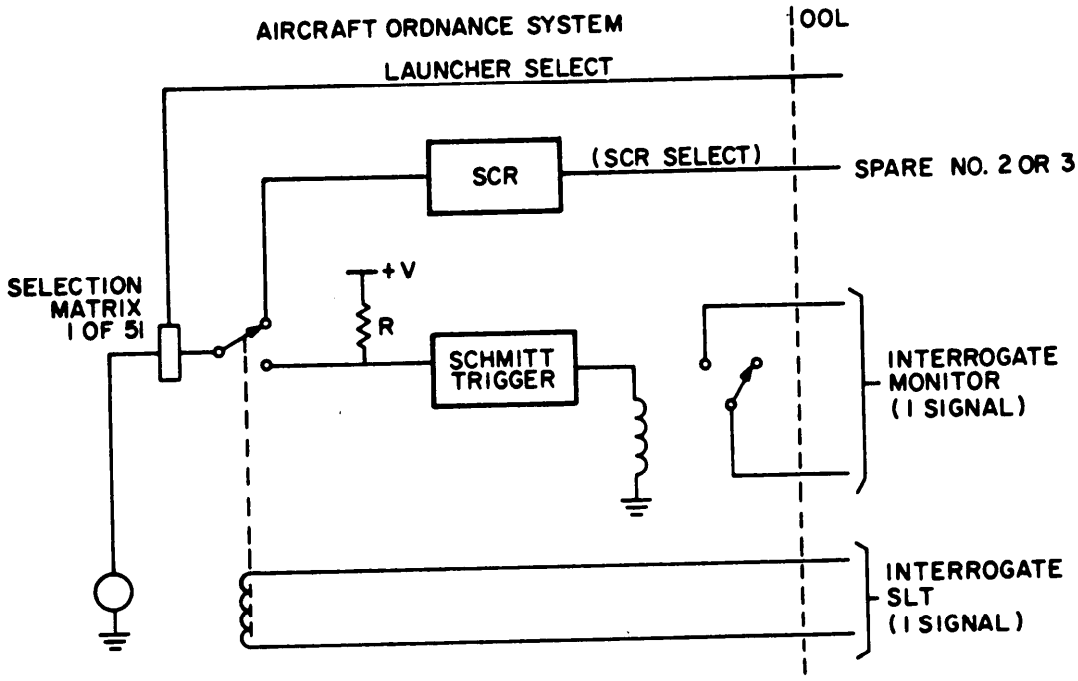


Figure 92. Ordnance Output Logic/SLT System Wiring for Interrogation Mode

3.5.2.4.6 Maintenance Control Panel Subunit

NOTE

Since the Maintenance Control Panels for the four Logic Units are nearly identical, only one over-all MCP description is given. Refer to 3.5.1.4.9.

3.5.2.4.7 Power Supply Subunit - Logic Unit 2 shall contain a Power Supply Subunit as described in 3.3.12.2.

3.5.3 Data Analysis Logic Unit MX-8034/AYA-8 (Logic Unit 3)

3.5.3.1 Function: See 3.4.9.

3. 5.3.2 Form Factor: Refer to illustration in EI-515, Avionics Installation instructions for Data Analysis Programming Group AN/AYA-8B.

3.5.3.3 Weight: See 3.5.1.3.

3.5.3.4 Contents: See 3.4.4.

3.5.3.4.1 Multipurpose Display Logic

3.5.3.4.1.1 Functional Description - The Multipurpose Display (MPD) Logic shall be designed to accept computer generated digital information, convert it to a form suitable for driving a 16 inch Charactron Display with alphanumeric symbols, conies, radar, and low light television patterns as required for the Tactical Coordinator and Sensor Station Operators. The MPD logic shall be capable of transmitting digital information to the computer. Figure 93 is a Functional Flow Diagram of the MPD Logic.

3.5.3.4.1.2 General Description - The MPD Logic Subunit receives signals, in the form of 30 bit parallel words, from the digital computer via the Maintenance Control Panel. These signals are transferred from the computer to the MPD Logic Subunit on an Output Data Request/Output Acknowledge basis or External Function Request/External Function basis.

The characteristics of this interface are described in Appendix I, Computer Input/Output Specification. The MPD Display is required to do several operations in response to the computer words. In one case, it must open an analog information channel to display conic, TV, or radar information, centering it on the computer supplied coordinates. Another command may cause it to draw a line between two points on the display's 512 by 512 coordinate grid. A third may cause it to plot an alphanumeric character or symbol at a specified point. A fourth may require it to print five characters in a horizontal line. There are many variations on the above mentioned operations, which will be described. The MPD requires binary signals to specify CRT beam position, character or symbol selection, analog gate control, properly timed signals for CRT unblinking, and beam focus signals for spot writing. The purpose of the MPD Logic is to convert com - puter signals to a form required by the MPD to perform the above operations. The MPD Logic shall transmit 24 bits of information on an input Data Request/Input Acknowledge basis, to the computer.

3.5.3.4.1.3 Operating Requirements - The MPD Logic shall be capable of performing the following operations:

(1) Receive data from the computer via the Maintenance Control Panel.

(2) Provide information to the MPD for plotting a character.

(3) Provide information for drawing a vector.

(4) Provide initial position, character selection and positioning information for simulating the operation of a typewriter.

(5) Interpreting and operating on digital commands in the typewriter mode.

(6) Provide information to the Function Generator Logic for drawing an ellipse or circle on the MPD.

(7) Provide information to the MPD for opening any of four analog channels.

(8) Interpret an End of Data signal from the computer and synchronize the display frame with the 40 Hz Sync.

(9) Select either the 40 Hz or 57.1 Hz frame Sync to synchronize display operations.

(10) Transmit data to the computer via the Maintenance Control Panel.

3.5.3.4.1.3.1 Modes of Operation - The MPD Logic shall be capable of manipulating input information in several different ways, depending on the setting of the Operating Mode switch located on the MPD console. The switch settings are: On- Line, for normal operation under computer control: Off -Line, for operation of the analog devices (scan converted radar, LLLTV, spare scan converter, and raw radar video on the Sensor Operator's MPD)) without the computer, and several internally generated test patterns for checkout, operational verification, and alignment of the analog portions of the display. Operation in the various modes is as follows:

(1) On-Line Mode - In the On-Line mode of operation, the display shall be under the control of the computer. Only the timing of the individual operations and frame rate timing are controlled by the MPD Logic. Operations performed by the MPD) Logic are: receive and transmit data from and to the computer via the Maintenance Control Panel; provide information for drawing a vector; provide initial position, X and Y position incrementation, and character selection information for simulating the operation of a typewriter; interpreting and operating on digital commands in the typewriter mode such as Carriage Return and End of Message; provide information to the Function Generator for drawing a conic; provide information to the MPD for opening analog channels 1, 2, 3, or 4; interpret an End of Data signal from the computer and use this to synchronize the display frame with the 40 or 57.1 Hz frame rate sync pulse from the Master Timing Logic (MTL).

(2) Off-Line/Analog Mode - The Off-Line mode of operation shall allow the analog channels to be activated manually from the MPD Off-Line/Analog Mode switch, located at the MPD, without the aid of the computer. This mode shall be used for testing or confidence check of the analog channels and peripheral devices. The settings of the Off-Line/Analog switch are: Channel 1, Channel 2, Channel 3, and Channel 4.

(3) Test Modes - To test the various operational functions of the logic and to aid in the alignment of the display, internally generated test patterns shall be incorporated and controlled from the MPD. The test patterns shall include the following: Matrix Test, an alignment pattern showing all 64 selectable characters in an 8 by 8 square array; Registration Test, a Matrix Test pattern except a "plus" sign is superimposed on each character; Vector Test, a pattern of vectors used for a confidence check and length alignment; Type Mode Test, a simulated typewritten page; and Function Generator Test, a confidence check and alignment pattern.

(4) Analog Channel Enable - This mode of operation shall allow for the display of the information present at the analog channels of the MPD, as selected by the MPD's Off-Line/Analog switch, bypassing the MPD Logic Unit. In this mode, all digital signals being transmitted to the MPD shall be a logical "O" except for frame and word sync.

3.5.3.4.1.4 Interface Requirements - Refer to the functional flow diagram (Figure 93).

3.5.3.4.1.4.1 General

3.5.3.4.1.4.1.1 Maintenance Control Panel - Signals between the MPD Logic and MCP shall be as follows:

(1) Computer Signals - The MPD Logic shall receive 30 bits and transmit 24 bit, parallel, binary words from and to the computer through the Maintenance Control Panel. Data transfer is accomplished as described in Appendix I.

(2) Type Spacing Switches - The MPD Logic shall receive two switch information bits from the Horizontal and Vertical Type Spacing switches located on the Maintenance Control Panel.

(3) Test Mode Switches - The Entry Mode operation shall enable the MPD Logic to receive data from the Maintenance Control Panel via the MCP Data Register pushbuttons. The logic operates on the data once every 25 milliseconds. For operations which normally require two words, the Test Mode Switch located on the Maintenance Control Panel, is set to the desired position (Plot or Analog, Vector, and Type) and only the second word need be entered into the pushbutton switches. For Conies, the second and third words may be transferred to the Function Generator with the Conic 1 and Conic 2 buttons.

(4) Reset, Request Word, Sync and Load Conic Switches - The MPD Logic shall receive switch position information lines from Reset, Request Word, Sync and Conic switches located on the Maintenance Control Panel.

(5) Verify Switch - In the Verify mode of operation, the logic' shall perform in exactly the same manner as the On-Line mode, except for the following: The Output Data Request line is controlled by a Request Word pushbutton at the Maintenance Control Panel in order that only one operation can be performed at a time. A consequence is that the 40 or 57.1 Hz Line Sync is no longer effective. In this mode the Maintenance Control Panel shall store each computer word and display the word on the panel. A Reset pushbutton shall be provided on this panel to extinguish the lamps. The MPD Logic shall not act on this data.

(6) Clock - The MPD Logic shall receive a 2.000 MHz square wave from the MTL. This signal shall be used to time logic operations within the MPD Logic.

3.5.3.4.1.4.1.2 Master Timing Logic - Signals between the MPD Logic and MTL shall be as follows:

(1) 40 or 57.1 Hz Sync - The MPD Logic shall receive a 40 Hz or 57.1 Hz Sync pulse from the MTL via the MCPL. This signal is used for Frame Sync of the MPD Logic.

(2) Analog Enable - The MTL shall transmit two Analog Enable signals to the MPD Logic. These signals are used by the MPD Logic to generate Analog Enable signals which are sent to the MPD.

(3) Channel Enable - The MPD Logic shall transmit two Channel Enable signals to the MTL. These signals are used to inform the MTL when to enable the Radar and Spare Scan Converters.

(4) One Hz Flash - The MPD Logic shall receive a one Hz square wave from the MTL. This signal and the Flash bit received from the computer are used by the logic to generate a blinking character on the MPD.

(5) LLLTV Active - The MPD Logic shall transmit the LLLTV signal to the MTL. This signal shall select display/computer synchronization to be either at a 40 or 57.1 Hz frame rate.

3.5.3.4.1.4.1.3 Multipurpose Display - Signals between the MPD Logic and MPD shall be as follows:

(1) Vertical Position - The MPD Logic shall transmit a nine-bit parallel word representing the vertical position, center 000000000, binary count toward top of screen. one's complement toward bottom. Figure 94 illustrates the display screen and the octal count of the various positions.

(2) Horizontal Position - The MPD Logic shall transmit a nine bit parallel word representing the horizontal position, center 000000000, binary count toward the right of screen, one's complement toward the left.

(3) Character Select - The MPD Logic shall transmit a six bit parallel word representing one of a possible 64 characters to be displayed on the MPD. Figure 94 illustrates the octal code of the various characters.

(4) Character, Vector, and Cursor Unblank - The MPD Logic shall transmit to the MPD three lines for the unblinking of the MPD screen.

(5) Focus - The MPD Logic shall transmit to the MPD three parrel lines containing analog or vector, character, and cursor focus data.

(6) Enable Analog Deflection - The MPD Logic shall transmit to the MPD four lines to inform the MPD which of the four analog deflection channels to display on the screen.

(7) Enable Analog Video - The MPD Logic shall transmit to the MPD four lines to inform the MPD which of the four analog video channels to display on the screen.

(8) Operation Mode Switch - The MPD Logic shall receive from the MPD console three lines that contain information as to the position of the Operation Mode Switch. The codes for this switch shall be as shown below, where switch closure represents a logical "1".

Switch Position	Switch Position Label	Switch Code
1	On-Line	000
2	Off-Line/Analog	001
3	Matrix Test Pattern	010
4	Registration Test Pattern	011
5	Vector Test Pattern	100
6	Type Test Pattern	101
7	Function Generator Test Pattern	110
8	Analog Channel Enable	111

(9) Off-Line/Analog Mode Switch - The MPD Logic shall receive from the MPD console two parallel lines that inform the logic as to the position of the Off-Line/Analog Mode Switch. The codes for this switch shall be as shown below, where switch closure represents a logical "l".

Switch Position	Switch Position Label	Switch Code
1	Channel 1	00
2	Channel 2	01
3	Channel 3	10
4	Channel 4	11

(10) Switch Common - The MPD Logic shall provide a reference line for the Operation Mode and Off-Line/Analog Switches.

(11) Overflow Indicator - The MPD Logic shall provide to the MPD two lines for overflow indication.

(12) Vector Slope - The MPD Logic shall transmit to the MPD a nine-bit parallel word which contains the vector's major axis length.

(13) Major Axis - The MPD Logic shall transmit to the MPD a signal that informs the MPD whether the X or Y axis is the major axis of the conic.

(14) X and Y Sign - The MPD Logic shall transmit to the MPD two parallel bits which inform the MPD of the sign of the X and Y axis in a vector figure.

(15) Sweep Enable - The MPD Logic shall transmit to the MPD an enable signal used to release the sweep generator in the MPD.

(16) Sync Signals - The MPD Logic shall transmit to the MPD two sync signals.

(a) Frame sync

(b) Word sync

3.5.3.4.1.4.1.4 Function Generator - Signals between the MPD Logic and Function Generator shall be as follows:

(1) Conic Words - The MPD Logic shall transmit to the Function Generator two 20-bit parallel words. These words shall define to the Function Generator the specific ellipse, circle, or straight line to be displayed on the MPD.

(2) Function Generator Test - The MPD Logic shall transmit to the Function Generator signals which allow for the Off-Line testing of the Function Generator.

(3) Control 1 and 2 - The MPD Logic shall transmit to the Function Generator two parallel lines that inform the Function Generator which word is presently being transmitted.

3.5.3.4.1.4.2 Input/Output Signal Characteristics

3.5.3.4.1.4.2.1 Maintenance Control Panel, Master Timing Logic and Function Generator - All internal signals between the MPD Logic and the Maintenance Control Panel, Master Timing Logic, and Function Generator shall be transmitted over single ended lines where logical "O" = O + O. 5 -0.0 volts and logical "l" = +5 ±1.5 volts. The 30 input and 30 output data lines and control signals are available from the Maintenance Control Panel.

3.5.3.4.1.4.2.2 Multipurpose Display Logic - The MPD Logic Input/Output Signals to and from the MPD shall be as follows:

(1) Twisted Pair Transmissions - The following transmissions shall be via twisted pair cable with line driver circuits as referenced in WR -101 Part II. Each pair shall be terminated by an input amplifier as defined in Appendix II or its electrical equivalent. The cable shall be limited to 100 feet maximum.

(a) Vertical Position -9 pairs

(b) Horizontal Position - 9 pairs

(c) Character Selection -6 pairs

(d) Character and Cursor Unblank -2 pairs

(e) Focus -3 pairs

(f) Enable Analog Deflection -4 pairs

(g) Enable Analog Video -4 pairs

(h) Vector Slope - 9 pairs

(i) Major Axis -1 pair

(j) X and Y Sign -2 Pairs

(k) Frame and Word Sync - 2 pairs

A logical "O" shall be 4 +1 volts, a logical "l" shall be O +0.5, -0.0 volts. Transition times shall be less than one microsecond when measured at the 10% and 90% amplitude points.

(2) Single Ended Transmissions

(a) Switch Common - This line shall be the common reference for the Operation Mode and Off- Line/Analog Mode Switches and shall have no other connection within the M PD.

(b) Operation Mode Switch - The three coded lines going to the MPD Logic shall have no internal connection within the MPD.

(c) Off-Line/Analog Switch - The two coded lines going to the MPD Logic shall have no connection within the MPD.

(d) Overflow Indicator - The two lines transmitted to the Overflow Indicator shall be 5 ±0.5 volts at 150 milliamperes maximum and the overflow active signal where "open" represents light ''off" and 0 ±0.5, -0.0 volts represents light "on". These signals shall have no other connection within the MPD. The 5 +0.5 volts at 150 milliamperes maximum shall be referenced to the overflow active line.

(3) Triaxial Transmissions - All coaxial transmissions shall be via Amphenol 421-033 cable or equivalent terminated in a differential amplifier with an input impedance of 90 to 95 ohms and 100 picofarads maximum. The following signals shall be transmitted via triaxial cables.

(a) Vector Unblank

(b) Sweep Enable

A logical "O" shall be 0 + 0.5, -0.0 volts, a logical "1" shall be 5 +1 volts. Transition times shall be less than 100 nanoseconds when measured at the 10% and 90% points. Triaxial cable lengths shall not exceed 100 feet.

3.5.3.4.1.4.3 Word Formats

3.5.3.4.1.4.3.1 Computer Output Signals - Output signals from the computer are in the form of a 30-bit parallel binary word. Word formats are shown in Figure 95.

3.5.3.4.1.4.3.1.1 Function Code - The Function Code of the Set or Plot word is used to identify that word. The function code designator is located in bit positions 4 and 3. The function code "01" shall designate the Plot function while the function code "10" shall designate the Set function.

3.5.3.4.1.4.3.1.2 X and Y Position Fields - The X and Y position fields are used only when a Plot or Set word has been received. The nine bit binary numbers located in each one of these fields shall be suitable for commanding the X and Y axis deflection circuits, in the MPD, to place the electron beam on the viewing screen of the MPD. The nine-digit binary numbers are represented by three-digit octal numbers. The positive number scale extends from zero to a maximum of" 377 octa!. Negative binary numbers are represented by corresponding one's complement binary

numbers. The octal representation of the one's complement binary number extends from octal 777 to octal 400, corresponding to minus zero and minus 377 octal respectively.

3.5.3.4.1.4.3.1.3 Inhibit Control - In the Plot or Set word the Inhibit Control (I), bit 1, shall provide for either displaying or not displaying the Plot or Set word command (i.e. if a Set word and an Inhibit bit are received, the display operation associated with that Set word is inhibited.) A logic "1" indicates an Inhibit operation while a logic "O" indicates normal operation.

3.5.3.4.1.4.3.1.4 Flash Control - In both the Plot and Set Position Words, bit 2 shall provide for flashing either the plot character or the first character of a type sequence. The flashing shall be at a one Hz rate; one-half second on, one-half second off. The code "0" shall call for a steady presentation whereas the code "1" shall cause the MPD Logic to flash the proper character at the prescribed rate.

3.5.3.4.1.4.3.1.5 Plot Character - In the Plot Word the character (CHAR) to be presented from the Character Matrix shall be selected by the six-digit binary number in bit positions 15 through 20 inclusive. The octal code for character selection is shown in Figure 96.

3.5.3.4.1.4.3.1.6 Bits "O" and "5" - In both the Plot Word and Set Position Word the function of bits "O" and "5" shall be unassigned.

3.5.3.4.1.4.3.1.7 Set Position Word Control Field - The Set Position Word Control Field shall be composed of the six bits from bit position 15 through bit position 20 inclusive. The Control Field codes and associated display operations are shown below:

Control Field Code (Octal)	Display Operation
00	No Display Operation
01	No Display Radar Scan Converter Outputs
02	Display LLLTV Outputs
03	Display Spare Scan Converter Outputs
04	Display Ftmction Generator Outputs
05	Display Vector
06	Display Normal Type Sequence
07	Display Short Type Sequence
10	End of Data
11	Display Raw Radar Video
12	40 Hz Sync
13	57.1 Hz Sync

(1) Control Field Code 01 - The Set Position Word Control Field Code 01 shall cause the Logic to enable the MPD to display the radar information being stored by the" Radar Scan Converter. The X and Y coordinates of the Set Position Word having a Control Field Code 01 shall cause the X and Y Deflection circuits to center the radar presentation on the specified X and Y coordinates.

(2) Control Field Code 02- The Set Position Word Control Field Code 02 shall cause the Logic to enable the MPD to display the signals from the LLLTV. The X and Y coordinates of the Set Position Word having a Control Field Code 02 shall control the X and Y Deflection circuits to center the presentation on the specified X and Y coordinates (normally expected to be 000 and 000 respectively). When in the LLLTV mode, no EOD word shall be sent to the MPD.

(3) Control Field Code 03 - The Set Position Word Control Field Code 03 shall cause the Logic to enable the MPD to display the sensor signals being stored by the Spare Scan Converter. The X and Y coordinates of the Set Position Word having Control Field Code 03 shall control the MPD X and Y Deflection circuits so as to center the presentation on the specified X and Y coordinates.

(4) Control Field Code 04 - The Set Position Word Control Field Code 04 shall command the Function Generator in such a manner that a conic in the form of an ellipse, circle, or straight line shall be generated, centered about the X and Y positions specified in the Set Position word containing the Control Field Code 04. The next two digital words immediately following this Set Position word shall be the two sequential Conic words having the formats shown in Figure 97.

Figure 99 illustrates the manner in which an ellipse shall be specified. Circles result when ax equals b_y, and a_y and b_x are zero. Straight lines result when either ax and a_y, or b_x and b_y are zero.

(5) Control Field Code 05 - Set Position Word Control Field Code 05 shall command the Logic to cause the MPD vector generator to prepare to generate and display a vector with the origin of the vector specified by the X and Y position given in the Set Position Word. Additional information concerning the vector to be displayed shall be given by the succeeding Vector word having the format shown in Figure 98.

(a) Vector Format - As outlined in 3.5.3.4.1.4.3. 1.7(5), a vector shall be described in terms of its projections along the X and Y axis (Ax and A y). The longer projected length shall be identified by the binary digits in bit positions 21 through 29 inclusive. The axis along which the longer projection lies shall be identified in bit position 17 where the X and Y axes are identified by “1” and “O” respectively. The direction of the vector extension from its origin shall be identified by the “signs” located in bit positions 16 and 15, the X and Y quadrant signs respectively. A “0” shall represent “+” and a “1” shall represent “-”. The slope of the vector. identified by the binary digits in bit positions 6 through 14 inclusive, is defined as the ratio of the smaller to the larger of the absolute values of Δx and Δy multiplied by 511. Vector generation is shown in Figure 100, where the vector origin shall be the X and Y coordinates given in the Set Position word. The vector extension, as specified by the “1” and “0’” in bits 16 and 15 of the Vector word. shall be into the + X and - Y quadrant of a Cartesian coordinate system assumed to originate at the specified X, Y vector origin. The length shall be specified along the X axis by the “l” in bit 17 and the octal 140 in the length segment, bits 29 through 21 inclusive. The angle made with the larger projection on the X axis shall be determined by the slope of 2/3 times 511 which is octal 525 as specified in bits 14 through 6 inclusive.

(6) Control Field Code 06 - Set Position Word Control Field Code 06 shall command the Logic to present a sequence of characters beginning at the X and Y position specified in the Set Position word. The characters to be typed shall be specified by a following series of Type words, each containing five character symbols identical to those of Figure 96 except that code 36 shall call for Carriage Return instead of symbol ⊙, and code 41 shall call for End of Message rather than symbol ▭.

(7) Control Field Code 07 (Short Type Mode) - Set Position Word Control Field Code 07 shall command the Logic to present a sequence of five characters beginning at the X and Y position specified in the Set Position word having the Display Control Field Code 07. Furthermore, Control Field 07 shall cause the Logic to respond at the end of the fifth character presented as though an End of Message character followed as described for the Control Field 06 type code in 3.5.3.4.1.4.3.1.7 (6). The formats for the Set Position Word Control Field 07 and the immediately following five character sequence shall be as shown in Figure 101. The character codes are given in Figure 102,

(8) Control Field Code 10 (EOD) - The function of the EOD Control Field Code shall be to cause an end to the MPD’s request for further data from the computer pending arrival of the next 40 Hz Sync pulse. If a Sync pulse is received following a sequence of words but prior to a Control Field Code 10, an alarm overflow indicator light shall be lit except during operation of the

analog modes described in 3.5.3.4.1.4.3.1. 7(2) and 3.5.3.4.1.4.3.1. 7(9). If an EOD command is received in the cycle immediately after the alarm occurs, operation at a 20 Hz rate continues: if no EOD occurs during either the first or second cycle, then the MPD Logic will generate its own reset upon receipt of the second 40 Hz Sync pulse.

(9) Control Field Code 11 - The Set Position Word Command Field 11 shall cause the Logic Unit to select and display the Raw Radar Video information from the AN/APS-80 ( ). The X and Y coordinates presented in the Set Position word having a Control Field of 11 shall cause the X and Y Deflection circuits to center the radar presentation on the specified X and Y coordinates. This radar presentation can be either a PPI or "A" scan presentation, depending on the function selected.

(10) Control Field Codes 12 and 13 - The Set Position Words with Control Field Codes 12 and 13 shall select either the 40 Hz or 57.1 Hz frame sync signals for synchronization among the MPD, central computer, and display associated analog devices. A Set Position word containing a Control Field Code 12 shall be transmitted to the MPD Logic each time there is a change in display presentation from LLLTV to a display format other than LLLTV. Upon receipt of this code the MPD Logic shall transmit a logical "0" on the LLLTV Active line to the MTL to select the 40 Hz Frame Sync signal. A Set Position Word containing a Control Field Code 13 shall be transmitted to the MPD Logic each time there is a change in display presentation to LLLTV from a display format other than LLLTV. Upon receipt of this code the MPD Logic shall transmit a logical "1" on the LLLTV Active line to the MTL to select the 57.1 Hz Frame Sync signal.

3.5.3.4.1.4.3.1.8 Diagnostic - The 16-bit diagnostic instruction word shall initiate diagnostic operation in the MPD Logic.

3.5.3.4.1.4.3.2 Input Computer Signals - Input signals to the computer shall be in the form of 30-bit parallel words plus control lines. These data lines shall provide diagnostic information to the computer.

3.5.3.4.1.5 Description of Multipurpose Display Logic Operation - The sequence and timing of each of the operations performed by the MPD Logic are outlined in the following paragraphs.

3.5.3.4.1.5.1 Load Data - In the On-Line Mode of operation, data is transferred from the computer to the MPD Logic on a Request - Acknowledge basis as described in Appendix I. Upon sensing the presence of an Output Acknowledge signal, the Logic clears its input register and loads the new 30-bit computer word. If the Inhibit bit is marked, the data is discarded and a new word is requested except in the case of the Typewriter mode. If the Inhibit bit is not marked, the Logic will operate on the word in accordance with the coding as explained below. In the various test modes of operation, data is loaded from the internal test pattern generator in a manner analogous to computer data.

3.5.3.4.1.5.2 Plot Character - The MPD Logic decodes this command, stores and sends the position information to the MPD, sends the character selection information to the MPD and waits 16 microseconds for deflection settling. Then the Logic sends a 24 microsecond Character Unblank signal to the MPD. At the end of this period, another request for information from the Computer is generated. Positioning information is stored separately from the input register because in some other modes, it must be remembered between operations. Figure 103 illustrates timing constraints for the Plot Mode.

3.5.3.4.1.5.3 Set Position - The Logic interprets this command, stores the position information and sends it to the display, and further interprets the Control Field Code to determine the subsequent operation. Some operations, such as Analog Channels 1, 2, 3, or 4 in the case of a Raw Radar Video presentation, or End of Data, require no additional information from the computer. For analog presentations, the Logic, upon receipt of the Set Position word, transmits the proper analog deflection enable signal, spot focus signal, and position and character (code 00) bits to the MPD. Sixteen microseconds later, the proper video enable signal is transmitted to the M PD. For an end of data, the Logic inhibits the generation of the Output Data Request until the 40 Hz Sync signal.

The other operations, Vector, Type, and Conic, require more computer information, so the Logic stores the command, and raises the Output Data Request line. Timing for the analog operations is illustrated in Figure 104. The operations are as follows:

(1) Analog Channel 1 - The Set Position word generates the necessary signals to open the MPD's analog gates for display of the stored radar scan converter presentation. The Logic will also generate an enable signal to the MTL which will return a timed scan converter read enable signal to the MPD Logic. The trailing edge of this signal will cause the MPD Logic to close the channel and request a new computer word.

(2) Analog Channel 2- The Set Position word generates the proper signals to open the MPD's analog gates for LLLTV readout. The LLLTV presentation will continue until the next 57.1 Hz Sync signal is received, at which time channel 2 will be closed and a request for a new computer word will be initiated.

(3) Analog Channel 3 - The Set Position word for analog channel 3 initiates the same chain of events for channel 3 as it did for channel 1, for Spare Scan Converter.

(4) Analog Channel 4 - The Set Position word for analog channel 4 will control the display of conies on the TACCO MPD and a raw radar video on the Sensor Operator's MPD. Upon receipt of the appropriate Set Position word, enable signals shall be generated in the MPD Logic which will open the MPD's analog gates for the positioning, unblank, and video information from either Function Generator or Radar Interface Unit.

At the end of each conic presentation, as signaled by the change of state of the Function Generator Unblank signal from Unblank to Blank, the Logic Unit shall send an Output Data Request signal to the computer. Raw radar video presentation shall be enabled from the time that the Logic Unit receives a Set Position word containing a Control Field Code of 11 until the time the next 40 Hz Sync pulse is received.

(5) Vector - If the previous Set Position word requested a vector, the MPD Logic will interpret the next word as such. The vector major axis length is loaded into a nine-bit, two MHz length counter. The nine-bit slope signal is sent out to the MPD as are the major axis and sign bits. The Logic releases the clamp (sweep enable) on the MPD sweep generator, starts the Vector Unblank, and starts the length counter de cementing toward zero. When the length counter reaches zero, the MPD Logic stops the Vector Unblank, reinstitutes the clamp on the sweep generator, and raises the Request line to the computer. The vector requires 1/2 microsecond for every plotting point of length: Negative minor axis components require the slope to be expressed in one's complement form. This shall be done automatically by the computer. The timing constraints for vector generation are illustrated in Figure 105.

(a) Analog Vector Generator - The MPD contains a device whose purpose is to draw straight lines in any of 2048 different directions and with any of 512 different lengths, on the CRT screen. It does this by generating x - axis and Y - axis components of a constant rate sweep waveform whose time duration is proportional to the desired line length, as shown in Figure 106. The major axis sweep is multiplied by 1, the minor axis sweep by the slope, a fraction of 512.

(6) Type - If the Set Position word requested the 'Typewriter mode, the series of words following will be interpreted as Type words. The Logic examines each character code for the special codes Carriage Return and End of Message on the selection lines. The position from the Set Position word is stored in a margin register, a horizontal position register, and a vertical position register. The Logic gates the first six bits of the Type word onto the character selection lines to the display, waits approximately four microseconds, and if the character is not a special code, raises the Character Unblank for 24 microseconds. The Logic then gates the next group of six bits onto the selection lines, advances the horizontal position register, and repeats the process. Altogether, the MPD Logic performs the above process for all five six-bit groups in the input register, i.e;, one computer word, then raises the request line to the computer for the next word. However, if a Carriage Return code is encountered, the MPD Logic will suppress the Unblank, reload the horizontal position

register with the contents of the margin register, decrement the vertical position register, delay for 16 microseconds to allow for settling, and then process the next character. An End of Message code will reset the MPD Logic from the Type mode. Whenever the horizontal or vertical position registers reach maximum deflection, further position incrementing shall be inhibited until receipt of a Carriage Return or End of Message code.

Following the presentation of the first character at the X and Y position of the Set Position Word, each succeeding character shall be presented approximately 1/6 of an inch to the right. The Carriage Return character shall cause the immediately succeeding character to be presented approximately 1/5 of an inch below the first character of the preceding row of characters. The horizontal spacing shall be selectable by means of an appropriate switch from 6/512 of the useful tube diameter to 8/512 of the diameter. Similarly, the vertical spacing shall be selectable by means of a switch from either 8/512 of the useful diameter to 12/512 of the diameter. The End of Message shall command the Logic to terminate the Type sequence. The sequence of words from the Set Position Word containing Control Field Code 06 to present the type series ABCD, EFGH in two rows shall be as shown in Figure 107. The characters are selected from Figure 102, a modification of Figure 96, as explained in the preceding sentences. The presentation of the above sequence of words is illustrated in Figure 108 where the expanded character spacings of 8/512 horizontally and 12/51 2 vertically are shown.

(7) Short Type - Timing for the Short Type operation shall be identical to that of .3.5.3.4.1.5.3 (6) except that an automatic End of Message shall be performed after the fifth character. If End of Message or Carriage Return codes are present in any of the five character locations, they shall be executed as described in 3.5.3.4.1.5.3(6).

(8) Flash, Inhibit, and End of Data (EOD) - The Flash, Inhibit, and End of Data bits serve to modify operation as follows: Whenever the flash bit is programmed in a Plot word, the plot character blinks at a one Hz rate. When the flash bit is programmed in a Set Position Type (or Short Type) word, the first character in the Typewriter mode blinks. Whenever an Inhibit bit is programmed in a one-word operation such as Plot or Set Position Analog, the MPD Logic will reject that word and request another immediately. When an inhibit bit is programmed for a multiword operation, not only is the Inhibited word rejected, but all subsequent related words are rejected. Whenever a Set Position (EOD) word is programmed, the MPD Logic will stop and wait for the next 40 Hz Sync pulse to send a request for computer data. Whenever a 40 Hz Sync pulse occurs, the MPD Logic tests for the prior receipt of an (EOD) function command if information other than raw radar video was displayed in the previous cycle. When display operations are synchronized with the 57.1 Hz Sync pulse, no check for an EOD is made. The absence of an End of Data word will enable an alarm (energize an Overflow lamp at the MPD). If an EOD command is received in the cycle immediately after the alarm occurs, operation at a 20 Hz rate continues. If no EOD occurs during either the first or second cycle, then the MPD Logic will generate its own reset upon receipt of the second 40 Hz Sync pulse.

(9) Conic - If the previous Set Position word specified a conic, the MPD Logic shall store this command, route the next two computer words to the Function Generator and open analog channel 4 in the MPD. It must accept a reset signal from the Function Generator. It will close the analog channel and reset from the Conic mode upon sensing the end of the reset signal from the Function Generator. A description of the operation of the Function Generator is given in 3.5.3.4.3.

(10) Non-operational Modes - Upon receipt of a Function Code 00 or 11 (binary) or Control Field Codes 14 through 77 (octal) the MPD Logic shall perform no display operation but shall request a new computer word.

3.5.3.4.1.5.4 Test Mode Operations - The test modes are controlled by an internal test pattern generator, and consist of: Matrix Test Alignment Test, Vector Test, Type Test and Conic Test. Data for the patterns is derived through gating from a counter which is synchronized with the 40 Hz line. The data is re-loaded into the input register through a Request Acknowledge scheme equivalent to On-Line operation. Operation in the test mode is as follows:

(1) Matrix Test - The Matrix Test uses a series of 64 Plot commands to achieve the pattern shown in Figure 109. The X and Y axes of the display are shown

here for convenience as are the octal locations of the corners of the pattern. They do not appear on the display.

(2) Alignment Test - The Alignment test uses a series of 128 plot words (the first half of which are exactly the same as Matrix Test) to obtain the pattern shown in Figure 110. The symbol "+" is superimposed over every symbol as an alignment aid.

(3) Vector Test - The Vector Test uses a pattern of 16 Set Position words interspersed with 16 Vector words to generate the Vector alignment pattern shown in Figure 111. Starting point locations, direction arrows, and sequence numbers show how the pattern is generated. but do not appear on the display.

(4) Type Test - The Type Test uses a Set Position Type command followed by 128 words containing a character code in the fifth character position, and all “1’ s“ in the other positions. The row and column positions shown in Figure 112 depend upon the setting of the horizontal and vertical Type Spacing switches.

(5) Conic Test - The Conic Test uses five Set Position Conic commands and 10 Conic Word Commands to achieve the pattern shown in Figure 113.

3.5.3.4.1.5.5 Off- Line/Analog Operation - With the Operating Mode switch on the MPD console in the Off- Line/Analog position, the operator may open one of the four analog channels by setting the Off- Line Analog switch at the MPD to Channel 1, Channel 2, Channel 3, or Channel 4. The switch contacts will cause the MPD logic to put the appropriate Set Position analog word into the input register at the 40 Hz Sync time for Channels 1, 3, and 4 and at the 57.1 Hz Sync time for Channel 2. The word will be reset as in the On- Line mode. Display coordinates will be centered on the display screen.

3.5.3.4.1.5.6 Test Mode Operation - With the Mode selector switch on the MCP in the Test position and the Test Mode Selection switch on the Maintenance Panel in the One Word position, the operator can manually enter a word into the input register using the 30 pushbutton-indicator switches on the Maintenance Control Panel. The display will act on this word at a 40 Hz frame rate, plotting a character or doing the appropriate analog operation, except for display of LLLTV which will be presented at a 57.1 Hz frame rate. If the operator wishes to do a two word operation such as Vector or Type, he positions the Test Mode Selection switch to the Vector position or the Type position, then manipulates the input Test switches for the second word. Positioning is centered for a two or three word operation. If the operator wishes to display a conic, he sets the Test Mode Selection switch to the Conic position and stores the second word of Conic operation in the MCP by depressing the Conic One pushbutton. The third word of Conic operation is stored in the MCP Data Register and the Conic display is initiated by depression of the Conic Two pushbutton. As before, the conic is displayed at a 40 Hz rate.

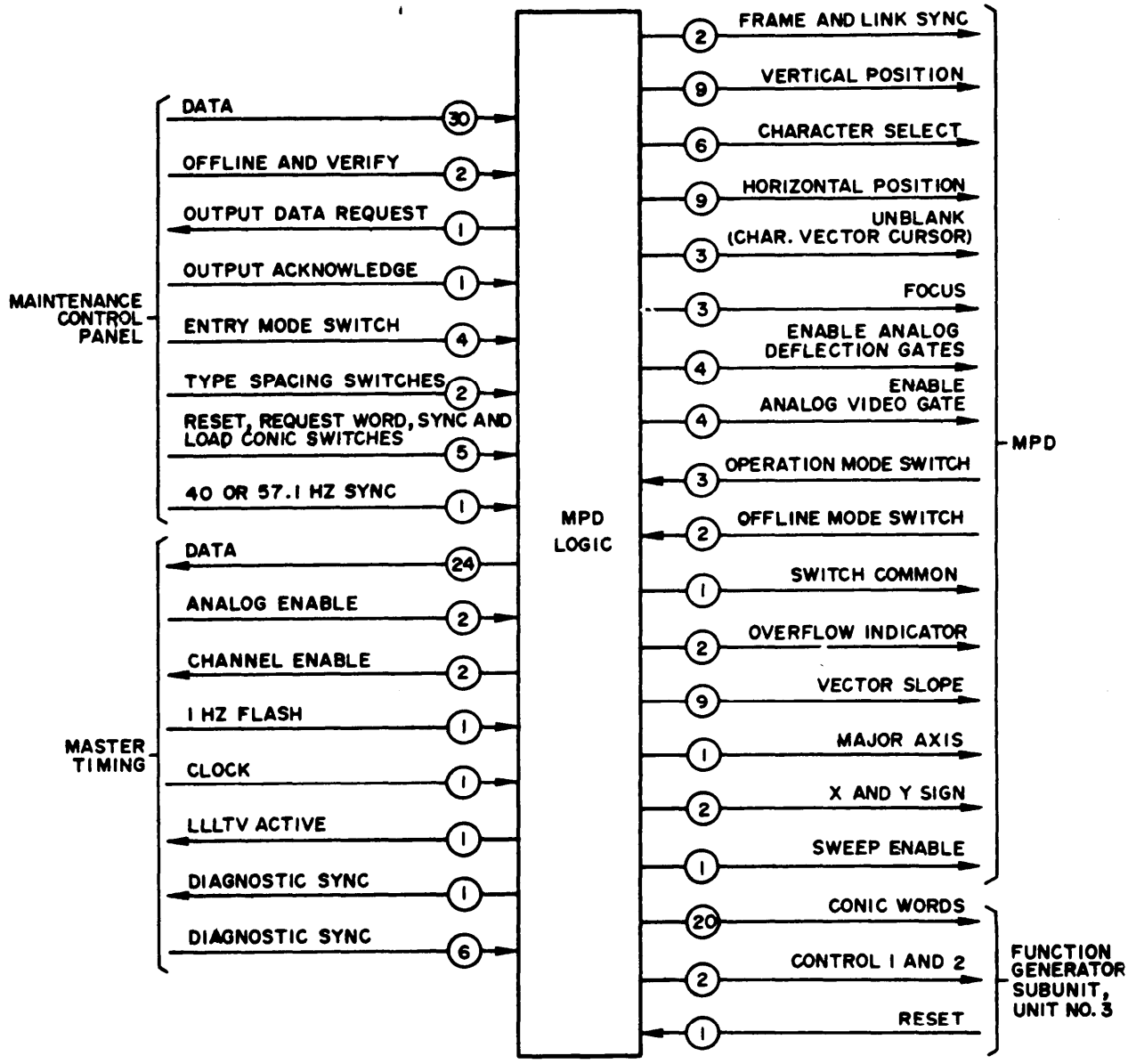


Figure 93. Multipurpose Display Logic, Functional Flow Diagram

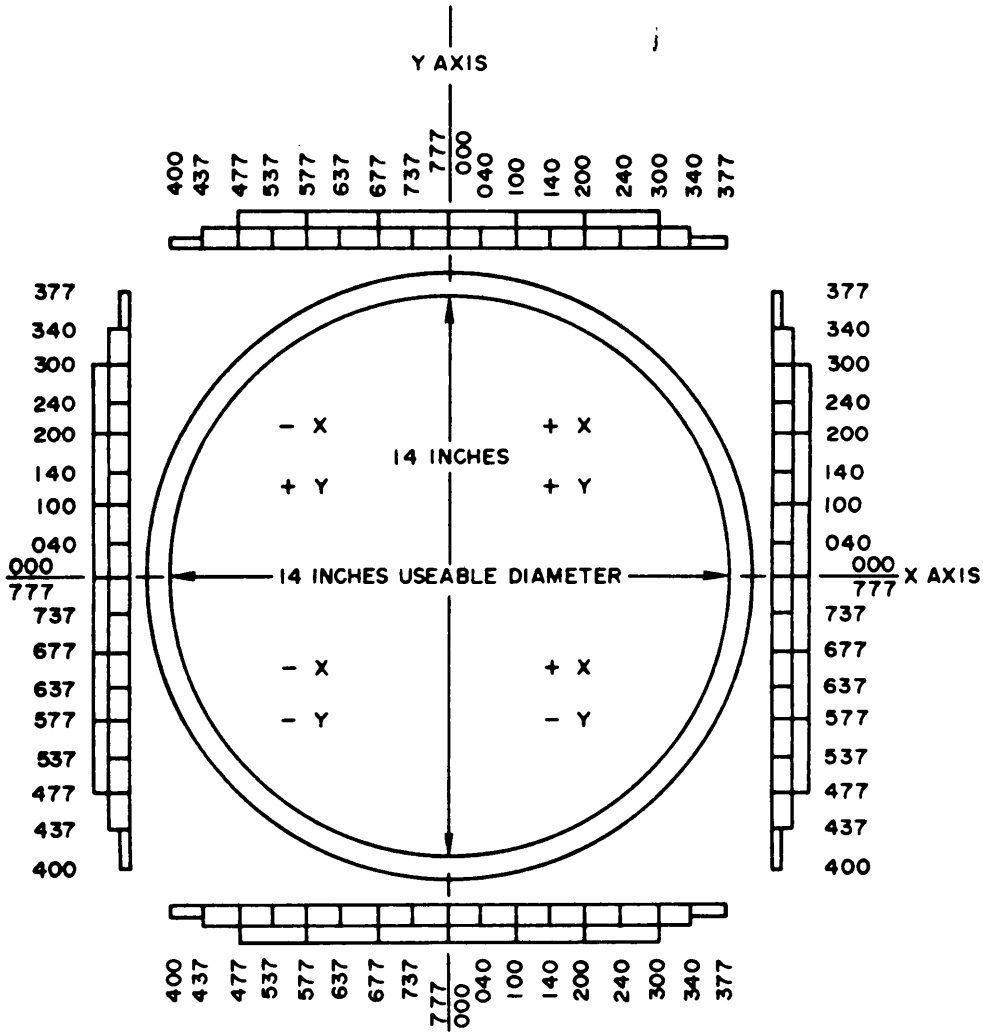


Figure 94. Multipurpose Display Screen and Octal Count of Various Positions

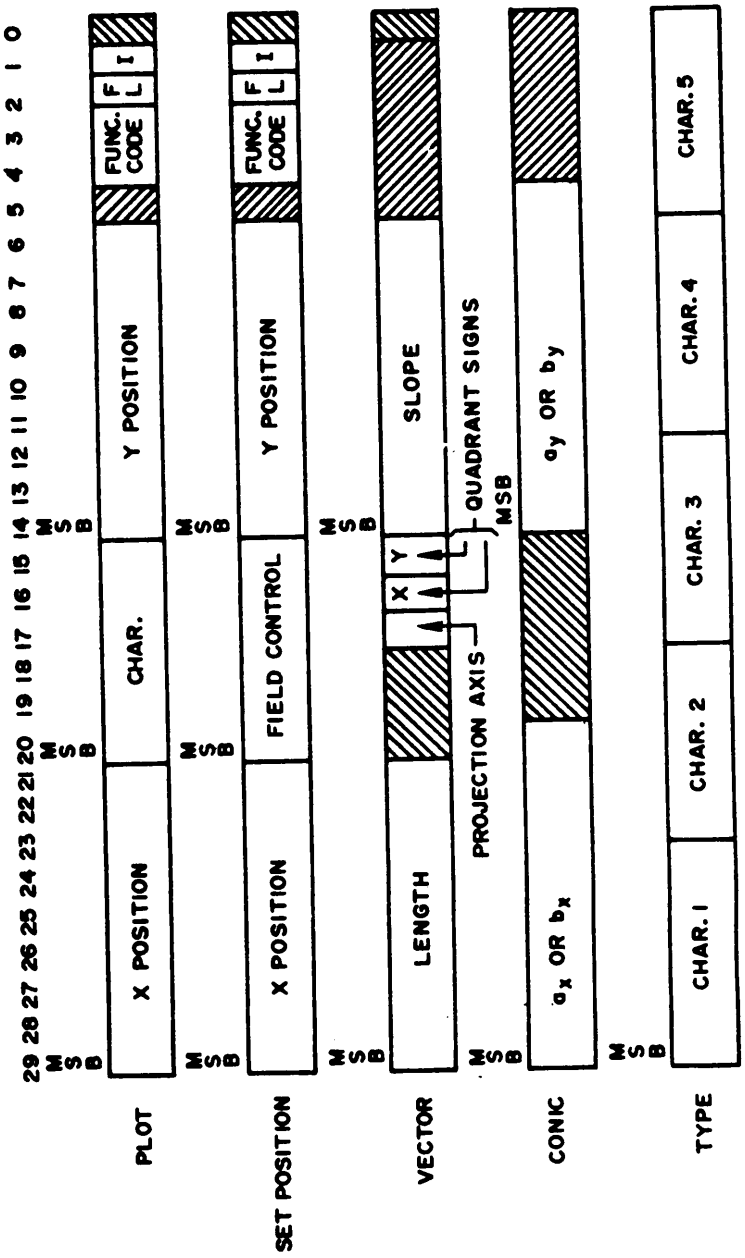


Figure 95. Format of Output Word from Computer to Multipurpose Display Logic

CODE	CHARACTER
00	BLANK
01	1
02	2
03	3
04	4
05	5
06	6
07	7
10	8
11	9
12	0
13	-
14	T
15	V
16	E
17	M
20	R
21	I
22	P
23	C
24	L

CODE	CHARACTER
25	J
26	D
27	+
30	S
31	B
32	⊠
33	△
34	⊙
35	⊕
36	⊙
37	O
40	D
41	□
42	N
43	)
44	2
45	✈
46	✈
47	✳
50	R
51	S

CODE	CHARACTER
52	A
53	B
54	C
55	E
56	F
57	G
60	H
61	I
62	J
63	K
64	L
65	M
66	P
67	Q
70	T
71	U
72	V
73	W
74	X
75	Y
76	Z
77	+

Figure 96; Characters to Be Displayed on Multipurpose Display and Corresponding Octal Codes

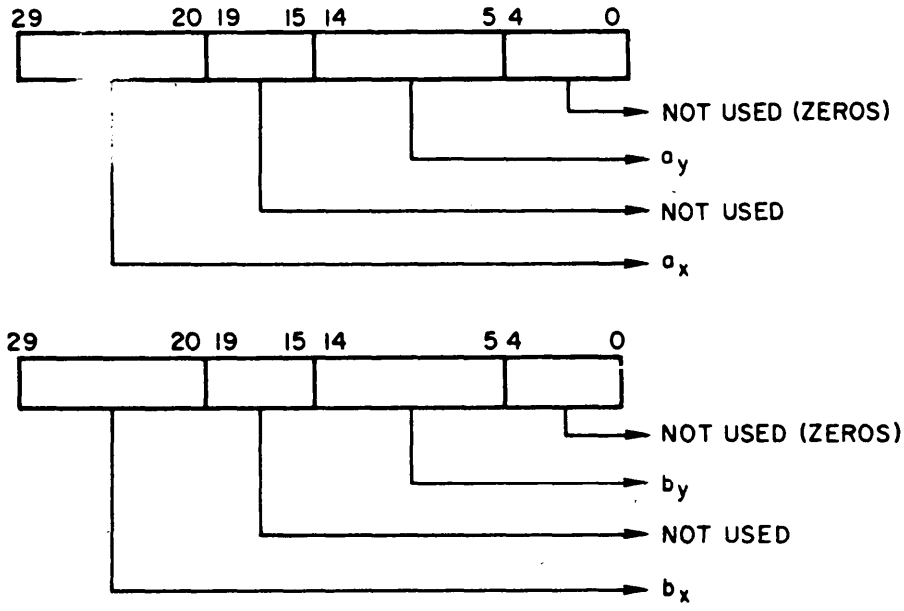


Figure 97. Format of Multipurpose Display Logic Conic Words

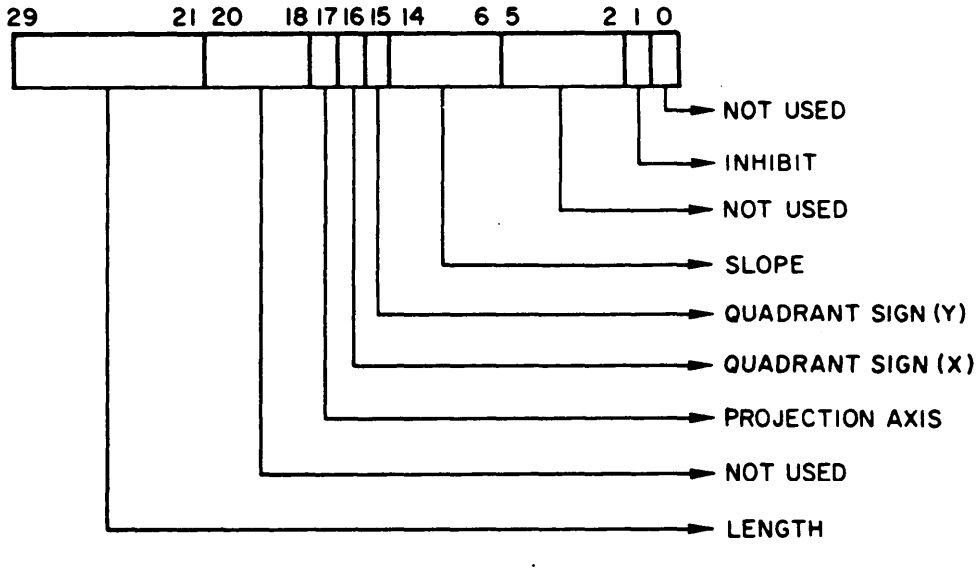
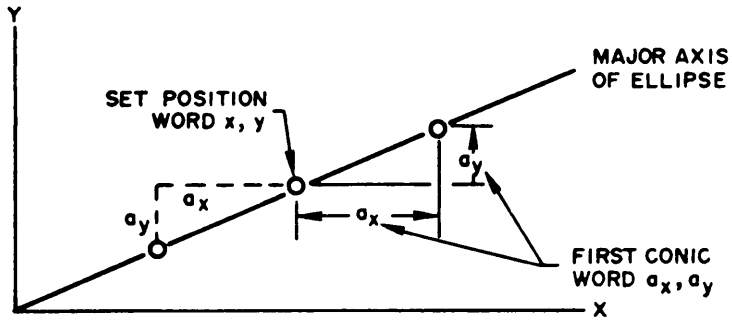
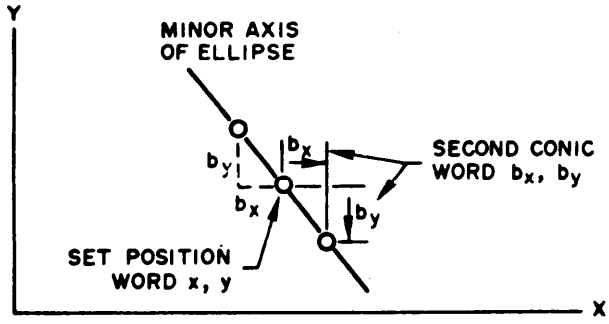


Figure 88. Format of Multipurpose Display Logic Vector Word





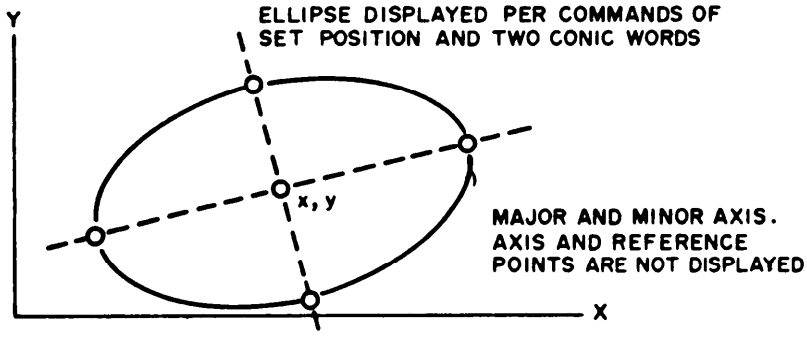


Figure 99. Multipurpose Display Conic Generation

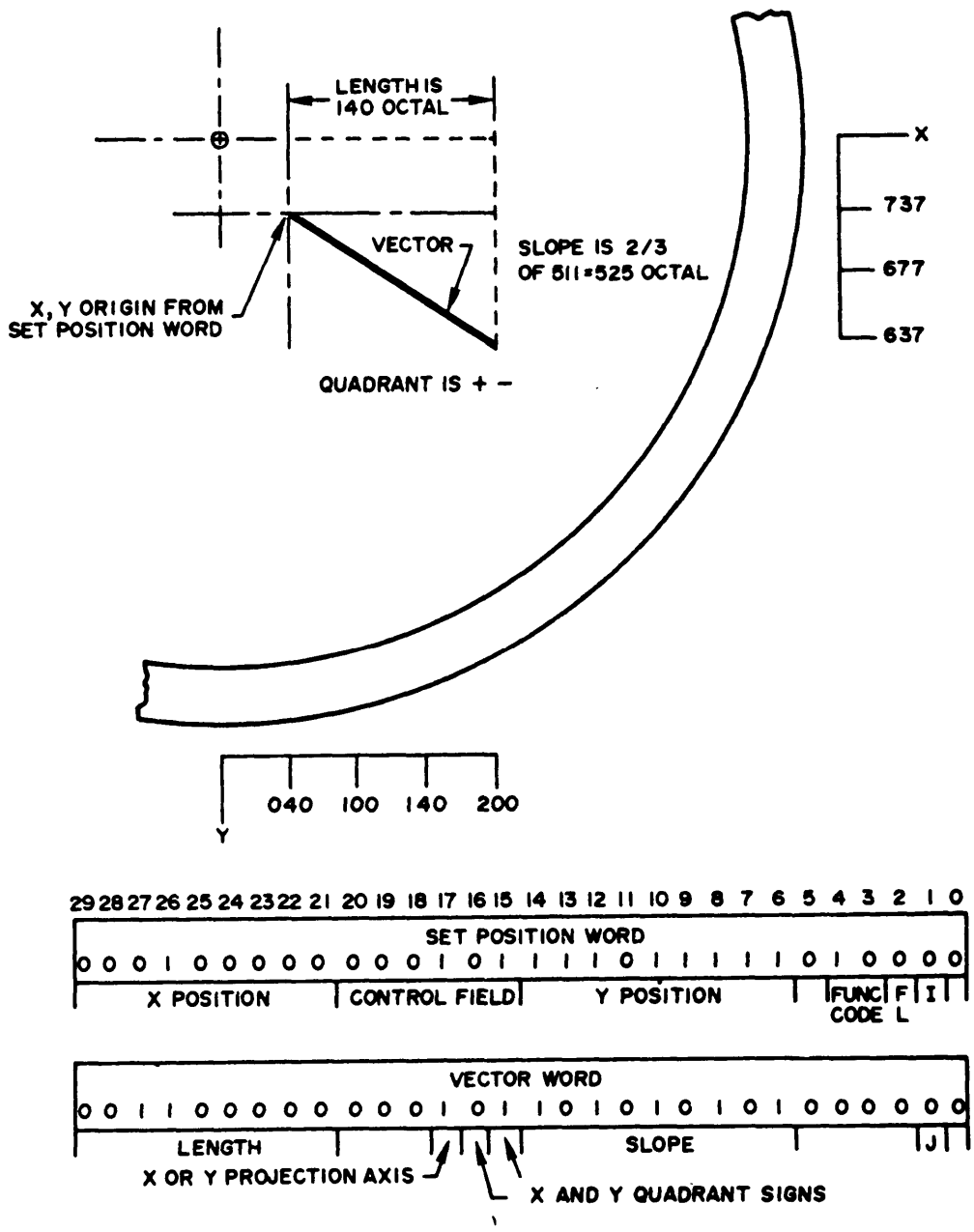


Figure 100. Multipurpose Display Vector Presentation

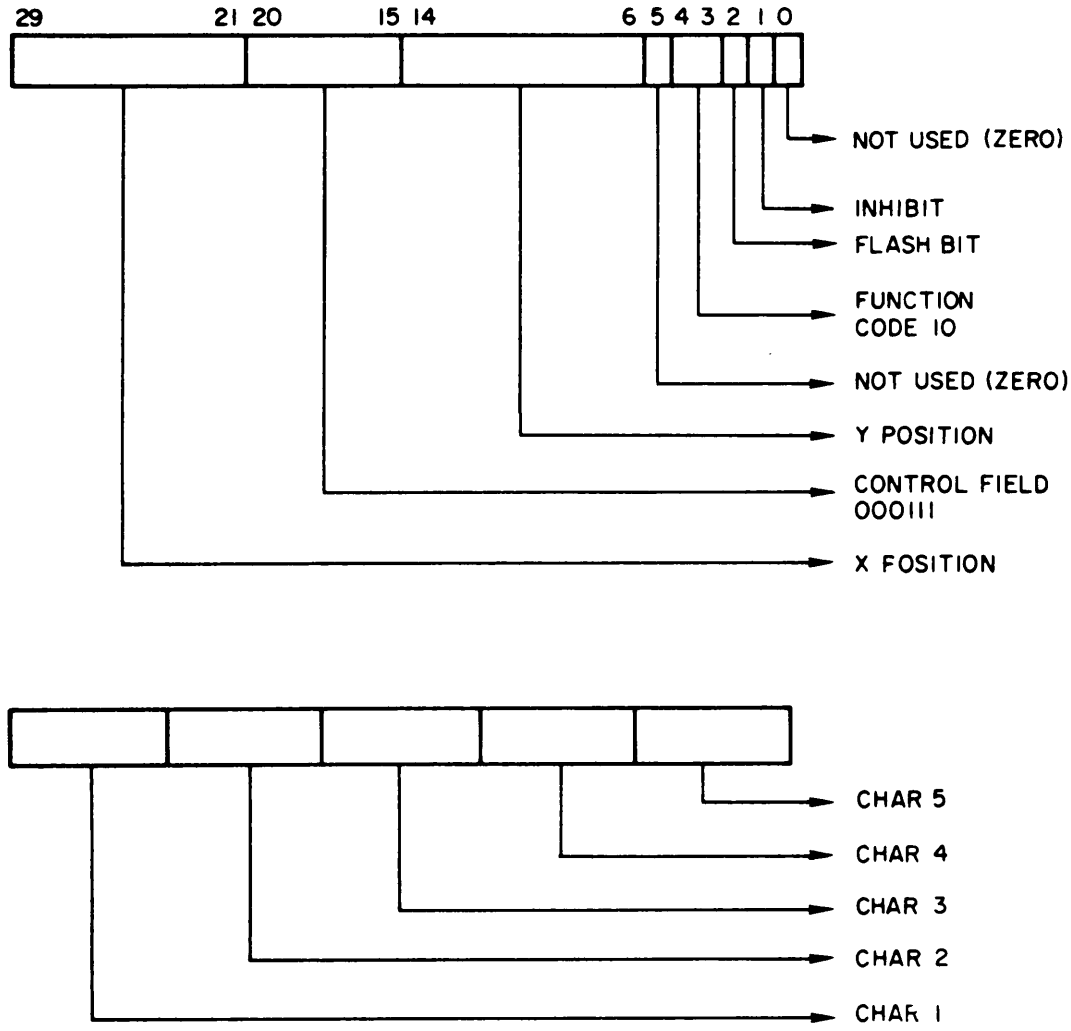


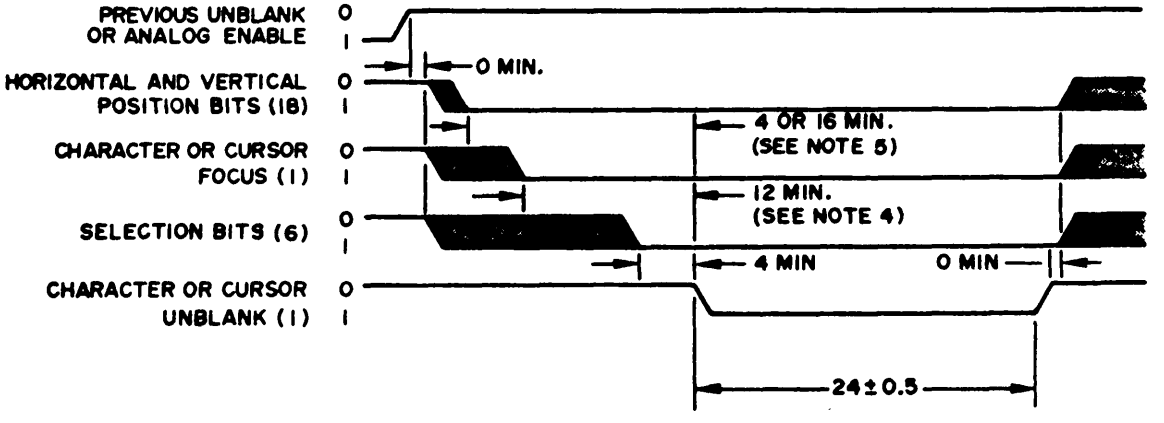
Figure 101. Multipurpose Display Logic Set Position Word with Control Field Code 07 (Short Type Mode) and the Five Character Sequence Which Follows

CODE	CHARACTER
00	BLANK
01	1
02	2
03	3
04	4
05	5
06	6
07	7
10	8
11	9
12	0
13	-
14	T
15	V
16	E
17	M
20	R
21	I
22	P
23	C
24	L

CODE	CHARACTER
25	J
26	D
27	
30	S
31	B
32	
33	
34	
35	
36	CARRIAGE RETURN
37	O
40	D
41	END OF MESSAGE
42	N
43	
44	
45	
46	
47	
50	R
51	S

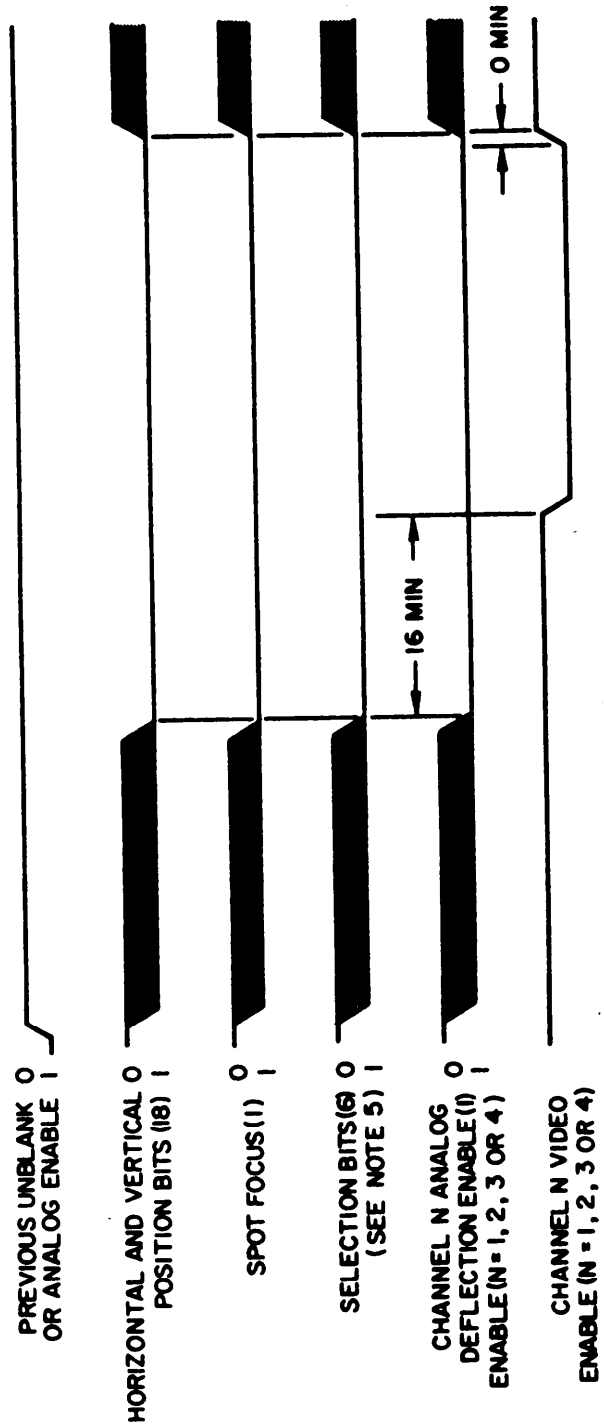
CODE	CHARACTER
52	A
53	B
54	C
55	E
56	F
57	G
60	H
61	I
62	J
63	K
64	L
65	M
66	P
67	Q
70	T
71	U
72	V
73	W
74	X
75	Y
76	Z
77	+

Figure 102. Charactron Set and Code for type Words



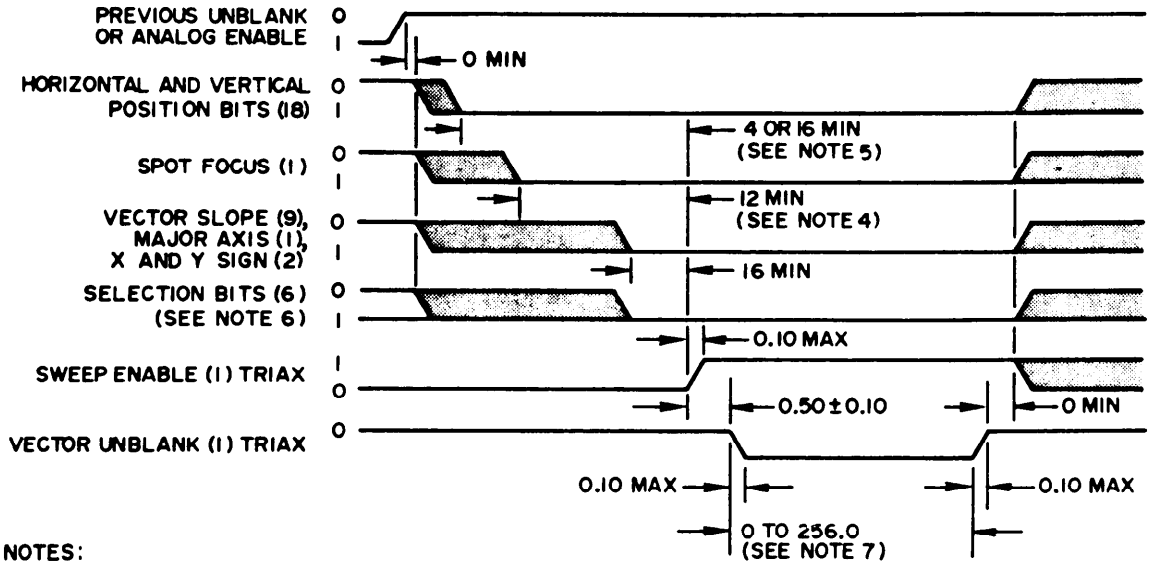
NOTES:
1. ALL TIMES ARE IN USEC.
2. RISE AND FALL TIMES 0.4 USEC MAXIMUM UNLESS OTHERWISE SPECIFIED.
3. SHADED REGIONS SHOW PERMISSIBLE TIMES FOR SIGNAL CHANGE.
4. 12 USEC REQUIRED ONLY AFTER FOCUS LINE FIRST COMES UP; IF ALREADY UP, NO SETTLING TIME REQUIRED.
5. 16 USEC REQUIRED WHENEVER X OR Y POSITION CHANGES MORE THAN 8 PLOT POSITIONS (8/512 OF DISPLAY DIAMETER); OTHERWISE 4 USEC REQUIRED.

Figure 103. Multipurpose Display Plot Mode Character or Cursor Timing



NOTES:
1. ALL TIMES ARE IN USEC.
2. RISE AND FALL TIMES 0.4 USEC MAXIMUM UNLESS OTHERWISE SPECIFIED.
3. SHADED REGIONS SHOW PERMISSIBLE TIMES FOR SIGNAL CHANGE.
4. SELECTION BITS DETERMINE CHARACTER WHICH IS FOCUSED TO A SPOT FOR DISPLAYING VIDEO. (CODE 00) SAME CHARACTER MUST ALWAYS BE USED.

Figure 104. Multipurpose Display Analog Channel Timing



NOTES:

1. ALL TIMES ARE IN USEC.
2. RISE AND FALL TIMES 0.4 USEC MAXIMUM UNLESS OTHERWISE SPECIFIED.
3. SHADED REGIONS SHOW PERMISSIBLE TIMES FOR SIGNAL CHANGE.
4. 12 USEC REQUIRED ONLY AFTER FOCUS LINE FIRST COMES UP; IF ALREADY UP, NO TIME REQUIRED.
5. 16 USEC REQUIRED WHENEVER X OR Y POSITION CHANGES MORE THAN 8 PLOT POSITIONS (8/512 OF DISPLAY DIAMETER); OTHERWISE 4 USEC REQUIRED.
6. SELECTION BITS DETERMINE CHARACTER WHICH IS FOCUSED TO A SPOT WHICH WRITES VECTOR. (CODE 00 IS SPECIFIED. SAME CHARACTER MUST ALWAYS BE USED.)
7. UNBLANK PULSE DETERMINES LENGTH OF MAJOR AXIS PROJECTION OF VECTOR.
8. TOLERANCE ON VECTOR UNBLANK AND SWEEP ENABLE SHOULD BE ±0.250 USEC.

Figure 105. Multipurpose Display Vector Timing

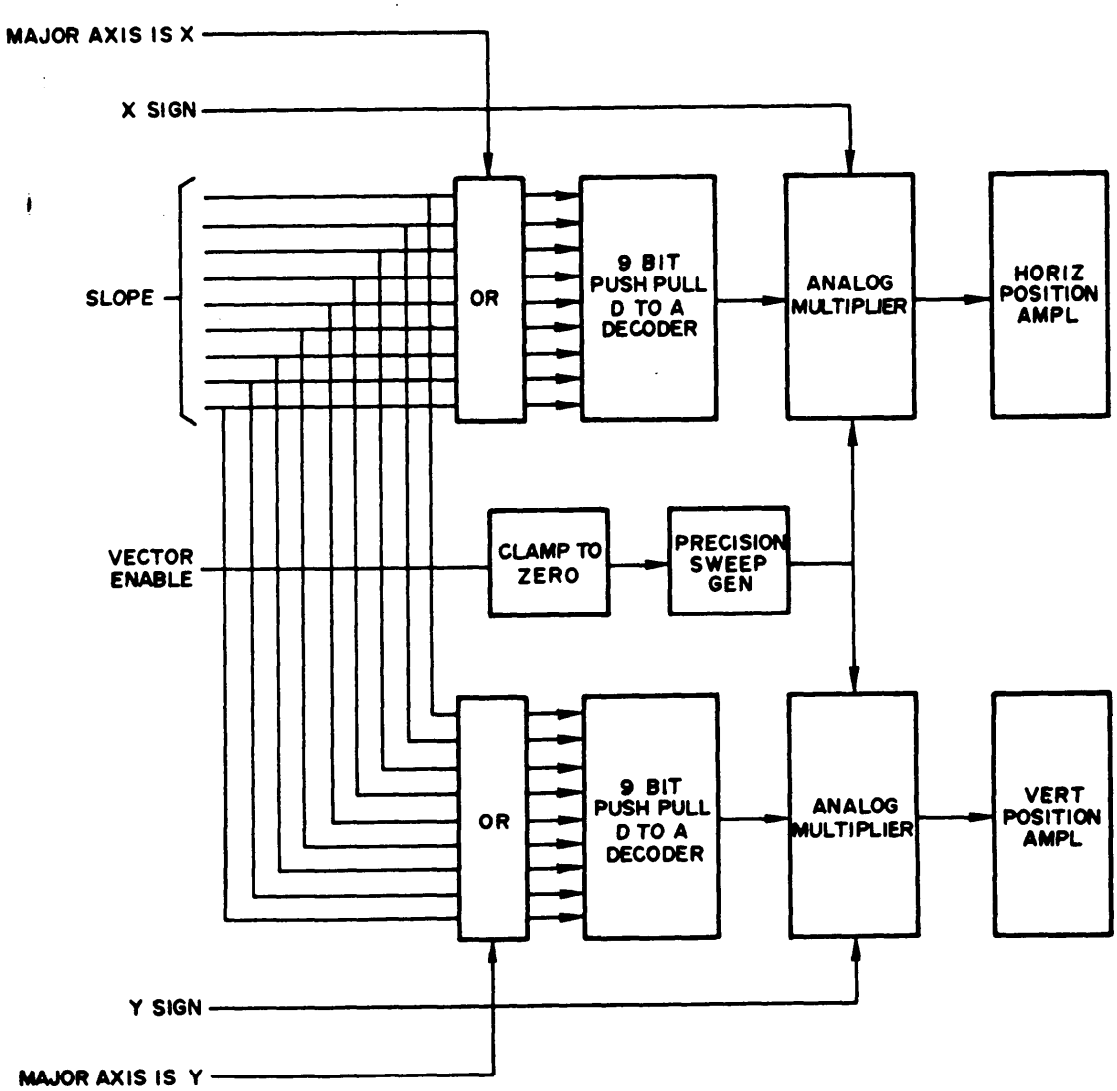


Figure 106. Multipurpose Display Vector Generator Block Diagram

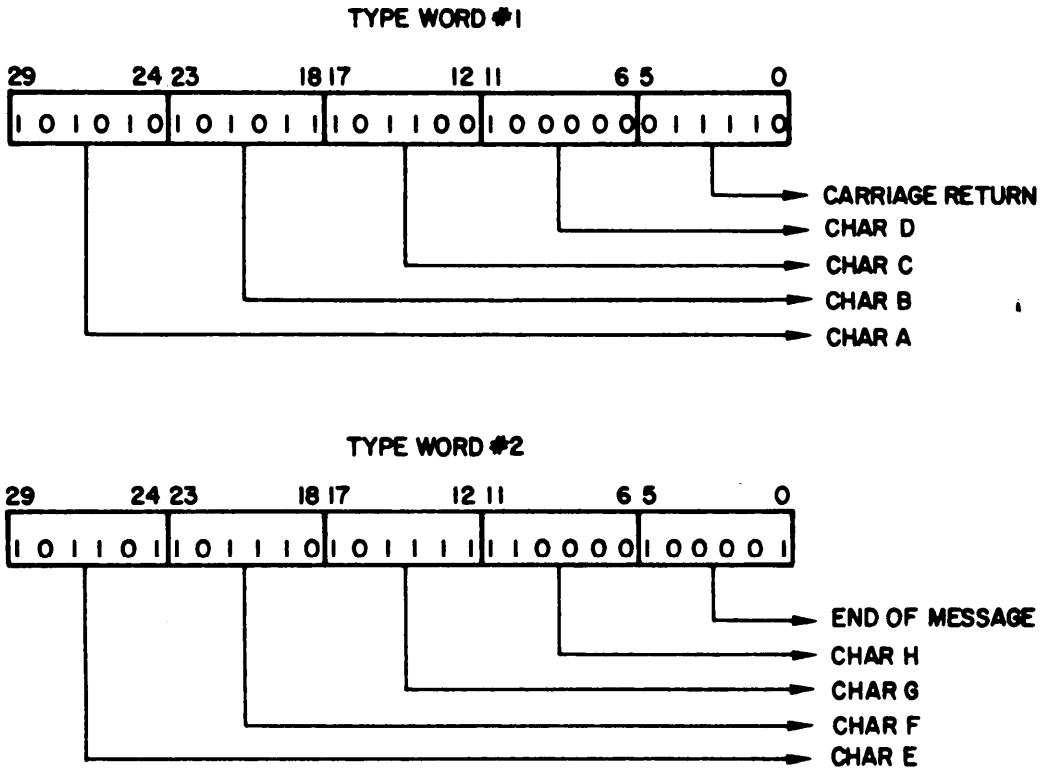


Figure 107. Sequence of Words from set Position Word (Control Field 06) to Present Type Series ABCD, EFGH

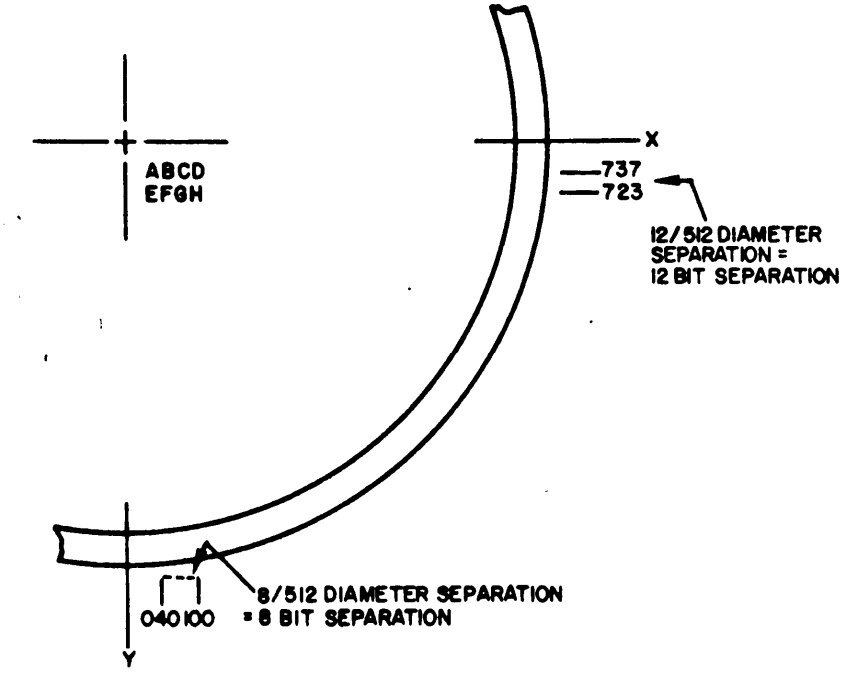


Figure 108. Multipurpose Display Character Presentation on Expanded Scale

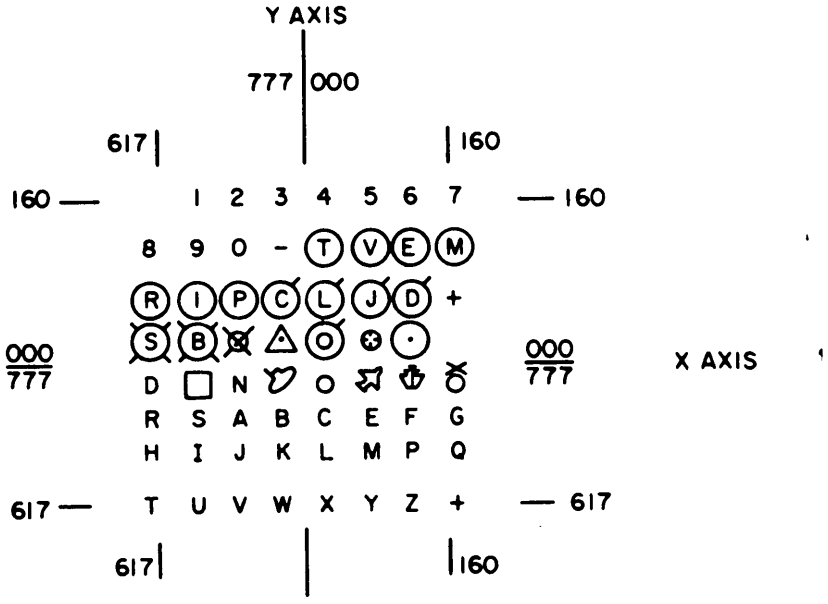


Figure 109. Multipurpose Display Matrix Test Pattern

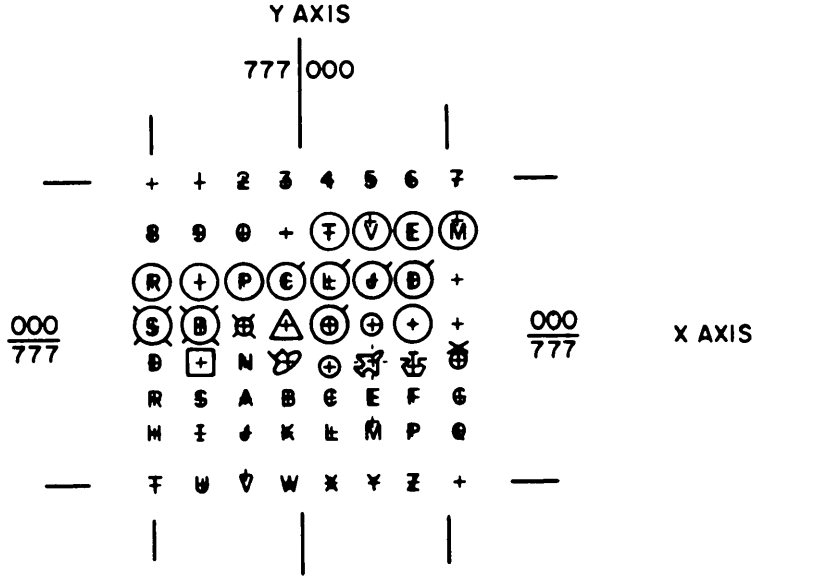


Figure 110. Multipurpose Displa Registration Test Pattern

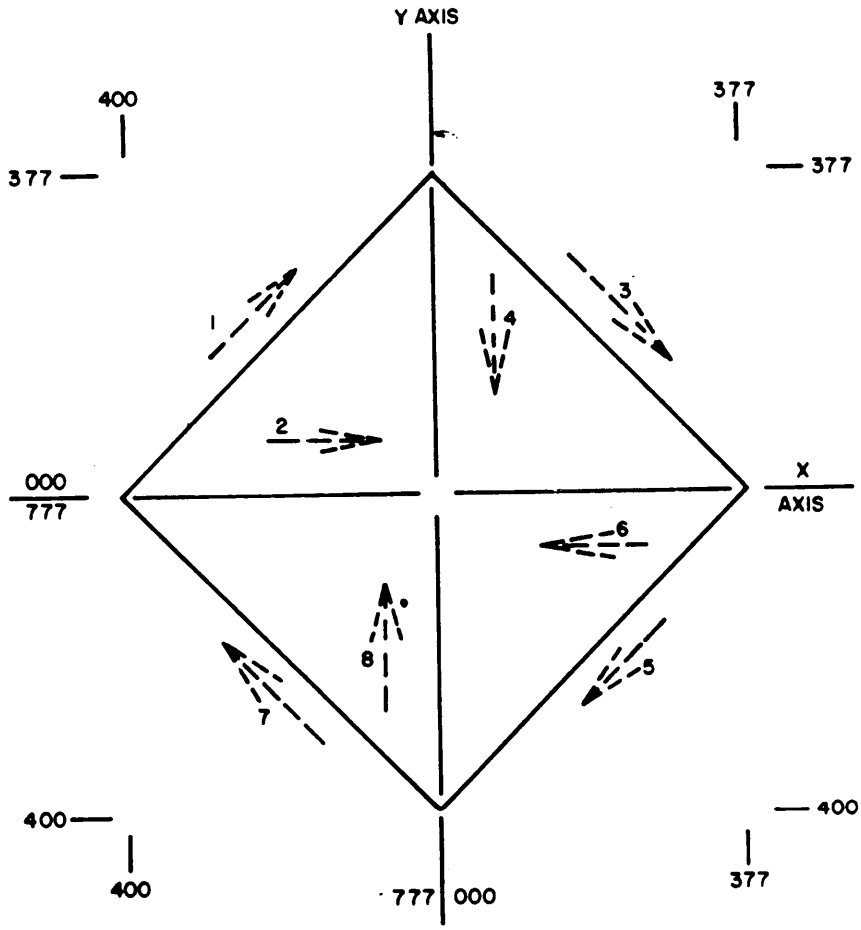


Figure 111. Multipurpose Display Vector Test Pattern

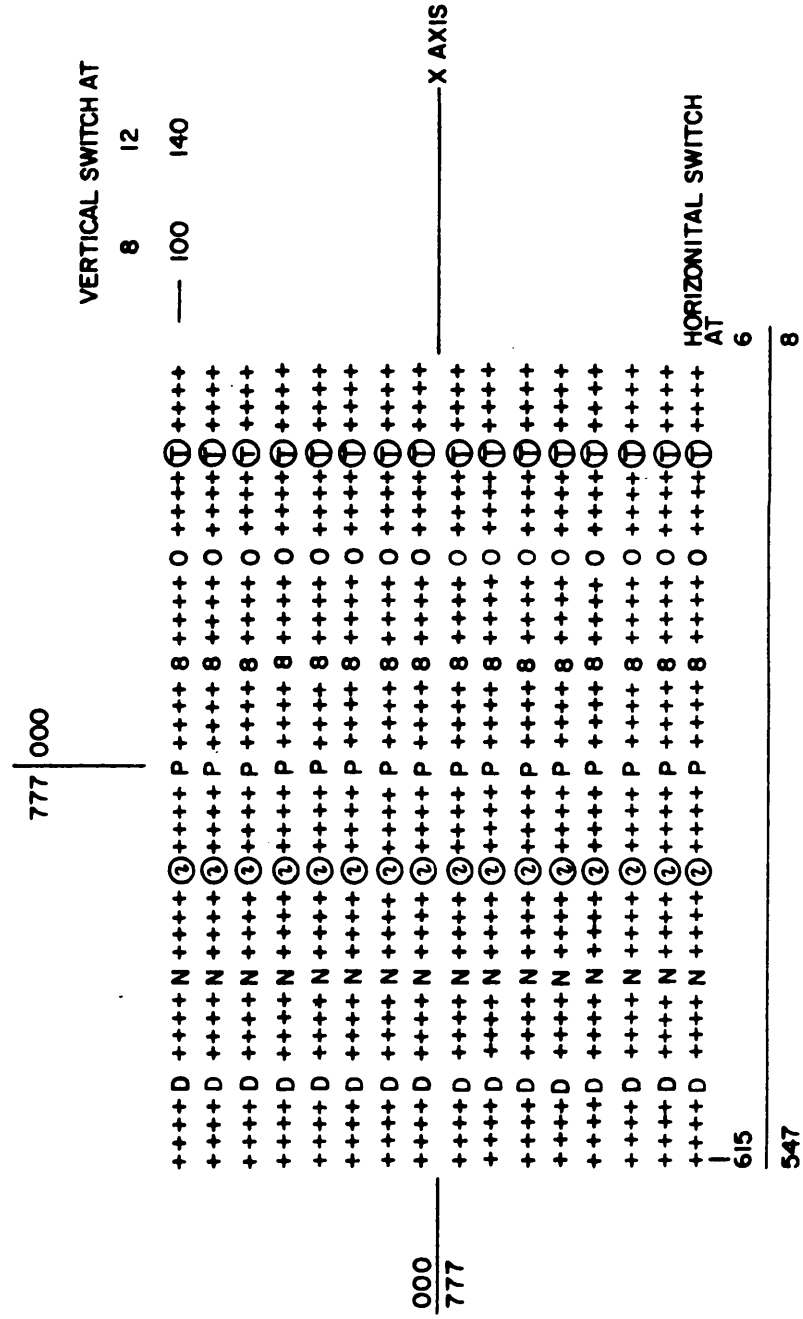


Figure 112. Multipurpose Display Type Test Pattern

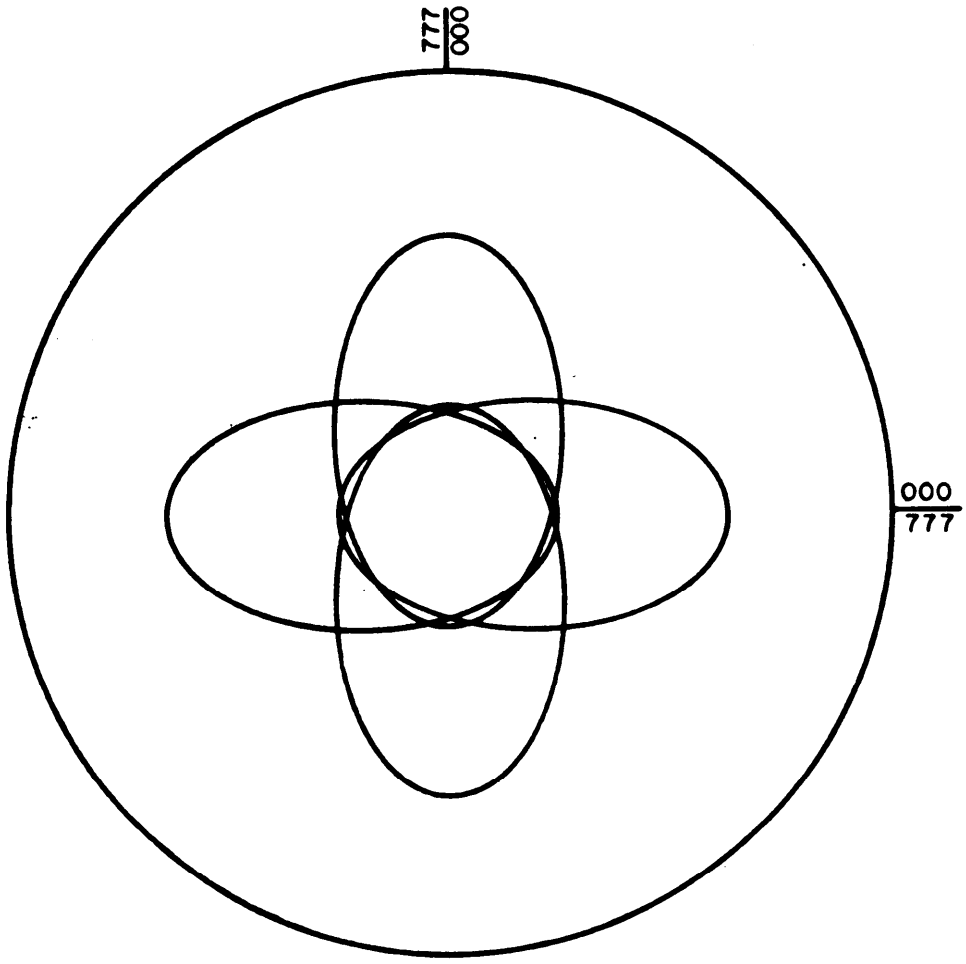


Figure 113. Multipurpose Display Conic Test Pattern

3.5.3.4.2 Pilot Display Logic

3.5.3.4.2.1 Functional Description - This subunit provides the interface between the computer and the Pilot Display. Under computer command, the Pilot Display Logic (PDL) provides timing,- control, deflection and vldeo signals to control the presentation of functional data on the CRT of the Pilot Display.

Figure 114 is a functional flow diagram for the PDL.

3.5.3.4.2.2 General Description

3.5.3.4.2.2.1 Presentation Repertoire -The PDL shall allow the computer to control the presentation of data on the Pilot's Display. Figure 115 shows the Pilot Display and x and y coordinate system in octal code. The data displayed is given in the paragraphs that follow:

(1) Aircraft Symbol with Azimuth Vector - The aircraft symbol to be used shall be selected from the available mode 02 symbols of the Character Generator. (See Figure 116). An azimuth vector is generated under computer control and has the origin at the center of the aircraft symbol. The Set Position word (Figure 119) specifies the aircraft position. The ax and a components of the Azimuth Vector word (Figure 121) determine the vector azimuth angle. (See Figure 117). This vector shall always have a 4 inch programmed length, but only 1/2 inch of the vector is unblanked.

(2) Fly-to-Points - A fly-to-point Shall consist of a dot with one or two adjacent alphanumeric characters, e. g., 31.

(3) Vectors - Vector origin, magnitude, and direction are controlled by the computer. All vectors are centered about the X, Y coordinate contained in the Set Position word. The magnitude and direction of the vector are defined by the a_x and a_y components of the Vector word, (Figure 121).

(4) Circles - Circle origin and radius are controlled by the computer. The origin of the circle is defined by the X, Y coordinate contained in the Set Position word. The radius of the circle is defined by the a_x and a_y components of the Circle word! Figure 122.

(5) Character Repertoire - The Character Generator shall have a full nonambiguous alphanumeric capability with eight special symbols. The codes for alphanumeric characters shall correspond to those shown in Figure 116. The characters presented on the display shall be controlled by the computer.

(6) Flashing Character - A selected symbol or group of characters may be caused to flash on the CRT under control of a 1 Hz signal from the Master Timing Logic (MTL) (this signal shall be referred to as the Flash signal).

(7) Tabular Information Display - An unlimited number of characters, contained in Character words (Figure 120), may be displayed starting at the X, Y coordinate defined in the Set Position word. This multi- character message shall be terminated by the receipt at the Pilot Display Logic of a new Set Position word.

3.5.3.4.2.2.2 Timing - The following tabulation specifies the maximum generation time for the various display functions. The generation time initiates at the trailing edge of the second computer Output Acknowledge signal and terminates at the next Output Data Request signal. The execution times in the following tabulation are based upon a character writing time of 166.6 microseconds and a 15 KHz low pass filter stabilization time of 240 microseconds maximum. The 166.6 microsecond character writing time is specified in order to enable synchronization of Character Generator control signals and provide a frequency compatible with 12 KHz sine wave for generation of vectors and circles.

The computer shall refresh the Pilot Display, via the Pilot Display Logic at a 40 Hz frame rate. The logic shall cease its request for data from the computer upon

receipt of an End of Data (EOD) code from the computer (last word in the display buffer). It shall resume requests for data upon receipt of the 40 Hz sync signal from the MTL via the MCP. The time between requests for sequential output data shall be in accordance with the timing constraints in the following table. Computer output timing shall be as described for Normal Output Data in Appendix I.

MAXIMUM OPERATION TIMES PER WORD

Operation	Execution Time
Positioning	24 µ sec nominal
Circle	550 µ sec maximum
Vector	550 µ sec maximum
Character (regardless of mode)	380 µ sec maximum
End of Data	5 µ sec maximum
No Operation	5 µ sec maximum

3.5.3.4.2.3 Operating Requirements - The following is a description of the operational requirements of the PDL.

3.5.3.4.2.3.1 Data Transmission - The PDL shall indicate its readiness to accept data by means of the ODR line being set. Data is of several categories and thus has unique timing controls for the various modes of operation. Typically, data shall be transmitted in two sequential words:

(1) First Transmission -

(a) Four bits denoting Set Position Mode

(b) Two eight-bit fields containing X and Y positioning

(2) Second Transmission -

(a) Four bits denoting Operation Mode

(b) Two nine-bit fields containing Command Word Data

3.5.3.4.2.3.2 Function Codes - There are four general types of Function Codes:

(1) Set Position Word - Two eight-bit one's complement fields for X and Y position.

(2) Circle Plot Word - Two eight-bit fields denoting the circle radius.

(3) Vector or Azimuth Vector Word - Two nine-bit one's complement field X and Y vector components.

(4) Character Plot Word - Two six-bit fields employed to specify two characters.

3.5.3.4.2.3.3 Diagnostics - The PDL shall provide diagnostic data which shall be initiated by a Diagnostic Instruction word from the computer via the MTL.

3.5.3.4.2.3.4 Character Generator - The character generator shall utilize the dot method to generate 47 possible characters. A six-bit counter shall generate a pattern of 8 by 8 dot positions through the use of two three-bit D/A converters. The six-bit counter also generates

timing pulses, which when gated through fixed wired character select gates, enable the video signal to select a desired dot in the pattern. The selected dots comprise the desired character. Figure 118 illustrates the dot method of character generation.

3.5.3.4.2.3.5 Display Synchronization - A 40 Hz synchronization (Sync) pulse from the MTL shall synchronously initiate the PDL in order to insure a jitter free display. When this occurs the logic shall transmit an ODR to the computer, which will respond with a data word to the PDL. Normal operation continues until an EOD, at which time the ODR remains low until the next cycle of the 40 Hz sync.

3.5.3.4.2.3.6 Circle and Vector Generation - Circle and Vector Generation is performed by logically controlling the phase and amplitude of the X and Y output signals. A sine-cosine generator provides a 12 KHz modulation source which operates in conjunction with the X and Y conic D/A converters to obtain amplitude modulated square waves. Square wave signals are then passed through low-pass filters to obtain amplitude modulated sinusoidal functions.

3.5.3.4.2.3.7 Type Mode - The PDL shall generate, under computer control, a sequence of characters which shall represent a typewriter page. This mode of operation shall require the computer to generate a series of code 04 words, each word consisting of two character codes. The PDL shall automatically increment its X Gross Position Register such that the characters are on 1/4 inch spacing. The incrementing shall continue until the computer sends a new Set Position word or EOD word. If the computer fails to terminate the X deflection incrementing, the PDL shall automatically cease incrementing when the X gross position register reaches its maximum deflection state.

3.5.3.4.2.3.8 Test Modes - The PDL operation shall be verified by utilizing the MCP for synthesis of various computer command words. The MCP shall provide simulated computer output words in three different operating modes:

(1) Single - The MCP shall transmit a manually programmed one output word when the operator depresses a momentary switch.

(2) Repetitive - The MCP shall continuously transmit a manually programmed word at the PDL's maximum rate for the function specified in the data word.

(3) Synchronous - The MCP shall output a manually programmed word at a fixed rate of 40 Hz which shall be locked to the 400 Hz line.

3.5.3.4.2.4 Interface Requirements - See functional flow diagram, Figure 114.

3.5.3.4.2.4.1 General

3.5.3.4.2.4.1.1 Master Timing Logic and Maintenance Control Panel to Pilot Display Logic - The PDL shall receive inputs from the MTL and the MCP.

3.5.3.4.2.4.1.1.1 Master Timing Logic to Pilot Display Logic - The MTL shall continuously transmit to the PDL, the 40 Hz sync via the MCP and 1 Hz Flash signal as defined in the MTL Section, 3.5.3.4.4.2.1.2.7. In addition, the PDL shall receive 1.536 MHz clock from the MTL and six lines of diagnostic instruction.

3.5.3.4.2.4.1.1.2 Maintenance Control Panel to Pilot Display Logic - The PDL receives data words, the Output Acknowledge signal, 40 Hz sync and switch closure lines from the MCP.

(1) Data - Data words which are received from the computer via the MCP shall command the timing, control, deflection, and video signals for the PDL. These signals will be a 30-bit data word, and shall adhere to the word formats shown in Figures 119 through 122.

(2) Output Acknowledge - The Output Acknowledge signal indicates that data on the data lines is ready for sampling by the PDL.

(3) Test Switch - The Test Switch closure lines provide instructions to the PDL to perform the tests as described in 3.5.3.4.2.3.8.

3.5.3.4.2.4.1.2 Pilot Display Logic to Maintenance Control Panel, Pilot Display and Master Timing Logic - The PDL shall transmit signals to the MCP, Pilot Display, and Master Timing Logic.

3.5.3.4.2.4.1.2.1 Pilot Display Logic to Maintenance Control Panel - The PDL shall transmit an Output Data Request to the MCP. This signal shall be compatible with the PDL and the computer requirements described in Appendix I.

3.5.3.4.2.4.1.2.2 Pilot Display Logic to Pilot Display

(1) "X" and "Y" Full Scale Deflection - Circuitry in the PDL shall be capable of accepting digital data that describes positions, straight lines, circles, and characters. This data shall generate waveforms which shall be transmitted to the horizontal and vertical deflection circuits of the Pilot Display. The signal level will be from 0 to between ± 6 to ± 8 volts peak amplitude for a beam deflection of one radius. Step setting time for the Pilot Display shall be no greater than 18 µsec for full screen deflection. The sinusoidal signals for vector and circle functions shall be 12 KHz, and character deflection axis bandwidth products shall be 110 KHz minimum.

Circuits shall be provided in the PDL that shall limit the summation of the character signals, sinusoidal signals, and positioning signals from exceeding one display radius along any coordinate axis in order to prevent overdriving the display deflection amplifiers. Limiting of the maximum allowable X and Y deflection signals shall be at X and Y deflection amplitude values of +6 to +8 V +10% -0%.

(a) Accuracy Under Nominal Conditions - Nominal conditions are defined as the temperature range of 10°C to 40°C, and the range of input power within the bounds of Limits 2 and 3 of Figure 3, MIL-STD-704 as modified by 3.3.12.1. Accuracies under these conditions shall be as follows:

1. The X and Y total harmonic distortion of the sinusoidal conic generation signals shall be less than 1%.

2. The phase difference between X and Y sinusoidal conic generation signals shall be less than one degree.

3. A change in the digital signal shall produce a corresponding change in the analog signal within one LSB.

4. The magnitude accuracy of X relative to Y shall be less than +1%.

5. The absolute accuracy of X or Y shall be less than +2%* "

(b) Accuracy Under Extreme Conditions - Extreme conditions shall be as defined in 3.3.10. Accuracies under these conditions shall be as fillows:

1. The X or Y total harmonic distortion of the sinusoidal conic generation signals shall be less than 2%.

2. The phase difference between the X and Y sinusoidal conic generation signals shall be less than 2.

3. A change in the digital signal shall produce a corresponding change in the analog signal within one LSB.

4. The magnitude accuracy of X relative to Y shall be less than ±2%.

5. The absolute accuracy of X or Y shall be less than +4%.

(2) "Z" Axis Video - Positive going video signals shall be DC coupled to the video amplifier of the Pilot Display for intensity modulation of the CRT. Video amplitude shall be proportional to writing speed.

(3) Unblank - The PDL shall provide a positive going voltage level to the Pilot Display for unblinking the CRT. The unblank signal shall have the same duration as the video signal, but shall have constant amplitude.

3.5..3 .4.2.4.1.2.3 Pilot Display Logic to Master Timing Logic - The PDL shall transmit diagnostic data to the MTL when required.

3.5.3 .4.2.4.2 Input/Output Signal Characteristics

3.5.3.4.2.4.2.1 Maintenance Control Panel and Master Timing - All internal signals between the PDL and the MCP and MTL shall be transmitted over single ended lines whose logical “0” = 0. 0 + 0.5, -0.0 volts and logical “1” = +5.0 +1.5 volts. -

3.5.3.4.2.4.2.2 Pilot Display - The PDL input/output signals to and from the Pilot’s Display shall be as follows:

3.5.3.4.2.4:2.2.1 Triaxial Transmissions - All signals to the Pilot Display shall be transmitted via Amphenol 421-033 cable or equivalent terminated in a differential amplifier whose input impedance shall be 90 to 95 ohms and 100 pf maximum. The coaxial cable shall not exceed 100 feet.

(1) X and Y Deflection Signals - The X and Y deflection signal characteristics shall be as described in 3.5.3.4.2.4.1.2.2(1). Transition times for gross positioning signals shall be less than 4.0 microseconds.

(2) "Z" Axis Video - This signal shall be positive going from 0 to between 2.0 to 2.5 volts peak. The video signal shall provide the following voltage levels in order to obtain uniform brightness on the CRT for conic and character generation.

(a) Conic

Video voltage +5%	% Maximum radius displayed
50% X Maximum voltage	O - 25%
65% X Maximum voltage	26- 50%
80% X Maximum voltage	51- 75%
Maximum voltage	76- 100%

(b) Character

Character Video Voltage = 50%x Max. Voltage ±5%.

(3) Unblank - This signal shall be +5. 0 ±1.5 volts with a rise time and fall time not to exceed 100 nanoseconds when measured at the 10% and 90% amplitude points.

3.5.3.4.2.4.3 Word Formats - The Pilot Display Logic shall be capable of recognizing the digital display Instruction Word formats shown in Figures 119 through 122. All of these programming words shall be of 30 bit length, with bit "29" being the Most Significant Bit (MSB) and bit "0" being the Least Significant Bit (LSB). Not all of the data bits contained in the instruction word are used. In all words, bits 26 through 29 define the function code. The list of display actions defined by the various function codes is shown in the following table. The function codes 'are shown in octal code representation.

Function Code	Function Performed
00	No Operation
01	Set Position Location Beam
02	Print 1 character - No 2nd char.
03	Print 2 characters and Point
04	Print Characters - No Point (Type Format)
05	Display Vector
06	Display Azimuth Vector
07	Display Circle
10	EOD
12	Identical to MODE 02 but flashing
13	Identical to MODE 03 but flashing
14	Identical to MODE 04 but flashing

3.5.3.4.2.4.3.1 No Operation - Function Code 00 - When a word containing this code is received from the computer, the Pilot Display Logic shall inhibit the normal processing of the word and request a new computer word.

3.5.3.4.2.4.3.2 Set Position Word - Function Code 01 - The Set Position word, Figure 123, shall contain the X and Y components of the positioning data for all vectors, circles, and characters. The X compound is contained in bits 15 through 22, where bit 22 is the MSB and bit 15 the LSB. The Y component is contained in bits O through 7, where bit 7 is the MSB and Mt O the LSB. The eight binary bits of horizontal deflection data and eight binary bits of vertical deflection data shall be utilized to define a Cartesian coordinate system with the origin at the center of the display. All of the X and Y coordinate data shall be expressed in the one's complement system. The maximum positive deflection for the 7.6 inch usable diameter of the 9-inch diameter CRT is defined by 177 in the octal code; the maximum negative deflection is defined as 200 in the octal code (see Figure 115). The use of the eight binary bit magnitude in conjunction with the 8-inch usable CRT diameter provides a plotting position selection capability of approximately 0.0312 inch apart.

3.5.3.4.2.4.3.3 Character Word - A character word, Figure 120, shall contain one or two character data codes, C_1 and C_2, Plus the Character Function Code. The Character Function Code shall describe the manner in which this Character Word is to be processed. Character 2 shall be contained inhibits 15 through 20 where bit 20 is the MSB and bit 15 is the LSB. Character 2 shall be contained in bits 0 through 5, where bit 5 is the MSB and bit 0 is the LSB.

(1) Function Code (02) - This shall be a one character message pertaining only to special characters. A point shall first be plotted at the X, Y position contained in the previous positioning word, and one of the special characters shall then be drawn with its center at

this point. The second character shall always be blank in this mode of operation. Special characters shall be defined by codes 00, 13, 14, 15, 16, 17, 41 and 44.

(2) Function Code (03) - This shall be a one character word message which indicates a point is to be plotted at the X, Y position defined in the previous position word. The leading edge of the first character will be drawn 0.25 inch to the right of this point. When only the second character is to be displayed, its leading edge will be 0.5 inch from the point.

(3) Function Code (04) - This code shall signify that a multi-character message is to be processed (Type Format). The lower left hand corner of the initial character will be O. 25 inch to the right of the X, Y position defined in the previous positioning word, or previous word containing a Function Code 04.

3.5.3 .4.2.4.3.4 Vector Word - The Vector Word (Figure 121) shall contain the data necessary to define both the normal vector and azimuth vector. The X component of the vector is contained in bits 15 through 23, where bit 23 is the MSB and bit 15 is the LSB. The Y component is contained in bits O through 8, where bit 8 is the MSB, and bit 0 is the LSB.

(1) Function Code (05) - This code shall signify that the data accompanying the code shall define a vector. The center of the vector shall be defined by the X, Y coordinates contained in the previous word. Both ax and a_y shall be 9 bit, one's complement quantities. The LSB = 1/2 set position bit.

(2) Function Code (06) - This code shall be used when an aircraft heading vector is to be displayed. The X, Y coordinates contained in the previous word will be that of the aircraft. A four-inch vector whose angular orientation is that of the aircraft heading vector will be programmed in the accompanying data. The resultant displayed vector shall be one-half inch long, originating from the Aircraft Symbol, and extending in the programmed direction. A Function Code (06) can follow a Function Code (02) without regenerating a new Set Position word (Function Code (01)).

3.5.3.4.2.4.3.5 Circle Word -- Function Code (07) - The Circle word, Figure 126, shall contain the necessary data for defining a circle. The radius defining this circle shall be contained in bits O through 7 and 15 through 22, where bits 7 and 22 are the MSB's and bits O through 15 are the LSB's. This word shall specify a circle centered on the X, Y coordinates contained in the previous Positioning word. The radius in this word shall always be an eight-bit, positive quantity, where 377 in the octal code represents one display diameter. The binary equivalent for radius shall be identical in both halves of the data word.

3.5.3.4.2.4.3.6 End of Data Word - Function Code (10) - This code shall indicate the End of Data (EOD) from the compuer during a particular 25 millisecond frame. If the EOD word is not received, the Pilot Display, upon reinitialization, shall continue to display the remaining buffer information during the next 25 millisecond frame.

3.5.3.4.2.4.3.7 Flashing Character - Function Codes (12), (13), and (14) - Codes (12), (13), and (14) shall signify that all character data accompanying codes (02), (03), and (04), respectively, shall be displayed in the Flashing Mode. Flashing shall be accomplished by displaying the information for one-half second, and then preventing the display of this information for the next half second, by inhibiting the Z axis (video) output.

3.5.3.4.2.4.3.8 Character Size - The PDL shall provide controls which shall enable an operator to continuously vary the size of the characters displayed. Character height and width shall be continuously adjustable from 1/8 to 1/4 inch.

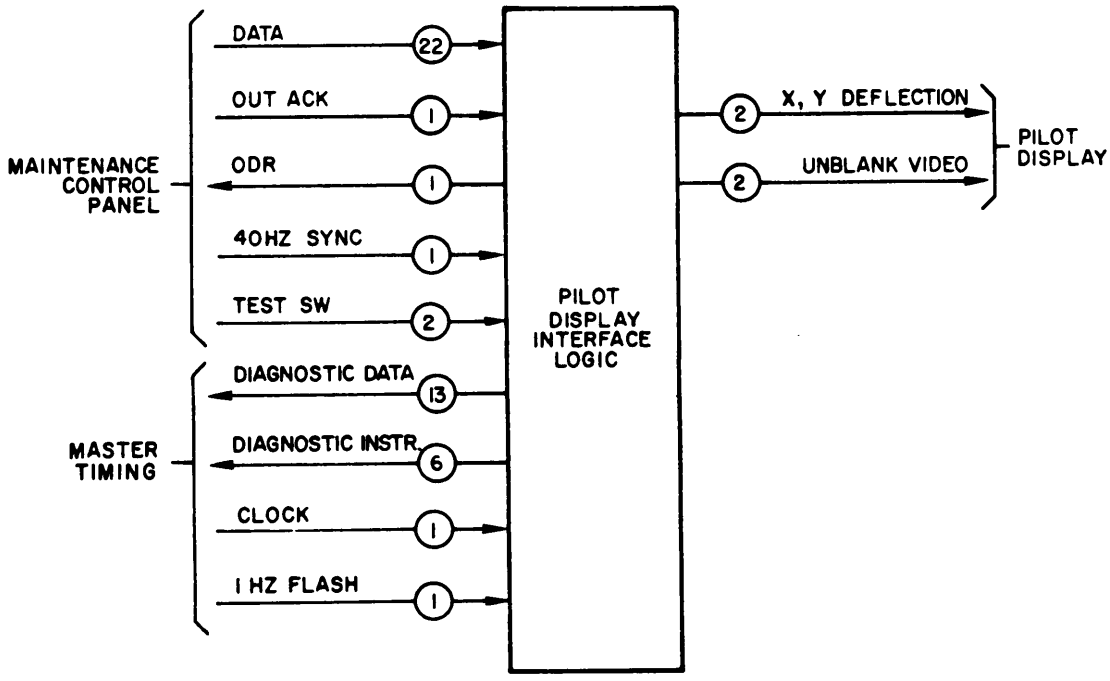


Figure 114. Pilot Display Logic, Functional Flow Diagram

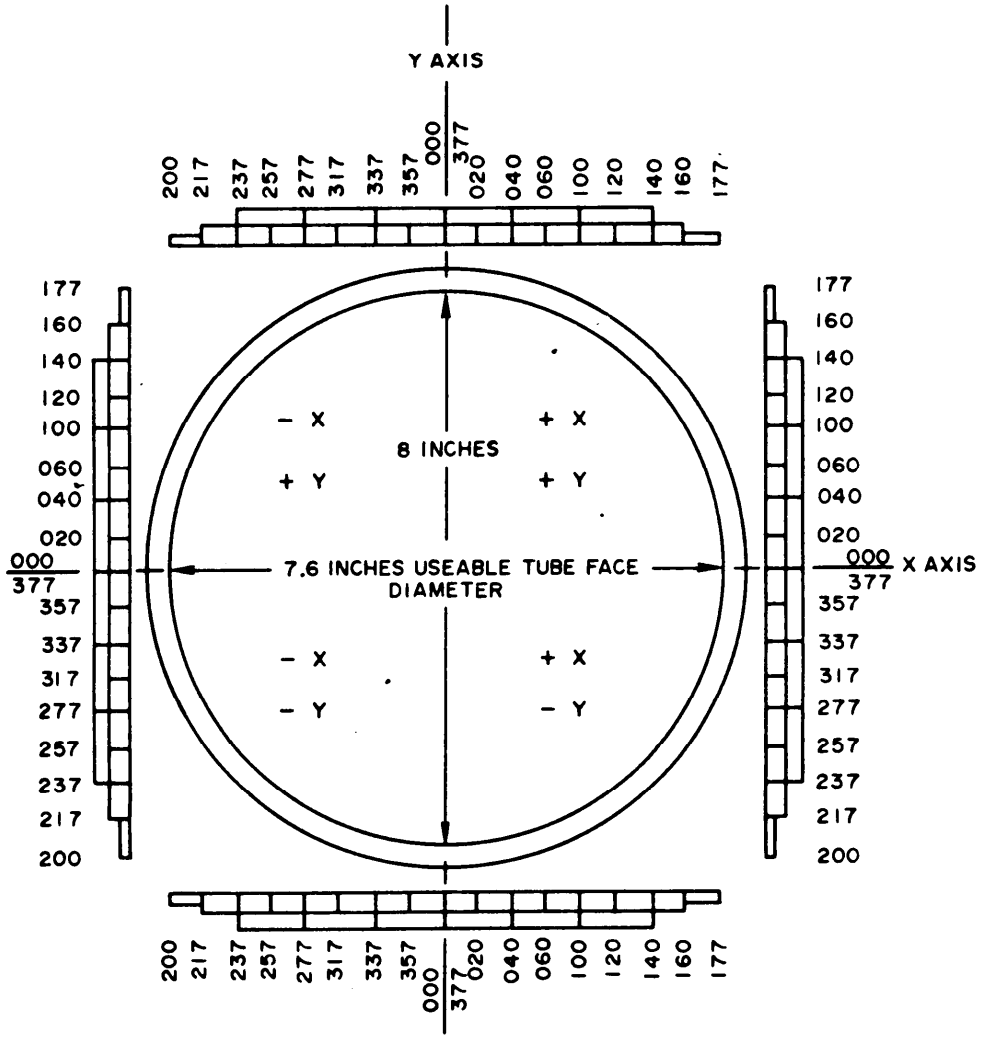


Figure 115. Pilot Display X and Y Coordinate System in Octal Code

CODE	CHAR
00	BLANK
01	1
02	2
03	3
04	4
05	5
06	6
07	7
10	8
11	9
12	0
13	–
14	⋈
15	⊠

CODE	CHAR
16	⊠
17	⊠
40	D
41	+
42	N
44	X
50	R
51	S
52	A
53	B
54	C
55	E
56	F
57	G
60	H

CODE	CHAR
61	I
62	J
63	K
64	L
65	M
66	P
67	Q
70	T
71	U
72	V
73	W
74	X
75	Y
76	Z
77	+

Figure 116. Pilot Display Character Repertoire

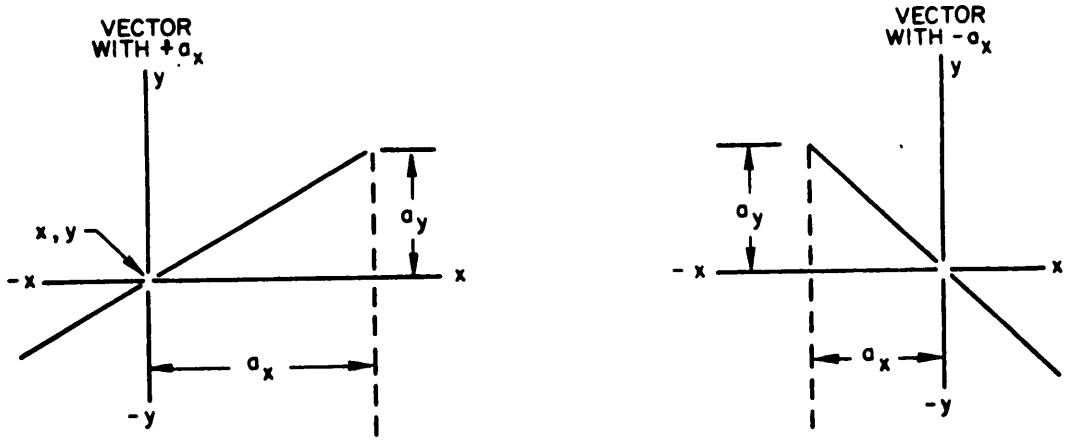


Figure 117. Vector Definitions

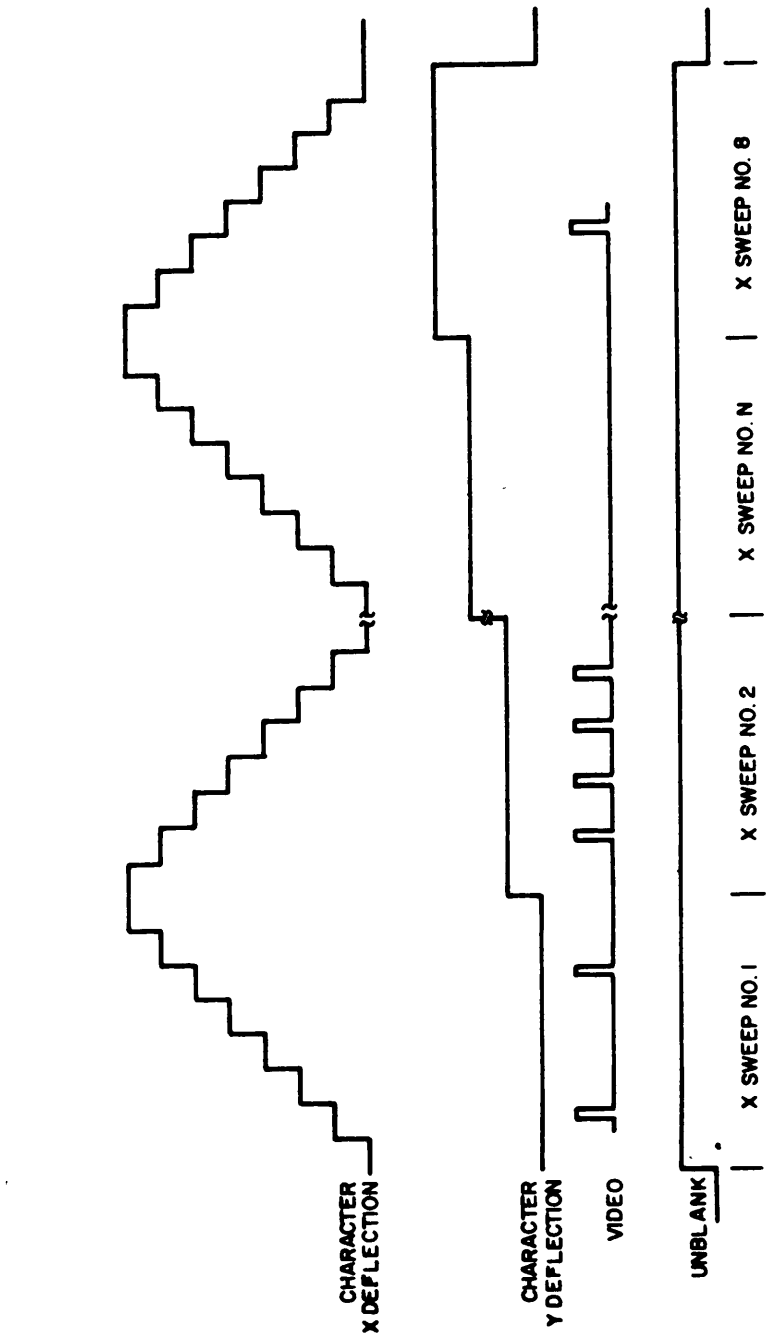


Figure 118. Dot Method of Character Generation

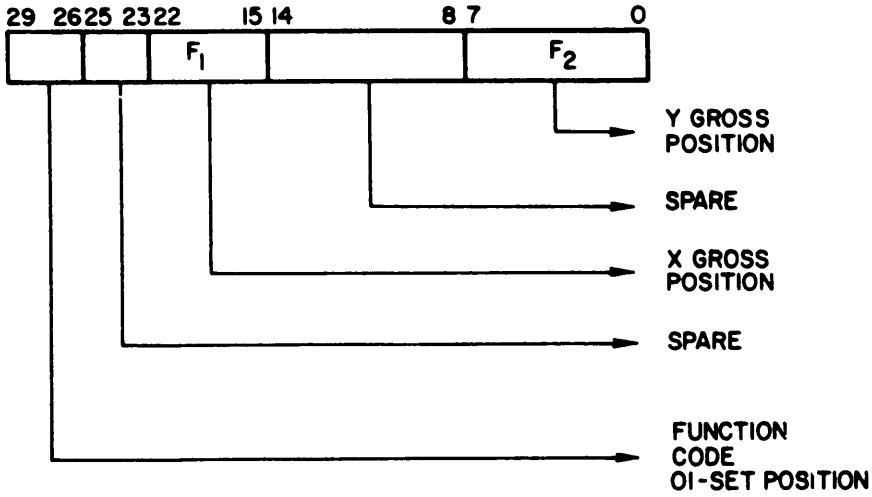


Figure 119. Format for Pilot Display Set Position WORD

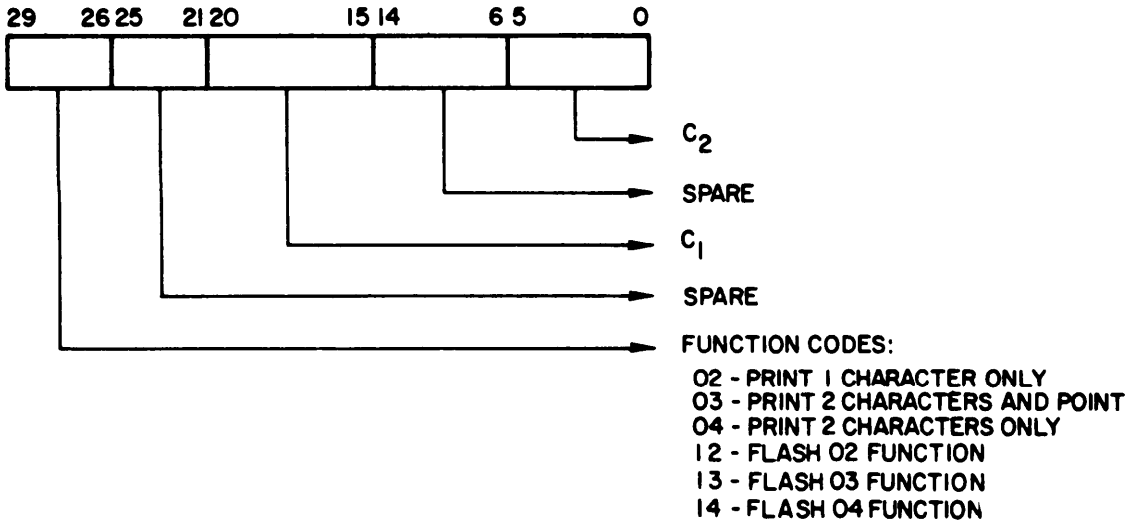


Figure 120. Format for Pilot Display Character Plot Word

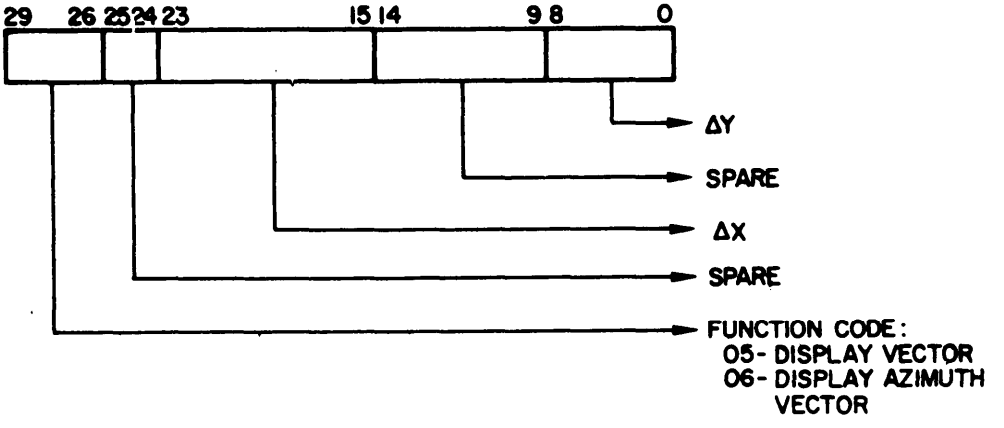


Figure 121. Format for Pilot Display Vector or Azimuth Vector Word

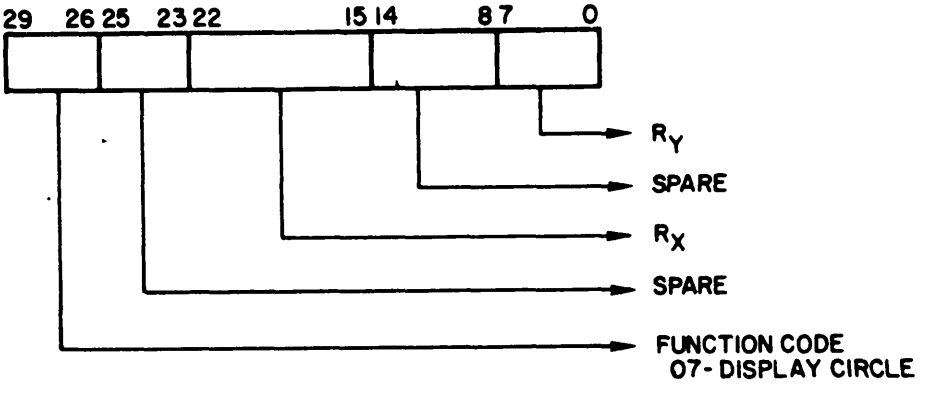


Figure 122. Format for Display Circle Plot Word

3.5.3.4.3 Function Generator Unit

3.5.3.4.3.1 Functional Description - The Function Generator Logic (FGL) shall accept computer generated digital information, and convert it to an analog form suitable for displaying conies on one of the Multipurpose Displays (MPD). The FGL shall process the computer data and generate the appropriate analog sinusoidal waves and unblank signal which result in the display of ellipses, circles, and vectors.

Figure 123 is a functional flow diagram of the FGL.

3.5.3.4.3.2 General Description - FGL receives 20-bit parallel words from the computer via the MCP and TACCO MPD Logic and utilizes this data to generate the analog signals necessary for conic presentation on the MPD. Two data w orals are required to define a conic. The FGL shall transmit the unblank signal to the MPD Logic when it is in a state to receive data describing a new conic. It shall also receive diagnostic instructions and transmit diagnostic data via the MTL.

3.5.3.4.3.3 Operating Requirements

3.5.3.4.3.3.1 Presentation Requirements

3.5.3.4.3.3.1.1 Configurations to be Displayed

(1) Ellipse - The X and Y components of the semimajor and semiminor axes are contained in Conic Data words 1 and 2 respectively. This data shall be referenced to the center of the ellipse as shown in Figure 124, part A. The semiminor axis shall be oriented at an angle of 90 degrees in the counterclockwise direction from the semimajor axis. Bit allocations for the data are shown in 3.5.3.4.3.3.2(1) and 3.5.3.4.3.3. 2(2).

(2) Circles - Circles shall be transmitted as two words. The length of the semimajor and semiminor axes shall be equal to each other. The first word shall contain the X coordinate of the end point of the semimajor axis and zero for the Y coordinate data. The second word shall contain the Y coordinate of the end point of the semiminor axis and zero for the X coordinate data (Figure 124, part B). Bit allocations for the data are shown in 3.5.3.4.3.3. 2(1) and 3.5.3.4.3.3.2(2).

(3) Vectors or Straight Lines - Vectors or straight lines shall be transmitted as two words. The first word shall contain the X and Y components of the semimajor axis. The second or semiminor axis word shall be transmitted as 0's (Figure 124, part C). Bit avocations for the data are shown in 3.5.3.4.3.3.2(1) and 3.5.3.4.3.3.2(2).

3.5.3.4.3.3.1.2 Symmetry - The property of symmetry shall be utilized to restrict the semimajor axis to the first and our h quadrants. The semiminor axis, being oriented 90° CCW, is similarly restricted to lie in the first and second quadrants. Ellipses or straight lines which have the Y axis as their semimajor axis, shall have the semimajor axis positioned in the first quadrant (Figure 124, parts D, E and F).

3.5.3.4.3.3.1.3 Timing - Timing shall be in accordance with Figure 125. The maximum generation time for one circle, ellipse or vector shall be 550 microseconds.

3.5.3.4.3.3.2 Data Transmission - Two sequential data transmissions shall be required to describe a complete ellipse, circle or vector (Figure 126).

(1) First Transmission - This data word shall contain the X and Y components of the semimajor axis (a_x and a_y). The transmission shall consist of a 20-bit message; bits 5 through 14 representing a_y and bits 20 through 29 representing ax. Bits 5 and 20 are the LSB's and bits 14 and 29 the MSB's. Negative numbers shall be expressed in one's complement code (Figure 126).

(2) Second Transmission- This data word shall contain the X and Y components of the semiminor axis (b_x and b_y). The bit allocations for the x and y data for the semiminor axis shall be the same as described in 3.5.3.4.3.3.2(1). Negative numbers shall be expressed in one's complement code.

3.5.3.4.3.3.3 Accuracy and Distortion - X and Y Full Scale Deflection

3.5.3.4.3.3.3.1 Accuracy and Distortion Under Nominal Conditions - Nominal conditions are defined as the temperature range of 10°C to 40°C, and the range of input power within the bounds of Limits 2 and 3 of Figure 3, MIL-STD-704 as modified by 3.3.12.1. Accuracies under these conditions shall be as follows:

(1) The X and Y total harmonic distortion of the sinusoidal conic generation signals shall be less than 1'%.

(2) The phase difference between the X and Y sinusoidal conic generation signals shall be less than one degree.

(3) A change in the digital signal shall produce a corresponding change in the analog signal within one LSB.

(4) The magnitude accuracy of X relative to Y shall be less than +1%.

(5) The absolute accuracy of X or Y shall be less than +2%.

3.5.3.4.3.3.3.2 Accuracy and Distortion Under Extreme Conditions - Extreme conditions shall be as defined in 3.3.10. Accuracies under these conditions shall be as follows:

(1) The X or Y total harmonic distortion of the sinusoidal conic generation signals shall be less than 2%.

(2) The phase difference between the X and Y sinusoidal conic generation signals shall be less than 2 degrees.

(3) A change in the digital signal shall produce a corresponding change in the analog signs 1 within one LSB.

(4) The magnitude accuracy of X relative to Y shall be less than +2%.

(5) The absolute accuracy of X or Y shall be less than +4%.

3.5.3.4.3.3.4 Test Mode - The MCP shall exercise the FG by synthesizing various computer command words. (Refer to 3.5.3.4.5.)

3.5.3.4.3.3.5 Scaling - The X and Y components of an ellipse are represented in 10-bit, one's complement, binary notation. The value of the LSB is 1/512 of the display diameter, approximately 1/32 inch on the MPD. The maximum magnitude of each component shall be one display diameter. This allows, for example, gene ration of the maximum circle, whose radius is equal to one display diameter.

3.5.3.4.3.4 Interface Requirements

3.5.3.4.3.4.1 General - The Function Generator Logic shall receive signals from the MTL, and the MPD Logic and transmit signals to both the MPD and MPD Logic, and the MTL.

3.5.3.4.3.4.1.1 Signals to Function Generator Logic

3.5.3.4.3.4.1.1.1 Signals from Multipurpose Display Logic - The FGL shall receive 20 data lines, and two control lines. The control 1 and 2 lines associate the axis (semimajor or the semiminor) with the data word. The time between transmission of the leading edges of adjacent control signals shall be a minimum of 8 microseconds. After the second control signal (semiminor axis data word identifier) is transmitted, the MPD Logic will inhibit transmission of any further control lines until after it receives the Reset signal from the FGL.

3.5.3.4.3.4.1.1.2 Signals from Master Timing Logic - The FGL shall receive the following signals from the MTL:

(1) Diagnostic Instruction - The FGL shall receive six lines of diagnostic instruction from the MTL.

(2) Clock - The FGL shall receive 1.536 MHz clock from the MTL.

3.5.3.4.3.4.1.2 Signa1s from Function Generator Logic

3.5.3.4.3.4.1.2.1 Signal to Multipurpose Display Logic - The FGL shall transmit the reset line to the MPD logic.

3.5.3.4.3.4.1.2.2 Signals to Master Timing Logic - The FGL shall transmit 13 bits of diagnostic data to the MTL when so instructed.

3.5.3.4.3.4.1.2.3 Signals to Multipurpose Display - These signals shall be as follows:

(1) Video Signal - The video signal shall have its amplitude directly proportional to the magnitude of the major axis, and shall have a minimum of four discrete levels of equal magnitude to control the brightness of conies on the MPD. The video circuit shall supply a positive going signal from O. 0 volts to btween 2.0 to 2.5 volts. The following is a table of the desired video increments.

Video Voltage (+5% +20 mv)	%Maximum Radius Displayed
0.0% x Maximum Voltage	0 - 25%
6. 5% x Maximum Voltage	26- 50%
25% x Maximum Voltage	51- 75%
Maximum Voltage	76- 100%

(2) Unblank Signal - The Unblank signal shall be transmitted as a positive pulse to the unblank input of the appropriate analog channel of the MPD. The amplitude of this pulse shall be +5.0 ±1,0 volts and a duration of 83.3 to 90 microseconds.

(3) Deflection Signals - The X and Y deflection sinusoidal signals shall have a frequency of 12 KHz. The maximum deflection voltage (one display radius) shall be +12.0 to +16.0 volts.

3.5.3.4.3.4.2 Input/Output Signal Characteristics

3.5.3.4.3.4.2.1 Maintenance Control Panel, MPD 1 Logic and Master Timing Logic - All internal digital signals between the FGL and the MCP, the MPD 1 Logic and MTL shall be transmitted over single ended lines whose logical “zero” shall be 0.0, +0.5, -0.0 volts and logical “one” shall be 5.0 +1.5 volts.

3.5.3.4.3.4.2.1.1 Clock - The clock signal transmitted from the MTL to the FGL shall be a square wave whose frequency is 1.536 MHz.

3.5.3.4.3.4.2.2 Triaxial Transmissions - All signals to the MPD 1 shall be transmitted via Ampheno1 421-033 cable or equivalent terminated in a differential amplifer whose input impedance shall be 90 to 95 ohms and 100 pf maximum. The coaxial cable shall not exceed 100 feet. The signals shall be as follows:

X and Y Deflection Signals - The X and Y deflection signal characteristics shall be as specified in 3. 5.3.4.3.3.3.1 and 3.5.3.4.3.4.1. 2.3(3).

(2) Video Signals - The video signal characteristics shall be as specified in 3.5.3.4.3.4.1.2.3(1). In addition, the rise time and the fall time of this signal when measured at the 10% and 90% amplitude points shall be a maximum of 100 nanoseconds.

(3) Unblank Signal - The Unblank signal characteristics shall be as specified in 3.5.3.4.3.4.1.2.3(2). In addition the rise time and fall time of this signal when measured at the 10% and 90% amplitude points shall be a maximum of 100 nanoseconds.

3.5.3.4.3.5 Description of Operation

3.5.3.4.3.5.1 Data Transmission - The computer via the MPD Logic, transmits two data words to the FG, in one's complement form. Each word is accompanied by one control signal which strobes the data into either the sin 8 or cosθ storage register. The crystal oscillator in the MCP generates a 1.536 MHz square wave which is divided into four 12 KHz output square waves. The timing and control circuitry senses the Word 2 strobe and permits the 12 KHz square waves to individually strobe the outputs of the storage registers.

3.5.3.4.3.5.2 Digital to Analog Converter - The digital to analog converter circuitry receives data at a 12 KHz rate. The D/A converts this 12 KHz signal into a modulated square wave symmetrical about a DC voltage level. The amplitude of the D/A output signal is a function of the one's complement data transferred from the storage registers.

3.5.3.4.3.5.3 Video Circuitry - This circuitry monitors the two most significant magnitude bits of the semimajor storage registers for the purpose of generating the video signal. This signal shall be a function of the conic size to be displayed.

3.5.3.4.3.5.4 Analog Filters and Sum Circuitry - This circuitry algebraically sums ax sin θ a_y sin θ and b_x cos θ by sin θ to produce a shifted sinusoidal signal. Low pass filters convert the incoming square wave into an analog sine wave signal.

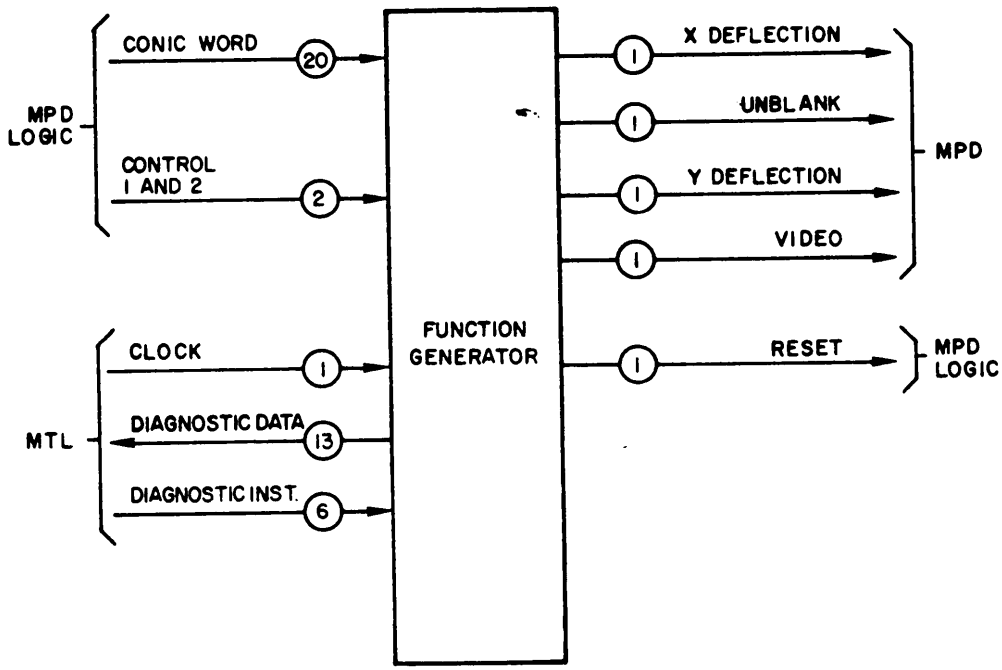


Figure 123. Function Generator Logic, Functional Flow Diagram

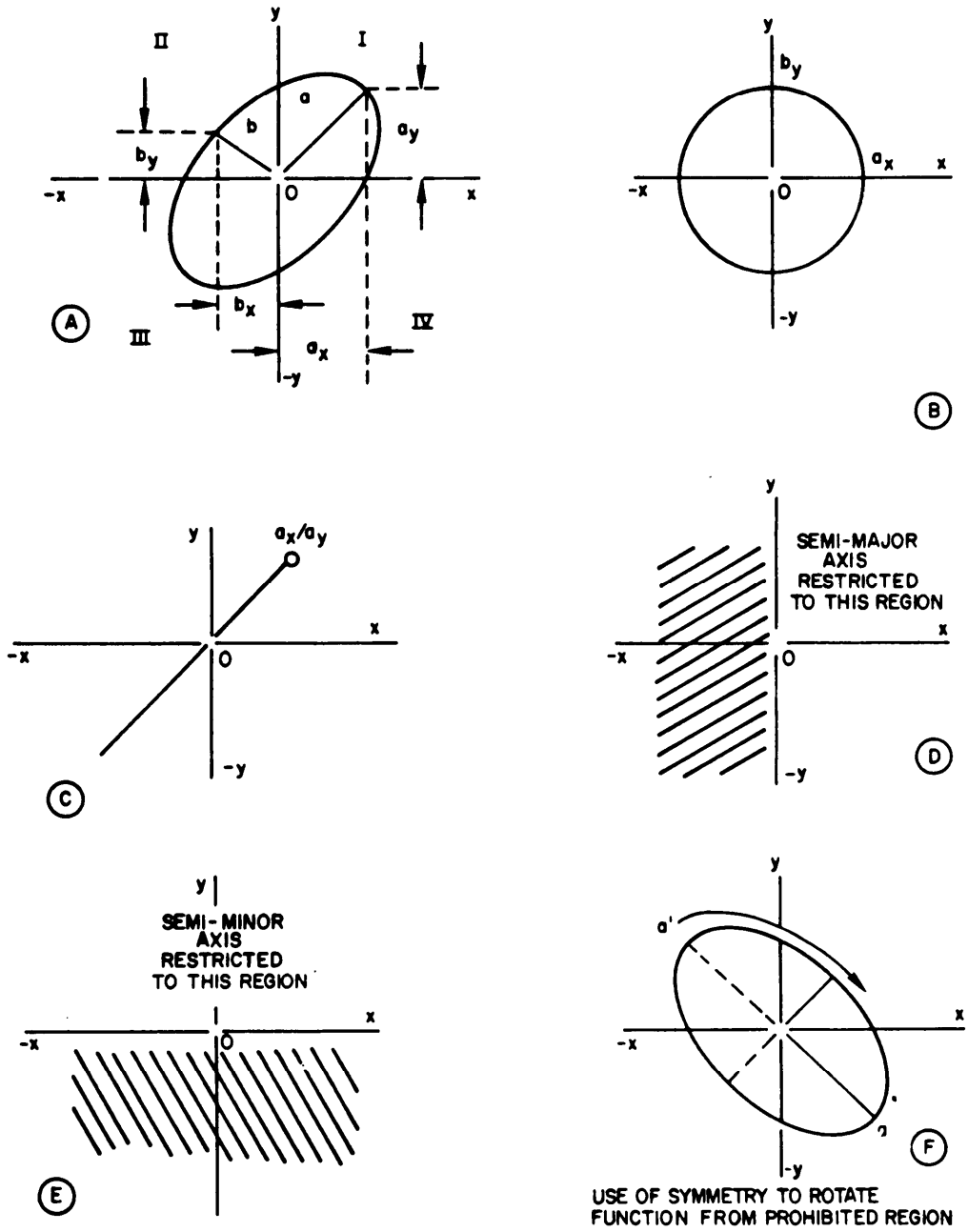


Figure 124. Conic Presentation on Multipurpose Display Using Function Generator Logic

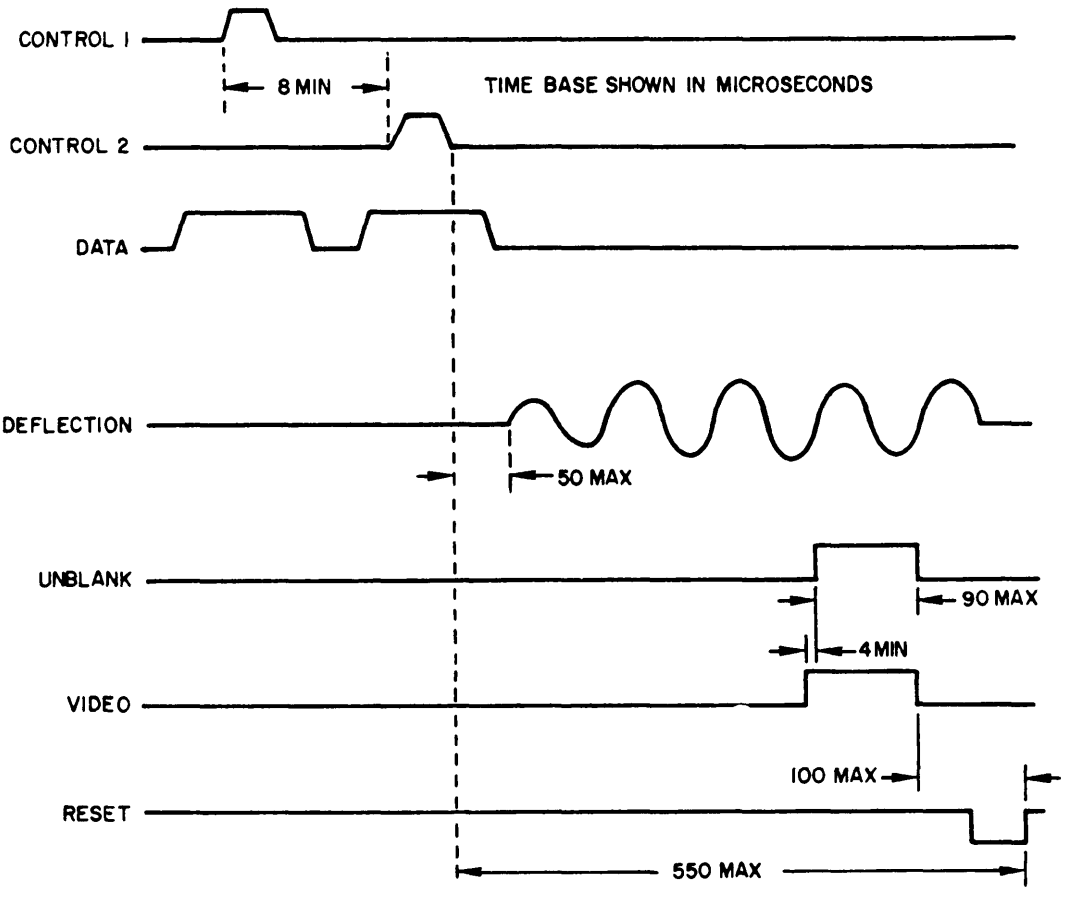
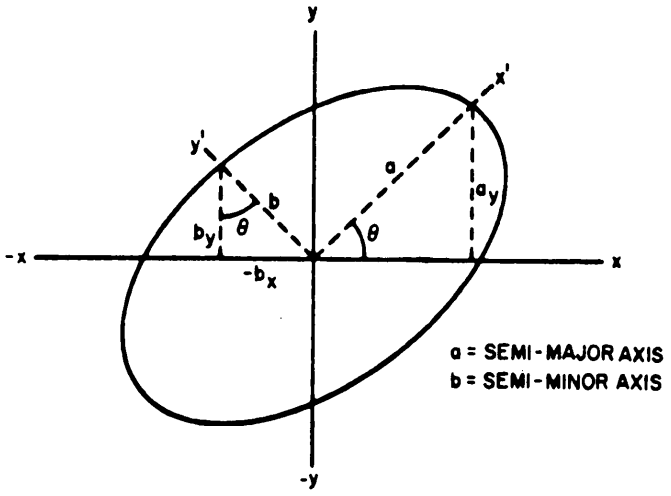


Figure 125. Function Generator Timing Diagram



$x' = a \sin wt$ $\qquad y' = b \cos wt$

$a_x = a \cos \theta$ $\qquad -b_x = b \sin \theta$

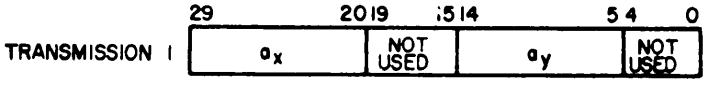
$a_y = a \sin \theta$ $\qquad b_y = b \cos \theta$

$x = a \cos \theta \sin wt + b \cos \theta \cos wt$

$y = a \sin \theta \sin wt + b \cos \theta \cos wt$

$x = a_x \sin wt + b_x \cos wt$

$y = a_y \sin wt + b_y \cos wt$



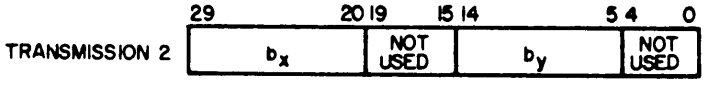


Figure 126. Word Formats and Definition of Axes for Conic Presentation on Multipurpose Display

3.5.3.4.4 Master Timing Logic

3.5.3.4.4.1 Functional Description - The Master Timing Logic (MTL) shall provide the timing and control signals necessary to "line-lock" (sync) display operations to the aircraft's 400 Hz power source. It shall also provide diagnostic control for Logic Unit 3.

Figure 127 is a functional flow diagram of the MTL.

3.5.3.4.4.2 Interface Requirements

3.5.3.4.4.2.1 General

3.5.3.4.4.2.1..1 Signa1s to Master Timing Logic - The MTL shall receive signals shown in Figure 127 from both the MPD 1 Logic, MPD 2 Logic, the PDL, the FGL, the power supply, the MCP and the computer.

3.5.3.4.4.2.1.1.1 Signals from MPD 1 Logic - The signals received from the MPD 1 Logic shall be as follows:

(1) Radar Scan Converter Enable - When this signal is present, the MTL shall transmit the RADAR S. C. Enable signal to both the Radar Scan Converter and MPD 1 Logic, and the RADAR Unblank to MPD 1.

(2) Spare Scan Converter Enable - When this signal is present, the MTL shall transmit the SPARE S. C. Enable signal to both the Spare Scan Converter and MPD 1 Logic.

(3) LLLTV Active - When this signal is a logic "1", the MTL shall cause the sync pulse to be generated at a 57.1 Hz rate. When this signal is a logic "0", the MTL shall cause the sync pulse to be generated at a 40 Hz rate.

(4) Diagnostic Data - When so instructed MPDL 1 shall transmit 24 bits of diagnostic data and a diagnostic sync to the MTL.

3.5.3.4.4.2.1.1.2 Signals from MPD 2 Logic - The signals received from the MPD 2 Logic shall be as follows:

(1) Radar Scan Converter Enable - When this signal is present, the MTL shall transmit the RADAR S.C. Enable signal to both the Radar Scan Converter and MPD 2 Logic, and the Radar Unblank to MPD 2.

(2) Spare Scan Converter Enable - When this signal is present, the MTL shall transmit the SPARE S. C. Enable signal to both the Spare Scan Converter and MPD 2 Logic.

(3) LLLTV Active - When this signal is a logical "l", the MTL shall cause the Sync pulse to be generated at a 57. 1 Hz rate. When this signal is a logical "O", the MTL shall cause-the 'sync pulse to be, generated at a 40 Hz rate.

Diagnostic Data - When so instructed the MPDL 2 shall transmit 24 bits of diagnostic data and a diagnostic sync to the MTL.

3.5.3.4.4.2.1.1.3 Signals from Power Supply - The MTL shall receive from the power supply a 400 Hz ±10% sine wave which is synchronized to the aircraft primary power source.

3.5.3.4.4.2.1.1.4 Signals from Function Generator Logic - When instructed the FGL shall transmit 12 bits of diagnostic data and a diagnostic sync to the MTL.

3.5.3.4.4.2.1.1.5 Signals from Pilot Display Logic - When so instructed the PDL shall transmit 12 bits of diagnostic data and a diagnostic sync to the MTL.

3.5.3.4.4.2.1.1.6 Signals from Computer - The computer shall transmit 16 bit diagnostic words to the MTL, via the MCP, by means of External Function Request/External Function operation as described in Appendix L

3.5.3.4.4.2.1.1.7 Signals from Maintenance Control Panel - The MCP shall transm it the On Line and Verify switch status lines for manual MTL operation.

3.5.3.4.4.2.1.2 Output Requirements - The MTL shall transmit signals, as shown in Figure 129, to the MPD 1 Logic, MPD 2, MPD 2 Logic, Radar Interface Unit, Radar Scan Converter, Spare Scan Converter, PDL, FGL, Computer, MCP and LLLTV control. Relative timing requirements for these signals are shown in Figure 128.

3.5.3.4.4.2.1.2.1 Signals to Multipurpose Display 1 - The MTL shall transmit the Radar Scan Converter Unblank to MPD 1 under the conditions of 3. 5.3.4.4,2.1.1.1 (l). This signal shall be a logical “1” 50 microseconds + 1 microsecond after the 40 Hz sync and shall drop to a logical “O” 17.45 msec +10% later.

3.5.3.4.4.2.1.2.2 Signals to Multipurpose Display 1 Logic - The MTL shall transmit signals to the MPD 1 Logic as follows:

(1) 40 or 57.1 Hz Sync - a four µ sec + 1.0 µ sec pulse every 25 or 17.5 msec ±10% as selected by the "LLLTV Active" line, via the MCP, as per 3.5.3.4.4.2.1.1. 2(3).

(2) 1 Hz Flash - a signal which is alternately high and low every half second +10%.

(3) Radar Scan Converter Enable - a signal which is a logical “l” for 17.5 msec ±10% initiated by the 40 Hz sync under the conditions of 3.5.3.4.4.2.1.1.1(1).

(4) Spare Scan Converter Enable - a signal which shall be variable between 17.5 and 22.5 milliseconds in increments of 2.5 milliseconds. The signal duration shall be selected by a wiring change. This signal is initiated by the 40 Hz sync under the conditions of 3.5.3.4.4.2.1.1. 1(2), and shall have a timing tolerance of +10%.

(5) Diagnostic Instruction - The MTL shall transmit six lines of diagnostic instruction to MPDL 1.

(6) Clock - The MTL shall transmit a 2.000 MHz square wave to MPDL 1.

3.5.3.4.4.2.1.2.3 Signals to Multipurpose Display 2 - The MTL shall transmit the Radar Scan Converter Unblank to MPD 2 under the conditions of 3.5.3.4.4.2.1.1.2(1). This signal is as described in 3.5.3.4.4.2.1.2.1.

3.5.3.4.4.2.1.2.4 Signals to Multipurpose Display 2 Logic - The MTL shall transmit the same signals to the MPD 2 Logic as those that are transmitted to MPD 1 Logic, specified in 3.5.3.4.4.2.1.2.2.

3.5.3.4.4.2.1.2.5 Signal to Radar Interface Unit - The MTL shall transmit the 1 Hz Flash signal continuously to the Radar Interface Unit.

3.5.3.4.4.2.1.2.6 Signal to Spare Scan Converter - The MTL shall transmit the SPARE S. C. Enable to the Spare Scan Converter under the conditions of 3.5.3.4.4.2.1.1. 1(2) and 3.5.3.4.4.2,1.1.2(2). This signal is described in 3.5.3.4.4.2. 1.2.2(4).

3.5.3.4.4.2.1.2.7 Signals to Pilot Display Logic - The MTL shall transmit signals to the PDL as follows:

(1) 40 Hz Sync - As per 3.5.3.4.4.2.1.2.2(1).

(2) 1 Hz Flash - As per 3.5.3.4.4.2.1.2.2(2).

(3) Diagnostic Instruction - The MTL shall transmit six lines of diagnostic instruction to the PDL.

(4) Clock - The MTL shall transmit a 1.536 MHz square wave to the PDL.

(5) Diagnostic Instruction - The MTL shall transmit six lines of diagnostic instruction to MPDL #l.

(6) Clock - The MTL shall transmit a 2.000 MHz square wave to MPDL #1.

3.5.3.4.4.2.1.2.8 Signal to Radar Scan Converter - The MTL shall transmit the Radar S. C. Enable to the Radar Scan Converter under the conditions of 3.5.3 .4.4.2.1.1.1(1) and 3.5.3.4.4.2.1.1.2(1). This signal is described in 3.5.3.4.4.2.1. 2.2(3).

3.5.3.4.4.2.1.2.9 Signal to LLLTV Control - The MTL shall transmit the 57.1 Hz Sync signal to the LLLTV Control Unit each 17.5 milliseconds. This signal shall have a pulse width (logical "1") of 2.5 milliseconds.

3.5.3.4.4.2.1.2.10 Signal to Computer - The MTL shall transmit 26 bits of diagnostic data to the computer via the MCP. This shall be accomplished through the use of Input Data Request/Input Acknowledge operation of the computer as described in Appendix I.

3.5,3.4,4.2.1.2.11 Signals to Maintenance Control Panel - The MTL shall transmit clock signals to the MCP.

3.5.3.4.4.2.2 Signal Characteristics

3.5.3.4.4.2.2.1 Signals to Master Timing Logic - The signals to the MTL described herein shall be levels where +5+1. 5 volts represents a logical "1" and 0+0.5,-0 volt, represents a logical "0".

3.5.3.4.4.2.2.2 Signals from Master Timing Logic

(1) Twisted Pair Transmissions - The following output signals from the MTL shall be transmitted via twisted Pair cable. Each pair shall be driven by line driver circuits as referenced in WR101 Part H and terminated by input amplifiers as specified in Appendix H or their electrical equivalent.

(a) 57.1 Hz Sync to LLLTV Control

(b) 1 Hz Flash to Radar Interface Unit

A logical "0" shall be 4 ±1 volts, a logical "1" shall be 0 +0.5, -0.0 volts. Transition times shall be less than one microsecond when measured at the 10% and 90% points.

(2) Triaxial Transmissions - All triaxial transmissions shall be via Amphenol 421-033 cable or equivalent, terminated in a differential amplifier, whose input impedance shall be 90 to 95 ohms and a 100 picofarads maximum. The following signals shall be transmitted via triaxial cables. The triaxial cable length shall not exceed 100 feet.

(a) Radar Scan Converter Unblank to MPD 1

(b) Radar Scan Converter Unblank to MPD 2

(c) Radar Scan Converter Enable to Spare Scan Converter

(d) Spare Scan Converter Enable to Spare Scan Converter

A logical “0” shall be 0+0.5, -0.0 volts, a logical “l” shall be 5 +1 volts. Transition times shall be less than 100 nanoseconds when measured at the 10% and 90% points.

(3) Internal Transmissions - All internal signals between the MTL and other subunits located in Logic Unit 3 shall be transmitted over single ended lines where a logical “0” is represented by 0 +0.5, -0.0 volts and a logical “1” is represented by +5 ±1.5 volts.

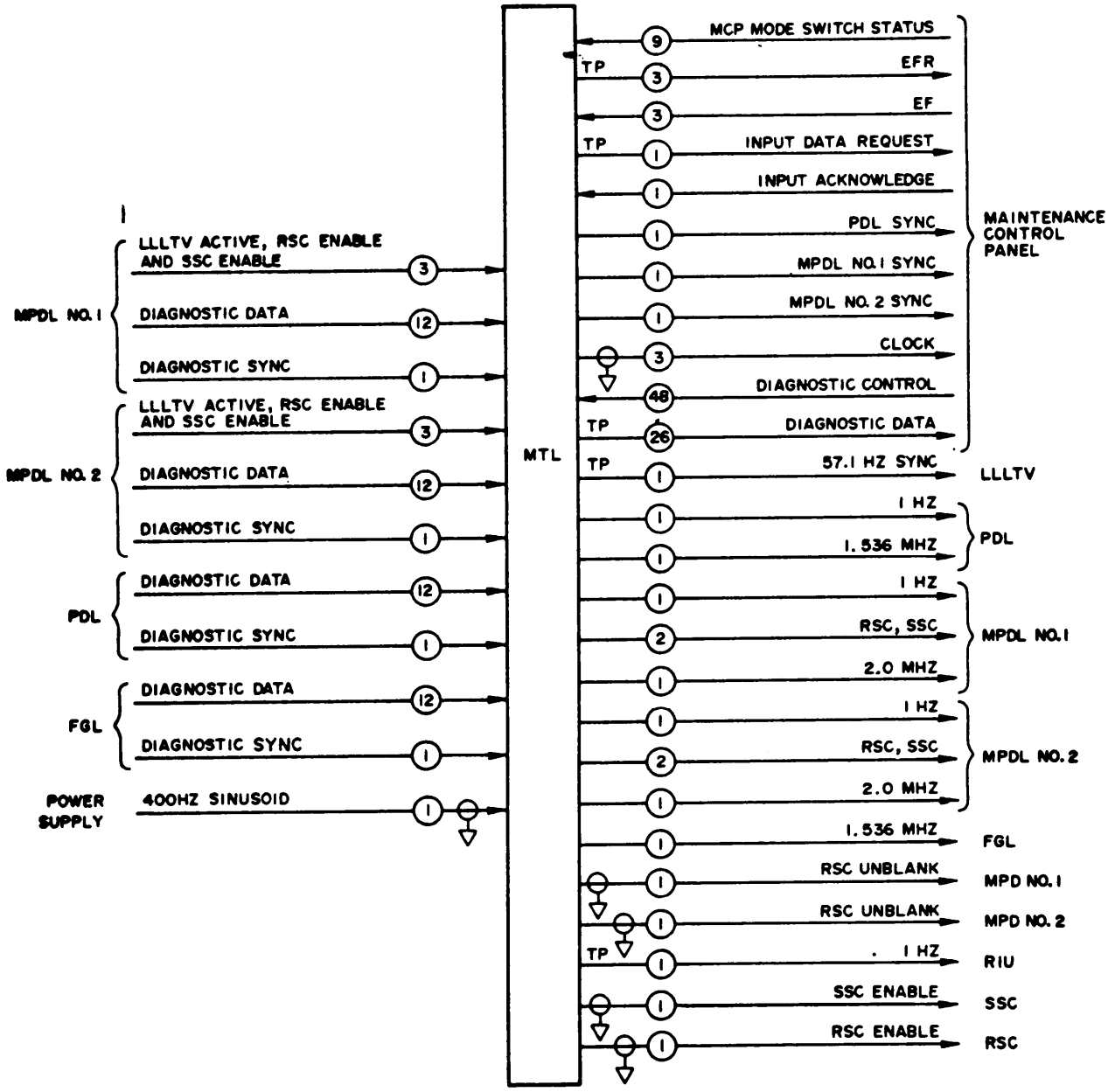


Figure 127. Master Timing Logic Functional Flow Diagram

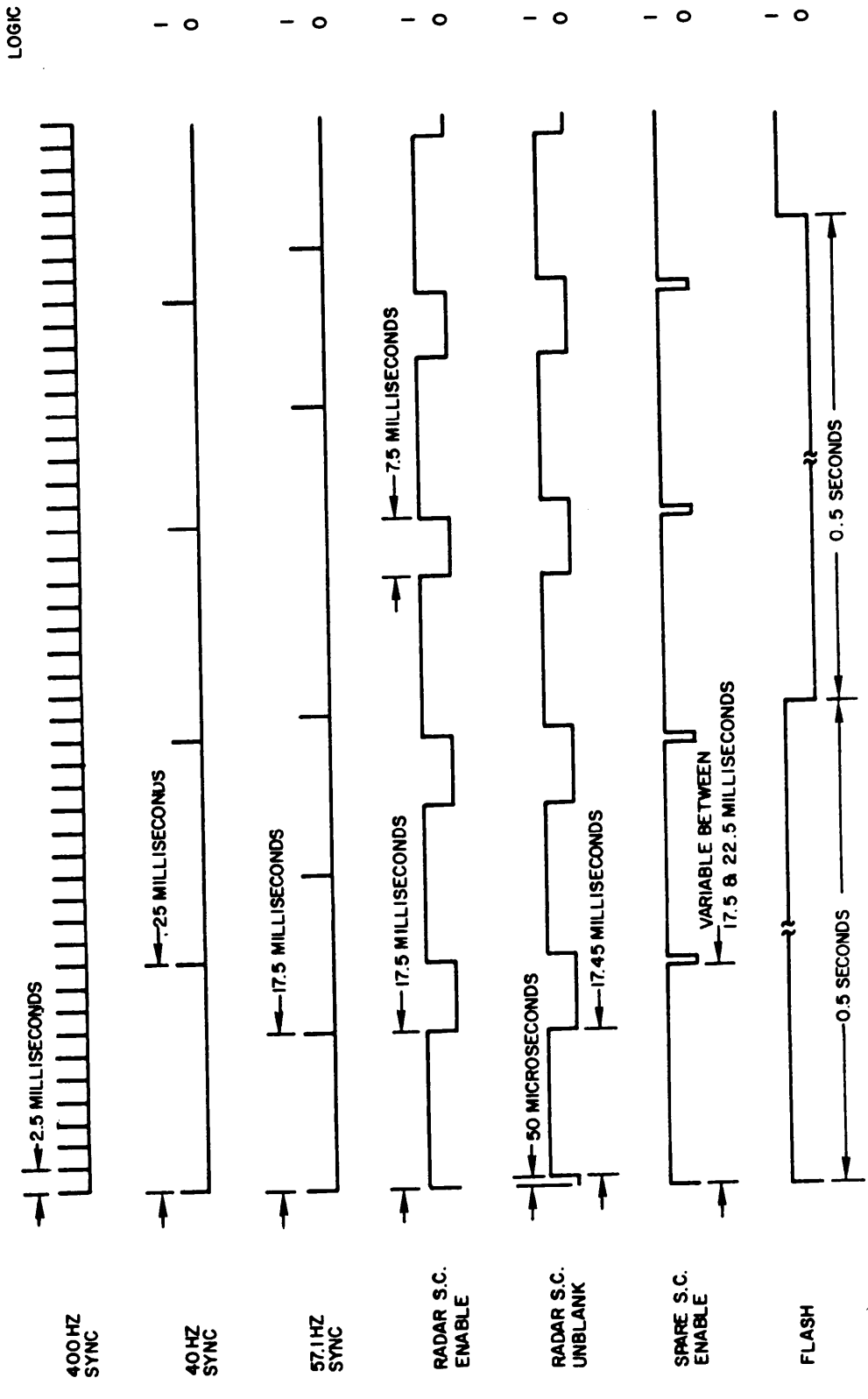


Figure 128. Master Timing Logic Output Signals

3.5.3.4.5 Maintenance Control Panel Subunit

NOTE

Since the Maintenance Control Panels for the four Logic Units are nearly identical, only one over-all MCP description is given. Refer to 3.5.1.4.9.

3.5.3.4.6 Power Supply Subunit - Logic Unit 3 shall contain a power supply subunit as described in 3.3.12.2.

3.5.4 Data Analysis Logic Unit MX-9360/AYA-8B (Logic Unit 4)

3.5.4.1 Function - See 3.4.10

3.5.4.2 Form Factor - Refer to illustration in EI-515, Avionics Installation Instructions for Data Analysis Programming Group AN/AYA-8B.

3.5.4.3 Weight - See 3.5.1.3

3.5.4.4 Contents - See 3.4.5

3.5.4.4.1 Data Multiplexer Subunit (DMS)

3.5.4.4.1.1 Functional Description - The computer will be capable of servicing 16 input peripheral equipments and 16 output peripheral equipments utilizing the normal input and output data transfer. The rate and priority of the data to many of the peripherals will not demand real time access to the computer memory, i. e. , many of the peripherals will be able to communicate with the computer via a buffer unit. The DMS will be such a unit. The DMS will be basically a multipole, multithrow logic switch under direct computer control, servicing a number of peripheral I/O's. Figure 139 is a functional flow diagram of the DMS.

3.5.4.4.1.2 General Description - The DMS shall provide the capability of transmitting 30 data bits to and from each of seven peripheral equipments and the computer via a single input/output computer channel. An additional channel shall be provided to loop computer output data back as computer input data through a minimum amount of DMS logic.

3.5.4.4.1.3 Operating Requirements

3.5.4.4.1.3.1 Data Transfer -- Peripheral Equipment and the DMS to the Computer - Communications between the DMS and the computer shall be in accordance with Appendix L A peripheral which connects with the computer via the DMS shall be able to transmit up to 30 bit data words to the computer using Input Data Request (IDR), Input Acknowledge (IA) or up to 26 bit data words to the computer using External Interrupt (EI). There shall be four input words, Peripheral IDR. IDR Monitor EI, Peripheral EI, and DMS Status EL If more than one of these inputs occurs at the same time, the following table shall determine which input shall be transmitted to the computer first. The Power Monitor EI for Logic Unit *4* as described in *3, 5.4.4 .1.3.1* (5) shall also be generated in the DMS and it shall be transmitted to the computer as an overriding input.

INPUT WORD PRIORITY

PRIORITY	INPUT WORD
Highest 1	Power Monitor EI
2	Peripheral EI
3	IDR Monitor EI
4	DMS Status EI
Lowest 5	Peripheral IDR

(1) Periheral IDR - Data transfer using IDR shall be under computer control. By outputting a DMS Instruction F see 3.5.4.4.1.5) the computer shall be able to select one and only one DMS Input Channel to input via IDR.

When an input peripheral raises an IDR to the selected DMS channel, the IDR and up to a 30-bit data word shall be routed directly to the computer. The acknowledge signal shall be routed directly to the peripheral when the computer acknowledges the IDR. The IDR input interface to the selected peripheral shall function as if the peripheral were interfacing directly with the computer.

(2) IDR Monitor EI - When an input peripheral raises an IDR to a DMS channel that is not selected, the fact that the IDR has been raised shall be transmitted to the computer via an IDR Monitor EI, identifying which peripheral raised the IDR. When the computer acknowledges this EI, the acknowledge signal shall not be transmitted to the peripheral. The peripheral will maintain the IDR on the line until the computer has selected the channel and acknowledged the IDR as discussed in the previous paragraph. Provisions shall be made in the DMS for the computer to enable any DMS channel combination to interrupt the computer with an IDR Monitor EI. An IDR from a DMS channel not so enabled shall not cause an IDR Monitor or EI to be generated.

If more than one peripheral raise IDR's to DMS channels that are not selected to input LDR's but are enabled to generate IDR Monitor El's, the channel to be transmitted to the computer first shall be in accordance with the following tabulation:

IDR MONITOR EI-CHANNEL PRIORITY

PRIORITY	DMS CHANNEL NUMBER
Highest 1	7
2	6
3	5
4	4
5	3
6	2
7	1
Lowest 8	0

(3) Peripheral EI - Data transfer using EI shall be under peripheral control. When an input peripheral raises an EI to any DMS channel, the DMS shall perform the following sequence of events:

(a) Complete any existing input operation

(b) Determine if the channel raising the EI is enabled to input EI's (provisions shall be made in the DMS for the computer to enable any DMS channel combination to interrupt the computer with a peripheral EI. An EI from a DMS channel not so enabled shall not cause a peripheral EI to be transferred to the computer).

(c) 1. If the channel is not enabled, continue with normal input operations. If the computer subsequently enables the channel, complete any existing input operation and proceed as in (c) 2.

(c) 2. If the channel is enabled, generate a four-bit tale to identify which peripheral raised the EL

(d) Place the four-bit identity code along with up to 26 bits from the peripheral on the computer's input data lines.

(e) Raise an EI to the computer.

(f) The computer at its convenience samples the input data lines and transmits an acknowledge signal to the DMS.

(g) On detecting the acknowledge signal, drop the EI line to the computer.

(h) Route the acknowledge signal to the peripheral that raised the EL

(i) Resume normal input operations.

If more than one peripheral raise EI's to DMS channels that are enabled to interrupt, the channel to be transmitted to the computer first shall be in accordance with the following tabulation:

PERIPHERAL EI CHANNEL PRIORITY

PRIORITY	DMS CHANNEL NUMBER
Highest 1	7
2	6
3	5
4	4
5	3
6	2
7	1
Lowest 8	0

(4) DMS Status EI - Provisions shall be made in the DMS for the computer to interrogate the state of previously outputted computer command codes. On receipt Of a DMS instruction E F (see 3.5.4.4.1. 5) with the multiplexer status request code, the DMS shall perform the following sequence of events: "

(a) Complete any existing input operation.

(b) Place the multiplexer status data on the computer input lines.

(c) Raise an EI to the computer.

(d) The computer, at its convenience, samples the input data lines and transmits an acknowledge signal to the DMS.

(e) On detecting the acknowledge signal, drop the EI line to the computer.

(f) Resume normal input operations.

(5) Power Monitor EI - On receipt of a change in power status (Power Turn-On or Power Out-Of-Tolerance) the DMS shall perform the following:

(a) Discontinue any existing input operation, resetting any active input request level, either EI or IDR.

(b) Place the Power Monitor data on the computer input data lines.

(c) Delay between 10 microseconds minimum and 20 microseconds maximum.

(d) Raise an EI to the computer.

(e) The computer, at its convenience, samples the input data lines and transmits an acknowledge signal to the DMS.

(f) On detecting the acknowledge signal, drop the EI line to the computer.

(g) Resume normal input operations.

3.5.4.4.1.3.2 Data Transfer - Computer to Peripheral Equipment and the DMS - An output peripheral equipment which communicates with the computer via the DMS shall be able to receive up to a 30-bit data word from the computer by the Output Data Request (ODR) /output Acknow - ledge (OA) data transfer mode or up to a 29-bit data word from the computer by the External Function Request (EFR) External Function (EF) data transfer mode. Output Bit 29 (OB29) of the EF word will not be available to the output peripherals. It shall, in the DMS, determine a peripheral EF word; a logic zero being a peripheral word. There will be two types of EF words which shall be used within the DMS and not transferred to the peripherals, Master Clear E F and DMS Instruction E F.

(1) Peripheral OA - Data transfer using OA shall be under computer control. By outputting a DMS Instruction E F, the computer shall be able to select one and only one DMS output channel to receive up to a 30-bit output data word via OA. When an output peripheral raises an ODR TO THE SELECTED DMS channel, indicating it is in a condition to accept data, the DMS shall perform the following sequence of events:

(a) Route the ODR directly to the computer.

(b) The computer 1/0 subunit detects the ODR.

(c) The computer at its convenience places up to 30 data bits on the computer output data lines. The 30 data bits are routed directly to all DMS channels. Except for interface circuits, the DMS shall perform no logic affecting this data.

(d) The computer sets the Output Acknowledge line indi- the data is ready to be sampled.

(e) The DMS routes the Output Acknowledge signal to the selected DMS channel.

(2) Peripheral EF - Data transfer using E F shall be the same as OA except only 29 bits will be available to the peripherals.

(3) (3) DMS E F - The computer will transmit this word to the DMS with force; on receipt of all EF words the DMS perform the following sequence:

(a) Determine the status of Output Bit 29.

(b) If Bit 29 equals a Logic O then the EF shall be routed as a Peripheral E F described previously.

(c) If Bit 29 equals a Logic 1 the DMS shall drop computer channel 13 EFR to a logic “0” for the duration of the EF Pulse and then perform either a Master Clear or a DMS Instruction,

3.5.4.4.1.3.3 Timing and Initialization

(1) The time required for the DMS to process one computer generated instruction shall not exceed 10 µ sec.

(2) The time between a peripheral raising an External Interrupt or an Input Data Request to the DMS and the transmission of that signal to the computer shall not ex- ceed 6 µsec assuming no other input operation is in progress when the DMS receives the signal. If an input operation is in progress, then the time from trailing edge of that input acknowledge to setting of the EI or IDR to the computer shall not exceed 6 µ sec.

(3) The time between a peripheral raising an External Function Request or an Output Data Request to the selected DMS channels and the transmission of that request to the computer shall not exceed 1 µ sec.

(4) The DMS shall be self-initializing, i.e. , when power is applied to the DMS, no logic 1's shall be transmitted on the DMS Control lines to the computer and the DMS shall be ready for normal operation.

(5) Provisions shall be made for the computer or the operator using the MCP to initialize the DMS. On receipt of the Master Clear EF. 3.5.4.4.1.6. 2(3), initializing signals shall be generated to the DMS, the ADL, and any internal (to Logic Unit 4) interface that may be added to a DMS spare channel. Following these initializing signals, the subunits shall be ready for normal operation.

3.5.4.4.1.4 Test Loops

3.5.4.4.1.4.1 In-Flight Performance Monitoring Channels - One DMS input channel and one DMS output channel shall be designated as test channels. The setting of request lines on these channels shall be controlled by the Computer program. The computer input data lines in the IDR/IA data transfer mode shall be controlled directly by the computer output data lines. The DMS shall transmit data from this channel to the computer and from the computer to this channel in the same manner as it would for any other DMS channel. This loop operation, computer to DMS to com - puter, will permit the computer to automatically monitor the performance of the DMS. In addition, it will allow the computer to check a full 30 bit interface through a minimum amount of peripheral hard- ware.

3.5.4.4.1.4.2 Diagnostic Test Loops - Provisions may be made in the DMS for additional test loops to be used in diagnosing malfunctions in the DMS and in those DMS-to-peripheral interfaces located within Logic Unit 4.

3.5.4.4.1.5 DMS Instruction Codes - The DMS Instruction Codes are four bit positions (27 through 24) of the DMS Instruction E F, Word Format 3.5.4.4.1.6. 2(4). The follow- ing describes the instruction functions.

DMS INSTRUCTION CODE

OCTAL	BINARY				
	27	26	25	24	
00	0	0	0	0	No Op - No operation performed by the DMS.
01	0	0	0	1	Select Input - The DMS shall connect an input peripheral per Field H to the computer input control and data lines. This selected peripheral shall be able to input to the computer via the IDR/IA data transfer mode.
02	0	0	1	0	Select Output - The DMS shall connect an output peripheral per Field G to the computer output control lines. This selected peripheral shall be able to receive data from the computer via the ODR/OA and the EFR/EF data transfer modes.
03	0	0	1	1	Select Input and Output - The DMS shall perform both a Select Input and a Select Output as described previously.
04	0	1	0	0	Enable Peripheral EI - The DMS shall enable. per Field F. from one to eight of the input peripherals serviced by the DMS, to access the computer via External Interrupt. This access shall be independent of peripheral select code. The access shall be via an External Interrupt, Word Format 3.5.4.4.1.6.1(2), generated by the DMS with a three-bit code identifying the peripheral raising the EI and one bit identifying this type of EI The remaining 26 bits of the word shall be transferred directly from the peripheral to the computer.

OCTAL	BINARY				
05	0	1	0	1	Enable IDR Monitor EI - The DMS shall enable, per Field F, from one to eight of the input peripherals to access the computer via an IDR when the peripheral is not selected. The access to the computer shall be via an External Interrupt generated by the DMS identifying which peripheral has raised the IDR. No data shall be transmitted from the peripheral to the computer and the peripheral's IDR shall not be cleared.
06	0	1	1	0	Enable Peripheral EI and IDR Monitor EI - The DMS shall perform both an Enable Peripheral EI and an Enable XDR Monitor EI as described previously.
07	0	1	1	1	Select Input and Output and Enable Peripherals EI and IDR Monitor EI - The DMS shall perform the four functions as previously described.
10	1	0	0	0	Multiplexer Status Request - The DMS shall transmit a DMS Status EI to the computer as described in the Word Format 3.5.4.4.1.6.1(4).
11	1	0	0	1	Set DM External Channel Test.
12	1	0	1	0	Reset DM External Channel Test.
13	1	0	1	1	Spare 1 Test, Spare 2 Test, Spare 3 Test, Spare 4 Test and Spare 5 Test - The DMS shall make available at its connector interface five signals, one for each instruction, indicating compute r test request that may be used for future subunit expansion. Two of these instructions may be used to initiate tests in existing subunits.
14	1	1	0	0	
15	1	1	0	1	
16	1	1	1	0	
17	1	1	1	1	

3.5.4.4.1.6 Interface Requirements - Refer to Figure 137, the Functional Flow Diagram for the DMS.

3.5.4.4.1.6.1 Format of Input Words to Computer from the DMS

(1) Peripheral IDR - Refer to word format shown in Figure 129.

Field A - Bits 29 through 0 - shall represent the data bits from the peripheral equipment being serviced by the selected DMS channel.

(2) Peripheral EI - Refer to format shown in Figure 130.

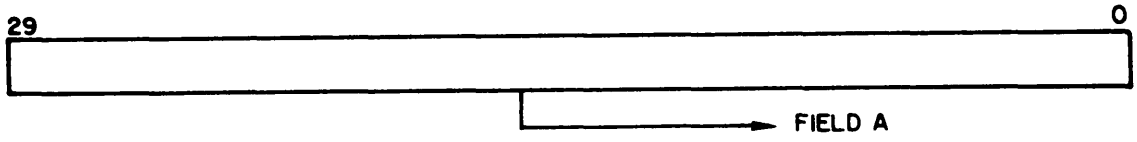


Figure 129. Format of Peripheral IDR Word

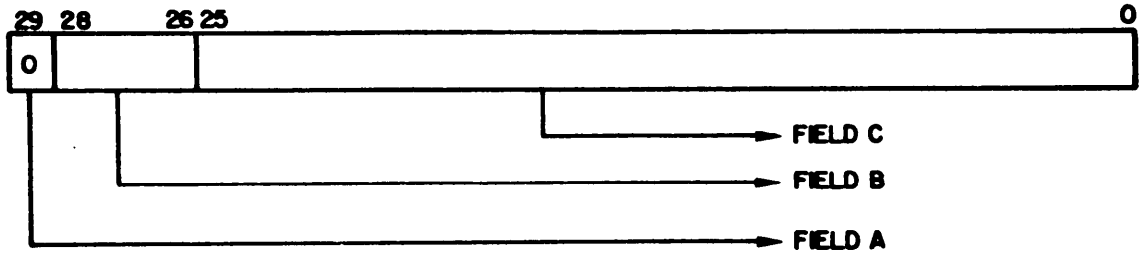


Figure 130. Format of Peripheral EI Word

Field A - Bit 29- EI Identifier bit and for this EI it shall always equal zero.

Field B - Bits 28 through 26- DMS input channel identifier per the following tabulation. The functional flow diagram, Figure 137, indicates the peripheral assigned to each DMS input channel.

DMS INPUT CHANNEL CODES FOR PERIPHERAL EI

BIT			DMS CHANNEL NUMBER
28	27	26	
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

Field C - shall represent the data bits from the peripheral equipment being serviced by the DMS.

(3) IDR Monitor EI - Refer to the word format shown in Figure 131

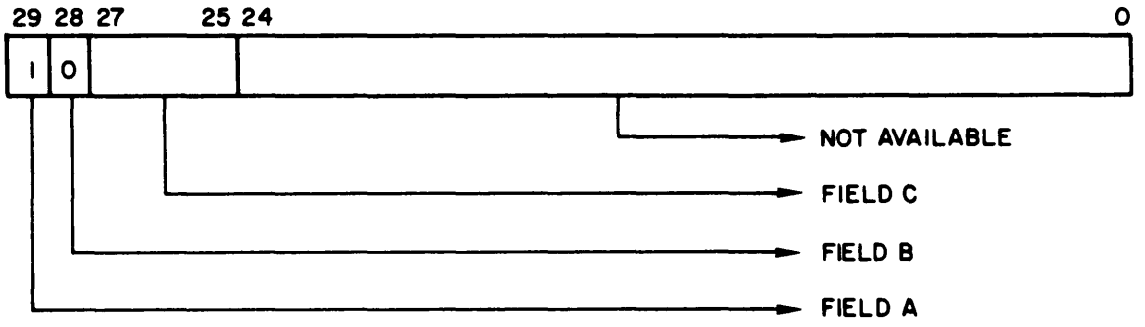


Figure 131. Format of IDR Monitor EI Word

Field A - EI Identifier bit and for this EI it shall always equal one.

Field B - Bit 28 bit and for this EI it shall always equal zero.

Field C - Bit 27 through 25- DMS Input channel identifier per the following tabulation:

DMS INPUT CHANNEL CODES FOR XDR MONITOR EI

BIT 27	26	25	DMS CHANNEL NUMBER
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

(4) DMS Status EI - Refer to the word format shown in Figure 132.

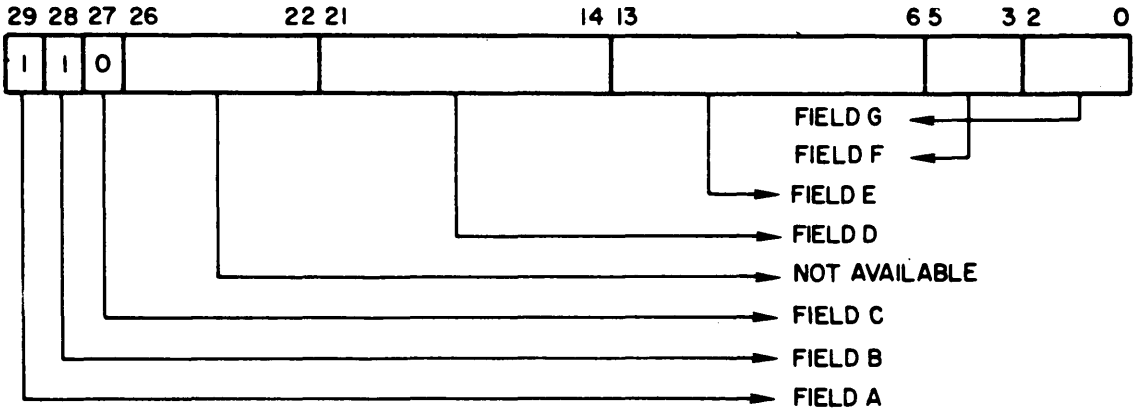


Figure 132. Format of DMS Status EI

Field A - Bit 29 - EI Identifier bit and for this EI It shall always equal one.

Field B- Bit 28 -DMS EI Idenifiier bit and for this EI it shall . always equal one.

Field C - Bit 27-Power monitor identifier bit and for this El it shall always equal zero.

Field D - Bits 21 through 14- Status of IDR Monitor EI enable code in the DMS. (Refer to the IDR Monitor EI Enable Code Table in 3.5.4.4.1.6. 2(4), Field E.)

Field E - Bits 13 through 6 - Status of Peripheral EI enable code in DMS. (Refer to the Peripheral EI Enable Code Table in 3.5.4.4.1.6. 2(4), Field F.)

Field F - Bits 5 through 3 - Status of Output select code in the DMS. (Refer to the Output DMS Channel Select Code Table in 3.5.4 .4.1.6.2 (4), Field G.)

Field G - Bits 2 through 0 - Status of input select code in the DMS. (Refer to the Input DMS Channel Select Codes Table in 3.5.4.4.1.6.2(4), Field H.)

3.5.4.4.1.6.2 Format of Output Words from the Computer to the DMS

(1) Peripheral OA - Refer to the word format shown in **Figure 133.**

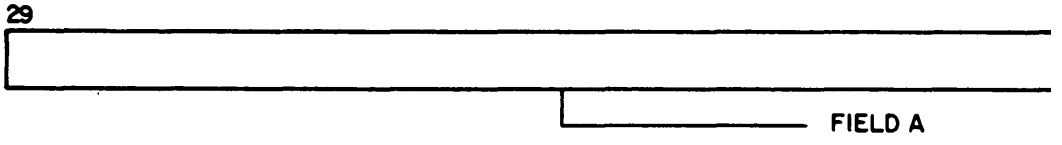


Figure 133. Format of Peripheral OA Word

Field A - Bits 29 through 0 - will represent the data bits from the computer via the ODR/OA data transfer mode to the peripheral equipment being serviced by the selected DMS channel.

(2) Peripheral EF - Refer to the word format shown in Figure 134.

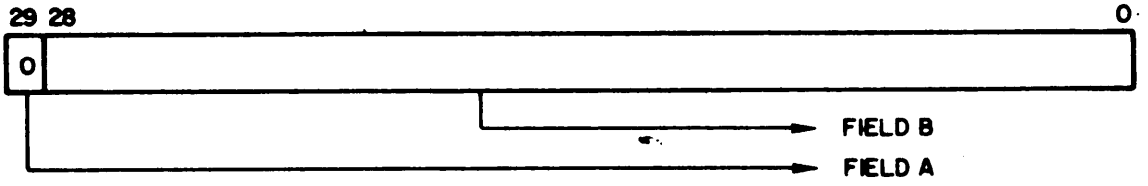


Figure 134. Format of Peripheral E F Word

Field A - Bit 29- EF Identifier code and for this EF it will always equal zero.

Field B - Bit 28 to 0 - will represent data bits from the computer via the EFR/EF data transfer mode peripheral being serviced by the selected DMS channel.

(3) Master Clear EF - Refer to the word format in Figure 135.

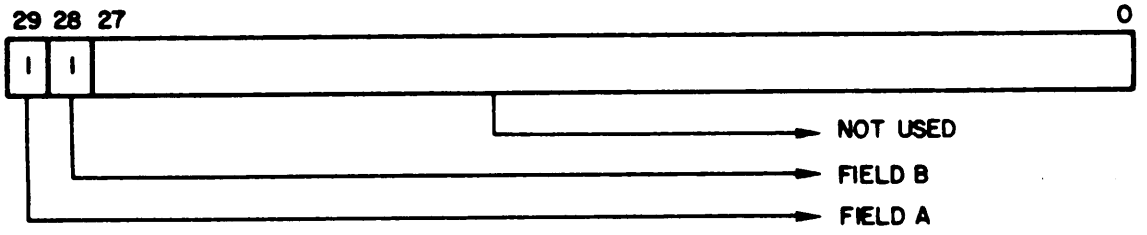


Figure 135. Format of Master Clear EF Word

Field A - Bit 29- EF Identifier code and for this EF it will always equal one.

Field B - Bit 28- Master Clear bit and for this EF it will always equal one.

(4) DMS Instruction EF - Refer to the word format shown in Figure 136.

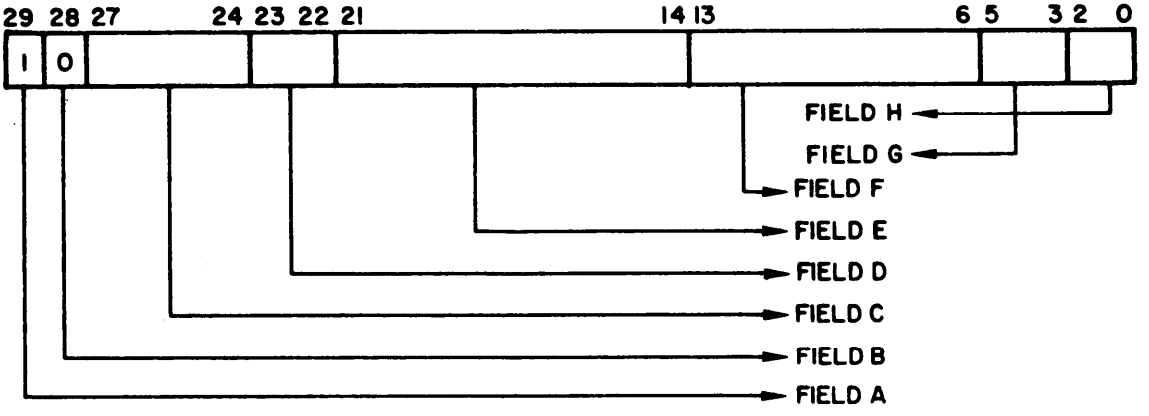


Figure 136. Format of DMS Instruction E F Word

Field A - Bit 29- EF Identifier code and for this EF it will always equal one.

Field B - Bit 28- Master Clear bit and for this EF it will always equal zero.

Field C - Bits 27 through 24- Instruction code shall control DMS operations in accordance with the following tabulation:

DMS INSTRUCTION CODES

BIT 27	26	25	24	DMS OPERATION*
0	0	0	0	No DMS operation
0	0	0	1	Select Input Peripheral per Field H
0	0	1	0	Select Output Peripheral per Field G
0	0	1	1	Select Input and Output Peripheral per Fields H and G
0	1	0	0	Enable Peripheral EI's per Field F
0	1	0	1	Enable XDR Monitor EI's per Field E
0	1	1	0	Enable Peripheral and IDR Monitor EI's per Fields F and E
0	1	1	1	Select Input and Output Peripherals and Enable EI's per Fields H-E
1	0	0	0	Multiplexer Status Request - Bits 23-0 Unused
1	0	0	1	Set DM External Channel Test
1	0	1	0	Reset DM External Channel Test
1	0	1	1	Spare 1 Test-Bits 23-0 available for test data
1	1	0	0	Spare 2 Test-Bits 23-0 available for test data
1	1	0	1	Spare 3 Test-Bits 23-0 available for test data
1	1	1	0	Spare 4 Test-Bits 23-0 available for test data
1	1	1	1	Spare 5 Test-Bits 23-0 available for test data

l For each instruction code only fields specified in this column are used.

Field D - Bits 23 through 22- Unused bits available for word expension.

Field E - Bits 21 through 14- The DMS shall, when instructed in Field C, enable the Peripherals being serviced by the DMS to access the computer via an IDR to an unselected DMS channel in accordance with the following tabulation:

IDR MONITOR EI ENABLE CODES

BIT	DMS CHANNEL NUMBER	FUNCTION
14	0	
15	1	
16	2	
17	3	1 = Enabled
18	4	0 = Not Enabled
19	5	
20	6	
21	7	

Field F - Bits 13 through 6- The DMS shall, when instructed in Field C, enable the peripherals being serviced by the DMS to access the computer via an EI to the peripheral's assigned DMS channel (selected or unselected) in accordance with the following tabulation:

PERIPHERAL EI ENABLE CODES

BIT	DMS CHANNEL NUMBER	FUNCTION
6	0	
7	1	
8	2	
9	3	1 = Enabled
10	4	O = Not Enabled
11	5	
12	6	
13	7	

Field G - Bits 5 through 3 - The DMS shall, when instructed in Field C, select one of the DMS output channels to receive ODR/OA and EFR/EF output data w orals from the computer in accordance with the following tabulation: ‘

OTUPUT DMS CHANNEL SELECT CODES

BIT 5 4 3	DMS CHANNEL NUMBER	AIRCRAFT PERIPHERAL
0 0 0	0	DMS Loop Test
0 0 1	1	Output DM Channel
0 1 0	2	Auxiliary Display Logic
0 1 1	3	Output DM Channel
1 0 0	4	Output DM Channel
1 0 1	5	Output DM Channel
1 1 0	6	Output DM Channel
1 1 1	7	Output DM Channel

Field H - Bits 2 through 0- The DMS shall when instructed in Field C select one of the DMS Input Channels to send IDR/IA input data to the computer in accordance with the following tabulation:

INPUT DMS CHANNEL SELECT CODES

BIT 2 1 0	DMS CHANNEL NUMBER	AIRCRAFT PERIPHERAL
0 0 0	0	DMS Loop Test
0 0 1	1	Input DM Channel
0 1 0	2	Auxiliary Display Logic
0 1 1	3	Input DM Channel
1 0 0	4	Input DM Channel
1 0 1	5	Input DM Channel
1 1 0	6	Input DM Channel
1 1 1	7	Input DM Channel

3.5.4.4.1.6.3 Data Multiplexer Subunit to Computer - Communications between the DMS and the computer shall be in accordance with Appendix I. Data transfer shall be accomplished by the Input Data Request/Input Acknowledge scheme and by the External Interrupt scheme.

3.5.4.4.1.6.4 Computer to Data Multiplexer Subunit - Communications between the computer and the DMS shall be in accordance with Appendix I. Data transfer shall be accomplished by the Output Data Request/Output Acknowledge scheme and by the External Function Request/External Function scheme.

3.5.4.4.1.6.5 Data Multiplexer Subunit to and from Maintenance Control Panel - Communications between the Maintenance Control Panel and the DMS shall be in accordance with 3.5.14.9.

3.5.4.4.1.6.6 Peripheral Equipments (External Interface Logic) and the DMS -

(1) Signal Characteristics - shall be in accordance with Appendix 11 and WR-101, Section IL

(2) All signals between these peripherals and the DMS shall be transmitted over twisted wire pair cables.

(3) DMS Channel Control Functions (EI, IDR, EFR, ODR, EIE, IA, E F and OA). These signals shall be transferred between these equipments per Appendix I if the peripheral device is being serviced by the selected DMS channel. If the DMS channel is not selected, these signals shall be transferred per Appendix I as modified by 3.5.4.4.1.3 with respect to communications with DMS channels not selected.

(4) Data, Input and Output shall be in accordance with Appendix I as modified by 3. 5.4.4.1.3 as to bit quantity.

3.5.4.4.1.6.7 Peripheral Equipments (Internal Interface Logic) and the DMS Signal Characteristics

(1) DMS Channel Control Functions EI, IDR, EFR, ODR, EIE IA, EF, OA and Output Data Signals - same as 3.5.4 .4.1.6. 6(3) and (4) - Output data to these DMS channels shall be transmitted from the MCP.

(2) Spare 1 Test, Spare 2 Test, Spare 3 Test, Spare 4 Test, Spare 5 Tests - Transmitted from the DNB for future expansion.

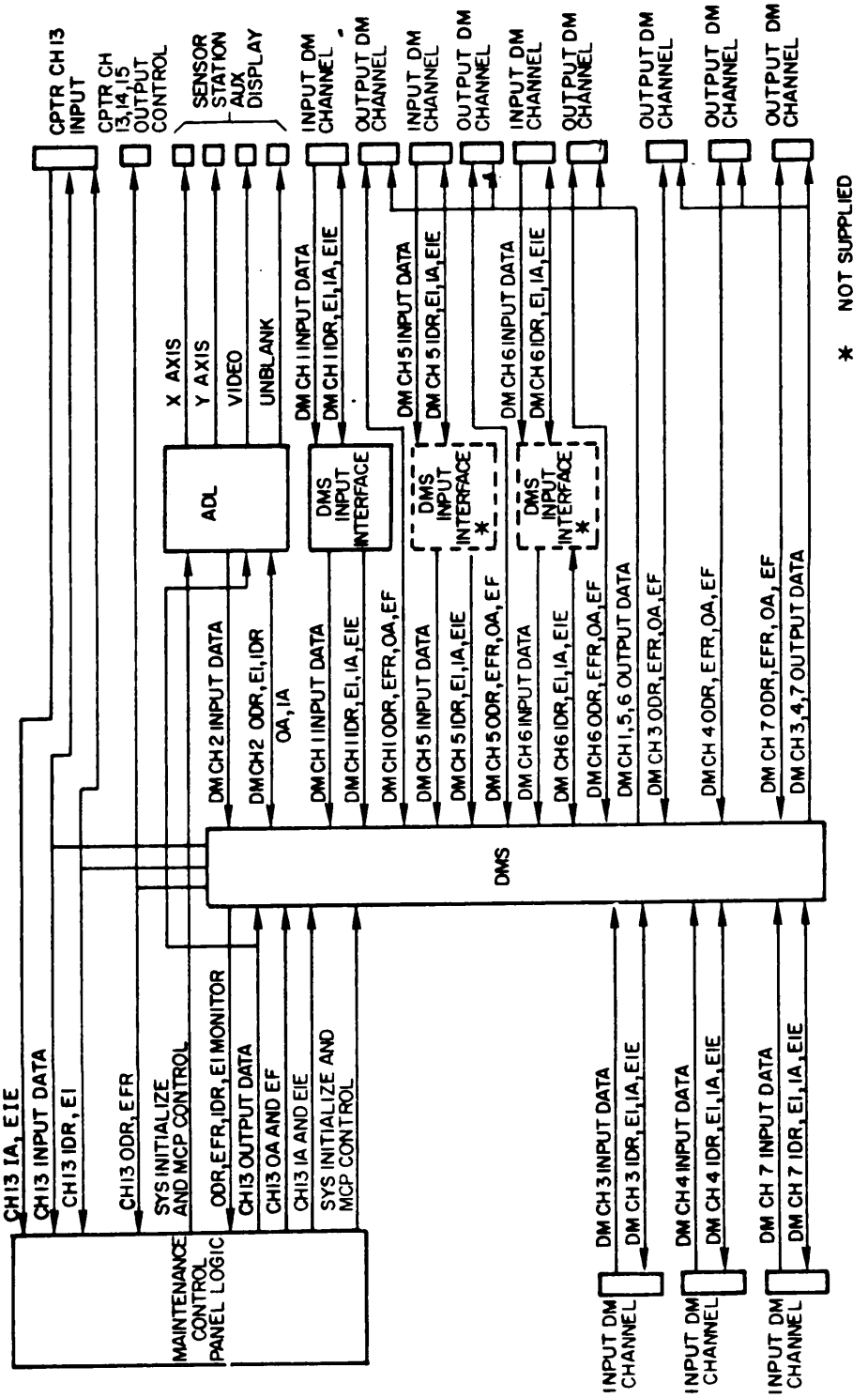


Figure 137. Data Multiplexer Subunit Functional Flow Diagram

3.5.4.4.2 Spare Computer Channel (SCC)

3.5.4.4.2.1 Functional Description - The SCC subunit shall be designed to interface signals between the computer, the Logic Unit 4 MCPL and an external peripheral assigned to computer channel 14.

3.5.4.4.2.2 General Description - The SCC shall provide the capability of transmitting 30 data bits to and from the peripheral assigned to computer channel 14. It shall also provide for transmitting 30 bits to and from the MCPL. The input and output control functions associated with computer channel 14 shall also be interfaced by the SCC.

3.5.4.4.2.3 Operating Requirements

3.5.4.4.2.3.1 Data Transfer - Peripheral Equipment and SCC to Computer- Communications from the SCC to the computer shall be in accordance with Appendix L A peripheral which connects to the computer via the SCC shall be able to transmit up to 30 data bits directly to the computer using Input Data Request/Input Acknowledge or External Interrupt.

3.5.4.4.2.3.2 Data Transfer - Computer to Peripheral Equipment and SCC - Communication from the computer to the SCC and the peripheral equipment shall be in accordance with Appendix L A peripheral which connects to the computer via the SCC shall be able to receive up to 30 data bits from the computer using Output Data Request/Output Acknowledge or External Function Request/External Function.

3.5.4.4.2.4 Timing and Initialization -

(1) The SCC shall not perform any logic function on the peripheral output or input lines that shall delay their transmission to the computer or to the peripheral for more than 1.0 microseconds.

(2) The SCC shall be self-initializing, i.e., when power is applied to the SCC, no Logic 1's shall be transmitted on the SCC control lines to the computer and the SCC shall be ready for normal operation.

3.5.4.4.2,5 Interface Requirements - Refer to Figure 138, the Functional Flow Diagram for the SCC.

3.5.4.4.2.5.1 SCC to Computer

(1) Signal characteristics shall be in accordance with Appendix 11 and WR-101, Section II.

(2) All signals shall be transmitted over twisted pair cables.

3.5.4.4.2.5.2 SCC to and from MCPL - Communications between the Maintenance Control Panel Logic and the SCC shall be in accordance with 3.5.1.4.9.

3.5.4.4.2.5.3 SCC to and from Peripheral Equipment

(1) Signal characteristics shall be in accordance with Appendix 11 and WR 101, Section II.

(2) All signals shall be transmitted over twisted pair cables.

(3) The interface that the SCC presents to the peripheral equipment will be identical to the interface that would be seen at the computer.

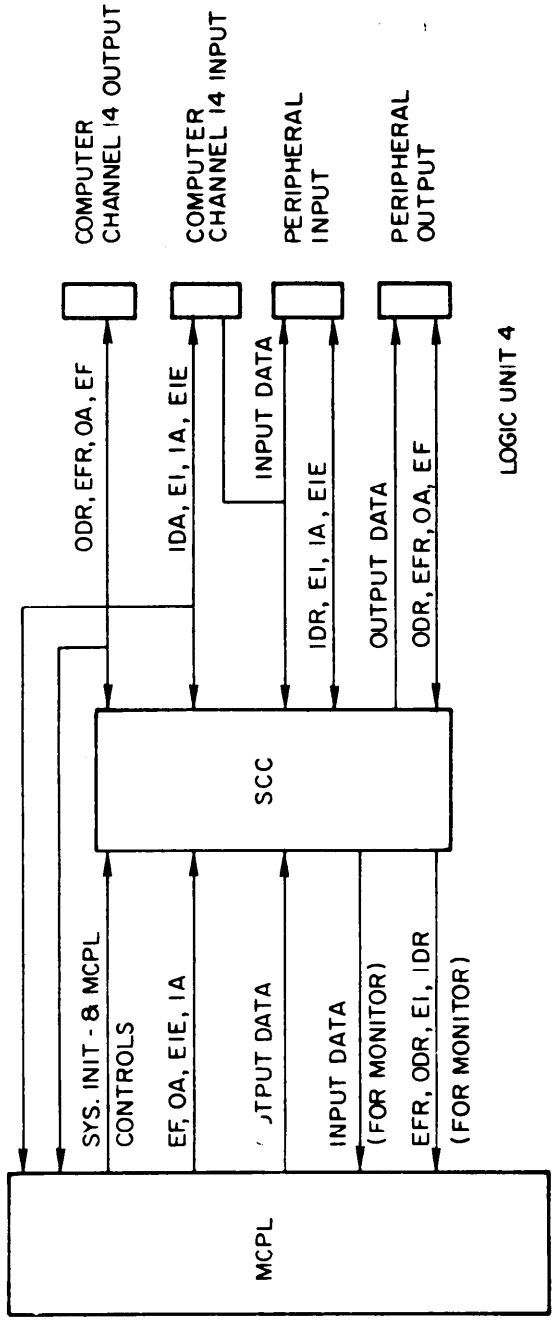


Figure 138. SCC Functional Flow Diagram

3.5.4.4.3 Auxiliary Display Logic

3.5.4 .4.3.1 Functional Description - This subunit provides the interface between the computer and the Auxiliary Display and shall be a DMS channel 2 peripheral. Under computer command, the Auxiliary Display Logic (ADL) provides timing, control, deflection and video signals to control the presentation of functional data on the CRT of the Auxiliary Display.

Figure 139 is a functional flow diagram for the ADL.

3.5.4.4.3.2 General Description

3.5.4.4.3.2.1 Presentation Repertoire - The ADL shall allow the computer to control the presentation of data on the Auxiliary Display. Figure 140 shows the Auxiliary Display and x and y coordinate system in octal code. The data displayed is given in the paragraphs that follow:

(1) Aircraft Symbol with Azimuth Vector - The aircraft symbol to be used will be selected from the available mode 02 symbols of the Character Generator, (see Figure 141). An azimuth vector shall be generated under computer control and have its origin at the center of the aircraft symbol. The Set Position word (Figure 142) shall specify the aircraft position. The ax and a components of the Azimuth Vector word (Figure 144) determine the vector azimuth angle. (See Figure 14?.) This vector shall always have a 4 inch programmed length, but only 1/2 inch of the vector shall be unblanked.

(2) F1y-to-Points - A fly-to-point will consist of a dot with one or two adjacent alphanumeric characters, e. g.,

(3) Vectors - Vector origin, magnitude, and direction are controlled by the computer. All vectors shall be centered about the X, Y coordinate contained in the Set Position word. The magnitude and direction of the vector shall be as defined by the ax and a_y components of the Vector word. Figure 147.

(4) Circles - Circle origin and radius shall be controlled by the computer. The origin of the circle shall be as defined by the X, Y coordinate contained in the Set Position w oral. The radius of the circle shall be as defined by the a_x and a_y components of the Circle word, Figure 145.

(5) Character Repertoire - The Character Generator shall have a full nonambiguous alphanumeric capability with eight special symbols. The codes for alphanumeric characters shall correspond to those shown in Figure 141. The characters presented on the display shall be controlled by the computer.

(6) Flashing Character - A selected symbol or group of characters shall be caused to flash on the CRT under control of a 1 Hz signal (O. 5 second on and 0.5 second off) .

(7) Tabular Information Display - A series of characters, contained in Character words (Figure 143), shall be displayed starting at the X, Y coordinate defined in the Set Position word. This multi-character message shall be terminated by the receipt at the ADL of a new Set Position word, No Operation w oral, EOD w oral, or the 40 Hz sync.

3.5.4.4.3.2.2 Timing - The following tabulation specifies the maximum generation time for the various display functions. The generation time shall initiate at the trailing edge of the second computer Output Acknowledge signal and terminate at the next Output Data Request signal The execution times in the following tabulation are based upon an average character writing time of 35 microseconds and a 15 KHz low pass filter stabilization time of 240 microseconds maximum.

The computer shall refresh the Axuiliary Display, via the Auxiliary Display Logic at a 40 Hz frame rate. The logic shall cease its request for data from the

computer via the DMS upon receipt of an End of Data (EOD) code from the computer (last word in the display buffer). It shall resume requests for data upon receipt of the 40 Hz sync signal. The time between requests for sequential output data shall be in accordance with the timing constraints in the following table. Computer output timing shall be as described for Normal Output Data in Appendix I.

MAXIMUM OPERATION TIMES PER WORD

Operation	Execution Time
Positioning	24 µsec nominal
Circle	550 µsec maximum
Vector	550 µsec maximum
Character (regardless of mode)	140 µsec maximum **
End of Data	5 µsec maximum
No Operation	5 µsec maximum

** l The average Type Character operation time per word shall be less than 95 microseconds.

3.5.4.4.3.3 Operating Requirements - The following is a description of the operational requirements of the ADL.

3.5.4.4.3.3.1 Data Transmission - The ADL shall indicate its readiness to accept data by means of the ODR line being set. Data will be of several categories and thus have unique timing controls for the various modes of operation. Data will be transmitted in two sequential words:

(1) First Transmission -

(a) Four bits denoting Set Position Mode

(b) ‘IWO eight-bit fields containing X and Y positioning

(2) Second Transmission -

(a) Four bits denoting Operation Mode

(b) TWO nine-bit fields containing Command Word Data

3.5.4.4.3.3.2 Function Codes - There are four general types of Function Codes:

(1) Set Position Word - Two eight-bit one’s complement fields for X and Y position.

(2) Circle Plot Word - Two eight-bit fields denoting the circle radius.

(3) Vector or Azimuth Vector Word - Two nine-bit one’s com - plement field X and Y vector components.

(4) Character Plot Word - TWO six-bit fields employed to specify two characters.

3.5.4.4.3.3.3 Diagnostics - The ADL shall provide diagnostic data to the computer. This data shall be initiated by a Diagnostic Instruction word from the DMS. The Diagnostic Instruction word shall be transmitted to the ADL via ODR/OA data transfer mode. The diagnostic data shall be transmitted to the DMS using the IDR/IA mode of data input.

3.5.4.4.3.3.4 Character Generator - The character generator shall utilize the dot method to generate 44 possible characters. A six-bit counter shall generate a pattern of 8 by 8 dot positions through the use of two three-bit D/A converters. The six-bit counter shall also generate timing pulses, which when gated through fixed wired character select gates, enable the video signal to select a desired dot in the pattern. The selected dots comprise the desired character. Figure 146 illustrates the dot method of character generation.

3.5.4.4.3.3.5 Display Synchronization - A 40 Hz synchronization (Sync) pulse generated by the ADL shall synchronously initiate the ADL in order to insure a jitter free display. When this occurs the logic shall transmit an ODR and an EI to the DMS. If enabled in the DMS the ADL EI will be transmitted to the computer. The computer may then select DMS output channel 2 and transmit output data to the ADL in response to an ADL ODR. Normal operation shall continue until an EOD at which time the ODR shall remain at a logic "0" until the next cycle of the 40 Hz sync.

3.5.4.4.3.3.5.1 Sync Control - The ADL shall generate 40 Hz sync pulses continuously when the DMS is not in a test mode. With the DMS in an MCP test mode, the sync generation shall be under the control of the MCP sync switch. The sync switch shall dictate to the ADL whether to generate 40 Hz sync pulses:

(1) Continuously

(2) Singularly

(3) None

3.5.4.4.3.3.6 Circle and Vector Generation - Circle and vector generation shall be performed by logically controlling the phase and amplitude the X and Y output signals. A sine- cosine generator shall provide a 12 KHz modulation source which shall operate in conjunction with the X and Y conic D/A converters to obtain amplitude modulated square waves. Square wave signals shall then be passed through low-pass filters to obtain amplitude modulated sinusoidal functions.

3.5.4.4.3.3.7 Type Mode - The ADL shall generate, under computer control, a sequence of characters which shall represent a typewriter page. This mode of operation shall require the computer to generate a series of code 04 w orals, each word consisting of two character codes. The ADL shall automatically increment its X Gross Position Register such that the characters are on 1/4 inch spacing. The incrementing shall continue until the computer sends a new Set Position word or EOD word. If the computer fails to terminate the X deflection incrementing, the ADL shall automatically cease incrementing when the X gross position register reaches its maximum deflection state.

3.5.4.4.3.3.8 Test Modes - The ADL operation shall be verified by utilizing the MCP for synthesis of various computer command words. The MCP shall provide simulated computer output words in three different operating modes:

(1) Single - The MCP shall transmit a manually programmed one output word when the operator depresses a momentary switch.

(2) Repetitive - The MCP shall continuously transmit a manually programmed word at the ADL's maximum rate for the function specified in the data w oral.

(3) Synchronous - The MCP shall output a manually programmed word at a fixed rate of 40 Hz which shall be locked to the 400 Hz line.

3.5.4.4.3.3.9 Initialization - The ADL shall be self initializing, i. e., when power is applied, no logic "1" shall be transmitted on the ADL control lines to the DMS and the ADL shall be ready for normal operations. The ADL shall also initialize at the 40 Hz sync pulse time.

3.5.4.4.3'4 Interface Requirements - See functional flow diagram, Figure 139.

3.5.4.4.3.4.1 General

3.5.4.4.3.4.1.1 Maintenance Control Panel Logic to Auxiliary Display Logic - The ADL shall receive the following signals from the MCPL.

(1) Output Data - Data words which will be received from the computer via the MCPL shall command the timing, control, deflection, diagnostic instruction, and video signals for the ADL. These signals will be a 30-bit data word and will adhere to the word formats shown in Figures 142 through 146.

(2) Clocks - The MCPL shall transmit the 1.536 MHz clock and 400 Hz clock signals to the ADL. The 400 Hz clock shall be derived from the AC 400 Hz Logic Unit 4 Input Power.

(3) Sync Control - The MCP sync switch shall Provide two signals to the ADL:

(a) Continuous Sync

(b) Single Sync

(4) ON LINE - The MCPL shall provide a signal to the ADL which shall inform the ADL that computer channel 13 is in an MCP test mode.

3.5.4.4.3.4.1.2 Data Multiplexer Subunit to Auxiliary Display Logic - The ADL will receive two computer acknowledge signals from the DMS.

(1) Output Acknowledge - The DMS channel 02 Output Acknowledge signal will indicate data on the output data lines is ready for sampling by the ADL.

(2) Input Acknowledge - The DMS channel 02 Input Acknowledge signal will indicate the computer has sampled the ADL IDR or EI word.

3.5.4.4.3.4.1.3 Auxiliary Display Logic to the Data Multiplexer Subunit - The ADL shall send the following signals to the DMS:

Input Data - The ADL shall transmit Diagnostic data to the computer via the DMS using the IDR/IA mode of data transfer.

(2) Computer Requests - The DMS shall receive an Input Data Request Signal from the ADL when the ADL has Input Data available. The ADL shall generate an Output Data Request (ODR) to the DMS when it is ready to accept diagnostic instruction or display data.

(3) External Interrupt - The ADL shall transmit an External Interrupt signal to the DMS whenever the 40 Hz sync pulse is generated in the ADL.

3.5.4 .4.3.4.1.4 Auxiliary Display Logic to Auxiliary Display

(1) "X' and "Y" Full Scale Deflection - Circuitry in the ADL shall be capable of accepting digital data that describes positions, straight lines, circles, and characters. This data shall generate waveforms which shall be transmitted to the horizontal and vertical deflection circuits of the Auxiliary Display. The signal level shall be from O to between ±6 to ±8 volts peak amplitude for a beam deflection of one radius. Step settling time for the Auxiliary Display shall be no greater than 18 microseconds for full screen deflection. The sinusoidal signals for vector and circle functions shall be 12 KHz, and character deflection axis bandwidth products shall be 110 KHz minimum.

Circuits shall be provided in the ADL that shall limit the summation of the character signals, sinusoidal signals. and positioning signals from exceeding one display radius along any coordinate axis in order to prevent overdriving the display deflection amplifiers. Limiting of the maximum allowable X and Y deflection signals shall be at X and Y deflection amplitude values of +6 to +8 Vdc +10% -0%.

(a) Accuracy Under Nominal Conditions -Nominal conditions are defined as the temperature range of 10°C to 40°C, and the range of input power within the bounds of Limits 2 and 3 of 'Figure 3, MIL-STD-704 as modified by 3.3.12.1. Accuracies under these conditions shall be as follows:

1. The X and Y total harmonic distortion of the sinusoidal conic generation signals shall be less than 1%.

2. The phase difference between X and Y sinusoidal conic generation signals shall be less than one degree.

3. A change in the digital signal shall produce a corresponding change in the analog signal within one LSB.

4. The magnitude accuracy of X relative to Y shall be less than +1%.

5. The absolute accuracy of X or Y shall be less than +2%.

(b) Accuracy Under Extreme Conditions_ - Extreme conditions shall be as defined in 3.3.10. Accuracies under these conditions shall be as follows:

1. The X or Y total harmonic distortion of the sinusoidal conic generation signals shall be less than 2%.

2. The phase difference between the X and Y sinusoidal conic generation signals shall be less than 2°.

3. A change in the digital signal shall produce a corresponding change in the analog signal within one LSB.

4. The magnitude accuracy of X relative to Y shall be less than +2%.

5. The absolute accuracy of X or Y shall be less than +4%.

(2) 'Z" Axis Video - Positive going video signals shall be DC coupled to the video amplifier of the Auxiliary Display for intensity modulation of the CRT. Video amplitude shall be proportional to writing speed.

(3) Unblank - The ADL shall provide a positive going voltage level to the Auxiliary Display for unblinking the CRT. The unblank signal shall have the same duration as the video signal, but shall have constant amplitude.

3.5.4.4.3,4.2 Output Signal Characteristics

3.5.4.4.3.4.2.1 Auxiliary Display - The ADL input/output signals to and from the Auxiliary Display shall be as follows:

3.5.4.4.3.4.2.1.1 Triaxial Transmissions - All signals to the Auxiliary Display shall be transmitted via Amphenol 421-033 cable or equivalent terminated in a differential amplifier whose input impedance shall be 90 to 95 ohms and 100 pf maximum. The coaxial cable shall not exceed 100 feet.

(1) X and Y Deflection Signals -The X and Y deflection signal characteristics shall be as described in 3.5.4.4.3.4.1.471 . Transition times for gross positioning signals shall be less than 4.0 microseconds.

(2) "Z" Axis Video - This signal shall be positive going from O to between 2.0 to 2.5 volts peak. The video signal shall provide the following voltage levels in order to obtain uniform brightness on the CRT for conic and character generation.

(a) Conic

Video voltage +5%	%-Maximum radius displayed
50% X Maximum voltage	0 - 25%
65% X Maximum voltage	26- 50%
80% X Maximum voltage	51- 75%
Maximum voltage	76- 100%

(b) Character

Character Video Voltage = 50% x Maximum Voltage +5%.

(3) Unblank - This signal shall be 5.0 +1.5 volts with a rise time and fall time not to exceed 100 nanoseconds when measured at the 10% and 90% amplitude points.

3.5.4.4.3.5 Word Formats - The Auxiliary Display Logic word formats are shown in Figures 142 through 146. There will be four basic types of word formats used in the ADL as follows:

(1) Display Instruction Word - An ODR word to the ADL indicating a display function.

(2) Diagnostic Instruction Word - An ODR word to the ADL instructing the ADL to execute a diagnostic test mode.

(3) Diagnostic Data - An IDR word to the DMS containing diagnostic data as a result of a Diagnostic Instruction Word.

(4) Frame Start - An EI word to the computer via the DMS indicating the occurrence of a 40 Hz sync pulse.

3.5.4.4.3.5.1 Output Word Format - The Auxiliary Display Logic shall be capable of recognizing a display instruction word or diagnostic instruction word formats. All of these programming words will be of 30 bit lengths. with bit "29" being the Most Significant Bit (MSB) and bit "0" being the Least Significant Bit (LSB). Not all of the data bits contained in the instruction words will be used.

3.5.4.4.3.5.1.1 Display Instruction Word - Figures 142 through 145 show the digital display instruction word formats. In all of these words bit 14 will be a logic 0 indicating a display instruction word and not a diagnostic instruction word. Bits 26 through 29 in all of the display words will define the display function. The list of display actions defined by the various function codes is shown in the following tabulation:

Function Code Bits					Function Performed
	Binary				
octal	29	28	27	26	
00	0	0	0	0	No Operation
01	0	0	0	1	Set Position - Location Beam
02	0	0	1	0	Print 1 character - No 2nd character
03	0	0	1	1	Print 2 characters and Point
04	0	1	0	0	Print characters - No Point (Type Format)
05	0	1	0	1	Display Vector
06	0	1	1	0	Display Azimuth Vector
07	0	1	1	1	Display Circle
10	1	0	0	0	EOD
12	1	0	1	0	Identical to Code 02 but Flashing
13	1	0	1	1	Identical to Code 03 but Flashing
14	1	1	0	0	Identical to Code 04 but Flashing

3.5.4.4.3.5.1.1,1 No Operation - Function Code 00- When a word containing this code is received from the computer, the Auxiliary Display Logic shall inhibit the normal processing of the word and request a new computer word.

3.5.4.4.3.5.1.1.2 Set Position Word - Function Code 01 - The Set Position word, Figure 142, will contain the "X and Y components of the positioning data for all vectors, circles, and characters. The X componet is contained in bits 15 through 22, where bit 22 is the MSB and bit 15 the LSB. The Y component is contained in bits 0 through 7, where bit 7 is the MSB and bit O the LSB. The eight binary bits of horizontal deflection data and eight binary bits of vertical deflection data shall be utilized to define a Cartesian coordinate system with the origin at the center of the display. All of the X and Y coordinate data will be expressed in the one's complement system. The maximum positive deflection for the 7.6 inch usable diameter of the 9-inch diameter CRT is defined by 177 in the octal code; the maximum negative deflection is defined as 200 in the octal code (see Figure 140). The use of the eight binary bit magnitude in conjunction with the 8-inch usable CRT diameter will provide a plotting position selection capability of approximately 0.0312 inch apart.

3.5.4.4.3.5.1.1.3 Character Word - A character word, Figure 143, will contain one or two character data codes, C_1 and C_2, plus the Character Function Code. The Character Function Code will describe the manner in which this Character Word is to be processed. . Character 2 will be contained in bits 15through 20 with bit 20 as the MSB and bit 15 as the LSB. Character 2 will be contained in bits O through 5, with bit 5 as the MSB and bit 0 as the LSB.

(1) Function Code (02) - This will be a one character message pertaining only to special characters. A point shall first be plotted at the X, Y position contained in the previous positioning word, and one of the special characters shall then be drawn with its center at this point. The second character will always be blank in this mode of operation. Special characters will be defined by codes 0.0, 13, 14, 15, 16, 17, 41 and 44.

(2) Function Code (03) - This will be a one character word message which indicates a point is to be plotted at the X, Y position defined in the previous position word. The leading edge of the first character will be drawn O. 25 inch to the right of this point. When only the second character is to be displayed, its leading edge will be O. 5 inch from the point.

(3) Function Code (04) - This code will signify that a multi-character message is to be processed (Type Format). The lower left hand corner of the initial character will be O. 25 inch to the right of the X, Y position defined in the previous positioning word, or previous word containing a Function Code 04.

3.5.4.4.3.5.1.1.4 Vector Word - The Vector Word (Figure 144) will contain the data necessary to define both the normal vector and azimuth vector. The X component of the vector will be contained in bits 15 through 23, with bit 23 as the MSB and bit 15 as the LSB. The Y component will be contained in bits O through 8, with bit 8 as the MSB, and bit 0 as the LSB.

(1) Function Code (05) - This code will signify that the data accompanying the code will define a vector. The center of the vector will be defined by the X, Y coordinates contained in the previous word. Both a_x and a_y will be 9 bit, one's complement quantities. The LSB = 1/2 set position bit.

(2) Function Code (06) - This code will be used when an aircraft heading vector is to be displayed. The X, Y coordinates contained in the previous word will be that of the aircraft. A four-inch vector whose angular orientation is that of the aircraft heading vector will be programmed in the accompanying data. The resultant displayed vector shall be one-half inch long, originating from the Aircraft Symbol, and extending in the programmed direction. A Function Code (06) shall be able to follow a Function Code (02) without regenerating a new Set Position word (Function Code (01)).

3.5.4.4.3.5.1.1.5 Circle Word - Function Code (07) - The Circle word, Figure 145, will contain the necessary data for defining a circle. The radius defining this circle will be contained in bits O through 7 and 15 through 22, with bits 7 and 22 as the MSB's and bits 0 and 15 as the LSB's. This word will specify a circle centered on the X, Y coordinates contained in the previous Positioning word. The radius in this word will always be an eight-bit, positive quantity, where 377 in the octal code represents one display diameter. The binary equivalent for radius will be identical in both halves of the data word.

3.5.4.4.3.5.1.1.6 End of Data Word - Function Code (10) - This code will indicate the End of Data (EOD) from the computer during a particular 25 millisecond frame. If the EOD word is not received the Auxiliary Display, upon reinitialization, shall continue to display the remaining buffer information during the next 25 millisecond frame.

3.5.4.4.3.5.1.1.7 Flashing Character - Function Codes (12), (13), and (14) - Codes (12), (13), and (14) will signify that all character data accompanying codes (02), (03), and (04), respectively, shall be displayed in the Flashing Mode. Flashing shall be accomplished by displaying the information for one-half second, and then preventing the display of this information for the next half second, by inhibiting the Z axis (video) output.

3.5.4.4.3.5.1.1.8 Character Size - The ADL shall provide controls which will enable an operator to continuously vary the size of the characters displayed. Character height and width shall be continuously adjustable from 1/8 to 1/4 inch.

3.5.4.4.3.5.1.2 Diagnostic Instruction Word - The Diagnostic Instruction Word will be indicated by a logic "l" in bit 14. The remaining bits will be used to describe the diagnostic test mode as needed (Figure 146).

3.5.4.4.3.5.2 Input Word Formats - The Auxiliary Display Logic shall generate frame start and diagnostic data words to the computer via the DMS.

3.5.4.4.3.5.2.1 Frame Start - The frame start word as described in 3.5.4.4.3. 5(4) shall contain no data on the input data lines.

3.5.4 .4.3.5.2.2 DMS CH 2 Input Data - 30 input data bits will be available for diagnostic data input to the computer via the DMS.

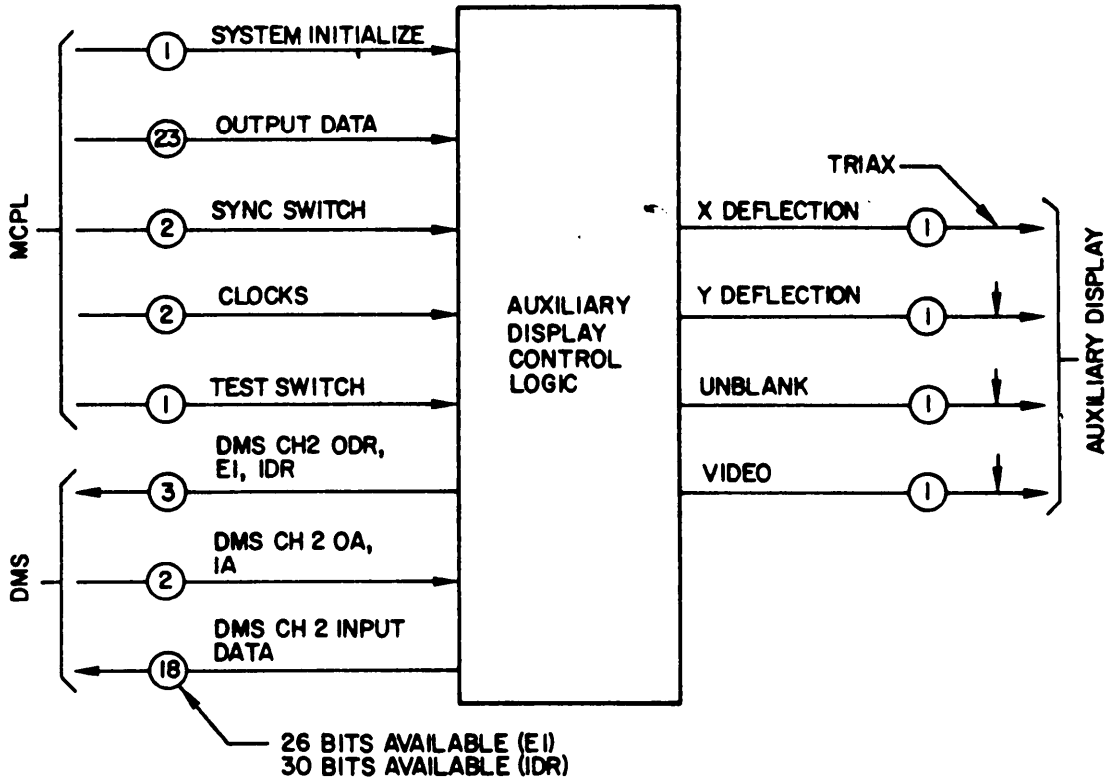


Figure 139. Auxiliary Display Logic, Functional Flow Diagram

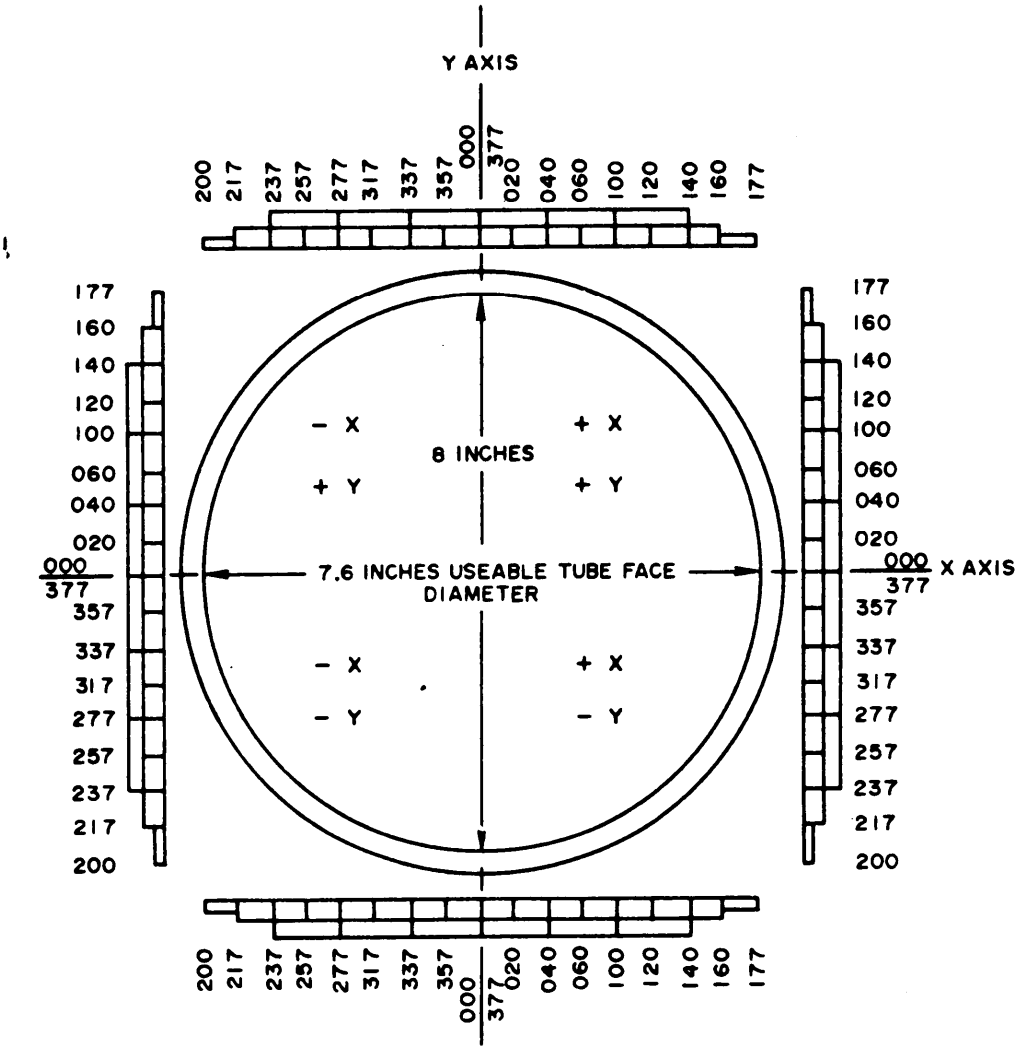


Figure 140. Auxiliary Display X and Y Coordinate System in Octal Code

CODE	CHAR
00	BLANK
01	1
02	2
03	3
04	4
05	5
06	6
07	7
10	8
11	9
12	0
13	-
14	⋈
15	⊠

CODE	CHAR
16	⊡
17	⊟
40	D
41	+
42	N
44	X
50	R
51	S
52	A
53	B
54	C
55	E
56	F
57	G
60	H

CODE	CHAR
61	I
62	J
63	K
64	L
65	M
66	P
67	Q
70	T
71	U
72	V
73	W
74	X
75	Y
76	Z
77	+

Figure 141. Auxiliary Display Character Repertoire

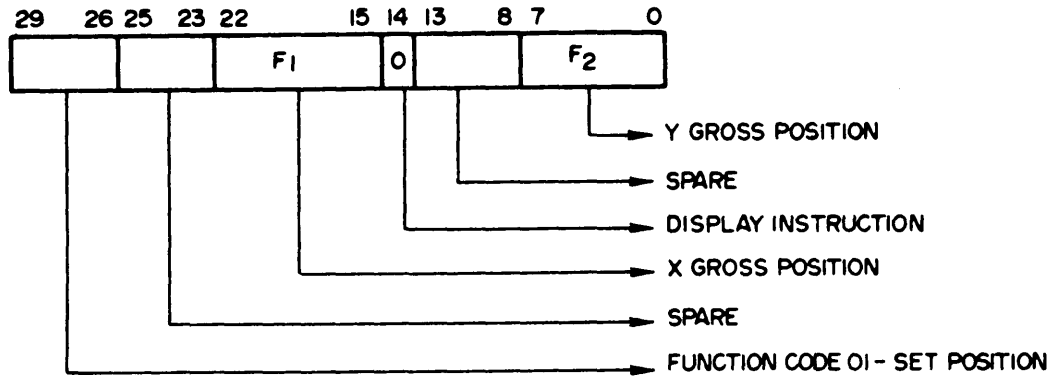


Figure 142. Format for Auxiliary Display Set Position Word

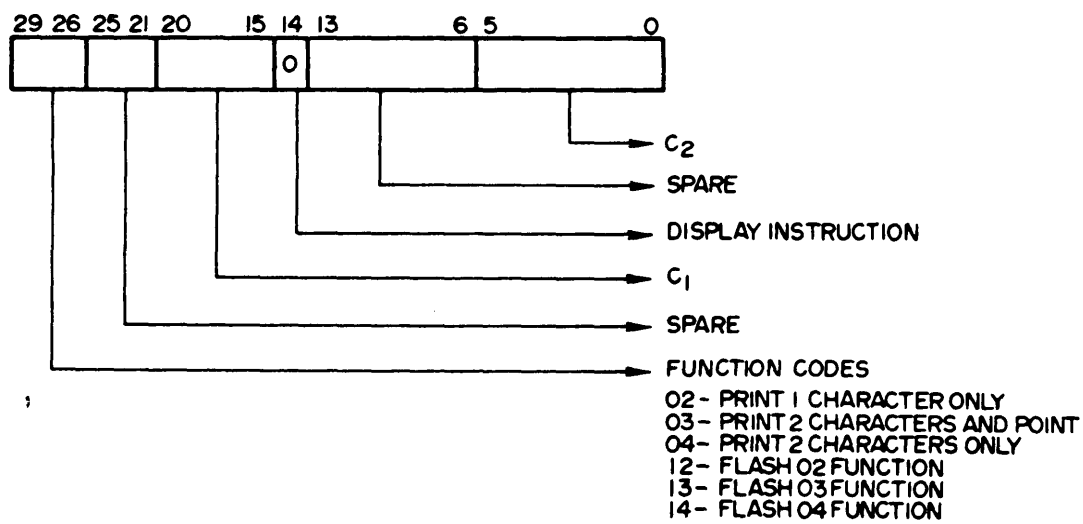


Figure 143. Format for Auxiliary Display Character Plot Word

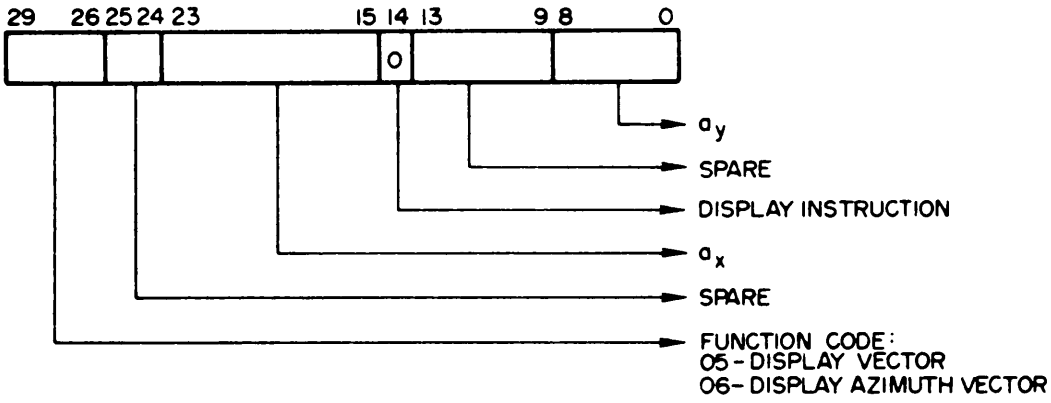


Figure 144. Format for Auxiliary Display Vector or Azimuth Vector Word

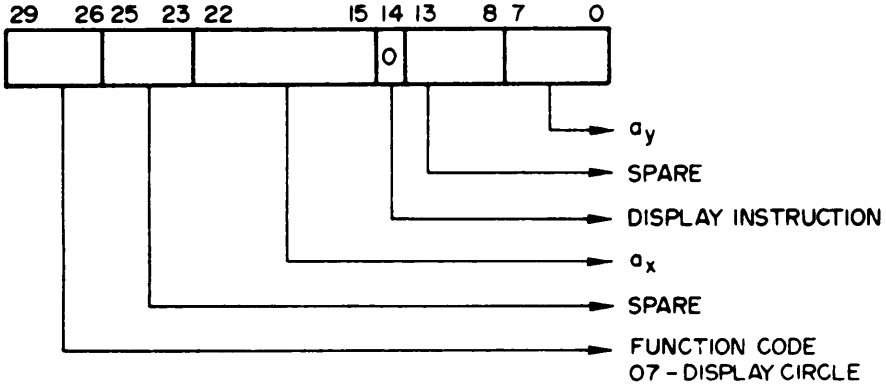


Figure 145. Format for Auxiliary Display Circle Plot Word

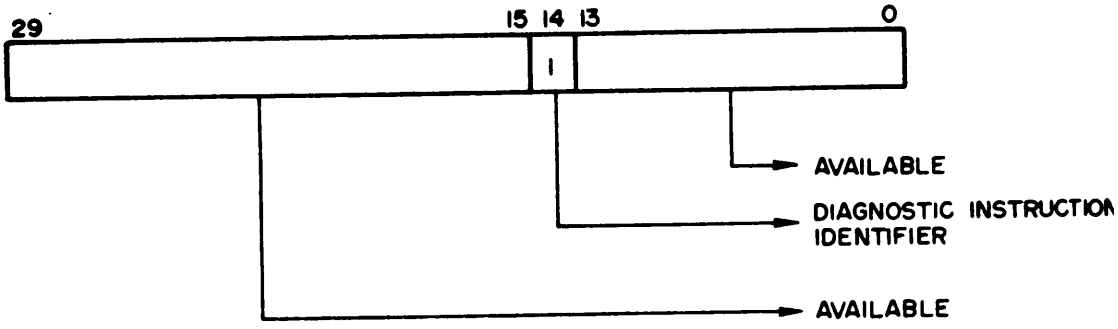


Figure 146, Format for Auxiliary Display Logic Diagnostic Instruction Word

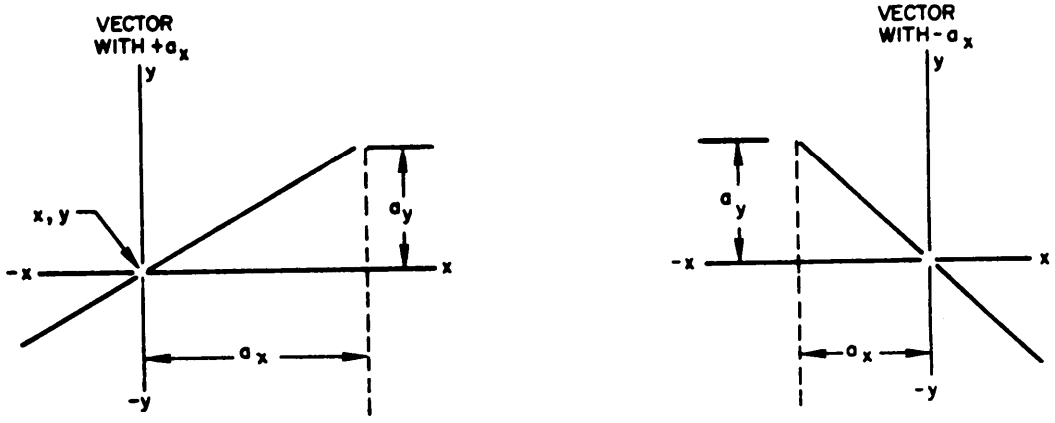


Figure 147. 155 Vector Definition

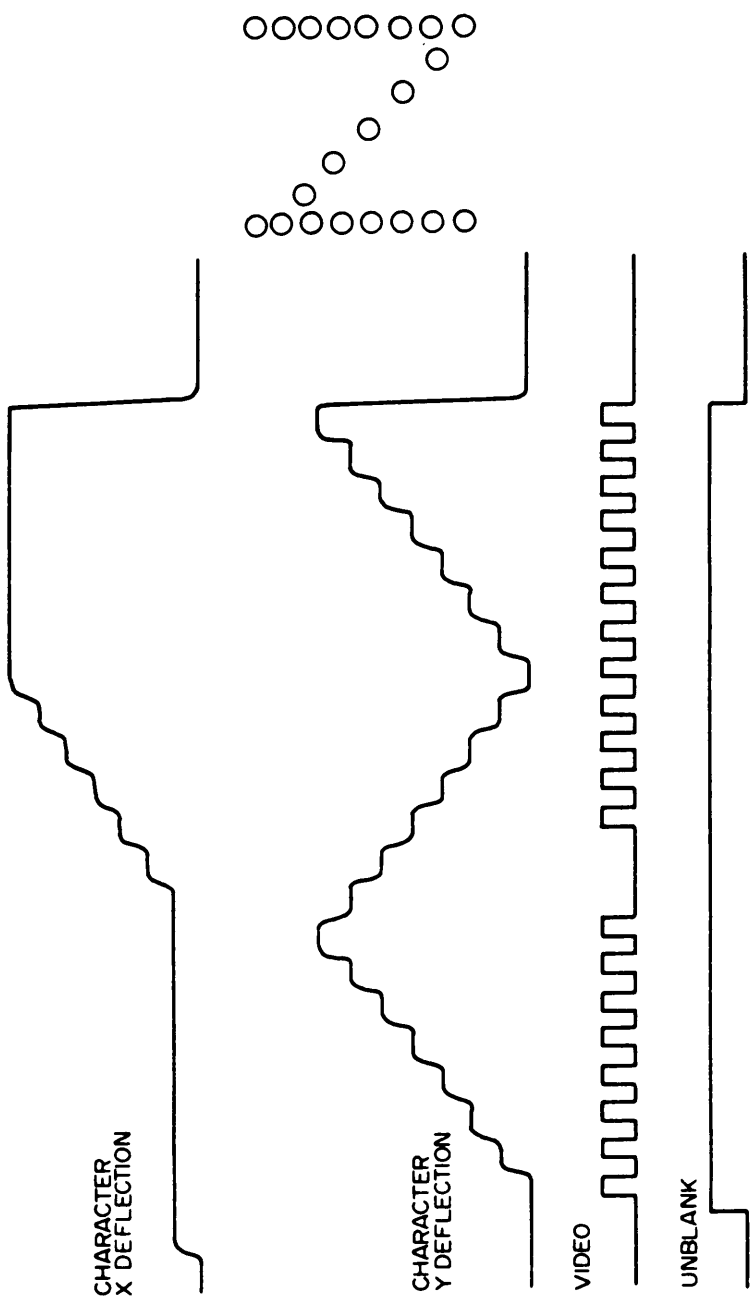


Figure 148. Sequential Dot Method of Character Generation

3.5.4.4.4 Drum Auxiliary Memory Subunit (DAMS)

3.5.4.4.4.1 General Functional Requirements

The block diagram for the Drum Auxiliary Memory Subunit (DAMS) is shown in Figure 151. The DAMS contains the Magnetic Drum Memory (MDM) and the Drum Controller. The DAMS shall receive control and data signals from the Computer via the MCP and shall transmit control and data signals to the Computer and to the MCP. Manual test operation of the DAMS shall be accomplished by placing the DAMS in the Off Line mode via the MCP. The DAMS shall meet the following general performance requirements.

3.5.4.4.4.1.1 Capacity

The DAMS shall be capable of storing a minimum of 196,608 and a maximum of 393,215 computer words (30 bits each). Each data track of the MDM shall be capable of storing 1024 computer words with the exception of the initial data track that is addressed. The initial data track shall be capable of a maximum of 1023 computer w orals and an MDM preamble word which shall precede the computer words.

3.5.4.4.4.1.2 Word Transfer Rate

The average data word transfer rate between the computer and the DAMS of Logic Unit 4 shall not be greater than 60K words/second nor less than 30K words, ‘second.

3.5.4.4.4.1.3 Access Time

The time to access the location of and read/write the first data word shall not exceed 30 milliseconds.

3.5.4.4.4.1.4 Error Rate

The error rate during read/write operations shall not exceed a single error in 10^{10} bits transferred to or from the DAMS. A single error is defined as any bit or combination of bits being incorrect in a 30 bit data word transferred between the DAMS and the computer.

3.5.4.4.4.1.5 Memory Protection

It shall be possible to protect the drum memory from writing in a protected area by means of memory protect switches and Computer command. For memory protect purposes, the memory shall be divided into blocks of 32, 768 consecutively addressable word locations.

3.5.4.4.4.1.6 System Initialization

Power to the DAMS shall be applied by means of the POWER ON/ OFF switch. During power initialization, the DAMS shall not transmit a Logic 1 on its Computer Control lines.

3.5.4.4.4.2 Drum Controller Requirements

The Drum Controller shall provide the interface for data handling and control purposes between the Magnetic Drum Memory and the Computer/MCP. The functional flow diagram for this interface is shown in Figure 152. The basic requirements of the Drum Controller shall be to provide the timing, control, and data handling logic needed for execution of the instructions from the Computer. The following paragraphs describe, in general terms, the basic requirements of the Drum Controller.

3.5.4.4.4.2.1 Instruction Execution

The Drum Controller shall contain the logic necessary for execution of the following set of instructions for the computer:

(1) Write

(2) Read

(3) Master Clear

(4) Read/Write Terminate

(5) status

(6) Memory Protect

(7) Test

3.5.4.4.4.2.2 Data Block Length

The Drum Controller shall provide the capability for writing or reading data from any continuous set of memory addresses where the data block size may be any number from 1 to 393,215 words.

3.5.4.4.4.2.3 Data Buffers

The Drum Controller shall contain dual 32 word data buffers for the purpose of accommodating the differences in data rates and timing between the Computer and the Magnetic Drum Memory.

3.5.4.4.4.2.4 Parity

The Drum Controller shall generate parity bits for each data word received from the Computer. During write operations, the parity shall be checked as the data leaves the buffers and as it enters the Magnetic Drum Memory. During read operations, the parity shall be checked as the data is received from the Magnetic Drum Memory and as it leaves the buffers.

3.5.4.4.4.2.5 Status

The Drum Controller shall detect and retain data pertinent to the status of the Magnetic Drum Memory and conditions internal to the Drum Controller and provide a status word to the computer for each operational instruction executed by the Drum Controller.

Following Power Turn On, System Initialization, or an Instruction Status Interrupt indicating Clock Error, Track Select Error, Power Fault, Speed Error, or Clock Loss, no EFR shall be sent to the Computer until a No Error Status condition is detected on the Clock Error, Track Select Error, Power Fault, Speed Error, and Clock Loss Signal Lines. A Drum Error signal is defined as the logic “OR” of the Clock Error, Speed Error, Track Select Error, Power Fault, Temperature Error, and Clock Loss Error Signals. This signal shall be monitored and, when it changes from no error to error, an interrupt to the Computer with the instruction status word shall be generated at a time when the Drum Controller is not actively executing an instruction.

3.5.4.4.4.3 Magnetic Drum Memory

3.5.4.4.4.3.1 General - The Magnetic Drum Memory (MDM) shall be a light-weight medium capacity magnetic drum memory system which provides a digital interface to the drum cent roller. The Magnetic Drum Memory shall meet the following requirements.

3.5.4.4.4.3.2 Functional Operations - The functional operations within the MDM fall into three categories - write operations, read operations, and test operations. These are described in detail in 3.5.4.4.4.3.3.4.1.

3.5.4.4.4.3.3 Requirements

3.5.4.4.4.3.3.1 Parts and Materials - In the selection of parts and materials, fulfillment of major design objectives shall be the prime consideration. In so doing, those objectives outlined in 3.2 shall govern.

3.5.4.4.4.3.3.2 Design and Construction - The MDM shall conform with all applicable requirements of Specification MIL-E-5400 for design, construction and workmanship, except as otherwise specified herein.

3.5.4.4.4.3.3.2.1 Weight - The total weight of the MDM, including cables, shall be a minimum consistent with good design and such as to permit the total Logic Unit 4 weight to meet the requirement of 3.3.1. To achieve this, a total weight of 85 pounds shall be considered a design objective.

3.5.4.4.4.3.3.2.2 Reliability - The reliability program for the MDM shall be in accordance with 3.3.2.1.

3.5.4.4.4.3.3.2.2.1 Operational Stability - The MDM shall operate with specified performance continuously or intermittently for a period of at least 10, 000 hours without the need for servicing other than replacement of failed components.

3.5.4.4.4.3.3.2.2.2 Operating (Service) Life - The MDM shall have a total operating life of at least 50,000 hours with reasonable servicing and replacement of parts.

3.5.4.4.4.3.3.2.2.3 Specified Mean-Time-Between Failures (MTBF) - The Mean-Time- Between Failures for the MDM shall be such as to allow Logic Unit 4 to meet its specified MTBF as stated in paragraph 3.3.2.4. To provide assurance that this requirement can be readily achieved, a design goal of 4500 hrs shall be allocated to the MDM.

3.5.4.4.3.3.2.3 MDM Connectors - Power and signal connectors at the interface between the MDM and Logic Unit 4 shall be in accordance with the requirements of MIL-C-81511.

3.5.4.4.4.3.3.2.4 Control Panel - The front panel of the MDM shall be an integral part of the assembly and shall contain switches, controls, indicators and an air filter.

3.5.4.4.4.3.3.2.5 Interchangeability - The MDM shall meet the interchangeability requirements of Specification MIL-E-5400.

3.5.4.4.4.3.3.2.6 Interference Control - When installed in the Logic Unit en-closure, the generation of electromagnetic interference by the MDM and the susceptibility of the equipment to electromagnetic interference shall be such as to permit Logic Unit 4 to meet the test requirements given in 4.2.2.2. To achieve this the design goals for the MDM for Electromagnetic Interference shall be as follows:

3.5.4.4.4.3.3.2.6,1 Power Line Conducted-Current Probe-Broadband and PCW Limit - The upper limit for this requirement shall be as follows:

(1) A straight line drawn from the point 30 Hz and 148 DB ua/MHz to 20 KHz and 148 DB ua/MHZ.

(2) A straight line drawn from the point 20 KHz and 148 DB ua/MHz to 50 KHz and 131 DB ua/MHz.

(3) A straight line drawn from the point 50 KHz and 131 DB ua/MHz to 2 MHz and 50 DB us/MHz.

(4) A straight line drawn from the point 2 MHz and 50 DB ua/MHz to 25 MHz and 50 DB ua/MHz.

3.5.4.4.4.3.3.2.6.2 Power Line Conducted- Current Probe- Narrowband Limit - The upper limit for this requirement shall be as follows:

(1) A straight line drawn from the point 30 Hz and 125 DB/ua to 1 KHz and 125 DB/ua.

(2) A straight line drawn from the point 1 KHz and 125 DB/ua to 50 KHz and 77 DB/ua.

(3) A straight line drawn from the point 50 KHz and 77 DB/ua to 2 MHz and 10 DB/ua.

(4) A straight line drawn from the point 2 MHz and 10 DB/ua to 25 MHz and 10 DB/ua.

3.5.4.4.4.3.3.2.6.3 Radiated Interference-Antenna Induced (AI) Broadhand and PCW Limit - The upper limit for this requirement shall be as follows:

(1) A straight line drawn from the point 0.15 MHz and 91 DB uv/MHz to 0.5 MHz and 84 DB uv/MHz.

(2) A straight line drawn from the point 0.5 MHz and 84 DB uv/MHz to 25 MHz and 80 DB uv/MHz.

(3) A straight line drawn from the point 25 MHz and 44 DB uv/MHz to 35 MHz and 50 DB uv/MHz.

(4) A straight line drawn from the point 35 MHz and 50 DB uv/MHz to 70 MHz and 52 DB uv/MHz.

(5) A straight line drawn from the point 70 MHz and 61.5 DB uv/MHz to 150 MHz and 63.5 DB uv/MHz.

(6) A straight line drawn from the point 150 MHz and 54.4 DB uv/MHz to 1000 MHz and 60.5 DB uv/MHz.

3.5.4.4.4.3.3.2.6.4 Radiated Interference-Antenna Induced (AI) Narrowband Limit - The upper limit for this requirement shall be as follows:

(1) A straight line drawn from the point 0.15 MHz and 37 DB uv to 3 MHz and 37 DB uv.

(2) A straight line drawn from the point 3 MHz and 37 DB uv to 25 MHz and 40 DB uv.

(3) A straight line drawn from the point 25 MHz and 30 DB uv to 35 MHz and 38 DB uv.

(4) A straight line drawn from the point 35 MHz and 38 DB uv to 300 MHz and 51.5 DB uv.

(5) A straight line drawn from the point 300 MHz and 32.5 DB uv to 1000 MHz and 40 DB uv.

3.5.4.4.4.3.3.2.6.5 Radiated Interference-Antenna Induced (AI) Broadband Limit-Rod Antenna - The upper limit for this requirement shall be a straight line drawn from the point 15 KHz and 109 DB uv/MHz to 150 MHz and 91 DB uv/MHz.

3.5.4.4.4.3.3.2.6.6 Radiated Interference-Antenna Induced (AI) Narrowband Limit Rod Antenna - The upper limit for this requirement shall be a straight line drawn from the point 15 KHz and 57 DB uv to 150 KHz and 37 DB uv.

3.5.4.4.4.3.3.2.6.7 Magnetic Coupling susceptibility - The magnetic coupling susceptibility requirement as specified in 4.2.1.3.1 of WR-101, Part I, shall not be required to be performed on the MDM interconnecting and interface signal lines.

3.5.4.4.4.3.3.2.6.8 Current Probe Conducted Interference - The current probe conducted interference tests as specified in 4.2.1.1. of WR-101 Part I, and 4.3.1 of MIL-I-6181D shall not be required to be performed on the MDM interconneting and interface signal lines.

3.5.4.4.4.3.3.2.7 Test Logic - The equipment shall contain test logic for the purpose of isolation of malfunctions down to a replaceable maintenance module. Test mode commands from the Drum Controller shall be the stimulus of the test function. Internal test signal responses shall be provided to the Drum Controller to provide the basis for automatic fault isolation. The volume of circuitry added for test purposes shall not exceed 15% of the normal operational circuitry.

3.5.4.4.4.3.3.2.8 Grounding - The Magnetic Drum Memory system shall be provided with a signal ground which is isolated from the MDM frame.

3.5.4.4.4.3.3.2.9 Hermetic Seal - The Magnetic Drum shall be a hermetically sealed unit and shall have a leak rate such that the Magnetic Drum remains pressurized to an operationally acceptable pressure for a period of at least two years.

3.5.4.4.4.3.3.2010 Provisions for Maintainability - Maintenance module require - ments for the MDM shall be as defined in 3.3.7.2.1.

3.5.4.4.4.3.3.2.11 Identification Marking - Identification marking for the MDM shall be in accordance with the requirements for a subassembly of Logic Unit 4 as given in MIL-E-5400.

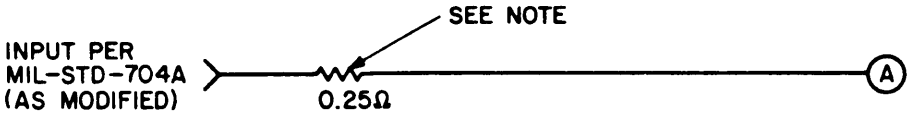
3.5.4.4.4.3.3.2.12 Standard Conditions - Those conditions given in 3.3.9 for Logic Unit 4 shall be used to establish normal performance characteristics for the MDM under standard conditions and for making laboratory bench tests.

3,5.4.4.4.3.3.2.13 Service Conditions - The MDM, when installed in a Logic Unit 4 enclosure, shall operate satisfactorily under any of the environmental service conditions specified in 3.3.10 except as modified herein. All environmental conditions shall be applied to the Logic Unit 4 enclosure.

3.5.4.4.4.3.3.2.13.1 Temperature - The MDM shall operate as specified herein when subjected to the temperatures specified in 3.3.10.5 except that at temperatures above 55° C the equipment shall not be required to meet the MDM error rate requirement. However, no damage to the MDM shall occur during the high temperature tests.

3.5.4.4.4.3.3.2.14 Warmup Time - The time required for the MDM to warm up prior to operation shall be kept to a minimum and shall not exceed 25 seconds for temperatures from 0° C to and including +55° C and shall not exceed 4.5 minutes for temperatures from less than 0° C to and including -25° C.

3.5.4.4.4.3.3.2.15 Input Electrical Power - The MDM shall operate with power as received at point A of Figure 149. The input to Figure 149 shall be as specified in MIL-STD-704A except that curve 3 of Figure 3 shall be modified such that its lower limit shall not fall below 80 volts. The MDM shall operate with three phase 400 Hz 115/200 volt (nominal) AC power. The total MDM power shall be 305 ±35 watts during normal operation. The maximum power required by the MDM of duration greater than 2 seconds but less than 60 seconds shall not be greater than 850 watts. Peak line current at power turn-on shall not exceed 105 amperes/phase and shall be below 10 amperes two milliseconds after power turn-on. No single phase power usage shall be allowed without the use of the three-phase neutral power return.



NOTE:
THE SERIES RESISTANCE SHOWN IS A MAXIMUM RESISTANCE AND SHALL NOT BE USED AS A CURRENT LIMITING RESISTANCE TO DETERMINE PEAK LINE INRUSH CURRENT AT POWER TURN ON.

Figure 149. MDM Input Power Source

3.5.4.4.4.3.3.2.15.1 Normal Conditions - Normal voltage conditions are defined as those voltage conditions which fall within the area defined by the curves obtained at point A of Figure 149 when the input to Figure 149 consists of curves 2 and 3 (as modified) of Figure 3 of MIL-STD-704A. The MDM shall perform as specified for all normal voltage conditions.

3.5.4.4.4.3.3.2.15.2 Abnormal Conditions - Abnormal voltage conditions are defined as those voltage conditions which fall outside the area defined the area defined by curves obtained at point A of Figure 149 when the input to Figure 149 consists of curves 2 and 3 (as modified) in Figure 3 of MIL STD-704A but remain within the area defined by the curves obtained at point A when the input to Figure 149 consists of curves 1 and 4 in Figure 3 of MIL-STD-704A. The MDM may malfunction during abnormal voltage conditions but shall automatically resume normal operation when the voltage conditions return within normal limits. No damage to the equipment or destruction of data already stored shall occur due to abnormal voltage conditions.

3.5.4.4.4.3.3.2.15.3 Loss of Power - No damage to the MDM or destruction of data already stored shall occur due to accidental or deliberate disruption of all three phases of input power regardless of the time in its operating cycle or the duration of interruption.

3.5.4.4.4.3.3.2.15.4 Power Factor - Power factor shall be defined as the ratio of real power per phase to volt amperes per phase (product of RMS phase voltage and RMS phase current). For a total real power of 305 ±35 watts, the MDM shall have a leading power factor on all phases from 0.800 to 0.950.

3.5.4.4.4.3.3.2.16 Power Supply - The MDM shall contain the power supply needed for read, write, test and control purposes. This power supply shall utilize the AC power as specified in 3.5.4.4.4.3.3.2.15.

3.5.4.4.4.3.3.2.16.1 Overload Protection - The power supply shall be protected from external overload conditions including short circuits.

3.5.4.4.4.3.3.2.16.2 Overvoltage Protection - The power supply shall provide over-voltage protection for the MDM under both normal and abnormal operating conditions.

3.5.4.4.4.3.3.2.16.3 Undervoltage Protection - The power supply shall provide under-voltage protection for the MDM under both normal and abnormal operating conditions.

3.5.4.4.4.3.3.2.16.4 Power Error Detection - The power supply shall have the cap ability of detecting an out of tolerance voltage condition which could affect normal MDM operation. During an out of tolerance or unpowered condition the Power Error Status line shall indicate an open-circuit condition. Whenever power returns within tolerance the Power Error Status line shall auto-matically recover and indicate a logic 1 level. Indication of this condition shall be provided to the drum controller as an MDM power error status signal.

3.5.4.4.4.3.3.2.16.5 Protective Devices - Where necessary, circuit breakers shall be used. When used circuit breakers shall be accessible from the exterior of the equipment. Fuses shall not be used.

3.5.4.4.4.3.3.2.17 Cooling - The MDM shall comply with the thermal design re-quirements of MIL-E-5400 class 1A-X when installed in the Logic Unit 4 enclosure. The MDM shall contain its own fan. The air inlet openings shall be located on the MDM front panel. Air exhaust openings shall be located on the bottom of the MDM and shall be compatible with the exhaust opening provided in Logic Unit 4. Cooling shall be achieved by use of a heat exchanger on which all sub-assemblies with the exception of the RF1 subassembly are mounted.

3.5.4.4.4.3.3.3 Performance - Unless otherwise specified, values set forth to establish the requirements of satisfactory performance apply to performance under both standard and extreme service and input power conditions. When reduced performance under the extreme conditions is acceptable, tolerances or values setting forth acceptable variations from the performance under the standard conditions will be specified,

3.5.4.4.4.3.3.4 Detail Requirements

3.5.4.4.4.3.3.4.1 Functions - The functional operations of the MDM fall into three categories -- write operations, read operations, and test operations.

3.5.4.4.4.3.3.4.1.1 Write Operation - During a write operation the Drum Controller shall supply a write command and data control signals at the appropriate times relative to the drum tachometer pulse. NRZ data transfer from the Drum Controller to the MDM shall take place in 8-bit bytes (four per 32-bit word) in synchronism with a byte clock supplied by the MDM. The data shall be recorded serially on the specified track. As the data bits are recorded a serial parity check shall be made.

3.5.4.4.3.3.4.1.2 Read Operation - During a read operation the Drum Controller shall supply a read command and data control signals at the appropriate times relative to the drum tachometer pulse. Data shall be read from the selected drum track in a serial manner and a serial parity check shall be made as the data bits are read from the drum. NRZ data shall be transferred from the MDM in 8-bit bytes (four per 32-bit word) in synchronism with a byte clock supplied by the MDM.

3.5.4.4.4.3.3.4.1.3 Test Operation - During a test operation the Drum Controller shall send a test mode command to the MDM. The MDM shall send internal test signals back to the Drum Controller for diagnostic fault isolation purposes. The test data shall be sent over the signal lines normally used for data, or over MDM status lines as required.

3.5.4.4.4.3.3.4.2 Drum Speed - Drum speed shall not be less than 4750 rpm nor greater than 4850 rpm.

3.5.4.4.4.3.3.4.3 Magnetic Drum Memory Subassemblies - The Magnetic Drum Memory shall be comprised of the following subassemblies:

(1) Drum Subassembly - The drum subassembly shall consist of the rotating drum mechanism, and those portions of the track address selection and read/write electronics which good engineering judgement indicates should be a part of the drum subassembly. The drum subassembly shall include an elapsed time meter type MS-17322-6A which shall be an integral part of the drum subassembly.

(2) Drum Electronics Subassemblies - The drum electronics subassembly or subassemblies shall contain all read/write, clock, addressing, and control electronics not included in the drum subassembly.

(3) Drum Power Supply Subassemblies - The drum power supply subassembly or subassemblies shall contain all power supplies needed by the drum and drum electronics subassemblies. In addition, if based on good engineering judgement, certain control functions such as the drum speed control may be located in this subassembly.

(4) Drum RFI Subassembly - The RFI subassembly shall consist of a suitable RFI filter such that the MDM can meet all of the applicable input electric power and EMI requirements of this specification. The RFI subassembly shall also include bleeder resistors to provide a discharge path for stored charge after power is removed from the MDM. Provision shall also be made internal to the RFI subassembly for termination of the MDM safety ground to the case of the RFI subassembly. The case of the RFI subassembly shall achieve chassis ground when installed in Logic Unit 4 through its mechanical configuration and the RFI mating surface shall therefore be free of any external electrical insulating materials, coatings, etc.

The interface between the MDM power cable and the RFI subassembly shall be a connector to allow the MDM assembly (less RFI subassembly) to be readily removed from the Logic Unit 4 enclosure.

3.5.4.4.4.3.3.4.4 Form Factor - The Magnetic Drum Memory shall have overall dimensions to comply with Unit 4 Outline Dimensions given in E 1-515, Avionics Installation Instructions for Data Analysis Programming Group AN/AYA-8B.

3.5.4.4.4.3.3.4.5 Mounting - All subassemblies of the MDM shall be mounted directly to the MDM assembly itself unless otherwise specified. The MDM shall be mounted on slides extending from the side of Logic Unit 4. These slides shall have two detents, one for normal inspection and normal troubleshooting and one for the removal of the MDM. These slides shall be strong enough to support the extended MDM. The MDM removal detent position shall protrude far enough to permit servicing the MDM without detaching from the logic enclosure. Cables, harnessing, clamps and retractors shall be such as to allow smooth operation of the MDM in and out of Logic unit 4.

3.5.4.4.4.3.3.4.6 Functional Interfaces - The interface between the Magnetic Drum Memory and the Drum Controller shall be as shown in Figure 153.

3.5.4.4.4.3.3.4.6.1 Drum Controller to Magnetic Drum Memory - Signals from the Drum Controller to the MDM shall consist of the following:

(1) Write Command -1 Line

(2) Read Command -1 Line

(3) Data -8 Lines

(4) Track Address -9 Lines

(5) MDM Test Modes -4 Lines

(6) Sector Begin - 1 Line

(7) Sector End -1 Line

(8) MDM Manual Test Inhibit -1 Line

(9) MDC Test Mode Inhibit -1 Line

(10) MDM SI (System Initialize) -1 Line

(11) DAMS OTB2 (Out-of-Tolerance Bit) -1 Line

(12) MDM Track Test Inhibit -1 Line

3.5.4.4.4.3.3.6.2 Magnetic Drum Memory to Drum Controller - Signals from the MDM to the Drum Controller shall consist of the following:

(1) Word Clock - 1 Line

(2) Tachometer Pulse - 1 Line

(3) Data - 8 Lines

(4) MDM Status -6 Lines

(5) Byte Parity Error - 2 Lines

(6) Byte Clock - 1 Line

(7) Preamble Detect -1 Line

(8) MDM Test Error -1 Line

(9) MDM Test Complete - 1 Line

(lo) MDM Temp Sht Dn Status (Temperature Shut Down Status) - 1 Line (return isolated ‘from ground)

(11) Bit Clk Tst (Bit Clock Test) - 1 Line

3.5.4.4.4.3.3.4.6.3 Mechanical Signature Analysis (MSA) Outputs - Two calibrated accelerometer shall be included as part of the drum subassembly for the purpose of obtaining mechanical signature analysis data. The accelerometers shall be located in close proximity to the drum bearings. Accelerometer outputs shall be provided and shall be located on the MDM front panel.

3.5.4.4.4.3.3.4.6.4 Controller Power Signals - Power signals between the Drum Controller and Magnetic Drum Memory shall be as follows:

(1) DAMS OTB 2 (DAMS tit-of-Tolerance Bit 2) - The MDM shall have the capability of monitoring the DAMS 2 line. Whenever a Logic 1 1evel is present on the DAMS OTB 2-line, the MDM shall process any write, read or test instruction. Whenever an open-circuit condition is detected, the MDM shall go into an immediate standby condition which precludes any further data processing activity or acceptance of control signals. Upon detection of a Logic 1

level, the MDM shall automatically resume normal operation and process any subsequent write, read or test instruction.

Manual tests conducted from the MDM front panel shall not be inhibited by the DAMS OTB 2 control line whenever the I/O interface cable is disconnected from the Drum Controller.

In the Logic 1 state, this line shall be required to sink no more than 10 milliamperes to ground. In the open-circuit condition no more than +12 VDC shall be applied to this line. The DAMS OTB 2 line shall not be subject to the MDM interface logic level requirements as stated in this specification except to the extent as explicitly stated in this paragraph.

(2) MDM SI (MDM System Initialize) - The MDM shall have the capability of monitoring the MDM S1 line in the following manner. Whenever an open-circuit condition is present on the MDM S1 line, the MDM shall process any write, read or test instruction. Whenever a Logic 1 level is detected the MDM shall go into an immediate standby condition which precludes any further data processing activity or acceptance of control signals. Upon detection of an open-circuit condition, the MDM shall automatically resume normal operation and process any subsequent write, read or test instruction. In the Logic 1 state, this line shall be required to sink no more than 10 milliamperes to ground. In the open-circuit condition no more than +12 VDC shall be applied to this line. The MDM S1 line shall not be subject to the MDM interface logic level requirements as stated in this specification except to the extent as explicitly stated in this paragraph.

3.5.4.4.4.3.3.4.6.5 Controller Test Signals - Test signals between the Drum Controller and MDM shall be as follows:

(1) MDC Test Mode Inhibit - The MDM, upon receipt of an MDC Test Mode Inhibit signal (Logic 1 level) from the Drum Controller, shall ignore all signals at the interface with the exception of the MDM S1 and the DAMS OTB 2 signals. Upon removal of the MDC Test Mode Inhibit signal, the MDM shall automatically resume normal operation and process all interface signals.

(2) MDM Manual Test Inhibit - The MDM shall have the capability of monitoring the MDM Manual Test Inhibit line as follows:

(a) For a Logic 1, the MDM shall inhibit all manual test operations from being performed from the MDM front panel. In addition the MDM shall not inhibit in any way operational instructions (write/read/test modes) from being performed when issued from the Drum Controller.

(b) For a Logic O, the MDM shall be capable of performing operational instructions (write/read/test modes) from the Drum Controller or manual tests from the MDM front panel. The MDM when performing manual test operations from the MDM f rent panel shall operate as specified by the status of the MDM Track Test Inhibit line.

(3) MDM Track Test Inhibit - The MDM shall have the capability of monitoring the MDM Track Test Inhibit Line and of performing as follows: Whenever a Logic 1 condition is present on the MDM Track Test Inhibit line, the MDM shall inhibit MDM Test Mode 1 and manual test operations from the MDM f rent panel from being performed on the normal data sector (1 to 1090 word locations) of all data tracks. Whenever an open circuit condition is present, the MDM shall be capable of performing MDM Test Mode 1 and manual test operations from the MDM front panel utilizing the entire normal data sector (1 to 1090 word locations) and test sector (1091 to 1239 word locations) of all data tracks. In addition, whenever the MDM Track Test Inhibit line is open circuit and MDM Test Mode 1 is initiated, the MDM during the entire MDM Test Mode 1 sequence starting with the first write operation using the first data pattern on the first track, shall send Parity Error 1/2 and Parity Error 3/4 pulses to the Drum Controller. Whenever the MDM Track Test Inhibit line is a Logic 1, Parity Error 1/2 and Parity 3/4 pulses shall be inhibited for the entire duration of MDM Test Mode 1.

3.5.4.4.4.3.3.4.6.6 MDM Status Signals - In addition to the power error, track error and clock error status signals defined in other paragraphs within the MDM section of this specification, the Magnetic Drum Memory shall provide the status signals defined in the following paragraphs.

(1) Temperature Error Status - The Magnetic Drum Memory shall have a device to detect a warning overtemperature condition in the drum subassembly. The warning overtemperature threshold of the sensor shall be selected such that any additional data processing (writing or reading) after an overtemperature indication could result in erroneous operation as a result of the increased temperature in the drum subassembly.

During a warning overtemperature condition the temperature error status line shall indicate an open-circuit condition at all times that a warning overtemperature condition exists. Whenever the temperature comes within the reset tolerance of the sensor, the temperature error status line shall automatically recover and indicate a Logic 1 level.

This signal shall be sent to the Drum Controller and shall be defined as the MDM temperature error status signal.

(2) Temperature Shutdown Status - The Magnetic Drum Memory shall have a device to detect a critical overtemperature condition in the drum subassembly. The critical overtemperature threshold of the sensor shall be selected such that any further operation of the drum subassembly after a critical overtemperature indication might subject the drum sub assembly to mechanical/electrical damage.

The sensor shall be normally open whenever the temperature is below the critical temperature limit and shall close whenever the critical temperature limit is exceeded. Whenever the temperature falls below the reset temperature limit of the sensor, the sensor shall automatically revert to a normally-open condition. Upon receipt of the critical temperature indication Logic Unit 4 shall automatically remove AC power from the MDM.

In the closed position, the sensor shall have a maximum resistance of O. 5 ohms and shall be capable of conducting 300 milliamperes continuously without damage. Both interface lines (MDM Temp Sht Dn and MDM Temp Sht Dn Ret) shall be isolated from the MDM chassis and MDM signal ground. This sign al shall be sent to the Drum Controller and shall be defined as the MDM temperature shutdown status signal.

(3) Speed Error Status - Whenever the MDM power error status line is a Logic 1 level, the MDM shall have the capability of detecting an out-of-tolerance drum speed condition or other normal operation speed related conditions which would inhibit write/read operations from being performed and provide a Logic 1 level on the MDM speed error status line as long as the condition exists. This signal is known as the MDM speed error status signal. A stable speed error status Logic 1 level shall be provided to the Drum Controller from the time the MDM power error status line becomes a Logic 1 to the time the drum speed error status line becomes a Logic O level.

(4) Pressure Error Status - The Magnetic Drum Memory shall have the capability of detecting an internal drum pressure error and provide a Logic 1 level as long as the pressure error exists. This signal is known as the MDM pressure error status signal.

3.5.4.4.4.3.3.4.6.7 Interface Logic Levels - Except as noted, all signal transmission between the MDM and the Drum Controller shall be digital in nature and conform to the following definit ions. (All voltage levels specified are referenced to signal ground.)

(1) Logic 1 Level - Logic 1 signal level is defined as the region -2.0 VDC to +2.0 VDC except that the -2.0 VDC (excursion from O VDC) shall be limited to a maximum of 200 nanoseconds. Unless stated otherwise, a Logic 1 signal level indicates that the signal is true.

(2) Logic O Level - Logic O signal level is defined as the region from +3.0 VDC to +7.0 VDC. Unless stated otherwise, a Logic O signal level indicates that the signal is false.

(3) Rise and Fall Time - Except as noted, rise and fall times are defined as the time for the signal transition between the + 1.75 VDC and +3.50 VDC voltage levels. All interface signal transitions (rise and fall) shall be less than 150 nanoseconds unless otherwise specified.

(4) Interface Timing Reference and Delay - The timing reference for all interface logic signals shall be with respect to the leading edge of the word clock pulse taken at the connector junction between the MDM and the Drum Controller. The maximum pulse delay through the Drum Controller as measured at the connector junction points shall be 560 nanoseconds.

(5) Pulse Width and Time Delay Measurements - All pulse width and time delay measurements on interface signals shall be made where signal transitions cross the +2. 50 VDC voltage level, unless otherwise specified.

(6) Signal Driver - Except as noted, the signal output driver circuits used in the MDM shall be capable of providing the specified logic levels, transition times, and pulse width (or delays) while driving the load (two logic level receivers) as shown in Figure 154.

(7) Signal Receivers - The signal receiver inputs to the MDM shall meet the maximum requirements as stated below and illustrated in Figure 150.

(a) The signal receivers shall require that the driver sink a maximum of 10 milliamperes to ground for the Logic 1 state.

(b) The signal receivers shall require that the driver supply a maximum of 50 microampere for the Logic O state.

(c) The signal receiver, including wiring capacitance, shall present a maximum capacitance of 250 picofarads.

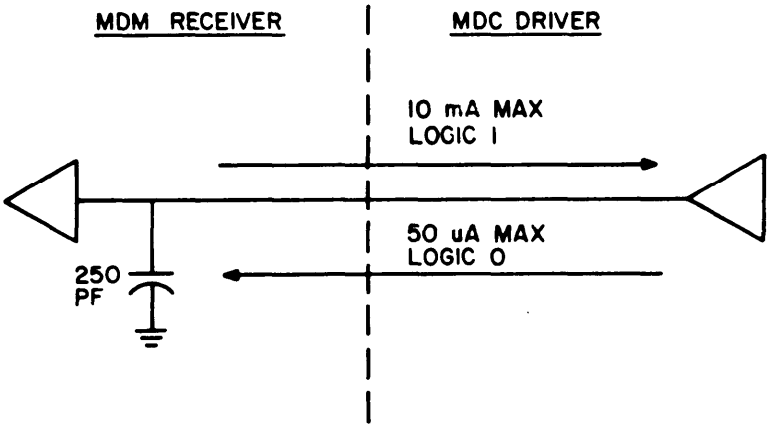


Figure 150. MDM Signal Receiver Requirements

(8) Noise - Noise of any type such as crosstalk, ringing, etc, shall not cause a logic level signal at the MDM/Logic Unit 4 interface to exceed any of the requirements as specified in the Logic 1 or Logic 0 definitions in the MDM section of this specification.

3.5.4.4.4.3.3.4.7 Data Tracks

3.5.4.4.4,3.3.4.7.1 Recorded Data Tracks - The Magnetic Drum shall contain 384 addressable data tracks. In addition there shall be a mmimum of 10 spare tracks (complete with heads) available for use in the event of track failure. Each data track shall have a flying read/write head. Utilization of the 10 spare tracks shall be a depot level maintenance procedure. It shall be necessary to de-pressurize the enclosed drum subassembly, rewire a spare track in place of the defective track and repressurize the enclosed drum subassembly.

3.5.4.4.4.3.3.4.7.2 Capacity of Track - Each data track shall have sufficient bit capacity to contain 1024 data words plus overhead bits needed for control and test purposes. Each data word is comprised of 30 computer data bits plus two parity bits.

3.5.4.4.4.3.3.4.7.3 Track Adressing - Track address shall be specified to the MDM by means of a nine-bit binary address word which shall remain static as long as that track is to be addressed for purposes of reading or writing. The lowest of the possible address states shall be used to address a track. The track address format shall be shown in the following track address table.

TRACK ADDRESS TABLE

	DRUM TRACK ADDRESS BITS									
		8	7	6	5	4	3	2	1	0	
Track Number Selected	1	0	0	0	0	0	0	0	0	0	Valid Track Address Codes
	2	0	0	0	0	0	0	0	0	1	
	3	0	0	0	0	0	0	0	1	0	
	4	0	0	0	0	0	0	0	1	1	
	5	0	0	0	0	0	0	1	0	0	
	.	.	.	.	.	.	.	.	.	.	
	.	.	.	.	.	.	.	.	.	.	
	.	.	.	.	.	.	.	.	.	.	
	380	1	0	1	1	1	1	0	1	1	
	381	1	0	1	1	1	1	1	0	0	
	382	1	0	1	1	1	1	1	0	1	
	383	1	0	1	1	1	1	1	1	0	
	384	1	0	1	1	1	1	1	1	1	
	385	1	1	0	0	0	0	0	0	0	Invalid Track Address Codes
	386	1	1	0	0	0	0	0	0	1	
	387	1	1	0	0	0	0	0	1	0	
	388	1	1	0	0	0	0	0	1	1	
	.	.	.	.	.	.	.	.	.	.	
	.	.	.	.	.	.	.	.	.	.	
	.	.	.	.	.	.	.	.	.	.	
	508	1	1	1	1	1	1	0	1	1	
	509	1	1	1	1	1	1	1	0	0	
	510	1	1	1	1	1	1	1	0	1	
	511	1	1	1	1	1	1	1	1	0	
	512	1	1	1	1	1	1	1	1	1	

(1's and 0's represent interface logic levels)

3.5.4.4.4.3.3.4.7.4 Track selection - The MDM shall include logic to decode the binary address and select one track for writing on or reading from the drum.

3.5.4.4.4.3.3.4.7.5 Track Switching - When the track address is changed from one track to another track, the new track shall be selected in less than eight word times of the time that the new address is sent to the MDM.

3.5.4.4.4.3.3.4.7.6 Track Error - The MDM shall provide a Logic 1 level to the Drum Controller whenever a track address change is made and any of the conditions listed below is detected.

(1) No track selection

(2) More than one track selected

(3) A track address greater than 384 selected

The track error signal shall assume its proper state no later than two word times after a track address change has been made by the Drum Controller.

This signal is defined as the MDM track error status signal.

3.5.4.4.4.3.3.4.8 Drum Clocks - Unless otherwise specified the MDM shall contain and provide clock signals to the drum controller as defined in the following paragraphs.

3.5.4.4.4.3.3.4.8.1 Bit Clock Selection - The MDM shall contain two bit clock tracks either of which is selectable by means of an external switch. It shall be possible to read data written by one of the two clocks by using either the original writing clock or the other clock. Specified operation is not required if the position of the clock select switch is changed during a read, write or test mode operation.

3.5.4.4.4.3.3.4.8.2 Bit Clock - The bit clock shall be supplied to the Drum Controller via the Bit Clk Tst Line and shall be under control of the MDM Track Test Inhibit line. Whenever a Logic 1 level is detected on the MDM Track Test Inhibit line, the MDM shall automatically inhibit bit clocks on the Bit Clk Tst line and provide a Logic O level to the Drum Controller. Upon detection of an open-circuit condition on the MDM Track Test Inhibit line, the MDM shall automatically provide bit clocks to the Drum Controller on the Bit Clk Tst line. The bit clocks supplied by the MDM shall have a pulse width of 156 ±50 nanoseconds and a period of 312.8 l 53 nanoseconds.

3.5.4.4.4.3.3.4.8.3 Tachometer Clock - The tachometer clock shall be supplied to the Drum Controller and shall consist of one pulse to a Logic 1 state per drum revolution. Pulse width shall be as indicated in the continuous clock timing diagram, Figure 155.

3.5.4.4.4.3.3.4.8.4 Word Clock - The word clock shall be derived from one of the recorded bit clocks and it shall be transmitted to the Drum Controller. There shall be 1249 word clock pulses per drum revolution which have pulse widths and time relationships to each other and to the tachometer clock pulses as shown in the continuous clock signal timing diagram, Figure 155.

3.5.4.4.4.3.3.4.8.5 Byte Clock - Data shall be transmitted between the MDM and the Drum Controller in four 8-bit bytes per word transmitted. The MDM shall send a byte clock to the Drum Controller with which the data bytes are synchronized. The time relationships between the byte clock and word clock or sector begin pulse shall be as defined in the write operation sequence, read operation sequence, MDM Test Mode 1 and MDM Test Mode 2 paragraphs of the MDM section of this specification.

3.5.4.4.4.3.3.4.8.6 Clock Error - The MDM shall have the capability of detecting a bit clock timing error. when an error is detected, a Logic 1 level signal shall be sent to the Drum Controller via the MDM Clock Error Status line. The minimum duration of this signal shall be two word times and the maximum shall be 1251 word times after the bit clock returns to normal. The MDM shall inhibit writing when a clock error is detected.

3.5.4.4.4.3.3.4.8.7 Clock Retention - During continuous drum operation or power on/power off cycling, the tachometer and bit clock shall not exhibit any deterioration effects such that write and/or read operations with the drum cannot be performed within the specified MDM error rate.

3.5.4.4.4.3.3.4.9 Write/Operations - The MDM shall perform data writing and reading as defined in the following paragraphs.

3.5.4.4.4.3.3.4.9.1 Write Operation Sequence - The write operation sequence timing is shown in the write operation timing diagram, Figure 156 and is described as follows:

(1) The write command signal becomes a Logic 1 at least eight word times prior to the actual initiation of writing and remains in that state.

(2) At the proper time a sector begin pulse is sent to the MDM. This pulse will be coincident with one of the word clock pulses, except for the effects of logic circuit time delays. When this pulse is received the MDM shall write the sector preamble word in the word space immediately following the sector begin pulse.

(3) The MDM shall, at the time that data words are needed, send byte clock pulses to the Drum Controller. The sectors may contain any number of data words greater than or equal to one. Each data word shall be sent to the MDM in four bytes of eight bits each. The data shall be recorded serially on the specified track using one word clock time per data word recorded. The number of byte clock pulses sent to the Drum Controller shall be some multiple of four.

(4) When the last data word of the sector has been received by the MDM, the Drum Controller shall send a sector end pulse after which the MDM shall cease sending byte clock pulses and terminate the write operation after the last byte has been written. Write current to the write head shall be “turned on” upon receipt of the sector begin pulse from the controller and automatically “turned off” after the last bit of the last byte of data has been written on the drum. The last word of a data sector shall be written in a position such that the preamble word for the next sector may be written in the next word space during either this same or any subsequent drum revolution by means of another sector begin pulse.

(5) As the data bytes are being written the MDM shall perform a serial parity check on the data. Each word of data is sent in a four byte sequence designated bytes 1, 2, 3, and 4 respectively. The combination of bytes 1 and 2 shall be checked for odd parity and a parity error shall be indicated by a pulse on the Byte 1/2 Parity Error line. The combination of bytes 3 and 4 shall be checked for odd parity and a parity error shall be indicated by a pulse on the Byte 3/4 Parity Error line.

(6) When a track switch is necessary, the track address state is changed at least eight word clock pulses prior to the time that a sector begin pulse is sent to the MDM. At no time shall a track switch occur within a sector.

3.5.4.4.4.3.3.4.9.2 Read Operation Sequence - The read operation sequence timing is shown in the read operation timing diagram, Figure 157, and is described as follows:

(1) The read command signal becomes a Logic 1 at least eight word times prior to the actual initiation of reading and remains in that state.

(2) At the proper time, a sector begin pulse is sent to the MDM. This pulse shall be coincident with one of the word clock pulses, except for the effect of logic circuit time delays. When this pulse is received the MDM shall start reading on the specified track the preamble word which should have been written in the word space immediately following the sector begin pulse. If the preamble word is not detected the Controller shall terminate the instruction by a Logic O on the Read Command line.

(3) When the preamble word is detected the MDM shall send a pulse on the Preamble Detect line and initiate the reading of the data. The data shall be read and formatted into eight-bit bytes just as it was received when written. The data transmission to the Drum

Controller shall be in synchronism with the byte clock generated by the MDM. The total number of byte clocks sent to the Drum Controller will be a multiple of four for each data sector read.

(4) When the last word of a sector has been received by the Drum Controller, a sector end pulse will be sent to the MDM. This pulse means that the MDM shall cease reading data and shall send no more byte clocks for that sector. If the MDM is to read the data sector immediately following the one just finished a sector begin pulse shall be sent simultaneously with the sector end pulse.

(5) As the data is being read, the MDM shall perform a serial parity check as was done when the data was written. Each word of data consists of four bytes designated 1, 2, 3, and 4. The combination of bytes 1 and 2 shall be checked for odd parity and a parity error shall be indicated by a pulse on the Byte 1/2 Parity Error line. The combination of bytes 3 and 4 shall be checked for odd parity and a parity error shall be indicated by a pulse on the Byte 3/4 Parity Error line.

(6) When a track switch is necessary, the track address state is changed at least eight word clock pulses prior to the time that a sector begin pulse is sent to the MDM. At no time will a track switch occur within a sector.

3.5.4.4.4.3.3.4.9.3 Termination of Operation - Normally, read or write operations are terminated by the transmission of a sector end pulse from the Drum Controller and MDM test mode tests are considered to be completed upon receipt of an MDM test complete pulse from the MDM. However, termination of an operation shall also occur if the corresponding write, read or MDM test mode 1, 2 or 3 signals become a Logic O. When this occurs, the MDM shall revert to a standby condition. When modes are switched (write to read write to MDM test mode, MDM test mode to read etc.), there is a period of at least one word time during which mode signals are simultaneously at Logic O.

3.5.4.4.4.3.3.4.9.4 Data Retention - After data has been written on any specified drum track or tracks and the corresponding track or tracks placed in either a protected or unprotected state, no data deterioration effects shall occur upon reading the data back when requested at any time with errors in excess of the specified error rate.

3.5.4.4.4.3.3.4.9.5 Error Rate - The MDM shall have an average of no more than one bit error in 2×10^{10} bits recorded and reproduced. The verification of the error rate shall be based upon using a read to write ratio of four.

3.5.4.4.4.3.3.4.10 Test Operations - The MDM shall have the test capability and performance as defined in the following paragraphs.

3.5.4.4.4.3.3.4.10.1 MDM Test Mode 1 Sequence - The MDM Test Mode 1 timing sequence is shown in the MDM Test Mode 1 timing diagram, Figure 158, and is described as follows for the MDM Track Test Inhibit line at Logic 1. When the MDM Track Test Inhibit line is open circuit, the sequence is the same except that write and read operations shall begin at word location 1 of each data track.

(1) The Test Mode 1 signal becomes a Logic 1 and shall remain in the Logic 1 state for the entire duration of Test Mode 1 tests.

(2) After the Test Mode 1 signal, the sector begin pulse is sent to the MDM.

(3) Starting with word location 1091 to and including word location 1239, the MDM shall write a preamble word and a predetermined word pattern starting with the first data track and continuing on to the last data track. At this time the MDM shall automatically switch to a read operation and proceed to read the preamble and word pattern previously written in word locations 1091 to 1239 at normal threshold sequentially from all data tracks starting with the first track. With the completion of the first read operation, the MDM shall automatically switch to a low threshold setting and re- read the test data. Upon completion of the second read operation the MDM shall automatically switch to a high threshold setting and re-read the test data. At this time the MDM

shall switch to a write operation and repeat the above procedure for a different predetermined word pattern. This process shall automatically continue provided no test errors have occurred and until eight unique word patterns have been written and the high threshold read operation of the last data pattern on the next to the last data track (track 383) has been completed. The MDM at this time shall terminate MDM Test Mode 1.

(4) At the completion of Test Mode 1, the MDM shall send to the Drum Controller a test complete pulse (Logic 1) via the MDM Test Complete line.

(5) If a test error is detected during any of the read operations, the MDM shall provide an error pulse (Logic 1) to the controller via the MDM Test Error line. The error pulse shall occur no more than 100 nanoseconds from the leading edge of word clock No. 1241.

(6) After a delay from the leading edge of the test error pulse, the MDM shall send to the Drum Controller the first of the four byte pulses used to transfer the test mode status word to the Drum Controller.

The Test Mode 1 status word format is as shown in Figure 159.

(7) Whenever an error is detected the MDM shall have the capability of detecting a sector end pulse (Logic 1) on the Sector End line. Upon detection of a sector end pulse, the MDM shall continue on with the testing sequence of Test Mode 1 on subsequent tracks. In the absence of a sector end pulse, the MDM shall remain in a state to continue testing on subsequent tracks and shall send continuous error pulses, byte clocks and error data as shown by Note 5 of Figure 158.

(8) The MDM shall have the manual capability to allow forcing a given number of known Test Mode 1 error status words during one complete operation of Test Mode 1.

3.5.4.4.4.3.3.4.10.2 MDM Test Mode 2 Sequence - The MDM Test Mode 2 timing sequence is shown in the MDM Test Mode 2 timing diagram (Figure 160) and is described as follows:

(1) The Test Mode 2 signal becomes a Logic 1 and shall remain in the Logic 1 state for the entire duration of Test Mode 2 tests.

(2) After the Test Mode 2 signal the sector begin pulse is sent to the MDM.

(3) After receipt of the sector begin pulse the MDM shall send four byte clocks to the Drum Controller. Byte clocks 1 and 2 shall be used to transfer the input stimulus data from the Drum Controller to the MDM and byte clocks 3 and 4 shall be used to transfer the output response data from the MDM to the Drum Controller. The MDM Test Mode 2 status word format is as shown in Figure 161.

(4) The parity error 3/4 pulses shall always occur as shown on the timing diagram during a Test Mode 2 test. The parity error 3/4 pulses are forced parity errors which indicate that the parity detect logic circuits are functioning properly.

(5) The parity error 1/2 pulses shall occur as shown on the timing diagram if parity errors are detected during the processing of the input stimulus data during Test Mode 2. The first parity error 1/2 pulse shall occur if a parity error is detected in the serialized data; the second parity error 1/2 pulse shall occur if a parity error is detected in the deserialized data.

(6) The preamble detect pulse shall always occur during Test Mode 2 as shown in the timing diagram whenever the preamble detect circuitry is functioning properly.

(7) At the conclusion of test, the MDM shall send an MDM test complete pulse (Logic 1) to the Drum Controller as shown in Figure 160.

3.5.4.4.4.3.3.4.10.3 MDM Test Mode 3 Sequence - The MDM Test Mode 3 timing sequence is shown in the MDM Test Mode 3 timing diagram, Figure 162, and is described as follows:

(1) The Test Mode 3 signal becomes a Logic 1 and shall remain in the Logic 1 state for the entire duration of Test Mode 3 tests.

(2) After the Test Mode 3 signal, the sector begin pulse is sent to the MDM.

(3) Upon receipt of the sector begin pulse, the MDM shall stimulate the MDM status lines. When the status lines stabilize, the MDM shall send a pulse (Logic 1) to the Drum Controller via the MDM Test Complete line.

(4) The MDM status lines shall remain in the stimulated test mode state until such time that the MDM Test Mode 3 signal line becomes a Logic O.

(5) Following the transition from a Logic 1 to a Logic O on the MDM Test Mode 3 line, the MDM status lines shall automatically return to their normal monitoring functions within 64 bit times.

3.5.4.4.4.3.3.4.10.4 MDM Test Mode 4 Sequence - The MDM Test Mode 4 timing sequence is shown in the MDM Test Mode 4 timing diagram, Figure 163, and is described as follows:

(1) The Test Mode 4 signal becomes a Logic 1 and shall remain in the Logic 1 state for the entire duration of Test Mode 4 tests.

(2) After the Test Mode 4 signal the sector begin pulse is sent to the MDM.

(3) Upon receipt of the sector begin pulse the MDM shall stimulate the specific circuitry associated with the speed control such that an out-of-tolerance speed condition occurs. The automatic shutdown circuitry for motor power associated with the speed controller shall then be allowed to function as required.

(4) After a time delay as shown on the timing diagram the MDM shall send to the Drum Controller an MDM test complete signal during which time the Drum Controller shall sample the MDM speed error status line.

NOTE: MDM Test Mode 4 exercises the speed error shutdown circuitry for the drum. After completion Test Mode 4, the main power to the MDM must be recycled to allow the drum to come up to nominal speed.

3.5.4.4.4.4 Detailed Functional Description

The following paragraphs contain a detailed functional description tion of the characteristics and performance requirements of the DAMS.

3.5.4.4.4.4.1 Word Formats

3.5.4.4.4.4.1.1 Operational Instruction Word Formats

Figure 164 shows the word formats for the normal operational instructions for reading, writing, status request, master clear, and terminate. In the cases of read and write instructions, each instruction shall be sent from the computer in a two-word sequence. The first word shall contain the begin address and the second word shall contain the end address of a data block to be written or read. All instruction words sent from the computer shall be sent under E F control.

3.5.4.4.4.4.1.2 Memory Protect and Test Instruction Word Formats

Figure 165 shows the word format for the Memory Protect instruction and indicates that any or all of the unused codes may be used for test mode operations. All instructions in these categories shall be sent from the computer under EF control.

3.5.4.4.4.4.1.3 Instruction Status Interrupt Word Format

Figure 166 shows the format of the Instruction Status Interrupt word. This word shall be sent to the computer with the status results of all instructions except the status request and test instructions. The contents of the word are described below:

(1) Bit 29 (Normal Completion) shall be used only following a read or write instruction. It shall be set to a Logic 1 to indicate that the instruction was completed with no data errors or fault conditions detected during the execution of the instruction. Status conditions which shall cause the Normal completion bit to remain reset are Drum Failure, Parity Error, Sync Detect Error or Invalid Function.

(2) Bit 28 (Parity Error) shall become a Logic 1 when a parity error is detected during a read or write instruction.

(3) Bit 27 (Sync Detect Error) shall become a logic 1 when the preamble word is not detected at the first addressed location of a read instruction or at the proper positions within the data block during a read operation. It shall be an indication that the preamble word was not properly written, on the drum, the preamble word was improperly read or that the data to be read was improperly addressed. A preamble word is located at the first addressed word location.

(4) Bit 26 (Drum Failure) shall be used in conjunction with bits 4 through 10 and shall become a Logic 1 whenever a drum malfunction is detected.

(5) Bit 25 (Cleared) shall be a Logic 1 when the Drum Controller is in an idle (inactive) state and all status registers have been cleared.

(6) Bit 24 (Standby) shall be a Logic 1 when the Drum Controller is in an idle (inactive) state and any status data accumulated during the previously executed instruction remains in the status register.

(7) Bit 23 (Invalid Function) shall be used in conjunction with Bits O through 3. It shall become a Logic 1 to indicate an error relating to the instruction word contents.

(8) Bits 22 through 11 (Memory Protect Status) shall indicate the state of the memory protect register flip-flops, denoting the status of the Memory Protect switches and/or the Computer Memory Protect Word.

(9) Bit 10 (Clock Loss) shall be a Logic 1 when any one or combination of the Word Clock, Tachometer Clock or Byte Clock is not received by the Drum Controller from the Magnetic Drum Memory.

(10) Bit 9 (Power Fault) shall be a Logic 1 when a fault exists in the power conditions of the Magnetic Drum Memory power supply,

(11) Bit 8 (Track select Error) shall become a Logic 1 when either more than one track is selected, no track is selected or a non-existent track is selected.

(12) Bit 7 (Clock Error) shall be a Logic 1 when the selected clock timing is out of tolerance.

(13) Bit 6 (Pressure Error) shall be a Logic 1 when the pressure in the Drum subassembly is below an acceptable level.

(14) Bit 5 (Overtemperature) shall be a Logic 1 when the temperature of the Drum subassembly exceeds an acceptable level.

(15) Bit 4 (Speed Error) shall be a Logic 1 when the speed (or speed related conditions) of the Magnetic Drum is out of tolerance.

(16) Bit 3 (Illegal Instruction) shall be a Logic 1 when the code of an instruction is not one of those listed as a valid operation code or one of the test codes.

(17) Bit 2 (Write Lockout) shall become a logic,1 when any portion of the memory addressed by a write instruction is a write protected section.

(18) Bit 1 (Address Error) shall be a Logic 1 when the begin address of a read or write instruction is greater than or equal to the end address (Address Overflow) or if a nonexistent track is addressed.

(19) Bit O (sequential/combinational Error) shall be a Logic 1 when the second word received in a two-word instruction is any word other than the correct one, master clear, read/write terminate or when the second word of a two word instruction is received first.

3.5.4.4.4.4.1.4 Parity Status Interrupt Word Format

Figure 167 shows the format of the parity status interrupt word. This word shall be sent to the computer following a Parity Status Request instruction. The contents of the word reflect data of the first parity error detected during a read or write operation and shall be as described below:

(1) Bit 29 (Parity Data Available) shall be a logic 1 if a parity error is detected and data on that parity error is stored in these registers.

(2) Bits 27 and 28 (Byte Designators) shall indicate in which byte the first parity error was located. Only one of these two bits may be a logic 1 and only if the first parity error detected occurred on data entering or leaving the drum.

(3) Bits 25 and 26 (Buffer Designators) shall indicate the buffer from which the word containing the first detected parity error had been received. Only one of these two bits may be logic 1 and only if the first parity error detected occurred on data retrieval from one of the buffers.

(4) Bit 24 (Read/Write Mode) shall indicate the type of instruction being executed when the parity error was detected.

(5) Bits 19 through 23 are not used and shall be logic 0's.

(6) Bits 10 through 18 shall contain the address of the track being used when the first parity error is detected. The contents of these nine bits have no meaning when the first error detected is a buffer error.

(7) Bits O through 9 shall contain the word address of the first detected register parity error. The contents of these 10 bits have no meaning when the first error detected is a buffer error.

3.5.4.4.4.4.1.5 Error Count Interrupt Word Format

Figure 168 shows the format of the Error Count Interrupt Word. This word shall be sent to the computer following the execution of the Error Count Request instruction. The contents of the word shall be as described below:

(1) Bit 29 (Error Count Data Available) shall be a logicl when at least one parity error or an overrun/underrun condition has been detected and that error count data is stored 'in these registers.

(2) Bits 20 through 28 (Overrun/Underrun count) shall be a binary count of the number of times an overrun or underrun condition was detected. Bit 20 shall be the least significant bit of the count. Acount of all 1's shall indicate that 511 or more such events were detected.

(3) Bits 10 through 19 (Buffer Error Count) shall be a binary count of the number of buffer parity errors detected. Bit 10 shall be the least significant bit of the count. The count shall reincremented by one each time a buffer error (on a whole wordbasis)is detected. Acount of all 1's shall indicate that 1023 or more buffer parity errors were detected.

(4) Bits 0 through 9 (Register Error Count) shall be a binary count of the number of register parity errors detected. Bit 0 shall be the least significant bit of the count. The count shall reincremented by one each time a register error (on a byte basis) is detected. A count of all 1's shall indicate that 1023 or more register parity errors were detected.

3.5.4.4.4.4.1.6 Read/Write Data Word Formats

Figure 169 shows the relationship between the 30-bit data word received from or sent to the computer and the 32-bit data word received from or sent to the magnetic drum memory.

The 30-bit computer word shall be divided into two 15-bit parts. A parity bit P shall be added to computer bits 0 through 14 to form bits 0 through 15 (Byte 1) of the drum word. A parity bit P_1 shall be added to computer bits 15 through 29 to form bits 16 through 31 (Byte 2) of the drum word. Odd parity shall be used in the generation of each of the parity bits.

Data transmission to and from the computer shall take place in a 30-bit parallel transfer mode. Data transmission to and from the selected drum track shall take place in a serial mode.

3.5.4.4.4.4.2 Data Addressing

A total of 19 bits of address shall be used to specify the location of a data word. Bits O through 9 of a read or write instruction shall be used to specify a particular word out of 1024 on a track (bit O shall be the least significant bit). Bits 10 through 18 of a read or write instruction shall be used to specify a particular track on the drum. Bit 10 shall be the least significant bit of the track address. The lowest 384 of the possible 512 binary states of these nine bits shall be used for track addressing.

A block of data to be written on or read from the drum shall be specified by two addresses, namely a begin address (word and track) and an end address (word and track). The begin address of an instruction shall specify the location at which a preamble word is to be or has been written. Therefore, if it is desired to write or read a block of data with N data words in the block, then the begin and end addresses of the instruction shall specify N + 1 address locations.

Data to be read from the drum shall be addressed in the same manner used to specify addresses when it was written. When executing a read instruction, if a preamble word is not detected at the begin address, the instruction shall be terminated and a Sync Detect Error indicated to the computer.

3.5.4.4.4.4.3 Data Buffers and Data Sectors

The Drum Controller shall include two 32-word (32 bits per word) data buffer in order to provide simultaneous data transfers. During a write instruction the drum. Conversely during a read of the buffers while the other buffer is being unloaded into the drum. Conversely during a read instruction the computer is unloading one of the-buffers while the drum is loading the other buffer.

Normally data will be transferred into and out of the buffers in 32 word groups called data sectors. The loading of a buffer shall not be started until it is empty and the unloading of a buffer shall not be started until it is full. However, the design of the Drum Controller shall provide the capability for correctly writing and reading data sectors of any length as the need arises. The situations where a variable length sector capability is required are those in which the number of data words to be written or read is not an integral multiple of 32, i.e. , a data block of 65 words would be written using two 32-word sectors and one 1-word sector.

Under normal circumstances, data transfer between the computer and Drum Controller can take place at a substantially higher word rate than that between the Drum and Drum Controller. Therefore, normally the computer will load/unload a buffer at a “Burst Rate” and then wait until the Drum has unloaded/loaded the alternate buffer. If, for some reason such as other program executions, the computer is unable to keep pace with the requirements of the Drum for data, the Drum Controller shall sense the condition and cause data transfers to/from the drum to cease until the Computer has had time to load/unload the buffer. This condition is called an Underrun during a write instruction and an Overrun during a read instruction.

The Drum Controller shall count the number of such occurrences during the execution of a read or write instruction and retain the count in the Error Count Status word.

3.5.4.4.4.4.4 Idle State and Interrupt Functions

While the Drum Controller is not actively executing an instruction it shall be in an idle state where internal controls are reset. Prior to the completion of all operational instructions, an Interrupt shall be sent to the Computer with the Instruction Status word or the requested Status word in the cases of the Status Request instructions. All instructions, except Master Clear and Read/Write Terminate shall start from the idle state and all instructions shall return the Drum Controller to the idle state following their completion.

During the execution of a read or write instruction, if a parity error is detected, an Interrupt with Instruction Status Word format shall be sent immediately to the computer (interleaved with the IDR’s in the case of a read instruction). However, this shall not terminate the instruction and the instruction shall be completed unless terminated by a subsequent computer instruction.

3.5.4 .4.4.4.5 Write Function Sequence

The following is the sequence of steps which shall occur during the execution of a write instruction:

(1) The computer acknowledges the EFR and sends the first word of the write instruction.

(2) The Drum Controller shall place a logic 0 on the EFR line and shall check the instruction code. If the code is that of the second word of the write instruction, a Sequential Error Interrupt shall be sent to the computer. When the instruction code is determined to be that of the first word of the write instruction, the EFR line shall be placed at logic 1.

(3) The computer acknowledges the EFR and sends the second word of the write instruction.

(4) The Drum Controller shall place a logic 0 on the EFR line and shall check the instruction code. If the code is that of any instruction other than the second word of the write instruction, master clear, or read/write terminate, a combinational Error Interrupt shall be sent to the Computer. When it is determined that the second word of the write instruction has been received, the addresses shall be checked for Address Error and Write Lockout Status. Detection of any of these error conditions shall cause an Interrupt to be sent to the Computer. If no error conditions are detected, the first data word shall be requested from the Computer.

(5) The Drum Controller shall place a logic 1 on the ODR line.

(6) The computer acknowledges the ODR and sends a 30-bit data word.

(7) The Drum Controller shall place a logic 0 on the ODR line, add the parity bits to the data word and place the 32-bit word in Buffer A.

(8) Steps (5), (6) and (7) shall be repeated until the buffer is filled.

(9) At this time two things shall occur. The Drum Controller shall start searching on the drum for the address where the data is to be written and the computer starts to load Buffer B with the sequence indicated by steps (5), (6) and (7).

(10) When the begin address is located (within one revolution) on the drum, the data in Buffer A shall be placed, one word at a time, into a parallel-to-serial register and shifted serially into the drum. A parallel parity check shall be made on each data word as it is placed into the register. A serial parity check shall be made on each byte of each data word as it is shifted into the drum. The data flow to the drum shall continue until Buffer A is empty.

(11) At this time the contents of Buffer B shall be written on the drum at their proper addresses in the same manner as described in step (10) and the computer loads Buffer A as in steps (5), (6) and (7).

(12) This alternate loading and unloading of the buffers shall continue until the Drum Controller has determined that the last addressed data word has been received from the computer. The Drum Controller shall, when it senses that the last addressed data word has been received, cease to send ODR signals to the computer and generate a full buffer condition if the total number of data words addressed was not an integral multiple of 32.

(13) The Drum Controller shall cause write operations to cease when it senses that the last addressed data word of the final buffer has been written.

(14) If, during the process of recording data on the drum, a parity error is detected, the Drum Controller shall send an Instruction Status word with an Interrupt to the computer indicating Parity Error Status as coon as the error is detected. The write operation shall continue until it either has been completed or has been terminated by the computer.

(15) If, during the process of recording data, the computer is unable to completely load one of the buffers by the time that the buffer contents must be written on the drum, the Drum Controller shall cause the recording process to cease for whatever number of drum revolutions (normally one) are needed for the computer to fill the buffer. This condition is called Underrun (Computer under runs the drum) and each such occurrence shall be counted and the count stored in the Error Count Status word.

(16) If no errors are detected during the instruction an Instruction Status Word Interrupt shall be sent to the computer indicating Normal Completion Status.

(17) when the computer acknowledges the Interrupt the Drum Controller shall reset the interrupt line and place a logic 1 on the EFR to the computer.

3.5.4.4.4.4.6 Read Function Sequence

The following is the sequence of steps which shall occur during the execution of a read instruction:

(1) The computer acknowledges the EFR and sends the first word of a read instruction.

(2) The Drum Controller shall place a logic 0 on the EFR line and shall check the instruction code. If the code is that of the second word of a read instruction, a Sequential Error Interrupt shall be sent to the computer. When the instruction code is determined to be that of the first word of a read instruction, a logic 1 shall be placed on the EFR line.

(3) The computer acknowledges the EFR and send the second word of the read instruction.

(4) The Drum Controller shall place a logic 0 on the EFR line and shall check the instruction code. If the code is that of any instruction other than the second word of a read instruction, master clear or read/write terminate, a Combinational Error Interrupt shall be sent to the computer. When it has been determined that the second word of a read instruction has been received, the addresses shall be checked for Address Error. If this condition is detected, an Address Error Interrupt shall be sent to the computer. If no error condition is detected, the Drum Controller shall start to search the drum for the begin address where a preamble word had been written.

(5) If a preamble word is not detected (within one revolution) at the begin address, a Sync Detect Error Status shall be sent with the Instruction Status Interrupt word to the computer. If the preamble word is detected, the reading of data shall proceed.

(6) The data words shall be read from the drum in a serial wanner and clocked into a serial-to-parallel register. As the words are placed into the register, each byte of each word shall undergo a serial parity check.

(7) As each 32 bit word is read, it shall be transferred into Buffer A.

(8) Steps (6) and (7) shall be repeated until Buffer A has been filled with 32 data words.

(9) The Drum Controller shall now switch to load Buffer B and shall proceed as described in steps (6), (7) and (8).

(10) The Drum Controller shall place a word from Buffer A on the computer Data Input lines and a logic 1 on the IDR line to the computer . As the data word is read from the buffer, a parallel parity check shall be made on the 32-bit word. The two parity bits shall be removed and the remaining 30-bit word shall be sent to the computer,

(11) The computer accepts the data word and acknowledges the IDR signal.

(12) The Drum Controller shall place a logic 0 on the IDR line and shall increment to the next word in Buffer A.

(13) Steps (10), (11) and (12) shall be repeated until all 32 words in Buffer A have been sent to the computer.

(14) As soon as the drum has filled Buffer B, two things shall occur. The computer unloads Buffer B as described in steps (10), (11) and (12) and the drum shall load Buffer A as described in steps (6), (7) and (8).

(15) This alternate loading and unloading of the buffers shall continue until the Drum Controller has determined that the last addressed data word has been received from the drum. The Drum Controller shall, when it senses that the last addressed data word has been received from the drum, cease to react data from the drum and generate a full buffer condition if the total number of data words addressed was not an integral multiple of 32.

(16) The Drum Controller shall send data to the Computer as described in steps (10), (11) and (12) until the last addressed word of the final buffer has been transmitted to the computer.

(17) If, during the process of reading data from the drum, a parity error is detected, the Drum Controller shall send an Instruction Status word with Interrupt to the computer indicating parity error status as soon as the error is detected. This Interrupt shall be interleaved with the IDR signals to the computer with no loss of data. The read operation shall continue until it either has been completed or has been terminated by the computer.

(18) If, during the process of reading data, the computer is unable to empty a buffer by the time it is required by the drum for the next data sector, the Drum Controller shall cause the reading process to cease for whatever number of drum revolutions (normally one) are needed for the computer to empty the buffer. This condition is called Overrun (Drum overruns the computer) and each such occurrence shall be counted and the count stored in the Error Count Status word.

(19) If no errors are detected during the instruction, an Instruction Status Interrupt shall be sent to the computer indicating Normal Completion Status.

(20) When the computer acknowledges the Interrupt, the Drum Controller shall reset the Interrupt line, and place a logic 1 on the EFR line to the computer.

3.5.4.4.4.4.7 Master Clear Function

The Master Clear Instruction shall be executed either in response to the EFR from the Drum Controller or by use of an E F with Force from the computer,

This instruction shall cause any instruction in process to be terminated and shall cause all status error data to be cleared. The contents of the Memory Protect Register shall not be altered by this instruction.

An Interrupt with the Instruction Status word shall be sent to the computer. After the computer acknowledges the Interrupt, the Drum Controller shall reset the Interrupt line and place a logic 1 on the EFR line to the computer.

3.5.4.4.4.4.8 Read/Write Terminate Function

The Read/Write Terminate Instruction shall be executed either in response to the EFR from the Drum Controller or by use of EF with Force from the computer.

This instruction shall cause a read or write instruction to be terminated but all status and error data shall remain unchanged.

An Interrupt with the Instruction Status word shall be sent to the computer. After the computer acknowledges the Interrupt, the Drum Controller shall reset the Interrupt line and place a logic 1 on the EFR line to the computer.

3.5.4.4.4.4.9 Status Function

The Instruction Status Interrupt word shall be sent to the computer following all operational instructions except for the two status request instructions. The status request instructions shall be executed as follows:

(1) The computer acknowledges the EFR and sends a status request instruction code (either Parity or Error Count).

(2) The Drum Controller shall place a logic 0 on the EFR line and check the instruction code of the word received from the computer.

(3) The Drum Controller shall place the requested status word on the data lines and a logic 1 on the Interrupt line to the computer.

(4) When the computer acknowledges the Interrupt, the Drum Controller shall reset the Interrupt line and place a logic 1 on the EFR line to the computer.

3.5.4.4.4.4.10 Memory Protect Function

The Drum Controller shall provide the capability to protect any combination of equal sized segments of the drum. Each section shall correspond to 32,768 consecutive addresses. It shall be possible to activate the protect features by means of both switches on the Control Panel or by means of a computer instruction.

The Memory Protect Function shall have the following features:

(1) when power is turned on or when complete DAMS initialization takes place, the Memory Protect Register shall be placed in the protect state (logic 1).

(2) When a switch is placed in the protected position, the corresponding register flip flop shall go to the protect (logic 1) state and remain there regardless of computer command.

(3) When a switch is place in the unprotected position, the corresponding register flip flop shall either be reset or set by the computer command.

(4) Switch 1 corresponds to the lowest 32,768 address codes. Switches 2 through 12 correspond to consecutive higher address groups with switch 12 corresponding to the highest 32,768 legal data addresses.

The Memory Protect Instruction operation sequence shall be as follows:

(1) The computer Ucknowledges the EFR and sends the Memory Protect Instruction Code.

(2) The Drum Controller shall place a logic 0 on the EFR line, check the instruction code, and clock the instruction memory protect bits to the Memory Protect Register.

(3) The Instruction Status word shall be placed on the data lines and a logic 1 shall be placed on the Interrupt line to the computer.

(4) When the computer acknowledges the Interrupt, the Drum Controller shall reset the Interrupt line and place a logic 1 on the EFR line to the computer.

3.5.4.4.4.4.11 Test Function

The DAMS shall have provisions for performing automatic and manual testing in order to meet the test requirements of this specification.

Manual testing shall be accomplished by using the features of the Maintenance Control Panel. There shall be two manual test modes with purposes as follows:

(1) Verify Mode shall be used in order to verify the data and control communication paths between the computer and the DAMS.

(2) Off Line Mode shall be used to permit the operator to perform all the instructions executed by the DAMS. The operational read and write instructions shall be executed in the following three modes; single instructions, repeat instruction execution without regard to error, and repeat instruction execution with halt on error. No communication shall take place with the Computer in Off Line Mode.

Automatic testing by means of computer instructions shall be provided in order that all areas of the Drum Controller and Magnetic Drum Memory are tested to the extent necessary in order that the fault detection and isolation requirements of this specification are met.

3.5.4.4.4.4.11.1 Diagnostic Test Mode Description

The diagnostics shall consist of 14 test modes for DAMS testing. The test mode codes and associated test loops are shown in the memory protect and test instruction word format. (See Figure 165.)

A description and sequence of operation for each of the test modes follows:

(1) TM-1 All Zeroes to Computer - This test mode shall enable a known condition of the 30 data input bits to be sent to the computer.

The test instruction shall be sent via the EFR/EF transfer sequence. The DAMMS shall set all computer input bits to a logic zero via the data input multiplexer and raise the EI. The input data transfer shall be accomplished by the EI/IA sequence.

(2) TM-2 All Ones to Computer - This test mode shall be similar to TM-1 except all input bits shall be set to a logic 1.

(3) TM-3 Computer Data to Computer - This test mode shall enable verification of the computer output data paths to the error count registers and the status input data paths from the error count registers.

In response to a TM-3 instruction code, the DAMS shall generate an ODR. The computer shall output a 30-bit data word which shall be loaded into the error count registers. The data shall be sent to the computer via the IDR/IA sequence.

(4) TM-4 Buffer A and B Load, Circulate and Unload - This test mode shall check the data paths from the computer to the buffers through the buffers, from the buffers to the computer.

Upon receipt of a TM-4 instruction code via an EFR/EF data transfer, the DAMS shall raise the ODR. The computer shall output 64 words, loading buffers A and B. When the loading is complete, the 64 words shall be sent to the computer via the IDR/IA data transfer. At the same time the data shall also be multiplexed and recirculated back into the buffers. The contents of buffers A and B shall be again unloaded to the computer by the IDR/IA transfer sequence.

(5) TM-5 Parity and Error Counters - During TM-5, the parity generators shall be disabled and the error counters shall be incremented to verify proper operation.

Test mode entry shall be via the EFR/EF data transfer. Output bit 21 shall exercise the byte or buffer priority logic and output bit 20 shall determine which parity bit generator is disabled. With output bit 20 a logic O, byte 1 parity shall be disabled and with output bit 20 a logic 1, byte 2 parity shall be disabled. Upon receipt of the test code, the DAMS shall generate an ODR which shall initiate a 64-word ODR/OA data transfer sequence. The bit contents of the computer data words shall determine correct or incorrect parity of the words loaded into buffers A and B.

Upon completion of the buffer loading, a 64 IDR/IA input sequence shall be initiated through the normal data paths. Any parity error detected during buffer unloading to the computer shall increment the buffer error, byte error and overrun/underrun counters. Upon detection of a parity error, with output bit 21 of the TM-5 instruction word a logic 1, the buffer error strobe shall precede the byte error strobe; with output 21 of the TM-5 instruction word a logic O, the byte error strobe shall precede the buffer error strobe.

Upon completion of the input data transfer, the instruction status word shall be sent to the computer via the EI/IA sequence. Any parity error detected shall set the parity error bit (bit 28) of the instruction status word. A computer initiated parity status and/or error count instruction shall be used to verify parity status bits and error count data.

Several TM-5 sequences shall be initiated to accumulate and verify full count of the error count registers. The error count data shall not be reset until a master clear, write/read instruction or any test instruction other than TM-5 is received.

(6) TM-6 Drum Fault Status Bits - This test mode shall exercise and verify the drum fault status register operation. TM- 6 shall verify DAMS status logic and data paths from the status registers to the computer.

Test mode entry shall be via the EFR/EF. The DAMS shall then raise the ODR to the computer. The computer shall respond with an OA word, the contents of which shall determine which of the register bits and drum fault indicators shall be set. If any or all of the OA word O0B09-04 is a logic 1, the corresponding status register bits shall be sent and the respective IB09-04 of the instruction status word shall indicate a drum fault. 0B03-00 of the OA word shall be used to test IB10 of the instruction status word.

Upon receipt of the OA, the DAMS shall raise the EI, enabling the instruction status word to the computer.

(7) TM-7 Address Logic and Error Address Counter - This test mode shall allow operational verification of the address counters, word counter, address comparators and parity error address counter. This shall be accomplished by using the byte error counter as a burst clock generator to increment the registers and counters.

Test mode entry shall require a two word EFR/EF sequence and one ODR/OA sequence:

(a) The first word shall load the computer and drum begin address registers and parity error address register.

(b) The second word shall load the instruction end address and word address counters. The status of bits 20 and 21 shall determine where the burst clocks are applied. Bit 20 shall inhibit or enable the burst clocks to the computer begin address and drum begin address registers. Bit 21 shall inhibit or enable the burst clocks to the instruction end address register and the track word address counter.

(c) The OA word shall load the byte error counter and determine the number of burst clocks to be generated.

Upon receipt of the OA, the byte error counter shall be enabled generating the predetermined number of burst clocks to increment the registers and counters. When the error counter is full, the DAMS shall raise the IDR, which shall result in the address comparator diagnostic data being supplied to the computer via the enabled data path. As the computer IA acknowledge is received, the DAMS shall send the parity status word to the computer via the EI/IA sequence for parity error address verification.

(8) TM-8 Control Logic - This test mode shall provide the capability for checking certain control signals within the DAMS not tested by the other DAMS test modes. The test shall be initiated by means of an instruction word from the computer using EFR/EF control sequent e. This word shall cause entry into the test mode and shall determine the behavior of the signals under test.

Following the E F word, the DAMS shall request a data word by means of the ODR/OA sequence. This word shall provide stimulus data for the signals to be tested and shall determine the number of burst clocks to be generated.

Following the generation of the specified number of burst clocks, the DAMS shall send a diagnostic word to the computer by means of IDR/IA control. The DAMS shall then send another diagnostic word to the computer by means of EI/IA control. These two diagnostic words shall provide 42 bits of test data to the computer.

(9) TM-9 Write/Read Address - The test mode shall verify the correct operation to select a specific track and perform a write or read operation. The Drum shall contain an area on each of the 384 addressable tracks for test purposes. The track test area shall be available even with the specific track included in a memory protect sector.

The TM- 9 instruction code shall be entered via the EFR/EF sequence with OB18-10 specifying the track address. The test area of the track shall be selected automatically by the DAMS logic. Bit 21 of the EF word shall define a write or read operation by a state of logic O or logic 1 respectively.

The actual operation after test mode entry shall be similar for a normal 64-word write (ODR/OA sequence) or read (IDR/IA sequence) instruction.

The instruction status word shall be reported to the computer via the EI/IA data transfer after the TM-9 instruction.

By repetitive use of TM-9 code with a different track address each time, the computer shall be able to write on or read from all 384 tracks in approximately five seconds.

(10) TM-10 Word Clock Rate - This test mode shall verify whether or not the correct number of word clocks is received from the Drum each revolution.

Following receipt of the TM-10 code via EFR/EF data transfer, the DAMS shall cause the error counters to count word clocks during selected portions of the test area. After the count has been accumulated, the DAMS shall send the error count status word to the computer via EI/IA control sequence.

(11) TM-11 Drum Write/Read - TM-11 shall verify the ability of the drum to write eight unique data patterns, read them back at three threshold levels and report any error detected,

Upon entry of the TM-11 instruction code, the drum shall automatically write the first of eight possible data patterns on all tracks in the test sector. The operation shall then switch to the read mode, and the test data shall be read at normal, low and high threshold levels. The sequence shall be repeated for each of the seven remaining data patterns.

Upon completion of the read operation on the last data pattern on track 383 at high threshold, the EI shall then be generated and the instruction status word shall be sent to the computer. The status word shall contain no useful information, but generation of the EI shall indicate a completed test.

Any errors detected shall be loaded into buffers A and B through the normal ‘data paths. The errors shall be stored in the buffers and reported via IDR/IA data transfer as either buffer A and B is filled or upon completion of the test before the EI is generated.

A forced error switch shall allow the error generation logic to be checked. Depression of the forced error switch shall cause an error word to be loaded into Buffer A or B for each of the tracks, with each pattern, on high and low threshold in the read mode except for the last pattern at high threshold on the last data track. Depression of the error switch must be done prior to initiation of the TM-11 EFR/EF word.

(12) TM-12 Data Paths and Parity Check - This test mode shall verify the data paths and byte parity logic of the drum by circulating data through the drum data paths.

TM-18 teat code when entered via EFR/EF sequence shall cause the DAMS to request one word of data from the computer via ODR/OA sequence. The data word when received shall be stored in Buffer A.

The DAMS shall then circulate 16 bits of this data word through the drum data paths and byte putty logic and place the circulated data in Buffer B.

The Data word in Buffer B shall then be transferred to the Computer via IDR/IA control. Following the acknowledgement of the IDR data transfer, the DAMS shall send the error count word to the computer via EI/IA control sequence.

(13) TM-13 Drum Status - This test mode shall verify the drum fault status Signals with the exception of the MDM temperature shutdown status by simulating the l xistence *of* a fault on the drum status line to the drum fault registers in the instruction status logic.

Upon receipt of the TM-13 instruction code via the EFR/EF sequence, the DAMS shall cause the drum to simulate a fault on all the drum status lines. The active drum fault status lines shall cause all drum fault registers to set. The DAMS shall then generate an EI reporting an instruction status word for computer verification of the drum fault status bits.

(14) TM-14 Temperature Error Shutdown - TM-14 shall verify proper operation of the shutdown circuit in the DAMS and Logic Unit 4.

The test shall be initiated by means of an instruction word from the computer using EFR/EF contro1.

The drum shall generate a speed error condition which shall cause the shutdown of drum motor drive power. The DAMS shall then send the instruction status word to the computer with EI/I4 control.

The DAMS shall then send a simulated temperature shutdown error signal to the temperature shutdown logic. This logic shall then time out a delay of about three seconds and shut down all rower to the drum. The instruction status word shall again be sent to the computer with an EI/IA.

Recovery from this test shall be accomplished by the computer sending either a Master Clear or Read/Write Terminate instruction to the DAMS using an “E F with force".

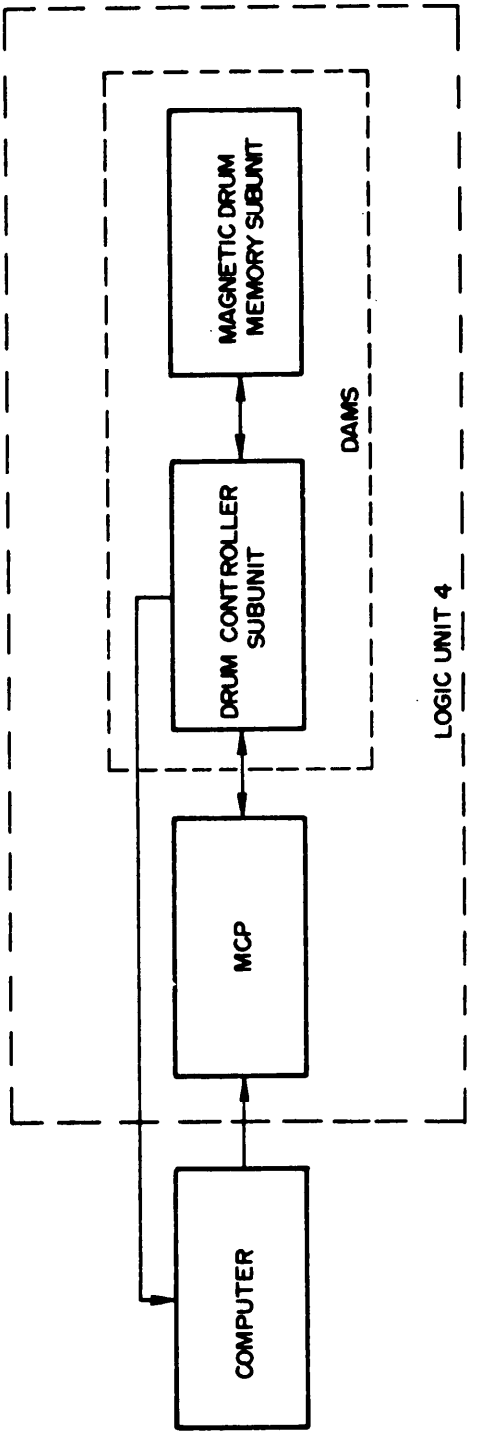


Figure 151. Drum Auxiliary Memory Subsystem Block Diagram

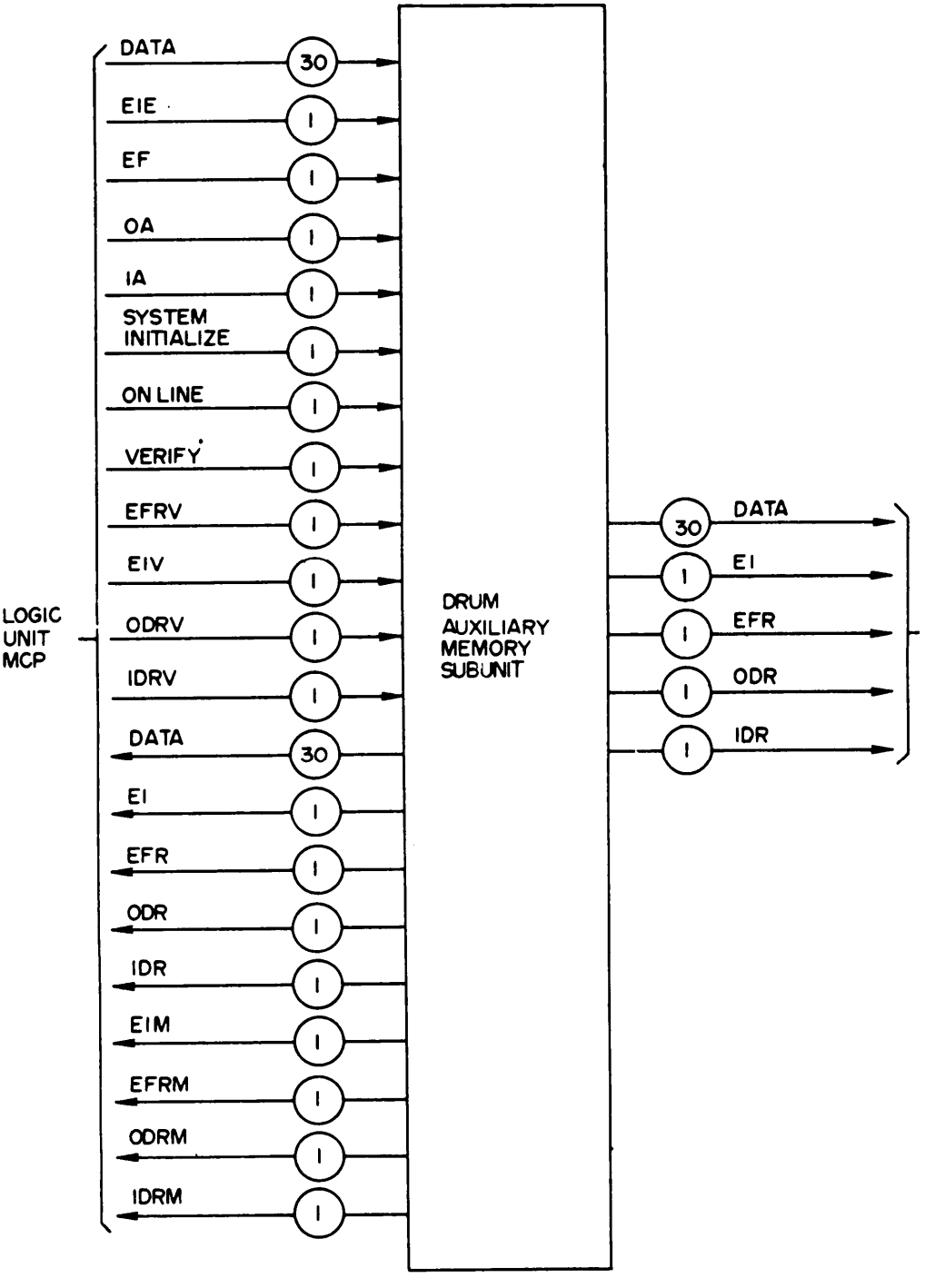


Figure 152. DAMS Functional Flow Diagram

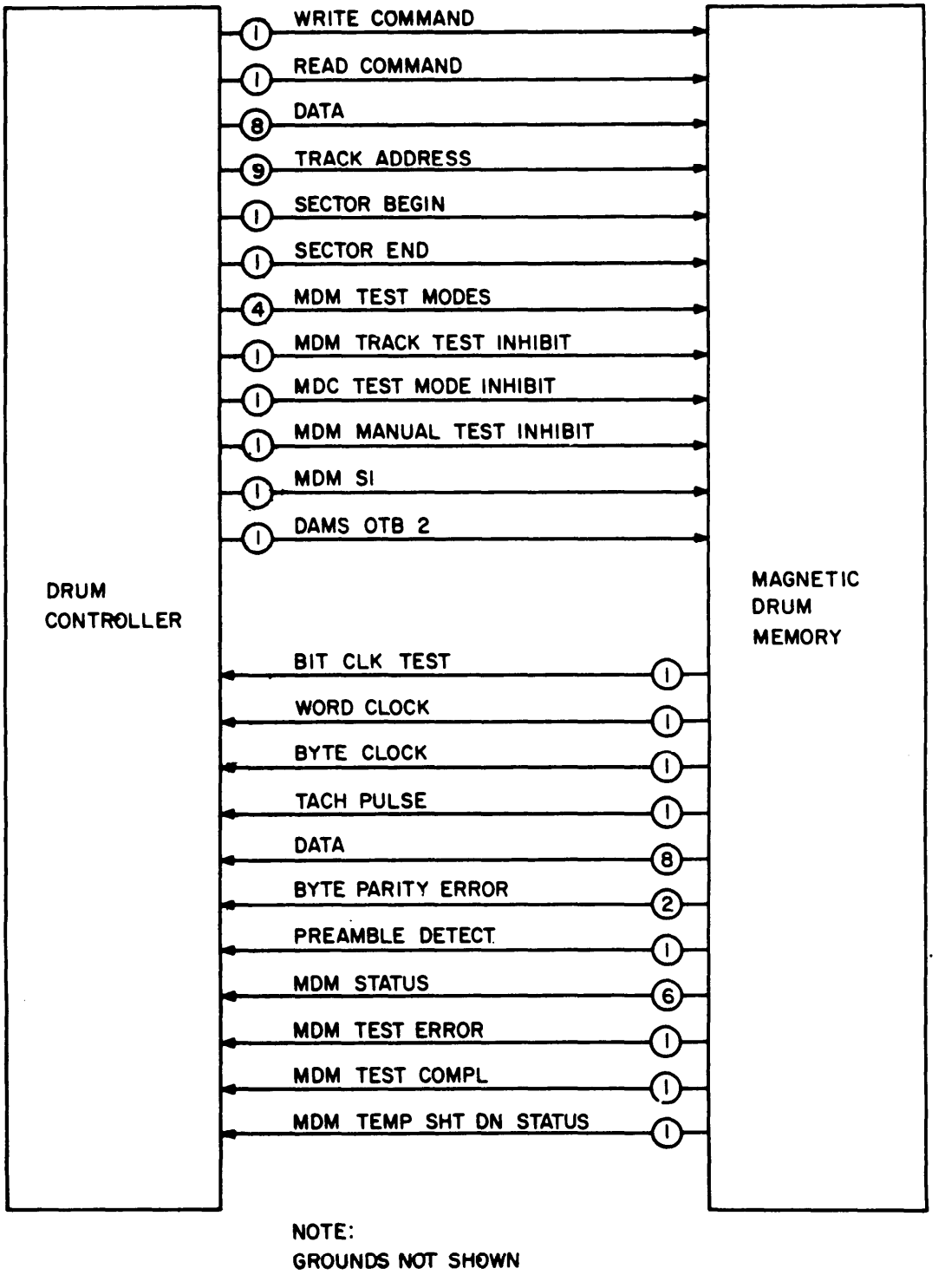


Figure 153. Magnetic Drum Memory/Drum Controller Interface

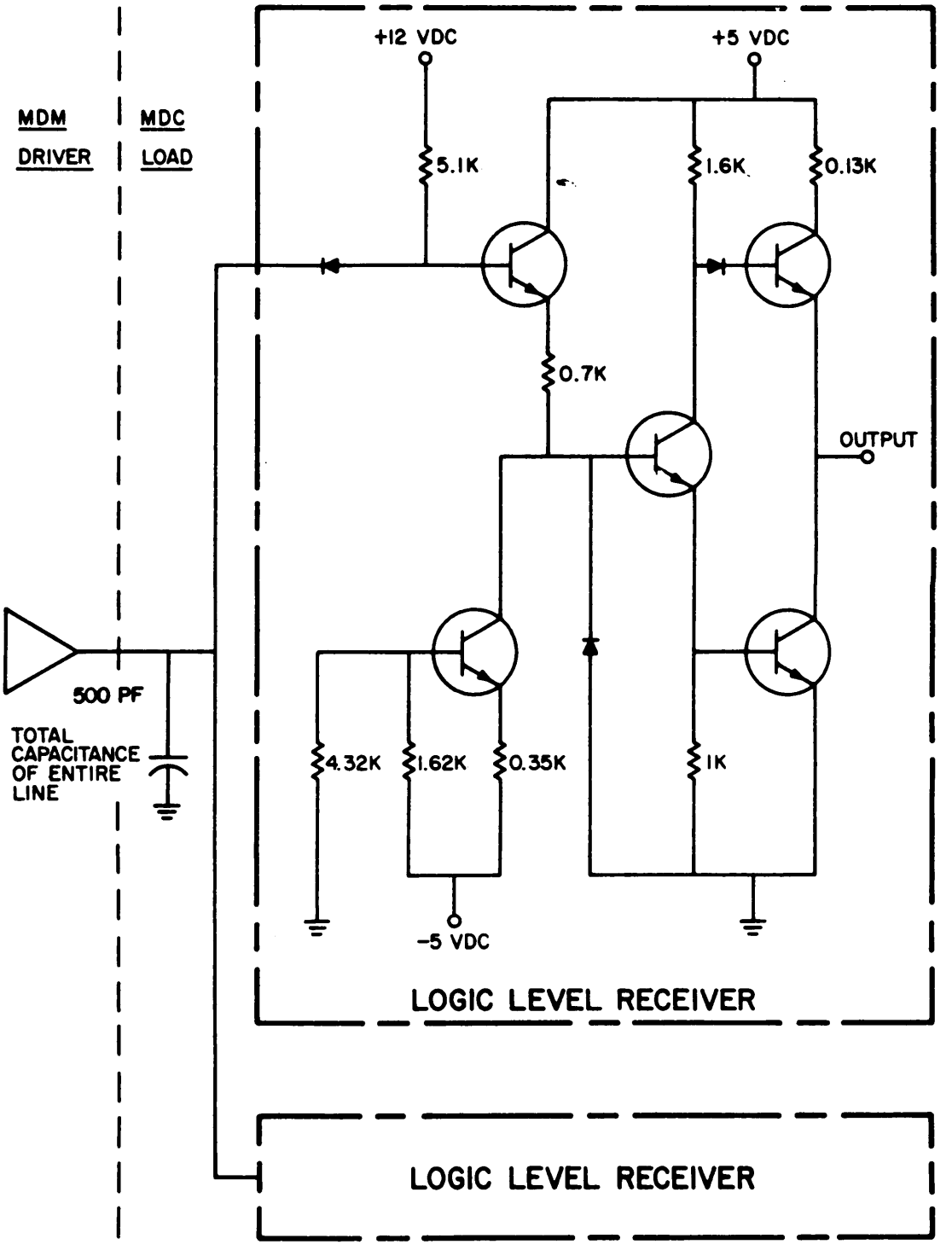
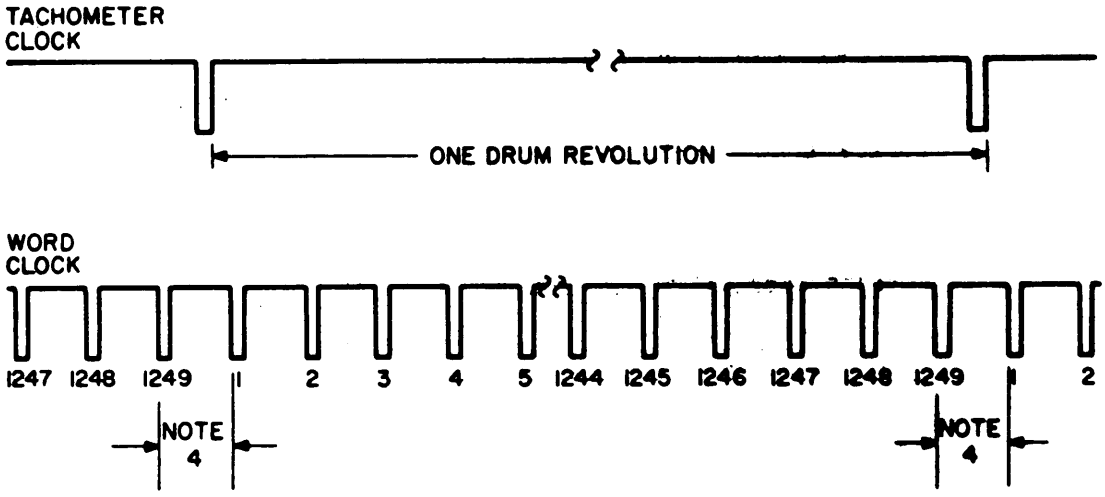


Figure 154. MDC Load f or Magnetic Drum Memory Interface Signal Drivers



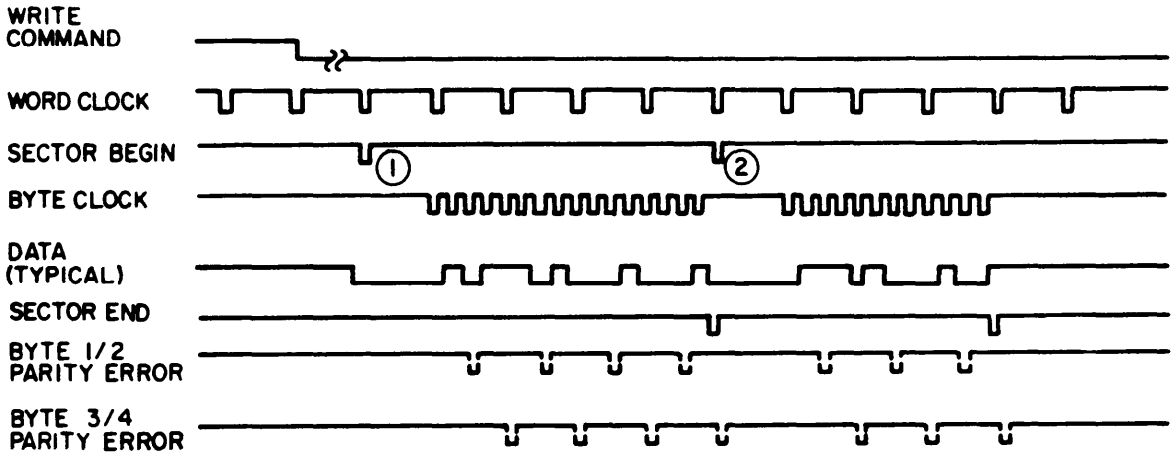
NOTES:

1. THE TIME BETWEEN CONSECUTIVE WORD CLOCK PULSES SHALL BE 32 BIT CLOCK TIMES UNLESS SPECIFIED OTHERWISE.
2. THE TACHOMETER CLOCK PULSE SHALL PRECEDE WORD CLOCK PULSE NO. 1 BY AT LEAST 8 BIT CLOCK TIMES.
3. THE TACHOMETER CLOCK PULSE SHALL FOLLOW WORD CLOCK PULSE NO. 1249 BY AT LEAST 8 BIT CLOCK TIMES.
4. THE TIME BETWEEN WORD CLOCK PULSES NO. 1249 AND NO. 1 NEED NOT BE 32 BIT CLOCK TIMES BUT SHALL BE NO LESS THAN 16 NOR MORE THAN 48 BIT CLOCK TIMES.
5. ALL PULSE WIDTHS IN THE ABOVE CLOCK TRAINS SHALL BE NO LESS THAN 0.55 MICROSECOND NOR MORE THAN 0.7 MICROSECOND.
6. THE FOLLOWING EXPRESSION SHALL BE USED IN DETERMINING TIME PERIODS FOR THE ABOVE SIGNALS AS REQUIRED:

   $T = [\,(312.8N)\,(1.0 \pm 0.01) \pm 50\,]$ NANOSECONDS

   N = NUMBER OF BIT TIMES

Figure 155. Continuoes Clock Signal Timing Diagram



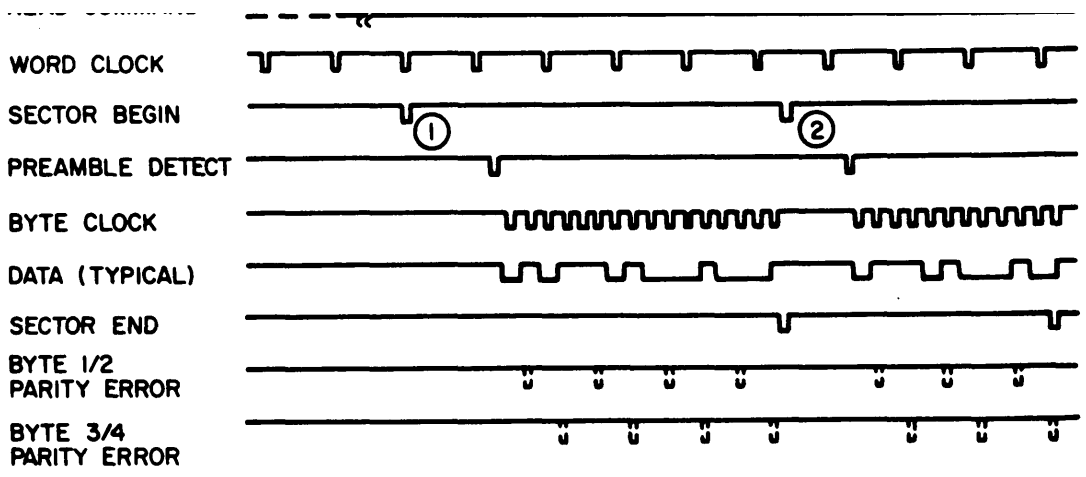
NOTES:

1. PARITY ERROR, WORD CLOCK, AND BYTE CLOCK PULSE WIDTHS SHALL BE NO LESS THAN 0.55 MICROSECOND AND NO MORE THAN 0.70 MICROSECOND. THE SECTOR BEGIN PULSE WIDTH AND SECTOR END PULSE WIDTH SHALL BE 0.85 ± 0.30 MICROSECONDS.
2. THE DATA SHALL BE STABLE DURING AND FOR 0.25 MICROSECOND BEFORE AND 0.15 MICROSECOND AFTER THE BYTE CLOCK PULSE.
3. TIME BETWEEN CONSECUTIVE BYTE CLOCKS OF A DATA SECTOR SHALL BE EQUAL TO 8 BIT CLOCK TIMES.
4. THE FIRST OF THE BYTE CLOCK PULSES OF A DATA SECTOR SHALL BE DELAYED BY NO MORE THAN 35.5 BIT CLOCK TIMES NOR LESS THAN 33 BIT CLOCK TIMES FROM THE SECTOR BEGIN PULSE.
5. THE LEADING EDGE OF THE SECTOR END PULSE SHALL OCCUR BETWEEN 0 AND 1.0 MICROSECOND AFTER THE LEADING EDGE OF THE LAST BYTE CLOCK OF THE DATA SECTOR.
6. TIME BETWEEN CONSECUTIVE LOCATIONS OF POSSIBLE BYTE 1/2 PARITY ERROR PULSES SHALL BE EQUAL TO 32 BIT CLOCK TIMES. TIME DELAY FROM THE TRAILING EDGE OF THE FIRST BYTE CLOCK PULSE OF A DATA SECTOR TO THE LEADING EDGE OF THE FIRST POSSIBLE BYTE 1/2 PARITY ERROR PULSE SHALL NOT BE LESS THAN 15.5 NOR EXCEED 18.5 BIT CLOCK TIMES.
7. TIME BETWEEN CONSECUTIVE LOCATIONS OF POSSIBLE BYTE 3/4 PARITY ERROR PULSES SHALL BE EQUAL TO 32 BIT CLOCK TIMES. TIME DELAY FROM THE FIRST POSSIBLE BYTE 1/2 PARITY ERROR PULSE TO THE FIRST POSSIBLE BYTE 3/4 PARITY ERROR PULSE SHALL NOT BE LESS THAN 15.5 NOR EXCEED 16.5 BIT CLOCK TIMES.
8. THE SECOND OF THE SECTOR BEGIN PULSES SHOWN, (2), CAN OCCUR AS SHOWN OR IN COINCIDENCE WITH ANY OF THE FOLLOWING WORD CLOCK PULSES.
9. THE FOLLOWING EXPRESSION SHALL BE USED IN DETERMINING TIME PERIODS AND PULSE WIDTHS FOR THE MDM/MDC SIGNALS AS REQUIRED:

   T = [(312.8N) (1.0±0.01)±50] NANOSECONDS

   N = NUMBER OF BIT TIMES

Figure 156. Write Operation Timing Diagram



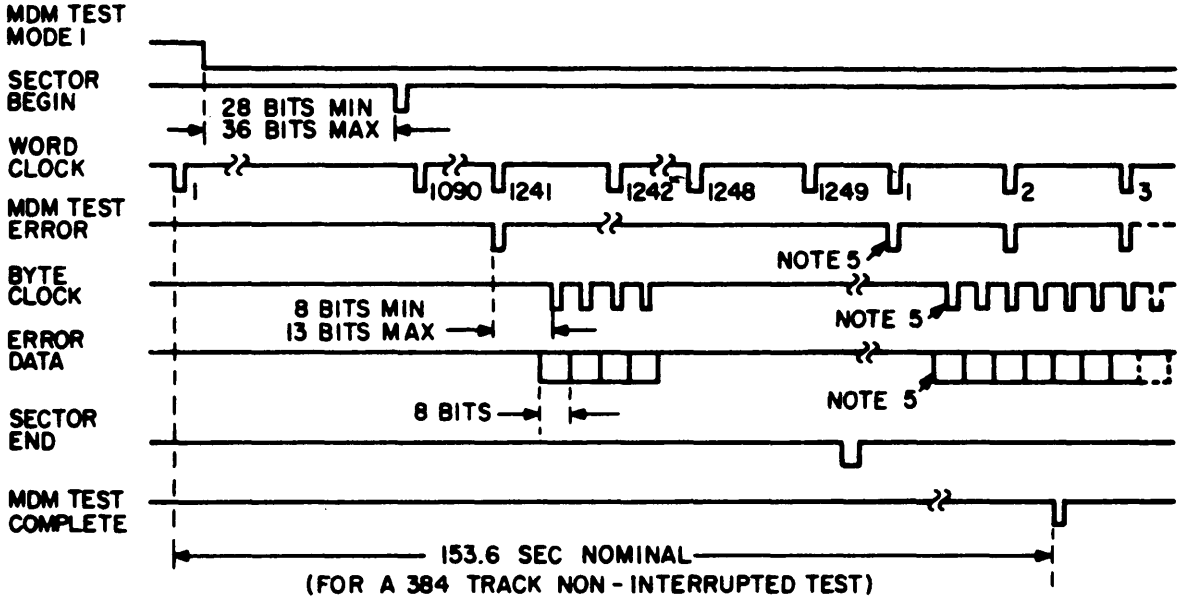
NOTES:

1. UNLESS OTHERWISE NOTED, PULSE WIDTHS OF ALL PULSES SHALL BE BETWEEN 0.55 AND 0.70 MICROSECOND. THE SECTOR END AND SECTOR BEGIN PULSE WIDTHS SHALL BE 0.85 ± 0.30 MICROSECOND. THE SECTOR BEGIN PULSE WHEN COINCIDENT WITH THE SECTOR END PULSE SHALL HAVE A PULSE WIDTH OF 0.85 ± 0.30 MICROSECOND.
2. WHEN THE READING OF A DATA SECTOR IMMEDIATELY FOLLOWS THE COMPLETION OF A PREVIOUS DATA SECTOR, THE SECTOR BEGIN PULSE FOR THE SECOND DATA SECTOR WILL BE COINCIDENT WITH THE SECTOR END PULSE OF THE FIRST DATA SECTOR. IF THE SECOND SECTOR WERE READ ON ANOTHER DRUM REVOLUTION, ITS SECTOR BEGIN PULSE WOULD BE IN THE NORMAL POSITION COINCIDENT WITH THE NEXT EARLIER WORD CLOCK PULSE.
3. THE PREAMBLE DETECT PULSE SHALL OCCUR NO MORE THAN 43.5 NOR LESS THAN 41 BIT CLOCK TIMES AFTER THE NORMAL SECTOR BEGIN PULSE POSITION.
4. THE DATA SHALL BE STABLE DURING AND FOR 0.25 MICROSECOND BEFORE AND 0.5 MICROSECOND AFTER THE BYTE CLOCK PULSE.
5. THE TIME BETWEEN CONSECUTIVE BYTE CLOCKS OF A DATA SECTOR SHALL BE EQUAL TO 8 BIT CLOCK TIMES.
6. THE FIRST OF THE BYTE CLOCK PULSES OF A DATA SECTOR SHALL BE DELAYED BY NO MORE THAN 8.5 NOR LESS THAN 7.5 BIT CLOCK TIMES AFTER THE PREAMBLE DETECT PULSE.
7. THE LEADING EDGE OF THE SECTOR END PULSE WILL OCCUR BETWEEN 0 AND 1.0 MICROSECOND AFTER THE LEADING EDGE OF THE LAST BYTE CLOCK PULSE OF THE DATA SECTOR.
8. TIME BETWEEN CONSECUTIVE LOCATIONS OF POSSIBLE BYTE 1/2 PARITY ERROR PULSES SHALL BE EQUAL TO 32 BIT CLOCK TIMES. THE FIRST POSSIBLE BYTE 1/2 PARITY ERROR PULSE LOCATION SHALL OCCUR NO MORE THAN 100 NANOSECONDS FROM THE LEADING EDGE OF THE SECOND BYTE CLOCK OF THE DATA SECTOR.
9. TIME BETWEEN CONSECUTIVE LOCATIONS OF POSSIBLE BYTE 3/4 PARITY ERROR PULSES SHALL BE EQUAL TO 32 BIT CLOCK TIMES. THE FIRST POSSIBLE BYTE 3/4 PARITY ERROR PULSE LOCATION SHALL OCCUR NO MORE THAN 100 NANOSECONDS FROM THE LEADING EDGE OF THE FOURTH BYTE CLOCK OF THE DATA SECTOR.
10. THE SECOND OF THE SECTOR BEGIN PULSES SHOWN, (2) CAN OCCUR AS SHOWN OR IN COINCIDENCE WITH ANY OF THE FOLLOWING WORD CLOCK PULSES.
11. THE FOLLOWING EXPRESSION SHALL BE USED IN DETERMINING TIME PERIODS AND PULSE WIDTHS FOR THE MDM/MDC SIGNALS AS REQUIRED:

    $T = [(312.8N)(1.0 \pm 0.01) \pm 50]$ NANOSECONDS

    N = NUMBER OF BIT TIMES

Figure 157. Read Operation Timing Diagram



NOTES:

1. THE WORD CLOCK, MDM TEST ERROR, BYTE CLOCK AND MDM TEST COMPLETE PULSE WIDTHS SHALL BE NO LESS THAN 0.55 MICROSECOND AND NO MORE THAN 0.70 MICROSECOND. THE SECTOR BEGIN PULSE WIDTH SHALL BE 0.85 ± 0.30 MICROSECOND.
2. THE ERROR DATA SHALL BE STABLE DURING AND FOR 0.25 MICROSECOND BEFORE AND 0.5 MICROSECOND AFTER THE BYTE CLOCK PULSE.
3. TIME BETWEEN CONSECUTIVE BYTE CLOCKS SHALL BE EQUAL TO 8 BIT TIMES.
4. THE SECTOR END PULSE WIDTH SHALL BE 0.85 ± 0.30 MICROSECOND. THE LEADING EDGE SHALL OCCUR BETWEEN 12 TO 19 BIT TIMES AFTER THE LEADING EDGE OF WORD CLOCK 1249 AS SHOWN ABOVE OR ANY TIME ASYNCHRONOUSLY THEREAFTER.
5. THE MDM TEST ERROR PULSE, BYTE CLOCKS AND ERROR DATA SHALL BE CONTINUOUSLY REPEATED FOR EACH WORD CLOCK EXCEPT FOR WORD CLOCKS 1242 TO AND INCLUDING 1249 AS SHOWN ABOVE IF NO SECTOR END PULSE IS SENT TO THE MDM.
6. THE LEADING EDGE OF THE MDM TEST COMPLETE PULSE SHALL NOT OCCUR EARLIER THAN THE TRAILING EDGE OF THE SECTOR END PULSE.
7. THE FOLLOWING EXPRESSION SHALL BE USED IN DETERMINING THE PERIODS AND PULSE WIDTHS FOR THE MDM/MDC SIGNALS AS REQUIRED:

   $T = [(312.8N)(1.0 \pm 0.01) \pm 50]$ NANOSECONDS;

   N = NUMBER OF BIT TIMES

Figure 158. MDM Test Mode 1 Timing Diagram

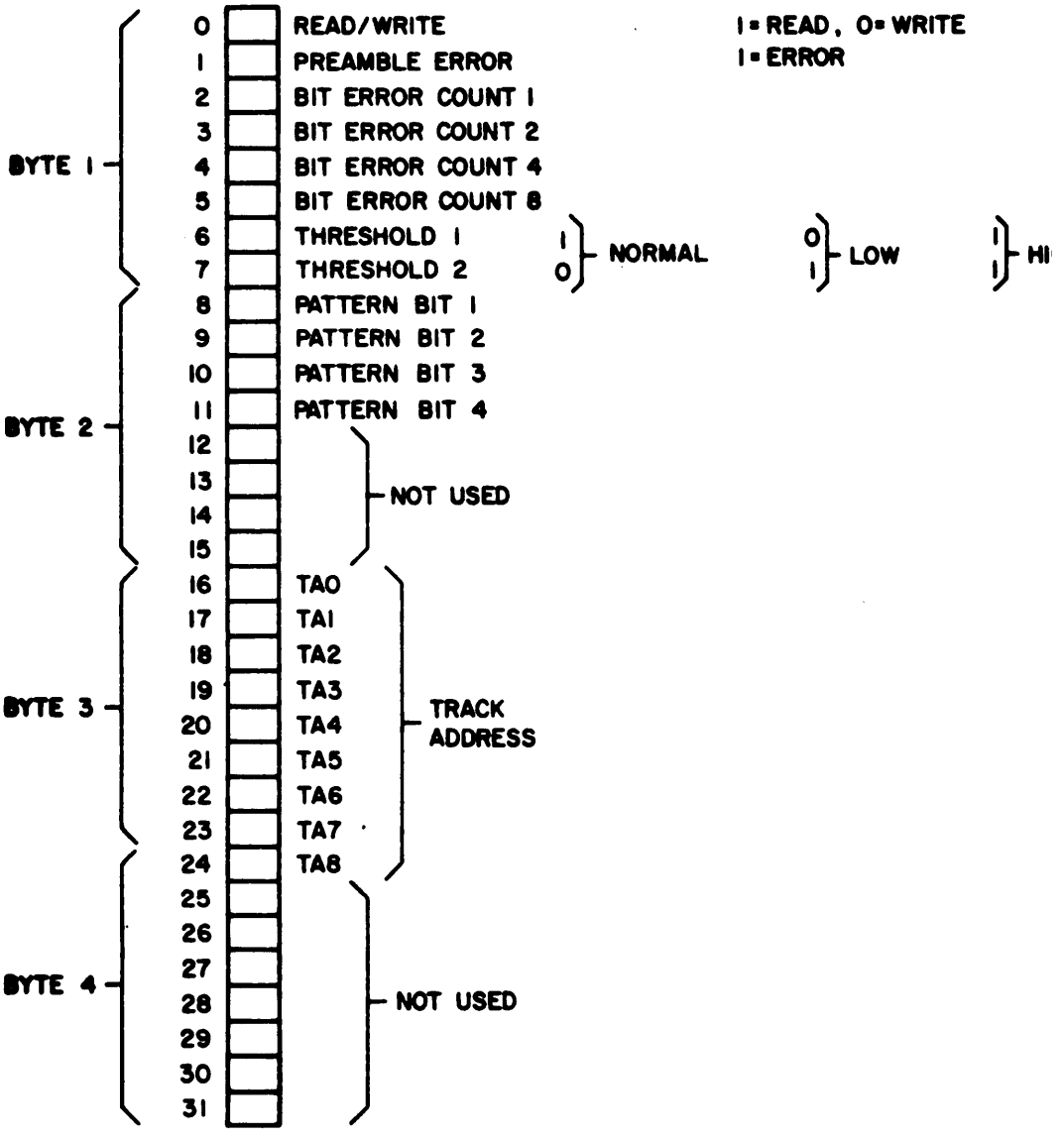
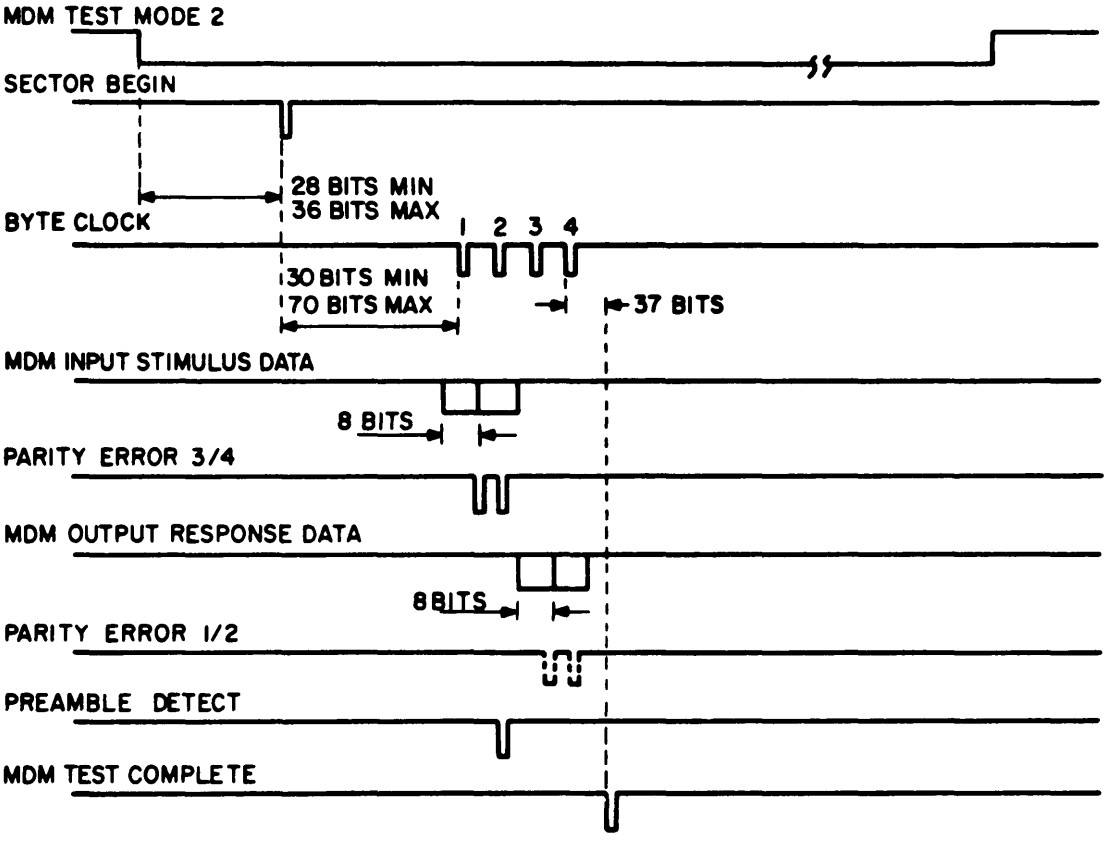


Figure 159. MDM Test Mode 1 Status Word Format



NOTES:

1. THE BYTE CLOCK, PARITY ERROR 3/4, PARITY ERROR 1/2, PREAMBLE DETECT AND MDM TEST COMPLETE PULSE WIDTHS SHALL BE NO LESS THAN 0.55 MICROSECOND AND NO MORE THAN 0.70 MICROSECOND. THE SECTOR BEGIN PULSE WIDTH SHALL BE 0.85 ± 0.30 MICROSECOND.
2. THE MDM INPUT STIMULUS AND OUTPUT RESPONSE DATA SHALL BE STABLE DURING AND FOR 0.25 MICROSECOND BEFORE AND 0.5 MICROSECOND AFTER THE BYTE CLOCK PULSE.
3. TIME BETWEEN CONSECUTIVE BYTE CLOCKS SHALL BE EQUAL TO 8 BIT TIMES.
4. THE FIRST PARITY ERROR 3/4 PULSE SHALL OCCUR NO LESS THAN 1.5 BITS NOR MORE THAN 4.5 BITS FROM THE LEADING EDGE OF THE FIRST BYTE CLOCK PULSE. THE SECOND PARITY ERROR 3/4 PULSE SHALL OCCUR NO MORE THAN 100 NANOSECONDS FROM THE LEADING EDGE OF THE SECOND BYTE CLOCK PULSE.
5. THE FIRST PARITY ERROR 1/2 PULSE SHALL OCCUR NO LESS THAN 1.5 BITS NOR MORE THAN 4.5 BITS FROM THE LEADING EDGE OF THE THIRD BYTE CLOCK PULSE. THE SECOND PARITY ERROR 1/2 PULSE SHALL OCCUR NO MORE THAN 100 NANOSECONDS FROM THE LEADING EDGE OF THE FOURTH BYTE CLOCK PULSE.
6. THE PREAMBLE DETECT PULSE SHALL OCCUR NO MORE THAN 100 NANOSECONDS FROM THE LEADING EDGE OF THE SECOND BYTE CLOCK PULSE.
7. THE FOLLOWING EXPRESSION SHALL BE USED IN DETERMINING TIME PERIODS AND PULSE WIDTHS FOR THE MDM/MDC SIGNALS AS REQUIRED:

   $T = [\ (312.8\ N)\ (1.0 \pm 0.01) \pm 50\ ]$ NANOSECONDS;

   N = NUMBER OF BIT TIMES

Figure 160. MDM Test Mode 2. Timing Diagram

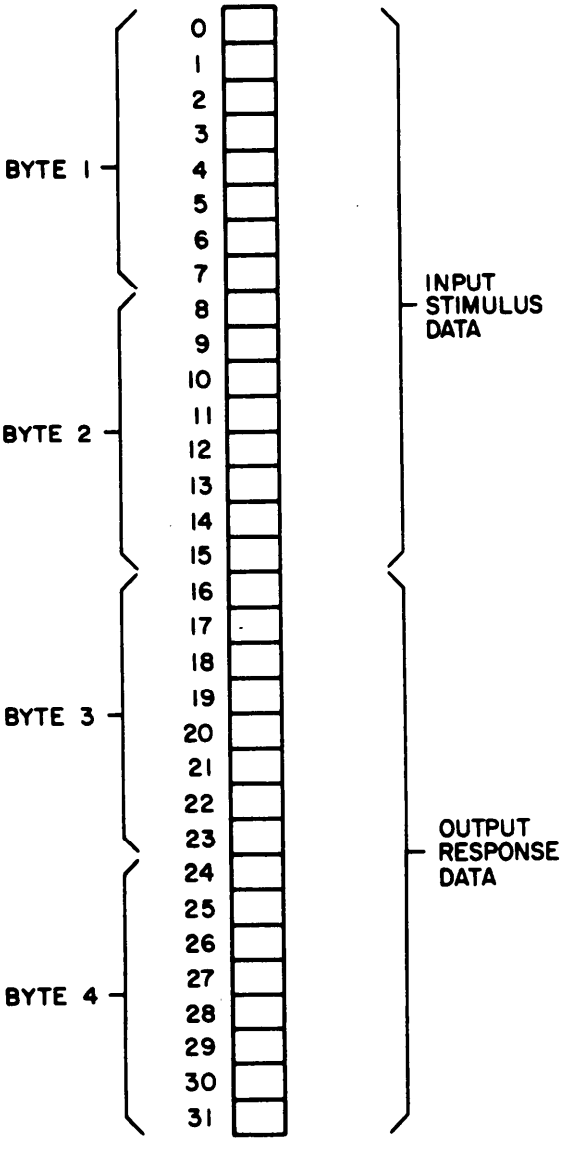
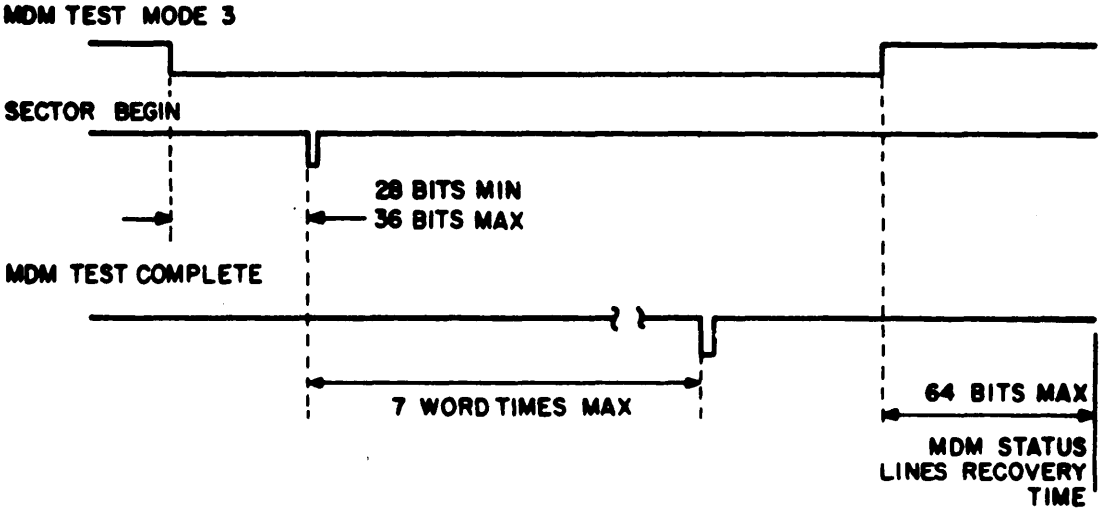


Figure 161. MDM Test Mode 2 *Status* Word Format

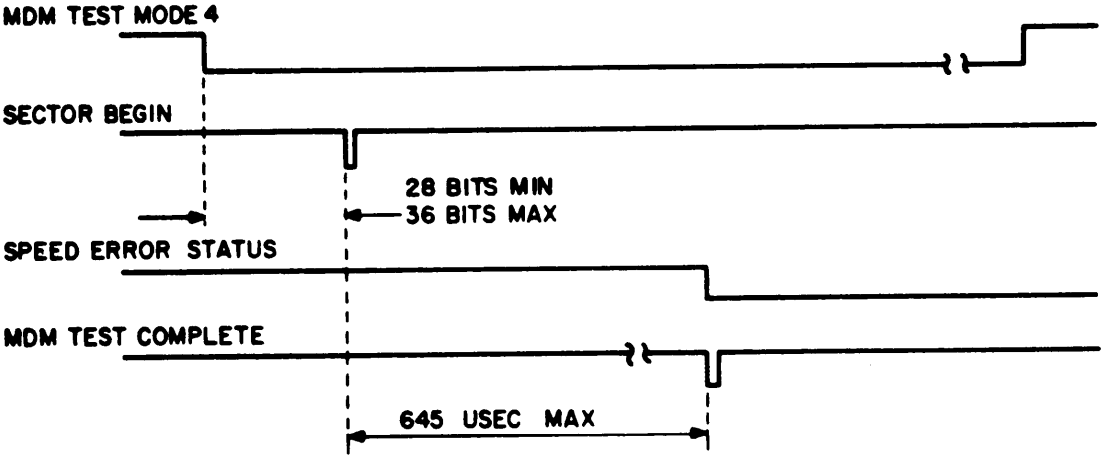


NOTES:

1. THE MDM TEST COMPLETE PULSE WIDTH SHALL BE NO LESS THAN 0.55 MICROSECOND AND NO MORE THAN 0.70 MICROSECOND. THE SECTOR BEGIN PULSE WIDTH SHALL BE 0.85 ± 0.30 MICROSECOND.
2. THE FOLLOWING EXPRESSION SHALL BE USED IN DETERMINING TIME PERIODS AND PULSE WIDTHS FOR THE MDM/MDC SIGNALS AS REQUIRED:

$$T = [(312.8N)(1.0 \pm 0.01) \pm 50] \text{ NANOSECONDS; } N = \text{NUMBER OF BIT TIMES}$$

Figure 162. MDM Test Mode 3 Timing Diagram

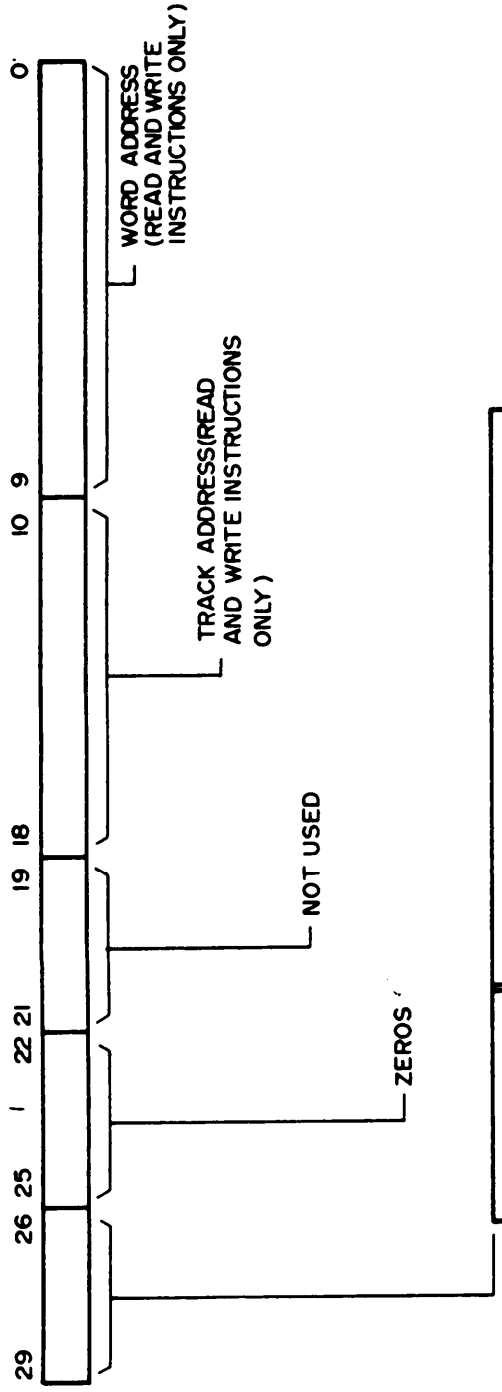


NOTES:

1. THE MDM TEST COMPLETE PULSE WIDTH SHALL BE NO LESS THAN 0.55 MICROSECOND AND NO MORE THAN 0.70 MICROSECOND. THE SECTOR BEGIN PULSE WIDTH SHALL BE 0.85 ± 0.30 MICROSECOND.
2. THE FOLLOWING EXPRESSION SHALL BE USED IN DETERMINING TIME PERIODS AND PULSE WIDTHS FOR THE MDM/MDC SIGNALS AS REQUIRED:

$$T = [(312.8N)\ (1.0 \pm 0.01) \pm 50]$$ NANOSECONDS; N=NUMBER OF BIT TIMES.

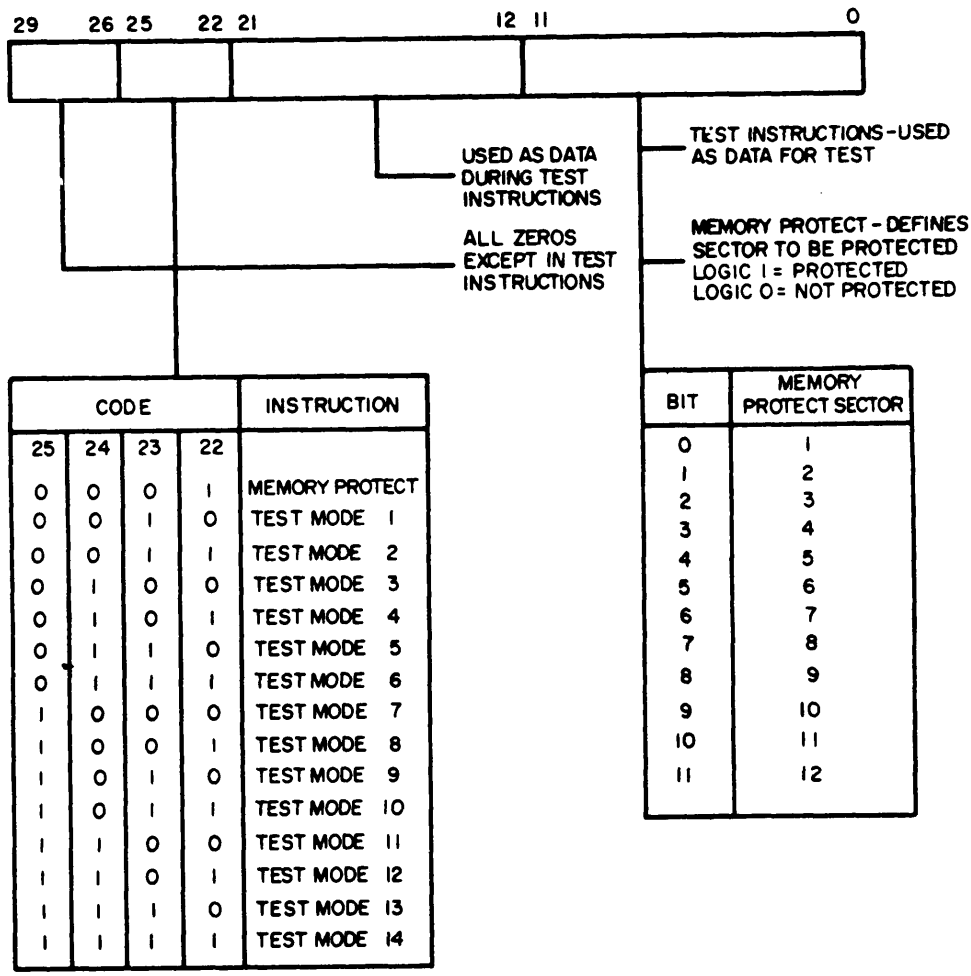
Figure 163. MDM Test Mode 4 Timing Diagram



CODE 29 28 27 26	INSTRUCTION
0 0 0 1	FIRST WORD OF WRITE INSTRUCTION
0 0 1 0	SECOND WORD OF WRITE INSTRUCTION
0 1 0 0	FIRST WORD OF READ INSTRUCTION
1 0 0 0	SECOND WORD OF READ INSTRUCTION
1 1 1 0	READ/WRITE TERMINATE
1 1 0 1	PARITY STATUS REQUEST
1 0 1 1	ERROR COUNT REQUEST
0 1 1 1	MASTER CLEAR

NOTE: UNLISTED CODES ARE ILLEGAL

Figure 164. Operational Instruction Word Formats



CODE				INSTRUCTION
25	24	23	22	
0	0	0	1	MEMORY PROTECT
0	0	1	0	TEST MODE 1
0	0	1	1	TEST MODE 2
0	1	0	0	TEST MODE 3
0	1	0	1	TEST MODE 4
0	1	1	0	TEST MODE 5
0	1	1	1	TEST MODE 6
1	0	0	0	TEST MODE 7
1	0	0	1	TEST MODE 8
1	0	1	0	TEST MODE 9
1	0	1	1	TEST MODE 10
1	1	0	0	TEST MODE 11
1	1	0	1	TEST MODE 12
1	1	1	0	TEST MODE 13
1	1	1	1	TEST MODE 14

BIT	MEMORY PROTECT SECTOR
0	1
1	2
2	3
3	4
4	5
5	6
6	7
7	8
8	9
9	10
10	11
11	12

Figure 165. DAMS Memory Protect and Teat Instruction Word Format

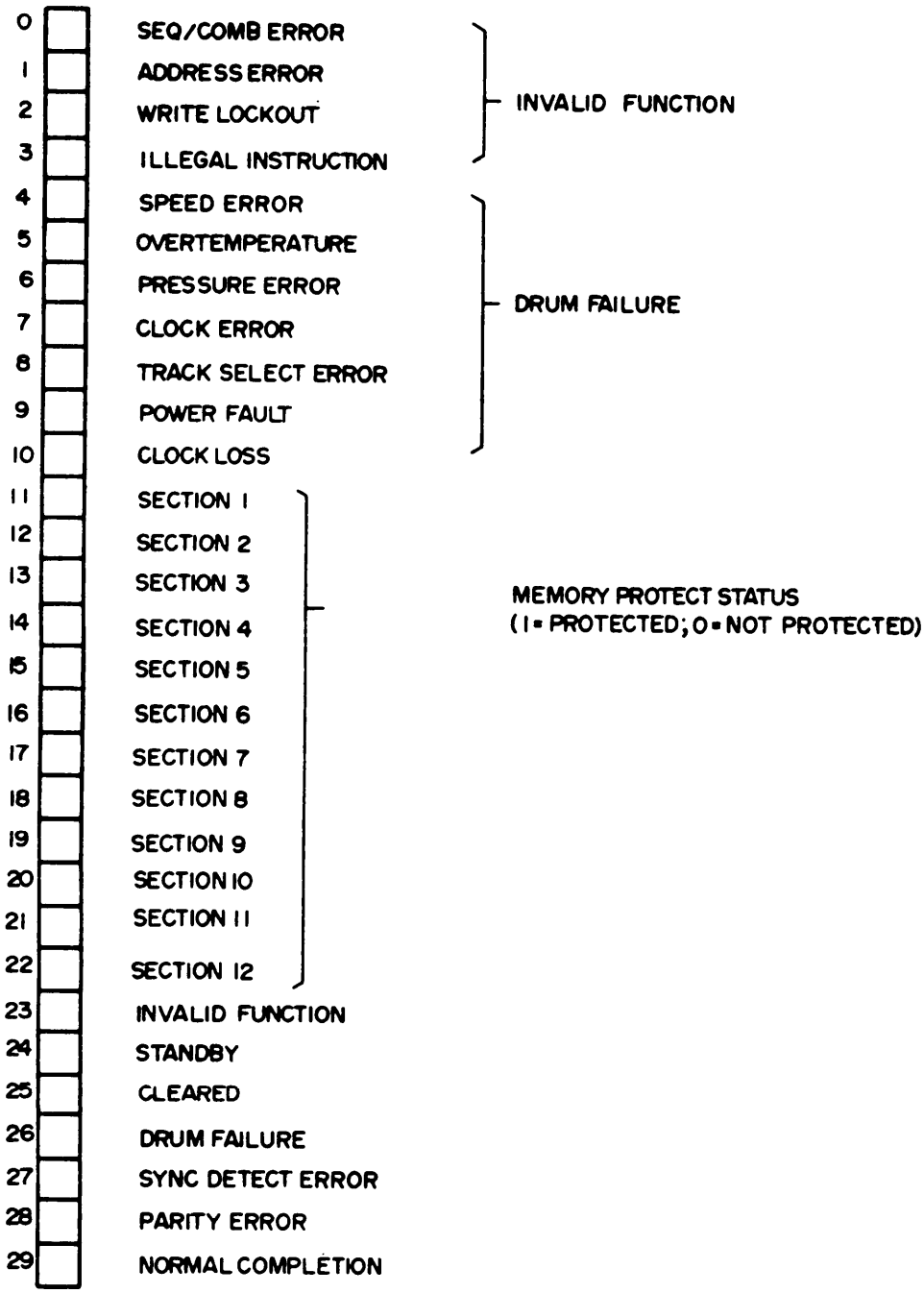


Figure 166. Instruction Satus Interrupt Word Format

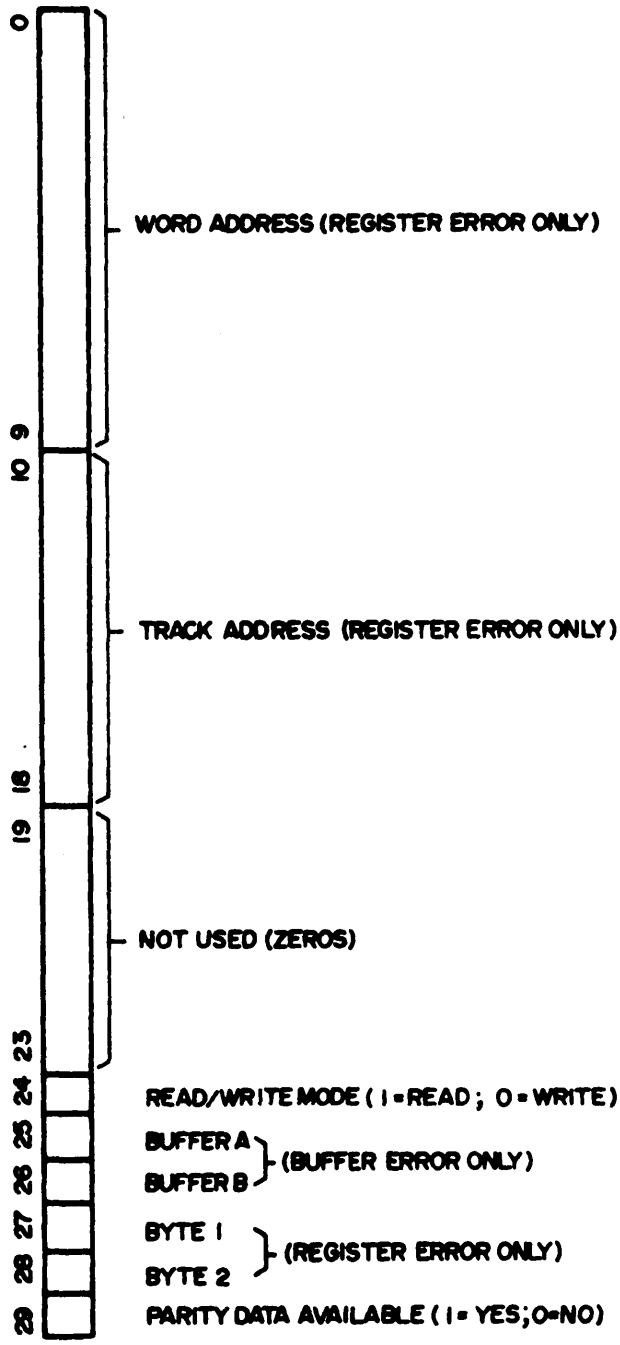


Figure 167. Parity Status Interrupt Word Format

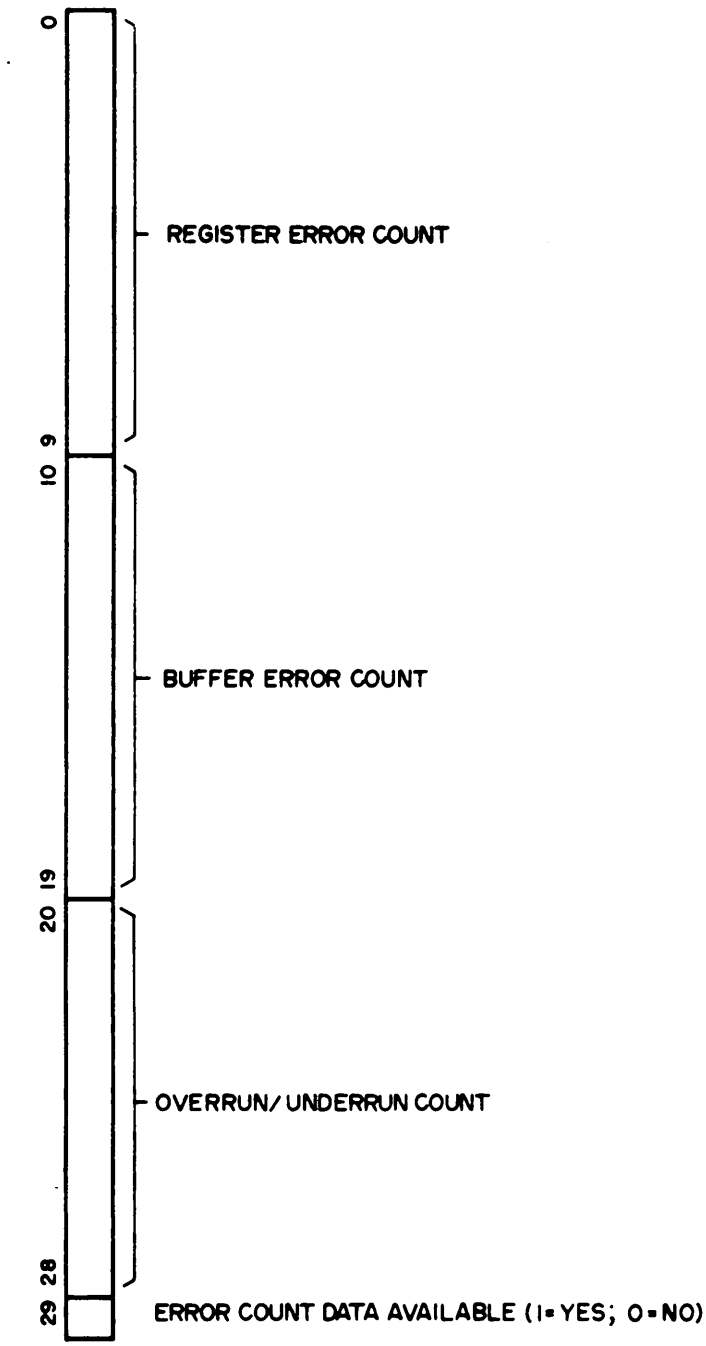
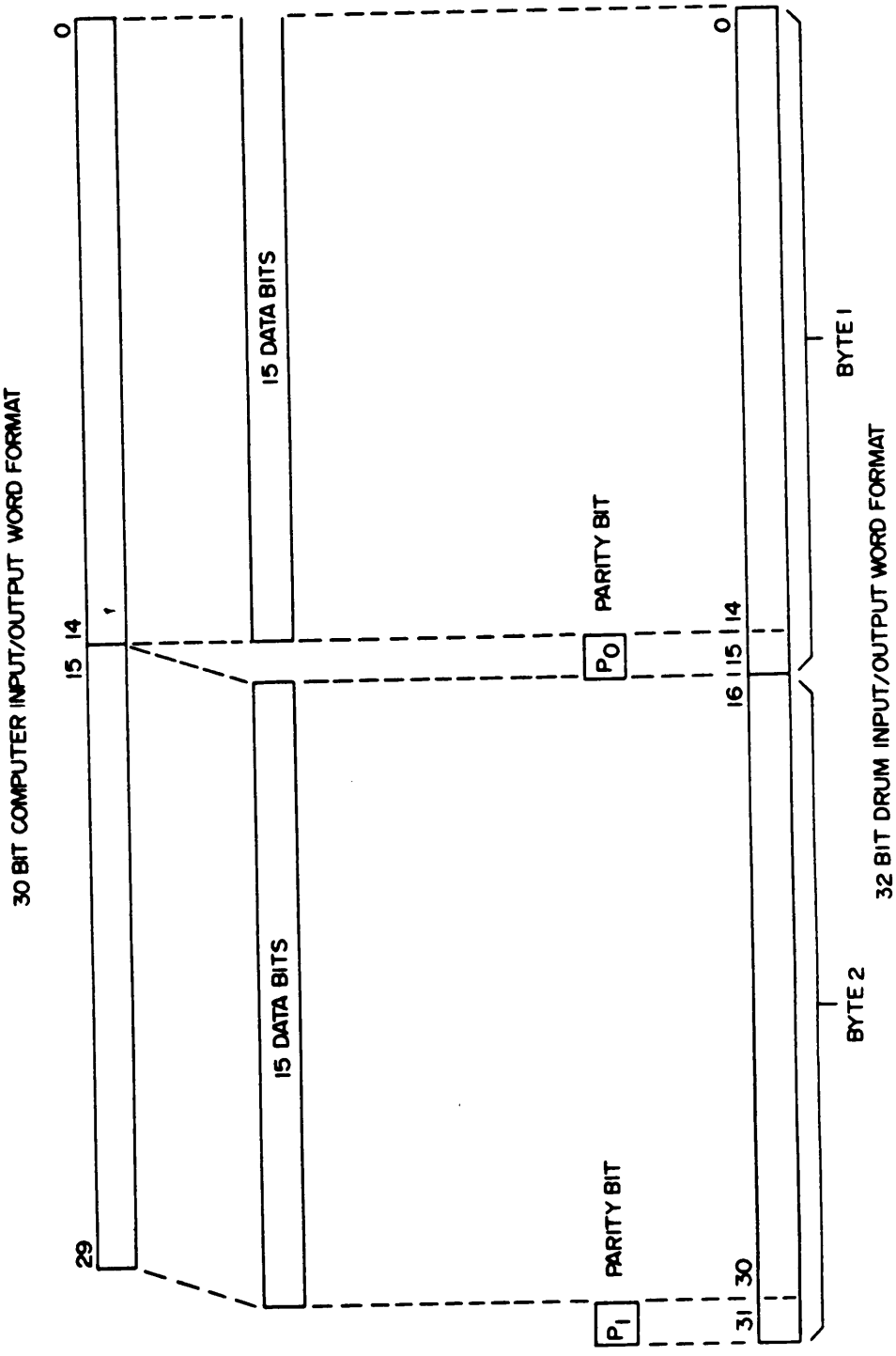


Figure 168. Error Count Interrupt Word Format



3.5.4.4.5 Maintenance Control Panel Subunit

NOTE

Since the Mainentnace Control Panel for the four Logic Units are nearly identical, only one over- all MCP description is given. Refer to 3.5.1.4.9.
The following paragraphs contain a description of functions unique to the Logic Unit 4 Maintenance Control Panel.

3.5.4.4.5.1 Special Test

The MCP of Logic Unit 4 shall provide for a manual special test feature for the DAMS and ADL subunits. This special test shall provide for transmitting three or more words to the subunits in "real time "o (Real time shall be as defined in Appendix I or as modified in the individual subunit paragraphs). Sixty switches (BANK 1 and BANK 2) shall be supplied to provide the first two words. Each switch shall be two position and labeled with a bit number, 29 through 0 for each bank. The switch/indicator data word (MCP Data Register) as described in 3.5.1 .4.9.2 (6) shall be repeated as the third and all subsequent words.

The DAMS special test shall allow for three instruction options under operator control. The instructions are stored in Bank 1 and Bank 2. EFR commands from the DAMS shall initiate the transfer of data from Bank 1 and Bank 2. The data words for each instruction sequence shall be stored in the MC P Data Register. ODR commands from the DAMS shall initiate the transfer of data from the MCP Data Register. The three instruction options are:

(1) Single Option - An instruction shall be performed only once.

(2) Repeat Option - An instruction shall be performed continuously without stopping on error.

(3) Hold Option - An instruction shall be performed continuously until an error occurs, at which time no further instructions shall be executed.

The ADL special test shall allow for the transfer of two data words stored in Bank 1 and Bank 2 to the ADL. The MCP Data Register shall then supply data to the ADL as the third data word. All data transfer shall be in receipt of ODR's from the ADL (via DMS). The ADL frame sync signal (40 Hz Sync) shall cause the special test logic to reset to the Bank 1 data word as the next output word.

3.5.4.4.6 Power Supply Subunit

3.5.4.4.6.1 General

Logic Unit 4 shall contain a power supply subunit as described in 3.3.12.2.

3.5.4.4.6.2 DAMS Power

Power supplied to the DAMS and the ON LINE functions of the MCP shall be independent of that supplied to the remainder of Logic Unit 4. Circuit breakers shall be used in lieu of fuses.

3.5.5 Keysets and Panels

3.5.5.1 General- This section describes the mechanical electrical requirements of the following items:

(1) Universal Keysets

(2) Pilot Keyset

(3) ordnance Pane1 (Keyset)

(4) Armament/Ordance Test Panel

3.5.5.2 Functional Description - The functional descriptions of these items are included in the corresponding logic subunit description.

3.5.5.3 Operating Requirements

3.5.5.3.1 Universal Keysets - All Monfunction, Keyboard and Matrix Select switches shall have one of their two lampa normally lit (green filter). The computer controlled lamps (except for PRO's) shall have an amber filter. AU lamps for PRO's shall be 718 subminiature, flanged base. Lamps for Monofunction Keyboard and Matrix Select switches shall be 815 subminiature, flanged base.

3.5.5.3.1.1 Power Supply - Each Universal Keyset shall contain its own power supply which shall provide the DC voltages an currents required by all components of the Keyset (including bias voltage for the lamp drivers and lamp driver/decoders).

The power supply shall not be damaged by current surges occurring either at power-on (in addition to normally lit lamps, all computer controlled lamps may be lit at power-on) or normal operation.

3.5.5.3.1.2 Lamp Intensity Control - Separate bank intensity controls shall be provided to regulate the voltage applied to the lamps in bank 1 and bank 2 from 2.0 to 5.2 volts. Under no circumstances shall the voltage applied to any lamp be greater than 5.2 volts. Bank 1 shall consist of all Monofunction, Keyboard and Matrix Select switches; bank 2 shall consist of all PRO's and Matrix switches.

3.5.5.3.2 Pilot's Keyset - All switches shall have one lamp normally lit (green filter). The computer controlled lamps shall have amber filters.

3.5.5.3.2.1 Power Supply - The Pilot's Keyset shall contain its own power supply which shall provide the DC voltages an currents required by all components of the Keyset (including bias voltage for the lamp drivers.)

The power supply shall not be damaged by current surges occurring either at power-on (in addition to normally lit lamps, all computer controlled lamps may be lit at power-on) or normal operation.

3.5.5.3.2.2 Lamp Intensity Control - An intensity control shall be provided to regulate the voltage applied to all lamps from 2.0 t05.2 volts. Under no circumstances shall the voltage applied to any lamp be greater than 5.2 volts.

3.5.5.3.3 Ordnance Panel - All switches shall have one lamp normally lit (green filter). The computer controlled status readout lamps shall have amber filters.

3.5.5.3.3.1 Power Supply - The Ordnance Panel shall contain its own power supply which shall provide the DC voltage and currents required by all components of the panel (including bias voltage for the lamp drivers and lamp driver/decoders).

The power supply shall not be damaged by current surges occurring either at power-on (in addition to normally lit lamps, all computer controlled lamps may be lit at power-on) or normal operation.

3.5.5.3.3.2 Lamp Intensity Control - An intensity control shall be provided to regulate the voltage applied to all lamps from 2. O-to 5.2 volts. Under no circumstances shall the voltage applied to any lamp be greater than 5.2 volts.

3.5.5.3.4 Armament/Ordnance Test Panel - The Armament/Ordnance Test Panel shall be wired in accordance with the logic description. (See 3.5.2.4.4.5.)

3.5.5.3.4.1 Power Supply - The Armament/Ordnance Test Panel shall contain its own power supply which shall provide the DC voltages and currents required by all components of the panel. In addition, the Armament/Ordnance Test Panel shall provide 12 volts, regulated, for relays in the Armament/Ordnance systems. This 12 volts shall not be referenced to any ground other than that of the DPS.

3.5.5.4 Mechanical Requirements

3.5.5.4.1 General - Mechanical packaging of the equipment described in is as required to meet an airborne environment. Captive nuts or other equivalent shall be employed. Military specifications MS-25212 and MS-25213 shall be used as design guides.

3.5.5.4.2 Physical Constraints

3.5.5.4.2.1 Overlay Panel - An aluminum overlay panel shall be used to cover the front mounting plate and associated mounting hardware. The Universal Keyset shall have an overlay panel hinged horizontally along its lower edge. The Pilot Keyset overlay panel shall be hinged horizontally at the top. The Ordnance Panel shall be hinged vertically at the left-hand side. The Armament/Ordnance Test Panel shall have no overlay panel. All overlay panel hinges, except that for the Pilot Keyset, shall be spring-loaded. The hinge shall be hidden from view from the front of the panel and spring loaded such that the overlay panel is held normally closed, flush against the mounting plate. Two captive 1/4" turn fasteners, per MIL-F-5591, will lock the overlay panel to the mounting plate in its closed position. A latching arrangement between the overlay and the mounting plate shall be used to lock the overlay panel in the open position. The latch shall limit the total swing of the overlay panel to approximately 90° from its fully closed to its fully open position. The overlay panel shall contain no mounting hardware other than the aforementioned hinge, latch assembly, and captive fasteners. All rivets shall be countersunk and filled and the external appearance of this panel shall be defect-free and flush, after painting, with the exception of the two 1/4" turn fasteners.

3.5.5.4.2.1.1 Finish - The Overlay Panel shall be prepared for painting as per FED-STD-595. Primer required shall conform to MIL-P-23377, or with other approved primer material. The front face and edges of the overlay panel for the Universal Keyset and Ordnance Panel shall be finished with dark gull gray color No. 36231. The front face and edges of the overlay panel for the Pilot Keyset shall be finished with lusterless black color no. 37038.

3.5.5.4.2.2 Front Mounting Plate - All switch and/or indicator housings shall be positively secured to the mounting plate. The switch/indicator light capsules or projection-type readouts containing the lamps and lens assemblies shall be removable from, and installable into, their respective housing from the front of the mounting plate without the use of any tools. A dimmer control on the mounting plate shall be used to control lamp intensity from the front of the overlay panel.

The mounting plate with all its wired associated switches, indicators, connectors and power supply shall be hard mounted. It shall be physically separable from the structural framework *of* the Keysets and attached thereto with countersunk flat screws.

3.5.5.4.2.2.1 Finish - The mounting plate shall be prepared for painting as per FE D-STD-595. Primer required shall conform to MIL-P-23377, or with other approved primer

material. The entire front mounting plate shall be finished with dark gull gray except that lusterless black color No. 37038 shall be used for the Pilot Keyset.

3.5.54.2.3 Fasteners - Provisions for mounting to the airframe shall be as specified by standard MS-25212. Fasteners shall be in accordance with Specification MIL-F-25173. For control panels larger than 6 inches, additional fastener studs shall be located so that no more than 4.875 inches of panel exists between stud centers. On any one panel, the fastener studs shall be spaced at approximately equal intervals in the length direction. Installation provisions shall be in accordance with Standard MS-25213.

3.5.5.4.2.4 Switch Mounting - All switches and/or indicators shall be mounted with respect to the overlay panel accordingly the following definitions. No barrier mounting type switches shall be used. Switches of the Jay-EI series 1064GE-1 type (or equivalent) shall be positioned and hard mounted to the mounting plate so that the viewing screen protrudes through the overlay panel. Hole clearances in the overlay panel between the edges of the overlay and edges of the protruding light capsules shall be approximately 0.060 inch. Switches and/or indicators of the Industrial Electronic Engineering Model 16417, 16418, 16416 and 16422 projection type readouts (or equivalent) shall be positioned and hard mounted to the mounting plate. Individual openings in the overlay panel, one for each 16418 (or equivalent) type shall be provided for these pushbutton type readouts. The dimensions of these openings in the overlay panel shall be such that the translucent viewing screen protrudes through the overlay panel to facilitate switch depression. Assemblies employing 16422 (or equivalent) type readouts shall be equipped with a continuous viewing screen of translucent plastic embedded and cemented into the back of the overlay panel.

3.5.5.4.2.5 Rear Panel - Keyset and power supply in/out connectors shall be secured to the inside surface of the rear panel. This panel, with all its associated power supplies and connectors in place and hard mounted and wired, shall be physically separable from the structural framework of the Keysets and attached thereto with screws. The length of the interconnecting cables between the switches and indicators attached to the front mounting plate and these power connectors shall be sufficient to permit rotating this rear panel about its diagonal to facilitate passing it through the structural framework of the Keysets. Power supplies shall be mounted to the outside of the rear panel.

3.5.5.4.2.5.1 Finish - The outside surface and edges shall be finished in the same manner as the front and overlay panels.

3.5.5.4.2.6 Structural Framework - The structural framework of the Keysets shall be such as to provide access from front and rear only.

3.5.5.4.2.6.1 Finish - The outside surfaces of the Keysets shall be finished in the same manner as the front and overlay panels.

4. QUALITY ASSURANCE PROVISIONS

4.1 Responsibility for Inspection - Unless otherwise specified in the contract or purchase order, the supplier is responsiblee for the performance of all inspection requirements as specified herein. Except as otherwise specified, the supplier may utilize his own facilities or any commercial laboratory acceptable to the Government. The Government reserves the right to perform "any of the inspections set forth in the specification where such inspections are deemed necessary to assure supplies and services conform to prescribed requirements.

4.1.1 Classification of Tests - Items covered by this specification shall be subjected to the following determine compliance with all applicable requirements. (These tests are to be performed only when specifically required in the Contract Schedule.)

(1) Preproduction (First Article) Tests

(2) Initial Production Tests

(3) Acceptance Tests

4.2 Preproduction (First Article) Tests - Preproduction tests shall be made on an equipment representative of the production equipment to be supplied under the contract. Preproduction tests shall be accomplished under the approved test procedure of 4.6. The Government inspector and the procuring activity shall be advised when tests are to be conducted so that a representative may be designated to witness or supervise the tests when so desired. Contractors not having adequate facilities to conduct all required tests shall obtain the services of a commercial testing laboratory acceptable to the procuring activity.

4.2.1 Preproduction (First Article) Test Data - The contractor shall submit all data collected in conducting these tests to the procuring activity for review and approval.

4.2.2 Scope of Tests - Preproduction tests shall include all tests deemed necessary by the procuring activity to determine that the equipment meets all the requirements of this specification and the contract, and shall include:

(1) Environmental Tests in accordance with MIL-T-5422 as modified by the requirements of 3.3.10. Only representative components need be tested for salt spray.

(2) Interference Tests in accordance with 4.2.2.2.

(3) Power Input Tests

4.2.2.1 Power Input Tests - An equipment shall be tested to determine that the input power (current, voltage, frequent y, etc.) over which it will satisfactorily operate will equal or exceed that specified in 3.3.12.

4.2.2.2 Interference Tests - Tests shall be conducted in accordance with WR-101, Part I with the following exceptions:

(1) Conducted Interference on Power Lines

(a) Broadband Interference

Reference Figure 3, Appendix D of WR-101, Part I.

1. A straight line from 30 Hz to 20 KHz at a constant level of 154 db greater than one microamp/MHz.

2. A straight line from 20 KHz and 154 db greater than one microamp/MHz to 50 KHz and 137 db greater than one microamp/MHz.

3. The limit from 50 KHz to 25 MHz remains the same as shown in Figure 3.

(b) Narrowband Interference

Reference Figure 2, Appendix D of WR-101, Part I.

1. A straight line from 30 Hz to 1 KHz at a constant level of 130 db greater than one microamp.

2. A straight line from 1 KHz and 130 db greater than one microamp to 50 KHz and 83 db greater than one microamp.

3. The limit from 50 KHz to 25 MHz remains as shown in Figure 2.

(2) Radiated Interference

(a) Broadband Interference

Reference Figure 5, Appendix D or WR-101, Part I.

1. Increase the limit by 20 db greater than one microvolt/MHz from 15 KHz to 150 KHz.

Reference Figure 16 of MIL-I-6181D.

2. Increase the limit by 20 db greater than one microvolt/MHz from 150 KHz to 25 MHz.

3. The limit remains the same as shown in Figure 16 from 25 MHz to 70 MHz.

4. Increase the limit by 15 db greater than one microvolt/MHz from 70 MHz to 150 MHz.

5. The limit from 150 MHz remains the same as shown in Figure 16.

(b) Narrow Band

Reference Figure 5, Appendix D of WR-101, Part I and Figure 14 of MIL-I-6181D.

1. The limit from 15 KHz to 3 MHz shall be increased by 20 db greater than one microvolt.

2. The limit from 3 MHz to 25 MHz shall be increased from 20 db at 3 MHz to 30 db greater than one microvolt at 25 MHz.

3. The limit from 25 MHz to 300 MHz shall be increased by 25 db greater than one microvolt.

4. The limit from 300 MHz to 1000 MHz remains as shown in Figure 14 of MIL-I-6181D.

(3) Conducted Interference on Interface Lines

Reference 4.2.1.1 of WR-101 Part I.

Conducted emissions on interface lines other than primary power shall not be measured.

(4) Short Duration Interference

Reference 3.2.2 of MIL-D-6181D

All DPS equipment switches shall be considered as manual switches which are not operated more than twice per normal operational period. Short duration impulse noise generated by operation of the switches shall be measured in all emission tests but no limits shall apply.

4.2.3 Preproduction (First Article) Approval - Approval of the pre - production sample shall be by the procuring activity upon satisfactory completion of all tests. No production equipments shall be delivered prior to the approval of the preproduction sample. Pre- fabrication of production equipment prior to the approval of the preproduction sample is at the con- tractor's own risk. The approved preproduction sample shall be retained by the contractor for his use in the fabrication and testing of equipment to be submitted for acceptance. The preproduction sample shall not be considered as one of the equipments under contract.

4.2.4 Production Equipments - Equipments supplied under the contract shall in all respects, including design, construction, wormanship, performance and quality, be equiv. alent to the approved preproduction sample. Each equipment shall be capable of successfully paining the same tests as imposed on the preproduction sample. Evidence of non-compliance with the above shall constitute cause for rejection and for equipment already accepted by the Government; it shall be the obligation of the contractor to make necessary corrections as approved by the procuring activity.

4.3 Initial Production Tests - One of the first ten production equip- ments shall be selected and sent at the contractor's expense to a designated Government laboratory for tests. This equipment shall be selected by the procuring activity after the equipment has success- fully passed all individual tests. The preproduct.ion sample shall not be selected for this test.

4 . 3 . 1 Scope of Tests - This equipment may be subjected to any and all tests the procuring activity deems necessary to assure that the production equipment is equivalent to the previously approved preproduction sample in design, construction, workmanship, performance and quality and that it meets all applicable requirements.

4.3.2 Accessory Material - In addition to the complete equipment sub- mitted for Initial Production Tests, the contractor shall also submit such accessory material and data as necessary to test the equipment;

4.3.3 Initial Production Sample Approval - Approval of the Initial Pro- duction Sample shall be by the procuring activity upon satisfactory completion of all tests. Any de- sign, material or performance defect made evident during this test shall be corrected by the contractor to the satisfaction of the procuring activity. Failure of the Initial Production Sample to pass any of the tests shall be cause for deliveries of equipment under the contract to cease until proper corrective action is approved and accomplished. Corrective action shall also be accomplished on equipment previously accepted when requested by the procuring activity.

4.3.4 Reconditioning of Initial Production Test Sample - On completion of the initial production test, the equipment shall be reworked by the contractor by replacing all worn or damaged items. After reworking, the contractor shall resubmit the equipment for acceptance.

4.4 Acceptance Tests - The contractor shall be responsible for accomplishing the acceptance tests. All inspection and testing shall be under the supervision of the government inspector. Contractors not having testing facilities satisfactory to the procuring activity shall engage the service of a commercial testing laboratory acceptable to the procuring activity. The contractor shall furnish test reports showing qualitative and quantitative results for all acceptance tests. Such reports shall be signed by an authorized representative of the contractor or laboratory, as applicable. Acceptance or approval of material during the course of manufacture shall not be construed as a guarantee of the acceptance of the finished product. Acceptance tests shall consist of the following:

(1) Individual Tests

(2) Maintainability Tests

(3) Reliability Assurance Tests

(4) Special Tests

4.4.1 Individual Tests - Each equipment submitted for acceptance shall be subjected to the individual tests.These tests shall be determine compliance with the requirements of material, workmanship, operational adequacy and reliability y. As a minimum each equipment accepted shall have passed the following tests:

(1) Examination of Product

(2) Operational Test

4.4.1.1 Examination of Product - Each equipment shall be examined carefully to determine that the material and workmanship requirements have been met.

4.4.1.2 Operational Test - Each equipment shall be operated long enough to permit the equipment temperature to stabilize and to check sufficient characteristics and record adequate data to assure satisfactory y equipment operation.

4.4.2 Maintainability Tests - The following procedure shall be used to demonstrate that the time-to-repair for this equipment is as specified.

4.4.2.1 Test Conditions - One equipment shall be used for this test. The contractor shall select any one of the equipments that is available. All dust covers shall be in place on the equipment prior to the initiation of this test. Two technicians shall be used to conduct these tests but only one shall be used per repair action as defined in 4.4.2.2. Before beginning the test, the equipment shall be checked to determine that it is operating normally. Test equipment, tools, spare parts, diagnostic programs, and documentation shall be available for the test. The test facility shall be provided by the procuring activity. The diagnostic program shall be the primary means of fault detection and isolation.

4.4.2.2 Repair Actions - A repair action shall be as follows:

(1) Final Fault Isolation after completion of the Diagnostic Program.

(2) Repair

(3) Equipment Checkout

4.4.2.3 Simulated Failures - A total of 100 failures one at a time shall be introduced into the DPS. The failures shall be randomly introduced into the DPS The failures shall be randomly introduced throughout the equipment. The points of failures shall be approved by the procuring activity prior to initiation of the test.

4.4.2.3.1 Inducing Failures - Single failures shall be induced into the equipment by the government representative by substituting modules that are known to be defective. Simulated failures using other means may be used but they shall be kept to a minimum. Each demonstrated failure will consist of a single solid malfunction.

4.4.2.4 Repair Time Measurements - The time required for the technician to perform each repair action, including the use of technical manuals and support equipment, shall be measured starting with final fault isolation after completion of the Diagnostic Program and ending at the time the equipment is restored to normal operation and proper operation is verified. Any delay, such as waiting for parts, obtaining test equipment, or administrative delays shall be excluded.

4.4.2.5 Test Repoting - The contractor shall submit to the procuring activity a report of the demonstration. This is report shall include all pertinent data and observations, major problem areas and recommendations for corrective action as required.

4.4.3 Reliability Assurance Tests - Reliability Assurance Tests shall be conducted in accordance with MIL-STD-781 for both the Qualification phase and the Production Acceptance phase. The Qualification phase shall include a Life Test of the Keyset and Panel mono-function switches. Classification of failures shall be in accordance with MIL-STD-781 and AR-34.

4.4.3.1 General Requirements

4.4.3.1.1 Test Details - Test level E of MIL-STD-781 shall be used except that the lower temperature limit shall be -25°C ±2°C and the maximum vibration for Logic Units 1, 2 and 3 shall be a maximum of ±2g ±l0%. The Logic Unit 4 vibration shall be at any nonresonant frequency between 20 and 60 Hz and at a level in accordance with MIL-E-5400 Curve I between 20 and 32 Hz or at ±2g between 32 and 60 Hz. No vibration shall be applied to the keysets and panels and measurements on these units shall be taken at room temperature only. Test chambers for keysets and panels shall be capable of maintaining the ambient and forced air temperatures at the specified test level temperatures ±3°C during the test. The rate of the temperature change of the thermal medium in both the heating and cooling cycles shall average not less than 2°C/minute. The length of the heat portion of the cycle, performance characteristics to be measured, special failure criteria etc. , shall be part of the test procedures to be submitted by the contractor and approved by the Procuring Activity prior to commencement of testing,

4.4.3.1.2 Preventive Maintenance - No preventive maintenance shall be allowed during any phase of the reliability testing except when approved in advance by the procuring activity. An unapproved preventive maintenance action shall be considered prima facie evidence of a failure.

4.4.3.2 Qualification Phase

4.4.3.2.1 Reliability Demonstration

4.4.3.2.1.1 Logic Units 1, 2, 3, and 4 - A group of four Logic Units comprised of one Logic Unit 1, one Logic Unit 2, one Logic Unit 3 and one Logic Unit 4 shall be tested for a fixed length test operating time of 1436 hours each. The Accept criterion shall be 12 or fewer failures for the group: the Reject criterion shall be 13 or more failures.

4.4.3.2.1.2 Keyset and Panel Components - The following Keyset and Panel components shall undergo demonstration testing for a cumulative test time of 3.9 times their specified MTBF's:

(1) 6 Volt Regulated Power Supply - Specified MTBF of 1000 hours.

(2) Blower - Specified MTBF of 2000 hours.

(3) Lamp Driver - Specified MTBF of 5000 hours.

(4) Binary Decoder - Specified MTBF of 4000 hours.

(5) Projection Readout - Specified MTBF of 3000 hours.

The Accept criterion for the 6 Volt Regulated Power Supply and Blower shall be six or fewer failures: the Reject criterion shall be seven or more failures. Accept-Reject criteria shall not apply to the lamp drivers, binary decoders and projection readouts. The tests of these components shall be performed for the purpose of obtaining reliability and quality information only.

4.4.3.2.3 Life Test of Switches - The Keyset and Panel monofunction Series 90E and Series 500 switches or their equivalents shall be subjected to Life Tests at normal room ambient environmental condition with simulated normal equipment switch loads. The life requirements are 25,000 cycles electrical life and 50,000 cycles mechanical life. The switches shall be tested for 1000 hours consisting of 20 intervals as follows:

(1) Switching operation -8 hours

(2) No operation -8 hours

(3) Switching Operation -24 hours

(4) No Operation -40 hours

4.4.3.2.3 Logic Unit 4 Test Analyze and Fix (TAAF) Test - A group of two Logic Units 4 shall be tested under conditions described in 4.4.3.1.1 for a fixed length operating time of 2500 hours minimum. An observed MTBF (obtained by dividing the total operating time by the number of chargeable failures) of 250 hours minimum shall be demonstrated.

4.4.3.3 Production Phase

4.4.3.3.1 Reliability Demonstration Test

4.4.3 .3.1.1 Logic Units 1, 2, 3, and 4 - Four Logic Units (1, 2, 3, and 4) from one system shall be subjected to a Reliability Demonstration Test for a period of operating time equal to the specified MTBF. The Accept criterion shall be seven or fewer relevant failures; the Reject criterion shall be eight or more relevant failures.

4.4.3.3.2 Reliability Production Test

4.4.3.3.2.1 Reliability Production Acceptance (Sampling) Phase Tests - The equipment, throughout production, shall be tested as outlined in MIL-STD-781 (as modified herein) under the section entitled "Production Acceptance (Sampling) Phase of Production Reliability Tests". Test levels shall be as specified in 4.4.3.1.1.

4.4.3.3.2.2 All Equipment Test - Each equipment produced except those submitted for the Reliability Qualification Test, shall be tested for a minimum of 100 hours. Prior to the 100 hour test on each equipment, a burn-in period may be used at the option of the contractor. If the burn-in period is to be used the details thereof must be included in the approved test procedures. The last 50 hours of this All Equipment Test shall be accomplished failure free.

To determine whether the MTBF is being met at any time during the contract the operating test hours and the failures therein (not counting burn-in failures or burn-in operating time) shall be totaled and the results compared with the reject line of Test Plan II of MIL-STD-781. (Extend the line as necessary to accommodate the data.) These totals shall accumulate so that at any one time the experience from the beginning of the contract is included. At the conclusion of each month the test results shall be sent to the procuring activity and to the Naval Air Systems Command, Attention: Avionics Division. At any time that the current totals of test hours and test failures plotted on Test Plan II curves show a reject situation, the procuring activity shall be notified. The procuring activity reserves the right to stop the acceptance of equipment at any time that a reject situation exists pending a review of the contractor's efforts to improve the equipment, the equipment parts, the equipment workmanship, etc. , so that the entire compilation will show other than a reject decision.

4.4.4 Reliability Engineering Analysis - Forty working days prior to the initiation of the releiability test, the contractor shall submit for approval, to the procuring agency, an analytical reliability analysis of the equipments. The analysis shall show as a minimum the electrical and thermal stress on each part, failure rates of parts, safety margins for parts, and environmental effects on parts. Supporting failure rate data and curves shall be submitted with the analysis.

4.4.5 Equipment Failure - Should a failure ocuur during either the Reliability Assurance or special Tests, the following action shall be taken.

(1) Determine the cause of failure

(2) Determine if the failure is an isolated case or design defect.

(3) Submit to the procuring activity for approval proposed corrective action intended to reduce the possibility y of the same failure(s) occurring in future tests.

(4) Where practical, include a test in the individual tests to check all equipment for this requirement until reasonable assurance is obtained that the defect has been satisfactorily corrected.

4.4.5.1 Failure Analysis - The contractor shall conduct a planned program of failure analysis throughout the life of the contract. All failures related to the Reliability test program or to deliverable equipment shall be analyzed to the level required to assure corrective action and to prevent reoccurrence. Failure analysis records shall be included in the monthly reliability report and contain the following information as a minimum requirement:

(1) Report Number

(2) Reporting Activity and Individual

(3) Equipment Identification

(4) Major Assembly Identification

(5) Subassembly Identification

(6) Component or Part Identification

(7) Date of Failure

(8) Time on Failed Part/Item

(9) Name of Test/Operation

(lo) Environment

(11) Description *of* Trouble

(12) Failure Cause/Analysis

(13) Disposition (Detail)

(14) Name of Failure Analysis Authority

(15) Corrective Action Required

(16) Failure Effect Analysis

4.5 Special Tests - Special tests shall be conducted on a quantity of equipments for the purpose of checking the effect of any design or material change on the performance of the equipment and to assure adequate quality control. The equipment selected for special tests may be selected from equipments previously subjected to the sampling or reliability assurance tests.

4.5.1 Special Test Schedule - Selection of equipments for special tests shall be made as follows:

(1) On an early equipment after an engineering or material change.

(2) Whenever failure reports or other information indicate that additional tests are required. (This will be determined by the procuring activity.)

4.5.2 Scope of Tests - Special tests shall consist of such tests as approved by the procuring activity. Test procedures previously approved for the preproduction tests shall be used where applicable. When not applicable, the contractor shall-prepare a test procedure and submit it to the procuring activity for approval prior to conducting the tests.

4.6 Test Procedures - The procedures used for conducting pre-production tests, acceptance tests and life tests shall be prepared by the contractor and submitted to the procuring activity for review and approval. The right is reserved by the procuring activity or the government inspector to modify the tests or require any additional tests deemed necessary to determine compliance with the requirements of this specification or the contract. Specification MI L-T- 18303 shall be used as a guide for preparation of test procedures. When approved test procedures are available from previous contracts such procedures will be utilized. However, the right is reserved by the procuring activity to require modification of such procedures, including additional tests, when deemed necessary. Test specifications may be supplied in lieu of test procedures with the concurrence and approval of the procuring activity.

4.7 Reconditioning of Tested Equiment - Equipment which has been subjected to preproduction or reliability assurance tests shall be reconditioned by the contractor by replacing all worn or damaged items affecting performance. After reworking the contractor shall resubmit the equipment for the operational portion of the individual tests.

4.8 Presubmission Testing - No item, part or complete equipment shall be submitted by the contractor until it has been previously tested and inspected by the contractor and found to comply, to the best of his knowledge and belief, with all applicable requirements.

4.9 Rejection and Retest - Equipment which has been rejected during acceptance test may be reworked or have parts replaced to correct the defects and resubmitted for acceptance. Before resubmitting, full particulars concerning previous rejection and the action taken to correct the defects found in the original shall be furnished the government inspector.

5. PREPARATION FOR DE LIVERY

5.1 General - All major units and parts of the equipment shall be preserved, packaged, packed and marked level of shipment specified in the contract or order in accordance with specifications MIL-E-17555 and MIL-STD-794. In the event the equipment is not covered" in specification MIL-E-17555, the method of preservation for Level A shall be determined in accordance with the selection chart in Appendix D of MIL-STD-794.

6. NOTES

6.1 Intended Use - To be used in the P-3C weapon system

6.2 Ordering Data - Purchasers should exercise any desired options offered herein, and procurement documents should specify the following:

(1) Title, number, and date of this specification.

(2) Selection of applicable levels of packaging and packing (see 5. 1).

6.3 Precedence of Documents - When the requirements of the contract, this specification, or applicable subsidiary specifications are in conflict, the following precedence shall apply:

(1) Contract - The contract shall have precedence over any specification.

(2) This Spedification - This specification shall have precedence over all applicable subsidiary specifications. Any deviation from this specification, or from subsidiary specifications where applicable shall be specifically approved in writing by the procuring activity.

(3) Referenced Specifications - Any referenced specification shall have precedence over all applicable subsidiary specifications referenced therein All referenced specifications shall apply to the extent specified.

6.4 Performance Objectives - Minimum size and weight, simplicity of operation, ease of maintenance. and an improvement in the performance and reliability of the specific functions beyond the requirements of this specification are objectives which shall be considered in the production of this equipment. Where it appears a substantial reduction in size and weight or improvement in simplicty of design, performance, ease of maintenance or reliability will result from the use of materials, parts and processes other than those specified in Specification MIL-E-5400, it is desired their use be investigated. When investigation shows advantages can be realized, a request for approval shall be submitted to the procuring activity for consideration. Each request shall be accompanied by complete supporting information.

6.5 Type Designations - The type designation maybe modified by the procuring activity upon application by the contractor for assignment of nomenclature in accordance with 3.3.8.

6.6 Revisions - Symbols are not used in this revision to identify changes with respect to the previous issue due to the extensiveness of the changes.

6.7 Associated Equipment

RD-319A/AYA-8	Magnetic Tape Transport
CP-901/ASQ-114	Computer, Avionic
AN/ALT-78	ECM
AN/APN-187	Doppler Velocity Altimeter Radar Set
AN/ARR-72(V)	Sonobuoy Receivers
AN/ASA-64	Submarine Anomaly Detection Group
AN/ASA-66	Pilot Display
AN/ASA-69	Radar Scan Converter
MX/ASA-69	Radar Interface Unit
IP-917/ASA-70	Multipurpose Data Display
IP-918/ASA-70	Sensor Data Display
IP-919/ASA-70	Auxiliary Readout Display
AN/ASN-84	Inertial Navigation Systems
AN/AXR-13	Television Camera Set

6.8 This specification is under the cognizance of AIR-533035.

APPENDIX I

COMPUTER INPUT/OUTPUT SPECIFICATION

1. SCOPE

1.1 This appendix details the input/output, transfer and timing sequences for Computer CP-901/ASQ-114.

2. REQUIREMENTS

2.1 Functional

2.1.1 General - Communication with the Computer is carried on in a 30-bit parallel mode over the input/output channels. The Computer accommodates four 1/0 channel groups, each channel group containing four pairs of input/output channels, a time shared output register, input selection circuits, local 1/0 control, and priority circuits. These channels can be designated as either normal or inter-computer channels. It should be noted that all references in this specification to input or output are made from the standpoint of the computer; that is, "input" is input to the computer and "output" is output from the computer.

2.1.2 Control Communication - The Computer is designed to use a d-c level input /output system. Signals are d-c levels which may be changed upon interchange of control information. Output data signals from an input/output unit may exist for microseconds or days, depending on the nature of the particular task. The data lines will not change until another output is made from one of the four output channels contained in a particular input/output group.

2.1.3 Data and Control signals - Each channel shall have associated with it 30 data lines and 4 control lines as listed in Table 1-1. All lines are twisted pair.

TABLE 1-1. CONTROL SIGNALS IN NORMAL PERIPHERAL EQUIPMENT CHANNELS

	Control Signal	Sending Equipment
Input Channel Control Lines	1. Interrupt Enable	Computer
	2. Interrupt	Peripheral
	3. Input Data Request	Peripheral
	4. Input Acknowledge	Computer
Output Channel Control Lines	1. External Function Request	Peripheral
	2. External Function	Computer
	3. Output Data Request	Peripheral
	4. Output Acknowledge	Computer

Figure 1-1 shows the Avionics Computer receiving input from Equipment I and sending output to Equipment II. Figure 1-2 shows a computer to computer interface. Note the direction of information flow. The Data Request signals are always sent from the peripheral equipment to the computer. The Acknowledge signals are always sent from the computer to the peripheral equipment.

2.1.4 Sequence of Events

2.1.4.1 Computer/Peripheral Equipment Communications

2.1.4.1.1 Input - The sequence of events for the two methods in which inputs can be made to the computer are as follows:

2.1.4.1.1.1 Interrupt Input - A peripheral equipment shall be able to input one 30 bit word to the computer by following the control line sequence below, as illustrated in Figure 1-3.

(1) Computer sets the Interrupt Enable when it is ready to accept an External Interrupt.

(2) Peripheral equipment detects the Interrupt Enable.

(3) Peripheral equipment places the Interrupt word on the 30 data lines.

(4) Peripheral equipment sets the Interrupt line to indicate that the External Interrupt word is on the data lines.

(5) Computer detects the Interrupt signal, and at its convenience, accepts the Interrupt word.

(6) Computer drops the Interrupt Enable.

(7) Peripheral equipment detects the drop of the Interrupt Enable and clears the Interrupt line and data lines.

The Input Acknowledge of an interrupt will be initiated at the same time that the Interrupt Enable is cleared. The simultaneous occurrence of these conditions should be used by peripheral equipment to differentiate between an Interrupt Acknowledge and a Data Acknowledge. If a peripheral equipment is not designed to sense an Interrupt Enable, then the sequence would include only steps (3), (4), (5), and the setting *of* the Input Acknowledge. An interrupt transfer would occur by Method II as shown in Figure 1-3.

2.1.4.1.1.2 Data Inputs - The computer shall be able to accept 30 bit data words from peripheral equipments by following the control line sequence below, as illustrated in Figure 1-4.

(1) Computer initiates input buffer for given channel.

(2) Peripheral equipment places data on the 30 data lines.

(3) Peripheral equipment sets the Input Data Request line to indicate that it has data ready for transmission.

(4) Computer detects the Input Data Request.

(5) Computer samples the 30 data lines, at its convenience.

(6) Computer sets the Input Acknowledge line, indicating that it has sampled the data.

(7) Peripheral equipment senses the Input Acknowlege line.

(8) Peripheral equipment drops the data lines and the Input Data Request line.

Steps (2) through (8) of this sequence are repeated for every data word until the number of words specified in the input buffer have been transferred.

2.1.4.1.2 Output - The sequence of events for the two methods in which outputs can be made from the computer are as follows:

2.1.4.1.2.1 Data Outputs - The computer shall be able to output 30 bit data words to a peripheral equipment by following the control line sequence below, as illustrated in Figure 1-5.

(1) Computer initiates output buffer for given channel.

(2) Peripheral equipment sets the Output Data Request line indicating that it is in a condition to accept data.

(3) Computer detects Output Data Request.

(4) Computer, at its convenience, places data on the 30 data lines.

(5) Computer sets the Output Acknowledge line, indicating that the data is ready for sampling.

(6) Peripheral equipment detects the Output Acknowledge.

(7) Peripheral equipment may drop ‘the Output Data Request any time after detecting the Output Acknowledge.

(8) Peripheral equipment samples the 30 data lines.

(9) Computer drops the Output Acknowledge.

Steps (2) through (9) of this sequence are repeated for every data word until the number of words specified in the output buffer have been transferred.

2.1.4.1.2.2 External Functions - The computer shall be able to output one 30 bit External Function word to a peripheral equipment by following the control line sequence below, as illustrated in Figure 1-5.

(1) Peripheral equipment sets the External Function Request line when it is ready to accept an External Function word.

(2) Computer defects the External Function Request

(3) Computer places the External Function word on the data lines (if its External Function buffer is active).

(4) Computer sets the External Function line to indicate that the External Function word is ready for sampling.

(5) The External Function should be used to clear the External Function Request at the peripheral equipment.

(6) Peripheral equipment samples the External function word.

(7) Computer drops the External Function line.

This sequencers repeated when the peripheral equipment is ready to accept another External Function word.

If an External Function with force is to be sent, then steps (3), (4), (6), and (7) would form the sequence as shown in Figure 1-6. Further External Function line. Function with force can be found in 2.2.2.2.

2.1.4.2 Inter-Computer Communications - In the Computer any or all of the input/output channels shall be cabling of being used for inter-computer communication. The control signals governing inter-computer communication are shown in Table 1-2.

TABLE 1-2. CONTROL SIGNALS IN INTER-COMPUTER CHANNELS

output	Input
External Function Request	Interrupt Enable
External Function	Interrupt
Ready	Input Data Request
Resume	Input Acknowledge

Note that the control signals in the input cable are the same for inter- computer communications as for communication with peripheral equipment. In the output control line cable, Ready and Resume signals are used to control the inter-computer transfer of data.

Figure 1-2 illustrates the interface between two Computers. Computer A is transmitting to Computer B.

2.1.4.2.1 Command Word - Computer A shall be able to transfer one 30 bit command to Computer B by following the control line sequence below.

(1) Computer B sets the Interrupt Enable when it is ready to accept a command word from Computer A.

(2) Computer A recognizes the Interrupt Enable as an External Function Request and places the External Function word on the 30 data lines.

(3) Computer A sets the External Finction to indicate that the External Function word is on the data lines.

(4) Computer B recognizes the External Function as an Interrupt and accepts the command word.

(5) Computer B clears the Interrupt Enable line and sets the Input Acknowledge line.

(6) Computer A recognizes the Input Acknowledge as a Resume and clears the External Function line.

In the event that Computer A sets the External Function line while the Interrupt Enable line is cleared (this is possible when an External Function with Force instruction is used), all communications on the associated group of output channels in A will be suspended until Computer B acknowledges receipt of the External Interrupt or until an inter-computer time out interrupt in A permits A to resolve the problem. If either Computer A or B is not designed for External Function Requests or Interrupt Enables, then all External Functions shall be transferred by force, and interrupts shall be transferred as shown by Method II of Figure 1-3.

2.1.4.2.2 Data Word - Computer A shall be able to transfer 30 bit words to computer B by following the control line sequence below.

(1) Computer B initiates an input buffer and Computer A initiates an output buffer for the required channel.

(2) Computer A places data in the data lines.

(3) Computer A sets the Ready line to indicate that the data is on the line.

(4) Computer B recognizes the Ready signal as an Input Data Request signal and, at its convenience, accepts the data word.

(5) Computer B sets the Input Acknowledge.

(6) Computer A recognizes the Input Acknowledge as a Resume signal and clears the Ready (Input Data Request) line.

(7) Repeat steps (2) through (6) for each word specified in the buffer.

2.1.5 I/O Priority - The computer shall perform an 1/0 priority scan concurrent with the performance of a program instruction sequence. The succession in which events are processed shall be in accordance with the function priority specified in the Priority Table, Table 1-3. For all events which are channel dependent, channel priority shall be considered first, function priority second.

Channel priorities shall be assigned as follows:

(1) The four input/output channel groups, in order of descending priority are: 1/0 Group 3, 1/0 Group 2, 1/0 Group 1, and I/O Group 0.

(2) The four input/output channels associated with each channel group, in order of descending priority are: Channel 3, Channel 2, Channel 1, and Channel 0. The Computer 1/0 Channel numbers, listed in reference with its respective I/O Group, and Channel within the I/O Group are specified in Table 1-4.

2.2 Input/Output Timing

2.2.1 Input Timing Considerations

2.2.1.1 Data Inputs to Computer from Peripheral Equipment - The input Data Request signal indicates to the computer that data has been placed on the 30 datelines. The Input Data Request must be maintained on the lines until an Input Acknowledge is received. As shown in Figure 1-3, there is a 7.75(-0.47) microsecond minimum delay between the setting of the Input Data Request and its answering Input Acknowledge. There is no maximum limit on the duration of the Input Data Request since its value for any particular cycle is determined by the interaction with the computer program and the other input/output channels. The data lines must remain stable as long as the Input Data Request is set.

The Input Acknowledge indicates to the peripheral equipment that its 30 datelines have been sampled. The Input Acknowledge signal is set for a fixed time interval. The peripheral equipment must be capable of detecting as an Input Acknowledge a signal which may exist in the stable "1" state for as little as 2.5 (±0.15) microseconds Upon sensing the Input Acknowledge, the Input Data Request may be dropped to the "0" state any time, but it must be dropped at least O. 53 microseconds before another Input Data Request can be initiated. It should be noted that the time relationships are such that the peripheral equipment desiring to send data at a maximum rate could legitimately reset the Input Data Request before the previous Input Acknowledge has been dropped. to the "O" state; however, the Input Acknowledge will always be returned to the "O" state before being reset to the "1" state. This will not affect operation of the input cycle.

2.2.1.2 External Interrupt Inputs to Computer - Two different methods are used to control the transmission of External Interrupts from peripheral equipment to the Computer. Which method is used depends upon the peripheral equipment. If 'the peripheral equipment is capable of sensing an Interrupt Enable signal, then the control signals and timing are as shown in Method I of Figure 1.3. If the peripheral equipment is not capable of sensing an Interrupt Enable, then the control signals and timing are as shown in Method II of Figure 1.3. When Method I is used, the Interrupt Enable line shall drop at the same time the Input Acknowledge is sent. This informs the peripheral equipment that the computer has accepted the Interrupt word and that the Interrupt signal may be dropped. Regardless of which method is used, a minimum delay of 3.75 (-O. 23) microseconds exist from the start of the setting of the Interrupt Line, to the start of the setting of the Input Acknowledge line. From the completion of the dropping *of* the Interrupt Line, a O. 53 microsecond minimum delay is required before the start of the setting of the Interrupt line for the second time. The data lines must remain stable as long as the Interrupt line is in the set condition.

2.2.2 Output Timing Considerations

2.2.2.1 Data Output and External Functions - Peripheral equipment must first set the Output Request line or External Function Request line indicating that it is in a condition to accept a data or External Function word from the computer. Data lines 'will not necessarily be cleared to the "O" state before being reset to the "1" state. The minimum time interval between the Output or External Function Request signal and the placement of answering data on the lines is 6.75 (-O. 41) microseconds. The maximum time interval depends upon the computer program, the priority of the particular channel, and the data request rates of the other peripheral equipment.

The Output Acknowledge or External Function signal indicates to the peripheral equipment that the requested word is now present on the data lines and that the lines should now be sampled. As shown in Figure 1-5, the Output Acknowledge or External Function signal will be sent a minimum of 0.4 microsecond after the data has been placed on the lines. The peripheral equipment must be capable of recognizing, as an Output Acknowledge or an External Function, a signal which may exist in the stable "1" state for as short a time as 2.2 microseconds. The computer will maintain stable data on the lines for a minimum of 0.5 microsecond after it starts to drop the Output Acknowledge or External Function.

TABLE 1-3. PRIORITY OF EVENTS

Function Priority	Function Title	Action When Processed
All three are first priority	Forced Instruction Request (occurs whenever instructions 13 (k=1,3) or 17 (k=2) occur).	As specified under the instruction definition.
	Program Fault Fast Interrupt (occurs from an illegal function code).	Program jump to address 00000 or 00540 depending upon automatic recovery switch setting.
	Additive Real-time clock Update request (occurs once every cycle of the additive real-time clock).	Increment the contents of address 00160 by one.
2 (Channel dependent)	External Interrupt (occurs when an external device sets the External Interrupt Request line).	Stores the External Interrupt Word at address 00520 plus channel number and sets the External 1/0 interrupt.
3 (Channel dependent)	External Function (occurs when an external device sets the External Function Request line).	Performs an External Function Buffer using the buffer control word at address 00140 plus channel number.
4-5* (Channel dependent)	Output Data Request (occurs when an external device sets the Output Data Request line).	Performs an Output Buffer using the buffer control word at address 00120 plus channel number.
5-4* (Channel dependent)	Input Data Request l Each time either 4 or 5 is detected they shall reverse their priority.	Performs an Input Buffer using the buffer control word at address 00100 plus channel number.
6 (Channel dependent)	Intercomputer time-out I/O Interrupt (occurs when the transmitting computer has held a word in an output register for the time specified without receiving an Acknowledge).	Program jump to Intercomputer Time-Out entrance register at address 00600 plus channel number.
7 (Channel dependent)	External 1/0 interrupt (occurs when an External Interrupt function priority 2, is processed).	Program jump to External Interrupt Entrance register at address 00020 plus channel number.
8 (Channel dependent)	External function monitor 1/0 interrupt (occurs when an External Function buffer with monitor terminates).	Program jump to the External Function Monitor Interrupt entrance register at address 00500 plus channel number.
9 (Channel dependent)	Output data monitor 1/0 interrupt (occurs when an output data buffer with monitor terminates).	Program jump to the Output Monitor Interrupt entrance register at address 00060 plus channel number.

TABLE 1-3. PRIORITY OF EVENTS (Continued)

Function Priority	Function Title	Action When Processed
10 (Channel dependent)	Input data monitor I/O interrupt (occurs when an input data buffer with monitor terminates).	Program jump to the Input Monitor Interrupt e..trance register at address 00040 plus channel number.
11	Program control and arithmetic operation.	Perform the action of reading the instruction or reading (storing) the operand.

TABLE 1-4. COMPUTER I/O CHANNEL NUMBERS

I/O Group Number	Channel Number Within I/O Group	Computer Channel Number
3	3	15
3	2	14
3	1	13
3	0	12
2	3	11
2	2	10
2	1	9
2	0	8
1	3	7
1	2	6
1	1	5
1	0	4
0	3	3
0	2	2
0	1	1
0	0	0

The Output or External Function Request maybe dropped to the "0''state any time after detecting the Output Acknowledge or the External Function. The Output or External Function Request cannot be reset immediately to indicate readiness of the peripheral equipment to accept a second word because the computer will not recognize the second Output or External Function Request unless. a minimum time delay of 0.8 microsecond is allowed between the completion of the dropping of the first Output or External Function Request and the start of the setting of the second Output or External Function Request. The timing would allow any peripheral equipment that wishes to receive data from the computer at a maximum rate, to legitimately set the Output or External Function Request to the "1" state for the second time before the first Output Acknowledge or External Function has dropped to the "0" state. This will not affect operation of the output cycle.

2.2.2.2 External Functions with Force - External Functions with Force are unique in that no Request is sent by the peripheral equipment. The computer places the External Function code on the 30 output data lines, and a minimum of 0.4 microsecond later energizes the External Function Line. The External Function Line will remain in the stable "1" state for an interval which may be as short as 2.05 (±0.15) microseconds. (See Figure 1-6.)

The External Function word will remain on the data line for a minimum of 0.5 microsecond after the External Function signal begins to drop.

The peripheral equipment has no control over the rate at which External Functions with Force are sent. The External Function Line will drop to the "O" state for an

interval which may be as short as 4.0 microseconds. If the peripheral equipments cannot accept External Functions at this rate, restrictions must be made in the programming of External Function instructions to the equipment. It should be noted that, if the peripheral equipments have no provisions for sending an External Function Request signal, all External Functions to existing peripheral equipment must be sent as External Function with Force.

2.3 Data Word Transfer Rates - The maximum multi-channel rate at which the computer shall be capable of transferring to peripheral equipment or receiving from peripheral equipment, 30 bit data words, Is 167 KHz (6 microseconds per transfer). Maximum single channel rate for data transfer is 125 KHz.

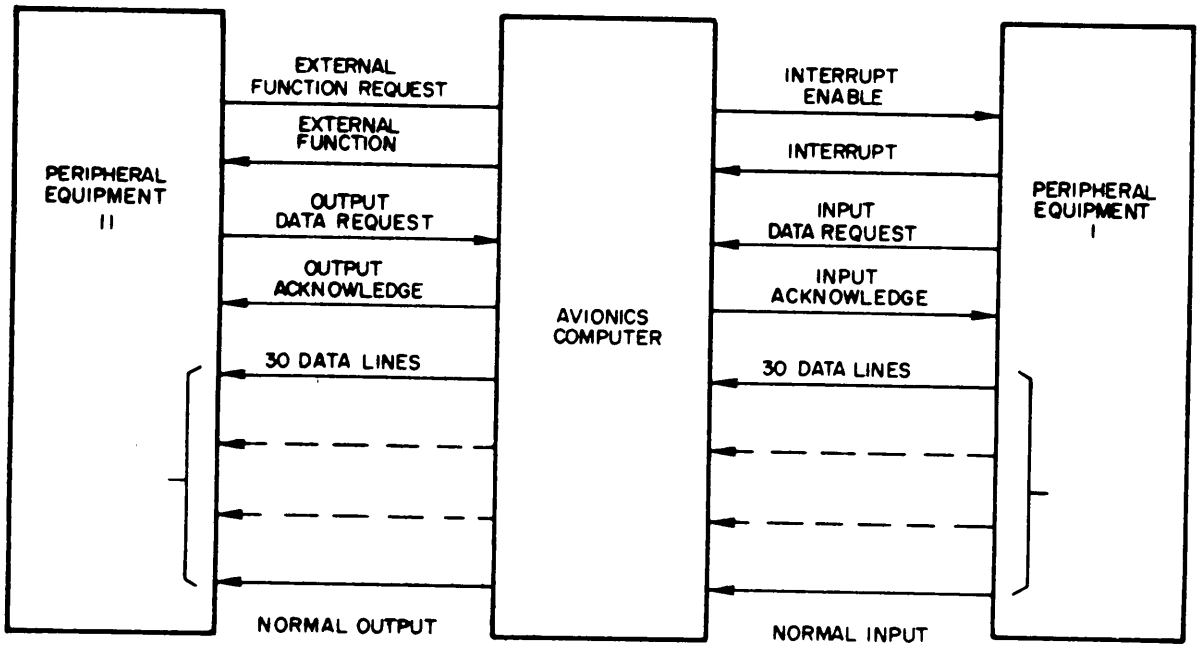


Figure 1-1. Computer to Peripheral Equipment Interface

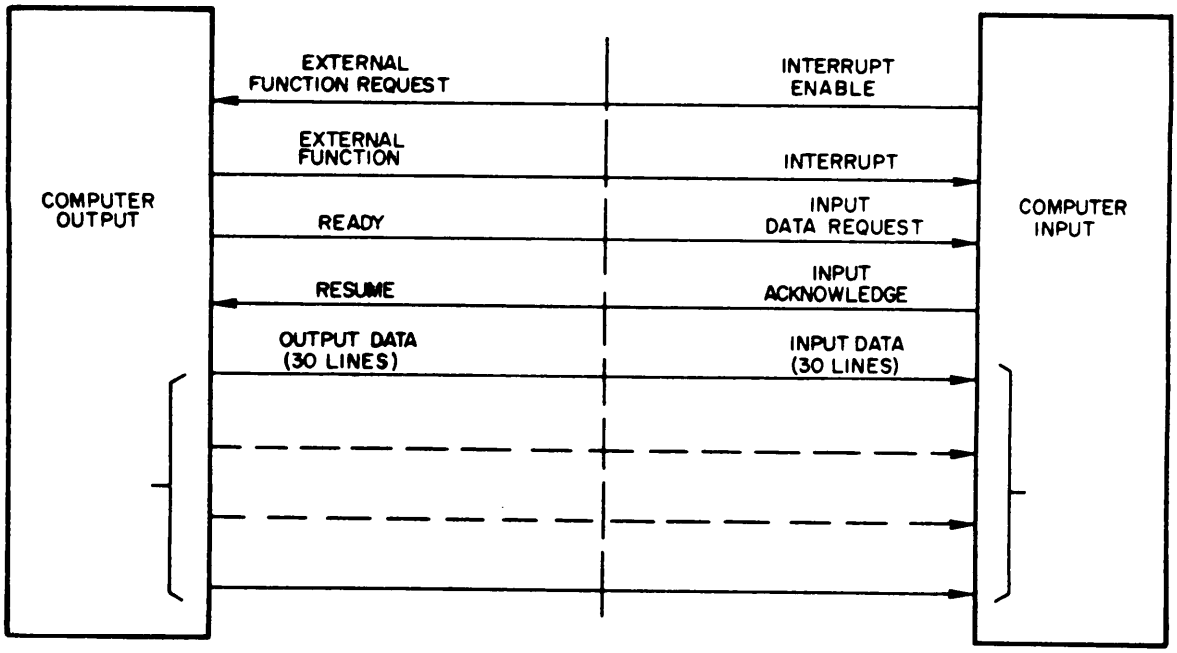
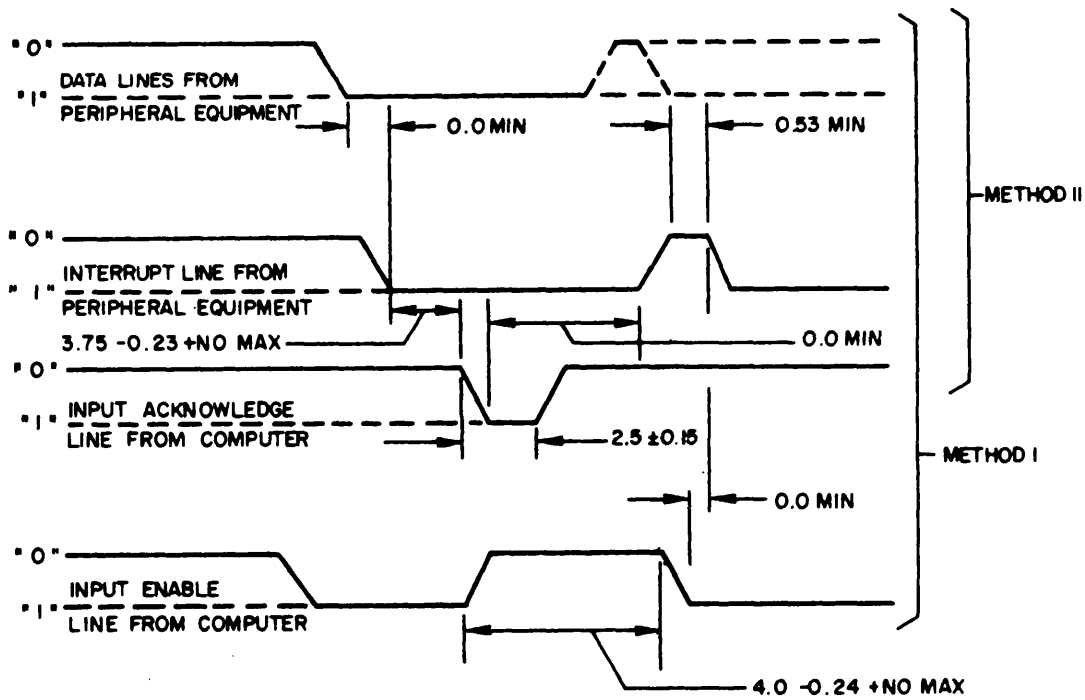


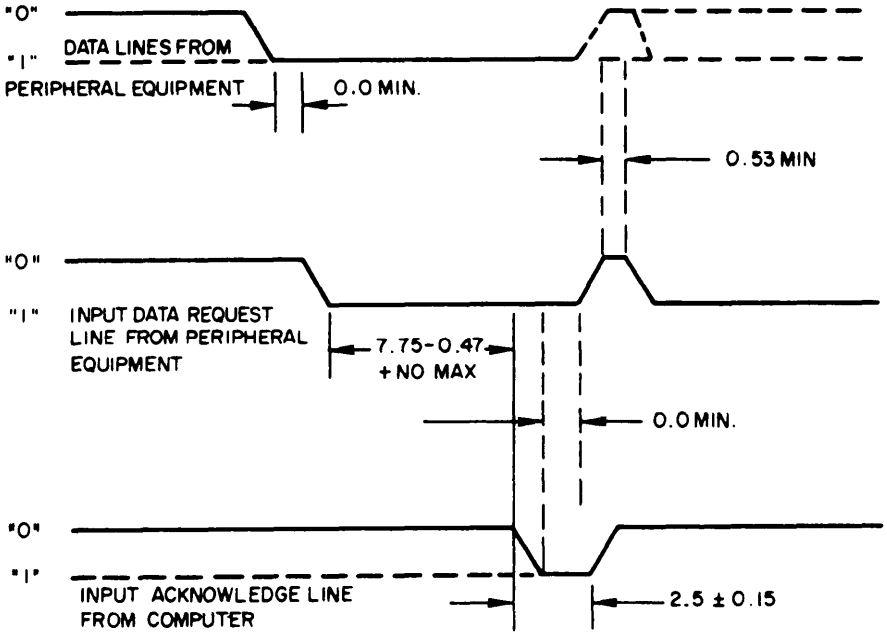
Figure 1-2. Computer to Computer Interface



NOTES:

1. ALL TRANSITION TIMES ARE: DATA LINES 1.0
   CONTROL LINES 0.25
2. ALL TIMES ARE IN MICROSECONDS
3. NO MAX DESIGNATION BEHIND A TIME NOTATION IMPLIES DEPENDENCE ON SPEED OF PERIPHERAL EQUIPMENT, I/O ACTIVITY, AND PROGRAM

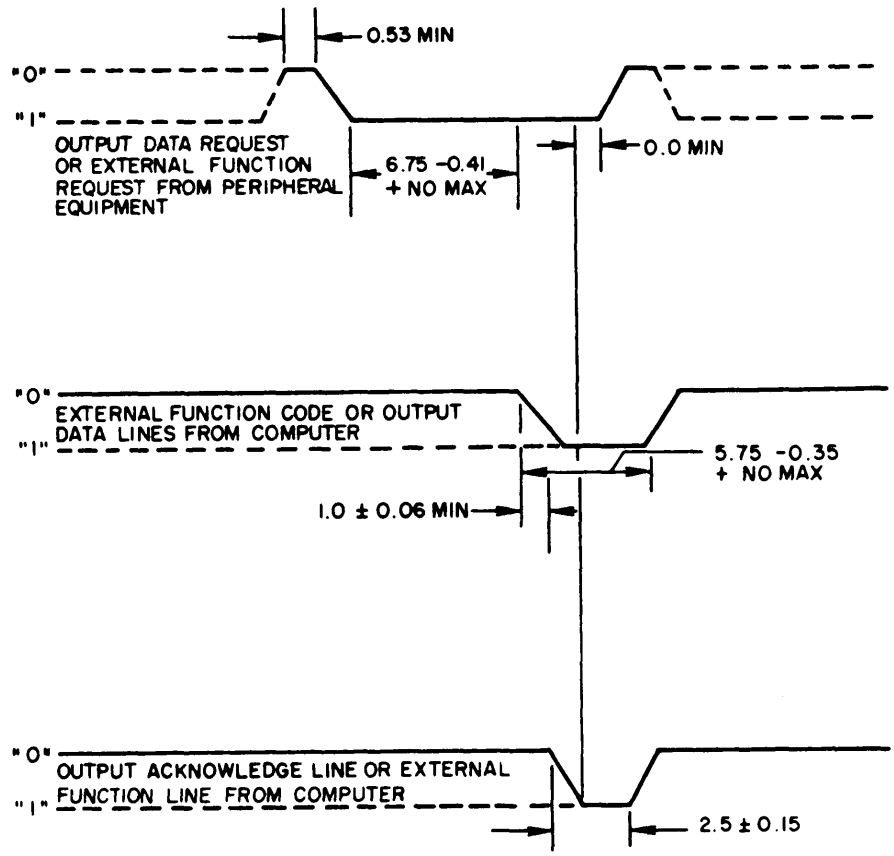
Figure 1-3. External Interrupt Input from Peripheral Equipment



NOTES:

1. ALL TRANSITION TIMES ARE: DATA LINES 1.0
   CONTROL LINES 0.25
2. ALL TIMES ARE IN MICROSECONDS
3. NO MAX. DESIGNATION BEHIND A TIME NOTATION IMPLIES DEPENDENCE ON SPEED OF PERIPHERAL EQUIPMENT, I/O ACTIVITY, AND PROGRAM

Figure 1-4. Data Input to Computer from Peripheral Equipment



NOTES:

1. ALL TRANSITION TIMES ARE: DATA LINES 1.0
   CONTROL LINES 0.25
2. ALL TIMES ARE IN MICROSECONDS
3. NO MAX DESIGNATION BEHIND A TIME NOTATION IMPLIES DEPENDENCE ON SPEED OF PERIPHERAL EQUIPMENT, I/O ACTIVITY, AND PROGRAM.

Figure 1-5. Data Outputs and External Functions from Computer

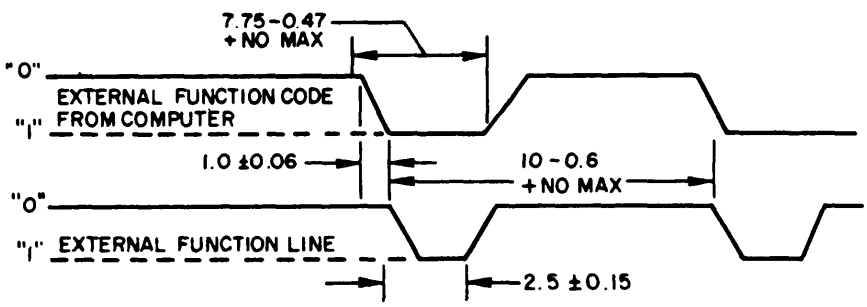


Figure 1-6. External Function with Force

APPENDIX II

INPUT AMPLIFIER CIRCUIT CHARACTERISTICS

1. SCOPE

1.1 This Appendix defines the characteristics for the Input Amplifier circuit referenced throughout this Specification.

2. REQUIREMENTS

2.1 Voltage Level Inputs - The logic “1” state shall be O volts l O. 5 volt and the logic "0" state shall be 2.5 to 5.0 volts as measured at the input terminals of the input amplifier. If both inputs of the input amplifier are disconnected this shall be considered a logic “O”.

2.2 Input Noise Rejection - The circuit shall be capable of handling common mode voltages of l 5 volts peak at the input terminals with no change in output level.

2.3 Input Impedance - The AC input impedance shall be 130 ohms nominal and the DC input impedance shall be 2000 ohms nominal.

2.4 Voltage Level Outputs - The logic “1” state shall be 4.0 to 5.5 volts and the logic “0” state shall be 0 volts ±0.5 volt.

2.5 Output Rise and Fall Times - The time required for the input amplifier circuit to switch logic levels, as measured from the 10% to 90% amplitude points at the output terminals of the amplifier shall be less than 0.5 microsecond when loaded as described in 2.7.

2.6 Output Propagation Delay - The propagation delay when loaded as described in 2.7 shall be less than 00 ns.

2.7 Output Loading- The circuit shall be capable of sinking to ground at least 10 milliamperes of current and driving a capacitive load of 50 pf at both output terminals.

2.8 Environmental Performance - The circuit shall operate within performance limits when subjected to temperatures over the range of -55°C to +100ºC.

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DOCUMENT IDENTIFIER AND TITLE

MIL-D-81347C(AS) Data Analysis Programming Group AN/AYA-8B

NAME OF ORGANIZATION AND ADDRESS

CONTRACT NUMBER

MATERIAL PROCURED UNDER A

☐ DIRECT GOVERNMENT CONTRACT ☐ SUBCONTRACT

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   A. GIVE PARAGRAPH NUMBER AND WORDING.

   B. RECOMMENDATIONS FOR CORRECTING THE DEFICIENCIES

2. COMMENTS ON ANY DOCUMENT REQUIREMENT CONSIDERED TOO RIGID

3. IS THE DOCUMENT RESTRICTIVE?

   ☐ YES ☐ NO *(If "Yes", in what way?)*

4. REMARKS

SUBMITTED BY *(Printed or typed name and address - Optional)*

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