INCH-POUND
MIL-PRF-55342H
w/ Amendment 4
29 January 2016
SUPERSEDING
MIL-PRF-55342H
w/ Amendment 3
9 June 2015

PERFORMANCE SPECIFICATION

RESISTOR, CHIP, FIXED, FILM, NONESTABLISHED RELIABILITY, ESTABLISHED RELIABILITY, SPACE LEVEL, GENERAL SPECIFICATION FOR

This specification is approved for use by all Departments and Agencies of the Department of Defense.

1. SCOPE

1.1 Scope. This specification covers the general requirements for nonestablished reliability (non-ER), established reliability (ER), and space level, fixed, film, chip resistors primarily intended for incorporation into surface mount and hybrid circuit applications. These resistors have a high degree of stability with respect to time under normal conditions. ER resistors covered by this specification have life failure rates (FR) ranging from 1 percent to 0.001 percent per 1,000 hours (see 1.2.7). These FRs are established at 60 percent confidence on the basis of life tests. Table I provides a summary of performance characteristics for these resistors. Designers are CAUTIONED on using these resistors in high power pulses applications (see 6.7).

1.2 Classification.

1.2.1 Part or Identifying Number (PIN). Resistors specified herein (see 3.1) are identified by a PIN which consists of the basic number and the associated specification. Each associated specification covers a different resistor style. The PIN provides information concerning the resistor characteristic, resistance value, resistance tolerance, termination material, and product designator. The PIN is in the following form:

* M55342	H	01	B	1E00	M
Specification indicating MIL-PRF-55342	Characteristic (see 1.2.3)	Specification sheet number Indicating MIL-PRF-55342/1	Termination material (see 1.2.4)	Resistance and resistance tolerance (see 1.2.5 & 1.2.6)	Product Level Designator (see 1.2.7)

* NOTE: A "D" prefix is used for the metric performance specification sheet MIL-PRF-55342/7.

1.2.2 Style. The style (see 3.1) is identified by the two-letter symbol "RM" followed by a four digit number; the letters identify fixed, film resistors, in a flat chip configuration.

1.2.3 Characteristic. The characteristic is identified by the single letter E, H, K, L or M, in accordance with table I.

Comments, suggestions, or questions on this document should be emailed to usarmy.apg.rdecom-cerdec.mbx.standardization-crx@mail.mil. Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at https://assist.dla.mil.

AMSC N/A FSC 5905

TABLE I Characteristics

Test or condition	Units	Symbol				
		E	H	K	L	M
Maximum ambient temperature at full wattage (see 3.6)	Temperature °C	70	70	70	70	70
Maximum ambient temperature at zero wattage (see 3.6)	Temperature °C	150	150	150	150	150
Thermal shock (see 3.9)	Maximum percent change in resistance (0.005 ohm additional allowed for measurement error)	±0.1%	±0.25%	±0.5%	±0.5%	±0.5%
Power conditioning (space level only) (see 3.10)		±0.2%	±0.25%	±0.5%	±0.5%	±0.5%
Low temperature operation (see 3.11)		±0.1%	±0.25%	±0.25%	±0.25%	±0.5%
Short time overload (see 3.12)		±0.1%	±0.1%	±0.25%	±0.25%	±0.5%
High temperature exposure (see 3.13)		±0.1%	±0.2%	±0.5%	±0.5%	±1.0%
Moisture resistance (see 3.15)		±0.2%	±0.4%	±0.5%	±0.5%	±0.5%
Life (see 3.17 & figure 3) Qualification FR level		 ±0.5% ±2.0%	 ±0.5% ±2.0%	 ±0.5% ±2.0%	 ±0.5% ±2.0%	 ±2.0% ±2.0%
Resistance to soldering heat (see 3.14.1)	Maximum percent change in resistance (0.01 ohm additional allowed for measurement error)	±0.2%	±0.25%	±0.25%	±0.25%	±0.25%
Resistance to bonding exposure (see 3.14.2)		±0.2%	±0.25%	±0.25%	±0.25%	±0.25%
Resistance temperature coefficient (see 3.16)	ppm/°C	±25	±50	±100	±200	±300
Resistance tolerance ± percent (see table IV)	± percent	 0.1 0.25 0.5 1.0 2.0 5.0 10.0	 0.1 0.25 0.5 1.0 2.0 5.0 10.0	 0.1 0.25 0.5 1.0 2.0 5.0 10.0	 0.1 0.25 0.5 1.0 2.0 5.0 10.0	 1.0 2.0 5.0 10.0

1.2.4 Termination material. The termination material designation will be in accordance with table II (see 4.8.1.3).

TABLE II. Termination materials.

Type	Material	Termination area	Code letters
Solderable 1/	Base metallization barrier metal, solder coated	Wraparound 2/	B 4/
Epoxy bondable	Gold	Wraparound 2/	G
	Platinum gold	Wraparound 2/ One surface	U T 3/
	Palladium/silver or Platinum/silver	Wraparound 2/	C
	Palladium/silver or Platinum/silver	One surface	D 3/
Wire bondable	Gold	One surface	W 3/

1/ Solderable termination's is pretinned for solder reflow operation and will meet the solderability test. The pretinning is, as a minimum, on at least the bottom and ends of the chip and only those surfaces must meet the solderability test (see figure 2).
2/ Wrap-around type will be illustrated on the associated specifications (see 3.5.2.1).
3/ See 6.4.4.
4/ See 6.4.7

1.2.5 Resistance. The nominal resistance expressed in ohms is identified by four characters consisting of three digits and a letter. The letter is used simultaneously as a decimal point, multiplier, and a resistance tolerance designator. For resistance values:

a. Greater than or equal to 1 ohm but less than 1,000 ohms, the letters A, D, G, J, M, R and W are used to represent a decimal point, depending on the resistance tolerance (see table III).

b. Greater than or equal to 1,000 ohms but less than 1 megohm, the letters B, E, H, K, N, U and Y are used to represent a decimal point, depending on the resistance tolerance (see table III).

c. Greater than or equal to 1 megohm, the letters C, F, T, L, P, V and Z are used to represent a decimal point, depending upon the resistance tolerance (see table III).

All digits preceding and following the letters (A, B, C, R, U, V, W, Y, Z, D, E, F, G, H, T, L, J, K, M, N, and P) of the group represent significant figures. The resistance value designators are shown in table III. Minimum and maximum resistance values will be as specified herein (see 3.1). The standard values for every decade will follow the sequence specified in table V for resistance tolerances 0.25 percent, 0.5 percent, 1.0 percent, 2.0 percent, 5.0 percent, and 10.0 percent. The resistance values for tolerance 0.1 percent maybe any value within the limits specified (see 3.1), but it is preferred that values be chosen from the 0.1 percent column of table V.

TABLE III. Designator of resistance values for resistance tolerances.

Designator for 0.1 percent tolerance	Resistance ohms	Designator for 0.25 percent tolerance	Resistance ohms
1A00 to 9A88 incl.	1.00 to 9.88 incl.	1R00 to 9R88 incl.	1.00 to 9.88 incl.
10A0 to 98A8 incl.	10.0 to 98.8 incl.	10R0 to 98R8 incl.	10.0 to 98.8 incl.
100A to 988A incl.	100 to 988 incl.	100R to 988R incl.	100 to 988 incl.
1B00 to 9B88 incl.	1,000 to 9,880 incl.	1U00 to 9U88 incl.	1,000 to 9,880 incl.
10B0 to 98B8 incl.	10,000 to 98,800 incl.	10U0 to 98U8 incl.	10,000 to 98,800 incl.
100B to 988B incl.	100,000 to 988,000 incl.	100U to 988U incl.	100,000 to 988,000 incl.
1C00 to 9C88 incl.	1,000,000 to 9,880,000 incl.	1V00 to 9V88 incl.	1,000,000 to 9,880,000 incl.
10C0 to 22C0	10,000,000 to 22,000,000	10V0 to 22V0	10,000,000 to 22,000,000
Designator for 0.5 percent tolerance	**Resistance ohms**	**Designator for 1 percent tolerance**	**Resistance ohms**
1W00 to 9W88 incl.	1.00 to 9.88 incl.	1D00 to 9D76 incl.	1.00 to 9.76 incl.
10W0 to 98W8 incl.	10.0 to 98.8 incl.	10D0 to 97D6 incl.	10.0 to 97.6 incl.
100W to 988W incl.	100 to 988 incl.	100D to 976D incl.	100 to 976 incl.
1Y00 to 9Y88 incl.	1,000 to 9,880 incl.	1E00 to 9E76 incl.	1,000 to 9,760 incl.
10Y0 to 98Y8 incl.	10,000 to 98,800 incl.	10E0 to 97E6 incl.	10,000 to 97,600 incl.
100Y to 988Y incl.	100,000 to 988,000 incl.	100E to 976E incl.	100,000 to 976,000 incl.
1Z00 to 9Z88 incl.	1,000,000 to 9,880,000 incl.	1F00 to 9F76 incl.	1,000,000 to 9,760,000 incl.
10Z0 to 22Z0	10,000,000 to 22,000,000	10F0 to 22F0	10,000,000 to 22,000,000
Designator for 2 percent tolerance	**Resistance ohms**	**Designator for 5 percent tolerance**	**Resistance ohms**
1G00 to 9G10 incl.	1.00 to 9.10 incl.	1J00 to 9J10 incl.	1.00 to 9 .10 incl.
10G0 to 91G0 incl.	10.0 to 91.0 incl.	10J0 to 91J0 incl.	10.0 to 91.0 incl.
100G to 910G incl.	100 to 910 incl.	100J to 910J incl.	100 to 910 incl.
1H00 to 9H10 incl.	1,000 to 9,100 incl.	1K00 to 9K10 incl.	1,000 to 9,100 incl.
10H0 to 91H0 incl.	10,000 to 91,000 incl.	10K0 to 91K0 incl.	10,000 to 91,000 incl.
100H to 910H incl.	100,000 to 910,000 incl.	100K to 910K incl.	100,000 to 910,000 incl.
1T00 to 9T10 incl.	1,000,000 to 9,100,000 incl.	1L00 to 9L10 incl.	1,000,000 to 9,100,000 incl.
10T0 to 22T0	10,000,000 to 22,000,000	10L0 to 22L0	10,000,000 to 22,000,000
Designator for 10 percent tolerance	**Resistance ohms**		
1M00 to 8M20 incl.	1.00 to 8.20 incl.		
10M0 to 82M0 incl.	10.0 to 82.0 incl.		
100M to 820M incl.	100 to 820 incl.		
1N00 to 8N20 incl.	1,000 to 8,200 incl.		
10N0 to 82N0 incl.	10,000 to 82,000 incl.		
100N to 820N incl.	100,000 to 820,000 incl.		
1P00 to 8P20 incl.	1,000,000 to 8,200,000 incl.		
10P0 to 22P0	10,000,000 to 22,000,000		

1.2.6 Resistance tolerance and multipliers. The resistance tolerance and multipliers are identified by a single letter in accordance with table IV.

TABLE IV. Resistance tolerance and multipliers.

Resistance tolerance (±)	Multiplier	Symbol		Resistance tolerance (±)	Multiplier	Symbol
0.1	X1	A		2.0	X1	G
0.1	X1,000	B		2.0	X1,000	H
0.1	X1,000,000	C		2.0	X1,000,000	T
0.25	X1	R		5.0	X1	J
0.25	X1,000	U		5.0	X1,000	K
0.25	X1,000,000	V		5.0	X1,000,000	L
0.5	X1	W		10.0	X1	M
0.5	X1,000	Y		10.0	X1,000	N
0.5	X1,000,000	Z		10.0	X1,000,000	P
1.0	X1	D				
1.0	X1,000	E				
1.0	X1,000,000	F				

TABLE V. Standard resistance values for the 10 to 100 decade.

0.1 0.25 0.5	1.0	2.0 5.0	10.0	0.1 0.25 0.5	1.0	2.0 5.0	10.0	0.1 0.25 0.5	1.0	2.0 5.0	10.0
10.00	10.00	10.00	10.00	20.00	20.00	20.00		37.90			
10.10				20.30				38.30	38.30		
10.20	10.20			20.50	20.50			38.80			
10.40				20.80						39.00	39.00
10.50	10.50			21.00	21.00			39.20	39.20		
10.60				21.30				39.70			
10.70	10.70			21.50	21.50			40.20	40.20		
10.90				21.80				40.70			
11.00	11.00	11.00				22.00	22.00	41.20	41.20		
11.10				22.10	22.10			41.70			
11.30	11.30			22.30				42.20	42.20		
11.40				22.60	22.60			42.70			
11.50	11.50			22.90						43.00	
11.70				23.20	23.20			43.20	43.20		
11.80	11.80			23.40				43.70			
12.00		12.00	12.00	23.70	23.70			44.20	44.20		
12.10	12.10			24.00		24.00		44.80			
12.30				24.30	24.30			45.30	45.30		
12.40	12.40			24.60				45.90			
12.60				24.90	24.90			46.40	46.40		
12.70	12.70			25.20				47.00		47.00	47.00
12.90				25.50	25.50			47.50	47.50		
13.00	13.00	13.00		25.80				48.10			
13.20				26.10	26.10			48.70	48.70		
13.30	13.30			26.40				49.30			
13.50				26.70	26.70			49.90	49.90		
13.70	13.70					27.00	27.00	50.50			
13.80				27.10						51.00	51.00 1/
14.00	14.00			27.40	27.40			51.10	51.10		
14.20				27.70				51.70			
14.30	14.30			28.00	28.00			52.30	52.30		
14.50				28.40				53.00			
14.70	14.70			28.70	28.70			53.60	53.60		
14.90				29.10				54.20			
15.00	15.00	15.00	15.00	29.40	29.40			54.90	54.90		
15.20				29.80				55.60			
15.40	15.40					30.00				56.00	56.00
15.60				30.10	30.10			56.20	56.20		
15.80	15.80			30.50				56.90			
16.00		16.00		30.90	30.90			57.60	57.60		
16.20	16.20			31.20				58.30			
16.40				31.60	31.60			59.00	59.00		
16.50	16.50			32.00				59.70			
16.70				32.40	32.40			60.40	60.40		
16.90	16.90			32.80				61.20			
17.20						33.00	33.00	61.90	61.90		
17.40	17.40			33.20	33.20					62.00	
17.60				33.60				62.60			
17.80	17.80			34.00	34.00			63.40	63.40		
18.00		18.00	18.00	34.40				64.20			
18.20	18.20			34.80	34.80			64.90	64.90		
18.40				35.20				65.70			
18.70	18.70			35.70	35.70			66.50	66.50		
18.90						36.00		67.30			
19.10	19.10			36.10						68.00	68.00
19.30				36.50	36.50			68.10	68.10		
19.60	19.60			37.00				69.00			
19.80				37.40	37.40						

TABLE V. Standard resistance values for the 10 to 100 decade - Continued.

0.1 0.25 0.5	1.0	2.0 5.0	10.0	0.1 0.25 0.5	1.0	2.0 5.0	10.0	0.1 0.25 0.5	1.0	2.0 5.0	10.0
69.80	69.80			79.60				88.70	88.70		
70.60				80.60	80.60			89.80			
71.50	71.50			81.60				90.90	90.90		
72.30						82.00	82.00			91.00	
73.20	73.20			82.50	82.50			92.00			
74.10				83.50				93.10	93.10		
75.00	75.00	75.00	1/ 75.00	84.50	84.50			94.20			
75.90				85.60				95.30	95.30		
76.80	76.80			86.60	86.60			96.50			
77.70				87.60				97.60	97.60		
78.70	78.70							98.80			

1/ Inactive for new design

1.2.7 Product level designator. The product level designator is specified in table VI by a single letter which identifies non-ER, ER or space level resistors.

TABLE VI. Product level designator.

Product level designator	Product level
C	Non-ER
M	1/ 1.0
P	1/ 0.1
R	1/ 0.01
S	1/ 0.001
T	Space level
U	1/ 0.01 with group A and all of B inspection test ran on each production lot.
V	1/ 0.001 with group A and all of B inspection test ran on each production lot.

1/ FR level in percent per 1000 hours

2. APPLICABLE DOCUMENTS

2.1 General. The documents listed in this section are specified in sections 3 and 4 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements documents cited in sections 3 and 4 of this specification, whether or not they are listed.

2.2 Government documents

2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

(See supplement 1 for list of associated specifications.)

* DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-202 - Electronic and Electrical Component Parts, Test Methods for.
MIL-STD-202-106 - Test Method Standard Method 106, Moisture Resistance.
MIL-STD-202-107 - Test Method Standard Method 107, Thermal Shock.
MIL-STD-202-108 - Test Method Standard Method 108, Life (At Elevated Ambient Temperature).
MIL-STD-202-208 - Test Method Standard Method 208, Solderability.
MIL-STD-202-210 - Test Method Standard Method 210, Resistant to Soldering Heat.
MIL-STD-202-215 - Test Method Standard Method 215, Resistant to Solvents.
MIL-STD-202-303 - Test Method Standard Method 303, DC Resistance.
MIL-STD-202-304 - Test Method Standard Method 304, Resistance-Temperature Characteristic.
MIL-STD-690 - Failure Rate Sampling Plans and Procedures.
MIL-STD-790 - Standard Practice for Established Reliability and High Reliability Qualified Products List (QPL) Systems for Electrical, Electronic, and Fiber Optic Parts Specifications.
MIL-STD-1285 - Marking of Electrical and Electronic Parts.

(Copies of these documents are available online at http://quicksearch.dla.mil.)

2.2.2 Other Government documents, drawings, and publications. The following other Government documents, drawings, and publications form a part of this document to the extent specified herein. Unless otherwise specified, the issues are those cited in the solicitation.

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION (NASA)

NASA 1124 - Outgassing Data for Selecting Spacecraft Materials.

(Hard copies of this document are no longer available from the NASA Goddard Materials Branch or the DLA Document Services. This information is only available at http://outgassing.nasa.gov.)

2.3 Non-Government publications. The following documents form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

SAE INTERNATIONAL

SAE-EIA-554-1 - Assessment of Outgoing Nonconforming Levels in Parts Per Million (ppm).
SAE-EIA-557 - Statistical Process Control Systems.

(Copies of these documents are available online at http://www.sae.org.)

AMERICAN SOCIETY FOR TESTING AND MATERIALS (ASTM)

ASTM E595 - Materials from Outgassing in a Vacuum Environment, Total Mass Loss and Collected Volatile Condensable, Standard Test Method for.

(Copies of these documents are available online at http://www.astm.org.)

IPC ASSOCIATION CONNECTING ELECTRONICS INDUSTRIES (IPC)

IPC CC 830 - Qualification and Performance of Electrical Insulation compound for Printed Wiring Assemblies

(Copies of this document are available online at www.ipc.org.)

2.4 Order of precedence. Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein (except for related, specification sheets), the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Specification sheets. The individual item requirements shall be as specified herein and in accordance with the applicable specification sheet. In the event of any conflict between the requirements of this specification and the specification sheet, the latter shall govern.

3.2 Qualification. Resistors furnished under this specification shall be products that are authorized by the qualifying activity for listing on the applicable qualified products list (QPL) before contract award. In addition, the manufacturer shall obtain certification from the qualifying activity that the product assurance requirements of 4.2.1 have been met and are being maintained.

3.3 QPL system. The manufacturer shall establish and maintain a QPL system for parts covered by this specification. Requirements for this system are specified in MIL-STD-790 (all product levels) and MIL-STD-690 (ER parts only). In addition, the manufacturer shall also establish a Statistical Process Control (SPC) and Part Per Million (ppm) system that meets the requirements as described in 3.3.1 and 3.3.2 respectively.

3.3.1 SPC system. As part of the overall MIL-STD-790 QPL system, the manufacturer shall establish an SPC system that meets the requirements of SAE-EIA-557. Typical manufacturing processes for application of SPC include formation of resistance elements, trimming, and termination. In addition, the manufacturer shall demonstrate resistance temperature characteristic (RTC) control in the process.

3.3.2 PPM system. As part of the overall MIL-STD-790 QPL system, the manufacturer shall establish a ppm system for assessing the average outgoing quality of lots in accordance with SAE-EIA-554-1 and 4.6.4. Data exclusion, in accordance with SAE-EIA-554-1, may be used with approval of the qualifying activity. The ppm system shall identify the ppm rate at the end of each month and shall be based on a six month moving average. PPM-2 and dc resistance shall be assessed for each style. Style reporting may include both non-ER and ER style combinations. Due to low production volume, ppm assessment does not apply to space level lots.

3.4 Materials. Materials shall be used which will enable the resistors to meet the performance requirements of this specification. Acceptance or approval of any constituent material shall not be construed as a guaranty of the acceptance of the finished product.

3.5 Interface and physical dimension requirements. Resistors shall meet the interface and physical dimensions specified (see 3.1).

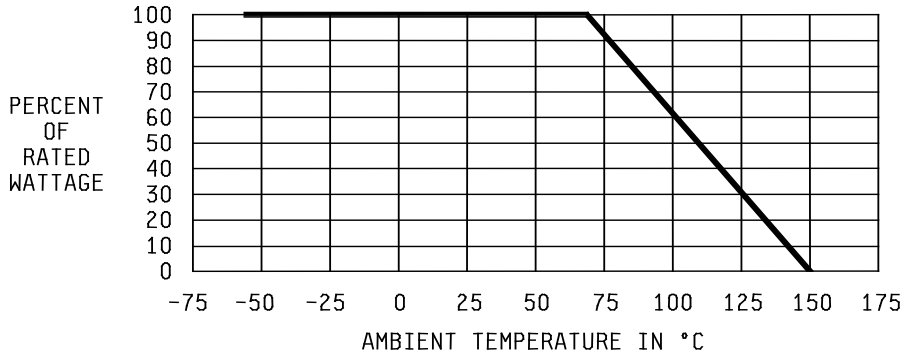
3.5.1 Termination. Unless otherwise specified, both terminations (areas) shall be available on one surface of the body of the resistor chip (see 1.2.4).

3.5.2 Barrier metallization. The barrier metallization for the B termination (base metallization barrier metal, solder coated) shall be nickel. The metallization shall be a minimum of 50 microinches.

3.5.2.1 Terminal substitution data. For existing design and logistical support of the deleted termination R (solderable pretinned wraparound termination's), termination B (solderable base metallization barrier metal, solder coated) shall be used as a substitute for termination R.

3.5.3 Pure tin. The use of pure tin, as an underplate or final finish is prohibited both internally and externally. Tin content of resistor components and solder shall not exceed 97 percent, by mass. Tin shall be alloyed with a minimum of 3 percent lead, by mass (see 6.4.5).

3.6 Power rating. The resistors shall have a power rating based on continuous full-load operation at an ambient temperature of 70°C. For operation at temperatures in excess of 70°C the load shall be derated in accordance with figure 1.



NOTE: This curve indicates the percentage of nominal wattage to be applied at temperature higher than 70°C. This curve applies only to units mounted on a board (see 4.8.1.3); however, at no time shall the applied voltage exceed the maximum for each style (see 3.1).

FIGURE 1. Derating curve for high ambient temperatures.

3.7 Voltage rating. Resistors shall have a rated dc continuous working voltage or an approximate sine wave root-mean-square (rms) continuous working voltage corresponding to the wattage (power) rating, as determined from the following formula:

$$E = \sqrt{PR}$$

Where:

E = Continuous rated dc or rms working voltage in volts.
P = Rated wattage in watts.
R = Nominal resistance in ohms.

In no case shall the rated voltage be greater than the applicable maximum voltage (see 3.1).

3.8 DC resistance. When resistors are tested as specified in 4.8.2, the dc resistance shall be within the specified tolerance of the nominal resistance (see 1.2.5).

3.8.1 Resistance value deviations. All maximum deviations as specified in this section are to be considered absolute limits with the exception of the contact resistance adjustments.

3.9 Thermal shock.

3.9.1 Thermal shock (failure rate levels (FRL) M, P, R, S, U and V). When resistors are tested as specified in 4.8.3, there shall be no evidence of mechanical damage; the change in resistance shall be within the specified initial resistance tolerance of the nominal resistance for group A tests and the change in resistance for group C tests shall not exceed the value specified in table I.

3.9.2 Thermal shock (space level only). When resistors are tested as specified in 4.8.3, there shall be no evidence of mechanical damage; the combined change in resistance for thermal shock and power conditioning during group A inspection shall not exceed the values listed in table I for power conditioning. For the 100 cycle qualification test, the change in resistance shall not exceed the values listed in table I for the power conditioning.

3.10 Power conditioning (space level only). When resistors are tested as specified in 4.8.4, there shall be no evidence of mechanical damage; the combined change in resistance, for thermal shock and power conditioning, shall not exceed the values listed in table I for power conditioning.

3.10.1 Power conditioning (space level only) alternate process. For T level wire-bondable (W termination) resistors, high temperature exposure may be used in lieu of power conditioning (see 3.10) after the thermal shock test. When resistors are tested as specified in 4.8.7 and 4.8.3 (except the parts shall not be mounted) there shall be no evidence of mechanical damage. The combined change in resistance, for high temperature exposure and thermal shock, shall not exceed the values listed in table I for power conditioning.

3.11 Low temperature operation. When resistors are tested as specified in 4.8.5, there shall be no evidence of mechanical damage; the change in resistance between the initial and the final measurement at 25°C ±5°C shall not exceed the value specified in table I.

3.12 Short time overload. When resistors are tested as specified in 4.8.6, there shall be no evidence of arcing, burning, or charring, the change in resistance shall not exceed the value specified in table I .

3.13 High temperature exposure. When resistors are tested as specified in 4.8.7, there shall be no evidence of mechanical damage and the change in resistance shall not exceed the value specified in table I.

3.14 Resistance to soldering heat and bonding exposure.

3.14.1 Resistance to soldering heat. When resistors are tested as specified in 4.8.8.1, there shall be no evidence of mechanical damage, no demetallization or leaching, and the change in resistance shall not exceed the value specified in table I.

3.14.2 Resistance to bonding exposure. When resistors are tested as specified in 4.8.8.2, there shall be no evidence of mechanical damage, no demetallization or leaching, and the change in resistance shall not exceed the value specified in table I.

3.15 Moisture resistance. When resistors are tested as specified in 4.8.9, there shall be no evidence of mechanical damage; the change in resistance between the initial and final measurements shall not exceed the value specified in table I.

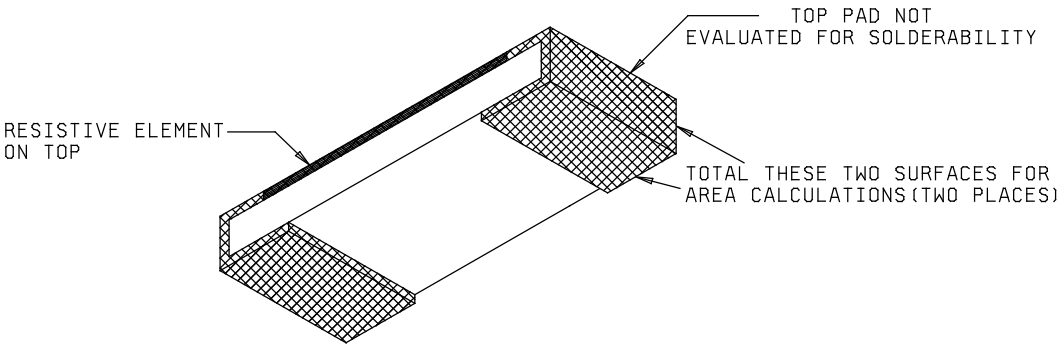
3.16 Resistance temperature characteristic. When resistors are tested as specified in 4.8.10, the resistance temperature characteristic, at each of the temperatures specified in 4.8.10b referred to room ambient temperature, shall not exceed the values specified in table I.

3.17 Life.

3.17.1 Qualification. When resistors are tested as specified in 4.8.11, there shall be no evidence of mechanical damage. The change in resistance between the initial measurement and any succeeding measurements up to and including 2,000 hours shall not exceed the value specified in table I.

3.17.2 FRL determination (ER). When resistors are tested as specified in 4.8.11, there shall be no evidence of mechanical damage to the resistance element, or enclosure. The change in resistance between the initial measurement and any of the succeeding measurements shall not exceed the value specified in table I. This single failure criterion shall be applicable to all measurements during the life test for purposes of determining FRL qualification and is applicable as a parallel requirement with 3.17.1 to measurements made during the life test specified for qualification inspection.

3.18 Solderability (applicable to termination B). When resistors are tested as specified in 4.8.12, the immersed metallized surface shall be at least 95 percent covered with a new clean smooth coating and shall exhibit no demetallization or leaching of the terminal areas. The remaining 5 percent may contain only small pinholes or rough spots; these shall not be concentrated in one area. In case of dispute, the percentage of coverage with pinholes or rough spots shall be determined by actual measurement of these areas, as compared to the total area. The top surface of the solder pad need not be considered in the evaluation for solderability (see figure 2). For coverage calculations, defective areas on each termination shall be compared to the total area of the end and bottom surfaces on the same termination.



NOTES:
1. Top solder pad need not be evaluated for solderability.
2. Resistive element on top.
3. Ends and bottom are surfaces to be evaluated.

FIGURE 2. Solderability coverage.

3.19 Mounting integrity.

3.19.1 Solder mounting integrity (applicable to termination B). When resistors are tested as specified in 4.8.13.1, there shall be no evidence of mechanical damage.

3.19.2 Bondable mounting integrity (applicable to termination's G, U, T, C, and D). When resistors are tested as specified in 4.8.13.2, there shall be no evidence of mechanical damage.

3.19.3 Wire bonding integrity (applicable to termination W). When resistors are tested as specified in 4.8.13.3, there shall be no evidence of mechanical damage.

3.20 Resistance to solvents (applicable to resistors that are marked with color dots or screen printed characters). When resistors are tested as specified in 4.8.14, there shall be no evidence of mechanical damage and the marking shall remain legible. The color dot marking shall be in accordance with MIL-STD-1285.

3.21 Marking legibility.

3.21.1 Marking legibility test (applicable to laser marked resistors). When resistors are tested as specified in 4.8.15, the marking shall remain legible.

3.22 Recycled, recovered, environmentally preferable, or biobased materials. Recycled, recovered, environmentally preferable or biobased materials should be used to the maximum extent possible, provided that the material meets or exceeds the operational and maintenance requirements, and promotes economically advantageous life cycle costs.

3.23 Visual inspection. Resistors shall be inspected as specified in 4.8.1, to verify that the interface, physical dimensions, marking, and workmanship are in accordance with the applicable requirements (see 3.1, 3.4, 3.5, 3.5.1 to 3.5.3 inclusive, and appendix B).

3.24 Outgassing (space level only). When examined as specified in 4.8.16, the samples shall meet the following requirements:

a. Total Mass Loss (TML) shall not exceed 1 percent.

b. Volatile Condensable Material (VCM) shall not exceed 0.1 percent.

3.24.1 Outgassing test data (see 2.2.2). Data listed in NASA 1124 may be used in lieu of actual test data for applicable materials.

3.25 Marking. A noncorrosive label containing the following information shall be applied to each unit package. PIN, "JAN" marking, date code, source code, and manufacturer's production lot code (see 4.6.2.2). Date and source code shall be in accordance with MIL-STD-1285. The following is an example of the complete marking:

12345 - CAGE
0312J - Date code and JAN marking
M55342H01 - PIN
B10A5M - PIN
- Manufacturer's production lot code

The date code shall be the date of the final assembly operation. The common manufacturing record shall include the same date code as that placed on the parts covered by the record. At the option of the manufacturer, resistors may be marked (i.e., laser, color dot, screen printed, etc.). Other markings which in any way interfere with, obscure, or confuse those specified herein are prohibited. Additional marking may appear on the package provided that it does not interfere with the required marking. The marking process must be approved by the qualifying activity based on testing specified herein. The marking shall remain legible after all tests.

3.25.1 Individual chip marking. Marking of individual chip resistors is not required but is permitted. Chip resistors may be marked using the following code systems. The marking requirement and code system used shall be specified on the order. If no code system is specified, the manufacturer may select the code. Abbreviated markings are due to limited space takes precedence over PIN format.

3.25.1.1 Option 1, four character part number code. Markings shall be the same four characters used to indicate resistance and tolerance in the PIN. See 1.2.5 and 1.2.6 and table III and table V.

Example: 30.1k ohms and 1 percent tolerance = 30E1
18.2 ohms and 1 percent tolerance = 18D2

3.25.1.2 Option 2, four characters for 0.1, 0.25, 0.5 and 1.0 percent tolerances. The first three digits are significant figures and the last digit specifies the number of zeros to follow. When the value of resistance is less than 100 ohms, or when fractional values of an ohm are required, the letter “R” shall be substituted for one of the significant digits to represent the decimal point. When the letter “R” is used, succeeding digits of the group represent significant figures.

Example: 5.62 ohms = 5R62
14.7 ohms = 14R7
30.1 kohms = 3012

3.25.1.3 Option 3, three characters for 0.1, 0.25, 0.5, 1.0, 2, 5, and 10 percent tolerances. The first two digits are significant figures and the last digit specifies the number of zeros to follow. When the value of resistance is less than 10 ohms, or when fractional values of an ohm are required, the letter "R" shall be substituted for one of the significant digits to represent the decimal point. When the letter "R" is used, succeeding digits for the group represents significant figures.

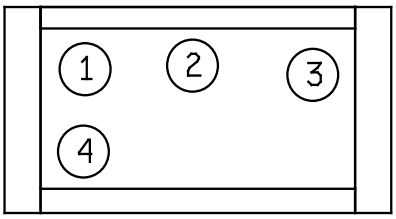
Example: 9.7 ohms = 9R7
330 kohms = 334
12 ohms = 120

Standard 0.1, 0.25, 0.5, and 1.0 percent values may be furnished to this option due to limited space provided the third character is insignificant, such as 21.00, 34.00, and 59.00.

3.25.1.4 Option 4, four dots for 0.1, 0.25, 0.5 and 1.0 percent tolerances. Four color dots shall be present in the location and order as shown in the following example.

Example: 1st dot = 1st significant digit
2nd dot = 2nd significant digit
3rd dot = 3rd significant digit
4th dot = multiplier (Ref. MIL-STD-1285)

30.1 kohms = Orange Black Brown Red

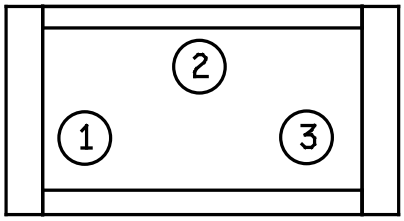


NOTE: Abbreviated marking due to limited space takes precedence over PIN format.

3.25.1.5 Option 5, three color dots for 2, 5, and 10 percent tolerances. Three color dots shall be present in the location and order as shown in the following example.

Example: 1st dot = 1st significant digit
2nd dot = 2nd significant digit
3rd dot = multiplier (Ref. MIL-STD-1285)

330 kohms = Orange Orange Yellow



NOTE: Abbreviated marking due to limited space takes precedence over PIN format.

3.25.2 Option 6, three digit code for indicating value and tolerance. For 0.1 percent, 0.25 percent, 0.5 percent, and 1 percent tolerance, the first two digits are numbers indicating standard decade values. The third character is a letter multiplier. For 2, 5, and 10 percent tolerances, the first character is a letter multiplier followed by a two digit number that indicates standard decade values as shown in the following examples.

THREE DIGIT CODE FOR 0.1, 0.25, 0.5 AND 1 PERCENT TOLERANCE

(A = 10^0, B = 10^1, C = 10^2, D = 10^3, E = 10^4, R = 10^{-1}, S = 10^{-2})

Examples:	Resistance	Code
	1.00	01S
	12.1	09R
	165	22A
	4.32 MEG	62E

0.1, 0.25, 0.5 and 1 percent tolerance											
Symbol	Resistance	Symbol	Resistance	Symbol	Resistance	Symbol	Resistance	Symbol	Resistance	Symbol	Resistance
01	100	17	147	33	215	49	316	65	464	81	681
02	102	18	150	34	221	50	324	66	475	82	698
03	105	19	154	35	226	51	332	67	487	83	715
04	107	20	158	36	232	52	340	68	499	84	732
05	110	21	162	37	237	53	348	69	511	85	750
06	113	22	165	38	243	54	357	70	523	86	768
07	115	23	169	39	249	55	365	71	536	87	787
08	118	24	174	40	255	56	374	72	549	88	806
09	121	25	178	41	261	57	383	73	562	89	825
10	124	26	182	42	267	58	392	74	576	90	845
11	127	27	187	43	274	59	402	75	590	91	866
12	130	28	191	44	280	60	412	76	604	92	887
13	133	29	196	45	287	61	422	77	619	93	909
14	137	30	200	46	294	62	432	78	634	94	931
15	140	31	205	47	301	63	442	79	649	95	953
16	143	32	210	48	309	64	453	80	665	96	976

THREE DIGIT CODE FOR 2, 5, and 10 PERCENT TOLERANCE

(A = 10^0, B = 10^1, C = 10^2, D = 10^3, E = 10^4, R = 10^{-1}, S = 10^{-2})

Examples:	Tolerance	Resistance	Code
	2-percent	1.00	S01
	5-percent	1.00	S25
	10-percent	1.00	S49
	5-percent	510	A42
	10-percent	820k	D60

2 percent		5 percent		10 percent	
Symbol	Resistance	Symbol	Resistance	Symbol	Resistance
01	100	25	100	49	100
02	110	26	110	50	120
03	120	27	120	51	150
04	130	28	130	52	180
05	150	29	150	53	220
06	160	30	160	54	270
07	180	31	180	55	330
08	200	32	200	56	390
09	220	33	220	57	470
10	240	34	240	58	560
11	270	35	270	59	680
12	300	36	300	60	820
13	330	37	330		
14	360	38	360		
15	390	39	390		
16	430	40	430		
17	470	41	470		
18	510	42	510		
19	560	43	560		
20	620	44	620		
21	680	45	680		
22	750	46	750		
23	820	47	820		
24	910	48	910		

NOTE: Abbreviated marking due to limited space takes precedence over PIN format.

3.25.3 JAN and J marking. The United States Government has adopted, and is exercising legitimate control over the certification marks "JAN" and "J", respectively, to indicate that items so marked or identified are manufactured to, and meet all the requirements of specifications. Accordingly, items acquired to, and meeting all of the criteria specified herein and in applicable associated specifications shall bear the certification mark "JAN" except that items too small to bear the certification mark "JAN" shall bear the letter "J". The "JAN" or "J" shall be placed immediately before the part number except that if such location would place a hardship on the manufacturer in connection with such marking, the "JAN" or "J" may be located on the first line above or below the part number. Items furnished under contracts or orders which either permit or require deviation from the conditions or requirements specified herein or in applicable associated specifications shall not bear "JAN" or "J". In the event an item fails to meet the requirements of this specification and the applicable specification sheets or associated specifications, the manufacturer shall remove completely the military part number and the "JAN" or "J" from the sample tested and also from all items represented by the sample. The “JAN” or “J” certification mark shall not be used on products acquired to contractor drawings or specifications. The United States Government has obtained Certificate of Registration Number 504,860 for the certification mark "JAN" and Registration Number 2,577,735 for the certification mark “J”.

3.25.4 Allowable substitution. A manufacturer may supply better products to less stringent product levels, resistance temperature characteristics, or resistance tolerances as specified in table VII. The label shall reflect the original part number ordered. Parts that are physically marked shall not be remarked unless specified in the contract or order (see 6.2).

3.26 Workmanship. Resistors shall be processed in such a manner as to be uniform in quality and shall meet the requirements of 3.1, 3.4, 3.5, 3.5.1 through 3.5.3 inclusive, and 3.25 as applicable, and be free from other defects that will affect life, serviceability, or appearance, and shall pass the visual inspection as specified in Appendix B.

TABLE VII. Allowable substitution.

Product level	Acceptable FR substitute
T (space)	------
V	T 1/
U	V, T 1/
S (0.001)	V, T 1/
R (0.01)	V, U, S, T 1/
P (0.1)	V, U, S, R,
M (1.0)	V, U, S, R, P
C (non-ER)	V, U, S, R, P, M
Resistance tolerance	**Acceptable resistance tolerance substitute**
0.1	----
0.25	0.1
0.5	0.1, 0.25
1.0	0.1, 0.25, 0.5
2.0	0.1, 0.25, 0.5, 1.0
5.0	0.1, 0.25, 0.5, 1.0, 2.0
10.0	0.1, 0.25, 0.5, 1.0, 2.0, 5.0
Characteristic	**Acceptable characteristic substitute**
E	---
H	E
K	E, H
L	E, H, K
M	E, H, K, L

1/ T level substitution is by qualifying activity approval.

4. VERIFICATION

4.1 Classification of inspections. The inspection requirements specified herein are classified as follows:

a. Qualification inspection (see 4.4).

b. Verification of qualification (see 4.5).

c. Conformance inspection (see 4.6).

d. Periodic inspection (see 4.7)

4.2 Reliability and quality.

4.2.1 QPL system. The manufacturer shall establish and maintain a QPL system as described in 3.3. Evidence of such compliance is a prerequisite for qualification and verification of qualification.

4.2.2 SPC program. A SPC program shall be maintained in accordance with SAE-EIA-557. Evidence of such compliance shall be verified by the qualifying activity of this specification as a prerequisite for qualification and continued qualification.

4.3 Inspections conditions and precautions.

4.3.1 Inspection conditions. Unless otherwise specified herein, all inspections shall be performed in accordance with the test conditions specified in the general requirements of MIL-STD-202.

4.3.2 Precautions. Adequate precautions shall be taken during inspection to prevent condensation of moisture on resistors, except during the moisture resistance temperature cycling tests.

4.4 Qualification inspection. Qualification inspection shall be performed at a laboratory acceptable to the Government (see 6.3).

4.4.1 Sample. The number of sample units comprising a sample of resistors to be submitted for qualification inspection shall be as specified in appendix A to this specification. The sample shall be taken at random from a production run and shall be produced with equipment and procedures normally used in production and which have been subjected to and passed the requirements of group A inspection (see 4.6.3). Qualification shall not be granted if group A inspection requirements are not complied with.

4.4.2 Test routine. Sample units shall be subjected to the qualification inspection specified in table VIII in the order shown. Sample sizes and extent of qualification for characteristics shall be specified in appendix A of this specification.

4.4.3 Defective. Defectives in excess of those allowed in table VIII shall be cause for refusal to grant qualification.

4.4.4 FRL verification (ER only).

4.4.4.1 Procedure. FR qualification shall be in accordance with the general requirements of MIL-STD-690 and the following details:

a. Procedure I: Qualification at the initial FR level. Level M (1.0 percent) of FRSP-60 shall apply. Sample units shall be subjected to the qualification inspection specified in group IV, table VIII (see 4.4.2). Entire life test sample shall be continued on test to 10,000 hours as specified in 3.17.1 upon completion of the 2,000 hour qualification.

b. Procedure II: Extension of qualification to lower FR levels. To extend qualification to the R (0.01 percent), S (0.001 percent), U (0.01 percent) and V (0.001 percent) FR levels, two or more styles of similar construction may be combined.

c. Procedure III: Maintenance of FR level qualification. Maintenance period A of FRSP-10 shall apply. Regardless of the number of production lots produced during this period, the specified number of unit hours shall be accumulated to maintain qualification (see 4.7).

4.5 Verification of qualification. Every 6 months the manufacturer shall provide verification of qualification to the qualifying activity. Continuation of qualification is based on meeting the following requirements.

a. MIL-STD-790 program.

b. Design of resistor has not been modified.

c. Lot rejection for group A (subgroup 2 and subgroup 4) does not exceed 5 percent or one lot, whichever is greater.

d. Lot rejection for group B inspection does not exceed 5 percent or one lot, whichever is greater.

e. Periodic group C inspection requirements are met.

f. FRL's are maintained as required.

g. PPM assessment. (NOTE: Grouping of styles is permitted).

h. Continued qualification to the non-ER level (C) shall be based on continued maintenance of qualification for the ER part (minimum P FRL maintenance).

i. Continued qualification to the space level (T) shall be based on:
(1). Maintaining minimum Established Reliability Failure Rate Level of R, S, U or V.

(2) Maintenance of the test capability and lot control system for testing space level resistors (see A.3.1).

(3). Submission of monthly Group-C subgroup 1 (Life test) samples representative of their production percentage or more.

(4). Reporting of Space-Level Group-C testing for each MIL-STD-690 reporting period as a subgroup (with styles, pieces on test, accumulated hours, etc.).

TABLE VIII. Qualification inspection.

Inspection	Requirement paragraph	Method paragraph	Number of samples	Number of defects allowed
Certification requirements				
Outgassing (space level only)	3.24	4.8.16	-----	----
Group I				
Visual and mechanical inspection	3.1, 3.4, 3.5, 3.5.1 through 3.5.3 inclusive, 3.23, and 3.25	4.8.1	All sample units except group V	0
DC resistance	3.8	4.8.2		
Group II				
Resistance to soldering heat	3.14.1	4.8.8.1		
Resistance to bonding exposure	3.14.2	4.8.8.2	10 highest	
Resistance temperature characteristic	3.16	4.8.10	10 critical	1
Low temperature operation	3.11	4.8.5	10 lowest	
Short time overload	3.12	4.8.6	30	
High temperature exposure	3.13	4.8.7		
Group III				
Resistance to soldering heat	3.14.1	4.8.8.1	10 highest	
Resistance to bonding exposure	3.14.2	4.8.8.2	10 critical	1
Moisture resistance	3.15	4.8.9	10 lowest (30)	
Group IV				
Subgroup 1 (ER qualification)				
Life	3.17	4.8.11	34 highest 34 critical 34 lowest	1
Group V				
Solderability 1/	3.18	4.8.12	10 any value	1
Group VI				
Solderable mounting integrity 1/	3.19.1	4.8.13.1	10 any value	
Bondable mounting integrity 2/	3.19.2	4.8.13.2	10 any value	1
Wire bonding integrity 3/	3.19.3	4.8.13.3	10 any value (30)	
Group VII				
Resistance to solvents 4/	3.20	4.8.14	10 any value 10 any value (20)	0
Marking legibility test (laser marking) 5/	3.21.1	4.8.15		
Group VIII (space level only)				
Thermal shock (100 cycles)	3.9.2	4.8.3	10 highest 10 critical 10 lowest (30)	0

1/ Applicable to termination B.
2/ Applicable to termination C, D, G, T and U.
3/ Applicable to termination W.
4/ Test applicable for parts marked using methods other than laser marking.
5/ Test applicable for laser marked parts.

4.6 Conformance inspection.

4.6.1 Inspection of product for delivery.

4.6.1.1 Non-ER resistors. The manufacturer's inspection system shall be used for preparation for delivery.

4.6.1.2 ER resistors. Inspection of product for delivery shall consist of group A and group B inspections. Group B inspection for preparation of delivery is not required when the qualifying activity has allowed group B testing to be performed annually (see table XI-1). Group B inspection shall be performed on inspection lot basis for product level M, P, R, and S and production lot for product level T, U, and V.

4.6.1.3 Space level. Inspection of product for delivery shall begin with "R", "S", "U", or "V" level product then upscreened to space level by resubmitting them to the entire group A and B inspection, and shall be performed on a production lot basis. Test deletion or reduction is not allowed for space level product.

4.6.2 Inspection and production lot.

4.6.2.1 Inspection lot. An inspection lot shall consist of resistors of the same style, characteristic, and termination type and manufactured under essentially the same process and conditions with the same basic materials and offered for inspection at one time. Non-ER, ER, and space level lots shall be kept separate.

4.6.2.2 Production lot (ER and space level only). A production lot shall consist of all resistors of the same style, nominal resistance value, resistance tolerance, resistance temperature characteristic, termination material manufactured and tested as a group using the same material, processes, specifications and procedures . Lot identity shall be maintained throughout the manufacturing cycle. The deposition/metallization shall be restricted to substrates produced for a single resistor style; the substrates shall be processed in a single continuous metallization run on the same equipment and the raw material used in the metallization process shall be from the same raw material lot. Non-ER, ER, and space level lots shall be kept separate.

4.6.2.3 Optional production lot control (characteristic E and characteristic K only). A manufacturer that has a single design that meets all the requirements of both characteristic E and characteristic K may, with qualifying activity approval, use a different control system. All products shall be processed as E characteristic but may be subsequently supplied as K characteristic provided the manufacturer marks the unit packages accordingly and performs all other tests for characteristic K.

4.6.3 In-process inspection and quality conformance inspection.

4.6.3.1 In-process inspection. Each thin film production lot shall have an in-process precap visual inspection and shall be in accordance with table IX.

TABLE IX. In-process inspection.

Inspection	Requirement paragraph	Test method paragraph	Sample size
Precap visual inspection (thin film only)	3.23	4.8.1	100 percent

4.6.3.2 Group A inspection.

4.6.3.2.1 Non-ER resistors. The manufacturer shall establish and maintain an inspection system to verify that resistors meet dc resistance, visual/mechanical, and solderability requirements. In-line or process controls may be part of such a system. The inspection system shall also include criteria for lot rejection and corrective actions. The inspection system shall be verified under the overall MIL-STD-790 QPL system. NOTE: Since the non-ER (C level) is the ER design without the mandatory conformance inspection and FRL assessment, this product is still expected meet the environmental qualification type requirements (e.g., resistance to soldering heat, moisture resistance, high temperature exposure, etc.).

4.6.3.2.2 ER and space level resistors. Group A inspection shall consist of the examinations and tests specified in table IX-1.

4.6.3.2.2.1 Subgroup 1 test (precap visual). The subgroup 1 test shall be performed on a production lot basis. Thirteen samples shall be subjected to subgroup 1. In the event of one or more failures, the lot shall be rejected.

4.6.3.2.2.1.1 Rejected lots. In the event of one or more defects and the production lot is rejected, the rejected production lot(s) shall be submitted to a 100 percent precap visual inspection as specified in 3.23. Resistors that pass precap visual inspection are available to continue group A testing.

4.6.3.2.2.2 Subgroup 2 tests. Subgroup 2 tests shall be performed on a production lot basis on 100 percent of the product supplied under this specification. Resistors that are out of resistance tolerance, or which experience a change in resistance greater than that permitted for the tests of this subgroup, shall be removed from the lot. Lots having more than 5 percent total rejects due to exceeding the specified resistance tolerance change limit shall not be furnished on contracts.

4.6.3.2.2.2.1 Manufacturer's production inspection. If the manufacturer performs tests similar to those specified in subgroup 2, table IX-1, as the final step of his production process, group A, subgroup 2 inspection may be waived. Authority to waive the subgroup 2 inspection shall be granted by the qualifying activity only. The following criteria must be complied with:

a. Tests conducted by the manufacturer during production shall be clearly identical to or more stringent than those specified for subgroup 2. Test conditions shall be equal to or more stringent than those specified for subgroup 2 tests.

b. Manufacturer subjects 100 percent of the product supplied under this specification to his production tests.

c. The parameters measured and the failure criteria shall be the same as, or more stringent than, those specified herein.

d. The lot rejection criteria are the same as, or more stringent than, those specified herein.

e. Once approved, the manufacturer shall not change the test procedures or criteria without prior notification to and concurrence from the qualifying activity.

TABLE IX-1. Group A inspection (ER and space level).

Inspection	Requirement paragraph	Method paragraph	Sampling procedure
Subgroup 1			
Precap visual inspection 1/	3.23	4.8.1	4.6.3.2.2.1
Subgroup 2			
Thermal shock 2/	3.9	4.8.3	
Power conditioning (space level only) 7/	3.10	4.8.4	4.6.3.2.2.2
DC resistance	3.8	4.8.2	
Subgroup 3			
Visual inspection	3.1, 3.4, 3.5 through 3.5.3 inclusive, and 3.23	4.8.1	4.6.3.2.2.3
Subgroup 4			
Solderability 3/	3.18	4.8.12	4.6.3.2.2.4
Subgroup 5 4/			
Resistance to solvents 5/	3.20	4.8.14	4.6.3.2.2.5
Marking legibility 6/	3.21	4.8.15	

1/ Precap visual inspection shall be performed when the resistance element cannot be inspected after passivation/glassivation in subgroup 3.

2/ If the manufacturer can demonstrate that the FRL of the parts can be maintained without performing the thermal shock screen, this test, with approval of the preparing activity and qualifying activity, may be deleted. If the design, material, construction, or processing of the part is changed, or if there are any quality problems or failures, the qualifying activity may require resumption of the test. As a minimum, for initial consideration of this option, the manufacturer shall demonstrate and validate using data equivalent to M FR qualification, that the test does not affect the FR of the resistor. Upon deletion of the test, the manufacturer must continue to maintain their existing FRL based on testing of parts without the thermal shock screening. (NOTE: Not applicable to space level.)

3/ The manufacturer may request the deletion of the Subgroup 4 solderability test, provided an in-line or process control system for assessing and assuring the solderability of terminations can be validated and approved by the qualifying activity. Deletion of the test does not relieve the manufacturer from meeting this test requirement in case of dispute. If the design, material, construction, or processing of the part is changed or if there are any quality problems, the qualifying activity may require resumption of the test. (NOTE: Not applicable to space level.)

4/ If the manufacturer can demonstrate that these tests have been performed five consecutive times with zero failures, the frequency of these tests, with the approval of the qualifying activity, can be performed on a annual basis. If the design, material, construction, or processing of the part is changed or, if there are any quality problems or failures, the qualifying activity may require resumption of the original test frequency. (NOTE: Not applicable to space level.)

5/ Test applicable for parts marked using methods other than laser marking.

6/ Test applicable for laser marked parts.

7/ For W termination only. An alternate test of high temperature exposure after the thermal shock test may be substituted for power conditioning (see 3.10.1).

4.6.3.2.2.3 Subgroup 3 (visual inspection). The subgroup 3 test shall be performed on an inspection lot basis for ER parts and a production lot basis for space level parts. A sample of parts shall be randomly selected in accordance with table X. If one or more defects are found, the lot shall be reworked or screened and defectives removed. After reworking or screening and removal of defectives, a new sample of parts shall be randomly selected in accordance with table X. If one or more defects are found in this second sample for the same quality characteristic, the lot shall be rejected and shall not be supplied to this specification.

4.6.3.2.2.4 Subgroup 4 (solderability) test. The subgroup 4 test shall be performed on an inspection lot basis for ER parts and on a production lot basis for space level parts. A sample shall be randomly selected from each lot in accordance with table X. As an option, the manufacturer may use electrical rejects from the subgroup 2 tests for all or part of the sample. If there are one or more defects, the lot shall be considered to have failed.

4.6.3.2.2.4.1 Rejected lots. In the event of one or more defects, the inspection lot is rejected. Each production lot that was used to form the failed inspection lot shall be individually submitted to the solderability test as required in 3.18. An additional sample shall be randomly selected from each production lot in accordance with table X. If the lot fails this solderability test, the lot may be reworked and retested. Any individual production lot that fails the solderability retest shall be considered to have failed and that lot will not be supplied to the requirements of the specification.

TABLE X. Sampling plans for subgroup 3 and subgroup 4 and ppm assessment.

Lot size	Sample size for subgroup 3	Sample size for subgroup 4	Sample size for ppm assessment
1 to 5	100%	100%	100%
6 to 13	100%	5	100%
14 to 125	13	5	100%
126 to 150	13	5	125
151 to 280	20	5	125
281 to 500	29	5	125
501 to 1,200	34	5	125
1,201 to 3,200	42	5	125
3,201 to 10,000	50	8	125
10,001 to 35,000	60	13	294
35,001 to 150,000	74	20	294
150,001 to 500,000	90	20	345
500,001 and over	102	20	435

4.6.3.2.2.4.2 Disposition of samples. The solderability test is considered a destructive test and samples submitted to the solderability test shall not be supplied on the contract.

4.6.3.2.2.5 Subgroup 5. Six samples shall be selected randomly from each inspection lot and subjected to the subgroup 5 tests. The manufacturer may use electrical rejects from the subgroup 2 screening tests for all or part of the samples to be used for the subgroup 5 testing. If there are one or more defects, the lot shall be considered to have failed.

4.6.3.2.2.5.1 Rejected lots. In the event of one or more defects, the inspection lot is rejected. Each production lot that was used to form the failed inspection lot shall be individually submitted to the subgroup 5 test as required in 3.20 or 3.21. An additional eight samples shall be randomly selected from each production lot and shall be tested. If there is one or more defects in the production lot sample, that production lot shall be considered to have failed and that product will not be supplied to the requirements of this specification. Individual production lots that pass the minimum marking test are available for shipment.

4.6.4 PPM assessment (non-ER and ER). The manufacturer shall establish and maintain a system for assessing the average outgoing quality in ppm of lots supplied to this specification. This ppm assessment should be based on inspections performed on each inspection lot to verify that resistors meet dc resistance and tolerance requirements (i.e., ppm-2). For ER resistors, this inspection shall occur after the group A, subgroup 2, 100 percent screens have been completed. In the event of one or more failures, the lot shall be rejected.

4.6.4.1 Sampling plans. Minimum sample sizes for inspection lots shall be selected in accordance with table X. For non-ER resistors, the sampling system and plan used for the group A inspection (see 4.6.3.1) may be the basis for assessing ppm.

4.6.4.2 Rejected lots. Any rejected inspection lot shall be segregated from new lots and those lots which have passed the ppm assessment. The manufacturer has two options on a rejected inspection lot.

Option 1:

a. The manufacturers can submit individual production lots that do not contain the samples that failed the inspection lot test to the ppm assessment. A sample from these production lots shall be selected in accordance with table X. Those production lots that have zero defects are available for shipment. Data from these production lots shall also be used for ppm calculations.

b. For those production lots that contain the samples that failed the inspection lot test, the production lot may be rescreened for the quality characteristics found defective in the sample and any defects removed. A second sample in accordance with table X shall be selected. If one or more defects are found, this lot is rejected and shall not be supplied to the specification.

Option 2:

a. A rejected inspection lot may be rescreened for the quality characteristics found defective in the inspection lot sample and any defects removed. A new second sample in accordance with table X shall be randomly selected. If one or more defects are found, this lot is rejected and shall not be supplied to this specification.

b. A rejected lot may be rescreened for the quality characteristics found defective in the sample and any defects removed. A new second sample shall be randomly selected. If one or more defects are found, this lot is rejected and shall not be supplied to the specification.

4.6.4.3 PPM calculations. PPM calculations shall be based on the accumulated results of the initial sample. Calculations and exclusions shall be in accordance with SAE-EIA-554-1. (NOTE: PPM calculations shall not be based on the second sample submission for a rejected lot as described in 4.6.4.2).

4.6.5 Group B inspection (ER and space level only). Group B inspection shall consist of the inspections specified in table XI in the order shown, and shall be performed on samples from lots which have been subjected to and have passed the group A inspection. Group B inspection shall be performed on monthly inspection lot basis for product level M, P, R, and S and production lot for product level T, U, and V.

4.6.5.1 Sampling plan.

4.6.5.2 Subgroup 1. Twenty sample units shall be randomly selected for test. If one or more defects are found, the lot shall be reworked or screened and defectives removed. After reworking or screening and removal of defectives, a new sample of 20 parts shall be randomly selected. If one or more defects are found in this second sample, the lot shall be rejected and shall not be supplied to this specification.

4.6.5.3 Subgroup 2. Ten sample units shall be randomly selected for test. If one or more defects are found, the lot shall be reworked or screened and defectives removed. After reworking or screening and removal of defectives, a new sample of ten parts shall be randomly selected. If one or more defects are found in this second sample, the lot shall be rejected and shall not be supplied to this specification.

4.6.5.3.1 Disposition of sample units. Sample units which have been subjected to group B inspection shall not be delivered on the contract or order.

TABLE XI. Group B inspection (ER and space level).

Inspection	Requirement paragraph	Method paragraph	Number of samples
Monthly			
Subgroup 1 1/			
Resistance temperature characteristic	3.16	4.8.10	
Short time overload	3.12	4.8.6	20 samples
Subgroup 2 2/			
Solder mounting integrity 3/	3.19.1	4.8.13.1	10 samples
Bondable mounting integrity 4/	3.19.2	4.8.13.2	10 samples
Wire bonding integrity 5/	3.19.3	4.8.13.3	10 samples

1/ If the manufacturer can demonstrate that these tests have been performed five consecutive times with zero failures, the frequency of these tests, with the approval of the qualifying activity can be performed on an annual basis. If the design, material, construction, or processing of the part is changed or, if there are any quality problems or failures, the qualifying activity may require resumption of the original test frequency. (NOTE: Not applicable to T, U and V failure rate levels).

2/ If the manufacturer can demonstrate that this test has been performed five consecutive times with zero failures, this test, with the approval of the qualifying activity, can be deleted. The manufacturer, however, shall perform this test every three years after the deletion as part of long term design verification. If the design, material, construction, or processing of the part is changed or, if there are any quality problems, the qualifying activity may require resumption of the specified testing. Deletion of testing does not relieve the manufacturer from meeting the test requirement in case of dispute. (NOTE: Not applicable to T, U and V failure rate levels).

3/ Applicable to termination B.

4/ Applicable to terminations C, D, G, T, and U.

5/ Applicable to termination W.

4.7 Periodic group C inspection (ER only). Group C inspection shall consist of the tests specified in table XII, in the order shown. Group C inspection shall be made on sample units selected from lots which have passed group A and group B inspection. Group C samples shall be representative of production. The allowable number of defectives shall be as indicated in table XII.

4.7.1 Sampling plan. If more than 1,000 resistors of any style or style grouping are produced over the maintenance period, the group C tests shall be performed as specified. If the production rate is less than 1,000 resistors for any style or style grouping over the maintenance period, then the monthly or quarterly group C inspection may be postponed until at least 1,000 resistors of that style or grouping are produced (except for the monthly life test). In any case, the monthly tests shall be performed at least once every 3 months. The quarterly tests shall be performed at least every 6 months. This requirement is waived if the manufacturer has obtained a reduced inspection status through the qualifying activity.

4.7.1.1 Monthly (subgroup 1). Samples shall be accumulated from ER and T level lots, and placed on extended life test in accordance with 4.8.11 once a month for the full 10,000 hour life test. A sufficient number of samples shall be selected by the manufacturer so that the maintenance of FR requirements complies with the specified maintenance period. Samples shall be representative of production of individual styles, characteristics, and termination's in the maintenance period. The manufacturer has the option, with qualifying activity approval, of selecting samples from RTC groups versus individual characteristics (group I: E or H; group II: K, L or M). As far as practical, the manufacturer shall select the resistance values so that all resistance decades produced during the maintenance period are represented.

4.7.1.2 Monthly (subgroup 2). Subgroup 2 tests shall be performed on a sample size of 30 units of each style, characteristic, and termination with one defective allowed for each group of 30.

4.7.2 Quarterly.

4.7.2.1 Subgroup 1. Every 3 months, 30 units of each style, characteristic, and termination material (any resistance value) shall be subjected to quarterly tests specified in table XII, in the order shown.

4.7.2.2 Subgroup 2. Every 3 months, 30 units of each style, characteristic, and termination material (any resistance value) shall be subjected to quarterly tests specified in table XII.

4.7.3 Noncompliance. If a sample fails to pass group C inspection, the contractor shall take corrective action on the materials or processes, or both, as warranted, and on all units of product which can be corrected and which were manufactured under essentially the same conditions, with essentially the same materials, processes, etc., and which are considered subject to the same failure. Acceptance of the product shall be discontinued until corrective action, acceptable to the Government, has been taken. After the corrective action has been taken, group C inspection shall be repeated on additional sample units (all inspection, or the inspection which the original sample failed, at the option of the Government). Group A and group B inspections may be reinstituted; however, final acceptance shall be withheld until group C reinspection has shown that the corrective action was successful

TABLE XII. Group C inspection.

Inspection	Requirement paragraph	Method paragraph	Number of samples	Number of defects allowed
Monthly Subgroup 1 Life (ER)	3.17.2	4.8.11	4.7.1.1	4.7.1.1
Subgroup 2 1/ Thermal shock Low temperature operation	3.9 3.11	4.8.3 4.8.5	30	1
Quarterly Subgroup 1 1/ Resistance to soldering heat Resistance to bonding exposure Moisture resistance	3.14.1 3.14.2 3.15	4.8.8.1 4.8.8.2 4.8.9	30	1
Subgroup 2 1/ High temperature exposure	3.13	4.8.7	30	1

1/ If the manufacturer can demonstrate that these tests have been performed five consecutive times with zero failures, the frequency of these tests, with the approval of the qualifying activity, can be performed on a annual basis. If the design, material, construction, or processing of the part is changed or, if there are any quality problems or failures, the qualifying activity may require resumption of the original test frequency. (NOTE: Not applicable to space level)

4.8 Methods of inspection.

4.8.1 Visual and mechanical inspection and chip mounting.

4.8.1.1 Visual and mechanical inspection. Unless otherwise specified, resistors shall be examined under 30X to 60X magnification. In case of conflict 30X will be the referee power, unless otherwise specified, to verify that the materials, design, construction, physical dimensions, and workmanship are in accordance with the applicable requirements (see 3.1, 3.4, 3.5, 3.5.1 through 3.5.3 inclusive, 3.23 and Appendix B).

4.8.1.2 Chip mounting procedures. When specified herein, the chip resistor shall be mounted on a test board as described in 4.8.1.3. For those test procedures where mounting requirements are unspecified, the chip resistors may be tested unmounted using pressure contacts.

4.8.1.3 Specified mounting. When specified in the test procedure, the chip resistor shall be mounted on a test board as specified on figure 3. The test board material shall be such that it shall not be the cause of, nor contribute to, any failure of a chip resistor in any of the tests for which it may be used. The test board shall be prepared with metallized surface land areas of proper spacing so that a test board surface area of at least four times the resistor chip surface area is provided for each resistor chip mounted. The metallized surface land areas shall be designed in a pattern to accommodate a number of resistor chips. The metallization material shall be compatible with the bonding technique to be employed and the material used on the chip termination. The method of chip mounting for the different termination materials shall be as follows:

a. Termination B (solderable). Termination B chip resistors shall be mounted on a fiberglass test board by soldering the chip terminations directly to the test board metallized land areas in the following manner:

   (1) Solder and soldering flux shall be of such a quality as to enable the chip resistors to meet all the requirements of this specification and shall be applied to the terminations of each chip of code letter B (see 1.2.4).

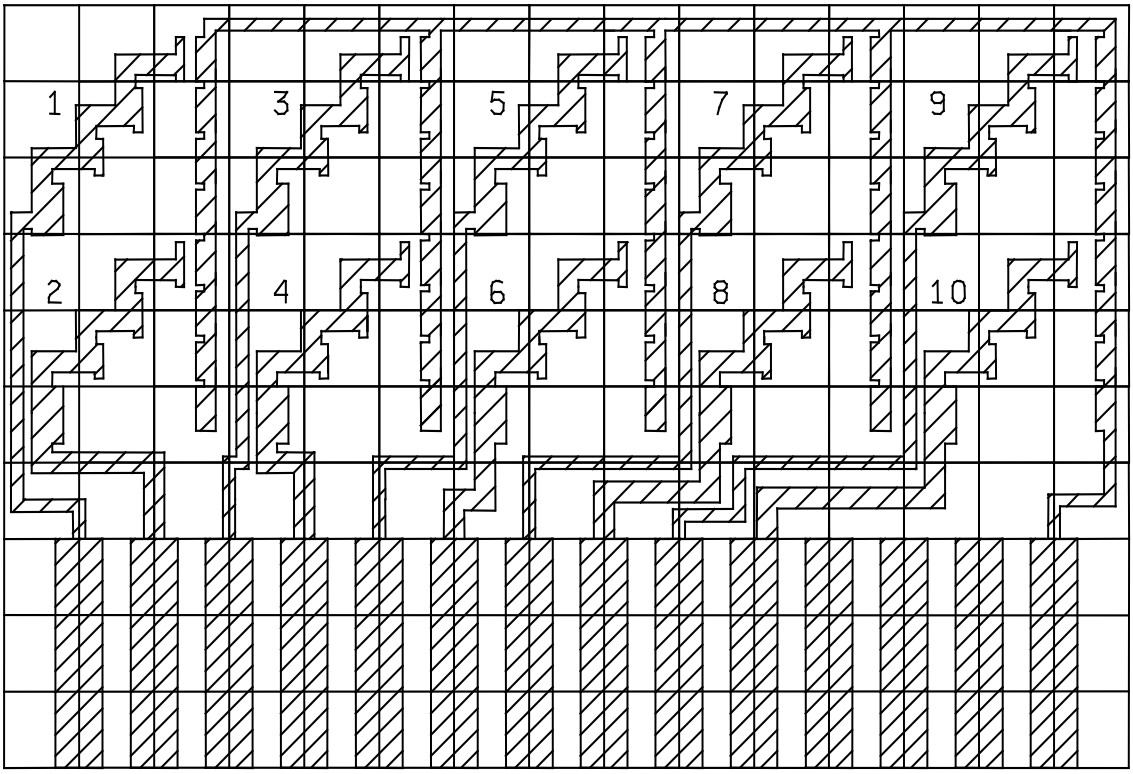
   (2) All chips shall be placed across the metallized land areas of the test board with contact between the chip termination's and board land areas only. The use of adhesive to keep chips in place during mounting operation is allowable except for preparation of solder mounting integrity test pieces.

   (3) For resistance to soldering heat, the test board with all chips in position shall be placed on a heat transfer unit (molten solder, hot plate, tunnel oven, etc.) with the temperature transitioned to 245°C ±5°C. The chips shall remain at 245°C ±5°C until the solder melts and reflows forming a homogenous solder bond.

   (4) For load life, the test board with all chips in position shall be placed on a heat transfer unit (molten solder, hot plate, tunnel oven, etc.) with suitable time and temperature to assure proper reflow mounting.

b. Terminations G, U, T, C, and D (epoxy bondable). As an alternative to 4.8.1.3.a (1), chip resistors may be mechanically attached to the ceramic test board with type 2 epoxy approved by the qualifying activity. The epoxy shall be cured at a minimum temperature of 150°C. The minimum curing time shall be 30 minutes.

c. Termination "W" (wire bondable). Chip resistors with wire bondable termination's shall be mechanically attached to the test board and electrically connected by wire bonding flying lead interconnections between the chip termination and the ceramic test board metallized land areas. The interconnecting lead shall be .001 inch (0.03 mm) in diameter gold wire. The chip shall be mechanically or adhesively mounted by any procedure which will not be the cause of or contribute to any failures of the chip resistor in any test.



NOTES:

1. Suggested ceramic test board (e.g., 96 percent alumina): 1.000 inch (25.40 mm) x 1.500 inch (38.10 mm) x 0.025 inch (0.64 mm) thick.
2. Suggested fiberglass test board (e.g., G30 or FR-4 glass epoxy): 1.000 inch (25.40 mm) x 1.500 inch (38.10 mm) x .0625 inch thick (1.5875 mm).
3. The contacts fit a printed circuit board connector with .100 inch (2.54 mm) in contact center.
4. Short lead wire may be soldered on and it will then fit a microcircuit connector, or test lead wires may soldered on for direct measurement.
5. Small grid square are 0.100 inch (0.25 mm).
6. A larger test board, to suitable scale, may be used to accommodate additional test samples or additional style/size configurations.

FIGURE 3. Suggested test board.

4.8.1.3.1 Fiberglass base board. Fiberglass base boards can be FR-4, G-10, G-30, or equivalent. When specified, a fiberglass test board with copper lamination shall be used for testing. The copper lamination shall be 70 micrometers copper (2 oz.) thickness (maximum).

4.8.2 DC resistance. The dc resistance shall be measured in accordance with method 303 of MIL-STD-202. The following details and exceptions shall apply:

a. Measuring apparatus: Different types of measuring test equipment (multimeters, bridges, or equivalent) are permitted to be used on the initial and final readings of this test, provided the equipment is the same type, model, or if it can be shown that the performance of the equipment is equivalent or better.

b. Test voltage for bridges: Measurements of resistance shall be made by using the test voltages up to the maximum values specified in table XIII. The test voltage chosen, whether it is the maximum or a lower voltage which would still provide the sensitivity required, shall be applied across the terminals of the resistor. This same voltage shall be used whenever a subsequent resistance measurement was made.

c. Measurement energy for electronic test equipment: The measurement energy applied to the unit under test shall not exceed 10 percent of the 25°C rated wattage times 1 second.

d. Temperature: The dc resistance test specified in group I of table VIII shall be performed at 25°C ±2°C. For all other tests, unless otherwise specified herein, the temperature at which subsequent and final resistance measurements are made in each test shall be within ±2°C of the temperature at which the initial resistance measurement was made.

TABLE XIII. Standard dc resistance test voltages.

Nominal resistance	Maximum test voltage			
	10 to 24 milliwatts	25 to 99 milliwatts	100 to 225 milliwatts	226 to 1,000 milliwatts
ohms	Volts	Volts	Volts	Volts
1 to 9.88	0.2	0.3	0.7	1.0
10 to 98.8	0.3	0.3	1.0	1.0
100 to 988	1.0	1.0	1.0	3.0
1,000 to 9,880	3.0	3.0	3.0	10.0
10,000 to 98,880	10.0	10.0	10.0	30.0
100,000 or higher	30.0	30.0	30.0	100.0

4.8.3 Thermal shock (see 3.9). Resistors shall be tested in accordance with method 107 of MIL-STD-202. The following details and exceptions apply:

a. Mounting: Resistors shall not be mounted. Resistors may be placed in metal baskets, vials, or other apparatus as long as resistors are subjected to the specified temperature extremes. (For group C inspection only, as an option to the manufacturers, resistors may be mounted or unmounted.)

b. Measurement before cycling:

(1) Qualification test: DC resistance shall be measured as specified in 4.8.2, except at 25°C ±5°C. The dc resistance shall be within the specified resistance tolerance of the nominal resistance value.

(2) Group C test: DC resistance shall be measured as specified in 4.8.2.

c. Test condition F (except temperatures shall be 150°C +10ºC, -0ºC and -65°C +0ºC, -10°C).

d. Measurement after cycling:

(1) Qualification and group A tests: After stabilization at room temperature, the dc resistance shall again be measured as specified in 4.8.2, except at 25°C ±5°C.

(2) Group C test (not applicable for space level): After stabilization at room temperature, the dc resistance shall again be measured as specified in 4.8.2. Following the test, the resistors shall be examined for evidence of mechanical damage.

4.8.4 Power conditioning (space level only) (see 3.10). Chip resistors shall be tested in accordance with method 108 of MIL-STD-202. The following details and exceptions shall apply:

a. Test temperature and tolerance: 70°C +5°C, -0°C.

b. Initial measurements: Measurements may be made inside or outside the chamber.

(1) Inside chamber: When measurements are to be made inside the chamber, the initial dc resistance shall be measured, at the applicable test temperature, after a thirty minute +90 minute, -15 minute stabilization period and within 8 hours of exposure of the chip resistors to the test temperature. This initial measurement shall be used as the reference temperature for all subsequent measurements under the same condition.

(2) Outside chamber: When measurements are to be made outside the chamber, the initial dc resistance shall be measured at room temperature. This measurement shall be used as the reference temperature for all subsequent measurements under the same condition.

c. Operating condition: A dc voltage or filtered or nonfiltered full-wave rectified ac voltage shall be applied to the chip resistor intermittently, one and one-half hours “on” and one-half hour “off”, for 100 hours ±4 hours and at the test temperature. During the “on” cycle, the voltage shall be regulated and controlled to maintain ±5 percent of the required test voltage. Unless otherwise specified (see 3.1), power applied shall be one and one-half times rated power not to exceed maximum voltage for the style. At no time during the test shall the resistor film temperature exceed 150°C. Adjust the ambient temperature, when necessary, in order to accomplish this.

d. Measurements after test: Following a thirty minute minimum stabilization period, dc resistance shall be measured as specified in 4.8.2.

e. Inspection after test: Chip resistors shall be inspected in accordance with 4.8.1.1.

4.8.5 Low temperature operation (see 3.11). A dc resistance measurement shall be made as specified in 4.8.2, mounted on a test board as specified in 4.8.1.3. The resistors shall be placed in a cold chamber maintained at -65°C +0°C, -5°C. After stabilization at this temperature, full rated continuous working voltage as specified in 3.7 shall be applied for 45 minutes +5 minutes, -0 minutes. Fifteen minutes +5 minutes, -0 minutes after the removal of the voltage, the resistors shall be removed from the chamber and maintained at a temperature of 25°C ±5°C until stabilized; the dc resistance shall be measured as specified in 4.8.2. Resistors shall be examined for evidence of mechanical damage.

4.8.6 Short time overload (see 3.12). The dc resistance shall be measured as specified in 4.8.2 and mounted on a test board as specified in 4.8.1.3. A dc test potential, 2.5 times the rated continuous working voltage but not exceeding twice the maximum voltage (see 3.1), shall be applied for 5 seconds to the resistor under the following conditions:

a. Resistors on test board shall be mounted so that the larger space of the resistor is on a horizontal plane.

b. In still air, with no circulation other than that created by the heat of the resistors being operated.

The resistors shall be stabilized at 25°C ±3°C after which the dc resistance shall be measured as specified. Resistors shall be examined for evidence of arcing, burning, and charring.

4.8.7 High temperature exposure (see 3.13). Resistors shall be mounted on a test board as specified in 4.8.1.3 and the dc resistance shall be measured as specified in 4.8.2. The resistors shall then be subjected to a continuous temperature of 150°C ±5°C for a period of 100 hours ±4 hours (125°C ±5°C for space level power conditioning alternate testing W termination), in a test chamber with forced air circulation. The resistors shall be stabilized at 25°C ±3°C after which the dc resistance shall be measured as specified. The change in resistance shall not exceed the value specified in table I.

4.8.8 Resistance to solder heat and resistance to bonding exposure.

4.8.8.1 Resistance to soldering heat (termination B) (see 3.14.1). Resistors shall be tested in accordance with method 210 of MIL-STD-202. The following details and exceptions shall apply:

a. Measurement before test: DC resistance shall be measured as specified in 4.8.2.

b. Mounting: Resistors shall be mounted on a fiberglass test board as specified in 4.8.1.3.a(3). This mounting procedure shall be considered one heat cycle.

c. Second heat cycle: Test condition J, except this is the last heat cycle. (NOTE: When a hot plate is used, the temperature shall be 245°C ±5°C for 60 seconds ±5 seconds and the temperature ramp and emersion/immersion rate does not apply.

d. Measurement after test: After completion of the cleaning process and following a stabilization period at room temperature the dc resistance shall be measured as specified in 4.8.2. The change in resistance shall not exceed the value specified in table I.

e. Examination after test: Resistors shall be examined for evidence of mechanical damage.

4.8.8.2 Resistance to bonding exposure (terminations W, G, U, T, C, and D) (see 3.14.2). The dc resistance of the chip resistor shall be measured as specified in 4.8.2. The chip resistor shall be mounted on a ceramic test board in accordance with 4.8.1.3. The test board, with resistors mounted, shall be stabilized at room temperature after which the dc resistance shall again be measured as specified in 4.8.2. The change in resistance shall not exceed the value specified in table I.

4.8.9 Moisture resistance (see 3.15). Resistors shall be tested in accordance with method 106 of MIL-STD-202. The following details and exceptions shall apply:

a. Mounting: Chip resistor sample units shall be mounted on a test board as specified in 4.8.1.3.

b. Initial measurement: Immediately following the initial conditioning period, dc resistance of each chip on the test board shall be measured as specified in 4.8.2.

c. Polarization and loading voltage: No voltage shall be applied.

d. Subcycle: Step 7b shall not be applicable. Step 7a shall be performed during any five of the first nine cycles only.

e. Measurements at high humidity: None.

f. Final measurements: Upon completion of step 6 of the final cycle, the resistors shall be removed from the chamber and air dried for 15 minutes to 120 minutes. The dc resistance shall then be measured in accordance with 4.8.2.

g. Examination after test: Resistors shall be examined for evidence of electrical and mechanical damage.

4.8.10 Resistance temperature characteristic (see 3.16). Resistors shall be tested in accordance with method 304 of MIL-STD-202. The following details and exceptions shall apply:

a. Reference temperature: Room ambient temperature.

b. Test temperature: In accordance with table XIV.

c. Accuracy of temperature measurement: Resistors shall be maintained for thirty minutes +90 minutes, -15 minutes within 3°C at each of the test temperatures listed in table XIV. This tolerance shall be maintained on the established test temperatures.

d. Mounting: Resistors shall be mounted on a test board as specified in 4.8.1.3.

e. The dc resistance shall be measured in accordance with 4.8.2.

As an option, the manufacturer may develop a control procedure for minimum stabilization times required for RTC testing. This procedure shall detail specific time elements required to reach thermal and electrical stability for specific part designs. Upon approval by the qualifying activity, the manufacturer may use this procedure for minimum stabilization times for RTC testing.

TABLE XIV. Resistance temperature characteristic.

Sequence	Temperature 1/
	°C
1	2/ 25 ±3
2	-55 ±3
3	2/ 25 ±3
4	125 ±3

1/ At the option of the manufacturer, the reverse sequence may be as follows:

1 - 1/ 25°C ±3°C
2 - 125°C ±3°C
3 - 1/ 25°C ±3°C
4 - -55°C ±3°C

2/ This temperature shall be considered the reference temperature for each of the succeeding temperatures.

4.8.11 Life test (ER level system) (see 3.17). Resistors shall be tested in accordance with method 108 of MIL-STD-202. The following details and exceptions shall apply:

a. Method of mounting: Termination B chip resistor sample units shall be mounted on a fiberglass test board as specified in 4.8.1.3. Terminations W, G, U, T, C, and D shall be mounted on ceramic test boards as specified in 4.8.1.3.

b. Test temperature and tolerance: 70°C ±5°C.

c. Initial resistance measurement of mounted resistors: Measurements may be made inside or outside the chamber. The dc resistance shall be measured in accordance with 4.8.2.

(1) Inside chamber: When measurements are to be made inside the chamber, the initial dc resistance shall be measured after mounting at the applicable test temperature, after a thirty minute +90 minute, -15 minute stabilization period, and within 8 hours of exposure of the resistors to the test temperature. This initial measurement shall be used as the reference dc resistance for all subsequent measurements under the same condition.

(2) Outside chamber: When measurements are to be made outside the chamber, the initial dc resistance shall be measured after mounting at room temperature. This initial measurement shall be used as the reference dc resistance for all subsequent measurements under the same condition.

d. Operating conditions: Rated dc continuous working voltage, or filtered or non-filtered full wave rectified ac voltage, shall be applied intermittently, 90 minutes “on” and 30 minutes “off”, for the applicable number of hours (see 4.8.11f(2)) and at the applicable test temperature. "On time" shall be three quarters of the total elapsed time. During the "on" cycle, the voltage shall be regulated and controlled to maintain ±5 percent of the rated continuous working voltage.

e. Test condition: Two thousand hours elapsed time for qualification inspection (ER only) with all samples continued to 10,000 hours. Ten thousand hours for FRL inspection group C.

f. Measurements during test: The dc resistance shall be measured in accordance with 4.8.2.

(1) Qualification inspection: DC resistance shall be measured at the end of the 30 minutes “off” periods after 250 hours +72 hours, -24 hours; 500 hours +72 hours, -24 hours; 1,000 hours +72 hours, -24 hours; and 2,000 hours +96 hours, -24 hours have elapsed.

(2) Extended life testing: DC resistance shall be measured at the end of the 30 minutes “off” periods after 250 hours +72 hours, -24 hours; 500 hours +72 hours, -24 hours, 1,000 hours +72 hours, -24 hours; and 2,000 hours +96 hours, -24 hours, and every 2,000 hours +96 hours, -24 hours thereafter until the required 10,000 +120, -0 hours have elapsed. Measurements shall be made as near as possible to the specified time but may be adjusted so that measurements need not be made during other than normal workdays.

(3) Measurements outside of the chamber: When measurements are made outside the chamber, resistors shall be outside of the chamber, for a minimum of 45 minutes and stabilized before measurement.

g. Examination after test: Resistors shall be examined for evidence of mechanical damage.

4.8.12 Solderability (applicable to termination B) (see 3.18). Resistors shall be tested in accordance with method 208 of MIL-STD-202. Both end terminations shall be immersed completely one at a time or both at the same time by dipping the entire chip in the solder pot. The following details and exceptions shall apply:

a. Apparatus:

(1) A solder pot capable of keeping the solder temperature to ±5°C of set point.

(2) A device to keep the specimen submerged in solder for the required time.

(3) Optical equipment capable of 30X magnification.

(4) A laboratory beaker or appropriate laboratory apparatus that is capable of:

(a) Supporting a nonmetallic device.

(b) Maintaining the test specimens at a distance of 1.50 inches (38.1 mm) to 2.50 inches (63.5 mm) from the surface of the boiling deionized water (DI) or distilled water while, at the same time, exposing them to the full flow of steam generated.

b. The requirement for standard solderable wire application shall not apply.

c. The immersion and emersion rates shall not apply.

d. The specimen shall be totally submerged for at least 5 seconds.

4.8.13 Mounting integrity (see 3.19).

4.8.13.1 Solder mounting integrity (termination B). The resistor chips shall be prepared as specified in 4.8.1.3a. A force shall be applied to all solderable units. The force shall be applied to the edge of the chip as shown on figure 4 for a minimum of 30 seconds. The resistor shall be examined for evidence of mechanical damage. The pusher width shall be a minimum of 30 percent of the length and the maximum width shall be 70 percent of the chip length. The applied force shall be as specified in table XV.

TABLE XV. Solder mounting integrity.

STYLE	FORCE APPLIED (kilograms)
RM0302 and RM0402	0.75
RM0502 and RM0603	1.0
RM0505, RM0705, RM1005, RM1206, and RM1505	2.0
RM1010, RM2010, RM2208, and RM2512	3.0

4.8.13.2 Bondable mounting integrity (termination's G, U, T, C, and D). The resistor chips shall be prepared as specified in 4.8.1.3b. A force shall be applied to all bondable units. The force shall be applied to the edge of the chip as shown on figure 4 for a minimum of 30 seconds. The resistor shall be examined for evidence of mechanical damage. The pusher width shall be a minimum of 30 percent of the resistor length and the maximum width shall be 70 percent of the chip length. The applied force shall be as specified in table XVI.

TABLE XVI. Bondable mounting integrity.

STYLE	FORCE APPLIED (kilograms)
RM0302 and RM0402	0.4
RM0502 and RM0603	0.5
RM0505, RM0705, RM1005, RM1206, and RM1505	1.0 1/
RM1010, RM2010, RM2208, and RM2512	1.5

1/ For termination D and T the applied force shall be 0.75 kilograms

4.8.13.3 Wirebonding integrity. The chip resistor shall be prepared as specified in 4.8.1.3c. A pull of 4 grams shall be applied by inserting a hook under the lead wire at approximately the center of the wire as shown in figure 5. The force shall be applied at a 90 degree angle to the surface of the chip, one lead at a time for a minimum of 30 seconds each.

4.8.14 Resistance to solvents (see 3.20). Resistors shall be tested in accordance with method 215 of MIL-STD-202. The following details and exceptions shall apply:

a. Mounting: Unmounted or mounted.

b. The marked portion of the resistor shall be brushed.

c. The number of sample units shall be as specified in table IX.

d. Resistors shall be inspected for mechanical damage and legibility of minimum marking.

4.8.15 Laser marking legibility test (see 3.21). Resistors shall be coated with .005 inch (0.13 mm) minimum of silicon resin insulated compound, type SR of IPC CC 830. After curing, coated resistors shall be examined for legibility under normal production room lighting by an inspector at 10X magnification.

4.8.16 Outgassing (see 3.24). The resistors organic material shall be tested in accordance with ASTM E595.

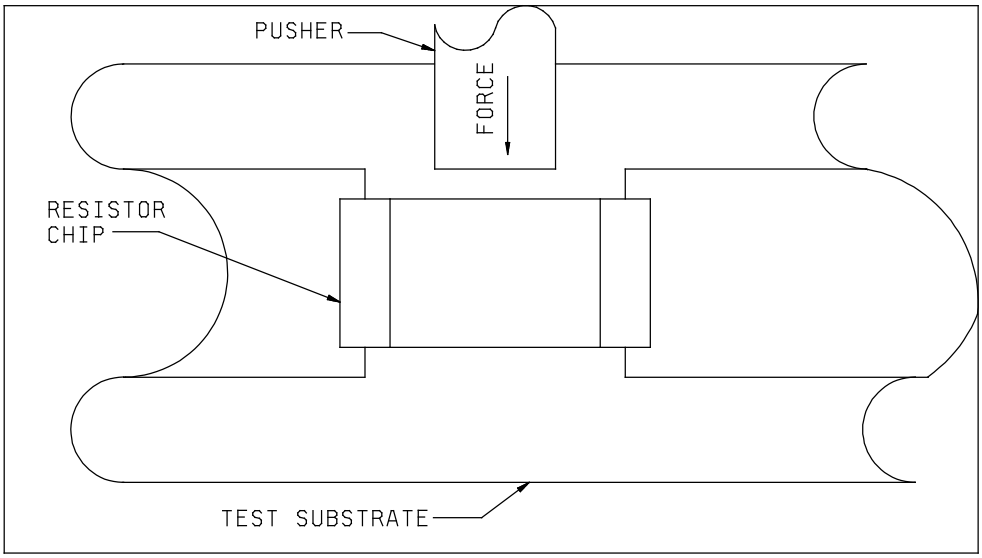


FIGURE 4. Mounting integrity test fixture.

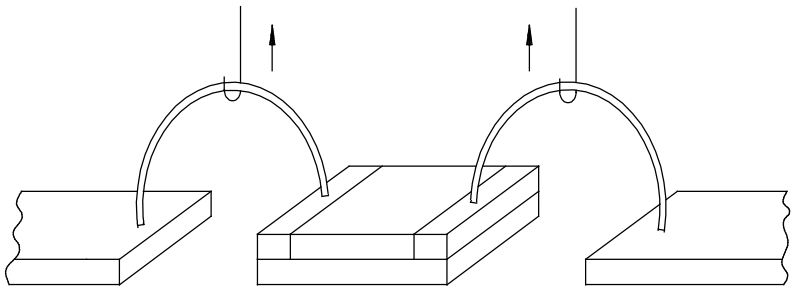


FIGURE 5. Weldable style units.

5. PACKAGING

5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When actual packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activity within the Military Service or Defense Agency, or within the military services system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory.)

6.1 Intended use. The chip resistors covered by this specification are military unique due to the fact that these devices must be able to operate satisfactorily in military systems under the following demanding conditions: 100 cycles of thermal shock at high and low temperature extreme, high temperature for an extended period of time, and low temperature for an extended period of time. In addition, these military requirements are verified under a qualification system and an extended failure rate of 0.001 percent per 1,000 hours. Commercial components are not designed to withstand these military environmental conditions.

6.2 Acquisition requirements. Acquisition documents must specify the following:

a. Title, number, date of this specification, the applicable associated specification, and the complete PIN (see 1.2.1).

b. Unless otherwise specified (see 2.1), the versions of the individual documents referenced will be those in effect on the date of release of the solicitation.

c. Packaging requirements (e.g., Electrostatic discharge (ESD) sensitivity) (see 5.1).

d. Allowable substitution (see 3.25.4).

e. If marking is required (see 3.25).

* 6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Products List QPL-55342 whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or purchase orders for the products covered by this specification. The activity responsible for the QPL is the US Army Communications - Electronics Research Development and Engineering Center, ATTN: RDER-PRO, Aberdeen Proving Ground, Bldg. 6010 K-130, MD 21005; however, information pertaining to qualification of products may be obtained from the DLA Land and Maritime, ATTN: VQP, P.O. Box 3990, Columbus, OH 43218-3990. An online listing of products qualified to this specification may be found in the Qualified Products Database (QPD) at https://assist.dla.mil.

6.4 Application notes.

6.4.1 Mounting of resistors. Resistors may be mounted individually on a test board, fiberglass base, and connected to conductor areas by means of solder perform, conductive cement, or wire bonding. Users are cautioned that the substrate and chip component must have compatible temperature coefficients of expansion to reduce the strain level imposed on the solder connections. They may also be directly connected to other components on the same test board by means of wire bonding using the test board as a base or carrier for the resistor.

6.4.2 Stacking of resistors. Stacking is generally discouraged since experience indicates that failure may occur due to electrolytic action in the bonding adhesive. This action occurs from the increase in temperature caused by stacking in conjunction with the operating voltage across the resistor. The bonding adhesive at the resistor chip interface chemically reacts with the active resistor material changing the noise and resistance values and eventually the resistor will open. If stacking resistors, care should be taken to compensate for the lower heat dissipation capabilities by derating the wattage rating.

6.4.3 Close tolerance resistors. Close tolerance resistors (i.e., ±0.1 percent) should be mounted on a test board by a method which produces the least heating effect over a short time to avoid permanent changes in resistance.

6.4.4 Resistor film orientation. It is recommended that the film side of resistors be mounted up when they are placed onto printed circuit boards. This is due to the effect of thermal stressing on epoxies used to hold them in place when mounted on the bottom of printed circuit boards. Resistor films can be torn from the substrate during thermal cycling substantially altering the value of the resistor.

6.4.5 Tin whisker growth. The use of alloys with tin content greater than 97 percent, by mass, may exhibit tin whisker growth problems after manufacture. Tin whiskers may occur anytime from a day to years after manufacture and can develop under typical operating conditions, on products that use such materials. Conformal coatings applied over top of a whisker-prone surface will not prevent the formation of tin whiskers. Alloys of tin containing 3 percent or more lead, by mass, have shown to inhibit the growth of tin whiskers. For additional information on this matter, refer to ASTM-B545 (Standard Specification for Electrodeposited Coatings of Tin).

6.4.6 Thermal management. The temperature of the larger chip sizes (2010 and 2512) shall not exceed 150°C. The larger chip sizes are conduction cooled devices and reliable operation depends upon maintaining the resistor film at or below 150°C. Adjusting the ambient temperature may be necessary.

6.4.7 Termination R substitution data. For all designs and logistic support of the cancelled termination R (solderable pretinned wraparound), termination B (solderable base metallization barrier metal, solder coated, wraparound) shall be used.

6.5 Noise level test. This specification does not include a noise test. If the user requires a noise test, it should be performed in accordance with method 308 of MIL-STD-202.

6.6 Electrostatic charge effects. Under relatively low humidity conditions, some types of film resistors, particularly those with small dimensions and high sheet resistivity materials, are prone to sudden significant changes in resistance (usually reductions in value) and to changes in temperature coefficient of resistance as a result of discharge of static charges built up on associated objects during handling, packaging, or shipment. Substitution of more suitable implements and materials can help minimize this problem. For example, use of cotton gloves, static eliminator devices, air humidifiers, and operator and work bench grounding systems can reduce static buildup during handling. Means of alleviating static problems during shipment include elimination of loose packaging of resistors and use of metal foil (conductive) and static dissipative packaging materials. Direct shipments to the Government are controlled by MIL-DTL-39032 which specifies a preventive packaging procedure.

6.7 Pulse applications. Designers are CAUTIONED on using these resistors in high power pulse applications. Since they have not been qualified nor tested for such applications, damage and premature failure are possible. These resistors only see a five second short time overload (see 4.8.6) as part of the group B inspection of this specification.

6.8 Environmentally preferable material. Environmentally preferable materials should be used to the maximum extent possible to meet the requirements of this specification. As of the dating of this document, the U.S. Environmental Protection Agency (EPA) is focusing efforts on reducing 31 priority chemicals. The list of chemicals and additional information is available on their website at http://www.epa.gov/osw/hazard/wastemin/priority.htm. Included in the list of 31 priority chemicals are cadmium, lead, and mercury. Use of these materials should be minimized or eliminated unless needed to meet the requirements specified herein (see Section 3).

6.9 Subject term (key word) listing.

Failure rate
Hybrid circuits
Surface mount
Termination

6.10 Amendment notations. The margins of this specification are marked with asterisks to indicate modifications generated by this amendment. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations.

APPENDIX A

PROCEDURES FOR QUALIFICATION INSPECTION

A.1 SCOPE

A.1.1 Scope. This appendix covers the procedure for qualification inspection of resistors covered by this specification. This appendix is a mandatory part of this specification. The information contained herein is intended for compliance. This appendix also outlines the procedure for extending qualification to the various product levels as well as the resistance range, characteristics, tolerances, and FRLs.

A.2 APPLICABLE DOCUMENTS. This section is not applicable to this document.

A.3 SUBMISSION

A.3.1 Product levels. Qualification of the C (non-ER) level is predicated upon meeting the ER qualification requirements for FRL P (see A.4.1). Qualification of the T (space) level is predicated upon meeting the ER qualifications requirements for FRL R or S (see A.4.1). To obtain qualification to the T (space) level, the manufacturers shall use the existing ER FRL (R, S, U, or V) design, and meet the additional requirements for outgassing and the 100 cycle thermal shock test (see A.3.2) as well as been approved by the qualifying activity on the capability to conduct tests and examinations for the space level product (e.g., resistance noise, destructive physical analysis, production lot formation). The procedure for submitting samples to become qualified to the initial FRL M is specified in A.3.2.

A.3.2 Sample. A sample consisting of 192 sample units, 34 of the lowest, 34 of the highest, and 34 of the critical or nearest to critical value (see table A-II), and in each style and characteristic, termination material, and resistance tolerance for which qualification is sought, shall be submitted to groups II, III, IV, and VI for normal ER qualification of VIII. In addition 30 samples of any value (10 for group V and 20 for group VII) shall be submitted. If applying for space level qualification an additional 30 samples (10 of the lowest, 10 of the highest, and 10 of the critical) shall be submitted to group VIII of table VIII. If qualification to a closer resistance tolerance than submitted above is desired, 30 additional sample units of the closer resistance tolerance shall be subjected to the following tests (see table A-I). After qualification has been granted, no changes shall be made in materials, design, or construction without prior notification to the qualifying activity.

TABLE A-I. Sample size for qualification inspection.

Inspection	Requirement paragraph	Method paragraph	Number of sample units for inspection	Number of defectives allowed
Visual and mechanical inspection	3.1, 3.4, 3.5, 3.5.1 through 3.5.3 inclusive, 3.23 and 3.25	4.8.1	30 (10 highest, 10 critical, 10 lowest)	0
DC resistance	3.8	4.8.2		
Thermal shock	3.9	4.8.3		

A.3.2.1 Qualification to extended resistance ranges. For qualification to the extended resistance ranges of higher resistance tolerances, 54 additional samples of high or low resistance shall be subjected to the tests of group I, group II, group III, and group IV of table VIII.

A.3.3 Outgassing (space level only). Manufacturers shall validate to the qualifying activity the outgassing requirements as specified in 3.24.

APPENDIX A

TABLE A-II. Critical resistance values for verification testing only and shall not be used for design and application purposes. 1/ 2/ 3/

STYLE	SLASH SHEET	CRITICAL RESISTANCE VALUE	PWR (milliwatts)	VOLTAGE (Volts)
RM0502	1	32.4	50	40
RM0505	2	13.0	125	40
RM0705	6	16.9	150	50
RM1005	3	28.7	200	75
RM1010	10	11.3	500	75
RM1505	4	105	150	125
RM2208	5	137	225	175
RM1206	7	40.2	250	100
RM2010	8	28.7	800	150
RM2512	9	40.2	1 Watt	200
RM0402	11	18.2	50	30
RM0603	12	25.5	100	50
RM0302	13	5.76	40	15

1/ Maximum continuous working voltage shall be applied (see 3.1).
2/ The critical resistance value is the maximum standard resistance value which will dissipate full wattage when the maximum continuous working voltage is applied.
3/ All resistance in kilohms.

A.4 EXTENT OF QUALIFICATION

A.4.1 Extent of qualification. The resistance range included in the qualification of any one style and tolerance shall be between any two adjacent resistance values which pass the required qualification inspection. The extent of qualification between styles, characteristics, termination's, FRLs, and resistance tolerances shall be as specified in table A-III.

APPENDIX A

TABLE A-III. Extension of qualification.

Style	Will qualify style 1/	
RM0302	RM0302	
RM0402	RM0402, RM0302	
RM0502	RM0502, RM0402, RM0302	
RM0603	RM0603, RM0502, RM0402, RM0302	
RM0505	RM0505	
RM0705	RM0705, RM0505	
RM1005	RM1005, RM0705, RM0505	
RM1010	RM1010, RM1005, RM0705, RM0505	
RM1505	RM1505, RM1005, RM0705, RM0505	
RM2208	RM2208	
RM1206	RM1206, RM1505, RM1010, RM1005, RM0705, RM0505	
RM2010	RM2208, RM2010	
RM2512	RM2010, RM2208, RM2512	
Characteristic	Will qualify characteristic	May qualify characteristic with minor additional testing 2/
E	E, H	K, L, M
H	H	K, L, M
K	K, L, M	
L	L, M	
M	M	
Termination	Will qualify termination	May qualify termination with minor additional testing 2/
G	G	B, W
W	W	
B	B	G, W, C, U 3/
U	U, T	C, D
T	T	D
C	C, D	U, T
D	D	T
Product level	Will qualify product level	
T	S, V, R, U, P, M, C	
S & V	R, U, P, M, C	
R & U	P, M, C	
P	M, C	
M	C	
C		
Resistance tolerance	Will qualify resistance tolerance	
0.1	0.1, 0.25, 0.5, 1.0, 2.0, 5.0, 10.0	
0.25	0.25, 0.5, 1.0, 2.0, 5.0, 10.0	
0.5	0.5, 1.0, 2.0, 5.0, 10.0	
1.0	1.0, 2.0, 5.0, 10.0	
2.0	2.0, 5.0, 10.0	
5.0	5.0, 10.0	
10.0	10.0	

1/ The same design and technology must be utilized for the style qualified and the styles that the qualification is extended to.
2/ To be determined by qualifying activity.
3/ Must contain barrier layer to qualify

APPENDIX B

VISUAL INSPECTION

B.1 SCOPE

B.1.1 Scope. This appendix details the procedure for visual inspection of conductors, metallization, scratches, voids, corrosion, substrate defects, etc., of chip resistors covered by this specification. This appendix is a mandatory part of this specification. The information contained herein is intended for compliance.

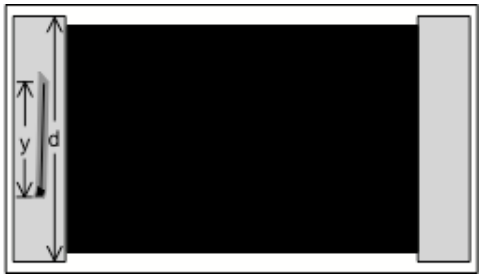
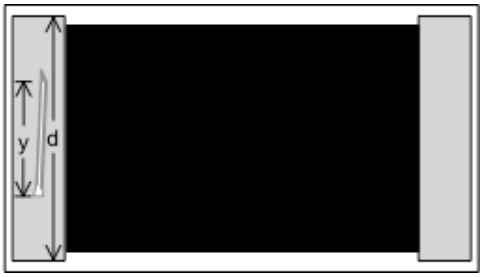
B.2 APPLICABLE DOCUMENTS

This section is not applicable to this appendix.

B.3 INSPECTION

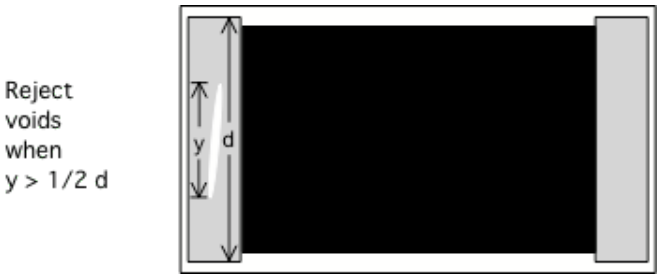
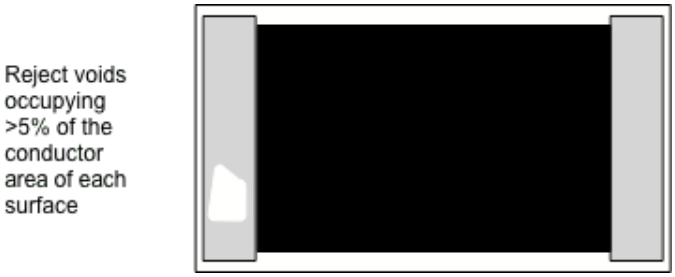
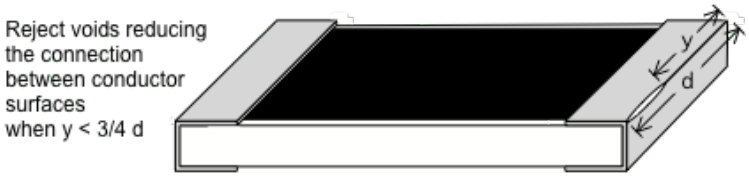
B.3.1 Conductor metallization defects (thick and thin film). Any resistor which exhibits the following defects in the active circuit metallization shall not be acceptable. The active circuit metallization is all metal or any other material used for interconnection except metallized scribe lines, unused bonding pads, and identification marking.

B.3.1.1 Conductor metallization scratches. A scratch is defined as any tearing defect that disturbs the original surface of the metallization.

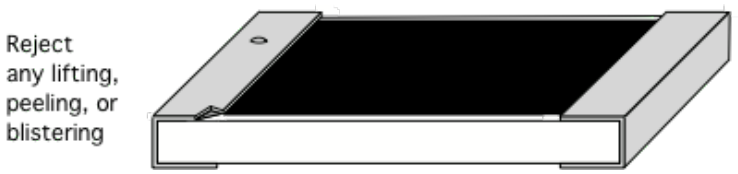
a. Reject any scratch exposing underlying resistor material or leaves < 50% of the original width remaining (see figure B-1).	Reject any exposed underlying resistor material or when y > 1/2 d  FIGURE B-1. Conductor metallization scratches.
b. Reject any scratch exposing substrate anywhere along its length or leaves < 50% of the original width remaining (see figure B-2).	Reject any exposed underlying substrate or when y > 1/2 d  FIGURE B-2. Conductor metallization scratches exposing substrate.

APPENDIX B

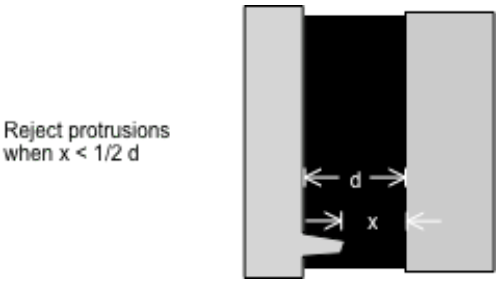
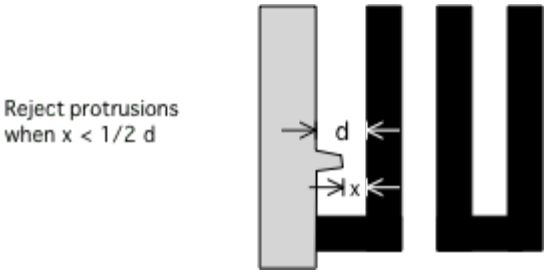
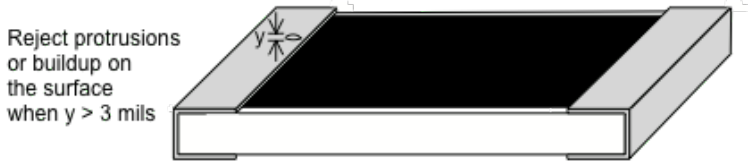
B.3.1.2 Conductor metallization voids. A void is defined as any region where the underlying resistive material or substrate is exposed which is not caused by a scratch.

a. Reject voids which leaves < 50% of the original width (see figure B-3).	 FIGURE B-3. Conductor metallization voids.
b. Reject voids larger than 5% of the conductor area of each surface (see figure B-4).	 FIGURE B-4. Conductor metallization voids larger than 5% of the conductor area.
c. Reject voids that reduce the connection between conductor surfaces to less than 75% of the original width (see figure B-5).	 FIGURE B-5. Conductor metallization void reduces connection between conductor surfaces.

B.3.1.3 Conductor metallization nonadherence. Conductor metallization nonadherence is defined as any evidence of metallization lifting, peeling, or blistering.

a. Reject any lifting, peeling, or blistering (see figure B-6).	 FIGURE B-6. Conductor nonadherence.

B.3.1.4 Conductor metallization protrusions. Conductor metallization protrusion defects are defined as extraneous metallization extending beyond the metallization patterns designed edge.

a. Reject protrusions that reduce the distance between any two metallization areas to < 50% of the original gap (see figure B-7).	 FIGURE B-7. Conductor metallization protrusions.
b. Reject protrusions between metallization and resistor pattern that reduces the distance to < 50% of the original gap (see figure B-8).	 FIGURE B-8. Conductor metallization protrusions between metallization and resistor pattern.
c. Reject protrusions or buildup on the surface of the conductor metallization that extends greater than 3 mils beyond the average thickness of the metallization (see figure B-9).	 FIGURE B-9. Conductor metallization protrusions or build up on the metallization surface.

B.3.1.5 Conductor metallization stain. Metallization stain is defined as any evidence of localized heavy discoloration.

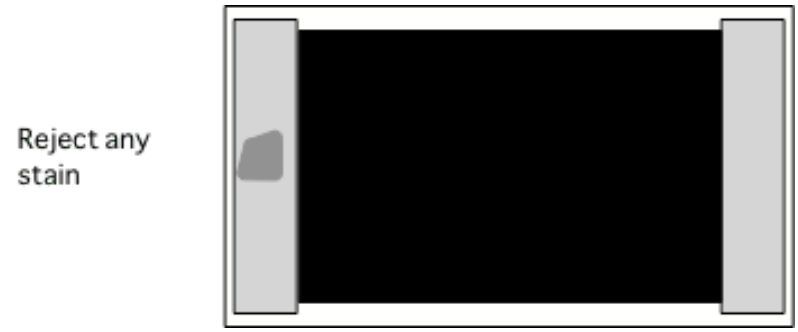
a. Reject any stain (see figure B-10).	

FIGURE B-10. Conductor metallization stain.

B.3.2 Resistor element defects (thick and thin film). Resistor elements are patterned into block or serpentine patterns to produce the range of resistance values provided (see figure B-11). Serpentine patterns are comprised of meanders and features (links, ladders, and top-hats) used to trim the resistance value. The trimming of serpentine resistor elements produces meanders and ladders that actively carry current between the terminals of the resistor element. These active meanders and ladders comprise the active region of the resistor element. Other meanders and ladders that are left untrimmed carry very little current and are considered non-active. Non-active regions are two links or rungs beyond the last trimmed link or rung (see figure B-12).

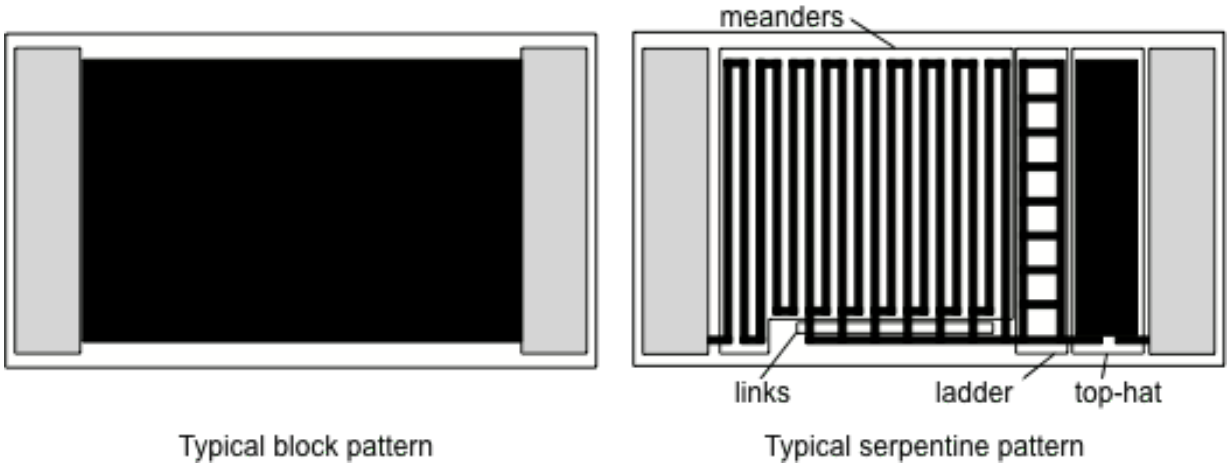


FIGURE B-11. Block and serpentine resistor elements.

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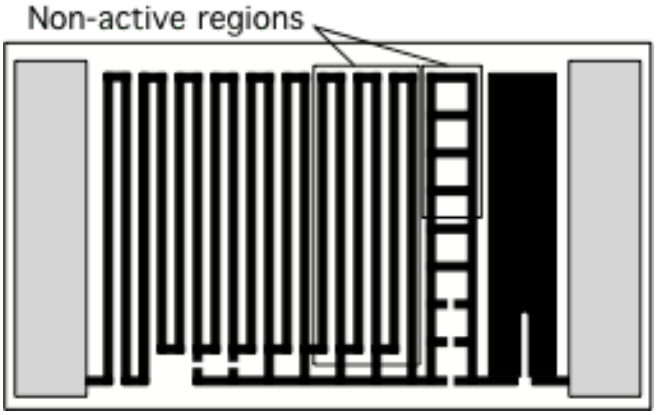
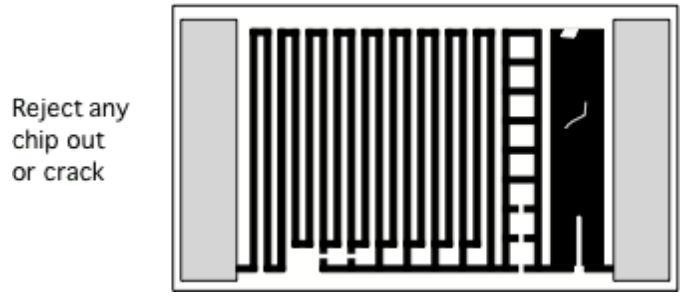


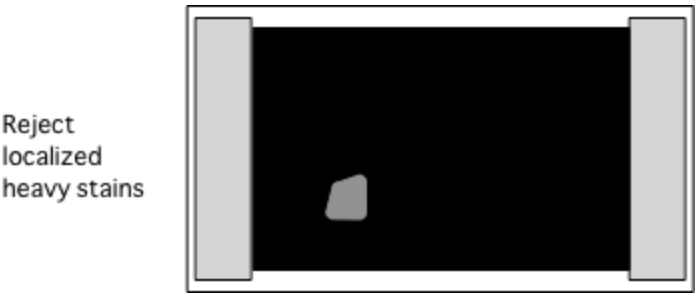
FIGURE B-12. Non-active regions of serpentine resistor elements.

B.3.2.1 Resistor element nonadherence. Reject any lifting, peeling, or blistering in the active or non-active regions of the resistor element.

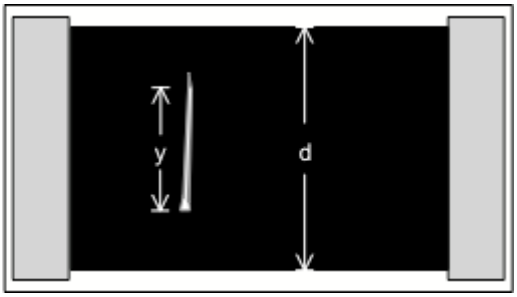
B.3.2.2 Resistor element cracks.

a. Reject any chip out or crack in the active or non-active regions of the resistor element (see figure B-13).	 FIGURE B-13. Resistor element cracks.

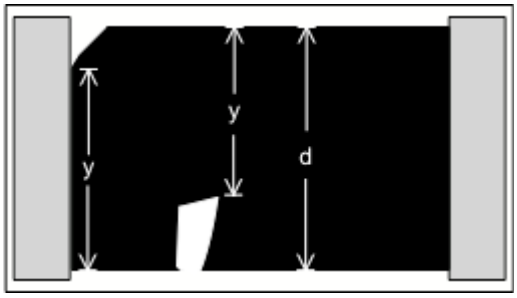
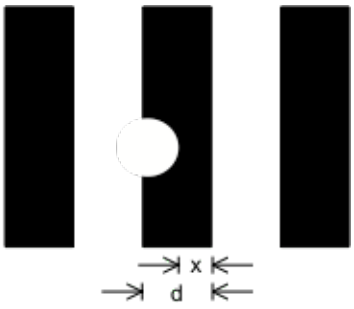
B.3.2.3 Resistor element stain.

a. Reject localized heavy stains in the active and non-active regions of the resistor element (see figure B-14). Note: Discoloration of the active and non-active regions of the resistor element due to thermal stabilization is not cause for rejection. Discoloration of resistor elements in and around trim kerfs is not cause for rejection.	 FIGURE B-14. Resistor element stain.

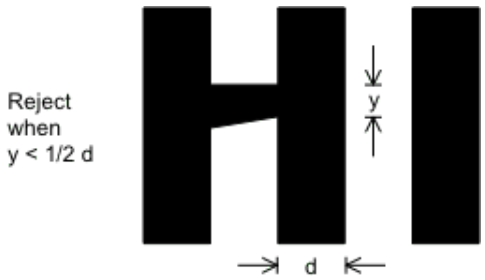
B.3.2.4 Resistor element scratches. A scratch is defined by either a disturbance of the surface of the resistor element or extraneous, shiny material remaining from the instrument causing the scratch.

a. Reject any scratch in the active region of the resistor element ≥0.001" in any direction or reduces the line width to <50% of the design line width (see figure B-15). Note: Scratches in the non-active regions of serpentine resistor elements are not cause for rejection.	Reject when y > 1 mil or y > 1/2 d  FIGURE B-15. Resistor element scratches.

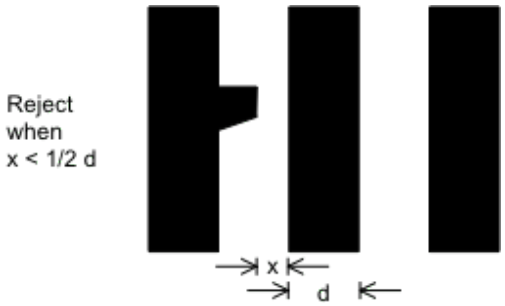
B.3.2.5 Resistor element voids. A void is defined as any region where the underlying material or substrate is exposed which is not caused by a scratch.

a. Reject any voids or neckdown in the resistor element area of a block pattern resistor element reducing the width of the resistor element to <90% of the original width (see figure B-16).	Reject when y < 9/10 d  FIGURE B-16. Resistor element voids – block pattern.
b. Reject any voids or neckdown in the active region of a serpentine pattern which reduces the width of the resistor element to <50% of the original width (see figure B-17). Note: Voids in the non-active regions of serpentine resistor elements are not cause for rejection.	Reject when x < 1/2 d  FIGURE B-17. Resistor element voids – serpentines pattern.

B.3.2.6 Resistor element bridges. Bridge defects are define as extraneous resistor material spanning two or more adjacent active resistance areas

a. Reject when the width of bridge is less than one half the smallest line width in the pattern (see figure B-18). Note: Bridging defects in the non-active regions of serpentine resistor elements are not cause for rejection.	 FIGURE B-18. Resistor element bridges.

B.3.2.7. Resistor element protrusions. Resistor protrusion defects are defined as extraneous resistor material extending beyond the resistor patterns designed edge.

a. Reject any resistor protrusion that reduces the distance between adjacent active resistance areas to <50 percent of the design separation (see figure B-19). Note: Protrusion defects in the non-active regions of serpentine resistor elements are not cause for rejection.	 FIGURE B-19. Resistor element protrusions.

B.3.2.8 Resistor element trim defects.

a. Reject any detritus (fragments of original or trim-modified material) in the trim kerf (see figure B-20).

Note: Accept attached detritus in the kerf of thin film resistor materials that are self-passivating (such as tantalum nitride) resistor material provided that a clear path ≥0.1 mil in width exists in the kerf, reject attached detritus in the trim kerf of self-passivating resistor material with separation <0.1 mil between the detritus particles.

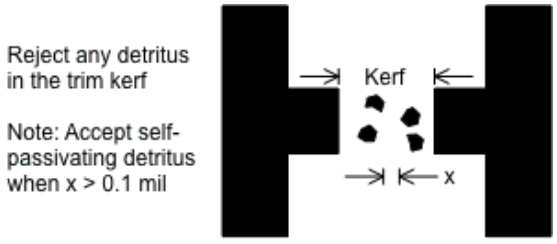


FIGURE B-20. Detritus in the trim kerf.

b. Reject trim kerfs with cracks, or similar damage in the underlying material (see figure B-21).

Note: Microcracks confined to the slag region of the trim kerf are not cause for rejection.

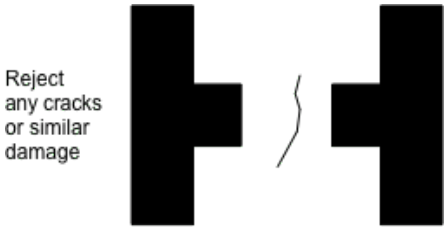


FIGURE B-21. Trim kerfs with cracks.

c. Trim kerf width. Reject thin film trim kerfs <0.1 mils wide and thick film trim kerfs <0.5 mils wide (see figure B-22 & B-23).

Note: Discoloration of resistor and passivation material in and around laser trim kerfs is not cause for rejection.

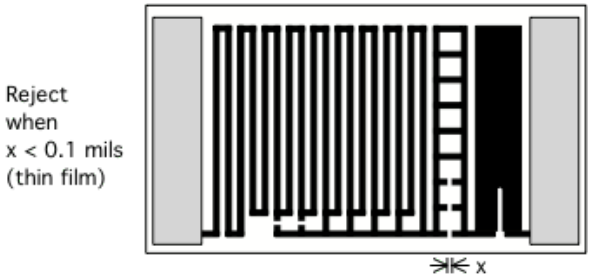


FIGURE B-22. Resistor element trim kerf width – thin film.

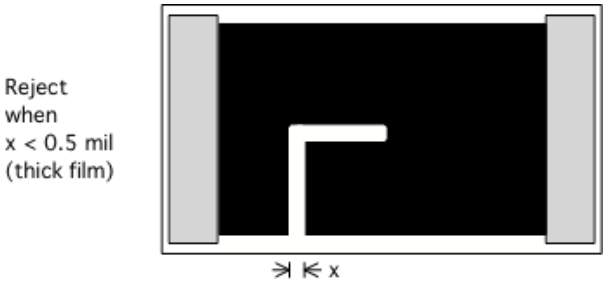
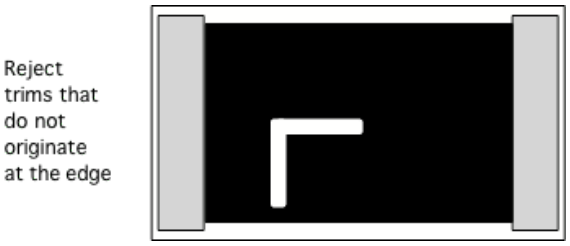
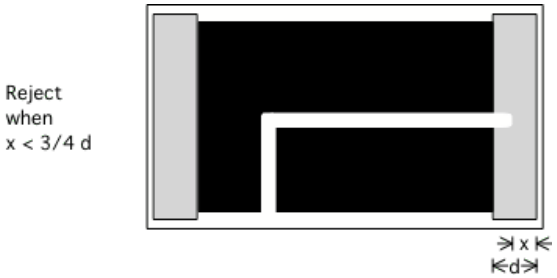
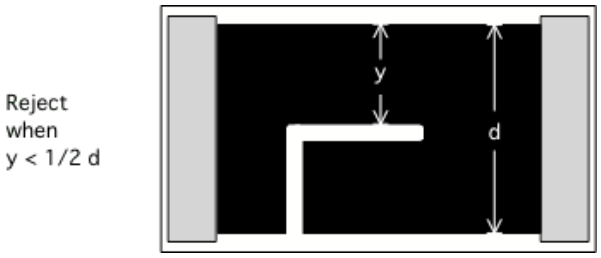
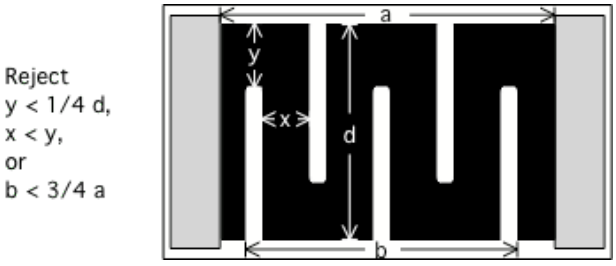
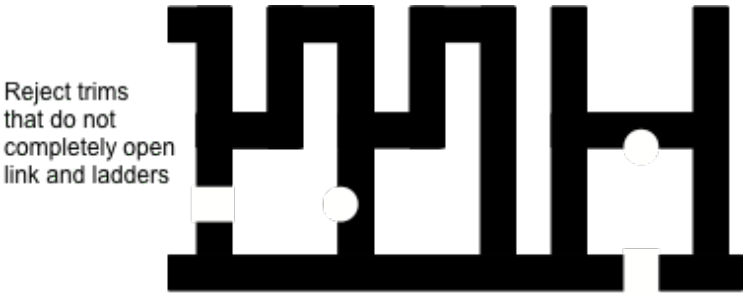
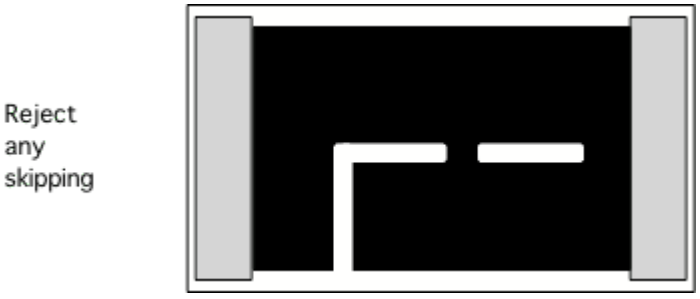


FIGURE B-23. Resistor element trim kerf width – thick film.

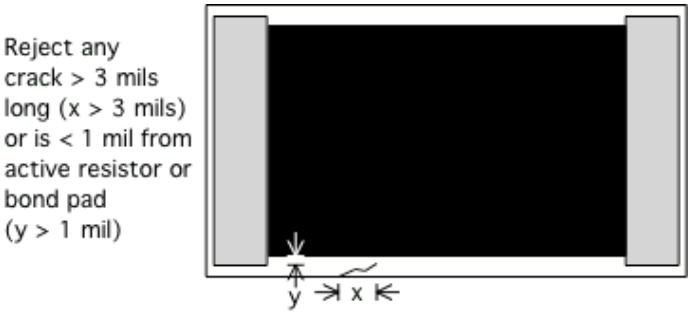
B.3.2.8 Resistor element trim defects (continued).

d. Trim location. Reject trims that do not originate at the edge of the resistor element (see figure B-24).	 FIGURE B-24. Trim kerfs that do not originate at the edge.
e. Trim location. Reject trims that extend into conductor metallization that leave <75% of the conductor undisturbed (see figure B-25).	 FIGURE B-25. Trim kerfs that extend into conductor metallization.
f. Trim depth. Reject trims that leave <50% of the width of the narrowest line in the pattern remaining (see figure B-26). * Note: Accept block patterns trimmed to create serpentine patterns. Reject plunge trims that leave <25% of the width remaining (y). Reject separation between trims (x) that is less than the width remaining (y). Reject plunge trims that span <75% of the length of resistor element (a) (see figure B-27).	 FIGURE B-26. Trim kerf depth – block pattern.  * FIGURE B-27. Trim kerf depth – serpentine pattern.

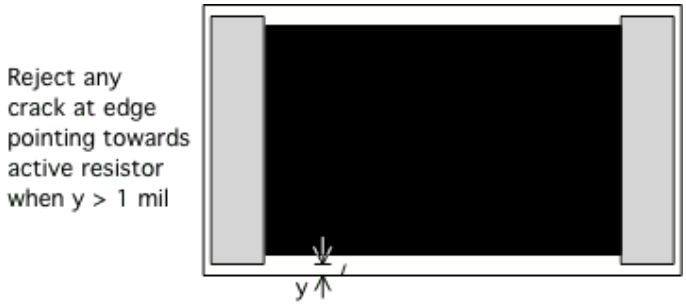
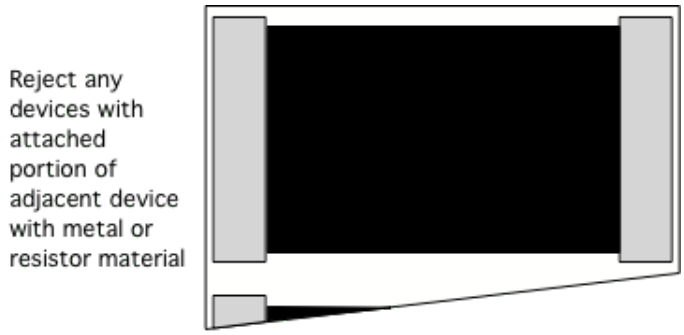
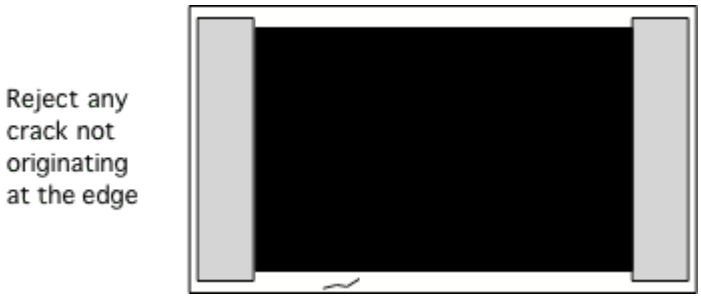
B.3.2.8 Resistor element trim defects (continued).

g. Link and ladder trim depth. Reject any trim that does not completely open any link or ladder (see figure B-28).	 FIGURE B-28. Trim kerf depth – link and ladder.
h. Skipping. Reject any discontinuous trim kerfs (see figure B-29).	 FIGURE B-29. Trim kerf depth – skipping.

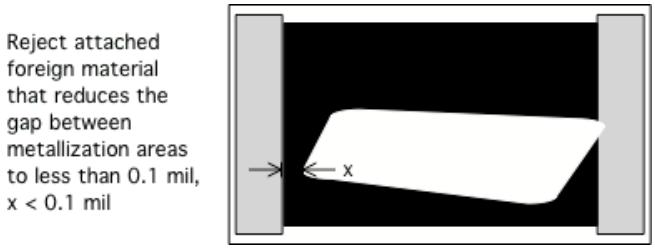
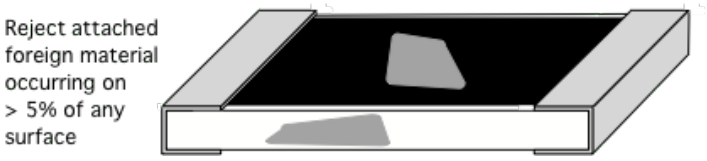
B.3.3 Substrate defects (thick and thin film).

a. Reject any crack in that exceeds 3.0 mil in length or comes closer than 1.0 mil to an active resistor or bonding pad area on the substrate (see figure B-30).	 B-30. Substrate crack.

B.3.3 Substrate defects (thick and thin film) (continued).

b. Reject any crack in a substrate that exceeds 1.0 mil in length and points towards the active resistor area (see figure B-31).	 FIGURE B-31. Crack that points towards the active area.
c. Reject any devices with an attached portion of an adjacent substrate which contains metallization or resistor material (see figure B-32).	 FIGURE B-32. Attached portion of an adjacent substrate.
d. Reject any crack not originating at a substrate edge (see figure B-33). Note: Microcracks confined to the slag region of the trim kerf are not cause for rejection.	 FIGURE B-33. Crack not originating at a substrate edge.

B.3.4 Foreign material (thick and thin film). Attached foreign material cannot be removed with a soft bristled brush or a nominal gas blow (of 20 psig) of dry nitrogen or air.

a. Reject attached foreign material that reduces the separation between metallization areas to ~~be~~ less than 0.1 mil (see figure B-34).	 FIGURE B-34. Attached foreign material reducing gap between metallization areas.
b. Reject attached foreign material occurring on greater than 5 percent of any surface (see figure B-35).	 FIGURE B-35. Attached foreign material on any surface.

B.3.5 Metal marks or extraneous termination material.

B.3.5.1 Heavy metal marks. Heavy metal marks are defined as extraneous termination material on the surface of the substrate or passivation greater than 0.001 inch. Heavy metal marks are similar in appearance to the termination material and typically exhibit metallic luster when viewed at 30X.

a. Reject for any heavy metal mark on the passivation greater than 2 mils in any direction (see figure B-36).

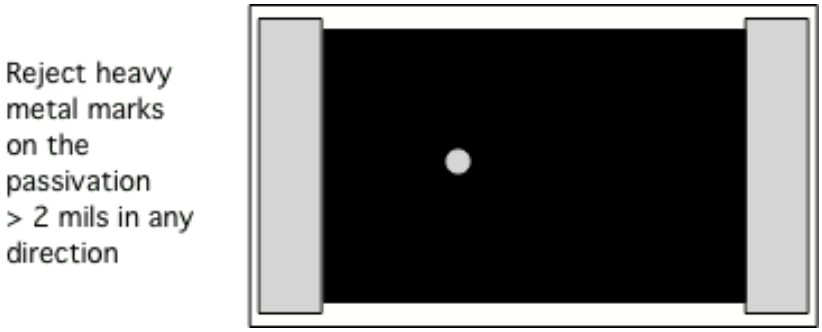


FIGURE B-36. Heavy metal marks on the passivation.

b. Reject for any heavy metal mark on the substrate greater than 10 mils in any direction. Up to 4 smaller heavy metal marks are allowed as long as none of the marks is larger than 3 mils in any direction and the cumulative total of the 4 smaller marks does not exceed 10 mils (see figure B-37).

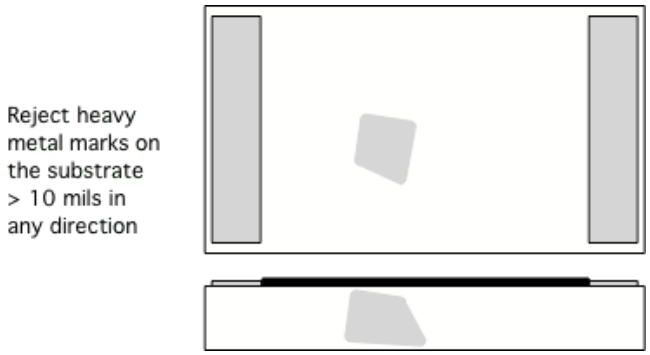


FIGURE B-37. Heavy metal marks on the substrate.

B.3.5.2 Light metal marks. Light metal marks are defined as deposits of small (less than 0.001 inch) particles of extraneous termination material on the surface of the substrate or passivation. Individual particles may or may not be apparent when view at 30X. These deposits typically do not exhibit metallic luster and may appear as a translucent residue due to the small size of the particles. Reject light metal marks that affect greater than 10 percent of the surface on which it occurs (see figure B-38).

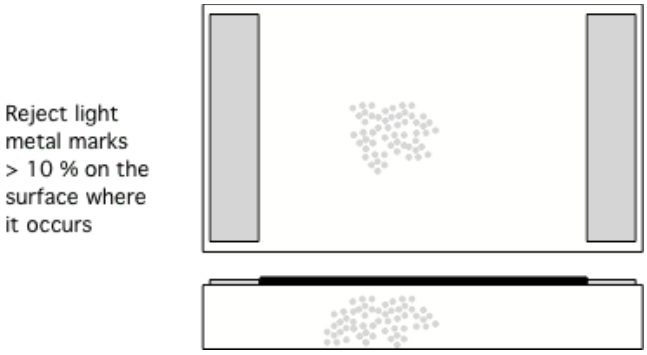


FIGURE B-38. Light metal marks.

B.3.5.3 Extraneous solder material. Reject protrusions or solder spikes from the conductor metallization edge longer than 10 mils or reduces the conductor separation to less than 50 percent of the design gap. Reject if attached solder spike can be removed with a soft bristled brush or a nominal gas blow (of 20 psig) of dry nitrogen or air (see figure B-39).

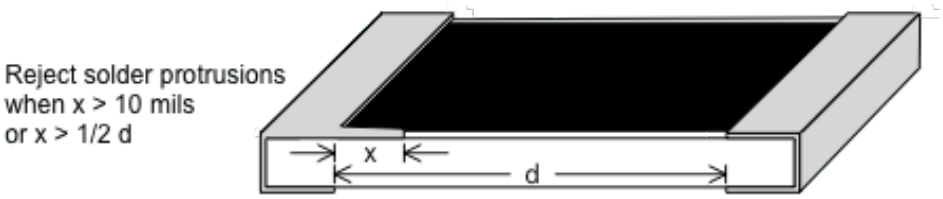
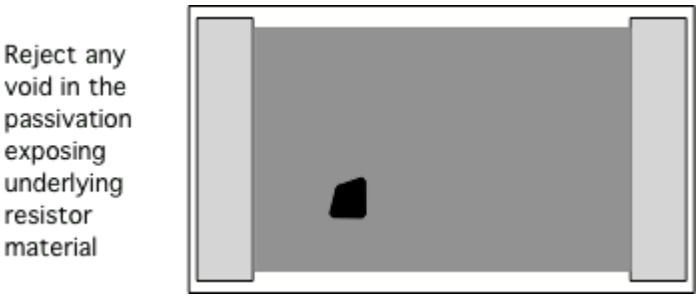


FIGURE B-39. Solder spike.

B.3.6 Coating Defects. Protective coating is applied over the resistor element for mechanical and environmental protection.

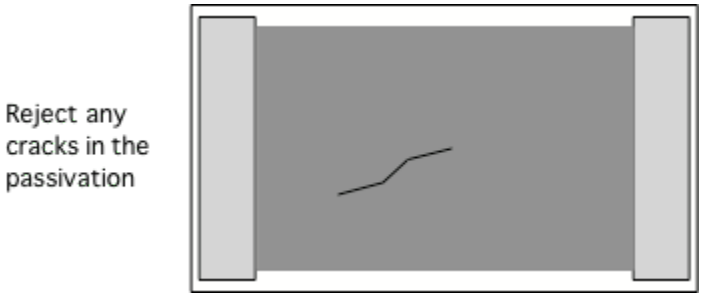
a. Reject for coating damage exposing underlying resistor element (see figure B-40).



Note: Trim kerfs may be visible or may be coated. Accept exposed resistor material along the edge of the trim kerf.

FIGURE B-40. Protective coating exposing underlying resistor element.

b. Reject for visible cracks in the coating (see figure B-41).



Note: Accept microcracks confined to the slag region of the trim kerf.

FIGURE B-41. Protective coating with visible cracks.

Custodians:
Army - CR
Navy - EC
Air Force - 85
DLA - CC
NASA - NA

Review activities:
Army - AR, AT, CR4, MI
Navy - AS, CG, MC, OS
Air Force - 19, 99
Other - MDA

Preparing activity:
Army - CR

Agent:
DLA - CC

(Project 5905-2016-015)

NOTE: The activities listed above were interested in this document as of the date of this document. Since organizations and responsibilities can change, you should verify the currency of the information above using the ASSIST Online database at https://assist.dla.mil.