The documentation and process conversion measures necessary to comply with this amendment shall be completed by 18 September 2017 (see 3.8).

INCH-POUND
MIL–PRF–55110H
W/AMENDMENT 2
19 May 2017
SUPERSEDING
MIL–PRF–55110H
W/AMENDMENT 1
20 May 2016
(See 6.6)

PERFORMANCE SPECIFICATION

PRINTED WIRING BOARD, RIGID, GENERAL SPECIFICATION FOR

Inactive for new design after 31 December 1997.
For new design use MIL–PRF–31032.

Comments, suggestions, or questions on this document should be addressed to DLA Land and Maritime ATTN: VAC, P.O. Box 3990, Columbus, OH 43218–3990, or by electronic mail to 5998.Documents@dla.mil. Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at https://assist.dla.mil.

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This specification is approved for use by all Departments and Agencies of the Department of Defense.

1. SCOPE

1.1 Scope. This specification establishes the performance and qualification requirements for rigid single–sided, double–sided, and multilayered printed wiring boards with or without plated through holes (see 6.1). Verification is accomplished through the use of one of two methods of product assurance (QPL or QPL/QML). Detail requirements, specific characteristics, and other provisions which are sensitive to the particular intended use are specified in the applicable master drawing.

1.2 Classification. Printed wiring boards are classified by 1.2.1 1.2.2 and 1.2.3.

1.2.1 Type. The printed wiring boards covered by this specification are of the following types:

Type 1 – Singled-sided printed wiring board (see 6.4.6.1).

Type 2 – Double–sided printed wiring board (see 6.4.6.2) with or without plated-through holes.

Type 3 – Multilayer printed wiring board with plated holes (see 6.4.6.3).

Type 4 – Multilayer printed wiring board with plated holes and blind or buried via holes (see 6.4.6.4).

1.2.2 Base material. The printed wiring board base material type should be identified by the applicable base material specification sheet or by the legacy base material type designator as required by the master drawing (see 3.1.1).

1.2.3 Wrap plating (surface and knee continuous copper plating). The wrap plating grade designation is defined by the amount of plated-through hole surface and knee continuous copper plating thickness remaining after surface processing. The grades are as follows:

A – Printed boards of this grade have 80 percent or more of the specified plating thickness in the wrap area after surface processing.

B – Printed boards of this grade have 50 percent or more of the specified plating thickness in the wrap area after surface processing.

C – Printed boards of this grade have 20 percent or more of the specified plating thickness in the wrap area after surface processing.

Unless otherwise specified, the default grade of wrap copper plating is grade A for printed board designs that will not undergo planarization and grade B for designs that require planarization.

1.3 Description of this specification. The main body contains general provisions and is supplemented by detailed appendices. Appendices A and B describe the two product assurance programs that can be implemented by the manufacturer. Appendix A contains the legacy Qualified Products List (QPL) product assurance program. Appendix B is an optional quality management approach using a technical review board concept along with a Qualified Manufacturer List (QML) product assurance program addressed in MIL–PRF–31032, to modify the generic verification criteria provided in this specification. Appendix C provides statistical sampling, and basic test and inspection procedures. Appendix D is optional and can be used when producing printed wiring boards designed to superseded design standards (see 6.6.2). Appendix D may also be used as a guide in developing a test plan for legacy or existing designs based on the tests and inspections of appendix A. Appendix E contains the qualification requirements. Appendix F and G contain illustrations of the acceptable and unacceptable conditions that are either externally or internally observable on printed boards. Appendix H contains the requirements for quality control test circuitry and is mandatory for manufacturers qualified to the QPL product assurance level of this specification.

2. APPLICABLE DOCUMENTS

2.1 General. The documents listed in this section are specified in sections 3 and 4 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3 and 4 of this specification, whether or not they are listed.

2.2 Government documents.

2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

MIL–PRF–31032 – Printed Circuit Board/Printed Wiring Board, General Specification for.

(Copies of these documents are online at http://quicksearch.dla.mil.)

2.3 Non-Government publications. The following documents form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

IPC – ASSOCIATION CONNECTING ELECTRONICS INDUSTRIES (IPC)

IPC–T–50 – Terms and Definitions for Interconnecting and Packaging Electronic Circuits.

(Copies of these documents are available online at http://www.ipc.org.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

2.4 Order of precedence. Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 General requirements. The manufacturer of printed wiring boards, in compliance with this specification, shall have and use production facilities, verification facilities, and product assurance procedures adequate to assure successful compliance with the provisions of this specification and the associated master drawing. Adequacy of a printed board manufacturer to meet the requirements of this specification shall be determined by the Government qualifying activity (DLA Land and Maritime, code VQE). Only printed wiring boards which are verified and meet all the applicable performance requirements contained herein and the design, construction, and material requirement of the associated master drawing shall be certified as compliant and delivered.

3.1.1 Master drawing. Printed wiring boards delivered under this specification shall be of the material, design, and construction specified on the applicable master drawing.

3.1.2 Conflicting requirements. In the event of conflict between the requirements of this specification and other requirements of the applicable master drawing, the precedence in which documents shall govern, in descending order, is as follows:

a. The applicable master drawing (see 3.1.1). Additional acquisition requirements (see 6.2) may be provided in the order or contract. Any deletion of any of the performance requirements or performance verifications of this specification not approved by the qualifying activity, will result in the printed wiring board being deemed noncompliant with this specification.

b. This specification.

c. The applicable design standard (see 3.1.1 and A.3.3 as applicable).

d. Specifications, standards, and other documents referenced in sections 2, A.2, B.2, C.2, and H.2.

3.1.3 Terms and definitions. The definitions for all terms used herein shall be as specified in IPC–T–50 and those contained herein (see 6.4, and appendices A, B, C, D, E, F, G, and H).

3.2 Qualification. Printed wiring boards furnished under this specification shall be products that are authorized by the qualifying activity for listing on the applicable QPL before contract award (see 4.3 and 6.3). In addition, the manufacturer shall receive certification from the qualifying activity that the product assurance requirements of 3.3 have been met and are being maintained. The qualification requirements shall be in accordance with appendix E. Products qualified in accordance with appendix E are monitored and maintained through the manufacturer's MIL–PRF–31032 Capability Verification Inspection program and do not require requalifiication to this specification.

3.3 Product assurance requirements. This specification contains two different methods of product assurance for printed wiring board compliance. The two levels of printed wiring product assurance are QPL (see 3.3.1) and QML (see 3.3.2) as defined herein.

3.3.1 QPL product assurance. A product assurance system for QPL printed wiring boards furnished under this specification shall satisfy the requirements of appendix A. QPL product assurance system procedures shall be revised to address changes from the previous revision of this specification and made available to the qualifying activity no later than 6 months after the date of this specification in order for the manufacturer to be retained on Qualified Products Database 55110 (QPD–55110). The manufacturer shall ensure the QPL product assurance system procedures reflect the actual product assurance practices of the manufacturing location qualified. The qualifying activity shall be notified within 28 days of any changes to these procedures.

3.3.2 QML product assurance. A product assurance program for QML printed wiring boards furnished under this specification shall satisfy the requirements of appendix B. QML product assurance procedures shall be revised to address changes from the previous revision of this specification and made available to the qualifying activity no later than 6 months after the date of this specification in order for QML–31032 manufacturers to be retained on QPD–55110. The manufacturer shall ensure the product assurance procedures reflect the actual product assurance practices of the manufacturing location qualified. The qualifying activity shall be notified concurrently of any changes to these procedures.

3.4 Letters of interpretation and policy. Letters of interpretation and policy applicable to this specification shall be approved in writing by the preparing activity or qualifying activity. All letters of interpretation and policy applicable to MIL–PRF–55110 written prior to the current date of this specification are not applicable to this revision. All subsequent letters of interpretation and policy letters are valid only until the next document change action (amendment or revision).

3.5 Recycled, recovered, environmentally preferable, or biobased materials. Recycled, recovered, environmentally preferable, or biobased materials should be used to the maximum extent possible, provided that the material meets or exceeds the operational and maintenance requirements, and promotes economically advantageous life cycle costs.

3.6 Certification of conformance and acquisition traceability. Unless otherwise specified by the contract or order (see 6.2), a certificate of conformance for compliant printed boards (see 6.5) shall be forwarded to the acquiring activity (see 6.4.1). When a certificate of conformance for compliant printed boards is supplied, it shall include the following information, as a minimum:

a. Manufacturer's name and address.

b. Customer's name and address.

c. Manufacturer's CAGE (Commercial and Government Entity) code (see 6.4.2).

d. Printed board description, including classification (printed wiring board type and base materials), specification number with revision letter and amendment number when applicable, the applicable product assurance level (either QPL or QML), master drawing or other identification number, and the applicable design standard or standards.

e. Lot date code.

f. Quantity of printed boards in shipment from manufacturer.

g. Statement certifying printed board conformance to this specification, the master drawing, and the contract or order.

h. The date of transaction.

i. A description or listing of the additional acquisition requirements (see A.6.2.2) not listed on the master drawing (see 3.1.1) that affects the design, test conditions, or acceptability requirements of the resulting printed boards.

j. The name of the company official approving the certificate of conformance. The manufacturer shall have a method for authenticating the approval of certificates of conformance for printed boards compliant to this specification.

3.7 Qualifying activity on-site audit. Manufacturers listed on QPD–55110 will be required to undergo periodic on-site audits of their facilities by the qualifying activity. The manufacturer shall demonstrate to the qualifying activity that controls have been implemented to assure compliance to the requirements of this specification. The qualifying activity reserves the right to perform on-site audits of any other facilities, such as contracted services, that the manufacturer uses for producing printed boards to this specification. The on-site audit shall verify that the manufacturer has an effective self-audit program for both itself and for all contract service operations used in the production of certified product.

3.8 Change effectivity. Unless otherwise specified by the preparing activity or the qualifying activity, all changes from the previous revision of MIL–PRF–55110 shall become effective within 120 days after the date of publication of this amendment. If a qualified manufacturer is unable to implement the changes within the 120 day time period, additional time shall be requested from the qualifying activity. Manufacturers that are QPL listed and have concerns regarding possible changes to retention reporting requirements should contact the qualifying activity for clarification.

3.9 Workmanship. Printed wiring boards shall be processed in such a manner as to be uniform in quality and shall be free from defects that exceed those allowed in this specification that could affect life or serviceability.

4. VERIFICATION

4.1 Classification of inspections. The inspection requirements specified herein are classified as follows:

a. Qualification inspection (see 4.3, A.4.5, or B.4.1).

b. Inspection of product for delivery (see A.4.6 or B.4.3.a).

c. Periodic conformance inspection (see A.4.7 or B.4.3.b).

4.2 Printed wiring board performance verification.

4.2.1 QPL. The minimum requirements for printed wiring board performance verification to the QPL product assurance level shall consist of inspections on the production printed wiring boards and the quality conformance test circuitry or test coupons referenced in appendix A.

4.2.2 QML. The minimum requirements for printed wiring board performance verification to the QML product assurance level shall satisfy the guidelines of appendix B.

4.3 Qualification inspection. The minimum requirements for qualification shall be as specified in appendix E. Qualification to appendix E shall be extended to cover qualification to appendix A. Manufacturers qualified through appendix E may accept and certify orders to appendix A product assurance level.

5. PACKAGING

5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of materiel is to be performed by DoD or in–house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain requisite packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activities within the Military Service or Defense Agency, or within the Military Service’s system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD–ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory.)

6.1 Intended use. Rigid printed wiring boards covered by this specification are intended for use in ground support, airborne, and shipboard electronic equipment to eliminate high density hand wiring and where compact electronic packaging is desirable.

6.2 Acquisition requirements. Acquisition documents should specify the following:

a. Title, number, revision letter (with any amendment number when applicable), and date of this specification.

b. The specific issue of individual documents referenced (see 2.2).

c. Title, number, revision letter (with any engineering change proposal or notice of revision number when applicable), and date of the applicable master drawing (see 3.1.1).

d. Appropriate printed wiring board type (see 1.2.1), base material type or classification (see 1.2.2), and grade of wrap plating (see 1.2.3).

e. The printed wiring board performance verification level desired (QPL or QML). If no level is specified, QPL printed wiring board performance verification will be used.

f. Requirements for certificate of conformance, if other than 3.6.

g. Packaging requirements (see 5.1).

6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in QPD–55110 whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from DLA Land and Maritime, ATTN: VQE, P.O. Box 3990, Columbus, Ohio 43218–3990 or by email 5998.Qualifications@dla.mil, or at Universal Resource Locator (URL) https://LandandMaritimeApps.dla.mil/Offices/Sourcing_and_Qualification. An online listing of products qualified to this specification may be found in the Qualified Products Database (QPD) at https://assist.dla.mil. Application procedures should conform to the guidelines of SD–6, "Provisions Governing Qualification" (see 6.3.4). In order to be listed in the QPD for QPL–55110, manufacturers will also have to maintain an active registration in the System for Award Management (SAM) database (see 6.4.3). Qualified capabilities details may be found in the Qualified Products Database Supplemental Information Sheet (QPDSIS) for QPL–55110 available at https://LandandMaritimeApps.dla.mil/programs/qmlqpl.

6.3.1 Transference of qualification. Manufacturers currently qualified to MIL–PRF–55110H will have their qualification transferred to this document under the conditions described in 3.3.1 and 3.3.2. The expiration date of their current qualification will not be changed. Qualifications in process (before the date of this document) will be performed to the requirements MIL–PRF–55110H. New applications for qualification (after the date of this document) will be performed to the requirements of this revision.

6.3.2 Retention of qualification. Printed wiring boards verified and certified to MIL–P–55110D, MIL–P–55110E, MIL–PRF–55110E, MIL–PRF–55110F, or MIL–PRF–55110G (with any amendment) or to any product assurance level contained herein will retain qualification to this document (see A.4.5.1).

6.3.3 Legacy manufacturer certification program. MIL–P–55110C certification program was not governed by the policies and procedures of the Defense Standardization Program as defined by DoD 4120.3–M and therefore does not exist within the QPL program of MIL–P–55110D and beyond. For additional information concerning this issue, see MIL–P–55110C, paragraph 60.1.

6.3.4 "Provisions Governing Qualification". Copies of SD–6, "Provisions Governing Qualification", may be downloaded at URL: http://quicksearch.dla.mil.

6.4 Definitions.

6.4.1 Acquiring activity. The organizational element of the Government which contracts for articles, supplies, or services may authorize a contractor or subcontractor to be its agent. When this organizational element of the Government has given specific written authorization to a contractor or subcontractor to serve as agent, the agent will not have the authority to grant waivers, deviations, or exceptions to this specification unless specific written authorization to do so has also been given by the Government organization, which is the preparing activity or qualifying activity. In the absence of a specific acquiring activity, the acquiring activity will be an organization within the supplier's company that is independent of the group responsible for device design, process development, or screening, or may be an independent organization outside the supplier's company.

6.4.2 Commercial and Government Entity (CAGE) code. The Commercial and Government Entity Code, or CAGE Code, is a 5 digit identifier assigned to suppliers to the Federal Government of the United States of America in order to provide a standardized method of identifying a given facility or a specific location. Request for or an update to a CAGE code can be obtained at URL: https://cage.dla.mil. CAGE was previously known as Federal Supply Code for Manufacturers (FSCM) and also the National Supply Code for Manufacturers (NSCM).

6.4.3 Customer. A customer is the recipient of a good, service, product or an idea, obtained from the certified and qualified manufacturer. For the purposes of this document, the terms "buyer", "client", "contractor", "purchaser", "subcontractor", or "user" will be interpreted as the customer.

6.4.4 Design standard. A document that establishes the baseline parameters (default values), standard practices and guidelines for the design of printed wiring boards. Within this specification, the term "design standard" is used to describe those documents that contain the design, construction, material, test coupon requirements, and guidelines used to produce panels of rigid printed wiring boards.

6.4.5 Manufacturer. The actual producer of a good, service, product or idea. For the purposes of this document, the terms "seller", "supplier", or "vendor" will be interpreted as the certified and qualified manufacturer.

6.4.6 Printed wiring board types. The printed wiring board types should be as specified herein.

6.4.6.1 Type 1. Type 1 rigid printed wiring boards have only one conductive layer (single–sided conductor pattern) with cover lay and no plating in the component holes.

6.4.6.2 Type 2. Type 2 rigid printed wiring boards are printed wiring boards with conductor patterns on both sides of the printed board (double–sided). In addition, the design of the printed wiring board may require plated-through holes in order to connect the conductor patterns on both sides together.

6.4.6.3 Type 3. Type 3 rigid printed wiring boards are multi–layered (with 3 or more conductor layers) with plated holes. Type 3 designs include those with metal core.

6.4.6.4 Type 4. Type 4 rigid printed wiring boards are multi–layered (with 3 or more conductor layers) with plated holes and blind or buried via holes.

6.4.7 Product assurance. The method of complying with the two different levels of this specification using either the QPL method, that has been integral to this specification since revision MIL–P–55110D, or the newer method, QML which was introduced in revision MIL–PRF–55110F.

6.4.7.1 QPL. A transitional program that allows a manufacturer that is certified and qualified to the QML program of MIL–PRF–31032 to fabricate, test, and supply products to this specification.

6.4.7.2 QML. A list of manufacturers, by name and plant address, who have met the certification and qualification requirements stated in MIL–PRF–31032. A QML focuses on qualifying an envelope of materials and processes rather than individual products or designs. That envelope is qualified by carefully selecting representative worst case test vehicles or representative samples from production that contain all potential combinations of materials and processes that may be subsequently used during production. A QML is normally appropriate for items of supply that have very rapid technological advancement or a myriad of variations or custom designs that make individual product qualifications impractical or excessively expensive.

6.4.8 Qualified Products Database (QPD). A QPD is an electronic version of a Qualified Products List (QPL) and Qualified Manufacturers List (QML) document. The QPD has replaced all of the information currently contained on QPL–55110. As the data in a specific QPL or QML is converted to database format, the QPL or QML will be phased out and replaced by an equivalent Qualification Dataset (QDS) associated with the specification requiring qualification. For MIL–PRF–55110, a Qualified Products Database Supplemental Information Sheet containing the information once listed on QPL–55110 is available from the qualifying activity.

6.4.9 Qualified Products Database Supplemental Information Sheet (QPDSIS). The qualified capabilities for manufacturers may be found in the QPDSIS for any particular MIL–PRF–55110 listing. The QPDSIS is available at https://LandandMaritimeApps.dla.mil/programs/qmlqpl.

6.4.10 System for Award Management (SAM). The Central Contractor Registration (CCR) system was transitioned to the System for Award Management (SAM) in 2012. The SAM is the primary registrant database for the U.S. Federal Government. SAM collects, validates, stores and disseminates data in support of agency acquisition missions. Qualified manufacturers should be registered in the SAM prior to the award of a contract; basic agreement, basic ordering agreement or blanket purchase agreement. SAM information can be obtained at https://www.sam.gov.

6.5 Compliant printed wiring boards. For a printed wiring board to be compliant with this specification, it must be produced by a manufacturer qualified for listing on QPD–55110 or reciprocal listing as described in appendix B, and must be obtained from a lot which was subjected to and passed all inspection of product for delivery verifications using the applicable product assurance program.

6.5.1 Reference to MIL–P–55110 and MIL–PRF–55110. When this document is referenced or used in conjunction with the processing and testing of QPL compliant printed boards in conformance with the requirements of appendix A, or QML printed boards in conformance with MIL–PRF–31032 using the requirements of appendix B, such processing and testing is required to be in full conformance with all applicable requirements and those of the specifically referenced test methods and procedures. The following conditions apply:

a. For contracts negotiated prior to 26 April 1978: Designs for printed board that have been classified as requiring compliance to MIL–P–55110 prior to 26 April 1978 are not required to meet 6.5.2 or 6.5.3.

b. Existing contracts as of 26 April 1978: Previously negotiated add-ons to these contracts, and future spares for these contracts may continue to use master drawings for printed boards which were classified as requiring compliance prior to 26 April 1978.

c. New contracts and any printed board designs classified to be compliant to MIL–P–55110 after 26 April 1978: These printed boards are required to comply with 6.5.2. Any printed boards meeting only the provisions of 6.5.3 are noncompliant to MIL–PRF–55110.

6.5.2 Provisions for the use of MIL–PRF–55110 in conjunction with compliant printed boards. When any manufacturer, contractor, subcontractor, or original equipment manufacturer requires or claims a printed board to be compliant with MIL–PRF–55110, all provisions of appendix A or B of MIL–PRF–55110 are required to be met. In addition, manufacturers that have produced, or are producing, printed boards in accordance with 6.5.1.a are subject to a qualifying activity compliance audit as specified in 3.7. Such processing and testing of printed boards are required to be in compliance with all of the applicable general controls and requirements defined herein, and those of the specifically referenced test methods and procedures with no reinterpretations, deviations, or omissions except as specifically allowed in the master drawing. Such references of compliance include the following:

a. Manufacturers who reference MIL–PRF–55110 in certificates of conformance, or make statements that printed boards are compliant with MIL–PRF–55110 (or MIL–P–55110), or make statements in advertisements, or in published brochures, or other marketing documents, that printed boards provided are compliant with MIL–PRF–55110.

b. Contractors, sub-contractors, or original equipment manufacturers who prepare master drawings, or printed board procurement documentation, which require compliance with MIL–PRF–55110 (or MIL–PRF–55110), or invoke it in its entirety as the applicable specification (see 6.5.3 for non-compliant printed boards) are be subject to the following:

   a. Printed boards described as compliant to MIL–P–55110 are required to meet all the requirements of MIL–P–55110 or appendix A of MIL–PRF–55110.

   b. Printed boards described as compliant to appendix B of MIL–PRF–55110 are required to meet all the requirements of the applicable MIL–PRF–31032 specification sheet.

   c. Custom technologies described on master drawings but not covered by MIL–P–55110 or MIL–PRF–55110 should be supplied by manufacturers qualified to MIL–PRF–31032.

6.5.3 Provisions for the use of MIL–PRF–55110 in conjunction with non-compliant printed boards. Any printed board that is processed with negative deviations (see 6.5.4) and which is not processed in compliance with the provisions of 6.5.2 herein cannot be claimed to be compliant and cannot be certified "to the intent of MIL–PRF–55110", "tested to, but not qualified to MIL–PRF–55110", or any variant thereof. All applicable documentation (including master drawings and printed board procurement documentation and responses to RFQ's invoking MIL–PRF–55110) are required to clearly and specifically define any and all areas of nonconformance and identify them as deviations in language that is not subject to misinterpretation by the acquiring activity.

6.5.4 Deviations to requirements. Deviations that increase sample sizes, tighten requierments, or add inspections and tests are considered additive deviations. These additive deviations do not negate the compliance of printed boards and hence, the certification of the affected printed boards as being compliant. Deviations that reduce sample sizes, loosen requirements, or eliminate inspections and tests, are viewed as negative deviations. These negative deviations negate the compliance of printed boards and hence, the certification of the affected printed boards is not possible.

6.6 Supersession.

6.6.1 Design, construction, and verification. Design, construction, and verification supersession information is included in appendix D of this specification.

6.6.2 Reference to superseded design standards. This specification contains requirements and guidelines for the testing of printed wiring boards that were designed to and make use of test coupons conforming to appendix H. See appendix D for additional guidance regarding the verification of printed boards using different design standards.

6.6.3 References on master drawings. All the requirements of this specification are interchangeable with those specifications identified as MIL–P–55110. Therefore, existing master drawings or OEM documents referencing MIL–P–55110 need not be revised, updated, or changed to make reference to MIL–PRF–55110 in order for this specification to be used.

6.6.4 Reference to superseded specifications. Superseded specifications are listed below.

a. MIL–P–55110 including:
   (1) MIL–P–55110C, dated 26 April 1978.
      (a) MIL–P–55110C with Amendment 1, dated 18 July 1978.
      (b) MIL–P–55110C with Amendment 2, dated 27 August 1979.
      (c) MIL–P–55110C with Amendment 3, dated 16 October 1980.
      (d) MIL–P–55110C with Amendment 4, dated 28 June 1982.
      (e) MIL–P–55110C with Amendment 5, dated 28 March 1984.
   (2) MIL–P–55110D, dated 31 December 1984.
      (a) MIL–P–55110D with Amendment 1, dated 6 March 1987.
      (b) MIL–P–55110D with Interim Amendment 2 (USAF), dated 22 April 1988.
      (c) MIL–P–55110D with Amendment 3, dated 18 May 1989.
      (d) MIL–P–55110D with Amendment 4, dated 2 December 1990.
   (3) MIL–P–55110E, dated 22 December 1993.
   (4) MIL–PRF–55110E, dated 29 September 1995.
   (5) MIL–PRF–55110F, dated 31 May 1997.
      (a) MIL–PRF–55110F with Amendment 1, dated 27 November 1998.
   (6) MIL–PRF–55110G, dated 11 December 2005.
      (a) MIL–PRF–55110G with Amendment 1, dated 2 July 2006.
      (b) MIL–PRF–55110G with Amendment 2, dated 2 August 2007.
      (c) MIL–PRF–55110G with Amendment 3, dated 29 February 2008.
   (7) MIL–PRF–55110H, dated 15 September 2014.

b. MIL–P–55640 including:
   (1) MIL–P–55640(EL), dated 6 February 1969.
   (2) MIL–P–55640A, dated 29 October 1970.
      (a) MIL–P–55640A with Amendment 1, dated 14 October 1971.
      (b) MIL–P–55640A with Amendment 2, dated 4 April 1975.

c. MIL–P–82585(OS), dated 24 February 1970.

d. MIL–P–55424(ER), dated 1 June 1965.

e. MIL–P–22629(OS), dated 10 March 1964.

f. MIL–P–21193(NOrd), dated 13 January 1958.

6.7 Automatic update notification. An electronic mail notification option is available to registered ASSIST users. If you do not receive an electronic mail message that an amendment or revision of this document has been completed, information pertaining to how to make use of this option within ASSIST may be obtained from DLA Land and Maritime, ATTN: VQE, P.O. Box 3990, Columbus, Ohio 43218–3990, or by e-mail to 5998.Qualifications@dla.mil, or at Universal Resource Locator (URL) https://LandandMaritimeApps.dla.mil/offices/sourcing_and_qualification.

6.8 Subject term (key word) listing.

Design standard
Master drawing
Qualified Manufacturer List (QML)
Qualified Product List (QPL)
Test coupon

6.9 Amendment notations. The margins of this specification are marked with vertical lines to indicate modifications generated by this amendment. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations.

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PRODUCT ASSURANCE (PERFORMANCE AND VERIFICATION) REQUIREMENTS FOR QUALIFIED PRODUCTS LIST LEVEL

A.1 SCOPE

A.1.1 Scope. This appendix contains the requirements and procedures for manufacturers using the traditional QPL method of product assurance (performance and verification inspection) for printed wiring boards covered by this specification. This appendix is a mandatory part of the specification when QPL compliance is required. The information contained herein is intended for compliance.

A.2 APPLICABLE DOCUMENTS

A.2.1 General. The documents listed in this section are specified in sections A.3 and A.4 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections A.3 and A.4 of this specification, whether or not they are listed.

A.2.2 Government documents.

A.2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

MIL–PRF–31032 – Printed Circuit Board/Printed Wiring Board, General Specification for.

(Copies of these documents are online at http://quicksearch.dla.mil.)

A.2.3 Non-Government publications. The following documents form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents are those cited in the solicitation or contract.

ASTM INTERNATIONAL (ASTM)

ASTM B567 – Standard Test Method for Measurement of Coating Thickness by the Beta Backscatter Method.
ASTM B568 – Standard Test Method for Measurement of Coating Thickness by X-Ray Spectrometry.

(Copies of these documents are online at http://www.astm.org.)

IPC – ASSOCIATION CONNECTING ELECTRONICS INDUSTRIES (IPC)

IPC–2220	–	Design Standards Series.
IPC–2221	–	Printed Board Design, Generic Standard on.
IPC–A–600	–	Acceptability of Printed Boards.
IPC–OI–645	–	Standard for Visual Optical Inspection Aids.
IPC–TM–650	–	Test Methods Manual.
IPC–7095	–	Design and Assembly Process Implementation for BGAs.
IPC–9252	–	Requirements for Electrical Testing of Unpopulated Printed Boards.

(Copies of these documents are online at http://www.ipc.org.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

A.2.4 Order of precedence. Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

A.3 REQUIREMENTS

A.3.1 General. The performance requirements contained in this section, although sometimes determined by examination of sampled printed wiring boards or test coupons, apply to all deliverable printed wiring boards.

A.3.1.1 Master drawing (see A.6.2.1.c). Printed wiring boards delivered under this specification shall be of the material, design, and construction specified on the applicable master drawing. For the purposes of this appendix, when the term "specified" is used without additional reference to a specific location or document, the intended reference shall be to the applicable master drawing. If individual design details are not specified on the applicable master drawing, then the baseline design parameters shall be as detailed in the design standard that was used to design the printed wiring board (see A.3.3).

A.3.2 Qualification. Printed wiring boards furnished under this appendix shall be products that are authorized by the qualifying activity for listing on the applicable QPL at the time of award of contract (see A.4.5 and A.6.3).

A.3.3 Design (see A.6.2.1.d). Printed wiring boards shall be of the design as specified (see A.3.1.1). Unless otherwise specified, if individual design details are not specified on the applicable master drawing, then the baseline design parameters to be use for acceptability of finished product requirements shall be as detailed in the design standard that was used to design the printed wiring board. If no design standard is specified on the master drawing or the appropriate design standard cannot be determined, then the default design shall be performance class 3 of IPC–2221.

A.3.3.1 Test coupons. Test coupon design shall be in accordance with the applicable design standard specified (see A.3.1.1) and herein. Test coupon placement and quantity on a production panel shall be in accordance with the requirements of appendix H. Test coupon selection and usage shall be determined by the manufacturer in order to meet the in-process, groups A and B inspection requirements herein. NOTE: Test coupon design shall be as specified in the applicable design standard or herein, and shall reflect worst case design conditions of the printed wiring board(s) they represent.

A.3.4 Material. The printed wiring boards shall be constructed of material as specified (see A.3.1.1). When a definite material is not specified on the applicable master drawing, a material shall be used that will enable the printed wiring board to meet the performance requirements of this specification. Acceptance or approval of any material shall not be construed as a guaranty of the acceptance of the finished printed wiring board.

A.3.4.1 Pure tin. Unless otherwise specified (see A.3.1.1), the use of pure tin, as an underplate or final finish, is prohibited both internally and externally. Tin content of printed board finishes and solder shall not exceed 97 percent, by mass. Tin shall be alloyed with a minimum of 3 percent lead, by mass (see A.6.8).

A.3.4.2 Recycled, recovered, environmentally preferable, or biobased materials. Recycled, recovered, environmentally preferable, or biobased materials should be used to the maximum extent possible, provided that the material meets or exceeds the operational and maintenance requirements, and promotes economically advantageous life cycle costs.

A.3.5 External visual and dimensional requirements. The finished printed wiring boards shall meet the visual and dimensional requirements specified in A.3.1.1 and A.3.5.1 through A.3.5.5.3. Scratches, dents, and tool marks shall not bridge or expose signal conductors, expose base metal, expose or disrupt reinforcement fibers, reduce dielectric properties, or reduce spacing below the minimum requirements herein. Appendix F contains figures and illustrations that can aid in the visualization of externally observable accept/reject conditions of printed wiring boards or test specimens. If a condition is not addressed herein or specified on the master drawing, it shall comply with the class 3 criteria of IPC–A–600.

A.3.5.1 Base materials.

A.3.5.1.1 Edges of base material. Burrs, crazing, and nicks along the edges of printed wiring boards, including edges of cutouts and edges of non-plated-though holes, shall be acceptable provided the penetration does not reduce the edge spacing by more than 50 percent of the edge spacing specified (see A.3.1.1) or .10 inch (2.5 mm), whichever is smaller. If no requirement for edge spacing is specified (see A.3.1.1), these types of penetrations shall not exceed .10 inch (2.5 mm). For haloing, the distance between the penetration and the nearest conductive feature shall not be less than the minimum lateral conductor spacing, or .004 inch (0.1 mm) if not specified. Inspection panels that are partially routed with breakaway tabs or scored for printed board or test coupon removal shall meet the de-panelization requirements specified (see A.3.1.1). Loose metallic burrs on the edges of base material shall not be acceptable.

A.3.5.1.2 Surface imperfections. Imperfections on the surface of the base material such as blistering, burrs, cuts, dents, foreign materials, gouges, nicks, pits, resin scorched areas, resin starved areas, scratches, tool marks, variations in color such as white spots or black spots, or other visual defects detrimental to the performance of the base material shall be acceptable in localized concentrations providing the following conditions are met:

a. The imperfection does not bridge between conductors (weave texture may bridge conductors).

b. The dielectric spacing between the imperfection and conductors does not reduce conductor spacing below the specified minimum requirements (see A.3.1.1).

A.3.5.1.2.1 Exposed or disrupted fibers. Exposed or disrupted reinforcement fibers on the horizontal surface of the printed board shall not bridge conductors and shall not reduce the conductor spacing below the minimum conductor spacing requirements. Unless otherwise specified, weave texture (reinforcement texture) or weave exposure (exposed reinforcement material fibers) by mechanical fabrication operations shall be acceptable provided they meet the exposed or disrupted reinforcement fiber requirements.

A.3.5.1.2.2 Surface pits and voids. Surface pits and voids in the base material shall be acceptable providing the following conditions are met:

a. Surface pits or voids are no bigger than .031 inch (0.8 mm) in the longest dimension.

b. The surface pits or voids do not bridge conductors.

c. The total area of all surface pits or voids does not exceed five percent of the total printed board area.

d. The surface pit or void does not affect the performance of the base material.

A.3.5.1.3 Subsurface imperfections (see A.6.8). Imperfections below the surface of the base material such as blistering, haloing, and delamination variations in color such as white spots or black spots, or other visual defects detrimental to the performance of the base material shall be acceptable in localized concentrations providing the following conditions are met:

a. The imperfection is translucent.

b. The imperfection does not bridge more than 25 percent of the distance between conductors or plated-through holes. No more than two percent of the printed wiring board area on each side shall be affected.

c. The imperfection does not reduce conductor spacing between adjacent conductors below the minimum requirements specified (see A.3.1.1).

d. The imperfection does not propagate as a result of testing (such as rework simulation, thermal stress, or thermal shock).

e. Color variations or mottled appearance in bond enhancement treatments shall be acceptable. Random areas of missing bond enhancement treatment shall not exceed 10 percent of the total conductor surface area of the affected layer.

A.3.5.1.3.1 Foreign inclusions. Foreign inclusions shall be acceptable provided they comply with the following:

a. The foreign inclusions are translucent.

b. The foreign inclusion is located at least .010 inch (0.25 mm) from the nearest conductor.

c. The foreign inclusion does not reduce the spacing between conductors below the minimum conductor spacing specified (see A.3.1.1). If not specified, the inclusion shall not reduce the conductor spacing by more than 25 percent.

d. The foreign inclusions longest dimension is no greater than .031 inch (0.8 mm) in circuitry areas. Inclusions in non-circuitry areas have no maximum dimension requirement.

e. When the base material specification allows for more or larger inclusions, those inclusions are allowed in the finished printed board, up to the size and quantity defined by the base material specification provided that the inclusion does not violate the conductor spacing requirements of A.3.5.1.3.c.

A.3.5.1.3.2 Subsurface spots. Subsurface spots shall be acceptable provided they comply with the following:

a. The spots are translucent.

b. The spots are known to be weave texture and not delamination or disbonding.

c. The spots are isolated white spots that do not propagate as a result of any soldering operation (gelation particles are acceptable regardless of location).

A.3.5.1.3.3 Measling and crazing. Measling and crazing shall not exceed the class 3 acceptable requirements specified in IPC–A–600 for bare printed wiring boards.

A.3.5.2 Conductor pattern.

A.3.5.2.1 Bonding of conductor to base material and lifted lands. There shall be no peeling or lifting of the conductor pattern (lands or conductors) the base material on the deliverable, non-stressed printed wiring board. (NOTE: See A.3.6.2.4 for allowances for the acceptable lifting of lands following rework simulation, solder float thermal stress, and thermal shock testing.)

A.3.5.2.2 Conductor finish. The conductor finish shall be as specified. A conductor finish plating or coating material shall be used that enables the printed wiring board to meet all of the performance requirements of this specification. Unless otherwise specified (see A.3.1.1), the following conductor finish conditions shall apply.

A.3.5.2.2.1 Coverage.

A.3.5.2.2.1.1 Metallic coatings or platings. The conductor finish plating or coating shall cover the basis metal of the conductive pattern. There shall be no evidence of any flaking, lifting, or separation of conductor finish plating or coating from the surface of the conductive pattern.

A.3.5.2.2.1.2 Tin alloys, reflowed tin-lead, or solder coated surfaces. Design requiring unfused tin-lead plating as a final conductor finish coverage, the thickness shall be as specified (see A.3.1.1 and A.3.3). Coverage of a conductor by solder does not apply to the vertical conductor edges.

A.3.5.2.2.1.2.1 Dewetting. For tin alloys, reflowed tin–lead, or solder coated surfaces, a maximum of five percent of dewetting is permitted on any conductive surface where a solder connection will be required.

A.3.5.2.2.1.2.2 Nonwetting. For tin alloys, reflowed tin–lead, or solder coated surfaces, nonwetting is not permitted on any conductive surface where a solder connection will be required. Absence of solder on the vertical sides of lands shall be acceptable.

A.3.5.2.2.2 Conductor finish voids in plated-through holes. The conductor finish plating and coating shall not have voids in plated-through holes that exceed the following limits:

a. No more than one final finish void in any plated-through hole.

b. Not more than 5 percent of the plated-through holes shall have conductor finish voids.

c. Any conductor finish void present is not more than 5 percent of the plated-through holes length.

d. Any conductor finish void present is less than 90 degrees of the circumference of the plated-through hole.

A.3.5.2.2.3 Edge board contacts. Unless otherwise specified, these requirements apply to the critical contact area. The critical contact area for edge board contacts shall be as specified.

a. Defects or surface imperfections in the edge board contact finish shall not expose base metal in critical contact area.

b. There shall be no nodules or metal bumps in the edge board contact finish in the critical contact area.

c. Pits, dents, or depressions in the edge board contact finish shall not exceed .0059 inch (0.15 mm) in their longest dimension. There shall be no more than three occurrences for each edge board contact, and no more than 30 percent of the contacts shall be affected.

A.3.5.2.2.4 Plating junctions (typical of edge board contacts). There shall be no exposed copper in the junction of metallic conductor finish platings or coatings. An overlap of metallic conductor finish platings or coatings shall be acceptable if less than .031 inch (0.8 mm) in length. When both solder coating and gold plating are present at a plating junction, a discolored or gray-black area at that plating overlap zone shall be acceptable.

A.3.5.2.2.5 Solder mask. Unless otherwise specified, on designs using solder mask over bare conductors, it shall be acceptable to have up to .010 inch (0.25 mm) of exposed base metal at the interface between the solder mask and the basis metal conductor finish.

A.3.5.2.2.6 Whiskers. There shall be no whiskers of solder or other conductor finish on the surface of the conductive pattern.

A.3.5.2.3 Conductor pattern imperfections (see figures F–1 and F–2). The conductor pattern shall contain no cracks, splits, or tears. Imperfections on conductor patterns shall be acceptable provided they do not exceed the defect requirements specified herein.

A.3.5.2.3.1 Miscellaneous imperfections. Unless otherwise specified (see A.3.1.1), any combination of edge roughness or conductor nicks exposing the base material shall not reduce each conductor trace width more than 20 percent of its minimum specified width.

A.3.5.2.3.2 Cuts and scratches. A cut or scratch of any length or width is permissible on ground or voltage planes, provided the dielectric is not exposed. Cuts and scratches on non-critical conductor traces may be of any length, but no deeper than 20 percent of the total conductor thickness. Cuts and scratches on conductor traces identified as critical shall be no longer than .50 inch (12.7 mm) or 10 percent of a conductor trace length, whichever is less and no deeper than 20 percent of the total conductor thickness.

A.3.5.2.3.3 Dents. A dent of any length or width on ground planes shall be acceptable provided the metal surface is not torn. Dents on conductive patterns may be of any length, but no deeper than .0005 inch (0.013 mm).

A.3.5.2.3.4 Pinholes. Pinholes in ground or voltage planes in non-critical areas shall be acceptable provided they have no single diameter greater than .040 inch (1.0 mm) and do not exceed four for each 1.0 inch (25.4 mm) diameter. Pinholes in a conductive pattern shall be acceptable, provided they do not reduce the width of a conductive pattern by 20 percent. Pinholes shall be limited to no more than one for each 1.0 inch (25.4 mm) of conductive length.

A.3.5.2.3.5 Pits. Pits in ground or voltage planes shall be acceptable provided they do not exceed 25 percent of the surface area. Any pit in the conductive pattern is acceptable provided the outline dimension does not exceed 20 percent of the conductor trace width and there is no more than one pit for each 1.0 inch (25.4 mm) of the conductor trace length.

A.3.5.2.3.6 Superfluous metal. Unless otherwise specified, small particles of metal such as extraneous copper, extraneous metal, or subsequent plating after etching that remains affixed to areas that are intended to be free of conductive material shall be acceptable providing the following conditions are met:

a. The conductive particle is no closer than .005 inch (0.13 mm) to the nearest conductor.

b. The conductive particle does not reduce the spacing between adjacent conductors to below the minimum spacing specified (A.3.1.1) or .005 inch (0.13 mm) when not specified.

c. The conductive particle is smaller than .005 inch (0.13 mm) at its greatest diameter or length.

d. The conductive particle does not affect the electrical parameters of the printed wiring board.

A.3.5.2.4 Conductor width and spacing.

A.3.5.2.4.1 Conductor spacing (see figure F–3). The conductor spacing, including tolerance, shall be as specified (see A.3.1.1). The minimum edge spacing shall be as specified (see A.3.1.1). Unless otherwise specified, if no conductor spacing tolerance is specified, a reduction in the conductor spacing of 10 percent above the specified spacing, due to isolated defects or misregistration, shall be considered acceptable.

A.3.5.2.4.2 Conductor width. The conductor width(s) shall be as specified (see A.3.1.1). Allowable reduction in the conductor width, due to isolated defects or misregistration, shall be in accordance with A.3.5.2.3.

A.3.5.2.5 Lands for component mounting. The lands to be used for component mounting shall be as specified. Imperfections on component hole lands, surface mount lands, or wire bond pads shall be acceptable provided they do not exceed the defect allowance requirements specified herein.

A.3.5.2.5.1 Component hole lands (see figures F–4 and F–5). The minimum external annular ring shall be as specified (see A.3.1.1). If not specified on the applicable master drawing, the minimum external annular ring shall not be less than the value specified in the IPC's 2220 series of documents for the design of rigid printed boards. On the date of publication of this document, the minimum external annular ring dimension is .002 inch (0.05 mm) for plated through holes and .006 inch (0.15 mm) for unsupported holes. Unless otherwise specified, the external annular ring may have, in isolated areas, a 20 percent reduction of the minimum external annular ring specified (see A.3.1.1), due to defects such as pits, dents, nicks, and pinholes. Hole breakout or misregistration shall not reduce the land-to-conductor junction below the specified minimum conductor width. No more than 20 percent of the annular ring circumference (72 degrees) may be affected.

A.3.5.2.5.2 Rectangular surface mount lands (see figure F–6). Defects such as nicks, dents, and pin holes along the external edge of the land shall not exceed 20 percent of either the length or width of the land and shall not encroach the pristine area, which is defined by the central 80 percent of the land width by 80 percent of the land length as shown on figure F–6. Defects internal to the land shall not exceed 10 percent of the length or width of the land and shall remain outside of the pristine area of the surface mount land. Electrical test probe "witness" marks are allowed within the pristine area.

A.3.5.2.5.3 Round surface mount lands (BGA pads) (see figure F–7). Defects such as nick, dents, and pin holes along the edge of the land shall not radially extend towards the center of the land by more than 10 percent of the diameter of the land and shall not extend more than 20 percent around the circumference of the land as shown on figure F–7. There shall be no defects within the pristine area which is defined by the central 80 percent of the land diameter. Electrical test probe "witness" marks are allowed within the pristine area.

A.3.5.2.5.4 Wire bond pads. The maximum conductor finish roughness (surface roughness) for pads or areas designated for wire bonding shall be no greater than 31 micro inches (0.8 micrometers). Unless otherwise specified, the wire bond pad bonding area shall be defined as the pristine area as shown on figure F–6 for rectangular pads or figure F–7 for round pads. There shall be no pits, nodules, scratches, electrical test probe "witness"' marks, or other defects in the pristine area that exceed the surface roughness limits.

A.3.5.2.6 Holes for interlayer connections. The external annular ring of holes used for interlayer connections shall be as specified. Unless otherwise specified, the external annular ring may have, in isolated areas, a 20 percent reduction of the specified minimum external annular ring due to defects such as dents, pinholes, pits, or nicks. Unless otherwise specified, plated-through holes identified as vias can have a maximum of 90 degrees of hole breakout if the breakout does not occur at the conductor to land intersection.

A.3.5.2.7 Registration, external.

A.3.5.2.7.1 Component hole lands. The registration of component hole lands shall be as specified (see A.3.1.1).

A.3.5.2.7.2 Rectangular surface mount lands. The registration of rectangular surface mount lands shall be as specified (see A.3.1.1).

A.3.5.2.7.3 Round surface mount (BGA) lands. Round surface mount lands, such as Ball Grid Array (BGA) lands, using copper–defined lands, solder mask-defined lands, owthor solder dam designs shall comply with IPC–7095.

A.3.5.2.8 Via cap copper plating. Via cap copper plating shall meet the requirements of A.3.5.5.

A.3.5.3 Dimensional requirements (interface and physical dimension). The finished printed wiring board shall meet the interface and physical dimension requirements specified. The dimensional requirements include items such as the conductor pattern including component lands and terminals, cutouts, overall board thickness, periphery, and other design features as specified (see A.3.1.1). In the event that a dimensional characteristic is not specified, the applicable class 3 of IPC–2221 design default for that characteristic shall apply.

A.3.5.3.1 Ball grid array (BGA) lands. BGA lands using copper–defined lands shall comply with the class 3 acceptable conditions of IPC–A–600.

A.3.5.3.2 Conductor pattern feature accuracy. Conductor pattern feature accuracy shall be as specified.

A.3.5.3.3 Edge board contacts edge condition. The, end, or beveled edge of edge board contacts, shall be smooth with no burrs, roughness, or lifted plating. There shall be no separation of the edge board contacts from the base material or any loose reinforcement fibers on the beveled edge. Exposed copper on the end, or beveled edge of the edge board contact, shall be acceptable. Conductor finish plating or coating shall comply with the requirements of A.3.5.2.2.

A.3.5.3.4 Hole pattern accuracy. The accuracy of the hole pattern (sizes and locations) on the printed wiring board shall be as specified (see A.3.1.1).

A.3.5.3.5 Hole size and locations. The hole size and tolerance shall be as specified (see A.3.1.1). Unless otherwise specified, hole size tolerance shall be applied after plating. Hole roughness, nodules, or rough plating in plated–through holes shall not reduce the hole diameter below the minimum limits specified. The locations of holes on the printed wiring board shall be as specified (see A.3.1.1).

A.3.5.3.6 Registration, external (method I). Registration of external lands shall be satisfied if the external layers meet the specified annular ring requirements (see A.3.1.1 and A.3.5.2.7). Misregistration shall not reduce the minimum external annular ring below its specified limits.

A.3.5.4 Solder mask (when applicable). The cured solder mask shall not exhibit any chalking, crazing, peeling, skipping, softening, spalling, swelling, or wrinkles in excess of the limits specified herein. Unless otherwise specified (see A.3.1.1), the solder mask requirements specified in A.3.5.4.1 through A.3.5.4.5 shall apply.

A.3.5.4.1 BGA lands. BGA lands using solder mask–defined lands or solder dam designs shall comply with the class 3 acceptable conditions of IPC–A–600.

A.3.5.4.2 Coverage. Solder mask coverage imperfections (such as blisters, delaminations, pits, skips, wrinkles, and voids) shall be acceptable providing the imperfection meets all of the following:

a. The solder mask imperfection shall not expose two adjacent conductors whose spacing is less than the electrical spacing required for the voltage range and environmental condition specified in the applicable design standard.

b. In areas containing parallel conductors, the solder mask imperfection shall not expose two isolated conductors whose spacing is less than .020 inch (0.5 mm) unless one of the conductors is a test point or other feature area which is purposely left uncoated for subsequent operations.

c. The exposed conductor shall not be bare copper.

d. The solder mask imperfection does not expose via holes that are to be tented or filled by solder mask.

e. Bubbles, pits or voids in non-conductor areas shall be acceptable if they have adherent edges and do not exhibit blistering or lifting in excess of that allowed in A.3.7.4.7.

f. For designs using solder mask over bare conductors, it shall be acceptable to have up to .010 inch (0.25 mm) of exposed base metal at the interface between the solder mask and the basis metal conductor finish.

A.3.5.4.3 Discoloration. Discoloration of metallic surfaces under the cured solder mask shall be acceptable.

A.3.5.4.4 Registration (see figures F–8 and F–9). The solder mask shall be registered to the land or terminal patterns in such a manner as to meet the requirements specified (see A.3.1.1). If no requirements are specified, the following apply:

a. For plated-through holes and vias, the following shall apply:

   (1) Solder mask misregistration onto plated-through component hole lands (plated-through holes to which solder connections are to be made) shall not reduce the external annular ring below the specified minimum requirements.

   (2) Solder mask shall not encroach into plated-through hole barrels or onto other surface features (such as edge board contacts or lands of unsupported holes) to which solder connections will be made.

   (3) Solder mask is permitted in plated holes or vias in which no lead is to be soldered.

b. For surface mount lands with no plated-through holes, the following shall apply:

   (1) For lands with a pitch of .050 inch (1.27 mm) or greater, solder mask encroachment is on one side of land only and does not exceed .002 inch (0.050 mm).

   (2) For lands with a pitch less than .050 inch (1.27 mm), solder mask encroachment is on one side of land only and does not exceed .001 inch (0.025 mm).

c. For ball grid array lands, the following shall apply:

(1) If the land is solder mask defined, allowable misregistration of the solder mask causes breakout of the land of not more than 90 degrees.

(2) If the land is copper defined, the solder mask shall not encroach onto the land. Solder mask on the land-to-via connecting conductor shall be acceptable.

(3) If solder mask dam is specified, the dam remains in place with the conductor to the via covered.

d. Edge-board contacts and test points which are intended for assembly testing shall be free of solder mask unless a partial coverage allowance is specified.

A.3.5.4.5 Thickness. The solder mask thickness shall be as specified (see A.3.1.1).

A.3.5.4.6 Solder mask cure. The cured solder mask coating shall not exhibit tackiness, blistering, or delamination in excess of that allowed in A.3.5.4.2.

A.3.5.4.7 Soda straw voids. There shall be no visible soda straw voids between the solder mask and the printed board base material surface and the edges of the conductor patterns.

A.3.5.5 Via protection.

A.3.5.5.1 Copper cap plating (filled via) (see figure F–10). When the design requires the copper cap plating of filled vias (see A.3.1.1), all vias required to be protected shall be completely covered by the cap plating, unless covered by soldermask. Visually discernable protrusions (bumps) and depressions (dimples) in the copper plating over filled vias shall be acceptable providing they meet the requirements of A.3.6.2.2.3. Voids in the copper cap plating over the filled portion of the via shall not be acceptable, unless covered by soldermask.

A.3.5.5.2 Solder mask plugging. When the design requires that through vias be plugged by solder mask, the percentage of plugging shall be as specified (see A.3.1.1). Voids in the solder mask within the plugged hole shall be as specified (see A.3.1.1).

A.3.5.5.3 Solder mask tenting (filled or unfilled via) (see figure F–11). When the design requires the tenting of solder mask over filled or unfilled vias (see A.3.1.1), all vias required to be protected shall be completely covered by solder mask. Voids in the solder mask over the via exposing the hole shall not be acceptable.

A.3.6 Plated hole structural requirements. When plated hole structures are examined in cross-section, the microsectioned test specimen (which includes plated-through holes, blind vias, buried vias, low aspect ratio blind vias, and microvias) shall meet the requirements of A.3.6.1 through A.3.6.7.2. Blind, buried, low aspect ratio blind vias, microvias, and through vias shall meet the requirements of plated-through holes. Non-stressed specimens refers to samples in the as received condition. Stressed specimens are samples that have been subjected to rework simulation, resistance to soldering heat, or thermal shock testing. Appendix G contains figures, illustrations, and photographs that can aid in the visualization of internally observable accept/reject conditions of microsectioned test specimens. If a condition is not addressed herein or specified on the master drawing, it shall comply with the class 3 criteria of IPC–A–600.

NOTE: The thermal zones of plated hole structures are shown on figures G–1 and G–2.

A.3.6.1 Base material. Base materials shall be of such quality as to enable the printed wiring board to meet all of the performance requirements of this specification. Unless otherwise specified, the base material imperfections listed in A.3.6.1.1 through A.3.6.1.6 shall be evaluated.

A.3.6.1.1 Cracks and voids. Base material cracks shall be classified and treated as laminate voids.

A.3.6.1.1.1 Non-stressed specimens. Laminate voids with the longest dimension of .003 inch (0.08 mm) or less shall be acceptable.

A.3.6.1.1.2 Stressed specimens (see figures G–1 and G–2). Laminate voids are not evaluated in zone A (the thermal zone of stressed plated hole structures). Laminate cracks and voids located wholly in zone A shall be acceptable. Laminate cracks and voids that originate in zone A and encroach into zone B shall not exceed a length of .003 inch (0.08 mm) into zone B. Laminate cracks and voids in zone B (the laminate evaluation area of stressed plated hole structures) with the longest dimension of .003 inch (0.08 mm) or less shall be acceptable provided the conductor spacing is not reduced below the minimum dielectric spacing requirements, laterally or vertically, as specified (see A.3.1.1). Multiple laminate cracks and voids located between two adjacent plated-through holes shall not have a combined length in excess of .003 inch (0.08 mm), shall not bridge adjacent uncommon conductors, and shall not reduce dielectric spacing, either laterally or vertically, below the minimum specified spacing.

A.3.6.1.2 Delamination. Printed wiring boards shall have no delaminations in excess of that allowed in A.3.5.1.3.

A.3.6.1.3 Dielectric layer thickness (see figure G–3). The minimum dielectric thickness separating the conductor layers of the printed wiring boards shall be as specified (see A.3.1.1). If not specified on the master drawing, the minimum dielectric spacing base materials should not be less than the value specified in the IPC's 2220 series of documents for the design of rigid printed boards. On the date of publication of this document, the minimum dielectric spacing dimension for rigid base materials shall not be less than .0035 inch (0.089 mm).

A.3.6.1.4 Dielectric thickness for heatsink planes (see figures G–4 and G–5). Defects such as radial cracks, wicking, or voids in the dielectric material used to insulate the heatsink plane, or metal core, from circuitry and plated through holes, shall not reduce by 75 percent the specified lateral spacing between adjacent conductive surfaces. If not specified on the master drawing, the minimum lateral spacing between adjacent conductive surfaces, nonfunctional lands, or plated-through hole and the heatsink plane should not be less than the value specified in the IPC's 2220 series of documents for the design of rigid printed boards. On the date of publication of this document, the minimum lateral spacing for heatsink planes shall not be less than .004 inch (0.10 mm). Wicking of copper and radial cracks from the plated–through hole edge into the hole–fill insulation material shall not exceed .003 inch (0.08 mm).

A.3.6.1.5 Hole wall to dielectric separation (resin recession) (see figures G–1 and G–2).

A.3.6.1.5.1 Non-stressed specimens. Any separation between the vertical edge of the dielectric material and the outer surface of the plated hole barrel wall (resin recession) shall be permitted provided the maximum depth as measured from the barrel wall does not exceed .003 inch (0.08 mm) and the resin recession on any side of the plated-through hole does not exceed 40 percent of the cumulative base material thickness (sum of the dielectric layer thickness being evaluated) on the side of the plated-through hole being evaluated.

A.3.6.1.5.2 Stressed specimens. Resin recession at the outer surface of the plated hole barrel wall shall be permitted and is not cause for rejection.

A.3.6.1.6 Via fill of blind and buried vias. Unless otherwise specified (see A.3.1.1), blind vias shall be at least 75 percent filled with the specified via fill material. Unless otherwise specified, buried vias shall be at least 95 percent filled with the specified via fill material.

A.3.6.2 Conductor pattern.

A.3.6.2.1 Conductor finish. A conductor finish plating or coating material shall be used that enables the printed wiring board to meet all of the performance requirements of this specification. Unless otherwise specified (see A.3.1.1), the following conductor finish conditions shall apply.

A.3.6.2.1.1 Dewetting. For tin alloys, reflowed tin-lead, or solder coated surfaces, a maximum of 5 percent of dewetting is permitted on any conductive surface where a solder connection will be required.

A.3.6.2.1.2 Nonwetting. For tin alloys, reflowed tin-lead, solder coated surfaces, nonwetting is not permitted on any conductive surface where a solder connection will be required. The absence of solder on the vertical sides of lands shall be acceptable.

A.3.6.2.1.3 Outgrowth and overhang. There shall be no outgrowth on the conductor edges when finished with fused tin-lead or solder coating. The maximum permissible outgrowth on conductor edges finished with surface finish metals other than tin-lead or solder shall be .001 inch (0.025 mm).

A.3.6.2.1.4 Protective finishes for internal metal cores or metal backing. The plating, coating, or surface treatment type and thickness of internal metal cores and metal backing materials shall be as specified (see A.3.1.1).

A.3.6.2.1.5 Thickness (plating or coating). The conductor finish plating or coating thickness shall be as specified (see A.3.1.1). If not specified on the applicable master drawing, the minimum conductor finish plating or coating thickness should not be less than the values specified in the IPC's 2220 series of documents for the design of rigid printed boards. On the date of publication of this document, those values are reproduced in table A–I. (Also see A.3.4.2 and A.3.5.2.6).

TABLE A–I. Conductor surface finish plating and coating thickness.

Material	Thickness, in inches 1/
Solder coat over base copper	Coverage and solderable 2/
Electrodeposited Tin-Lead, fused or solder coat	Coverage and solderable 2/
Electrodeposited Tin-Lead, unfused	.0003 (0.008 mm)
Organic Solderabilty Preservative (OSP) and high-temp OSP	Solderable 2/
Immersion silver (IAg)	Solderable 2/
Gold (for edge-board contacts and areas not to be soldered) (minimum)	.00005 (0.0013 mm)
Gold (on areas to be soldered) (maximum)	.000018 (0.00046 mm)
Gold (on areas to be wire bonded, ultrasonic) (minimum)	.000002 (0.00005 mm)
Gold (on areas to be wire bonded, thermosonic) (minimum)	.00003 (0.0008 mm)
Immersion gold (IAu)	.000002 to .000009 (0.00005 to 0.00023 mm)
Nickel (for edge-board contacts) (minimum)	.0001 (0.0025 mm)
Nickel (barrier to prevent formation of copper-tin compounds) (minimum)	.0002 (0.005 mm)
Electroless nickel, immersion gold (ENIG)	EN: .0001 to .0002 (0.0025 to 0.005 mm)
	IG: .0002 (0.005 mm)
Electroless nickel, electroless palladium, immersion gold (ENEPIG)	EN: .000118 (0.003 mm)
	EP: .000002 (0.00005 mm)
	IG: Coverage and solderable 2/
Direct Immersion Gold (DIG)	Solderable 2/

1/ The non-destructive plating and coating measurement techniques of A.4.8.1.6 shall be used when a plating or coating thickness is below .00005 inch (0.00125 mm).
2/ Solderability shall be in accordance with A.3.7.4.7.

A.3.6.2.2 Conductor thickness (see figure G–6). The conductor thickness shall be as specified (see A.3.1.1).

A.3.6.2.2.1 Conductors with copper plating (after processing). Conductors with copper plating are typical of external layers of multilayer designs and both external and internal layers of sequential laminated multilayer designs.

A.3.6.2.2.1.1 Minimum external conductor thickness (types 2, 3 and 4). The external conductor thickness shall be as specified (see A.3.1.1). When an external conductor thickness is specified, the conductor thickness (copper foil and copper plating) shall be equal to or greater than the specified thickness. When an external conductor thickness with tolerance is specified, the external conductor thickness (copper foil and copper plating) shall be within the specified tolerance for the specified thickness. If only a starting external metal foil weight requirement is specified, the thickness limits for conductors with plating shall meet the requirements of table A–II. If only final external metal foil weight requirement is specified, the limits for minimum conductor thickness shall be as defined by the procuring activity.

A.3.6.2.2.1.2 Planarized conductor surfaces (types 2, 3 and 4). Unless otherwise specified (see A.3.1.1), the final external conductor thickness of planarized layers will be less than the values in table A–II due to the reduction allowance of A.3.6.4.3.

TABLE A–II. Thickness of external conductors with copper plating after processing (not planarized).

Starting copper foil weight 1/	Foil thickness (minimum) 2/		Processing reduction allowance (maximum) 3/		Surface conductor thickness after plating (minimum)		Surface conductor thickness after plating and processing (minimum)	
	inch	(µm)	inch	(µm)	inch	(µm)	inch	(µm)
1/8	.00018	4.6	.00006	1.5	.00117	29.7	.00110	27.94
1/4	.0003	7.6	.00006	1.5	.00129	32.8	.00123	31.24
3/8	.00043	10.8	.00006	1.5	.00141	35.8	.00135	34.30
1/2	.0006	15.2	.00008	2	.00159	40.4	.00151	38.40
1	.0012	30.5	.00012	3	.0022	55.9	.00208	52.83
2	.00243	61.7	.00012	3	.00341	86.6	.00330	83.82
3	.00365	92.7	.00016	4	.00463	117.6	.00447	113.54
4	.00486	123.4	.00016	4	.00585	148.6	.00569	144.53

1/ The starting copper foil weight shall be as specified on the master drawing.
2/ This value is the low end of the allowed range minus the allowed 10 percent reduction for in accordance with the applicable foil specification. For foils with double-treated finishes, an addition 10 percent reduction shall be acceptable.
3/ The processing reduction allowance does not factor in any rework processing for copper foil weights below 1/2. For weights of 1/2 and above, the processing reduction allowance accounts for one rework process.

A.3.6.2.2.2 Conductors without copper plating (after processing).

A.3.6.2.2.2.1 Minimum external conductor thickness (types 1 and 2). The external conductor thickness shall be as specified (see A.3.1.1).

A.3.6.2.2.2.2 Minimum internal conductor thickness (types 3 and 4). The internal conductor thickness shall be as specified (see A.3.1.1). When a minimum conductor thickness is specified, the conductor thickness (metal foil only) shall be equal to, or greater than, the specified thickness. When a conductor thickness with tolerance is specified, the conductor thickness (metal foil only) shall be within the specified tolerance for the specified thickness. If only a starting metal foil weight requirement is specified, the limits for internal layer foil thickness after processing shall be in accordance with table A–III. If only final metal foil weight requirement is specified, the limits for minimum conductor thickness shall be as defined by the procuring activity.

A.3.6.2.2.3 Via cap plating. Via cap plating shall not be included in the surface copper measurement.

TABLE A–III. Thickness of conductors without copper plating (after processing).

Starting copper foil weight 1/	Foil thickness (minimum) 2/		Processing reduction allowance		Minimum surface conductor thickness (after processing)	
	inches	(µm)	inches	(µm)	Inches	(µm)
1/8	.00018	(4.6)	.00006	(1.5)	.00012	3.05
1/4	.0003	(7.6)	.00006	(1.5)	.00024	6.09
3/8	.00043	(10.9)	.00006	(1.5)	.00037	9.40
1/2	.0006	(15.2)	.00016	(4.0)	.00044	11.17
1	.00122	(30.9)	.00024	(6.0)	.00098	24.89
2	.00243	(61.7)	.00024	(6.0)	.00219	55.63
3	.00365	(92.7)	.00024	(6.0)	.00341	86.61
4	.00486	(123.4)	.00024	(6.0)	.00462	117.35

1/ The starting copper foil weight shall be as specified on the master drawing.
2/ This value is the low end of the allowed range minus the allowed 10 percent reduction for in accordance with the applicable foil specification. For double treat foil, reduce by another 10 percent (20 percent total).

A.3.6.2.3 Conductor width. The conductor width shall be as specified (see A.3.1.1).

A.3.6.2.3.1 Annular ring, internal (see figure G–7). The minimum annular ring for functional internal lands on types 3 and 4 printed wiring boards shall be as specified (see A.3.1.1). If not specified on the applicable master drawing, the minimum internal annular ring should not be less than the values specified in the IPC's 2220 series of documents for the design of rigid printed wiring boards. On the date of publication of this document, that value was listed as .002 inch (0.05 mm). Hole breakout shall not be acceptable.

A.3.6.2.3.2 Undercutting. Undercutting at each edge of the conductors shall not exceed the total thickness of the copper foil and plated copper.

A.3.6.2.4 Bonding of conductor to base material, lifted lands, and gaps under lands (see figure G–8).

A.3.6.2.4.1 Non-stressed specimens. There shall be no lifted lands, or evidence of lifted lands on the non-stressed test specimen. Open gaps between the land and the base material shall not be acceptable. When inspected in accordance with A.4.8.2 and lifted lands are present, the lot shall be 100 percent visually inspected in accordance with A.4.8.1 for separation of the lands from the base material. Gaps between the bottom of the land and the base material that have been filled by either conductive or non-conductive material shall be acceptable. Under land gaps shall not propagate due to testing.

A.3.6.2.4.2 Stressed specimens. After undergoing rework simulation, resistance to soldering heat, or thermal shock testing (see A.3.7.4.6, A.3.7.6.2, and A.3.7.6.3), the maximum allowed distance from the plane of the base material surface to the bottom of the edge of the land or pad shall be no greater than the total land thickness. The total land thickness is equal to the combined thickness of the metal foil and copper plating on that land.

A.3.6.3 Hole preparation prior to metallization.

A.3.6.3.1 Desmear (smear removal and hole cleaning) (see figures G–9 and G–10). When etchback is not specified (see A.3.1.1) on the applicable master drawing, the vertical faces of the internal conductors of the plated hole structure shall be cleaned to be free of resin smear. Lateral removal of base material from the hole wall shall not exceed .001 inch (0.03 mm). When desmear is used for hole metallization preparation, a negative etchback of .0005 inch (0.013 mm) maximum shall be acceptable.

A.3.6.3.2 Etchback (postive) (when specified, see A.3.1.1) (see figure G–11 and G–12). When specified (see A.3.1.1), holes that will be plated shall be processed for the lateral removal of resin and reinforcement material (woven glass or other media) from the internal conductors prior to plating. Unless otherwise specified (see A.3.1.1), etchback shall be a minimum of.0002 inch (0.005 mm) and no greater than the specified minimum internal annular ring or .002 inch (0.05 mm), whichever is less, with a preferred depth of .0005 inch (0.013 mm) when measured at the internal copper contact area protrusion (see figure G–11). The etchback shall be effective on at least the top or bottom (or both) surface of each internal conductor to provide at least a two (2) point contact with the subsequent hole plating (see figure G–12). Negative etchback is not acceptable when etchback is specified. Wicking shall meet the requirements of A.3.6.4.5.

A.3.6.4 Plated hole structure plating. Unless otherwise specified (see A.3.1.1), the copper plating thickness of plated hole structures includes to the hole wall, the hole knee, and the surface land of the plated-through hole. Via cap plating shall not be included in the wrap copper measurement.

A.3.6.4.1 Conductive material interfaces and separations (see A.7.5). The term conductive interfaces shall be used to describe the junction between the hole wall plating or coating and the surfaces of internal and external layers of copper or metal foil. The interface between platings and coating (electroless copper, direct metallization copper, nonmetallic conductive coatings, or vacuum deposited copper, and electrolytic copper, whether panel or pattern plated) shall also be considered a conductive interface. Separations in conductive interfaces shall be limited to the conditions listed herein.

A.3.6.4.1.1 Copper to copper interfaces (see figure G–13). Except along the vertical edge of the external copper foil there shall be no separations or contamination between the hole wall copper conductive interfaces. Conductive interface separations along the vertical edge of the external copper foil shall be acceptable.

A.3.6.4.1.2 Dissimilar metal interfaces (see figure G–14). For printed wiring board deigns containing metal cores with dissimilar metals (such as copper-invar-copper), contamination or separation at the conductive interface of dissimilar metals shall not exceed 20 percent of the thickness of the dissimilar metal.

A.3.6.4.1.3 Heat sink planes (see figure G–4). Unless otherwise specified (see A.3.1.1), when heat sink planes are used as electrically functioning circuit, they shall meet the requirements of A.3.6.4.

A.3.6.4.2 Plated hole structure copper plating thickness (when applicable) (see figures G–15, G–16, G–17, and G–18). The copper plating thickness of plated hole structures shall be as specified (see A.3.1.1). If not specified on the master drawing, the copper plating shall be in accordance with the thicknesses of table A–IV.

A.3.6.4.3 Wrap plating (see figure G–18). Unless otherwise specified, the wrap plating (plated-through hole continuous hole-knee-surface copper plating thickness shall be as specified (see A.3.1.1). If not specified, the wrap copper plating thickness shall be as specified in table A–IV. The wrap copper plating shall not be reduced below the specified minimum wrap copper plating thickness due to processing (etching, planarization, etc.).

TABLE A–IV. Plated hole structure copper plating thickness (hole wall and surface).

Design feature	Minimum average	Minimum thin area	Minimum wrap
Through holes	.001 (0.025 mm)	.0008 (0.020 mm)	.0005 (0.013 mm)
Blind vias	.001 (0.025 mm)	.0008 (0.020 mm)	.0005 (0.013 mm)
Buried vias where the core is greater than 2 layers in thickness	.001 (0.025 mm)	.0008 (0.020 mm)	.0005 (0.013 mm)
Buried vias where the core is only 2 layers in thickness	.0006 (0.015 mm)	.0005 (0.013 mm)	.0003 (0.008 mm)
Buried vias where the core is a single layer in thickness	.0005 (0.013 mm)	.0004 (0.010 mm)	.00025 (0.006 mm)
Microvias (blind or buried)	.0005 (0.013 mm)	.0004 (0.010 mm)	.00025 (0.006 mm)
Via cap (via protection plating)	.0005 (0.013 mm)		

A.3.6.4.4 Hole wall copper plating defects.

A.3.6.4.4.1 Plated hole structure wall deficiencies (see figures G–19 and G–20). Nodules, plating folds, or plated reinforcement material (glass fibers) that project into the copper plating shall be acceptable provided that the hole diameter and the hole wall copper thickness are not reduced below the limits specified (see A.3.1.1). Isolated areas of reduced copper thickness due to reinforcement material protrusions shall meet the minimum thickness requirements specified, when measured from the end of the protrusion to the edge of the hole plating.

A.3.6.4.4.2 Thin copper plating. Unless otherwise specified (see A.3.1.1), a 20 percent reduction of the specified hole wall copper plating thickness shall be acceptable if it is non-continuous (isolated; not more than 10 percent of the composite board thickness). Any hole wall copper plating less than 80 percent of the specified thickness shall be treated as a copper plating void in accordance with A.3.6.4.4.3. Wrap plating shall meet the requirements of A.3.6.4.3.

A.3.6.4.4.3 Copper plating voids (see figure G–21). The copper plating in the plated hole structure shall not exhibit any void in excess of the following:

a. There shall be no more than one plating void for each inspection panel, regardless of length or size.

b. There shall be no plating void in excess of 5 percent of the total printed wiring board thickness.

c. There shall be no plating voids evident at the interface of an internal conductive layer and plated hole wall.

Conductor finish plating or coating material between the base material and copper plating (i.e., between the hole wall copper plating and base material) is evidence of a void. Any plated–through hole exhibiting this condition shall be counted as having one void for each occurrence.

A.3.6.4.5 Wicking of copper plating (see figure G–22). When measured from the edge of the drilled hole, the wicking of copper plating into the base material shall not extend past the calculated allowable wicking limit provided this limit does not reduce the conductor spacing below the minimum clearance spacing requirements specified (see A.3.1.1). The maximum allowable wicking limit is calculated by adding a .003 inch (0.08 mm) allowance to the hole cleaning dielectric removal value (desmear or ecthback). See A.3.6.3.1 for dielectric removal value for desmear, or if applicable, A.3.1.1 and A.3.6.3.2 for the specified etchback value. The combination of the .003 inch (0.08 mm) allowance, the hole cleaning dielectric removal value, and any random drill gouges or tears caused by hole formation shall not exceed the calculated allowable wicking limit.

A.3.6.5 Miscellaneous hole and plating deficiencies. Barrel cracks, butt plating joints, circumferential separations, and corner cracks shall not be acceptable.

A.3.6.5.1 Metallic cracks (see figure G–23). There shall be no cracks in any plating, coating, or the internal layer conductive foils. Cracks in outer layer conductive foil shall be acceptable if they do not propagate into any plating or coating. Cracks shall not be acceptable in the copper plating.

A.3.6.5.2 Nail-heading. Nail-heading of conductors shall not exceed one and a half times the copper foil thickness.

A.3.6.6 Solder mask thickness (see figure G–24). The minimum solder mask thickness shall be as specified (see A.3.1.1). If not specified on the applicable master drawing, the minimum solder mask thickness should not be less than the values specified in the IPC's 2220 series of documents for the design of rigid printed wiring boards.

A.3.6.7 Via cap plating.

A.3.6.7.1 Thickness. For designs that specify copper plating for via protection, the minimum via cap plating thickness over filled vias shall be as specified. Unless otherwise specified (A.3.1.1), the minimum via cap copper plating thickness over filled vias shall be in accordance with the minimum wrap copper plating thickness specified in table A–IV.

A.3.6.7.2 Via cap plating imperfections (see figures G–25 and G–26). When cap plating of a filled via is specified (see A.3.1.1), voids in the plating over the via fill shall not be acceptable. Separation of the via cap plating to non conductive via fill material shall be acceptable. Separation of the via cap plating to underlying plating shall not be acceptable. Depressions (dimples) below the surface of the land shall be no greater than .003 inch (0.08 mm). Protrusions (bumps) of the cap plating above the surface of the land shall be no greater than .002 inch (0.05 mm).

A.3.7 Inspection requirements. The detailed requirements contained in this section, although determined by examination of sample printed wiring board test specimens (production printed wiring boards, test coupons, or microsectioned test coupons), apply to all deliverable printed wiring boards.

A.3.7.1 External visual and dimensional acceptability (of printed wiring boards). When examined as specified in A.4.8.1, the printed wiring boards shall be in accordance with the requirements specified in A.3.1.1 (master drawing), A.3.3 (design), A.3.4 (material), A.3.5 (visual and dimensional), A.3.8 (marking), A.3.10 (repair), and A.3.12 (workmanship).

A.3.7.2 Destructive physical analysis (DPA) by metallographic evaluation of printed board test specimens (microsection evaluation).

A.3.7.2.1 Non-stressed specimens (as received condition). After meeting the requirements of A.3.8 and A.3.12 when inspected in accordance with A.4.8.1, the non-stressed (as received) printed wiring board test specimen shall be microsectioned and inspected in accordance with A.4.8.2 and shall meet the requirements of A.3.1.1, A.3.3, and A.3.6.

A.3.7.2.2 Stressed specimens. The stressed printed wiring board test specimens (finished printed wiring boards, supporting test coupons, or qualification test specimens) shall be microsectioned and examined as specified in A.4.8.2, and shall be meet the requirements of A.3.1.1, A.3.3, and A.3.6.

A.3.7.2.3 Registration, internal.

A.3.7.2.3.1 Method II (by microsection). Unless otherwise specified (see A.3.1.1), when inspected as specified in A.4.8.2.4, the layer-to-layer pattern misregistration of internal lands shall not reduce the minimum annular ring below the limits specified (see A.3.1.1 and A.3.5.2.5.1).

A.3.7.2.3.2 Method III (by registration test coupons) (optional). Registration test coupons may have been designed into the printed wiring board by the design activity, or may be added to the inspection panel by the manufacturer to enhance testability (see A.4.8.2.4.2 and appendix H). To be usable for acceptance purposes, registration test coupons shall relate the actual grid location of each circuitry layer to all other circuitry layers and to the hole pattern accuracy required (see A.3.5.3.5) in each printed wiring board.

A.3.7.3 Chemical requirements.

A.3.7.3.1 Ionic contamination (cleanliness). When printed wiring boards are tested in accordance with A.4.8.3.1, the levels of ionic contamination shall be in accordance with the requirements of A.3.7.3.1.1 or A.3.7.3.1.2, as applicable. The sodium chloride salt equivalent ionic contamination test equipment specified in A.6.4.2 may be used in lieu of the method specified in A.4.8.3.1. When printed wiring boards are tested using the sodium chloride salt equivalent ionic contamination test equipment specified in A.6.4.2, the final value shall be less than equivalents of sodium chloride specified for the printed wiring board surface area tested.

A.3.7.3.1.1 Prior to the application of solder mask (see A.6.4). Unless otherwise specified (see A.3.1.1), the level of ionic contamination shall not exceed an equivalent of 10.06 micrograms/square inch (1.56 micrograms/square centimeter) of sodium chloride prior to the application of solder mask.

A.3.7.3.1.2 Completed inner layer prior to lamination (when specified, see A.3.1.1 and A.6.2.2.g). The levels of ionic contamination for completed inner layers prior to lamination shall be as specified.

A.3.7.3.1.3 Completed printed wiring boards (when specified, see A.3.1.1 and A.6.2.2.g). The levels of ionic contamination for completed printed wiring boards shall be as specified.

A.3.7.3.2 Resistance to solvents (marking inks or paints). After ink or paint based markings or legends are tested in accordance with A.4.8.3.2, any specified markings or legends which are missing in whole or in part, faded, smeared, or shifted (dislodged) to the extent that they cannot be readily identified shall constitute failure. A slight change in the color of ink or paint markings after the test shall be acceptable.

A.3.7.4 Physical requirements.

A.3.7.4.1 Adhesion, legend and marking. After legends or marking are tested in accordance with A.4.8.4.1, any specified legend or markings which are missing in whole or in part, faded, shifted (dislodged), or smeared to the extent that it is no longer legible shall constitute failure. A slight change in the color of ink or paint markings after the test shall be acceptable.

A.3.7.4.2 Adhesion, plating. When tested as specified in A.4.8.4.2, there shall be no plating particles or conductor patterns removed from the printed wiring board test specimen except for outgrowth.

A.3.7.4.3 Adhesion, solder mask. When tested as specified in A.4.8.4.3, the maximum percentage of cured solder mask lifted from the surface of the base material, conductors, and lands of the coated printed wiring board test specimen shall be in accordance with the following:

a. Bare copper or base material: Maximum percentage of lifting 0 percent.

b. Gold or nickel plating: Maximum percentage of lifting 5 percent.

c. Melting metals (tin-lead plating, solder coating, indium, bismuth, and others): Maximum percentage of lifting 10 percent.

A.3.7.4.4 Bow and twist. When tested as specified in A.4.8.4.4, the maximum allowable bow and twist of the printed wiring board shall be within the limits specified (see A.3.1.1). If not specified, the limits for bow and twist shall be 0.75 percent for designs that use surface mount components and 1.5 percent for all other designs.

A.3.7.4.5 Conductor edge outgrowth. For starting copper foil weight greater than 3 ounces per square foot only.

A.3.7.4.5.1 Conductors covered with solder. When the printed wiring board test specimen is examined as specified in A.4.8.1, there shall be no outgrowth of the solder coating on the conductor edges.

A.3.7.4.5.2 Conductors covered with metals other than solder. After undergoing the test as specified in A.4.8.4.5, the printed wiring board test specimen shall be examined as specified in A.4.8.1 and the maximum permissible outgrowth on conductors shall be .001 inch (0.03 mm).

A.3.7.4.6 Rework simulation. Rework simulation is not applicable for printed wiring board designs that do not use any through-holes (unsupported or plated) for component attachment.

A.3.7.4.6.1 Type 1 with unsupported holes (bond strength). After undergoing the test specified in A.4.8.4.6, the unsupported land shall withstand 5 pounds (2.27 Kg) pull or 500 PSI (3.4 MPa), whichever is less.

A.3.7.4.6.2 Types 2, 3 and 4 with plated hole structures. After undergoing the test specified in A.4.8.4.6, the type 2, 3, or 4 printed wiring board test specimens shall meet the following requirements:

a. External visual and dimensional inspection: When inspected as specified in A.4.8.1, there shall be no evidence of blistering, crazing, or delamination in excess of that allowed in A.3.5.

b. Internal visual and dimensional inspection: After the printed wiring board test specimen is microsectioned and inspected in accordance with A.4.8.2, the requirements specified in A.3.1.1, A.3.3, and A.3.6 shall be met.

A.3.7.4.7 Solderability. Solderability testing is applicable only on printed wiring board designs that require soldering during circuit card assembly processes. Unless otherwise specified (see A.3.1.1), printed wiring board designs that use compliant pin technology only for component attachment do not require solderability testing. Unless otherwise specified (see A.3.1.1), printed wiring board designs that use surface mount components only shall be tested for surface solderability, not hole solderability.

A.3.7.4.7.1 Hole (plated through hole). After undergoing the test specified in A.4.8.4.7.1, the printed wiring board test specimen shall conform to the accept/reject criterion (good wetting, pinholes, dewetting, non-wetting, etc.) specified in the solderability test methods listed in appendix J of MIL–PRF–31032, as applicable.

A.3.7.4.7.2 Surface or surface mount land. After undergoing the test specified in A.4.8.4.7.2, the printed wiring board test specimen shall conform to the accept/reject criterion (good wetting, pinholes, dewetting, non-wetting, etc.) specified in the solderability test methods listed in appendix J of MIL–PRF–31032, as applicable.

A.3.7.4.8 Surface peel strength (types 3 and 4 foil laminated printed wiring boards). When tested as specified in A.4.8.4.8, the surface conductor shall withstand a minimum peel strength greater than or equal to the "after thermal stress" values for the corresponding copper foil and profile as specified by either the applicable base material specification or the master drawing. If no value for peel strength is listed in the base material specification for the copper foil used (as is the case with many low profile style foils), then a value that is 75 percent of the standard profile copper foil shall be used. Unless otherwise specified (see A.3.1.1), the peel strength values for base material thicknesses over .0197 inch (0.500 mm) specified by the base material specification shall be used. This requirement is only applicable to foil laminated types 3 and 4 printed wiring boards that have surface conductors or surface mount lands. Printed wiring boards with no external circuitry (external terminal land or pads only) do not require peel strength testing.

A.3.7.4.9 Solder mask cure. When inspected as specified in A.4.8.1, the cured solder mask shall not exhibit tackiness, blistering, or delamination.

A.3.7.5 Electrical requirements. See IPC–9252 for additional guidelines.

A.3.7.5.1 Continuity and isolation resistance, production screening. When specified that it is acceptable (see A.3.1.1), verification of circuit continuity, isolation resistance, and shorts by indirect testing by signature comparison in accordance with A.4.8.5.1 may be used for production screening.

A.3.7.5.2 Continuity and isolation resistance, periodic and referee testing.

A.3.7.5.2.1 Circuit continuity. When tested as specified in A.4.8.5.2, the resistance between the end-points of conductor patterns within a network of conductors shall be as specified (see A.3.1.1). Unless otherwise specified (see A.3.1.1), for production printed boards, there shall be no circuits whose resistance exceeds the class C requirements of IPC–9252 for resistive continuity testing. Unless otherwise specified (see A.3.1.1), for referee purposes, 0.1 ohm maximum for each inch of circuit length shall apply. Conductor patterns that consist of long runs of narrow conductors or short runs of very wide conductors may increase or decrease the resistance. The acceptability of these type of circuits, of controlled impedance nets, or of embedded resistive patterns shall be specified.

A.3.7.5.2.2 Isolation resistance (circuit shorts). When tested as specified in A.4.8.5.2, the insulation resistance between mutually isolated conductors shall be as specified (see A.3.1.1) Unless otherwise specified (see A.3.1.1), for production printed boards, the insulation resistance shall comply with the class C requirements of IPC–9252 for resistive isolation testing.

A.3.7.5.3 Circuit or plated-through hole short to metal core substrate. When printed wiring board designs with metal cores are tested in accordance with A.4.8.5.2, the dielectric material used to insulate the heat-sinking plane from circuitry and plated through holes shall provide an insulation resistance greater than 10 megohms. Electrical access to the metal core substrate shall be provided in the design when this test is to be performed.

A.3.7.5.4 Dielectric withstanding voltage (DWV). When inspected as specified in A.4.8.5.3, there shall be no flashover, sparkover, or breakdown between isolated conductors.

A.3.7.5.5 Impedance testing (when specified). When impedance resistance values are specified (see A.3.1.1), all printed boards shall be electrically testing tested as specified in A.4.8.5.4.

A.3.7.6 Environmental requirements.

A.3.7.6.1 Moisture and insulation resistance (MIR).

A.3.7.6.1.1 Non-flush conductor printed boards. When tested as specified in A.4.8.6.1.1, the printed wiring board test specimen shall have a minimum of 500 megohms of resistance between conductors when tested at 500 volts (+25, –0) direct current. After the test, the specimen shall be inspected in accordance with A.4.8.1 and the specimen shall not exhibit blistering, measling, or delamination in excess of that allowed in A.3.5.1.3.

A.3.7.6.1.2 Flush conductor printed boards. When tested as specified in A.4.8.6.1.2, the printed wiring board designed for flush conductor applications shall have a minimum of 50 megohms of resistance between conductors when tested at 500 volts (+15, –0) direct current. After the test, the specimen shall be inspected in accordance with A.4.8.1 and the specimen shall not exhibit blistering, measling, or delamination in excess of that allowed in A.3.5.1.3.

A.3.7.6.2 Resistance to soldering heat.

A.3.7.6.2.1 Solder float thermal stress (single side, single cycle, component holes).

A.3.7.6.2.1.1 Type 1. After undergoing the test specified in A.4.8.6.2.1.1, the printed wiring board test specimen shall be inspected in accordance with A.4.8.1 and shall not exhibit any cracking or separation of plating and conductors, blistering or delamination shall not exceed the limits allowed in A.3.5.1.3 and lands shall not lift in excess of that allowed in A.3.5.2.1.

A.3.7.6.2.1.2 Types 2, 3 and 4. After undergoing the test specified in A.4.8.6.2.1.2, the printed wiring board test specimen shall be examined in accordance with A.4.8.1 and shall exhibit no blistering or delamination in excess of that allowed in A.3.5.1.3. After meeting the external visual and dimensional requirements of A.3.5.1.3, the printed wiring board test specimen shall meet the DPA requirements of A.3.7.2.2.

A.3.7.6.3 Thermal shock.

A.3.7.6.3.1 Thermosetting resin base materials (see A.7.15.1). While undergoing the test specified in A.4.8.6.3.1, a resistance change of 10 percent or more between the first and last high temperature measurements shall be considered a reject. After the test, the printed wiring board test specimens shall meet the following requirements:

a. External visual and dimensional inspection (all types): When inspected as specified in A.4.8.1, there shall be no evidence of plating cracks, blistering, or delamination in excess of that allowed in A.3.5.1.3.

b. Internal visual and dimensional inspection (types 3 and 4 only): When the printed wiring board test specimen is microsectioned and inspected in accordance with A.4.8.2, the requirements specified in A.3.1.1, A.3.3, and A.3.6 shall be met.

A.3.7.6.3.2 Thermoplastic resin base materials (see A.7.15.2). While undergoing the test specified in A.4.8.6.3.2, a resistance change of 15 percent or more between the first and last high temperature measurements shall be considered a reject. After the test, when printed wiring board test specimens are inspected as specified in A.4.8.1, there shall be no evidence of plating cracks, blistering, or delamination in excess of that allowed in A.3.5.1.3.

A.3.8 Marking.

A.3.8.1 Product identification and test vehicle traceability codes. Unless otherwise specified (see A.6.2), each production printed wiring board, each qualification test specimen, and each set of quality conformance test circuit strips (as opposed to each individual test coupon) shall be marked as specified (see A.3.1.1) and herein. As a minimum, each production printed wiring board, qualification test specimen, and quality conformance test circuit strip shall be marked with the printed wiring board manufacturers' CAGE code (see 6.4.2), lot date code (see A.3.8.5), and traceability code (see A.7.18). Additional marking on the printed wiring boards is allowed provided it does not interfere with the required marking.

A.3.8.2 Legend. Legend on printed wiring boards shall be as specified (see A.3.1.1).

A.3.8.3 Methods of producing legend and marking. Legend and marking shall be produced by one of the following methods: The same process used in producing the conductive pattern; or the use of a fungistatic ink or paint applied to the printed wiring board; or on a label which is applied to the printed wiring board; or by a mechanical pencil, mechanical machining, or laser machining on a metallic area provided for marking purposes. Conductive legends or marking shall be no closer to the conductive pattern of the printed wiring board than the spacing requirements specified (see A.3.1.1).

A.3.8.4 Product identification and test vehicle traceability legibility. All product identification and test vehicle traceability marking shall be able to withstand solder fluxes, cleaning solutions, and molten solder encountered in the manufacture of printed wiring boards. The marking shall remain legible after all tests, and in no manner affect printed wiring board performance. After any or all tests, product identification and traceability marking shall comply with the class 3, acceptable conditions detailed in IPC–A–600.

A.3.8.5 Lot date code. The lot date code is a unique code to identify the period during which the printed wiring boards were manufactured. Unless otherwise specified by the acquiring activity (see A.3.1.1), the first two numbers in the lot date code shall be two digits of the number of the year, and the third and fourth number shall be two digits indicating the calendar week of the year. When the number of the week is a single digit, it shall be proceeded by a zero reading from left to right or from top to bottom, the code number shall designate the year and week, in that order.

A.3.9 Traceability. Traceability shall be available for review by the qualifying or acquiring activity for a minimum of 3 years after delivery of the printed wiring boards. Supporting test data, test coupons, and microsection mounts shall be retained by the manufacturer. Lost or inadequate quality records, supporting data, and test coupons (including microsection mounts and untested test coupons) may result in loss of qualification.

A.3.9.1 Quality–conformance test circuitry, test coupons, and microsection mounts. Each quality–conformance test circuitry (QCTC) shall be identifiable with those corresponding production printed wiring boards produced on the same inspection panel that also produced the QCTC. Unless otherwise specified (see A.3.1.1), each QCTC shall be traceable to its originating position on the panel. All individual test coupons (including those in microsection mounts) separated from its QCTC, or qualification test specimen, shall have its traceability maintained back to the inspection panel, QCTC, or qualification test specimen from where the test coupons originated. When a QCTC or test coupon is representative of more than one printed board design (multiple designs on each panel), it shall be traceable to those printed boards fabricated on that inspection panel. When a microsection mount contains more than one specimen, an orientation mark or other identification marking shall identify layer one of the first specimen. Unless otherwise listed on the multiple specimen microsection mount, traceability identifying all specimens contained in a mount shall be maintained.

A.3.9.2 Printed board materials. Traceability shall be such that for each printed wiring board, all printed board materials specified (see A.3.1.1) or used shall be traceable to a material production lot, inspection lot, or other specified grouping.

A.3.9.3 Serialization. When the contract requires the printed wiring boards to be serialized, each printed wiring board or qualification test specimen shall be marked with a unique serial number assigned consecutively within the inspection lot, allowing traceability of the printed wiring board and its test results.

A.3.9.4 Quality records. Manufacturers producing printed wiring boards to the QPL product assurance level system shall have a process in place to track all quality records, including, but not limited to, the results of all qualification, inspection of product for delivery tests (including microsection mounts), and examinations (attributes or variable data), any required failure analysis, and contract services records. The retention period for each type of quality records shall be a minimum of 3 years.

A.3.10 Rework and repair.

A.3.10.1 Rework. The touch-up of surface imperfections in the base material, removal of residual plating materials, or extraneous copper shall be permitted when such action does not affect the functional integrity of the printed wiring board.

A.3.10.2 Repair. When inspected in accordance with A.4.8.1, printed wiring boards shall not be repaired or reveal any evidence of repair.

A.3.11 Recycled, recovered, environmentally preferable, or biobased materials. Recycled, recovered, environmentally preferable, or biobased materials should be used to the maximum extent possible provided that the material meets or exceeds the operational and maintenance requirements, and promotes economically advantageous life cycle costs.

A.3.12 Workmanship. Printed wiring boards shall be processed in such a manner as to be uniform in quality and shall be free from defects in excess of those allowed in this appendix that could affect life or serviceability.

A.4. VERIFICATION

A.4.1 Classification of inspections. The inspection requirements specified herein are classified as follows:

a. Qualification inspection (see A.4.5).

b. Inspection of product for delivery (see A.4.6).

c. Periodic conformance inspection (see A.4.7).

A.4.2 Test and measuring equipment. Measuring and test equipment of sufficient precision and bias, quality, and quantity to permit performance of the required inspection shall be established and maintained by the manufacturer. The establishment and maintenance of a calibration system to control the accuracy of the measuring and test equipment shall be in accordance with section C.5 of appendix C, or equivalent.

A.4.3 Inspection conditions. Unless otherwise specified in the applicable test method or procedure, inspections and tests shall be performed in accordance with test method number 1.3 of IPC–TM–650.

A.4.4 Printed wiring board performance verification.

A.4.4.1 General. Printed wiring board performance verification shall consist of inspections on the production printed wiring boards and the QCTC or test coupons referenced in tables herein for in-process, groups A and B inspections. Selection of test coupons for testing shall be in accordance with the applicable inspection table. Each production printed wiring board or production panel of printed wiring boards shall include sufficient test coupons to complete the applicable verification requirements specified. The design of test coupons shall be as specified on the applicable master drawing (see A.3.1.1). The minimum number of test coupons on the production panel and the requirements for positioning the test coupons on the inspection panel shall be in accordance with the requirements of appendix H.

A.4.4.2 Verifications performed by a certified suitable laboratory. Because of the performance nature of this document, the design and construction details of the printed boards, or the test coupons that represent the printed boards, shall be supplied with the sample units to be inspected or tested by a certified suitable laboratory. The design and construction details are needed so that the resulting evaluations can confirm compliance to both the master drawing and the acceptability requirements herein. This communication of design and construction details shall apply whenever printed wiring boards, inspection panels of printed wiring boards, or test coupons are tested and inspected to either group A (including electrical testing) or group B inspection herein performed by a certified suitable laboratory.

A.4.5 Qualification inspection (see A.6.3). Qualification inspection shall be performed at the manufacturing location and a laboratory acceptable to the Government (see A.6.5) on sample qualification test specimens produced with material, equipment, processes, and procedures normally used in production. The requirements for qualification to the QPL product assurance level shall be in accordance with appendix E.

A.4.5.1 Retention of qualification. To retain qualification, the manufacturer shall make available to the qualifying activity data concerning production of qualified product at 12-month intervals. The qualifying activity shall establish the initial reporting date. The retention of qualification data shall consist of:

a. A summary of the results of the tests performed for inspection of product delivery (in-process and group A) indicating as a minimum the number of lots that have passed and the number of lots that have failed. The results of tests of all reworked lots shall be identified and accounted for.

b. A summary of the results of tests performed for periodic conformance inspection (group B) performed and completed during the 12-month period. Group B shall be performed only for those months in which production occurred.

c. The actual test data for groups A and B shall be supplied to the qualifying activity upon request.

d. The extent of qualification of base materials specified in E.4 shall apply.

e. In the event that no production occurred during the 12-month period, the manufacturer shall certify that it still has the capabilities and facilities necessary to produce and test the qualified product.

A.4.5.2 Failure to submit retention data. Failure to communicate with the qualifying activity within 60 calendar days after the end of the 12 month period may result in loss of qualification. In addition, the manufacturer shall notify the qualifying activity within 3 business days if at any time during the 12 month period, that the results of periodic inspection indicates failure of the qualified product to meet the performance requirements of this appendix.

A.4.5.3 Non-production during reporting period. In the event that there is no production of any compliant printed wiring boards during the 12 month reporting period, the manufacturer shall either certify to the qualifying activity that the capabilities and facilities necessary to manufacture and test QPL printed wiring boards still exists and that the manufacturer wants to remain on the QPL or requalify. If during two consecutive reporting periods there has been no production of the qualified product, the manufacturer may be required, at the discretion of the qualifying activity, to submit a representative printed wiring board of each base material type qualified to partial or full re-qualification testing. For the case when the manufacturer is qualified to more than one base material type and there has been no production of the qualified product of one or all qualified base material types, the manufacturer may be required, at the discretion of the qualifying activity, to submit a representative product of those base material types to testing.

A.4.5.4 Requalification. Requalification is not required as long as the manufacturer maintains a listing for an equivalent technology to be supplied to this appendix on QML–31032.

A.4.6 Inspection of product for delivery. Inspection of product for delivery shall consist of in-process and group A inspection. Except as specified in A.4.7.1.4, delivery of printed wiring boards which have passed in-process and group A inspection shall not be delayed pending the results of the periodic inspection. Anomalies or defects noted on sample printed wiring boards or test coupons (or both) defined herein shall be recorded and the proper corrective action shall be initiated. Manufacturers that are qualified to use contract services are still responsible for in-process and group A inspections and shall be subject to loss of qualification for failure to complete the in-process and group A inspections.

A.4.6.1 In-process inspection. Each inspection lot of printed wiring boards or inspection panels, as applicable, shall be inspected in accordance with table A–V. When permanent solder mask is specified (see A.3.1.1), the in-process inspections specified in subgroups 1, 2, and 3 of table A–V shall be performed prior to solder mask application. Prior to lamination of types 3 or 4 printed wiring boards, the in-process inspections specified in subgroup 2 of table A–V shall be performed.

A.4.6.1.1 Inspection lot.

A.4.6.1.1.1 Subgroup 1. An inspection lot shall correspond to each production lot or each change of shift of work force, whichever occurs first. Production lots may be grouped based on same materials, same type or types of interfacial connections and terminations, and same processing requirements.

A.4.6.1.1.2 Subgroups 2 and 3. An inspection lot shall consist of the number of printed wiring boards fabricated from the same materials, using the same processing procedures, produced under the same conditions within a maximum period of 1 month and offered for inspection at one time.

A.4.6.1.2 Sample size. The number of printed wiring boards or inspection panels to be selected from each inspection lot shall be in accordance with appendix H.

TABLE A–V. In-process inspection.

Inspection	Requirement paragraph	Method paragraph	Sample size 1/	Notes
Subgroup 1				
Material	A.3.4	A.4.8.1.10	See A.4.8.1	
Ionic contamination (cleanliness)	A.3.7.3.1	A.4.8.3.1	Plan BN or TL	2/
Subgroup 2				
Conductor spacing	A.3.5.2.4.1	A.4.8.1	Plan BH	2/ 3/
Conductor width	A.3.5.2.4.2	A.4.8.1	Plan BH	2/ 3/
Conductor pattern imperfections	A.3.5.2.3	A.4.8.1	Plan BH	2/ 3/
Annular ring of internal layers	A.3.5.2.6	A.4.8.1	Plan BH	4/
Subgroup 3				
Plating adhesion	A.3.7.4.2	A.4.8.4.2	Plan BH	2/ 5/

1/ See appendix C, table C–I for C = 0 sampling plans.
2/ Performed prior to solder mask application.
3/ Performed prior to lamination on each production lot.
4/ External lands of vias produced as sequentially laminated structures shall be evaluated prior to additional lamination(s).
5/ When fused tin-lead is specified as a surface finish, a non-reflowed test coupon prior to reflow may be required (see A.6.2).

A.4.6.1.3 Rejected lots. If an inspection lot is rejected as a result of a failure to pass the subgroup 1 tests specified, the manufacturer shall withdraw the lot, take corrective action in connection with the cleaning materials and procedures, reclean the lot prior to application of permanent solder mask coating, and resubmit the lot for inspection. Printed wiring boards are not acceptable if the permanent solder mask coating has been applied to a contaminated surface. If an inspection lot is rejected for subgroup 2 or 3 tests, the manufacturer may screen (100 percent inspection) out the defective units (printed wiring boards or printed boards represented by inspection panels). Defective printed wiring boards shall not be shipped.

A.4.6.2 Group A inspection. Group A inspection shall consist of the inspections specified in table A–VI. The qualified manufacturer shall be responsible for completion of all group A inspections and shall be subject to loss of qualification for failure to complete all group A tests and inspections.

A.4.6.2.1 Inspection lot. A group A inspection lot shall consist of the number of printed wiring boards fabricated from the same materials, using the same processing procedures, produced under the same conditions within a maximum period of 1 month and offered for inspection at one time.

A.4.6.2.2 Sampling procedures. Statistical sampling and inspection shall be in accordance with appendix C. For 100 percent inspection, all rejected units (printed wiring boards or panels of printed wiring boards) shall not be supplied on the contract. The following details on panel/test coupon sampling shall apply:

a. Solderabilty (see A.3.7.4.7): For printed wiring board using only surface mount (SMT) components, the surface solderability test can be used in lieu of the hole solderability test. For mixed component designs (both SMT and through hole attachment), unless otherwise specified, only the hole solderability test shall be performed.

   (1) For sequential electrochemical reduction analysis (SERA), samples shall be selected in accordance with appendix G of MIL–PRF–31032.

   (2) For the other solderability test methods detailed in appendix J of MIL–PRF–31032: When using test coupon "S", the number of samples to be tested shall be based on a statistical sample of the inspection panels in the lot in accordance with series L of table C–I. When using test coupon "A", the number of samples to be tested shall be based on the same statistical sample of test coupon "S", but a multiple of four shall be applied to the resulting sample size.

   Example: The lot size of inspection panels is 30. If test coupon "S" is present on the inspection panel, then at least 3 randomly selected samples would need to be tested. If test coupon "A" is being used in lieu of test coupon "S" (no "S" test coupons present), then at least 12 randomly selected samples would need to tested.

b. Resistance to soldering heat (solder float thermal stress) (see A.3.7.6.2).

   (1) Type 1: The test specimen shall be test coupon "B". The number of test coupons to be tested and inspected shall be based on a statistical sample of the number of inspection panels in the lot in accordance with appendix C, table C–I, series L.

   (2) Type 2: The test specimen shall be test coupon "B". The number of test coupons to be tested and microsectioned shall be based on a statistical sample of the number of inspection panels in the lot in accordance with appendix C, table C–I, series J.

   (3) Type 3: A minimum of two test specimens (one "A" and one "B" test coupon) for each completed panel shall be subjected to the resistance to soldering heat test. The two test coupons shall be taken from opposite corners of the panel. After the test, one of the test coupons shall be microsectioned in the panel's length (X direction) and the other shall be microsectioned along the panel's width (Y direction).

   (4) Type 4 (type 3 with blind and buried vias): In addition to the sampling required in A.4.6.2.2.b(3), printed wiring boards with blind, buried, or both blind and buried vias shall have as a minimum, one additional resistance to soldering heat test specimen tested in accordance with A.4.8.6.2 and inspected to the requirements of A.3.7.2 for each panel for each additional hole copper plating process used.

   For panels with printed board designs with blind, buried, or both blind and buried vias and no corresponding test coupons reflecting these types of plated structures, the use of printed boards from the panel in lieu of dedictated test coupons shall be acceptable. The areas from printed boards to be microsection and inspected shall contain the types of plated structures present in the design so that all of the different criteria can be evaluated.

c. Registration.

(1) Method I (types 1 and 2 only): When method I is used, registration shall be evaluated using any combination of "A" test coupons taken from diagonal corners of the inspection panel.

(2) Method II (types 3 and 4 only): When method II is to be used, registration shall be evaluated using any combination of two microsectioned test specimens taken from diagonal corners of the inspection panel. Both test coupons shall have been microsectioned in the vertical plane with one test coupon representing the panel's length (X) direction and the other representing the panel's width (Y) direction. Test coupons from the "non-stressed" (see A.3.7.2.1) or "resistance to soldering heat" (see A.3.7.6.2) verifications may be used.

(3) Method III: When method III is to be used, the number of sample units needed for verifying registration shall be documented in the qualifying activity approved alternate test plan (see C.5.2.2).

d. Copper plating voids (see A.3.6.4.4.3). When a single plating void that is within the acceptable limits of A.3.6.4.4.3 is present in a microsection or set of microsections representing an inspection panel, a referee sample unit from that panel shall be microsectioned and inspected for copper plating voids. The referee microsection shall be performed using test coupon "A" or "B" from the opposite corner of the suspect panel. If the referee microsection has no plating voids, then that panel is acceptable, however, if a plating void is present in the referee microsection, that panel of printed wiring boards shall be rejected. Any plated-through hole in the microsection failing the plating void criteria specified in A.3.6.4.4.3 subparagraphs a, b, or c, shall be cause for the entire inspection panel of printed wiring boards associated with the microsection to be rejected.

A.4.6.2.3 Alternative to sampling inspection (first piece produced design inspection see A.7.18). In lieu of performing sample inspections of all characteristics or parameters detailed on the master drawing, manufacturers may use first piece produced design inspection. This type of inspection is only applicable to the criteria described in A.4.6.2.3.1 and A.4.6.2.3.2. First piece produced design inspection can be performed on the first printed wiring board that is representative of all printed wiring boards in the production lot of the design. The use of automated inspection technology shall be acceptable.

A.4.6.2.3.1 Board and conductor pattern features. Unless otherwise specified, the accuracy of board and conductor pattern features may be verified by performing first piece produced design inspection on a representative first production run part or by sampling the printed boards in the lot.

A.4.6.2.3.2 Hole pattern accuracy. Unless otherwise specified, only the holes that are specifically dimensioned on the master drawing shall be inspected for hole pattern accuracy to meet the board dimensional requirements specified. Unless otherwise specified, the accuracy of the hole pattern may be verified by performing first piece produced design inspection on a representative first production run part or by sampling the printed boards in the lot. Unless otherwise specified, the hole pattern accuracy of nonspecifically dimensioned holes, such as plated through holes and vias, do not need to be checked as their locations are set by the design activity supplied database and are controlled by external and internal annular ring requirements.

A.4.6.2.4 Rejected lots. If an inspection lot is rejected, the manufacturer may rework it to correct the defects and resubmit the lot for reinspection, or screen out the defective units (if possible). Resubmitted lots shall be inspected using tightened inspection (see appendix C). Such lots (reworked or screened) shall be clearly identified as reinspected lots. Products which have failed any group A inspection herein and have not been reworked and have not passed reinspection (as specified in this appendix) may not be delivered as compliant printed wiring boards.

A.4.6.2.5 Disposition of sample units. Sample printed wiring boards which have passed all of group A inspection herein may be delivered if the inspection lot is accepted.

TABLE A–VI. Group A inspection.

Inspection	Requirement paragraph	Method paragraph	Test specimen 1/			Sample plans 2/
			T1	T2	T3 / T4	
Visual and dimensional						
Acceptability	A.3.7.1	A.4.8.1	PWB	PWB	PWB	Plan BH 3/ 4/
Registration, external	A.3.5.3.6	A.4.8.1.5	5/	5/		Plan TJ
DPA by microsection						
Registration, internal	A.3.7.2.3	A.4.8.2.4				See 6/ and 7/
Chemical						
Resistance to solvents	A.3.7.3.2	A.4.8.3.2	8/	8/	8/	See 8/
Physical						
Plating adhesion	A.3.7.4.2	A.4.8.4.2	PWB or C	PWB or C	PWB or C	Plan BH/TJ 3/ 9/
Solder mask adhesion	A.3.7.4.3	A.4.8.4.3	G	G	G	Plan TJ
Bow and twist	A.3.7.4.4	A.4.8.4.4	PWB	PWB	PWB	Plan BH
Conductor edge outgrowth	A.3.7.4.5	A.4.8.4.5	PWB	PWB	PWB	Plan BH
Solderability						
Hole	A.3.7.4.7.1	A.4.8.4.7.1		10/	10/	See 6/ and 10/
Surface	A.3.7.4.7.2	A.4.8.4.7.2	11/	11/	11/	Plan BH/TJ 6/ 11/
Electrical						
Circuit continuity	A.3.7.5.1	A.4.8.5.1	PWB	PWB	PWB	100 percent 12/
Isolation resistance	A.3.7.5.1	A.4.8.5.1	PWB	PWB	PWB	100 percent 12/
Environmental						
Resistance to soldering heat	A.3.7.6.2	A.4.8.6.2	B	B	A and B	See 6/

1/ T1 designates a type 1 design; T2 designates a type 2 design; T3 designates a type 3 design; T4 designates a type 4 design; and PWB means inspect the entire board, whereas an individual test coupon designation means inspect the specified test coupon. See appendix D herein for test coupon identification (name) translation to the applicable design standard.
2/ See appendix C, table C–I for C = 0 sampling plans and C.4.5 for examples.
3/ Some attributes may need to be inspected prior to lamination or solder mask application (see A.4.6.1).
4/ The solder mask thickness test can be performed on either a test coupon at a sampling of TJ or production printed wiring board at a sampling of BH, manufacturer's option.
5/ Test coupon or production printed wiring board, manufacturer’s option.
6/ See A.4.6.2.2 for sample size and test specimen description.
7/ Optional method by designated registration test coupons (method III), see A.4.8.2.4.2 for test specimen description and sample size.
8/ See A.4.8.3.2.1 for test specimen description and sample size.
9/ Applicable to platings only. This inspection does not need to be performed on solder or organic coatings.
10/ A or S test coupon, manufacturer’s option.
11/ PWB, C, or M test coupon, manufacturer's option. For printed wiring boards using only surface mount lands for component attachment, the surface solderability test can be used in lieu of the hole solderability test.
12/ Types 2, 3 and 4 printed wiring boards only.

A.4.7 Periodic conformance inspection. Periodic conformance inspection shall consist of group B inspection. Except where these inspections show noncompliance with the applicable requirements (see A.4.7.1.4), delivery of printed wiring boards which have passed in-process and group A inspection shall not be delayed pending the results of these periodic inspections. Periodic inspections shall be performed at a certified suitable laboratory (see A.6.5). Because of the performance nature of this document, the design details of the printed wiring boards represented by the sample units need to be made available to the testing facility (see A.6.7 and C.6.1).

A.4.7.1 Group B inspection. Group B inspection shall consist of the tests specified in table A–VII. All tests in subgroup 1 tests shall be performed. Tests in subgroup 2 are dependant on printed wiring board construction techniques and if compliance testing was performed during group A.

A.4.7.1.1 Inspection lot. The sample units shall be randomly selected from an inspection lot or lots that have passed all in-process and group A inspections during that production month (i.e., the group B reporting period). The sample units shall represent the most complex design features of the printed wiring boards produced during the reporting period. Design complexity shall be as determined by the manufacturer using its definition of printed board design complexity (see A.7.4), subject to approval by the qualifying activity. If all the inspections in table A–VI cannot be performed on the most complex lot of the month, additional sample units from other designs shall be submitted if they address the design, materials, or technology to be verified.

A.4.7.1.2 Sampling procedures. Samples units for each base material type groupings produced during that reporting period shall be subjected to group B inspection. Except for the case of a one panel inspection lot, the sample units shall be selected from different panels. The extent of qualification of types allowed by appendix E shall apply. The following criteria shall be used in selecting samples for group B testing:

a. Rework simulation and MIR. The sample units shall be from the most complex (see A.7.4) printed wiring board design produced that calendar month. Because of the performance nature of this document, the design details of the test coupons or the printed boards that they represent shall be supplied with the sample units so that proper verification can be confirmed (see A.6.7). The sample units can be either:

   (1) Two sets of quality conformance test circuitry, or

   (2) Two test coupons for each test to be performed.

b. Surface peel strength. When multiple lots using foil lamination are available, a minimum of eight peel strength specimens shall be selected from at least two different production lots; a maximum of four from each lot or 100 percent if the number of coupons available is less than four for a production lot. If only one foil laminated lot is available for a calendar month, then only the test coupon(s) from that lot shall be submitted for testing.

c. Resistance to solvents. The test specimens can be either whole or parts of production printed wiring boards or quality conformance test circuitry strip identification areas containing ink or paint marking. The minimum number of samples shall be at least one sample for each solution specified by the applicable test method (i.e., one sample for each solution required).

Example: The most complex lot using FR-4 base material did not use ink or paint marking, foil lamination construction, and was a surface mount only design. However, other compliant lots constructed that month of legacy types GB and GH base materials (within the same base material grouping) did use ink or paint marking, foil lamination, and though-hole mounting. The group B inspection lot for that month shall contain samples from more than one design (or part number) or lot of printed board design in order to comply. The exact breakdown of 5 different part numbers for the group B submission could be as follows:

(1) Part number "A" for the MIR–DWV test, the most complex design of the month. Although part number "A" is a SMT only design with no component size holes, it still can and shall be used because the test coupon hole size is determined by IPC–2221 for SMT designs.

(2) Part numbers "B" and "D" for surface peel strength testing.

(3) Part number "C" for rework simulation testing. Part number "C" is the third most complex design produced that month, but it is the most complex design using component holes.

(4) Part numbers "B", "D", and "E" for resistance to solvents testing since this test is not being performed during group A on a lot–to–lot basis. Alternately, three specimens from part number "B" could be submitted.

A.4.7.1.3 Frequency. The frequency of selecting sample units and performing group B testing shall be on a monthly basis. The sample units shall be submitted for testing within 30 calendar days after the end of each reporting period.

A.4.7.1.4 Failures. If one or more sample units fail to pass group B inspection, the sample shall be considered to have failed. The qualifying activity shall be notified of any group B failure within 3 business days. Group B inspection shall be repeated on additional sample units (either all group B inspections or just the group B inspection which the original sample failed, at the discretion of the qualifying activity) from the next most complex (see A.7.4) inspection lot from the same month that the failure occurred. Group A inspection and shipment of the product represented by the failed group B sample shall be discontinued.

TABLE A–VII. Group B inspection.

Inspection	Requirement paragraph	Method paragraph	Test coupon by type 1/ 2/		
			Type 1	Type 2	Types 3 / 4
Subgroup 1					
Rework simulation	A.3.7.4.6	A.4.8.4.6	3/	3/	3/
Moisture and insulation resistance	A.3.7.6.1	A.4.8.6.1	E	E	E
Dielectric withstanding voltage	A.3.7.5.3	A.4.8.5.3	4/	4/	4/
Subgroup 2					
Resistance to solvents	A.3.7.3.2	A.4.8.3.2	5/	5/	5/
Surface peel strength	A.3.7.4.8	A.4.8.4.8			N or P 6/

1/ See 1.2, A.3.1.1, and A.7.4 herein.
2/ See appendix D for test coupon identification letter translation to the applicable design standard.
3/ The holes to be tested and inspected shall represent component holes used for through–hole mounting.
4/ Dielectric withstanding voltage shall be performed after the moisture and insulation resistance test on the same test coupon subjected to the moisture and insulation resistance test.
5/ See A.4.8.3.2.1 for test specimen description and number of samples required.
6/ Test coupon "N" minimum length shall be 2 inches (50.8 mm). Test coupon "P" is depicted on figure H–2. A minimum of eight test specimens ("N" or "P") shall be inspected. If two or more lots are produced, four test specimens from two lots shall be selected.

A.4.7.1.4.1 Corrective actions. Corrective actions shall be taken on the materials or processes, or both, as warranted, and on all units of product which can be corrected and which were manufactured under essentially the same conditions (materials, processes, and equipment) and which are considered subject to the same failure.

A.4.7.1.4.2 Noncompliance. If the lot or lots directly represented by the group B failure have been shipped, the manufacturer shall notify the acquiring activity of the failure and shall recall the affected lot or lots for reinspection, if possible. All other lots represented by extension of qualification by the failed group B sample are considered noncompliant until a sample from the next most complex (see A.7.4) inspection lot passes group B inspection.

A.4.7.1.4.3 Reinstitution of group A inspection. After successful completion of group B reinspection, group A inspection of product represented by the group B failure may be reinstituted.

A.4.7.1.5 Disposition of sample units. Sample units which have been subjected to group B shall be retained as specified in A.3.9.

A.4.8 Methods of inspection. The following inspections and test methods are used to assure printed wiring board integrity within typical operating conditions. Alternate test methods may be allowed with prior approval by the qualifying activity. The following inspections and test methods described herein are the preferred methods and shall be the referee method in case of dispute if alternate test methods result in differing or conflicting results.

A.4.8.1 Visual and dimensional inspection. The visual and dimensional features of the printed wiring board test specimen shall be inspected using either test method number 2.2.1 or 2.2.2 of IPC–TM–650, as applicable. Unless otherwise specified, the magnifications in table A–VIII shall be used for the conductor width or land diameter/width of features under inspection. Referee inspection needed to confirm a suspected defect of the specimen features shall be accomplished at a magnification of up to 40X, as applicable to confirm the suspected defect. Characteristics not observable through solder mask shall be evaluated prior to its application to the surface of the printed wiring board (see A.4.6.1). Verification of printed wiring board dimensional parameters using automated inspection technology (AOI and AXI) shall be acceptable.

TABLE A–VIII. Inspection magnification.

Conductor width or land diameter/width	Magnification 1/		IPC–OI–645 grade
	Standard inspection	Referee inspection	
Greater than .04 inches (1.0 mm)	1.75X	4X	IV and V
From .02 to .04 inches (0.5 to 1.0 mm)	4X	10X	V and VI
From .001 to .02 inches (0.025 to 0.5 mm)	10X	20X	VI and VII
Less than .001 inches (0.025 mm)	20X	40X	VII and VIII

1/ Referee conditions are used to verify printed wiring boards rejected at the standard inspection magnification power. For printed wiring board designs with mixed conductor and land diameters and widths, the greater magnification power may be used for the inspection of the entire printed wiring board.

A.4.8.1.1 Component hole land annular ring, external (see A.3.5.2.5.1). The measurement of the annular ring on external layers is from the inside surface (within the hole) of the plated hole structure or unsupported hole to the outer edge of the annular ring on the surface of the printed wiring board (see figure F–4 for illustration).

A.4.8.1.2 Conductor spacing and width (see A.3.5.2.4). The external measurement of the conductor spacing and conductor width is performed at the plane of the surface of a base material (see figure F–3 for illustration).

A.4.8.1.3 Hole size (see A.3.5.3.5). The finished hole size and tolerance shall be verified on a sample basis across all hole sizes applicable to the design. The number of hole size measurements needed for each hole size shall be determined by the manufacturer. The number of holes to be sampled for each hole size present on the printed wiring board shall be determined based on the number of holes within the population. The sampling plan used shall be documented by the manufacturer in its product assurance plan.

A.4.8.1.4 Overall printed board thickness (see A.3.5.3). Unless otherwise specified, the overall printed board thickness measurement shall be inspected non-destructively in accordance with test method number 2.2.18 of IPC–TM–650 or by destructively by microsection in accordance with A.4.8.2.

A.4.8.1.4.1 With edge-board contacts. Printed boards with edge-board contacts shall have the overall thickness measured across the board on the final finish plated surfaces of opposite contacts.

A.4.8.1.4.2 Without edge-board contacts. Unless otherwise specified, printed boards without edge-board contacts shall have the overall thickness measured across the board from plated copper surface to plated copper surface not including the final finish plating.

A.4.8.1.5 Registration (method I) (types 1 and 2) (see A.3.5.3.6). Registration of types 1 and 2 printed wiring boards shall be satisfied if the outer layers meet the external annular ring (see A.3.1.1 and A.3.5.2.7) and hole pattern accuracy (see A.3.1.1 and A.3.5.3.4) requirements.

A.4.8.1.6 Non destructive plating and coating measurement techniques. When a plating or coating thickness is below .00005 inch (0.00125 mm), the thickness measurements shall be performed in accordance with one of the following procedures:

a. ASTM B567, measurement of thickness by the beta backscatter method.

b. ASTM B568, measurement of thickness by X-ray spectrometry.

A.4.8.1.7 Product identification and test vehicle traceability (marking). The printed wiring board specimen shall be inspected in accordance with test method number 2.1.8 of IPC–TM–650, except that the magnification shall be 1.75X (3 diopters), minimum.

A.4.8.1.8 Solder mask thickness (see A.3.5.4.5). Solder mask thickness shall be inspected by micrometer or by microsection in accordance with A.4.8.2.

A.4.8.1.9 Wire bond pad surface roughness. The printed wiring board specimen shall be inspected in accordance with test method number 2.4.15 of IPC–TM–650. Only the pristine area of the terminal shall be evaluated.

A.4.8.1.10 Materials inspection. Prior to any fabrication, materials inspection shall consist of certification supported by verification data, which verifies that the materials specified (see A.3.1.1) used in fabricating the printed wiring boards are in accordance with the applicable referenced specifications or requirements specified. Unless otherwise specified, verifying data does not need to be submitted to the qualifying activity or acquiring activity, but shall be made available upon request.

A.4.8.1.11 Workmanship. The printed board specimen shall be inspected in accordance with test method number 2.1.8 of IPC–TM–650, except that the magnification shall be in accordance with table A–VIII.

A.4.8.2 Microsection preparation and examination. Microsection examination (to evaluate characteristics such as plated-through holes, plating thickness, or foil thickness) shall be accomplished by using the following preparation and inspection methods.

A.4.8.2.1 Preparation. Microsection preparation shall be accomplished by using methods in accordance with test method number 2.1.1 of IPC–TM–650. Automatic microsectioning techniques may be used in lieu of test method 2.1.1 of IPC–TM–650 (see A.6.10). The following details shall apply:

a. Number of holes for each specimen. A minimum of at least three plated hole structures shall be cross sectioned vertically for each printed wiring board test specimen required.

b. Grinding and polishing accuracy.

(1) Through holes and non-copper filled microvias. The grinding and polishing accuracy for mounts shall be in accordance with the minimum qualities specified in test method 2.1.1 of IPC–TM–650.

(2) Copper filled microvias. The grinding and polishing accuracy shall be sufficient to evaluate the plating to microvia target land contact dimension.

c. Pre–microetch evaluations. The three plated hole structures of the test specimens shall be evaluated for plating separations, superfulous copper, and wicking prior to microetching (see A.6.11).

d. When more than two printed wiring board test specimens are contained in a mount (coupon–stacking or gang mounting), the following shall apply:

(1) The printed wiring board test specimens shall not be in direct contact with any other printed wiring board test specimen in the mount. The recommended minimum distance between printed wiring board test specimens in a mount is .010 inch (0.25 mm).

(2) The traceability requirements of A.3.9.1 shall apply.

A.4.8.2.2 Examination and inspection. Microsection examination and inspection shall be accomplished in accordance with test method number 2.2.5 of IPC–TM–650 to evaluate characteristics such as dielectric spacing, etchback, foil thickness, plating integrity, plating thickness, plating voids, etc., in plated hole structures. If more than three plated hole structures are in a printed wiring board test specimen cross section (as with test coupon "AB–R"), all plated hole structures in the cross section shall be evaluated. Each side of the plated hole structures shall be viewed independently. The following details shall apply:

a. Magnifications. The printed wiring board test specimens shall be inspected at the magnifications specified in test method number 2.2.5 of IPC–TM–650.

b. Evaluations. Pre– and post–microetch evaluations for the criteria of A.3.6 shall be accomplished at magnifications specified above. The printed wiring board test specimens shall be evaluated for plating separations, superfulous copper, and wicking prior to microetching (see A.6.11).

c. Measurements. Specified thickness measurements shall be averaged from at least three determinations taken from different locations on that side of the plated hole structure. Isolated thick or thin sections shall not be used for averaging; however, isolated areas of reduced copper thickness shall be measured and evaluated to the copper plating void rejection criteria specified in A.3.6.4.4.2.

   EXAMPLE: The copper plating thickness of the plated hole wall shall be determined from the average of three measurements, approximately equally spaced, taken on each side of the plated-through hole. Conductor thickness shall be determined by an average of three measurements on each layer and each side of the hole.

d. Final finish plating and coatings that are less than .00005 inch (0.00125 mm) in thickness shall not be measured using metallographic techniques. The plating and coating thickness shall be evaluated using the alternate measurement techniques of A.4.8.1.6.

A.4.8.2.3 Evaluation of plated hole structure features by DPA (see A.3.6). When external and internal features and structures (such as plated holes) are inspected in accordance with A.4.8.2.2, the following details shall apply:

a. Annular ring (internal) (see A.3.6.1). The measurement of the annular ring on internal layers is from the inside drilled surface (within the hole) of the plated hole or unsupported hole to the outer edge of land (see figure G–7). This measurement shall apply to all internal lands for all three holes.

b. Dielectric layer thickness (see A.3.6.4). The dielectric layer thickness shall be inspected between all conductor layers present in the test specimen. Dielectric layer thickness of types 3 and 4 designs shall determined by microsection in accordance with method number 2.2.18.1 of IPC–TM–650. NOTE: Dielectric layer thickness of type 1 and 2 designs by mechanical measurement can be determined in accordance A.4.8.1.4.

c. Conductor thickness (see A.3.6.2). The external and internal metal foil thickness shall be inspected on all conductor layers present in the test specimen. The following shall apply:

   (1) External conductor thickness. Measurements of external conductor thickness may be averaged from determinations taken at the inner edge, outer edge, and the middle of the land for each side of the plated hole structure.

   (2) Internal conductor thickness. If a side of a conductor has been treated, the median base of dendritic growth across the conductor shall be used as the measuring point for that conductor side. If a scratch or valley extends beyond the measurement line by 20 percent or more of the required thickness after processing, then the measurement on that side shall begin at the trough of the scratch or valley.

d. Copper plating thickness. Measurements of copper plating thickness for each side of the plated hole structure shall be averaged from at least three determinations taken from different locations on that side of the hole. Isolated thick or thin sections shall not be used for averaging; however, isolated areas of reduced copper thickness shall be measured and evaluated to the copper plating void rejection criteria specified in A.3.6.4.4.3.

e. Copper plating voids (see A.3.6.4.4.3). Any plated hole structure in the microsection failing the plating void criteria of A.3.6.4.4.3 subparagraphs a, b, or c, shall be cause for the entire inspection panel of printed wiring boards associated with the microsection to be rejected. The following details apply if a single plating void is found:

(1) Type 2: If the plating void does not exceed the conditions of A.3.6.4.4.3, the entire lot (100-percent panel inspection) shall have test specimens from each inspection panel microsectioned and inspected for voids. If a plating void is present in any microsection mount representing an inspection panel, a referee microsection shall be performed using test coupon "A", "B, or "AB–R" from the opposite corner of that inspection panel. If the referee has no plating voids, that panel is acceptable, however, if a plating void is present in that microsection, that inspection panel of printed wiring boards shall be rejected.

(2) Types 3 and 4: If the plating void does not exceed the conditions of A.3.6.4.4.3, a referee microsection shall be performed using test coupons "A", "B", or "AB–R" from the opposite corner of the inspection panel. If the referee has no plating voids, the panel is acceptable, however, if a plating void is present in that microsection, that inspection panel of printed wiring boards shall be rejected.

f. Heatsink and thermal planes (see A.3.6.1.4 and figure G–4). The lateral dielectric spacing between the heatsink planes and adjacent conducting surfaces, nonfunctional lands, or plated-through holes shall be measured at the closest point between these surfaces.

g. Conductor finish plating and coating thickness (see A.3.6.2.1). Isolated thick or thin sections shall not be used for averaging.

A.4.8.2.4 Registration (types 3 and 4). Layer-to-layer registration shall be determined by either evaluating microsectioned test coupons (method II, see A.4.8.2.4.1) or by evaluating of special registration coupons when provided (method III, see A.4.8.2.4.2).

A.4.8.2.4.1 Method II (by cross-section). Method II registration shall be determined by using two printed wiring board test specimens taken from diagonal corners of the panel. Any combination of either the non-stressed specimens (as received) (see A.3.7.2.1) and or the resistance to soldering heat (see A.3.7.6.2) microsectioned printed wiring board test specimens can be used. One of the printed wiring board test specimen shall be cross-sectioned in the panel's length (X) direction and the other shall be cross-sectioned in the panel's width (Y) direction.

A.4.8.2.4.2 Method III (optional) (by registration test coupons). Method III registration shall be determined using registration test coupons, when provided by the printed wiring board fabricator, and techniques or methods approved by the qualifying activity and when applicable, the acquiring activity. Unapproved methods of measurement using registration test coupons shall be backed up by method II of A.4.8.2.4.1 using the appropriate test coupons (see table A–IV) from the same inspection panel.

A.4.8.3 Chemical inspection.

A.4.8.3.1 Ionic contamination (by resistance of solvent extract) (see A.3.7.3.1 and A.6.4). The printed wiring board shall be tested for ionic contamination in accordance with test method number 2.3.25 of IPC–TM–650. Other alternate test methods not specified in A.6.4 may be used in lieu of test method number 2.3.25 of IPC–TM–650 only when specifically approved by the Government acquisition activity. Such approval shall be determined on the basis that the alternate test method is demonstrated to have equal or better sensitivity and employs solvents with the ability to dissolve flux residue as does the alcohol-water solutions specified in test method number 2.3.25 of IPC–TM–650.

A.4.8.3.2 Resistance to solvents (marking ink or paint) (see A.3.7.3.2). Marking ink or paint resistance to solvents shall be tested in accordance with test method number 2.3.4 of IPC–TM–650. The following details apply:

a. The marked portion of the printed wiring board test specimen shall be brushed.

b. After the test, the printed wiring board test specimen shall be visually inspected in accordance with A.4.8.1 for legibility of marking and the requirements of A.3.7.3.2.

A.4.8.3.2.1 Sampling procedures. The resistance to solvents test shall be performed either during group A (every lot) or during group B (monthly).

A.4.8.3.2.2 Test specimens. The test specimens can be either production printed wiring boards or quality conformance test circuitry strip identification areas containing ink or paint marking. The minimum number of samples shall be at least one sample for each solution specified by the applicable test method (i.e., one sample for each solution required).

A.4.8.4 Physical inspections.

A.4.8.4.1 Adhesion, legend and marking (see A.3.7.4.1). The printed wiring board test specimen shall be inspected in accordance with test method number 2.4.1.1 of IPC–TM–650. The printed wiring board test specimen shall be as described in appendix H.

A.4.8.4.2 Adhesion, plating (see A.3.7.4.2). The printed wiring board shall be tested in accordance with test method number 2.4.1 of IPC–TM–650, with the following details and exceptions. When edge-board contacts are part of the pattern, at least one pull shall be on the contacts. Fresh tape shall be used for each pull. If overhang metal breaks off (slivers) and adheres to the tape, it is evidence of outgrowth, but not a plating adhesion failure.

A.4.8.4.3 Adhesion, solder mask (see A.3.7.4.3). The permanency and adhesion of cured solder mask shall be determined in accordance with test method number 2.4.28.1 of IPC–TM–650.

A.4.8.4.4 Bow and twist (see A.3.7.4.4). The printed wiring board shall be inspected for bow and twist in accordance with test method number 2.4.22 of IPC–TM–650.

A.4.8.4.5 Conductor edge outgrowth (see A.3.7.4.5). The extent of outgrowth, on conductors covered with metals other than fused tin-lead or solder coating, shall be determined by measuring the conductor width before and after mechanically removing the overhang metal. If a referee test is required, cross-sectioning of the conductor shall be performed. The procedure for removing overhang metal, for this test, shall be as follows:

a. Wet the printed wiring board specimen in tap water at approximately room temperature.

b. While wet, brush the printed wiring board specimen with a brass wire brush to remove the overhang metal. Brush in the direction of the functional line, using moderate pressure.

A.4.8.4.6 Rework simulation (see A.3.7.4.6).

A.4.8.4.6.1 Unsupported hole (see A.3.7.4.6.1). The printed wiring board test specimen holes shall be tested in accordance with test method number 2.4.21 of IPC–TM–650 with the following details and exceptions: Three holes for each test coupon shall be tested. Insert wires into the holes of selected lands and solder to lands by machine or hand, as applicable. The insert wire lead shall have a diameter so that the diameter of the hole will be at a maximum of .020 inch (0.51 mm) greater than the diameter of the inserted wire lead. The insert wires shall not be clinched. It shall be considered a failure when a land around an unsupported hole is loosened.

A.4.8.4.6.2 Plated through hole (see A.3.7.4.6.2). The printed wiring board test specimen plated-through holes shall be tested in accordance with test method number 2.4.36 of IPC–TM–650. The following details shall apply:

a. Unless otherwise specified, method A shall be used initially.

b. For designs with an overall printed board thickness greater than .120 inch (3.0 mm), one row of plated-through holes shall be used to assure that the pre-designated method to be used for the soldering and desoldering operation will produce satisfactory solder connections (the wire is wetted through the entire plated hole within the soldering time limits specified in the test method) for the printed wiring board test specimen design being tested.

c. In case of an unsatisfactory solder connection (an insufficient solder connection is produced or the soldering time exceeds the limits specified in the test method), another plated-through hole on the row shall be soldered using the soldering temperature of the next higher method (for example, method B if method A is insufficient, or method C if method B does not suffice) until a satisfactory solder connection is made. If the temperatures of method C still yields unsatisfactory solder connections, consult the qualifying activity for additional guidance before proceeding further with the testing.

d. Once a method that produces satisfactory solder connections has been determined, the soldering and desoldering operation shall proceed using a different row of plated-through holes which will be evaluated to the acceptance criteria of A.3.7.4.6.2 herein. The final test method used shall be noted in the test report.

A.4.8.4.7 Solderability (see A.3.7.4.7). Unless otherwise specified (see A.3.1.1), the printed wiring board test specimens shall be tested and inspected in accordance with the solderability test methods test described in appendix J of MIL–PRF–31032. For printed wiring boards using only surface mount components, the surface solderability test can be used in lieu of the hole solderability test. For mixed component designs (both surface mount and through hole attachment), unless otherwise specified, only the hole solderability test shall be performed.

A.4.8.4.7.1 Hole (plated-through hole) (see A.3.7.4.7.1). The printed wiring board test specimens shall be tested and inspected in accordance with the solderability test methods described in appendix J of MIL–PRF–31032.

A.4.8.4.7.2 Surface or surface mount land (see A.3.7.4.7.2). The printed wiring board test specimens shall be tested and inspected in accordance with the solderability test methods of described inappendix J of MIL–PRF–31032.

A.4.8.4.8 Surface peel strength (types 3 and 4 using foil lamination) (see A.3.7.4.8). The printed wiring board test specimen shall be tested and inspected in accordance condition A of test method number 2.4.8 of IPC–TM–650. Conditions B and C (after thermal stress and after exposure to processing chemicals) shall not be performed. The test specimen shall be as specified in appendix H. All surface finish plating or coatings (e.g., plated tin-lead, solder coating, or other plated metals) on the foil shall be chemically removed prior to test or shall be prevented from being deposited during manufacturing. The test specimen shall not be coated with any organic coating for test. No individual value in the calculation of the average peel strength shall be more than 1.5 pounds per inch (0.26 N/mm) less than the specified minimum value.

A.4.8.4.9 Solder mask cure (see A.3.7.4.9). The printed wiring board test specimens shall be inspected for cured of solder mask in accordance A.4.8.1.

A.4.8.5 Electrical inspection.

A.4.8.5.1 Continuity and isolation resistance, production screening. Printed wiring boards shall be electrically tested using either automatic or manual equipment capable of verifying the test level C requirements of IPC–9252 for 100 percent continuity and isolation resistance. The following details shall apply:

a. Unless otherwise specified, both horizontal and vertical adjacency testing is required.

b. Unless otherwise specified, the adjacency distance for horizontal adjacency testing shall be the IPC–9252 default of .050 inch (1.27 mm) minimum.

c. Unless otherwise specified, the adjacency distance for vertical adjacency testing shall be for the features on adjacent layers that are within the horizontal adjacency distance specified.

A.4.8.5.2 Continuity and isolation resistance, periodic and referee testing.

A.4.8.5.2.1 Circuit continuity (see A.3.7.5.2.1). A current shall be passed through each net by applying electrodes on the terminals at each end of the net. The current passed through the net shall not exceed those specified in the applicable design standard (see A.3.1.1 and appendix D) for the smallest conductor in the circuit. See IPC–9252 for additional guidelines.

A.4.8.5.2.2 Isolation resistance (circuit shorts) (see A.3.7.5.2.2). A test voltage shall be applied between each net and all other nets that are adjacent to the net under test. The voltage shall be applied between nets of each layer and the electrically isolated net of each adjacent layer. For manual testing, the voltage shall be 200 volts minimum and shall be applied for a minimum of 5 seconds. When automated test equipment is used, the minimum applied test voltage shall be as specified on the applicable master drawing. If a test voltage of the printed wiring board is not specified on the applicable master drawing, the test voltage shall be the maximum rated voltage of the net being tested. If no maximum rated voltage is specified, the minimum test voltage shall be 40 volts.

A.4.8.5.3 Circuit or plated-through hole short to metal core substrate (see A.3.7.5.3). A polarizing voltage of 500 volts shall be applied between conductors and or lands and the metal core substrate in a manner such that each conductor and or land is tested to the conditions of A.4.8.5.2.2.

A.4.8.5.4 Dielectric withstanding voltage (see A.3.7.5.4). The printed wiring board test specimen shall be tested in accordance with test method number 2.5.7 of IPC–TM–650, test condition B. The following details and exceptions apply:

a. Test specimen: The test specimen shall be as identified in table A–VII or table H–I. The test specimen shall have previously been subjected to the moisture and insulation resistance test.

b. Test specimen preparation: This portion of the test method shall be skipped. DWV testing shall be performed once the test specimen has stabilized to laboratory ambient temperatures; however, the testing shall begin no later than 2 hours after removal of specimen from the moisture chamber.

c. Points of application: The dielectric withstanding voltage shall be applied between all common portions of each conductor pattern and all adjacent common portions of each conductor pattern. The voltage shall be applied between conductor patterns of each layer and the electrically isolated pattern of each adjacent layer.

A.4.8.5.5 Impedance testing (see A.3.7.5.5). Impedance testing shall address the parameters required by the level C requirements of IPC–9252.

A.4.8.6 Environmental inspection.

A.4.8.6.1 Moisture and insulation resistance (MIR) (see A.3.7.6.1).

A.4.8.6.1.1 Non-flush conductor printed boards (see A.3.7.6.1.1). The printed wiring board test specimen shall be tested in accordance with test method number 2.6.3 of IPC–TM–650, class 3, test specimen preparation method A (with conformal coating). The initial and final resistance measurements shall be taken at 500 volts direct current (+25 volts direct current, –0 volts direct current).

A.4.8.6.1.2 Flush conductor printed boards (see A.3.7.6.1.2). The test specimens shall be inspected in accordance with A.4.8.6.1.1 with the following details and exceptions:

a. The specimen shall be conditioned with 100 V direct current +/– 15 percent, applied between all conductors for a minimum of 60 seconds within 2 minutes after removal of the test specimen from the humidity chamber.

b. The insulation resistance measurement shall be taken within 60 seconds after electrical conditioning.

A.4.8.6.2 Resistance to soldering heat (see A.3.7.6.2).

A.4.8.6.2.1 Solder float thermal stress (for designs using component holes) (see A.3.7.6.2). Unless otherwise specified, this test shall be performed on only one side of the printed wiring board for a single cycle.

A.4.8.6.2.1.1 Type 1 (see A.3.7.6.2.1.1). The printed wiring board test specimen shall be tested in accordance with test condition A of appendix F of MIL–PRF–31032 except that post evaluation microsectioning is not required.

A.4.8.6.2.1.2 Types 2, 3 and 4 (see A.3.7.6.2.1.2). The printed wiring board test specimen shall be tested in accordance with test condition A of appendix F of MIL–PRF–31032 except that the pretest conditioning may be eliminated at the manufacturer's option. The following details shall apply.

a. Test specimens constructed of glass reinforced thermoset resin base materials shall be subjected to test condition A.

b. Test specimens constructed of aramid reinforced thermoset resin base materials shall be subjected to test condition B.

c. Test specimens constructed of thermoplastic resin base materials shall be subjected to test condition C.

A.4.8.6.3 Thermal shock (see A.4.8.6.3).

A.4.8.6.3.1 Thermoset base materials. The printed wiring board test specimen shall be tested in accordance with test method number 2.6.7.2 of IPC–TM–650, with the following details:

a. Test specimen: See table H–I.

b. Test condition: D, E, or F (see E.4.1.2).

c. Maximum change in resistance: 10 percent.

A.4.8.6.3.2 Thermoplastic base materials. The printed wiring board test specimen shall be tested in accordance with test method number 2.6.7 of IPC–TM–650, test condition B, with the following details:

a. Test specimen: See table H–I.

b. Maximum change in resistance: 15 percent.

A.5. PACKAGING

A.5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see A.6.2). When packaging of materiel is to be performed by DoD or in house personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activity within the Military Service or Defense Agency, or within the Military Service's system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD–ROM products, or by contacting the responsible packaging activity.

A.6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory.)

A.6.1 Intended use. This appendix is intended to be used by manufacturers certified to the QML printed board specification, MIL–PRF–31032 to supply product to legacy drawings.

A.6.2 Acquisition requirements.

A.6.2.1 Primary acquisition requirements. Acquisition documents should specify the following:

a. Title, number, revision letter (with any amendment number when applicable), and date of this specification.

b. Appropriate type (see 1.2.1), base material designation (see 1.2.2), and grade of copper wrap (1.2.3).

c. Title, number, revision letter (with any engineering change proposal or notice of revision number when applicable), and date of the applicable master drawing (see A.3.1.1).

d. Title, number, revision letter (with any notice number when applicable), and date of the applicable design standard (see A.3.3).

e. Part identification (if applicable), and marking instructions including size, location, and application method (see A.3.1.1 and A.3.8).

f. Whether microsectioned test specimens, samples or photographs are required to be delivered with the order.

g. Packaging requirements (see A.5.1).

A.6.2.2 Additional acquisition requirements. Acquisition documents should also specify the following data, if applicable:

a. Design related if different than the applicable design standard (see appendix D).

(1) Minimum annular ring (external/internal)(see A.3.1.1), if different than the applicable design standard.

(2) Minimum conductor width (see A.3.1.1), if different than the applicable design standard.

(3) Minimum conductor spacing (see A.3.1.1), if different than the applicable design standard.

(4) Minimum dielectric thickness (see A.3.1.1), if different than the applicable design standard.

(5) Minimum edge spacing requirement (see A.3.1.1), if different than the applicable design standard.

(6) Copper plating thickness (see A.3.1.1), if different than the applicable design standard.

(7) Grade of copper wrap (see A.3.1.1), if different than the defaults of 1.2.3.

(8) Conductor finish plating (see A.3.1.1), if other than solder coating or tin-lead.

b. Conductor edge outgrowth or overhang, if applicable (see A.3.7.4.5).

c. Isolation resistance (circuit shorts) requirements including minimum applied test voltage (see A.3.7.5.1 and A.3.7.5.2.2).

d. Surface (foil lamination) peel strength, if applicable (see A.3.7.4.8).

e. Non-delivery of sample units which have not been subjected to electrical testing (circuit continuity and circuit shorts tests) and have passed all other tests to groups A and B inspection.

f. If special or other identification marking is required (see A.3.8).

g. Level of ionic contamination (cleanliness) (see A.3.7.3.1 and A.6.4).

A.6.3 Qualification.

A.6.3.1 Transference of qualification. Manufacturers currently qualified to MIL–PRF–55110G will have their qualification transferred to this document. The expiration date of their current qualification will not be changed. Qualifications in process (before the date of this document) will be performed to the requirements of the specification revision and amendment listed on the approved DLA Land and Maratime Authorization to Test Form. New applications for qualification (after the date of this document) will be performed to the requirements of this revision.

A.6.3.2 Qualification expiration and Qualified Products Database (QPD) 55110. Qualification listings within QPD–55110 for manufacturers qualified under this appendix (QPL product assurance level) includes the qualification expiration date as the last six digits of the test reference number. This date, formatted as (month/day/year), is the actual qualification expiration date for that listing. This date signifies that the company is no longer qualified (unless notified in writing by the qualifying activity) whether or not that individual listing has been removed the QPD. If the company has not requalified before the next issue of the QPD is published, then the listing will not be included on the updated QPD.

A.6.4 Ionic contamination testing (surface cleanliness). The values of ionic contamination specified in this document were established in the late 1970's by the U.S. Navy with the issuance of the Naval Air Center Materials Research Report No. 3–78. The values used in the report were eventually used in the cancelled specification MIL–P–28809 as a baseline needed for completed assemblies. The chemistries of the fluxes and cleaning solutions used in the 1970's were very different than what is used currently. If levels of ionic contamination that are needed for today's circuit card assemblies may be well below that threshold established in Naval Air Center Materials Research Report No. 3–78 or allowed by this document.

A.6.4.1 Flux removal. Selection of procedures for flux removal is at the manufacturer's discretion. A procedure should be chosen which will enable the printed wiring board fabricator to produce results enabling compliance with this document. Both polar and nonpolar solvents may be required to effect adequate flux removal.

A.6.4.2 Alternate methods and equipment. The following methods of determining the ionic contamination of printed wiring boards have been shown to be equivalent to the resistance of solvent extract test method:

a. The Kenco Alloy and Chemical Company, Incorporated, "Omega Meter™, Model 200."

b. Alpha Metals Incorporated, "Ionograph™" (see URL: http://www.scscookson.com).

c. Zero Systems, Incorporated, "Zero Ion™, Model ZI–100"(see URL: http://www.aqueoustech.com).

d. Westek, "ICOM 5000™."

Table A–IX lists the equivalence factors for these methods in terms of microgram equivalents of sodium chloride per unit area.

TABLE A–IX. Equivalence factors.

Method	Equivalence factors	Equivalents of sodium chloride		Related IPC-TM-650 test method
		Micrograms per square inch	Micrograms per square cm	
Resistance of solvent extract (ROSE)	1.00	10.06	1.56	2.3.25
Omega meter™	1.39	14.00	2.20	2.3.25
Ionograph™	2.01	20.00	3.10	2.3.25
Zero ion™	3.68	37.00	5.80	N/A
ICOM 5000™	2.20	22.00	3.40	N/A

A.6.5 Certified suitable laboratories (acceptable to the Government). Government accepted test laboratories are those facilities (either internal to the qualified manufacturer or a separate independent laboratory) that have demonstrated their ability to perform the verification testing required by this document. A listing of those certified laboratories is available at https://landandmaritimeapps.dla.mil/Offices/Sourcing_and_Qualification/labsuit.aspx. Search for a document titled "PWB Commercial Lab List (31032/50884/55110)".

A.6.6 Alternate test methods. Other test methods may be substituted for those specified herein provided it is demonstrated to and approved by the qualifying activity that such a substitution in no way relaxes the requirements of this specification.

A.6.7 Group B sample critical design details. Past versions of this document contained default design details that were assumed to apply to all test coupons subjected to group B inspection, regardless of the master drawing design requirements. With the issuance of this document, the design details which were universally used to determine acceptance or failure of the group B samples, are no longer considered universally applicable to the group B test coupons. The printed wiring board design details (plating thickness, dielectric separation, external, and internal annular ring, etc.) or the default design standard that applies to the test coupons, should be submitted along with test coupons so that a proper group B evaluation of the design can be verified.

EXAMPLE: The master drawing of the most complex design selected for group B testing requires .0015 inch (0.038 mm) of copper plating thickness, .006 inch (0.15 mm) of dielectric spacing, and .003 inch (0.076 mm) internal annular ring. These design details are considerably different than the baseline design parameters found in IPC–2221. If on these same samples, the certified suitable laboratory found that the samples exhibited .001 inch (0.025 mm) of copper plating thickness, .005 inch (0.13 mm) of dielectric spacing and .002 inch (0.051 mm) internal annular ring, the manufacturer or certified suitable laboratory could not claim, state, or certify that the results of group B testing or the samples met the master drawing or specification requirements.

A.6.8 Tin finishes (see A.3.4.2). The use of alloys with tin content greater than 97 percent may exhibit tin whisker growth problems after manufacture. Tin whiskers may occur anytime from a day to years after manufacture, and can develop under typical operating conditions on products that use such materials. Tin whisker growth could adversely affect the operation of electronic equipment systems. Conformal coatings applied over top of a whisker-prone surface will not prevent the formation of tin whiskers. Alloys of 3 percent lead have shown to inhibit the growth of tin whiskers. For additional information on this matter refer to ASTM B545.

A.6.9 Alternate microsection preparation procedure guidelines. IPC–MS–810 "Guidelines for High Volume Microsection" contains many recommendations and suggestions that can be helpful in preparing microsection mounts containing multiple test specimens.

A.6.10 Microsection mount microetch caution. Prior to microetching, if lines are visible in the areas of inner layer to hole wall interfaces, care should be taken to not over-etch the mount so that the various plating layers will still be visible in the etched mount. This will enable accurate determination as to whether the line is separation or a polishing artifact.

A.6.11 Blind, buried, and through vias. This specification includes provisions for verifying the performance of rigid printed wiring boards containing blind vias, buried vias, controlled depth drilled vias, laser drilled vias, low aspect ratio blind vias, microvias, semi-blind vias, semi-buried vias, and through vias.

A.6.12 Referenced IPC–TM–650 test methods. The following test method numbers are referenced in this document:

2.1.1 – Microsectioning.
2.1.8 – Workmanship.
2.2.1 – Mechanical Dimensional Verification.
2.2.2 – Optical Dimensional Verification.
2.2.5 – Dimensional Inspections Using Mircosections.
2.3.4 – Chemical Resistance, Marking Paints and Inks.
2.3.25 – Detection and Measurement of Ionizable Surface Contaminants by Resistivity of Solvent Extract.
2.4.1 – Adhesion, Tape Testing.
2.4.1.1 – Adhesion, Marking Paints and Inks.
2.4.8 – Peel Strength of Metallic Clad Laminates.
2.4.15 – Surface Finish, Metal Foil.
2.4.21 – Land Bond Strength, Unsupported Component Hole.
2.4.22 – Bow and Twist (Percentage).
2.4.28.1 – Adhesion, Solder Resist (Mask), Tape Test Method.
2.4.36 – Rework Simulation, Plated-Through Holes for Leaded Components.
2.5.7 – Dielectric Withstanding Voltage, PWB.
2.6.3 – Moisture and Insulation Resistance, Printed Boards.
2.6.7.2 – Thermal Shock, Continuity and Microsection, Printed Board.

A.7. DEFINITIONS

A.7.1 As received (microsection inspection). As received means after tin alloy plating is reflowed or fused or after solder coating but prior to thermal stress, rework simulation, or thermal shock testing.

A.7.2 Board thickness. The overall printed wiring board thickness includes metallic depositions, fusing, and solder mask. The overall thickness is measured across the printed wiring board extremities (thickest part), unless a critical area, such an edge-board contacts or card guide mounting location, is identified on the master drawing.

A.7.3 Commercial and Government Entity (CAGE) code. The Commercial and Government Entity Code, or CAGE Code, is a 5 digit identifier assigned to suppliers to the Federal Government of the United States of America in order to provide a standardized method of identifying a given facility or a specific location. CAGE was previously known as Federal Supply Code for Manufacturers (FSCM) and also the National Supply Code for Manufacturers (NSCM). U.S. based companies can obtain CAGE code information at URL: https://cage.dla.mil/search. Non-U.S. based companies can obtain CAGE information at URL: https://eportal.nspa.nato.int/AC135Public/scage/CageList.aspx.

A.7.4 Complexity of a printed board design, construction, or materals (as related to group B testing). Complexity of printed wiring boards will usually depend on the base materials used; dielectric layer thickness; overall printed wiring board thickness; number of conductor layers; conductor widths and spacings; intricacy of patterns; size, quantity, aspect ratio and positioning of plated holes; tolerancing of any or all of the above; the presence of internal heatsink planes or thermal planes, and all combinations of the above with respect to their manufacturing difficulty, and their effects upon the consistent ability of the printed wiring boards to meet the requirements of the periodic testing, unless otherwise specified by the contracting activity.

A.7.5 Conductive interfaces. The term conductive interfaces is used to describe the junction between the hole wall plating or coating and the surfaces of internal and external layers of metal foil. The interface between platings and coating (electroless copper, direct metallization copper, vapor deposited copper, non-metallic electroless copper substitutes, etc., and electrolytic copper, whether panel or pattern plated), are also considered a conductive interface.

A.7.5.1 External conductive interfaces. An external conductive interface is considered to be the junction between the surface copper foil and the deposited or plated copper.

A.7.5.2 Internal conductive interfaces. An internal conductive interface is considered to be the junction between the internal layers (copper foil posts or internal layers) and the deposited or plated copper.

A.7.6 Contract service. Contract services are those services contracted or performed (or both) outside the qualified manufacturer's immediate facility, not to include verification testing or electrical function tests. For the purposes of this appendix, the internal equipment/process condition applies only to those processes used to manufacture the qualification test specimen. When applying for qualification of contracted services, the process to be subcontracted and the company performing the contracted service shall be identified.

A.7.6.1 Mass lamination. Manufacturers requesting to use contract services lamination (mass lamination) will be qualified to types 3 or 4 of the same base material type requested. The qualification test specimens will be produced by the QPL manufacturer and the mass laminator and should be representative of the subsequent production process.

A.7.6.2 Sub-assembly (mass lamination) facility. A facility authorized, by both the manufacturer and the qualifying activity, to perform manufacturing steps in accordance with processing procedures contained in the qualified product system.

A.7.7 Destructive physical analysis (DPA). A DPA is a systematic, logical, detailed examination of parts during various stages of physical disassembly, conducted on a sample of completed parts from a given lot, wherein parts are examined for a wide variety of design, workmanship, and processing problems that may not show up during normal screening tests. The purpose of these analyses is to determine those lots of parts, delivered by a vendor, which have anomalies or defects such that they could, at some later date, cause a degradation or catastrophic failure of a system.

A.7.8 First piece produced design inspection. The analysis of the first item manufactured in a production run to verify correct setup and process alignment.

A.7.9 Inspection panel. A production panel which includes a sufficient quantity of QCTC necessary to complete all qualification inspections or group A and group B verifications, as applicable. Inspection panels may have been wholly or partially processed as a larger production panel. Separation of a production panel into multiple inspection panels is acceptable if each of the smaller sub-panels contain a sufficient quantity of QCTC necessary to complete all qualification inspections or group A and group B verifications, as applicable. In order for printed boards to be potential compliant printed boards, they must have been processed on inspection panels.

A.7.10 Printed board thickness. See “board thickness”.

A.7.11 Printed wiring board test specimen. The term printed wiring board test specimen is used to describe all of the following; production printed wiring boards, qualification test specimens, or test coupons.

A.7.12 Quality–conformance test circuitry (QCTC). See IPC–T–50.

A.7.13 Quality assurance. Quality assurance is a planned and systematic pattern of all actions necessary to provide adequate confidence that adequate technical requirements are established; products and services conform to established technical requirements; and satisfactory performance is achieved.

A.7.13.1 System. A composite of equipment, skills, and techniques, that is capable of performing or supporting an operational role or both. A complete system includes all equipment, related facilities, material, software, services, and personnel required for its operation and support to the degree that it can considered self-sufficient in its intended operational environment.

A.7.14 Referee testing. The re-inspection or testing of a printed board attribute for the purpose of resolving an acceptance issue at the request of the acquiring activity, manufacturer, or the qualifying activity.

A.7.15 Resin systems families.

A.7.15.1 Thermoset resin. For the purposes of this document, base materials conforming to the following legacy type designators are classified as containing thermosetting resins: AF, BF, AI, BI, GB, GC, GF, GH, GI, GM, QI, and SC.

A.7.15.2 Thermoplastic resin. For the purposes of this document, base material conforming to the following legacy type designators are classified as containing thermoplastic resin: GR, GP, GT, GX, and GY.

A.7.16 Screenable defect. A screenable defect is one for which an effective, nondestructive screening test or inspection can be reasonably developed and applied to eliminate with confidence the nonconforming items from the lot.

A.7.17 Solder mask terms.

A.7.17.1 Chalking (of cured solder mask). When the solder mask is degraded such that fine particulates can be removed from the surface.

A.7.17.2 Crazing (of cured solder mask). A network of fine cracks on the surface of or within the coating.

A.7.17.3 Soda straw voids. A soda straw void is a long tubular-like void along the edges of conductive patterns where the solder mask is not bonded to the base material surface or the edge of the conductor. Contaminents such as tin/lead fusing fluxes, fusing oils, solder fluxes, cleaning agents, or volatile materials can be trapped in the soda straw void.

A.7.17.4 Tented solder mask. Tenting refers to a via with a dry film mask material applied bridging over the via wherein no additional materials are in the hole. It may be applied to one side or both sides of the via structure.

A.7.18 Traceability code. The manufacturer defined traceability code is used to insure traceability between the printed wiring boards and the quality conformance test circuitry that represent them for manufacturing history.

A.7.19 Visual defect terms.

A.7.19.1 Blister. A blister is delamination in the form of a localized swelling and separation between any of the layers of a lamination base material, or between base material and conductive foil, or protective coating.

A.7.19.2 Delamination. A separation between plies within a base material, between a material and conductive foil, or any other planar separations within a printed wiring board.

PRODUCT ASSURANCE REQUIREMENTS (PERFORMANCE AND VERIFICATION) FOR QUALIFIED MANUFACTURER LIST LEVEL

B.1 SCOPE

B.1.1 Scope. This appendix contains optional requirements concerning the QML product assurance level for printed wiring boards covered by this specification. This appendix is a mandatory part of the specification when the product assurance level of appendix A is not used. The information contained herein is intended for compliance when the product assurance requirements of appendix A are not used.

B.2 APPLICABLE DOCUMENTS

B.2.1 General. The documents listed in this section are specified in sections B.3 and B.4 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections B.3 and B.4 of this specification, whether or not they are listed.

B.2.2 Government documents.

B.2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

MIL–PRF–31032	–	Printed Circuit Board/Printed Wiring Board, General Specification for.
MIL–PRF–31032/1	–	Printed Wiring Board, Rigid, Multilayered, Thermosetting Resin Base Material, with or Without Blind and Buried Plated through Holes, for Soldered Part Mounting.
MIL–PRF–31032/2	–	Printed Wiring Board, Rigid, Single And Double Layer, Woven E-Glass Reinforced Thermosetting Resin Base Material, with or without Plated Holes, for Soldered Part Mounting.
MIL–PRF–31032/5	–	Printed Wiring Board, Rigid, Multilayered, Thermoplastic, Thermosetting, or Thermoplastic and Thermosetting Resin Base Material, with Plated Through Holes, for High Frequency Applications.
MIL–PRF–31032/6	–	Printed Wiring Board, Rigid, Single and Double Sided, Thermoplastic Resin Base Material, with or without Plated-Tthrough Holes, for High Frequency Applications.

(Copies of these documents are available online at http://quicksearch.dla.mil.)

B.2.3 Order of precedence. Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

B.3 REQUIREMENTS

B.3.1 Performance requirements. The performance requirements of the applicable MIL–PRF–31032 specification sheet shall apply to all printed wiring boards procured to the QML product assurance level.

B.3.2 Accept/reject criteria. The accept/reject criteria of the applicable MIL–PRF–31032 specification sheet shall apply to all printed wiring boards procured to the QML product assurance level.

B.3.3 QML brand. At the option of the manufacturer, the QML brand specified in MIL–PRF–31032 may be placed on printed wiring boards that comply with the product assurance requirements of this appendix.

B.4 VERIFICATION

B.4.1 Qualification inspection. Manufacturers shall be qualified for listing on QML–31032 for the technology and capabilities required to produce printed boards under this appendix.

B.4.2 QML product assurance. The product assurance requirements for the QML level of printed wiring board furnished under this specification shall be satisfied by certification to MIL–PRF–31032. All printed wiring boards manufactured and delivered in compliance with this appendix shall be produced in accordance with the approved quality management plan.

B.4.3 Printed wiring board performance verification. Printed wiring board performance verification inspection shall consist of inspections on the production printed wiring boards and test coupons specified in the applicable MIL–PRF–31032 specification sheet. The following details are applicable to the QML product assurance level:

a. Lot conformance inspection (LCI) product acceptance testing shall be based on the applicable verification flows (in-process and group A) offered by this document (see A.4.4 and appendix D) or the routine from a similar technology described by a MIL–PRF–31032 specification sheet. The various verification flows shall be based upon the design standard used to design the printed wiring boards and the available panel test coupons for the printed wiring boards.

b. MIL–PRF–31032 periodic conformance inspection (PCI) program can be used in lieu of group B inspection (see A.4.7.1).

c. Test optimization is applicable to this appendix and can be applied to any verification flow detailed in this document.

B.5 PACKAGING

B.5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see A.6.2). When packaging of materiel is to be performed by DoD or in house personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activity within the Military Service or Defense Agency, or within the Military Service’s system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD–ROM products, or by contacting the responsible packaging activity.

B.6 NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory.)

B.6.1 Intended use. This appendix is intended to be used by manufacturers certified to MIL–PRF–31032 and qualified to MIL–PRF–31032/1, MIL–PRF–31032/2, MIL–PRF–31032/5, or MIL–PRF–31032/6 to reduce the complexity of maintaining multiple product/process and testing flows (both MIL–PRF–55110 or MIL–PRF–31032) within a the manufacturing and testing facility.

B.6.2 Application of the QML product assurance level to existing requirements.

B.6.2.1 Use of existing master drawings. The QML printed wiring board manufacturer can use pre-existing master drawing without any modifications. Production masters and tooling may need to be modified to account for type, design, placement, and quantity of test coupons needed for compliance to this appendix.

B.6.2.2 Form, fit, and function. The form, fit, and function of the printed wiring boards, whether the QML product assurance level or the QPL product assurance level is used, will be the same.

B.6.2.3 Certification of conformance. The printed wiring boards can be certified as being compliant to appendix B of this document (MIL–PRF–55110).

B.6.3 Benefits of the QML product assurance level. Printed wiring boards produced by QML manufacturers using the provisions of this appendix in lieu of previous revisions would be compliant to this specification (MIL–PRF–55110) in accordance with the QML product assurance level with the added benefits as follows:

a. The QML manufacturer can use pre-existing master drawing without any modifications. Production masters and tooling may need to be modified to account for type, design, placement, and quantity of test coupons needed for compliance to this appendix.

b. The printed wiring boards, whether the QML option or the QPL option is used, will be the same.

c. The level of quality will be the same or higher than the QPL product assurance level.

d. When using the correct verification test (for the design), the cost should be the same or less due to enhancements made to accept/reject criteria.

e. Customers will be more confident that a QML manufacturer has demonstrated the capabilities to build its design dues to its QML certification and qualification rather the generic standardized qualification test vehicle of the QPL quality assurance level portion of previous revisions of this document.

B.6.4 Retention issues. The manufacturer need only to keep the qualifying activity apprised of its total QML program, i.e., their MIL–PRF–31032 QML program and this specification's QML product assurance level. This means that the manufacturer does not have to maintain two separate compliance programs, (i.e., no requirement for a QPL compliance program for this specification to be separate from a QML program for MIL–PRF–31032).

B.6.5 Certificates of compliance issues. The manufacturer can certify QML printed wiring boards processed under their MIL–PRF–31032 QML program as compliant to this document. The certificate of compliance should reference the QML product assurance level to differentiate the compliant product from printed wiring boards verified using the QPL product assurance level offered in this document.

B.6.6 Past specification revisions (see appendix D). Printed wiring boards procured to this document meets and exceeds all quality and reliability requirements of previous revisions of MIL–P–55110 or MIL–PRF–55110.

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C = 0 (ZERO DEFECT) SAMPLING, TEST EQUIPMENT, AND INSPECTION FACILITIES

C.1 SCOPE

C.1.1 Scope. This appendix details the statistical sampling procedures to be used with the QPL product assurance level of this specification. It also details requirements and procedures pertaining to test equipment and inspection facilities. This appendix is a mandatory part of the specification. The information contained herein is intended for compliance.

C.2 APPLICABLE DOCUMENTS

C.2.1 General. The documents listed in this section are specified in sections C.3, C.4, or C.5 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections C.3, C.4, or C.5 of this specification, whether or not they are listed.

C.2.2 Non-Government publications. The following documents form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

ASTM INTERNATIONAL (ASTM)

ASTM E29 – Standard Practice for Using Significant Digits in Test Data to Determine Conformance with Specifications.

(Copies of this document are available online at http://www.astm.org.)

IPC – ASSOCIATION CONNECTING ELECTRONICS INDUSTRIES (IPC)

IPC–QL–653 – Certification of Facilities that Inspect/Test Printed Boards, Components and Materials.

(Copies of this document are available online at http://www.ipc.org.)

INTERNATIONAL ORGANIZATION FOR STANDARDIZATION (ISO)

ISO 17025 – General Requirements for the Competence of Testing and Calibration Laboratories.

(Copies of this document are available online at http://www.iso.org.)

NCSL INTERNATIONAL (NCSL)

NCSL Z540.3 – Requirements for the Calibration of Measuring and Test Equipment.

(Copies of this document are available online at http://www.ncsli.org.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

C.2.3 Order of precedence. Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

C.3 DEFINITIONS AND SYMBOLS FOR C = 0 SAMPLING

C.3.1 Definitions. The following definitions shall apply for all statistical sampling procedures:

a. C = 0 sample plan: The C = 0 sample plans are defined as a combination of a test specimen usage identifier (see C.3.1.b) and a sample size series (see C.3.1.c). The resulting C = 0 sample plan will be a two character designator combination that identifies the sample size series that is to be with a type of test specimen for a particular verification (see C.4.5).

b. Test specimen usage identifier (see C.4.5 for examples): The following usage modifiers are used to differentiate when a particular plan is to be used for a particular test specimen:

(1) The letter "B" will be used to signify that production printed boards are to be sampled.

(2) The letter "T" will be used to signify that test coupons are to be sampled based on the number of panels in the lot.

(3) An asterisk " * " will be used for either printed boards or test coupons.

c. Sample size series: The sample size series is defined as the following series of letters: "A", "D", "F", "H", "J", "L", and "N" that are listed in table C–I (see C.4.5 for examples).

NOTE: Sample size series "A" was identified as "B" in previous revisions.

d. Tightened inspection: Tightened inspection is defined as sampling using an increased sample size (see C.4.3).

e. Acceptance number (C): The acceptance number is defined as an integral number associated with the selected sample size which determines the maximum number of defectives permitted for that sample size.

f. Rejection number (R): Rejection number is defined as one plus the acceptance number.

C.3.2 Symbols. The following symbols shall apply for all statistical sampling procedures:

a. C: Acceptance number.

b. R: Rejection number.

C.4 STATISTICAL SAMPLING PROCEDURES AND SAMPLE PLAN TABLE

C.4.1 General. Statistical sampling shall be conducted using the C = 0 method. The C = 0 method as specified herein is a sampling plan that provides a high degree of assurance that a lot having a proportion defective greater than the specified acceptance number (C = 0) will not be accepted. For all situations, the acceptance number (C) shall be equal to 0 (C = 0) and the rejection number (R) shall be 1 or greater (R ≥ 1).

C.4.2 Acceptance and procedure.

C.4.2.1 Acceptance number (C = 0). Acceptance of inspection lots shall be based on an acceptance number of zero (C = 0).

C.4.2.2 Rejection number (R ≥ 1). Failure of a sample unit for one or more tests of a subgroup shall be charged as a single failure. One or more sample rejects shall be cause for failure of the lot or sublot, as applicable. Any failure on any of the sample units shall constitute a failure of the entire inspection lot or sublot.

C.4.3 Tightened inspection (for reevaluation purposes). Tightened inspection shall be performed by sampling using double the sample size as specified in table C–I with zero failures allowed or 100 percent.

C.4.4 Sample size. The sample size for each subgroup shall be determined from table C–I. If lot size is smaller than sample size, test all of the units. The manufacturer may, at their option, select a sample size greater than that required; however, the number of failures permitted shall not exceed the acceptance number.

C.4.5 C = 0 sample plan construction (selection and usage of the sample size series). The sample size series of table C–I to be used will be directed from the appropriate inspection table. The inspection table will specify the C = 0 sample plan (test specimen identifier and sample size series) or plans (test printed wiring board, panels, or either one) to use.

EXAMPLES: If an inspection table specified that "Plan BF or TL" be used when verifying test specimens, it is specifying that sample size series "F" of table C–I shall be used for selecting printed wiring boards and sample size series "L" shall be used for selecting test coupons from panels. If the same inspection table specified that "Plan *D" be used, then sample size series "D" of table C–I can be used for either printed wiring boards or panels.

TABLE C–I. C = 0 (zero defect) sampling.

Lot size	Sample size (number of test specimens to be inspected) 1/						
	Series A	Series D	Series F	Series H	Series J	Series L	Series N
1 to 8	All	All	All	5	3	2	1
9 to 15	All	All	13	5	3	2	1
16 to 25	All	All	13	5	3	2	1
26 to 50	All	32	13	5	5	3	2
51 to 90	50	32	13	7	6	4	2
91 to 150	50	32	13	11	7	5	2
151 to 280	50	32	20	13	10	6	4
281 to 500	50	48	29	16	11	7	4
501 to 1,200	75	73	34	19	15	8	4
1,201 to 3,200	116	73	42	23	18	9	4

1/ If lot size is smaller than sample size test all of the units. Sample size series "A" was identified as "B" in previous revisions.

C.5 TEST EQUIPMENT, CALIBRATION, MEASUREMENTS, AND INSPECTION FACILITIES

C.5.1 Test equipment and calibration. All tests and measurements for process control, qualification testing, inspection of product for delivery (in-process and group A), or periodic conformance inspection (group B) shall be made with capable instruments whose accuracy has been verified. Calibration of measurement, test equipment, and test standards that control the accuracy of inspection and test equipment and facilities shall be in accordance with NCSL Z540.3 or equivalent. Calibrated test equipment and test standards shall be controlled, used, and stored in a manner suitable to protect calibration integrity. Test equipment requiring calibration shall be identified and labeled in accordance with NCSL Z540.3 or an equivalent system, approved by the qualifying activity.

C.5.1.1 Resolution of measurement devices and test equipment capability. Unless otherwise specified (see A.3.1.1), the resolution of measurement devices and test equipment used for the evaluation of printed board performance shall be at least a factor of 10 better than the limits or tolerances of a value to be determined. For example: a voltmeter would need a resolution of +/– 0.1 percent to determine a tolerance of +/– 1 percent.
NOTE: State of the art requirements in which a 10:1 ratio cannot be effectively achieved due to a lack of national standards shall be justified and documented.

C.5.1.2 Electrical test frequency. When specified (see A.3.1.1), the frequency of the electrical test shall be the specified operating frequency of the printed board. Where a frequency range is specified, major functional parameters shall be tested at the maximum and minimum frequencies of the range in addition to those tests conducted at any specified frequency within the range. Whenever electrical tests are conducted on printed boards for which a range of frequencies, or more than a single operating frequency is specified, the frequency at which tests are conducted shall be recorded along with the parameters measured at those frequencies.

C.5.2 Test methods.

C.5.2.1 Acquiring activity or manufacturer imposed tests. Acquiring activity or manufacturer imposed tests shall be in accordance with the requirements specified in the master drawing. If any additional imposed tests detect a problem, the manufacturer shall submit all panels/printed wiring boards in the lot to those tests to eliminate rejects and shall take steps to determine and eliminate the cause of failure.

C.5.2.2 Test method alternatives or variations. Alternate test methods, or variation from the specified test method, are allowed provided that it is demonstrated to the qualifying activity or their agent that such alternatives or variations in no way relax the requirements of this performance specification or the referenced test method. Alternate test methods or variation from the specified test method shall be approved by the qualifying activity or their agent before testing is performed. For proposed test variations, a test method comparative error analysis shall be made available for checking by the qualifying activity or their agent (see appendix B).

C.5.2.3 Procedure in case of test equipment malfunction or inspection/test personnel error. When it has been established that a improper test is due to test equipment malfunction or inspection/test personnel error, the inspection facility shall document the results of its investigations and corrective actions, if required, and shall make this information available to the qualifying activity and the acquiring activity, as applicable.

C.5.3 Numeric reporting. The results of printed wiring board verification shall be presented in accordance with requirements outline herein.

C.5.3.1 Observed values (true and nominal). The specification limit requirements specified are for true values. Nominal values are indicated by the inclusion of a tolerance. Proper allowance shall be made for measurement errors (including those due to deviations from nominal test conditions) in establishing the working limits to be used for the values to be measured, so that the values of the test specimen parameters (as they would be under nominal test conditions) can be determined properly.

C.5.3.2 Significant digits. Unless otherwise specified (see A.3.1.1), the significant digits to be retained of an observed value shall be in accordance with the resolution requirements of C.5.1.1.

C.5.3.3 Rounding method. For purposes of determining conformance with the specification limit, an observed value, or a calculated value, shall be rounded "to the nearest unit" in the last right-hand significant digit to be retained (see C.5.3.2) in expressing the specification limit, in accordance with the rounding method of ASTM E29. The significant digits to be retained of an observed value or calculated value shall reflect the resolution requirements of C.5.1.1.

Example 1: The minimum specified etchback requirement is .0002 inch. The resolution required of the measurement device in accordance with C.5.1.1 would to the +/– .00001 inch. The significant digit to be retained would be one digit to the right of requirement. For this example, the significant digit to be retained would be .0000X, where the "X" represents the significant digit. In a situation where a test personnel uses an instrument capable of resolution to +/– .000001 inch, a measurement of .000186 inch is determined for etchback on that test specimen. This value can be rounded to .00019 inch or reported as taken (.000186 inch). The observed value of .000186 inch cannot be rounded to .0002 inch.

Example 2: The maximum specified printed board thickness requirement is .090 inch. The resolution required of the measurement device in accordance with C.5.1.1 would to the +/– .0001 inch. For this example, the test personnel uses an instrument capable of resolution to +/– .0001 inch, and records measurements of .0899, .0900, .0898, and .0897 inch for the printed board thickness on that test specimen. The test determination of (.3594 / 4) .08985 inch is calculated. This test determination can be rounded to .0898 inch or reported as calculated. Rounding this value to .0899 inch would not be in accordance with the Rounding Method of ASTM E29.

C.5.4 Control based on uncertainty. Test processes that have complex characteristics are best performed and controlled by the application of uncertainty analysis. The overall uncertainty in a test or measurement process shall be determined and the impact of said uncertainty on the product parameter tolerance shall be taken into account. The methods used for determining uncertainty shall be defined and documented. The method selected may use any (or combinations) of the following forms:

a. Arithmetic addition (linear), normally produces an overly conservative estimate and reflects a highly improbable situation in which contributing errors are at their maximum limit at the same time and same direction.

b. Root Sum Square (RSS), normally applied where the errors tend to fit a normal distribution (gaussian) and are from independent sources.

c. Partial derivatives, used where complex relationships exist.

d. Monte Carlo simulation, used in very complex situations where other methods are not easily applied or do not fit.

e. Standard reference material (or controlled correlation device) testing providing observable data. NOTE: Observable data from a controlled device may be relied upon to provide feedback that confirms process performance is within statistical limits.

f. Analysis of systematic and random errors, applying corrections as applicable.

g. Any other recognized method of combining errors into an expression of uncertainty substantiated by an engineering analysis.

C.6 SUITABILITY OF INSPECTION FACILITIES

C.6.1 Suitability of inspection facilities. The inspection facility (either the manufacturer's site or a certified suitable laboratory) used to perform qualification testing and periodic conformance inspection shall be found suitable by the qualifying activity to the requirements of ISO 17025, IPC–QL–653, or equivalent for the performance of the tests and inspection requirements of compliant printed wiring boards. Additional details regarding the suitability status of an inspection facility are outlined in the DLA Land and Maritime publication "Laboratory Suitability Information" that can be obtained online at URL: "https://LandandMaritimeApps.dla.mil/Downloads/VQGeneral/Labsuit-Book-140116.pdf".

C.6.2 Suitability status and test reports. Granting of laboratory suitability to an inspection facility does not mean that the Government will automatically accept or approve a test report prepared by the inspection facility. Some common reasons for rejection of qualification and periodic conformance test reports are the following:

a. Testing prior to receipt of an authorization to test.

b. Failure to record actual test conditions or results.

c. Failure to perform the proper test.

d. Failure to perform the test on the proper qualification test specimen.

e. Failure to test the minimum number of samples specified.

f. Incorrect test procedures.

g. Use of improperly calibrated test equipment.

h. Use of test equipment not previously found acceptable by DLA Land and Maritime.

C.6.3 Referee testing. Concerns with sample condition or sample identification shall be made to the qualifying activity prior to commencement of the referee testing. Comments on deviations from the applicable test method shall be made immediately at the time of testing. Unresolved concerns shall be specific in nature and submitted in writing to the laboratory's designated qualifying activity representative and the other observer at the time of testing.

C.7 DEFINITIONS FOR TEST EQUIPMENT AND INSPECTION FACILITIES

C.7.1 Accuracy. A measure of the closeness of an individual measurement or the average of a number of measurements to the true value. Accuracy includes a combination of random error (precision) and systematic error (bias) components that are due to sampling and analytical operations.

C.7.2 Bias. The systematic or persistent distortion of a measurement process, which causes errors in one direction (i.e., the expected sample measurement is different from the sample's true value).

C.7.3 Calibration. Calibration is an activity related to measurement and test equipment. Calibration is the comparison of measurement standard, instrument, or item of known precision and bias with another standard, instrument, or item to detect, correlate, report, or eliminate by adjustment, any variation in the precision and bias of the item being compared. Use of calibrated measurement standard, instrument, or items provide the basis for value traceability of product technical specifications to national standard values.

C.7.4 Limit or specification limit. A specification limit are numerical requirements specified in appendix A, in the applicable master drawing, or in referenced documents, for the minimum or maximum value used for acceptance purposes.

C.7.5 Measurement and testing equipment. Tools, gauges, instruments, sampling devices, or systems used to calibrate, measure, test, or inspect in order to control or acquire data to verify conformance to specified requirements.

C.7.6 Precision. The degree to which a measurement standard, instrument, item, test, or process exhibits repeatability. Expressed statistically or through various techniques of Statistical Process Control (SPC), the term is many times used interchangeably with "repeatability". Precision is a measurement of how closely the analytical results can be duplicated.

C.7.7 Resolution. The smallest unit of readability or indication of known value on an instrument, device, or assemblage thereof. It is also related to the gradations on measuring instruments and the ability of the inspection/test personnel to interpret between those gradations. The resolution value is frequently used in the device literature to classify the instrument.

C 7.8 Standard reference material (SRM). A device or artifact recognized and listed by the National Institute of Standards and Technology (NIST) as having known stability and characterization. SRMs used in product testing provide traceability for technical specifications. SRMs do not require calibration when used and stored in accordance with NIST accompanying instructions. They are used as "certified materials".

C.7.9 Tolerance. The total amount by which a specific dimension is permitted to vary. A tolerance is indicated in this specification only if it is expressed as the variation about a specified value (also known as a "nominal value").

C.7.10 Uncertainty. An expression of the combined errors in a test measurement process. Stated as a range within which the subject quantity is expected to lie. Comprised of many components including: estimates of statistical distribution and results of measurement or engineering analysis. Uncertainty established with a suitable degree of confidence, may be used in assuring or determining product conformance and technical specifications.

C.8 NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory.)

C.8.1 Supporting documents. The documents in this section may be used as guidelines for understanding measurement and test assurance principals.

INTERNATIONAL ORGANIZATION FOR STANDARDIZATION (ISO)

ISO 10012	–	Measurement Management Systems – Requirements for Measurement Processes and Measuring Equipment.
ISO 14253–1	–	Geometrical Product Specifications (GPS) – Inspection by Measurement of Workpieces and Measuring Equipment – Part 1: Decision Rules for Proving Conformance or Non-Conformance with Specifications.

(Copies of these documents are available online at http://www.iso.org.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

C.8.2 Documents regarding uncertainty. The documents in this section may be used as guidelines in understanding measurement and test assurance principals.

ASME INTERNATIONAL (ASME)

ASME B89.7.3.1 – Guidelines For Decision Rules: Considering Measurement Uncertainty In Determining Conformance To Specifications.
ASME B89.7.3.2 – Guidelines for the Evaluation of Dimensional Measurement Uncertainty.

(Copies of these documents are available online at http://www.asme.org.)

INTERNATIONAL ORGANIZATION FOR STANDARDIZATION (ISO)

ISO GUIDE 98–3 – Uncertainty of Measurement – Part 3: Guide to the Expression of Uncertainty in Measurement.

(Copies of these documents are available online at http://www.iso.org.)

NCSL INTERNATIONAL (NCSL)

NCSL Z540.2 – U. S. Guide to the Expression of Uncertainty in Measurement.

(Copies of this document are available online at http://www.ncsli.org.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

SUPERSESSION, CONFORMANCE INSPECTION OPTIONS, AND USE OF LEGACY DESIGN STANDARDS

D.1 SCOPE

D.1.1 Scope. This appendix contains information and guidance concerning the supersession of legacy Department of Defense documents such as MIL–P–55110, revisions C, D, and E and cancelled DoD and industry printed board design standards. This appendix is not a mandatory part of this specification. The information contained herein is intended for guidance only.

D.2 APPLICABLE DOCUMENTS

D.2.1 General. The documents listed in this section are specified in sections D.3 and D.4 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections D.3 and D.4 of this specification, whether or not they are listed.

D.2.2 Non-Government publications. The following documents form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

IPC – ASSOCIATION CONNECTING ELECTRONICS INDUSTRIES (IPC)

IPC–T–50	–	Interconnecting and Packaging Electronic Circuits, Terms and Definitions.
IPC–2221	–	Printed Board Design, Generic Standard on.

(Copies of these documents are available online at http://www.ipc.org.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

D.2.3 Order of precedence. Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

D.3 DEFINITIONS

D.3.1 Design standard. A document that establishes the standard practices, guidelines, and default values for the design of printed wiring boards. Within this appendix, the term "design standard" is used to describe those documents that contain the design, construction, material, and test coupon requirements and guidelines.

D.3.2 Legacy designs or documents (superseded standards). See D.4.1.

D.3.3 Supersession. The act of replacing a legacy document that no longer exists or is no longer supported with a currently supported document.

D.3.4 Quality conformance test circuitry. See IPC–T–50.

D.4 SUPERSESSION

D.4.1 Superseded specifications.

D.4.1.1 General. Appendix A of this document includes the essential requirements of the previous revision and can be used to supersede the specifications listed in 6.6.4.

D.4.1.2 Reference to superseded specifications. All the requirements of this document (MIL-PRF-55110G) can be interchangeable with those of MIL–P–55110. Therefore, existing procurement documents (master drawings or OEM documents) referencing MIL–P–55110 need not be revised, updated, or changed to make reference to MIL–PRF–55110 in order for this document to be used.

D.4.2 Superseded standards. The following design standards have been superseded by IPC–2221 for all types and classes of rigid printed wiring boards:

a. MIL–STD–275D, dated 26 April 1978.

1. MIL–STD–275D with notice 1, dated 19 January 1979.

2. MIL–STD–275D with notice 2, dated 10 October 1979.

3. MIL–STD–275D with notice 3, dated 5 October 1980.

4. MIL–STD–275D with notice 4, dated 28 May 1982.

5 MIL–STD–275D with notice 5, dated 7 February 1984.

b. MIL–STD–275E, dated 31 December 1984.

1. MIL–STD–275E with notice 1, dated 8 July 1986.

c. IPC–D–275, dated September 1991.

1. IPC–D–275 with amendment 1, dated April 1996.

d. IPC–2221, dated February 1998.

1. IPC–2221 with amendment 1, dated January 2000.

e. IPC–2221A, dated May 2003.

f. IPC–2221B, dated November 2012.

D.4.2.1 Estimation of design standard used. When no design standard is listed on the master drawing, either the design activity or printed board manufacturer, should be contacted to ascertain which design standard should be used to verify the design parameters during group A or group B inspection.

D.4.2.2 Retooling. Printed wiring boards that were designed using superseded Department of Defense design standards may need to have its test coupons converted to types, designs, placement, and quantity specified in IPC–2221 and the quantity specified in appendix H.

D.4.3 Testing.

D.4.3.1 Group A testing. Group A testing should be performed to the specific revision, and amendment if applicable, called out by the acquisition documents. For example, if printed wiring boards are produced to MIL–P–55110D with amendment 1, MIL–P–55110D with amendment 3, and MIL–P–55110E, a manufacturer would be expected to perform group A testing, for the applicable lot, to the requirements of the revision specified. In those three different revisions (D with amendment 1, D with amendment 3, and E) a requirement for an acceptability criteria or test procedure may be the exact same, it might be slightly different, it may be significantly different, or there may not even be a requirement. Retention of qualification summaries for group A should list the lots produced, grouped by revision, and when applicable, revision with specific amendment.

D.4.3.2 Group B samples and testing. Samples to be selected for group B testing should be based on the most complex compliant printed wiring boards produced that month. For example, if printed wiring boards are produced to MIL–P–55110D, MIL–PRF–55110E with amendment 1, and MIL–PRF–55110F during a given month, and the most complex printed wiring boards produced that month were in the lot ordered to MIL–PRF–55110E with amendment 1, then that should be the lot from which the group B sample should be selected. The samples should be tested in accordance with MIL–PRF–55110E with amendment 1. If during that same month, printed wiring boards were produced to MIL–P–55110A and MIL–P–55110B, group B tests to those specific revisions would also be required in order to be compliant to those revisions, unless specifically specified in the contract.

D.4.4 Superseded test coupons.

D.4.4.1 General. Before MIL–P–55110C, test coupons were only used for first article inspection and not required for production. The production panel test coupons were introduced within MIL–P–55110C its associated design standard and were for the supplier certification program concept. The production test coupons of MIL–P–55110C should be used when already incorporated onto production tooling. New designs or jobs should use the test coupons specified in IPC–2221.

D.4.4.2 Test coupons, placement, quantity, and usage. Appendix H contains a table that specifies for each production panel the test coupon placement, quantity (see note) and usage.

NOTE: There needs to be a sufficient number of test coupons on the production panel in order to be able to perform group A and, when necessary, group B inspection regardless of the number of test coupons specified by the design standard.

D.4.5 Intended use and intent of this appendix. This appendix can be used to understand the test coupons that were referenced in previous revisions of this document. These guidelines are intended for the re-identification and proper usage of test coupons within this document that are, or were originally identified, in various legacy Department of Defense printed wiring board design standards. This appendix is intended for use in conjunction with a manufacturer's verification conformance compliancy program.

D.4.5.1 Revisions. Printed wiring boards tested to this document generally would meet or exceed the performance requirements of past revisions. However, due to various changes in acceptability and evaluation criteria, testing procedures, and test coupon sampling, an exact duplication of a previous revision cannot be claimed or made in all areas of concern. Manufacturers should not pick-and-choose or mix acceptability requirements or test procedures from one revision of MIL–PRF–55110 or MIL–P–55110 to another. Compliance should be either to MIL–P–55110C, MIL–P–55110D, MIL–P–55110E, MIL–PRF–55110E, MIL–PRF–55110F, MIL–PRF–55110G (with a specific amendment, if applicable), or this document entirely, unless the manufacturer documents a direct correlation between the revisions (with any amendments, if applicable) under consideration.

D.4.5.2 Test coupons, placement, quantity, and usage. Appendix H contains a table that specifies for each production panel the test coupon placement, quantity, and usage.

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QUALIFICATION REQUIREMENTS FOR ALL LEVELS OF PRODUCT ASSURANCE

E.1 SCOPE

E.1.1 Scope. This appendix contains the qualification requirements for all levels of product assurance of printed wiring boards covered by this specification. The process for extending qualification is also outlined herein. This appendix is a mandatory part of this specification. The information contained herein is intended for compliance.

E.2 APPLICABLE DOCUMENTS

E.2.1 General. The documents listed in this section are specified in sections E.3 and E.4 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections E.3 and E.4 of this specification, whether or not they are listed.

E.2.2 Government documents.

E.2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

MIL–PRF–31032	–	Printed Circuit Board/Printed Wiring Board, General Specification for.
MIL–PRF–31032/1	–	Printed Wiring Board, Rigid, Multilayered, Thermosetting Resin Base Material, with or Without Blind and Buried Plated through Holes, for Soldered Part Mounting.
MIL–PRF–31032/2	–	Printed Wiring Board, Rigid, Single And Double Layer, Woven E-Glass Reinforced Thermosetting Resin Base Material, with or without Plated Holes, for Soldered Part Mounting.
MIL–PRF–31032/5	–	Printed Wiring Board, Rigid, Multilayered, Thermoplastic, Thermosetting, or Thermoplastic and Thermosetting Resin Base Material, with Plated Through Holes, for High Frequency Applications.
MIL–PRF–31032/6	–	Printed Wiring Board, Rigid, Single and Double Sided, Thermoplastic Resin Base Material, with or without Plated-Tthrough Holes, for High Frequency Applications.

(Copies of these documents are available online at http://quicksearch.dla.mil.)

E.2.3 Order of precedence. Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

E.3 REQUIREMENTS FOR QUALIFICATION TEST SPECIMENS

E.3.1 Qualification inspection. Qualification testing shall be performed on suitable test vehicles in accordance with the qualifying activity approved MIL–PRF–31032 qualification test plan.

E.3.1.1 Expiration of qualification. Manufacturers already qualified to the QPL level of this document will retain that listing until it expires. The 3 year expiration time will not apply to any qualifications performed to this appendix.

E.3.1.2 Requalification. Products qualified in accordance with this appendix shall be monitored and maintained through the manufacturer's Capability Verification Inspection program and do not require requalifiication to this specification.

E.3.2 Reciprocal qualification from MIL–PRF–31032. A reciprocal qualification listing (i.e., from a technology qualified to a MIL–PRF–31032 specification sheet) to this document will depend on the level of QML technology qualified. Unless otherwise detailed in MIL–PRF–31032 qualification test plan, following guidelines will apply:

a. Printed wiring board type (see 6.4.5). The extent of qualification for base materials types defined in E.4 will apply. EXAMPLE: A type 2 qualification under MIL–PRF–31032/2 or MIL–PRF–31032/6 will not justify a type 3 qualification listing to this document.

b. Printed board material. The extent of qualification for base materials types defined in MIL–PRF–31032 will apply. EXAMPLE: A thermoplastic metal clad base material qualification under MIL–PRF–31032/5 will justify a thermoplastic flexible metal clad base material qualification listing to this document (of the corresponding type).

c. Complexity. Printed wiring board designs verified using the QML product assurance option shall flow through the conversion of customer requirements element of the approved Quality Management (QM) plan as described in MIL–PRF–31032, appendix A. The Technical Review Board (TRB) shall evaluate designs exceeding their current QML–31032 qualification listing to determine if the add–on qualification provisions of MIL–PRF–31032 shall be used. Reasons for not using the add–on qualification provisions shall be documented in the periodic status reports.

E.3.3 Retention (see B.6.4). The QML status report described in MIL–PRF–31032 will cover the retention requirements to this document.

E.4 EXTENT OF QUALIFICATION

E.4.1 Extent of qualification. The extent of qualification shall be in accordance with the following ranges specified in E.4.1.1 through E.4.1.5.4.

E.4.1.1 Printed wiring board type. Qualification of a particular printed wiring board type shall be extended to cover all conductor patterns of that same printed wiring board type produced.

a. Qualification of type 4 printed wiring boards (MIL–PRF–31032/1 or MIL–PRF–31032/5) shall be extended to cover types 1, 2 and 3 printed wiring boards.

b. Qualification of type 3 printed wiring boards (MIL–PRF–31032/1 or MIL–PRF–31032/5) shall be extended to cover types 1 and 2 printed wiring boards.

c. Qualification of type 2 printed wiring boards (MIL–PRF–31032/2 or MIL–PRF–31032/6) shall be extended to cover type 1 printed wiring boards.

E.4.1.2 Base material types. Printed wiring board designs using different base material types (mixed base materials) shall be fabricated by manufacturers qualified for all base materials required by the design. Qualification using base material (laminates) shall be as follows:

a. Qualification with woven glass reinforced thermosetting epoxy resin base material type FR-4 (legacy type GF) shall be extended to cover types G-11 and FR-5 (legacy types GB and GH) of woven glass reinforced thermosetting epoxy resin base materials.

b. Qualification with woven glass reinforced thermosetting polyimide resin base material type GPY (legacy type GI) shall be extended to cover all other types of woven glass reinforced thermosetting polyimide resin base materials.

c. Qualification with nonwoven glass reinforced thermoplastic polytetrafluoroethylene resin base material types (legacy type GR) shall be extended to cover all other types of nonwoven glass reinforced thermoplastic resin base materials (legacy type GP).

d. Qualification with woven glass reinforced thermoplastic polytetrafluoroethylene resin base material types (legacy type GY) shall be extended to cover all other types of woven glass reinforced thermoplastic resin base materials (legacy type GT and GX).

e. Qualification with non-woven glass reinforced thermoplastic polytetrafluoroethylene resin base material legacy type GX shall be extended to cover legacy type GT.

f. Qualification with woven glass reinforced thermosetting cyanate ester resin base materials shall be extended to cover all other types of woven glass reinforced thermosetting cyanate ester resin base materials.

g. Qualification using any other base materials shall qualify only that base material.

E.4.1.3 Conductor surface finish. The qualification of a conductor surface finish shall be extended to cover all compositions or thicknesses of that specific conductor surface finish material.

E.4.1.4 Solder mask. Qualification of any printed wiring board type shall be extended to cover the approved type with solder mask.

E.4.1.5 Processes.

E.4.1.5.1 Etchback. Qualification using etchback shall be extended to cover non-etchback. Manufacturer qualifying using contract service etchback shall submit two additional qualification test specimens fabricated using their own internal desmear process.

E.4.1.5.2 Foil lamination. Qualification using foil lamination shall be extended to cover cap lamination.

E.4.1.5.3 Mass lamination (see A.7.6.1). Qualification of a contract service lamination (four conductor layers) shall be extended to cover a contract service lamination of up to four conductor layers. Qualification of a contract service lamination (ten conductor layers) shall be extended to cover a contract service lamination of five or more conductor layers.

E.4.1.5.4 Process changes. Any changes to a manufacturer's qualified base material type, equipment, or processes will be reviewed by the qualifying activity for determination if partial or full requalification is necessary.

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EXTERNAL VISUAL AND DIMENSIONAL ILLUSTRATIONS

F.1 SCOPE

F.1.1 Scope. This appendix establishes uniform criteria for evaluating and classifying defects on partially complete or completed printed boards, qualification test specimens, and test coupons during visual and dimensional inspections. This appendix describes the desired, acceptable, and nonconforming conditions of printed boards that are externally observable. It represents the visual interpretation of minimum requirements set forth in appendix A of this specification. The criteria shall apply whether a 100-percent inspection or a sampling plan procedure is used. This appendix is a mandatory part of the specification for manufacturers supplying printed boards to the QPL product assurance level of appendix A. The information contained herein is intended for compliance.

F.2 APPLICABLE DOCUMENTS

F.2.1 General. The documents listed in this section are specified in sections F.3 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirement documents cited in sections F.3 of this specification, whether or not they are listed.

F.2.2 Non–Government publications. The following documents form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

IPC – ASSOCIATION CONNECTING ELECTRONICS INDUSTRIES (IPC)

IPC–A–600 – Acceptability of Printed Boards.

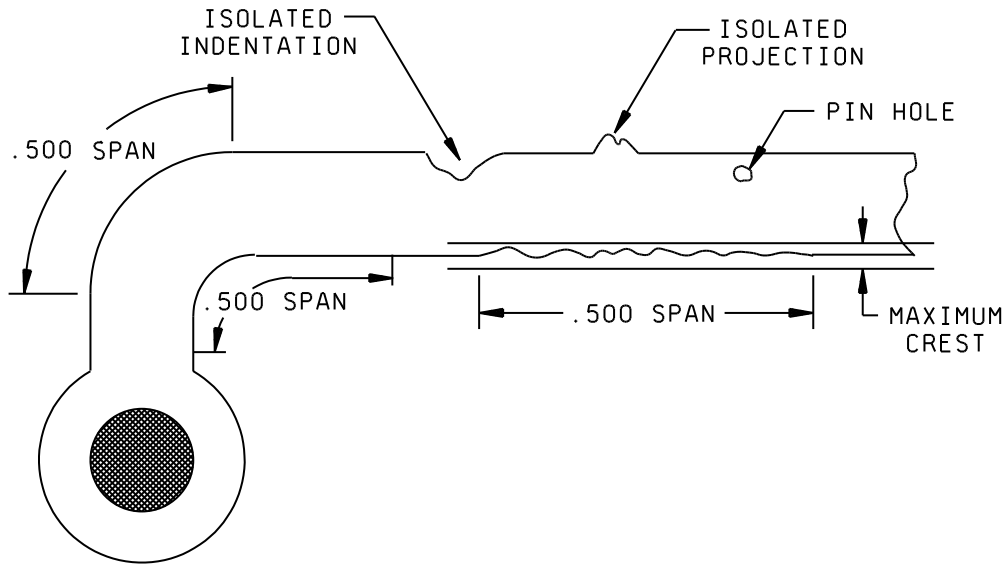
(Copies of these documents are available online at http://www.ipc.org.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

F.2.3 Order of precedence. Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

F.3 EXTERNALLY OBSERVABLE CHARACTERISTICS

F.3.1 General. This section addresses those characteristics which are observable from the surface of printed wiring boards. This includes those characteristics that are external and internal in the printed board, but visible from the surface (see figures F–1 through F–11). IPC–A–600 contains figures, illustrations, and photographs that can aid in the visualization of externally observable accept/reject conditions. If a condition is not addressed herein, or specified on the printed board procurement documentation, it shall comply with the class 3 "acceptable" or "target condition" criteria of IPC–A–600.



NOTES:
1. Dimensions are in inches.
2. The millimeter equivalent of .500 inch (12.7 mm) is given for general information only.

FIGURE F–1. Conductor edge definition imperfection measurement.

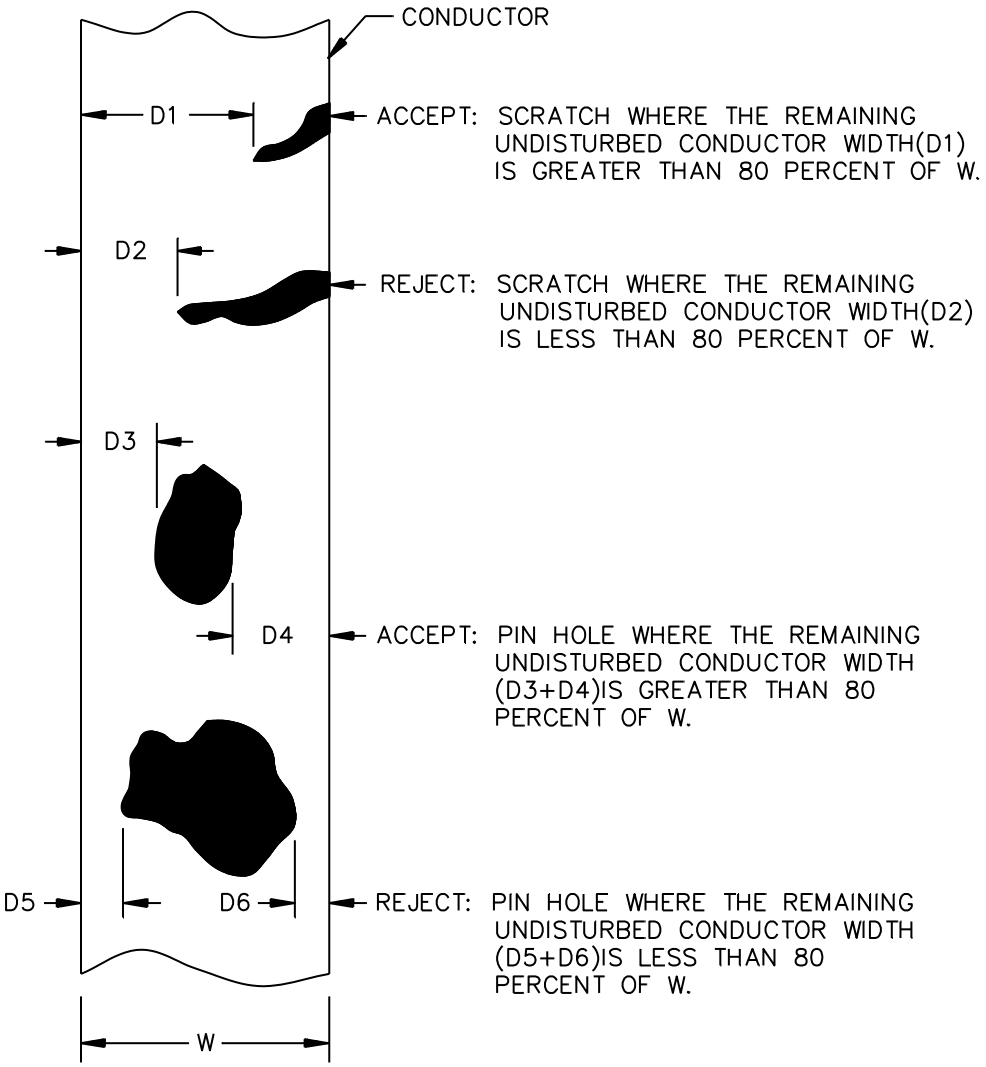
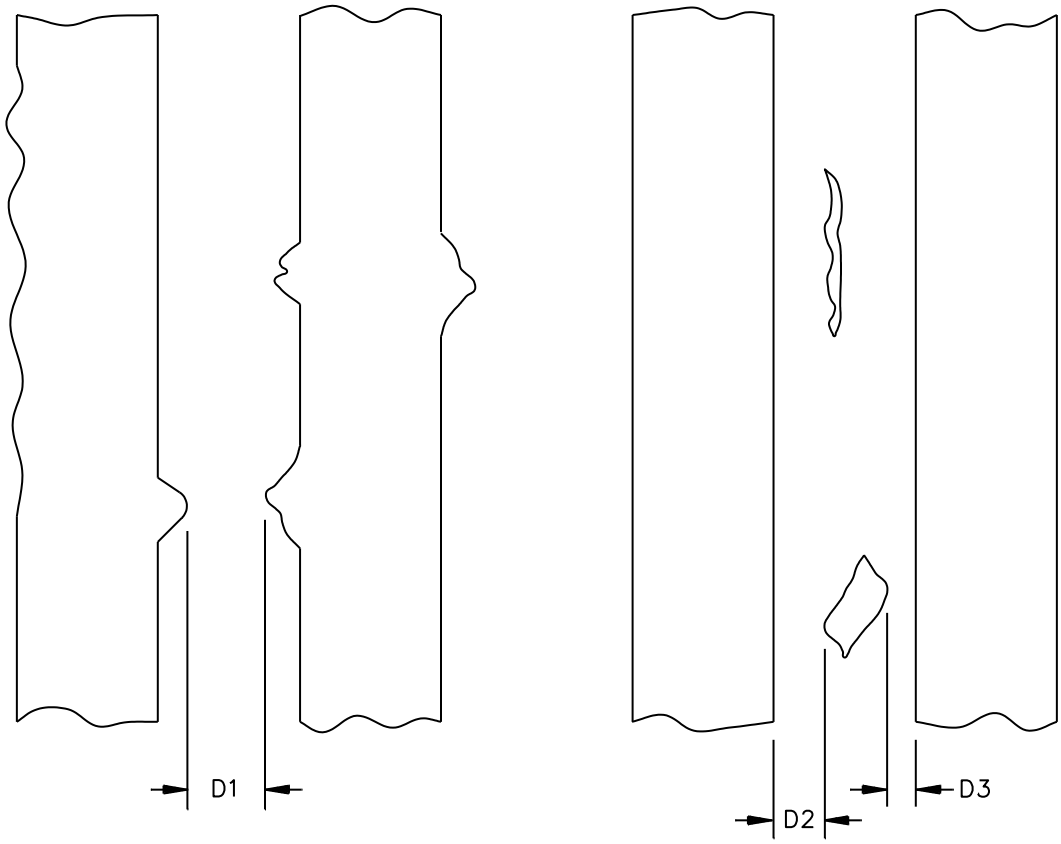


FIGURE F–2. Conductor pattern imperfections.



NOTES:
1. Accept when dimension D1 is greater than or equal to 80 percent of specified spacing.
2. Accept when dimension D2 and D3 together are greater than or equal to 80 percent of specified spacing.

FIGURE F–3. Conductor to conductor spacing measurements.

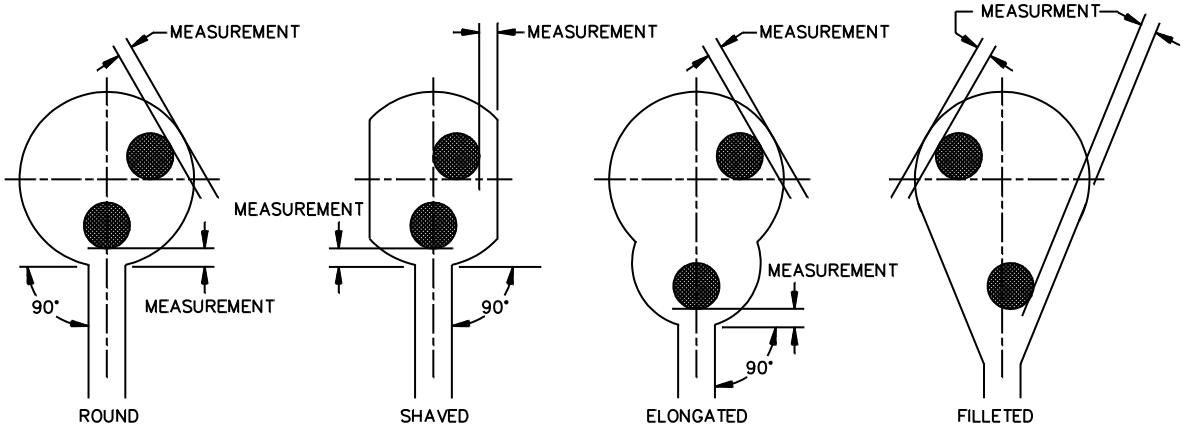
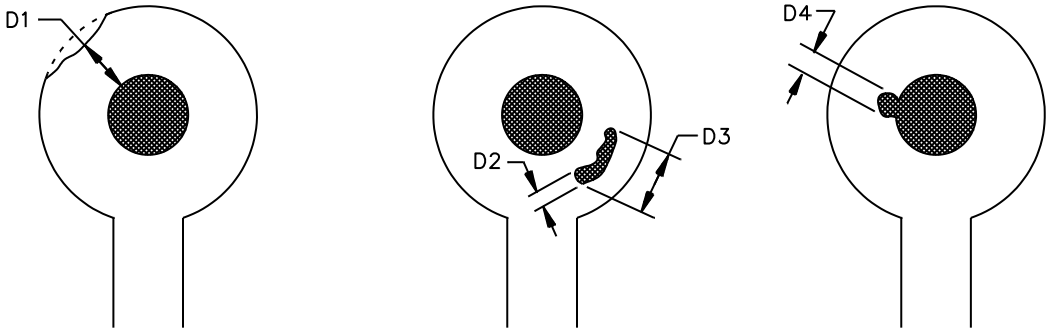


FIGURE F–4. External annular ring measurement.



NOTES:

1. Accept when dimension D1 is greater than or equal to 80 percent of specified external annular ring.
2. Accept when dimension D2 is less than or equal to 20 percent of the specified external annular ring circumference. Accept when dimension D3 is less than or equal to 72 degrees.
3. Accept when dimension D4 is less than 33 percent of the total circumference.

FIGURE F–5. Annular ring imperfections.

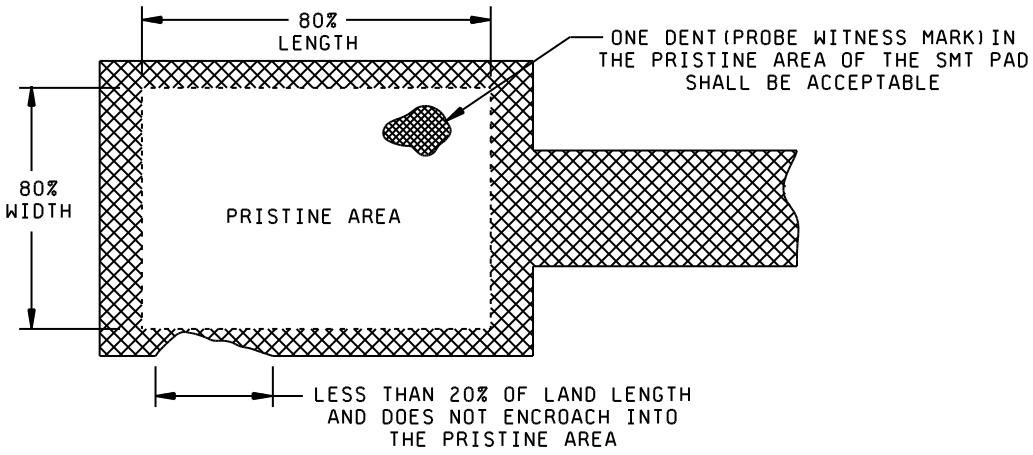


FIGURE F–6. Rectangular surface mount pads.

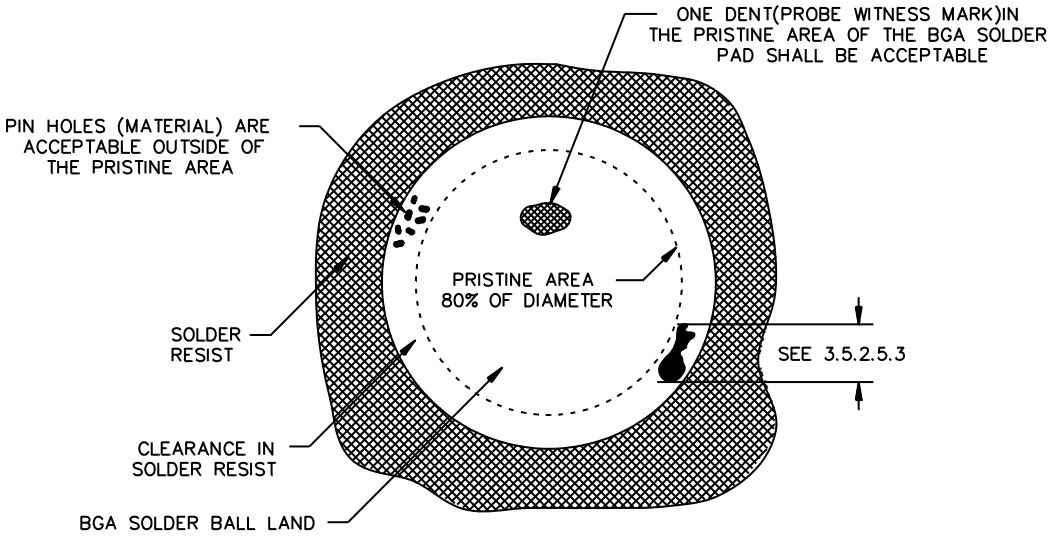


FIGURE F–7. Round surface mount lands (BGA pads).

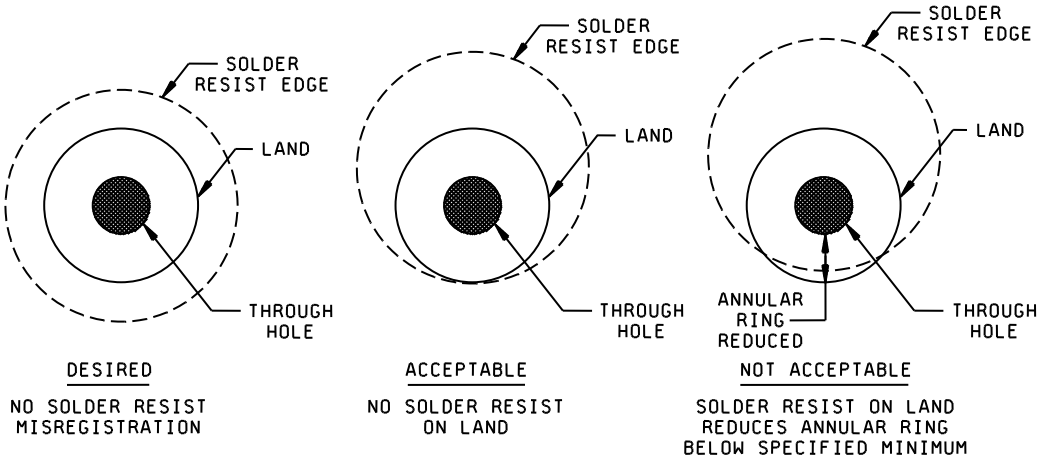


FIGURE F–8. Solder mask registration.

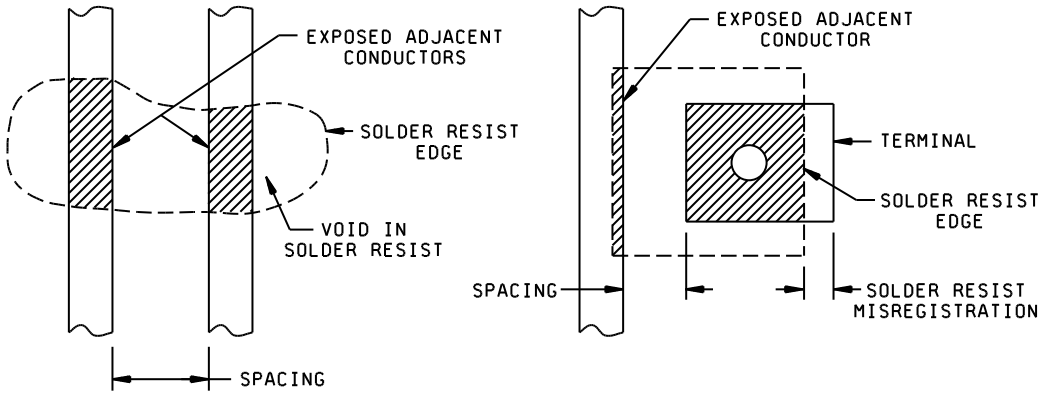


FIGURE F–9. Solder mask deviations.

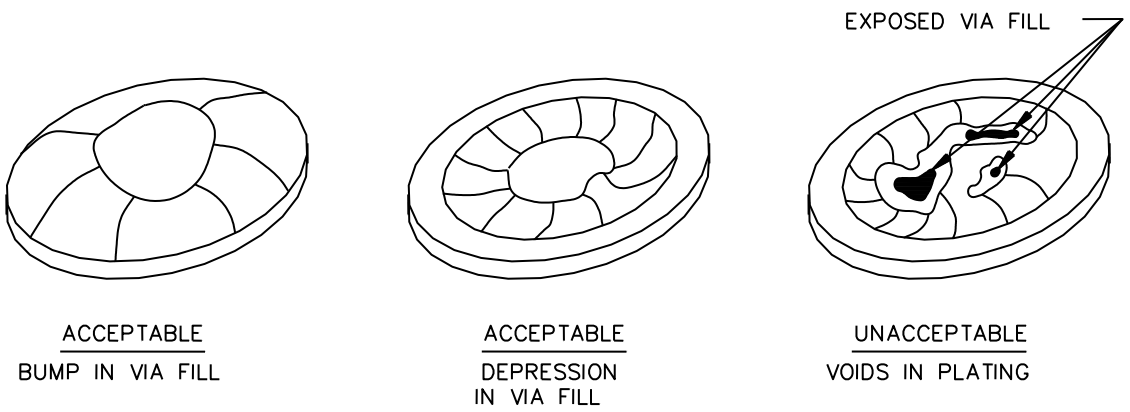


FIGURE F–10. Via copper cap plating deviations.

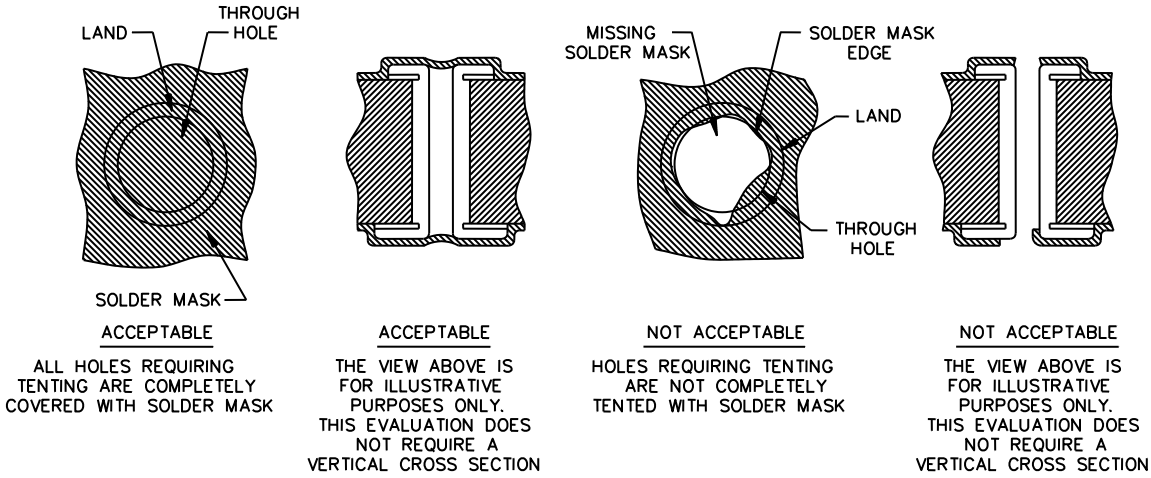


FIGURE F–11. Solder mask tenting deviations.

METALOGRPAHIC ILLUSTRATIONS

G.1 SCOPE

G.1.1 Scope. This appendix establishes uniform criteria for evaluating and classifying characteristics and defects which are observable using metallographic techniques on partially complete or completed printed boards, qualification test specimens, and test coupons. This appendix describes the preferred, acceptable, and nonconforming conditions that are internally observable. It represents the visual interpretation of minimum requirements set forth in appendix A of this specification. The criteria shall apply whether a 100-percent inspection or a sampling plan procedure is used. This appendix is a mandatory part of the specification for manufacturers supplying printed boards to the QPL product assurance level of appendix A. The information contained herein is intended for compliance.

G.2 APPLICABLE DOCUMENTS This section is not applicable to this appendix.

G.2.1 General. The documents listed in this section are specified in sections G.3 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirement documents cited in sections G.3 of this specification, whether or not they are listed.

G.2.2 Non–Government publications. The following documents form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

IPC – ASSOCIATION CONNECTING ELECTRONICS INDUSTRIES (IPC)

IPC–A–600 – Acceptability of Printed Boards.

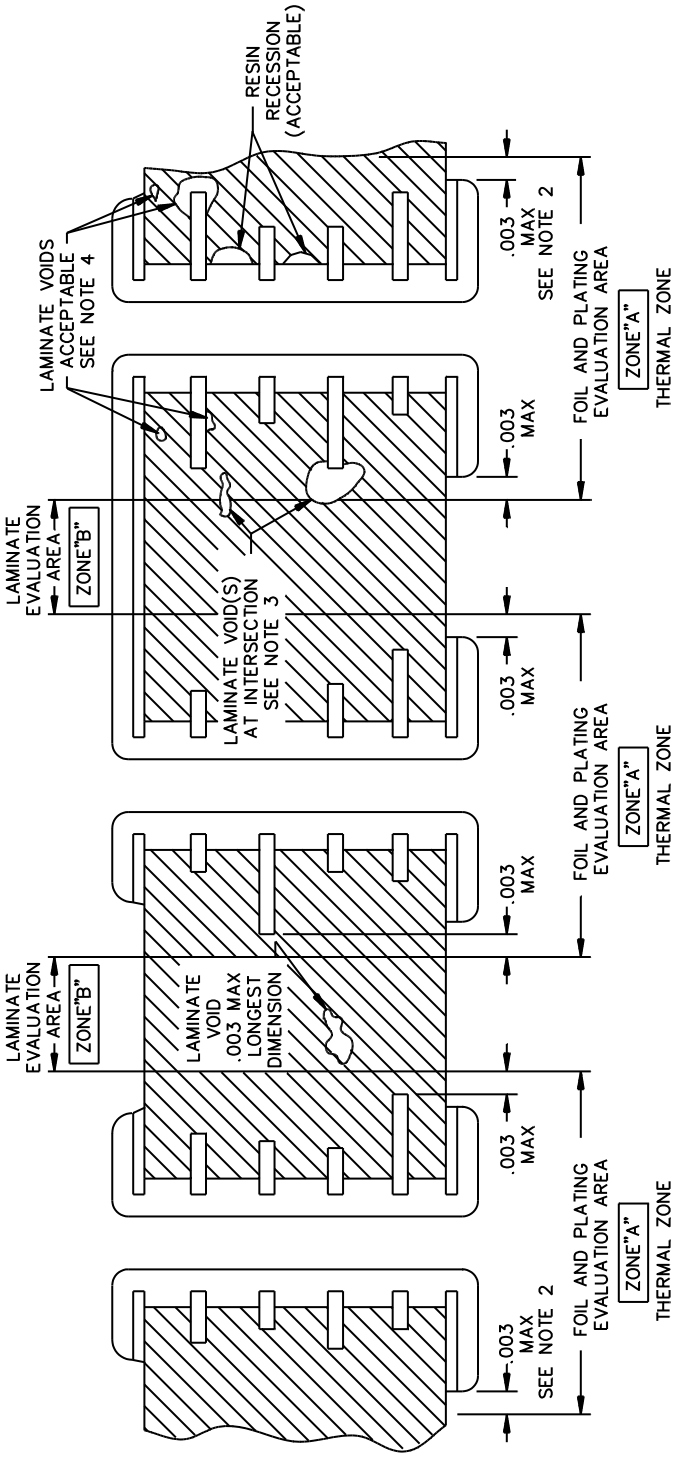
(Copies of these documents are available online at http://www.ipc.org.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

G.2.3 Order of precedence. Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

G.3 INTERNALLY OBSERVABLE CHARACTERISTICS

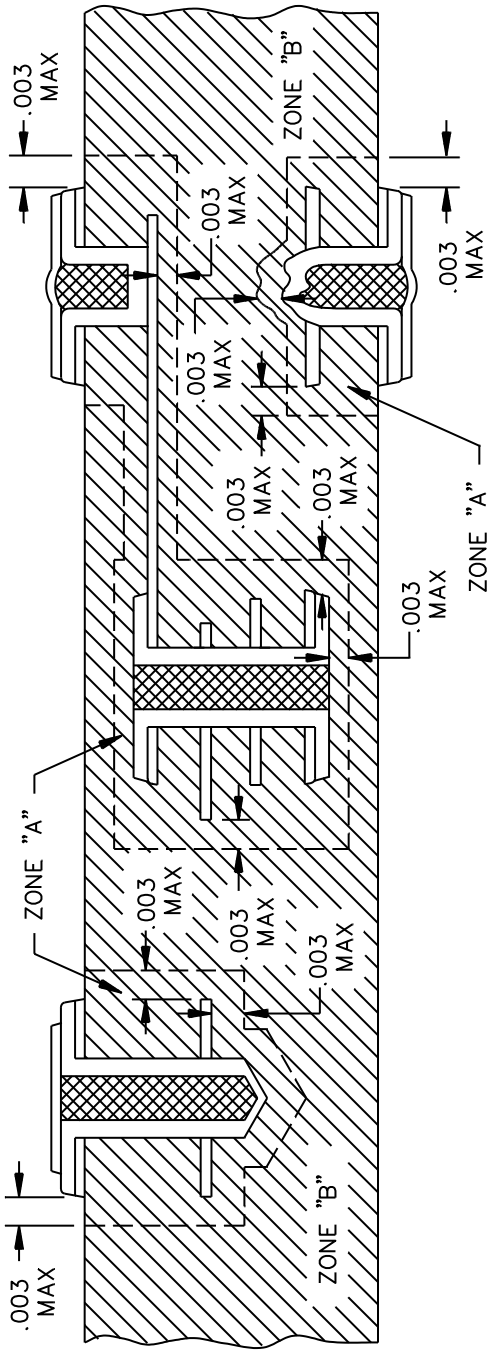
G.3.1 General. This section addresses those characteristics which are observable during metallographic examination. This includes those characteristics that are both internal and on the surface layer of the printed wiring board test specimen (see figures G–1 through G–26 for examples). IPC–A–600 contains figures, illustrations, and photographs that can aid in the visualization of internally observable accept/reject conditions of microsectioned test specimens. If a condition is not addressed herein, or specified on the printed board procurement documentation, it shall comply with the class 3 "acceptable" or "target condition" criteria of IPC–A–600.



NOTES:

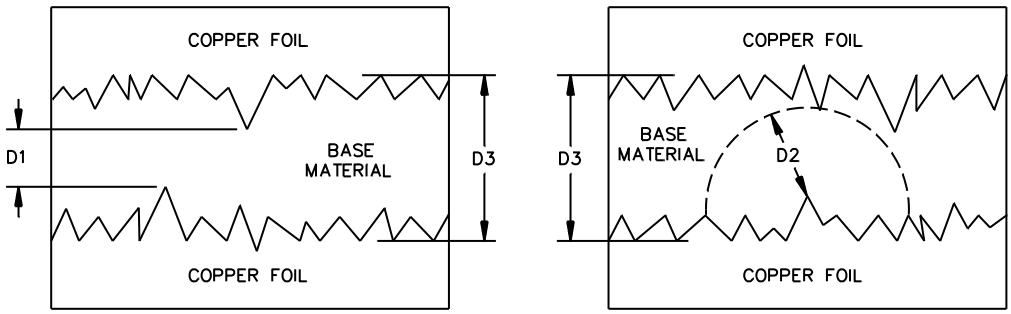
1. Dimensions are in inches. The millimeter equivalent of .003 inch (0.08 mm) is given for general information only.
2. Typically beyond land edge most radially extended.
3. Voids at intersection of zone A and zone B. Laminate voids greater than .003 inch (0.08 mm) that extend into zone B are rejectable.
4. Laminate voids are not evaluated in zone A.
5. Multiple adhesive voids between two adjacent plated-through holes in the same plane shall not have a combined length exceeding .02 inch (0.5 mm).
6. For test specimens which have been subjected to resistance to soldering heat, rework simulation, or thermal shock tests, laminate imperfections are not evaluated in the areas outside of the plated holes (at either end of the microsection specimen).

FIGURE G–1. Thermal zone for plated-through holes (cross section) after stress testing.



NOTES:
1. Dimensions are in inches. The millimeter equivalent of of .003 inch (0.08 mm) is given for general information only.
2. Typically beyond land edge most radially extended.
3. Voids at intersection of zone A and zone B. Laminate voids greater than .003 inch (0.08 mm) that extend into zone B are rejectable.
4. Laminate voids are not evaluated in zone A.

FIGURE G–2. Thermal zone for blind and buried vias cross section after stress testing.



NOTES:
1. Dimension D1 is the minimum distance between parallel lines drawn from any two point on the foil.
2. Dimension D2 is the length of a radius between any point on one copper foil nearest to a point on the opposite copper foil in a 180 degree arc.
3. Dimension D3 is the dielectric thickness typically found when using non-destructive mechanical methods.

FIGURE G–3. Dielectric thickness measurement.

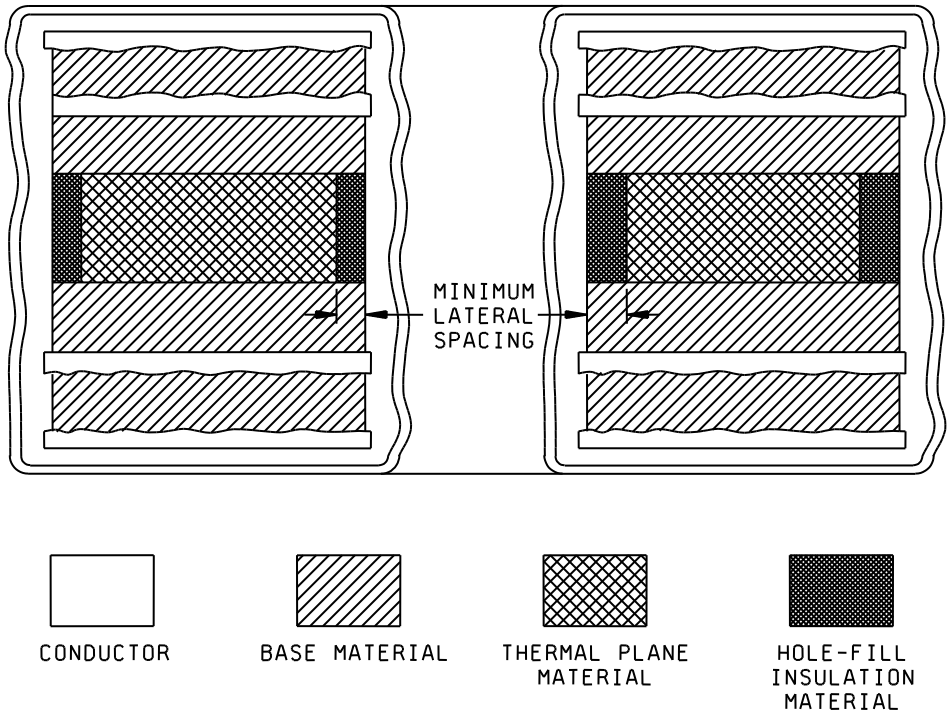


FIGURE G–4. Isolated heat sink plane dielectric spacing.

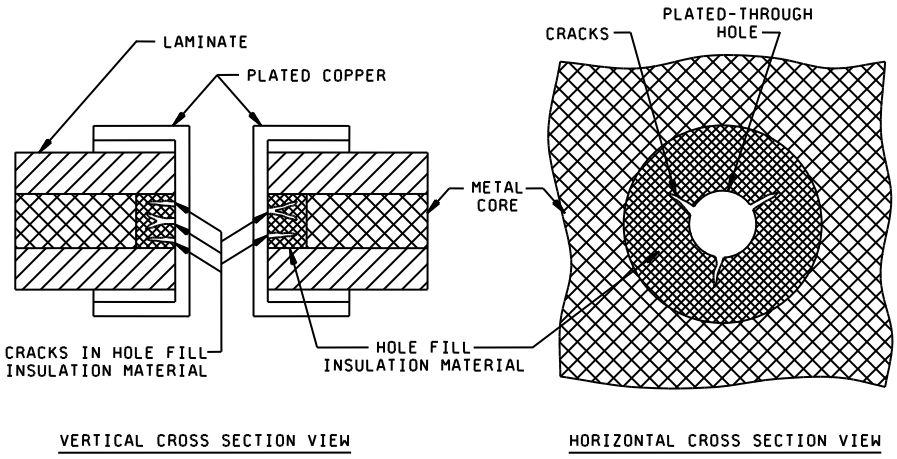


FIGURE G–5. Insulation material cracks, metal cores or heat sink planes.

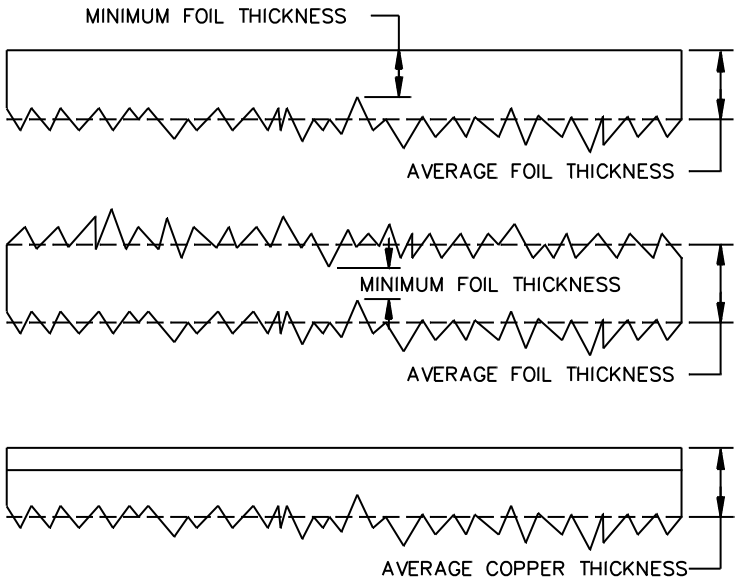


FIGURE G–6. Copper foil and copper foil with plating thickness measurement.

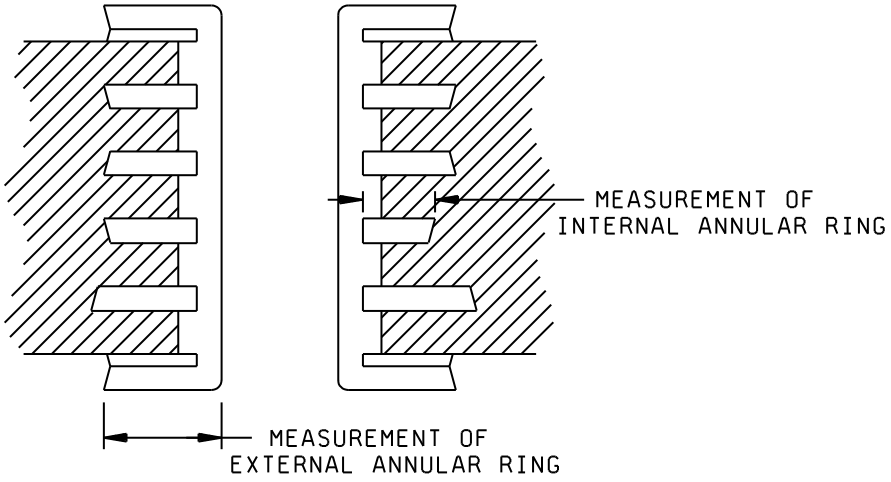


FIGURE G–7. Internal annular ring measurements.

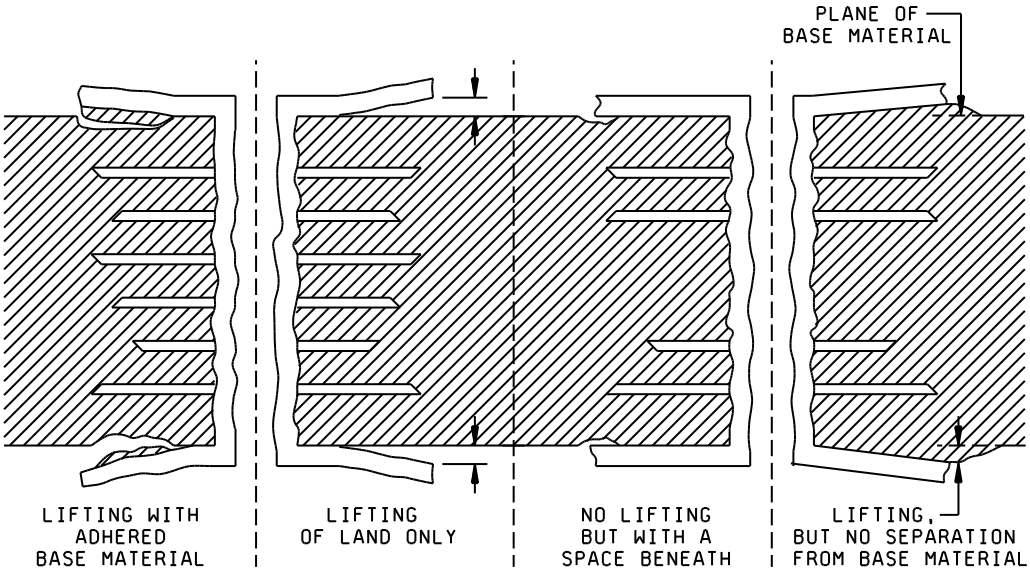
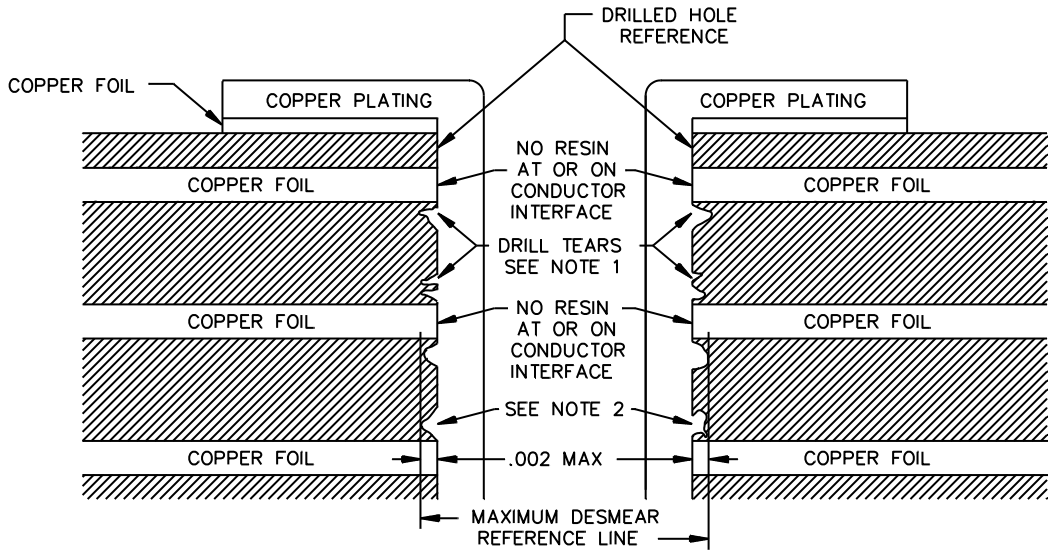


FIGURE G–8. Bonding of conductor to base material and lifted lands.



NOTES:
1. Drill tears are not measured. Drill tear-outs shall be enclosed.
2. The dielectric material removed shall be enclosed.

FIGURE G–9. Smear removal.

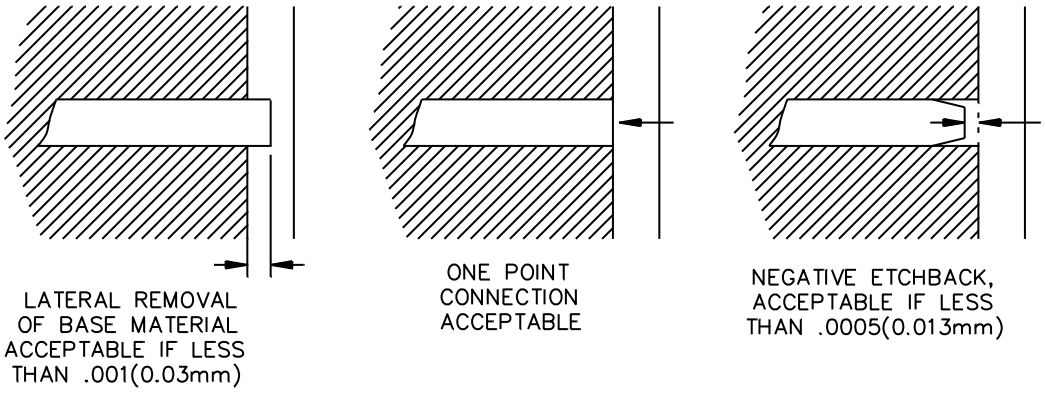


FIGURE G–10. Post–desmear plating connections to internal layers.

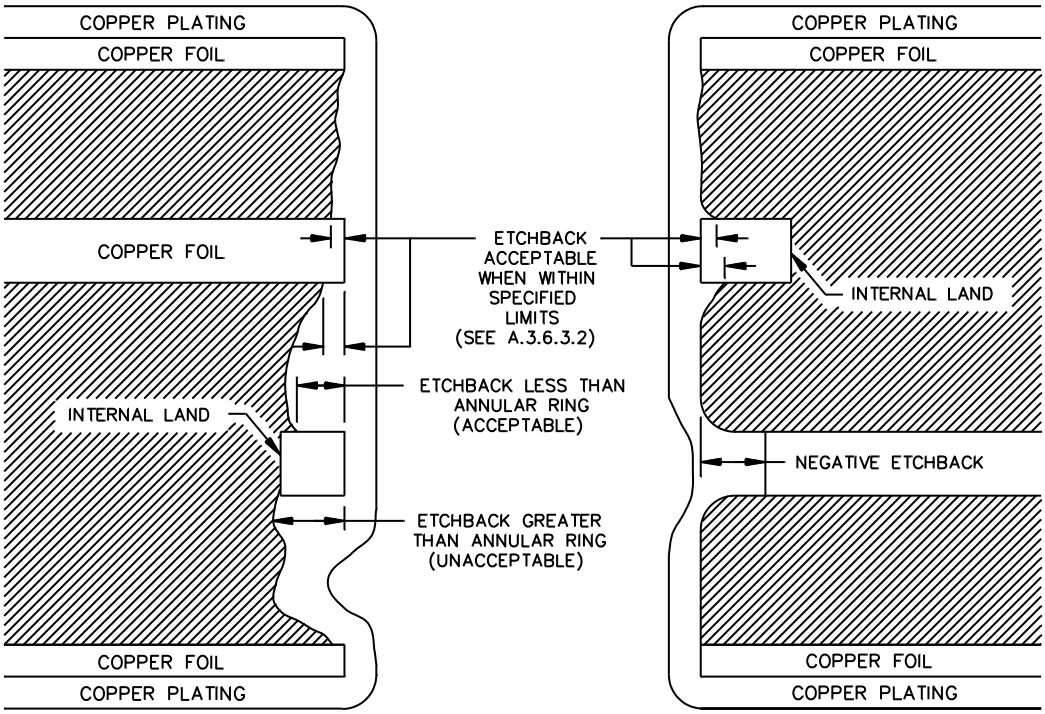


FIGURE G–11. Etchback.

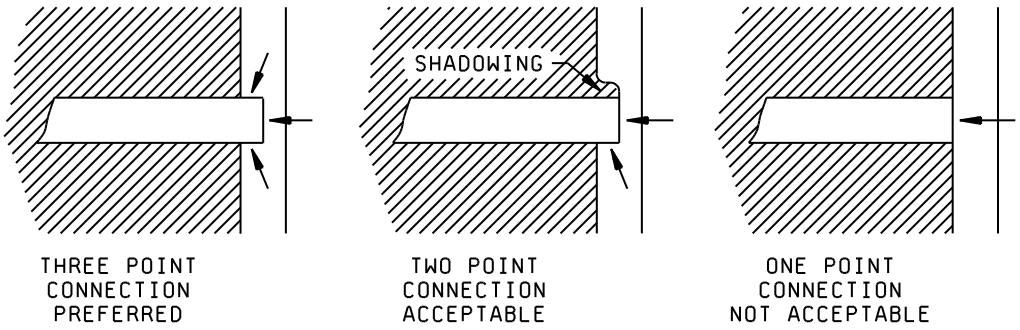


FIGURE G–12. Post–etchback plating connections to internal layers.

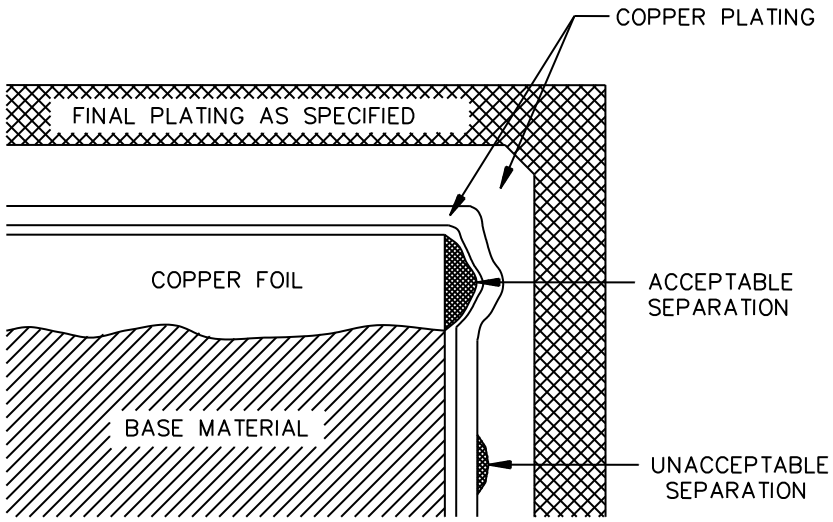


FIGURE G–13. Conductive interface separations.

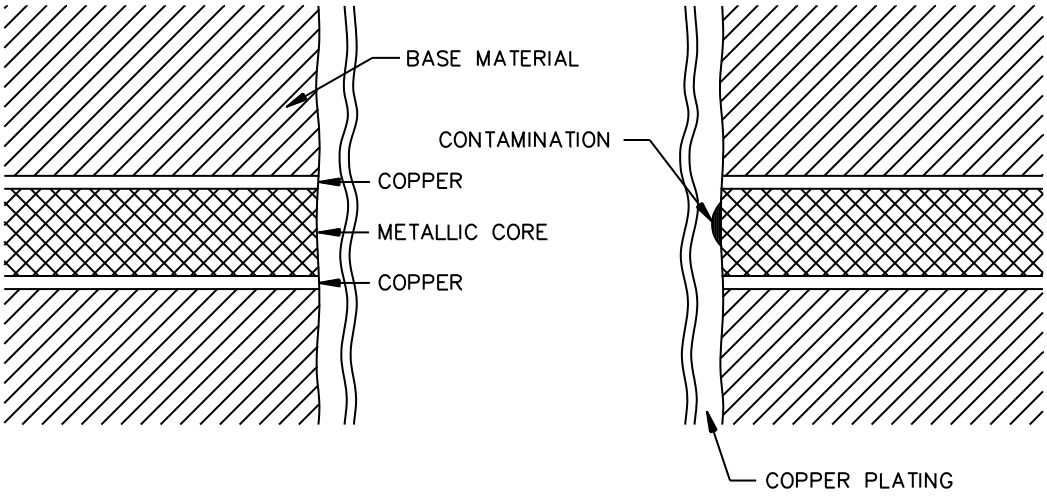


FIGURE G–14. Dissimilar metal interfaces.

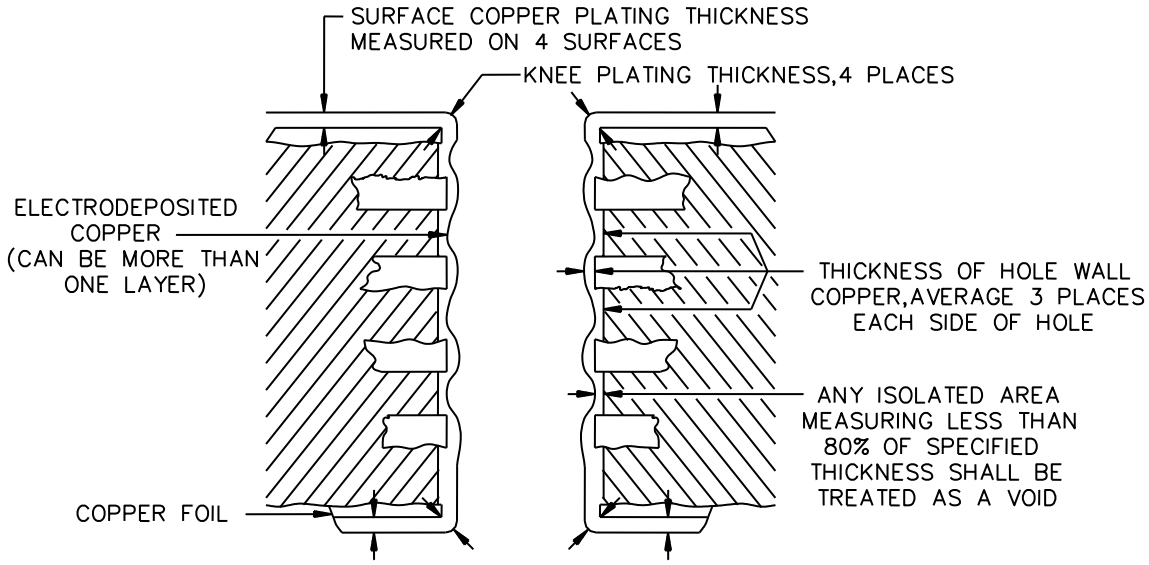


FIGURE G–15. Copper plating thickness.

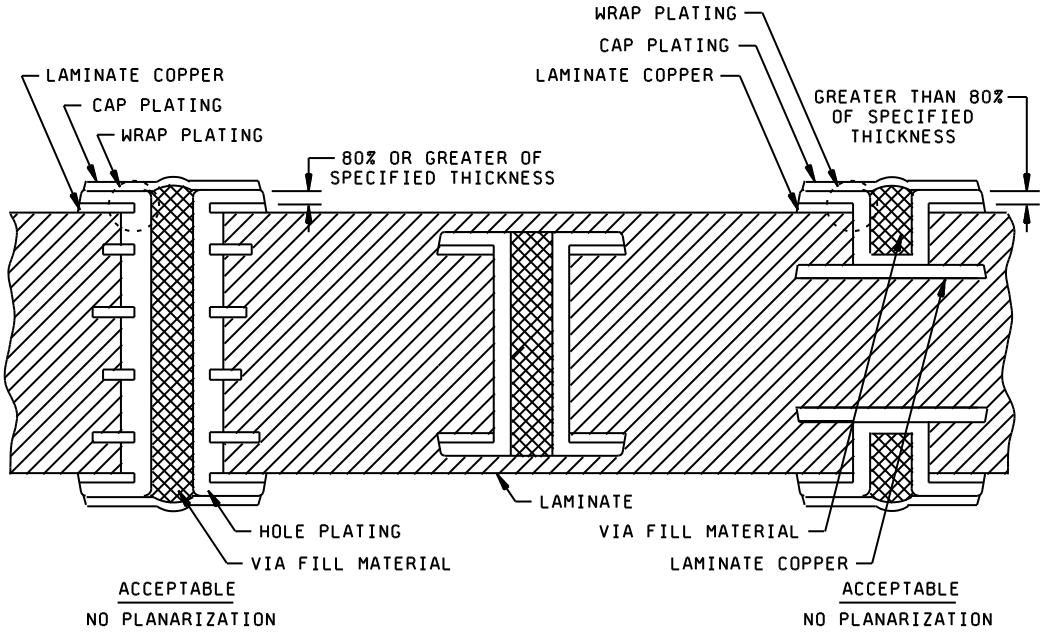


FIGURE G–16. Acceptable, non-planarized plated hole structure wrap copper plating.

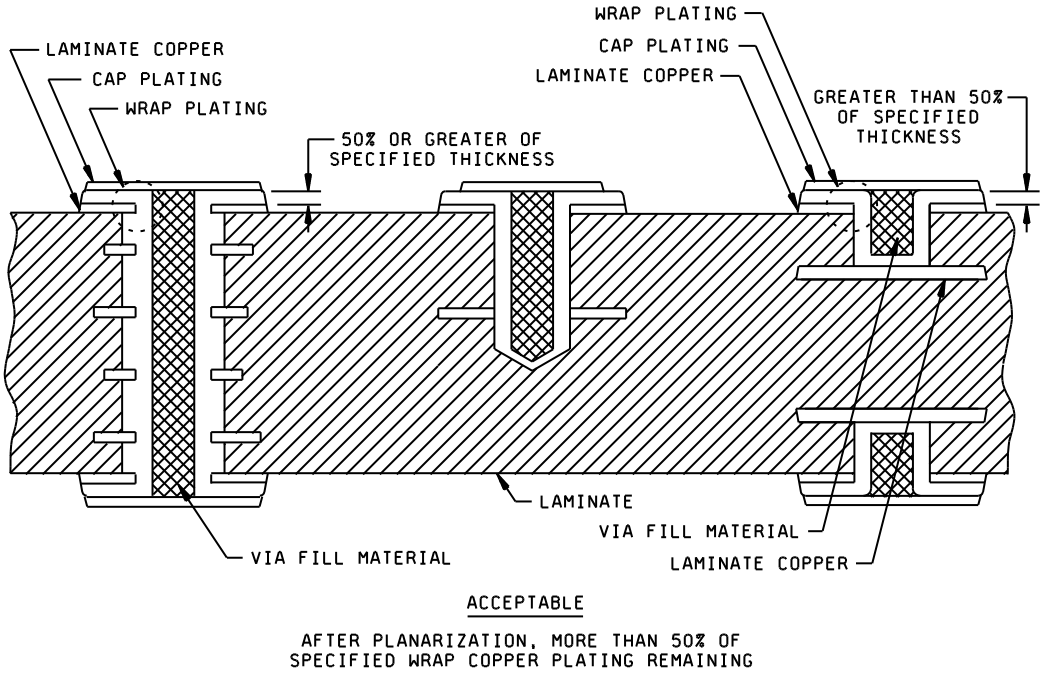


FIGURE G–17. Acceptable planarized plated hole structure wrap copper plating.

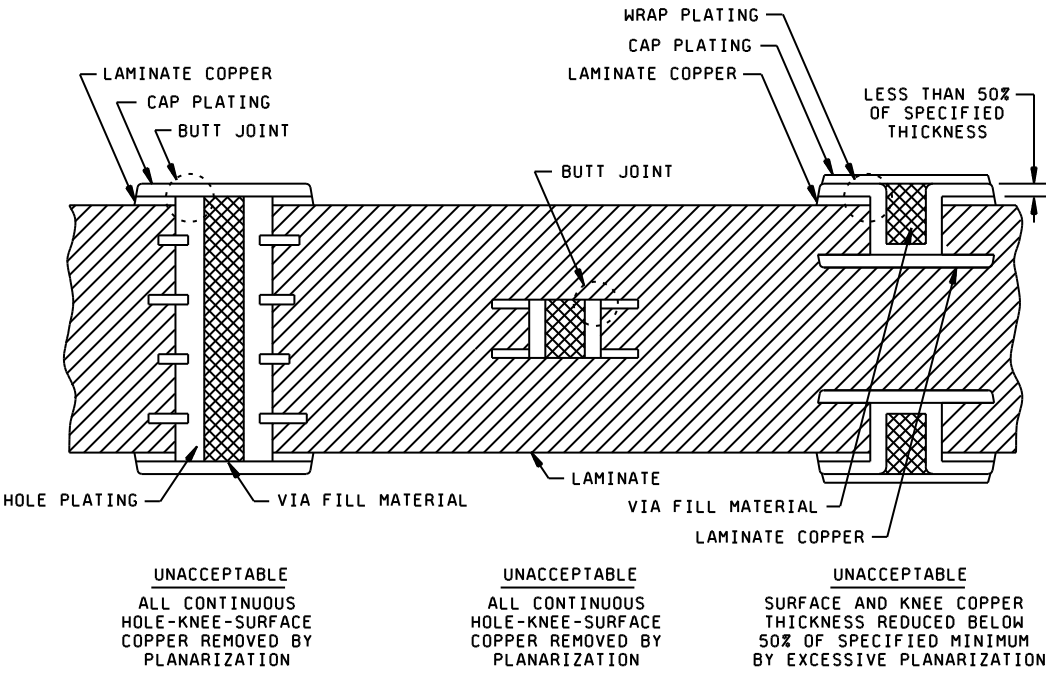


FIGURE G–18. Unacceptable planarized plated hole structure wrap copper plating.

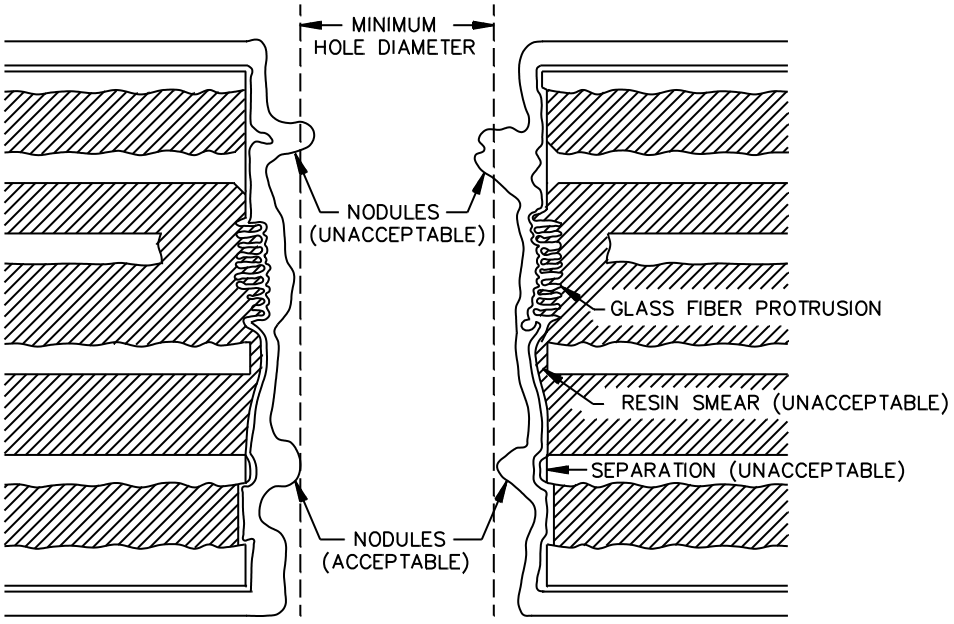
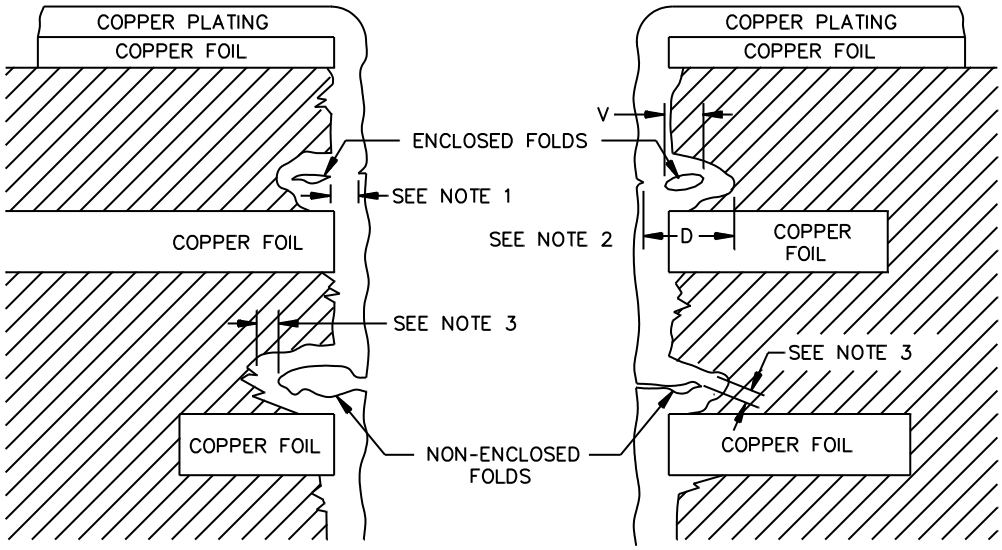


FIGURE G–19. Plated-through hole deficiencies.



NOTES:

1. Minimum copper plating thickness measurement point. Plating folds that are enclosed shall be acceptable if the minimum copper plating thickness is met.
2. Regions with the appearance of plating folds where there is no plating demarcation evident between the void and the inside edge of plating. Measure the distances between lines on inclusion and the overall . The dimension D minus dimension V shall meet the minimum copper plating thickness.
3. Minimum copper plating thickness measurement point. Plating folds that are not enclosed shall be acceptable if the minimum copper plating thickness is met.

FIGURE G–20. Plating fold evaluation.

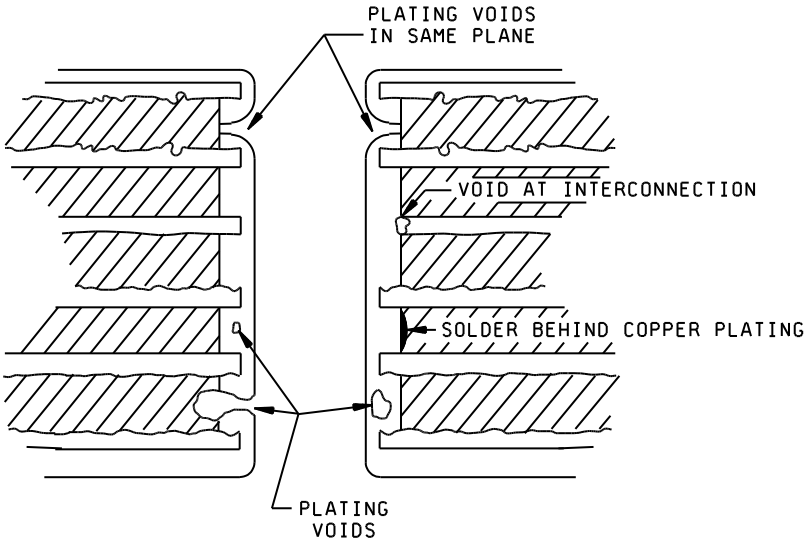


FIGURE G–21. Copper plating voids.

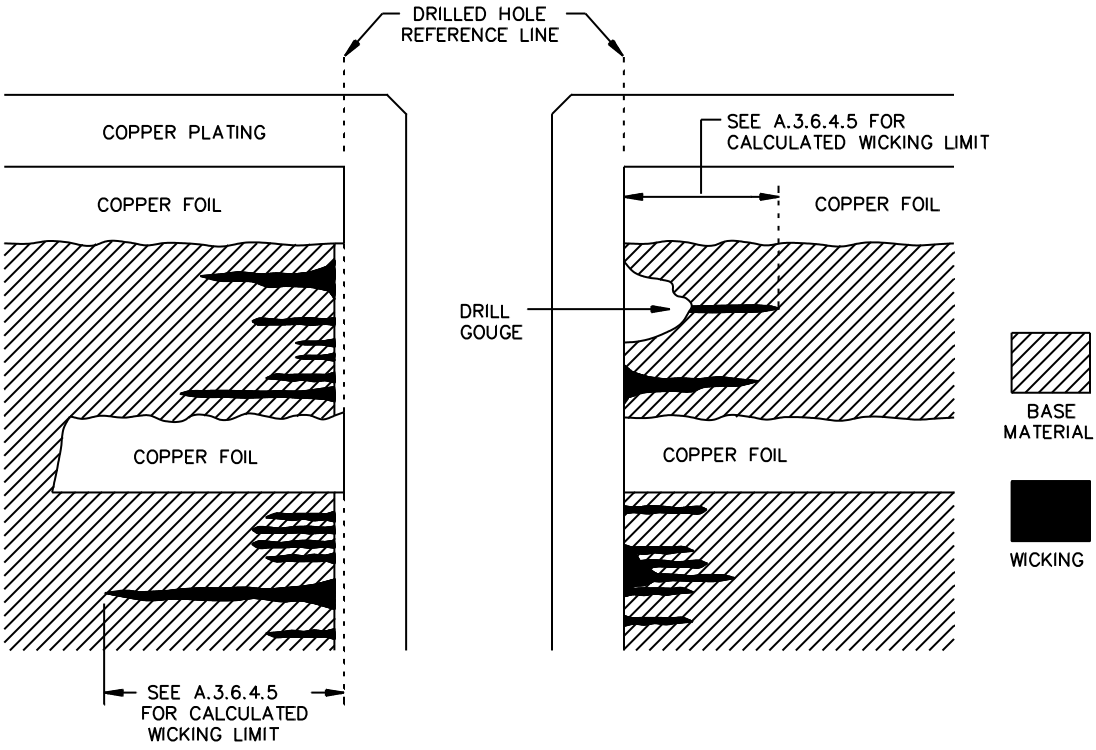


FIGURE G–22. Wicking of copper plating.

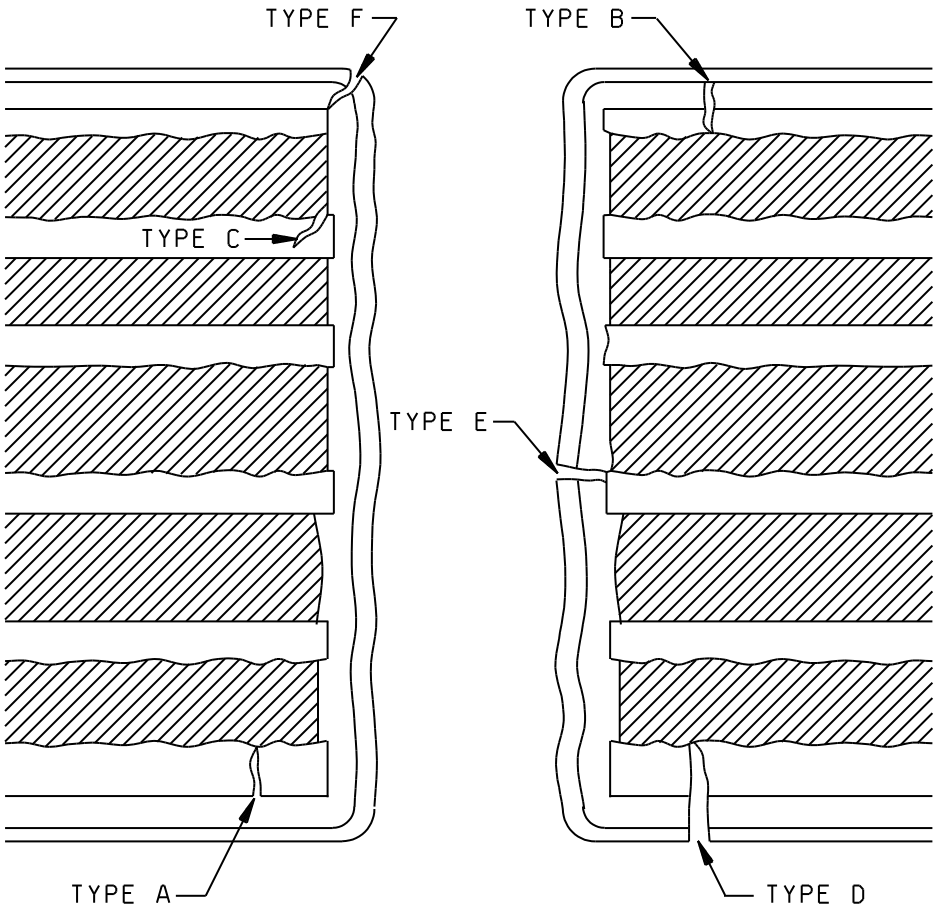


FIGURE G–23. Unacceptable metallic cracks.

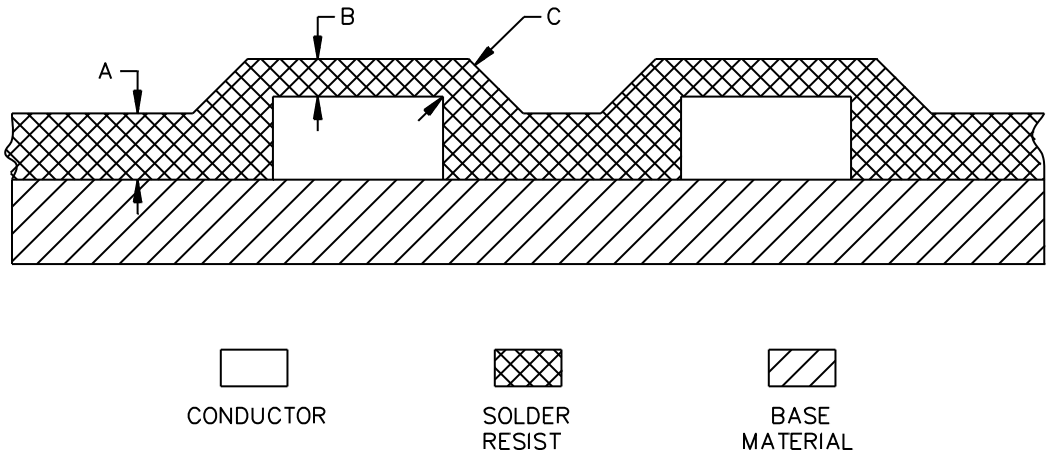


FIGURE G–24. Solder mask thickness.

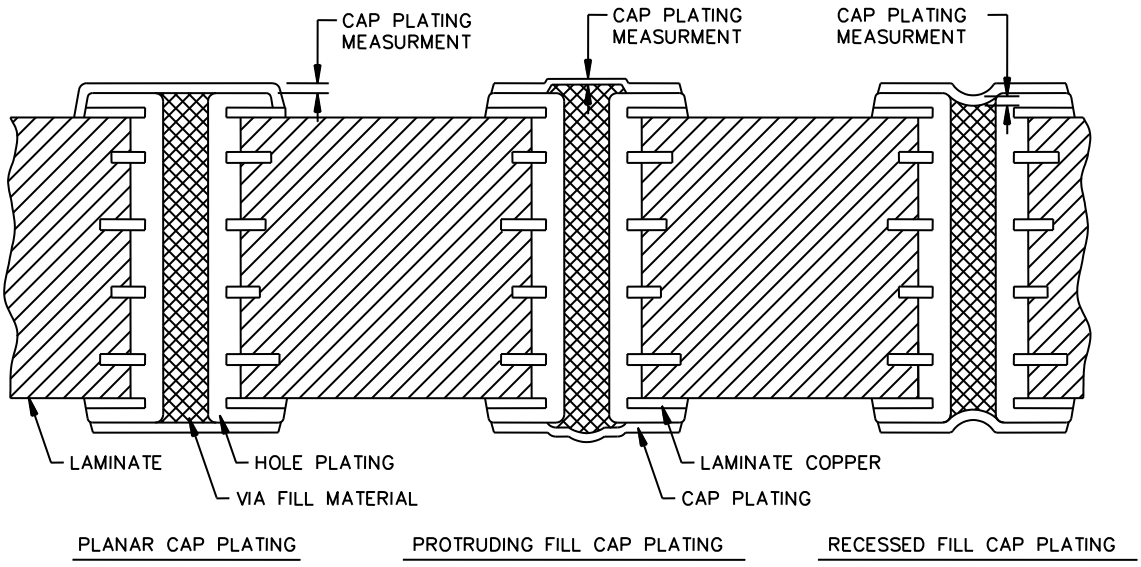


FIGURE G–25. Acceptable via cap plating.

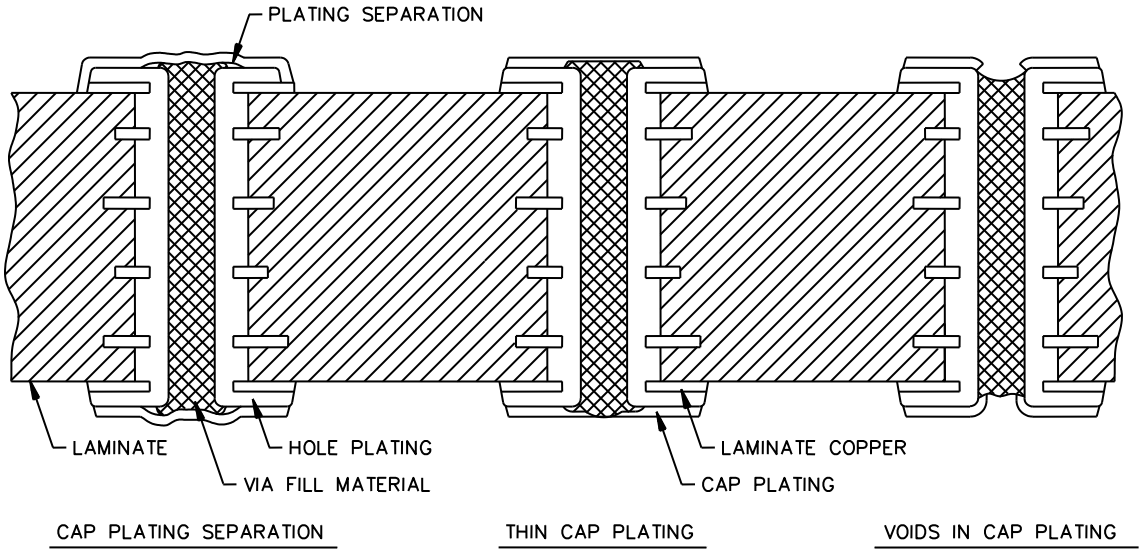


FIGURE G–26. Unacceptable via cap plating.

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QUALITY CONFORMANCE TEST CIRCUITRY

H.1 SCOPE

H.1.1 Scope. This appendix contains requirements, information, and guidance concerning design standard IPC–2221. This appendix is a mandatory part of this specification for manufacturers qualified to the QPL product assurance level of appendix A. The information contained herein is intended for compliance.

H.2 APPLICABLE DOCUMENTS

H.2.1 General. The documents listed in this section are specified in sections H.3 and H.4 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirement documents cited in sections H.3 and H.4 of this specification, whether or not they are listed.

H.2.2 Non–Government publications. The following documents form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

IPC – ASSOCIATION CONNECTING ELECTRONICS INDUSTRIES (IPC)

IPC–2221	–	Generic Standard on Printed Board Design.
IPC–TM–650	–	Test Methods Manual.

(Copies of these documents are available online at http://www.ipc.org.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

H.2.3 Order of precedence. Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

H.3 QUALITY CONFORMANCE TEST CIRCUITRY (QCTC) REQUIREMENTS

H.3.1 General. Test coupons or QCTC strips shall be a part of every inspection panel on which printed wiring boards intended to be compliant to appendix A are fabricated. When test coupon retention is required for traceability it is recommended that an additional set of test coupons be combined into a common QCTC strip. Figure H–1 shows an example of QCTC strip location and placement concepts.

H.3.1.1 Panel location and placement of test coupons. Except for the "A" and "B" test coupons, the printed wiring board manufacturer may position the QCTC strip or individual test coupons to optimize panelization, tooling, and material utilization; however, at least one hole in each test coupon shall be located on the same grid as the printed wiring board features. The location of the "A" and "B" test coupons shall be positioned no further than .5 inch (12.7 mm) of the printed wiring board profile and shall be closer to the panel corner than the QCTC strip identification, as displayed on figure H–1, in order to reflect fabrication and copper plating characteristics.

H.3.1.2 Performance and reliability verification test coupons. The recommended minimum number of test coupons that are required for performing the in-process, groups A, and B verifications of appendix A are specified in table H–I.

H.3.1.3 Process control and acquiring activity required test coupons. Test coupons of custom configuration used for process control or acquiring activity purposes may be added to the production panel. These custom configuration test coupons should incorporate features on the same dimensional plane to ensure compatibility with the required performance verification test coupons specified in table H–I. All applicable custom configuration test coupons shall be defined on the master artwork, the master drawing, or added to the production artwork by the manufacturer.

H.3.2 QCTC strip identification. When test coupons are grouped together in a QCTC strip, the strip shall contain space for QCTC strip identification and traceability marking. Unless otherwise specified, the minimum identification marking shall be as follows:

a. The printed wiring board part identification number (see A.3.8).

b. The manufacturer's Commercial and Government Entity (CAGE) code (see A.3.8.1).

c. The lot date code (see A.3.8.5).

d. The traceability code or identification (see A.3.9).

In addition, any acquiring activity specified special coding systems may be used, provided they are defined on the master drawing.

H.3.3 Using table H–I. The requirements for test coupon quantity and placement on the inspection panel are codified using a 4-digit dash number under the printed wiring board types of table H–I. The last column of table H–I uses a 2-digit code to specify the inspection group the test coupon is typically needed for. The codes for test coupon quantity on an inspection panel are specified in H.3.3.1. The codes for test coupon placement on an inspection panel are specified in H.3.3.2. The codes for test coupon inspection group usage are specified in H.3.3.3. An example of the 4-digit dash number is "1–ML". This dash number designates that a minimum of one test coupon of this type is required on the inspection panel and that its placement is the manufacturer's option.

H.3.3.1 Test coupon quantity codes. The codes used to designate the test coupon quantity in table H–I shall be as follows:

1 – Minimum of one test coupon for this verification on each inspection panel.

2 – Minimum of two test coupons for this verification on each inspection panel.

3 – Minimum of three test coupons for this verification on each inspection panel.

4 – Minimum of four test coupons for this verification on each inspection panel.

– This test coupon is required on the inspection panel only if the performance characteristic represented by the design or construction technique used to fabricate the printed wiring boards is present on the printed wiring boards. The minimum number required needs to be determined by the number of inspection groups needing the test coupon for verification purposes.

TABLE H–I. Test coupons on inspection panels.

Inspections (associated with the identified test coupon)		Test coupon identifier	Type 1	Type 2	Type 3	Type 4	Inspection group
Plating adhesion		C	2–ML	2–ML	2–ML	2–ML	GP and GA
		M	#–ML	#–ML	#–ML	#–ML	GP and GA
Solder mask	Standard	G	2–ML	2–ML	2–ML	2–ML	GP and GA
	Tented vias	T		#–ML	#–ML	#–ML	GP and GA
Non-stressed specimens (microsection) 1/		A	1–ML	1–ML	1–ML	1–ML	GA
Resistance to soldering heat (microsection) 1/		B	2–DC	2–DC	2–DC	$–DC	GA
Non-stressed specimens and resistance to soldering heat 1/		AB–R	2–DC	2–DC	2–DC	$–DC	GA
Solderability	Through hole 2/	A		4–ML	4–ML	4–ML	GA
	Through hole 2/	S		1–ML	1–ML	1–ML	GA
	Surface mount	M	#–BS	#–BS	#–BS	#–BS	GA
Adhesion, legend		3/	1–ML	1–ML	1–ML	1–ML	GA
Resistance to solvents 4/		5/	3–ML	3–ML	3–ML	3–ML	GA or GB
Rework simulation (through hole)		A	1–ML	1–ML	1–ML	1–ML	GB
Insulation resistance 6/		E	2–ML	2–ML	2–ML	2–ML	GB
Surface peel strength 7/		P			2–BS	2–BS	GB
Thermal shock 8/		D	#–ML	#–ML	#–ML	#–ML	GD

1/ Test coupon "AB–R" is an optional test coupon that can be used in lieu of test coupons "A" and "B". See H.4.3.1 for alternate test coupon design.
2/ Either one "S" or four "A" test coupons are needed on the inspection panel for solderability testing. The through–hole solderability test requires that 30 holes be inspected. One "S" coupon has 40 holes and four "A" test coupons will yield a total of 36 holes for the inspection.
3/ See H.4.3.2 for test specimen details.
4/ Test method number 2.3.4 of IPC-TM-650 designates that three solutions shall be used for testing marking. Either one test specimen can be used for each solution (three total specimens needed) or one test specimen can be subjected to all three solutions.
5/ See H.4.3.3 for test specimen details.
6/ See H.4.3.4 for alternate test coupon design.
7/ See H.4.3.5 for test specimen design and details.
8/ Thermal shock testing is only applicable to printed board types 2, 3, and 4.

H.3.3.2 Test coupon placement codes. The codes used to designate the test coupon placement in table H–I shall be as follows:

ML – The location of the test coupon on the inspection panel is the manufacturer's option.

DC – The location of the test coupon on the inspection panel shall be on opposite corners.

BS – The location of the test coupon on the inspection panel is the manufacturer's option. The test coupon shall be place on each external layer (top and bottom) of the inspection panel.

H.3.3.3 Test coupon inspection group usage codes. The code used to designate the inspection group usage of a test coupon in table H–I shall be as follows:

GA – This code designates that the test coupon is used during group A inspection.

GB – This code designates that the test coupon is used during group B inspection.

GD – This code designates that the test coupon is used for process qualification or requalification.

GP – This test coupon is used during in-process inspection.

H.4 TEST COUPONS AND TEST SPECIMENS

H.4.1 General test coupon requirements. Individual test coupons shall be designed to evaluate specific individual characteristics of the printed wiring boards they represent. Variations in specified test coupon design shall meet the intent of the original design and be representative of the printed wiring board. The test coupons shall reflect the design of the printed wiring boards in regards to the plated–through holes, conductor patterns, spacings, and other characteristics that are to be evaluated on the specific test coupon.

H.4.2 Process control test coupons. When test coupons are used to establish process control parameters, they shall consistently use a single hole size or land configuration which reflects the process used. The process characteristics and general printed wiring board characteristics should be matched (for example, threshold technology or leading edge technology) by the test coupons.

H.4.3 Designs and placement. The following test specimen configurations and designs shall be used to verify printed wiring boards to the requirements of appendix A.

H.4.3.1 Alternate test coupon 'AB–R' for the verification of structural integrity of plated holes. Test coupon "AB–R" can be used in lieu of test coupon "A" or "B" specified in IPC–2221.

H.4.3.1.1 Design of alternate test coupon 'AB–R'. The layout of this alternate test coupon is shown on figure H–2.

H.4.3.1.2 Panel placement. The alternate test coupon "AB–R" shall be placed on the inspection panel in place of "A" and "B" test coupons.

H.4.3.1.3 Description of test coupon 'AB–R'. A description and brief explanation of the features available on test coupon "AB–R" is as follows:

a. Holes identified as A. These holes are to represent the largest component hole using a pad less than or equal to .0787 inch (2.0 mm) with its smallest associated drill. The holes have round pads present on all layers.

b. Holes identified as B. These holes are to represent the smallest via using a pad less than or equal to .0394 inch (1.0 mm) with its smallest associated drill. The holes are differentiated into four categories as follows:

(1) B1 has round pads on layers 2 and n-1.

(2) B2 has round pads on signal layers.

(3) B3 has round pads on plane layers.

(4) B4 has square pads on all layers. A line width and spacing check is located in-line with B4 pads based on individual layer features.

c. Holes identified as C. These holes are to represent the smallest via or component hole using a pad less than or equal to .0787 inch (2.0 mm) with its smallest associated drill. These holes have round pads on all layers.

d. Holes identified as Rx. These holes are used to evaluate registration features. The holes are differentiated into four categories as follows:

(1) RA holes are based on holes identified as A design features.

(2) RB holes are based on holes identified as B design features.

(3) RB-1 holes are based on holes identified as B design features minus .0394 inch (1.0 mm).

(4) RC holes are based on holes identified as C design features.

e. Holes identified as T. These holes are tooling holes. The size of the tooling holes are .0787 inch (2.0 mm). These tooling holes have a plane layer anti-pad of .1037 inch (2.635 mm) and solder mask anti-pad of .0866 inch (2.2 mm).

H.4.3.2 Test coupons for the verification of adhesion, legend, and marking (see A.4.8.4.2).

H.4.3.2.1 Design of test specimen for legend and marking adhesion. The test specimens can be either a production printed wiring board, a portion of a production printed wiring board, or a quality conformance test circuitry strip identification areas containing ink or paint marking.

H.4.3.2.2 Panel placement. The placement of the test specimen on the inspection panel shall be where space is available.

H.4.3.3 Test specimens for the verification of resistance to solvents (see A.4.8.3.2).

H.4.3.3.1 Design of test specimens used for resistance to solvents. The printed wiring board test specimens for the resistance to solvents verification can be either portions or whole production printed wiring boards, quality conformance test circuitry strip identification areas containing ink, or paint marking.

H.4.3.3.2 Panel placement. The printed wiring test specimens shall be placed on the inspection panel where space is available.

H.4.3.4 Alternate test coupon 'E' for the verification of moisture and insulation resistance (see A.4.8.6.1). An alternate design of test coupon "E" can be used to evaluate the moisture and insulation resistance of laminated base materials.

H.4.3.4.1 Design of alternate test coupon 'E'. The design of alternate test coupon "E" is shown on figure H–3. This test coupon can be used in lieu of the test coupon "E" specified in IPC–2221.

H.4.3.4.2 Panel placement. At least two alternate test coupons "E" shall be placed on the inspection panel where space is available.

H.4.3.5 Test coupon 'P' for the verification of conductor surface peel strength (see A.4.8.4.8). This printed wiring test specimen is used to evaluate the peel strength of metallic foils as the result of the foil lamination fabrication process.

H.4.3.5.1 Design of test coupon 'P' for verification of conductor surface peel strength. The design of test coupon "P" is shown on figure H–4. The test coupon shall consist of a conductor that provides a minimum test length of 2 inches (50.8 mm) and a minimum conductor width of .125 inch (3.18 mm).

H.4.3.5.2 Panel placement. At least one test coupon "P" for each foil laminated side of the printed wiring board shall be placed on the inspection panel where space is available.

H.4.3.6 Alternate test coupon for the verification of registration (see A.3.7.2.3.2 and A.4.8.2.4.2).

H.4.3.6.1 Design of alternate registration test coupon. There are at least two test coupon designs for evaluating registration using non-destructive methods. The designs are as follows:

a. Test coupon "F" (etch factor not needed) as specified in IPC–2221.

b. Test coupon "R" (etch factor of each layer needed) as specified in IPC–2221.

If other registration test coupon designs and requirements are provided as an element of the design documentation set, registration can be evaluated in accordance with the criteria specified on the applicable master drawing.

H.4.3.6.2 Panel placement. When using non-destructive registration in lieu of destructive evaluation of registration, at least one non-destructive registration test coupons shall be placed on the inspection panel where space is available.

H.5 NOTES

H.5.1 Discussion. Test coupons used for verification inspections and testing, when required, shall be in accordance with this appendix. Quality assurance provisions often require the use of specific test procedures or evaluations to determine if a particular design of a printed wiring board meets the requirements of the design activity and the specification. Some of the verification inspections are performed visually and are non-destructive, while others are only capable through destructive testing and destructive evaluations. Some quality evaluations are performed on test coupons because the test is destructive or the nature of the test requires a specific structure or configuration which may not exist on the printed wiring board.

Test coupons are used in these types of inspections as representatives of the printed wiring boards fabricated on the same panel. In many cases, a test coupon is a suitable printed wiring board test specimen for physical destructive analysis, or testing, since it has been subjected to the same manufacturing processes as the printed wiring boards on the panel. However, the design of the test coupons and their location on a panel are critical in order to ensure that the test coupons are truly representative of the printed wiring boards they represent. A production printed wiring board may be used for destructive tests. Tests requiring specific conductor pattern configuration (for example, insulation resistance) may also be performed on production printed wiring boards if appropriate conductor patterns are included in the design of the printed wiring board.

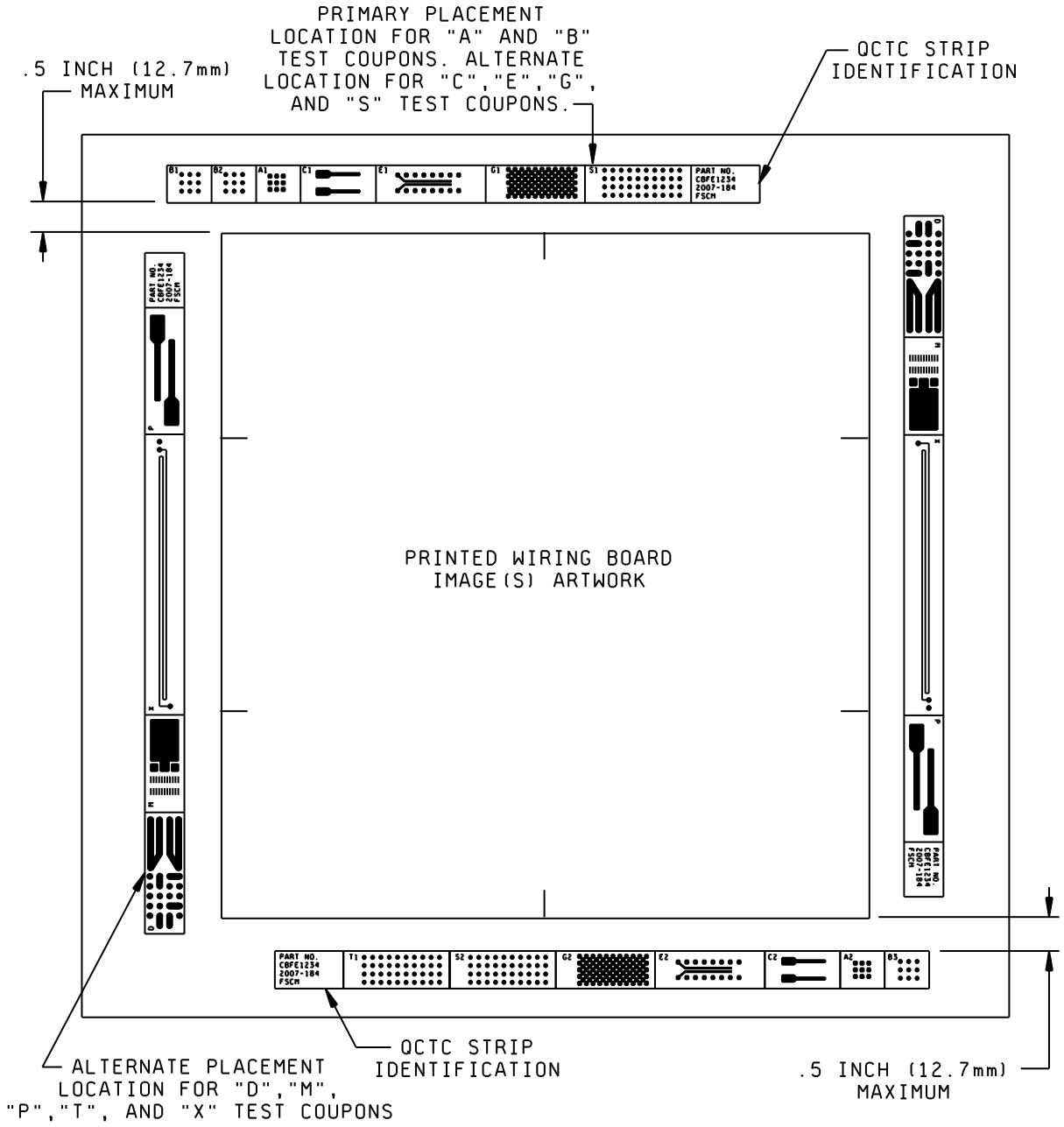
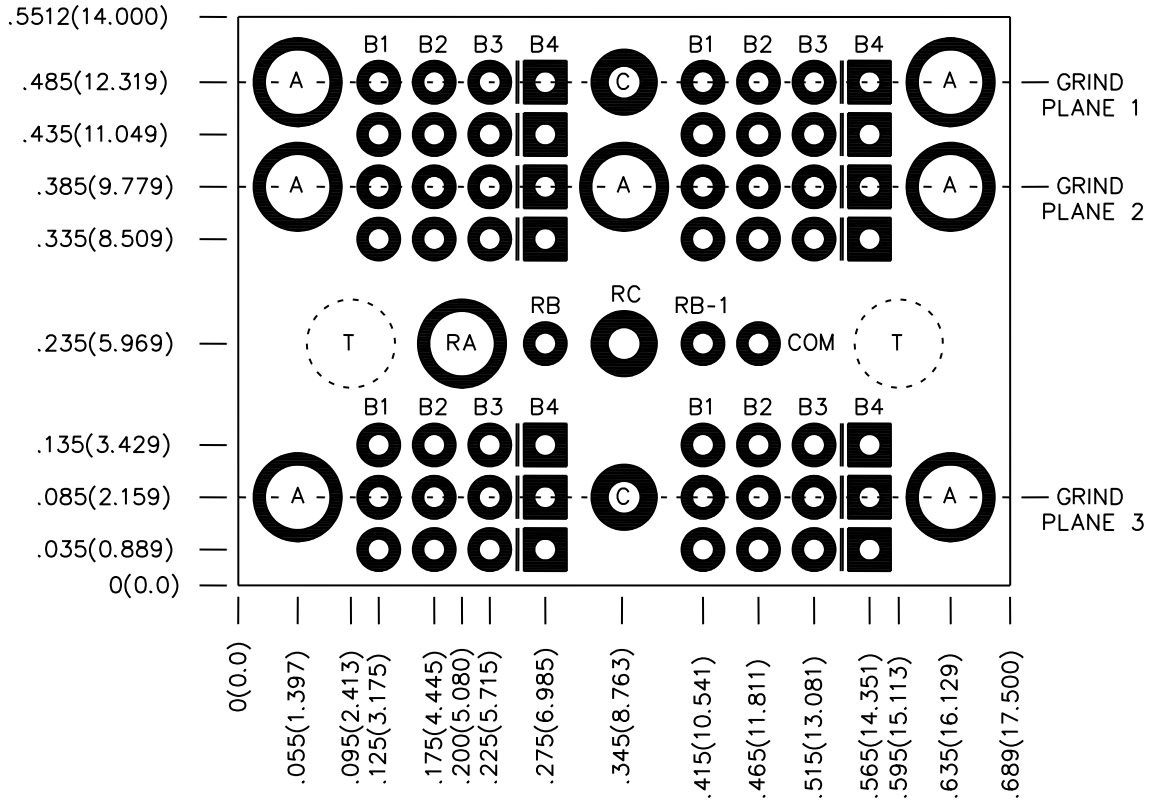


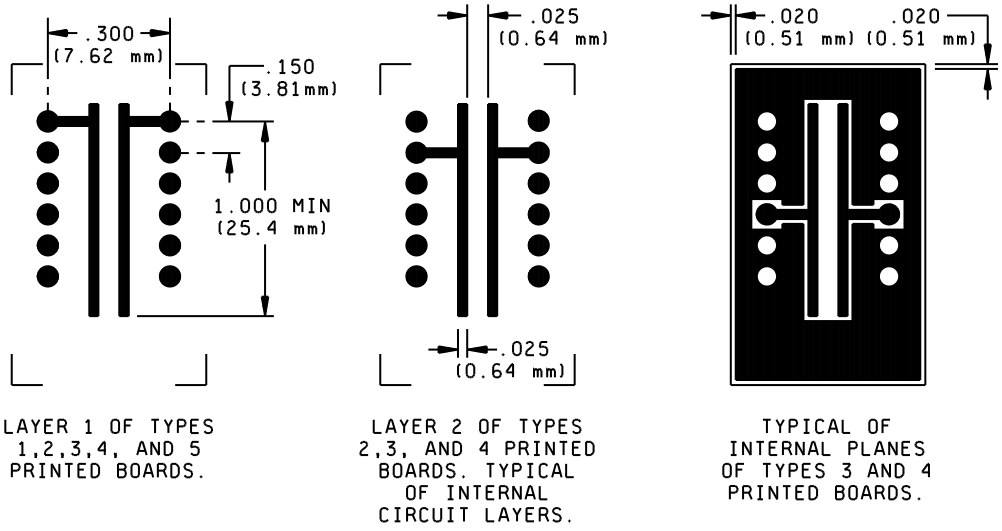
FIGURE H–1. Panel location of quality control test circuitry.



NOTES:

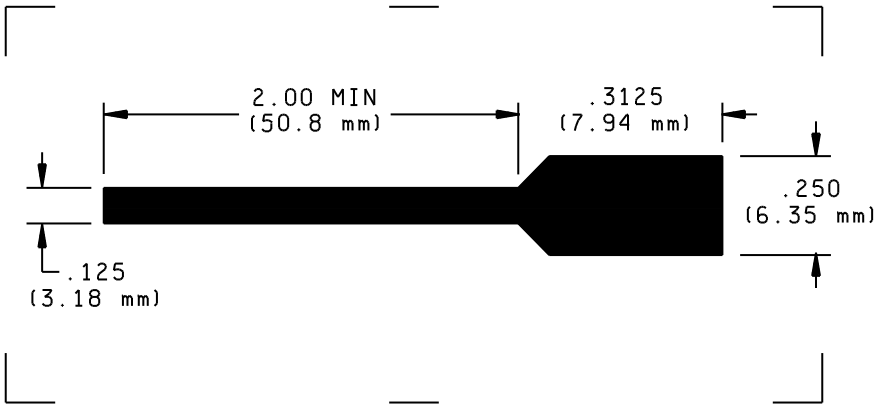
1. Dimensions are in inches. Millimeters are given for general information only.
2. Holes identified as A are used to evaluate the largest component holes of the printed board design.
3. Holes identified as Bn are used to evaluate the smallest via holes of the printed board design.
4. Holes identified as C are used to evaluate the smallest component holes of the printed board design.
5. Holes identified as RA, RB, and RC are used for evaluating registration.
6. Holes identified as T are tooling holes.

FIGURE H–2. Test coupon 'AB–R'.



NOTES:
1. Dimensions are in inches. Millimeters are given for information only.
2. Unless otherwise specified, tolerances are for ±.02 inch (0.51 mm) for two place decimals and ±.010 inch (0.25 mm) for three place decimals.

FIGURE H–3. Alternate design for test coupon 'E'.



NOTES:
1. Dimensions are in inches. Millimeters are given for information only.
2. Unless otherwise specified, tolerances are for ±.02 inch (0.51 mm) for two place decimals and ±.010 inch (0.25 mm) for three place decimals.

FIGURE H–4. Test coupon 'P'.

Custodians:
Army – CR
Navy – EC
Air Force – 85
DLA – CC

Preparing activity:
DLA – CC

(Project 5998–2017–017)

Review activities:
Army – AR, MI
Navy – AS, CG, MC, OS, SH
Air Force – 16, 19, 99
NSA – NS

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