The documentation and process conversion measures necessary to comply with this revision shall be completed by 30 June 2006.

INCH-POUND

MIL–PRF–55110G
11 December 2005
SUPERSEDING
MIL–PRF–55110F
31 May 1997
(See 6.4)

PERFORMANCE SPECIFICATION

PRINTED WIRING BOARD, RIGID, GENERAL SPECIFICATION FOR

Inactive for new design after 31 December 1997.
For new design use MIL–PRF–31032.

Comments, suggestions or questions on this document should be addressed to: Defense Supply Center, Columbus, ATTN: DSCC–VAC, P.O. Box 3990, Columbus, OH 43218–3990 or e–mailed to 5998.Documents@dscc.dla.mil. Since contact information can change, you may want to verify the currency of address information using the ASSIST Online database at Universal Resource Locator (URL) http://assist.daps.dla.mil.

CONTENTS

PARAGRAPH PAGE

CONTENTS

PARAGRAPH PAGE

CONTENTS

PARAGRAPH PAGE

CONTENTS

PARAGRAPH PAGE

CONTENTS

PARAGRAPH PAGE

CONTENTS

PARAGRAPH PAGE

CONTENTS

PARAGRAPH PAGE

CONTENTS

CONTENTS

PARAGRAPH PAGE

CONTENTS

PARAGRAPH PAGE

TABLES

FIGURES

This specification is approved for use by all Departments and Agencies of the Department of Defense.

1. SCOPE

1.1 Scope. This specification establishes the performance and qualification requirements for rigid single–sided, double–sided, and multilayered printed wiring boards with or without plated through holes (see 6.1). Verification is accomplished through the use of one of two methods of product assurance (QPL or QPL/QML). Detail requirements, specific characteristics, and other provisions which are sensitive to the particular intended use are specified in the applicable master drawing.

1.2 Classification. Printed wiring boards are classified by 1.2.1 and 1.2.2.

1.2.1 Type. Printed wiring boards are of the types described herein, as specified (see 3.1).

Type 1 – Singled-sided printed wiring board (see 6.5.3.1).
Type 2 – Double–sided printed wiring board (see 6.5.3.2) with or without plated-through holes.
Type 3 – Multilayer printed wiring board with plated holes (see 6.5.3.3).

1.2.2 Base material. The printed wiring board base material type should be identified by the applicable base material specification sheet or by the legacy base material type designator as required by the master drawing (see 3.1.1).

1.3 Description of this specification. The main body contains general provisions and is supplemented by detailed appendices. Appendices A and B describe the two product assurance programs that can be implemented by the manufacturer. Appendix A contains the traditional Qualified Products List (QPL) product assurance program. Appendix B is an optional quality management approach using a technical review board concept along with a Qualified Manufacturer List (QML) product assurance program addressed in MIL–PRF–31032, to modify the generic verification criteria provided in this specification. Appendix C provides statistical sampling, and basic test and inspection procedures. Appendix D is optional and can be used when producing printed wiring boards designed to superseded design standards (see 6.5.2). Appendix D may also be used as a guide in developing a test plan for legacy or existing designs based on the tests and inspections of appendix A. Appendix E is optional and describes an alternative procedure used to evaluate oxidation levels on solderable surfaces. The procedure involves using electrochemical reduction techniques to determine the type and quantity of oxide on plated-through holes.

2. APPLICABLE DOCUMENTS

2.1 General. The documents listed in this section are specified in sections 3, 4, or 5 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3, 4, or 5 of this specification, whether or not they are listed.

2.2 Non-Government publications. The following documents form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

IPC – ASSOCIATION CONNECTING ELECTRONICS INDUSTRIES (IPC)

IPC–T–50 – Terms and Definitions for Interconnecting and Packaging Electronic Circuits.

(Application for copies should be addressed to the IPC – Association Connecting Electronics Industry, 3000 Lakeside Drive, Suite 309 S, Bannockburn, IL 60015–1249 or at URL http://www.ipc.org.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

2.3 Order of precedence. In the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 General requirements. The manufacturer of printed wiring boards, in compliance with this specification, shall have and use production facilities, verification facilities, and product assurance procedures adequate to assure successful compliance with the provisions of this specification and the associated master drawing. Adequacy of a printed board manufacturer to meet the requirements of this specification shall be determined by the Government qualifying activity (Defense Supply Center, Columbus, code DSCC–VQE). Only printed wiring boards which are verified and meet all the applicable performance requirements contained herein and the design, construction, and material requirement of the associated master drawing shall be certified as compliant and delivered.

3.1.1 Master drawing. Printed wiring boards delivered under this specification shall be of the material, design, and construction specified on the applicable master drawing.

3.1.2 Conflicting requirements. In the event of conflict between the requirements of this specification and other requirements of the applicable master drawing, the precedence in which documents shall govern, in descending order, is as follows:

a. The applicable master drawing (see 3.1.1). Additional acquisition requirements (see 6.2) may be provided in the order or contract. Any deletion of any of the performance requirements or performance verifications of this specification not approved by the qualifying activity, will result in the printed wiring board being deemed noncompliant with this specification.

b. This specification.

c. The applicable design standard (see 3.1.1, A.3.3 as applicable).

d. Specifications, standards, and other documents referenced in section 2.

3.1.3 Terms and definitions. The definitions for all terms used herein shall be as specified in IPC-T-50 and those contained herein (see 6.5, and appendices A, B, C, D, and E).

3.2 Qualification. Printed wiring boards furnished under this specification shall be products that are authorized by the qualifying activity for listing on the applicable QPL before contract award (see 4.3 and 6.3). In addition, the manufacturer shall certify for QPL or receive certification from the qualifying activity for QPL/QML that the product assurance requirements of 3.3 have been met and are being maintained.

3.2.1 QPL. The qualification requirements for the QPL product assurance level shall be in accordance with appendix A.

3.2.2 QPL/QML. The qualification requirements for the QPL/QML product assurance level shall be in accordance with appendix B.

3.3 Product assurance requirements. This specification contains two different methods of product assurance for printed wiring board compliance. The two levels of printed wiring product assurance are QPL (see 3.3.1) and QPL/QML (see 3.3.2).

3.3.1 QPL product assurance. Product assurance procedures (see A.4.5.5.2) shall be made available to the qualifying activity in order for the manufacturer to be listed on QPL–55110. The product assurance procedures shall, as a minimum, consist of the items outlined in A.4.5.5.2. The manufacturer shall ensure the product assurance procedures reflect the actual product assurance practices of the manufacturing location. The qualifying activity shall be notified within 14 days of any changes to these procedures. The product assurance procedures shall also be available upon request of the qualifying activity.

3.3.2 QPL/QML product assurance. A product assurance program for QPL/QML printed wiring board furnished under this specification shall satisfy the requirements of appendix B.

3.4 Letters of interpretation and policy. Letters of interpretation and policy applicable to this specification shall be approved in writing by the preparing activity or qualifying activity. All letters of interpretation and policy applicable to MIL–PRF–55110 written prior to the current date of this specification are not applicable to this revision. All subsequent letters of interpretation and policy letters are valid only until the next document change action (amendment or revision).

3.5 Recycled, recovered, or environmentally preferable materials. Recycled, recovered, or environmentally preferable materials should be used to the maximum extent possible provided that the material meets or exceeds the operational and maintenance requirements, and promotes economically advantageous life cycle costs.

3.6 Certification of conformance. Unless otherwise specified by the contract or order (see 6.2), a certificate of conformance for compliant printed boards shall be forwarded to the acquiring activity (see 6.5.1). When a certificate of conformance for compliant printed boards is supplied, it shall include the following information, as a minimum:

a. Manufacturer’s name and address.

b. Customer’s name and address.

c. Manufacturer’s CAGE (Commercial and Government Entity) code.

d. Printed board description, including classification (type and base material), specification number with revision and amendment level, master drawing or other identification number, and the applicable design standard.

e. Lot date code.

f. Quantity of printed boards in shipment from manufacturer.

g. Statement certifying printed board conformance to this specification, the master drawing, and the contract or order.

h. The date of transaction.

i. The name of the company official approving the certificate of conformance. The manufacturer shall have a method for authenticating the approval of certificates of conformance for printed boards compliant to this specification.

3.7 Qualifying activity on-site audit. Manufacturers listed on QPL–55110 will be required to undergo periodic on-site audits of their facilities by the qualifying activity. The manufacturer shall demonstrate to the qualifying activity that controls have been implemented to assure compliance to the requirements of this specification. The qualifying activity reserves the right to perform on-site audits of any other facilities, such as contracted services, that the manufacturer uses for producing printed boards to this specification.

3.8 Workmanship. Printed wiring boards shall be processed in such a manner as to be uniform in quality and shall be free from defects that exceed those allowed in this specification that could affect life or serviceability.

4. VERIFICATION

4.1 Classification of inspections. The inspection requirements specified herein are classified as follows:

a. Qualification inspection (see 4.3, A.4.5, or B.4.1).

b. Inspection of product for delivery (see A.4.6 or B.4.3.a).

c. Periodic conformance inspection (see A.4.7 or B.4.3.b).

4.2 Printed wiring board performance verification.

4.2.1 QPL. Printed wiring board performance verification inspection shall consist of inspections on the production printed wiring boards and the quality conformance test circuitry or test coupons referenced in appendix A.

4.2.2 QPL/QML. The minimum requirements for printed wiring board performance verification to the QPL/QML product assurance level shall satisfy the guidelines of appendix B.

4.3 Qualification inspection. Qualification is possible by two different methods based on the product assurance level used, QPL (see 4.3.1) or QPL/QML (see 4.3.2).

4.3.1 QPL. Qualification inspection for the QPL product assurance level shall be performed at a laboratory acceptable to the Government (hereafter referred to as a "certified suitable laboratory", see C.5) on qualification test specimens produced with material, equipment, and procedures that will be used in subsequent production (see 6.3). The requirements concerning the qualification test specimens, number of specimens to be tested, and the test routines they shall be subjected to, and the extent of qualification shall be as specified in appendix A.

4.3.2 QPL/QML. The minimum requirements for qualification to the QPL/QML product assurance level shall be as specified in appendix B.

5. PACKAGING

5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of materiel is to be performed by DoD or in house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain requisite packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activities within the Military Service or Defense Agency, or within the Military Service’s system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory.)

6.1 Intended use. Rigid printed wiring boards covered by this specification are intended for use in ground support, airborne, and shipboard electronic equipment to eliminate high density hand wiring and where compact packaging is desirable.

6.2 Acquisition requirements. Acquisition documents should specify the following:

a. Title, number, revision letter (with any amendment number when applicable), and date of this specification.

b. Packaging requirements (see 5.1).

c. Appropriate type (see 1.2.1) and base material type (see 1.2.2).

d. Title, number, revision letter (with any engineering change proposal or notice of revision number when applicable), and date of the applicable master drawing (see 3.1.1).

e. Requirements for certificate of conformance, if other than 3.6.

f. The printed wiring board performance verification level desired (QPL or QPL/QML). If no level is specified, QPL printed wiring board performance verification will be used.

6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Products List (QPL) No. 55110 whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from Defense Supply Center Columbus, ATTN: DSCC–VQE, P.O. Box 3990, Columbus, Ohio 43218–3990 or by email 5998_Qualifications@dscc.dla.mil or at URL http://www.dscc.dla.mil/programs/qmlqpl. Application procedures should conform to the guidelines of SD–6, "Provisions Governing Qualification" (see 6.3.3).

6.3.1 Transference of qualification. Manufacturers currently qualified to MIL-PRF-55110F will have their qualification transferred to this specification. The expiration date of their current qualification will not be changed. Qualifications in process (before the date of this specification) will be performed to the requirements MIL-PRF-55110F with amendment 1. New applications for qualification (after the date of this specification) will be performed to the requirements of this revision.

6.3.2 Retention of qualification. Printed wiring boards verified and certified to MIL-P-55110D, MIL-P-55110E, MIL-PRF-55110E, or MIL-PRF-55110F (with any amendment) or to any product assurance level contained herein will retain qualification to this specification.

6.3.2.1 Discussion. MIL-P-55110C certification program was not governed by the policies and procedures of the Defense Standardization Program as defined by DoD 4120.3-M and therefore does not exist within the QPL program of MIL-P-55110D and beyond. For additional information concerning this issue, see MIL-P-55110C, paragraph 60.1.

6.3.3 "Provisions Governing Qualification". Copies of SD–6, "Provisions Governing Qualification", may be upon application to Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094 or obtained online at URL http://assist.daps.mil/quicksearch or http://assist.daps.dla.mil/.

6.4 Supersession.

6.4.1 Design, construction, and verification. Design, construction, and verification supersession information is included in appendix D of this specification.

6.4.2 Reference to superseded design standards. This specification contains requirements and guidelines for the testing of printed wiring boards that were designed to and or make use of test coupons conforming to IPC-2221. See appendix D for additional guidance regarding the verification of printed boards using different design standards.

6.4.3 References on master drawings. All the requirements of this specification can be interchangeable with those specifications identified as MIL-P-55110. Therefore, existing master drawings or OEM documents referencing MIL-P-55110 need not be revised, updated, or changed to make reference to MIL-PRF-55110 in order for this specification to be used.

6.4.4 Reference to superseded specifications. Superseded specifications are listed below.

a. MIL-P-55110 including:
   (1) MIL-P-55110C, dated 26 April 1978.
      (a) MIL-P-55110C with Amendment 1, dated 18 July 1978.
      (b) MIL-P-55110C with Amendment 2, dated 27 August 1979.
      (c) MIL-P-55110C with Amendment 3, dated 16 October 1980.
      (d) MIL-P-55110C with Amendment 4, dated 28 June 1982.
      (e) MIL-P-55110C with Amendment 5, dated 28 March 1984.
   (2) MIL-P-55110D, dated 31 December 1984.
      (a) MIL-P-55110D with Amendment 1, dated 6 March 1987.
      (b) MIL-P-55110D with Interim Amendment 2 (USAF), dated 22 April 1988.
      (c) MIL-P-55110D with Amendment 3, dated 18 May 1989.
      (d) MIL-P-55110D with Amendment 4, dated 2 December 1990.
   (3) MIL-P-55110E, dated 22 December 1993.
   (4) MIL-PRF-55110E, dated 29 September 1995.
   (5) MIL-PRF-55110F, dated 31 May 1997.
      (a) MIL-PRF-55110F with Amendment 1, dated 27 November 1998.

b. MIL-P-55640 including:
   (1) MIL-P-55640(EL), dated 6 February 1969.
   (2) MIL-P-55640A, dated 29 October 1970.
      (a) MIL-P-55640A with Amendment 1, dated 14 October 1971.
      (b) MIL-P-55640A with Amendment 2, dated 4 April 1975.

c. MIL-P-82585(OS), dated 24 February 1970.

6.5 Definitions.

6.5.1 Acquiring activity. The organizational element of the Government which contracts for articles, supplies, or services may authorize a contractor or subcontractor to be its agent. When this organizational element of the Government has given specific written authorization to a contractor or subcontractor to serve as agent, the agent will not have the authority to grant waivers, deviations, or exceptions to this specification unless specific written authorization to do so has also been given by the Government organization, which is the preparing activity or qualifying activity. In the absence of a specific acquiring activity, the acquiring activity will be an organization within the supplier's company that is independent of the group responsible for device design, process development, or screening, or may be an independent organization outside the supplier's company.

6.5.2 Design standard. A document that establishes the baseline parameters (default values), standard practices and guidelines for the design of printed wiring boards. Within this specification, the term "design standard" is used to describe those documents that contain the design, construction, material, test coupon requirements, and guidelines used to produce panels of rigid printed wiring boards.

6.5.3 Printed wiring board types. The printed wiring board types should be as specified herein.

6.5.3.1 Type 1. Type 1 rigid printed wiring boards have only one conductive layer (single–sided conductor pattern) with cover lay and no plating in the component holes.

6.5.3.2 Type 2. Type 2 rigid printed wiring boards are printed wiring boards with conductor patterns on both sides of the printed board (double–sided). In addition, the design of the printed wiring board may require plated-through holes in order to connect the conductor patterns on both sides together.

6.5.3.3 Type 3. Type 3 rigid printed wiring boards are multi–layered (with 3 or more conductor layers) with plated holes. Type 3 designs include those with metal core and blind or buried via holes.

6.5.4 Product assurance. The method of complying with the two different levels of this specification using either the QPL method that has been integral to this specification since revision MIL-P-55110D or the newer method, QPL/QML which was introduced in revision MIL-PRF-55110F.

6.5.4.1 QML. A list of manufacturers, by name and plant address, who have met the certification and qualification requirements stated in MIL-PRF-31032. A QML focuses on qualifying an envelope of materials and processes rather than individual products or designs. That envelope is qualified by carefully selecting representative worst case test vehicles or representative samples from production that contain all potential combinations of materials and processes that may be subsequently used during production. A QML is normally appropriate for items of supply that have very rapid technological advancement or a myriad of variations or custom designs that make individual product qualifications impractical or excessively expensive.

6.5.4.2 QPL. A QPL focuses on qualifying individual products or families of products. A QPL will normally be appropriate for items of supply that are stable and will be continually available for extended period of time.

6.5.4.3 QPL/QML. A transitional program that allows a manufacturer that is certified and qualified to the QML program of MIL-PRF-31032 to fabricate, test, and supply products to this specification.

6.5.5 QPL product assurance procedures. The product assurance procedures includes all associated documentation that is used by the manufacturer in order to comply with the requirements of this specification.

6.6 Environmentally preferable materials. Environmentally preferable materials should be used to the maximum extent possible that the material meets or exceeds the operational and maintenance requirements, and promotes economically advantageous life cycle costs. Table I lists the Environmental Protection Agency's (EPA) top 17 hazardous materials targeted for major usage reduction. If any of these hazardous materials are required, it is recommended that it be used only when other materials cannot meet performance requirements.

TABLE I. EPA top seventeen hazardous materials.

Benzene	Dichloromethane	Tetrachloroethylene
Cadmium and compounds	Lead and compounds	Toluene
Carbon Tetrachloride	Mercury and compounds	1,1,1 – Trichloroethane
Chloroform	Methyl Ethyl Ketone	Trichloroethylene
Chromium and compounds	Methyl Isobutyl Ketone	Xylenes
Cyanide and compounds	Nickel and compounds	

6.7 Subject term (key word) listing.

Design standard
Master drawing
Qualified Manufacturer List (QML)
Qualified Product List (QPL)
Test coupon

6.8 Compliant printed wiring boards. For a printed wiring board to be compliant with this specification, it must be produced by a manufacturer qualified for listing on QPL–55110 or reciprocal listing as described in appendix B, and must be obtained from a lot which was subjected to and passed all inspection of product for delivery verifications using the applicable product assurance program.

6.9 Changes from previous issue. Marginal notations are not used in this revision to identify changes with respect to the previous issue due to the extensiveness of the changes.

PRODUCT ASSURANCE (QUALIFICATION AND VERIFICATION) REQUIREMENTS FOR QUALIFIED PRODUCTS LIST PROGRAMS

A.1. SCOPE

A.1.1 Scope. This appendix contains the requirements and procedures for manufacturers using the traditional QPL method of product assurance (qualification and verification inspection) for printed wiring boards covered by this specification. The process for extending and retaining qualification is also herein. This appendix is a mandatory part of the specification for non-QML manufacturers. The information contained herein is intended for compliance only.

A.2. APPLICABLE DOCUMENTS

A.2.1 General. The documents listed in this section are specified in sections A.3, A.4, or A.5 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections A.3, A.4, or A.5 of this specification, whether or not they are listed.

A.2.1.1 Non-Government publications. The following documents form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents are those cited in the solicitation or contract.

IPC – ASSOCIATION CONNECTING ELECTRONICS INDUSTRIES (IPC)

J–STD–003	–	Solderability Tests for Printed Boards.
IPC–2221	–	Printed Board Design, Generic Standard on.
IPC–A–600	–	Acceptability of Printed Boards.
IPC–TM–650	–	Test Methods Manual.
IPC–9252	–	Guidelines and Requirements for Electrical Testing of Unpopulated Printed Boards.
IPC–100041	–	Master Drawing for Single Sided Printed Boards.
IPC–100042	–	Master Drawing for Double Sided Printed Boards.
IPC–100043	–	Master Drawing for 10 Layer Multilayer Printed Boards.
IPC–100044	–	Master Drawing for 4 Layer Multilayer Printed Boards.
IPC–100047	–	Composite Test Pattern Basic Dimension Drawing (Ten Layers).

(Application for copies should be addressed to the IPC – Association Connecting Electronics Industry, 3000 Lakeside Drive, Suite 309 S, Bannockburn, IL 60015–1249 or at URL http://www.ipc.org.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

A.2.2 Order of precedence. In the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

A.3. REQUIREMENTS

A.3.1 General. The performance requirements contained in this section, although sometimes determined by examination of sampled printed wiring boards or test coupons, apply to all deliverable printed wiring boards.

A.3.1.1 Master drawing (see A.6.2.1.c). Printed wiring boards delivered under this specification shall be of the material, design, and construction specified on the applicable master drawing. For the purposes of this appendix, when the term "specified" is used without additional reference to a specific location or document, the intended reference shall be to the applicable master drawing. If individual design details are not specified on the applicable master drawing, then the baseline design parameters shall be as detailed in the design standard that was used to design the printed wiring board (see A.3.3).

A.3.2 Qualification. Printed wiring boards furnished under this specification shall be products that are authorized by the qualifying activity for listing on the applicable QPL at the time of award of contract (see A.4.5 and A.6.3). In addition, the manufacturer shall certify that the product assurance procedure requirements of A.4.5.5.2 have been met and are being maintained.

A.3.3 Design (see A.6.2.1.d). Printed wiring boards shall be of the design as specified (see A.3.1.1). Unless otherwise specified, if individual design details are not specified on the applicable master drawing, then the baseline design parameters to be use for acceptability of finished product requirements shall be as detailed in the design standard that was used to design the printed wiring board. If no design standard is specified on the master drawing or the appropriate design standard cannot be determined, then the default design shall be performance class 3 of IPC-2221.

A.3.3.1 Test coupons. Test coupon design and placement on a panel shall be in accordance with the applicable design standard specified (see A.3.1.1). Test coupon selection, usage, and quantity on a panel shall be determined by the manufacturer in order to meet the in-process, group A, and group B inspection requirements. NOTE: Test coupon design shall be as specified in the applicable design standard and shall reflect worst case design conditions of the printed board(s) they represent.

A.3.4 Material. The printed wiring boards shall be constructed of material as specified (see A.3.1.1). When a definite material is not specified (see A.3.1.1), a material shall be used that will enable the printed wiring board to meet the performance requirements of this specification. Acceptance or approval of any material shall not be construed as a guaranty of the acceptance of the finished printed wiring board.

A.3.4.1 Recycled, recovered, or environmentally preferable materials. Recycled, recovered, or environmentally preferable materials should be used to the maximum extent possible, provided that the material meets or exceeds the operational and maintenance requirements, and promotes economically advantageous life cycle costs.

A.3.4.2 Pure tin. Unless otherwise specified (see A.3.1.1), the use of pure tin, as an underplate or final finish, is prohibited both internally and externally. Tin content of printed board finishes and solder shall not exceed 97 percent, by mass. Tin shall be alloyed with a minimum of 3 percent lead, by mass (see A.6.8).

A.3.5 External visual and dimensional requirements. When examined in accordance with A.4.8.1, the finished printed wiring board shall meet the visual and dimensional requirements specified in A.3.1.1 and A.3.5.1 through A.3.5.7.5. IPC-A-600 contains figures, illustrations, and photographs that can aid in the visualization of externally observable accept/reject conditions of test specimens. If a condition is not addressed herein or specified on the master drawing, it shall comply with the class 3 criteria of IPC-A-600.

A.3.5.1 Base materials.

A.3.5.1.1 Edges of base material. Burrs, crazing, nicks, and haloing along the edges of printed wiring boards, including edges of cutouts and edges of non-plated-though holes, shall be acceptable provided the penetration does not reduce the edge spacing by more than 50 percent of the edge spacing specified (see A.3.1.1) or .10 inch (2.5 mm), whichever is smaller. If no requirement for edge spacing is specified (see A.3.1.1), the penetration shall not exceed .10 inch (2.5 mm). Panels that are partially routed with breakaway tabs or scored for printed board removal shall meet the de-panelization requirements specified (see A.3.1.1).

A.3.5.1.2 Surface imperfections. Surface imperfections (such as scratches, pits, dents, cuts or exposed reinforcement fibers, and weave texture) shall be acceptable providing the imperfection meets the following:

a. The base material reinforcement material (woven or non-woven fiber) is not cut, disturbed, or exposed.

b. The imperfection does not bridge between conductors (weave texture may bridge conductors).

c. The dielectric spacing between the imperfection and conductors does not reduce conductor spacing below the specified minimum requirements (see A.3.1.1).

A.3.5.1.3 Subsurface imperfections (see A.6.8). Subsurface imperfections (such as blistering, haloing, and delamination) shall be acceptable providing the imperfection meets the following:

a. The imperfection is translucent.

b. The imperfection does not bridge more than 25 percent of the distance between conductors or plated-through holes. No more than two percent of the printed wiring board area on each side shall be affected.

c. The imperfection does not reduce conductor spacing between adjacent conductors below the minimum requirements specified (see A.3.1.1).

d. The imperfection does not propagate as a result of testing (such as rework simulation, thermal stress, or thermal shock).

e. Color variations or mottled appearance in bond enhancement treatments shall be acceptable. Random areas of missing bond enhancement treatment shall not exceed 10 percent of the total conductor surface area of the affected layer.

A.3.5.1.3.1 Foreign inclusions. Foreign inclusions shall be permitted when they meet the following:

a. The foreign inclusions are translucent.

b. The foreign inclusion is located at least .010 inch (0.25 mm) from the nearest conductor.

c. The foreign inclusion does not reduce the spacing between conductors below the minimum conductor spacing specified (see A.3.1.1). If not specified, the inclusion does not reduce the conductor spacing by more than 50 percent.

d. The foreign inclusions longest dimension is no greater than .032 inch (0.81 mm) in circuitry areas. Inclusions in non-circuitry areas have no maximum dimension requirement.

e. When the base material specification allows for more or larger inclusions, those inclusions are allowed in the finished printed board, up to the size and quantity defined by the base material specification provided that the inclusion does not violate the conductor spacing requirements of A.3.5.1.3.c.

A.3.5.1.3.2 Subsurface spots. Subsurface spots shall be permitted when they meet any of the following:

a. The spots are translucent.

b. The spots are known to be weave texture and not delamination or disbonding.

c. The spots are isolated white spots that are at least .010 inch (0.25 mm) from the nearest conductor or that do not propagate as a result of any soldering operation (gelation particles are acceptable regardless of location).

A.3.5.1.3.3 Measling and crazing. Measling and crazing shall not exceed the requirements specified in IPC-A-600, class 3, for bare printed wiring boards.

A.3.5.2 Conductor pattern.

A.3.5.2.1 Annular ring, external (see figure A–1). The minimum external annular ring shall be as specified (see A.3.1.1). If not specified, the minimum external annular ring shall be .002 inch (0.051 mm) for plated through holes and .006 inch (0.152 mm) for unsupported holes. Unless otherwise specified, the external annular ring may have, in isolated areas, a 20 percent reduction of the minimum external annular ring specified (see A.3.1.1), due to defects such as pits, dents, nicks, and pinholes.

A.3.5.2.2 Conductor spacing. The conductor spacing, including tolerance, shall be as specified (see A.3.1.1). The minimum edge spacing shall be as specified (see A.3.1.1). If no conductor spacing tolerance is specified, a reduction in the conductor spacing of 10 percent above the specified spacing, due to isolated defects or misregistration, shall be considered acceptable.

A.3.5.2.3 Conductor width. The conductor width(s) shall be as specified (see A.3.1.1).

A.3.5.2.4 Conductor pattern imperfections (see figure A–2). The conductor pattern shall contain no cracks, splits or tears. Unless otherwise specified (see A.3.1.1), any combination of edge roughness, nicks, pinholes, cuts or scratches exposing the base material shall not reduce each conductor width more than 20 percent of its minimum specified width. There shall be no occurrence of the 20 percent reductions greater than .50 inch (12.70 mm) or 10 percent of a conductor length, whichever is less.

A.3.5.2.5 Conductor width reduction (see figure A–2). Allowable reduction in the conductor width, due to isolated defects or misregistration, shall not exceed 20 percent of the minimum conductor width.

A.3.5.2.6 Conductor finish coverage. The conductor finish plating or coating shall completely cover the basis metal of the conductive pattern. Complete conductor coverage by solder does not apply to the vertical conductor edges. There shall be no evidence of any lifting or separation of conductor finish plating or coating from the surface of the conductive pattern. There shall be no whiskers of solder or plating on the surface of the conductive pattern. For designs using solder resist over bare conductors, it shall be acceptable to have up to .010 inch (0.25 mm) of exposed base metal at the interface between the solder resist and the basis metal conductor finish. For design requiring unfused tin-lead plating as a final conductor finish coverage, the thickness shall be as specified (see A.3.1.1 and A.3.3).

A.3.5.2.7 Solderable surface mount lands and wire bond pads. The allowable imperfections along the external edges of lands, or to the surface of the land of surface mount lands or wire bond pads, shall not exceed the requirements specified in IPC-A-600, class 3, for surface plating - wire bond pads.

A.3.5.3 Dimensions of features. The finished printed wiring board shall meet the dimensional requirements for features such as cutouts, periphery, overall board thickness, etc. as specified (see A.3.1.1).

A.3.5.4 Hole pattern accuracy. The accuracy of the hole pattern, sizes and locations, on the printed wiring board shall be as specified (see A.3.1.1).

A.3.5.5 Lifted lands. There shall be no lifted lands on the deliverable, non-thermal stressed printed wiring board.

A.3.5.6 Registration, external (method I). Registration of external lands shall be satisfied if the external layers meet the specified annular ring requirements (see A.3.1.1 and A.3.5.2.1). Misregistration shall not reduce the minimum external annular ring below its specified limits.

A.3.5.7 Solder resist (when applicable). Unless otherwise specified, the solder resist requirements specified in A.3.5.7.1 through A.3.5.7.5 shall apply.

A.3.5.7.1 Coverage. Solder resist coverage imperfections (such as blisters, delaminations, pits, skips, wrinkles, and voids) shall be acceptable providing the imperfection meets all of the following:

a. The solder resist imperfection shall not expose two adjacent conductors whose spacing is less than the electrical spacing required for the voltage range and environmental condition specified in the applicable design standard.

b. In areas containing parallel conductors, the solder resist imperfection shall not expose two isolated conductors whose spacing is less than 0.5 mm (.020 inch) unless one of the conductors is a test point or other feature area which is purposely left uncoated for subsequent operations.

c. The exposed conductor shall not be bare copper.

d. The solder resist imperfection does not expose via holes that are to be tented or filled by solder resist.

e. Pits or voids in non-conductor areas shall be acceptable if they do not exhibit blistering or lifting in excess of that allowed in A.3.7.4.6.

A.3.5.7.2 Discoloration. Discoloration of metallic surfaces under the cured solder resist shall be acceptable.

A.3.5.7.3 Registration (see figure A–3). The solder resist shall be registered to the land or terminal patterns in such a manner as to meet the requirements specified (see A.3.1.1). If no requirements are specified, the following apply:

a. For plated-through holes and vias, the following shall apply:

   (1) Solder resist misregistration onto plated-through component hole lands (plated-through holes to which solder connections are to be made) shall not reduce the external annular ring below the specified minimum requirements.

   (2) Solder resist shall not encroach into plated-through hole barrels or onto other surface features (such as connector fingers, or lands of unplated holes) to which solder connections will be made.

   (3) Solder resist is permitted in plated holes or vias in which no lead is to be soldered.

b. For surface mount lands with no plated-through holes, the following shall apply:

   (1) For lands with a pitch of .050 inch (1.27 mm) or greater, solder resist encroachment is on one side of land only and does not exceed .002 inch (0.050 mm).

   (2) For lands with a pitch less than .050 inch (1.27 mm), solder resist encroachment is on one side of land only and does not exceed .001 inch (0.025 mm).

c. For ball grid array lands, the following shall apply:

(1) If the land is solder resist defined, allowable misregistration of the solder resist causes breakout of the land of not more than 90 degrees.

(2) If the land is copper defined, the solder resist shall not encroach onto the land. Solder resist on the land-to-via connecting conductor shall be acceptable.

(3) If solder resist dam is specified, the dam remains in place with the conductor to the via covered.

d. Edge-board contacts and test points which are intended for assembly testing shall be free of solder resist unless a partial coverage allowance is specified.

A.3.5.7.4 Thickness (see figure A–4). The solder resist thickness shall be as specified (see A.3.1.1).

A.3.5.7.5 Solder resist cure. The cured solder resist coating shall not exhibit tackiness, blistering, or delamination in excess of that allowed in A.3.5.7.1.

A.3.6 Plated hole requirements. When plated holes are examined by microsection, the test specimen shall meet the requirements of A.3.6.1 through A.3.6.15. IPC-A-600 contains figures, illustrations, and photographs that can aid in the visualization of internally observable accept/reject conditions of microsectioned test specimens. If a condition is not addressed herein or specified on the master drawing, it shall comply with the class 3 criteria of IPC-A-600.

A.3.6.1 Annular ring, internal (see figure A–5). The minimum annular ring for functional internal lands on type printed wiring boards shall be as specified (see A.3.1.1). If not specified on the master drawing, the minimum internal annular ring shall not be less than .002 inch (0.051 mm). Hole breakout shall not be acceptable.

A.3.6.2 Minimum external conductor thickness (types 2 and 3). The external conductor thickness shall be as specified (see A.3.1.1). When an external conductor thickness is specified, the conductor thickness (copper foil and copper plating) shall be equal to, or greater than, the specified thickness. When a conductor thickness with tolerance is specified, the external conductor thickness (copper foil and copper plating) shall be within the specified tolerance for the specified thickness. If nothing is specified, the limits for external conductors with plating defined in the "External conductor thickness after plating" table of IPC-2221 shall apply.

A.3.6.3 Minimum internal conductor thickness (type 3) and external thickness (type 1). The internal conductor thickness shall be as specified (see A.3.1.1). When a copper foil weight requirement is specified, a reduction in thickness up to 10 percent below the minimum allowable foil thickness specified by the applicable material specification shall be considered acceptable in order to accommodate a processing allowance for cleaning either by chemical or mechanical means. If the master drawing specifies a minimum conductor thickness for internal conductors, the resulting conductor shall be equal to or within the specified tolerance for the specified conductor thickness. If nothing is specified, the limits for internal layer foil thickness after processing defined in the "Internal layer foil thickness after processing" table of IPC-2221 shall apply.

A.3.6.4 Dielectric layer thickness (see figure A–6). The minimum dielectric thickness separating the conductor layers of the printed wiring boards shall be as specified (see A.3.1.1). If not specified on the master drawing, the minimum dielectric spacing base materials shall not be less .0035 inch (0.089 mm).

A.3.6.4.1 Heatsink planes (see figure A–7). Radial cracks, wicking, or voids in the dielectric material used to insulate the heatsink plane, or metal core, from circuitry and plated through holes, shall not reduce by 75 percent the specified lateral spacing between adjacent conductive surfaces. Unless otherwise specified (see A.3.1.1), the minimum lateral spacing between adjacent conductive surfaces, nonfunctional lands, or plated-through hole and the heatsink plane shall be .004 inch (0.102 mm).

A.3.6.5 Delamination. Printed wiring boards shall have no delaminations in excess of that allowed in A.3.5.1.3.

A.3.6.6 Etchback or smear removal (type 3).

A.3.6.6.1 Etchback (when specified, see A.3.1.1) (see figures A–8 and A–9). When specified (see A.3.1.1), printed wiring boards shall be etched back for the lateral removal of resin and reinforcement material (woven glass or other media) from the internal conductors prior to plating. Unless otherwise specified (see A.3.1.1), etchback shall be a minimum of.0002 inch (0.005 mm) and no greater than the specified minimum internal annular ring or .002 inch (0.05 mm), whichever is less, with a preferred depth of .0005 inch (0.013 mm) when measured at the internal copper contact area protrusion (see figure A–8). The etchback shall be effective on at least the top or bottom (or both) surface of each internal conductor to provide at least a two (2) point contact with the subsequent hole plating (see figure A–9). Negative etchback is not acceptable when etchback is specified. Wicking shall meet the requirements of A.3.6.6.3.

A.3.6.6.2 Smear removal (hole cleaning) (see figure A–8). When etchback is not specified (see A.3.1.1), the vertical faces of the internal conductors of the plated-through hole shall be cleaned to be free of resin smear. Lateral removal of base material from the hole wall shall not exceed .001 inch (0.03 mm). When etchback is not specified (see A.3.1.1), a negative etchback of .0005 inch (0.013 mm) maximum shall be acceptable.

A.3.6.6.3 Wicking (see figure A–10). Wicking of copper plating extending .003 inch (0.08 mm) into the base material shall be acceptable provided it does not reduce the conductor spacing below the minimum clearance spacing requirements specified (see A.3.1.1).

A.3.6.7 Laminate (base material) voids. Laminates cracks shall be considered and treated as laminate voids.

A.3.6.7.1 As received condition. Laminate voids with the longest dimension of .003 inch (0.08 mm) or less shall be acceptable.

A.3.6.7.2 After rework simulation, thermal shock or thermal stress testing (see figure A–11). Laminate voids are not evaluated in zone A (the thermal zone of stressed plated holes of figure A–11). Laminate voids in zone B (the laminate evaluation area of stressed plated holes of figure A–11) with the longest dimension of .003 inch (0.08 mm) or less shall be acceptable provided the conductor spacing is not reduced below the minimum dielectric spacing requirements, laterally or vertically, as specified (see A.3.1.1).

A.3.6.8 Lifted lands (see figure A–12).

A.3.6.8.1 As received condition. There shall be no lifted lands on the as received specimen. When inspected in accordance with A.4.8.2 and lifted lands are present, the lot shall be 100 percent visually inspected in accordance with A.4.8.1 for separation of the lands from the base material.

A.3.6.8.2 After rework simulation, thermal stress or thermal shock testing. After undergoing rework simulation, thermal stress, or thermal shock testing (see A.3.7.4.4, A.3.7.4.8, and A.3.7.6.2), the maximum allowed distance from the plane of the base material surface to the bottom of the edge of the land or pad shall be no greater than the total land thickness. The total land thickness is equal to the combined thickness of the metal foil and copper plating on that land.

A.3.6.9 Plating and coating properties.

A.3.6.9.1 Plating and coating thickness (when applicable). Unless otherwise specified (see A.3.1.1), the plating or coating thickness shall be in accordance with table A–I. (Also see A.3.4.2 and A.3.5.2.6).

TABLE A–I. Conductor plating and finish thickness.

Material	Thickness, in inches
Copper (in holes, blind vias, surface)	.001 (0.025 mm)
Copper (buried vias)	.0006 (0.015 mm)
Copper (low aspect ratio blind vias, blind microvias)	.00047 (0.012 mm)
Gold (for edge-board contacts and areas not to be soldered) (minimum)	.00005 (0.0013 mm)
Gold (on areas to be soldered) (maximum)	.000018 (0.00046 mm)
Gold (on areas to be wire bonded, ultrasonic) (minimum)	.000002 (0.00005 mm)
Gold (on areas to be wire bonded, thermosonic) (minimum)	.00003 (0.0008 mm)
Immersion gold	.000002 to .000009 (0.00005 to 0.00023 mm)
Nickel (for edge-board contacts) (minimum)	.0001 (0.0025 mm)
Nickel (barrier to prevent formation of copper-tin compounds) (minimum)	.0002 (0.005 mm)
Nickel, Electroless	.0001 to .0002 (0.0025 to 0.005 mm)
Organic Solderabilty Preservative (OSP), immersion silver	Solderable
Tin-lead, fused or solder coat	Coverage and solderable
Tin-lead, unfused	.0003 (0.008 mm)
Solder coat over base copper	Coverage and solderable

A.3.6.9.2 Copper plating thickness (when applicable) (see figure A–13). Copper plating thickness (on the surface, in plated-through holes, buried vias, blind vias, and low aspect ratio blind vias) shall be as specified (see A.3.1.1). If not specified on the master drawing, the copper plating shall comply with the thicknesses defined in table A–I.

A.3.6.9.3 Copper plating defects. Unless otherwise specified (see A.3.1.1), a 20 percent reduction of the specified copper plating thickness shall be acceptable if it is non-continuous (isolated; not more than 10 percent of the composite board thickness). Any copper plating less than 80 percent of the specified thickness shall be treated as a copper plating void.

A.3.6.9.3.1 Copper plating voids (see figure A–14). The copper plating in the plated holes shall not exhibit any void in excess of the following:

a. There shall be no more than one plating void per panel, regardless of length or size.

b. There shall be no plating void in excess of 5 percent of the total printed wiring board thickness.

c. There shall be no plating voids evident at the interface of an internal conductive layer and plated hole wall.

A.3.6.9.4 Plating separations (see figures A–15, A–16, and A.7.3). Except for along the vertical edge of the external copper foil, there shall be no separations or contamination between the hole wall conductive interfaces. Conductive interface separations along the vertical edge of the external copper foil shall be acceptable.

A.3.6.10 Heatsink planes (see figure A–7). Unless otherwise specified (see A.3.1.1), when heatsink planes are used as electrically functioning circuit, they shall meet the requirements of A.3.6.9.2 through A.3.6.9.4 inclusive.

A.3.6.11 Plated hole wall deficiencies (see figure A–16). Nodules, plating folds, or plated reinforcement material fibers that project into the copper plating shall be acceptable provided that the hole diameter and the hole wall copper thickness are not reduced below their specified limits.

A.3.6.12 Metallic cracks. There shall be no cracks in any plating, coating, or the internal layer conductive foils. Cracks in outer layer conductive foil shall be acceptable if they do not propagate into any plating or coating. Cracks shall not be acceptable in the copper plating.

A.3.6.13 Nail-heading. Nail-heading of conductors shall not exceed one and a half times the copper foil thickness.

A.3.6.14 Resin recession.

A.3.6.14.1 As received specimens. Resin recession at the outer surface of the plated hole barrel wall shall be permitted provided the maximum depth as measured from the barrel wall does not exceed .003 inch (0.08 mm) and the resin recession on any side of the plated-through hole does not exceed 40 percent of the cumulative base material thickness (sum of the dielectric layer thickness being evaluated) on the side of the plated-through hole being evaluated.

A.3.6.14.2 Stressed specimens (after rework simulation, thermal shock or thermal stress testing). Resin recession at the outer surface of the plated hole barrel shall be permitted and is not cause for rejection.

A.3.6.15 Undercutting. Undercutting at each edge of the conductors shall not exceed the total thickness of the copper foil and plated copper.

A.3.7 Inspection requirements. The detailed requirements contained in this section, although determined by examination of sample printed wiring board test specimens (production printed wiring boards, test coupons, or microsectioned test coupons), apply to all deliverable printed wiring boards.

A.3.7.1 Acceptability (of printed wiring boards). When examined as specified in A.4.8.1, the printed wiring boards shall be in accordance with the acceptance requirements specified in A.3.1.1 (master drawing), A.3.4 (material), A.3.5 (visual and dimensional), A.3.7.4.6.1 (solder resist cure), A.3.8 (marking), A.3.10 (repair), and A.3.12 (workmanship), as applicable.

A.3.7.2 Microsection evaluation.

A.3.7.2.1 As received printed wiring board test specimens. When “as received” printed wiring board test specimens (unstressed printed wiring boards, supporting test coupons, or qualification test specimens) are examined as specified in A.4.8.1, the requirements specified in A.3.8 and A.3.12 shall be met. After meeting the external visual requirements, the “as received” printed wiring board test specimens shall be microsectioned and examined as specified in A.4.8.2 and the requirements of A.3.6 shall be met.

A.3.7.2.2 Registration, internal.

A.3.7.2.2.1 Method II (by microsection). Unless otherwise specified (see A.3.1.1), when inspected as specified in A.4.8.2.4, registration of internal lands shall be satisfied if the internal layers meet the specified annular ring requirements (see A.3.1.1 and A.3.5.2.1).

A.3.7.2.2.2 Method III (by registration test coupons). Registration test coupons may have been designed into the printed wiring board by the design activity, or may be added to the panel by the manufacturer to enhance testability (see A.4.8.2.4.2 and appendix D). To be usable for acceptance purposes, registration test coupons shall relate the actual grid location of each circuitry layer to all other circuitry layers and to the hole pattern accuracy required (see A.3.5.4) in each printed wiring board.

A.3.7.3 Chemical requirements.

A.3.7.3.1 Cleanliness. When printed wiring boards are tested in accordance with A.4.8.3.1, the levels of cleanliness shall be in accordance with the requirements of A.3.7.3.1.1 or A.3.7.3.1.2, as applicable.

A.3.7.3.1.1 Prior to the application of solder resist and qualification (see A.6.4). For qualification, and unless otherwise specified, prior to the application of solder resist, the level of ionic contamination shall not exceed an equivalent of 10.06 micrograms/square inch (1.56 micrograms/square centimeter) of sodium chloride. Alternative test methods or test equipment specified in A.6.4 may be used in lieu of the method specified in A.4.8.3.1. When printed wiring boards are tested using an alternative test method or test equipment specified in A.6.4, the final value shall be less than the equivalents of sodium chloride specified for the printed wiring board surface area tested.

A.3.7.3.1.2 Completed printed wiring boards (when specified, see A.3.1.1 and A.6.2.2.g). The levels of cleanliness for completed printed wiring boards shall be as specified.

A.3.7.3.2 Resistance to solvents (marking inks or paints). After marking is tested in accordance with A.4.8.3.2, any specified markings which are missing in whole or in part, faded, smeared, or shifted (dislodged) to the extent that they cannot be readily identified shall constitute failure.

A.3.7.4 Physical requirements.

A.3.7.4.1 Bow and twist. When tested as specified in A.4.8.4.1, the maximum allowable bow and twist of the printed wiring board shall be within the limits specified (see A.3.1.1). If not specified, the limits for bow and twist shall be 0.75 percent for designs that use surface mount components and 1.5 percent for all other designs.

A.3.7.4.2 Conductor edge outgrowth.

A.3.7.4.2.1 Conductors covered with solder. When the printed wiring board test specimen is examined as specified in A.4.8.1, there shall be no outgrowth of the solder coating on the conductor edges.

A.3.7.4.2.2 Conductors covered with metals other than solder. After undergoing the test as specified in A.4.8.4.2, the printed wiring board test specimen shall be examined as specified in A.4.8.1 and the maximum permissible outgrowth on conductors shall be .001 inch (0.03 mm).

A.3.7.4.3 Plating adhesion. When tested as specified in A.4.8.4.3, there shall be no plating particles or conductor patterns removed from the printed wiring board test specimen except for outgrowth or slivers.

A.3.7.4.4 Rework simulation. Rework simulation is not applicable for printed wiring board designs that do not use any through-holes (unsupported or plated) for component attachment.

A.3.7.4.4.1 Type 1 with unsupported holes (bond strength). After undergoing the test specified in A.4.8.4.4.1, the unsupported land shall withstand 5 pounds (2.27 Kg) pull or 500 PSI (3.4 MPa), whichever is less.

A.3.7.4.4.2 Types 2 and 3 with plated-through holes. After undergoing the test specified in A.4.8.4.4.2, the type 2 or 3 printed wiring board test specimens shall meet the following requirements:

a. External visual and dimensional inspection: When inspected as specified in A.4.8.1, there shall be no evidence of blistering, crazing, or delamination in excess of that allowed in A.3.5.

b. Internal visual and dimensional inspection: After the printed wiring board test specimen is microsectioned and inspected in accordance with A.4.8.2, the requirements specified in A.3.6 shall be met.

A.3.7.4.5 Solderability. Solderability testing is applicable only on printed wiring board designs that require soldering during circuit card assembly processes. Unless otherwise specified (see A.3.1.1), printed wiring board designs that use compliant pin technology only for component attachment do not require solderability testing. Unless otherwise specified (see A.3.1.1), printed wiring board designs that use surface mount components only shall be tested for surface solderability, not hole solderability. Printed wiring board designs that use both surface mount and through-hole mounted components shall be tested for both surface and hole solderability.

A.3.7.4.5.1 Hole (plated through hole). After undergoing the test specified in A.4.8.4.5.1, the printed wiring board test specimen shall conform to the accept/reject criterion (good wetting, pinholes, dewetting, non-wetting, etc.) specified in J-STD-003, class 3 or appendix E, as applicable.

A.3.7.4.5.2 Surface or surface mount land. After undergoing the test specified in A.4.8.4.5.2, the printed wiring board test specimen shall conform to the accept/reject criterion (good wetting, pinholes, dewetting, non-wetting, etc.) specified in J-STD-003, class 3 or appendix E, as applicable.

A.3.7.4.6 Solder resist cure and adhesion.

A.3.7.4.6.1 Solder resist cure. When inspected as specified in A.4.8.1, the cured solder resist shall not exhibit tackiness, blistering, or delamination.

A.3.7.4.6.2 Solder resist adhesion. When tested as specified in A.4.8.4.6, the maximum percentage of cured solder resist lifted from the surface of the base material, conductors, and lands of the coated printed wiring board test specimen shall not exceed the following:

a. Bare copper or base material: 0 percent.

b. Gold or nickel plating: 5 percent.

c. Melting metals, including tin-lead plating or solder coating: 10 percent.

A.3.7.4.7 Surface peel strength (type 3 foil laminated printed wiring boards). After undergoing the test specified in A.4.8.4.7, the surface conductor shall withstand a minimum peel strength greater than or equal to the "after thermal stress" values for the corresponding copper foil type, profile, and weight specified by the base material specification. This requirement is only applicable to foil laminated type 3 printed wiring boards that have surface conductors or surface mount lands. Printed wiring boards with no external circuitry (external terminal land or pads only) do not require peel strength testing.

A.3.7.4.8 Thermal stress.

A.3.7.4.8.1 Type 1. After undergoing the test specified in A.4.8.4.8.1, the printed wiring board test specimen shall be inspected in accordance with A.4.8.1 and shall not exhibit any cracking or separation of plating and conductors, blistering or delamination shall not exceed the limits allowed in A.3.5.1.3 and lands shall not lift in excess of that allowed in A.3.5.5.

A.3.7.4.8.2 Types 2 and 3. After undergoing the test specified in A.4.8.4.8.2, the printed wiring board test specimen shall be examined in accordance with A.4.8.1 and shall exhibit no blistering or delamination in excess of that allowed in A.3.5.1.3. After meeting the visual and dimensional requirements of A.3.5, the printed wiring board test specimen shall be microsectioned and inspected in accordance with A.4.8.2 and shall meet the requirements of A.3.6.

A.3.7.5 Electrical requirements (see IPC–9252 for additional guidelines).

A.3.7.5.1 Circuit continuity. The circuit continuity test shall be in accordance with A.4.8.5.1. For qualification inspection there shall be no circuit whose resistance exceeds 20 ohm. Unless otherwise specified (see A.3.1.1), for referee purposes, 0.1 ohm maximum per inch of circuit length shall apply. Circuits that consist of long runs of narrow conductors or short runs of very wide conductors may increase or decrease the resistance. The acceptability of these type of circuits, of controlled impedance nets, or of designed resistive patterns shall be specified on the master drawing (see A.3.1.1).

A.3.7.5.2 Circuit shorts. When tested as specified in A.4.8.5.2, the resistance between mutually isolated conductors shall be greater than 2 megohms.

A.3.7.5.3 Dielectric withstanding voltage (DWV). When tested as specified in A.4.8.5.3, there shall be no flashover, sparkover, or dielectric breakdown.

A.3.7.5.4 Heatsink planes or metal core printed boards. When designs with heatsink planes or metal cores are inspected as specified in A.4.8.5.2, the dielectric material used to insulate the heatsink plane or metal core from the conductor pattern and plated through holes shall provide an insulation resistance greater than 2 megohm. The printed board shall be capable of withstanding the specified voltage between the conductor pattern or plated-through holes and the heat sink plane. During the test there shall be no flashover, sparkover, or dielectric breakdown.

A.3.7.6 Environmental requirements.

A.3.7.6.1 Moisture and insulation resistance (MIR).

A.3.7.6.1.1 Non-flush conductor printed boards. When tested as specified in A.4.8.6.1, the printed wiring board test specimen shall have a minimum of 500 megohms of resistance between conductors when tested at 500 volts (+25, –0) direct current. After the test, the specimen shall be inspected in accordance with A.4.8.1 and the specimen shall not exhibit blistering, measling, or delamination in excess of that allowed in A.3.5.1.3.

A.3.7.6.1.2 Flush conductor printed boards. When tested as specified in A.4.8.6.1.1, the printed wiring board designed for flush conductor applications shall have a minimum of 50 megohms of resistance between conductors when tested at 500 volts (+15, –0) direct current. After the test, the specimen shall be inspected in accordance with A.4.8.1 and the specimen shall not exhibit blistering, measling, or delamination in excess of that allowed in A.3.5.1.3.

A.3.7.6.2 Thermal shock.

A.3.7.6.2.1 Thermosetting resin base materials (see A.7.6.1). While undergoing the test specified in A.4.8.6.2.1, a resistance change of 10 percent or more between the first and last high temperature measurements shall be considered a reject. After the test, the printed wiring board test specimens shall meet the following requirements:

a. External visual and dimensional inspection (all types): When inspected as specified in A.4.8.1, there shall be no evidence of plating cracks, blistering, or delamination in excess of that allowed in A.3.5.1.3.

b. Internal visual and dimensional inspection (type 3): When the printed wiring board test specimen is microsectioned and inspected in accordance with A.4.8.2, the requirements specified in A.3.6 shall be met.

A.3.7.6.2.2 Thermoplastic resin base materials (see A.7.6.2). While undergoing the test specified in A.4.8.6.2.2, a resistance change of 10 percent or more between the first and last high temperature measurements shall be considered a reject. After the test, when printed wiring board test specimens are inspected as specified in A.4.8.1, the shall be no evidence of plating cracks, blistering, or delamination in excess of that allowed in A.3.5.1.3.

A.3.8 Marking. Unless otherwise specified (see A.6.2), each production printed wiring board, each qualification test specimen, and each set of quality conformance test circuit strips (as opposed to each individual test coupon) shall be marked as specified (see A.3.1.1) and herein. As a minimum, each production printed wiring board, qualification test specimen, or quality conformance test circuit strip shall reference the printed wiring board manufacturers' CAGE code, lot date, and printed wiring board traceability code. The marking shall be produced by the same process used in producing the conductive pattern; or by the use of a nonconductive, fungistatic ink; or paint applied to the printed wiring board; or to a label which is applied to the printed wiring board; or by mechanical pencil marking, mechanical machining, or laser machining on a metallic area provided for marking purposes. All marking shall be able to withstand solder fluxes, cleaning solutions, and molten solder encountered in the manufacture of printed wiring boards. The marking shall remain legible after all tests and in no manner affect printed wiring board performance.

A.3.9 Traceability. Unless otherwise specified, traceability shall be available for review by the qualifying or acquiring activity for a minimum of 3 years after delivery of the printed wiring boards. Supporting test data, test coupons, and microsection mounts shall be retained by the manufacturer or acquiring activity.

A.3.9.1 Quality conformance test circuitry, test coupons, and microsection mounts. Each quality conformance test circuitry (QCTC) shall be identifiable with those corresponding production printed wiring boards produced on the same panel that also produced the QCTC. All individual test coupons (including those in micorsection mounts) separated from its QCTC, or qualification test specimen, shall have its traceability maintained back to the panel, QCTC, or qualification test specimen from which the test coupons were separated. When a QCTC or test coupon is representative of more than one printed board design (multiple designs per panel), it shall be traceable to those printed boards fabricated on that panel. When a microsection mount contains more than one specimen, an orientation mark or other identification marking shall identify layer one of the first specimen. Also, unless otherwise listed on the multiple specimen microsection mount, traceability identifying all specimens contained in a mount shall be maintained.

A.3.9.2 Printed board materials. Traceability shall be such that for each printed wiring board, all printed board materials specified or used shall be traceable to a material production lot, inspection lot, or other specified grouping.

A.3.10 Repair. When inspected in accordance with A.4.8.1, printed wiring boards shall not be repaired or reveal any evidence of repair.

A.3.11 Recycled, recovered, or environmentally preferable materials. Recycled, recovered, or environmentally preferable materials should be used to the maximum extent possible provided that the material meets or exceeds the operational and maintenance requirements, and promotes economically advantageous life cycle costs.

A.3.12 Workmanship. Printed wiring boards shall be processed in such a manner as to be uniform in quality and shall be free from defects in excess of those allowed in this appendix that could affect life or serviceability.

A.4. VERIFICATION

A.4.1 Classification of inspections. The inspection requirements specified herein are classified as follows:

a. Qualification inspection (see A.4.5).

b. Inspection of product for delivery (see A.4.6).

c. Periodic conformance inspection (see A.4.7).

A.4.2 Test and measuring equipment. Measuring and test equipment of sufficient precision and bias, quality, and quantity to permit performance of the required inspection shall be established and maintained by the manufacturer. The establishment and maintenance of a calibration system to control the accuracy of the measuring and test equipment shall be in accordance with appendix C.

A.4.3 Inspection conditions. Unless otherwise specified in the applicable test method or procedure, inspections and tests shall be performed in accordance with test method number 1.3 of IPC-TM-650.

A.4.4 Printed wiring board performance verification. Printed wiring board performance verification shall consist of inspections on the production printed wiring boards and the QCTC or test coupons referenced in tables herein for in-process, groups A and B inspections. Selection of test coupons for testing shall be in accordance with the applicable inspection table. Each production printed wiring board or panel of printed wiring boards shall include sufficient test coupons to complete the applicable verification requirements specified. The design of test coupons shall be as specified on the applicable master drawing (see A.3.1.1). The minimum number of test coupons on the production panel and the requirements for positioning the test coupons on the panel shall be in accordance with the requirements of the applicable design standard (see A.3.1.1 and appendix D).

A.4.4.1 Verifications preformed by a certified suitable laboratory. Because of the performance nature of this document, the design and construction details of the printed boards, or the test coupons that represent the printed boards, shall be supplied with the sample units to be inspected or tested by a certified suitable laboratory. The design and construction details are needed so that the resulting evaluations can confirm compliance to both the master drawing and the acceptability requirements herein. This communication of design and construction details shall apply whenever printed wiring boards, panels of printed wiring boards, or test coupons are tested and inspected to either group A (including electrical testing) or group B inspection herein performed by a certified suitable laboratory.

A.4.5 Qualification inspection. Qualification inspection shall be performed at the manufacturing location and a laboratory acceptable to the Government (see 6.3) on sample units produced with equipment and procedures normally used in production.

A.4.5.1 Qualification eligibility. The fabrication of the qualification test vehicles may begin before authorization to test is granted; however, before the start of qualification testing, the manufacturer shall receive authorization from the qualifying activity.

A.4.5.2 Samples.

A.4.5.2.1 Qualification test specimens. Qualification test specimens shall conform to the following for the type of printed wiring boards for which qualification is sought:

a. Type 1: The qualification test specimens for type 1 shall meet the requirements specified on DSCC Form 19W and the hole locations and conductor patterns of master drawing IPC-100041.

b. Type 2: The qualification test specimens for type 2 shall meet the requirements specified on DSCC Form 19W and the hole locations and conductor patterns of master drawing IPC-100042.

c. Type 3 using thermosetting resin base materials: The qualification test specimens for type 3 using thermosetting materials shall meet the requirements specified on DSCC Form 19W and the hole locations and conductor patterns of master drawing IPC-100043.

d. Type 3 using thermoplastic resin base materials: The qualification test specimens for type 3 using thermoplastic materials shall meet the requirements specified on DSCC Form 19W and the hole locations and conductor patterns of master drawing IPC-100044.

e. Type 3 alternative: The qualification test specimens for type 3 using thermosetting resin base materials shall meet the requirements specified on master drawing IPC-100047.

If design defaults are not listed on DSCC Form 19W, then the values specified in IPC-2221 shall apply. See modification to the requirements of IPC-100041, IPC-100042, IPC-100043, and IPC-100044 specified in A.4.5.2.1.1.

A.4.5.2.1.1 Modifications to qualification test specimens. All portions of zones A, B, C (except for the external conductor traces on test coupon E–5), and D of the test pattern are now required for qualification testing. Zone D will be used only in the manufacturer test routine detailed in A.4.5.3.1. Other changes to the design or requirements of the qualification test specimens are detailed on the authorization to test form, DSCC Form 19W, available from the qualifying activity. Requests for other modifications to the qualification test specimens shall be made prior to, or at the time of, the request for qualification testing.

A.4.5.2.2 Sample size. A sample of at least four qualification test specimens shall be produced by the manufacturer. Unless otherwise specified on the qualifying activity approved authorization, the qualification test specimens shall be serialized and comply with the identification marking requirements of A.3.8.

A.4.5.3 Inspection routines. Qualification inspection shall consist of the tests and inspections specified below. The following details shall apply:

a. At least four qualification test specimens (zones A, B, C, and D) shall be tested by the manufacturer in accordance with A.4.5.3.1.

b. Two of the partial qualification test specimens (zones A, B, and C) that passed the tests specified in A.4.5.3.1 shall then be destructively tested at a certified suitable laboratory (see A.6.5) in accordance with A.4.5.3.2.

c. The two remaining partial qualification test specimens not subjected to destructive testing at a certified suitable laboratory shall be retained as reference samples by the manufacturer for a period of 12 months.

A.4.5.3.1 Manufacturer test routine (MTR). The manufacturer shall perform the inspections specified in column MTR of table A–II. Non-desctructive inspections shall be performed on zones A, B, and C on all of the completed qualification test specimens in the lot. Destructive testing and microsection inspections shall be performed on test coupons from zone D. Further details concerning test coupons selection can be found in the application for qualification available from the qualifying activity.

A.4.5.3.2 Certified suitable laboratory test routine (CTR). The certified suitable laboratory shall subject two of the partial qualification test specimens (zones A, B, and C) to the inspections specified in column CTR of table A–II. The order of the inspections and tests is optional; however, the cleanliness test shall be performed first and DWV shall be performed after MIR.

A.4.5.3.3 Contract services (see A.7.4). Manufacturers wanting to use contract services for production of printed wiring boards shall first qualify using their own equipment or processes internal to their facility. Once qualified internally, a manufacturer may qualify using the contract services. This additional contract services qualification will not be listed on the QPL. The contract services shall not be extended to another external subcontractor or manufacturing location. If the contract service process or manufacturing location is changed, the manufacturer shall requalify the new contract service process.

A.4.5.3.4 Qualification rejection. Qualification approval will not be granted if any of the qualification test specimens tested in accordance with table A–II fail to meet the specified requirements.

A.4.5.4 Extent of qualification.

A.4.5.4.1 Printed wiring board type. Qualification of a particular printed wiring board type shall be extended to cover all conductor patterns of that same printed wiring board type produced.

a. Qualification of type 3 printed wiring boards shall be extended to cover types 1 and 2 printed wiring boards.

b. Qualification of type 2 printed wiring boards shall be extended to cover type 1 printed wiring boards.

TABLE A–II. Qualification inspection.

Inspection	Requirement Paragraph	Method paragraph	Test specimen 1/		Notes
			MTR	CTR	
Visual and dimensional:					
Acceptability	A.3.7.1	A.4.8.1	PWB	PWB	
Microsection:					
As received	A.3.7.2.1	A.4.8.2	AB–12	A–3	
Registration (method II)	A.3.7.2.2	A.4.8.2.4	2/	2/	
Chemical:					
Cleanliness	A.3.7.3.1	A.4.8.3.1	PWB	PWB	
Resistance to solvents	A.3.7.3.2	A.4.8.3.2	3/	3/	
Physical:					
Bow and twist	A.3.7.4.1	A.4.8.4.1	PWB	PWB	
Plating adhesion	A.3.7.4.3	A.4.8.4.3	J–1 & J–2	C–5	
Rework simulation	A.3.7.4.4	A.4.8.4.4		B–2	
Solderability					
Hole	A.3.7.4.5.1	A.4.8.4.5.1	AB–10	A–4 & B–4	4/
Surface 5/	A.3.7.4.5.2	A.4.8.4.5.2		D–2 & D–6	5/
Surface peel strength	A.3.7.4.7	A.4.8.4.7		C–1 & C–4	
Thermal stress	A.3.7.4.8	A.4.8.4.8	AB–8 & AB–13	A–1 & B–6	6/
Electrical:					
Circuit continuity	A.3.7.5.1	A.4.8.5.1	H–1, –2, & –3	D–3	7/
Circuit shorts	A.3.7.5.2	A.4.8.5.2	H–1, –2, & –3	E–3	
Dielectric withstanding voltage	A.3.7.5.3	A.4.8.5.3		E–1	8/
Environmental:					
Moisture and insulation resistance	A.3.7.6.1	A.4.8.6.1		E–1	8/
Thermal shock	A.3.7.6.2	A.4.8.6.2		D–3	

1/ See A.4.5.2 for qualification test specimen description. MTR designates manufacturer's test routine and CTR designates the certified test laboratories test routine. The reference "PWB" in a column means inspect all features, holes, and patterns in zones A, B, and C of a qualification test specimen with the exception that conductor spacing and width on test coupon E–5 shall not be evaluated in zone C. For column MTR, when a test coupon is referenced (e.g. AB–10), only one of the two coupons (9 of 18 available holes) shall be inspected, whereas for column CTR, when an individual test coupon designation is referenced (e.g. D–3) means inspect the specified test coupon. See qualification test specimen master drawing for test coupon design.

2/ Type 3 only. See A.4.8.2.4.1 for registration sample units and microsectioning details. Test coupons AB–8 and AB–13 (column MTR) or A–1 and B–6 (column CTR) can be used to meet the diagonal corner requirement.

3/ The minimum number of samples shall be at least one sample for each solution specified by the applicable test method (i.e., one sample for each solution required).

4/ Test coupons AB–10 (36 holes from four specimens) shall be used for the MTR routine; test coupons A–4 and B–4 (36 holes from two specimens) shall be used for the CTR routine.

5/ Type 1 only.

6/ Use coupon closest to the corner on MTR routine. One of the test coupons shall be microsectioned in the qualification test specimen's length direction and the other shall be microsectioned along the qualification test specimen's width direction.

7/ When circuit continuity verification is performed manually, the current shall not be in excess of 1.5 amperes and the time of application shall not exceed 30 seconds.

8/ The DWV test shall be performed after the MIR test.

A.4.5.4.2 Base material types (see A.7.6). Qualification using base material (laminates) shall be as follows:

a. Qualification with woven glass reinforced thermosetting epoxy resin base material type FR-4 (legacy type GF) shall be extended to cover types G-11 and FR-5 (legacy types GB and GH) of woven glass reinforced thermosetting epoxy resin base materials.

b. Qualification with woven glass reinforced thermosetting polyimide resin base material type GPY (legacy type GI) shall be extended to cover all other types of woven glass reinforced thermosetting polyimide resin base materials.

c. Qualification with woven glass reinforced thermoplastic polytetrafluoroethylene resin base material types (legacy type GR) shall be extended to cover all other types of woven glass reinforced thermoplastic resin base materials (legacy type GP).

d. Qualification with non-woven glass reinforced thermoplastic polytetrafluoroethylene resin base material types (legacy type GY) shall be extended to cover all other types of non woven glass reinforced thermoplastic resin base materials (legacy type GT and GX).

e. Qualification with non-woven glass reinforced thermoplastic polytetrafluoroethylene resin base material legacy type GX shall be extended to cover legacy type GT.

f. Qualification with woven glass reinforced thermosetting cyanate ester resin base materials (leagcy type GC) shall be extended to cover all other types of woven glass reinforced thermosetting cyanate ester resin base materials (legacy type SC).

g. Qualification using any other base materials shall qualify only that base material.

A.4.5.4.3 Mass lamination (see A.7.4.1). Qualification of a contract service lamination (four conductor layers) shall be extended to cover a contract service lamination of up to four conductor layers. Qualification of a contract service lamination (ten conductor layers) shall be extended to cover a contract service lamination of five or more conductor layers. NOTE: Test specimens for four layer contract lamination shall meet the requirements specified in master drawing IPC-100044. Test specimens for ten layer contract lamination shall meet the requirements specified in master drawing IPC-100043.

A.4.5.4.4 Solder resist. Qualification of any printed wiring board type shall be extended to cover the approved type with solder resist.

A.4.5.4.5 Processes.

A.4.5.4.5.1 Etchback. Qualification using etchback shall be extended to cover non-etchback. Manufacturer qualifying using contract service etchback shall submit two additional qualification test specimens fabricated using their own internal desmear process.

A.4.5.4.5.2 Process changes. Any changes to a manufacturer's qualified base material type, equipment, or processes will be reviewed by the qualifying activity for determination if partial or full requalification is necessary.

A.4.5.5 Retention of qualification. To retain qualification, the manufacturer shall make available to the qualifying activity data concerning production of qualified product at 12-month intervals. The qualifying activity shall establish the initial reporting date. The retention of qualification data shall consist of:

a. A summary of the results of the tests performed for inspection of product delivery (in-process and group A) indicating as a minimum the number of lots that have passed and the number of lots that have failed. The results of tests of all reworked lots shall be identified and accounted for.

b. A summary of the results of tests performed for periodic conformance inspection (group B) performed and completed during the 12-month period.

c. The actual test data for groups A and B shall be supplied to the qualifying activity upon request.

d. The extent of qualification of base materials specified in A.4.5.4 shall apply.

e. To retain qualification, the manufacturer shall comply with A.4.5.5.1.

f. In the event that no production occurred during the 12-month period, the manufacturer shall either certify that it still has the capabilities and facilities necessary to produce and test the qualified product or requalify.

In the event that no production occurred during the 12-month reporting period, the manufacturer shall either certify to the qualifying activity that the capability to manufacture and test QPL printed wiring boards still exists and that the manufacturer wants to remain on the QPL or requalify. If during two consecutive reporting periods there has been no production, the manufacturer may be required, at the discretion of the qualifying activity, to submit a representative printed wiring board of each base material type qualified to testing in accordance with the qualification inspection requirements. Failure to communicate with the qualifying activity within 60 days after the end of the 12-month reporting period may result in loss of qualification. In addition, the manufacturer shall notify the qualifying activity in accordance with A.4.7.1.4, at any time during the 12-month reporting period, that the group B inspection data indicates failure of the qualified product to meet the performance requirements of this appendix.

A.4.5.5.1 Requalification (see A.6.3.2). Qualifications expire 36 months from the date of qualification. In order to maintain a QPL listing, manufacturers shall complete requalification before the end of its current 36-month qualification period.

A.4.5.5.2 Product assurance procedures. The manufacturer shall make available to the qualifying activity an approved quality manual or procedures that, as a minimum, addresses the following information:

a. In-process (table A–III) and group A (table A–IV) verification procedures. If applicable, group B (table A–V) verification procedures when group B testing is preformed at the manufacturing location.

b. Test coupon design, quantity on a panel, panel placement, strip identification scheme, and usage procedures for the different design standards used for printed boards manufactured (see appendix D).

c. Procedures detailing the method used to select group B samples (definition of complexity, see A.7.2) and, when applicable, for providing design details when group B verification testing is preformed externally by a certified suitable laboratory.

Product assurance procedures that reflect the changes in this specification shall be made available to the qualifying activity prior to the end of the document and process conversion grace period. Unless otherwise specified by the qualifying activity, a copy of the most recent product assurance procedures shall be submitted with each qualification or re-qualification.

A.4.6 Inspection of product for delivery. Inspection of product for delivery shall consist of in-process and group A inspection. Except as specified in A.4.7.1.4, delivery of printed wiring boards which have passed in-process and group A inspection shall not be delayed pending the results of the periodic inspection. Anomalies or defects noted on sample printed wiring boards or test coupons (or both) defined herein shall be recorded and the proper corrective action shall be initiated. Manufacturers that are qualified to use contract services (see A.4.5.3.3) are still responsible for in-process and group A inspections and shall be subject to loss of qualification for failure to complete the in-process and group A inspections.

A.4.6.1 In-process inspection. Each inspection lot of printed wiring boards or panels, as applicable, shall be inspected in accordance with table A–III. When permanent solder resist is specified (see A.3.1.1), the in-process inspections specified in subgroups 1, 2, and 3 of table A–III shall be performed prior to solder resist application. Prior to lamination of type 3 printed wiring boards, the in-process inspections specified in subgroup 2 of table A–III shall be performed.

TABLE A–III. In-process inspection.

Inspection	Requirement paragraph	Method paragraph	Sample size 1/
Subgroup 1			
Material	A.3.4	A.4.8.1	See A.4.6.1.4
Cleanliness 2/	A.3.7.3.1	A.4.8.3.1	Plan BN or TL
Subgroup 2			
Conductor spacing 2/ 3/	A.3.5.2.2	A.4.8.1	Plan BH
Conductor width 2/ 3/	A.3.5.2.3	A.4.8.1	Plan BH
Conductor pattern imperfections	A.3.5.2.4	A.4.8.1	Plan BH
Subgroup 3			
Plating adhesion 2/ 4/	A.3.7.4.3	A.4.8.4.3	Plan BH

1/ See appendix C, table C–I for C = 0 sampling plans.
2/ Performed prior to solder resist application.
3/ Performed prior to lamination on each production lot.
4/ A non-reflowed test coupon prior to reflow may be required (see A.6.2).

A.4.6.1.1 Inspection lot.

A.4.6.1.1.1 Subgroup 1. An inspection lot shall correspond to each production lot or each change of shift of work force, whichever occurs first. Production lots may be grouped based on same materials, same type or types of interfacial connections and terminations, and same processing requirements.

A.4.6.1.1.2 Subgroups 2 and 3. An inspection lot shall consist of the number of printed wiring boards fabricated from the same materials, using the same processing procedures, produced under the same conditions within a maximum period of 1 month and offered for inspection at one time.

A.4.6.1.2 Sample size. The number of printed wiring boards or panels to be selected from each inspection lot shall be in accordance with table A–III.

A.4.6.1.3 Rejected lots. If an inspection lot is rejected as a result of a failure to pass the subgroup 1 tests specified, the manufacturer shall withdraw the lot, take corrective action in connection with the cleaning materials and procedures, reclean the lot prior to application of permanent solder resist coating, and resubmit the lot for inspection. Printed wiring boards are not acceptable if the permanent solder resist coating has been applied to a contaminated surface. If an inspection lot is rejected for subgroup 2 or 3 tests, the manufacturer may screen (100 percent inspection) out the defective units (printed wiring boards or panels). Defective printed wiring boards shall not be shipped.

A.4.6.1.4 Materials inspection. Materials inspection shall consist of certification supported by verifying data that the materials used in fabricating the printed wiring boards are in accordance with the applicable referenced specifications or requirements specified (see A.3.1.1), prior to such fabrication. Unless otherwise specified (see A.3.1.1), verifying data need not be submitted to the qualifying activity or acquiring activity, but shall be made available upon request.

A.4.6.2 Group A inspection. Group A inspection shall consist of the inspections specified in table A–IV. The qualified manufacturer shall be responsible for completion of all group A inspections and shall be subject to loss of qualification for failure to complete all group A tests and inspections.

A.4.6.2.1 Inspection lot. A group A inspection lot shall consist of the number of printed wiring boards fabricated from the same materials, using the same processing procedures, produced under the same conditions within a maximum period of 1 month and offered for inspection at one time.

A.4.6.2.2 Sampling procedures. Statistical sampling and inspection shall be in accordance with appendix C. For 100 percent inspection, all rejected units (printed wiring boards or panels of printed wiring boards) shall not be supplied on the contract. The following details on panel/test coupon sampling shall apply:

a. As received (see A.3.7.2.1):

   (1) Types 1 and 2: The number of test coupons to be microsectioned shall be based on a statistical sample of panels in the lot in accordance with appendix C, table C–I, series L.

   (2) Type 3: One test coupon per panel shall be microsectioned and inspected (see A.4.6.2.2.d). The orientation of the section shall be orthogonal to the "thermal stress" microsection.

b. Solderabilty (see A.3.7.4.5): For printed wiring board using only surface mount (SMT) components, the surface solderability test can be used in lieu of the hole solderability test. For mixed component designs (both SMT and through hole attachment), unless otherwise specified, only the hole solderability test shall be performed.

   (1) For sequential electrochemical reduction analysis (SERA), samples shall be selected in accordance with appendix E.

   (2) For J-STD-003, class 3, the samples shall be selected in accordance with table A–IV and appendix C, table C–I, series L. A minimum of 30 holes need to be tested and inspected to comply with the requirements of J-STD-003.

c. Thermal stress (see A.3.7.4.8).

(1) Type 1: The number of test coupons to be tested and inspected shall be based on a statistical sample of panels in the lot in accordance with appendix C, table C–I, series L.

(2) Type 2: The number of test coupons to be tested and microsectioned shall be based on a statistical sample of panels in the lot in accordance with appendix C, table C–I, series J.

(3) Type 3: A minimum of two test coupons (one A and one B) per panel shall be microsectioned and inspected. One of the test coupons shall be microsectioned in the panel's length direction and the other shall be microsectioned along the panel's width direction.

d. Registration (method II, type 3 only): When method II is to be used, registration shall be evaluated using any combination of two microsectioned test specimens taken from diagonal corners of the panel. Both test coupons shall have been microsectioned in the vertical plane with one test coupon representing the panel's length (X) direction and the other representing the panel's width (Y) direction. Test coupons from the "as received" (see A.3.7.2.1) or "thermal stress" (see A.3.7.4.8) verifications may be used.

NOTE: Concerning type 3 "as received" and "thermal stress" microsections, a minimum of two test coupons (one A and one B) per panel shall be microsectioned. One of the test coupons shall be microsectioned in the panel's length direction and the other shall be microsectioned along the panel's width direction. One of the test coupons shall represent the "as received" condition and the other the after "thermal stress" condition.

A.4.6.2.3 Rejected lots. If an inspection lot is rejected, the manufacturer may rework it to correct the defects and resubmit the lot for reinspection, or screen out the defective units (if possible). Resubmitted lots shall be inspected using tightened inspection (see appendix C). Such lots (reworked or screened) shall be clearly identified as reinspected lots. Products which have failed any group A inspection herein and have not been reworked and have not passed reinspection (as specified in this appendix) may not be delivered as compliant printed wiring boards.

A.4.6.2.4 Disposition of sample units. Sample printed wiring boards which have passed all of group A inspection herein may be delivered if the inspection lot is accepted.

TABLE A–IV. Group A inspection.

Inspection	Requirement paragraph	Method paragraph	Test specimen 1/			Sample plans 2/
			T1	T2	T3	
Visual and dimensional						
Acceptability 3/ 4/	A.3.7.1	A.4.8.1	PWB	PWB	PWB	Plan BH 3/ 4/
Registration, external	A.3.5.6	A.4.8.1.3	5/	5/		Plan TJ see 6/
Microsection						
As received	A.3.7.2.1	A.4.8.2		B	A or B	See 6/
Registration, internal	A.3.7.2.2.1	A.4.8.2.4				See 6/ and 7/
Chemical						
Resistance to solvents	A.3.7.3.2	A.4.8.3.2	8/	8/	8/	See 8/
Physical						
Bow and twist	A.3.7.4.1	A.4.8.4.1	PWB	PWB	PWB	Plan BH
Conductor edge outgrowth	A.3.7.4.2	A.4.8.4.2	PWB	PWB	PWB	Plan BH
Plating adhesion	A.3.7.4.3	A.4.8.4.3	PWB	C	C	Plan BH/TJ 3/ 9/
Solderability 6/ 9/						
Hole	A.3.7.4.5.1	A.4.8.4.5.1		A or S	A or S	See 6/ & 10/
Surface	A.3.7.4.5.2	A.4.8.4.5.2	PWB	C	C	Plan BH/TJ 6/ 11/
Solder resist adhesion	A.3.7.4.6.2	A.4.8.4.6			G	Plan TJ
Thermal stress	A.3.7.4.8	A.4.8.4.8		B	A & B	See 6/
Electrical						
Circuit continuity	A.3.7.5.1	A.4.8.5.1	PWB	PWB	PWB	100 percent 12/
Circuit shorts	A.3.7.5.2	A.4.8.5.2	PWB	PWB	PWB	100 percent 12/

1/ T1 designates a type 1 design; T2 designates a type 2 design; T3 designates a type 3 design; and PWB means inspect the entire board, whereas an individual test coupon designation means inspect the specified test coupon. See appendix D herein for test coupon identification (name) translation to the applicable design standard.
2/ See appendix C, table C–I for C = 0 sampling plans and C.4.5 for examples.
3/ Some attributes may need to be inspected prior to lamination or solder resist application.
4/ The solder resist thickness test can be performed on either a test coupon at a sampling of TJ or production printed wiring board at a sampling of BH, manufacturer's option.
5/ Test coupon or production printed wiring board, manufacturer’s option.
6/ See A.4.6.2.2 for sample size and test specimen description.
7/ Optional method by designated registration test coupons (method III), see A.4.8.2.4.2 for test specimen description and sample size.
8/ See A.4.8.3.2.1 for test specimen description and sample size.
9/ This inspection does not need to be performed on solder coated printed boards.
10/ A or S test coupon, manufacturer’s option.
11/ For printed wiring boards using only surface mount lands for component attachment, the surface solderability test can be used in lieu of the hole solderability test.
12/ Type 2 and 3 printed wiring boards only.

A.4.7 Periodic conformance inspection. Periodic conformance inspection shall consist of group B inspection. Except where these inspections show noncompliance with the applicable requirements (see A.4.7.1.4), delivery of printed wiring boards which have passed in-process and group A inspection shall not be delayed pending the results of these periodic inspections. Periodic inspections shall be performed at a certified suitable laboratory (see A.6.5).

A.4.7.1 Group B inspection. Group B inspection shall consist of the tests specified in table A–V. All tests in subgroup 1 tests shall be performed. Tests in subgroup 2 are dependant on printed wiring board construction techniques and if compliance testing was performed during group A.

A.4.7.1.1 Inspection lot. The sample units shall be randomly selected from an inspection lot or lots that have passed all in-process and group A inspections during that production month (i.e., the group B reporting period). The most complex printed wiring boards shall be as determined by the manufacturer using its definition of complex (see A.7.2), subject to approval by the qualifying activity. If all the inspections in table A–V cannot be performed on the most complex lot of the month, additional sample units from other designs shall be submitted if they address the technology to be verified.

A.4.7.1.2 Sampling procedures. Samples for each base material type groupings (see A.4.5.4.2) produced during that reporting period shall be subjected to group B inspection. The extent of qualification of types allowed by A.4.5.4.1 shall apply. The following criteria shall be used in selecting samples for group B testing:

a. Rework simulation and MIR. The sample units shall be from the most complex (see A.7.2) printed wiring board design produced that calendar month. Because of the performance nature of this document, the design details of the test coupons or the printed boards that they represent shall be supplied with the sample units so that proper verification can be confirmed (see A.6.7). The sample units can be either:

   (1) Two sets of quality conformance test circuitry, or

   (2) Two test coupons for each test to be performed.

b. Surface peel strength. When multiple lots using foil lamination are available, a minimum of eight peel strength specimens shall be selected from at least two different production lots; a maximum of four from each lot or 100 percent if the number of coupons available is less than four for a production lot. If only one foil laminated lot is available for a calendar month, then only the test coupon(s) from that lot shall be submitted for testing.

c. Resistance to solvents. The test specimens can be either whole or parts of production printed wiring boards or quality conformance test circuitry strip identification areas containing ink or paint marking. The minimum number of samples shall be at least one sample for each solution specified by the applicable test method (i.e., one sample for each solution required).

Example: The most complex lot using FR-4 base material did not use ink or paint marking, foil lamination construction, and was a surface mount only design. However, other compliant lots constructed that month of legacy types GF and GH base materials (within the same base material grouping) did use ink or paint marking, foil lamination, and though-hole mounting. The group B inspection lot for that month shall contain samples from more than one design (or part number) or lot of printed board design in order to comply. The exact breakdown of 5 different part numbers for the group B submission could be as follows:

(1) Part number “A” for the MIR–DWV test, the most complex design of the month. Although part number “A” it is a SMT only design with no component size holes, it still can and must be used because the test coupon hole size is determined by IPC-2221 for SMT designs.

(2) Part numbers “B” and “D” for surface peel strength testing.

(3) Part number “C” for rework simulation testing. Part number “C” is the third most complex design produced that month, but it is the most complex design using component holes.

(4) Part numbers “B”, “D”, and “E” for resistance to solvents testing since this test is not being preformed during group A on a lot–to–lot basis.

A.4.7.1.3 Frequency. The frequency of selecting sample units and performing group B testing shall be on a monthly basis. The sample units shall be submitted for testing within 30 calendar days after the end of each reporting period.

A.4.7.1.4 Failures. If one or more sample units fail to pass group B inspection, the sample shall be considered to have failed. The qualifying activity shall be notified of any group B failure within 3 business days. Group B inspection shall be repeated on additional sample units (either all group B inspections or just the group B inspection which the original sample failed, at the option of the qualifying activity) from the next most complex (see A.7.2) inspection lot from the same month that the failure occurred. Group A testing and shipment of the product represented by the failed group B sample shall be discontinued.

A.4.7.1.4.1 Corrective actions. Corrective actions shall be taken on the materials or processes, or both, as warranted, and on all units of product which can be corrected and which were manufactured under essentially the same conditions (materials, processes, etc.), and which are considered subject to the same failure.

A.4.7.1.4.2 Noncompliance. If the lot or lots directly represented by the group B failure have been shipped, the manufacturer shall notify the acquiring activity of the failure and shall recall the affected lot or lots for reinspection, if possible. All other lots represented by extension of qualification by the failed group B sample are considered noncompliant until a sample from the next most complex (see A.7.2) inspection lot passes group B inspection.

A.4.7.1.4.3 Reinstitution of group A inspection. After successful completion of group B reinspection, group A inspection of product represented by the group B failure may be reinstituted.

A.4.7.1.5 Disposition of sample units. Test coupons which have been subjected to group B shall be retained as specified in A.3.9.

TABLE A–V. Group B inspection.

Inspection	Requirement paragraph	Method paragraph	Test coupon by type 1/ 2/		
			Type 1	Type 2	Type 3
Subgroup 1					
Rework simulation	A.3.7.4.4	A.4.8.4.4	3/	3/	3/
Moisture and insulation resistance	A.3.7.6.1	A.4.8.6.1	E	E	E
Dielectric withstanding voltage 4/	A.3.7.5.3	A.4.8.5.3	4/	4/	4/
Subgroup 2					
Resistance to solvents 5/	A.3.7.3.2	A.4.8.3.2	5/	5/	5/
Surface peel strength	A.3.7.4.7	A.4.8.4.7			N 6/

1/ See 1.2, A.3.1.1, and A.7.2 herein.
2/ See appendix D for test coupon identification letter translation to the applicable design standard.
3/ The holes to be tested and inspected shall represent component holes used for through–hole mounting.
4/ Dielectric withstanding voltage shall be performed after the moisture and insulation resistance test on the same test coupon subjected to the moisture and insulation resistance test.
5/ See A.4.8.3.2.1 for test specimen description and number of samples required.
6/ Test coupon N minimum length shall be 2 inches (50.8 mm). A minimum of eight test specimens shall be inspected. If two or more lots are produced, four test specimens from two lots shall be selected.

A.4.8 Methods of inspection. The following identified tests and test methods are used to assure printed wiring board integrity within typical operating conditions. Alternate commercial or industry standard test methods may be allowed; however, if an alternate method is to be used, the qualifying activity shall be notified prior to the performance of the test. The following verification test methods described herein are proven methods and shall be the referee method in case of dispute.

A.4.8.1 Acceptability inspection. The visual and dimensional features of the printed wiring board test specimen shall be inspected using test method numbers 2.2.1 and 2.2.2 of IPC-TM-650, as applicable. Referee inspection needed to confirm a suspected defect of the test specimen features shall be accomplished at a magnification of up to 30X, as applicable to confirm the suspected defect.

A.4.8.1.1 Annular ring, external (see A.3.5.2.1). The measurement of the annular ring on external layers is from the inside surface (within the hole) of the plated hole or unsupported hole to the outer edge of the annular ring on the surface of the printed wiring board. See figure A–1 for illustration.

A.4.8.1.2 Overall printed board thickness (see A.3.5.3). Unless otherwise specified, the overall printed board thickness measurement shall be inspected by any micrometer or by microsection in accordance with A.4.8.2.

A.4.8.1.2.1 With edge-board contacts. Printed boards with edge-board contacts shall have the overall thickness measured across the board on the final finish plated surfaces of opposite contacts.

A.4.8.1.2.2 Without edge-board contacts. Printed boards without edge-board contacts shall have the overall thickness measured across the board from plated copper surface to plated copper surface not including the final finish plating.

A.4.8.1.3 Registration (method I) (types 1 and 2) (see A.3.5.6). Registration of type 1 and type 2 printed wiring boards shall be satisfied if the outer layers meet the external annular ring (see A.3.1.1 and A.3.5.2.1) and hole pattern accuracy (see A.3.1.1 and A.3.5.4) requirements.

A.4.8.1.4 Solder resist thickness (see A.3.5.7). Solder resist thickness shall be inspected by any micrometer or by microsection in accordance with A.4.8.2.

A.4.8.1.5 Workmanship. The printed board specimen shall be inspected in accordance with test method number 2.1.8 of IPC-TM-650, except that the magnification shall be 1.75x (3 diopters), minimum.

A.4.8.2 Microsection inspection.

A.4.8.2.1 Microsection preparation. Microsection preparation shall be accomplished by using methods in accordance with either test method numbers 2.1.1 or 2.1.1.2 of IPC-TM-650. Automatic microsectioning techniques may be used in lieu of test methods 2.1.1 or 2.1.1.2 of IPC-TM-650 (see A.6.10). The following details shall apply:

a. Number of holes per specimen. A minimum of at least three plated holes cross sectioned vertically shall be made for each test specimen required. Each side of the three plated holes shall be viewed independently.

b. Accuracy. All three plated holes of each test specimen shall be sectioned, ground, and polished to within ±10 percent of the center of the drilled diameter of the hole.

c. Pre microetch evaluations. The specimens shall be evaluated for plating separations, superfulous copper, and wicking prior to microetching (see A.6.11).

d. When more than two test specimens are contained in a mount (coupon–stacking or gang mounting), the following shall apply:

   (1) The test specimens shall not be in direct contact any other specimen in the mount. The recommended minimum distance between test specimens in a mount is .010 inch (0.025 mm).

   (2) The traceability requirements of A.3.9.1 shall apply.

A.4.8.2.2 Microsection examination and inspection. Microsection examination and inspection shall be accomplished in accordance with test method number 2.2.5 of IPC-TM-650 to evaluate characteristics such as dielectric spacing, etchback, plating thickness, foil thickness, etc., in plated holes. If more than three plated holes are on a test specimen, all holes shall be evaluated. The following details shall apply:

a. Magnifications. Unless otherwise specified in test method number 2.2.5 of IPC-TM-650, the test specimens shall be inspected at a magnification of 100X ±5 percent. Referee inspections shall be accomplished at a magnification of 200X ±5 percent.

b. Evaluations. Pre and post microetch evaluations for the criteria of A.3.6 shall be accomplished at magnifications specified above. The specimens shall be evaluated for plating separations, superfulous copper, and wicking prior to microetching (see A.6.11)

c. Measurements. Measurements shall be averaged from at least three determinations for each side of the plated hole. Isolated thick or thin sections shall not be used for averaging; however, isolated areas of reduced copper thickness shall be measured and evaluated to the copper plating void rejection criteria specified in A.3.6.9.3.1.

A.4.8.2.3 Plated hole inspection (see A.3.6). When plated holes are inspected in accordance with A.4.8.2.2, the following details shall apply:

a. Annular ring (internal) (see A.3.6.1). The measurement of the annular ring on internal layers is from the inside drilled surface (within the hole) of the plated hole or unsupported hole to the outer edge of land (see figure A-5). This measurement shall apply to all internal lands for all three holes.

b. Dielectric layer thickness (see A.3.6.4). The dielectric layer thickness shall be inspected between all conductor layers present in the test specimen.

c. Metal foil thickness (see A.3.6.2). The external and internal metal foil thickness shall be inspected on all conductor layers present in the test specimen.

d. Plating and coating thickness (see A.3.6.9). Isolated thick or thin sections shall not be used for averaging. However, isolated areas of reduced copper thickness shall be measured for compliance with the requirements of A.3.6.9.

e. Copper plating voids (see A.3.6.9.3.1). Any plated hole in the microsection failing the plating void criteria of A.3.6.9.3.1 subparagraphs a, b, or c, shall be cause for the entire panel of printed wiring boards associated with the microsection to be rejected. The following details apply if a single plating void is found:

(1) Type 2: If the plating void does not exceed the conditions of A.3.6.9.3.1, the entire lot (100-percent panel inspection) shall have test specimens from each panel microsectioned and inspected for voids. If a plating void is present in any microsection mount representing a panel, a referee microsection shall be performed using an A or B test coupon from the opposite corner of that panel. If the referee has no plating voids, that panel is acceptable, however, if a plating void is present in that microsection, that panel of printed wiring boards shall be rejected.

(2) Type 3: If the plating void does not exceed the conditions of A.3.6.9.3.1, a referee microsection shall be performed using an A or B test coupon from the opposite corner of the panel. If the referee has no plating voids, the panel is acceptable, however, if a plating void is present in that microsection, that panel of printed wiring boards shall be rejected.

f. Heatsink planes (see A.3.6.4.1 and figure A–7). The lateral dielectric spacing between the heatsink planes and adjacent conducting surfaces, nonfunctional lands, or plated-through holes shall be measured at the closest point between these surfaces.

A.4.8.2.4 Registration. Registration shall be determined by either evaluating microsectioned test coupons (method II, see A.4.8.2.4.1) or by evaluating of special registration coupons when provided (method III, see A.4.8.2.4.2).

A.4.8.2.4.1 Method II (by microsectioned sample units). Registration shall be evaluated using the internal annular ring measurement. Two test specimens (any combination of the “as received” (see A.3.7.2.1) and “thermal stress” (see A.3.7.4.8) microsections) from diagonally opposing panel corners shall be inspected. Both test specimens shall have been microsectioned in the vertical plane with one test coupon representing the panel's length (X axis) direction and the other representing the panel's width (Y axis) direction.

A.4.8.2.4.2 Method III (optional) (by registration test coupons). Registration test coupons and techniques, when provided by the printed wiring board fabricator, shall be evaluated in accordance with methods approved by the qualifying activity and when applicable, the acquiring activity. Unapproved methods of measurement using registration test coupons shall be backed up by method II of A.4.8.2.4.1 using the appropriate test coupons (see table A-IV) from the same panel. Two non-destructive methods for determining registration are available using the following test coupon designs:

a. Test coupon F (etch factor not needed).

b. Test coupon R (etch factor of each layer needed).

If other registration test coupon designs and requirements are provided as an element of the design documentation set, registration can be evaluated in accordance with the criteria specified on the applicable master drawing.

A.4.8.3 Chemical inspection.

A.4.8.3.1 Cleanliness (by resistance of solvent extract) (see A.3.7.3.1 and A.6.4). The printed wiring board shall be tested for cleanliness in accordance with test method number 2.3.25 of IPC-TM-650. Other alternate test methods not specified in A.6.4 may be used in lieu of test method number 2.3.25 of IPC-TM-650 only when specifically approved by the Government acquisition activity. Such approval shall be determined on the basis that the alternate test method is demonstrated to have equal or better sensitivity and employs solvents with the ability to dissolve flux residue as does the alcohol-water solutions specified in test method number 2.3.25 of IPC-TM-650.

A.4.8.3.2 Resistance to solvents (marking ink or paint) (see A.3.7.3.2). Marking ink or paint resistance to solvents shall be tested in accordance with test method number 2.3.4 of IPC-TM-650. The following details apply:

a. The marked portion of the test specimen shall be brushed.

b. After the test, the test specimen shall be visually inspected in accordance with A.4.8.1 for legibility of marking and the requirements of A.3.7.3.2.

A.4.8.3.2.1 Sampling procedures and test specimens. The resistance to solvents test shall be performed either during group A (every lot) or during group B (monthly). The test specimens can be either production printed wiring boards or quality conformance test circuitry strip identification areas containing ink or paint marking. The minimum number of samples shall be at least one sample for each solution specified by the applicable test method (i.e., one sample for each solution required).

A.4.8.4 Physical inspections.

A.4.8.4.1 Bow and twist (see A.3.7.4.1). The printed wiring board shall be inspected for bow and twist in accordance with test method number 2.4.22 of IPC-TM-650.

A.4.8.4.2 Conductor edge outgrowth (see A.3.7.4.2). The extent of outgrowth, on conductors covered with metals other than fused tin-lead or solder coating, shall be determined by measuring the conductor width before and after mechanically removing the overhang metal. If a referee test is required, cross-sectioning of the conductor shall be performed. The procedure for removing overhang metal, for this test, shall be as follows:

a. Wet the printed wiring board specimen in tap water at approximately room temperature.

b. While wet, brush the printed wiring board specimen with a brass wire brush to remove the overhang metal. Brush in the direction of the functional line, using moderate pressure.

A.4.8.4.3 Plating adhesion (see A.3.7.4.3). The printed wiring board shall be tested in accordance with test method number 2.4.1 of IPC-TM-650, with the following details and exceptions. When edge-board contacts are part of the pattern, at least one pull shall be on the contacts. Fresh tape shall be used for each pull. If overhang metal breaks off (slivers) and adheres to the tape, it is evidence of outgrowth (see A.3.7.4.2), but not a plating adhesion failure.

A.4.8.4.4 Rework simulation.

A.4.8.4.4.1 Unsupported hole (see A.3.7.4.4.1). The printed wiring board test specimen holes shall be tested in accordance with test method number 2.4.21 of IPC-TM-650 with the following details and exceptions: Three holes per test coupon shall be tested. Insert wires in holes in selected lands and solder to lands by machine or hand, as applicable. The insert wire lead shall have a diameter so that the diameter of the hole will be at a maximum of .020 inch (0.51 mm) greater than the diameter of the inserted wire lead. The wires shall not be clinched. It shall be considered a failure when a land around an unsupported hole is loosened.

A.4.8.4.4.2 Plated through hole (see A.3.7.4.4.2). The printed wiring board test specimen plated-through holes shall be tested in accordance with test method number 2.4.36 of IPC-TM-650, except that the rework simulation shall be performed after stabilizing the test coupons at temperatures of 15 degrees Celsius to 35 degrees Celsius and relative humidity of 40 to 85 percent for a period of 24 hours.

A.4.8.4.5 Solderability (see A.3.7.4.5).

A.4.8.4.5.1 Hole (plated-through hole) (see A.3.7.4.5.1). The printed wiring board test specimens shall be tested and inspected in accordance with J-STD-003, class 3 or appendix E.

A.4.8.4.5.2 Surface or surface mount land (see A.3.7.4.5.2). The printed wiring board test specimens shall be tested and inspected in accordance with J-STD-003, class 3 or appendix E.

A.4.8.4.6 Solder resist adhesion (see A.3.7.4.6). The permanency and adhesion of cured solder resist shall be determined in accordance with test method number 2.4.28.1 of IPC-TM-650.

A.4.8.4.7 Surface peel strength (type 3 using foil lamination) (see A.3.7.4.7). The printed wiring board test specimen shall be tested and inspected in accordance condition A of test method number 2.4.8 of IPC-TM-650. Conditions B and C (after thermal stress and after exposure to processing chemicals) shall not be performed. Plated tin-lead, solder coating, or other plated metallic resist shall be chemically removed prior to test or shall be prevented from being deposited during manufacturing. The test specimen shall not be coated with any organic coating for test. All peel strength readings obtained shall meet the minimum requirement.

A.4.8.4.7.1 Test specimens. The specimen shall consist of conductors that provide a minimum test length of 2 inches (50.8 mm) and a conductor width of .125 inch (3.3 mm). NOTE: This test coupon is described in the default design standard (test coupon "N") or number 5.8.3 of IPC-TM-650. At least one test coupon per foil laminated side shall be placed on the production panel where space is available.

A.4.8.4.8 Thermal stress (see A.3.7.4.8).

A.4.8.4.8.1 Type 1 (see A.3.7.4.8.1). The printed wiring board test specimen shall be tested in accordance with test method number 2.6.8 of IPC-TM-650 except that post evaluation microsectioning is not required.

A.4.8.4.8.2 Types 2 and 3 (see A.3.7.4.8.2). The printed wiring board test specimen shall be tested in accordance with test method number 2.6.8 of IPC-TM-650. The following details shall apply.

a. Test specimens constructed of thermoset resin base materials shall be subjected to test condition A.

b. Test specimens constructed of aramid reinforced thermoset resin base materials shall be subjected to test condition B. Test specimens constructed of thermoplastic resin base materials shall be subjected to test condition C.

A.4.8.5 Electrical inspection.

A.4.8.5.1 Circuit continuity (see A.3.7.5.1). A current shall be passed through each net by applying electrodes on the terminals at each end of the net. The current passed through the net shall not exceed those specified in the applicable design standard (see A.3.1.1 and appendix D) for the smallest conductor in the circuit. See IPC-9252 for additional guidelines.

A.4.8.5.2 Circuit shorts (isolation resistance) (see A.3.7.5.2). A test voltage shall be applied between each net and all other nets that are adjacent to the net under test. The voltage shall be applied between nets of each layer and the electrically isolated net of each adjacent layer. For manual testing, the voltage shall be 200 volts minimum and shall be applied for a minimum of 5 seconds. When automated test equipment is used, the minimum applied test voltage shall be as specified on the applicable master drawing. If a test voltage of the printed wiring board is not specified on the applicable master drawing, the test voltage shall be the maximum rated voltage of the net being tested. If no maximum rated voltage is specified, the minimum test voltage shall be 40 volts.

A.4.8.5.3 Dielectric withstanding voltage (see A.3.7.5.3). The printed wiring board test specimen shall be tested in accordance with test method number 2.5.7 of IPC-TM-650, test condition B. The following details and exceptions apply:

a. Test specimen: The test specimen shall be as identified in tables A–II or A–V and shall been subjected to the moisture and insulation resistance test.

b. Test specimen preparation: This portion of the test shall be skipped.

c. Points of application: The dielectric withstanding voltage shall be applied between all common portions of each conductor pattern and all adjacent common portions of each conductor pattern. The voltage shall be applied between conductor patterns of each layer and the electrically isolated pattern of each adjacent layer.

A.4.8.6 Environmental inspection.

A.4.8.6.1 Moisture and insulation resistance (MIR) (see A.3.7.6.1.1). The printed wiring board test specimen shall be tested in accordance with test method number 2.6.3 of IPC-TM-650, class 3, test specimen preparation method A (with conformal coating). The initial and final resistance measurements shall be taken at 500 volts direct current (+25 volts direct current, –0 volts direct current).

A.4.8.6.1.1 Flush conductor printed boards (see A.3.7.6.1.2). The test specimens shall be inspected in accordance with A.4.8.6.1, except the insulation resistance measurement shall be taken within 60 seconds after removal of the test specimen from the humidity chamber and after 100 V direct current, +/– 15 percent has been applied between all conductors for a minimum of 60 seconds.

A.4.8.6.2 Thermal shock (see A.3.7.6.2 and A.4.5.4.2).

A.4.8.6.2.1 Thermoset base materials. The printed wiring board test specimen shall be tested in accordance with test method number 2.6.7.2 of IPC-TM-650, with the following details:

a. Test specimen: See table A–II.

b. Test condition: D, E, or F, see A.4.5.4.2.

c. Maximum change in resistance: 10 percent.

A.4.8.6.2.2 Thermoplastic base materials. The printed wiring board test specimen shall be tested in accordance with test method number 2.6.7 of IPC-TM-650, test condition B, with the following details:

a. Test specimen: See table A–II.

b. Maximum change in resistance: 15 percent.

A.5. PACKAGING

A.5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see A.6.2). When actual packaging of materiel is to be performed by DoD or in house personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activity within the Military Service or Defense Agency, or within the Military Service’s system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

A.6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory.)

A.6.1 Intended use. This appendix is intended to be used by manufacturers not certified to the QML printed board specification, MIL-PRF-31032. This appendix is not a duplicate or look–alike of any MIL-PRF-31032 specification sheet. Most of the historic performance and verification requirements are still contained in this appendix. However, many of the "enhanced" acceptance criteria or verification methods developed for MIL-PRF-31032 specifications sheet have been added as the baseline or are available as an option using appendix B.

A.6.2 Acquisition requirements.

A.6.2.1 Primary acquisition requirements. Acquisition documents should specify the following:

a. Title, number, revision letter (with any amendment number when applicable), and date of this specification.

b. Appropriate type (see 1.2.1) and base material designations (see 1.2.2).

c. Title, number, revision letter (with any engineering change proposal or notice of revision number when applicable), and date of the applicable master drawing (see A.3.1.1).

d. Title, number, revision letter (with any notice number when applicable), and date of the applicable design standard (see A.3.3).

e. Part identification (if applicable), and marking instructions including size, location, and application method (see A.3.1.1 and A.3.8).

f. Whether microsectioned test specimens, samples or photographs are required to be delivered with the order.

g. Packaging requirements (see A.5.1).

A.6.2.2 Additional acquisition requirements. Acquisition documents should also specify the following data, if applicable:

a. Verification Conformance Inspection option (if other than option 4)(see appendix D).

b. Design related if different than the applicable design standard (see appendix D).

(1) Minimum annular ring (external/internal)(see A.3.1.1), if different than the applicable design standard.

(2) Minimum conductor width (see A.3.1.1), if different than the applicable design standard.

(3) Minimum conductor spacing (see A.3.1.1), if different than the applicable design standard.

(4) Minimum dielectric thickness (see A.3.1.1), if different than the applicable design standard.

(5) Minimum edge spacing requirement (see A.3.1.1), if different than the applicable design standard.

(6) Copper plating thickness (see A.3.1.1), if different than the applicable design standard.

(7) Conductor finish plating (see A.3.1.1), if other than solder coating or tin-lead.

c. Conductor edge outgrowth or overhang, if applicable (see A.3.7.4.2).

d. Circuit shorts (isolation resistance) requirements including minimum applied test voltage (see A.3.7.5.2 and A.4.8.5.2).

e. Surface (foil lamination) peel strength, if applicable (see A.3.7.4.7).

f. Non-delivery of sample units which have not been subjected to electrical testing (circuit continuity and circuit shorts tests) and have passed all other tests to groups A and B inspection.

g. Cleanliness (see A.3.7.3.1 and A.6.4).

h. If special or other identification marking is required (see A.3.8).

A.6.3 Qualification master drawings. Although the qualification test specimen master drawings IPC-100041, IPC-100042, IPC-100043, and IPC-100044 specified in A.2.1.1 specifies the use of rigid base materials compliant to MIL-P-13949, manufacturer's can qualify using base material by specifying the base material on the application for qualification. In addition, the zone C (except for the external conductor traces on test coupon E–5) of the qualification master drawing is required to be present on the qualification test specimen and is to be examined during qualification testing.

A.6.3.1 Transference of qualification. Manufacturers currently qualified to MIL-PRF-55110F will have their qualification transferred to this document. The expiration date of their current qualification will not be changed. Qualifications in process (before the date of this document) will be performed to the requirements MIL-PRF-55110F with amendment 1. New applications for qualification (after the date of this document) will be performed to the requirements of this revision.

A.6.3.2 Qualification expiration and QPL-55110. Qualification listings within QPL-55110 for manufacturers qualified under this appendix (QPL product assurance level) includes the qualification expiration date as the last six digits of the test reference number. This date, formatted as (month/day/year), is the actual qualification expiration date for that listing. This date signifies that the company is no longer qualified (unless notified in writing by the qualifying activity) whether or not that individual listing has been removed the QPL. If the company has not requalified before the next issue of the QPL is published, then the listing will not be included on the updated QPL.

A.6.4 Cleanliness, alternate methods. The following methods of determining the cleanliness of printed wiring boards have been shown to be equivalent to the resistance of solvent extract test method:

a. The Kenco Alloy and Chemical Company, Incorporated, "Omega Meter™, Model 200."

b. Alpha Metals Incorporated, "Ionograph™" (see URL: http://www.scscookson.com).

c. Zero Systems, Incorporated, "Zero Ion™, Model ZI–100"(see URL: http://www.aqueoustech.com).

d. Westek, "ICOM 5000™."

Table A–VI lists the equivalence factors for these methods in terms of microgram equivalents of sodium chloride per unit area.

TABLE A–VI. Equivalence factors.

Method	Equivalence factors	Equivalents of sodium chloride		Related IPC-TM-650 test method
		Micrograms per square inch	Micrograms per square cm	
Resistance of solvent extract (ROSE)	1.00	10.06	1.56	2.3.25
Omega meter™	1.39	14.00	2.20	2.3.25
Ionograph™	2.01	20.00	3.10	2.3.25
Zero ion™	3.68	37.00	5.80	N/A
ICOM 5000™	2.20	22.00	3.40	N/A

A.6.5 Certified suitable laboratories (acceptable to the Government). Government accepted test laboratories are those facilities (either internal to the QPL manufacturer or a separate independent laboratory) that have demonstrated their ability to perform the verification test required by this document. A list of laboratories that have been certified is available at http://www.dscc.dla.mil/offices/sourcing_and_qualification. Search for a document titled “PWB Commercial Lab List (31032/50884/55110)”.

A.6.6 Alternate test methods. Other test methods may be substituted for those specified herein provided it is demonstrated to and approved by the qualifying activity that such a substitution in no way relaxes the requirements of this specification.

A.6.7 Group B sample critical design details. Past versions of this document contained default design details that were assumed to apply to all test coupons subjected to group B inspection, regardless of the master drawing design requirements. With the issuance of this document, the design details which were universally used to determine acceptance or failure of the group B samples, are no longer considered universally applicable to the group B test coupons. The printed wiring board design details (plating thickness, dielectric separation, external, and internal annular ring, etc.) or the default design standard that applies to the test coupons, should be submitted along with test coupons so that a proper group B evaluation of the design can be verified.

EXAMPLE: The master drawing of the most complex design selected for group B testing requires .0015 inch (0.038 mm) of copper plating thickness, .006 inch (0.15 mm) of dielectric spacing, and .003 inch (0.076 mm) internal annular ring. These design details are considerably different than the baseline design parameters found in IPC-2221. If on these same samples, the certified suitable laboratory found that the samples exhibited .001 inch (0.025 mm) of copper plating thickness, .005 inch (0.13 mm) of dielectric spacing and .002 inch (0.051 mm) internal annular ring, the manufacturer or certified suitable laboratory could not claim, state, or certify that the results of group B testing or the samples met the master drawing or specification requirements.

A.6.8 Tin finishes (see A.3.4.2). The use of alloys with tin content greater than 97 percent may exhibit tin whisker growth problems after manufacture. Tin whiskers may occur anytime from a day to years after manufacture, and can develop under typical operating conditions on products that use such materials. Tin whisker growth could adversely affect the operation of electronic equipment systems. Conformal coatings applied over top of a whisker-prone surface will not prevent the formation of tin whiskers. Alloys of 3 percent lead have shown to inhibit the growth of tin whiskers. For additional information on this matter refer to ASTM B545.

A.6.9 DSCC Form 19W. Copies of DSCC Form 19W, “PWB-QPL Application/Authorization to Test" may be obtained at http://www.dscc.dla.mil/offices/sourcing_and_qualification/ or upon application to DSCC–VQE, PO Box 3990, Columbus, OH 43218-3990.

A.6.10 Alternate microsection preparation procedure guidelines. IPC–MS–810 “Guidelines for High Volume Microsection” contains many recommendations and suggestions that can be helpful in preparing microsection mounts containing multiple test specimens.

A.6.11 Microsection mount microetch caution. Prior to microetching, if lines are visible in the areas of inner layer to hole wall interfaces, care should be taken to not over-etch the mount so that the various plating layers will still be visible in the etched mount. This will enable accurate determination as to whether the line is separation or a polishing artifact.

A.7. DEFINITIONS

A.7.1 Board thickness. The overall printed wiring board thickness includes metallic depositions, fusing, and solder resist. The overall thickness is measured across the printed wiring board extremities (thickest part), unless a critical area, such an edge-board contacts or card guide mounting location, is identified on the master drawing.

A.7.2 Complex (as related to group B testing). Complexity of printed wiring boards will usually depend on the base materials used; dielectric layer thickness; overall printed wiring board thickness; number of conductor layers; conductor widths and spacings; intricacy of patterns; size, quantity, aspect ratio and positioning of plated holes; tolerancing of any or all of the above; the presence of internal heatsink planes or thermal planes, and all combinations of the above with respect to their manufacturing difficulty, and their effects upon the consistent ability of the printed wiring boards to meet the requirements of the periodic testing, unless otherwise specified by the contracting activity.

A.7.3 Conductive interfaces. The term conductive interfaces is used to describe the junction between the hole wall plating or coating and the surfaces of internal and external layers of metal foil. The interface between platings and coating (electroless copper, direct metallization copper and non-electroless electroless copper substitutes, etc., and electrolytic copper, whether panel or pattern plated), are also considered a conductive interface.

A.7.3.1 External conductive interfaces. An external conductive interface is considered to be the junction between the surface copper foil and the deposited or plated copper.

A.7.3.2 Internal conductive interfaces. An internal conductive interface is considered to be the junction between the internal layers (copper foil posts or internal layers) and the deposited or plated copper.

A.7.4 Contract service. Contract services are those services contracted or performed (or both) outside the qualified manufacturer's immediate facility, not to include verification testing or electrical function tests. For the purposes of this appendix, the internal equipment/process condition applies only to those processes used to manufacture the qualification test specimen. When applying for qualification of contracted services, the process to be subcontracted and the company performing the contracted service shall be identified.

A.7.4.1 Mass lamination. Manufacturers requesting to use contract services lamination (mass lamination) will be qualified to type 3 of the same base material type requested. The qualification test specimens and sample size will be as specified in A.4.5.2.1. The qualification test specimens will be produced by the QPL manufacturer and the mass laminator and should be representative of the subsequent production process. Printed wiring board manufacturers using contract services are subject to the conditions of A.4.5.3.3.

A.7.5 Printed wiring board test specimen. The term printed wiring board test specimen is used to describe all of the following; production printed wiring boards, qualification test specimens, or test coupons.

A.7.6 Resin systems families.

A.7.6.1 Thermoset resin. For the purposes of this document, base materials conforming to the following legacy type designators are classified as containing thermosetting resins: AF, BF, AI, BI, GB, GC, GF, GH, GI, GM, QI, and SC.

A.7.6.2 Thermoplastic resin. For the purposes of this document, base material conforming to the following legacy type designators are classified as containing thermoplastic resin: GR, GP, GT, GX, and GY.

A.7.7 Printed board thickness. See “board thickness”.

A.7.8 Quality–conformance test circuitry (QCTC). See IPC-T-50.

A.7.9 As received (microsection inspection). As received means after tin alloy plating is reflowed or fused or after solder coating but prior to thermal stress, rework simulation, or thermal shock testing.

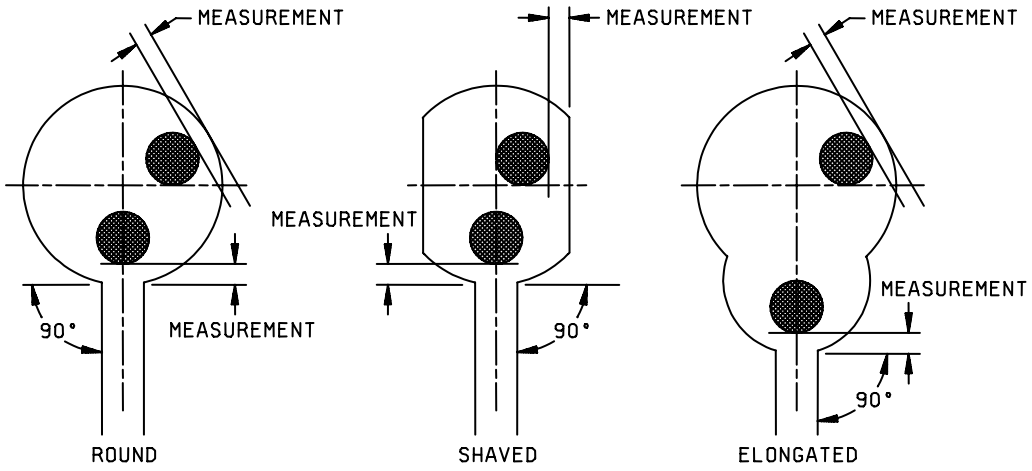


FIGURE A–1. External annular ring measurement.

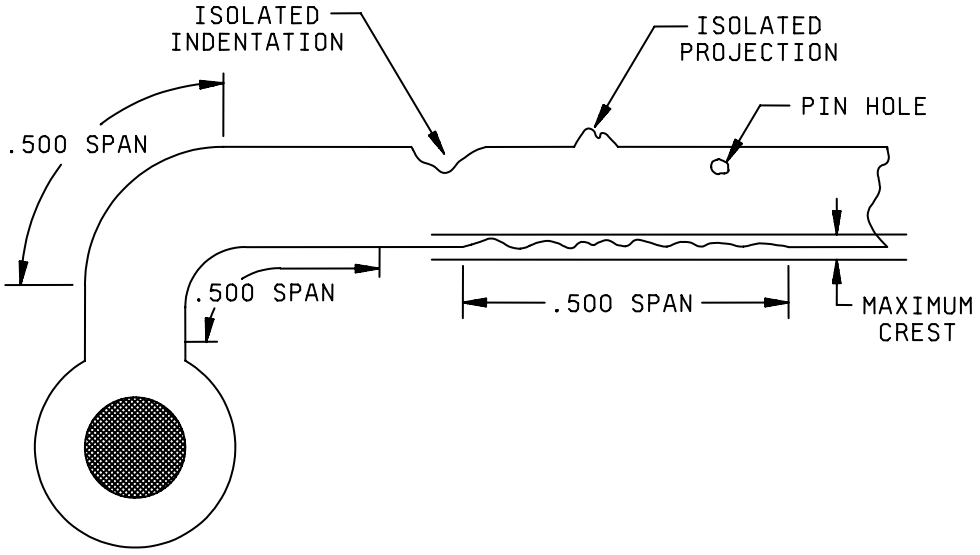


FIGURE A–2. Conductor pattern imperfection measurements.

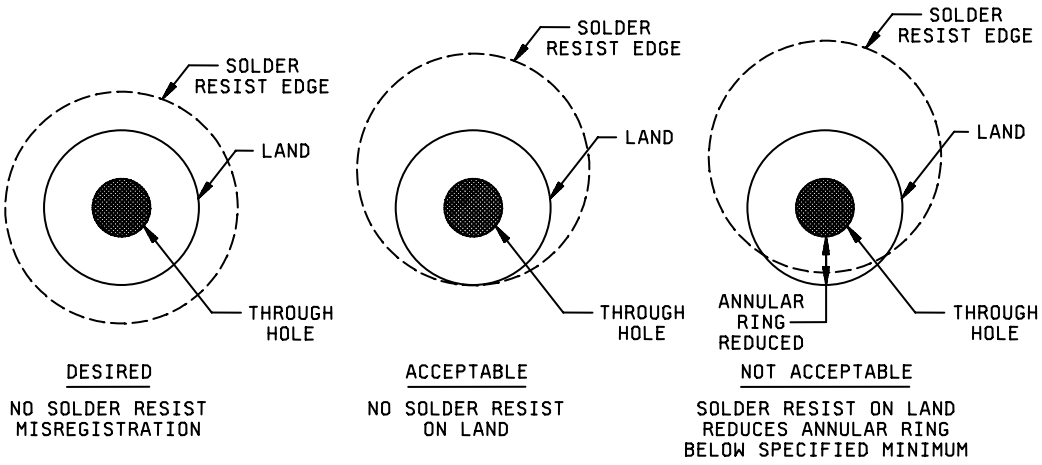


FIGURE A–3. Solder resist registration.

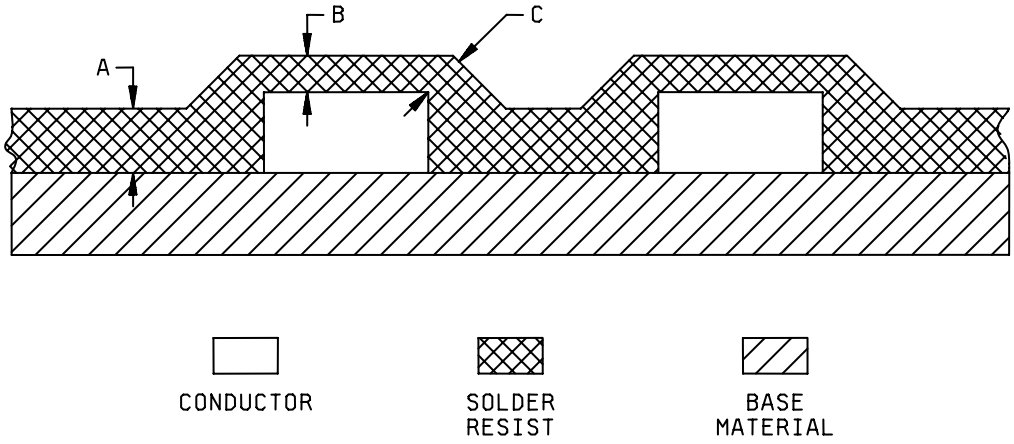


FIGURE A–4. Solder resist thickness measurement.

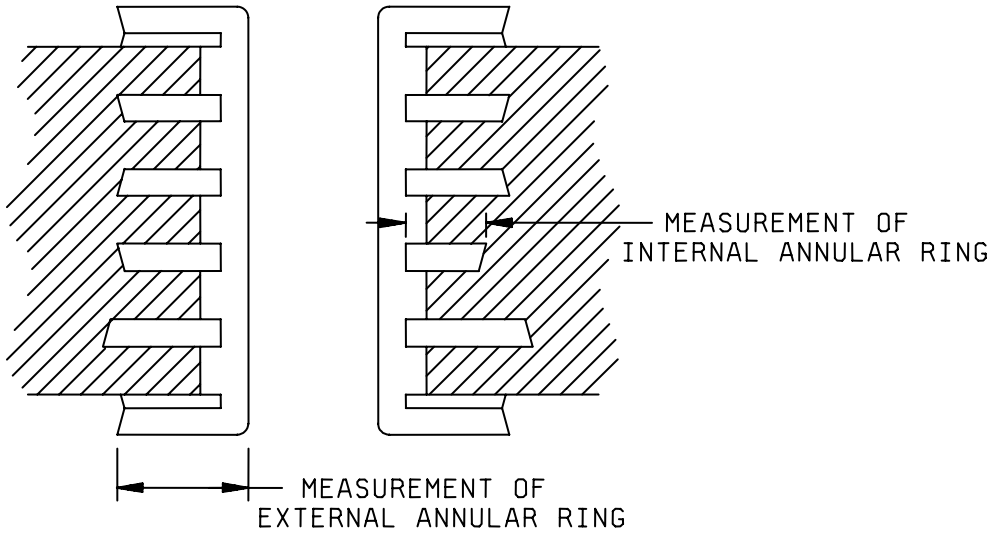


FIGURE A–5. Internal annular ring measurements.

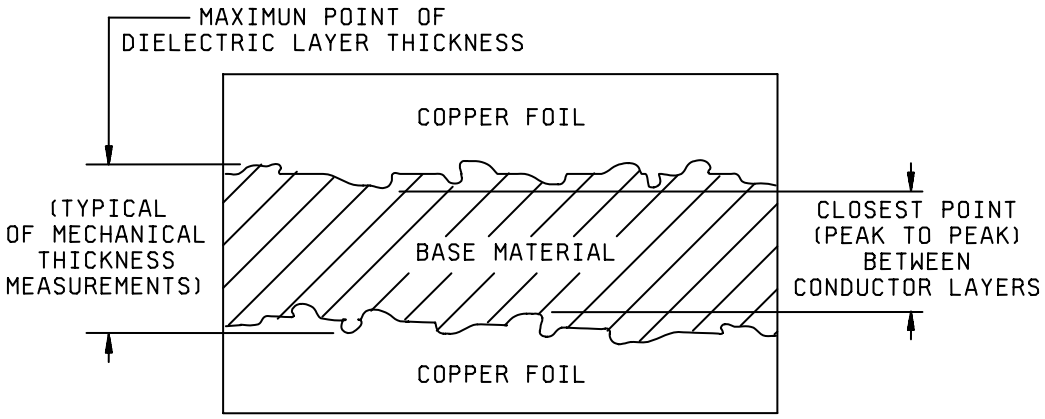


FIGURE A–6. Dielectric thickness measurement.

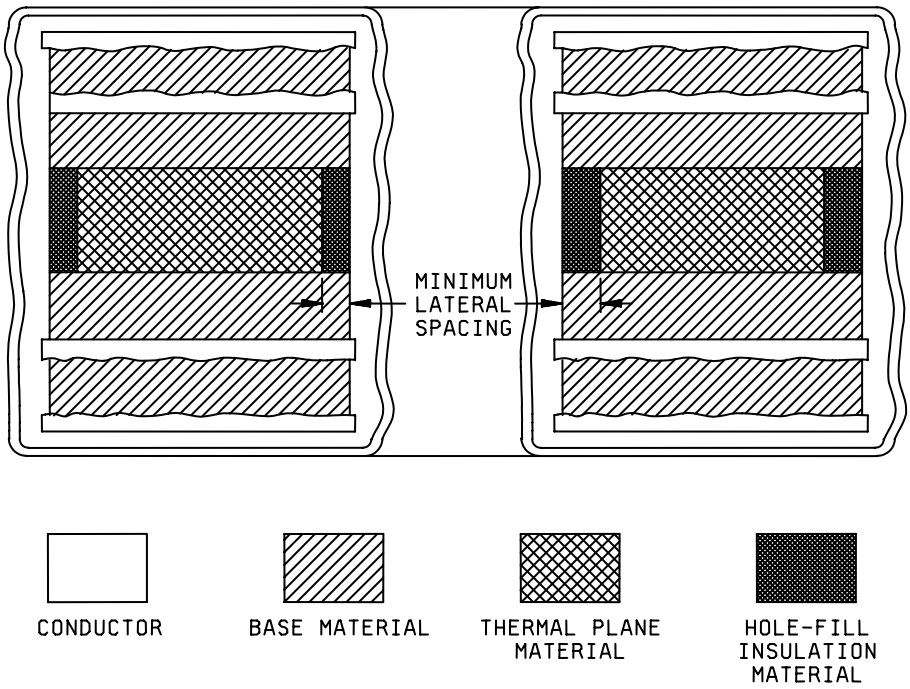


FIGURE A–7. Isolated heatsink plane dielectric spacing.

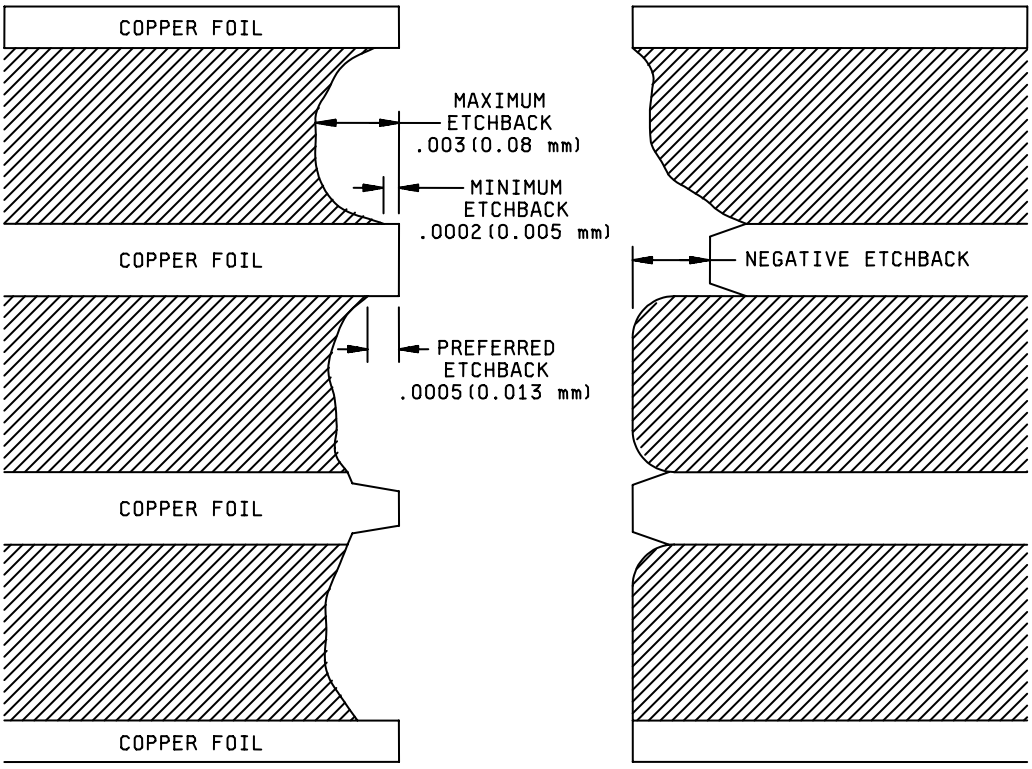


FIGURE A–8. Etchback.

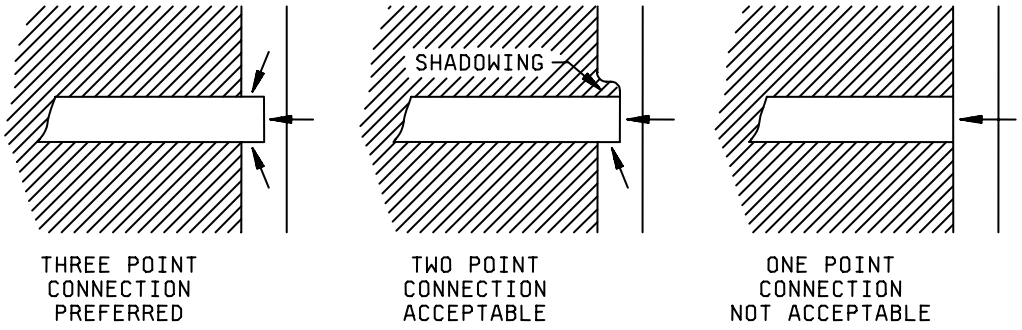


FIGURE A–9. Forms of plating to internal layer connections.

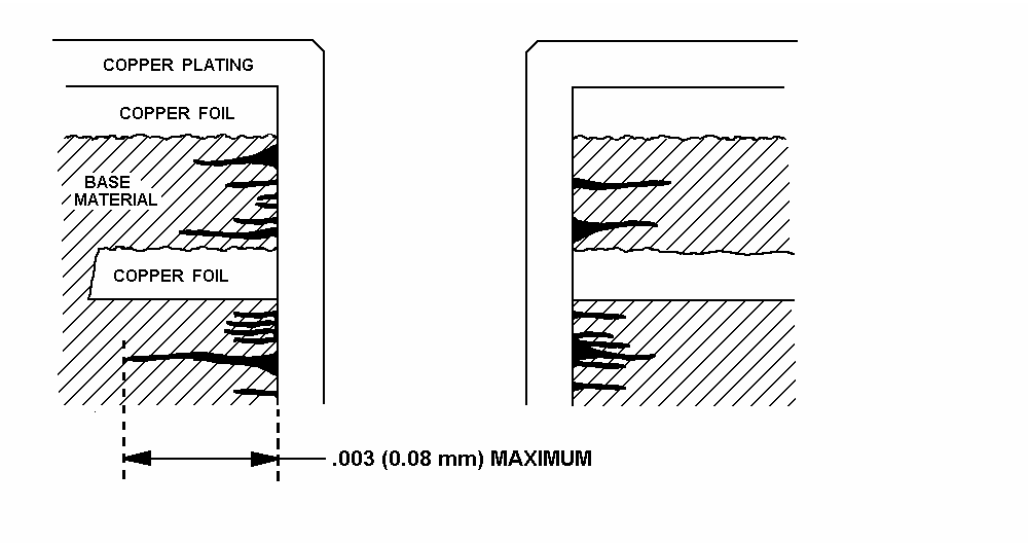
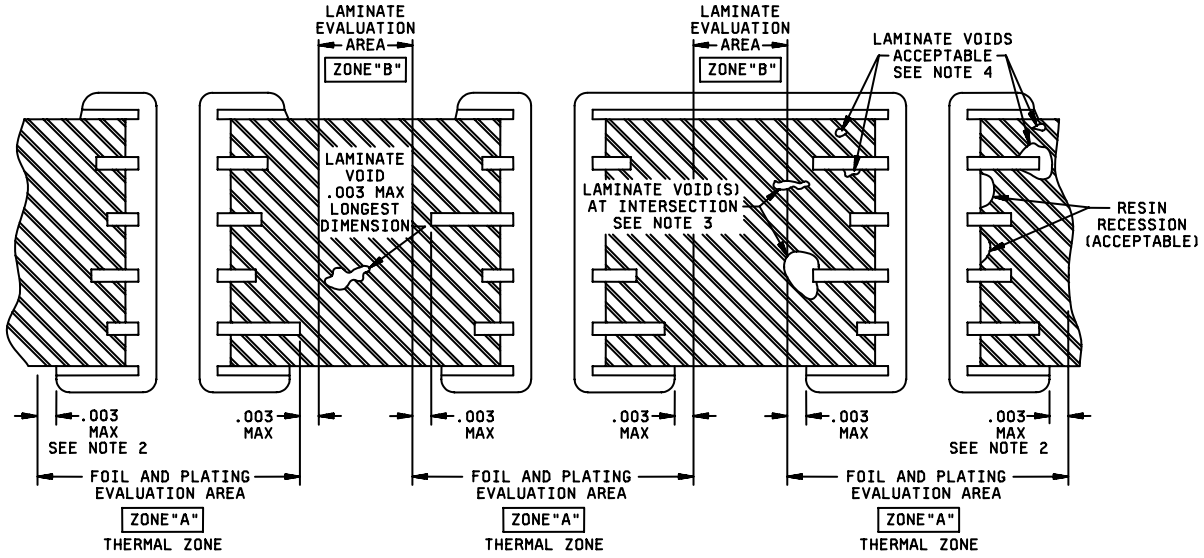


FIGURE A–10. Wicking.



NOTES:

1. Dimensions are in inches. Millimeter equivalents are given for general information only.
2. Typically beyond land edge most radially extended.
3. Voids at intersection of zone A and zone B. Laminate voids greater than .003 inch (0.08 mm) that extend into zone B are rejectable.
4. Laminate voids are not evaluated in zone A.

FIGURE A–11. Typical plated-through hole cross section after thermal stress or rework simulation.

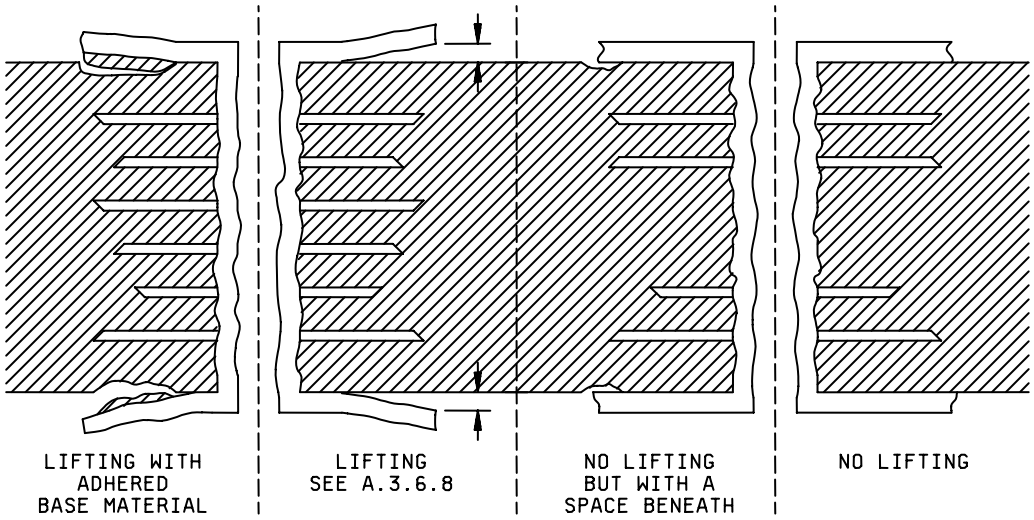


FIGURE A–12. Types of lifted lands.

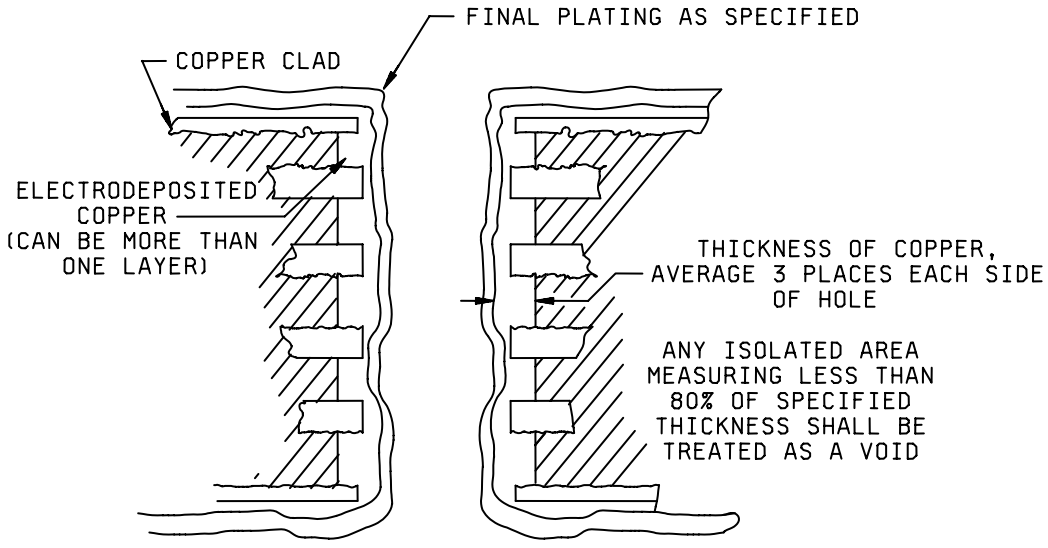


FIGURE A–13. Copper plating thickness.

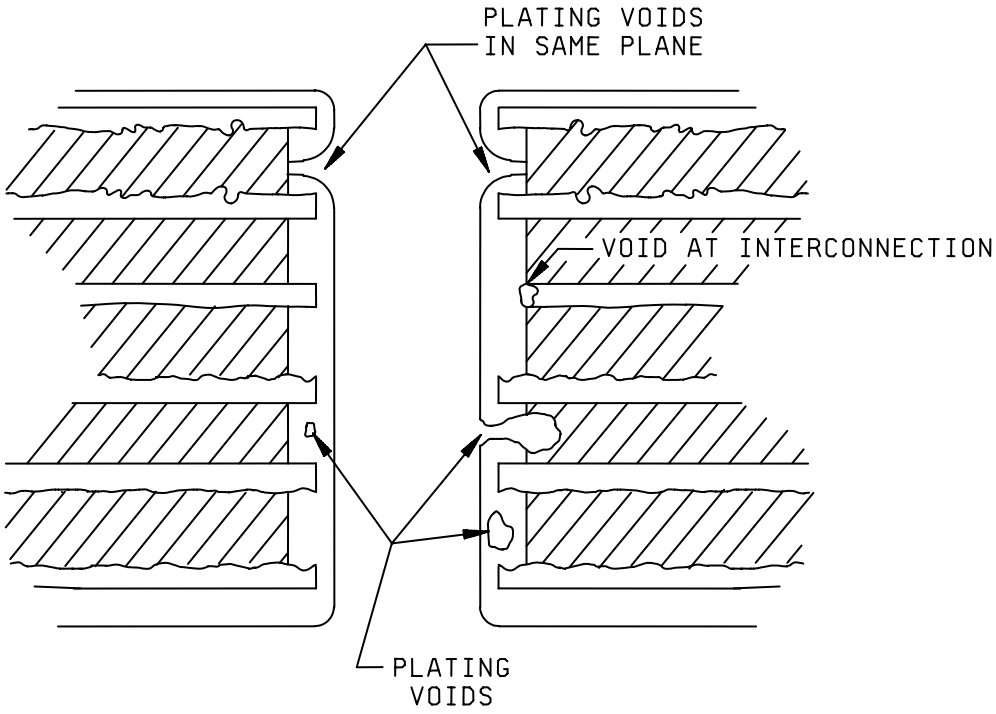


FIGURE A–14. Copper plating voids.

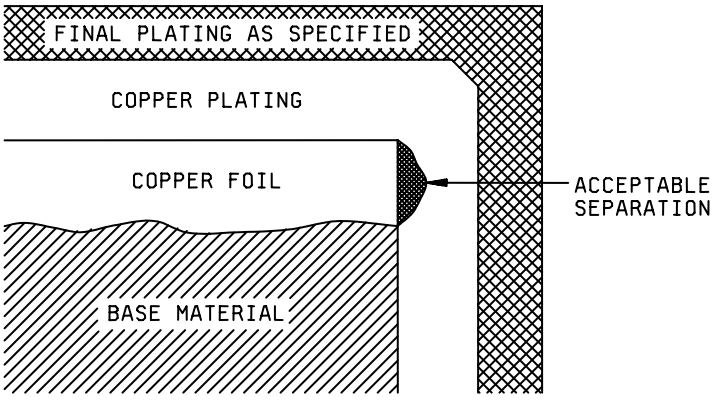


FIGURE A–15. Acceptable separation at external copper clad.

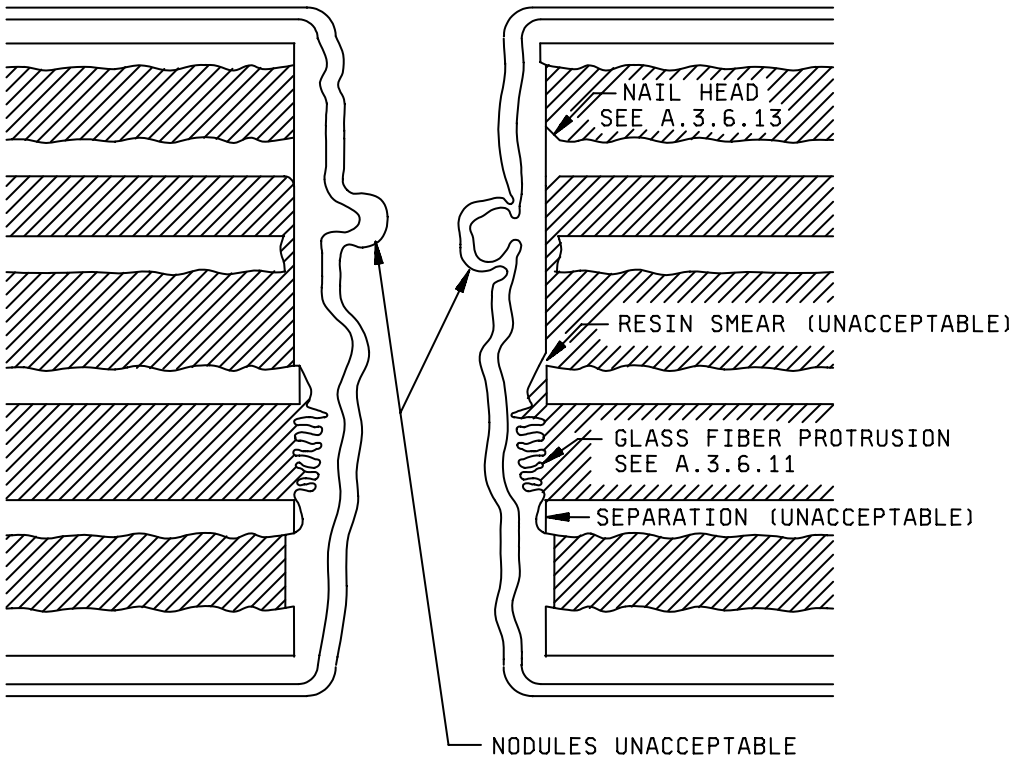


FIGURE A–16. Plated through hole deficiencies.

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OPTIONAL QPL/QML PRODUCT ASSURANCE REQUIREMENTS FOR QUALIFIED MANUFACTURER LIST PROGRAMS

B.1. SCOPE

B.1.1 Scope. This appendix contains optional requirements concerning the QPL/QML product assurance level for printed wiring boards covered by this specification. The process for extending qualification is also outlined herein. This appendix is a mandatory part of the specification when the QPL product assurance level of appendix A is not implemented. The information contained herein is intended for compliance. This appendix can be used only by manufacturers certified and qualified for listing on QML-31032.

B.2. APPLICABLE DOCUMENTS

B.2.1 General. The documents listed in this section are specified in sections B.3, B.4, or B.5 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections B.3, B.4, or B.5 of this specification, whether or not they are listed.

B.2.2 Government documents.

B.2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

MIL-PRF-31032 – Printed Circuit Board/Printed Wiring Board, General Specification for.

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or http://assist.daps.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111–5094.)

B.2.3 Order of precedence. In the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

B.3. REQUIREMENTS

B.3.1 Performance requirements. The performance requirements of the applicable MIL-PRF-31032 specification sheet shall apply to all printed wiring boards procured to the QPL/QML product assurance level.

B.3.2 Accept/reject criteria. The accept/reject criteria of the applicable MIL-PRF-31032 specification sheet shall apply to all printed wiring boards procured to the QPL/QML product assurance level.

B.3.3 QML brand. At the option of the manufacturer, the QML brand specified in MIL-PRF-31032 may be placed on printed wiring boards that comply with the product assurance requirements of this appendix.

B.4. VERIFICATION

B.4.1 Qualification inspection (reciprocal qualification from MIL-PRF-31032). A reciprocal qualification listing (i.e., from a technology qualified to a MIL-PRF-31032 specification sheet) to this document will depend on the level of QML technology qualified. Unless otherwise detailed in MIL-PRF-31032 qualification test plan, the following guidelines will apply:

a. Printed board type (see 6.5.3 and A.4.5.4.1). The extent of qualification for base materials types defined in A.4.5.4 will apply. EXAMPLE: A type 2 qualification under a MIL-PRF-31032 specification sheet will not justify a type 3 qualification listing to this document.

b. Printed board material (see A.4.5.4.2). The extent of qualification for base materials types defined in A.4.5.4 will apply. EXAMPLE: A qualification using a woven aramid reinforced thermosetting epoxy resin base material under a MIL-PRF-31032 specification sheet will justify and equivalent base material qualification listing to this document.

c. Complexity. The QPL/QML manufacturer can supply QPL compliant printed wiring boards greater than their qualified QML capability (similar to the traditional QPL product assurance level). Printed board designs verified using the QPL/QML option shall flow through the conversion of customer requirements element of the approved Quality Management (QM) plan as described in MIL-PRF-31032 appendix A. The Technical Review Board (TRB) shall evaluate designs exceeding their current QML-31032 qualification listing to determine if the add-on qualification provisions of MIL-PRF-31032 shall be used. Reasons for not using the add-on qualification provisions shall be documented in the periodic status reports.

B.4.1.1 Concurrent qualification. Manufacturers already qualified to the QPL level of this document will retain that listing after transitioning to the QPL/QML level. The 3 year expiration time will not apply to the QPL/QML product assurance level.

B.4.1.2 Retention (see B.6.4). The QML status report described in MIL-PRF-31032 will cover the QPL/QML retention requirements to this document.

B.4.2 QPL/QML product assurance. The product assurance requirements for the QPL/QML level of printed wiring board furnished under this specification shall be satisfied by certification to MIL-PRF-31032. All printed wiring boards manufactured and delivered in compliance with this appendix should be produced in accordance with the approved quality management plan.

B.4.3 Printed wiring board performance verification. Printed wiring board performance verification inspection shall consist of inspections on the production printed wiring boards and test coupons specified in the applicable MIL-PRF-31032 specification sheet. The following details are applicable to the QPL/QML product assurance level:

a. Lot conformance inspection (LCI) product acceptance testing should be based on the applicable verification flows (in-process and group A) offered by this document (see A.4.4 and appendix D) or the routine from a similar technology described by a MIL-PRF-31032 specification sheet. The various verification flows should be based upon the design standard used to design the printed wiring boards and the available panel test coupons for the printed wiring boards.

b. MIL-PRF-31032 periodic conformance inspection (PCI) program can be used in lieu of group B inspection (see A.4.7.1).

c. Test optimization is applicable to this appendix and can be applied to any verification flow detailed in this document.

B.5. PACKAGING

B.5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see A.6.2). When actual packaging of materiel is to be performed by DoD or in house personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activity within the Military Service or Defense Agency, or within the Military Service's system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

B.6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory.)

B.6.1 Intended use. This appendix is intended to be used by manufacturers certified to MIL-PRF-31032 to reduce the complexity of maintaining multiple product/process and testing flows (both MIL-PRF-55110 or MIL-PRF-31032) within a the manufacturing and testing facility.

B.6.2 Application of the QPL/QML product assurance level to existing requirements.

B.6.2.1 Use of existing master drawings. The QPL/QML printed wiring board manufacturer can use pre-existing master drawing and production artwork without any modifications (existing production masters test coupons and requires no additional or new ones).

B.6.2.2 Form, fit, and function. The form, fit, and function of the printed wiring boards, whether the QPL/QML product assurance level or the QPL product assurance level is used, will be the same.

B.6.2.3 Certification. The printed wiring boards can be certified as being compliant to this specification (MIL-PRF-55110).

B.6.3 Benefits of the QPL/QML product assurance level. Printed wiring boards produced by QML manufacturers using the provisions of this appendix in lieu of previous revisions would be compliant to this specification (MIL-PRF-55110) in accordance with the QPL/QML product assurance level with the added benefits as follows:

a. The QPL/QML manufacturer can use pre-existing master drawing and production artwork without any modifications needed (can use existing production masters test coupons and requires no additional or new ones).

b. The printed wiring boards, whether the QPL/QML option or the QPL option is used, will be the same.

c. The level of quality will be the same or higher than the QPL product assurance level.

d. When using the correct verification test (for the design), the cost should be the same or less due to enhancements made to accept/reject criteria.

e. Customers will be more confident that a QPL/QML manufacturer has demonstrated the capabilities to build its' design dues to its QML certification and qualification rather the generic standardized qualification test vehicle of the QPL quality assurance level portion of this document.

B.6.4 Retention issues. The manufacturer need only to keep the qualifying activity apprised of its total QML program, i.e., their MIL-PRF-31032 QML program and this specification's QPL/QML product assurance level. This means that the manufacturer does not have to maintain two separate compliance programs, (i.e., no requirement for a QPL compliance program for this specification to be separate from a QML program for MIL-PRF-31032).

B.6.5 Certificates of compliance issues. The manufacturer can certify QPL/QML printed wiring boards process under their MIL-PRF-31032 QML program as compliant to this document. The certificate of compliance should reference the QPL/QML product assurance level to differentiate the compliant product from printed wiring boards verified using the QPL product assurance level offered in this document.

B.6.6 Past specification revisions (see appendix D). Printed wiring boards procured to this document meets and exceeds all quality and reliability requirements of previous revisions of MIL-P-55110 or MIL-PRF-55110.

C = 0 (ZERO DEFECT) SAMPLING, TEST EQUIPMENT, AND INSPECTION FACILITIES

C.1. SCOPE

C.1.1 Scope. This appendix details the statistical sampling procedures to be used with the QPL product assurance level of this specification. It also details requirements and procedures pertaining to test equipment and inspection facilities. This appendix is a mandatory part of the specification. The information contained herein is intended for compliance.

C.2. APPLICABLE DOCUMENTS

C.2.1 General. The documents listed in this section are specified in sections C.3, C.4, or C.5 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections C.3, C.4, or C.5 of this specification, whether or not they are listed.

C.2.2 Non-Government publications. The following documents form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

NCSL INTERNATIONAL (NCSL)

NCSL Z540-1 – Calibration Laboratories and Measuring and Test Equipment, General Requirements for.

(Application for copies should be addressed to the NCSL International, 2995 Wilderness Place, Suite 107, Boulder, CO 80301–5404 or at URL http://www.ncsli.org.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

C.2.3 Order of precedence. In the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

C.3. DEFINITIONS AND SYMBOLS FOR C = 0 SAMPLING

C.3.1 Definitions. The following definitions shall apply for all statistical sampling procedures:

a. C = 0 sample plan: The C = 0 sample plans are defined as a combination of a test specimen usage identifier (see C.3.1.b) and a sample size series (see C.3.1.c). The resulting C = 0 sample plan will be a two character designator combination that identifies the sample size series that is to be with a type of test specimen for a particular verification (see C.4.5).

b. Test specimen usage identifier (see C.4.5 for examples): The following usage modifiers are used to differentiate when a particular plan is to be used for a particular test specimen:

   (1) The letter "B" will be used to signify that production printed boards are to be sampled.

   (2) The letter "T" will be used to signify that test coupons are to be sampled based on the number of panels in the lot.

   (3) An asterisk "*" will be used for either printed boards or test coupons.

c. Sample size series: The sample size series is defined as the following series of letters: A, D, F, H, J, L, and N that are listed in table C–I (see C.4.5 for examples). NOTE: Sample size series “A” was identified as “B” in previous revisions.

d. Tightened inspection: Tightened inspection is defined as sampling using an increased sample size (see C.4.3).

e. Acceptance number (C): The acceptance number is defined as an integral number associated with the selected sample size which determines the maximum number of defectives permitted for that sample size.

f. Rejection number (R): Rejection number is defined as one plus the acceptance number.

C.3.2 Symbols. The following symbols shall apply for all statistical sampling procedures:

a. C: Acceptance number.

b. R: Rejection number.

C.4. STATISTICAL SAMPLING PROCEDURES AND SAMPLE PLAN TABLE

C.4.1 General. Statistical sampling shall be conducted using the C = 0 method. The C = 0 method as specified herein is a sampling plan that provides a high degree of assurance that a lot having a proportion defective greater than the specified acceptance number (C = 0) will not be accepted. For all situations, the acceptance number (C) shall be equal to 0 (C = 0) and the rejection number (R) shall be 1 or greater ($R \geq 1$).

C.4.2 Acceptance and procedure.

C.4.2.1 Acceptance number (C = 0). Acceptance of inspection lots shall be based on an acceptance number of zero (C = 0).

C.4.2.2 Rejection number ($R \geq 1$). Failure of a sample unit for one or more tests of a subgroup shall be charged as a single failure. One or more sample rejects shall be cause for failure of the lot or sublot, as applicable. Any failure on any of the sample units shall constitute a failure of the entire inspection lot or sublot.

C.4.3 Tightened inspection (for reevaluation purposes). Tightened inspection shall be performed by sampling using double the sample size as specified in table C–I with zero failures allowed or 100 percent.

C.4.4 Sample size. The sample size for each subgroup shall be determined from table C–I. If lot size is smaller than sample size, test all of the units. The manufacturer may, at their option, select a sample size greater than that required; however, the number of failures permitted shall not exceed the acceptance number.

C.4.5 C = 0 sample plan construction (selection and usage of the sample size series). The sample size series of table C–I to be used will be directed from the appropriate inspection table. The inspection table will specify the C = 0 sample plan (test specimen identifier and sample size series) or plans (test printed wiring board, panels, or either one) to use.

EXAMPLES: If an inspection table specified that "Plan BF or TL" be used when verifying test specimens, it is specifying that sample size series "F" of table C–I shall be used for selecting printed wiring boards and sample size series "L" shall be used for selecting test coupons from panels. If the same inspection table specified that "Plan *H" be used, then sample size series "H" of table C–I can be used for either printed wiring boards or panels.

TABLE C–I. C = 0 (zero defect) sampling.

Lot size	Sample size (number of test specimens to be inspected) 1/						
	Series A	Series D	Series F	Series H	Series J	Series L	Series N
1 to 8	All	All	All	5	3	2	1
9 to 15	All	All	13	5	3	2	1
16 to 25	All	All	13	5	3	2	1
26 to 50	All	32	13	5	5	3	1
51 to 90	50	32	13	7	6	4	2
91 to 150	50	32	13	11	7	5	2
51 to 280	50	32	20	13	10	6	2
281 to 500	50	48	29	16	11	7	3
501 to 1,200	75	73	34	19	15	8	4
1,201 to 3,200	116	73	42	23	18	9	5

1/ If lot size is smaller than sample size test all of the units. Sample size series “A” was identified as “B” in previous revisions.

C.5. TEST EQUIPMENT AND INSPECTION FACILITIES

C.5.1 Test equipment and calibration. All tests and measurements for process control, qualification testing, inspection of product for delivery (in-process and group A), or periodic conformance inspection (group B) shall be made with capable instruments whose accuracy has been verified. Calibration of measurement, test equipment, and test standards that control the accuracy of inspection and test equipment and facilities shall be in accordance with NCSL Z540-1 or equivalent. Calibrated test equipment and test standards shall be controlled, used, and stored in a manner suitable to protect calibration integrity. Test equipment requiring calibration shall be identified and labeled in accordance with NCSL Z540-1 or an equivalent system, approved by the qualifying activity.

C.5.2 Inspection facilities. The inspection facility (either the manufacturer’s site or a certified suitable laboratory) used to perform qualification testing and periodic conformance inspection shall be approved by the qualifying activity for the performance of the tests and inspection requirements of compliant printed wiring boards.

C.5.3 Acquiring activity or manufacturer imposed tests. Acquiring activity or manufacturer imposed tests shall be in accordance with the requirements specified in the master drawing. If any additional imposed tests detect a problem, the manufacturer shall submit all panels/printed wiring boards in the lot to those tests to eliminate rejects and shall take steps to determine and eliminate the cause of failure.

C.5.4 Test method alternatives. Alternate test methods are allowed provided that it is demonstrated to the qualifying activity that such alternatives in no way relax the requirements of the test method referenced by this specification (see appendix B).

C.5.5 Procedure in case of test equipment malfunction or inspection/test personnel error. When it has been established that a improper test is due to test equipment malfunction or inspection/test personnel error, the inspection facility shall document the results of its investigations and corrective actions, if required, and shall make this information available to the qualifying activity and the acquiring activity, as applicable.

C.5.6 Resolution of measurement devices and test equipment. Unless otherwise specified (see 3.1.1), the resolution of measurement devices and test equipment used for the evaluation of printed board performance shall be at least a factor of 10 better than the limits or tolerances of a value to be determined. (For example: a voltmeter resolution of +/– 0.1 percent to determine level to a tolerance of +/– 1 percent).

C.5.7 Values (true and nominal). The limits of size specified in this specification are for true values. Nominal values are indicated by the inclusion of a tolerance. Proper allowance shall be made for measurement errors (including those due to deviations from nominal test conditions) in establishing the working limits to be used for the values to be measured, so that the values of the test specimen parameters (as they would be under nominal test conditions) can be determined properly.

C.5.8 Numeric reporting. The results of printed wiring board verification shall be presented in accordance with test method number 1.6 of IPC-TM-650.

C.5.9 Rounding of measurements. Values determined by measurement can be rounded to one decimal place beyond the resolution specified. Example, the minimum etchback requirement is .0002 inch. The resolution required of the measurement device in accordance with C.5.6 would to the +/– .00001 inch. In a case where an inspection/test personnel uses an instrument capable of resolution to +/– .000001 inch, a measurement of .000186 inch is determined for etchback on that test specimen. This value cannot be rounded to .0002 inch or even .00019 inch. It can be truncated to .00018 inch or reported as taken as .000186 inch.

C.6. DEFINITIONS FOR TEST EQUIPMENT AND INSPECTION FACILITIES

C.6.1 Accuracy. A measure of the closeness of an individual measurement or the average of a number of measurements to the true value. Accuracy includes a combination of random error (precision) and systematic error (bias) components that are due to sampling and analytical operations.

C.6.2 Bias. The systematic or persistent distortion of a measurement process, which causes errors in one direction (i.e., the expected sample measurement is different from the sample's true value).

C.6.3 Calibration. Calibration is an activity related to measurement and test equipment. Calibration is the comparison of measurement standard, instrument, or item of known precision and bias with another standard, instrument, or item to detect, correlate, report, or eliminate by adjustment, any variation in the precision and bias of the item being compared. Use of calibrated measurement standard, instrument, or items provide the basis for value traceability of product technical specifications to national standard values.

C.6.4 Measurement and testing equipment. Tools, gauges, instruments, sampling devices, or systems used to calibrate, measure, test, or inspect in order to control or acquire data to verify conformance to specified requirements.

C.6.5 Precision. The degree to which a measurement standard, instrument, item, test, or process exhibits repeatability. Expressed statistically or through various techniques of Statistical Process Control (SPC), the term is many times used interchangeably with "repeatability". Precision is a measurement of how closely the analytical results can be duplicated.

C.6.6 Resolution. The smallest unit of readability or indication of known value on an instrument, device, or assemblage thereof. It is also related to the gradations on measuring instruments and the ability of the inspection/test personnel to interpret between those gradations. The resolution value is frequently used in the device literature to classify the instrument.

C 6.7 Tolerance (IPC-T-50). The total amount by which a specific dimension is permitted to vary. A tolerance is indicated in this specification only if it is expressed as the variation about a specified value (also known as a “nominal value”).

C.6.8 Uncertainty. An expression of the combined errors in a test measurement process. Stated as a range within which the subject quantity is expected to lie. Comprised of many components including: estimates of statistical distribution and results of measurement or engineering analysis. Uncertainty established with a suitable degree of confidence, may be used in assuring or determining product conformance and technical specifications.

C.6.9 Supporting documents. The documents in this section may be used as guidelines for understanding measurement and test assurance principals.

INTERNATIONAL ORGANIZATION FOR STANDARDIZATION (ISO)

ISO14253–1 – Geometrical Product Specifications (GPS) - Inspection by Measurement of Workpieces and Measuring Equipment - Part 1: Decision Rules for Proving Conformance or Non-Conformance with Specifications.

(Application for copies should be addressed to the International Organization for Standardization, Case Postale 56, Geneva, Switzerland CH–1211 or at URL http://www.iso.org.)

NCSL INTERNATIONAL (NCSL)

NCSL Z540–2 – U. S. Guide to the Expression of Uncertainty in Measurement.

(Application for copies should be addressed to the NCSL International, 2995 Wilderness Place, Suite 107, Boulder, CO 80301–5404 or at URL http://www.ncsli.org.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

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SUPERSESSION, VERIFICATION CONFORMANCE INSPECTION OPTIONS, AND USAGE OF PAST DESIGN STANDARDS

D.1. SCOPE

D.1.1 Scope. This appendix contains information and guidance concerning the supersession of legacy Department of Defense documents such as MIL-P-55110, revisions C, D, and E and MIL-STD-275, revisions D and E. This appendix is not a mandatory part of this specification. The information contained herein is intended for guidance only.

D.2. APPLICABLE DOCUMENTS

D.2.1 General. The documents listed in this section are specified in sections D.3 and D.4 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections D.3 or D.4 of this specification, whether or not they are listed.

D.2.2 Non-Government publications. The following documents form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

IPC – ASSOCIATION CONNECTING ELECTRONICS INDUSTRIES (IPC)

IPC-T-50	–	Interconnecting and Packaging Electronic Circuits, Terms and Definitions.
IPC-D-275	–	Design Standard for Rigid Printed Boards and Rigid Printed Board Assemblies.
IPC-2221	–	Printed Board Design, Generic Standard for.
IPC-2222	–	Sectional Design Standard for Rigid Organic Printed Boards.

(Application for copies should be addressed to the IPC – Association Connecting Electronics Industry, 3000 Lakeside Drive, Suite 309 S, Bannockburn, IL 60015–1249 or at URL http://www.ipc.org.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

D.2.3 Order of precedence. In the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

D.3. DEFINITIONS

D.3.1 Design standard. A document that establishes the standard practices, guidelines, and default values for the design of printed wiring boards. Within this appendix, the term "design standard" is used to describe those documents that contain the design, construction, material, and test coupon requirements and guidelines.

D.3.2 Legacy designs or documents (superseded standards). See D.4.1.

D.3.3 Supersession. The act of replacing a legacy document that no longer exists or is no longer supported with a currently supported document.

D.3.4 Quality conformance test circuitry. See IPC-T-50.

D.3.5 Printed wiring board types. The printed board types shall be as defined in IPC-D-275 or IPC-2222. Printed board types 4, 5, and 6 described by IPC-D-275 or IPC-2222 were included in type 3 of MIL-STD-275.

D.4. SUPERSESSION

D.4.1 Superseded specifications. Appendix A of this document includes the essential requirements of the previous revision and can be used to supersede the specifications listed in 6.4.4.

D.4.1.1 Reference to superseded specifications. All the requirements of this document (MIL-PRF-55110G) can be interchangeable with those of MIL-P-55110. Therefore, existing procurement documents (master drawings or OEM documents) referencing MIL-P-55110 need not be revised, updated, or changed to make reference to MIL-PRF-55110 in order for this document to be used.

D.4.2 Superseded guidelines and standards. The following design standards have been superseded by IPC-2221 or IPC-D-275 for all types and classes of printed wiring boards:

a. MIL-STD-275D, dated 26 April 1978.
   1. MIL-STD-275D with notice 1, dated 19 January 1979.
   2. MIL-STD-275D with notice 2, dated 10 October 1979.
   3. MIL-STD-275D with notice 3, dated 5 October 1980.
   4. MIL-P-55110C with notice 4, dated 28 May 1982.
   5 MIL-P-55110C with notice 5, dated 7 February 1984.

b. MIL-STD-275E, dated 31 December 1984.
   1. MIL-STD-275E with notice 1, dated 8 July 1986.

c. IPD-D-275, dated September 1991.
   1. IPC-D-275 with amendment 1, dated April 1996.

d. IPC-2221A, dated May 2003.
   1 IPC-2221 with amendment 1, dated January 2000.
   2. IPC-2221, dated February 1998.

D.4.2.1 Estimation of design standard used. When no design standard is listed on the master drawing, either the design activity or printed board manufacturer, should be contacted to ascertain which design standard should be used to verify the design parameters during group A or group B inspection.

D.4.2.2 Retooling. Printed wiring boards that were designed using superseded Department of Defense design standards do not require conversion to IPC-2221 or IPC-D-275.

D.4.3 Testing.

D.4.3.1 Group A testing. Group A testing should be performed to the specific revision, and amendment if applicable, called out by the acquisition documents. For example, if printed wiring boards are produced to MIL-P-55110D with amendment 1, MIL-P-55110D with amendment 3, and MIL-P-55110E, a manufacturer would be expected to perform group A testing, for the applicable lot, to the requirements of the revision specified. In those three different revisions (D with amendment 1, D with amendment 3, and E) a requirement for an acceptability criteria or test procedure may be the exact same, it might be slightly different, it may be significantly different, or there may not even be a requirement. Retention of qualification summaries for group A should list the lots produced, grouped by revision, and when applicable, revision with specific amendment.

D.4.3.2 Group B samples and testing. Samples to be selected for group B testing should be based on the most complex compliant printed wiring boards produced that month. For example, if printed wiring boards are produced to MIL-P-55110D, MIL-PRF-55110E with amendment 1, and MIL-PRF-55110F during a given month, and the most complex printed wiring boards produced that month were in the lot ordered to MIL-PRF-55110E with amendment 1, then that should be the lot from which the group B sample should be selected. The samples should be tested in accordance with MIL-PRF-55110E with amendment 1. If during that same month, printed wiring boards were produced to MIL-P-55110A and MIL-P-55110B, group B tests to those specific revisions would also be required in order to be compliant to those revisions, unless specifically specified in the contract.

D.4.4 Superseded test coupons. Before MIL-P-55110C, test coupons were only used for first article inspection and not required for production. The production panel test coupons were introduced within MIL-P-55110C and MIL-STD-275D were for the supplier certification program concept. The production test coupons of MIL-P-55110C, described within MIL-STD-275, should be used when already incorporated onto production tooling. New designs or jobs should use the test coupons specified in IPC-2221.

D.4.4.1 Test coupons, placement, quantity, and usage. IPC-2221 contains a table that specifies for each production panel the test coupon placement, quantity (see note) and usage (similar to IPC-D-275 and MIL-STD-275). NOTE: There needs to be a sufficient number of test coupons on the production panel in order to be able to perform group A and, when necessary, group B inspection regardless of the number of test coupons specified by the design standard.

D.4.5 Intended use and intent of this appendix. This appendix can be used to understand the test coupons that were referenced in previous revisions of this document. These guidelines are intended for the re-identification and proper usage of test coupons within this document that are, or were originally identified, in various legacy Department of Defense printed wiring board design standards. This appendix is intended for use in conjunction with a manufacturer's verification conformance compliancy program.

D.4.5.1 Revisions. Printed wiring boards tested to this document generally would meet or exceed the performance requirements of past revisions. However, due to various changes in acceptability and evaluation criteria, testing procedures, and test coupon sampling, an exact duplication of a previous revision cannot be claimed or made in all areas of concern. Manufacturers should not pick-and-choose or mix acceptability requirements or test procedures from one revision of MIL-PRF-55110 or MIL-P-55110 to another. Compliance should be either to MIL-P-55110C, MIL-P-55110D, MIL-P-55110E, MIL-PRF-55110E, MIL-PRF-55110F (with a specific amendment, if applicable), or this document entirely, unless the manufacturer documents a direct correlation between the revisions (with any amendments, if applicable) under consideration.

D.4.5.2 Test coupons, placement, quantity, and usage. IPC-2221 contains a table that specifies for each production panel the test coupon placement, quantity, and usage (as did IPC-D-275 and MIL-STD-275).

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SEQUENTIAL ELECTROCHEMICAL REDUCTION ANALYSIS (SERA) SOLDERABILITY TEST

E.1. SCOPE

E.1.1 Scope. This test method describes the method and procedure used to evaluate oxidation levels on solderable surfaces. The type and quantity of oxides on copper, tin, and lead surfaces have a significant impact on solderability. The procedure involves using electrochemical reduction techniques to determine the type and quantity of oxide on plated-through holes, attachment lands, and printed wiring board surface conductors. The SERA solderability test method is offered as an alternative to other solderability test methods required by this document. This test method shall not be contractually imposed upon either the contractor or sub-contractor. This appendix is not a mandatory part of the specification. The information contained herein is intended for compliance only when volunteered as an alternative to the other solderability test methods detailed.

E.2. APPLICABLE DOCUMENTS

E.2.1 General. The documents listed in this section are specified in sections E.3 and E.4 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements documents cited in sections E.3 and E.4 of this specification, whether or not they are listed.

E.2.2 Government documents.

E.2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

COMMERCIAL ITEM DESCRIPTION

A–A–59282 – Chemicals, Analytical; General Specification for.

(Copies of these documents are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111–5094 or online at http://assist.daps.dla.mil/quicksearch/ or http://assist.daps.dla.mil.)

E.2.2.2 Non-Government publications. The following documents form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

IPC – ASSOCIATION CONNECTING ELECTRONICS INDUSTRIES (IPC)

J-STD-004 – Soldering Fluxes, Requirements for.

(Application for copies should be addressed to the IPC – Association Connecting Electronics Industry, 3000 Lakeside Drive, Suite 309 S, Bannockburn, IL 60015–1249 or at URL http://www.ipc.org.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

E.2.3 Order of precedence. In the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

E.3. DEFINITIONS

E.3.1 Sequential Electrochemical Reduction Analysis (SERA). A chronopotentiometric reduction method for assessing tin-lead finish solderability.

E.4. TESTING

E.4.1 Apparatus (see figure E–1).

E.4.1.1 Reservoir (see detail A). The reservoir shall be a container constructed of a nonmetallic, nonreactive material with a minimum volume of 500 ml. The reservoir shall have an inlet/outlet port, test head chamber port, and a saturated calomel electrode (SCE) reference electrode port. The inlet/outlet port shall be connected to a vacuum trap tube. The inlet/outlet port shall incorporate a diffuser to aid in the effectiveness of the inert gas purging. Polypropylene tubing may be used for connection tubing. All connection fittings shall be of a nonreactive material. The reservoir shall have the capability of maintaining a positive pressure environment. The reservoir shall be emptied and rinsed with deionized water for every 16 hours of testing.

E.4.1.2 Test head (see detail B). The test head shall be constructed of a nonmetallic, nonreactive material. The test head shall have ports to allow inert gas purging and intake/expulsion of borate buffer solution. The test head shall have either an optical or mechanical means of aligning the test head chamber over the test plated-through hole. The test head shall use Vitron or equivalent o-rings for the test head to test surface interface seals. These o-rings shall be replaced after every 8 hours of testing unless integrity of the o-rings can be documented for extended periods. The test head shall have the capability of maintaining a positive pressure environment.

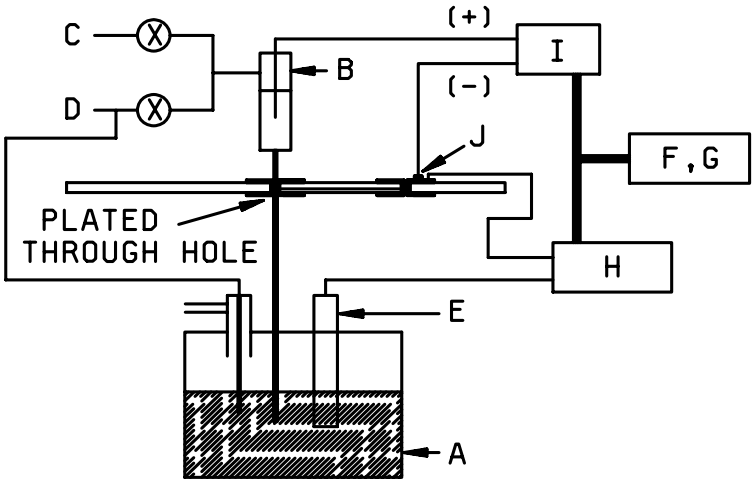

FIGURE E–1. Schematic of SERA plated through hole apparatus.

E.4.1.3 Vacuum pump (see detail C). A vacuum pump shall be used to draw buffer solution into and out of the test head compartment. The vacuum pump shall be able to draw minimum vacuum of 5 inches of Hg (16.9 kPa).

E.4.1.4 Gas regulator (see detail D). An in-line gas regulator shall be used to monitor the flow of the inert purging gas. The gas regulator shall be able to measure a minimum of 1 cubic foot per hour (0.02832 cubic meters per hour) at standard temperature and pressure.

E.4.1.5 SCE reference electrode (see detail E). The reference electrode shall be a SCE reference electrode with a temperature range of –5 degrees Celsius to +60 degrees Celsius and a Ph range of 0–14. The SCE reference electrode shall be stored in such a manner as to prevent drying out (either in a saturated KCI solution or in accordance with the manufacturer's instructions). The SCE reference electrode shall be calibrated in accordance with the manufacturer's instructions once every 30 days.

E.4.1.6 Computer (see detail F). The computer shall be equivalent to or better than a MS-DOS compatible, 80286-12 MHz, with 512 Kbyte of internal memory and floppy and hard disk drives.

E.4.1.7 IEEE-488 interface card (see detail G). An IEEE-488 interface card is required for data acquisition between the computer, the digital multimeter, and the programmable current source.

E.4.1.8 Digital multimeter (see detail H). A digital multimeter is required to measure the voltage changes during the SERA reduction. The digital multimeter shall have the following characteristics:

a. A measurable voltage range of 0 V to –2.0 V.

b. A voltage measurement tolerance of ±5 mV.

c. Voltage measurement RMS noise level should not exceed 10 Mv.

d. Input impedance should be greater than 1 G-ohm.

E.4.1.9 Programmable current source (see detail I). A programmable current source is required to apply a constant current during the SERA reduction. The programmable current source shall have the following minimum characteristics:

a. The applied current should be variable in 0.1 microamp steps between 1.0 microamps and 10 microamps.

b. The applied current should remain constant within ±5 percent.

E.4.1.10 Printed wiring board (PWB) contact pin (see detail J). A contact pin is required to complete the electrical circuit with the test plated-through hole. The contact pin shall not exert a force of greater than .5 pounds (0.23 Kg) nor alter the plated-through hole form, fit, or function.

E.4.2 Materials.

E.4.2.1 Borate buffer solution. The SERA test requires the use of a borate buffer solution. This solution uses reagent grade boric acid, sodium borate ($Na_2B_40_7 * 10\ H_20$), and de-ionized water. The recipe is 6.18 grams/liter boric acid and 9.55 grams/liter of sodium borate. The Ph of the borate buffer solution shall be in the range of 8.3 to 8.4. Adjustments to the buffer Ph shall be made using either boric acid or sodium borate additions.

E.4.2.2 Inert gas. An inert gas is required to purge oxygen from the system. Either argon or ultra high purity (99.998 percent) dry nitrogen shall be used.

E.4.2.3 De-ionized water. De-ionized water comprises a portion of the borate buffer solution and shall be used to rinse the test plated-through hole after completion of the SERA analysis. The de-ionized water shall be 1 Megohm conductivity or better.

E.4.2.4 Isopropyl alcohol. Isopropyl alcohol is used to rinse the test plated-through hole after the completion of the SERA analysis. Reagent grade isopropyl alcohol, in accordance with A-A-59282, shall be used.

E.4.2.5 Potassium chloride solution (KCl). The SCE reference electrode may be stored in a saturated KCl solution. This solution uses reagent grade potassium chloride, in accordance with A-A-59282, in a saturated solution form.

E.5. PROCEDURES

E.5.1 General. The test procedure shall be performed on three plated-through holes randomly chosen on the printed wiring board or representative test coupon. The SERA test shall be performed just prior to packaging for storage or shipment or immediately upon removal from the manufacturer's protective package. During handling, care shall be exercised to prevent the surfaces being tested from being abraded or contaminated by grease, perspirants, abnormal atmosphere, etc. The test procedure consists of the following operations:

a. Proper preparation of SERA system (see E.5.2).

b. Application of test method (see E.5.3).

c. Evaluation of test data (see E.5.4).

d. Proper post-test preparation of SERA system (see E.5.5).

E.5.2 Preparation of SERA systems.

a. Initiate inert gas flow into system and allow a minimum of 10 minutes to elapse prior to testing.

b. Turn on digital multimeter and programmable current source and allow a minimum of 10 minutes to elapse prior to testing.

c. Remove reference electrode port and rinse with deionized water. Replace reference electrode port and add sufficient quantity of borate buffer solution to immerse the SCE reference electrode a minimum of 1 inch (25.4 mm).

d. Remove SCE reference electrode from storage container. Rinse with deionized water, wipe with clean soft cloth, and place into reference electrode port. Attach system electrical connections in accordance with figure E-1.

e. Remove and replace test head o-ring seals as required (see E.4.1.2).

f. Close SERA test head together thus seating o-rings together on a representative sample plated-through hole and perform vacuum check on system. No visible air bubbles shall be detected in the test head chamber which would indicate improper sealing.

E.5.3 Application of test method.

a. The inspection/test personnel shall record the specimen lot date code and manufacturer for each individual printed wiring board. An individual printed wiring board reference chart for the test plated-through holes and PWB contact pin locations shall be maintained for each test specimen configuration.

b. Insert test specimen onto SERA test head and allow a minimum of 4 seconds for inert gas purging of the test head. Ensure inert gas bubbling is occurring in the reservoir tube.

c. Attach PWB contact pin.

d. Attach electrical source leads.

e. Draw borate buffer solution into test head chamber a minimum of 75 percent of chamber height. Visually monitor test head chamber for leaks.

f. Partially flush test head chamber to 50 percent height to dislodge any gas bubbles which could be trapped in test hole.

g. Input computer data for test specimen and test hole identification. Set current density at 30 µamp per centimeter squared (plated-through hole area shall be calculated as specified in E.5.3.1), test duration at a minimum of 400 seconds, the number of open circuit samples to be measured, and the number of systems measurements at one reading per second. The minimum test duration may be reduced provided complete plated-through hole reduction has been achieved.

h. Perform SERA test to test duration completion.

i. Remove electrical source leads.

j. Remove PWB contact clamp.

k. Flush borate buffer solution from test hole.

l. Remove test specimen from SERA test head.

m. Rinse test plated-through hole with deionized water saturated cotton swab for a minimum of 3 seconds, then rinse test plated-through hole with isopropyl alcohol saturated cotton swab for a minimum of 3 seconds. Allow test plated-through hole to air dry. The rinsing operations may be conducted for all test holes as a one time operation provided the rinsing operation is completed within 10 minutes of completion of the last test hole on that individual printed wiring board specimen. Other documented rinsing operations may be used provided their effectiveness is as good as or better than the cotton swab rinse process.

E.5.3.1 Plated-through hole area calculation. The area of plated-through holes shall be determined using:

$$\text{Area} = (2)(\pi)(R1)(H) + [(2)(\pi)(R2^2) - (2)(\pi)(R1^2)]$$

where

H = Printed wiring specimen thickness.
R1 = Plated-through hole radius.
R2 = O-ring internal radius.

An example of the calculation is as follows:

H = See table E–I for the values for H.
R1 = Plated-through hole radius = .018 inches nominal (0.046 cm).
R2 = O-ring internal radius = 0.075 cm.

$$\text{Area} = (2)(\pi)(0.046)(H) + [(2)(\pi)(0.075)^2 - (2)(\pi)(0.046)^2]$$

$$= (0.22890)(H) + [0.03534 - 0.013295]$$

$$= 0.2890 \text{ cm (H cm)} + [0.022045 \text{ cm}^2]$$

TABLE E–I. SERA plated-through hole example calculation data.

Printed wiring board thickness (inches)	H (centimeters)	Area (centimeters^2)
.020	0.0508	0.0367
.030	0.0762	0.0441
.040	0.1016	0.0514
.050	0.1270	0.0587
.060	0.1524	0.0661
.070	0.1778	0.0734
.080	0.2032	0.0808
.090	0.2286	0.0881
.100	0.2540	0.0955
.110	0.2794	0.1028

E.5.4 Evaluation of test data. The change in reduction voltage shall be plotted versus the charge density (current density x time). This SERA curve generated shall be differentiated and then incorporate the following moving window average, curve smoothing function:

$$V(n) = \text{SUM } [V(n-5) \text{ through } V(n+5)] / 11$$

The following eight SERA parameters shall be calculated from the differentiated and smoothed SERA curve using the following threshold limits listed below. Figure E–2 illustrates these parameters and threshold limits on an example SERA curve.

1. Voc = The final open circuit voltage measured for the SERA differentiated/smoothed curve.
2. Q1 = The area under the curve defined by: Nmin1 threshold value (defined constant value).
3. V2 = The voltage on the differentiated/smoothed curve defined by: (Nmin3 + Nmin1 threshold values) / 2.
4. Q2 = The area under the curve defined by: Nmin3 threshold value – Nmin 1 threshold value.
5. V3 = The voltage on the differentiated/smoothed curve defined by: (Nmin5 + Nmin3 threshold value)/2.
6. Q3 = The area under the curve defined by: Nmin5 threshold value – Nmin3 threshold value.

7. Vf = Most negative reduction voltage measured for the SERA differentiated/smoothed curve.

8. Qt = Total reduction charge (summation of Q1 + Q2 + Q3) for the SERA differentiated/smoothed curve.

9. Threshold constraints:

   a. Constant = First point on curve for measured voltage before applying current.

   b. Nmin1 = First point on curve where measured voltage < –0.85 volts.

   c. Nmin3 = Minimum calculated dVoltage between N1 and N2.

      (1) N1 = First point between Nmin1 and N2 where calculated Dvoltage < –0.003 volts.

      (2) N2 = Last point on curve where measured voltage < –1.3 volts.

   d. Nmin5 = Last point on curve where calculated Dvoltage < –1.3 volts.

Unless otherwise agreed upon by the printed wiring board fabricator and user, the SERA parameter for V2 shall meet the minimum acceptable value listed in table E–II. The other seven SERA parameters shall be within the ranges listed in table E–III for a RMA flux in accordance with J-STD-004. The printed wiring board soldering performance in the manufacturing process will be directly related to the specific flux used in the soldering process. It is the printed wiring board users responsibility to document the critical SERA parameter levels for other specific flux systems.

TABLE E–II. Minimum acceptable V2 value.

SERA parameter	Minimum acceptable value
V2	Equal to or more positive than –1.07 V

TABLE E–III. SERA values for RMA flux in accordance with J-STD-004.

SERA parameter	Minimum acceptable value
Voc	–0.461 to –0.613 V
Q1	0.0 to +1.312 mC/cm^2
Q2	0.0 to +3.823 mC/cm^2
Q3	0.0 to +3.299 mC/cm^2
V3	–1.29 to –1.412 V
Vf	–1.365 to –1.466 V
Qt	+2.005 to +5.985 mC/cm^2

E.5.5 Proper post-test preparation of SERA system.

a. Shut off inert gas flow into system.

b. Shut off digital multimeter and programmable current source.

c. Remove SCE reference electrode, rinse with deionized water and wipe clean with clean soft cloth. Place SCE reference electrode in storage container.

d. Remove reference electrode port and dump out borate buffer solution. Rinse inner and outer surfaces of reference electrode port with deionized water. Replace reference electrode port into system.

e. Remove o-rings and dispose of as required (see E.4.1.2). Rinse test head o-ring seal with deionized water and wipe dry with clean soft cloth.

f. Empty reservoir of borate buffer solution, rinse with deionized water, and refill with buffer solution as required (see E.4.1.1).

E.6. NOTES

E.6.1 Note. The equipment described herein is a result of a United States Army MANTECH Program investment. SERA is a scientific means of measuring solderability of circuit boards and components. The technology is based upon measurements of the type and quantity of oxides using Sequential Electrochemical Reduction Analysis. Rockwell International at Thousand Oaks, CA is the patent holder, and the United States Army MANTECH Program was successful in developing, proving, commercializing, and standardizing the equipment and processes. Round robin tests by a government-industry team were successfully completed in the standardization effort. The United States Army has a perpetual royalty free license, and the equipment is currently on a number of weapons production lines. The technical point of contact for future inquiries should be directed to the sole source supplier listed as follows:

ECI Technology
1 Madison Street
East Rutherford, NJ 07073

Phone: (973) 773–8686
Facsimile: (973) 773–8797
Electronic mail: ecitechnology@eci.com or info@ecitechnology.com
URL: http://www.ecitechnology.com

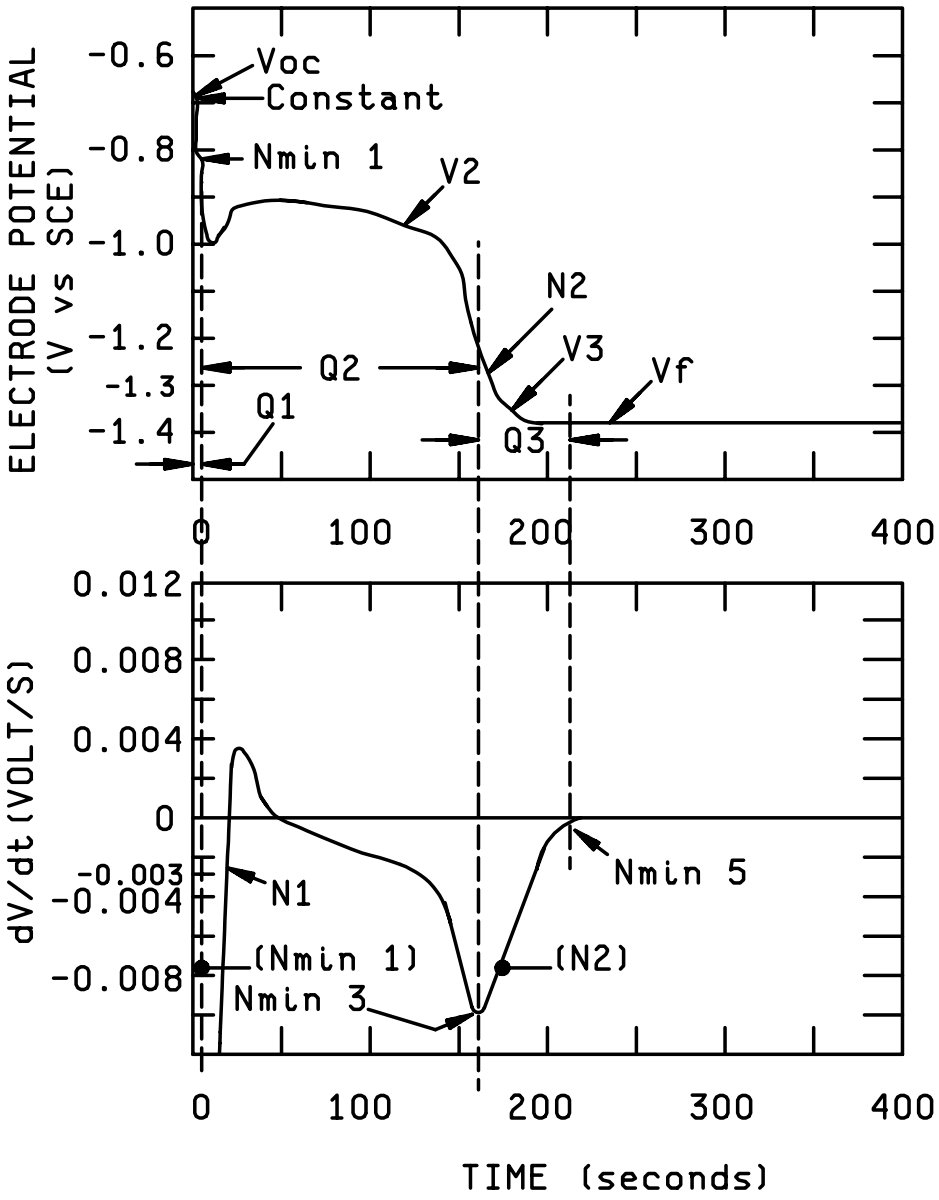

FIGURE E–2. Example SERA differentiated/smoothed curve.

Custodians:
Army – CR
Navy – EC
Air Force – 11
DLA – CC

Review activities:
Army – AR, MI
Navy – AS, CG, MC, OS, SH, TD
Air Force – 16, 19, 99
NSA – NS

Preparing activity:
DLA – CC

(Project 5998–0126)

NOTE: The activities listed above were interested in this document as of the date of this document. Since organizations and responsibilities can change, you should verify the currency of the information above using the ASSIST Online database at http://assist.daps.dla.mil.