INCH-POUND
MIL-PRF-49470B
13 January 2003
SUPERSEDING
MIL-PRF-49470A
11 January 2000

PERFORMANCE SPECIFICATION

CAPACITOR, FIXED, CERAMIC DIELECTRIC, SWITCH MODE POWER SUPPLY (GENERAL PURPOSE AND TEMPERATURE STABLE), STANDARD RELIABILITY AND HIGH RELIABILITY, GENERAL SPECIFICATION FOR

This specification is approved for use by all Departments and Agencies of the Department of Defense.

1. SCOPE

1.1 Scope. This specification covers the general requirements for general purpose (BQ, BR, and BX characteristics) and temperature stable (BP characteristic) ceramic capacitors for use in switch mode power supplies. Two product levels are offered: B level (standard reliability) and T level (high reliability). An acceleration factor of 8:1 has been used to relate life test data obtained at 200 percent of rated voltage at maximum rated temperature to rated voltage at rated temperature.

1.2 Classification. Capacitors covered by this specification should be classified by the style, as specified (see 3.1).

1.2.1 Part or Identifying Number (PIN). Capacitors specified herein (see 3.1); should be identified by a PIN that should consist of the basic number of the performance specification and a coded number. The coded number should provide information concerning the characteristic, specification sheet number, capacitance, capacitance tolerance, voltage, and, where applicable, lead configuration. The PIN should be in the following form with the coded number derived as indicated.

1/ M49470	R	01	474	K	C	N
Performance specification indicating MIL-PRF-49470	Characteristic (1.2.1.1)	Performance specification sheet number (indicating MIL-PRF-49470/1)	Capacitance (1.2.1.2)	Capacitance tolerance (1.2.1.3)	Rated voltage (1.2.1.4)	Configuration (see 1.2.1.5)

1.2.1.1 Characteristic. The characteristic refers to the voltage-temperature limits of the capacitor. The first letter (B) (not shown) identifies the rated temperature range of -55°C to +125°C . The second letter indicates the voltage-temperature limits as shown in table I.

1/ A “T” prefix is used in place of the “M” for T level product.

Beneficial comments (recommendations, additions, deletions) and any pertinent data which may be of use in improving this document should be addressed to: US Army Communications-Electronics Command, ATTN: AMSEL-LC-LEO-E-EP, Fort Monmouth, NJ 07703-5023, by using the Standardization Document Improvement Proposal (DD Form 1426) appearing at the end of the document, or by letter.

TABLE I. Characteristic.

Symbol	Capacitance change with reference to +25°C	
	Step A through step D of table XII	Step E through step G of table XII
P	0 ppm/°C ±30 ppm/°C	0 ppm/°C ±30 ppm/°C
Q	±15 percent	+15, -50 percent
R	±15 percent	+15, -40 percent
X	±15 percent	+15, -25 percent

1.2.1.2 Capacitance. The nominal capacitance value, expressed in picofarads (pF) is identified by a three digit number; the first two digits represent significant figures and the last digit specifies the number of zeros to follow.

1.2.1.3 Capacitance tolerance. The capacitance tolerance is identified by a single letter in accordance with table II.

TABLE II. Capacitance tolerance.

Symbol	Capacitance tolerance
J	±5 percent
K	±10 percent
M	±20 percent

1.2.1.4 Rated voltage. The rated voltage for continuous operation at +125°C is identified by a single letter as shown in table III.

TABLE III. Rated voltage.

Symbol	Rated voltage
A	50
B	100
C	200
E	500

1.2.1.5 Configuration. The configuration is identified by single letter; as shown in table IV (see 3.1).

TABLE IV. Configuration.

Symbol (last digit of PIN)	Lead style	Height profile (Dimension A)	Formed lead length, L (inches)
N	N (straight)	Standard	N/A
L	L (formed)	Standard	.070 ± .010
M	L (formed)	Standard	.045 ± .010
J	J (formed)	Standard	.070 ± .010
K	J (formed)	Standard	.045 ± .010
A	N (straight)	Low	N/A
B	L (formed)	Low	.070 ± .010
D	L (formed)	Low	.045 ± .010
C	J (formed)	Low	.070 ± .010
F	J (formed)	Low	.045 ± .010

2. APPLICABLE DOCUMENTS

2.1 General. The documents listed in this section are specified in sections 3 and 4 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of the documents cited in sections 3 and 4 of this specification, whether or not they are listed.

2.2 Government documents.

2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation (see 6.2).

SPECIFICATIONS

DEPARTMENT OF DEFENSE

MIL-I-46058 - Insulating Compound, Electrical (for Coating Printed Circuit Assemblies).

(See supplement 1 for list of specification sheets.)

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-202 - Test Methods Standard Electronic and Electrical Component Parts.
MIL-STD-790 - Standard Practice for Established Reliability and High Reliability Qualified Products List (QPL) Systems for Electrical, Electronic, and Fiber Optic Parts Specifications.
MIL-STD-1276 - Leads for Electronic Component Parts.

(Unless otherwise indicated, copies of the above specifications, standards, and handbooks are available from the Document Automation and Production Service, Building 4D (DPM-DODSSP), 700 Robbins Avenue, Philadelphia, PA 19111-5094.)

2.3 Non-Government publications. The following documents form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents that are DoD adopted are those listed in the issue of the DoDISS cited in the solicitation. Unless otherwise specified, the issues of documents not listed in the DoDISS are the issues of the documents cited in the solicitation (see 6.2).

ELECTRONIC INDUSTRIES ALLIANCE (EIA)

EIA-469	-	Standard Test Method for Destructive Physical Analysis (DPA) of Ceramic Monolythic Capacitors. (DoD adopted).
EIA-557	-	Statistical Process Control Systems. (DoD adopted).

(Application for copies should be addressed to the Electronic Industries Alliance, 2500 Wilson Boulevard, Arlington, VA 22201-3834.)

2.4 Order of precedence. In the event of a conflict between the text of this document and the references cited herein (except for related associated specifications, specification sheets, or MS standards), the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Specification sheets. The individual item requirements shall be as specified herein and in accordance with the applicable specification sheet. In the event of any conflict between the requirements of this specification and the specification sheet, the latter shall govern.

3.2 Qualification. Capacitors furnished under this specification shall be products that are authorized by the qualifying activity for listing on the applicable qualified products list (QPL) before contract award (see 4.4 and 6.3). In addition, the manufacturer shall obtain certification from the qualifying activity that the QPL requirements of 3.3 and 4.2.1 have been met and are being maintained. Authorized distributors who are approved to MIL-STD-790 distributor requirements by the QPL manufacturer are listed in the QPL.

3.3 QPL system. The manufacturer shall establish and maintain a QPL system for parts covered by this specification. Requirements for this system are specified in MIL-STD-790. In addition, the manufacturer shall establish a Statistical Process Control (SPC) system that meets the requirements of 3.3.1.

3.3.1 SPC system. As part of the overall MIL-STD-790 QPL system, the manufacturer shall establish a SPC system that meets the requirements of EIA-557. Typical manufacturing processes for application of a SPC include raw material mixing and blending, dielectric sheet manufacturing, stacking and electrode printing, laminating and dicing, chip firing, termination, conformal coating, and encapsulation.

3.4 Materials. Materials shall be as specified herein. However, when a definite material is not specified, a material shall be used which will enable the capacitors to meet the performance requirements of this specification. Acceptance or approval of any constituent material shall not be construed as a guarantee of the acceptance of the finished product.

3.5 Interface and physical dimension requirements. Capacitors shall meet the interface and physical dimensions specified (see 3.1).

3.5.1 Dielectric parameters. Capacitors supplied to this specification shall have a minimum dielectric thickness of 0.8 mil for 50 volt rated capacitors or 1 mil for capacitors with ratings above 50 volts. Dielectric thickness is the actual measured thickness of the fired ceramic dielectric layer. Voids, or the cumulative effect of voids, shall not reduce the total dielectric thickness by more than 50 percent (see figure 1).

3.5.2 Lead attachment. When solder is utilized to attach the lead frame to the chip capacitor, the solder shall have a liquidus temperature of 260°C or greater.

FIGURE 1. Dielectric parameters.

3.5.3 Terminal lead finish. The terminal lead finish shall be in accordance with code 32 or code 52 of MIL-STD-1276 (NOTE: The 200 microinch maximum dimension for code 52 is not applicable).

3.5.3.1 Solder dip (retinning). The manufacturer may solder dip/retin the leads of capacitors supplied to this specification provided the solder dip process (see appendix) has been approved by the qualifying activity.

3.5.3.2 Tin plated finishes. Tin plating is prohibited as a final finish or as an undercoat. Tin-lead (Sn-Pb) finishes are acceptable provided that the minimum lead content is 3 percent (see 6.5).

3.6 Nondestructive internal examination (T level product only). Prior to assembly, all chip capacitors shall be subjected to ultrasonic examination or some other method of nondestructive internal examination approved by the qualifying activity. When capacitors are examined as specified in 4.8.1, there shall be no capacitors delivered that show unacceptable responses as specified in EIA-469.

3.7 Chip level DPA (T level product only). When examined as specified in 4.8.2, chip capacitors shall meet the defect criteria of EIA-469. The EIA-469 delamination criteria shall be replaced with the following:

a. Any single delamination of an interface of material layers exceeding 20 percent of the overall interface (pertaining to the overall chip element length or width), and exceeding .005 inch (0.13 mm).

b. Any single delamination of an interface of material layers, in the active area, which exceeds .005 inch (0.13 mm), and displaces adjacent dielectric layers by more than 50 percent of the average nominal dielectric thickness.

c. Any knitline delamination which exceeds 20 percent of the length of the knitline interface (end margin length) or which exceeds .010 inch (0.25 mm), whichever is smaller.

d. Any delamination in any material interface of a side margin.

NOTE: Delaminations or longitudinally migrating voids within a dielectric material layer may be treated as delaminations at material interfaces; or, they may be treated as dielectric voids, in which case the zone of interest must include all of the migratory segments (see figures EIA-469 D.1 and D.2).

3.8 In-process visual examination. When capacitors are inspected as specified in 4.8.3, no device shall be acceptable that exhibits the following:

3.8.1 Ceramic body defects.

a. Cracks or pre-chipouts.

b. Exposed electrodes.

c. Delaminations.

d. Electrodes visible in chipouts.

e. Chipouts longer than 30 percent of each axis or longer than .100 inch (2.54 mm), whichever is less.

f. Lifted terminations.

3.8.2 Lead attachment defects.

a. Exposed electrodes.

b. Solder balls or conductive epoxy particles.

c. Exposed base metal on the lead frame that exceeds 5 percent of the total solderable area.

d. Less than or equal to 80 percent solder attachment.

e. Fractured solder.

f. Bent, twisted or fractured leads.

g. Residual flux.

3.9 Thermal shock and voltage conditioning. When tested as specified in 4.8.5, capacitors shall withstand the extremes of high and low temperature without visible damage and meet the following requirements:

Insulation resistance (at +125°C)	As specified in 3.10.
Dielectric withstanding voltage (at +25°C)	As specified in 3.11.
Insulation resistance (at +25°C)	As specified in 3.10.
Dissipation factor (at +25°C)	As specified in 3.12.
Capacitance (at +25°C)	Shall be within the tolerance specified (see 3.1).

3.10 Insulation resistance. When measured as specified in 4.8.11, the insulation resistance shall not be less than the following:

At +25°C, rated voltage; 100,000 megohms or 1,000 megohm-μF, whichever is less.

At +125°C, rated voltage: 10,000 megohms or 100 megohm-μF, whichever is less.

3.11 Dielectric withstanding voltage. When tested as specified in 4.8.8, there shall be no evidence of breakdown or visible evidence of arcing or sparking.

3.12 Dissipation factor. When determined as specified in 4.8.7, the dissipation factor shall be 0.15 percent maximum for the BP characteristic and 2.5 percent maximum for all other characteristics.

3.13 Capacitance. When measured as specified in 4.8.6, the capacitance shall be within the specified tolerance (see 3.1).

3.14 Barometric pressure. Capacitors shall withstand the dc potential specified in 4.8.9 without flashover or damage.

3.15 Solderability. When capacitors are tested as specified in 4.8.12, the dipped surface of the leads shall be at least 95 percent covered with a new, smooth, solder coating. The remaining 5 percent may contain only small pinholes or rough spots; these shall not be concentrated in one area. All pins are common per side. For inspection purposes, all pins per side are considered as one lead. Bare base metal where the solder dip failed to cover the original coating is an indication of poor solderability and shall be cause for failure. In case of dispute, the percent of coverage with pinholes or rough spots shall be determined by actual measurement of these areas, as compared to the total area.

3.16 Voltage-temperature limits. The capacitance change over the range of temperatures specified in 4.8.13 shall not exceed the limits specified (see 3.1). The capacitance value obtained in step C of table XII shall be considered as the reference point.

3.17 Vibration, high frequency. When capacitors are tested as specified in 4.8.14, there shall be no intermittent contacts of 0.5 millisecond (ms) or greater duration, open-circuiting or short-circuiting, or evidence of mechanical damage.

3.18 Immersion. When tested as specified in 4.8.15, capacitors shall meet the following requirements:

Visual examination	No mechanical damage. Marking shall remain legible.
Dielectric withstanding voltage	As specified in 3.11.
Insulation resistance	Not less than 50 percent of the initial requirement.
Capacitance	Change not to exceed ±3 percent of initial measured value for the BP characteristic or ±10 percent for all other characteristics.
Dissipation factor (at +25°C)	Shall not exceed initial limits.

3.19 Shock, specified pulse. When tested as specified in 4.8.16, there shall be no momentary or intermittent contact of 0.5 ms or greater duration, open-circuiting or short-circuiting, or other evidence of breakdown, arcing, and mechanical damage.

3.20 Resistance to soldering heat. When tested as specified in 4.8.17, capacitors shall meet the following requirements:

Insulation resistance at +25°C	Not less than the initial 25°C requirement.
Capacitance	Shall change not more than ±3 percent for the BP characteristic or -5 percent to +15 percent for all other characteristics.
Dissipation factor	Shall not exceed the initial limits.

3.21 Moisture resistance. When tested as specified in 4.8.18, capacitors shall meet the following requirements:

Visual examination	No mechanical damage. Marking shall remain legible.
Dielectric withstanding voltage	As specified in 3.11.
Insulation resistance	Not less than 30 percent of the initial +25°C requirement for the BP characteristic; not less than 10 percent of the initial +25°C requirement for all other characteristics.
Capacitance	Change not to exceed ±3 percent from initial measured value for the BP characteristic or ±10 percent from the initial measured value for all other characteristics.
Dissipation factor	As specified in 3.12.

3.22 DPA (T level only). When inspected as specified in 4.8.19, there shall be no evidence of capacitor cracking.

3.23 Resistance to solvents. When capacitors are tested as specified in 4.8.20, there shall be no evidence of mechanical damage and the marking shall remain legible.

3.24 Terminal strength. When capacitors are tested as specified in 4.8.10, there shall be no loosening or rupturing of the terminals.

3.25 Humidity, steady-state, low voltage (T level only). When tested as specified in 4.8.21, capacitors shall meet the following requirements:

Visual examination	There shall be no mechanical damage, and marking shall remain legible.
IR (at +25°C)	Shall meet the initial 25°C requirement specified in 3.10.
Capacitance change (BQ, BR and BX)	Shall not change more than ±10 percent from the initial measured value.
Capacitance change (BP)	Shall not change more than ±0.3 percent of the nominal value or 0.3 pF, whichever is greater, from the initial measured value.

3.26 Life (at +125°C). When tested as specified in 4.8.22, capacitors shall meet the following requirements:

Insulation resistance (at +125°C)	As specified in 3.10.
Visual examination	No mechanical damage. Marking shall remain legible.
Insulation resistance (at +25°C)	As specified in 3.10.
Capacitance	Shall not change more than ±3 percent for the BP characteristic or ±20 percent for all other characteristics.
Dissipation factor	As specified in 3.12.

3.27 Low temperature storage. When tested as specified in 4.8.23, capacitors shall withstand the low temperature as specified without evidence of mechanical damage.

3.28 Marking. Capacitors shall be marked as specified herein. Paper labels shall not be used. Other markings that in any way interfere with, obscure, or confuse those specified herein, are prohibited. Each capacitor shall be legibly marked with smear-resistant ink that will withstand the environmental conditions specified herein. At the option of the manufacturer, capacitors may be laser marked. The marking shall remain legible after all tests. Additional marking is allowed provided it does not interfere with the required marking.

3.28.1 Marking legibility (laser marking only). When tested as specified in 4.8.4.1, the marking shall remain legible.

3.28.2 Full marking. Capacitors shall be marked with at least the "JAN" or "J" marking, date code, manufacture's name or trademark or Commercial and Government Entity (CAGE) code, and capacitance and capacitance tolerance codes, in accordance with the following examples. The date code shall consist of the year and week. For example: The third week of 1996 would be 9603 for a 4-digit date code or 603 for a 3-digit date code. At the option of the manufacturer, the date code may be placed on a separate line.

Case codes 1, 2, and 6 shall be marked with a complete PIN, "JAN" brand, 4-digit date code, the manufacturer's name or trademark or CAGE code, the capacitance value, and the rated voltage. These shall be marked on the top of the horizontally stacked styles or on one side of the vertically stacked styles.

Case codes 4 and 5 shall be marked with the following sequence of information:

	Case code 4 or 5 example
"J" brand (1 digit), product level designator ("B" or "T")	JT
Manufacturer's identification (1 to 5 digits)	12345
Capacitance code (3 digits) and capacitance tolerance (1 digit)	106K
Date code (3 or 4 digits)	9603

Case code 3 shall either be fully marked or partially marked like case code 4 or 5 parts, at the option of the manufacturer.

3.28.3 Substitution of capacitance tolerance, voltage and level. Parts qualified and marked to tighter capacitance tolerance or higher rated voltage or higher product level are substitutable, with procuring agency approval, for parts ordered to looser capacitance tolerance, lower rated voltage, or lower product level, provided all other values, such as case size, characteristic, and leads are the same. Unless specified in the contract or order (see 6.2), the substitutable parts shall not be remarked, the lot date code on the parts are unchanged, and the workmanship criteria is met.

3.28.4 JAN and J marking. The United States Government has adopted, and is exercising legitimate control over the certification marks "JAN" and "J", respectively, to indicate that items so marked or identified are manufactured to, and meet all the requirements of specifications. Accordingly, items acquired to and meeting all of the criteria specified herein and in applicable specification, shall bear the certification mark "JAN" except that items too small to bear the certification mark "JAN" shall bear the letter "J". The "JAN" or "J" shall be placed immediately before the PIN except that if such location would place a hardship on the manufacturer in connection with such marking, the "JAN" or "J" may be located on the first line above or below the PIN. Items furnished under contracts or orders which either permit or require deviation from the conditions or requirements specified herein and in applicable specifications shall not bear "JAN" or "J". In the event an item fails to meet the requirements of this specification and the applicable specification sheets or associated specifications, the manufacturer shall remove completely the military PIN and the "JAN" or the "J" from the sample tested and also from all items represented by the sample. The "JAN" or "J" certification mark shall not be used on products acquired to contractor drawings or specifications. The United States Government has obtained Certificate of Registration Number 504,860 for the certification mark "JAN" and Registration Number 1,586,261 for the certification mark "J".

3.29 Recycled, recovered, or environmentally preferable materials. Recycled, recovered, or environmentally preferable materials should be used to the maximum extent possible provided that the material meets or exceeds the operational and maintenance requirements, and promotes economically advantageous life cycle costs.

3.30 Workmanship. Capacitors shall be processed in such a manner as to be uniform in quality when using 2X minimum to 4X maximum magnification. External leads shall not exhibit cuts, nicks, or scrapes exceeding 10 percent of the length of the leads. The surface of the lead may exhibit bare base metal on the edges and cut ends of the pins but not on the flat portion of the leads. These capacitor leads are not expected to be solderable above the seating plane for unencapsulated or conformally coated parts or solderable within .050 inch (1.27 mm) of the seating plane for encapsulated parts (see 3.1).

4. VERIFICATION

4.1 Classification of inspections.

a. Qualification inspection (see 4.4).

b. Verification of qualification (see 4.5).

c. In-process inspection and conformance inspection (see 4.6).

d. Group B inspection (see 4.7).

4.2 Reliability and quality.

4.2.1 QPL system. The manufacturer shall establish and maintain a QPL system in accordance with 3.3. Evidence of such compliance is a prerequisite for qualification and retention of qualification.

4.2.2 SPC. A SPC program shall be established and maintained in accordance with EIA-557. Evidence of such compliance shall be verified by the qualifying activity as a prerequisite for qualification and retention of qualification.

4.3 Inspection conditions and methods.

4.3.1 Conditions. Unless otherwise specified herein, all inspections shall be made in accordance with the "GENERAL REQUIREMENTS" of MIL-STD-202 except relative humidity shall not exceed 75 percent. Accuracy of all test voltage measurements shall be within ±2.0 percent of the specified voltage.

4.3.2 Methods.

4.3.2.1 Reference measurements. When requirements are based on comparative measurements made before and after conditioning, the reference measurement shall be considered the last measurement made at +25°C ±3°C prior to conditioning. Unless reference measurements have been made within 30 days prior to the beginning of conditioning, they shall be repeated.

4.3.3 Power supply. The power supply used for life testing shall have a regulation of ±2 percent or less of the specified test voltage.

4.4 Qualification inspection. Qualification inspection shall be performed at a laboratory acceptable to the Government (see 6.3), on sample units produced with equipment and procedures normally used in production.

4.4.1 Sample size. The number of capacitors to be submitted for qualification inspection shall be as specified in table V and in the appendix of this specification. Each capacitor style shall be qualified separately.

4.4.2 Test routine. Sample units shall be subjected to the qualification inspection specified in table V, in the order shown. All sample units shall be subjected to the inspection of group I and group II. The sample shall then be divided as specified in table V for group III through group VIII, and subjected to the tests for their particular group.

4.4.3 Failures. Failures in excess of those allowed in table V shall be cause for refusal to grant qualification approval.

4.5 Verification of qualification. Every 6 months, the manufacturer shall provide verification of qualification to the qualifying activity. Continuation of qualification shall be based on meeting the following requirements:

a. MIL-STD-790 program.

b. The capacitor design, construction, basic materials or critical processes have not been modified without prior approval from the qualifying activity.

c. Lot rejection for group A inspection does not exceed 10 percent or one lot, whichever is greater.

d. Group B inspection.

TABLE V. Qualification inspection.

Inspection	Requirement paragraph	Test method paragraph	Number of sample units to be inspected	Number of defectives permitted 1/
Group I Thermal shock and voltage conditioning	3.9	4.8.5	All units	Not Applicable
Group II 2/ Visual and mechanical examination: Material Physical dimensions Interface requirements (other than physical dimensions) Marking Workmanship	 3.4 3.1 3.5 and 3.5.1 3.28 3.30	4.8.4	3/ 67 (T level) 3/ 55 (B level)	1
Group III Low temperature storage Barometric pressure Terminal strength	 3.27 3.14 3.24	 4.8.23 4.8.9 4.8.10	6	1
Group IV Voltage-temperature limits Vibration, high frequency Immersion	 3.16 3.17 3.18	 4.8.13.1 4.8.14 4.8.15	12	1
Group V Shock, specified pulse Resistance to soldering heat Moisture resistance	 3.19 3.20 3.21	 4.8.16 4.8.17 4.8.18	12	1
Group VI DPA (T level only)	 3.22	 4.8.19	6	0
Group VII Humidity, steady state, low voltage (T level only)	 3.25	 4.8.21	6	0
Group VIII Life	 3.26	 4.8.22	24	1

1/ A sample unit having one or more defects will be charged as a single defective.
2/ Nondestructive examinations and tests.
3/ One additional sample unit is included in each sample of 67/55 sample units to permit substitution for the permitted defective in group II.

4.6 In-process inspection and conformance inspection.

4.6.1 In-process inspection. Each production lot shall be inspected as individual chips prior to assembly and as stacked assemblies, after attachment of the termination lead frame, in accordance with table VI.

TABLE VI. In-process inspection.

Inspection	Requirement paragraph	Test method paragraph	Sample size	
			Chips	Stacked assembly
Nondestructive internal examination (T level only)	3.6	4.8.1	100%	N/A
Chip level DPA (T level only)	3.7	4.8.2	see table VII	N/A
In-process visual examination	3.8	4.8.3	100%	100%

TABLE VII. Chip level destructive physical analysis sample size.

Lot size	Minimum sample size Case codes 1, 2, 6 1/	Minimum sample size Case codes 3, 4, 5 2/	Accept	Reject
1 – 500	7	14	0	1
501 – 10000	16	32	1	2
10001 – 35000	25	50	2	3
35001 – 500000	40	80	3	4

1/ Case codes 1, 2, and 6 parts require 2 cuts: one cut at approximately 25 percent from top of part and one cut at approximately 25 percent from bottom of part.
2/ Case codes 3, 4, and 5 parts require one cut at location determined by manufacturer.

4.6.2 Conformance inspection. Inspection of B level product for delivery shall consist of group A inspection. Inspection of T level product for delivery shall consist of in-process inspection, group A, and subgroups 4 and 5b of group B.

4.6.2.1 Inspection and production lot.

4.6.2.1.1 Inspection lot. An inspection lot shall consist of all capacitors of the same voltage-temperature characteristic, produced under essentially the same conditions with the same basic materials, and offered for inspection in the same week. The capacitance values and voltages produced shall be represented in the lot in approximately the ratio of production. The following styles may be combined:

Group	Style
1	PS01, PS02, PS03 (horizontally stacked).
2	PS04, PS05, PS06 (vertically stacked).

4.6.2.1.2 Production lot. A production lot shall consist of all capacitors of the same style, voltage rating, nominal capacitance value, voltage-temperature characteristic, and termination finish. Manufacture of all parts in the lot shall have been started, processed, assembled, and tested as a group. Lot identity shall be maintained throughout the manufacturing cycle. In addition, for T level capacitors, a production lot shall consist of a single chip lot. A single chip lot is one that is processed from a single lot of dielectric powder in a continuous basis.

4.6.3 Group A inspection. Group A inspection shall consist of the inspections specified in table VIII.

TABLE VIII. Group A inspection.

Inspection	Requirement paragraph	Test method paragraph	Sampling procedure	
Subgroup 1 Thermal shock and voltage conditioning 1/	3.9	4.8.5	100% inspection	
Subgroup 2 Visual and mechanical examination: Material Physical dimensions Interface requirements (other than physical dimensions) Marking 2/ Workmanship	3.4 3.1 3.5 and 3.5.1 3.28 3.30	4.8.4	13 samples 0 failures	
Subgroup 3 Solderability 3/	3.15	4.8.12	B Level 5 samples 0 failures	T level 3 samples 0 failures
Subgroup 4 DPA (T level only)	3.22	4.8.19	3 samples 0 failures	

1/ Post checks are required (see 3.9).
2/ Marking defects are based on visual examination only. Any subsequent electrical defects shall not be used as a basis for determining marking defects.
3/ The manufacturer may request the deletion of the subgroup 3 solderability test, provided an inline or process control system for assessing and assuring the solderability of leads can be validated and approved by the qualifying activity. Deletion of the test does not relieve the manufacturer from meeting this test requirement.

4.6.3.1 Subgroup 1 tests. Subgroup 1 tests shall be performed on a production lot basis on 100 percent of the product supplied under this specification. Capacitors failing the tests of subgroup 1 shall be removed from the lot. For B level capacitors, if, during the 100 percent inspection, screening requires that more than 10 percent of the capacitors or 1 capacitor, whichever is greater, be discarded, the entire lot shall be rejected. For T level capacitors, if screening requires more than the PDA allowed in table IX, the entire lot shall be rejected.

4.6.3.2 Manufacturer's production inspection. If the manufacturer performs tests similar to those specified in subgroup 1, table VIII as the final step of their production process, group A, subgroup 1 inspection may be waived and the data resulting from the manufacturer's production tests may be used instead. Authority to waive the subgroup 1 inspections shall be granted by the qualifying activity only. The following criteria must be complied with:

a. Tests conducted by the manufacturer during production shall be clearly identical to, or more stringent than, that specified for subgroup 1.

b. Manufacturer subjects 100 percent of the product supplied under this specification to their production tests.

c. The parameters measured and the failure criteria shall be the same as, or more stringent than, those specified herein.

d. The lot rejection criteria is the same as, or more stringent than, that specified herein.

e. The manufacturer shall make available all information concerning the test procedures and instrumentation used in their production tests.

f. Once approved, the manufacturer shall not change the test procedures or criteria without prior notification of, and concurrence by, the qualifying activity.

4.6.3.3 Rejected lots. Production lots exceeding the PDA of group A, subgroup 1 inspection shall be rejected and shall not be resubmitted.

TABLE IX. T level PDA for subgroup 1, group A inspection.

Case code	PDA last 48 hours during voltage conditioning	PDA overall
1	1% or 1 unit, whichever is greater	8% or 1 unit, whichever is greater
2	1% or 1 unit, whichever is greater	8% or 1 unit, whichever is greater
3	1% or 1 unit, whichever is greater	8% or 1 unit, whichever is greater
4	.5% or 1 unit, whichever is greater	5% or 1 unit, whichever is greater
5	.5% or 1 unit, whichever is greater	5% or 1 unit, whichever is greater
6	1% or 1 unit, whichever is greater	8% or 1 unit, whichever is greater

4.6.3.4 Subgroup 2.

4.6.3.4.1 Sampling plan. Subgroup 2 tests shall be performed on an inspection lot basis for B level capacitors and a production lot basis for T level capacitors. In the event of one or more failures, the lot shall be rejected.

4.6.3.4.2 Rejected lots. The rejected lots shall be segregated from new lots and those that have passed inspection. Rejected lots shall be 100 percent reworked or scrapped. The rejected lot may be rescreened and the defects removed. The lot may then be resubmitted to the sample plan. If one or more defects of the same type are found in this second sample, the lot is rejected and shall not be supplied to this specification. If another defect of a different type is found in the second sample, a rescreen for that defect is also permitted.

4.6.3.5 Subgroup 3.

4.6.3.5.1 Sampling plan. Solderability tests shall be performed on an inspection lot basis for B level capacitors and on a production lot basis for T level capacitors. The samples shall be selected randomly and subjected to the solderability test. The manufacturer may use electrical rejects from the subgroup 1 and subgroup 2 tests for all or part of the samples to be used for solderability testing. If there are one or more defects, the lot shall be rejected.

4.6.3.5.2 Rejected lots. In the event of one or more defects, the manufacturer may use one of the following options to rework the lot:

a. Each production lot that was used to form the failed inspection lot shall be individually submitted to the solderability test as required in 4.6.3.5.1. Production lots that pass the solderability test are available for shipment. Production lots failing the solderability test can be reworked only if submitted to the solder dip procedure in 4.6.3.5.2b.

b. The manufacturer shall submit the failed production lot to a 100 percent solder dip; using an approved solder dip process in accordance with the appendix. Two hundred sample units from this lot shall then be subjected to all group A, subgroup 1, post-electrical tests, with no defects allowed.

(1) If the sample units pass the group A, subgroup 1 post-electrical tests, five additional units shall then be subjected to the solderability test, with no defects allowed. If there are one or more defects, the lot shall be considered rejected and shall not be furnished against the requirements of this specification.

(2) If the sample units fail group A, subgroup 1 post-electrical tests, these tests shall be performed on 100 percent of the lot. The lot must meet the PDA requirements as specified in 4.6.3.1. If the PDA requirements are not met, the lot shall be considered rejected and shall not be furnished against the requirements of this specification. If the PDA requirements are met, five sample units shall be subjected to the solderability testing criteria of 4.6.3.5.2b(1).

4.6.3.5.3 Disposition of samples. The solderability test is considered a destructive test and samples submitted to the solderability test shall not be supplied on the contract or order.

4.6.3.6 Subgroup 4 (T level only).

4.6.3.6.1 Sampling plan. Three samples shall be selected randomly from every production lot and subjected to the DPA test. If there are one or more defects, the lot shall be rejected.

4.7 Group B inspection. Group B inspection shall consist of the tests specified in table X in the order shown, and shall be performed on sample units selected from lots which have passed group A inspection. The tests of subgroups 1, 2, 3, and 5a shall be done on a periodic basis. The tests of subgroup 4 and subgroup 5b shall be done on each T level production lot. For B level product, except where the results of this inspection show noncompliance with the applicable requirements (see 4.7.3), delivery of products which have passed group A inspection shall not be delayed pending the results of this inspection.

4.7.1 Sampling plan.

4.7.1.1 Subgroup 1 through sugbroup 3. The number of sample units required by table X shall be taken from production for the period 12 months after initial qualification and if successfully passed, 24 months thereafter and subjected to the applicable tests for their particular subgroups. Capacitor styles manufactured during that period shall be represented, as far as practical, in at least the approximate ratio of production.

4.7.1.2 Subgroup 4 (T level only). For subgroup 4, the number of sample units required by table X shall be taken from each T level production lot.

4.7.1.3 Subgroup 5a (B level only). For subgroup 5a, the number of sample units required by table X shall be taken from production every 3 months. Horizontal capacitors (styles PS01, PS02, PS03) and vertical capacitors (styles PS04, PS05, PS06) shall be tested separately. Within each category, horizontal and vertical, 2 groups shall be formed:

Group 1 (Case size 3, 4, 5) - Pick the largest case size produced in the following order: Case size 3, 4 and 5. That is, if case size 3 is produced, pick case size 3.

Group 2 (Case size 6, 2, 1) - Pick the largest case size produced in the following order: Case size 6, 2 and 1. That is, if case size 6 is produced, pick case size 6.

Group 1 and group 2 shall each be divided into two voltage temperature limit groups: (BQ, BR and BX) and BP. Six of the largest capacitance value capacitors in the highest voltage range produced and six of the largest capacitance value capacitors in the lowest voltage range produced, in each of the two separate voltage temperature groups, shall be tested. If only one voltage is produced, 12 samples of that voltage shall be tested. The above groups are shown in table XI. No more than one failure is allowed in two consecutive quarters.

4.7.1.4 Subgroup 5b (T level only). For subgroup 5b, the number of sample units required by table X shall be taken from each T level production lot.

TABLE X. Group B inspection. 1/

Inspection	Requirement paragraph	Test method paragraph	Number of sample units to be inspected	Number of defectives permitted 2/	
Subgroup 1 3/ Voltage-temperature limits Resistance to solvents 4/ 5/ Immersion Terminal strength 4/	3.16 3.23 3.18 3.24	4.8.13.2 4.8.20 4.8.15 4.8.10	12	1	6/ 1
Subgroup 2 Resistance to soldering heat Moisture resistance	3.20 3.21	4.8.17 4.8.18	12	1	
Subgroup 3 Marking legibility (laser marking only)	3.28.1	4.8.4.1	6	1	
Subgroup 4 (T level only) Humidity, steady-state, low voltage	3.25	4.8.21	6	0	
Subgroup 5a (B level only) Life	3.26	4.8.22	12	7/ 1	
Subgroup 5b (T level only) Thermal shock and electrical tests Life	3.9 3.26	4.8.5.1 and 4.8.5.3 4.8.22	12	1	

1/ Unless otherwise specified herein, when necessary, mounting of group B samples shall be at the discretion of the manufacturer.
2/ A sample unit having one or more defects shall be charged as a single defective.
3/ Order of tests is at discretion of manufacturer.
4/ Sample size shall be 3 pieces with zero defectives permitted.
5/ When more than one marking type is used, an additional three samples shall be added for each additional marking type (see 3.28).
6/ Total of one defect allowed for combination of subgroup 1, subgroup 2, and subgroup 3 inspections.
7/ No more than 1 failure allowed in two consecutive quarters except if manufacturer is maintaining T level.

TABLE XI. Group B, subgroup 5a test groups.

Horizontal (styles PS01, PS02, PS03)				Vertical (styles PS04, PS05, PS06)			
Case size 3, 4, 5 (choose in order)		Case size 6, 2, 1 (choose in order)		case size 3, 4, 5 (choose in order)		case size 6, 2, 1 (choose in order)	
BQ, BR, BX	BP	BQ, BR, BX	BP	BQ, BR, BX	BP	BQ, BR, BX	BP
6 highest voltage + 6 lowest voltage	6 highest voltage + 6 lowest voltage	6 highest voltage + 6 lowest voltage	6 highest voltage + 6 lowest voltage	6 highest voltage + 6 lowest voltage	6 highest voltage + 6 lowest voltage	6 highest voltage + 6 lowest voltage	6 highest voltage + 6 lowest voltage

4.7.2 Disposition of sample units. Sample units that have been subjected to group B inspection shall not be delivered on the contract.

4.7.3 Noncompliance (B level only). If a sample unit fails to pass group B inspection, the manufacturer shall notify the qualifying activity and cognizant inspection activity of such failure and take corrective action on the materials or processes, or both, as warranted, and on all units of product which can be corrected and which were manufactured under essentially the same conditions, with essentially the same materials and processes, and which are considered subject to the same failure. Acceptance and shipment of the product shall be discontinued until corrective action, acceptable to the Government, has been taken. After the corrective action has been taken, group B inspection shall be repeated on additional sample units (all inspections), or the inspection that the original sample failed, at the option of the qualifying activity. Group A inspection may be reinstituted, however, final acceptance shall be withheld until the group B inspection has shown that corrective action was successful. In the event of failure after reinspection, information concerning the failure and corrective action taken shall be furnished to the cognizant inspection activity and the qualifying activity.

4.8 Methods of examination and test.

4.8.1 Nondestructive internal examination (T level product only) (see 3.6). Prior to assembly, all chip capacitors shall be subjected to ultrasonic examination or some other method of nondestructive internal examination approved by the qualifying activity, which allows the capacitors to meet the requirements of EIA-469.

4.8.2 Chip level DPA (T level product only) (see 3.7). Prior to assembly, chip capacitors selected in accordance with table VI shall be examined for the criteria specified in 3.7.

4.8.3 In-process visual examination (see 3.8).

4.8.3.1 Prior to assembly, all chip capacitors shall be visually examined using 7X to 10X magnification, for the criteria specified in 3.8.1.

4.8.3.2 After assembly, all capacitor stacks shall be visually examined using 7X to 10X magnification, for the lead attachment criteria specified in 3.8.2.

4.8.4 Visual and mechanical examination. All capacitors shall be examined using 7X to 10X magnification to verify that the materials, design, construction, physical dimensions, and marking are in accordance with the applicable requirements (see 3.1, 3.4 through 3.5.1 inclusive, and 3.28). All capacitors shall also be examined using 2X to 4X magnification to verify that workmanship is in accordance with the applicable requirements (see 3.30).

4.8.4.1 Marking legibility (laser marking only, see 3.28.1). Capacitors shall be coated with .005 inch (0.13 mm) minimum of silicone resin insulating compound, type SR of MIL-I-46058. After curing, coated capacitors shall be examined for legibility under normal production room lighting by an inspector with normal or corrected 20/20 vision.

4.8.5 Thermal shock and voltage conditioning (see 3.9). Capacitors shall be subjected to the tests of 4.8.5.1 and 4.8.5.2.

4.8.5.1 Thermal shock. Capacitors shall be tested in accordance with method 107 of MIL-STD-202. The following details shall apply:

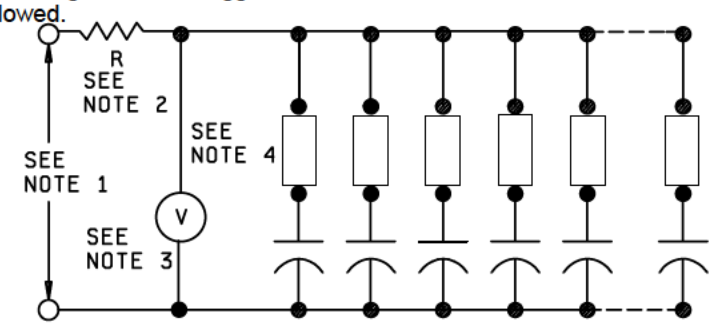
a. Test condition A, except that in step 3, units shall be tested at 125°C.

b. Number of cycles:

Qualification:	T level	100 cycles
	B level	5 cycles
Group A:	T level	20 cycles
	B level	5 cycles
Group B:	T Level	100 cycles

B level N/A

4.8.5.2 Voltage conditioning. The intent of voltage conditioning is that all parts be exposed to a predetermined test voltage ±5 percent, for a defined time and temperature. Voltage conditioning is done to help eliminate infant mortality capacitors from the production lot. All parts offered for electrical testing shall be subjected to the voltage conditioning test in 4.8.5.2.1 for B level or 4.8.5.2.2 for T level, or optional voltage conditioning test in 4.8.5.2.3. It shall be verifiable that all parts offered for electrical tests have been exposed to the required voltage conditioning for the required time duration. See figure 2 for a suggested test circuit. An alternate test circuit can be used, provided the notes of figure 2 are followed.



NOTES:
1. The power supply shall be capable of supplying the required test voltage.
2. The current limiting device shall be a resistor or a fuse. The current shall be limited to no less than 30 milliamperes (mA) and no more than 10 A.
3. There shall be a voltage monitor that will indicate when the applied voltage drops or increases by more than 5 percent, and shut off the test. The resistance of the voltage monitor shall be a minimum of 10X the equivalent resistance of the series resistor and the device under test.
4. Each device under test must have a resistor or fuse in series with it. The value of the resistor shall be such that it does not restrict the power supply's ability to provide the required test voltage to the device under test (±5 percent).

FIGURE 2. Suggested test circuit.

4.8.5.2.1 Voltage conditioning (B level). Voltage conditioning shall consist of applying a minimum of twice the rated voltage (120 percent of rated voltage for 500 volt rated parts) to the unit at the maximum rated temperature +4°C, -0°C for 96 hours minimum. Voltage shall be applied and shall reach maximum value within two minutes maximum. After testing, perform measurements of 4.8.5.3.

* 4.8.5.2.2 Voltage conditioning (T level). Voltage conditioning shall consist of applying a minimum of twice the rated voltage (120 percent of rated voltage for 500 volt rated parts) to the unit at the maximum rated temperature +4°C, -0°C for a minimum 168 hours and a maximum of 264 hours. Voltage conditioning may be terminated at any time during the 168 to 264 hour time interval, provided that the number of failures detected during the last 48 hours of test meets the PDA requirements specified in table IX. Failures shall be determined by +125°C IR failures. +125°C IR measurements should be made at 120 hours, 168 hours, 216 hours, and 264 hours as necessary. Measurements may be made more often or at different times as long as the last 48 hour PDA can be substantiated. Voltage shall be applied and shall reach maximum value within two minutes maximum. After testing, perform measurements of 4.8.5.3.

4.8.5.2.3 Optional voltage conditioning (Capacitors with voltage ratings of 200 volts or less only). The manufacturer, with approval from the qualifying activity, may perform an optional voltage conditioning test instead of the standard voltage conditioning tests of 4.8.5.2.1 or 4.8.5.2.2. All conditions of 4.8.5.2.1 (B level) or 4.8.5.2.2 (T level) apply, with the exception of the voltage applied, the test time, and the time required for meeting the PDA (T level only). The accelerated condition selected for the optional voltage conditioning shall be used for the duration of the test. At no time shall a combination of standard and optional voltage conditioning be allowed on the same samples. The minimum time duration, T(test) minimum, and the time required for meeting the PDA (T level), T(test) PDA, shall be calculated as follows:

$$T_{test}\ (min.) = \frac{1344}{(E_{test} / E_{rated})^3} \qquad T_{test}\ (PDA) = \frac{384}{(E_{test} / E_{rated})^3}$$

Where: $2 \times E_{rated} \le E_{test} \le 4 \times E_{rated}$

E_{test} = Applied voltage

E_{rated} = Rated voltage of the capacitor

T_{test} (min.) = Minimum test time in hours

T_{test} (PDA) = Time required for meeting the PDA

4.8.5.3 Measurements after testing. After completion of the test, the insulation resistance shall be measured at +125°C in accordance with 4.8.11.2. The units shall then be allowed to stabilize at room temperature (+25°C). After stabilization at room temperature, the dielectric withstanding voltage, insulation resistance, capacitance and dissipation factor shall be measured as specified in 4.8.8.1, 4.8.11.1, 4.8.6, and 4.8.7, respectively.

4.8.6 Capacitance (see 3.13). Capacitors shall be tested in accordance with method 305 of MIL-STD-202. The following details and exceptions shall apply:

a. Test frequency: 1 kilohertz ±100 Hz.

b. Voltage: A root-mean-square potential of 1.0 volt ±0.2 volt (open circuit voltage).

NOTE: Following a dielectric withstanding voltage or insulation resistance test, capacitance measurement may be delayed for a period up to 24 hours.

4.8.7 Dissipation factor (see 3.12). The dissipation factor shall be measured with a capacitance bridge or other suitable method at the frequency and voltage specified in 4.8.6a and 4.8.6b. Unless otherwise specified, the inherent accuracy of the measurement shall be ±2 percent of the reading plus 0.1 percent dissipation factor (absolute). Suitable measurement techniques shall be used to minimize errors due to the connections between the measuring apparatus and the capacitor. The dissipation factor shall be measured under the same conditions as capacitance.

4.8.8 Dielectric withstanding voltage (see 3.11).

4.8.8.1 Dielectric. Capacitors shall be tested in accordance with method 301 of MIL-STD-202. The following details shall apply:

a. Magnitude and nature of test voltage: A minimum of 150 percent of the dc rated voltage for 500 volt rated parts, and a minimum of 250 percent of the dc rated voltage for all other voltage ratings.

b. Duration of application of test voltage: 5 seconds ±1 second. The test voltage shall be raised from zero volts to the specified value within 1 second, maximum.

c. Points of application of test voltage: Between the capacitor-element terminals.

d. Limiting value of surge current: Shall be limited to between 30 mA and 50 mA.

e. Examination after test: Capacitors shall be examined for evidence of damage and breakdown.

4.8.8.2 Body insulation (encapsulated styles only, see 3.1). Capacitors shall be tested as specified in 4.8.8.1 with the following exception: Points of application of test voltage-capacitors shall be wrapped with a conductive tape or foil so that the conductive tape or foil shall not be less than .0625 inch (1.59 mm) and more than .125 inch (3.18 mm) away from the lead wires. A dc potential of 1,300 volts shall be applied between the two leads on either side connected together and the tape or foil for a period of 5 seconds ±1 second. The test circuit shall be so arranged that the surge current does not exceed 50 mA.

4.8.9 Barometric pressure (see 3.14). Capacitors shall be tested in accordance with method 105 of MIL-STD-202. The following details and exceptions shall apply:

a. Method of mounting: Securely fastened by their normal mounting means.

b. Test condition: D (100,000 feet) (30.48 km) (0.315 inch (8.00 mm) of mercury).

c. Test during subjection to reduced pressure: A dc potential equal to 80 percent of the dc rated voltage for 500 volt rated parts, and 100 percent of the rated voltage for all other voltage ratings, shall be applied for a period of 5 seconds ±1 second.

d. Points of application: The test voltage shall be applied between the capacitor-element terminals.

e. Surge current: Shall not exceed 50 mA.

f. Examination during and after test: Capacitors shall be visually monitored for evidence of flashover or damage.

4.8.10 Terminal strength (see 3.24). The leads shall be bent 90° away from capacitor body then tested in accordance with method 211 of MIL-STD-202. The following details and exceptions shall apply:

a. Test condition A.

b. Method of holding: Capacitors shall be held by one set of terminals and the loads shall be applied gradually to the other set of terminals. Leads may be trimmed.

c. Applied force: Case codes 1, 2, 3, 4, and 6 - 5 pounds.
Case code 5 - 4 pounds.

d. Examination after test: Capacitors shall be visually examined for evidence of loosening or rupturing of the terminals.

4.8.11 Insulation resistance (see 3.10). Capacitors shall be tested in accordance with method 302 of MIL-STD-202. The vendors may determine criteria tighter than the specification limit to which the capacitors may be screened. Only capacitors that fail the specification limit shall be counted against the PDA. The following details shall apply.

4.8.11.1 Insulation resistance at +25°C.

a. Test potential: Rated voltage minimum.

b. Test temperature: +25°C

c. Special conditions: If a failure occurs at a relative humidity above 50 percent, the insulation resistance may be measured again at any relative humidity less than 50 percent.

d. Points of measurement: Between the mutually insulated points.

4.8.11.2 Insulation resistance at +125°C.

a. Test potential: Rated voltage minimum.

b. Test temperature: +125 ±3°C

c. Special conditions: Capacitors shall have stabilized at +125°C with test voltage applied prior to performing the test.

d. Points of measurement: Between the mutually insulated points.

4.8.12 Solderability (see 3.15). Capacitors shall be tested in accordance with method 208 of MIL-STD-202. The following details shall apply:

a. The capacitors shall be preheated. The preheat shall not exceed 4°C per second. The maximum preheat temperature shall be within 50°C of the solder bath temperature.

b. Number of terminations to be tested: All leads (see 3.1) (All pins are common per side. For inspection purposes, all pins per side are considered as one lead).

c. The leads shall be immersed up to the seating plane for unencapsulated and conformally coated parts, or to within .050 inch (1.27 mm) of the seating plane for encapsulated parts (see 3.1).

4.8.13 Voltage-temperature limits (see 3.16).

4.8.13.1 For qualification inspection. The temperature of each capacitor shall be varied as specified in table XII. Capacitance measurements shall be made at the frequency and voltage specified in 4.8.6a and 4.8.6b. The dc rated voltage need only be applied to the capacitor in each of step E through step G of table XII until voltage stability is reached and the capacitance measurement is made. Capacitance measurements shall be made at each step specified in table XII and at a sufficient number of intermediate points between step B and step G to establish a true characteristic curve. Capacitance measurements at each temperature shall be taken at five-minute intervals and shall be stopped and recorded when two successive readings indicate capacitance change of less than one percent.

4.8.13.2 For quality conformance inspection. Capacitance measurements shall be made as specified in 4.8.13.1, except that the measurements shall be made only for step C, step D, step E, and step G of table XII.

TABLE XII. Voltage-temperature limit cycle.

Step	Voltage, dc	Temperature, °C
A	None	+25 ± 2
B	None	-55 ± 2
C 1/	None	+25 ± 2
D	None	+125 ± 2
E	Rated	+125 ± 2
F	Rated	+25 ± 2
G	Rated	-55 ± 2

1/ Reference point.

4.8.14 Vibration, high frequency (see 3.17). Capacitors shall be tested in accordance with method 204 of MIL-STD-202. The following details and exception shall apply:

a. Mounting: Capacitors shall be rigidly mounted; by the body. Electrical connections to the leads shall be made in such a manner that the leads are not damaged during the vibration test (i.e., external wiring to the capacitor shall be sufficiently supported). The test fixture shall be so constructed as to preclude any resonance within the test range. An examination of the mounting fixture shall be made on a vibrator. If any resonant frequencies are observed, adequate steps must be taken to damp the structure.

b. Electrical load conditions: During the test, a dc potential equal to rated voltage or 200 volts, whichever is less (see 3.1), shall be applied between the terminals of the capacitor element under test.

c. Test condition D: 20 G's.

d. Duration and direction of motion: Three hours in each of three mutually perpendicular planes.

e. Measurements during vibration: During the last cycle in each direction, an electrical measurement shall be made to determine intermittent contacts of 0.5 ms or greater duration, or open-circuiting or short-circuiting.

f. Examination after vibration: Capacitors shall be visually examined for evidence of mechanical damage.

4.8.15 Immersion (see 3.18). Capacitors shall be tested in accordance with method 104 of MIL-STD-202. The following details shall apply:

a. Test condition: B.

b. Examinations and measurements after final cycle: Capacitors shall be visually examined for evidence of mechanical damage and obliteration of marking; dielectric withstanding voltage, insulation resistance at 25°C, capacitance, and dissipation factor shall then be measured as specified in 4.8.8.1, 4.8.11.1, 4.8.6, and 4.8.7, respectively.

4.8.16 Shock, specified pulse (see 3.19). Capacitors shall be tested in accordance with method 213 of MIL-STD-202. The following details shall apply:

a. Mounting: Capacitors shall be rigidly mounted by the body.

b. Test condition I: 100 G's.

c. Measurements during shock: During the last shock in each direction, an electrical measurement shall be made to determine intermittent contacts of 0.5 ms or greater duration, or open-circuiting or short-circuiting.

d. Examination after shock: Capacitors shall be visually examined for evidence of breakdown, arcing, and mechanical damage.

4.8.17 Resistance to soldering heat (see 3.20). Capacitors shall be tested in accordance with method 210 of MIL-STD-202. The following details and exceptions shall apply:

a. The capacitors shall be preheated. The preheat shall not exceed 4°C per second. The maximum preheat temperature shall be within 50°C of the solder bath temperature.

b. Surface oxides and dross shall be skimmed off the solder pot immediately before lead immersion to ensure full and complete heat flow through the leads.

c. Depth of immersion in the molten solder: To a minimum of .050 inch -0 inch, +.020 inch (1.27 mm -0 mm, +0.51 mm) from the capacitor body.

d. Test condition: N lead style - test condition B.
J and L lead styles - test condition I.

e. Measurements after test: Dielectric withstanding voltage, insulation resistance at 25°C, capacitance, and dissipation factor shall be measured as specified in 4.8.8.1, 4.8.11.1, 4.8.6, and 4.8.7, respectively.

f. Internal examination after test: Not required.

4.8.18 Moisture resistance (see 3.21). Capacitors shall be tested in accordance with method 106 of MIL-STD-202. The following detail and exceptions shall apply:

a. Initial measurements: Not applicable.

b. Number of cycles: Twenty continuous cycles.

c. Step 7b: Not applicable.

d. Loading: During the first ten cycles only, a dc potential of 100 volts or rated voltage, whichever is less, shall be applied across the capacitor terminals. There shall be a voltage monitor that will indicate when the applied voltage drops or increases by more than 5 percent, and shut off the test. The resistance of the voltage monitor shall be a minimum of 10X the equivalent resistance of the series resistor and the device under test.

* e. Examinations and final measurement: On completion of step 6 of the final cycle, capacitors shall be conditioned at 25°C ±5°C and a maximum relative humidity of 55 percent for a period of 18 hours minimum, 24 hours maximum, and shall be visually examined for evidence of mechanical damage and obliteration of marking; dielectric withstanding voltage, insulation resistance at 25°C, capacitance, and dissipation factor shall then be measured as specified in 4.8.8.1, 4.8.11.1, 4.8.6, and 4.8.7, respectively.

4.8.19 DPA (T level only) (see 3.22). Capacitors shall be examined as specified in EIA-469 for the criteria specified in 3.22.

4.8.20 Resistance to solvents (see 3.23). Capacitors shall be tested in accordance with method 215 of MIL-STD-202. The following details shall apply:

a. The marked portion of the capacitor body shall be brushed.

b. Capacitors shall be visually examined for evidence of mechanical damage and obliteration of marking.

4.8.21 Humidity, steady state, low voltage (see 3.25). Capacitors shall be tested in accordance with method 103, condition A of MIL-STD-202. The following details and exceptions shall apply:

Note: At no time during test shall voltage greater than 1.55 volts be applied to any capacitor under test.

a. Initial measurements: Capacitance shall be measured in accordance with 4.8.6.

b. Tests: Capacitors shall be subjected to an environment of +85°C with 85 percent relative humidity for 240 hours minimum. Cycling shall not be performed. A dc potential of 1.3 ± 0.25 volts shall be applied continuously through a 100 kilohm resistor.

c. Final measurements: On completion of test, remove the capacitors from the chamber and allow 3 hours, 30 minutes, ±30 minutes for drying and stabilization at 25°C before performing insulation resistance (through a 100 kilohm resistor at 1.3 ± 0.25 volts) and capacitance in accordance with 4.8.11.1 and 4.8.6, respectively. The capacitors shall then be examined for evidence of mechanical damage and obliteration of marking.

4.8.22 Life (at +125°C) (see 3.26). Capacitors shall be tested in accordance with method 108 of MIL-STD-202. The following details and exceptions shall apply:

a. Distance of temperature measurements from specimens, in inches: Not applicable.

b. Operating conditions: Capacitors shall be subjected to 125°C at a minimum of 120 percent of the rated dc voltage for 500 volt rated parts, and a minimum of 200 percent of dc rated voltage for all other voltage ratings. Voltage shall be applied and shall reach maximum value within two minutes maximum. Test circuitry shall be the same as that required for voltage conditioning (see 4.8.5.2).

c. Length of test:

T level qualification:	4,000 hours minimum.
B level qualification:	1,000 hours minimum.
B level and T level group B:	1,000 hours minimum.

d. Measurements during and after exposure:

T level product: Insulation resistance shall be measured during exposure to the high test temperature at 250 hours, 1000 hours, and 4000 hours as specified in 4.8.11.2. Measurements may be taken at additional times. At the option of the manufacturer, the units may be immediately transferred (period of transfer not to exceed 15 minutes) to another chamber maintained at the same temperature for the purpose of measuring insulation resistance. The insulation resistance measurement shall be made only after the units have stabilized at the test temperature. The capacitors shall then be returned to the inspection conditions specified in 4.3 and shall be visually examined for evidence of mechanical damage and obliteration of marking; insulation resistance, capacitance, and dissipation factor, shall be measured as specified in 4.8.11.1, 4.8.6, and 4.8.7, respectively.

B level product: At the conclusion of this test and while the capacitors are at the high test temperature, the insulation resistance shall be measured as specified in 4.8.11.2. At the option of the manufacturer, the units may be immediately transferred (period of transfer not to exceed 15 minutes) to another chamber maintained at the same temperature for the purpose of measuring insulation resistance. The insulation resistance measurement shall be made only after the units have stabilized at the test temperature. The capacitors shall then be returned to the inspection conditions specified in 4.3 and shall be visually examined for evidence of mechanical damage and obliteration of marking; insulation resistance, capacitance, and dissipation factor, shall be measured as specified in 4.8.11.1, 4.8.6, and 4.8.7, respectively.

4.8.23 Low temperature storage (see 3.27). Capacitors shall be subjected to exposure at -65°C +0°C, -3°C for a period of 8 hours, minimum.

5. PACKAGING

5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When actual packaging of materiel is to be performed by DoD personnel, these personnel need to contact the responsible packaging activity to ascertain requisite packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activity within the Military Department or Defense Agency, or within the Military Department's System Command. Packaging data retrieval is available from the managing Military Departments or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but not mandatory.)

6.1 Intended use. These capacitors are primarily designed for use where a small physical size with comparatively large electrical capacitance and high insulation resistance is required. General purpose (BQ, BR, and BX characteristics) ceramic capacitors are not intended for frequency-determining or precision circuits but are suitable for use as by-pass, filter, and noncritical coupling elements in high-frequency circuits. All of these applications are of the type where dissipation factor is not critical and moderate changes due to temperature, voltage, and frequency variations do not affect the proper functioning of the circuit. BP characteristic ceramic capacitors are for use in critical frequency determining applications, timing circuits, and other applications where absolute stability is required. Two product levels are offered: B level (standard reliability) and T level for higher reliability applications.

6.1.1 Caution. Capacitors covered by this specification of case size 5 may be prone to arcing if used above 300 volts.

6.1.2 Precautionary note. Capacitors covered by this specification are very susceptible to thermal shock damage due to their large ceramic mass. Temperature profiles used should provide adequate temperature rise and cool-down time to prevent damage from thermal shock. The capacitors should be preheated. The preheat and cool down should not exceed 4°C per second. The maximum preheat temperature should be within 50°C of the solder bath temperature. Consult manufacturers for further recommendation.

6.1.3 Precautionary note. Capacitors covered by this specification have high mass and are susceptible to thermal and mechanical damage. Special board assembly processing and mounting precautions may be necessary especially in high vibration environments. Consult manufacturers for recommendations.

6.2 Acquisition requirements. Acquisition requirements must specify the following:

a. Title, number, and date of this specification, the applicable specification sheet, and the complete PIN (see 3.1).

b. Issue of DoDISS to be cited in the solicitation, and if required title, number, and date of the applicable specification sheet, and the complete PIN (see 3.1).

c. Packaging requirements (see 5.1).

6.3 Qualification. With respect to products requiring qualification, awards will be made only for products that are, at the time of award of contract, qualified for inclusion in the Qualified Products List whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or orders for the products covered by this specification. The activity responsible for the Qualified Products List is the U.S. Army Communications-Electronics Command, ATTN: AMSEL-LC-LEO-E-EP, Fort Monmouth, NJ 07703-5023; however, information pertaining to qualification of products may be obtained from Defense Supply Center, Columbus, ATTN: DSCC-VQP, Post Office Box 3990, Columbus, OH 43216-5000.

6.3.1 Copies of SD-6. Copies of SD-6, "Provisions Governing Qualification", may be obtained upon application to Document Automation and Production Service, Building 4D (DPM-DODSSP), 700 Robbins Avenue, Philadelphia, PA 19111-5094.

6.4 Case insulation. It is not intended that the case insulation be subjected to sustained voltage in excess of 150 percent of the dc rated voltage of the capacitor. Supplementary insulation should be provided where the case may come in contact with higher voltage.

6.5 Tin plated finishes. Tin plating is prohibited (see 3.5.3.2) because it may result in tin whisker growth. Tin whisker growth could adversely affect the operation of electronic equipment systems. For additional information, see ASTM B545 (Standard Specification for Electrodeposited Coating of Tin).

6.6 Subject term (key word) listing.

Dielectric withstanding voltage
Dissipation factor
Insulation resistance
Statistical process control (SPC)

6.7 Changes from previous issue. The margins of this specification are marked with asterisks to indicate where changes from the previous issue were made. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations and relationship to the last previous issue.

APPENDIX

PROCEDURE FOR QUALIFICATION INSPECTION

10. SCOPE

10.1 Scope. This appendix details the procedure for submission of samples for qualification inspection of capacitors covered by this specification. The procedures for extending qualification of the required sample to other capacitors covered by this specification; is also outlined herein. This appendix is a mandatory part of this specification. The information contained herein is intended for compliance.

20. APPLICABLE DOCUMENTS. This section is not applicable to this appendix.

30. SUBMISSION

30.1 Sample.

30.1.1 Single-style submission. A sample of the size required in table V, of the highest capacitance value in each voltage rating, in each voltage-temperature limit, in each style for which qualification is sought shall be submitted.

30.1.2 Extension of qualification by similarity. Qualification may be extended for each case type (unencapsulated, encapsulated, or conformally coated) for either the horizontally or vertically stacked parts. The number of samples submitted for qualification shall be evenly divided for all groups in table XIII.

TABLE XIII. Qualification samples.

Qualification inspection group (see table V)	Number of samples of each case type for horizontally or vertically stacked parts
Group III	2 each of the unencapsulated, encapsulated, and conformally coated or
	3 each of the unencapsulated and conformally coated or
	3 each of the unencapsulated and encapsulated.
Group IV	4 each of the unencapsulated, encapsulated, and conformally coated or
	6 each of the unencapsulated and conformally coated or
	6 each of the unencapsulated and encapsulated.
Group V	4 each of the unencapsulated, encapsulated, and conformally coated or
	6 each of the unencapsulated and conformally coated or
	6 each of the unencapsulated and encapsulated.
Group VI	2 each of the unencapsulated, encapsulated, and conformally coated or
	3 each of the unencapsulated and conformally coated or
	3 each of the unencapsulated and encapsulated.
Group VII	2 each of the unencapsulated, encapsulated, and conformally coated or
	3 each of the unencapsulated and conformally coated or
	3 each of the unencapsulated and encapsulated.
Group VIII	8 each of the unencapsulated, encapsulated, and conformally coated or
	12 each of the unencapsulated and conformally coated or
	12 each of the unencapsulated and encapsulated.

APPENDIX

40. EXTENT OF QUALIFICATION

40.1 Single-style submission.

a. Capacitance: Range qualification will be restricted to values equal to and less than the capacitance value submitted.

b Capacitance tolerance: Capacitance tolerance qualification will be restricted to tolerances equal to and wider than the tolerance submitted.

c. DC rated voltage qualification will be restricted to that submitted. Operating temperature range and voltage-temperature limit qualification will be restricted to that submitted.

40.2 Product level.

40.2.1 B level qualification from T level. Qualification of the T level product qualifies to the B level product of same design.

40.2.2 T level qualification from B level. To add T level qualification once qualified to B level, the following needs to be accomplished, in the following order:

a. Table V, group I (Thermal shock - 100 cycles). Voltage conditioning after thermal shock is not required but may be performed at the manufacturer's option. Electrical measurements of 4.8.5.3 shall be performed regardless of whether voltage conditioning is performed or not.

b. Table V, group VI (DPA) with the requirements of 3.7 and 3.22.

c. Table V, group VII (Humidity, steady state, low voltage).

d. Table V, group VIII (Life - 4,000 hours minimum).

The lot used for qualification shall not be sold as T level parts.

50. SOLDER DIP (RETINNING) LEADS

50.1 Solder dip (retinning) leads. The manufacturer may solder dip/retin the leads of capacitors supplied to this specification provided the solder dip process (50.2) or an equivalent process has been approved by the qualifying activity.

50.2 Qualifying activity approval. Approval of the solder dip process will be based on one of the following options:

a. When the original lead finish qualified was hot solder dip lead finish 52 in accordance with MIL-STD-1276 (NOTE: The 200 microinch maximum thickness is not applicable). The manufacturer shall use the same solder dip process for retinning as was used in the original manufacture of the capacitor.

b. When the lead originally qualified was not solder dip lead finish 52 of MIL-STD-1276 as prescribed in 50.2a, approval for the process to be used for solder dip shall be based on the following procedure:

(1) Twenty samples of any capacitance value for each style and lead finish shall be subjected to the manufacturer's solder dip process. The capacitors shall then be subjected to all group A, subgroup 1 post-electrical tests with no defects allowed.

(2) Ten of the samples shall then be subjected to the solderability test, with no defects allowed.

(3) The remaining 10 samples shall be subjected to the resistance to soldering heat test, followed by the moisture resistance test with no defects allowed.

50.3 Solder dip/retinning options. The manufacturer may solder dip/retin as follows:

a. As a corrective action if the lot fails the group A solderability test.

b. After the group A inspection has been completed, and following the solder dip/retinning process, the dielectric withstanding voltage, insulation resistance (at +25°C), dissipation factor, and capacitance measurements shall be performed on 100 percent of the lot. The percent defective allowable (PDA) shall be the same as that allowed for subgroup 1 of the group A inspection.

Custodians:
Army - CR
Navy - EC
Air Force - 11
DLA - CC
NASA - NA

Review activities:
Army - AR, AT, AV, MI
Navy - MC
Air Force - 19, 99

Preparing activity:
Army - CR

Agent:
DLA - CC

(Project 5910-2208)

STANDARDIZATION DOCUMENT IMPROVEMENT PROPOSAL

INSTRUCTIONS

1. The preparing activity must complete blocks 1, 2, 3, and 8. In block 1, both the document number and revision letter should be given.

2. The submitter of this form must complete block1s 4, 5, 6, and 7, and send to preparing activity.

3. The preparing activity must provide a reply within 30 days from receipt of the form.

NOTE: This form may not be used to request copies of documents, nor to request waivers, or clarification of requirements on current contracts. Comments submitted on this form do not constitute or imply authorization to waive any portion of the referenced document(s) or to amend contractual requirements.

I RECOMMEND A CHANGE:	**1. DOCUMENT NUMBER** MIL-PRF-49470B	**2. DOCUMENT DATE** (YYMMDD) 13 January 2003

3. DOCUMENT TITLE CAPACITOR, FIXED, CERAMIC DIELECTRIC, SWITCH MODE POWER SUPPLY (GENERAL PURPOSE AND TEMPERATURE STABLE), STANDARD RELIABILITY AND HIGH RELIABILITY, GENERAL SPECIFICATION FOR

4. NATURE OF CHANGE (Identify paragraph number and include proposed rewrite, if possible. Attach extra sheets as needed.)

5. REASON FOR RECOMMENDATION

6. SUBMITTER

a. NAME (Last, First, Middle initial)	b. ORGANIZATION	
c. ADDRESS (Include Zip Code)	d. TELEPHONE (Incl Area Code) (1) Commercial (2) DSN (If applicable)	7. DATE SUBMITTED (YYYYMMDD)

8. PREPARING ACTIVITY

a. NAME US Army Communications-Electronics Command	b. TELEPHONE (Include Area Code) (1) Commercial (732) 532-9104 (2) DSN 992-9104
c. ADDRESS (Include Zip Code) ATTN: AMSEL-LC-LEO-E-EP Fort Monmouth, NJ 07703-5023	**IF YOU DO NOT RECEIVE A REPLY WITHIN 45 DAYS, CONTACT:** Defense Standardization Program Office (DLSC-LM) 8725 John J. Kingman Road, Suite 2533 Fort Belvoir, Virginia 22060-6221 Telephone (703) 767-6888 DSN 427-6888