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This document and process conversion measures necessary to comply with this revision shall be completed by 1 May 98.

INCH-POUND

MIL-PRF-38535E
1 December 1997
SUPERSEDING
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31 October 1995

PERFORMANCE SPECIFICATION

INTEGRATED CIRCUITS (MICROCIRCUITS) MANUFACTURING, GENERAL SPECIFICATION FOR

This specification is approved for use by all Departments and Agencies of the Department of Defense.

This document is a performance specification. It is intended to provide the device manufacturers an acceptable established baseline in order to support Government microcircuit application and logistic programs. The basic document has been structured as a performance specification which is supplemented with detailed appendices. These appendices provide guidance to manufacturers on demonstrated successful approaches to meeting military performance needs. In general, these appendices are included as a benchmark and are not intended to impose mandatory requirements. Exceptions to this policy are: Appendix A is mandatory for manufacturers of device types supplied in compliance with MIL-M-38510 and MIL-STD-883. Appendix B is intended for space application and is required for a V level device. Appendix C is mandatory for systems requiring Radiation Hardness Assurance (RHA).

1. SCOPE

* 1.1 Scope. This specification establishes the general performance requirements for integrated circuits or microcircuits and the quality and reliability assurance requirements which must be met for their acquisition. The intent of this specification is to allow the device manufacturer the flexibility to implement best commercial practices to the maximum extent possible while still providing product which meets the military performance needs. Detail requirements, specific characteristics of microcircuits, and other provisions which are sensitive to the particular use intended will be specified in the device specification. Quality assurance requirements outlined herein are for all microcircuits built on a manufacturing line which is controlled through a manufacturer's Quality Management (QM) program and has been certified and qualified in accordance with requirements herein. Several levels of product assurance including Radiation Hardness Assurance (RHA) are provided for in this specification. The certification and qualification sections found herein outline the requirements to be met by a manufacturer to be listed on a Qualified Manufacturer Listing (QML). After listing of a technology flow on a QML, the manufacturer must continually meet or improve the established baseline of certified and qualified procedures, the QM program, the manufacturer's review system, the status reporting and quality and reliability assurance requirements for all QML products. The manufacturer may present alternate methods of addressing the requirements contained in this document. This specification requires a manufacturer to establish a process flow baseline. If sufficient quality and reliability data is available, the manufacturer, through the QM program and the manufacturer's review system, may modify substitute or delete tests.

* Beneficial comments (recommendations, additions, deletions) and any pertinent data which may be of use in improving this document should be addressed to: Defense Supply Center Columbus, 3990 E. Broad Street, Columbus OH, 43216-5000 by using the Standardization Document Improvement Proposal (DD Form 1426) appearing at the end of this document or by letter.

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FSC 5962

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2. APPLICABLE DOCUMENTS

2.1 General. The documents listed in this section are needed to meet the requirements specified in sections 3, 4, and 5 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements documents cited in sections 3, 4, and 5 of this specification, whether or not they are listed.

2.2 Government documents.

2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-1285 - Marking of Electrical and Electronic Parts.

HANDBOOK

DEPARTMENT OF DEFENSE

MIL-HDBK-780 - Standard Microcircuit Drawings.
* MIL-HDBK-103 - List of Standard Microcircuit Drawings (SMD's).

(Unless otherwise indicated, copies of the above specifications, standards, and handbooks are available from the Standardization
* Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094).

2.2.2 Other Government documents, drawings, and publications. The following other Government documents, drawings, and publications form a part of this document to the extent specified herein. Unless otherwise specified, the issues are those cited in the solicitation.

Handbook H4/H8 - Commercial and Government Entity (CAGE) Handbook.
NAVSHIPS 0967-190-4010 - Manufacturer's Designating Symbols.

(Copies of other Government documents required by contractors in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.3 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents which are DoD adopted are those listed in the issue of the DoDISS cited in the solicitation. Unless otherwise specified, the issues of documents not listed in the DoDISS are the issues of the documents cited in the solicitation.

* ELECTRONIC INDUSTRIES ASSOCIATION (EIA)

EIA-STD-625 - Requirements for Handling Electrostatic Discharge Sensitive (ESDS) Devices.
JEDEC publication 109 - General Requirements for Distributors of Military Integrated Circuits.
JEP 121 - Guidelines for MIL-STD-883 Screening and QCI optimization.
JESD 22-A102 - Accelerated Moisture on Unbiased Autoclave.
JESD 22-B101 - External Visual.

(Applications for copies of EIA/JEDEC documents should be addressed to Global Engineering Documents, 15 Inverness Way East, Englewood, CO 80112-5704).

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* 2.4 Order of precedence. In the event of a conflict between the text of this document and the references cited herein (except for device specifications), the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

* 3.1 General. The manufacturer of QML microcircuits in compliance with this specification shall have or have access to and use of production and test facilities, and a QM program to assure successful compliance with the provisions of this specification. All microcircuits manufactured on a QML line shall be processed on a certified fabrication line, and shall be assembled on a certified assembly line. All microcircuits shall be electrically capable of meeting parameters over the specified temperature range in accordance with the device specification in a certified test facility before delivery of the product. The QML certification mark (3.6.3) indicates compliance to all the performance provisions of this specification. The requirements described herein shall be addressed in one of two ways. These are as follows:

a. As specified herein.

b. Demonstration to the qualifying activity and validation team when applicable, of an alternate method, which addresses the same quality and reliability concerns as defined by the requirement, or demonstration to the qualifying activity that the requirement is not applicable to the manufacturer's technology.

NOTE: A QML manufacturer may modify screening and Technology Conformance Inspection (TCI) requirements of the device specification or Standard Microcircuit Drawing (SMD) under special criteria defined within this specification and as defined in the manufacturer's QM plan. (For guidance on screening optimization see JEP 121 - Guidelines for MIL-STD-883 Screening and QCI Optimization.) These changes cannot affect any thermal, mechanical or electrical parameters, which affect form, fit, or function of the device, defined within the device specification or SMD.

* 3.1.1 Reference to applicable device specification. For purposes of this specification, when the term "as specified" is used without additional reference to a specific location or document, the intended reference shall be to the device specification.

* 3.2 Item requirements. The individual item requirements, including temperature range, for integrated circuits delivered under this specification shall be documented in the device specification prepared in accordance with 3.5 herein. Devices produced under this specification may have any operating temperature range (case, ambient, or junction) as long as it is specified in the device specification, and any references to minimum or maximum operating temperatures shall refer to the respective lower and upper limits of this range. However, the manufacturer shall demonstrate the operating temperature range (case, ambient, or junction) capability of the technology being offered. The Standard Evaluation Circuit (SEC) is typically used for this demonstration.

3.2.1 Certification of conformance and acquisition traceability. Manufacturers or suppliers including distributors who offer QML microcircuits described by this specification shall provide written certification, signed by the corporate officer who has management responsibility for the production of the QML microcircuits, (1) that the QML microcircuits being supplied have been manufactured and shall be capable of passing the tests in accordance with this specification, (2) that all QML microcircuits are as described on the certificate of conformance which accompanies the shipment, and (3) that dealers and distributors have handled the QML microcircuit in accordance with the requirements of EIA-STD-625 and JEDEC publication 109. The responsible corporate official may, by documented authorization, designate other responsible individuals to sign the certificate of conformance (such as members of the manufacturer's review system), but, the responsibility for conformity with the facts shall rest with the responsible corporate officer. The certification shall be confirmed by documentation to the Government or to users with Government contractors or subcontractors, regardless of whether the QML microcircuits are acquired directly from the manufacturer or from another source such as a distributor. When other sources are involved, their acquisition certification shall be in addition to the certificates of conformance and acquisition traceability provided by the manufacturer and previous distributors. The certificate shall include the following information:

a. Manufacturer documentation:

1. Manufacturer's name and address.
2. Customer's or distributor's name and address.
3. Device type.
4. Date code and latest reinspection date, if applicable.
5. Quantity of devices in shipment from manufacturer.
6. Statement certifying QML microcircuit conformance and traceability.
7. Solderability reinspection date, if applicable.
8. Signature and date of transaction.

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b. Distributor documentation for each distributor:

1. Distributor's name and address.
2. Name and address of customer.
3. Quantity of devices in shipment.
4. Latest reinspection date, if applicable.
5. Certification that this shipment is a part of the shipment covered by the manufacturer's documentation.
6. Solderability reinspection date, if applicable.
7. Signature and date of transaction.

3.3 Quality Management (QM) program. A QM program shall be implemented by the manufacturer (see G.3.1).

3.3.1 Manufacturer's review system. A dedicated system of review, for the purposes of this document hereafter referred to as the Technical Review Board (TRB), shall be responsible for: the implementation of the QM program, as reflected in the QM plan; maintenance of all certified and qualified processes; process change control; reliability data analysis, failure analysis, and corrective actions; QML microcircuit recall procedures; and qualification status of the technology.

3.3.2 QM plan. A QM plan reflects the major elements of the manufacturer's QML process (see G.3.3). The QM plan is kept current and up-to-date and reflects all major changes.

3.3.3 Self-assessment program. The manufacturer shall have a self-assessment program with an evaluation system and the results of that assessment shall be made available for review (see G.3.1).

3.3.4 Change control procedures. The manufacturer shall have a system which shall include procedures for notification of change that affects form, fit, and function, to all known acquiring activities. The manufacturer may make notification of this change of product through the Government-Industry Data Exchange Program (GIDEP) using the Product Change Notice, in any case the manufacturer shall assure that all known acquiring activities are notified. The following processes and procedures shall be addressed (see G.3.4):

a. Design methodology changes.

b. Fabrication process changes.

c. Assembly process changes.

d. Package changes.

e. Test facility changes.

* 3.4 Requirements for listing on a QML. To be listed on a QML the manufacturer shall demonstrate compliance to the QML certification requirements (see 3.4.1), demonstrate compliance to the QML qualification requirements (see 3.4.2), and work with the Defense Supply Center Columbus (DSCC) to develop a SMD describing the candidate QML device(s) (see 3.5). An existing MIL-M-38510 associated device specification may be used. The qualifying activity will verify compliance to the requirements and will list the manufacturer's technology on the QML.

3.4.1 QML certification requirements. The manufacturers shall meet the minimum procedures and requirements in this section for QML certification of a manufacturing line. The qualifying activity will determine adequacy and compliance to the requirements as specified herein and will report their findings and recommendations to the manufacturer's TRB. Each portion of a QML microcircuit manufacturer's line capability, including any offshore operations, may be demonstrated independently, but validation by the qualifying activity will assess a complete technology flow. To maintain certification the manufacturer shall provide notification of change to the process baseline to the qualifying activity. For generic qualification procedures, certification shall consist of:

a. Quality management program documentation (see G.3.1).

b. Process capability demonstration (see H.3.2).

c. Qualifying activity management and technology validation (see 3.4.1.2).

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d. Demonstration of manufacturer's control of any offshore operations (see appendix E).

e. All procedures used to manufacture masks for monolithic fabrication (see appendix H).

3.4.1.1 Process capability demonstration. As part of certification, the manufacturer shall build devices, perform tests and run software benchmarks necessary to demonstrate that the manufacturer has a comprehension of the capability of the manufacturing process as related to quality, reliability and producibility. The summary of the results of all of these tests shall be available for review by the qualifying activity (prior to scheduling a validation review). These tests shall be designed to be used as a continual check of the process capability as well as an initial demonstration of such capability. The TRB shall determine when such tests are to be performed after initial certification.

Process capability demonstration shall consist of:

a. Design.

1. Circuit.
2. Package.

b. Wafer fabrication.

c. Statistical Process Control (SPC) and in-process monitoring programs including the Technology Characterization Vehicle (TCV) program, the Standard Evaluation Circuit (SEC), and Parametric Monitors (PM) (see appendix H).

d. Wafer acceptance plan.

e. Assembly and packaging.

f. RHA (see appendix C).

3.4.1.2 Management and technology validation. The validation by the qualifying activity will include, as a minimum, the following applicable areas of the manufacturer's facility: Management quality assurance, design, mask, wafer fabrication, assembly and package, and electrical test. This validation procedure will involve a qualifying activity review of the manufacturer's QM plan, self-validation and an on-site visit of the manufacturer's facility.

3.4.1.3 On-site validation. Manufacturer shall make available to the qualifying activity all data needed to support QM policy and procedures. Qualifying activity access to manufacturing and testing facilities and operators will be required, including any offshore sites. For first time certification, on-site validation reviews of the manufacturer's design, wafer fabrication, assembly, and test facilities will be required. After the initial qualification is accomplished, the manufacturer may add other design, wafer fabrication, assembly and/or test facilities upon completion of the appropriate qualification testing, TRB approval, and qualifying activity approval. The qualifying activity reserves the right to perform on-site reviews of any facilities/technologies that the manufacturer plans to add to their QML listing. Validation of third party suppliers is the responsibility of the manufacturer.

3.4.1.3.1 Second and third party validations. The process used by the manufacturer to validate a third party facility shall be reviewed during the initial QML validation process. The qualifying activity reserves the right to visit third party facilities to verify that the manufacturer's validation process is effective. A QML certified manufacturer may use second party facilities with the approval of the qualifying activity. A second party facility must be a QML certified manufacturer facility or a facility that has been granted approval by the qualifying activity for the manufacturer of QML product.

3.4.1.3.2 Radiation Source of Supply (RSS) validations. An RSS shall receive a QML validation for all processes listed in this specification and the RSS's program plan. This includes a QML validation of the manufacturing process and laboratory suitability of the RHA test facilities.

3.4.1.4 Technology validation. The manufacturer's technology flow shall be reviewed. Detailed information of what the qualifying activity will want to discuss during the validation can be found in the self-audit guideline list (available from the qualifying activity when QML validation is requested) and the Validation Procedural Guide (available from the qualifying activity). Some critical areas which will be reviewed by the qualifying activity, as applicable, during the validation are:

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a. Design center procedures.

b. Design review procedures.

c. Model verification.

d. Software configuration and configuration management.

e. Testability procedures and policies (e.g., Joint Test Action Group (JTAG)) as applicable.

f. Archival system (e.g., VHSIC Hardware Description Language (VHDL)).

g. Mask inspection procedures.

h. TCV, SEC, parametric monitor tests and data.

i. Fabrication rework procedures.

j. SPC program (all areas).

k. Design rule documentation.

l. Clean room procedures.

m. Wafer traceability.

n. GaAs wafer boule evaluation procedure.

o. Assembly rework procedure.

p. Die attach procedures.

q. Wire/ribbon bonding.

r. Device traceability and travelers.

s. Lot formation (wafer, device and inspection).

t. Assembly area environmental control.

u. Internal moisture vapor control program.

v. Electrostatic Discharge (ESD) control and testing.

w. Visual inspection.

x. Human contamination prevention procedures.

y. Equipment calibration and maintenance.

z. Training policy and procedures.

aa. Electrical test procedures.

bb. Screening procedure.

cc. TCI procedures.

dd. Third party design center procedures.

ee. Change control procedure.

ff. Chip encapsulation/molding.

gg. Qualification test plan.

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3.4.1.4.1 Package design selection reviews. The manufacturer shall establish and implement systematic package design or selection reviews to ascertain compatibility of chip(s) and packages with respect to thermal, electrical and mechanical performance and manufacturing, testing, and reliability requirements.

3.4.1.5 Manufacturer self-validation. The manufacturer shall perform a self-validation to determine compliance to the QM plan (see appendix G).

3.4.1.6 Change management system. The manufacturer shall have a system for change management. This system shall include a process to monitor internal changes and the assessment of those changes as to the impact to customers. An appropriate customer notification methodology shall be in place.

3.4.1.7 Deficiencies and concerns. Deficiencies and concerns shall be noted by the validation team during an exit critique and will be followed up with a written report. The microcircuit manufacturer shall not receive a letter of certification until all certification requirements are met.

3.4.1.8 Letter of certification. After validation, the qualifying activity will issue a letter of certification to the manufacturer, which will include any applicable offshore site(s) as defined by appendix E.

3.4.2 QML qualification requirements. Integrated Circuits (ICs) furnished under this specification shall be products which are authorized by the qualifying activity for listing on the QML. Qualification testing shall be performed in accordance with the agreed upon qualification plan. (See appendix H for guidance on qualification testing.)

3.4.2.1 Qualification extension. When a basic plant desires to qualify a device or process flow that includes an offshore site, certification and qualification may be extended under the following conditions:

a. Control and approval of the assembly and test operations by the TRB/basic plant is required along with periodic self assessments of the offshore sites. The TRB/basic plant shall review all screening and TCI tests to determine whether they should be performed exclusively in the offshore site or reserved for the basic plant in order to assure quality and reliability. The TRB/basic plant assessment shall be made available to the qualifying activity for review or approval as appropriate.

b. Qualifying activity certification of the offshore site is required. Qualification of these offshore operations is also required. For assembly site(s) an initial site will be certified and qualified by the qualifying activity. Additional assembly sites will be addressed subsequent to the initial validation.

c. All devices assembled in the offshore assembly site shall have a country of origin marking (see 3.6.5) reflecting the assembly site. In addition a unique code shall be marked on each device to assure traceability to the assembly site(s).

d. All operations, flows, quality control procedures and test standards at the offshore site shall be under the control of the TRB/basic plant. All such operations, flows, procedures and test standards must be baselined by the TRB/basic plant and the offshore site at all times.

e. The qualifying activity reserves the right to audit the offshore site(s) with a minimum notice. The basic plant site shall be responsible to facilitate all qualifying activity site visits. Any refusal to allow such a site visit may result in an immediate de-certification and QML removal.

* 3.4.3 Qualification to RHA levels. Qualification to an RHA level shall consist of qualification to the appropriate quality and reliability assurance level (class N, Q, or V) and RHA levels as defined below:

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Radiation Hardness Assurance (RHA) level

RHA level designator (see 3.6.2.1)	Radiation and total dose (Rad (Si))
/ or -	No RHA
M	3000
D	10^4
L	5×10^4
R	10^5
F	3×10^5
G	5×10^5
H	10^6

3.4.4 QML listing. A certificate of qualification will be issued upon successful completion of all qualification tests on the two demonstration vehicles and the acceptance of the qualification documentation by the qualifying activity. Issuance of the certificate of qualification will coincide with listing of the manufacturing line and the SMD(s), or existing MIL-M-38510 associated device specification(s) on the QML. The manufacturer may be removed from the QML by the qualifying activity for cause.

3.4.5 Maintenance and retention of QML. In order to sustain qualification status after initial qualification, the manufacturer shall fabricate and perform qualification testing on the selected SEC and TCV, or approved alternate assessment procedure as defined in the QM plan.

3.4.6 QML line shutdown. If an extended shutdown of a QML certified/qualified flow is necessary, the TRB shall assess and ensure that the process is still capable when production is restarted.

3.4.7 Revalidation reviews. The interval between on-site revalidation reviews shall normally not exceed two years, but the qualifying activity will adjust this interval based on the manufacturer's TRB reports, customer feedback, and other indications of the manufacturer's maintenance of the QML system.

* 3.5 Device specification. MIL-HDBK-780 details the SMD format to be used (SMD's are to be used except where the device specification is a MIL-M-38510 associated device specification or an altered item drawing is required by the associated device specification or SMD) and data requirements to be submitted with any device procured under this specification. The QML certification mark shall not be used until the device specification is approved (see 3.6.3).

3.6 Marking of microcircuits. Marking of QML microcircuits shall be in accordance with the following and the identification and marking provisions of the device specification or drawing. The marking shall be legible and complete. If any special marking (e.g., altered item drawing number) is used by the device supplier or user/equipment contractor, it shall be in addition to the existing/original marking as required herein and shall be visibly separate from and in no way interfere with the marking required herein. The following shall be placed on each microcircuit:

a. Index point (see 3.6.1).

b. Part or Identifying Number (PIN) (see 3.6.2).

c. "Q" or "QML" certification mark (see 3.6.3).

d. Manufacturer's identification (see 3.6.4).

e. Country of origin (see 3.6.5).

f. Date code (see 3.6.6).

g. Special marking (see 3.6.7).

h. Serialization; when specified by the procuring activity, each microcircuit shall be marked with a unique serial number assigned within that inspection lot prior to the first recorded electrical measurement in screening.

i. Electrostatic discharge sensitivity identifier, if applicable (see 3.6.7.2).

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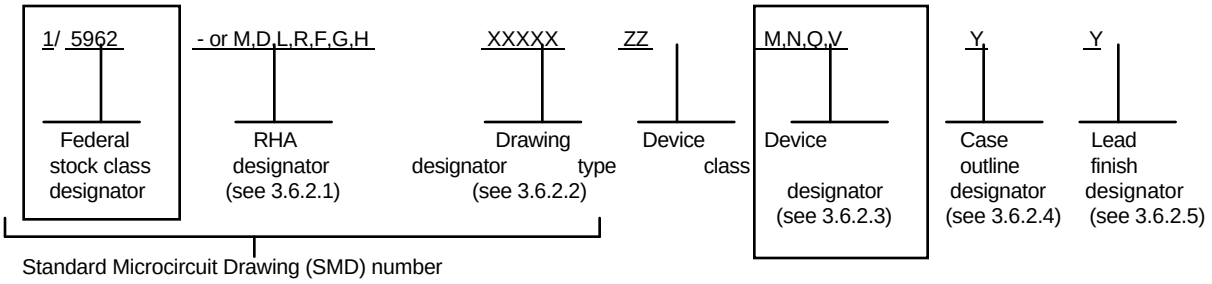
* NOTE: For unpackaged die only items b through i shall apply and be marked on the wafer or die carrier and any other container external to the wafer or die carrier. For Tape Automated Bonded (TAB) (see Appendix F) devices marking shall be as defined in the procurement document.

* 3.6.1 Index point. The index point, tab, or other marking indicating the starting point for numbering of leads or for mechanical orientation shall be as specified in the device specification and shall be designed so that it is visible from above when the microcircuit is installed in its normal mounting configuration. The outline or solid equilateral triangle(s), which are used as an electrostatic identifier (see 3.6.7.2) may also be used as the pin 1 identifier.

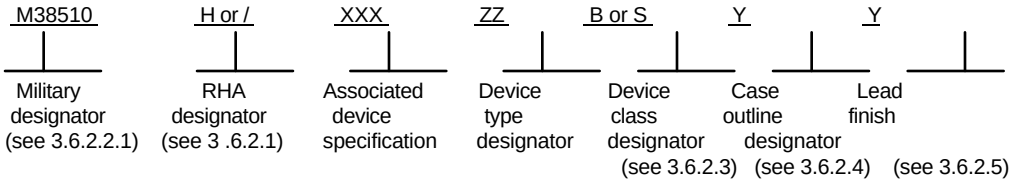
* 3.6.2 Part or Identification Number (PIN). Each QML microcircuit shall be marked with the complete PIN. The PIN may be marked on more than one line provided the PIN is continuous except where it "breaks" from one line to another. As of revision B of MIL-PRF-38535, several types of documents are acceptable for use when specifying QML microcircuits. They are MIL-M-38510 device specifications, Standard Microcircuit Drawings (SMD), or one part one part number SMD's. The PIN marked on those parts under QML will be the same as when supplied by the manufacturer prior to being listed on the QML-38535. The "Q" or "QML" designator combined with the listing of that PIN on a particular vendors QML listing shall indicate the fact that the manufacturer of the device is QML certified and qualified for the processes used to build that product. The PIN system shall be of one of the following forms, as applicable to the SMD or MIL-M-38510 associated device specification used for production:

a. SMD PINs shall be as follows:



For packages where marking of the entire SMD PIN number and all other required topside marking are not possible due to space limitations, the manufacturer has the option of leaving the “5962-“ off the marking. The allowance for optional marking will be indicated in the individual SMD. For RHA product using this option, the RHA designator shall still be marked.

* b. Associated device specification documents, dated prior to 27 July 1990, shall be as follows:



All new PINs specified by new documents, dated after 27 July 1990, shall be in accordance with the one part-one part number system.

* All PINs specified by existing associated device specifications with the number assigned prior to 27 July 1990, may use either the original assigned PIN or the one part one-part number system with the first two digits in the drawing designator being "38" and the last three being the associated device specification number (e.g., M38510/00101BAC will become 5962-3800101BAC).

1/ Drawings initiated prior to 1986 may not contain a federal stock class designator.

* 2/ Non one-part SMDs do not contain a device class designator. See MIL-HDBK-103 for qualification information. Old MIL-M-38510 associated device specifications converted to SMDs will contain a B or S class designator.

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* 3.6.2.1 RHA designator. A "- or /" indicates no radiation hardness assurance. Letters M, D, L, R, F, G, or H designation levels are defined in 3.4.3.

* 3.6.2.2 Drawing designator. The first two characters of the designator will consist of the last two digits of the year, the last three characters will consist of unique characters assigned to the drawing by DSCC.

* 3.6.2.2.1 Military designator. The M38510 military designator for microcircuits means a "MIL" specification item produced in full compliance with this document or for JAN manufacturers appendix A of this document including qualification, and the device specification. Any device which does not meet all the requirements of this specification and the device specification shall not be marked M38510 and shall not make reference to MIL-PRF-38535 or MIL-PRF-38535 appendix A.

* Note: The military designator is optional for leadless chip carrier outlines which have a surface area smaller than the C-10 package provided the full certification mark “JAN” is used rather than the abbreviation “J”.

* 3.6.2.3 Device class designator. The device class shall be designated by a single letter identifying the quality assurance level. For example:

Military documentation format	Example PIN under new system	Manufacturing source listing	Document listing
MIL-PRF-38535 Standard Microcircuit Drawings	5962-XXXXXZZ(N, Q, V (B or S))YY	QML-38535	MIL-HDBK-103
1.2.1 of MIL-STD-883 Standard Microcircuit Drawings	5962-XXXXXZZ(M)YY	MIL-HDBK-103	MIL-HDBK-103

* 3.6.2.4 Case outline. The case outline shall be designated by a single letter assigned to each outline within each device specification.

3.6.2.5 Lead finish. The lead finish shall be designated by a single letter as follows:

Finish letter	Process
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
X	Either A, B, or C (mark on specification only)

3.6.3 Certification marks. All microcircuits acquired to and meeting the requirements of this specification and the applicable SMD, associated device specification, or military temperature range data book parts, which are approved for supply under QML shall bear the "QML" or "Q" certification mark. The "J" marking which was required by MIL-M-38510 may be marked in front of the military designator portion of the associated device specification part number at the QML vendors option. This "J" was not and shall not be considered part of the official part number used to assign a national stock number.

3.6.4 Manufacturer's identification. Microcircuits shall, as a minimum, identify the manufacturer by the marking of name or trademark of the manufacturer. When space permits, the manufacturer may also mark the manufacturer's Commercial and Government Entity (CAGE) code. The identification of the equipment manufacturer may appear on the microcircuit only if the equipment manufacturer is also the microcircuit manufacturer. If the microcircuit manufacturer's designating symbol or CAGE code number is marked, it shall be as listed on NAVSHIPS 0967-190-4010 or cataloging handbook H4/H8. The designating symbol shall be used only by the manufacturer to whom it has been assigned and only on those devices manufactured at that manufacturer's plant. In the case of small microcircuits, the manufacturer's designating symbol may be abbreviated by omitting the first "C" in the series of letters.

3.6.4.1 Code for assembly sites. If the provisions for appendix E are used and the manufacturer has more than one offshore facility for assembly in a given country, a unique single letter code shall be assigned for the assembly sites used. This code shall be marked on the device immediately preceding or immediately after the date code. The assembly codes and the full address shall be included in the QML.

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3.6.5 Country of origin. The name of the country of assembly or an appropriate abbreviation shall be marked in small characters below or adjacent to the other marking specified. Backside marking of the country of origin information is permitted.

3.6.6 Date code. Microcircuits shall be marked with a unique code to identify the first or the last week of the period (6 weeks maximum) during which devices in that inspection lot were sealed. The first two numbers in the code shall be the last two digits of the number of the year, and the third and fourth numbers shall be two digits indicating the calendar week of the year.

3.6.7 Marking location and sequence. The QML mark, the PIN, the date code, and ESD identifier, if applicable (see 3.6.7.2), shall be located on the top surface of leadless or leaded chip carriers, pin grid array packages, flat packages or dual-in-line configurations and on either the top or the side of cylindrical packages (TO configurations and similar configurations). When the size of a package is insufficient to allow marking of special process identifiers on the top surface, the backside of the package may be used for these markings except the ESDS identifier, if applicable, shall be marked on the top. Button cap flat packs with less than or equal to 16 leads may have the identifier marked on the ceramic. Backside marking with conductive or resistive ink shall be prohibited. For unpackaged die marking is to be located on the container.

3.6.7.1 Beryllium oxide package identifier. If a microcircuit package contains beryllium oxide, the part shall be marked with the designation "BeO".

* 3.6.7.2 Electrostatic Discharge Sensitivity (ESD) identifier. ESD classification marking is not required. The manufacturer will have an option of no ESD marking, marking a single ESD triangle or marking in accordance with the ESD device classification (i.e., class 1 - one Δ; class 2 - two Δ's; class 3 - no marking). Because it may no longer be possible to determine the ESD classification from the part marking, the device discharge sensitivity classification, as defined in test method 3015 of MIL-STD-883, will have to be obtained through MIL-HDBK-103 or QML-38535.

3.6.8 QML marked product. For QML certified and qualified manufacturers and manufacturers who have been granted transitional certification (see H.3.3), standard product (JAN, class M SMDs, and military temperature range class B data book product), produced on a QML flow may be marked with the "Q" or "QML" certification mark. This allowance applies to contractor prepared drawings covering standard product only if the drawing was released prior to 31 Dec 1993 or the date the product becomes QML whichever is the later date, and the part is marked with the standard part number. A list of the manufacturer's military temperature range product to be included under QML must be submitted to the qualifying activity for approval. Contractor prepared drawings written for nonstandard parts may not be marked with a "Q" or "QML". The only exception to this requirement is an altered item drawing required by an device specification or SMD.

Only parts covered by a MIL-M-38510 device specification, an SMD, or generic parts which have been grandfathered (a list of eligible
* devices must be submitted to DSCC-VA or DSCC-VQ for review) will be listed on QML-38535. After 31 Dec 93, new QML products, which are marked with a "Q" or "QML" certification mark, must be documented on an SMD (see 3.5)." Any device that is not processed in compliance with the provisions of MIL-PRF-38535 shall not be claimed to be compliant. Non-compliant products shall not contain “QML”, “QMLV” or any variant thereof within the vendors part number or within any marking located on the package.

3.6.9 Marking on container. All of the markings specified in 3.6, except the index point, shall appear on the die container/package (e.g., waffle pack, etc.), carrier, unit pack (e.g., individual foil bag), unit container, or multiple carriers (e.g., tubes, rails, magazines) for delivery. For ESD sensitive devices, an industry standard symbol used to identify ESD sensitivity (e.g., EIA-STD-RS-471 symbol) shall be marked on the carrier or container. However, if all the marking specified above is clearly visible on the devices and legible through the unit carrier or multiple carrier, or both then the ESD marking only shall be required on the multiple carrier. These requirements apply to the original or repackaged QML microcircuits by the manufacturer or distributor.

3.7 Remarking. QML microcircuits may be remarked provided that all remarking procedures are approved by the TRB. Remarking shall be in accordance with 3.6 herein.

3.8 Screening and test. All microcircuits delivered in accordance with this document shall be capable of meeting the screening and testing requirements of 4.2 herein.

3.9 Technology Conformance Inspection (TCI). All microcircuits delivered in accordance with this document shall be capable of meeting the TCI requirements of 4.3 herein.

3.9.1 TCI assessment. In the event the TRB determines that the TCI requirements are not met the TRB shall notify the Qualifying Activity (QA) immediately, an assessment of the product shall be made by the TRB, and the qualifying activity shall be notified of the decision.

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3.10 Solderability. All parts shall be capable of passing the solderability test in accordance with MIL-STD-883, test method 2003, on delivery.

3.11 Traceability. Traceability to the wafer lot level (for GaAs to wafer level) shall be provided for all delivered microcircuits. Traceability includes, as a minimum, the completion of each step required in design (when applicable), fabrication, assembly, test and any applicable qualified rework procedure.

3.12 ESD control. QML microcircuits shall be handled in accordance with EIA-STD-625 or other industry standard practices, to safeguard against discharge damage.

* 3.13 Recycled, recovered, or environmentally preferable materials. Recycled, recovered, or environmentally preferable materials should be used to the maximum extent possible provided that the material meets or exceeds the operational and maintenance requirements, and promotes economically advantageous life cycle costs.

4. VERIFICATION (QUALITY ASSURANCE PROVISIONS)

4.1 Verification. A verification system shall be in place to verify the requirements of section 3 herein. For additional guidance see appendix J.

4.2 Screening. All QML integrated circuits shall be capable of passing the screens specified in tables IA and IB herein. The procedures and accept and/or reject criteria for the screens shall have been certified by the qualifying activity. With qualifying activity approval the requirements of test method 5004, MIL-STD-883 may be substituted for the screening requirements herein. When using test method 5004, class Q shall be capable of passing the Class level B screening flow and Class V shall be capable of passing the Class level S screening flow. The manufacturer, through its TRB, should identify which tests are applicable to guarantee the quality and reliability of the associated technology or end product (e.g., wafer or die product, packaged product, plastic, etc.) and may elect to eliminate or modify a screen based on supporting data which indicates that for the QML technology, the change is justified. If such a change is implemented, the manufacturer is still responsible for providing product which meets all of the performance, quality, and reliability requirements herein.

4.2.1 Screen testing failures. Devices which fail any screen test shall be identified, segregated, or removed.

4.2.2 Screening resubmission criteria. When it has been established that a failure during screening tests is due to operator error or equipment failure and it has been established that the remaining QML microcircuits have not been damaged or degraded, the surviving microcircuits, as the case may be, may be resubmitted to the corrected screening test(s) in which the error occurred. Failures verified as having been caused by test equipment failure or operator error shall not be counted in the PDA calculation (when applicable). ESD failures shall be counted as rejects and shall not be attributed to equipment failure or operator error.

4.2.3 Electrostatic discharge sensitivity. Electrostatic discharge sensitivity testing shall be done in accordance with test method 3015 of MIL-STD-883, and the device specification. Unless otherwise specified, tests shall be performed for initial qualification and product redesign as a minimum.

* 4.3 TCI. All product shipped shall be capable of passing TCI in accordance with tables II, III, IV, and V, for plastic packages see Table IB herein. With qualifying activity approval when test method 5005 is used as a TCI option, Class Q shall be capable of passing the Class level B flow and Class V shall be capable of passing the Class level S flow. TCI testing shall be accomplished by the manufacturer on a periodic basis to assure that the manufacturer's quality, reliability, and performance capabilities meet the requirements of the QM plan (see G.3.3).

5. PACKAGING

5.1 Packaging requirements. Packaging shall prevent mechanical damage of the devices during shipping and handling and shall not be detrimental to the device.

5.2 Marking. Marking shall be in accordance with 3.6.9 herein.

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6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory.)

* 6.1 Intended use. This specification is intended to support Government microcircuit application and logistic programs. Detailed characteristics of microcircuits needed for a program are to be defined by the device specification.

*

TABLE IA. Microcircuit screening procedure for hermetic QML microcircuits.

Screen	MIL-STD-883 test method and condition
1. Electrostatic Discharge Sensitivity (ESD)	3015 (see 4.2.3, initial qualification only)
2. Wafer acceptance	TRB plan (see H.3.2.3)
3. Internal visual	2010, test condition B (see J.3.3)
4. Temperature cycling	1010, test condition C, 50 cycles minimum
5. Constant acceleration	2001, test condition E (minimum) Y1 orientation only (see J.3.4)
6. Serialization	In accordance with device specification
7. Interim (pre burn-in) electrical parameters	In accordance with device specification
8. Burn-in test	1015, 160 hours at +125°C minimum (see J.3.5)
9. Interim (post burn-in) electrical parameters	In accordance with device specification
10. Percent Defective Allowable (PDA) calculation	5 percent, all lots (subgroup I, table III, herein)
11. Final electrical test a. Static test (table III) 1. +25°C 2. Maximum and minimum rated operating temperature b. Dynamic or functional tests (table III) 1. +25°C 2. Maximum and minimum rated operating temperature c. Switching tests (tableIII) 1. +25°C 2. Maximum and minimum rated operating temperature	In accordance with device specification
12. Seal a. Fine b. Gross	1014 (see J.3.7)
13. External visual	2009

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* TABLE IB. Tests/monitors for plastic packages. 1/

Test/monitor	MIL-STD-883 test method or industry standard
1. Wafer acceptance	TRB plan (see H.3.2.3)
2. Internal visual	TM 2010 or per manufacturers internal procedures
3. Temperature cycling/thermal shock	TM 1010/TM 1011
4. Resistance to solvents	TM 2015
5. Bond strength	TM 2011
6. Ball shear	ASTM F 1269
7. Solderability	TM 2003
8. Die Shear or stud pull	TM 2019 or TM 2027
9. Steady-state life test Endpoint electricals	TM 1005 per device specification
10. Physical dimensions	TM 2016
11. Lead integrity	TM 2004
12. Inspection for delamination	e.g., TM 1034 (dye penetrant), cross-sectioning, CSAM etc.
13. HAST	100 hours, +130°C, 85% RH 2/
14. Autoclave	JESD 22-A102 (no bias) 2 atm., +121°C
15. Salt atmosphere	TM 1009
16. Adhesion to lead finish	TM 2025
17. Interim pre burn-in electricals	Per device specification
18. Burn-in test	TM 1015, 160 hours at +125°C or per manufacturers QM plan
19. Interim post burn-in electricals	Per device specification
20. Percent Defective Allowable (PDA) or alternate procedure for lot acceptance	1% PDA or per manufacturer's QM plan
21. Final electrical tests (see table III, herein, for definition of subgroups) a. static b. dynamic c. functional d. switching	Per device specification
22. External visual	TM 2009 or JESD 22-B101 or manufacturers internal procedures

1/ Test methods are listed herein to give the manufacturer an available method to use. Alternate procedures and test methods may be used. Monitor frequency and sample plan shall be in accordance with manufacturer's QM plan.

2/ An alternate process monitor may be used; e.g., +85°C/85% RH.

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TABLE II. Group B tests.

Subgroup	MIL-STD-883			Minimum sample size quantity (accept no.)
	Test	Test method	Condition	
1	Resistance to solvents	2015		3(0)
2	Bond strength	2011		22(0)
	(1) Thermo compression		(1) C or D	Based on the number of wires
	(2) Ultrasonic		(2) C or D	
	(3) Flip-chip		(3) F	
	(4) Beam lead		(4) H	
	Die shear test or stud pull	2019 or 2027		3(0)
3	Solderability	2003	Solder temperature +245°C ±5°C	See J.3.9.2

TABLE III. Group A electrical tests. 1/

Subgroup	Parameters	Quantity (accept no.)
1	Static tests at +25°C	116(0)
2	Static tests at maximum rated operating temperature	116(0)
3	Static tests at minimum rated operating temperature	116(0)
4	Dynamic tests at +25°C	116(0)
5	Dynamic tests at maximum rated operating temperature	116(0)
6	Dynamic tests at minimum rated operating temperature	116(0)
7	Functional tests at +25°C	116(0)
8	Functional tests at maximum and minimum rated operating temperature	116(0)
9	Switching tests at +25°C	116(0)
10	Switching tests at maximum rated operating temperature	116(0)
11	Switching tests at minimum rated operating temperature	116(0)

* 1/ The specific parameters to be included for test in each subgroup shall be as specified in the device specification. Where no parameters have been identified in a particular subgroup or test within a subgroup, no group A testing is required for that subgroup or test to satisfy group A requirements.

TABLE IV. Group C tests.

Test	MIL-STD-883		Quantity (accept no.)
	Test method	Condition	
Subgroup 1 a. Steady-state life test	1005	Test condition to be specified (1,000 hrs at +125°C or equivalent)	45(0)
b. End-point electrical parameters		As specified in the applicable device procurement specification	

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* TABLE V. Group D test.

Subgroup	MIL-STD-883			Quantity (accept no.)
	Test	Test method	Condition	
1	Physical dimensions	2016		15(0)
2	a. Lead integrity	2004	B2 fatigue or as applicable for the package technology style	15(0)
	b. Seal			
	(1) Fine	1014	As applicable	
	(2) Gross	1014	As applicable	
3	a. Thermal shock	1011	B, 15 cycles	15(0)
	b. Temperature cycling	1010	C, 100 cycles	
	c. Moisture resistance	1004		
	d. Seal	1014	As applicable	
	(1) Fine			
	(2) Gross			
	e. Visual	1004, 1010		
	f. End-point electricals		As specified in the applicable device specification	
4	a. Shock	2002	B	15(0)
	b. Vibration, variable frequency	2007	A	
	c. Acceleration	2001	E, Y1 orientation or in accordance withJ.3.4	
	d. Seal	1014	As applicable	
	(1) Fine			
	(2) Gross			
	e. Visual examination	2009		
	f. End-point electricals		As specified in the applicable device specification	
5	a. Salt atmosphere	1009	A	15(0)
	b. Seal	1014	As applicable	
	(1) Fine			
	(2) Gross			
	c. Visual	1009	(Visual criteria)	
6	Internal water vapor (cavity packages)	1018	5000 ppm +100°C	3(0) or 5(1)
7	Adhesion of lead finish	2025		15(0)
8	Lid torque	2024	glass frit seal only	5(0)

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* 6.2 Terms and definitions. For the purpose of this specification, the terms, and definitions of MIL-STD-883 and MIL-STD-1331, and those contained herein apply and should be used in the applicable device specifications wherever they are pertinent.

6.2.1 Microelectronics. That area of electronic technology associated with or applied to the realization of electronic systems from extremely small electronic parts or elements.

6.2.2 Element (of a microcircuit or integrated circuit). A constituent of the microcircuit or integrated circuit that contributes directly to its operation.

6.2.3 Substrate (of a microcircuit or integrated circuit). The supporting material upon or within which the elements of a microcircuit or integrated circuit are fabricated or attached.

6.2.4 Integrated circuit (microcircuit). A small circuit having a high equivalent circuit element density, which is considered as a single part composed of interconnected elements on or within a single substrate to perform an electronic circuit function.

6.2.4.1 Multichip microcircuit. An integrated circuit or microcircuit consisting of elements formed on or within two or more semiconductor chips which are separately attached to a substrate or package.

6.2.4.2 Monolithic microcircuit. An integrated circuit or microcircuit consisting exclusively of elements formed in situ on or within a single semiconductor substrate with at least one of the elements formed within the substrate.

6.2.4.3 Microcircuit module. An integrated circuit, which is an assembly of microcircuits or an assembly of microcircuits and discrete parts, designed to perform one or more electronic circuit functions, and constructed such that for the purposes of specification testing, commerce, and maintenance, it is considered indivisible.

6.2.5 Production lot. A production lot consist of devices manufactured on the same production line(s) (QM technology flow) by means of the same production technique, materials, controls, and design.

* 6.2.6 Inspection lot. A quantity of integrated circuits submitted at one time for inspection to determine compliance with the requirements and acceptance criteria of the applicable device specification. Each inspection lot is to be manufactured on the same production line through final seal by the same production techniques.

6.2.7 Wafer lot. A wafer lot consists of integrated circuit wafers formed into a lot at the start of wafer fabrication for homogeneous processing as a group, and assigned a unique identifier or code to provide traceability.

6.2.8 Percent Defective Allowable (PDA). Percent defective allowable is the maximum observed percent defective which will permit the lot to be accepted after the specified 100 percent test.

6.2.9 Delta limit. The maximum change in a specified parameter reading which will permit a device to be accepted on the specified test, based on a comparison of the present measurement with a specified previous measurement.

NOTE: When expressed as a percentage value, it should be calculated as a proportion of the previous measured value.

6.2.10 Rework. Any processing or reprocessing operation documented in accordance with the manufacturer's QM plan, other than testing, applied to an individual device, or part thereof, and performed subsequent to the prescribed nonrepairing manufacturing operations which are applicable to all devices of that type at that stage.

6.2.11 Final seal. That manufacturing operation which completes the enclosure of a device so that further internal processing cannot be performed without disassembling the device.

6.2.12 Acquiring activity. The organizational element which contracts for articles, supplies, or services; or it may be a contractor or subcontractor when the organizational element has given specific written authorization to such contractor or subcontractor to serve as agent of the acquiring activity. A contractor or subcontractor serving as agent of the acquiring activity does not have the authority to grant waivers, deviations, or exceptions to this specification unless specific written authorization to do so has been given by the organization (i.e., preparing activity, qualifying activity).

6.2.13 Qualifying activity. The organizational element of the Government that grants certification, and qualification for the specific technology flow in accordance with this specification.

6.2.14 Parts Per Million (PPM). Parts per million is as defined in ANSI/EIA-557.

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6.2.15 Device type. The term device type refers to a single specific microcircuit configuration.

6.2.16 Die type. A microcircuit manufactured using the same physical size, materials, topology, mask set, process flow, on a single fabrication line.

* 6.2.17 Radiation Hardness Assurance (RHA). The portion of product assurance which assures that parts continue to perform as specified or degrade in a specified manner when subjected to the specified radiation environmental stress. The RHACL (radiation hardness assurance capability level) is the radiation level which the manufacturer chooses for each radiation environment appropriate to his technology as a consistently achievable exposure level that does not cause degradation in the microcircuit beyond the specified level of performance.

6.2.18 Electrostatic Discharge Sensitivity (ESD). ESD is defined as the level of susceptibility of a device to damage by static electricity. The level of susceptibility of a device is found by ESD classification testing and is used as the basis for assigning an ESD class.

6.2.19 Package family. A group of package types with identical configuration and process techniques (e.g., cerdip, side braze, cerpack).

6.2.20 Technology flow. A technology flow is that specific manufacturing line from design, fabrication, assembly, packaging, and test in a given technology from which a manufacturer designs, builds, and tests integrated circuits. Once a manufacturer's technology flow has been certified and qualified by the qualifying activity, it is listed on the qualified manufacturer's listing.

6.2.21 Qualified Manufacturer's Listing (QML). The qualified manufacturer's listing is that listing which defines and specifies the certified and qualified technology flow of a manufacturer from which QML integrated circuits may be purchased.

6.2.22 Third party design center. A subcontract design center, or an OEM design center, that uses a microcircuit manufacturer's design tools (including approved industry/third party tools), interface procedures, design rules, and design controls.

6.2.23 Radiation Source of Supply (RSS). A company (e.g., Original Equipment Manufacturer (OEM)) who establishes a relationship with a device manufacturer for the sole purpose of developing qualified Radiation Hardness Assured (RHA) product and has the responsibility to incur the radiation response of said product to the requirements of MIL-PRF-38535, the applicable detail specification, and the RSS program plan. The RSS will be listed in the QML for those devices covered by the RSS's QML. All requests for this product will be submitted through the RSS.

6.2.24 Form. The shape, size, dimension, mass, weight, and other visual parameters which uniquely characterize an item. For software, form denotes the language and media.

6.2.25 Fit. The ability of an item to physically interface or interconnect with or become an integral part of another item.

6.2.26 Function. The action or actions which an item is designed to perform.

6.2.27 Class M. Items which have been subjected to and passed all applicable requirements of Appendix A herein and are documented on an SMD.

6.2.28 Class N. Items which have been subjected to and passed all applicable requirements of this specification including qualification testing, screening testing, and TCI/QCI inspections, and are encapsulated in plastic.

6.2.29 Class Q. Items which have been subjected to and passed all applicable requirements of this specification including qualification testing, screening testing, and TCI/QCI inspections.

6.2.30 Class V. Items which meet all the Class Q requirements and have been subjected to and passed all applicable requirements of appendix B herein.

6.3 Discussion. The foundation of generic qualification is the instillment of Quality Management (QM) within the manufacturing environment. QM requires that all levels of management and non-management be actively involved in the commitment to quality. Also, a TRB must be established to control, stabilize, monitor and improve the qualified technology. The TRB should develop a quality management plan that outlines how the manufacturing operation for a given technology is controlled, monitored and improved throughout its entire "life cycle". Key aspects of this plan are the establishment of statistical process control, field failure return programs, corrective action procedures, quality improvement and any other approaches required to control and improve product quality and reliability. These requirements are detailed in this document.

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Further, this document describes procedures and requirements for manufacturer's listing on the QML for integrated circuits. Manufacturers listed on the QML will be able to produce microcircuits without the need for extensive end-of-manufacturing qualification testing and quality conformance inspections on each device design. The reduction of the end-of-manufacturing testing will be replaced with in-line monitoring and testing and Statistical Process Controls (SPC). Also, surrogate devices, such as the SEC will be used to assess the technology's reliability. Introduction of this methodology shifts the emphasis from the need of individual microcircuit qualification to process (technology) certification and qualification. This will accelerate the microcircuit insertion cycle of high quality and reliable microcircuits.

The generic qualification philosophy, leading to QML, is a process by which a manufacturer acquires a manufacturing line or technology flow certification and qualification. Ongoing monitoring techniques will be used to maintain QML status. The manufacturing line consists of facilities and procedures appropriate to accomplish the design, mask making, wafer fabrication, assembly, package and testing of microcircuits (see figure 2). Figure 3 illustrates six possible combinations of a manufacturing line utilizing three design centers, two mask fabrication facilities, three wafer fabrication facilities, two package and assembly sites and two test facilities. The procedure of generic qualification is accomplished in two stages; certification and qualification. The process of certification is the recognition of evidence by the qualifying activity that the manufacturing line is capable of producing microcircuits of high quality and compliant with the requirements of this document. Qualification is the actual demonstration of the certified manufacturing line capabilities by producing "first pass" microcircuits compliant with the requirements of this document and the device specification. On figure 3, each block can be individually reviewed, but must be certified as a flow. The only process flow which would be qualified (QML listed) would be the group of blocks which are linked together and tested during qualification. The letters "A" and "B" indicate a QML flow where qualification testing has qualified a complete path. The other paths are not QML
until certification and qualification testing of the processes is done.

FIGURE 2. The QML manufacturing line.

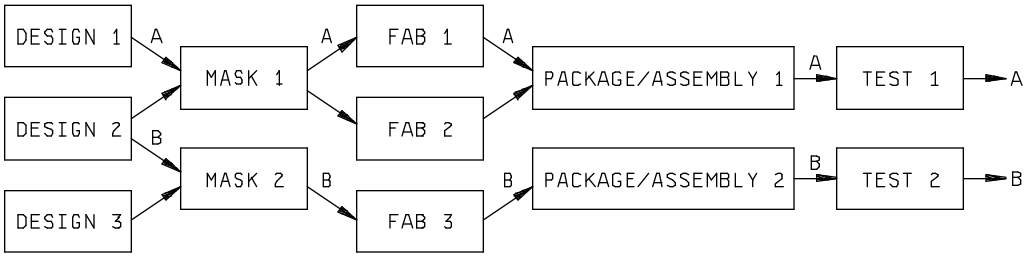

FIGURE 3. Combinations of a manufacturing line.

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QM does not stop with a manufacturer listed on the QML. This specification identifies the necessary screens which QML devices must be capable of meeting. These screens can be reduced or changed by the manufacturers' TRB when gathered reliability data on the technology indicates that such changes are substantiated. The philosophy of generic qualification incorporates the idea that high quality and reliable microcircuits can be obtained without excessive testing if the processes are properly monitored and controlled at each step of the manufacturing line. The following describes the monitors and controls which may be used.

a. The design procedure and tools are controlled in such a manner that the ensuing microcircuit design performs only with limits that have been shown to be reliable for the technology being used, within the constraints of established design rules (electrical, geometric and reliability).

b. The mask fabrication facility is controlled such that an error free mask is produced from the microcircuit design database. Monitoring, controlling and reducing defect density is helpful in obtaining error free masks.

c. The wafer fabrication process is controlled with the following: use of in-line statistical control; a parametric monitor structure for measuring electrical parameters; a TCV structure to study intrinsic reliability mechanisms; and a SEC to monitor the fabrication process and to serve as a surrogate microcircuit for reliability testing.

d. The package and assembly facility is controlled with emphasis on in-line statistical process control of all assembly steps.

e. The test area controls consist of test equipment accuracy and calibration as well as a controlled interface to the microcircuit design center.

f. The overall control of the processes are under the auspices of a TRB which is established by the manufacturer. The TRB is solely responsible for the QML flow that has been certified and qualified.

g. For RHA devices, procedures and requirements are integrated into this document for establishing and demonstrating a RHACL for the technology. Many device oriented tests can be reduced or eliminated when correlation data for models and test structures have been established by the TRB. The main concern in the RHA community is whether the device specification accurately describes the device performance in the radiation environment specified. Until such models and test structures are developed, some actual device radiation testing will be required.

h. Appendix B to this specification defines an implementation transition approach which may be used for space or other critical environment applications.

* 6.4 Additional reference documents. The following documents are not directly referenced herein but should be used as guidelines.

DNA-TR-36-38	-	Hardness Assurance Guidelines for MIL-HDBK-339(USAF).
MIL-HDBK-814	-	Ionizing Dose and Neutron Hardness Assurance Guidelines for Microcircuits.
MIL-HDBK-815	-	Dose-Rate Hardness Assurance Guidelines.
MIL-HDBK-816	-	Guidelines for Developing Hardness Assured Device Specifications.
MIL-HDBK-817	-	System Development Radiation Hardness Assurance.
MIL-HDBK-339	-	Custom Large Scale Integrated Circuit for Space Applications.

AMERICAN SOCIETY FOR TESTING AND MATERIALS (ASTM)

ASTM B487-79	-	Measurement of Metal and Oxide Coating Thicknesses by Microscopical Examination of a Cross Section.
ASTM B567-79A	-	Measurement of Coating Thickness by the Beta Backscatter Method.

(Application for copies should be addressed to the American Society for Testing and Materials, 1916 Race Street, Philadelphia, PA 19103.)

ELECTRONIC INDUSTRIES ASSOCIATION (EIA)

EIA-STD-541	-	Packaging Materials Standard for Electrostatic Discharge Sensitive Items.
JEDEC publication 95	-	JEDEC Registered and Standard Outlines for Semiconductor Devices.
JEDEC publication 16	-	Assessment of Microcircuit Outgoing Quality Levels in Parts Per Million (PPM).

(Application for copies should be addressed to the Electronic Industries Association, 2500 Wilson Boulevard, Arlington, VA 22201-3834.)

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6.5 Subject term (key word) listing.

*

Application Specific Integrated Circuit (ASIC)
Computer Automated Design (CAD)
Design-For-Test (DFT)
Design Rule Check (DRC)
Electrical Rule Check (ERC)
Electrostatic Discharge Sensitivity (ESD)
Failure Analysis (FA)
Joint Test Action Group (JTAG)
Linear Energy Transfer Threshold (LET_{TH})
Mean-Time-to-Failure (MTF)
Parametric Monitor (PM)
Post Irradiated end-point Parameter Limits (PIPL)
Quality Assurance (QA)
Quality Management (QM)
Radiation Hardness Assurance (RHA)
Radiation Hardness Assurance Capability Level (RHACL)
Single Event effects (SEE)
Standard Evaluation Circuit (SEC)
Statistical Process Control (SPC)
Technology Characterization Vehicle (TCV)
Technology Conformance Inspection (TCI)
Technology Review Board (TRB)
Time Dependent Dielectric Breakdown (TDDB)
Very High Speed Integrated Circuit (VHSIC)
VHSIC Hardware Description Language (VHDL)

* 6.6 Changes from previous issue. The margins of this revision are marked with an asterisk to indicate where changes were made. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations and relationship to the last previous issue. All paragraph numbers in the appendices were changed to reflect changes in MIL-STD-961.

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APPENDIX A

CLASS LEVEL B AND S REQUIREMENTS

A.1 SCOPE

A.1.1 Scope. This appendix establishes the minimum requirements for class level B and S monolithic and multichip microcircuits and the quality and reliability assurance requirements which must be met in the acquisition of these microcircuits. Detail requirements, specific characteristics of microcircuits, and other provisions which are sensitive to the particular use intended shall be specified in the applicable device specification. Two levels, class B and S, of product assurance requirements and control for monolithic and multichip microcircuits are provided for in this appendix. It is the intent of the Government that a compliant manufacturer can use this appendix as the first step to becoming a qualified manufacturer under the QML program. Appendix A is mandatory for those manufacturers who choose the option to be compliant to this appendix.

A.2 APPLICABLE DOCUMENTS

A.2.1 General. The documents listed in this section are specified in sections A.3, A.4, and A.5 of this appendix. This section does not include documents cited in other sections of this appendix or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements documents cited in sections A.3, A.4, and A.5 of this appendix, whether or not they are listed.

A.2.2 Government documents.

A.2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATIONS

* DEPARTMENT OF DEFENSE

MIL-I-23011	-	Iron-Nickel Alloys for Sealing to Glass and Ceramics.
MIL-I-46058	-	Insulating Compound, Electrical (For Coating Printed Circuit Assemblies).

STANDARDS

* DEPARTMENT OF DEFENSE

MIL-STD-280	-	Definitions of Item Levels, Item Exchangeability, Models and Related Terms.
MIL-STD-973	-	Configuration Management.
MIL-STD-883	-	Test Methods and Procedures for Microelectronics.
MIL-STD-1285	-	Marking of Electrical and Electronic Parts.
MIL-STD-1835	-	Interface Standard for Microcircuit Case Outlines.

HANDBOOKS

* DEPARTMENT OF DEFENSE

MIL-HDBK-780	-	Standard Microcircuit Drawings.
MIL-HDBK-1331	-	Parameters to be Controlled for the Specification of Microcircuits.
MIL-HDBK-103	-	List of Standard Microcircuit Drawings (SMD's)

* (Unless otherwise indicated, copies of the above specifications, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094).

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A.2.2.2 Other Government documents, drawings, and publications. The following other Government documents, drawings, and publications form a part of this document to the extent specified herein. Unless otherwise specified, the issues shall be those cited in the solicitation.

NAVSHIPS 0967-190-4010 - Manufacturer's Designating Symbols.
* DSCC-VQC-42 - Baseline Sheet for Microcircuits Materials and Construction
HANDBOOK H4/H8 - Commercial and Government Entity (CAGE) Handbook.

* (Copies of MIL-HDBK-103 and DSCC-VQC-42 are available from Defense Supply Center Columbus, 3990 E. Broad Street, Columbus OH 43216-5000. Copies of HANDBOOK H4/H8 are available from Commander, Defense Logistics Services Center, Battle Creek, MI 49017-3084. Copies of NAVSHIPS 0967-190-4010 are available from Standardization Documents Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094. Specifications, standards, and other Government documents required by contractors in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

A.2.3 Non-Government publications. The following documents form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents which are DOD adopted are those listed in the issue of the DoDISS cited in the solicitation. Unless otherwise specified, the issues of documents not listed in the DoDISS are the issues of the documents cited in the solicitation.

AMERICAN SOCIETY FOR TESTING AND MATERIALS (ASTM)

ASTM F15 - Iron-Nickel-Cobalt Sealing Alloy, Specification for.
ASTM F30 - Iron-Nickel Sealing Alloy, Specification for.
ASTM B170 - Oxygen-Free Electrolytic Copper, Refinery Shapes.
ASTM B487 - Measurement of Metal and Oxide Coating Thicknesses by Microscopical Examination of a Cross Section.
ASTM B567 - Measurement of Coating Thickness by the Beta Backscatter Method.
ASTM B568 - Measurement of Coating Thickness by X-Ray Spectrometry.

(Application for copies should be addressed to the American Society for Testing and Materials, 1916 Race Street, Philadelphia, PA 19103.)

AMERICAN NATIONAL STANDARDS INSTITUTE (ANSI)

ANSI/NCSL Z540-1 - Calibration Laboratories and Measuring and Test Equipment - General Requirements

(Application for copies should be addressed to the American National Standards Institute, Incorporated, 1430 Broadway, New York, NY 10018.)

ELECTRONIC INDUSTRIES ASSOCIATION (EIA)

EIA-STD-541 - Packaging Materials Standard for Electrostatic Discharge Sensitive Items.
EIA-STD-625 - Requirements for Handling Electrostatic Discharge Sensitive (ESDS) Devices.
JEDEC Publication 109 - General Requirements for Distributors of Military Integrated Circuits.
JEDEC Standard 114 - Guidelines for Particle Impact Noise Detection (PIND) Testing, Operator Training, and Certification.

(Applications for copies of EIA/JEDEC documents should be addressed to Global Engineering Documents, 15 Inverness Way East, Englewood, CO 80112-5704.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

* A.2.4 Order of precedence. In the event of a conflict between the text of this appendix and the references cited herein (except for device specifications), the text of this appendix takes precedence. Nothing in this appendix or document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

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A.3 REQUIREMENTS

* A.3.1 General. The manufacturer of microcircuits in compliance with this appendix shall have and use production and test facilities and a quality and reliability assurance program adequate to assure successful compliance with the provisions of this appendix, the manufacturer's baseline (DSCC-VQC-42 or equivalent) and the device specification or drawing. The individual item requirements shall be as specified herein, and in accordance with the device specification or drawing.

The requirements of this appendix or 1.2.1 of MIL-STD-883 are met or exceeded by product built to a QML certified flow by a QML certified and qualified manufacturer or by a manufacturer who has been granted transitional certification to MIL-PRF-38535. The QML flow as documented in the QM plan allows modification to processes and tests used in producing QML devices. These changes shall not affect the form, fit, or function of any devices defined by device class M SMDs, the manufacturer's 883 compliant class B data book product, or contractor prepared drawings which call out these devices released before 31 Dec 93, or the date the product becomes QML whichever is the later date. Generic 883 compliant data book product introduced by the manufacturer after 31 Dec 93 shall be submitted to DSCC for review and possible standardization action. These devices are marked with the "Q" or "QML" certification mark to reflect the QML flow used. The acquiring activity shall be notified of the marking prior to shipping of these devices.

* A.3.1.1 Reference to device specification or drawing. For purposes of this appendix, when the term "as specified" is used without additional reference to a specific location or document, the intended reference shall be to the device specification or drawing which constitutes the applicable individual device specification.

* A.3.1.2 Conflicting requirements. In the event of conflict between the requirements of this appendix, this specification and other requirements of the applicable device specification, the precedence in which requirements shall govern, in descending order, is as follows:

a. Applicable device specification or drawing.

b. This appendix.

c. Specifications, standards, and other documents referenced in A.2.2 and A.2.3.

A.3.1.3 Terms, definitions, and symbols. For the purpose of this appendix, the terms, definitions, and symbols of MIL-STD-883 and MIL-HDBK-1331, and those contained herein shall apply and shall be used in the applicable device specifications or drawings wherever they are pertinent. The definitions of part, subassembly, assembly, unit, group, set, and system, as well as the ancillary terms accessory and attachment are contained in MIL-STD-280. To further define a particular type of microcircuit, additional modifiers may be prefixed.

A.3.1.3.1 Microelectronics. That area of electronic technology associated with or applied to the realization of electronic systems from extremely small electronic parts or elements.

A.3.1.3.2 Element (of a microcircuit or integrated circuit). A constituent of the microcircuit or integrated circuit that contributes directly to its operation. (A discrete part incorporated into a microcircuit becomes an element of the microcircuit.)

A.3.1.3.3 Substrate (of a microcircuit or integrated circuit). The supporting material upon or within which the elements of a microcircuit or integrated circuit are fabricated or attached.

A.3.1.3.4 Microcircuit. A small circuit having a high equivalent circuit element density, which is considered as a single part composed of interconnected elements on or within a single substrate to perform an electronic circuit function. (This excludes printed wiring boards, circuit card assemblies, and modules composed exclusively of discrete electronic parts.)

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A.3.1.3.4.1 Multichip microcircuit. A microcircuit consisting of elements formed on or within two or more semiconductor chips which are separately attached to a substrate or package.

A.3.1.3.4.2 Hybrid microcircuit. A microcircuit consisting of elements which are a combination of the film microcircuit type (see A.3.1.3.4.4) and the semiconductor types (see A.3.1.3.4.1 and A.3.1.3.4.3) or a combination of one or both of the types with discrete parts.

A.3.1.3.4.3 Monolithic microcircuit (or integrated circuit). A microcircuit consisting exclusively of elements formed in situ on or within a single semiconductor substrate with at least one of the elements formed within the substrate.

A.3.1.3.4.4 Film microcircuit (or film integrated circuit). A microcircuit consisting exclusively of elements which are films formed in situ upon an insulating substrate.

A.3.1.3.5 Microcircuit module. An assembly of microcircuits or an assembly of microcircuits and discrete parts, designed to perform one or more electronic circuit functions, and constructed such that for the purposes of specification testing, commerce, and maintenance, it is considered indivisible.

A.3.1.3.6 Production lot. A production lot shall consist of devices manufactured on the same production line(s) by means of the same production technique, materials, controls, and design. Where a production lot identification is terminated upon completion of wafer or substrate processing, or at any later point prior to device sealing, it shall be permissible to process more than a single device type in a single production lot provided traceability is maintained by assembling devices into inspection lots, as defined herein, at the point where production lot identification is terminated.

A.3.1.3.7 Inspection lot - class level S. An inspection lot for class level S microcircuits shall consist of a single device type from a maximum of four wafer lots in a single package type and lead finish. All devices shall be sealed within a single week. All assembly operations from die mounting through package sealing shall be completed within the same 6-week period. Each inspection sublot shall be uniquely identified to maintain traceability of that sublot from the wafer lot to the inspection lot (see A.3.4.6 and A.4.3.3).

A.3.1.3.8 Inspection lot - class level B. A quantity of microcircuits submitted at one time for inspection to determine compliance with the requirements and acceptance criteria of the applicable device specification. Each inspection lot shall consist of microcircuits of a single device type, in a single package type and lead finish. Each inspection lot shall be manufactured on the same production lines through final seal by the same production techniques and sealed within the same period not exceeding 6 weeks. Inspection lot identification shall be maintained from the time the inspection lot is formed through the time the lot is accepted, and shall be traceable to the production lot(s) from which the inspection lot was formed (see A.3.4.6 and A.4.3.3).

A.3.1.3.9 Inspection sublot - class level S. An inspection sublot for class level S microcircuits shall be a division (one wafer lot maximum) of parts in an inspection lot into smaller quantities of parts (see A.4.5.2 herein).

A.3.1.3.10 Inspection lot split - class level B. A class level B inspection lot split shall be a further division of the number of parts in an inspection lot into smaller quantities of parts (see A.4.5.2 herein).

A.3.1.3.11 Wafer lot. A wafer lot consists of microcircuit wafers formed into a lot at the start of wafer fabrication for homogeneous processing as a group, and assigned a unique identifier or code to provide traceability, and maintain lot integrity throughout the fabrication process (see A.4.3.3 herein).

A.3.1.3.12 Package type. A package with a unique case outline (see MIL-STD-1835), configuration, materials (including bonding wire and die attach), piece parts (excluding preforms which differ only in size), and assembly processes.

A.3.1.3.13 Microcircuit group. Microcircuits which are designed to perform the same type of basic circuit function (e.g., for linear: Amplifier, comparator, sense amplifier, regulator, etc.; for digital: Logic gate buffer, flip-flop, combinational gate, sequential register/counter) within a given circuit technology (e.g., DTL, Non-Schottky TTL, ECL, Schottky TTL, Linear, Hybrid, MOS) which are designed for the same supply, bias and signal voltages and for input-output compatibility and which are fabricated by use of the same basic die construction and metallization; the same die attach method; and by use of bonding interconnects of the same size, material and attachment method.

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A.3.1.3.14 Percent defective allowable (PDA). Percent defective allowable is the maximum observed percent defective which will permit the lot to be accepted after the specified 100 percent test.

* A.3.1.3.15 Delta limit (Δ). The maximum change in a specified parameter reading which will permit a device to be accepted on the specified test, based on a comparison of the present measurement with a specified previous measurement. Note: When expressed as a percentage value, it shall be calculated as a proportion of the previous measured value.

A.3.1.3.16 Rework. Any processing or reprocessing operation documented in accordance with A.4.8.1.1.6h herein, other than testing, applied to an individual device, or part thereof, and performed subsequent to the prescribed nonrepairing manufacturing operations which are applicable to all devices of that type at that stage.

A.3.1.3.17 Final seal. That manufacturing operation which completes the enclosure of a device so that further internal processing cannot be performed without disassembling the device.

A.3.1.3.18 Acquiring activity. The organizational element of the Government which contracts for articles, supplies, or services; or it may be a contractor or subcontractor when the organizational element of the Government has given specific written authorization to such contractor or subcontractor to serve as agent of the acquiring activity. A contractor or subcontractor serving as agent of the acquiring activity shall not have the authority to grant waivers, deviations, or exceptions to this appendix unless specific written authorization to do so has also been given by the Government organization (i.e., preparing activity).

A.3.1.3.19 Qualifying activity. The organizational element of the Government that grants certification and qualification for the specific associated end-product in accordance with this appendix and the applicable device specification or drawing. For non-JAN product build in accordance with this appendix, the qualifying activity shall be either the acquiring activity or quality organization within the manufacturer's company that is independent of the group(s) responsible for device production screening and marketing or by an independent organization outside the manufacturer's company.

A.3.1.3.20 Device type. The term device type refers to a single specific microcircuit configuration. Samples of the same device type will be electrically and functionally interchangeable with each other at the die or substrate level even though made by different manufacturers using different mechanical layouts and possibly different materials. The electrical and environmental limits will be the same (but not necessarily the inherent reliability) for a given device type even though the device class, the case outline, the lead finish, the lot identification code, and the manufacturer may be different.

A.3.1.3.21 Die type. A microcircuit manufactured using the same physical size, materials, topology, mask set, and process flow, on a single fabrication line.

A.3.1.3.22 Antistatic. An antistatic material resists triboelectric charging upon contact and separation with another material. Plastic materials impregnated with antistatic agents (antistats) are antistatic if their surface resistivity is between 10^9 and 10^{14} ohms/square.

A.3.1.3.23 Conductive. A conductive material is one capable of electrostatic field shielding and having a volume resistivity of 10^3 ohm-cm maximum or a surface resistivity less than 10^5 ohms/square.

A.3.1.3.24 Insulating. An insulating material is defined as having a volume resistivity of 10^{12} ohm-cm minimum, or a surface resistivity of 10^{14} ohms/square minimum.

A.3.1.3.25 Dissipative. A dissipative material is defined as having a surface resistivity between 10^5 and 10^9 ohms/square.

A.3.1.3.26 Radiation hardness assurance (RHA). The portion of product assurance which insures that parts continue to perform as specified or degrade in a specified manner when subjected to the specified radiation environmental stress.

A.3.1.3.27 Electrostatic discharge sensitivity (ESDS). Electrostatic discharge sensitivity is defined as the level of susceptibility of a device to damage by static electricity. The level of susceptibility of a device is found by ESDS classification testing and is used as the basis for assigning an ESDS class (see A.3.4.1.4).

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A.3.1.3.28 Custom microcircuits. A nonstandard microcircuit, the design, and right(s) to the design (for example, ownership, control, or proprietary rights) of which are under the control of the purchaser-user of the microcircuit.

A.3.1.3.29 Die family. All devices manufactured by the same basic process (e.g., low power Schottky, HCMOS, FAST) as specified in tables A-VI, A-VII, A-VIII, and A-IX.

A.3.1.3.30 Package family. A set of package types with the same package configuration (e.g., side brazed, bottom brazed) material type (e.g., alumina, beryllium oxide (BeO)) package construction techniques (e.g., single layer, multilayer) terminal pitch, except for can packages in which pin circle diameter can be used in place of terminal pitch, lead shape (e.g., gullwing, J-hook), and row-spacing (i.e., dual-in-line packages only) and with identical package assembly techniques (e.g., material and type of seal, wire bond method and wire size, die attach method and material).

A.3.1.3.31 Military operating temperature range. The military temperature range or military operating temperature range is defined as -55°C to +125°C.

A.3.1.3.32 Process monitor. The regularly scheduled periodic sample measuring of a parameter during normal performance of production operations in accordance with the manufacturer's approved program plan. The parameter to be measured, the frequency of measurement, the number of sample measurements, the conditions of measurement, the analysis of measurement data will vary as a function of the requirements, capability and criticality of the operation being measured.

A.3.1.3.33 Device specification. The terms device specification or Standard Microcircuit Drawing (SMD) shall be used exclusively to reference or describe Government published documents with the combined purposes of standardization and procurement which detail the specific requirements of performance based microcircuits.

A.3.1.3.34 Class level B. Items which have been subjected to and passed all applicable requirements of this appendix including screening tests, qualification testing, and quality conformance inspections, except those identified as class level S only.

A.3.1.3.35 Class level S. Items which meet all the Class level B requirements and those identified as Class level S only.

A.3.2 Item requirements. The individual item requirements for microcircuits delivered under this appendix shall be documented in the device specification or Standard Microcircuit Drawing or other drawing (SMD format, in accordance with MIL-HDBK-780, shall be used for drawings). Unless otherwise specified in the device specification or drawing, all devices procured under this appendix shall have an operating ambient temperature range from -55°C to +125°C and any references to minimum or maximum operating temperatures shall refer to the respective lower and upper limits of this range. Contractor-prepared specifications or drawings shall be approved by the acquiring activity as acceptable for the requirements of a specific contract or order, at the time of acquisition.

A.3.2.1 Electrical test requirements. The electrical test requirements (parameters, test conditions, test limits, and applicable test temperatures) which apply to electrical screening (i.e., final electrical parameters), Group A Quality Conformance Inspection (QCI), and endpoint electrical testing for other QCI subgroups shall be clearly documented by the manufacturer as to the actual parameters, conditions, methods, limits, burn-in/life test circuits, and test temperatures used in device testing. All those parameters important to the design application of the device shall be specified over the full military operating temperature range and supply voltage range and be included in the testing requirements of the applicable specification(s). For devices whose initial release date is after 29 May 1987, the subgroups to be tested, and the parameters that constitute a subgroup shall as a minimum be equivalent to those of the most similar device specification or drawing. The manufacturer's electrical test specification must be documented in a device specification table I format, or equivalent, that is clear to the user and must be available to the user upon request.

A.3.2.2 Die/fabrication requirements. When deemed necessary by the preparing or acquiring activity, (e.g., a class M SMD device, a DSCC drawing device, an 883 compliant device or a QPL device or a unique package/die combination is not available from a DSCC drawing, SMD, QML, or QPL source that meets the full wafer fabrication requirements of this appendix), the DSCC drawing, SMD, JAN slash sheet or other procurement document may be modified to provide a source for logistics support. This modification will allow either a detailed certificate of compliance (itemized listing of die fabrication requirements from this appendix - see example in A.3.2.2.1 herein) or a die evaluation as defined by paragraph A.3.2.2.2 herein to be used in lieu of the full fabrication requirements. The manufacturer that meets the die/fabrication requirements by utilizing die evaluation is required to perform QCI testing of Groups C and D (and E if applicable) on the first inspection lot of each wafer lot and shall replace the “C” certification mark with a “D” certification mark. An additional complete Group D test is not required if the manufacturer already has Group D coverage on the package family, however, Subgroups D3 and D4 shall be required on the first inspection lot of the wafer lot. For excess die from the evaluated wafer lot, an additional Group C and Group D (subgroups D3 and D4 only) tests are not required for subsequent inspection lots built solely from die from that wafer lot. If the full certificate of compliance documentation is available, the “C” certification mark shall be used on the device.

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A.3.2.2.1 Example C of C. This C of C certifies that the product identified by fabrication code XXXXXX meets the fabrication requirements of Appendix A of MIL-PRF-38535 (1.2.1 of MIL-STD-883) including the following itemized requirements:

a) Change to product requirement of A.3.4.2.
b) Internal conductor (current density) requirements of A.3.5.5.
c) Traceability requirements of A.3.4.6.
d) Glassivation thickness requirements of A.3.5.8.
e) Die thickness requirement of A.3.5.9.
f) Quality Assurance program requirements of A.4.8.
g) Control and traceability of design documentation requirements of A.3.5.4.
h) Workmanship and rework provisions of A.3.7.
i) Design and construction baseline requirements of A.4.8.1.3.8.

A.3.2.2.2 Die evaluation requirements. The following requirements shall be met for each wafer lot. The results of this evaluation shall demonstrate compliance to this appendix for wafer manufacturing requirements.

a) Functional diagram and high power photomicrographs.
b) Analysis of internal conductor materials.
c) Composition of glassivation material and thickness measurement.
d) Total die thickness measurement.
e) SEM analysis of metalization.
f) Adhesion of gold backing.
g) Calculated current density in accordance with this appendix.

A.3.3 Classification of requirements. The requirements of the microcircuits are classified herein as follows:

Requirement	Paragraph
Quality assurance	A.3.4
Qualification	A.3.4.1
General	A.3.4.1.1
Radiation hardness assurance	A.3.4.1.3
Electrostatic discharge sensitivity class	A.3.4.1.4
Change of qualified product	A.3.4.2
Screening	A.3.4.3
Quality conformance inspection	A.3.4.4
Wafer lot acceptance	A.3.4.5
Traceability	A.3.4.6
Design and construction	A.3.5
Marking	A.3.6
Workmanship	A.3.7

A.3.3.1 Certification of conformance and acquisition traceability. Manufacturers or suppliers including dealers and distributors who offer the product described by this appendix shall provide written certification, signed by the corporate officer who has management responsibility for the production and assurance of the quality and reliability of the product, (1) that the product being supplied has been manufactured and tested in accordance with this appendix and conforms to all of its requirements, and can be reasonably expected to remain in conformance indefinitely unless destructively mishandled, (2) that all products are as described on the certificate which accompanies the shipment, and (3) that dealers and distributors have handled the product in accordance with the requirements of EIA-STD-625 and JEDEC Publication 109. The responsible corporate official may, by documented authorization, designate other responsible individuals to sign the certificate, but, the responsibility for conformity with the facts shall rest with the responsible corporate officer. The certification shall be confirmed by documentation to the Government or to users with Government contractors or subcontractors, regardless of whether the products are acquired directly from the manufacturer or from another source such as a distributor. When other sources are involved, their acquisition certification shall be in addition to the certificates of conformance and acquisition traceability provided by the manufacturer and previous distributors. The certificate shall include the following information:

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a. Manufacturer documentation:

(1) Manufacturer's name and address.
(2) Customer's or distributor's name and address.
(3) Device type and product assurance level.
(4) Lot date code and latest reinspection date, if applicable.
(5) Quantity of devices in shipment from manufacturer.
(6) Statement certifying product conformance and traceability.
(7) Solderability reinspection date, if applicable.
(8) Signature and date of transaction.

b. Distributor documentation for each distributor:
(1) Distributor's name and address.
(2) Name and address of customer.
(3) Quantity of devices in shipment.
(4) Latest reinspection date, if applicable.
(5) Certification that this shipment is a part of the shipment covered by the manufacturer's documentation.
(6) Solderability reinspection date, if applicable.
(7) Signature and date of transaction.

A.3.4 Quality assurance requirements. The quality assurance provisions provided in this appendix are intended to provide a class level B or level S device (see A.3.1.3.34 and A.3.1.3.35). Devices or lots which have failed to pass any tests applied or acceptance criterion (PDA) shall not be downgraded to any lower quality assurance level even though that test or criterion may not be a requirement of the lower level (a failed device or lot shall not be accepted). Where shown, method references are in accordance with MIL-STD-883.

A.3.4.1 Qualification. The manufacturer supplying devices in compliance to this appendix shall perform sufficient product qualification testing to assure the devices supplied meet the minimum class level B or S performance requirements as described herein. The manufacturer shall maintain documentation of qualification testing for review of the preparing or acquiring activity upon request.

A.3.4.1.1 Compliance validation. Although audits are not a condition to begin supplying under the requirements of this appendix, all manufacturers supplying in compliance to this appendix are subject to periodic Government compliance validation audits on a drop-in basis with a minimum of notice.

A.3.4.1.2 Process monitor programs. Process monitor programs performed by the manufacturer shall be established as a minimum for the following processes: Scanning Electron Microscope (SEM), wire bonding, die attachment, lid seal, particle detection, lead trimming, and final lead finish thickness. The implementing procedures shall provide for frequency, sample size, reject criteria, allowable rework, and disposition of failed product/lot(s). With the exception of the particle detection monitor, a procedure is required for the traceability, recovery, and disposition of all units monitored since the last successful test. As with all monitors, the particle detection procedure shall provide for continual process improvement. Records of these monitors and procedures shall be maintained and available for review.

A.3.4.1.2.1 Inspection by scanning electron microscope (SEM). A continuing SEM program shall be established to ensure adequate process control and coverage of metallization at oxide steps, contact openings, and general metallization. A monthly (minimum frequency) SEM evaluation shall be performed on product which is in the manufacturing process. The SEM program shall establish routine control over metallization processes by process families or inspection of products.

A.3.4.1.2.2 Wire bonding. The manufacturer shall monitor the wire bond strength in accordance with the manufacturer's documented procedure. The frequency of this procedure shall be performed at machine setup as a minimum. At the manufacturer's option, this procedure shall consider shift start and stop, change of operators, spools, packages, wire size, lot size, and other related factors.

A.3.4.1.2.3 Die attachment. The manufacturer shall monitor the die attachment integrity in accordance with the manufacturer's documented procedure. This procedure shall be performed at each equipment setup as a minimum. At the manufacture's option, this procedure shall consider other related factors.

A.3.4.1.2.4 Lid seal. The manufacturer shall monitor, as a minimum, glass frit packages for seal integrity in accordance with the manufacturer's documented procedure. A sample and test plan shall be available for review by the qualifying or preparing activity.

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A.3.4.1.2.5 Particle detection. The manufacturer shall establish a particle detection monitoring program which assesses the particle contamination of sealed devices on an individual manufacturing line basis. The monitor shall have provisions for testing in accordance with test method 2020, condition A of MIL-STD-883. JEDEC Standard 114, "Guidelines for Particle Impact Noise Detection (PIND) Testing, Operator Training, and Certification" may be used as a guideline. Suitable data for each manufacturing line shall be used to establish an appropriate need, sample size, and sampling frequency for each package family. Unless otherwise approved by the qualifying activity, the minimum sampling frequency of those devices in production shall be once each month per package family. Investigative and corrective actions shall be established which address noted deficiencies. Records of this monitor shall be made available for review and shall represent at least the six month period preceding the audit.

A.3.4.1.2.6 Lead trimming and final lead finish thickness. The manufacturer shall monitor the package lead lengths to assure meeting the applicable device specification or drawing for proper lead length and the final lead finish thickness in accordance with this appendix. The frequency of the lead length monitor shall be performed at each equipment setup as a minimum. A sample and test plan shall be available for review by the qualifying or preparing activity.

* A.3.4.1.3 Qualification to RHA levels. Qualification to an RHA level shall consist of qualification to the appropriate quality and reliability assurance level (class level S or B) plus group E tests in accordance with, test method 5005 of MIL-STD-883. RHA levels are defined as follows:

Radiation hardness assurance (RHA) level

RHA level designator (see A.3.6.2)	Radiation and total dose (Rad (Si))
/ or -	No RHA
M	3000
D	10^4
L	5×10^4
R	10^5
F	3×10^5
G	5×10^5
H	10^6

A.3.4.1.4 Qualification to ESDS classes. Initial qualification to an ESDS class or requalification after redesign shall consist of qualification to the appropriate quality and reliability level (class level S or B) plus ESDS classification in accordance with test method 3015 of MIL-STD-883.

ESDS classification levels are defined as follows:

ESDS class designator	Prior designation category	Marking	Electrostatic voltage
1	A	Δ	0 to 1999 V
2	B	Δ Δ	2000 V to 3999 V
3	---	---	≥ 4000 V

a. Devices existing prior to 30 September 1989 that were not ESDS classification tested shall be marked as class 1 until classified. Devices previously classified by test as category A shall be marked class 1. Devices previously classified by test as category B shall be marked as class 2. If it can be shown that test results obtained using test method 3015.3 correlate with results using test method 3015.6 (or later versions) and give correct ESDS classification, retesting of previously tested devices is not required except where redesign has occurred. Completed (sealed and date coded) devices in inventory or distribution prior to 30 September 1989 need not be remarked for ESDS.

b. Beginning no later than 31 December 1988, all newly designed or redesigned device types shall be classified as ESDS class 1, 2, or 3 in accordance with test method 3015 of MIL-STD-883.

c. After 30 September 1989, in order to be compliant with this appendix or 1.2.1 of MIL-STD-883, all other device types for use in new system or equipment designs or system or equipment redesigns shall have completed classification in accordance with test method 3015 of MIL-STD-883. All devices of existing design (i.e. not subject to A.3.4.1.4b above) shall be marked class 1 except when known by test to be, in fact, class 2 or better, in which case they shall be correctly identified for ESDS.

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d. Although little variation due to case outline is expected, if a device type is available in more than one package type or case outline, ESDS testing and classification shall be applied to at least that one package type shown by experience to be worst case for ESDS.

* e. ESD testing classification results (or class one marking assigned without test) shall be submitted to DSCC-VA for all SMD devices built in compliance to this appendix. ESD testing classification results for non SMD devices built in compliance to this appendix shall be retained by the manufacturer and made available to the acquiring or preparing activity upon request.

A.3.4.2 Change to product or quality assurance program. The manufacturer shall be responsible for the implementation of any major change(s) of the product or quality assurance program which may affect performance, quality, reliability, radiation hardness assurance (when specified), ESDS class, or interchangeability (see table A-I). The information needed to support these changes shall include acceptable engineering data, quality conformance inspection data, or a test plan sufficient to demonstrate that the change(s) will not adversely affect performance, quality, reliability, interchangeability, radiation hardness, or electrostatic discharge sensitivity and that the product will continue to meet the specification requirements.

* A.3.4.2.1 Notification of change. Notification to the acquiring activity of change of product involving devices acquired to any detail specification/drawing/data sheet is required for any class I change, as defined in MIL-STD-973, at the time of acceptance of a new order or delivery of existing order by manufacturer. The manufacturer may make notification of this change of product through the GIDEP using the Product Change Notice, in any case the manufacturer shall assure that all acquiring activities for this product are notified.

A.3.4.3 Screening. All microcircuits to be delivered or submitted for quality conformance in accordance with this appendix shall have been subjected to, and passed, all the screening tests detailed in test method 5004 of MIL-STD-883 for the type of microcircuit and quality assurance level (device class) specified.

A.3.4.4 Quality conformance inspection. Microcircuits shall not be accepted or approved for delivery until the inspection lot has passed quality conformance inspection (see A.4.5).

A.3.4.5 Wafer lot acceptance. Class level S microcircuits furnished under this appendix shall be products from wafer lots that are subjected to and successfully meet the wafer lot acceptance inspections and tests specified in test method 5007 of MIL-STD-883 or equivalent procedures approved by the acquiring activity.

A.3.4.6 Traceability. Traceability shall be provided for all microcircuit quality assurance levels. Each delivered microcircuit shall be traceable to the inspection and wafer lot(s) (see A.4.8.1.2).

A.3.4.6.1 Lot travelers. The manufacturer shall maintain lot travelers to document the completion of each required processing step from wafer diffusion for class level S (and class level B radiation hardened devices) and beginning with assembly for class level B with wafer lot identification through microcircuit assembly and screening test. Travelers shall provide space for those items specified in A.4.8.1.3.7. The lot travelers shall provide traceability to all prior processing steps and shall be identifiable through assembly and acceptance testing and shall be monitored by the manufacturer's quality control organization.

A.3.4.7 Government source inspection. Government source inspection is required as detailed in the contract or a purchase order.

A.3.5 Design and construction. Microcircuit design and construction shall be in accordance with all the requirements specified herein and in the device specification or drawing.

A.3.5.1 Package. All devices supplied under this appendix shall be hermetically sealed in glass, metal, or ceramic (or combinations of these) packages. No organic or polymeric materials (lacquers, varnishes, coatings, adhesives, greases, etc.) shall be used inside the microcircuit package unless specifically detailed in the device specification or drawing (e.g., polyimide interlayer dielectric). Alpha Particle protection is permitted if permitted by the device specification or drawing. Desiccants may be used in the microcircuit package (except for class level S devices where they are prohibited) only if each lot is subjected to and passes an internal water vapor test, test method 1018 of MIL-STD-883, with a limit of 1000 ppm at +100°C for a sample of 3(0) or 5(1). The internal moisture content for class level S devices after completion of all screening shall not exceed 5,000 ppm at +100°C. Polymer impregnations (backfill, docking, coating, or other uses of organic or polymeric materials to effect, improve, or repair the seal) of the microcircuit packages shall not be permitted. Polymer coating used to effect or improve marking adhesion shall not be applied over lid seal area.

NOTE: Packages containing beryllia shall not be ground, sand-blasted, machined, or have other operations performed on them which will produce beryllia or beryllium dust. Furthermore, beryllium oxide packages shall not be placed in acids that will produce fumes containing beryllium.

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* A.3.5.1.1 Polymeric die attach materials. Polymeric die attach materials shall be allowed under the following conditions. Polymeric materials shall be approved by the acquiring or preparing activity. All adhesive materials shall meet the requirements of MIL-STD-883, test method 5011.

A.3.5.1.2 Package configurations. Package configurations (e.g., 14-lead flat package, 16-lead DIP, 20-terminal SQ.CCP, etc.) defined in MIL-STD-1835 shall be in accordance with the case outline of MIL-STD-1835. Package configurations not defined in MIL-STD-1835 shall be specified in the applicable acquisition document, and require approval of the acquiring activity.

A.3.5.2 Metals. External metal surfaces shall be corrosion-resistant or shall be plated or treated to resist corrosion. External leads shall meet the requirements specified in A.3.5.6.

A.3.5.3 Other materials. External parts, elements or coatings including markings shall be inherently nonnutrient to fungus and shall not blister, crack, outgas, soften, flow or exhibit defects that adversely affect storage, operation, board assembly (e.g., permanently attached organic bumpers), or environmental capabilities of microcircuits delivered to this appendix under the specified test conditions.

A.3.5.4 Design documentation. Design, topography, and schematic circuit information for all microcircuits supplied under this appendix shall be available for review by the acquiring activity and the preparing activity upon request. Control and traceability of design documentation for all new designs and redesigns shall follow the guidelines of A.3.5.4.1 through A.3.5.4.4. This design documentation shall be sufficient to depict the physical and electrical construction of the microcircuits supplied under this appendix, and shall be traceable to the specific part, drawing, or type numbers to which it applies, and to the production lot(s) and inspection lot codes under which microcircuits are manufactured and tested so that revisions can be identified.

A.3.5.4.1 Die topography. For semiconductor die (monolithic die or dice for inclusion in multichip microcircuits), there shall be a photograph, drawing(s), mask list with revisions or other representation defining the topography of the elements of the die without the intraconnection pattern.

A.3.5.4.2 Die intraconnection pattern. There shall be an enlarged photograph(s) or transparency of diazotypes of the mask set to the same scale as the die topography (see A.3.5.4.1) showing the specific intraconnection pattern used to connect the elements on the die so that elements used and those not used can be easily determined. For multichip microcircuits, this requirement shall apply to the substrate and all conductor pattern and active or passive circuit elements deposited thereon, as well as to semiconductor die, as applicable.

A.3.5.4.3 Die to terminal interconnection. There shall be an enlarged photograph(s), transparency, or drawing(s) to scale and of sufficient magnification to clearly depict the interconnection pattern for all connections made by wire or ribbon bonding, beam leads or other methods between the semiconductor die, other elements of the microcircuit, substrate(s) and package terminals or lands as applicable to the specific type of microcircuit supplied. If these interconnections show clearly on the die intraconnection pattern photograph, an additional photograph or drawing is not required.

A.3.5.4.4 Schematic diagrams. For microcircuits supplied under this appendix, the actual schematic diagram(s), logic diagram(s), or combination thereof shall be maintained, sufficient to represent all electrical elements functionally designed into the microcircuit together with their values (when applicable). For simple devices, this shall be a complete detailed schematic circuit showing all functional elements and values. For complex devices or those with redundant detail, the overall microcircuit may be represented by a logic diagram in combination with schematic details. As a minimum, details which must be included are: A schematic presentation of input/output stages and protection network details identified by appropriate pin numbers. Sufficient details to depict addressing or other device elements where the test parameters, conditions, or limits are sensitive to the specific device schematics. Where parasitic elements are important to the proper functioning of any microcircuit, they shall be included in the schematic diagram.

A.3.5.5 Internal conductors. Internal thin film conductors on semiconductor die or substrate (metallization stripes, contact areas, bonding interfaces, etc.) shall be designed so that properly fabricated conductor shall not experience in normal operation (at worst case specified operating conditions), a current density in excess of the maximum allowable value shown below for the applicable conductor material:

Conductor material	Maximum allowable current density
Aluminum (99.99 percent pure or doped) without glassivation or without glassivation layer integrity test	2×10^5 A/cm^2
Aluminum (99.99 percent pure or doped) glassivated (see A.3.5.5.4)	5×10^5 A/cm^2
Refractory metals (Mo, W, Ti-W, and Ti-N) glassivated (see A.3.5.5.4)	5×10^5 A/cm^2
Gold	6×10^5 cm^2
All other	2×10^5 A/cm^2

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TABLE A-I. Testing guidelines for changes identified as major.

Major changes		Testing, MIL-STD-883, test method 5005 (All electrical parameters in accordance with the device specification or drawing 1/
a.	Doping material source concentration	Group A and C-1 deltas (variables only when deltas are required)
	Process technique	
b.	Diffusion profile	Group A and C-1 deltas (variables only when deltas are required)
c.	Die structure	Group A and C-1 deltas (variables only when deltas are required)
d.	Mask changes affecting die size or active element	Variable group A, C-1 prior to shipment, and notify qualifying activity if new area is smaller/larger in applicable package than previously qualified.
	Wafer diameter	Group A, C-1 prior to shipment
	Final die thickness	Group D-3
e.	Passivation/glassivation	Group A, C-1 and glass integrity test if current density is over 2×10^5
f.	Metallization changes	Group A, C-1, and B-5
g.	Die attach method	D-3 and D-4
h.	Die attach process	D-3 and D-4
i.	Bond process	B-5 and D-3
j.	Bond wire material/dimension	B-5 and D-3
k.	Package or lid structure	D-1 (variables), D-3, D-4, D-8 (lid torque) (variables)
	Package or lid material	D-3, D-4, D-5, D-6 (variables), and D-8 (lid torque) (variables)
	Package or lid dimension	D-1 (variables), D-2, and D-8 (lid torque) (variables)
	Lead frame material	See A.4.4.2.7
	Lead frame dimension	D-1 (variables) and D-2
	Cavity dimension	B-5, D-2, D-6 (variables), and D-8 (lid torque) (variables)
l.	Sealing profile	D-3, D-4, D-6 (variables), and D-8 (lid torque) (variables)
	Sealing material	D-3, D-4, D-6 (variables), and D-8 (lid torque) (variables)
	Frame attach	B-3, D-3, D-4, D-6 (variables), and D-7 (adhesion of lead finish) (variables)
	Frame cleaning	B-3, D-2, D-3, and D-7 (adhesion of lead finish)
m.	Implementation of test methods	Notify qualifying activity (may involve test demonstration)
n.	Critical documents (see A.4.8.1.3b)	Notify qualifying activity (may involve test demonstration)
o.	Fab move	Group A and C
p.	Assembly move	Group D per each package family (see A.3.1.3.30) prior to ship

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TABLE A-I. Testing guidelines for changes identified as major - Continued.

Major changes		Testing, MIL-STD-883, test method 5005 (All electrical parameters in accordance with the device specification or drawing 1/
q.	Test facility move	Notify qualifying activity
r.	Scribe/die separation	5 SEM photographs of randomly selected die showing one full edge of die front and back
s.	Qualification/QCI procedures	Notify qualifying activity
t.	Passivation for RHA	Group A, E, C-1, and glass integrity test if current density is over 2 x 10^5
u.	Diffusion profile for RHA	Group A, E, and C-1 deltas (variables only when deltas are required).
v.	Sinter/anneal for RHA	Group A, E, C-1, and B-5

1/ This table is for class level B subgroups only. For class level S, use the equivalent class level S subgroups.

The current density shall be calculated at the point(s) of maximum current density (i.e., greatest current (see A.3.5.5a) per unit cross section) for the specific device type and schematic or configuration. Individual device calculations are not required when appropriate documented design rules or requirements have been used, which limit or control the current density in the resulting design.

a. Use a current value equal to the maximum continuous current (at full fanout for digitals or at maximum load for linears) or equal to the simple time-averaged current obtained at maximum rated frequency and duty cycle with maximum load, whichever results in the greater current value at the point(s) of maximum current density. This current value shall be determined at the maximum recommended supply voltage(s) and with the current assumed to be uniform over the entire conductor cross-sectional area.

b. Use the minimum allowed metal thickness in accordance with manufacturing specifications and controls including appropriate allowance for thinning experienced in the metallization step. The thinning factor over a metallization step is not required unless the point of maximum current density is located at the step.

c. Use the minimum actual design conductor widths (not mask widths) including appropriate allowance for narrowing or undercutting experienced in metal etching.

d. Areas of barrier metals, not intended by design to contribute to current carrying capacity, and nonconducting material shall not be included in the calculation of conductor cross section.

Thick film conductors multichip substrates (metallization strips, bonding interfaces, etc.) shall be designated so that no properly fabricated conductor shall dissipate more than 4 watts/cm^2 when carrying, maximum design current.

A.3.5.5.1 Metallization thickness. For class level S microcircuits, the minimum metallization thickness shall be 8,000 Å (800 nm) for single level metal and for the top level of multi-level metal, and 5,000 Å (500 nm) for the lower level(s) of multi-level metal. In all cases, the current density requirements of A.3.5.5 shall also be satisfied.

A.3.5.5.2 Internal wire size and material. For class level S microcircuits, the internal wire diameter shall be .001 inch minimum (0.03 mm) and the internal lead wire shall be of the same metal as the die metallization.

A.3.5.5.3 Internal lead wires. Internal lead wires or other conductors which are not in thermal contact with a substrate along their entire length (such as wire or ribbon conductors) shall be designed to experience, at maximum rated current, a continuous current for direct current, or an RMS current (peak current divided by $\sqrt{2}$), for alternating or pulsed current, not to exceed the values established by the following relationship:

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$$I = Kd^{3/2}$$

where: I = Maximum allowed current in amperes.
d = Diameter in inches for round wire (or equivalent round wire diameter which would provide the same cross-sectional area for other than round wire internal conductor).
K = A constant taken from the table below for the applicable wire or conductor length and composition used in the device.

Composition	"K" values for bond-to-bond total conductor length	
	Length ≤ 0.040" (0.10 cm)	Length > 0.040" (0.10 cm)
Aluminum	22,000	15,200
Gold	30,000	20,500
Copper	30,000	20,500
Silver	15,000	10,500
All other	9,000	6,300

A.3.5.5.4 Verification of glassivation layer integrity. Where the current density of aluminum metallization for a device type to be qualified exceeds the allowable current density for unglassivated aluminum, the device type shall be subjected to and pass the requirements of MIL-STD-883, test method 2021 prior to qualification and the glassivation layer integrity sample used along with and a photograph of the etched die shall be documented and maintained. One resubmission is permitted at twice the sample size. Unless otherwise specified by the qualifying activity, the device type shall be tested after sealing (or after exposure to the time/temperature sealing profile) in the package type that receives the highest temperature range during sealing for which the device type is to be qualified. Changes in design, materials, or process which affect current density or glassivation shall also be evaluated using MIL-STD-883, test method 2021. This evaluation applies only when the current density requirements for unglassivated aluminum are exceeded.

A.3.5.6 Package element material and finish.

A.3.5.6.1 Package material. Package body material shall be metal, glass, or ceramic in accordance with A.3.5.1.

* A.3.5.6.2 Lead or terminal material. Lead or terminal material shall conform to one of the following compositions:

a. Type A: Iron-nickel-cobalt alloy: MIL-I-23011, class I, ASTM F15.

b. Type B: Iron-nickel alloy (41 percent nickel): MIL-I-23011, class 5, ASTM F30.

c. Type C: Co-fired metallization such as nominally pure tungsten. The composition and application processing of these materials shall be subject to qualifying activity approval and submitted with application to test and as otherwise requested by the qualifying activity.

d. Type D: Copper-core, iron-nickel ASTM F30 alloy (50.5 percent nickel). The core material shall consist of copper (oxygen-free), ASTM B170, grade 2.

e. Type E: Copper-core ASTM F15 alloy. The core material shall consist of copper (oxygen-free) ASTM B170, grade 2.

f. Type F: Copper (oxygen-free) ASTM B170, grade 2. This material shall not be used as an element of any glass-to-metal seal structure.

g. Type G: Iron-nickel alloy (50.5 percent nickel): MIL-I-23011, class 2, ASTM F30.

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A.3.5.6.3 Microcircuit finishes. Finishes of all external leads or terminals and all external metal package elements shall conform to either A.3.5.6.3.2 or A.3.5.6.3.3, as applicable. The lead finish designator (see A.3.6.2.7) shall apply to the finish of the leads or terminals. The leads or terminals shall meet the applicable solderability and corrosion resistance requirements. The other external metallic package elements (including metallized ceramic elements) shall meet the applicable corrosion resistance requirements. Finishes on interior elements (e.g. bonding pads, posts, tabs) shall be such that they meet the lead bonding requirements and applicable design and construction requirements. The use of strike plates is permissible to the maximum thickness of 10 microinches (0.25 micrometer). All plating of finishes and undercoats shall be deposited on clean, nonoxidized metal surfaces. Suitable deoxidation or cleaning operations shall be performed before or between plating processes. All parts shall be capable of meeting the following requirements of MIL-STD-883:

NOTE: Pure tin is prohibited on leads and cases as a final finish. Use of tin-lead finishes are acceptable provided they meet the lead content requirements herein.

a. Test method 2004, lead integrity, test condition B1, B2, or D, or test method 2028, pin-grid package destructive lead pull test, as applicable.

b. Test method 1009, salt atmosphere.

c. Test method 2003 or test method 2022, solderability (plus time/temperature exposure of burn-in except for devices which have been hot solder dipped or have undergone tin fusing after burn-in).

d. Test method 2025, adhesion of lead finish.

Compliance to the above requirements shall be demonstrated when and as specified.

A.3.5.6.3.1 Finish thickness measurements. Lead finish thickness measurements shall be taken at the seating plane on surface mount leads (such as J-bend and gull-wing type leads) and approximately halfway between the seating plane and the tip of the lead on all other lead types. (This requirement is to avoid having the inspector select a nontypical portion of the lead on which to perform the measurement.) On all lead shapes other than round, the finish thickness measurement shall be taken at the crest of major flats. Measurements taken on the shorting bar shall be correlated by direct measurement on the lead. Finish thickness measurements for package elements other than leads shall be taken at the center of major flats. Finish thickness measurements shall be performed in accordance with one of the following procedures:

a. ASTM B487.
b. ASTM B567.
c. ASTM B568.

The aforementioned ASTM methods are provided as reference methods to be used when the failure to pass other finish requirements suggests deficiencies in plating thickness. Compliance to the finish thickness requirements shall be demonstrated when and as specified.

A.3.5.6.3.2 Lead finish. The finish system on all external leads or terminals shall conform to one of the combinations listed in table A-II, and to the thickness and composition requirements of table A-III. The finish system shall also conform to the requirements of A.3.5.6.3.4 and A.3.5.6.3.5, where applicable.

A.3.5.6.3.3 Package element (other than lead or terminal) finish. External metallic package elements other than leads and terminals (e.g., lids, covers, bases, and seal rings) shall meet the applicable environmental requirements without additional finishing of the base materials or else they shall be finished so they meet those requirements using a finish system conforming to one of the combinations listed in table A-IV, and conforming to the thickness and composition requirements of table A-III. The finish system shall also conform to the requirements of A.3.5.6.3.4 and A.3.5.6.3.5, where applicable.

A.3.5.6.3.4 Hot solder dip. The hot solder dip shall be homogeneous and shall be applied as follows:

a. All outlines with hot solder dip over compliant coating. The hot solder dip shall extend beyond the effective seating plane. If the seating plane is not defined, the hot solder dip shall extend to within .040 inch (1.02 mm) of the lead/package interface. For leadless chip carrier devices, the hot solder dip shall cover a minimum of 95 percent of the metallized side castellation or notch and metallized areas above and below the notch, except the index feature if not connected to the castellation. Terminal area intended for device mounting shall be completely covered.

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b. All outlines with hot solder dip over base metal or noncompliant coating. The solder shall extend to the glass seal or point of emergence of the metallized contact or lead through the package wall. If solder is applied up to the seal, a hermeticity test (test method 1014, see MIL-STD-883, TM 5004, 12/) shall subsequently be performed and passed. For leadless chip carrier devices, the hot solder dip shall completely cover the metallized side castellation or notch and metallized areas above and below the notch, except the index feature if not connected to the castellation.

A.3.5.6.3.5 Tin-lead plate. Tin-lead plate may be fused after plating before or after burn-in by heating above its liquidus temperature. Tin-lead plate shall be visually inspected after fusing and shall exhibit a dense, homogeneous, and continuous coating. The visual inspection after fusing shall be conducted on a sample basis by the manufacturer as an in-process control. Visual inspection of the fusing shall be performed at a frequency sufficient to assure continuous compliance with these requirements on the finished product.

TABLE A-II. Lead finish systems.

Finish	Applied over	Required underplate		
	Gold plate	Electroplated Nickel	Electroless Nickel 1/	None
Hot solder dip 2/				X
Hot solder dip 2/		X		
Hot solder dip 2/			X	
Hot solder dip 2/	X	X		
Hot solder dip 2/	X		X	
Tin-lead plate 3/				X
Tin-lead plate 3/		X		
Tin-lead plate 3/			X	
Gold plate		X		
Gold plate			X	

1/ Electroless nickel shall not be used as the undercoat on flexible or semi-flexible leads (see 3.3.1 and 3.3.2 of test method 2004 of MIL-STD-883) and shall be permitted only on rigid leads or package elements other than leads.

2/ Hot solder dip shall be applied in accordance with A.3.5.6.3.4.

3/ Fusing of tin-lead plating is permitted in accordance with A.3.5.6.3.5.

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TABLE A-III. Coating thickness and composition requirements.

Coating	Thickness (microinch/micrometer)		Coating composition requirements
	Minimum 1/	Maximum 2/	
Hot solder dip (for all round leads) 3/	60/1.52	NS	The solder bath shall have a nominal composition of Sn60 or Sn63.
Hot solder dip (for all shapes other than round leads which have ≤ 25 mil pitch) 3/	150/3.80	NS	The solder bath shall have a nominal composition of Sn60 or Sn63.
Hot solder dip (for all shapes other than round leads with > 25 mil pitch) 3/	200/5.08	NS	The solder bath shall have a nominal composition of Sn60 or Sn63.
Tin-lead plate (as plated) 4/	300/7.62	NS	Shall consist of 2 to 50 percent by weight lead (balance nominally tin) homogeneously co-deposited. Shall contain no more than 0.05 percent by weight co-deposited organic material measured as elemental carbon. 5/
Tin-lead plate (fused) 4/	200/5.08	NS	
Gold plate	50/1.27	225/5.72	Shall contain a minimum of 99.7 percent gold. Only cobalt shall be used as the hardener.
Nickel plate (electroplate)	50/1.27	350/8.89	The introduction of organic addition agents to nickel bath is prohibited. Up to 40 percent by weight cobalt is permitted as a co-deposit.
Nickel plate (electroless)	50/1.27	250/6.35	The introduction of organic additive agents to nickel bath is prohibited.
Nickel cladding	50/1.27	350/8.89	

1/ Package elements having noncompliant coatings are permitted provided they are subsequently hot solder dipped in accordance with A.3.5.6.3.4b.

2/ NS = Not specified.

3/ See A.3.5.6.3.4.

4/ See A.3.5.6.3.5.

5/ The maximum carbon content (and minimum lead content in tin-lead plate) shall be determined by the manufacturer on at least a weekly basis. The determination of carbon and lead content may be made by any accepted analytical technique (e.g., for carbon: pyrolysis, infrared detection (using an IR212, IR244 infrared detector, or equivalent); for lead: X-ray fluorescence, emission spectroscopy) so long as the assay reflects the actual content in the deposited finish.

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TABLE A-IV. Package element (other than leads/terminals) finish systems.

Finish	Applied over	Required underplate			
	Gold plate	Electroplated nickel 1/	Electroless nickel 1/	Nickel cladding 1/	None
Hot solder dip					X
Hot solder dip		X			
Hot solder dip			X		
Hot solder dip				X	
Hot solder dip	X	X			
Hot solder dip	X		X		
Hot solder dip	X			X	
Tin-lead plate 2/					X
Tin-lead plate 2/		X			
Tin-lead plate 2/			X		
Tin-lead plate 2/				X	
Gold plate 3/		X			
Gold plate 3/			X		
Gold plate 3/				X	
Electroplated nickel 1/					X
Electroless nickel 1/					X
Nickel cladding 1/					X

1/ Combinations of electroplated nickel and electroless nickel and nickel cladding are permitted.

2/ Fusing of tin-lead plate is permitted in accordance with A.3.5.6.3.5.

3/ Multilayer gold and nickel finish structures are acceptable provided the outer gold layer meets a minimum thickness of 25 microinches (0.635 micrometer), the total of the gold layers meet a minimum thickness of 50 microinches (1.27 micrometers), and each of the nickel undercoats meet the thickness requirements of table A-III with the total nickel thickness not to exceed 450 microinches (11.43 micrometers). For multilayer finish structures, nickel plate, nickel cladding, or gold plate are permitted on the base metal.

A.3.5.7 Die plating and mounting. Pure glass shall not be used for microcircuit die mounting. Metal glass die mounting and Silver
* Cyanate Ester (see Rome Labs letter 31 May 94 for Guidelines) are acceptable with qualifying activity approval. Electroplated and electroless plated gold backing on dice shall not be used, with the exception of GaAs dice which may use electroplated gold backing.

A.3.5.8 Glassivation. All microcircuits shall be coated with a transparent glass or other approved coating, except where glassivation is omitted by documented design rules (e.g., probe opening, fuse pads, etc.) The minimum glassivation thickness shall be 6000 Å (600 nm) for $Si0_2$, 2,000 Å (200 nm) for Si_3N_4, or approved thicknesses for approved coatings. The composition and minimum thickness of other approved coatings are subject to approval by the qualifying activity. The glassivation/nitridation shall cover all electrical conductors except the bonding or test pads. NOTE: For GaAs microwave microcircuits, the glassivation or nitride dielectric shall cover the semiconductor regions (e.g., FET) of the device and planar thin film resistors as a minimum. Furthermore; for class S devices, the glassivation or nitride dielectric shall cover regions where conductors are separated by less than the minimum particle size detectable by a PIND test. For RF/microwave GaAs microcircuits, the manufacturer shall define appropriate glassivation thickness requirements for the technology in the internal baseline documentation.

A.3.5.9 Die thickness. Appropriate die thickness requirements for each product or process shall be defined in the manufacturer's baseline documentation. This thickness shall be sufficient to avoid die cracks due to handling, die attach, wire bonding or other process stresses, which could lead to latent field failure.

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A.3.5.10 Laser scribing. For class level S microcircuits, laser scribing shall not be used for die separation except for backside scribing of silicon on sapphire (S0S) wafers. Laser trim of resistors and shorting bars and laser scribed package external markings are not prohibited unless otherwise specified.

A.3.5.11 Internal lead separation for class level S devices. For class level S devices, the minimum separation of the internal leads (excluding conductors which are at the die or substrate potential) from the unglassivated surface of the die shall be a minimum of 1.0 mil. This design requirement shall be verified during qualification and during group B internal visual and mechanical test in accordance with MIL-STD-883, test method 5005.

A.3.6 Marking of microcircuits. Marking shall be in accordance with the requirements of this appendix, and the identification and marking provisions of the device specification or drawing. The marking shall be legible and complete, and shall meet the resistance to solvents requirements of MIL-STD-883, test method 2015. When laser marking is performed, it shall be clearly visible through those
* conformal coatings approved for use in MIL-I-46058, (see test method 2015 of MIL-STD-883 if contrasting material or ink is used to highlight the trace). Laser marked metal surfaces shall have been submitted to and passed all group D test requirements. If any special marking is used, it shall in no way interfere with the marking required herein, and shall be visibly separated therefrom. The following marking shall be placed on each microcircuit. If any special marking (e.g., altered item drawing number) is used by the device supplier or user/equipment contractor, it shall be in addition to the existing/original marking as required herein and shall be visibly separate from and in no way interfere with the marking required herein. The following shall be placed on each microcircuit:

a. Index point (see A.3.6.1).
b. PIN (see A.3.6.2).
c. Identification codes (see A.3.6.3).
d. Manufacturer's identification (see A.3.6.4 and A.3.6.5).
e. Country of origin (see A.3.6.6).
f. Compliance indicators (see A.3.6.7)
g. Serialization, when applicable (see A.3.6.8).
h. Special marking (see A.3.6.9, A.3.6.9.1).
i. Electrostatic discharge sensitivity identifier, if applicable (see A.3.6.9.2).

NOTE: All devices shall be marked by the manufacturer in such a manner as to leave space for additional unique marking (assigned and applied by the user or called out in the purchase order or contract).

A.3.6.1 Index point. The index point, tab, or other marking indicating the starting point for numbering of leads or for mechanical orientation shall be as specified (see MIL-STD-1835) and shall be designed so that it is visible from above when the microcircuit is installed in its normal mounting configuration. The outline or solid equilateral triangle(s) (Δ) which may be used as an electrostatic identifier (see A.3.6.9.2), may also be used as the pin 1 identifier.

A.3.6.2 PIN. Each microcircuit shall be marked with the complete PIN. The PIN may be marked on more than one line provided the PIN is continuous except where it "breaks" from one line to another. The PIN system shall be as described in 3.6.2 a and b for microcircuits produced in accordance with this appendix and either an SMD, or device specification. For devices produced in accordance with this appendix which are not documented on SMDs or M38510 slash sheets, the PIN shall be the vendors generic part number or the contractors part number as applicable.

* A.3.6.2.1 Military designator. Any device which does not meet all the requirements of this appendix and the applicable device specification except as allowed by H.3.3 shall not be marked M38510 and shall not make reference to MIL-M-38510 or MIL-PRF-38535.

A.3.6.2.2 RHA designator. A "/" or "-" indicates no radiation hardness assurance. Letters M, D, L, R, F, G, or H designator levels are defined in A.3.4.1.3.

A.3.6.2.3 Device specification. When used in association with this document or appendix (i.e., QML), the M38510 device specification shall consist of three digits from 001 to 999 as applicable.

A.3.6.2.4 Device type. The device type number shall be as specified in the device specification or SMD. The numbers shall consist of two digits assigned sequentially, from 01 to 99 within each device specification or SMD.

A.3.6.2.5 Device class. The device class shall be designated by a single letter identifying the quality assurance level. For devices built compliant to this appendix and documented on a one part-one part number SMD, the device class designator shall be an 'M'.

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A.3.6.2.6 Case outline. The case outline shall be designated by a single letter assigned to each outline.

A.3.6.2.7 Lead finish. Lead frame or terminal material and finish shall be as specified in A.3.5.6. The lead finish shall be designated by a single letter as follows:

Finish letter	Lead frame or terminal material and finish (see note below)
A	Types A, B, C, D, E, F, G, or H with hot solder dip
B	Types A, B, C, D, E, F, G, or H with tin-lead plate
C	Types A, B, C, D, E, F, G, or H with gold plate
X	Types A, B, C, D, E, F, G, or H with finishes A, B, or C (see note below)

NOTE: Finish letter "X" shall not be marked on the microcircuit or its packaging. This designation is provided for use in drawings, part lists, purchase orders, or other documentation where lead finishes A, B, or C are all considered acceptable and interchangeable without preference. For Government logistic support, the A lead finish will be acquired and supplied to the end user when the X is included in the PIN for lead finish. If the PIN is not available with the A lead finish, the same PIN will be acquired except with the B or C lead finish designator as determined by availability. Type C terminal material is a fired on metallization used with leadless chip carriers.

* A.3.6.2.8 Drawing designator. For new one part-one part number drawings without existing device specifications the first two characters of the drawing designator will consist of the last two digits of the year and the last three characters will consist of unique characters assigned to the drawing by DSCC. When an existing MIL-M-38510 device specification PIN is converted to a one part-one part number PIN via a substitution statement, the first two characters of the drawing designator of the one part-one part number will be replaced with the first two digits of MIL-M-38510 (i.e., 38), and the last three characters of the one part-one part number will be replaced with the three digit identifier assigned to the device specification (e.g., M38510/00101BAC will become 5962-3800101BAC).

A.3.6.3 Identification codes. Identification codes shall be as follows.

A.3.6.3.1 Class level B die fabrication date code. Class level B microcircuits may be marked with a unique code to identify the year and quarter in which the die fabrication was started (or completed at the manufacturer's predesignated option). The first character of the code shall be the last digit of the year in which die fabrication started (or completed at the manufacturer's predesignated option). The second character of the code shall be a letter (A, B, C, or D) respectively designating the first quarter (weeks 1 - 13), the second quarter (weeks 14 - 26), third quarter (weeks 27 - 39), or fourth quarter (weeks 40 - 52 or 53) of the calendar year of die fabrication.

A.3.6.3.2 Inspection lot identification code for class levels S and B. Microcircuits shall be marked with a unique code to identify the inspection lot (see A.3.1.3.7 and A.3.1.3.8) and identify the first or the last week of the period (6 weeks maximum) during which devices in that inspection lot were sealed. At the option of the manufacturer, the actual week of seal may be used. The first two numbers in the code shall be the last two digits of the number of the year, and the third and fourth numbers shall be two digits indicating the calendar week of the year. When the number of the week is a single digit, it shall be preceded by a zero. Reading from left to right or from top to bottom, the code number shall designate the year and week, in that order. When two or more different inspection lots (or class level S sublots), each having the same part number, are to be marked with the same identification code, a unique suffix letter representing each additional inspection lot (or class level S sublot) shall appear immediately following the identification code except the unique suffix letter may be omitted when an alternate lot identifier is used which maintains the unique traceability required. Once assigned, the inspection lot identification code shall not be changed.

NOTE: These die fabrication date codes may be combined with the inspection lot identification code as shown:

FAB YR	FAB QTR	ASSY YR	ASSY WK	Unique suffix
6	B	87	10	A
1986	2nd qtr	1987	10	First lot

A.3.6.4 Manufacturer's identification. Microcircuits shall be marked with the name or trademark of the manufacturer. The identification of the equipment manufacturer may appear on the microcircuit only if the equipment manufacturer is also the microcircuit manufacturer.

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A.3.6.5 Manufacturer's designating symbol. The microcircuit manufacturer's designating symbol or CAGE code may also be marked on each device in addition to the manufacturer's identification. If the microcircuit manufacturer's designating symbol or CAGE code number is marked, it shall be as listed on NAVSHIPS 0967-190-4010 or cataloging Handbook H4/H8. The designating symbol shall be used only by the manufacturer to whom it has been assigned and only on those devices manufactured at that manufacturer's plant. In the case of small microcircuits, the manufacturer's designating symbol may be abbreviated by omitting the first "C" in the series of letters.

A.3.6.6 Country of origin. The identifier of the country in which assembly is performed shall be marked on all devices supplied under this appendix. If abbreviations are used, a cross reference should be published in the manufacturers data books or catalogs.

A.3.6.7 Compliance indicator/certification mark. The compliance indicator "C" shall be marked on all non-JAN devices built in compliance to this appendix. The compliance indicator "C" shall be replaced with a "Q" or "QML" certification mark or the "Q" or "QML" certification mark added when product is built to a QML process (see A.3.2.1). The "J" or "JAN" certification mark may not be used on devices built in compliance to this appendix, except as permitted by paragraph 3.6.3. The device manufacturer alone has the authority to apply or remove the JAN brand.

A.3.6.8 Serialization. Prior to the first recorded electrical measurement in screening each class level S microcircuit and, when specified, each class level B microcircuit shall be marked with a unique serial number assigned consecutively within the inspection lot. This serial number allows traceability of test results down to the level of the individual microcircuit within that inspection lot. For class level S, inspection lot records shall be maintained to provide traceability from the serial number to the specific wafer lot from which the devices originated.

A.3.6.9 Marking location and sequence. The certification mark, the PIN, identification codes and ESDS identifier shall be located on the top surface of leadless or leaded chip carriers, pin grid array packages, flat packages, or dual-in-line configurations and on either the top or the side of cylindrical packages (TO configurations and similar configurations). When the size of a package is insufficient to allow marking of special process identifiers on the top surface, the backside of the package may be used for these markings except the ESDS identifier, if marked, shall be marked on the top. Button cap flat packs with less than or equal to 16 leads may have the identifier marked on the ceramic. Backside marking with conductive or resistive ink shall be prohibited.

A.3.6.9.1 Beryllium oxide package identifier. If a microcircuit package contains beryllium oxide (see A.3.5.1 note), the part shall be marked with the designation "Be0".

* A.3.6.9.2 Electrostatic discharge sensitivity identifier. Microcircuits shall be ESDS classified in accordance with A.3.4.1.4, however, ESD classification marking is not required. The manufacturer will have an option of no ESD marking, marking a single ESD triangle or marking in accordance with the ESD device classification (i.e., class 1 - one Δ; class 2 - two Δ's; class 3 - no marking). Because it may no longer be possible to determine the ESD classification from the part marking, the device Discharge Sensitivity Classification, as defined in test method 3015 of MIL-STD-883, will have to be obtained through MIL-HDBK-103 or QML-38535.

A.3.6.10 Marking on container. See A.5.1.2 for additional marking requirements.

A.3.6.11 Marking option for controlled storage of class level B. Where microcircuits are subjected to testing and screening in accordance with some portion of the quality assurance requirements and stored in controlled storage areas pending receipt of orders requiring conformance to the same or a different level, the inspection lot identification code shall be placed on the microcircuit package along with the other markings specified in 3.6 sufficient to assure identification of the material. As an alternative, if the microcircuits are stored together with sufficient data to assure traceability to processing and inspection records, all markings may be applied after completion of all inspections to the specified level.

A.3.6.12 Marking option for qualification or quality conformance inspection. The manufacturer has the option of marking the entire lot or only the sample devices to be submitted to qualification or groups B, C, and D (and E if applicable) quality conformance inspection, as applicable. If the manufacturer exercises the option to mark only the sample devices, the procedures shall be as follows:

a. The sample devices shall be marked prior to performance of groups B, C, and D (and E if applicable) qualification or quality conformance inspections, as applicable.

b. At the completion of inspection, the marking of the sample devices shall be inspected for conformance with the requirements of A.3.6.

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c. The inspection lot represented by the conforming qualification or quality conformance sample shall then be marked and any specified visual and mechanical inspection performed.

d. The marking materials and processing applied to the inspection lot shall be to the same specifications as those used for the inspection sample.

A.3.6.13 Remarking. If sealed devices are remarked (to change or correct the marking as specified in A.3.6), the reason for remarking and a description of the process shall be recorded in the qualification test report and quality conformance test record. In addition to the tests described below for qualification of the remarking procedure, subgroup B-2 and internal visual and mechanical tests (test method 2014 with sample size/(accept no.) of 1(0) for class B devices and subgroups B-2a and B-2b (test method 2014 only) for class level S devices shall be performed on each remarked lot to assure marking permanency and that markings and device type coincide. An appropriate Group A test, with a sample size/(accept no.) of 116(0), (100 percent for class level S) may be performed, in lieu of internal visual and mechanical tests, to demonstrate that the markings and device types coincide. Remarking procedures shall be approved by the qualifying activity. Approval shall be required once only for each package material (i.e., lid, base) composition (regardless of package configuration), or at change of remarking procedures or materials. For qualification of the remarking procedure, a sample of remarked devices shall be tested to the following test methods according to test method 5005 of MIL-STD-883:

a. Test method 2015, resistance to solvents (3 devices).

b. Test method 1011, thermal shock (test condition B, 15 cycles minimum).

c. Test method 1004, moisture resistance.

d. Test method 1009, salt atmosphere.

NOTE: Electrical tests are not required. Visual inspection, after each test in accordance with applicable failure criteria, shall be conducted.

A.3.7 Workmanship. Microcircuits shall be manufactured, processed, and tested in a careful and workmanlike manner in accordance with good engineering practice, with the requirements of this appendix, and with the production practices, workmanship instructions, inspection and test procedures, and training aids prepared by the manufacturer in fulfillment of the quality assurance program (see A.4.8 herein).

A.3.7.1 Rework provisions. All rework (see A.3.1.3.16) permitted on microcircuits acquired under this appendix shall be accomplished in accordance with procedures and safeguards documented in accordance with A.4.8.1.1.6 and available for review by the preparing and acquiring activity. In addition, all rework operations shall be clearly identified on each process flowchart. Allowable rework of sealed packages includes recleaning of any microcircuit or portion thereof, any rebranding (see A.3.6.13) to correct defective marking and lead straightening (provided the reworked devices meet the requirements of A.4.6.2 for conditions of leads). For monolithic wafers of any class, the strip and redeposition of a layer or additional processing to correct a nonconformance to a specification limit is not allowed, except for the strip and redeposition of sacrificial layer(s) used exclusively as a masking function (e.g.,photoresist, nitride, nitride glass). Documenting rework of these sacrificial layers on the flow chart is not required. In the event of equipment failure beyond manufacturer control, continuation of processing is permitted and is considered allowable rework provided the manufacturer assures, through evaluation, that no alteration in material film properties occurs (e.g. oxidation, corrosion, grain size, film stress, adhesion) and baselined limits are met. The strip and redeposition of backside metalization is considered allowable rework. No delidding or package opening for rework shall be permitted for microcircuits of any class. For monolithic microcircuit wafers of any class, the strip and redeposition of a layer or additional processing to correct a nonconformance to a specification limit is not allowed, except as specified above. For class level S any assembly rework operation prior to package seal is not allowed, except as specified in A.3.7.1.1.

A.3.7.1.1 Rebonding of monolithic devices. Visual criteria for rebonding and rebonding limitations for class level S and class level B monolithic microcircuits shall be in accordance with test method 2010, Internal Visual (Monolithic), of MIL-STD-883, (see 3.2.1.4i and 3.2.1.5 of MIL-STD-883, test method 2010). For class level S devices the manufacturer's rebonding operation and rebonding procedure shall be documented in accordance with A.4.8.1.1.6, and will be reviewed during audits. Rebonding shall be limited to the bonding operation only.

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* A.4 VERIFICATION (QUALITY AND RELIABILITY ASSURANCE PROVISIONS)

A.4.1 Responsibility for inspection. Unless otherwise specified in the contract or purchase order, the contractor is responsible for the performance of all inspection requirements as specified herein and in the device specification or drawing.

A.4.1.1 Inspection during manufacture. The manufacturer shall establish and maintain in-process production controls, quality controls and inspections at appropriately located points in the manufacturing process in accordance with the procedures described in A.4.8.1.1 to assure continuous control of quality of materials, subunits, and parts during manufacture and testing. These controls and inspections shall be adequate to assure compliance with the applicable acquisition documentation and quality standards of microcircuits manufactured to this appendix and the applicable device specification or drawing.

A.4.1.1.1 Metal package isolation test for class level S devices. Prior to die mount, each metal-bodied package with leads glass-isolated within .005 inch (0.13 mm) of the metal body shall have 600 V dc applied between the case and leads not connected to the case. Packages which exhibit leakage greater than 100 nA shall be rejected.

A.4.1.2 Control and inspection of acquisition sources. The manufacturer shall be responsible for assuring that all supplies and services used in the manufacture and test of microcircuits conform to all the requirements of this appendix, the device specification or drawing, and other provisions of the applicable acquisition documentation.

A.4.1.3 Control and inspection records. The manufacturer shall maintain objective evidence documenting that each lot has been subjected to all processing controls, inspections, and tests accomplished in accordance with sections A.3 and A.4 herein. Records shall be retained as specified in A.4.8.1.2.

A.4.1.4 Government source inspection. Source inspection (GSI and CSI) shall be required only when specified in the purchase order or subcontract. Notification of test initiation shall be given to the acquiring activity.

A.4.1.5 Manufacturer control over its distributors. The manufacturer shall be responsible for assuring that its distributors maintain adequate controls to assure that products sold are of the same quality as products acquired directly from the manufacturer.

A.4.1.6 Distributor inventory, traceability and handling control. Distributors shall, as a minimum, maintain adequate inventory control system, traceability documentation required by this specification and their appropriate certification, adequate handling, storage, and repackaging methods to protect quality and prevent damage and degradation of products.

A.4.2 Solderability. All parts shall be capable of passing the solderability tests in accordance with MIL-STD-883, test method 2003, on delivery.

A.4.3 General inspection conditions. The general requirements of MIL-STD-883 shall apply.

A.4.3.1 Classification of inspections and tests. The inspections and tests required to assure conformance to the specified quality assurance levels of microcircuits or lots thereof are classified as follows:

Requirement	Paragraph
Qualification procedures	A.4.4
Quality conformance inspection	A.4.5
Screening	A.4.6
Data recording	A.4.7
Quality Assurance Program	A.4.8

A.4.3.2 Sampling. Statistical sampling for qualification and quality conformance inspections shall be in accordance with the sampling procedures of appendix D of this specification, and as specified in the device specification or drawing, as applicable. Reserve sample devices may be tested with the subgroups to provide replacements in the case of test equipment failure or operator error (see A.4.3.5, A.4.4.2.1.1, A.4.4.2.1.3). These devices shall be used in predesignated order. Initial samples (and added samples, when applicable) shall be randomly selected from the inspection lot or sublot, as applicable. After a test has started, the manufacturer may add an additional quantity to the initial sample, but this may be done only once for any subgroup with a specified sample size number (accept number). Add-on samples are not allowed for fixed sample size subgroups nor for resubmitted lots. The added samples shall be subjected to all the tests within the subgroup. The total samples (initial and added samples) shall determine the new acceptance number. The total defectives of the initial and second sample shall be additive and shall comply with the specified sample size number(accept number). The manufacturer shall retain sufficient microcircuits from the lot to provide for additional samples.

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* A.4.3.2.1 Disposal of samples. Devices subjected to destructive tests or which fail any test shall not be shipped on the contract or purchase order as acceptable product. They may, however, be delivered at the request of the acquiring activity if they are isolated from, and clearly identified so as to prevent their being mistaken for acceptable product. Sample microcircuits, from lots which have passed quality assurance inspections or tests and which have been subjected to mechanical or environmental tests specified in groups B, C, and D inspection and not classified as destructive, may be shipped on the contract or purchase order provided the test has been proved to be nondestructive (see A.4.3.2.3) and each of the microcircuits subsequently passes final electrical tests in accordance with the applicable device specification.

* A.4.3.2.2 Destructive tests. The following MIL-STD-883, or other test as specified, shall be classified as destructive:

Internal visual and mechanical (method 2014).
Bond strength.
Solderability (for lead finishes B and C).
Moisture resistance.
Lead integrity.
Salt atmosphere.
SEM inspection for metallization.
Steady-state life test (accelerated).
Die shear strength test.
Total dose radiation hardness test.
Neutron irradiation.
Electrostatic discharge sensitivity classification test.
Lid torque test.
Adhesion of lead finish.
Vibration, variable frequency.
Internal water vapor test.
Single-event-effects (ASTM F-1192 or EIA /JESD 57)
Dose-Rate Upset

All other mechanical or environmental tests (other than those listed in A.4.3.2.3), shall be considered destructive initially, but may subsequently be considered nondestructive upon accumulation of sufficient data to indicate that the test is nondestructive. The accumulation of data from five repetitions of the specified test on the same sample of product, without evidence of cumulative degradation or failure to pass the specified test requirements in any microcircuit in the sample, is considered sufficient evidence that the test is nondestructive. Any test specified as a 100 percent screen shall be considered nondestructive for the stress level and duration or number of cycles applied as a screen.

A.4.3.2.3 Nondestructive tests. The following tests are classified as nondestructive:

Barometric pressure
** Steady state life
** Intermittent life
*** Solderability (for lead finish A only)
Seal
External visual
Internal visual (pre-cap)
** Burn-in screen
Radiography
Particle impact noise detection
Physical dimensions
Nondestructive 100 percent bond pull test where stress does not exceed the specified pull force and positive tolerance
Resistance to solvents

** When the test temperature exceeds the maximum specified junction temperature for the device (including maximum specified for operation or test), these tests may be considered destructive. To ship these tested devices, the manufacturer must have data to support that the test is not destructive and has not degraded the device.

*** For glass sealed devices, lead finish A shall be considered nondestructive unless electrical test, visual inspection, or other evaluation shows that package integrity or electrical performance has been degraded.

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A.4.3.3 Formation of lots. Microcircuits shall be segregated into identifiable production lots as defined in A.3.1.3.6 as required to meet the production control and inspection requirements of A.4.8. Microcircuits shall be formed into inspection lots as defined in A.3.1.3.7 and A.3.1.3.8 as required to meet the quality assurance inspection and test requirements of this specification.

Wafer lot processing as a homogeneous group (see A.3.1.3.11) shall be accomplished by any of the following procedures, providing process schedules and controls are sufficiently maintained to assure identical processing in accordance with process instructions of all wafers in the lot:

a. Batch processing of all wafers in the wafer lot through the same machine process step(s) simultaneously.

b. Continuous or sequential processing (wafer by wafer or batch portions of wafer lot) of all wafers through the same machine or process step(s).

c. Parallel processing of portions of the wafer lot through multiple machines or process stations on the same certified line, provided statistical quality control assures and demonstrates correlation between stations and separately processed portions of the wafer lot.

A.4.3.3.1 Resubmission of failed lots. Resubmitted lots shall be kept separate from new lots and shall be clearly identified as resubmitted lots. When any lot submitted for qualification or quality conformance inspection fails any subgroup requirement of group B, C, or D tests, it may be resubmitted once for that particular subgroup using tightened inspection criteria (as defined in D.4.2). Resubmission for group A inspection failure is not permitted. In case of group B, subgroup B-2a failure, the entire lot may be remarked as defined in A.3.6.13. The remarked lot shall not be acceptable for alternate group B (class level B only) coverage of a standard lot (see A.4.5.8.2 for recovery). For fixed sample size subgroups, lots may be resubmitted one time only at double the sample size with zero failures allowed. All submissions shall be subject to the sampling requirements of A.4.3.2. A second resubmission (class level S lots shall be resubmitted one time only) using a second tightened inspection criteria is permitted only if failure analysis is performed to determine the mechanism of failure for each failed microcircuit from the prior submissions and it is determined that failure(s) is (are) due to:

a. A defect that can be effectively removed by rescreening or reworking the entire lot (see A.3.7.1).

b. Random type defects which do not reflect poor basic device design or poor basic processing procedures.

In all instances where analysis of the failed devices indicates that the failure mechanism is due to poor basic processing procedures, a basic design fault or nonscreenable defects, the lot shall not be resubmitted.

A.4.3.4 Test method deviation. Deviations from test methods or test circuits specified are allowed provided that it is demonstrated to the preparing activity that such deviations in no way relax the requirements of this appendix and that they are approved by the preparing activity before testing is performed. The preparing activity shall be notified by the device manufacturer of any proposed test method deviation. For proposed electrical test deviations, schematic wiring diagrams of the test equipment shall be made available for review.

A.4.3.5 Procedure in case of test equipment failure or operator error. Whenever a microcircuit is believed to have failed as a result of faulty test equipment or operator error, unless otherwise specified in the test method, the failure shall be entered in the test record which shall be retained for review along with a complete explanation verifying why the failure is believed to be invalid. For JAN product, when lot jeopardy is involved and failure occurs during the processing of microcircuits with Government Source Inspection (GSI) required, the Government Quality Assurance Representative (QAR) shall be notified within 1 working day and given details from the test record and the opportunity to challenge the validity of the error claimed. If no challenge is made within the next working day, the error will be considered valid as recorded.

NOTE: ESD failures shall be counted as rejects and not be attributed to equipment/operator error for screening, group A, and end-point electrical tests of test method 5005 of MIL-STD-883.

A.4.3.5.1 Procedure for sample tests. When it has been established that a failure is due to test equipment failure or operator error and it has been established that the product has not been damaged or degraded, a replacement microcircuit from the same inspection lot may be added to the sample. The replacement microcircuit shall be subjected to all those tests to which the discarded microcircuit was subjected prior to its failure and to any remaining specified tests to which the discarded microcircuit was not subjected prior to its failure. The manufacturer, at his own risk, has the option of replacing the failed microcircuit and continuing with the tests before the validity of the test equipment failure or operator error has been established.

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A.4.3.5.2 Procedure for screening tests. When it has been established that lot failure(s) during screening test(s) are due to operator or equipment error and it has been established that the remaining product has not been damaged or degraded, the lot or surviving portion of the lot, as the case may be, may be resubmitted to the corrected screening tests(s) in which the error occurred. Failures verified as having been caused by test equipment failure or operator error shall not be counted in the PDA calculation (when applicable).

A.4.3.5.3 Failure and corrective action reports. When the procedures of A.4.3.5.1 and A.4.3.5.2 are utilized in continuing sample tests or resubmitting lots for screening tests, the manufacturer shall document the results of his failure investigations and corrective actions and shall make this information available to the Government QAR, the acquiring activity, or the qualifying activity, as applicable.

A.4.3.6 Electrical test equipment verification. The manufacturer shall verify the measurement/operation characteristics of the electrical test equipment in accordance with 4.5 of MIL-STD-883.

A.4.3.7 Manufacturer imposed tests. Any manufacturer imposed test(s) (i.e., gross and fine leak) which exceed the minimum class level B requirements herein shall be documented on the manufacturers process baseline. If any manufacturer imposed tests detects a problem, the manufacturer shall submit all devices in the lot to those tests to eliminate rejects and shall take steps to determine and eliminate the cause of failure (e.g., rough handling which has produced gross leaks).

A.4.4 Qualification procedures.

A.4.4.1 General. The manufacturer shall perform sufficient qualification inspection to assure that the devices supplied to this appendix meet the minimum class level B or S performance requirements as defined herein. Qualification to a given quality assurance level qualifies the product for all lower quality assurance levels provided the product for all levels is manufactured on the same line and meets all the requirements of the lower level.

A.4.4.2 Qualification. A manufacturer should qualify individual devices by subjecting them to, or assuring that, they satisfy all the groups A, B, C, and D (and E if applicable) requirements of test method 5005 or test method 5010 as applicable of MIL-STD-883 for the specified device class and type of microcircuits. Paragraphs A.4.4.2.1 through A.4.4.2.7 should be used as guidelines.

A.4.4.2.1 Inspection routine. Except where the use of electrical rejects is allowed, all microcircuits subjected to groups B, C, and D (and E if applicable) tests should have previously been subjected to and passed all tests of group A inspection specified as end-point electrical parameters. The microcircuits should then be divided into the subgroups for groups B, C, and D (and E if applicable) inspection. When necessary to meet subsequent sample requirements, all failures found in the course of group A inspection should be replaced by microcircuits which have passed group A tests prior to subjection to group B, C, or D (and E if applicable) tests. All tests should be applied to and all acceptance criteria referenced to the entire lot or sublot as applicable, not to an arbitrary quantity of devices tested.

A.4.4.2.1.1 Sample. The number of microcircuits to be tested should be chosen (independent of lot size) by the manufacturer and should be adequate to demonstrate conformance to the inspection criteria for each subgroup of groups A, B, C, and D (and E if applicable) inspection. All qualification test samples for subgroups which require variables data should be serialized prior to qualification tests.

A.4.4.2.2 Group A electrical testing. The parameters, conditions of test and limits for group A testing should be as specified in test method 5005 of MIL-STD-883 and the applicable device specification or drawing. Group A testing may be performed in any order. If an inspection lot is made up of a collection of splits or class level S inspection sublot, each split or class level S inspection sublot, should pass group A inspection as specified.

A.4.4.2.3 Group B testing. Group B tests should be as specified in test method 5005 of MIL-STD-883.

A.4.4.2.4 Groups C and D testing. Groups C and D tests should be as specified in test method 5005 of MIL-STD-883.

A.4.4.2.5 Group E testing. Group E tests should be conducted as specified in test method 5005 of MIL-STD-883. Group E is required for initial qualification and after process or design changes which may effect radiation hardness (see A.3.4.2). Qualification for RHA should be for a specific microcircuit die and package type, except as authorized by the qualifying activity. Microcircuits which pass the quality assurance and RHA requirements to a higher reliability or RHA level should be acceptable to a lower level or as non-RHA parts if all other applicable requirements and pre- and postirradiation electrical parametric and timing limits are met.

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A.4.4.2.6 Approval of other lead finishes. After qualification of one package type with a single lead finish, other lead finishes may be approved by submitting a single device type for each additional lead finish in the previously approved package family to group B, subgroup 3 and group D, subgroups 1, 3, 5, and 7 tests. Subgroup D-7 testing should not be required for hot solder dip over lead finishes B or C (tin-lead, gold plate) which have been qualified on the same package family.

A.4.4.2.7 Approval of other lead material. After the first lead material is qualified with a particular package family, the new lead material for the package family can be considered qualified provided the required lead finish tests specified (see A.4.4.2.6) with the addition of subgroup D-2, are successfully performed. Subgroup D-6 should be completed when the lead frame extends into the die cavity.

A.4.4.2.8 Electrostatic discharge sensitivity. Electrostatic discharge sensitivity classification testing shall be done in accordance with test method 3015 of MIL-STD-883, and the applicable device specification or drawing (see A.3.6.9.2). Devices shall be handled in accordance with the manufacturer's in-house control documentation. Handling documentation shall be maintained by the manufacturer. Guidance for device handling is available in EIA-STD-625.

A.4.5 Quality conformance inspection.

A.4.5.1 General. Quality conformance inspection shall be conducted in accordance with the applicable requirements of groups A, B, C, and D (and E if applicable) of test method 5005 or test method 5010 when applicable), MIL-STD-883, for the specified device class and test method 5007 of MIL-STD-883, when applicable. Inspection lot sampling shall be in accordance with appendix D of this specification. Test results shall be recorded by inspection lot identification code (see A.3.6.3) for each inspection lot.

A.4.5.2 Group A inspection. Group A inspection shall be performed on each inspection lot in accordance with MIL-STD-883 and shall consist of electrical parameter tests specified for the specified device class. If an inspection lot is made up of a collection of splits or class level S inspection sublots, it shall be recombined into an inspection lot before the group A inspection sample is taken or a group A inspection sample shall be taken from each split or class level S inspection sublot.

A.4.5.3 Group B inspection. Group B inspection shall be performed in accordance with MIL-STD-883 on each inspection lot for each package type and lead finish. As an alternate, except for class level S (at the manufacturer's option) group B inspection may be performed on each package type and lead finish in accordance with 3.5.2 of test method 5005 or 3.4.2.1 of test method 5010 of MIL-STD-883. For class level S, group B, subgroups 1A, 2, 3, and 4 inspections shall be performed on each sublot (split) when the manufacturer elects to keep the sublots (splits) separate from each other after screen tests are completed. Except as otherwise specified in test method 5005 of MIL-STD-883, samples for this inspection shall be completed and fully marked devices from lots which have been subjected to and passed the post burn-in +25°C final electrical static tests (subgroup 1). Class level S steady-state life test, subgroup B-5, results shall not be used to support class level B shipments.

A.4.5.4 Group C inspection for class level B only. Group C inspection (die-related tests) shall be in accordance with MIL-STD-883 and shall include those tests specified which are performed periodically. Group C shall have been completed on product with a die fabrication date code within four calendar quarters prior to the die fabrication date code of product being submitted for acceptance. Group C tests are required for devices from each microcircuit group (see A.3.1.3.13) in which a manufacturer is supplying product. Group C tests for each microcircuit group shall be performed on one inspection lot of the most complex device type available at the time of selection from production devices produced on each certified die fabrication line once per calendar year.

A.4.5.4.1 Group C sample selection. Samples selected for group C inspection shall meet all of the following requirements:

a. Must be chosen at random from any inspection lot comprised only of die from the quarter of the year (see A.3.6.3.1) for which quality conformance inspection is being established in a particular microcircuit group (see A.3.1.3.13 and tables A-VI, A-VII, A-VIII, and A-IX) for each certified die fabrication line.

b. Must be chosen from an inspection lot that has been submitted to and passed group A quality conformance inspection (regardless of whether that inspection lot has been submitted and passed group B quality conformance inspection).

c. The inspection lot from which the samples are selected shall be the one with the most complex device type available at the time of selection.

d. On multichip microcircuits, the group C die fabrication date code requirement shall be determined by considering only the latest date code of the most complex die contained within the package.

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A.4.5.4.1.1 Microcircuit group assignments. Microcircuits group assignments and technologies/die family assignments shall be as specified in tables A-VI, A-VII, A-VIII A-IX and A.3.1.3.13. Microcircuit groups shall be structured such that they appropriately group all of the devices produced by the manufacturer, including those which do not coincide with any of the current microcircuit groups listed. In the tables, each number represents a different microcircuit group. Each letter in the top row of the table represents a different technology group. Each table entry in the line below the technologies (e.g., Standard TTL, Schottky TTL, CMOS, etc.) represent a separate die family (e.g., 93, 93H, LS, etc).

A.4.5.4.1.2 Product acceptable for delivery. Product shall be acceptable for delivery only after the successful completion of all group C testing and shall be comprised of die meeting the following requirements:

a. Manufactured on the same die fabrication line as the sample selected for A.4.5.4.1.

b. In the same microcircuit grouping as the sample selected in A.4.5.4.1.

c. Which was started (or completed, at the manufacturer's predesignated option) within the same year the sample selected in A.4.5.4.1.

d. Group C coverage is required for each year of material production on each microcircuit group.

NOTE: The above group C inspection and corresponding marking system shall be implemented on all devices with an inspection lot date code (seal week) of 8840 and later for JAN product and 8939 and later for non-JAN product. Inspection lots formed using die fabricated prior to 1988 for JAN product and prior to 1989 for non-JAN product shall be grandfathered according to the previous group C QCI requirements and marked with "GF" for the die fab symbolization (see A.3.6.3.1).

A.4.5.5 Group D inspection. Group D inspection (package related tests) shall be in accordance with test method 5005 of MIL-STD-883 and shall include those package or case-related tests which are performed periodically. Group D tests shall be performed every 26 calendar weeks on each package family for each assembly line (traceable to the inspection lot identification code of the week tested). If no production is performed for an extended period of time, coverage can be reestablished on the next available production run for the package family in need of coverage. Group D results can be used to support any class provided all of the Group D sampling criteria are met. Each additional lead finish for each package family shall be subjected to subgroups 3, 5, and 7 of group D. Subgroup D-7 testing is not required for hot solder dip over lead finishes B or C (tin-lead, gold plate) which have been periodically tested for quality conformance inspection on the same package family. For hot solder dipped leadless chip carriers, the B3 and L3 dimensions may be measured prior to solder dip. In addition, laser marked devices for each package family, which do not have group D coverage for laser marking, shall be subjected to subgroups 3 and 5 of group D.

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TABLE A-VI. Digital microcircuits.

Technology group	A				B	C			L	M
Technologies	Standard TTL	Schottky TTL	Low power TTL	DTL	ECL	CMOS	PNMOS	NMOS	Combination bipolar and CMOS	Integrated
Die family	93,93H, 54,54H	S,LS, F,ALS	93L, 54L			54HC54 A,4xxx			54BCT, 54ABT	Injection logic
Functions										
Gates	1	8	15	22	29	36	NA	NA	125	NA
Buffers	2	9	16	23	30	37	NA	NA	126	NA
Flip-Flops	3	10	17	24	31	38	NA	NA	127	NA
Combinational gates	4	11	18	25	32	39	NA	NA	128	NA
Sequential registers/ counters	5	12	19	26	33	40	45	48	129	97
RAM	6	13	20	27	34	41	43	46	130	98
ROM/PROM/PLA	7	14	21	28	35	42	44	47	131	99
Microprocessors interface peripherals FIFO	100	101	102	103	104	105	106	107	132	108

NA - None assigned; to be assigned at a later date as necessary.

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TABLE A-VII. Linear microcircuits. 1/

Technology group	D	E	F	G
Technologies	Bipolar	J-FET	CMOS	Combinational
Functions				
Operational amplifiers	49	61	73	85
Comparators	50	62	74	86
Sense Amplifiers	51	63	75	87
Regulators	52	64	76	88
Line drivers/receivers	53	65	77	89
Timers	54	66	78	90
Core drivers	55	67	79	91
D/A converters	56	68	80	92
A/D converters	57	69	81	93
Analog switches/ multiplexers	58	70	82	94
Voltage reference	59	71	83	95
Sample and hold	60	72	84	96
Active filters	109	112	115	118
Telecommunications	110	113	116	119
Electro-optics	111	114	117	120

1/ Die families are defined as microcircuit groups shown.

TABLE A-VIII. Other microcircuits.

Technology group	Function
H	Multichip

TABLE A-IX. Application specific microcircuits. 1/

Technology group	K	
Technologies	Bipolar	CMOS
Function		
Gate array	121	123
Linear array	122	124

1/ Die families are defined as microcircuit groups shown.

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A.4.5.5.1 Group D sample selection. Sample selection for group D shall be as follows:

a. The package types selected for Group D inspection shall be either rotated among the package types available at the time of sample selection from the allotted package family or worst case available from the allotted package family. Worst case shall be determined by the manufacturer based on an incoming vendor material control program (see A.4.5.5.2). For glass-sealed packages (e.g., cerdips, cerpaks), worst case is based on the minimum seal area and the maximum cavity size (in most cases this will be two packages). Under the rotation option, if a package type has not been tested for 3 years, then the next assembled lot of that package type shall receive group D inspection. If the manufacturer has a single package, which cannot be grouped into a package family, the manufacturer has the option to perform the group D testing once per calendar year on that package.

b. The product accepted for delivery shall be the inspection lot identification codes of the 36 successive weeks, except as allowed in item a, beginning with the inspection lot identification code of the successful group D sample for the package family.

c. Different device types may be used for different subgroups. Testing of a subgroup using a single device type enclosed in the intended package type shall be considered as complying with the requirements for that subgroup for all the device specifications or drawings utilizing the qualified package family and lead finish.

d. Technical justification must be given for device selections for subgroups D-3 and D-4 in regards to device technology electrical performance and package interaction. If a package and technology interaction is present, subgroup D-3 and D-4 shall be performed on the affected combination separately or used as coverage for the whole package family. Rotation of device technology is allowed to address this requirement. For nonconformance see A.4.5.8.

A.4.5.5.2 Incoming vendor material control program. The manufacturer who utilizes the worst case group D option shall have in place an incoming vendor material control program for the piece parts used in packaging (e.g., vendor SPC program). The methods and procedures used to control inspection, storage, and handling of incoming materials shall be documented.

A.4.5.6 Group E inspection. Group E inspection shall be in accordance with test method 5005 of MIL-STD-883 and, at the contractors option, is allowed anytime following completion of wafer fabrication. A device type which fails group E inspection may not be certified as an RHA microcircuit at the failed or higher level, but may be used as a non-RHA microcircuit or certified at another (lower) level if the microcircuit meets the lower level requirements and all other applicable requirements including pre- and postirradiation electrical and timing parametric limits.

A.4.5.6.1 Group E sample selection. Sample selection shall be in accordance with test method 5005 of MIL-STD-883 and shall be from each wafer prior to assembly or from each inspection or wafer lot. QCI requirements for class level B wafer lots shall be satisfied if all wafers used in that lot have been tested individually in accordance with class level S requirements. For traceability, see A.3.4.6.

A.4.5.7 End-point tests for groups B, C, and D (and E if applicable) inspections. End-point measurements and other specified post-test measurements shall be made for each microcircuit of the sample after completion of all other specified tests in the subgroup. The test limits for the end-point measurements shall be the same as the test limits for the respective group A subgroup inspections. Different end-points may be specified for group E tests in the device specification or drawing. Any additional end-point electrical measurements which may be performed at the discretion of the manufacturer, shall be accomplished in accordance with A.3.4.3 (i.e., tests performed on sample devices subjected to groups B, C, and D (and E if applicable) tests shall be performed as a 100-percent screen on all production devices represented by the sample).

A.4.5.8 Nonconformance. Lots which fail subgroup requirements of groups A, B, C, and D (and E if applicable) may be resubmitted in accordance with the provisions of A.4.3.3.1. A failed lot which is reworked (see A.3.7.1) or is rescreened (resubmittal to inadvertently missed process steps is not considered a rescreen) may not be resubmitted to the failed subgroups (and must be counted as a failure) for periodic group B, C, or D (or E if applicable) quality conformance inspection coverage. The lot may be resubmitted only to the failed subgroup to determine its own acceptance. If a lot is not resubmitted or fails the resubmission, the lot shall not be shipped and all references to MIL-PRF-38535, or this appendix shall be removed. For RHA microcircuits where group E tests are performed, and a sample plan of 18(1) and 38(1) is utilized for two successive lots of the same device type or for more than 10 percent of the lots during the preceding 18 months, data as specified herein
shall be provided. Resubmission for RHA qualification inspection, in this case, may be required. Lots that are not resubmitted, fail the resubmission, are withdrawn from compliance consideration, reworked, or rescreened (excluding resubmittal to final electricals when test conditions or limits are not changed) due to the failure of a PDA or QCI requirement of this appendix must be recorded and properly dispositioned. The reporting of these lots shall include the following, as applicable:

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a. PIN.
b. Inspection lot identification code.
c. Quantity of lot.
d. Point of scrap in manufacturer's flow.
e. Test results and date of failure (including all rescreening, reworks, and resubmissions).
f. Reason for failure or scrapping including applicable test results.
g. Date of scrapping or withdrawal from military consideration.
h. Disposition action of affected lots.

NOTE: The Government reserves the right to request and receive information concerning implementation of corrective actions and justification for rework and rescreening.

A.4.5.8.1 Group B failure. When a lot failure occurs for a group B subgroup, then all other sublots within the inspection lots must be submitted to the failed subgroup.

A.4.5.8.2 Alternate group B failure. When a failure has occurred in group B using the alternate group B procedure, samples from three additional inspection lots of the same package type, lead finish and week of seal as the failed package shall be tested to the failed subgroups. If all three inspection lots pass, then all devices manufactured on the same assembly line using the same package type and lead finish and sealed in the same week may be accepted for group B inspection. If one or more of the three additional inspection lots fails, then no inspection lot containing devices manufactured on the same assembly line using the same package type and lead finish sealed in the same week shall be accepted for group B inspection until each inspection lot has been subjected to and passed the failed subgroups.

A.4.5.8.3 Group C failure. When a group C failure occurs, samples from subsequent wafer lots submitted for acceptance in the same microcircuit group (see A.3.1.3.13), produced on the same die fabrication line, and started (or completed at the manufacturer's option) die fabrication during the same year shall be subjected to group C. The testing shall be performed on a wafer-lot-by-wafer-lot basis until three consecutively tested wafer lots from the same microcircuit group and year of fabrication pass group C; the testing may then return to periodic testing. A device type which fails a group C inspection shall not be accepted until the device type which failed successfully completes group C. In addition, any other inspection lots using die from the same failed wafer lot must successfully complete group C prior to shipment until three successive inspection lots from the same wafer lot have passed group C using a tightened sample size number(accept number) with C = 0. In the event of a group C failure the manufacturer shall evaluate the possible impact on product which has been manufactured since the last acceptable group C test (based on wafer fab code), from the failed microcircuit group.

A.4.5.8.4 Group D failure. When a failure occurs for a group D subgroup(s), samples from subsequent lots submitted for acceptance of the same package family and lead finish shall be subjected to all the tests in the failed subgroup(s). The testing shall be performed on a lot-by-lot basis until three successive lots of the same package family pass the failed subgroup(s). Testing of the package family may then return to periodic testing. The package type that failed the Group D subgroup(s) shall be tested on a lot-by-lot basis until 3 successive lots pass the failed subgroup(s) at which time it may return to periodic inspection coverage. Under the worst case conditions option, when a glass sealed package fails, every package type in the package family must pass the failed group D subgroup, prior to shipping the device. Failed package types shall be tested on a lot-by-lot basis until 3 successive lots of the same package type pass the failed subgroup(s) at which time it may return to periodic inspection. In the event of a group D failure the manufacturer shall evaluate the possible impact on product which has been manufactured since the last acceptable group D (based on seal or encapsulation date code), for the failed package family.

A.4.6 Screening. Each microcircuit shall have been subjected to and passed all the screening tests detailed in test method 5004 or test method 5010, as applicable, of MIL-STD-883 for the specified quality assurance level and type of microcircuit in order to be acceptable for delivery. When a PDA (see A.3.1.3.14 herein and test methods 5004, or 5010 of MIL-STD-883) or delta limits (see A.3.1.3.15) has been specified or other conditions for lot acceptance, have been imposed, the required data shall be recorded and maintained as a basis for lot acceptance. Devices which fail any test criteria in the screening sequence shall be removed from the lot at the time of observation or immediately at the conclusion of the test in which the failure was observed. Once rejected and verified as a device failure, no device may be retested for acceptance.

A.4.6.1 Burn-in. Burn-in shall be performed on all microcircuits where specified and the specified pre- and post-burn-in electrical parameters shall be measured.

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A.4.6.1.1 Lots and sublots resubmitted for burn-in. Inspection lots, lot splits, and class level S sublots may be resubmitted for burn-in one time only and may be resubmitted only when the observed percent defective does not exceed twice the specified PDA, or 20 percent whichever is greater. Resubmitted inspection lots, lot-splits, and class level S sublots shall contain only parts which were in the original lot or sublot. Resubmitted inspection lots, lot splits, and class level S sublots shall be kept separate from new lots and sublots and shall be inspected for all specified characteristics using a tightened inspection PDA equal to the next lower number in the sample size series (see appendix D), or one device, whichever is greater.

A.4.6.1.2 Burn-in acceptance criteria. The PDA for each inspection lot or class level S sublot submitted to burn-in and interim (post burn-in) electrical parameters (see test method 5004 of MIL-STD-883) shall be 5 percent (or one device, whichever is greater) on all failures. In addition, for class level S, the PDA shall be 3 percent (or one device, whichever is greater) on functional failures. A manufacturer may elect to divide inspection lots into splits for burn-in and interim electrical parameter measurement and calculate a PDA for each split, or the manufacturer may elect to add all failures from the constituent splits together to calculate a PDA for the original inspection lot. If a PDA is calculated for each split it shall be used as accept/reject criteria for that split only and shall not be combined with the PDA from any other lot or split for any reason related to lot or split acceptance. If a PDA is calculated for an inspection lot by adding the failures found in the various constituent splits, this PDA shall be used as accept/reject criteria for the entire lot and shall, in no way, be used as accept/reject criteria for any grouping of devices other than the entire lot. Delta limits shall be defined in the device specification or drawing. When the PDA applies to delta limits, the delta parameter values measured after burn-in (100 percent screening test) shall be compared with the delta parameter values measured prior to that burn-in. Lots may be resubmitted only when the observed percent defective does not exceed twice the specified PDA or 20 percent, whichever is greater. The delta criteria applying to such resubmissions shall be in accordance with the following procedure:

a. Devices having delta drift values in excess of the device specification or drawing limits shall be rejected.

b. The remaining devices shall then be submitted to the balance of inspections and tests as specified herein.

A.4.6.1.2.1 Failure analysis of burn-in screen failures for class level S devices. Catastrophic failures (i.e., shorts or opens measurable or detectable at +25°C) subsequent to burn-in shall be analyzed. Analysis of catastrophic failures may be limited to a quantity and degree sufficient to establish failure mode and cause and the results shall be documented and made available to the Government representative.

A.4.6.2 External visual screen. The final external visual screen shall be conducted in accordance with test method 2009 of MIL-STD-883 after all other 100 percent screens have been performed to determine that no damage to, or contamination of the package exterior has occurred.

A.4.6.3 Particle impact noise detection (PIND) test for class level S devices. The inspection lot (or sublots) shall be submitted to 100 percent PIND testing a maximum of five times in accordance with test method 2020 of MIL-STD-883, condition A. PIND prescreening shall not be performed. The lot may be accepted on any of the five runs if the percentage of defective devices is less than 1 percent (zero failures allowed for lots of less than 100 devices). All defective devices shall be removed after each run. Lots which do not meet the 1 percent PDA on the fifth run, or exceed 25 percent defectives cumulative, shall be rejected and resubmission is not allowed.

A.4.6.4 Lead forming. When lead forming (bending) is specified for any device class, a sample fine and gross seal test shall be performed in accordance with test method 5004 of MIL-STD-883 after the lead forming operations and prior to final visual inspection of these devices, and devices which fail any test shall be removed from the lot.

A.4.6.5 Nondestructive bond pull test for class level S devices. Nondestructive 100 percent bond pull test shall be performed for class level S devices. The total number of failed wires and the total number of devices failed shall be recorded. The lot shall have a PDA of 2 percent or less based on the number of wires pulled in specified lot. The test shall be performed in accordance with test method 2023 of MIL-STD-883. Devices from lots which have been subjected to the nondestructive 100 percent bond pull test and have failed the specified class level S, PDA requirement shall not be delivered as class level B product.

A.4.7 Test results. The results of all qualification and quality conformance tests and inspections and the results of all required failure analysis shall be recorded and maintained in the manufacturer's facility in accordance with A.4.8. The Quality Assurance Program Plan, qualification test reports, summary of QCI data, and any other data reports required by the applicable acquisition document shall be maintained by the manufacturer (or submitted to the acquiring activity when specified in the purchase agreement). The disposition of all lots or samples submitted for wafer lot acceptance, screening (when PDA is specified), quality conformance inspection or qualification shall be fully documented and lots which fail any specified requirement shall be recorded as failed lots whether resubmitted or withdrawn. Disposition of resubmitted lots shall likewise be recorded so that a complete history is available for every lot tested from initial submission to final disposition including all failures, resubmissions, and withdrawals.

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A.4.7.1 Screening test data for class level S microcircuits. When specified in the acquisition document, a copy of the attributes test data, a copy of the variables data and the delta calculations resulting from the applicable delta parameter tests before and after each burn-in, and a copy of the X-rays required by the device specification or drawing shall accompany each lot of class level S microcircuits shipped. The manufacturer shall maintain one complete copy of all screening data for 5 years after delivery of the parts. This data shall be legible and shall be correlatable to the applicable PIN, the lot date code, and the individual serial number. The data shall be verified by the manufacturer's quality assurance organization and must bear evidence of such verification.

A.4.8 QUALITY ASSURANCE PROGRAM

A.4.8.1 Manufacturer certification. The manufacturer shall establish, implement, and maintain a quality assurance program in accordance with A.4.8 through A.4.9.3.8 (summarized in table A-X) in order to be a manufacturer of class level B microcircuits. The manufacturer's quality assurance program shall demonstrate and assure that design, manufacture, inspection and testing of microcircuits are adequate to assure compliance with the applicable requirements and quality standards of this specification. Where the manufacture or any portion of the manufacturing and testing operation is other than the manufacturer's facility, it shall be the responsibility of the manufacturer to secure and prove the documentation and control of the quality assurance program as described herein. The program shall be documented in these ways:

a. Design, processing, manufacturing, and testing instructions (A.4.8.1.1).

b. Records to be maintained (A.4.8.1.2).

c. Quality assurance program plan (A.4.8.1.3).

All required documentation shall be available at, and continually effective in the manufacturer's plant while it is producing microcircuits which are intended to be offered for qualification and quality conformance inspections under this specification.

All required program documentation and records shall be available for review by acquiring activity upon request. The acquiring activity shall have access to nonproprietary areas of the manufacturer's plant for the purpose of verifying its implementation, and the Government shall have access to all areas of the manufacturer's plant for the purpose of verifying its implementation.

Personnel performing quality functions shall have sufficient well defined responsibility, authority, and the organizational freedom to identify and evaluate quality problems and to initiate, recommend, and provide solutions.

A.4.8.1.1 Design, processing, manufacturing, and testing instructions. The manufacturer shall have in effect documented instructions covering, as a minimum, these areas:

a. Conversion of customer requirements into manufacturer's internal instructions (see A.4.8.1.1.1).

b. Personnel training and testing (see A.4.8.1.1.2).

c. Inspection of incoming materials, utilities, and work in-process (see A.4.8.1.1.3).

d. Quality-control operations (see A.4.8.1.1.4).

e. Quality-assurance operations (see A.4.8.1.1.5).

f. Design, processing, manufacturing equipment, and materials instructions (see A.4.8.1.1.6).

g. Cleanliness and atmosphere control in work areas (see A.4.8.1.1.7).

h. Design, material, and process change control (see A.4.8.1.1.8).

i. Tool, gauge, and test equipment maintenance and calibration (see A.4.8.1.1.9).

j. Failure and defect analysis and feedback (see A.4.8.1.1.10).

k. Corrective action and evaluation (see A.4.8.1.1.11).

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l. Incoming, in-process, and outgoing inventory control (see A.4.8.1.1.12).

m. Schematics (see A.4.8.1.1.13).

n. ESD handling control program (see A.4.8.1.1.14).

Detailed requirements for coverage of these items are stated in A.4.8.1.1.1 through A.4.8.1.1.14. These requirements will normally be expected to be met by the manufacturer's standard drawings, specifications, process instructions, and other established manufacturing practices. If particular requirements are not
covered by the manufacturer's established practices, suitable documentation shall be added to satisfy those requirements.

A.4.8.1.1.1 Conversion of customer requirements into manufacturer's internal instructions. The procedure by which customer requirements, as expressed in specifications, purchase orders, etc., are converted into working instructions for the manufacturer's personnel shall be documented.

A.4.8.1.1.2 Personnel training and testing. The motivational and work training and testing practices employed to establish, evaluate, and maintain the skills of personnel engaged in reliability-critical work shall be documented as to form, content, and frequency of use.

A.4.8.1.1.3 Inspection of incoming materials and utilities, and of work in-process. Inspection operations shall be documented as to type of inspection, sampling and test procedures, acceptance-rejection criteria, and frequency of use.

A.4.8.1.1.4 Quality-control operations. Quality-control operations shall be documented as to type, procedures, rating criteria, action criteria, records, and frequency of use.

A.4.8.1.1.5 Quality-assurance operations. Quality-assurance operations shall be documented as to type, procedures, equipment, judgment and action criteria, records, and frequency of use.

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TABLE A-X. Quality assurance program requirements.

In-house documentation covering these areas (see A.4.8.1.1)	In-house records covering these areas (see A.4.8.1.2)	A program plan covering these areas (see A.4.8.1.3)	Self-audit plan covering these areas (see A.4.9)
a. Conversion of customer requirements into manufacturer's internal instructions (see A.4.8.1.1.1)	a. Personnel training and testing (see A.4.8.1.2.1)	a. Functional block organization chart (see A.4.8.1.3.1)	a. Self-audit program (see A.4.9.3.1)
b. Personnel training and testing (see A.4.8.1.1.2)	b. Inspection operations (see A.4.8.1.2.2)	b. Examples of manufacturing flowchart (see A.4.8.1.3.2)	b. Self-audit representatives (see A.4.9.3.2)
c. Inspection of incoming materials and utilities and of work in-process (see A.4.8.1.1.3)	c. Failure and defect reports analysis (see A.4.8.1.2.3)	c. Proprietary documents (see A.4.8.1.3.3)	c. Audit deficiencies (see A.4.9.3.3)
d. Quality-control operations (see A.4.8.1.1.4)	d. Initial documentation and subsequent changes in design, materials, or processing (see A.4.8.1.2.4)	d. Examples of design, material, equipment, and process instructions (see A.4.8.1.3.4)	d. Audit follow-up (see A.4.9.3.4)
e. Quality assurance operations (see A.4.8.1.1.5)	e. Equipment calibrations (see A.4.8.1.2.5)	e. Examples of records (see A.4.8.1.3.5)	e. Audit schedules (see A.4.9.3.5)
f. Design, processing, manufacturing equipment, and materials instructions (see A.4.8.1.1.6)	f. Process utility and material controls (see A.4.8.1.2.6)	f. Examples of design, material, and process change control documents (see A.4.8.1.1.8 and as required in A.3.4.2 herein)	f. Self-audit report (see A.4.9.3.6)
g. Cleanliness and atmosphere control in work areas (see A.4.8.1.1.7)	g. Product lot identification (see A.4.8.1.2.7)	g. Examples of failure and defect analysis and feedback documents (see A.4.8.1.1.10)	g. Self-audit (see A.4.9.3.7)
h. Design, material, and process change control (see A.4.8.1.1.8)	h. Product traceability (see A.4.8.1.2.8)	h. Examples of corrective actions and evaluations documents (see A.4.8.1.1.11)	h. Self-audit checklist (see A.4.9.3.8)
i. Tool, gauge, and test equipment maintenance, and calibration (see A.4.8.1.1.9)	i. Self-audit report (see A.4.9.3.6)	i. Manufacturer's internal instructions for internal visual inspection (see A.4.8.1.3.6)	
j. Failure and defect analysis and feedback (see A.4.8.1.1.10)		j. Examples of test travelers (see A.4.8.1.3.7)	
k. Corrective action and evaluation (see A.4.8.1.1.11)		k. Examples of design and construction baselines (see A.4.8.1.3.8)	
l. Incoming, in-process, and out-going inventory control (see A.4.8.1.1.12)		l. Manufacturer's self-audit (see A.4.9.1)	

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TABLE A-X. Quality assurance program requirements - Continued.

In-house documentation covering these areas (see A.4.8.1.1)	In-house records covering these areas (see A.4.8.1.2)	A program plan covering these areas (see A.4.8.1.3)	Self-audit plan covering these areas (see A.4.9)
m. Schematics (see A.4.8.1.1.13) n. ESD handling control program (see A.4.8.1.1.14)			

A.4.8.1.1.6 Design, processing, manufacturing equipment, and materials instructions. Device design, processing, manufacturing equipment and materials shall be documented in drawings, standards, specifications, or other appropriate media which shall cover the requirements and tolerances for all aspects of design and manufacture including equipment test and prove-in, materials acquisition and handling, design-verification testing and processing steps. As a minimum requirement, detailed documentation must exist for the following items and must be adequate to assure that quantitative controls are exercised, that tolerances or limits of control (limits shall be established for baselined and other critical wafer fabrication process monitors used for acceptance of class levels B and S product) are sufficiently tight to assure a reproducible high quality product and that process and inspection records reflect the results actually achieved:

a. Incoming materials control (wafers, substrates, packages, active and passive chips or elements for hybrid or multichip microcircuits, wire, water purification, etc.).

b. Masking, photoresist, and mask registration.

c. Epitaxy and diffusion.

d. Oxidation and passivation.

e. Metallization and film deposition.

f. Die, element, and substrate attachment.

g. Bonding.

h. Rework.

i. Sealing.

A.4.8.1.1.7 Cleanliness and atmosphere control in work areas. The requirements for cleanliness and atmosphere control in each work area in which unsealed devices, or parts thereof, are processed or assembled shall be documented. During manufacture, transit, and storage, prior to seal, microcircuit die/wafers shall be protected from human contamination, machine overspray, or other sources of contamination which may occur due to human error or machine design which does not totally eliminate the possibility of overspray or other forms of contamination. Airborne particulate class limits shall be as defined by Federal Standard 209. A method for class verification and reverification shall be documented and implemented. Federal Standard 209 may be used as a guideline. The manufacturer shall establish action and absolute control limits (at which point work stops until corrective action is completed) based on historical data and criticality of the process in each particular area. For foreign material identification and control, see internal visual inspection requirements test method 2010 of MIL-STD-883.

A.4.8.1.1.8 Design, material, and process change control. The methods and procedures for implementation and control of changes in device design, material and processing, and for making change information available to the acquiring activity, when applicable, shall be documented.

A.4.8.1.1.9 Tool, gauge, and test equipment maintenance and calibration. The maintenance and calibration procedures, and the frequency of scheduled actions, for tools, gauges, manufacturing and test equipment shall be documented and in accordance with in-house requirements. ANSI/NCSL Z540-1 or equivalent should be used as a guideline. Failure to perform scheduled maintenance, repair and recalibration requirements critical to a process (as defined by the manufacturer) shall require corrective action.

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A.4.8.1.1.10 Failure and defect analysis and feedback. The procedures for identification, handling, and analysis of failed or defective devices and for dissemination of analysis data shall be documented, including the procedure for informing the qualifying activity of analysis results, when applicable.

A.4.8.1.1.11 Corrective action and evaluation. The procedure and responsibility for decisions regarding the necessity for corrective action as a result of failure or defect analysis, and for evaluation and approval of proposed corrective actions, shall be documented. If the procedure for evaluation and approval of changes proposed for other reasons, such as cost reduction or product improvement, differs from the above, it shall also be documented.

A.4.8.1.1.12 Incoming, in-process, and outgoing inventory control. The methods and procedures shall be documented which are used to control storage and handling of incoming materials, work in-process, and warehoused and outgoing product in order to (a) achieve such factors as age control of limited-life materials; and (b) prevent inadvertent mixing of conforming and nonconforming materials, work, or finished product. Tests and inspections performed by the manufacturers on acquired materials and supplies shall include verification of chemical, physical, and functional characteristics required by manufacturer drawings and specifications. Procedures shall be prepared and maintained for controlling the receipt of acquired materials and supplies. The procedures shall provide the following:

a. Withholding received materials or supplies from use pending completion of the required inspection or tests, or the receipt of necessary reports.

b. Segregation and identification of nonconforming materials and supplies from conforming materials and supplies and removal of nonconforming subassemblies and parts.

c. Identification and control of limited-life materials and supplies.

d. Identification and control of raw materials.

e. Assurance that the required test reports, certification, etc., have been received.

f. Clear identification of materials released from receiving inspection and test to clearly indicate acceptance or rejection status of material pending review action.

A.4.8.1.1.13 Schematics. Schematics pertaining to the testing of microcircuits shall be under document control. This includes device schematics, burn-in schematics in accordance with the applicable device specification or drawing.

A.4.8.1.1.14 ESD handling control program. The ESD handling control program documentation shall be under document control. This includes methods, equipment and materials, training, packaging, handling, and procedures for handling ESD sensitive devices.

A.4.8.1.2 Records to be maintained. The records required by this section shall be continuously maintained during the manufacture of microcircuits which are intended to be submitted for quality conformance inspection under this specification. The records pertaining to production processes, incoming and in-process inspections shall be retained as detailed in item b below. Those pertaining to screening and quality conformance inspection shall be retained for a minimum of 5 years after performance of the inspections. Records shall be maintained as a minimum for:

a. Personnel training and testing (see A.4.8.1.2.1) (1-year active file retention; 5-year total record retention).

b. Inspection operations (see A.4.8.1.2.2) (1-year record retention for production processes, incoming and in-process; 5-year record retention for screening, qualification, and quality conformance inspection).

c. Failure and defect reports and analyses (see A.4.8.1.2.3) (5-year record retention).

d. Initial documentation and subsequent changes in design, materials, or processing (see A.4.8.1.2.4) (5-year record retention).

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e. Equipment calibrations (see A.4.8.1.2.5) (see ANSI/NCSL Z540-1 for records).

f. Process, utility, and material controls (see A.4.8.1.2.6) (1-year record retention).

g. Product lot identification (see A.4.8.1.2.7) (5-year record retention).

h. Product traceability (see A.4.8.1.2.8) (5-year record retention).

i. Self-audit report (see A.4.9.3.6) (4-year retention).

Altered records shall not be considered acceptable data unless documented instructions are followed which shall include:

j. For changed data:

(1) Identification of individual making new entry.

(2) Maintain identity of all original data entries (white out is not permitted).

(3) Justification and date noted for change and verification by a second party (QA shall verify screening, qualification and quality conformance inspection records) when change affects lot jeopardy (i.e., lot originally considered to be rejected is changed to pass status).

k. For transferred data to new test record:

(1) Identification of individual transferring data.

(2) All original record entries shall be transferred.

(3) New test record entries shall be verified against the original record by a second party.

l. Computerized records are optional provided they clearly and objectively indicate that all minimum class level B requirements of this appendix have been met. The computerized records for traceability, screening and quality control inspection shall be readily accessible and available to Government personnel for review and an appropriate electronic/hard copy provided to the qualifying activity as required. The requirements below shall be met.

(1) Entry verification:

(a) Each individual making entries shall be uniquely identified.

(b) All manually entered data shall be verified at the time of entry by the same operator.

(c) All accepted transactions (i.e., entered data) shall be identified by time/date or date/entry sequence to protect against "out of sequence" entries. No recorded transactions shall be deleted or changed.

(2) Control procedures for lot history records:

(a) Lot histories may be modified only by additions (i.e., original entries plus corrective addenda).

(b) All corrective addenda shall meet all the requirements of A.4.8.1.2i.

(c) Only limited designated operators shall be able to access lot history computer records for corrective addenda. Documented security procedures shall be followed to assure that limited access is maintained (e.g., restricted terminals, passwords, etc.).

(d) A quality assurance representative shall verify screening, qualification and quality conformance inspection records when corrective addenda affect lot jeopardy.

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(3) Control of computerized lot history records:

(a) All computer lot history records shall have an accurate tape or equivalent backup generated prior to lot shipment. Within 3 months of lot shipment, the backup record shall be transferred to a secure location to be archived.

(b) These archived tapes or equivalent media shall be kept for a minimum of 5 years.

A.4.8.1.2.1 Personnel training and testing. Records shall cover the nature of training or testing given, the date thereof by week and length in hours, and the group(s) of personnel given work training and testing. Records are required only for product-related training and testing as distinguished from safety, first aid, etc.

A.4.8.1.2.1.1 Training of operators and inspectors. All critical processes and production inspection shall be performed by personnel who have been trained by the manufacturer to perform their assignment task in accordance with manufacturer's in-house standards, including a formal training (e.g., classroom or on the job training supervised by a certified trainer) and test procedure to assure the proficiency of each individual. Each individual shall be retested or retrained at the end of a designated period or when personnel performance indicates poor proficiency. Personnel shall not be used in critical processes or inspections until the required level of proficiency has been demonstrated.

A.4.8.1.2.2 Inspection operations. Records of inspection operations shall cover the tests or inspections made, the materials group (lot, batch, etc.) inspected, the controlling documentation, the date of completion of inspection, the amount of material tested, and acceptance, rejection, or other final disposition of the material.

A.4.8.1.2.3 Failure and defect reports and analyses. Records of failed or defective devices shall cover the source from which each device was received, the test or operation during which failure occurred or defects were observed, and prior testing or screening history of the device, the date of receipt, and the disposition of the device. Records of failure and defect analyses analysis shall cover the nature of the reported failure or defect (failure or defect mode), verification of the failure or defect, the nature of any device discrepancies which were found during analysis (failure or defect mechanism), assignment of the failure-activating cause if possible, the date of completion of the analysis, identification of the group performing the analysis, disposition of the device after analysis, and the distribution of the record. The record shall also treat the relationship of observed failure or defect modes in related lots or devices and, where applicable, corrective action taken as a result of the findings.

A.4.8.1.2.4 Initial documentation and subsequent changes in design, materials, or processing. Records shall cover the initial documentation and all changes with the date upon which each change in design, materials, or processing becomes effective for devices intended to be submitted for quality conformance inspection under this specification, the documents authorizing and implementing the change, and identification of the first production and quality conformance inspection lot(s) (as applicable) within which product incorporating the change is included shall be maintained when the change requires notification of the qualifying activity (see A.3.4.2 herein).

A.4.8.1.2.5 Equipment calibrations. Records shall cover the scheduled calibration intervals for each equipment item, the dates of completion of actual calibration, identification of the group performing the calibration, and certification of the compliance of the equipment with documented requirements after calibration, (use ANSI/NCSL Z540-1 or equivalent, as a guideline).

A.4.8.1.2.6 Process, utility, and material controls. Records shall cover the implementation of devices such as control charts (e.g., X bar R charts) or other means of indication of the degree of control achieved at the points in the material, utility, and assembly process flow documented in the manufacturing instructions. Records shall also indicate the action taken when each out-of-control condition is observed, and the disposition of product processed during the period of out-of-control operation.

A.4.8.1.2.7 Product lot identification. Records shall be maintained to identify when each production or inspection lot or both was processed through each area. Records shall be capable of identifying for each production and acceptance-inspection lot (as applicable) of finished product, these items as a minimum:

a. The acceptance-inspection tests performed on the lot, and their results.

b. The serial numbers (when applicable) of all devices in the lot.

c. The date of completion of acceptance inspection of the lot.

d. Identification of the lot.

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e. The pertinent device specification or drawing under which inspection was performed.

f. Final disposition of the lot (withdrawn, not accepted, accepted).

g. Acquiring activity source inspection consideration of the lot.

h. The number of devices, by device type, in each lot at the time of seal.

i. Independently identify, by device type, the number of devices shipped and the number of devices in stock inventory.

A.4.8.1.2.8 Product traceability. The traceability system shall be maintained such that the qualifying activity can trace and determine that the microcircuits passed the applicable screening, qualification and quality conformance inspections; that the microcircuits were assembled on the proper certified assembly line, and processed on the correct wafer process line.

A.4.8.1.3 Quality assurance program plan. The quality assurance program plan shall be established and maintained by the manufacturer, and shall be reviewed by the qualifying activity. It shall consist of a volume or portfolio, or series of same, which will serve to demonstrate that the manufacturer's understanding of a complete quality assurance program, as exemplified by his documentation system, is adequate to assure compliance of his product with the applicable specifications and quality standards. If the quality assurance program exemplified is applied consistently to all product lines intended to be submitted for acceptance inspection under this specification, only one program plan is required for each manufacturing plant; any difference in treatment of different product lines within a plant shall be stated and explained in the program plan, or separate program plans prepared for such different lines. The program plan shall contain, as a minimum, these items:

a. Documents representing the manufacturer's quality organization:

(1) Functional block organization chart (see A.4.8.1.3.1).

(2) Example of manufacturing flowchart (see A.4.8.1.3.2).

(3) Proprietary-document identification (see A.4.8.1.3.3).

(4) Examples of design, material, equipment, visual standard, and process instructions (see A.4.8.1.3.4).

(5) Examples of records (see A.4.8.1.3.5).

(6) Examples of design, material and process change control documents (see A.4.8.1.1.8).

(7) Examples of failure and defect analysis and feedback documents (see A.4.8.1.1.10).

(8) Examples of corrective action and evaluation documents (see A.4.8.1.1.11).

(9) Manufacturer's internal instructions for internal visual inspection (see A.4.8.1.3.6).

(10) Examples of test travelers (see A.4.8.1.3.7).

(11) Examples of design and construction baseline (see A.4.8.1.3.8).

(12) Manufacturer's self-audit program (see section A.4.9).

NOTE: Where a manufacturer's lot/test traveler (see A.4.8.1.3.7) contains all the information required for a flowchart (see A.4.8.1.3.2), it may be used to satisfy the requirement for the flowchart.

b. Critical documents which are to be kept current and on file by the qualifying activity:

(1) SPC program plans/milestones, as applicable.

(2) Process flowcharts and baselines (wafer fabrication and assembly).

(3) General QCI procedures.

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(4) Major change notification procedure.

(5) Internal visual inspection procedure.

A.4.8.1.3.1 Functional block organization chart. This chart shall show, in functional block-diagram form, the lines of authority and responsibility (both line and staff) for origination, approval, and implementation of the several aspects of the quality assurance program. Names of incumbents are not required in this chart.

A.4.8.1.3.2 Examples of manufacturing flowchart. The flowchart for all devices shall reflect the complete manufacturing processes being used at the time and shall show all manufacturing, inspection, testing and quality verification points and the point where all materials or subassemblies enter the flow. The flowchart shall clearly show any utilization of third party activities. The chart will identify all major documents pertaining to the inspection of materials, the production processes, the production environments, and production controls which were used. The documents will be identified by name and number. Changes approved thereafter will be treated in accordance with the approved document change control procedures in A.3.4.2.

A.4.8.1.3.3 Proprietary-document identification. A listing of proprietary documents and areas shall be included in the program plan and maintained on a current basis (see A.4.8.1).

A.4.8.1.3.4 Examples of design, material, equipment, visual standard, and process instructions. An example of each type of design, material, equipment, visual standard, and process instruction used in the manufacture of microcircuits intended to be submitted for acceptance inspection under this specification shall be included in the program plan. These may be either dummies or actual working documents, but shall in either event show the form of the pertinent document; blank forms shall not be included.

A.4.8.1.3.5 Examples of records. Examples of records, complying with the requirements of A.4.8.1.3.4 for instructions, shall be included in the program plan.

A.4.8.1.3.6 Manufacturer's internal instructions for internal visual inspection. The manufacturer's internal instructions for internal visual inspection in accordance with test method 2010 or test method 2017, as applicable, of MIL-STD-883 for the applicable device class, shall be included in the program plan.

A.4.8.1.3.7 Examples of travelers. Wafer fab, assembly, screening, and groups A, B, C, D (and E, if applicable) travelers shall be included in the program plan and maintained on current basis. The traveler utilized for quality conformance inspection lots may be the same traveler as used for qualification lots. When in-line inspections are allowed (i.e., alternate group A or B) the traveler shall include documentation of required inspections. The travelers shall include all manufacturer imposed tests. The test traveler shall include all the following minimum information (if applicable):

a. Identification as to whether the lot is qualification or QCI.

b. Name or title of operation and specification number of each process or test.

c. PIN, date code, and manufacturer internal lot identification number(s).

d. Date(s) of test and operator identification.

e. Calibration control number or equipment identification of all major equipment components used for test.

f. Quantity tested and rejected for each process or test and actual quantity tested if sampled.

g. Serial numbers of passing and failing devices when applicable.

h. Time in and out of process or test if critical to process or test results (i.e., burn-in and 96-hour window).

i. Specific major conditions of test that are verifiable by operator including times, temperatures, RPMs, etc. (Not required for screening and QCI traveler.)

j. The percent defective calculated for burn-in.

k. Burn-in/life test board serial number or test circuit identification number and revision.

l. All required variables data except for electrical tests (attachments permitted). (Not required for QCI traveler.)

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m. For electrical tests, test program number and revision and identify when variables data is required.

* A.4.8.1.3.8 Examples of design and construction baseline. The design and construction baseline information (e.g., DSCC-VQC-42 DSCC Microcircuit Materials and Construction Baseline Sheet, or equivalent) shall be included in the manufacturer's program plan and maintained under document control. The baseline form shall clearly show any utilization of third party activities.

A.4.9. SELF-AUDIT REQUIREMENTS

A.4.9.1 Self-audit requirements. The intent of the self-audit program is to assure continued conformance to specification requirements.

A.4.9.2 DEFINITIONS

A.4.9.2.1 Self-audit. The performance of periodic survey by the device manufacturer's designated personnel to evaluate compliance to specifications.

A.4.9.2.2 Audit checklist. A form listing specific items which are to be audited.

A.4.9.3 GENERAL

A.4.9.3.1 Self-audit program. The manufacturer shall establish an independent self-audit program under the direction of the quality organization to assess the effectiveness of the manufacturer's compliance to all applicable specifications. The manufacturer's self-audit program which identifies key review areas, their frequency of audit, and the corrective action system to be employed when variations from the approved procedures or specification requirements are identified shall be included in the program plan. The self-audit program shall, as a minimum, incorporate the following requirements.

A.4.9.3.1.1 Correction of deficiencies. A system to identify and correct any deficiencies (e.g., processing and testing) or deviations from the specification requirements.

A.4.9.3.1.2 Deviation from critical documents. Provide for review of all deviations from critical documents, such as, baseline(s), flowchart(s), traveler(s), QCI procedures, etc.

A.4.9.3.1.3 Training and retention of auditors. Specify the selection and training/retraining requirements for auditors.

A.4.9.3.1.4 Self-audit schedule and frequency. Specify the self-audit frequencies and require that a schedule be established and adhered to.

A.4.9.3.2 Self-audit representatives. The quality assurance representatives or the designated appointees shall perform all self-audits. The designated auditors shall be independent from the area being audited. If the use of an independent auditor is not practical, then as a minimum, another individual should be assigned to participate in the audit or review the results with the auditor from the area. The auditors shall be trained in the area to be audited, in the applicable specification requirement and provided with an appropriate checklist for annotating deficiencies. Prior to the audit, the assigned auditor(s) shall review the previous audit checklist to assure corrective actions have been implemented and are sufficient to correct the deficiencies.

A.4.9.3.3 Audit deficiencies. All audit deficiencies shall be documented on the appropriate form and a copy submitted to the department head for corrective action(s). All corrective actions shall be agreed to by the quality organization or Material Review Board.

A.4.9.3.4 Audit follow up. All audit reports will be filed and maintained by the quality organization. The quality organization shall establish a procedure to follow up on all audit deficiencies to assure that the corrective actions have been implemented in a timely manner. A system (e.g., Management Review) shall also be established to review the acceptability and timeliness of all corrective actions and to determine if any deficiencies have repeated since the last required self-audit. If any deficiencies have occurred two or more times in the predetermined time period, additional corrective actions shall be taken to assure immediate correction of the problem and the qualifying activity shall be notified. The self-audit team shall perform a 6-month follow-up verification of corrective actions covering all deficiencies found during the qualifying activity audit and annual self-audit to assure corrective actions are adequate and maintained.

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A.4.9.3.5 Audit schedules and internals. The original audit interval shall be established with a schedule by the quality organization but in no case exceed 1 year for each area, unless authorized by the qualifying activity. A self-audit shall be conducted and corrective actions completed prior to the initial qualifying activity audit. Changes to the audit schedule, due to being consistently above or below average performance on the self-audit shall require approval of the qualifying activity.

A.4.9.3.6 Self-audit report. The self-audit report shall be signed by the quality assurance representative responsible for the quality assurance program's overall success or failure. The manufacturer shall make available to the qualifying activity, during audits, the self-audit report, deficiencies, and corrective actions taken. This report shall include a summary report of self-audit results categorized by deficiency type (i.e., nonconformance to specification requirement(s), occurrences affecting product reliability, recurring deficiencies).

A.4.9.3.7 Self-audit areas. The self-audit will be performed to assure conformance to the checklist and specification in at least the following areas:

Calibration and preventive maintenance
Fabrication
Assembly operations
Electrical test
Test methods
Environmental control
Incoming inspection
Inventory control and traceability
ESD handling control program
DI water controls
Training
Failure analysis
Qualification/QCI system
Document control
Design change control
Statistical process control, as applicable
Third party subcontractors 1/

A.4.9.3.8 Self-audit checklist. The audit checklist shall be prepared by the quality organization and maintained under document control. The checklist shall assure that the quality assurance system is adequate and followed by all personnel in each area.

A.5 PACKAGING

A.5.1 Packaging requirements. The packaging of microcircuits shall prevent mechanical damage to the device during shipping and handling and the packaging material shall not be detrimental to the device.. In addition, microcircuits which have been determined to require electrostatic discharge protection, category A or class 1 or 2 by test method 3015 of MIL-STD-883, shall be packaged in conductive material or packaged in accordance with one of the following:

Category A.

(1) Unit container suitable for ESD protection.
or

(2) Conductive noncorrosive rail with noncorrosive and conductive or antistatic foam plugs at both ends of each rail which prevents movement.
or

(3) Antistatic noncorrosive rail with noncorrosive and conductive or antistatic foam plugs at both ends of each rail which prevents movement. Antistatic rails shall be packaged in conductive, electrostatic field shielding material.

(Other packaging methods shall require the approval of the acquiring activity.)

NOTE: Rails (i.e., multiple carriers) coated but not impregnated with antistats shall be used only if the antistatic properties are proven to be intact on the surface. These measurements shall conform to A.3.1.3.22 and EIA-STD-541.

A.5.1.1 Carrier and container. When specified on the associated detail specification or purchase order, microcircuits shall be supplied mounted in the carrier (unit or multiple) and carrier container, or carrier and unit container. Marking on the carrier or unit container shall be as specified in A.5.1.2.

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A.5.1.2 Marking of container. All of the markings specified in A.3.6, except the index point and serialization, shall appear on the carrier, unit pack (e.g., individual foil bag), unit container, or multiple carriers (e.g., tubes, rails, magazines) for delivery. An industry standard symbol for identifying ESD sensitive items (e.g., EIA-STD-RS-471 symbol) shall be marked on the carrier or container. However, if all the marking specified above is clearly visible on the devices and legible through the unit carrier or multiple carrier, or both, then the ESD marking only (in accordance with MIL-STD-1285) shall be required on the multiple carrier. These requirements apply to the original or repackaged product by the manufacturer or distributor.

A.6 NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory.)

A.6.1 Intended use. Microcircuits conforming to this appendix are intended for use for Government microcircuit application and logistic purposes. For maximum cost effectiveness while maintaining essential quality and reliability requirements, it is recommended that, for initial acquisitions for original equipment complements, the device class appropriate to the need of the application (see A.3.4) be acquired.

A.6.2 Acquisition requirements. Acquisition documents should specify the following:

a. Title, number, and date of the specification.

b. Issue of DoDISS to be cited in the solicitation, and if required, the specific issue of individual documents referenced (see A.2.1).

c. PIN and compliance identification (if applicable).

d. Test data to be furnished.

e. Selection of applicable level of packaging required (see A.5.1), specification of carrier and container, as applicable (see A.5.1.1) and special marking, when applicable (see A.5.1.2).

f. Requirement for radiation hardness assurance testing (see A.4.4.2.5 and A.4.5.6).

A.6.2.1 Lead finish designator. For Government logistic support, the A lead finish will be ordered and supplied to the end user when X is used in place of the A, B, or C lead finish designator. If the device type is not available with lead finish A, the same PIN will be ordered except that C or B will be used as the lead finish designator depending upon which is available.

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APPENDIX B

SPACE APPLICATION

B.1 SCOPE

* B.1.1 Scope. This appendix presents the requirements which shall be used to supplement this specification for space system microcircuits. The manufacturer's process may include innovative and improved processes that result in an equivalent or higher quality product, provided that the process used to evaluate and document these changes has been reviewed and approved. The approach outlined in this appendix is a proven baseline which contains details of the screening and TCI procedures. Manufacturers must be able to demonstrate a process control system that achieves at least the same level of quality as could be achieved by complying with this appendix. This appendix is intended for space application and is mandatory for a V level device.

* B.2 APPLICABLE DOCUMENTS.
(This section is not applicable to this appendix)

B.3 REQUIREMENTS

* B.3.1 General. Microcircuits supplied to this appendix shall be manufactured and tested in accordance with approved baselines and the requirements herein as applicable. Only “V” level product marked with an RHA designator is required to meet Table B-1 herein. Upon approval from the TRB and the qualifying activity, screening and TCI may be modified for QML V level product, provided substantiating data is submitted to demonstrate that the manufacturer has a defined capability on the manufacturing line which is controllable, and in control. These changes cannot affect any thermal, mechanical or electrical parameters, which affect form, fit, or function of the device, defined within the device specification or SMD. NASA, Air Force Space and Missiles Center, and the customer shall be notified of major changes to the manufacturer's QM plan.

B.3.1.1 Acquiring activity. When specified by the acquisition document (purchase order), the acquiring activity may:

a. Require prior notification of major changes to the baselined processes, procedures, or testing.

b. Require independent verification of wafers (unprobed) or packaged devices (TCV, SEC, or actual devices) by OEM's or Government agencies.

c. Request screening and TCI summary data be delivered with the devices.

* B.3.2 Conflicting requirements. In the event of conflict between the requirements of this appendix and other referenced documents, the order of precedence shall be as follows:

a. The acquisition document (purchase order).

b. Applicable device specification.

c. This appendix.

d. MIL-PRF-38535.

e. Specifications, standards, and other documents referenced in 2.1 of MIL-PRF-38535.

NOTE: The acquisition document may specify additional requirements, but shall not reduce or waive any requirements herein.

* B.3.3 Validation (certification). Validation of a manufacturing line for production of integrated circuits for use in space systems shall be accomplished by a team headed by DSCC with observers solicited from NASA, Air Force Space and Missiles Center, the services, and the customer.

B.3.4 Manufacturing verification. When specified, the manufacturing verification procedure for new microcircuits shall include characterization of actual devices in increments of ambient or case temperature, supply voltage and input voltage levels over the specified parameter range.

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B.3.5 Design verification. When specified, a fully functional VHSIC Hardware Description language (VHDL) model shall be available.

B.3.6 Part or Identifying Number (PIN). Each V level QML microcircuit shall be marked with the device class designator "V" in place of the "Q" designator in the PIN format, see 3.6.2a herein. Devices procured to M38510 PINs shall be marked in the format in 3.6.2b herein with the device class designator "S".

B.3.7 Serialization. Prior to the first recorded electrical measurement in screening each class V microcircuit shall be marked with a unique serial number assigned within the level of the individual microcircuit within that inspection lot.

B.3.8 Traceability. For class V, inspection lot records shall be maintained to provide traceability from the device serial number to the specific wafer lot or to the specific wafer when testing to any group E subgroup (see table B-I), is performed on a wafer by wafer basis.

B.4 VERIFICATION (QUALITY AND RELIABILITY ASSURANCE)

B.4.1 Screening. In addition to the screening tests specified in the main body of this specification the screening tests specified below shall be performed, unless prior approval for deletion or modification is given by the qualifying activity.

a. Nondestructive Bond Pull (NDBP) in accordance with MIL-STD-883, test method 2023, or approved alternate verified during validation, on each interconnect bond. An alternate method, if necessary, shall consider a 100 percent visual inspection of the elements to be bonded (i.e., bond pads and posts) prior to the bonding operation, as one part of an overall alternate method.

b. Internal visual inspection in accordance with MIL-STD-883, test method 2010, condition A, or approved alternate verified during validation on each microcircuit. An alternate method, if necessary, must address all the inspection topics of test method 2010.

c. Particle Impact Noise Detection (PIND) in accordance with MIL-STD-883, test method 2020 on each device.

* d. Reverse bias burn-in in accordance with MIL-STD-883, test method 1015 on each device as specified in the applicable device specification.

e. Radiograph inspection in accordance with MIL-STD-883, test method 2012 on each device. Only one view is required for flat packages and LCC's having lead terminal metal on four sides.

f. Burn-in test in accordance with MIL-STD-883, test method 1015, on each device for 240 total hours at +125°C. For a specific device type, the burn-in duration may be reduced from 240 to 160 hours if three consecutive production lots of identical parts, from three different wafer lots pass PDA requirements after completing 240 hours of burn-in. Sufficient analysis (not necessarily failure analysis) of all failures occurring during the run of the three consecutive burn-in lots shall not reveal a systematic pattern of failure indicating an inherent reliability problem which would require that burn-in be performed for a longer time. Other burn-in conditions may be considered by a class V validation team. The manufacturer's burn-in procedures must contain corrective action plans, approved by the validation team, for dealing with lot failures. PDA shall be in accordance with MIL-STD-883, test method 5004, for class S.

B.4.2 Technology Conformance Inspection (TCI). Unless otherwise noted herein, the TCI requirements listed below apply on each lot of deliverable devices. The group and table references correspond to those contained herein. These requirements do not replace the normal TCI testing requirements of this specification.

a. Group A, table III, shall be performed on each deliverable lot using actual devices. For those lots having a quantity of less than 116 devices, the tests shall be imposed on a 100 percent basis and the lot accepted on zero test rejects. If a microcircuit fails a group A test parameter as a result of faulty test equipment or operator error, the cause shall be determined and documented, and corrective action shall be implemented and documented.

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The affected lot may then be accepted by being resubmitted to the failed test parameters using a 116/0 or 100 percent/0 sample. If a microcircuit fails a group A test due to a previously unscreened parameter, the affected lot may be accepted by screening the lot 100 percent for the failed parameters, and resubmitting a group A sample to the failed subgroup using a 116/0 or 100 percent/0 sample. Any failures resulting from the second screen shall count toward the lot total percent defective. PDA shall be in accordance with MIL-STD-883, test method 5004, for class S.

Group A electrical tests are not required to be performed when the following conditions are met:

1. The final electrical tests of the 100 percent screening test (see table I) includes all required group A tests (see table III).
2. The test setup and test conditions are verified by a certified monitor other than the test operator.
3. Analysis of failures does not indicate a generic or lot related reliability problem.

In no event shall the absence of separate group A testing result in a failure to satisfy the data requirements of section B.3.1.1c.

* b. Group B, table II, shall be performed on actual devices except as noted here-in. Empty device packages or electrical rejects may be used for subgroups B-1 and B-3, and electrical rejects that have been subjected to the 100 percent screening tests may be used for subgroup B-2. The electrical rejects and empty packages shall have been produced under equivalent conditions as the production lot. The TRB must determine that the intent of the tests are not violated. The sample size of table II is acceptable provided the 22(0) bond strength and solderability criteria has been applied to at least two separate devices (i.e., 11 leads per device), and the die shear test is applied with a 2(0) criteria.

c. The group C requirements shall be met using one of the procedures below.

c-I. Group C, table IV, shall be performed on a quantity (accept) criteria of 22(0). For lots greater than 200, actual devices shall be used. For lots less than or equal to 200, the number of actual devices shall be the greater of 5 devices or 10 percent of the lot, and the SEC shall supplement actual devices to result in a sample of 22 unless acceptable group C data from the SEC is available for the previous 3 months. The SEC shall have been produced under equivalent conditions as the production lot and as close in time as feasible, but not to exceed a 3-month period.

c-II. Group C tests shall be performed on the initial production lot of actual devices from each wafer lot, in accordance with table IV. Group C tests are not required to be performed on subsequent production lots when all the following conditions are met:

1. Subsequent production lots utilize die from the same wafer lot as the initial production lot.
2. Wafers and/or die remaining from the initial production lot are stored in dry nitrogen, and in covered containers.
3. No major changes to the assembly processes have occurred since the group C test was performed on the initial wafer lot.

d. Group D test requirements, following package technology style characterization testing (see table H-IIA and H-IIB), and group D testing on the initial production lot utilizing the package family of interest, shall be in accordance with MIL-PRF-38535 and the manufacturer's approved QM plan. A package family consists of a set of package types with the same package configuration (e.g., side brazed, bottom brazed) material type (e.g., alumina, beryllium oxide (BeO)) package construction techniques (e.g., single layer, multilayer) terminal pitch, except for can packages in which pin circle diameter can be used in place of terminal pitch, lead shape (e.g., gullwing, J-hook), and row spacing (i.e., dual-in-line packages only) and with identical package assembly techniques (e.g., material and type of seal, wire bond method and wire size, die attach method and material). All new alternate sources of package elements must be qualified to the applicable group D tests.

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e. Group E inspection shall be performed in accordance with table B-I below. MOS microcircuits, when specified, shall be tested for time dependent effects post total dose irradiation. When 100 percent latch-up screen is specified, the PDA shall be 5 percent or one device, whichever is greater. The devices used for group E testing shall pass the specified group A electrical tests. An alternate procedure to table B-I may be used upon approval of the qualifying activity.

* TABLE B-I. Group E (RHA) TCI, Class V. 1/

Test	Test method (MIL-STD-883)	Quantity (accept number)	Notes
* Subgroup 1 Neutron irradiation	1017	2(0) devices/wafer or 11(0) devices/wafer lot	2/3/10/ 6/ 2/3/10/ 6/
Subgroup 2 Total ionization dose	1019	2(0) devices/wafer or 22(0) devices/wafer lot	2/9/10/ 2/10/
		1(0) device/wafer + 4(0) test structures/wafer or 5(0) devices/wafer lot + 4(0) test structures/wafer	2/4/5/10/ 2/4/5/10/
Subgroup 3 Transient ionization	1021 1023	2(0) devices/wafer or 11(0) devices/wafer lot	6/ 6/
Subgroup 4 Dose-Rate latch-up	1020	As specified in the device specification	6/7/
* Subgroup 5 Single-event effects	ASTM F-1192 or EIA /JESD 57	4(0) devices/wafer	8/ 6/

1/ Group E tests may be performed prior to device screening. Endpoint electrical parameters are specified in the detail specifications. Read and record critical parameters.

2/ Parts used for one subgroup test may not be used for other subgroups, but may be used for higher levels in the same subgroup. For subgroup 2, total dose exposure shall not be considered cumulative unless testing is performed within the time limits of the test method.

3/ Not required for MOS devices unless bipolar elements are included by design.

4/ For device types with greater than 100,000 equivalent transistor per die.

5/ The test structures shall be randomly selected from the wafer. An X-ray source may be used on test structures at the wafer level provided correlation has been established between the X-ray and the Cobalt-60 source.

6/ Test to be conducted only when specified in the purchase order or contract.

7/ Latch-up testing is not required for SOS, SOI, and DI technologies when latch-up is physically not possible. Test conditions, sample size, test temperature, and the electrical parameters to be measured pre, post and during irradiation shall be specified in the acquisition document.

* 8/ SEE testing shall be performed during qualification and after any design or process change that may affect SEE response.

9/ Traceability to the specific wafer is required.

10/ Subgroups shall be invoked when RHACL specification requirements listed in table C-I are not met.

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APPENDIX C

RADIATION HARDNESS ASSURANCE (RHA)

C.1 SCOPE

* C.1.1 Scope. This appendix presents the requirements which shall be used to supplement MIL-PRF-38535 for device manufacturers supplying RHA microcircuits. This appendix is mandatory for RHA devices.

C.2 APPLICABLE DOCUMENTS

C.2.1 Government documents.

C.2.1.1 Standard. The following handbooks form a part of this specification to the extent specified herein. Unless otherwise specified, the issues of these documents shall be those listed in the issue of the Department of Defense Index of Specifications, Standards, and Handbooks (DoDISS) and supplement thereto, cited in the solicitation.

HANDBOOK

DEPARTMENT OF DEFENSE

MIL-HDBK-814 - Ionizing Dose and Neutron Hardness Assurance Guidelines for Microcircuits and Semiconductor Devices.

MIL-HDBK-815 - Dose-Rate Hardness Assurance Guidelines.

(Copies of specifications, standards, handbooks and other Government documents required by contractors in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

C.2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents which are DoD adopted are those listed in the issue of the DoDISS cited in the solicitation. Unless otherwise specified, the issues of documents not listed in the DoDISS are the issues of the documents cited in the solicitation (see C.6.2).

AMERICAN SOCIETY FOR TESTING AND MATERIALS (ASTM)

ASTM 1032 - Measuring Time-Dependent Total-Dose Effects in Semiconductor Devices Exposed to Pulse Ionizing Radiation.

* ASTM 1192 - The Measurement of Single Event Phenomena from Heavy Ion Irradiation of Semiconductor Devices

EIA/JESD 57 - Test Procedures for the Measurement of Single-Event Effects in Semiconductor Device from Heavy Ion Irradiation

(Application for copies of ASTM documents should be addressed to the American Society for Testing and Materials 100 Bar Harbor Dr, West Conshoken, PA 19428-2959. Applications for copies of EIA/JEDEC documents should be addressed to Global Engineering Documents, 15 Inverness Way East, Englewood, CO 80112-5704)

C.3 REQUIREMENTS

C.3.1 General. Microcircuits supplied to this document shall be manufactured and tested in accordance with approved baseline manufacturing flow and the requirements herein. RHA QML manufacturers shall meet all of the requirements of MIL-PRF-38535 and the additional requirements specified herein. The TRB shall not make major changes to the baselined design rules, processes, procedures, or testing without notifying the qualifying activity prior to implementation of the change.

C.3.2 TRB duties. The TRB duties shall be as outlined in G.3.2.2.

C.3.2.1 TRB/RSS. In the case of a Radiation Source of Supply (RSS) (see 6.2.23), the RSS shall establish a TRB and representatives from the device manufacturer, assembly facility, and test facility shall be part of the TRB. The RSS TRB shall be responsible for all aspects of the device manufacturing process. Details of how all aspects of the device manufacturing processes are controlled shall be documented in the RSS QM plan. These include conversion of customer requirements, design, wafer fabrication, assembly, test, RHA testing and verification, and characterization for device specification.

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* C.3.3 RHA QM plan. A RHA QM plan shall be developed to document the major elements of the manufacturer's QML process (G.3.3). This plan establishes the procedures to be followed to ensure that the devices meet the Radiation Hardness Assured Capability Level (RHACL). The RHA QM plan shall be kept current and up-to-date and reflect all major changes to the RHACL.

C.3.4 RHA/QML certification requirements. See 3.4.1 herein. In addition to standard flow certification the manufactures RHA certification testing shall be performed by a laboratory which has received suitability from the qualifying activity.

C.3.4.1 Process capability demonstration. The manufacturer shall meet the requirements in 3.4.1.1 and shall also meet the following for an RHA device. A RHACL shall be established for the environments selected by the TRB and consistently demonstrated for a technology at the specified level of electrical performance. Changes in the RHACL may require reevaluation of these capabilities by the TRB. Listed below are the radiation environments which shall be addressed:

a. Natural:

* 1. Total ionizing dose and time dependent effects for ionizing radiation (MIL-HDBK-814, ASTM 1032 and MIL-STD-883 TM1019).
2. Single-Event-Effects (SEE): Including upset, latch-up, burnout, gate rupture caused by Galactic Cosmic Rays (GCR), Solar Enhanced Particles (SEP) and energetic neutron and protons (ASTM 1192 or EIA/JESD 57).
3. Displacement damage: Caused by energetic neutrons and protons

b. Weapon:

* 1. Dose rate: Upset, latch-up, burnout (MIL-HDBK-815, MIL-STD-883 TM1020, TM1021 and TM1023).
2. Neutron irradiation (MIL-HDBK-814 and MIL-STD-883 TM1017).
3. Total ionizing dose (MIL-HDBK-814 and MIL-STD-883 TM1019).

C.3.4.1.1 Design. The manufacturer shall address the design methodology for the following areas of design:

(NOTE: These are also applicable to third party design centers.)

a. Model verification. Model Verification shall provide evidence that models defining device response in radiation environments accurately predict the nominal and worst-case circuit response over operating voltage limits and over the temperature range selected for the technology at the RHACL.

* b. Design rule verification. The vendor shall document his design rules for radiation hardening his technology and demonstrate his procedures for verifying rule compliance in the context of Design Rules Check (DRC), Electrical Rules Check (ERC) and reliability checking procedures (see G.3.1.b, G.3.4.1.c, H.3.2.1.1.b.). These rules cover, as a minimum:

1. Design Rules Check (DRC): Geometric and physical.
2. Electrical Rules Check (ERC): Shorts and open, connectivity.
3. Reliability verification: Electromigration (current density), latch-up, ESD, and fuse/anti-fuse reliability.
4. RHA rules: The vendor shall document his design rules for radiation hardening in his technology and the procedures for verifying rule compliance.

* c. Performance verification. The vendor shall demonstrate his ability to predict the response of the post-irradiation performance at the RHACL including the effects of the specified limits for temperature and voltage variations and the influence of process variations (see H.3.2.1.1.c). Any deviation from these requirements shall receive qualification activity approval.

C.3.4.1.2 Wafer fabrication. As part of certification, the manufacturer shall identify a specific technology or technologies for the wafer fabrication (see H.3.2.2).

a. SPC and in-process monitoring program for RHA. SPC is especially critical for maintaining a technology's RHACL. This occurs since relatively minor changes in a process flow can drastically effect device radiation performance. The manufacturer shall identify and document all critical process nodes associated with RHA. See H.3.2.2.1 for a general list of critical process steps, any deviation from this list shall receive qualifying activity approval.

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* b. TCV program. The TCV program is an integral part of a technology's RHA and must be carefully configured to ensure the accurate characterization of a technologies radiation capability. The TCV program shall be designed to support RHA activities, parametric extraction, model development and validation, SPC and failure mode analysis. (See H.3.2.2.2.) The TCV structures shall be used to determine a technologies RHACL and in addition determine failure modes and mechanisms by irradiation to 2x RHACL or failure, whichever comes first. Failure can be either functional or parametric.

c. TCV certification. When radiation hardness is a requirement of the technology, special structures shall be incorporated into the TCV program to characterize the technology's capability for producing devices with assured radiation hardness to the RHACL. To determine that the RHACL is appropriate for the technology, the vendor shall irradiate the TCV to 2x the RHACL or until failure to determine failure mode and mechanism(s). Also, the bounds of the radiation response shall be determined by testing the appropriate TCV test structures for worst case bias conditions, annealing conditions, and temperature.

* d. Standard Evaluation Circuit (SEC). The SEC shall utilize all relevant radiation hardness assurance design rules and shall be used to demonstrate the specified level of performance at the RHACL. When radiation hardness assurance is a requirement of the technology, the SEC shall be used to certify and monitor the RHACL of a specific fabrication technology in a specific fabrication facility. The SEC shall be designed so it can be used to assess and monitor the radiation hardness of the fabrication process and design rules (see H.3.2.2.3). The SEC reliability data, including failure analysis results, shall be available for review by the qualifying activity. For RHA environments, the manufacturer shall irradiate SEC to 2x the requested RHACL or to failure (whichever occurs first) under worst case bias, annealing and temperature conditions as a demonstration of the technology's capability to meet the RHACL. A different SEC may be required whenever the design rules, the materials, the basic processes, or the basic functionality of the technology differ.

* e. Process monitor. The Process Monitor (PM) is an integral part of a technology's RHA SPC program for in-line process monitoring. The structures must be carefully designed and configured to ensure the accurate characterization of a technology's radiation performance and capability. The PM shall support wafer acceptance testing and TCI (see H.3.2.2.4). Any deviation from this guidance shall be justified to the qualifying agency.

When RHA is a requirement of the QML line, as a minimum, process monitors for RHA qualified technologies shall include test structures to support the following:

1. MOS RHA parameters:

   (a) Gate oxide thickness; Structures shall be included to ensure gate oxide thickness since this is a critical parameter affecting radiation performance.

   (b) The following parameters shall be measured as a function of total ionizing dose:
      (1) Threshold voltage (V_T); The linear V_T for each transistor in a cell.
      (2) Linear transconductance (gm); The linear gm for a set of transistors.
      (3) I_{on}/I_{off} (leakage current).
      * (4) Propagation delay time (t_{PD}); A test structure in the form of a functional circuit such as an inverter or register chain shall be available to support this measurement.
      (5) Field transistor leakage; Field transistor leakage for the minimum design/layout rules.

* 2. Bipolar parameters. The bipolar parameters should be those found in H.3.2.2.4c and shall be measured as a function of total ionizing dose and neutron fluence (as appropriate).

* 3. GaAs parameters. The following parameters should be measured as a function of total ionizing dose and neutron/proton fluence (as appropriate).

   (a) Sheet resistance.

   (b) Isolation; An ohmic transmission line structure should be included to measure contact resistance and transfer length.

   (c) FAT FET; A long length gate FET suitable for the measurement of Schottky barrier height, ideality factor, carrier concentration, and channel depth should be available.

   (d) GaAs FET parameters; see H.3.2.2.4d.

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4. Radiation Hardness Assurance. When RHA is a requirement of the technology, the PM shall include test structures to monitor the following phenomena, as applicable:

   (a) Dose-rate latch-up.

   (b) Dose-rate upset.

   (c) Single-event effects.

   (d) Total ionizing dose.

   (e) Displacement damage from neutron or proton irradiation.

* 5. Other RHA considerations. In addition, test structures to monitor and characterize radiation response mechanisms and for linear circuit applications shall be included (as appropriate). These structures would include but not be limited to:

   (a) Matched transistor pairs for offset current and voltage characterization.

   (b) Annular and dual or multi-edged transistor sets for sub threshold I-V characterization.

   (c) Four contact devices for charge pumping measurements.

* C.3.4.1.3 Wafer acceptance plan. The TRB shall develop and demonstrate a wafer acceptance plan based on electrical and radiation measurement of parametric monitors. Parametric monitors shall be used to determine wafer and wafer lot uniformity and latch-up immunity (when specified). Further testing of the actual device to table C-I may be required. As an option to actual device testing, after initial establishment of device specification and device Post-Irradiation Parameter Limits (PIPL), the following procedures are presented as examples for the specified radiation environments:

1. Latch-up: The parametric monitor should utilize worst case latch-up structures to determine latch-up holding voltage at maximum temperature. The holding voltage must be greater than the maximum rated voltage.
2. SEE: The parametric monitor should utilize SEE structures such as cross-coupling resistors to memory cells to assure critical parameters agree with worst case acceptance criteria.
3. Dose rate: The parametric monitor should utilize structures to ensure rail span collapse does not cause upset or burnout or both and that the metallization resistivity, contact resistance, via resistance, epi, substrate resistivity and minority carrier lifetime specifications are met.
4. Total ionizing dose: The parametric monitor should utilize structures such as capacitors and transistors to ensure that critical parameters agree with worst case PIPL values.

C.3.5 On-site validation. In addition to the requirements in 3.4.1.3 the on-site validation shall include RHA test procedures and RHA data reduction.

C.3.5.1 Technology validation. The general requirements for a technology validation are defined in 3.4.1.4. For RHA technology the following items shall be added:

a. Radiation test procedures.

b. RHA data reduction (e.g., interface state and oxide trapped charge separation).

C.3.6 RHA packages. Packages used for RHA microcircuits shall be characterized for effects which may influence the hardness of packaged product. Characterization shall include impedance of the power and ground distribution network, impedance contributions of bond wires and die attach, and the impedance associated with any passive elements included as integral parts of the package. Qualification of the same die in different packages shall require demonstration either by test or similarity analysis.

* C.3.7 Demonstration vehicles. The demonstration vehicles shall be as described in H.3.4.1. Each demonstration vehicle shall operate and perform in compliance with the device specification and to the RHACL for a radiation hardened process (which must be submitted to the qualifying activity) and shall be manufactured in packages which have been tested to C.3.6 herein prior to use for qualification. For a technology which has die as its primary product, the demonstration vehicle shall be suitably packaged to allow evaluation of the technology without adversely affecting the outcome of the tests.

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* C.3.7.1 Qualification test plan. See H.3.4.2. Note that for RHA the die traceability shall be to the individual wafer.

* C.3.7.2 Qualification test report. For RHA testing, the pre and post irradiation, electrical parameters and the transient and SEE test conditions shall be retained by the manufacturer.

C.4 VERIFICATION

C.4.1 Traceability. Traceability to the wafer lot level (for GaAs to wafer level) shall be provided for all delivered microcircuits. Traceability shall document, as a minimum, the completion of each step required in design (when applicable), fabrication, assembly, test and any applicable qualified rework procedure.

* C.4.2 Design requirements. The manufacturer shall show evidence that all QML/RHA product has been through the qualified RHA technology flow. For RHA devices, sample testing of each design to verify PIPL shall be conducted to determine total dose and neutron hardness level, dose rate upset threshold, latch-up immunity (when specified) at maximum temperature and voltage, and linear energy transfer threshold (LET_{TH}) for upset and latch-up as well as the cross section for SEE. If simulation models can be verified by test to address these concerns, they would be acceptable. It is anticipated that several designs of each ASIC family will be tested.

* C.4.3 Radiation response characterization. When specified in the acquisition document, radiation response characterization data shall be provided for QML microcircuits in those environments specified in the device specification. The characterization shall be obtained in increments of irradiation levels to failure or to a radiation level at or beyond the specification level as determined by the TRB. The characterization data shall be accompanied by the mean and standard deviation of the critical parameters. The results obtained from table C-I testing herein shall be added to the characterization data (at fluence level, dose rate, and parameter levels defined in the device procurement specification test conditions) periodically.

* C.4.4 End-of-line Technology Conformance Inspection (TCI) testing (option 1). Group E inspection shall include radiation hardness assurance tests on each wafer lot. The PIPL, transient and SEP response (as applicable), and test conditions shall be as specified in the device specification. End-of-line TCI testing shall be performed as recommended in table J-I herein. Requirements as detailed in MIL-STD-883 method 5005 may be used, with qualifying activity approval, in place of the TCI requirements herein. All group E testing shall be performed on microcircuits to be delivered as RHA QML microcircuits.

Group E inspection is required only for parts intended to be marked as radiation hardness assured. RHA quality conformance inspection sample tests shall be performed at the level(s) specified and in accordance with table C-I herein. The applicable subgroups of group E shall be performed when specified in the acquisition document. The actual devices used for group E testing shall be assembled in a qualified package and, as a minimum, shall pass group A, subgroups 1, 7, and 9 at +25°C prior to irradiation. If a manufacturer elects to eliminate a quality conformance inspection step by substituting an in-process control or statistical process control procedure, the manufacturer is only relieved of the responsibility of performing the TCI operation associated with that step. The manufacturer is still responsible for providing a product which meets all of the performance, quality, and reliability requirements herein and in the device specification. Documentation supporting substitution for TCI shall be retained by the manufacturer and available to the qualifying activity upon request. For some devices, there are differences in the total dose radiation response before and after burn-in. Unless it has been shown by prior characterization or by design that burn-in has negligible effect (parameters remain within postirradiation specified electrical limits) on the total dose radiation response, then one of the following must be done:

a. The manufacturer shall subject the radiation samples to the specified burn-in conditions prior to conducting total dose radiation testing.

b. The manufacturer shall develop a correction factor (which is acceptable to the parties to the test) taking into account the changes in total dose response resulting from subjecting product to burn-in. The correction factor shall then be used to accept product for total dose response without subjecting the test samples to burn-in.

C.4.4.1 End-point tests for group E . End-point measurements and other specified post-test measurements shall be made for each sample after completion of all other specified tests in the subgroup. The test limits for the end-point measurements shall be the same as the test limits for the respective group A subgroup inspections. Different end-points may be specified for group E tests in the detailed specifications. Any additional end-point electrical measurements may be performed at the discretion of the manufacturer.

* C.4.5 In-line TCI testing (option 2). In-line control testing shall be performed through the use of the approved SEC or QML microcircuit. The following shall be addressed for RHA devices; group E testing shall be performed on the SEC or product meeting SEC complexity at intervals set by the TRB in the QM plan. Burn-in shall be addressed as per C.4.4a or C.4.4b above.

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* TABLE C-I. Group E (RHA testing) Class Q. 1/

TEST	MIL-STD-883		RHACL/SPEC	Quantity 3/
	Method	Condition	2/	(accept no.)
Subgroup 1				
Neutron 4/ irradiation	1017	+25°C	> 10 > 1 ≤ 10	No testing required 2(0) devices/wafer 5(0) devices/wafer lot
End-point electrical parameters		As specified in the applicable device specification		11(0) devices/inspection lot 5/
Subgroup 2				
Total ionizing radiation dose	1019	+25°C	> 10 > 1 ≤ 10	No testing required 2(0) devices/wafer 5(0) devices/wafer lot
End-point electrical parameters		As specified in the applicable device specification		22(0) devices/inspection lot 6/
Single event effects	EIA/JESD 57 or ASTM 1192	+25°C		4/

1/ Parts used for one subgroup test may not be used for other subgroups but may be used for higher levels in the same subgroup. Total dose exposure shall not be considered cumulative unless testing is performed within the time limits of the test method. For Class V level product see Table B-1.

2/ The RHACL/SPEC is the ratio of the capability level to the specification level of fluence.

3/ Per wafer lot. Alternatively, each wafer may be accepted on a 2(0) quantity (accept) number. If the alternate is chosen, a PDA of 10 percent or equivalent shall apply to the lot.

* 4/ Test to be conducted only when specified in the purchase order or contract.

* 5/ In accordance with inspection lot. If one part fails, 16 additional parts may be added to the test sample with no additional failures allowed, 27(1).

* 6/ In accordance with inspection lot. If one part fails, 16 additional parts may be added to the test sample with no additional failures allowed, 38(1).

C.5 NOTES.
(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory.)

C.5.1 Supporting documents. The documents in this section may be used as guidelines for the development of a hardness assurance program and are not mandatory for this specification.

C.5.1.1 Government specification, standards and handbooks:

MIL-PRF-38534 General Specification for Hybrid Microcircuits.

MIL-STD-1546 Parts, Materials and Processes Control Program for Spacecraft and Launch Vehicles.

MIL-STD-1547 Technical Requirements for Electronic Parts, Materials, and Processes for Space and Launch vehicles.

MIL-HDBK-179 Microcircuit Applications Handbook.

* MIL-HDBK-816 Guideline for Developing a Radiation Hardness Assured Device Specification.

MIL-HDBK-817 System Development Radiation Hardness Assurance.

(Copies of specifications, standards, and other Government documents required by contractors in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

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C.5.1.2 Non-Government specifications, standards, and guidelines:

AMERICAN SOCIETY FOR TESTING AND MATERIALS (ASTM)

ASTM E665 Standard Practice for Determining Absorbed Dose Versus Depth in Materials Exposed to the X-Ray Output of Flash X-Ray Machines.

ASTM E666 Standard Practice for Calculating Absorbed Dose from Gamma or X Radiation.

ASTM E668 Standard Practice for the Application of Thermoluminescence-Dosimetry (TLD) Systems for Determining Absorbed Dose in Radiation-Hardness Testing of Electronic Devices.

ASTM F744 Standard Test Method for Measuring Dose Rate Threshold for Upset of Digital Integrated Circuits.

ASTM F773 Standard Practice for Measuring Dose Rate Response of Linear Integrated Circuits.

(Application for copies should be addressed to the American Society for Testing and Materials, 1916 Race Street, Philadelphia, PA 19103-1187.)

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APPENDIX D

STATISTICAL SAMPLING, TEST AND INSPECTION PROCEDURES

D.1 SCOPE

D.1.1 Scope. This appendix contains statistical sampling, life test and qualification procedures used with microcircuits.

D.2 APPLICABLE DOCUMENTS

(This section is not applicable to this appendix.)

* D.3 REQUIREMENTS

D.3.1 Definitions. The following definitions shall apply for all statistical sampling procedures:

a. Sample size series: The sample size series is defined as the following decreasing series of values: 50, 30, 20, 15, 10, 7, 5, 3, 2, 1.5, 1, 0.7, 0.5, 0.3, 0.2, 0.15, and 0.1.

b. Tightened inspection: Tightened inspection is defined as inspection performed using the next sample size value in the sample size series lower than that specified.

c. Acceptance number (c): The acceptance number is defined as an integral number associated with the selected sample size which determines the maximum number of defectives permitted for that sample size.

d. Rejection number (r): Rejection number is defined as one plus the acceptance number.

D.3.2 Symbols. The following symbols shall apply for all statistical sampling procedures:

a. c: Acceptance number.

b. r: Rejection number.

D.4 STATISTICAL SAMPLING PROCEDURES AND TABLE

D.4.1 General. Statistical sampling shall be conducted using the sample size method. The sample size method as specified herein is a sampling plan which provides a high degree of assurance that a lot having a percent defective greater than or equal to the specified sample size value will not be accepted. The procedures specified herein are suitable for all quality conformance requirements.

D.4.1.1 Selection of samples. Samples shall be randomly selected from the inspection lot or inspection sublots. For continuous production, the manufacturer, at his option, may select the sample in a regular periodic manner during manufacture provided the lot meets the formation of lots requirement.

D.4.1.2 Failures. Failure of a unit for one or more tests of a subgroup shall be charged as a single failure.

D.4.2 Single-lot sampling method. Quality conformance inspection information (sample sizes and number of observed defectives) shall be accumulated from a single inspection lot to demonstrate conformance to the individual subgroup criteria.

D.4.2.1 Sample size. The sample size for each subgroup shall be determined from table D-I or D-II and shall meet the specified sample size series. The manufacturer may, at his option, select a sample size greater than that required; however, the number of failures permitted shall not exceed the acceptance number associated with the chosen sample size in table D-I or D-II. In table D-II, the sample size series column to be used for sample size determination shall be that given in the lot size column which is nearest in value of the actual size of the submitted lot, except that if the actual lot size is midway between two of the lot sizes given in the table, either of the bounding lot size columns may be used at the manufacturer's option. If, in table D-II, the appropriate lot size column does not contain a sample size series value equal to or less than the specified sample size series value, 100 percent inspection shall be used. In table D-II, the sample size series value in the appropriate lot size column which is numerically closest to the specified sample size series value shall be used to determine the sample size.

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D.4.2.2 Acceptance procedure. For the first sampling, an acceptance number shall be chosen and the associated number of sample devices for the specified sample series selected and tested (see D.4.2.1). If the observed number of defectives from the first sample is less than or equal to the preselected acceptance number, the lot shall be accepted. If the observed number of defectives exceeds the preselected acceptance number, an additional sample may be chosen such that the total sample complies with D.4.2.3. The table (D-I or D-II), which is used for the first sampling of a given inspection lot for a given subgroup shall be used for any and all subsequent samplings for the same lot and subgroup for each lot submission.

D.4.2.3 Additional sample. The manufacturer may add an additional quantity to the initial sample, but this may be done only once for any subgroup and is limited to the initial sample (i.e., does not apply to resubmitted lots after initial failure). The added samples shall be subjected to all the tests within the subgroup. The total sample size (initial and added samples) shall be determined by a new acceptance number selected from table D-I or D-II).

D.4.2.4 Multiple criteria. When one sample is used for more than one acceptance criterion, the entire sample for a subgroup shall be used for all criteria within the subgroup. In table D-I, the acceptance number shall be that one associated with the largest sample size in the appropriate sample size series column which is less than or equal to the sample size used. In table D-II, the acceptance number shall be that one associated with the specified samples size series, in the appropriate lot size column, for the sample size used.

D.4.2.5 One hundred percent inspection. Inspection of 100 percent of the lot shall be allowed, at the option of the manufacturer, for any or all subgroups other than those which are called "destructive". If the observed percent defective for the inspection lot exceeds the specified samples size series value, the lot shall be considered to have failed the appropriate subgroup(s). Resubmission of lots tested on a 100 percent inspection basis shall also be on a 100 percent inspection basis only and in accordance with the tightened inspection sample series value and other requirements of A.4.3.3.1.

D.4.2.6 Tightened inspection. Tightened inspection shall be performed by testing to the criteria of the next sample size series value lower than that specified in the series 1, 1.5, 2, 3, 5, and 7 times 10^n, where n is an integral number.

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TABLE D-I. Sample size series sampling plan - 1/ 2/ 3/

Maximum percent defective (sample size series)	50	30	20	15	10	7	5	3	2	1.5	1	0.7	0.5	0.3	0.2	0.15	0.1
Acceptance number (C) (r = c + 1)	Minimum sample sizes (For device-hours required for life test, multiply by 1000)																
0	5 (1.03)	8 (0.64)	11 (0.46)	15 (0.34)	22 (0.23)	32 (0.16)	45 (0.11)	76 (0.07)	116 (0.04)	153 (0.03)	231 (0.02)	328 (0.02)	461 (0.01)	767 (0.007)	1152 (0.005)	1534 (0.003)	2303 (0.002)
1	8 (4.4)	13 (2.7)	18 (2.0)	25 (1.4)	38 (0.94)	55 (0.65)	77 (0.46)	129 (0.28)	195 (0.18)	258 (0.14)	390 (0.09)	555 (0.06)	778 (0.45)	1296 (0.027)	1946 (0.018)	2592 (0.013)	3891 (0.009)
2	11 (7.4)	18 (4.5)	25 (3.4)	34 (2.24)	52 (1.6)	75 (1.1)	105 (0.78)	176 (0.46)	266 (0.31)	354 (0.23)	533 (0.15)	759 (7.59)	1065 (0.080)	1773 (0.045)	2662 (0.031)	3547 (0.022)	5323 (0.015)
3	13 (10.5)	22 (6.2)	32 (4.4)	43 (3.2)	65 (2.1)	94 (1.5)	132 (1.0)	221 (0.62)	333 (0.41)	444 (0.31)	668 (0.20)	953 (0.14)	1337 (0.10)	2226 (0.062)	3341 (0.041)	4452 (0.031)	6681 (0.018)
4	16 (12.3)	27 (7.3)	38 (5.3)	52 (3.9)	78 (2.6)	113 (1.8)	158 (1.3)	265 (0.75)	398 (0.50)	531 (0.37)	798 (0.25)	1140 (0.17)	1599 (0.12)	2663 (0.074)	3997 (0.049)	5327 (0.037)	7994 (0.025)
5	19 (13.6)	31 (8.4)	45 (6.0)	60 (4.4)	91 (2.9)	131 (2.0)	184 (1.4)	308 (0.85)	462 (0.57)	617 (0.42)	927 (0.28)	1323 (0.20)	1855 (0.14)	3090 (0.085)	4638 (0.056)	6181 (0.042)	9275 (0.028)
6	21 (15.6)	35 (9.4)	51 (6.6)	68 (4.9)	104 (3.2)	149 (2.2)	209 (1.6)	349 (0.94)	528 (0.62)	700 (0.47)	1054 (0.31)	1503 (0.22)	2107 (0.155)	3509 (0.093)	5267 (0.062)	7019 (0.047)	10533 (0.031)
7	24 (16.6)	39 (10.2)	51 (7.2)	77 (5.3)	116 (3.5)	166 (2.4)	234 (1.7)	390 (1.0)	589 (0.67)	783 (0.51)	1178 (0.34)	1680 (0.24)	2355 (0.17)	3922 (0.101)	5886 (0.067)	7845 (0.051)	11771 (0.034)
8	26 (18.1)	43 (10.9)	63 (7.7)	85 (5.6)	128 (3.7)	184 (2.6)	258 (1.8)	431 (1.1)	648 (0.72)	864 (0.54)	1300 (0.36)	1854 (0.25)	2599 (0.18)	4329 (0.108)	6498 (0.072)	8660 (0.054)	12995 (0.036)
9	28 (19.4)	47 (11.5)	69 (8.1)	93 (6.0)	140 (3.9)	201 (2.7)	282 (1.9)	471 (1.2)	709 (0.77)	945 (0.58)	1421 (0.38)	2027 (0.27)	2842 (0.19)	4733 (0.114)	7103 (0.077)	9468 (0.057)	14206 (0.038)
10	31 (19.9)	51 (12.1)	75 (8.4)	100 (6.3)	152 (4.1)	218 (2.9)	306 (2.0)	511 (1.2)	770 (0.80)	1025 (0.60)	1541 (0.40)	2199 (0.28)	3082 (0.20)	5133 (0.120)	7704 (0.080)	10268 (0.060)	15407 (0.040)
11	33 (21.0)	54 (12.8)	83 (8.3)	111 (6.2)	166 (4.2)	238 (2.9)	332 (2.1)	555 (1.2)	832 (0.83)	1109 (0.62)	1664 (0.42)	2378 (0.29)	3323 (0.21)	5546 (0.12)	8319 (0.083)	11092 (0.062)	16638 (0.042)
12	36 (21.4)	59 (13.0)	89 (8.6)	119 (6.5)	178 (4.3)	254 (3.0)	356 (2.2)	594 (1.3)	890 (0.86)	1187 (0.65)	1781 (0.43)	2544 (0.3)	3562 (0.22)	5936 (0.13)	9804 (0.086)	11872 (0.065)	17808 (0.043)
13	38 (22.3)	63 (13.4)	95 (8.9)	126 (6.7)	190 (4.5)	271 (3.1)	379 (2.26)	632 (1.3)	948 (0.89)	1264 (0.67)	1896 (0.44)	2709 (0.31)	3793 (0.22)	6321 (0.134)	9482 (0.089)	12643 (0.067)	18964 (0.045)
14	40 (23.1)	67 (13.8)	101 (9.2)	134 (6.9)	201 (4.6)	288 (3.2)	403 (2.3)	672 (1.4)	1007 (0.92)	1343 (0.69)	2015 (0.46)	2878 (0.32)	4029 (0.23)	6716 (0.138)	10073 (0.092)	13431 (0.069)	20146 (0.046)
15	43 (23.3)	71 (14.1)	107 (9.4)	142 (7.1)	213 (4.7)	305 (3.3)	426 (2.36)	711 (1.41)	1086 (0.94)	1422 (0.71)	2133 (0.46)	3046 (0.33)	4265 (0.235)	7108 (0.141)	10662 (0.094)	14216 (0.070)	21324 (0.047)
16	45 (24.1)	74 (14.6)	112 (9.7)	150 (7.2)	225 (4.8)	321 (3.37)	450 (2.41)	750 (1.44)	1124 (0.96)	1499 (0.72)	2249 (0.48)	3212 (0.337)	4497 (0.241)	7496 (0.144)	11244 (0.096)	14992 (0.072)	22487 (0.048)
17	47 (24.7)	79 (14.7)	118 (9.86)	158 (7.36)	236 (4.93)	338 (3.44)	473 (2.46)	788 (1.48)	1182 (0.98)	1576 (0.74)	2364 (0.49)	3377 (0.344)	4728 (0.246)	7880 (0.148)	11819 (0.098)	15759 (0.074)	23639 (0.049)
18	50 (24.9)	83 (15.0)	124 (10.0)	165 (7.54)	248 (5.02)	354 (3.51)	496 (4.96)	826 (1.5)	1239 (1.0)	1652 (0.75)	2478 (0.50)	3540 (0.351)	4956 (0.251)	8260 (0.151)	12390 (0.100)	16520 (0.075)	24780 (0.050)
19	52 (25.5)	86 (15.4)	130 (10.2)	173 (7.76)	259 (5.12)	370 (3.58)	518 (2.56)	864 (1.53)	1296 (1.02)	1728 (0.77)	2591 (0.52)	3702 (0.358)	5183 (0.256)	8638 (0.153)	12957 (0.102)	17276 (0.077)	25914 (0.051)
20	54 (26.1)	90 (15.6)	135 (10.4)	180 (7.82)	271 (5.19)	386 (3.65)	541 (2.60)	902 (1.56)	1353 (1.04)	1803 (0.78)	2705 (0.52)	3864 (0.364)	5410 (0.260)	9017 (0.156)	13526 (0.104)	18034 (0.078)	27051 (0.052)
25	65 (27.0)	109 (16.1)	163 (10.8)	217 (8.08)	326 (5.38)	466 (3.76)	652 (2.69)	1086 (1.61)	1629 (1.08)	2173 (0.807)	3259 (0.538)	4656 (0.376)	6518 (0.269)	10863 (0.161)	16295 (0.108)	21726 (0.081)	32589 (0.054)

1/ Sample sizes are based upon the poisson exponential binomial limit.
2/ The minimum quality (approximate AQL) required to accept (on the average) 19 of 20 lots is shown in parenthesis for information only.
3/ Minimum size of sample to be tested to assure with a 90 percent confidence that a lot having percent-defective equal to the specified sample size series value will not be accepted (single sample).

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TABLE D-II. Hypergeometric sampling plans for small lot sizes of 200 or less.

(N = lot size, n = sample size, c = acceptance number).

C = 0

N	10		20		30		40		50		60		80		100		120		150		160		200	
n	AQL	SSS	AQL	SSS	AQL	SSS	AQL	SSS	AQL	SSS	AQL	SSS	AQL	SSS	AQL	SSS	AQL	SSS	AQL	SSS	AQL	SSS	AQL	SSS
2	2.2	85	2.5	86	2.5	67	2.5	67	2.5	67	2.5	68	2.5	68	2.5	68	2.5	68	2.5	68	2.5	68	2.5	68
4	1.2	36	1.2	40	1.2	42	1.2	42	1.3	42	1.3	43	1.3	43	1.3	43	1.3	43	1.3	43	1.3	44	1.3	44
5	1.0	29	1.0	43	1.0	34	1.0	35	1.0	35	1.0	35	1.0	36	1.0	36	1.0	37	1.0	37	1.0	37	1.0	37
8	0.5	15	0.6	20	0.6	22	0.6	23	0.6	23	0.6	23	0.6	24	0.7	24	0.7	24	0.7	24	0.7	24	0.7	25
10			0.4	15	0.5	17	0.5	19	0.5	19	0.5	19	0.5	20	0.5	20	0.5	20	0.5	20	0.5	20	0.5	20
16			0.2	6.9	0.25	10	0.25	11	0.3	11	0.3	12	0.3	12	0.3	13	0.3	13	0.3	13	0.3	13	0.3	13
20					0.2	6.8	0.2	8.0	0.25	8.7	0.25	9.0	0.25	9.4	0.25	10	0.25	10	0.25	10	0.25	10	0.25	11
25					0.15	4.3	0.15	3.7	0.2	6.4	0.2	6.9	0.2	7.4	0.2	7.5	0.2	7.6	0.2	7.7	0.2	7.8	0.2	7.9
32							0.1	3.7	0.1	4.4	0.1	5.0	0.1	5.5	0.1	5.9	0.15	6.0	0.15	6.2	0.15	6.3	0.15	6.3
40									0.1	3.0	0.1	3.4	0.1	4.0	0.1	4.5	0.1	4.6	0.1	4.9	0.1	5.0	0.1	5.0
50											0.1	2.3	0.1	2.9	0.10	3.3	0.1	3.5	0.10	3.7	0.1	3.7	0.10	3.9
64													0.08	1.7	0.08	2.2	0.06	2.5	0.06	2.7	0.06	2.8	0.06	2.9
80															0.07	1.5	0.07	1.7	0.07	2.0	0.07	2.1	0.07	2.2
100																	0.05	1.1	0.05	1.5	0.05	1.5	0.05	1.7
125																			0.04	0.8	0.04	0.9	0.04	1.2
128																			0.04	0.8	0.04	0.9	0.04	1.1
160																							0.03	0.7

C = 1

N	10		20		30		40		50		60		80		100		120		150		160		200	
n	AQL	SSS	AQL	SSS	AQL	SSS	AQL	SSS	AQL	SSS	AQL	SSS	AQL	SSS	AQL	SSS	AQL	SSS	AQL	SSS	AQL	SSS	AQL	SSS
2	27	95	24	95	24	95	23	95	23	95	23	95	23	95	23	95	23	95	22	95	22	95	22	95
4	15	62	12	66	12	66	11	67	11	67	10	67	10	67	10	67	10	67	9.8	67	9.7	67	9.7	68
5	13	51	10	55	8.8	56	8.5	57	8.4	57	8.1	58	7.9	58	7.6	58	7.5	58	7.5	58	7.5	58	7.5	58
8	11	28	7.2	35	6.2	38	5.8	38	5.4	39	5.0	39	4.7	39	4.5	39	4.3	39	4.3	40	4.2	40	4.2	40
10			6.2	30	5.0	30	4.6	31	4.2	32	4.2	22	4.2	32	3.9	32	3.5	33	3.3	33	3.3	33	3.3	33
16			5.6	15	4.2	18	3.8	18	3.4	20	3.0	20	2.9	21	2.6	21	2.5	21	2.3	21	2.3	22	2.2	22
20					4.0	13	3.2	15	2.8	16	2.5	16	2.4	16	2.3	16	2.1	17	2.0	17	2.0	17	2.0	18
25					3.8	9.2	3.1	11 3.1	2.5	12 2.4	2.2	13	2.0	13	1.8	13	1.7	13 1.5	1.6	14 1.4	1.6	14 1.3	1.6	14 1.3
32							7.4		8.2		2.1	9.0	1.8	9.9	1.6	10	10.5		11		11		11	1.1
40									2.4	5.9	2.1	6.8	1.6	7.8	1.4	7.8	1.3	8.2	1.2	8.3	1.2	8.4	8.6	
50											1.7	4.6	1.4	5.6	1.2	6.1	1.2	6.4	1.0	6.5	0.9	6.7	0.9	6.7
64													1.3	3.8	1.1	4.4	1.0	4.7	0.8	5.0	0.8	5.0	0.7	5.2
80															1.1	3.0	1.0	3.4	0.8	3.7	0.7	3.8	0.6	4.0
100																	0.9	2.5	0.7	2.8	0.7	2.8	0.6	3.0
125																			0.7	1.9	0.7	2.0	0.5	2.2
128																			0.7	1.7	0.7	1.9	0.5	2.2
160																							0.5	1.5

C = 2

N	10		20		30		40		50		60		80		100		120		150		160		200	
n	AQL	SSS	AQL	SSS	AQL	SSS	AQL	SSS	AQL	SSS	AQL	SSS	AQL	SSS	AQL	SSS	AQL	SSS	AQL	SSS	AQL	SSS	AQL	SSS
4	33	82	28	83	27	84	27	85	27	85	26	85	26	85	26	86	26	86	25	86	25	86	25	86
5	27	69	23	73	21	74	20	74	20	74	20	75	20	75	19	75	19	75	19	75	19	75	19	75
8	22	42	15	49	14	49	13	52	13	52	13	52	12	53	12	53	12	53	11	53	11	53	11	53
10			13	39	11	42	11	42	10	43	10	43	9.6	43	9.2	44	9.1	44	8.9	44	8.9	44	8.7	44
16			11	12	8.6	25	6.9	27	6.8	27	6.4	27	6.0	28	6.0	29	5.9	29	5.9	29	5.7	29	5.5	30
20					7.7	19	6.2	21	5.9	22	5.6	22	5.1	23	4.8	23	4.8	23	4.6	23	4.5	24	4.5	24
25					7.4	13	6.0	16	4.9	17	4.5	17	4.3	18	4.1	18	3.9	18	3.7	18	3.7	19	3.7	19
32							5.5	11	4.8	12	4.3	13	3.6	14	3.4	14	3.2	14	3.0	14.5	3.0	15	2.9	15
40									4.6	8.9	3.9	9.8	3.1	11	2.8	12	2.6	12	2.4	12	2.4	12	2.3	12
50											3.5	6.9	2.8	8.1	2.4	8.4	2.3	8.6	2.1	9.0	2.1	9.3	2.0	9.5
64													2.6	5.7	2.2	6.2	2.0	6.6	1.8	7.1	1.7	7.1	1.6	7.4
80															2.1	4.5	1.8	4.9	1.6	5.4	1.5	5.4	1.4	5.6
100																	1.8	3.5	1.4	3.9	1.4	4.0	1.2	4.4
125																			1.4	2.8	1.3	2.9	1.1	3.3
128																			1.4	2.6	1.3	2.9	1.1	2.2
160																							1.1	2.3

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APPENDIX D

TABLE D-II. Hypergeometric sampling plans for small lot sizes of 200 or less - Continued.

Table D-II gives the AQL and Sample Size Series (SSS) values associated with certain single sampling plans (acceptance number, sample size, and lot size). The table has the following features:

a. Calculation are based upon the hypergeometric distribution (exact theory) for lot sizes 200 or less.

b. The AQL of a sampling plan is defined as the interpolated percent defective for which there is a 0.95 probability of acceptance under the plan. The AQL so defined need not be a realizable lot percent defective for the lot size involved (e.g., 12 percent is not a realizable percent defective for a lot size of 20).

c. The sample size series of a sampling plan is defined as the interpolated percent defective for which there is a 0.10 probability of lot acceptance under the plan. The sample size series value so defined need not be a realizable lot percent defective for the lot size involved.

d. The sequence of sample sizes and lot sizes are generated by taking products of preceding numbers in the respective sequences.

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APPENDIX E

PROVISIONS GOVERNING THE CERTIFICATION AND QUALIFICATION
OF OFFSHORE PROCESSES

E.1 SCOPE

E.1.1 Scope. The following extension procedures should be used when a manufacturer having qualification under MIL-PRF-38535 decides to perform selected operations at an offshore site. The provisions of this appendix do not require a ratified international standardization agreement. This appendix is provided as guidance whenever a manufacturer requests an extension of certification and qualification to an offshore site.

E.1.2 Eligibility. To be eligible for an extension of certification and qualification to an offshore site, a manufacturer must first qualify those operations and facilities. The QML listed manufacturer must demonstrate sufficient control of the offshore site(s) to the qualifying activity to assure compliance to all provisions of this document.

E.2 APPLICABLE DOCUMENTS. This section is not applicable to this appendix.

* E.3 REQUIREMENTS.

E.3.1 Basic plant. The basic plant is the QML listed plant(s) that assumes full responsibility for the offshore site as specified in E.3.2. The basic plant should control the offshore operations to assure they continuously meet the baseline assembly and test flows.

E.3.2 Offshore site(s). Offshore site(s) are facilities outside the U.S. or its territories. The offshore operation should not deviate from the flow and test procedures as required by this document and approved by the basic plant. The location of the site(s) should be included on the QML. No offshore device should be marked with a QML quality certification mark until approval for listing on QML has been granted.

E.3.3 Material to be submitted. The following information concerning the use and the quality control operations of offshore site(s) should be furnished to the qualifying activity:

a. A quality management plan outlining the offshore site flow/procedure.

b. Procedures on how the TRB/basic plant will assure proper oversight of these site(s). Notification of the qualifying activity that demonstrates the TRB/basic plant is monitoring their offshore activities for changes in the offshore operations is required during the normal TRB reporting cycle or in another manner deemed appropriate by the qualifying activity.

c. Organization charts showing management, quality control, and production relationships between the basic plant and the offshore site(s).

d. List of selected screening and TCI test procedures to be performed at the offshore sites as the qualifying activity deems appropriate.

e. A statement by a responsible company official showing the degree of ownership (i.e., corporate or other) and control by the basic plant.

f. A copy of a self audit report approved by the TRB/basic plant, verifying that the facilities have been found acceptable and that all the information and material furnished to the qualifying activity is complete and accurate.

g. A corporate plan that shows the TRB/basic plant has considered and developed a contingency plan to handle potential disruptions to the offshore operations. The plan should consider such things as how the basic plant will ramp up production in another site, the time delayed and the resultant impact to the military and commercial customer base. Based upon the above information and the manufacturer's site(s) current status in the QML program, the qualifying activity in conjunction with the TRB/basic plant will determine what is needed to complete the certification and qualification actions.

E.3.4 Nonapproved plants. Products manufactured at any site(s) location other than the ones approved by the qualifying activity, TRB/basic plant for listing on the QML are not in accordance with the qualification terms specified herein and, therefore, are not considered qualified products and may not be marked or sold as such.

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APPENDIX F

GENERAL PROVISIONS FOR TAPE AUTOMATED BONDED (TAB) MICROCIRCUITS

F.1 SCOPE

F.1.1 Scope. This appendix contains provisions for Tape Automated Bonded (TAB) microcircuits. It provides design guidelines, in-process controls, screening and TCI requirements, and general manufacturing guidelines in order to produce a compliant TAB microcircuit. It is intended for use in conjunction with a manufacturer's compliancy program.

F.2 APPLICABLE DOCUMENTS

F.2.1 Non-Government publications. The following documents form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents which are DoD adopted are those listed in the issue of the DoDISS cited in the solicitation. Unless otherwise specified, the issues of documents not listed in the DoDISS are the issues of the documents cited in the solicitation.

ELECTRONIC INDUSTRIES ASSOCIATION (EIA)

JEDEC STD 22 TM A101 - Steady-state Temperature Humidity Bias Life Test.
JEDEC STD 22 TM A112 - Highly Accelerated Temperature and Humidity Stress Test.
JEDEC Pub 95-US-001 - TAB Package Family (Metric).
JEDEC Pub 95-CO-009 - TAB Carrier Outline.

(Application for copies should be addressed to the Electronic Industries Association, 2500 Wilson Boulevard, Arlington, VA 22201-3834.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

F.2.2 Order of precedence. In the event of a conflict between the text of this appendix and the references cited herein (except for associated detail specifications), the text of this appendix shall take precedence. Nothing in this appendix, however, shall supersede applicable laws and regulations unless a specific exemption has been obtained.

* F.3 REQUIREMENTS

* F.3.1 Marking. Marking shall be in accordance with the device specification and in an appropriate medium. The following should be used as guidance: Marking may be in ink, laser marked or etched in the copper of the lead frame tape. Ink-marking may be performed before or after burn-in. Ink-marked parts shall be subjected to resistance to solvents (MIL-STD-883, test method 2015, (see F.4.7.2.1 herein)). In either the ink-marked or tape design case, the following should be included on each device:

a. On the excised portion of the tape (that portion which remains with the microcircuit):

(1) Name of manufacturer or CAGE code.
(2) Inspection lot date code (determined by the date of final assembly operation, such as date of encapsulation or date of bonding operation.

b. The following should also be marked on each device, but location may be on the non-excised portion of the tape, the individual device carrier, or the excised portion of the tape at the manufacturers option:

(1) PIN.
(2) ESD identifier.
(3) Compliance indicator or certification, whichever is applicable.
(4) Serialization, if applicable.

F.3.2 Process monitors. The applicable process monitors of see A.3.4.1.2 shall be performed. The quality assurance provisions described below within this appendix will be used to address some of these process monitors.

* F.3.3 Lead finish. Lead finish shall be gold, designated a "C", unless otherwise specified in the device specification.

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* F.3.4 Item requirements. The individual item requirements for TAB microcircuits delivered under this appendix shall be documented in the device specification prepared in accordance with 3.5 of this document.

F.4. QUALITY ASSURANCE PROVISIONS

F.4.1 General operation flow. The following represents the general operational flow that TAB microcircuits follow.

Reference paragraph	Operation
F.4.6.1	Internal visual (optional)
F.4.3	Bump (100 percent)
F.4.3.1	Bump visual
F.4.4	Inner Lead Bond (ILB) (100 percent)
F.4.4	Inner Lead Bond (ILB) Visual
F.4.6.2	Internal visual (100 percent)
F.4.5	Encapsulant (optional)
F.4.5.1	Encapsulant visual
F.4.6.3	Temperature cycle (100 percent)
F.3.1	Mark (100 percent)
F.4.6.4	Pre burn-in electrical (optional)
F.4.6.4	Burn-in (100 percent)
F.4.6.4	Post burn-in electrical (100 percent)
F.4.6.5	PDA
F.4.6.6	External visual (100 percent)
F.4.7	Quality conformance inspection

F.4.2 Tape. Procurement of tape shall be baselined by the manufacturer to include the following items a - f. Items e and f shall be sampled on a frequency basis necessary to demonstrate process control.

a. Design configuration.

b. Tape composition.

c. Coefficient of thermal expansion.

d. Test for delamination of layers.

e. Plating thickness and composition.

f. Dimensions (lead, terminal, external, and window).

F.4.3 Bump. The bump process shall be baselined by the manufacturer to include the following items a - j. Items f - j shall be sampled on a frequency basis necessary to demonstrate process control.

a. Minimum glassivation overlap.

b. Barrier metal system - deposition, composition.

c. Step coverage (bump to glassivation).

d. Design configuration.

e. Thickness of barrier metal.

f. Thickness of bump.

g. Hardness.

h. Bump height uniformity.

i. Bump shear.

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j. Bath purity.

F.4.3.1 Visual examination of bump. Visual examination of the bump is required prior to bond. Sample size and accept/reject limits shall be documented and determined by the manufacturer, and, at a minimum, address the following areas:

a. Alignment of bump to pad.

b. Contaminants, conductive residue.

c. Bleeding bump (metallization exposed to higher than normal temperature excursions).

d. Ineffective or improper photoresist application or removal.

e. Cracks, voids.

f. Partial and/or missing bumps.

g. Nodules or malformed bumps.

h. Discolored bumps.

I. Mechanically damaged bumps.

F.4.4 Bond. Bond requirements shall be as specified in F.4.4.1-F.4.4.3.

F.4.4.1 Bond process characterization. Process characterization of inner lead bond is critical to the quality and reliability of a TAB device and must be performed and documented to ascertain the minimum, maximum, and mean destructive bond pull limits to meet the requirements set forth herein. During the process characterization the following factors shall be considered and included as appropriate:

a. Tape composition.

b. Bond force.

c. Bond temperature.

d. Bond pressure.

e. Underlying layers such as:

- Bump configuration.
- Glassivation composition.
- Bond pad opening.

f. Any underlying metallization and passivation.

g. Cracking (the manufacturer shall evaluate the significance of any cracking throughout the device including around and below the bump area).

F.4.4.2 Visual inspection of bond. Visual inspection of bond is required prior to encapsulation. Sample size and accept/reject limits shall be documented and determined by the manufacturer, and, at a minimum, shall include the following criteria:

a. ILB lead to bump alignment.

b. Lead contact length; bond lead contact length (L) must be greater than the lead width (W). (See figure F-1.)

c. Lead side edge overhang shall be evaluated.

d. No open/lifted, peeling, or missing leads.

e. No visual shorts.

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f. Cracks in bumps, thin film gold bump pad, glassivation, metal, or active area adjacent to the inner lead bond bumps shall not exceed the characterization requirements in F.4.4.1.

g. For single point bonds, the tool impression must cover 100 percent of the lead to bump contact width.

h. For alloy bonds, fillet must be visible on at least one side of the lead continuously across the bump.

F.4.5 Encapsulant. The following items a - h, as a minimum, shall be baselined by the manufacturer, and items g - h shall be sampled on a frequency basis necessary to demonstrate process control.

a. Coefficient of thermal expansion and relationship to underlying layers.

b. Presence of volatile components.

c. Gel time and temperature.

d. Cure profile (initial, ramp, and final): Time and temperature.

e. Final properties of cured polymer.

f. Storage of encapsulant.

g. Thickness.

h. Viscosity.

F.4.5.1 Visual examination of encapsulant. Visual inspection of the applied encapsulant post-cure is required. Sample size and accept/reject limits shall be documented and determined by the manufacturer, and, at a minimum, address the following areas:

a. Cracks.

b. Voids.

c. Lack of interfacial adhesion.

d. Poor uniformity.

e. Stress on underlying layers.

f. Coverage of desired area.

F.4.6 Screening. One hundred percent screening shall be performed in accordance with MIL-STD-883 test method 5004, with the following deletions and additions:

F.4.6.1 Optional internal visual. An optional internal visual examination may be performed prior to bump utilizing applicable criteria within MIL-STD-883 test method 2010 and/or manufacturer's internal criteria in order to screen die defects. Sample size and accept/reject criteria shall be determined and documented by the manufacturer.

F.4.6.2 Internal visual screen. One hundred percent internal visual examination shall be performed prior to encapsulant utilizing applicable criteria within MIL-STD-883 test method 2010 to screen die defects. At the manufacturer's option, bump visual and ILB visual may be combined with this internal visual examination provided 100 percent of the product is examined.

F.4.6.3 Temperature cycle. One hundred percent temperature cycle shall be performed in accordance with MIL-STD-883, test method 1010, test condition C.

* F.4.6.4 Burn-in. One hundred percent pre, interim, and post burn-in electrical test shall be performed per the device specification. One hundred percent burn-in shall be performed in accordance with MIL-STD-883 test method 1015.

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F.4.6.5 Percent Defective Allowable (PDA). PDA shall be calculated in accordance with MIL-STD-883 test method 5004.

F.4.6.6 External visual. 100 percent external visual examination shall be performed in accordance with MIL-STD-883 test method 2009 or manufacturer's applicable external criteria.

F.4.7 Quality conformance inspection. Quality conformance inspection shall be performed in accordance with MIL-STD-883 test method 5005 with the following deletions and additions:

* F.4.7.1 Group A inspection. Group A inspection shall be in accordance with MIL-STD-883 test method 5005 and the applicable device specification.

F.4.7.2 Group B inspection. Group B inspection shall be in accordance with the following:

F.4.7.2.1 Resistance to solvents. Resistance to solvents (MIL-STD-883 test method 2015) shall be performed when ink marking is utilized. Sample size shall be in accordance with MIL-STD-883 test method 5005.

* F.4.7.2.2 Attachability. Attachability of the outer lead bond shall be assured as documented in the device specification and shall include sample size and accept/reject limits.

* F.4.7.2.3 Destructive bond strength. Destructive bond strength (MIL-STD-883 test method 2011) shall be performed, prior to encapsulation, on inner lead bonds and may be performed during the assembly operation, prior to burn-in. Sample size shall be in accordance with MIL-STD-883 test method 5005. The minimum value of destructive bond strength shall be documented in the device specification. Defect criteria shall include identification of the site of failure at one or more of the following areas:

a. Lead lift.

b. Lead break at bump.

c. Lead break away from bump.

d. Lead break at tape window.

e. Metal peels off tape.

f. Bump delamination from thin film metal.

g. Thin film metal delamination.

h. Crater under bump.

i. Not bonded.

j. Error (operator, machine, hook slips, etc.).

* F.4.7.2.4 Constant acceleration. Constant acceleration (MIL-STD-883 test method 2001, test condition E (min), Y1 direction only) shall only be required if documented in the device specification.

F.4.7.3 Group C inspection. Group C inspection shall be performed in accordance with MIL-STD-883 test method 1005. Sample size shall be in acordance with MIL-STD-883 test method 5005. Initial group C must be completed utilizing TAB packaging, while subsequent group C inspections may be performed utilizing alternate packaging technology.

F.4.7.4 Group D inspection. Group D inspection shall be in accordance with MIL-STD-883 test method 5005 with the following deletions and additions:

a. Subgroup 1 of table IV shall be performed as specified.

b. Subgroups 2, 6, 7, and 8 of table IV of test method 5005 shall not be performed.

c. Subgroup 3 of table IV of test method 5005 shall be performed as specified with the exception of moisture resistance (test method 1004) and seal (test method 1014).

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* d. Subgroup 4 of table IV of test method 5005 shall be performed as specified with the exception of constant acceleration (unless specified in the device specification) (test method 2001) and seal (test method 1014).

e. Subgroup 5 of table IV of test method 5005 shall be performed as specified with the exception of seal (test method 1014).

F.4.7.4.1 Highly Accelerated Stress Testing (HAST). HAST shall be performed in accordance with JEDEC standard 22 TM A112, and shall be performed using a sample size number (accept number) of 15(0) for 50 hours at +130°C at 85 percent relative humidity. As an option, 85/85 testing in accordance with JEDEC standard 22 TM A101 shall be performed using 15(0) sample size (accept number) for 1000 hours.

F.4.7.4.2 Post-test visual examinations. Post-test visual examinations shall be performed in accordance with F.4.6.6 of this appendix.

F.4.8 Major changes. Major changes shall be as set forth in MIL-PRF-38535 as applicable. In addition, the following shall be considered as a major change:

a. Any change to baselined items in this appendix.

b. Bond characterization parameters.

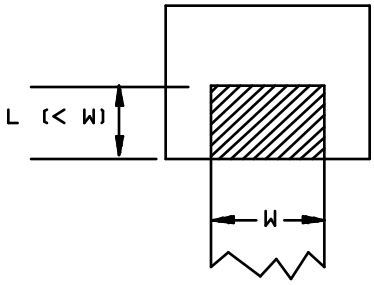

FIGURE F-1. Lead contact length.

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APPENDIX G

THE QML PROGRAM

G.1 SCOPE

G.1.1 Scope. The QML program measures and evaluates the manufacturers' manufacturing process against a baseline for that process. This baseline can include innovative and improved processes that result in an equivalent or higher quality product, provided that the process used to evaluate and document these changes has been reviewed and approved. Changes to the process baseline can be made by the manufacturer's TRB after achieving QML status with documented reliability and quality data. The approach outlined in this appendix is a proven baseline which contains details of the QM program including the TRB, the QM plan, and change control procedures. Compliance with this appendix is not mandatory. However, manufacturers must be able to demonstrate a process control system that achieves at least the same level of quality as could be achieved by complying with this appendix.

G.2 APPLICABLE DOCUMENTS

ELECTRONIC INDUSTRIES ASSOCIATION (EIA)

EIA-557-A Statistical Process Control Systems.

(Application for copies should be addressed to the Electronic Industries Association, 2500 Wilson Boulevard, Arlington, VA 22201-3834.)

* G.3 REQUIREMENTS. The requirements of the microcircuits are classified in the generic qualification flow diagram (see figure 1).

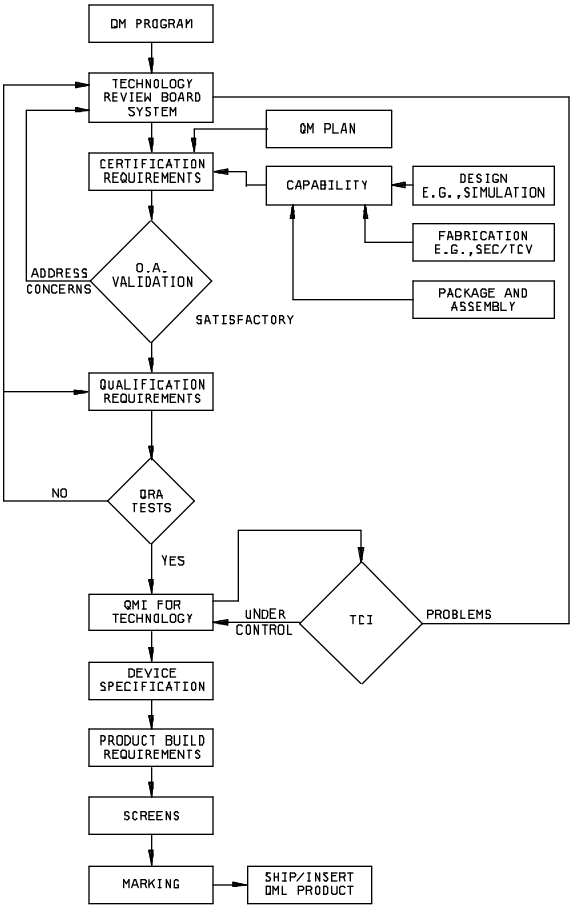

FIGURE 1. Generic qualification flow diagram.

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G.3.1. QM program. A quality management program will be developed and implemented by the manufacturer and documented in the QM plan (see G.3.3 herein). Also, the manufacturer shall have a self-assessment program with an evaluation system similar to that posed by the Malcolm Baldridge Quality Award, and the results of this assessment shall be made available for review. The manufacturer is encouraged to apply for the Malcolm Baldridge National Quality Award within 5 years of initial request for QML status.

G.3.2 Manufacturer's Review System (TRB). The TRB, is responsible for development of the QM plan, maintenance of all certified and qualified processes, process change control (see 3.3.4), reliability data analysis, failure analysis, corrective actions, QML microcircuit recall procedures, and qualification status of the technology.

G.3.2.1 Organizational structure. The manufacturer's TRB should insure communication is established and maintained among representatives from device design, technology development, wafer fabrication, assembly, testing, quality assurance and third party organizations. Records of the TRB deliberations and decisions should be maintained. These records will be made available to the qualifying activity. The manufacturer will submit the name(s) and telephone numbers of their TRB systems' contact person(s) to the qualifying activity.

G.3.2.2 TRB duties. The TRB will keep the qualifying activity updated on the status of QML technology and products. The TRB should have a methodology in place for assessing the current status of the quality and reliability of its microcircuits by review of the Statistical Process Control (SPC) procedures and QM status of the manufacturer's process technology, reliability test data (i.e., parametric monitor, Technology Characterization Vehicle (TCV), Standard Evaluation Circuit (SEC) and device), and the Failure Analysis (FA) results of burn-in/screening failures and board/assembly failures and field returns, as applicable. A method or procedure to verify correlation between test structures and actual product should be approved by the TRB. The TRB will maintain records, available for qualifying activity review, of conditions found and the action taken. The TRB is required to report periodically to the qualifying activity on the status of the QML technology and products (see G.3.2.3 herein). The TRB should also address the impact of key managerial/TRB personnel changes and business plans in order to evaluate any impact they may have on the QML system.

When the reliability data indicates corrective action is required, the TRB should determine and implement the appropriate action in a timely manner. The SEC and TCV (see G.3.3f herein) data are to be used as a tool for monitoring the quality and reliability of the manufacturer's line and do not automatically disqualify a manufacturer when trends or limits require corrective action.

When reliability of shipped microcircuits is called into question, the TRB should provide evaluation and corrective action and prompt notification to the qualifying activity to preserve the manufacturer's qualified status and assure that defective product is not shipped.

G.3.2.2.1 QML certification and qualification test plan (see G.3.3g). Before a management and technology validation is scheduled, the manufacturer should submit to the qualifying activity a TRB approved test plan with milestone charts outlining the tests to be used to certify processes and the tests and devices to be used to qualify the certified processes to the requirements of 3.4.1. The TRB will determine the tests to be accomplished on the TCV, SEC, and parametric monitor and submit to the qualifying activity a test plan with parametric limits and accept and reject criteria.

G.3.2.3 Status report. The manufacturer's TRB will submit a status report to the qualifying activity describing the health of the QML manufacturer's line including all changes and the criticality of the changes in microcircuit quality, reliability, performance, and interchangeability. Support test data should be retained by the manufacturer. The qualifying activity can request to review the supporting data. The following areas should be addressed in each status report: (The information in the status report may be addressed in various ways, such as, copies of TRB meeting minutes, summary of major actions, etc.)

a. Field returns and corrective actions.

b. SPC and continuous improvement program update (e.g., defect density summary, in-process reliability monitors, Cpk programs, etc.).

c. SEC and TCV test data summary, including radiation data if applicable.

d. Design facility.

e. Fabrication line.

f. Assembly facility.

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g. Test facility.

h. Major changes.

i. Newly qualified packages.

j. Third party activities.

The interval of the status reports to the qualifying activity will be determined by the TRB, but should be as a minimum, quarterly for the first year following the attainment of QML status and as a minimum, semiannually (no further than six months apart) thereafter. If major problems with the technology are encountered, more frequent reports may be required by the qualifying activity to keep informed of the status. In addition to the above report, the manufacturer will make a presentation yearly to the qualifying activity outlining the status of the technology, products offered, future trends and other strategic business plans of the technology including foreseen changes. At the discretion of the qualifying activity, this presentation may be in lieu of a status report.

G.3.3 QM plan. The TRB will oversee and approve the QM plan consisting of the following activities and initiatives, as a minimum:

a. Quality improvement plan. This plan documents the specific procedures to be followed by the manufacturer to assure continuous improvement in quality, and reliability of the process and the product being produced.

b. Failure analysis program. This program establishes the procedures that a manufacturer self-imposes to test and analyze sufficient failed parts to determine each failure category from all stages of manufacturing and the field. This program should also identify corrective actions or specify the use of a corrective action plan based on the findings of the failure analysis.

c. SPC plan. A specific plan defining the manufacturer's SPC program within the manufacturing process to the requirements of EIA-557-A .

d. Corrective action plan. This plan should specify the specific steps followed by the manufacturer to correct any process which is out of control or found to be defective.

e. Change control program. This program addresses the process by which a manufacturer addresses changes to the technology. Further information of areas to be considered critical for change control are outlined in G.3.4 herein.

f. SEC and TCV assessment program. The frequency, testing methods, and criteria for evaluations of the SEC or the TCV or both, including correlation of test structures and actual product, are to be determined by the TRB based on the manufacturer's assessment of risk. The manufacturer's SEC and TCV evaluation plan shall be documented.

g. Certification and qualification plan. The certification and qualification plan should be defined in appendix H including self-assessment and corrective actions.

* h. Retention of data. This program establishes the requirements for data retention (see A.4.8.1.2 as a guideline).

G.3.3.1 QM plan outline. The following should be addressed in the QM plan. Submittal of the QM plan is required before the validation (certification) meeting.

NOTE: Many of these items and their associated documentation may be reviewed during the validation.

a. Index of certified baseline documents. - A list of the specification titles, document numbers, and revisions which make up the QML program. This is the baseline the manufacturer was certified to at a validation review.

b. Conversion of customer requirements. - A system for converting all customer's requirements into in house requirements. This includes determining if certification and QML coverage exist. The following are both part of the QM plan and the manufacturer's conversion system:

1. Device specification requirements (Standard Microcircuit Drawing (SMD)).
2. Controlled design procedures and tools (established geometric, electrical, and reliability design rules).
3. Mask generation procedure within the controlled design procedures of 2.
4. Wafer fabrication and assembly capabilities baselined.
5. Design, mask, fabrication, assembly, and test flows.

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6. QML listing coverage.
7. SEC, TCV or alternate assessment procedure, and parametric monitor programs and test procedures (see G.3.3f).
8. Incoming inspection and vendor procurement document covering design, mask, fabrication, and assembly.
9. Screening and traveler.
10. Technology Conformance Inspection (TCI) procedures, including identification of destructive/nondestructive classification of tests.
11. Marking.
12. Rework.

c. Functional organization Chart covering the TRB, quality assurance, and production.

d. Change control program (see G.3.4 herein). - This item shall consist of a system by which changes to the QML program are classified and necessary actions taken. The following shall be addressed, as a minimum:

1. Major changes.
2. Required testing.
3. * TRB responsibility (e.g., notification policy).
4. TRB MIL-PRF-38535 program interface for Defense Supply Center Columbus (DSCC).

e. Failure analysis (see G.3.3b).

f. Self-audit program and audit results.

* g. TRB reporting (to DSCC), including checklist and procedure.

h. Yield improvement program (see G.3.3a).

i. SPC program (EIA-557-A should be used as a guideline) including, goals and plans of implementation, in-line Process Monitors (PM's), SPC measurement points (including location and procedure number on applicable flow charts; see G.3.3c).

j. List of test methods for laboratory suitability including any outside lab.

k. Major test methods for which data may be requested to be submitted:

1. Burn-in.
2. Temperature cycle.
3. Fine and gross leak.
4. Particle Impact Noise Detection (PIND).
5. Temperature/humidity testing.
6. Preconditioning (board assembly/rework simulation.)
7. Wafer (lot) acceptance.
8. Internal visual.
9. Nondestructive Bond Pull (NDBP).
10. SEM or nondestructive SEM.
11. Life test.
12. Radiographic inspection.
13. Radiation testing.

l. Calibration.

m. Retention of qualification.

n. Training.

o. Cleanliness and atmospheric controls.

p. Electrostatic Discharge Sensitivity (ESDS) program.

q. Certification and qualification test plan (see G.3.2.2.1).

r. Process for control of third party activities.

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G.3.4 Change control procedures. The following paragraphs outline areas of concern where a change may require action by the manufacturer. All changes to any part of a QML manufacturer's line are to be governed by the manufacturer's TRB and made available to the qualifying activity. All changes should be documented as to the reason for the change with supporting data taken to support the change, including reliability data as appropriate. The decision as to the criticality of the change will be guided by the potential effect of the change on quality, reliability, performance and interchangeability of the resulting microcircuits. For any change that merits consideration for requalification, the TRB should decide if requalification is needed. Microcircuits should be shipped following a change only upon approval of the TRB. Modifications to screens and TCI's are allowed but must be justified, documented, and submitted to the qualifying activity. Notification of the change should be made concurrently to the qualifying activity for a period of not less than one year after initial QML listing. Thereafter, notification should be made in the TRB status reports (see G.3.2.3 herein). The manufacturer may make notification of this change of product through the Government-Industry Data Exchange Program (GIDEP) using the Product Change Notice, in any case the manufacturer should assure that all known acquiring activities are notified.

G.3.4.1 Design methodology change. Changes in the design methodology to be evaluated by the TRB will include, but not be limited to, changes in the following areas:

a. Technology data base (cell/design library).

b. Design flow.

c. Design system (Computer Automated Design (CAD), design rules).

d. Software updates.

e. Model or modeling procedures.

f. Configuration management.

g. Radiation hardness assurance (if applicable).

h. Electrical performance.

G.3.4.2 Fabrication process change. Changes in the fabrication process to be evaluated by the TRB will include but not be limited to changes in the following areas:

a. Fabrication process sequence or process limits.

b. Fabrication process materials or material specifications, including epitaxial layer thickness.

c. Photoresistive materials or material specifications.

d. Doping material source, concentration, or process technique (e.g., ion implantation versus diffusion).

e. Cross section diffusion profile.

f. Passivation or glassivation material, thickness or technique (including addition or deletion of passivation).

g. Metallization system (pattern, material, deposition or etching technique, line width or thickness).

h. Baseline (DSCC-VQC-42 form or equivalent).

i. Conductor, resistor or dielectric materials.

j. Wafer fabrication move from one line or building to another.

k. Passivation or glassivation process temperature and time.

l. Oxidation or diffusion process, oxide composition and thickness, oxidation temperature and time.

m. Sintering or annealing temperature and time.

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n. SEC and how it is tested.

o. Method of mask making.

p. Parametric monitor and how it is tested.

q. Wafer acceptance criteria.

r. TCV and how it is tested.

s. Sample plans (quantity and acceptance numbers).

t. Gate formation process, material, technique.

u. Backside process to include, wafer thinning and backside metallization.

v. Ohmic contact formation.

w. Starting material qualification (i.e., GaAs boule).

x. Lot formation.

G.3.4.3 Assembly process change. Changes in the assembly process to be evaluated by the TRB will include but not be limited to changes in the following areas:

a. Die attach material, method, or location.

b. Wire/ribbon bond interconnect method.

c. Wire material composition and dimensions.

d. Seal technique (materials or sealing process, gas composition (e.g., for RHA)).

e. Implementation procedures for internal visual and other test methods.

f. Assembly flow.

g. Assembly operation move.

h. Scribing and die separation method.

i. TCI procedures including manufacturer imposed tests.

j. Screening tests.

k. Sample plans (quantity and acceptance numbers).

l. Die back surface preparation.

m. Bond pad geometry, spacing, or metallization.

n. Molding material, method, or location.

o. Chip encapsulation/coating material and technique.

p. Device marking process.

q. Lot formation.

G.3.4.4 Package change. Changes in the package qualification to be evaluated by the TRB will include, but not be limited to changes in the following areas:

a. Vendor.

b. External dimensions.

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c. Cavity dimensions.

d. Number of leads or terminals.

e. Lead or terminal dimensions (length times width or diameter).

f. Lead or terminal base material.

g. Lead or terminal plating material.

h. Lead or terminal plating thickness (range of).

i. Body material.

j. Body plating material.

k. Body plating thickness (range of).

l. Die pad material.

m. Die pad plating.

n. Die pad plating thickness (range of).

o. Lid material.

p. Lid plating materials (range of).

q. Lid plating thickness (range of).

r. Lid seal (preform) material.

s. Lid glass seal material.

t. Lead glass seal material.

u. Lead glass seal diameter (range of).

v. Leads or terminals spacing.

w. Lead configuration (e.g., J-lead, gullwing).

x. Die size.

y. Device marking process.

z. Lead attachment.

G.3.4.5 Test facility change. Changes in the test facility to be evaluated by the TRB will include but not be limited to changes in the following areas:

a. Implementation procedures for internal visual and other test methods.

b. Testing flow.

c. Test facility (with laboratory suitability) move from one facility or building to another.

d. Sample plans (quantity and acceptance numbers).

e. Test procedures (including test vector generation).

f. Lot formation.

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APPENDIX H

CERTIFICATION, VALIDATION, AND QUALIFICATION

H.1 SCOPE

H.1.1 Scope. The QML program measures and evaluates the manufacturers' manufacturing process against a baseline for that process. This baseline can include innovative and improved processes that result in an equivalent or higher quality product, provided that the process used to evaluate and document these changes has been reviewed and approved. Changes to the process baseline can be made by the manufacturer's TRB after achieving QML status with documented reliability and quality data. The approach outlined in this appendix is a proven baseline which contains details of the certification, validation, and qualification programs. Compliance with this appendix is not mandatory. However, manufacturers must be able to demonstrate a process control system that achieves at least the same level of quality as could be achieved by complying with this appendix.

H.2 APPLICABLE DOCUMENTS

ELECTRONIC INDUSTRIES ASSOCIATION (EIA)

EIA-557-A - Statistical Process Control Systems.

(Application for copies should be addressed to the Electronic Industries Association, 2500 Wilson Boulevard, Arlington, VA 22201-3834.)

H.3 CERTIFICATION

H.3.1 General. The qualifying activity will evaluate the manufacturer's approach to the process baseline.

H.3.2 Process capability demonstration. Process capability demonstration should consist of:

a. Design

1. Circuit
2. Package

b. Wafer fabrication

c. SPC and in-process monitoring programs including the TCV program and the Standard Evaluation Circuit (SEC), and parametric monitors

d. Wafer acceptance plan

e. Assembly and packaging

f. RHA (see appendix C)

H.3.2.1 Design. The manufacturer should address the design methodology for the following areas of design.

NOTE: These are also applicable to third party design centers.

H.3.2.1.1 Circuit design. QML microcircuits should address the circuit design requirements and performance characteristics herein:

a. Model verification. Provide evidence that all models utilized in the design process are functional, predictable and accurate over the worst case temperature and electrical extremes. Examples of these models are: transistor behavioral, logic, fault, timing, simulation, fabrication, assembly and package.

b. Layout verification. Demonstrate the capability of the automated or manual procedures routinely used for design, electrical and reliability rule checking to catch all known errors singly and combinationally. These rules cover, as a minimum:

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1. Design Rules Check (DRC): Geometric and physical.
2. Electrical Rules Check (ERC): Shorts and open, connectivity.
3. Reliability rules: Electromigration and current density, I_R drops, latch-up, Single Event Upset (SEU), hot electrons, ESD, burnout backgating.

c. Performance verification. The manufacturer should design and construct a chip or set of chips to assess the process capability to perform routing and to accurately predict post-routing performance. The manufacturer should demonstrate that the actual measured performance for each function over temperature and voltage falls between the two worst case CAD simulation performance limits. All critical minimum geometric and electrical design rules should be stressed via devices or structures located on the SEC, TCV, and/or PMs. The electrical stress requirements for the transistors and interconnects on these structures should be worst case conditions. Failure Analysis (FA) should be conducted to identify all failure mechanisms occurring in the failed devices and structures, and actions should be taken to correct any problems found.

d. Testability and fault coverage verification. The manufacturer should demonstrate a design style and a Design-For-Test (DFT) methodology which, in conjunction with demonstrated CAD for test tools, can provide 99 percent or greater fault coverage on a design of reasonable complexity. The manufacturer should also address his approach for a testability bus to groups such as the Joint Test Action Group (JTAG). The manufacturer should demonstrate the fault coverage measurement (fault simulation, test algorithm analysis, etc.) capability which is used to provide fault coverage statistics of the design that uses the demonstrated design style, DFT method and CAD for test tools. Measurement of fault coverage should be in accordance with the procedures defined in MIL-STD-883, test method 5012. For nondigital microcircuits, the fault coverage requirement may not be applicable, but should be supplemented as measures of analog fault coverage become better-defined. For microcircuits with both analog and digital functions, this requirement fully applies to the digital portions of the microcircuits.

H.3.2.1.2 Package design and characterization. Packages used for QML microcircuits should address the design requirements and performance characteristics herein. Characterization may be performed by the microcircuit manufacturer, by an external lab or by the package supplier. In any case, the manufacturer's assembly of QML microcircuits should address all the testing requirements herein. The manufacturer must address package design/construction quality and reliability. The manufacturer is responsible to maintain documented validation of all characterization methods used, including all supporting data.

a. Thermal characterization. The thermal resistance should be determined for all packages used in the manufacture of QML parts. This value may be obtained by direct or indirect measurements, or by simulation tools or calculations. Test method 1012 of MIL-STD-883 may be used for this calculation. If the thermal resistance is obtained by a calculation or simulation tool, this procedure should be certified. To certify such a method of theoretical estimation, the manufacturer must demonstrate a correlation between the theoretically estimated value and the actual measured value for at least one package of the same style with equal or greater pin count.

b. Electrical characterization. The following electrical characterization parameters should be addressed:
   1. Ground and power supply impedance. Packages used in the manufacture of QML microcircuits should be minimal contributors to ground and power supply noises. The above requirement can be met either through the use of documented package design rules or through testing of the packages, either individually or by similarity, in accordance with test method 3019 of MIL-STD-883.
   2. Cross-coupling effects. Cross-coupling of wideband digital signals and noise between pins in packages used for digital QML microcircuits should be minimized. The above requirement can be met either through the use of documented package design rules or through testing the packages, either individually or by similarity, in accordance with test methods 3017 and 3018 of MIL-STD-883.
   3. High voltage effects. The voltage applied to a QML package should not produce a surface or bulk leakage between adjacent package conductors (including leads or terminals). The above requirement can be met either through the use of documented high voltage package design rules aimed at minimizing bulk or surface leakage, or through testing of the high voltage packages, either individually or by similarity, in accordance with test method 1003 of MIL-STD-883.

Test plans for each of these areas should be approved by the TRB and made available as part of the certification test plan (see G.3.2.2.1). All tests should be completed, documented and analyzed and a summary made available to the qualifying activity before or during the management and technology validation.

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H.3.2.2 Wafer fabrication. As part of certification, the manufacturer should identify a specific technology or technologies for the wafer fabrication. A technology consists of the fabrication sequence, design rules and electrical characteristics. Demonstration of wafer fabrication capability consists of the following and all supporting documentation and data should be made available to the qualifying activity before or during the management and technology validation.

H.3.2.2.1 SPC and in-process monitoring program. An in-process monitoring system should be used by the manufacturer to control key processing steps to insure device yield, reliability and RHA if applicable. The monitoring system can utilize various test structures, methods and measurement techniques. The critical operations to be monitored should be determined by the manufacturer based on his experience and knowledge of his processes. The resulting data should be analyzed by appropriate SPC methods (in accordance with the requirements of EIA-557-A) to determine control effectiveness. The following should be addressed for the wafer fabrication process as a minimum by the manufacturer:

1. Incoming mask and fabrication process materials.
2. Equipment used for wafer fabrication.
3. Doping material concentration.
4. Cross section diffusion or concentration profile, and epitaxial layer.
5. Passivation or glassivation.
6. Metallization deposition.
7. Photolithography and resultant line width.
8. Passivation process temperature and time.
9. Diffusion, implant anneal process temperature and time, or both.
10. Sintering or annealing temperature and time.
11. All reliability test data including the SEC.
12. Mask inspection and defect density data.
13. Parametric monitor test data.
14. Wafer acceptance test.
15. TCV.
16. Photoresistive processing (including rework procedures).
17. Ion implant.
18. Wafer backside preparation.
19. Wafer probe acceptance criteria.
20. Rework.
21. Oxide process.
22. Gate formation.
23. Air bridge process.
24. Via hole process.

H.3.2.2.2 TCV program. A TCV program should be implemented by the manufacturer for the technology or process being considered for certification. The program should contain, as a minimum, those test structures needed to characterize a technology's susceptibility to intrinsic reliability failure mechanisms such as electromigration, Time Dependent Dielectric Breakdown (TDDB), gate sinking, ohmic contact degradation, sidegating/backgating, and hot carrier aging. If other wearout mechanisms are discovered as integrated circuit technology continues to mature, test structures for the new wearout mechanisms should be added to the TCV program. The TCV program will be used for the following purposes: certification of the technology; reliability monitoring; radiation hardness assurance and monitoring, when applicable; change control; and the characterization of fast-test intrinsic reliability structures.

NOTE: The test structures necessary to monitor intrinsic reliability failure mechanisms do not have to be a single die or location, but can appear on the parametric monitor, the SEC, or the device itself. The TCV program (see G.3.3f) should, however, indicate where the structures are located and how they are tested and analyzed.

H.3.2.2.2.1 TCV certification. For initial certification, sufficient TCV test structures for each wear-out mechanism should be subjected to accelerated aging experiments. The TCV test structures should be randomly chosen from and evenly distributed from three homogeneous wafer lots in the technology to be certified in the fabrication facility to be certified. These wafers must have passed the wafer or wafer lot acceptance requirements. The accelerated aging experiments should produce an estimate of the Mean-Time-To-Failure (MTTF) and a distribution of the failure times under worst case operating conditions and circuit layout consistent with the design rules for each wear-out mechanism. From the MTTF and distribution of failures a worst case operating lifetime or a worst case failure rate can be predicted. Test structures should be from completed wafers which have been passivated/glassivated. A summary of the accelerated aging data and analysis should be available for review by the qualifying activity. The initial certification MTTF, failure distribution and acceleration factors should be used as benchmarks for the technology to which subsequent TCV results will be compared.

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All of the TCV test structures must be packable using the same packaging materials and assembly procedures as standard circuits in the technology.

NOTE: In those cases where this may not be possible, the TCV should be packaged in a suitable package to allow for the evaluation of the chip technology to be qualified, without adversely affecting the outcome of the test.

The TCV structures need not use a fully qualified package since qualified packages will tend to have lead counts far in excess of those needed for intrinsic reliability studies. The packaging requirement for the TCV may be waived by the qualifying activity if the manufacturer can supply documentation showing the equivalence of wafer level and packaged accelerated aging results.

An example of the need to package a TCV test structure concerns the hydrogen content of a ceramic package and its effect on hot carrier aging. It is known that hydrogen present in a MOS device can aggravate hot carrier aging. If the passivation layer of the device does not contain enough hydrogen to mask the presence of hydrogen in the ceramic package, the aging results for hot carrier studies can differ substantially for packaged and nonpackaged devices. The minimum requirements to be addressed for the TCV structures for specific mechanisms are given below.

a. Hot carrier aging. The TCV should use structures that monitor hot carrier aging applicable to the technology to be used in QML microcircuits. Device degradation is to be characterized in terms of both linear transconductance (gm) and Threshold Voltage (VT) and the resistance to hot carrier aging is to be based on whichever parameter experiences the manufacturers' specified degradation limit for the minimum channel length and width allowed in the technology. A wafer level fast-test screen should be established for technologies that are susceptible to hot carrier aging. This test should be part of the wafer acceptance criteria.

1. MOS. The TCV should have structures to characterize the effects of hot carrier aging as a function of channel length for MOS transistors for each of the nominal threshold voltages used in the technology. Degradation should be characterizable in terms of gm and VT.

2. Bipolar. The TCV should contain structures for characterizing hot carrier aging of diodes in bipolar technologies.

b. Electromigration. The TCV should contain structures for the worst case characterization of metal electromigration over:

1. Flat surfaces.
2. Worst case noncontact topography.
3. Through contacts between conductive layers.
4. Contacts to the substrate.

The current density and temperature acceleration factors for electromigration should be determined and a MTTF and failure distribution determined for the worst case current, temperature and layout geometry allowed in the technology. From the MTTF and failure distribution, a failure rate for electromigration in the technology should be calculated.

c. Time Dependent Dielectric Breakdown (TDDB) (MOS). The TCV should contain structures for characterizing TDDB of gate oxides. The structures should have gate oxide area and perimeter dominated structures. Separate perimeter structures should be used for the gate ending on a source or drain boundary and where the gate terminates over the transistor to transistor isolation oxide. The electric field and temperature acceleration factors for TDDB should be determined and a MTTF and failure distribution determined for the worst case voltage conditions and thinnest gate oxide allowed in the technology. From the MTTF, a failure rate for TDDB in the technology should be calculated.

d. TCV fast test structure requirements. The structures to be used for the fast test reliability monitoring of hot electron aging should be included in the TCV program so that correlations of the fast-test measurements with the accelerated aging results may be made.

NOTE: It is strongly recommended that fast test intrinsic reliability structures for electromigration and TDDB be included in the TCV program so that correlations can be made with longer term aging experiments. It is likely that these structures will be required for wafer acceptance in the future.

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e. Ohmic contact degradation. The TCV should have a structure for assessing the degradation of ohmic contacts with time at temperature, especially for GaAs.

f. Sidegating/Backgating. A structure should be included for evaluating sidegating/backgating of FET's in GaAs technology.

g. Sinking gate. A FET structure should be included for evaluating the sinking gate degradation mechanism and other channel degradation mechanisms of GaAs FET's.

H.3.2.2.3 Standard Evaluation Circuit (SEC). A manufacturer should have an SEC for the technology or process being considered for certification. A manufacturer's SEC should be used to demonstrate fabrication process reliability for the technology. The SEC design documentation should address: The design methodology, the software tools used in the design, the functions it is to perform, its size in terms of utilized transistor or gate count, and simulations of its performance. Documentation procedures for the SEC and standard production devices should be the same so that correlation can be made. The SEC may be designed solely for its role as a quality and reliability monitoring vehicle or it may be a product meant for system use. (For RHA environment, see appendix C). The SEC should address the following requirements:

a. Complexity. The complexity of the SEC for digital microcircuits should contain, as a minimum, one-half the number of transistors expected to be used in the largest microcircuit to be built on the QML line. For analog microcircuits, the SEC should exercise the functionality of the process technology flow, be of a representative complexity and be comprised of major circuit element types.

b. Functionality. The SEC should contain fully functional circuits capable of being tested, and screened in a manner identical to the QML microcircuits.

c. Design. The SEC should be designed to stress the design capabilities of the process (see H.3.2.1.1c). The architecture of the SEC should be designed so that failures can be easily diagnosed.

d. Fabrication. The SEC should be processed on a wafer fabrication line which is intended to be or already is a certified QML line.

e. Packaging. The SEC should be packaged in a package qualified in accordance with requirements in 3.4.1.4.1 herein.

NOTE: A different SEC may be required whenever the design rules, the materials, the basic processes, or the basic functionality of the technology differ.

For initial certification, a sufficient number of SEC devices is required, from wafers passing the wafer screen requirements of H.3.2.3 and randomly chosen and evenly distributed from three wafer lots and tested to requirements of tables I - V in the technology to be qualified on the fabrication facility to be qualified. The number of SEC device failures will serve as a qualification benchmark for the technology. Failure Analysis (FA) should be done on failed SEC's to determine each failure category and action taken to correct any problems found. The SEC reliability data, including failure analysis results, should be available for review by the qualifying activity. For RHA environments, irradiate SEC to demonstrate RHACL.

H.3.2.2.4 Parametric Monitor (PM). The manufacturer should have parametric monitors to be used for measuring electrical characteristics of each wafer type in a specified technology. The parametric monitor test structures can be incorporated into the grid (kerf), within a device chip, as a dedicated drop-in die or any combination thereof. Location of the parametric monitor test structures should be optimally positioned to allow for the determination of the uniformity across the wafer. A suggested location scheme is one near the wafer center and one in each of the four quadrants of the wafer, at least two-thirds of a radius away from the wafer center. The manufacturer should establish and document reject limits and procedures for parametric measurements including which parameters will be monitored routinely and which will be included in the SPC program. Documentation of the parametric monitor should also include parametric monitor test structure design, test procedure (including electrical measurement at temperature and the relationship between the measured limits and those determined in the manufacturer's circuit simulations), design rules and process rules. Alternate measurement techniques, such as in-line monitors, are acceptable if properly documented. The following parameters are to be used as a guideline by the manufacturer's TRB in formulating the parametric monitor.

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a. General electrical parameters.

1. Sheet resistance: Structures should be included to measure the sheet resistance of all conducting layers.
2. Junction breakdown: Structures should be included to measure junction breakdown voltages for all diffusions.
3. Contact resistance: Structures should be included to measure contact resistance of all interlevel contacts.
4. Ionic contamination and minority carrier life time: Structures should be included to measure ionic contamination, such as sodium, in the gate, field, and intermetal dielectrics and minority carrier lifetime.

b. MOS parameters.

1. Gate oxide thickness: Structures should be included to measure gate oxide thickness for both n and p gate oxides as applicable.

2. MOS transistor parameters: A minimum set of test transistors should be included for the measurement of transistor parameters. The minimum transistor set should include a large geometry transistor of sufficient size that short channel and narrow width effects are negligible, and transistors that can separately demonstrate the maximum short channel effects and n arrow width effects allowed by the geometric design rules. Both "N" and "P" transistors should be included for a CMOS technology. If there is more than one nominal threshold voltage for either the "N" or "P" transistor type the minimum set should be included for each threshold. The transistor parameters to be measured are given below:

   (a) Threshold voltage: The linear Threshold Voltage (VT) for each transistor in the minimum set of transistors should be measured.

   (b) Linear transconductance: The linear transconductance (gm) for the full minimum set of transistors should be measured.

   (c) Effective channel length: The effective channel length for the minimum channel length of each transistor type should be measured.

   (d) I_{on}: I_{on} for representative transistors in the set.

   (e) I_{off}: I_{off} for representative transistors in the set.

   (f) Propagation delay: A test structure should be available in the form of a functional circuit from which propagation delay information can be measured at room temperature.

   (g) Field leakage: Field transistor leakage for the minimum spaced adjacent transistors at the maximum allowed voltage should be measured.

c. Bipolar parameters. Care should be taken in the manner and sequence in which all breakdown voltage and current measurements are taken so as to not permanently alter the device for other measurements.

1. Sheet resistance: Structures should be included which can be used to measure sheet resistance of all doped regions (e.g., emitter, buried collector.)

2. Schottky diode parameters: The following measurements should be made on Schottky diodes representative of the size used in the technology:

   (a) Reverse leakage: The Reverse Leakage Current (I_R) should be measured at a specified reverse voltage.

   (b) Reverse breakdown: The reverse Breakdown Voltage (BV) should be measured at a specified current.

   (c) Forward voltage: The Forward turn-on Voltage (V_f) should be measured at a specified current.

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* 3. Bipolar transistor parameters: The following measurements should be made on bipolar transistors representative of the size and type used in the technology. The types should include NPN, Schottky clamped NPN, vertical PNP, substrate PNP and lateral PNP transistors as applicable.

(a) Transistor gain: The common Emitter Current dc gain, (Hfe), should be measured on representative transistors at three decades of collector current, the center of which is at the rated current of the device.

(b) Leakage currents: The Leakage Currents (I_{CEO}, I_{CBO}, and I_{EBO}) should be measured on representative transistors at a specified voltage.

(c) Breakdown voltages: The Breakdown Voltages (BV_{EBO}, BV_{CBO}, and BV_{CEO}) should be measured on representative transistors at specified currents.

(d) Forward voltages: The Forward Voltages (V_{BEO} and V_{BCO}) should be measured on representative transistors at the rated currents.

(e) Propagation delay: A test structure should be available in the form of a functional circuit from which propagation delay information can be measured at room temperature.

4. Isolation leakage: The Isolation Leakage Current (I_L) between minimum spaced adjacent transistor collectors should be measured at a specified voltage.

d. <u>GaAs parameters</u>.

1. Sheet resistance: Structures should be included which can be used to measure sheet resistance of each of the conducting layers.
2. MIM capacitor: Capacitor test structures should be included so that dc and rf capacitance, leakage, and breakdown can be measured.
3. FAT FET: A long gate length FET suitable for measurement of Schottky barrier height and ideality factor, carrier concentration and mobility, and channel depth should be included.
4. Isolation: A structure for use in measuring substrate isolation breakdown should be included.
5. Ohmic contacts: An ohmic contact transmission line structure should be included so that specific contact resistance and transfer length can be measured.
6. GaAs FET parameters: FET test structures should be included, suitable for rf probing, which can be used for measurement of both dc and rf FET parameters. The following parameters should be measured:

(a) I_{dss} - saturated drain current at zero gate bias.

(b) gm - transconductance at saturation and at 50 percent I_{dss}.

(c) Pinch off voltage.

(d) Gate-drain leakage and breakdown voltage.

(e) Gate-source breakdown voltage.

(f) Source and drain resistance.

(g) S-parameters of FET over frequency range of technology.

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e. Fast-test reliability structures. Fast-test reliability structures are structures meant to evaluate, within a few seconds of testing, a particular known reliability failure mechanism to insure that the processing which an individual wafer received is consistent with the reliability goals of the technology. The fast-test structures are in general new and, with the exception of hot carrier aging structures, are not sufficiently mature. Development work on them is intense however, and it is intended that these structures when mature, will become a mandatory part of the parametric monitor. For this reason it has been decided to include information regarding fast-test reliability structures in the following paragraphs. Documentation should be available which shows the correlation between fast-tests and the results of the more traditional accelerated aging tests performed on the TCV.

1. Hot carrier aging: A fast-test structure should be included to evaluate the susceptibility of MOS transistors to hot electron aging. This structure may be one of the parametric monitor test transistors.
2. Electromigration: Worst-case design rule fast-test structures should be included to evaluate the susceptibility of each metal level and the associated contacts to electromigration.
3. TDDB: Fast-test structures should be included that can evaluate the long term reliability of gate oxides.
4. Contact resistance: Fast-test structures should be included that can evaluate the long term reliability of contacts.
5. Gate diffusion: Fast-test structures should be included that can evaluate the long term reliability of the gate contact.

H.3.2.3 Wafer acceptance plan. The TRB should develop and demonstrate a wafer acceptance plan based on electrical and radiation (if applicable) measurement of parametric monitors. This plan should utilize the parametric monitor and should include visual criteria, if applicable. The use of test method 5013 of MIL-STD-883 is encouraged for GaAs technology devices. In addition, this plan should address the concerns detailed in MIL-STD-883, test method 2018 (e.g., metallization, step coverage). The use of test method 2018 is encouraged, however alternate procedures utilizing parametric monitors and in-line monitors are accepted if approved during validation. Parametric monitor data should be recorded and made available for review. This plan can be either a wafer by wafer acceptance plan or a wafer lot acceptance plan, but must address the following concerns:

a. Small lots.

b. Large lots.

c. Specialty lots.

H.3.2.4 Assembly and packaging. The manufacturer should demonstrate the capability of the assembly and package processes by qualifying the SEC package or actual product to the package certification and qualification procedures described in 3.4.1.1. The test results of the SEC package qualifications should be made available to the qualifying activity as part of the certification procedure.

H.3.2.4.1 Assembly processes. The manufacturer should list the assembly processes (die-attachment, wire/ribbon bonding, seal molding and code marking) that is expected to be listed on the QML and used in QML microcircuit assembly, and should qualify those processes by testing of fully assembled packages in accordance with the appropriate tests from table H-IA or H-IB for the assembly/packaging technology used. Sample sizes should be determined by the TRB.

H.3.2.4.2 Package technology styles. The manufacturer should document how packages used in the manufacture of QML products are qualified. In particular, the manufacturer should document how packages that offer similar characteristics are grouped together for qualification and change control purposes. Package technology style qualification test methodologies, vehicles, and results should be made available to the qualifying activity upon request. Tables H-IIA and H-IIB identify key package characteristics for which testing must be addressed on each QML package technology style.

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H.3.2.4.3 SPC and in-process monitoring program. A process monitoring system should be used by a manufacturer to control key processing steps to insure product yield and reliability. The monitoring system can utilize various test chips, methods and measurement techniques. The critical operations to be monitored will be determined by the manufacturer based on his experience and knowledge of his processes. The resulting data should be analyzed by appropriate SPC methods to determine control effectiveness. The following should be addressed as a minimum by the manufacturer:

1. Incoming assembly process materials.
2. Incoming package acceptance.
3. Equipment used for assembly.
4. Wafer acceptance criteria.
5. Die attach.
6. Chip to package interconnect (wire/ribbon bond, tab, flip chip).
7. Package seal.
8. Marking.
9. Rework.
10. Lead trim, form and final finish.
11. Atmosphere and cleanliness control.
12. Chip encapsulation/molding.
13. Encapsulant purity.
14. Internal water vapor.

TABLE H-IA. Assembly process qualification testing for hermetic packages.

Group number	Process	Test	MIL-STD-883 test method and condition or JEDEC test method
1	Die-attach and interconnect	Thermal shock (100 cycles) End-point electricals X-Ray or Ultrasonic Visual inspection Bond strength Die shear or stud pull	TM 1011, condition C per device specification TM 2012 or TM 2030 TM 2010 (die-mount and wire bond) plus die cracks TM 2011 TM 2019 or TM2027
2	Die-attach, interconnect and seal	Mechanical shock Variable frequency vibration Constant acceleration Fine and gross leak Visual inspection End-point electricals	TM 2002, condition B TM 2007, condition A TM 2001 TM 1014 TM 1010 criteria, 20X magnification per device specification
3	Lid seal	Internal water vapor (5,000 ppm maximum at +100°C)	TM 1018
4	Lid seal	Lid torque	TM 2024 (glass seal)
5	Code marking	Resistance to solvents	TM 2015
6	Final package testing	High temperature storage	TM 1008 1,000 hours at +150°C
7	Post burn-in lead finish	Solderability	TM 2003 (+245°C ±5°C)

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TABLE H-IB. Assembly process qualification testing for plastic packages. 1/

Group number	Process	Test	MIL-STD-883 test method or industry standard
1	Die-attach and interconnect	In-line visual inspection In-line bond strength In-line ball bond shear In-line die shear/stud pull Post molding X-ray	TM 2010 (die-mount and wire bond) TM 2011 ASTM F 1269 TM 2019 or TM 2027 TM 2012
2	Die-attach, interconnect, and molding	X-ray, ultrasonic inspection, etc.	TM 2012 (die-mount and wire bond), TM 2030
3	Die-attach, interconnect, and molding	Temperature cycling (1000 cycles) Endpoint electricals	TM 1010 Condition C or JESD 22-A104 per device specification
4	Die-attach, interconnect, and molding	Thermal shock (100 cycles)	TM 1011 Condition C or JESD 22-A106 Condition C
5	Marking	Resistance to solvents	TM 2015
6	Storage conditions	High temperature storage	TM 1008, 1000 hours at +150°C
7	Post burn-in lead finish	Solderability	TM 2003

1/ The test methods are listed herein to give the manufacturer an available method to use. Alternate procedures or test methods may be used.

TABLE H-IIA. Technology style characterization testing for hermetic packages.

Group number	Process	Test	MIL-STD-883 test method and condition or JEDEC test method
1	Dimension	Physical dimension	TM 2016
2	Resistance to moisture	15 Thermal shocks 100 Temperature cycles Moisture resistance Visual inspection Fine and gross leak	TM 1011, condition C TM 1010, condition C TM 1004, no bias TM 1010 and TM 1004 criteria TM 1014
3	Susceptibility to corrosion	Salt atmosphere	TM 1009, condition A
4	Leads	Lead integrity	TM 2004, condition A, B2 or D TM 2028 for pin grid array

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TABLE H-IIA. Technology style characterization testing for hermetic packages. - continued

Group number	Process	Test	MIL-STD-883 test method and condition or JEDEC test method
5	Susceptibility to Electrostatic Discharge Sensitivity (ESD)	ESD	TM 3015
6	Susceptibility to latch-up	Latch-up test	JESD 17 or manufacturers internal procedures
7	Thermal resistance	Thermal characteristics	TM 1012

TABLE H-IIB. Technology style characterization testing for plastic packages.

Group number	Process	Test	MIL-STD-883 test method or industry standard
1	Dimensions	Physical dimension	TM 2016 1/
2	Resistance to moisture	Preconditioning Electrical testing Biased HAST (500 hours, +130°C, 85% RH) Endpoint electricals	2/ per device specification JESD 22-A110 3/ per device specification
3	Susceptibility to corrosion	Salt atmosphere	TM 1009
4	Susceptibility to leakage and corrosion	Autoclave (no bias) (pressure pot) 2 atm., +121°C	JESD 22-A102 (data to be provided for 96 hours and 168 hours)
5	Leads	Lead integrity	TM 2004, condition A, B2 or D
6	Susceptibility to moisture induced cracking at reflow soldering for surface mount and applicable through hole packages	Moisture intake Reflow simulation Inspection for delamination and cracks	168 hours at +85°C/85% RH or bake + minimum guaranteed time at +30°C/60% RH Vapor phase (+219°C, no preheat) or Infrared (+240°C maximum) Cross-section at 1000X, ultrasonic (CSAM) etc.
7	Safety	Flammability	UL94-V-O, ASTM2863-77
8	Fungus resistance	Fungus test	Required only if fungus is a concern
9	Susceptibility to Electrostatic Discharge Sensitivity (ESD)	ESD	TM 3015
10	Susceptibility to latch-up	Latch-up test	JESD 17 or manufacturers internal procedures
11	Thermal resistance	Thermal characteristics	TM 1012

1/ Performed as either characterization or as part of qualification.

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TABLE H-IIB. Technology style characterization testing for plastic packages. - Continued

2/ The manufacturer shall define a "preconditioning" procedure that simulates board assembly of plastic surface mount devices. This procedure should include moisture intake and reflow simulation. Exposure to soldering fluxes (possible source of corrosiveness) and to board cleaning agents is also recommended for preconditioning the devices.

3/ 500 hours of HAST is preferred but the qualifying activity will consider the manufacturers overall processing and testing to evaluate this requirement. The actual HAST hours or alternate testing will be included in the QM plan.

H.3.3 Transitional certification and qualification. Manufacturers may be granted transitional certification based on the following requirements:

a. The manufacturer has qualifying activity approval that all facilities covered by the transitional certification supply product built to the previously certified and qualified MIL-M-38510 product flows. Facilities not meeting this conditions are eligible for transitions certification, but they may require an audit if deemed necessary by the qualifying activity.

If the manufacturer has never received MIL-M-38510 certification and qualification, but has been approved by DSCC for Class M products only, an audit of the facilities under QML consideration will be required. If these facilities have been audited by DSCC under the Class M (SMD) random audit program, the audit may not be necessary, as determined by the qualifying activity.

Facilities that have never been audited by DSCC are eligible for transitional certification and an audit will be required unless the qualifying activity determines that an audit is not necessary.

* b. The manufacturer should submit a plan for achieving full QML. The plan should include a self-assessment, quality improvement plan, SPC plan, and a plan to upgrade any DSCC drawing or SMD part to one part-one part number Q level devices.

c. The manufacturer should comply with all requirements of appendix A of this document until the qualifying activity has approved the manufacturer for full QML certification at which time the previous MIL-M-38510 (appendix A of MIL-PRF-38535) requirements will be superseded by the requirements of the main body of this document. As the manufacturer moves toward full QML certification the qualifying activity can allow variations to appendix A as part of the transition process. For class V only, the manufacturer should notify NASA and Air Force Space and Missiles Center (AFSMC) of any proposed major variations to appendix A requirements. Further review by these organizations may be necessary before these variations can be sanctioned.

d. Any major changes to the transitional certification lines should be approved by the qualifying activity until such time as the qualifying activity approves the manufacturers TRB system and QM plan. This includes any deletion of test requests.

e. If any requalifications are required they should be in accordance with the guidelines of appendix A or as approved by the qualifying activity.

f. If the manufacturer has any off-shore facilities covered under transitional certification the requirements of appendix E should apply.

The QML allowances given by this transitional certification will be approved by the qualifying activity. In addition, the manufacturer must make a commitment to becoming QML certified for all portions of the process under transitional certification. If this commitment is not met, the qualifying activity reserves the right to remove the transitional certification and all benefits associated with that certification.

NOTE: The transitional certification is not permanent (approximately 2 years maximum) but allows the manufacturer some flexibility while still working toward QML on the remainder of the processes committed to QML.

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H.3.3.1 QPL manufacturers not transitioned to QML. In the event that a former QPL manufacturer elects not to transition to the QML or is unable to demonstrate capability to transition to QML, that manufacturer should meet all applicable requirements (class S or B as appropriate) of appendix A for as long as they wish to supply any product that was listed on QPL part I. The manufacturers QPL certification will remain valid for this time period with reaudits as deemed necessary by the qualifying activity. The provisions for the removal qualification and certification should apply to the manufacturers existing QPL certification. Products in this category will still be considered JAN product and marked with the JAN certification mark and completely manufactured in the United States or its territories. All former QPL product not transitioned to QML will be listed in section II of QML-38535.

H.3.4 Qualification eligibility. Design, wafer fabrication, assembly, and qualification testing of the demonstration vehicles may begin before certification is granted. However, if deficiencies and concerns found during the validation required changes to the process flows, the design, wafer fabrication, assembly, and testing must be redone on the new process flows. In all cases, start of the qualification testing of the two demonstration vehicles should begin no later than 6 months after the letter of certification is received in order to retain the manufacturer's initial certification. Completion should be achieved in a timely manner or recertification may be necessary.

* H.3.4.1 Demonstration vehicles. The manufacturer should produce, on the certified manufacturing line, two demonstration vehicles, as applicable, as documented in the qualification plan submitted during the certification process. The demonstration vehicles should be of such complexity as to be representative of the microcircuits to be supplied by the manufacturer. Each demonstration vehicle should operate and perform in compliance with the device specification and to the RHACL for a radiation hardened process (which must be submitted to the qualifying activity) and should be manufactured in packages which have been tested prior to use for qualification.

NOTE: For a technology which has die as its primary product, the demonstration vehicle should be suitably packaged to allow evaluation of the technology without adversely affecting the outcome of the tests.

H.3.4.2 Qualification test plan. The manufacturer should present a qualification test plan as part of the certification information which details the test flow, test limits, test data to be measured, recorded and analyzed, test sampling techniques, and traceability records. The test plan should detail materials, manufacturing construction techniques (including design CAD tools), testing and reporting techniques and should be made available to the qualifying activity at the time of certification. The test plan should include traceability documentation, milestone charts and the proposed demonstration vehicle descriptions. All test limits should be in accordance with the requirements of the qualification test plan. All demonstration vehicles must be representative of the manufacturing and screening processes.

H.3.4.3 Qualification test report. The manufacturer should present to the qualifying activity an analysis of the qualification data. The aim of this analysis is to show that all process variables are under control and repeatable within the certified technology and that parametric monitor, TCV, and SEC data monitoring are adequate and correlatable to the process. The qualifying activity should be notified of any improvements/changes to the certified QML technology flow as a result of evaluating the qualification testing data. The following data, if applicable, should be addressed and retained by the manufacturer to support the results:

a. Simulation results from the design process (can be reviewed during the validation).

b. Parametric monitor test data.

c. Results of each subgroup test conducted, both initial and any resubmissions.

d. Number of devices tested and rejected.

e. Failure mode and mechanism for each rejected device.

f. Read and record variable data on all specified electrical parameter measurements.

NOTE: Specified electrical tests from a serialized, random sample (minimum of 22 devices) may be used to satisfy this requirement. The manufacturer may submit variables data in histogram format giving mean and standard deviation or equivalent for passing microcircuits.

g. Where delta limits are specified, variable data, identified to the microcircuit serial number, should be provided for initial and final measurements.

h. For physical dimensions, the actual dimension measurements on three randomly selected microcircuits, except where verification of dimensions by calibrated gauges, overlays, or other comparative dimensions verification devices is allowed.

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i. For bond strength testing, the forces at the time of failure and the failure category, or the minimum and maximum readings of the microcircuits if no failures occur.

j. For die shear or stud pull strength testing, the forces at the time of the failure and the failure category, or the die shear or stud pull reading if no separation occurs.

k. A copy of the test data on nondestructive bond pull testing as required by test method 2023 of MIL-STD-883.

l. For RHA testing, pre and post test end-point electrical parameters, transient and SEP response and test conditions (if applicable).

m. For lid torque strength testing, the forces at the time of failure or the actual torque if no separation occurs.

n. For internal water vapor content readings, report all gases found.

H.3.4.4 Qualification test failures. If any particular testing results are not successful, the manufacturer should perform failure analysis and take necessary corrective action. The manufacturer should notify the qualifying activity of any decision not to pursue qualification of any material or manufacturing construction technique previously certified. After corrective actions have been implemented, qualification testing should restart.

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APPENDIX J

TCI AND SCREENING INFORMATION

J.1 SCOPE

J.1.1 Scope. The QML program measures and evaluates the manufacturers' manufacturing process against a baseline for that process. This baseline can include innovative and improved processes that result in an equivalent or higher quality product, provided that the process used to evaluate and document these changes has been reviewed and approved. Changes to the process baseline can be made by the manufacturer's TRB after achieving QML status with documented reliability and quality data. The approach outlined in this appendix is a proven baseline which contains details of the screening and TCI procedures. Compliance with this appendix is not mandatory. However, manufacturers must be able to demonstrate a process control system that achieves at least the same level of quality as could be achieved by complying with this appendix.

J.2 APPLICABLE DOCUMENTS

(This section is not applicable to this appendix.)

J.3 TCI AND SCREENING INFORMATION

J.3.1 Mask requirements (when applicable). If the mask shop is internal to the manufacturing organization, all designs shall be checked for errors utilizing appropriate design rule checkers before start of the mask making. Before use, the mask shall be inspected for flaws and errors. The final photolithographic mask to be used for QML microcircuit wafer fabrication shall be compliant with the critical dimensions. Measurements shall show that the pattern sizes and positions are consistent with the design rules. All masks shall be maintained under an inventory control program which outlines the inspection and the release of masks to fabrication, recording of usage, cleaning cycles, and maintenance repair. All conditions for removal of masks from inventory shall be documented.

J.3.1.1 Wafer fabrication process. The wafer fabrication process shall be monitored and controlled using a SEC, TCV or alternate assessment procedure, and parametric monitors in accordance with 3.4. The wafer fabrication sequence to produce finished wafers shall be established with processing limits for each wafer fabrication step. Specific items to be addressed are detailed below:

Procedure	Paragraph
Traceability	3.11
Lot travelers	As required (TRB determined)
Glassivation/passivation	H.3.2.2.1
Parametric monitors	H.3.2.2.4
Wafer acceptance	H.3.2.3
Standard evaluation circuits	H.3.2.2.3
Technology characterization vehicles	H.3.2.2.2
Rework	Per QM plan
Internal conductors and metallization thickness	Per applicable design rules

J.3.2 Assembly process procedures. The following assembly process procedures shall be used, as applicable, to assemble QML microcircuits. The manufacturer shall control all phases of the assembly line to ensure that contamination from any source or equipment operation and human intervention does not degrade the reliability of the assembly process or QML microcircuit. Specific items to be addressed are shown below:

Assembly and package procedure	Paragraph
Incoming inspection	H.3.2.2.1
Eutectic die attach	Test method 2010, H.3.2.4.3
Noneutectic die attach	Test method 2010, H.3.2.4.3, Test method 5011 (as applicable)
Internal visual	Test method 2010, H.3.2.4.3 or H.3.4.1.4w herein
Hermeticity	Test method 1014, test method 1018

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Assembly and package procedure	Paragraph
Handling	G.3.3.1g or 3.4.1.4v herein
Human contamination	3.4.1.4x
Rework	J.3.2.1
Internal water vapor content	Test method 1018
Wirebonding	3.4.1.4g, herein

J.3.2.1 Assembly rework requirements. All QML microcircuit rework procedures shall be certified and documented in the QM plan.

J.3.3 Internal visual inspection. Internal visual inspection shall be performed to the requirements of test method 2010, condition B of MIL-STD-883. Microcircuits awaiting pre-seal inspection, or other accepted, unsealed microcircuits awaiting further processing shall be stored in a dry, inert, controlled environment until sealed. Alternate procedures, such as those provided in test method 5004 of MIL-STD-883 or some other TRB approved alternate, may be used. For GaAs devices only, test method 5013, MIL-STD-883, should be used.

J.3.4 Constant acceleration. All microcircuits shall be subjected to constant acceleration, except as modified in accordance with 4.2, in the Y1 axis only, in accordance with test method 2001, condition E (minimum) of MIL-STD-883. Microcircuits which are contained in packages which have an inner seal or cavity perimeter of two inches or more in total length or have a package mass of five grams or more may be tested by replacing condition E with condition D in test method 2001. For packages which cannot tolerate the stress level of condition D, the manufacturer must have data to justify a reduction in the stress level. The reduced stress level shall be specified in the manufacturers QM plan. The minimum stress level allowed in this case is condition A.

J.3.5 Burn-in. Burn-in shall be performed on all QML microcircuits, except as modified in accordance with section 4.2, at or above their maximum rated operating temperature (for devices to be delivered as wafer or die, burn-in of packaged samples from the lot shall be performed to a quantity accept level of 10(0)). For microcircuits whose maximum operating temperature is stated in terms of Ambient Temperature (T_A), table I of test method 1015 of MIL-STD-883 applies. For microcircuits whose maximum operating temperature is stated in terms of Case Temperature (T_C), and where the ambient temperature would cause T_J to exceed +175°C, the ambient operating temperature may be reduced during burn-in from +125°C to a value that will demonstrate a T_J between +175°C and +200°C and T_C equal to or greater than +125°C without changing the test duration. Data supporting this reduction shall be available to the acquiring and qualifying activities upon request.

* J.3.6 Final electrical measurements. Final electrical testing of microcircuits shall assure that the microcircuits tested meet the electrical requirements of the device specification and shall include the tests of group A, subgroups 1, 2, 3, 4, or 7, 5 and 6 or 8, and 9, 10, and 11, unless otherwise specified in the device specification.

* J.3.7 Seal (fine and gross leak) testing. Fine and gross leak seal tests shall be performed, as specified in 4.2, between temperature cycling and final electrical testing after all shearing and forming operations on the terminals in accordance with MIL-STD-883, test method 1014.

J.3.8 Pattern failures. Pattern failure criteria may be used as an option for any screen provided that preburn-in testing is done. When acceptance is based on pattern failures (multiple device failures - two or more caused by the same basic failure mechanism) shall apply as specified in the acquisition document. If not otherwise specified, the maximum allowable failures shall be 5 devices for each failure pattern established. Accountability shall include burn-in through final electrical test.

J.3.8.1 Pattern failure rejects. When the number of pattern failures exceeds the specified limits, the burn-in lot shall be rejected. At the manufacturer's TRB option, the rejected lot may be resubmitted to burn-in one time provided:

a. The cause of the failure has been determined and evaluated.

b. Appropriate and effective corrective action has been completed to reject all microcircuits affected by the failure cause.

c. Appropriate preventive action has been initiated.

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* J.3.9 TCI. TCI testing shall be accomplished by the manufacturer on a periodic basis to assure that the manufacturer's quality, reliability, and performance capabilities meet the requirements of the QM plan. The manufacturer of QML microcircuits shall be certified by the qualifying activity to use one or a combination of both of the TCI procedures described below. The two TCI procedures are end-of-line TCI (option 1) and in-line control (option 2).

NOTE: All tests may not be appropriate for the technology (e.g., for wafer or die product group B subgroups 1 and 3 and group D do not apply). The manufacturer's TRB shall determine that the appropriate tests are completed to assure conformance of the product to be delivered.

* J.3.9.1 General. Any QML or SEC integrated circuit used for either TCI option (see J.3.10 or J.3.11) must be screened in accordance with 4.2.

* J.3.9.2 TCI reporting. Summary of TCI tests analysis shall be submitted to the qualifying activity in accordance with 3.9.1 requirements. If TCI requirements are not met, the TRB shall notify the qualifying activity immediately and all products manufactured and delivered between the last TCI and the failed TCI shall be placed in suspect status. The manufacturer shall analyze the failure, determine the reason for failure and submit a corrective action plan. An assessment of whether to recall all suspect products shall be made by the TRB and the qualifying activity shall be notified of the decision. Recertification and requalification of the QML line may be required based on the nature of the problem and action taken by the manufacturer. Procedures for standard TCI and in-line control for a QML line are described in the following paragraphs.

* J.3.10 End-of-line Technology Conformance Inspection (option 1). End-of-line QCI testing shall be performed every QCI interval, as recommended in table J-1 herein. QCI requirements as detailed in MIL-STD-883 test method 5005 may be used, with qualifying activity approval, in place of the QCI requirements herein. Each end-of-line QCI vehicle shall pass the end-of-line quality conformance. All groups A, B, and E (as applicable) testing shall be performed on microcircuits to be delivered as QML microcircuits. Groups C and D testing shall be done on either the SEC or QML microcircuits. Groups A, B, C, D, and E requirements are found in tables II through V and table C-I.

Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.4.3). RHA quality conformance inspection sample tests shall be performed at the level(s) specified and in accordance with appendix C. The applicable subgroups of group E, (see appendix C) shall be performed when specified in the acquisition document. The actual devices used for group E testing shall be assembled in a qualified package and, as a minimum, shall pass group A, subgroups 1, 7, and 9 at +25°C prior to irradiation.

* NOTE: If a manufacturer elects to eliminate a quality conformance inspection step by substituting an in-process control or statistical process control procedure, the manufacturer is only relieved of the responsibility of performing the QCI operation associated with that step. The manufacturer is still responsible for providing a product which meets all of the performance, quality, and reliability requirements herein and in the device specification. Documentation supporting substitution for QCI shall be retained by the manufacturer and available to the qualifying activity upon request.

Each group may contain individual subgroups for the purposes of identifying individual tests or groups of tests. Subgroups within a group of tests may be performed in any sequence but individual tests within a subgroup (except group B, subgroup 2) shall be performed in the sequence indicated for groups B, C, D, and E tests herein. Electrical reject devices from the same inspection lot may be used for all subgroups when electrical end-point measurements are not required.

* J.3.10.1 Group A inspection. Group A inspection shall be performed on each inspection lot and shall consist of electrical parameter tests specified for the specified device. Group A inspection may be performed in any order.

* J.3.10.2 Group B inspection. Group B inspection shall be performed on each inspection lot, for each qualified package type and lead finish. Group B shall consist of mechanical and environmental tests for the specified device class. Resubmission procedures shall be documented in the QM plan. For solderability, a statistical sound sample size (sample sizes indicated in MIL-STD-883 TM 5005 are acceptable, as a minimum) consisting of leads from several packages shall be tested with zero failures. The actual number shall be determined by the TRB and detailed in the TCI procedures in the QM plan.

* J.3.10.3 Group C inspection. Group C inspection shall include die-related tests specified which are performed periodically. Resubmission procedures shall be documented in the QM plan. Where group C end-points are done on actual devices, group C end-points shall be specified in the device specification.

* J.3.10.4 Group D inspection. Group D inspection shall include package related tests which are performed periodically. Resubmission procedures shall be documented in the QM plan. Where group D end-points are done on actual devices, group D end-points shall be specified in the device specification.

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* J.3.10.5 Group E inspection. When applicable, group E inspection shall include radiation hardness assurance tests on each wafer lot. The PIPL, transient and SEP response (as applicable), and test conditions shall be as specified in the device specification.

* J.3.10.6 End-point tests for groups C, D, (E if applicable). End-point measurements and other specified post-test measurements shall be made for each sample after completion of all other specified tests in the subgroup. The test limits for the end-point measurements shall be the same as the test limits for the respective group A subgroup inspections. Different end-points may be specified for group E tests in the detail specifications. Any additional end-point electrical measurements may be performed at the discretion of the manufacturer.

* J.3.10.7 End-of-line TCI testing (option 1). All microcircuits used in end-of-line TCI testing that meet the requirements of this document and the device specification and are subjected to destructive tests or which fail any test shall not be shipped on the contract or purchase order as acceptable QML product. They may, however, be delivered at the request of the acquiring activity if they are isolated from, and clearly identified so as to prevent their being mistaken for acceptable product. Sample microcircuits, from lots which have passed quality assurance inspections or tests and which have been subjected to mechanical or environmental tests specified in groups B, C, and D inspection and not classified as destructive, may be shipped on the contract or purchase order provided the test has been proven to be nondestructive (see A.4.3.2.3) and each of the microcircuits subsequently passes final electrical tests in accordance with the applicable device specification.

* TABLE J-I. End-of-line TCI testing procedure (option 1). 1/

Table	TCI requirements	TCI vehicle	Interval
Table III	Group A electrical testing	Actual device	Each inspection lot
Table II	Group B testing	Actual device	Each inspection lot
Table IV	Group C testing	SEC or actual device	Every 3 months
Table V	Group D testing	SEC or actual device	Every 6 months
Table C-I	Group E testing	Actual device	Each wafer lot

1/ Each group may contain individual subgroups for the purposes of identifying individual tests or groups of tests.

* J.3.11 In-line TCI testing (option 2). In-line control testing shall be performed through the use of the approved SEC or QML microcircuit. The in-line control test plan shall show how all the groups A, B, C, D, and E test conditions are incorporated under SPC or process control to allow in-line control monitoring. The following shall also be addressed.

* J.3.11.1 Group A electrical testing. Group A electrical testing shall be satisfied by in-line inspections performed in accordance with the applicable procedure of MIL-STD-883 on actual devices.

* J.3.11.2 Group C life tests. Life tests shall be performed on the SEC at intervals set by the TRB in the quality management plan.

* J.3.12 Test optimization. The process used by the manufacturer to optimize testing utilizing the best commercial practices available while still assuring all performance, quality and reliability requirements herein. Any screen or TCI (QCI) test prescribed herein may be reduced, modified, moved or eliminated by the QML manufacturer provided the following considerations are addressed as a minimum.

a. Nodes critical to test outcome, called test critical nodes, have been identified and are in control in accordance with EIA-557-A.

b. Test critical nodes have exhibited sufficient capability to assure low product defect rates.

c. An understanding and control of assignable causes at test critical nodes.

d. The long term reliability of devices remains unaffected or is improved.

e. Low defect rates in the process and delivered product are maintained.

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f. Measurements taken for out of control conditions along with corrective actions are recorded and this data is maintained for a time period consistent with data retention requirements herein.

The manufacturer is expected to maintain the established process control and evaluate the effect on quality and reliability of any out of control conditions that may exist at critical nodes. The manufacturer must also evaluate if a relationship exists between any optimized test and any field failure returns, take appropriate corrective actions, and report this information as part of the TRB status reports. Regardless of testing modifications the manufacturer shall supply product capable of passing any screening or TCI (QCI) test prescribed herein. As a part of the QML philosophy and the conversion of customer requirements the manufacturer must communicate variations in screening, end-of-line testing with customers as appropriate. This information should be accessible via the manufacturers QM plan and is available from the qualifying activity.

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