Downloaded from http://www.everyspec.com

INCH-POUND
MIL-PRF-32159
w/ AMENDMENT 3
6 December 2007
SUPERSEDING
MIL-PRF-32159
w/ AMENDMENT 2
9 September 2005

PERFORMANCE SPECIFICATION

RESISTORS, CHIP, FIXED, FILM, ZERO OHM, INDUSTRIAL, HIGH RELIABILITY, SPACE LEVEL, GENERAL SPECIFICATION FOR

This specification is approved for use by all Departments and Agencies of the Department of Defense.

1. SCOPE

1.1 Scope. This specification covers the general requirements for fixed, film, chip resistors primarily intended for incorporation into surface mount applications. This specification has three product levels, a space level "T" part number with 100 percent burn-in and screening, a high reliability 100 percent screened "M" part number level, and a part level "C" using the manufacturer's inspection system to validate conformance (see 1.2.1).

1.2 Classification.

1.2.1 Part or Identifying Number (PIN). Resistors specified herein (see 3.1) are identified by a PIN which consists of the basic number of the associated specification. Each associated specification covers a different resistor style. The number is coded to provide information concerning the level of burn-in screening of the resistor and termination material. The PIN is in the following form.

M32159	B	01	C
Specification indicating MIL-PRF-32159	Termination material (see 1.2.3)	Specification sheet number indicating MIL-PRF-32159/1	Product level Designator (see 1.2.4)

1.2.2 Style. The style (see 3.1) is identified by the three-letter symbol "RCZ" followed by a four digit number; the letters identify fixed, film, chip, zero ohm resistors, in a flat chip configuration.

1.2.3 Termination material. The termination material is in accordance with table I.

1.2.4 Product level designator. The product level designator is identified by a single letter which denotes an industrial grade resistor (C), and military grade resistor (M), or a space level resistor (T).

Comments, suggestions, or questions on this document should be addressed to Defense Supply Center Columbus, ATTN: DSCC-VAT, Post Office Box 3990, Columbus, OH 43218-3990, or emailed to Resistor@dla.mil. Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at http://assist.daps.dla.mil.

Downloaded from http://www.everyspec.com

TABLE I. Termination materials.

Type	Material	Termination area	Code letters
Solderable 1/	Base metallization barrier metal, solder coated	Wraparound 2/	B
Epoxy bondable	Gold	Wraparound 2/	G
	Platinum gold	Wraparound 2/ One surface	U T
	Palladium/silver or Platinum/silver	Wraparound 2/	C
	Palladium/silver or Platinum/silver	One surface	D

1/ Solderable termination's will be pretinned (see 3.5.3) for solder reflow operation and will meet the solderability test. The pretinning will be, as a minimum, on at least the bottom and ends of the chip and only those surfaces must meet the solderability test (see figure 2).

2/ Wrap-around type will be illustrated on the associated specifications.

2. APPLICABLE DOCUMENTS

2.1 General. The documents listed in this section are specified in sections 3 and 4 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as samples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements documents cited in sections 3 and 4 of this specification, whether or not they are listed.

2.2 Government documents.

2.2.1 Specifications, standards, or handbooks. The following specifications, standards, or handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-202 - Electronic and Electrical Components Parts.
MIL-STD-790 - Standard Practice for Established Reliability and High Reliability Qualified Products List (QPL) Systems for Electrical, Electronic, and Fiber Optic Parts Specifications.
MIL-STD-1285 - Marking of Electrical and Electronic Parts.

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or http://assist.daps.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

Downloaded from http://www.everyspec.com

2.2.2 Other Government documents, drawings, and publications. The following other Government documents, drawings, and publications form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION (NASA)

NASA 1124 - Outgassing Data for Selecting Spacecraft Materials.

(Hard copies of this document are no longer available from the NASA Goddard Materials Branch or the Document Automation and Production Service Detachment Office (DAPS). This information is only available at http://outgassing.nasa.gov.

2.3 Non-Government publications. The following documents form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents are those cited in the solicitation or contract.

AMERICAN SOCIETY FOR TESTING AND MATERIALS (ASTM)

ASTM E595 - Total Mass Loss and Collected Volatile Condensable Materials from Outgassing in a Vacuum Environment.

(Application for copies are available online at www.astm.org or can be obtained through the American Society for Testing and Materials (ASTM), 1916 Race Street, Philadelphia, PA 19103.)

IPC-ASSOCIATION CONNECTING ELECTRONICS INDUSTRIES (IPC)

IPC-CC-830B - Qualification and Performance of Electrical Insulation Compound for Printed Wiring Assemblies

(Application for copies are available online at www.ipc.org or can be obtained through the IPC-Association Connecting Electronics Industry, 2215 Sanders Road, suite 200 South, Northbrook, IL 60062-6135.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

2.4 Order of precedence. In the event of a conflict between the text of this document, and the references cited herein (except for related specification sheets) the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

Downloaded from http://www.everyspec.com

3. REQUIREMENTS

3.1 Specification sheets. The individual item requirements shall be as specified herein and in accordance with the applicable specification sheet. In the event of any conflict between the requirements of this specification and the specification sheet, the latter shall govern.

3.2 Qualification. Resistors furnished under this specification shall be products that are authorized by the qualifying activity for listing on the applicable qualified products list (QPL) before contract award. In addition, the manufacturer shall obtain certification from the qualifying activity that the product assurance requirements of 4.2.1 have been met and are being maintained. Authorized distributors that are approved to MIL-STD-790 distributor requirements by the QPL manufacturer are listed in the QPL.

3.3 QPL system. The manufacturer shall establish and maintain a QPL system for parts covered by this specification. Requirements for this system are specified in MIL-STD-790 and herein.

3.4 Materials. Materials shall be used which will enable the resistors to meet the performance requirements of this specification. Acceptance or approval of any constituent material shall not be construed as a guaranty of the acceptance of the finished product.

3.5 Interface and physical dimension requirements. Resistors shall meet the interface and physical dimensions specified (see 3.1).

3.5.1 Termination. Unless otherwise specified, both terminations (areas) shall be available on one surface of the body of the resistor chip (see 1.2.3).

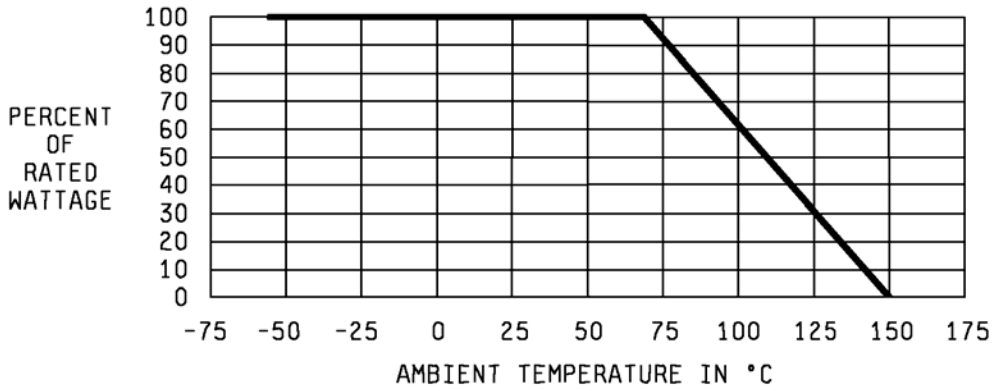
3.5.2 Barrier metallization. The barrier metallization for the B termination (base metallization barrier metal, solder coated) shall be nickel. The metallization shall be a minimum of 50 microinches.

* 3.5.3 Pure tin. The use of pure tin, as an underplate or final finish is prohibited both internally and externally. Tin content of resistor components and solder shall not exceed 97 percent, by mass. Tin shall be alloyed with a minimum of 3 percent lead, by mass (see 6.4.4).

3.6 Power rating. The resistors shall have a power rating based on continuous full-load operation at an ambient temperature of 70°C. For operation at temperatures in excess of 70°C the load shall be derated in accordance with figure 1.

NOTE: With a maximum resistance limit, the actual resistance value could vary. Therefore a single test voltage based on wattage and a maximum resistance could cause lower value jumpers to be overpowered.

Downloaded from http://www.everyspec.com



NOTE: This curve indicates the percentage of nominal wattage to be applied at temperature higher than 70°C. This curve applies only to units mounted on a board (see 4.8.1.3); however, at no time shall the current exceed the maximum for each style (see 3.1).

FIGURE 1. Derating curve for high ambient temperatures.

3.7 Current rating. The current rating shall be as specified herein (see 3.1).

3.8 DC resistance (by termination). When resistors are tested as specified in 4.8.2, the dc resistance shall not exceed the maximum resistance specified (see 3.1).

3.8.1 Resistance value deviations. All maximum deviations as specified in this section are to be considered absolute limits with the exception of the contact resistance adjustments.

3.9 Thermal shock.

3.9.1 Thermal shock (high reliability). When resistors are tested as specified in 4.8.3, there shall be no evidence of mechanical damage; the resistance shall not exceed the maximum resistance value specified (see 3.1).

3.9.2 Thermal shock (space level). When resistors are tested as specified in 4.8.3, there shall be no evidence of mechanical damage; the resistance for thermal shock and power conditioning combined shall not exceed the maximum resistance value specified (see 3.1).

3.10 Power conditioning (space level only). When resistors are tested as specified in 4.8.4, there shall be no evidence of mechanical damage; the resistance for thermal shock and power conditioning combined shall not exceed the maximum resistance value specified (see 3.1).

3.11 Low temperature operation. When resistors are tested as specified in 4.8.5, there shall be no evidence of mechanical damage, the change in resistance between the initial and final measurement made at 25°C ±5°C, shall not exceed the maximum resistance value specified (see 3.1).

3.12 Short time overload. When resistors are tested as specified in 4.8.6, there shall be no evidence of arcing, burning, or charring; the resistance shall not exceed the maximum resistance value specified (see 3.1).

Downloaded from http://www.everyspec.com

3.13 High temperature exposure. When resistors are tested as specified in 4.8.7, there shall be no evidence of mechanical damage; the resistance shall not exceed the maximum resistance value specified (see 3.1).

3.14 Resistance to soldering heat. When resistors are tested as specified in 4.8.8, there shall be no evidence of mechanical damage, no demetallization or leaching; the change in resistance shall not exceed the maximum value specified (see 3.1).

3.15 Resistance to bonding exposure. When resistors are tested as specified in 4.8.9, there shall be no evidence of mechanical damage; the resistance shall not exceed the maximum resistance value specified (see 3.1).

3.16 Moisture resistance. When resistors are tested as specified in 4.8.10, there shall be no evidence of mechanical damage; the resistance shall not exceed the maximum resistance value specified (see 3.1).

3.17 Life. When resistors are tested as specified in 4.8.11, there shall be no evidence of mechanical damage. The change in resistance value at the initial measurement and any succeeding measurements up to and including 2,000 hours shall not exceed the maximum value specified (see 3.1).

3.18 Solderability (applicable to termination B). When resistors are tested as specified in 4.8.12, the immersed metallized surface shall be at least 95 percent covered with a new clean smooth coating and shall exhibit no demetallization or leaching of the terminal areas. The remaining 5 percent may contain only small pinholes or rough spots; these shall not be concentrated in one area. In case of dispute, the percentage of coverage with pinholes or rough spots shall be determined by actual measurement of these areas, as compared to the total area. The top surface of the solder pad need not be considered in the evaluation for solderability (see figure 2). For coverage calculations, defective areas on each termination shall be compared to the total area of the end and bottom surfaces on the same termination.

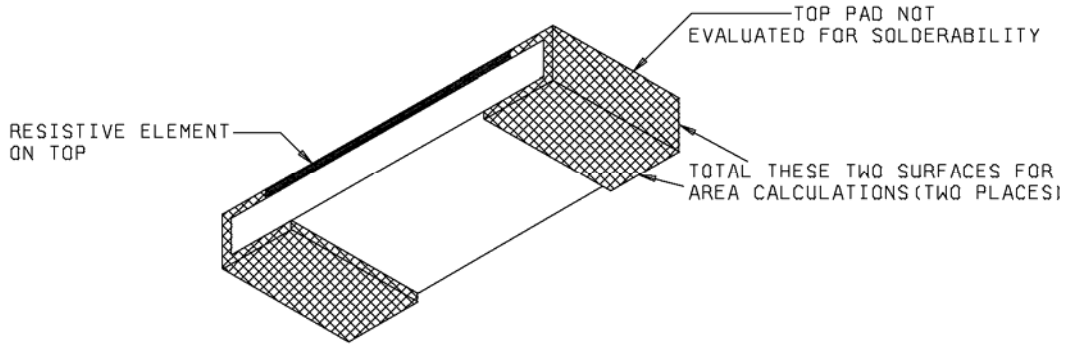
3.19 Mounting integrity.

3.19.1 Solder mounting integrity (applicable to termination B). When resistors are tested as specified in 4.8.13.1, there shall be no evidence of mechanical damage.

3.19.2 Bondable mounting integrity (applicable to termination's G, U, T, C, and D). When resistors are tested as specified in 4.8.13.2, there shall be no evidence of mechanical damage.

3.20 Resistance to solvents (applicable to resistors that are screen printed). When resistors are tested as specified in 4.8.14, there shall be no evidence of mechanical damage and the marking shall remain legible.

Downloaded from http://www.everyspec.com



NOTES:
1. Top solder pad need not be evaluated for solderability.
2. Resistive element on top.
3. Ends and bottom are surfaces to be evaluated.

FIGURE 2. Solderability coverage.

3.21 Marking legibility.

3.21.1 Marking legibility test (applicable to laser marked resistors). When resistors are tested as specified in 4.8.15, the marking shall remain legible.

3.22 Outgassing (space level only). When examined as specified in 4.8.16, the samples shall meet the following requirements:

a. Total Mass Loss (TML) shall not exceed 1 percent.

b. Volatile Condensable Material (VCM) shall not exceed 0.1 percent.

3.22.1 Outgassing test data (see 2.2.2). Data listed in NASA Publication 1124 may be used in lieu of actual test data for applicable materials.

3.23 Recycled, recovered, or environmentally preferable materials. Recycled, recovered, or environmentally preferable materials should be used to the maximum extent possible provided that the material meets or exceeds the operational and maintenance requirements, and promotes economically advantageous life cycle costs.

3.24 Visual inspection. Resistors shall be inspected as specified in 4.8.1, to verify that the interface, physical dimensions, marking, and workmanship are in accordance with the applicable requirements (see 3.1, 3.4, 3.5, 3.5.1 to 3.5.3 inclusive, and appendix B).

Downloaded from http://www.everyspec.com

3.25 Marking. A noncorrosive label containing the following information shall be applied to each unit package. PIN, "JAN" marking, date code, and source code. Date and source code shall be in accordance with MIL-STD-1285. The following is an example of the complete marking:

12345	-	CAGE
0312J	-	Date code and JAN marking
M3215901B	-	PIN

The date code shall be the date of the final assembly operation. The common manufacturing record shall include the same date code as that placed on the parts covered by the record. At the option of the manufacturer, resistors may be marked (i.e., laser or screen printed). The marking process must be approved by the qualifying activity based on testing specified herein. The marking shall remain legible after all tests.

3.25.1 Individual chip marking. Marking of individual chip resistors is not required but is permitted. Chip resistors may be marked using the following code system. The marking requirement shall be specified on the order.

T	0	J
Inspection Level (T, M, or C)	Zero ohm	JAN marking

3.25.2 JAN and J marking. The United States Government has adopted, and is exercising legitimate control over the certification marks "JAN" and "J", respectively, to indicate that items so marked or identified are manufactured to, and meet all the requirements of specifications. Accordingly, items acquired to, and meeting all of the criteria specified herein and in applicable associated specifications shall bear the certification mark "JAN" except that items too small to bear the certification mark "JAN" shall bear the letter "J". The "JAN" or "J" shall be placed immediately before the part number except that if such location would place a hardship on the manufacturer in connection with such marking, the "JAN" or "J" may be located on the first line above or below the part number. Items furnished under contracts or orders which either permit or require deviation from the conditions or requirements specified herein or in applicable associated specifications shall not bear "JAN" or "J". In the event an item fails to meet the requirements of this specification and the applicable specification sheets or associated specifications, the manufacturer shall remove completely the military part number and the "JAN" or "J" from the sample tested and also from all items represented by the sample. The “JAN” or “J” certification mark shall not be used on products acquired to contractor drawings or specifications. The United States Government has obtained Certificate of Registration Number 504,860 for the certification mark "JAN" and Registration Number 1,586,261 for the certification mark “J”.

3.25.3 Supplying to higher product levels. A manufacturer may supply to all higher product levels to which they are qualified. Parts qualified to lower product levels (i.e., more stringent), with acquiring agency approval, are substitutable for higher product levels as long as the label reflects the original product level ordered (see table II). Parts that are physically marked shall not be remarked unless specified in the contract or order (see 6.2).

Downloaded from http://www.everyspec.com

TABLE II. Substitution data.

Product level	Acceptable substitute
T (Space)	-----
M (HR)	T
C (Ind)	M, T

3.26 Workmanship. Resistors shall be processed in such a manner as to be uniform in quality and shall meet the requirements of 3.1, 3.4, 3.5, 3.5.1 through 3.5.3 inclusive, and 3.25 as applicable, and be free from other defects that will affect life, serviceability, or appearance, and shall pass the visual inspection as specified on figure B-1 and figure B-2 in appendix B.

4. VERIFICATION

4.1 Classification of inspections. The inspection requirements specified herein are classified as follows:

a. Qualification inspection (see 4.4).

b. Verification of qualification (see 4.5).

c. Conformance inspection (see 4.6).

d. Periodic Group C inspection (see 4.7)

4.2 Reliability and quality.

4.2.1 QPL system. The manufacturer shall establish and maintain a QPL system as described in 3.3. Evidence of such compliance is a prerequisite for qualification and verification of qualification.

4.3 Inspections conditions and precautions.

4.3.1 Inspection conditions. Unless otherwise specified herein, all inspections shall be performed in accordance with the test conditions specified in the general requirements of MIL-STD-202.

4.3.2 Precautions. Adequate precautions shall be taken during inspection to prevent condensation of moisture on resistors, except during the moisture resistance temperature cycling tests.

4.4 Qualification inspection. Qualification inspection shall be performed at a laboratory acceptable to the Government (see 6.3).

4.4.1 Sample. The number of sample units comprising a sample of resistors to be submitted for qualification inspection shall be as specified in appendix A to this specification. The sample shall be taken at random from a production run and shall be produced with equipment and procedures normally used in production and which have been subjected to and passed the requirements of group A inspection (see 4.6.3). Qualification shall not be granted if group A inspection requirements are not complied with.

Downloaded from http://www.everyspec.com

4.4.2 Test routine. Sample units shall be subjected to the qualification inspection specified in table III in the order shown. All sample units, with the exception of ten sample units for group V inspection, shall be subjected to the inspection of group I. The 182 sample units shall be divided as specified in table III for group II, group III, group IV, and group VI and subjected to the inspection for their particular group. Twenty sample units shall be submitted to group VII, if applicable. Sample sizes and extent of qualification shall be specified in appendix A of this specification.

4.4.3 Defective. Defectives in excess of those allowed in table III shall be cause for refusal to grant qualification.

4.5 Verification of qualification. Every 6 months the manufacturer shall provide verification of qualification to the qualifying activity. Continuation of qualification is based on meeting the following requirements.

a. MIL-STD-790 program.

b. Design of resistor has not been modified.

c. Lot rejection for group A (subgroup 2 and subgroup 4) does not exceed 5 percent or one lot, whichever is greater.

d. Periodic group C inspection requirements are met.

e. Continued qualification to the non burn-in “C” level shall be based on continued maintenance of qualification for the “M” level part.

4.6 Conformance inspection.

4.6.1 Inspection of product for delivery.

4.6.1.1 “C” level. The manufacturer’s inspection system shall be used for preparation for delivery.

4.6.1.2 “M” level. Inspection of product for delivery shall consist of group A (power conditioning does not apply) and group B inspections. Group B inspection for preparation of delivery is not required when the qualifying activity has allowed group B testing to be performed annually (see table VI).

4.6.1.3 ”T” level. Inspection of product for delivery shall consist of group A and group B inspections and shall be performed on production lot basis. Test deletion or reduction, which may be granted for “M” level product, is not allowed for space level product.

4.6.2 Inspection lot. An inspection lot shall consist of all resistors of the same style and termination type manufactured under essentially the same process and conditions with the same basic materials and offered for inspection at one time. All product level lots shall be kept separate.

4.6.2.1 Production lot. A production lot shall consist of a group of resistors manufactured during the same period from the same materials, under the same specifications and procedures. These resistors shall be produced using the same processes and process equipment. The manufacturer’s documentation shall define the qualified production system through all significant manufacturing operations, including final assembly.

Downloaded from http://www.everyspec.com

TABLE III. Qualification inspection.

Inspection	Requirement Paragraph	Method paragraph	Number of samples	Number of defects allowed
Certification requirements				
Outgassing (space level only)	3.22	4.8.16	---	---
Group I				
Visual and mechanical inspection	3.1, 3.4, 3.5, 3.5.1 through 3.5.3 inclusive, 3.24, and 3.25	4.8.1	All sample units except group V	0
DC resistance	3.8	4.8.2		
Group II				
Resistance to soldering heat	3.14	4.8.8	30	1
Resistance to bonding exposure	3.15	4.8.9		
Low temperature operation	3.11	4.8.5		
Short time overload	3.12	4.8.6		
High temperature exposure	3.13	4.8.7		
Group III				
Resistance to soldering heat	3.14	4.8.8	30	1
Resistance to bonding exposure	3.15	4.8.9		
Moisture resistance	3.16	4.8.10		
Group IV				
Life	3.17	4.8.11	102	1
Group V				
Solderability 1/	3.18	4.8.12	10	1
Group VI				
Solderable mounting integrity 1/	3.19.1	4.8.13.1	20	1
Bondable mounting integrity 2/	3.19.2	4.8.13.2		
Group VII				
Resistance to solvents 3/	3.20	4.8.14	20	0
Marking legibility test (laser marking) 4/	3.21.1	4.8.15		
Group VIII (space level only)				
Thermal shock (100 cycles)	3.9	4.8.3	30	0

1/ Applicable to termination B.
2/ Applicable to termination G, U, T, C, and D.
3/ Test applicable for non-laser marked parts.
4/ Test applicable for laser marked parts.

Downloaded from http://www.everyspec.com

4.6.3 Group A inspection.

4.6.3.1 "C" level part. The manufacturer shall establish and maintain an inspection system to verify that resistors meet dc resistance, visual/mechanical, and solderability requirements. In-line or process controls may be part of such a system. The inspection system shall also include criteria for lot rejection and corrective action. (NOTE: Since the "C" level network is the "M" level design without the mandatory conformance inspection system, this product is still expected to meet the environmental qualification type requirements (e.g., moisture resistance and thermal shock).

4.6.3.2 "M" level and "T" level part. Group A inspection shall consist of the inspections specified in table IV.

4.6.3.2.1 Subgroup 1 test (precap visual). The subgroup 1 test shall be performed on a production lot basis. Thirteen samples shall be subjected to subgroup 1. In the event of one or more failures, the lot shall be rejected.

4.6.3.2.1.1 Rejected lots. In the event of one or more defects, the production lot is rejected and the rejected production lot(s) shall be submitted to a 100 percent precap visual inspection as specified in 3.24. Resistors that pass precap visual inspection are available to continue group A testing.

4.6.3.2.2 Subgroup 2 tests. Subgroup 2 tests shall be performed on a production lot basis on 100 percent of the product supplied under this specification. Resistors that exceed the maximum resistance allowed (see 3.1) shall be removed from the lot. Lots having more than 5 percent total rejects shall not be furnished on contracts.

4.6.3.2.2.1 Manufacturer's production inspection. If the manufacturer performs tests similar to those specified in subgroup 2, table IV, as the final step of his production process, group A, subgroup 2 inspection may be waived. Authority to waive the subgroup 2 inspection shall be granted by the qualifying activity only. The following criteria must be complied with:

a. Tests conducted by the manufacturer during production shall be clearly identical to or more stringent than those specified for subgroup 2. Test conditions shall be equal to or more stringent than those specified for subgroup 2 tests.

b. Manufacturer subjects 100 percent of the product supplied under this specification to his production tests.

c. The parameters measured and the failure criteria shall be the same as, or more stringent than, those specified herein.

d. The lot rejection criteria are the same as, or more stringent than, those specified herein.

e. Once approved, the manufacturer shall not change the test procedures or criteria without prior notification to and concurrence from the qualifying activity.

Downloaded from http://www.everyspec.com

TABLE IV. Group A inspection.

Inspection	Requirement paragraph	Method paragraph	Sampling Procedure
Subgroup 1			
Precap visual inspection 1/	3.24	4.8.1	4.6.3.2.1
Subgroup 2			
Thermal shock 2/	3.9	4.8.3	
Power conditioning (space level only)	3.10	4.8.4	4.6.3.2.2
DC resistance	3.8	4.8.2	
Subgroup 3			
Visual inspection	3.1, 3.4, 3.5 through 3.5.3 inclusive, and 3.24	4.8.1	4.6.3.2.3
Subgroup 4			
Solderability 3/	3.18	4.8.12	4.6.3.2.4
Subgroup 5 4/			
Resistance to solvents 5/	3.20	4.8.14	4.6.3.2.5
Marking legibility 6/	3.21	4.8.15	

1/ Precap visual inspection shall be performed when the resistance element can not be inspected after passivation/glassivation in subgroup 3.

2/ If the manufacturer can demonstrate that these tests have been performed five consecutive times with zero failures, the frequency of these tests, with the approval of the qualifying activity, can be performed on a annual basis. If the design, material, construction, or processing of the part is changed or if there are any quality problems or failures, the qualifying activity may require resumption of the original test frequency. (NOTE: Not applicable to space ("T") level product since test deletion or reduction of space level product is not allowed.)

3/ The manufacturer may request the deletion of the subgroup 4 solderability test, provided an in-line or process control system for assessing and assuring the solderability of terminations can be validated and approved by the qualifying activity. Deletion of the test does not relieve the manufacturer from meeting this test requirement in case of dispute. If the design, material, construction, or processing of the part is changed or if there are any quality problems, the qualifying activity may require resumption of the test. (NOTE: Not applicable to space ("T") level product since test deletion or reduction of space level product is not allowed.)

4/ If the manufacturer can demonstrate that these tests have been performed five consecutive times with zero failures, the frequency of these tests, with the approval of the qualifying activity, can be performed on a annual basis. If the design, material, construction, or processing of the part is changed or if there are any quality problems or failures, the qualifying activity may require resumption of the original test frequency. (NOTE: Not applicable to space ("T") level product since test deletion or reduction of space level product is not allowed.)

5/ Test applicable for non-laser marked parts.

6/ Test applicable for laser marked parts.

Downloaded from http://www.everyspec.com

4.6.3.2.3 Subgroup 3 (visual inspection). The subgroup 3 test shall be performed on an inspection lot basis for product level M and production lot basis for space level product T. A sample of parts shall be randomly selected in accordance with table V. If one or more defects are found, the lot shall be reworked or screened and defectives removed. After reworking or screening and removal of defectives, a new sample of parts shall be randomly selected in accordance with table V. If one or more defects are found in this second sample for the same quality characteristic, the lot shall be rejected and shall not be supplied to this specification.

4.6.3.2.4 Subgroup 4 (solderability) test. The subgroup 4 test shall be performed on an inspection lot basis for product level M and production lot basis for space level product T. A sample shall be randomly selected from each lot in accordance with table V. As an option, the manufacturer may use electrical rejects from the subgroup 2 tests for all or part of the sample. If there are one or more defects, the lot shall be considered to have failed.

4.6.3.2.4.1 Rejected lots. In the event of one or more defects, the inspection lot is rejected. If the lot fails this solderability test, the lot may be reworked and retested. Any inspection lot that fails the solderability retest shall be considered to have failed and that lot will not be supplied to the requirements of the specification.

TABLE V. Sampling plans for subgroup 3 and subgroup 4.

Lot size	Sample size for subgroup 3	Sample size for subgroup 4
1 to 5	100%	100%
6 to 13	100%	5
14 to 150	13	5
151 to 280	20	5
281 to 500	29	5
501 to 1,200	34	5
1,201 to 3,200	42	5
3,201 to 10,000	50	8
10,001 to 35,000	60	13
35,001 to 150,000	74	20
150,001 to 500,000	90	20
500,001 and over	102	20

4.6.3.2.4.2 Disposition of samples. The solderability test is considered a destructive test and samples submitted to the solderability test shall not be supplied on the contract.

4.6.3.2.5 Subgroup 5. Eight samples shall be selected randomly from each inspection lot and subjected to the subgroup 5 tests. The manufacturer may use electrical rejects from the subgroup 2 screening tests for all or part of the samples to be used for the subgroup 5 testing. If there are one or more defects, the lot shall be considered to have failed.

Downloaded from http://www.everyspec.com

4.6.3.2.5.1 Rejected lots. In the event of one or more defects, the inspection lot shall be reworked or screened and defectives removed. An additional eight samples shall be randomly selected from each inspection lot and be tested. If there is one or more defects in the inspection lot sample, that inspection lot shall be considered to have failed and that product will not be supplied to the requirements of this specification. Individual inspection lots that pass the minimum marking test are available for shipment.

4.6.4 Group B inspection. Group B inspection shall consist of the inspections specified in table VI in the order shown, and shall be performed on samples from lots which have been subjected to and have passed the group A inspection. Group B inspection shall be performed on inspection lot basis.

4.6.4.1 Sampling plan.

4.6.4.2 Subgroup 1. Twenty sample units of parts shall be randomly selected from the inspection lot. If one or more defects are found, the lot shall be reworked or screened and defectives removed. After reworking or screening and removal of defectives, a new sample of 20 parts shall be randomly selected. If one or more defects are found in this second sample, the lot shall be rejected and shall not be supplied to this specification.

TABLE VI. Group B inspection (HR and space level).

Inspection	Requirement paragraph	Method paragraph	Number of samples
Subgroup 1 1/ Short time overload	3.12	4.8.6	20 samples
Subgroup 2 2/ Solder mounting integrity 3/ Bondable mounting integrity 4/	 3.19.1 3.19.2	 4.8.13.1 4.8.13.2	 10 samples 10 samples

1/ If the manufacturer can demonstrate that these tests have been performed five consecutive times with zero failures, the frequency of these tests, with the approval of the qualifying activity can be performed on an annual basis. If the design, material, construction, or processing of the part is changed or, if there are any quality problems or failures, the qualifying activity may require resumption of the original test frequency. (NOTE: Not applicable to space ("T") level product since test deletion or reduction of space level product is not allowed.)

2/ If the manufacturer can demonstrate that this test has been performed five consecutive times with zero failures, this test, with the approval of the qualifying activity, can be deleted. The manufacturer, however, shall perform this test every three years after the deletion as part of long term design verification. If the design, material, construction, or processing of the part is changed or, if there are any quality problems, the qualifying activity may require resumption of the specified testing. Deletion of testing does not relieve the manufacturer from meeting the test requirement in case of dispute. (NOTE: Not applicable to space ("T") level product since test deletion or reduction of space level product is not allowed.)

3/ Applicable to termination B.

4/ Applicable to termination's G, U, T, C, and D.

Downloaded from http://www.everyspec.com

4.6.4.3 Subgroup 2. A sample of ten parts for each test of subgroup 2 shall be randomly selected from the inspection lot. If one or more defects are found, the lot shall be reworked or screened and defectives removed. After reworking or screening and removal of defectives, a new sample of ten parts shall be randomly selected. If one or more defects are found in this second sample, the lot shall be rejected and shall not be supplied to this specification.

4.6.4.3.1 Disposition of sample units. Sample units which have been subjected to group B inspection shall not be delivered on the contract or order.

4.7 Periodic group C inspection. Group C inspection shall consist of the tests specified in table VII, in the order shown. Group C inspection shall be made on sample units selected from lots which have passed group A and group B inspection. Group C samples shall be representative of production. The allowable number of defectives shall be as indicated in table VII.

TABLE VII. Group C inspection.

Inspection	Requirement paragraph	Method paragraph	Number of samples	Number of defects allowed
Monthly Subgroup 1				
Life	3.17	4.8.11	10	0
Subgroup 2 1/				
Thermal shock Low temperature operation	3.9 3.11	4.8.3 4.8.5	30	1
Subgroup 3 1/				
Resistance to soldering heat Resistance to bonding exposure Moisture resistance	3.14 3.15 3.16	4.8.8 4.8.9 4.8.10	30	1
Subgroup 4 1/				
High temperature exposure	3.13	4.8.7	30	1

1/ If the manufacturer can demonstrate that these tests have been performed five consecutive times with zero failures, the frequency of these tests, with the approval of the qualifying activity, can be performed on a annual basis. If the design, material, construction, or processing of the part is changed or, if there are any quality problems or failures, the qualifying activity may require resumption of the original test frequency.

Downloaded from http://www.everyspec.com

4.7.1 Sampling plan. If more than 1,000 resistors of any style or style grouping are produced over the maintenance period, the group C tests shall be performed as specified. If the production rate is less than 1,000 resistors for any style or style grouping over the maintenance period, then the monthly group C inspection may be postponed until at least 1,000 resistors of that style or grouping are produced (except for the monthly life test). In any case, the monthly tests shall be performed at least once every 3 months. This requirement is waived if the manufacturer has obtained a reduced inspection status through the qualifying activity.

4.7.1.1 Monthly (subgroup 1). A minimum of ten sample units representative of production shall be subjected to the test of subgroup 1. No defects shall be allowed.

4.7.1.2 Monthly (subgroup 2). Subgroup 2 tests shall be performed on a minimum sample size of 30 units representative of production with one defective allowed for each group of 30.

4.7.1.3 Monthly (subgroup 3). Subgroup 3 tests shall be performed on a minimum sample size of 30 unit's representative of production with one defective allowed for each group of 30.

4.7.1.4 Monthly (subgroup 4). Subgroup 4 test shall be performed on a minimum sample size of 30 units representative of production with one defective allowed for each group of 30.

4.7.2 Noncompliance. If a sample fails to pass group C inspection, the contractor shall take corrective action on the materials or processes, or both, as warranted, and on all units of product which can be corrected and which were manufactured under essentially the same conditions, with essentially the same materials and processes, and which are considered subject to the same failure. Acceptance of the product shall be discontinued until corrective action, acceptable to the Government, has been taken. After the corrective action has been taken, group C inspection shall be repeated on additional sample units (all inspection, or the inspection which the original sample failed, at the option of the Government). Group A and group B inspections may be reinstituted; however, final acceptance shall be withheld until group C reinspection has shown that the corrective action was successful.

4.8 Methods of inspection.

4.8.1 Visual and mechanical inspection and chip mounting.

4.8.1.1 Visual and mechanical inspection. Unless otherwise specified, resistors shall be examined under 30X to 60X magnification. In case of conflict 30X will be the referee power, unless otherwise specified, to verify that the materials, design, construction, physical dimensions, and workmanship are in accordance with the applicable requirements (see 3.1, 3.4, 3.5, 3.5.1 through 3.5.3 inclusive, 3.24 and appendix B).

4.8.1.2 Chip mounting procedures. When specified herein, the chip resistor shall be mounted on a test board as described in 4.8.1.3. For those test procedures where mounting requirements are unspecified, the chip resistors may be tested unmounted using pressure contacts.

Downloaded from http://www.everyspec.com

4.8.1.3 Specified mounting. When specified in the test procedure, the chip resistor shall be mounted on a test board as suggested on figure 3. The test board material shall be such that it shall not be the cause of, nor contribute to, any failure of a chip resistor in any of the tests for which it may be used. The test board shall be prepared with metallized surface land areas of proper spacing so that a test board surface area of at least four times the resistor chip surface area is provided for each resistor chip mounted. The metallized surface land areas shall be designed in a pattern to accommodate a number of resistor chips. The metallization material shall be compatible with the bonding technique to be employed and the material used on the chip termination. The method of chip mounting for the different termination materials shall be as follows:

a. Termination B (solderable). Termination B chip resistors shall be mounted on the fiberglass test board by soldering the chip termination's directly to the test board metallized land areas in the following manner:

(1) Solder and soldering flux shall be of such a quality as to enable the chip resistors to meet all the requirements of this specification and shall be applied to the terminations of each chip of code letter B (see 1.2.3).

(2) All chips shall be placed across the metallized land areas of the test board with contact between the chip termination's and board land areas only. The use of adhesive to keep chips in place during mounting operation is allowable except for preparation of solder mounting integrity test pieces.

(3) For resistance to soldering heat, the test board with all chips in position shall be placed on a heat transfer unit (molten solder, hot plate, tunnel oven, etc.) with the temperature transitioned to 245°C ±5°C. The chips shall remain at 245°C ±5°C until the solder melts and reflows forming a homogenous solder bond.

(4) For load life, the test board with all chips in position shall be placed on a heat transfer unit (molten solder, hot plate, or tunnel oven) with time and temperature to assure proper reflow mounting.

b. Terminations G, U, T, C, and D (epoxy bondable). As an alternative to 4.8.1.3a(1), chip resistors may be mechanically attached to the ceramic test board with type 2 epoxy approved by the qualifying activity. The epoxy shall be cured at a minimum temperature of 150°C. The minimum curing time shall be 30 minutes.

4.8.1.3.1 Fiberglass base board. Fiberglass base boards can be FR-4, G-10, G-30, or equivalent. When specified, a fiberglass test board with copper lamination shall be used for testing. The copper lamination shall be 70 micrometers copper (2 ounce) thickness (maximum).

Downloaded from http://www.everyspec.com

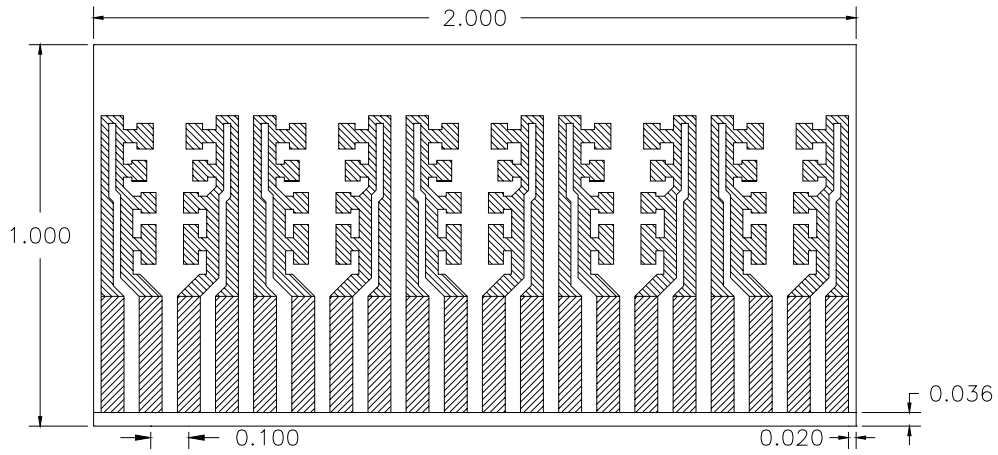
4.8.2 DC resistance (see 3.8). The dc resistance shall be measured in accordance with method 303 of MIL-STD-202. The following details and exceptions shall apply:

a. Measuring apparatus: Different types of measuring test equipment (multimeters, bridges, or equivalent) are permitted to be used on the initial and final readings of this test, provided the equipment is the same type, model, or if it can be shown that the performance of the equipment is equivalent or better.

b. Measurement energy for electronic test equipment: The measurement energy applied to the unit under test shall not exceed 10 percent of the 25°C rated wattage times 1 second.

c. Temperature: The dc resistance test specified in group I of table III shall be performed at 25°C ±2°C. For all other tests, unless otherwise specified herein, the temperature at which subsequent and final resistance measurements are made in each test shall be within ±2°C of the temperature at which the initial resistance measurement was made.

NOTE: In case of dispute, four wire Kelvin measurement shall be made as far from film as possible.



NOTES:
1. Suggested ceramic test board (e.g., 96 percent alumina): 2.000 inch (50.80 mm) x 1.000 inch (25.40 mm) x 0.025 inch (0.64 mm) thick.
2. Suggested fiberglass test board (e.g., G30 or FR-4 glass epoxy): 2.000 inch (50.80 mm) x 1.000 inch (25.40 mm) x .0625 inch thick (1.588 mm).
3. The contacts fit a printed circuit board connector with .100 inch (2.54 mm) in contact center.
4. Short lead wire may be soldered on and it will then fit a microcircuit connector, or test lead wires may soldered on for direct measurement.
5. Accommodates Kelvin four wire measurement.
6. A larger test board, to scale, may be used to accommodate additional test samples or additional style/size configurations.

FIGURE 3. Suggested test board.

Downloaded from http://www.everyspec.com

4.8.3 Thermal shock (see 3.9). Resistors shall be tested in accordance with method 107 of MIL-STD-202. The following details and exceptions apply:

a. Mounting: Resistors shall not be mounted. Resistors may be placed in metal baskets, vials, or other apparatus as long as resistors are subjected to the specified temperature extremes. (For group C inspection only, as an option to the manufacturers, resistors may be mounted or unmounted.)

b. Measurement before cycling:

(1) Qualification test: DC resistance shall be measured as specified in 4.8.2, except at 25°C ±5°C. The dc resistance shall be within the maximum value specified (see 3.1).
(2) Group C test: DC resistance shall be measured as specified in 4.8.2.

c. Test condition F (except temperatures shall be 150ºC +10ºC, -0ºC and -65ºC +0ºC, -10ºC).

d. Measurement after cycling:

(1) Qualification and group A tests: After stabilization at room temperature, the dc resistance shall again be measured as specified in 4.8.2, except at 25°C ±5°C.
(2) Group C test (not applicable for space level): After stabilization at room temperature, the dc resistance shall again be measured as specified in 4.8.2. Following the test, the resistors shall be examined for evidence of mechanical damage.

4.8.4 Power conditioning (space level only) (see 3.10). Chip resistors shall be tested in accordance with method 108 of MIL-STD-202. The following details and exceptions shall apply:

a. Test temperature: 70°C +5°C, -0°C.

b. Initial measurements: Measurements may be made inside or outside the chamber.

(1) Inside chamber: When measurements are to be made inside the chamber, the initial dc resistance shall be measured, at the applicable test temperature, after a 30 minute +90 minute, -15 minute stabilization period and within 8 hours of exposure of the chip resistors to the test temperature. This initial measurement shall be used as the reference temperature for all subsequent measurements under the same condition.

(2) Outside chamber: When measurements are to be made outside the chamber, the initial dc resistance shall be measured at room temperature. This measurement shall be used as the reference temperature for all subsequent measurements under the same condition.

c. Operating condition: A current shall be applied to the chip resistor intermittently, one and one-half hours “on” and one-half hour “off”, for 100 hours $\pm$4 hours and at the test temperature. During the “on” cycle, the current shall be regulated and controlled to within $\pm$5 percent. Unless otherwise specified (see 3.1), current applied shall be one and one-half times the rated current.

Downloaded from http://www.everyspec.com

d. Measurements after test: Following a minimum one-half hour stabilization period, dc resistance shall be measured as specified in 4.8.2.

e. Inspection after test: Chip resistors shall be inspected for evidence of mechanical damage.

4.8.5 Low temperature operation (see 3.11). A dc resistance measurement shall be made as specified in 4.8.2, mounted on a test board as specified in 4.8.1.3. The resistors shall be placed in a cold chamber maintained at -65°C +0°C, -5°C. . After stabilization at this temperature, the rated current as specified in 3.7 shall be applied for 45 minutes, +5 minutes, -0 minutes. Fifteen minutes +5 minutes, -0 minutes after the removal of the current, the resistors shall be removed from the chamber and maintained at a temperature of 25°C ±5°C until stabilized; the dc resistance shall be measured as specified in 4.8.2. Resistors shall be examined for evidence of mechanical damage.

4.8.6 Short time overload (see 3.12). The dc resistance shall be measured as specified in 4.8.2 and mounted on a test board as specified in 4.8.1.3. A dc test potential, 2.5 times the rated current (see 3.1), shall be applied for 5 seconds to the resistor under the following conditions:

a. Resistors on test board shall be mounted so that the larger space of the resistor is on a horizontal plane.

b. In still air, with no circulation other than that created by the heat of the resistors being operated.

The resistors shall be stabilized at a temperature of 25°C ±3°C after which the dc resistance shall be measured as specified in 4.8.2. Resistors shall be examined for evidence of arcing, burning, and charring.

4.8.7 High temperature exposure (see 3.13). Resistors shall be mounted on a test board as specified in 4.8.1.3 and the dc resistance shall be measured as specified in 4.8.2. The resistors shall then be subjected to a continuous temperature of 150°C ±5°C for a period of 100 hours ±4 hours, in a test chamber with forced air circulation. The resistors shall be stabilized at 25°C ±3°C after which the dc resistance shall be measured as specified in 4.8.2. The resistance shall not exceed the maximum value specified (see 3.1).

4.8.8 Resistance to soldering heat (B termination) (see 3.14). Resistors shall be tested in accordance with method 210 of MIL-STD-202. The following details and exceptions shall apply:

a. Measurement before test: DC resistance shall be measured as specified in 4.8.2.

b. Mounting and testing: Resistors shall be mounted on a fiberglass test board as specified in 4.8.1.3a(3) and this shall count as one heat cycle.

c. Second heat cycle: Test condition J, except this is the last heat cycle. (NOTE: When a hot plate is used, the temperature shall be 245°C ±5°C for 60 seconds, ±5 seconds and the temperature ramp and emersion/immersion rate does not apply.

Downloaded from http://www.everyspec.com

d. Measurement after test: After completion of the cleaning process and following a stabilization period at room temperature the dc resistance shall be measured as specified in 4.8.2. The resistance shall not exceed the maximum value specified (see 3.1).

e. Examination after test: Resistors shall be examined for evidence of mechanical damage.

4.8.9 Resistance to bonding exposure (terminations G, U, T, C, and D) (see 3.15). The dc resistance of the chip resistor shall be measured as specified in 4.8.2. The chip resistor shall be mounted on a test board in accordance with 4.8.1.3. The test board, with resistors mounted, shall be stabilized at room temperature after which the dc resistance shall again be measured as specified in 4.8.2. The resistance shall not exceed the maximum value specified (see 3.1).

4.8.10 Moisture resistance (see 3.16). Resistors shall be tested in accordance with method 106 of MIL-STD-202. The following details and exceptions shall apply:

a. Mounting: Chip resistor sample units shall be mounted on a test board as specified in 4.8.1.3.

b. Initial measurement: Immediately following the initial conditioning period, dc resistance of each chip on the test board shall be measured as specified in 4.8.2.

c. Subcycle: Step 7b shall not be applicable. Step 7a shall be performed during any five of the first nine cycles only.

d. Measurements at high humidity: None.

e. Final measurements: Upon completion of step 6 of the final cycle, the resistors shall be removed from the chamber and air dried for 30 minutes, +90 minutes, -15 minutes. The dc resistance shall then be measured in accordance with 4.8.2.

f. Examination after test: Resistors shall be examined for evidence of electrical and mechanical damage.

4.8.11 Life test (see 3.17). Resistors shall be tested in accordance with method 108 of MIL-STD-202. The following details and exceptions shall apply:

* a. Method of mounting: Termination B chip resistor sample units shall be mounted on a fiberglass test board as specified in 4.8.1.3. Terminations G, U, T, C, and D, shall be mounted on ceramic test boards.

b. Test temperature: 70°C ±5°C.

Downloaded from http://www.everyspec.com

c. Initial resistance measurement of mounted resistors: Measurements may be made inside or outside the chamber.

(1) Inside chamber: When measurements are to be made inside the chamber, the initial dc resistance shall be measured after mounting at the applicable test temperature, after a 30 minute +90 minute, -15 minute stabilization period, and within 8 hours of exposure of the resistors to the test temperature. This initial measurement shall be used as the reference dc resistance for all subsequent measurements under the same condition.

(2) Outside chamber: When measurements are to be made outside the chamber, the initial dc resistance shall be measured after mounting at room temperature. This initial measurement shall be used as the reference dc resistance for all subsequent measurements under the same condition.

d. Operating conditions: Rated current shall be applied intermittently, 90 minutes “on” and 30 minutes “off”, for the applicable number of hours (see 4.8.11.f(1)) and at the applicable test temperature. "On time" shall be three quarters of the total elapsed time. During the "on" cycle, the current shall be regulated and controlled to maintain ±5 percent of the rated current.

e. Test condition: Two thousand hours total test time.

f. Measurements during test:

(1) DC resistance shall be measured at the end of the 30 minutes “off” periods after 250 hours +72 hours, -24 hours; 500 hours +72 hours, -24 hours; 1,000 hours +72 hours, -24 hours; and 2,000 hours +96 hours, -24 hours have elapsed.

(2) Measurements outside of the chamber: When measurements are made outside the chamber, resistors shall be outside of the chamber, for a minimum of 45 minutes and stabilized before measurement.

g. Examination after test: Resistors shall be examined for evidence of mechanical damage.

Downloaded from http://www.everyspec.com

4.8.12 Solderability (applicable to termination B) (see 3.18). Resistors shall be tested in accordance with method 208 of MIL-STD-202. Both end terminations shall be immersed completely one at a time or both at the same time by dipping the entire chip in the solder pot. The following details and exceptions shall apply:

a. Apparatus:

(1) A solder pot capable of keeping the solder temperature to ±5°C of set point.

(2) A device to keep the specimen submerged in solder for the required time.

(3) Optical equipment capable of 30X magnification.

(4) A laboratory beaker or appropriate laboratory apparatus that is capable of:

(a) Supporting a nonmetallic device.

(b) Maintaining the test specimens at a distance of 1.50 inches (38.1 mm) to 2.50 inches (63.5 mm) from the surface of the boiling deionized water (DI) or distilled water while, at the same time, exposing them to the full flow of steam generated.

b. The requirement for standard solderable wire application shall not apply.

c. The immersion and emersion rates shall not apply.

d. The specimen shall be totally submerged for at least 5 seconds.

4.8.13 Mounting integrity.

4.8.13.1 Solder mounting integrity (termination B) (see 3.19.1). The resistor chips shall be prepared as specified in 4.8.1.3a. A force shall be applied to all solderable units. The force shall be applied to the edge of the chip as shown on figure 4 for a minimum of 30 seconds. The resistor shall be examined for evidence of mechanical damage. The pusher width shall be a minimum of 30 percent of the length and the maximum width shall be 70 percent of the chip length. The applied force shall be as specified in table VIII.

TABLE VIII. Solder mounting integrity.

Style	Force applied (kilograms)
RCZ0302 and RCZ0402	0.75
RCZ0502 and RCZ0603	1
RCZ0505, RCZ0705, RCZ1005, RCZ1206, and RCZ1505	2
RCZ1010, RCZ2010, RCZ2208, and RCZ2512	3

Downloaded from http://www.everyspec.com

* 4.8.13.2 Bondable mounting integrity (termination's G, U, T, C, and D) (see 3.19.2). The resistor chips shall be prepared as specified in 4.8.1.3b. A force shall be applied to all bondable units. The force shall be applied to the edge of the chip as shown on figure 5 for a minimum of 30 seconds. The resistor shall be examined for evidence of mechanical damage. The pusher width shall be a minimum of 30 percent of the resistor length and the maximum width shall be 70 percent of the chip length. The applied force shall be as specified in table IX.

TABLE IX. Bondable mounting integrity.

Style	Force applied (kilograms)
RCZ0302 and RCZ0402	0.4
RCZ0502 and RCZ0603	0.5
RCZ0505, RCZ0705, RCZ1005, RCZ1206, and RCZ1505	1
RCZ1010, RCZ2010, RCZ2208, and RCZ2512	1.5

4.8.14 Resistance to solvents (see 3.20). Resistors shall be tested in accordance with method 215 of MIL-STD-202. The following details and exceptions shall apply:

a. Mounting: Unmounted and mounted.

b. The marked portion of the resistor shall be brushed.

c. The number of sample units shall be as specified in table V.

d. Resistors shall be inspected for mechanical damage and legibility of minimum marking.

4.8.15 Laser marking legibility test (see 3.21). Resistors shall be coated with .005 inch (0.13 mm) minimum of silicon resin insulated compound, type SR of IPC-CC-830B. After curing, coated resistors shall be examined for legibility under normal production room lighting by an inspector at 10X magnification.

4.8.16 Outgassing (see 3.22). The resistors organic material shall be tested in accordance with ASTM E595.

Downloaded from http://www.everyspec.com

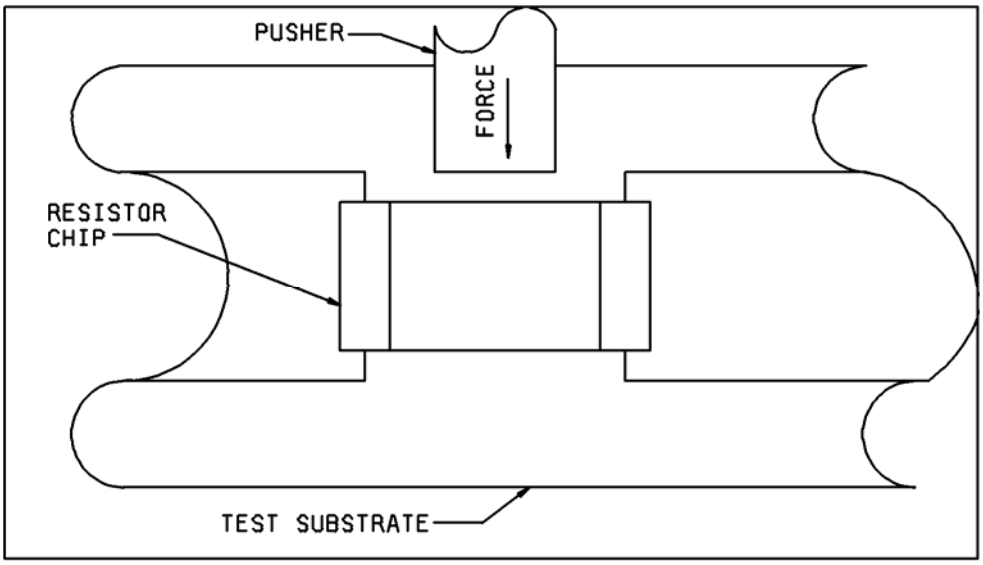


FIGURE 4. Mounting integrity test fixture.

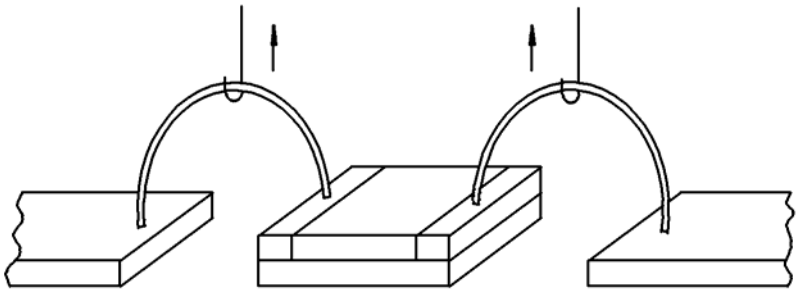


FIGURE 5. Weldable style units.

Downloaded from http://www.everyspec.com

5. PACKAGING

5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activity within the Military Service or Defense Agency, or within the military services system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory.)

6.1 Intended use. The chip resistors covered by this specification are military unique due to the fact that these devices must be able to operate satisfactorily in military systems under the following demanding conditions: 100 cycles of thermal shock (space level only) at high and low temperature extreme and high and low temperature for an extended period of time. In addition, these military requirements are verified under a qualification system. Commercial components are not designed to withstand these military environmental conditions.

6.2 Acquisition requirements. Acquisition documents should specify the following:

a. Title, number, date of this specification, the applicable associated specification, and the complete PIN (see 1.2.1).

b. If not otherwise specified (see 2.1), the versions of the individual documents referenced will be those in effect on the date of release of the solicitation.

c. Packaging requirements (see 5.1).

d. If marking is required (see 3.25).

6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in the QPL whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or purchase orders for the products covered by this specification. The activity responsible for the QPL is the Defense Supply Center, Columbus, (DSCC-VQP), P.O. Box 3990, Columbus, OH 43218-3990.

Downloaded from http://www.everyspec.com

6.4 Application notes.

6.4.1 Mounting of resistors. Resistors may be mounted individually on a test board, fiberglass base, and connected to conductor areas by means of solder preforms, conductive cement, or wire bonding. Users are cautioned that the substrate and chip component must have compatible temperature coefficients of expansion to reduce the strain level imposed on the solder connections. They may also be directly connected to other components on the same test board by means of wire bonding using the test board as a base or carrier for the resistor.

6.4.2 Stacking of resistors. Stacking is generally discouraged since experience indicates that failure may occur due to electrolytic action in the bonding adhesive. This action occurs from the increase in temperature caused by stacking in conjunction with the operating current through the resistor. The bonding adhesive at the resistor chip interface chemically reacts with the active resistor material changing the noise and resistance values and eventually the resistor will open. If stacking resistors, care should be taken to compensate for the lower heat dissipation capabilities by derating the wattage rating.

6.4.3 Resistor film orientation. It is recommended that the film side of resistors be mounted up when they are placed onto printed circuit boards. This is due to the effect of thermal stressing on epoxies used to hold them in place when mounted on the bottom of printed circuit boards. Resistor films can be torn from the substrate during thermal cycling, and substantially altering the value of the resistor.

* 6.4.4 Tin whisker growth. The use of alloys with tin content greater than 97 percent, by mass, may exhibit tin whisker growth problems after manufacture. Tin whiskers may occur anytime from a day to years after manufacture and can develop under typical operating conditions, on products that use such materials. Conformal coatings applied over top of a whisker-prone surface will not prevent the formation of tin whiskers. Alloys of tin containing 3 percent or more lead, by mass, have shown to inhibit the growth of tin whiskers. For additional information on this matter, refer to ASTM-B545 (Standard Specification for Electrodeposited Coatings of Tin).

6.5 Noise level test. This specification does not include a noise test. If the user requires a noise test, it should be performed in accordance with method 308 of MIL-STD-202.

* 6.6 Environmentally preferable material. Environmentally preferable materials should be used to the maximum extent possible to meet the requirements of this specification. As of the dating of this document, the U.S. Environmentally Protection Agency (EPA) is focusing efforts on reducing 31 priority chemicals. The list of chemicals is available on their website at http://www.epa.gov/epaoswer/hazwaste/minimize/chemlist.htm. Further information is available at the following EPA site: http://www.epa.gov/epaoswer/hazwaste/minize/. Included in the EPA list of 31 priority chemicals are cadmium, lead, and mercury. Use of the materials on the list should be minimized or eliminated unless needed to meet the requirements specified herein (see Section 3).

Downloaded from http://www.everyspec.com

6.7 Subject term (key word) listing.

Flat chip
Surface mount
Wrap around

6.8 Amendment notations. The margins of the specification are marked with asterisks to indicate modifications generated by this amendment. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations.

Downloaded from http://www.everyspec.com

APPENDIX A

PROCEDURES FOR QUALIFICATION INSPECTION

A.1 SCOPE

A.1.1 Scope. This appendix covers the procedure for qualification inspection of resistors covered by this specification. This appendix is a mandatory part of this specification. The information contained herein is intended for compliance only.

A.2 APPLICABLE DOCUMENTS. This section is not applicable to this document.

A.3 SUBMISSION

A.3.1 Product levels. Qualification of the C level is predicated upon meeting the M level qualification requirements. The procedure for submitting samples to become qualified to the M level is specified in A.3.2.

A.3.2 Sample. A sample consisting of 182 sample units in each style and termination material for which qualification is sought, shall be submitted to group II, group III, group IV, and group VI for qualification of table III. In addition 30 samples (10 for group V and 20 for group VII) shall be submitted. If applying for space level qualification an additional 30 samples shall be submitted to group VIII of table III. After qualification has been granted, no changes are to be made in materials, design, or construction without prior notification to the qualifying activity.

A.4 EXTENT OF QUALIFICATION

A.4.1 Extent of qualification. The extent of qualification between styles and shall be as specified in table A-I.

Downloaded from http://www.everyspec.com

APPENDIX A

TABLE A-I. Extension of qualification.

Style	Will qualify style 1 /	
RCZ0302	RCZ0302	
RCZ0402	RCZ0402, RCZ0302	
RCZ0502	RCZ0502, RCZ0402, RCZ0302	
RCZ0603	RCZ0603, RCZ0502, RCZ0402, RCZ0302	
RCZ0505	RCZ0505	
RCZ0705	RCZ0705, RCZ0603, RCZ0505	
RCZ1005	RCZ1005, RCZ0705, RCZ0505	
RCZ1010	RCZ1010, RCZ1005, RCZ0705, RCZ0505	
RCZ1505	RCZ1505, RCZ1005, RCZ0705, RCZ0505	
RCZ2208	RCZ2208	
RCZ1206	RCZ1206, RCZ1505, RCZ1010, RCZ1005,	
RCZ2010	RCZ2010, RCZ0705, RCZ0505	
RCZ2512	RCZ2512, RCZ2208, RCZ2010	
Termination	Will qualify termination	May qualify termination with minor additional testing 2/
G	G	B
B	B	G, C, U 3/
U	U, T	C, D
T	T	D
C	C, D	U, T
D	D	T

1/ The same design and technology must be utilized for the style qualified and the styles that the qualification is extended to.

2/ To be determined by qualifying activity.

3/ Must contain barrier layer to qualify.

Downloaded from http://www.everyspec.com

APPENDIX B

VISUAL INSPECTION

B.1 SCOPE

B.1.1 Scope. This appendix details the procedure for visual inspection of conductors, scratches, voids, corrosion, substrate and defects of chip resistors covered by this specification. This appendix is a mandatory part of this specification. The information contained herein is intended for compliance only.

B.2 APPLICABLE DOCUMENTS

This section is not applicable to this appendix.

B.3 INSPECTION

B.3.1 Conductor metallization defects (thick or thin film). Any resistor which exhibits the following defects in the active circuit metallization shall not be acceptable. The active circuit metallization is all metal or any other material used for interconnection.

B.3.1.1 Conductor metallization scratches (thick or thin film). A scratch is defined as any tearing defect that disturbs the original surface of the metallization.

a. Any scratch in metallization through which the underlying resistor material also appears to be scratched.

b. Any scratch in the interconnecting metallization which exposes resistive material, substrate, or oxide anywhere along its length and reduces the width of the connecting strip to less than 50 percent of its original width.

B.3.1.2 Conductor metallization nonadherence (thick or thin film). Conductor metallization nonadherence is defined as any evidence of metallization lifting, peeling, or blistering (see figure B-1).

B.3.1.3 Conductor metallization missing (thick or thin film). Conductor metallization defects are defined as more than 5 percent of the metallization area missing from the bonding pad (see figure B-1).

B.3.1.4 Conductor metallization corrosion (thick and thin film). Metallization corrosion is defined as any evidence of localized heavy stains, metallization corrosion, discoloration or mottled metallization (see figure B-1).

B.3.1.5 Excessive metallization (thick and thin film). A buildup or protrusions of termination material shall not exceed 0.003 inches (0.08 mm) above the average thickness of the termination's surface (see figure B-1).

B.3.1.6 Substrate defects (thick and thin film). Any resistor which exhibits a substrate defect is cause for rejection and defined as follows (see figure B-1):

a. Any crack that exceeds 3.0 mil in length or comes closer than 1.0 mil to an active resistor or bonding pad area on the substrate (see figure B-1).

Downloaded from http://www.everyspec.com

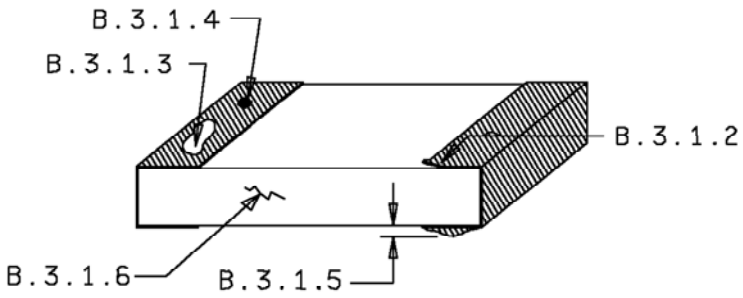


FIGURE B-1. Conductor metallization defects.

B.3.2 Resistor defects (thick and thin film). Any resistor which exhibits the following defects in the active area shall not be acceptable. The active area of a resistor is that part of a resistor pattern which remains in series connection between resistor terminals.

B.3.2.1 Resistor scratches (thick or thin film) (see figure B-2). Resistor scratches are defined as any scratch within the active resistor area one mil or longer. A scratch must be indicated by either disturbance of the surface resistor or extraneous, shiny material remaining from the instrument causing the scratch.

B.3.2.2 Resistor voids (thick and/or thin film) (see figure B-2).

a. For block patterns, a void or neckdown in the active resistor area which reduces the width of the area by more than 10 percent of the original area (see figure B-2).

B.3.2.3 Resistor nonadherence (thick and thin film). Resistor nonadherence is defined as any evidence of resistor film lifting, peeling, or blistering (see figure B-2).

B.3.2.4 Resistor cracks (thick and thin film). Any chip out or crack in the resistor area.

B.3.2.5 Resistor material corrosion (thick and thin film). Resistor material corrosion is defined as follows:

a. Any evidence of localized heavy stains or corrosion of resistor material in the active resistor area (see figure B-2).

Downloaded from http://www.everyspec.com

APPENDIX B

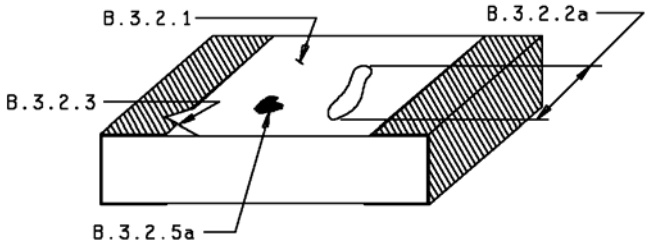


FIGURE B-2. Resistor voids.

B.3.3 Foreign material (thick and thin film). Material is considered attached when it cannot be removed with a soft bristled brush or a nominal gas blow (of 20 psig) of dry nitrogen or air. Attached foreign material which reduces the separation between metallization areas to less than 0.1 mil or is greater than 5 percent of the surface area on which it occurs is cause for rejection.

B.3.4 Heavy metal marks (thick and thin film). Metal marks are defined as termination material on the surface of the substrate or passivation. Heavy metal marks are defined as dots of solder that are continuous and do not allow the substrate/passivation to be seen between the individual dots of metal when viewed at 30X. Light metal marks are defined as dots of metal when viewed at 30X. Light metal marking can be accepted.

a. Reject for any heavy metal marks greater than 10 mils in any direction.

b. Reject for 5 or more heavy metal marks larger than 3 mils but less than 10 mils in any direction on a surface of a resistor chip.

Custodians:
Army - CR
Navy - EC
Air Force - 11
DLA – CC

Preparing activity:
DLA - CC

(Project 5905-2007-020)

Review activities:
Army - AR, AT, AV, CR4
Navy - AS, CG, MC, OS
Air Force - 19, 99

Civil agencies:
NASA - NA

NOTE: The activities listed above were interested in this document as of the date of this document. Since organizations and responsibilities can change, you should verify the currency of the information above using the ASSIST Online database at http://assist.daps.dla.mil.