NOT MEASUREMENT SENSITIVE

MIL-PRF-32006

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PERFORMANCE SPECIFICATION

PROGRAMMABLE CONTROLLER, NAVAL SHIPBOARD

This specification is approved for use by all Departments and Agencies of the Department of Defense.

1. SCOPE

1.1 Scope. This specification covers the requirements for a high-end, rack-mounted, module type programmable controller for naval shipboard use. The terms programmable controller and programmable logic controller (PLC) are used interchangeably throughout this specification.

2. APPLICABLE DOCUMENTS

2.1 General. The documents listed in this section are specified in section 3, 4, or 5 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in section 3, 4, or 5 of this specification, whether or not they are listed.

2.2 Government documents.

2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

FEDERAL STANDARDS

FED-STD-595/26307 Gray, Semigloss

DEPARTMENT OF DEFENSE SPECIFICATIONS

MIL-DTL-2212	Contactors and Controllers, Electric Motor AC or DC, and Associated Switching Devices
MIL-E-2036	Enclosure for Electric and Electronic Equipment, Naval Shipboard
MIL-S-901	Shock Tests, H.I. (High Impact) Shipboard Machinery, Equipment, and Systems, Requirements For

Beneficial comments, recommendations, additions, deletions, clarifications, etc. and any data, that may improve this document should be sent to: Commander, Naval Sea Systems Command, ATTN: SEA 05Q, 1333 Isaac Hull Avenue, SE, Stop 5160, Washington Navy Yard DC 20376-5160 or emailed to commandstandards@navsea.navy.mil, with the subject line "Document Comment". Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at www.dodssp.daps mil.

AMSC N/A FSC 5998

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-167-1	Mechanical Vibrations of Shipboard Equipment (Type I - Environmental and Type II - Internally Excited)
MIL-STD-461	Requirements for the Control of Electromagnetic Interface - Characteristics of Subsystems and Equipment

(Copies of these documents are available online at http://assist.daps.dla mil/quicksearch or www.dodssp.daps mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.3 Non-Government publications. The following documents form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents are those cited in the solicitation or contract.

INSTITUTE OF ELECTRICAL AND ELECTRONIC ENGINEERS

IEEE 802.3	Information Technology - Telecommunications and Information Exchange between Systems - LAN/MAN Specific Requirements - Part 3: Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method and Physical Layer Specifications
IEEE C95.1	IEEE Standard for Safety Levels with Respect to Human Exposure to Radio Frequency Electromagnetic Fields, 3kHz to 300 GH

(Applications for copies are available from the IEEE Service Center, 445 Hoes Lane, Piscataway, NJ 08855-1331 or www.ieee.org.)

INTERNATIONAL ELECTROTECHNICAL COMMISSION

IEC 61131-2	Programmable Controllers – Part 2: Equipment Requirements and Tests
IEC 61131-3	Programmable Controllers – Part 3: Programming Languages

(Applications for copies are available from the IEC, UBS SA, 1201 Geneva, Switzerland or www.iec.ch.)

NATIONAL ELECTRICAL MANUFACTURERS ASSOCIATION

250	Enclosures for Electrical Equipment (1000 Volts Maximum)
ICS 2	Industrial Control and Systems: Controllers, Contactors and Overload Relays, Rated Not More Than 2000 Volts AC or 750 Volts DC

(Applications for copies should be addressed to the National Electrical Manufacturing Association, 2101 L Street, NW Suite 300, Washington DC 20037 or www.nema.org.)

ELECTRONICS INDUSTRIES ALLIANCE

EIA 232	Interface Between Data Terminal Equipment and Data

(Applications for copies should be addressed to the IHS, 15 Inverness Way, East Englewood, Colorado 80155-6800 or custsvc@ihs.com.)

2.4 Order of precedence. In the event of a conflict between the text of this document and the references cited herein (except for related associated specifications or specification sheets), the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 First article. When specified (see 6.2), a sample shall be subjected to first article inspection in accordance with 4.2.

3.2 Materials. The contractor shall select materials capable of meeting all of the operational and environmental requirements specified herein. The materials specified in this specification are recommended, but are not mandatory.

3.2.1 Recycled, recovered, or environmentally preferable materials. Recycled, recovered, or environmentally preferable materials should be used to the maximum extent possible, provided that the material meets or exceeds the operational and maintenance requirements, and promotes economically advantageous life cycle costs.

3.2.2 Included parts. The controller shall be supplied with a module mounting rack, Central Processing Unit (CPU), input/output scanner, inputs, outputs, network interface(s), memory, power supply, power and interface cables, and software necessary to function as a complete and operable PLC system. The PLC system may include an enclosure as needed to meet the requirements specified herein or as cited in the solicitation or contract.

3.3 Design. The PLC shall be designed to allow an easy interface to existing systems. The processor, input and output circuitry shall have a modular field expandable design. The PLC design shall allow for expansion of the system by the addition of hardware and/or user software.

3.3.1. Component compatibility. The PLC system shall have downward compatibility whereby all new system components can be interchanged with similar modules to reduce obsolescence. The PLC system shall be open distributed and scaleable with a reconfigurable architecture and shall maximize the use of current commercial technology.

3.3.2 Front panel. The front panel of the programmable controller shall include a holder and a connector for a lithium or equivalent battery.

3.3.3 Sharp edges. The PLC shall be designed with no sharp edges, which could cause cuts or abrasions to the operator.

3.4 Performance characteristics.

3.4.1 Reliability. The mean time between failure (MTBF) shall be a minimum of 20,000 operating hours. All components of the PLC system shall not require maintenance more frequently than annually.

3.4.2 Duty. The PLC shall be constructed to operate for continuous duty and general-purpose service as specified in MIL-C-2212.

3.4.3 Diagnostics. The PLC system shall have resource and diagnostic control at all system levels. The PLC system shall provide diagnostics capabilities to allow troubleshooting down to the lowest replaceable unit. Diagnostics shall be of power up and on-line type. The PLC shall be capable of supporting a device that will display diagnostic results, status of selectable addresses, and the suspected modules that could cause the failure. The elimination of suspected failed modules shall be a maximum of three of the most likely modules that could cause that particular failure.

3.4.4 Logic function. The internal wiring of the controller shall be fixed, and all logic functions that shall be performed in a given application shall be programmed into its memory.

3.4.5 Serial port. The PLC shall have one dedicated serial port that supports Electronic Industries Alliance (EIA) 232 signals. It shall be accessible in control logic and provide support for Master and Slave SCADA communication protocol systems. Alternatively, it shall be usable for programming purposes or for access to peripheral devices such as bar code scanners, CRTs, etc.

3.4.6 Electrical service. The PLC shall operate in compliance with an electrical service of either 120 VAC, single phase, in the frequency range from 47 to 63 Hz, or 24 VDC (see 6.2).

3.4.7 Cooling. All system modules, main and expansion chassis shall provide free airflow convection cooling. No internal fans or other means of cooling, except heat sinks, shall be permitted.

3.4.8 Central processing unit.

3.4.8.1 Function. The PLC Central Processing Unit (CPU) shall be a self-contained unit and shall provide control program execution, I/O scanning and support remote or local programming.

3.4.8.2 Discrete and analog points. The processor shall be capable of addressing a minimum of 10,000 discrete points or 1,000 analog points. Processor shall be capable of communicating with 50 physical locations each containing I/O as a minimum or as specified on section 6.2.

3.4.8.3 Multiple independent, asynchronous scans. The PLC processor shall use designated scans for processing of input and output information, program logic, and background processing of other processor functions (see 6.2). Input and output devices located in the same backplane (local I/O) as the CPU shall produce at the rate of the configured Requested Packet Interval (RPI), and for inputs enabled for Change of State (COS), at the time any point changes state. Scan rates for devices located in backplanes other than that in which the processor is located shall be user selectable and shall range from 2 to 100 milliseconds (ms).

3.4.8.4 Features. The processor shall contain the following performance features as a minimum:

a. 16K user memory words capability.

b. Battery-backed CMOS RAM.

c. Ladder logic, Sequential Function Chart (SFC), and structured-text programming support compliant with the IEC 61131-3 standard.

d. Configurable EIA 232 port for programming.

e. Advanced instruction set including file handling, sequencer, diagnostic, shift register, immediate-I/O, and program control instructions.

f. Multiple main control programs for segregation of control tasks.

g. Processor input interrupts and global status flags.

h. Programmable fault response for reacting to a fault before the system goes down.

i. Timed-interrupt routine for examining specific information at specific time intervals.

3.4.8.5 Removable programmable devices. The operating system and application specific program files shall be contained in removable programmable devices that allow for easy field replacement.

3.4.8.6 Fault indication. The CPU shall perform internal diagnostic checks and give visual indication to the user by illuminating a “green” indicator when no fault is detected and a “red” indicator when a fault is detected as specified (see 6.2).

3.4.8.7 Data bits. The CPU shall be capable of addressing at least 48,000 words comprised of 16 data bits.

3.4.8.8 User program. The user programs and data shall be contained in non-volatile, battery-backed memory.

3.4.8.9 Firmware. The operating system shall be contained in non-volatile firmware.

3.4.8.10 Memory. The controller shall contain no less then 100 kilobytes of base memory. It shall provide the capability to increase the memory up to at least 2 megabytes or as required (see 6.2).

3.4.8.11 Mode selector switch. The processor mode shall be selectable by a key switch mounted on the front panel of the CPU. The key switch shall allow the selection of the following modes:

a. RUN - No control logic edits possible, program always executing.

b. PROGRAM - Programming allowed, program execution disabled.

c. REMOTE - Programming terminal can make edits and change processor mode, including TEST mode, whereby the logic executes and inputs are monitored, but edits are not permanently active unless assembled.

3.4.8.12 Processor fault. The PLC shall provide a visual indication of a PLC processor fault. By default, a PLC processor fault shall cause analog control signals to fail in the last state and digital control signals to fail in the low state. The PLC shall provide the capability to change the analog and digital control signal state in response to a failure. If the fault is caused by a memory problem, it shall be possible to clear the fault using a procedure to boot the PLC from the EEPROM or FLASHPROM memory. The devices associated with the control signals shall remain in the last state, with the exception of signals that require a continuous output voltage.

3.4.8.13 Power loss. A total loss of 120 VAC supplying the PLC shall cause the PLC system to shutdown. All control signals associated with that PLC shall fail in the low state. Loss of 24-VDC PLC power supply shall prevent commands associated with that PLC from being energized. Status change signals that do not have alarms

associated with them shall display the open state of the digital contact. Control signals that rely on 24-VDC power from the PLC cabinet shall fail to energize.

3.4.8.14 Input and output devices. Input and output devices located in the same backplane (local I/O) as the CPU shall be capable of being scanned synchronously in under 0.5 ms. Concurrent with this I/O update time, the processing of a typical logic program shall not exceed 0.5 to 2 ms for 1024 instructions with a maximum overhead of 4.5 ms.

3.4.8.15 Remote input and output devices. Input and output devices located remotely should be capable of being scanned in under 10 ms for a 57.6-kilobyte/sec transfer rate, under 7 ms for a 115.2-kilobyte/sec transfer rate, and under 3 ms for a 230.4-kilobyte/sec transfer rate.

3.4.9 Chassis. The I/O chassis shall be capable of holding the CPU, communication modules and I/O modules. The chassis size shall be a minimum of 5 incremental sizes ranging between 4 and 20 module slots.

3.4.9.1 Indicators. The main chassis front panel shall include two-color indicators showing the following status information:

a. PROGRAM or RUN mode of the CPU.

b. The RUN/FAULT status of the CPU.

c. ENABLED/DISABLED state of outputs.

d. State of the I/O adapters.

e. Data I/O forces PRESENT/ACTIVE.

f. Remote device communicating via the inter-processor communications link.

g. Status of the Ethernet transceiver port.

h. Data transfer activity over the Ethernet.

i. EIA 232 activity.

j. Battery status.

3.4.9.2 Mounting and construction. The PLC chassis shall be capable of being back stud mounted to an enclosure panel without the need for an external bracket. The chassis shall be constructed of a material with sufficient strength to meet the requirements of sections 3.5.3 and 3.5.4.

3.4.9.3 Internal power distribution. In a single chassis, all system and signal power to the CPU and support modules shall be distributed on a single motherboard or back plane with no interconnecting wiring between these modules via plug-terminated jumpers.

3.4.10 Modules. Application specific modules shall be specified in section 6.2.

3.4.10.1 Removable modules. All system modules shall have the option of being removed from the chassis or inserted into the chassis while power is being supplied to the chassis without faulting the processor or damaging the modules, or as specified (see 6.2).

3.4.10.2 PLC modules. PLC modules shall plug and lock into the PLC chassis.

3.4.10.3 Key ways. Modules shall be keyed to allow installation in predetermined slots and proper direction.

3.4.10.4 Self-contained unit. Each module shall be a self-contained unit housed within an enclosure.

3.4.10.5 Analog and discrete signals. The PLC system shall be capable of addressing a minimum of 1,000 analog and 1,000 discrete signals necessary to interface with the shipboard system(s). The PLC system shall be able to interface with the following signal types:

a. Analog Input:

0 to 10 VDC

0 to -12 VDC

0 to 160 VAC

4 to 20 mA

± 20 mA

0 to 5 A

Tachometer

RTD

Thermocouple

b. Analog Output:

0 to 10 VDC

0 to -10 VDC

4 to 20 mA

± 20 mA

c. Digital Input:

Normally closed contact

Normally closed supervisory

Normally open contact

Normally open supervisory

d. Digital Output:

Continuous +24 VDC

Continuous +28 VDC

Momentary +24 VDC

Momentary +28 VDC

Normally open contact

Normally closed contact

3.4.10.6 I/O modules types. The following types of I/O modules shall be available for use in the PLC chassis:

a. 16-channel (minimum) 10- to 30-VDC Digital Input Module capable of being selectable to reset or hold last state during a fault.

b. 16-channel (minimum) 0- to 30-VDC Diagnostic Discrete Input Module. The card shall be able to detect a wire break versus an open contact.

c. 6-channel (minimum) 16-bit RTD Input Module capable of reporting degrees Celsius (°C), degrees Fahrenheit (°F), or current for 100-ohm platinum, 120-ohm nickel, or 10-ohm copper sensors.

d. 8-channel (minimum) 16-bit Thermocouple Input Module capable of interfacing with type B, C, E, J, K, N, R, S, and T thermocouples.

e. 16-channel (minimum) 12-bit Analog Input Module capable of 0 to 5 VDC, ±5 VDC, ±10 VDC, 4-20 mA, 0-20 mA, ±20 mA. The card shall contain 8 differential inputs with 1,000-volt isolation or 16 single-ended inputs selectable. The card shall provide binary or binary-coded decimal (BCD) scaling.

f. 16-channel (minimum) 12-bit Analog Output Module capable of 0-5 VDC, ±5 VDC, ±10 VDC, 4-20 mA, 0-20 mA, ±20 mA. The card shall contain 8 differential outputs with 1000-volt insulation or 16 single-ended outputs selectable. The card shall provide binary or BCD scaling.

g. 16-channel (minimum) 24 to 250 VAC individually isolated Contact Output Module. A minimum of 8 contact outputs shall be selectable between normally open and normally closed.

h. 16-channel (minimum) 10- to 30-VDC Digital Output Module.

i. 16-channel (minimum) 30- to 60-VDC Digital Output Module.

j. A module capable of high speed power system monitoring, power system synchronization and load sharing. The module shall be capable of measuring voltage and current from the two three-phase systems and provide control and error signals to implement automatic governor control and synchronization. The module shall generate breaker closure commands within specified windows. Power transducers shall be included in the PLC system.

k. 16-channel (minimum) 30- to 55-VDC Digital Input Module.

l. 16-channel (minimum) 30- to 55-VDC Diagnostic Digital Input Module. The module should be able to detect a wire loss.

m. 16-channel (minimum) 10- to 30-VAC Digital Input Module.

n. 16-channel (minimum) 10- to 30-VAC Diagnostic Digital Input Module. The module should be able to detect a wire loss.

o. 16-channel (minimum) 79- to 132-VAC Digital Input Module.

p. 16-channel (minimum) 79- to 132-VAC Diagnostic Digital Input Module. The module should be able to detect a wire loss.

q. 16-channel (minimum) 10- to 30-VAC Digital Input Module.

r. 16-channel (minimum) 10- to 30-VAC Diagnostic Digital Output Module. The module should be able to detect loss of load or output power.

s. 16-channel (minimum) 79- to 132-VAC Digital Output Module.

t. 16-channel (minimum) 79- to 132-VAC Diagnostic Digital Output Module. The module should be able to detect loss of load or output power.

u. 16-channel (minimum) 10- to 30-VDC Diagnostic Digital Output Module. The module should be able to detect loss of load or output power.

v. 16-channel (minimum) 30- to 60-VDC Diagnostic Digital Output Module. The module should be able to detect loss of load or output power.

3.4.10.7 High resolution analog input module. The High Resolution Analog Input Module shall perform analog to digital conversions to directly interface analog signals to PLC data table values using a minimum of 16-bit resolution. Analog Input must be capable of being user-configured for the desired fault-response state in the event that I/O communication is disrupted. This feature shall provide a safe reaction/response in case of a fault, limit the extent of faults, and provide a predictable fault response. This module shall provide high (minimum of 1,000 volts) isolation between channels. This module shall be capable of providing a minimum of eight thermocouple/mV type inputs covering a range of -5 to 55 mV.

a. Data format shall be natural binary or BCD scaling to ±9,999.

b. Minimum channel update/resolution shall be 18ms/8 channels, 36ms/16 channels, and at least 16-bit resolution.

c. An analog module status block to provide information to the processor for alarming and troubleshooting.

d. User-configurable output response (min, max, mid-range, or last value) for safe reaction to an analog module fault.

e. Analog module software-selectable features to include digital filtering for noisy transmitters and environments, and range selection per input.

3.4.10.8 Analog alarm. Alarm indication for each analog signal shall be determined on a point-by-point basis. As a minimum, each analog signal shall have an out-of-range high and out-of-range low alarm indication (see 6.3.1 and 6.3.2). Alarm indications shall have a reset requirement as specified (see 6.2). Alarm indications shall have the option of an automatic reset. The analog signal shall have only one current alarm indication such that only one alarm type shall be active for a particular signal. The hierarchy shall be as follows. Warn high shall be cleared upon receiving a high alarm; high alarm shall be cleared upon receiving an out-of-range high. Warn low shall be cleared upon receiving a low alarm, low alarm shall be cleared upon receiving an out of range low. High and low alarm indications shall be mutually exclusive, such that the active alarm is the only current alarm indication. A general alarm indication inclusive of the alarm states shall be latched in until an acknowledgement is received. Upon issuing an out-of-service status, all alarming shall be disabled for that signal. An unknown condition shall occur if the communications to the analog module is lost. An unknown condition shall also occur if the set points are defined in such a way that two alarms are active simultaneously. An alarm time delay shall be available as an option. Alarms shall be identified for each analog point in each PLC. Alarm set points and time delays shall be accessed directly on a point-by-point basis.

3.4.10.9 Analog signal status. The following status shall be programmable for each analog signal.

a. Out-of-Range High.

b. Alarm High.

c. Warn High.

d. Normal.

e. Unknown.

f. Warn Low.

g. Alarm Low.

h. Out-of-Range Low.

i. Out-of-Service.

3.4.10.10 Digital alarms. The PLC shall be capable of supporting two (2) types of digital alarms. The first type of alarms are those determined from discrete digital input signals. Digital inputs for these types of alarms shall be fail-safe as specified (see 6.2). The digital input is defined as normally open or normally closed. However, the alarm state of the contact shall be defined in such a way to cause the input contact to open when an alarm condition occurs. The second types of digital alarms are those generated by PLC logic. These types of alarms are for device level alarm indications, such as valves, pumps and diesels, and for command failures. Alarms shall be identified for each discrete digital point in each PLC.

3.4.11 Communication. The PLC system shall have the ability to support several communications options for processor-to-processor, processor to remotely located I/O racks, and processor to human machine interface (HMI) communications with a maximum of one card per communication network. BOOTP client capability shall be provided in the PLC processor to allow assignment of an IP address upon power up. The option shall be selectable on or off.

3.4.11.1 Communication protocol types. The PLC system shall be capable of supporting token passing and (carrier sense multiple access/collision detection) CSMA/CD Ethernet protocols as specified in IEEE 802.3.

3.4.11.2 Network media. The PLC system shall enable all communications to be accomplished through copper or fiber optic media.

3.4.11.3 Network topologies. PLC system networks shall support bus, ring and/or a combination thereof.

3.4.11.4 General network capabilities. All PLC system network communications shall contain the following performance features:

a. Message error checking.

b. Retries of unacknowledged messages.

c. Diagnostic checks on other stations.

d. Interface with more than one network.

e. Ability to perform PLC processor memory uploads and downloads.

f. Bi-directional communication between programmable controllers and communication networks via a standard modem interface. The communication protocol(s) shall meet EIA 232 or ANSI standard communication protocol requirements.

g. Ability to communicate with all other models of PLCs manufactured by the same supplier.

h. Ability to monitor the status of any processor remotely via the network.

3.4.11.5 Loss of communications. During the loss of communications, individual PLCs shall continue to run and remain in a safe state of control. Loss of communication between PLCs shall cause signals to remain in their last known state in the PLC that requires the information. Control signals shall fail in a deenergized state.

3.4.11.6 PLC processor-to-PLC processor (peer-to-peer) communications. PLC processors shall have the ability to send and receive data from other PLC processors through Ethernet and other network protocols.

3.4.11.7 PLC processor to remote I/O rack communications. PLC processors shall have the ability to send and receive data from remote I/O racks via Ethernet and other network protocols.

3.4.11.8 PLC processor to human machine interface (HMI) communications. The PLC processor shall be capable of transferring data to and from HMI application software via Ethernet TCP/IP, UDP, IP multicast, or OPC.

3.4.11.9 OLE for process control (OPC). Data communications using OPC shall be accomplished using an external OPC server software application, using the PLC processor itself as an OPC server or having a module within the PLC rack that contains an OPC server, as specified (see 6.2).

3.4.11.10 UDP broadcast data. The PLC processor shall be capable of sending data on a network using UDP or IP multicast protocols.

3.4.11.11 TCP/IP protocol. The PLC processor shall be capable of sending and receiving data on a network using the TCP/IP protocol. Communication with HMI devices shall require no intermediate external software applications.

3.4.11.12 Ethernet. The PLC system shall provide industry standard Ethernet communication capabilities embedded either in the PLC processor or through an Ethernet communication module.

3.4.11.12.1 General Ethernet capabilities. The Ethernet interface shall support the following:

a. Standard IP communications.

b. Standard Ethernet media (10base2, 10base5, 10/100baseT, 10/100baseF).

c. CSMA/CD access method.

d. Subnet masking in order to comply with networks that use subnetting.

e. Standard repeaters, bridges, routers, host computers, peer PLCs.

f. RJ-45 and AUI ports.

g. BOOTP client (selectably turned on or off).

h. Bridging to other types of networks (e.g. ControlNet and Profibus).

3.4.11.12.2 Network connection. The PLC processor shall have a selectable option of using IEEE 802.3 as the interface to the network as well as DIX.

3.4.11.12.3 Ethernet diagnostic status. The programmable controller shall maintain locally an Ethernet diagnostic status file that contains relative counters to record the number of retries.

3.4.11.12.4 Token passing network. The PLC system shall provide an industry standard token passing network option with the following minimum capabilities:

a. Support a data transfer rate of at least 5 megabit/sec.

b. Support up to at least 48 addressable nodes without a repeater.

c. Support the use of repeaters to extend the number of addressable nodes.

d. Support both scheduled and unscheduled messaging.

e. Support update times of at least 100 ms.

f. Support multiple network media and topologies as specified (see 6.2).

3.4.12 Power supply. The system power supply shall be capable of converting 120 VAC line power to the DC power required to operate the programmable controller backplane, CPU, and modules. The power supply shall operate with 97 to 132 VAC, single phase, from 47 to 63 Hz or 19 to 32 VDC as specified (see 6.2).

3.4.12.1 Power up. Operation of the processor and I/O modules shall be inhibited during power up until DC values are within specified limits.

3.4.12.2 Power shut down. Power supply shall automatically shut down the PLC system when the output current exceeds 125% of rated current. If the voltage level is out of range for more than ½ cycle, the power supply shall automatically shut down the system and remain shut down until the voltage returns to the proper level. The power supply shall provide surge protection, isolation, and outage carryover up to 2 cycles of the AC line.

3.4.12.3 Diagnostic indicators. The PLC power supply shall include diagnostic indicators mounted in a position easily viewed by the user. These indicators shall provide the operator with the status of the DC power applied.

3.4.12.4 Main power supply. A single main power supply shall have the capability of supplying power to the CPU and local I/O modules. Auxiliary power supplies shall provide power to remotely located racks.

3.4.12.5 Constant voltage transformer. In cases where the AC line is especially unstable or subject to unusual variations, it shall be possible to install a constant voltage transformer having a sinusoidal output waveform.

3.4.12.6 Insulating cover. An insulating cover shall be mounted over high voltage terminals to provide protection for maintenance personnel and allow for easy removal.

3.4.12.7 Fuse protection. The power supply shall have adequate fuse protection to prevent damage to the power supply in the event of overcurrent.

3.4.12.8 Fluctuation. The power supply shall not fluctuate for loads between 1 and 10 amps as specified (see 6.2).

3.4.12.9 Auxiliary power supply. The auxiliary power supply shall include provisions for remote sensing and/or external output adjustment, and shall be short circuit proof with automatic recovery (electronic current limiting). Response time shall be less than 20 microseconds as specified (see 6.2).

3.4.13 Terminal boards.

3.4.13.1 EC type. EC type terminal boards shall be provided for field wire connections as specified (see 6.2).

3.4.13.2 Location. The terminal boards shall be located near the cable entrance as specified (see 6.2).

3.4.13.3 Accessibility. Terminal boards shall be accessible from the front of the enclosure as specified (see 6.2).

3.4.13.4 Identification. All terminal boards shall be organized and marked to establish easy identification of signals as specified (see 6.2).

3.4.13.5 Fused terminal blocks. Fused terminal boards shall be provided for 4 to 20 mA transmitters, discrete input, and discrete output signals as specified (see 6.2).

3.4.14 Enclosure. Each PLC enclosure shall contain the PLC I/O chassis, PLC processor, PLC I/O modules, supporting power supplies, and terminal boards. The PLC enclosure shall meet the following requirements as specified (see 6.2).

3.4.14.1 Enclosure type. MIL-E-2036 and NEMA 250 shall be used as guidelines for specifying enclosure type. The enclosure shall be rigid and self-supporting with suitable structural reinforcement, stiffening, and bracing. All enclosure surfaces shall be flat and smooth.

3.4.14.2 Enclosure doors. All enclosure doors shall be easily removable and shall be fitted with a locking mechanism, capable of keeping the door closed and sealed. The enclosure door shall be grounded if electrical or electronic components mounted on the door are powered by 30 volts or more. A flexible ground conductor shall be installed between the door frame and the enclosure frame. The ground conductor size shall be equal to or greater than the size of one of the conductors supplying AC power to the enclosure door.

3.4.14.3 Interface cables. Each enclosure shall accept system interface cables through stuffing tubes on the top, bottom or sides of the enclosure.

3.4.14.4 Painting. The PLC system enclosure shall be painted Machinery Gray in accordance with FED-STD-595/26307 as specified (see 6.2).

3.4.14.5 Nameplate. Each enclosure shall have a phonemic nameplate attached representing each enclosure and function.

3.4.14.6 Hardware. Each enclosure shall house all hardware necessary to interface the field machinery with the PLC enclosure, including terminal block/strips for terminating all required field wiring, power supplies required for loop and I/O power, and any necessary relays and transducers. All spare PLC I/O card channels shall be wired to spare terminal block points.

3.4.14.7 Enclosure size. The PLC system components shall be mounted in an enclosure with dimensions as specified (see 6.2).

3.4.15 Wiring.

3.4.15.1 Wiring terminations. All internal enclosure wiring terminations shall be tinned or ferruled as specified (see 6.2).

3.4.15.2 Size. The minimum wiring size for all PLC wiring connections shall be 22 AWG.

3.4.15.3 Low smoke. Wire used in the PLC system shall be rated for low smoke applications. Polyvinyl chloride (PVC) insulation shall not be used. Wire ends shall be fitted with crimp type ferrules at termination points.

3.4.15.4 Temperature rating. The minimum temperature rating for wires shall be 105 °C. Wires exposed to heat shall have a temperature rating of no less than 125 °C.

3.4.16 Switches and Indicator Lights. All switches, indicator lights and other operator devices supplied with the PLC system shall be UL listed and/or CSA approved and shall meet the requirements of NEMA ICS 2. Identification plates shall clearly indicate the function of indicator lights and switches. Identification plates shall indicate each position of selector switches. The switches, indicator lights and other operator devices shall be as specified (see 6.2).

3.4.17 Program creation and storage.

3.4.17.1 Control logic programs. Control logic programs shall provide for immediate access to the sub-elements of control structures by address and sub-element mnemonic, such as timer accumulator value, timer done bit, or PID process variable value.

3.4.17.2 Non-volatile memory. The operating system information shall be stores in non-volatile memory to protect against loss in the case of power loss or system shutdown as specified (see 6.2).

3.4.17.3 Program storage medium. The program storage medium shall be of a static battery backed RAM type.

3.4.17.4 Memory. Memory shall be available in 48K word segments of RAM memory.

3.4.17.5 Access method. The access method to the media shall be Carrier Sense with Multiple Access and Collision Detection (CSMA/CD).

3.4.17.6 Battery back-up. Memory shall contain a battery back-up capable of retaining all stored program data through a continuous power outage for 4 months under worst-case conditions.

3.4.17.7 System power. The capability shall exist to remove all batteries from the system without removing system power.

3.4.17.8 Low battery condition. A means shall be provided to detect a low battery condition in ladder logic.

3.4.17.9 Non-volatile memory. The PLC processor shall provide the use of a non-volatile memory such as EEPROM or FLASHPROM as a back up for volatile memory up to the full capacity of the controller.

3.4.17.10 Memory back-up. The capability to back-up volatile memory, including data and program logic onto either 3 ½-inch floppy diskettes or external hard disk, shall be provided.

3.4.17.11 Upgradeable processor memory. The capability to upgrade to a processor memory with a larger size simply by saving a program, replacing the processor, and downloading the program to the new system without having to make any program changes shall be provided.

3.4.17.12 User memory. All user memory in the processor not used for program storage shall be allocable from main memory for the purpose of data storage. The programmable controller system shall be capable of storing predefined, user-defined and module-defined data types as specified (see 6.2).

a. Boolean values.
b. Control structure.
c. Counter values.
d. Integer values.
e. Message values.
f. Real numbers.
g. Signed integer numbers.
h. Timer values.
i. External output status.
j. External input status.
k. Floating point numbers.
l. Decimal numbers.
m. Binary numbers.
n. BCD numbers.
o. Direct and indexed addressing.
p. Internal processor status information.
q. ASCII character data.
r. ASCII string data.
s. Data transfer control structures.
t. File instruction control structures.
u. Message control structures.

3.4.17.13 Access to sub elements. Control logic programs shall have immediate access to the sub elements of control structures by address and sub element mnemonic, such as timer accumulator value, timer done bit, or PID Process Variable value.

3.4.17.14 Timer programming. The number of times a timer or counter can be programmed shall be limited only by the memory capacity to store these instructions.

3.4.17.15 Internal output programming. The number of times a normally open (NO) and/or normally closed (NC) contact of an internal output can be programmed shall be limited only by the memory capacity to store these instructions.

3.4.17.16 Application logic. The capability shall be provided to program select application logic more than once into memory.

3.4.17.17 Contacts and rungs. If contacts or entire rungs are intentionally deleted from an existing logic program, the remaining program shall be automatically repositioned to fill this void. Whenever contacts or entire rungs are intentionally inserted into an existing program, the original program shall automatically be repositioned to accommodate the enlarged program. All rungs shall maintain their original links.

3.4.17.18 Base processor memory. Base processor memory shall be provided for user program and data.

3.4.17.19 Module-defined data. Module-defined data types shall include a structure for each I/O module and system or module specific information (hidden from user). Any data can be displayed in Binary, Octal, Hexadecimal, or Decimal radices.

3.4.17.20 User-defined data. User-defined data types shall include user-defined structures capable of containing one or more pre-defined data members.

3.4.17.21 Application program interface. Application Program Interface (API) shall be provided for the HP-UX, VMSTM, Sun Solaris, and Windows operating systems in the form of linkable libraries for C application programs as specified (see 6.2).

3.4.17.22 Task programs. Each task can include up to 32 programs that are capable of being ordered for execution in each task as specified (see 6.2).

3.4.17.23 On-line programming. On-line programming and upload/downloads of control programs shall be capable of occurring over the Ethernet network.

3.4.17.24 Programming terminal. The programming terminal shall be connected either directly to the PLC processor or via the Ethernet interface.

3.4.17.25 Software and licenses. Software and licenses shall be provided to interface the Windows based processor HMI program with the PLC processors as specified (see 6.2).

3.4.17.26 Sub-system. The programmable controller sub-system shall have the ability to be updated electronically to interface with new modules

3.4.17.27 Programming format. The programming format shall be IEC 61131-3 compliant for Instruction List, Structured Text, Ladder Diagram and Function Block Diagram as specified (see 6.2).

3.4.17.28 Sequential function chart and structured text operations. Sequential function chart and structured text operations shall execute in the CPU in native op codes. Representative ladder logic shall not be generated for corresponding sequential function chart and structured text operations.

3.4.17.29 Maximum instruction matrix. It shall be possible to program a maximum instruction matrix of 7 wide by 6 deep containing as many as 77 examine instructions.

3.4.17.30 Periodic tasks. Periodic tasks shall run via an interrupt at a user-defined interval in one-millisecond increments to a maximum of 2000 seconds. The periodic tasks shall have an associated, user assignable priority from one to fifteen (one being the highest priority), which specifies that task's relative execution priority in the multitasking hierarchy.

3.4.17.31 Interrupt mechanism. The interrupt mechanism of periodic tasks shall adhere to the IEC 61131-3 definition of pre-emptive multitasking.

3.4.17.32 Number of individual tasks. The controller shall be able to accommodate 32 individual tasks of which a minimum of one shall be continuous.

3.4.17.33 Watchdog timeout. Each task shall have a watchdog timeout that is unique to that task and user-defined.

3.4.17.34 Ladder logic routines. Each program shall include user ladder logic routines of which a minimum of one shall be specified in the main routine and at least one shall be specified as the fault routine. The maximum number of routines contained in a program shall be limited only by memory.

3.4.17.34.1 Programming. It shall be possible to program ladder rungs with the following restrictions. Series instruction count limited only by user memory, branch extensions limited only by user memory, branch nesting to 6 levels or more.

3.4.17.34.2 Contact editing. The capability shall exist to change the state of a contact from normally open to normally closed, add instructions, and change addresses, without deleting and reprogramming the entire rung.

3.4.17.34.3 Deletion commands. A single program command or instruction shall enable deletion of an individual ladder diagram rung from memory, without deleting the rung contact by contact.

3.4.17.34.4 Deletion safeguard. A two-part command shall be used to delete all relay ladder rungs from memory, providing a safeguard wherein the operator must verify their intentions before erasing the entire program.

3.4.17.34.5 Rung comments. The system shall have the capability to enter rung comments above ladder logic rungs. The capability shall be provided to enter comments at the same time the ladder logic is entered.

3.4.17.34.6 Rung editing. The capability shall exist for adding, removing, or modifying ladder logic rungs during program execution. When changes to ladder logic are made or new logic rungs are added, it shall be possible to test the edits of such rungs before removal of the prior logic rung is executed.

3.4.17.34.7 Relay ladder logic rungs. It shall be possible to insert relay ladder logic rungs anywhere in the program even between existing rungs.

3.4.17.34.8 Ladder logic editing. The PLC System shall have the capability to remove an entire logic rung into an edit buffer where individual parameters may be easily altered.

3.4.17.35 Controller variables. Variables within the controller shall be referenced as unique, default, or user defined tags.

3.4.17.36 Tags. The ability to program control logic via tags of the programmable controller shall exist. Tags shall be created off-line, on-line in program mode, and at the same time the ladder logic is entered.

3.4.17.36.1 Availability. Tags shall be available to all tasks in the controller (controller scoped) or limited in scope to the routines within a single program (program scoped) as defined by the user.

3.4.17.36.2 Alias. Any tag shall have the ability to be aliased by another tag that is defined and has meaning to the user.

3.4.17.36.3 Tag naming convention. Tag naming convention shall adhere to IEC 61131-2.

3.4.17.36.4 Description. The system shall have the capability to store a description for each tag.

3.4.17.37 User-defined data structures. The capability shall exist to organize data in the form of User-Defined Data Structures. All aforementioned data types, as well as others, shall be used in such structures along with embedded arrays and other User-Defined Data Structures.

3.4.17.38 Array configuration. Arrays shall be configurable with one, two, or three dimensions.

3.4.17.38.1 Value arrays. Value arrays shall be limited in size only by the amount of available memory.

3.4.17.38.2 Addressing index. The CPU shall support indexed addressing of array elements.

3.4.17.38.3 Array element manipulation instructions. Array element manipulation instructions such as high speed “array copy” and “array fill”, “array to array” move, “element to array” move, “array to element” move and “first in - first out” shall be supported by the system. The four-function math instructions and instructions for performing “logical OR”, “logical AND”, “exclusive OR”, and comparison instructions such as “less than”, “greater than”, and “equal to” shall be included within the system. All instructions shall execute on either single words or arrays.

3.4.17.39 Status of channels. For any module specifically associated with the programmable controller, it shall be possible to query the current status of all channels through controller-scoped tags without any programming.

3.4.17.40 Master system clock. The programmable controller shall provide a master system clock that shall allow synchronization of all axes in the chassis local to the controller.

3.4.17.41 User applications. The controller shall organize user applications as tasks that can be specified as continuous or periodic.

3.4.17.42 Clock/calendar. A clock/calendar feature shall be included within the CPU with access from the programming terminal, user program, or message generation.

3.4.17.43 Latch functions. Latch functions shall be internal and programmable.

3.4.17.44 Software timers and counters. The system shall have the capability to address software timers and software counters in any combination and quantity up to the limit of available memory. The CPU shall handle all management of these instructions into memory. Instructions shall permit programming timers in the on or off delay modes. Timer programming shall also include the capability to interrupt timing without resetting the timers. Counters shall be programmable using up-increment and down-increment.

3.4.17.45 Timer instructions. Timer instructions shall include selectable time bases in increments of 1 second, 10 ms, and 1 ms with at least 10 ms accuracy. The timing range of each timer shall be from 0 to 2,147,483,648 increments. It shall be possible to program and display separately the timer's preset and accumulated values.

3.4.17.46 Signed integer format. The PLC processor shall use a double integer format ranging from -2,147,483,648 to +2,147,483,647 for data storage of the counter preset and accumulated values.

3.4.17.47 Data storage. The PLC processor shall store data in the following formats:

a. Boolean Values (0 or 1).

b. Short Integer Numbers ranging from -128 to +127.

c. Signed Integer Numbers ranging from -32,768 to +32,767.

d. Double Integer Numbers ranging from -2,147,483,648 to +2,147,483,647.

e. Floating Point Numbers consisting of eight significant digits. For numbers larger than eight digits, the CPU shall convert the number into exponential form with a range of ± 1.175494 E -38 to ± 3.402824 E +38.

f. Decimal Numbers ranging from 0 to 9,999.

3.4.17.48 Math functions. The processor shall have support for integer and floating point signed math functions consisting of addition, subtraction, multiplication, division, and square root.

3.4.17.49 Multiple channels. When using modules such as analog where multiple channels are terminated on one module, it shall be possible to transfer the current status of all channels to the CPU upon execution of one program instruction. This instruction shall be bi-directional to include data transfer from the CPU to the module or from the module to the CPU.

3.4.17.50 Grouping contiguous 16-bit data words. Instructions shall be provided for grouping contiguous 16-bit data words into a file. The system shall address up to 1,000 files with up to 1,000 words per file. File manipulation instructions such as high-speed "file copy" and "file fill", "file to file" move, "element to file" move, "file to element" move, and "first in - first out" shall be supported by the system. The four function math instructions and instructions for performing "logical OR", "logical AND", "exclusive OR", and comparison instructions such as "less than", "greater than", and "equal to" shall be included within the system. All instructions shall execute on either single words or files.

3.4.17.51 Asynchronous and synchronous. The processor shall contain instructions, which shall construct asynchronous and synchronous 16-bit word shift registers. Additional instructions shall be provided to construct synchronous bit shift registers.

3.4.17.52 Jump instruction. The processor shall have a jump instruction that shall allow the programmer to jump over portions of the user program to a portion marked by a matching label instruction.

3.4.17.53 Management of all data types. The CPU shall automatically manage all data types. For example, if a word stored in the integer section of memory is transferred into the floating-point section, the CPU shall convert the integer value into floating-point prior to executing the transfer.

3.4.17.54 Subroutine section. In applications requiring repeatable logic rungs, the capability shall exist to place such rungs in a subroutine section. Instructions, which call the subroutine and return to the main program, shall be included within the system. The capability shall exist to program several subroutines and define each subroutine by a unique program file designator. The processor shall support nesting of subroutines a minimum of seven levels deep. The program format as displayed on the CRT/LCD shall clearly define the main program and all subroutines. The capability shall exist to pass selected values (parameters) to a subroutine before its execution, enabling the subroutine to perform mathematical or logical operations on the data and return the results to the main program upon completion. These subroutines shall be accessed by jump-to-subroutine instructions.

3.4.17.55 Program format. The program format shall display all instructions on a CRT/LCD programming panel with appropriate mnemonics to define all data entered by the programmer. The system shall be capable of providing a "HELP" instruction which, when called by the programmer, shall display on the CRT a list of instructions and all data and keystrokes required to enter an instruction into the system memory.

3.4.17.56 Displayed system memory. At the request of the programmer, data contained in system memory shall be displayed on the CRT/LCD programming panel. This monitoring feature shall be provided for input/output status, timer/counter data, files, and system status. Ladder logic rungs shall be displayed on the CRT with rung numbers in sequential order. However, the programmer shall have the option of selecting and displaying logic rungs non-contiguously. Sequential function charts shall be displayed on the CRT/LCD. Structured text shall be displayed on the CRT.

3.4.17.57 Addressing comments. The system shall have the capability to enter address comments and symbols. These entities shall have the capability to be entered at the same time the ladder logic is entered.

3.4.17.58 Manually setting. The capability shall exist to manually set (force) either ON or OFF all hardwired input or output. Removal of these forced I/O points shall be either individually or totally through selected keystrokes. The programming terminal shall be able to display forced I/O points.

3.4.17.59 Fault recovery. A means to program a fault recovery routine shall exist. When a major system fault occurs in the system, the fault recovery routine shall be executed and then the system shall determine if the fault has been eliminated. If the fault is eliminated, program execution shall resume. If the fault still exists, the system shall shut down. A user shall have the option to either resume operation or to shut down upon fault detection.

3.4.17.60 Fault routine. The capability shall exist for each program to have its own fault routine for program fault recovery and each having the same features as the controller based fault routine.

3.4.17.61 Interrupt routine. An interrupt routine shall be programmable such that the routine shall be an instruction and shall be supported to incorporate closed loop control systems. The "proportional", "integral", and "derivative" elements shall be accessible to the user in order to tune a closed loop system. This instruction shall fully support floating-point math. An interrupt routine shall be programmable such that the routine shall be executed regularly. The interval at which the routine is executed shall be user-specified in the range of 1 to 65,535 ms. An interrupt routine shall be programmable such that the routines shall be executed based upon the input condition of one of the discrete hardware inputs in the processor chassis. The routine shall be executed within 2 ms of the detection of the input signal.

3.4.17.62 Software instruction set addressing. The CPU shall support indexed and indirect addressing of inputs and outputs, along with all data table words (integer, binary, floating point, timers, and counters) for the software instruction set.

3.4.17.63 Symbols. The ability to program control logic via symbols from the global database of the PLC processor shall exist.

3.4.17.64 Control program instruction. An instruction shall be available to give the control program diagnostic information, state control, and sequencing of a process simultaneously, while allowing the capability of user-friendly state programming techniques.

3.4.17.65 Diagnostic instructions. The system shall support both bit and word level diagnostic instructions.

3.4.17.66 Function block programming. The processor shall be able to edit, build, and execute logically constructed function block routine. These function blocks shall be executed either selectively, based upon application logic (transitions), or simultaneously. The ability to "zoom" in on a given routine shall be inherent to

allow the user to quickly diagnose their application program. The overall effect of the function chart programming shall to be to provide a more efficient flow of the user's application program.

3.4.17.67 Event detection programming. To facilitate conditional event detection programming, output instructions shall include "one shot" instructions, which shall provide the capability of being triggered on either low-to-high (rising) or high-to-low (falling) rung conditions.

3.4.17.68 Debugging. To facilitate debugging, an "always false" instruction shall temporarily inhibit the execution of control logic.

3.4.17.69 Master control reset. The processor shall support Master Control Reset (Relay) type functionality to selectively disable sections of logic.

3.4.17.70 Trigonometric instructions. Trigonometric instructions supported shall include Sine, Cosine, Tangent, Inverse Sine, Inverse Cosine, and Inverse Tangent. These instructions shall fully support floating-point math.

3.4.17.71 Floating-point instructions. Additional floating-point instructions supported shall include Log 10, Natural Log, and Exponential.

3.4.17.72 Calculations. It shall be possible to complete complex, combined calculations in a single instruction, such as flow totaling or equations of the format ((A+ ((B-C)*D))/E).

3.4.17.73 File function instructions. File function instructions supported shall include Sort, Average, Square Root, and Standard Deviation.

3.4.17.74 FOR-NEXT loop. The processor shall include direct support of FOR-NEXT loop constructions.

3.4.17.75 ASCII string manipulation instructions. The processor instruction set shall provide support for a variety of ASCII string manipulation instructions such as search, concatenation, extraction, compare, and to/from integer conversion.

3.4.17.76 Control logic functions. The processor shall support control logic functions providing ASCII port control such as read, write, handshake line control, and buffer examination.

3.4.17.77 Configuration. The capability shall exist to configure control programs that consist of hybrid control functions combining both relay ladder logic, sequential function chart operations, and structured text operations.

3.4.17.78 Communication. The programmable controller shall communicate with remote I/O racks or other PLCs via fiber optic cable by inserting fiber optic converters into the links. The fiber link shall support distances between converters up to 6500 cable feet. Redundant fiber optic cabling shall be an option.

3.4.18 Diagnostics and state control. The programmable controller system shall be capable of support the diagnostic functions indicated or as specified in Section 6.2.

3.4.18.1 Diagnostic instruction. A diagnostic instruction in the PLC processor shall be capable of executing level 1, level 2, or level 3 diagnostics. Level 1 diagnostics shall use control logic for control with control logic fault detection logic setting fault bits that are monitored by the instruction for diagnostic message generation only. Level 2 diagnostics shall use control logic to control outputs, but the instruction shall monitor inputs and conditions to detect faults and generate a diagnostic message. In level 3 diagnostics, the instruction shall control outputs, monitor inputs for state control, perform diagnostic detection, and generate a diagnostic message.

3.4.18.2 Diagnostic messages. Diagnostic messages shall be assembled automatically using text from the PLC processor documentation such as address comments, symbols, step names, instruction comments, processor name, and other accessible PLC parameters. These fragments shall be user configurable in terms of size and usage. These automatic messages shall not require pre-storage by the user as they are dynamically assembled and generated.

3.4.18.3 Network multiple PLC processors. It shall be possible to network multiple PLC processors, each of which shall report diagnostic information to a common terminal.

3.4.18.4 Diagnostic messages. The system shall provide the following types of diagnostic messages:

a. Status messages.

b. Error messages.

c. Time-out messages.

d. Warning time-out messages.

e. One valid exit message.

f. Mismatch message.

3.5 Environmental conditions.

3.5.1 Operating temperature. The PLC system shall operate at an ambient temperature of 0 °C to 60 °C and a storage ambient temperature of –40 °C to 85 °C.

3.5.2 Humidity range. The PLC system shall operate in the relative humidity range of 5% to 95% non-condensation.

3.5.3 Shock. The PLC system shall meet specified performance requirements after being subjected to shock levels as specified in MIL-S-901, for Grade A, Class II, Type B shock (see 6.2). No portion of the PLC system shall break or cause a hazard to personnel.

3.5.4 Vibration. The PLC system shall operate without failure when tested in accordance with the vibration requirements of MIL-STD-167-1 Type I.

3.5.5 Inclination. The PLC system shall operate when permanently inclined in any direction at any angle up to 15 degrees from the normal operating position and during temporary inclinations of up to 45 degrees in any direction from the normal operating position.

3.5.6 Electromagnetic interference. The levels of electromagnetic interference (EMI) shall not exceed the limits for human exposure in accordance with IEEE C95.1. Mission specific emissions and susceptibility shall be as specified (see 6.2). The use of line-to-ground filters shall be minimized and line-to-line filters are preferred. If utilized, the line-to-ground capacitance shall not exceed 0.1 microfarads. The PLC system shall meet EMI requirements when tested in accordance with MIL-STD-461.

4. VERIFICATION

4.1 Classification of inspections. The inspection requirements specified herein are classified as follows:

a. First article inspection (see 4.2).

b. Conformance inspection (see 4.3).

4.2 First article inspection. The PLC shall be subjected to first article inspection, which shall consist of the tests indicated in Table I and paragraphs 4.4 and 4.5.

4.3 Conformance inspection. Conformance inspection shall include the examination of 4.4 and the tests of 4.5.4 through 4.5.7 (see Table I).

TABLE I. First article tests and conformance inspections.

Requirement	Requirement Paragraph	First Article Test Paragraph	Conformance Inspection Test Paragraph
Visual and Dimensional	3.2 through 3.3.3	4.4	4.4
Performance	3.4	4.5.7	4.5.7
Operating Temperature	3.5.1	4.5.1	4.5.1
Humidity	3.5.2	4.5.2	4.5.2
Shock	3.5.3	4.5.3	4.5.3
Vibration	3.5.4	4.5.4	4.5.4
Inclination	3.5.5	4.5.5	4.5.5
EMI	3.5.6	4.5.6	4.5.6

4.4 Examination. Each PLC shall be examined for compliance with the requirements specified in 3.2 through 3.5. Any redesign or modification of the contractor's standard product to comply with specified requirements, or any necessary redesign or modification following failure to meet the specified requirements shall receive particular attention for adequacy and suitability. This element of inspection shall encompass all visual examinations and dimensional measurements. Non-compliance with any specified requirements or presence of one or more defects preventing or lessening maximum efficiency shall constitute cause for rejection.

4.5 Methods of inspection.

4.5.1 Burn-in. The PLC shall be subjected to a burn-in test at 60 °C for at least 96 hours.

4.5.2 Relative humidity. The PLC system shall be tested for conformance to the relative humidity requirements specified in 3.5.2.

4.5.3 Shock. The PLC shall be shock tested in accordance with MIL-S-901 Grade A, Class II, Type B (see 3.5.3).

4.5.4 Vibration. The PLC shall be vibration tested in accordance with MIL-STD-167-1 Type I (see 3.5.4).

4.5.5 Inclination. Equipment shall pass a general operation test when inclined form bulkhead mounted orientation to the maximum angles specified in 3.5.5.

4.5.6 EMI. The PLC shall be tested for EMI in accordance with MIL-STD-461 (see 3.5.6).

4.5.7 Performance. Each PLC and the programming terminal shall be subjected to a performance test to ensure that it meets all performance and design requirements as specified. Verify that the PLC can be powered and the lights are functioning. Verify that a PLC program can be uploaded and stored in non-volatile memory. Verify the proper operation of the input and output modules utilizing appropriate voltage and current signals. Verify the proper operation of the communication links and modules utilizing the appropriate communication protocol.

5. PACKAGING

5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or purchase order (see 6.2). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packing requirements are maintained by the Inventory Control Point's packaging activity within the Military Service or Defense Agency, or within the military service's system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory.)

6.1 Intended use. The PLC system is intended for use when the basic circuit arrangement incorporates ten or more control or timing relays.

6.2. Acquisition requirements. Acquisition documents should specify the following:

a. Title, number, and date of specification.
b. When first article is required (see 3.1).
c. Power requirement (see 3.4.6).
d. PLC processor type (see 3.4.8).
e. Fault indication (see 3.4.8.6).
f. Fixed memory (see 3.4.8.10).
g. Quantity and type of input, output, and communication modules (see 3.4.10).
h. Analog alarm indication (see 3.4.10.8).
i. Alarm requirements (see 3.4.10.10).
j. Network interface and requirements (see 3.4.11).
k. OPC server application (see 3.4.11.9).
l. Network interface requirements (see 3.4.11.12.4.f).
m. Power supply(s) (see 3.4.12).
n. Terminal board(s) size and type (see 3.4.13).
o. Enclosure size and type (see 3.4.14).
p. Paint and graphic displays (see 3.4.14.4).
q. Wiring termination requirements (see 3.4.15).
r. Indicator lights, switches, and other operator devices (see 3.4.16).
s. Non-volatile memory requirements (see 3.4.17.2).
t. Data types (see 3.4.17.12).
u. Application program interface (see 3.4.17.21).
v. Software and license provided (3.4.17.25).
w. Programming format (see 3.4.17.27).
x Diagnostics and state control (see 3.4.18).
y. Type of shock requirement (see 3.5.3).
z Mission specific emissions and susceptibility (see 3.5.6).
ab. Packaging requirements (see 5.1).

6.3 Definitions.

6.3.1 Out-of-range high. The out-of-range high is when the signal is greater than 100.009% of scale.

6.3.2 Out-of-range low. The out-of-range low is when the signal is less than -1.2% of scale.

6.4 Subject term (key word) listing.

Central Processing Unit
Chassis
CPU

Module

Custodians:
Army - CR
Navy - SH
Air Force - 11

Preparing Activity:
Navy - SH
(Project 5998-0116)

Review Activities:
Army - MI
Navy - AS, BC, CG, EC, NW
Air Force - 03, 19, 99,
DLA - CC
CIV - 7FLE

NOTE: The activities listed above were interested in this document as of the date of this document. Since organizations and responsibilities can change, you should verify the currency of the information above using the ASSIST Online database at www.dodssp.daps.mil.