The documentation and process conversion measures necessary to comply with this revision must be completed by 22 December 1999

INCH-POUND

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22 October 1999
SUPERSEDING
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22 October 1998

PERFORMANCE SPECIFICATION

SEMICONDUCTOR DEVICES,
GENERAL SPECIFICATION FOR

This specification is approved for use by all Departments and Agencies of the Department of Defense.

1. SCOPE

1.1 Scope. This specification establishes the general performance requirements for semiconductor devices. Detail requirements and characteristics are specified in the performance specification sheet. Revisions to this and performance specification sheets are structured to assure the interchangeability of devices of the same part type regardless of manufacturing date code or conformance inspection (CI) completion date. Five quality levels for encapsulated devices are provided for in this specification, differentiated by the prefixes JAN, JANTX, JANTXV, JANJ, and JANS. Seven radiation hardness assurance (RHA) levels are provided for the JANTXV and JANS quality levels. These are designated by the letters M, D, L, R, F, G, and H following the quality level portion of the prefix. Two quality levels for unencapsulated devices are provided for in this specification, differentiated by the prefixes JANHC and JANKC.

1.2 Description. This specification contains the performance requirement and verification methods for semiconductor devices. The main body specifies the performance requirements and requires the manufacturer to verify that their devices are capable of meeting those performance requirements. Appendix A contains definitions of terms used throughout the specification. Appendix B contains abbreviations and symbols. Appendix C contains the Quality Management (QM) Program. Appendix D contains the quality system. Appendix E contains the standard verification system for qualified products. Appendix F contains the Radiation Tolerant Source of Supply Program for semiconductor devices. Appendix G contains the standard verification flow for unencapsulated devices. Appendix H contains critical interface and materials for semiconductor devices.

1.3 Identification. The part numbering schemes are as follows:

a. The Part or Identifying Number (PIN) for encapsulated semiconductor devices furnished under this specification is formulated as follows:

JANQQQ	A	XN	YYYY	ZZZ
JAN brand and quality level (see 1.3.1)	RHA designator (see 1.3.4)	Component designation (see 1.3.5)	Identification number (see 1.3.6)	Suffix letters (see 1.3.7)

b. The PIN for unencapsulated semiconductor devices furnished under this specification is formulated as follows:

JANQCW	A	XN	YYYY	ZZ
JAN brand quality level and identifiers (see 1.3.2 and 1.3.3)	RHA designator (see 1.3.4)	Component designation (see 1.3.5)	Identification number (see 1.3.6)	Suffix letters (see 1.3.7)

Beneficial comments (recommendation, additions, deletions) and any pertinent data which may be of use in improving this document should be addressed to: Defense Supply Center Columbus, ATTN: DSCC/VAC, P.O. Box 3990, Columbus OH 45316-5000, by using the Standardization Document Improvement Proposal (DD Form 1426) appearing at the end of this document or by letter.

AMSC N/A FSC 5961

1.3.1 Quality level for encapsulated devices. The quality levels for encapsulated devices includes the JAN brand and associated modifiers as applicable (denoted by "QQQ" in 1.3). These quality levels from the lowest level to the highest level are JAN, JANTX, JANTXV, JANJ and JANS in accordance with appendix E. JANS is intended for space applications. The JANJ quality level is defined in the associated performance specification and in 3.3.1 herein. In performance specification sheets where the JAN level has been removed or omitted, it is acceptable via this document to manufacture and qualify the JAN assurance level once the qualifying activity has been notified and qualification has been extended to the JAN level. In these cases, the manufacturer will also notify the preparing activity to include the JAN level in the next revision of the applicable performance specification sheet.

1.3.2 Quality level for unencapsulated devices. The quality levels for unencapsulated devices includes the JAN brand and associated modifiers as applicable (denoted by "QC" in 1.3b). JANKC is intended for space applications and JANHC is intended for standard military applications.

1.3.3 Manufacturers and critical interface identifiers. W is the place holder for the applicable letter which identifies the manufacturer and the critical interface of a semiconductor die.

1.3.4 RHA designator. The RHA designator is a letter which identifies the applicable RHA level (denoted by "A" in 1.3). The RHA levels from lowest to highest are M, D, L, R, F, G, and H. (See appendix E, table II.)

1.3.5 Component designation. Semiconductor devices are identified by the prefix "XN". The "X" will usually be a number that is one less than the number of active element terminations.

1.3.6 Identification number. It is recommended that each type of semiconductor device intended for standardization be assigned an identification, serially, by the Joint Electron Device Engineering Council, a council sponsored by the Electronic Industries Alliance (EIA) 2500 Wilson Boulevard, Arlington, VA 22201-3834. The assignment will provide the component designation and the identification number.

1.3.7 Suffix letters. The following suffix letters may be incorporated in the military type number as applicable.

A, B, C, etc. (except L, M, R, S, U, P)	Indicates a modified version which is substitutable for the basic numbered (non-suffix) device
M	Indicates matching of specified parameters of separate devices
R	Indicates reverse polarity packaging of the basic numbered device
L or S	Indicates that the terminal leads are longer or shorter, respectively, than those of the basic numbered device
P	Indicates particle impact noise detection (PIND) screened devices (JANTX, and JANTXV only).
U	Indicates unleaded or surface mounted devices (different package configurations may also include a suffix letter).
UR	Indicates unleaded or surface mounted (round end cap diodes).
US	Indicates unleaded or surface mounted (square end cap diodes).
-1	Indicates metallurgical bond.

Suffix letter(s), except for P, must be used and marked on the device only when specific device types are covered by the applicable performance specification sheet requiring the suffix letters (see 3.10.6).

1.3.8 Device substitutions. A device of a higher product assurance level may be substituted for the same basic PIN device of a lower product assurance level. Product assurance levels, in descending order of assurance are: JANS, JANTXV, JANTX, and JAN (for chips, JANKC may replace JANHC). RHA devices tested to a higher total dose requirement may be substituted for the same basic PIN device with a lower total dose requirement (see appendix E, table II). For axial leaded diodes where the same PIN, both with, and without a dash one (-1) suffix exists, the dash one device is considered to be a higher assurance level and may be substituted for the non-dash one part. Non-dash one devices are inactive for new design (whenever dash-one devices exist). For those devices selected to voltage tolerance (e.g., zener diodes, transient voltage suppressors) the tighter tolerance device may be substituted for one of the more relaxed tolerance devices. For those devices selected to temperature coefficient (e.g., voltage reference diodes) the tighter tolerance device may be substituted for one of the more relaxed tolerance devices. Those devices (including unencapsulated devices) having higher voltage ratings may be substituted for lower voltage ratings, provided all other parameters are equal (e.g., 600 PIV for 100 PIV diode). Devices having suffix letters L or S or no lead length designator, may be substituted for each other in applications where the alternate lead length will fit. JANTX 'P' devices are substitutable for JANTX devices and JANTXV 'P' devices are substitutable for JANTXV devices. The part being used for substitution may retain its original marking, or the PIN may be remarked. Lot records must maintain traceability of any remarking.

2. APPLICABLE DOCUMENTS

2.1 General. The documents listed in this section are specified in sections 3 and 4 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements found in documents cited in sections 3 and 4 of this specification, whether or not the documents are listed.

2.2 Government documents.

2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation (see 6.2).

SPECIFICATIONS

DEPARTMENT OF DEFENSE

(See supplement 1 for list of performance specification sheets.)

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-750 - Test Methods for Semiconductor Devices.

(Unless otherwise indicated, copies of the above specifications, standards, and handbooks are available from the Defense Automated Printing Service, Bldg 4D (DPM-DODSSP), 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2.2 Other Government documents, drawings, and publications. The following other Government documents, drawings, and publications form a part of this document to the extent specified herein. Unless otherwise specified, the issues are those cited in the solicitation.

NAVSHIPS 0967-LP-190-4010	Electronic Equipment PAV-1A, -2A, AND -3A Manufacturer Designating Symbols for Navy Type Numbers and Plates For, TM.
QML-19500	Qualified Manufacturers List for Products Qualified Under Performance Specification MIL-PRF-19500, Semiconductor Devices, General Specification For.
DSCC-VQE-19500	Certification and Qualification Information for Manufacturers
MIL-HDBK-5961	List of Standard Semiconductor Devices

2.3 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents which are DoD adopted are those listed in the issue of the DODISS cited in the solicitation. Unless otherwise specified, the issues of documents not listed in the DODISS are the issues of the documents cited in the solicitation (see 6.2).

ELECTRONIC INDUSTRIES ALLIANCE (EIA)

EIA-625	Requirements for Handling Electrostatic Discharge Sensitive (ESDS) Devices.
JEDEC Standard, JESD31	General Requirement for Distributors.

(Application for copies should be addressed to the Electronic Industries Alliance, 2500 Wilson Boulevard, Arlington VA 22201-3834.)

(Non-Government standards and other publications are normally available from the organizations which prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

2.4 Order of precedence. In the event of a conflict between the text of this document and the references cited herein (except for related associated specifications or specification sheets), the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 General requirements. The individual device requirements shall be as specified herein and in accordance with the applicable performance specification. The general requirements of referenced documents shall also apply. Only devices or die listed or approved for listing on the Qualified Manufacturers List (QML) which meet all the performance requirements of the applicable performance specification sheets for the applicable quality level shall be marked and delivered. Any DoD specification or standard referred to in this specification may be replaced by an equivalent commercial standard as determined by the preparing activity and the qualifying activity. If a manufacturer opts to use an equivalent system it is the responsibility of the manufacturer to demonstrate to the qualifying activity equivalence to the applicable requirements.

3.2 Performance specification sheets. The individual item requirements shall be as specified herein and in accordance with the applicable performance specification. In the event of a conflict between the requirements of this specification and the performance specification, the latter shall govern. (If a specific requirement specified herein is not required for an item, it shall be so indicated on the performance specification; for example, Shock, N/A.).

3.3 Performance requirements for JAN, JANTX, JANTXV, and JANS devices and JANHC and JANKC die. It shall be demonstrated that parts delivered to this specification are capable of passing the tests and inspections specified in appendix E or appendix G, as required, for the applicable quality level.

3.3.1 Performance requirements for JANJ devices. The manufacturer of a JANJ device shall be a certified and qualified QPL/QML manufacturer approved by the qualifying activity. The JANJ devices shall be manufactured on a certified and qualified QPL/QML line as defined herein**.** It shall be demonstrated that JANJ devices delivered to this specification are capable of passing the tests and inspections specified in appendix E for JANTXV as a minimum. Manufacturers of JANJ devices shall define a JANJ flow within their Quality System/technology flow. The manufacturer of JANJ devices shall be certified to appendix C or as a minimum certified to appendix D and compliant with the following elements of appendix C: C3, C4, C5, C7, C8.1, C8.3, C8.4, and C8.5. The JANJ flow shall be developed and approved by the manufacturer's Technology Review Board (TRB). Copies of this technology flow including supporting documentation shall be submitted to and approved by the qualifying activity prior to listing as an approved source of supply. This technology flow and supporting documentation shall be available to the systems manufacturers and government customers for review. The customers will be notified of major changes which affect form, fit, or function of the device defined within the device specification and the manufacturer's Quality Management (QM) Program. Major changes will be submitted to the qualifying activity for approval. The qualifying activity will review the suppliers in house space flow for acceptability of use in a space environment prior to JANJ qualification.

3.3.1.1 Radiation requirements. Manufacturers supplying JANJ devices shall demonstrate RHA design capability and the method of characterization shall be documented in the QM program for the radiation hardness assurance level specified for the device offered. All devices supplied to this product class shall be marked with a rad hard designator as specified in table II in appendix E. Traceability shall be established such that there is a technical basis for compliance to the specified RHA level designator as marked on the device.

3.3.1.2 Technology flow. It is the manufacturer's responsibility to document and approve each technology flow through their Technical Review Board (TRB) (see C.4). This flow shall include the design requirements, raw material controls, process controls, tests, screens, and inspection for devices offered to this product class. It is the responsibility of the device manufacturer to optimize the attributes of each technology flow.

3.3.1.3 Part reliability. The device manufacturer shall establish the reliability of each technology offered in this product level and shall baseline the method of calculating the reliability of the technologies offered. The device manufacturer shall maintain an ongoing reliability assessment program.

3.4 Reference to performance specification sheets. For purposes of this specification, when the term "specified" is used without references to a specific document, the intended reference is to the performance specification sheets.

3.5 Certification. The qualifying activity shall verify that the manufacturer's quality system and device verification system meet 4.1, 4.2, and, if applicable, 4.3, and that the manufacturer is producing devices which meet 3.3. Wafer fabrication and assembly operations shall be performed in a facility or facilities certified by the qualifying activity for the applicable technology to the applicable level. The two levels of certification available are JAN, JANTX, JANTXV Certification and JANS Certification. There are two options for obtaining certification from the qualifying activity, either to the Quality Management Program of appendix C or to the Quality System of appendix D. Manufacturers certified to appendix D, qualify products (or families of products) while manufacturers certified to appendix C, qualify manufacturing lines (processes). Each manufacturer's certification status is listed in Section I of QML-19500. Qualified devices supplied by certified manufacturers are listed in Section II of QML-19500. Re-audits are required to maintain certification and qualification. The standard re-audit frequency is two years. This certification period may be extended by the qualifying activity if the manufacturer can demonstrate to the qualifying activity adequate controls of their system.

3.5.1 Transitional certification to appendix C. Manufacturers may be granted transitional certification to appendix C once the manufacturer has completed an audit to appendix C, and has submitted a plan to the qualifying activity and preparing activity for achieving full appendix C implementation. The plan will include self audit results and milestones identifying the tasks necessary for appendix C compliance. As a minimum, the manufacturer will have implemented in C.3.1. The transitional certification will be based on a commitment by the manufacturer to become appendix C certified and if the commitment is not met, the qualifying activity reserves the right to remove the transitional certification.

3.5.2 Diminishing Manufacturing Sources (DMS) Approval. This section was created to provide sources of supply for difficult procurement situations. A DMS source has a verification system that qualifies devices for listing based on MIL-STD-750 laboratory suitability and a limited approval of all the quality system requirements that pertain to laboratory suitability, as follows:

a. Conversion performance specification sheet requirements (see D.3.3).

b. Document control (see D.3.5) including production travelers.

c. Product identification and traceability (see D.3.8).

d. Inspection and test (see D.3.10).

e. Control of measuring and test equipment (see D.3.11).

f. Inspection and test status (see D.3.12).

g. Handling, storage, packaging, and delivery (see D.3.15).

h. Quality records (see D.3.16).

i. Internal Quality Audits (see D.3.17).

j. Training (see D.3.18).

In addition, the following shall be addressed as they apply to inspection and test:

a. Management responsibility (see D.3.1.1, D.3.1.2, D.3.1.3.3, D.3.1.3.4, D.3.1.4, D.3.1.5, D.3.1.6).

b. Quality system (see D.3.2.1, D.3.2.2, D.3.2.3).

c. Control of non conforming product (see D.3.13).

d. Corrective and preventative action (see D.3.14).

3.5.3 DMS listing. Section III of QML-19500 is the DMS qualified products section of the QML. DMS allows qualification of JAN products without certification based on an acceptable qualification report, MIL-STD-750 laboratory suitability, and DMS Approval (see 3.10.10 for part marking). DMS approval will be granted on a case-by-case basis by the qualifying activity. Section III listings may be superseded by any multiple section II listings of the same part number. The qualifying activity will determine when it is appropriate to add or delete a DMS listing. These listings may be an interim step to achieving section II listing or a manufacturer may remain on section III indefinitely.

3.5.4 MIL-STD-750 laboratory suitability. All testing of JAN devices shall be performed at a facility with MIL-STD-750 laboratory suitability, as granted by the qualifying activity, for the applicable test methods (see appendix D).

3.6 Qualification. Devices furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing before contract award (see appendix E).

3.6.1 Qualification options. MIL-PRF-19500L will offer two options of JAN Qualification (in addition to the DMS provisions) : the traditional QPL qualified products approach (see appendix D and E) and the new QML qualified processes approach (see appendix C). They will be clearly identified on our device listings document, which is now redefined as Qualified Manufacturers List (QML). Methods of qualification is further explained in 6.4.1. The QML format is explained in 6.4.2.

3.7 Certification of conformance and acquisition traceability. Manufacturers and Distributors who offer the products as described in this specification shall provide written certification signed by the company or corporate official who has management responsibility for the production of the products, (1) that the product being supplied has been manufactured and shall be capable of passing the tests in accordance with this specification and conforms to all of the requirements as specified herein, (2) that all products are as described on the certificate which accompanies the shipment. The responsible official may, by documented authorization, designate other responsible individuals to sign the certificate, but the responsibility for conformance to the facts shall rest with the responsible official. The certification shall be confirmed by documentation to the Government or to users with Government contracts or subcontracts, regardless of whether the products are acquired directly from the manufacturer or from another source such as a distributor. When other sources are involved, their acquisition certification shall be in addition to the certificates of conformance and acquisition traceability provided by the manufacturer and previous distributors. In no case shall the manufacturer's certificate be altered or show signs of alteration. The certificate shall include the following information:

a. Manufacturer documentation:

(1) Manufacturer's name and address.

(2) Customer's or distributor's name and address.

(3) Device type, quality level, and performance specification sheet number.

(4) Lot identification code (including assembly plant code).

(5) Inspection date.

(6) Quantity of devices in shipment from manufacturer.

(7) Statement certifying product conformance and traceability.

(8) Signature and date of transaction.

(9) Solderability inspection date and re- inspection date (only when performed, see 3.11).

(10) “DMS” marking for part III listing in accordance with 3.5.2 herein.

b. Distributor documentation for each distributor:

(1) Distributor's name and address.

(2) Name and address of customer.

(3) Quantity of devices in shipment.

(4) Certification that this shipment is a part of the shipment covered by the manufacturer's documentation, and an attached copy of the manufacturer's original certification.

(5) Signature and date of transaction.

(6) Certification that Authorized dealers and distributors have handled the products in accordance with the requirements of JEDEC Standard JESD 31 and EIA-625.

(7) Solderability inspection date and re- inspection date (only when performed, see 3.11).

(8) ”DMS” marking for part III listing.

(9) Device type, quality level, and performance specification sheet number.

3.8 Critical interface and materials. Critical interface and materials for devices furnished under this specification shall be such that the devices meet the performance requirements of 3.3 (see appendix H).

3.9 Lead and terminal finish. The lead and terminal finish shall be in accordance with appendix H herein.

3.10 Marking.

3.10.1 Marking on each device. The following marking shall be placed on each encapsulated semiconductor device and shall be legible. Devices having inadequate marking area for all applicable markings shall have as many of the following as possible in the following order of precedence (with "a." being most important). Unencapsulated semiconductor devices (die) do not require individual device marking.

a. Polarity marking, when applicable (see 3.10.5).

b. PIN (see 3.10.6).

c. Manufacturer's name, trademark, or identification (see 3.10.12) or manufacturer's designating symbol (see 3.10.7).

d. Lot identification code and code for plants (see 3.10.8 and 3.10.8.2).

e. Serial number, if applicable (see 3.10.9).

f. “DMS” marking, if applicable (See 3.10.10).

g. Special marking (see 3.10.3). Beryllium oxide identifier (see 3.10.3.2). The “P” suffix marking for PIND testing (see 1.3.7) may follow the type number or be marked any place on the device within the marking area.

h. Electrostatic discharge sensitivity (ESDS) identifier (optional see 3.10.3.1).

i. Country of origin (optional see 3.10.11).

3.10.2 Marking on initial container (unit package). All device marking, except for polarity and serial numbers, shall also appear on the unit package used as the initial protection for delivery. See appendix G, section G.6.2 for marking requirements of die unit packaging.

3.10.3 Special marking. If any special marking is used, it shall in no way interfere with or obscure the marking required in 3.10.1.

3.10.3.1 ESDS identifier ESDS testing shall be done in accordance with test method 1020 of MIL-STD-750. Unless otherwise specified, tests shall be performed for initial qualification and product redesign. When a device's ESDS class is determined by the ESDS classification test (see appendix E), the devices represented by the test may at the option of the manufacturer be marked as follows:

Class 1	1,999 V and below	Δ - single equilateral triangle outline or solid (still acceptable as pin one designator).
Class 2	2,000 V to 3,999 V	$\Delta\Delta$ - double equilateral triangle outline or solid (still acceptable as pin one designator).
Class 3	4,000 V to 15,999 V	no designator.
Non-sensitive	Above 15,999 V	no designator.

3.10.3.2 Beryllium oxide package identifier. If a semiconductor package contains beryllium oxide (beryllia), the device shall be marked with the designation 'BeO'.

3.10.4 Marking legibility. Marking shall remain legible. Marking damage caused by mechanical handling shall not be cause for lot rejection. Devices having damaged markings shall be remarked prior to shipment to insure legibility.

3.10.5 Polarity marking of unidirectional diodes and thyristors. The polarity shall be indicated by one of the following methods.

3.10.5.1 Diodes.

a. A diode graphic symbol or arrow with the arrow pointing toward the cathode terminal for forward bias.

b. A single contrasting color band or a minimum of three contrasting color dots spaced around the periphery on the cathode end may be used.

c. An ESD identifier may be used to indicate polarity for sensitive devices.

NOTE: U, US or UR diodes shall have a cathode band or three dots indicating cathode end.

3.10.5.2 Thyristors. A graphic symbol for a thyristor with the arrow pointing toward the cathode terminal (for stud-mounted thyristors only).

3.10.6 PIN. Each semiconductor device shall be marked with the type designation which shall be formulated as shown in 1.3. If the device size does not allow the complete PIN to be marked on the device, the component designation portion (see 1.3.5) shall be omitted first followed by the quality level. RHA designators will be included to the abbreviated PIN as appropriate.

3.10.6.1 JAN and J marking. The United States Government has adopted, and is exercising legitimate control over the certification marks "JAN" and "J", respectively, to indicate that items so marked or identified are manufactured to, and meet all the requirements of the applicable specification, including qualification. Accordingly, items acquired to, and meeting all of the criteria specified herein and in applicable specifications shall bear the certification mark "JAN" except that items too small to bear the certification marked "JAN" shall bear the letter "J". The "JAN" or "J" shall be placed immediately before the part number except that if such location would place a hardship on the manufacturer in connection with such marking, the "JAN" or "J" may be located on the first line above or below the part number. Items furnished under contracts or orders which either permit or require deviation from the conditions or requirements specified herein or in applicable specifications shall not bear "JAN" or "J". In the event an item fails to meet the requirements of this specification and the applicable performance specification sheets, the manufacturer shall remove completely the military part number and the "JAN" or the "J" from the sample tested and also from all items represented by the sample. The “JAN“ or “J” certification mark shall not be used on products acquired to contractor drawings or specifications (see 6.2.1). The United States Government has obtained Certificate of Registration Number 504,860 for the certification mark "JAN" and Registration Number 1,586,261 for the certification mark "J".

3.10.6.1.1 JAN branded prefix. The type number of all semiconductor devices acquired to and meeting the requirements of this specification and the applicable performance specification sheet shall bear the applicable prefix. In the case of small size semiconductor devices, the abbreviated prefix J (for JAN) ,JJ (for JANJ), JX (for JANTX), JV (for JANTXV), JS (for JANS) may be used.

3.10.7 Manufacturer's designating symbol. The manufacturer's designating symbol shall be as listed in the QML and assigned by the qualifying activity. The symbol shall be used only by the manufacturer to whom it has been assigned and only on those devices manufactured at that manufacturer's plant. In the case of small devices, the manufacturer's designating symbol may be abbreviated by omitting the first "C" in the series of letters. (See 3.10.12)

3.10.8 Lot identification code. Semiconductor devices shall be marked by a code indicating the last week of sealing for the inspection lot accumulation period. The first two numbers in the code shall be the last two digits of the number of the year. The third and fourth numbers shall be two digits indicating the calendar week of the year. When the number of the week is a single digit, it shall be preceded by a zero. Reading from left to right or top to bottom, the code number shall designate the year and week. For axial diodes, the lot identification code is required for DO-35 package sizes and larger.

3.10.8.1 Lot identification code suffix letter. When more than one lot of a device type sealed within the same lot accumulation period is submitted for conformance inspection, a lot identification code suffix letter, consisting of a single capital letter, shall appear on each semiconductor device immediately following the date code. This letter shall be chosen by the manufacturer so that each inspection lot is uniquely identified by the lot identification code and by the lot identification suffix letter, if one is required.

3.10.8.2 Code for plants. If the devices are assembled or fabricated at a plant other than the basic plant, the lot identification code shall include a single letter which uniquely identifies the plant. This plant designator shall appear immediately preceding and adjacent to the date code. The plant designator will be listed with the addresses in the QML.

3.10.9 Serialization. JANS devices and, when specified, other device levels shall be marked with a unique serial number assigned consecutively within the inspection lot. JANS devices shall be marked with the serial number in screening, and inspection lot records shall be maintained to provide traceability from the serial number to the specific wafer lot from which the devices originated. For small devices with insufficient area for serialization, lead or body tags may be used.

3.10.10 DMS marking. The DMS marking applies to qualified product listed on section III of the QML. The DMS mark is not part of the part number, and will not be included in the PIN and shall be distinctly separate from all other marking. "DMS” may be abbreviated as “D”.

3.10.11 Country of origin. The manufacturer shall indicate the country of origin of the device if other than USA. At the option of the manufacturer the country of origin marking may be omitted from the body of the device but shall be retained on the initial container.

3.10.12 Manufacturer's name, abbreviation, or trademark. At the manufacturer's option, devices supplied to this specification may be marked with the device manufacturer's name, abbreviation, or trademark in place of the designating symbol described in 3.10.7, except for a manufacturer with multiple facility locations. The name or trademark of only the original manufacturer shall appear on the device or initial container. Alteration of name or trademark shall not be permitted.

3.10.13 Marking option. Except for serialization, the manufacturer has the option of marking the entire lot or only the sample devices prior to Conformance Inspection (CI). If the manufacturer exercises the option to mark only the sample devices, the procedure shall be as follows:

a. The sample devices shall be marked prior to performance of conformance or qualification inspection.

b. At the completion of inspection, the marking of the sample devices shall be inspected for conformance with the requirements of 3.10.1 and 3.10.4.

c. The inspection lot represented by a conforming inspection sample shall then be marked and any specified visual and mechanical inspection performed.

d. The marking materials and processing applied to the inspection lot shall be to the same specification as those used for the inspection sample.

3.11 Solderability. All parts shall be capable of passing the solderability test in accordance with MIL-STD-750, test method 2026, on delivery. Re-inspection of solderability is not required by this specification. However, when solderability re-inspection is performed (either at the option of the manufacturer, or by customer contract), the re-inspection date shall appear on all subsequent Certificates of Conformance and Traceability (See 3.7).

3.12 ESD control. Semiconductors classified as class 1 or 2 (see E4.2.1.1) shall be handled in accordance with EIA-625 or other industry standard practice, to safeguard against discharge damage, as applicable.

3.13 Traceability. All devices delivered to this specification shall be identified (see 3.7 and 3.10.1) such that they shall be traceable through the lot identification code and inspection lot records. In addition, JANS devices shall have a lot control system from wafer processing through screening which provides wafer lot identification, operation (machine), date of operation, operator(s) identification, quantity, and serial numbers of devices processed.

3.14 Recycled, recovered, or environmentally preferable materials. Recycled, recovered, or environmentally preferable materials should be used to the maximum extent possible provided that the material meets or exceeds the operational and maintenance requirements, and promotes economically advantageous life cycle costs.

4. VERIFICATION

4.1 Quality system. The manufacturer shall implement and maintain a quality system. This system shall assist the manufacturer in producing devices which meet section 3. See appendix D for the quality system to be maintained by qualified suppliers to this specification. See appendix C for the optional Quality Management Program.

4.2 Device verification. The manufacturer shall implement and maintain a verification program which demonstrates that devices meet section 3. Appendix E is the standard verification flow for qualified products, appendix G is the standard verification flow for unencapsulated devices.

4.2.1 Classification of inspections. The inspection requirements specified herein are classified as follows:

a. Qualification inspection (see appendix E).

b. Screening (see appendix E).

c. Conformance inspection (CI)(see appendix E).

d. Element evaluation (see appendix G).

4.3 Radiation tolerant source of supply program. Appendix F may be used in developing a radiation tolerant source of supply.

4.4 Test modification, reduction, or elimination. Tests and inspections may be modified, reduced, or eliminated with the approval of the Preparing Activity and the qualifying activity. When a manufacturer modifies, reduces, or eliminates a test or inspection, the manufacturer is only relieved of the responsibility of performing that test or inspection. The manufacturer is still responsible for providing product which meets 3.

5. PACKAGING

5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When actual packaging of materiel is to be performed by DoD personnel, these personnel need to contact the responsible packaging activity to ascertain requisite packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activity within the Military Department or Defense Agency, or within the Military Department's System Command. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contracting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory.)

6.1 Intended use. This specification covers the general requirements for semiconductor devices used in electronic equipment. The semiconductor devices covered by this specification are unique due to the fact that these devices must be able to operate satisfactorily in systems under demanding conditions such as: 20 g's vibration, 100 g's of shock, salt atmosphere, wide temperature range (e.g. -55°C to +150°C. In addition, these requirements are verified under a qualification system. Commercial components are not designed to withstand these environmental conditions.

6.2 Acquisition requirements. Acquisition documents must specify the following:

a. Title, number, and date of this specification.

b. Issue of DoDISS to be cited in the solicitation, and if required, the specific issue of individual documents referenced (see 2.2.1).

c. Packaging requirements (see 5.1).

d. PIN (see 1.3).

e. Number of the applicable performance specification sheets (see 3.2 and supplement 1 of this document). For additional information on PINs not included in supplement 1, contact the Defense Supply Center Columbus, DSCC-VAC, P.O. Box 3990, Columbus, OH 43216-5000.

f. Lead formation, length, finish, if other than that specified, or when a choice is required by the device application.

g. Data requirements, when applicable.

h. Specify point of shipment.

i. PIND screening when required.

j. Date code and specification revision letter should not be restricted by the acquisition documents (see 3.10.8).

6.2.1 Purchase order requirements. The Date code and specification revision letter should not be restricted by the acquisition documents (see 3.10.8) The JAN brand or the abbreviations (See 3.10.6) must not be used on any semiconductor device acquired under contracts which permit or require any changes to this specification or the applicable performance specification sheet, except for:

a. Lead length.

b. Lead finish.

c. PIND testing. PIND screening to requirements beyond those specified herein may be performed only when imposed by the acquisition document upon the component manufacturer. A new PIN will be created in accordance with 1.3 and 3.10.3. Devices which pass such screens may be JAN branded or may retain the JAN brand if already marked. All devices failing such screens must not be JAN branded or, if already marked must have the JAN brand removed or the device destroyed.

d. Lead forming (See E.5.3.5). The forming of leads must not be performed except for specific customer purchase orders where the lot is controlled throughout processing by specific lot travelers. The bend must not be closer than .050 inch (1.27 mm) to the lead to package seal.

e. Additional marking

6.3 Supersession information. Devices covered by performance specification sheets are substitutable for the manufacturer's and user's PIN's. This information in no way implies that manufacturer's PINs are suitable as a substitute for the military PIN. The table below is an example of the type of cross reference data that should be available in the performance specification sheets.

Supersession and cross reference data.

Military PIN	Manufacturer's CAGE code	Manufacturer's and user's PIN

6.4 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of a contract, qualified for inclusion in QML, whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or orders for the products covered by this specification. The information pertaining to qualification of products may be obtained from the Defense Supply Center Columbus, P.O. Box 3990, Columbus, OH 43216.

6.3.1 Methods of qualification. There are two methods to supply JAN semiconductors to MIL-PRF-19500. Appendix D and appendix E defines the historical screening, sampling and quality system approach formerly listed on the Qualified Products List (QPL). Appendix C defines the Qualified Manufacturers List approach. It includes the following important features:

a. Technical Review Board.

b. Optimization.

c. Quality planning.

d. Statistical Techniques.

e. On Going Reliability Program (Fit rate prediction).

f. Quality Management Plan.

g. Product characterization and capability evaluation.

h. FMEA.

One method is not preferred over the other. When large volume device production is typical the (see appendix C) Qualified Manufacturer approach, which focuses on qualifying the process and production line, offers significant advantages to the supplier. Small companies with modest volumes often find the historical "Qualified Products" approach more cost effective. Suppliers should choose their method based on their business environment. Leveraging off high volume commercial lines has proven to be effective in the Microcircuit QML. However, the majority of our JAN semiconductor suppliers do not have similar high volume commercial production to leverage from.

6.4.2 QML format. QML-19500 will be divided into three sections. Section I will alphabetically list manufacturers with the following information as a minimum:

a. Manufacturers' name, Manufacturers' Management Representative, address, fax, e-mail and phone number,

b. Location of wafer fabrication, assembly and test operations,

c. Contracted operations (if applicable),

d. Technology and package certifications,

e. Cage code and manufacturing designating symbol and logo,

f. Qualified Manufactures approval status (appendix C certification),

g. Qualified products approval status (appendix D certification, or DMS approval),

h. MIL-STD 750 laboratory suitability status.

The second section will include all device listings qualified by the manufacturer. Section II will list part number, ESD class, manufacturers designating symbol, qualification reference, performance specification sheets and manufacturer's plants. Section III is for DMS sources, (see 3.5.1) and will be organized the same as section II.

6.5 Intent and definition of JANJ level. In addition, the JANJ level is intended to be a flexible JANTXV plus quality level which contains the essential supplier imposed requirements and design ruggedness to perform in a space environment. JANJ was conceived to standardize suppliers in house space flows and offer an alternative to up screening and customer drawings generated by space customers who do not need and will not buy a JANS device. JANJ level is not intended as a replacement for high-reliability JANS product nor would it be appropriate to do so in many applications.

6.6 Subject term (key word) listing:

Conformance inspection (CI)
Double plug construction
Electrostatic discharge sensitivity (ESD)
Failure analysis (FA)
Metallurgical bond
Qualification
Qualified manufacturers listing (QML)
Radiation hardness assurance (RHA)
Statistical process control (SPC)
Technical review board (TRB)
Test optimization
Thermal match
Thermal response

6.7 PIN. This specification requires a PIN that describes codification and/or classification and appropriate references to associated documents (see 1.3 and 3.2 herein).

6.8 Changes from previous issue. Marginal notations are not used in this revision to identify changes with respect to the previous issue due to the extensiveness of the changes.

APPENDIX A

DEFINITIONS

A.1 SCOPE

A.1.1 Scope. This appendix contains the definitions of terms used with semiconductor devices. This appendix is not a mandatory part of this specification. The information contained herein is intended for guidance only.

A.2 APPLICABLE DOCUMENTS.

A.2.1 General. The documents listed in this section are specified in sections 3 and 4 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements found in documents cited in sections 3 and 4 of this specification, whether or not the documents are listed.

A.2.2 Government documents.

A.2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation (see 6.2).

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-750 - Test Methods for Semiconductor Devices.

(Unless otherwise indicated, copies of the above specifications, standards, and handbooks are available from the Defense Automated Printing Service, Bldg 4D (DPM-DODSSP), 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

A.2.3 Order of precedence. In the event of a conflict between the text of this document and the references cited herein (except for related performance specification sheets), the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

A.3 SEMICONDUCTOR COMMON DEFINITIONS

A.3.1 Absolute maximum ratings. The values specified for "ratings", "maximum ratings", or "absolute maximum ratings" are based on the "absolute system" and unless otherwise required for a specific test method are not to be exceeded under any service or test conditions. These ratings are limiting values beyond which the serviceability of any individual semiconductor device may be impaired. Unless otherwise specified, the voltage, current, and power ratings are based on continuous dc power conditions at free air ambient temperature of +25°C. For pulsed or other conditions or operation of similar nature, the current, voltage, and power dissipation ratings are a function of time and duty cycle. In order not to exceed absolute ratings, the equipment designer has the responsibility of determining an average design value, for each rating, below the absolute value of that rating by a safety factor, so that the absolute values will never be exceeded under any usual conditions of supply-voltage variation, load variation, or manufacturing variation in the equipment itself.

A.3.2 Ambient temperature. Ambient temperature is the air temperature measured below a semiconductor device, in an environment of substantially uniform temperature, cooled only by natural air convection and not materially affected by reflective and radiant surfaces.

A.3.3 Anode. The electrode from which the forward current flows within the device.

A.3.4 Performance specification sheet. Since this specification covers the general requirements and tests for semiconductor devices, the details of performance of the semiconductor device must be specified in the performance specification sheet. Items listed below should be covered in the performance specification sheet:

a. PIN (see 1.3)

b. Generic design, construction, and material (see appendix H).

c. The marking to be omitted if any (see 3.10). The order of precedence for marking is as listed in 3.10.1.

d. Classification of inspection.

e. Examination and tests to be performed under qualification inspection.

f. Examination and tests to be performed under CI.

g. Examination and tests to be performed under screening inspection.

h. End-point measurements to be made for group A B, C, D, and E inspections (see appendix E).

i. Quality levels covered.

j. Device level and screening procedure if other than table IV.

k. Sequence of test, test method, test condition, limit, cycles, temperature, or axis; when not specified, or if other than specified herein.

l. Interim (pre- and post-burn-in) electrical parameters.

m. Burn-in test condition and burn-in test circuit.

n. Delta parameter measurements or provisions for PDA including procedures for traceability, where applicable.

o. Final electrical measurements.

p. Requirements for data recording and reporting, where applicable.

A.3.4.1 MIL-STD-750 details. In addition to the items as specified in A.3.4, the applicable details required by MIL-STD-750 should be listed in the performance specification sheet.

A.3.5 Blocking. A term describing the state of a semiconductor device or junction which eventually prevents the flow of current.

A.3.6 Breakdown voltage. The breakdown voltage is the maximum instantaneous voltage, including repetitive and nonrepetitive transients, which can be applied across a junction in the reverse direction without an external means (circuit) of limiting the current. It is also the instantaneous value of reverse voltage at which a transition commences from a region of high small-signal impedance to a region of substantially lower small-signal impedance.

A.3.7 Case mount. A type of package (outline) which provides a method of readily attaching one surface of the semiconductor device to a heat dissipater to achieve thermal management of the case temperature (example: TO-3, DO-4).

A.3.8 Case temperature. Case temperature is that temperature measured at a specified point on the case of a semiconductor device.

A.3.9 Cathode. The electrode to which the forward current flows within the device.

A.3.10 Characteristic. An inherent and measurable property of a device. Such a property may be electrical, mechanical, thermal, hydraulic, electromagnetic, or nuclear, and can be expressed as a value for stated or recognized conditions. A characteristic may also be a set of related values usually shown in graphical form.

A.3.11 Control plans. Control plans are written descriptions of the system for controlling parts and processes. They are written by suppliers to address the importance characteristics and engineering requirements of the product. Each part shall have a control plan, but in many cases “family “ control plans can cover a number of part products using a common process.

A.3.12 Constant current source. A current source shall be considered constant if halving the generator impedance does not produce a change in the parameter being measured that is greater than the required precision of the measurement.

A.3.13 Constant voltage source. A voltage source shall be considered constant if doubling the generator impedance does not produce a change in the parameter being measured that is greater than the required precision of the measurement.

A.3.14 Disc type. A type of package (outline) for very high power devices which provides two parallel surfaces for mounting into a specialized heat dissipator capable of applying a specified compressive force to the device.

A.3.1.5 Engineering evaluation. An engineering evaluation is an in depth scientific investigation of anomalies or potential problems to determine root cause and provide solutions. An analysis of a possible non-conformance or quality defect will be performed by appropriate engineers or applicable technical experts. An assessment of the damage or nonconformance will be documented and corrective action will be implemented. Conclusions are based on visual inspection, data, past history, failure analysis, DPA, delidding, step stress testing, electric screening, or any reasonable tool or combinations of tools. In all cases the qualifying activity will be notified.

A.3.16 Failure analysis. Failure Analysis (FA) is the discipline incorporating all techniques of physical, chemical and Electro-magnetic (EM) characterization of product and/or materials to isolate the mode of failure and define the mechanism of occurrence. FA is used as an integral tool in root cause determination and process-segment targeting in the corrective action procedure.

A.3.17 Forward bias. The bias which tends to produce current flow in the forward direction (p type semiconductor region at a positive potential relative to n type region).

A.3.18 Failure Mode and Effects Analysis (FMEA). A FMEA is an analytical technique used as a means to assure potential failure modes and their associated causes/mechanisms have been considered and addressed. The process and design FMEA's should identify process and design failure modes, and identify process and design variables on which to focus controls for detection and occurrence reduction. It develops a list of potential failure modes and establishes a priority system for corrective action considerations. Creation of the FMEA should start with the process flow. A potential failure mode is defined as the manner in which the process could potentially fail to meet the process requirements or design intent. FMEAs also include information on potential effects of failure, severity level, potential causes, current process controls as well as other information.

A.3.19 Metallurgical bond, diode construction, and thermal matching. Metallurgical bonds as used in JAN-brand semiconductor devices will be identified by one of the following categories. The listing of the three types of metallurgical bonds is for clarification and may not necessarily be listed in order of merit.

A.3.19.1 Double plug construction. Double plug construction is one where the terminal plugs have equal nominal diameters. Plug contact with the semiconductor die may be achieved either through direct contact with the die metallization materials or via brazing or solder preform metallization. The use of a point contact whisker or other wire conductors is not allowed.

A.3.19.2 Dash-one construction. Dash-one diodes shall be of double plug construction utilizing high temperature metallurgical bonding between both sides of the silicon die and attach preform or terminal pins.

A.3.19.3 Category I metallurgical bond. A category I metallurgical bond is formed when the bond between the semiconductor element (such as silicon or germanium.) and the package consists of a phase which melts during the bonding process and which includes in the solidified melt both a portion of the semiconductor element and a portion of the metallization layer which is on the package mounting surface. Category I bonds between adjacent semiconductor elements (as in stacks) shall include portions of both semiconductor elements in the solidified melt. Unless otherwise specified in the performance specification sheet, category I metallurgical bonds are typically required for all axial leaded diodes, equal to and greater than 1 watt or 1 amp.

A.3.19.4 Category II metallurgical bond. A category II metallurgical bond is formed utilizing a brazing or soldering alloy which melts during the bonding process and bonds to a metallization layer on each of the surfaces being joined. Dissolution of the semiconductor element or any of the wetted surface layers is not required.

A.3.19.5 Category III metallurgical bond. A category III metallurgical bond is formed when the surfaces to be bonded are brought together under conditions of temperature and pressure such that a diffusion bond is formed between the outermost metallization layer of the elements being joined. This bond is characterized by having species from both sides of the original interface diffused across the interface without any molten phase having been present.

A.3.19.6 Non-cavity double plug diode. Double plug construction where the package glass is in intimate contact with the semiconductor die isolating the anode and cathode regions, and insuring immunity from particle related failures. Voids may be present provided isolation (to prevent arcing) and particle immunity are insured.

A.3.19.7 Thermally matched axial leaded diodes. Diode construction within the coefficients of thermal expansion of the die, plug, and package materials shall be thermally matched such that the diodes are immune to intermittent opens by design. Axial-leaded diode critical interfaces which comply with this definition must utilize tungsten or molybdenum plugs.

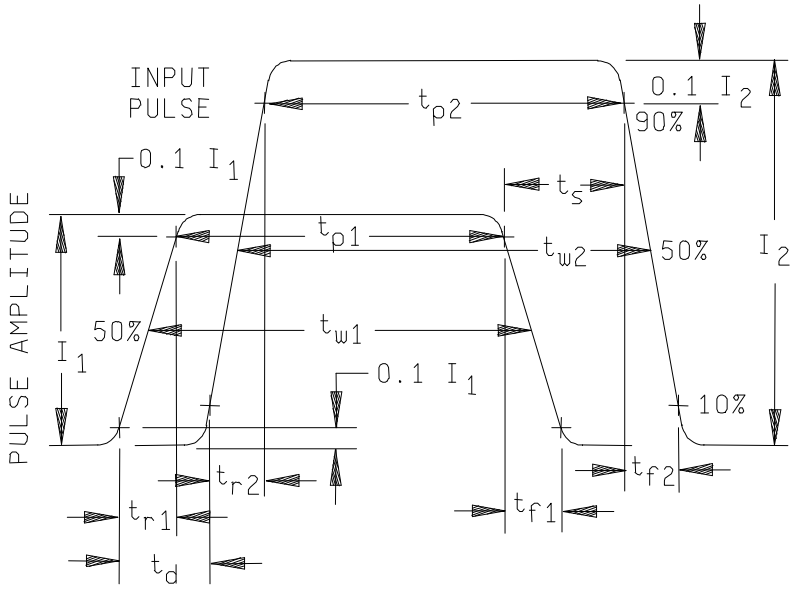
A.3.19.8 Metallurgically bonded-thermally matched-noncavity-double plug construction. Axial-leaded diodes meeting this definition must be of double plug construction utilizing tungsten or molybdenum plugs. Both sides of the diode chip (die) must be bonded to the corresponding plug by a category I metallurgical bond. The package must be thermally matched, non-cavity construction (see A.3.19.1 through A.3.19.3, A.3.19.6, and A.3.19.7). The plated silver button contact design is not permitted.

A.3.20 Noise figure. At a selected input frequency, the noise figure is the ratio of the total noise power per unit bandwidth (at a corresponding output frequency) delivered to the output termination, to the portion thereof contributed at the input frequency by the input termination, whose noise temperature is standard (293°K) at all frequencies.

A.3.21 Open circuit. A circuit shall be considered as open circuited if halving the magnitude of the terminating impedance does not produce a change in the parameter being measured greater than the specified accuracy of the measurement.

A.3.22 Package type. A package type is a package which has the same case outline, configuration, materials (including bonding, wire, or ribbon and die attach) piece parts (excluding preforms which differ only in size) and assembly processes.

A.3.23 Pulse. A pulse is a flow of electrical energy of short duration. See figure 1 for illustrations of the characteristics defined in A.3.24 to A.3.29, inclusive.



t_r = Pulse rise time.

t_d = Pulse delay time.

t_p = Pulse time.

t_s = Pulse storage time.

t_f = Pulse fall time.

t_w = Pulse average time.

I = Pulse amplitude.

NOTES:
1. Subscript 2 denotes output.
2. Subscript 1 denotes input.

FIGURE 1. Pulse measurements.

A.3.24 Pulse average time. The average pulse time of a pulse is the time duration from a point on the leading edge which is 50 percent of the maximum amplitude to a point on the trailing edge which is 50 percent of the maximum amplitude.

A.3.25 Pulse delay time. The delay time of a pulse is the time interval from a point at which the leading edge of the input pulse has risen to 10 percent of its maximum amplitude to a point at which the leading edge of the output pulse has risen to 10 percent of its maximum amplitude.

A.3.26 Pulse fall time. The fall time of a pulse is that time duration during which the amplitude of its trailing edge is decreasing from 90 to 10 percent of the maximum amplitude.

A.3.27 Pulse rise time. The rise time of a pulse is that time duration during which the amplitude of its leading edge is increasing from 10 to 90 percent of the maximum amplitude.

A.3.28 Pulse storage time. The storage time of a pulse is the time interval from a point 10 percent down from the maximum amplitude on the trailing edge of the input pulse to a point 10 percent down from the maximum amplitude on the trailing edge of the output pulse.

A.3.29 Pulse time. The pulse time of a pulse is the time interval from the point on the leading edge which is 90 percent of the maximum amplitude, to the point on the trailing edge which is 90 percent of the maximum amplitude.

A.3.30 Radiation failures. A radiation failure is defined at the lowest radiation level when either any device parameter exceeds its specified post irradiation parameter limits (PIPL) or the device fails any functional test in accordance with stated test conditions.

A.3.31 Radiation hardness assurance (RHA). That portion of performance verification testing that assures that parts meet the radiation response characteristics as specified in this specification and the performance specification sheet.

A.3.32 Rating. The nominal value of any electrical, thermal, mechanical, or environmental quantity assigned to define the operating conditions under which a component, machine, apparatus, or electronic device is expected to give satisfactory service.

A.3.33 Reverse bias. The bias which tends to produce current flow in the reverse direction (n type semiconductor region at a positive potential relative to the p type region).

A.3.34 Semiconductor devices. Electronic device in which the characteristic distinguishing electronic conduction takes place within a semiconductor.

A.3.35 Semiconductor diode. A semiconductor device having two terminals and exhibiting a nonlinear voltage-current characteristic.

A.3.36 Semiconductor junction. A region of transition between semiconductor regions of different electrical properties (e.g., n-n+, p-n, p-p+ semiconductors) or between a metal and a semiconductor.

A.3.37 Short circuit. A circuit shall be considered short-circuited if doubling the magnitude of the terminating impedance does not produce a change in the parameter being measured that is greater than the specified accuracy of the measurement.

A.3.38 Small signal. A signal shall be considered small if doubling its magnitude does not produce a change in the parameter being measured that is greater than the specified accuracy of the measurement.

A.3.39 Storage temperature. Storage temperature is a temperature at which the device may be stored without any power being applied.

A.3.40 Temperature coefficient. The ratio of the change in a parameter to the change in temperature.

A.3.41 Thermal compression bond. A bond achieved when pressure and temperature are present regardless of how the temperature rise was achieved except without ultrasonic assist.

A.3.42 Thermal equilibrium. Thermal equilibrium is reached when doubling the test time interval does not produce a change, due to thermal effects, in the parameter being measured that is greater than the specified accuracy of the measurement.

A.3.43 Thermal resistance. Thermal resistance is the temperature rise, per unit power dissipation, of a junction above the temperature of a stated external reference point under conditions of thermal equilibrium.

A.3.44 Thyristor. A bi-stable semiconductor device that comprises three or more junctions and can be switched from the off state or on state to the opposite state.

A.3.45 Transistor. An active semiconductor device capable of providing power amplification and having three or more terminals.

A.3.46 Expanded metallization. Expanded metallization is metallization that increases in area (example, metal line to bond pad area) (see figure 2).

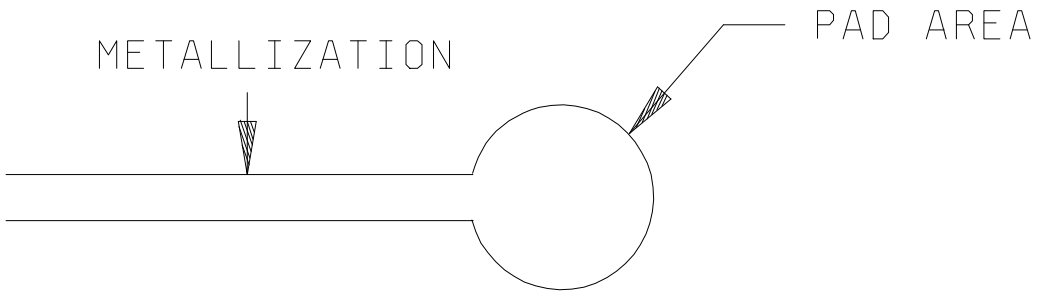


FIGURE 2. Example of expanded metallization.

A.3.47 Impulse waveform. A pulse with a defined virtual front and impulse duration for either a voltage or current amplitude of unidirectional polarity.

A.3.48 Virtual front duration. The pulse time as defined by 1.67 times time for voltage to increase from 30 percent to 90 percent of crest (peak value) or 1.25 times time for current to increase from 10 percent to 90 percent of crest.

A.3.49 Impulse duration. The time required for an impulse waveform to decay to 50 percent of the peak value measured from the start of the virtual front duration of zero crossover.

A.3.50 Line. A collection of similar wafer fabrication flows, or similar package assembly flows used to manufacture semiconductors in accordance with a specified process flow.

A.4 TRANSISTOR DEFINITIONS

A.4.1 Junction transistors, multijunction types.

A.4.1.1 Base. A region which lies between an emitter and collector of a transistor and into which minority carriers are injected.

A.4.1.2 Collector. A region through which a primary flow of charge carriers leaves the base.

A.4.1.3 Cutoff current. The cutoff current is the measured value of dc current when a transistor is reverse biased by a voltage less than the breakdown voltage.

A.4.1.4 Emitter. A region from which charge carriers that are minority carriers in the base are injected into the base.

A.4.1.5 Junction, collector. A semiconductor junction, normally biased in the reverse direction, the current through which can be controlled by the introduction of minority carriers into the base.

A.4.1.6 Junction, emitter. A semiconductor junction normally biased in the forward direction to inject minority carriers into the base.

A.4.1.7 Saturation. A base current and a collector current condition resulting in a forward-biased collector junction.

A.4.2 Unijunction transistors.

A.4.2.1 Peak point. The point on the emitter current-voltage characteristic corresponding to the lowest current at which the change in emitter base voltage with respect to emitter current equals zero.

A.4.2.2 Unijunction transistor. A three-terminal semiconductor device having one junction and a stable negative-resistance characteristic over a wide temperature range.

A.4.2.3 Valley point. The point on the emitter current-voltage characteristic corresponding to the second lowest current at which the change in emitter base voltage with respect to emitter current equals zero.

A.4.3 FETs.

A.4.3.1 Depletion-mode operation. The operation of a FET such that changing the gate to source voltage from zero to a finite value decreases the magnitude of the drain current.

A.4.3.2 Depletion-type-FET. A FET having appreciable channel conductivity for zero gate to source voltage. The channel conductivity may be increased or decreased according to the polarity of the applied gate to source voltage.

A.4.3.3 Drain. A region into which majority carriers flow from the channel.

A.4.3.4 Enhancement-mode operation. The operation of a FET such that changing the gate to source voltage from zero to a finite value increases the magnitude of the drain current.

A.4.3.5 Enhancement-mode FET. A FET having substantially zero channel conductivity for zero gate to source voltage. The channel conductivity may be increased by the application of a gate to source voltage of appropriate polarity.

A.4.3.6 FET. A transistor in which the conduction is due entirely to the flow of majority carriers through a conduction channel controlled by an electric field arising from a voltage applied between the gate and source terminals.

A.4.3.7 Gate. The electrode associated with the region in which the electric field due to the control voltage is effective.

A.4.3.8 Insulated-gate FET. A FET having one or more gate electrodes which are electrically insulated from the channel.

A.4.3.9 Junction-gate FET. A FET that uses one or more gate regions to form p-n junction(s) with the channel.

A.4.3.10 MOSFET. An insulated gate FET in which the insulating layer between each gate electrode and the channel is oxide material.

A.4.3.11 N-channel FET. A FET that has an n type conduction channel.

A.4.3.12 P-channel FET. A FET that has a p type conduction channel.

A.4.3.13 Source. A region from which majority carriers flow into the channel.

A.5 DIODE AND RECTIFIER DEFINITIONS

A.5.1 Signal diodes and rectifier diodes.

A.5.1.1 Semiconductor rectifier diode. A device having an asymmetrical voltage-current characteristic used for rectification.

A.5.1.2 Semiconductor signal diode. A device having an asymmetrical voltage-current characteristic and used for signal detection.

A.5.2 Microwave diodes.

A.5.2.1 Detector diode. A device which converts rf energy into dc or video output.

A.5.2.2 Gunn diode. A microwave diode that exhibits negative resistance arising from the bulk negative differential conductivity occurring in several compound semiconductors such as gallium arsenide, and that operates at a frequency determined by the transit time of charge bunches formed by this negative differential conductivity.

A.5.2.3 IMPATT diode (impact, avalanche and transit time diode). A semiconductor microwave diode that, when its junction is biased into avalanche, exhibits a negative resistance over a frequency range determined by the transit time of charge carriers through the depletion region.

A.5.2.4 LSA diode (limited space-charge accumulation diode). A microwave diode similar to the Gunn diode except that it achieves higher output power at frequencies, determined by the microwave cavity, that are several times greater than the transit-time frequency by avoiding the formation of charge bunches or domains.

A.5.2.5 Matched pair. A pair of diodes identical in outline dimensions and with matched electrical characteristics. The two diodes may both be forward polarity, or one forward and one reverse polarity, or both reverse polarity.

A.5.2.6 Microwave diode. A two terminal device that is responsive in the microwave region of the electromagnetic spectrum, commonly regarded as extending from 1 to 300 GHz.

A.5.2.7 Mixer diode. A microwave diode that combines rf signals at two frequencies to generate an rf signal at a third frequency.

A.5.2.8 TRAPATT diode (trapped plasma avalanche transit time diode). A microwave diode that, when its junction is biased into avalanche, exhibits a negative resistance at frequencies below the transit time frequency range of the diode due to generation and dissipation of trapped electron-hole plasma resulting from the intimate interaction between the diode and a multiresonant microwave cavity.

A.5.3 Tunnel diodes.

A.5.3.1 Tunnel diodes. A device in which quantum-mechanical tunneling leads to a region of negative slope in the forward direction of the current-voltage characteristic.

A.5.3.2 Backward diode. A device in which quantum-mechanical tunneling leads to a current-voltage characteristic with a reverse current greater than the forward current, for equal and opposite applied voltages.

A.5.4 Voltage-regulator and voltage-reference diodes.

A.5.4.1 Voltage-reference diode. A diode which is normally biased to operate in the breakdown region of its voltage-current characteristic and which develops across its terminals a reference voltage of specified accuracy, when biased to operate throughout a specified current and temperature range.

A.5.4.2 Voltage-regulator diode. A diode which is normally biased to operate in the breakdown region of its voltage-current characteristic and which develops across its terminals an essentially constant voltage throughout a specified current range.

A.5.5 Current-regulator diodes.

A.5.5.1 Current-regulator diode. A diode which limits current to an essentially constant value over a specified voltage range.

A.5.6 Varactor diodes.

A.5.6.1 Varactor diode. A two terminal semiconductor device in which use is made of the property that its capacitance varies with the applied voltage.

A.5.6.2 Tuning diode. A varactor diode used for rf tuning including functions such as automatic frequency control (AFC) and automatic fine tuning (AFT).

A.5.7 Transient voltage suppressors.

A.5.7.1 Varistor. A transient voltage suppressor that is a nonlinear resistor with symmetrical characteristics.

A.5.7.2 Avalanche-junction. A transient voltage suppressor that is a semiconductor diode that can operate in either the forward or reverse direction of its voltage-current characteristic to limit voltage transients.

A.5.7.3 Clamping voltage. The voltage in a region of low differential resistance that serves to limit the transient voltage across the device terminals.

A.5.7.4 Clamping factor. The ratio of clamping voltage to breakdown voltage.

A.5.7.5 Peak impulse current. The peak current for a series of essentially identical impulses.

A.5.7.6 Standby current. The dc current through a transient voltage suppressor at rated standoff voltage.

A.5.7.7 Repetitive peak pulse power. The peak power dissipation resulting from the peak impulse current I_{PP}.

A.5.7.8 Response time. The time interval between the point on the impulse waveform at which the amplitude exceeds the clamping voltage level and the peak of the voltage overshoot.

A.5.7.9 Voltage overshoot. The excess voltage over the clamping voltage that occurs when a current impulse having short virtual front duration is applied.

A.5.7.10 Forward surge current. The peak current for a single impulse for forward biased diode.

A.5.7.11 Working peak voltage. The peak voltage, excluding all transient voltage, usually referred to as standoff voltage.

A.6 CLASSES OF THYRISTORS

A.6.1 Thyristor. A bi-stable semiconductor device that comprises three or more junctions and can be switched between conducting and nonconducting status.

A.6.1.1 Bi-directional diode thyristor. A two terminal thyristor having substantially the same switching behavior in the first and third quadrants of the principal voltage-current characteristic.

A.6.1.2 Bi-directional triode thyristor. An n-gate or p-gate thyristor having substantially the same switching behavior in the first and third quadrants of the principal voltage-current characteristic.

A.6.1.3 N-gate thyristor. A three-terminal thyristor in which the gate terminal is connected to the n-region adjacent to the region to which the anode terminal is connected and that is normally switched to the on-state by applying a negative signal between gate and anode terminals.

A.6.1.4 P-gate thyristor. A three-terminal thyristor in which the gate terminal is connected to the p-region adjacent to the region to which the cathode terminal is connected and that is normally switched to the on-state by applying a positive signal between gate and cathode terminals.

A.6.1.5 Reverse blocking diode thyristor. A two-terminal thyristor that switches only for positive anode to cathode voltages and exhibits a reverse blocking state for negative anode to cathode voltages.

A.6.1.6 Reverse blocking triode thyristor. An n-gate or p-gate thyristor that switches only for positive anode to cathode voltages and exhibits a reverse blocking state for negative anode to cathode voltages.

A.6.1.7 Reverse conducting diode thyristor. A two terminal thyristor that switches only for positive anode to cathode voltages and conducts large currents at negative anode to cathode voltages comparable in magnitude to the on-state voltage.

A.6.1.8 Reverse conducting triode thyristor. An n-gate or p-gate thyristor that switches only for positive anode to cathode voltages and conducts large currents at negative anode to cathode voltages comparable in magnitude to the on-state voltages.

A.6.1.9 Turn off thyristor. A thyristor that can be switched between conducting and nonconducting states by applying control signals of appropriate polarities to the gate terminal, with the ratio of triggering power to triggered power appreciably less than one.

A.6.2 Physical structure terms.

A.6.2.1 Gate. An electrode connected to one of the semiconductor regions for introducing control current.

A.6.2.2 Main terminals. The two terminals through which the principal current flows.

A.6.3 Electrical characteristic and rating terms.

A.6.3.1 Anode to cathode voltage-current characteristic (anode characteristic). A function, usually represented graphically, relating the anode to cathode voltage to the principal current, with gate current where applicable, as a parameter.

A.6.3.2 Breakover point. Any point on the principal voltage-current characteristic for which the differential resistance is zero and where the principal voltage reaches a maximum value.

A.6.3.3 Negative differential resistance region. Any portion of the principal voltage-current characteristic in the switching quadrant within which the differential resistance is negative.

A.6.3.4 Off impedance. The differential impedance between the terminals through which the principal current flows when the thyristor is in the off state.

A.6.3.5 Off state. The condition of a thyristor corresponding to the high resistance low current portion of the principal voltage-current characteristic between the origin and the breakover point in the switching quadrant.

A.6.3.6 On impedance. The differential impedance between the terminals through which the principal current flows when the thyristor is in the on state.

A.6.3.7 On state. The condition of a thyristor corresponding to the low resistance, low voltage portion of the principal voltage-current characteristic in the switching quadrant.

A.6.3.8 Principal current. A generic term for the current through the device excluding gate current.

A.6.3.9 Principal voltage. The voltage between the main terminals.

A.6.3.10 Principal voltage-current characteristic (principal characteristic). A function, usually represented graphically, relating the principal voltage to the principal current, with gate current where applicable, as a parameter.

A.6.3.11 Reverse blocking impedance. The differential impedance between the two terminals through which the principal current flows when the thyristor is in the reverse blocking state at a stated operating point.

A.6.3.12 Reverse blocking state. The condition of a reverse blocking thyristor corresponding to the portion of the anode to cathode voltage-current characteristic for which the reverse currents are of lower magnitude than the reverse breakdown current.

A.6.3.13 Switching quadrant. A quadrant of the principal voltage-current characteristic in which a device is intended to switch between an off state and an on state.

A.7 OPTOELECTRONIC DEVICE DEFINITIONS

A.7.1 Optoelectronic device. A device that is responsive to or that emits or modifies electromagnetic radiation in the visible, infrared, or ultraviolet spectral regions; or a device that utilizes such electromagnetic radiation for its internal operation.

A.7.1.1 Conversion efficiency. The ratio of maximum available power output resulting from photovoltaic operation to total incident radiant flux.

A.7.1.2 Dark condition. The condition attained when the electrical parameter under consideration approaches a value which cannot be altered by further irradiation shielding.

A.7.1.3 Dark current. The current that flows through a photosensitive device in the dark condition.

A.7.1.4 Light current. The current that flows through a photosensitive device when it is exposed to radiant energy.

A.7.1.5 Photoconductive diode. A photodiode that is intended to be used as a photoconductive transducer.

A.7.1.6 Photocurrent. The difference in magnitude between light current and dark current.

A.7.1.7 Photodiode. A diode that is intended to be responsive to radiant energy.

A.7.1.8 Photodiode, avalanche. A photodiode that is intended to take advantage of avalanche multiplication of photocurrent.

A.7.1.9 Photoemitter. A device that emits electromagnetic radiation in the visible, infrared, or ultraviolet spectral regions.

A.7.1.10 Photosensitive device. A device that is responsive to electromagnetic radiation in the visible, infrared, or ultraviolet spectral regions.

A.7.1.11 Photothyristor. A thyristor that is intended to be responsive to radiant energy for controlling its operation as a thyristor.

A.7.1.12 Phototransistor. A transistor that is intended to be responsive to radiant energy.

A.7.1.13 Photovoltaic diode. A photodiode that is intended to generate a terminal voltage in response to radiant energy.

A.7.2 Photoemitting devices.

A.7.2.1 Avalanche luminescent diode. A light emitting diode that emits luminous energy when a controlled reverse current in the breakdown region is applied.

A.7.2.2 Infrared emitting diode. A diode capable of emitting radiant energy in the infrared region of the spectrum resulting from the recombination of electrons and holes.

A.7.2.3 Light emitting diode. A diode capable of emitting luminous energy resulting from the recombination of electrons and holes.

A.7.2.4 Radiant efficiency. The ratio of the total radiant flux emitted to the total input power.

A.7.3 Opto-couplers.

A.7.3.1 Photodarlington coupler. An opto-coupler in which the photo-sensitive element is a darlington connected phototransistor.

A.7.3.2 Photodiode coupler. An opto-coupler in which the photosensitive element is a photodiode.

A.7.3.3 Photothyristor coupler. An opto-coupler in which the photosensitive element is a photothyristor.

A.7.3.4 Phototransistor coupler. An opto-coupler in which the photosensitive element is a phototransistor.

A.8 ELECTRICAL AND ENVIRONMENTAL STRESS SCREENING DEFINITIONS.

A.8.1 Electrical and environmental stress screening.

a. Electrical stressing near maximum rating of semiconductor devices is performed to remove devices within a given lot which are subject to early life failures due to improper processing.

b. Determine if wear-out mechanisms are present in a given lot which will shorten the time to failure (life tests).

A.8.2 Power burn-in. A generic term describing a screening test which operates the device by internally dissipating sufficient power to significantly heat the device junction for a specified time.

A.8.2.1 Rectifying ac power burn-in. Power burn-in whereby junction heating is accomplished through the alternate application every half cycle of forward current and reverse voltage.

A.8.2.2 Steady-state dc power burn-in. Power burn-in whereby junction heating is accomplished through the application of steady-state forward current, reverse current, or forward power for diodes (including rectifiers), zeners, and transistor respectively.

A.8.3 High temperature reverse bias. A generic term describing a screening test which applies a blocking voltage and is normally performed at T_A = +150°C through the external application of heat.

A.8.3.1 Steady-state dc high temperature reverse bias. High temperature reverse bias which applies steady-state dc blocking voltage.

A.8.3.2 Half-wave high temperature reverse bias. High temperature reverse bias which applies half-wave blocking voltage.

A.8.3.3 Full-wave high temperature blocking bias. High temperature reverse bias which applies full-wave blocking voltage; sometimes applicable to symmetrical thyristors or transient voltage suppressors.

A.8.4 Operating life. A generic term describing a sample test which operates and internally heats a device junction for an extended time to verify lot integrity. This is generally an extension of power burn-in.

A.8.4.1 Rectifying ac operating life. Operating life whereby heating is accomplished through the alternate application of forward current and reverse voltage.

A.8.4.2 Steady-state dc operating life. Operating life whereby heating is accomplished through the application of steady-state forward current, reverse current, or forward power for diodes (including rectifiers), zeners, and transistors respectively.

A.8.4.3 Intermittent operating life. Operating life whereby T_J and T_C is cycled through a specified temperature range by a heating current or power and a cooling period, when current or power is removed.

A.8.4.3.1 Rectifying ac intermittent operating life. Intermittent operating life whereby the device is subjected to forward current and reverse voltage, during the heating period.

A.8.4.3.2 DC intermittent operating life. Intermittent operating life whereby the device is subjected to steady-state forward current or equivalent half sine forward current, during the heating period. This test is also known as power cycling or thermal fatigue.

A.8.5 Blocking life. A generic term describing a sample test which applies a blocking voltage and is normally performed at a specified high ambient or case temperature through the external application of heat.

A.8.5.1 Steady-state dc blocking life. Blocking life which applies steady-state dc blocking voltage.

A.8.5.2 Half-wave blocking life. Blocking life which applies half-wave blocking voltage.

A.8.5.3 Full-wave blocking life. Blocking life which applies full-wave blocking voltage.

A.8.6 Temperature cycling (air to air). Temperature cycling at device's case temperature through a specified range by the external heating and cooling of the device in an air to air environment.

A.8.7 Thermal shock (liquid to liquid). Thermal shock cycling at device's case temperature through a specified range by the external heating and cooling of the device in a liquid to liquid environment.

A.8.8 Thermal impedance. Thermal impedance for the purpose of this specification is the application of an electrical stress sufficient to pass heat through the interface of dissimilar materials, primarily to determine the quality of attachment by measuring the electrical characteristics of the temperature sensitive parameter. Thermal impedance measurement is performed by quantifying changes to the heat sensitive parameter caused by current flow and its induced heating. It is used to detect interface voids between die, attachment medium and the header or heat sink.

A.8.9 Surge. Surge is the application of a high peak current ten times (minimum) the device average current maximum rating applied for a short pulse width appropriate to determine processing defects (e.g., wire bond integrity, micro cracks, and bond voids).

APPENDIX B

ABBREVIATIONS AND SYMBOLS

B.1 SCOPE

B.1.1 Scope. This appendix covers the abbreviations and symbols for use with semiconductor devices. This appendix is not a mandatory part of this specification. The information contained herein is intended for guidance only.

B.2 APPLICABLE DOCUMENTS. This section is not applicable to this appendix.

B.3 GENERAL SEMICONDUCTOR ABBREVIATIONS AND SYMBOLS.

B.3.1 Abbreviations.

AFC	Automatic frequency control
AFT	Automatic fine tuning
BIST	Backward instability shock test
CI	Conformance inspection
ESD	Electrostatic discharge
ESDS	Electrostatic discharge sensitive
FET	Field-effect transistor
FIST	Forward instability shock test
GaAs	Gallium arsenide
HTRB	High temperature reverse bias
IGBT	Insulated gate bipolar transistor
IMPATT	Impact, avalanche, and transit time diode
LSA	Limited space-charge accumulation
MOSFETS	Metal oxide semiconductor field-effect transistors
OEM	Original equipment manufacturer
PDA	Percent defective allowed
PIN	Part or identifying number
PIND	Particle impact noise detector
PIPL	Post-irradiation parameter limits
PPM	Parts per million
QML	Qualified manufacturers list
RHA	Radiation hardness assurance
RHAPM	Radiation hardness assurance part managers
RMS	Root means square
SEM	Scanning electron microscope
SOA	Safe operating area
SPC	Statistical process control
TP	True position

TRAPATT	Trapped plasma avalanche transit time diode	
UHF	Ultra high frequency	

B.3.2 Symbols.

		Old symbol
F	Spot noise figure	(NF)
F	Average noise figure	
R_{θ}	Thermal resistance	(θ)
$R_{\theta CA}$	Thermal resistance, case to ambient	
$R_{\theta JA}$	Thermal resistance, junction to ambient	(θ_{J-A})
$R_{\theta JC}$	Thermal resistance, junction to case	(θ_{J-C})
$R_{\theta JL}$	Thermal resistance, junction to lead	
$R_{\theta JR}$	Thermal resistance, junction to reference	
T_A	Ambient or free air temperature	
T_C	Case temperature	
TEC	End cap temperature	
T_J	Junction temperature	
TL	Lead temperature	
T_{op}	Operating temperature	
T_{STG}	Storage temperature	
t_d	Delay time	
t_f	Fall time	
t_{off}	Turn off time	
t_{on}	Turn on time	
t_p	Pulse time	
t_r	Rise time	
t_s	Storage time	
t_w	Pulse average time	
$V_{(BR)}$	Breakdown voltage	(BV)

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B.4 TRANSISTORS SYMBOLS

B.4.1 Junction transistors, multijunction type symbols.

C_{ibo}, C_{ieo}	Input capacitance, (common base, common emitter) collector open circuited for ac
C_{ibs}, C_{ies}	Input capacitance, (common base, common emitter) collector short-circuited to reference terminal for ac
C_{obo}, C_{oeo}	Output capacitance, (common base, common emitter) input open circuited to ac
C_{obs}, C_{oes}	Output capacitance, (common base, common emitter) input short-circuited to reference terminal for ac
f_{hfb}, f_{hfc}, f_{hfe}	Small signal, short-circuit forward current transfer ratio cutoff frequency (common base, common collector, common emitter)
f_{max}	Maximum frequency of oscillation
f_T	Extrapolated unity gain frequency
g_{MB}, g_{MC}, g_{ME}	Static transconductance (common base, common collector, common emitter)
g_{mb}, g_{mc}, g_{me}	Small signal transconductance (common base, common collector, common emitter)
G_{PB}, G_{PC}, G_{PE}	Large signal insertion power gain (common base, common collector, common emitter)
G_{pb}, G_{pc}, G_{pe}	Small signal insertion power gain (common base, common collector, common emitter)
h_{FB}, h_{FC}, h_{FE}	Static forward current transfer ratio (common base, common collector, common emitter)
h_{fb}, h_{fc}, h_{fe}	Small signal short circuit forward current transfer ratio (common base, common collector, common emitter)
$\lvert h_{fe} \rvert$	Magnitude of common emitter small signal short circuit forward current transfer ratio
h_{IB}, h_{IC}, h_{IE}	Static input resistance (common base, common collector, common emitter)
h_{ib}, h_{ic}, h_{ie}	Small signal short circuit input impedance (common base, common collector, common emitter)
h_{ob}, h_{oc}, h_{oe}	Small signal open circuit output admittance (common base, common collector, common emitter)
h_{rb}, h_{rc}, h_{re}	Small signal open circuit reverse voltage transfer ratio (common base, common collector, common emitter)
I_B	Base current (dc)
I_C	Collector current (dc)
I_E	Emitter current (dc)
i_B	Base current (instantaneous total value)
i_C	Collector current (instantaneous total value)
i_E	Emitter current (instantaneous total value)
I_{CBO}	Collector cutoff current (dc) emitter open

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I_{CEO}	Collector cutoff current (dc) base open
I_{CER}	Collector cutoff current (dc) with specified resistance between base and emitter
I_{CES}	Collector cutoff current (dc) base short circuited to emitter
I_{CEV}	Collector cutoff current (dc) with specified voltage between base and emitter
I_{CEX}	Collector cutoff current (dc) with specified circuit between base and emitter
I_{EBO}	Emitter cutoff current (dc) collector open
I_{ECS}	Emitter cutoff current (dc) base short-circuited to collector
I_S	Collector efficiency
P_C	Collector power dissipation
P_T	Total power dissipation, all terminals
R_B	External base resistance
r_b	Base spreading resistance
rb'cc	Collector-base time constant
R_C	External collector resistance
$r_{CE(sat)}$	Collector to emitter saturation resistance
R_E	External emitter resistance
r_{iep}	Small signal short circuit parallel input resistance (common emitter)
t_c	t_{OFF} crossover time (the time interval during which the collector voltage decreases from 10 percent of its peak off-state value and the collector current decreases to 10 percent of its peak on state value)
V_{BB}	Base supply voltage
V_{BE}	Base to emitter voltage (dc)
$V_{BE(sat)}$	Base to emitter saturation voltage
$V_{(BR)CBO}$	Breakdown voltage collector to base, emitter open
$V_{(BR)CEO}$	Breakdown voltage collector to emitter, base open
$V_{(BR)CER}$	Breakdown voltage collector to emitter, with specified resistance between base and emitter
$V_{(BR)CES}$	Breakdown voltage collector to emitter, with base short-circuited to emitter
$V_{(BR)CEX}$	Breakdown voltage collector to emitter, with specified circuit between base and emitter
$V_{(BR)EBO}$	Breakdown voltage emitter to base, collector open
V_{CB}	Collector to base voltage (dc)
V_{CBF}	DC open circuit voltage (floating potential) between the collector and base, with the emitter biased in the reverse direction with respect to the base
V_{CBO}	Collector to base voltage (static), emitter open
V_{CC}	Collector supply voltage

V_{CE} ..... Collector to emitter voltage (dc)

V_{ce} ..... Collector to emitter voltage (rms)

v_{ce} ..... Collector to emitter voltage (instantaneous)

$V_{CE}(sat)$ ..... Collector to emitter saturation voltage

V_{CEO} ..... Collector to emitter voltage (static) base open

$V_{CEO(sus)}$ ..... Breakdown voltage, collector to emitter, sustained

V_{CER} ..... Collector to emitter voltage (dc), with specified resistance between base and emitter

V_{CES} ..... Collector to emitter voltage (dc), base short-circuited to emitter

V_{EB} ..... Emitter to base voltage (dc)

V_{eb} ..... Emitter to base voltage (rms)

v_{eb} ..... Emitter to base voltage (instantaneous)

V_{EBF} ..... DC open circuit voltage (floating potential) between the emitter and base, with the collector biased in the reverse direction with respect to the base

$V_{(BR)CEV}$ ..... Breakdown voltage collector to emitter, with specified voltage between base and emitter

V_{EBO} ..... Emitter to base voltage (static) collector open

V_{EC} ..... Emitter to collector voltage (dc)

V_{ECF} ..... DC open circuit voltage (floating potential) between the emitter and collector, with the base biased in the reverse direction with respect to the collector

V_{EE} ..... Emitter supply voltage

V_{RT} ..... Reach through voltage

B.4.2 FET symbols.

b_{is} ..... Small-signal, common-source, short-circuit, input susceptance

b_{os} ..... Small-signal, common-source, short-circuit, output susceptance

b_{fs} ..... Small-signal, common-source, short-circuit, forward transfer susceptance

b_{rs} ..... Small-signal, common-source, short-circuit, reverse transfer susceptance

C_{ds} ..... Small-signal drain to source capacitance

C_{du} ..... Small-signal drain to substrate capacitance

C_{iss} ..... Small-signal, common-source, short-circuit, input capacitance

C_{oss} ..... Small-signal, common-source, short-circuit, output capacitance

C_{rss} ..... Small-signal, common-source, short-circuit, reverse transfer capacitance

D, d ..... Drain terminal

E_{AR} ..... Repetitive avalanche energy capability

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E_{AS} ..... Single pulse avalanche energy capability

G, g ..... Gate terminal

g_{fs} ..... Small-signal, common-source, short-circuit, forward transfer conductance

g_{is} ..... Small-signal, common-source, short-circuit, input conductance

g_{os} ..... Small-signal, common-source, short-circuit, output conductance

G_{pg} ..... Small-signal, common-gate insertion power gain

G_{ps} ..... Small-signal, common-source insertion power gain

g_{rs} ..... Small-signal, common-source, short-circuit, reverse transfer conductance

G_{tg} ..... Small-signal, common-gate, transducer power gain

G_{ts} ..... Small-signal, common-source transducer power gain

I_D ..... Drain current

I_{AR} ..... Rated avalanche current (repetitive and nonrepetitive)

$I_{D(on)}$ ..... On-state drain current

$I_{D(off)}$ ..... Drain cutoff current

I_{DSS} ..... Zero-gate-voltage drain current

I_G ..... Gate current

I_{GF} ..... Forward gate current

I_{GR} ..... Reverse gate current

I_{GSS} ..... Reverse gate current with all other terminals short-circuited to source (junction-gate)

I_{GSSF} ..... Forward gate current with all other terminals short-circuited to source (insulated-gate)

I_{GSSR} ..... Reverse gate current with all other terminals short-circuited to source (insulated-gate)

I_S ..... Source current through drain diode (forward biased V_{SD})

$I_{S(off)}$ ..... Source cutoff current

I_{SDS} ..... Zero-gate-voltage source current

$I_{(ISO)}$ ..... Source pin to case isolation current

$Q_{g(th)}$ ..... Gate charge that must be supplied to reach minimum specified gate-source threshold voltage

$Q_{g(on)}$ ..... Gate charge that must be supplied to reach the gate-source voltage specified for the device $r_{DS(on)}$ measurement

$Q_{gm(on)}$ ..... Gate charge that must be supplied to the device to reach the maximum rated gate-source voltage

Q_{gs} ..... Charge required by C_{GS} to reach a specified I_D

Q_{gd} ..... Charge supplied to the drain from the gate to change the drain voltage under constant drain current conditions

$r_{ds(on)}$ ..... Small-signal, drain to source on-state resistance

$r_{DS(on)}$ ..... Static drain to source on-state resistance

S, s ..... Source terminal

$t_{d(off)}$ ..... Turn-off delay time

$t_{d(on)}$ ..... Turn-on delay time

U, u ..... Substrate (bulk) (terminal, when substrate is externally terminated)

$V_{(BR)GSS}$ ..... Gate to source breakdown voltage, all other terminals short-circuited to source (junction-gate)

$V_{(BR)DSS}$ ..... Drain to source breakdown voltage, all other terminals short-circuited to source (junction-gate)

$V_{(BR)GSSF}$ ..... Forward gate to source breakdown voltage

$V_{(BR)GSSR}$ ..... Reverse gate to source breakdown voltage

V_{DD} ..... Drain supply voltage

V_{DG} ..... Drain to gate voltage

V_{DS} ..... Drain to source voltage

$V_{DS(on)}$ ..... On-state drain to source voltage

V_{DU} ..... Drain to substrate voltage

V_{GG} ..... Gate supply voltage

V_{GP} ..... Gate plateau voltage

V_{GS} ..... Gate to source voltage

V_{GSF} ..... Forward gate to source voltage

V_{GSR} ..... Reverse gate to source voltage

$V_{GS(off)}$ ..... Gate to source cutoff voltage

$V_{GS(th)}$ ..... Gate to source threshold voltage

V_{GU} ..... Gate to substrate voltage

V_{ISO} ..... Source pin to case isolation voltage

V_{SS} ..... Source supply voltage

V_{SU} ..... Source to substrate voltage

y_{fs} ..... Magnitude of small-signal common-source short-circuit forward transfer admittance

y_{is} ..... Magnitude of small-signal common-source short-circuit input admittance

y_{rs} ..... Magnitude of small-signal common-source short-circuit reverse transfer admittance

B.4.3 Unijunction transistor symbols.

$I_{B2(mod)}$ ..... Interbase modulated current

I_{EB20} ..... Emitter reverse current

I_P ..... Peak point current

I_v ..... Valley point current

r_{BB} ..... Interbase resistance

V_{B2B1} ..... Interbase voltage

$V_{EB1(sat)}$ ..... Emitter saturation voltage

V_{OB1} ..... Base - 1 peak voltage

V_p ..... Peak point voltage

V_v ..... Valley point voltage

η ..... Intrinsic standoff ratio

B.5 DIODES AND RECTIFIERS SYMBOLS

B.5.1 Diodes and rectifier symbols.

C_J ..... Junction capacitance

$I_{F(RMS)}$, I_f, I_F, $I_{F(AV)}$, i_F, I_{FM} ..... Forward current

I_{FSM} ..... Forward current, surge peak

$I_{F(OV)}$ ..... Forward current, overload

I_O ..... Average forward current, 180° conduction angle, 60 Hz, half sine wave

$I_{R(RMS)}$, I_r, I_R, $I_{R(AV)}$, i_R, I_{RM} ..... Reverse current

$i_{R(REC)}$, $I_{RM(REC)}$ ..... Reverse recovery current

I_{RRM} ..... Reverse current, repetitive peak

I_{RSM} ..... Reverse current, surge peak

P_F, $P_{F(AV)}$, P_F, P_{FM} ..... Forward power dissipation

P_R, $P_{R(AV)}$, P_R, P_{RM} ..... Reverse power dissipation

Q_S ..... Stored charge

t_{fr} ..... Forward recovery time

t_{rr} ..... Reverse recovery time

$V_{(BR)}$, $v_{(BR)}$ ..... Breakdown voltage (dc, instantaneous total value)

$V_{F(RMS)}$, V_f, V_F, $V_{F(AV)}$, v_F, V_{FM} ..... Forward voltage

$V_{R(RMS)}$, V_r, V_R, $V_{r(AV)}$, v_R, V_{RM} ..... Reverse voltage

V_{RWM} ..... Working peak reverse voltage

V_{RRM} ..... Repetitive peak reverse voltage

V_{RSM} ..... Nonrepetitive peak reverse voltage

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B.5.1.1 Letter symbol table (diodes and rectifiers).

	Total RMS value	RMS value of alternating component	DC value no alternating component	DC value with alternating component	Instantaneous total value	Maximum (peak) total value
Forward current	$I_{F(RMS)}$	I_F	I_F	$I_{F(AV)}$	I_F	I_{FM}
Forward current average, 180°C conduction angle 60 Hz, half sine wave				I_O		
Forward current repetitive peak						I_{FRM}
Forward current, surge peak						I_{FSM}
Forward current, overload						$I_{F(OV)}$
Reverse current	$I_{R(RMS)}$	I_F	I_R	$I_{R(AV)}$	i_R	I_{RM}
Reverse recovery current					$i_{R(REC)}$	$I_{RM(REC)}$
Forward power dissipation			P_F	$P_{F(A)}$	P_F	P_{FM}
Reverse power dissipation			P_R	$P_{R(A)}$	P_R	P_{RM}
Forward voltage	$V_{F(RMS)}$	V_f	V_F	$V_{F(A)}$	V_F	V_{FM}
Reverse voltage	$V_{R(RMS)}$	V_r	V_R	$V_{R(A)}$	V_R	R_{RM}
Reverse voltage working peak						V_{RWM}
Reverse voltage repetitive peak						V_{RRM}
Reverse voltage nonrepetitive peak						V_{RRM}
Breakdown voltage			$V_{(BR)}$		$V_{(BR)}$	

B.5.2 Microwave diode symbols.

$\overline{F}_o$	Overall average noise figure (of a mixer diode)
$\overline{F}_{os}$	Standard overall average noise figure (of a mixer diode)
L_c	Conversion loss
M	Figure of merit (of a detector diode)
N_r	Output noise ratio
TSS	Tangential signal sensitivity
VSWR	Voltage standing wave ratio
z_{if}	Impedance, intermediate-frequency
z_{rf}	Impedance, radio-frequency
z_m	Impedance, modulator-frequency load
z_v	Video impedance

B.5.3 Tunnel diodes and backward diode symbols.

I_I	Inflection point current
I_P	Peak point current
I_V	Valley point current
r_i	Dynamic resistance at inflection point
V_{PP}	Projected peak point voltage
V_I	Inflection point voltage
V_P	Peak point voltage
V_V	Valley point voltage

B.5.4 Voltage regulator and voltage-reference diode symbols.

I_F	Forward current, dc
I_R	Reverse current, dc
I_Z, I_{ZK}, I_{ZM}, I_{ZSM}	Regulator current, reference current (dc, dc near breakdown knee, dc maximum rated current, dc maximum rated surge current)
V_F	Forward voltage, dc
V_R	Reverse voltage, dc
V_Z, V_{ZM}	Regulator voltage, reference voltage (dc, dc at maximum rated current)
z_z, z_{zk}, z_{zm}	Regulator impedance, reference impedance (small-signal, at I_Z, at I_{ZK}, at I_{ZM})
α_{VZ}	Temperature coefficient of regulator voltage, temperature coefficient of reference voltage

B.5.5 Current regulator diode symbols.

I_L ..... Limiting current

I_p ..... Regulator current

V_K ..... Knee voltage

V_L ..... Limiting voltage

ΔI_P ..... Regulator current variation

V_S ..... Regulator voltage

z_k ..... Knee impedance

z_s ..... Regulator impedance

α_{Ip} ..... Temperature coefficient of regulator current

B.5.6 Varactor diode symbols.

C_c ..... Case capacitance

C_j ..... Junction capacitance

C_t ..... Total capacitance

$\frac{C_{t1}}{C_{t2}}$ ..... Capacitance ratio

f_{co} ..... Cut-off frequency

L_s ..... Series inductance

Q ..... Figure of merit

r_s ..... Series resistance, small-signal

α_C ..... Temperature coefficient of capacitance

η ..... Efficiency

B.5.7 Transient voltage suppressor symbols.

CF ..... Clamping factor

I_D ..... Standby current

I_{FS} ..... Forward surge current

I_{FSM} ..... Rated forward surge current

I_{PP} ..... Peak impulse current

I_{PPM} ..... Rated peak impulse current

I_S ..... Surge peak transient current

I_{SM} ..... Rated surge peak transient current

$P_{(A)}$ ..... Average power dissipation

$P_{M(A)}$ ..... Rated average power dissipation

P_{PP} ..... Repetitive peak pulse power dissipation

P_{PPM} ..... Rated repetitive peak pulse power dissipation

t_{os} ..... Overshoot duration

t_{res} ..... Response time

$V_{(BR)}$ ..... Breakdown voltage

V_C ..... Clamping voltage

W_W ..... Working peak voltage, also standoff voltage

$W_{WM(RMS)}$ ..... Working rms voltage

V_{WM} ..... Rated working peak voltage

V_{CS} ..... Voltage overshoot

$\alpha V_{(BR)}$ ..... Temperature coefficient of breakdown voltage

B.6 THYRISTORS SYMBOLS

B.6.1 Thyristor symbols.

dv/dt ..... Critical rate of rise of off-state voltage

$I_{(BO)}$, $i_{(BO)}$ ..... Breakover current

$I_{(BR)}$, $i_{(BR)}$ ..... Reverse breakdown current (of a reverse-blocking thyristor)

$I_{D(RMS)}$, I_D, $I_{D(A)}$, i_D, I_{DM} ..... Off-state current

I_{DRM} ..... Repetitive peak off-state current

I_G, $I_{G(A)}$, i_G, I_{GM} ..... Gate current

I_{GD}, i_{GD}, I_{GDM} ..... Gate nontrigger current

I_{GQ}, i_{GQ}, I_{GQM} ..... Gate turn-off current (of a turn-off thyristor)

I_{GT}, i_{GT}, I_{GTM} ..... Gate trigger current

I_H, i_H ..... Holding current

I_L, i_L ..... Latching current

$I_{R(RSM)}$, I_R, $I_{R(A)}$, i_R, I_{RM} ..... Reverse current (of a reverse-blocking or reverse-conducting thyristor)

I_{RRM} ..... Repetitive peak reverse current (of a reverse-blocking thyristor)

I_{RSM} ..... Nonrepetitive peak reverse current (of a reverse-blocking thyristor)

$I_{T(RMS)}$, I_T, $I_{T(A)}$, i_T, I_{TM} ..... On-state current

I_{TRM} ..... Repetitive peak on-state current

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I_{TSM} ..... Nonrepetitive peak on-state current

P_G, $P_{G(A)}$, P_G, P_{GM} ..... Gate power dissipation

P_R, $P_{R(A)}$, P_R, P_{RM} ..... Reverse power dissipation

t_{gd} ..... Gate-controlled delay time

t_{gq} ..... Gate-controlled turn-off time (of a turn-off thyristor)

t_{gt} ..... Gate-controlled turn-on time

t_q ..... Circuit-commutated turn-off time

$V_{(BO)}$, $v_{(BO)}$ ..... Breakover voltage

$V_{(BR)}$, $v_{(BR)}$ ..... Reverse breakdown voltage (of a reverse-blocking thyristor)

$V_{D(RMS)}$, V_D, $V_{D(A)}$, v_D, V_{DM} ..... Off-state voltage

V_{DRM} ..... Repetitive peak off-state voltage

V_{DSM} ..... Nonrepetitive peak off-state voltage

V_{DWM} ..... Working peak off-state voltage

V_G, $V_{G(A)}$, v_G, V_{GM} ..... Gate voltage

V_{GD}, v_{GD}, V_{GDM} ..... Gate nontrigger voltage

V_{GQ}, v_{GQ}, V_{GQM} ..... Gate turn-off voltage (of a turn-off thyristor)

V_{GT}, v_{GT}, V_{GTM} ..... Gate trigger voltage (of a reverse-blocking thyristor

V_{RRM} ..... Repetitive peak reverse voltage (of a reverse-blocking thyristor)

V_{RSM} ..... Nonrepetitive peak reverse voltage (of a reverse-blocking thyristor)

V_{RWM} ..... Working peak reverse voltage (of a reverse-blocking thyristor)

$V_{T(RMS)}$, V_T, $V_{T(A)}$, v_T, V_{TM} ..... On-state voltage

$V_{T(MIN)}$ ..... Minimum on-state voltage

B.6.1.1 Letter symbol table (thyristors).

	Total RMS value	DC value no alternating component	DC value with alternating component	Instantaneous total value	Maximum (peak) total value
On-state current	$I_{T(RMS)}$	I_T	$I_{T(A)}$	i_T	I_{TM}
Repetitive peak, on-state current					I_{TRM}
Surge (nonrepetitive) on-state current				I_{TSM}	
Overload on-state current					$I_{T(OV)}$
Breakover current		$I_{(BO)}$		$i_{(BO)}$	
Off-state current	$I_{D(RMS)}$	I_D	$I_{D(A)}$	i_D	I_{DM}
Repetitive peak, off-state current					I_{DRM}
Reverse current	$I_{R(RMS)}$	I_R	$I_{R(A)}$	i_R	I_{RM}
Repetitive peak, reverse current					I_{RRM}
Reverse breakdown current		$I_{(BR)R}$		$i_{(BR)R}$	
On-state voltage	$V_{T(RMS)}$	V_T	$V_{T(A)}$	v_T	V_{TM}
Breakover voltage		$V_{(BO)}$		$v_{(BO)}$	
Off-state voltage	$V_{D(RMS)}$	V_D	$V_{D(A)}$	v_D	V_{DM}
Minimum on-state voltage		$V_{T(MIN)}$			
Working peak, off-state voltage					V_{DWM}
Repetitive peak off-state voltage					V_{DRM}

B.6.1.1 Letter symbol table (thyristors) - Continued.

	Total RMS value	DC value no alternating component	DC value with alternating component	Instantaneous total value	Maximum (peak) total value
Nonrepetitive off-state voltage					V_{DSM}
Reverse voltage	$V_{R(RMS)}$	V_R	$V_{R(A)}$	v_R	V_{RM}
Working peak reverse voltage					V_{RWM}
Repetitive peak, reverse voltage					V_{RRM}
Nonrepetitive peak, reverse voltage					V_{RSM}
Reverse breakdown voltage		$V_{(BR)R}$		$v_{(BR)R}$	
Holding current		I_H		i_H	
Latching current		I_L		i_L	
Gate current		I_G	$I_{G(A)}$	i_G	I_{GM}
Gate trigger current		I_{GT}		i_{GT}	I_{GTM}
Gate nontrigger current		I_{GD}		i_{GD}	I_{GDM}
Gate turn-off current		I_{GQ}		i_{GQ}	I_{GQM}
Gate voltage		V_G	$V_{G(A)}$	v_G	V_{GM}
Gate trigger voltage		V_{GT}		v_{GT}	V_{GTM}
Gate nontrigger current		V_{GD}		v_{GD}	V_{GDM}
Gate turn-off voltage		V_{GQ}		v_{GQ}	V_{GQM}
Gate power dissipation		P_G	$P_{G(A)}$	P_G	P_{GM}

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B.7 OPTOELECTRONIC DEVICES SYMBOLS

B.7.1 Optoelectronic device symbols.

Q, (Q_e)	Radiant energy
Q, (Q_v)	Luminous energy
t_d	Delay time
t_f	Fall time
t_{off}	Turn-off time
t_{on}	Turn-on time
t_r	Rise time
t_s	Storage time
τ	Time constant
ϕ	Luminous flux, radiant flux

B.7.2 Photosensitive device symbols.

A_D	Area, detector
E	Illuminance (illumination); irradiance
f_{mod}	Modulation frequency
I_n	Detector noise
I_S, I_s	Detector signal current (dc; rms value of ac component)
P_n	Noise equivalent power
V_n	Detector noise voltage
V_S, V_s	Detector signal voltage (dc; rms value of ac component)
μf	Noise equivalent bandwidth

B.7.3 Photoemitting device symbols.

I	Luminous intensity; radiant intensity
L	Luminance; radiance
t_f	Radiant-pulse fall time
t_r	Radiant-pulse rise time
w	Luminous density; radiant density
$\Delta\lambda$	Spectral bandwidth
λ_p	Peak wavelength

B.7.4 Optocoupler (photocoupler and opto-isolator) symbols.

C_{io} .....Input-to-output internal capacitance; transcapacitance

h_F .....Current transfer ratio

I_{IO}.....DC input-to-output current; isolation current

r_{IO} .....Isolation resistance

V_{IO} .....DC input-to-output voltage; isolation voltage

APPENDIX C

QUALITY MANAGEMENT PROGRAM

C.1 SCOPE

C.1.1 Scope. This appendix outlines a Quality Management Program and has been prepared to allow manufacturers to produce high quality, reliable military discrete semiconductors under one quality system utilizing best commercial practices. However, manufacturers who choose to participate must implement a Technical Review Board (TRB), and conduct product quality planning. Manufacturers with a certified Quality Management Program will be approved by the qualifying activity to make decisions normally reserved for the qualifying activity. This level gives unique flexibility to applicable suppliers. A Qualified Manufacturer is compliant to this appendix. A Qualified Manufacturer is a supplier who exercises a system which focuses on the manufacturing process and technology capability. The DSCC audit is process oriented. This appendix is a mandatory part of this specification. The information contained herein is intended for compliance only.

C.2 APPLICABLE DOCUMENTS

C.2.1 General. The documents listed in this section are specified in sections C.3, C.4 and C.8 of this appendix. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements found in documents cited in this appendix, whether or not the documents are listed.

C.2.2 Government documents.

C.2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation (see 6.2).

HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-5961 - List of Standard Semiconductor Devices.

(Unless otherwise indicated, copies of the above specifications, standards, and handbooks are available from the Defense Automated Printing Service, Bldg 4D (DPM-DODSSP), 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

C.2.2.2 Non-Government standards and other publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents which are DoD adopted are those listed in the issue of the DODISS cited in the solicitation. Unless otherwise specified, the issues of documents not listed in the DODISS are the issues of the documents cited in the solicitation (see 6.2).

ELECTRONIC INDUSTRIES ALLIANCE (EIA)

EIA-557	Statistical Process Control Systems.
JEP-121	Guidelines for MIL-STD-883 Screening and QCI Optimization.

(Application for copies should be addressed to the Electronic Industries Alliance, 2500 Wilson Boulevard, Arlington VA 22201-3834.)

(Non-Government standards and other publications are normally available from the organizations which prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

C.2.3 Order of precedence. In the event of a conflict between the text of this appendix and the references cited herein (except for related performance specification sheets), the text of this appendix takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

C.3 Quality Management (QM) program. A quality management program that embodies the principles of Total Quality Management (TQM) will be developed and implemented by the manufacturer and documented in the QM plan. This is a management approach that is applied over the life cycle of the product to provide visibility and control of the functional and physical characteristics of devices marked with the JAN designator.

C.3.1 QM plan. The QM plan documents the Quality Management (QM) Program and consists of the following 3 major elements: The quality manual, in accordance with the quality system specified in appendix D; the TRB information (see C.4); and Product quality planning information (see C.5). Product quality planning is expected to be comprised of individual groups of documents that are specific to the technology being offered. Each technology that is offered will have its own product quality planning information. The QM plan, itself, may be an index of references to other documents which include the information required. In addition to these 3 major elements, the QM plan will include as a minimum:

C.3.1.1 Quality improvement plan. The quality improvement plan documents are the specific procedures to be followed by the manufacturer to assure continuous improvement (defined by C.8.5) in quality, and reliability of the process and the product being produced.

C.3.1.2 Failure analysis. This establishes the procedures that a manufacturer self-imposes to test and analyze a sufficient quantity of failed parts to determine each failure category from all stages of manufacturing and the field. This should also identify corrective actions or specify the use of a corrective action plan based on the findings of the failure analysis

C.3.1.3 SPC plan. A specific plan defining the manufacturer's SPC program within the manufacturing process to the requirements of EIA-557-A.

C.3.1.4 Certification and qualification plan. The certification and qualification plan will be defined (see C.4 and C.8).

C.3.1.5 Conversion/review of customer requirements. A procedure for reviewing customer’s requirements, as expressed in specifications and purchase orders to determine if the device will meet expectations. This includes determining if certification and QML coverage does not exist, and it may include converting the customer's requirements into in-house requirements. This procedure should be documented (in addition to D.3.3).

C.4 Technical Review Board (TRB) responsibilities. The manufacturer defines its own TRB structure. The purpose of the TRB is to assess the impact of proposed product/process changes for reliability and form, fit and function. The TRB is responsible for product quality planning, covered by the QM program for the introduction of new products and maintains the QML lines. Written procedures which will govern the operation of the TRB shall be maintained and updated regularly.

C.4.1 Organizational structure. The manufacturer’s TRB will ensure communication is established and maintained among representatives from device design, technology development, wafer fabrication, assembly, test, production and quality assurance. The TRB is intended to be a cross-functional technical group. The manufacturer will submit the name(s) and telephone numbers of their TRB contact person(s) to the qualifying activity. The members of the TRB shall have the responsibility and authority to make decisions and the resources to implement these decisions. Records of the TRB deliberations and decisions will be maintained and made available to the qualifying activity.

C.4.2 TRB duties. The TRB duties are defined as follows:

a. The TRB will keep the qualifying activity updated on the status of QML technologies and products.

b. The TRB will have a methodology in place for assessing and monitoring the quality and reliability of its products.

c. The TRB shall set measurable quality objectives and monitor their progress towards meeting those objectives.

d. The TRB is responsible for control of all technology families.

e. The technology families will be defined by the TRB.

f. A manufacturer can have more than one TRB if appropriate.

g. The TRB controls all aspects of product design changes, material changes and process changes.

h. The TRB will approve all process flow charts, failure mode effects analysis (FMEA) and Control Plans for each individual process. The TRB determines what test or verifications are needed to prove out proposed design and construction changes (See table IV of appendix E).

i. The TRB decides what devices (i.e., worst case) shall be used to qualify a new technology family.

j. The TRB will also address the impact of key personnel changes on the QML system.

k. The TRB shall maintain records and make them available for qualifying activity review.

l. The TRB is required to report periodically to the qualifying activity on the status of the QML technology and products (see C.4.5).

C.4.3 TRB input The TRB must be provided input in order to monitor the quality of products. Examples of needed input are; self-audit results, SPC data, production yields, customer returns and corrective/preventive action initiatives. Other TRB responsibilities include but are not limited to:

a. Quality improvement initiatives (see C.8.4).

b. Reliability program results (see C.8.1.1, C.8.1.2, and C.8.4.1).

c. Qualification test data and process validation review.

d. Design and process change test data review (see C.7).

e. Reviewing results of failure analysis.

f. Monitor performance of any contract services.

g. Monitor customer returns and complaints.

C.4.4 TRB authority. After the manufacturers QM program has been certified by the qualifying activity, the manufacturer's TRB will have the authority to review and approve the following without prior approval of the qualifying activity:

a. Laboratory suitability for new test methods.

b. Qualification and design change test plans.

c. Qualification, design, and construction test data.

d. Ship ahead of group B or C completion.

In addition, when errors and omissions are identified in a performance specification sheet the manufacturer's TRB may make the appropriate corrections provided the qualifying activity and preparing activity are notified prior to imlementation.

C.4.5 TRB status reporting. The manufacturers TRB will submit a status report to the qualifying activity describing the health of the QML technology families including all changes and the criticality of the changes with respect to quality, reliability, performance, and interchangeability. This report will be submitted semi-annually unless modified by the qualifying activity. Supporting test data shall be retained by the manufacturer where applicable. The following areas shall be addressed in each report as a minimum:

a. TRB meeting minutes and decisions.

b. Production summaries on all QML products.

c. Customer returns and corrective actions.

d. Changes, additions, and improvements in design, fabrication, assembly, or test process.

e. Changes to the facility and new process equipment.

f. Qualification planning (proposed new qualifications).

g. How well the TRB is doing at meeting their quality objectives.

h. Changes to FMEAs and control plans.

i. Ship ahead of group B or C completion.

j. Laboratory suitability approvals.

k. Product qualifications.

l. New or revised 36 D form.

m. Contracted services.

C.5 Product quality planning. Quality planning is a controlled method of assuring that a product meets the customers performance needs. This is accomplished through characterization of all applicable technology families and associated processes. In addition to the requirements of appendix D.3.2.4, formal technology process flowcharts, FMEA's and Control Plans shall be generated and maintained under the manufacturers' document control system.

C.5.1 Technology process flowchart. Flow charts must be generated for each certified technology. The flow chart consists of a diagram showing the sequence of material processing from incoming material through final shipment, including any production testing.

C.5.2 FMEA. The TRB is responsible for assuring that all actions recommended have been implemented or adequately addressed in the FMEA's.

C.5.3 Control plans. The control plan is prepared to summarize the process control planning for each technology. Product characteristics that should be included in a control plan are control item characteristics and significant characteristics. The evaluation method, sampling plans, data analysis method and out of control plans are part of the Control Plan. Control Plan updating should be tied to the corresponding FMEA updates.

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C.6 QM program certification process. The effectiveness of the manufacturers QM program can only be determined over time. Manufacturers must have a working TRB in place prior to requesting a Quality Management Program Certification audit. A comprehensive self-audit must be performed by the manufacturer after a sufficient implementation period to get a realistic snapshot of the QM program and TRB effectiveness. All correspondence sent to the qualifying activity must be first reviewed by the TRB. Results of such reviews are required for qualification reports and design changes. These reviews will be used in part to gauge the effectiveness of the TRB. Quality Management program certification audits will not be scheduled until the manufacturer has submitted all pre-audit information and has demonstrated a working and effective TRB. The following items are examples of pre-audit submission:

a. Quality planning information.

b. Manufacturers QM plan (see C.3.1).

c. Quality policy.

d. TRB procedure (see C.4) and meeting minutes.

e. List of methods for lab suitability.

f. Self-audit results.

g. Appropriate documents to demonstrate compliance to MIL-PRF-19500 requirements.

The qualifying activity will review the pre-audit submissions for compliance to MIL-PRF-19500. Any initial concerns will be addressed at this time. Additional information, such as detailed procedures may be requested. The audit will be scheduled once all the pre-audit information is approved. The validation will focus on the TRB, QM plan, and process controls for each technology family. Once corrective actions have been taken and approved by the qualifying activity, certification will be issued.

C.7 Design, construction and process change control procedures. Any changes to the manufacturers certified process flow or design and construction are to be governed by the manufacturer's TRB. All changes should be documented as to the reason of the change with supporting data taken to justify the change, as appropriate. All changes must be classified by the TRB as major or minor. For any change that merits consideration for requalification, the TRB will decide if requalification is needed. The effect on any test optimization must be evaluated prior to the implementation of a design change. Notification of major changes should be made concurrently to the qualifying activity until further notice from the qualifying activity.

C.7.1 Change notification. Any changes that will affect the design and construction information are considered major changes. The qualifying activity must be provided the latest design and construction information to keep DSCC files current.

C.7.2 Design and process methodology change. Changes in the design and process methodology to be evaluated by the TRB will include, but not limited to, changes in the following areas:

a. Technology flow chart (see C.5.1).

b. FMEA (see C.5.2).

c. Control plan (C.5.3).

d. Bill of materials.

e. Any changes that affect form, fit, or function.

C.8 QML processing. The QML manufacturer is expected to use the following items within each technology family.

a. Design qualification.

b. Process optimization.

c. Process validation.

d. Continuous improvement.

e. Qualification.

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C.8.1 Design qualification. The qualification activity will commence as soon as a "design freeze" is agreed upon that can meet the targeted performance criteria and the product target specification (mechanical/electrical/reliability/thermal). Prior to the start of the Product Design Qualification (PDQ), a meeting will be called by the TRB to determine the tests that need to be performed. The general principle of testing product, under worst case conditions, in accordance with the target specification, should be adhered to, to determine product capability at published operating levels.

C.8.1.1 General elements of a design qualification program. A design qualification program is a qualification of the design and the manufacturing process, more commonly referred to as Product Design Qualification (PDQ). These tests are usually performed as part of the quality design process for determining the long-term reliability of the design and the manufacturing process. Once performed and acceptable these tests are not repeated unless a major design change is made which would require a new PDQ.

a. Product failures: Perform step stress testing in order to generate failures, not produce the absence of failures.

b. Failure analysis: Once failure occurs, perform failure analysis (if needed) to ascertain the mechanisms and failure rates or time to wearout.

c. Engineering evaluations: Evaluate to constantly improve the final product quality and reliability.

d. Failure mechanism identification: Identify and focus on failure mechanisms typical for the technology (assembly, packages, and die-level failures).

C.8.1.2 Detailed elements of a design qualification program.

a. Defining a device family: In order to provide acceptable coverage during representative reliability assessment testing, all devices must first be grouped into their respective device families. Device families may be selected based on characteristics from the following three categories:

    1) Package grouping based on: package profile, volume, complexity of package construction, and number of pins or wire bonds.

    2) Overall construction grouping based on: Die attach method, interconnect construction techniques (e.g., spring contact) or category of bond.

    3) Die grouping based on: Overall dimensions, aspect ratio, thickness, number of bonds, voltage, frequency, or power rating.

When selecting device families, consideration must also be given to differences due to the use of different production facilities, variations in fabrication procedures, and differing design techniques. Differences or variations, which may influence device reliability, imply that a separate device family should be established. Ignoring these factors in creating device families must be justified to the qualifying activity.

Identification of worst case devices: Once device families have been established, worst case device types from within those families must be selected which will provide coverage for the reliability assessment of all other devices within the family. Worst case parameters (or combinations of parameters) from within the three categories listed above (i.e., packaging, overall construction, and die) must be identified in order to establish which devices are worst case.

C.8.2 Process optimization. Process optimization is the mechanism to provide for continuous improvement as equipment and materials technology changes. Following process characterization, it is necessary to optimize the process parameters. Optimization is accomplished through identification of optimal targets and continual reduction of variation around those targets. Process characterization should be conducted on the entire process (i.e., design through delivery). A matrix should be developed that identifies failure mechanisms and their controls (see C.5.2 FMEA). The ability to maintain control of key process points will determine process capability.

C.8.2.1 Test optimization. The manufacturer may use statistical techniques and historical data to reduce, modify, move or eliminate tests. Manufacturer specific optimization requires the approval of the qualifying activity, and preparing activity. The manufacturer must have a test optimization program in place that meets JEP121 or, an equivalent system, which justifies the proposed changes. Process monitoring and controls, statistical techniques (i.e., PPM, Cpk, FIT), and accumulated data may be used to prove the validity of test optimization. All optimizations shall be monitored for compliance to initial qualification baseline requirements.

C.8.2.2 Methods of test optimization. Test optimization includes the alternative methods listed below.

a. Reduction of testing/sampling. This includes reduction in the number of samples or test frequency, whether it is within a lot or periodic sampling.

b. Modification of tests. This includes using alternative test procedures, or equipment.

c. Moved tests. This pertains to performing tests in process instead of after all processing is complete.

d. Elimination of tests. The tests are no longer performed.

e. Any combination of the above.

C.8.3 Process validation: (on-going reliability) or (conformance inspection). The process needs to be validated on a regular basis to confirm continuing conformance to the originally qualified design parameters. The two methods of validation are either conformance inspection (appendix E) or on-going reliability. Conformance inspection may only be used as a validation for this appendix if a continuous improvement feedback loop is documented that ensures conformance failures are analyzed for root cause and corrective actions are taken to modify both the FMEA and the control plan thereby eliminating the failure mechanism.

C.8.3.1 On-going reliability guidance criteria. With the approval of the qualifying activity and preparing activity, this program or an equivalent program may be used as an alternative to the conformance inspection.

C.8.3.1.1 General elements of an on-going reliability program. An ongoing reliability program is designed to create a closed loop feedback system, which will generate continuous improvement. Existing production lines are constantly sampled and tested. This proves the critical interfaces and manufacturing process are stable and repeatable, as well as providing a mechanism for failures to be evaluated and the process improved. The ongoing reliability program shall include, as a minimum, the following:

a. Program will formalize the routine reliability testing and tie failures to a specific manufacturing process.

b. Program will integrate FMEA with reliability surveillance.

c. Restructure surveillance program by "root technologies", rather than by individual part numbers.

d. All ongoing reliability testing will continue routinely.

e. Samples will be tested per a specified frequency in key environmental test, eg., HTRB, Solder Dip, and Thermal Shock.

f. Failures will be reviewed and tracked to a specific manufacturing process.

g. The ongoing reliability program will record type of failure, manufacturing process, and root cause/ corrective action.

C.8.4 Continuous improvement. A comprehensive continuous improvement philosophy shall be fully deployed throughout the company’s organization. Manufacturers shall continuously improve in quality, service and reliability for all customers. This requirement does not replace the need for innovative improvements. Manufacturers shall develop specific action plans for continuous improvement in processes that are most important to the customer once those processes have demonstrated stability and acceptable capability. Continuous improvement means optimizing the characteristics and parameters at a target value and reducing variation around that value.

C.8.4.1 Quality and productivity improvement. The manufacturer shall identify opportunities for quality and productivity improvement and implement appropriate action plans. Some examples are:

a. Excessive variation.

b. Manufacturing yields.

c. Scrap, rework and repair.

d. Optimization of tests.

e. Excessive cost of non-quality.

f. Machine down-time.

g. Machine set-up.

h. Cycle time.

i. Customer dissatisfaction, e.g., complaints, repairs, returns, mis-shipments, incomplete orders, customer plant concerns, and warranty.

C.8.4.2 Measures and methodologies. The manufacturer shall demonstrate knowledge of the following measures and methodologies and shall use those that are appropriate:

a. Capability indices.

b. Control charts.

c. Design of experiments.

d. Cost of quality.

e. Parts per million analysis.

f. Problem solving.

g. Benchmarking.

C.8.5 Qualification. The manufacturer shall have a qualification procedure. Initial qualifications for any product shall demonstrate compliance to the Performance Specification Sheet. It may be an extension of the product design qualification (PDQ) or a modification to the Product Manufacturing Qualification (PMQ). The qualification plan should include the following elements:

a. Multiple samples.

b. hour or cycle tests.

c. Pre conditioning, if warranted.

d. Mechanical test.

e. Electrical test.

f. Environmental stress test.

Existing data can be submitted for evaluation by the qualifying activity if the data is from the same product family and the designs are similar. The TRB defines the qualification test plan and monitors lot formation and inspection results. This plan may be based on previous data recorded for other purposes. Equivalence of all tests and inspections must be determined by the TRB. The TRB must be able to demonstrate to the Preparing and qualifying Activities that the product is capable of meeting the performance requirements outlined in MIL-PRF-19500 and the performance specification sheets. The TRB must perform a comprehensive analysis of the qualification data. The data and the results of the TRB review must be available to the qualifying activity upon request. The TRB then notifies the qualifying activity of part numbers and quality assurance levels for inclusion on QML-19500. Design and construction information must also be submitted with qualification notification.

APPENDIX C

C.9 Maintaining QM program certification. Certification and lab suitability will be maintained through DSCC re-audits based on the previous audit findings, status reports, and other correspondence. As the confidence level and relationship between the manufacturer and the qualifying activity increases, the need for re-audits decreases.

C.10 Removal of TRB authority. The success of the TRB depends on the manufacturer. Continuing participation is conditioned upon compliance with the QML requirements. Responsibility for removing TRB authority is a function of the qualifying activity.

APPENDIX D

QUALITY SYSTEM

D.1 SCOPE

D.1.1 Scope. This appendix contains details of the quality system for MIL-PRF-19500 semiconductor devices. The verification system measures and evaluates the manufacturer's manufacturing process against a baseline for that process. This baseline can include innovative and improved processes that result in an equivalent or higher quality product, provided that the process used to evaluate and document these changes has been reviewed and approved by the qualifying activity (see 4.4). Changes to the process baseline can be made by the manufacturer after achieving approval with documented reliability and quality data. The approach outlined in this appendix is a proven baseline which contains details of a quality system including best commercial practices. However manufacturers must demonstrate to the qualifying activity a quality system that achieves at least the same level of quality as could be achieved by complying with this appendix. Certification is provided by the qualifying activity upon approval by the preparing activity (for equivalent quality systems) and qualifying activity. Reduction of test will be approved on a case by case basis. A Qualified Products supplier is compliant to this appendix. A Qualified Products supplier is one who exercises a system which focuses on product and inspections. The DSCC audit is product oriented. This appendix is a mandatory part of this specification. The information contained herein is intended for compliance only.

D.2 APPLICABLE DOCUMENTS.

D.2.1 General. The documents listed in this section are specified in sections 3 and 4 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements found in documents cited in sections 3 and 4 of this specification, whether or not the documents are listed.

D.2.2 Non-Government standards and other publications. The following documents form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents which are DoD adopted shall be those listed in the issue of the DODISS cited in the solicitation. Unless otherwise specified, the issues of documents not listed in the DODISS are the issues of the documents cited in the solicitation (see 6.2).

AMERICAN NATIONAL STANDARDS INSTITUTE (ANSI)

ANSI/NCSL-Z540-1-1994	Calibration Systems Requirements.
ANSI/ISO/ASQC Q9001-1994	Quality Systems - Model for QA in Design, Development, Production Installation, and Servicing

(Application for copies should be addressed to the American National Standards Institute, 11 West 42nd Street, New York, NY 10036.)

ELECTRONIC INDUSTRIES ALLIANCE (EIA)

EIA-554 A	Method selection for assessment of Non-conforming Levels in Part Per Million (PPM) (DOD adopted).
EIA-557	Statistical Process Control Systems.
EIA-625	Requirements for Handling Electrostatic-Discharge Sensitive (ESDS) Devices.
JEDEC Publication 114	Analysis of Component PIND Test Failures.

(Application for copies should be addressed to the Electronic Industries Alliance, 2500 Wilson Boulevard, Arlington, VA 22201-3834.)

(Non-Government standards and other publications are normally available from the organizations which prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

D.2.3 Order of precedence. In the event of a conflict between the text of this document and the references cited herein (except for related performance specification sheets), the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

D.3 Quality system. Devices furnished under this specification shall comply with the performance requirements of 3. herein, and shall be prepared for delivery in accordance with 5. herein. The verification system shall assure that the design, processing, assembly, inspection, and testing of semiconductor devices comply with this specification and the performance specification sheet. ANSI/ISO/ASQC-Q9001-1994 is a baseline which contains details of a quality system.

APPENDIX D

D.3.1 Management responsibility.

D.3.1.1 Management responsibility. Management shall provide sufficient resources, personnel, and authority necessary for performing all applicable verification and manufacturing certification requirements specified herein.

D.3.1.2 Organization. A functional block organization chart shall be included in the quality system program (see D.3.2.1) which shows the lines of responsibility and authority for organization, approval, and implementation of all aspects of the quality program. A management representative shall be identified who has defined responsibility and authority to ensure that the requirements of this specification are met.

D.3.1.3 Responsibility and authority.

D.3.1.3.1 Definition of a manufacturer. For guidance on specific business scenarios, details of implementation, financial commitment to this program, or interpretation of criteria herein, contact the qualifying activity. The manufacturer is the basic plant.

D.3.1.3.1.1 Basic plant. The basic plant is where wafer fabrication or device assembly is performed. The basic plant has the responsibility for device critical interfaces, performance, quality, and reliability. The manufacturer's designating symbol of the basic plant shall appear on the finished product. Total ownership of the basic plant is required for listing and JAN Branding. The basic plant shall be certified and qualified by the qualifying activity. Contractors shall ensure their subcontractors meet the requirements of MIL-PRF-19500.

D.3.1.3.1.2 Contracted plant. The basic plant may contract assembly or wafer fabrication provided control of the contracted plant is demonstrated to the qualifying activity. A written agreement between a basic plant and a contracted plant is necessary for all contracting scenarios. This agreement shall establish who is the basic plant. For any device type a basic plant may not contract both assembly and wafer fabrication. The contracted plant shall be certified by the qualifying activity. Qualification of assembled devices or wafers will be the responsibility of the basic plant. Manufacturers may offer their certified line services to each other through the contracted plant provisions.

D.3.1.3.1.3 Contracted wafer fabrication. JANHC die evaluation or equivalent die evaluation per wafer lot shall be performed whenever a contracted wafer fabrication plant is utilized by the basic assembly plant. This die evaluation may be performed by either the contracted plant or the basic plant and is applicable to JAN, JANTX, and JANTXV. A JANS certified assembly facility may contract any JANS certified wafer fabrication facility for the purpose of qualifying JANS devices. For JANS devices, JANKC die evaluation or equivalent applies.

D.3.1.3.1.4 Wafer fabrication. The wafer fabrication plant (basic wafer fabrication plant or contracted wafer fabrication plant) may contract any or all of the following processes to specialty laboratories:

a. Epitaxial deposition.

b. Ion implantation.

c. Irradiation (for carrier lifetime suppression).

d. Back grinding.

The applicable flow chart and traveler will identify any contracted process.

D.3.1.3.2 Responsibility of the manufacturer. The manufacturer is responsible for the performance of all inspection requirements as specified herein, and in the performance specification sheet. The manufacturer may use their own or other suitable facilities which have been approved and granted laboratory suitability by the qualifying activity for the performance of MIL-STD-750 inspection requirements specified herein. The Government or acquiring activity reserves the right to witness or perform any of these inspections set forth herein or in the performance specification sheet and to audit the data resulting from the manufacturer's performance of these specifications.

D.3.1.3.3 Incoming, in-process, and outgoing inventory control. The manufacturer shall employ procedures to control storage and handling of incoming materials, work in-process, warehoused and outgoing product in order to (a) achieve such factors as age control of limited-life materials; and (b) prevent inadvertent mixing of conforming and nonconforming materials, work in process, finished product, resubmitted lots, or customer returns.

D.3.1.3.4 Personnel. Personnel performing quality functions shall have sufficient well-defined responsibility, authority, and the organizational freedom to identify and evaluate quality problems and to initiate, recommend, or provide solutions.

D.3.1.4 Resources. The manufacturer shall identify requirements and provide adequate resources for management, performance of work, verification activities, and internal audits. For the purpose of this document, resources shall include, but not be limited to, materials, equipment, training, and personnel.

D.3.1.5 Management representative. The manufacturer shall appoint a member of his management who has the authority and responsibility for development and implementation of the quality system of this appendix. This individual shall insure that the quality system is maintained and shall periodically report to the manufacturers management on the performance of the system and opportunities to improve it. The qualifying activity shall be informed whenever there is a change in the management representative.

D.3.1.6 Management review. The manufacturers management shall maintain an ongoing cognizance of the status of the quality system to ensure its' continuous suitability and effectiveness in satisfying the requirements herein through periodic reviews of the quality system.

D.3.2 Quality system.

D.3.2.1 Quality system requirements. A quality system shall be established by each manufacturer which implements all requirements of this appendix. This system shall be documented in a Quality Manual. The current revision of the Quality Manual shall serve to demonstrate to the qualifying activity that the manufacturer's system is adequate to assure compliance with the applicable specifications and quality standards. Proprietary documents shall be clearly identified by category in the system.

D.3.2.2 Process flows. The system includes process flows for each distinct product family. As a minimum, flows shall include wafer fabrication, assembly, screening and CI, and shall indicate which CI option has been selected.

D.3.2.3 Quality system procedures. The manufacturer shall implement the approved system. The range and detail of the procedures shall ensure compliance with this system.

D.3.2.4 Quality planning. The manufacturer shall define how the requirements for quality will be met. Quality planning shall be consistent with all other requirements of the manufacturer's quality system. The manufacturer shall give consideration to the following activities, as appropriate, in meeting the specified requirements for products.

a. The preparation of quality plans.

b. The identification and acquisition of any controls, processes, equipment (including inspection and test equipment), fixtures, resources, and skills that may be needed to achieve the required quality.

c. Ensuring the compatibility of the design, production process, inspection, and test procedures.

d. The updating, as necessary, of quality control, inspection, and testing techniques, including the development of new instrumentation.

e. The identification of any measurement requirement involving capability that exceeds the known state of the art, in sufficient time for the needed capability to be developed.

f. The identification of suitable verification at appropriate stages in the realization of product.

g. The clarification of standards of acceptability for all features and requirements, including those which contain a subjective element.

h. The identification of all subcontracted processes.

D.3.3 Conversion of customer requirements. The manufacturer shall have a system to convert performance specification sheet requirements to in-house, procedures, methods, and specifications. The system shall include revision and distribution controls. The manufacturer's system ensures review of purchase requirements (and modifications) received from their customer. The review shall insure that the purchase order does not violate this specification for JAN product of any level and that any special instructions are accounted for. The system shall provide objective evidence of this review.

D.3.4 Critical interface control.

D.3.4.1 Design, materials, and processing documentation. Each product design shall be fully specified such that all aspects of design, verification testing, processing, and materials are described. In addition, each manufacturer shall have a flow chart, traveler and a design and construction form for each certified product line (see qualifying activity).

D.3.4.2 Design changes. After qualification, the manufacturer shall notify the qualifying activity prior to the release and shipment (for JANS prior to line implementation except for evaluation samples) of product which undergoes any change in the product or verification program which affects performance, quality, appearance, reliability or interchangeability (see appendix E, table III) and E.6.1.6. The changes shall be approved by the qualifying activity prior to release and shipment of product. Changes in design, materials, or processes for any device must be processed in accordance with established change control procedures for all affected documents (see D.3.4.1 and D.3.5). Such notification shall include a thorough description of the proposed change and a test plan designed to demonstrate that the change will not adversely affect performance, quality, reliability, or interchangeability and that the changed product will continue to meet the specification requirements. The completed test results shall be approved by the qualifying activity. After approval of the design change, all product inventory of the old design must be submitted to CI within 6 months, unless authorization is extended by the qualifying activity (see H.3.1). Unless the design change has been required to correct or eliminate a verified design defect, finished devices manufactured to the previously approved design which are in inventory or in process of testing (i.e., inspection lot identification code assigned) will remain qualified only until that inventory is depleted.

D.3.5 Document control.

D.3.5.1 Document control. The manufacturer shall establish and maintain procedures to control all documents that relate to the requirements of this specification. This includes, to the extent applicable, military and industry specifications and standards. These procedures are required to be in a language that is understandable by the operator performing the given operation.

D.3.5.2 Document approval and issue. Documents shall be reviewed and approved for adequacy by authorized personnel prior to issue. A procedure shall be established to ensure that the current issue of appropriate documents are available at all required locations, that invalid or obsolete documents are promptly removed from all points of issue, and that any obsolete documents which are retained are suitably identified.

D.3.5.3 Document changes. Unless designated otherwise, changes to documents shall be reviewed and approved by the same functions/organizations that performed the original review and approval.

D.3.6 Purchasing.

D.3.6.1 Acquisition documentation. A system for the acquisition of supplies and approval of suppliers shall be established.

D.3.7 Control of customer supplied material. The manufacturer shall establish and maintain procedures for the control, verification, maintenance and storage, as applicable, of customer supplied materials and equipment. Any material which is lost or becomes unsuitable for use shall be recorded and reported to the customer.

D.3.8 Product identification and traceability. All devices delivered to this specification shall be traceable through the lot identification code and inspection lot records, and identified as in 3.7 and 3.10. In addition, JANS devices shall have a lot control system from wafer processing through screening which provides wafer lot identification; operation (machine); date of operation, operator(s) identification, quantity; and serial numbers (after step 8 of appendix E, table IV) of devices processed.

D.3.9 Process control. The manufacturer shall assure that all manufacturing operations are carried out to insure continued process capability. Operations shall be controlled as to the manner of production, requirements for monitoring and control, and output product characteristics. Where necessary, due to the complexity or sensitivity of operation parameters, the process shall consider working environment, workmanship criteria, equipment set-up and the need for special operator certification or continuous monitoring of critical parameters.

D 3.9.1 Statistical Process Control (SPC). Where SPC is used to control a process, the control must be established in accordance with EIA-557. If a sample exhibits an out-of-control condition, the product represented by the sample shall be subjected to evaluation and disposition. The evaluation process, results, and disposition shall be documented and traceable.

D 3.9.2 Environmental controls. The relative humidity, temperature, and particle count for each applicable critical process step (e.g., wafer fabrication, assembly) shall be specified, controlled, and recorded. The procedures and techniques for measuring these environmental parameters and limits shall be documented. The procedures shall contain corrective actions for out-of-tolerance environmental conditions. Unsealed parts shall be handled in such a way as to minimize the introduction of foreign material into the cavity. In addition, spittle protection is required in applicable critical areas. See MIL-STD-750, test method 5010.

D 3.9.3 Chemical controls. The purity of chemicals, including water, shall be specified and controlled. The purity of process water shall be measured and recorded in terms of resistivity at +25°C (resistivity cells and meters shall be calibrated), total solids, organic impurities and bacteria count.

D.3.9.4 Wafer lot process and inspection. The methods and procedures which are utilized within wafer production for the following functions, as a minimum, must be documented:

a. Sample sizes.

b. Wafer cleaning and handling operations.

c. Junction and surface preparations.

d. Alloying processes.

e. Control of wafer thickness (For JANS, deviation must be within 20 percent of the approved design nominal.)

f. Metal deposition and thickness (For JANS, maximum thickness deviation shall be within 30 percent for the approved design nominal of > 35KA, and within 25 percent for $\leq$ 35KA.

g. Glassivation and passivation thickness (For JANS, deviation shall be within 30 percent of the approved design nominal. For overlay structures or expanded metallization a minimum thickness of 6,000 Å for SiO_2 or 2000 Å for Si_3N_4) is required.

h. Gold backing thickness, when applicable (For JANS, deviation shall be within 30 percent of the approved design nominal.

i. SEM, see E.3.1.2.2 (For JANS).

Where limits are based on tolerances about an “Approved Design Nominal” the nominal shall be stated in DSCC Design and Construction Sheet, DSCC Form 36D, submitted for approval by the qualifying activity.

D.3.9.5 Process monitor programs. Process monitor programs shall be established as referenced below, for processes performed by the manufacturer. A fully implemented and approved SPC program (in accordance with D.3.20.1) may replace all or portions of the process monitor programs with the approval of the qualifying activity. These programs shall be documented and made available to the certification team for review. The implementing procedures shall provide for frequency, sample size, reject criteria, allowable rework, and disposition of failed product/lots. Investigative and corrective actions shall be established which address noted deficiencies. With the exception of the particle detection monitor, a procedure is required for the traceability, recovery, and disposition of all units monitored since the last successful test. As with all monitors, the particle detection procedure shall provide for continual process improvement. Records of these monitors shall be available to any (Government or military user) audit team for review. As a minimum, the process monitors shall include the following, or equivalent as approved by the qualifying activity:

a. Die attachment. The type of die mounting method, die material, die mounting material, package material, and mounting configuration shall be documented. The time, temperature, pressure, scrubbing, cleanliness, and environment shall also be specified. The manufacturer shall monitor the die attach integrity for all silicon transistors and case mounted diodes in accordance with test method 2017 or thermal response test methods 3101, 3161, 3131, 3103, and 3104 of MIL-STD-750 using the manufacturer's documented procedure. This procedure shall be performed at each equipment set up as a minimum for JANTX and JANTXV and may, at the manufacturers option, consider other related factors. This test shall be conducted on a minimum of two devices from each die attach station at the start and finish of operator change, package type change, die size change and after every two hours of production for JANS. If an appropriate thermal response method is performed in 100 percent screening, this shall serve as the die attach process monitor. In the event that the die shear is less than the value of figure 1 of test method 2017, or the test leaves less than 75 percent silicon remaining of die-to-header bond surface, the output of the die attach station shall not be used until tests show that satisfactory operation has been re-established. A procedure for the traceability, recovery, and disposition of all units bonded since the last successful die attach integrity test is required. This procedure shall provide for sample size, reject criteria, and disposition of failed lots. This test may be conducted on the same samples used for the wire bond strength test.

b. Wire bonding or interconnection. The bonding techniques, type of bond wire, and lead material used in connecting the die to the package leads shall be documented and comply with this specification and the applicable performance specification sheets. The temperature, pressure, dwell time, control of condition of capillary or electrode, ultrasonic power, composition of metals, lead dress, thickness to width ratio of bond, and environment shall be specified. The manufacturer shall monitor the wire bond strength in accordance with test method 2037 of MIL-STD-750 using the manufacturer's documented procedure. This procedure shall be performed at each equipment setup as a minimum for JANTX and JANTXV and may, at the manufacturer's option consider change of operators, lot size, shift start and stop, and other related factors. As a minimum for JANS each operator/wire bonding station shall have two device samples taken at the start and end of each shift, after each two hours of production, and after changing operators, spools, shifts, packages, wire size, and maintenance of equipment. When more than one lot is processed for JANS in a two-hour period, samples shall be tested from each lot. Pull strength data shall be read and recorded and shall be control charted and maintained in accordance with the specified requirements. Data shall include the force, in grams, required for failure, the physical location of the point of failure, and the nature of the failure. In event that any bond strength is less than the pre-seal value given in table I, test method 2037, of MIL-STD-750, the bonder shall be inactivated immediately and not returned to production until tests show that satisfactory operation has been re-established. When the system at the die surface is bimetallic and the lead wires are less than 5 mils in diameter, the lead shall be pulled to destruction and if the chip bond lifts before the wire breaks, the lot shall be rejected. A procedure for the traceability, recovery, and disposition of all units bonded since the last successful bond strength test is required. This procedure shall provide for sample size, number of bonds and device to be tested, reject criteria, and disposition of failed lots.

c. Glass-to-lead seals on clear glass diodes. Visual inspection procedures shall specify inspection criteria, the use of visual aids, and shall comply with the requirements of test methods 2069, 2070, 2072 or 2073 (die visual), and 2074 of MIL-STD-750. In addition, the manufacturer shall monitor the lead-to-glass seal following final plating operation for all JANTX, JANTXV, JANJ and JANS clear glass diodes constructed with borated seal using the manufacturer's documented procedure. The procedures shall specify criteria and visual aids and shall be capable of detecting significant loss of glass-to-lead seal.

d. Lid seal. The moisture content of the sealing environment shall be controlled. The internal moisture content of device packages with an internal cavity greater than .01 cc shall not exceed 5,000 PPM when tested in accordance with MIL-STD-750, test method 1018 at +100°C. All manufacturers shall exercise package internal moisture content monitors at key locations in the manufacturing flow. When the internal water vapor content test is performed, the samples shall have been subjected to screen 3 or equivalent; not required for devices which are inactive for new design. All devices not utilizing a eutectic or epoxy die attach shall have the internal oxygen content of the sealing environment controlled. For devices not utilizing a eutectic or epoxy die attach the internal oxygen content of the device package shall not exceed 2,000 PPM at +100°C. When the internal oxygen content test is performed, the samples shall have been subjected to screen 3 of table IV or equivalent; not required for devices which are inactive for new design.

e. Particle contamination. The manufacturer shall establish a particle detection monitoring program which assesses the source of particle contamination of sealed cavity devices on an individual manufacturing line basis. The monitor shall have provisions for testing in accordance with method 2052, condition A, of MIL-STD-750. JEDEC Publication 114, "Guidelines for Particle Impact Noise Detection (PIND) Testing, Operator Training, and Certification" may be used as a guideline. Unless otherwise exempt herein, this monitor is applicable to all metal or ceramic cavity package outlines. This monitor shall be performed at the assembly location, or locations, to ensure the most effective feedback loop for corrective action.

f. Application of final lead finish: (see appendix H).

g. Wafer fabrication. The manufacturer shall establish the necessary controls (or equivalent, subject to the approval of the qualifying activity) for D.3.9.4, e through h above. For JANS, compliance to tolerance about the “Approved Design Nominal” shall be demonstrated.

h. Lot norm testing. For all diodes, zeners, and rectifiers with a power dissipation rating of $\leq$ 1 watt the manufacturer shall have a documented program to characterize leakage current at + 25°C and, when specified, thermal impedance to identify atypical devices. Devices which exhibit atypical behavior shall be rejected and removed from the lot.

D.3.10 Inspection and testing.

D.3.10.1 Inspection of purchased materials. The manufacturer is responsible for assuring that all supplies and services procured from suppliers conform to the purchase contract. The manufacturer shall have a system which controls inspection, storage, and handling of incoming materials, and periodic evaluation of material received. The system may include verification of chemical, physical, and functional characteristics required by manufacturer drawings and specifications. The manufacturer may utilize a certified supplier program to reduce or eliminate receiving inspection.

D.3.10.1.1 Certified supplier program. The capability of supplied material may be validated through a supplier certification system. This program selects and monitors suppliers in order to guarantee that the supplied material will meet and maintain required capability levels (e.g., Cpk, PPM, etc.).

D.3.10.2 In-process quality control. The manufacturer shall perform in-process inspections to the extent necessary to assure product conformance to the end item specification. This shall include inspections and tests which assure that the manufacturing processes are in a state of control as indicated in D.3.9 herein.

D.3.10.2.1 Manufacturer imposed tests. Any manufacturer imposed test(s) (e.g., gross and fine leak) conducted prior to any qualification or CI, are to be performed on all subsequent lots until re-qualified. If any manufacturer imposed tests detect a problem, the manufacturer shall submit all devices in the lot to those tests to eliminate rejects and shall take steps to determine and eliminate the cause of failure (e.g., rough handling which has produced gross leaks).

D.3.10.3 Testing and screening operations. Testing and screening operations may only be performed in a facility which has received laboratory suitability approval from the qualifying activity for each MIL-STD-750 test method to be employed. The environmental conditions where testing and screening are performed shall be maintained to assure compliance with the requirements of MIL-STD-750.

D.3.10.4 Final inspection and testing.

D.3.10.4.1 Qualification and conformance inspection. Qualification and Conformance Inspection shall be performed as required by the performance specification sheet and herein at a facility which has received laboratory suitability approval from the qualifying activity. The results of testing shall be reviewed and approved.

D.3.10.5 Inspection and test verification. The manufacturer shall verify that all inspection and testing required by this specification and their quality plan (see D.3.2.4) has been accomplished as specified. Verification shall clearly show whether the product passed or failed any requirement and shall contain sufficient detail to allow traceability to a specific operator, test date, and program.

D.3.11 Control of inspection measuring and test equipment.

D.3.11.1 Test programs and setups. The test programs and setups used to sort, classify, and test for MIL-PRF-19500 requirements are required to be traceable through each document control system to insure the correct revision was used when testing MIL-PRF-19500 devices.

D.3.11.2 Test equipment maintenance and calibration system. Maintenance and calibration systems and the frequency of scheduled actions, for gauges and test equipment, shall be established. The system may use ANSI/NCSL Z540-1-1994, or equivalent, as a guideline.

D.3.11.3 Conditions and methods of test. The general requirements, conditions and methods of test shall be in accordance with MIL-STD-750.

D.3.11.4 Electrical test equipment verification. The manufacturer shall define and utilize a method (e.g., correlation samples, diagnosis routines, etc.) to verify the measurement and operation characteristics of the test equipment when in use. In the event of verification of failure, the manufacturer shall utilize a procedure which will determine the requirements for traceability, recovery, and when re-testing is required of all units tested since the last successful verification.

D.3.12 Inspection and test status.

D.3.12.1 Inspection and test status. A system shall be maintained to insure that products are identified by their test or inspection status. The system shall insure the separation of products that have been tested or inspected from product that has not.

D.3.13 Control of nonconforming product. The manufacturer shall maintain a system which will prevent the shipment or use of nonconforming product. The system shall provide for identification, segregation, and evaluation of product which does not conform to specified requirements at any point in the manufacturing and screening flow. Devices or lots which fail any specification or internal tests, procedures, and requirements above and beyond the specification, except electrical selections, are not suitable for any JAN level. Lots failing electrical selections for any JAN level which 1) are above and beyond this specification, and 2) are intended to select a portion of a lot having greater performance or reliability than the overall average performance or reliability of the lot other than through statistical methods are not suitable for any JAN level.

D.3.13.1 Reworked product. Reworked or repaired product shall be re-inspected in accordance with the appropriate procedures. All rework performed shall be documented and traceable and may be part of management review.

D.3.13.2 Rework provisions. All allowable rework on devices manufactured under this specification shall be accomplished in accordance with the established procedures. Lots shall not exceed two reworks for any process.

D.3.13.2.1 Wafer rework. For wafers, rework is limited to the following: Additional etch to correct a nonconformance to a specification limit; photoresist strip and recoat; additional processing to continue or finish incomplete processing; strip and redeposit of non-junction passivation or backside metallization. For JANS, strip and redeposition of any oxide, or passivation layer is not allowed.

D.3.13.2.2 Rework of assembled devices. No delidding or package opening shall be permitted except for disc packages. Unless otherwise specified, rework of sealed packages is limited to recleaning, rebranding to correct defective marking, and lead straightening, re-plating or re-solder dipping of the leads. After any re-plating, all JANS, JANTXV, and JANTX shall pass as a 100 percent screen the requirements of group A, subgroup 2 and the hermetic seal requirements of screen 7 of table IV herein. Solder dip rework shall be in accordance with appendix H.

D.3.13.3 Rejected lots. Lots with an unscreenable failure mode shall be rejected

D.3.14 Corrective and preventive action.

D.3.14.1 Corrective action. The system identifies the necessity for corrective action as a result of failure, defect analysis, inappropriate performance of inspections/procedures, product trends, product returns, inappropriate records and audits. Failure to initiate corrective action may result in removal of products from the qualified product list. The corrective action system shall identify when a failure analysis is to be employed (i.e., Field use, user analysis, GIDEP, competitive analysis).

D.3.14.2 Preventive action. Appropriate sources of information such as processes and work operations which affect product quality, audit results, quality records, and customer complaints shall be used to detect, analyze, and eliminate potential causes of non-conformities. The methodology for the initiation, implementation, and follow up of preventive actions shall be documented by the manufacturer.

D.3.15 Handling, storage, packaging, and delivery.

D.3.15.1 Security of completed devices. Marked devices which have passed all screening and conformance requirements shall be retained in a secure area prior to shipment delivery. Device inventory shall be controlled by device type, lot identification code, quantity, product assurance level, and transaction date. This requirement applies to both the manufacturer and the distributor(s).

D.3.15.2 ESDS program. The manufacturer of ESDS class 1 and 2 devices shall institute an ESDS program commensurate with the product classification. The product classification shall be as indicated in appendix E. The requirements of EIA-625 apply but may be tailored for establishing an ESDS program. Justification for the tailoring shall be made available to the qualifying activity for approval upon request.

D.3.16 Quality records. A system shall be in place to track all quality records, including but not limited to the results of all qualification, screening, conformance tests (attributes or variable data) and inspections, any required failure analysis, subcontractor records, internal quality audit results, training, and management reviews. The retention period for each type of quality records shall be a minimum of 5 years.

D.3.17 Internal quality audits.

D.3.17.1 Internal audit program. The manufacturer shall establish an independent internal audit program which shall be included in the quality system. The internal audit program shall assess compliance with all applicable quality system requirements and shall identify key review areas, their frequency of audit, and corrective actions shall be resolved through the corrective action system (see D.3.14). The internal audit program shall include any subcontractors used.

D.3.17.1.1 Internal audit checklist. The internal audit checklist shall assure that the quality system is adequate and followed by all personnel in each area.

D.3.17.2 Audit schedules and frequencies. The audit frequency shall in no case exceed one year for each area unless authorized by the qualifying activity. An internal audit shall be conducted and corrective actions completed prior to the initial qualifying activity audit. The qualifying activity may modify the frequency of the internal audit(s) or require additional inspection based on the effectiveness of the manufacturer's internal audit program, and assessment of the internal audit findings.

D.3.17.3 Auditors. The designated auditors shall be independent from the area being audited. If the use of an independent auditor is not practical a second individual should be assigned to participate in the audit or review the results. Auditors shall be trained in the area to be audited, in the applicable military specification requirements and provided with an appropriate checklist for annotating deficiencies. Prior to the audit, the assigned auditor(s) shall review the previous internal audit results to assure corrective actions have been implemented and are effective.

D.3.17.4 Audit deficiencies. All audit deficiencies shall be conveyed to the responsible individual for corrective action(s). All corrective actions shall be agreed to by the management representative. A procedure shall be established to follow up on all audit deficiencies to assure that the corrective actions have been implemented in a timely manner. If recurrent deficiencies are found additional corrective action shall be taken to assure correction of the problem and the qualifying activity shall be notified. The internal audit team shall perform a 6-month follow-up verification of corrective actions to assure that they are adequate.

D.3.18 Training.

D.3.18.1 Personnel performing quality operations. All personnel performing an operation affecting quality shall be trained in and familiar with that part of the operation relevant to their function. They shall have sufficient responsibility and authority to inspect and accept or reject product according to the applicable specifications.

D.3.18.2 Training requirements. Work training practices shall be established and utilized in acquiring and maintaining job skills as required in critical work areas.

D.3.19 Servicing. The manufacturer's system shall describe the methods used to meet customer expectations, this includes but is not limited to: applications support, customer returns, stock rotation, GIDEP issuance, warranty issues, and customer complaints.

D.3.20 Statistical techniques.

D.3.20.1 SPC program. The method used for process control may or may not utilize SPC, but will use a method that is appropriate for the process being controlled. Compliance with EIA-557 is a requirement for JANS certification.

D.3.20.2 Parts per million (PPM) Program. The manufacturer shall implement a Non-conforming Level Assessment in accordance with EIA-554A, and associated documents. The manufacturer's Quality System documentation shall outline the method(s) utilized, and the subsequent reporting structure.

APPENDIX E

STANDARD VERIFICATION SYSTEM FOR QUALIFED PRODUCTS

E.1 SCOPE

E.1.1 Scope. This appendix contains the standard verification system which, when performed in its entirety, assures that the product will meet the performance requirements. This Qualified Products program also measures and evaluates the manufacturer's manufacturing process against a baseline for that process. This baseline can include innovative and improved processes that result in an equivalent or higher quality product, provided that the process used to evaluate and document these changes have been reviewed and approved by the qualifying activity. Changes to the process baseline can be made by the manufacturer after achieving approval with documented reliability and quality data. The approach outlined in this appendix is a proven baseline which contains details of the screening and CI procedures. However, manufacturers must demonstrate to the qualifying activity a system that achieves at least the same level of quality as could be achieved by complying with this appendix. This appendix is a mandatory part of this specification. The information contained herein is intended for compliance only.

E.2 APPLICABLE DOCUMENT

E.2.1 General. The documents listed in this section are specified in E.3 through E.6 of this specification. This section does not include documents cited in other sections of this appendix or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements documents cited in sections E.3 through E.6 herein, whether or not they are listed.

E.2.2 Non-Government standards and other publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents which are DoD adopted are those listed in the issue of the DODISS cited in the solicitation. Unless otherwise specified, the issues of documents not listed in the DODISS are the issues of the documents cited in the solicitation (see 6.2).

AMERICAN NATIONAL STANDARDS INSTITUTE (ANSI)

ANSI/NCSL-Z540-1-1994	Calibration Systems Requirements.

(Application for copies should be addressed to the American National Standards Institute, 11 West 42nd Street, New York, NY 10036.)

ELECTRONIC INDUSTRIES ALLIANCE (EIA)

EIA-557	Statistical Process Control Systems.
EIA-625	Requirements for Handling Electrostatic-Discharge Sensitive (ESDS) Devices.

(Application for copies should be addressed to the Electronic Industries Alliance, 2500 Wilson Boulevard, Arlington VA 22201-3834.)

(Non-Government standards and other publications are normally available from the organizations which prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

E.2.3 Order of precedence. In the event of a conflict between the text of this document and the references cited herein (except for related performance specification sheets), the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

E.3 GENERAL TEST AND INSPECTION INFORMATION

E.3.1 Formation of inspection lots. The product shall be assembled into an identifiable inspection lot or collection of inspection sublots. Each inspection lot shall be identified by a unique lot identification code (see 3.10.8).

E.3.1.1 JAN, JANTX, and JANTXV inspection lot. The total number of devices that the manufacturer submits at any one time for qualification or CI shall constitute an inspection lot. The maximum small inspection lot size shall be 2,500 devices. Small lot samples may not be used to satisfy group B or C requirements for large lots of structurally identical devices. Small lot samples may only be used to satisfy group B and C for the part number base lined. The inspection lot is submitted to determine compliance with the requirements of the performance specification sheets. Each inspection lot shall consist of devices of a single device type or consist of a collection of sublots of structurally identical devices contained on one or more performance specifications sheets (see E.3.2). Lot identification shall be maintained from the time the lot is assembled.

E.3.1.1.1 Inspection sublot. An inspection sublot shall consist of a single device type contained on a single performance specification sheet manufactured on the same production line(s) through final seal by the same fabrication technique and to the same device design with the same material requirements and within the same 6-week period.

E.3.1.2 JANS inspection lot.

E.3.1.2.1 Wafer lots. Wafer lots consist of semiconductor wafers formed into lots at the start of wafer fabrication for processing as a group. Each lot is assigned a unique identifier to provide traceability and maintain lot integrity throughout the fabrication process. The wafer lot shall be traceable to the silicon lot(s) or portion thereof. Wafer lot processing as a group is accomplished by any of the following procedures, providing process schedules and controls are sufficiently maintained to assure identical processing in accordance with process instructions of all wafers in the lot:

a. Batch processing of all wafers in the wafer lot through the same machine process steps simultaneously.

b. Continuous and sequential processing (wafer by wafer or batch portions of wafer lot) of all wafers through the same machine(s) or process steps. No other product, lots, equipment maintenance, repair or calibration shall interrupt continuous or sequential processing. Any deviation from this processing requires the written approval of the qualifying activity or a new wafer lot identifier will be assigned.

E.3.1.2.2 Scanning Electron Microscope (SEM) inspection. If any wafer lot is of a selected die design (such as overlay structure devices and devices with metallization path to bond pad crossing any junction covered by passivation or glassivation where the bonding pad is not on the same active area of the device), SEM inspection is required prior to acceptance of the wafer lot. This inspection shall be performed in accordance with MIL-STD-750, test method 2077, for each of these lots. If a contracted laboratory is used for the actual SEM inspection, the manufacturer shall document and define the responsibilities of the manufacturer and contractor regarding steps within test method 2077 that may be performed by either party, such as: Sample selection and sample preparation.

E.3.1.2.3 Device inspection lot. A JANS inspection lot shall consist of the total number of devices that the manufacturer submits at one time and which conforms to the following criteria:

a. Small lots shall not exceed 1,000 pieces. Sampling inspection for large or small lots shall be in accordance with table VIa, VIb, and VII.

b. All devices shall be of a single device type.

c. All devices shall be from a single wafer lot.

d. All devices shall be assembled on the same production line with the same technique from die attach through final seal, within 21 working days not to exceed 31 calendar days.

E.3.2 Structurally identical device types. Structurally identical device types are devices manufactured on the same production line(s) within the same plant through final seal, by the same fabrication technique within the same package family and to the same device design with the same material requirements and differ only electrically or by dimensional proportions. Examples of such structurally identical device types are as follows:

a. Rectifiers, diodes, or thyristors grouped into different voltage ratings. Rectifiers and diodes with identical design rules (same passivation and device structure) which differ only in die size and package size are considered structurally identical. Initially, group B and C shall be performed on each device construction. On subsequent lots, the die sizes/package styles which receive group B and C inspection shall be rotated on every lot thus assuring that all die/package styles receive groups B and C inspection.

b. Transistors grouped for gain limits and voltage ratings. Transistors (> 4 watts) with similar die structures that vary only in die size are considered structurally identical if the following criteria are met.

    1) Die must have the same generic design rules and vary only in size. Channel stop, voltage enhancement, and emitter ballasting techniques, epi-base, diffused base, expanded contacts and metal interconnects over oxide steps must be similar. The process sequence in the diffusion and photolithographic areas must be the same. Transistors must have similar peak frequency responses and V ratings that do not vary more than three to one (eg., 3 MHz to 9 MHz, 60 V dc to 180 V dc). Darlington transistors cannot be grouped with standard transistors.

    2) Overall construction must be the same. The number and size of wires can change as is needed to handle the power rating, but the die attach, wire attach and encapsulation method must be identical.

c. Power MOSFETs grouped for $r_{DS}(on)$ and voltage ratings. Power MOSFETs of the same voltage types with identical design rules (field termination and cell density) and which differ only in die size are considered structural identical. Initially, groups B and C shall be performed on the largest die size available within each structurally identical voltage grouping. The die sizes which receive groups B and C inspection shall be rotated on a periodic basis thus assuring that all die sizes receive groups B and C inspection.

E.3.3 Disposal of samples. Devices subjected to destructive tests or which fail any test shall not be shipped. Sample devices from lots which have passed CI and which have been subjected to mechanical or environmental tests specified in groups B and C inspection and not classified as destructive, may be shipped provided each of the devices subsequently passes group A, subgroup 2 inspection.

E.3.4 Destructive tests. Unless otherwise demonstrated, the following MIL-STD-750 tests are classified as destructive:

Method number	Test
1017	Neutron irradiation
1018	Internal water –vapor content
1019	Steady state total dose irradiation
1020	ESDS classification
1021	Moisture resistance
1036, 1037	Intermittent operation life
1041	Salt atmosphere
1042 (condition D)	Burn-in/life test for power MOSFETs
1046	Salt spray
1056	Thermal shock (glass strain)
1080	Single Event Gate Rupture and Drain Burn-Out Test
2017	Die shear test
2101	DPA procedures for diodes
2031	Soldering heat
2036	Terminal strength
2037	Post seal bond strength
2075	Decap internal visual design verification
2077	SEM
3478	Power transistor electrical dose rate test method

All other mechanical or environmental tests (other than those listed in E.3.5) shall be considered destructive initially, but may subsequently be considered nondestructive upon accumulation of sufficient evidence to indicate that the test is nondestructive. The accumulation of data from five repetitions of the specified test on the same sample of product, without significant evidence of cumulative degradation in any device in the sample, is considered sufficient evidence that the test is nondestructive for the device of that manufacturer. Any test specified as a 100 percent screen shall be considered nondestructive for the stress level and duration or number of cycles applied as a screen.

E.3.5 Nondestructive tests. Unless otherwise demonstrated, the following MIL-STD-750 tests are classified as nondestructive:

Method number	Test
1038, 1039, 1040	Burn-in screen
1042 (conditions A, B, and C)	Burn-in/life test for power MOSFETs
1051(100 cycles or less)	Thermal shock (temperature cycling)
1001	Barometric pressure
1022	Resistance to solvents
1026, 1027	Steady-state life
1031, 1032	High temperature life (non operating)
1048	Blocking Life
1071	Hermetic seal tests
2006	Constant acceleration
2016	Shock
2026	Solderability (If the original lead finish is unchanged and if the maximum allowable number of reworks is not exceeded.)
2052	PIND test
2056	Vibration, variable frequency
2066	Physical dimensions
2069, 2070, 2072, 2073, 2074	Internal visual (pre-cap)
2071	External visual
2076	Radiographic inspection
2081	Forward instability shock test (FIST)
2082	Backward instability shock test (BIST)
3101	Thermal impedance testing of diodes
3103	Thermal impedance measurements for IGBTs
3104	Thermal impedance measurements for GaAs
3051, 3052, 3053, 3474 (with limited supply voltage)	Safe operating area (SOA) (condition A for test method 3053)
3131	Thermal resistance (emitter to base forward voltage, emitter-only switching method)
3161	Thermal impedance measurements for vertical power MOSFET's (delta source-drain voltage method).
3181	Thermal resistance for thyristors
4066	Surge current
4081	Thermal resistance of lead mounted diode (forward voltage, switching method)

When the junction temperature exceeds the device maximum rated junction temperature for any operation or test (including electrical stress test), these tests shall be considered destructive except under transient surge or nonrepetitive fault conditions or approved accelerated screening when it may be desirable to allow the junction temperature to exceed the rated junction temperature. The feasibility shall be determined on a part by part basis and in the case where it is allowed adequate sample testing shall be performed to provide the proper reliability safeguards.

E.3.6 Resubmitted lots.

E.3.6.1 Resubmitted lots of JANS. Resubmitted lots shall be kept separate from new lots and shall be clearly identified. Any failed lot for group B and group C may be resubmitted one time only, for the failed subgroup, at double the large lot sample size with zero failures if it is determined by analysis of all the failed devices, that the failure mechanism is due to a defect that can be effectively removed by rescreening the entire lot, and that rescreening has been performed. Failure analysis shall be performed on all failed lots. Lots which fail group B, bond strength, decap internal visual and SEM (when applicable) shall not be resubmitted. For group A, E.3.6.2 shall apply.

E.3.6.2 Resubmitted lots of JANTXV, JANTX, and JAN. Resubmitted lots shall be kept separate from new lots and shall be clearly identified. When any lot submitted for qualification or CI fails any applicable subgroup requirement of groups A (for A-2, A-3, and A-4, see footnote 2 of table V), B, C, or E tests it may be resubmitted once, after an analysis (discrepancy report required), for that particular subgroup at double the large lot sample size with zero failures. A second resubmission, using double the large lot sample size with zero failures, may only be performed if it is determined by analysis of all the failed devices, that the failure mechanism is due to a defect that can be effectively removed by rescreening the entire lot, and that rescreening has been performed.

E.3.6.3 Resubmitted lots of RHA devices. A JANTXV lot which fails group D tests may be resubmitted once, in accordance with note 4 or 7, as applicable, of table VIII. A JANS lot which fails group D, subgroups 1 or 3 tests, may be re submitted once, in accordance with footnote 3 of table VIII. JANS wafers which fail group D, subgroup 2 tests shall not be resubmitted. In lieu of resubmission , a lot or wafer which fails group D testing may be used as a non-RHA device or may be certified at a lower RHA level if the group D data indicates the lot or wafer meets the lower level requirements.

E.3.7 Conditions and methods of test. Conditions and methods of test shall be in accordance with MIL-STD-750. The general requirements of MIL-STD-750 apply as specified. A system for control and calibration of test equipment shall be established. ANSI/NCSL Z540-1-1994 may be used as guidance for the calibration system.

E.3.7.1 Alternative test methods. Other test methods or circuits may be substituted for those specified in MIL-STD-750 provided it is demonstrated to and approved by the qualifying activity that such a substitution in no way relaxes the requirements of this specification. The schematic wiring diagram of the test equipment shall be made available for review by the qualifying activity.

E.3.7.2 Procedure in case of test equipment failure or human error. If it is determined through an engineering evaluation that a failed device is the result of test equipment failure or human error, a replacement device from the same inspection lot may be added to the sample. The replacement device shall be subjected to all those tests to which the discarded device was subjected prior to its failure and to any remaining specified tests to which the discarded device was not subjected prior to its failure. Failures occurring as a result of operator error, prior to the start of testing, may be replaced by the manufacturer but shall be noted on the lot history. Any ESD failures shall be counted as rejects and not be attributed to equipment/operator error for screening, group A, and end-point electrical tests of MIL-STD-750.

E.3.7.2.1 PIND test equipment failure or error. If it is determined through an engineering evaluation and traceable through the manufacturer's quality system, that PIND rejects are the result of equipment failure or human error, then all devices (passed and rejected) subsequent to the equipment failure or human error, may be restarted. The devices shall be restarted at the run in which it was determined the equipment failed or the human error occurred.

E.3.7.3 Standard mixer diodes and holders. The manufacturer of UHF and microwave mixer diodes shall establish and maintain standard mixer diodes and standard mixer holders for use in qualification and quality conformance testing of UHF and microwave mixer diodes. These standards shall be calibrated at least once in each successive 12-month period or prior to use if over 12 months, at a laboratory acceptable to the Government.

E.3.8 JANS electrical test data. Unless otherwise specified in the performance specification sheet, all electrical measurements performed on devices after screen 8 shall be recorded.

E.3.8.1 Summary of parts fallout. A summary of the JANS parts fallout during screening tests shall be prepared by the manufacturer in accordance with the requirements of the qualifying activity

E.3.9 Preservation of lot identity. During all screening, inspection, and marking operations, each lot, and sublot shall be kept segregated, secure, and traceable.

E.4 QUALIFICATION

E.4.1 Qualification inspection. Qualification inspection shall be performed at a facility approved by the qualifying activity and shall be conducted in accordance with the procedures described herein for group A, B, C, D, and E inspection and by the qualifying activity. Qualification of a particular device type to a given quality level may be extended by the qualifying activity to any other quality level provided all the groups A, B, C, D, and E requirements of the other level have been met and provided that suitable approved screening facilities are available for the other tests and stress levels. In addition, the requirements of appendix H shall be met. Small lot sampling shall not be used for qualification inspection.

Group D is required for each inspection lot of RHA types as specified in the performance specification sheet. Qualification for RHA shall be for a specific semiconductor die.

An alternate qualification procedure for RHA devices for levels M, L, and D only, are available for devices with demonstrated RHA. These devices must be submitted for qualification inspection and CI, if process or design changes affecting RHA are made.

E.4.2 Inspection routine. All samples subjected to groups B, C, D, and E must have been chosen from a lot which has passed the requirements for group A except as modified in E.6.5. The following conditions apply:

a. The required sample plan for series of devices shall consist of group A inspection for the highest and the lowest voltage types or as the qualifying activity requires.

b. A sample from one sublot shall be tested for each group B subgroup. A sample device from each sublot (each device type) shall be submitted to the design verification examination.

c. A sample from one sublot shall be tested for each group C subgroup. At the option of the manufacturer, devices from group B, tables VIa and VIb, may be continued on in group C, subgroup 6, to achieve 1,000 hours or 6,000 cycles total, or separate samples may be used.

d. When group D (RHA) qualification extension is granted, the radiation facility shall be approved by the qualifying activity. A sample from a sublot of each device type shall be tested for each group D subgroup.

e. Devices which are constructed using braided leads may be processed through table IV screening and qualification high temperature testing prior to the addition of leads. Qualification testing requiring load current conduction will require that leads be attached.

E.4.2.1 Qualification to ESDS classes. Initial qualification to an ESDS class or requalification after redesign shall consist of qualification to the appropriate quality and reliability level plus ESDS classification in accordance with test method 1020 of MIL-STD-750.

ESDS classification levels are defined as follows:

ESDS class designator	Prior designation category	Marking	Electrostatic voltage
1	A	Δ	0 - 1,999 V
2	B	$\Delta\Delta$	2,000 - 3,999 V
3			4,000 - 15,999 V
Non sensitive			> 15,999 V

a. Although little variation due to case outline is expected, if a device type is available in more than one package type or case outline, ESDS testing and classification shall be applied to at least that one package type shown by experience to be worst case for ESDS. ESDS classification test results shall be submitted to the qualifying activity for all performance specification sheets for listing. Specifications using structurally identical die designs may be classified with data from previously classified types. Any dissimilar designs within a performance specification sheet shall have ESDS classifications for each structurally identical grouping.

b. All power bi-polar transistors and rectifiers except schottkys are considered to be at least class 3 by design. Schottky case mounted rectifiers may be designated class 3, upon successful completion of a 2 ampere reverse energy test. Other schottky rectifier package configurations may be designated class 3, if they pass a reverse energy test which has been demonstrated to correlate with class 3 classification.

c. All zeners, (voltage reference and voltage regulators) and transient suppressors are considered non-sensitive by design.

E.4.2.1.1 ESDS. ESDS classification testing shall be done in accordance with test method 1020 of MIL-STD-750 and the applicable performance specification sheet (see 3.10.3.1). Devices shall be handled in accordance with the manufacturer's in-house control documentation. Devices that are classified class 3 or non-sensitive, are not required to be handled as ESD sensitive, and manufacturer's in-house control documentation plan is not required. Handling shall begin at lead clip or wire bond (e.g., for packages which do not have a lead shorting bar or do not have leads shorted together). Guidance for device handling is available in the EIA-625 document.

E.4.2.2 Qualification by extension. Qualification of a structurally identical device, a series of devices from the same or different performance specification sheets, or qualification of a new package for a previously qualified die may be extended from a previously fully qualified device provided the following information and data are supplied to the qualifying activity:

a. Previously qualified device type, performance specification sheet number, and qualification reference number.

b. Design and construction information on devices covered under different performance specification sheets.

c. Samples of structurally identical devices with certification that these samples are structurally identical to the previously qualified device.

d. Group A variables data on a sample plan of each structurally identical device type except for series of devices which shall be the sample plan of the highest and the lowest voltage types or as the qualifying activity requires, or as specified in performance specification sheets covering groups of devices. Test samples of selected devices in a group or portion of a group shall be from the same inspection lot.

e. Results and variables data for each structurally identical device on all group B and C electrical tests not specified in group A, including tests at temperature extremes.

f. All results and variables data on group B and C tests as follows:

    1) Data on any tests not required by the qualified device.

    2) Data that is the result of tests performed at stress levels greater than those required for the qualified device.

    3) Data for any tests requiring more exacting limits than those found for the qualified device.

g. Items E.4.2.2d through E.4.2.2f shall not be required if the qualifying activity can be assured that the previously fully qualified device at least meets all of the conditions and requirements for the proposed structurally identical device type, except for device type marking.

Qualification by extension does not necessarily imply conformance inspection coverage to all device types covered by the qualification by extension approval.

E.4.3 End points. End-point electrical measurements shall be measured and recorded as applicable (e.g., if delta's are required) starting and after completion of all specified tests in the subgroups of groups B, C, and D. Pre-test end point failures shall be replaced by acceptable devices.

E.4.4 Selection of samples. All samples shall be randomly selected from the qualification inspection lot. Sample selection for group D testing shall be in accordance with table VIII and shall be from each wafer or from each inspection lot, as appropriate.

E.4.5 Identification of samples. The manufacturer's management representative may, at his option, mark or authorize the marking of each sample to be subjected to qualification testing in order to distinguish these devices from those not intended for qualification inspection.

E.4.6 Qualification inspection lot release. The inspection lot from which the qualification samples are selected may be offered for delivery under contract after qualification approval has been granted provided screening and conformance inspection requirements are satisfied.

E.5 SCREENING

E.5.1 Screening. All JANS, JANTXV, and JANTX semiconductor devices (100 percent) shall have been subjected to and passed, all the applicable screening tests (as specified in table IV) in the sequence shown and the applicable percent defective allowed (PDA) for the type of semiconductor and quality level (device class) specified. Devices which fail any test criteria in the screening flow, shall be identified and controlled until removal from the lot. At the option of the manufacturer, the rejects may continue processing. The lot records shall identify the point of failure and the actual percent defective (PD) (as applicable). Any rejected devices shall be removed from the lot prior to shipment. Except for JANS, the conditioning and screening tests performed as standard production tests need not be repeated when these are predesignated and acceptable to the qualifying activity as being equal to or more severe than specified herein provided the relative process conditioning sequence is maintained. All tests, preconditioning and screening operations which were performed on the devices submitted for qualification inspections specified herein shall be performed on all devices subsequently submitted for CI (see E.6.).

E.5.2 Percent Defective Allowable (PDA). Selected electrical parameters shall be designated in the performance specification sheet for screen 11 and 13 which shall be used for the PDA calculation. These parameters may also be compared to determine whether the change during burn-in (delta) is indicative of a lot stability problem. All burn-in pre-conditioning failures, either HTRB or power burn-in, shall be counted towards the applicable PD unless the pre-conditioning is part of the manufacturer's standard flow.

E.5.2.1 JANTX and JANTXV PDA. The PDA for each inspection lot (or screening lot if the alternate flow is used) shall be 10 percent (for each burn-in) on all failures for the specified electrical parameters in steps 11 and 13a. Delta limits shall be defined in the performance specification sheets. For delta limits, the delta parameter values measured after burn-in (100 percent screening test) shall be compared with delta parameter values measured prior to that burn-in. Unless otherwise specified, inspection lots which exceed the 10 percent PDA may be resubmitted one time only to the burn-in operation failed. The PDA shall be 3 percent on the resubmitted inspection lot to each failed burn-in. If the combined burn-in PD's for the first submission exceeds 20 percent or either of the resubmitted burn-in exceed the 3 percent PDA, the entire lot shall be unacceptable for any quality level.

E.5.2.2 JANS PDA**.** The PDA for each inspection lot shall be 5 percent (for each burn-in) on all failures for specified electrical parameters in steps 11 and 13a. Delta limits shall be defined in the performance specification sheets. For PDA delta limits, the delta parameter values measured after burn-in (100 percent screening test) shall be compared with delta parameter values measured prior to that burn-in. Unless otherwise specified, inspection lots which exceed the 5 percent PDA may be resubmitted one time only to the burn-in operation failed. The PDA shall be 3 percent on the resubmitted inspection lot to each failed burn-in. If the combined burn-in PD for the first submission exceeds 10 percent or either of the resubmitted burn-in exceed the 3 percent PDA, the entire inspection lot shall be unacceptable for any quality level.

E.5.3 JANTX and JANTXV product. The procedure for testing and screening for JANTXV and JANTX devices shall be in accordance with tables IV, V, VIb, VII, figure 3, and as specified in the applicable performance specification sheet.

E.5.3.1 Alternate procedure for screening of JANTX and JANTXV types. JAN types may be processed and marked as JANTX and JANTXV types by the original part manufacturer on his own qualified product provided the following procedures are satisfied:

a. All devices to be proposed for JANTXV processing (except clear glass JANTXV diodes which shall be subjected to internal visual inspection before printing or marking) must have been subjected to and passed JANTXV internal visual 100 percent screening prior to seal.

b. Groups A, B, and C inspection shall have met the JANTX and JANTXV level requirements in accordance with tables V, VIb, VII , figure 4, and the applicable performance specification sheet.

c. Screening shall be conducted in accordance with table IV, figure 4, and the applicable performance specification sheet. All units failing these tests shall be removed from the lot and the quantity removed shall be noted in the lot history.

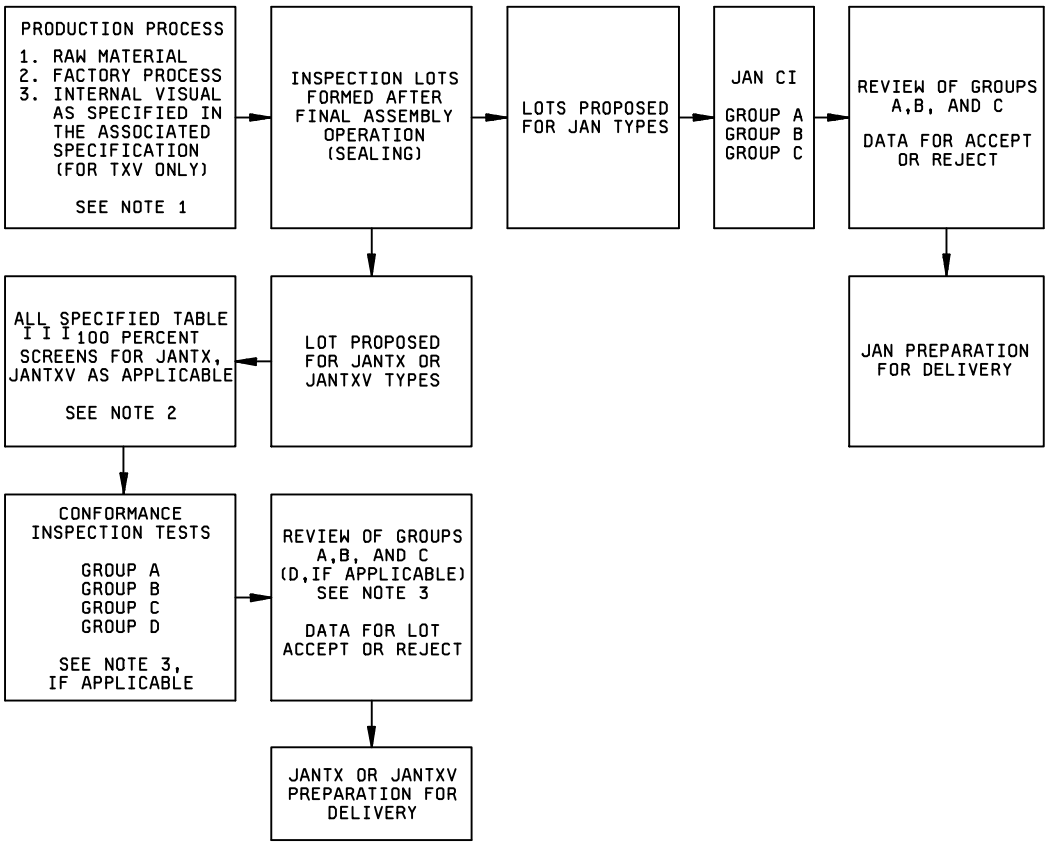
d. A sample of the screened devices shall be submitted to and pass the requirements of group A-1 and A-2 inspection (see table V and B-1) (see table VIb, subgroup 1) subsequent to the 100 percent screening (of the lot or separate portions thereof) as specified in E.5.3.1c and as shown on figure 4.

E.5.3.2 Bin and cell pre and post burn-in electrical measurements. Alternate methods to variables recording may be used to determine delta end point requirements of JANTX and JANTXV burn-in provided the qualifying activity has granted written approval. When alternate methods to variables recording are used to determine delta end point requirements, devices shall be separated into groups, each of which shall have maximum and minimum limits on the variable parameter(s). The difference in parameter limits for any group shall not exceed the delta requirements for the variable parameter(s).

E.5.3.3 Alternate procedures for qualification and CI where JAN is not covered by the performance specification sheet. When the JAN quality level is not included in the performance specification sheet, or at the option of the manufacturer, the alternate flow (see figure 4) may be used for qualification and CI. The lot used shall be marked in accordance with 3.10.1, except the "JAN" designating symbol shall be replaced by "JANQ". Unless they are submitted to the flow that the lot was submitted to, these samples shall not be shipped.

E.5.3.5 Lead forming for JANTX and JANTXV. When lead forming is specified, it shall be followed by n = 116, c = 0 fine and gross seal tests, group A, subgroup 2, and external visual examination n = 45, c = 0.

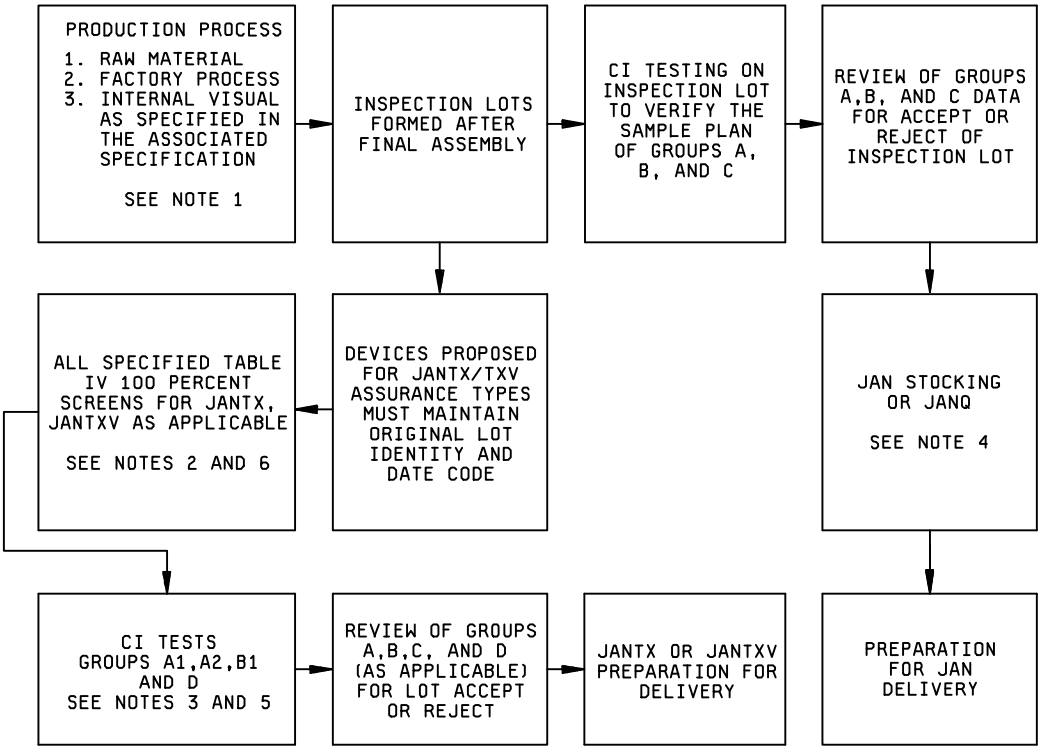
E.5.4 JANS product. The procedure for testing and screening of JANS devices shall be in accordance with tables, IV,V, VIa, VII, figure 5, and the applicable performance specification sheet.



NOTES:

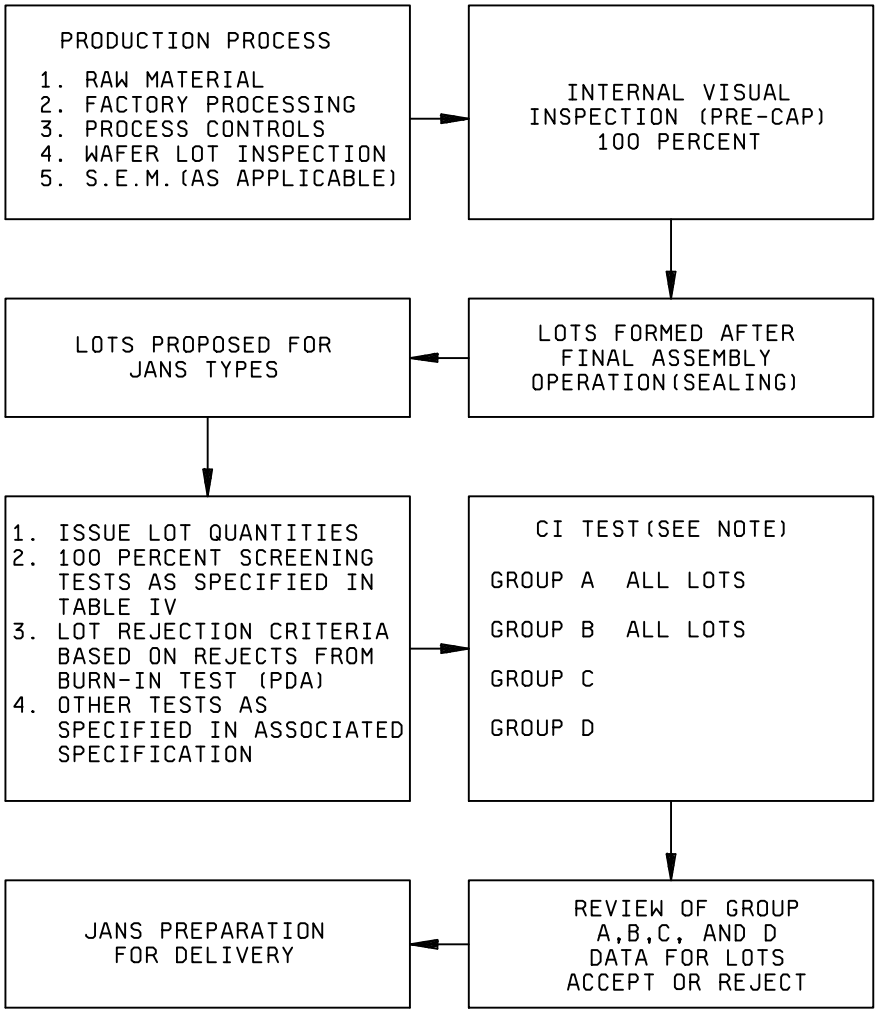
1. All products to be proposed for JANTXV processing must have been subjected to and passed JANTXV internal visual 100 percent screening at this step (except for clear glass JANTXV diodes which shall be subjected to internal visual inspection prior to painting and marking).
2. Order of the tests shall be performed as specified in table IV.
3. Group D inspection may be performed at any point prior to lot formation.

FIGURE 3. Order of procedure diagram for JAN, JANTX, and JANTXV device types.



NOTES:
1. All product proposed for JANTXV processing must have been subjected to and passed JANTXV internal visual 100 percent screening in accordance with table IV herein at this step (except for clear glass JANTXV diodes which shall be subjected to internal visual prior to body paint or mark).
2. The order of all screening tests shall be performed as specified in table IV.
3. B1 may be performed simultaneously with A. Steam age is not required for solderability testing at this step only.
4. JANQ product must be screened and receive the appropriate CI testing prior to shipping (see E.5.3.3).
5. If a JAN inspection lot is not processed in parallel with the material designated for JANTX and JANTXV, all group A, B, C, and D testing must be performed on a JANTX or JANTXV inspection lot.

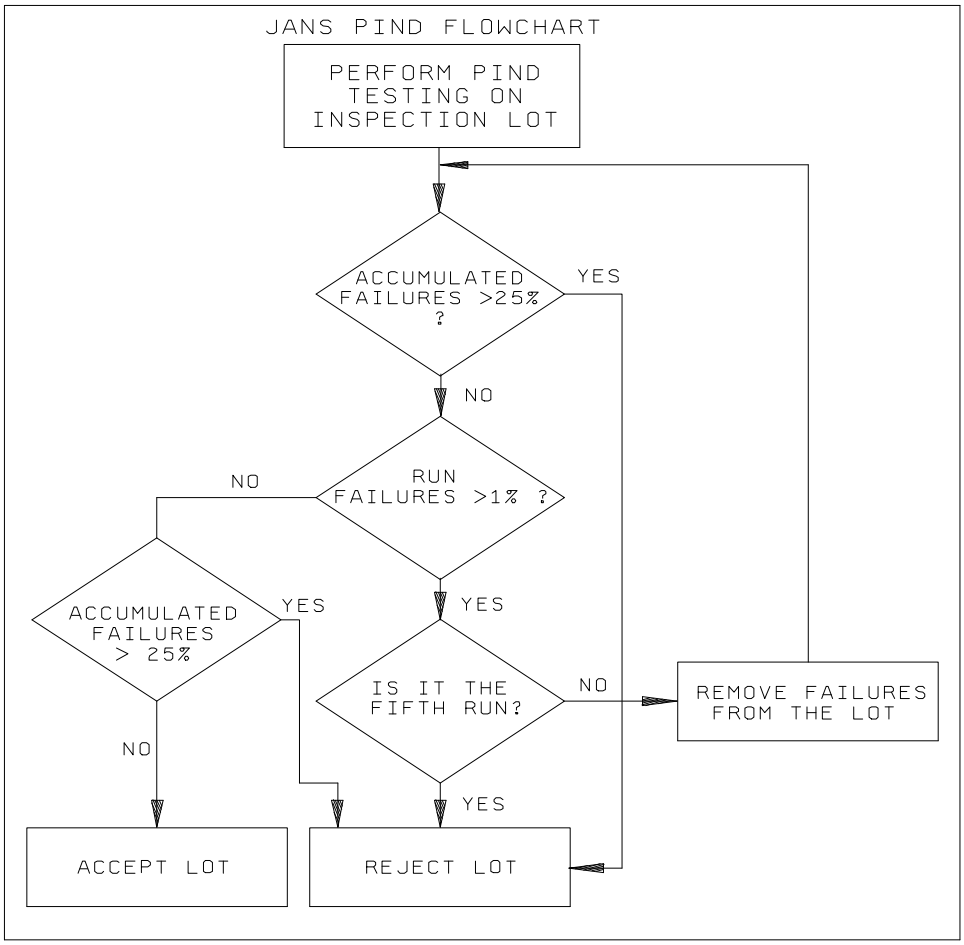
FIGURE 4. Alternate order of procedure diagram for JAN, JANTX, and JANTXV device types.



NOTES:
1. Group D testing may be performed at any point following the production process (see E.6.5).

FIGURE 5. Order of procedure diagram for JANS.

E.5.4.1 PIND test for JANS devices. The inspection lot (or sublots) shall be submitted to 100 percent PIND testing a maximum of five times in accordance with test method 2052 of MIL-STD-750, test condition A. PIND prescreening shall not be performed. The lot may be accepted on any of the five runs if the percentage of defective devices is less than one percent (zero failures allowed for lots of less than 50 devices). All defective devices shall be removed after each run. Lots which do not meet the one percent PDA on the fifth run, or exceed 25 percent defectives cumulative, shall be rejected and resubmission is not allowed. These parts shall not be shipped as any other quality level. When calculating numbers of allowed failures using percentages, fractional values shall be increased to the next whole integer.



E.5.4.2 Lead forming for JANS. When lead forming is performed on JANS devices, it shall be followed by screen 7, group A, subgroup 2, and external visual examination on 100 percent of the lot.

E.5.4.3 Burn-in socket verification for JANS. The electrical continuity between each device and the socket shall be verified prior to initiating burn-in (see MIL-STD-750 for details).

E.5.5 Failure evaluation for JANS. Failures that occur during JANS screening shall be evaluated to determine if failure mode is the result of a latent (time dependent) defect, workmanship, or design weakness. This information shall be retained and presented to the qualifying activity, when requested, for review and determination if a failure trend is developing that needs corrective action. The manufacturer's procedure (s) shall define when a formal failure analysis is required to be performed.

APPENDIX E

E.6 CONFORMANCE INSPECTION (CI)

E.6.1 CI. CI shall be conducted in accordance with the requirements of groups A, B, and C for the specified quality level as well as group D to the applicable RHA level. If a lot is withdrawn in a state of failing to meet conformance requirements and is not resubmitted, it shall be considered a failed lot and reported as such. Each lot shall be subjected to group A and B inspection. Successful completion of group C conformance for a given quality level shall satisfy the group C requirements for all quality levels and devices represented by the structurally identical group. The grouping of structurally identical devices shall be as agreed between the manufacturer and the qualifying activity. JANS devices shall not be used to represent the other quality levels. If a manufacturer elects to eliminate all or any CI step substituting either a process monitor or SPC procedures (when approved by the preparing activity and qualifying activity), the manufacturer is only relieved of the responsibility of performing the CI (see 4.4). The manufacturer still bears full liability for any failure that may result if these tests are performed at a later time. A manufacturers reliability program may be used in lieu of all or any CI when equivalent to or compliant with C.8.4.

TABLE I. Sample plans.

Maximum percent defective or lambda	50	30	20	15	10	7	5	3	2
Accept Number (c) (r=c+1)	Minimum sample sizes (For device-hours required for life test, multiply by 1,000)								
0	5	8	11	15	22	32	45	76	116
1	8	13	18	25	38	55	77	129	195

E.6.1.1 Nonconformance. Lots which fail subgroup requirements of group A, B, C or D may be resubmitted in accordance with the provisions of E.3.6. However, if the lot is not resubmitted or fails resubmission, the lot shall not be shipped and the JAN marking shall be obliterated or removed within 30 days. For additional, guidance on Group D failures see E.6.5.

E.6.2 Group A inspection. Group A inspection shall be performed on each inspection lot and shall consist of visual and mechanical inspection and electrical tests as specified in table V and the performance specification sheet. Group A inspection may be performed in any order. If an inspection lot is made up of a collection of sublots, each sublot shall pass group A inspection as specified. Unless the entire inspection lot has seen the same screening, devices which have received PIND (one pass condition A) may not be considered as candidates for this inspection.

E.6.3 Group B inspection. Group B inspection shall be performed on each inspection lot. Group B shall be in accordance with table VIa or VIb as applicable, and the performance specification sheet. Testing of one device type sublot in any subgroup shall be considered as complying with the requirements for that subgroup for all types in the lot. Different device types may be used for each subgroup except for JANS. All inspections except for life tests shall be applied only to completed and fully marked devices from lots which have been subjected to and passed the group A, subgroup 1,2, and 3 requirements. When the final lead finish is solder, or any plating prone to oxidation at high temperature, the samples for life tests (groups B3 and B6 for JX and JV, and groups B4 and B5 for JANS) may be pulled prior to the application of final lead finish. Tests within a subgroup shall be performed in the order specified. The test samples may be cleaned prior to the electrical end-point testing. An evaluation shall be performed on all failures to determine if the failure mode is the result of a latent (time dependent) defect, workmanship, or design weakness. Appropriate corrective action shall be performed as a result of the evaluation. All tests within a subgroup shall be performed in the order specified except table VIa, subgroup 2, and table VIb, subgroup 1.

E.6.3.1 Lots shipped prior to group B completion. No lots shall be shipped prior to completion of group B without the approval of the qualifying activity. This provision is only to be requested for emergency procurement situations and it is expected that the user will provide a justification.

E.6.4 Group C inspection. Group C inspection shall be in accordance with table VII and shall include those tests specified which are performed periodically at 1 year intervals on at least one device type from each structurally identical device grouping (from the same or different performance specification sheet) in which the manufacturer has qualified device types. This inspection shall be applied only to completed and fully marked devices from lots which have been subjected to and passed the group A, subgroup 1,2, and 3 requirements. When the final lead finish is solder, the life test subgroup may be pulled prior to the application of final lead finish. All tests within a subgroup shall be performed in the order specified. The test samples may be cleaned prior to the electrical end-point testing. An evaluation shall be performed on all failures to determine if the failure mode is the result of a latent (time dependent) defect, workmanship, or design weakness. Appropriate corrective action shall be performed as a result of the evaluation. Lots with an unscreenable failure mode shall be rejected. Unless all devices intended for manufacturing during that period will receive as a minimum the same screening, devices which have received PIND screening in accordance with E.5.4.1 may not be used to qualify the next group C inspection periods. A device type which fails a group C inspection shall not be accepted until the device type which failed, successfully completes the failed group C subgroup(s). Other device types from the same qualified group represented by the failed device type may be accepted provided group C inspection requirements have been satisfied for those device types.

Samples from subsequent lots of the device types in the structurally identical device grouping which failed group C inspection, shall then be subjected to all the tests in the subgroup in which the failure occurred, on a lot-by-lot basis until three successive lots pass the failed subgroup. The testing may then return to periodic testing.

E.6.4.1 Group C sample selection. Samples for subgroups in group C shall be chosen at random from the first lot submitted for CI during the specified group C inspection interval. Testing of one device type for each subgroup shall be considered as complying with the requirements for that subgroup for all structurally identical types (see E.3.2). A different device type(s) shall be tested at each successive inspection interval until all structurally identical device types qualified on the same or different performance specification sheets from the same qualified line have been tested, except power MOSFETs grouped by the same voltage as described in E.3.2. When none of the inspection lots passing group A of the first lot submitted contain the device type which is due to be tested, the samples for inspection shall be chosen from those types in the inspection lots being tested which have not been used for the longest time for group C inspection. The date code of the lot establishes (begins) the one year group C interval. Groups A and B shall also be completed on the group C inspection lot date code prior to the coverage being valid.

E.6.4.2 Lots shipped prior to group C completion. No lots shall be shipped prior to completion of group C without the approval of the qualifying activity. This provision is only to be requested for emergency procurement situations and it is expected that the user will provide a justification

E.6.5 Group D inspection. Group D inspection shall be performed in accordance with table VIII and the requirements of the performance specification sheet. Group D may be completed any time in the lot history (e.g., prior to lot formation, or before screening). Group D sample devices shall be assembled in it's qualified package or in any qualified package that the manufacturer has data to correlate the performance to the designated package and as a minimum, pass group A, subgroup 2 prior to irradiation. A sample which fails group D may be resubmitted once, in accordance with E.3.6.3. In lieu of resubmission, a lot or wafer which fails group D testing may be used as a non-RHA devices or may be certified at a lower RHA level if the group D data indicates the lot or wafer meets the lower level requirements.

E.6.6 Group E inspection. Group E is a workmanship, ruggedness, and critical interface verification inspection. Group E testing, when specified on the performance specification sheet is required for initial qualification, re-qualification, and when device requirements are changed. The results of group E testing shall be submitted to the qualifying activity (by all manufacturers prior to shipment of product, as applicable). Product redesigns may be subjected to group E testing as required by the qualifying activity.

E.6.6.1 Group E testing requirements. Group E shall be performed in accordance with table IX herein and the performance specification sheet. All tests within a subgroup shall be performed in the order specified. An evaluation shall be performed on all failures to determine if the failure mode is the result of a latent (time dependent) defect, workmanship, or design weakness. Appropriate corrective action shall be performed and approved by the qualifying activity.

E.6.6.2 Alternate group E testing procedures. Manufacturers may use internal design verification or ongoing reliability assessment programs in lieu of group E, subgroups 1 and 2 only, provided this testing is equivalent to or more stressful than group E and is performed using the same design and construction on file at the qualifying activity. This alternate testing must be approved by the preparing activity and the qualifying activity.

E.6.7 Group B, C, D, and E end points. Post test end points specified in the performance specification sheet shall be measured for each device of the sample after completion of all specified tests in the subgroups. Except as specified or otherwise required, all life test (such as operation, storage, blocking) end point measurements shall be performed within 96 hours after sample units have been subjected to and removed from required tests. All other end-point test measurements shall be made within 168 hours, or as specified. Additional measurements may be made at the discretion of the manufacturer. If endpoint measurements can not be performed within the specified time refer to the applicable MIL-STD-750 test method for the procedure to follow.

APPENDIX E

TABLE II. RHA levels and requirements. 1/ 4/

Radiation level		
RHA designation	Total ionizing dose (RAD(Si)) 2/	Neutron fluence (N/Cm^2) 3/
M	3×10^3	
D	1×10^4	
L	5×10^4	
R	1×10^5	
F	3×10^5	
G	6×10^5	
H	1×10^6	

1/ See 4.3. and E.6.5
2/ Test in accordance with MIL-STD-750, test method 1019.
3/ Test in accordance with MIL-STD-750, test method 1017. Unless otherwise specified in the performance specification sheet, the minimum neutron fluence shall be 2×10^{12} N/cm^2.
4/ The highest level may be qualified without qualifying any lower level.

TABLE III. Testing guidelines for changes to a qualified product. 1/ 2/ 3/ 4/ 5/ 6/ 7/

Changes (see D.3.4.2)		Testing, MIL-STD-750, (All electrical parameters as specified in performance specification sheets)	Samples to be submitted to qualifying activity
a.	Doping material source Concentration Process technique	Groups A and C-6 deltas (variables only when deltas are required)	C-6 (2 samples)
b.	Die structure/topography	Same as a.	B-2 (2 samples)
c.	Mask changes affecting die size or active element Wafer diameter Final die thickness	Variable groups A, B-2, and C6, if new die area is smaller/ larger in the applicable package than previously qualified Groups A and C-6 Groups B-2 and B-4	 C-6 (2 samples) B-2 (2 samples)
d.	Passivation/glassivation or die coating	Groups A and C-6	C-6 (2 samples)
e.	Metallization changes.	Groups A, B-2, B-4, and C-6	B-2 (2 samples)
f.	Die attach method	B-2 and C-3	C-3 (2 samples)
g.	Bond process	B-4 and C-3	C-3 (2 samples)
h.	Bond wire material, doping dimensions	B-4 and C-3	C-3 (2 samples)
i.	Package or lid structure Package or lid material Package or lid dimension	B-1, B-2, and C-3 B-1, B-2, and C-3 B-1, B-2, and C-3	C-3 (2 samples) C-3 (2 samples) C-3 (2 samples)
j.	Sealing technique	B-1, B-2, and C-3	C -3 (2 samples)
k.	Sealing environment	B-1, B-2, and C-3	C-3 (2 samples)
l.	Implementation of test methods	Notify qualifying activity (may involve test demonstration)	As required
m	Changes in flow chart	Same as l.	As required.
n.	Fab move	Conformance inspection test report attributes data) group A (read and record)	One test sample each subgroup (B and C)
o.	Assembly move	Same as l	Same as l
p.	Test facility move	Notify qualifying activity	As required.
q.	Scribe/die separation	B-2 and C-3	B-2 (2 samples)
r.	Qualification/CI procedures	Notify qualifying activity	As required.

1/ Acceptable supporting data may be submitted to reduce or eliminate required testing.
2/ When variable data is required for applicable groups A and C testing, data histograms providing acceptable parameter data summaries may be submitted in place of variables.
3/ If changes involve more than one device type from the same certified line, contact the qualifying activity to determine appropriate selection of device type(s) to be selected for testing.
4/ The qualifying activity may add or reduce testing if warranted by performance specification sheet requirements or unique design or process circumstances after notification of the manufacturer.
5/ All groups and subgroups referenced herein apply to JANTX and JANTXV only. Test requirements for sample submittals for design changes to JANS level qualified product are to be determined by the qualifying activity.
6/ Additional testing and evaluation in accordance with group E to establish confidence in the proposed change shall be performed as required by the qualifying activity (see E.6.1.6).
7/ New die design requires full qualification.

APPENDIX E

TABLE IV. Screening requirements.

Screen	MIL-STD-750 method	Condition	JANS requirements	JANTXV requirements	JANTX requirements
1a. Die visual for diodes	2073	Die form prior to assembly	100 percent	When specified	Not applicable
1b. Internal visual (pre-cap) inspection			100 percent	100 percent	Not applicable
For diodes	2074 1/				
For POWERFETs	2069				
For microwave transistors	2070				
For transistors	2072				
2. High temperature life Nonoperating life (stabilization bake)	1032	T_{STG} ≤ maximum rated storage temperature t = as specified	Optional	Optional	Optional
3a. Temperature cycling	1051	No dwell time is required at +25°C. Test condition C, or maximum storage temperature, whichever is less, 20 cycles	100 percent	100 percent	100 percent
3b. Surge (as specified) 2/	4066	Condition A or B, as specified	100 percent	100 percent	100 percent
3c. Thermal .impedance 2/ (as specified)		As specified	100 percent	100 percent	100 percent
Transistors,					
POWERFETs	3161				
Bipolar	3131				
Diodes	3101				
IGBT	3103				
GaAs FET	3104				
4. Constant acceleration. Not required for stud devices and metallugically bonded diodes.	2006	Y_1 direction at 20,000 G minimum except at 10,000 G minimum for devices with power rating of ≥10 watts at T_C = +25°C. The 1 minute hold time requirement shall not apply.	100 percent	Optional 3/	Optional 3/

See footnotes at end of table.

TABLE IV. Screening requirements - Continued.

Screen	MIL-STD-750 method	Condition	JANS requirements	JANTXV requirements	JANTX requirements
5. PIND 4/	2052	Condition A	100 percent see E.5.4.1	Not applicable	Not applicable
6. Instability shock test (axial lead diodes only) 5/					
a. FIST	2081		100 percent		
b. BIST	2082		100 percent		
7. Hermetic seal 6/					
a. Fine	1071	Omit for double plug diodes. Test condition G or H, maximum leak rate = 5 x 10^{-8} atm cc/s except 5 x 10^{-7} atm cc/s for devices with internal cavity > 0.3 cc. Maximum leak rate = 5 x 10^{-6} atm cc/s for cavities 3-40 cc. For clear glass noncavity diodes, utilize condition E	Optional 12/	100 percent 7/	100 percent 7/
b. Gross				100 percent 7/	100 percent 7/
8. Serialization		See 3.10.9.	100 percent	Not applicable	Not applicable
9. Interim electrical parameters		As specified	100 percent (Read and record)	For case mounted rectifiers as specified.	For case mounted rectifiers as specified.
10. High temperature reverse bias (HTRB)					
a. For transistors	1039	Test condition A. 80 percent (minimum) of rated V_{CB} (bipolar), V_{GS}(FET) or V_{DS}(FET), as applicable.	100 percent	100 percent	100 percent

See footnotes at end of table.

TABLE IV. Screening requirements - Continued.

Screen	MIL-STD-750 method	Condition	JANS requirements	JANTXV requirements	JANTX requirements
10. High temperature reverse bias (HTRB) - Continued					
b. For POWER FETs	1042	Test condition B. 80 percent (minimum) of rated V_{GS}	100 percent	100 percent	100 percent
c. For diodes and rectifiers	1038	Test condition A. Diodes (not required for LEDs, zeners, and case mounted rectifiers) 80 percent minimum of rated V_R or V_{RWM} when dc conditions are specified. 95 - 100 percent of V_{RWM}, when half sine condition is specified.	100 percent 9/	100 percent	100 percent
11. Interim electrical and delta parameter for PDA (see E.5.2)		As specified but including all delta parameters as a minimum. When HTRB is performed leakage current shall be measured on each device before any other specified parametric test is made.	100 percent (Measure all specified parameters. Measure leakage current within 16 hours after removal of applied voltage in HTRB. Record those parameters which have a delta limit.) (See screen 13.)	100 percent (Measure all specified parameters. Measure leakage current within 24 hours after removal of applied voltage in HTRB. Record those parameters which have a delta limit.) (See screen 13.)	100 percent (Measure all specified parameters. Measure leakage current within 24 hours after removal of applied voltage in HTRB. Record those parameters which have a delta limit.) (See screen 13.)
12. Burn-in		As specified.	100 percent	100 percent	100 percent
a. For bipolar transistors	1039	Test condition B.	240 hours (minimum)	160 hours (minimum)	160 hours (minimum)
b. For POWERFETs	1042	Test condition A.	240 hours (minimum)	160 hours 8/ (minimum)	160 hours 8/ (minimum)

See footnotes at end of table.

TABLE IV. Screening requirements - Continued.

Screen	MIL-STD-750 method	Condition	JANS requirements	JANTXV requirements	JANTX requirements
12. Burn-in - Continued		As specified.	100 percent	100 percent	100 percent
c. For diodes, zeners, and rectifiers	1038	Test condition B.	240 hours / (minimum)	96 hours (minimum)	96 hours (minimum)
For case mount rectifiers		Condition A, JANTX and JANTXV only.	Not applicable	48 hours (minimum)	48 hours (minimum)
		Condition B, for JANS	240 hours (minimum)	Not applicable	Not applicable
d. For thyristors 10/	1040		240 hours (minimum)	96 hours (minimum)	96 hours (minimum)
13. Final electrical test (see E.5.2 For PDA) 11/		As specified.	100 percent	100 percent	100 percent
a. Interim electrical and delta parameters for PDA			Group A, subgroup 2, Interim electrical and delta parameters. (Read and record)	Group A, subgroup 2. Read and record Interim electrical and delta parameters (See E.5.3.2).	Group A, subgroup 2. Read and record Interim electrical and delta parameters (See E.5.3.2).
b. Other electrical parameters			Group A, subgroup 3.		
14. Hermetic seal 6/	1071	(Same as 7 above) 12/	100 percent	Optional 7/	Optional 7/
a. Fine					
b. Gross					

See footnotes at end of table.

TABLE IV. Screening requirements - Continued.

Screen	MIL-STD-750 method	Condition	JANS requirements	JANTXV requirements	JANTX requirements
15. Radiography	2076	13/	100 percent 14/	Not applicable	Not applicable
16. External visual examination	2071	To be performed after complete marking and prior to lot acceptance	100 percent	Not applicable	Not applicable

1/ Visual inspection (test method 2074) on clear glass diodes shall be performed any time prior to marking.
2/ Shall be performed any time before completion of screen 13. Surge shall precede thermal impedance. Surge and thermal impedance are applicable only when specified in the screening table of the performance specification sheet.
3/ Constant acceleration shall be performed on gold ball bond devices and gold wire for germanium.
4/ PIND is not applicable to any device with external and internal pressure contacts (die to electrical contacts), optical coupled isolators, and double plug diodes. PIND screening may be performed any time after screen 4 when imposed by contract or purchase order (see E.5.4.1).
5/ Omit BIST and FIST tests for double plug or case-mounted diodes. Omit FIST test for temperature compensated referenced diodes.
6/ Non-transparent glass encased double plug noncavity axial lead diodes only may use test method 2068 in lieu of 1071.
7/ Fine and gross seal leak test for JANTX and JANTXV shall be performed in either screen 7 or screen 14.
8/ Optional accelerated HTRB for POWERFETs in accordance with test method 1042, condition A, shall be 48 hours minimum at T_A = +175°C minimum. Initial use of this option is contingent upon subsequent completion of a one time 1,000 hour qualification in accordance with test method 1042, and as specified on group E of the individual performance specification sheet, condition A to be submitted with the initial qualification report.
9/ For JANS only, zener diodes shall be subjected to high temperature reverse bias at 80 - 85 percent of nominal V_Z for V_Z > 10 V. Omit test for devices with $V_Z \leq 10$ V. For JANS case mounted rectifiers condition A is required.
10/ For JANTX and JANTXV levels full wave-blocking test shall replace power burn-in for all thyristors.
11/ Tests previously performed 100 percent (surge, thermal impedance) need not be repeated in screen 13.
12/ Hermetic seal screens for JANS may be performed in any order following final electrical test. Glass diodes shall not be painted until after seal tests. When hermetic seal testing is performed in screen 7 it does not have to be performed again in screen 14 for double plug diode construction.
13/ The radiographic screen for JANS may be performed in any sequence after screen 8.
14/ Conformance inspection may be initiated immediately prior to screen 15.

APPENDIX E

TABLE V . Group A inspection.

Subgroups	JANS 1/ sample plan	JAN, JANTX, JANTXV sample plan 1/
Subgroup 1 Visual and mechanical inspection (MIL-STD-750, test method 2071)	15 devices c = 0	45 devices c = 0
Subgroup 2 DC (static) test at +25°C	116 devices c = 0	116 devices 2/ c = 0
Subgroup 3 DC (static) tests at maximum rated and minimum rated operating temperatures	2/ 4/	116 devices 2/ 3/ c = 0
Subgroup 4 Dynamic tests at +25°C		116 devices 2/ 3/ c = 0
Subgroup 5 Safe operating area test (for transistors only): a. DC b. Clamped inductive (only when applicable) c. Unclamped inductive (only when applicable) End-point electrical measurements	5/ 45 devices c = 0	45 devices c = 0
Subgroup 6 Surge current (for diodes/rectifiers only) End-point electrical measurements		22 devices c = 0
Subgroup 7 Selected static and dynamic tests		22 devices c = 0

1/ The specific parameters to be included for tests in each subgroup shall be as specified in the applicable performance specification sheet. Where no parameters have been specified in a particular subgroup or test within a subgroup, no group A testing is required for that subgroup or test to satisfy group A requirements. A single sample may be used for all subgroup testing. These tests are considered nondestructive and devices may be shipped.

2/ If a device in the sample fails one or more test(s) in the subgroup(s) being sampled, each device in the (sub)lot represented by the sample shall be screened for the test(s) for which the sample failed. An alternate test method (for A3 or A4 only) to remove the failure mode may be used after an Engineering evaluation is performed. A second sample (first resubmittal) using double the large lot sample size shall be tested to the failed parameter. If the second sample fails, the lot shall be screened to the failed test(s) and a third sample (second resubmittal) using double the large lot sample size shall be tested to the failed parameter or the lot shall be rejected.

3/ For small lot sampling plan, n = 45.

4/ All devices required by the specified sample plan shall be subjected to subgroups 2, 3, and 4 combined.

5/ All devices required by the specified sample plan shall be randomly selected from the devices subjected to subgroups 2, 3, and 4, and shall be subjected to subgroups 5, 6, and 7 combined.

TABLE VIa. Group B inspections for JANS devices.

Inspections	MIL-STD-750 method	MIL-STD-750 condition	Qualification and large lot conformance inspection sample plan	Small lot CI
Subgroup 1 1/ Physical dimensions	2066	Dimensions in accordance with case outline specified in performance specification sheets	22 devices c = 0	8 devices c = 0
Subgroup 2 1/ Solderability	2026	Separate samples may be used for each test. The sample plan applies to the number of leads inspected. A minimum of 3 devices shall be tested.	15 leads c = 0	6 leads c = 0
Resistance to solvents	1022	Not required if marking is etched into the device.	15 devices c = 0	6 devices c = 0
Subgroup 3 Temperature cycling (air-to-air) (except for axial lead glass diodes)	1051	Test condition C, or maximum storage temperature, whichever is less. (100 cycles)	22 devices c = 0	6 devices c = 0
Thermal shock (liquid-to-liquid) (For axial lead glass diodes only)	1056	25 cycles, condition A		
Surge	4066	As specified.		
Hermetic seal 2/	1071			
a. Fine		Not required for double plug diodes. Test condition G or H, maximum leak rate = 5×10^{-8} atm cc/s, except 5×10^{-7} atm cc/s for devices with internal cavity > 0.3 cc. Maximum leak rate = 5×10^{-6} atm cc/s for cavities 3-40 cc		
b. Gross Electrical measurements		As specified.		

See footnotes at end of table.

TABLE VIa. Group B inspections for JANS devices - Continued.

Inspections	MIL-STD-750 method	MIL-STD-750 condition	Qualification and large lot conformance inspection sample plan	Small lot CI
Subgroup 3 - Continued				
Decap-internal visual (design verification) 3/	2075	Visual criteria in accordance with qualified design and internal visual precap criteria.	6 devices c = 0	6 devices c=0
Bond strength (wire or clip bonded devices only)	2037		22 wires or 11 devices c = 0 (Whichever requires the smaller number of devices.)	12 wires or 6 devices c=0 (Whichever requires the smaller number of devices.)
SEM (when specified) 4/	2077		6 devices c = 0	
Die shear (excluding axial leaded devices)	2017	The same number of devices used for bond strength will also be used for die shear (minimum of six die)		
Subgroup 4			22 devices c = 0	12 devices c = 0
Intermittent operation life	1037 1042	2,000 cycles As specified. Condition D		
Electrical measurements		Thermal impedance and other electrical measurements as specified.		
Subgroup 5			22 devices c = 0	12 devices c = 0
Accelerated steady-state operation life		Bias conditions as specified.		
Eutectic die attached semiconductors	1027	T_J = +275°C minimum (for 96 hours minimum)		
Soft solder die attached power semiconductors	1027	T_J = +225°C minimum (for 168 hours minimum)		
Electrical measurements		As specified.		

See footnotes at end of table.

TABLE VIa. Group B inspections for JANS devices - Continued.

Inspections	MIL-STD-750 method	MIL-STD-750 condition	Qualification and large lot conformance inspection sample plan	Small lot CI
Subgroup 5 - Continued				
Schottky diodes	1038	T_J = rated T_J maximum (for 240 hours minimum)		
Electrical measurements		As specified.		
Accelerated steady-state gate stress power MOSFETS	1042	Condition B, V_{GS} = rated, T_A = +175°C, t = 24 hours or T_A = 150°C, t = 48 hours		
Electrical measurements		As specified.		
Accelerated steady-state reverse bias power MOSFETS	1042	Condition A, V_{DS} = rated, T_A = +175°C, t = 120 hours or T_A = 150°C, t = 240 hours and as specified		
Electrical measurements		As specified.		
Category II Metallurgical bond Diodes		T_J =+200°C min. for 240 hours min.		
Bond strength All Au-Al interconnects	2037	As specified. Bond strength samples shall have passed accelerated steady-state operation life.	20 wires c = 0	20 wires c = 0
Subgroup 6 5/			22 devices c = 0	8 devices c = 0
Thermal resistance Diodes	3101 or 4081	As specified.		
Transistors (bipolar)	3131			
Transistors (POWER FETs)	3161			
Thyristors	3181			
IGBT	3103			
GaAs FET	3104			

1/ Electrical reject devices from the same inspection lot, may be used for all subgroups, when electrical end-point measurements are not required. Other non-catastrophic rejected devices (i.e., PIND, X-ray) may be utilized for all subgroups. For subgroups with end-point measurements, the devices shall be screened to table IV through block 13.
2/ Non-transparent glass encased double plug noncavity axial lead diodes only may use test method 2068 in lieu of 1071.
3/ Verification of metallurgical bond as defined in appendix A in its entirety shall be documented. (Photos are required with a scale or magnification identifier)
4/ This test may be performed at any time prior to lot formation.
5/ Thermal resistance may be performed on a group C frequency whenever 100 percent thermal impedance is performed

TABLE VIb. Group B inspections for JAN, JANTX, and JANTXV devices.

Inspections	MIL-STD-750		Sample plan	Small lot conformance inspection
	Method	Condition		
Subgroup 1 1/		Separate samples may be used for each test		
Solderability	2026	The sample plan applies to the number of leads inspected. A minimum of 3 devices shall be tested.	15 leads c = 0	4 leads c = 0
Resistance to solvents	1022	Not required if marking is etched into the device.	15 devices c = 0	3 devices c = 0
Subgroup 2			22 devices c = 0	6 devices c = 0
Temperature cycling (air-to-air) except for axial lead glass diode	1051	Test condition C, or maximum storage temperature whichever is less, (45 cycles, including screening)		
Thermal shock (liquid-to-liquid) (For axial lead glass diodes only)	1056	10 cycles, condition A		
Surge	4066	As specified.		
Hermetic seal 2/				
a. Fine leak	1071	Not required for double plug diode. Test condition G or H, maximum leak rate = 5×10^{-8} atm cc/s, except 5×10^{-7} atm cc/s for devices with internal cavity > 0.3 cc. Maximum leak rate = 5×10^{-6} atm cc/s for cavities 3-40 cc		
b. Gross leak				
Electrical measurements 3/		As specified.		

See footnotes at end of table.

TABLE VIb. Group B inspections for JAN, JANTX, and JANTXV devices - Continued.

Inspections	MIL-STD-750		Sample plan	Small lot conformance inspection
	Method	Condition		
Subgroup 3 4/			45 devices c = 0	12 devices c = 0
Steady-state operation life or intermittent operation life 5/	1027 1037 1042	Bias conditions as specified, 340 hours (minimum) 2,000 cycles (minimum) Condition D, 2,000 cycles (minimum)		
Electrical measurements		As specified.		
Bond strength (wire or clip bonded devices only)	2037	The sample shall include a minimum of 3 devices and shall include all wire sizes.	11 wires c = 0	11 wires c = 0
Subgroup 4			1 device c = 0	1 device c = 0
Decap internal visual (design verification)	2075	Visual criteria in accordance with qualified design.		
SEM (when specified)	2077		6 devices c = 0	6 devices c = 0
Subgroup 5			15 devices c = 0	6 devices c = 0
Thermal resistance:		As specified. Thermal resistance maybe performed on group C frequency whenever 100 percent thermal impedance is performed.		
Diodes	3101 or 4081			
Transistors (bipolar)	3131			
Transistors (POWERFETs)	3161			
Thyristors	3181			
IGBT	3103			
GaAs FET	3104			
Subgroup 6 6/			32 devices c = 0	12 devices c = 0
High-temperature life (nonoperating)	1032	340 hours minimum, $T_{STG(max)} = T_A$		
Electrical measurements		As specified.		

1/ Electrical reject devices from the same inspection lot, may be used for all subgroups when electrical end-point measurements are not required. Other non-catastrophic rejected devices (i.e., PIND, X-ray) may be utilized for all subgroups. For subgroups with end-point measurements, the devices shall be screened to table IV through block 13.

2/ Non-transparent glass encased double plug noncavity axial lead diodes only may use test method 2068 in lieu of 1071. This test may be performed after electrical measurements.

3/ Unless otherwise specified, omit delta parameters limits for low current gain (h_{fe}) and leakage measurements included in end-point measurements.

4/ If a given inspection lot undergoing group B inspection has been selected to satisfy group C inspection requirements, the 340-hour or 2,000 cycle life tests may be continued on test to 1,000 hours or 6,000 cycles, as applicable, in order to satisfy the group C life test requirements and bond pull may be performed after group C life test. End-point measurements shall be performed or either group B, subgroup 3 (340 hours or 2,000 cycles, as applicable) to satisfy group B lot acceptance or group C, subgroup 6 (1,000 hours or 6,000 cycles, as applicable) to satisfy group B and C lot acceptance.

5/ Intermittent operation life shall be performed on all case mounted devices.

6/ Not required for power MOSFETs.

APPENDIX E

TABLE VII. Group C periodic inspections (all quality levels).

Inspections	MIL-STD-750		Sample plan	Small lot conformance inspection
	Method	Condition		
Subgroup 1			15 devices c = 0	6 devices c = 0
Physical dimensions 1/ (Not required for JANS)	2066	Dimensions in accordance with case outline specified in performance specification sheets		
Subgroup 2			22 devices c = 0	6 devices c = 0
Thermal shock (glass strain)	1056	Test condition A, except test condition B for devices with power rating of > 10 watts at T_C = +25°C.		
Terminal strength	2036	As specified.		
Hermetic seal 2/				
a. Fine leak	1071	Not required for double plug diodes. Test condition G or H, maximum, leak rate = 5 x 10^{-8} atm cc/s, except 5 x 10^{-7} atm cc/s for devices with internal cavity > 0.3 cc. Maximum leak rate = 5 x 10^{-6} atm cc/s for cavities 3-40 cc.		
b. Gross leak				
Moisture resistance	1021	Omit initial conditioning.		
Electrical measurements		As specified.		
Subgroup 3		Not required for disc packages or metallurgically bonded double plug devices, or stud packaged devices.	22 devices c = 0	6 devices c = 0
Shock	2016	Nonoperating, 1,500 G's, 0.5 ms, 5 blows in each orientation, X1, Y1, and Z1 (Y1 only for axial glass diodes.)		
Vibration, variable frequency	2056			
Constant acceleration 3/	2006	1 minute minimum in each orientation. X1, Y1, and Z1 at 20,000 G's minimum, except at 10,000 G's minimum for devices with power rating of ≥ 10 watts. T_C = +25°C.		
Electrical measurements		As specified.		

See footnotes at end of table.

TABLE VII. Group C periodic inspections (all quality levels) - Continued.

Subgroup 4 Salt atmosphere (corrosion) 1/	1041		15 devices c = 0	6 devices c = 0
Subgroup 5 Thermal resistance 7/	3101 3103 3104 3131 3161 3181 4081	As specified.	15 devices c = 0	6 devices c = 0
Subgroup 6 4/ 5/ Steady-state operation life or Intermittent operation life or Blocking life Electrical measurements	 1026 6/ 1037 1042 1048 6/	Not required for disc packages. 1,000 hours minimum at maximum operating junction temperature 6,000 cycles minimum. Condition D, 6,000 cycles minimum. As specified.	22 devices c = 0	12 devices c = 0
Subgroup 7 Internal water vapor 8/	 1018	 To be performed on each structurally identical package family	3 devices c = 0 or 5 devices c=1 9/	3 devices c = 0 or 5 devices c=1 9/

1/ Electrical reject devices from the same inspection lot, may be used for all subgroups when electrical end-point measurements are not required. Other non-catastrophic rejected devices (i.e., PIND, X-ray) may be utilized for all subgroups. For subgroups with end-point measurements, the devices shall be screened to table IV through block 13.

2/ Non-transparent glass encased double plug noncavity axial lead diodes only may use test method 2068 in lieu of 1071. This test may be performed after electrical measurements.

3/ Not applicable to any devices with external and internal pressure contacts (die to electrical contacts), optical coupled isolators, and double plug diodes.

4/ If a given inspection lot undergoing group B inspection has been selected to satisfy group C inspection requirements, the 340-hour or 2,000 cycles life tests may be continued on test to 1,000 hours or 6,000 cycles, as applicable, in order to satisfy the group C life test requirements. End-point measurements shall be performed on either table VIa, group B, subgroup 4, or table VIb group B, subgroup 3 (340 hours or 2,000 cycles, as applicable) to satisfy group B (table VIa or table VIb) lot acceptance or group C, subgroup 6 (1,000 hours or 6,000 cycles, as applicable) to satisfy group B and C lot acceptance.

5/ Intermittent operation life shall be performed on all case mounted devices.

6/ The sample size may be increased and the test time decreased so long as the devices are stressed for a total of 22,000 device hours minimum, and the actual time of test is at least 340 hours.

7/ Not required when performed in group B

8/ Not required when internal water vapor process monitor (see D.3.9.5.d) is approved by the qualifying activity (written authorization is required). Subgroup 7 is not required for noncavity devices.

9/ An engineering evaluation shall be performed if there is a device failure. Corrective action shall be taken as necessary.

TABLE VIII. Group D inspection (RHA inspections). 1/

Test	MIL-STD-750		JANS		JANTXV	
	Method	Condition	Quantity/ (accept number)	Notes	Quantity (accept number)	Notes
Subgroup 1 2/ Neutron irradiation Qualification and CI End-point electrical parameters	1017	+25°C As specified in accordance with performance specification sheet	11(0)	3/	(a) 11(0)	4/
Subgroup 2 5/ Steady-state total dose irradiation Qualification and CI End-point electrical parameters	1019	+25°C As specified in accordance with performance specification sheet	4(0) 2(0) 1(0)	6/ 8/ 9/	11(0)	7/
Subgroup 3 10/ Power transistor electrical dose rate test End-point electrical parameters	3478	+25°C As specified in accordance with associated specification.	11(0)	3/	11(0)	4/

1/ Parts used for one subgroup test may not be used for other subgroups but may be used for higher levels in the same subgroup. Unless testing is performed within the time limits of the test method, total exposure shall not be considered cumulative. Group D tests may be performed prior to device screening (see E.6.1.5).
2/ Unless by design, waive neutron tests for MOS devices, bipolar elements are an integral part of the device function.
3/ In accordance with wafer lot. If one part fails, seven additional parts may be added to the test sample with no additional failures allowed, 18 devices, c = 1.
4/ In accordance with inspection lot. If one part fails, seven additional parts may be added to the test sample with no additional failures allowed, 18 devices, c = 1.
5/ JANTXV devices shall be inspected using either the JANTXV quantity/accept number criteria as specified, or by using the JANS criteria on each wafer.
6/ For device types with greater than or equal to 4,000 die per wafer, selected from a random locations on the wafers.
7/ In accordance with inspection lot. If one part fails, 16 additional parts may be added to the test sample with no additional failures allowed, 27 devices, c = 1. For devices which require more than one bias, the sample size shall be 11(0) for each bias.
8/ For device types with greater than 500 and less than 4,000 die per wafer, selected from random locations on each wafer.
9/ For device types with less than or equal to 500 die per wafer, selected from random locations on each wafer.
10/ Upset testing during qualification on first CI shall be conducted when specified in purchase order or contract. When specified, the same devices may be tested in more than one subgroup.

APPENDIX E

TABLE IX. Group E inspections (all quality levels) for qualification only.

Inspections	MIL-STD-750		Sample plan
	Method	Condition	
Subgroup 1			
Thermal shock or	1056	100 cycles or as specified.	As specified.
Temperature cycling	1051	500 cycles minimum or as specified.	
Electrical measurements			
Subgroup 2		As specified.	As specified.
Intermittent operating life	1037		
Life test	1042		
Electrical measurements or			
Steady-state operating life	1026		
Electrical measurements or			
Blocking life	1048		
Electrical measurements			
Subgroup 3 As specified		As specified.	As specified.
Destructive physical analysis	2101 2102		
Subgroup 4		As specified.	22 devices c = 0
Thermal resistance			
Transistors			
POWERFETs	3161		
Bipolar	3131		
Diodes	3101 or 4081		
IGBT	3103		
GaAs FET	3104		
Subgroup 5		As specified.	15 devices c = 0
Barometric pressure (reduced) (required only on all devices with rated voltage > 200 V)	1001		
Subgroup 6			
ESD	1020	As required by E.4.2.1	3 devices

APPENDIX E

TABLE X. Data guidance for JANS devices.

Data	
Wafer lot Inspection (see E.3.1.2.2) Screening (see E.5) Conformance Inspection(see E.6)	1. SEM photographs (when applicable) 2. Electrical data 3. Radiographs 4. Screen data 5. Electrical data 6. SEM photographs (when applicable) 7. Bond pull limits (when applicable) 8. Lot rejection report 9. CI data (groups A, B, C, and D)

APPENDIX F

RADIATION TOLERANT SOURCE OF SUPPLY

F.1 SCOPE

F.1.1 Scope. This appendix presents the requirements for radiation tolerant source of supply program. This appendix is not a mandatory part of this specification. The information contained herein is intended for guidance only. Manufacturers must demonstrate to the qualifying activity a system that achieves at least the same level of quality as could be achieved by complying with this appendix.

F.2 APPLICABLE DOCUMENTS. This section is not applicable to this appendix.

F.3 RADIATION HARDNESS ASSURANCE PART MANAGER PROGRAM

F.3.1 Radiation hardness assurance part manager (RHAPM). An RHAPM is a certified company (e.g., original equipment manufacturer (OEM)) who establishes a relationship with a component manufacturer for the sole purpose of developing RHA semiconductors and has the responsibility to ensure compliance of all manufacturing and testing procedures. The certified company shall be listed as the manufacturer for the semiconductor device specified. The RHAPM is responsible for setting up a control system to ensure all requirements of the general and associated device specifications are met.

F.3.1.1 Eligibility of participants. To be eligible to qualify a RHA part, a specification for the part must exist. Performance specification sheets are controlled and modified by the preparing activity. Participants shall be certified on the basis of a facilities survey.

F.3.1.1.1 Preparation of the associated device specification. After the parts selection and prior to a third party agreement with a device manufacturer, the RHAPM must notify the preparing activity of their intent and request that an associated device specification number be assigned. This can be accomplished in writing or by submitting a DD Form 2052 Non-standard Parts Approval Request through the Military Parts Control Advisory Group (MPCAG). In the justification section of this form the RHAPM will indicate a willingness to prepare the performance specification sheet. After the applicable parts control procedures have been followed, the preparing activity will assign a JAN performance specification sheet number or revision letter. The RHAPM will prepare the preliminary draft and submit it to the preparing activity. This preliminary draft does not have to be complete. It may have blank tables, figures, and it may be group D only, but it must be in the correct JAN associated device specification format. A copy of this format is available from any of the technology representatives within the preparing activity (see figure 6).

F.3.1.1.2 Participants preparation for certification. All participants shall comply with the RHAPM management plan and all applicable requirements as specified in sections 3 and 4 of MIL-PRF-19500 and F.3.3.1 herein. Qualification of RHA devices shall comply with the provisions in appendix E. CI shall comply with the provisions of appendix E and F.3.3.1.

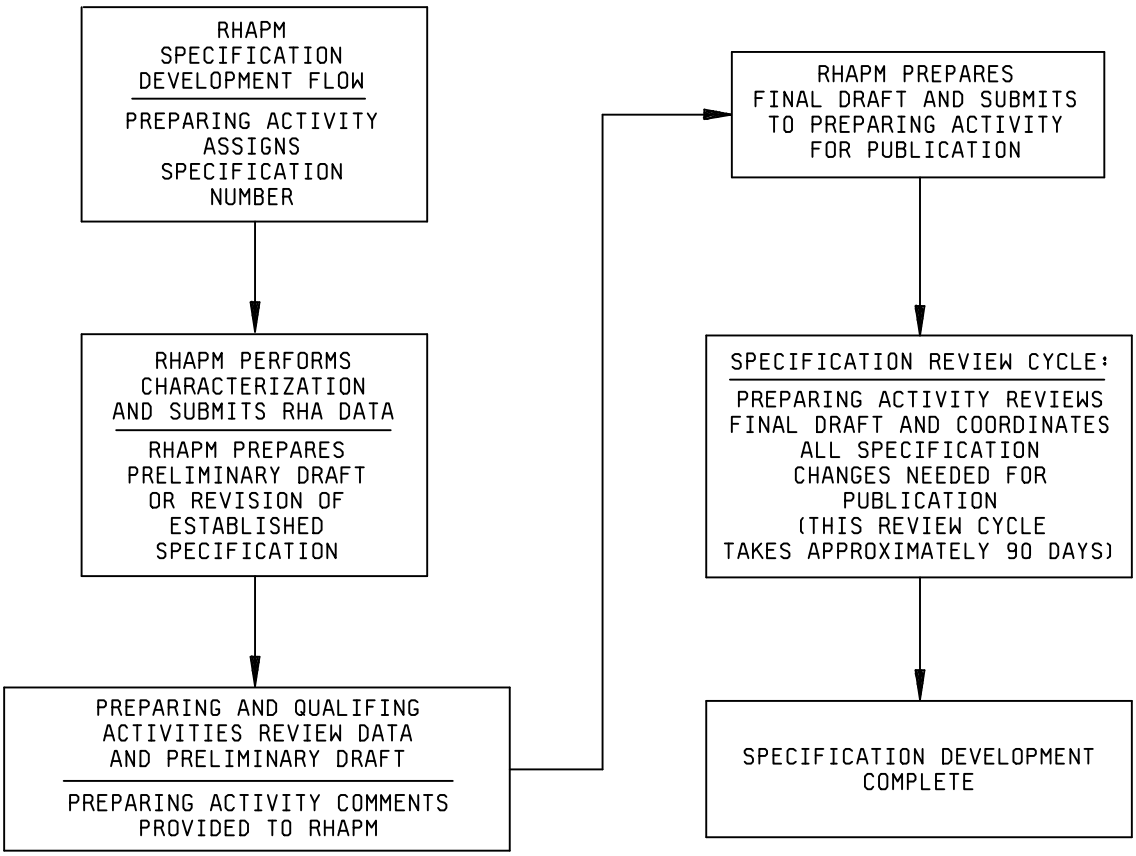


FIGURE 6. Specification development flow.

F.3.2 RHAPM verification requirements. The RHAPM verification program shall assure that the design, processing, assembly, inspection and testing of semiconductor devices comply with this specification and the applicable performance specification sheet. This program shall not require ownership of all manufacturing and testing facilities and establishes additional requirements for the sole purpose of developing a standard RHA product. As a minimum the RHAPM shall document the relationship as follows:

a. Individual responsibilities.

b. Product reliability.

c. Product quality.

d. Traceability.

e. Individual liability.

f. Data support.

g. Part marking.

h. Lot integrity of RHA product.

i. Testing (e.g., certified and qualified to MIL-PRF-19500).

A RHAPM must maintain an active working relationship with the device manufacturer, the preparing and qualifying activities, and the Systems Program Office (SPO). These relationships will constitute a partnership between the RHAPM, the device manufacturer, and the Government to insure the availability of high reliable standard RHA product to be used in more than one Department of Defense (DoD) system.

F.3.2.1 Management review. The RHAPM verification program shall be reviewed at appropriate intervals by responsible management to ensure RHA performance, product reliability, and the effectiveness of the established program. Records of management review shall be maintained covering the following minimum areas:

a. RHA design (when needed).

b. RHA baselines.

c. RHA characterization.

d. Process change control.

e. RHA testing (MIL-STD-750 test methods).

f. RHA Test laboratory suitability (Qualifying Activity).

g. Development of associated device specifications (Preparing Activity).

F.3.2.2 Management plan. The management plan shall be established in accordance with appendix D and submitted to the qualifying activity prior to a survey. It shall serve as a basis to demonstrate to the qualifying activity that the RHAPM has an understanding of a complete RHA verification program. The management plan, as exemplified by its documentation system, is adequate to assure compliance with the applicable specifications and quality standards. The management plan shall contain, as a minimum, these items and they shall be available for review at all sites:

a. Functional block diagrams.

b. Manufacturing flow charts by technology.

c. Examples of documentation as required by F.3.2.

d. Examples of records as required by F.3.2.

e. Examples of internal and device manufacturer audit activities.

f. Examples of ppm/spc monitoring.

F.3.3 Certification requirements. Only RHAPM certified companies may develop RHA products and be listed.

F.3.3.1 RHAPM certification. Before an OEM can be considered as a RHAPM, he must demonstrate the capability to control and manage radiation hardened product. This can be accomplished through a pre-certification review and certification audit (see figure 7).

F.3.3.1.1 Pre-certification review. The pre-certification review of the OEM's management plan shall address the following:

a. The interface between the RHAPM and the third parties.

b. The availability of RHA product to other programs.

c. Methods for acquisition, storage, and delivery.

Upon completion of this review the OEM shall receive an authorization to pursue certification as a RHAPM. After receiving authorization the potential RHAPM has one year to establish a qualification plan and develop third party relationships with subcontractors.

F.3.3.1.2 RHAPM certification and laboratory suitability. After the third party relationships have been established the qualifying activity must be notified and qualification milestones, certifications, and laboratory suitabilities, must be established. Laboratory suitability shall be obtained from the qualifying activity for all facilities designated to perform RHA characterization and CI. A list of laboratories being used shall be submitted to the qualifying activity. It will be the responsibility of the RHAPM to insure each RHA test facility maintains suitability. The RHAPM will be responsible for the CI. CI shall be part of the RHA baseline and shall be performed as specified in the general and performance specification sheets.

F.3.3.1.2.1 Characterization. The RHAPM must be responsible for the performance of all RHA characterization. This includes all known and testable radiation effects. As a minimum characterization shall include the following test methods:

a. Neutron irradiation (MIL-STD-750, test method 1017).

b. Ionizing radiation (MIL-STD-750, TOTAL DOSE test method 1019).

c. Dose rate burnout (MIL-STD-750, test method 3478).

d. Single Event Gate Rupture: (MIL-STD-750, test method 1080)

All characterization shall be to the device capability (not the system capability) under worst case conditions for the device technology and design. Data will be to functional failure or to a level of irradiation which best represents the product capability. From this data, endpoint electrical parameter limits shall be established. The associated device specification shall represent these limits in the appropriate test tables.

F.3.3.1.2.2 Baselines. The RHAPM shall establish the RHA baseline and insure the device manufacturer maintains the manufacturing controls in accordance with this baseline. Any changes to the baseline must be coordinated through the RHAPM and reported to the qualifying activity.

F.3.3.1.2.3 RHA qualification. In order to be listed as a source, the RHAPM must receive from the qualifying activity the following:

a. Certification: wafer fabrication, assembly, and test.

b. Suitability: test laboratories and radiation facilities.

F.3.3.1.3 Retention for RHAPM. This listing requires that the RHAPM shall maintain the following documentation:

a. Annual retention reports.

b. Self-audits.

c. Annual recertification/resuitability (class S).

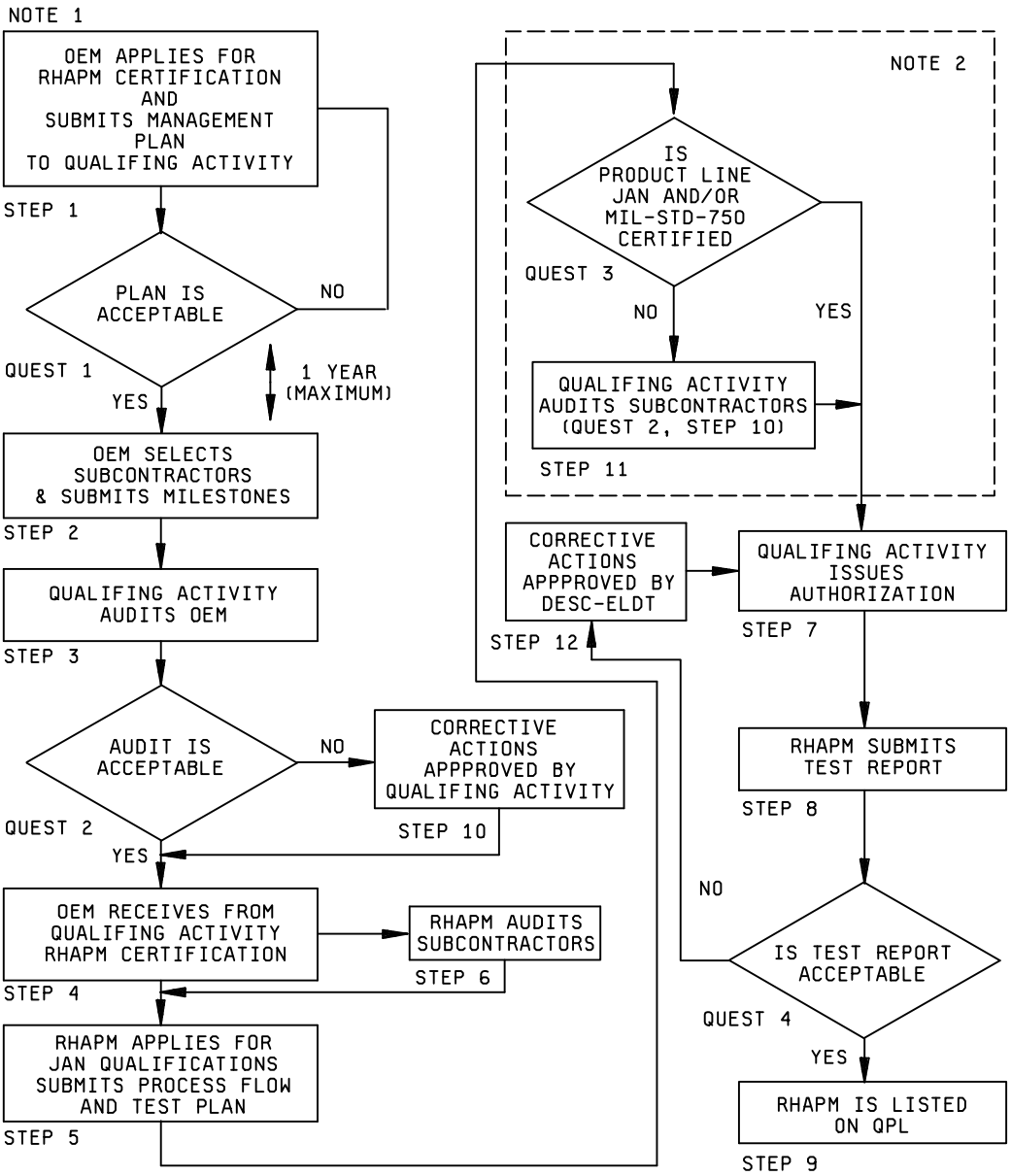


FIGURE 7. Product development flow.

NOTES:
1. The product development flow is as follows:

Step 1. OEM applies for certification as a RHAPM. At this point the qualifying activity will request a management plan (see F.3.2.2) be formulated and presented to the certifying activity (preparing and qualifying activities).

NOTES - Continued

Question 1. The certifying activity will review the management plan. When all problem areas have been resolved the OEM may be considered as a potential RHAPM. Upon acceptance of the management plan the potential RHAPM will have up to 1 year to accomplish step 2 herein.

Step 2. The potential RHAPM establishes relationships with subcontractors and submits a detailed outline of these relationships (see F.3.1.1.2) to the certifying activity for review. This outline must include qualification milestones.

Step 3. The certifying activity reviews potential RHAPM's verification program, management plan and verifies by auditing the potential RHAPM's procedures to insure compliance to MIL-PRF-19500 and all of appendix F.

Question 2. After reviewing all audit data the certifying activity will issue RHAPM certification. If there are any unresolved issues step 10 must be completed before certification can be issued.

Step 4. The qualifying activity issues RHAPM certification (see F.3.3). The RHAPM's management plan is implemented.

Step 5. Product line, RHA characterization, lab and device manufacturer are selected. The RHAPM is responsible for maintaining compliance to MIL-STD-750 and MIL-PRF-19500 by it's subcontractors. It is also the RHAPM's responsibility to insure that it's subcontractors procedures and documentation meet the baseline established within the RHAPM's management plan (see F.3.2 and F.3.3).

Step 6. RHAPM will prepare preliminary draft specifications for submission to the preparing activity. After the associated device specification has been approved and dated the RHAPM applies for device qualification (see F.3.1.1.1 and figure 6). This application must include a process flow and test report.

Question 3. Before an authorization (step 7) can be issued all device fabrication and assembly must be JAN or MIL-STD-750 certified and all test facilities must have received suitability from the qualifying activity. If not Step 11 must be completed.

Step 7. The qualifying activity issues authorization. The qualification test notification outlines the product to be tested, testing to be performed, sample sizes, and test locations.

Step 8. The qualification data test report is submitted to the qualifying activity for evaluation and review.

Question 4. If all qualification data is in accordance with MIL-PRF-19500, the associated device specification, and the RHAPM's management plan listing is authorized. If not Step 12 must be completed.

Step 9. The RHAPM is listed as the source of supply for the JAN RHA device.

Steps 10 and 12. If questions 2 and 4 are "NO", the qualifying activity will evaluate proposed correction actions. These corrective actions must be implemented and approved before the next step can be accomplished.

Step 11. All subcontractors must be certified or have received from the qualifying activity laboratory suitability (see F.3.3). If the answer to Question 3 is "NO", the qualifying activity must perform an audit of the facility in question. Any deficiencies requiring corrective action must be implemented and approved prior to granting manufacturer certification or laboratory suitability (see question 2 and step 10).

2. Question 3 may be answered at any time within the certification process, but if the answer is "NO" step 11, question 2 and step 10 must be accomplished before qualification testing can be authorized.

APPENDIX G

DISCRETE SEMICONDUCTOR DIE/CHIP LOT ACCEPTANCE

G.1 SCOPE

G.1.1 Scope. The purpose of this appendix is to establish minimum standards for screening and qualification of JANHC and JANKC unencapsulated discrete semiconductor devices (die/chips) for use in semiconductor devices. This appendix is a mandatory part of this specification. The information contained herein is intended for compliance only.

G.2 APPLICABLE DOCUMENTS. This section is not applicable to this appendix.

G.3 DEFINITIONS

G.3.1 Date code. Seal week of the Element Evaluation (EE) packaged samples.

G.3.2 Die/chips. Unencapsulated discrete semiconductors. The term chip is interchangeable with the term die.

G.3.3 Manufacturer. Original wafer lot fabricator.

G.3.4 Identification. See 1.3 for identification.

G.3.5 Wafer lot. A wafer lot shall consist of only semiconductor wafers subjected to each and every process step as a group. Each wafer lot shall be assigned a unique identifier which provides traceability to all wafer processing steps. Rework provisions shall be in accordance with D.3.13.2. Wafer lot records shall identify all JANHC and JANKC device inspection lots formed from the wafer lot.

G.3.6 Inspection lot. An inspection lot shall consist of one device type from a single wafer lot.

G.4 REQUIREMENTS

G.4.1 General. Semiconductor die shall conform to the requirements contained herein.

G.4.2 Screening. Semiconductor die shall be screened in accordance with table XI.

G.4.3 Qualification. Qualification shall be based on the results of the first EE performed and submitted to DSCC.

G.4.3.1 Wafer fabrication. Qualification shall be performed by the original wafer lot manufacturer from die manufactured in the same wafer fab that was used to qualify a PIN on the QML of the same function and technology. Qualification for JANKC can only be approved on die processed in a wafer fab that has been used to qualify a JANS part on the QML of the same technology and function. For the purpose of this specification, examples of function are: signal transistor, FREDS, power transistor, zener diode, rectifier or transient suppressor. The term technology may include: DMOS, VMOS, diffused junction, alloy junction, JFET and Schottky.

G.4.3.2 Facility. JANHC qualification shall only be granted to a manufacturer who has a MIL-PRF-19500 certified facility. JANKC qualification will only be granted to a manufacturer who is MIL-PRF-19500 certified to manufacture JANS products.

G.4.4 Performance characteristics. The electrical performance characteristics of semiconductor die shall be as specified in the performance specification sheet.

G.4.5 Critical interfaces. The critical interfaces and physical dimensions of the semiconductor die shall be in accordance with the requirements of MIL-PRF-19500 and with G.4.5.1 through G.4.5.3. A completed design and construction form and die topography, including dimensions, pad locations, and metallization descriptions (die map) shall be made available for inspection to the qualifying activity prior to qualification. A unique critical interface identifier as part of the PIN shall be assigned based on any of the following differences:

a Bond pad metal.

b. Backside metal.

G.4.5.1 Bonding pad. The bonding pad size, location, and electrical function shall be in accordance with the applicable performance specification sheet. Unless approved by the qualifying activity, the minimum bond pad dimensions shall be 3 mils.

G.4.5.1.1 Metallization integrity. The bonding pads shall be metallized and suitable for bonding as specified in the associated performance specification sheet and shall meet the requirements of G.5.2.5.1.

G.4.5.2 Backing material. The backing material shall be as described in the performance specification sheet, and meet the requirements of G.5.2.5.2.

G.4.5.3 Glassivation. Glassivation requirements of H.3.7 apply.

G.5 VERIFICATION PROVISIONS.

G.5.1 General. EE of semiconductor die shall be performed at a facility with MIL-STD-750 laboratory suitability for the applicable test methods.

G.5.1.1 Responsibility for inspection. The supplier shall be responsible for the performance of all inspection requirements as specified herein and in the performance specification sheet.

G.5.1.2 Retention of records. The supplier shall maintain adequate records of all examinations, inspections, and tests performed in accordance with the requirements specified herein and the associated performance specification sheet. Records, including variables data, shall be retained in accordance with appendix D.

G.5.1.3 JANKC wafer lot inspection. For JANKC, the process monitors of D.3.9.4 shall apply.

G.5.1.4 Sequence of testing. Subgroups within a group (table XII) of tests may be performed in any sequence, but individual tests within a subgroup shall be performed in the sequence indicated.

G.5.1.5 Sample selection. Samples shall be randomly drawn from inspection lots. The sample size columns in the evaluation tables give minimum quantities to be evaluated with applicable accept number enclosed in parenthesis.

G.5.1.6 Wafer traceability. For JANKC, wafer traceability shall be maintained on the inspection lot and the element evaluation.

G.5.2 Element evaluation. Die from each wafer lot shall be evaluated in accordance with table XII.

G.5.2.1 Subgroup 1, 100 percent electrical test of die. Each die shall be electrically tested, which may be done at the wafer level provided all failures are identified and removed from the lot when the die are separated from the wafer. Test limits and conditions shall be chosen by the supplier to assure compliance with all the electrical characteristics specified by the associated specification. This allows the supplier to assign test values or test details which differ from the performance specification sheet requirements.

G.5.2.2 Subgroup 2, 100 percent visual inspection of die. Each die shall be visually inspected to assure conformance with the die related requirements of MIL-STD-750, test methods 2069, 2070, 2072 or 2073 as applicable. Qualified die may be stored at the manufacture's facility prior to 100 percent visual.

G.5.2.3 Subgroup 3.

G.5.2.3.1 Internal/die visual inspection. The 10 piece die visual sample shall be randomly selected from die that have successfully completed subgroup 2, table XII.

G.5.2.3.2 Test sample preparation. Test samples shall be assembled in suitable packages using standard assembly procedures.

G.5.2.3.3 Packaged sample identification. The packaged sample shall be marked or labeled in such a manner to identify the following:

a. Serial numbers if required.

b. Device PIN.

c. Inspection lot number or date code.

G.5.2.3.4 Internal visual. Each sample may be visually inspected after assembly and prior to encapsulation to assure conformance with the applicable requirements of MIL-STD-750, test methods 2069, 2070, 2072 or 2073.

G.5.2.4 Subgroup 4.

G.5.2.4.1 Subgroup 4. Each sample shall be processed in accordance with subgroup 4 of table XII.

G.5.2.4.2 Class HC sample size. The JANHC sample will consist of at least 10 die from each inspection lot.

G.5.2.4.3 Class KC sample size. The JANKC sample shall require 3 die from each wafer and a minimum of 10 die from each inspection lot.

G.5.2.5 Subgroups 5A and 5B.

G.5.2.5.1 Bond pull (5A). From each wafer lot, a sample of at least 5 die requiring 10 bond wires minimum shall be selected.

G.5.2.5.1.1 Wire bond strength testing. Bond strength shall be performed in accordance with MIL-STD-750, test method 2037 condition A.

> The die metallization shall be acceptable if no failure occurs. If only one wire bond fails, another sample may be selected in accordance with G.5.2.5.1and subjected to subgroup 5A evaluation. If the second sample contains no failures, the bonding test results are acceptable and the lot of die is acceptable. If the second sample contains one or more failures, or if more than one failure occurs in the first sample, the lot of die shall be rejected.

G.5.2.5.2 Die shear (5B). Die shear shall be performed in accordance with MIL-STD-750, test method 2017. If only one die fails, another sample may be selected and subjected to subgroup 5B evaluation. If the second sample contains no failures, the Die Shear test results are acceptable and the lot of dice is acceptable. If the second sample contains one or more failures, or if more than one failure occurs in the first sample, the lot of dice shall be rejected.

G.5.2.6 Subgroup 6, scanning electron microscope (SEM). To be performed on selected die designs in accordance with E.3.1.2.2. Sample selection and reject criteria shall be in accordance with MIL-STD-750, test method 2077.

G.5.2.7 Subgroup 7, radiation hardness assurance. Radiation hardness assurance inspection shall be as specified in the performance specification sheet.

G.5.3 Sample acceptance. The lot is acceptable if it passes all the appropriate requirements of table XII. If the test sample fails the criteria of the appropriate flow, the inspection lot shall be rejected. For JANKC lots represented by 5 wafers or more, any wafer whose assembled sample fails any of the requirements of table XII, subgroup 4, may be removed from the lot with no jeopardy to the rest of the lot if failure analysis determines that the failure mechanism is inherent to the removed wafers only. The inspection lot is rejected if more than 20 percent of the wafers had failures in subgroup 4 of table XII. If a failure is attributed to packaging or handling defects, ESD, equipment malfunction, or operator error, these samples shall be verified by failure analysis. Upon verification of such defects, the test sample may be replaced in accordance with appendix E.

G.5.4 Storage. Die shall be stored in dry nitrogen or other inert atmosphere.

G.6 PACKAGING

G.6.1 Packaging. All semiconductor die shall be packaged in individually lidded containers. For ESD sensitive devices (classes 1 and 2) conductive or anti-static containers shall be required with an external conductive field shielding barrier. Stacking of containers without lids shall not be allowed. The supplier may submit an alternate procedure for packaging of die for approval by the using activity.

G.6.2 Container marking. The following information shall be marked on each container of semiconductor die:

a. Type designation.

b. Applicable specification number.

c. Manufacturer’s logo or designation symbol.

d. Lot identification code.

e. Quantity.

f. ESD symbol (if applicable).

g. Date code (G.3.1).

h. Wafer identity for JANKC.

G.6.3 Certificate of conformance. The certificate of conformance shall be in accordance with 3.7 of MIL-PRF-19500.

APPENDIX G

TABLE XI. Steady state life time and temperature.

Option	Minimum time	Minimum junction temperature Tj
A	240 hours	175°C
B	500 hours	150°C
C	1,000 hours	125°C

1/ Example: If Tj of steady state life test is 187.5°C± 12.5°C, then option A is used.

TABLE XII. Die element evaluation requirements.

Subgroup	Class K	Class H	Test	MIL-STD-750 Method	MIL-STD-750 Condition	Quantity (accept no.)	Reference paragraph
1	x	x	Electrical test			100 percent	G.5.2.1
2	x	x	Visual Inspection	2069 2070 2072 2073		100 percent	G.5.2.2
3a	x	x	Internal/die Visual inspection	2069 2070 2072 2073		10 (0)	G.5.2.3.1
3b	x	x	Sample assembly			10 pieces minimum	G.5.2.3.2 G.5.2.3.3
4	x	x	Stabilization	1032	C t = 24 hour min	10 (0)	G.5.2.4.1 G.5.2.4.2 G.5.4.2.3
	x	x	Temperature cycling	1051	C		
	x		Mechanical shock or	2016	Y1 direction		
			Constant acceleration	2006	Y1 direction		
	x	x	Electrical test (Read/record)		Group A, subgroups 2, 3, 4		
	x	x	HTRB		Screen 10		1/
	x	x	Electrical test (Read/record)		Group A, subgroup 2		2/ 6/
	x	x	Burn-in		Screen 12		1/
	x	x	Electrical test (Read/record)		Group A, subgroup 2		2/ 6/
	x		Steady state life				3/
			Transistors Power FETS Diodes/rectifiers	1039 1042 1038	B A A or B		
	x		Electrical test (Read/record)		Group A, subgroup 2 and subgroup 3		2/

See footnotes at end of table.

TABLE XII. Die element evaluation requirements - Continued.

Subgroup	Class K	Class H	Test	MIL-STD-750 Method	MIL-STD-750 Condition	Quantity (accept no.)	Reference paragraph
5A	x	x	Wire bond evaluation	2037	Condition A	10 (0) wires or 20 (1) wires	G.5.2.5.1
5B	x	x	Die shear evaluation	2017		5 (0) or 10 (1)	G.5.2.5.2
6	x		SEM	2077		See test method 2077	G.5.2.6 5/
7	x x		RHA Total dose Neutron irradiation	 1019 1017		4/	G.5.2.7 5/

1/ HTRB and burn-in shall be performed when specified on the applicable performance specification sheet..
2/ Thermal Impedance shall not apply.
3/ Time and temperature requirements in accordance with table XI.
4/ Sample size shall be in accordance with the performance specification sheet.
5/ May be performed at any time.
6/ For JANHC only, if one device fails during any of the subgroup 4 tests following “Electrical tests” (group A, subgroups 2, 3, or 4), then 20 additional devices may be added to the element evaluation with no additional failures allowed, 30 devices, c = 1.

APPENDIX H

CRITICAL INTERFACE AND MATERIALS

H.1 SCOPE

H.1.1 Scope. This appendix contains critical interface information which will assist manufacturers in producing devices which meet 3.2. This appendix is not a mandatory part of this specification. The information contained herein is intended for guidance only.

H.2 APPLICABLE DOCUMENTS

H.2.1 General. The documents listed in this section are specified in sections H.3 and H.4 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements documents cited in sections H.3 and H.4 of this specification, whether or not they are listed.

H.2.2 Government documents.

H.2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DODISS) and supplement thereto, cited in the solicitation (see 6.2).

STANDARDS

FEDERAL

FED-STD-H28 - Screw-Thread Standards for Federal Services.

MILITARY

MIL-STD-750 - Test Methods for Semiconductor Devices.

(Unless otherwise indicated, copies of the above specifications, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

H.2.3 Order of precedence. In the event of a conflict between the text of this document and the references cited herein (except for related performance specification sheets), the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

H.3 CRITICAL INTERFACE AND CONSTRUCTION CRITERIA

H.3.1 Allowable alternate design, materials, and construction. Multiple device designs will be approved by the qualifying activity on a case by case basis for JAN, JANHC, JANKC, JANTX, and JANTXV per manufacturer, provided appropriate identification (as a minimum) is provided to ensure traceability. For JANS devices, only one design is allowed per manufacturer, and it may differ from the design of other verification levels. For radiation hardened devices of all levels, only one design is allowed, and it may differ from the design of non-radiation hardened devices. With the approval of the qualifying activity (see D.3.4.2), design material and construction alternatives for qualified device types may be allowed only for a limited time. An alternate design submitted for approval must be definitive of all pertinent construction features. Particular design features are not interchangeable between approved designs. A single inspection lot or sublot, in the case of lots made up of sublots of structurally identical devices, shall contain only one approved design, material and construction so that homogeneity is preserved within a given lot identification code and device type. The qualifying activity shall be notified of the first lot incorporating the change and the last lot of the present existing design and effective date codes for each. If the existing design is to be maintained, the manufacturer shall justify the retention, subject to approval by the qualifying activity. The qualifying activity may periodically identify specific alternate designs by device type and performance specification sheet and request justification for continued retention of that specific alternate design.

H.3.2 Package. All packaged devices supplied under this specification shall be hermetically sealed. No organic or polymeric material shall be used as a package or package seal.

H.3.3 Fungus-resistant material. External parts of the semiconductor device shall be inherently non-nutrient to fungus.

H.3.4 Metals. Internal surfaces shall be capable of resisting progressive degradation within a hermetically sealed package. External metal surfaces shall be corrosion resistant or shall be plated or treated to resist corrosion. Device package material shall be free of burrs and other potential particle contamination.

H.3.5 Screw threads. Standard screw threads listed in FED-STD-H28 shall be required for all semiconductor devices where screw threads are a mechanical requirement of the device.

H.3.6 Internal conductors. Internal conductors which are in thermal contact with a substrate along their entire lengths (such as metallization strips, contact areas, and bonding interfaces) shall be designed so that no properly fabricated conductor shall experience, at device maximum rated current, a current density in excess of the values shown below for the applicable conductor material including allowances for worst case conductor composition, cross-sectional area, normal production tolerances on critical interface dimensions, and actual thickness at critical areas, such as, steps in the elevation or contact windows:

Conductor material	Maximum allowable continuous current density (RMS for pulse applications)
Aluminum (99.99 percent pure or doped) without glassivation	2×10^5 amps/cm^2
Aluminum (99.99 percent pure or doped) with glassivation	5×10^5 amps/cm^2
Gold	6×10^5 amps/cm^2
All other (unless otherwise specified)	2×10^5 amps/cm^2

H.3.6.1 Wire bonds. Thermocompression wedge bonds shall not be utilized when aluminum wire is used.

H.3.6.2 Die mounting. Pure glass shall not be used for device die mounting.

H.3.7 Silicon transistor metallization protective coating. All silicon transistors with maximum rating of less than 4 watts at T_C of +25°C, shall have an inorganic transparent protective overlay material on the active metallization (excluding the bonding pads). For JANS (overlay structures or expanded metallization) devices, the minimum deposited glassivation thickness shall be 6,000 Å of $Si0_2$ or 2,000 Å of Si_3N_4. The glassivation shall cover all electrical conductors on the chip except the bonding pads. For JANS (overlay structures or expanded metallization) devices, a minimum of 0.050 mm (2 mils) distance shall be maintained between all uncoated conducting paths, except where the functional performance parameters of the device require closer spacing.

H.3.8 Critical interface restrictions. Unless it is part of the original design, the external surface of package, header, or flange shall be finished and not have any depression or cavity. External parts, elements, or coatings shall not blister, crack, (excluding glass meniscus), outgas, soften, flow, or exhibit defects that adversely affect storage, operation, or environmental capabilities of semiconductor devices. For JAN, JANTX, and JANTXV the use of silicone or organic material inside the packages shall be approved by the qualifying activity. Desiccants shall not be used. For JANS devices, silicone or organic materials may only be used when specified by the associated specification. Polymer impregnations (such as backfill) of the packages shall not be permitted.

WARNING: Packages containing beryllium oxide (BeO) shall be marked in accordance with 3.10.3.2 and shall not be ground, machined, sandblasted, or subjected to any mechanical operation which will produce dust containing any beryllium compound. Packages containing any beryllium compound shall not be subjected to any chemical process (such as etching) which will produce fumes containing beryllium or it's compounds.

H.3.9 Metallurgical bond for JANS axial diodes. All JANS diodes (excluding Schottky barrier and point contact ultra high frequency (UHF) devices) shall be metallurgically bonded at the interface of any mechanical connection within the assembly of the device (see appendix A for axial lead diodes).

H.3.10 Requirements for JANS transistor structure.

H.3.10.1 Front metallization thickness. The minimum front metallization thickness shall be 8,000 Å.

H.4 Package finish

H.4.1 Package finish. External metallic package elements including leads and terminals shall meet the applicable environmental requirements without additional finishing or shall be finished with a coating which conforms to one of the options listed in H4.3 and table XIII. Pure tin may not be used to coat any surface (see H 4.3.e).

H.4.2 Lead and terminal finish. In addition to the requirements of H 4.1, all leads and terminals except those intended to be attached using threaded fasteners shall be solderable in accordance with MIL-STD-750, test method 2026.

H.4.3 Detail lead finish requirements.

a. For all devices mounted by leads or terminals coated by hot solder dipping, the coating shall extend to the seating plane. For devices which are to be connected by wires soldered to lugs or other terminals not used to mount the device, the solder must cover an area extending .050 Inches (1.27 mm) in all directions beyond the designed attachment area.

b. For leads with solder applied over a surface which is not compliant with table XIII, all non-compliant material must be covered by solder to the package seal or point of lead emergence, or the lot must pass a MIL-STD-750, test method 1041 salt atmosphere test with sample size of to 22 pieces, no failures allowed. For glass-to-metal sealed products, all devices with terminals which are solder dipped to the seal shall pass screen 7 of table IV, appendix E with a sample size of 116 pieces, no failures allowed.

c. All copper or copper clad leads that are to be plated with gold or silver must first be coated with a barrier layer to prevent diffusion of the copper through the final lead finish.

d. Silver leads and silver cladding shall contain a minimum of 99.7 percent pure silver.

e. Tin based coatings shall be alloyed with a minimum of 3 percent of a second metal (e.g. Lead) which has been shown to inhibit the growth of tin whiskers.

TABLE XIII. Coating thickness and composition requirements.

Coating	Thickness microinch/micrometer		Coating composition requirements
	Minimum	Maximum 1/	
Hot solder dip (for round leads) 2/	60/1.52	NS	The solder bath shall have a nominal composition of Sn60 or Sn63. 6/
Hot solder dip (for all shapes other than round leads) 2/ 4/	200/5.08	NS	The solder bath shall have a nominal composition of Sn60 or Sn63. 3/ 6/
Tin plate (as plated) 5/	300/7.62	NS	Shall contain no more than 0.12 percent by weight co-deposited organic material measured as elemental carbon. See H.4.3.e
Tin-lead plate (as plated) 4/ 5/	200/5.08	NS	Shall consist of 3 to 50 percent by weight lead (balance nominally tin) homogeneously co-deposited. Shall contain no more than 0.12 percent by weight co-deposited organic material measured as elemental carbon.
Tin dipping 4/	100/2.54		See H.4.3.e
Gold plate	10/.254	225/5.72	Shall contain a minimum of 99.7 percent gold. Only cobalt shall be used as the hardener.
Silver plate	100/2.54	425/10.8	99.7 percent silver minimum.
Silver cladding	250		
Nickel plate (electroplate) 8/	50/1.27	350/8.89	The introduction of organic addition agents to nickel bath is prohibited. Up to 40 percent by weight cobalt is permitted as a co-deposit.
Nickel plate (electroless)	50/1.27	250/6.35	The introduction of organic addition agents to nickel bath is prohibited.
Nickel cladding 7/	50/1.27	350/8.89	

1/ NS = not specified.
2/ See H.4.3.a and H.4.3.b
3/ As measured to the center of the flat.
4/ For threaded stud packages and for terminals not intended for mounting the device only, the minimum coating thickness shall be 100 microinches/0.54 micrometers.
5/ The maximum carbon content (and minimum lead content in tin-lead plate) shall be determined by the manufacturer on at least a quarterly basis. The determination of carbon and lead content may be made by any accepted analytical technique (e.g., for carbon: Pyrolysis, infrared detection (using an IR212, IR244 infrared detector or equivalent); for lead: X-ray fluorescence, so long as the assay reflects the actual content in the total deposited finish.
6/ The solder Sn concentration in the pot may range from 50 percent Sn to 70 percent Sn.
7/ Maximum nickel thickness applies only to lead material.
8/ The maximum specified thickness applies to the final coating, provided all previously deposited nickel layers have been annealed to eliminate the residual deposition stress.

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DLA - CC

(Project 5961-2232)

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