NOTE: MIL-STD-2165A has been redesignated as a handbook, and is to be used for guidance purposes only. This document is no longer to be cited as a requirement. For administrative expediency, the only physical change from MIL-STD-2165A is this cover page. However, this document is no longer to be cited as a requirement. If cited as a requirement, contractors may disregard the requirements of this document and interpret its contents only as guidance.

NOT MEASUREMENT SENSITIVE

MIL-HDBK-2165
31 July 1995
SUPERSEDING
MIL-STD-2165A
01 February 1993

DEPARTMENT OF DEFENSE

TESTABILITY HANDBOOK FOR SYSTEMS AND EQUIPMENT

AMSC No. N6742
AREA ATTS
DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

FOREWORD

1. This military standard is approved for use by all Departments and Agencies of the Department of Defense.

2. Beneficial comments (recommendations, additions, deletions) and any pertinent data which may be of use in improving this document should be addressed to: Commander, Naval Sea Systems Command, ATTN: SEA 05Q42, 2531 National Center Bldg. 3, Washington, DC 20362-5160 by using the self-addressed Standardization Document Improvement Proposal (DD Form 1426) appearing at the end of this document or by letter.

3. Testability addresses the extent to which a system or unit supports fault detection and fault isolation in a confident, timely and cost-effective manner. The incorporation of adequate testability, including built-in test (BIT), requires early and systematic management attention to testability requirements, design and measurement.

4. This standard prescribes a systematic approach to establishing and conducting a testability program. Included are:

(a) Testability program planning
(b) Testability reviews
(c) Diagnostic concepts and testability requirements
(d) Inherent testability design and assessment
(e) Test design and assessment.

5. This standard also prescribes the integration of these testability program requirements with design and engineering functions, and with other closely related, interdisciplinary program requirements, such as reliability, maintainability and logistic support.

6. Five appendices are included to augment the tasks of this standard:

(a) Appendix A provides guidance in the selection and application of testability program tasks and depicts the interface with other engineering and logistics disciplines.
(b) Appendix B describes the inherent testability assessment which provides a measure of testability early in the design phase.
(c) Appendix C provides a glossary of terms used in this standard.
(d) Appendix D provides requirements for UUT compatibility with off-line ATE (applicable to Navy procurements only).
(e) Appendix E defines the System Synthesis Model (SSM) input data sheets as they relate to the Consolidated Automated Support System (CASS).

CONTENTS

1. SCOPE

1.1 Purpose. This standard prescribes a uniform approach to testability program planning, establishment of diagnostic concepts and testability (including BIT) requirements, testability and test design and assessment, and requirements for conducting testability program reviews.

1.2 Application. This standard is applicable to the development of all types of components, equipments, and systems for the Department of Defense. Appropriate tasks of this standard are to be applied during the Conceptual phase, Demonstration and Validation phases, Full-scale Development phase and Production phase of the system acquisition process.

1.3 Tailoring of tasks. Tasks described are intended to be tailored to the particular needs of the system or equipment acquisition program. Application guidance and rationale for selecting and tailoring tasks are included in appendix A and the associated Testability Analysis Handbook.

2. APPLICABLE DOCUMENTS

2.1 Government documents.

2.1.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DODISS) and supplement thereto, cited in the solicitation (see 6.2).

SPECIFICATION

MILITARY

MIL-H-46855 - Human Engineering Requirements for Military Systems, Equipment and Facilities.

STANDARDS

MILITARY

MIL-STD-470 - Maintainability Program for Systems & Equipment.
MIL-STD-721 - Definitions of Terms for Reliability and Maintainability.
MIL-STD-785 - Reliability Program for Systems and Equipment Development and Production.
MIL-STD-1309 - Definitions of Terms for Test, Measurement and Diagnostic Equipment.
MIL-STD-1388-1 - Logistic Support Analysis.
MIL-STD-1521 - Technical Reviews and Audits for Systems, Equipments, and Computer Software.

(Unless otherwise indicated, copies of federal and military specifications, standards, and handbooks are available from the Standardization Documents Order Desk, Bldg. 4D, 700 Robbins Avenue, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. DEFINITIONS

3.1 Definitions. The definitions included in MIL-STD-1309 and MIL-STD-721 shall apply. In addition, the definitions of appendix C are applicable.

3.2 Acronyms and abbreviations. The following acronyms and abbreviations listed in this military standard are defined as follows:

a. ATE - automatic test equipment
b. BIT - built-in test
c. BITE - built-in test equipment
d. CAD - computer-aided design
e. CDR - critical design review
f. CDRL - contract data requirements list
g. CI - configuration item
h. CND - cannot duplicate
i. CE - concept exploration
j. DID - data item description
k. D&V - demonstration and validation
l. ED/M - engineering development and manufacturing
m. EO - electro-optical
n. FMEA - failure modes and effects analysis
o. FMECA - failure modes and effects criticality analysis
p. FQR - formal qualification review
q. ID - interface device
r. I/O - input or output
s. ILSMT - integrated logistic support management team
t. LSA - logistic support analysis
u. MSCM - mechanical systems condition monitoring
v. P/D - production and deployment
w. PDR - preliminary design review
x. RF - radio frequency
y. ROM - read only memory
z. SDR - system design review
aa. T&E - test and evaluation
bb. TPS - test program set
cc. TRD - test requirements document
dd. UUT - unit under test

4. GENERAL REQUIREMENTS

4.1 Scope of testability program. This standard is intended to define and facilitate interdisciplinary efforts required to develop testable systems and equipments. The testability program scope includes:

(a) Support of an integrated diagnostic concept, whereby all elements associated with effective and efficient diagnostics are planned for, and integrated into, a cohesive fielded capability which satisfies weapon system mission and performance requirements.
(b) Support of, and integration with, maintainability design, including requirements for performance monitoring and corrective maintenance action at all levels of maintenance.
(c) Support of integrated logistic support requirements, including the support and test equipment element and other logistic elements.
(d) Support of, and integration with, design engineering requirements, including the hierarchical development of testability designs from the piece part to the system levels.

4.2 Testability program requirements. A testability program shall be established which accomplishes the following general requirements:

(a) Development of a testability program plan.
(b) Establishment of sufficient, achievable, and affordable diagnostic concept and testability built-in and off-line test performance requirements.
(c) Integration of testability into equipments and systems during the design process in coordination with the maintainability design process.
(d) Evaluation of the extent to which the design meets testability requirements.
(e) Inclusion of testability in the program review process.

4.3 Application of requirements. Detailed testability requirements described in this standard are to be selectively applied and are intended to be tailored, to particular systems and equipment acquisition programs. Appendix A provides rationale and guidance for the selection and tailoring of testability program tasks.

5. DETAILED REQUIREMENTS

5.1 Task descriptions. Individual task requirements are provided for the establishment of a testability program for system and equipment acquisition. The tasks are categorized as follows:

TASK SECTION 100. PROGRAM MONITORING AND CONTROL

Task 101 Testability Program Planning
Task 102 Testability Reviews

TASK SECTION 200. DESIGN AND ANALYSIS

Task 201 Diagnostic Concepts and Testability Requirements
Task 202 Inherent Testability Design and Analysis Assessment
Task 203 Test Design and Assessment

5.2 Task integration. The individual task requirements provide for integration with other specified engineering and management tasks to preclude duplication and overlap, while ensuring timely consideration and accomplishment of testability requirements.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory.)

6.1 Intended use. This standard is intended to prescribe a systematic approach to establishing and conducting a testability program for systems and equipments.

6.2 *Issue of DODISS*. *When this standard is used in acquisition,* the applicable issue of the DODISS must be cited in the solicitation (see 2.1.1).

6.3 Data requirements. The following Data Item Descriptions (DID's) must be listed, as applicable, on the Contract Data Requirements List (DD Form 1423) when this standard is applied on a contract, in order to obtain the data, except where DOD FAR Supplement 27.475-1 exempts the requirement for a DD Form 1423.

Reference Paragraph	DID Number	DID Title	Suggested Tailoring
Task 101.1	DI-ATTS-81270	Testability program plan	---
Task 102.1	DI-E-5423	Design review data package	Equivalent DID may be used
Task 201.4.1	DI-ATTS-81271	Testability requirements analysis report	---
Task 202.4.2 and 202.4.4	DI-ATTS-81272	Inherent testability design and assessment report	---
Task 203.4.3, 203.4.4, and 203.4.6	DI-ATTS-81273	Test design and assessment report	---
Appendix D 50.2.1	DI-ATTS-81291	Compatibility Problem Report	---
Appendix D 50.3	DI-ATTS-81292	UUT Input/Output Description	---

The above DID's were those cleared as of the date of this standard. The current issue of DoD 5010.12-L, Acquisition Management Systems and Data Requirements Control List (AMSDL), must be researched to ensure that only current, cleared DID's are cited on the DD Form 1423.

6.4 Subject term (key word) listing.

Diagnostics
Diagnostic requirements
Diagnostic testing
Embedded test
External test
Fault detection
Fault isolation
Test assessment
Test design

6.5 Changes from previous issue. Marginal notations are not used in this revision to identify changes with respect to the previous issue due to the extensiveness of the changes.

Custodians:
Army - CR
Navy - SH
Air Force - 17

Preparing activity:
Navy - SH
(Project ATTS-8904)

TASK SECTION 100

PROGRAM MONITORING AND CONTROL

TASK 101

TESTABILITY PROGRAM PLANNING

101.1 PURPOSE. To plan for a testability program which will identify and integrate all testability and test design management tasks required to accomplish program requirements, as specified in a testability program plan (see 6.3).

101.2 TASK DESCRIPTION.

101.2.1 Identify a single organizational element within the performing activity which has overall responsibility and authority for implementation of the testability program. Establish analyses and data interfaces among the organizational elements responsible for each of the elements of the diagnostic capability.

101.2.2 Establish a procedure by which testability requirements are based on mission needs and system performance requirements and are traceable throughout the design process and are integrated with other design requirements, and how these requirements are disseminated to design personnel and subcontractors. Establish controls for ensuring that each subcontractor's testability practices are consistent with overall system or equipment requirements.

101.2.3 Identify testability design guides and analysis models and procedures to be imposed upon the design process. Plan for the review, verification, and utilization of testability data submissions.

101.2.4 Describe the approach to be used for establishing vertical test traceability to ensure compatibility of testing among all levels of testing, including factory testing. The approach must address both the compatibility of testing tolerances among levels and the compatibility of testing environments.

101.2.4.1 Describe the approach to be used to identify high-risk diagnostic technology applications and to provide procedures to lower these risks.

101.2.4.2 Describe the approach to be used to ensure integration and compatibility between testability and other diagnostic elements (that is, technical information, personnel, and training) and among all levels of maintenance.

101.2.4.3 Define the means for demonstrating and validating that the diagnostic capability meets specified requirements, using maintainability demonstrations, test program verification, and other demonstration methods.

101.2.4.4 Define an approach and methodology to ensure that as test and evaluation of the system progresses, problems presented by new failure modes, test voids, ambiguities, and test tolerance difficulties are recognized and defined, and solutions are traceable to diagnostic hardware and software, and manual procedures updates.

101.2.4.5 Define an approach for the analysis of production and acceptance test and evaluation results to determine how BIT hardware and software, ATE hardware and software, and maintenance documentation performed as a means for satisfying production testing, as well as meeting testability requirements.

101.2.4.6 Establish procedures to analyze maintenance actions for fielded systems to determine if the diagnostic capability is performing within specified requirements and take corrective measures. Define data collection requirements to conduct these analyses. Data collection shall be integrated with similar data collection procedures, such as those for reliability and maintainability and logistic support analysis and shall be compatible with specified data systems in use by the military user organizations.

101.2.5 Develop a testability program plan which describes how the testability program will be conducted. The plan must also include the time phasing of each task and relationships to other tasks. Diagnostic issues which relate to reliability, maintainability, logistics, human engineering, safety, and training shall also be addressed in those individual plans.

101.3 TASK INPUT.

101.3.1 Identifications of each task which is required to be performed as part of the program.*

101.3.2 Identification of the time period over which each task is to be conducted.*

101.3.3 Identification of approval procedures for plan updates.*

101.3.4 Identification of deliverable data items.*

101.3.5 Identification of items to be demonstrated.*

101.3.5.1 Identification of existing maintenance data collection systems in use by the using command.*

101.4 TASK OUTPUT.

101.4.1 Testability program plan if specified as a stand-alone plan. When required to be a part of another engineering or management plan, such as the Systems Engineering Management Plan (SEMP), use the appropriate, specified DID.

* To be specified by the requiring authority.

TASK 102

TESTABILITY REVIEWS

102.1 PURPOSE. To establish a requirement for the performing activity to (1) provide for all official review of testability design information in a timely and controlled manner, and (2) conduct in-process testability design reviews at specified dates to ensure that the program is proceeding in accordance with the contract requirements and program plans (see 6.3).

102.2 TASK DESCRIPTION.

102.2.1 Include the formal review and assessment of the testability program as an integral part of each system program review (such as system design review, preliminary design review, critical design review, etc.) specified by the contract. Reviews shall cover all pertinent aspects of the testability program such as:

(a) Status and results of testability-related tasks.
(b) Documentation of task results.
(c) Testability-related requirements in specifications.
(d) Testability design, cost, or schedule problems.

102.2.2 Conduct and document testability design reviews with performing activity personnel, subcontractors, and suppliers. Coordinate and conduct these reviews in conjunction with reliability, maintainability, and logistic support reviews whenever possible. Inform the requiring authority in advance of each review. Utilize MIL-STD-1521 and program review criteria contained in MIL-STD-470, MIL-STD-785, and MIL-STD-1388-1. Design reviews shall cover all pertinent aspects of the design, such as the following:

(a) Review the impact of the selected diagnostic concept on readiness, life cycle costs, manpower, and training.
(b) Review performance monitoring, built-in test, off-line test and maintenance aid performance requirements and constraints to ensure that they are complete and consistent.
(c) Review the rationale for the inherent testability criteria and weighting factors selected.
(d) Review the testability techniques employed by the design groups. Identify design guides or procedures used. Describe any testability analysis procedures or automated tools to be used.
(e) Review the extent to which testability criteria are being met. Identify any technical limitations or cost considerations inhibiting full implementation.
(f) Review adequacy of failure mode data as a basis for test design. Assess adequacy of testability/FMEA data interface.
(g) Review integration among BIT hardware, BIT software, and operational software efforts. Review BIT interface to operator and maintenance personnel.

(h) Review BIT fault detection and fault isolation measures to be used. Identify models used and model assumptions. Identify any methods to be used for automatic test generation and test grading.

(i) Review BIT fault detection and fault isolation performance to determine if BIT specifications are met. Review efforts to improve BIT performance through improved tests or item redesign. Assess adequacy of testability/maintainability data interfaces.

(j) Review testability parameters to be included in the maintainability demonstration. Identify procedures by which testability concerns are included in demonstration plans and procedures.

(k) Review compatibility of signal characteristics at test points with planned test equipment. Assess adequacy of data interface between testability and support and test equipment organizational elements.

(l) Review completeness and consistency of performance monitoring, BIT and off-line test performance.

(m) Review approach and methodology to ensure that as test and evaluation of the system progresses, problems presented by new failure modes, test voids, ambiguities, and test tolerance difficulties are recognized and defined and solutions are traceable to diagnostic software and manual procedures updates.

(n) Review approaches to monitoring production testing and field maintenance actions to determine fault detection and fault isolation effectiveness.

(o) Review plans for evaluating impact on the diagnostic capability for engineering change proposals.

102.3 TASK INPUT.

102.3.1 Identification of amount of time to be devoted to the testability program at each formal review and the level of technical detail to be provided.*

102.3.2 Identification of level of participation desired by the requiring authority in internal and subcontractor design reviews.*

102.4 TASK OUTPUT.

102.4.1 Results of testability assessments as an integral part of system program review documentation (see 102.2.1).

102.4.2 Results of testability design reviews, including action items pending (see 102.2.2).

* To be specified by the requiring authority.

TASK SECTION 200

DESIGN AND ANALYSIS

TASK 201

DIAGNOSTIC CONCEPTS AND TESTABILITY REQUIREMENTS

201.1 PURPOSE. To evaluate alternative diagnostic concepts and (1) recommend system test and testability requirements which best implement selected diagnostic concepts and (2) allocate those requirements to subsystems and items.

201.2 TASK DESCRIPTION.

201.2.1 Derive and establish system-level diagnostic needs. This includes:

(a) Identifying those system mission and performance requirements which directly require diagnostic functions (such as, safety, mission critical).
(b) Translating those system mission and performance requirements into diagnostic needs which support the mission scenario and system design and conform to the system's operational constraints.

201.2.2 Derive alternative diagnostic concepts which satisfy mission requirements and provide a complete (100 percent) diagnostic capability at each level of maintenance. Include for each level of maintenance varying degrees of BIT, manual and automatic testing, technical information delivery, personnel skill levels, and training concepts, along with deferred, preventive, and scheduled maintenance concepts. Considerations include:

(a) Identification of standard, existing, or planned, or existing and planned diagnostic resources (such as, family of testers, maintenance aids) that have potential benefits. Identify resource limitations.
(b) Identification of diagnostic problems on similar systems which should be avoided.
(c) Identification of technology advancements that can be exploited in system development and diagnostic element development which have the potential for increasing diagnostic effectiveness, reducing diagnostic costs, or enhancing system availability.

201.2.3 Evaluate alternative diagnostic capability concepts. Identify the selected diagnostic concept. The evaluation shall include:

(a) A determination of the sensitivity of system readiness parameters to variations in the diagnostic mix and to variations in key testability/diagnostic parameters.
(b) A determination of the sensitivity of life cycle costs to variations in the key testability/diagnostic parameters, mix, and placement of diagnostic resources.
(c) An estimation of the impact of alternative diagnostic concepts on direct maintenance man-hours per operating hour, job classifications, skill levels, or other diagnostic measures, required at each level of maintenance.

(d) An estimation of risk associated with each concept.

201.2.4 Recommend system-level fault detection and isolation requirements for inclusion in system specifications, including those requirements addressed in paragraph 201.3.4.

201.2.5 Allocate system-level testability requirements to configuration item specifications based on reliability, criticality considerations, technology risks, and the potential efficiency and effectiveness of the diagnostic capability. Allocation shall address all diagnostic elements which constitute the diagnostic capability (that is, test, technical information, and personnel).

201.2.6 Recommend off-line test fault detection and isolation requirements for each item designated as a unit under test for inclusion in CI development specifications.

201.3 TASK INPUT.

201.3.1 Mission and performance requirements and operational constraints from weapon system statement of need and MIL-STD-1388-1, task 201. (Needed for 201.2.1)

201.3.2 Supportability analysis data in accordance with MIL-STD-1388-1 (201 through 204 and 301 and 302) or other method approved by the requiring authority. (Needed for 201.2.2)

201.3.3 Reliability allocation from task 202 of MIL-STD-785. (Needed for 201.2.5)

201.3.4 Specific numeric diagnostic and testability requirements not subject to requirements trade-offs.* (Needed for 201.2.1, 201.2.4, and 201.2.5)

201.3.5 Human engineering analysis and requirements, such as from MIL-H-46855. (Needed for 201.2.2, 201.2.3, and 201.2.5)

201.4 TASK OUTPUT.

201.4.1 Description of selected diagnostic capability tradeoff methodology, evaluation criteria, models used, and analysis results (see 201.2.3 and 6.3).

201.4.2 Recommended diagnostic and testability monitoring requirements for system specification (see 201.2.4 and 201.2.5).

201.4.3 Recommended diagnostic and testability requirements for each configuration item specification (see 201.2.6).

* To be specified by the requiring authority.

TASK 202

INHERENT TESTABILITY DESIGN AND ASSESSMENT

202.1 PURPOSE. To incorporate testability design practices into the design of a system or equipment early in the design phase and to assess the extent to which testability is incorporated.

202.2 TASK DESCRIPTION.

202.2.1 Institute testability design concepts as an integral part of the system or equipment design process.

202.2.2 Incorporate appropriate testability design concepts into the preliminary design for each item. Provide inputs to system engineering on the impact of system architecture alternatives on inherent diagnostic capability. Recommend diagnostic architecture considerations, such as testability bus, system-level BIT, onboard diagnostic data collection, and sensor locations.

202.2.3 Select testability design criteria from appendix B to be implemented in the design. Tailor criteria and add new criteria for the specific design. Include criteria for UUT compatibility with off-line ATE.

202.2.4 Analyze and evaluate the selected testability concepts of the system or equipment design in a qualitative manner to ensure that the design will support the required level of testing. Conduct an analysis of the inherent (intrinsic) testability of the design. The analysis identifies the presence or absence of hardware features which facilitate testing and identifies problem areas. The method of appendix B shall be applied to each item identified for inherent testability assessment by the requiring authority. Methods, such as dependency modeling analysis of the design, can be utilized to optimize test point placement and partitioning strategies.

202.2.5 Modify the design, until the inherent testability equals or exceeds the threshold value. If achieving the threshold is not possible or cost effective, but fault detection and fault isolation requirements can be met, supporting data shall be prepared.

202.3 TASK INPUT.

202.3.1 System or equipment design data.

202.3.2 Identification of items to be included in inherent testability analysis (see appendix B).*

202.3.3 For each item included, the inherent testability threshold value to be achieved.* Guidance for establishing a threshold value is given in appendix B, 50.2.4.1.

202.4 TASK OUTPUT.

202.4.1 Testability features integrated into system or equipment design (see 202.2.1, 202.2.2, and 202.2.4).

202.4.2 Description of testability design tradeoffs and testability features selected for implementation (see 202.2.2, 202.2.4, and 6.3).

202.4.3 For each item included, assignment of a weighting factor and scoring method for each testability criterion (see appendix B and 202.2.3).

202.4.4 Inherent testability assessment (see 202.2.3 and 6.3).

* To be specified by the requiring authority.

TASK 203

TEST DESIGN AND ASSESSMENT

203.1 PURPOSE. To design the embedded and external test capability for a system or equipment which will satisfy testability performance requirements; to assess the level of test effectiveness which will be achieved for a system or equipment design; and to ensure effective integration and compatibility of this test capability with other diagnostic elements.

203.2 TASK DESCRIPTION.

203.2.1 Incorporate testability, including built-in test, into the detailed design for each item.

203.2.2 Identify and define the methodology to be used for predicting fault detection and fault isolation performance levels at the system test level and the item test level.

203.2.3 Analyze the prime system design to ensure that all system-level functions are exercised by testing (such as, BIT, performance monitoring) to the extent specified, and that the testing function has been effectively integrated with other system-level diagnostic resources (such as, maintenance aids, technical publications). Ensure that performance monitoring functions and display formats provide the operator with appropriate information. Particular attention should be given to the separation of hardware faults from software problems.

203.2.4 Develop system-level BIT hardware and software, integrating the built-in test capabilities of each subsystem/item.

203.2.5 Predict the level of BIT fault detection for the overall system based on the BIT detection predictions, weighted by failure rate, of the individual items, including Government-furnished equipment (GFE). Predict the level of fault isolation for the overall system provided by system-level test.

203.2.6 Conduct an analysis of the test effectiveness of shop tests for each CI and for each physical partition of the CI designated at a UUT. Item built-in test and external ATE tests shall be included in this analysis. Ensure that the testing function has been effectively integrated with other shop diagnostic resources (such as, technical publication, management information systems).

203.2.7 For both system-level and shop-level analyses:

(a) Identify the failures of each component and the failures between components which correspond to the specific failure modes for each item to be tested. These failures represent the predicted failure population and are the basis for test derivation (BIT and off-line test) and test effectiveness evaluation. Maximum use shall be

made of a failure modes and effects analysis (FMEA) from Task 204 of MIL-STD-470, if a FMEA is required. The FMEA requirements may have to be modified or supplemented to provide the level of detail needed.

(b) Model components and interconnections for each item so that the predicted failure population may be accurately modeled. The performing activity shall develop or select models which are optimum, considering accuracy required, cost of test generation and simulation, standardization, and commonality. Analyze and evaluate UUT compatibility with off-line ATE. (Appendix D provides requirements for off-line ATE compatibility).

(c) Analyze and evaluate the effectiveness of planned testing based on the predicted failure population. The analysis shall give particular emphasis to fault detection and fault isolation for critical and high failure rate items and interconnections. The test effectiveness data shall be used to guide redesign of equipment and test programs, as required, and to assist in the prediction of spares requirements.

(d) Prepare justification for any classes of faults which are poorly isolated, when using the developed test stimuli, and submit to the requiring authority for review. Prepare additional or alternative diagnostic approaches. Identify hard-to-test-faults to the LSA process.

203.2.8 Iterate the design of the item built-in test until each predicted test effectiveness value equals or exceeds the specified value.

203.2.9 Iterate the design of the item external test until each predicted test effectiveness value equals or exceeds the specified value.

203.2.10 Assemble cost data associated with BIT and design for testability on a per unit basis (such as, additional hardware, increased modularity, and additional connector pins). Extract and summarize cost data associated with the implementation of the testability program, test generation efforts, and production test. Provide test effectiveness predictions as inputs to maintainability and logistic tasks.

203.2.11 Implement procedures for vertical test traceability to ensure compatibility of testing among all levels of testing, including factory testing. These procedures shall address both the compatibility of testing tolerances among levels and the compatibility of testing environments.

203.3 TASK INPUT.

203.3.1 Identification of items to be included in test effectiveness predictions.*

203.3.2 System or item design data.

203.3.3 BIT and external test requirements.

203.3.4 Identification of failure modes and failure rates for each item from task 204 of MIL-STD-470.

203.3.5 Test effectiveness data for GFE.*

203.3.6 Corrective action recommendations from the maintainability demonstration.

203.4 TASK OUTPUT.

203.4.1 Built-in test features integrated into the system or item design which meet testability and maintainability requirements. (203.2.1, 203.2.4, 203.2.5)

203.4.2 Description of methodologies, models, and tools to be used in item and system test effectiveness predictions (see 203.2.1).

203.4.3 Description of built-in test and testability features for each item designed as a UUT, in appropriate test requirements document (see 203.2.1).

203.4.4 Test effectiveness prediction for each item: data provided in support of task 205 of MIL-STD-470 and task 401 of MIL-STD-1388-1 (see 203.2.5, 203.2.6, and 6.3).

203.4.5 System test effectiveness prediction from information provided in support of task 205 of MIL-STD-470 (see 203.2.4, 203.2.7 and 6.3).

203.4.6 Description of vertical test traceability and design integration (see 203.2.11 and 6.3).

* To be specified by the requiring authority.

APPENDIX A

TESTABILITY PROGRAM GUIDANCE

CONTENTS

APPENDIX A

CONTENTS - (Continued)

APPENDIX A

TESTABILITY PROGRAM GUIDANCE

10. SCOPE

10.1 Purpose. This appendix provides rationale and guidance for the selection and tailoring of tasks to define a testability program which meets established program objectives. No contractual requirements are contained in this appendix. This appendix is not a mandatory part of the standard. The information contained herein is intended for guidance only.

20. APPLICABLE DOCUMENTS

20.1 Government documents.

20.1.1 Specifications and standards. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DODISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

MILITARY

MIL-H-46855 - Human Engineering Requirements for Military Systems, Equipment and Facilities

STANDARD

MILITARY

MIL-STD-882 - System Safety Program Requirements

(Unless otherwise indicated, copies of federal and military specifications, standards, and handbooks are available from the Standardization Documents Order Desk, Bldg. 4D, 700 Robbins Avenue, Philadelphia, PA 19111-5094.)

20.1.2 Other Government documents, drawings, and publications. The following other Government documents, drawings, and publications form a part of this document to the extent specified herein. Unless otherwise specified, the issues are those cited in the solicitation.

NAVMATP 9405 Joint Service Built-In Test Design Guide.
DARCOM 34-1
AFLCP 800-39
AFSCP 800-39
NAVMC 2721, 19 March 1981

TECHNICAL REPORTS

Rome Air Development Center September 1990 RADC-TR-90-239	Testability/Diagnostic Design Encyclopedia
Rome Air Development Center December 1979 RADC-TR-79-309	*BIT/External Testing Figures of* Merit and Demonstration Techniques

30. DEFINITIONS

30.1 Definitions. The definitions included in MIL-STD-1309, MIL-STD-721, and appendix C shall apply.

40. GENERAL APPLICATION GUIDANCE

40.1 Task selection criteria. The selection of tasks which can materially aid the attainment of testability requirements is a difficult problem for both Government and industry organizations faced with severe funding and schedule constraints. This appendix provides guidance for the selection of tasks based upon identified program needs. Once appropriate testability program tasks have been selected, each task shall be tailored in terms of timing, comprehensiveness and end products to meet the overall program requirements.

MIL-STD-2165 is a programmatic standard which defines the task requirements for conducting a testability program within a system or equipment development program. MIL-STD-2165 is comprised of a series of tasks which may be selectively applied, for the specific system being developed and the phase of development. The tasks include program administration and control tasks and design and analysis tasks. Each task has a number of subtasks. These subtasks are the key to the tailoring of the testability program. Subtasks may be called out in statements of work. This defines the work to be accomplished within the testability program.

40.2 System testability program (see figure 1). For major systems, the testability tasks for each program phase are summarized in table I and listed below.

(a) Concept exploration phase.

(1) Develop testability program plan (see task 101).
(2) Establish system-level fault detection and isolation requirements (see task 201).
(3) Conduct testability reviews, as part of system requirements review (see task 102).

(b) Demonstration and validation phase.

(1) Develop testability program plan (see task 101).
(2) Allocate diagnostic requirements (see task 201).
(3) Impose testability design discipline (see task 202).
(4) Conduct testability reviews as part of system design reviews (see task 102).

(c) Full-scale development phase.

(1) Develop testability program plan (see task 101).
(2) Incorporate testability features into full-scale development items and evaluate effectiveness (see task 202 and 203).
(3) Conduct testability reviews as part of preliminary and critical design reviews (see task 102).
(4) Ensure compatibility of diagnostic elements (see task 203).

(d) Production and Deployment Phase

(1) Collect data on achieved testability effectiveness.
(2) Take corrective action.

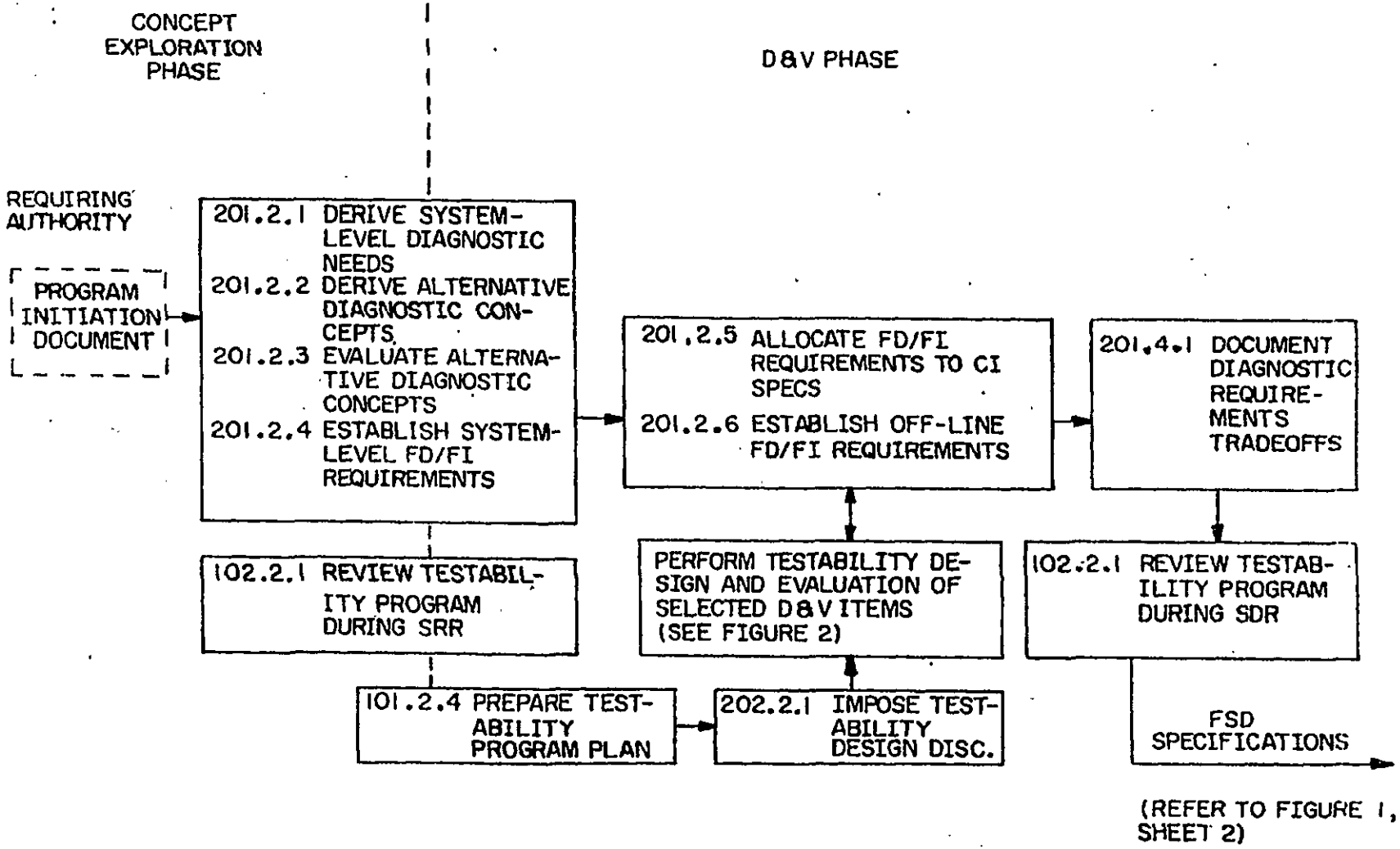

FIGURE 1. System testability program flow diagram.

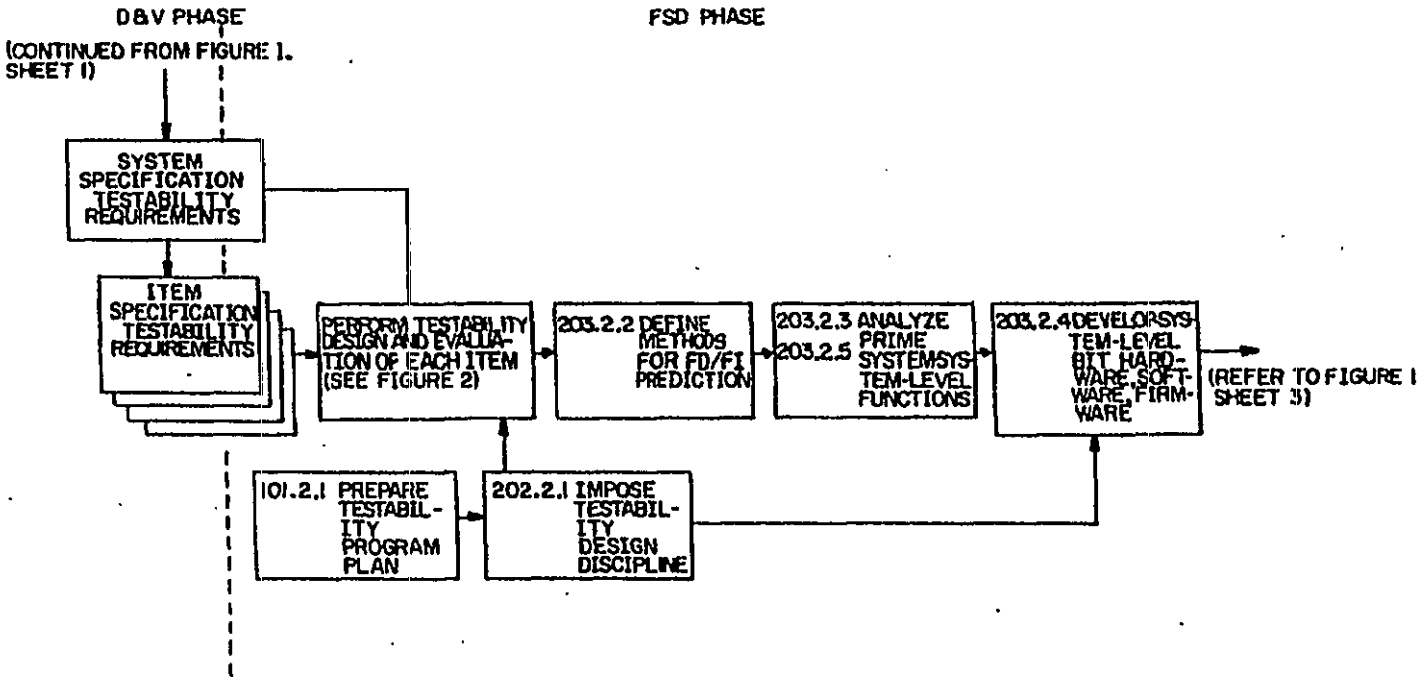

FIGURE 1. System testability program flow diagram - Continued.

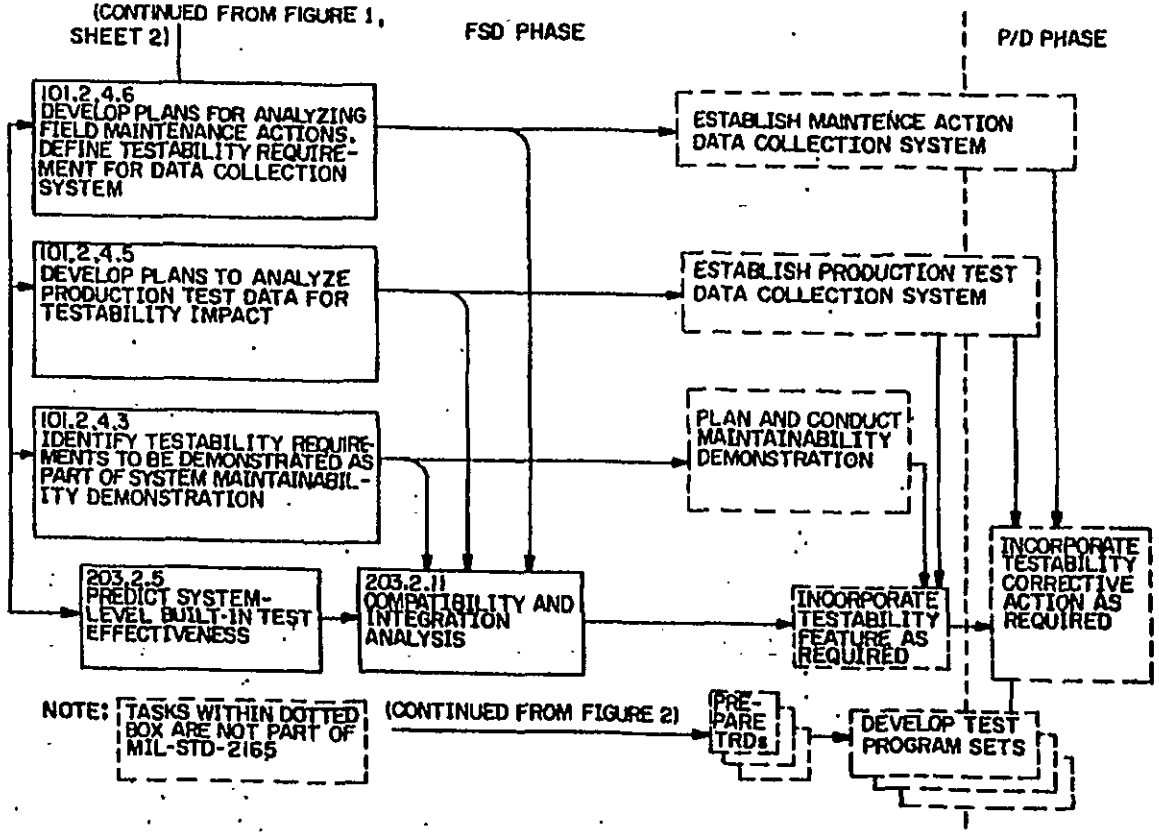

FIGURE 1. System testability program flow diagram - Continued.

TABLE I. Task application guidance matrix.

TASK		PROGRAM PHASE			
		CE	D&V	ED/M	P/D
101	Testability program planning	G	G	G	N/A
102	Testability reviews	G	G	G	S
201	Diagnostic concepts and testability requirements	G	G	G	N/A
202	Inherent testability design and assessment	N/A	S	G	S
203	Testability detail design and analysis assessment	N/A	S	G	S

N/A - Not applicable
G - Generally applicable
S - Electively applicable to high-risk items during D&V, or to design changes during P/D

CE - Concept exploration
D&V - Demonstration and validation
ED/M - Engineering development and manufacturing
P/D - Production/Deployment

40.3 Item testability program (see figure 2). For all items, whether developed as a subsystem under a system acquisition program or developed under an equipment acquisition program, the testability tasks are listed below:

(a) Preliminary design.

(1) Develop testability program plan, if a plan was not developed as part of a system acquisition program (see task 101).
(2) Incorporate testability features into preliminary design (see task 202).
(3) Develop inherent testability checklist for each item (see task 202).
(4) Conduct testability review as part of preliminary design review (see task 102).

(b) Detail design.

(1) Predict inherent testability for each item (see task 202).
(2) Incorporate testability features into detail design (see task 203).
(3) Predict test effectiveness for each item (see task 203).
(4) Conduct testability review as part of the critical design review (see task 102).

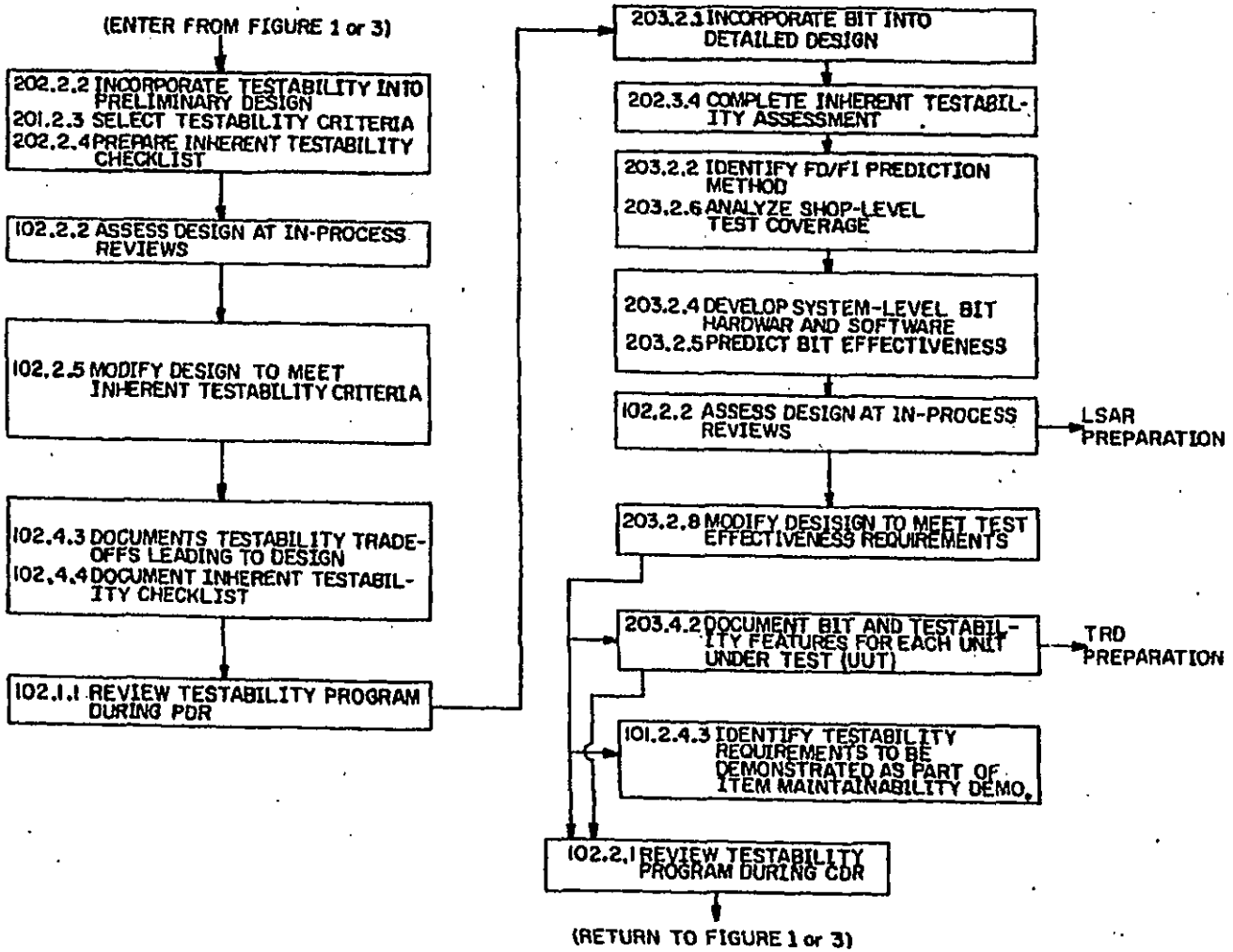

FIGURE 2. Item testability design detailed flow diagram.

40.4 Criteria for imposing a testability program during the D&V phase. During D&V phase, a formal testability program should be applied to the system integration effort and, in addition, shall be selectively applied to those subsystems which present a high risk in testing. The high risk aspect of test design may be a result of:

(a) A criticality of function to be tested,
(b) Difficulty of achieving desired test quality at an affordable cost,
(c) Difficulty of defining appropriate testability measures or demonstrations for technology being tested,
(d) Large impact on maintainability if expected test quality, automation, throughput, and other requirements, are not achieved, or
(e) High probability that modifications to the subsystem during ED/M will be limited.

40.5 Equipment testability program (see figure 3). For the acquisition of less-than-major systems or individual equipments, the testability tasks are listed below.

(a) Establish system or equipment testability requirements. (Performed by requiring authority using the process defined in task 201.)
(b) Develop testability program plan (see task 101).
(c) Incorporate testability features into items and evaluate effectiveness (see 40.3).
(d) Collect data on achieved testability effectivenesss (performed by requiring authority using figure 1, sheet 3 as guidance).

40.6 Iterations. Certain tasks contained in this standard are highly iterative in nature and recur at various times during the acquisition cycle, proceeding to lower levels of hardware indenture and greater detail in the classical systems engineering manner.

50. DETAILED APPLICATION GUIDANCE

This section provides detailed guidance for conducting each testability task.

50.1 Task 101, testability program planning.

50.1.1 Scope. The testability program plan is the basic tool for establishing and executing an effective testability program. The testability program plan should document what testability tasks are to be accomplished, how each task will be accomplished, when they will be accomplished, and how the results of the task will be used. The testability program plan may be a stand-alone document, but preferably should be included as part of the systems engineering management plan (SEMP), if one is required. Plans assist the requiring authority in evaluating the prospective performing activities approach to, and understanding of, the testability task requirements and the organizational structure for performing testability tasks. The testability program plan should be closely coordinated with the maintainability program plan and the LSA plan.

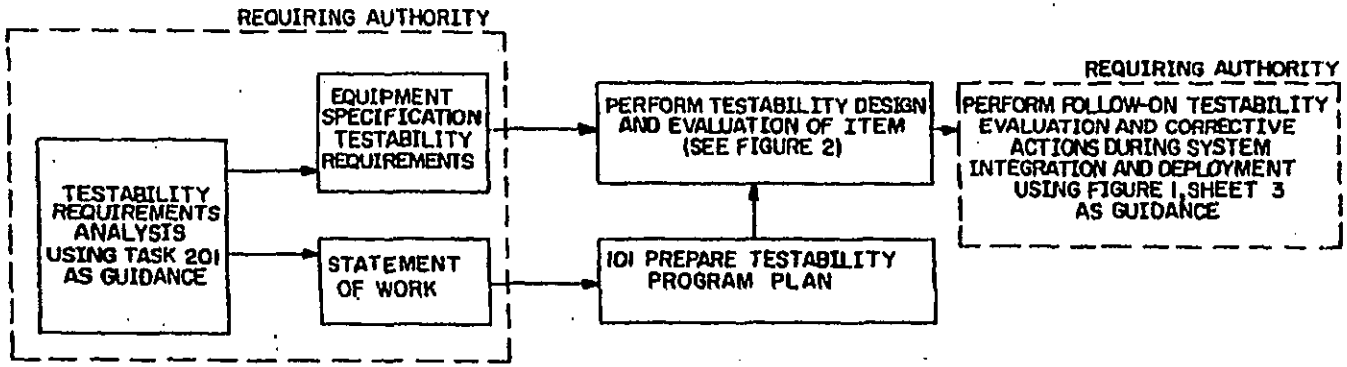

FIGURE 3. Equipment testability program flow diagram.

50.1.2 Submission of the plan. When requiring a testability program plan, the requiring authority should allow the performing activity to propose specifically tailored tasks with supporting rationale to show overall program benefits. The testability program plan should be a dynamic document that reflects current program status and planned actions. Accordingly, procedures shall be established for updates and approval of updates by the requiring authority when conditions warrant. Program schedule changes, test results, or testability task results may dictate a change in the testability program plan, in order for it to be used effectively as a management document.

50.1.3 Plan phases. The testability program plan is prepared or revised during each of the acquisition phases. During the concept exploration phase, the plan shall describe the methodology to be used in establishing the diagnostic concept and system-level diagnostic needs. During the demonstration and validation phase, the plan should address how these diagnostic needs will be translated into testability requirements and, subsequently allocated down to subsystem and configuration item levels. In addition, the plan shall describe testability activities which will take place during the later acquisition phases. This includes methods for establishing procedures which will ensure compatibility and integration of all diagnostic elements and means for demonstrating, testing, and evaluating the performance of the diagnostic capability. Finally, the plan should describe a method for identifying and tracking testability-related problems during the latter stages of full-scale development and system production/ deployment. In all cases, sufficient data shall be furnished to the Government to permit a meaningful evaluation of testing and testability alternatives. The testability program plan should indicate how the flow of information is to be accomplished through informal customer reviews, through CDRL data submissions, and through testability reviews.

50.1.4 Organizational interfaces. In order to establish and maintain an effective testability program, the testability manager shall form a close liaison with all design disciplines, including BIT software design. In satisfying system support requirements, the prime system design shall be treated as one of the elements which may be traded off through the supportability analysis process. As a result, the testability manager shall be prepared to work aggressively with design engineers to ensure a proper balance between performance, cost, and supportability. It is not efficient nor effective for the testability manager to assume the role of post-design critic and risk large cost and schedule impacts. The testability influence must be apparent from the initiation of the design effort, through design guidelines, training programs, and objective measures.

50.1.5 Testability effectiveness tracking. A testability program cannot be totally effective unless provisions are made for the systematic tracing and evaluation of testability effectiveness beyond the system development phase. The objective is to plan for the evaluation of the impact of actual operational maintenance environments on the ability of production equipment to be tested. The effectiveness of testability design techniques for intermediate or depot level maintenance tasks is monitored and analyzed as part of this evaluation. Much of the actual collection and analysis of data and resulting corrective actions may

occur beyond the end of the contract under which the testability program is imposed and may be accomplished by personnel other than those of the performing activity. Still, it is essential that the planning for this task be initiated early in the program.

Most test implementations, no matter how well conceived, require a period of time for identification of problems and corrective action to reach specified performance levels. This "maturing" process applies equally to BIT and off-line test. This is especially true in setting test tolerances for BIT and off-line test used to test analog parameters. The setting of test tolerances to achieve an optimum balance between failure detection and false alarms usually requires the logging of considerable test time. It should be emphasized, however, that the necessity for "fine-tuning" a test system during production and deployment in no way diminishes the requirement to provide a "best possible design" during the full-scale development phase. One way of accelerating the test maturation process is to utilize planned field or depot testers for portions of the acceptance test. BIT test hardware and software should be exercised for those failures discovered and the BIT effectiveness documented and assessed.

50.2 Task 102, testability review.

50.2.1 Type of review. This task is directed toward two types of review: (1) formal system program reviews (see subtask 102.2.1) and (2) review of design information within the performing activity from a testability standpoint (see subtask 102.2.2). The second type provides testability specialists with the authority to manage design tradeoffs. For most developers, this type of review is a normal operating practice. Procedures for this type of review would be included in the testability program plan.

50.2.1.1 Program reviews. System program reviews, such as the preliminary design review and the critical design review, are important management and technical tools of the requiring authority. They should be specified in statements of work to ensure adequate staffing and funding and are held during an acquisition program to evaluate overall program process, consistency, and technical adequacy. An overall testability program status should be an integral part of these reviews, whether conducted with subcontractors or with the requiring authority.

50.2.1.2 Testability design reviews. Testability design reviews are necessary to assess the progress of testability design in greater technical detail and at a greater frequency than is provided by system program reviews. The reviews shall ensure that the various organizational elements within the performing activity which impact, or are impacted by, testability are represented and have an appropriate degree of authority in making decisions. The results of the performing activity's internal and subcontractor system reviews shall be documented and made available to the requiring authority on request. These reviews shall be coordinated, whenever possible, with maintainability, ILSMT, and program management reviews.

50.2.2 Additional data review. In addition to formal reviews, useful information can often be gained from performing activity data which is not submitted formally, but which can be made available through an accession list. A data item for this list shall be included in the CDRL. This list is a compilation of documents and data which the requiring authority can order, or which can be reviewed at the performing activity's facility.

50.3 Task 201, diagnostic concept and testability requirements.

The purpose of task 201 is to evaluate alternative diagnostic concepts and recommend test and testability requirements which best implement this diagnostic concept and allocate these requirements to subsystems and items.

Task 201 is implemented in the early phases of system development (concept exploration and demonstration and validation phases), while the operational support requirements of the system are being firmed-up, traded-off, analyzed, and optimized in relation to each other. Testability considerations and impacts are an integral part of this analysis process. The impact of various testability alternatives on mission capability, performance parameters, support costs, and effectiveness shall be evaluated. Testability performance parameters (fault detection and isolation levels) and the diagnostic resource mix shall be evaluated with respect to overall system goals. A diagnostic concept is developed for the system, which considers an embedded as opposed to an external diagnostic capability and the resources required at all levels of maintenance. The impact of various diagnostic concepts are evaluated in terms of the impact on manpower and personnel requirements, and life cycle costs. The results, or output, of task 201 are testability requirements suitable for inclusion in system and configuration item specifications. Based on these specified requirements, the design effort incorporates testability features to meet these requirements (see tasks 202 and 203).

Task 201 addresses the establishment of quantitative requirements for all diagnostic elements (that is, testing, technical information, personnel, and training) which constitute the entire diagnostic capability. Thus analysis and tradeoffs can take into account all factors which affect fault detection and isolation capabilities. In some instances, this analysis and tradeoff may be performed under the LSA or maintainability programs. If so, task 201 can be tailored to address only the embedded and external test functions.

50.4 Task 202, inherent testability design and assessment.

Task 202 has two primary thrusts. The first is to get testability into the mainstream of the early design effort. The second is the assessment of testability features incorporated into the design. The approach to accomplishing this assessment is key to the overall testability program. The assessment uses the inherent testability assessment contained in appendix B. The inherent testability assessment provides visibility to testability design issues, identifies the presence or absence of hardware design features which support (or inhibit

testing, and identifies general problem areas. The inherent testability assessment serves as feedback on the testability of the design to the contractor and Government at a point in time when the design can be changed relatively easily.

50.5 Task 203, test design and assessment.

The purpose of task 203 is to incorporate test features into the design that will satisfy testability performance requirements and predict, through analysis, the level of test effectiveness which will be achieved. The key distinction between tasks 202 and 203 is that the result of task 202 is an inherently testable hardware design. The results of task 203 are fault detection and isolation performance levels that achieve the specified requirements. The types of measures applied to the detail design are also different. The prediction of test effectiveness is based on the application of a test sequence to the design (whether BIT or off-equipment test program). The inherent testability assessment is based solely on the design of the system/item, not on the application of test sequences on the design. Inherent testability assessment is oriented more toward testability design practices such as partitioning, controllability, and observability.

Two reference documents provide guidance on performing effort under Task 203. The first is the Joint Service Built-In Test Design Guide, which provides guidance for tramslating BIT design requirements into integral features of equipment design. The second document is the BIT/External Testing Figures of Merit and Demonstration Techniques, which identifies these figures of merit and various analysis and demonstration techniques that apply to each figure of merit.

Vertical test traceability and the design integration of all diagnostic elements is key to ensuring compatibility of testing and diagnostic functions at, and among, all levels of maintenance. Specific guidance on the accomplishment of this compatibility design is contained in Rome Air Development Center's publication "Testability/Diagnostic Design Encyclopedia, Appendix D".

Task 203 is generally applicable only in the full-scale development phase because of the detailed design nature of the task.

50.6 Interfaces with logistic support and engineering disciplines.

By design, MIL-STD-2165 tasks are formulated to interface closely with the LSA process and the other engineering disciplines. It is extremely important that the relationship between other disciplines and testability are clearly understood because inputs and outputs flow back and forth. Breakdowns in this information flow can have serious effects such as diverging requirements and duplication of effort. Therefore, a series of tables and diagrams follows to promote understanding and help in tailoring tasks for inclusion in contractual documents.

Figure 4 shows the interfaces between MIL-STD-2165, task 201, diagnostic concept and testability requirements, and the LSA (MIL-STD-1388-1) process. Inputs to and outputs from task 201 are described in table II.

Figure 5 depicts the information flow between task 201 and the following engineering disciplines.

MIL-STD-785 - Reliability Program for Systems and Equipment Development and Production.
MIL-STD-470 - Maintainability Program for Systems and Equipment.
MIL-H-46855 - Human Engineering Requirements for Military Systems, Equipment and Facilities.
MIL-STD-882 - System Safety Program Requirements.

Tables III and IV describe the inputs to and outputs from tasks 201, 202, and 203 to these engineering disciplines.

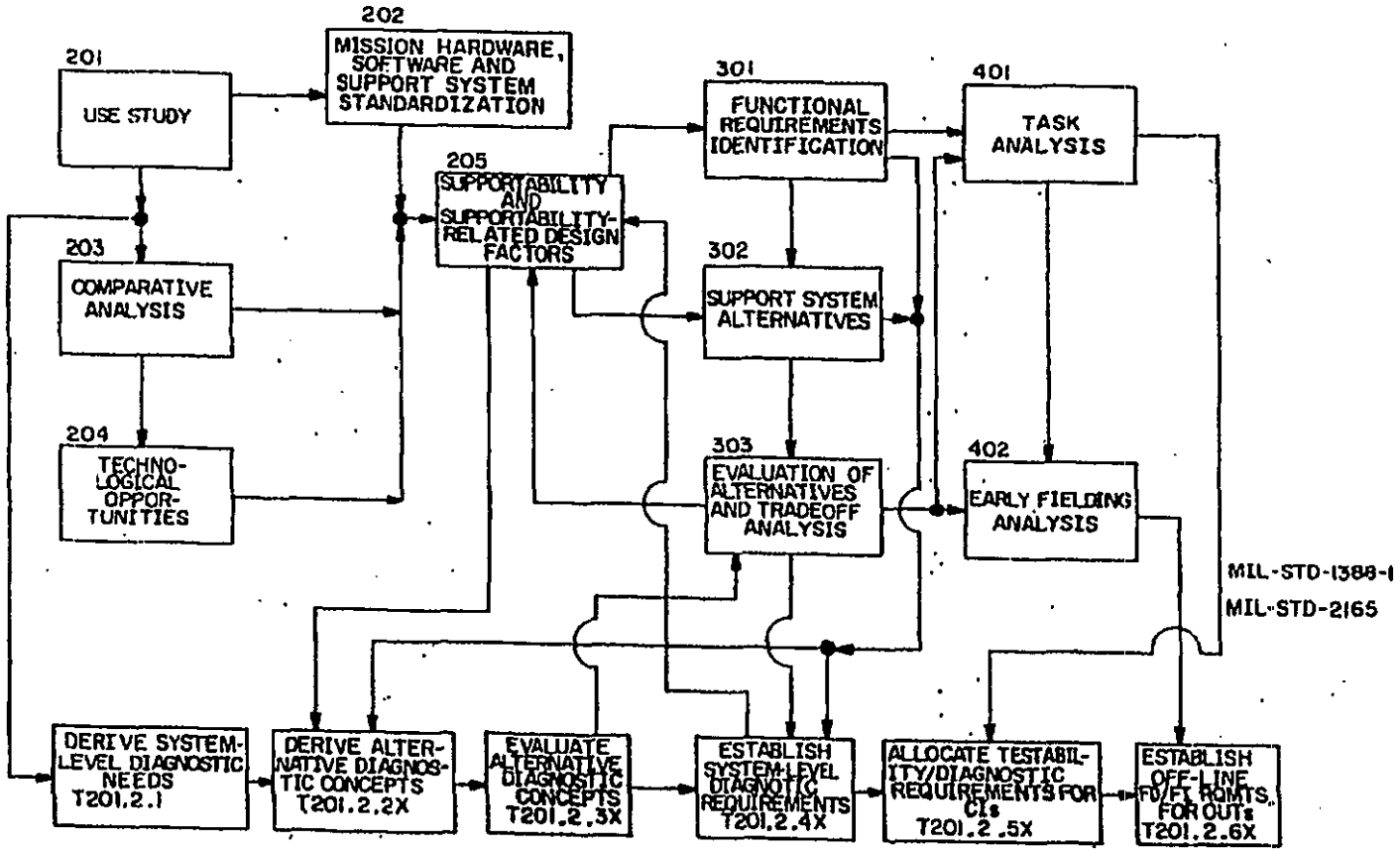

FIGURE 4. LSA/testability information flow.

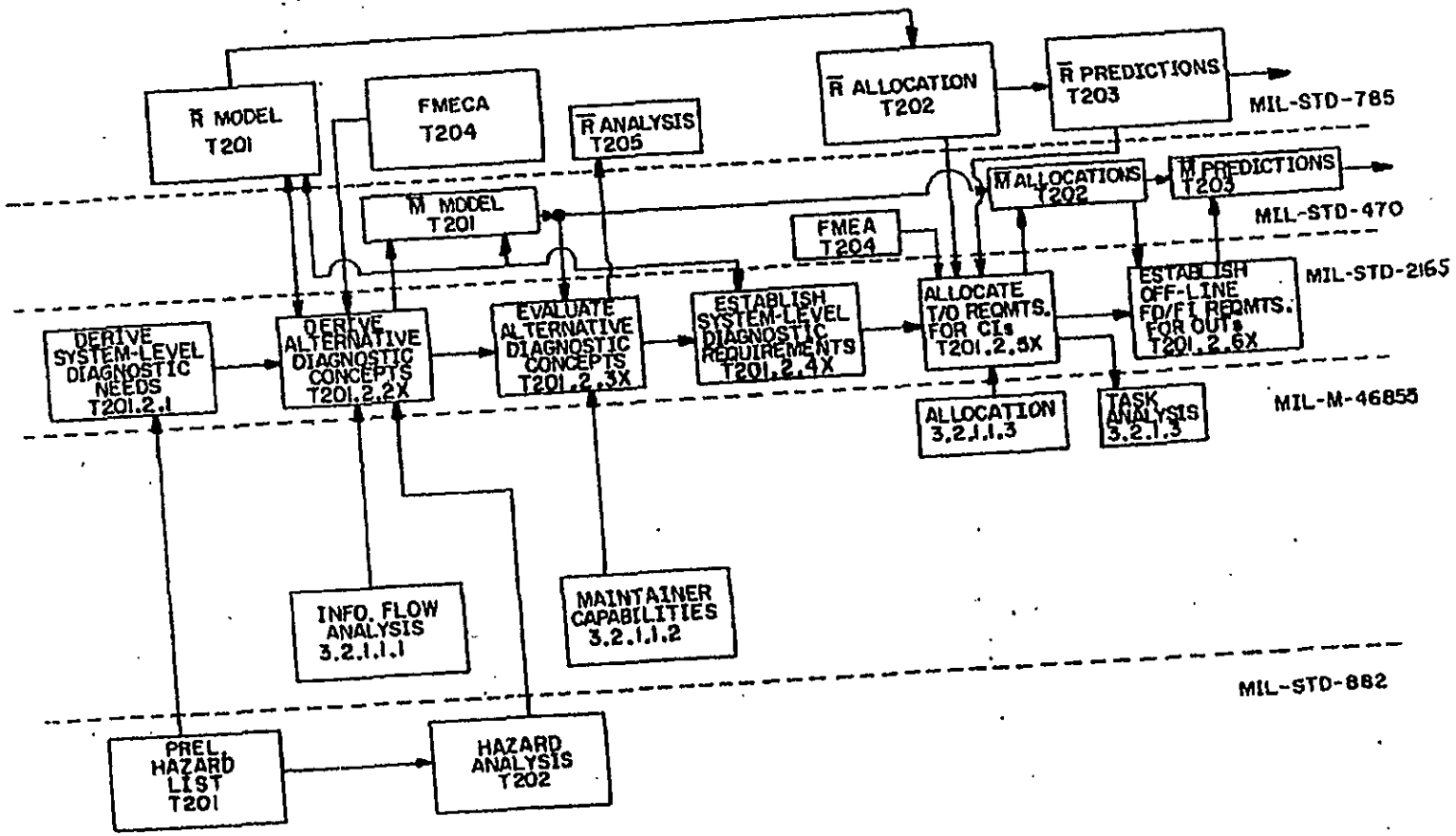

FIGURE 5. Task 201, engineering disciplines/testability information flow.

TABLE II. LSA interface (task 201 diagnostic concept and testability requirements).

	MIL-STD-1388-1 TASK NUMBERS											
	INPUT TO AND OUTPUT FROM TASK 201, MIL-STD-2165											
	201	202	203	204	205		301	302	303		401	402
TASK NUMBERS	INPUT	INPUT	INPUT	INPUT	INPUT	OUTPUT	INPUT	INPUT	INPUT	OUTPUT	INPUT	INPUT
201.2.1 DERIVE SYSTEM-LEVEL DIAGNOSTIC NEEDS	SUPPORTABILITY FACTORS RELATING TO INTENDED USE											
201.2.2 DERIVE ALTERNATIVE DIAGNOSTIC CONCEPTS		CONSTRAINTS BASED ON EXISTING LOGISTIC RESOURCES	BASELINE COMPARISON SYSTEM DATA	PRIME SYSTEM TECHNOLOGY TO BE APPLIED	QUANTITATIVE SUPPORTABILITY VALUES & DESIGN GOALS		OPERATION AND SUPPORT FUNCTIONS	SYSTEM SUPPORT CONCEPT 302.2.1				
201.2.3 EVALUATE ALTERNATIVE DIAGNOSTIC CONCEPTS										EVALUATION OF DIAGNOSTIC CONCEPT ALTERNATIVE 303.2.8		
201.2.4 ESTABLISH SYSTEM-LEVEL FD/FI REQUIREMENTS						SYSTEM-LEVEL DIAGNOSTIC REQUIREMENTS	SUPPORT FUNCTIONS 301.2.4	LOWER LEVEL SUPPORT PLAN 302.2.3	ESTABLISH SUPPORTABILITY REQUIREMENTS			
201.2.5 ALLOCATE TESTABILITY/ DIAGNOSTIC REQUIREMENTS											ANALYSIS OF MAINTENANCE TASKS	
201.2.6 ESTABLISH OFF-LINE FD/FI REQUIREMENTS FOR UUTs												ASSESS. OF POTENTIAL FIELD PROBLEMS

TABLE III. Maintainability and safety interface.

	MIL-STD-470 TASKS								MIL-STD-882 : TASKS	
	INPUTS TO AND OUTPUTS FROM MIL-STD-2165 TASKS 201, 202, 203									
	201		202		203	204		205	201	202
TASK NUMBERS	INPUT	OUTPUT	INPUT	OUTPUT	INPUT	INPUT	OUTPUT	INPUT	INPUT	INPUT
201.2.1 DERIVE SYSTEM-LEVEL DIAGNOSTIC NEEDS									SAFETY MONITORING REQUIREMENTS	
201.2.2 DERIVE ALTERNATIVE DIAGNOSTIC CONCEPTS		INPUTS TO MAINTAINABILITY MODEL FOR ALLOCATION METHOD								HAZARD ANALYSIS
201.2.3 EVALUATE ALTERNATIVE DIAGNOSTIC CONCEPTS	M MODEL STRUCTURE									
201.2.4 ESTABLISH SYSTEM-LEVEL FD/FI REQUIREMENTS		UPDATE M MODE (FEEDBACK)								
201.2.5 ALLOCATE TESTABILITY/ DIAGNOSTIC REQUIREMENTS				ALLOCATED CI TESTABILITY REQUIREMENTS		FMEA DATA				
201.2.6 ESTABLISH OFF-LINE FD/FI REQUIREMENTS FOR UUTs			M ALLOCATION INFORMATION		OFF-LINE FD/FI REQUIREMENTS					
202 INHERENT TESTABILITY ANALYSIS							TESTABILITY DESIGN			
203.2.5 & 203.2.6 EFFECTIVENESS ANALYSIS					EMBEDDED AND EXTERNAL TEST EFFECTIVENESS ANALYSIS	FMEA DATA				
203.2.4 PREDICT BIT FD/FI								BIT FD/FI LEVELS		

TABLE IV. Reliability and human engineering interface.

	MIL-STD-785 - TASK NUMBERS				MIL-H-46855 - PARAGRAPH NUMBERS			
	INPUTS TO AND OUTPUTS FROM MIL-STD-2165, TASK 201							
	201	202	203	204	3.2.1.1.1	3.2.1.1.2	3.2.1.1.3	3.2.1.3
TASK NUMBERS	INPUT	INPUT	INPUT	INPUT	INPUT	INPUT	INPUT	OUTPUT
201.2.1 DERIVE SYSTEM-LEVEL DIAGNOSTIC NEEDS								
201.2.2 DERIVE ALTERNATIVE DIAGNOSTIC CONCEPTS	RELIABILITY MODELING TECHNIQUES			FMEA DATA	INFORMATION FLOW ANALYSIS			
201.2.3 EVALUATE ALTERNATIVE DIAGNOSTIC CONCEPTS						EVALUATION OF HUMAN RESOURCES NEEDS		
201.2.4 ESTABLISH SYSTEM-LEVEL FD/FI REQUIREMENTS								
201.2.5 ALLOCATE TESTABILITY/DIAGNOSTIC REQUIREMENTS		RELIABILITY ALLOCATIONS DRIVE FD/FI ALLOCATIONS	M PREDICTIONS FOR ALLOCATION REVIEW				HUMAN ALLOCATION FOR DIAGNOSTIC FUNCTIONS	TASK ANALYSIS RESULTS
201.2.6 ESTABLISH OFF-LINE FD/FI REQUIREMENTS FOR UUT's								

APPENDIX B

INHERENT TESTABILITY ASSESSMENT

CONTENTS

FIGURES

TABLES

APPENDIX B

INHERENT TESTABILITY ASSESSMENT

10. SCOPE

10.1 Purpose. This appendix provides requirements for the assessment of the inherent testability of a system or equipment design. This appendix is a mandatory part of the standard. The information contained herein is intended for compliance.

10.2 Application. Appendix B shall be considered as forming a part of the standard.

20. APPLICABLE DOCUMENTS

This section is not applicable to this appendix.

30. DEFINITIONS

This section is not applicable to this appendix.

40. GENERAL REQUIREMENTS

40.1 General requirements. Conduct an analysis of the inherent (intrinsic) testability of the design. The analysis identifies the presence or absence of hardware features which support testing and identifies problem areas. The method of this appendix shall be applied to each item identified for inherent testability assessment by the requiring authority. Any testability criteria designated as mandatory by the requiring authority, and therefore not subject to design tradeoffs, shall be assessed separately from this procedure. In addition, if analysis of specific testability areas is desired or required separately, then the use of more than one figure of merit will be necessary.

50. DETAILED REQUIREMENTS

50.1 Overview. Assessment of the inherent testability of a system or equipment design shall be conducted using the inherent testability checklist, table IV, of this document. This assessment shall be conducted as follows:

(a) Delete those testability criteria from table IV which are not applicable to the design.
(b) Add additional testability criteria to table IV which are relevant to the design (or modify table IV criteria).
(c) Assign weighting factors (WT) to each item based on its relative importance in achieving a testable product. ($1 \leq WT \leq 10$)
(d) Develop a scoring system for item ($0 \leq$ score ≤ 100) where 100 represents maximum testability and 0 represents a complete lack of testability.

(e) Obtain concurrence on (a) through (d) above from the requiring authority.
(f) Count the design attributes which are relevant to each testability item (such as, the total number of nodes in a circuit).
(g) Count the design attributes which meet the testability criteria for each item (such as, the number of nodes accessible to the tester).
(h) Apply the scoring system to each item (such as, Score = accessible nodes ÷ total nodes, or Score = 100 if YES and = 0 if NO).
(i) Calculate the weighted score for each item, WT Score = WT x Score.
(j) Calculate the inherent testability of the design, TESTABILITY = Sum (WT Score) ÷ Sum (WI). This assessment should be conducted using the detailed guidance provided in the following paragraphs.

50.2 Detailed guidance.

50.2.1 Checklist sample format. The checklist sample format is shown in figure 6.

Testability design criteria	Weight	Total number of occurrences	Number meeting criteria	Score	Weighted score
Criterion 1					
Criterion 2					
.					
.					
.					
Criterion N					
Total					

FIGURE 6. Checklist sample format.

50.2.2 Criteria determination.

The criteria contained in the inherent testability checklist, table VI provide a starting point for conducting an inherent testability assessment. However, some tailoring will always be required to accommodate the specifics of an individual design and the technology utilized. This tailoring process provides the design activity with a methodology for interacting with the requiring activity in determining what testability criteria are relevant for the system under consideration.

The criteria relate to factors which impact the ability of the circuitry to be tested. For example, one criteria from the partitioning section asks: "Is each function to be tested placed wholly upon one board?" From a testability perspective, this design feature would be desirable because loss or degradation of that function would directly imply which board is bad--fault detection, in this case, equals fault isolation.

General guidance for application of testability criteria is listed in table V.

TABLE V. Application of testability criteria.

System	System	Subassembly	Circuit
Test requirements	A	A	A
Built-in test 1/	A	A	A
Partitioning	A	A	A
Test control	A	A	A
Test access	A	A	A
Test data	M	M	A
Mechanical design	M	A	A
Analog design	N/A	N/A	A
Digital design	N/A	N/A	A
Parts selection	A	A	A

Key: A - Applicable; M - Modified for available detail; N/A - Not applicable.

1/ Many of the checklist items that are included in table V under the heading of Built-in test also apply to mechanical testing. In these instances, the word "BIT" may be replaced by another appropriate word.

50.2.3 Testability design criteria tailoring and weighting rationale.

The intent of the checklist is to provide a starting point to select and tailor testability criteria to make it specific to the system. The criteria presented is very broad and covers the full gamut of testability-related considerations. Many criteria may not be applicable to the specific design. As a first step in the tailoring process, these should be dropped out of the checklist. Many of the items within the checklist are also very generically stated, so that these items can be broadly applicable. The intent of the criteria items shall be evaluated in terms of the specific design, and the item should be tailored to make it apply to the specific characteristics and requirements of the design. Finally, it may be necessary to add new criteria items which are not covered in the checklist (new technology, and so forth). In particular, if automated testability analysis tools are to be used, their measures should be included in the checklist.

Items within the checklist can be weighted, based on relative importance to testability. The perceived value of each of the criteria is established by the weighting factor assigned by the design activity and approved by the requiring authority. The most important factor in this "negotiation" is that the requiring authority must be aware of what criteria are significant to achieving a testable design. Conversely, it is important for the design activity to develop a solid rationale for its recommended weighting factors.

The relative importance of each checklist element is established through the assignment of a weight in the range of 1 to 10. Any design criteria which are critical to meeting testability requirements shall be assigned a weighting factor of 10. A weighting factor of 5 shall be assigned to design criteria which are important, but not absolutely critical, to meeting testability requirements. Any criteria which contribute to good testability design practices, but are not critical to meeting testability requirements, shall be assigned a weighting factor of 1. This keeps the requirement visible but will not significantly affect the final calculated testability figure of merit.

50.2.4 Assessment methodology.

50.2.4.1 Inherent testability threshold.

The assignment of the threshold values to be used for the inherent testability assessment is the responsibility of the requiring authority. Due to the broad range of applications subject to evaluation and the basic judgmental nature of what constitutes an adequate level of testability, there is no single "best" threshold value that can be recommended. Upon completion of tailoring and weighting of the checklist items, a score of 100 represents total incorporation of the agreed-upon testability criteria for that particular design. A commitment to the achievement of a 100 percent compliance with the established testability criteria shall be the goal. This goal shall be modulated by "program realities," in terms of what is achievable within the context of the overall system engineering process and associated design constraints.

Typically, a threshold value of 85 to 95, out of a fully compliant value of 100, is reasonable when undertaking inherent testability assessment in a real world environment. The final threshold value established is typically a result of a negotiation process, which involves cost, schedule, and impact on other disciplines, and is not due to any technological limitations experienced by the designer.

50.2.4.2 Scoring methodology.

There are two major types of scoring that can be used. The first is a single occurrence type, which requires a simple "yes" or "no" answer. An example of the type of criterion that can be answered with a single "yes" or "no" response is: "Does the design contain only synchronous logic?" In this instance, a binary

"yes" or "no" scoring method would be applicable, for example, if the presence of only one asynchronous device negates the entire testability approach being utilized.

The second scoring method is a ratio, whereby percentage of occurrence of the criterion is scored. The same criterion is scored as a ratio (such as, "What percent of the latches are synchronous?"), if the presence, or occurrence, of asynchronous logic represented an isolated testing difficulty and not a total obstacle to implementing a design for testability concept.

50.2.4.3 Checklist scoring.

Checklist scoring is a straightforward process which can take place when sufficient design detail is available to undertake an inherent testability assessment and when determination of the checklist criteria and associated weighting factors have been established. Checklist scoring is a five-step process, as summarized below:

Step 1: Determine and enter into the checklist form the total number of occurrences for each criterion.

This step involves invoking the methodology discussed in 50.2.4.2.

Step 2: Determine the number of occurrences meeting each criterion.

This step requires an assessment of the design detail available to determine which of the total number of occurrences of a specific criterion meet the specific testability attribute being assessed by the criterion. This assessment process for determining compliance, or noncompliance, minimizes the need for judgment on the part of the evaluator to the maximum degree possible.

Step 3: Calculate the score for each criterion.

For example, for a "ratio" scoring method:

$$\text{Score} = \frac{\text{Number meeting criterion}}{\text{Total number of occurrences}} \times 100.$$

Step 4: Calculate the weighted score for each criterion.

Multiply the score computed in step 3 by the weight that was established prior to initiating the inherent testability assessment. The weighted score may be expressed as follows:

Weighted score = Weight X Score

Step 5: Calculate the testability figure of merit (TFOM).

Sum the weight (WT) and weighted score (WT Score) columns and use the following equation:

$$\text{TFOM} = \frac{\text{Sum of criterion weighted scores}}{\text{Sum of criterion weights}}$$

50.3 Criteria. Modify the design until the inherent testability equals or exceeds the threshold value.

TABLE VI. Inherent testability checklist.

	WT	Total number	Number meeting criteria	Score	WT score
Mechanical design (for electronic functions)					
Is a standard grid layout used on boards to facilitate identification of components?					
Is enough spacing provided between components to allow for clips and test probes?					
Are all components oriented in the same direction (pin 1 always in same position)?					
Are standard connector pin positions used for power, ground, clock, test, and other common signals?					
Are the number of input and output(I/O) pins in an edge connector or cable connector compatible with the I/O capabilities of the selected test equipment?					
Are connector pins arranged such that the shorting of physically adjacent pins will cause minimum damage?					
Does the board layout support guided-probe testing techniques?					
Has provision been made to incorporate a test-header connector into the design to enhance ATE testing of surface-mounted devices?					
Is defeatable keying used on each board so as to reduce the number of unique interface adapters required?					
When possible, are power and ground included in the I/O connector or test connector?					
Have test and repair requirements impacted decisions on conformal coating?					

TABLE VI. Inherent testability checklist - Continued.

	WT	Total number	Number meeting criteria	Score	WT score
Is the design free of special set-up requirements (special cooling) which would slow testing?					
Does the item warm up in a reasonable amount of time?					
Is each hardware component clearly labeled?					
Partitioning (for electronic functions)					
Is each function to be tested placed wholly upon one board?					
If more than one function is placed on a board, can each be tested independently?					
Within a function, can complex digital and analog circuitry be tested independently?					
Within a function, is the size of each block of circuitry to be tested small enough for economical fault detection and isolation?					
If required, are pull up resistors located on same board as the driving component?					
Are analog circuits partitioned by frequency to ease tester compatibility?					
Is the number of power supplies required compatible with the test equipment?					
Is the number and type of stimuli required compatible with the test equipment?					
Are elements which are included in an ambiguity group placed in the same package?					

TABLE VI. Inherent testability checklist - Continued.

	WT	Total number	Number meeting criteria	Score	WT score
Test control					
Are connector pins not needed for operation used to provide test stimulus and control from the tester to internal nodes?					
Can circuitry be quickly and easily driven to a known initial state? (master clear; less than N clocks for initialization sequence)?					
Are redundant elements in design capable of being independently tested?					
Is it possible to disable on-board oscillators and drive all logic using a tester clock?					
Can long counter chains be broken into smaller segments in test mode with each segment under tester control?					
Can the tester electrically partition the item into smaller independent, easy-to-test segments? (placing tri-state elements in a high impedance state).					
Is circuitry provided to by-pass any (unavoidable) one-shot circuitry?					
Can feedback loops be broken under control of the tester?					
Have provisions been made to test the system bus as a stand-alone entity?					
In microprocessor-based systems, does the tester have access to the data bus, address bus and important control lines?					

TABLE VI. Inherent testability checklist - Continued.

	WT	Total number	Number meeting criteria	Score	WT score
Are test control points included at those nodes which have high fan-in (test bottlenecks)?					
Are input buffers provided for these control point signals with high drive capability requirements?					
Are active components, such as demultiplexers and shift registers, used to allow the tester to control necessary internal nodes using available input pins?					
Test access					
Are unused connector pins used to provide additional internal node data to the tester?					
Are signal lines and test points designed to drive the capacitive loading represented by the test equipment?					
Are test points provided such that the tester can monitor and synchronize to onboard clock circuits?					
Are test access points placed at those nodes which have high fan-out?					
Are buffers employed when the test point is a latch and susceptible to reflections?					
Are buffers or divider circuits employed to protect those test points which may be damaged by an inadvertent short circuit?					
Are active components, such as multiplexers and shift registers, used to make necessary internal node test data available to the tester over available output pins?					

TABLE VI. Inherent testability checklist - Continued.

	WT	Total number	Number meeting criteria	Score	WT score
Are all high voltages scaled down within the item prior to providing test point access so as to be consistent with tester capabilities?					
Is the measurement accuracy of the test equipment adequate compared to the tolerance requirement of the item being tested?					
Parts selection					
Is the number of different part types the minimum possible?					
Have parts been selected which are well characterized in terms of failure modes?					
Are the parts independent of refresh requirements? If not, are dynamic devices supported by sufficient clocking during testing?					
Is a single logic family being used? If not, is a common signal level used for interconnections?					
Analog design					
Is one test point per discrete active stage brought out to the connector?					
Is each test point adequately buffered or isolated from the main signal path?					
Are multiple, interactive adjustments prohibited for production hems?					
Are circuits functionally complete without bias networks or loads on some other UUT?					
Is a minimum number of multiple phase-related or timing-related stimuli required?					

TABLE VI. Inherent testability checklist - Continued.

	WT	Total number	Number meeting criteria	Score	WT score
Is a minimum number of phase or timing measurements required?					
Is a minimum number of complex modulation or unique timing patterns required?					
Are stimulus frequencies compatible with tester capabilities?					
Are stimulus rise time or pulse width requirements compatible with tester capabilities?					
Do response measurements involve frequencies compatible with tester capabilities?					
Are response rise time or pulse width measurements compatible with tester capabilities?					
Are stimulus amplitude requirements within the capability of the test equipment?					
Are response amplitude measurements within the capability of the test equipment?					
Does the design avoid external feedback loops?					
Does the design avoid or compensate for temperature sensitive components?					
Does the design allow testing without heat sinks?					
Are standard types of connectors used?					

TABLE VI. Inherent testability checklist - Continued.

	WT.	Total number	Number meeting criteria	Score	WT score
RF design					
Do transmitter outputs have directional couplers or similar signal sensing/attenuation techniques employed for BIT or off-line test monitoring purposes, or both?					
If an RF transmitter is to be tested utilizing off-line ATE, has suitable test fixturing (anechoic chamber) been designed to safely test the subject end item over its specified performance range of frequency and power?					
Have suitable termination devices been employed in the off-line ATE or BIT circuitry to accurately emulate the loading requirements for all RF signals to be tested?					
Has provision been made in the off-line ATE to provide switching of all RF stimulus and response signals required to test the subject RF UUT?					
Does the off-line ATE or BIT diagnostic software provide for compensation of UUT output (response) power and adjustment of input (stimulus) power, so that RF switching and cable errors are compensated for in the measurement data?					
Does the RF UUT employ signal frequencies or power levels in excess of the core ATE stimulus/measurement capability? If so, are signal converters employed within the ATE to render the ATE/UUT compatible?					
Are the RF test input/output access ports of the UUT mechanically compatible with the off-line ATE I/O ports?					

TABLE VI. Inherent testability checklist - Continued.

	WT	Total number	Number meeting criteria	Score	WT score
Has the UUT/ATE RF interface been designed so that the system operator can quickly and easily connect and disconnect the UUT without special tooling?					
Has the RF UUT been designed so that repair or replacement of any assembly or subassembly can be accomplished without major disassembly of the unit?					
Have adequate testability (controllability/observability) provisions for calibrating the UUT been provided?					
Have RF compensation procedures and data bases been established to provide calibration of all stimulus signals to be applied and all response signals to be measured by BIT or off-line ATE to the RF UUT interface?					
Have all RF testing parameters and quantitative requirements for these parameters been explicitly stated at the RF UUT interface for each RF stimulus/response signal to be tested?					
EO design					
Have optical splitters/couplers been incorporated to provide signal accessibility without major disassembly?					
Have optical systems been functionally allocated so that they and associated drive electronics can be independently tested?					
Does the test fixturing intended for the off-line test present the required mechanical stability?					

TABLE VI. Inherent testability checklist - Continued.

	WT	Total number	Number meeting criteria	Score	WT score
Has temperature stability been incorporated into fixture/UUT design to assure consistent performance over a normal range of operating environments?					
Are the ATE system, light sources, and monitoring systems of sufficient wavelength to allow operation over a wide range of UUT's?					
Is there sufficient mechanical stability and controllability to obtain accurate optical registration?					
Can requirements for boresighting be automated or eliminated?					
Has adequate filtering been incorporated to provide required light attenuation?					
Do light sources provide enough dynamics over the operating range?					
Do monitors possess sufficient sensitivity to accommodate a wide range of intensities?					
Can all modulation models be simulated, stimulated, and monitored?					
Do test routines and internal memories test pixels for shades of gray?					
Can optical elements be accessed without major disassembly or realignment?					
Can targets be automatically controlled for focus and aperture presentation?					
Are optical collimators adjustable over their entire range of motion via automations?					

TABLE VI. Inherent testability checklist - Continued.

	WT	Total number	Number meeting criteria	Score	WT score
Do they possess sufficient range of motion to meet a variety of test applications?					
Digital design					
Does the design contain only synchronous logic?					
Are all clocks of differing phases and frequencies derived from a single master clock?					
Are all memory elements clocked by a derivative of the master clock? (Avoid elements clocked by data from other elements.)					
Does the design avoid resistance capacitance one-shots and dependence upon logic delays to generate timing pulses?					
Does the design support testing of "bit slices"?					
Does the design include data wraparound circuitry at major interfaces?					
Do all buses have a default value when unselected?					
For multilayer boards, is the layout of each major bus such that current probes or other techniques may be used for fault isolation beyond the node?					
Is a known output defined for every word in a read only memory (ROM)?					
Will the selection of an unused address result in a well defined error state?					

TABLE VI. Inherent testability checklist - Continued.

	WT	Total number	Number meeting criteria	Score	WT score
Is the number of fan-outs for each internal circuit limited to a predetermined value?					
Is the number of fan-outs for each board output limited to a predetermined value? Are latches provided at the inputs to a board in those cases where tester input skew could be a problem?					
Is the design free of WIRED-OR's?					
Does the design include current limiters to prevent domino effect failures?					
If the design incorporates a structured testability design technique (scan path, signature analysis), are all the design rules satisfied?					
Are sockets provided for microprocessors and other complex components?					
Built-in test (BIT)					
Can BIT in each item be exercised under control of the test equipment?					
Is the test program set designed to take advantage of BIT capabilities?					
Are on-board BIT indicators used for important functions? Are BIT indicators designed such that a BIT failure will give a "fail" indication?					
Does the BIT use a building-block approach (all inputs to a function are verified before that function is tested)?					
Does building-block BIT make maximum use of mission circuitry?					

TABLE VI. Inherent testability checklist - Continued.

	WT	Total number	Number meeting criteria	Score	WT score
Is BIT optimally allocated in hardware, software, and firmware?					
Does on-board ROM contain self-test routines?					
Is the self-test circuitry designed to be testable?					
Have means been established to identify whether hardware or software has caused a failure indication?					
Does BIT include a method of saving on-line test data for the analysis of intermittent failures and operational failures which are non-repeatable in the maintenance environment?					
Is the predicted failure rate contribution of the BIT circuitry within stated constraints?					
Is the additional weight attributed to BIT within stated constraints?					
Is the additional volume attributed to BIT within stated constraints?					
Is the additional power consumption attributed to BIT within stated constraints?					
Is the additional part count due to BIT within stated constraints?					
Does the allocation of BIT capability to each item reflect the relative failure rate of the items and the criticality of the items' functions?					

TABLE VI. Inherent testability checklist - Continued.

	WT	Total number	Number meeting criteria	Score	WT score
Are BIT threshold values, which may require changing as a result of operational experience, incorporated in software or easily-modified firmware?					
Is processing or filtering of BIT sensor data performed to minimize BIT false alarms?					
Are the data provided by BIT tailored to the differing needs of the system operator and the system maintainer?					
Is sufficient memory allocated for confidence tests and diagnostic software?					
Does mission software include sufficient hardware error detection capability?					
Is the failure latency associated with a particular implementation of BIT consistent with the criticality of the function being monitored?					
Are BIT threshold limits for each parameter determined as a result of considering each parameter's distribution statistics, the BIT measurement error and the optimum fault delection/false alarm characteristics?					
Performance monitoring					
Have critical functions been identified (by FMECA) which require monitoring for the system operation and users?					
Has the displayed output of the monitoring system received a human engineering analysis to ensure that the user is supplied with the required information in the best usable form?					

TABLE VI. Inherent testability checklist - Continued.

	WT	Total number	Number meeting criteria	Score	WT score
Have interface standards been established that ensure the electronic transmission of data from monitored systems is compatible with centralized monitors?					
Mechanical systems condition monitoring (MSCM)					
Have MSCM and battle damage monitoring functions been integrated with other performance monitoring functions.					
Are preventive maintenance monitoring functions (oil analysis, gear box cracks) in place?					
Have scheduled maintenance procedures been established?					
Sensors					
Are pressure sensors placed very close to pressure sensing points to obtain wideband dynamic data?					
Has the selection of sensors taken into account the environtental conditions under which they will operate?					
Has the thermal lag between the test media and sensing elements been considered?					
Have procedures for calibration of sensing devices been established?					
Diagnostic capability integration					
Have vertical testability concepts been established, employed, and documented?					

TABLE VI. Inherent testability checklist - Continued.

	WT	Total number	Number meeting criteria	Score	WT score
Has a means been established to ensure compatibility of testing resources with other diagnostic resources at each level of maintenance (technical information, personnel, and training)?					
Has the diagnostic strategy (dependency charts, logic diagrams) been documented?					
Test requirements					
Has a "level of repair analysis" been accomplished?					
For each maintenance level, has a decision been made for each item on how built-in test, automatic test equipment, and general purpose electronic test equipment, will support fault detection and isolation?					
Is the planned degree of test automation consistent with the capabilities of the maintenance technician?					
For each item, does the planned degree of testability design support the level of repair, test mix, and degree of automation decisions?					
Test data					
Do state diagrams for sequential circuits identify invalid sequences and indeterminate outputs?					
If a computer-aided design system is used for design, does the CAD data base effectively support the test generation process and test evaluation process?					

TABLE VI. Inherent testability checklist - Continued.

	WT	Total number	Number meeting criteria	Score	WT score
For large scale integrated circuits used in the design, are data available to accurately model the circuits and generate high-confidence tests?					
For computer-assisted test generation, is the available software sufficient in terms of program capacity, fault modeling, component libraries, and post-processing of test response data?					
Are testability features included by the system designer documented in the TRD in terms of purpose and rationale for the benefit of the test designer?					
Are test diagrams included for each major test? Is the diagram limited to a small number of sheets? Are inter-sheet connections clearly marked?					
Is the tolerance band known for each signal on the item?					

APPENDIX C

GLOSSARY

CONTENTS

APPENDIX C

GLOSSARY

10. SCOPE

10.1 Scope. Appendix C shall be considered as forming a part of the basic standard. This appendix is not a mandatory part of the standard. The information contained herein is intended for guidance only.

10.2 Purpose. The purpose of this appendix is to provide definitions of terms used for clarity of understanding and completeness of information. As a general rule, the definitions provided are currently accepted and have been extracted verbatim from other directives (regulations, manuals, military standards, DOD Directives.) A limited number of terms are presented for which definitions were developed from several reference documents.

20. APPLICABLE DOCUMENTS

This section is not applicable to this appendix.

30. DEFINITIONS

Acquisition phases.

(a) Concept exploration phase. The identification and exploration of alternative solutions or solution concepts to satisfy a validated need.
(b) Demonstration and validation phase. The period when selected candidate solutions are refined through extensive study and analyses; hardware development, if appropriate; test; and evaluations.
(c) Engineering development and manufacturing phase. The period when the system and the principal items necessary for its support are designed, fabricated, tested, and evaluated.
(d) Production and deployment phase. The period from production approval until the last system is delivered and accepted.

Built in test (BIT). An integral capability of the mission system or equipment which provides an automated test capability to detect, diagnose, or isolate failures.

Built-in test equipment (BITE). Hardware which is identifiable as performing the built-in test function; a subset of BIT.

Cannot duplicate (CND). A fault indicated by BIT or other monitoring circuitry which cannot be confirmed at the first level of maintenance.

Diagnostics. The hardware, software, or other documented means used to determine that a malfunction has occurred and to isolate the cause of the malfunction. Also refers to "the action of detecting and isolating failures."

Diagnostic capability. The capability of the system to detect and isolate faults utilizing automatic and manual testing, maintenance aids, technical information, and the effects of personnel and training.

Diagnostic concept. An initial or preliminary view of the scope, function, and operation of a system's or equipment's diagnostic capability.

Diagnostic element. One part of the diagnostic capability (ATE).

Diagnostic needs. Factors that can be assembled to form diagnostic requirements, based on weapon system operational needs and constraints or functions which are required to be diagnosed. The time needed to perform these diagnostics is also included.

Embedded diagnostics. Any portion of the weapon system's diagnostic capability which is an integral part of the prime system or support system. "Integral" implies that the embedded portion is physically enclosed in the prime system or permanently attached, or both--physically or electrically.

External diagnostics. Any portion of the weapon system's diagnostic capability which is not embedded.

Failure latency. The elapsed time between fault occurrence and failure indication.

False alarm. A fault indicated by BIT or other monitoring circuitry where no fault exists.

Fault coverage, fault detection. The ratio of failures detected (by a test program or test procedure) to failure population; expressed as a percentage.

Fault isolation time. The elapsed time between the detection and isolation of a fault; a component of repair time.

Fault resolution, fault isolation. The degree to which a test program or procedure can isolate a fault within an item; generally expressed as the percent of the cases for which the isolation procedure results in a given ambiguity group size.

Inherent testability. A testability which is dependent only upon hardware design and is independent of test stimulus and response data.

Interface device (ID). Provide mechanical and electrical connections and any signal conditioning required between the ATE and the UUT; also known as an interface test adapter or interface adapter unit.

Integrated diagnostics. A structured design and management process to achieve the maximum effectiveness of a weapon system's diagnostic capability by considering and integrating all related pertinent diagnostic elements. The process includes interfaces between design, engineering, testability, reliability, maintainability, human engineering, and logistic support analysis. The goal is a cost-effective capability to detect and unambiguously isolate all faults known or expected to occur in weapon systems and equipment in order to satisfy weapon system mission requirements.

Item. A generic term which may represent a system, subsystem, equipment, assembly, or subassembly, depending upon its designation in each task. Items may include configuration items and assemblies designated as UUT's.

Maintenance aid. The maintenance aid, sometimes called a job performance aid, presents information to assist the technician. It is a device, publication, or guide used on the job to facilitate performance of maintenance. It can deliver:

- Historical information on what fault was found when similar symptoms were experienced.
- Troubleshooting logic to assist in finding the fault.
- Procedural information which assists the technician in finding and correcting a failure.

Off-line testing. The testing of an item with the item removed from its normal operational environment.

Performing activity. That activity (Government, contractor, subcontractor, or vendor) which is responsible for performance of testability tasks or subtasks as specified in a contract or other formal document of agreement.

Requiring authority. That activity (Government, contractor, or subcontractor) which levies testability task or subtask performance requirements on another activity (performing activity) through a contract or other document of agreement.

Retest okay. A unit under test that malfunctions in a specific manner during operational testing, but performs that specific function satisfactorily at a higher level maintenance facility.

Testability. A design characteristic which allows the status (operable, inoperable, or degraded) of an item to be determined and the isolation of faults within the item to be performed in a timely manner.

Test effectiveness. Measures which include consideration of hardware design, BIT design, test equipment design, and TPS design. Test effectiveness measures include, but are not limited to, fault coverage, fault resolution, fault detection time, fault isolation time, and false alarm rate

Test program set (TPS). The combination of test program, interface device, test program instruction, and supplementary data required to initiate and execute a given test of a unit under test (UUT).

Test requirements document. An item specification that contains the required performance characteristics of a UUT and specifies the test conditions, values (and allowable tolerances) of the stimuli, and associated responses needed to indicate a properly operating UUT.

APPENDIX D

UNIT UNDER TEST COMPATIBILITY WITH AUTOMATIC TEST EQUIPMENT; GENERAL REQUIREMENTS FOR

CONTENTS

APPENDIX D

10. SCOPE

10.1 Purpose. This Appendix is a mandatory part of MIL-STD-2165A for U.S. Navy procurement. The information contained herein is intended for compliance. This Appendix contains requirements for equipment which is to be supported with Automatic Test Equipment (ATE). It includes requirements to consider the capability of the off-line ATE system during the design phase of the equipment and during maintainability and testability analyses. This Appendix supplements MIL-STD-2165A and establishes requirements for electronic system's compatibility with Automatic Test Equipment (ATE) and establishes the Consolidated Automated Support System (CASS) as the off-line ATE to be used when ATE is determined to be required to support the weapon system. It is applicable to Naval Air System Command acquisitions.

Coupling equipment testability, maintainability and ATE compatibility during initial avionic system design, assists in assuring that full and effective use of the ATE can be made when the equipment is tested.

This Appendix together with the other DOD and Military documents referenced in Section 20, provides the means for establishing ATE compatibility early in a system's life cycle. Data Item Descriptions applicable to this Appendix are listed in Section 60.

20. APPLICABLE DOCUMENTS

20.1 Government Documents.

20.1.1 Standards and handbooks. The following standards and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DODISS) and supplement thereto, cited in the solicitation.

STANDARDS

MILITARY

MIL-STD-1309	- Definition of Terms for Test Measurement and Diagnostic Equipment
MIL-STD-1388-1	- Logistic Support Analysis
MIL-STD-1521	- Technical Reviews and Audits for System, Equipment and Computer Software
MIL-STD-2084	- Maintainability of Avionic and Electronic Systems and Equipment, General Requirements for
MIL-STD-2077	- Test Program Sets, General Requirements for

(Copies of specifications, standards and publications required by contractors in connection with specific procurement functions should be obtained from th Standardization Documents Order Desk).

OTHER

NAEC-MISC-52-1075 Naval Air Engineering Center Report, Unit Under Test (UUT) Input/Output Requirements for the Consolidated Automated Support System.

(NAEC Reports are available from Commanding Officer, Naval Air Engineering Center, ATTN: 34A, Lakehurst, NJ 08733.)

INFORMATION

SECNAVINST 3960.6 Department of the Navy Policy and Responsibility for Test, Measurement, Monitoring, Diagnostic Equipment and Systems, and Metrology and Calibration (METCAL).

30. DEFINITIONS

30.1 Source of Terms. The definition of terms used in this notice may be found in MIL-STD-1309 and are consistent with MIL-STD-2084 and MIL-STD-2077.

30.2 Weapon Replaceable Assembly (WRA). A generic term which includes all replaceable packages of a system installed in that system with the exception of cables, mounting provisions and fuse boxes or circuit breakers.

30.3 Shop Replaceable Assembly (SRA). A generic term which includes all packages within a WRA including the chassis and wiring as a unit.

30.4 Sub-Shop Replaceable Assembly (Sub-SRA). A modular form item packaged on an SRA.

30.5 Interface Device (ID). The ID is any device which provides mechanical and electrical connection and signal conditioning between the ATE and the UUT.

30.5.1 Simple Interface Device. The ID is a connecting device only. It may contain passive circuit elements and simple active circuits.

30.6 Unit Under Test (UUT). A general term used to signify any unit to be tested on ATE. It includes WRA, SRA and Sub-SRA.

30.7 UUT Test Program Sets (TPS). A TPS consists of those items necessary to test a WRA, SRA or Sub-SRA on ATE. This includes electrical, mechanical and test program elements. The individual elements are the test program, the interface device and the test program set documents.

40. GENERAL REQUIREMENTS

40.1 ATE Compatibility. Electronic systems, subsystems or components for which test on ATE is a requirement at Intermediate or Depot maintenance levels, shall be designed to incorporate features which facilitate rapid automatic fault detection and fault isolation to the levels specified in the contract of each WRA,

SRA, and Sub-SRA of the system, subsystem or equipment using the test resources available in the off-line ATE and without stimulation by another WRA, SRA or Sub-SRA and without manual intervention on the part of the ATE operator. The system shall incorporate features to allow fault detection and isolation, by a test program executed on the ATE, to the levels specified in the contract when the unit is connected to the ATE through a simple interface device.

40.2 Off-line ATE: For electronic systems the off-line ATE is the Consolidated Automatic Support System (CASS), as required by SECNAVINST 3960.6 unless otherwise directed by the contract.

50. DETAILED REQUIREMENTS

50.1 Features. Among the features required of UUTs within the scope of this standard are the following:

50.1.1 Compatibility With Automatic Test Equipment (ATE). Design for ATE shall be for complete compatibility of the UUT with the capability of the off-line ATE. When an incompatibility exists between the test requirements of the UUT and the capability of the off-line ATE, the contractor shall submit a Compatibility Problem Report as described in paragraph 50.2.1. For testing on ATE, compatibility requirements include:

a. When CASS is the off-line ATE, UUTs (WRA, SRA, Sub-SRA) be tested by utilization of the CASS stimulus and measurement capability directly without the use of active circuit elements in the interface devices. All circuitry required to accommodate CASS capability shall be contained within the UUT. A description of CASS stimulus and measurement capability is available in NAEC-MISC-52-1075.

b. Stimulus and measurement signals required by the UUT in programmable increments and have accuracy and tolerance requirements available within off-line ATE capabilities.

c. Particular emphasis shall be placed on the UUT to insure that the interface between the UUT and off-line ATE will be simple, through maximum utilization of CASS System capabilities.

50.2 UUT/ATE Incompatibility. Any UUT parameters or characteristics which represent test and or compatibility problems with the off-line ATE shall be presented as a potential problem to the procuring agency and the government cognizant activity when the problem becomes known.

50.2.1 Compatibility Problem Report. When it is not technically feasible to comply with specific requirements of Section 40 and 50 of this notice, a Compatibility Problem Report will be forwarded to the procuring activity. In order for the procuring activity to evaluate the effects of any incompatibility, all compatibility problem reports shall contain the following information.

a. System Name/Nomenclature
WRA Name/Nomenclature
SRA Reference Designator
Sub-SRA Reference Designator

b. Reference to the applicable section of NAEC-MISC-52-1075 and technical description of the problem.

c. Proposed alternative concepts or proposed solutions. A detailed justification, including cost benefit analyses, for any proposed solutions and/or the alternative concepts provided shall be fully described. Alternatives for consideration by the procuring activity include:

(1) Manual intervention by the ATE operator during the execution of a test program beyond the entry of the results of visual observations or manipulation of switches.

(2) Stimulus or measurement through the use of an indirect, alternate capability of the off-line ATE.

(3) Providing the required capability in the off-line ATE,

(4) Providing the required capability in an interface device, and

(5) Use of external stimulus or measurement equipment.

50.3 UUT Input/Output Description. The Contractor shall provide a description of the UUTs Input/Output (I/O) parameters for use by the government in evaluating WRA, SRA and Sub-SRA compatibility with the off-line ATE. The format for submitting the UUT I/O description is contained in Data Item Description (TBD).

60. QUALITY ASSURANCE

60.1 ATE Compatibility Verification. The Contractor's compliance with the requirements of this notice will be subject to procuring activity verification, inspection, demonstration and approval in accordance with the following paragraphs.

60.1.1 ATE Compatibility Verification Process. Off-line ATE/UUT System compatibility will be determined by consideration of the following areas:

a. Physical interface between the UUT and the off-line ATE.

b. Electronic and power interface between the UUT and the off-line ATE.

60.1.1.1 Specific Characteristics. The following specific characteristics and features will be analyzed:

a. Maintainability and testability data required by MIL-STD-1388-1, MIL-STD-2084, and this standard.

b. UUT stimulus, measurement and accuracy requirements to insure that they are within the capability of the off-line ATE.

c. Equipment external to the off-line ATE required to generate signals or monitor responses.

60.1.2 UUT Documentation Analysis and Hardware Inspection. The capability reflected in Paragraph 60.1.1.1 will be determined by analysis of UUT documentation supplemented by actual hardware inspection. Reviews shall be performed as an adjunct to the normal hardware design reviews and acceptance tests. The effort will be performed at the contractor's or subcontractor's plant where adequate work facilities and contractor personnel/technical assistance can be provided.

60.1.2.1 Review Phases and Requirements. Formal review and assessment of compatibility related contract requirements shall be an integral part of each WRA, SRA, and Sub-SRA design review (e.g. system design review (SDR), preliminary design review (PDR), critical design review (CDR), etc.) specified by the contract. The contractor shall schedule reviews with subcontractors, as appropriate, and inform the requiring authority in advance of each review. Results of each design review shall be documented. Design reviews shall identify and discuss all pertinent aspects of UUT and ATE compatibility.

a. Demonstration and Validation Phase. It shall be the responsibility of the contractor to implement review of compatibility with the off-line ATE in conjunction with MIL-STD-1388-1, MIL-STD-2084 and this standard's maintainability and testability reviews. Design Review Agendas (DI-A-7088) shall be developed in accordance with MIL-STD-1521, coordinated to address at least the following topics as they apply to the program phase activity and the review being conducted.

(1) Compatibility between the UUT and the off-line ATE.

(2) Compatibility design requirements.

(3) Progress toward establishing or achieving ATE compatibility.

(4) Comparative analysis with existing WRAs, SRAs, and Sub-SRAs

(5) Design and redesign actions proposed or taken to ensure UUT compatibility.

(6) Cost Estimates that reflect the impact of design and redesign actions proposed or taken to ensure UUT compatibility.

b. Engineering Manufacturing Development Phase (EMD). During Full Scale Development, the contractor shall implement detailed reviews of compatibility with the off-line ATE in conjunction with MIL-STD-1388-1, MIL-STD-2084 and this

standard's maintainability and testability reviews. Design Review Agendas (DI-A-7088) shall be developed to address the following topics as they apply to the development phase and review being conducted (Preliminary Design, Critical Design Reviews).

(1) Compatibility between the UUT and off-line ATE.

(2) Progress toward establishing or achieving UUT compatibility with the off-line ATE.

(3) UUT/ATE incompatibilities and proposed corrective actions.

(4) Design and redesign action or proposed action to achieve ATE compatibility.

(5) Compatibility Problem Reports in process or contemplated.

(6) Requirements for incorporation of a specific capability within the off-line ATE.

(7) Cost Estimates.

60.1.3 Data Requirements. The following data is required to be submitted in accordance with the contract DD Form 1423.

a. DI-A-7088 Conference Agenda

b. Contractor Format Compatibility Problem Report

c. Per NAEC Report MISC-52-1075 UUT Input/Output Description

d. Applicable sections of Appendix E, MIL-STD-2165A.

70. PREPARATION FOR DELIVERY

70.1 Packaging and Packing. Reports or data required by this standard shall be packed and packaged for delivery in accordance with the contractor's best commercial practice.

70.2 Marking for Shipments. All shipments of reports shall be marked as stated in the contract or as otherwise instructed by the procuring agency.

APPENDIX E

SYSTEM SYNTHESIS MODEL INPUT DATA SHEETS

CONTENTS

APPENDIX E

SYSTEM SYNTHESIS MODEL INPUT DATA SHEETS

CONTENTS (Con't)

SYSTEM SYNTHESIS MODEL INPUT DATA SHEETS

10. SCOPE

10.1 Purpose. This Appendix is a mandatory part of MIL-STD-2165A for U.S. Navy procurement. The information contained herein is intended for compliance. This appendix defines the System Synthesis Model (SSM) input data sheets to facilitate the collection of Unit Under Test (UUT) and workload data as they relate to the Consolidated Automated Support System (CASS). This appendix also, in part, establishes the mapping model's performance and design limitations.

This appendix together with the other DoD and Military documents referenced in Section 20, provides the means for establishing UUT/CASS compatibility early in a system's life cycle. Data Item Descriptions applicable to this Appendix are listed in Section 40.

20. APPLICABLE DOCUMENTS

20.1 Government Documents.

20.1.1 Standards. The following standards form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DODISS) and supplement thereto cited in the solicitation.

STANDARDS

MILITARY

MIL-STD-1309	- Definition of Terms for Test Measurement and Diagnostic Equipment
MIL-STD-1388-1	- Logistic Support Analysis
MIL-STD-1521	- Technical Reviews and Audits for System, Equipment and Computer Software
MIL-STD-2084	- Maintainability of Avionic and Electronic Systems and Equipment, General Requirements for.

(Unless otherwise indicated, copies of federal and military specifications, standards, and handbooks are available from the Standardization Documents Order Desk, Bldg. 4D, 700 Robbins Avenue, Philadelphia, PA 19111-5094.)

20.1.2 Other government documents and publications. The following other government documents and publications form a part of this document to the extent specified herein. Unless otherwise specified, the issues are those specified in the solicitation.

NAEC-MISC-52-1075	Naval Air Engineering Center report, CASS Interface Description.

(NAEC Reports are available from Commanding Officer, Naval Air Warfare Center, ATTN: 34A, Lakehurst, NJ 08733)

Instruction

SECNAVINST 3960.6 Department of the Navy Policy and Responsibility for Test, Measurement, Monitoring, Diagnostic Equipment and Systems, and Metrology and Calibration (METCAL).

30. DEFINITIONS

30.1 Source of Terms. The definition of terms used in this notice may be found in MIL-STD-1309 and are consistent with MIL-STD-2084 and MIL-STD-2077.

30.2 Weapon Replaceable Assembly (WRA). A generic term which includes all replaceable packages of a system installed in that system with the exception of cables, mounting provisions and fuse boxes or circuit breakers.

30.3 Shop Replaceable Assembly (SRA). A generic term which includes all packages within a WRA including the chassis and wiring as a unit.

30.4 Sub-Shop Replaceable Assembly (Sub-SRA). A modular form item packaged on an SRA.

30.5 Interface Device (ID). The ID is any device which provides mechanical and electrical connection and signal conditioning between the ATE and the UUT.

30.5.1 Simple Interface Device. The ID is a connecting device only. It may contain passive circuit elements and simple active circuits.

30.6 Unit Under Test (UUT). A general term used to signify a unit to be tested on ATE. It includes WRA, SRA and Sub-SRA.

30.7 UUT Test Program Sets (TPS). A TPS consists of those items necessary to test a WRA, SRA or Sub-SRA on ATE. This includes electrical, mechanical and test program elements. The individual elements are the test program, the interface device and the test program set documents.

40. GENERAL DESCRIPTION

40.1 Types of data sheets. This appendix refers to FIVE types of forms, used by the SSM. Forms 1, 2 and 3 are used to identify UUT workload requirements, Form 4 identifies UUT parametric test requirements, and the fifth form (not numbered) identifies the source of the information being provided. The forms are as follows:

Form Number	Paragraph	Title
No Number Assigned	3.1	Source Data Summary Form
1	3.2	Weapon System Data Form
2	3.3	Weapon Replaceable Assembly (WRA) Data Form
3	3.5	Site Data Form
4	3.7	UUT Test Requirements Data Form

50. FORMS AND INSTRUCTIONS

50.1 Source Data Summary Form instructions

50.1.1 General Instructions. One Source Data Summary Form should be filled out for each data collection package completed. This form is divided into two parts. The first part (top) identifies the office and individual responsible for the data. The second part (bottom) provides information on the type and amount of information provided. This information is required for proper data tracking and validation.

50.1.2 Detailed Instructions

Office Code: Identification code of the office entering the data. Example: NAWCADLKE-PD25. This code should be included on each data form submitted.

Name: Last and first name of the individual responsible for the data included in the package.

Address: Location of the individual responsible for the data. Example: Naval Air Warfare Center.

City: City of the individual responsible for the data. Example: Lakehurst.

State: Two-character abbreviation of the state of the individual responsible for the data. Example: NJ

Zip Code: Five-or nine-digit code assigned to the postal location. Example: 08733.

Phone: Commercial area code and phone number of the individual responsible for the data.
Example: (908) 323-0000

Date: Date of data package completion.
Example: 880222 for February 22, 1988.

Number of data forms being submitted with this package:

Example: one system contains 10 WRAs (4 of the WRAs have 10 shop replaceable assemblies (SRAs) and 6 of the WRAs have 5 SRAs). The system is deployed on two platform types at three sites. The data forms required will be:

1 Weapon System Data Form

10 WRA Data Forms

3 Site Data Forms

80 UUT Test Requirement Data Forms (10 WRAs and 70 SRAs)

SOURCE DATA SUMMARY FORM

OFFICE CODE _____

NAME _____

ADDRESS _____

CITY _____ STATE _____ ZIP CODE _____

PHONE _____ DATE (YYMMDD _____

NUMBER OF DATA FORMS BEING SUBMITTED WITH THIS PACKAGE

QTY	FORM	CONTENTS
_____	1	WEAPON SYSTEM DATA FORM
_____	2	WRA DATA FORM
_____	3	SITE DATA FORM
_____	4	UUT TEST REQUIREMENTS DATA FORM*

*Note: To determine UUT compatibility with CASS, only data Form 4 needs to be completed.

50.2 Weapon System Data Form instructions.

50.2.1 General Instructions. One Weapon System Data Form should be filled out for each system. The weapon system data form is divided into four parts. The first (top) identifies the source of the data and its level of validity. The second (middle) is for data specific to the weapon system description. The third (bottom left) provides the system quantity per platform. The fourth (bottom right) provides information on each WRA assigned to the system.

50.2.2 Detailed Instructions.

System AN Nomenclature:	Official Item designation Example: AN/ASW32
Noun Nomenclature:	Common item name. Example: Automatic Flight Control Set
Work Unit Code:	Official code assigned to the weapon system Example: 5771000
Platform:	Type/model/series of aircraft, ship that the weapon system in on Example: F-14A
System Quantity/Platform:	Number of this system assigned to each platform identified
WRA AN Nomenclature:	Official designation of the item Example: CP1029/ASW32 (optional)
WRA Manufacturer's Part Number:	Manufacturer's part number Example: A51A9002-101
WRA Quantity/System:	Number of identified WRAs assigned to this system
WRA MTBUMA (Hours):	Mean time between unscheduled maintenance actions in hours includes MTBF + A799s Example: 245.5

WEAPON SYSTEM DATA FORM 1

SYSTEM AN NOMENCLATURE _____
(Maximum 24 characters)

NOUN NOMENCLATURE
(Maximum 36 characters) _____

WORK UNIT CODE _____
(Maximum 8 characters)

PLATFORM	SYSTEM QUANTITY/ PLATFORM	WRA AN NOMENCLATURE (OPTIONAL)	WRA MFG PART NUMBER	WRA QUANTITY /SYSTEM	WRA MTBUMA HRS

50.3 WRA Data Form instructions

50.3.1 General Instructions. One WRA data form should be filled out for each WRA. The WRA data form is divided into three parts. The first (top) identifies the source of the data and the level of its validity. The second (middle) is for data specific to the WRA description. The third (bottom) provides information on each SRA within the WRA.

50.3.2 Detailed Instructions

WRA AN Nomenclature:	Official item designation. Example: CP1029/ASW32
WRA Noun Nomenclature:	Common item name. Example: Aircraft Roll Computer
Manufacturer's Part Number:	Manufacturer's part numbers. Example: A51A9002-101
FSCM:	Federal supply code for manufacturers. Example: 26512
SM&R Code:	Source, maintenance, and recoverability code. Example: PAOGD
WUC:	Official code assigned to the UUT Example: 5771100
SRA AN Nomenclature:	Official item designation. Example: CP1029/ASW32
SRA Noun Nomenclature:	Common item name. Example: Aircraft Roll Computer
SRA Manufacturer's Part No.	Manufacturer's part number. Example: A51A9002-101
SRA FSCM:	Federal supply code for manufacturers. Example: 26512
SRA WUC:	Official code assigned to the UUT. Example: 5771100
SRA EMT (Hours):	Elapsed on-station maintenance time.
SRA SM&R Code:	Source, maintenance, and recoverability code. Example: PAOGD

SRA Quantity/WRA:	Number of identified SRAs assigned to this WRA
SRA MTBUMA:	Mean time between unscheduled maintenance actions in hours includes MTBF + A799s. Example: 4080.8

WRA DATA FORM 2

WRA AN NOMENCLATURE _____
(Maximum 24 characters)

WRA AN NOMENCLATURE _____
(Maximum 36 characters)

WRA PART NUMBER _____
(Maximum 24 characters)

FSCM _____ SM&R CODE _____

WUC _____

SRA AN NOMENCLATURE	SRA NOUN NOMENCLATURE	SRA MFG PART NUM.	SRA FSCM	SRA WUC	SRA EMT IN HRS	SRA SM&R CODE	SRA QTY PER WRA	SRA MTBUMA (HRS)

50.4 Non applicable to the SSM

50.5 Site Data Form instructions.

50.5.1 General Instructions. One site data form should be filled out for each site at which a system is deployed. The site data form is divided into three parts. The first identifies the source of the data and its level of validity. The second describes the system and site where it is located. The third provides the operational hours and quantity/platform for each platform the system is on.

50.5.2 Detailed Instructions

Description:	Official system designation Example: AN/ASW32
Platform:	Type/model/series of aircraft, ship Example: F-14A
Peace Time Operational Hours:	Nominal number of hours the platform operates per month at that site during peach time. Example: 30.0
Combat Time Operational Hours:	Nominal number of hours the platform operates per month at that site during combat. Example: 45.0
Platform Quantity at Site:	Number of platforms with the identified system at site. Example: 12

NOTE: THIS SHEET MUST BE LABELED CLASSIFIED WHEN CLASSIFIED DATA IS ENTERED.

SITE DATA FORM 3

DESCRIPTION

PLATFORM	PEACETIME OPERATIONAL HOURS/MONTH	COMBAT OPERATIONAL HOURS/MONTH	PLATFORM QUANTITY AT SITE

NOTE: THIS SHEET MUST BE LABELED CLASSIFIED WHEN CLASSIFIED DATA IS ENTERED.

50.6 Not applicable to the SSM.

50.7 UUT Test Requirements Data Form instructions.

50.7.1 General Instructions. When completing the Test Requirements Data Forms, high and low values should be entered only when a range is specified; Example: 0.0 to 10.0V, 1.0 to 3.0A, or 10.0E3 to 100.0E3 Hz. These entries should not account for accuracies and tolerances. When only one value is given, enter the nominal value in both high field and low field, then enter the tolerance in the appropriate tolerance or accuracy fields. Take careful note of the units in the tolerance and accuracy fields; some require a percentage and others require specific units.

The two power requirement categories (AC and DC power supplies) are reserved for UUT power supplies. Test stimuli are to be entered in the waveform generation category.

Only one value is permitted in each field. Therefore, an entry of +1/-3 is not permitted in a tolerance field, not is 1.0 to 3.0A valid in a current field. Symbols such as +/-, "G.T.", and "L.T." are not permitted.

To avoid the confusion that results when Greek-letter prefixes are used, only generalized units are required. Therefore, it is requested that all fields be entered using exponentials. Example: 10 mV should be entered as 10.0E-3, .1E-1 or .010

Note that a decimal is required in the mantissa of the E format. Some fields have no units but require alphanumeric codes that categorize the signal. Codes are listed in 50.7.2.2. Every effort must be made to properly enter these fields.

50.7.1.1 UUT identification. The following UUT identification information is required for each UUT for which test requirements are being provided.

Office Code:	Identification code of the office entering the data. Example: NAWC-PD25
Data Level:	Enter one digit: 1, 2, 3, or 4 1:estimated figures/values 2:contractor proposed or approved figures/values 3:contract figures/values 4:actual or documented figures/values
Data Source:	Document type and number. Example: TRD-Y228A789

Expiration Date:	The last date that the data included in this package is considered valid in its data level.
Commodity:	For NAVAIR use only.
Program Element:	For NAVAIR use only
UUT Class:	Enter the appropriate character code: W: WRA S: SRA, or C: CASS SRA
Part Number:	Manufacturer part number
National Stock No:	National stock number
Noun Nomenclature:	Common item name
AN Nomenclature:	Official designation of the item
Work Unit Code:	Official code assigned to the UUT
EMT:	Elapsed on-station maintenance time. For fielded UUTs, this is total maintenance time; for CASS testables, this is estimated station run-time.
TEC:	Type equipment code

50.7.1.2 Special Instructions. One set of UUT test requirement data forms should be filled out for each UUT. When filling out the forms, carefully follow these instructions and use your best engineering judgment. UUT stimulus and measurement requirements should be entered under the appropriate test category given in table 1, paragraph 50.7.2.1. The information for a signal should only be entered on one sheet. Additional instructions are included at the bottom of each data entry sheet. If any field is not applicable, leave it blank. If any sheet is not applicable, leave it out.

The EO test categories are unique in that they work as a group. Test category 22 (FLIR), 23 (LASER DESIGNATOR), 24 (LASER RANGE), and 25 (TV SYSTEMS) are to be filled out for the individual EO function. In some cases the EO function is a standalone and in some cases the user will have a UUT which is a combination of two or more of the available categories. In any event, test category 26 should be filled out indicating the components of the EO function the aperture, and maximum boresight (if necessary). It is not important to maintain the same record number across the categories as each requirement is filled in. As an example, there is a UUT with a FLIR requirement. Test category 22 and test category 26 must both be filled in to complete the test requirement. For test category 26 only the FLIR column for the component would be filled in, as well as

the aperture, and boresight. As another example, test category 23 (LASER DESIGNATORS) does not have a requirement for boresight and in test category 26, the boresight field should be left blank.

50.7.1.3 Critical parameters. Critical parameters are those parameters in a given test category that must be present for translation to be valid by the SSM. On the input sheets, critical parameters are highlighted by shading.

50.7.2 Detailed Instructions.

Measurement/Stimulus - Measurement requirements are those signals output by the UUT that must be measured by test station instrumentation. Stimulus requirements are signals that must be provided by the tester to the UUT.

Tolerance/Accuracy - Tolerance fields are usually required for stimulus and power requirements and accuracies for measurement requirements. In either case, the term refers to the UUT signal requirement, not to the test station performance characteristics.

Number of Test Pins/Channels - Both terms are used interchangeably and refer to the number of signals simultaneously required to complete a test.

50.7.2.1 Test categories.

Test Category	Category Description
01	DC Power Supply Requirements
02	AC Power Supply Requirements
03	DC Measurement Requirements - DC Voltage Measurement
04	DC Measurement Requirements - DC Current Measurement
05	DC Measurement Requirements - Resistance Measurement
06	Analog Stimulus Requirements - Pulse Generation Excluding Complex RF Pulse Formats
07	Analog Stimulus Requirements - Waveform Generation
08	Analog Measurement Requirements - AC Voltage Measurement
09	Analog Measurement Requirements - Frequency Measurement Excluding Complex Waveforms
10	Analog Measurement Requirements - Time Interval Measurement

11	Analog Measurement Requirements - Complex Waveform Measurement Excluding RF Signals
12	Analog Measurement Requirements - Pulse Measurement
13	Digital Test Requirements - Stimulus/Measurement
14	Resistive Load Requirements
15	Synchro/Resolver Stimulus Requirements
16	Synchro/Resolver Measurement Requirements
17	Interface Bus Requirements
18	RF Stimulus Requirements
19	RF Measurement Requirements
20	Pneumatic Requirements
21	INS Requirements
22	Electro-Optic Requirements - FLIR
23	Electro-Optic Requirements - Laser Designators
24	Electro-Optic Requirements - Laser Range finders
25	Electro-Optic Requirements - TV Systems
26	Electro-Optic Requirements - Multispectral Systems
27	Electro-Optic Requirements - Displays

50.7.2.2 Codes

50.7.2.2.1 Waveform Generation, Complex Waveforms Measurement(Test Categories 7 and 11).

WAVEFORM TYPE	CODE
DC	DC
Sinusoidal	SIN
Square Wave	SQW
Triangle Wave	TRI
Ramp/Sweep	RMP
Pulse	IPU
Logic Data	LD
Arbitrary	ARB
AC	AC

MODULATION TYPE	CODE
NO MODULATION	NOMOD
AMPLITUDE	AMPLM
FREQUENCY	FREQM

50.7.2.2.2 AC Voltage Measurement Requirements (Test Category 8).

Voltage Type	Code
Peak-Peak	P-P
True RMS	RMS

50.7.2.2.3 Complex Waveform Measurement (Test Category 11).

Signal Type	Code
Single Shot	TRANS
Repetitive	REPET

50.7.2.2.4 Digital Stimulus and Measurement Requirements (Test Category 13).

Logic Type	Code
Diode-Coupled Logic	DCL
Transistor-Transistor Logic	TTL
Diode-Transistor Logic	DTL
Resister-Transistor Logic	RTL
Hybrid-Transistor Logic	HTL
Emitter-Coupled Logic	ECL
Metal-Oxide Semiconductor	MOS
Complementary-Symmetry MOS	CMS
Discrete	DIS

Pin Type	Code
Stimulus	S
Measurement	M
Bidirectional	B

50.7.2.2.5 Interface Bus Requirements (Test Category 17).

Bus Type	Code	Bus Type	Code
MIL-STD-1533A/B	1553	ARINC 42	429
IEEE-488	488	McAIR A3818	3818
Ethernet	802.3	High-Speed Data Bus	HSDB
MIL-STD-1397	1397	Fiber-Optic Data Bus	FODB
RS232, 19.2K Baud	232	Manchester (RS-485)	MANC
MIL-STD-1773	1773	Harpoon/SLAM (RS-485)	HARP
EIA-RS-422, up to 38.4K Baud	422	RS-485	485

50.7.2.2.6 RF Stimulus Requirements (Test Category 18).

Waveform Type	Code
SINUSOID	SIN
PULSE MODULATED	PUL

Modulation Type	Code
No Modulation	NOM
Amplitude Modulation	AMI
Frequency Modulation	FMI
Pulse Modulation	PUL

50.7.2.2.7. RF Measurement Requirements (Test Category 19).

Waveform Type	Code
Sinusoid	SIN
Amplitude Modulation	AM
Frequency Modulation	FM
Phase Modulation	PM
Pulsed AC	PUL1
Pulsed DC	PUL2
Square Wave	SQW
Triangle Wave	TRI
Arbitrary	ARB
Ramp	RMP

Modulation Type	Code
None	

50.7.2.2.8 INS Requirements (Test Category 21).

Code	UUT Type
AR57A	AR57A Communication Interface

50.7.2.2.9 Electro-Optical Requirements (Test Category 22-27).

Video or Raster Format	Code
RS-343	343
RS-170	170
A6-DRS	DRS
Digital	DIG

Laser Mode	Code
Pulsed	PUL
Single Shot	SHT

Display Type	Code
Raster	RAS
Stroke	STR
Raw Video	RAW
Composite	COM
Non Composite	NCM

Type Input Signal	Code
Composite Video	COM
Analog Stroke	STR

UUT TEST REQUIREMENTS DATA FORM 4 (SHEET 1 OF ____)

PART NUMBER

NOUN NOMENCLATURE

A/N NOMENCLATURE

UUT CLAS (Maximum 1 character)

NATIONAL STOCK NO.

WORK UNIT CODE

FSCM

SM&R CODE

EMT (hours)

OFFICE CODE

EXPIRATION DATE

DATA LEVEL

DATA SOURCE

PROGRAM ELEMENT

COMMODITY

UUT TEST REQUIREMENTS DATA FORM 4 (SHEET ___ OF ___)

PART NUMBER _____

DC POWER SUPPLY REQUIREMENTS					TEST CATEGORY 01
VOLTAGE		VOLTAGE TOLERANCE	LOAD CURRENT CAPABILITY	RIPPLE	QUANTITY
HIGH	LOW				
(VOLTS)	(VOLTS)	(VOLTS)	(AMPS)	(P-P VOLTS)	(NO.)

Instructions:
(1) There should be one entry for each UUT pin that requires a different DC supply voltage.
(2) If the UUT has several pins with the same voltage applied, the current can be summed and entered as a single requirement.
(3) Voltage tolerance should be entered as a single requirement.
(4) Ripple should be entered in peak to peak volts.
(5) If a supply is used to provide a DC reference voltage (to one or more pins), the range of operation can be entered in the high or low voltage fields.
(6) The high voltage field must be filled in.

UUT TEST REQUIREMENTS DATA FORM 4 (SHEET ___ OF ___)

PART NUMBER

AC POWER SUPPLY REQUIREMENTS								TEST CATEGORY 02
VOLTAGE		VOLTAGE TOLERANCE	CURRENT CAPACITY	FREQUENCY		FREQUENCY TOLERANCE	NUMBER PHASES	QTY
HIGH RMS VOLTS	LOW RMS VOLTS	RMS VOLTS	AMPS	HIGH HZ	LOW HZ	HZ	NO.	NO.

Instructions: (1) Voltage and voltage tolerance should be entered in rms volts.
(2) The high voltage and high frequency fields must be filled in.

UUT TEST REQUIREMENTS DATA FORM 4 (SHEET ___ OF ___)

PART NUMBER _____

DC MEASUREMENT REQUIREMENTS. DC VOLTAGE MEASUREMENT		TEST CATEGORY 03
VOLTAGE		ACCURACY
HIGH (VOLTS)	LOW (VOLTS)	%

Instructions (1) High and low voltages should be entered in volts.
(2) Accuracy should be entered as a percentage of the low voltage.
(3) The high voltage and low voltage fields must be filled in.

UUT TEST REQUIREMENTS DATA FORM 4 (SHEET ___ OF ___)

PART NUMBER _____

DC MEASUREMENT REQUIREMENTS DC CURRENT MEASUREMENT		TEST CATEGORY 04
CURRENT		ACCURACY
HIGH (AMPS)	LOW (AMPS)	%

Instructions: (1) High and low current should be entered in amps.
(2) Current accuracy should be entered in percent.
(3) Since the current values are entered in amps, 5 milliamps should be entered either as 0.005 or 5.E-3.
(4) The high current and low current fields must be filled in.

UUT TEST REQUIREMENTS DATA FORM 4 (SHEET ___ OF ___)

PART NUMBER

DC MEASUREMENT REQUIREMENTS RESISTANCE MEASUREMENT	TEST CATEGORY 05

MAXIMUM RESISTANCE
(OHMS)

Instructions: (1) The maximum resistance must be entered in ohms.
(2) Do not use "open" or "short" for the resistance value.

UUT TEST REQUIREMENTS DATA FORM 4 (SHEET ___ OF ___)

PART NUMBER _____

ANALOG STIMULUS REQUIREMENTS PULSE GENERATOR					TEST CATEGORY 06	
PULSE REPETITION PERIOD	PULSE WIDTH	RISE TIME	FALL TIME	DELAY TIME	VOLTAGE	
(SEC)	(SEC)	(SEC)	(SEC)	(SEC)	HIGH (VOLTS)	LOW (VOLTS)

Instructions:
(1) Delay time should be the time from the start of the waveform and the first pulse.
(2) Time values are entered in sec.; thus 5 millisec should be entered either as 0.005 or 5.E-3 and 10 nanosec should be entered either as 10.E-9 or 1.E-8
(3) Voltage at the top (such as: peak) of the pulse is entered in voltage high.
(4) Voltage at the bottom of the pulse is entered in voltage low.

UUT TEST REQUIREMENTS DATA FORM 4 (SHEET ___ OF ___)

PART NUMBER

ANALOG STIMULUS REQUIREMENTS WAVEFORM GENERATION						TEST CATEGORY 07	
WAVEFORM TYPE (SIN, SQW, TRI)	FREQUENCY		WAVEFORM AMPLITUDE		MOD TYPE	CURRENT	
CODE	HIGH (HZ)	LOW (HZ)	HIGH (VOLTS)	LOW (VOLTS)	CODE	MAX (AMPS)	MIN (AMPS)

Instructions:

(1) Frequency values are entered in Hz; thus, 5 MHz should be entered wither as 5000000. or 5.E+6.
(2) The codes for waveform and modulation type are in paragraph 50.7.2.2.1.
(3) Each waveform requirement should be entered on a separate line.
(4) For high and low amplitudes, enter the actual voltage values in the appropriate dimension for that waveform type in standard electrical engineering terminology. (such as: pulse is volts peak, DC is volts, sine is RMS).

UUT TEST REQUIREMENTS DATA FORM 4 (SHEET ___ OF ___)

PART NUMBER

ANALOG MEASUREMENT REQUIREMENTS AC VOLTAGE MEASUREMENT					TEST CATEGORY 08
VOLTAGE		FREQUENCY		TYPE (P-P, RMS, ETC)	TOTAL HARMONIC CONTENT
HIGH (VOLTS)	LOW (VOLTS)	HIGH (HZ)	LOW (HZ)	(CODE)	(%)

Instructions:
(1) Frequency values are entered in Hz; thus, 5MHz should be entered either as 5000000. or 5.E+6.
(2) The codes for voltage type are in paragraph 50.7.2.2.2.
(3) Total harmonic content should be entered as a percentage of the voltage amplitude.
(4) If the voltage or frequency does not vary, the nominal value can be entered in either the high or the low column.
(5) A series of tests can be entered on a test-by-test basis or they can be entered on a single line with the high and low parameter limits specified.

UUT TEST REQUIREMENTS DATA FORM 4 (SHEET ___ OF ___)

PART NUMBER _____

ANALOG MEASUREMENT REQUIREMENTS FREQUENCY MEASUREMENT			TEST CATEGORY 09
FREQUENCY		VOLTAGE	
HIGH (HZ)	LOW (HZ)	HIGH (VOLTS)	LOW (VOLTS)

Instructions:

(1) Frequency values are entered in Hz; thus, 5MHz should be entered either as 5000000. or 5.E+6.
(2) A series of tests can be entered on a test-by-test basis or they can be entered on a single line with the high and low parameter limits specified.
(3) Voltage at the top of the measured signal is entered in voltage high.
(4) Voltage at the bottom of the measured signal is entered in voltage low.

UUT TEST REQUIREMENTS DATA FORM 4 (SHEET ___ OF ___)

PART NUMBER _____

ANALOG MEASUREMENT REQUIREMENT TIME INTERVAL MEASUREMENT			TEST CATEGORY 10
TIME INTERVAL		VOLTAGE	
MAXIMUM (SEC)	MINIMUM (SEC)	HIGH (VOLTS)	LOW (VOLTS)

Instructions:
(1) Time values are entered in sec.; thus, 5 millisec should be entered either as 0.005 or 5.E-3.
(2) A series of tests can be entered on a test-by-test basis or they can be entered on a single line with the high and low parameter limits specified.
(3) Voltage at the top of the measured signal is entered in voltage high.
(4) Voltage at the bottom of the measured signal is entered in voltage low.

UUT TEST REQUIREMENTS DATA FORM 4 (SHEET ___ OF ___)

PART NUMBER

ANALOG MEASUREMENT REQUIREMENTS COMPLEX WAVEFORM MEASUREMENT					TEST CATEGORY 11	
WAVEFORM TYPE	FREQUENCY		WAVEFORM AMPLITUDE		MODULATION TYPE	SIGNAL TYPE
CODE	HIGH (HZ)	LOW (HZ)	HIGH (VOLTS)	LOW (VOLTS)	CODE	CODE

Instructions:

(1) Frequency values are entered in Hz; thus, 5MHz should be entered either as 5000000. or 5.E+6.
(2) A series of tests can be entered on a test-by-test basis or they can be entered on a single line with the high and low parameter limits specified.
(3) The codes waveform, modulation, and signal type are in paragraphs 50.7.2.2.1 and 50.7.2.2.3.
(4) For high and low amplitudes, enter the actual voltage values in the appropriate dimension for that waveform type in standard electrical engineering terminology (such as: pulse is volts peak, DC is volts, sine is RMS).

UUT TEST REQUIREMENTS DATA FORM 4 (SHEET ___ OF ___)

PART NUMBER

ANALOG MEASUREMENT REQUIREMENTS PULSE MEASUREMENT					TEST CATEGORY 12	
PULSE REPETITION PERIOD	PULSE WIDTH	RISE TIME	FALL TIME	DELAY TIME	VOLTAGE	
(SEC)	(SEC)	(SEC)	(SEC)	(SEC)	HIGH (VOLTS)	LOW (VOLTS)

Instructions:
(1) Delay time should be the maximum time between any two channels required simultaneously.
(2) Time values are entered in sec., thus, 5 millisec should be entered either as 0.005 or 5.E-3.
(3) Voltage at the top of the pulse is entered in voltage high.
(4) Voltage at the bottom of the pulse is entered in voltage low.

UUT TEST REQUIREMENTS DATA FORM 4 (SHEET ___ OF ___)

PART NUMBER

DIGITAL TEST REQUIREMENTS STIMULUS/MEASUREMENT								TEST CATEGORY 13
NO. PINS IN LOGIC FAMILY	PIN TYPE	MAX DATA RATE	VOLTAGE HIGH		VOLTAGE LOW		MAX DRIVE CURRENT	LOGIC TYPE
(NO.)	(CODE)	(BITS/ SEC)	VOLTS	TOL (%)	VOLTS	TOL (%)		

Instructions: (1) For the logic family, make an entry for the total number of unique stimulus(s), measurement (m), and bidirectional (b) pins.
(2) Max drive current is the maximum single channel drive current on any pin within a logic family.
(3) The codes for pin type and logic types are in paragraph 50.7.2.2.4.

UUT TEST REQUIREMENTS DATA FORM 4 (SHEET ___ OF ___)

PART NUMBER

RESISTIVE LOAD REQUIREMENTS				TEST CATEGORY 14
RESISTANCE		ACCURACY	MAXIMUM POWER DISSIPATION	QUANTITY
MAXIMUM	MINIMUM			
(OHMS)	(OHMS)	(%)	(WATTS)	(NO.)

Instructions: (1) The accuracy value supplied should be associated with the minimum resistance.

UUT TEST REQUIREMENTS DATA FORM 4 (SHEET ___ OF ___)

PART NUMBER

SYNCHRO/RESOLVER
STIMULUS REQUIREMENTS — TEST CATEGORY 15

VOLTAGE	ACCURACY		HARMONIC CONTENT	MAX RATE	ANGULAR RANGE		ACCURACY	
	(+)	(-)			MAX	MIN	FINE (+/-)	COARSE (+/-)
(VOLTS)	(%)	(%)	(%)	(DEG/ SEC)	(DEG)	(DEG)	(DEG)	(DEG)

SYNCHRO/RESOLVER
STIMULUS REQUIREMENTS (CONTINUED)

RESOLUTION		INPUT BREAKDOWN VOLTAGE		REFERENCE IMPEDANCE	OUTPUT DRIVE	REFERENCE FREQUENCY		ACCURACY	
FINE (+/-)	COARSE (+/-)	(+)	(-)			MAX	MIN	(+)	(-)
(DEG)	(DEG)	(VOLTS)		(OHMS)	(VA)	(HZ)	(HZ)	(% NOM)	

Instructions: (1) The voltage and maximum rate fields must be filled in

UUT TEST REQUIREMENTS DATA FORM 4 (SHEET ___ OF ___)

PART NUMBER _____

SYNCHRO/RESOLVER MEASUREMENT REQUIREMENTS							TEST CATEGORY 16
VOLTAGE	FREQUENCY		MAX RATE	ANGULAR RANGE		ACCURACY	
	MAX	MIN		MAX	MIN	FINE (+/-)	COARSE (+/-)
(VOLTS)	(HZ)	(HZ)	(DEG/SEC)	(DEG)	(DEG)	(DEG)	(DEG)

SYNCHRO/RESOLVER MEASUREMENT REQUIREMENTS (CONTINUED)				
RESOLUTION		INPUT BREAKDOWN VOLTAGE		REFERENCE IMPEDANCE
FINE (+/-)	COARSE (+/-)	(+)	(-)	
(DEG)	(DEG)	(VOLTS)		(OHMS)

Instructions: (1) The voltage and maximum rate fields must be filled in.

UUT TEST REQUIREMENTS DATA FORM 4 (SHEET ___ OF ___)

PART NUMBER _____

INTERFACE BUS REQUIREMENTS		TEST CATEGORY 17
BUS TYPE (1553, 488, 232, ETC.)	NUMBER OF CHANNELS	DATA RATE
(CODE)	(NO.)	(BITS/SEC)

Instructions: (1) The codes for bus type are in paragraph 50.7.2.2.5
(2) Date rate should be entered as the maximum transmission rate per channel. Example: an 8-line parallel bus transmitting data at 1 Mhz should be entered as 8000000.0 or 8.+E6 bits/sec.

UUT TEST REQUIREMENTS DATA FORM 4 (SHEET ___ OF ___)

PART NUMBER

RF STIMULUS REQUIREMENTS									TEST CATEGORY 18
WAVE FORM TYPE	FREQUENCY		OUTPUT POWER RANGE SIGNAL POWER		OUTPUT POWER TOLER-ANCE AT 0 DBM	MODULA-TION TYPE	DIGITAL MODULA-TION DATA RATE	PHASE SHIFT RANGE	CHARAC-TERIS-TIC IMPE-DANCE
CODE	HIGH HZ	LOW HZ	HIGH DBM	LOW DBM	DBM	CODE	BITS/ SEC	DEG	OHMS

Instructions: (1) Frequency values are entered in Hz; thus, 5 MHz should e entered either as 5000000. or 5.+E6.
(2) The codes for waveform and modulation type are in paragraph 50.7.2.2.6.
(3) Enter the waveform type code if appropriate or leave the field blank.

UUT TEST REQUIREMENTS DATA FORM 4 (SHEET ___ OF ___)

PART NUMBER _____

RF MEASUREMENT REQUIREMENTS							TEST CATEGORY 19
WAVE FORM TYPE	FREQUENCY		INPUT POWER RANGE SIGNAL POWER		MODULATION TYPE	DIGITAL MODULATION DATA RATE	CHARACTERISTIC IMPEDANCE
CODE	HIGH HZ	LOW HZ	HIGH DBM	LOW DBM	CODE	BITS/SEC	OHMS

Instructions: (1) Frequency values are entered in Hz; thus, 5 MHz should be entered either as 5000000. or 5.+E6.
(2) The codes for waveform and modulation type are in paragraph 50.7.2.2.6.

UUT TEST REQUIREMENTS DATA FORM 4 (SHEET ___ OF ___)

PART NUMBER _____

PNEUMATIC REQUIREMENTS								TEST CATEGORY 20
STATIS PRESSURE				PITOT (TOTAL) PRESSURE				CAPACITY
HIGH (IN. HG)	LOW (IN. HG)	ACCURACY (IN. HG)	CHANGE RATE (FT/MIN)	HIGH (IN. HG)	LOW (IN. HG)	ACCURACY (IN. HG)	CHANGE RATE (KNOTS/ MIN)	(CUBIC INCHES)

Instructions: (1) High and low pressures should be entered in inches of mercury.
(2) Pressure change rate accuracy should be entered in the units shown.
(3) The high pressure and pressure change rate fields must be filled in.

UUT TEST REQUIREMENTS DATA FORM 4 (SHEET ___ OF ___)

PART NUMBER

INS REQUIREMENTS	TEST CATEGORY 21

UUT TYPE
CODE

Instructions: (1) The code for INS is in paragraph 50.7.2.2.8.

UUT TEST REQUIREMENTS DATA FORM 4 (SHEET ___ OF ___)

PART NUMBER

ELECTRO-OPTICAL REQUIREMENTS FLIR											TEST CATEGORY 22
OPTICAL BANDPASS		APER-TURE	IFOV		FOV		SPATIAL BANDPASS		BORE-SIGHT ALIGN-MENT	STABI-LIZED PLAT-FORM	OUTPUT VIDEO FORMAT
HIGH	LOW		X	Y	X	Y	HIGH	LOW			
MICRONS		SQ CM	RADIANS		DEGREES		HZMRAD		RAD	1=YES 0=NO	CODE

ELECTRO-OPTICAL REQUIREMENTS LASER DESIGNATORS						TEST CATEGORY 23
WAVELENGTH	APERTURE	OUTPUT POWER	BEAM DIVERGENCE	PULSE WIDTH	STABILIZED PLATFORM	LASER MODE
MICRONS	SQ CM	JOULES	MILLIRAD	SEC	1 = YES 0 = NO	CODE

ELECTRO-OPTICAL REQUIREMENTS LASER RANGE FINDERS						TEST CATEGORY 24
WAVELENGTH	APERTURE	RECEIVER INPUT POWER RANGE		PULSE WIDTH	BORESIGHT ALIGNMENT	STABILIZED PLATFORM
		HIGH	LOW			
MICRONS	SQ CM	WATTS/SQ CM		SEC	RAD	1=YES 0=NO

Instructions: (1) See special instructions in paragraph 50.7.1.2
(2) The EO codes are in paragraph 50.7.2.2.9.
(3) Spatial bandpass should be entered in hertz per milliradian.

UUT REQUIREMENTS DATA FORM 4 (SHEET ___ OF ___)

PART NUMBER

ELECTRO-OPTICAL REQUIREMENTS TV SYSTEMS									TEST CATEGORY 25
OPTICAL BANDPASS		APERTURE	FOV		SPATIAL BANDPASS		BORESIGHT ALIGNMENT	STABILIZED PLATFORM	OUTPUT VIDEO FORMAT
HIGH	LOW		X	Y	HIGH	LOW			
MICRONS		SQ CM	DEGREES		HZ MRAD		RADIANS	1=YES 0=NO	CODE

ELECTRO-OPTICAL REQUIREMENTS MULTISPECTAL SYSTEMS COMPONENTS						TEST CATEGORY 26
FLIR	TV	LASER	LASER RANGE FINDER	TOTAL APERTURE	BORESIGHT ALIGNMENT	STABILIZED PLATFORM
1=YES 0=NO	1=YES 0=NO	1=YES 0=NO	1=YES 0=NO	SQ CM	RADIANS	1=YES 0=NO

ELECTRO-OPTICAL REQUIREMENTS DISPLAYS								TEST CATEGORY 27
TYPE DIS-PLAY	COLOR MONITOR	RASTER FORMAT	TYPE INPUT SIGNAL	MINIMUM LINE WIDTH	DISPLAY SIZE	INTENSITY RANGE		AMBIENT LIGHT INTEN-SITY CONTROL
						HIGH	LOW	
CODE	1=YES 0=NO	CODE	CODE	METERS	SQ CM	FT-LAMBERTS		1=YES 0=NO

Instructions: (1) See special instructions in paragraph 50.7.1.2
(2) The EO codes are in paragraph 50.7.2.2.9.
(3) Spatial bandpass should be entered in hertz per milliradian.

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intentionally.

60. DATA REQUIREMENTS. The following data is required to be submitted in accordance with the contract DD Form 1423.

a. DI-ATTS-91292 - Unit Under Test (UUT) Input/Output Description.

70. PREPARATION FOR DELIVERY

70.1 Packaging and Packing. Reports or data required by this standard shall be packed and packaged for delivery in accordance with the contractor's best commercial practice.

70.2 Marking for Shipments. All shipments of reports shall be marked as stated in the contract or as otherwise instructed by the procuring agency.

STANDARDIZATION DOCUMENT IMPROVEMENT PROPOSAL

INSTRUCTIONS

1. The preparing activity must complete blocks 1, 2, 3, and 8. In block 1, both the document number and revision letter should be given.
2. The submitter of this form must complete blocks 4, 5, 6, and 7.
3. The preparing activity must provide a reply within 30 days from receipt of the form.

NOTE: This form may not be used to request copies of documents, nor to request waivers, or clarification of requirements on current contracts. Comments submitted on this form do not constitute or imply authorization to waive any portion of the referenced document(s) or to amend contractual requirements.

I RECOMMEND A CHANGE:	1. DOCUMENT NUMBER	2. DOCUMENT DATE (YYMMDD)
	MIL-STD-2165A	1 FEBRUARY 1993

3. DOCUMENT TITLE
TESTABILITY PROGRAM FOR SYSTEMS AND EQUIPMENTS

4. NATURE OF CHANGE *(Identify paragraph number and include proposed rewrite, if possible. Attach extra sheets as needed.)*

5. REASON FOR RECOMMENDATION

6. SUBMITTER

a. NAME (Last, First, Middle Initial)	b. ORGANIZATION	
c. ADDRESS (Include Zip Code)	d. TELEPHONE (Include Area Code) (1) Commercial (2) AUTOVON (If applicable)	7. DATE SUBMITTED (YYMMDD)

8. PREPARING ACTIVITY

a. NAME	b. TELEPHONE (Include Area Code)	
TECHNICAL POINT OF CONTACT (TPOC): M. DIAMOND, SEA 04DS4 COMMANDER, NAVAL SEA SYSTEMS COMMAND	(1) Commercial (703) 602-2224	(2) AUTOVON 8-332-2224
c. ADDRESS (Include Zip Code) 2531 NATIONAL CENTER BLDG 3 WASHINGTON, DC 20362-5160	IF YOU DO NOT RECEIVE A REPLY WITHIN 45 DAYS, CONTACT: Defense Quality and Standardization Office 5203 Leesburg Pike, Suite 1403, Falls Church, VA 22041-3466 Telephone (703) 756-2340 AUTOVON 289 2340	

DD Form 1426, OCT 89 *Previous editions are obsolete.* 198/29