NOTICE OF CHANGE

MIL-HDBK-978-B (NASA)
NOTICE 1
1 SEPTEMBER 1989

MILITARY HANDBOOK
NASA PARTS APPLICATION HANDBOOK

TO ALL HOLDERS OF MIL-HDBK-978-B:

1. THE FOLLOWING PAGES OF MIL-HDBK-978-B HAVE BEEN REVISED AND SUPERSEDE THE PAGES LISTED:

NEW PAGE	DATE	SUPERSEDED PAGE	DATE
5-97	1 March 1988	5-97	REPRINTED WITHOUT CHANGE
5-98	1 September 1989	5-98	1 March 1988
5-99	1 September 1989	5-99	1 March 1988
5-100	1 September 1989	5-100	1 March 1988
5-101	1 September 1989	5-101	1 March 1988
5-102	1 September 1989	5-102	1 March 1988
5-103	1 September 1989	5-103	1 March 1988
5-104	1 September 1989	5-104	1 March 1988
5-105	1 September 1989	5-105	1 March 1988
5-106	1 September 1989	5-106	1 March 1988
5-107	1 September 1989	5-107	1 March 1988
5-108	1 September 1989	5-108	1 March 1988
5-109	1 September 1989	5-109	1 March 1988
5-110	1 September 1989	5-110	1 March 1988
5-111	1 September 1989	5-111	1 March 1988
5-112	1 March 1988	5-112	REPRINTED WITHOUT CHANGE

2. RETAIN THIS NOTICE AND INSERT BEFORE TABLE OF CONTENTS.

3. Holders of MIL-STD-978-B will verify that changes and additions indicated above have been entered. This notice page will be retained as a check sheet. This issuance, together with appended pages, is a separate publication. Each notice is to be retained by stocking points until the military standard is completely revised or canceled.

Custodian:
NASA-NA

Preparing activity:
NASA-NA

(Project 59GP-K079)

AMSC N/A **FSC 59GP**

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited

5.3 TRANSISTORS, HIGH POWER

5.3.6 Environmental considerations. Refer to paragraph 5.1.6.2 Environmental considerations.

5.3.7 Reliability considerations. Refer to paragraph 3.1.6 Reliability consideration, for a complete list of failure mechanisms and application considerations.

5.4 TRANSISTORS, FIELD EFFECT

5.4.1 Introduction. The field-effect transistor (FET) is a semiconductor device in which the flow of charge carriers is controlled by a charge on the gate electrode. Unlike conventional transistors, which are bipolar devices (i.e. performance depends on the interaction of two carriers: holes and electrons), field-effect transistors are unipolar devices. Their operation is basically a function of only one type of carrier: holes in p-channel devices, and electrons in n-channel devices.

There are two basic types of FET devices: the junction FET (JFET) and the metal-oxide-semiconductor FET (MOSFET). Either can be structured to operate in depletion-mode or enhancement-mode. However, enhancement-mode JFETs are very rare. Both JFETs and MOSFETs are available as either p- or n- channel devices.

The forebear of the power MOSFET is not a MOSFET but a junction field effect transistor (JFET). This development will be discussed further in the section on basic structures (5.4.3). Since the introduction of the power MOSFET in 1975, technological advances have made them a rapidly growing industry. As a result, device specifiers can become overwhelmed by the various assortment of trade names available in the power MOSFET marketplace, including SIPMOS Siemens, HEXFET, International Rectifier, MOSPOWER, and Siliconix.

5.4.1.1 JFET operation. JFET operation is based on pn junction behavior. Figure 79 illustrates a basic silicon pn junction.

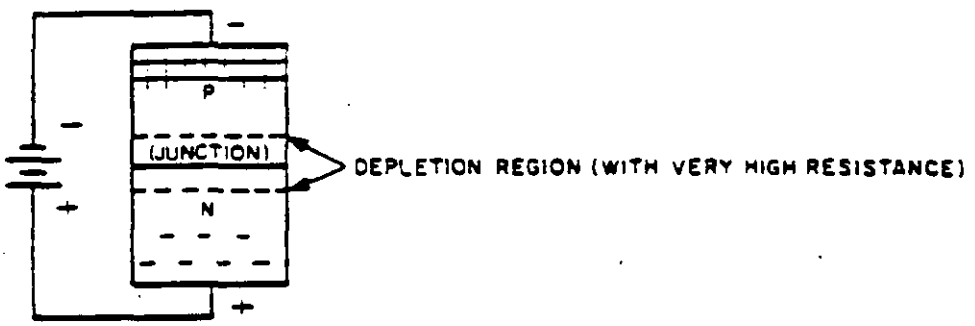


FIGURE 79. Basic silicon pn junction.

With the voltage connected as shown, the junction is reverse biased because the positive and negative carriers (holes and electrons) are attracted away from the junction. The empty area created at the junction is the key to JFET operation. This area is called the depletion region and contains neither holes nor free electrons in sufficient quantity for easy current flow: therefore, resistance is very high. Only a small leakage current flows.

The JFET can best be described as a bar of n-type silicon with two p-type regions diffused into it as shown in Figure 80.

5.4 TRANSISTORS, FIELD EFFECT

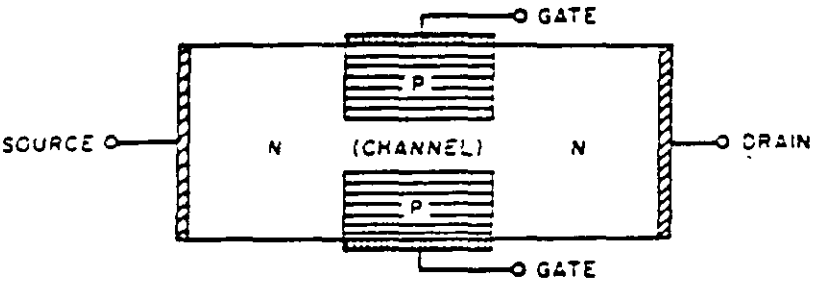


FIGURE 80. Physical configuration of an n-channel JFET

The n-region between the two p-regions is called the channel. The source connection is so named because this is the source of the carriers which enter the device. The opposite connection is called the drain because this is where the carriers flow out. The gate terminals (which are normally connected together to one lead of the device or one external circuit connection) control the turn-on and turn-off.

In the configuration shown in Figure 81A, both junctions are reverse biased and a depletion region is created at the pn junction. If these regions extend across the channel and meet, a pinch-off condition is developed.

If a small positive voltage is applied on the drain as shown in Figure 81B, the two depletion regions are widened even more because of the reverse biased voltage.

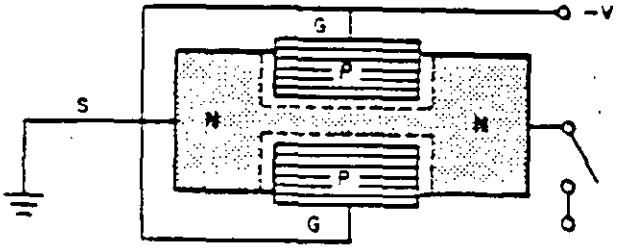
As reverse biased voltage is increased, the width of these depletion areas will extend completely through the channel and meet at one point, as shown in Figure 81C. In this condition, the channel for drain-source current (I_{DS}) flow is pinched off.

The voltage value at which this condition occurs is a parameter normally specified on JFET data sheets as the gate-source cutoff voltage ($V_{GS(off)}$). Raising the voltage above $V_{GS(off)}$ will result in no appreciable decrease in I_{DS}.

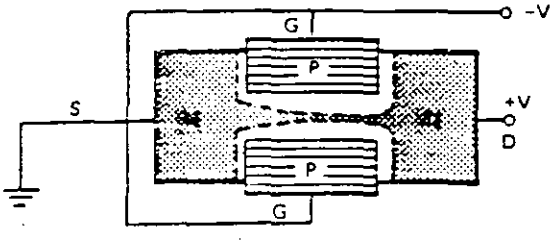
From the discussion above it can be seen that the JFET transistor is a voltage-control device which can perform the complete switching function.

The operation of a p-channel JFET is the same, except that the polarities are reversed.

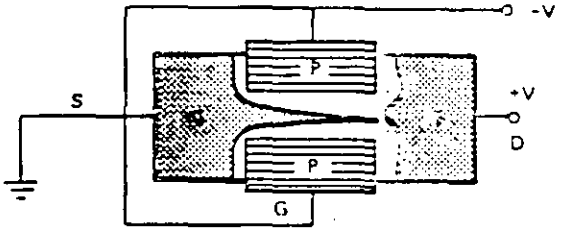
5.4 TRANSISTORS, FIELD EFFECT



A. Gate biased and drain unbiased



B. Gate and drain biased



C. Pinched off condition

FIGURE 81. Operation of an n-channel JFET

5.4.1.2 MOSFET basic operation. Due to the electrically isolated gate, a MOSFET can be described as a high-input-impedance, voltage controlled device. As a majority-carrier semiconductor, a MOSFET stores no charge, and so can switch in the nanosecond range. MOSFETs may be operated in either the enhancement mode or the depletion-mode, as described in the following paragraphs. The key to MOSFET operation is the creation of the inversion channel beneath the gate. This conversion is called the surface-inversion phenomenon. In effect, the MOSFET ceases to be an n-p-n device. Current is allowed to flow through the p region which has essentially changed into an n-type region. This results in an n-n-n type device. Thus the operation of a MOSFET is entirely different than the operation of the bipolar transistor, which always retains its n-p-n character. A useful by-product of the MOSFET process is the internal parasitic diode formed between the source and the drain. There is no equivalent for this diode in a bipolar transistor (other than a Darlington transistor). Its characteristics make it useful as a clamp diode in inductive-load switching.

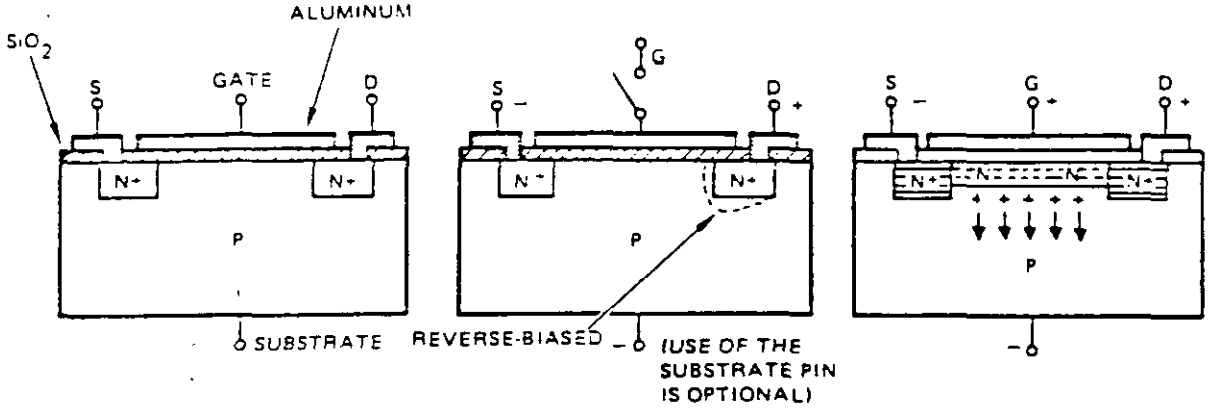
5.4.1.2.1 Enhancement-mode MOSFETs. Figure 82A illustrates an unbiased enhancement-mode device.

An aluminum plate (gate) and the p-type substrate form equivalent plates of a capacitor, with the silicon dioxide acting as a dielectric. The other aluminum areas are used as bonding pads for the source and drain connections. If voltage is applied between the

source and drain, only leakage current flows, because the pn junction will be reverse biased (gate open), as shown in Figure 82B.

In order to make the device conduct, a positive charge is applied to the gate. Because unlike charges attract, the available free electrons in the substrate are pulled up to the area under the silicon dioxide, as illustrated in Figure 82C. This concentration of electrons causes the normally p-type region to become n-type in a layer between the source and drain. This induced channel allows electrons to flow from source to drain. The gate-source voltage (V_{GS}) at which I_D starts to flow is called V_{GS} threshold (V_{GSth}). This configuration of a MOSFET, which uses the induced channel principle, is called the enhancement-mode MOSFET because the current flow is enhanced by the application of gate voltage.

The operation of a p-channel enhancement-mode device is the same except that polarities are reversed.



A. Unbiased B. Drain biased C. Gate and drain biased

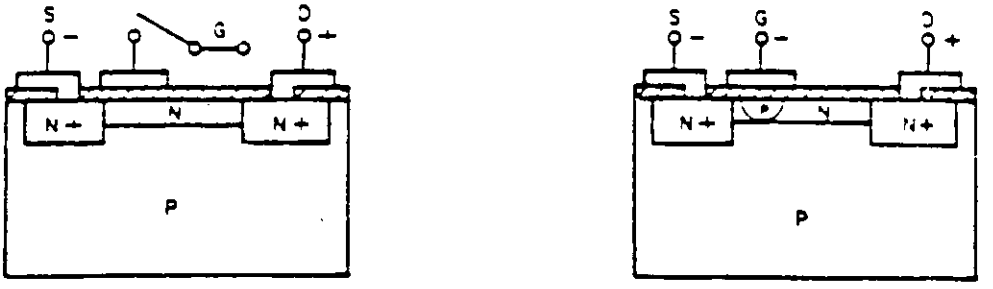
Figure 82. Operation of an n-channel enhancement-mode MOSFET

5.4.1.2.2 Depletion-mode MOSFETs. In this structure, a lightly doped n-channel is diffused into a p-material, as illustrated in Figure 83A. As a result, current will flow from source to drain with no voltage on the gate.

However, if a negative voltage is applied to the gate, the free electrons will be repelled out of the diffused channel, as illustrated in Figure 83B. This creates a current-limiting condition similar to the no-gate-voltage condition of the enhancement-mode MOSFET described previously. The V_{GS} required to achieve cutoff I_D is also called $V_{GS(off)}$ as in a JFET device.

Again, the operation of a p-channel depletion-mode device is the same except the polarities are reversed.

5.4 TRANSISTORS, FIELD EFFECT



A. Drain biased

B. Gate and drain biased

FIGURE 83. Operation of an n-channel depletion-mode MOSFET.

5.4.1.2.3 Power MOSFETs. Most commercially available power MOSFETs operate in either the n- or p-channel enhancement mode. The power MOSFET differs from the MOS transistor in that it has a short channel length and the ability to withstand high drain-to-source voltages. This is because of the separation of the active or channel region of the device from the region that sustains the drain-to-source voltage. In a long-channel MOSFET, the drain current is related to voltage by the square law relationship of the transistor current and the gate-to-source voltage. In the power MOSFET with its short channel lengths, the carrier velocity in the channel region saturates under even moderate drain-to-source voltages as a result of the interaction between the carriers. When this velocity saturation occurs, drain current is linearly related to the gate-to-source voltages by the equation:

$$I_D = C_o Z V_{SAT}(V_{GS}-V_T)$$

where V_{sat} = saturation velocity of an electron in silicon
C_O = capacitance per unit of the gate oxide
Z = width of channel

These differences will be further discussed in the paragraphs on structure. The p-channel power MOSFETS are larger than n-channel power MOSFETs. With this increased size comes increased capacitance.

5.4.2 Usual applications. FET technology can be used in a wide range of applications. This by no means implies that FETs will replace the widely-known bipolar transistor in every case. Because FET characteristics vary from those of bipolar devices it is often possible to design technically superior and sometimes less expensive circuits. The following list of FET applications demonstrates the versatility of the FET family:

5.4 TRANSISTORS, FIELD EFFECT

Amplifiers:	Switches:	Other Uses:
Small Signal	Chopper-type	Current Limiters
Low Distortion	Analog Gate	Voltage-Controlled Resistors
High Gain	Commutator	Mixers
Low Noise		Oscillators
Selective		
D.C.		
High Frequency		

Current popular applications of the power MOSFET devices are in switching power supplies, hammer drivers, audio amplifiers, motor speed control, AM transmitters, and induction heating systems. Again, it is almost never sufficient to make a one-to-one substitution for a bipolar transistor in an otherwise unmodified circuit. For example, lower drive requirements of the FETs mean significant simplification in the drive circuitry, and faster switching speeds offer the possibility of lower losses. Key parameters necessary for design and applications engineers are discussed in 5.4.5 Electrical characteristics.

5.4.2.1 FET advantages. As mentioned earlier, the FET has several inherent advantages over bipolar transistors because of the unique construction and method of operation of the field-effect device. These include low noise, no thermal runaway, low distortion and negligible intermodulation products, high impedance at low frequencies, very high dynamic range (>100dB), zero temperature coefficient Q point, and junction capacitance independent of device current. Three basic common-source circuits illustrating three biasing schemes used to establish an FET's operating point (Q point) are shown here. These schemes are constant-voltage bias, constant-current bias, and self-bias (also called source bias).

5.4.2.1.1 Constant-voltage bias. This circuit would be most useful for rf and video amplifiers employing small dc drain resistors. The transfer characteristic is a plot of I_D vs V_{GS} for constant V_{DS}. Since the curve doesn't change much with changes in V_{DS}, it is useful in establishing operating bias points. This circuit is shown in Figure 84 for a typical 2N4339 FET with its corresponding transfer curve. The Input signal(e_g) moves the load line horizontally. Large input signals, as noted in the illustration, could cause severe distortion of the output characteristics. The heavy vertical line at V_{GS} = -0.4V establishes the Q point of Figure 84. Excursions of the input signal shifting the bias line develop the output signal current.

5.4.2.1.2 Constant-current bias. In this circuit, the input signal excursion merely shifts the bias line horizontally and produces no gate-source voltage excursion. This bias technique is best suited for low-drift dc amplifier applications, such as source followers and source-coupled differential pairs. Figure 85 illustrates the constant-current bias circuit which fixes the output voltage for any R_D. Input signals cannot affect the output unless the current source is bypassed.

5.4 TRANSISTORS, FIELD EFFECT

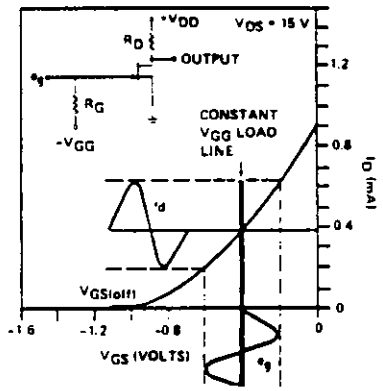


Figure 84. Constant voltage bias circuit

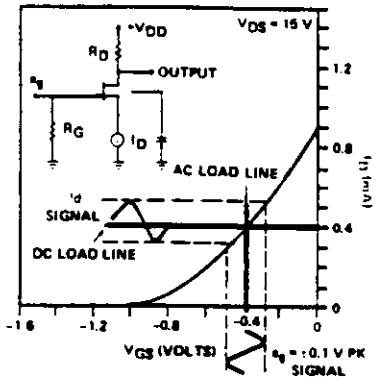


Figure 85. Constant current bias circuit

5.4.2.1.3 Self-bias. Self-bias is also referred to as source bias, or automatic bias. This scheme is particularly useful in AC amplifiers. Figure 86 illustrates the self-biased circuit with a load line passing through the origin. Bypassing R_S will steepen the slope. Signal development is the same as in the case of a partially bypassed (AC ground provided by a bypass capacitor across the current source) constant-current scheme except the load line is a DC bias line.

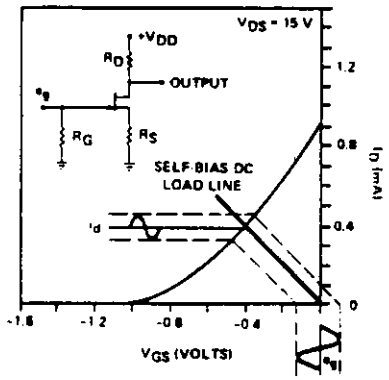


Figure 86. Self-bias.

A fourth biasing method combining the advantages of constant-current biasing and self-biasing is obtained by combining the constant voltage circuit with the self-bias circuit. A principal advantage of this system is that it can be made to constant-current bias without any additional power supply requirements.

5.4.2.2. Power MOSFETs. A common application of power MOSFETs is in switching schemes. Care must be taken in developing the circuit layout, and using the integral body-drain diode. Gate-to-source and drain-to-source voltage spikes must also be avoided. Self-inflicted over voltage transients can be produced when the device is switched off. This is a result of inductance in the circuit. The faster the device is switched, the higher the overvoltage will be. Inductance is always present to some degree in a practical circuit, and therefore there is always a danger of inducing overvoltage transients when switching off. The primary approach to reducing this problem is to

minimize stray circuit inductance by careful circuit layout. A clamping device should be connected as close to the drain and source terminals as possible. A convertible zener diode or a "transorb" device is suitable for this purpose. Stray inductance slows down the switching speed and causes unexpected imbalance of current between parallel connected devices in addition to undesirable oscillations. Care should be taken to keep circuit layout symmetrical.

5.4.3 Physical construction.

5.4.3.1 Die structure. Figure 87 illustrates basic JFET structures. Figure 87a shows the basic enhancement-mode MOSFET. This can easily be compared to the two examples of vertical technology power MOSFETs in Figures 87c and d, where the source and gate are located on the top of the chip and the drain is located below. The evolution of the power MOSFET structure can be traced to limitations of the JFET structure. The key to the problem is channel length. MOSFET channel length is inversely proportional to forward transconductance and directly proportional to on-resistance. The double-diffused MOS "DMOS" FET was one of the earliest successful efforts in short channel MOSFET technology. Similar is the "VMOS" with a v-groove MOSFET as shown in Figure 87c. For the most part, silicon gate has replaced metal gate technology in power MOSFET designs.

The earlier, double-diffused version of the power MOSFET had the device terminals on the top surface of the die. As the cell structure for power MOSFETs continued to evolve, the drain contact was dropped through the n-substrate to the back of the die. The double-diffused planar structure (DMOS) is shown in Figure 87d.

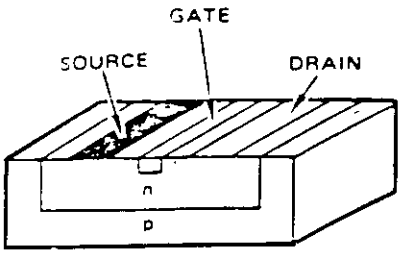


Figure 87a. Structure of an n-channel JFET.

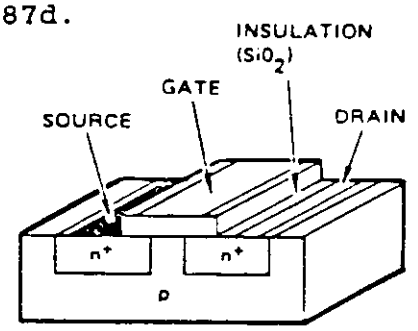


Figure 87b. Structure of an n-enhancement-mode MOSFET

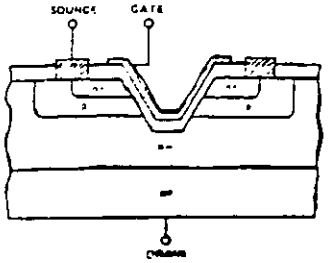


FIGURE 87c. VMOS structure of an n-channel power MOSFET

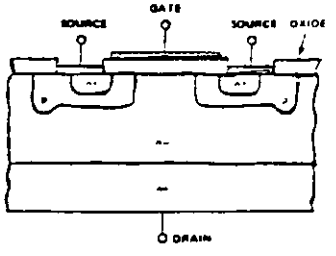


FIGURE 87d. DMOS structure of an n-channel power MOSFET

5.4 TRANSISTORS, FIELD EFFECT

5.4.3.2 Packaging. Two of the standard packages used for FET devices are the JEDEC TO-204 and TO-205 (formerly TO-3 and TO-39). Examples of the TO-204 and TO-205 are shown in Figure 88. Figure 89 illustrates a typical construction. Special heatsinking requirements are needed in many applications, especially for the thermally limited power MOSFETs. Heatsinking for power MOSFETs is required to prevent the temperature of the junction from exceeding its worst case rating. In switching applications, total power dissipated is due to conduction losses and switching losses. Switching time is essentially independent of temperature, but the conduction losses increase with temperature, and hence the drain-to-source resistance ($R_{DS(on)}$) increases. This must be taken into account when heatsinking, and is included in the calculation of thermal resistance for the heatsink. Typically, calculations of thermal resistance coefficients are available from the manufacturers' data sheets, using the temperature coefficient provided for any particular device.

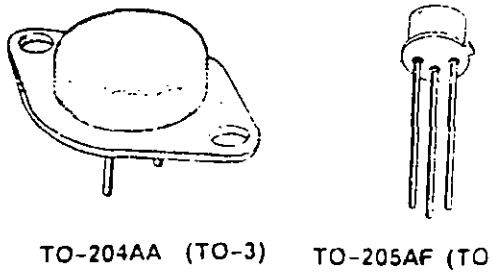


Figure 88. Typical FET packaging.

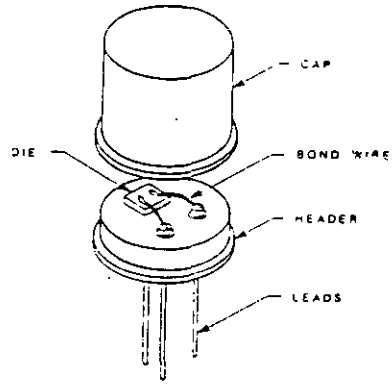


Figure 89. Typical construction

Die bonding of these devices can be achieved using either soft solder or gold eutectic. Both methods have been found to be reliable.

For wire bonding, either aluminum or gold wires are used. The wire bonding methods most frequently employed are thermocompression or ultrasonic bonding.

Package sealing is performed in an inert atmosphere using electrical welding techniques: consequently, it is possible that weld splashes may occur and cause particles to be released inside the package. However, all MIL-STD-975 devices require 100 percent PIND and X-ray testing which should detect such defects.

5.4.4 Military designation. The military designation for transistors is formulated as follows:

JANS	XN	YYYY	ZZ
Prefix	Component designation	Identification number	Suffix letter(s)

The prefix includes the level of product assurance. For NASA applications, the level of product assurance is restricted to JANTXV or JANS in accordance with MIL-STD-975.

The component designation is 2N for transistors.

The identification number is assigned in order of registration and has no other significance.

Suffix M represents matched devices, suffix S or L indicates shorter or longer terminal leads, and any other letter is used for a modified version of a device.

Any radiation hardness assurance (RHA) designation code is placed after the prefix. See MIL-S-19500 for details.

5.4.5 Electrical characteristics. All FET types have a basically similar operation. The changing charge on the gate electrode and the amount of charge in the conductive channel combine to change the drain current (see Figure 90).

5.4.5.1 FET electrical parameters. The major parameters for FET behavior are:

- I_{DSS} - Drain current with the gate shorted to the source.
- $V_{GS(off)}$ - Gate-source cutoff voltage.
- I_{GSS} - Gate-to-source current with the drain shorted to the source.
- BV_{GSS} - Common-source breakdown voltage with the drain shorted to the source.
- G_{fs} - Common-source forward transconductance.
- C_{gs} - Gate-source capacitance.
- C_{gd} - Gate-drain capacitance.

Power MOSFET major parameters also include the on-resistance, $R_{DS(on)}$. The on-resistance determines the amount of current the device can handle without excessive power dissipation. The threshold voltage $V_{GS(th)}$ is the lowest gate voltage at which a specified drain current begins to flow.

In using a power MOSFET device as a switch it is important to appreciate the gate drive power needed to activate the power MOSFET. The driver must be able to deliver sufficient current during the transition from off to on to adequately charge the input capacitor in the desired time. The following equations show that for high speed switching, driving the gate from a low impedance, high current source is certainly desirable.

$$t = 2.2\ Rg \cdot C_{in}$$
$$i = C_{in}\ dV/dT$$

5.4 TRANSISTORS, FIELD EFFECT

where R_g = input resistance
C_{in} = input capacitance
dV/dT = rate of voltage change.

The phenomenon of the Miller effect takes place as the voltage increases. Once the threshold voltage is passed, the power MOSFET begins to draw more drain current. As the current increases, transconductance rises to saturation. This increase in transconductance is proportional to the increase in gain. The once-low feedback capacitance now increases, and appears as an addition to input capacitance.

$$C_{in} = C_{iss} + (1 + A_v)C_{gd}$$

where C_{iss} = common-source input capacitance
C_{gd} = gate - drain capacitance
A_v = voltage gain

If the driver is deficient in its reserve of drive current, the switching speed will suffer. If the driver can deliver the required charging current, the switching speed is solely dependent on how fast the driver can deliver it.

The current-voltage relationship for the FET is nearly a square law: it is

$$I_D = I_{DSS}\left[1-\frac{V_{GS}}{V_{GS(off)}}\right]^2$$

where V_{GS} is the gate voltage
$V_{GS(off)}$ is the value of V_{GS} necessary to reduce the drain current to zero
I_{DSS} is the zero-gate-voltage drain current (saturation drain current)

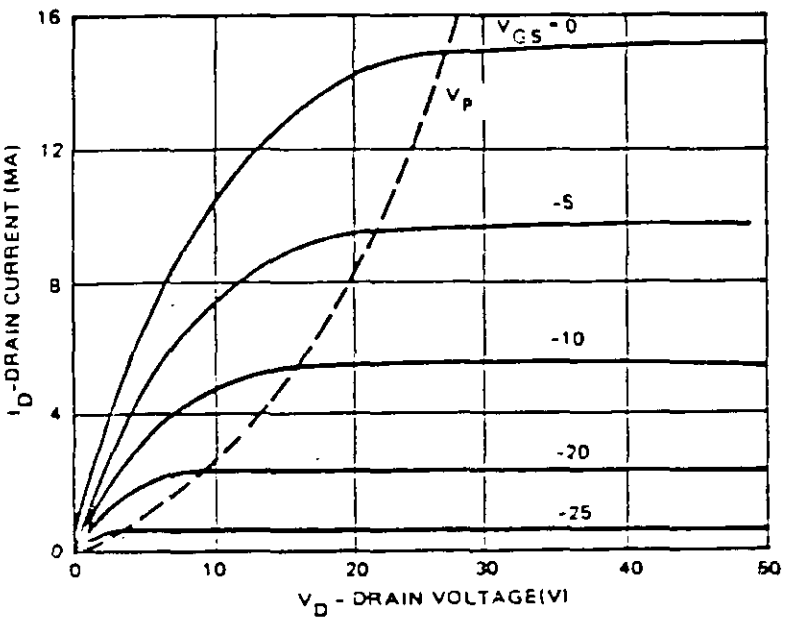


FIGURE 90. Typical output characteristics of a JFET.

5.4 TRANSISTORS, FIELD EFFECT

The square law relationship between current and the gate-to-source voltage is a dependence seen in long-channel MOS transistors under moderate gate voltages. In devices with short channel lengths, such as power MOSFETs, saturation is attained under even moderate drain-to-source voltages. As a result of the interaction between the carriers the equation is no longer valid. In this case, the drain current is linearly related to the gate-to-source voltages by the equation $I_D=CoZV_{sat}\ (V_{GS}-V_T)$, where V_{sat} is the saturation velocity of the electron in silicon.

The transconductance of the FET varies with gate voltage according to the relation:

$$G_{fs} = G_{fso}\left[1-\frac{V_{GS}}{V_{GS(off)}}\right]$$

The forward transconductance is a function of I_{DSS} and $V_{GS(off)}$ at zero drain-current.

The basic current-voltage relationship for a depletion-mode MOSFET operating in the common-source configuration is shown in Figure 91. At low drain-to-source potentials and with the gate returned to source (V_{GS} = 0), the resistance of the channel varies linearly with voltage, as illustrated in region A-B. As the drain current increases beyond point B, the voltage drop in the channel produces a progressively greater voltage difference between the gate and points in the channel which are closer to the drain. As the potential difference between the gate and the channel increases, the channel is depleted of carriers (becomes constricted). Therefore, the drain current increases at a much slower rate with further increase in drain-to-source voltage, as shown in region B-C. An additional increase in drain-to-source voltage beyond point C produces no change in drain current until point D is reached. This condition leads to the description of region B-D as the "pinch-off" region. Beyond point D, the transistor enters the "breakdown" region, and the drain current may increase dramatically. The upper curve in Figure 91 also applies to enhancement-mode MOSFETs, provided that the gate voltage V_{GS} is large enough to produce channel conduction.

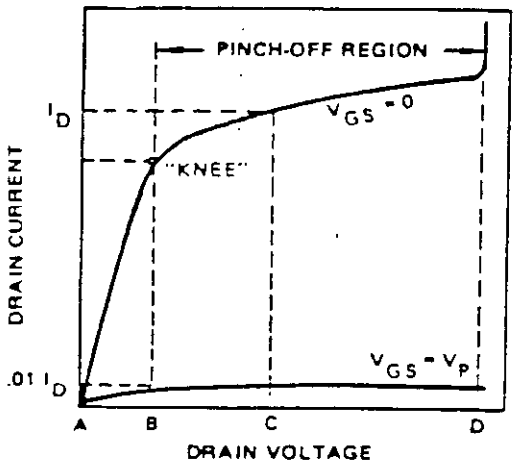


Figure 91. Basic current-voltage relationship for a depletion-mode MOSFET.

5.4 TRANSISTORS, FIELD EFFECT

A MOSFET channel may achieve self pinch-off by the intrinsic IR drop alone, by a combination of intrinsic IR drop and an external voltage applied to the gate, or by an external gate voltage alone, which has the same magnitude as the self pinch-off IR drop (V_P). In any case, channel pinch-off occurs when the sum of the intrinsic IR drop and the extrinsic gate voltage reaches V_P. The pinch-off voltage (V_P) is usually defined as the gate cutoff voltage $V_{GS(off)}$ that reduced the drain current between 0.1 and 1 percent of its zero-gate-voltage value at a specified drain-to-source voltage (this corresponds to the "knee" voltage, point B in Figure 91, of the zero-gate-voltage output characteristics).

The pinch-off region between points B and D in Figure 91 is where MOSFET transistors are especially useful as high impedance voltage amplifiers. In the ohmic region between points A and B, the linear variation in channel resistance makes the device useful in voltage-controlled resistor applications.such as the chopper unit at the input of some dc amplifiers.

Typical output-characteristic curves for n-channel MOSFETs are shown in Figure 92. (For p-channel MOSFETs, the polarity of the voltage and current are reversed.) In the pinch-off region, the dynamic output resistance, r_{os}, of the transistor may be approximated from the slope of the output-characteristic curve at any given set of conditions.

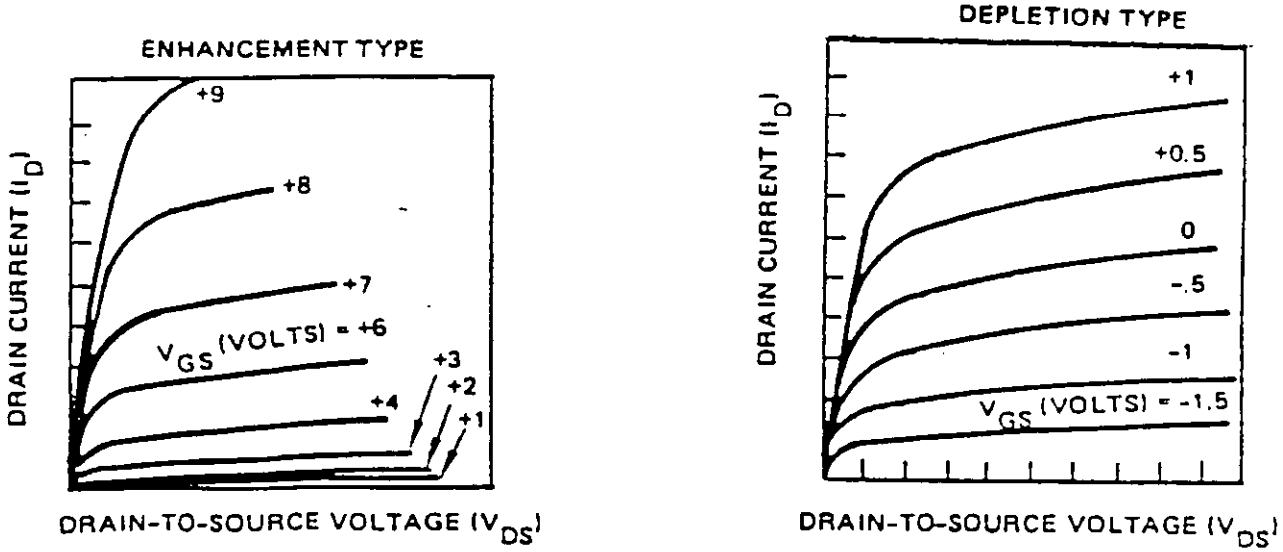
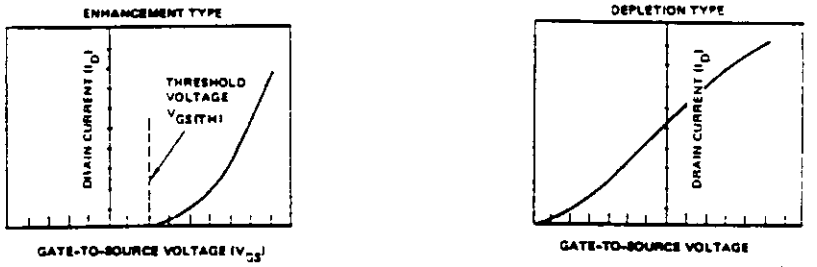


Figure 92. Typical output characteristics for n-channel MOSFETs

Typical transfer characteristics for n-channel MOSFETs are shown in Figure 93 (polarities would be reversed for p-channel devices). The threshold voltage shown in Figure 93 is an important parameter for enhancement mode MOSFETs, because it provides a desirable region of noise immunity for switching applications.

SUPERCEDES PAGE 5-110 OF MIL-HDBK-978B

5.4 TRANSISTORS, FIELD EFFECT



A. Enhancement mode B. Depletion mode

FIGURE 93. Typical transfer characteristics for an n-channel MOSFET

5.4.6 Environmental considerations. Refer to paragraph 5.1.6.3, "Environmental considerations," in the general section. Field effect transistors, like bipolar high frequency transistors, are susceptible to gate insulation damage by electrostatic discharge of energy through the devices. In some MOSFETs, diodes are electrically connected between each insulated gate and the source. These diodes do offer some protection against static discharge; however, basic ESD precautions must be utilized when handling these devices.

Power MOSFETs have heat dissipation requirements, which were mentioned in the section on packaging. The design engineer must also take into account radiation considerations (see paragraph 5.1.6.3.2). Studies show that power MOSFETs are particularly susceptible to total dose induced radiation damage. Prior to use in a critical environment, this aspect should be reviewed with a radiation specialist.

5.4.7 Reliability considerations. The failure modes seen in FETs are also commonly seen in bipolar transistors. These failure modes are discussed in paragraph 5.1.6, "Reliability considerations" in the general section.

An additional defect may arise if caution is not exercised when applying voltage to a MOSFET device. Performance of MOS transistors depends on the relative perfection of the insulating layer between the control electrode (gate) and the active channel. If this layer is punctured by an inadvertent application of excess voltage to the external gate connection, the damage is irreversible. If the damaged area is relatively small, the additional leakage may not be noticed in most applications. However, greater damage may degrade the device to the leakage levels associated with JFET transistors.

Therefore, it is very important that appropriate precautions be taken to ensure that the MOSFET gate-voltage ratings are not exceeded.

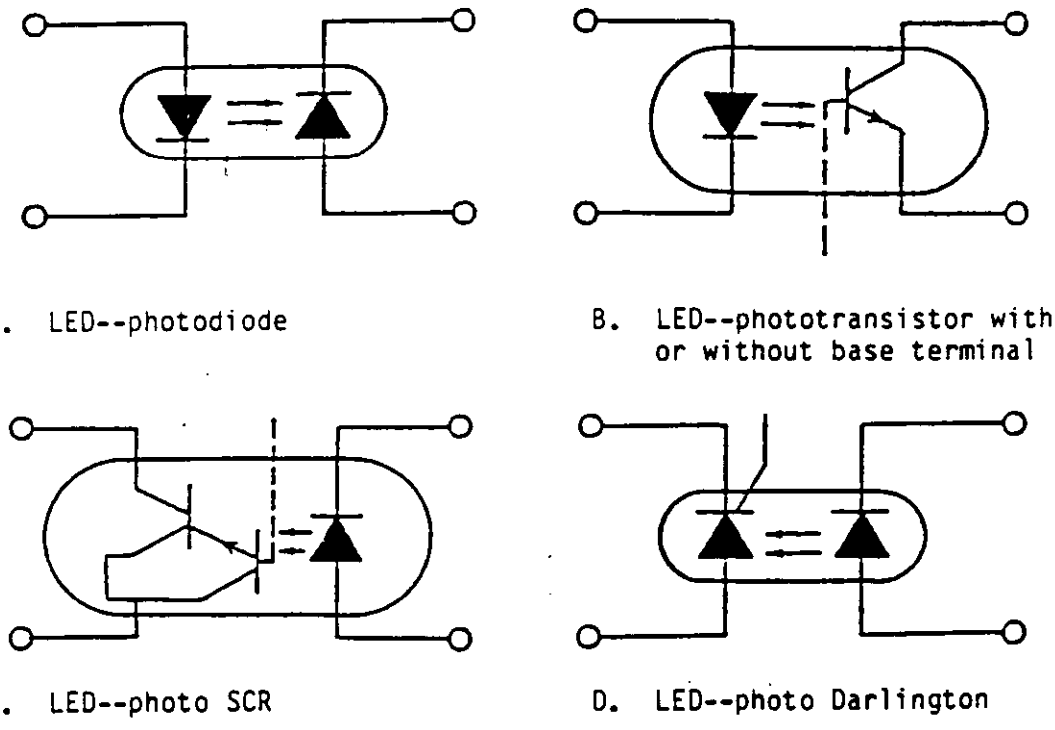
In addition, for power MOSFETs the gates of the devices are essentially capacitors, and should not be left floating or open circuited in circuits. These conditions can result in activation of the devices due to voltage buildup on the input capacitor caused by leakage currents or pickup. Gate protection by an internal monolithic zener diode connected gate-to-source is not found on power MOSFETs. therefore if gate protection is required an external zener should be used.

5.5 OPTOCOUPLERS

5.5 Optocouplers.

5.5.1 Introduction. Optically coupled isolators, also called optocouplers, are used to isolate electrical systems from each other in an electronic circuit. Optocouplers allow very good circuit control with a high degree of electrical isolation between the input and output. These isolators are ideally suited for eliminating problems such as ground loop isolation, common mode noise rejection, and electromagnetic interference. These devices replace mechanical relays and pulse transformers. Optocouplers provide electrical isolation of potentially dangerous voltages in the equipment.

An optically coupled isolator consists of a light source coupled through an optically transparent insulation to a light detector and is housed in a light-excluding package. The light source may be an incandescent or neon lamp, or a light-emitting diode (LED). The transparent insulation may be air, glass or plastic. The detector may be a photoconductor, photodiode, phototransistor, photo silicon controlled rectifier (SCR), photo Darlington, or an integrated combination photodiode/amplifier. The discussion will be limited here to optocouplers having infrared-emitting diodes (IRED) coupled to a solid state photodetector. Diagrams of some basic optically coupled isolators are shown in Figure 94.



A. LED--photodiode

B. LED--phototransistor with or without base terminal

C. LED--photo SCR

D. LED--photo Darlington

FIGURE 94. Basic types of optically coupled isolators.