NOT MEASUREMENT
SENSITIVE

MIL-HDBK-528A(AS)
14 February 2019
SUPERSEDING
MIL-HDBK-528(AS)
31 October 2017

DEPARTMENT OF DEFENSE
HANDBOOK

DESIGN FOR TESTABILITY (DFT)
FOR
BOUNDARY SCAN DIAGNOSTICS (BSD)

This handbook is for guidance only.
Do not cite this document as a requirement.

DISTRIBUTION STATEMENT A. Approved for public release; distribution unlimited.

AMSC N/A AREA ATTS

FOREWORD

1. This handbook is approved for use by the Department of the Navy and is available for use by all Departments and Agencies of the Department of Defense (DoD).

2. This handbook provides guidance on the acquisition of Boundary Scan, or JTAG, technology as part of a larger acquisition of electronic equipment.

3. This handbook is intended to aid DoD personnel in writing requirements for Boundary Scan, or JTAG, technologies as part of a system performance specification.

4. Comments, suggestions, questions or additional information on this document should be addressed to: Naval Air Warfare Center Aircraft Division, Code 4.1.2.2, Route 547, Mail Stop 120-3, Joint Base MDL, NJ 08733-5100 or emailed to michael.sikora@navy.mil. Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at https://assist.dla.mil.

CONTENTS

CONTENTS

PARAGRAPH PAGE

1. SCOPE

1.1 Scope. This handbook provides guidance for the Department of Defense (DoD) to acquire avionics systems that use Boundary Scan. This document describes the design considerations necessary for a host system to implement Boundary Scan Diagnostics (BSD). Boundary Scan is a technique used to test the interconnections between integrated circuits (ICs) on a circuit card assembly (CCAs), as well as to test the health of the ICs themselves and to load data into them. Boundary Scan can also be used in a system-level configuration between several boards. Boundary Scan is low cost and requires less physical access to circuit components than traditional testing techniques, such as In-Circuit Testing (ICT) for detecting and isolating component failures. With today's highly complex and dense circuit cards, Boundary Scan is a useful technique for troubleshooting and ensuring production quality.

The Joint Test Action Group (JTAG), an electronics industry association formed in 1985, has used Boundary Scan to develop the Institute of Electrical and Electronic Engineers (IEEE) Standard 1149.1-1990, titled "Standard Test Access Port and Boundary-Scan Architecture." This IEEE standard has become synonymous and interchangeable with the group's name. Therefore, this handbook will use the terms "Boundary Scan" and "JTAG" interchangeably. Boundary Scan/JTAG can be used at various levels of maintenance for testing avionic circuit cards. DoD can benefit from this technology as it will enhance the reliability, availability, and maintainability (RAM) of avionics and, as a result, increase operational availability (Ao) and potentially reduce the total ownership cost (TOC) of systems acquired.

Boundary Scan can test the interconnections of ICs such as Field Programmable Gate Arrays (FPGAs) and Central Processing Units (CPUs) on a CCA for short and open circuit faults. Data is sent to the IC from a piece of Automatic Test Equipment (ATE), or from a Personal Computer (PC). The output of the IC is sent back to the ATE to be examined. With multiple ICs on a CCA, the ATE sends the boundary scan test signal into the first IC and the output of this IC will be the input of the next IC, the output of the second IC will be the input to the third IC, and so on. The output of the last IC on the CCA will be sent back to the ATE for examination, thus creating a chain, also known as the "scan chain." A two-IC configuration example is shown on Figure 1. The scan chain verifies that the Boundary-Scan-enabled ICs on the CCA are communicating properly and identifies any short-circuit or open-circuit failures on the CCA.

Boundary Scan can also be used in a system-level test configuration, connecting multiple boards. Just as boundary scan can connect multiple ICs to form a scan chain, system-level boundary scan can form a chain between multiple boards, allowing testing interconnections across multiple boards using only one source. System-level boundary scan can be configured in many different topologies. Some of the proposed topologies include a ring configuration, where the scan chains of each board are each chained; this higher level scan chain would be controlled by a single boundary scan controller. Another proposed topology is a star configuration. In this topology, the controller would have access to the scan chains of all the boards, but be able to access them in parallel instead of in series. One more proposed topology has a system-level controller's boundary scan connections across the backplane connecting all the boards together. Each board's boundary scan controller interfaces with this bus, and would then provide boundary scan testing to individual boards. No matter the configuration, system-level boundary scan provides benefits in system testability, as testing would be standardized across an entire system, and only a single test sequence would be needed. Ideally, this handbook would be used in conjunction with MIL-HDBK-2165.

This document does not address security requirements associated with the implementation of boundary scan.

This handbook is for guidance only and cannot be cited as a requirement.

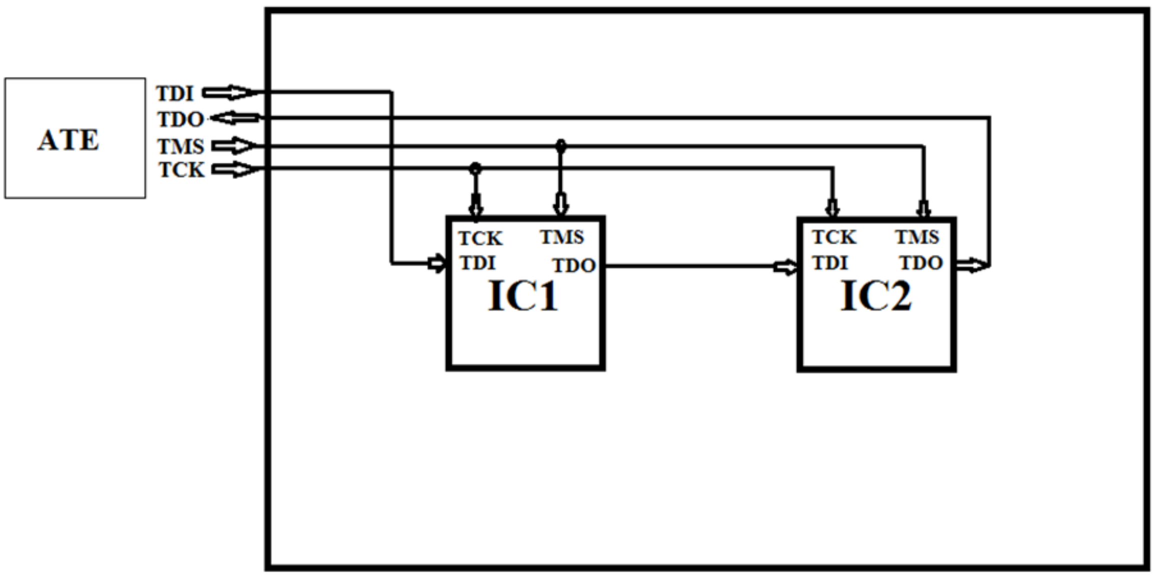

FIGURE 1. Boundary scan chain.

2. APPLICABLE DOCUMENTS

2.1 General. The documents listed below are not necessarily all of the documents referenced herein, but are those needed to understand the information provided by this handbook.

2.2 Government documents.

2.2.1 Handbook. The following handbook forms a part of this document to the extent specified herein.

DEPARTMENT OF DEFENSE HANDBOOK

MIL-HDBK-2165 Testability Program for Systems and Equipments

(Copies of this document are available at https://quicksearch.dla.mil.)

2.3 Non-Government publications. The following non-government documents form a part of this document to the extent specified herein.

INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS (IEEE)

IEEE Std 1149.1	IEEE Standard for Test Access Port and Boundary-Scan Architecture
IEEE Std 1532	IEEE Standard for In-System Configuration of Programmable Devices
IEEE Std 1687	IEEE Standard for Access and Control of Instrumentation Embedded within a Semiconductor Device

(Copies of these documents are available at https://standards.ieee.org.)

INTERNATIONAL ELECTROTECHNICAL COMMISSION (IEC)

IEC 61690-2	Electronic Design Interface Format (EDIF) Version 4.0.0

(Copies of this document are available at https://webstore.iec.ch.)

ASSET INTERTECH, INC.

ASSET-SVF-DOC	Serial Vector Format Specification

(Copies of this document are available at https://www.asset-intertech.com.)

3. ACRONYMS AND DEFINITIONS

The following acronyms are applicable to this handbook.

A_o	Operational Availability
ASIC	Application-Specific Integrated Circuit
ATE	Automatic Test Equipment
BOM	Bill of Materials
BR	Bypass Register
BSD	Boundary Scan Diagnostics
BSDL	Boundary Scan Description Language
BSR	Boundary Scan Register
CCA	Circuit Card Assembly
CPU	Central Processing Unit
DFT	Design for Test
DoD	Department of Defense

EDIF	Electronic Design Interchange Format
FPGA	Field Programmable Gate Array
FSM	Finite State Machine
I-Level	Intermediate Level of Maintenance
IC	Integrated Circuit
IJTAG	Internal Joint Test Action Group
I/O	Input/Output
IR	Instruction Register
JTAG	Joint Test Action Group
O-Level	Organizational Level of Maintenance
SRA	Shop Replaceable Assembly
SVF	Serial Vector Format
TAP	Test Access Port
TCK	Test Clock
TDI	Test Data Input
TDO	Test Data Output
TDR	Test Data Register
TMS	Test Mode Select
TRST	Test Reset
UUT	Unit Under Test
WRA	Weapons Replaceable Assembly

4. GENERAL GUIDANCE

4.1 Boundary scan overview. Boundary-scan-based DFT architectures have become inherent in modern electronics design. Boundary scan consists of four (five in some cases) signals that comprise a Test Access Port (TAP). The four signals are: Test Data Input (TDI), which is the input data inserted from the ATE into ICs on a CCA; Test Data Output (TDO), which is the output data from the ICs that gets sent back to the ATE for examination; Test Clock (TCK), which synchronizes the transfer of data and instructions among various registers on the ICs; and Test Mode Select (TMS), which acts as the sole test control input to the TAP controller. The optional fifth signal is the Test Reset (TRST), which resets the TAP Controller. An example of this Boundary Scan TAP architecture is shown on Figure 2.

Boundary Scan adds linked cells at the boundary of the IC's at each input and output pins, thus creating a register known as the Boundary Scan Register (BSR). These are the pins that the TAP signals are inserted into which test the interconnections of the ICs.

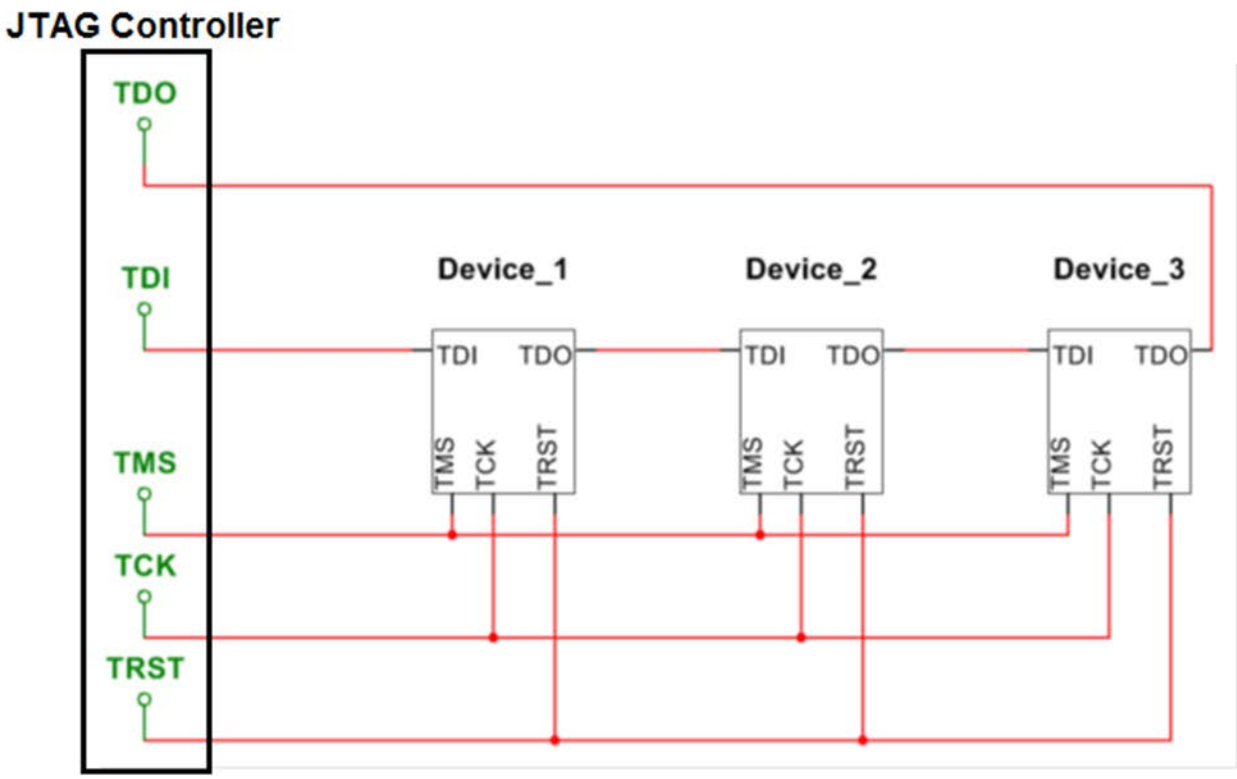

FIGURE 2. Boundary scan TAP architecture example.

5. DETAILED GUIDANCE

5.1 System design. A single TAP, ideally, can be used for both boundary scan diagnostics and programming. Therefore, standard industry practice is to avoid a design that has multiple TAPs on a single board, as it will unduly complicate the boundary scan chain. However, multiple TAPs can be used for a board or system that requires a separation of testing and programming ports for security purposes.

5.1.1 Circuit Card Assemblies (CCA) scan chain. Organize all CCAs in a system supporting boundary scan into a single scan chain. It is preferable that there is a single TAP for each boundary-scan chain, and that it will operate through this single TAP.

5.1.1.1 Multiple scan chains. Use multiple TAPs for systems whose complexity exceeds the ability to conduct boundary scan on a single scan chain. All the TAPs should be accessible by the BSD ATE.

5.1.1.1.1 One TAP per CCA. For systems that include multiple circuit boards, there should be only one TAP on each boundary-scan-enabled CCA.

5.1.2 TAP connection(s) accessibility. All boundary scan TAP connections should be available on an external connector of a Weapons Replaceable Assembly (WRA) for Operational

Level (O-level) of maintenance testing, and/or accessible on a Shop Replaceable Assembly (SRA) at the Intermediate Level (I-level) of maintenance on an edge connector. The connector should be appropriate to the intended operational environment.

5.2 Configuration Management (CM). A product, throughout its lifecycle, may be updated or redesigned several times. Boundary-scan-enabled boards each have a unique infrastructure and interconnections that are dependent on the specific internal components. Thus, each revision should be maintained and tracked by a BSD test plan separately in a configuration management plan. Track each configuration change affecting the BSD scan chain in configuration management, as applicable.

5.2.1 Data deliverables. Ensure that each CCA is delivered with its netlist, schematic, Bill of Materials (BOM), and associated Boundary Scan Description Language (BSDL) files stored under configuration management.

5.2.2 Tracking of data deliverables. Configuration management should track each revision of a CCA, including its netlist, schematic, BOM and associated BSDL files.

5.2.3 BSD data formatting. Format each netlist, schematic, BOM, and associated BSDL files in an industry standard format for that type of file. One such industry standard format is the Electronic Design Interchange Format (EDIF) for netlists and schematics. For more information regarding EDIF, see IEC 61690-2.

5.3 Routing. This section describes the boundary scan routing for the cases where boards must support device programming (as outlined in IEEE 1532), board emulation or fault detection.

5.3.1 BSD devices signal routing. All mandatory IEEE 1149.1 signals should be routed between all boundary-scan-enabled devices. If the optional TRST (active low) signal is integrated on a boundary-scan-enabled device, it should be independently accessible at the TAP interface for the device's respective chain.

5.3.2 BSD TAP connector routing. All IEEE 1149.1 boundary scan signals should be routed to a TAP connector.

5.3.3 Multi-scan chain routing. Route the boundary scan signals between each TAP connector when multiple scan chains are used. Some emulation solutions require a single device on the chain. Multiple TAPs will allow easier isolation of an infrastructure failure in that case.

5.3.4 Clock skew verification. Verify the signal integrity of a scan chain to ensure the clock skew is in compliance with IEEE 1149.1.

5.3.5 Devices using JTAG port for emulation. Place devices that use the JTAG port for emulation on a separate chain. Separating the emulation scan chain and the non-emulation scan chain precludes emulation issues.

5.4 Boundary Scan Enabled Components. Boundary scan enabled components will need to follow the listed design considerations for a successful BSD implementation.

5.4.1 Component compliance. The boundary scan component should be compliant with IEEE 1149.1.

5.4.2 Component BSD required BSDL file. The device vendor is required to supply a BDSL description to verify IEEE 1149.1 compliance. Therefore, the Unit Under Test (UUT) design activity should provide a modified version of the vendor-supplied BSDL file which accurately describes the device in its functional, post-configured state.

The vendor-supplied BSDL file should be reviewed to confirm that the BSDL description coincides with the device package specified by the UUT design activity. Special attention should be paid to ensuring that the logical port, pin mapping, and boundary-scan register descriptions corroborate with UUT design activity technical documentation. The developer-supplied BSDL file should also be reviewed to ensure that it accurately describes a device in its functional, post-configured state. This review should also include confirmation that logical port, pin mapping, and boundary-scan register descriptions corroborate with UUT design activity technical documentation.

5.4.3 Boundary-scan clock signals. The boundary scan TCK clock signals should follow the same layout convention as other CCA clock signals.

5.5 TAP placement. Boundary scan enabled circuit cards and WRA's will need to follow TAP placement requirements, in the following subsections, to ensure usability.

5.5.1 TAP signal pins separation. The TAP signal pins (TDI, TDO, TMS, TCK and TRST) should not be electrically short-circuited together.

5.5.2 Single scan chain. Wherever practical, route all boundary-scan component connections into a single scan chain, as shown on Figure 1.

5.5.2.1 Multiple TAP use. When all of the boundary scan components in a system cannot be organized into a single scan chain, then use more than one TAP.

5.5.3 TAP signals to input/output (I/O) pins. TAP signals should not be connected to I/O pins of devices in the scan chain. JTAG's flexible mode allows TAP signals to be optionally used as I/O pins on some devices. This is to preclude board designers from using TAP signals as extra I/O outside of their intended boundary scan function.

5.6 Higher-order instruction capture bits. Set the higher-order instruction capture bits to a known value so that the component can be easily identified.

5.7 Connectors, signals, and termination. The design should follow a connection scheme that will enable maintainability of the device.

5.7.1 Board connector. There are no standard JTAG connectors, but there are 10-, 16-, and 20-pin connectors which are readily available in "common" configurations specifically tailored to interface with COTS TAP controllers. Interconnect density should be capable of supporting a return path (ground) contact for each exposed TAP I/O. Interconnect durability should be rated for a minimum 500 mate/demate cycles to optimize for the in-service production environment.

5.7.2 TAP connector TDI resistor. A series damping resistor on the first device in the chain should be connected TDI pin. The resistor should be physically located as near as practical to the TDI pin.

5.7.3 TAP connector TDO resistor. A series damping resistor on the last device in the chain should be connected to the TDO pin. The resistor should be physically located as near as practical to the TDO pin.

5.7.4 Undriven Input States. Place a pull-up resistor next to any supply voltage (V_{CC}) between 1.25V and 3.3V, matching the boundary-scan devices in the chain.

5.7.5 Grounding. All grounds should be connected and accessible at the TAP.

5.8 Bypassing Boundary Scan Devices. When necessary to bypass a boundary scan device, use the BYPASS instruction. If not implementing an IEEE 1149.1-compliant architecture, then include additional logic to continue the boundary scan chain.

5.9 Configurable Boundary Scan Devices. A configurable boundary scan device should set boundary scan mode using the TRST or a combination of TCK and TMS signal levels. However, some boundary-scan-enabled devices require additional signals to be set to a defined voltage level in order to be put into boundary scan mode. Other boundary-scan-enabled devices (such as FPGAs) can be configured during power-up and, as a result, behave differently in boundary scan mode.

5.10 IJTAG (compatibility of board test instrumentation). Internal JTAG (IJTAG) specifies the IEEE 1687 standard for interface of embedded instruments (on-chip programmable logic) to the JTAG TAP. The purpose of the IEEE standard is to connect the on-chip instruments and describe a language for communicating with the instruments via IEEE 1149.1 Test Data Registers.

5.11 IEEE 1687 compliance for TAP connection. On-chip instrumentation should conform to IEEE 1687 in order to interface via the JTAG TAP connector.

5.12 Verification. It is recommended that a verification plan be requested by the Government in order to verify boundary scan functions, as per applicable contract requirements. Where practical, the Government should request boundary scan routines in Serial Vector Format (SVF) as deliverables. These boundary scan routines should use the SVF format given in ASSET-SVF-DOC.

6. NOTES

6.1 Intended use. This handbook provides guidance on the acquisition of Boundary Scan, or JTAG, technology as part of a larger acquisition of electronic equipment.

6.2 Subject term (key word) listing.

Avionics
BIT
Built-in Test
I-Level
Joint Test Action Group
JTAG
Maintenance
O-Level
R&M
Reliability & Maintainability
Supportability
Systems Engineering

6.3 Document reference. All references to IEEE 1149.1 refer to the IEEE 1149.1-2013 version.

6.4 Changes from previous issue. Marginal notations are not used in this revision to identify changes with respect to the previous issue due to the extent of the changes.

Custodian:
Navy – AS

Preparing activity:
Navy - AS
Project ATTS-2018-001

NOTE: The activity listed above was interested in this document as of the date of this document. Since organizations and responsibilities can change, you should verify the currency of the information above using the ASSIST Online database at https://assist.dla.mil.