MIL-HDBK-339 (USAF
31 JULY 1984

MILITARY HANDBOOK

CUSTOM LARGE SCALE INTEGRATED CIRCUIT DEVELOPMENT AND ACQUISITION FOR SPACE VEHICLES

FSC 1820

DEPARTMENT OF DEFENSE
Washington, D. C. 20301

MIL-HDBK-339 (USAF)

1. This military handbook is approved for use by all Departments and Agencies of the Department of Defense.

2. Beneficial comments (recommendations, additions, deletions) and any pertinent data which may be of use in improving this document should be addressed to:

Space Division SD/ALM
Air Force Systems Command
P.O. Box 92960
Worldway Postal Center
Los Angeles, CA 90009

by using the self-addressed Standardization Document Improvement Proposal (DD Form 1426) appearing at the end of this document or by letter.

FOREWORD

The acquisition of custom large scale integrated circuits (CLSICs) presents many new and complex technical and management challenges. This handbook is primarily intended to document the design standards and management practices that should be implemented during the acquisition of a high reliability CLSIC for a space system. The requirements are intended to achieve an optimum balance among performance, reliability, and system life cycle cost. The focus is on requirements to assure that the design and manufacturing processes will result in a CLSIC with the desired performance and reliability as contrasted to other possible goals, such as minimizing chip size or chip cost. The requirement are arranged in sections that correspond to the typical sequence in the acquisition process. By the use of "should" instead of "shall," the requirements are intended as guidance rather than contractual compliance. However, adherence to, or deviations from the "should" requirements could be agenda items at appropriate program reviews. The information in this handbook is therefore intended to supplement other contractual requirements for reviews. audits, and for part and material controls. To accommodate direct referencing in contractor detailed specifications for CLSICs, and to assure appropriate compliance, the requirements in the general specification (Appendix C of this handbook) are stated using "shall."

The selection of a CLSIC implementation instead of an implementation using other devices should be based upon a comparison among the alternatives of performance, schedule. system life cycle cost, and risk. This comparison should recognize that with another implementation using mature devices, the reliability and performance margins might be better known due to the maturity of the devices used. Also, an implementation using mature devices might offer other advantages. such as possible alternate suppliers. On the other hand, a CLSIC implementation may offer the possibility for improved performance, much lower power. much less weight, fewer off-chip connections. and lower cost, as compared to other implementations. A CLSIC implementation may also offer the possibility for very high reliability, if it is based on mature design and mature manufacturing concepts. However, the "custom" in CLSIC means that at least some features of a CLSIC may be unique and lack successful usage experience. This lack of maturity is the major problem that may make it difficult, if not impossible, to accurately predict schedules, performance,

(Continued)

FOREWORD (Continued)

performance margins, and reliability for a CLSIC. In addition, the inherent complexity of a CLSIC makes it difficult to measure all critical performance parameter, or to estimate performance margins, even by testing completed devices.

Meeting the high reliability, performance, and radiation hardness requirements for CLSICs used in space systems is dependent both on the maturity of the major design features and the maturity of the manufacturing processes used. In addition, the quality and reliability margins must be assured at every step during design, simulation, fabrication, and assembly by the design analysis, processes, and controls used. Therefore, successful acquisitions of high reliability CLSICs may require different and more stringent actions by all participants at every step in the design and manufacturing processes as compared to the acquisition of other devices. When one performs extensive “front end” audits, design analysis, simulations, documentation, and design reviews, the risks in using CLSICs are expected to be reduced. This handbook is an attempt to document the actions required. Note that although the emphasis in the handbook is on digital devices, the handbook is intended to apply to both digital and linear circuitry of CLSICs.

CONTENTS

CONTENTS (Continued)

CONTENTS (Continued)

CONTENTS (Continued)

CONTENTS (Continued)

CONTENTS (Continued)

CONTENTS (Continued)

CONTENTS (Continued)

CONTENTS (Continued)

CONTENTS (Continued)

CONTENTS (Continued)

Page

APPENDICES

THIS PAGE INTENTIONALLY LEFT BLANK

SECTION 1

SCOPE

1.1 PURPOSE

This handbook presents requirements for the management. design, and manufacturing control of custom monolithic large scale integrated circuits intended for use in high reliability space systems. In addition, this handbook presents the general requirements for the application or use of such devices in high reliability applications such as space systems and launch systems. This handbook is intended to provide the required guidance to ensure coordinated management of the design, development, application, procurement, control, and standardization of Custom Large Scale Integrated Circuits (CLSICs) in order to eliminate any failures of such devices and to reduce any problems in their acquisition.

1.2 APPLICATION

This handbook is basically intended to be listed as a guidance document in space vehicle acquisition contracts. However, the guidance information incorporated in the handbook may be followed as a matter of good management practice, whether contractually suggested or not. Of course, the handbook or some of the requirements in the handbook, could be formally imposed as compliance by appropriate referencing. Even in that case, unless tailoring modifies the compliance required, the use of “should” instead of “shall” in all sections except Appendix C essentially turns the handbook requirements into guidance information only. In any case, the degree of compliance with the “should” requirements might be appropriately scheduled as agenda items at design reviews or technical interchange meetings. Resulting action items, whether in scope or out of scope, would be handled the same as in scope or out of scope action items on any other subject. Nevertheless, the intended degree of compliance with the “should” requirements must be clearly stated in the contract, and not left to be interpreted after contract award.

When the space vehicle contractor procures CLSICs from another organization, the applicable provisions of this handbook should be included in the purchase order or subcontract. Specific CLSIC technical requirements and other design, fabrication, or test provisions which are directly applicable to a particular device are usually determined by the

space vehicle contractor. The device requirements to be formally imposed for compliance by the device supplier would be stated in a detailed technical requirement document prepared by the contractor, such as a detailed specification for the CLSIC. In that case, the general technical requirements stated in Appendix C of the handbook should be imposed by appropriate referencing of Appendix C in the detailed specification for the CLSIC (see Section 10).

When this handbook is applied to CLSICs for use in other high reliability applications such as launch vehicles, or other equipment, the term space vehicle should be interpreted as the applicable vehicle or equipment. When this handbook is applied to the acquisition of custom very large scale integrated circuits (VLSIC), or to other device types, the term CLSIC should be interpreted as the applicable device. For the purposes of this handbook, LSIC, CLSIC, and VLSIC have the same requirements.

SECTION 2

REFERENCED DOCUMENTS

2.1 GOVERNMENT DOCUMENTS

The following documents, of the issue in effect on the date of invitation for bids or request for proposal, form a part of this handbook to the extent specified herein.

SPECIFICATIONS

STANDARDS

DOD-STD-100	Engineering Drawing Practices
MIL-STD-883	Test Methods and Procedures for Microelectronics
FAR 2.000	Federal Acquisition Regulations

Copies of specifications, standards, drawings, and publications required by contractors in connection with specific procurement functions should be obtained from the contracting office or as directed by the contracting officer.

THIS PAGE INTENTIONALLY LEFT BLANK

SECTION 3

DEFINITIONS AND ACRONYMS

3.1 ABSORBED DOSE, TOTAL

The total absorbed dose is the amount of energy deposited per unit mass (Joule/kg) in a given material resulting from exposure to radiation. The unit of absorbed dose is the Gray (Gy). For silicon (Si) material, one Joule/kg would be expressed as 1 Gy(Si). Note that the response of a device to radiation may depend upon the rate of exposure, so the rate is normally specified as well as the total absorbed dose.

3.2 ACCEPTANCE TEST

Acceptance tests are the required formal tests conducted to demonstrate acceptability of an item for delivery. They are intended to demonstrate performance to specification requirements and to act as quality control screens to detect deficiencies of workmanship, material, and quality.

3.3 AGING SENSITIVITY

Aging sensitivity is the variation of the useful life of a device resulting from deterioration mechanisms such as oxidation and wear.

3.4 ATE

ATE is the acronym for automatic test equipment.

3.5 AUTOMATIC TEST EQUIPMENT

Automatic test equipment (ATE) refers to equipment external to a CLSIC device that is capable of automatic generation of test vectors for that device. It may also include features to apply the test vectors to the device under test, monitor and evaluate its test responses, and provide an indication of the operational status that specifies the presence or location of faults.

3.6 BASIC CIRCUIT STRUCTURES

The four basic circuit structures for a CLSIC are busses, random access memories, registers and combinational logic. The simplest cases of a bus, memory, register, and

combinational logic are, respectively, a wire, an addressable storage for one bit, a flip-flop, and a gate.

3.7 BILBO

BILBO is the acronym for built-in logic block observation.

3.8 BUILT-IN TEST

Built-in test (BIT) refers to testing which forms an integral part of the CLSIC design, and serves to make it self-testing to some degree. Built-in self test is achieved by special hardware. firmware, or software, or by some combination of the three.

3.9 BUILT-IN TEST FEATURES

Built-in test features for CLSICs include the built-in test circuitry, other special built-in test structures, and the embedded firmware and software used to implement built-in testing. For example, built-in test features may include functional circuits such as LSSD registers, set/scan registers, BILBO registers, counters, comparators, encoders, and decoders or they may be nonfunctional such as those used for process monitoring or to enable external testing.

3.10 BUILT-IN TEST STRUCTURES

A built-in test structure for a CLSIC is an individual pattern of integrated circuit elements designed to provide information on specific parameters critical to the design, fabrication, or evaluation of the integrated circuit.

3.11 CAPABILITY AUDIT

The capability audit consists of a designer capability audit team reviewing the designer's capabilities and a manufacturer capability audit team reviewing the manufacturer’s capabilities to produce CLSICs. These audit teams review the applicable organizations, program management, design tools, design rules, mask fabrication, wafer fabrication, assembly, screening tests, electrical tests, product evaluation tests, lot conformance tests, facilities, and other related areas.

3.12 CAPABILITY AUDIT TEAM

A capability audit team consists of a team chairman and other designated representative(s) charged with the responsibility of auditing either the designer’s capabilities

or the manufacturer's capabilities, or both, for the purpose of determining the capability of supplying high reliability CLSICs.

3.13 CELL

A cell is an elementary subcircuit that implements the most primitive function of a circuit or subsystem. Much of the overall circuit or subsystem can be synthesized through the replication of such cells, which may or may not be identical to each other. Macro-cells and modules extend the concept to higher levels of design, respectively implementing more complex functions.

3.14 CHIP ARCHITECTURE

Chip architecture consists of the specification of the major functional blocks within an integrated circuit and their interconnection.

3.15 CHIP BEHAVIOR

Chip behavior is the black-box functioning of the chip. The chip behavior consists of descriptions of input-output transformations performed by the chip and the associated timing relations.

3.16 CHIP FLOOR PLAN

A chip floor plan is a schematic showing the placement of various functional blocks within the chip and their sizes. All interconnections need not be shown.

3.17 CIRCUIT

A circuit is a collection of active and passive circuit elements, interconnected by various conductors providing one or more closed paths, which implements a well defined function.

3.18 CLSIC

CLSIC is the acronym for custom large scale integrated circuit (see 3.25).

3.19 COMPONENT

A component is a functional unit that is viewed as an entity for purposes of analysis, manufacturing, maintenance, or record keeping. Examples are individual electronic boxes such as receivers, multiplexer, or transmitters. A computer

program component (CPC) is a functionally or logically distinct part of a computer program configuration item (CPCI) that is distinguished for the purpose of convenience in designing and specifying a complex CPCI as an assembly of subordinate elements.

3.20 CONCEPTUAL DESIGN

A conceptual design for a chip consists of the chip behavior, chip architecture, and the floor plan.

3.21 CONTRACTING OFFICER

The contracting officer is the individual in the procuring office with the authority to enter into and administer contracts and to make determinations and findings with respect thereto, or with any part of such authority. The term also includes the authorized representative of the contracting officer within the limits of his authority. A more detailed definition is given in the Federal Acquisition Regulation, FAR 2.000, for application to government contracts. The reason that the term “contracting officer” is used in this handbook instead of the commonly used term “procuring activity” is that some government documents define “procuring activity” in such a way that it would not be the correct term if this handbook were referenced in a government contract. In the case where a manufacture is furnishing items in accordance with a contractor specification for an item that references this military handbook, the contracting officer is also clearly identified by this definition. In that case, the individual in the contractor organization who entered into the procurement agreement or contract with the manufacturer is the contracting officer.

3.22 CONTRACTOR

In this handbook the term contractor signifies the producer of a space vehicle or a component of a space vehicle. The contractor is the organization that uses the CLSIC, as distinguished from the designer of the CLSIC and the manufacturer of the CLSIC. The CLSIC designer organization and the CLSIC manufacturer may, in fact, be part of the contractor organization; however, either or both may be entirely separate companies. The separate terms are used in this handbook to distinguish or divide the various responsibilities specified among the user, designer, and manufacturer of CLSICs . In this way, the document may be easily tailored for use by either the designer organization or the manufacturer organization. However, this division should not be interpreted as reducing

the obligation of the space vehicle contractor to meet all contractual requirements. Nor should the division be interpreted as encouraging or discouraging the same company, or different companies, to be the designer, Manufacturer, or user.

3.23 CONTROL FLOW

Control flow is the specification of when and under what circumstances each function specified in the data flow is performed and, hence, the parallelism to be implemented in the design. Included in the control flow are precise timing. conditional execution, concurrent operation. state sequencing. and response to error conditions.

3.24 CONTROLLABILITY

Controllability is a measure of the extent to which signals at any node in a circuit may be controlled using externally applied test signals.

3.25 CUSTOM LARGE SCALE INTEGRATED CIRCUIT (CLSIC)

A custom large scale integrated circuit is a nonstandard monolithic large scale integrated circuit (LSIC) which is designed and fabricated for a specific system application.

3.26 DATA FLOW

Data flow is made up of the set of functions to be performed on data, along with a specification of input and output variables. Data flow describes variable interactions and potential parallelisms in the behavioral design. The ordering of operations or functions is done on the basis of data precedence.

3.27 DATA FLOW GRAPH

A data flow graph consists of a set of nodes interconnected with arcs, where each node represents an operation and the arcs represent flow of data between the operation nodes.

3.28 DATA FLOW LANGUAGE

A data flow language expresses data flow in language form and is capable of expressing potential parallelism.

3.29 DESIGN BASELINE

The design baseline for CLSICs is a compilation of design tools and design documentation including design guidelines and design rules.

3.30 DESIGN FOR TESTABILITY

Design for testability is a process, forming an integral part of a design program. which requires a deliberate effort to ensure that the CLSIC being designed is capable of being tested thoroughly. This should be accomplished with minimum effort and cost, and with minimal impact on reliability, resulting in a high testing confidence level.

3.31 DESIGN STYLE

Design style refers to a specific organization or architecture in which a basic CLSIC circuit or structure can be implemented. It is usually a function of technology and circuit layout. Examples of design styles for combinational logic are programmable logic arrays (PLAs), read only memories (ROMs), pass transistor logic, and gate combinational networks.

3.32 DESIGN VALIDATION

Design validation is an informal process whereby certain aspects of the design at a particular level are shown to be equivalent, in either behavior or structure, to one or more corresponding aspects of the design at another level.

3.33 DESIGN VERIFICATION

Design verification is a formal, algorithmic process for proving that two designs exhibit equivalent performance under all specified conditions.

3.34 DESIGNER

The designer is the organization that establishes the design baseline and the electrical, logical, and physical configuration of a CLSIC. The designer organization may be part of the contractor organization which has the CLSIC application or may be part of a different company or organization.

3.35 DYNAMIC MEMORY

Dynamic memory consists of storage circuitry, usually capacitive, which must be recharged or “refreshed” repetitively at frequent intervals to avoid loss of data.

3.36 ELECTRON EXPOSURE

Electron exposure is expressed in numbers of electrons per square centimeter (e/cm^2). Electron exposure causes ionization effects in semiconductors and, when the electron energy is high enough, displacement damage may also be produced. Ionization is specified in terms of the absorbed dose in units of Grays (Si). If the fluence of electrons with energies greater than or equal to 1 MeV is greater than 10^{12} e/cm then an equivalent displacement damage electron fluence should also be specified.

3.37 EMP INDUCED PIN TRANSIENTS

EMP induced pin transients are the voltage or current transients caused by electromagnetic pulse (EMP) fields which may result from detonation of a nuclear weapon. The EMP is specified by either (a) the worst case current or voltage transient waveforms at each external pin or (b) the worst case equivalent single positive or negative open circuit voltage pulse of specified magnitude, width, rise and fall time, and specified source impedance.

3.38 END-OF-LIFE DESIGN LIMIT

The end-of-life design limit is the expected variation in the electrical parameters of a device for which allowance is made in the design of the circuit. The parameter variations are usually expressed as percentage changes from the specified minimum and maximum values.

3.39 ERROR

An error is an incorrect signal value or state that results from the presence of a physical failure mode or logical fault in a device.

3.40 ERROR-DETECTING/ERROR-CORRECTING CODE

An error-detecting/error-correcting code is a method of encoding information, e.g., by appending redundant check bits, so that errors in the encoded information can be automatically detected and corrected by the appropriate checking circuits.

3.41 FAILURE MODE

A failure mode is a characterization of a change or imperfection in the physical structure of a circuit or device, e.g., opens, shorts, or pattern sensitivity which may result in erroneous circuit operation. Failure modes may vary across different integrated circuit technologies.

3.42 FAULT

A fault is a change or imperfection in the logical structure of a device, resulting either from a design error or a physical failure in the device.

3.43 FAULT COVERAGE

Fault coverage is a quantitative measure of a test. It is normally expressed as the percentage of faults within a given fault population that are detectable by means of the employment of that test.

3.44 FAULT DETECTION TEST

A fault detection test consists of test vectors or input stimuli which, when applied to a device under test, produce output response signals from the device that differ according to whether the device is faulty or fault-free.

3.45 FAULT LOCATION TEST

A fault location test consists of test vectors which, when applied to a device under test, serve to identify or locate a faulty element within the device. They do so by producing output signals that vary in a unique manner with the location of the faulty element.

3.46 FAULT DICTIONARY

A fault dictionary is a table or other listing that relates all expected faulty output signatures to a corresponding combination of input stimuli test patterns and internal faults. A fault dictionary is usually based on a particular set of documented fault models.

3.47 FAULT MODEL

A fault model is a mathematical description of a physical failure mode or logical fault that is utilized in the simulation or analysis of the behavior of a circuit under Specified conditions. For example, see “Stuck-At Fault,” 3.112.

3.48 FAULT POPULATION

The fault population for a given device consists of the group of individual faults that correspond to a set of specified failure modes. It is used to provide a basis for the design and evaluation of tests.

3.49 FAULT RESOLUTION

Fault resolution is a quantitative measure of the ability of a test to pin-point the location of faulty elements within a device under test. It thus measures the extent to which faults can be isolated or different faults can be distinguished by the erroneous test responses produced by the fault.

3.50 FAULT SIGNATURE

A fault signature is a set of test responses, often compressed into a compact form, that serves to identify the response from a circuit containing a specific fault to a specific test procedure.

3.51 FAULT SIMULATION

Fault simulation is the process of determining the expected faulty behavior of a device based on specific fault models and a behavioral or structural model of the device. The simulation may be accomplished by means of either a computer program or a hardware implementation. Fault simulation is used in the generation of test vectors for the device and also to measure the effectiveness and fault coverage of those vectors.

3.52 FAULT TOLERANCE

Fault tolerance is the ability of a design to accommodate internal failures and continue to operate correctly. Means of accomplishing this include the employment of circuit redundancy, error detection, and error correction.

3.53 FIRMWARE

Firmware is a computer program or data set which is stored in a form that is unalterable during normal operation. The usual implementation is in some form of read-only memory that is accessed directly by associated circuitry. as opposed to a software program that is stored in some medium which must be entered into the random access memory of the device before it can be used. The stored program may consist of microcode or machine code. The programs are ones and zeros, as stored.

3.54 FORMAL DESCRIPTION

A formal description is an unambiguous description of a digital design, which is machine processable. The syntax (structure) and semantics (meaning) of the elements of the descriptive technique are well defined.

3.55 FORMAL GRAPHICAL DESCRIPTION

A formal graphical description is any formal description which contains graphical elements such as nodes and arcs, for which the semantics and graph structure are well defined; e.g., a Petri Net (see 3.87).

3.56 FREE FIELD RADIATION ENVIRONMENT

The free field radiation environment consists of the radiation fields incident on the system which would exist in the absence of the system.

3.57 FUNCTIONAL TEST

A functional test is a test that is intended to exercise an identifiable function or task of a design or circuit. The function often is tested independently of the physical implementation of the function.

3.58 GRAY (GY)

The Gray is the unit of absorbed radiation dose per unit mass. It equals 1 Joule per kilogram. The abbreviation of Gray is Gy; with reference to absorption in silicon, the abbreviation is Gy (Si). The conversion of rad units to Gy units is 100 rad = 1 Gy.

3.59 HARDNESS ASSURANCE

Hardness assurance consists of the procedure, controls, and tests applied during CLSIC design, fabrication, and procurement to ensure that the CLSIC has a response to natural radiation and nuclear-induced stresses that is within known and acceptable limits. The procedures may include, but are not limited to, electrical screening, radiation screening, and lot conformance testing in a radiation environment.

3.60 HARDNESS ASSURANCE DESIGN DOCUMENTATION

The hardness assurance design documentation details the hardness assurance activities relative to the CLSIC. This includes, but is not limited to, the design, fabrication. radiation response data, analyses, and acceptance criteria for the CLSIC.

3.61 HARDNESS NONCRITICAL PARTS

Hardness noncritical parts are devices that have such a high radiation design margin, typically 100 or higher, that

they require no radiation lot conformance testing for that radiation environment.

3.62 HARDWARE DESCRIPTIVE LANGUAGE (HDL)

A hardware descriptive language (HDL) is a language which formally describes the behavior or structure of a digital design.

3.63 HAZARD

A circuit contains a hazard if errors can be caused by certain permissible combinations of input sequences and stray delays. A hazard represents a malfunction possibility that reduces a circuit's reliability.

3.64 INITIALIZATION

Initialization is the process of applying an input pattern or sequence of input patterns to a device under test to place that device in a known initial state before actual testing commences.

3.65 INTEGRATED CIRCUIT

An integrated circuit is a combination of interconnected circuit elements or cells inseparably associated on or within a continuous, monolithic substrate. Thus , it is an inseparable single entity containing substrate, circuit elements, and interconnection pattern.

3.66 INTERFACE BEHAVIOR

Interface behavior is the way in which a CLSIC interacts with circuitry external to itself. Interface behavior parameters include the applied voltages and the ordering and relative timing of the reading and writing of external variables.

3.67 KERNEL

The kernel is the circuitry intrinsic to the functional nature of the CLSIC which is tested. It may be tested by built-in testing circuitry in a built-in self-test testing strategy, or by external test equipment. A CLSIC may contain several kernels, each of which is considered individually for testing purposes.

3.68 LARGE SCALE INTEGRATED CIRCUIT (LSIC)

An LSIC is an integrated circuit which normally contains between 100 and 10,000 logic gates or the equivalent 300 to 30,000 transistors.

3.69 LOGIC DESIGN

A logic design is a digital design consisting of a set of elements and their interconnection. Element types include logic gates, flip-flops, latches, and transistors used as switches. (Transistors, such as pull-ups, which have no specified logic function, are seldom included in logic designs.)

3.70 LOT (PRODUCTION LOT, ASSEMBLY LOT, AND INSPECTION LOT)

A production lot consists of all CLSICs that are manufactured during the same time period on the same production line(s) by means of the same production techniques, materials. controls, facilities, and design. The production lot as used in this handbook would also be the assembly lot and the inspection lot as defined in other documents.

3.71 LSIC

LSIC is the acronym for large scale integrated circuit.

3.72 LSSD

LSSD is the acronym for level sensitive scan design.

3.73 MANUFACTURER

The manufacturer is the organization that is the fabricator and supplier of the CLSIC. The manufacturer organization may be part of the contractor organization which has the CLSIC application, it may be the designer of the CLSIC. or it may be part of a different company or organization.

3.74 MANUFACTURER SURVEILLANCE

Manufacturer surveillance consists of monitoring by the contractor, or the contractor’s designated representative. of the manufacturer’s fabrication, inspection, and test facilities, equipment, processes, procedures, and controls based on preestablished criteria. Manufacturer surveillance includes Contractor Source Inspection.

3.75 MANUFACTURING BASELINE

The manufacturing baseline for CLSICs is a description of the sequences of manufacturing operations necessary to produce CLSICs (normally in the form of a flow chart or lot travelers). All documents pertaining to the procurement and inspection of materials, production processes, production environments, and production controls are identified. Documents are identified by name, number, and current approved revision. The flow chart reflects the complete manufacturing processes used for the CLSIC and shows all manufacturing, inspection, testing, quality verification points, and the points where all materials or subassemblies enter the flow. The manufacturer usually documents the baseline using a controlled access file or books which contain all referenced documents noted on the flow chart, including in-house documents referenced.

3.76 MICROCODE OR MICROINSTRUCTION

A microcode or microinstruction consists of a simple, elementary machine language subinstruction which forms a single control word in a microprogram: the level of programming at which every part of an integrated circuit may be controlled explicitly.

3.77 MICROPROGRAM

A microprogram is a subroutine, used to execute an assembly language macroinstruction (from program memory), which consists of a sequence of microinstruction resident in firmware. A control unit whose control variables are stored in a memory is called a microprogrammed control unit. In general, for a microprogrammed device, every machine code or assembly level instruction is implemented by a microprogram consisting of microcode instruction.

3.78 MISSION-CRITICAL FAILURE

A mission-critical failure is a physical failure in a device whose undetected occurrence may result in overall failure of the mission or main application for which the device is designed.

3.79 MUX (DEMUX)

MUX is the acronym for multiplexer, and DEMUX is the acronym for demultiplexer.

3.80 NEUTRON EXPOSURE

Neutron exposure occurs when a device is exposed to energetic neutrons. Neutron exposure is specified by the equivalent fluence for displacement damage in neutrons per square centimeter, n/cm^2. If the integrated fluence is greater than 10^{12} n/cm^2 (1 MeV Si equivalent), the time dependence of the neutron exposure is normally specified.

3.81 OBSERVABILITY

Observability is a measure of the degree of ease or difficulty involved in deducing the status of internal nodes of a device under test by examination of the test responses.

3.82 PARAMETER DESIGN MARGIN

The parameter design margin is the ratio of the end point electrical parameter failure limit for a test sample to the device parameter mean value degradation at the specified radiation level. For a log normal distribution, the geometric mean is used.

3.83 PARAMETER FAILURE VALUE

Parameter failure value is a specified parameter value at which the device is considered to fail.

3.84 PARTITION

A partition is the subdivision of a circuit into one or more not necessarily disjoint subcircuits.

3.85 PARTS, MATERIALS, AND PROCESSES CONTROL BOARD (PMPCB)

The PMPCB is an organization established by contract to assist the prime contractor in managing and controlling the selection and documentation of parts, materials, and processes. In this handbook, it is assumed that the PMPCB has a member who is the authorized representative of the contracting officer, with the right of veto.

3.86 PARTS, MATERIALS, AND PROCESSES SELECTION LIST

The parts, materials, and processes selection list is a list of all parts, materials, and processes approved for use in a specific system or equipment. It is composed of standard and nonstandard items which have been approved by the PMPCB.

3.87 PETRI NET

A Petri Net is a formal graphic description of a digital design (see 3.55). Petri Nets usually are used to express control flow. They allow expression of asynchrony, potential parallelism, and conditional execution of actions.

3.88 PLA

PLA is the acronym for programmable logic array.

3.89 PMPCB

PMPCB is the acronym for the parts, materials, and processes control board (3.85).

3.90 PROCESS VALIDATION WAFER

A process validation wafer is composed entirely of test chips that are used to determine intrawafer variations. It provides data for the evaluation of processing equipment and is used as a means of process characterization. It may also be used to determine radiation response characteristics of the process.

3.91 RACE CONDITION

A race condition is present in a circuit if the behavior of a state transition depends on the order in which two or more state variables change value. This is determined by permissible combinations of input signal transition times and stray delays. If an erroneous final state is possible, the circuit is said to contain a critical race condition.

3.92 RADIATION CHARACTERIZATION

Radiation characterization consists of representative measurements of the response of critical electrical parameters as a function of radiation environment(s) under specified test conditions.

3.93 RADIATION DESIGN MARGIN

The radiation design margin is the ratio of the mean radiation failure value for a test sample to the device radiation specification level. For a log normal distribution. the geometric mean is used.

3.94 RADIATION-TO-FAILURE METHOD

The radiation-to-failure method consists of stressing the device under test to increasing levels of ionizing radiation until the parameter failure value has been reached.

3.95 RADIATION FAILURE VALUE

The radiation failure value is the lowest radiation test value at which a device fails to meet a specified criterion.

3.96 RADIATION TEST FACILITY

The radiation test facility is a facility used as a source of energetic particles or electromagnetic ionizing radiation for the purpose of simulating the radiation environments from space or nuclear weapons. Such facilities include, but are not limited to, electron and heavy particle accelerators, flash X-ray machines, Co^{60} irradiation cells, and nuclear reactors.

3.97 RAM

RAM is the acronym for random access memory.

3.98 REDUNDANT SUBCIRCUIT

A redundant subcircuit is a part of a circuit whose removal does not alter the functional behavior of the circuit. Redundant subcircuits are used to enhance a circuit's fault tolerance; they may contain undetectable faults.

3.99 REGISTER-TRANSFER DESIGN

A register-transfer design is the design of an item which involves elements at the register level. These can be classified into combinational and sequential circuits, where registers form the main sequential elements which transfer or operate on data words.

3.100 RELIABILITY

The reliability of a circuit or device is the probability that it can survive, i.e., continue to function correctly, for a specified period of time.

3.101 ROM

ROM is the acronym for read only memory.

3.102 SCAN-IN/SCAN-OUT DESIGN

Scan-in/scan-out refers to a class of design which is characterized by the fact that the memory elements can be reconfigured to form a Shift register during testing. This design-for-testability concept includes methods such as level sensitive scan design and scan path testable design. The state of the circuit can be directly controlled by shifting test data in (the scan-in step), and observed by shifting test data out (the scan-out step) of this shift register.

3.103 SELF-CHECKING CIRCUIT

A self-checking circuit is one that automatically tests itself while operating on-line and signals the presence of internal errors in the circuit. Self-checking circuits typically incorporate error-detecting and error-correcting codes.

3.104 SELF TEST

Self test is a test, or series of tests, performed by a device upon itself usually while operating off-line. This shows whether or not it is operating within specified (or designed) limits. Included are test programs to check out performance status and readiness.

3.105 SINGLE PARTICLE EXPOSURE

Exposure to single energetic ionizing particles may produce upsets in CLSIC devices. Single particle exposure can be specified in terms of a flux of particles whose distribution in mass, energy, and angle with respect to the top surface of the microcircuit is specified. The worst case exposure depends on the radiation environment in which the system operates.

3.106 SOURCE CONTROL DRAWING

A source control drawing is a drawing usually prepared in accordance with DOD-STD-100 by the contractor for use in procurements of specific parts from specific manufacturers. A source control drawing for a CLSIC contains, by reference, all of the detailed requirements and other technical provisions which are needed for the procurement. In this handbook, the term “detailed specification” is interpreted to include a source control drawing.

3.107 SPECIFICATION CONTROL DRAWING

A specification control drawing is a drawing usually prepared in accordance with DOD-STD-100 by the contractor for use in procurements of specific manufacturer parts with added controls. A specification control drawing for a CLSIC contains, by reference, all of the detailed requirements and other technical provisions which are needed for the procurement. In this handbook, the term "detailed specification" is interpreted to include a specification control drawing.

3.108 SPECIFIED RADIATION ENVIRONMENTS

The specified radiation environments are the worst case environments that the CLSIC is predicted to encounter in its system application. They are derived from the free field environment specified for the system and are defined in terms of electron, X-ray, gamma ray, neutron, proton, EMP, and heavy ion exposure.

3.109 STATE

State is a concept associated with a digital system and is determined by the values associated with certain variables (inputs, outputs, internal elements, or devices) in the system. Often the state of a circuit is specified by the logic values stored in the storage devices of the circuit.

3.110 STATIC (MEMORY)

A static memory consists of storage circuitry which retains the data without refreshing as long as the power is applied, unless it is altered externally.

3.111 STRUCTURE

A structure is the interconnection of one or more basic structures, i.e., an interconnection of busses, random access memories, registers, and combinational logic.

3.112 STUCK-AT FAULT

Stuck-at fault refers to a fault model that allows any one node in a circuit to permanently be held at the logical 1 level (stuck-at-1) or the logical 0 level (stuck-at-0).

3.113 SYMBOLIC SIMULATION

Symbolic simulation is simulation of a design with the inputs represented by symbols (variables) so that the output of the simulator is an expression of each output of the design as a function of the input symbols. The function is closed over the set of valid symbols.

3.114 TEST ANALYSIS

Test analysis consists of the examination and interpretation of the responses to test stimuli (test response) of a device under test, in order to determine the operational condition of the device or to determine the cause or location of a failure.

3.115 TEST CHIP

A test chip is a chip consisting of an assemblage of test structures, each designed to measure one or more parameters resulting from the fabrication process. It is usually substituted for the production circuit at one or more selected sites on the production wafer. It may also be used as a process monitor of dynamic device performance or radiation hardness.

3.116 TEST GENERATION

Test generation is the process of determining test patterns, test sequences, and the corresponding test responses necessary to detect and locate a specified set of faults in a specified circuit or device. Test generation may be performed manually, by computer programs, or by automatic test equipment.

3.117 TEST PATTERN

A test pattern is a set of input signal values that are applied to a device at any one time. A test pattern is the same as a test vector (see 3.127).

3.118 TEST POINT

A test point is an input or output terminal (e.g., a pad or pin of an integrated circuit) and the associated circuitry that are added to a circuit to increase the controllability Or observability of the circuit during testing.

3.119 TEST PROCEDURE

The test procedure is a step-by-step description of the detailed operations required to test a specific unit with a specific test system.

3.120 TEST REQUIREMENT ANALYSIS

A test requirement analysis consists of the examination of documents such as schematics, assembly drawings, and specifications for the purpose of deriving test requirements for a device.

3.121 TEST REQUIREMENT DOCUMENT

A test requirement document is the document that specifies the tests and test conditions required to detect and locate faults in a device.

3.122 TEST RESPONSE

A test response is the set of output signal values that are produced by a device under test when a sequence of test patterns is applied to it.

3.123 TEST SEQUENCE

A test sequence is a set of related test patterns in a specific order for application to a device under test during a particular phase of testing.

3.124 TEST STRATEGY

Test strategy refers to the testing-related aspects of a design, which include the following: (a) the use of test equipment external to the CLSIC chip, accessing the CLSIC through pins or probe pads; (b) the use of built-in test (BIT) schemes, where testing circuitry is included on the chip itself: and (c) the generation of test vectors, patterns, and sequences related to both items (a) and (b) (e.g., employment of the D-algorithm or other means of test generation).

3.125 TEST STRUCTURE (see 3.10)

3.126 TEST VALIDATION

Test validation consists of establishing the validity of the testing software prepared for a specific device by obtaining a quantitative measure of the fault coverage provided by such software by means of either software or hardware simulation techniques.

3.127 TEST VECTOR

A test vector is a set of signal values associated with a device under test. The input vectors are those sets of values that are applied (individually) to the device during testing. The output vectors are the corresponding sets of values that are expected from the device as a result of the input vectors. Sets of output values which deviate from the expected output vectors are indicative of the existence of logical faults. The test vector is the preferred terminology for, but has the same meaning as, the test pattern (see 3.117).

3.128 TEST VERIFICATION

Test verification is that process, related to test generation, by which the correctness of the testing software is verified by running it on the automatic test equipment together with the device under test, or a surrogate such as a hardware fault simulator. The process includes the identification of run-time errors, procedure errors, and other noncompiler errors not uncovered by pure software methods.

3.129 TESTABILITY

Testability is an attribute of the design of a circuit that allows its status (e.g., operable, inoperable, or degraded) to be confidently determined in a timely manner by testing the circuit. Testability may be measured quantitatively by the testing confidence level (see 3.132).

3.130 TESTABLE DESIGN METHODOLOGY

A testable design methodology consists of a kernel circuit structure and a test strategy. That portion of a testable design methodology which deals only with the hardware on the chip itself constitutes a testable structural style.

3.131 TESTABLE STRUCTURAL STYLE

A testable structural style is an architecture or hardware organization consisting of a circuit structure to be tested (kernel) and associated structures that include built-in test circuitry. Example architectures are LSSDs, BILBO designs, and syndrome testable designs. A good testable structural style is an appropriate matching between the kernel, which often is a basic circuit structure having a well-defined design style. and the built-in test features employed.

3.132 TESTING CONFIDENCE LEVEL (TCL)

Testing confidence level (TCL) is a measure of the effectiveness of a set of test patterns. The testing confidence level is usually specified as a percentage of the possible single stuck-at (1 or 0) faults identified as detected by a fault simulator after simulation of the test. These percentages can vary due to necessary modeling work-arounds, fault collapsing. or other factors.

3.133 TESTING SOFTWARE

Testing software consists of the total set of instruction sequences utilized with automatic test equipment to control the input test patterns, test sequences, and measurement parameters used in the testing of a device.

3.134 TOTAL DOSE (See 3.1)

3.135 VARIABLE SAMPLING TEST METHOD

The variable sampling test method is a test method based on a statistical analysis of either: (a) the measured values of the critical electrical parameters after irradiation or (b) the measured radiation to failure values.

3.136 VERY LARGE SCALE INTEGRATED CIRCUIT(S)

A very large scale integrated circuit (VLSIC) is similar to a large scale integrated circuit, but a VLSIC contains 10,000 to 100,000 logic gates (or an equivalent 30,000 to 500,000 transistors).

3.137 WAFER LOT

A wafer lot consists of CLSIC wafers processed in a manner that requires every wafer to be subjected to each batch process step as a group.

3.138 X-RAY, GAMMA RAY EXPOSURES

X-ray and gamma ray exposures are specified by the dose rate and integral absorbed dose in the bulk semiconductor. For silicon CLSICs, the dose rate is specified by Gy(Si)/sec and the absorbed dose by Gy(Si).

SECTION 4

GENERAL REQUIREMENTS

401 JUSTIFICATION FOR USE OF CLSICs

Standard devices should be used by the contractor if system requirements can be effectively met by their use. Otherwise, CLSICs or other nonstandard devices must be used. The use of CLSICs rather than standard devices or some other type of nonstandard devices should be justified by the contractor by tradeoff analysis. The analysis should include, but not be limited to, consideration of the following issues:

a. Availability of standard devices or other types of nonstandard devices which satisfy system requirements

b. Potential advantages of using CLSICs (comparisons of performance, power, weight, cost, off-chip interconnections, and reliability)

c. Demonstrated performance, reliability, capability, and relevant experience of the proposed CLSIC designer and manufacturer

d. Potential risks regarding schedule, cost, radiation hardness, and reliability

e. Long term availability of the CLSIC and potential future supply problems as compared to other implementations

Prior to proceeding with a formal CLSIC acquisition, the justification for the selection of a CLSIC should be presented to the contracting officer or his designated representative on the Parts, Materials, and Processes Control Board (PMPCB) for concurrence.

4.2 APPLICATION

The contractor policy regarding the application requirements of CLSICS should be documented. This policy should encompass application conditions of the CLSICs as they affect sensitive parameters and maximum rating variations expected over the mission life. CLSIC qualification time should be included in the application considerations. The application policy should also include derating due to radiation effects, if applicable.

4.2.1 Compliance with System Requirements. The requirements of this handbook for CLSIC program control and procurement do not relieve the contractor of the responsibility for complying with all the system performance and reliability requirements as set forth in applicable system specifications and contracts. The radiation environment should include all natural environments and nuclear threat environments, as applicable. The government contracting officer is responsible for specifying the free field nuclear threat radiation environment to which the space vehicle may be subjected during the course of a mission.

4.2.2 CLSIC Selection. The contractor should select the technology. design methodology, and production capability for each CLSIC in accordance with system requirements and the criteria specified in this handbook. The selection should maximize the use of standard technology and minimize the variety of different technologies used to satisfy program design and performance requirements. Prior to the final selection of a technology and production capability, a radiation hardness feasibility study should be performed to assure that the planned CLSIC can satisfy the radiation hardness requirement.

4.3 CLSIC PROGRAM PLAN

The contractor, in conjunction with the CLSIC designer and CLSIC manufacturer, should develop a CLSIC program plan which outlines the function and procedures to be followed to ensure the acquisition of satisfactory CLSICs. The program plan should identify the various responsibilities and authorities as well as the methods to be used for integration, coordination and approval of engineering, CLSIC design, design validation, reliability analysis, hardness assurance, producibility, test methods, process controls, and product assurance efforts. Methods for integration and coordination of subcontractor effort, methods for tracking program performance, plans and schedules for CLSIC program reviews, and status reviews with the contracting officer should be included. The CLSIC program plan is intended as a management information document to help all participants understand their roles and responsibilities in relation to the entire effort. The contract (CDRL) should require that the preliminary CLSIC program plan be prepared and submitted to the contracting officer 30 days after contract award for review and approval. The contract (CDRL) should require that the final CLSIC program plan be available for review 30 days prior to the preliminary design review for the component requiring the use of the CLSIC. The plan is not intended as a compliance document unless so referenced in the contract.

4.3.1 Testability Assurance Program. The contractor should devise and implement a Comprehensive program to satisfy the requirements for testability of the CLSIC. This testability assurance program should be included in the program plan. A testability assurance program should form an integral part of the design effort at all levels.

4.3.1.1 Testability Requirements. The contractor should prepare testing and testability requirements for the CLSIC design to be carried out in each phase of the acquisition. The requirements should be based upon the specifications set forth by the contract consistent with the requirements for functionality and reliability (see Appendix B). Testability features of the CLSIC design should include consideration of hardness assurance. The testability requirements include the measures used for each fault type.

4.3.1.1.1 Fault Types. The contractor should define the fault types (e.g., stuck-at faults, bridging faults, delay faults, or other types) to be considered, including their occurrence probability and characteristics (e.g., permanent or intermittent) on which the testing strategy and testability measures should be based (see 3.1 in Appendix B). Special attention should be paid to any mission-critical failures that can be identified.

4.3.1.1.2 Testability Measures. The two primary measures used to gauge the testability of the CLSIC design and the effectiveness of its testing procedures, fault coverage, and fault resolution should be determined (see 3.2 in Appendix B). Other measures may be useful in making design choices in specific cases. The total set of possible measures includes the following:

a. The fault coverage for each specified fault type. that is, the percentage of possible faults that are detectable. The average fault coverage for all specified fault types, which is termed the testing confidence level, should serve as a single measure of overall testability.

b. The resolution to which faults can be physically located on the chip via analysis of the test data. This fault resolution can be measured in terms of transistors.

c. The hardware circuit overhead of the design measured by the percentage of hardware elements (e.g., transistors or logic gates) that are included in the design exclusively to enhance its testability.

d. The chip area overhead measured by the percentage increase in the area of the CLSIC due to its testability features.

e. Where applicable, the software and firmware overhead measured by the percentage of software and firmware instructions and microinstruction that are included in the design exclusively to enhance its testability.

f. The operating performance overhead of the design measured by the percentage change, if any, in such functional performance parameters as maximum clock frequency or maximum duty cycle, due to the testability features of the design.

g. The reliability overhead measured by the change. if any, in the reliability of the CLSIC due to the testability features of the design.

h. Where applicable, the testing speedup, measured by the percentage decrease in testing time due to the testability features of the design, compared to the time required to achieve the same level of fault coverage for a functionally equivalent design without those features.

4.3.1.2 Testability Synthesis. The contractor should carry out a detailed analysis of the anticipated failure modes. and develop the necessary testing strategies and design techniques to meet the testability requirements (see 3.3 in Appendix B).

4.3.1.2.1 Fault Characterization. The contractor should characterize the anticipated failure modes for the CLSIC design (see 3.3.1 in Appendix B). This characterization should take into account the following topics:

a. The circuit technology and fabrication techniques to be employed

b. Detrimental environmental effects in the intended application including radiation. thermal and mechanical stress, and power supply fluctuations

4.3.1.2.2 Testing Techniques and Strategy. The contractor should develop the necessary strategy to meet the testing and testability requirements of the CLSIC design. This strategy should include such techniques as may be required for functional validation and device acceptance as well as

self-check and self-test capabilities required by reliability considerations. The tests to be performed for each designated failure mode should be specified. Test patterns may be generated by means external to the chip, or they may be generated on the chip itself by means of built-in test features (see 3.3.2 in Appendix B).

4.3.1.2.3 Intermittent Failure Detection. To the extent practicable, the CLSIC and associated software should be designed 60 that a predictable built-in test response results from intermittent failures (see 3.3.3 in Appendix B). Detection of a failure by built-in test features should be followed by a second test of the indicated failing operation whenever practical. The optimum number of repeated tests and repeated failure indications necessary to establish a solid failure condition should be determined.

4.3.1.3 Testability Evaluation. A methodology should be established to assess the effectiveness of such testability features as are incorporated in the design (see 3.3.4 in Appendix B).

4.3.2 Product Assurance Program. The contractor and the CLSIC manufacturer should establish, implement, and maintain a product assurance program. The product assurance program should assure compliance with the required quality, material control, reliability, and performance of the CLSIC including the requirement of this handbook, the requirements of the detailed specification, and the requirements of the contract. The product assurance program should be documented in the CLSIC program plan and should detail:

a. Requirement to be imposed during design, processing, manufacturing, and testing

b. Records to be maintained

All design, construction, and workmanship, including rework permitted on CLSICs, should be accomplished in accordance with documented procedures and safeguards. These procedures should be available for review.

4.3.2.1 Contractor Product Assurance Program.

4.3.2.1.1 Manufacturer Product Assurance Plan. The contractor should ensure that the manufacturer has a product assurance plan which meets the requirements of the CLSIC and this handbook.

4.3.2.1.2 Destructive Physical Analysis. A destructive physical analysis, on a sample basis, should be performed on each lot of CLSICs.

4.3.2.1.2.1 Destructive Physical Analysis Management. The contractor should identify the facilities to be used for destructive physical analysis, and document the destructive physical analysis methods and procedures to be used for inspecting the internal materials, design, construction, and workmanship of the CLSICs. These procedures should define the lot acceptance and reject criteria and should identify any approvals required to initiate other special destructive physical analyses. The facilities and procedures should be reviewed and approved by the contracting officer or the PMPCB prior to performing any contractually required destructive physical analyses. The destructive physical analyses may be performed by the contractor, by the manufacturer of the CLSIC, by an independent laboratory, or by a combination of organizations, as long as there is prior approval of the facilities and procedures by the contracting officer or the PMPCB.

4.3.2.1.2.2 Destructive Physical Analysis Policy. Procedures, and Reports. A standardized destructive physical analysis policy, procedure, and summary report format should be established and used by all participants. The contractor's destructive physical analysis findings should be reviewed by the PMPCB on a regular basis.

4.3.2.1.3 Configuration Control. The contractor should institute a continuous in-house assessment of the physical characteristics of the CLSIC. This configuration analysis program should include tasks that develop the following four interrelated data forms:

a. Documentation and controls used in the design of the CLSICS

b. A configuration drawing or sketch which geometrically delineates a pictorial view

c. Correlation of destructive physical analysis results with a. and b., above

d. A manufacturing baseline which contains a process flow chart that accurately defines the sequence of operations and the degree of monitoring (including inspection points and procedures) of each operation, and that indicates which operations are critical (i.e., may inadvertently cause a degradation of radiation hardness or reliability). The manufacturing baseline should include applicable physical dimensions and tolerances such as junction depths, dielectric and conductor thicknesses, and critical lateral spacing.

4.3.2.1.4 Source Surveillance. The contractor is responsible for reviewing all design documentation, product assurance programs, test procedures, and manufacturing processes prior to the production of devices. After production has been initiated, the contractor should perform independent surveillance and monitoring functions related to fabrication, inspection, and testing of devices. The contractor is also responsible for authorizing shipment of CLSICs from the manufacturer. After receipt of CLSICs, the contractor should perform any incoming inspections and tests that might be required to verify their integrity.

4.4 ROLE OF PARTS, MATERIALS, AND PROCESSES CONTROL BOARD

An authorized representative of the contracting officer for parts, materials, and processes is usually the voting member of the PMPCB. In that case, the PMPCB approves the selection and usage of CLSICs and monitors the CLSIC program throughout development, design, procurement, and test. The contractor supports the PMPCB and designates a member whose responsibility is to ensure that hardness is achieved during design and production by requiring appropriate configuration controls and processing procedures. Areas which should be addressed by the PMPCB with respect to hardness assurance are circuit design and layout, processing, testability, assembly, packaging, and handling.

4.5 PROGRAM AND DESIGN REVIEWS

The contractor should periodically conduct program reviews or technical reviews to examine CLSIC design methodology, technology selections, CLSIC design, development, technical progress, manufacturing, testing, and compliance with system or program requirements. The contractor should state in the CLSIC program plan whether these reviews are intended to be part of other contractually required reviews or whether they are separately conducted reviews. The contractor should conduct preliminary design reviews and critical design reviews on the CLSICs. The physical structures, electrical (functional) and logic design, design verification, testability, radiation hardening, and test coverage should be reviewed. Participants would usually include appropriate engineering, manufacturing, product assurance, hardness assurance, and testing experts.

4.6 DETAILED SPECIFICATION

The contractor should develop a detailed technical requirement document for each CLSIC. It should completely define the design methodology and technology selection, geometrical configuration, performance requirements, radiation

hardness requirements, electrical parameters, screening, and lot conformance testing Requirements (see Section 10). The term "detailed specification" is used in this handbook to refer to this detailed technical requirement document, regardless of whether it is prepared as a detailed specification, a specification control drawing, or a source control drawing. The preliminary detailed specification requires review at the component preliminary design review, and the final detailed specification is reviewed at the component critical design review.

4.7 CAPABILITY AUDIT

A capability audit should be conducted by a capability audit team prior to design and prior to fabrication of CLSICs. The capability audit team should review the designer's capabilities to design CLSICs and the manufacturer's capabilities to produce CLSICs in accordance with the requirements of this handbook and should issue a report of its findings and recommendations. Required corrective actions should be included in the audit report. The contracting officer should notify the contractor, CLSIC designer, and manufacturer in writing regarding approval of the capability audit within 30 calendar days of completion of the audit or correction of discrepant conditions.

4.7.1 Designer Capability Audit. A capability audit team would visit the designer's facilities and assess the designer's capabilities to comply with the requirements of the detailed specification or contract.

4.7.2 Design Baseline. Subsequent to the designer capability audit, the design baseline should be maintained current and the resulting documentation should be maintained under configuration control following approval of the capability audit.

4.7.3 Manufacturer Capability Audit. A capability audit team would visit the manufacturer's facilities and assess the manufacturer's capabilities to comply with the manufacturing and test requirements of the detailed specification 01 contract. The manufacturing and assembly baselines for the applicable technology, in effect at the time of the audit, should be provided to the capability audit team. Subsequent major changes in a baseline should be submitted to the contracting officer for approval.

4.7.4 Manufacturing Baseline. Subsequent to the manufacturer capability audit, the manufacturing baseline should be maintained current, and the resulting documentation

should be maintained under configuration control following approval of the capability audit.

4.8 HARDENING AND HARDNESS ASSURANCE PROGRAM

The contractor should implement a program pertaining to hardening and hardness assurance, as applicable, for the design, development, construction, and testing of CLSICs. The contractor should arrive at a baseline part that has the required hardness, and then develop and document a hardness assurance program for the CLSIC which details the hardness assurance tasks and responsibilities to assure that the baseline hardness is achieved and maintained. This program should be reviewed at the component preliminary design review. The hardness assurance tasks include, but are not limited to, the following:

a. Formation of a hardness assurance organization

b. Development of a hardness assurance program plan

c. Development of hardness assurance design documentation

d. Representation of hardness assurance issues at the preliminary and critical design reviews (PDR and CDR)

e. Representation to the PMPCB and capability audits

f. Development of hardness assurance requirements for the detailed specification

4.8.1 Hardness Assurance Organization. The contractor should identify their organizational group or groups that have responsibilities to implement, control, and coordinate hardness assurance activities associated with CLSICs. This includes the organizational interface with management on hardness assurance issues and the review of assigned responsibilities to assure that all aspects of the hardness assurance program are carried out. The managers with responsibility for hardness assurance issues should be identified.

4.8.2 Hardness Assurance Program Plan. The contractor should develop and document a hardness assurance program plan for CLSICs which details the hardness assurance tasks and identifies responsibilities for assuring that the tasks are carried out. This hardness assurance program plan should be

incorporated as part of the overall program plan for CLSICs, and should address the following items:

a. Description of the hardness assurance organization with designated responsibilities

b. Responsibilities of representatives to preliminary design reviews, critical design reviews, the PMPCB, and capability audits

c. Definition of the system radiation environments

d. Specification of worst case CLSIC radiation environment(s)

e. Definition of failure in each radiation environment

f. Specification of end point electrical parameters, tolerances, and recovery tine following a nuclear event and parameter values at the end of mission

g. Maintenance of a radiation characterization data base for use in feasibility analyses

h. A feasibility analysis which demonstrates that the proposed design and technology are adequate for the radiation requirements

i. Identification of hardness assurance critical factors in design, layout, processing, assembly, and handling

j. Identification of hardness assurance testability requirements and test chips

k. A verification analysis and test

l. Device categorization in each environment

m. Preparation of the radiation test requirements for the detailed specification

n. Development of hardness assurance design documentation

4.8.3 Hardness Assurance Design Documentation . The contractor should prepare a Hardness Assurance Design Document which details all radiation response data, analyses, and

requirements for the CLSIC. The designer should provide the contractor with the data needed to establish this document. This documentation should include but not be limited to:

a. Circuit schematic, functional description, pin out, operating conditions, and application

b. Specification of worst case radiation environment for each application of CLSICs

c. Definition of functional failure and maximum allowed degradation of all critical parameters for each radiation environment

d. Radiation characterization data base for each circuit

e. Results of feasibility study for each circuit

f. Results of verification analysis and tests

g. Testability requirement and description of hardness assurance test chips

h. List of critical design and processing parameters in each radiation environment

i. Categorization of CLSICs in each radiation environment

j. Lot acceptance criteria and test results

k. Any hardness-dedicated features of the design

4.8.4 Preliminary and Critical Design Reviews(PDR & CDR). The contractor should have a hardness assurance representative present at the preliminary and critical design reviews. The contractor should ensure that all system design decisions that affect hardness assurance of CLSICs are made with the concurrence of the hardness assurance representative. In addition, the representative should ensure that the hardness assurance program plan, the hardness assurance design documentation, and the detailed specification are appropriately modified, if necessary, to incorporate any hardness assurance critical decisions made at the preliminary and critical design reviews.

4.8.5 Capability Audits. The hardness assurance Organization should assure that hardness assurance issues are considered in the designer and manufacturer capability audits.

The hardness assurance program manager should assign a member of his organization to the audit team or coordinate with the audit team chairman to assure that hardness assurance issues are given consideration during the audit.

4.8.6 Detailed Specification. The detailed specification for a specific CLSIC should state the applicable radiation hardness requirements for design, layout, processes, assembly, packaging, handling, test chips, testable networks, special probe and bond pads, electrical and radiation preliminary screens, radiation lot sample tests in each environment (for which the part is category 1), sample sizes (per wafer when specified), test methods, confidence and probability of survival requirement, radiation specification levels, part failure criteria, radiation test procedures, radiation test facilities and dosimetry, data analysis, failure analysis and lot acceptance criteria, and radiation 100 percent screens (if any).

4.8.7 Manufacturer Requirements for Hardness Assurance Design Documentation. The contractor is responsible for the hardness assurance design documentation which summarizes all radiation hardness manufacturing activities and test results and that serves as the basis for the radiation testing requirements specified in the detailed specification. The manufacturer should prepare and make available to the contractor documents which identify the elements in the design and construction of CLSIC that are critical to hardness assurance. Examples are: critical design and processing parameters for each radiation environment; radiation characterization data on test devices, test elements, subcircuits, or library cells processed with the same processing technology used for the CLSICs; hardness verification analysis and tests; and all radiation characterization tests on actual CLSICs fabricated with the process technology used for the custom circuits.

4.8.8 Radiation Testing. The radiation test methods should be in accordance with the detailed specification. The lot conformance tests, sample plan, and acceptance criteria should be as specified in the detailed specification. When nondestructive radiation screening tests are required for the CLSIC, the manufacturer should use the test methods and procedures required by the detailed specification.

4.9 CLSIC MASTER SCHEDULE

The contractor should develop and maintain a master schedule for the CLSIC program that shows the schedule of major milestones and formal reviews.

SECTION 5

DESIGNER CAPABILITY AUDIT

5.1 GENERAL REQUIREMENTS FOR A DESIGNER CAPABILITY AUDIT

The request for a designer capability audit is submitted to the contracting officer by the contractor. The audit team reviews the designer's capability in the areas of organization. program management, design, design rules, design verification, configuration control, and documentation as applicable. The designer is presented with a preliminary list of discrepancies found by the audit team members during the exit critique. Each audit team member submits to the audit team chairman, within 10 working days following the audit, a letter detailing findings, discrepancies, and recommendations. The chairman submits a formal report summarizing the audit findings, including required corrective actions, to the contracting officer, contractor, and designer within 20 working days following the audit. The contractor and designer are advised of acceptable designer capability by the contracting officer subsequent to correction of discrepancies or implementation of corrective actions.

5.2 AUDIT TEAM

5.2.1 Members of the Audit Team. The audit team should be composed of members representing the contractor(s) and the contracting officer. The audit team would normally consist of four to six members nominated by the contractor. The contracting officer should approve the members of the audit team and select the chairman for the audit.

5.2.2 Responsibilities of the Audit Team Chairman. The audit chairman's responsibilities include the following:

a. Review the technical qualifications of the audit team members.

b. Schedule the audit in coordination with the designer and audit team members.

c. Inform the team members of the audit schedule not less than 20 working days in advance.

d. Ensure that the team members received the applicable preaudit documents from the designer prior to the actual audit.

e. Conduct meetings with the audit team members during the audit.

f. Conduct the exit critique.

g. Prepare a report to the contracting officer within 20 working days identifying any deficiencies or discrepancies and stating the recommended actions.

h. Schedule and arrange for reaudit or follow-up audit.

i. Ensure that the designer's proprietary information is properly safeguarded.

5.2.3 Deficiencies. The deficiencies or discrepancies are classified according to their severity. The audit team should determine whether correction of the deficiencies is required or recommended. A reaudit may be scheduled to ensure that the discrepancies are corrected.

5.3 DESIGNER AUDIT DETAILS

Detailed information should be given on the designer's recent design, fabrication. reliability. and testing experience as well as other accomplishments in the proposed technology and device complexity. The information should also include names of users, descriptions of devices, and dates of development and manufacture.

5.3.1 Designer Preaudit Information. The designer should submit to the audit team chairman, at least 20 working days before the scheduled audit, documents describing the designer's prior experiences and accomplishments in CLSIC design and implementation. The documents should also include: an organization chart; list of facilities, equipment, and personnel; schedule; and the design baseline as detailed in the following paragraphs.

5.3.1.1 Organization Chart. The chart should show the lines of authority for origination, approval, implementation, and control of designs of the proposed CLSIC.

5.3.1.2 Facilities, Equipment, and Personnel. Information should be given on the facilities, equipment, and manpower to be dedicated to the proposed program.

5.3.1.3 Schedule. An estimated schedule, with intermediate milestones, should be given for the delivery of the CLSIC design.

5.3.1.4 Design Baseline. The design baseline applicable to the CLSIC should be identified.

5.3.2 Audit Team Plan and Approach. The following issues should be addressed by the audit team:

a. Choice of technology

b. Design philosophy

c. Design rules and data base

d. Design tools

e. Mask verification to the logic and to the circuit analysis

f. Engineering release system

g. Change controls (process, materials, and design)

h. Manufacturing interface including failure analysis and device characterization.

5.3.3 Evaluation of Designer's Capabilities. The audit team should evaluate the designer's capabilities.

5.3.3.1 Design and Design Verification Procedures. The design, design for testability, circuit design rules, layout rules, analysis, and tests should meet the requirements of the detailed specification or contract. The procedure and controls used for implementing the design requirements into physical layout and processing requirements, such as masks and diffusion information, should be documented. The interface procedures and controls between the designer, manufacturer, and testing organization should be defined.

5.3.3.2 Computer-Aided Design Capability. The computer-aided design capability should be demonstrated to the audit team. Its capability should include, but not be limited to:

a. Logic simulation

b. AC and DC analysis

c. Design graphics capability to generate circuit schematics, topological layout, symbolic layout, and documentation

d. Design rule checking

e. Geometrical pattern generation and wafer mask fabrication

f. Cell library (gates, macrocells, custom)

g. Test pattern generation

5.3.3.3 Testability and Fault Tolerance Design Capability. The designer should demonstrate the capabilities in designing specified testable CLSICs. In addition, the capability of designing special test chips or structure(s) to be used for process control, electrical tests, and radiation response should be documented. The means of evaluating testability in a quantitative manner should be demonstrated. The procedures for validating the in-process screening, post-assembly screening, and lot conformance tests should be described.

5.3.3.4 Design Validation. The approach to final design validation should be described.

5.3.3.5 Documentation. The design standards and interface controls should be documented.

5.3.3.6 Packaging Design. The designer should provide information which demonstrates that the packages planned for usage are suitable for high reliability applications.

5.3.3.7 Power Dissipation. The designer should demonstrate analyses of power dissipation requirements by conducting thermal design and analysis or thermal verification tests.

5.3.4 Hardness Assurance. The designer should demonstrate capability of meeting the hardness assurance requirements, when applicable, for the design and development of the CLSIC, including the following:

a. The use of layout rules, circuit design rules, processing, assembly, and packaging, critical to hardness

b. Experience in hardness assurance modeling and analysis, testing techniques, and data analysis

SECTION 6

MANUFACTURER CAPABILITY AUDIT

6.1 GENERAL REQUIREMENTS FOR A MANUFACTURER CAPABILITY AUDIT

The request for a manufacturer capability audit is submitted to the contracting officer by the contractor. The audit team should review the manufacturer's capability in the areas of organization, program management, process control, material control, tool control, corrective action procedures, testing, screening, wafer lot acceptance, fabrication, assembly, environmental tests, electrical characterization tests, product assurance programs, and documentation as applicable. The manufacturer is presented with a preliminary list of discrepancies found by the audit team members during the exit critique. Each audit team member submits to the audit team chairman, within 10 working days following the audit, a letter detailing findings, discrepancies, and recommendations. The chairman submits a formal report summarizing the audit findings, including required corrective actions, to the contracting officer, contractor, and manufacturer within 20 working days following the audit. The contractor and manufacturer are advised of acceptable capability by the contracting officer subsequent to correction of discrepancies or implementation of corrective actions.

6.2 AUDIT TEAM

6.2.1 Members of the Audit Team. The audit team should be composed of members representing the contractor(s) and the contracting officer. The audit team would normally consist of four to six members nominated by the contractor. The contracting officer should approve the members of the audit team and select the chairman for the audit.

6.2.2 Responsibilities of the Audit Team Chairman. The audit chairman's responsibilities include the following:

a. Review the technical qualification of the audit team members.

b. Schedule the audit in coordination with the manufacturer and audit team members.

c. Inform the team members of the audit schedule not less than 20 working days in advance.

d. Ensure that the team members received the applicable preaudit documents from the manufacturer prior to the actual audit.

e. Conduct meetings with the audit team members during the audit.

f. Conduct the exit critique.

g. Prepare a report to the contracting officer within 20 working days identifying any deficiencies or discrepancies and stating the recommended actions.

h. Schedule and arrange for reaudit or follow-up audit.

i. Ensure that the manufacturer's proprietary information is properly handled.

6.2.3 Deficiencies. The deficiencies or discrepancies are Classified according to their severity. The audit team should determine whether correction of the deficiencies is required or recommended. A reaudit may be scheduled to ensure that the discrepancies are corrected.

6.3 MANUFACTURER AUDIT PROCESS

6.3.1 Manufacturer Preaudit Information. The manufacturer should submit to the audit team chairman, at least 20 working days before the scheduled audit, documents describing the manufacturer's recent experience in fabricating and testing CLSIC devices with complexity and technology similar to the proposed CLSIC. The information should include the names of the users, the description of the devices, and the dates of development and manufacture. The documents should also include an organization chart; a list of facilities, equipment, and personnel; a schedule; and the manufacturing baseline as detailed in the following paragraphs.

6.3.1.1 Organization Chart. The chart should show the lines of authority and responsibility for origination, approval, implementation, and control of the fabrication, inspections, and testing of the proposed CLSIC.

6.3.1.2 Facilities, Equipment, and Personnel. Information should be given on the facilities, equipment, and manpower to be dedicated to the proposed program.

6.3.1.3 Schedule. An estimated schedule, with intermediate milestones, should be given for the delivery of the CLSIC.

6.3.1.4 Manufacturing Baseline. The manufacturing baseline applicable to the CLSIC should be identified.

6.3.2 Audit Team Plan and Approach. The following issues should be addressed by the audit team:

a. Facilities

b. Test equipment

c. Process controls

d. Material controls

e. Quality controls

f. Change controls

g. Engineering interface including failure analysis

6.3.3 Evaluation of Manufacturer's Capabilities. The audit team should evaluate the manufacturer's capabilities including the following areas.

6.3.3.1 Manufacturing Baseline. Specific details of the fabrication process should be documented by the manufacturer and should be made available to the audit team, contractor, or contracting officer, upon request. These should include, but not be limited to, the following items: specification of the initial wafer conditions including crystalline orientation, uniform doping level, and dopant(s), if present. All processing step information should be presented in the order in which the steps are to be performed, and time and temperature data should be provided for each step. For oxidations, the ambient should be specified. For ion implantations, the implanted element. dose, and energy should be specified. For diffusions, the impurity and the source should be detailed. For epitaxial growth, the source, target epitaxy thickness, impurity element, and target concentration should be provided. For chemical vapor deposition, the deposited material and target thickness should be detailed. Typical impurity profiles for the devices on the CLSIC should be provided to the contractor or contracting officer upon request. The following should be included: metallurgical junction depths, surface impurity concentrations, sheet resistivities (for all layers), and device vertical and lateral dimensions and tolerances for each device type represented in the CLSIC.

6.3.3.2 Manufacturing and Product Assurance Program. The product assurance program should demonstrate and assure that the

manufacture, inspection, and testing of the CLSIC and associated test structures are in accordance with requirements for space quality parts, the requirements of applicable specifications, and the requirements herein.

6.3.3.3 Fabrication and Wafer Process Control. The fabrication capability of the manufacturer for the proposed CLSIC technology and complexity should be demonstrated. The process control procedure(s) should be documented and demonstrated to the audit team.

6.3.3.3.1 Wafer Lot Acceptance. Wafer lot acceptance tests should be in accordance with the detailed specification.

6.3.3.3.2 Wafer Probe. The manufacturer should provide information relative to the wafer probe test capability and final test capabilities including availability of:

a. Test program(s) and control

b. Electrical parameter test capability information

c. Adequate equipment (e.g., for testing at temperature extremes)

6.3.3.3.3 Fabrication Capability. The manufacturer should demonstrate the capability to perform and control the following processes and steps:

a. Incoming materials inspection to the acceptance criteria

b. Calibration

c. Environmental control(s)

d. Purity control of water and materials

e. Wafer fabrication (including all processes, process records, and controls)

f. Contamination

g. Deposition of dielectrics

h. Assembly

i. Mask fabrication and inspection

j. Operator training and certification

6.3.3.3.4 Process Control. The manufacturer should identify all the controls maintained on the incoming materials, environments, and wafer fabrication process. The records should include charts with parameter limits that show continuous control of the processes.

6.3.3.3.5 Test Structures. The manufacturer should describe and demonstrate capabilities of the parametric test structures used in process control and evaluation, both individually and in selected combinations thereof, and indicate the acceptance criteria derived from them.

6.3.3.3.6 Metallization. Evidence should be presented which demonstrates the quality and stability of the metallization layers and other intraconnects, as applicable. This includes consideration of electromigration, maximum allowable current density used in the design, and maximum temperature applicable to testing and system usage. The equipment and procedures for conducting scanning electron microscope (SEM) examinations should be demonstrated.

6.3.3.3.7 Capacitance versus Voltage Plotting. The techniques, equipment, frequency of test, and test conditions including time, temperature, and bias should be specified and demonstrated.

6.3.3.3.8 Assembly and Package Controls. The manufacturer should monitor the assembly steps and sealing operation and document the procedures employed and the limits imposed. The manufacturer should document the corrective action taken for lots which exceed any of the parameter limits.

6.3.3.3.9 Die Shear and Wire Bond Pull Tests. Where applicable, a die shear test and a wire bond pull (destructive and nondestructive) test capability should be demonstrated by the manufacturer. Documentation should include sample size, frequency of testing. records, traceability and recall, and disposition of all units bonded following the failure of a test.

6.3.3.3.10 Internal Visual Inspection. An internal visual inspection capability should be demonstrated by the manufacturer. Capability of meeting the requirement of Method 2010, MIL-STD-883 should be demonstrated, as applicable to the proposed CLSIC.

6.3.3.3.11 Dielectric Defects. For technologies which use thin dielectrics (less than 0.2 micrometers thick), the manufacturer should demonstrate the in process means of measuring and controlling defects in the dielectric layers.

6.3.3.4 Acceptance Tests. The equipment, test methods, control, and procedures for conducting the post-assembly screening tests and the lot conformance tests should be documented, and the tests should be demonstrated to the audit team.

6.3.3.4.1 Post-assembly Screening Tests. The manufacturer should demonstrate capability to perform the applicable post-assembly screening tests and should provide documentation for conducting the tests. The applicable post-assembly tests include:

		MIL-STD-883 Method
a.	Lead integrity	2004
b.	Stabilization bake	1008
c.	Burn-in test	1015
d.	Steady-state life	1005
e.	Temperature cycling	1010
f.	Constant acceleration	2001
g.	PIND	2020
h.	Fine and gross seal	10'
i.	Internal water vapor content	1016
j.	Resistance to solvent	2015
k.	Solderability	2003
l.	Radiographic inspection	2012
m.	Electrostatic discharge sensitivity	3015
n.	Internal visual	2010
o.	Internal visual for DPA	2013
p.	Other tests as may be applicable to the CLSIC	

6.3.3.4.2 Electrical Tests. The manufacturer should provide a program plan outlining methods used to verify that the

CLSIC electrical characterization meets design requirements. In addition, the manufacturer should demonstrate the ability to conduct other required activities following the post-assembly screening tests and the end point electrical measurements following radiation testing. These include:

a. Static, dynamic, and functional tests at various temperatures and speeds

b. Delta computation and data analysis

c. Acceptance and rejection criteria

d. Test procedures and controls

e. Other tests as may be applicable to the CLSIC

6.3.3.4.3 Failure Analysis and Corrective Action Capabilities. The manufacturer should demonstrate the capability of performing failure analysis and should provide documentation on:

a. Failure reporting system

b. Facilities and equipment list

c. Failure analysis reports

d. Corrective analysis reports and corrective action procedures

6.3.4 Hardness Assurance. The manufacturer should demonstrate the capability of meeting the hardness assurance requirements, when applicable, for the fabrication and testing of the CLSIC, including the following:

a. Radiation effects analysis including results of past studies

b. Capability of providing test structures or combinations of test structures which yield information that can be used for radiation response testing and analysis

c. Radiation testing procedures and analysis

d. Experience with radiation facilities and dosimetry

In those cases where the manufacturer subcontracts all radiation effects analysis and testing, the manufacturer should demonstrate, by example, his ability to manage such contracts.

THIS PAGE INTENTIONALLY LEFT BLANK

SECTION 7

CLSIC CONCEPTUAL PHASE

The conceptual design phase is the initial phase of the technical program. During this phase, the formal descriptions of the behavior and architecture of the integrated circuit(s) are developed including the major building blocks, their interconnection, and the layout or chip floorplan, The choice of design methods and the specification of requirements for the behavior, performance, power consumption, reliability. testability, and interface of the CLSIC should be described. Tradeoffs between potentially competing factors are to be identified and analyzed. The functional design of the CLSIC should be as general as possible within the constraints and requirements of the application. These items should be documented and submitted for review to the PMPCB before the functional design phase is implemented.

7.1 DESIGN REQUIREMENTS, DESCRIPTION, AND SYNTHESIS

7.1.1 System Behavioral Description. The behavioral requirements for the proposed CLSIC design should be established, based upon the system behavior in which the CLSIC is embedded. An analysis of the system behavior should be performed by the contractor, or furnished to the contractor by the contracting agency, according to the contract statement of work. The system behavior should be described formally, either by means of formal graphic models or with a hardware descriptive language, and should include descriptions of data flow and control flow. If an informal description is furnished to the contractor by the contracting agency. then the contractor should translate this description into a formal one.

7.1.2 CLSIC Behavioral Description. The CLSIC behavior should be described, using either formal graphic models or a hardware descriptive language. This description should contain the externally visible behavior and interface to the programmer, if the CLSIC is programmable. The complexity of the CLSIC architecture may require hierarchical decomposition of the design to allow adequate description before initiation of the register-transfer and logic design. Should this be the case, only the highest level of design should be described during this phase, with lower levels of design being addressed during the functional design phase. The description of the CLSIC should include descriptions of data flow and control flow. They may be combined in a single description (e.g., with a hardware descriptive language). This description should include any behavior resulting from fault-tolerant or testing requirements.

7.1.2.1 Data Flow. The data flow description should include the following information:

a. The input and output specification for the integrated circuit

b. The set of operations to be performed on the data

c. The ordering of operations on the basis of data availability and the potential parallelism in the design

d. The required accuracy (bit widths and representation) of the data

Tools to describe data flow include hardware descriptive languages, data flow graphs, and data flow languages. The choice of the descriptive tool depends on the descriptive requirements of each design.

7.1.2.2 Control Flow. The control flow description should contain a specification of the timing of the input and output data sequences and a specification of when and under what circumstances each operation in the data flow is performed. Tools to describe control flow include hardware descriptive languages, Petri Nets, state diagrams, and state tables. The choice of a descriptive tool depends on the descriptive requirements of each design. Precise timing of inputs and outputs, conditional execution, concurrent operations, major state sequencing, and response to error conditions should be included in the control flow description whenever applicable.

7.1.3 Architecture. The architecture of the CLSIC corresponding to the behavioral description should be specified. This specification should include the following information, as applicable:

a. The major building blocks and their interconnection, in block diagram form

b. The size of memory and number of registers available to the programmer

c. The general layout or floorplan

7.1.3.1 Design Style. The global shape of the data flow, as it is to be implemented in hardware, is described by the design style. Examples include:

a. Central arithmetic logic unit

b. Random (unstructured)

c. Parallel

d. Pipelined

The design style chosen for utilization should be described, preferably in a hardware descriptive language. The basis for selection of the design style should be documented and should include a tradeoff analysis.

7.1.3.2 Design Rules. Any architectural-level design rules that can be defined at this time, based on the analysis of the system requirements and preliminary design constraints. should be documented for use in subsequent design phases. (An example of such a rule would be a requirement that a programmable chip contain unused opcodes for future extension.)

7.1.4 Technological Requirements and Constraints.

7.1.4.1 Packaging The integrated circuit should be designed for use in a hermetically sealed package employing glass, metal, ceramic, or combination of these materials.

7.1.4.2 Interfacing. System interfacing requirements should be established and documented, both for use as a basis for package pin-out and for reference in subsequent design phases.

7.1.4.3 Power Consumption. Power consumption limits should be established, based on system constraints.

7.1.4.4 Other. Other technological requirements and constraint having impact on the architectural–level design and specification of the integrated circuit should be identified and documented by the contractor and included in the preliminary design specification.

7.2 RELIABILITY REQUIREMENTS

The contractor should determine the reliability requirements for the CLSIC and perform a reliability analysis of the planned design. The requirements and analysis should be based on the specifications set forth by the contract and should be consistent with the requirements for system reliability (based upon mission lifetime, operating environment, and radiation vulnerability). Both mean time between failures and mean time between errors should be included. Multiple simultaneous soft errors should also be considered. The

contractor should incorporate such fault-tolerant techniques as may prove necessary to enhance the inherent reliability of the circuitry and to meet the required reliability levels. Such techniques include the following, both individually and in some combination:

a. Redundancy

b. Error detection and correction

c. Self check

d. Self test and self reconfiguration

e. Testability

The implementation of these techniques should be consistent and compatible with the requirements for testability.

7.3 DESIGN VALIDATION AND VERIFICATION

When practical, the method for verifying logical correctness of the design should involve formal proof techniques (for example, symbolic simulation). If such techniques cannot be used on sections of the CLSIC, the behavior of the CLSIC should be simulated to demonstrate total compliance with the behavioral requirements of the system into which the CLSIC is to be embedded. The model to be simulated should be the behavioral description. If no further design levels (between the logic design level and this level) are identified, then this simulation model should serve as a reference for all verification and validation processes associated with the logic level. The input test data for the simulation should be chosen such that each conditional branch in the model is simulated at least once.

7.4 TRADEOFF ANALYSIS

A comprehensive tradeoff analysis (at the conceptual level) should be performed and documented. The analysis should treat the issues of testability, reliability, hardness, and behavior, with consideration of system requirements and constraints. Architectural tradeoffs should be addressed, including alternative assignments of functions to structures and alternative fault-tolerant implementations. The relative merits of built-in test structures versus external test equipment utilization for the particular design and application should be examined with respect to constraint on testability and testing.

7.5 CONCEPTUAL DESIGN DATA BASE

The conceptual design phase data base should contain the descriptions of the overall behavior, major internal building blocks, internal interconnection, and the chip floorplan of the integrated circuit. Any information (such as that used for simulations and analysis) which influenced the architectural design process, including system level information and documentation of the conceptual design phase, should be included in the data base. The documentation should contain the rationale for the choice of design style and design methods and the tradeoff analyses between potentially competing factors in the design. Included in the conceptual design documentation should be a statement explaining the preliminary architectural design decisions influenced by the intended system usage. All relevant documents, reports, diagrams, and software containing information used in the architectural design should also be included in the documentation package. Thus, the data base should constitute the conceptual design and should be used as a means of communicating design requirements.

7.6 TESTABILITY ANALYSIS, CONCEPTUAL DESIGN PHASE

During the conceptual design phase, the testability of the CLSIC design should be analyzed in a qualitative manner to ensure that the required level of testability can be achieved (See 3.5 in Appendix B). This analysis should give particular attention to the following topics:

a. The provision of a sufficient number of test and control points for test pattern injection and response observation

b. The ability to partition the design into subcircuits that allow the required levels of fault coverage to be achieved. Particular attention should be paid to the testability of redundant circuitry

c. The ability of the built-in test features to meet the self-checking requirements of the design.

d. The formulation of the specific testability measures or figures of merit to be used, which should include testing confidence level, testing speedup, hardware circuit overhead, software and

firmware overhead, performance degradation (if any), fault resolution, and reliability degradation (if any). The range of values for these measures permitted in the design should be specified by the contractor and submitted to the contracting agency for approval. The contractor should also specify the means to be used to validate the CLSIC design with respect to the proposed testability measures.

7.7 RADIATION HARDNESS, CONCEPTUAL DESIGN PHASE

Prior to any decision to initiate the development of CLSICs for a system, an assessment should be performed by the contractor to determine the feasibility of meeting the hardness requirements with a given design and technology (see Appendix A). In order to perform this feasibility study, the procedures outlined in the following paragraphs should be followed.

7.7.1 Device Radiation Specification Level. The contractor should obtain. by analysis, the radiation environments that the CLSICs would be exposed to during the course of a mission. These environments should be determined from the free field radiation environments specified for the system. Then, using the proposed system configuration, one should estimate or calculate the transport of the free field environment to the CLSIC location. These device radiation environment levels, or the worst case levels during the service life, should be used as the radiation levels for the design. product evaluation. characterization. and lot conformance testing (see Appendix A). If a proposed CLSIC is to be used in more than one application, the device radiation level specified for each environment should correspond to the worst case application.

7.7.2 Device Performance Requirements. The contractor should specify the end point electrical and timing parameters, tolerances, and recovery time allowed following a nuclear event, if applicable. The end of mission electrical and timing parameters should also be specified. Examples are maximum clock frequency and power supply current for total dose irradiation on MOS circuits and output drive and input leakage for neutron irradiation on bipolar circuits.

7.7.3 Radiation Characterization Data Base. The contractor should be responsible for establishing a radiation effects characterization data base for the proposed technology to be used for the CLSICs. The data base should include, but not be limited to, all anticipated environments of the mission. The order of preference for these data should be:

a. First, data from custom large scale integrated circuits similar in function to the proposed device that were built with the proposed technology using the same process baseline and design rules.

b. Second, data from medium scale integrated circuits that were built with the proposed technology.

co Last, if “a” or “b” is not available for characterization, an experimental circuit using sizes comparable to those in the proposed CLSIC and using the proposed technology should be designed and built for initial product evaluation testing to determine the radiation characterization.

All circuit and test structure characterization data should be taken on devices manufactured by the proposed manufacturer of the CLSIC. This data base should be maintained in order to determine the feasibility of meeting the radiation requirements with the proposed design and technology for the CLSICs.

7.7.4 Feasibility Analysis for Meeting the Radiation Requirements. The contractor should demonstrate, by analysis, that the proposed design and technology for the CLSICs are capable of meeting the radiation requirements. This analysis, including latch-up analysis, should be based on the radiation performance parameters derived from the characterization data base, the electrical performance requirements established for the CLSIC, and the radiation environments derived for the CLSIC. If the only data available are on test structures or test devices, then the feasibility analysis should involve a circuit analysis using degraded device performance or transient response to predict the CLSIC performance. If it cannot be demonstrated that the proposed CLSIC design and technology can meet all of the radiation requirements, then alternative designs or technologies should be used. The results of this feasibility analysis should be presented at the preliminary design review.

7.8 TECHNICAL REVIEWS AND SURVEILLANCE

During the conceptual design phase, cognizant contractor engineering personnel should visit or be resident at the designer's facility to review the status of the design effort. Design, analysis, plans, schedules, and test documentation that have been generated should be reviewed, and plans for future effort should be reviewed and approved during these visits.

SECTION 8

FUNCTIONAL DESIGN PHASE

The functional design phase follows the conceptual phase of the technical program. It is concerned with the specification of the register-transfer level and logic level designs. The design depends upon the integrated circuit technology to be employed in the physical implementation of the CLSIC, and the design rules and constraints associated with both the technology and the specific line on which fabrication is planned to take place. This phase should include a feasibility analysis which demonstrates the adequacy of the proposed design and technology to meet the radiation and reliability requirements.

8.1 DESIGN REQUIREMENTS

During this design phase, the original architectural design should be modified to include the details remaining from the conceptual design phase and any modifications to the preliminary architectural design made to meet technology compatibility requirements. Three primary criteria should be employed in the design of the CLSIC. They are functionality, testability, and reliability.

Both the register-transfer and logic designs should be carried out in four well-defined and documented stages representing description, synthesis, evaluation, and validation. The description of the design should be formal, preferably by using a hardware descriptive language. The synthesis of the conceptual design down to the register-transfer and logic design level should be done either manually or by using synthesis software. Logic and fault simulation should be performed in accordance with the detailed requirements of this document. Failure modes and the fault populations to be used as a basis for testing should be defined. Testability features should be evaluated to ensure that the design supports the required level of testing. The testability evaluation should give particular attention to circuit partitioning and to the capability of the CLSIC design to provide test control and test access. Test vectors for built-in test features or automatic test equipment should be generated and their effectiveness evaluated in a quantitative manner. Particular emphasis should be given to predicted levels of fault detection. Fault isolation within the CLSIC should also be determined to assist process control. The evaluation should also consider timing and other design constraints and performance criteria. Design

validation at the register-transfer and logic design levels should be documented and presented at the preliminary design review.

8.1.1 Design Description. Description of the design should preferably be through use of a hardware descriptive language. Register-transfer descriptions contain information about the movement of vectors of data through combinational logic and into and out of registers. Logic-level descriptions contain information about the implementation of the Boolean functions specified in the register-transfer description. Both levels of description should be structured hierarchically, and labels (names) used in the descriptions should be consistent with all other design documentation.

8.1.2 Design Synthesis. Synthesis of the register-transfer and logic designs should be done by transforming the conceptual design formal description to the register-transfer and logic formal description either manually or by using synthesis software.

8.1.3 Design Evaluation. Evaluation should be done to determine that design requirements have been met. Performance evaluation should be carried out either by a timing simulation or by means of a critical path timing analysis. The timing simulation should be detailed enough to model significant propagation delays existing due to characteristics of the proposed floor plan and layout methodology. The testability of the design should ensure that the required level of testing is adequate. The evaluation should include an analysis of reliability and fault–tolerance.

8.1.4 Design Validation. The behavioral model (corresponding to the behavioral description) should be used as a reference for validation and verification of the logic design. Where possible, the method for verifying logical correctness of the design should involve formal proof techniques. If such techniques cannot be used on sections of the CLSIC, a detailed simulation and logic simulation should be performed and the results should be correlated with the results of the simulation in 7.3. At the very least, the input test data for the simulations should be chosen such that each conditional branch in the models is simulated at least once. Any part of the design which has been generated automatically from a higher level design need not be validated if the automatic design system has been validated. Design validation at the register-transfer and logic design levels should be documented and presented at the component preliminary design review.

8.2 Hardness Categorization.

8.2.1 Initial Categorization. Based on the specified radiation levels, the characterization data for the device, and the feasibility analysis, the contractor should determine the hardness category for the CLSIC in each radiation environment. For each type of radiation environment, there are three radiation hardness categories of interest, i.e., Hardness Critical Category 1, Hardness Critical Category 2. and a Hardness Noncritical Category. The radiation hardness categorization criteria are presented in Appendix A. The categorization criteria are based on the radiation design margin, sample size, confidence level, required survival probability, and the standard deviation.

8.2.1.1 Hardness Critical Category 1. Hardness Critical Category 1 devices have a radiation design margin that is between a specified minimum acceptable value (say 1.4) and the minimum radiation design margin specified for Hardness Critical Category 2 devices (typically about 10). Therefore, devices that are in Hardness Critical Category 1 for a particular radiation environment have a lower radiation design margin in that environment than devices that are in Hardness Critical Category 2. Because of the low radiation design margin, radiation hardness lot conformance testing is required on every production lot for each environment where the devices are in Hardness Critical Category 1.

8.2.1.2 Hardness Critical Category 2. Hardness Critical Category 2 devices have a radiation design margin that equals or exceeds the upper limit specified for Hardness Critical Category 1 devices (typically about 10), but is less than the minimum radiation design margin specified for Hardness Noncritical Category devices (typically about 100). To assure that the devices are in the correct category, radiation hardness lot conformance testing is required on the first production lot for each environment where the devices are in Hardness Critical Category 2. Because of the higher radiation design margin, radiation hardness lot conformance testing is not usually required on subsequent production lots of Hardness Critical Category 2 CLSICs.

8.2.1.3 Hardness Noncritical Category. CLSICs devices that have an extremely high radiation design margin, typically over 100, may be considered to be in a special Hardness Noncritical Category. This occurs when no radiation environment level is specified, or when the specified radiation environment level is small compared to the level that represents the inherent device tolerance to that type of radiation. No radiation hardness lot conformance testing is required for those

environment where the devices are in the Hardness Noncritical Category, except as might be required on the first production lot for device characterization.

8.2.1.4 Category Selection. In each application using CLSICs, one would like to first select devices in the Hardness Noncritical Category, and if they are not available, then in the Hardness Critical Category 2. This is not only because of their higher radiation design margins and therefore lower failure risk in the operational environment, but because the radiation hardness lot conformance testing costs are less. Radiation hardness lot conformance testing is only required for the first lot for Hardness Critical Category 2. Unfortunately, devices may not be available in either of these categories for the specified levels of all of the various types of radiation environments. For those radiation environments where the Hardness Critical Category 2 criteria cannot be met, devices would be specified in the Hardness Critical Category 1. Of course, Hardness Critical Category 1 devices may be used whenever Hardness Noncritical Category devices or Hardness Critical Category 2 devices would not be practicable or cost-effective, or would not be available when needed.

8.2.2 Category Reevaluation. Changes in many factors, such as the specified radiation levels for a particular device, may change the radiation hardness category of that device. The radiation hardness categorization is therefore an iterative process for the CLSIC. Typically, the location and therefore the transported environment for the application, may change during the development. Also, the characterization for the CLSIC may vary from prototype results to the results from initial production units. The standard deviation used in the categorization should represent the variation between lots based on data or estimation of worst case value. The initial categorization in each radiation environment should be based on the radiation design margins for the parts estimated from the characterization data base and feasibility analysis. The categorization in each radiation environment should then be reevaluated based on any additional hardness evaluation testing. Also, based on the results of lot conformance testing for the first lot or of any succeeding lot, the CLSICs may be reclassified from one category to another. Note that changes in the radiation hardness category of a production device do not change the inherent radiation hardness of that device.

8.3 TESTABILITY DESIGN REQUIREMENTS

The CLSIC should be designed to maximize its testability within the constraints imposed by the specified requirements (see 3.6 in Appendix B). The resolution and precision of the

planned tests should be consistent with the performance and reliability requirements of the CLSIC. In general, each design step in achieving the required functions should be matched by an associated test step that would allow the certification of the function. In all cases, the design should include the following testability features:

a. A means of injecting test patterns or stimuli, as required (controllability requirement)

b. Adequate access for checking purposes to the internal states or signals of the CLSIC (observability requirement)

c. Timely and unambiguous indication of the presence of errors

d. Comprehensive checking of the built-in test circuitry itself

These design goals should be achieved by the inclusion of one or more of the design features set forth in the following paragraphs.

8.3.1 Simplicity and Regularity. If permitted by design requirements, the designer should provide regularly structured designs using standard cells rather than randomly structured circuitry or nonstandard cells (see 3.6.1 in Appendix B).

8.3.2 Circuit Partitioning. The designer should design the integrated circuit such that relatively small independent and manageable blocks of circuitry can be defined as the basis for test generation, documentation, and evaluation. The partitioning of the circuit into subcircuits (groups of cells) should be accomplished to maximize the testability of the CLSIC (see 3.6.2 in Appendix B). If fault-tolerant features are included in the design specifications, the designer should integrate design for fault tolerance with design for testability. The design should provide the means for independent testing of redundant circuitry.

8.3.3 Built-in and External Testing. The contractor should incorporate a combination of built-in testing features into the CLSIC with provisions to accommodate external testing to provide fault coverage consistent with the system reliability specifications (see 3.6.3 in Appendix B). Alternative designs should be analyzed to arrive at an optimal testability configuration. The contractor should include test signals at subcircuit interfaces that maximize the similarity of testing by built-in and external test equipment.

8.3.4 Test and Control Point Allocation. Sufficient input and output connections and their associated circuits should be included in the CLSIC design to meet the controllability and observability requirements; but the total connections should be consistent with the connection constraints imposed by circuit technology and packaging requirements (see 3.6.4 in Appendix B). These test and control points may be provided on an ad hoc basis to improve controllability and observability at a local level. Alternatively, test and control points may be provided systematically by the use of structured design techniques like scan-in/scan-out. Where necessary, test points should be employed to permit redundant circuits to be made temporarily nonredundant during testing.

8.3.5 Test Memory Allocation. Test memory should be assigned to nonalterable memory resources (e.g., read-only memories) in a manner that ensures the integrity and reliability of the built-in test process (see 8.5.2 and Appendix B 3.6.5).

8.3.6. Self-Checking Circuits. Provisions should be made for sufficient additional bits (check bits) to be added to data words to provide for code-based error detection and correction, as required (see 3.6.6 in Appendix B). The necessary encoding and decoding check circuits should be included in the CLSIC design, and provisions should be made to make the check circuits self–checking, if specified.

8.3.7 Initialization. The contractor should design the CLSIC such that it is capable of being placed into a well defined initial state to commence the testing process (see 3.6.7 in Appendix B).

8.3.8 Interfacing to External Test Equipment. Consideration should be given to the interfacing of the device under test to the appropriate automatic test equipment (see 3.6.8 in Appendix B). The packaging and external connections should be consistent with the interfacing capabilities of the specified automatic test equipment. The designer should determine the number and respective functions of pins on the CLSIC to be dedicated to test functions, based upon fault isolation requirements.

8.3.9 Error Detection. To the extent practicable, all designs should include sufficient interrupt and trap capability to support the immediate processing of critical errors detected by self-check circuits prior to the loss of information concerning the nature of the error (see 3.6.9 in Appendix B).

8.3.10 Design Requirements for Hardness Assurance Testability. In the design and layout of CLSICs, the designer is required to make the following provisions for hardness assurance.

8.3.10.1 Testable Networks. The designer may be required to ensure that certain networks within the large scale integration array can be tested for radiation response. Special requirements for network testability should be as specified in the applicable detailed specification.

8.3.10.2 Special Probe and Bond Pads. The contractor may require the designer to provide special probe or bonding pads to be used for special radiation effects testing and analysis. These probe or bonding pads should be included in the layout for the CLSIC as specified in the detailed specification.

8.4 TEST CHIPS AND STRUCTURES

8.4.1 Test Structures. Test structures shall be incorporated at appropriate locations on all wafers and, where applicable, on each chip to provide data for use in simulation, evaluation, process control, and verification procedures.

8.4.1.1 Process and Device Characteristics. Test structures should be provided to evaluate process, material, and device parameters such as layer uniformity, interface properties, crystalline defects in the semiconductor material, sheet resistance for each nondielectric layer (e.g., diffused or implanted region, polysilicon, metal, or other), contact resistance, dielectric thickness (using capacitor), transistor parameters, surface mobility, electrical line widths, junction leakages, interface state density, surface concentrations or doping profiles, metal-to-silicon contact resistance, insulator thickness, interface state density, and leakage current.

8.4.1.2 Design Layout Rules. Test structures should be provided to evaluate the geometrical layout features forming the geometrical layout-rule set and to allow electrical or optical evaluation of layer-to-layer misalignments which might occur during fabrication. These test structures include cross-bridge sheet resistors, isolation resistors, and bridge alignment resistors and structures to evaluate design rules such as the gate to contact spacing for MOS or the metal and diffusion overlap on contacts. Also, in order to magnify problems and aid in the diagnostic capability, structures with design layout rules beyond worst case should be added, when feasible, and monitored. These types of structures will help to define process and device limits and assure reliability.

8.4.1.3 Global Random Defects. Test structures should be provided to evaluate the occurrence of global random defects in the semiconductor materials. These structures should evaluate the integrity of contacts, conductors, and dielectric material. These structures may include series, parallel, and addressable arrays of identical elements. Layers of conductors separated by deposited dielectrics are useful in finding dielectric defects.

8.4.1.4 Circuit Performance. Test structures should be used to ensure that the wafer fabrication process is capable of producing a functioning circuit and to characterize the dynamic performance of both test and production circuits. Unless otherwise specified, a ring oscillator type circuit should be used to measure gate delay. Additional circuits such as RAM. MACROs, and inverter chains may be included as suggested by the device design.

8.4.1.5 Device and Circuit Reliability (including radiation hardness). Test structures should be provided to establish circuit reliability assurance by evaluating the stability of the semiconductor materials when subject to stresses such as voltage, temperature, humidity, and radiation. These structures should include transistors and capacitors for measurements such as oxide charge density and threshold voltage shifts, diodes for the measurement of changes in junction leakage, and resistors for the measurement of current carrying capabilities and electromigrations. Provisions should a1so be included for measuring dielectric breakdown voltage for each dielectric layer. The breakdown test is a destructive test; therefore, several structures would be required to obtain values over the thermal range. A ring oscillator type structure should also be included to determine the shift, if any, in gate delay as a result of thermal stress or radiation. To evaluate other radiation effects, test structures provided might include:

a. FETS (Field oxide or Gate oxide)

b. P or N well isolation resistance

c. Device isolation (field leakage)

d. Propagation delay chains

e. Lateral NPN, PNP device leakage

f. Beta degradation

g. Base-collector leakage

h. Oxide isolation

8.4.1.6 Technology Additional special structures for a particular technology shall be used when appropriate (e.g., latch-up structures for CMOS).

8.4.2 Test Chips. Wafers in all development and production lots should include chips composed entirely of test structures to monitor the process and to serve as a surrogate for the CLSIC. The test chips that provide radiation hardness and reliability assessment data may be employed in wafer acceptance testing or in lot screening or acceptance testing. The test chips should include test structures to allow appropriate radiation evaluations of applicable features.

8.5 BUILT-IN TEST DESIGN

8.5.1 Functional Design. The functional design should be reviewed (see 3.7.1 in Appendix B) for the inclusion of suitable built-in test features, including use of the following:

a. Built-in test failure indicators

b. Handbook cells, circuits, or other structures, to implement built-in test

c. Modular, flexible, built-in test designs

d. Active stimulus injection for built-in test

e. Circuitry to check built-in test circuitry

8.5.2 Memory Allocation. The inclusion of test requirements should be assessed in the sizing of memory contained in the CLSIC (see 8.3.5 and Appendix B, 3.7.2).

8.5.2.1 Word Allocation. Sufficient words should be allocated in memory for the storage of microdiagnostics, initialization routines, and error processing routines (see 3.7.3 in Appendix B).

8.5.2.2 Bit Allocation. Sufficient number of bits should be assigned to each data word to provide for error detection and error correction technique, as required (see 3.7.4 in Appendix B).

8.5.2.3 Protection Allocation. A sufficient number of memory words should be assigned to nonalterable memory resources (e.g., ROM) to ensure the integrity of critical test routines and data (see 3.7.5 in Appendix B).

8.6 TESTABILITY ANALYSIS

An analysis should be conducted of the potential (intrinsic) testability of the logic-level design (see 3.8 in Appendix B). The analysis should address the functional design of test methods, the ability of the automatic test equipment to support the test methods, the presence or absence of circuit features which support testing, and any general problem areas. The fault coverage provided by each testing resource (built-in test structure, automatic test equipment, or other) should be analyzed in a quantitative manner. The analysis should be documented in the preliminary testability analysis report, and deficiencies should be corrected before proceeding.

Once the functional design process has been completed. a formal analysis of the CLSIC'S testability should be carried out. This analysis should include quantitative measurements appropriate to the functional level of the various testability figures of merit approved for the design. The ability of the proposed testing strategies and test equipment to achieve the required levels of testability should be determined. Any necessary design changes to meet the testability requirements should be identified. The results of this analysis should also be documented in the preliminary testability analysis report.

The testability analysis should be summarized in a final testability analysis report that would serve as a single source of information on all aspects of the testability of the CLSIC design, and should include the following:

a. A description of the overall design-for-testability features and testing strategies used

b. A description of the partitioning methods used to enhance testability and a functional description of each circuit partition

c. An analysis of the fault types considered and their effects on circuit operation

d. A detailed description of the testing strategies used for each circuit partition

e. A functional description of the built-in test features of the design

f. A listing and analysis of the measures or figures of merit used to evaluate the testability of the design

g. A functional description of the testability measurement techniques (e.g., computer-aided analysis tools) used in the testability analysis

8.7 DESIGN ASSURANCE

The detailed behavioral description or simulation (corresponding to the lowest level architectural description) should be used as a reference for validation or verification of all subsequent design simulations or implementations. During the functional design phase, an acceptable logical simulation should be performed to relate the logical design to this behavioral reference.

8.8 FUNCTIONAL DESIGN DATA BASE

The data base should contain the descriptions of the register-transfer and the logic designs, documentation of the logic design phase, and the set of design rules to be followed. The documentation of the logic design process should contain the rationale for the design decisions and the tradeoff analyses between potentially competing factors in the design. The use of handbook cells and regular circuit structures in the design should be documented. The initial state of the CLSIC should be indicated, and fault-tolerant features of the design should be described. The data base should also contain a specification of the semiconductor technology to be used and the design rules and constraints associated with both the technology and the specific fabrication line. Any changes of chip architecture to make the design compatible with respect to the semiconductor technology to be used should be documented. Information used for evaluation and validation should be included. This should consist of logic and fault simulation inputs and results, failure modes and fault populations to be used as a basis for testing, testability analysis, test vectors for built-in test structures or automatic test equipment, and the evaluation of their effectiveness (if fault simulation is appropriate at this time). A description of the test points and internal or external test circuitry to provide observability and controllability should be prepared.

8.9 TECHNICAL REVIEWS AND SURVEILLANCE

During the functional design phase, cognizant contractor engineering and CLSIC manufacturing personnel should visit or be resident at the designer’s facility to review the status of the design effort and to review future plans.

THIS PAGE INTENTI0NALLY LEFT BLANK

SECTION 9

PHYSICAL DESIGN PHASE

The physical design phase follows the functional phase of the technical program. It is concerned with the translation of the logic design into the actual circuit and mask designs that are to be implemented in hardware. This is usually accomplished in four well-defined and documented developmental stages representing description, synthesis, evaluation, and validation. Circuit simulation should be carried out in accordance with the requirements of this document. The accuracy of device models and circuit descriptions should be demonstrated and documented. The use of breadboarding and hardware fault simulation is encouraged, and both may be required. A plan for a comprehensive test program should be prepared for evaluation and approval. An integral part of this plan should describe the use of test structures or test circuits included with the physical implementation of the integrated circuit. Test vector generation, evaluation, and validation should be performed. Mask design also should go through the process of synthesis, description, evaluation, and validation. Final design validation and analyses of design testability and reliability of the circuit design should be prepared and submitted for review at the critical design review.

9.1 DESIGN REQUIREMENTS

9.1.1 Testability. During the physical design phase (see 3.9 in Appendix B), the following testability considerations should be included in the design:

a. The circuit is physically partitioned to support the test process.

b. Conservative timing tolerances and conservative signal tolerances are used in the design whenever possible.

c. Regular, structured, or hierarchical designs are used whenever possible.

d. Sufficient hardware, or firmware, is included to confidently drive the CLSIC to a known state or condition prior to running diagnostic tests.

9.1.2 Testability Analysis. On completion of the physical or circuit design phase, the contractor should conduct a final

analysis of the CLSIC's testability (see 3.10 in Appendix B). This analysis should include quantitative measurement. appropriate to the circuit level, of the various testability figures of merit approved for the design. Particular attention should be paid to circuit partitioning, signal timing. controllability, and observability.

9.1.3 Test Vector Validation. The contractor should validate the test stimuli and response data used in the design, as well as all associated testing software or firmware (see 3.11 in Appendix B). This validation would normally be accomplished by simulation of the design under faulty and fault-free condition. Hardware or software fault simulation may be used; the choice of method depends on the fault types under consideration, the fault coverage required, the availability of suitable fault simulation tools to the contractor, the cost of constructing the necessary simulation models, and the cost of conducting the simulation experiments. Sets of test vectors whose validity is known a priori need not be simulated. Examples of such tests include exhaustive test vector sets for combinational circuitry and proven test generation algorithms for specific circuit structures, such as the Galloping Pattern (GALPAT) algorithm for certain types of random access memory testing.

9.1.4 Circuit Models and Electrical Simulation. Descriptions of the circuit models employed and electrical circuit analyses of the CLSIC should be provided. These include:

a. Description of the models used to develop the analysis, along with a justification of the assumptions or an explanation of the perceived impact of these assumptions. All model parameters should be numerically defined, and all calculation and measurement techniques should be stipulated. Included in the phrase. "model parameters," are the parameters embedded in the subcircuit models which account for static and dynamic parasitic induced either by layout or limitations inherent in the fabrication process.

b. Range of model validity, e.g., voltage and current levels, dynamic signal amplitudes, slew rates and frequency, device geometry factors, doping levels, temperature, and frequency

c. Demonstration that the models are within their range of validity in the circuit simulations

d. Inclusion, for active integrated circuit elements, of the processing information after processing is completed (all vertical doping profiles, cross-section geometries, and surface geometries). Profiles can either be measured or can be the simulation results of a process simulator. Design fabrication parameters such as diffusion times, temperature, and ionization energies need not be supplied in order to avoid divulging proprietary information.

e. Computer simulations of the electrical characteristics for all active and passive circuit elements representative of those embedded in the actual design. Simulation results are to be compared with measured electrical properties of available test devices, and the test procedures for such measurements are to be clearly defined.

f. Typical critical path circuit simulations incorporating all exploited modeling routines. These simulations should include a sensitivity analysis to demonstrate fulfillment of all circuit specifications despite mathematical or engineering uncertainties in critical model parameters.

g. Simulation of circuit elements representative of those to be used in the actual design, along with a comparison of simulation results to measured test device performance

h. Experimental measurement of representative devices showing the effects of process variation on device performance

9.1.5 Evaluation of Layout at the Cell and Transistor Level. The various sections of the layout which implement the logic to be mechanized should be analyzed. This analysis should include:

a. Logic correctness

b. Electrical (transient and dc) characteristics

c. Drive capability (capacitive loading) computation

d. Rise and fall time computation

e. Propagation delays computation

f. Power requirement and heat dissipation

9.1.6 Circuit Simulation. The contractor should describe the extent to which circuit simulation is used in the design of the CLSIC, e.g., how critical paths are selected and analyzed. Analyses of worst case critical paths should be presented. Techniques for verifying the circuit level performance of the entire CLSIC (e.g., Speed, voltage, current, and power levels) should be discussed.

9.1.7 Layout Rules. A complete description of the design rules used should be provided. Those particularly critical for achieving maximum circuit performance and reliability should be indicated. The layout rules should include:

a. Device sizing and layout definitions

b. All minimum and maximum allowable dimensions

c. Definitions of each mask layer and specific rules

d. All shrink or expansion (correction factors) numbers for mask manufacturing

9.1.8 Radiation-Critical Layout Rules. The designer should identify the layout rules which are critical for each radiation environment. Examples of radiation-critical layout rules are:

a. The maximum current density for survival

b. The placement of guardbands in MOS devices for the total dose environment

c. The minimum allowed spacing between isolated components in bipolar circuits for the dose rate (latch=up) environment

d. The location of metallization runs in linear bipolar circuits for the total dose environment

These radiation-critical layout rules once established and identified should not be changed without contracting officer approval.

9.1.9 CAD Tools for Layout. The techniques used for layout of the CLSIC should be described. These may include, but are not limited to, full custom, symbolic, gate arrays,

semicustom, and macrocell. If digitizing is employed, the method used to check results should be described.

9.1.10 Circuit Parasitic. Circuit and device parasitic should be calculated for various tolerances in the layout design rules and parameters. These parasitic calculations should be included in the design data base.

9.1.11 Design Verification. The completed topological layout should be verified correct through the use of design rule checks and circuit simulation. These verifications should be performed on all areas of the circuit, either in part or as a whole circuit. Where the circuit is evaluated in sections, a verification should be performed to verify that the interconnections of the parts are correct. All design assurance checks should be documented.

9.1.12 Design Validation. The design should be validated to ensure equivalence of the final layout with the original design intent and that circuit layout is compatible with the system requirements.

9.1.13 Radiation Hardness Circuit Design Considerations. The designer should identify for each radiation environment the circuit design rules critical to the radiation response. Examples of such circuit design considerations are:

a. The forced beta and operating current of switching transistors in bipolar circuits for the neutron environment

b. Input protection networks for an electrical overstress environment

c. Photocurrent compensation diodes for a dose rate environment

These radiation-critical circuit design considerations, once established and identified, should not be changed unless approved by the contracting officer.

9.1.14 Other Requirements. Additional design information should be provided regarding:

a. A description of the package to be used, including a pin-out diagram, a bonding diagram which is sufficiently detailed to show bond angles, and a thermal analysis

b. A detailed test plan to be employed during characterization of the CLSIC

c. Input protection used on the CLSIC

d. An estimate of the total power consumed by the CLSIC, including worst case voltage drops and current densities in on-chip power and ground distribution lines

e. A description of the data base used in the design of the CLSIC and its contents, e.g., design file, geometry file, simulation file, cell parameters, cell libraries, and others

9.2 TECHNICAL REVIEWS AND SURVEILLANCE

During the physical design phase, cognizant contractor engineering and CLSIC manufacturing personnel should visit or be resident at the facility to review the status of the effort and to approve future effort.

SECTION 10

DETAILED SPECIFICATIONS

This section contains the requirements for the detailed specification needed to define an individual CLSIC for procurement. The preliminary development specification for the CLSIC should be prepared and submitted so that it can be reviewed and approved by the contracting officer no later than the Preliminary Design Review. The final specification should be prepared and submitted so that it can be reviewed and approved by the contracting officer no later than the Critical Design Review.

10.1 SUBCONTRACT OR PURCHASE ORDER

Procurement of a specific CLSIC for space vehicle application from another supplier is based upon the contractor preparing a subcontract or a purchase order that would reference the detailed specification for the specific CLSIC. In addition to referencing the applicable detailed specification, the subcontract or purchase order should also state:

a. Quantity of CLSICs being ordered

b. Delivery schedule

c. Delivery of data requiring contracting officer approval prior to proceeding, such as plans and audits

d. Delivery of data, such as test results and x-ray negatives with each device

e. Criteria for acceptance or for disapproval of each lot

f. Provisions for independent monitoring and the authority of the monitors to grant deviations or waivers

10.2 DETAILED SPECIFICATION FOR A CLSIC

Depending upon the contractor practices, or the specific contract, the detailed specification may be called a specification control drawing, a source control drawing, or some other name. In any case, it should address all of the technical requirements needed to procure the CLSIC. Regardless of the

actual document name, it should be prepared in a book form specification format. The requirement section (Section 3) should first incorporate the Specimen general requirements for CLSICs by referencing Appendix C of the handbook, or an equivalent general specification for LSIC, and then using a format similar to Appendix C, the needed new requirements and deviations required for the procurement of the specific CLSZC should be stated in each paragraph as appropriate. By arranging the detailed specification in the same format as the general specification. the manufacturers and others using the detailed specification can easily determine the total set of requirements for the specific CLSIC.

Note that many of the detailed requirements needed are not included in the specimen general specification, Appendix C. The additional items that should be included, or considered for inclusion, in the detailed specification of a specific CLSIC are:

a. Contractor part number (in Section 1, Scope)

b. Reference to the general specification (in Section 3, Requirements)

c. Any specific manufacturing requirements that may be applicable to ensure radiation hardness or other characteristics of the CLSIC. These could include specific process controls, test equipment, quality constraints, assembly requirements, or other specific manufacturing requirements (3.3 and subparagraphs).

d. Approved manufacturer and specific manufacturing processes and controls (3.3.1)

e. Wafer and production lot limitations, if any (3.3.2)

f. Electrostatic discharge sensitivity and handling requirements (3.3.3)

g. Independent surveillance and monitoring requirements (3.3.5)

h. Any specific design requirements that may be applicable to ensure radiation hardness or other characteristics of the CLSIC. These could include handbook cell constraints, test structures, test chips, probe pads, internal test failures, layout rules, levels of input protection required, or other specific design requirements (3.4, 3.5.1.3, and subparagraphs).

i. Approved designer and specific design rules and computer programs (3.4).

j. Die size (3.5.1).

k. Package material or specify whether the case is conductive or nonconductive. For metal cases, specify whether the case is connected to the ground lead or to any other part of the device (3.5.4).

l. Package configuration including lead designations and internal connections (3.5.4)

m. Functional requirements for the device including: CLSIC input signals, logic or schematic diagrams, operating conditions, limits, and outputs (3.6)

n. CLSIC supply power (voltages) and ground points (3.6)

o. Environmental conditions including thermal stress, mechanical shock, and radiation (3.7)

p. Special marking provisions (3.8)

q. Any specific quality assurance requirement that may be applicable to ensure radiation hardness or other characteristics of the CLSIC. These could include test methods, test facilities, test equipment, dosimetry measurements, and other specific quality assurance requirements (4 and subparagraphs).

r. Details of in-process inspections and tests including the use of test structures and test chips (4.3)

s. Wafer lot acceptance criteria including indicator parameters (4.3.3.1)

t. Details of preseal visual inspection criteria (4.3.3.6)

u. Special product evaluation or reliability assessments, tests, and characterization requirements (4.4)

v. Details of the post-assembly screening tests including: test methods, test circuitry, test

conditions, and the accept or reject values for the test parameters and for the delta limits. Any requirements for the reverse bias burn-in should be stated. The percent defective allowable (PDAs) for each test should be specified (4.5)

w. Deletion or modification of partial noise impact detection test based upon added design or added in-process test or inspection requirements to avoid particle problems (4.5.2)

x. Details of the lot conformance tests including: sample sizes, accept or reject quantities, test methods, test circuitry, test conditions, and the accept or reject values for the test parameters (4.6)

y. Specific requirements for radiation hardness lot conformance tests including: sample size, accept or reject quantities, test methods, test circuitry, test conditions, and the accept or reject values for the test parameters (4.6.4)

z. Packaging and package marking requirements (5)

SECTION 11

FABRICATION PHASE

The fabrication phase follows the physical design phase of the CLSIC development program. It encompasses mask and chip fabrication, assembly, in-process testing, validation, and the related issues of manufacturer capability and product assurance. During this phase, the design is transferred to the semiconductor material. The semiconductor technology and associated design rules and constraints employed in the physical implementation should be consistent with those employed in the earlier design phases and the capability audit. After the initial masking and fabrication of the CLSIC, the first task should be to test and validate the physical embodiment of the design to ensure correct implementation. The chip validation should be referenced to the same behavioral simulation utilized in the design and test generation stages. All fabrication should be carried out in accordance with the product assurance provisions of this document and the program plan.

11.1 PRODUCTION PHASE SURVEILLANCE

During the production phase, the contractor should have technical or inspection personnel perform independent surveillance and monitoring functions related to the fabrication, assembly, inspection, testing, and shipment of each lot of CLSICs. As a minimum, the contractor surveillance personnel should perform the following tasks:

a. Verify that devices are fabricated and assembled in accordance with an approved manufacturing baseline which conforms to applicable manufacturing flow charts, process specifications, tests and inspection procedure, and procurement documentation.

b. Conduct mandatory inspections at designated fabrication, assembly, and test steps as defined in customer approved manufacturing flow charts.

c. Witness wafer lot acceptance and SEM testing, and participate in review and analysis of test results and photographs.

d. Witness tests and inspection relative to software to be used for functional testing.

e. Perform preseal inspection of devices at designated points in the approved flow charts.

f. Provide surveillance of in-process die shear and bond strength tests.

g. Provide surveillance of functional test equipment and burn-in test equipment checkout.

h. Provide surveillance of tests required by the procurement documentation.

i. Provide surveillance of failure analysis activities and corrective actions resulting from the analysis.

j. Witness functional tests performed to ascertain use of proper procedures and to verify adequacy of results obtained.

k. Witness screening tests.

l. Audit data and documentation applicable to each lot of devices, and maintain information summary files.

m. Interpret or solicit contractor interpretation of applicable procurement requirements as required by the designer or manufacturer, and recommend specification changes if applicable.

n. Provide final lot inspection and authority for shipment of devices.

o. Provide written notification to the manufacturer, PMPCB, and contracting officer of any observed discrepancies.

11.2 RADIATION HARDNESS MANUFACTURING REQUIREMENTS

11.2.1 Critical Procedures and Processes During Wafer Fabrication. The manufacturer should identify and document, for each radiation environment, all fabrication, materials, and processes critical to the radiation response. Once these radiation-critical processes have been established and identified. they should not be changed during the course of a specific program unless approved by the contracting officer. Examples of radiation-critical processes are: the method, temperature, and pressure of oxide growth, and thickness of the gate oxide in MOS circuits for the total dose environment; post-gate oxide processing temperature profiles, process (epitaxial, gold doping, or neutron irradiation) used for

latch-up control in MOS devices; metallization process; and the base width and doping profile in bipolar transistors for the neutron environment.

11.2.2 Critical Procedures and Processes During Assembly. The manufacturer should identify and document all materials, procedures, and processes, critical to hardness, which are used during assembly, packaging, and handling of CLSICs (see Appendix A). Once these materials, procedures, and processes have been established and identified, they should not be changed during the course of a specific program unless approved by the contracting officer. The device response to total dose environment, for example, may be affected by such factors as the type and pressure of gas present inside the hermetically sealed package and the type and thickness of the packaging material (dose enhancement effects). For the X-ray environment, the die bond material. fly wire material, and bonding procedure are all critical for high-level pulsed ionizing radiation survivability.

11.2.3 Hardness Verification Analysis. The designer and manufacturer should perform and document a hardness verification analysis to ensure that the circuit design and processing technology being used to develop and produce the CLSICs is capable of meeting the hardness assurance requirements. This hardness verification analysis can be performed using radiation effects data on test devices, subcircuits, or library design cells (built with the proposed process) along with circuit analysis programs and basic radiation effects prediction techniques . The hardness verification analysis should be performed prior to committing a design or process to production. The analysis should demonstrate that the proposed design and process can achieve the required radiation design margin for each radiation environment (see Appendix A).

11.2.4 Radiation Test Procedure. Prior to the initiation of any radiation test, the supplier should generate a radiation test plan and detailed test procedures. The test procedures should state the details of the testing to be performed for each radiation environment including:

a. Method of test sample selection

b. Radiation test facility to be used

c. Dosimetry procedure

d. Equipment required and calibration procedures

e. Step by step test procedures including circuit diagrams, pre- and post-electrical tests, exposure levels, bias, and test conditions during exposure

f. Documentation of results

g. Data processing and analysis

11.2.5 Hardness Verification Testing. Before proceeding with the final design of devices that have a radiation environment specified, a hardness verification test using the variable sampling test method should be performed on test chips or subcircuits of the CLSIC device. A minimum of five devices should be tested in each radiation environment. These test devices should be tested to failure or 10 times the specification level, whichever is less, and the radiation failure levels of all tested devices should exceed the specification level for the CLSICs to be fabricated with the process. The supplier should use these data to determine when a redesign or change in construction or processing is necessary to meet the radiation requirements on the final product. The results of these tests should be recorded and be made available to the contracting office. Based on the hardness verification testing, the contractor may recategorize the part for the specific environments.

11.2.5.1 Radiation Facilities. The radiation test facilities should be approved by the contracting officer. A list of approved test facilities should be provided in the detailed specification.

11.2.5.2 Dosimetry. The dosimetry methods and procedures used by the supplier should be those published in the ASTM documents. If the appropriate dosimetry documentation is not available for a particular radiation test, then the dosimetry technique and procedures to be used should be included in the detailed specification.

11.3 PRODUCT EVALUATION

11.3.1 Characterization. Each CLSIC device type and applicable test chip should be characterized over the specified operating conditions including: temperature range, voltage range, Speed, and radiation environment. The resulting data should be used in developing the electrical, mechanical, and radiation test requirement for use in the detailed specification.

11.3.2 Reliability Assessment. Preliminary burn-in, preliminary life test data, and other stress test data such as electrical, thermal, and mechanical test data for each CLSIC device type should be obtained.

11.3.3 Test Coverage. Built-in and external testing should be used to ensure detection of errors at internal nodes. Functional tests should cover the full range of instruction, data ranges, speeds, voltages, and temperatures plus sufficient margins. as needed by system requirements. These tests should be included in the screening test requirements in the detailed specification.

11.4 RADIATION HARDNESS SCREENING TESTS

The manufacturer may be required to perform 100 percent radiation tests on the CLSICs for certain radiation environments either when the devices cannot pass a lot sample test but are still needed for the system or when there is a concern about mavericks. Examples where such a test might be required are: dose rate induced latch-up screening, dose rate upset screening, and total dose 100 percent irradiate and anneal screening on MOS devices. Radiation screening tests can only be used for those cases where nondamaging effects have been demonstrated and the screening tests are approved by the PMPCB. In those cases where a radiation screen is required, the test method and procedures should be provided in the detailed specification.

11.5 RADIATION HARDNESS FAILURE ANALYSIS

A radiation failure analysis is required on devices that fail the formal radiation product evaluation tests or the lot conformance tests. This failure analysis should be used to identify layout errors, processing problems, packaging problems, or other problem areas that contributed to the failure. Once the problem area is identified. the manufacturer should review the controls and procedures for that particular part of the design and processing and recommend solutions for assuring that the problem is eliminated. Details of the failure analysis requirements and procedures should be included in the detailed specification.

11.6 PRODUCT ACCEPTANCE CRITERIA

The acceptance of a production lot of CLSIC should be based on the product evaluation tests, the post-assembly screening tests, the life tests on the test chip evaluation samples, and the lot conformance (sample) testing. The tests used should be consistent with system requirements. The final acceptance criteria for CLSICs should be as stated in the detailed specification.

11.7 FINAL MANUFACTURING BASELINE

The final manufacturing baseline should reflect the manufacturing processes and designs used by the manufacturer to build the CLSIC. Subsequent changes in process or design require reapproval and updating of the manufacturing baseline. The manufacturer should submit changes proposed in the manufacturing baseline to the Parts, Materials, and Processes Control Board or contracting officer for approval prior to implementation.

SECTION 12

CONTRACTOR QUALITY ASSURANCE

12.1 INCOMING INSPECTION

Upon receipt of each lot of CLSICs, the contractor should perform applicable tests and inspections. As a minimum, the tests and inspections should include the following:

a. Performance of all tests and inspections included in the detailed specification as required to verify the acceptance test results

b. External inspection of all devices and device packaging to ascertain conformance to workmanship, marking, finish, packaging, and electrostatic protection requirements and to confirm absence of defects due to shipping and handling

c. A destructive physical analysis on a sample basis to be performed on each lot of CLSICs received. The minimum sample size should be 2.

12.2 FAILURE ANALYSIS

Failure analysis should be performed on catastrophic or other major failures experienced Subsequent to burn-in. Devices failing to survive a postburn-in electrical test or a subsequent test because of opens, shorts, inoperability, or logic error should be analyzed at the manufacturer's or contractor's facility to the extent necessary to ensure understanding of failure mode and cause. Failure analysis should also be performed on devices that fail the formal radiation product evaluation tests or the lot conformance tests. The failure analysis should be used to identify layout errors, processing problems, packaging problems, or other areas that contributed to the failure. The failure analysis reports should be provided to the contractor. A sufficient quantity of failed CLSICs occurring in any lot that fails any specified lot acceptance criterion (e.g., percent defective allowable, lot tolerance percent defective, or any acceptance number) should be analyzed to establish cause(s) of failure(s) and necessary corrective action to detect and correct out-of-control processes and to determine lot disposition. Appropriate corrective action should be implemented by the manufacturer. Failure analysis and

failure reporting requirements should be included in the procurement of the CLSIC device. All failures should be reported to the PMPCB and the contracting officer.

12.3 PROCEDURE FOR LOTS HELD MORE THAN 24 MONTHS

Each CLSIC held for a period exceeding 24 months following the date of the inspection lot identification code, and that is not installed in equipment, should be retested by the manufacturer or contractor for all specified functional and parametric test requirements prior to installation. CLSICs which fail any of these tests should be removed from the lot(s) and rejected. The devices should retain the original inspection lot identification code. Records of retesting should be maintained.

Custodian:
Air Force - 19

Preparing Activity:
Air Force - 19
Project # 1820-F010

APPENDIX A

RADIATION HARDNESS REQUIREMENTS

THIS PAGE INTENTIONALLY LEFT BLANK

CONTENTS

THIS PAGE INTENTIONALLY LEFT BLANK

APPENDIX A

RADIATION HARDNESS REQUIREMENTS

10. SCOPE

This appendix identifies requirement that should be incorporated into the detailed specification to specify radiation hardness for specific LSICs. It identifies types of environments and requirements for lot conformance testing for the acceptance of radiation hard LSICs. It provides methodology for establishing the lot acceptance criteria to meet specific hardness assurance requirements based on the system application and environments.

20. REFERENCED DOCUMENTS

DEFENSE NUCLEAR AGENCY

DNA 5910F	Piece Part Neutron Hardness Assurance Guidelines for Semiconductor Devices
DNA 5909F	Total Dose Hardness Assurance Guidelines for Semiconductor Devices

30. SYMBOLS

R_{SPEC} is the specified radiation environment level

R_{FA} is the environment failure level of a test device.

$\overline{\ln(R_{FAIL})}$ is the mean of the logarithms of the sample failure levels.

K is the one-sided tolerance limit for a normal distribution. It is a function of the confidence level, sample size, and survival probability (see Table A-I and Table A-II).

S_R is the standard deviation of the logarithms of the sample failure levels: $S_R = S_{\ln(R_{FAIL})}$

PAR_{FAIL} is the parameter or functional failure value for the device.

PAR_{RAD} is the radiation-induced parameter value for a given device.

$\overline{ln(PAR_{RAD})}$ is the mean of the logarithms of the values PAR_{RAD} for the tested devices.

S_P is the standard deviation in the sample values of $ln(PAR_{RAD})$; $S_P = S_{ln(PAR_{RAD})}$

n is the sample size.

C is the confidence level.

P is the survival probability.

RDM is the radiation design margin.

R_{MF} is the geometric mean radiation failure value.

PDM is the parameter design margin.

P_{MD} is the parameter mean value degradation.

40. ENVIRONMENTS AND PART CATEGORIES

40.1 Radiation Environments. The various types of radiation environments and the design levels are specified in the detailed specification. These radiation environments are derived from the free field environments as transported through the materials surrounding the LSIC for the worst case location and application. The types of radiation environments may include:

a. Neutron fluence (1 Mev equivalent) specified in neutrons per square centimeter, and the number of bursts

b. Total radiation dose specified in Gray(Si) and the dose rate specified in Gray(Si) per second

c. Transient ionization that may cause upset. latch-up, or burnout. State the peak dose rate in Gray(Si) per second and the transient pulse duration in seconds.

d. Particles that could cause a single event upset or latch-up. State the particle type, energy per square centimeter, and the angle of incidence. (State the acceptable number of upsets per gate, or device, per day.)

e. Current and voltage transient waveforms at each external pin during exposure to EMP and system generated EMP (SGEMP). Each transient waveform can be specified by an equivalent open circuit voltage pulse of specified magnitude, width, rise and fall time, and source impedance.

40.2 Radiation Hardness Categorization. For each type of radiation environment, there are three radiation hardness categories of interest, i.e., Hardness Critical Category 1, Hardness Critical Category 2, and a Hardness Noncritical Category. Devices that are in Hardness Critical Category 1 for a particular radiation environment have a lower radiation design margin in that environment than devices that are in Hardness Critical Category 2. Devices that are in the Hardness Noncritical Category for a particular radiation environment have the highest radiation design margin in that environment. Because of the low radiation design margin. radiation hardness lot conformance testing is required on every production lot for each environment where the devices are in Hardness Critical Category 1. To assure that the Hardness Critical Category 2 devices are in the correct category. radiation hardness lot conformance testing is required on the first production lot for each applicable environment. Because of the even higher radiation design margins for the Hardness Noncritical Category, typically 100 or higher, no radiation hardness lot conformance testing is required for those environments, except as might be required on the first production lot for device characterization.

In each application using CLSICs, one would like to select devices in the Hardness Noncritical Category and, if they are not available, then in the Hardness Critical Category 2. This is not only because of their higher radiation design margins and therefore lower failure risk in the operational environment, but because the radiation hardness lot conformance testing costs are usually less than for Hardness Critical Category 1 devices. Unfortunately, devices may not be available in either of these categories for the specified levels of all of the various types of radiation environments. For those radiation environments where the Hardness Critical Category 2 criteria cannot be met, devices would be Specified in the Hardness Critical Category 1. Of course, Hardness Critical Category 1 devices may be used whenever Hardness Noncritical Category devices or Hardness Critical Category 2 devices would not be practicable or cost-effective or would not be available when needed.

The radiation hardness categorization criteria are based on the radiation design margin, sample size, confidence level, required survival probability, and the standard deviation.

The radiation design margin depends upon the specified radiation environments as well as the radiation hardness characterization results for the LSIC. The categorization criteria in this document are based on a log normal failure distribution. In general, the categorization criteria should be based on a failure distribution that best fits the radiation test data. The standard deviation used in the categorization, S_R, must represent the variation between lots based on data or estimation of worst case value.

The radiation hardness categorization is therefore typically an integrative process for the LSIC because the location, and therefore the transported environment for the application, may change during the development, and the characterization for the LSIC may vary from prototype results to the results from initial production units.

40.2.1 Radiation Design Margin (RDM). The radiation design margin RDM is defined as

$$RDM = \frac{R_{MF}}{R_{SPEC}} \qquad (1)$$

where

$$R_{MF} = \exp\left[\overline{\ln(R_{FAIL})}\right] \qquad (2)$$

and

$$\overline{\ln(R_{FAIL})} = \frac{1}{n}\sum_{i=1}^{n} \ln(R_{FAIL_i}) \qquad (3)$$

where R_{FAIL_i} is the radiation failure level for the ith device.

40.2.2 Standard Deviation. The standard deviation, S_R, is defined for n greater than 1 as:

$$S_R = \left\{ \frac{1}{n-1} \sum_{i=1}^{n} \left[\ln(R_{FAIL_i}) - \overline{\ln(R_{FAIL})} \right]^2 \right\}^{1/2} \qquad (4)$$

40.2.3 Hardness Critical Category 1 Criterion. The criterion for Hardness Critical Category 1 for a particular type of radiation is that the radiation design margin (RDM) of the device in that radiation environment must be greater than

the minimum acceptable value specified (MIN), but not more than $\exp(K_{TL}S_R)$. i.e., the minimum radiation design margin for Hardness Critical Category 2.

$$MIN \leq RDM \leq \exp(K_{TL}S_R) \qquad (5)$$

Unless otherwise specified, the value of K_{TL} would be based upon a survival probability P equal to 0.999 and a confidence level C equal to 0.95 (see Table A-II). However, the minimum acceptable value, MIN, for the radiation design margin (RDM) for Hardness Critical Category 1 devices, if not specified, should be based upon a survival probability P equal to 0.999, a confidence level C equal to 0.95 (see Table A-II), and S_R which is equal to the minimum estimated $S_R(MIN)$. In that case, the value for MIN would be

$$MIN = \exp\left[K_{TL}(n,\ P = 0.999,\ C = 0.95)\ S_R(MIN)\right]$$

40.2.4 Hardness Critical Category 2 Criterion. Hardness Critical Category 2 devices have a radiation design margin (RDM) that equals or exceeds the upper limit specified for Hardness Critical Category 1 devices, but is less than the minimum radiation design margin specified for Hardness Noncritical Category devices (typically about 100). Therefore, the criterion for Hardness Critical Category 2 for a particular type of radiation is that the radiation design margin (RDM) of the device in a radiation environment must be greater than exp (K_T but less than 100 (or the value for Hardness Noncritical Category devices), i.e.,

$$100 > RDM > \exp(K_{TL}S_R) \qquad (6)$$

To assure that the devices are in the correct category, radiation hardness lot conformance testing is required on every item in the first production lot for each environment where the devices are in Hardness Critical Category 2. Because of the higher radiation design margin, radiation hardness lot conformance testing is not usually required on subsequent production lots of Hardness Critical Category 2 CLSICs.

40.2.5 Hardness Noncritical Category Criterion. Devices that have an extremely high radiation design margin, typically over 100, may be considered to be in a special Hardness Noncritical Category. This occurs when no radiation environment level is specified, or when the specified radiation environment level is small compared to the level that represents the inherent device tolerance to that type of radiation.

50. LOT CONFORMANCE TESTS

50.1 Test Requirements. Radiation lot conformance tests are specified in the detailed specification based upon the radiation hardness category classification of the LSIC for each type of radiation environment.

a. No radiation hardness lot conformance testing is required for LSICs that do not have a radiation environment specified.

b. LSICs in Hardness Critical Category 1 for a particular type of radiation environment require radiation hardness lot conformance testing of every production lot for that radiation type. In LSICs where the radiation response to the specified radiation environment is largely variable from one wafer to the next within a diffusion lot, the radiation hardness lot conformance testing is required for the devices fabricated from each wafer.

c. LSICs in Hardness Critical Category 2 for a particular type of radiation environment require radiation hardness lot conformance testing for that radiation type on the first production lot only. However, radiation hardness lot conformance testing may be required periodically thereafter if so specified in the detailed specification.

d. LSICs that are in a Hardness Noncritical Category for particular types of radiation environments do not require radiation hardness lot conformance testing for those radiation types.

Note that the LSIC may have different radiation hardness category classifications for each type of radiation. For example, it could be in Hardness Critical Category 1 for one type of radiation, in Hardness Critical Category 2 for another type of radiation, in a Hardness Noncritical Category for another type of radiation, and for another type of radiation no category can be identified because the actual radiation design margin might be less than the minimum specified for Hardness Critical Category 1.

50.2 Lot Conformance Testing Methods. For each radiation environment where radiation hardness lot conformance testing is required, a sample of the LSICs is tested as a

basis for acceptance of the production lot or as a basis for acceptance of devices from a single wafer. The radiation hardness of the sample is determined by testing parameter degradation to failure (the radiation to failure test of 50.3), or by testing at a single radiation level (50.4). Prior to testing at a single radiation level, it should be demonstrated that the specified parameter(s) degradation is a well-behaved function (monotonic) of the radiation environment over the specified range.

The lot acceptance criterion assumes a log normal failure distribution. In those cases where the distribution is shown to be other than log normal, the lot acceptance criterion should be determined by the appropriate type of distribution.

50.3 Radiation to Failure Test. This lot conformance test consists of exposing the sample of LSIC parts to increasing radiation levels until the radiation-induced parameter value, PAR_{RAD} for each part exceeds the specified end point electrical failure limit, PAR_{FAIL}. Following each radiation test level, the data are recorded (see Figure A-1).

From the data, the values of R_{FAIL} at PAR_{FAIL} are obtained. (The annealing effect should be considered when applicable.)

The lot is accepted when

$$RDM(Lot) \geq \exp(K_{TL}S_R) \qquad (7)$$

The values for RDM and S_R are obtained from Equations (1), (2), (3), and (4).

Note that Equation (7) is similar in form to Equation (6) with the exception that in Equation (7) RDM and SR are the values obtained for the lot.

If, in the course of categorization, the critical parameter does not reach the failure criterion at 10 times the specified radiation level, the categorization should be based on the parameter design margin at the specified radiation level (see Section 50.4).

50.4 Single Radiation Level Testing. When previous data have shown that radiation degradation of the electrical parameters over the specified range of radiation levels is well behaved (monotonic), then the lot conformance test can be conducted at a single radiation level, the specified level R_{SPEC}.

The lot acceptance is based on the parameter design margin, PDM, which is the ratio of the end point electrical parameter failure limit PAR_{FAIL} and the parametric mean value degradation P_{MD} following the radiation exposure (see Figure A-1).

The parameter mean value degradation P_{MD} is calculated from the radiation-induced parameter value PAR_{RAD} as follows:

$$\overline{\ln(PAR_{RAD})} = \frac{1}{n}\sum_{i=1}^{n}\ln(PAR_{RAD_i}) \qquad (8)$$

where PAR is the radiation-induced parameter value for the ith device

$$P_{MD} = \exp\left[\overline{\ln PAR_{RAD}}\right] \qquad (9)$$

The lot is acceptable if the design margin, DM, is greater than the exponential of the product K_{TL} and S_P for the lots.

(a) For parameter value increasing with radiation:

$$PDM = \frac{PAR_{FAIL}}{P_{MD}} \geq \exp(K_{TL}\, S_P) \qquad (10)$$

(b) For parameter value decreasing with radiation:

$$PDM = \frac{P_{MD}}{PAR_{FAIL}} \geq \exp(K_{TL}\, S_P) \qquad (11)$$

where

$$S_P = \left\{ \frac{1}{n-1}\sum_{i=1}^{n}\left[\ln(PAR_{RAD_i}) - \overline{\ln(PAR_{RAD})}\right]^2 \right\}^{1/2} \qquad (12)$$

50.5 Example 1. Lot acceptance, using the radiation to failure test for the radiation-induced change in input bias current, $\Delta I_$, for an LSIC. R_{SPEC} is 1.25 KGray(Si). ΔPAR_{FAIL} is taken to be 90 nanoamperes, n=6, C=95 percent, and P=99.9 percent.

Step 1: Irradiate the six test samples at increasing dose levels until all six devices have reached the ΔPAR_{FAI} value of 90 nanoamperes. Plot I versus total dose as shown in Figure A-2 for each device.

Step 2: Determine the total dose R_{FAIL} for each device at 90 nA from Figure A-2.

DEVICE	R_{FAIL} in KGray(Si)
1	15
2	13
3	19
4	11
5	17
6	10

Step 3: Determine from Equations (2) and (3)

$$\overline{\ln(R_{FAIL})} = \frac{1}{6}\sum_{1}^{6}\ln(R_{FAIL}) = 2.624$$

$$R_{MF} = e^{2.624} = 13.80 \text{ KGray(Si)}$$

$$RDM = \frac{R_{MF}}{R_{SPEC}} = \frac{13.80 \text{ KGray(Si)}}{1.25 \text{ KGray(Si)}} = 11$$

Determine the value S_R using Equation (4)

$$S_R = \left\{ \frac{1}{5}\left[(\ln 15 - 2.624)^2 + (\ln 13 - 2.624)^2 + (\ln 19 - 2.624)^2 + \right.\right.$$
$$\left.\left. + (\ln 11 - 2.624)^2 + (\ln 17 - 2.624)^2 + (\ln 10 - 2.624)^2 \right] \right\}$$

This gives S_R = 0.25

For n-6, c=95 percent, and P=99.9 percent;

K_{TL} from Table A-I is 6.612.

Using Equation (7) the lot is accepted when

$$RDM \geq \exp(K_{TL}\ S_R)$$

$$11 \geq \exp(6.612X0.25) = 5.22$$

Since RDM of 11 is larger than 5.22, this lot is acceptable.

50.6 Example 2. Lot acceptance for LSIC using a single dose level. The following information is given: R_{SPEC} = 1.50 KGray(Si), n=5, C=95 percent, P=99 percent, and PAR_{FAIL} = 15 milliamperes.

Step 1: Irradiate and measure PAR_{RAD} for the sample of five parts at R_{SPEC} = 1.5 KGray(Si). The following data are obtained.

Test Part	PAR_{RAD} in microsmperes
1	190
2	200
3	170
4	160
5	130

Step 2: Determine $\exp\left[\overline{\ln(PAR_{RAD})}\right]$ and S_P using Equations (8) and (12), respectively.

$$\overline{\ln(PAR_{RAD})} = \frac{1}{5}\left[\ln 190 + \ln 200 + \ln 170 + \ln 160 + \ln 130\right]$$

$$\overline{\ln(PAR_{RAD})} = \frac{1}{5}\left[\ln(190)(200)(170)(160)(130)\right] = \frac{25.615}{5} = 5.123$$

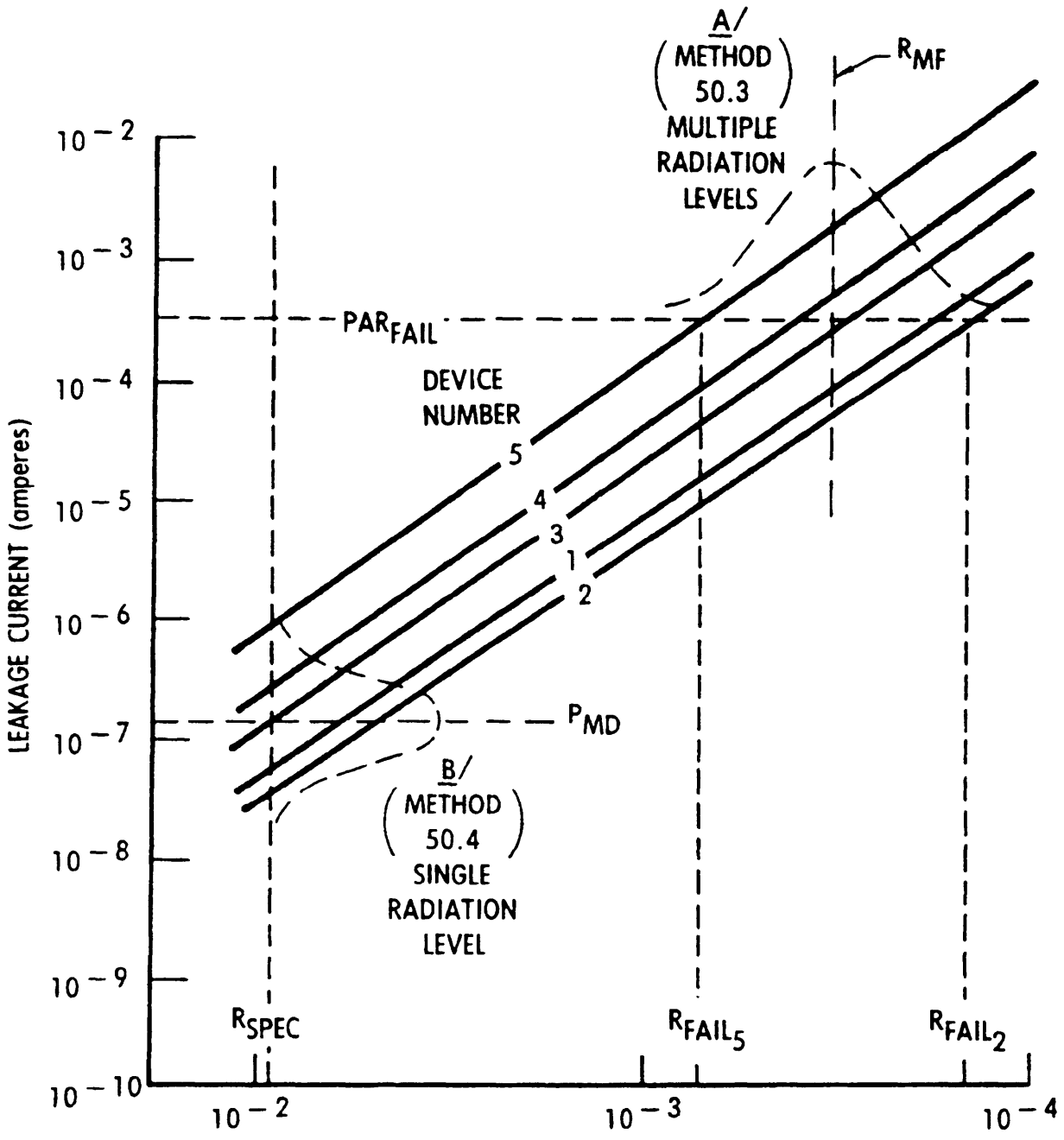
$$P_{MD} = \exp\left[\overline{\ln PAR_{RAD}}\right] = 167.8 \text{ microamperes}$$

$$S_P = 0.169$$

Step 3: Determine design margin for the lot which for increasing parameter value with radiation is equal to:

$$PDM = \frac{PAR_{FAIL}}{P_{MD}} = \frac{15mA}{0.167\ mA} = 89.3$$

From Table A-II for n=5, C=95 percent, and P=99 percent, K_{TL} is equal to 5.7; thus, $\exp(K_{TL}\, S_P)$ = 3.6. The parameter design margin is greater than 3.6 therefore this lot is acceptable.



Notes: A/ Method 50.3; Multiple radiation levels
B/ Method 50.4; Single radiation level

FIGURE A-1. Lot Conformance Tests

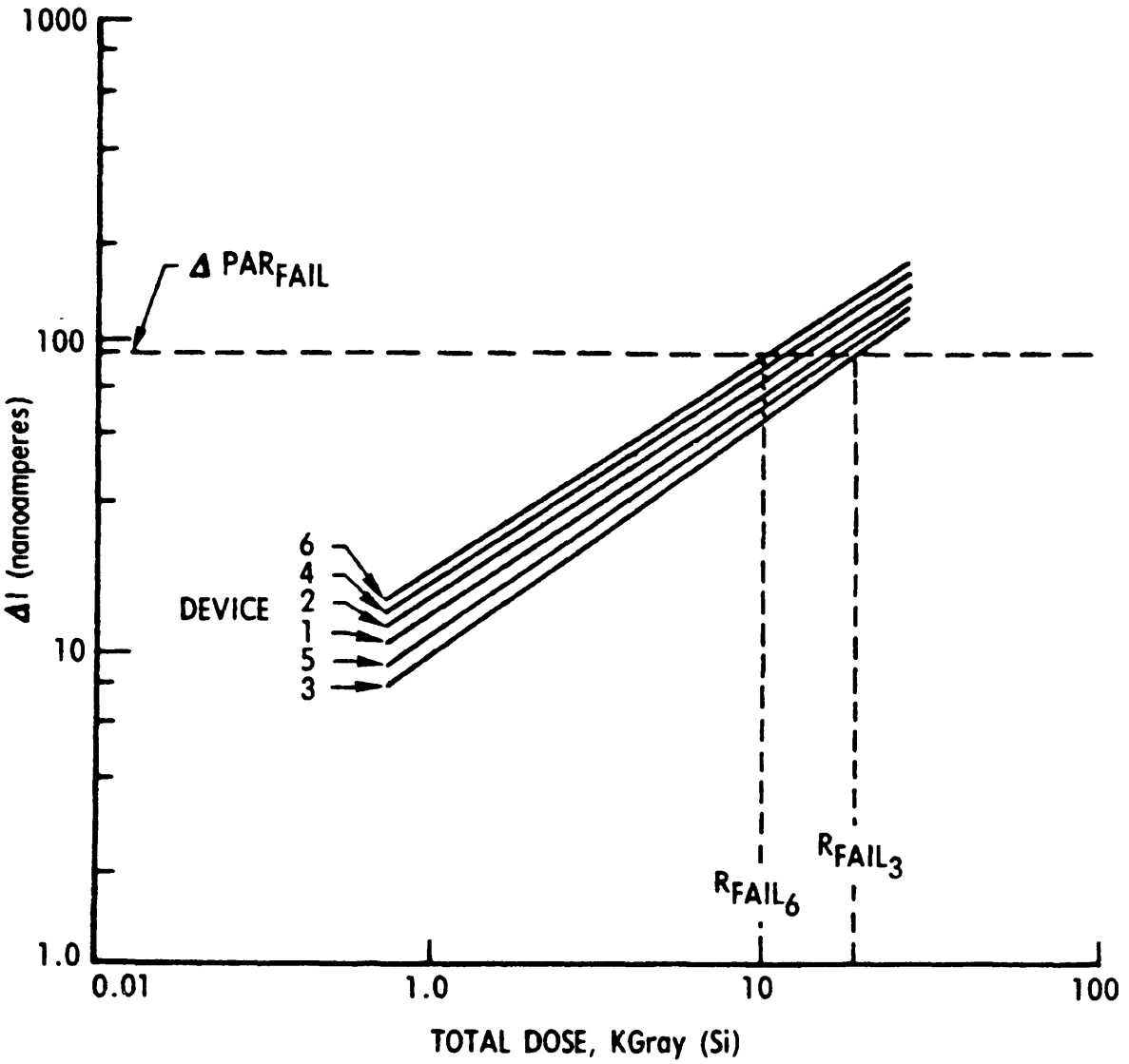


FIGURE A-2. Change in Leakage Current with Total Dose for Six Devices

TABLE A-I. K_{TL} Factors for One-Sided Tolerance Limits for Normal Distributions

	C = 0.75					C = 0.90				
n	p 0.75	p 0.90	p 0.95	p 0.99	p 0.999	p 0.75	p 0.90	p 0.95	p 0.99	p 0.999
3	1.464	2.501	3.152	4.396	5.805	2.602	4.258	5.310	7.340	9.651
4	1.256	2.134	2.680	3.726	4.910	1.972	3.187	3.957	5.437	7.128
5	1.152	1.961	2.463	3.421	4.507	1.698	2.742	3.400	4.666	6.112
6	1.087	1.860	2.336	3.243	4.273	1.540	2.494	3.091	4.242	5.556
7	1.043	1.791	2.250	3.126	4.118	1.435	2.333	2.894	3.972	5.201
8	1.010	1.740	2.190	3.042	4.008	1.360	2.219	2.755	3.783	4.955
9	0.984	1.702	2.141	2.977	3.924	1.302	2.133	2.649	3.641	4.772
10	0.964	1.671	2.103	2.927	3.858	1.257	2.065	2.568	3.532	4.629
11	0.947	1.646	2.073	2.885	3.804	1.219	2.012	2.503	3.444	4.515
12	0.933	1.624	2.048	2.851	3.760	1.188	1.966	2.448	3.371	4.420
13	0.919	1.606	2.026	2.822	3.722	1.162	1.928	2.403	3.310	4.341
14	0.909	1.591	2.007	2.796	3.690	1.139	1.895	2.363	3.257	4.274
15	0.899	1.577	1.991	2.776	3.661	1.119	1.866	2.329	3.212	4.215
16	0.891	1.566	1.977	2.756	3.637	1.101	1.842	2.299	3.172	4.164
17	0.883	1.554	1.964	2.739	3.615	1.085	1.820	2.272	3.136	4.118
18	0.876	1.544	1.951	2.723	3.595	1.071	1.800	2.249	3.106	4.078
19	0.870	1.536	1.942	2.710	3.577	1.058	1.781	2.228	3.078	4.041
20	0.865	1.528	1.933	2.697	3.561	1.046	1.765	2.208	3.052	4.009
21	0.859	1.520	1.923	2.686	3.545	1.035	1.750	2.190	3.028	3.979
22	0.854	1.514	1.916	2.675	3.532	1.025	1.736	2.174	3.007	3.952
23	0.849	1.508	1.907	2.665	3.520	1.016	1.724	2.159	2.987	3.927
24	0.845	1.502	1.901	2.656	3.509	1.007	1.712	2.145	2.969	3.904
25	0.842	1.496	1.895	2.647	3.497	0.999	1.702	2.132	2.952	3.882
30	0.825	1.475	1.869	2.613	3.454	0.966	1.657	2.080	2.884	3.794
35	0.812	1.458	1.849	2.588	3.421	0.942	1.623	2.041	2.833	3.730
40	0.803	1.445	1.834	2.568	3.395	0.923	1.598	2.010	2.793	3.679
45	0.795	1.435	1.821	2.552	3.375	0.908	1.577	1.986	2.762	3.638
50	0.788	1.426	1.811	2.538	3.358	0.894	1.560	1.965	2.735	3.604

TABLE A-II. K_{TL} Factors for One-Sided Tolerance Limits for Normal Distributions

	C = 0.95					C = 0.99				
n	P 0.75	P 0.90	P 0.95	P 0.99	P 0.999	P 0.75	P 0.90	P 0.95	P 0.99	P 0.999
3	3.804	6.158	7.655	10.552	13.857	--	--	--	--	--
4	2.619	4.163	5.145	7.042	9.215	--	--	--	--	--
5	2.149	3.407	4.202	5.741	7.501	--	--	--	--	--
6	1.895	3.006	3.707	5.062	6.612	2.849	4.408	5.409	7.334	9.550
7	1.732	2.755	3.399	4.641	6.061	2.490	3.856	4.730	6.411	8.348
8	1.617	2.582	3.188	4.353	5.686	2.252	3.496	4.287	5.811	7.566
9	1.532	2.454	3.031	4.143	5.414	2.085	3.242	3.971	5.389	7.014
10	1.465	2.355	2.911	3.981	5.203	1.954	3.048	3.739	5.075	6.603
11	1.411	2.275	2.815	3.852	5.036	1.854	2.897	3.557	4.828	6.284
12	1.366	2.210	2.736	3.747	4.900	1.771	2.773	3.410	4.633	6.032
13	1.329	2.155	2.670	3.659	4.787	1.702	2.677	3.290	4.472	5.826
14	1.296	2.108	2.614	3.585	4.690	1.645	2.592	3.189	4.336	5.651
15	1.268	2.068	2.566	3.520	4.607	1.596	2.521	3.102	4.224	5.507
16	1.242	2.032	2.523	3.463	4.534	1.553	2.458	3.028	4.124	5.374
17	1.220	2.001	2.486	3.415	4.471	1.514	2.405	2.962	4.038	5.268
18	1.200	1.974	2.453	3.370	4.415	1.481	2.357	2.906	3.961	5.167
19	1.183	1.949	2.423	3.331	4.364	1.450	2.315	2.855	3.893	5.078
20	1.167	1.926	2.396	3.295	4.319	1.424	2.275	2.807	3.832	5.003
21	1.152	1.905	2.371	3.262	4.276	1.397	2.241	2.768	3.776	4.932
22	1.138	1.887	2.350	3.233	4.238	1.376	2.208	2.729	3.727	4.866
23	1.126	1.869	2.329	3.206	4.204	1.355	2.179	2.693	3.680	4.806
24	1.114	1.853	2.309	3.181	4.171	1.336	2.154	2.663	3.638	4.755
25	1.103	1.838	2.292	3.158	4.143	1.319	2.129	2.632	3.601	4.706

0887b/0185b

THIS PAGE INTENTIONALLY LEFT BLANK

APPENDIX B

TESTABILITY GUIDELINES FOR CUSTOM LARGE SCALE INTEGRATED CIRCUITS FOR USE IN SPACE VEHICLES

THIS PAGE INTENTIONALLY LEFT BLANK

CONTENTS

CONTENTS (continued)

CONTENTS (continued)

THIS PAGE INTENTIONALLY LEFT BLANK

SECTION 1

SCOPE

This appendix summarizes the main concepts in the design for testability of custom large scale integrated circuits (CLSICs) and concepts evolved in testing for physical faults in actual hardware. Section 2 of this appendix points out the important problems and issues which should be considered in designing a testable CLSIC, including test structures and design style, test strategies, test strategy measures, and testable design methodologies.

Section 3 of this Appendix elaborates on various sections in the handbook to provide additional guidance and clarification. The corresponding paragraph numbers for the handbook are shown in parentheses for the convenience of the reader. Although this information may be helpful, it is not intended to be an in-depth analysis of each subject. More extensive information is available in the literature.

THIS PAGE INTENTIONALLY LEFT BLANK

SECTION 2

DESIGN OF TESTABLE CUSTOM LARGE SCALE INTEGRATED CIRCUITS

This section reviews some of the major concepts related to the design of a testable CLSIC. The partitioning of a CLSIC into testable circuit structures, the basic criteria and techniques used in testing. and the addition of built-in test features to facilitate testing are discussed. Built-in test features for CLSICs include the built-in test circuitry, other special built-in test structures, and the embedded firmware and software used to implement built-in testing. For example, built-in test features may include on-chip functional circuit structures such as signature generators, comparators. parity trees, counters, encoders, and decoders or they may be nonfunctional such as structures used for process monitoring or to enable external testing. Nonfunctional built-in test structures are usually process peculiar and will not be discussed in any detail.

A testable circuit structure refers to a logical organization or architecture of a CLSIC subcircuit which consists of the functional circuitry to be tested, called the kernel, and associated built-in test circuitry. Built-in test circuitry consists of additional circuitry, peripheral to the functional nature of the CLSIC, which is added to the chip specifically to aid in testing the functional circuitry. The built-in test circuitry may itself be functional in nature. Examples of testable circuit structures are level sensitive scan designs (LSSD), built-in logic block observation designs (BILBO), and syndrome testable designs.

2.1 STRUCTURES AND DESIGN STYLES

There are four fundamental units of logic circuitry that are used to implement digital systems, namely busses, random access memories, registers, and combinational logic. These fundamental logic units are referred to as basic circuit structures. The simplest case of a bus is a wire, of a random access memory is a one-bit storage element, of a register is a latch or flip-flop, and of a combinational logic circuit is a gate. More complicated circuitry. such as decoders and multiplexer, are also often implemented as basic structures. The interconnection of two or more of these basic structures (either different or identical units) results in a circuit structure. The difference between a basic circuit structure and a circuit structure is rather subtle. Arithmetic logic units, counters, and shift registers are examples of simple circuit structures. Circuit structures often have design styles associated with them, such as pipeline, bus-oriented, or bit-sliced.

There are numerous ways of implementing a basic structure in a single silicon chip. They differ in circuit design considerations such as: (a) how transistors are constructed, (b) how transistors are interconnected to form logic functions, (c) how logic functions are interconnected, and (d) what technology is used. Variations in circuit design and logic function lead to different design styles. such as read only memories (ROM), programmable logic arrays (PLA), and gate combinational networks, e.g., a NAND gate network. Hence, the use of a basic structure often defines a circuit's design style. For example, a combinational logic basic structure implementing some Boolean function, such as an arithmetic logic unit, may have as a design style read only memory, programmable logic array, or gate combinational network.

The importance of identifying design styles is that different design styles can lead to unique failure mechanisms; hence, the corresponding basic structures are often tested differently. This is often not true when exhaustive testing is employed, in which case the design style is usually ignored.

As an example, consider the programmable logic array design style. Because of the high fan-in often found in the AND array, programmable logic arrays are usually not tested very completely by random test vectors. Also, programmable logic arrays are susceptible to unique failure mechanisms, such as extra or missing crosspoint connections. Hence, a test methodology for a programmable logic array may be quite different from that for a read only memory or gate combinational network.

Often circuit structures are specially designed to enhance testability, such as in the level sensitive scan design methodology. In this case, a combinational logic basic structure C and a shift register structure S are interconnected to enhance the testing of C, which normally has the design style of a gate combinational network. The architecture consisting of the combination of the level sensitive scan register connected to C is said to constitute the level sensitive scan design testable structural style; the combinational logic network C which is to be tested is the kernel of the style.

In general, a CLSIC can be partitioned into functional blocks , such as control, input/output, arithmetic logic unit, and memory. For testing purposes, a CLSIC can also be partitioned into "testable" subcircuits. each subcircuit being tested in its own unique ways. These subcircuits may, but not necessarily. correspond to functional blocks. By definition, they are circuit structures. Often, one of the first steps to be taken in the design of a testable CLSIC is to partition it into subcircuits. The subcircuits in turn define circuit structures whose fault characteristics are well defined and for which one or more

testing strategies are known. Each such structure may be modified by the inclusion of specified built-in test circuitry in order to enhance its testability. The subcircuits so defined by the partition process need not be disjoint; in fact, they often have built-in test circuits in common.

A maximal basic circuit structure is a basic structure not contained within a larger basic structure. Often a chip is tested by identifying maximal basic circuit structures and testing them individually. If a circuit structure is not too complex, such as a counter, it can be tested as an entity. For complex circuit structures, such as a microprocessor, testing it as one entity becomes extremely complex.

2.2 TESTING TAXONOMY

The design of a reliable CLSIC includes two major concepts; namely. fault tolerance and testing

2.2.1 Fault Tolerance. Three major topics fall under this heading: software techniques, hardware techniques, and analysis tools. Some specific techniques in each of these areas are listed.

a. Software techniques
- Rollback
- Error recovery
- Exception handling
- Fail Safe design

b. Hardware Techniques
- Coding
- Duplication and comparison (duplex design)
- Triple modular redundancy
  - static
  - dynamic
- Hybrid redundance

c. Analysis tools
- Reliability measures
- Reliability models
- Yield
- Chip area estimation
- Availability
- Performance

2.2.2 Testing. The process of testing a circuit structure in order to detect or locate hardware faults can be carried out in one of two modes, known as external testing and self testing. The former deals with the use of automatic test equipment to test

the circuit structure; the latter relies on the chip itself to carry out the testing process. A circuit structure is often tested using precomputed test programs which are created via the process of test program generation. Two major aspects of testing, therefore, are test program generation and design for testability.

2.2.2.1 Test Program Generation. The major concepts related to test program generation are: fault modeling, test generation, response evaluation, fault simulation, and fault location.

2.2.2.1.1 Fault Modeling. Fault modeling deals with the process of representing the actual physical faults in the circuit (structure) under test by some type of abstract model. It is these modeled faults which are actually processed by most test synthesis and analysis tools. Examples of commonly used fault models are listed below:

a. Single stuck-at faults
b. Multiple stuck-at faults
c. Shorts and bridging faults
d. Functional faults
e. Coupling faults
f. Pattern sensitive faults
g. Delay faults
h. Parametric faults
i. Nonclassical MOS faults. such as opens

2.2.2.1.2 Test Generation. Tests for a circuit can be determined in several ways. The most common are listed below:

a. Manual
b. Algorithmic
c. Pseudorandom
d. Exhaustive
e. Standard test patterns

The method used to generate the test must be compatible with the level of description available for the circuit structure under consideration. For example, employing a path sensitization algorithm may require a gate level description of a circuit structure; employing a test generation algorithm for programmable logic arrays may require only the truth table of the functions being implemented; employing a functional/behavioral approach may require a high level language description of the circuit structure, such as the Instruction Set Processor (ISP) notation.

2.2.2.1.3 Response Evaluation. Once tests are generated they can be translated into a test program which can then be applied either by the automatic test equipment or by built-in test features to the circuit under test. Based upon the response measured, the circuit under test can be characterized as being faulty or not. If it is faulty, diagnosis or fault location can be carried out. Methods for processing the response are listed below:

a. Direct comparison
   - Stored response
   - Gold unit (standard hardware)

b. Comparison with data compression (compact testing)
   - Transition counting
   - One's counting or syndrome testing
   - Signature analysis

2.2.2.1.4 Fault Simulation. Normally, the fault coverage of a test can be determined by using a fault simulator. Fault simulation can be carried out either in software or in hardware.

2.2.2.1.5 Fault Location. Fault location can be carried out by using either fault dictionaries, diagnostic routines, or effect-cause analysis.

2.2.2.2 Design for Testability. Design for testability is carried out for several reasons, such as to reduce the complexity of test generation and to make the chip partially or fully self testable. The complexity of test generation may be reduced by enhancing controllability and observability. The chip may be made partially or fully self testable by employing built–in test structures or other built-in test features. The major concepts in this field fall into ad hoc design methods, structural built-in test methods, designing with easily testable components. and analysis tools.

2.2.2.2.1 Ad Hoc Design Methods

a. Degating
b. Adding test points
c. Bus architecture
d. Partitioning
e. Self-comparison
f. Self-oscillation

2.2.2.2.2 Structured Built-in Test Methods

a. Semi built-in
   - Level sensitive scan design
   - Scan path
   - Random-access scan
   - Scan/set logic
   - Partitioning

b. Fully built-in
   - On-line
     - Error detection and correction codes
     - Totally self-checking circuits
     - Self-verification
   - Off-line
     - BILBO
     - Store and generate
     - Verifying Walsh coefficients
     - Autonomous testing
     - Syndrome testing

2.2.2.2.3. Disigning with Easily Testable Components

a. EOR trees
b. Canonic Reed-Muller circuits
c. Easily testable programmable logic arrays
d. Easily testable iterative logic arrays
e. Bit-slice systems

2.2.2.2.4 Analysis Tools

a. Measurements
   - COMET
   - SCOAP
   - TMEAS
   - CAMELOT

b. Design: Automatic design for testability

Numerous ad hoc designs for testability techniques have evolved over the years. Most have dealt with small scale or medium scale integrated circuits on printed circuit boards. Included in these techniques are concepts such as resetable flip-flops, test points to increase observability, logical cutting of feedback lines, and inhibiting internal clocks. Extensions to these early techniques have led to many of the built-in test methods currently used extensively in VLSI circuits.

Semi built-in test methods employ hardware structures, such as set/scan registers, to increase controllability and observability. Off-line test generation is usually still required.

The on-line fully built-in test methods are examples of concurrent testing. The off-line testing methods, such as built-in logic block observation, are gaining in popularity. These methods eliminate the need for off-line test generation and minimize the need for automatic test equipment. These techniques often require minor or no changes to the kernel structure being tested.

Designing with easily testable components is a methodology which deals primarily with the design of the kernel itself, and where the main objective is to make the kernel easy to test. A simple example would be those techniques which rely heavily on the use of exclusive-or gates. For such gates, a single error on an input always produces an output error, making the concept of path sensitization particularly easy to achieve.

Finally, several analysis tools have been proposed for aiding design for testability. These analysis tools usually estimate the degree of controllability and observability of the various signal lines in a circuit. Based on these results, the circuit design should be modified, if necessary, in order to enhance testability.

2.2.3 Structure and Testing. Four important factors to be considered in testing a kernel are:

a. Fault modes

b. Whether or not a single vector or a sequence of vectors are required to detect a fault

c. Complexity of test generation

d. Timing

The structure of a kernel and its design style are the primary factors which influence these factors.

Fault modes are often a function of design style. Random access memories exhibit the phenomenon of adjacent pattern interference: programmable logic arrays are susceptible to crosspoint failures (extra or missing connections); gate combinational networks are often tested for stuck-at faults, shorts, and sometimes memory retention.

For a combinational circuit, only one vector is usually required to detect a fault, while for sequential circuits a sequence of test vectors is often necessary. Faults in combinational circuits which induce memory retention may require a sequence of two vectors to detect.

The complexity of test generation is strongly related to design style as well as circuit structure. For random access memories, standard test sequences usually exist. Automatic test generation is usually a difficult if not impossible task for complex random sequential circuits. For programmable logic arrays, special algorithms exist which make test generation a fairly effective and efficient process.

Finally, timing issues related to factors such as races, hazards, and static and dynamic logic are a function of both design style and circuit structure. For example, asynchronous circuits are circuit structures and are susceptible to races. A random access memory design style may be susceptible to pattern interference faults which are both timing and data sensitive.

In summary, different design styles and circuit structures have unique testing characteristics and are thus amenable to unique testing approaches and built-in test strategies. As an example. a programmable logic array can be built such that the signal values on the row (product) and column (word) lines have odd parity; this concept is not directly applicable to a gate combinational network implementation of the same functions. A unique logic structure for the testing of internal arrays, and the testing for pattern sensitive faults in read only memories are discussed in the literature.

2.3 TEST STRATEGIES

A test strategy for a kernel structure is the complete process involved in testing the structure. This includes the following three main attributes:

a. Off-line test generation

b. Run-time test hardware
   - Automatic test equipment (external)
   - Built-in test (internal)

c. Test accessibility
   - Controllability
   - Observability

2.3.1 Off-Line Test Generation. Off-line test generation is the method used to derive test vectors and sequences. This process is necessary for some types of test strategies, e.g., in

the level sensitive scan design (LSSD) methodology, but not for others, e.g., when a circuit is tested using the built-in logic block observation (BILBO) methodology. There are several ways to carry out off-line test generation. some of which are summarized below:

a Manual

Circuit-oriented, e.g., process sensitized paths

Functional, e.g., execute every instruction

b. Algorithmic/heuristic

PODEM

D-algorithm

Programmable logic array test generation

Delay test generation

LASAR (D-LASAR, LASAR 5.6)

Functional

c. Pseudo-random

d. Exhaustive (not normally done off-line)

e. Standard test sets

GALPAT for random access memories

Universal test sets for programmable logic arrays

Except for exhaustive and standard test sets, tests once generated are usually processed through a fault simulator to determine fault coverage.

It is seen that the process of off-line test generation can involve the overhead of a complex and sophisticated suite of software modules, including design capture. testability analysis, test generation. and fault simulation routines. The resulting tests are often processed via additional software to create a fault dictionary, if required, and via a translator in order to obtain a test program that runs on a specified piece of automatic test equipment.

2.3.2 Run-Time Test Hardware. Run-time test hardware is that hardware used during the actual testing process of the structure. This hardware is used to produce the test vectors required to test the circuit structure as well as process the responses obtained. Table B-I summarizes some of the hardware used in this process. There are two main categories of hardware used; namely, external automatic test equipment and internal built-in test circuitry.

TABLE B-I. Run-Time Test Hardware

- Off-chip automatic test equipment
- On-chip built-in test circuitry
  - Generation of test stimuli
    - Built-in logic block observation register
    - Linear feedback shift register
    - Counter (exhaustive testing)
    - Read only memory (stored test patterns)
    - General sequential circuit
    - Gray code generator
  - Processing of test responses
    - Signature generator
    - Built-in logic block observation register
    - Syndrome generator/one's counter
    - Transition counter
    - Comparator
    - Random access memory (store responses)
    - Parity detector
    - Single error correction-double error detection
    - General sequential circuit

2.3.3 Test Accessibility. During the testing process, one needs a hardware mechanism in order to actually apply the test vectors to the inputs of the kernel structure under test, as well as observe the response data produced at the outputs of this structure. Since this structure is often deeply buried within a chip, built-in test features are often added to the circuit to implement these controllability and observability functions. Table B-II indicates some examples of how that accessibility is achieved.

TABLE B-II. Test Accessibility

o Input Primary inputs Scan-in registers Level sensitive scan design registers Built-in logic block observation register Multiplexers o Output Primary outputs/test points Scan-out registers Level sensitive scan design registers Built-in logic block observation registers Multiplexers

In some cases, such as with a built-in logic block observation register, the run-time test hardware and the test accessibility registers are one and the same. For the level sensitive scan design methodology, this is not the case. Tests are first generated off-line, usually using some type of test algorithm; external hardware (automatic test equipment) is then used at test run time to generate and process the tests; level sensitive scan design registers are then used only to achieve input and output access to the structure under test.

In summary, a test strategy involves three key concepts; namely, a means for generating input test data. the hardware required to produce the test vectors and process responses during the testing cycle, and finally a means for applying the input test data to the input lines and observing the response data at the output lines of the circuit structure under test.

2.4 TEST STRATEGY MEASURES

Numerous test strategies exist. With each test strategy, one can associate several measures dealing with performance criteria, constraint, and goals. An example of a performance criterion is the length of time it takes to test a circuit structure; an example of a constraint is that the input and output pin requirements for the built-in test circuitry be less than some given quantity; an example of a goal is that the test strategy achieve at least 98 percent fault coverage of the single detectable stuck-at faults.

The three concepts of performance, constraints, and goals have been lumped together because they are usually highly interrelated, and often tradeoffs are made between them. For example, achieved fault coverage is often a function of the expense one is willing to incur in test generation. The incremental increase in fault coverage as a function of cost may be extremely high as one approaches 100 percent coverage. Also, for sequential circuits, the incremental increase in test length for each 1 percent additional fault coverage may become extremely large. Hence, all goals may not be feasible. Unfortunately, the quantitative prediction of performance measures is a difficult task. Hence, one cannot, for example, predict a priori the cost of test generation versus fault coverage for a given circuit.

Because of these dichotomies, the concepts of Performance constraints, and goals have been lumped into the general category of measures. In Table B-III, a few important measures are listed which may need to be considered in selecting a test strategy for a circuit structure.

The tradeoff between more area for built-in test circuitry and decreased chip functionality leads to a classic battle between chip designers and users. Hence, the driving force for using built-in test circuitry comes from design specifications where the testability and functionality of the chip are made equally important design criteria. One other concept not addressed in this report but which must also be given great consideration is design correctness; hence, design verification and validation are key issues.

Test application time is usually critical when expensive automatic test equipment is employed. When a chip is part of a large system, such as a space satellite which employs off-line self test procedures, testing time may be important because it may significantly affect the time the system is not available for normal use.

Performance degradation deals with the effect on a circuit’s operating characteristics during its functional operation due to built-in test hardware. For example, using a pair of level sensitive latches in a feedback path, as found in level sensitive scan designs. instead of some other form of flip-flop, may reduce the system clock rate by a small amount.

Preprocessing cost deals with the process of off-line test generation and the associated costs of acquiring and executing the required software.

Finally, the cost of processing engineering changes varies widely for different test strategies. When off-line test generation is employed, processing an engineering change can be quite costly.

TABLE B-III. Measures Associated with a Test Strategy

M1	Yield and area effect due to built-in test circuitry
	Example: o Level sensitive scan designs often requires a 5 to 20 percent area overhead
M2	Test Application Time
	Example: o In level sensitive scan designs, each test vector is shifted sequentially hence slowing down the test process
M3	Input and output pin demand
	Example: o Level sensitive scan designs require four additional pins
M4	Fault coverage and fault types
	Examples: o For level sensitive scan designs, coverage of the single stuck-at fault can be arbitrarily high and can be measured via fault simulation
	o For built-in logic block observation testing, coverage is difficult to determine
	o For autonomous testing, coverage is essentially complete for all fault modes
M5	Test input or output storage volume (on chips)
	Examples: o For microdiagnostics, test volume is high
	o For signature generation, volume is low
	o For level sensitive scan designs, no on-chip storage is required
M6	Performance degradation
M7	Preprocessing (off-line) costs
M8	Cost of off-line automatic test equipment
M9	Cost of accommodating engineering changes

2.5 TESTABLE DESIGN METHODOLOGY

The combination of (a) a kernel structure S and (b) a test strategy (test generation, run-time test hardware. and hardware for accessibility) constitutes a testable design methodology. If the structure S has a design style D, then it can be said that the testable design methodology is for design style D.

The general form for a testable design methodology is represented as follows:

A1. A kernel structure to be tested
(optional: A basic circuit structure and its design style)

A2. A test strategy
A2.1 An off-line test generation strategy
A2.2 A run time testing environment
A2.3 Hardware for test accessibility

2.5.1 Level Sensitive Scan Design(LSSD) Example of Testable Design Methodology. As an example, a level sensitive scan design is associated with a testable design methodology having the following attributes:

A1 Gate combinational network
A2.1 Test generation algorithm/fault simulator/translator
A2.2 Automatic test equipment
A2.3 Level sensitive scan design registers

Figure B-1 indicates the major components associated with the level sensitive scan design testable design methodology. In Figure B-2 a specific example of a testable circuit structure having a level sensitive scan design testable structural style is shown.

The space of testable design methodologies can be thought of as a multi-dimensional space having the following three main components:

a. The structure of the circuit to be tested and possibly its basic structure and design style

b. The test strategy selected to test the circuit

c. The value of the measures, such as M1 through M9, associated with the above two items

Given this space, some testable design methodology can be judged to be good, others to be poor. For example, replacing

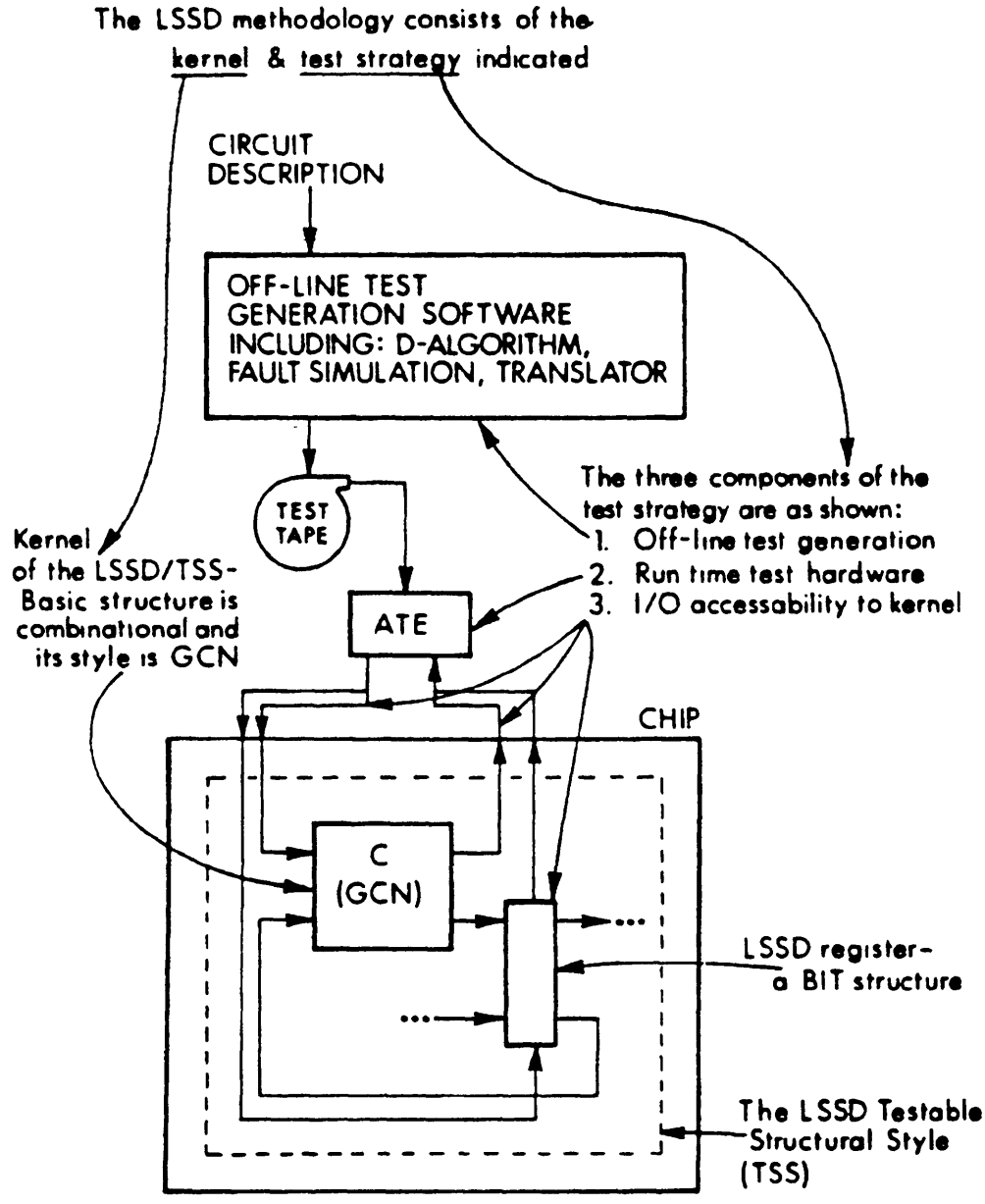


FIGURE B-1. The Level Sensitive Scan Design Testable Design Methodology

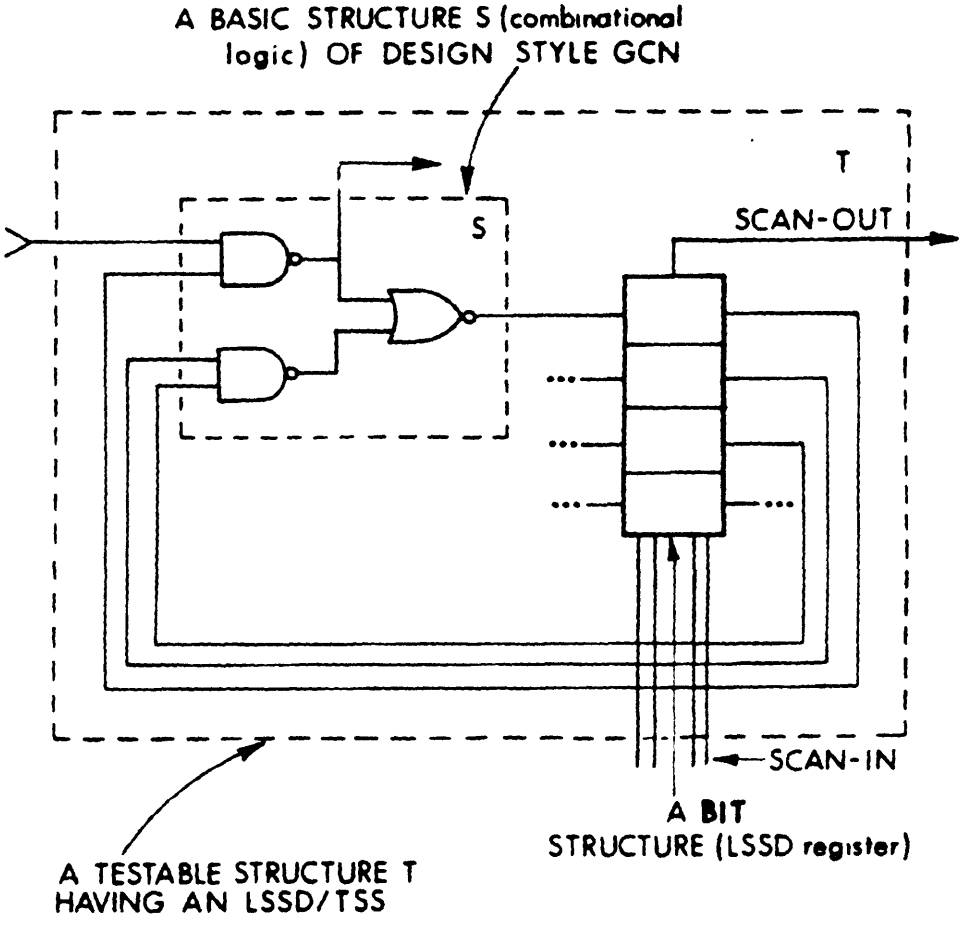


FIGURE B-2. A Testable Structure Having a Level Sensitive Scan Design Testable Structural Style

the gate combination network by a random access memory in the level sensitive scan design would not lead to a useful testable design methodology.

2.5.2 The Design Problem. The main tasks in designing a testable CLSIC chip can be stated as follows:

a. Partition a design into circuit structures. Depending on the testing strategy to be used. some or all of these structures may be basic circuit structures having well defined design styles.

b. Select an appropriate test strategy for each structure.

c. Modify the design as necessary to implement the selected testable design methodologies satisfying all measures associated with the chip.

2.6 CHIP BUILT-IN TEST CIRCUITRY

In making a chip testable, several standard hardware structures are often added to the chip in order to enhance its testability. Examples of such built-in test circuits are:

a. Set/scan registers, e.g., level sensitive scan design registers

b. Counters (generates 2^n test vectors)

c. Built-in logic block observation registers

d. Comparators

e. Linear feedback shift registers

f. Parity generators

Over the last several years, increased levels of observability and controllability in VLSI circuits have been obtained by replacing normal flip-flops in a circuit by dual mode registers which, in normal mode, act as normal flip-flops. In the test mode, they act as shift registers, enabling test vectors to be scanned into the circuit and test responses to be scanned out. To achieve exhaustive testing, counters can be added to a circuit so that all possible test patterns can be generated. To carry out ones or transition count testing, a count register can be used. Between these two extremes, one can employ linear feedback shift registers, such as in the built-in

logic block observation (BILBO) methodology, to either generate pseudorandom test vectors or to generate a signature. Finally, a comparator can be used to compare a generated signature with a stored correct signature. When these test circuits, as well as others, are used, powerful testable structural styles can be created.

Except for the parity generator, the test circuits listed previously are used for off-line testing. When on-line testing is used. then other built-in test circuits are employed. They are usually used to implement some coding or decoding scheme. Other examples of such test circuits are self-checking checkers.

2.7 EXAMPLES OF TESTABLE DESIGN METHODOLOGIES

This section briefly illustrates a few popular testable design methodologies.

2.7.1 Level Sensitive Scan Design (LSSD) Testable Design Methodology. Probably the most well known testable design methodology is the level sensitive scan design testable design methodology introduced by IBM. This methodology has been depicted in Figures B-1 and B-2.

2.7.2 Scan Path Testable Design Methodology. This methodology is similar to the level sensitive scan design testable design methodology. The main differences lie in the type of flip-flops used in the registers and the clocking scheme employed.

2.7.3 Scan-Set Testable Design Methodology. The scan-set testable structural style is shown in Figure B-3. Note that the kernel structure is now a sequential circuit; hence, the off-line test generation process for this methodology can be significantly more complex than that for the previous two methodologies. The register can either load data (observability) in parallel from test points in the kernel structure and shift these data out (scan-out), or else scan-in new data (controllability) and apply these data to test points in the kernel.

2.7.4 Random Access Scan Testable Design Methodology. The testable structural style for the random access scan testable design methodology is shown in Figure B-4. Again, off-line test generation is required along with automatic test equipment, and the kernel is combinational. For this testable structural style, the flip-flops in the original sequential circuits are made individually addressable during the testing mode, and their contents are set and read via the automatic test equipment. During the normal mode of operation, the kernel and flip-flops in the addressable storage array operate as a normal sequential circuit.

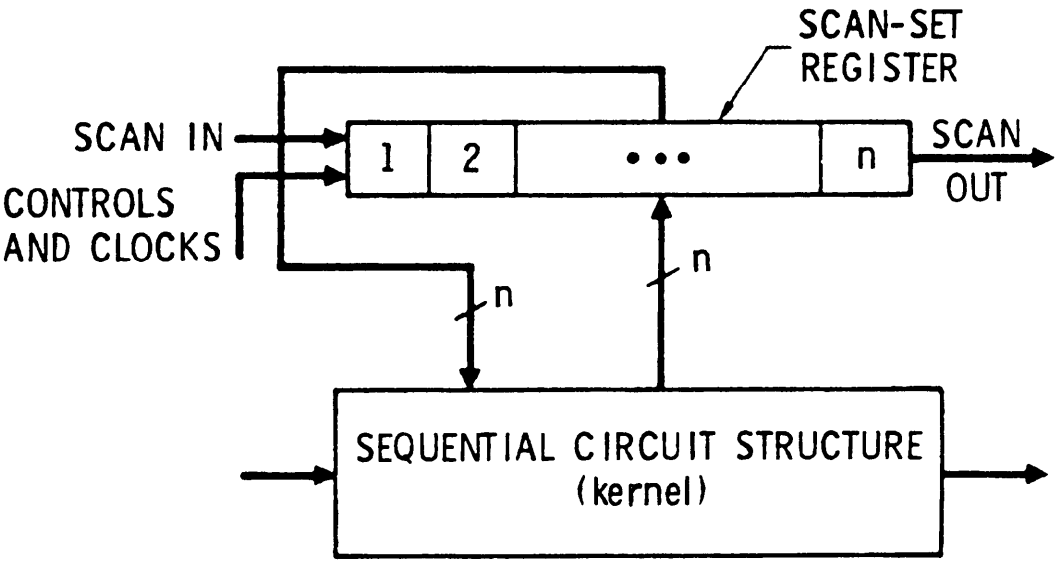


FIGURE B-3. The Testable Structural Style Used in the Scan-Set Testable Design Methodology

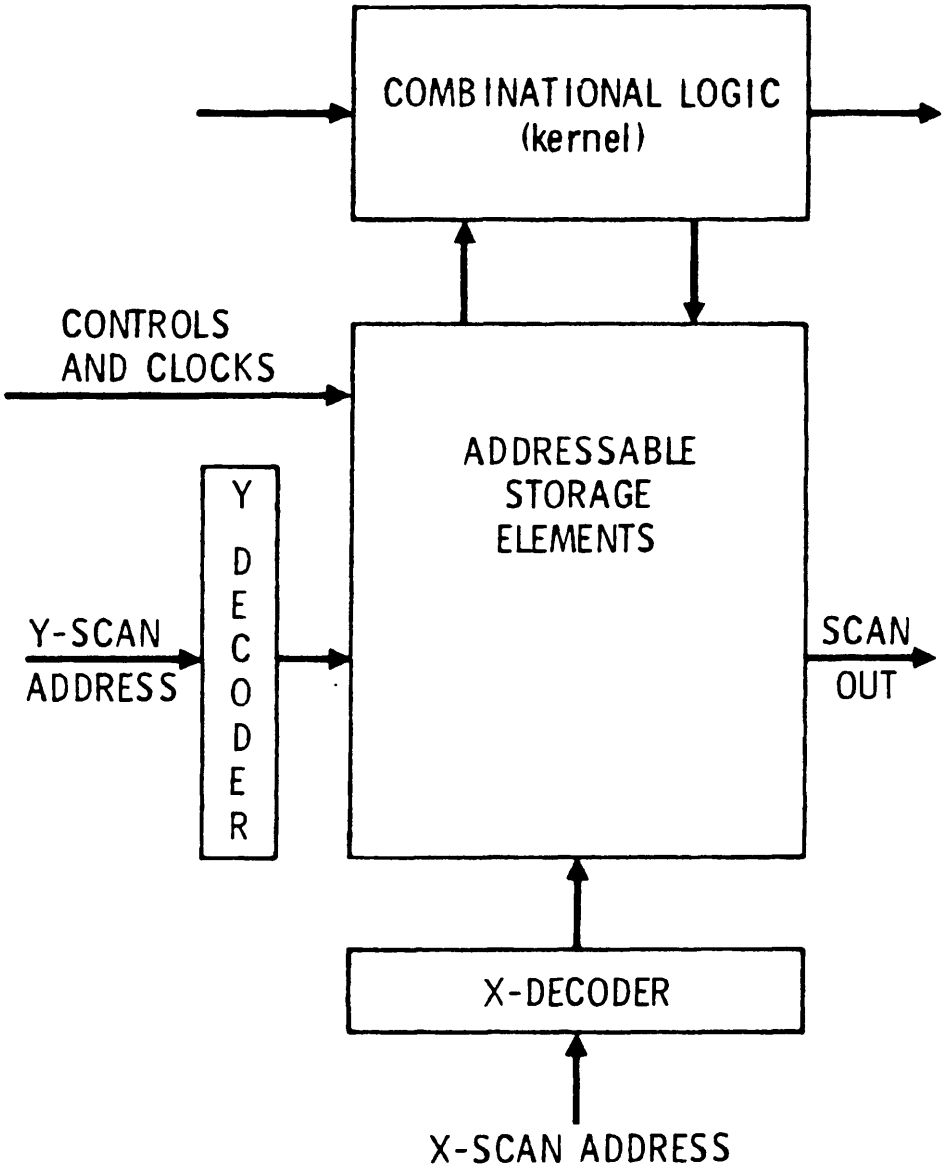


FIGURE B-4. Random Access Scan Testable Structural Style

2.7.5 Built-in Logic Block Observation (BILBO) Testable Design Methodology. This testable structural style is an example of a fully built-in test approach: hence, no off-line test generation is used, and only minimal automatic test equipment is required. The built-in logic block observation registers carry out four functions for testing; namely, controllability, improvement, test sector generation, observability, and test response processing (signature generation).

Figure B-5 shows the testable structural style used in the built-in logic block observation testable design methodology. The kernel is again combinational logic and usually of the gate combination network design style. Since this approach is based upon pseudorandom test patterns, a read only memory or programmable logic array design style is not suitable. The circuit C_1 is tested by configuring the built-in logic block observation register on the left as a pseudorandom pattern generator and the built-in logic block observation on the right as a signature generator.

2.7.6 Syndrome Testable Design Methodology. The testable structural style for the syndrome testable design methodology is shown in Figure B-6. Again, the kernel is combinational, but this approach is applicable to gate combination network. programmable logic array, or read only memory design styles. Only a single output is indicated. Testing is accomplished by having the counter produce all 2^n input vectors. while the count register counts the number of 1's on the output. The correct number of 1's is the number of minterms in the function realized by C and is denoted by K. Then $S=K/2^n$ is Said to be the syndrome. Fault detection is achieved by comparing the final state of the count register with S. In this built-in self test methodology, no off-line test generation is required. and the automatic test equipment requirements are minimal. Often the design of the circuit C (for gate combination network and programmable logic array design styles) is modified to enhance testability; e.g., a syndrome testable circuit is one for which every single stuck-at fault is detectable by this testing approach.

There are several variations to this form of testing. For autonomous testing, the output of the kernel is directly observed by an automatic test equipment rather than compacted into a signature (syndrome). This form of testing thus guarantees detection of all faults which are not sequential in nature. Alternatively, the response can be processed via a linear feedback shift register, and again a signature can be generated.

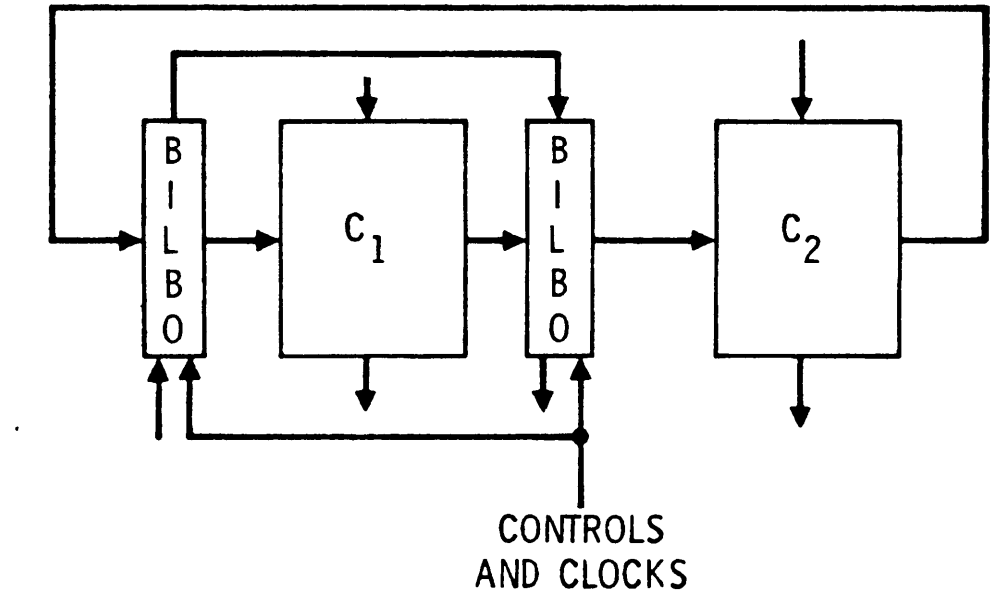


FIGURE B-5. Built-in Logic Block Observation Testable Structural Style

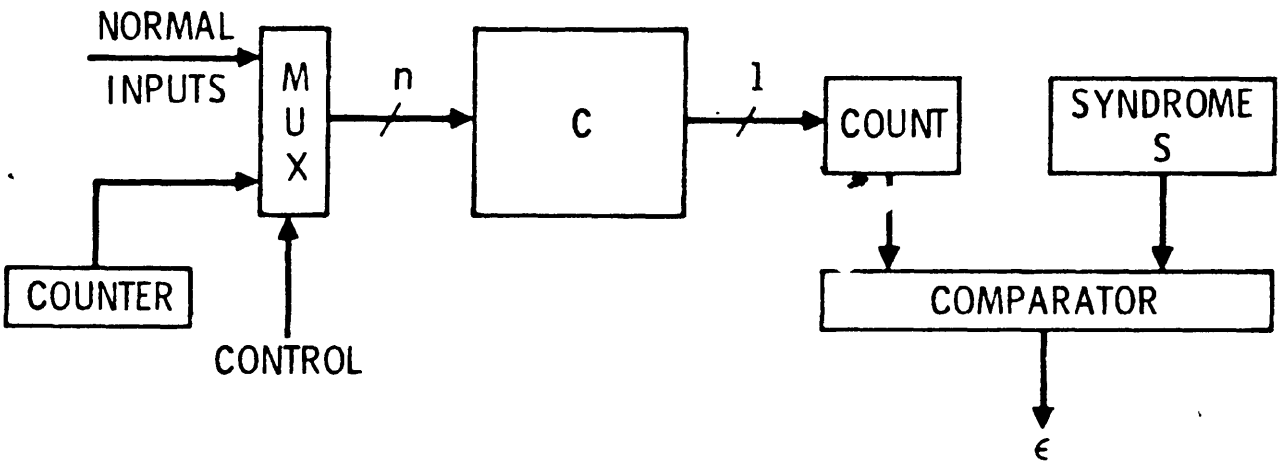


FIGURE B-6. Syndrome Testable Structural Style

2.7.7 Easily Testable Bit-Sliced Testable Design Methodology. While bit-sliced architectures are usually implemented via interconnecting chips, as the level of integration increase these architectural style will be used more extensively at the chip level. One reason for this is regularity in layout and testing. A testable structural style ideal for bit-sliced architectures has been developed. One version of this architecture is for CI-testable arrays. To introduce this concept, a few definitions are needed. An iterative logic array is a one-dimensional cascade of identical cells (see Figure B-7). The cells can be either combinational or sequential circuits. An iterative logic array is said to be C-testable if it can be tested with a constant number of test patterns, independent of the array size N. Let T be a test set that tests an iterative logic array D completely under the assumption that only one cell in the array is faulty. D is I-testable with respect to T if the expected responses to T appearing at the vertical outputs of every cell L_i of D are identical. A CI-testable iterative logic array is both C-testable and I-testable with respect to some test set T. The necessary and sufficient conditions for an iterative logic array to be CI-testable are given in the literature.

In Figure B-7 $L_1, L_2,$ represents the CI-testable iterative logic array to be tested. The normal inputs and outputs are shown. The test T can be stored off-chip and applied via automatic test equipment or on-chip and stored in a read only memory. The equality checker determines if the responses from each L_i are identical. The case of a single output line from each L_i is shown, but the concept can be easily generalized to the case of multiple output lines.

Off-line test generation is required for this methodology; for complex cells, this process may be quite difficult and require the use of checking sequences. Real time test hardware can be either on-line or off-line. Test application to the kernel is achieved via the multiplexer. while observability of the responses is not required due to the equality checker and the concept of I-testability.

2.7.8 Summary. In summary, fully built-in testing deals with those test strategies where the role of the external test equipment is minimal. Built-in logic block observation and syndrome testing are examples of methodologies which employ fully built-in testable structural styles. The general architecture for such a style is shown in Figure B-8. Table B-IV summarizes the various options for each block in Figure B-8. When built-in test structures are added to a

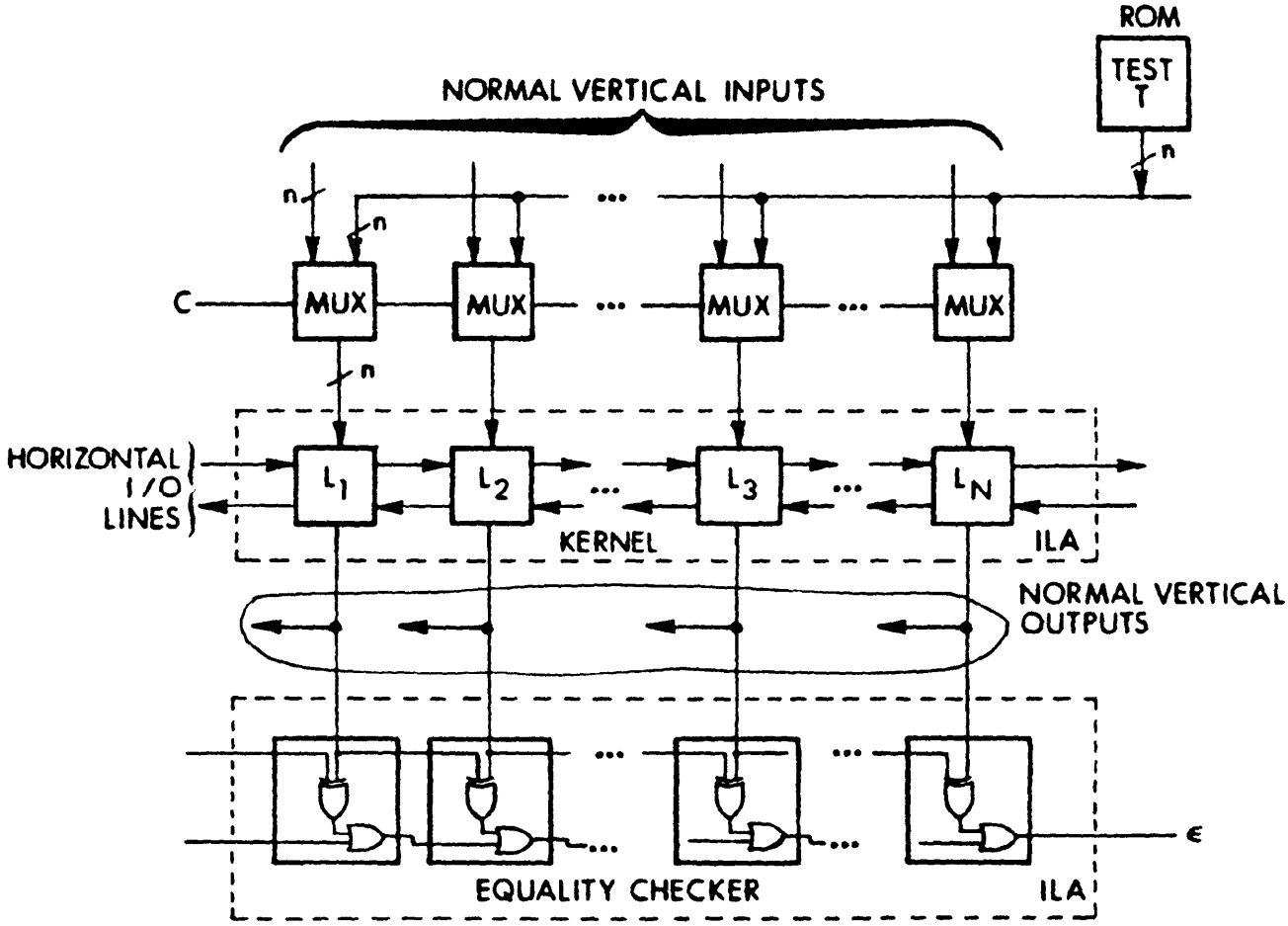


FIGURE B-7: Bit-Sliced Testable Structural Style

TABLE B-IV: Some Options in the Design of a Fully Built-In Testable Structural Style

- Stimulus Generator
  - Hardware test generation
    - random patterns using a linear feedback shift register
    - all input combinations using a linear feedback shift register or a counter (exhaustive)
    - some specified patterns using a nonlinear feedback shift register
  - Stored test patterns
  - Store and generate - store some pre-calculated patterns as initial values for a linear feedback shift register
- Functional circuit
  - Sequential circuit - can be partitioned into combinational parts using set/scan registers
  - Combinational circuit - partition into manageable subcircuits
- Response analyzer
  - Use compressed responses -
    - syndrome (one's counting)
    - signature using linear feedback shift register
    - transition counting
  - Store the correct responses
  - Generate the correct response
  - Compare responses with correct ones and generate go or no-go signal
- Controller
  - Control transition between test mode and normal mode
  - Control testing process

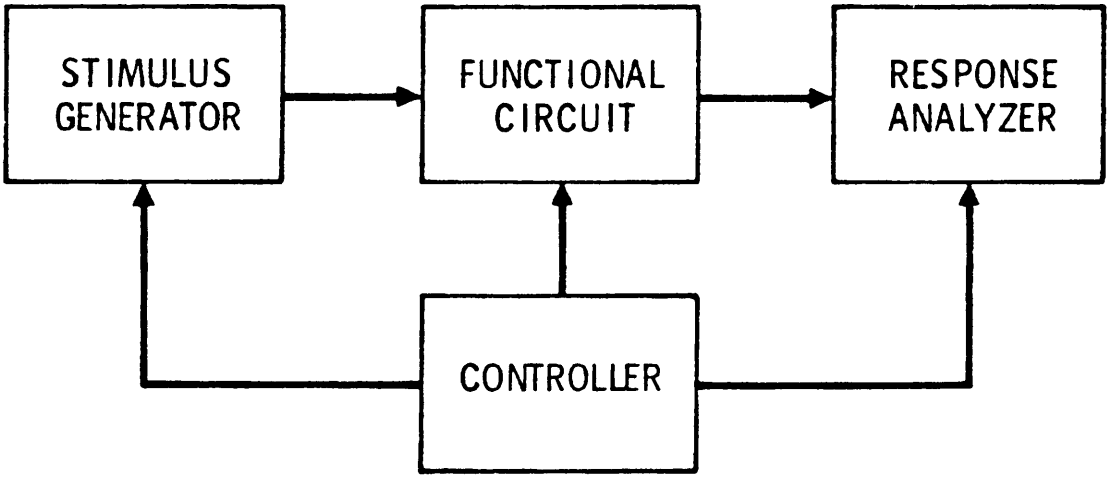


FIGURE B-8. General Form for a Fully Built-In Testable Structural Style

circuit, care must be taken to ensure that the test structures are themselves tested, either implicitly or explicitly. Also, when several different testable structures exist on a chip, some additional hardware overhead may be required to control the test process.

2.8 TESTABLE DESIGN METHODOLOGIES FOR PROGRAMMABLE LOGIC ARRAYS

Numerous techniques for testing the programmable logic array design style have been suggested. Figure B-9 indicates several testable design methodologies for programmable logic arrays according to certain attribute, such as whether or not they support concurrent testing, produce a self-testing programmable logic array, require off-line test generation, and are based upon a special design approach. Naturally, these techniques could have been classified and grouped differently, such as by fault coverage area overhead.

Figures B-10, B-11, and B-12 indicate the testable structural styles corresponding to just three of the techniques listed in Figure B-9.

2.8.1 Programmable Logic Array with Universal Test Set. Figure B-10 indicates a testable structural style for a programmable logic array which employs a universal test set; hence, no test pattern derivation is required. The normal design of the programmable logic array is shown in heavy lines. The medium lines indicate added built-in test structures, and the thin lines indicate wires. The product term selector is a shift register; the data in this register enable and disable the product lines in the array. The AND array is extended by one product line such that each input row has an odd parity; a word parity line is also added to the OR array. The inputs y_0, y_1, y_2 are used to control the circuit during the normal and test mode. An error is indicated by testing the two lines (z_1, z_2). This test can be done on-chip or off-chip. The Di_n is a new input used to supply data to the product term selector register. Normally the universal test set is stored off-chip and is applied via the automatic test equipment.

If the programmable logic array has n inputs and m product lines, then the number of tests in the universal test set is 2n + 3m. These tests detect all single stuck-at faults in the decoder blocks f and the programmable logic array, all crosspoint faults in the programmable logic array. and all stuck-at faults in the parity chain #1.

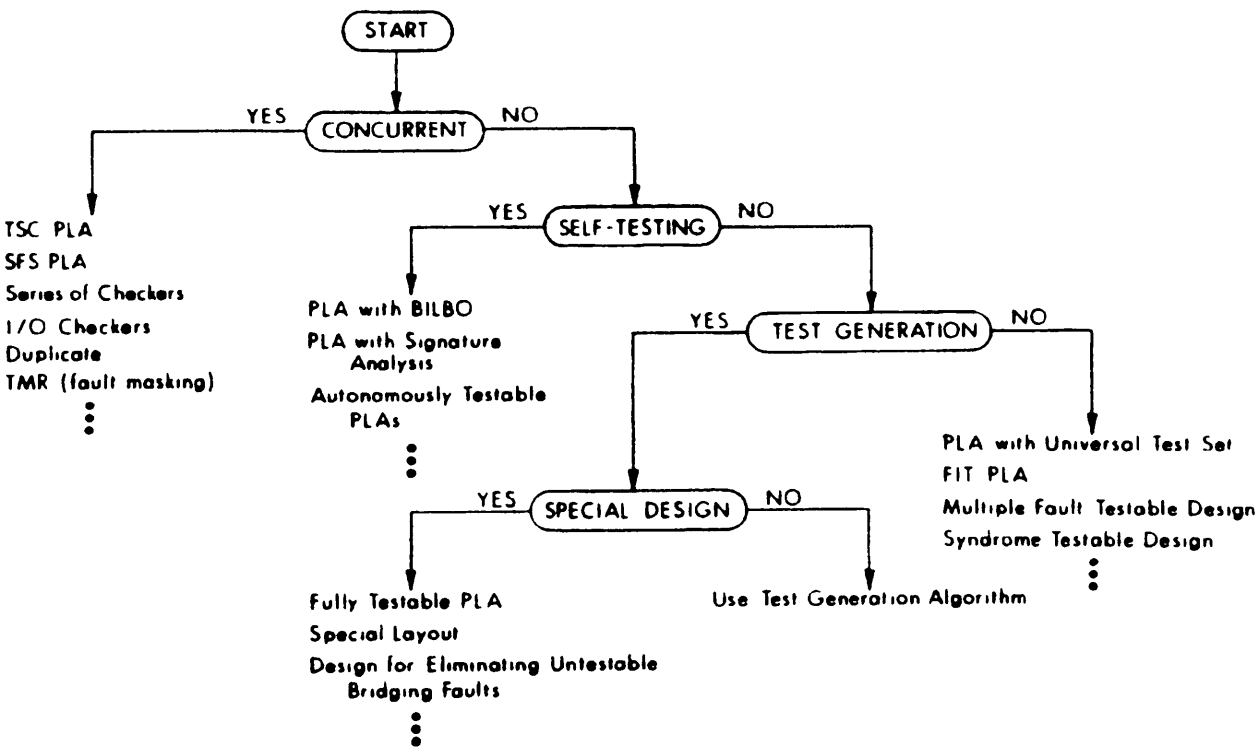


FIGURE B-9. Testable Design Methodologies for Programmable Logic Arrays

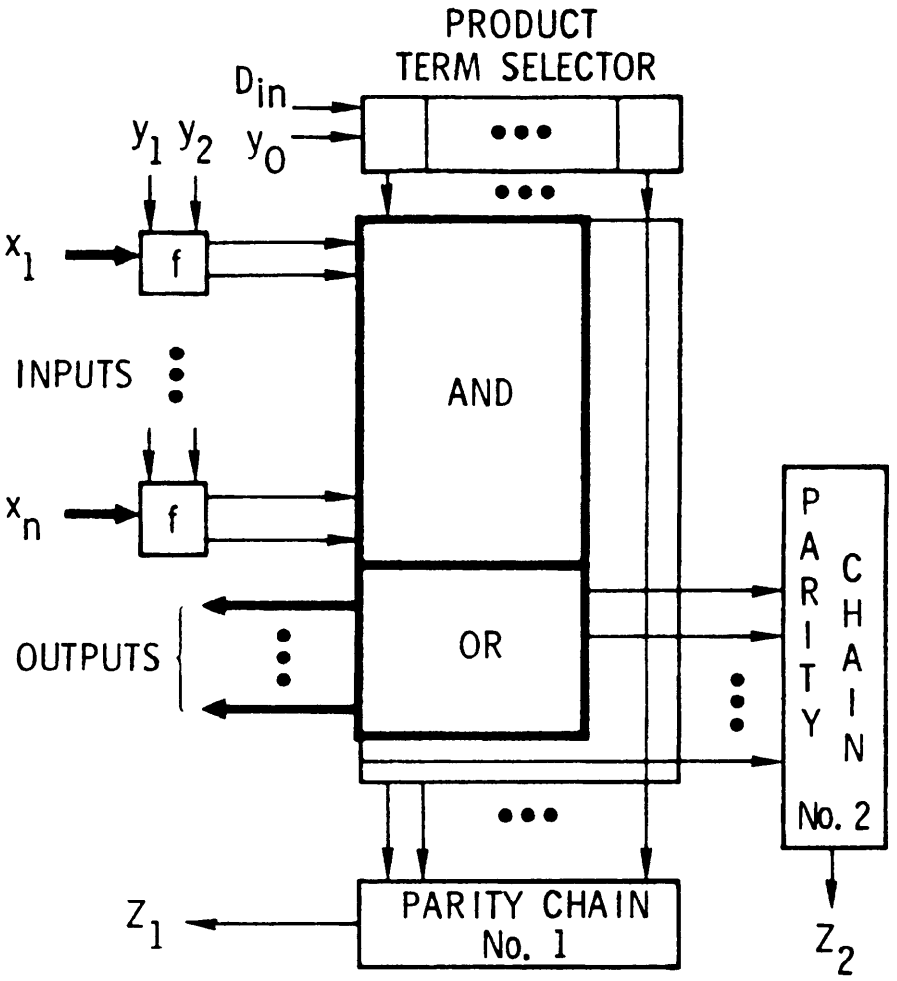


FIGURE B-10. Programmable Logic Array with Universal Test Set

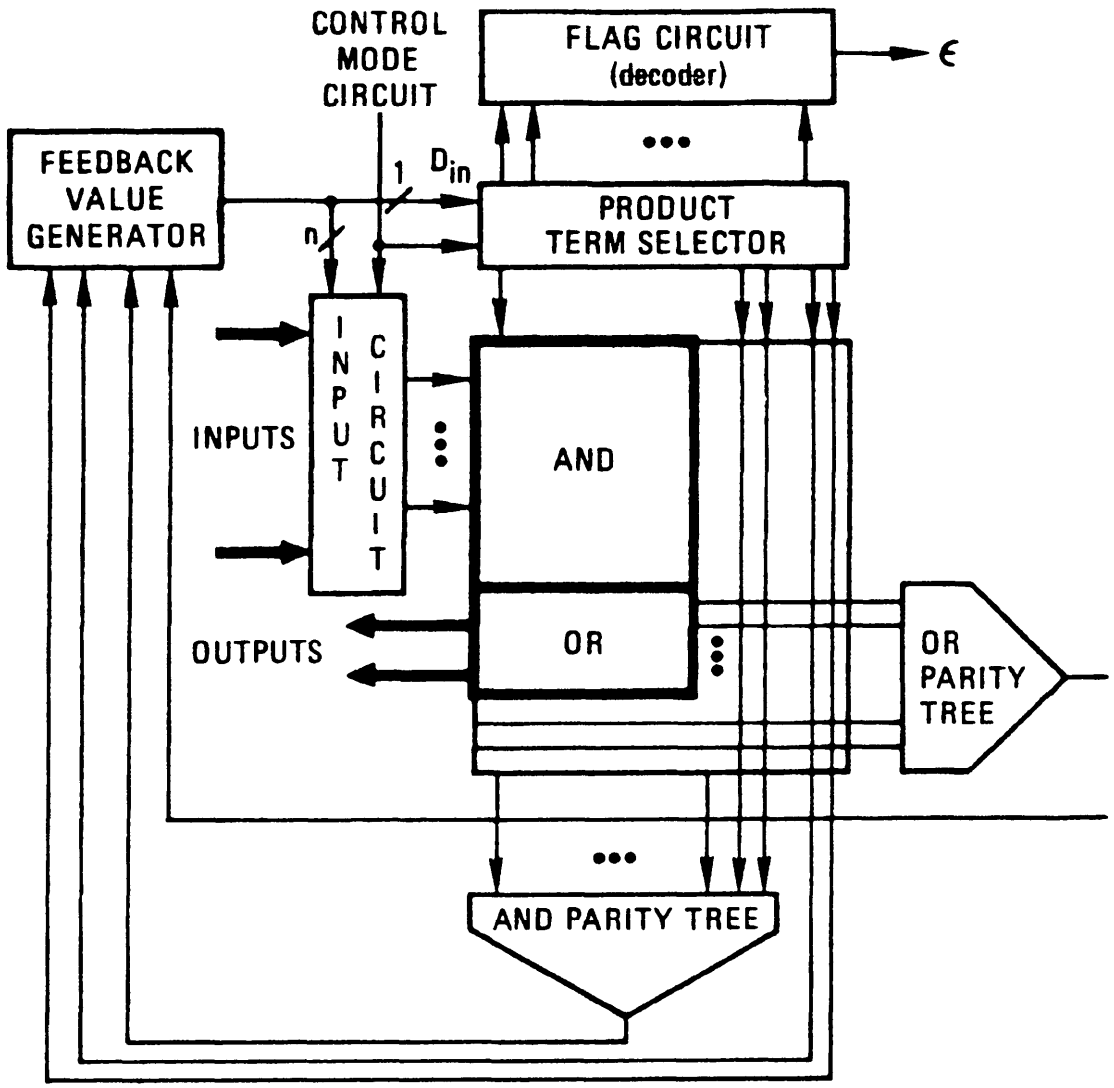


FIGURE B-11. Autonomously Testable Programmable Logic Arrays

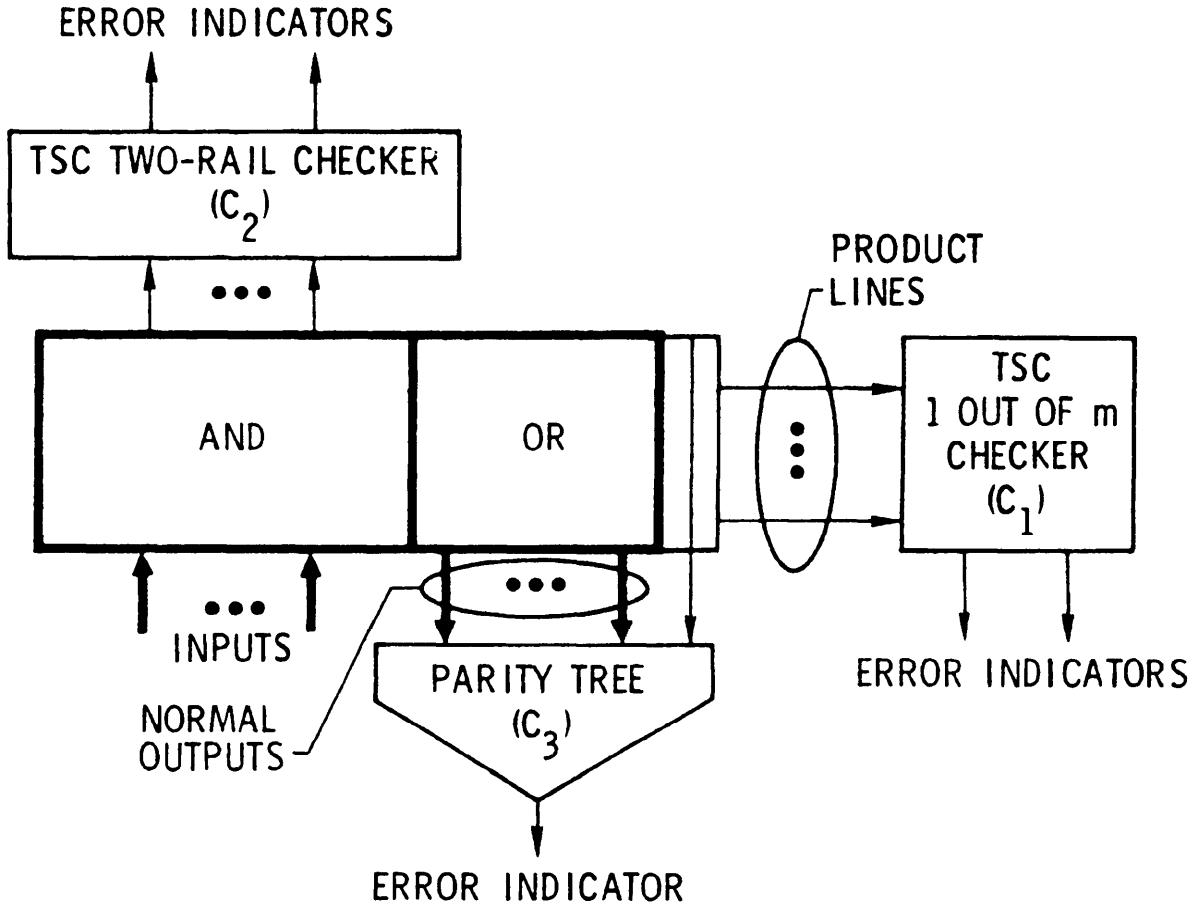


FIGURE B-12. Programmable Logic Array with Concurrent Error Detection and Testing

2.8.2 Automously Testable Programmable Logic Arrays. Figure B-11 indicates what is referred to as an autonomously testable structural programmable logic array style. This form of testing is very similar to the universal test set approach, except that rather than store the universal test set and have them applied via an automatic test equipment, the autonomous test approach generates the test patterns on-chip.

For this design, a product term selector register. several additional parity word and product term lines, and the parity chains have again been replaced by parity trees to enhance their testability.

The control for normal and test modes may still be external: however, the input test data and the data for Di_n are now all generated on-chip by the feedback value generator which is a simple sequential circuit. At the end of the test process, the product term selector register contains a signature: it is decoded by the flag circuit which produces an error flag if a fault has been detected.

This approach employs n+2m+8 tests and detects all cross point faults in the programmable logic array as well as all single stuck-at faults in the entire circuit except for parts of the feedback value generator and flag circuit. These can be duplicated if necessary.

2.8.3 Programmable Logic Arrays with Concurrent Error Detection and Testing. Figure B-12 indicates a programmable logic array testable structural style which supports concurrent error detection. The programmable logic array must be designed so that it has concurrent product lines, i.e., exactlv one product term is true for every input vector. This condition usually increases the size of the programmable logic array. Since the programmable logic array inputs exist as a two-rail circuit (x_i, x'_i). a totally self-checking two-rail checker C_2 is used to detect stuck-at faults on input lines. A parity output word is added to the OR array, and a parity tree C_3 is used to detect errors on the outputs. Since concurrent testing is employed. a totally self-checking 1 out of m checker C_1 can be used to detect errors on the product lines.

During normal operation, this testable structural style will detect any of the following faults which produce output errors: single stuck-at faults. shorts between adjacent lines, and crosspoint faults. Most transient faults are also detected. Since it is possible that the normal inputs may not completely test C_1 and C_3. it may be necessary to carry out off-line testing so that these circuits can be completely tested.

2.9 SUMMARY

This section has presented a survey of some of the important concepts related to the design of a testable CLSIC. The concepts of fault tolerance and testing have been touched on. Both external testing and design for testability have been discussed. Several design for testability concepts have been presented, with emphasis on structures for semi and fully built-in testing.

In addition, an approach to achieve testable designs has been suggested. In this approach, it is necessary to first partition a CLSIC into structures to be tested as separate entities. Some of these structures may be basic structures and have design styles. Often the characteristics inherent in a structure or its design style dictate a testing approach. The concept of a test strategy, consisting of off-line test generation, run-time test hardware, and built-in test structures for input and output accessibility, was introduced. Given a selected test strategy for a structure to be tested, a testable structural style is created. A testable chip thus consists of instances of testable structures. each of which corresponds to some testable structural style. The result of using these concepts in an orderly and effective way, satisfying the goals and constraints imposed by the design specifications, constitutes a testable design methodology.

SECTION 3

GUIDELINES

This section elaborates on those sections of the handbook dealing with testing and testability. After each section number the corresponding section in the handbook being addressed is indicated.

3.1 FAULT TYPES (4.3.1.1.1)

The expected physical failure modes and their probability of occurrence may be estimated from an analysis of the specific IC manufacturing technology being used for the CLSIC. The major failure modes include package wiring faults; on-chip metallization failures due to corrosion, electromigration. microcracks, or bridging; dielectric failure due to mask defects or ESD; pattern sensitivity; and radiation-induced soft faults. Useful failure statistics on established IC technologies are published regularly by the Reliability Analysis Center (Rome Air Development Center, Griffiss Air Force Base, NY, 13441). Failures may be characterized as permanent, intermittent (temporary and recurring), or transient (temporary and nonrecurring). Physical failures frequently result in logical faults which may be represented by functionally equivalent logical fault modes for test vector generation and testability analysis purposes. The standard logical fault model is the single stuck-line model, which allows any logic signal connection in a circuit to be permanently stuck-at logical 0 or 1. The single stuck-line model has been found adequate for representing most types of permanent logic faults encountered in bipolar digital circuits. It is inadequate for dealing with some types of open-circuit and short-circuit faults. pattern-sensitive faults. and delay faults involving changes in signal propagation delays. Some of these faults can be dealt with by either localized exhaustive testing or by devising "workaround" circuits that allow the nonstandard fault of interest to be replaced by an equivalent single stuck-line fault model. The occurrence of hard to detect faults can be reduced by making appropriate modifications to the logic design and layout of the CLSIC. Often, the fault model selected for a particular circuit is based upon the design style of that circuit, such as a programmable logic array, random access memory, or read only memory. Based upon the failure statistics of the IC technology and the fault types selected to be considered, the contractor can determine the correlation between those faults covered by the models and the physical failure mechanisms exhibited by the chip.

3.2 TESTABILITY MEASURES (4.3.1.1.2)

The two primary measures of testability are fault coverage and fault resolutions. Other measures may only be useful in making design choices in specific cases. Comparisons of designs that satisfy the fault coverage and fault resolution requirements with designs that do not meet those requirements are usually not significant and may be misleading.

3.2.1 Fault Coverage. The need to measure fault coverage and the means for carrying out this measure are a function of the testing approach taken for a particular circuit.

If a complete functional or exhaustive test is carried out and the response data are not compacted, then fault coverage for permanent stuck-at faults is presumably 100 percent, and no further analysis is required.

The fault coverage with respect to a specified set of faults F and nonexhaustive tests T can be calculated by simulating the response of the device under test to T with each of the faults from F present. Fault coverage may also be obtained as a byproduct of the test generation process itself: typical test generation programs use simulation to check the ability of the tests T being generated to cover the target faults F. Representative commercial computer programs for test generation and simulation that can provide fault coverage data are D-LASAR (Teradyne) and TEGAS (Comsat-CGL). The cost of formulating the simulation models and executing the test generation and simulation programs can be very high for large unstructured designs. It can be kept to manageable levels by the use of testable design styles such as level sensitive scan design (see Section 3.6.4). If the fault class is extremely large, e.g., the set of all possible multiple stuck-at faults, then fault coverage can be estimated statistically by simulating only a subset of the possible faults. The nonsimulation technique of critical path tracing can also be used to estimate fault coverage in combinational circuits. In general, the goal of 100 percent fault coverage of the detectable single stuck-at failures should be sought.

Fault coverage may be calculated directly without simulation for some types of self-checking circuits whose error detecting capability is known a priori. For example, in a random access memory employing a single-error correcting double-error detecting code, faults causing one or two bits of a data word storage cell to become stuck at 0 or 1 can be detected by the code-checking circuitry with a fault coverage of 100 percent.

When the syndrome testing techniques are employed, 100 percent fault coverage of the single stuck-at faults can be guaranteed via the testability synthesis approach, and simulation is not necessary. When standard or universal test sets are employed, again the fault coverage is often known a priori.

When linear feedback shift registers are employed for on-chip pattern generation and signature generation, as in the built-in logic block observation techniques, then fault coverage can still be estimated via simulation. For this form of built-in testing, the actual fault coverage can be increased in a number of ways, such as by selecting more than one feedback network for the registers or by increasing the length of the registers. The main goal in this form of testing is to minimize the problem of aliasing (having an erroneous output produce the correct signature), and of not generating a critical input pattern (having a faulty circuit not produce an output error).

3.2.2 Fault Resolution. Since CLSIC chips cannot be repaired, fault resolution does not have the same relevance as it has for a printed circuit board. Its use in the CLSIC context is primarily for identifying flaws in the design process or in the silicon processing.

Fault resolution may be defined as the maximum or worst case number of circuit elements to which any given fault can be isolated or located via the specified testing procedures. Fault resolution can be determined by fault simulation programs, as discussed under “Fault Coverage” (3.2.1 above). Because of the large amount of simulation time involved, the measurement of fault resolution may be based on simulation of a small but statistically representative sample of the fault types under consideration. If acceptable to the contracting agency, estimates may also be based on manual analysis of the CLSIC that identifies the worst case faults from a resolution viewpoint.

The fault resolution with respect to a test T for a subcircuit in the CLSIC can also be specified in tabular form, such as the one indicated in Table B-V. In a particular case, Xl may represent the range 10 to 15 transistor, and Y_1 may be 3 percent of the stuck-at faults; X_2 the range 5 to 9, Y_2=17 percent; X_3 the range 3 to 4, Y_3=30 percent; X_4 the range 1 to 2, and Y_4=50 percent. What this means is that, in this case, at least 50 percent of the stuck-at faults must be locatable to 1 or 2 transistors.

TABLE B-V. Fault Resolution Table

Size of Fault Resolution Class	Percent of Faults in Fault Resolution Class
x_1	Y_1
x_2	Y_2
.	.
.	.
.	.
x_n	Y_n
	100 percent

3.2.3 Hardware Circuit Overhead. The hardware circuit overhead is given by the formula

$$\frac{h_T}{h-h_T} \times 100 \text{ percent}$$

where h is the number of transistors or logic gates in the CLSIC as a whole, and h_T is the number used in the circuits included exclusively to enhance testability. The h and h_T are determined by actual count.

3.2.4 Chip Area Overhead. The chip area overhead is given by the formula

$$\frac{a_w - a_{wo}}{a_{wo}} \times 100 \text{ percent}$$

where a_w is the surface area of CLSIC chip, and a_{wo} is the actual area, or a reasonable estimate thereof, of a functionally equivalent chip without the CLSIC's testability features. This formula implicitly includes the extra pads, drivers, and other features required to support the functional part of the testability circuits.

3.2.5 Software and Firmware Overhead. The software and firmware overhead may be computed from the formula

$$\frac{m_T}{m-m_T} \times 100 \text{ percent}$$

where m is the total capacity of the relevant memory (main memory in the software case and control memory in the firmware case) in the CLSIC, and m_T is the amount of memory space devoted to enhancing testability. These capacity figures may be measured by the number of executable instructions of microinstruction involved; they may also be measured in bits.

3.2.6 Performance Overhead. The clock frequency overhead may be determined from a worst case analysis of the effect. if any, of the testability features on circuit propagation delays and, hence, on maximum clock frequency. This duty cycle measure is usually appropriate for CLSICs that have a separate testing mode during which the normal computational functions of the CLSIC are temporarily halted. A suitable performance measure in this case is the availability A, which is defined as the mean percentage of time during which an operational chip performs normal (nontesting) functions.

3.2.7 Reliability Overhead. The reliability of the CLSIC may be specified by the predicted failure rate λ, the corresponding mean time to failure MTTF $=1/\lambda$, or the reliability function $R(t) = e^{-\lambda}$ The MIL-HDBK-217 model is widely used for calculating λ for ICs. It defines λ the failure rate per million hours of operation, in terms of the IC technology used (MOS, bipolar, or others), the maturity of the fabrication process, the device screening quality, the operating environment, the component density (the number of gates or transistors used per square millimeter), the pin count, and other relevant parameters. By computing λ for the CLSIC both with (λ_w) and without (its testability features, an indication of the impact of these features on reliability can be measured by the formula

$$\frac{\lambda_w - \lambda_{wo}}{\lambda_{wo}} \times 100 \text{ percent}$$

denoting the percentage increase in failure rate. Note that this analysis does not take into account the impact on reliability of any fault tolerance mechanisms in the CLSIC. Computer programs implementing various versions of the MIL-HDBK-217 failure rate model are available.

3.2.8 Testing Speedup. The testing speedup can be expressed by the formula

$$\frac{s_w - s_{wo}}{s_{wo}} \text{ X 100 percent}$$

where s and s_{wo} denote the total testing times for the CLSIC with and without its testability features, respectively. The times s_w and s_{wo} may be determined precisely by actual construction and testing of two versions of the CLSIC: they can also be obtained, usually at far less cost, by computer simulation. In other cases, an estimate of s_{wo} may be used to calculate the testing speedup, based on the actual value of s_w and a manual analysis of the impact of the testing features of the CLSIC on testing time.

3.3 TESTABILITY SYNTHESIS (4.3.1.2)

The development of an effective testability design methodology involves the following steps:

a. Specification of the relevant failure modes, testability measures, and error notification requirements

b. Identification of candidate testing methods, both on-line (built-in) and off-line, and their support requirements, e.g., automatic test equipment or software

c. Evaluation of the effectiveness of the candidate approaches and selection of the most cost-effective one

3.3.1 Fault Characterization (4.3.1.2.1). When faults are characterized, the following aspects are to be considered:

a. How circuits fail, i.e., failure mode analysis

b. The logical models used for characterizing these failures

c. The relative probability of occurrence of each failure mechanism

Circuit failures occur due to numerous reasons, such a radiation, metal migration, punch through effects, and capacitance and resistance effects. The effect of initial metal migration may be to cause transient errors, while extreme

cases may cause a permanent open circuit. The types of failures and their probability of occurrence are a function of several factors, such as the design rules, the IC family, the process characteristics, and the circuit layout. For example, shorts between lines may be much more probable in a programmable logic array than in a NAND gate realization of the same function. Once the failure mechanism types have been identified, they can be placed into categories dealing with their effect on timing, circuit structure, and logical behavior. For example, capacitance-related faults can affect timing and may require dynamic testing. Shorts and opens affect circuit structure. The modeling of faults for purposes of test generation or simulation can be a function of the circuit structure in which the fault exists. For example, an open in a combinational circuit and in a random access memory may be modeled and processed entirely differently.

Failure mode analysis is based primarily on data from device screening tests, accelerated life testing, and field operation. Detailed data for widely used IC families are published by the Reliability Analysis Center. For test generation and testability evaluation, logical fault models such as the single stuck-at line model are widely used (see Section .

The results from fault characterization can be a tabulated list of faults or fault modes which can occur in the CLSIC, the models used to characterize these faults. and the relative probability of occurrence of each fault or fault mode. The number of occurrences of a particular fault mode should be determined, since this number is useful in evaluating fault coverage and determining the probability of a faulty chip passing a test.

3.3.2 Testing Techniques and Strategies (4.3.1.2.2). Most external (off-line) test generation methods for general logic circuits employ computer programs that implement the D-algorithm or a similar path-sensitization technique. They also usually employ the single stuck-line fault model as the standard model. Nonstandard faults can sometimes be handled via workaround circuits containing functionally equivalent single stuck-line faults. Commercial test generation programs such as TEGAS and LASAR typically achieve single stuck-line fault coverage in the 60 to 95 percent range for circuits up to about 1000 gates and 50 flip-flops. To obtain comparable or higher fault coverage for larger circuits. use of an easily testable design technique such as level sensitive scan design appears to be necessary.

Built-in testing methods for general circuits fall into two main groups: concurrent and nonconcurrent. Error detecting and error correcting codes are the basis for most concurrent built-in tests. Such codes are widely used for testing memories and busses and are well understood. Concurrent built-in tests can also be implemented by replicating the components to be tested and continuously monitoring their outputs via match circuits. Of course. this entails at least doubling the amount of hardware used. Nonconcurrent built-in test methods have two operating modes: a test mode and a normal mode during which no testing is performed. Tests are executed periodically under the control of resident test hardware, software, or firmware. The test data are either precomputed and stored in a read only memory or generated via built-in test algorithms. Microprogrammed self-test firmware has proven very effective where it is applicable. One hardware-based built-in test technique, referred to as built-in logic block observation (BILBO), is based on signature analysis and is currently under development. It involves very little hardware overhead for testing, but its fault coverage is unclear.

A large number of easily programmed testing techniques have been developed for random access memories, but test generation for microprocessors or microprocessor-based circuits is still a poorly understood heuristic process. Nonreplicated complex components such as microprocessors are usually tested by heuristic methods that attempt to exercise the component's functions. Since they do not employ explicit fault models, the effectiveness of these testing methods is difficult to determine.

The overall test strategy should consider all available testing techniques and select those appropriate for the specific technology used and for the functions, testability features, and other requirements of the specific CLSIC. The overall test strategy for the CLSIC should include the individual test strategies for each of the various design structures on the CLSIC. The major issues in developing an overall testing strategy are:

a. Identification of the stages in the development and fabrication at which testing is to be carried out

b. Selection of the testing techniques to be used at each stage

c. Allocation of the testing facilities between external testing and built-in test

d. Design or acquisition of the hardware and software facilities needed to implement each test process

3.3.3 Intermittent Failure Detection (4.3.1.2.3). Intermittent failures may be detected rapidly on coded data via self-checking circuits such as the checkers associated with error detection/error correction codes. Detected errors should be logged in appropriate error registers. e.g., in on-chip random access memories, that are accessible to the on-chip or off-chip diagnostic procedures. Automatic retry facilities should be used to repeat any operation that may be attributed to an intermittent or transient fault, e.g., an unsuccessful memory read or write operation. The retry function can be efficiently implemented via a software or firmware interrupt that is invoked by an error signal. This routine typically restores the circuit to the state existing before the error appeared and causes the faulty operation to be repeated. Successful implementation of retry requires good error confinement to limit the spread of error signals throughout the circuit. This in turn usually requires extensive use of hardware, firmware, or software facilities to check the consistency of all major data transfer, processing. and control functions. Failures that result in incomplete operations, e.g., the failure to issue a required acknowledge signal, can be detected via time out circuits (watchdog timers). The number of retry attempts needed to distinguish permanent (unrecoverable) failures from intermittent or transient failures depends primarily on the expected duration of the nonpermanent failures, as well as the circuit's ability to limit error propagation during retry attempts.

3.4 TESTABILITY EVALUATION (4.3.1.3)

The testability measures defined in Section 3.2 provide key quantitative figures-of-merit for evaluating the CLSIC. Their application requires a thorough analysis of the expected physical failure modes and failure rates, as well as the circuit's logical structure, speed of operation, and the hardware and software overhead attributable to testing. Once the testing strategies for each circuit structure in the CLSIC are established, the contractor should determine how the testability measures defined in Section 3.2 are to be evaluated. Specified approaches and tools should be identified for each item: e.g., How will fault coverage be measured? If simulation is chosen, which simulator will be used? The contractor should determine whether these tools are already available, or whether they must be developed. Proven tools should be used, since new ones require validation.

If the CLSIC consists of many different structures, then an analysis of the various parameters associated with these structures must be carried out to ensure that the overall testability requirement of the CLSIC are met. Hence, structures on the chip which have higher failure rates may require more thorough test strategies than other structures.

Based upon the fault modes inherent in a technology. their probability of occurrence, and the fault models employed, the relationship between fault coverage and the probability that a faulty chip successfully passes a test can be determined by the contractor. This information can be used later to determine a minimal acceptable value of fault coverage.

3.5 TESTABILITY ANALYSIS, CONCEPTUAL DESIGN PHASE (7.6)

The first step of this preliminary stage in the design process is the selection of the testing methodology to be used for the major architectural elements of the CLSIC such as for the memories, processors, or busses. This selection will be guided by the expected fault types for the CLSIC's technology type and operating environment (see Section 3.1) and also by any constraints that might be placed on chip area, pin count, or operating speed. A priori requirements for compatibility with existing circuits or IC families will influence architectural style and testability. A major decision is to determine the relative use to be made of built-in test features and external automatic test equipment. In the design of built-in test features. it should be decided where concurrent and nonconcurrent testing methods would be used. High-speed continuous operating requirements favor concurrent testing. Error correction/error detection code checking methods provide a good degree of testing confidence at moderate hardware circuit overhead. Higher confidence can be obtained via replication and comparison (match circuits), but the chip area overhead is large. A self-testing computer employing comprehensive concurrent testing with moderate overhead for built-in test features has been designed. Nonconcurrent testing programs may be readily included in circuits with resident program or microprogram memories. Typically, these programs systematically exercise the major functions of the circuit. The testing confidence and testing time generally increase with the size of the testing program.

Access points for wafer testing may be provided by means of test pads at the interfaces of all major components of the CLSIC. Access after packaging can be provided by test pins. In bus-oriented circuitry, such as a microprocessor-like circuit, it is desirable to provide the automatic test equipment with direct access and control over the main internal

busses. This can be achieved by providing programmable data paths from all busses of interest to an externally accessible bus port of the chip. Such a "diagnostic port" is found. for example, in the Fairchild/Mostek 3870 microcomputer chip. Access to input and output pads via some mechanism such as scan paths should be made available so that tests for interconnect failures at the next higher level of integration can be executed.

Circuit partitioning is an important means for enhancing testability. The use of bit-slice architectures leads to testing of smaller, regular structures. Large combinational logic structures may need to be partitioned 60 that they can be processed more effectively by test generation algorithms. Where built-in test techniques are employed, such as syndrome testing or built-in logic block observation, circuits may need to be partitioned 60 that the test application time is not excessive. Often, the number of inputs to circuits tested by such means is limited to about 20.

3.6 TESTABILITY DESIGN REQUIREMENTS (8.3)

a. Test pattern injection is a primary concern when external automatic test equipment is used. It can be achieved by careful design of the circuit's functional interface so that normal access paths can be used for testing purposes. Where necessary, and permitted by pin constraints, special test points for test pattern injection can be provided. Where input data access is desired but not available via the primary inputs, then special circuitry can be employed such as scan path registers or the level sensitive scan design methodology.

b. The access requirements for observability purposes are basically similar to those noted under Paragraph (a) above for controllability. For CLSICs containing large amounts of memory in the form of registers, stacks, and random access memories, observability and controllability can be enhanced via architectural considerations which allow these registers to be read by and written from a circuit bus. This also makes many important operational processes easier to handle, such as initialization, rollback. interrupt processing, and retry.

c. External error indication is best provided by a single output pin that is activated by the built-in test features when an error occurs. Additional status bits may be provided to enable the built-in test features to supply diagnostic information. The 6805, for example, outputs a 4-bit word indicating the results of executing its on-chip test program.

d. Checking the built-in test features itself may be accomplished by the use of self-checking checkers. which are most suited to designs employing error detection/error correction codes or replication with matching. It may also be desirable to design the built-in test structures so they can be easily isolated from the rest of the circuit for testing by external automatic test equipment.

Careful analysis of built-in test structures often indicates that little. if any, additional checking of this circuitry is necessary. That is, the test circuitry is normally thoroughly checked when it is used in the testing process of the CLSIC. Provisions must be made, however, to test error indication circuits via injection of error conditions. For example, to check a parity checker, it may be necessary to inject a parity error in a data word.

3.6.1 Simplicity and Regularity (8.3.1). IC design styles that favor regularity are those employing programmable logic arrays, read only memories, random access memories. bit-slicing, and microprogramming. It is generally desirable to make the standard cells as large as is feasible within the constraints imposed by the CLSIC's functional requirements. Small cells such as those found in gate arrays tend to require complex and irregular interconnections which increase the difficulty of testing.

Employing standard cells which have been previously used, verified and tested leads to a more reliable chip. Architectures supported via mature silicon compilers and assemblers are desirable, since they tend to minimize human design errors, though at the expense of increased silicon area. Yield and reliability tradeoffs should be evaluated for each design.

3.6.2 Circuit Partitioning (8.3.2). Certain complex structures are known to be difficult to test and should be eliminated by appropriate partitioning. A well known example is a long counter chain which can be made more testable by

breaking it into a set of short counters that can be tested separately. Several general approaches to circuit partitioning to improve testability have been proposed. The COMET technique developed at Bell Laboratories for board-level circuits partitions the circuit into subcircuits of similar complexity to allow efficient fault detection via a binary search technique. The IBM Selective Control technique allows subcircuits to be systematically enabled and disabled during testing, while simultaneously allowing direct injection and monitoring of test signals. This is similar to the level sensitive scan design method covered in Section 3.6.4. Circuits tested via built-in test methods such as syndrome testing. autonomous testing. or using built-in logic block observation circuits must be partitioned so that these techniques can be executed in an efficient manner. The requirements of fault tolerance and testability tend to conflict, since fault tolerance. especially that of the static masking variety such as triple modular redundancy, is designed to conceal the effects of faults that testability is intended to uncover. Redundant circuitry used for fault masking can be tested by temporarily disconnecting it during testing. To test a triple modular redundancy circuit, for example, in which three copies of a particular unit U are attached to a voter, control signals should be provided for disabling the outputs of any two copies of U while the third copy is tested.

3.6.3 Built-in and External Testing (8.3.3). The available testing techniques for digital circuits are discussed in Section 3.2.2. The methods selected for testing a particular CLSIC depend primarily on its structure and its fault detection requirements. Built-in testing has the advantage over external testing in that the time during which a fault remains undetected (the error latency) can be kept small. Means must be provided for controlling the execution of the built-in test. This may be done via an on-chip test controller or by the automatic test equipment. Compatibility between the built-in test features and external automatic test equipment usually requires that they use test signals having the same electrical and timing characteristics. A mechanism should be provided for allowing the external tester and the built-in test circuitry to be synchronized. This can be done either by making the CLSIC's internal clock signal. if any, available at an external pin, or by permitting the external tester to disable the on-chip clock and replace it with its own clock signal. Built-in test circuits consume power if continuously energized, 60 design consideration should also be given to selectively enabling those circuits.

3.6.4 Test and Control Point Allocation (8.3.4). Appropriate sites for test and control points include the following: memory elements determining the circuit's major control state, major signal transfer paths such as busses,

deeply buried component, subcircuits of very high fan-out or fan-in. on-chip clocks, feedback paths, and redundant subcircuits. Less obvious locations can be identified by analyzing the circuit with a program like SCOAP, which assigns numbers denoting relative observability and controllability to every line in the circuit (see Section 3.4). A method has been developed that can be used to automatically identify control and test points. In this method, the computation of testability measures like those computed by SCOAP are formulated as an integer linear programming problem, and control and test point locations are found which minimize an objective function which is related to testability. If a circuit is unstructured. the number of test and control points needed may exceed the number of test pins or pads permitted by the IC technology and packaging method used. In that case, it may be possible to connect all or some of the test and control point sites to a small time-shared bus which is made externally accessible. A multiplexer can also be used to scan the test points sequentially. A structured design method like level sensitive scan design or SCAN/SET solves the test and control point problem. while simultaneously simplifying the test generation problem. The basic idea is to design a logic circuit so that. during testing, all its memory elements can be linked together to form a shift register S. The rest of the circuit then constitutes a large combinational circuit C. Input test data are shifted serially into S (scan in), and the resulting responses are shifted serially out of S (scan out). A control line is required to switch the circuit from normal to test mode. One of the two additional lines (which may be functional lines of the circuit) is needed to access S. The scan-in/scan-out technique provides almost complete controllability and observability using the minimum number of test points and is now widely used in the computer industry. Its main disadvantage is the slow scan-in/scan-out process which makes testing slow if the number of memory elements or the number of test vectors is large. Also, some fault modes, such as delay faults, may not be detected because of the slow scan-in/scan-out process. This technique is generally suited to circuits of moderate complexity (no more than a few hundred flip-flops). It is unsuitable for circuits containing large random access or read only memories.

3.6.5 Test Memory Allocation (8.3.5). Built-in test generation algorithms and precomputed test data should be stored in programmable read only memories. These programmable read only memories may form part of the instruction-level main memory or the microinstruction-level control memory. Where microprogramming is employed, the use of control memory as a test memory is recommended, since it allows greater fault coverage and reduces error latency.

3.6.6 Self-Checking Circuits (8.3.6). A circuit is self checking if its output signals are encoded in some error-detecting code format. Normal outputs correspond to codewords; faults are indicated by the appearance of a noncodeword at the circuit's output. Typically, special encoding circuits are included in a self-checking circuit to encode its output signals. Decoding circuits (checkers) are needed to monitor the outputs in order to detect errors. Many coding schemes involve appending extra bits (check bits) to the ordinary outputs (information bits) of the circuit. Most are used in circuits that transmit or store data with little or no processing, e.g., busses and random access memories. Parallel data sources are typically checked using parity-check codes. e.g., Hamming codes, while serial data sources are typically checked by cyclic codes. Many special purpose codes are also known, e.g., residue codes which can be used to make certain types of arithmetic circuits self checking. The widely used coding techniques have the property that the encoding and decoding circuitry required to make a circuit self checking constitutes a relatively small part (e.g., 10 to 20 percent) of the total circuit size or chip area. Practical coding methods with this property are not known for complex or unstructured circuits such as control read only memories or general purpose (micro-) processors. These circuits can be made self checking via duplication. Error detection is then performed by a match circuit that compares each duplicated pair (x_i, x'_i) of output signals. The normal values assumed by (x_i, x'_i) are (0,0) and (1,1): the faulty values are (0,1) and (1,0), so that (xi, x'_i) defines a one-out-of-two code. Methods of making code checkers self checking are known for most commonly used codes, including m-out-of-n codes.

3.6.7 Initialization (8.3.7). In circuits with a small number of registers or flip-flops. initialization is best achieved by connecting them all to a common reset line which. when activated, sets every flip-flop to a predetermined state. Each individual storage element may be supplied with an (asynchronous) preset or preclear line to which the reset line can be connected. The reset line should be controllable by the internal or external test circuitry, so that it can be directly activated at the start of any testing period. It is usually not feasible to supply random access memories, stacks, and similar storage circuits with a single reset signal. In such cases, the registers controlling these circuits, e.g., the corresponding address register, should be reset. In general, all registers and flip-flops defining a circuit's major control state must be initializable Note that a level sensitive scan

design circuit is inherently initializable to any desired state. When fault analysis, simulation, and test generation are conducted. faults in the reset circuitry should be considered.

3.6.8 Interfacing To External Test Equipment (8.3.8). The functional, electrical, and mechanical interfaces of the CLSIC must be compatible with those of the automatic test equipment used to test it. The automatic test equipment interface specification may be determined from the manufacturer's literature. The major functional characteristics of interest are the automatic test equipment's fault coverage, fault resolution, and testing time, which must meet the testability specifications of the CLSIC. The automatic test equipment's compatibility with the CLSIC's built-in test features must also be considered. In particular, the automatic test equipment must be able to synchronize with the built-in test circuitry or, if necessary, disable the built-in test circuitry (see 3.6.3 in this appendix). The electrical interface factors to be considered include signal voltage levels, current sourcing and sinking limits, minimum pulse widths. and maximum clock rates. Mechanical considerations include the number, size, and location of the test probes connected to the CLSIC by the automatic test equipment.

3.6.9 Error Detection (8.3.9). Error indications produced by built-in test features must be communicated to the next higher level of on-chip or off-chip control. In a processor-based design, errors detected by circuits outside the controlling processor are communicated to it via interrupt request. Errors detected within the processor itself. especially software errors such as a divide by zero attempt, are termed traps rather than interrupts. Both traps and interrupts are handled by the processor temporarily suspending its current task and switching to an error-handling procedure. If rapid error response is required to prevent loss of information, the corresponding trap or interrupt request should be nonmaskable, and the error-handling routine should be noninterruptable. When many different trap or interrupt sources exist requiring different error-handling procedures. vectored interrupt control should be used, where the trap or interrupt source provides immediate identification of the error type to be processed. An example of a modern microprocessor with well designed interrupt and trap facilities is the Motorola 68000.

3.7 BUILT-IN TEST DESIGN (8.5)

The factors influencing the choice of the built-in test features to be used are discussed in Sections 3.5 and 3.6.

3.7.1 Functional Design (8.5.1). In designing a CLSIC chip to be testable, built-in test hardware as well as embedded firmware and software is often employed. The built-in test hardware is used for several purposes, such as to generate test data, to compact and process response data, to improve controllability and observability, to control the on-chip testing process. and to store and execute microdiagnostic test procedures. When used to process response data, failure indicator circuits are necessary. As the complexity of the built-in test hardware increases, then consideration as to its testing must also be addressed. Often, built-in test hardware is highly functional and can be tested as such. Also, much of this hardware is thoroughly tested while used in the testing of the CLSIC itself.

To reduce design time, eliminate design errors. and simplify the entire process of test generation and test analysis, standard built-in test features should be employed where applicable, such as counters, shift registers, parity circuits. comparators, and linear feedback shift registers for signature analysis and pattern generation.

3.7.2 Memory Allocation (8.5.2). Memory space is required for the storage and execution of test programs. The test programs and associated data are stored in nonalterable memory circuits (read only memories), while working space needed during test execution is assigned to read-write memories. The impact of the added memory on the reliability and testability requirements of the CLSIC should be assessed.

Microprograms may be stored in a conventional single-level control memory (microspore) M1. A saving in total memory size may be realized by using a two-level control approach in which the microspore control memory M1 is backed up by a second control memory or nanostore control memory M2. Two-level microprogrammed control is used in the Motorola 68000 microprocessor chip.

3.7.3 Word Allocation (8.5.2.1). Memory space must be allocated for the storage of (micro-) diagnostic programs that perform test initialization, fault detection and location. and error processing and notification. The design and organization of such programs is highly dependent on the circuit architecture used.

3.7.4 Bit Allocation (8.5.2.2). The number of check bits that must be added to data words to implement error correction/error detection coding techniques depends on the code used and can be found in any coding theory test. In the case of single-error correcting, double-error detecting, parity check codes. for example, the number of check bits C that-must be appended to n-bit data words is the smallest integer satisfying the relation

$$C \geq \log_2(n + C + 1)$$

Hence, if n = 32, then C = 6, which represents a word-size overhead of 19 percent. Error detection and partial error location can be obtained with fewer check bits by interleaving the check bits. For example, suppose that 32-bit data words are divided into four 8-bit slices, each of which is checked by a separate parity check bit, for a total of four check bits. This allows detection of all single-bit errors and all multiple-bit errors with at most one erroneous bit in each slice. Individual error bits can be resolved to the slice level.

3.7.5 Protection Allocation (8.5.2.3). Critical test routines are assigned to read only memories because they are nonvolatile and, for most IC technologies, are less susceptible to failure than alterable memories. Critical memories may be made self checking by the use of coding techniques, as discussed in Section 3.7.3. Interleaved parity check codes are widely used for control memories with large word size, because they require relatively few check bits.

3.8 TESTABILITY ANALYSIS (8.6)

At the completion of the functional design level, most design for testability issues should be resolved. These include how each subcircuit of the CLSIC is to be tested, how initialization is to be achieved, the type of built-in test features to be used, and the type and extent to which off-line test generation and simulation are to be employed. Some decisions may be required at the logic design level, such as where to place additional control and test points. Standard testing approaches should be used for each subcircuit structure so that fairly accurate predictions can be made at this functional design level for the testability measures. For example. using the level sensitive scan design philosophy can lead to nearly 100 percent fault coverage of the detectable single stuck-at faults, independent of the logic design.

At the logic design level, more accurate quantitative values for the required testability measures can be determined. At this level, exact fault coverage for most fault models can be

measured via analytical models or simulation techniques. Performance, area, and reliability measures can also be estimated.

Based upon the value of the measures obtained, tradeoffs between test strategies can be made. Also, the circuit may require a modification in its design or be partitioned differently for testing. The probability of a faulty chip passing a test can now be determined. If this value is not acceptable to the contracting agency, then some modification to the design, manufacturing process. or testing methodology is required.

3.9 TESTABILITY (9.1.1)

When conservative design techniques are employed, the number of faults and the failure rate can be reduced. Conservative timing tolerances can be used to minimize the effect of stray delays. Conservative signal tolerances can be used to minimize the effect of variations in signal levels within the CLSIC. It is known that some fault modes, such as opens and shorts in MOS devices, cannot be modeled directly via the classical stuck-at fault model. However, most of these faults are still detected by tests which detect the stuck-at faults, i.e., the stuck-at faults dominate most other faults. For those situations where this is not the case. then the occurrence of such faults can be minimized by employing appropriate layout design rules.

3.10 TESTABILITY ANALYSIS (9.1.2)

Once the physical design of the CLSIC is completed, the following testability measures can be determined: hardware circuit overhead, chip area overhead, software and firmware overhead, operating performance, fault resolution, and reliability overhead. The equations for calculating these measures are given in Section 3.2 of this appendix.

3.11 TEST VECTOR VERIFICATION (9.1.3)

Once the physical design of a circuit is complete. a detailed analysis of all fault modes is possible. Since the placement and routing of all circuit elements and interconnects are known, layout dependent faults such as shorts can now be identified. All structures for implementing logical primitives are now known. This also includes programmable logic arrays and read only memory characterization data. Fault coverage for various testing approaches and fault modes which were not determined during the testability analysis phase at the logic design level can now be accurately determined via fault simulation or any other testability evaluation approach which may be applicable.

THIS PAGE INTENTIONALLY LEFT BLANK

APPENDIX C

SPECIMEN GENERAL SPECIFICATION

FOR

CUSTOM LARGE SCALE INTEGRATED CIRCUITS FOR SPACE VEHICLES

USAGE OF THIS APPENDIX

Procurement of a specific CLSIC for space vehicle applications is based upon the contractor preparing a subcontract or a purchase order that would reference the detailed specification for the specific CLSIC. The detailed specification should address all of the technical requirements needed to procure the CLSIC. This appendix is intended to help in the preparation of the detailed specification by providing a general set of requirements for CLSIC in the correct book format. Note that many of the detailed requirements needed for a specific CLSIC are not included in this specimen general specification. The additional items that should be included, or considered for inclusion, in the detailed specification of a specific CLSIC are listed in Section 10 of this handbook. By arranging the detailed specification in the same format as this specimen general specification, the manufacturers and others using the detailed specification can easily recognize the process controls needed and can determine the total set of requirements for the specific CLSIC.

Although this handbook is intended for guidance, some contractors may elect to reference directly this specimen general specification in detailed specifications for a specific CLSIC. To accommodate that possibility, and to assure appropriate compliance by the supplier, the requirements in this appendix are stated using "shall."

1. SCOPE

1.1 Purpose. This process control specification sets forth the general requirements for the design, manufacture, and testing of custom large scale integrated circuits (LSICs). The requirements stated in the specification are a composite of those that have been found to be cost effective for high reliability space vehicle applications.

1.2 Application. The specimen general requirements covered by this specification are applicable to large scale integrated circuit devices intended for very high reliability applications. This specification is intended for reference in space vehicle specifications to incorporate the general requirement which are common to large scale integrated circuit devices intended for space vehicle applications. This specification may also be used to specify requirement for large scale integrated circuit devices to be used on launch vehicles. missiles, or other vehicles requiring very high reliability devices. For those applications, the term “space vehicle” is to be interpreted as the applicable vehicle or equipment.

This specimen general specification is also intended for reference in requirement documents used for procuring specific LSICs to incorporate general requirements that may be applicable. The requirement document for procuring a specific LSIC is identified herein as a detailed specification, although it could be a specification control drawing, or a source control drawing, rather than a detailed specification.

This specimen general specification may also be referenced in detailed specifications for any complex microcircuit device in order to incorporate applicable requirements. In that case, LSIC is to be interpreted as the item or device covered by the detailed specification.

2. APPLICABLE DOCUMENTS

2.1 Issues Of Documents. The following documents of the issue in effect on the date of invitation for bids or request for proposal, form a part of this specification to the extent specified herein.

SPECIFICATIONS

Military

MIL-M-55565	Microcircuits Packaging of

STANDARDS

Federal

FED-STD-209	Clean Room and Work Station Requirement, Controlled Environment

Military

MIL-STD-129	Marking for Shipment and Storage
MIL-STD-883	Test Methods and Procedures for Microelectronics

HANDBOOKS

DOD-HDBK-263	Electrostatic Discharge Control Handbook for Protection of Electrical and Electronic Parts, Assemblies and Equipment

(Copies of specifications, standards, drawings, and publications required by contractors in connection with specific procurement functions should be obtained from the contracting office or as directed by the contracting officer.)

3. REQUIREMENTS

3.1 Flight Accreditation. LSICs furnished under this specification. or under associated detailed specifications. shall be flight accredited. LSICs are flight accredited if the LSICs satisfy all of the following conditions or the conditions have been waived by the contracting officer:

a. The design baseline and manufacturing baseline processes used for the LSICs have been audited by the assigned audit teams and have been approved by the contracting officer (see 4.3).

b. The LSICs have passed the specified product evaluation tests (see 4.4).

c. The LSICs have passed the Specified post-assembly screening tests (see 4.5).

d. The LSICs are from a production lot that passed the specified lot conformance tests (see 4.6).

e. The LSICs have been transported, handled, and stored within the specified nonoperational environmental limits.

f. No unresolved generic failures have been identified in devices using similar designs or manufacturing processes that would jeopardize the high reliability prediction for the LSIC.

3.2 Order of Precedence. In the event of conflict between the documents referenced herein and the contents of this specification, the contents of this specification shall be considered the superseding requirements.

3.3 Manufacturing. All manufacturing and assembly processes required by this specification shall be accomplished within the United States and its territories.

3.3.1 Processes and Controls. The manufacturing of LSICs shall be accomplished in accordance with documented procedures and process controls. These manufacturing processes and controls shall provide a manufacturer controlled baseline that assures subsequent production items can be manufactured that are equivalent in performance, radiation hardness, quality, and reliability to initial production items. These process controls shall be documented to give visibility to the procedures and specifications by which all processes, operations, inspections, and tests are to be accomplished by the manufacturer. This

internal manufacturer documentation shall include the name of each part or component, each material required, the point it enters the manufacturing flow, and the controlling specification or drawing. The documentation shall indicate required tooling. facilities, and test equipment; the manufacturing check points; the quality assurance verification points; and the verification procedures corresponding, to each applicable process, or material listed. The specifications, procedures, drawings, and supporting documentation shall reflect the specific revisions in effect at the time the LSICs are produced. When approved by the audit team or the contracting officer, these flow charts and the referenced specifications, procedures, drawings, and supporting documentation become the manufacturing baseline for process control and shall be retained by the manufacturer for reference. It is recognized that many factors may warrant making changes to this documented baseline; however, all changes to the baseline processes used, or the baseline documents used, shall be recorded by the manufacturer following the production of the first lot. These changes provide the basis for flight accreditation of subsequent production lots, so the changes should be approved by the contracting officer or his designated representative prior to implementation.

3.3.2 Production Lots. LSICs and their subelements shall be grouped together in individual lots during the various stages of manufacturing to assure that all LSICs in a production lot are fabricated and assembled during the same time period using the same production materials, equipment, methods, personnel, and controls. The wafers that are processed as a group shall be identified as a wafer lot. Each wafer lot shall be assigned a unique wafer lot number. Chips from a single wafer lot may be assembled into one or more production lots. A production lot shall not be assembled using chips from more than four wafer lots. In some LSICs, where the radiation response to one or more specified radiation environments is known to be largely variable from one wafer to the next within a diffusion lot, the production lot shall be controlled to provide traceability to the devices fabricated from a single wafer. Each production lot shall be identified by a unique lot date code. A serial number shall be assigned to each LSIC in each production lot at an appropriate point in the manufacturing flow. The serial number should be assigned such that each device is traceable to the individual wafer. As a minimum, the serial number shall be traceable to the wafer lot and shall be assigned prior to post-assembly screening tests.

3.3.2.1 Lot Date Code. The lot date code is a number that indicates the year, calendar week, and sequence letter indicative of the manufacturing period. The first two digits in the lot number shall be the last two digits in the number of the year, and the third and fourth digits shall indicate the calender week of the year. When the number of the week is a single digit, it shall be preceded by a zero. When more than one lot of a type are manufactured within the same week, a lot suffix letter shall be added at the end of the lot date code number for the second and subsequent lots to indicate the manufacturing sequence for the various lots that were manufactured during that week. The calendar week shall indicate either the first week or the last week of the period during which the devices were sealed.

3.3.2.2 Production Lot Traceability. The manufacturer's records shall identify, for each production lot of finished product, the following items as a minimum:

a. The part number (or detailed specification number), the lot date code, and the serial numbers of all LSICs in the lot

b. The date of completion of lot conformance tests (if applicable)

c. The post-assembly screening and lot conformance tests performed on the lot, and summaries of the test results for each device (or the read and record data if it is required by the tests)

d. Traceability data of each device to its wafer lot or preferably to an individual wafer

e. The pertinent specifications or control drawings under which inspections were performed

f. The identification, revision letter. and date of the manufacturing baseline used for the lot. A lot traveler containing the process history referenced to the process documentation may be used to establish the manufacturing baseline.

g. Final disposition of the lot (withdrawn, not accepted, accepted)

3.3.2.3 Lot Travelers. The manufacturer shall maintain lot travelers to document the completion of each required processing step from wafer diffusion through LSIC post-assembly screening tests. Traveler(s) shall provide for the following

information: dates, operations performed, operator's name or identification, and quantity of parts into and out of each operation. The lot traveler(s) shall accompany the lot through assembly and testing.

3.3.3 Fabrication and Handling.

3.3.3.1 Protection Against Electrostatic Discharge. LSICs shall be protected from electrostatic discharge by utilizing appropriate procedures and guidance information contained in DOD-HDBK-263.

3.3.3.2 In-process Handling and Storage. In-process handling and storage shall be in accordance with documented procedures that prevent LSIC degradation or damage. Chips, LSIC subassemblies, and LSICs shall be transported and stored in conductive carriers or containers that provide physical protection. As a minimum, the handling and storage procedures shall provide for:

a. The control of environments including temperature, humidity, contamination, and pressure

b. Measures to segregate discrepant devices from accepted devices

c. The use of protective cushioning and containers during transportation and storage

d. Control measures to limit access of personnel to LSICs which have been inspected and stored

e. Provisions to prevent contact with LSICs by bare hands during handling, inspection, and tests

f. Provisions for protection from damage by electrostatic discharge in accordance with the information in DOD-HDBK-263. For example, all external leads of the LSIC or subassemblies should be shorted together. Also, bonders. pellet pickup tools, table tops, trim and form tools, sealing equipment, and other equipment used in chip or LSIC handling should be properly grounded.

3.3.3.3 Facility Cleanliness. LSICs shall be fabricated in clean areas with dust control provisions. Chemical vapors shall be vented outside the fabrication areas away from any inlet duct. Critical wafer fabrication processes such as masking, diffusion, and photolithography shall be accomplished

in clean room areas where the dust levels do not exceed the requirements of FED-STD-209, Class 100. All assembly operations up to and including final sealing shall be accomplished in clean room areas where the dust levels do not exceed the requirements of FED-STD-209, Class 10,000. and shall have laminar flow benches at die attach. wire bond. and precap inspection. The dust levels at the work space of the laminar flow benches shall not exceed the requirements of FED-STD-209, Class 100. Manufacturing and test operations. subsequent to final sealing. may be accomplished in a normal noncontrolled environment.

3.3.3.4 Certified Operators and Production Inspectors. All critical processes and all production inspections shall be performed by personnel who have been certified by the manufacturer to perform their assigned task in accordance with the applicable in–house standards. The manufacturer's in-house standards, including certification procedures, shall be documented and available for review. For certification purposes. the critical processes are: oxidation. diffusion, implantation, chemical vapor disposition, metallization, die mount, internal wire bonding, internal preseal visual examination (pre-cap), sealing, radiographic examination, and testing. Production inspections are those that are conducted by personnel assigned to the production department (as distinguished from quality assurance department inspections).

The certification of these personnel shall include a formal training and testing procedure to assure the proficiency of each individual. Records shall be maintained for each individual to indicate the type and date of training received and to document their performance.

Recertification of personnel shall be performed annually to assure a continuously high level of competence. Personnel who fail to meet the requirements of certification or recertification, or whose manufacturing performance indicates poor proficiency. shall be removed from the production of LSICs.

3.3.4 Device Cleanliness. The particulate cleanliness shall be maintained such that there are no conductive foreign particles. attached or not, on the surface of the die or within the package or on the lid or cap that are large enough in any dimension to bridge the narrowest unglassivated operating metal spacing, wire spacing, or biased unpassivated die area spacing or any combination thereof. Also, no particle shall be larger than 3 roils in any dimension even if otherwise meeting the foregoing criteria. Silicon chips and silicon-gold eutectic slag shall be considered as conductive foreign particles. Laser scribing shall not be used on silicon wafers. External surfaces shall be visibly clean.

3.3.5 Independent Monitoring. Facilities and inspection stations shall be provided in the manufacturing area for the surveillance and monitoring of critical operations by representatives of the contracting officer or by an independent monitoring organization approved by the contracting officer.

3.3.6. Rework. Rework is not allowed on wafer metallization. oxidation, or passivation. Photoresist rework is permitted. No delidding or package opening for rework shall be permitted. Allowable rework of sealed packages includes recleaning of the LSIC or portion thereof, rebranding to correct defective marking, and lead straightening (provided the reworked devices meet the requirement conditions of leads), unless otherwise specified. Nonconforming units that are reworked or refurbished so they can be used in ground tests shall be clearly identified as “NOT FOR FLIGHT" (see 3.8.3).

3.3.7 Craftsmanship. LSICs shall be manufactured, processed, tested, and handled such that the finished items are of sufficient quality to ensure reliable operation, safety, and service life. The LSICs shall be free of defects that would interfere with operational use such as excessive scratches, nicks, burrs, loose material, contamination. and corrosion.

3.4 General Design Requirements. The general design shall be in accordance with documented design rules and design tools reviewed by the assigned design audit team and approved by the contracting officer. The LSIC design shall incorporate test points and self-test features to the extent practicable. The goal shall be to incorporate test capabilities to make the LSIC fully testable. The wafer layout shall also incorporate relevant test features, test structures, and test chips to aid in evaluating and controlling the manufacturing processes.

3.4.1 Standard Cells. Where practicable, the LSIC shall use standard cells organized in simple regular patterns rather than randomly structured circuitry or nonstandard cells.

3.4.2 Circuit Partitioning. The LSIC shall be partitioned into subcircuits or groups of cells to maximize the testability and to minimize the pin count of the package. Where practicable, independent testing provisions shall be provided for redundant circuitry.

3.4.3 Test Features. To the extent practicable, test features shall be incorporated on the wafer and in the design of the chip to allow monitoring of critical parameters and performance margins. Critical parameters include sheet resistance, linewidth uniformity, photomask alignment. contact resistance, minority carrier lifetime, leakage current, and

random fault density. The test features may include probe pads, data paths, internally generated test signals, internal monitoring circuits, and other types of test structure. Extra probe pads shall be provided where practicable to allow confirmation of probe-to-pad continuity. Modular test structures, such as those developed by The National Bureau of Standards, having integral probe pads arranged in a standardized configuration shall be used, where practicable. Reliance on the post-assembly screening tests to detect discrepant devices shall be reduced to the extent practicable by the use of design features and test structures that can be used for in-process controls, inspections. or tests.

3.4.4 LSIC Testability. To the extent practicable, the LSIC shall be designed with self-test features that can verify functional performance or identify any failures including any intermittent failures. LSIC functions that do not have self-test features shall have data paths to external pins to accommodate the injection of test signals and the monitoring of the device response so performance can be measured and internal faults detected.

3.4.5 Test Structures. Test structures consisting of applicable integrated circuit elements shall be designed and included in appropriate locations on each production wafer to provide critical data for the control of the fabrication processes.

3.4.6 Test Chips. Test chips shall be substituted as a test surrogate for a production LSIC at one or more selected sites on each production wafer. The test chips shall be an assemblage of the LSIC circuit elements and the test structures selected to monitor the fabrication processes. A minimum of five test chips per wafer lot shall be assembled into packages and identified as the Test Chip Evaluation Samples for that wafer lot.

3.4.7 Selection of Parts, Materials, and Processes. Unless otherwise specified in the contract, the parts, materials, and processes shall be selected and controlled in accordance with contractor established and documented procedures to satisfy the specified requirements. The selection and control procedures shall emphasize quality and reliability to meet the requirements. The parts, materials, and processes selected shall be of sufficient proven quality to allow the LSICs to meet the functional performance, reliability, and strength as required during the anticipated life cycle. including all environmental degradation effects. Care shall be exercised in the selection of materials and processes to avoid the generation and entrapment of loose particles or contamination that could cause failures in a space environment.

Parts, materials, and processes shall be selected to ensure that any damage or deterioration from the space environment or the outgassing effects in the space environment, would not reduce the performance of the LSIC beyond the specified limits.

3.5 Detailed Design Requirements.

3.5.1 Die.

3.5.1.1 Internal Conductors. Internal thin film conductors on silicon die or substrate (metallization stripes, contact areas, bonding interfaces, etc.) shall be designed so that no properly fabricated conductor shall experience in normal operation (at worst case specified operating conditions) a current density in excess of the maximum allowable value shown in Table C-I for the applicable conductor material.

The current density shall be calculated at the point(s) of maximum current density (i.e., greatest current per unit cross section) for the specific device type and schematic or configuration. The current density calculation shall:

a. Use a current value equal to the maximum continuous current (at full fanout for digitals or at maximum load for linears) or equal to the simple time-averaged current obtained at maximum rated frequency and duty cycle with maximum load. whichever results in the greater current value at the point(s) of maximum current density. This current value shall be determined at the maximum allowed supply voltage(s) and with the current assumed to be uniform over the entire conductor cross-sectional area.

b. Use the minimum allowed metal thickness per manufacturing specifications and controls. This minimum shall include the metal thinning which occurs at steps on the surface or at any other locations.

c. Use the minimum conductor widths (not mask widths) including appropriate allowance for narrowing or undercutting experienced in metal etching.

d. Not include areas of barrier metals and nonconducting material in the calculation of conductor cross section.

3.5.1.2 Metallization. The minimum metallization thickness shall be 0.8 micrometer for single level metal and for the top level of multilevel metal. Except for test structures, there shall be no metallization in the streets between dice.

TABLE C-I. Allowable Current Density.

CONDUCTOR MATERIAL	MAXIMUM ALLOWABLE CURRENT DENSITY (amperes per sq. cm)
Aluminum (99.99 percent pure or doped) without glassivation	1×10^5
Aluminum (99.99 percent pure or doped) glassivated	2×10^5
Gold	6×10^5
All others (unless otherwise specified)	2×10^5

3.5.1.3 Input Protection. Input protection circuits to prevent device failure due to electrostatic discharge shall be used on each input lead except where speed degradation due to input protection would cause the circuits to be unacceptably slow.

3.5.1.4 Pad Size. The metallization pad, exposed through the glassivation layer, shall be a minimum of 0.003 X 0.003 inch (0.0076 X 0.0076 cm).

3.5.1.5 Pad Spacing. The minimum spacing between exposed pad metallization to other exposed pad metallization shall be 0.003 inch (0.0076 cm).

3.5.1.6 Passivation. The distance between the edge of the surface passivation and the cut edge of the die (after dicing) shall be a maximum of 0.001 inch (0.0025 cm). The surface passivation shall extend to a minimum of 0.002 inch (0.0051 cm) beyond the edges of the metallization pads.

3.5.2 Die Mount. A metallurgical die mount shall be employed.

3.5.3 Internal Wire Size and Material. The internal lead wire shall be of the same metal composition (±5 percent) as the die pad metallization. The internal wire diameter shall be 0.001 inch, minimum (0.025 mm). Internal lead wires or other conductors which are not in thermal contact With a substrate along their entire length (such as wire or ribbon conductors) shall be designed to experience, at maximum rated current, a continuous current for direct current, or an RMS current for alternating or pulsed current, not to exceed the values established by the following relationship:

where: I = maximum allowed current in amperes

d = diameter in inches for round wire (or equivalent round wire diameter which would provide the same cross-sectional area for other than round wire internal conductor)

K = a constant taken from Table C-II for the applicable wire or conductor length and composition used in the device

TABLE C-II. K Values

WIRE COMPOSITION	"K" VALUES FOR BOND-TO-BOND LENGTH EQUAL OR LESS THAN 0.040 inch (0.10 cm)	"K" VALUE FOR TOTAL CONDUCTOR LENGTH GREATER THAN 0.040 inch (0.10 cm)
Aluminum	22,000	15,200
Gold	30,000	20,500
Copper	30,000	20,500
Silver	15,000	10,500
All other	9,000	6,300

3.5.4 Package

3.5.4.1 Package Materials. Devices shall be hermetically sealed in cases of glass, metal, ceramic, or combinations thereof. The package materials shall be corrosion resistant or suitably treated to resist corrosion when subjected to the specified environments.

3.5.4.2 Sealing. LSICs shall be sealed using only metallurgical sealing to ensure protection from external environments and to contain internal gases. Plastic cases are prohibited. The maximum leak rate using helium shall be less than 0.01 atmospheric cubic millimeters per second when subjected to a pressure differential of 101.3 ± 10 kilopascals. The internal moisture content of the packages subsequent to sealing shall not exceed 3000 ppm at 100 deg C. The sealing of all LSICs in a single production lot shall be accomplished in a timely manner, and in no case shall it extend longer than six weeks.

3.6 Performance Requirements. The supply power and performance requirements shall be as specified in the detailed specification.

3.7 Environmental Design Requirements. The LSIC shall be designed to function as specified when exposed to environmental levels within the range of levels specified. Or within the range expected during its service life. whichever is more severe.

3.7.1 Nonoperational Environments. LSICs shall be designed to function within performance specifications after exposure to environmental levels that exceed the extremes of the predicted nonoperational environments specified. The LSICs shall also be capable of functioning within specifications after exposure to the environments generated during device mounting and lead termination.

3.7.1.1 Temperature. The LSIC shall be capable of sustaining thermal environments that are between -65 deg C and +150 deg C.

3.7.1.2 Humidity. The LSIC shall be capable of sustaining exposures up to 12 hours to moderately humid or mildly corrosive environments, such as industrial environments or sea coast fog, without generating destructive corrosion.

Destructive corrosion shall be construed as being any type of corrosion which interferes with meeting the specified performance and intended application of the LSIC or its associated parts.

3.7.1.3 Pressure. The LSIC shall be capable of operating in environments which range from a pressure of 200 kilopascals to pressures that are less than 133 micropascals. The LSIC shall also operate satisfactorily when the pressure varies from one extreme to the other extreme in one minute.

3.7.1.4 Shock. The LSIC shall be designed to operate satisfactorily when exposed to five mechanical shocks of 1500 g peak, sequentially applied in 0.0005-second pulses in any direction.

3.7.1.5 Acceleration. The LSIC shall be capable of sustaining steady acceleration of up to 30,000 g applied in any direction for one millisecond.

3.7.2 Operational Environments. The LSIC shall be designed to function within performance specifications when exposed in the operational configuration to environmental levels within the maximum predicted range of environments specified, or within the range of operational environments, whichever is more severe. The operational environment include temperature and radiation.

3.7.2.1 Temperature. The LSICs shall operate at any temperature within their thermal design range. Unless otherwise specified, the thermal design range, measured at the mounting surface of the case, shall not be less than from -55 deg C to +125 deg C. In addition, the LSIC shall operate satisfactorily while exposed to 100 thermal cycles where the temperature varies at a rate of at least 3 deg C per minute from one extreme of the thermal design range to the other.

3.7.2.2 Radiation. The LSIC shall meet the radiation requirements specified in the detailed specification.

3.8 Marking.

3.8.1 Identification. A unique identification shall be marked directly on each LSIC. The marking shall utilize suitable letter size and contrasting colors. contracting surface finishes, or other techniques to provide identification that is readily legible. The marking shall be capable of withstanding cleaning procedures and environmental exposures anticipated during the service life of the LSIC without

becoming illegible. Where practicable, identification shall be in locations which permit observation of the marking at the next higher level of assembly The identification marking should contain, as a minimum, the following:

a. Reference to this specification number

b. Contractor part number

c. Device type or manufacturer's part number

d. Production lot date code

e. Device serial number

f. Manufacturer (or manufacturer identification)

Where practicable, the marking should also indicate the input voltage, the maximum operating temperature, and applicable radiation hardness.

When size limitations. cost, or other considerations preclude marking all applicable information on an LSIC, the marking may simply provide a reference key to a data card that would accompany the device.

The marking of any two or more LSICs intended for space applications with the same identification (except for lot date code and serial number) shall indicate that they may be capable of being changed, one for another, without alteration of the LSICs themselves or of adjoining components, if the LSICs also meet the specified flight accreditation requirements (see 3.1).

3.8.2 Index Point. An index point, tab. or mark that is visible after mounting shall be provided to indicate the starting point for numbering leads and for mechanical orientation.

3.8.3 "NOT FOR FLIGHT" Marking. LSICs which by intent or by material disposition are not suitable for use in flight, and which could be accidently substituted for flight or flight spare hardware, shall be red tagged or striped with red paint or both, to prevent such substitution. The red tag shall be conspicuous and marked "NOT FOR FLIGHT." The red paint shall be material compatible and the stripes unmistakable.

3.9 Operability

3.9.1 Reliability. The reliability goal for successful operation of each LSIC shall be at least 0.999 at 95 percent confidence. If a higher reliability is required by a program, the higher figures shall be specified in the detailed specification.

3.9.2 Service Life. LSICs shall be designed for a service life of 20 years, where practicable. The service life starts with the completion of assembly as indicated by the date code included in the lot number and ends with the last operational usage for units from that production lot.

3.9.3 Storage. Flight accredited LSICs awaiting shipment or use shall be stored in locked storerooms in sealed packages. Only antistatic wrapping material shall be used. Stocking procedures, packaging, and labeling shall be designed to minimize handling and possible handling damage during inventory or stock removal.

4. QUALITY ASSURANCE PROVISIONS

4.1 Reponsibility for Inspections and Tests. Unless otherwise specified in the contract or purchase order, the manufacturer is responsible for the performance of all inspection and test requirements as specified herein. Except as otherwise specified in the contract or order, the manufacturer may use his own or any other facilities suitable for the performance of the inspection and test requirements specified herein. unless disapproved by the government. The government reserves the right to perform any of the inspections set forth in the specification where such inspections are deemed necessary to assure that supplies and services conform to prescribed requirements.

4.2 Classification of Inspections and Tests. The tests and inspections specified herein are classified as follows:

a. Parts, materials, and process controls (4.3)

b. Product evaluation tests (4.4)

c. Post-assembly screening tests (4.5)

d. Lot conformance tests (4.6)

e. Qualification tests (4.7)

4.3 Parts, Materials, and Process Controls. The contractor shall verify that the LSIC design was accomplished using the design baseline (i.e., the design, design tools, design rules, and processes) approved for the device type either by the contracting officer or by an approved design audit team. The contractor shall verify that the manufacturing baseline (i.e., the manufacturing facility, test facilities. manufacturing equipment, tooling, baseline processes, test equipment, and controls) used for manufacturing the LSICs have been approved either by the contracting officer or by an approved manufacturing audit team. The part controls, material controls, and process controls are to be performed to the baseline requirements on each production lot to ensure that reliable LSICs are fabricated. All materials shall be adequately controlled and inspected prior to assembly. During fabrication, the tools and processes, as well as parts and materials, shall be adequately controlled and inspected to assure compliance with the approved manufacturing processes and controls.

4.3.1 Records. Records documenting accreditation status (see 3.1) shall be maintained following assignment of the lot date code to each production lot. The inspection records and test records shall be maintained by LSIC serial number to provide traceability data for the service life of each device in each production lot. Traceability of the piece parts used for each production lot shall be maintained. The complete design baseline, manufacturing baseline, and detailed manufacturing records on each production lot shall be retained for at least seven years and shall be available for review. The records shall indicate compliance with the documented manufacturing baseline, including all relevant test data, and all rework or modifications.

4.3.2 Inspector Certification. All quality assurance inspections shall be performed by personnel who have been certified by the manufacturer to perform their assigned task in accordance with the applicable in-house standards. These in-house quality assurance standards, including certification procedures, shall be documented.

The certification of personnel shall include a formal training and testing procedure to assure the proficiency of each individual. Personnel satisfactorily completing the training and the required tests shall be given a card, badge, or similar objective evidence of certification. The date of last certification and the period of effectivity of the certification shall be indicated on the card or badge. Records shall be maintained for each individual to indicate the type and date of training received and to document their performance.

Each individual shall be retested at the end of the designated certification period for recertification. Personnel failing certification or recertification, or whose quality assurance performance indicates poor proficiency, shall be removed from the inspection of LSICs.

4.3.3 Manufacturing Controls. Each production lot of LSICs shall be subjected to in-process production screens to assure compliance with the established manufacturing baseline and the specified requirements. Compliance with the documented process controls, documented screening requirements. required hardware configuration, and general workmanship requirements shall be verified.

4.3.3.1 Wafer Lot Acceptance. LSICs submitted for post-assembly screening or lot conformance tests shall be assembled from wafer lots which meet the requirements of Method 5007. MIL-STD-883. The five or more test chips per wafer lot that were assembled into packages and identified as the Test Chip Evaluation Samples for that wafer lot shall be subjected to evaluation tests including a life test. Unless otherwise specified, the life test shall be in accordance with MIL-STD-883, Method 1005, Condition D or E, for 500 hours at 150 deg C or for 1000 hours at 125 deg C minimum. The alternate removal-of-bias provisions shall not apply if the test is run at a temperature above 125 deg C. The indicator parameters specified in the applicable detailed specification shall be read and recorded before and after the life test. If one or more devices fail, as a result of design or generic manufacturing problems, the entire wafer lot shall be rejected.

4.3.3.2 Equipment Verification. The manufacturer shall define and utilize a method to periodically verify the operational characteristics of the equipment used during manufacturing.

4.3.3.2.1 Wire Bonding Machine Tests. Each wire bonding machine, when in use, shall have two device or test samples taken and destructively tested at the start of production on each shift, also after any nondestructive test failure, also after four hours of operation, and also when operators, wire, or device types are changed. The device or test samples may be electrical reject die from the same wafer lot as the devices being manufactured. The destructive wire bond test shall be conducted on five wires (as a minimum) of each sample microcircuit in accordance with the requirements of MIL-STD-883, Method 2011, Condition D. Pull strength data shall be read and recorded. The force required for failure. the physical location of the point of failure, and the nature of the failure shall be recorded. The data shall be plotted to

show statistical trends and limits for each bonding machine. Records shall also indicate the action taken when each out-of-control condition is observed. In the event that any bond pull fails the test, the wire bonder shall be inactivated immediately and shall not be returned to production until tests show that satisfactory operation has been established. The samples used in the destructive wire bond tests may, in addition, be used for die shear tests.

4.3.3.2.2 Die Shear Test. At each station that is performing the die to case attachment operation. one completed sample, as a minimum, shall be tested. in accordance with Method 2019 of MIL-STD-883, at the start of each attachment run. This test shall be repeated every two hours during the run, as a minimum, and at the close of the attachment run. The die-to-case shear test shall also be performed on destructive wire bond pull samples used to verify satisfactory operation of the wire bonding machines and on destructive physical analysis samples. The criteria for failure of this test shall be the same as in Method 2019 of MIL-STD-883 except that:

a. Shattered die particles shall remain attached to 75 percent, as a minimum, of the design attach area (instead of 50 percent).

b. The acceptable minimum die shear failure force shall be 50 percent of that shown in Figure 2019-4 of Method 2019.

In the event that a unit fails to meet these criteria. those units which were assembled since the last satisfactory test shall be rejected.

4.3.3.3 Package Lot Control. Materials for use in packages shall be separated into lots not exceeding 1500 packages per lot. They shall be subjected to 100 percent visual examination and to sample mechanical and mensuration tests. Each lead of each package shall be electrically tested at a minimum of 500 Vdc, and the current (leakage) to the case or any other lead shall not exceed 0.1 microampere.

4.3.3.4 Contamination Monitoring. All gases, fluids, and critical materials used in the manufacture of LSICs shall be monitored for contamination levels on a periodic basis. The test sensitivity and frequency shall be such that any trend towards an out-of-tolerance condition can be corrected in a timely manner. Particulate levels shall be determined for all assembly areas on a daily basis.

4.3.3.5 Nondestructive Bond Pull Test. Each bond in each LSIC shall be subjected to a nondestructive bond pull test preformed in accordance with MIL-STD-883, Method 2023. The total number of failed wires and the total number of devices failed shall be recorded. The lot shall have a percent defective allowable (PDA) of 2 percent based on the number of wires pulled in a specified lot.

4.3.3.6 Preseal Visual. Each LSIC shall be subjected to a preseal inspection in accordance with MIL-STD-883, Method 2010, Condition A low power and high power criteria. The high power criteria shall be as modified in the approved manufacturing-baseline screening procedure and detailed specification. Built-in test features, custom design features, longer burn-in time, overvoltage stress during preceding burn-in, or other techniques shall be incorporated in the manufacturing baseline screening procedure to the extent practicable and safe to improve the reliability and reduce the reliance on high power preseal visual inspection requirements. However, the elimination or modification of a screening criterion shall be based upon documented data and analysis to assure that the intended reliability level is achieved.

4.4 Product Evaluations. Prior to finalizing the post-assembly screening tests and the lot conformance tests, including the associated pass-fail criteria, a product evaluation is required. The product evaluation shall be adequate to demonstrate the suitability of the LSIC to meet its specifications and perform its mission. Test units for the product evaluation shall be sufficiently similar to the final production units so as not to jeopardize the validity of the test results. Similar LSICs that have been previously flight accredited or qualified usually provide the basis for initial product evaluation. Deficiencies in meeting all requirements may be fulfilled by supplementing the existing data with new test data. However, reevaluation testing is required for LSICs that incorporate extensive changes in design, manufacturing processing, environmental levels, or other requirements. The final product evaluation tests are usually combined with the post-assembly screening and lot conformance tests of the first production lot to reduce the total test program. However, the total test program shall satisfy all requirements specified for product evaluation as well as for post-assembly screening tests.

4.4.1 Physical Evaluation Tests. Evaluation tests of the LSIC shall be performed to demonstrate compliance of new or unqualified physical design features with the specified design requirements.

4.4.2 Electrical Tests and Criteria. Electrical tests shall be performed to demonstrate compliance with the specified functional and parametric requirements and to develop applicable pass-fail test criteria for post-assembly screening tests and lot conformance tests. Electrical testing shall be performed over the specified range of temperature, voltage, and frequency to validate the static, dynamic, switching, and functional behavior of the LSIC.

4.4.2.1 Characterization. Prior to, or as part of the production phase, at least two samples per lot of each LSIC shall be functionally characterized over and beyond the full temperature, speed, and voltage range specified to determine if any malfunctioning condition exists within or at the limits defined by specified end points. At least two lots shall be sampled. Tests beyond the specified end points shall be performed to provide information regarding potential marginal design within the LSIC. Samples shall also be characterized subsequent to burn-in and life test in order to develop information on the stability of the LSICs.

Two - and three-dimensional data plots ("Schmoo" plots) should be used to document the characterization. If marginal or nonfunctional domains within the operating limits are found. "Schmoo" plots covering the parameters of concern shall be prepared as part of the screening tests for each LSIC delivered to demonstrate acceptable performance over the full operating range. The delta limits to be specified for use in burn-in shall be developed by utilizing the characterization and reliability assessment data to determine the limits of acceptable parameter drift.

4.4.2.2 Input Protection. The effectiveness of the input protection circuitry to electrostatic discharge on the input leads shall be demonstrated.

4.4.2.3 Reliability Assessment. Preliminary burn-in and life tests shall be conducted on at least two samples of each LSIC type. test chip, or equivalent device(s) of the same complexity, technology, and design rules to establish the final burn-in and life-test circuits and circuit test conditions to be specified in the applicable test procedures. The preliminary burn-in and life tests shall be conducted at the maximum rated device voltage. Electrical parametric and functional testing shall be performed prior to and after the burn-in and life tests. Both static and dynamic burn-in tests are required.

4.4.2.4 Evaluation of Nonoperating Constraints. The effects of nonoperational environment on the LSICs may be determined by development tests. These tests would be used to identify fabrication storage, handling, transportation, installation, and launch preparation constraints or controls that may be necessary. Approval of the contracting officer is required if the test results indicate that it is necessary to provide special nonoperating environmental controls other than those specified herein.

4.4.3 Radiation Hardness Evaluation Tests. The radiation hardness of LSICs with radiation hardness requirements specified in the detailed specification shall be evaluated using prototype devices, test chips, or subcircuits of the LSIC. A minimum of five devices shall be tested in each radiation environment. Where practicable, the same device can be tested in more than one environment. These devices shall be tested to failure or to ten times the specification level, whichever is less. The data are used to determine if a redesign or change in construction or processing is necessary to meet the radiation requirements on the final product (see Appendix A).

4.5 Post-assembly Screening Tests. Unless modified by the approved manufacturing baseline or by the contracting officer, each production lot of LSICs shall be screened in accordance with the requirements specified, including the tests specified in Table C-III.

4.5.1 Lead Shearing and Forming. When lead shearing and forming operations are specified. a 100 percent fine and gross seal test shall be performed after those operations and prior to final visual inspection of these devices.

4.5.2 Particle Impact Noise Detection (PIND) Test. The production lot shall be submitted to PIND testing a minimum of three times and a maximum of five times in accordance with MIL-STD-883, Test Method 2020, Condition A. If on the first, second, or third runs the number of defective Parts is less than 1 percent per run of the number of parts submitted to the run (or one part, whichever is greater), then the lot shall be accepted. PIND prescreening shall not be performed. All defective parts shall be removed after each run. Production lots that do not meet the 1 percent (or one part, whichever is greater) of defective allowable (PDA) by the third run, or exceed 25 percent detectives cumulative, shall be rejected; resubmission is not allowed.

TABLE C-III. Post-Assembly Screening Tests

TEST	MIL-STD-883 METHOD	REQUIREMENT
(1) Stabilization bake (no end point measurements required)	1008, Cond. C, 24 hrs, min. 1/	100%
(2) Temperature cycling	1010, Cond. C	100%
(3) Constant acceleration	2001, Cond. E , Y1 orientation only. 2/	100%
(4) Particle Impact Noise Detection (PIND)	2020, Cond. A 3/	100% PDA 3/
(5) Interim (preburn-in) electrical tests	4/	100%
(6) Burn-in	1015, 240 hrs at 125°C min 5/	100%
(7) Interim (postburn-in) electrical tests	4/	100% PDA 5%
(8) Reverse bias	1015, burn-in 72 hrs at 150°C min 5/, 6/	100%
(9) Interim (postburn-in) electrical tests	4/	100% PDA 5%
(10) Seal (a) Fine and (b) gross	1014, 7/	100% PDA 5%
(11) Final electrical test	4/	
(a) Static tests	@ 25°C and at max and min operating temp. 4/	100% PDA 5%
(b) Dynamic tests or switching tests	@ 25°C and at max and min operating temp. 4/	100% PDA 5%
(c) Functional tests	@ 25°C and at max and min operating temp. 4/	100% PDA 5%
(12) Radiographic	2012, two views 8/	100%
(13) External visual	2009, 9/	100%
(14) Radiation	4/	100%

TABLE C-III. Post-Assembly Screening Tests (Continued)

Footnotes for Table C-III.

1/ It shall be permissible to divide the total minimum stabilization bake time between preseal and postseal bake as long as the total bake time equals or exceeds 24 hours, the postseal bake time equals or exceeds 16 hours, and the preseal bake occurs immediately prior to sealing.

2/ Mechanical shock (MIL-STD-883, Method 2002, Condition B) may be performed as an alternate, if specified in the applicable detailed specifications.

3/ The PIND test may be performed in any sequence after (3) and prior to (10). See paragraph 4.5.2 for PDA.

4/ Per applicable detailed specification

5/ Test Condition F of Method 1015 shall not apply. As an alternative, the test may be conducted for 150 hrs, min, at 150 deg C.

6/ The reverse bias burn-in (8) is a requirement only when specified in the applicable detailed specification. It is recommended only for MOS, linear, or other microcircuits where surface sensitivity may be of concern. When reverse bias burn-in is not required, interim electrical parameters of (7) may be omitted. The order of performing burn-in (6) and the reverse bias burn-in (8) may be reversed.

7/ The seal test may be performed in any sequence between (9) and (14), but it shall be performed after all shearing, forming, and bending operations. The Krypton method shall not be used. An optional seal test may also be performed after (4).

8/ The radiographic screening may be performed in any sequence after (3). When aluminum bond wires are used, only one view is required.

9/ At the manufacturer's option, visual inspection for catastrophic failures may be conducted after each of the thermal/mechanical screens, after the seal test sequence, or after the radiation test. Catastrophic failures are defined as missing leads, broken packages, or lids off.

4.5.3 Electrical Tests and Conditioning.

4.5.3.1 Electrical Tests. Each LSIC shall be subjected to its applicable dc, functional, and ac electrical tests at +25°C, -55°C, and +125°C. Electrical parameters, as specified, shall be read and recorded, and percent defective allowable (PDA) applied. A failure in any built-in test shall be cause for rejection of the LSIC even if other functional or parameter test results are acceptable.

4.5.3.2 Delta Computation. Delta computation shall be performed for those parameters for which delta limits are established. Delta is defined as the difference between a specified parameter reading at 25°C prior to a given test and that same parameter reading at 25°C subsequent to that test. If the Delta value for a part exceeds the established Delta limits, that part has failed the test and shall be removed from the lot.

4.5.3.3 Burn-in. Each LSIC shall be subjected to 240 hours total (combined) burn-in at 125 deg C ambient. Both static burn-in (with dc bias) and dynamic burn-in (operating) are required. The bias used shall not be less than 90 percent of the maximum rated bias. The percent defective allowable (PDA) for each lot submitted for burn-in shall be five percent. The percent defective shall be determined by the total of the number of catastrophic burn-in failures plus the postburn-in electrical limit measurement failures plus the Delta limit failures divided by the number of LSICs placed on burn-in multiplied by 100. Rejected lots may be resubmitted to additional screening only after approval is received from the contracting officer. Except as otherwise specified in the detailed specification, preburn-in is not permitted.

4.5.4 Radiographic Inspection. Radiographic inspection shall be performed on each LSIC in accordance with MIL-STD-883. Method 2012.

4.5.5 Screening Test Data. The following screening test data shall be recorded for each lot:

a. The part number, lot date code, date(s) of test, total quantity tested, accept and reject quantity, serial numbers which failed, and at what test sequence they failed

b. Electrical test - read and record parameters and deltas.

c. Statistical parametric summary of postburn-in recorded parameters including the minimum, maximum, mean, standard deviation, three sigma values, and histograms. Devices exceeding the three sigma values shall be identified.

d. "Schmoo" plots for each device if the product evaluations tests indicated marginal performance or nonfunctioning regimes (see 4.4.2.1)

e. PDA calculation and lot disposition across burn-in

f. Extended power, life, and long term stability test results

g. X-ray report and film negative for each device

h. Failure analysis report, if applicable

i. SEM photographs and results summary

4.5.6 Failure Analysis. Failure analysis shall be performed on catastrophic failures experienced subsequent to burn-in. LSICs failing to survive a postburn-in electrical test or a subsequent test because of opens, shorts, inoperability, or logic error shall be analyzed to the extent necessary to ensure understanding of the failure mode and cause. Failure analysis shall also be performed on devices that fail during the formal radiation hardness evaluation tests (see 4.4.3) or during radiation lot conformance tests (see 4.6.3). The failure analysis shall be used to identify the problem areas that contributed to the failure, such as layout errors, processing problems, or packaging problems. In any lot that fails any specified lot acceptance criterion, sufficient quantity of failed LSICs occurring shall be analyzed to establish cause(s) of failure(s), such as an out-of-control processes, to determine necessary corrective actions and to determine lot disposition. The failure record and failure analysis shall be documented and retained for at least seven years.

4.5.7 Nonconforming Material. Nonconforming material or assembled units that do not meet the established tolerance limits set for the production screens shall be removed from the production lot. Nonconforming material or assembled units may be reworked and rescreened in accordance with 3.3.6. If the reworked material or assembled unit subsequently passes the production screens, it can again be considered part of the

production lot. Nonconforming material or assembled units that do not satisfy these rework criteria shall be considered as scrap. Reassignment of assembled production units to a different production lot shall not be made.

4.5.8. Procedure in Case of Test Equipment Failure or Operator Error During Screening Tests. Whenever an LSIC is believed to have failed as a result of faulty test equipment or operator error, the failure shall be entered in the test record along with a complete explanation verifying why the failure is believed to be invalid. When source inspection is required. the source inspector or contracting officer shall be notified within one working day and given details from the test record and the opportunity to challenge the validity of the error claimed. If no challenge is made within the next working day, the error may be considered valid as recorded. If it is determined that the remaining product has not been damaged or degraded. the lot or surviving portion of the lot, as the case may be, may be resubmitted to the corrected screening test(s) in which the error occurred. Failures verified as having been caused by test equipment failure or operator error shall not be counted in the PDA calculation (when applicable).

4.6 Lot Conformance Tests. Lot conformance testing shall be performed as the basis for lot acceptance on each production lot manufactured. Lot conformance testing is a sampling test performed to demonstrate a degree of confidence that a production lot of LSIC that has passed the in-process and post-assembly screening tests and inspections also meets the other requirements of this specification. Unless modified in the approved manufacturing baseline or by the contracting officer, lot conformance tests shall be performed in accordance with the requirements specified including the applicable tests specified in Table C-IV.

4.6.1 Test Devices. The lot conformance tests shall be conducted on randomly selected samples from the production lot of LSICs that have been manufactured in accordance with the parts, materials, processes, and controls specified and that have passed all in-process screening including the post-assembly screening tests (see 4.5). However, electrical rejects from the post-assembly screening tests of the same production lot may be used for all subgroups when end-point electrical parameters are not required. The same device may be used for more than one test. Reserve sample devices may be tested with the subgroups to provide replacements in the case of test equipment failure or operator error. These devices shall be used in predesignated order.

TABLE C-IV. Lot Conformance Tests

TEST	MIL-STD-883 METHOD	CONDITION	LOT SAMPLE QUANTITY 1/
Subgroup 1			
Physical dimensions	2016		2
Solvent resistance	2015		2
Lead integrity	2004	Test condition B2, Lead fatigue	2
Solderability 2/	2003	Soldering temperature 245°C ± 5°C	2
DPA	5009		2
Subgroup 2			
Thermal shock	1011	Test condition B, 15 cycles, minimum	2
Temperature cycling	1010	Test condition C 100 cycles, minimum	2
Moisture resistance	1004		2
seal	1014	The Krypton method	2
(a) Fine		shall not be used	
(b) Gross			
External visual		Use criteria of 1004	2
End-point electrical parameters		3/, 4/	2
Subgroup 3			
Electrical parameters		4/	3
Steady state life test	1005 5/	Condition D or E 150°C 500 hours, or 125°C, 1000 hours, minimum	3
End-point electrical parameters		3/, 4/	3
Electrostatic Discharge Sensitivity	3015		3
Subgroup 4 6/			6/
Neutrons	1017	4/	5
Total dose	1019	4/	5
Transient ionization			
Upset	1021/1023	4/	5
Latch-up	1020	4/	5
Burnout		4/	5
Transient annealing		4/	5
Single event effects		4/	5
EMP		4/	5

TABLE C-IV. Lot Conformance Tests (Continued)

Footnotes for Table C-IV.

1/ The lot sample quantity as shown in Table C-IV is for production lot quantities less than 100. For production lot quantities of 100 to 500, the sample quantity shall be increased by 1 unit for each additional 100 units. For production lots greater than 500, the sample size shall be as approved by the contracting officer (see 4.6.1).

2/ All devices submitted for solderability testing shall have a lead finish that has been through the temperature/time exposure of burn-in.

3/ At the manufacturer's option, end-point electrical parameters may be measured after moisture resistance test and before seal test.

4/ Per applicable detailed specification

5/ The alternate removal-of-bias provisions of Paragraph 3.3.1 of Method 1005 shall not apply for test temperatures above 125 deg C.

6/ Each Subgroup 4 test is required only if specified in the detailed specification. Unless otherwise specified, the survival probability shall be 0.999 and the confidence level shall be 0.95. For devices where the response to a radiation environment is largely variable from one wafer to the next within a diffusion lot, the lot sample quantity (5) for each Subgroup 4 test is for each wafer in the production lot.

4.6.2 Procedure in Case of Test Equipment Failure or Operator Error During Lot Conformance Tests. Whenever an LSIC is believed to have failed as a result of faulty test equipment or operator error, the failure shall be entered in the test record along with a complete explanation verifying why the failure is believed to be invalid. When source inspection is required, the source inspector or contracting officer shall be notified within one working day and given details from the test record and the opportunity to challenge the validity of the error claimed. If no challenge is made within the next two working days, the error may be considered valid as recorded. If it is established that the product has been damaged or

degraded, a replacement LSIC from the same production lot may be added to the sample. The replacement LSIC shall be subjected to all those tests to which the discarded LSIC was subjected prior to its failure and to any remaining specified tests to which the discarded microcircuit was not subjected prior to its failure The manufacturer, at his own risk, has the option of replacing the failed LSIC and continuing with the tests before the validity of the test equipment failure or operator error has been established.

4.6.3 Radiation Lot Conformance Testing. Subgroup 4 of Table C-IV outlines the lot conformance tests that may be required to demonstrate satisfactory radiation hardness characteristics for a production lot of LSICs. As noted in Appendix A, the tests in Subgroup 4 of Table C-IV are not always required to demonstrate radiation hardness of a particular lot. When any of the Subgroup 4 tests are required, either a radiation to failure test or a single radiation level test may be used.

4.6.3.1 Radiation to Failure Test. For each environment. a random sample of at least five LSIC parts from the production lot are exposed to increasing radiation levels until each part fails. A failure is indicated by the radiation-induced parameter value for the part exceeding the parameter test limit value established for the part in the detailed specification. Based upon the mean radiation failure level and the specified maximum radiation environment for the part, the radiation design margin is calculated as discussed in 50-1 of Appendix A. If this calculated radiation design margin does not satisfy the acceptance criteria specified in the detailed specification, the lot shall be rejected.

4.6.3.2 Single Radiation Level Test Method. For each environment, a random sample of at least five LSIC parts from the production lot are exposed to the radiation level specified in the detailed specification, and the radiation-induced changes in parameter values for each part are recorded. Based on the mean values of the radiation-induced parameters and the corresponding end point electrical parameter failure limits, the parameter design margin is calculated as discussed in 50.4. of Appendix A. If this calculated parameter design margin does not satisfy the acceptance criteria specified in the detailed specification, the lot shall be rejected.

4.6.4 Lot Acceptance Criteria. Acceptance of a production lot of LSICs is achieved when:

a. The product evaluation tests for the LSIC have been satisfactorily completed (see 4.4).

b. The life tests on the Test Chip Evaluation Samples for the applicable wafer lot have been satisfactorily completed without failure (see 4.3.3.1).

c. The lot conformance tests have been completed without failure (see 4.6).

4.6.5 Disposal of Samples. LSICs subjected to destructive tests or which fail any test shall not be shipped on the contract or purchase order as acceptable products. They may. however. be delivered at the request of the contracting officer as a special shipment if they are clearly identified so as to prevent their being mistaken for acceptable product. A destructive test is one in which the applied stresses or environment may permanently damage the part. Sample LSICs. from lots which have passed product assurance inspections or lot conformance tests and which have only been subjected to mechanical or environmental inspections or tests not classified as destructive. may be shipped on the contract or purchase order, provided the actual testing was nondestructive and each of the microcircuits subsequently passes final electrical tests.

4.7 Qualification. LSICs manufactured and delivered in accordance with this specification and that are flight accredited (see 3.1) are qualified.

5. PACKAGING.

LSICs shall be prepared for delivery in accordance with the preservation packaging and packing requirements of MIL-M-55565, unless otherwise specified in the applicable detailed specification or purchase order. In addition, the following requirements shall be applied to ensure electrostatic protection:

a. LSICs and packages shall be marked or identified with electrostatic sensitivity labels per MIL-STD-129.

b. LSICs shall be individually packaged and serialized. and shall be separated from each other.

c. LSICs shall be fully enclosed in an antistatic material with sufficient permanent conductivity on all surfaces to bleed-off static charges and to prevent the introduction of electronic charges from the external environment.

d. Packaging and packing materials used shall not crumble, flake, powder, or shed.

e. Leads shall be secured to protect against vibration and to retain their shape.

f. Isolation from shock and vibration shall be provided.

g. Individual packages and external containers shall be marked to clearly indicate the content.

6. NOTES

6.1 Intended Use. It is intended that detailed specifications prepared for the procurement of specific devices would reference this general specification to incorporate the applicable requirements. LSICs covered by this specification are intended for use in space vehicles or in equipment with very high reliability requirements. The requirements stated in the specification are a composite of those that have been found to be cost effective for high reliability space vehicle applications. The general manufacturing process control requirements specified are intended to assure that a known quality product is manufactured and that all units in all production lots will have a uniform high reliability. The emphasis is on designing and manufacturing a reliable LSIC rather than screening defective LSICs from the production lot.

The specification imposes the concept of product flight accreditation (see 3.1) to assure that the LSICs satisfy all requirements that have been found necessary to assure successful space vehicle missions.

6.2 Tailored Application. Where possible, the requirements in the specification are stated in ways that are self tailoring to each application. Nevertheless. all requirements of this specification should be evaluated for each application and those that seem inappropriate should be identified and reviewed. Contractors are encouraged to identify to the contracting officer, for program office review and consideration, any requirements believed excessive or conflicting. However, contractors are reminded that deviations from contractually imposed requirements can be granted only by the contracting officer. Deviations to the referenced test methods incorporated in the manufacturing baseline should be reviewed by the audit team and are approved if that baseline is approved.

An attempt was made to state the requirements in ways that would be self tailoring to the specific applications without paragraph referencing. For example, if a space vehicle specification states that LSICs shall be in accordance with this specification," then all requirements stated in this specification are applicable. If a detailed specification for a particular LSIC states that the LSIC "shall be tested in accordance with this specification." then only the device testing requirements would be made applicable by that reference and the other requirements such as for LSIC design and manufacturing would not apply.

6.3 Ordering Data. Procurement of a specific LSIC for space vehicle applications is based upon the contractor preparing a purchase order that would reference the complete detailed technical requirements for the specific LSIC. Depending upon the contractor practices, or the specific contract. the technical requirement document may be called a detailed specification, a Specification Control Drawing, a Source Control Drawing, or some other name. In any case, it is referred to in this general specification as the detailed specification. Regardless of the actual document name, it should be prepared in a book form format similar to this general military specification. In other words, the detailed specification should incorporate the requirements of this general specification (by reference) then, using a similar format, the needed new requirements and deviations required for the procurement of the specific LSIC should be stated. By using the same format as this general specification, the manufacturer and others using the detailed specification can easily determine the total set of requirements for the specific LSIC.

INSTRUCTIONS: In a continuing effort to make our standardization documents better, the DoD provides this form for use in submitting comments and suggestions for improvements. All users of military standardization documents are invited to provide suggestions. This form may be detached, folded along the lines indicated, taped along the loose edge *(DO NOT STAPLE)*, and mailed. In block 5, be as specific as possible about particular problem areas such as wording which required interpretation, was too rigid, restrictive, loose, ambiguous, or was incompatible, and give proposed wording changes which would alleviate the problems. Enter in block 6 any remarks not related to a specific paragraph of the document. If block 7 is filled out, an acknowledgement will be mailed to you within 30 days to let you know that your comments were received and are being considered.

NOTE: This form may not be used to request copies of documents, nor to request waivers, deviations, or clarification of specification requirements on current contracts. Comments submitted on this form do not constitute or imply authorization to waive any portion of the referenced document*(s)* or to amend contractual requirements.

★ U.S. Government Printing Office: 1983—382-870/8004

(Fold along this line)

(Fold along this line)

NO POSTAGE NECESSARY IF MAILED IN THE UNITED STATES

OFFICIAL BUSINESS
PENALTY FOR PRIVATE USE $300

BUSINESS REPLY MAIL
FIRST CLASS PERMIT NO. 73236 WASH DC

POSTAGE WILL BE PAID BY HQ U.S. AIR FORCE

SD/ALM
P. O. Box 92960
Worldway Postal Center
Los Angeles, CA 90009

STANDARDIZATION DOCUMENT IMPROVEMENT PROPOSAL

(See Instructions – Reverse Side)

1. DOCUMENT NUMBER	2. DOCUMENT TITLE
MIL-HDBK-339 (USAF)	Custom Large Scale Integrated Circuit Development and Acquisition for Space Vehicles

3a. NAME OF SUBMITTING ORGANIZATION	4. TYPE OF ORGANIZATION *(Mark one)*
	☐ VENDOR
b. ADDRESS *(Street, City, State, ZIP Code)*	☐ USER
	☐ MANUFACTURER
	☐ OTHER *(Specify)*: _____

5 PROBLEM AREAS

a. Paragraph Number and Wording

b. Recommended Wording

c. Reason/Rationale for Recommendation

6. REMARKS

7a. NAME OF SUBMITTER *(Last, First, MI)* – Optional	b. WORK TELEPHONE NUMBER *(Include Area Code)* – Optional
c. MAILING ADDRESS *(Street, City, State, ZIP Code)* – Optional	8. DATE OF SUBMISSION *(YYMMDD)*

DD FORM 82 MAR 1426

PREVIOUS EDITION IS OBSOLETE.