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MILITARY HANDBOOK

ELECTRONIC RELIABILITY DESIGN HANDBOOK

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RELI

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ELECTRONIC RELIABILITY DESIGN HANDBOOK

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1. This standardization handbook was developed by the Department of Defense in accordance with established procedures and is approved for use by all Departments and Agencies of the Department of Defense.

2. This publication was approved 15 October 1984 for printing and inclusion in the military standardization handbook series.

3. Every effort has been made to reflect the latest information on electronic reliability design techniques. It is the intent to review this handbook periodically to insure its completeness and currency.

4. Beneficial comments (recommendations, additions, deletions) and any pertinent data which may be of use in improving this document should be addressed to: Commander, Rome Air Development Center, AFSC, ATTN: RBE-2, Griffiss Air Force Base, New York 13441, by using the self-addressed Standardization Document Improvement Proposal (DD Form 1426) appearing at the end of this document or by letter.

TABLE OF CONTENTS

TABLE OF CONTENTS (Cont'd)

TABLE OF CONTENTS (Cont'd)

TABLE OF CONTENTS (Cont'd)

TABLE OF CONTENTS (Cont'd)

TABLE OF CONTENTS (Cont'd)

TABLE OF CONTENTS (Cont'd)

TABLE OF CONTENTS (Cont'd)

LIST OF TABLES

LIST OF TABLES

LIST OF TABLES

LIST OF TABLES

LIST OF TABLES

LIST OF TABLES

LIST OF FIGURES

LIST OF FIGURES

LIST OF FIGURES

LIST OF FIGURES

LIST OF FIGURES

LIST OF FIGURES

1.0 SCOPE

As stated in the preface the Electronic Reliability Design Handbook is an updating and extensive revision of the Reliability Design Handbook (RDH-376) published in 1976 by the Reliability Analysis Center under contract with Rome Air Development Center. A great deal of effort has been expended in obtaining the latest available information pertinent to the subject of component parts reliability. Sources of information have included papers presented at symposia, studies sponsored by military agencies, articles appearing in technical journals, MIL and DOD documents, and the Reliability Analysis Center's databank.

Volume 2 of the Electronic Reliability Design Handbook has been designed to provide as much practical and useful information as possible on the considerations and procedures to be employed in the selection, specification, application and control of electronic parts in order to achieve reliable equipment.

The format used to accomplish this goal divides the subject matter into seven distinct chapters, as follows:

1.0 Scope and General Information. This chapter traces the history of component reliability, points out the need for reliable components, discusses the technologies, materials, packaging and testing methods employed in current state-of-the-art devices, and describes predictable trends for the future development of component parts.

2.0 Referenced Documents.

3.0 Definitions.

4.0 Reliability Theory. This chapter addresses the subject of probability distributions such as Weibull, exponential, gamma, etc. used in reliability procedures and discusses confidence intervals and the temperature dependence of failure rates.

5.0 Component Reliability Design Considerations. This chapter presents guidelines for part selection and control of standard, nonstandard and critical parts, as well as parts selection and application guidelines for thirteen generic part types (including standard electronic modules (SEM).

6.0 Applications Guidelines. This chapter considers those environmental factors which the electronic part must be capable of withstanding during production as well as during field operation. It contains guidelines for the design of reliable circuits including such factors as electrical derating and thermal design.

7.0 Specification and Control During Acquisition. This chapter is devoted to the portrayal of those elements of a reliability program which come into play during parts acquisition including parts screening, screening effectiveness, microcircuit testing and automatic test equipment; it also treats the subject of the management of parts selection and control efforts and of a suitable reliability program.

8.0 Logistic Support. This chapter addresses general storage considerations, including the storage characteristics of specific part types; and parts provisioning techniques used to control parts in deployed military systems.

9.0 Failure Reporting and Analysis. This chapter covers closed-loop failure reporting/corrective action systems, data collection and retention, general considerations in failure analysis, causes of parts failure and failure categories.

Thus, this volume attempts, by orderly progression, to discuss and develop guidelines for all the essential ingredients of a successful parts reliability program.

Whenever it has been possible to get our message across merely by referencing an existing specification or standard, we have done so. However, where we have felt that the point we wanted to make required the explicit use of material from an existing specification or standard we appropriated and included that material in order to illuminate our meaning. Where information pertinent to our subject matter is to be found in Volume I of the Handbook, we have referred the reader to the appropriate section.

Finally, in line with our goal of being as concise, explicit and brief as possible, we have tried to exclude unessential detail characteristics of the devices under discussion. Thus, for example, in the case of resistors and capacitors we refrained from supplying MIL-type designations, standard values and sample failure rates. All of this information and more can be easily obtained by the reader himself from either the MIL part specification or MIL-HDBK-217.

1.1. GENERAL INFORMATION

There exists an abundance of military specifications and standards which portray the physical dimensions, electrical ratings, operating characteristics, environment withstanding capabilities, preferred styles and preferred electrical ratings, etc., for electronic component parts. There exist MIL documents which define standard methods for the electrical and environmental test of parts for either qualification or screening purposes; qualified parts lists; procedures for part failure rate prediction; ESD damage protection methods, and the requirements for suitable parts control. Also there exist documents which specify the requirements for the materials used in part manufacture, for process control, and for the packaging, marking, shipping and storage of electronic parts.

The goal of the Electronic Reliability Design Handbook is to provide instruction on when, why and how to use any part or all of these available documents. It represents the Rome Air Development Center response to the recognized need for a comprehensive treatment of the problems, considerations and recommended engineering and management methods associated with the design of reliable end item equipments.

1.1.1 HISTORY OF COMPONENT RELIABILITY

1.1.1.1 INTRODUCTION

In examining the history of electronic parts, it is apparent that the emphasis on reliability has been directed at the active elements, including vacuum tubes, discrete semiconductor devices, integrated circuits, large scale integrated circuits and now, at the beginning of the 1980s, very large scale integrated circuits and very high speed integrated circuits. Typically, the active components have been the most significant contributors to equipment reliability problems. Although there have been reliability problems attributed to specific passive component types, e.g. electrolytic capacitors, potentiometers, etc., passive components have not been subject to the revolutionary, rapid change in technology and fabrication that active components have undergone in the last several decades. This is not to imply that the reliability of passive components has not improved over the years. It has improved, but the process has been a more orderly one because component designers were able to build upon tried and proven technologies.

Prior to and following World War II, and until the mid-1950s, the vacuum tube was of prime importance to the reliability of electronic equipment. From the mid-1950s until the mid-1960s, the reliability of the discrete semiconductor diode and transistor received the most attention. Since the mid-1960s, the integrated circuit (or microcircuit) has been the focus of attention relative to the reliability of military electronic equipment. As the semiconductor industry continues to improve technology whereby more functions can be included on a silicon chip, the 1980s promise to be a new era of improved device capability and reliability. In the remainder of this chapter, a brief summary is provided on the history of electronic part reliability, highlighting the areas discussed above.

1.1.1.2 VACUUM-TUBE ERA (1940-1950)

Before World War II, military electronic equipment was relatively simple. However, with the onset of war came the demand for increasingly complex equipment, e.g., radar, miniaturized proximity fuse, walkie talkies, etc., which could withstand higher levels of environmental stress, and a major concern in this frantic period was vacuum tube reliability. Tube quality and reliability were increased by more stringent application of lot control practices in accepting produced lots for military application. The basic policies and procedures for statistical quality control were established in 1941 and 1942 under American War Standards. In 1944, the U.S. Navy began a program to obtain more rugged tubes for shipboard use. Since shock and vibration

requirements caused many tube failures in fire control radars and related equipment, shock and vibration equipment were developed to aid in tube testing, while structural modifications were made in standard vacuum tubes to increase their resistance to shock. As a result of these efforts, the ruggedized "W series" evolved, covering 40 different vacuum tube types. In 1946, Aeronautical Radio, Inc, (ARINC), was established by the airlines to collect and analyze defective tubes in commercial airline applications. As a result of ARINC's efforts, in concert with the tube manufacturers, greater attention was directed towards assembly in production. Post manufacture tests included testing of all tubes for shorts, continuity, shock and transconductance. Sampling inspection testing included vibration testing, filament cycling and life tests. Toward the end of this decade, ARINC's tube work was directed toward military problems. Under a joint services contract, failed tubes were collected at various military installations, together with reliability data on the failure or cause of removal, hours of use, and use conditions. One of the results of the 1950 ARINC study was the discovery that only 33% of Navy electronic equipment on shipboard was operating satisfactorily at any one time. This kind of information set the stage for the reliability thrust that developed in the period 1950-1960.

With the veil of wartime censorship lifted, details of some of the progress made in electronics began to appear. The miniaturization requirement of the proximity fuse had resulted, in the active components area, in the development of subminiature tubes. In the passive components area, it led to the development of thick film hybrid technology. Thick-film silver conductors and carbon resistors were screened and fired onto ceramic substrates. Small disk ceramic capacitors were attached to the substrates. This technology ultimately resulted in the module circuit designs of the 1950s.

1.1.1.3 THE RELIABILITY DECADE AND THE EMERGENCE OF THE TRANSISTOR (1950-1960)

The focus on electron tube reliability continued in the early 1950s. In 1950, an Ad Hoc Group on Electronic Equipment was formed by the Department of Defense (DoD). One of the by-products of this activity of importance to electronic part reliability was the formation of the Advisory Group on Reliability of Electronic Equipment, AGREE, in August, 1952. In March, 1954, the Panel on Electron Tubes was redesignated the Advisory Group on Electron Tubes, AGET, and in June 1954, the Advisory Group on Electronic Parts, AGEP, was formed. One of the recommendations found in the AGREE report of June, 1957, was that a permanent group be established at the DoD level to include representatives of industry and the three services to be charged with the task of developing military component specifications, testing component parts for design capability, and developing inspection methods. This group would serve as the National Reliability Center. One year later, in July 1958, OASD, and the Ad Hoc Group on Parts Specification Management for Reliability was established to analyze the recommendations made by AGREE in order to advise the Assistant Secretaries of Defense Research and Engineering and Supply and Logistics

regarding efficient implementation methods and procedures. One result of the Ad Hoc Group's activities was the development of what is known today as the Established Reliability (ER) specifications for electronic parts.

While now limited mainly to capacitors and resistors, the original intent was to apply ER specifications to a broader class of electronic parts. Another important output in this decade of electronic parts awareness and one which is also still in very active use today is MIL-STD-202, "Test Method for Electronic Components and Parts."

In March 1959, the Inter-Service Data Exchange Program was born and is currently active as the Government/Industry Data Exchange Programs (GIDEP). The purpose of this program is to provide for the free and automatic interchange of unclassified, nonproprietary reliability data among the ballistic missile major contractors, subcontractors, and involved government agencies.

In October 1959, the Air Force issued the "RADC Reliability Notebook" in loose-leaf form. Part of this document, in particular Section 8, was the forerunner of MIL-HDBK-217, "Reliability Prediction of Electronic Equipment.

The preceding information, relative to the events in the 1950s, represents a logical extension of the activities of the 1940s. However, the invention of the transistor in the late 1940s and its practical implementation in the early to mid 1950s opened up new vistas of potential improvement in electronic equipment reliability. Early alloy junction transistors were at least an order of magnitude more reliable than receiving electron tubes. These first transistors were encapsulated in a variety of plastic materials, but humidity testing soon indicated that these materials could not adequately control the very sensitive device surface conditions. Plastic sealing (found ineffective) led to solder sealing (also ineffective) and ultimately led to the evolution of precision glass-to-metal headers in the mid to late 1950s which, with improvement, is the method applied today for reliable semiconductor parts, as well as for many passive parts.

The military services were the first to realize and exploit the reliability potential of the transistor and began to design it for use in military electronic equipment. During the period 1952 through 1960, approximately 60 new transistors, both germanium and silicon, were developed by the Army alone. These programs led to the development of end-item equipment whose reliability reflected that of the transistor itself. Some of the equipment developed in the late 1950s is still in field use today, with perhaps only some minor improvements in devices, but still employing discrete semiconductors.

The early use by the military of the transistor developed a need for a means of control and specification. MIL-S-19500, "General Specifications for Transistors," came into being in the mid-1950s and was patterned after the traditional specification for electron tubes (MIL-E-1) which,

while it tended to control the average quality level, could allow rather wide variations in the reliability of individual lots. MIL-S-19500B encompassed both the transistor and diode, the latter device previously being covered under MIL-E-1. MIL-S-19500B included a sampling plan giving the user a high degree of assurance that the specific product would not have a higher failure rate than that specified for the given use condition. This approach required the testing of many devices for long periods of time under typical use conditions, which led to the conclusion that an approach other than use conditions was necessary if reliability of semiconductor parts was to be assured at a reasonable cost. In general, the reliability assurance techniques for the semiconductor product prevalent up to the end of the 1950s could not be practically applied to provide guaranteed rather than estimated reliability.

It is interesting to note that developments of the 1950s precursed the invention of the processes and techniques of the modern integrated circuit. In the 1950s, the following service programs were working toward electronic circuit miniaturization:

- Navy's Project Tinkertoy (1950-1953)
- Army's Diamond Ordinance Fuze Laboratories 2-D Program (1957-1959)
- Army Signal Corps Micromodule Program (1958-1963)

The latter two programs relied heavily on the semiconductor diode and transistor as the active circuit elements.

The evolution of the modern integrated circuit stemmed from two major developments in the late 1950s. Silicon transistor technology was maturing in the late 1950s, and in August 1959 the PLANAR process, so named because it resulted in the fabrication of flat transistors, produced the first modern diffused transistor at Fairchild Corporation. Earlier in March 1959, at the IRE Show in New York City, Texas Instruments announced the invention of the integrated circuit. The combination of these two inventions is the basis for the integrated, large scale integrated, and very large scale integrated circuits we know today.

During this era, significant advances in passive component technology accompanied the active component devices. The etched printed circuit began its steady growth toward becoming the principal method of interconnection. It resulted from the pioneering work done by the U.S. Army in 1949 in developing dip-solderable etched printed circuit boards. This was followed in the early 1950s by industrial development of a PC board manufacturing capability. From this time to 1960, PC technology evolved gradually but steadily, with plated through-holes appearing in 1953, glass-epoxy, copper-clad laminates in 1952, solder marks in 1955, and the multilayer board in 1960.

Other developments of the 1950s in the passive components included:

- Semi-automated wirewrap techniques

- Resistors
  1) Deposited carbon and metal-film resistors for better temperature stability
  2) Smaller, more reliable, power resistors

3) Potentiometer
   a. Resistance elements of small metallic films and conductive plastics
   b. Small trimmer types

o Capacitors
   1) Tantalum dielectric electrolytics
   2) Smaller size and higher temperature operation

o Magnetic devices
   1) Ferrite and powdered iron cores for inductors and transformers
   2) Toroidal construction
   3) Metallized glass conductors for greater stability and ruggedness
   4) Smaller wires, cores and insulation

1.1.1.4 THE DECADE OF THE INTEGRATED CIRCUIT (1960-1970)

The decade of the 1960s belongs to the integrated circuit (also called microcircuit). However, advances were also made in the development of military specifications for discrete semiconductors. MIL-S-19500, "General Specification for Semiconductor Devices," and MIL-STD-750, "Test Methods for Semiconductor Devices," were issued very early in 1962. These documents originated early in 1960 when it was decided by the NATO countries that a Standard NATO Agreement (STANG) be generated for semiconductor devices. In August, a joint UK-US working group prepared a draft document. The document was the forerunner of MIL-S-19500 and MIL-STD-750. The formatting of MIL-M-38510, "General Specification for Microcircuits," and MIL-STD-883, "Test Methods and Procedures for Microelectronics," generated much later in this decade followed similar formatting.

The invention of the integrated circuit and the PLANAR process set the stage for the exploitation of integrated circuits in the late 1960s. In 1962, Texas Instruments was awarded an Air Force contract to design and build twenty-two special integrated circuits for the improved Minuteman Missile System, representing the first large scale use of these devices. Their application allowed missile range to be increased by reducing the size and weight of the existing electronic package and avoided a costly and lengthy program for the development of higher performance propulsion. Most references cite the microcircuit application to Minuteman as the springboard for the wide usage of microelectronics by the industrial/consumer sector as well as by the military. This was later followed by NASA's widespread use of microcircuits in the Apollo program.

The significance of the integrated circuit application to Minuteman reliability can be quantified as follows. In 1958, an average microcircuit failure rate of 0.0007 percent per 1000 hours was required. However, at that time, the failure rate for transistors was about 1.0 percent per 1000 hours. Improvements from the Minuteman program resulted in decreasing the failure rates of integrated circuits to about 0.0003 percent per 1000 hours.

The changes in the general status of semiconductor reliability from the 1950s to the 1960s stemmed from three major factors which evolved from important technological breakthroughs, i.e., the inventions of the PLANAR process and integrated circuit. These were:

1) The need for increasingly higher reliability such as required by Minuteman

2) The development of structures capable of being tested at higher stress levels, both thermal and mechanical

3) The increasing evidence that if workmanship defects could be controlled, devices could be made extremely reliable by improving device design, materials and process controls

With the growth in the use of discrete semiconductors and integrated circuits came the recognition that, no matter how stringent the process control sampling and efforts to "build in" reliability into the product, it was more economical and frequently more efficient to test (in fact, "screen") the final product to eliminate workmanship defects. This was in contrast to attempting to eliminate such defects by tight control of the fabrication process. In October 1966, the Air Force issued RADC Specification 2867, "Quality and Reliability Assurance Procedures for Monolithic Microcircuits," applying screening techniques to microcircuits. This specification was replaced in May 1968 by MIL-STD-883. In November 1969, the first general specification for microcircuits, MIL-M-38510, was issued. It should be noted that development of military specifications and standards was hampered by the DoD policy current at the time. In essence, military specifications and standards were discouraged because of the belief that standarization at that time would impair design flexibility and system optimization.

The three main areas covered by MIL-M-38510, "General Specification for Microcircuits," are: (1) requirements for adequate and documented process control, (2) specified plans of device screening and preconditioning and (3) specified criteria for lot acceptance test and lot acceptance criteria applied to lot screening results. Lot screening removes early failures or infant mortality subpopulation of the integrated circuit lot in question. Test Methods 5004 and 5005, "Test Methods and Procedures for Microelectronics," specify in detail the appropriate screening tests to be used with MIL-STD-883.

The requirement of MIL-M-38510 for microcircuit production in the continental United States has spawned vendor high reliability processed parts generally in line with Methods 5004 and 5005 of MIL-STD-883 under a variety of company trade names. Microcircuits for military application are procured in accordance with MIL-M-38510 and MIL-STD-883 or their vendor equivalents.

The issuance of MIL-S-19500, "Semiconductor Devices, General Specifications for," and MIL-STD-750, "Test Methods for Semiconductor Devices," in their current formats for discrete semiconductor devices preceded the issuance of their microcircuit specification counterparts by six to seven years. Yet, the inclusion of screening and burn-in test methods in the desirable semiconductor specifications post-dated the issuance of the microcircuit general specification and test standard.

With the wider application of semiconductor devices in the 1960s, it became evident that the reliability of these and other electronic parts required the combined efforts of many specific disciplines. It was recognized that while reliability was an engineering problem, the device technology incorporated a host of physical science disciplines. An important step was taken in 1962 when the Rome Air Development Center sponsored the first Physics of Failure Symposium in Chicago, Illinois. The Air Force continued to sponsor the annual symposia until 1967 when the IEEE assumed sponsorship. Through the medium of this symposium, the failure mechanisms encountered in the emerging device technologies are identified to the scientific community charged with their elimination in electronic parts. It serves as a mechanism to bridge the communication gap between the solid state physicist and the reliability engineer.

In the passive component areas, in order to make it possible to fabricate complete circuits on a single chip, thin film resistors were fabricated making use of the ohmic properties of the bulk materials, and capacitors were formed by reverse-biased pn junctions.

Hybrid microcircuits began to make their appearance. Hybrids required the development of thin-film conductors, resistors, and capacitors which were evaporated in high vacuum onto a glass or ceramic substrate.

1.1.1.5 DECADE OF THE LARGE SCALE INTEGRATED CIRCUIT (LSI) (1970-1980)

The decade of the 1970s saw the evolution of the LSI integrated circuit. However, during this decade, the military efforts toward improved reliability of electronic equipment in the parts area were directed toward more pragmatic improvements.

The preparation of a list of standard types of microcircuits was prohibited by a DoD directive dated April 1967 (revised September 1969). As a result of this directive and the increased use of microcircuits, military nonstandard microcircuits proliferated. To reduce this nonstandard part proliferation, the Joint Technical Coordinating Group in Electronic Equipment Reliability (JTCG-EER) and other interested groups succeeded in having the original policy rescinded in August 1974. Subsequently, a list of standard types of microcircuits, MIL-STD-1562, was prepared and published in November 1974, paving the way for reductions in nonstandard microcircuit parts usage. As a result of these actions, by the end of 1975, more than 350 microcircuits were either covered or in the process of being covered by military specifications.

As an adjunct to the microcircuit military specification exercise to reduce proliferation of nonstandard parts, the use of the Defense Electronics Supply Center, Military Parts Control Advisory Group (MPCAG) was expanded from sole Air Force utilization to use by all services. In concert with the expanding role of MPCAG and its use by the Services, MIL-STD-965, "Parts Control Program," was issued in April 1977. MIL-STD-965 serves as the basis today for a parts control program in use by all the military services. See Section 5.1 (Parts Control).

Many critical equipments and systems under development in the 1970s could only be realized by the use of hybrid microcirucits. It was found that, because of inadequate control and insufficient device testing, reliability problems were discovered only after the hybrid circuits were installed in equipment and systems. As a result of this situation. Method 5008, "Test Procedures for Hybrid and Multichip Microcircuits," was added to MIL-STD-883 to remove some of the causative reasons for failure.

As mentioned earlier, the earliest transistors built at the Bell Telephone Laboratories were encapsulated in plastic materials. It was immediately recognized that plastic encapsulations were not suitable enclosures, particularly for nonpassivated semiconductors. The invention of the PLANAR process in the late 1950s lead to the reemergence of the plastic transistor in the early 1960s. The 1960s saw widespread nonmilitary application of the plastic transistor in conjunction with passivated surfaces made possible by the PLANAR Process. The military interest in applying plastic encapsulation heightened in the 1970s as significant technological improvements were made in plastic encapsulation materials and methods of encapsulation, but despite these improvements, the military position against the use of plastic encapsulated devices has not changed. Currently, both MIL-S-19500 and MIL-M-38510 allows the use of hermetically sealed devices only.

In the 1970s, the industrial/consumer section greatly benefited from the earlier military spearheading of the integrated circuit development. The electronic calculator market started in 1971. The first hand held calculator sold for $240 in September 1971, $40 in 1976, and ten dollars or less by the end of the decade, all made possible by the mass availability of integrated circuits.

The application of integrated circuits as microprocessors (computer on a chip) seems likely to exceed all integrated circuit applications. Microprocessors convert hardware problems into programming tasks; they are large scale integrated circuits embodying generalized computer logic. The range of products that can productively employ microprocessors is enormous. They are adaptable to automotive applications, refrigerators, microwave ovens, radios, telephones, and word processors, to mention only a few uses. They have reduced the cost of process control a hundredfold over that of twenty years ago.

During this decade, advances in passive components kept pace with microcircuit developments. Resistors and capacitors became the size of IC chips so that they could fit on hybrid substrates. All manner of components - resistors, capacitors, networks, reed relays, switches, and nickel cadmium batteries - were squeezed into the dual in-line package.

Connector reliability technology also advanced with the development of fiber optic connectors, zero insertion force, and the use of tin lead in gas tight, high pressure connectors.

1.1.1.6 THE DECADE OF VERY LARGE SCALE INTEGRATED CIRCUITS (VLSI) AND VERY HIGH SPEED INTEGRATED CIRCUITS (VHSIC)(1980)

The 1960s saw the emergence of the microcircuit and the generation of many nonstandard part specifications due to DoD concern with inhibition of parts application by part standardization. In the 1970s, with the maturing of microcircuit device technologies, greater efforts by the military were geared toward minimization of microcircuit types via the means of military parts lists. Unfortunately, too many military systems programs allow greater deviations from the screening procedures called out in MIL-STD-750 and MIL-STD-883. There are many "hi rel" devices specified for military use which allow various combinations of screening and burn-in methods not strictly in accordance with those prescribed in the above standards. The 1980s will see a move on the part of the device manufacturers to hold the screening and burn-in of military semiconductor parts to the regimen spelled out in MIL-STD-750 and MIL-STD-883.

The VLSI technology was expected to emerge toward the end of the 1970s. Because of the processing demands placed on VLSI devices, they did not come to fruition in the decade of the 1970s. In 1980, the Very High Speed Integrated Circuit Program (VHSIC) was initiated by the Department of Defense to develop VLSI signal processors with several hundred times higher speed and computing power than today's LSI devices. The goal of the VHSIC program is pilot production, in 1986, of processors on a single chip containing one-quarter million gates (10^6 transistors) operating at clock speeds of 25 MHz and performing several million to several billion operations per second. The gates will be fabricated utilizing MOS or bipolar technology and have minimum dimensions of 0.5 to 0.8 micrometers. This program is significant because it entails the development and application of entirely new device fabrication methods and procedures to accomplish the high component density and small device size requirements.

Military electronic subsystems continue to grow in complexity, so complex in fact that despite the steadily improving reliability of integrated circuits, the failure of advanced electronic subsystems and systems is becoming a problem. The higher complexity of VLSI must be used to increase overall system reliability, since these advanced devices will contain fewer major sources of failure; i.e., power circuits and external connections.

MIL-M-38510 and the MIL-STD-883 came into being with the application of microcircuits in military equipment. The transition from the small scale to large scale integrated circuit technology has not seen any radical change to the basic philosophies espoused in the above documents. By the mid-to-late 1980s, the Very High Speed Integrated Circuit is expected to come to fruition. Already, in the very large scale integrated circuit area, there are preliminary indications that these product documents are capable of being applicable. It is expected that, with refinement, the transition to VHSIC will be as orderly as previous transitions to LSI.

1.1.1.7 EPILOGUE

In developing the history of electronic parts and their reliability, it becomes difficult if not impossible to sort out unequivocally, commercial and military practices. Rather, it must be apparent from the history that there has always been a great degree of cross-fertilization consistent with the ultimate objective of reliability versus cost. The reliability improvements in the vacuum tube were driven by the demanding military environments in World War II. These improvements were capitalized upon and extended by the airline industry following World War II. Again, in the 1950s, the military exploitation of the transistor set the pace for the ultimate large scale commercial/industrial use in the late 1950s. The tens of millions of dollars applied by the military to transistor manufacturing methods, pilot line development, specification and testing resulted in devices acceptable for consumer/industrial application. The industrial development of the integrated circuit and the PLANAR transistor were capitalized on by the military in the exploitation of the military microcircuit. The first and only user of the microcircuit in the early and mid-1960s was the military. Today, however, integrated circuits are applied to many consumer products, resulting in improved performance and reliability.

The BS9000 system, used in the United Kingdom, is a prime example of the interrelationship among military and industrial applications and reliability. Simply stated in this system, a given electronic part, i.e., a transistor, is considered for more than one application. The same part type may be considered for consumer, professional, military, and aerospace applications. The degree of quality and reliability is dictated by the parameter limits, quality levels, environmental and life requirements spelled out in the detailed specification. The basic and generic specifications for electronic part classes are common.

REFERENCES

1. Ryerson, C.M.,"The Reliability and Quality Control Field from Its Inception to the Present," Proc. IRE, Vol. 50, May 1962.

2. Peck, D.S., and C.H.Zierdt, "The Reliability of Semiconductor Devices in the Bell System," Proc. IEEE, Vol. 62, No. 2, Feb. 1974.

3. Vaccaro, J.,"Semiconductor Reliability Within the U.S. Department of Defense," Proc. IEEE, Vol. 62, No. 2, Feb. 1974.

4. Bridges, J.M.,"Integrated Electronics in Defense Systems," Proc. IEEE, Dec. 1964.

5. Asher, N.J.,and L.D.Strom, "The Role of Department of Defense in the Development of Integrated Circuits," IDA Paper, p. 1271, May 1977.

6. Sumney, L.W.,"VLSI With a Vengeance," IEEE Spectrum, April 1980.

7. Reich, B.,"Military IC Standardization Acquisition and Technology," Proceedings of the 1975 Annual Reliability and Maintainability Symposium.

8. Anon. Electronics Magazine, Special Commemorative Issue, April 17, 1980.

1.1.2 NEED FOR RELIABLE COMPONENTS

1.1.2.1 INTRODUCTION

The ultimate goal of a circuit designer is to produce circuits which when assembled into an end-item subsystem or system will enable the equipment to perform its intended function with less than a defined percentage of downtime due to equipment malfunction. To do this, the designer must have knowledge of all facets of reliability, some of which are:

(a) The relationship of component reliability to system reliability
(b) The causes of component failure including electrical, environmental, and mechanical stress
(c) How reliability is measured
(d) The various methods in achieving reliability assurance by specification
(e) The factors involved in the selection of the required components
(f) The effect of circuit design upon overall system reliability

There are also some other, more subtle aspects to component reliability that should be addressed by the system designer. These include:

(1) Component safety in end-item use
(2) Problems associated with part selection in situations where repair is either not possible or impractical
(3) The choice of parts in a critical application
(4) The life cycle costs associated with the choice of a part

1.1.2.2 COMPONENT SAFETY

Part failure in its end-item application will occur either instantaneously or later in its intended purpose. A failed part may also have a secondary or lingering property which can cause additional damage to other parts of the system and may even affect human life. MIL-STD-454 treats personnel safety from an equipment design and development basis in Requirement #1. The component safety aspects are treated in specific materials and component requirements throughout the MIL Standard. For example, Requirement #3 requires that flammable materials which will support combustion or cause an explosion (such as materials used for electrical insulation or mechanical support purposes) shall not be used in electronic equipment. Only materials classified as non-burning or self-extinguishing will be used. This requirement relates to circuit or part potting compounds as well as conductor insulating material.

A specific example of the importance of Requirement #3 is cited here. During the development stages of plastic encapsulated semiconductors, it was found that when some devices failed in the short-circuit mode, a hazardous condition would develop. The diameter of one of the internal connector wires was such that it would not act as a fuse and open; therefore, current would continue to flow through the shorted device. In this stage of plastic encapsulated device development, flame retardant materials were not used and as a result of continued heating, the plastic material could burst into flame and cause fire in the end equipment.

Requirement 11 (Insulating Materials, Electrical) addresses specific material requirements including safety aspects. MIL-STD-454 also addresses the possibility of certain material emitting carcinogens. These materials are clearly identified. The toxicity of a substance included for use in an electronic component must be considered.

1.1.2.3 NON-REPAIRABLE EQUIPMENT SITUATIONS

In some military applications equipment repair is not possible by virtue of the inaccessibility of the end item. One such application could be a space satellite where redundancy may not be feasible throughout the system because of weight and size limitations. One of the most effective ways of insuring the reliability of such systems is by means of controlling, in its broadest sense, the quality of the part applied. Screening is a key element in the production of electronic equipment required for hi-rel applications. Cost/reliability tradeoffs dictate the required screening, be it at the part, assembly or subsystem/system level.

Military parts can be procured to meet the requirements of nonrepairable equipment. Table 1.1.2.3-1 illustrates some of the generic part types available for hi-rel applications, indexed for all military applications when the appropriate screening level is chosen. For a hi-rel application it is advisable to chose the highest reliability parts, i.e., Class S for microcircuits, JANS for semiconductors, Class M for resistors, etc.

TABLE 1.1.2.3-1: PART TYPE VS. SCREENING DESIGNATOR

Part Type	Screening Designator
Microelectronics	S, B
Discrete Semiconductors (Transistors, Diodes, etc.)	JANS, JANTXV, JANTX, JAN
Resistors (Established Reliability, ER)	M, P, RS
Capacitors (Established Reliability, ER)	L, M, P, RS
Relays (Established Reliability, ER)	L, M, P, R
Coils, Molded (Established Reliability, ER)	M, P, RS

As an example, Method 5004 MIL-STD-883 defines the screening required for a Class S microcircuit which would be used in a nonrepairable equipment situation. For the Class S device the most stringent screening requirements are applied. One of the screening requirements applied for Class S measurements is: Method 2010A, Test Condition A, Internal Visual which provides the most vigorous and detailed procedure for internal visual inspection intended for high reliability Class S measurements. In addition, Method 2020 Particle Detection Test is applied to detect loose particles in the device enclosure. Both normal burn-in and reverse bias burn-in are required per Method 1015, the former burn-in lasting 240 hours. Both fine and gross leak screens for Method 1014 are also required.

In addition to the above screens, MIL-M-38510 requires manufacturer's line certification for Class S devices.

In addition to extensive parts screening, workmanship defects at higher orders of systems integration may be screened by a combination of temperature and equipment power cycling, coupled with vibration.

The combination of the above screening methods are the best means available to insure reliability for the nonrepairable equipment/system application.

1.1.2.4 CRITICAL FUNCTIONS APPLICATIONS

The size and complexity of some military equipment such as, for example, a large telephone switching central terminal is such that the system design and device reliability are clearly interrelated. The system design must provide the necessary features to assure acceptable user service while tolerating part failures expected for a known part reliability. Because of the factor of equipment size and complexity an important consideration is the significance of tradeoffs between device reliability and device cost and between system tolerance for device failure and system operating cost. With the multiplying factor of large device usage in a complex system, device cost is obviously a critical consideration but so also is the cost of system repair due to service failure. Therefore, a tradeoff must be made between the device type to be chosen versus the cost of removing a failure. Table 1.1.2.4-1 cites examples of costs of failure removal at different levels of circuit integration for parts to be applied in military environments and space applications.

TABLE 1.1.2.4-1: COSTS OF REMOVAL AT LEVELS OF PART/CIRCUIT INTEGRATION

Cost ($) for	Incoming Part	Removal at Printed Circuit Board	Removal at Systems Test	Field Removal
Military	10.50	75.00	180.00	1500.00
Space	22.50	112.50	450.00	- -

1.1.2.5 LIFE CYCLE COMPONENT COST

The project engineer on the military equipment has the responsibility of choosing the parts that go into the equipment/system. Very often the choice is between a standard and a nonstandard part. The details and benefits of parts control and selection including the specification hierarchy will be covered in another section of this handbook. At this point in the handbook the prime purpose is to acquaint those involved in parts control and selection with the costs involved in choosing nonstandard parts.

When choosing standard parts the costs of developing the specification, qualification and logistic support are inherently included in the overall part cost. When a nonstandard part is chosen the cost of developing the specification and qualifying the part is borne by the project requiring the item.

o Cost of Documentation/Specifications. Listed below in Table 1.1.2.5-1 are the costs involved in the preparation of documentation for a variety of electronic parts as estimated by the Defense Electronics Supply Center.

TABLE 1.1.2.5-1: COSTS OF DOCUMENT PREPARATION (Non-Standard Parts)

Component Part	Documentation Cost ($)
Passive Parts (Resistors, Capacitors, etc.)	400-3625
Microcircuits	600-5500
Discrete Semiconductors	400-4250
Other Electronic Parts	450-6150

o Cost of Qualification/Testing. Prior to the use of new or nonstandard parts responsible equipment/system developers must assure themselves of the quality and reliability of the part selected, as shown in Table 1.1.2.5-2.

TABLE 1.1.2.5-2: COSTS OF QUALIFICATION/TESTING (Non-Standard Parts)

Component Part	Testing Cost ($)
Passive Parts (Resistors, Capacitors, etc.)	5,000
Microcircuits	25,000
Discrete Semiconductors	10,000
Other Electronic Parts	5000-6000

o Logistic Costs. Finally, entering a new item into the supply inventory adds the additional costs of item entry and management for at least a 10 year period. Shown in Table 1.1.2.5-3 are the costs of such actions.

TABLE 1.1.2.5-3: LOGISTIC SUPPORT COSTS (Non-Standard Parts)

Entry of Item (National Stock Number (NSN), Assignment)	$ 207
Management of NSN for 10 years	$1650
Total Logistic Cost	$1857

1.1.3 PRESENT STATE OF THE ART

The state-of-the-art in component development is paced by the advances in LSI, VLSI and VHSIC microcircuit technology. Through the late 1950's and early 1960's, the circuit designer's problems were limited to choosing passive and active parts and integrating these individual parts into a circuit function, i.e., amplifier, oscillator, switching circuit, etc. The invention and implementation of the integrated circuit made it necessary for the circuit designer to have a broader knowledge not only of circuit function complexity but also of the basic materials and processes needed for microcircuit fabrication. The emergence of Very Large Scale and Very High Speed Integrated Circuits will be even more demanding on the designers who will be required to understand the total technology employed in integrated circuit manufacture as well as the ultimate system design.

The presentation in this portion of the Handbook is directed towards those whose job functions require a comprehension of all the aspects of integrated circuit technology from basic materials and processing to final packaging ready for circuit integration. In this treatment attention will also be given to passive devices used in the microcircuit environment.

1.1.3.1 SEMICONDUCTOR TECHNOLOGY AND MATERIALS

There are many types of semiconductor materials. The earliest was germanium, which was used to fabricate the first transistors but whose temperature limitation to approximately 75°C for practical devices made it unattractive for high reliability military applications. Silicon discrete transistors emerged in the 1950's and reached their maturity in the early 1960's, and silicon is today the most popular and widely used semiconductor material. The silicon transistor overcame the temperature limitation of germanium and operation to approximately 175° became possible. Consideration was given to an even higher temperature device material, gallium arsenide, but its use has been primarily directed at the development of higher frequency discrete devices, i.e., Schottky barrier diodes, varactor diodes, Gunn devices and light emitting diodes. There is now some exploratory work being done in the application of gallium arsenide material to the fabrication of monolithic high frequency integrated circuits (see Section 1.1.4.2).

1.1.3.1.1 CLASSES OF SEMICONDUCTOR DEVICES

Both discrete semiconductor and microcircuit devices can be characterized in the manner shown below in Figure 1.1.3.1.1-1. The system designer applying semiconductor devices will be confronted with some or all of the configurations shown.

The differing features between a bipolar device and a field effect or unipolar device relate to the composition of current flow; the bipolar have two components, the unipolar a single component. In the semiconductor classes of Figure 1.1.3.1.1-1 a single semiconductor type material like silicon is assumed.

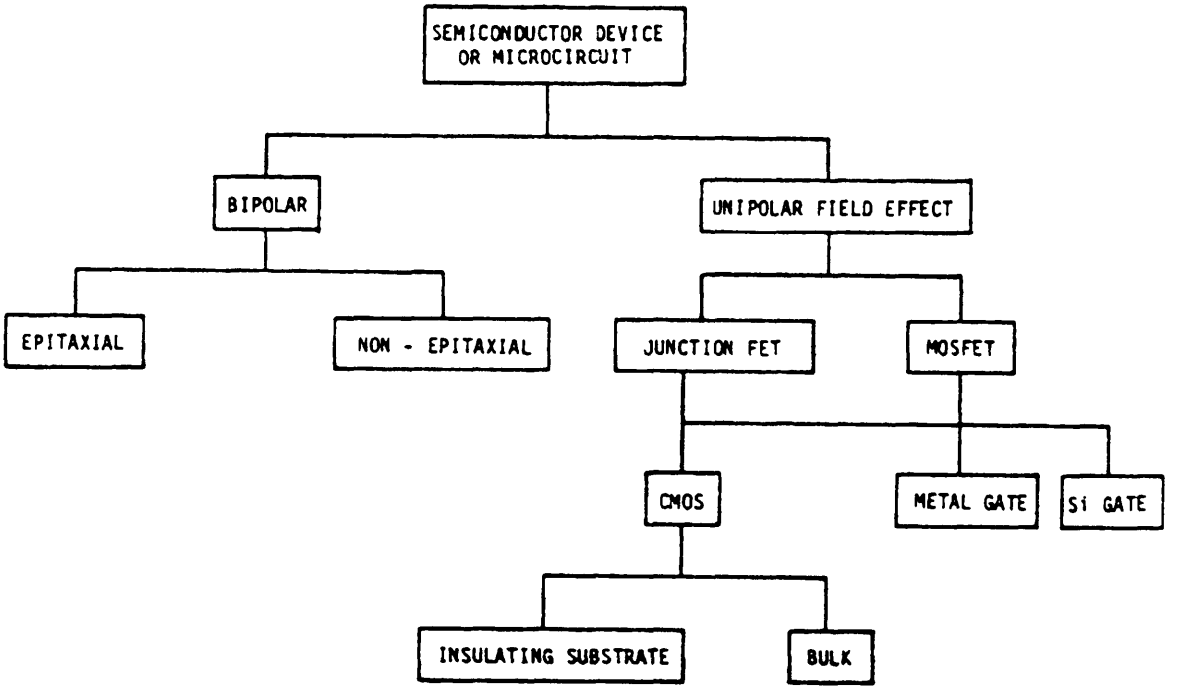


FIGURE 1.1.3.1.1-1: SEMICONDUCTOR CLASSES

1.1.3.2 SEMICONDUCTOR DEVICE MATERIALS AND PROCESSING

Figure 1.1.3.2-1 presents generically the material and processes used in the fabrication of semiconductor devices and microcircuits. There are two major stages in the creation of a finished device. The first is the fabrication of the active and passive devices at the chip level. The second stage relates to the final packaging of the chip within a controlled environment to insure device reliability over extended periods. Reagents and gases serve in an ancillary manner to aid the diffusion process and for cleansing the wafers during the overall processing cycle. One process aid not shown in Figure 1.1.3.2-1 but which is particularly required in both the doping and the interconnection process is the fabrication and use of masks.

1.1.3.2.1 PHOTOFABRICATION

In order to process the integrated circuit through the steps which define the active and passive devices and their ultimate interconnection, a series of masks must be generated. The masks are used in conjunction with photolithographic processing to produce the desired circuit function in the smallest possible area. The selective deposition into and removal of material from the silicon wafer is required in the manufacture of circuits.

For the production of bipolar circuits from five to ten masks may be required; for an MOS circuit four to seven masks may be required. Figure 1.1.3.2.1-1 illustrates a series of masks that may be required to fabricate a microcircuit wafer.

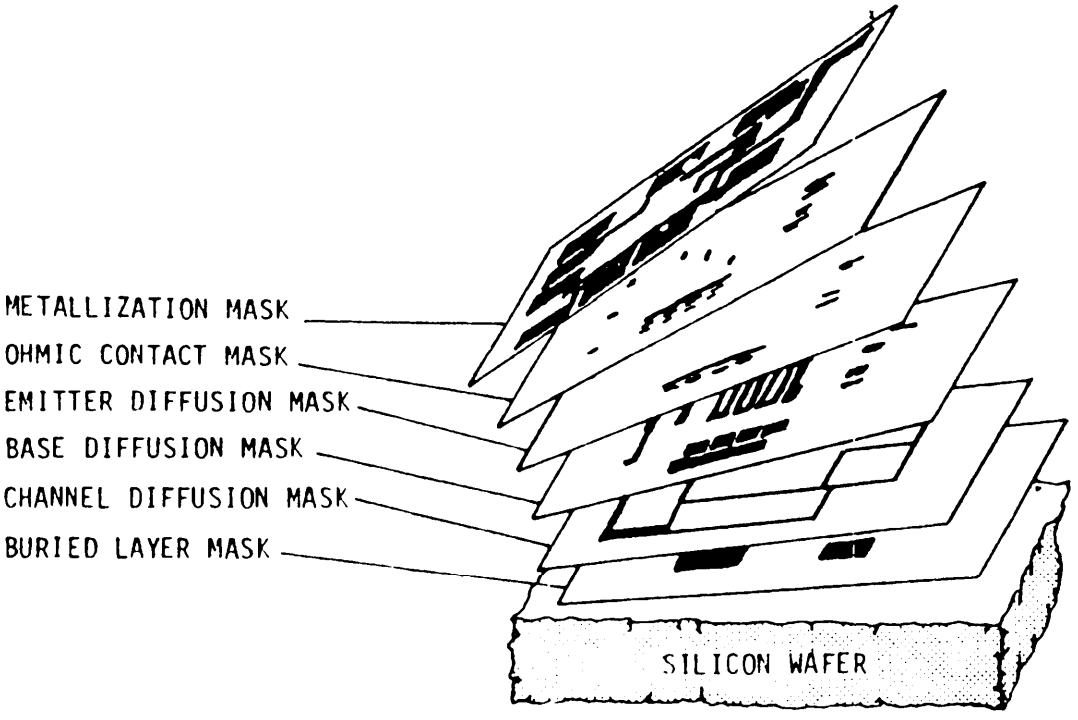


FIGURE 1.1.3.2.1-1: SERIES OF PHOTO MASKS NEEDED TO FABRICATE A BIPOLAR IC

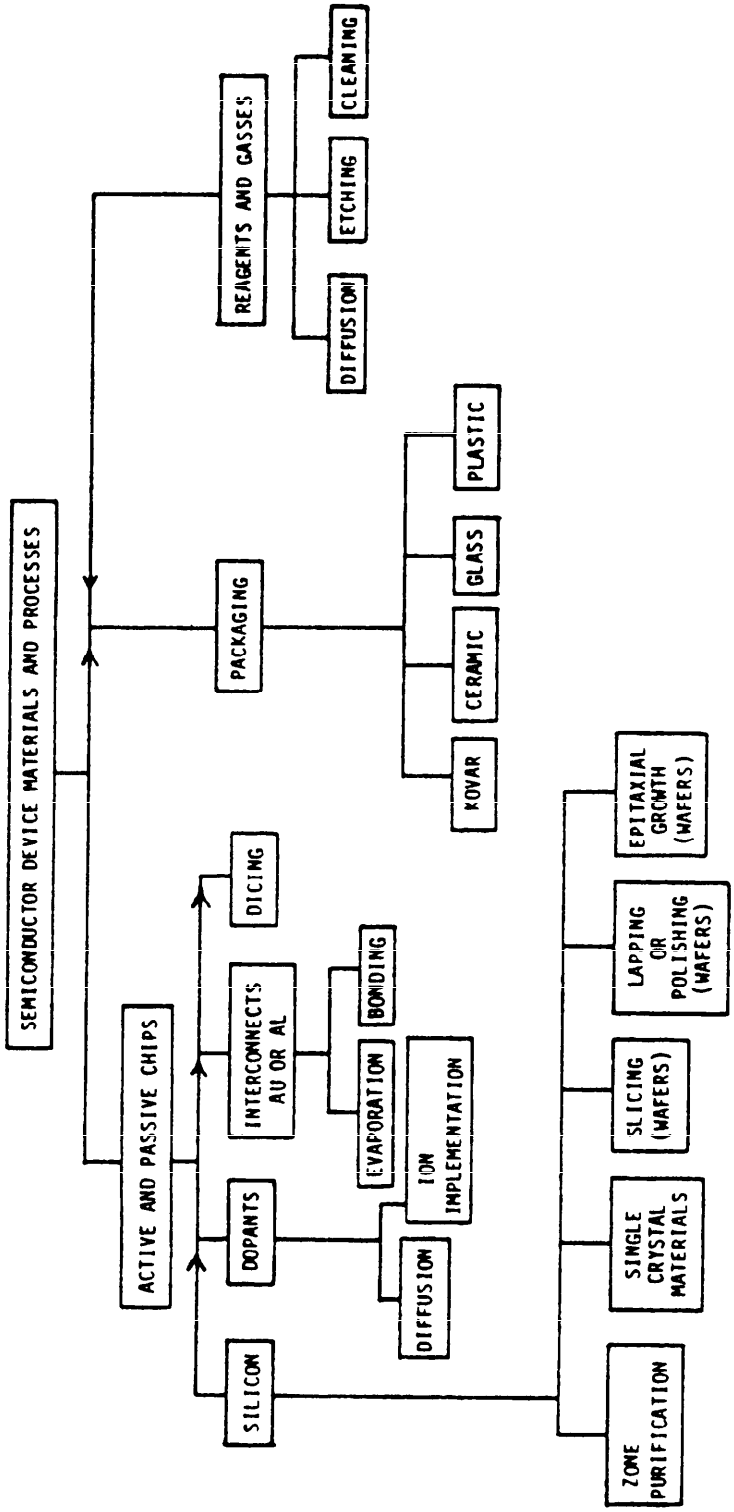


FIGURE 1.1.3.2-1: MATERIALS AND PROCESSES USED IN SEMICONDUCTOR FABRICATION

In order to generate one of the required masks a series of three basic steps are required:

- o Initial Artwork
- o Photoreduction
- o Final Mask Copies

Usually the initial artwork from which photomasks are made is a very accurate drawing, 100-1000 times final size, produced by exposing a photographic film on a computer-controlled drafting machine called a coordinatograph. The typical initial artwork is usually 1 x 1 meter and reflects the geometric representation, when ultimately reduced to required size, to be applied to the microcircuit.

The production of the final photographic masks to final dimensions from the original artwork requires a reduction in size and faithful replication of the images so that many circuits can be processed simultaneously on a large substrate. The reduction from original artwork to final dimensions is accomplished in stages by a "step-and-repeat process" resulting in an array of as many as several hundred identical images representing the number of identified chips on the wafer. This generates the master mask.

Numerous copies of the master mask must then be replicated for production purposes. The life of a single photographic emulsion mask copy is between ten and twenty mask operations when extreme care is exercised in its use.

1.1.3.2.2 PHOTOLITHOGRAPHY

It has been established that the circuit implementation on a silicon substrate is accomplished by a series of diffusion and interconnection steps. The geometrical patterns applied to the wafer substrate are defined by a series of masks. The mask pattern and its implementation on the chip is accomplished through the use of photoresist materials. Photoresists are organic compounds whose solubility is affected by ultraviolet light. There are two classes of photoresist: negative and positive. For the negative resist ultraviolet light causes the exposed area to have lower solubility in the solvent (developer) whereas in a positive resist the exposed areas are more soluble in the developer. Each photoresist operation in an IC fabrication sequence has many steps. These consist of (1) initial cleaning and baking (2) resist application (3) resist exposure (4) developing and (5) rinsing and cleaning.

1.1.3.2.3 FILM TYPE INTEGRATED CIRCUITS

There is another very important class of integrated circuits known as film integrated circuits whose elements are formed in situ upon an insulating substrate. In the case of monolithic silicon integrated circuits the silicon material performs the circuit function following suitable processing steps such as function formation and interconnection. In the case of film circuits the substrates are usually inert, with the one notable exception of microwave film circuits where the dielectric properties of the substrate are very important.

Hybrid integrated circuits are those employing more than one type of circuit technology in their makeup. Therefore a film integrated circuit which may have passive components deposited along with bonded silicon monolithic circuits integrated by interconnect metallization is considered a hybrid integrated circuit (also called a hybrid microcircuit). There are two types of film circuits: thick film and thin film.

1.1.3.2.3.1 THICK FILM CIRCUITS

A thick film circuit consists of passive elements which are formed in place on the substrates by the selective application of materials in the form of paste. These pastes are subsequently fired at high temperature to form the desired films. (Usually discrete components, such as resistors, capacitors, and integrated circuits are then added to form the hybrid microcircuit). There are a number of factors favoring thick film screened microcircuits. Some of these are:

- Lower cost than other film approaches
- Quick response time
- Simple drafting procedures
- Reliable added components with desired properties and quality
- A versatile technology permitting easy addition of discrete components.
- Compatability with flow soldering techniques
- Fabrication by moderately skilled assemblers

o Description of Thick Film Process: The materials that will ultimately form the thick film are prepared as a suspension or emulsion of conductive or dielectric particles in a suitable organic vehicle of solvents. The suspension materials are then forced through a screen by means of a moving squeegee to form the desired geometrical pattern. Analogous to a conventional screen printing process, these suspensions of particles are called inks. Thick film inks consist of the following:

- Finely divided metal or metal alloy powders which give the film cohesion. In the case of conductive film these metals determine the electrical conductivity.
- Metallic oxides which in the case of resistive film determine film resistivity.
- Finely divided glass frits which determine the adherence of the film to the substrate.
- An organic vehicle to provide required flow properties of the films and can later be evaporated during firing of the film.

Two critical paste properties which control the print quality are viscosity and surface tension. The paste or ink must not flow through the screen until forced to do so by the wiping action of the squeegee. Thereafter the paste must then adhere to the substrate and hold its form without screening when the screen is removed.

After the ink is screened onto the substrate (usually through a stainless steel mesh), it is air dried at about 25°C for five to fifteen minutes followed by a bake at 125-150°C to dry out the volatile solvents. The ink is then subjected to a firing sequence with temperatures ranging from 500°C to 1000°C followed by a cool-down cycle.

In the usual fabrication sequence for conductive and resistive films the conductive pattern is first screen printed and fired. The resistor pattern is deposited over the conductive terminations and fired at the same or lower peak temperature than the conductive pattern. Resistors are then abrasively or laser trimmed to the desired final value. The hybrid microcircuit is then completed by attaching components and wire bonding the necessary interconnections.

1.1.3.2.3.2 THIN FILM CIRCUITS

o Description of Thin Film Process: Thin film circuits generally consist of electronic components and circuits applied by vacuum evaporation, sputtering, chemical vapor deposition, electrolytic plating and electroplating techniques and defined by photofabrication. Thin film microcircuits are fabricated by a sequence of material deposition, photoresist pattern formation and etching steps in a manner very similar to the processing of monolithic integrated circuits.

In the processing of thin film circuits several precision photomasters are required to define the various conductor, resistor and capacitor patterns. These are employed sequentially with the respective deposition and etching steps, as is done with silicon microcircuits.

The substrate for most thin film circuits should be inert, acting as a carrier for the thin film components. A notable exception is the microstrip transmission line in which the substrate is an integral part of the circuit. The substrate requirements for thin film circuits are far more exacting than those for thick film circuits. One requirement is for a perfectly smooth surface to permit the growth of thin, defect free films. Commonly used substrate materials include aluminum, beryllium and various glasses. Thin film techniques capable of producing useful quantities of economical, reliable, uniform, active devices have not yet been developed economically. Although complete thin film passive circuits are available, active devices must be added separately.

1.1.3.3 PACKAGING

Several types of packages are used in silicon microcircuits. These are:

- Transistor type metal cans
- Ceramic dual-in-line packages (DIP)
- Ceramic flat packs
- Plastic dual-in-line packages (PDIP)
- Plastic or hermetic chip carriers

Generically, the metal type package was one of the first enclosures used for discrete transistors. It comes in two sections: a top cover made (usually) of Kovar, and a base or header (usually gold plated). Gold plated leads are glassed in place with the header portion of the package.

While the original metal can type package had only three leads, multi-individual packages were developed to accommodate integrated circuits. The individual circuit chip or die is eutectically bonded to the head prior to the welding of the top of the package header.

The dual-in-line package (DIP) was developed primarily for use in automatic assembly of printed wiring assemblies. One version consists of a ceramic base and tops and a Kovar lead frame separately mounted to the base with a glass frit. The chip is bonded either eutectically or by metal-filled epoxy to a gold-plated metal pad on the package base. The package is furnace sealed using a glass frit between bottom and top. In the case of plastic DIPs the chip is connected to a Kovar lead frame by bonding wires and the entire assembly subsequently encapsulated by being molded in epoxy, or sometimes other plastic materials, resulting in a rugged, inexpensive package. Unlike the ceramic DIP the plastic DIP is not considered hermetic and water easily permeates the package to the chip.

In the case of the DIP, the lead plane is perpendicular to the package plane. In the case of flat packs, the lead plane parallels the package plane. Flat packages result in higher packaging assembly levels but are not as adaptable to automated assembly of printed wiring boards as are the DIP packages. Chip carriers are quite similar to ceramic flat packs except that the contact leads are brought out in the film, near the edge of the package. This type of package achieves the highest packaging density.

1.1.3.4 TESTING OF ELECTRONIC PARTS

Three military standards exist which contain test methods and procedures applicable to MIL-specified component parts (see Section 5.1.2, Standard Part Selection). These documents can be of incalculable value to the design or project engineer faced with the problem of ensuring that procured parts will meet the required quality and reliability levels. These documents, MIL-STD-202, Test Methods for Electronic and Electrical Parts, MIL-STD-750, Test Methods for Semiconductor Devices, and MIL-STD-883, Test Methods and Procedures for Microelectronics, are briefly discussed below:

o MIL-STD-202 was originally proposed in the mid-1950's primarily to standardize the environmental test methods for both active and passive parts. With the increased sophistication of semiconductor and microcircuit technology, it became necessary to develop individual test standards to cover these latter classes of component parts. Therefore, MIL-STD-202 in its present version established uniform methods for testing electronic and electrical component parts, including basic environmental tests to determine resistance to deleterious effects of natural elements and conditions encountered in military operations. Passive parts as related to MIL-STD-202 are such items as capacitors, resistors, switches, relays, transformers, and connectors. The tests described in this Standard are divided into three classes: Test Methods 101 to 199 inclusive cover environmental tests; those numbered 201 to 299 inclusive cover physical characteristic tests; and those numbered 301 to 399 inclusive cover electrical characteristic tests. Tables 1.1.3.4-1, 1.1.3.4-2 and 1.1.3.4-3 list some test method numbers and test method titles for all three test categories.

TABLE 1.1.3.4-1: ENVIRONMENTAL TESTS (100 CLASS)

Test Method Number	Test Method Title
101	Salt Spray (Corrosion)
103	Humidity (Steady State)
104	Immersion
105	Barometric Pressure (reduced)
106	Moisture Resistance
107	Thermal Shock
108	Life (elevated temperatures)
109	Explosion
110	Sand and Dust
111	Flammability
112	Seal

TABLE 1.1.3.4-2: PHYSICAL CHARACTERISTIC TESTS (200 CLASS)

Test Method Number	Test Method Title
201	Vibration
204	Vibration, High Frequency
206	Life (Rotational)
207	High-impact Shock
208	Solderability
209	Radiographic Inspection
210	Resistance to Soldering Heat
211	Thermal Strength
212	Acceleration
213	Shock (Specified pulse)
214	Random Vibration
215	Resistance to Solvents
217	Particle Impact Noise Detection

TABLE 1.1.3.4-3: ELECTRICAL CHARACTERISTIC TESTS (300 CLASS)

Test Method Number	Test Method Title
301	Dielectric Withstanding Voltage
302	Insulation Resistance
303	DC Resistance
304	Resistance - Temperature Characteristic
305	Capacitance
306	Quality Factor
307	Contact Resistance
308	Current Noise Test for Fixed Resistors
309	Voltage Coefficient of Resistance
310	Contact-Chatter Monitoring
311	Life Low-level Switching
312	Intermediate Current Switching

o MIL-STD-750 was developed in the early 1960's to address the specific needs for testing discrete semiconductor devices. Many additions and changes have been made since that time to enhance the utility of the document. MIL-STD-750 is structured similarly to MIL-STD-202 in that five classes of test methods are established. The 1000 Class of Test Methods covers Environmental Tests. The 2000 Class covers Mechanical Characteristic Tests; the 3000 Class covers Electrical Characteristic Tests for Transistors; the 3100 Class covers Circuit Performance and Thermal Resistance Measurements and the 3200 Class covers Low Frequency Tests.

Some notable test methods usually associated with semiconductor reliability in the 1000 Class are Methods 1026 and 1027 covering steady-state, operational life and Methods 1031 and 1042 covering nonoperational or storage life of semiconductor devices. Methods 1038, 1039 and 1040 cover burn-in tests for diodes and rectifiers, transistors, and thyristors, respectively. However, screening requirements (including burn-in) for JANS, JAN TXV and JANTX are covered in the General Specification for Semiconductor Devices MIL-S-19500. Also to be found in MIL-S-19500 are the Quality Assurance Requirements for: Group A Inspection which includes primarily electronic test (Classes 3000 and 3200), Group B Inspection which includes primarily mechanical and environmental test (Classes 1000, 2000, and 3100) and Group C or periodic tests primarily for design verification of the semiconductor (Classes 1000 and 2000). MIL-S-19500 also specifies which of the test methods of MIL-STD-750 are considered destructive and those which are considered nondestructive.

o MIL-STD-883 was developed by the Air Force in the mid to late 1960's to address the needs for testing microelectronic devices. Many additions and changes have been made since that time to enhance the utility of the document. Since it was the primary microelectronic testing document, preceding the General Specification for Microcircuits (MIL-M-38510), it is more inclusive than MIL-STD-750. (As noted in the presentation on MIL-STD-750, information on qualification, quality conformance and burn-in sequences are found in MIL-S-19500). MIL-STD-883, however, is self contained in this respect. As with MIL-STD-750, MIL-STD-883 is structured into five classes of Test Methods: the 1000 Class addresses Environmental Tests, 2000 Class addresses Electrical Tests; 3000 Class addresses Electrical Tests for Digital Circuits; 4000 Class addresses Electrical Tests for Linear Circuits; and the 5000 Class addresses Test Procedures.

Some notable test methods usually associated with microelectronic reliability in the Class 1000 Methods are: Methods 1005 and 1006 covering Steady State and Intermittent Life; Method 1007, Agree Life; Method 1008, High Temperature Storage; Method 1015, Burn-in Test. In Class 2000: Method 2010 covers Internal Visual (monolithic); Method 2017 covers Internal Visual (hybrid); Method 2011, Bond Strength; and Method 2018, Scanning Electron Microscope (SEM) Inspection of Metallization. The 5000 Class Test Methods cover Screening Procedures, Method 5004.4, and Qualification and Quality Conformance Procedures Method 5005.4. The above summary of some of the Test Methods does not imply that those methods not specifically spelled out are not important to the quality and reliability of microcircuits.

Test Method 5004 Screening Procedures addresses screening including burn-in requirements for Class S, and Class B microcircuits. Test Method 5005 addresses qualification and Quality Conformance Procedures. Four groups of testing are specified: Group A covers Electrical Test requirements; Group B addresses Mechanical and Environmental Tests; Group C addresses die-related Mechanical and Environmental Tests and Group D addresses package-related Mechanical and Environmental Tests.

REFERENCES

1. MIL-STD-202 - Test Methods for Electronic and Electrical Parts
2. MIL-STD-750 - Test Methods for Semiconductor Devices
3. MIL-STD-883 - Test Methods and Procedures for Microelectronics

1.1.4 FUTURE TRENDS

While over the past thirty years electronic circuitry has undergone a tremendous reduction in size coupled with an impressive increase in complexity, more is yet to come. By the use of recognizable objects for comparison, Table 1.1.4-1 graphically illustrates the proportionate miniaturization which has taken place in one type of equipment (i.e., computers) since the days when the use of electron tubes was prevalent through today's use of LSI microcircuits, the use of VLSI microcircuits in the mid-80's and the expected use of ultra-LSI devices by the '90's.

We are not at the ultra-LSI stage yet, but developmental work is well underway in programs designed to develop new switching speeds, increased device complexity and new integrated circuit manufacturing technology.

1.1.4.1 VHSIC

The VHSIC program was initiated in 1980 by the U.S. Department of Defense to develop VLSI signal processors which will possess several hundred times higher speed and computing capability than LSI devices available at that time. The planned processors must also consume less power and be smaller and more reliable than contemporary technology would allow. Their application will be solely military, with no commercial or industrial counterparts - mainly real time signal processing for weapons systems of the next decade. VLSI systems will be more reliable than equivalent assemblies of LSI (Large Scale Integration) or MSI (Medium Scale Integration) devices, since they will contain fewer major sources of failure such as power chips and external connections. The principal limitation of contemporary system technology is the fact that systems contain from five to twenty MSI chips, discrete components, power supply, and input/output for each LSI chip. The increased reliability of VLSI circuits will reduce the cost of unscheduled maintenance, a major reason for lost operational time in many weapons systems.

Military electronic subsystems have grown so complex that, despite the steadily improving reliability of integrated circuits, the failure rate of advanced systems has become a serious problem. The point has been reached where the military can no longer devote increased computing power to improving performance alone. The higher complexity of VLSI circuits must also be used to improve reliability.

The goal of the VHSIC program is pilot production in the latter half of the 1980 decade for processors containing 250,000 gates, operating at clock speeds of 25MHz and performing several million to several billion operations per second. The gates would be fabricated by MOS or bipolar technology and have minimum dimensions of 0.5 to 0.8 micrometers. The required speed and circuit density would be obtained both by scaling down current LSI circuits and by developing new types of system architecture and software.

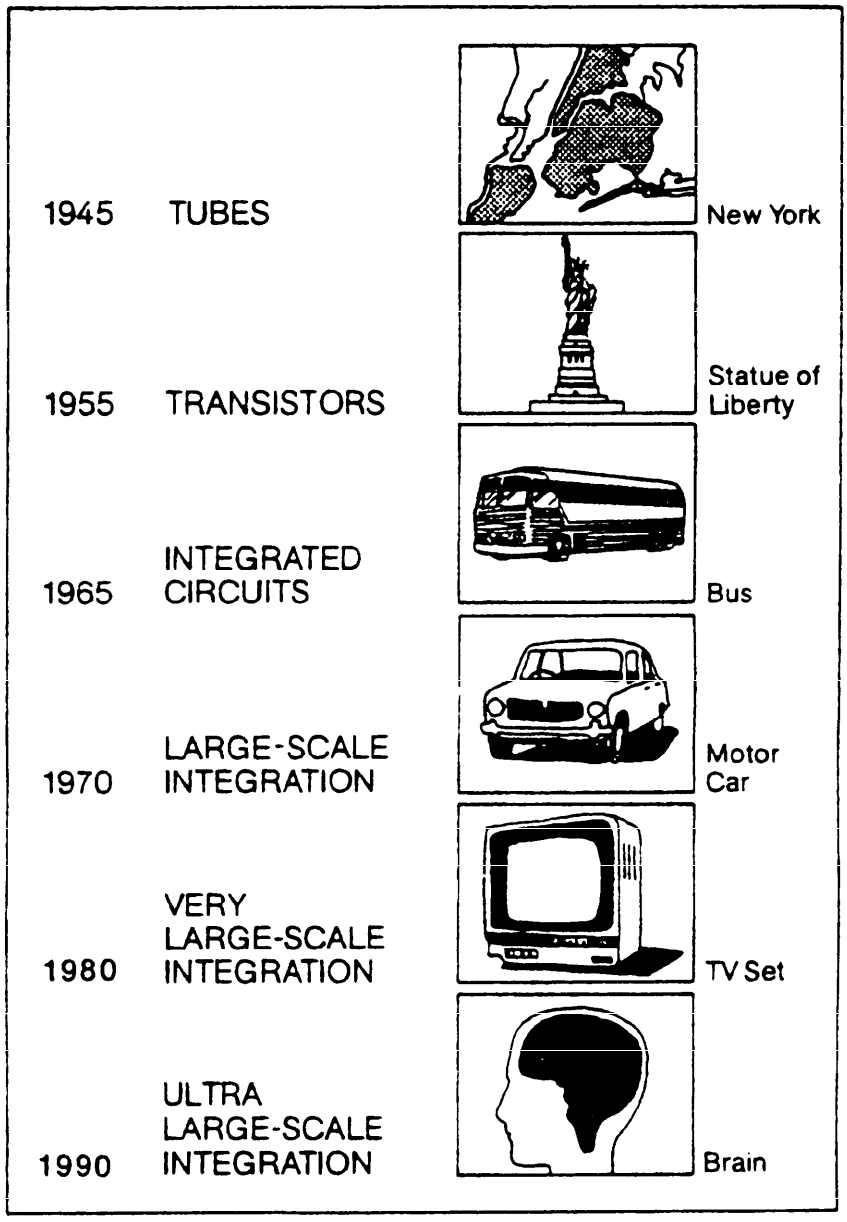


TABLE 1.1.4-1: TRENDS IN MINIATURIZATION

Concurrent with the development of these VLSI processors will be the development of test techniques and test equipment capable of verifying the functional capabilities of the devices. The very high switching speed and very large scale integration goals of the VHSIC development program will spawn the development of a new generation of automatic test equipment.

1.1.4.2 OTHER NEW TECHNOLOGIES

Silicon has historically dominated integrated circuit technology development as the primary semiconductor material. The only minor variation of silicon as a basic substrate material uses a layer of silicon epitaxially grown on sapphire substrates and is commonly referred to as Silicon-On-Sapphire (SOS).

In recent years attention has been focused principally on Gallium Arsenide (GaAs) as a substrate material destined to achieve performance superior to that of silicon.

Figure 1.1.4.2-1 reveals the increased capability of GaAs over silicon. Electron mobility of GaAs is between five and six times that of silicon. This characteristic, coupled with the semi-insulating substrate of GaAs, leads to the increased performance of GaAs versus silicon in both speed and power consumption.

Properties	Silicon	GaAs
1. Mobility (cm^2/V-sec)		
μ_n (Electrons)	1500	8500
μ_p (Holes)	600	400
2. Maximum Operating Temperature (^oC)	200	350
3. Minor Carrier Lifetime (sec)	2.5×10^3	2×10^8
4. Energy Gap (eV)	1.12	1.43
5. Breakdown Field (V/cm)	3×10^5	4×10^8
6. Relative Abundance in Earth's Crust (gm/ton)	227,200	$\frac{Ga}{15}$ $\frac{As}{5}$

FIGURE 1.1.4.2-1: PROPERTIES OF SILICON AND GaAs AT 300^oK

Gallium Arsenide (GaAs) integrated circuit technology is now emerging from the laboratory into the realm of application in a variety of electronic equipment. The silicon industry will begin to feel the dramatic impact of GaAs ICs during the last year or two of this decade.

During the coming decade, GaAs ICs will be demand driven, fitting into applications not easily solved by other technologies. High interest in the development of GaAs IC technology exists among a number of nontraditional IC suppliers. Most of this interest arises from projected in-house needs, with only a handful of companies expected to enter the market as merchant suppliers. The U.S. government fuels a large amount of the interest with funding to several companies for development of GaAs IC technology for military applications.

Initial GaAs IC products are expected to emerge by the end of 1981 and will perform analog functions in applications such as amplifiers, modulators, mixers and multiplexers. Digital IC functions will appear by 1983 at the latest. Initial products will perform simple functions dominated by a large number of custom circuit applications. Eventually, following a period of technology evaluation and acceptance, applications will proliferate, high volume standard product circuits will arise and total industry sales will accelerate.

GaAs IC technology will solve a multitude of problems not easily solved or not solvable at all by other technologies. At this time there is not a lack of potential applications; rather, there is a lack of production experience.

As production experience grows, however, prices will fall and market elasticity will show up in increased demand for GaAs IC circuit functions. Military systems and IC test equipment requirements will drive initial applications in the U.S., while satellite-to-home TV receivers will dominate in Europe and Japan.

The strong GaAs discrete transistor technology and market which emerged in the last few years will serve as a foundation for the initial GaAs IC products, primarily analog functions. Future process trends include MOSFET structures, new oxide growth and deposition techniques, and refinements in ion implantation methods and equipment. Materials will evolve with a movement to Liquid Encapsulated Czochralski (LEC), which have lower defect densities and costs. Suppliers and users alike will make major efforts to establish reliability.

Three digital IC technologies under advanced development exhibit potential for significantly increased future performance: N-channel MOS silicon-gate technology; Josephson junction technology; and Gallium Arsenide technology. Josephson junction devices have achieved the best performances recorded to date in research laboratories.

A substantial number of practical problems remain to be solved in this technology, however, many of which are centered on the cryo-cooler system necessary to achieve the $4^{o}K$ operating temperature of the Josephson junctions.

Despite the problems, Josephson junctions have achieved single-stage delays of 13 picoseconds. For more realistic operating conditions, where each logic gate has multiple inputs and a fan-out of three, the average delay would be about 35 psec per logic gate. The power dissipation of such a typical gate would be approximately 10 uW.

N-channel MOS silicon-gate technology was first realized on a commercial basis in the early 1970s. Recent efforts concentrate on achieving higher speeds and circuit densities by reducing critical circuit dimensions. Single-stage delays of 300 psec have been achieved for power dissipations of less than 1 mW.

Most GaAs IC technology developments depend on a Schottky-gate MESFET structure. Current results tend to substantiate a six times speed improvement over silicon-based IC technology. At the same time, for comparable speeds, GaAs consumes 25 to 40 times less power than silicon.

Figure 1.1.4.2-2 shows a comparison of current capabilities of all three technologies, based on published reports. The diagonal lines represent limits of operability exhibiting a constant speed-times-power product. All three technologies currently possess minimum propagation delays that application of additional power cannot further reduce.

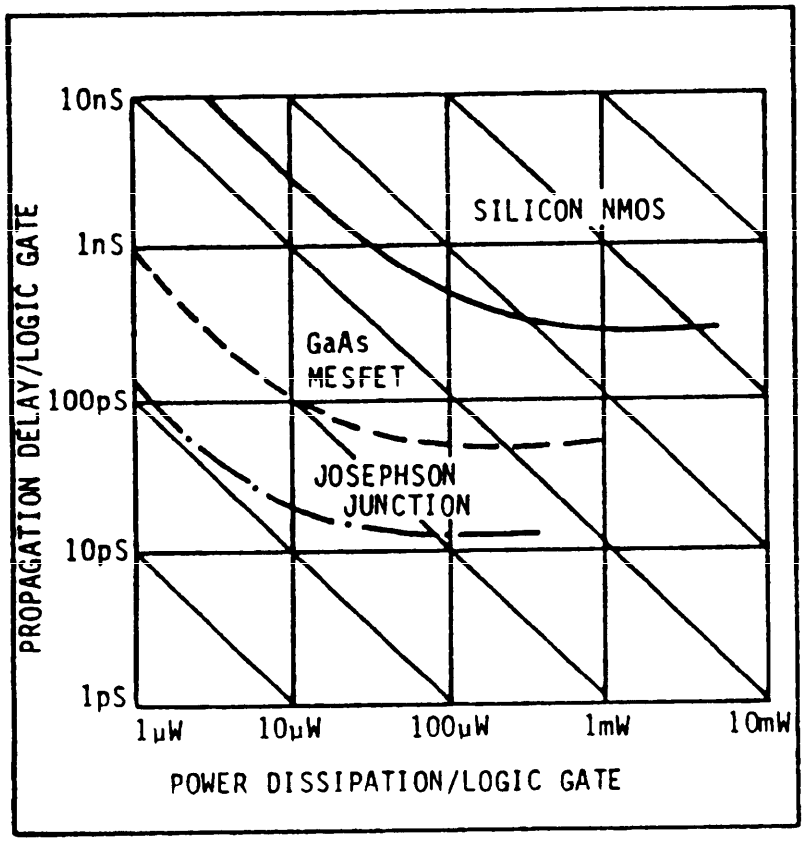


FIGURE 1.1.4.2-2: COMPARISON OF SPEED/POWER CAPABILITIES OF DIGITAL TECHNOLOGIES

The curves shown in Figure 1.1.4.2-2 are based on comparable conditions - typically, single fan-in or fan-out at nominal supply voltage and temperature (300°K for NMOS and GaAs, and 4°K for Josephson junctions). The results shown will likely improve somewhat with time, although intercircuit delays in the Josephson junction example constitute approximately 50% of the minimum reported logic delay of 13 psec.

Minimum logic delays for GaAs fall in the 50 psec range, with minimum NMOS silicon-gate circuits currently at 300 psec, or six times slower than GaAs. Both NMOS and GaAs circuit technologies will likely improve in speed and performance in the future, with GaAs remaining a multiple of five or six times faster than NMOS silicon gate.

Silicon bipolar technology has dominated the analog world since its inception. For frequencies less than several hundred megahertz, this dominance will likely continue. However, for applications requiring operating frequencies greater than several hundred megahertz, GaAs is rapidly becoming the dominant technology.

Initial applications of analog GaAs technology utilize discrete and dual-gate devices. Commercial GaAs transistors feature useful power gain up to 18 GHz. The maximum frequency of self-oscillation of these devices falls in the range of 50 to 70 GHz.

Even more astounding are the noise figures of GaAs discrete transistors designed especially for high-quality signal amplification. Figure 1.1.4.2-3 shows the noise figure capabilities of the GaAs transistors attained in various R&D laboratories. Commercial realization normally follows in about two years.

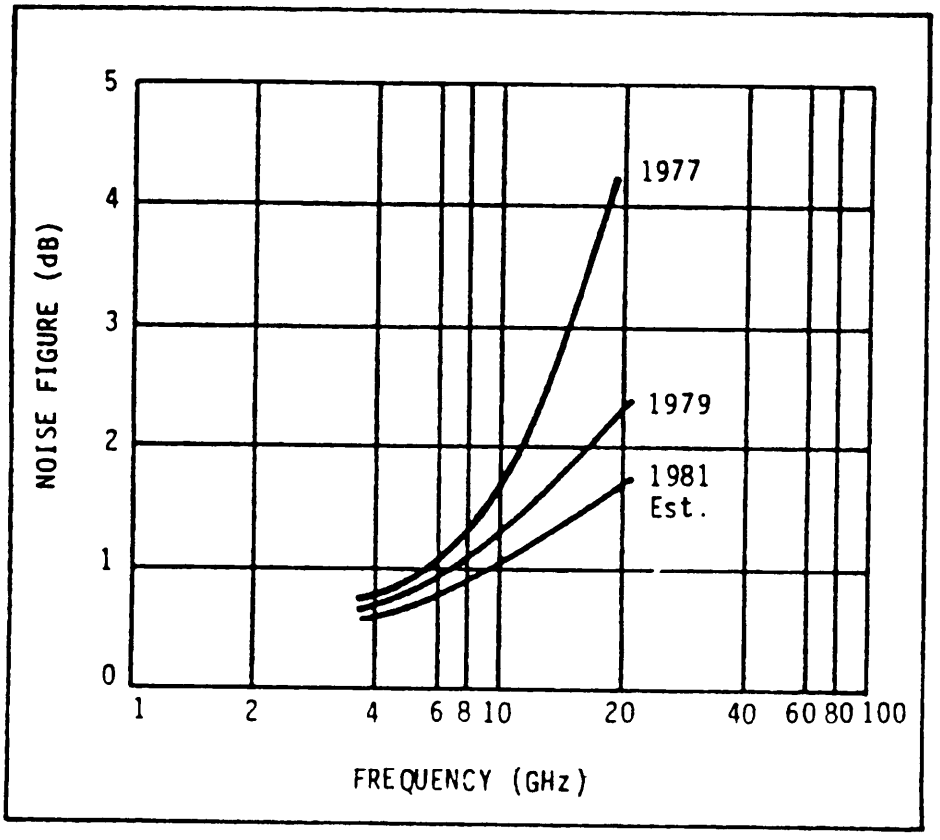


FIGURE 1.1.4.2-3: NOISE FIGURE PERFORMANCE OF GaAs LABORATORY DEVICES

The high-frequency capabilities of GaAs technology, coupled with superior noise performance, will lead initially to microwave IC modulators, mixers and amplifiers. Industry visionaries already predict complete microwave receivers on a single IC.

Currently, GaAs devices displace silicon devices in applications above 1 GHz where the noise figure is critical. For applications above the frequency range of 3 to 4 GHz, GaAs displaces silicon because of lower cost. The current useful upper frequency limit of silicon devices is approximately 6 GHz, while R&D laboratories have used GaAs to build a 30 GHz amplifier.

It is expected that GaAs analog ICs will not only take over the greater majority of applications with frequencies from several hundred gigahertz and up but will also promote an entirely new spectrum of applications because of their superior performance characteristics.

REFERENCES

1. Sumney, L.W., "VLSI With A Vengeance," IEEE Spectrum, April 1980.

2. Anon., "Gallium Arsenide Integrated Circuits," Circuits Manufacturing, Vol. 21, No. 2, February 1981.

3. Evans, C., The Micromillenium, The Viking Press, 1980.

2.0 REFERENCED DOCUMENTS

2.1 ISSUES OF DOCUMENTS

The following documents of the issue in effect on the date of invitation for bids or request for proposal, form a part of the Handbook to the extent specified herein.

SPECIFICATIONS

Military

MIL-E-1	Electron Tube, General Specification For
MIL-C-5	Capacitors, Fixed, Mica-Dielectric, General Specification For
MIL-C-17	Cable, Radio Frequency, Flexible and Semirigid, General Specification For
MIL-R-19	Resistor, Variable, Wirewound (Low Operating Temperature), General Specification For
MIL-C-20	Capacitor, Fixed, Ceramic Dielectric (Temperature Compensating) Established and Nonestablished Reliability, General Specification For
MIL-R-22	Resistor, Variable (Wirewound, Power Type), General Specification For
MIL-R-26	Resistor, Fixed, Wirewound (Power Type), General Specification For
MIL-T-27	Transformer and Inductor (Audio, Power, and High Power Pulse), General Specification For
MIL-W-76	Wire and Cable, Hookup, Electrical, Insulated
MIL-C-81	Capacitor, Variable, Ceramic Dielectric, General Specification For
MIL-C-92	Capacitor, Variable, Air Dielectric (Trimmer), General Specification For
MIL-R-94	Resistor, Variable, Composition, General Specification For
MIL-C-442	Cable, (Wire), Two Conductor, Parallel
MIL-C-3432	Cable (Power and Special, Purpose, Wire, Electrical, 300 and 500 Volts)

MIL-C-3607	Connector, Coaxial, Radio Frequency, Series Pulse, General Specification For
MIL-C-3643	Connector, Coaxial, Radio Frequency, Series HN, Associated Fittings, General Specification For
MIL-C-3650	Connector, Coaxial, Radio Frequency, Series LC
MIL-C-3655	Connector, Plug and Receptacle, Electrical (Coaxial Series Twin) and Associated Fittings, General Specification For
MIL-C-3767	Connector, Plug and Receptacle (Power, Bladed Type), General Specfication For
MIL-S-3786	Switch, Rotary Circuit Selector, Low Current Capacity, General Specification For
MIL-L-3890	Line, Radio Frequency Transmission (Coaxial, Air Dielectric)
MIL-S-3950	Switch, Toggle, Environmentally Sealed, General Specification For
MIL-C-5015	Connector, Electrical, Circular Threaded, AN Type, General Specification For
MIL-W-5086	Wire, Electric, Polyvinyl Chloride Insulated, Copper or Copper Alloy
MIL-R-5757	Relay, Electromechanical General Specification For
MIL-R-6106	Relay, Electromagnetic (Including Established Reliability (ER) Types), General Specification For
MIL-W-7072	Wire Electric, 600 Volt, Aluminum, Aircraft, General Specification For
MIL-C-7078	Cable, Electric, Aerospace Vehicle, General Specification For
MIL-W-8777	Wire, Electrical, Silicone Insulated, Copper, 600 Volt, 200 Degrees C
MIL-S-8805	Switches and Switch Assemblies, Sensitive and Push, Snap Action, General Specification For
MIL-R-10509	Resistor, Fixed Film (High Stability), General Specification For
MIL-C-10950	Capacitor, Fixed, Mica Dielectric, Button Style, General Specification For

MIL-C-11015	Capacitor, Fixed, Ceramic Dielectric (General Purpose), General Specification For
MIL-P-11268 (EL)	Parts, Materials and Processes Used in Electronic Equipment
MIL-C-11693	Capacitor, Feed Through, Radio Interference Reduction, AC and DC, (Hermetically Sealed in Metal Cases) Established and Nonestablished Reliability, General Specification For
MIL-R-11804	Resistor, Fixed, Film (Power Type), General Specification For
MIL-S-12285	Switch, Thermostatic
MIL-R-12934	Resistor, Variable, Wirewound, Precision, General Specification For
MIL-C-13777	Cable, Special Purpose, Electrical, Conductors, General Specification For
MIL-P-13949	Plastic Sheet, Laminated Metal Clad (for Printed Wiring) General Specification For
MIL-C-14409	Capacitor, Variable (Piston Type, Tubular Trimmer), General Specification For
MIL-C-15305	Coil, Fixed and Variable, Radio Frequency, General Specification For
MIL-S-15743	Switch, Rotary, Enclosed
MIL-W-16878	Wire, Electrical, Insulated, High Temperature, General Specification For
MIL-E-17555	Electronic and Electrical Equipment, Accessories and Repair Parts, Packaging and Packing Of
MIL-S-18396	Switches, Motor and Control, Naval Shipboard
MIL-R-18546	Resistor, Fixed, Wirewound (Power Type, Chassis Mounted) General Specification For
MIL-W-19150	Wire, Insulated, Hard Drawn Copper
MIL-S-19500	Semiconductor Devices, General Specification For
MIL-R-19523	Relay, Control, Naval Shipboard
MIL-C-19547	Cable, Electrical, Special Purposes, Shore Use
MIL-R-19648	Relay, Time Delay, Thermal, General Specification For

MIL-C-19978	Capacitor, Fixed Plastic (or Paper-Plastic) Dielectric (Hermetically Sealed in Metal, Ceramic or Glass Cases), Established and Nonestablished Reliability, General Specification For
MIL-T-21038	Transformer, Pulse, Low Power, General Specification For
MIL-C-21097	Connector, Electrical, Printed Wiring Board, General Purpose, General Specification For
MIL-S-21604	Switch, Rotary, Multipole and Selector Type
MIL-C-21609	Cable, Electrical, Shielded, 600 Volt (For Nonflexing Service)
MIL-R-22097	Resistor, Variable, Nonwirewound (Adjustment Types), General Specification For
MIL-R-22684	Resistor, Fixed, Film, Insulated, General Specification For
MIL-W-22759	Wire, Electric, Fluoropolymer Insulated, Copper or Copper Alloy
MIL-C-22931	Cable, Radio Frequency, Semirigid, Coaxial, Semi-air-dielectric, General Specification For
MIL-C-22992	Connector, Plugs & Receptacles, Electrical Waterproof Quick Disconnect, Heavy Duty Type General Specification for
MIL-C-23183	Capacitor, Fixed or Variable, Vacuum Dielectric, General Specification For
MIL-C-23269	Capacitors, Fixed, Glass Dielectric, Established Reliability, General Specification For
MIL-R-23285	Resistor, Variable, Nonwirewound, General Specification For
MIL-C-23437	Cable, Electrical, Shielded Pairs
MIL-T-23648	Thermistor, (Thermally Sensitive Resistor), Insulated, General Specification For
MIL-C-23806	Cable, Radio Frequency, Coaxial, Semirigid, Foam Dielectric, General Specification For
MIL-C-24308	Connector, Electrical, Rectangular, Miniature Polarized Shell, Rack and Panel, General Specification For

MIL-W-25038	Wire, Electrical, High Temperature and Fire Resistant, General Specification for
MIL-C-25516	Connector, Electrical, Miniature, Coaxial, Environment Resistant Type, General Specification For
MIL-C-26482	Connector, Electrical (Circular, Miniature, Quick Disconnect, Environment Resisting) Receptacles and Plugs, General Specification For
MIL-C-27072	Cable, Special Purpose, Electrical, Multiconductor
MIL-R-27208	Resistor, Variable, Wire wound (Adjustment Type) General Specification For
MIL-C-27500	Cable, Electrical, Shielded and Unshielded, Aerospace
MIL-S-28788	Switch, Air and Liquid Flow, Sensing General Specification For
MIL-C-28731	Connectors, Electrical, Rectangular, Removable Contact, Formed Blade, Fork Type (For Rack and Panel and other applications) General Specification for
MIL-C-28748	Connector, Electrical, Rectangular, Rack and Panel, Solder Type and Crimp Type Contacts, General Specification For
MIL-R-28750	Relay, Solid State, General Specification for
MIL-M-28787	Module, Standard Electronic, General Specification For
MIL-P-28809	Printed Wiring Assemblies
MIL-M-38510	Microcircuits, General Specification For
MIL-C-38999	Connector, Electrical, Circular, Miniature, High Density, Quick Disconnect, (Bayonet, Threaded, and Breech Coupling) Environment Resistant, Removable Crimp and Hermetic Solder Contacts, General Specification For
MIL-C-39001	Capacitor, Fixed, Mica Dielectric, Established Reliability, General Specification For
MIL-R-39002	Resistor, Variable, Wirewound, Semi Precision, General Specification For

MIL-C-39003	Capacitor, Fixed, Electrolytic, (Solid Electrolyte), Tantalum, Established Reliability, General Specification For
MIL-R-39005	Resistor, Fixed, Wirewound, (Accurate) Established Reliability, General Specification For
MIL-C-39006	Capacitor, Fixed, Electrolytic (Nonsolid Electrolyte) Tantalum, Established Reliability, General Specification For
MIL-R-39007	Resistor, Fixed, Wirewound, (Power Type) Established Reliability, General Specification For
MIL-R-39008	Resistor, Fixed, Composition, (Insulated) Established Reliability, General Specification For
MIL-R-39009	Resistor, Fixed, Wirewound, (Power Type, Chassis Mounted) Established Reliability, General Specification For
MIL-C-39010	Coil, Fixed, Radio Frequency, Molded, Established Reliability, General Specification For
MIL-C-39012	Connector, Coaxial, Radio Frequency, General Specification For
MIL-C-39014	Capacitor, Fixed, Ceramic Dielectric (General Purpose), Established Reliability, General Specification For
MIL-R-39015	Resistor, Variable, Wirewound, (Lead Screw Actuated) Established Reliability, General Specification For
MIL-R-39016	Relay, Electromagnetic, Established Reliability, General Specification For
MIL-R-39017	Resistor, Fixed, Film (Insulated), Established Reliability, General Specification For
MIL-C-39018	Capacitor, Fixed, Electrolytic, (Aluminum Oxide) Established Reliability and Nonestablished Reliability, General Specification For
MIL-C-39022	Capacitor, Fixed, Metallized Paper, Paper Plastic Film, or Plastic Film Dielectric, Direct and Alternating Current, (Hermetically Sealed in Metal Cases) Established Reliability, General Specification For
MIL-R-39023	Resistor, Variable, Nonwirewound, Precision, General Specification For

MIL-R-39035	Resistor, Variable, Nonwirewound, (Adjustment Type) Established Reliability, General Specification For
MIL-I-46058	Insulating Compound, Electrical (For Coating Printed Circuit Assemblies)
MIL-P-50884	Printed Wiring, Flexible, General Specification For
MIL-C-55021	Cable, Twisted Pairs and Triples, Internal Hookups, General Specification For
MIL-P-55110	Printed Wiring Boards
MIL-R-55182	Resistor, Fixed, Film, Established Reliability, General Specification For
MIL-C-55302	Connector, Printed Circuit, Subassembly and Accessories
MIL-C-55365	Capacitor, Chip, Tantalum Dielectric, Established Reliability
MIL-R-55432	Resistor, Film, Chip, Established Reliability
MIL-C-55514	Capacitor, Fixed, Plastic (or Metallized Plastic) Dielectric, Direct Current, In Non-Metal Cases, General Specification For
MIL-T-55631	Transformer, Intermediate Frequency, Radio Frequency, and Discriminator, General Specification For
MIL-W-81044	Wire, Electric, Crosslinked Polyalkene, Cross linked Alkane-imide Polymer, or Polyarylene Insulated, Copper or Copper Alloy
MIL-W-81381	Wire, Electric, Polyimide Insulated, Copper and Copper Alloy
MIL-C-81511	Connector, Electrical, Circular, High Density, Quick Disconnect, Environment Resisting, and Accessories, General Specification For
MIL-P-81728	Plating. Tin Lead (Electrodeposited)
MIL-R-83401	Resistor Networks, Fixed, Film, General Specification For
MIL-C-83421	Capacitor, Fixed, Supermetallized Plastic Film Dielectric (DC, AC or DC and AC), Hermetically Sealed in Metal Cases, Established Reliability, General Specification For

MIL-T-83720	Transformers and Inductors, Nonexplosive, General Specification For
MIL-T-83721	Transformers, Variable, Power, 400HZ General Specification For
MIL-C-83723	Connector, Electrical (Circular, Environment Resisting), Receptacles and Plugs, General Specification For
MIL-R-83725	Relay, Vacuum, General Specification For
MIL-R-83726	Relay, Time Delay, Electric and Electronic, General Specification For
MIL-C-83733	Connector, Electrical, Miniature, Rectangular Type, Rack to Panel, Environment Resisting, 200 Degrees C Total Continuous Operating Temperature, General Specification For
DOD-C-85045	Cables, Fiber Optics, General Specification For

STANDARDS

Military

MIL-STD-105	Sampling Procedure and Tables for Inspection by Attributes
MIL-STD-198	Capacitors, Selection and Use Of
MIL-STD-199	Resistors, Selection and Use Of
MIL-STD-200	Electron Tubes, Selection and Use Of
MIL-STD-202	Test Methods for Electronic and Electrical Component Parts
MIL-STD-210	Climatic Extremes for Military Equipment
MIL-STD-454	Standard General Requirements for Electronic Equipment
MIL-STD-690	Failure Rate Sampling Plan and Procedures
MIL-STD-701	List of Standard Semiconductor Devices
MIL-STD-750	Test Methods for Semiconductor Devices
MIL-STD-785	Reliability Program for System and Equipment, Development and Production

MIL-STD-790	Reliability Assurance Program for Electronic Parts Specifications
MIL-STD-883	Test Methods and Procedures for Microelectronics
MIL-STD-965	Parts Control Program
MIL-STD-1131	Storage Shelf Life and Reforming Procedures for Aluminum Electrolyte Fixed Capacitors
MIL-STD-1132	Switch and Associated Hardware, Selection and Use Of
MIL-STD-1286	Transformers, Inductors and Coils, Selection and Use Of
MIL-STD-1346	Relays, Selection and Use Of
MIL-STD-1353	Electrical Connectors, Plug In Sockets and Associated Hardware, Selection and Use of
MIL-STD-1378	Requirements for Employing Standard Electronic Modules
MIL-STD-1389	Design Requirements for Standard Electronic Modules
MIL-STD-1562	List of Standard Microcircuits
MIL-STD-1635	Reliability Growth Testing
MIL-STD-1655	Module Description for the SEM Program
MIL-STD-1678	Fiber Optics Test Methods and Instrumentation
DOD-STD-1686	Electrostatic Discharge Control Program for Protection of Electrical and Electronic Parts, Assemblies and Equipment (Excluding Electrically Initiated Explosive Devices) METRIC

HANDBOOKS

MIL-HDBK-175	Microelectronic Device Data Handbook
MIL-HDBK-217	Reliability Prediction of Electronic Equipment
MIL-HDBK-246	Program Managers Guide for the Standard Electronic Modules Program
MIL-HDBK-251	Reliability/Design Thermal Applications

DOD-HDBK-263	Electrostatic Discharge Handbook for Protection of Electrical and Electronic Parts, Assemblies and Equipment (Excluding Electrically Initiated Explosive Devices) METRIC
TP-526	SEM Program Microprocessor Application Handbook
TP-528	SEM Program Memory Application Handbook
TP-529	SEM Thermal Application Handbook
TP-531	In Process Module Descriptions Handbook

(Copies of specifications, standards, drawings and publications required by contractors in connection with specific procurement functions should be obtained from the procuring activity or as directed by the contracting officer.)

3.0 DEFINITIONS

ACCESSIBILITY

A measure of the relative ease of admission to the various areas of an item.

AVAILABILITY

A measure of the degree to which an item is in the operable and committable state at the start of the mission, when the mission is called for at an unknown (random) point in time.

BURN-IN

The operation of an item to stabilize its characteristics.

CAPABILITY

A measure of the ability of an item to achieve mission objectives given the conditions during the mission.

CHECKOUT

Tests or observations of an item to determine its conditions or status.

DEBUGGING

A process to detect and remedy inadequacies, preferably prior to operational use.

DEMONSTRATED

That which has been proven by the use of concrete evidence gathered under specified conditions.

DEPENDABILITY

A measure of the item operating condition at one or more points during the mission, including the effects of Reliability, Maintainability and Survivability, given the item condition(s) at the start of the mission. It may be stated as the probability that an item will (a) enter or occupy any one of its required operational modes during a specified mission, (b) perform the functions associated with those operational modes.

DERATING

(a) Using an item in such a way that applied stresses are below rated values, or

(b) The lowering of the rating of an item in one stress field to allow an increase in rating in another stress field.

FAILURE

The inability of an item to perform within previously specified limits.

FAILURE ANALYSIS

The logical, systematic examination of an item or its diagram(s) to identify and analyze the probability, causes, and consequences of potential and real failures.

FAILURE, DEPENDENT

One which is caused by the failure of an associated item(s). Not independent.

FAILURE, INDEPENDENT

One which occurs without being related to the failure of associated items. Not dependent.

FAILURE, RANDOM

Any failure whose occurrence is unpredictable in an absolute sense but which is predictable only in a probabilistic or statistical sense.

FAILURE RATE

The total number of failures within a population, divided by the total number of life units expended by that population, during a particular measurement interval under stated conditions.

HUMAN ENGINEERING

The area of human factors which applies scientific knowledge to the design of items to achieve effective man-machine integration and utilization.

HUMAN FACTORS

A body of scientific facts about human characteristics. The term covers all biomedical and psychosocial considerations: it includes, but is not limited to, principles and applications in the areas of human engineering, personnel selection, training, life support, job performance aids, and human performance evaluation.

INFANT MORTALITY

The initial phase of the lifetime of a population of a particular component when failures occur as a result of manufacturing errors, etc. Infant mortalities are screened out by burn-in.

INHERENT RELIABILITY

A measure of reliability that includes only the effect of an item design and its application and assumes an ideal operation and support environment.

LIFE SUPPORT

The area of human factors which applies scientific knowledge to items which require special attention or provisions for health promotion, biomedical aspects of safety, protection, sustenance, escape, survival, and recovery of personnel.

MAINTAINABILITY

A characteristic of design and installation which is expressed as the probability that an item will be retained in or restored to a specified condition within a given period of time, when the maintenance is performed in accordance with prescribed procedures and resources.

MAINTENANCE

All actions necessary for retaining an item in or restoring it to a specified condition.

MAINTENANCE, CORRECTIVE

The actions performed, as a result of failure, to restore an item to a specified condition.

MAINTENANCE, PREVENTIVE

The actions performed in an attempt to retain an item in a specified condition by providing systematic inspection, detection and prevention of incipient failure.

MEAN-TIME-BETWEEN-FAILURE (MTBF)

A basic measure of reliability for repairable items. The mean number of life units (e.g., hours x 10^6) during which the component performs to specification, during a particular measurement interval under stated conditions.

MEAN-TIME-BETWEEN-MAINTENANCE

The mean of the distribution of the time intervals between maintenance actions (either preventive, corrective, or both).

MEAN-TIME-TO-FAILURE (MTTF)

A basic measure of reliability for nonrepairable items and hence more application to component reliability. The total number of life units divided by the total number of failures, for a population of components operating during a particular measurement interval under stated conditions.

MEAN-TIME-TO-REPAIR (MTTR)

The total corrective maintenance time divided by the total number of corrective maintenance actions during a given period of time.

MISSION

The objective or task, together with the purpose, which clearly indicates the action to be taken.

OPERABLE

The state of being able to perform the intended function.

OPERATIONAL

Of, or pertaining to, the state of actual usage.

PREDICTED

That which is expected at some future date, postulated on analysis of past experience.

RATING

The value of an item parameter which shall be attained under specified conditions.

REDUNDANCY

The existence of more than one means for accomplishing a given function. Each means of accomplishing the function need not necessarily be identical.

RELIABILITY

The probability that an item shall perform its intended function for a specified interval under stated conditions.

SAFETY

The conservation of human life and its effectiveness, and the prevention of damage to items, consistent with mission requirements.

STORAGE LIFE (SHELF LIFE)

The length of time an item can be stored under specified conditions and still meet specified requirements.

TIME, DOWN (DOWNTIME)

That element of time during which the item is not in condition to perform its intended function

USEFUL LIFE

The second phase of the lifetime of a population of a particular component when only random failures occur.

WEAROUT

The third and final phase of the lifetime of a population of components when failures occur due to wearout.

4.0 RELIABILITY THEORY

4.1 INTRODUCTION

This chapter constitutes a gathering together of some of the main points of reliability theory applicable to components, and as such will be a useful reference for the design engineer. Rigorous mathematical explanation is not given but the interested reader is referred to relevant texts as appropriate. Additional information on reliability theory is given in Volume 1 of this Handbook.

The material in this chapter should serve to provide explanations for some of the more common methods and terms which appear in data books, specifications and technical references.

It is interesting to note that the same concepts as those used in reliability theory are used by actuaries in calculating life insurance premiums and that human mortality provides a useful analogy for component reliability.

4.1.1 DEFINITIONS

A list of words and terms which are particularly applicable when considering component reliability is given below:

o Reliability: The probability that a component will perform its intended function for a specified time interval under stated conditions.

o Failure Rate: The total number of failures within a population, divided by the total number of life units expended by that population, during a particular measurement interval under stated conditions.

o Inherent Reliability: A measure of reliability that includes only the effects of an item design and its application, and assumes an ideal operation and support environment.

o Mean Time Between Failure (MTBF): A basic measure of reliability for repairable items. The mean number of life units (e.g. hours x 10^6) during which the component performs to specification, during a particular measurement interval under stated conditions.

o Mean Time to Failure (MTTF): A basic measure of reliability for non-repairable items and hence more applicable to component reliability. The total number of life units divided by the total number of failures, for a population of components operating during a particular measurement interval under stated conditions.

o Infant Mortality: The initial phase of the lifetime of a population of a particular component when failures occur as a result of manufacturing errors, etc. Infant mortalities are screened out by burn-in.

o Useful Life: The second phase of the lifetime of a population of a particular component when only random failures occur.

o Wearout: The third and final phase of the lifetime of a population of components when failures occur due to wearout.

A partial listing of appropriate definitions can be found in MIL-STD-721 (Definitions of Terms for Reliability and Maintainability).

4.2 PROBABILITY DISTRIBUTIONS

4.2.1 GENERAL

If we are interested in some variable which is defined by some probabilistic law, we call it a random variable. Such variables may be discrete or continuous. The properties of a random variable are specified by the set of possible values it may take together with their associated probabilities of occurrence. The graph of probability against the random variable is called a probability distribution, and the mathematical expression for that distribution is called the probability density function (p.d.f). Since the relative frequency of occurrence of each value of the random variable is a measure of its probability, we usually define the vertical axis as frequency and the horizontal axis defines the random variable.

The probability density function (p.d.f) of resistance values for a nominal 4.7 ohm resistor might look like this:

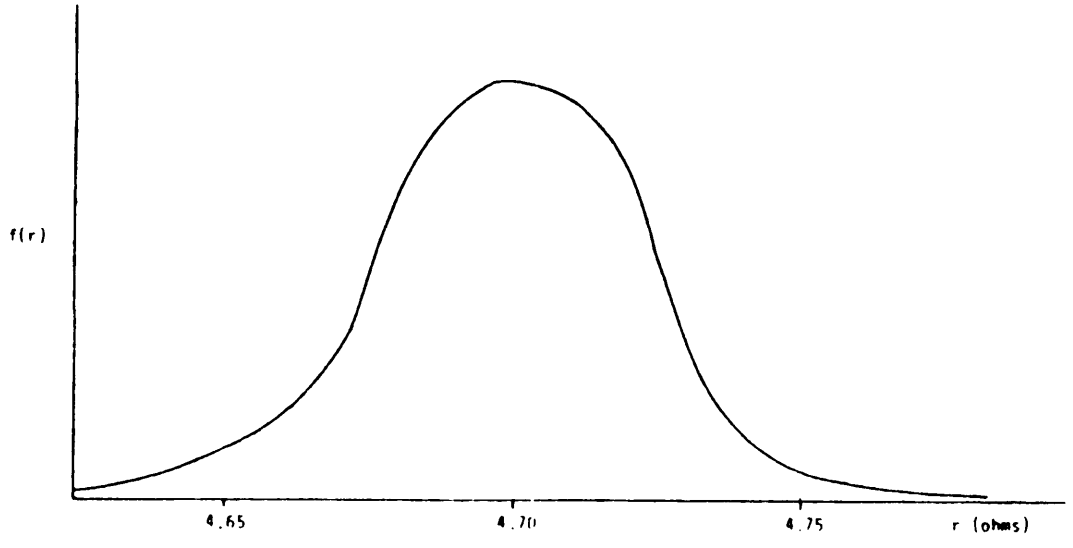


FIGURE 4.2.1-1: THE NORMAL DISTRIBUTION

f(r) is used to denote the relative frequency of the random variable which in this case is r, the resistance (in ohms).

The p.d.f's in this section all have time (or part hours) as the random variable. Some general terms used are illustrated on the (hypothetical) distribution given by f(x), as follows:

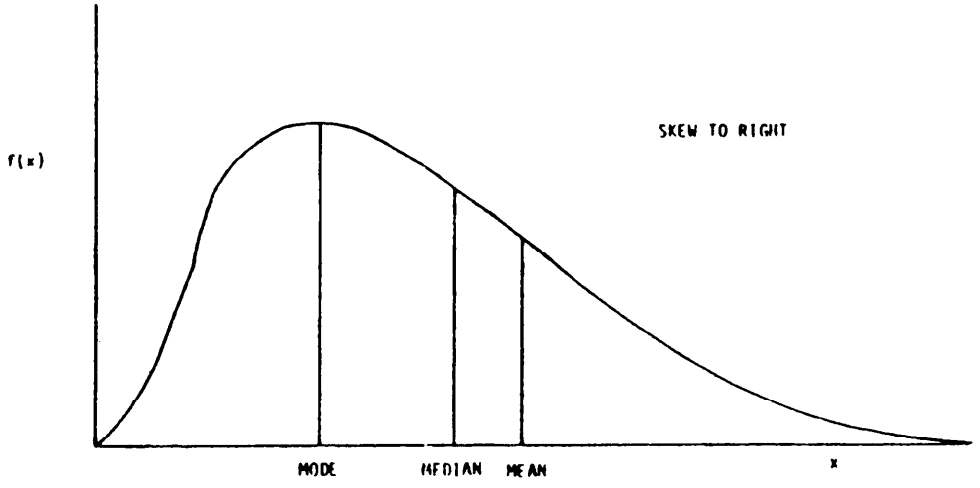


FIGURE 4.2.1-2: A TYPICAL PROBABILITY DENSITY FUNCTION

The median is the middle ordered value.
The mean is the arithmetic average of x.
The mode is the most common value of x.
The variance measures the spread of a set of values and is given by:

$$\sum_{i-1}^{n} (x_i-\bar{x})^2/(n-1)$$

where

x_i are observations
$\bar{x}$ is the sample mean
n is the sample size

The standard deviation is the square root of the variance. In mechanics, mean is analogous to center of gravity, variance to moment of inertia.
The skew of a distribution is a measure of its non-symmetry so the above distribution is skew to the right.
The kurtosis is a measure of the length of the tails of a distribution.

Cumulative distribution functions are also used. These are simply functions giving cumulative probabilities at the same value of the random variable. They are derived by integrating (or summing) the p.d.f. over some range of the random variable. Thus, they give the probability that the random variable is in some specified range. Statistical tables give values of the cumulative distribution over specified ranges, typically for the upper tail.

4.2.2 DISTRIBUTIONS USED IN RELIABILITY

Standard probability distributions are applicable in many reliability models. They may be used to define the probability of a component failing in a certain time interval. The most appropriate model for a particular component may be decided either empirically or theoretically or by a combination of both approaches.

A distribution may be chosen empirically by fitting to data. Simple methods for doing this have been developed, which affords a graphical means of fitting distributions using probability paper. The method is described in some detail for the Weibull distribution which is particularly useful in reliability work because of its flexibility.

Goodness of fit tests such as chi-square or Kolmogorov - Smirnov may be used to decide whether a particular distribution fits a particular set of data well enough. These tests give an unbiased, objective assessment of the goodness of fit. Full descriptions and examples of their use are given in any introductory statistical text (see References).

A distribution may be chosen theoretically by considering the underlying failure mechanism, and the physics of that mechanism. Such considerations are explained under the detailed discussion for each of the probability distributions given in this section.

Before proceeding to the individual distributions it is necessary to define the concept of a hazard rate. The hazard rate function h(t) is the instantaneous failure rate and is defined mathematically by:

$$h(t) = \frac{f(t)}{1-F(t)}$$

where f(t) is the probability density function associated with the lifetime of the component.

F(t) is the cumulative density function for f(t). Probabilistically, the hazard rate represents the probability that a component will fail in the time interval $(t + \Delta t)$ given that it has survived to time t.

Perhaps the simplest explanation of hazard rate and its relation to failure rate is given by analogy. Consider a typical family making a journey of 220 miles. If they complete the trip in four hours, their average rate was 55 m.p.h. although they drove faster at some times and slower at others. Their rate at any given instant could have been determined by consulting the speedometer or driving through a radar trap. The 55 m.p.h. is analogous to the failure rate and the speed at any point is analogous to the hazard rate.

Life distributions often follow the ubiquitous "bathtub" curve which describes the higher hazard rates at burn-in and wearout, with the constant hazard rate in between (useful life). The initial part of the curve exhibits a decreasing hazard rate (DHR) and is usually termed "infant mortality". The final part of the curve exhibits an increasing hazard rate (IHR) and is usually termed "wearout".

Some particular probability distributions which are often used in reliability modelling and analysis are now described. Their use in systems applications is described in Volume I of this Handbook.

4.2.2.1 EXPONENTIAL DISTRIBUTION

If failures are random in time, they obey a particular law called the Poisson process. The time to failure (TTF) is then found to have an exponential distribution given by

$$f(t) = \lambda e^{-\lambda t}$$

where λ is the failure rate. The exponential distribution is shown below:

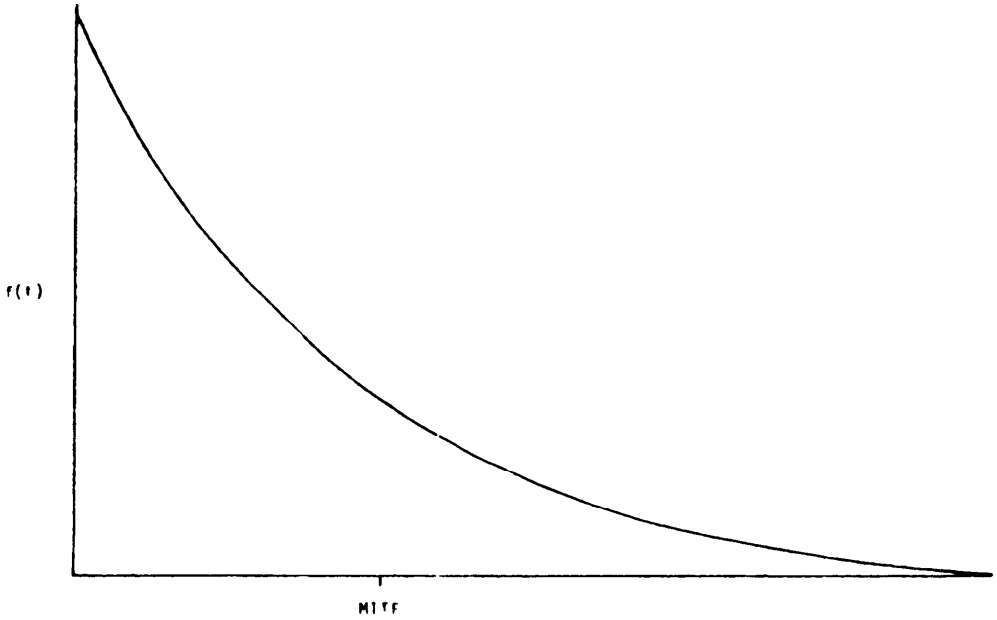


FIGURE 4.2.2.1-1: THE EXPONENTIAL DISTRIBUTION

Note the simplicity of the model which is completely defined on a single parameter λ. This makes estimation from data, and mathematical manipulation in general, extremely easy. Consequently the exponential distribution of TTF has become very popular but its validity should be checked in each case. The reliability function from the definition given in Section 4.1.1, is the probability that the component is working to specification at time t, (which is 1 - Prob. [Failure in time t]). So:

$$R(t) = 1 - \int_0^t \lambda e^{-\lambda u}\, du$$

where u is a substitute time variable for integration and where R(t) is the reliability function.

$$R(t) = 1 - [\, -e^{-\lambda u} \,]_0^t$$

$$= 1 - (1 - e^{-\lambda t})$$

$$\therefore R(t) = e^{-\lambda t}$$

The hazard rate is given by $h(t) = \frac{f(t)}{R(t)}$

$$= \frac{\lambda e^{-\lambda t}}{e^{-\lambda t}} = \lambda$$

Hence the hazard rate for the exponential distribution is found to be constant and equal to λ. This property is exploited in MIL-HDBK-217, which gives a comprehensive tabulation of failure rates for various components, on the constant failure rate assumption. The underlying mechanism of the exponential TTF distribution, is randomness. If it is felt that a component fails purely at random and is not subject to burn-in or wearout (at least for a specified portion of its lifetime) then the exponential model is probably justified.

The exponential distribution is a special case of the gamma distribution which is described later.

4.2.2.2 LOG-NORMAL DISTRIBUTION

If the logarithm of the TTF is found to be distributed normally, then the TTF distribution is said to be log-normal and is given by

$$f(t) = \frac{1}{\sqrt{2\pi}\,\sigma t} \exp\left\{-\left(\frac{\ln(t)-\mu)^2}{2\sigma^2}\right)\right\}$$

where μ is the mean and σ the standard deviation of the associated normal distribution (i.e., of log (t)). In practical terms, μ defines the location of the distribution and σ the shape. Some examples are shown below. Note that a third parameter may be incorporated in the log-normal distribution. The third parameter represents the minimum life.

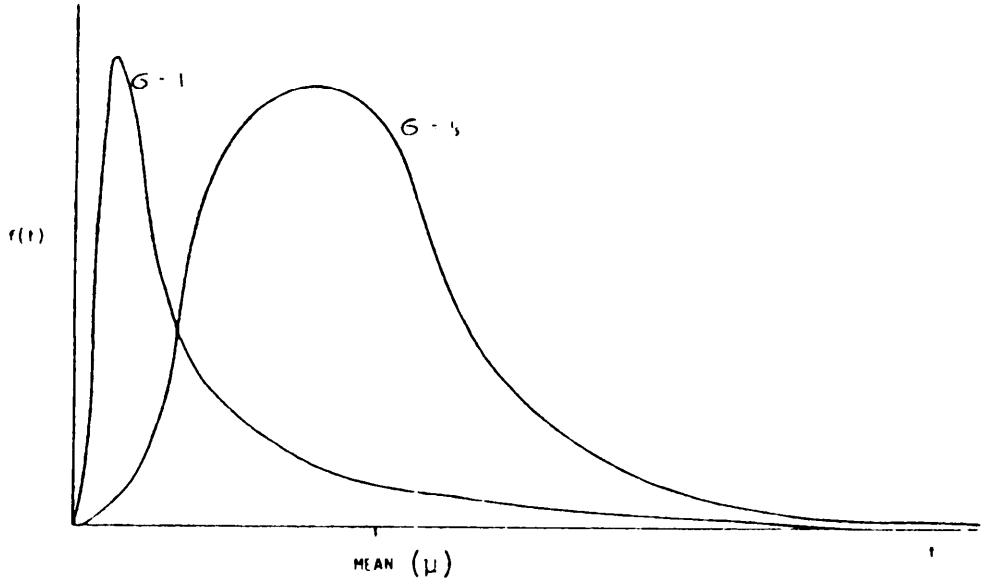


FIGURE 4.2.2.2-1: THE LOG-NORMAL DISTRIBUTION

The reliability function R(t) is quite complex and so its mathematical description is not given here.

The hazard rate is not constant in the log-normal distribution. The hazard rate function may be divided into two phases, the first increasing with time, the second decreasing.

The physical significance of the lognormal distribution is explained by components which operate for some time and then fail due to some wearout mechanism. For example, light bulbs eventually suffer filament deterioration and empirically follow a lognormal distribution. Semiconductors have been found (although not by any means in all cases) to follow lognormal distributions.

4.2.2.3 WEIBULL DISTRIBUTION

The Weibull distribution is particularly useful since it is of a general form covering many specific distributions in a three parameter model.

The general form will be found to vary amongst texts but the most common is given by:

$$F(t) = \frac{\beta}{\alpha}\frac{(t-\gamma)^{\beta-1}}{\alpha}\exp\left[-\frac{(t-\gamma)^{\beta}}{\alpha}\right]$$

where α is a scale parameter (characteristic life)
β is a shape parameter
γ is the minimum life

In practice, γ is often taken as, or found to be, zero, and the function becomes simpler.

According to the value of β, the Weibull distribution takes on the form of other distributions as follows:

Beta	Distribution Type	Hazard Rate
$\beta < 1$	Gamma	Decreasing
$\beta = 1$	Exponential	Constant
$\beta = 2$	Rayleigh	Increasing/Decreasing

In addition, the Weibull is found to approximate other distributions although mathematically, not exactly. These are normal ($\beta \simeq 3.44$) and log-normal ($\beta \simeq 2$).

Extreme value distributions are also defined by the Weibull, using a logarithmic transformation on the data.

A useful tool in identifying particular distributions is the Weibull probability plot which is shown in Figure 4.2.2.3-1. This is a type of graph paper whose axes are defined on transformed scales such that the cumulative Weibull distribution function appears as a straight line. Thus, any set of data may be plotted on Weibull probability paper, and if a straight line results the values of α, β, γ and the mean life may be read directly from the paper. In practice the process is not quite so clean as data rarely fall exactly on a straight line. Statistical

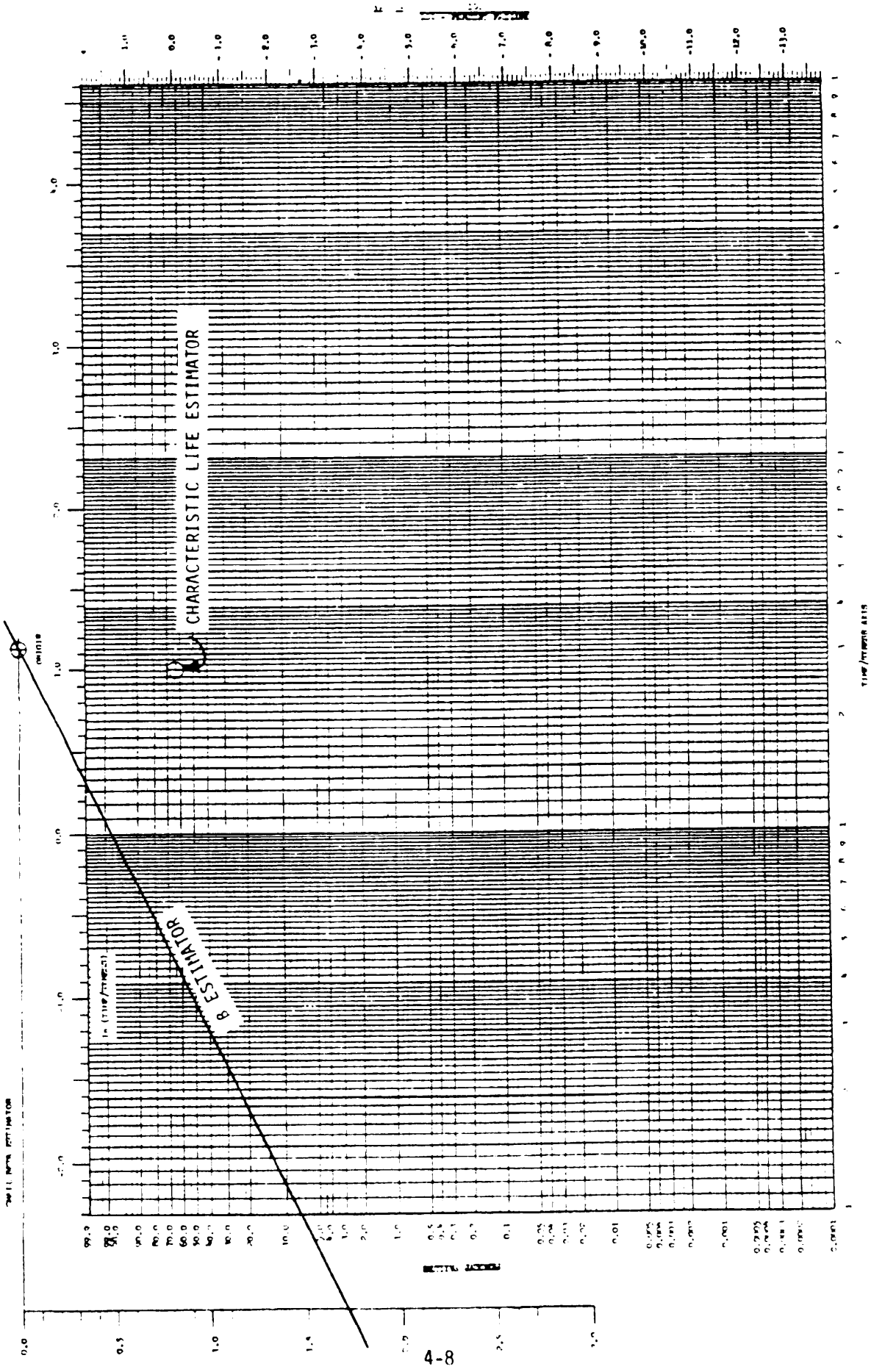


FIGURE 4.2.2.3-1: WEIBULL PROBABILITY PAPER

tests of linearity are advisable as false conclusions are easily drawn otherwise. Weibull probability paper is particularly useful as an exploratory technique to help in understanding data. Its use is defined as follows. (Here, time to failure is used as the random variable although any variable may be selected).

(a) Order the TTF data smallest to largest and assign a rank to each observation. So if there are n observations, the ranks will run from 1 to n. We will call i the rank of the i^{th} observation. If any observations are found to be equal, then the median rank is used for each of those "tied" observations.

(b) The observed cumulative distribution is then evaluated by calculating the percentiles for each observation. There are a number of ways to do this, the simplest being:

$$P_i = \frac{i}{n} \times 100$$

where P_i is the cumulative percent of failures at the i^{th} observation.

Unfortunately, this method is very biased. $100\ i/(n + 1)$ is better but is still unduly pessimistic. A simple unbiased method is given by Bernard's formula:

$$P_i = \frac{i - 0.3}{n + 0.4}$$

(c) Plot the values of P_i against the TTF on Weibull probability paper.

(d) If a reasonably straight line results, put in the line of best fit by eye. (Least square methods may be used if necessary).

(e) Read off the value of β on the scale provided. The methods for doing this vary depending on whose paper is used. Most construct either a parallel or perpendicular on the fitted line, through some origin provided. Each method will be self-explained by the paper.

The characteristic life (α) may be estimated from the value of TTF corresponding to P = 63.2%, as determined by the fitted line, i.e., construct a horizontal through the 63.2 percentile and drop a perpendicular onto the TTF axis, from the point where the horizontal intersects the fitted line. Most Weibull paper includes a clear indication of the 63.2% line.

Thus the characteristic life of a component is the time at which 63.2% of the population have failed. (It is analogous to the characteristic time of a capacitor).

The mean life, or mean time to failure (MTTF) is sometimes accommodated on Weibull paper. It may be read from a percentile (as for α) but the percentile varies according to the value of β.

An approximate list of percentiles which may be used to evaluate the MTTF is given by the following table:

TABLE 4.2.2.3-1: PERCENTILE USED TO ESTIMATE MEAN LIFE

β	Percentile
0.5	75 %
1.0	64 %
1.5	57.5%
2.0	54.5%
2.5	52.5%
3.0	51 %
3.44	50 %

A fuller description of the use of Weibull probability paper, with further techniques such as confidence interval estimation, may be found in Refs. 2 and 3.

An example of the use of Weibull paper is now given. Eighteen observations of TTF were collected and are ordered in the following table. The percentiles P_i, are estimated using Bernard's formula.

TABLE 4.2.2.3-2: TIME-TO-FAILURE, RANKS AND PERCENTILES

Time-to-Failure ($\times 10^4$ hours)	Rank (i)	P_i(%)
0.02	1	3.8
0.45	2	9.2
0.52	3	14.7
0.60	4	20.1
0.99	5	25.5
1.35	6	31.0
1.78	7	36.4
1.83	8	41.8
2.16	9	47.3
2.22	10	52.7
2.34	11	58.2
2.94	12	63.6
3.43	13	69.0
4.82	14	74.5
5.32	15½	82.6
5.32	15½	82.6
6.44	17	90.8
7.8	18	96.2

The data is then plotted on Weibull probability paper as shown in Figure 4.2.2.3-2.

The line is fitted as shown and found to have a β of about 1.16 as shown by the (dotted) parallel line. A value of 1.16 indicates that the data are close to exponential.

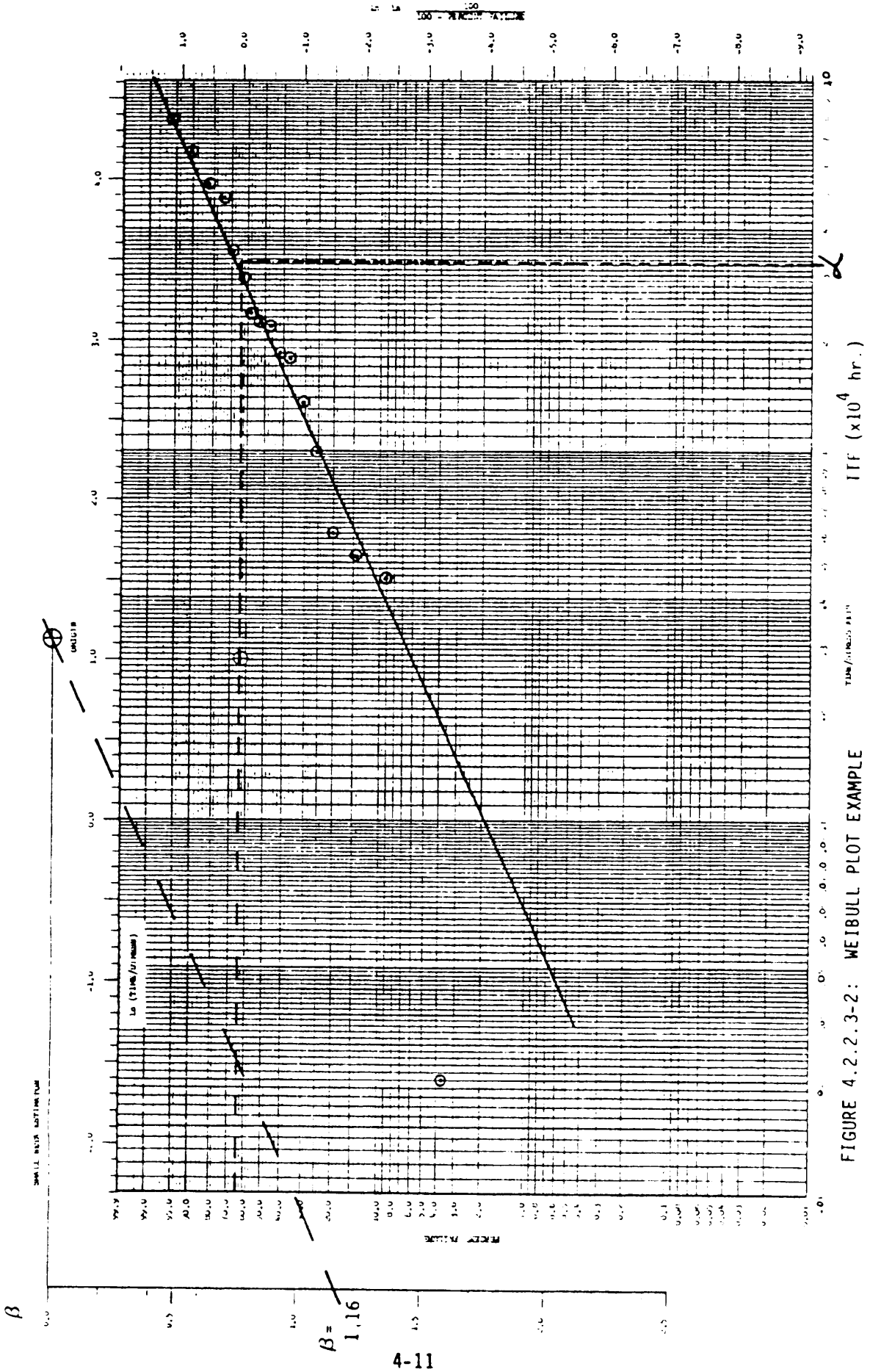


FIGURE 4.2.2.3-2: WEIBULL PLOT EXAMPLE

From the 63.2% estimated, α is found to be 3.25×10^4. Hence, the characteristic life is estimated at 32,500 hours.

The mean life (or MTTF) is estimated from (approximately) the 61% value of P and is hence found to be 31,000 hours. Note that if the data were truly exponential, the mean and characteristic life would be one and the same thing.

To sum up, although the various parameters may be estimated analytically, directly from the data, the Weibull probability plot provides a quick, easy method which may be particularly attractive to the non-specialist.

It is emphasized that conclusions based on Weibull plots should strictly be backed up by a statistical goodness-of-fit test such as Kolmogorov - Smirnov or chi-squared tests. Extended methods and many useful mathematical ideas are given in Ref. 3.

4.2.2.4 GAMMA DISTRIBUTION

This is a more complex p.d.f. to manipulate mathematically. The p.d.f. is given by

$$f(t) = \frac{\lambda}{\Gamma(k)} (\lambda t)^{k-1} e^{-\lambda t}$$

where λ is a scale parameter and k is a shape parameter. $\Gamma(k)$ is the gamma function. The gamma distribution covers a large number of different shapes of distribution depending on k. It is used in reliability, particularly for integer k, since it describes the time to k^{th} failure. Thus if a component fails as a result of some combination or sequence of k mechanisms, it may be found to follow a gamma distribution. Note that by setting k = 1 the time to first failure is considered and the exponential distribution results.

i.e., $f(t)_{k=1} = \frac{\lambda}{\Gamma} (\lambda t)^0 e^{-\lambda t} = \lambda e^{-\lambda t}$

$0! = 1$

$= \lambda e^{-\lambda t}$

In many cases it is easier to use the Weibull distribution which covers the gamma distribution. Examples of gamma distributions are given in Figure 4.2.2.4-1.

4.2.3 CONFIDENCE INTERVALS

Component manufacturers often indicate the reliability of their product by some kind of confidence interval on the life length or failure rate. It is important to understand the concept of a confidence interval as well as one or two common methods for constructing them.

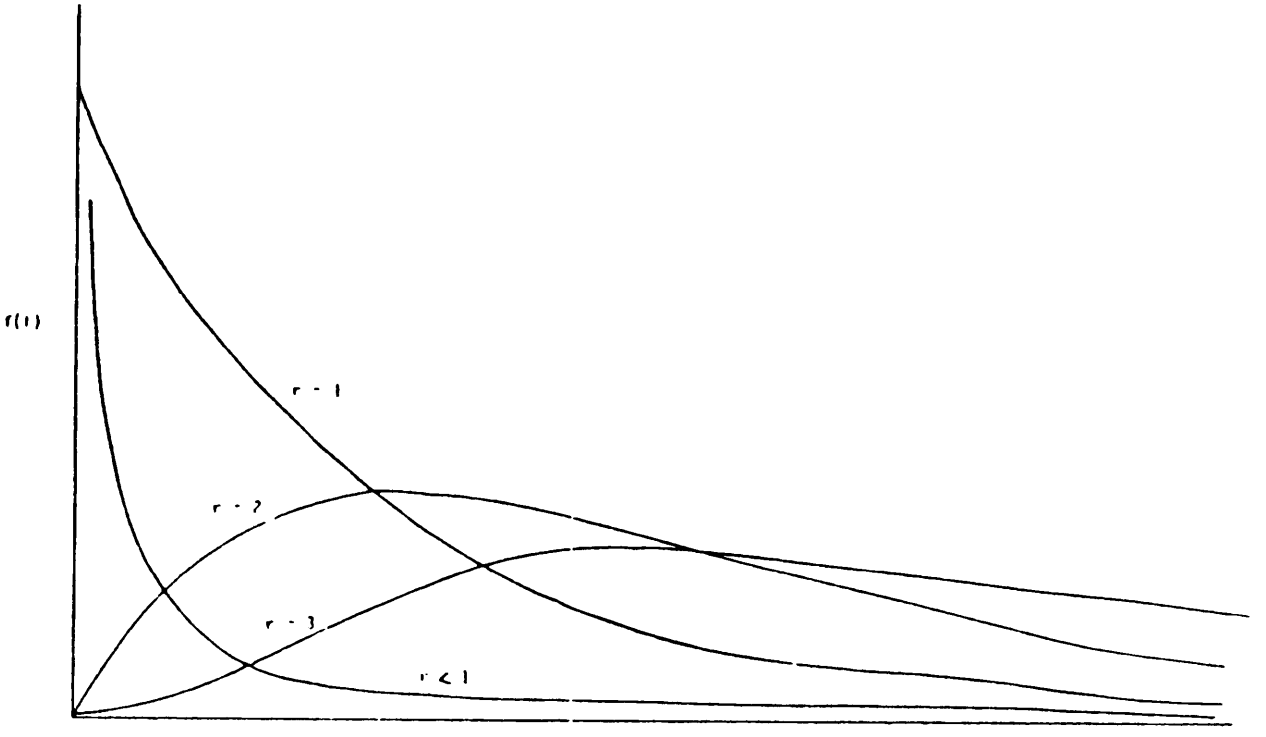


FIGURE 4.2.2.4-1: THE GAMMA DISTRIBUTION

A point estimate of some parameter such as failure rate or life is not meaningful without some measure of its possible error. Such a measure, which is often used, is called the confidence interval. Different samples of data yield different intervals; some of these intervals will contain the parameter and some will not. It is possible to define a $100(1 - \alpha)\%$ interval such that $100(1 - \alpha)\%$ of the intervals (of which ours is just one) will contain the parameter. Usually we compute two-sided central confidence intervals which lie symmetrically about the parameter with equal rises of the parameter being excluded on either side. It is also possible to compute one-sided intervals, which just give an upper or lower confidence limit, and non-central intervals which have unequal risks in each tail. In reliability, a one-sided interval might be used when a test has not yielded any failures over a certain time and yet an interval on the mean life is required. In such cases it is only possible to give a lower bound and hence a one-sided confidence interval is called for.

In many modern technology devices, the lifetime is of the order of 10^6 hours (or better) and hence the one sided confidence interval is quite prevalent in manufacturer's reliability reports.

The confidence level $1 - \alpha$ is expressed between 0 and 1 although in practice it typically varies between at least 0.5 (or 50%) and 0.999 (or 99.9%). Confidence intervals may be constructed on any parameter, e.g. mean, median, variance, etc.

4.2.3.1 CONFIDENCE LEVELS FOR THE MEAN OF AN EXPONENTIAL DISTRIBUTION

The mathematical justification for the construction of confidence intervals is not necessary to an understanding of this section. The interested reader is referred to the Reference texts.

The confidence interval on the mean of the exponential is given here because of its common usage in component reliability.

For a central, two sided confidence interval or mean life, the upper limit is given by

$$\frac{2t}{\chi^2_{2f,\ 1-\alpha/2}}$$

where t is the test time
f is the number of observed failures
$1 - \alpha$ is the required confidence
$\chi^2_{2f,\ 1-\alpha/2}$ is the value of the chi-squared distribution with 2f degrees of freedom, evaluated from tables of the chi-squared distribution which are included in any book of statistical tables.

The lower limit is given by

$$\frac{2t}{\chi^2_{2(f+1),\ \alpha/2}}$$

Confidence limits on the point estimate of the failure rate are given similarly by

$$\text{upper limit} = \frac{\chi^2_{2(f+1),\ \alpha/2}}{2t}$$

$$\text{lower limit} = \frac{\chi^2_{2f,\ 1-\alpha/2}}{2t}$$

with the symbols defined as before.

For example if 29 devices were tested for a total of 78×10^6 test hours, and they all failed, the point estimate failure rate would be 0.37×10^6 hours and a 60% central confidence interval would be defined on the interval 0.31×10^6 hours to 0.44×10^6 hours.

4.2.4 STATISTICAL QUALITY CONTROL

Introduction

When buying components in bulk there is a chance that some are defective. It is not often practical to test each one and so a sample is tested. Statistical methods are used to define how many of the components should be tested, and how many defectives may be allowed per batch. It is not realistic to specify that there be no defectives (in some cases this is

s and that human mortality provides a useful analogy for premiums

required and 100% inspection is called for) but we can specify some small number which reflects chance or random defectives.

In this book, we only consider inspection by attributes, that is, the measurement of defects as defined by some plan. Items are classified simply as defective or not.

Sampling Plans

Statistical sampling plans are concerned with defining the sample size upon which to base a decision as to whether the batch is good or bad, and the acceptable number of defectives per sample. Before defining a plan it is necessary to specify the producer's risk and the consumer's risk. These risks are defined as follows.

Producer's risk (α) is the probability that a good batch is rejected.
Consumer's risk (β) is the probability that a bad batch is accepted.

It is the consumer's risk which the design engineer is more directly concerned with since that sets his probability of having to waste time fault finding and repairing a board with a defective component.

Since the number of defectives per batch (which we will call θ) is a variable, it may take on values from zero upwards. Ideally we would define a sampling plan which measured θ exactly and this θ would exactly reflect the quality of the batch.

We could then define an acceptable θ, with which the producer could agree and everyone would be happy. The probability ($P(\theta)$) of accepting a batch of quality θ would be defined as in Figure 4.2.4-1 below. This graph is commonly referred to as the operating characteristic (OC) curve.

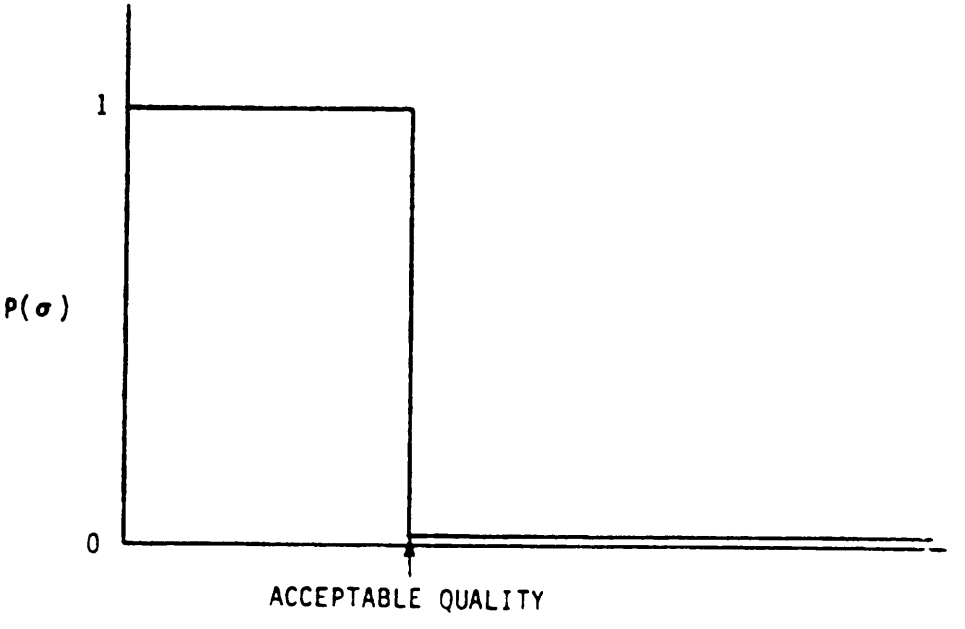


FIGURE 4.2.4-1: IDEAL OPERATING CHARACTERISTIC CURVE

each value of the random variable is a measure of its probability. We

The real world problem is not so straightforward since the number of defectives does not precisely measure the quality of the batch, due to sampling errors; and also it is not always possible to detect defects with perfect accuracy. Hence a compromise is required, with producer and consumer accepting certain risks. A more typical OC curve which illustrates these risks is given in Figure 4.2.4-2.

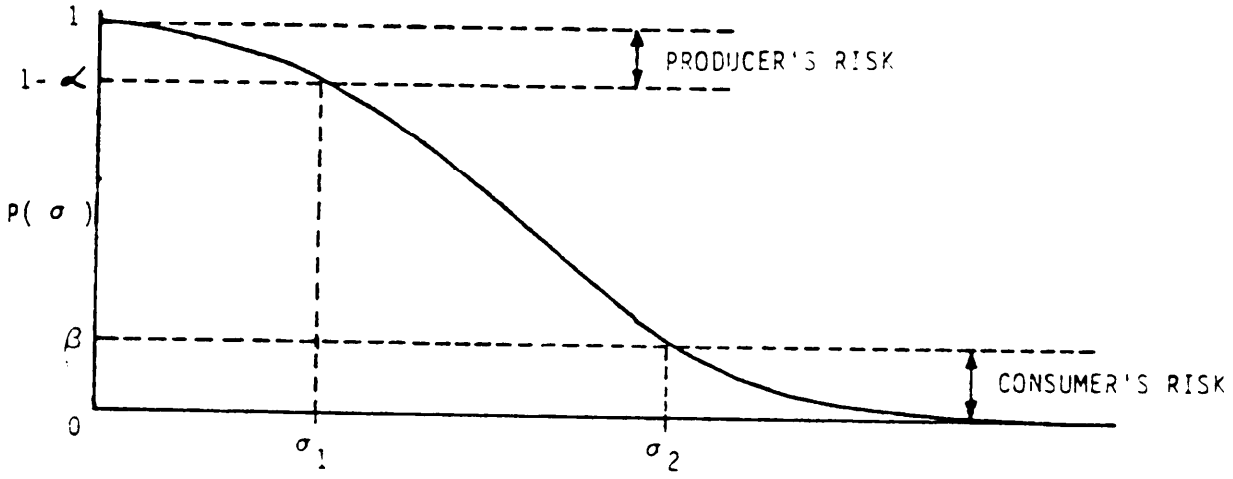


FIGURE 4.2.4-2: TYPICAL OPERATING CHARACTERISTIC CURVE

Many statistical plans have been developed to evaluate the risks α and β for a given sample size, or to choose a sample size given α and β. They are usually based on the Poisson (or exponential) distribution. At this point we introduce two terms which are commonly used in such plans.

o Acceptable Quality Level (AQL). This is often referred to when purchasing components and is the maximum percent defective (or the number of defects per hundred units which may or may not be the same thing) which can be considered satisfactory as a process average. The letters AQL stand simply for "acceptable quality level."

Various sampling plans are available, based on the AQL concept, a frequently used one being MIL-STD-105. In this scheme, sampling procedures and sample sizes, are given so that the consumer's probability of acceptance of a batch at AQL varies from 0.8 to over 0.99 depending on sample size. The OC curves are given in the standard so that risks may be assessed in each case.

MIL-STD-105 makes the distinction between percent defective, and defects per hundred units, since in the latter case, more than one defect per unit under inspection may be counted. Thus, MIL-STD-105 is designed to ensure that the greater majority of components of quality as good as, or better than the AQL, are accepted by the consumer. The scheme is ideally suited for continuous monitoring where batches are being inspected one after the other over a period of time and as such, normal, tightened and reduced inspection plans are given depending on how the process is faring (it will have its ups and downs). In Figure 4.2.4-2, θ_1 may be taken as the AQL.

o Lot Tolerance Percent Defective (LTPD). The lot tolerance percent defective is sometimes used and is defined as some chosen limiting value of percent defective in a lot. The LTPD is chosen such that components of quality worse than the LTPD are rejected with high probability. θ_2 may be taken, in Figure 4.2.4-2 as the LTPD. For very small defect rates (e.g., microprocessor chip devices) the LTPD scheme may be found to be more practical.

4.3 TEMPERATURE DEPENDENCE OF FAILURE RATE

Most failure mechanisms involve one or more physical or chemical processes which occurs at a rate which is highly dependent on temperature. Chemical reactions and diffusion mechanisms are common examples. Because of this strong temperature dependence, considerable effort has been expendend to predict temperature reaction rates by means of mathematical equations. The two most widely accepted models in reliability work are the Arrhenius and the Eyring models.

4.3.1 ARRHENIUS MODEL

The Arrhenius model is based on empirical data and predicts that the rate of a given reaction will be exponential with temperature:

Rate = $A \exp\left[\frac{-Ea}{KT}\right]$ when A is a normalizing constant, K is Boltzman's constant 8.63×10^{-5} eV/°K, T is the ambient temperature in degrees Kelvin, and E_a is a constant referred to as activation energy and is unique for each specific chemical reaction or failure mechanism.

4.3.2 EYRING MODEL

The Eyring equation, Rate = $A\,T \exp\left[\frac{-Ea}{KT}\right]$ is similar to the Arrhenius, except that the temperature T appears twice, once as a linear term and once in the exponent. While the Eyring model is esthetically appealing because it may be derived from first principles, in practice it has proven to be no more accurate than the Arrhenius in predicting reaction rates (and thus failure) in actual microcircuits. Consequently, the Arrhenius relationship is the one most often used in reliability since it is somewhat simpler and still does an adequate job of predicting reaction rates.

4.3.3 ACTIVATION ENERGY

Each and every chemical reaction, diffusion mechanism, etc, has a unique activation energy (Ea) associated with it. In an actual electronic component there are several such reactions proceeding simultaneously, each capable of eventually causing a failure. The cumulative effects of several different Arrhenius reactions will result in a microcircuit failure rate which exhibits some complex, non-Arrhenius, temperature-dependent failure rate.

Specific chemical reactions have activation energies; components do not. While technically incorrect, the activation energy concept has been applied to components often enough to warrant further discussion here. It has been found that for general classes of components, where the distribution of failures remains fairly constant among the various mechanisms/reactions, the cumulative effects of these various reactions is a failure rate whose temperature dependence is approximately exponential over a limited temperature range. As a result, people have a tendency to refer to an "activation energy" for a given type of component. Even though this is a case of erroneous terminology, its use does serve a purpose, since it tells one that the component is exhibiting a failure rate having a temperature dependence the same as would a component failing due to a single mechanism with the specified activation energy. There are many problems and limitations with such a statement and the misuse of the activation energy concept by applying it to other than specific reactions or mechanisms is not condoned.

A common misconception is that a higher activation energy indicates a higher failure rate: this is not necessarily the case. If one plots $\ell n \lambda$ versus $\frac{1}{KT}$ the result will be a straight line of slope -Ea. Consider Figure 4.3.3-1.

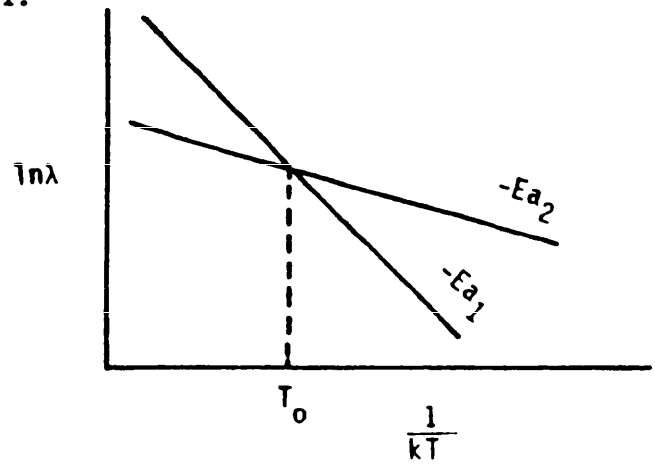


FIGURE 4.3.3-1: FAILURE RATE VS. TEMPERATURE

Note that $Ea_1 > Ea_2$ so that the temperature dependence of the first is greater than that of the second. It is important to note that for $T < T_0$ (or equivalently $\frac{1}{KT} > \frac{1}{KT_0}$), the failure rate to reaction 2 with activation energy Ea is greater than that for reaction 1, even though it has a lower activation energy.

REFERENCES

1. Hald, A., "Statistical Theory with Engineering Applications."

2. Siegel, S., "Non-parametric Statistics for the Behavioral Sciences," McGraw-Hill, 1956.

3. Mann, N.R., R.E. Schafer and N.D. Singpurwalla, "Methods for Statistical Analysis of Reliability and Life Data," Wiley, 1974.

4. Johnson, L.H., "The Statistical Treatment of Fatigue Experiments," Elsevier Publishing Co., 1964.

5. Kendall, M.G. and A. Stuart, "The Advanced Theory of Statistics," Vol. 2, Hafner, 1961.

5.0 COMPONENT RELIABILITY DESIGN CONSIDERATIONS

5.1 PART SELECTION AND CONTROL

A diversified complement of electronic parts is available to structure modern military electronic systems. These parts constitute the building blocks from which systems are fashioned and, as such, greatly impact hardware reliability. Since the reliability of the end item is dependent upon these building blocks, the importance of selecting and applying the most effective parts cannot be overemphasized.

The task of selecting, specifying, assuring proper design application and, in general, controlling parts used in complex electronic systems is a major engineering task. Part selection and control is a multidisciplinary undertaking involving the best efforts of component engineers, failure analysts and reliability engineers as well as design engineers. Numerous controls, guidelines and requirements must be formulated, reviewed and implemented during the development effort. The selection process for parts should include design evaluation, reliability history review, construction analysis, failure mode and effects analysis and cost effectiveness studies, as necessary. The control effort should include the development of meaningful procurement specifications which, when completed, reflect a balance among design requirements, QA and reliability needs consistent with apportionment studies and which cover:

- QA provisions (including incoming inspection)
- Quality Conformance/Qualification Testing

A well controlled parts program involves establishing a vendor control program, audits of vendor processes, the establishment of source inspection, where applicable, and the preparation of associated documentation. Table 5.1-1 presents a simplified list of the ground rules and activities needed to assure that this task is adequately considered. The material which follows provides detailed information, data and specific guidelines relating to the general ground rules listed in Table 5.1-1. Section 5.1 covers general part control considerations, while Section 5.2 provides specific part selection, usage and application guidelines as they apply to each generic part classification.

5.1.1 PART CONTROL

Part control activities comprise a large segment of the total effort for part selection, application and procurement. The effort encompasses tasks for standardization, approval, qualification and specification of parts which meet performance, reliability and other requirements of the evolving design. This subsection of the handbook provides further details with regard to these control tasks, indicates their importance within the part selection process and provides appropriate design guidance.

TABLE 5.1-1: GROUND RULES FOR PARTS SELECTION AND CONTROL

a) Determine part type needed to perform the required function and the environment in which it is expected to operate.

b) Determine part criticality.

- o Does part perform critical functions, i.e., safety or mission critical?
- o Does part have limited life?
- o Does part have long procurement lead time?
- o Is the part reliability sensitive?
- o Is the part a high cost item or does it require formal qualification testing?

c) Determine part availability.

- o Is part preferred?
- o Is part a Standard MIL item available from a qualified vendor?
- o What is the part's normal delivery cycle?
- o Will part continue to be available throughout the life of the equipment?
- o Is there an acceptable part procurement specification?
- o Are there multiple sources available?

d) Estimate expected part stress in its circuit application.

e) Determine reliability level required for the part in its application.

f) Appropriate screening/Quality Conformance Inspection (QCI) methods.

g) Prepare an accurate and explicit part procurement specification. Specifications shall include specific screening/QCI provisions to ensure adequate reliability.

h) Determine actual stress level of the part in its intended circuit application. Perform failure rate calculation per MIL-HDBK-217.

i) Employ appropriate derating factors consistent with reliability prediction studies.

j) Determine need for nonpreferred part and prepare a request for approval as outlined in MIL-STD-965.

Electronic parts for many electronic equipments constructed for military purposes are under the cognizance of the Military Parts Control Advisory Group (MPCAG), located in the Directorate of Engineering Standardization at the Defense Electronics Supply Center (DESC). This group promotes standardization in part selection and application. The use of preferred parts in new equipment design and development programs, saves considerable time and effort in documentation. Also, equipment performance and reliability are improved and logistic support costs are reduced.

DESC promotes the use of existing preferred parts and also conducts the standardization procedures for parts which are initially characterized as nonstandard but whose repetitive use makes their standardization necessary. DESC, as DoD's standardization manager, works closely with the military services and industry in developing an effective standardization program for new systems.

MIL-STD-965, Parts Control Program, details parts control procedures to be used in the design and development of equipment for military use. The DOD Parts Control System has as its objective the achievement of design to cost and life cycle cost savings and cost avoidances. This objective is to be achieved by applying techniques that: (1) assist equipment or system managers and their contractors in the selection of parts commensurate with contractual requirements, (2) minimize the variety of parts used in new design, (3) enhance interchangeability, reliability and maintainability of military equipments and supplied and (4) conserve resources.

Guidelines for implementing a Parts Control System are found in MIL-STD-965. Some of the key points required by MIL-STD-965 include: (1) meeting between contractor and procuring activity 30 days after award, (2) outline specification formats, (3) identify critical items, (4) develop preliminary preferred parts list, and (5) define the role of management. The development of a Program Parts Selection List (PPSL) is the goal of the Parts Control System. Figure 5.1.1-1 gives a flow diagram of this task.

The underlying factor for a successful Parts Control System is cooperation between the contractor and the various DOD interfacing agencies. By following the guidelines outlined in MIL-STD-965, this spirit of cooperation can be nutured into a successful program resulting in less costly and more reliable equipment/systems.

5.1.2 PART SELECTION

The general rule for part selection is that, wherever possible, preferred devices should be used. These devices may be defined as those which by virtue of systematic testing programs and a history of successful use in equipment have demonstrated their ability to consistently function within certain specific electrical, mechanical and environmental limits and, as a result, have become the subject of military (MIL) specifications. MIL specifications which thoroughly delineate a part's substance, form, operating characteristics and testing methods exist, or are in preparation, for practically every known type of electronic component. These standards, whose contents are discussed in Section 1.1.3.4 (Testing of Electronic Parts) are:

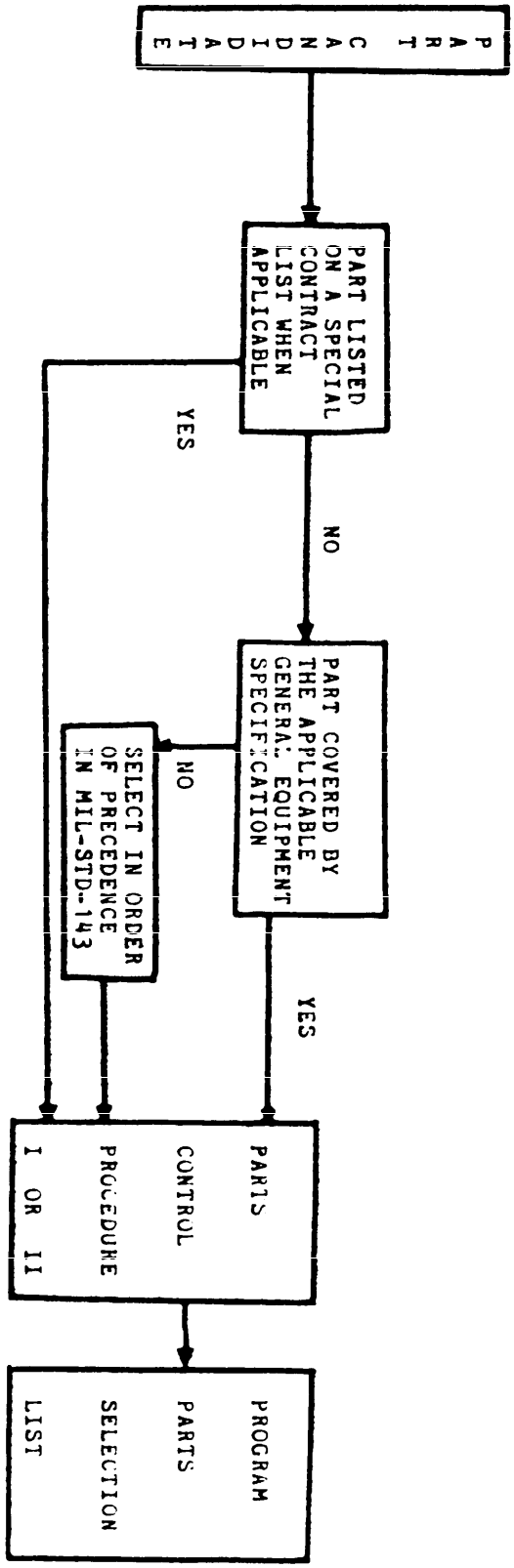


FIGURE 5.1.1-1: DEVELOPMENT OF A PROGRAM PARTS SELECTION LIST (PPSL)

- MIL-STD-202, Test Methods for Electronic Parts
- MIL-STD-750, Test Methods for Semiconductor Devices
- MIL-STD-883, Test Methods for Microelectronic Devices

In addition, military standards exist which list by MIL designation those parts or devices which are preferred for use in military equipment. For example:

- MIL-STD-199, Selection and Use of Resistors
- MIL-STD-198, Selection and Use of Capacitors
- MIL-STD-1132, Switches and Associated Hardware, Selection and Use Of
- MIL-STD-1562, Standard Microcircuits, Lists of
- MIL-STD-701, Standard Semiconductors, Lists of

5.1.2.1 MRAP/SRAP

The Rome Air Development Center (RADC), Griffiss AFB, NY 13441, has developed two computerized listings, Microcircuit Reliability Assessment Program (MRAP) and Semiconductor Reliability Assessment Program (SRAP) for use as the microelectronic and semiconductor device baseline for new system design.

MRAP is the procedure which tracks MIL-M-38510 detail specification (slash sheet) activity from the time that a device is selected as a potential standard part candidate through its inclusion on the Qualified Products List (QPL) for microcircuits. This can effectively be used to generate a microcircuit baseline Program Parts Selection List (PPSL).

Although MRAP maintains information on devices which are not recommended for use in new equipment designs, these devices will not be included in a MRAP generated PPSL. This is to insure that only proven high technology microcircuit types are identified for use in DOD equipments. The complete MRAP listing contains information on the status of all phases of device specification through QPL listing.

The SRAP program was developed for use in the evaluation of military system parts submittals for discrete semiconductors. The data which SRAP provides is in the form of a complete listing of all the devices which are currently covered under MIL-S-19500, and it is intended to be used as the semiconductor baseline for military system usage. The SRAP listing is divided into THREE sections: (1) devices which are preferred and recommended for use, (2) devices not recommended for new designs for which there are substitutes, and (3) devices which will not be approved for new designs. In the first section, the devices are listed in order of their EIA/JEDEC registration number and accompanied by all pertinent information including QPL status. The second section of the SRAP listing is composed of a series of tables which are broken down by device function. The devices are listed by part number within each table. For the devices which are not recommended for use, an alternate perferred device is indicated.

The use of MRAP/SRAP by circuit designers as a baseline parts selection guide is encouraged, because it includes the latest status of DoD microcircuit specifications, it indicates that electrical characterization is either planned or underway, and it provides device selections that are usually not single source items. As a result, fewer nonstandard part drawings will require approval, nonstandard part negotiations should be minimized and an improvement in system level reliability and life cycle costs should result.

The data base for MRAP/SRAP is continuously updated as new device types are selected for specification coverage and as the status of existing devices or specification changes. The information used for this update is developed from inputs provided by RADC, DESC, NASA, and other military agencies. Quarterly issues of the MRAP/SRAP data are now available in the form of a quarterly updated loose leaf volume from the Reliability Analysis Center, Griffiss Air Force Base, NY 13441.

Also, the MRAP/SRAP data base is now used for the preparation and updating of MIL-STD-1562 and MIL-STD-701. Plans are to update these documents quarterly.

5.1.3 PART APPROVAL

Although this Handbook calls for the use of preferred electronic and electromechanical parts, there may be cases where the application of existing preferred parts is not feasible or suitable. Such cases require part and procurement specifications approval and is comprised of those activities required to document and secure authorization to use the part in the system. MIL-STD-965 outlines the functions of a Part Advisory Group or a Part Control Board operating under both government and contractor cognizance, which provides the necessary mechanism for securing approval of these parts.

5.1.3.1 PART JUSTIFICATION

The use of all parts requires justification in accordance with MIL-STD-965. In addition to the requirements of MIL-STD-965 at least the following detail must be provided:

o Data must be provided sufficiently detailing why the proposed part is needed including advantages and disadvantages. New technology devices, custom hybrid and monolithic microcircuits should be treated in great detail and early in the system development cycle.

o Provision of data that substantiates that the electrical performance characterizations are compatible with the long life reliability assurance criteria of the application.

o If the part need is dictated by size, cost or weight, detail effect on reliability in the long term deployment of the equipment.

5.1.3.2 PART APPLICATION

When any part is proposed for an application beyond the recommended device parameters criteria supplemental justification should be required. For example, if a tantalum capacitor is intended for use at a frequency not recommended by the typical application, objective data should be presented to show that the capacitor will perform the desired circuit function without degradation of reliability over the expected life cycle mission of the system or equipment.

5.1.3.3 PART PARAMETERS

When any part is proposed for an application in which circuit performance depends on a characteristic or parameter that is not controlled by the governing specification, justification for use of the part shall include substantive data to show that the parameter will be maintained. Such justification should include data that shows that interrelated parameters are controlled to the extent necessary to assure that the critical parameter will be consistently within established limits or that supplementary parameter limits have not been imposed by specification which add prohibitive cost or effect availability.

5.1.4 CRITICAL PARTS

The parts control effort includes identifying all critical parts, equipment/components, and other items considered critical from any of the following standpoints:

o mission and safety sensitive (failure impacts mission success and flight safety, i.e., flight safety critical)

o reliability sensitive (from early R studies, apportionments, etc.)

o limited life (are required to operate for short time periods under conditions of great overstress)

o high cost items

o long procurement lead times

o require formal statistical qualification testing

Some device types which fulfill most or all of the above criteria for criticality include custom LSI and hybrid microcircuits. The criticality of these items are not related just to reliability but include cost and availability as well.

These devices should be divided into three categories:

A unique new device that has never been made before
A device that has been qualified through previous system usage
A device that is customized only at final metallization

In most cases, it is the unique device that creates the most unpredictable cost and schedule problems because it requires that both the device and system be developed concurrently, thereby, compounding the problem. Usage of the second category device is not as risky, but if the sole source vendor loses the recipe or decides to discontinue the production line without adequate warning serious problems can develop. The last category of device is considered the least risky. Experience gained from monitoring custom LSI or hybrid developments as well as the utilization of new complex devices in general, indicate that a pessimistic view must be taken regarding the impact of these items on cost and schedule. Examination of the intricacies of chip or circuit design, electrical verification, production design and electrical characterization reveals a design to shipment time cycle of approximately two (2) years for complex microcircuits from a high volume semiconductor manufacturer. When this development cycle is initiated by a system house, i.e., chip design, fabrication and packaging, the time cycle is often increased. Finally, when the custom device is ready for production applications and reliability characterization has not been completed, system reliability can be affected, thus impacting on schedule and cost.

In conclusion, a cautious parts control approach that limits the use of unique custom LSI or hybrid devices is recommended. This requires a detailed technical review and approval prior to designing the devices into the system. Also, a requirement in the system specification to identify and control these types of devices as critical reliability items is a must. However, when these devices are necessary to satisfy technical (i.e., not reliability) requirements the system program office must be provided guidance to enable the establishment of a realistic delivery schedule and adequate product assurance testing. Recent developments which directly affects the acceptability of hybrid devices for use by the military has been the revision of Appendix G to specification MIL-M-38510. This revision incorporates many changes and defines many requirements which clarify quality levels, and test and procurement procedures of vital importance to both vendor and user.

In addition to defining custom hybrid microcircuits, Appendix G now imposes two levels of product assurance - Classes S and B. The devices included as custom hybrid microcircuits are the conventional digital and analog (or combinations thereof) types and microwave and surface-acoustic-wave (SAW) devices.

Along with the expansion of device type and class coverage in MIL-M-38510, Appendix G includes the following:

- Traceability of elements and materials used in device manufacture will be required
- Process and quality audit will be required
- Process unification details and design guidelines will be issued
- Process traceability will be required
- Applicable areas relative to hybrid microcircuit design, manufacture and test are now covered
- Screening and processing to Method 5008 of MIL-STD-883 is expanded
- Water vapor content is lowered to 5000 ppm for Class B, and a value of 3000 ppm was established for Class S devices

Major rework relaxations permitted are:

- Temperature excursion on rework may not exceed original temperature excursion (relative to epoxy bonding)
- Rebond criteria are removed for Class B devices
- The limitation on the number of rework cycles has been removed. Epoxy bonded elements may be replaced up to two times (once for Class S devices) and eutectic bonded devices may be replaced once
- Substrate placement into a new package is permitted one time
- One time package delidding is permitted for Class B devices

These significant changes will enable the hybrid microcircuit manufacturer's yield to improve legitimately without affecting quality or reliability and will give birth to a series of standard hybrid microcircuits which will be qualified and certified to the requirements of MIL-M-38510.

Another significant document used to ensure that hybrid microcircuits will be reliable and of high quality is MIL-STD-1772, "Certification Requirements for Hybrid Microcircuit Facilities and Lines." The purpose of this standard is to establish criteria for certification (as required by MIL-M-38510). Definite criteria will insure that hybrid microcircuits are manufactured under conditions which have been demonstrated to be capable of continuously producing highly reliable products. This is accomplished by evaluating the manufacturer's capability for holding critical processes within established limits at specified critical points and continuously maintaining this capability during production. The certification and the maintenance is performed in advance and independent of procurement. The intent of the document is to standardize the documentation and testing for hybrid microcircuits for use in military and aerospace application. It covers the interface between user and manufacturer and it is not intended

to be a complete set of documentation required to build hybrid microcircuits.

In the Custom LSI and VLSI area, RADC is presently preparing test procedures for screening and quality assurance testing as part of the VHSIC Program.

Planning for critical item control must include special handling, the identification of characteristics to be inspected or measured during incoming inspection material review procedures, traceability criteria and periodic audits.

5.1.5 FAILURE RATE PREDICTION

The intent of the parts selection and control effort is the selection and application of parts in such manner as to achieve the lowest possible failure rates for the parts and subsequently for the equipment in which they are used. The recommended methods for the selection, screening and stress reduction (i.e., derating, mounting, etc.) of components are outlined in MIL-STD-454, "Standard General Requirements for Electronic Equipment," Requirement 64 and Microelectronic Devices are all pointed towards the accomplishment of this end.

5.1.5.1 MIL-HDBK-217

Designers of equipment intended for military use are required by contract to demonstrate a reliability prediction for the equipment, based upon the parts failure rate prediction models of MIL-HDBK-217 (Reliability Prediction of Electronic Equipment).

A discussion of the use of MIL-HDBK-217 failure rate prediction models and methods and how reliability prediction fits into an overall system stress analysis is presented in Volume 1, Section 6.4 of the Handbook, and again in Appendix A, and need not be repeated here. However, a delineation of those design, environmental and operating stress factors which have an affect on the failure rates of parts is necessary.

Some key points are:

(1) Not all types of devices are affected by all of the four basic MIL-HDBK-217 factors of temperature, environment, quality level and stress ratio.

(2) There are failure rate factors unique to certain part types and styles.

(3) Some types of parts have failure rate factors additional to those spelled out in MIL-HDBK-217.

MIL-HDBK-217 is a dynamic document. Due to the steady accumulation of real-time operating life data which substantiates changes in or additions to its panoply of failure rate prediction models, it is constantly being revised, but because the accumulation of adequate life data requires the passage of a considerable amount of time, the base failure rates and the

• Acceptable Quality Level (AQL) - This is often referred to when

reliability prediction models (especially for active devices) generally lag behind the state-of-the-art. Nevertheless, MIL-HDBK-217 serves the electronics community as a common reference point, with a common language and a commonly accepted means of establishing component part and equipment reliability.

A governmental contract under the auspices of RADC/RB, Griffiss AFB, NY 13441, serves as a focal point for the collection, storage and analysis of data reflecting the operational reliability experience of microelectronic and nonelectronic (i.e., switches, sockets, gyros, transducers, relays, sensors, etc.) parts in many ongoing military and industrial programs.

Analyzed failure rate, failure modes and mechanisms, and failure analysis information from these programs are published and sold under a Department of Defense cost recovery directive.

In the these databooks the observed, real-life failure rates are compared, on a generic part type basis, with appropriate MIL-HDBK-217 failure rate predictions. This information can serve a design or reliability engineer as a useful tool in parts selection and application considerations.

The government contractual agency monitoring this aspect for RADC is the Reliability Analysis Center (RAC), RADC/RBRAC (Bldg. 104), Griffiss AFB NY 13441-5700.

5.2 PARTS SELECTION GUIDELINES

5.2.1 MICROCIRCUITS

5.2.1.1 SELECTION GUIDELINES

The selection of a specific microcircuit type for use in military equipment is governed by the criteria defined in MIL-STD-454 Requirement 64 and is depicted in Table 5.2.1.1-1.

TABLE 5.2.1.1-1: MICROCIRCUIT SELECTION GUIDELINES

1.	MIL-M-38510 JAN microcircuits listed in MIL-STD-1562.
2.	Other MIL-M-38510 JAN Microcircuits.
3.	Other microcircuits subject to procuring activity approval. MIL-STD-965 shall govern the procedures for part selection and approval.

5.2.1.1.1 MONOLITHIC MICROCIRCUIT TECHNOLOGY

During the past decade microelectronic technology has evolved at a staggering pace resulting in dramatic advances in integrated circuit physical and performance characteristics. The two principal motivating forces which are responsible for the technological advances are circuit performance and economic benefits. The levels of circuit integration are continually being raised to incorporate more complex functions, thereby reducing electronic equipment size and cost.

Microelectronic devices offer several advantages over circuits made from discrete devices. Complex circuits can be made with a minimum of connections within a hermetically sealed package, thereby increasing the overall system reliability. Higher packaging densities reduce the size of end products and minimize propagation delay times.

Circuit integration, however, is not without concerns. Some of the major considerations which should be reviewed during any microcircuit implementation with a system are:

o Technology Tradeoffs. Within the two groupings of microcircuits (Linear and Digital), there are several technologies to choose from. Each technology provides the designer with an unique collection of functions and capabilities. The major divisions of technologies are bipolar and MOS. These two technologies are further subdivided based on unique processing and design techniques. Discussion of the specifics of these technologies are found in Section 5.2.1.1.2.

o Speed Tradeoffs. This area of concern with microcircuits is mainly technology related. For years bipolar devices outperformed MOS devices in speed. Today, with new designs and processing techniques MOS in some applications is outperforming bipolar.

o Timing Considerations. Care should be taken in the design of a system to avoid timing or "race" conditions. Timing conditions can occur due to misapplication of a microcircuit, such as improper consideration of delay times or improper mix of technologies.

o Temperature Considerations. Heat is one of the more destructive elements on microcircuits. One's design should take into consideration the following factors all of which effect device temperature; maximum ambient (environment) temperature, cooling techniques, technologies chosen, packaging and heat sinking and system speed. These factors will be discussed in further detail in Section 6.2.

o Packaging Considerations. The overall reliability of a system design can be greatly affected by the microcircuit packaging techniques chosen. In military systems plastic or epoxy packaging techniques are not recommended due to the inherent reliability problems associated with the non-hermeticity and rate of wirebond/plastic coefficients of expansion. Also, proper packaging practices can significantly lessen the detrimental effect of temperature on integrated circuits. Epoxy die attach is not recommended since they can outgas corrosive contaminants into the hermetic package ambient thereby significantly lowering device reliability. Section 5.2.1.2.2 discusses these concerns in more detail.

5.2.1.1.2 BIPOLAR DEVICE TECHNOLOGIES

Technology advances which have facilitated the evolution of bipolar technologies into complex and LSI devices include: 1) Schottky barrier contacts to limit voltage swings, prevent saturation and increase speeds; 2) dielectric isolation techniques to reduce device size and parasitic effects; 3) ion implantation to control impurities and tolerances; 4) thin epitaxial growth techniques to reduce size; 5) triple diffusion process without a buried layer which simplifies fabrication techniques; 6) implementation of PNP transistors for specific application requirements.

Conflicts between power dissipation, density and speed requirements have diminished the emphasis on bipolar technologies for LSI designs. FET or MOS technologies with self isolation, high impedance load devices, lower power dissipation and less complex processing have been much better suited to LSI design, making their relatively slow speeds more tolerable.

Even within the bipolar family a wide variety of attributes can be obtained as a result of various enhancements. To understand how these attributes are derived a description of the major bipolar technologies is presented.

o TTL and Schottky TTL. TTL (transistor/transistor logic) is one of the oldest and most basic bipolar technologies. This technology evolved from its predecessors RTL (resistor/transistor logic) and DTL (diode/transistor logic). The TTL fabrication techniques and basic circuit elements provided the opportunity to incorporate large numbers of devices on a single chip at reasonably fast switching speeds and low power dissipation.

TTL is a saturating logic technology. Gold doping is employed to reduce minority carrier lifetimes and increase speeds. The gold diffusion also reduces the transistor betas and degrades yields due to the critical nature of the diffusion.

Schottky TTL (STTL) is a nonsaturating logic form. The Schottky transistor employs a Schottky diode in parallel with the collector base junction. The diode has a lower forward voltage than the collector base junction which allows it to shunt excess base current reducing the stored charge at the junction and preventing saturation. This results in improved switching speeds over TTL in addition to reduced power dissipation. The STTL speed power product is about half that of TTL (60pj compared to 100pj) despite its higher power dissipation. STTL devices offer lower output impedances which can drive higher capacitance loads with very low susceptability to AC noise. The Schottky clamped input diodes suppress line noise due to the transfer characteristics which are much sharper than TTL and reduce undershoot risetime effects.

The typical STTL gate propagation delay is 3nS with a power dissipation of about 20mW/gate. Rise and fall times are in the 2-3nS range. The area required for a STTL circuit is about half of a standard TTL which affords higher densities. The use of Schottky clamps also enhances performance through the elimination of gold doping which improves the stability of AC delays and DC thresholds over operating temperature ranges.

The major disadvantage of STTL is its high power dissipation. The dissipation at low and medium frequencies (approx. 10 to 20 MHz) is somewhat comparable to standard TTL. However, at higher frequencies the dissipation increases dramatically. This increase in dissipation is attributed to the overlap of the low impedance totem pole output and current spikes which result from stray capacitances at the device output. At 100MHz, power dissipation can be about 2½ times its DC dissipation value.

Another family of logic which recently has become popular is the low power Schottky family. Low power Schottky TTL integrated circuits are now firmly established as the standard logic configuration for new high performance system designs. They have essentially replaced standard "gold doped" TTL devices in all applications. In addition, they have relegated the other logic families to specialized needs where the ultimate in high speed (ECL) or low power for battery operated operation (CMOS) is mandatory.

This wide acceptance has been achieved because LS offered all of the important features of the earlier TTL families with two significant advantages:

(a) LS circuits provide performance equal to that of standard TTL at between 20% and 50% of the power requirements. As a result, considerable system cost savings have been made in bulky power supplies and fans.

(b) LS technology allows more complex designs to be fabricated on a given die size. A far wider selection of system's oriented MSI and LSI functions have, therefore, been developed in the LS family.

(c) Typical gate propagation delay is 10 ns/gate with a typical power dissipation of 2mw/gate.

The LS TTL family devices is preferred over the standard TTL family for new designs.

The next generation of the TTL family lowers the speed power curve further. These include FAST family with 3ns/gate delay at 6mw/gate power dissipation and the ALS family with 6ns/gate delay at 1mw/gate power dissipation. ALS and Fast generally have higher input thresholds by design than LS and Schottky. This improves the low level noise margin. A full TTL compatible family is available in these two technologies.

o ECL. (Not preferred for new designs) ECL (Emitter-Coupled Logic) is another nonsaturating logic form. ECL transistors are operated in the active region never actually being fully turned on or off. ECL has a gate propagation delay of 1-3nS but a per gate power dissipation of 30mw. Also, ECL requires compensating circuitry to maintain voltage and temperature stability. ECL has a speed power product of 100pj compared to 60 pj for STTL. ECL is not easily interfaced with TTL families due to power supply and logic level requirements.

The major disadvantage of the ECL technology is its very high power dissipation. While the power dissipation is essentially constant with frequency, large complexity ECL circuits require special thermal enhancements to provide thermal stability. Additionally, its extremely high switching speeds can necessitate special interconnection and wiring techniques to avoid undesirable noise and reflection problems.

ECL circuits are, however, the fastest of all currently available technologies and have continued to provide the mainstay for low density, high speed technology applications. (Not preferred for new designs.)

o I^2L. I^2L (Integrated Injection Logic) is one of the latest additions to the bipolar technology family. The simple 4-mask, 2-diffusion I^2L process fabrication complexity compares favorably to all technologies including TTL's 7-mask, 4-diffusion and CMOS's 6-mask and 3 diffusions. The chip area required for I^2L is less than one-tenth the area of conventional TTL or CMOS gates and occupies one-fourth the space of the latest LSI forms of TTL. I^2L has the lowest speed power product of any current technology, approaching a theoretical limit of 10^{-2} picojoules. I^2L gates can be pushed at 10 to 20nS while maintaining a virtually constant speed power product.

I^2L logic eliminates the fundamental limitations of conventional bipolar circuits: space consuming resistors and isolation. I^2L circuits use pnp transistors as current sources and npn transistors as drivers and switches. Furthermore, the npn transistors are implemented in an inverted fashion with the collectors on top and emitters below. Emitter follower circuits are readily fabricated by a triple diffusion process consisting of vertical npn transistors. Current hogging logic circuits are also possible with lateral npn and pnp transistors with a heavily doped n+ under the device functioning as the buried base.

I^2L's major advantage is the ability to combine relatively low speed, low power PNP devices for high density memories with high speed, high gain, npn devices for off the chip buffering, driving and amplification all on the same chip.

5.2.1.1.3 MOS Technology Families.

Metal Oxide Semiconductors (MOS) processes have become a dominant force in state-of-the-art semiconductor technology. The simple fabrication processes and high densities of MOS devices makes them ideal for LSI and VLSI components.

o Standard P Channel MOS. The standard PMOS process has the highest yield per unit area of any MOS process. With only four mask steps and one diffusion, it is also one of the simplest devices to fabricate. Its slow speed (less than 1 MHz) and relatively high power dissipation limit its usefulness in many applications. A speed/power product of 900 picojoules ranks PMOS towards the bottom of the scale. Power supply voltages of 10 to 15 volts are usually required, and logic levels are not usually TTL compatible.

o Silicon Gate PMOS. The silicon gate PMOS offers lower threshold voltages and lower gate-to-drain capacitances than the standard metal gate PMOS. This allows for speeds of up to several megahertz. This improved performance is achieved at the expense of additional processing and reduced yield.

o Silicon Gate N Channel MOS. Silicon gate NMOS offers low threshold voltages, high speed and high packing density, making it extremely popular for LSI devices such as microprocessors and semiconductor memories. Logic levels are TTL compatible, and supply voltages are usually compatible with TTL circuitry. Speed power products of the order of 100 pj can be routinely achieved with this process.

On the negative side, the tight tolerance on the threshold voltage of N channel devices is more difficult to maintain. The tight spacings used to achieve maximum densities in LSI devices further increase stability problems. The maturity of this process, however, has minimized problems in this area, so that present day NMOS technology is as reliable as any on the market.

o Complementary MOS(CMOS). Complementary MOS circuitry, using both PMOS and NMOS circuitry offers low power, moderately fast throughputs, single power supply requirements, minimum clocking requirements and full swing of output voltage. The high threshold voltage of the CMOS gate provides good noise immunity. CMOS is usually employed where low power is a major consideration. Recent process improvements have dramatically increased the speed of CMOS devices. CMOS devices are now being introduced into the linear arena. Many major semiconductor manufacturers are directing their efforts towards this technology for VLSI because of recent developments, e.g., P^2 CMOS, M^2 CMOS and others.

o Silicon-on-Sapphire Technologies. Silicon-on-Sapphire (SOS) is the most common implementation of the more general class silicon-on-insulator. By producing an integrated circuit on an insulating substrate, a number of improvements can be achieved, including improved resistance to radiation, high speed and good packaging density.

Although any MOS circuitry can be fabricated using SOS processing, it is most often produced using CMOS. CMOS/SOS circuitry is particularly important in military applications requiring radiation hardened circuitry.

Important characteristics of each of the various microcircuit technologies are summarized in Figures 5.2.1.1.2-1, 5.2.1.1.2-2, 5.2.1.1.2-3 and 5.2.1.1.2-4 and in Table 5.2.1.1.2-1. These illustrations permit rapid comparison of alternative technologies with respect to specific parameters of interest in any given application.

5.2.1.2 APPLICATION CONSIDERATIONS

Standard ICs in accordance with MIL-STD-1562 should be used to the fullest extent practicable. Some general application considerations are discussed in the following paragraphs.

5.2.1.2.1 IC PACKAGE TYPES

There are four basic types of IC packages (reference Appendix C of MIL-M-38510). These are: type F - flat packs; type D - dual in line; type A - metal can; and type C - chip carriers. TO-3 packages are also used where high power dissipation is involved, such as with voltage regulator circuits.

The real weak spot in any IC package is at the seals where the leads enter the case or body. These seals are usually of glass and can be easily broken, exposing the chip and metal inside the package. This can occur if the leads are bent or twisted during production or repair. Also, broken seals can result in moisture and other undesired elements entering the IC package. While this may not cause immediate failure, it will shorten the life of the IC. The exposed bare metal under the seal can also corrode and affect the IC's performance.

DIPs are ideally suited for mounting on printed circuit (PC) boards. During production, DIPs can be inserted (manually or automatically) into mounting holes on PC boards and soldered by various mass production techniques.

However, the DIP is relatively large and heavy, and as pin counts increase (as with VLSI devices) these factors are aggravated. In addition, the resistance and inductance from the corner pins to the input/output terminals of the die become significant for high speed functions, quickly approaching DIP's 500-megahertz limit. Leadless chip carriers raise the speed limit out to 4-gigahertz and these packages will play a significant role in the DOD VHSIC program. Chip carriers present an opportunity to halve the memory real estate on printed wiring boards while improving the capabilities and, potentially, the reliability of electronic equipment.

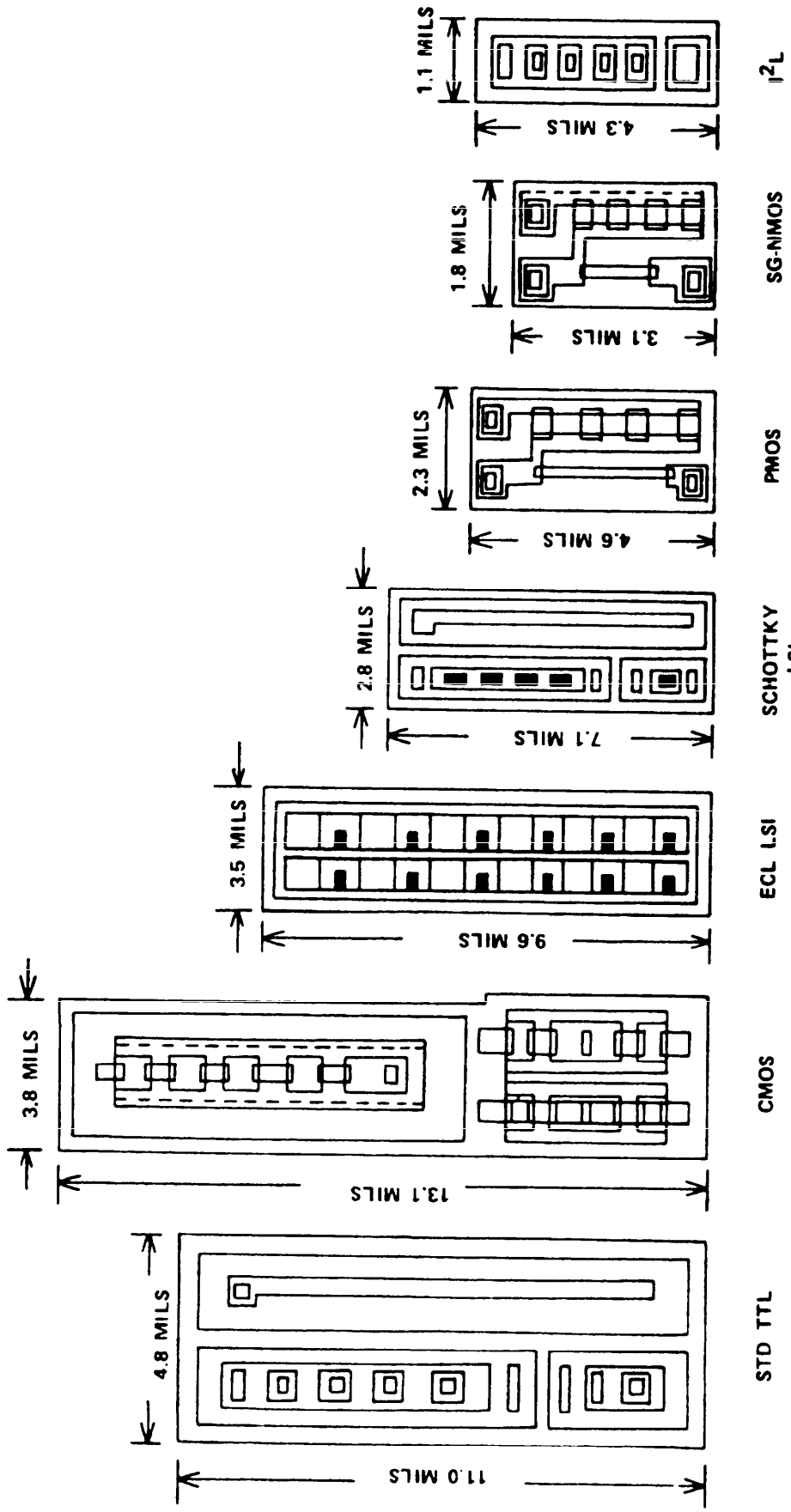


FIGURE 5.2.1.1.2-1: FABRICATION AND DESIGN DETAILS OF ALTERNATIVE MICROCIRCUIT TECHNOLOGIES

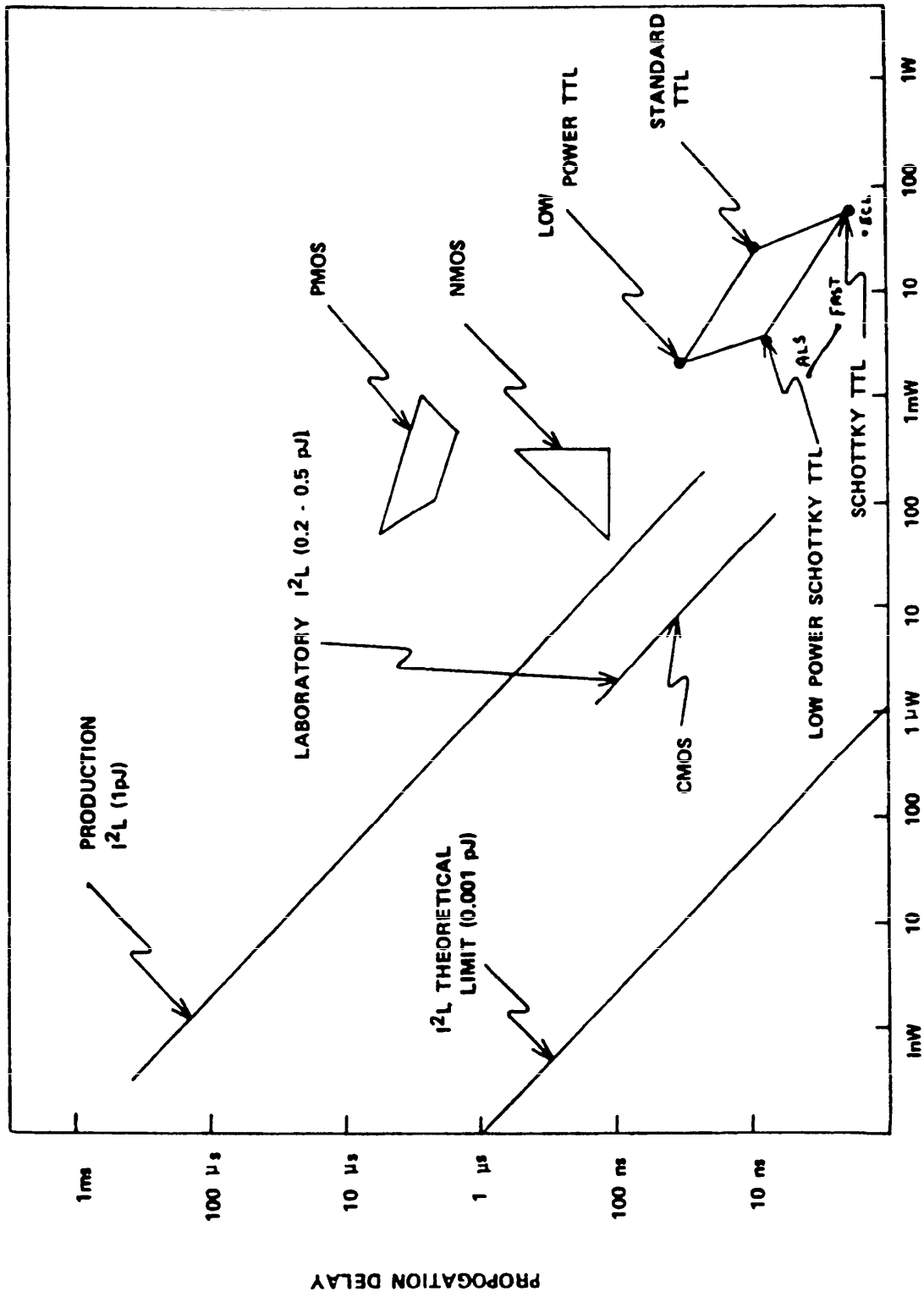
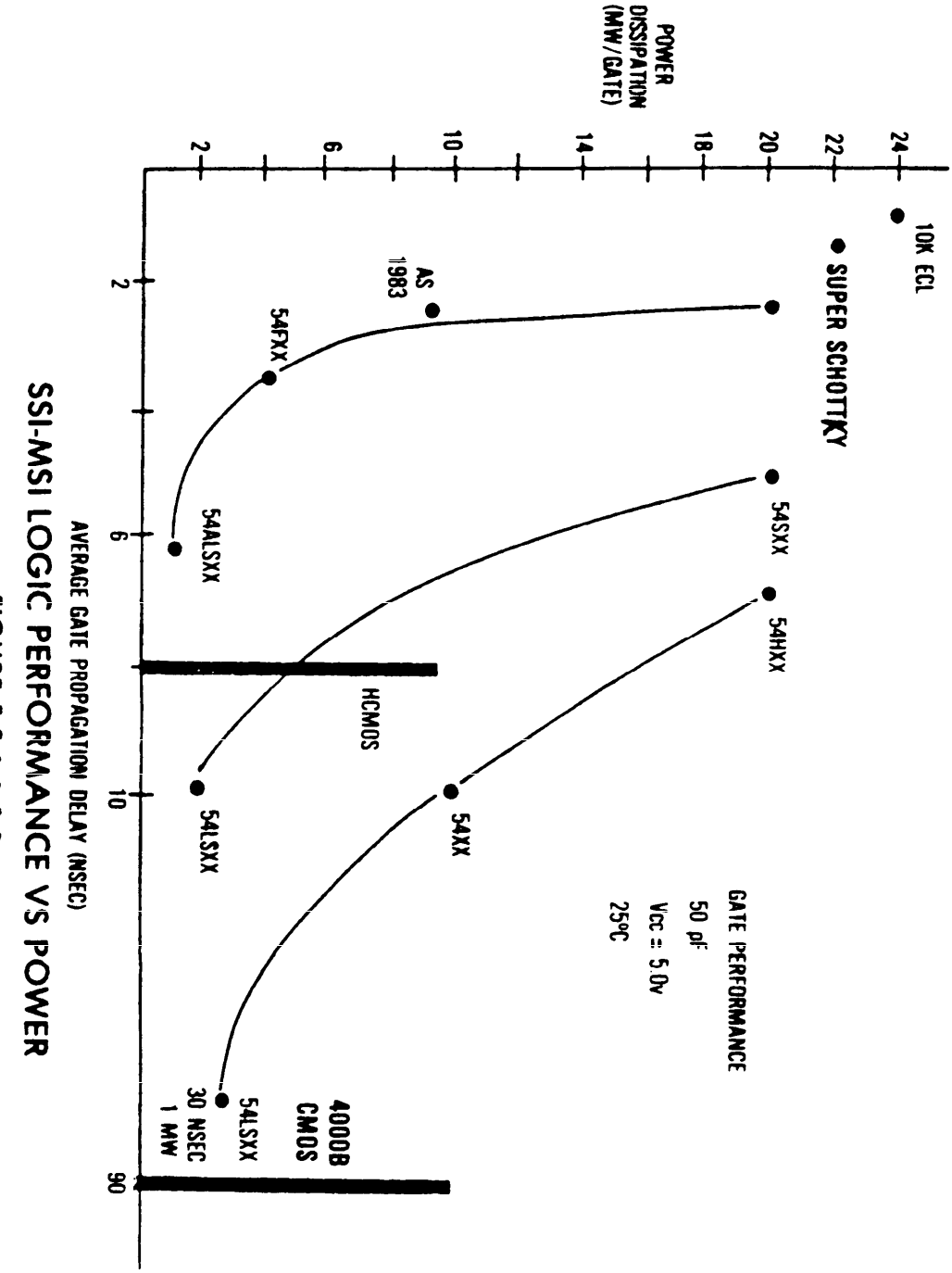


FIGURE 5.2.1.1.2-2: SPEED AND POWER TRADEOFFS FOR ALTERNATIVE MICROCIRCUIT TECHNOLOGIES



SSI-MSI LOGIC PERFORMANCE VS POWER

FIGURE 5.2.1.1.2-3

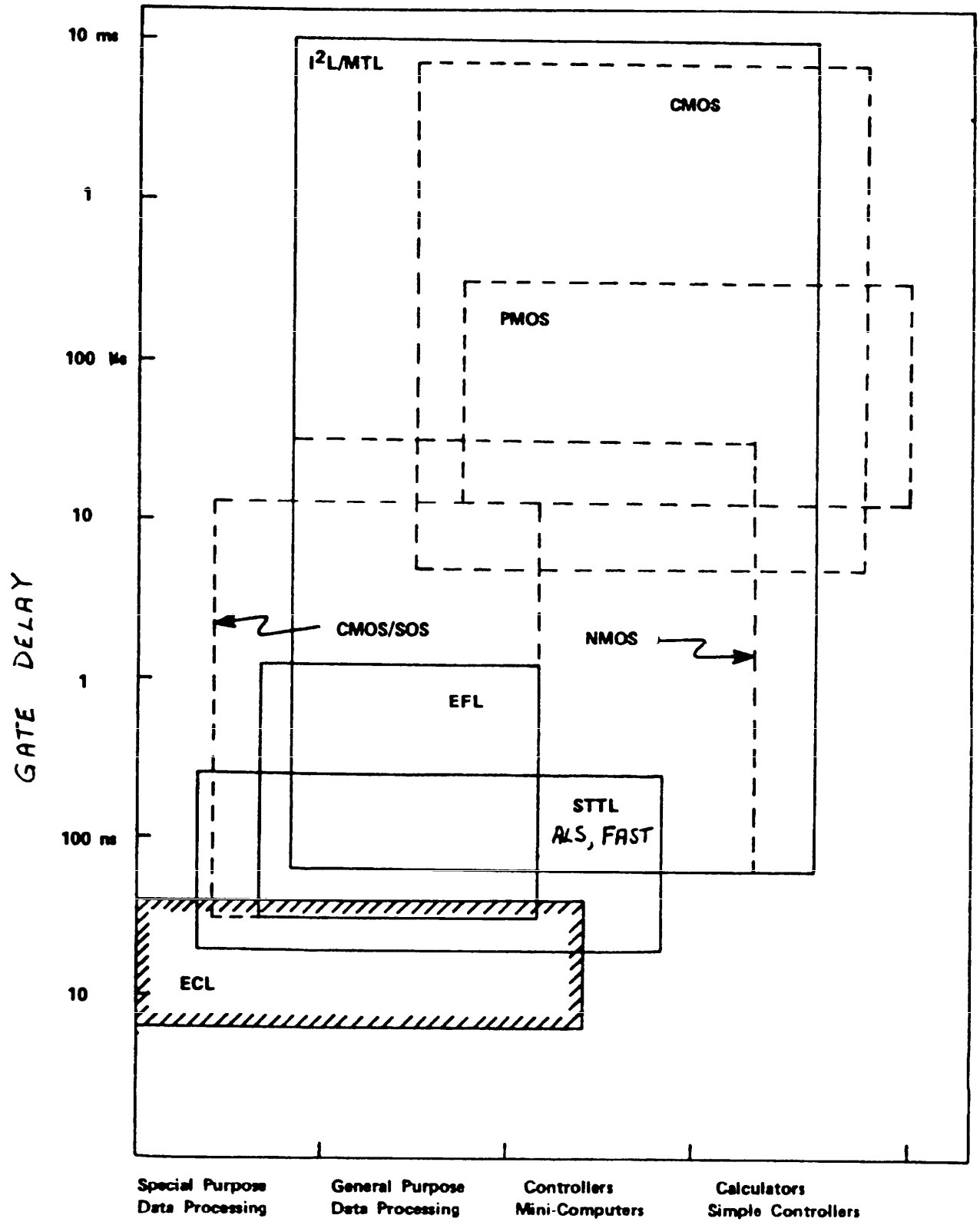


FIGURE 5.2.1.1.2-4: SPEED AND APPLICATIONS OF ALTERNATIVE MICROCIRCUIT TECHNOLOGIES

TABLE 5.2.1.1.2-1: LSI TECHNOLOGY CHARACTERISTICS

PARAMETER/ TECHNOLOGY	TYPICAL PROPAGATION DELAY (ns)	TIMING PULSE REQUIRED FOR LSI (ns)	TYPICAL POWER DISSIPATION PER GATE (μW)	CHIP DENSITY GATES/MIL^2
PMOS	30-100	1000-2000	20-700	0.5
NMOS	20-70	200-1000	20-700	0.5
CMOS	40-100	50-200	1-1000	0.2 - 0.3
PMOS/SOS	30-100	100-500	70-700	0.5
NMOS/SOS	25-50	80-250	70-700	0.5
CMOS/SOS	10-40	70-200	90-100	0.3
I^2L	15-40	80-200	100-200	1.0 - 2.0
LOW POWER TTL	30-50	400	1000	0.2
TTL	8-12	70	10,000	0.2
LOW POWER SCHOTTKY	8-12	70	2000	0.1 - 0.2
SCHOTTKY	3-5	50	20,000	0.1 - 0.2
ECL	1-2	40	20,000-30,000	0.1 - 0.2
FAST	3-4	70	4000	.01 - .02
ALS	6-7	70	1000	.01 - .02

TO-5 packages in general should not be used in avionics or other applications involving vibration, shock or acceleration, since they are mounted cantilevered by their leads with no support for the body. When TO-5 cans must be used, a dielectric spacer should be employed to provide mechanical support to the body of the package.

Ceramic flat packs are being phased out by the chip carriers, which have the size advantages of flat packs along with much greater interconnection density.

5.2.1.2.2 MOUNTING AND CONNECTIONS

Once the package type has been selected, the IC must be mounted and electrically connected to other parts. The selection of a particular method of mounting and connection of ICs depends upon: the type of IC package, the equipment available for mounting and interconnection, the connection method used (soldering, welding, crimping, etc.), the size, shape and weight of the overall equipment package, the degree of reliability, the ease of replacement in the field, and the cost factor. The following sections summarize mounting and connection methods for the three basic package types.

o Ceramic Flat Pack Mounting and Connection. There are a number of methods for making solder connections to flat packs. The notch in one end of the package which is used as a reference point to identify the lead numbering is generally nearest to lead number 1. Always consult the manufacturer's data regarding IC lead numbering.

Some common soldering techniques use in-line lead and pad arrangements. Although such arrangements simplify lead forming, they result in very close spacing between leads (typically .032 inches) and require the use of high precision production techniques in both board manufacture and the assembly of ICs on the board, particularly when the leads must be inserted through holes on the PC board. Another disadvantage of the in-line arrangement is the limited space available for routing circuit conductors between adjacent solder pads.

o Dual-In-Line Package Mounting and Connection. Because the package configurations are very similar, the mounting arrangements and terminal sorting techniques used for these circuits are much the same as those used in the in-line method for the flat pack ICs. The DIP terminal leads are larger than those of the flat pack; the larger sized terminals are more rigid and more easily inserted in PCB.

Another significant feature of the DIP is the sharp step increase in width of the terminals near the package end. This step forms a shoulder upon which the package rests when mounted on the board. Thus, the DIP package is not mounted flush against the board and, as a result, allows printed circuit wiring directly under the package.

o TO-5 Package Mounting and Connection. These packages provide a kovar header with kovar external leads to which the circuit is attached and over which a metal cap is welded. These packages offer the advantages of relatively good heat conduction, radiation, ease of obtaining a good hermetic seal, ruggedness and long experience of handling in manufacture. The principal disadvantages of these packages are their relatively inefficient use of space and the limited number of leads. Also, these packages require support to prevent fatigue or damage due to vibration or shock.

o Chip Carrier Mounting and Connection. The ceramic (hermetically sealed) chip carrier is leadless and must be mounted to a substrate which has a compatible temperature coefficient of expansion. In some cases they are reflow soldered to a ceramic motherboard which is then attached to a PC board. Since integrated circuit reliability is directly related to junction temperature, effective thermal design in mounting is important. JEDEC standards have specified two basic types of carriers.

The type A and type D carriers are cavity down. In these carriers, the die is closer to the top, where the best heat radiating surface exists. The types B and C carriers have a cavity-up configuration with the major heat radiating surface facing the board. Two types of heat transfer occur: conduction and convection. Most commercial systems employ forced air and convection cooling, so surface area is a key to good heat transfer. Most military manufacturers and some commercial ones do not have the luxury of moving in outside air with a fan and blowing it around their devices. They rely on conduction to transfer the heat through the frame to an outside heat sink. Thus, the thermal properties of the package must be factored into the design to prevent thermal overstress of the chip.

o Plastic Packages (Not recommended for designs.) In considering the type of package, it should be noted that plastic packaged devices tend to be less expensive but are more susceptible to seal leakage than ceramic packages. Therefore, for ranges of high relative humidity a ceramic package is recommended. The plastic package is also prone to contamination and wire bond intermittencies. Contamination may be caused by improper mix of the material or insufficiently thorough mixing process and is usually lot dependent.

The bond intermittency usually occurs as a result of internal wires and/or bonds broken by improper/uneven curing of the plastic. These broken wires/bonds are most commonly held in place by the plastic thus making a pressure contact. Quite often they are not detected during normal electrical testing. However, when the operating conditions change, the pressure contacts become intermittently open. This type of failure is difficult to detect and is expensive in terms of warranty repairs and customer satisfaction. Therefore, plastic packages are not recommended for use in military systems.

The goal of the VHSIC program is VHSIC production in the latter half of the

5.2.1.2.3 CONSIDERATIONS IN THE BOARD LAYOUT OF ICs

Different parameters should be considered in layout of each type of IC. For example, most linear ICs have high gain and are thus subject to oscillation if feedback is not controlled by proper design. On the other hand, digital ICs rarely oscillate due to operation of transistors in saturated or off states, but are subject to noise signals. Proper circuit layout can minimize the generation and pick up of such noise. The following paragraphs describe those circuit board layout problems that IC users must face at one time or another.

o Board Layout of Digital ICs. All logic circuits are subject to noise. Therefore, it is recommended that noise and grounding problems be considered from the very beginning of design layout.

Several types of noise must be dealt with in logic systems. The following classification of noise is used:

o External Noise - environmental noise radiated into the system. Such noise results from circuit breakers, brush motors, arcing relay contacts, or magnetic field generating activity.

o Power Line Noise - noise coupled through the ac or dc power distribution system.

o Cross Talk - noise induced into signal lines from adjacent signal lines.

o Signal Current Noise - noise generated in stray impedances throughout the circuit from the flow of required signal currents.

o Transmission Line Reflections - noise from unterminated transmission lines that cause ringing and overshoot.

o Icc Current Spikes - noise caused by switching of the output stage of bipolar devices.

Figure 5.2.1.2.3-1 lists the above noise types and shows some design considerations which if followed will help prevent system noise problems. A discussion of these considerations is provided here.

Noise Types	Considerations
External	Shielding
Power line	Grounding
Cross talk	Decoupling
Signal Current	Device Properties
Transmission Line	
Icc Spikes	

FIGURE 5.2.1.2.3-1: NOISE TYPE AND DESIGN CONSIDERATIONS

o Shielding - Noise pulses may come from many sources, but will be either an electrostatic field or electromagnetic field. The noise wavefront must be prevented from entering the equipment. These noise fields are usually changing at a rapid rate; therefore, the shield required may be quite small. For more effective exclusion, the sensitive circuitry must be completely shielded. Although aluminum or similar materials may be effective in stopping electrostatic noise, only a ferrous metal can successfully protect equipment against magnetic fields. It is helpful to connect the system to a good earth ground, but the shield system must be complete and must be grounded to the system ground; otherwise the shield may couple the noise into the system.

o Grounding and Decoupling - When digital circuits are driving transmission lines, care must be taken to assure that the transmission line is properly grounded. From transmission line theory, line termination is not a factor in drive current until after a reflected pulse returns from the termination to the transmitting device. If there is a poor ground return, current can flow in the transmission line ground. If the line and return are originated and terminated close to the driving and receiving devices, there is no discontinuity in the line. Where the ground is poorly returned; the currents flowing see the discontinuity in the cable as a high impedance, and a noise spike is generated. Figure 5.2.1.2.3-2 shows an example of noise generation in a transmission line.

If the ground return is properly made, desirable results are obtained in that the impedance discontinuity is eliminated and current cancellation occurs at the ground point. Undesirable voltage spikes are then eliminated. Three rules to reduce transmission line current effects are:

(1) Carry twisted pair and coaxial returns to a good ground termination close to the driving and receiving devices.

(2) Decouple Vcc of line driving and line receiving gates close to the device with a 0.1uf capacitor.

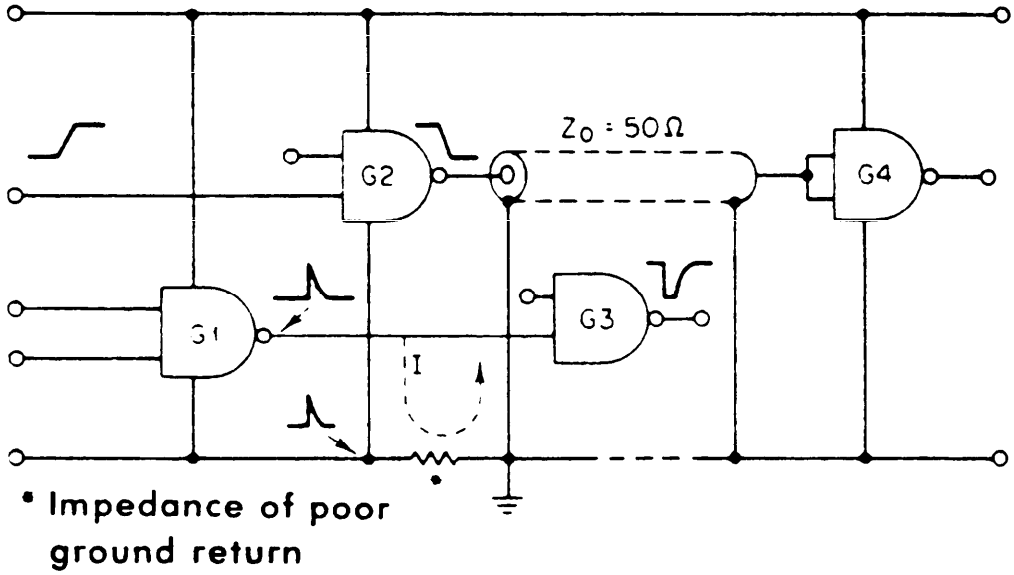
(3) Zero point grounding through a "mecca" ground.

Pulses on the ground line can quite readily exceed the noise threshold. Only if a good ground system is maintained can this problem be overcome.

The concept of a common ground plane structure as used in RF and high speed digital systems is quite different from that of the common ground point as used in low frequency circuits. The more closely the chassis and ground can approach being an integral unit, the better the noise suppression characteristics of the system. Consequently, all parts of the chassis and ground bus system should be bound tightly together electrically and mechanically. Floating or poorly grounded sections not only break the integrity of the ground system, but may actually act as a noise distribution system.

The matter of grounds and decoupling on printed boards requires some attention here. The most desirable arrangement would be a double clad board with one side carrying the interconnections and the other a solid ground plane. Where component density prohibits this, the ideal should be relaxed

d in the recommended ... the problem is evident, it shall be check



NOISE GENERATION DUE TO POOR TRANSMISSION-LINE RETURNS

FIGURE 5.2.1.2.3-2

only as far as necessary. Cross talk can be a problem on large boards; an adequate board ground mesh will go far in reducing cross talk as well as ground noise. Some suggestions for board grounds where a plane is not practical are:

(1) Make the ground strap as wide as possible everywhere, even though this may mean its width varies radically.

(2) Form a complete loop around the board; bring both sides of the board through separate pins to the system ground.

The Vcc line can provide part of the ground mesh on the board, provided it is properly decoupled. A good rule of thumb is 0.01uf per synchronously driven gate and a least 0.1uf per 10 IC packages regardless of synchronization. This capacitance may be lumped, but it is more effective if distributed over the board. A good rule to follow is to permit no more than 5 inches of wire between any two package Vcc points. RF-type capacitors for decoupling are mandatory; disk ceramics are a good choice. It is sometimes a good practice to decouple the board from the external Vcc line with 2.2uH inductor and a 10 to 50uf capacitor. It is also strongly recommended that gates driving long lines have the Vcc supply decoupled at the gate Vcc terminal and that the capacitor ground, device ground, and the transmission line ground be brought to a common point.

o Board Layout of Linear ICs - The basic building block for linear ICs is the op amp. Therefore, the discussion of layout suggestions will concentrate on op amps, but these suggestions are still useful for all types of linear ICs. Some of the design techniques for linear devices which should be considered include: passive component selection, bypassing decoupling/grounding, circuit layout and device protection.

o Passive Component Selection - Resistors and capacitors are the two most popular passive components in use in linear circuits. Tables 5.2.1.2.3-1 and 5.2.1.2.3-2 give the advantages and disadvantages of various resistors and capacitors, respectively.

The most basic electrical component is the resistor. The most popular systems of today are based on 12 bit accuracy and performance; therefore, errors or shifts in accuracy of as little as $\pm$ 0.012% in resistors can in some applications degrade performance to an unacceptable level. Resistor stability over the operating temperature range is an important consideration. Most users will recognize that the absolute temperature coefficient of resistors is not very crucial as long as those two resistors have matching temperature coefficients. Table 5.2.1.2.3-3 points out some temperature considerations in precision resistors. Also, Figure 5.2.1.2.3-3 provides some circuit board mounting techniques which should be followed for all resistors.

A capacitor can perform nonideally, thus compromising the performance of a precision circuit. A concern with ceramic capacitors used in linear circuits is dielectric absorption. Dielectric absorption, referred to by many as the memory effect, is the charge absorbed into the dielectric that is not immediately added to or removed from the capacitor when rapidly charged or discharged. This effect can be very damaging in data acquisi-

RESISTOR COMPARISON CHART

TABLE 5.2.1.2.3-1

TYPE	ADVANTAGES	DISADVANTAGES
DISCRETE		
Carbon Composition	Lowest Cost High Power/Small Case Size	Poor Tolerance (5%) Poor Temperature Coefficient (1500ppm/°C)
Wire-Wound	Excellent Tolerance (0.01%) Excellent TC (1ppm/°C) High Power	Reactance May be a Problem Large Case Size Most Expensive
Metal Film	Good Tolerance (0.1%) Good TC (<1 to 100ppm/°C) Moderate Cost	Must be Stabilized with Burn-In Low Power
Bulk Metal or Metal Foil	Excellent Tolerance (to 0.005%) Excellent TC (to <1ppm/°C) Low Reactance	Low Power Very Expensive
High Megohm	Very High Values (10^8 - 10^{14} Ω) Only Choice for Some Circuits	High Voltage Coefficient (200ppm/V) Fragile Glass Case Expensive

RESISTOR COMPARISON CHART

TABLE 5.2.1.2.3-1

TYPE	ADVANTAGES	DISADVANTAGES
NETWORKS		
Thick Film	Low Cost High Power Laser-Trimmable Readily Available Suitable for Hybrid IC Substrate	Fair Matching (0.1%) Poor TC (>100ppm/°C) Poor Tracking TC (10ppm/°C)
Thin Film on Glass	Good Matching (<0.01%) Good TC (<100ppm/°C) Good Tracking TC (2ppm/°C) Moderate Cost Laser-Trimmable Low Capacitance	Not Suitable for Monolithic IC Construction Delicate Often Large Geometry Low Power
Thin Film on Ceramic	Good Matching (<0.01%) Good TC (<100ppm/°C) Good Tracking TC (2ppm/°C) Moderate Cost Laser-Trimmable Low Capacitance Suitable for Hybrid IC Substrate	Often Large Geometry Not Suitable for Monolithic IC Construction
Thin Film on Silicon	Good Matching (<0.01%) Good TC (<100ppm/°C) Good Tracking TC (2ppm/°C) Moderate Cost Laser-Trimmable Suitable for Monolithic IC Construction	Not Suitable for Hybrid IC Substrate Some Capacitance to Substrate Low Power
Thin Film on Sapphire	Good Matching (<0.01%) Good TC (<100ppm/°C) Good Tracking TC (2ppm/°C) Laser-Trimmable Low Capacitance Suitable for Monolithic IC Construction	Higher Cost Low Power

CAPACITORS FOR SWITCHED DATA APPLICATIONS

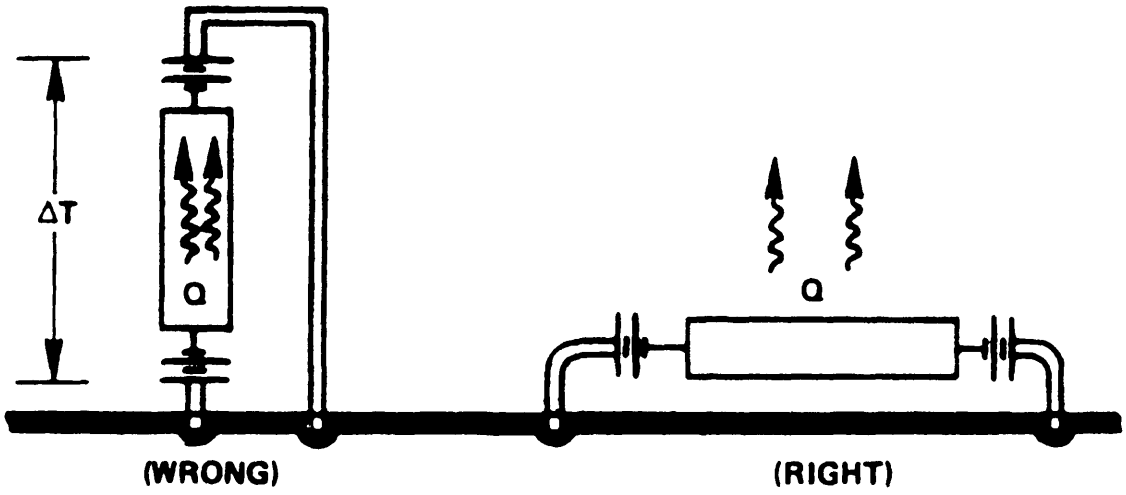
TYPE	TYPICAL DIELECTRIC ABSORPTION	ADVANTAGES	DISADVANTAGES
NPO Ceramic	0.1%	Small Case Size Inexpensive Good Stability Wide Range of Values Many Vendors Available in Chip Form	DA too High for More than 8-Bit Applications
Polystyrene	0.001% to 0.02%	Inexpensive Low DA Available Wide Range of Values Good Stability	Destroyed by Temperature $>+85^{\circ}C$ Large Case Size Not Available in Chip Form
Polypropylene	0.001% to 0.02%	Inexpensive Low DA Available Wide Range of Values	Destroyed by Temperature $>+105^{\circ}C$ Large Case Size
Teflon	0.003% to 0.02%	Low DA Available Good Stability Operational Above $+125^{\circ}C$ Wide Range of Values	Relatively Expensive Large Not Available in Chip Form
MOS	0.01%	Good DA Small Operational Above $+125^{\circ}C$ Available in Chip Form	Limited Availability Available only in Small Capacitance Values
Polycarbonate	0.1%	Good Stability Low Cost Wide Temperature Range	Large Not Available in Chip Form DA Limits to 8-Bit Applications
Polysulfone	0.1%	Good Stability Low Cost Wide Temperature Range	Large Not Available in Chip Form DA Limits to 8-Bit Applications

TABLE 5.2.1.2.3-2: CAPACITORS FOR SWITCHED DATA APPLICATIONS

TABLE 5.2.1.2.3-3

TEMPERATURE CONSIDERATIONS IN PRECISION RESISTORS

1. CLOSELY MATCHED TEMPERATURE COEFFICIENTS
2. LOW ABSOLUTE TEMPERATURE COEFFICIENTS
3. LOW THERMAL RESISTANCE
   (HIGHER POWER RATING - LARGER CASE)
4. LOW VOLTAGE COEFFICIENT OF RESISTANCE
5. TIGHT THERMAL COUPLING OF MATCHED RESISTORS
   (ONE PACKAGE - RESISTOR NETWORK)



MOUNTING TECHNIQUES FOR RESISTORS

FIGURE 5.2.1.2.3-3

tion systems where many channels with widely varying data are being sampled for A/D conversion by a sample-and-hold device prior to conversion. The only solution is to use a capacitor with a dielectric absorption less than the maximum tolerable error. Section 5.2.4 of the Handbook discusses the attributes of various types of capacitors.

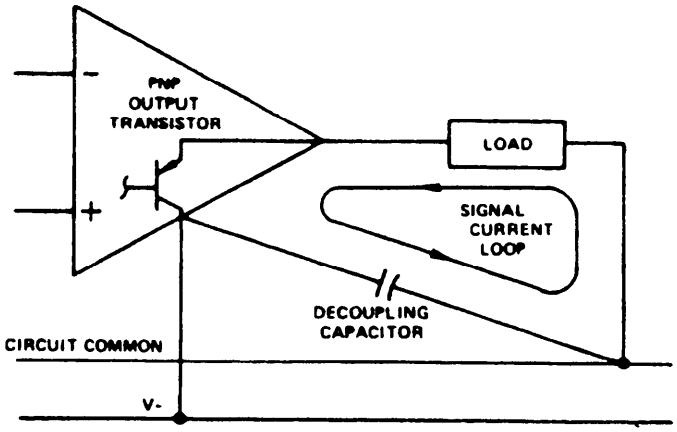
o Decoupling and Grounding - The source of much woe in linear designs is often careless handling of grounds and power supply distribution. The first rule of arranging grounds and power distribution is to begin considering "ground" and "power" connections as the resistors and inductors they really are. Consider the path through which signal current must flow in an op amp circuit. Current must flow from the power supply to the op amp, through the op amp, through the load, through the "ground" leads, and eventually back to the power supply. It is the voltage drops caused by the current flowing in the supply leads and ground impedances which can create havoc in a system. The traditional solution is "decoupling," a term only slightly less vague than "ground." Proper supply decoupling involves more than simply scattering capacitors around a circuit diagram.

Consider the case where an op amp drives a load which connects to a long ground line (returning to a power supply terminal). Here, the return path for load current is as long as or longer than the power supply lines powering the op amp. In this situation, the most effective decoupling occurs if the decoupling connects by the shortest path between the load and the load voltage control element. Figure 5.2.1.2.3-4 gives an example of proper decoupling in this situation. Here, an op amp swinging a resistive load circuit negative typically drives the load from an internal PNP transistor connected to V-. Decoupling the V- pin of the op amp to the low side of the load provides the most direct return path for high frequency currents and bypasses them around ground and power busses.

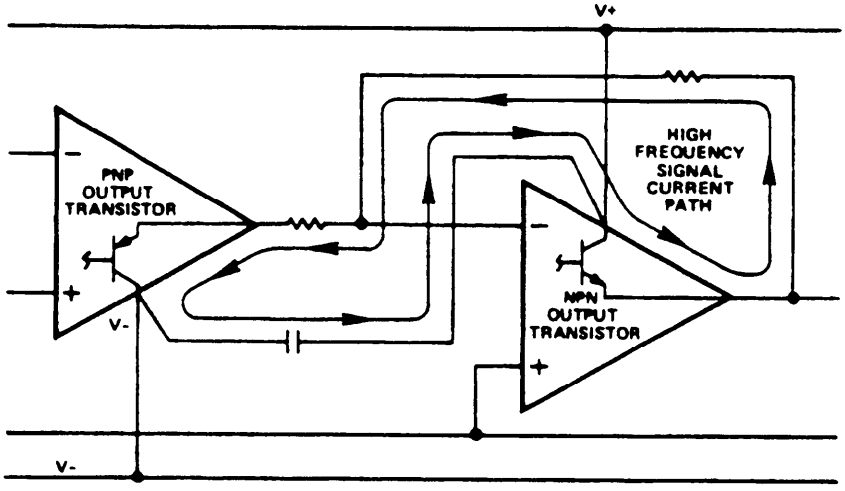
However, if the amplifier is driving a load that goes to a virtual ground, the actual load current does not return to ground. Rather, it must be supplied by the amplifier creating the virtual ground as shown in Figure 5.2.1.2.3-5. In this case, decoupling the negative supply of the first amplifier to the positive supply of the second amplifier closes the fast signal current loop without disturbing ground or signal paths.

In reality, most op amps are indeed more sensitive to transients on one supply line than the other. Thus far the examples have concentrated on decoupling techniques for negative power supply. For amplifiers where the integration is referred to the positive supply, decoupling of the positive supply should be considered.

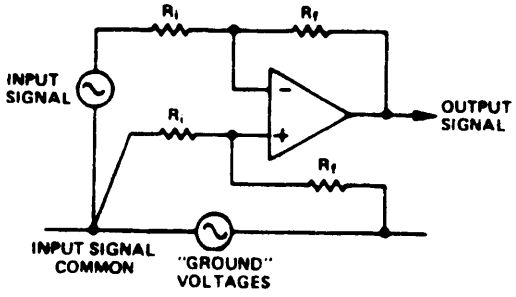
Ground in most electronic equipment is not an actual earth ground connection, but rather a common connection to which signals and power are referred. "Common" is a much better term for this connection, and implies that this point must be made common. Recognizing that the impedance of ground interconnections will have voltages across them when currents flow through them is important to avoiding ground errors. Figure 5.2.1.2.3-6 gives an example of a subtractor amplifier which can be used to reject errors due to grounding problems.



DECOUPLING NEGATIVE SUPPLY
OPTIMIZED FOR "GROUNDED" LOAD
FIGURE 5.2.1.2.3-4



DECOUPLING NEGATIVE SUPPLY
OPTIMIZED FOR "VIRTUAL GROUND" LOAD
FIGURE 5.2.1.2.3-5



SUBTRACTOR AMPLIFIER ELIMINATES GROUND PROBLEMS
FIGURE 5.2.1.2.3-6

o Printed Circuit Boards - Printed circuit boards are the "unseen components" in all precision circuit designs. Since the electrical characteristics of PC boards are rarely designed into a circuit, the overall effect can be harmful to performance. Some advantages of PC boards are shown in Table 5.2.1.2.3-4. PC circuit boards provide the advantage of reducing noise pickup. The ability to apply shields and guards can be even more effective in improving circuit performance. Placement of a guard track can preserve the high frequency response of a buffer amplifier by minimizing the differential voltage across parasitic impedances. Ground planes and shields can be used to control capacitance on lines, reduce crosstalk and shield from noise.

On the negative side, the two dimensional nature of PC boards can become a barrier to proper circuit performance. Conductors that carry small, high precision or fast signals, or connect to high impedance terminations can cause problems in PC circuits by exposing those signals to parasitic resistances, capacitances or dielectric absorption. The effects of all of these parasitics would be the same as that of "real" components of the same type. Also, since PC material is hygroscopic, changes in humidity may cause the contributions of these parasitics to vary.

Table 5.2.1.2.3-5 gives some typical applications where printed circuit board effects should be considered. In Table 5.2.1.2.3-6 some printed circuit board application aids are presented.

5.2.1.2.4 POWER DISSIPATION IN ICS

The maximum allowable power dissipation "P_D" for an IC is a function of the maximum rated junction temperature "T_J," the maximum application case temperature "T_C" and the junction to case thermal resistance θ_{JC} (^{o}C/watt). The basic relationship is:

$$P_D = \frac{T_J - T_C}{\theta_{JC}}$$

IC data sheets do not necessarily list all of these parameters. It is quite common to list only the maximum power dissipation for a given ambient temperature and a maximum power decrease for a given increase in temperature.

For example, a typical IC might show a maximum power dissipation of 110 mW at 25^{o}C, with a power derating of 1 mW/^{o}C for each ^{o}C above 25^{o}C. If this IC is operated at 100^{o}C, the maximum power dissipation would be: (110 mW - ((100^{o}C-25^{o}C) (1 mW/^{o}C)) = 35 mW.

In the absence of specific data sheet information, the following typical temperature characteristics for typical environments can be applied to the basic IC package types (reference Section 5.1.2.5 of MIL-HDBK-217D):

OPPORTUNITIES	PITFALLS
Ground planes Shields and Guards Close Proximity of Components	Leakage Resistances Dielectric Absorption Hygroscopicity Two Dimensional Layout (Less Flexible) Stray Capacitances "Hook" (Capacitance Varies with Frequency)

TABLE 5.2.1.2.3-4
PRINTED CIRCUIT BOARD
ELECTRICAL OPPORTUNITIES AND PITFALLS

Electrometer Amplifiers Instrumentation Amplifiers Many Varied Signals Present 12-Bit Accuracy Required High Impedances RF or Fast-Rising Signals	Fast Settling Required High Noise Environment High Humidity Impulse Response is Critical Low Capacitance Circuitry

TABLE 5.2.1.2.3-5
TYPICAL APPLICATIONS REQUIRING CAREFUL
PRINTED CIRCUIT TECHNIQUES

Improved PC Material (Teflon has low D.A., is highly moisture resistant, is stable over temperature)	Guards for conductors with sensitive signals
	Low impedance designs where possible
Qualify vendors and institute controls	Breadboard must work better than required, operation must be fully understood
Bake the PC board to assure complete curing	Conformal coating-Beware! D.A. may cancel moisture resistance benefits
Critical conductors and components on Telfon standoffs and sockets.	Sensitive signals physically separated from digital logic
Ground planes and shields	Think like an Electron-follow every track

TABLE 5.2.1.2.3-6
PRINTED CIRCUIT BOARD
APPLICATION AIDS

If T_C cannot be determined, use the following:

ENVIRO.	G_B	S_F	G_F	N_{SB}	N_S	M_P	G_M	M_{FF}	A_{IT}	M_{FA}
T_C(°C)	35	40	45	45	45	40	50	60	60	50

If θ_{JC} cannot be determined, use the following:

Package Type	Die Attach*	Number of Package Pins	
		≤ 22 pins	> 22 pins
Hermetic DIPs or Chip Carriers	Eutectic Epoxy or Glass	30 125	25 100
Nonhermetic DIPS or Chip Carriers	Eutectic Epoxy or Glass	30 125	25 100
Hermetic Flatpacks	Eutectic Epoxy or Glass	40 125	35 100
Hermetic Cans	Eutectic Epoxy or Glass	30 125	NA NA

*If the die attach method cannot be determined, assume that epoxy die attach is used for hermetically packaged CMOS and eutectic die attach for all other hermetic packages.

o Maximum Power Dissipation. This term refers to the absolute maximum power a device can dissipate when used at a given temperature (usually 25°C), maximum power supply voltages, input signals and maximum output loads. As the ambient temperature of the environment increases the maximum power dissipation capability of a given device decreases. During any design the maximum power dissipation limit of a device should be avoided. Recommended derating procedures for electronic devices over various environments are given in the sections where a particular device type application is given.

o Thermal Resistance. The thermal resistance (θ_{JC}) of a semiconductor device is a measure of the ability of its carrier or package and mounting technique to provide for heat removal from the semiconductor junction. θ_{JC} is defined in MIL-HDBK-217 as the junction to case thermal resistance (°C/watt) for a device soldered into a printed circuit board.

o Operating ICs With or Without Heat Sinks. In general, 1 watt is the maximum power dissipation for an IC operating without a heat sink. After about 1 watt it becomes impractical to increase the size of the case to make the case-to-ambient air thermal resistance term comparable to the junction-to-case term.

Therefore, it may become necessary to use heat sinks to aid in the heat dissipation from the IC device. Listed below are some practical guides to be used when heat sinks are required:

(a) Use large areas to minimize thermal resistance.

(b) Do not mount parts so that the only conduction path to the heat sink is through the leads.

(c) Mount high power parts cooled by free convections and radiation or by impingment cooling on heat transfer finds.

(d) Do not use tightly spaced fins for free convection cooling. Do not use more than four fins per inch, and do not use higher than one inch.

(e) Maximize the areas of all conduction paths and interfaces between the parts and the sink.

(f) For maximum electrical insulation and minimum thermal resistance use mica, beryllium oxide or anodized aluminum insulators with typical °C/W ratings of 0.4, 0.25, and 0.35, respectively. NOTE: Packages containing beryllia shall not be ground, sand blasted, machined or have other operations performed on them which will produce beryllia or beryllium dust. Furthermore, beryllium oxide packages shall not be placed in acids that will produce fumes containing beryllium. Normal safety precautions for handing beryllium oxide shall be based on OSHA procedures for beryllium oxide materials.

(g) Use zinc oxide filled silicon compound between the washer and chassis to decrease thermal resistances.

(h) Use of a washer between IC case and heat sink introduces capacitance to the circuit. In general, capacitance is low and will have no effect on operation of IC's unless the frequency is above 100 MHZ. In such cases the capacitance effect should be considered in the design.

o Effects of Temperature Extremes on ICs. The effects of temperature extremes (either high or low) will vary with the type of IC involved, case style, fabrication techniques and device technology. The following general rules can be applied to most ICs:

(a) In general, high temperatures cause the IC characteristics to change. An increased operating temperature also produces increased leakage currents, increased sensitivity to noise, increased unbalance in balanced circuits, increased "switching spikes" or transient voltages for transistors in digital ICs, and an increase in the failure rate.

(b) Many of the degradation and/or failure mechanisms in ICs are temperature dependent. Common examples are corrosion, diffusion and most chemical reactions. High temperatures accelerate these mechanisms, thereby reducing the reliability of the parts.

(c) If the power supply voltages, input signals, output loads, and ambient temperatures specified on the data sheet are observed, there should be no danger of exceeding the maximum rated junction temperature. However, a thermal analysis over the system environmental stresses and the mounting should be made to assure reliable operation.

5.2.1.3 APPLICATION NOTES FOR COMMONLY USED LINEAR ICS

o Operational Amplifiers. Operational amplifiers, or op amps, are the basic building blocks of nearly all linear circuits. In most circuit applications op amps behave as nearly ideal amplifiers, with infinite gain and input impedance, zero output impedance and unlimited frequency response. In fact, the extreme versatility of these devices contribute to the designer's problems, since most poor designs are a result of assuming ideal amplifier response in operating conditions where ideal behavior is not a good approximation. A common example of this is a slew rate problem, wherein the output signal is distorted due to frequency limitations of the op amp.

For applications requiring special device characteristics, there are a number of high performance amplifiers available offering wide band frequency response, high input impedance (i.e., FET-input amplifiers) improved power handling capabilities, etc. In addition, op amps are available in multiple configurations, especially duals and quads (2 and 4 op amps per package, respectively). The reliability trade offs of duals and quads must be carefully weighed, with reliability performance depending primarily on application.

Multiple amplifier packages reduce package count, size, and weight by combining 2 to 4 separate circuits in a single package. This is usually done by integrating multiple op amps on a single silicon chip. While reducing parts count, solder connections and PC board space, and the reliability hazards associated with them, it is important to note that there is now a common mode hazard: certain failure modes could destroy the entire package, with a resultant loss of four circuits instead of just one. For this reason, duals and quads should not be used for parallel redundancy.

On the other hand for a series configuration where the output of one op amp feeds the input of the next a multiple amp circuit would be acceptable, since the function is lost whether one amp fails or whether all the amps in the series fail.

o Voltage Comparator. A voltage comparator is basically a high gain amplifier designed for comparison measurements. Its output is fixed at one level when an input voltage exceeds a given reference voltage and another limit when the input voltage is less than the reference voltage. It is normally designed for open loop operation.

An op amp can be used for a comparator; however, its response time is often too slow for many applications. For this reason, many ICs are available for this specific function.

o Voltage Follower. A voltage follower is an amplifier optimized to buffer voltage sources from their loads. An op amp in a voltage follower configuration is given in Figure 5.2.1.3-1.

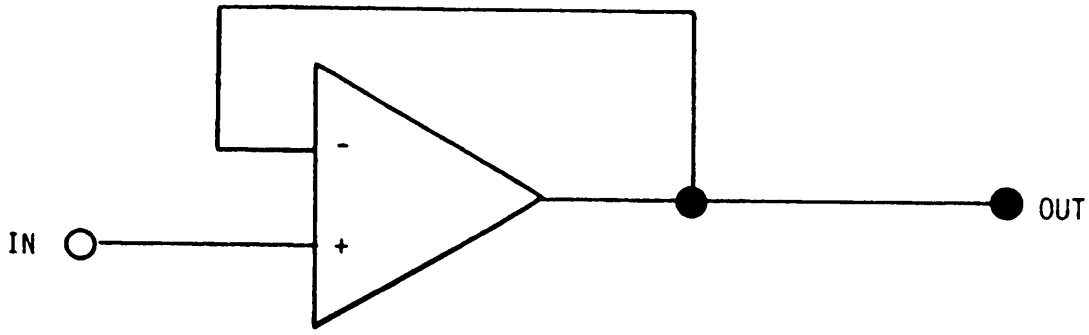


FIGURE 5.2.1.3-1 VOLTAGE FOLLOWER CIRCUIT

Here, the entire output voltage is fed to the inverting input of the op amp, assuring a gain of 1 while providing a high impedance for the input voltage and a low impedance for the output. Here again, as in the voltage comparator, general use op amps are usually not the best devices to use in many applications requiring a voltage follower. They are usually too slow since voltage followers often require maximum frequency compensation.

Also, when designing a voltage follower amplifier, many of the problems of op amps (used as voltage followers) can be overcome. For example, since the high gain stages normally associated with op amps are not needed in followers, the complimentary transistors can be done away with, making a faster device and increasing the slew rate.

o Current Amplifier. It sometimes becomes necessary when driving a low impedance line to increase the circuit's current driving capability. For example, if an op amp is not capable of driving the next stage of a system, a current amp could be used. One configuration to achieve a higher current capability is to use the current amp in the feedback loop of the op amp as in Figure 5.2.1.3-2.

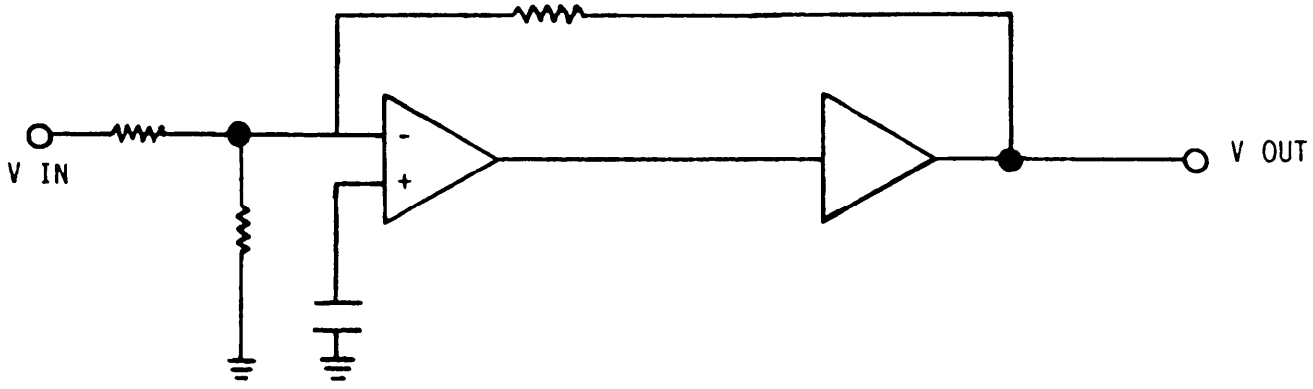


FIGURE 5.2.1.3-2

o Line Drivers. Linear line drivers are devices which must exhibit high capacitance drive capability since they are often required to drive a signal into a coaxial cable or shielded cable which generally have a high capacitance per unit length associated with them. Provisions are usually made when using these devices to adjust them (externally) to a particular driving load (since maximum power transfer is obtained when the output impedance of the amplifier is matched to the load). The need for a high capacitance drive capability stems from the fact that the circuit must actually "charge up" the line. It is also for this reason that these drive amplifiers must have a relatively high current drive capability.

o Line Receivers. A line receiver is basically a differential comparator op amp. This is a good application for the differential amp because the noise picked up on the transmission line (if it is a twisted pair) is predominantly a common mode signal, meaning the noise and interference picked up on the two lines of the pair is the same, whereas the signal is not common mode. This type of line receiver acts to delete any signal that is common to both lines, thus effectively extracting the signal from the noise.

o Sense Amps. Sense amps are used to detect low level signals. These amps can have input sensitivities as low as ± 10 mV and often have differential inputs, allowing them to reject common mode signals, thereby increasing the effective sensitivity.

o Analog Switches and Multiplexers. Since the advent of integrated circuits, the requirements of complex circuits are such that electromechanical switches are often not adequate and semiconductor switches are a good alternative. Because the life of a semiconductor switch is not limited by mechanical wear (as electromechanical devices are) the reliability is often better than the electromechanical type. They also exhibit higher reliability in adverse environments (shock vibration, temperature, pressure, etc.). They are, however, subject to reliability problems that mechanical devices are not, such as radiation, electrical overstress from transients, and noise sensitivity on the input(s). The ON and OFF resistances of field effect transistors make them an ideal choice for use in semiconductor switching.

There are three basic types of FET switches: JFET, MOSFET, and CMOS. The JFET type (P or N channel) is a depletion mode device and hence needs a VGS of near 0 volts to maintain the transistor in the ON state. In this type of switch, the ON resistance VDS (ON) stays at a constant value for all d.c. levels of analog input signal. In the MOSFET (P or N channel) switch the gate is held at a reference voltage which keeps the voltage above the threshold voltage for all values of analog input. The resistance VDS (ON) of the MOSFET type switches vary as the input voltage varies. This variation can cause a distortion of the analog input if the load resistance is small or comparable to the VDS.

The CMOS switch is effectively a parallelled N and P channel MOS device, thereby keeping the ON resistance relatively constant over the range of analog input voltages.

Each of these types of switches requires a driver circuit which can be either bipolar or FET.

o Multiplexers. In systems in which many analog signals must be handled, it is sometimes practical to sample them periodically rather than continuously. Any system which otherwise would require long multiconductor cables for transmission of information is a candidate for multiplexing. There are basically two types of multiplexing: time domain multiplexing and frequency domain multiplexing. Frequency domain multiplexing is a situation where one signal carries the information of more than one channel by modulating them in different manners.

An example of this is FM broadcasting, where two signals are decoded by means of using a subcarrier signal. This type of multiplexing is most common in RF communications. It does become difficult to implement, however, when there is a large number of data channels.

The other type of multiplexing, time domain multiplexing, is accomplished by allowing each data line a certain "time slot." This time slot duration and frequency is determined by the clock rate and the number of data lines to be multiplexed. The clock rate which controls the sampling of the analog inputs is limited by the speed of the analog switches used. Normally the channel selection is accomplished by means of a binary control signal.

o Sample and Hold. The sample and hold circuit is used when a signal must be instantaneously monitored and held for processing. A simple circuit which accomplishes this is given in Figure 5.2.1.3-3.

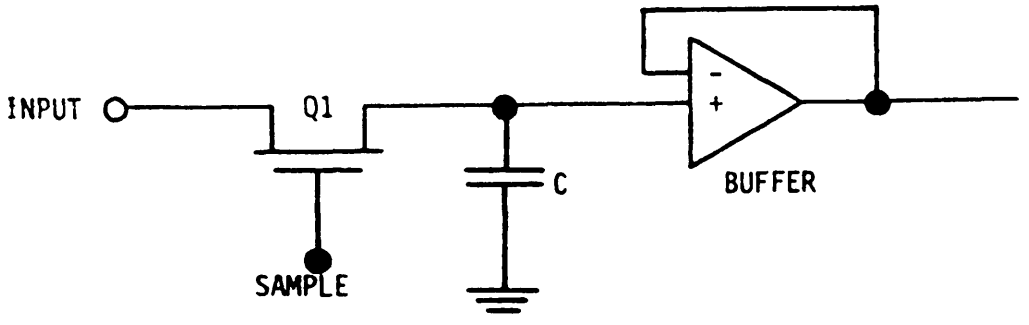


FIGURE 5.2.1.3-3

It uses the energy storage capability of the capacitor (C) as the storage element. The field effect transistor (Q1) is used as a switch here. When the sample signal is negative, effectively turning the switch on, the capacitor is charged to the instantaneous voltage of the input. When the sampling signal turns Q1 off, the resistance of the switch is very high, and since the input resistance of the buffer amplifier is also very high, the capacitor will hold the voltage obtained during sampling almost indefinitely, and the output of the amplifier is the same as that of the instantaneously obtained voltage (assuming a buffer gain of 1).

o Voltage Regulators. There are three basic types of voltage regulators: fixed, variable, and switching. Fixed voltage regulators are the most widely used. An advantage of the adjustable regulator is the fact that one specific regulator type can be used in many applications, thereby possibly reducing the list of standard parts. Operationally, adjustable and fixed regulators are very similar, and each is available in packages capable of handling several amps. Both of these regulators have fast response to load transients and low noise and ripple. There is an inherent disadvantage, however, since they are "dissipating type" regulators in that they must dissipate the difference in power between the unregulated input and the regulated output. The consequence of this dissipation is that the regulator is of low efficiency and normally operates at a higher temperature than other components in a system. Because of this, care must be taken by the designer to insure the regulator is not placed near temperature sensitive components.

These devices are available for regulating both positive and negative voltages. The basic regulator circuit uses an op amp to monitor and regulate the output voltage in a negative feedback loop. The basic circuit for this type of device is given in Figure 5.2.1.3-4 (positive voltage regulator).

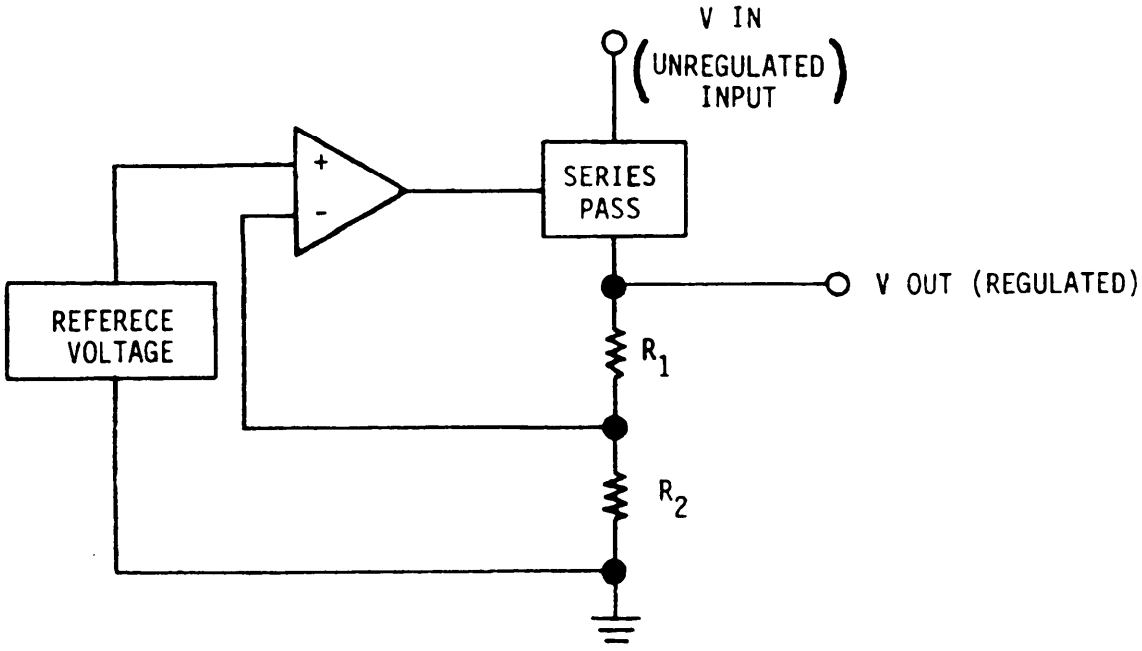


FIGURE 5.2.1.3-4

The op amp (used here as a differential amp) continuously compares a fraction of the output voltage:

$$\left((V_{out}) \left(\frac{R_2}{R_1 + R_2} \right) \right)$$

with the reference voltage and adjusts its output accordingly to achieve the desired Vout. Therefore, the output is adjustable by adjusting the external resistors R1 and R2. The series pass network is generally a transistor whose base emitter junction is forward biased in normal operation. In this circuit it is required that the Vin (unregulated voltage) be a minimum of 3V above the desired Vout since the unregulated voltage is required by the differential amp and the series pass transistor. The reference voltage is normally a temperature compensated avalanche diode whose voltage is divided for input into the differential amp. Fixed voltage regulators can achieve typical line regulations of 0.05% per volt at several amps. The output power can be further increased with the addition of external power transistors.

The single most dominant failure mechanism in this type of regulator is "burnout" due to excessive power dissipation by the series pass transistor.

o Switching Voltage Regulators. To overcome the problem of excessive power dissipation, a switching regulator may be employed. This type of regulator normally employs a circuit similar to the dissipating type of regulator with some modifications. It uses the pulse width modulation principle, which essentially means that the voltage to the load is regulated by adjusting the pulse width (of a given voltage) into an inductor. This controls the average output voltage which is then filtered by the LC circuit. Since the switching frequency is relatively high (20 KHz to 100 KHz), the capacitor and inductors needed are relatively small. Also, since there are no resistances in the circuit the theoretical power dissipation is 0. Practical efficiencies of 90% can be realized using a switching regulator. Advantages of using this type of regulator include a very low power dissipation and hence reduced size per watt output. When properly designed these regulators can reliably regulate large amounts of power. The disadvantages are that since the switching rate is high (and hence the slew rate of the voltage) stray capacitance and inductive coupling can pick up noise and/or voltage transients in other parts of a circuit. This problem is compounded by the fact that a square wave has harmonics much higher than the fundamental frequency. For these reasons, shielding is often required. Another drawback in using this type of regulator is that a failed switching transistor can cause catastrophic failure (since it is in series with the input and the output of the regulator). Therefore protective circuitry on the input and output may be a desirable precaution. Also, a switching regulator does not adjust as fast to rapid load changes as a linear type (dissipating type), thereby making it less desirable when the load current contains fast pulses.

o Voltage References. Voltage references provide a stable, precise reference voltage ideal for use with A/D and D/A converters, calibration standards, precision voltage or current sources or precision power supplies. Voltage references are stable over a wide temperature range with

very low noise as compared to voltage regulators. In spite of these features, it is important to isolate the reference from thermal excursions and electrical noise if maximum stability is to be realized. The reference should not be placed in direct air flow from a cooling fan for example. Due to the nature of these devices, they may be vulnerable to damage from either line transients or electrostatic discharges (ESD). Precautions should be taken as necessary to prevent damage to the device from these effects. To minimize loading of the reference, the output should be buffered with an op amp or similar device.

o Digital to Analog Converters. Digital to analog converters are devices which convert a digitally encoded signal to the corresponding analog voltage. D/A converters serve as a primary means of interfacing digital processing units with sensors and actuators used to implement control functions. They provide the means for generating analog signals under digital software control.

D/A converters are most commonly implemented by means of a resistor R-2R ladder network as in Figure 5.2.1.3-5.

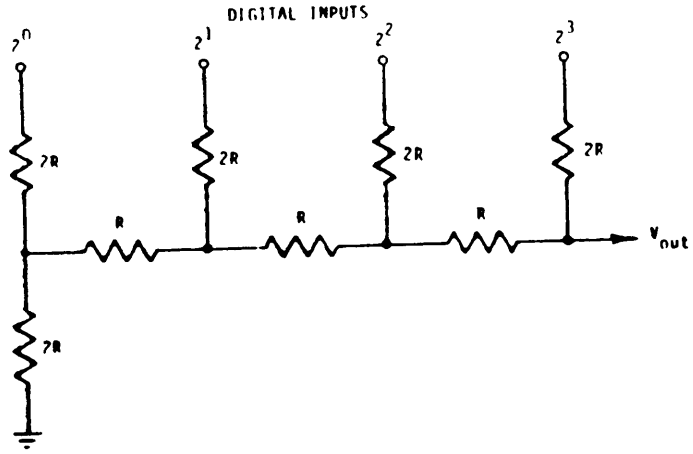


FIGURE 5.2.1.3-5: D/A CONVERTER IMPLEMENTED USING R-2R RESISTOR LADDER NETWORK

The configuration of the preceding ladder network is such that a binary coded digital signal at the inputs will provide the proper analog current Io at the output. Most D/As have a current output (usually 2mA full scale) which allows logic voltage compatibility for many systems. The designer may choose his logic levels.

o Weighted Resistor D/A Conversion. An alternative to the ladder network for D/A conversion is the weighted resistor network shown in Figure 5.2.1.3-6.

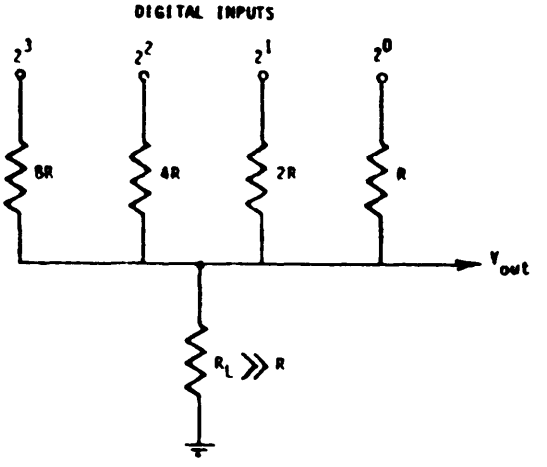


FIGURE 5.2.1.3-6: WEIGHTED RESISTOR NETWORK

As before, the appropriate binary input signal will provide the proper analog output current Io. While this approach uses fewer resistors, its disadvantages are the unequal current (and power) loads of various resistors and the need for precision resistors for minimizing nonlinearities. As a result, the ladder network is the preferred technique for most applications.

o Analog to Digital Converters. A/D converters are commonly used data acquisition devices which convert analog voltage signals to digital signals to permit processing by digital computers. Several A/D conversion algorithms are available, offering various degrees of conversion speed, accuracy and component cost.

(a) Ramp Conversion. The ramp type A/D conversion method matches the unknown voltage to a steadily increasing ramp voltage. The ramp voltage is internally generated by means of a digital counter and a digital-to-analog (D/A) converter. When the unknown voltage is matched to the ramp voltage the digital signal which generated the ramp is fed to the output. While conceptually simple and easy to implement, this conversion algorithm is relatively slow, taking on the average 2^{n-1} increments of the counter to match the signal on an n-bit converter.

(b) Successive Approximation. The successive approximation algorithm (the preferred procedure in military applications) performs tests based on the weight of each binary bit position, going from the most significant bit (MSB) to the least significant bit (LSB). Beginning with the MSB, the bit weight is compared to the unknown voltage; if the unknown voltage is greater than the running sum, the bit weight is added to a running sum. If the unknown voltage is less than the running sum, the bit weight is not added to the sum. The algorithm steps through from MSB to LSB, so that at the end of the LSB, the value of the running sum is equal to the unknown voltage. Table 5.2.1.3-1 demonstrates this algorithm for an 8-bit A/D converter and the number 147.

TABLE 5.2.1.3-7 A/D CONVERSION OF THE NUMBER 147

Test Bit Weight	Response	Sum
128	Too low, add to sum	128
64	Sum of 128 + 64 too high, do not add	128
32	Sum of 128 + 32 still too high, do not add	128
16	128 + 16 < 147, add to sum	144
8	144 + 8 too high, do not add	144
4	144 + 4 too high, do not add	144
2	144 + 2 too low, add to sum	146
1	144 = 1 just right, add to sum	147

It can be seen that this conversion algorithm accomplished the conversion in n-steps for an n-bit converter. In the above example, the number 147 was converted in 8 steps using successive approximation, as opposed to 147 steps using the ramp method.

(c) "Flash" A/D Conversion. The flash method of A/D conversion is a parallel scheme in that all bits are computed simultaneously by means of parallel comparators with appropriate voltage references. A typical flash converter is shown in Figure 5.2.1.3-7.

The parallel processing feature offers ultra fast conversion times useful for video and radar applications. For an n-bit binary output, 2^n-1 comparators are required. This method requires a considerable amount of power.

(d) Dual Slope Method. A fourth approach to A/D conversion is the dual slope method, which indirectly measures voltage by converting it to a time period. The unknown voltage is integrated over a fixed period T1. At the end of this period, the integrators input is switched to a stable reference voltage with a polarity opposite that of the unknown voltage. This has the effect of subtracting from the sum integrated over T1. Since the reference potential is a constant, the slope of the integrators output will be constant, so that the time T2 required to discharge the sum in the integrator at the end of period T1 is related to the unknown voltage by:

$$E_{unknown} = \left(\frac{T_2}{T_1}\right) V_{ref}$$

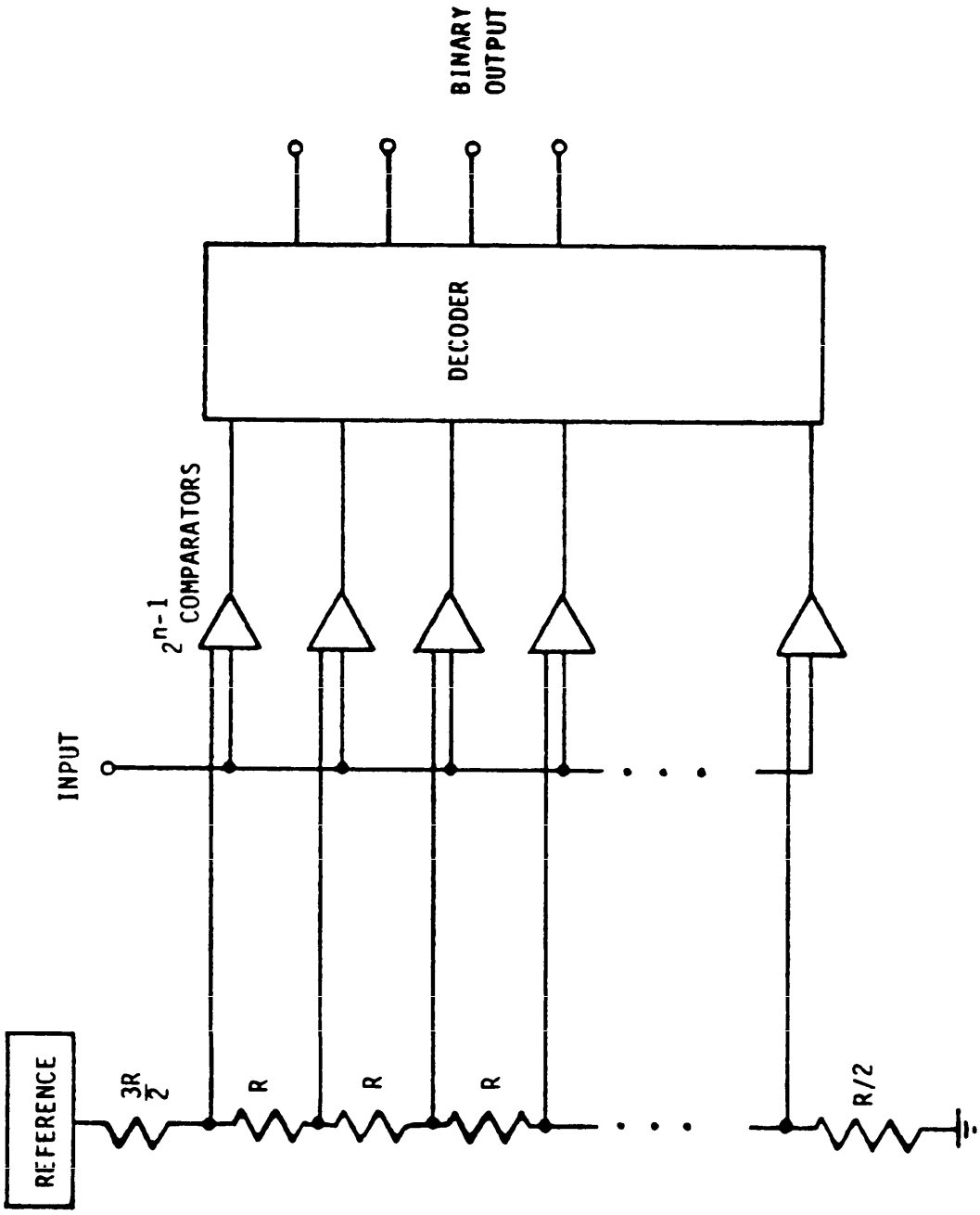


FIGURE 5.2.1.3-8 "FLASH" OR PARALLEL A/D CONVERTER

While this algorithm may be relatively slow, it has the advantage that the input is integrated over time T_1, so that noise pulses which are short compared to T_1 will be integrated and consequently averaged to zero. (Random noise has an average value of zero.) In addition, this method provides inherent monotonicity.

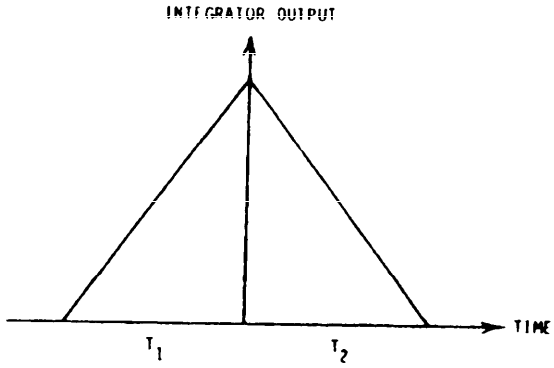


FIGURE 5.2.1.3- 9 DUAL-SLOPE INTEGRATION ALGORITHM

Figure 5.2.1.3-8 illustrates the integrator output as a function of time using the dual slope algorithm. Digital conversion is accomplished by gating a pulse generator during period T_2 so that the number of pulses passing to the counter is a function of the pulse rate and the time T_2. By appropriate selection of V_{ref} and the pulse rate, the output of the counter will be a digitally encoded measure of the input voltage. This conversion technique is commonly employed in digital panel meters and other applications where speed is not critical and the voltages to be measured may be noisy.

o Phase Locked Loop (PLL). The phase locked loop function has two distinctly different applications: (1) to produce an output voltage that varies with the frequency of the input voltage, essentially a frequency to voltage converter, and (2) to produce an output frequency which is exactly the same frequency as the input but without all the noise, distortion, or modulation that may be characteristic of the input signal. The block diagram of the phase locked loop is given in Figure 5.2.1.3-9.

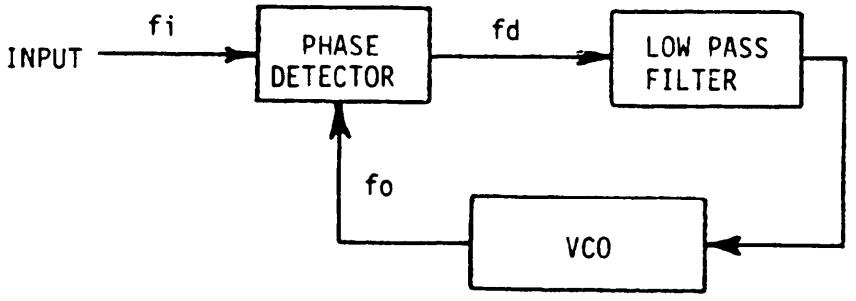


FIGURE 5.2.1.3-10 PHASE LOCK LOOP BLOCK DIAGRAM

The function of the phase detector is to produce an output which is proportional to the phase difference between the input and the output of the VCO (voltage controlled oscillator). Ideally, if $f_i = f_o$ (frequency of input and frequency of the output of the VCO, respectively), the output would be d.c. If there is a small difference between f_i and f_o, the output of the phase detector would be the beat frequency ($f_i - f_o$), and the instantaneous output is proportional to the instantaneous phase difference. Realistically, the output of the phase detector is a more complex function, since f_o is usually a square wave and harmonics are present. When the beat frequency ($f_i - f_o$) is low, it will pass through the low pass filter and into the VCO. The VCO is a device whose output frequency is directly proportional to the input voltage. Since the output of the phase detector is an a.c. signal the frequency of the output of the VCO is also varying in time. Therefore, when the output of the phase detector reaches the voltage such that the frequency of the VCO is the same as the input frequency ($f_i = f_o$), the phase locked loop will be locked. At this instant the output voltage of the filter will be able to maintain lock.

o Timers. The most universal IC timer available today is the 555. It is a general purpose device which can be used as a pulse generator, oscillator, ramp generator, frequency divider, pulse width modulated oscillator, or astable multivibrator. A simplified schematic of the circuit of a 555 timer is given in Figure 5.2.1.3-10.

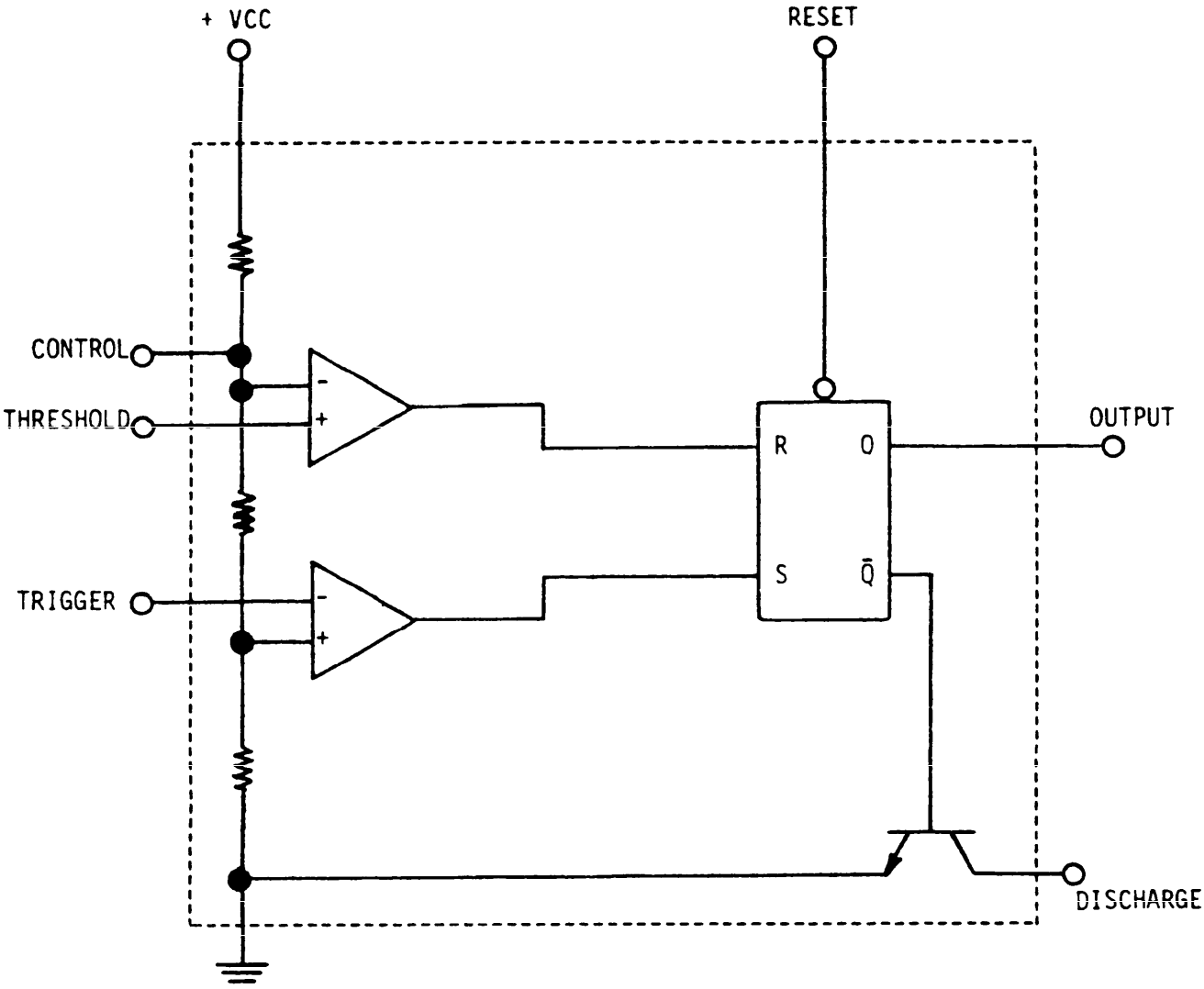


FIGURE 5.2.1.3-11 SIMPLIFIED SCHEMATIC OF 555 TIMER

A pair of comparators drives the inputs of an RS flip flop. Since the resistors used to divide the supply voltages for inputs into the comparators are equal in value, when the trigger input falls below 1/3 VCC, the comparator is driven high which in turn causes a high output. The trigger function can only be rearmed when the trigger input voltage is raised above 1/3 VCC. When the threshold voltage is raised above 2/3 VCC, the comparator is flipped, thus creating a low output. It also turns on the discharge transistor which is used to discharge the timing capacitor (external) at the end of a cycle. In many applications, the threshold input is connected to the timing capacitor (thereby resetting the device when the capacitor voltage falls below 2/3 VCC.) The two basic configurations of the 555 in which other circuits are based are the (1) triggered one shot and (2) free running oscillator.

The entire circuit is contained in a single monolithic package with two resistors and one capacitor being the only external components needed to adjust the timing interval. Dual timers (2 circuits on one chip) are also available.

5.2.1.4 APPLICATION DATA FOR COMMONLY USED DIGITAL MICROCIRCUITS.

This section will discuss some of the commonly used digital circuit functions that are available to the IC designer. In doing so, certain circuits were grouped together because of similarities in function or electrical attributes. Circuits will be classified as either sequential or combinational; gates are combinational.

Regardless of the type of circuit being considered in the implementation of a design, the prime and overridding consideration will be "Which logic family will be better able to provide the correct mix of attributes in terms of cost, power, speed and density?"

o The first group that will be discussed will be the standard logic gates, buffer/drivers and Schmitt triggers.

The standard gate is a logic device which operates on a two state principle of either open (1) or short (0) of the input voltage. This particular principle lends itself to the implementation of Boolean Algebra and therefore the use of SOP (sum of product) and POS (product of sum) forms to aid in the design of a circuit function.

All the logic expressions that can be represented with Boolean Algebra can be implemented using AND gates, OR gates and inverters. AND gates are simply placed wherever two variables are multiplied together, and OR gates are placed wherever two variables are added. The resulting circuit is the hardware implementation of the given Boolean expression.

To optimize the selection of gates in a design a designer must minimize the number of bit literals in a Boolean expression and then implement the expression in POS or SOP form. For some logic expressions the SOP form is simpler and easier to implement. For other expressions, the POS form is preferable.

There is no prior way of knowing which form yields the simpler circuit. The wise designer develops both the SOP and POS expression before building the circuit. The implementation of the design will depend on which form (SOP or POS) requires fewer gates, the availability of the gates and the number of wires required.

If gate inputs are unused, they can be tied to used inputs on the same gate. This is the most popular way of handling unused gate inputs, but often leads to mistakes in determining fanout. The unused input can also use clamps and pull up resistors to tie the inputs to a logic 1. But these methods can not be used on OR or NOR gates, although unused OR and NOR inputs can be tied to ground.

o The second group of gates are those which are primarily used with transmission lines. These circuits will include buffer/drivers, receivers, transceivers and Schmitt triggers (which can be used as receivers).

Buffer/drivers differ from ordinary gates in that buffers have a large current sinking capability and a large fanout. They are used to drive many loads or loads that require high current.

Drivers are usually operated in the voltage mode in single ended systems to provide good noise immunity.

The drive current required is determined by the load impedance. It is desirable to drive a line with devices providing up to 100mA drive at TTL voltage levels and speeds. Single ended devices having this capability are of three basic configurations as shown in Figure 5.2.1.4-1.

A transceiver is simply a bidirectional driver. These gates when used in the driver mode, possess high current capability. They have high impedance in the receive mode to prevent loading down the line. Good bidirectional lines must be terminated in an open collector configuration (or 3-state).

The Schmitt trigger is a special type of NAND gate which can be used as a receiver for data transmission. The Schmitt trigger will not turn on unless the input voltage is greater than the positive going threshold voltage, and will not turn off unless the input voltage is less than the negative threshold voltage.

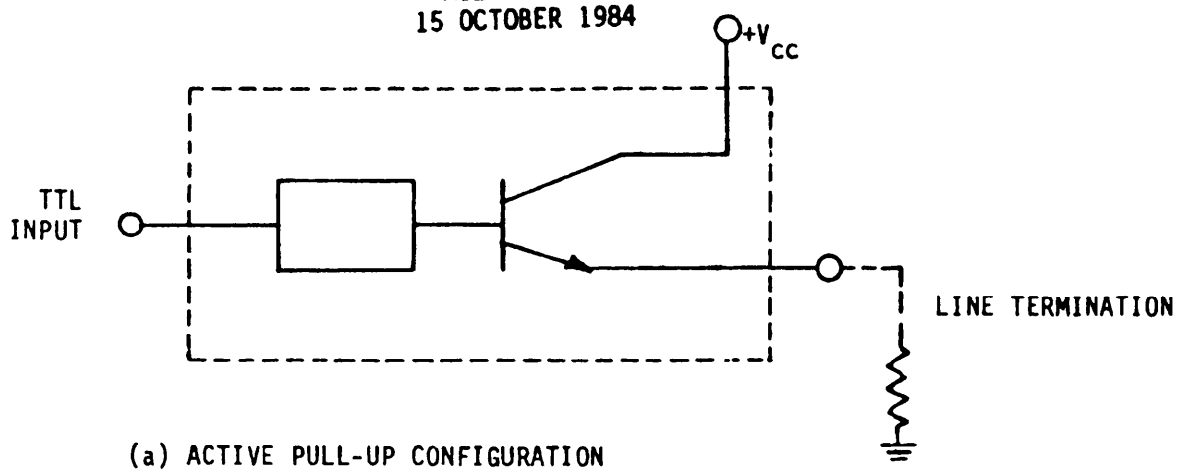
The positive going threshold voltage (V_{T+}) is greater than the negative going threshold voltage (V_{T-}). The difference between V_{T+} and V_{T-} is called hysteresis, and gives the Schmitt trigger the ability to square up slow and jagged waveforms. Sometimes a hysteresis symbol (⊓) is placed within the gate to distinguish a Schmitt trigger from a NAND gate.

Gates used for a single ended applications such as drivers and receivers are capable of high speeds (> 10 MHz), TTL compatable, require only one power supply and can operate from a common supply voltage. The disadvantages of these devices are that they have poor noise immunity, no common mode rejection, require short lines only (< 3 feet), have problems in driving low-Z lines, poor receiver sensitivity and little party line capability.

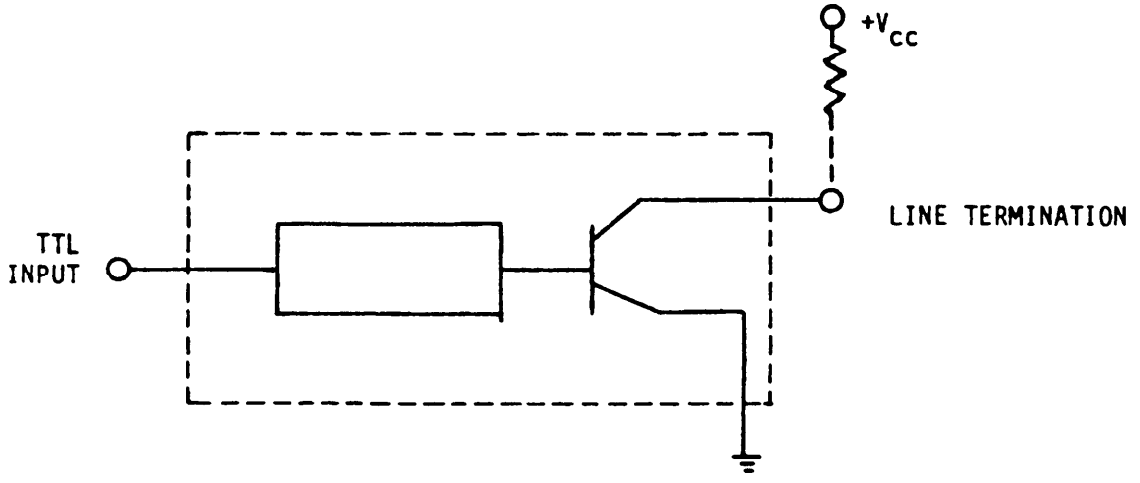
It can be seen that the disadvantages outweigh the advantage of using gates to perform a receiver or driver function in data line transmission.

o The next major group of circuits that will be discussed will be the multivibrators. Flip flops, shift registers, data registers and counters will be included in this discussion since these circuits are mainly composed of flip flops.

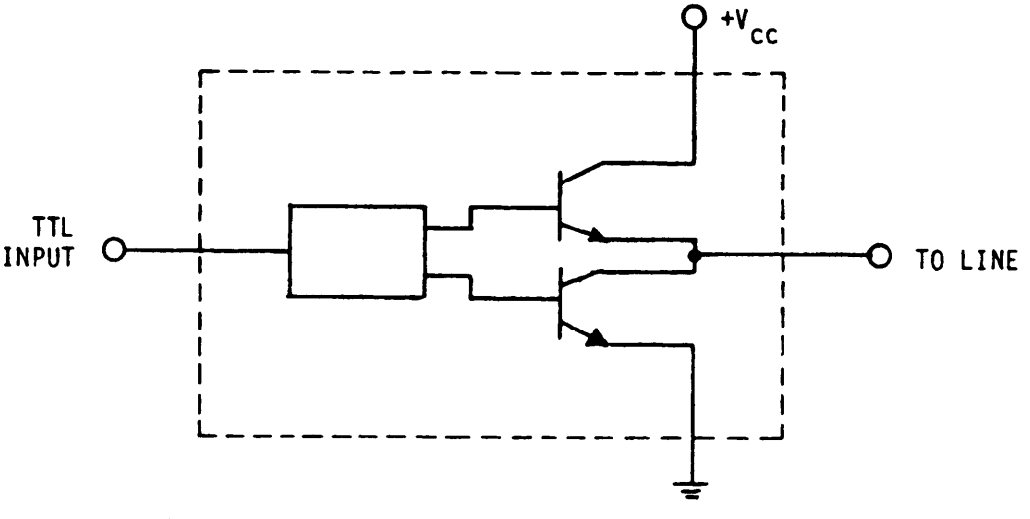
The flip flop (FF) is a sequential circuit which is capable of storing data or information. A simple FF is often described as a one bit memory. When



(a) ACTIVE PULL-UP CONFIGURATION



(b) ACTIVE PULL-DOWN CONFIGURATION



(c) TOTEM-POLE CONFIGURATION

FIGURE 5.2.1.4-1: BASIC CONFIGURATIONS OF SINGLE-ENDED DEVICES WITH DRIVE CAPABILITIES UP TO 100MA

both input are quiescent (neither SET nor RESET is active) the FF "remembers" which input was most recently active. If a SET signal was received last, the FF output will be SET (Q=1, $\overline{Q}$=0) and if a RESET signal was received last, the FF output will be RESET.

The internal circitry of most FFs is symmetrical, and when power is applied after the circuit has been turned OFF, there is no way of telling whether the FF will come ON in the SET or RESET state. Many sophisticated systems use a POWER-ON CLEAR signal, generated whenever power is first applied, to clear all critical FFs before operation begins.

There are three basic types of flip flops: the latch, the D type, and the JK. The simplest type of flip flop is the latch which can use two cross coupled NOR or NAND gates. The latch or set/reset flip flop is the simplest form of binary storage element. The latch has two inputs, S and R, and two outputs Q and $\overline{Q}$. Applying the appropriate logic signal to either the S or R input will put the latch into one state or the other. The S input is used to set the flip flop. When a flip flop is set, it is said to be storing a binary 1. The R input is used to reset the flip flop. A reset flip flop is said to be storing a binary 0.

The D flip flop has two outputs that are used to determine its contents but, the "data" applied to the "D" input is delayed before appearing at the output by half of one clock cycle (hence the "D" meaning delayed). The input to the "D" flip flop works differently compared to that of the latch. The D is where you apply the data or bit to be stored. The T (enable) input line controls the flip flop. It determines whether the input data is recognized or ignored. If the T input line is high or binary 1 the data on the D line is stored in the flip flop. If the T line is low or binary 0, the D input line is not recognized. The D-type FF can operate as either an asynchronous or a synchronous flip flop.

The J-K flip flop is the most versatile type of binary storage element in common use. It can perform all of the functions of the RS and D type flip flop plus it can do several other things that these simple flip flops cannot. An integrated circuit J-K flip flop is really two flip flops in one. It usually consists of two latches, one feeding the other, with appropriate input gating on each. The arrangement is called a master-slave J-K flip flop. The master flip flop is the input circuit. Logic signals applied to the J-K flip flop set or reset this master latch. The slave flip flop is the latch from which the outputs are taken. The slave latch gets its input from the master latch. Both latches are controlled by a clock pulse. Since there are two places to store bits in a J-K flip flop, there can be times when both master and slave latches are identical or times they are complementary. But only one of these latches is responsible for indicating the state of the J-K flip flop.

Edge triggered J-K flip flop can be used where it is necessary to eliminate the problem of setting the master flip flop while the clock is high. They react to the J and K inputs only at the negative edge of the clock.

In addition, J-K flip flop with data lockout are available. Using data lockout, the data is stored in the master flip flop on the positive edge of the clock pulse and transferred to the output on the negative edge of the clock pulse.

One of the most common errors made by designers is their attempt to clock a flip flop too soon after the removal of a direct input. The time required between removal of a direct input and the successful application of a clock is not specified by the manufacturer, but experience has shown it to be between 10 and 30 ns. Inserting inverters may delay the clock long enough to allow the circuit to work, but this also depends upon the transition times of the inverters as well as the speed of the direct CLEAR.

A race condition can exist if a circuit output depends upon which of two nearly simultaneous inputs arrive at a point in the circuit first, or where there may not be enough time between the removal of one input and the arrival of another.

Circuits that contain race conditions are unreliable. If the same circuit is built several times or mass produced, the output of each circuit is liable to be different due to the varying speeds of the circuit components. What is worse the output of the same circuit may be different at different times.

Consequently, engineers devote considerable time and effort toward eliminating race conditions. A thorough examination of the specific circuit usually reveals a satisfactory way of controlling pulses so that races are eliminated. Only when all else fails should brute force techniques be used, such as cascaded inverters, to delay inputs.

TTL flip flops operate properly if all pulses applied to them are longer than 50 ns. For circuits which must be designed for higher speed, the following parameters are specified by the manufacturer and should be observed.

(1) f(max) - This is the highest frequency at which clock pulses may be applied to a flip flop and still maintain proper stable clocking. For a 7474 or a 74107, the minimum value of fmax is 15 MHz. The manufacturers state that typical 7474s and 74107s will toggle at 20 and 25 MHz rates, but they do not guarantee the flip flops will toggle faster than 15 MHz.

(2) t(setup) - This is the time a signal must be present on one terminal before an active transition occurs at another terminal. For a 7474, t(setup) is 20 nsec this means that the D input must be held constant for at least 20 ns before a positive clock edge to assure a reliable output.

(3) t(hold) - This is the time a signal must remain at a terminal after an active transition occurs. For a 7474, this is 5ns. The signal at the D input should be removed no sooner than 5 ns after the positive edge of the clock. There is zero hold time for most J-K flip flops.

(4) Clock high pulse width. This is the minimum time a clock must remain in its high state for reliable clocking.

(5) Clock low pulse width. This is the minimum time a clock must remain in its low state for reliable clocking.

(6) Preset or Clear Low. This is the minimum time a PRESET or CLEAR pulse must be low for reliable setting or clearing.

Registers are usually composed of a group of flip flops; that is, an n-bit register consists of n FFs. Very often no logic or arithmetic operations are performed on the bits in the register; the function of the register is simply to retain (store, data register) the word for a period of time.

Shift registers can be built from D-type flip flops by connecting the Q output of each stage to the D input of the next succeeding stage. Since the D input to each stage is the same as the Q output of the previous stage, data will be shifted one bit to the right on the positive edge of each clock pulse.

J-K flip flops can also be used to construct shift registers by connecting the Q and $\overline{Q}$ outputs of each stage to the J and K inputs of the succeeding stage. The information in the register shifts one stage to the right in each negative transition of the clock. Since the data is constant for the entire clock period, master-slave type problems are not encountered in a J-K shift register.

A binary counter is a sequential logic circuit made up of flip flops that is used to count the number of binary pulses applied to it. The pulses or logic level transitions to be counted are applied to the counter input. These pulses cause the flip flop in the counter to change state in such a way that the binary number stored in the flip flops is representative of the number of input pulses that have occurred. By observing the flip flop outputs you can determine how many pulses were applied to the input. A count-by-n circuit, which is capable of counting up to a specified number n, will require at least K flip flops, where $2^K = n$.

There are several different types of counters used in digital circuits. The most commonly used is the binary counter. This type of counter counts in the standard pure binary code. BCD counters which count in the standard 8421 BCD code are also widely used. Both up and down counters are available.

D-type FF can be used to design synchronous counters if one realizes that the Q outputs for the next state must be the same as the present state D inputs. Knowing the present state of the counter, and its desired next state is enough to construct the Karnaugh maps and design the circuitry for the D inputs.

Adders are very versatile cicuits which can be used in arithmetic units as well as being able to be used as comparators and counters, such as up/down counters.

The basic adder for binary numbers accept two n-bit binary numbers as input, and produces an N+1 bit binary number as the sum. Essentially it consists of a half-adder, n-1 full adder circuits, and the n+1 stage (the MSB) that only receives the carry from the nth stage.

The basic adder stage accepts inputs from the addend, augend and a carry in from the less significant stage. It generates a sum output and a carry output, which it sends to the next more significant (succeeding) stage. A half adder is simpler. It only accepts addend and augend inputs. Because it need not accept a carry in, it can be used for the least significant stage of an adder, where there is never a carry input.

A half adder circuit can be implemented by the use of two gates where an exclusive "OR" gate is used to generate the sum of the inputs and an "AND" gate is used to generate the carry output.

A full adder circuit can be implemented simply by the use of two half adders plus the addition of an "OR" gate. Since a carry can be generated from the addition of the two inputs or the addition of their sum and the carry, the two carry outputs are "ORed" together to produce a correct carry output that will feed the next most significant bit adder.

o A basic procedure for error detection and correction is to design a code in which each work contains more bits than are needed to represent all the symbols used in a data set. If a bit sequence is found that is not among those assigned to the data symbols, an error is known to have occurred.

One such commonly used error detection code is called the parity check. Suppose that 8 bits are used to represent data and that an additional bit is reserved as a check bit. A simple electronic circuit can determine whether an odd or even number of "1" bits is included in the 8 bit positions. If an even number exists, a 1 bit can be inserted in the check position. If an odd number of 1's exist, the check position contains a zero. As a result, all code words must contain an odd number of 1 bits. If a 9-bit sequence is found to contain an even number of 1's, an error can be presumed.

This parity error detection method does not ensure complete freedom from or knowledge about all possible error conditions. The parity technique assumes that an error will occur in only one bit position of a word. If parity errors occur in two bit positions, it is possible for the word to be transmitted incorrectly while no parity error will be indicated.

It is simple to correct any error in a stream of binary data: the value of any bit known to be erroneous is simply inverted. However, the technique described above does not identify which bit location contains the incorrect value.

The Hamming code was the first of many techniques for manipulating data streams so as to detect and correct errors. It depends on a clever interweaving of the data bit stream with another bit stream composed of the Hamming (or check, or parity) bits. The values of the Hamming bits are determined by the values of the data bits and their positions are fixed in relation to the data bit positions according to equations developed by Richard Hamming. Since the receiver knows how the transmitter does this, it can infer the existence of a bit error from any discrepancy between the Hamming and the data bits.

No longer an optional luxury, error detection and correction codes are becoming standard on most computer systems as hardware costs come down and system complexity goes up. Semiconductor memories particularly need the codes, being more prone to errors than the older magnetic core designs.

But now increased chip densities make the use of these codes even more critical. The denser memories are especially susceptible to single bit errors induced by alpha particles hitting the same conductor. As chip densities increase (64K and 256K) the computer makers are looking toward new schemes that go beyond the Hamming code to detect as many as 3 failing bits and correct up to 2-bit errors.

o The multiplier circuit is a complex circuit composed of a combinational circuit (an adder) and sequential circuits (shift register). A binary mutiplier uses a shift register as a multiplicand that shifts each time a clock pulse occurs and sends the number that was entered into the adder. Another shift register, the multiplier, shifts so that the LSB appears in the accumulator register as a clock pulse to transfer the information into the adder. The adder in turn adds both the accumulator register and the multiplicand register and sends the result back to the accumulator to be processed again and again until the multiplier register has processed the required binary value.

o Multiplexers, encoders, function generators, demultiplexers and decoders all are structured in the same format with the basic difference only between multiplexers and demultiplexers. For instance some IC chips can perform either a decoder function or a demultiplexer function depending on how the strobe line and the data select lines are connected.

The basic decoding circuit is an AND gate. The output of an AND gate is a binary 1 only if all inputs are a binary 1. By properly connecting the inputs on an AND gate to the source of the data, the presence of any binary number will be detected when the output is binary 1.

Demultiplexers take a single input line and route it to one of many output lines. They also require enough SELECT inputs to specify which one of n output lines is connected to the input line. Demultiplexers can be used as digital decoders. A digital decoder has 2^n outputs and accept n inputs. Only the output that corresponds to the binary number on the input lines is activated.

An encoder is a combinational logic circuit that accepts one or more inputs and generates a multi bit binary output code. Now if one evaluates the circuit structure and the intended application of the multiplexer the similarities between the two circuit types will be quite apparent. A multiplexer is a electronic circuit that is used to select and route anyone of a number of input signals to a single output. The inputs to a multiplexer are the several input lines, and the SELECT input determine which one of the input lines is connected to the output.

Besides providing a convenient means of selecting one of several inputs to be connected to its single output, a multiplexer has several special applications which make it even more useful. Besides the data selector application, multiplexers are also used to provide parallel-to-serial data, conversion, serial pattern generation and the simplified implementation of Boolean functions.

Functional generation can also be accomplished with the use of a multiplexer which greatly simplifies the implementation of Boolean functions in the sum-of-products form. The multiplexer circuit inherently implements the sum-of-products for all input combinations by use of the select lines. By connecting a binary 1 or binary 0 to the appropriate data inputs, the products desired in the output can be selected.

o The basic logic structure of the PLA consists of a programmable AND array whose outputs feed a programmable OR array. The designer has complete control over all inputs and outputs, which provides the ultimate flexibility for implementing logic functions.

The basic logic structure of the PAL or gate array consists of a programmable AND array whose outputs feed a fixed OR array. Listed below is a table summarizing the characteristics of the PROM, PLAs and PALs logic families.

	AND	OR	*Output Options
FPLA	Prog	Prog	TS, OC, Fusible Polarity
FPGA	Prog	None	TS, OC, Fusible Polarity
PMUX	Fix/Prog	Fixed	TS
PAL	Prog	Fixed	TS, Registered, Feedback, I/O

*TS = Tri State
OC = Open Collector

PALS come in the following basic configurations: PAL gate arrays are available in sizes from 10 x 8 (10 input terms, 8 output terms) to 16 x 2, with both active high and active low output configurations available. This wide variety of input/output formats allows the PAL to replace many different sized blocks of combinational logic with a single package.

PAL are manufactured using proven TTL Schottky bipolar TI-W fuse process used to make fusible link PROMs. An NPN emitter follower array forms the programmable AND array. PNP inputs provide high impedance inputs (0.25 MA MAX) to the array. All outputs are standard TTL drivers with internal active pull up transistors. Typical PAL propagation delay time is 25 ns.

High end members of the PAL family feature registered data outputs with registered feedback. Each product term is stored into a D-type output flip flop on the rising edge of the system clock. The Q output of the flip flop can then be gated to the output pin by enabling the active low tri-state buffer.

In addition to being available for transmission, the Q output is fed back into the PAL array as an input term. This feedback allows the PAL to "remember" the previous state, and it can alter its function based upon that state. This allows the designer to configure the PAL as a state sequencer which can be programmed to execute such elementary functions as count up, count down, skip, shift and branch. These functions can be executed by the registered PAL at rates of up to 20 MHz.

There are also PALs that feature an exclusive OR function. These PALs allow the sum of products to be segmented into two sums which are then exclusive ORed (XOR) at the input of the D-type flip flop. The exclusive OR PALs usually include all of the features of the registered PALs. The XOR function provides an easy implementation of the HOLD operation used in counters.

With the addition of gated feedback to the exclusive OR (XOR) PALs arithmetic functions can be implemented. The XOR at the input of the D-type flip flop allows carrys from previous operations to be XORed with two variable sums generated by the PAL array: the flip flop Q output is fed back to be gated with output terms. This gated feedback provides any one of the 16 possible Boolean combinations which can be mapped and be programmed by the PAL. These features provide for versatile operations on two variables and facilitate the parallel generation of carrys necessary for fast arithmetic operations.

o The last, and one of the most complex, digital device to be considered is the Manchester Encoder/Decoder which is used to perform time division multiplexing of serial data protocols. This device can be compared to a UART which is used to communicate between parallel input devices, such as a computer and synchronous serial interfaces.

The type of time division multiplexing that is performed is the Manchester II bi-phase level (data code). This code produces a bipolar coded signal for the transmitting of binary zeros and ones. A logic one shall be transmitted as a bipolar coded signal 1/0 (i.e., a positive pulse followed by a negative pulse). A logic zero shall be a bipolar coded signal 0/1 (i.e., a negative pulse followed by a positive pulse). A transition through zero occurs at the midpoint of each bit time. This code eliminates the DC component that appears on the bus thus enabling the use of transformer coupling and providing excellent isolation among the systems and their environments.

The chip is divided into two sections: an encoder and a decoder, these sections operate completely independent of each other, except for the master reset function. The encoder produces the synchronization pulse and the parity bit as well as the encoding of the data bits. The decoder recognizes the synchronization pulse and identifies it as well as decoding the data bits and checking parity. This circuit is meant to meet the needs of aircraft internal time division command/response multiplex data bus of MIL-STD-1553.

5.2.1.5 APPLICATION DATA FOR COMMONLY USED LSI MICROCIRCUITS

Due to the high complexity of LSI and VLSI circuits, it is extremely difficult and sometimes impossible to test every single gate in a microcircuit. It is therefore important that particular attention be paid to the production and processing sequence to insure the procurement of reliable products.

o Memories. There are a variety of semiconductor memories available to the designer, each having attributes which recommend it in a particular application. The following guidelines should assist the designer in selecting components which will perform reliably in a given application.

o Read Only Memories (ROM). A read only memory (ROM) is an electronic circuit used to store binary information. The major components of a ROM are an address decoder, memory storage elements, and output circuits. It is programmed during the fabrication process by means of a customized metallization mask. This process permanently programs a ROM, creating a nonvolatile memory useful in applications where "permanent" memory is required. At this time 128K bit ROMs have been made available while more complex 256K and 512K ROMs are still under development.

When programmed appropriately, ROMs may be used to replace many different types of combinational circuits. In particular, complex logic functions with multiple inputs and outputs can easily be replaced by a ROM. However, if the circuit to be implemented has fewer than four inputs and outputs the circuit could be implemented better with an SSI or MSI logic circuit. Only when the output and inputs equal or exceed four does the use of a ROM become practical and economical. Other uses for ROMs include the storage of high level languages, character generation, operating systems, and other permanent software requirements.

o Programmable ROM (PROM). PROMs are functionally equivalent to ROMs with the added advantage of being user programmable. They can be tailored to fit any given application without the expense of having a ROM specifically built at the factory. The passing of current pulses through fusible links within the PROM programs specific bits by the "blowing of fuses." The final result is a fixed memory content which has been field programmed. At this time 64K bits of programmable memory is not uncommon to PROMs.

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Generally PROMs are used where there is a need for more fixed storage than writeable storage. Applications include such usages as look up tables, encoders, and decoders. In addition PROMs are often used in the critical developmental stages of microprocessor systems. Since programming of these devices is performed by the user, these parts cannot be given a complete functional test by the vendor.

o Erasable PROMs. Erasable PROMs overcome the primary drawback of fusible link PROMs - namely that they can not be reprogrammed. EPROMS are offered in two basic varieties: ultraviolet light erasable PROMS (UV EPROMs) and electrically erasable (EEPROMs).

o UV PROMs. UV PROMs are packaged such that a transparent window allows light to pass through the package to the semiconductor chip itself. When high energy ultraviolet light is used, ionization currents result in a "deprogramming" of the PROM. It can be reprogrammed to the needs of the user by selectively applying electrical signals. The fact that these PROMs can be reprogrammed allows errors or obsolete data in the fixed storage pattern to be updated even after installation in the field. At this time the memory capabilities of UV PROMs are limited to 64K bits with 128K UV PROMs still under development.

Generally UV PROMs are more expensive than ROMs. Their applications include prototype, development, small production runs, or any application where one time, one of a kind data is needed and the total quantity required does not justify the use of mask programmable ROMs.

UV PROMs are prone to erasure and programming problems. Erasure is not selective. Therefore, the entire chip has to be cleared by exposure to ultraviolet light. Overexposure will cause voltage threshold shifts that result in memory malfunction while underexposure causes incomplete erasure.

As would be expected, UV PROMs should not be used in applications where high energy radiation will be present. Sunlight and even common fluorescent light have been found to erase UV PROMs over a period of time. However, through the use of a special window covering, unwanted erasure of information may be prevented. Also, UV PROMs portray typically poor performances in radiation environments due to ionization currents. High temperature applications can also be a problem with these parts; since leakage currents are temperature dependent the charge stored in the cell may leak off during prolonged exposure to high temperatures. These parts are not generally recommended for high volume production or severe environments.

o EEPROMs. Electrically erasable PROMs are similar to UV PROMs except that these devices are erased by means of an electrical signal instead of ultraviolet radiation. Bulk erasure or erasure and programming of individual bytes while in the printed board socket is possible with EEPROMs. These nonvolatile memories allow realtime program changes, have reasonable speed for reading data, and can be programmed quicker and easier than UV PROMs. In all other aspects EEPROMs operate in a similar manner to UV PROMs and are therefore subject to the same strengths and limitations.

o RAM. Random Access Memories (RAMs) are the only true semiconductor read/write memory presently in common use. RAM usually provides the memory used for data storage, scratch pad memory, working space, etc. RAM is available in two basic types: static and dynamic. Static RAM uses a memory cell configuration which toggles, so that each bit is stable and permanent so long as power is applied. A static RAM can be either bipolar or MOS. Bipolar memories are very fast and are used in high speed systems. They require only one standard +5V power supply. MOS memories on the other hand are slower and may require more than one power supply. They do, however, require less power and have a higher packaging density. Dynamic RAMs, which are all MOS, operate on a charged capacitor principle; the memory location is like a capacitor and must be refreshed periodically to compensate for leakage currents. Dynamic memories require fewer transistors per bit, so that higher densities can be achieved than with static RAMs. This advantage is partially offset by the need for additional circuitry to perform the refresh function.

Due to leakage sensitivities, dynamic RAMs are vulnerable to radiation, high temperatures and other such stresses which increase leakage currents. This is particularly true for high density RAMs (above 16K) since higher densities are achieved by using smaller geometries and thus smaller capacitors.

While RAMs are volatile in that memory contents are lost when power to the devices is removed, it is relatively simple to install a battery back up circuit such that when AC power is removed the battery circuit switches in to maintain power to the RAMs, thereby preserving memory contents. Another way in which RAMs are made nonvolatile is by the addition of an on-chip EEPROM. This nonvolatile RAM (NVRAM) functions similarly to an ordinary RAM in a normally powered system. If power starts to fail a simple TTL-level signal stores a "snapshot" of the RAMs contents in the EEPROM. Once stored the RAMs' contents can easily be recalled from the EEPROM through another TTL signal. At this time RAMs having up to 64K bits of accessible memory are available while RAMs upwards to 256K bits of accessible memory are still under development.

o Bubble Memories. Bubble memories are not actually semiconductor memories but are analogous in operation and interfacing to semiconductor memories. Bubble memories are composed of a thin film of magnetic garnet which lies perpendicular to a magnetic field. This field magnetizes tiny cylindrical portions of the surface. A second magnetic field can be found parallel to the film. When the direction of this second magnetic field is changed the cylinders (bubbles) are moved around the film surface.

Digital data may be represented by these magnetic bubbles. The presence of a bubble represents a logic "1" while the absence of a bubble denotes a logic "0". These bubbles may be held in a fixed position with a simple magnetic field. Therefore, if power is interrupted or removed any stored data will remain intact as long as the magnetic field is not disturbed.

Due to speed limitations present day bubble memory devices are competing with core memories and other magnetic storage devices such as disc and tape. Unlike magnetic tapes and discs, bubble memories require no moving parts to store or retrieve data and in general require less power to operate.

As of the middle of 1982, most major manufacturers of bubble memories have withdrawn from the market. As a result, bubble memories are recommended for new designs only if second sources and long term availability of the product can be insured. When used, bubble memories offer the storage of large quantities of data in small areas which remains intact even when power is removed. They also have large memory storage capabilities with up to 4 megabits of accessible memory at the time of the writing.

For military programs, MIL-M-38510 qualified memories should be used whenever possible. In addition to mechanical and electrical specifications, MIL-M-38510 slash sheets often give testing plans and/or requirements which will insure maximum testing efficiency with minimum time and expense.

5.2.1.6 MICROPROCESSORS, MICROCOMPUTERS AND BIT-SLICE PROCESSORS

In the trend from SSI to LSI and VLSI, hardware has become more and more generalized, in order to accomodate the large markets needed to recover extensive development costs. Specifics needed to tailor a component to a particular application are being developed through software. As a result, the engineering and development of new systems has changed from hardware intensive to software intensive.

o Selection of Processing Units. Processing units are microcircuits with hardware which is "customized" for a specific task through software and firmware. While each uP on the market has unique features recommending it in certain applications, these complex chips may be broadly categorized by the design philosophy employed and the system configuration used. Alternatives include bit slice processors, microcomputers, and the basic microprocessor. A general characterization of the features of these types of processor is given in Figure 5.2.1.6-1.

(a) BIT Slice. Bit slice processors are designed to handle a relatively small number of bits (typically 4) in a parallel fashion. If a longer word is needed, the bit slice is designed such that 2 or 4 of these units may be used in parallel to provide the necessary number of bits. While the bit slice is a versatile and potentially powerful approach to data processing, it places great demands on the designer, since much of the I/O capabilities and control functions must be ahcieved through hardware or firmware. High development costs have presented bit slice units for gaining wide use in the more conventional applications.

While not necessaily more reliable, bit slice designs are usually much easier to test than are microprocessor or microcomputer designs due to the accessibility of test modes.

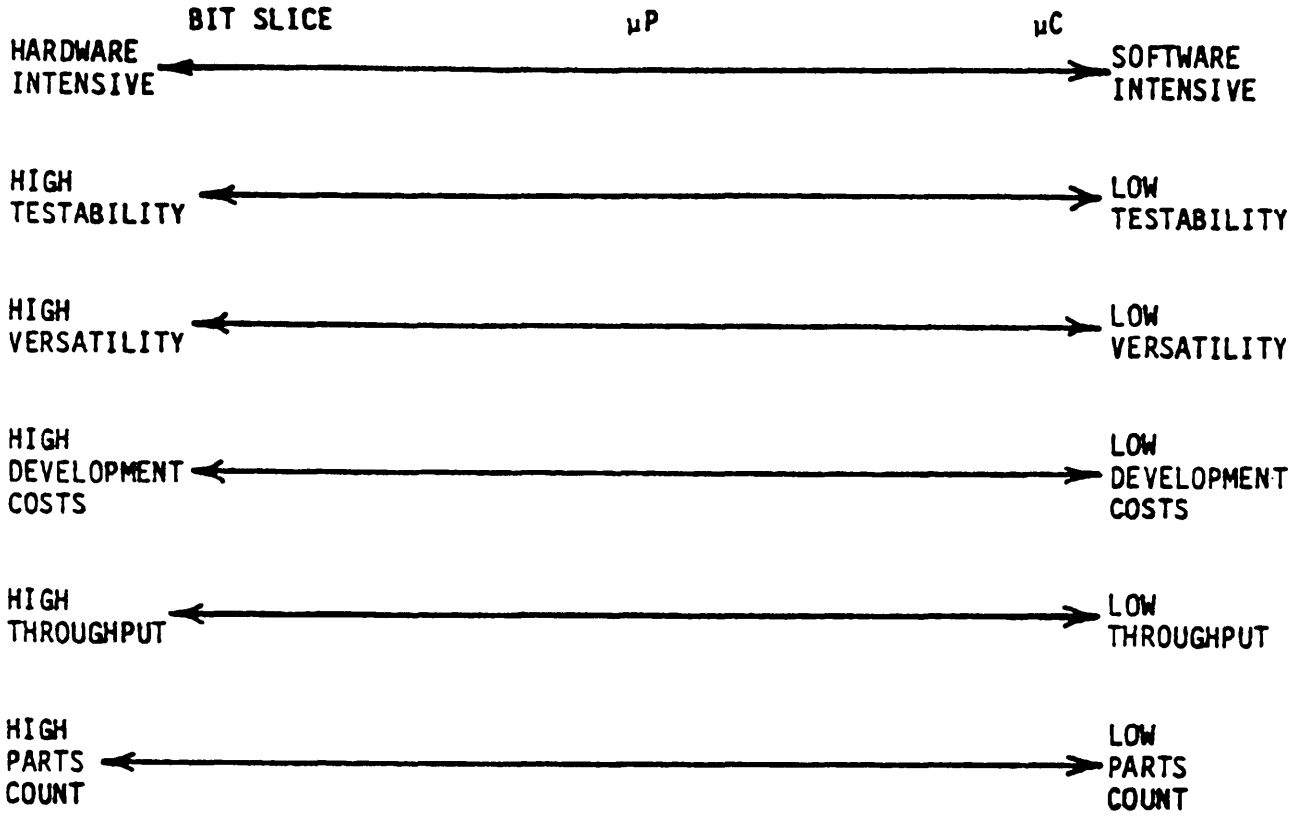


FIGURE 5.2.1.6-1: PROCESSING UNIT CHARACTERISTICS

(b) Microprocessors. Microprocessors represent the middle-of-the-road approach, providing the optimal balance between hardware and software for the vast majority of applications. Microprocessors provide for simpler designs by placing much of the I/O and memory addressing under software control. At the same time, sufficient versatility is provided that expansion of memory of I/O is very easy within broad limits. While more consolidated than the bit slice processor, the microprocessor still employs a number of components to realize a processing system. Most memory and interfacing is done through external support chips, so that testability is still more or less acceptable. There are, however, several features being offered on uPs, which simplify design but are proving very difficult to test adequately. These features include internal generation of voltages (so that only a single +5V supply is needed), internal generation of multi phase clocks, and the use of pseudo static RAMs (dynamic RAMs with internal refresh). These and other functions which cannot be directly accessed through package pins should be carefully scrutinized.

(c) Microcomputers. As used here, a microcomputer is nothing more than a uP where the memory, I/O, and other support circuitry have been integrated onto the same chip with the processing unit. This provides the designer with what is essentially a single chip computer. Design is greatly simplified with such a chip, however, versatility is rather limited.

Due to the high level of integration, testability is very low for these devices, and fault isolation is often impossible. For noncritical, easily maintainable applications, the uC may be ideal, since by replacing the single uC chip, essentially the entire processing/memory/control circuit has been replaced. In critical and/or nonmaintainable systems, the difficulty of verifying a good part (or conversely detecting a fault in a bad part) may make the uC a poor choice.

Most standard parts have MIL-M-38510 slash sheets available, containing detailed specifications and testing requirements. This information is based on exhaustive testing and a detailed analysis of the physical, electrical and thermal characteristics of the part. For this reason, MIL-M-38510 specifications should be called out in procurement documents whenever possible.

Despite very small power requirements per gate, the very large number of gates per chip in a random logic LSI microcircuit results in a substantial overall power requirements. For this reason, thermal design is an important consideration. Another area of concern is that the larger rigid ceramic DIP packages have proven vulnerable to failure in high mechanical stress environments. In fact, centrifuge testing of large cerdips is nearly impossible, since the package breaks at a lower level of stress than the bonds for which the test was designed.

The compact leadless chip carrier packages seem to offer better mechanical strength and higher board densities, but may have poor thermal characteristics as compared to large DIP packages.

The following is a brief summary of each of the processing units for which MIL-M-38510 specifications were completed or in process at the time of this writing.

AMD 2900 FAMILY

The AM 2900 Bipolar Microprocessor Family offers a full line of LSI and support products optimized for high performance CPU applications. The devices use Schottky and low power Schottky process technologies to implement LSI functions.

The LSI members of the 2900 family represent new kinds of building blocks for designers of high performance systems. Each part is specialized for a particular part of the system, such as the arithmetic unit or memory control. Lower complexity support chips are available to provide optimum interface between functional elements of the system.

The 2901B offers the following features:

- 2 address architecture
- 8 function ALU
- flexible data source selection
- left/right shift independent of ALU
- 4 status flags
- expandable bit-slice architecture
- microprogrammable
- 115 ns for 16-bit addition
- 40 pin DIP

Second sourcing is available from Fairchild, Motorola, National, NEC and Raytheon.

INTEL 8048/8035/8748

The 8048/8035/8748 are totally self sufficient 8 bit parallel computers fabricated on a single silicon chip using silicon gate NMOS technology.

The 8748 contains a 1K x 8 UV erasable user programmable program memory, a 64 x 8 RAM data memory, 27 I/O ports and an 8-bit timer/counter in addition to on board oscillator and clock circuits. For systems that require extra capabilities, the 8748 can be expanded using standard memories and MCS-80/MCS-85 peripherals. The 8035 is the equivalent of an 8748 without program memory and can be used with external ROM and RAM.

To reduce development problems and provide maximum flexibility, three interchangeable pin compatible versions of this single chip microcomputer exist: the 8748 with UV EPROM program memory, the 8048 with factory programmed mask ROM program memory for low cost high volume production, and the 8035 without program memory for use with external program memories. The following are key features of the 8048/8748/8035 family:

- o single 5 volt supply
- o over 90 instructions, 70% single byte
- o single level interrupt
- o compatible with 8080/8085 series peripherals
- o interval timer/event counter

No second sources were available as of this writing.

INTEL 8080

As the most popular "workhorse" among the microprocessor, the 40-pin silicon gate N-channel microprocessor is TTL compatible. It is operationally a parallel CPU with an instruction cycle time of 2 us at the nominal clock rate of a 2 MHz, and 78 microinstructions, and clocked with a 2-phase, nonoverlapping clock. It has 14 control lines, and a 8-line bidirectional data bus; a 16-line bus is used for addressing the memory along with a 24-I/O line section. All system controls are decoded on the chip. The CPU accesses up to 64-K bytes of memory, and operates up to 256 input and 256 output 8-bit channels; it has a provision of 8 interrupt levels.

High speed I/O structure, memory, and control lines permit its use as a controller and a data processing subsystem. Stack architecture enables the programmer to effectively process both subroutines and interrupts. Instructions are capable of handling strings of data along with decimal and double byte arithmetic. Both decimal and binary data are handled with equal speed.

The Intel 8080 microprocessor employs the programmable peripheral interface (PPI) 8255 for easy interface to printers, keyboards, displays, and motor drives. It has 13 options for memory circuits, such as 16-K bit ROMs, 8-K bit EPROMs, and 4-K bit RAMs (at high density and low cost) plus CMOS-RAMs for minimum power requirements.

For military applications a ruggedized version M8080A is preferred. The 8080 is not recommended for new designs. Several second sources exist.

INTEL 8086

The Intel 8086 (iAPX 86/10) is a new generation high performance 16-bit microprocessor implemented in N-channel, depletion mode silicon gate technology (HMOS) and packaged in a 40 pin ceramic dual in-line package.

The processor has attributes for both 8- and 16-bit microprocessors. It addresses memory as a sequence of 8-bit bytes, but has a 16-bit physical path to memory for high performance. The military version is rated over the full military temperature range, -55^{o}C to +125^{o}C. The following are highlights of the capabilities of the 8086:

- o direct addressing of 1M byte of memory
- o 24 operand addressing modes
- o assembly language compatible with 8080/8085
- o bit, byte, word and block operations
- o 8- and 16-bit signed and unsigned arithmetic in binary or decimal including multiply and divide
- o 5 MHz clock rate
- o multibus system compatible interface

Second sourcing for the M8086/iAPX 86/10 include Mitsubishi, Mostek, Siemens and NEC.

MOTOROLA 6800

The MC 6800 was introducted in 1974 as the first processor of the 6800 family, and still remains a high cost effective processor for a great many process control and data communications applications. Seventy-two instructions and six addressing modes give it a high degree of versatility. A full range of compatible peripheral chips offer the considerable latitude in system implementation. Years of field use have insured a fully debugged processor with considerable software available.

The MC6800 is an 8-bit processor implemented using NMOS technology. It operates from a single 5 volt supply at clock rates from 1-2 MHz (2 phase). The 6800 can directly address 65K of RAM and has a register-to-register add time of 1 usec (2 MHz clock). Much software support is available, and second sourcing is available from AMI, Fairchild, Hitachi, and Fujitsu.

MOTOROLA MC 68000

The 68000 CPU was introduced in 1979 and has been followed by a host of peripherals. (It should be noted that all MC6800 peripherals interface directly with the MC 68000, so upward compatibility is built in.) The 16-bit MC 68000 has been implemented using high performance HMOS technology, operates from a single 5V supply and dissipates approximately 1200 mW. 16 Mb of memory may be directly addressed by this CPU. Four versions of the 68000 are available, having clock frequencies of 4 MHz, 6 MHz, 8 MHz, and 10 MHz. Second source for this device include Hitachi, Mostek, Phillips, Rockwell and Signetics.

RCA CDP 1802

The CDP 1802 microprocessor is an 8-bit LSI silicon gate CMOS register oriented central processing unit designed for use as a general purpose computing or control element in a wide variety of military, industrial, and commercial applications.

The CMOS technology provides a high noise immunity to enable the 1802 to operate in electrically hostile environments. The 1802 can be powered by an unregulated supply over a wide operating voltage range. Further the processor is completely static so that its system clock can be controlled

to interface with slow memories, or stopped to provide reduced power consumption during standby conditions. Highlights of the CDP 1802 are as follows:

- 8-bit static CMOS processor
- power dissipation 80 mW at 10 volts
- clock rate 0-6.6 MHz
- direct address capability to 64K
- full MIL temp. range (standard)
- high level languages include Basic, Pascal, PL/M

Second sourcing of the 1802 is available from Hughes.

TI 9900A

The Texas Instruments 9900A is a 16-bit central processing unit (CPU) implemented using integrated injection logic (I^2L) technology. The fully static circuitry may be clocked at 0-3 MHz/1 phase. A first generation processor of the 9900 family, this component has been superceded by the SBP 9989, and is therefore not recommended for new designs.

Texas Instruments SBP 9989

The SBP 9989 is a second generation 16-bit processor of the TI 9900 family, implemented in advanced oxide separated current mode logic (I^2L). Since its inception in 1972, I^2L has proved to be a useful LSI technology, offering excellent speed/power performance and the small gate geometries required to pack an LSI function onto a producible bipolar IC chip. Since an I^2L gate is current injected, no transistor on an I^2L device is subjected to more voltage stress than is necessary to implement a primitive logic function. Also, since the ground current path for an I^2L device is vertical, the devices tend to be more immune to radiation effects than those built in other technologies.

The SBP 9989 offers 2 times the throughput of its predecessor, the 9900A, while maintaining compatibility with it. Software of the 9900A is also compatible with the 9989, although the faster clock may require reprogramming of the WAIT states.

A summary of features of the SBP 9989 follows:

- 16-bit data and address bus
- 4.4 MHz rate, single phase, 50% duty cycle
- fully static, advanced I^2L technology
- 10 prioritized hardware interrupts/16 software interrupts
- 9900 family instruction set
- direct access to 132K bytes of memory
- operation over full MIL-TEMP range: $-55^{o}C$ to $+125^{o}C$
- radiation tolerance characteristic of I^2L technology
- available in 64 pin DIP or 68 pin-pad leadless chip carrier (LCC) package

As of this writing (May 1982), no second sources are available for this device.

ZILOG Z80

The Z80 is an 8-bit central processing unit (CPU) implemented using NMOS technology. It operates from a single 5 volt supply and dissipates 1100 mW. Since its introduction in 1976, the Z80 has proven to be an extremely popular and versatile performer. All 8080A software is compatible with the Z80 providing for a wealth of software, although the Z80 has an instruction set of 158 commands as opposed to 78 for the 8080A. The following are key features of the Z80:

- o 4 and 6 MHz clock versions available
- o directly addresses 65K words
- o vectored maskable; unmaskable interrupts
- o register to register add time 0.667 usec
- o PL/Z high level language available
- o Fortran IV cross assemblies available
- o MIL-SPEC versions available
- o special low power (Z80 L) is available

Second sources for the Z80 include Mostek, NEC and SGS. Improved versions incuding the Z80A and Z80B are now available and are preferred for new designs.

ZILOG Z8000 FAMILY

The Z8000 is an advanced 16-bit microprocessor implemented using NMOS technology. A single 5 volt power supply is required, and the device dissipates 1200 mW. The Z8000 CPU is available in two versions, the Z8001 48 pin segmented CPU and the Z8002 40-pin nonsegmented CPU. The main difference between the two is in the addressing range; the Z8001 can directly address 8 M bytes of memory, the Z8002 directly addresses 64 K bytes. A summary of important features follows:

- o eight (8) user selectable addressing modes
- o seven (7) data types
- o system and normal operating modes
- o separate code, data and stack spaces
- o sophisticated interrupt structure
- o 32-bit operations, including signed multiply and divide
- o Z-BUS compatible

Second sourcing for the Z8000 is available from AMD.

ZILOG Z8 FAMILY

The Z8 microcomputer family consists of the following:

Z8611/Z8601	Single chip microcomputer with 4K/2K ROM
Z8612/Z8602	Development device with memory interface
Z8613/Z8603	Prototyping device with EPROM interface

The Z8611/Z8601, as the production versions, represent sophisticated single chip microcomputers implemented in NMOS. Under program control, they can be tailored to the needs of the user. They can be configured as a stand above microcomputers with internal ROM, as traditional processors that manage up to 124K bytes of external memory, or as parallel processing elements in a system with other processors and peripheral controllers.

Features include the following:

- o average instruction time of 2.2 usec
- o vectored priority interrupts
- o on-chip oscillator
- o single +5 volt supply
- o low power standby operation

Second sourcing is available from Synertek.

5.2.1.7 DERATING

Derating may be defined as the practice of limiting electrical, thermal and mechanical stresses on parts to levels below their specified or proven capabilities in order to enhance reliability. By derating the margin between the operating stress level and the maximum stress level for a part is increased, thus providing added protection from system anomalies unforeseen by the designer. Some suggested derating guidelines for microcircuits are outlined in the following tables.

	Environmental Derating Factor	
Parameter	Benign	Severe
Supply Voltage (1)	.80	.70
Input voltage	.70	.60
Output Current	.80	.70
Maximum Junction Temp (^{o}C)	105	80

(1) For devices with dynamic supply voltage ranges only; all others use the manufacturers' recommended supply voltage. Derating below 80% of the supply voltage may operate the device below recommended operating voltages.

TABLE 5.2.1.7-1: LINEAR MICROCIRCUIT DERATING

high impedance inputs (1) 2b MA programmable AND array 4NK inputs provide

	Environmental Derating Factor	
Parameter	Benign	Severe
Fixed Supply Voltage (1)	+/-5%	+/-3%
Dynamic Supply Voltage	.85	.70(2)
Frequency (Bipolar) (3)	.95	.80
Frequency (MOS) (3)	.90	.80
Output Current (4)	.90	.80
Maximum Junc. Temp. (^{o}C)	110	85

(1) Tighten tolerance from nominal value for bipolar.
(2) Designing below 80% of the supply voltage may cause operation of the device below the recommended operating voltage.
(3) For dynamic devices care should be taken not to operate below minimum frequency requirements.
(4) Reducing fanout may increase part count, which in turn increases equipment failure rate. Adjustment should be allowed to prevent this occurrence.

TABLE 5.2.1.7-2: DIGITAL MICROCIRCUIT DERATING

	Environmental Derating Factor	
Parameter	Benign	Severe
Maximum Junc. Temp. (^{o}C)	110	85
Thick Film Power Density (1)	50 W/in^2	50W/in^2
Thin Film Power Density (1)	40 W/in^2	40W/in^2

(1) For every degree C above 100^{o}C case temperature derate the power density 1 W/in^2 below the values shown.

TABLE 5.2.1.7-3: HYBRID DEVICES DERATING

REFERENCES

1. Hnatek, E.R., "Semiconductor Memory Update: EEPROMs," Computer Design, December 1981, pp. 137-144.

2. Huffman, G.D., "Alterable-Memory Innovations Enhance New-Product Designs," EDN, January 1982, pp. 89-98.

3. Twaddell, W., "Semiconductor RAMs," EDN, September 1980, pp. 118-132.

4. Leonard, M. "Semiconductor Memory: A Special Report," IC Update, Vol. III, No. 2, April 1981, pp. 6-38.

5. Bipolar LSI 1982 Databook, 4th ed. MMI-4 Monolithic Memories.

6. MC MOS Handbook Motorola, 1974.

7. Linear and Interface Circuit Applications, Texas Instruments TI-27.

8. Heathkit Continuing Ed. Digital Techniques Book II, Chapters 5 through 10.

9. Practical Digital Design Using IC, Joseph D. Greenfield.

10. Digital Bipolar/CMOS, Vol. 2, 1981, Harris HA-13.

11. MIL-STD-1553B Aircraft Internal Time/Division Command/Response Multiplex Data Bus.

12. McGlynn, D.R., "Microprocessors," John Wiley & Sons, 1976.

13. Lloyd, D.K. and M. Lipow, "Reliability: Management Methods and Mathematics," 1977.

14. Computer Search, "Microprocessor Failures Due to Software."

15. Morris, R. L. and J. Miller, "Designing with TTL Integrated Circuits," McGraw-Hill Book Company, NY, 1971.

16. Schottky and Low Power Schottky Data Book, Advanced Micro Devices, Inc., 1977.

17. Analog Circuit Design Seminar Manual, Analog Devices, 1982.

18. Component Technology and Standardization Guidelines, General Electric Company.

5.2.2 DISCRETE SEMICONDUCTOR DEVICES

5.2.2.1 INTRODUCTION

Expanding technology, widespread use and the economics of large volume production have resulted in a proliferation of discrete semiconductor devices. There exists a wide variety of functional classifications based upon electrical characteristics, such as low or high power, switching time, internal capacitance and forward current, available to the designer. In addition, there are several categories relating to semiconductor device materials, processes, technologies and configurations.

5.2.2.2 DEVICE SELECTION

The selection of a specific semiconductor device is governed by the guidelines depicted in Table 5.2.2.2-1. As shown in this table, the governing specification for discrete semiconductor devices is MIL-S-19500. This basic document and its appended, detailed specification sheets establish the general and specific requirements including definitions, abbreviations and symbols, electrical characteristics, electrical, mechanical and environmental requirements, styles, test methods, quality assurance provisions, and qualification and inspection procedures for all semiconductor devices.

A quarterly updated publication entitled "Lists of Standard Semiconductors," MIL-STD-701 describes the current qualification status of, and provides a preferred part selection list for, a wide variety of microcircuit and discrete semiconductor types.

TABLE 5.2.2.2-1: SEMICONDUCTOR SELECTION CRITERIA

1.	MRAP/SRAP "Microcircuit/Semiconductor Reliability Assessment Program"
2.	MIL-S-19500, "Semiconductor Devices, General Specifications For" ("JANTXV" or "JANTX" devices).
3.	MIL-STD-1547, "Parts Materials and Processes for Space and Launch Vehicles, Technical Requirements For"

5.2.2.3 GENERAL APPLICATION DATA

o Device Parameter Drift. Semiconductor devices may exhibit change in parameter values over their life within specified limits. Therefore, for long life reliability the design should be able to tolerate a shift in the parameters as shown on the individual MIL-S-19500 detail specification.

o Sealing. Only hermetically sealed devices should be used. No plastic (organic or polymeric) encapsulated or sealed devices shall be used. Devices with plastic material over the junction should not be used.

o Reverse Current. In no case should the leakage current exceed 100% of the maximum specification limit.

o Uncontrolled Characteristics. Satisfactory equipment performance should not depend on a semiconductor device characteristic which is not controlled by the applicable MIL-S-19500 detail specification.

o Non-glassivated Semiconductors. Non-glassivated semiconductors in which leads cross scribe lines with clearances of less than 0.002 inches shall not be used.

o Hot-welded Cans. No semiconductor devices packaged in hot-welded cans shall be used.

o DO-7 Package. No diodes packaged in DO-7 packages shall be used.

o Whisker Diodes. No point contact (whisker) diodes shall be used.

o Germanium Devices. No germanium (Ge) semiconductors shall be used.

o Unijunction Devices. No unijunction devices shall be used.

o Gold Aluminum Bonds. Devices fabricated with gold-to-aluminum bonds shall be used only when the following two in-process controls are implemented to assure adequate bond strength: accelerated testing of bond strength and control of burn-in conditions.

a) Accelerated Testing of Bond Strength. A high temperature bake followed by cooling to room temperature shall precede the bond pull. This test shall be conducted during device manufacture. One of the following times and temperatures shall be used for accelerated testing of Au-Al bond integrity.

1 hour at 350°C
4 hours at 300°C
24 hours at 250°C
200 hours at 200°C
3000 hours at 150°C

This test shall be used for bond pull tests every two hours of production. The sample size shall be 5 devices or 2 percent, whichever is larger. Any bond strength determined which is less than 0.5 of the bond strength specified for the "as made" or the "post seal" condition in MIL-STD-750, Method 2037, shall be a cause for rejection.

b) Burn-In Control. Burn-in of bi-metallic wire bonded devices shall be conducted at such conditions of thermal impedance, power, and fixture variations that the maximum junction temperature is 150°C. The time for such burn-in should be determined using the time/temperature regression data of Method 1015, MIL-STD-883, as shown in Figure 5.2.2.3-1.

follows:

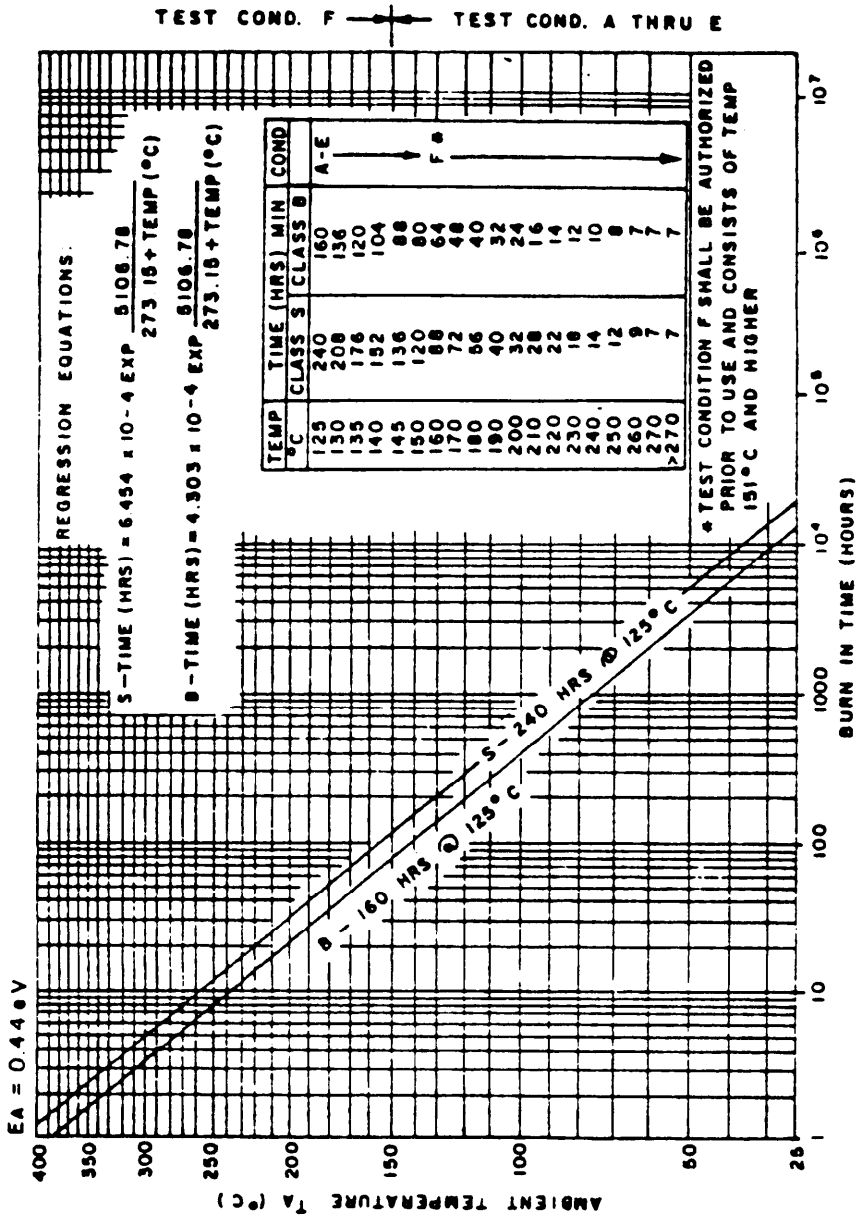


FIGURE 5.2.2.3-1: TIME TEMPERATURE REGRESSION

o Metallurgical Bonds. Axial-lead diodes and rectifiers shall be solid glass construction utilizing high temperature ($> 700^{0}C$) metallurgical bonding between both sides of the silicon die and therminal pins.

o MOSFET Structure. Only vertical diffusion, non-V-groove structure MOSFETs shall be used.

o Peak Current Rating. Do not exceed a MOSFET's peak current rating. In addition to sometimes supplying unexpectedly high currents to a commutating diode during its reverse recovery time, a MOSFET circuit might have to allow for heating, lighting and motor loads that consume high inrush currents when first turned on. These turn-on loads can be controlled by sensing the MOSFET's current and shutting down the drive signal when it reaches a preset limit.

o RMS Current Limit. The total continuous rms current (I_D) must not exceed the MOSFET's maximum rated value. Thus, in switching applications, if the duty cycle is D =tON/tTOTAL and the continuous-drain-current rating is I_D, the maximum permissible peak current level is

$$I_{PK} \leq \frac{I_D}{\sqrt{D}}$$

as long as this value remains below the MOSFET's specified maximum peak current rating, no problems should arise.

o Thermal Considerations. The maximum operating temperature rating of a MOSFET must not be exceeded. Remember that in switching circuits, the total power dissipated equals the sum of the conduction and switching losses. Switching losses are essentially temperature independent, but because a MOSFET's ON resistance increases with temperature, the designer must take these losses into account when sizing a heat sink.

o Electrostatic Damage Sensitivity. Certain types of semiconductor devices are susceptible to electrostatic discharge (ESD) damage. Appropriate procedures should be observed prior to handling these parts, and selections of devices should include an analysis of the input protection circuitry (see Section 6.1.6, Volume 2).

5.2.2.3.1 DIODES

(a) Rectifiers

o Characteristics. Junction diodes designed for use as rectifiers should have I-V characteristics as close as possible to that of the ideal diode. The reverse current should be negligible, and the forward current should exhibit little voltage dependence. The reverse breakdown voltage should be large, and the offset voltage in the forward direction should be small.

o High Temperature Reverse Bias Devices. High temperature reverse bias devices should be of bevelled edge or guard ring construction.

o Rectifier Junction Mounting. The mounting of a rectifier junction is critical in its ability to handle power. For diodes used in low power circuits, glass encapsulation or a simple header mounting is adequate. However, high current devices which must dissipate large amounts of heat require special mountings to transfer thermal energy away from the junction. Generally Si power rectifiers are mounted on molybdenum or tungsten disks to match the thermal expansion properties of the Si. The disk is fastened to a large stud of copper or other thermally conductive material that can be bolted to a heat sink.

o Recovery Time. If the external voltage is suddenly reversed in a diode circuit which has been carrying current in the forward direction, the diode will not immediately fall to its steady-state reverse-voltage value until the excess minority carrier density has dropped nominally to zero. There is also a switching transient time (recovery time) when the voltage is switched from reverse to forward direction, because the depletion layer capacitance has to be discharged and diffusion capacitance has to be charged before the steady-state forward current is established.

The effect of a finite recovery time on the uses and limitations of diodes for rectification and switching is considerable. When rectifying, it is obvious that if a high frequency voltage is to be rectified having a period of the same order of magnitude as the recovery time, there would be no rectification. During the first, positive, half cycle, the diffusion capacitance would discharge and the diode would operate as if it were a capacitor and not a rectifying element. Each diode has, therefore, an upper limit to the frequency at which it can be used for rectification (or for demodulation of RF waves in the case of diodes intended for RF detection). The rectification efficiency of a diode which usually operates as a line-frequency rectifier or as a low frequency switch, may drop to 50% when the frequency is increased to a few kilohertz. As the frequency limit of the device is approached, its rectification efficiency decreases proportionately. This can result in the overheating and destruction of the device.

(b) Schottky Barrier Rectifiers

Schottky power diodes are majority carrier devices ideally having no discernible reverse recovery characteristics due to minority carrier storage. This feature is most important in high frequency system applications in low voltage rectifier circuits.

The Schottky diode has a metal barrier type junction rather than a diffused P-N junction of standard power diodes. The Schottky diode has two characteristics that are very advantageous as rectifiers in power supply circuits. (1) The low forward voltage drop results in considerably less heat dissipation, therefore has a higher operating efficiency in the circuit. (2) The low recovery time at frequencies above 10kHz is also a significant advantage. The reverse recovery time of the Schottky is generally less than 10 ns compared to 50 ns for a standard fast recovery P-N junction diode, (e.g., 1N6304, 1N6305, 1N6306).

allow the sum of products to be segmented into two sums which are then

The Schottky diode has some disadvantages which should also be considered. The most significant disadvantage is the reverse voltage characteristics. The reverse voltage is lower than the P-N junction diode, therefore limiting its use to low voltage applications. The reverse current is higher than the P-N types.

Device manufacturers use different barrier layers including chromium, tungsten, molybdenum, platinum and modified, (i.e., "doped") versions thereof. All device types except those utilizing the chromium barrier layer perform satisfactorily at junction temperatures up to 150°C, and some "high temperature process" devices (using a modified molybdenum and platinum barrier layer) are capable of satisfactorily operating at 175°C junction temperature (at the expense of a higher forward voltage). Only these high temperature process devices are recommended for use in military equipments, and chromium barrier types shall not be used because of the possibility of thermal runaway above 85°C.

(c) Varactors

o Application. The varactor diode is designed to exploit the voltage variable properties of the junction capacitance. For example, a varactor (or a set of varactors) may be used in the tuning stage of a radio receiver to replace the bulky variable plate capacitor. The size of the resulting circuit can be greatly reduced, and its dependability is often improved. The series resistance and leakage current should be small so that the selectivity "Q" is high. In addition, the range of capacitance variation should be large. For some high frequency applications, varactors can be designed to exploit the forward-bias charge storage capacitance. The step-recovery diode is an example of this type of device.

(d) Thyristors

Thristors comprise a family of bistable semiconductor devices composed of three or more junctions that can be switched from the OFF state to the ON state or vice versa, such switching occurring within at least one quadrant of the principal voltage-current characteristic. Silicon controlled rectifier (SCRs) are the most commonly used type of thyristors.

(e) Silicon Controlled Rectifiers (SCRs)

o Turn-on Time. One limitation of the SCR, specified by the manufacturer, is the maximum rate at which the anode current may be increased immediately after the device is triggered. The reason for this dI/dt limitation is the non-uniform distribution of I across the device area just after the gate pulse. Most of the current is concentrated very near the gate contact. Some finite time must pass before the carriers diffuse all across that area to conduction. It should be remembered that modern thyristors are very high current devices and their diameter may be 50 mm or more. By limiting the rate of growth of threshold current I, overheating near the gate contact is prevented.

o Repetitive Pulsing. SCR turn-off time, t_{off}, signifies the ability of the device to withstand reapplication of a forward voltage t_{off} seconds after the anode current goes below the holding current "I_H." At this point

the device is supposed to switch off. Due to the excess stored charge left over from the conduction period the device may turn on spontaneously if forward voltage is reapplied too quickly. One solution is the use of gold diffusion, which increases the number of recombination centers. This method shortens the device life time. Another method uses a momentary negative voltage pulse to the gate, sweeping out the charge. This is known as gate assisted turn-off.

5.2.2.3.2 TRANSISTORS

(a) Bipolar

o Maximum Current Ratings. Maximum collector current is usually determined by junction heating considerations and the heat convection ability of the transistor and its mount. In large area power transistors there is the danger of non-uniform current distribution across the emitter area. Hot spots can form where current densities exceed the average. Special emitter structures are used to prevent this. Sometimes manufacturers' current limitations arise from the method and materials used for interconnecting the transistor chip to the encapsulation terminals.

A reason for recommending maximum operating current is the sharp drop in h_{FE} beyond that point. The base emitter junction is especially vulnerable to overheating because of its much smaller area. Also, this junction usually contains a smaller metal contact than the collector's contact which helps in heat removal.

o Maximum Power Dissipation. The danger of collector junction overheating is most severe when both high current and high voltage conditions exist. The dissipated power that must be removed is approximately the product of the average values of I_C and V_{CE}. Transistor data sheets include the maximum collector dissipation rating, "P_D" maximum, at a given transistor case temperature, "T_C". This power is obtained from the heat flow equation:

$$T_j max - T_C = \theta_{jc} P_{dmax}$$

Where θ_{jc} ($^oC/W$) is the thermal resistance from collector junction to transistor case and T_j is the maximum allowable junction temperature.

o Maximum Voltages, First Breakdown. In some high frequency alloy junction transistors, with narrow, low doped bases, punch-through breakdown can limit the maximum collector voltage. The collector junction depletion layer extends through the whole base, reaching the emitter junction on the other side when V_{CE} is high. Further increase of V_{CE} will forward bias the emitter junction, causing a sharp current increase which is limited only by the external circuit. If no overheating occurs, however, the transistor suffers no permanent damage.

Punch-through breakdown does not usually occur in planar type transistors because the base impurity density obtained by diffusion is higher everywhere except at the collector. This causes the depletion layer to extend mostly into the collector, by increasing the collector voltage junction fields to the point where avalanche multiplication starts before punch-

through is reached. At this point, the current is then multiplied by a factor and increases very fast with the voltage. It is to be noted that high voltage transistor operation necessitates the use of low collector doping densities in the transistor design since this increases B_{VCBO}. Reduced collector doping, however, increases its parasitic bulk resistance between the junction and the outside terminal. This is why the planar epitaxial transistor was developed. Here low collector doping is maintained only near the collector junction, while the collector bulk needed for mechanical strength has high doping and low resistivity. Such a structure is essential for a switching transistor that must withstand high voltage in its "off" state and must present low saturation voltage in its "on" state.

Emitter base junction breakdown occurs at rather low reverse voltage in planar transistors due to the relatively high doping densities on both sides of the junction. One should not apply more than a few volts of reverse voltage to it without an external series resistance high enough to protect against excessive current when breakdown occurs. Alloy junction transistors can withstand high reverse base voltages due to their lower base doping.

o Secondary Breakdown. If a power transistor is allowed to reach and maintain high currents in the high voltage avalanche zone (see Figure 5.2.2.3-2) the second breakdown phenomenon may occur. By "second breakdown" we refer to a destructive process that can occur even though the current and voltage separately are still below the maximum ratings.

Secondary breakdown results from hot spot formation in the semiconductor from non-uniform current density distribution and a positive feedback effect. Accidental crystal faults, doping fluctuation or other non-uniformities originated by processing may cause this current non-uniformity. At extreme operating conditions these spots overheat, reducing the necessary V_{BE} for a given current and increasing the local thermally generated carrier density, resulting in more current concentration. Within a few microseconds local melting can occur with irreparable damage. This is evidenced in the device operating characteristics by a sudden collector voltage drop followed by a sharp current increase.

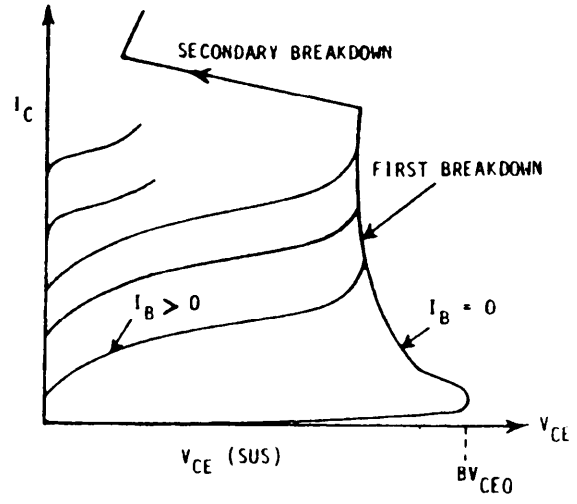


FIGURE 5.2.2.3-2: SECONDARY BREAKDOWN AT EXTREME OPERATING CONDITIONS

Some manufacturers supply a chart of I_C - V_{CE} (see Figure 5.2.2.3-3 below) that divides the active region into safe operating areas. The transistor is safe from secondary breakdown if it operates in that area for a limited time. For example, transistor 2N3719 can tolerate I_C = 10 A at V_{CE} = 30 V for only 5u secs but may tolerate 1 A at the same V_{CE} for 500u secs and 0.1 A for indefinite periods.

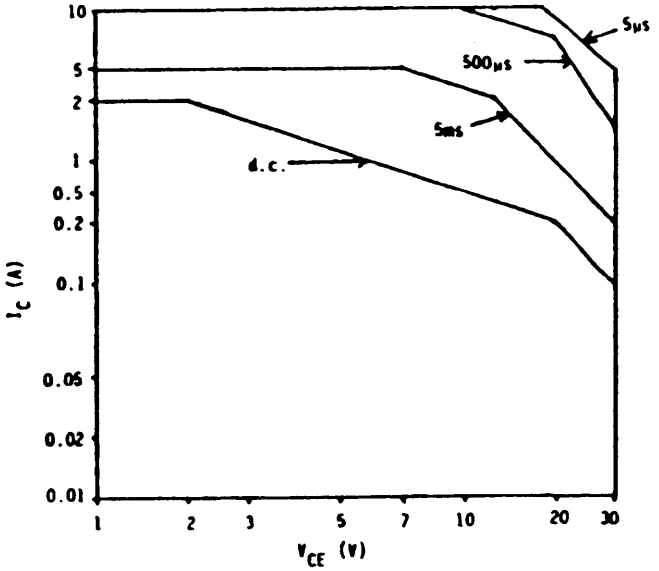


FIGURE 5.2.2.3-3: SECONDARY BREAKDOWN (SAFE OPERATING AREAS)

(b) FET (Field Effect Transistor)

The field effect transistor is a voltage-controlled device which can perform the complete switching function. Its electrical characteristics resemble those of a vacuum-tube. (Figure 5.2.2.3-4 shows how the collector, base and emitter terminology for the terminals of a bipolar transistor is replaced by drain, gate, and source, respectively for a MOSFET.) The flow of charge carriers between the source and the drain is controlled by the charge on the control or gate electrode. The device has the inherent advantage of solid-state technique, little or no noise, high resistance to the effects of nuclear radiation, high input impedance (typically many megohms), is readily self-biased and exhibits a non-linearity characteristic. Unlike conventional bipolar transistors field-effect transistors are unipolar devices (i.e., operation is basically a function of only one type of charge carrier: holes in p-channel devices or electrons in n-channel devices).

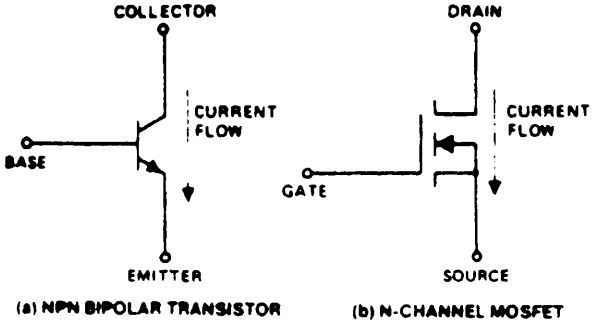


FIGURE 5.2.2.3-4: ELECTRICAL SYMBOLS FOR BIPOLAR AND MOSFET

A field effect transistor is essentially a semiconductor current path whose conductance is controlled by applying an electric field perpendicular to the current. The electric field results from reverse biasing a p-n junction.

(c) Power MOSFET

Power MOSFETS offer the superior characteristics of Field Effect Transistors at true high power levels. Power MOSFETs simplify circuitry because they are voltage-controlled devices and require only very small instantaneous currents from the signal source. They achieve switching times of less than 100 nanoseconds at high current levels. They have great ruggedness because of the absence of the second breakdown failure mechanism of bipolar transistors. In parallel operation they inherently "current share" rather than "current hog." The stability of the gain and response time characteristics over a wide temperature range is outstanding.

Power MOSFETs are majority carrier semiconductor devices whose construction and principles of operation are fundamentally different from those of traditional bipolar transistors, which are minority carrier semiconductors.

The MOSFET is a voltage-controlled device. A voltage must be applied between the gate and source terminals to produce a flow of current in the drain, as illustrated in Figure 5.2.2.3-5. The gate is isolated electrically from the source by a layer of silicon oxide. Theoretically no current flows into the gate when a DC voltage is applied to it, although, in practice, there will be an extremely small leakage current, in the order of nanoamperes.

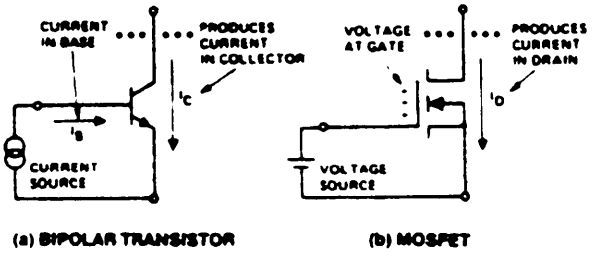


FIGURE 5.2.2.3-5: BIPOLAR TRANSISTOR IS CURRENT-DRIVEN, MOSFET IS VOLTAGE-DRIVEN

With no voltage applied between the gate and source electrodes, the impedance between the drain and source terminals is very high, and only a small leakage current flows in the drain until the applied voltage exceeds the drain-to-source avalanche voltage. This is illustrated in Figure 5.2.2.3-6.

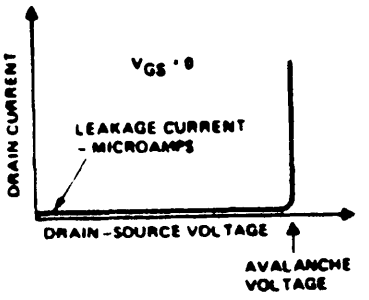


FIGURE 5.2.2.3-6: DRAIN-SOURCE BLOCKING CHARACTERISTIC

Currently available MOSFETs will conduct their rated continuous drain current, I_D, with less than 10 volts, V_{GS}, applied from gate-to-source. Conduction will begin before 3 volts, $V_{SG(th)}$, threshold voltage is applied to the gate. The threshold voltage is always greater than 1 volts, which allows leakage currents from a previous stage to be easily bypassed to ground. A cutoff condition of the power stage is thereby assured without any specification reverse-biasing. All units have a maximum junction operating temperature of 150°C.

One vendor's style MOSFET which is rated at 100v, 28A continuous and 70A pulsed has an on-resistance rating of 0.055 ohm, maximum. The typical on-resistance of this device, just 0.04 ohm, produces a 1.0v saturation drop @ 25A, which is low enough to compare with the $V_{CE}(SAT)$ of a bipolar transistor of similar size and lower than that of a Darlington transistor.

o Switching Times. MOSFET power transistors are much faster than bipolar power transistors of comparable size, principally because they do not have minority carrier delay times. The response times of MOSFETs are determined primarily by the device capacitances, and secondarily by such factors as the extremely short channel transit time of the electrons.

The input capacitance, C_{iss}, is the primary factor which determines the response time of a MOSFET. Although MOSFETs can be controlled by extremely low currents, i.e., high source impedances, the relatively long charge and discharge time of the input capacitance, C_{iss}, results in a tradeoff of response time against extreme sensitivity. A first order approximation of the response time of a MOSFET can be made by determining the time constant which results from the input capacitance times the effective source impedance.

Figure 5.2.2.3-7 shows typical switching waveforms of power MOSFET when driven by a 500 nanosecond-wide pulse. A good first order understanding of the switching response times, $t_{d(on)}$, t_r, $t_{d(off)}$, and t_f, can be made by considering the power MOSFET an ideal switch with a 3 volt "on" threshold. The output current can be considered controlled, without delay, by the instantaneous gate voltage which, in turn, is controlled by the time constant formed by $R_{input} \times C_{iss}$.

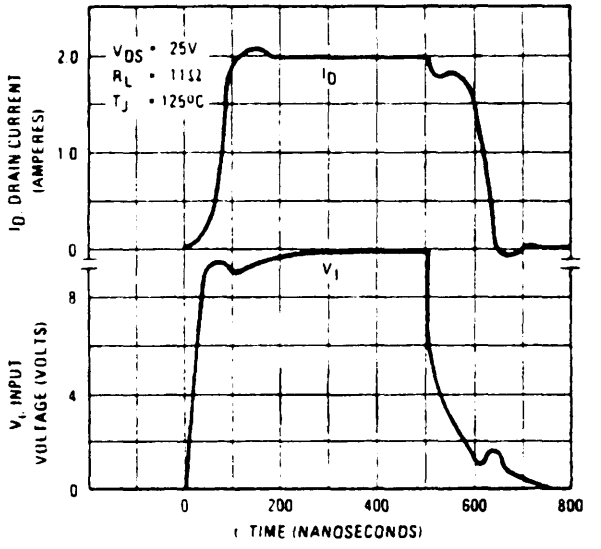


FIGURE 5.2.2.3-7: TYPICAL SWITCHING WAVEFORMS

o Simple Capacitive Speed-Up Circuit. Circuit techniques for forcing the charge on C_{iss}, give a means of controlling the response time of the MOSFET, or alternatively, the input impedance level at which a given response time occurs.

Figure 5.2.2.3-8 shows a simple gate "speed-up" circuit. The circuit produces a significant reduction in the switching times, at the expense of the need for an increased amplitude of input gate signal, and an increased, (but still comparatively low) current drain on the drive source. When switching on, the capacitor C initially provides a low impedance path for the applied gate pulse, bypassing the resistor R_2, and thus the input capacitance C_{iss} of the MOSFET is rapidly charged. When switching off, the capacitor C is charged positively on its left-hand terminal; the charged capacitor forces a discharge current through the input capacitance of the MOSFET, thus making it switch off rapidly.

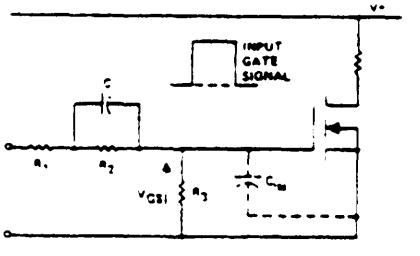


FIGURE 5.2.2.3-8: GATE SPEED-UP CIRCUIT

A point to remember about this gate speed-up circuit is that to be effective it requires an increase in the amplitude of the source signal voltage, because of the voltage dividing effect of R_3 with R_1 and R_2. Another point is that the resistor R_3 draws a continuous current from the gate drive source. Clearly it is desirable that the value of R_3 should be as high as possible. Figure 5.2.2.3-9 shows typical switching times for different values of R_3, for a given values of R_1, R_2 and C. It is seen that very fast switching times, in the order of 50 nanoseconds, can be obtained with the gate-to-source resistance R_3 as high as 10k ohms. This represents a continuous current drain on the gate drive source of about 1 mA. This is an order of magnitude lower than the drive current required for a comparably rated bipolar Darlington, which in any event exhibits switching times more than an order of magnitude longer.

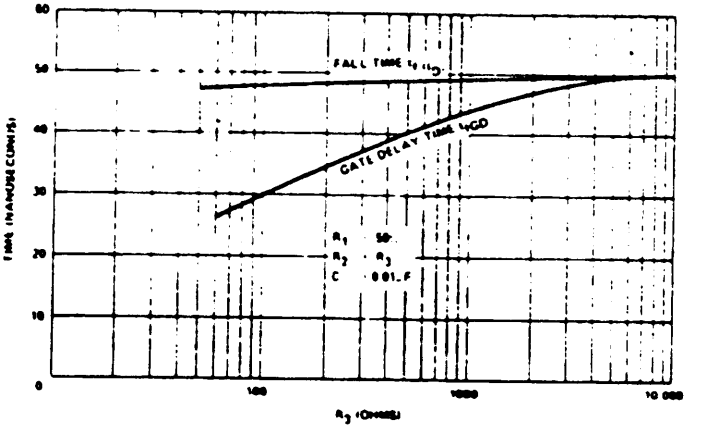


FIGURE 5.2.2.3-9: VALUES IN GATE SPEED-UP CIRCUIT AND SWITCHING TIMES

Figure 5.2.2.3-10 shows typical relationships between the switching speeds and the drain current, with and without a gate speed-up circuit. Note the drastic reduction in the turn of delay and fall times with the speed-up circuit, at drain current levels above 1A. The increase in the fall time at low levels of drain current is due to the drain-to-source capacitance, C_{oss}. The lower the drain current, the higher the load resistance R, and the greater the time constant R C_{oss}.

o Maximum Operating Frequency. Because the switching times of the power MOSFET are very fast, at least an order of magnitude faster than those comparably rated bipolar transistors, the energy dissipated during switching is very much lower, and the power MOSFET is able to operate at switching frequencies an order of magnitude or more higher.

Typical relationships between operating frequency and switching efficiency of power MOSFETs with a resistive load, are shown in Figure 5.2.2.3-11. This data is based upon actual measured values of switching energy at a supply voltage of 300v, and a 50% duty cycle. Figure

5.2.2.3-11 takes account of the losses in the power MOSFET itself, and not of other components in the circuit; it does not therefore represent the overall circuit efficiency. Clearly, as far as the MOSFET itself is concerned, switching frequencies up to 500kHz or higher are quite feasible. The switching efficiency is defined as:

$$\text{Switching Efficiency} = \frac{\text{Power Input - MOSFET losses}}{\text{Power Input}}$$

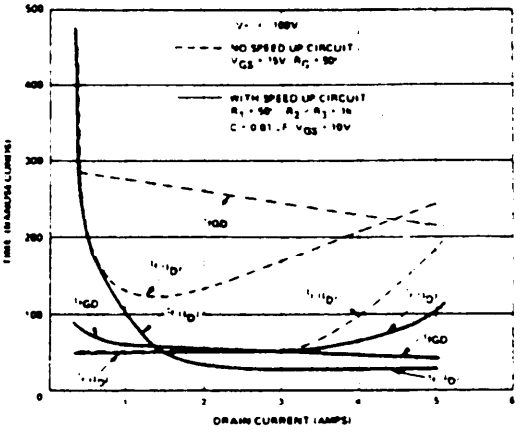


FIGURE 5.2.2.3-10: TYPICAL RELATIONSHIPS BETWEEN SWITCHING TIMES AND DRAIN CURRENT WITH AND WITHOUT GATE SPEED-UP CIRCUIT

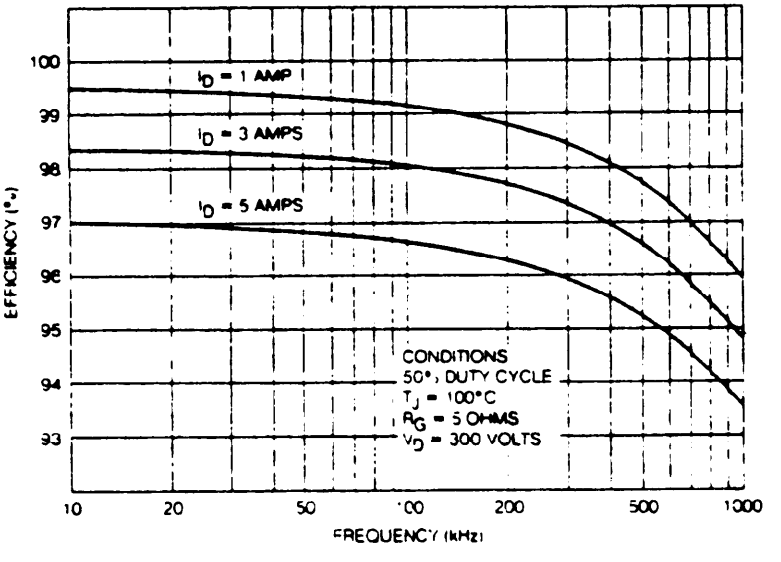


FIGURE 5.2.2.3-11: SWITCHING EFFICIENCY

o Safe Operating Area. One of the outstanding features of power MOSFETs is that they do not display the second breakdown phenomenon which is frequently the Achilles heel of bipolar transistors. A simple physical explanation accounts for this superiority. If localized, potentially-destructive, heating occurs within a MOSFET transistor, the carrier mobility in that area decreases. As a result the MOSFET has a positive temperature coefficient and acts in a self-protective manner by forcing currents to be uniformly distributed through the silicon die. In contrast a bipolar transistor, particularly under conditions of high collector-emitter voltage, displays "current crowding" in the base region, which causes hot spots. Because of the bipolar's negative temperature coefficient, these hot spots tend to further "hog" the current and cause instantaneous, catastrophic destruction of the die.

The absence of second breakdown means that the power MOSFET is generally a much more rugged device than the bipolar transistor. This is extremely important, both for "linear" and "switching" applications.

o Voltage Clamping. The V_{DS} absolute maximum rating of MOSFETs should not be exceeded by allowing them to operate in the avalanche region. However, it is possible to reliably turn off high level inductive currents, which can generate high voltage inductive transients, by using a simple voltage clamp circuit. Because MOSFETs are very fast devices, caution must be taken that the voltage clamp device has a sufficiently fast response, and that it is closely coupled to the drain-source terminals. A zener diode connected physically as close as possible to the drain and source terminals generally will provide acceptable voltage clamping. An example of a clamped inductive test circuit is given in Figure 5.2.2.3-12.

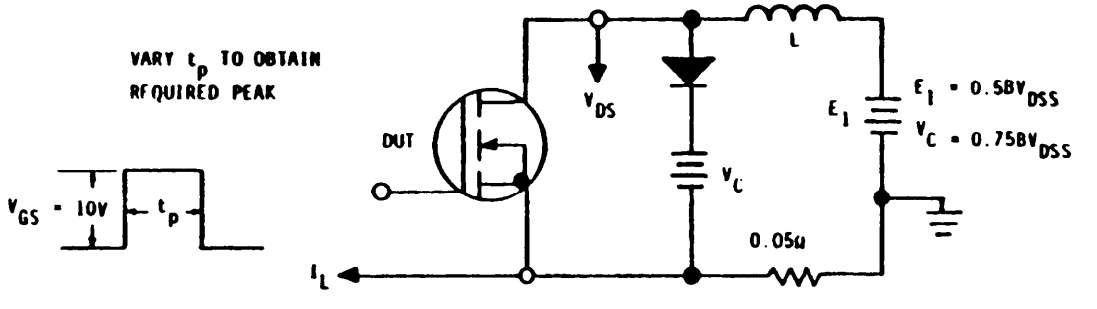


FIGURE 5.2.2.3-12: CLAMPED INDUCTIVE TEST CIRCUIT

o Temperature Stability. MOSFETs have outstanding gain and switching time stability with temperature variations, relative to the stability of typical bipolar transistors. The transconductance of power MOSFETs typically carries less than +20% from the 25°C value, over a -55°C to 125°C range. The DC current gain of a power bipolar transistor commonly varies by a factor of 2 or 3 over this temperature range.

A rough comparison of the typical DC gain stability for a power MOSFET versus a power bipolar would yield a transconductance, gfs, temperature coefficient of about -0.2% per °C versus a bipolar current gain, hFE, temperature coefficient of about +0.8% per °C, a four fold difference.

The switching time of power MOSFETs is essentially independent of operating temperature. This is a tremendous advantage relative to bipolar transistors, for which the 25°C switching times and associated power losses commonly increase by a factor of 2 or 3 at the higher actual operating temperatures. The extraordinary switching time stability of MOSFETs results because the response times are primarily dependent on the input capacitance, Ciss, which is essentially temperature invariant.

The on-resistance, RD(on) of power MOSFETs, has a positive temperature coefficient, of approximately +0.7% per °C. This is an advantage in paralleling MOSFETs, and as has been seen it also accounts for their excellent safe operating area. However, in determining the on-state power losses in a switching mode, the increased value of RD(on) at the actual maximum junction operating temperature must be used. Sufficient heatsink must always be used so that a thermal runaway situation cannot occur.

o Paralleling. Power MOSFETs are easy to parallel because the positive temperature coefficient forces current sharing among the paralleled devices. Current sharing resistors, with their associated power losses, are not necessary. Some resistance in series with the gates (typically 100 ohms) and close paralleled lead connections may be necessary to assure that the good high frequency response of the MOSFETs does not cause oscillations.

o MOS Caution. The +20 volt absolute maximum gate voltage rating of power MOSFETs should never be exceeded, or permanent damage can occur.

Zener diode protection should be used if there is a danger of transient gate overvoltages. This caution applies also to the buildup of static charge. Power MOSFETs have large gate capacitances and thick oxide layers relative to low level MOS devices, where static charge damage can be particularly dangerous. Though significantly more rugged than such low level MOS devices, reasonable precautions which are normally taken in handling MOS devices should be observed until the installation of MOSFETs in a circuit.

5.2.2.3.3 MICROWAVE SEMICONDUCTOR DEVICES

(a) Characteristics

The use of the microwave frequency range, i.e., from 1 GHz (10^9 Hz) up to 100 GHz and further, is becoming more common in present day communication systems. Low power (up to a few watts) solid state microwave devices are becoming more available. The high power microwave field is still dominated by vacuum tubes. The requirements relating to high power and high frequency semiconductor device design are often contradictory.

Some specially designed high frequency transistors can provide amplification at the lower microwave frequencies; however, transient time and other effects limit the application of transistors beyond the 10^9 Hz range. Therefore, devices other than solid state semiconductors are required to perform electronic functions such as amplification and d-c to microwave power conversion at higher frequencies.

Several high frequency devices use the inherent instability characteristics which occur in semiconductors. One such instability is the acousto-electric effect involving the high frequency interaction between electrons and the lattice vibrations of certain crystals. There are other types of instabilities, including "negative conductance." The most common negative conductance devices are: Impact Avalanche Transit Time (IMPATT) diodes, which depend on a combination of impact ionization and transit time effects, and Gunn diodes which depend on the transfer of electrons from a high mobility state to a low mobility state. Each is a two terminal device which can be operational in a negative conductance mode to provide amplification or oscillation at microwave frequencies.

(b) Use of Si vs GaAs for Microwave Applications

As a semiconductor, gallium arsenide is more attractive for microwave devices than silicon for two reasons:

o The electron mobility in GaAs is several times higher than in Si. This shortens transit times and increases the high frequency capability of these devices.

o GaAs can withstand higher working temperatures due to its larger band gap. This is particularly important in the very small geometry devices used in microwaves that must dissipate a lot of power.

There are, however, serious drawbacks in using GaAs. GaAs technology is lagging behind that of Si. A complicated structure such as a bipolar transistor cannot be made to a high enough standard of quality and repeatability, especially as minority carrier. Life times are very short and base width must therefore be very narrow. A majority carrier device, however, similar to a JFET, where operation does not depend on surface effect and oxide can be made with present day technology. This device which is called a MESFET has a cutoff frequency of 35 GHz for a channel length of 1um. Such a device is a good small signal microwave amplifier. If a wide enough channel and good heat sinking is used, it can also serve as a power amplifier; power outputs of several watts at frequencies up to 15 GHz can be obtained.

(c) The IMPATT Device

This device is commonly used for power generation at microwave frequencies because of its small size, reliability and output power. Calculation of the IMPATT device input impedance depends on the impurity profile, on knowledge of the ionization coefficients for holes and electrons and their dependence on the field. Efficiencies as high as 30% were achieved in GaAs devices. Output power as high as 10W (CW) at 10 GHz can also be obtained. This is higher than any other semiconductor device can deliver today at this frequency. One important drawback is the noise inherent in the IMPATT ionization process which can interfere with the signal in some frequency ranges.

(d) The Gunn or Transferred Electron Device (TED)

Microwave devices which operate by the transferred electron mechanism are called Gunn diodes after J. B. Gunn, who first demonstrated one of the forms of oscillation. Basically, the device is made from a piece of GaAs with N+ regions for contacts. In the transferred electron mechanism, the conduction electrons of some semiconductors are shifted from a state of high mobility to a state of low mobility by the influence of a strong electric field.

Gunn diodes and related devices are simple structures in principle, since they are basically homogeneous samples with ohmic contacts on each end. In practice, however, considerable care must be taken in fabricating and mounting workable devices. In addition to the obvious requirements of doping density, carrier mobility, and sample length, there are important considerations relating to contacts, heat sinking, and parasitic reactances of the packaged device.

Removal of heat is a very serious problem in these devices. The power dissipation may be 10^7 W/CM^3 or greater, resulting in considerable heating of the device. As the temperature increases, the device characteristics vary because of changes in carrier concentration and mobility. As a result of such heating effects, these devices seldom reach their theoretical maximum efficiency. Pulsed operation allows better control of heat dissipation than does continuous operation, and efficiencies near the theoretical limits can sometimes be achieved in the pulsed mode. The limited space charge accumulation (LSA) mode is particularly suitable for microwave power generation because of its relatively high efficiency and high operating frequencies. If the application does not require continuous operation, peak powers of hundreds of watts can be achieved in pulses of microwave oscillation.

5.2.2.4 DERATING

Circuits should be designed with the semiconductors derated as suggested in Tables 5.2.2.4-1 and 5.2.2.4-2. The extent to which electrical stress (e.g., voltage, current, power or fanout) is derated is dependent upon temperature. The general interrelationship between electrical stress and temperature is shown in Figure 5.2.2.4-1. The best operating conditions lie within the area below the benign limitation line (ES_B). Operation at conditions between the benign limitation line and the severe limitation (ES_S) curves results in lower reliability (see MIL-HDBK-217).

Numerical values are applied to the curves for each part type based upon a percentage of the device manufacturer's maximum rated values.

TABLE 5.2.2.4-1: DERATING FACTORS FOR TRANSISTORS

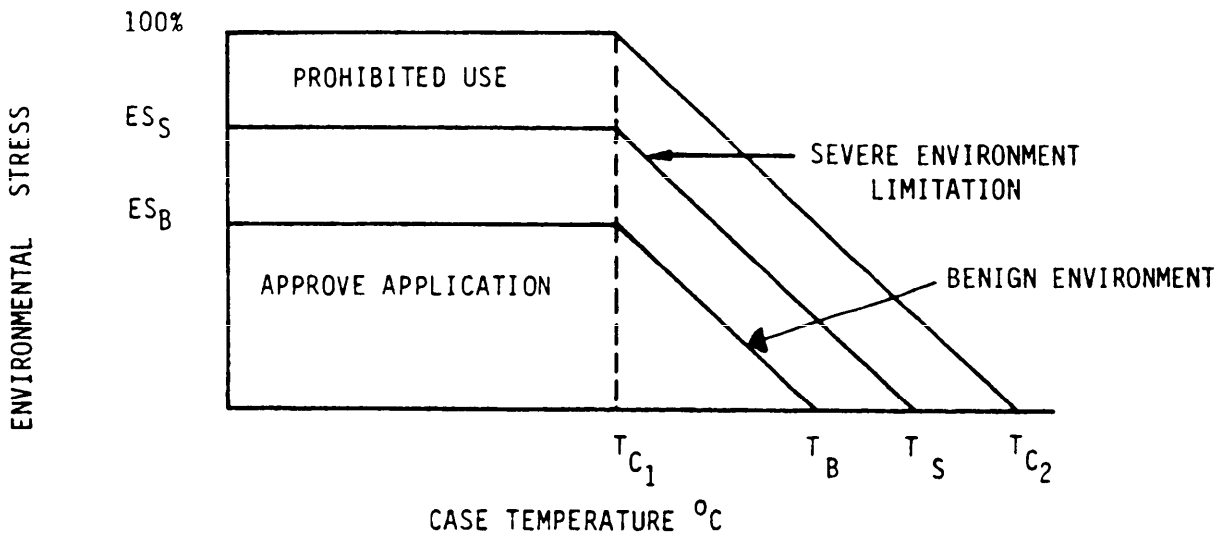
Transistor Type	Parameter	Environmental Derating Factor Benign	Severe
All Silicon Types	Power	0.70	0.50
	Max Junc. Temp(^{o}C)	125	0.95
	Breakdown Volt	0.70	0.60

TABLE 5.2.2.4-2: DIODE DERATING

Diode Type	Environmental Derating Factor Benign	Severe	Parameter
Light Emitting	110	95	Max Junc Temp (^{o}C)
	0.75	0.50	Avg. Forward Current
Rectifier (Power)	125	95	Max Junc. Temp (^{o}C)
	0.70	0.70	PIV
	0.75	0.50	Forward Current
Switching	0.70	0.50	Power
	0.70	0.70	PIV
	125	95	Max Junc Temp (^{o}C)
	0.75	0.50	Forward Current
Varactor	0.50	0.70	Power
	0.75	0.80	PIV
	0.75		Forward Current
Voltage Reference*	125	95	Max Junc Temp (^{o}C)
	0.70	0.50	Power
Transient Suppressor	0.75	0.50	Avg. Current
	0.70	0.50	Power
	125	95	Max Junc Temp (^{o}C)
Microwave	125	95	Max Junc Temp (^{o}C)
	0.70	0.70	PIV or
	0.70	0.50	Power

* The zener current should be limited to no more than $I_z = I_z$ nominal + 0.5 (I_z maximum - I_z nominal), but do not derate to the point where the device is operating at the knee.

The worst case combination of ac, dc, and transient voltages shall be no greater than the allowed percentage of rated voltage.



WHERE:

T_{C_1} = Case temperature above which applied electrical stress must be reduced.

T_{C_2} = Maximum allowable case temperature per detailed specification.

T_B = Benign boundary limitation.

T_{WC} = Severe thermal boundary.

ES_B = Benign Environmental Stress.

ES_S = Severe Environmental stress including electrical transient and radiation effects.

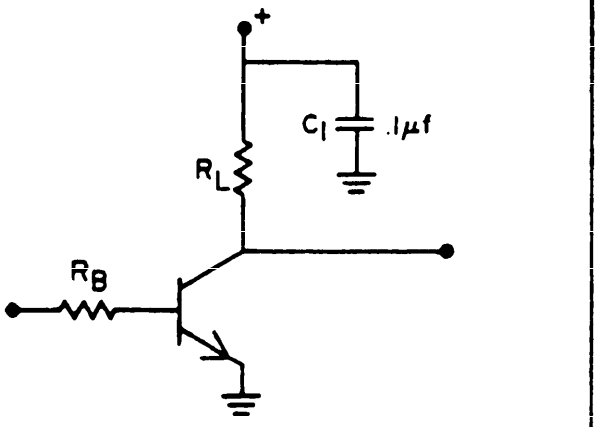
100% = Maximum rated value per detailed specification.

FIGURE 5.2.2.4-1: STRESS TEMPERATURE DERATING SCHEME

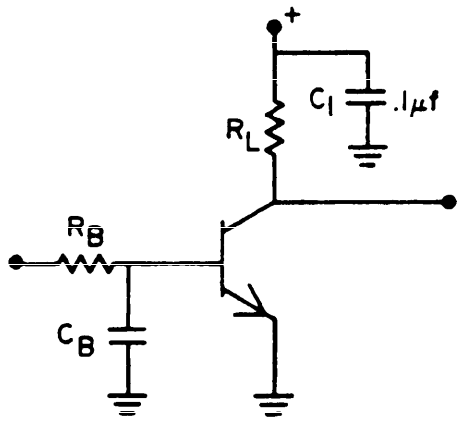
o Transient Suppression for Semiconductors. There are many techniques available for transient suppression. Some of these are illustrated in Figures 5.2.2.4-2 through 5.2.2.4-8 and apply in the following areas:

- o Transistors
- o SCRs
- o CMOS
- o TTL Protection
- o Diode Protection

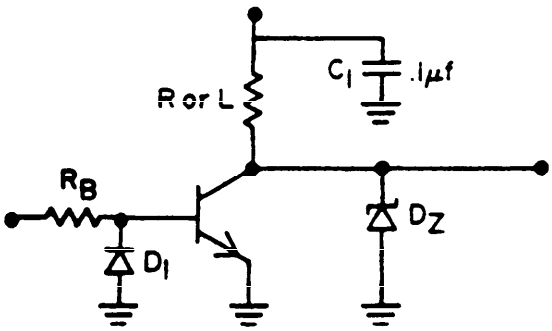
These techniques are representative of generally applicable methods and are not intended as an exhaustive list.



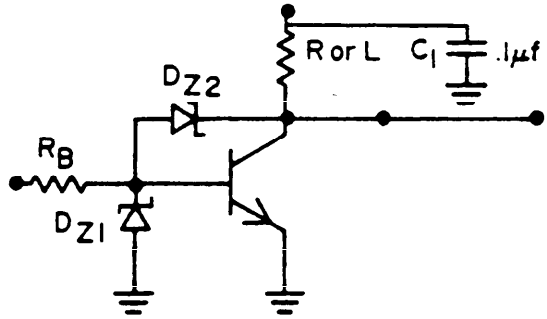
(A) Current Limiting Resistor (R_B) And Transient Suppression Capacitor (C_1)



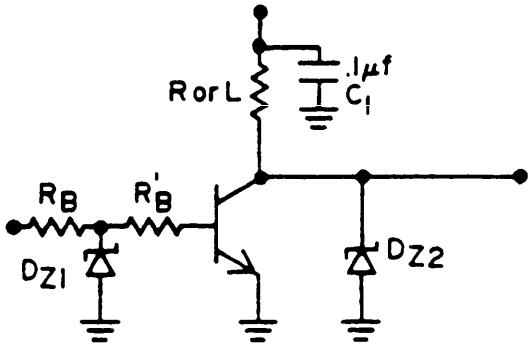
(B) Low Gain Filter (R_B, C_B) And Transient Suppression Capacitor (C_1)



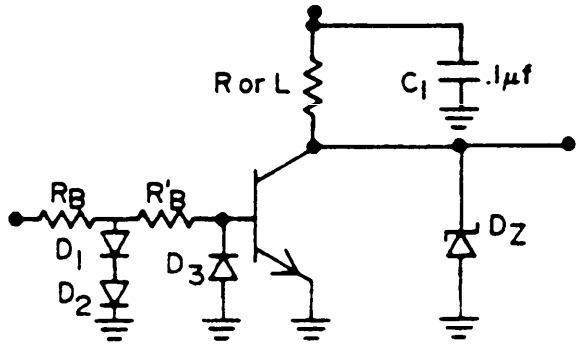
(C) Transient Limiter (R_B, D_1, D_Z) And Transient Suppression Capacitor (C_1)



(D) Transient Suppression For Base And Collector (R_B, D_{Z1}, D_{Z2})

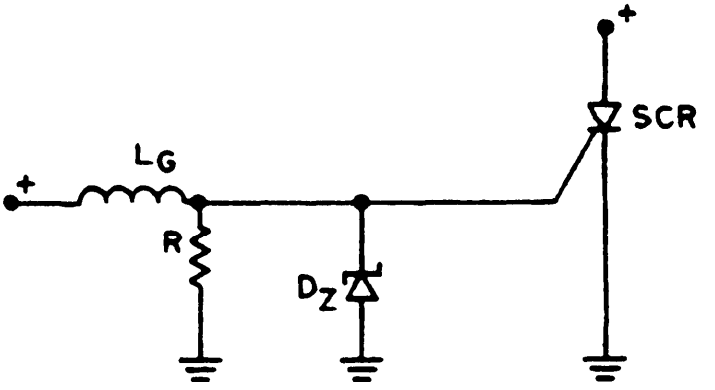


(E) Reverse And Forward Transient Limiter (R_B, D_{Z1}, D_{Z2}) And Transient Capacitor

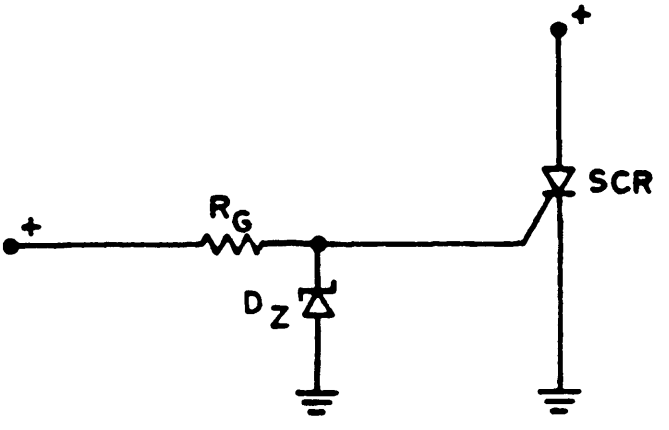


(F) Complete Transient Protection (R_B, D_1, D_2, D_Z, C_1)

FIGURE 5.2.2.4-2: TRANSISTOR PROTECTION

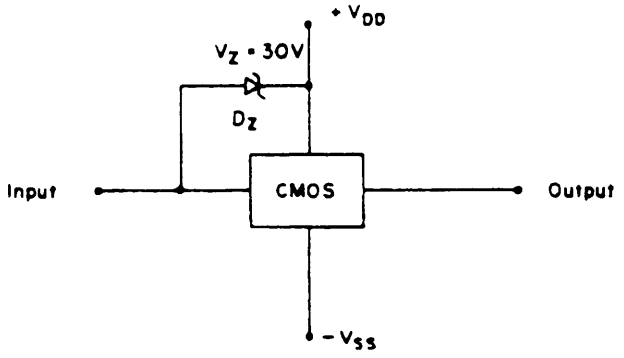


(A) Integrator (L_G, R) Serves To Limit The Initial Surge Current When The Gate Is Turned On. Diode D_Z Protects Against Voltage Transients. The PIV of the SCR Should Be Chosen To Provide Sufficient Anode To Cathode Protection.

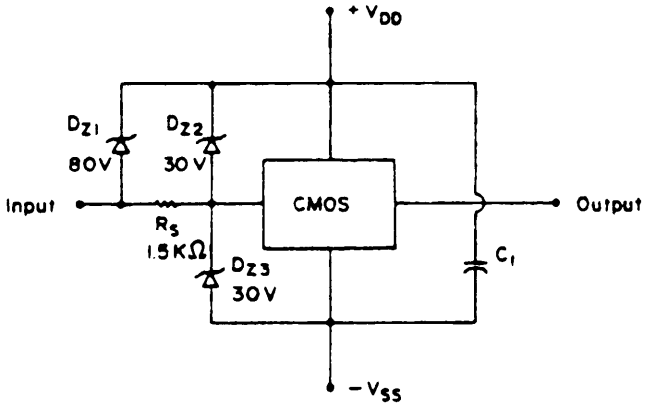


(B) Resistor R_G Limits The Gate Current Of The SCR and Diode D_Z Protects The Gate Against Voltage Transients

FIGURE 5.2.2.4-3: SCR PROTECTION



a) Single Diode Clamps Positive Input Voltage To V_{DD} And Negative Input Voltages To V_{DD} - 30 Volts Thus Preventing Gate Breakdown.



b) Diode D_{Z2} And D_{Z3} Clamps Positive Input To V_{DD} And Negative Input To V_{SS}. Diode D_{Z1} And R_S Provide Time Delay And Current Limit Action. Capacitor C_1 Prevents High Frequency Transient From Entering The Device Through The Power Supply.

FIGURE 5.2.2.4-4: CMOS PROTECTION

a) Store Unused Devices In Conductive Foam Or Use Any Method That Shorts All Leads Together

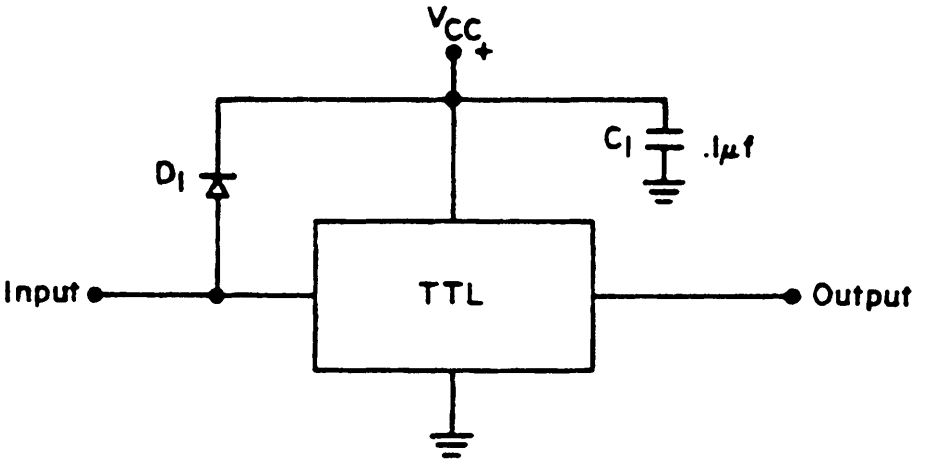
b) Use Grounded Soldering Iron

c) Ground All Test Equipment

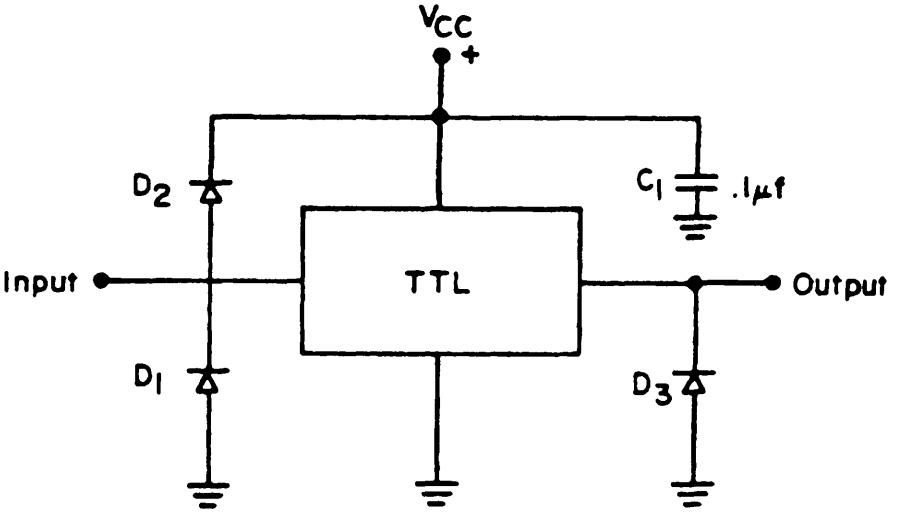
d) All Unused Device Inputs Should Be Connected To V_{DD} Or V_{SS}

e) All Low Impedance Equipment Should Be Disconnected From Device Inputs Before DC Power Supplies Are Turned Off

FIGURE 5.2.2.4-5: CMOS HANDLING PRECAUTIONS

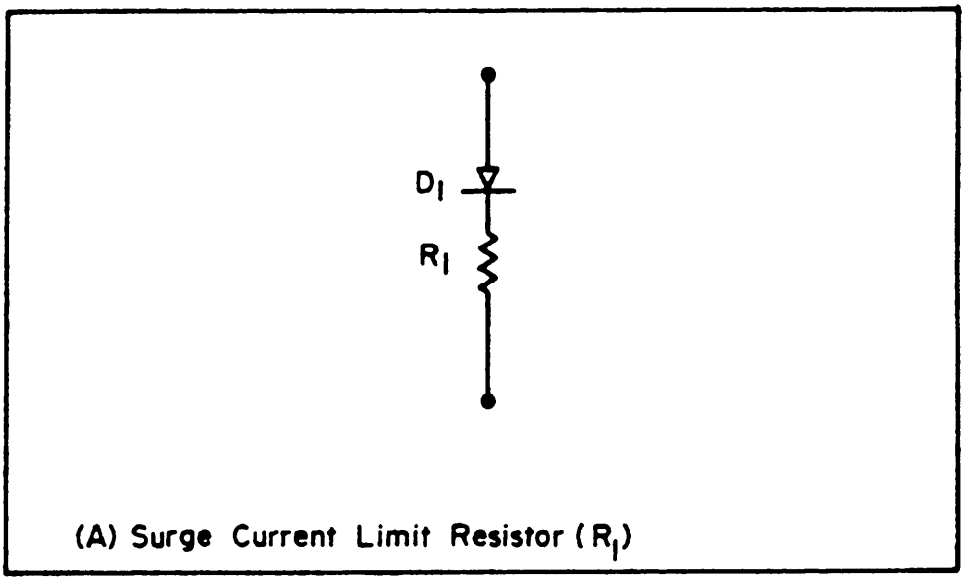


(A) Diode D_1 Prevents Input From Becoming Greater Than V_{CC} And Capacitor C_1 Absorbs High Frequency Transients On The Power Supply Line

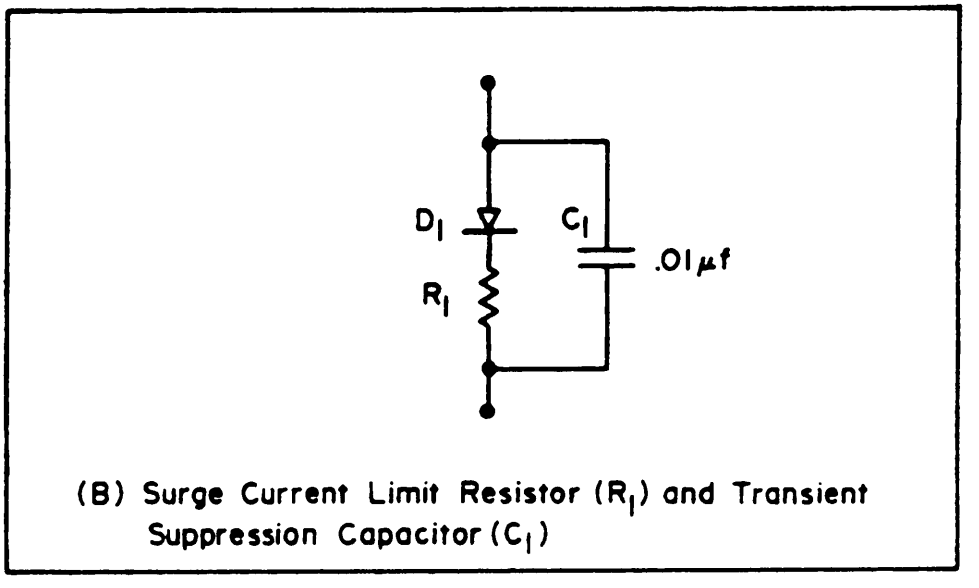


(B) Diodes D_1 And D_2 Clamp The Positive Input To V_{CC} And The Negative Input To Ground. Diode D_3 Prevents The Output From Going Below Ground C_1 Absorbs High Frequency Transients On The Power Supply Line.

FIGURE 5.2.2.4-6: TTL PROTECTION



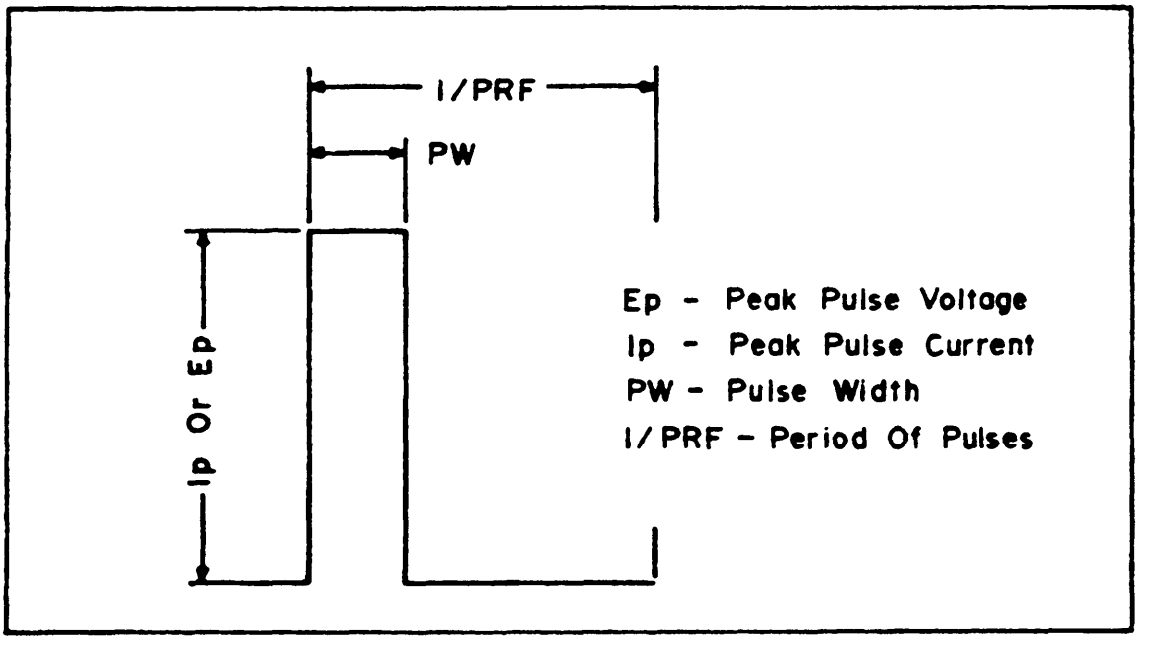
(A) Surge Current Limit Resistor (R_1)



(B) Surge Current Limit Resistor (R_1) and Transient Suppression Capacitor (C_1)

Note: The Best Protection For A Diode Is Sufficient Overrating Of The Reverse Breakdown Voltage (PIV), Forward Surge Current (I_S) And Power DissipationCapability (P)

FIGURE 5.2.2.4-7: DIODE PROTECTION



Power Of The Pulse :		$P_{pulse} = (Ip) \times (Ep)$
	Or	$P_{pulse} = (Ep)^2/R$
Energy Of The Pulse :		$E_{pulse} = (P_{pulse}) \times (PW)$
Average Power Of The Pulse :		$P_{avg.} = (P_{pulse}) \times (PW)/(1/PRF)$
Duty Factor Of The Pulse :		$DF = PW/(1/PRF)$

FIGURE 5.2.2.4-8: PULSE WAVEFORM

REFERENCES

1. Wojnas, E.J. (RADC, GAFB, NY 13441), "Electrical and Reliability Characterization of Schottky Power Diodes," (RADC-TR-81-38), April, 1981.

2. Pelly, B.R. "Applying International Rectifier's Power MOSFETs," International Rectifier Application Notes, No. AN-930.

5.2.3 RESISTORS

5.2.3.1 INTRODUCTION

Resistors are functionally classified as fixed and variable. Resistor construction is of three general types: composition, film or wirewound, and consists of a resistive element mounted on a base (chassis) with environmental protective coating and external electrical leads to allow insertion into an electrical circuit. Composition resistors are made from a mixture of resistive material and a binder and are molded into a shape and a specific resistance value. Film resistors consist of a resistive film deposited inside or outside an insulating cylinder. The wirewound type is composed of resistive wire wound on an insulative body. These three basic types of resistors differ from each other in reliability, size, cost, resistance range, power rating and general characteristics. No one type has all the best characteristics. The choice among them depends on initial and long-term operating requirements, the environment in which they must exist, and other factors.

5.2.3.2 SELECTION

As a generic class of electronic devices, resistors have been well documented by MIL specifications and standards. Consequently, a selection from among a variety of available standard types and styles can be made. For economic reasons, standard resistors are normally produced in large production runs, making the selection of standard devices even more attractive. Note, however, that there are exceptions. Extremely tight-tolerance fixed resistors and certain precision type variable resistors, which require a unique output voltage curve, taps or stacking configuration, may be difficult or expensive to procure or may possess questionable reliability. Standard resistors are specified in MIL-STD-199. This standard presents detailed data for use in the design of military equipment. Resistor selection is governed by the criteria given in Table 5.2.3.2-1. Usage and selection guidelines appear in Table 5.2.3.2-2.

TABLE 5.2.3.2-1: RESISTOR SELECTION CRITERIA

1.	MIL-STD-199 "Resistors, Selection and Use Of"
2.	The 39000 series of Established Reliability military specifications.
3.	MIL specifications on resistors
4.	Historical test data (similar application) or other engineering information and/or data that provides assurance that the device is sufficiently rugged and reliable for the application (e.g., previous use in military equipment, comparable application or GFE).

NOTE: For selecting particular resistors for specific applications, the qualified product list should be consulted for a list of qualified sources prior to procurement commitment.

TABLE 5.2.3.2-2: USAGE AND SELECTION GUIDELINES FOR RESISTORS

Military Specifications	Type	Styles	Usage Notes	Failure Modes
Fixed Resistors				
MIL-R-11	Composition, insulated	Inactive for new design. Use MIL-R-39008		
MIL-R-26	Wire-wound (power type)	RW29 RW37 RW31 RW38 RW33 RW47 RW35 RW57	See data on MIL-R-39007	
MIL-R-93	Wire-wound (accurate)	Inactive for new design. Use MIL-R-39005		
MIL-R-10509	Film (high stability)	RN75	See data on MIL-R-55182	
MIL-R-11804	Film (power type)	RD60 RD65	Use where power dissipation equivalent to MIL-R-39007 are required and where ac performance must be considered. RD60, RD65, and RD70 are considered uninsulated.	SHORTS - Humidity or salt air can cause shunt paths on surface of resistor and shorting between sprials. OPENS - Can be caused by mechanical damage. Operation at RF above 100 MHz may produce inductive effects on spiralled units.
MIL-R-18546	Wire-wound power type (chassis mounted)	RE77 RE80	See data on MIL-R-39009	
MIL-R-22684	Film (insulated)	Inactive for new design. Use MIL-R-39017		
MIL-R-39005	Wire-wound (accurate) ESTABLISHED RELIABILITY	RBR52 RBR56 RBR53 RBR57 RBR54 RBR71 RBR55 RBR72	Styles RBR52, 53, 54, 55, and 71 are preferred for new design. Preferred resistance tolerances are ± 0.1% and ±1.0%.	SHORTS - Application of over-voltage can cause insulation breakdown between windings. OPENS - Resistors employ plastic or ceramic bobbins which are subject to mechanical damage, resulting in open windings. Operation over 50 kHz can produce inductive and intrawinding capacitive effects.
MIL-R-39007	Wire-wound (power type) ESTABLISHED RELIABILITY	RWR74 RWR81 RWR78 RWR84 RWR80 RWR89	Use for large power dissipation where ac performance is not vital (e.g., as voltage dividers, or bleeders in power supplies). Satisfactory for use at frequencies up to 20 kHz even though the ac characteristics are not controlled. The use of tapped resistors should be avoided; the insertion of taps weakens the resistor mechanically and lowers the effective power rating. Resistors are not suitable for use above 50 kHz.	SHORTS - Rarely occur, but can happen due to intrawinding insulation breakdown. OPENS - Usually occur due to mechanical damage suffered by the resistor or from winding burnout due to the wattage rating or the rated continuous working voltage being exceeded.

TABLE 5.2.3.2-2: USAGE AND SELECTION GUIDELINES FOR RESISTORS (Cont'd)

Military Specifications	Type	Styles	Usage Notes	Failure Modes
		Fixed Resistors		
MIL-R-39008	Composition (insulated) ESTABLISHED RELIABILITY	RCR05 RCR07 RCR20 RCR32 RCR42	Use for general application where initial tolerance needs to be no tighter than ± 5% and long term stability under fully rated operating conditions needs to be no better than ± 15%. Resistance increased up to 20% during storage in humidity. Operation of the resistor at rated load will drive out the moisture and bring the resistor value back to within tolerance.	Both shorts and opens very rarely occur unless resistor is so over-loaded or over-heated as to cause the phenolic case or thermo-setting binder material to carbonize. In high impedance circuits, the failure mode is generally a short; in low impedance circuits, the failure mode is open. High "JOHNSON" noise levels are present in resistor values above 1.0 megohm. DRIFT - RF will produce capacitance effects end-to-end. Operation at VHF or higher frequency reduces effective resistance due to dielectric losses (the "Boello" effect).
MIL-R-39009	Wire-wound (power type) ESTABLISHED RELIABILITY	RER40 RER60 RER45 RER65 RER50 RER70 RER55 RER75	Use where a lower tolerance and a greater power dissipation is required for a given unit size than is provided by MIL-R-39007 resistors and where ac performance is not critical. The power dissipation capacity of these resistors is dependent upon the area of heat sink upon which it is mounted.	SHORTS - May occasionally occur due to intrawinding insulation breakdown. OPENS - May occasionally occur due to damage to the winding, poor winding to terminal connection, etc., suffered during fabrication.
MIL-R-39017	Film (insulated) ESTABLISHED RELIABILITY	RLR05 RLR07 RLR20 RLR32 RLR42	Resistors have semi-precision characteristics and small sizes. The sizes and wattage ratings are comparable to MIL-R-39008 and MIL-R-55182. Full power operating temperature should not exceed 70°C. Resistance-temperature characteristic is ± 200 PPM/°C.	SHORTS or OPENS may occur if resistor is poorly fabricated or over-loaded in application. Operation at RF above 100 MHz may produce inductive effects on spiral-cut types.
MIL-R-55182	Film ESTABLISHED RELIABILITY	RNR50 RNR55 RNR60 RNR65 RNR70	Use where high stability, long life, reliable operation and accuracy are required. Resistors are particularly suited for high frequency applications. Application examples include: high-frequency, tuned circuit loaders, television side-band filters, rhombic antenna terminators, radar pulse equipment, and metering circuits.	SHORTS - May occasionally occur because of protuberances on adjacent resistance spirals. OPENS - May occasionally occur due to non-uniform spirals resulting in a too-thin resistance path. Operation at 400 MHz and above will result in resistance decrease due to shunt capacitance effects.
MIL-R-55432	Film, chip ESTABLISHED RELIABILITY	RM0502 RM0505 RM0705 RM1005 RM1505 RM2208	Use in hybrid microelectronic circuits. These resistors are uncased leadless chip devices and shall not be procured for logistics support.	Subject to excessive loss of resistance (> 50%) due to electrostatic discharge effects.

TABLE 5.2.3.2-2: USAGE AND SELECTION GUIDELINES FOR RESISTORS (Cont'd)

Military Specifications	Type	Styles	Usage Notes	Failure Modes
			Fixed Resistors	
MIL-R-83401	Film, Network	RZ010 RZ020 RZ030 RZ040 RZ050	Use where accuracy, stability, small size, long life and reliable operation are important considerations. Resistance elements may be interconnected electrically and arranged in any circuit configuration.	Subject to resistance decrease due to shunt capacitance effects if used at frequencies of 200 MHz and above.
			Variable Resistors	
MIL-R-19	Wire-wound (low operating temperature)	RA20 RA30	Use for noncritical, low power, low frequency applications where the characteristics of wirewound devices are more desirable than those of composition. Common applications are bias controls and voltage dividers. Wattage rating depends upon the size and type of heat sink unit is mounted on. Resistors have high inductance between windings.	Variable resistors as a class of components share many common failure modes: 1. Wire-wound units are self inductive, (winding-to-winding), causing resistance drift and affecting circuit accuracy. 2. Wire-wound units suffer shorts between winding loops due to insulation breakdown or contaminants which bridge the insulation. 3. Windings will rupture with sufficient wear by the wiper arm, resulting in an open circuit. 4. All variable reisistors can suffer movement of the wiper on the resistance element as the result of shock or vibration. In critical applications, the resultant change of the output voltage can constitute a "failure" of the resistor. 5. Non-wire-wound units become noisier with wear life and will suffer resistance change due to humidity. 6. Power ratings for all variable resistors are based upon the engagement of the maximum resistance by the wiper. Excessive currents can be drawn when less-than-maximum resistance is engaged, resulting in a burn-out of the resistance element.
MIL-R-22	Wire-wound (power type)	RP05 RP06 RP10 RP15 RP20 RP25 RP30	Use in such applications as motor speed controls; lamp dimming; heater and oven controls; potentiometric uses; applications where voltage or current variation is required, such as voltage-divider or bleeder circuits.	
MIL-R-94	Composition (insulated)	RV4 RV6	Rate for full-load operation at 70°; otherwise SEE DATA ON MIL-R-23285.	
MIL-R-12934	Wire-wound, precision	RR0900 RR1000 RR1100 RR1300 RR1400 RR2000 RR2100 RR3000	Use in applications requiring close conformity of the electrical output (in terms of applied voltage) to the angular position of the wiper arm on the resistance element. This functional conformity (whether producing a linear or nonlinear output curve with shaft rotation) is available in tolerances ranging from 0.025% through 1.0%. Power rating is dependent on the size and type of heat sink upon which resistor is mounted.	
MIL-R-23285	Composition (insulated)	RVC6	Use where initial setting stability is not critical and long term stability needs to be no better than +20%. Rated for full load operation at 125°C.	

TABLE 5.2.3.2-2: USAGE AND SELECTION GUIDELINES FOR RESISTORS (Cont'd)

Military Specifications	Type	Styles	Usage Notes	Failure Modes
		Variable Resistors		
MIL-R-22097	Non-wire-wound (lead-screw actuated)	RJ12 RJ24 RJ22 RJ26 RJ50	See data on MIL-R-39035	Variable resistors as a class of components share many common failure modes. (See preceding page.)
MIL-R-27208	Wire-wound (lead-screw actuated)	RT26	See data on MIL-R-39015	
MIL-R-39002	Wire-wound semi-precision	RK09	Use where the precision needed is better than that supplied by MIL-R-19 units and less than that supplied by MIL-R-12934 units. Power rating is dependent on size and type of heat sink upon which resistor is mounted.	
MIL-R-39015	Wire-wound (lead-screw actuated) ESTABLISHED RELIABILITY	RTR12 RTR22 RTR24	Use for matching, balancing, and adjusting circuit variables in critical applications. For extremely critical applications, use in conjunction with a fixed resistor, so that change in wiper setting due to shock or vibration limits output voltage change to a negligible minimum.	
MIL-R-39035	Non-wire-wound (lead-screw actuated) ESTABLISHED RELIABILITY	RJR12 RJR14	Same as MIL-R-39015	
		Thermistors		
MIL-T-23648	Film, thermistor (insulated)	RTH	Use for temperature compensation, control or measurement.	Subject to drift due to moisture absorption Heat generated while soldering resistor leads to terminal points can permanently change the resistance-temperature characteristics of the unit.

5.2.3.3 GENERAL APPLICATION DATA

5.2.3.3.1 RESISTOR MOUNTING

Resistor mounting plays an important role in resistor reliability. The mounting determines to a large extent how thermal stress, shock and vibration are transmitted from the environment to the resistor. Mounting guidelines are presented below.

o Large resistors should be provided with some adequate means of mounting other than the leads. Under conditions of vibration or shock, lead failure can occur, and the larger the mass supported by the leads the more probable it is that leads will fatigue. Even when vibration or shock is not a serious problem, ease of assembly and replaceability suggest that large components be individually mounted. Resistors should be mounted in such a manner that the body of the resistor is restrained from movement with respect to the mounting base. It should be noted that the heat dissipating qualities of the resistor can be enhanced or retarded depending on whether the clamping material is a good or poor heat conductor.

o Maintain lead lengths to a minimum. The lead contacts with the printed circuit board act as a heat sink.

o Where temperature variations are present, leads should be offset (bent slightly) to allow for thermal contraction and expansion.

o Close tolerance and low value resistors require special precautions (i.e., short leads and good soldering techniques) since the resistance of the leads and/or a poor solder joint could comprise several percent of the resistance of the resistor.

o When resistors are mounted in rows or banks, they should be so spaced that, taking into consideration the restricted ventilation and heat dissipation of nearby resistors, no resistor in the row or bank exceeds its maximum permissible hot spot temperature. An appropriate combination of resistor spacing and resistor power rating should be chosen if this is to be assured.

o For resistors mounted in series, the heat being conducted through the leads to the next resistor should be considered.

o Large power resistors should be mounted on a metal chassis for heat dissipation.

o Do not mount power type resistors directly on terminal or printed circuit boards without heat sinks.

o To provide for the most efficient operation and even heat distribution, power resistors should be mounted in a horizontal position.

o Select mounting materials that will not char, and design mounts so they withstand strain due to thermal expansion and contraction.

- Consider proximity to other heat sources as well as self heat.

- A resistor that dissipates over two watts can char a terminal board. A charred board will have a lower insulation resistance than an uncharred board.

- Supplementary insulation should be used if a resistor normally mounted directly onto a chassis is to be used at a higher potential above ground than is specified for the resistor. However, the mounting must still be able to dissipate the generated heat.

- Assembly techniques can affect resistor reliability. Resistors should never be overheated by excessive soldering iron heat, and the resistor leads should not be abraded by assembly tools. Normal soldering practice should include heat sinking to the extent that the resistor will not be physically damaged or its resistance value changed from the soldering operation.

- When choosing a variable resistor, take care to ensure that the power rating of the unit will be sufficient to handle the higher current produced when the resistance is reduced.

5.2.3.3.2 TEMPERATURE EFFECTS

Inadequate heat dissipation is the predominant cause of failure for any type of resistor. Figure 5.2.3.3-1 depicts the manner in which heat is dissipated from fixed resistors in free air. The lowest possible resistor surface temperature should be maintained using radiation, conduction, and convection to the fullest extent to accomplish the necessary dissipation. Under normal atmospheric conditions (25°C, 30 in. Hg), resistors up to two watts dissipate heat in the following proportions: 10 percent radiation, 40 percent convection and 50 percent conduction through leads. Resistors with substantially larger wattage ratings, by virtue of increased surface area, dissipate heat in proportions of: 50 percent radiation, 25 percent convection and 25 percent conduction.

Resistors should be chosen so that, when mounted in equipment, they will not be required to operate at a temperature in excess of their rating even under the following conditions:

- In the maximum specified ambient temperature.

- With maximum temperature rise in each resistor.

- With all enclosures in place.

- At high altitude.

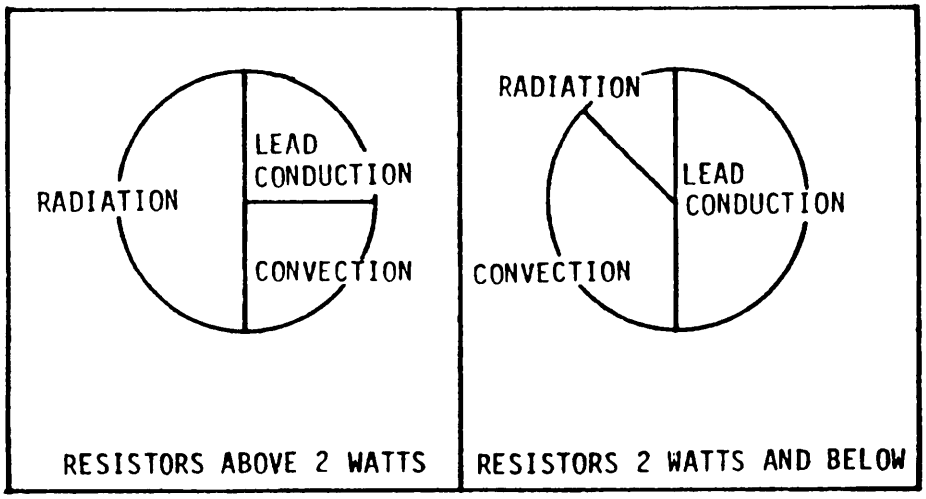


FIGURE 5.2.3.3-1: HEAT DISSIPATION FROM FIXED RESISTORS IN FREE AIR

Thermal dissipation guidelines for the three methods of heat transfer include:

a. Radiation considerations:

- o Maximize spacing between resistors to reduce cross radiation heating effects.
- o Place resistors so that adjacent large metallic areas are so located as to absorb significant amounts of radiated heat.
- o Use vented or similar types of body clamps on larger size resistors.

b. Conduction considerations:

- o Use resistors with thick leads and minimum length.
- o Terminate resistor leads at tie points of sufficient mass to perform the function of a heat sink.
- o Mount large size resistors with body clamps to large metallic masses.

c. Convection considerations:

- o Use the maximum possible spacing between resistors to allow reduced resistance to air flow.
- o Orient resistors and provide baffles where needed for exposure to air flow by both natural and forced convection.

5.2.3.3.3 FORM FACTORS AND PREFERRED RESISTANCE VALUE

For physical form and preferred resistance values of each resistor style, see MIL-STD-199 or the appropriate resistor detailed military specification.

5.2.3.3.4 VARIABLE RESISTORS

The use of variable resistors is not recommended for high reliability applications. Since these resistors are not hermetically sealed, they are susceptible to degraded performance due to the ingestion of soldering flux, cleaning solvents and conformal coatings during equipment fabrication. Also variable resistors contain moving parts that wear with use. The reliability of variable resistors is relatively low when compared to fixed resistors. When variable resistors must be used, the following precautions should be followed:

o Enclosed units should be used to keep out as much dust and dirt as possible and to protect the mechanisms from mechanical damage. The presence of lubrication oil can cause dust or wear particles to concentrate within the unit.

watts can char a terminal board

o A resistor that dissipates over two

o It is necessary to prevent unwanted movement of the wiper arm on the resistance element. For resistors which are not in continuous use, a short locked shaft with a slotted end is preferred. For continuous use, a high torque shaft will limit the amount of motion due to shock, vibration, and accidental movement. Where it is absolutely necessary to have a long shaft, a coupled extension is preferred to one long integral shaft. Regardless of the type of shaft, the use of oversize control knobs which permit high rotational torque will generally result in damage to the integral stop. Use the smallest size knob to reduce applied torque.

o When a variable linear resistor is being used as voltage divider, the output voltage through the wiper will not vary linearly if current is being drawn through it. This characteristic is usually called the "loading error." To reduce the loading error, the load resistance should be at least 10 to 100 times as great as the end-to-end potentiometer resistance.

o In potentiometer applications the load current as well as the "bleeder" current will be flowing through a part of the resistor and will contribute to the heating effect.

5.2.3.3.5 COMPOSITION RESISTORS, GENERAL APPLICATION CONSIDERATIONS

Composition resistors are small, inexpensive and have good reliability when properly used. They have poor resistance stability, high noise characteristics and appreciable voltage and temperature coefficients. They do, however, have good high frequency characteristics although this characteristic is not controlled by specification. Other application considerations of composition resistors include:

o The fact that there are voltage limits in the application of composition resistors is often overlooked. These maximum permissible voltages, which are specified in the applicable MIL specifications and in MIL-STD-199, are imposed because of insulation breakdown problems and should be considered in addition to the specified power dissipation limits.

o Exposure to humidity may have two effects on the resistance value: (1) Surface moisture can result in leakage paths which will lower the resistance values, or (2) absorption of moisture into the element may increase the resistance. These phenomena are more noticeable in higher resistance ranges. When exposed to high humidity, either operating at low power levels or during shelf storage, equipment nonoperating status, or shipping, resistance value can change by as much as 15 percent.

o Resistor characteristics can be permanently damaged by exposure to high operating temperatures.

o When composition resistors are used under low duty cycle pulse conditions, the maximum permissible operating voltage is limited by breakdown rather than by heating. In such applications the peak value of the pulse should not exceed 2 times the rated rms continuous working voltage for the resistor used. In general, the peak power should not be more than approximately 30 to 40 times the normal power rating.

o Thermal agitation or Johnson noise and resistance fluctuations or carbon noise, present only when current is flowing, are characteristic of carbon composition resistors. Use of these resistors, in low level, high resistance (1 megohm or more) circuits should be avoided. The expected noise level is approximately 3 to 10 microvolts per volt. A film or wirewound resistor will usually yield lower noise levels.

o When used in high frequency circuits (1 megahertz and above), the effective resistance will decrease as a result of dielectric losses and shunt capacitance (both end-to-end and distributed capacitance to mounting surface). High frequency characteristics of carbon composition resistors are not controlled by specification.

o All properties of a composition resistor may be seriously affected when soldering irons are applied too close to a resistor body or for too long a period. The length of lead between the resistor body and the soldering point should not be less than ¼ inch. Heat dissipating clamps should be used when soldering resistors in close quarters. In general, if it is necessary to unsolder a resistor to make a circuit change or during maintenance, the resistor should be replaced by a new one.

o Fixed composition resistors exhibit little change in effective dc resistance up to 100 KHz. Resistors with values above .3 megohms start to decrease in resistance at approximately 100 KHz. Above a frequency of 1 MHZ, resistors of all values exhibit decreased resistance. However, the resistor operates as a pure resistance free from any reactive component into the megacycle region.

o Nominal minimum resistance tolerances available for fixed composition resistors are ±5 percent. Combined effects of climate and operation on unsealed types can raise this tolerance to ±15 percent. These effects include aging, pressure, temperature, humidity and voltage gradient.

o Composition elements of variable resistors can wear away after extended use, leaving particles of the element to permeate the mechanism. This can result in warmer operation and high resistance shorts within the variable resistor.

o Variable composition resistors should not be used at potentials to ground or case greater than 500 volts peak unless supplementary insulation is provided.

5.2.3.3.6 FILM RESISTOR, GENERAL APPLICATIONS CONSIDERATIONS

Film type resistors are highly stable and demonstrate the best high frequency performance of all resistor types. The effective dc resistance for most resistance values remains fairly constant up to 100 MHz and decreases at higher frequencies. In general, the higher the resistance value the greater the effect of frequency. Other application considerations are:

o Some lower power, tighter tolerance film resistors are quite susceptible to electrostatic damage. (See Section 6.1.6, Volume 2; DOD-STD-1686; DOD-HDBK-263).

o When metal film resistors are used in low duty cycle pulse circuits, peak voltage should not exceed 1.4 times the rated continuous working voltage (RCWV). However, if the duty cycle is high or the pulse width is appreciable, even though average power is within ratings, the instantaneous temperature rise can be excessive, requiring a resistor of higher wattage rating. Peak power dissipation should not exceed four times the maximum rating of the resistor under any conditions.

o Film resistors are recommended for use where high stability and close tolerance resistance values are required. That is, where the resistance value must be accurately maintained over a broad range of temperature or for long periods of equipment storage and operation. Regardless of the purchase tolerance (nominally $\pm$ 1% or less), the design should be able to tolerate a $\pm$ 2% shift in resistance to assure long life reliability in military applications. Minimum resistance tolerance available is 0.1 percent.

o The resistance-temperature characteristics of film resistors is fairly low ($\pm$ 500 PPM/^{o}C and $\pm$ 200 PPM/^{o}C) for thick film types RD and RLR and very low ($\pm$ 25 PPM/^{o}C) for metal film types RN and RNR.

o Operation at radio frequencies above 100 MHz can produce inductive effects on spiral-cut types.

o Operation at reduced frequency may produce inductive effects on spiral-wound types; skin inductive effects are negligible.

o Exposure to moisture can seriously affect this type of resistor if not protected by molded or ceramic casing or internal deposition of the resistance element.

o Carbon-film resistance elements are susceptible to physical damage; hermetic seals are preferred for film-type resistors.

o The noise level of variable film resistors is quite low compared to variable composition resistors.

Since under conditions of shock, vibration or acceleration the wiper arm can move along the resistance element of variable film units, thus changing the voltage output of the resistor, care should be taken to lock the resistor shaft in place.

5.2.3.3.7 WIREWOUND RESISTORS, GENERAL APPLICATION CONSIDERATIONS

o Wirewound resistors have inductive and capacitive effects and are normally unsuited for use above 50 KHz. Wirewound resistors usually exhibit an increase in resistance with high frequencies because of the "skin" effect.

long a period. The length of lead between the resistor body and the

o Although some resistors are constructed using reverse Pi-winding, Ayrton-Perry or bifilar winding to reduce inductance, they are not designed for high frequency applications where ac performance is of critical importance.

o Wirewound, power resistors have high stability, medium temperature coefficient, high reliability, negligible voltage coefficient, poor high frequency characteristics, negligible noise and are capable of dissipating considerable heat.

o Wirewound, accurate resistors are physically large and costly when compared to composition types of the same power rating. They exhibit very high stability, negligible voltage coefficent, and good high frequency characteristics to 50 KHz maximum.

o Application of voltages in excess of the voltage rating can cause insulation breakdown between the windings.

o Wirewound power variable resistors are generally not supplied in low tolerances, since most applications for this type do not require accurate resistance.

o The use of tapped resistors is to be avoided because insertion of taps weakens the resistor mechanically and lowers the effective power rating.

o The presence of moisture may degrade coating or potting compounds used in these resistors.

o Although power type wirewound resistors can reliably withstand pulse voltages of much greater amplitude than permitted for steady state operation, care should be taken not to exceed the specified maximum voltage limits. The pulse power and average power must not exceed the derated value determined by the derating requirements.

o Fixed, wirewound, accurate resistors are physically the largest of all types for a given resistance and power rating, since they are very conservatively rated. Due to their size and weight, in applications where severe shock or high frequency forces are encountered, the bodies of these resistors should be constrained from movement.

o Variable wirewound resistors have the lowest temperature coefficient and greatest stability of any potentiometer.

o Due to the stepping action of the wiper from wire to wire on the resistance element, variable wirewound resistors have the highest electrical noise characteristic of all variable resistors.

5.2.3.4 MIL-R-19, RESISTORS, VARIABLE, WIREWOUND (LOW OPERATING TEMPERATURE) (STYLE RA)

5.2.3.4.1 SPECIAL APPLICATION CONSIDERATIONS

o Selection of a Safe Resistor Style - The wattage ratings of these resistors are based on operation at 40°C, mounted on a 16 gage steel plate, 4 inches square. This mounting technique should be taken into consideration when the wattage is applied during specific applications. For other types of mountings, the ratings must be properly modified.

o Choice of Linear and Nonlinear Tapers - The application shall dictate the choice between linear (Taper A) and non-linear (Taper C) resistance elements.

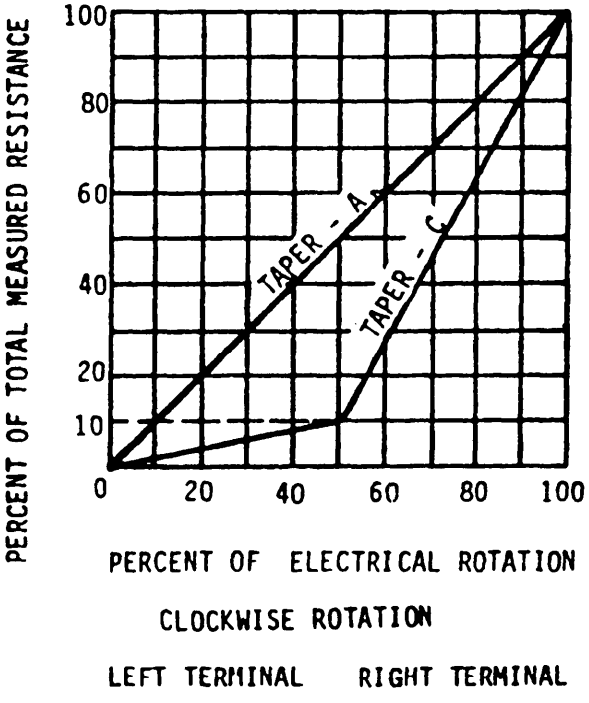


FIGURE 5.2.3.4-1: RESISTANCE TAPERS

o Derating - For reliable performance this style resistor should be operated at 50% of its absolute maximum wattage rating. The absolute maximum rating curve and the recommended minimum derating curve are shown below. The maximum ambient operating temperature should be limited to 85°C.

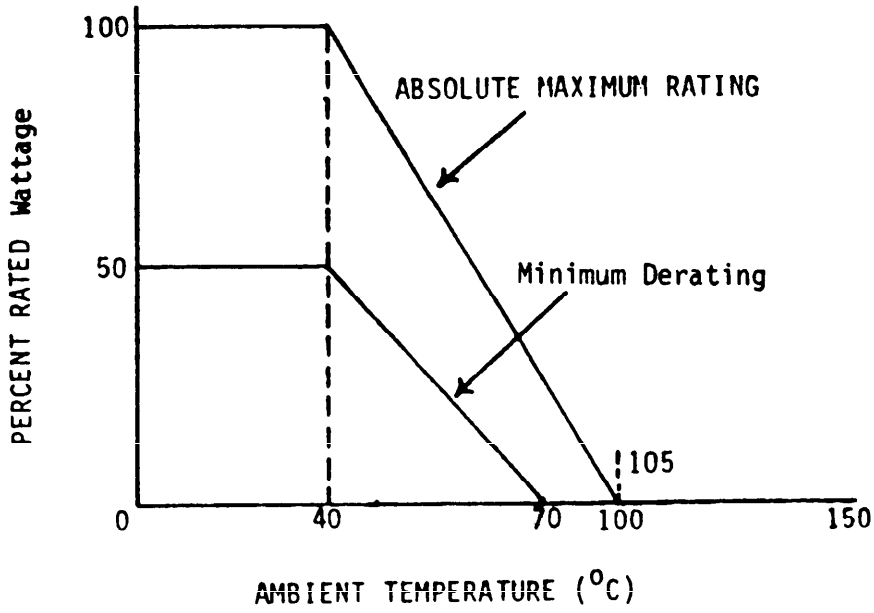


FIGURE 5.2.3.4-2: DERATING CURVE

5.2.3.5 MIL-R-22, RESISTORS, VARIABLE, WIREWOUND (POWER TYPE) (STYLE RP) (UNENCLOSED)

5.2.3.5.1 SPECIAL APPLICATION CONSIDERATIONS

o Selection of a Safe Resistor Style - The wattage ratings of these resistors are based on operation at 25°C, mounted on a 12" square steel panel, .063" thick (4" square x 0.050" for RP05 and RP06). This mounting technique should be taken into consideration when the wattage is applied during specific applications. For other types of mountings, the ratings should be properly modified.

o Supplementary Insulation - These resistors should not be used at potentials above ground greater than 500 volts (250 volts for RP05 and RP06) unless supplementary insulation is used.

o Electrical Off Position - Care should be exercised in specifying the electrical off position when resistors are required to break dc circuits having potentials in excess of 40 volts.

o Derating - For reliable performance this style resistor should be operated at 50% of its absolute maximum wattage rating. The absolute maximum rating curve and the recommended minimum derating curve are shown below.

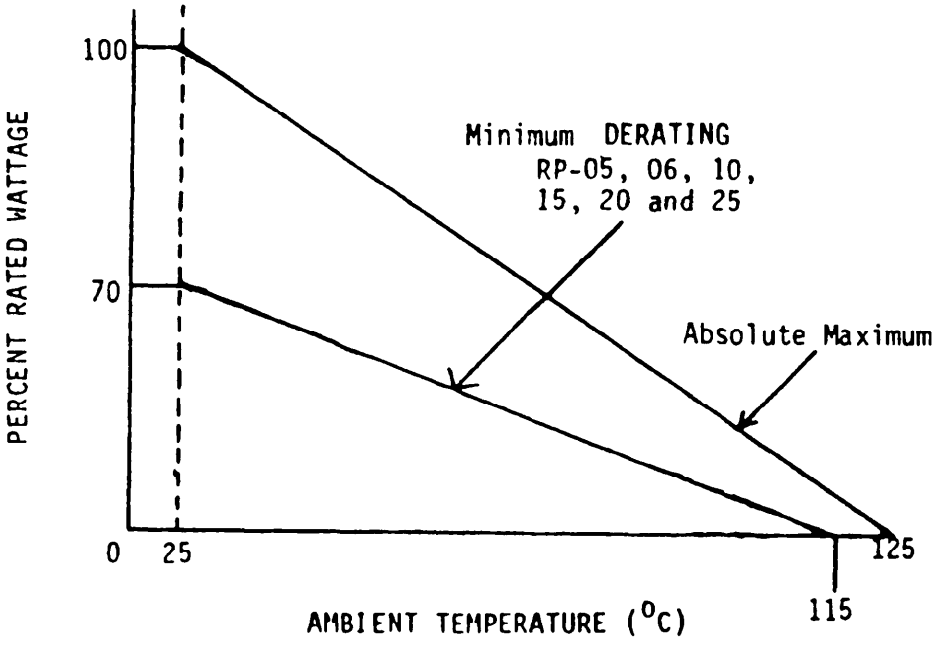


FIGURE 5.2.3.5-1: DERATING CURVES

5.2.3.6 MIL-R-26, RESISTORS, FIXED, WIREWOUND (POWER TYPE) (STYLE RW)

5.2.3.6.1 SPECIAL APPLICATION CONSIDERATIONS

o Substitution - use MIL-R-39007 Style RWR resistors instead of MIL-R-26 Style RW when practicable.

o Operating Temperature - The maximum operating temperature is limited to 200°C. Above 200°C, the resistors are subject to "outgassing" of the volatile materials used in their fabrication.

o Derating - For reliable performance this style resistor should be operated at 50% of its absolute maximum wattage rating. The absolute maximum rating curve and the recommended 50% derating curve are shown below. The maximum ambient operating temperature should be limited to 200°C.

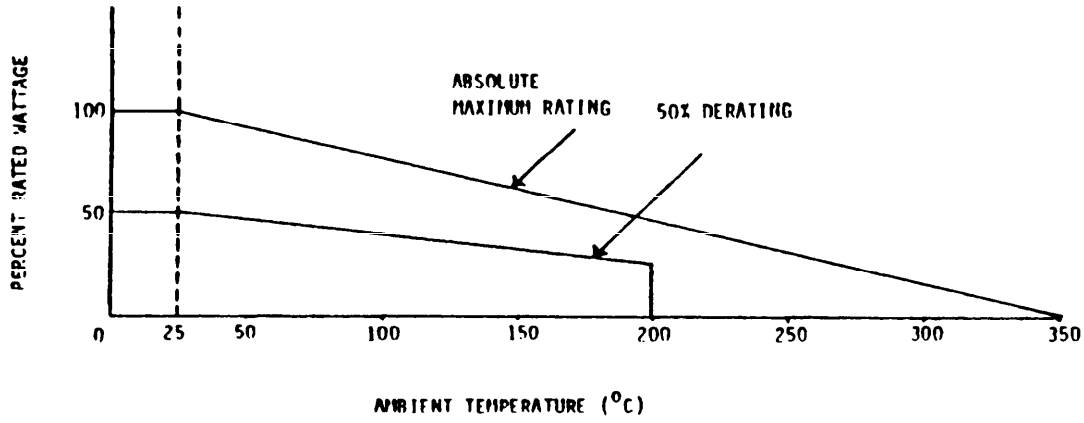


FIGURE 5.2.3.6-1: DERATING CURVE

5.2.3.7 MIL-R-94, RESISTORS, VARIABLE, COMPOSITION (STYLE RV)

5.2.3.7.1 SPECIAL APPLICATION CONSIDERATIONS

o Selection of Bushing - Non-locking type bushings should be used whenever possible to assure longer life.

o Shelf Life - An average resistance change (R) of 20% per year under normal storage conditions is estimated.

o Derating - For reliable performance this style resistor should be operated at 50% of its absolute maximum wattage rating. The absolute maximum rating curve and the recommended minimum derating curve are shown below. The maximum ambient operating temperature should be limited to 100°C.

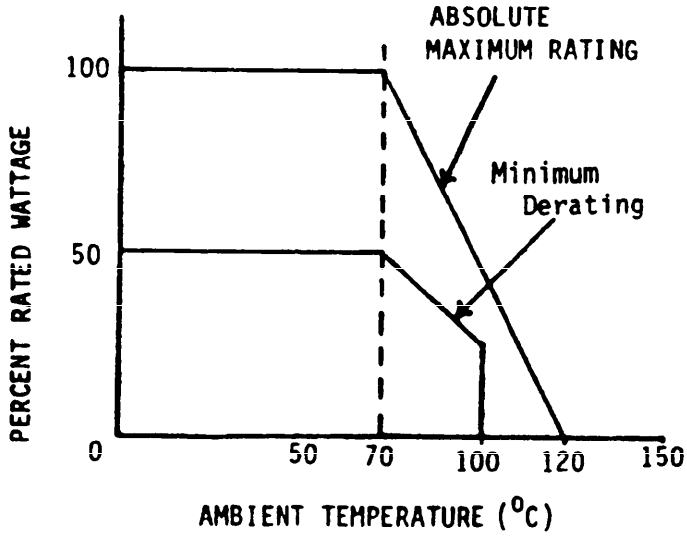


FIGURE 5.2.3.7-1: DERATING CURVE

5.2.3.8 MIL-R-11804, RESISTORS, FIXED, FILM (POWER TYPE) (STYLE RD, UNINSULATED)

5.2.3.8.1 SPECIAL APPLICATION CONSIDERATIONS

o Characteristics - These resistors have good stability, low voltage coefficients, low noise, low inductance and low capacitance. These resistors are suitable for use in high frequency circuits, bridges and various test equipment, such as high gain amplifiers and pulse circuits.

o Derating - For reliable performance this style resistor should be operated at 50% of its absolute maximum wattage rating. The absolute maximum rating curve and the recommended 50% derating curve are shown below. The maximum ambient operating temperature should be limited to 200°C.

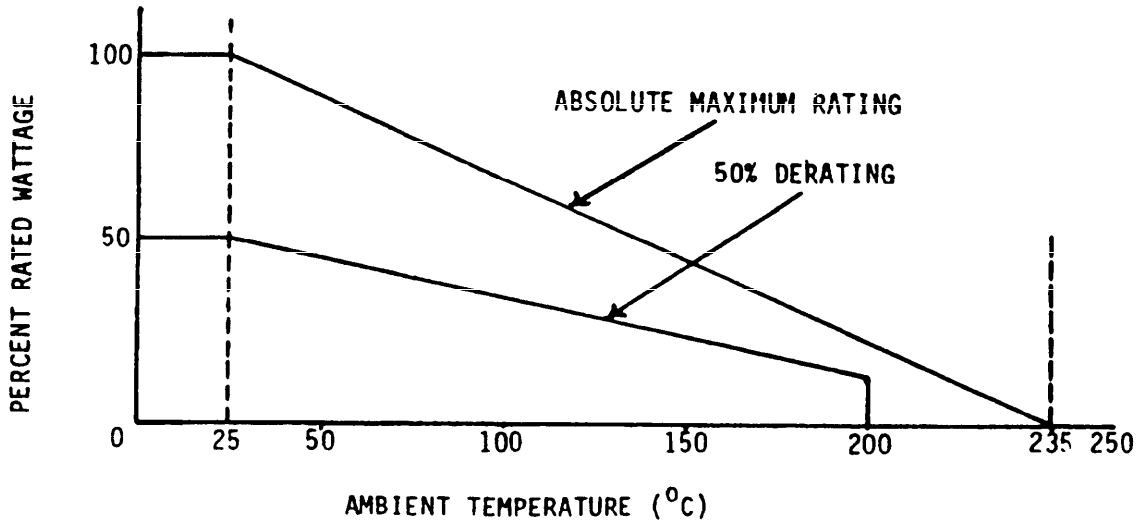


FIGURE 5.2.3.8-1: DERATING CURVE

5.2.3.9 MIL-R-12934, RESISTORS, VARIABLE, WIREWOUND, PRECISION (STYLE RR)

5.2.3.9.1 SPECIAL APPLICATION CONSIDERATIONS

o Selection of a Safe Resistor Style - The wattage rating of these resistors is based on operation at 85°C, mounted on a 4" square, 0.25" thick alloy aluminum panel. This mounting technique should be taken into consideration when calculating the wattage dissipated during specific applications. When other types of mountings are employed, the wattage ratings should be properly modified.

o Bushings - Use a non-locking type bushing whenever possible to assure longer life.

o Derating - For reliable performance this style resistor should be operated at 50% of its absolute maximum wattage rating. The absolute maximum rating curve and the recommended minimum derating curve are shown below. The maximum ambient operating temperature should be limited to 130°C.

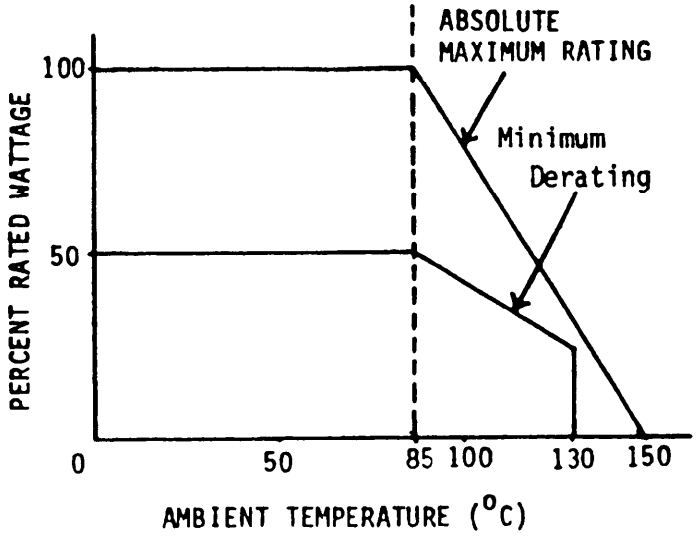


FIGURE 5.2.3.9-1: DERATING CURVE

5.2.3.10 MIL-R-18546, FIXED, WIREWOUND, (POWER TYPE, CHASSIS MOUNTED) (STYLE RE)

5.2.3.10.1 SPECIAL APPLICATION CONSIDERATIONS

o Substitution - Use MIL-R-39009 Style RER resistors instead of MIL-R-18546 Style RE when practicable.

o Operating Temperature - The maximum operating temperature is limited to 185°C, since above 185°C the resistors may be subject to "outgassing" of the volatile materials used in their fabrication.

o Derating - For reliable performance this style resistor should be operated at 50% of its absolute maximum wattage rating. The absolute maximum rating curve and the recommended 50% derating curve are shown below. The maximum ambient operating temperature should be limited to 150°C.

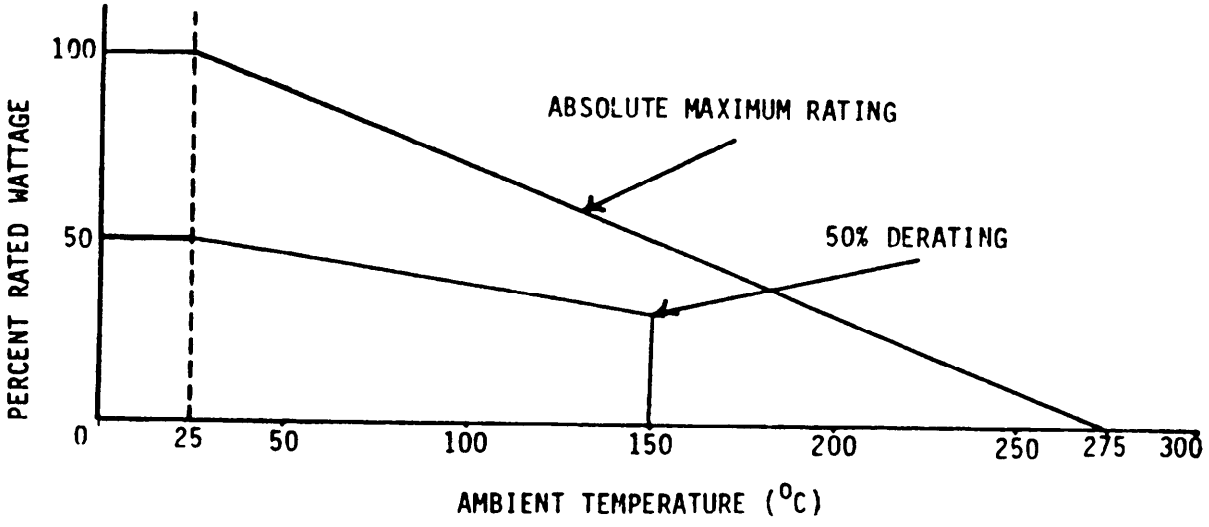


FIGURE 5.2.3.10-1: DERATING CURVE

5.2.3.11 MIL-R-22097, RESISTORS, VARIABLE, NONWIREWOUND (ADJUSTMENT TYPE) (STYLE RJ)

5.2.3.11.1 SPECIAL APPLICATION CONSIDERATIONS

o Substitution - Substitute MIL-R-39035, Type RJR for MIL-R-22097, Style RJ, whenever practicable.

o Derating - For reliable performance this style resistor should be operated at 50% of its absolute maximum wattage rating. The absolute maximum rating curve and the recommended minimum derating curve are shown below. The maximum ambient operating temperature should be limited to 120°C.

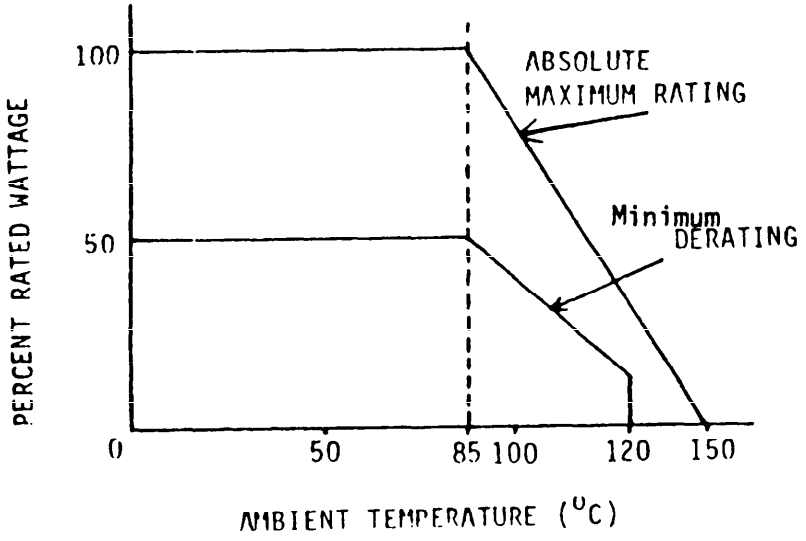


FIGURE 5.2.3.11-1: DERATING CURVE

5.2.3.12 MIL-R-23285, RESISTORS, VARIABLE, NONWIREWOUND (STYLE RVC)

5.2.3.12.1 SPECIAL APPLICATION CONSIDERATIONS

These resistors are suitable for rheostat or potentiometer applications, where high precision is not required. They are capable of withstanding acceleration, shock, high frequency vibration and 125°C operating temperature at rated load. They are most useful in circuitry where high resistance values and lower power dissipation are encountered in controlling volume, bias, tone voltage output and pulse width.

o Selection of Safe Resistors - The wattage ratings of these resistors are based on operation at 125°C, mounted on a 16-gage steel plate, 4" square. This mounting technique should be taken into consideration when the wattage is applied during specific applications. When using other types of mountings, the power ratings should be properly modified.

o Choice of Linear and Nonlinear Tapers - The application shall dictate the choice between linear (Taper A) and non-linear (Taper C) resistance elements.

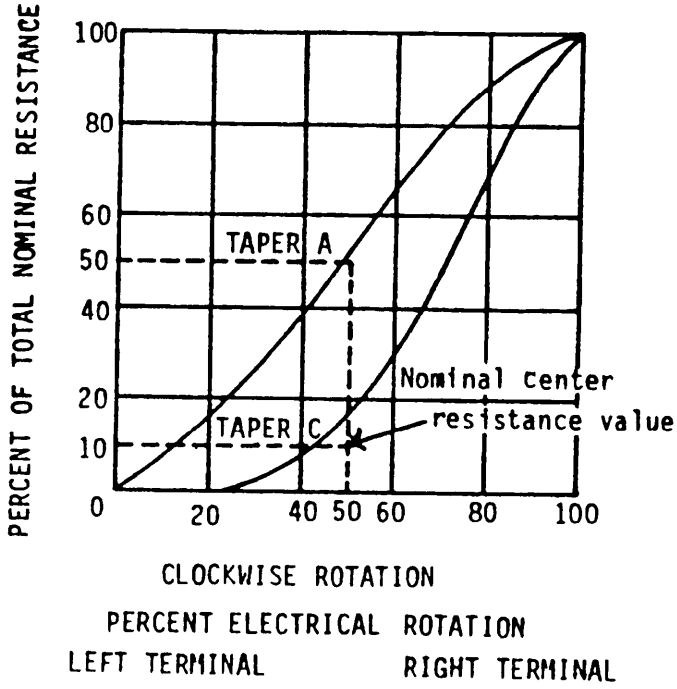


FIGURE 5.2.3.12-1: RESISTANCE TAPERS

o Derating - For reliable performance this style resistor should be operated at 50% of its absolute maximum wattage rating. The absolute maximum rating curve and the recommended 50% derating curve are shown below. The maximum ambient operating temperature should be limited to 155°C.

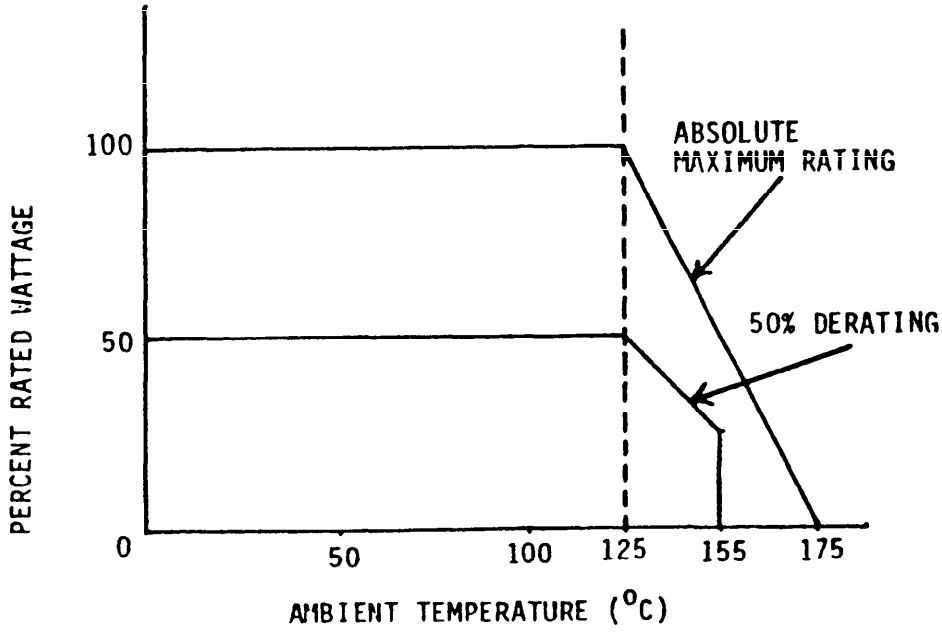


FIGURE 5.2.3.12-2: DERATING CURVE

5.2.3.13 MIL-R-27208, RESISTORS, VARIABLE, WIREWOUND (ADJUSTMENT TYPE) (STYLE RT)

5.2.3.13.1 SPECIAL APPLICATION CONSIDERATIONS

o Substitution - Use MIL-R-39015 Style RTR resistors instead of MIL-R-27208 Style RT, when practicable.

o Derating - For reliable performance this style resistor should be operated at 50% of its absolute maximum wattage rating. The absolute maximum rating curve and the recommended minimum derating curve are shown below. The maximum ambient operating temperature should be limited to 130°C.

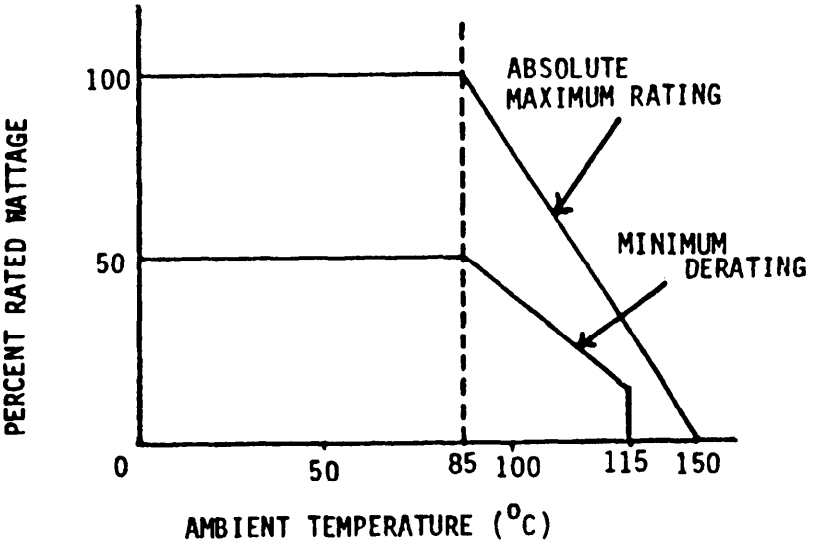


FIGURE 5.2.3.13-1: DERATING CURVE

5.2.3.14 MIL-R-39002, RESISTORS, VARIABLE, WIREWOUND, SEMIPRECISION (STYLE RK)

5.2.3.14.1 SPECIAL APPLICATION CONSIDERATIONS

o Selection of a Safe Resistor Style - The wattage rating of these resistors is based on operation at 85°C, mounted on a 4" square, 0.050" thick, steel panel. This mounting technique should be taken into consideration when wattage is applied during specific applications. When using other types of mountings, the power rating must be properly modified.

o Derating - For reliable performance this style resistor should be operated at 50% of its absolute maximum wattage rating. The absolute maximum rating curve and the recommended 50% derating curve are shown below. The maximum ambient operating temperature should be limited to 115°C.

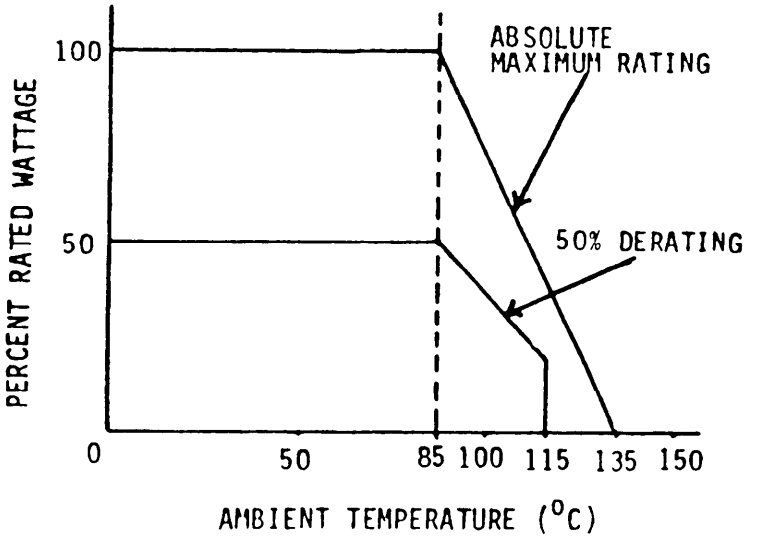


FIGURE 5.2.3.14-1: DERATING CURVE

5.2.3.15 MIL-R-39005, RESISTORS, FIXED, WIREWOUND (ACCURATE) ESTABLISHED RELIABILITY (STYLE RBR)

5.2.3.15.1 SPECIAL APPLICATION CONSIDERATIONS

These resistors are intended for use where extremely close tolerances (± 1% to ± 0.01%), a long life and a high degree of temperature stability is required.

o Derating - For reliable performance this style resistor should be operated at 50% of its absolute maximum wattage rating. The absolute maximum rating curve and the recommended 50% derating curve are shown below. The maximum ambient operating temperature should be limited to 125°C.

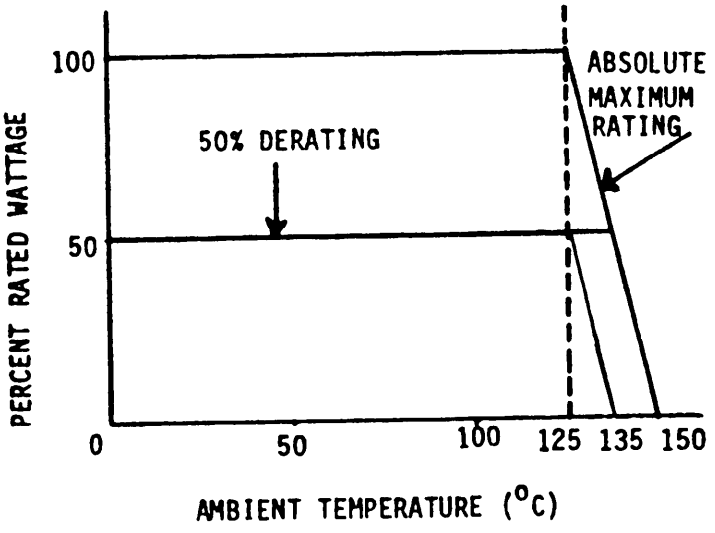


FIGURE 5.2.3.15-1: DERATING CURVE

5.2.3.16 MIL-R-39007, RESISTORS, FIXED, WIREWOUND (POWER TYPE), ESTABLISHED RELIABILITY (STYLE RWR)

5.2.3.16.1 SPECIAL APPLICATION CONSIDERATIONS

These resistors are recommended for use where greater power handling capacity is required. The RWR resistors are available in very close tolerance (to ± 0.1%) and have tightly controlled temperature coefficients (± 20 PPM/°C for values of 10 ohm or greater). Regardless of purchase tolerance, the design should tolerate a ± shift in resistance value to assure long life reliability in military applications.

o Derating - For reliable performance this style resistor should be operated at 50% of its absolute maximum wattage rating. The absolute maximum rating curve and the recommended 50% derating curve are shown below. The maximum ambient operating temperature should be limited to 150°C.

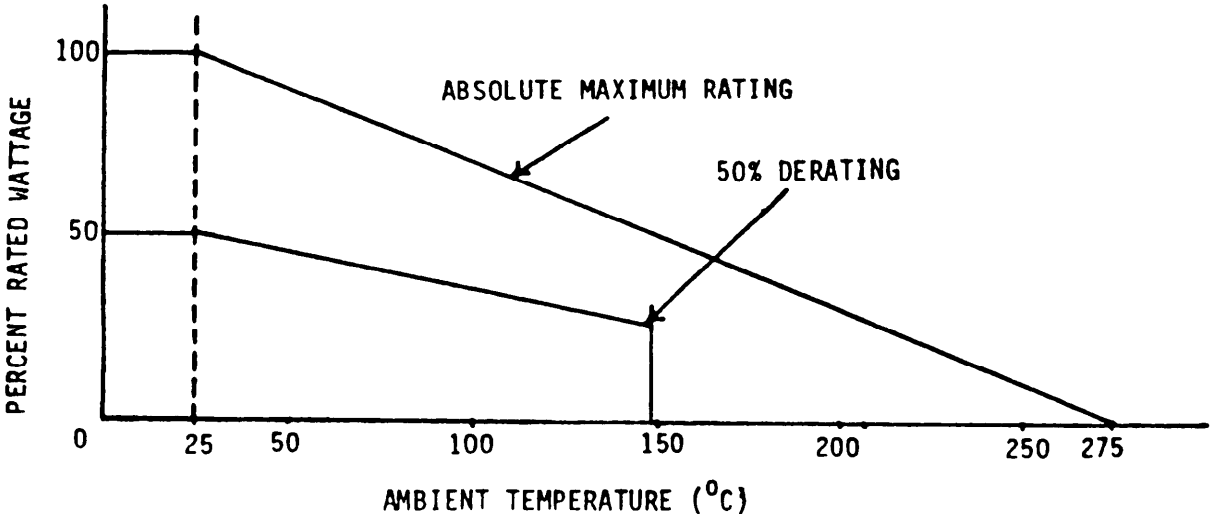


FIGURE 5.2.3.16-1: DERATING CURVE

5.2.3.17 MIL-R-39008, RESISTORS, FIXED, COMPOSITION (INSULATED) ESTABLISHED RELIABILITY (STYLE RCR)

5.2.3.17.1 SPECIAL APPLICATION CONSIDERATIONS

o Voltage Coefficient - For resistance greater than 100 ohms, resistance values can change with the application of voltage, as follows:

RCR 05	0.05%/volt
RCR 07, RCR 20	0.035%/volt
RCR 32, RCR 42	0.02%/volt

The voltage coefficient for resistors below 1,000 Ohms is not controlled by specifications and these resistors should not be used in circuits which are sensitive to this parameter.

o Derating - For reliable performance this style resistor should be operated at 50% of its absolute maximum wattage rating. The absolute maximum rating curve and the recommended 50% derating curve are shown below. The maximum ambient operating temperature should be limited to 120°C for styles RCR 05 and 07 and to 100°C for styles RCR 20, 32 and 42.

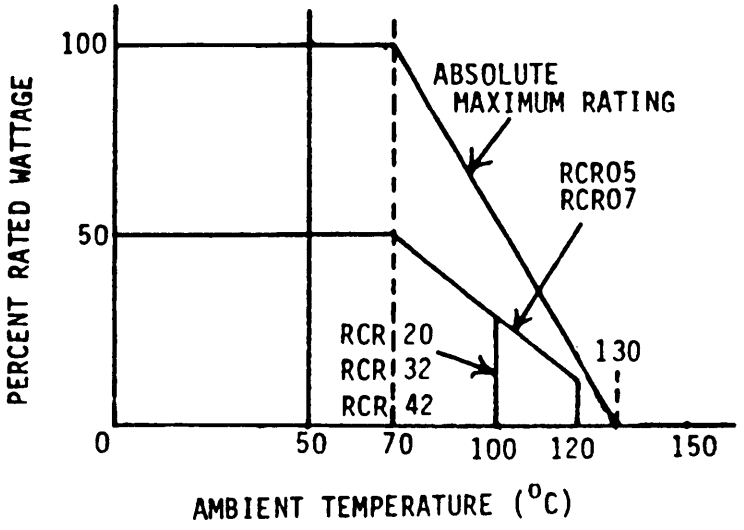


FIGURE 5.2.3.17-1: DERATING CURVE

5.2.3.18 MIL-R-39009, RESISTORS, FIXED, WIREWOUND (POWER TYPE, CHASSIS MOUNTED) ESTABLISHED RELIABILITY (STYLE RER)

5.2.3.18.1 SPECIAL APPLICATION CONSIDERATIONS

o Resistance Tolerance - Only one tolerance range (±1%) is available. The temperature stability is very good (±30 PPM/°C for values of 20 ohms or higher). The design should tolerate a ±1.5% shift in resistance value to assure long life reliability in military applications.

o Derating - For reliable performance this style resistor should be operated at 50% of its absolute maximum wattage rating. The absolute maximum rating curve and the recommended 50% derating curve are shown below. The maximum ambient operating temperature should be limited to 150°C.

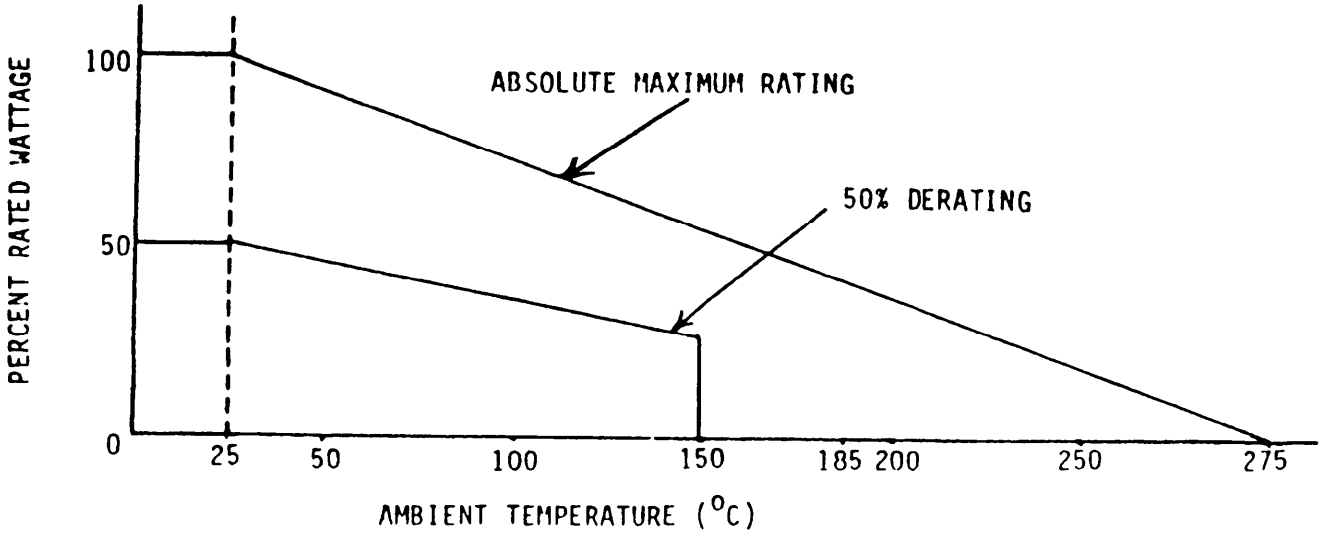


FIGURE 5.2.3.18-1: DERATING CURVE

5.2.3.19 MIL-R-39015, RESISTORS, VARIABLE, WIREWOUND (LEAD SCREW ACTUATED) ESTABLISHED RELIABILTY (STYLE RTR)

5.2.3.19.1 SPECIAL APPLICATION CONSIDERATIONS

o Selection of a Safe Resistor Style - The wattage ratings of these resistors are based on operation at 85°C when mounted on a 1/16-inch thick, glass base, epoxy laminate. Therefore, the heat sink effect as provided by steel test plates in other specifications is not present. The wattage rating is applicable when the entire resistance element is engaged in the circuit. When only a portion is engaged, the wattage is reduced directly in the same proportion as the resistance.

o Bushing - The use of nonlocking type bushings is recommended for longer life.

o Mounting - Resistors with terminal Type L should not be mounted by their flexible wire leads. Mounting hardware should be used. Printed circuit types are frequently terminal mounted, although brackets may be necessary for a high shock and vibration environment.

o Environmental Conditions - Special care should be taken when using these resistors in highly humid conditions, since high humidity can cause turn-to-turn shorts. It is better to avoid the use of these resistors in high humidity environments.

o Derating - For reliable performance this style resistor should be operated at 50% of its absolute maximum wattage rating. The absolute maximum rating curve and the recommended minimum derating curve are shown below. The maximum ambient operating temperature should be limited to 115°C.

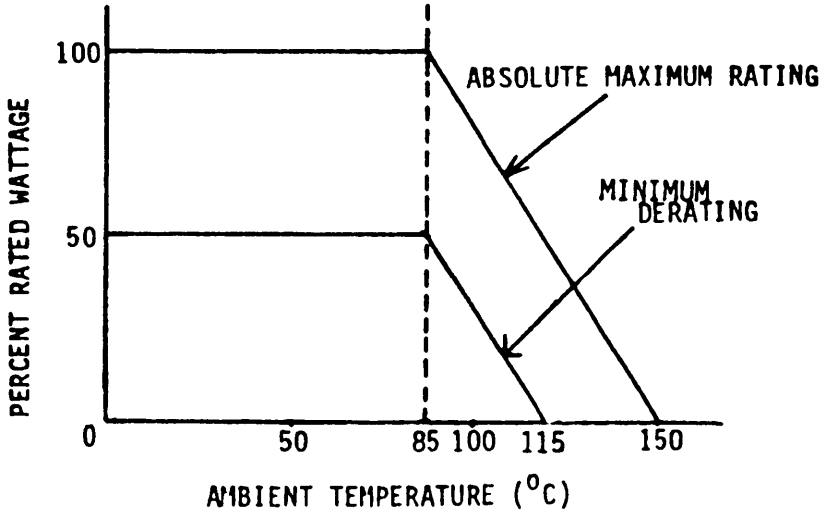


FIGURE 5.2.3.19-1: DERATING CURVE

5.2.3.20 MIL-R-39017, RESISTORS, FIXED, FILM (INSULATED), ESTABLISHED RELIABILITY (STYLE RLR)

5.2.3.20.1 SPECIAL APPLICATION CONSIDERATIONS

o Resistance Tolerance - These resistors are recommended for use where very close tolerances are not required and where the composition type resistors do not provide the needed accuracy or stability. Regardless of the purchase tolerance (i.e., ± 1% or ± 2%), the design should tolerate an additional ± 5% shift in resistance value to assure long-life reliability in military applications.

o Operating Frequency - These resistors perform well in high frequency applications (up to about 100 MHz). The frequency characteristics are as shown in the figure below.

o Noise - The noise generated by these resistors is negligible.

o Pulsed Power Applications - The resistor should never be exposed to pulse voltages exceeding the maximum determined by the dielectric breakdown voltage. The average power dissipation should never exceed four times the nominal power rating of the device.

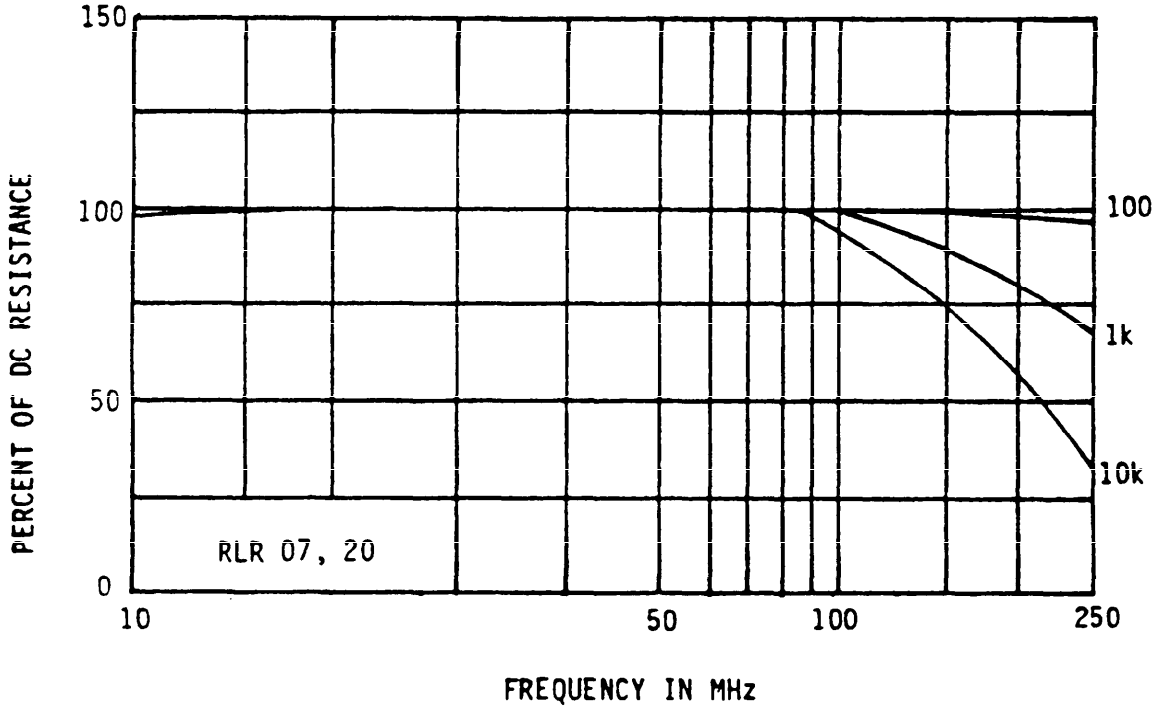


FIGURE 5.2.3.20-1: HIGH FREQUENCY OPERATING CHARACTERISTICS

o Derating - For reliable performance this style resistor should be operated at 50% of its absolute maximum wattage rating. The absolute maximum rating curve and the recommended minimum derating curve are shown below. The maximum ambient operating temperature should be limited to 110°C.

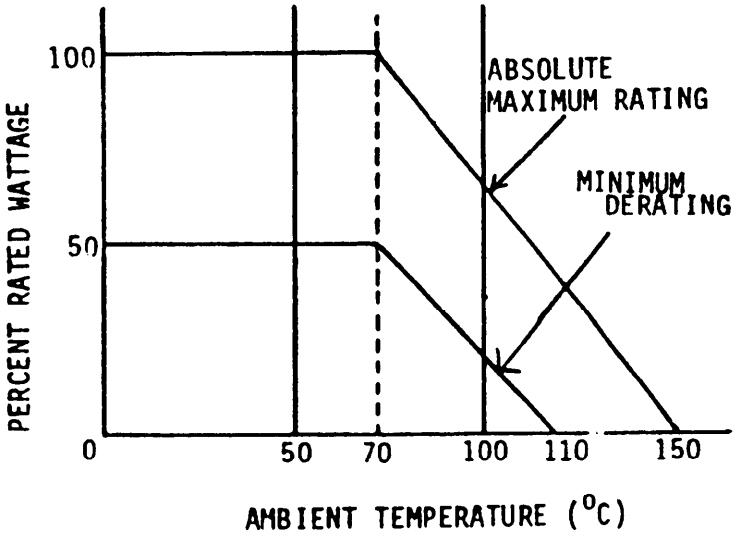


FIGURE 5.2.3.20-2: DERATING CURVE

5.2.3.21 MIL-R-39023, RESISTORS, VARIABLE, NONWIREWOUND, PRECISION (STYLE RQ)

5.2.3.21.1 SPECIAL APPLICATION CONSIDERATIONS

o Output - The output of these resistors (in terms of percent of applied voltage) is linear with respect to the angular position of the operating shaft.

o Temperature Characteristics - An average resistance change of ±10% due to temperature cycling is common.

o Selection of Safe Resistors - The wattage rating of these resistors is based on operation at 70°C, mounted on a 4" square, 0.25" thick alloy aluminum panel. This mounting technique should be taken into consideration when a wattage is dissipated during specific applications. When using other types of mountings, the wattage ratings should be properly modified.

o Derating - For reliable performance this style resistor should be operated at 50% of its absolute maximum wattage rating. The absolute maximum rating curve and the recommended 50% derating curve are shown below. The maximum ambient operating temperature should be limited to 85°C.

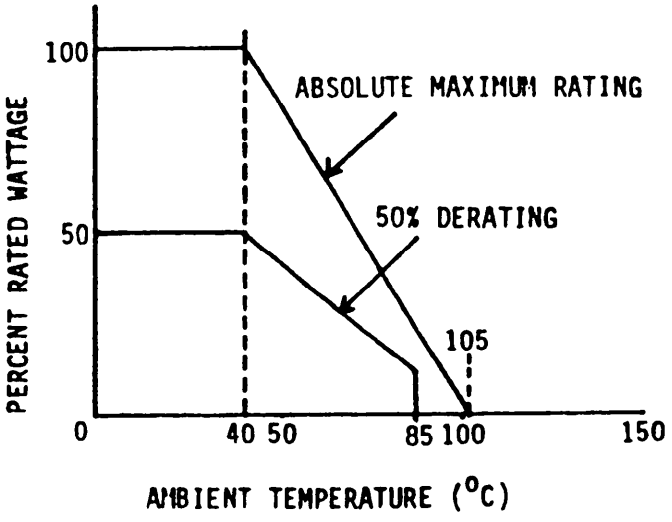


FIGURE 5.2.3.21-1: DERATING CURVE

5.2.3.22 MIL-R-39035, RESISTORS, VARIABLE, NONWIREWOUND (LEAD-SCREW ACTUATED) ESTABLISHED RELIABILITY (STYLE RJR)

5.2.3.22.1 SPECIAL APPLICATION CONSIDERATIONS

o Tolerance - These resistors have a resistance tolerance of ±10%. Regardless of the purchase tolerance, the design should be able to tolerate a ±10% shift in resistance value to assure long life reliability in military applications.

o Resolution - The resolution of type RJR resistors is very high (essentially infinite).

o Noise - The noise level is not controlled but it is normally relatively low.

o Selection of Safe Resistors - The wattage ratings of these resistors are based on operation at 85°C when mounted on a 1/16-inch thick, glass base, epoxy laminate. Therefore, the heat sink effect as provided by steel test plates in other specifications is not present. The wattage rating is applicable when the entire resistance element is engaged in the circuit. When only a portion is engaged, the wattage is reduced in direct proportion to the resistance.

o Bushing - A non-locking type bushing should be used whenever possible for longer life.

o Secondary Insulation - Where voltages higher than 250 volts rms are present between the resistor circuit and grounded surface on which the resistor is mounted or where the dc resistance is so high that the insulation resistance to the ground is an important factor, secondary insulation to withstand the conditions should be provided between the resistor and the mounting or between the mounting and ground.

o Resistor Mounting - Resistors with flexible, insulated wire leads (terminal Type L) should not be mounted by leads. Mounting hardware should be used. Printed-circuit types are frequently terminal mounted, although brackets may be necessary for a high-shock and vibration environment.

o Variation - The contact resistance variation should not exceed 3 percent or 20 ohms for the characteristic C and 3 percent or 3 ohms for characteristics F and H, whichever is greater.

o Derating - For reliable performance this style resistor should be operated at 50% of its absolute maximum wattage rating. The absolute maximum rating curve and the recommended minimum derating curve are shown below. The maximum ambient operating temperature should be limited to 115°C.

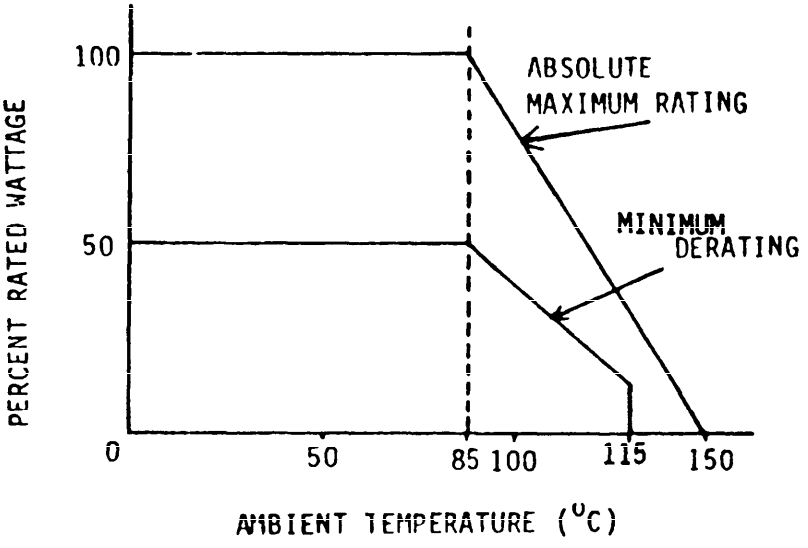


FIGURE 5.2.3.22-1: DERATING CURVE

5.2.3.23 MIL-R-55182, RESISTORS, FIXED, FILM, ESTABLISHED RELIABILITY (STYLE RNR).

5.2.3.23.1 SPECIAL APPLICATION CONSIDERATIONS

o Derating - For reliable performance this style resistor should be operated at 50% of its absolute maximum wattage rating. The absolute maximum rating curve and the recommended 50% derating curve are shown below. The maximum ambient operating temperature should be limited to 150°C.

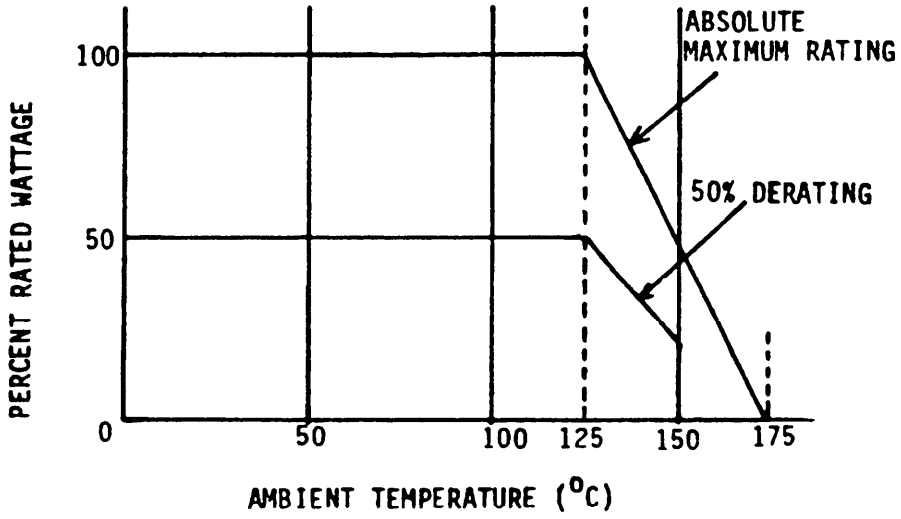


FIGURE 5.2.3.23-1: DERATING CURVE

5.2.3.24 MIL-R-55342, RESISTORS, FIXED, FILM, CHIP, ESTABLISHED RELIABILITY

5.2.3.24.1 SPECIAL APPLICATION CONSIDERATIONS

o Use - These chip resistors are intended to be used in thin or thick film hybrid circuitry where microcircuitry is indicated.

o Mounting - These resistors may be mounted individually on a substrate, usually 95% alumina, and connected to conductor areas by means of solder preforms, conductive cement or wire bonding. They can also be directly connected to other components on the same substrates by means of wire binding, using the substrate as a base or carrier for the resistor.

o Stacking of Resistors - Stacking of resistors should be avoided where possible, since failure can occur due to electrolytic action in the bonding adhesive. When stacking the resistors, care should be taken to compensate for the lower heat dissipation capabilities by properly derating the wattage rating.

o Electrostatic Damage Sensitivity - Some types of film devices are found to be affected by electrostatic discharge (ESD).

o Derating - For reliable performance this style resistor should be operated at 50% of its absolute maximum wattage rating. The absolute maximum rating curve and the recommended 50% derating curve are shown below. The maximum ambient operating temperature should be limited to 100°C.

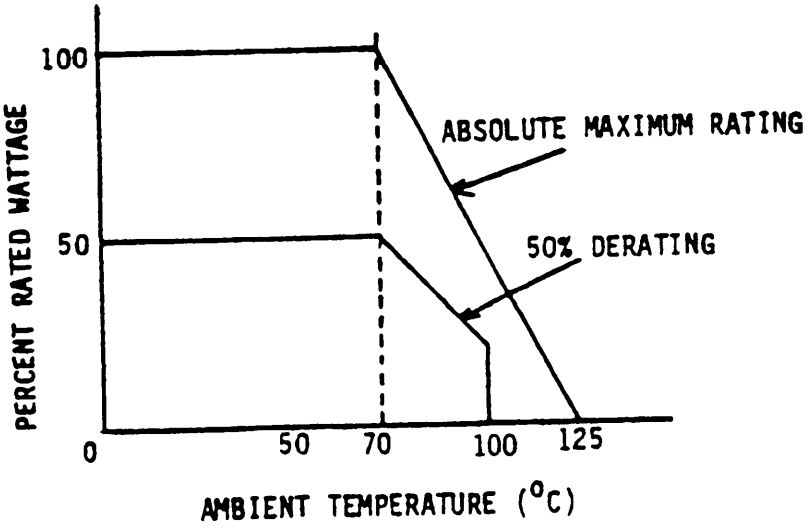


FIGURE 5.2.3.24-1: DERATING CURVE

5.2.3.25 MIL-R-83401, RESISTOR NETWORKS, FIXED, FILM (STYLE RZ)

5.2.3.25.1 SPECIAL APPLICATION CONSIDERATIONS

The RZ type resistors are in a resistor network configuration having a film resistance element and in a DIP or flat pack configuration. These resistors are stable with respect to time, temperature and humidity and are capable of full load operation at an ambient temperature up to 70°C after which they are derated to zero power at 125°C.

o Use - These resistors are designed for use in critical circuitry where stability, long life, reliable operation and accuracy are of prime importance. They are particularly desirable for use where miniaturization is important. They are also useful where a number of resistors of the same resistance values are required in the circuit.

o Operating Frequency - When used in high frequency circuits (200 MHz and above), the effective resistance will be reduced as a result of shunt capacity between resistance elements and connecting circuits. The high frequency characteristics of these networks are not controlled by specification.

o Noise - The noise output is not controlled by specification, but it is typically very low for these resistors.

o Resistance Tolerance - Operation of these resistor networks under military ambient conditions could cause permanent or temporary changes in resistance sufficient to exceed their initial tolerances. In particular, operation at extremely high or low ambient temperatures causes significant temporary changes in resistance. Care should be taken to assure that the circuit design will tolerate these changes.

o Mounting - Under severe shock or vibration conditions (or a combination of both), the resistor network should be restrained from movement with respect to the mounting base. If clamps are used, certain electrical characteristics can be altered. The heat dissipating qualities will be enhanced or retarded depending on whether the clamping material is a good or poor conductor of heat. This phenomenon should be given due consideration.

o Electrostatic Susceptibility - Some film resistors are found to be susceptible to electrostatic damage.

o Derating Requirements - For reliable performance this style resistor should be operated at 50% of its absolute maximum wattage rating. The absolute maximum rating curve and the recommended 50% derating curve are shown below. The maximum ambient operating temperature should be limited to 105°C.

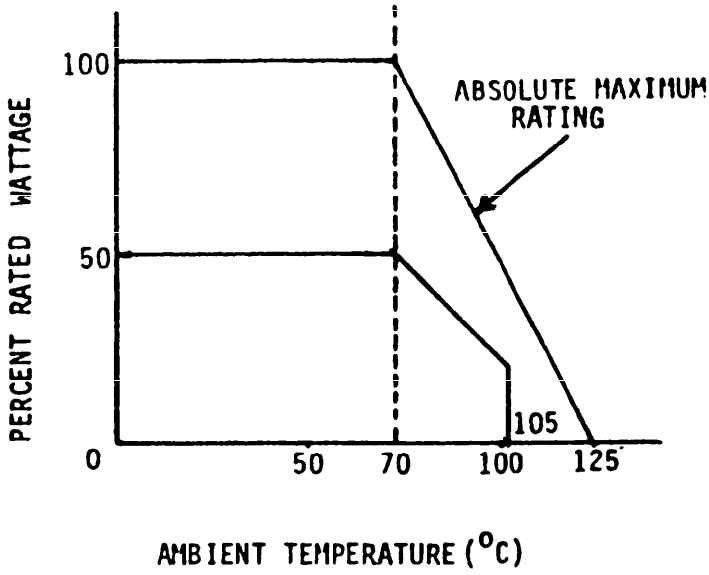


FIGURE 5.2.3.25-1: DERATING CURVE

5.2.3.26 MIL-T-23648, THERMISTOR (THERMALLY SENSITIVE RESISTOR) INSULATED (STYLE RTH)

5.2.3.26.1 SPECIAL APPLICATION CONSIDERATIONS

o Intended Use - Thermistors are intended to be used in applications such as temperature compensation, control and measurement in their specified temperature ranges.

o Incoming Inspection - Adequate precautions should be taken during inspection to prevent condensation of moisture on thermistors, except during test where moisture is part of the test.

o Soldering - Precautions should be taken to prevent damage by heat when soldering thermistors to terminals. It is recommended that a heat dam between the hot soldering iron and thermistor body be used to prevent damage to the thermistor.

o Derating Requirements - For reliable performance this style resistor should be operated at 50% of its absolute maximum wattage rating. The absolute maximum rating curve and the recommended 50% derating curve are shown below. The maximum ambient operating temperature should be limited to $T_{(max)}$ -20°C.

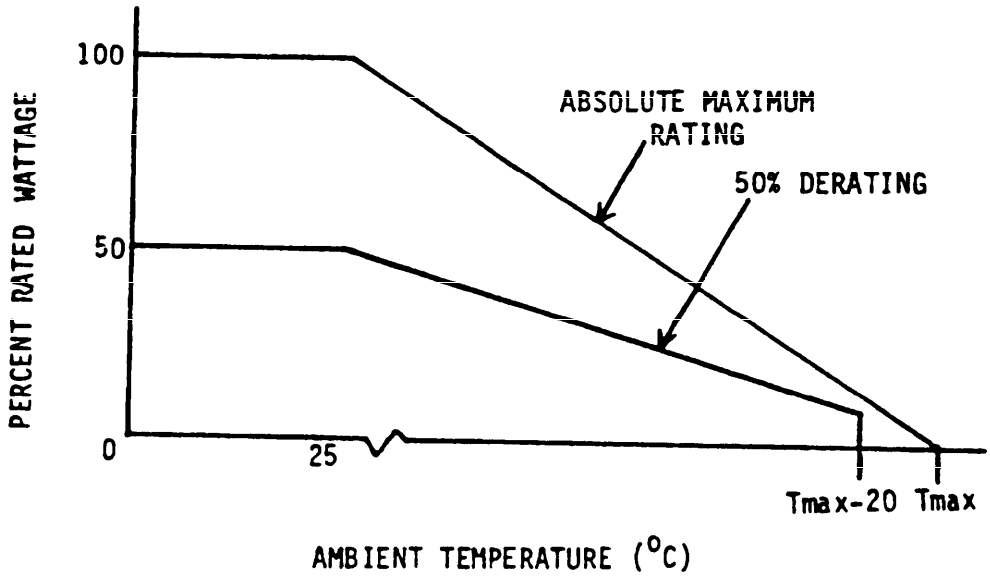


FIGURE 5.2.3.26-1: DERATING CURVE

5.2.4 CAPACITORS

5.2.4.1 INTRODUCTION

Capacitors can be broadly categorized into the following types according to the dielectric material used:

o Mica Capacitors. Mica is one of a very few natural materials directly adaptable for use as a capacitor dielectric. Its physical and electrical properties, plus its rare characteristics of nearly perfect cleavage make it probably the best known capacitor dielectric. It is inherently stable, both dimensionally and electrically, therefore, mica capacitators exhibit excellent temperature coefficient characteristics and very low aging with operation.

o Paper, Plastic, Paper-Plastic and Metallized Dielectric Capacitors. Paper, plastic, paper-plastic, and metallized dielectric capacitors serve the broad middle ground of capacitor requirements. This grouping includes a wide variety of dielectric systems, styles, voltage ratings and temperature characteristics. Continuing developments in dielectric materials, construction techniques and manufacturing processes have resulted in a highly versatile family of devices. As a group they have high insulation resistance, fairly good stability, and are capable of operation at ambient temperatures up to 125^{o}C. Certain of the plastic dielectric types, such as polycarbonate, polystyrene, and teflon, also have excellent temperature coefficient characteristics.

o Glass Capacitors. Glass dielectric capacitor electrical characteristics are very similar to those of mica capacitors: they have excellent long term stability, a low temperature coefficient, and a history of good reliability.

o Ceramic Capacitors. Ceramic capacitors can be defined as capacitative tive devices in which the dielectric material is a high temperature, sintered, inorganic compound. Ceramic capacitors are available in a variety of physical forms. In all their variations, ceramic dielectric capacitors are probably used more than any other single dielectric family. This high usage occurs because of their low cost, wide range of characteristics, good volumetric efficiency, and excellent high frequency capabilities. However, not all desirable characteristics are available in any single style.

o Solid Tantalum Capacitors. Solid tantalums are the electrolytic capacitors most widely used for military electronics equipment. They have high volumetric efficiency, good stability with time and temperature and are reliable devices when properly applied. Because the electrolyte used is solid and dry, these capacitors have a more stable capacitance temperature characteristic than any other of the electrolytic capacitors. Their limitations are a relatively high leakage current, limited voltage range available. These capacitors are available in both polarized and nonpolarized units.

o Nonsolid Tantalum Capacitors. Nonsolid tantalum capacitators are composed of two distinct types, the "wet slug" and the foil type. Foil type tantalums are probably the most versatile of all electrolytic capacitors. They are available in both polar and nonpolar construction, and in a wide range of voltage ratings. They are capable of operation at 125°C with proper derating, and are electrically the most rugged of the three basic tantalum types. Their prime disadvantages, as compared to other tantalum types, are relatively large size, fairly large change in capacitance with temperature, and high equivalent series resistance, especially at cold temperatures.

The liquid electrolyte sintered anode tantalum electrolytic capacitor, commonly known as the "wet slug", was the first type of tantalum capacitor to be developed for large scale production. It represented the initial breakaway from essentially total dependence on aluminum electrolytics for applications where large capacitance values at medium voltage ratings were required. The outstanding advantage of the wet slug type is its high volumetric efficiency; for capacitance values in the microfarad range, it will generally provide the smallest case size available in a given voltage rating. However, (1) neither the CLR-65 style nor the CLR-79 style can tolerate any reverse voltage for even short periods of time, and (2) its electrolyte, which is a sulphuric acid solution in liquid or gel form, is highly corrosive, and any electrolyte leakage can cause destruction of neighboring circuitry. For this reason, the use of wet slug tantalum capacitors, except for those cased in tantalum (type CLR-79) is not recommended.

o Aluminum Electrolytic Capacitors. Aluminum electrolytic capacitors, while not as volumetric efficient as tantalum capacitors, do provide the lowest cost per microfarad. They are not hermetically sealed, and are not recommended for airborne equipment applications where they would be subjected to low barometric pressures at high altitudes. In the past, aluminum electrolytic capacitors have been known for their limited shelf life and poor low temperature characteristics. In recent years, significant improvements have been made in these characteristics, greatly improving but not completely eliminating these shortcomings. One unique characteristic of aluminum electrolytic capacitors is their tendency to lose any unused portion of their rated voltage. Therefore, excessive voltage derating should not be applied to aluminum electrolytic capacitors.

o Standard capacitors. Standard capacitors are specified in MIL-STD-198. This standard presents detailed data for use in the design of military equipment. Data is presented on terminology, capacitor selection, environmental effects on characteristics and life, applications, application data, failure rates and aging curves. In addition, detailed design data are presented for each capacitor type.

5.2.4.2 CAPACITOR SELECTION

Factors to be considered in capacitor selection are:

- o Temperature
- o Humidity
- o Barometric pressure
- o Applied voltage
  - Alternating/ripple current
  - Frequency
  - Dissipation factor
  - Equivalent series resistance
  - Reverse voltage levels
- o Vibration
- o Current
- o Life
- o Stability
- o Retrace
- o Size
- o Volume
- o Mounting method
- o Cost

Similar to resistors, capacitors have been thoroughly investigated for operational characteristics, identified for form, function and applicable ratings, and documented for procurement, test, qualification approval, quality control and standardization within MIL specifications and standards. Like resistors, they are normally produced in large production runs which tends to keep unit prices low and promotes standardization. Capacitor selection is governed by the criteria given in Table 5.2.4.2-1.

TABLE 5.2.4.2-1: CAPACITOR SELECTION CRITERIA

1.	MIL-STD-198, "Capacitors, Selection and Use Of."
2.	Established Reliability Series of Military Specifications
3.	Other MIL Specifications on capacitors
4.	Historical test data (from similar applications) or other engineering information and/or data that provides assurance that the device is sufficiently rugged and reliabile for the application (e.g., previous use in military equipment, comparable applications, or GFE).

NOTE:
In selecting particular capacitors for specific applications, the qualified product list should be consulted for a list of qualified sources prior to procurement commitments.

5.2.4.2.1 USAGE FACTORS

Usage and selection guidelines for capacitors, including the predominant failure modes are given in Table 5.2.4.2-2.

TABLE 5.2.4.2-2: SELECTION AND USAGE GUIDE FOR CAPACITORS

Military Specification	Type	Style	Usage Notes	Failure Modes
		FIXED, MICA		
MIL-C-5	Mica dielectric	CM05 CM07 CM06 CM08	Inactive for new design. Use MIL-C-39001	
		CM15 CM35 CM20 CM45 CM30 CM50	Use in circuits requiring precise, high-frequency filtering, bypassing. Use where close impedance limits are essential with respect to temperature, frequency and aging--such as in tuned circuits which control frequency, reactance, or phase. Use as padders in tuned circuits, as secondary capacitance standards, and for tuning of high frequencies. Also used in delay lines and stable low-power networks, capacitors are inexpensive and have good stability and reliability.	Shorts can occur due to moisture absorption, or due to internal solder flow resulting from excessive heat generated during external lead-soldering. Opens usually result for rupture of weak internal connections due to vibration or shock.
MIL-C-10950	Mica dielectric	CB50 CB61 CB55 CB62 CB56 CB65 CB57 CB66 CB60 CB67	Intended for use at frequencies up to 500 MHz. Use in tuned circuits, and in coupling and bypassing applications in VHF and UHF circuits. Units have high reliability if properly protected from high ambient temperature and humidity conditions.	Capacitors are very susceptible to silver-ion migration, resulting in shorts. Migrations can occur in a few hours when capacitors are simultaneously exposed to dc voltage stress, humidity and high temperature.
MIL-C-39001	Mica dielectric ESTABLISHED RELIABILITY	CMR03 CMR04 CMR05 CMR06 CMR07 CMR08	Intended for use where known orders of ability are required. Failure rate depends on unit's application; e.g., (1) with constant temperature, capacitor life is inversely proportional to the 8th power of the applied dc voltage, or (2) with constant dc voltage, life decreases approximately 50% per each 10°C rise in temperature. Life expectancy at rated conditions is 50,000 hrs, minimum.	Same comments as given for MIL-C-5.
		FIXED, GLASS		
MIL-C-11272	Glass dielectric		Inactive for new design. Use MIL-C-23269.	
MIL-C-23269	Glass dielectric ESTABLISHED RELIABILITY	CYR10 CYR13 CYR15 CYR17 CYR20 CYR22 CYR30 CYR32 CYR41	Capacitors should be used as substitutes for mica units in applications requiring known reliability and where the differences in temperature coefficeint and dielectric loss are taken into account. They are stable in extreme environmental conditions, have long life (30,000 hrs and more) and are very satisfactory for use in missile-borne and space equipment. These	Degradation of dielectric crystalline structure can occur as the result of storage below 45°C. The capacitance will decrease with the decrease in dielectric constant and the unit will drift out of tolerance. Opens are frequently due to poor connections of leads to the plates or mechanical damage to the capacitor. Over-heating during external soldering can result in internal solder

TABLE 5.2.4.2-2: SELECTION AND USAGE GUIDE FOR CAPACITORS (Cont'd)

Military Specification	Type	Style	Usage Notes	Failure Modes
		FIXED, GLASS (Cont'd)		
MIL-C-23269 (Cont'd)		CYR42 CYR43 CYR51 CYR52 CYR53	physically-small units are resistant to high G loads, but are susceptible to damage from mild mechanical shocks. Therefore, they should be handled carefully. They exhibit a much higher Q over a wider capacitance range than mica dielectric units.	flow (shorts) or rupture of internal solder connection (opens).
		FIXED, PAPER AND PLASTIC		
MIL-C-25	Paper (or paper-plastic dielectric		Inactive for new design. Use MIL-C-19978.	
MIL-C-12889	Bypass radio-interference reduction paper dielectric, ac and dc		Inactive for new design. Use MIL-C-39022.	
MIL-C-18312	Metallized paper (or polyester film) dielectric		Inactive for new design. Use MIL-C-39022.	
MIL-C-19978	Plastic (or paper-plastic) dielectric ESTABLISHED RELIABILITY	CQR07 CQR09 CQR12 CRQ13 CQR29 CQR32 CQR33	Capacitors are intended for use in applications which require high insulation resistance, low dielectric absorption, or low loss factor over wide temperature ranges, and where the ac component of the impressed voltage is small compared to the dc voltage rating. If ac components are present, the sum of the dc peak voltage and the ac peak voltage shall never exceed the rated dc voltage, nor shall the peak ac voltage exceed 20% of the dc voltage rating at 60Hz, 15% at 120Hz, or 1.0% at 10,000Hz.	Principal failure modes are open, due to poor internal connections and use at rated voltage levels in high temperatures. Shorts can occur due to internal solder flow caused by excessive heat being applied to terminals during external soldering. Shorts also occur due to contaminants in the dielectric causing momentary breakdown which can result in a carbonization of the plastic, which, if extensive enough, will result in a permanent short.
		FIXED, CERAMIC		
MIL-C-11015	Ceramic dielectric (general purpose)	CK50 CK63 CK51 CK65 CK52 CK66 CK53 CK67 CK54 CK68 CK55 CK69 CK60 CK70 CK62 CK71 CK80	Intended for use where small size, comparatively large capacitance and high insulation resistance are required. Capacitors are suitable for use as bypass, filter and noncritical coupling elements in high-frequency circuits where applicable capacitance change caused by temperature variations can be tolerated.	Shorts--can occur due to silver ion migration caused by high humidities coupled with the application of high dc voltage. Opens--generally result from damage done to the capacitor by handling or by the application of excessive heat during soldering which ruptures internal connections.

TABLE 5.2.4.2-2: SELECTION AND USAGE GUIDE FOR CAPACITORS (Cont'd)

Military Specification	Type	Style	Usage Notes	Failure Modes
		FIXED, CERAMIC (Cont'd)		
MIL-C-11015 (Cont'd)			Typical cases include resistive-capacitive coupling for audio and radio frequency, RF and IF cathode bypass, etc. Use where dissipation factor is not critical and moderate changes due to temperature, voltage and frequency variations, do not affect proper circuit function.	Shorts can also occur by internal solder reflow due to excessive heat applied to leads during external soldering without use of a proper heat sink procedure.
MIL-C-39014	Ceramic dielectric, ESTABLISHED RELIABILITY (FR: 1 to 0.001)	CKR05 CKR14 CKR06 CKR15 CKR11 CKR64 CKR12 CKR72	Use in applications where the required reliability level is known. Suitable for use as bypass, filter and non-critical coupling elements in high frequency circuits.	Same as MIL-C-11015.
		FIXED, CERAMIC, TEMPERATURE COMPENSATING		
MIL-C-20	Ceramic dielectric, Temperature Compensating ESTABLISHED RELIABILITY	CCR05 CCR76 CCR06 CCR76 CCR07 CCR77 CCR08 CCR78	These capacitors are zero temperature coefficient units which should be used in applications requiring high stability over a wide temperature range.	Due to internal pressures during the encapsulation process the primary failure mode is open.
		FIXED, ELECTROLYTIC		
MIL-C-62	Electrolytic (dry electrolyte aluminum)		Not approved for Air Force or Navy use in new design.	
MIL-C-3965	Electrolytic (non-solid electrolyte) tantalum		Inactive for new design. See Established Reliability Type MIL-C-39006.	
MIL-C-39003	Tantalum (solid electrolyte) ESTABLISHED RELIABILITY (FR: 2 to 0.001)	CSR09 CSR13 CSR33 CSR91	Intended for use where a known order of reliability is required. These capacitors are the most stable, reliable and long-lived electrolytics available. These units are not temperature sensitive. Limitations are relatively high leakage current, small voltage range (6-120V) and a maximum allowable reverse current of 5% of rated dc voltage at +25C to 1.0% at +125°C. Capacitors are used where low-frequency, pulsating dc components are to be bypassed or filtered-out and for uses requiring large capacitances, small size and the ability to withstand significant shock and vibration levels. Use for filtering, bypass, coupling, blocking, energy storage and other low voltage dc applications. Capacitors are available only in polarized form; use only in dc circuits with the polarity observed.	Shorts can occur due to solder-balls created by internal solder flow resulting from heat generated during the external soldering of leads. Shorts due to dielectric breakdown are rare due to self-healing effect of high leakage current on the MnO_2, provided current is limited by use of a 3 ohm/volt line resistance in series with the capacitor. Open occur mainly due to poor solder or weld internal connections which rupture during vibration or shock.

TABLE 5.2.4.2-2: SELECTION AND USAGE GUIDE FOR CAPACITORS (Cont'd)

Military Specification	Type	Style	Usage Notes	Failure Modes
MIL-C-39006	Electrolytic (non-solid electrolyte) tantalum ESTABLISHED RELIABILITY	CLR25 CLR35	Polarized foil capacitors (styles CLR25 and CLR35) should be used where large capacitance values are required and wide tolerances are acceptable. Use for bypassing or filtering-out low frequency pulsating dc components. When used for low frequency coupling in vacuum tube and transistor circuits, allow for leakage current. Units should be used only in dc circuits with polarity properly observed. If ac components are present, the sum of the peak ac voltage plus the applied dc voltage must not exceed the dc rated voltage. Also, peak ac voltage shall not exceed the applied dc voltage.	Capacitors are subject to failure (shorts) due to leakage of the electrolyte which can be caused by wide-range temperature cycling, vibration or agencies which damage the seal. The application of reverse voltage will also result in shorts. Opens are usually associated with faults in external lead welds.
		CLR27 CLR37	Nonpolarized foil capacitors (styles CLR27 and CLR37) are suitable for use in ac applications where dc voltage reversals occur. Examples: tuned, low frequency circuits; phasing low-voltage ac motors; computer circuits, servo systems.	
		CLR65	Sintered-slug (style CLR65) are used because of their high volumetric efficiency primarily in low voltage power supply filtering circuits. Use in dc applications only; no reverse voltage can be tolerated.	CLR-65 used silver plated cases to contain sulfuric acid electrolyte. Silver migration caused by voltage reversal results in catastrophic failures. Excessive ripple can be a problem too.
		CLR79	Sintered-slug (style CLR79) similar to CLR65 but utilizes tantalum cases. CLR79 does not require silver plating. The tantalum case is impervious to attack by H_2SO_4.	
MIL-C-39018	Electrolytic (aluminum oxide electrolyte) ESTABLISHED RELIABILITY	CU15 CUR13 CUR17 CUR19 CUR71 CUR91	Use in filter, coupling, and bypass applications in which large capacitances are needed and capacitance excesses over the nominal value can be tolerated. For polarized units (all except style CU15) the applied ac peak voltage should never exceed the applied dc voltage. The sum of the applied ac peak and dc voltages should never exceed the dc rated voltage. Use where low-frequency, pulsating dc signal components are to be filtered out, such as in B+ power supplies up to 400 dc working volts; at plate screen connections to B+; and as cathode bypass units in self-biasing circuits.	Gradual loss of capacitance and increasing dissipation factor are the primary failure modes. Excessive voltage derating can cause loss of unused capability and thus require dielectric reforming.

TABLE 5.2.4.2-2: SELECTION AND USAGE GUIDE FOR CAPACITORS (Cont'd)

Military Specification	Type	Style	Usage Notes	Failure Modes
MIL-C-39022	Metallized dielectric, dc (hermetically sealed in metal cases), ESTABLISHED RELIABILITY	CHR09 CHR19	Intended for use in applications where the ac voltage component is small compared to the dc voltage rating and where occasional periods of low insulation resistance and momentary breakdown can be tolerated. If ac component is present, the sum of the applied dc and the peak ac voltage shall not exceed the rated dc voltage, and the ac voltage shall not exceed 20% of the dc voltage rating.	Opens occur due to poor internal connections, which under strong electrical or mechanical stress, will rupture. Shorts can occur due to internal solder flow as the result of over-heating the leads during external soldering. Momentary shorts occur very frequently because the dielectric is so thin, but will heal themselves, losing a small amount of capacitance in the process.
MIL-C-55514	Plastic or metallized plastic dielectric ESTABLISHED RELIABILITY	CFR02 CFR03 CFR04 CFR05 CFR06 CFR08	Capacitors for use in applications requiring high insulation resistance, low dielectric absoprtion or low loss factor over wide temperature ranges and where ac is small with respect to the dc rating. Capacitors have limited moisture resistance and are not recommended where heavy transient or pulse currents are encountered.	Same comments as given for MIL-C-39022.
FIXED, HYBRID, CHIP				
MIL-C-55681	Chip Ceramic dielectric ESTABLISHED RELIABILITY	CDR01 CDR02 CDR03 CDR04	Intended for use in thin or thick film hybrid circuits.	Decreased insulation resistance and shorts are the principal failure modes. Causes are severe delamination, ceramic rupture and electrode misregistrations.
MIL-C-55365	Chip Tantalum dielectric ESTABLISHED RELIABILITY	CWR02 CWR05 CWR03 CWR06 CWR04 CWR07 CWR08	Intended for use in thin or thick film hybrid circuits for filtering, bypassing, coupling where the ac is small compared to the dc rated voltage. To be used only where protected from moisture.	
VARIABLE, CERAMIC				
MIL-C-81	Ceramic dielectric	CV11 CV21 CV31	Capacitors are intended for use where fine tuning adjustments are periodically required. They are frequently used in RF, IR, oscillator, phase shifter, and discriminator stages. Capacitance and adjustment are relatively linear. Capacitance change with temperature change is nonlinear; also the temperature sensitivity over the capacitance range is nonlinear. Do not use these units for temperature compensation. These are small-size trimmers which are relatively stable under shock and vibration. Where greater stability is required, air trimmers should be used.	Same comments as given for MIL-C-11015.

TABLE 5.2.4.2-2: SELECTION AND USAGE GUIDE FOR CAPACITORS (Cont'd)

Military Specification	Type	Style	Usage Notes	Failure Modes
MIL-C-14409	Variable, Glass dielectric trimmer	PC25 PC40 PC26 PC42 PC38 PC43 PC39 PC48 PC52	Capacitors are small-sized, sealed, tabular trimmer, variable units designed for fine tuning adjustments such as trimming and coupling circuits in RF, IF, oscillator, phase shifter and discriminator stages.	Mechanical binding of the piston and fracturing of the adjustment screw both due to solder flux contaminants are frequent failure modes.

5.2.4.3 GENERAL APPLICATION CONSIDERATIONS

(a) Dielectric Versus Volume. In electrolytic capacitors, the dielectric is an almost negligible part of the volume of the capacitor. In other capacitors, such as mica, plastic, ceramic and glass dielectrics, the dielectric compromises nearly the entire volume of the capacitor element. Theoretically, for all capacitors except electrolytes where almost the entire volume of the unit is an active dielectric, the volume (v) is directly proportional to CV^2 (where C is the capacitance and V is the maximum voltage rating). The proportionality constant depends on the dielectric constant of the material, its dielectric strength, and the life expected of the capacitors. For the electrolytic types, the volume has been found empirically to vary more nearly with CV than CV^2.

(b) Operating Frequency. All capacitors have some operating frequency limitations due to the nature of the dielectric and other construction features. Figure 5.2.4.3-1 shows the operating frequency ranges for common types of capacitors except electrolytic. The frequency range for electrolytics is not readily described in this manner, because the effective capacitance of these type parts involves a complex relationship of voltage rating, case size, nominal capacitance value, and operating frequency.

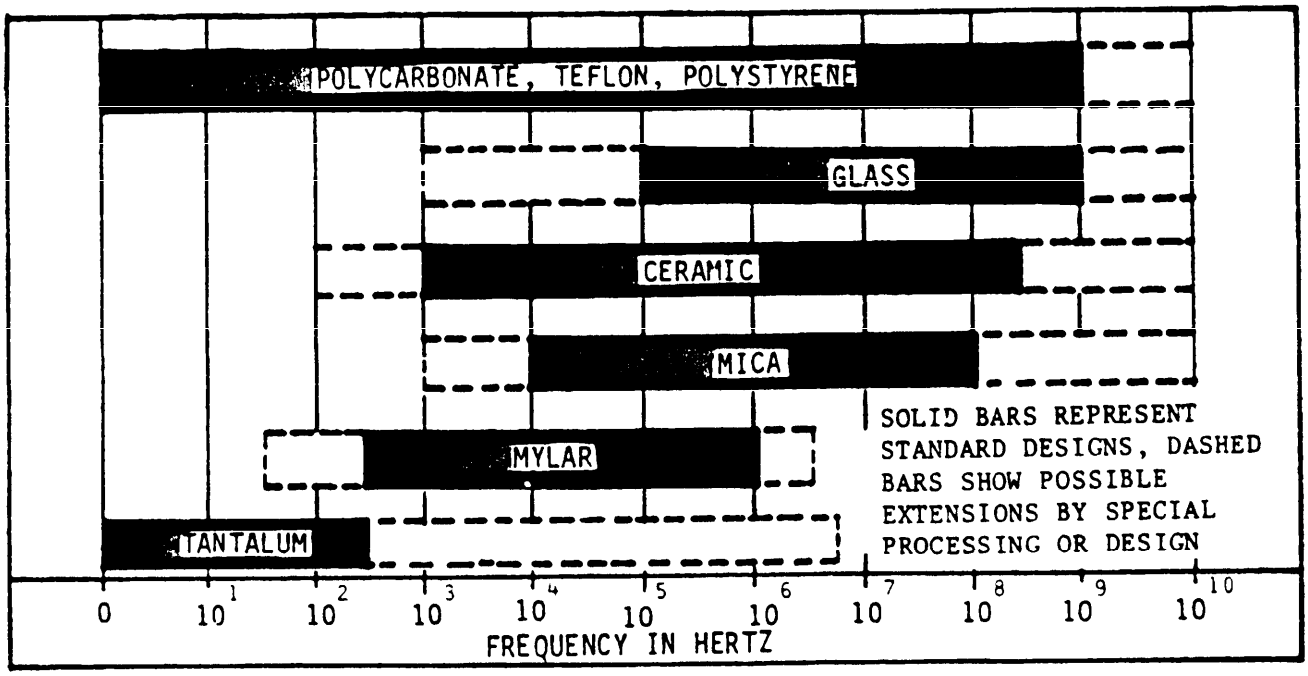


FIGURE 5.2.4.3-1: OPERATING FREQUENCY LIMITS FOR CAPACITATORS

(c) Voltage Rating and Life. Since the catastrophic failure of capacitors is usually caused by dielectric failure, voltage ratings of nonelectrolytic capacitors are based on a given life expectancy at a maximum ambient temperature and voltage stress. Dielectric failure is typically a chemical effect, and for well sealed units, where atmospheric contamination of the dielectric does not contribute, is a function of time, temperature, and voltage. The time-temperature relationship affects the chemical activity or rate of degradation; that is, degradation proceeds at a doubled rate for each 10^{0}C rise in temperature (e.g., a capacitor operating at 100^{0}C will have half the life of a similar one operating at 90^{0}C). Extensive studies have been made of certain organic dielectrics in which it has been found that the deterioration is proportional to V^{5} (fifth power of the voltage). For example, a capacitor operating at 20 volts will last 32 times as long as a similar one operating at 40 volts. The 10^{0}C rule, of course, is applicable only over a temperature range where no significant changes of state occur to affect the dielectric. That is, no freezing, melting, boiling, condensing, loss or gain of water, crystallization or other change in stable crystal structure. The V^{5} rule is also subject to modification by consideration that the dielectric will puncture suddenly if some particular voltage stress is exceeded, and that there are other electric fields (notably around the edges of the dielectric extending beyond the conducting plates) where breakdown can occur without failure of the principal dielectric.

5.2.4.3.1 CAPACITOR, MICA DIELECTRIC, GENERAL APPLICATION CONSIDERATIONS

o Both glass and mica capacitors have high capacitance per unit volume or mass with the glass having a much higher capacitance to its volume/mass ratio than the mica. Bodies of glass capacitors are often made of dielectric material and are capable of resisting moisture to a large degree. However, nonhermetically sealed units should not be subjected to relative humidities higher than 80%. These capacitors are very brittle due to their construction and materials used and may be damaged by high shock or vibration.

o These capacitors perform well at frequencies up to 500 MHz.

o When AC operation is required, the peak AC voltage plus any DC bias should not exceed the derated values obtained from derating guidelines. Where transients are encountered, the effects of these transients should also be considered.

o Silvered mica capacitors should never be subjected to DC voltage stresses in combination with high humidity and high temperatures for extended periods due to silver ion migration effects.

5.2.4.3.2 CAPACITORS, CERAMIC DIELECTRIC, GENERAL APPLICATION CONSIDERATION

o Temperature Compensation Capacitors. The temperature-time curve of the selected capacitor should be the exact opposite of the temperature-time curve of the coil or other part being compensated. Combinations of different capacitance values and temperature coefficients can give more precise compensation than can be obtained from a single capacitor. Full consideration should be given to the physical placement of compensating capacitors. Locations near hot operating parts could affect the designed-in circuit temperature compensation.

5.2.4.3.3 CAPACITORS, ELECTROLYTIC, GENERAL APPLICATION CONSIDERATIONS

Electrolytic capacitors are smallest in size and cost for a specific capacitance and voltage rating. Although these capacitors are available with high capacitance values, the initial tolerances are large. These capacitors cannot be used where close tolerances are required.

o Shelf Life. Tantalum electrolytes have excellent shelf life characteristics. Shelf life of aluminum electrolytic capacitors, however, is limited because the film dissolves in the electrolyte.

o Case. The largest possible case size should be used for a given capacitor voltage rating as this provides thicker oxide dielectric, lower equivalent series resistance, lower dissipation factor, better heat dissipation, and greater capacitance stability. Only sealed units should be used since the penetration of moisture could affect the electrolyte.

o Use Restrictions. Electrolytic capacitors are not suitable for application in low pressure, high altitude environments. Many of these capacitors are polarized and should not be subjected to reverse bias voltages.

o Operating Frequency. Generally, the filtering capability of electrolytic capacitors is limited to frequencies below 10KHz. Above 10KHz, the effective capacitance rapidly decreases until the capacitor becomes purely resistive (except for CUR19 and CUR91).

o Operation in Parallel. When electrolyte capacitors are operated in parallel, the ripple or surge currents for each should not exceed the recommended limit. The currents will not divide evenly due to the difference in internal impedances and this should also be considered in parallel applications.

5.2.4.3.4 CAPACITOR TANTALUM, GENERAL APPLICATION CONSIDERATIONS

o Series Impedance. These capacitors should have an effective series impedance of at least 3 ohms/volt. This will allow the capacitor to self-heal internal momentary breakdowns. If the current is limited to 330 MA when the capacitor is momentarily shorted, this will also satisfy the requirements.

o Assembly Considerations. When solid electrolyte capacitors are used in banks, series limiting resistors should be installed with each capacitor to prevent discharge of the entire bank into a scintillation fault. When the capacitors are used in series, balancing resistors should be used to assure proper division of voltages. When they are used in banks, they should be assembled in easily removable modules to facilitate replacement and test.

o Ripple Current. The ripple current in all capacitors should be limited to values which do not bring the temperature above the derated rating. When capacitors are used in banks the capacitor with the lowest equivalent series resistance will carry the largest ripple current. For foil and solid electrolyte capacitors, the allowable ripple current should be derated to 70% of the manufacturer's suggested derating for high reliability.

o Reliability Considerations

a. For high reliability, polarized capacitors should be protected or applied so that voltage reversal never occurs, including the conditions of combined ac and dc voltage.

b. The temperature of solid electrolyte capacitors should be limited to 50°C, including internal temperature rise; the foil and wet slug types should be limited to 70°C.

5.2.4.3.5 CAPACITORS, ALUMINUM ELECTROLYTIC, GENERAL APPLICATION CONSIDERATIONS

Aluminum electrolytic capacitors have in the past experienced deterioration of the oxide film when operated at less than rated voltage for prolonged periods of time. The oxide film deformed to a lower voltage and the capacitor would be destroyed upon application of full rated voltage. This phenomena would also occur if the capacitors were stored for a long period of time, particularly at high temperature. Due to improvement of the oxide film and manufacturing processes this problem has virtually disappeared. If the capacitors have been in storage for longer than 5 years, however, it is recommended that they be checked for leakage prior to being used.

5.2.4.3.6 CAPACITORS, PAPER/PLASTIC/PAPER-PLASTIC DIELECTRIC, GENERAL APPLICATION CONSIDERATIONS

These capacitors can be used in applications that require high and stable insulation resistance at high temperature and good capacitance stability over a wide temperature range. This permits use in a wide range of applications ranging from computers to guided missiles. The relatively high dielectric strength of some of the plastic capacitors can lead to attractive small physical dimensions. These capacitors are of a small relative size for equivalent CV rating except for MIL-C-19978 polystryene types which are medium to large size. Metallized paper capacitors have low insulation resistance and are prone to dielectric breakdown. Plastic dielectric capacitors have superior moisture characteristics in that they are nonabsorbent.

o Seal. All units should be hermetically sealed. Small amounts of moisture can increase the rate of chemical reactions within the capacitor materials.

o Mounting. Capacitors with lengths of 1.375 or widths of 0.672 inches or greater should not be supported by their leads. These capacitors should be provided with a supplementary means for mounting, such as tangential brackets. To keep inductance to a minimum, the capacitors should be installed close to the source so that the lead length is as short as possible. The output lead should be kept away from the input lead. In severe cases the input lead should be shielded. Good bonding is extremely important in the installation of capacitors.

o AC Operation. When AC operation is required, care should be taken to ensure that: (a) the sum of the DC voltage and the peak AC voltage does not exceed the DC voltage rating; and (b) the AC voltage does not exceed 20 percent of the DC voltage rating or the value calculated from the following equation whichever is smaller:

$$V_pAC = \frac{(T_{dc} - T_a) \cdot A \cdot e}{T_a \cdot f \cdot C \cdot D}$$

Where:

V_pAC = peak value of AC component

f = Frequency in Hertz of AC component

D = 2 (maximum derating factor (DF) at applicable high test temperature)

C = Nominal capacitance in farads

A = Exposed capacitor case surface area in square centimeters (cm), exclusive of portion occupied by terminal mountings

T_{dc} = Applicable high test temperature in degrees Celsius

T_a = Maximum ambient operating temperature expected within equipment containing capacitor

e = Convection coefficient in watts per $cm^2/^oC$ (the value of "e" is approximately equal to 0.0006).

o Faults or "Clearings". For metallized paper and plastic capacitors, where the conducting plates have thicknesses in the micrometer or submicrometer range, a puncture of the dielectric can cause a relatively harmless vaporization of a small area of the plates (known as "clearings") with the effect of a noise spike and a small reduction of total capacitance. These phenomena are not considered failures of the capacitor, until enough of them occur to cause significant reduction in capacitance. However, metallized plastic capacitors should not be used in timing or memory (storage) circuits or anywhere a momentary breakdown in the dielectric cannot be tolerated. They should not be used in high impedance or low energy circuits where the fault will not clear.

5.2.4.4 MIL-C-20, CAPACITORS, FIXED, CERAMIC DIELECTRIC (TEMPERATURE COMPENSATION), ESTABLISHED RELIABILITY (STYLE CCR)

5.2.4.4.1 SPECIAL CONSIDERATIONS

o Capacitance Tolerance. These capacitors come in tolerances of ± .25pf, ± .5pf, ±1%, ±2%, ±5% and ±10%. However, regardless of the purchase tolerance, the design should tolerate a ±1% absolute change in capacitance value to assure long life reliability in military applications. The temperature characteristics, however, are expected to remain virtually unchanged throughout the life of the capacitor.

o Dielectric Strength. Where the capacitor body normally contacts parts with a potential difference of more than 750 volts, supplementary insulation should be used.

o Temperature Coefficient. These capacitors exhibit a zero +30 PPM temperature coefficient over the temperature range of -55°C to +125°C.

o Operating Frequency. These capacitors are suitable for operating frequencies ranging from 1 KHz to 300 MHz.

5.2.4.5 MIL-C-81, CAPACITORS, VARIABLE, CERAMIC DIELECTRIC (STYLE CV)

5.2.4.5.1 SPECIAL CONSIDERATIONS

o Temperature-Capacitance Characteristics. Changes in nominal capacitance from the values measured at +25°C may vary from -4.5% to +14% at -55°C or -10% to +2% at +85°C when measurements are made: (1) after the capacitors have reached thermal stability; (2) at a frequency range of 0.1 to 0.2 MHz and with the capacitor charged from 80 to 90% of maximum capacity.

o Drift with Age. The capacitance drift over time is within 0.5pf.

o Mounting. These capacitors may be mounted close to a metal panel with little increase in capacitance. To avoid cracking or chipping of the ceramic mounting base, a resilient mounting (or mounting surface spacer) should be used.

o Stability. Even though these capacitors are relatively stable under shock and vibration (which tend to cause changes in capacitance), air trimmers due to their low mass should be used where higher order of stability is required.

5.2.4.6 MIL-C-10950, CAPACITORS, FIXED, MICA DIELECTRIC, BUTTON STYLE (STYLE CB)

5.2.4.6.1 SPECIAL CONSIDERATIONS

o Seal. These capacitors are hermetically glass sealed, except for style CB50, which is resin sealed.

5.2.4.7 MIL-C-11015, CAPACITORS, FIXED, CERAMIC DIELECTRIC (GENERAL PURPOSE) (STYLE CK)

5.2.4.7.1 SPECIAL CONSIDERATIONS - See MIL-C-20 Notes

5.2.4.8 MIL-C-14409, CAPACITORS, VARIABLE (PISTON TYPE, TABULAR TRIMMER), (STYLE PC)

5.2.4.8.1 SPECIAL CONSIDERATIONS

o Stability. Because of their low mass, these capacitors are relatively stable under shock and vibration.

o Linearity and Backlash. The capacitance change is linear with respect to rotation within +10%. Backlash is virtually nonexistent except on Styles PC39 and PC43 which can have a backlash of 2%.

o Torque. For styles PC25 and PC26 capacitor, the driving torque is between 0.5 and 6.0 ounce-inches over the temperature range (-55 to +125°C); on all other styles, the driving torque is 16 ounce-inches maximum at -55°C and 1 to 10 ounce-inches at all other temperatures within the operating temperature range.

o AC Operation. In AC operation, the sum of the peak AC voltage and any DC bias should not exceed its voltage derating value.

o Construction. Styles PC25 and PC26 capacitors are constructed with a series of concentric circular metal bands forming plates which interleave. The capacitance is varied by adjustment of the relative depth of engagement of the metal bands. All other style capacitors are constructed of glass or quartz dielectric cylinders and metal tuning pistons. A portion of the cylinder is plated with metal to form the stator. The metal piston, controlled by a tuning screw, acts as the rotor. Overlap of the stator and rotor determines the capacitance. The self-contained piston within the dielectric cylinder functions as a low inductance coaxial assembly.

5.2.4.9 MIL-C-19978, CAPACITORS, FIXED, PLASTIC (OR PAPER-PLASTIC), DIELECTRIC (HERMETICALLY SEALED IN METAL CASES), ESTABLISHED RELIABILITY (STYLE COR)

5.2.4.9.1 SPECIAL CONSIDERATIONS

o Use

- Polyethylene terephthalate (characteristic M capacitors) - Characteristic M capacitors are intended for high temperature applications similar to those served by hermetically sealed paper capacitors. Most of these capacitors also exhibit high insulation resistance at the upper temperature limits. Mylar units, however, should not be used above 85°C.

- Paper and polyethylene terephthalate (characteristic K capacitors)- Characteristic K capacitors are intended for applications where high insulation resistance is necessary.

- Polycarbonate (characteristic Q capacitors) - Characteristic Q capacitors are intended for applications where minimum capacitance changes with temperature are required. These capacitors are especially suitable for use in tuned and precision timing circuits.

o Capacitance Tolerance. These capacitors come with tolerances of ±2%, ±5% and ±10%. However, regardless of the purchase tolerance, designs using these capacitors should tolerate a ±2% change in capacitance value to assure long life reliability in military applications.

o Barometric Pressure (Flashover) for Metal-Cased Tubular Capacitors. The DC voltage that can be applied to metal-cased tubular capacitors at different altitudes can be obtained from Figure 5.2.4.9-1. The DC voltage should not exceed the specified derating levels.

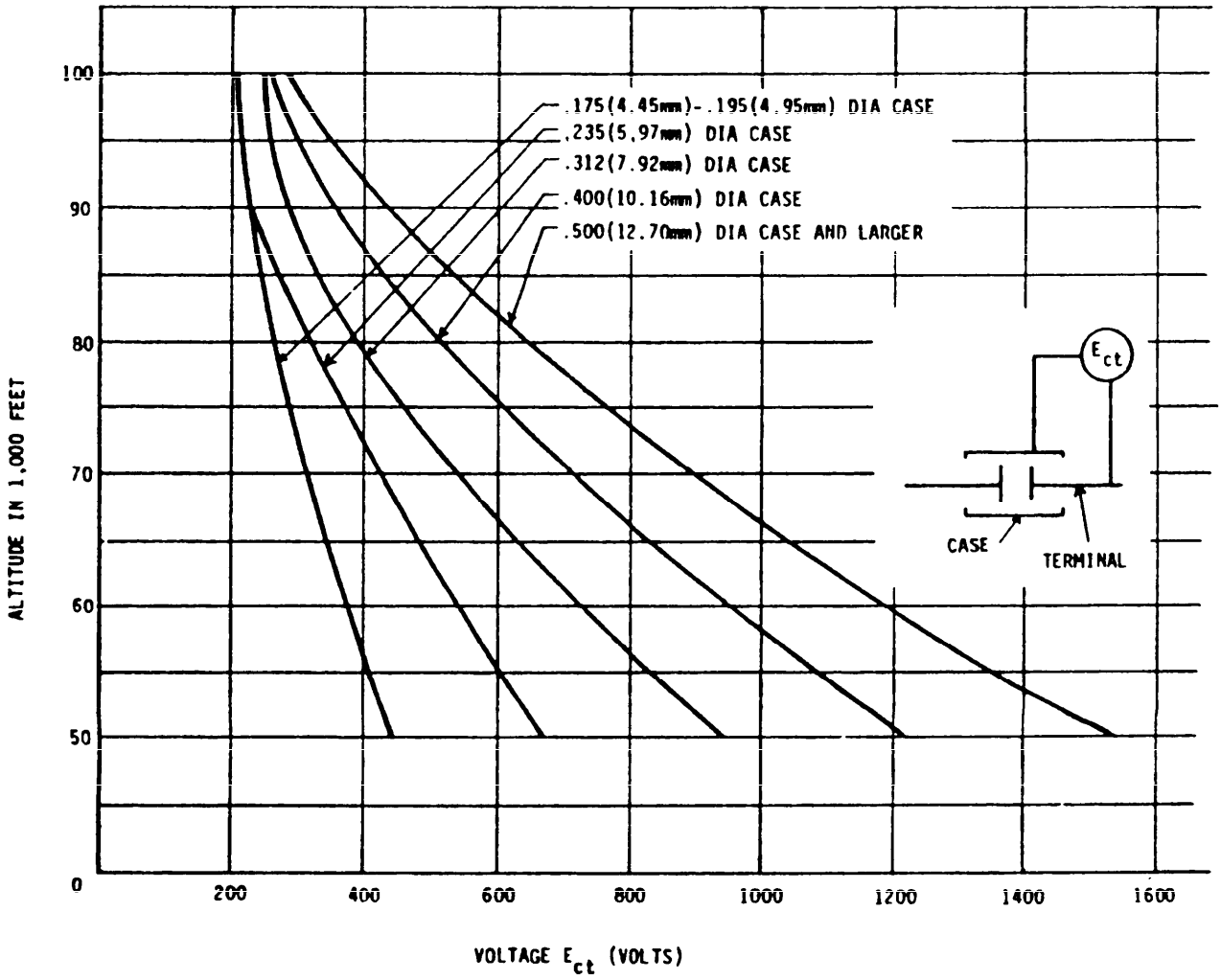


FIGURE 5.2.4.9-1: MAXIMUM DC VOLTAGE-VS-ALTITUDE RATINGS FOR MIL-C-19978 METAL CASED, TUBULAR CAPACITORS

5.2.4.10 MIL-C-23183, CAPACITORS, FIXED OR VARIABLE, GAS OR VACUUM DIELECTRIC, CERAMIC, CERAMIC OR GLASS ENVELOPE (STYLE CG)

5.2.4.10.1 SPECIAL CONSIDERATIONS

o Voltage Rating. The voltage indicated in the type designation data is the 60Hz test voltage, at maximum capacitance. This is the absolute maximum voltage the unit can withstand before breakdown occurs. The breakdown voltage is greater at capacitances less than maximum, becoming as much as 300% greater at minimum capacitance for lower voltage units. The breakdown voltage at radio frequencies is the same as for low frequencies up to about 2.5MHz, and becomes about 10% lower at 30MHz. The continuous duty operating voltage is lower for higher frequencies. The continuous RF rating of a vacuum capacitor is arbitrarily defined as that voltage and current that will raise the temperature to a steady 85°C without cooling apparatus. This rating can be increased by additional cooling such as blowers, heat sinks, or water cooling.

5.2.4.11 MIL-C-23269, CAPACITORS, FIXED, GLASS DIELECTRIC, ESTABLISHED RELIABILITY (STYLE CYR)

5.2.4.11.1 SPECIAL CONSIDERATIONS

o Capacitance Tolerance. These capacitors come with tolerances of ±1%, ±2% and ±5%. However, regardless of purchase tolerance, the design should be able to tolerate a ±1% change in capacitance value to assure long life reliability in military applications.

o Temperature Coefficient and Capacitance Drift. These capacitors are available with three temperature coefficients. For the axial lead capacitors, the temperature coefficient is 140 ±25PPM/°C or 0 ±25PPM/°C (for style CYR41). For the axial-radial lead capacitors, the temperature coefficient is 105 ±25PPM/°C. The capacitance drift is ±0.1% or 0.1pf, whichever is greater, for all capacitors.

o AC Operation. When AC operation is required, the peak voltage plus any DC bias should not exceed the value established by the derating requirements.

o Quality Factor "Q". These capacitors exhibit a much higher "Q" factor over a wider capacitance range than mica dielectric capacitors where "Q" is the ratio of reactance to effective resistance.

5.2.4.12 MIL-C-39001, CAPACITORS, FIXED, MICA DIELECTRIC, ESTABLISHED RELIABILITY (STYLE CMR)

5.2.4.12.1 SPECIAL CONSIDERATIONS

o Capacitance Tolerance. These capacitors come with tolerances of ±0.5 pf, ±1%, ±2% and ±5%. However, regardless of the purchase tolerance, the design should tolerate a ±0.5% change in capacitance value to assure long life reliability in military applications.

o Operating Frequency. These capacitors perform very well at frequencies up to 500 MHz with a typical operating frequency range of 10 KHz to 500 MHz.

o Insulation Resistance. These capacitors have very high insulation resistance and low dissipation factors.

5.2.4.13 MIL-C-39003, CAPACITORS, FIXED, ELECTROLYTIC (SOLID ELECTROLYTE), TANTALUM, ESTABLISHED RELIABILITY (STYLE CSR)

5.2.4.13.1 SPECIAL CONSIDERATIONS

o Temperature Coefficient. Because their passive electrolyte is solid and dry, these capacitors are not temperature sensitive; they have a lower capacitance-temperature characteristic than any of the other electrolytic capacitors.

o Dielectric Absorption. These capacitors exhibit the characteristic of dielectric absorption whereby a voltage across them will reappear after they have been shorted. This should be considered in their use in RC timing circuits, triggering systems and phase shift networks.

o Reverse Voltage. These capacitors should never be exposed to dc or peak ac voltages greater than 2% of their rated dc voltage in the reverse of the normal polarization.

o Mounting. Supplementary mounting means should be used where the application of these capacitors involves vibration frequencies above 55Hz.

5.2.4.14 MIL-C-39006, CAPACITORS, FIXED, ELECTROLYTIC (NON-SOLID ELECTROLYTE) TANTALUM, ESTABLISHED RELIABILITY (STYLE CLR)

5.2.4.14.1 SPECIAL CONSIDERATIONS

These capacitors are recommended for use where high capacitance is required in a small volume, at medium to high voltages. The nonsolid (wet) electrolyte capacitors fall into four broad categories, which vary substantially in pertinent characteristics.

o Sintered Slug (Type CLR65 and CLR79). The CLR65 is the most popular type, because it provides the greatest volumetric efficiency (ratio of capacitance to voltage rating, and case size) of any capacitor in the medium voltage range (up to 125 volts). The CLR65 is available with capacitance tolerances of +5%, +10% and +20%; however, the variation of capacitance with temperature is quite large, especially for the "higher capacitance series." The CLR65 uses silver plated cases to contain the sulfuric acid (H_2SO_4) electrolyte. The silver migrates if the capacitor is subjected to voltage reversals, resulting in catastrophic failures.

The recently introduced CLR79 types have most of the features of the CLR65, but utilize tantalum cases. The CLR79 does not require the silver plating of the CLR65 and the tantalum is impervious to attack by H_2SO_4.

o Plain Foil (Type CLR35 and CLR37). These capacitors are characterized by their high voltage ratings (up to 450 volts). They are comparatively larger than the sintered slug or etched foil types for a given capacitance value and have only moderate purchase tolerances (±20%).

o Etched Foil Nonpolarized (Type CLR25 and CLR27). These capacitors provide substantial improvements in volumetric efficiency over the plain foil types, and are available in higher voltage ratings than the sintered slug types. They are characterized by extremely high capacitance values (up to 580uF) but have broad purchase tolerances (+75% to -15%).

o Life Tolerance. As described above, these capacitors come with various tolerances from -15% to +75%. However, regardless of the purchase tolerance, the design should be able to tolerate an additional 10% reduction in capacitance as compared to the initial value, to compensate for the cumulative effects of temperature and aging over the life of these capacitors.

o Polarization. CLR style capacitors are polarized except for styles CLR27 and CLR37. Nonpolarized types are primarily suitable for AC applications or where DC voltage reversals can occur. Examples of these uses are in: (a) tuned low frequency circuits; (b) phasing of low voltage AC motors; (c) computer circuits and (d) servo systems.

o Series Operation. Whenever these capacitors are connected in series for higher voltage operation, a resistor should be paralleled across each unit. Unless a shunt resistor is used, the DC rated voltage can easily be exceeded on the capacitor in the series network depending upon the capacitance, the average DC leakage and the capacitor construction.

o Parallel Operation. When these capacitors are operated in parallel, care should be taken to assure that the sum of the peak voltage ripple and the applied DC voltage does not exceed the DC rated voltage. The connecting leads of the parallel network should be large enough to carry the combined currents without reducing the effective capacitance resulting from series lead resistance.

o High Capacitance Series. It is not recommended to select the highest capacitance value suitable for a given voltage rating and case size. In some of the MIL-C-39006 detail specifications, these capacitors are flagged by an "*". Reasons for not selecting these capacitors are:

(a) They represent the ultimate in the capability of the manufacturing process. They are thus less predictable, and inherently less reliable.

(b) They are typically much more expensive than the lower capacitance values in the same voltage rating and case sizes.

(c) In the process of manufacture, the "forming" voltage will generally be lower (as a ratio of the rated operating voltage) than for lower capacitance values, providing a lesser margin of safety.

(d) They will typically exhibit a greater decrease of capacitance at low temperature, and thus provide only an illusion of higher capacitance in the actual operating environment.

o Hermetic Seal. Only hermetically sealed capacitors should be used. The use of the liquid or gelled electrolyte absolutely precludes the use of nonhermetic types. The nonhermetic types have been proven unreliable because the electrolyte can escape, either in a liquid or gaseous form, reducing the capacitance and causing catastrophic failure under extended exposure to military service environments.

o Restricted Use of Wet Slug Tantalum Capacitors. The order of preference for the selection of the types described above is as follows:

(a) Sintered Slug, Tantalum Case (Type CLR79)
(b) Plain Foil, (Type CLR35 and CLR37)
(c) Etched Foil (Type CLR25 and CLR27)

Wet slug tantalum capacitors cannot be used on Naval Air Systems Command programs without approval. Wet slug capacitors other than MIL-C-39006/22 (CLR79) cannot be used on other programs without approval.

5.2.4.15 MIL-C-39014, CAPACITORS, FIXED, CERAMIC DIELECTRIC (GENERAL PURPOSE), ESTABLISHED RELIABILITY (STYLE CKR)

5.2.4.15.1 SPECIAL CONSIDERATIONS

o Capacitance Tolerance. These capacitors are available with initial tolerances of +10% or +20%. However, regardless of the purchase tolerance, the design should be able to tolerate a +20% change in capacitance value to assure long life reliability in military applications.

o Operating Frequency. The typical operating frequency range is from 1KHz to 300MHz.

o Capacitance To Size Ratio. These capacitors have the largest capacitance to size ratios of all high resistance dielectric capacitors.

o Humid Operating Conditions. Ceramic materials are nonhygroscopic, effectively impermeable and have practically no moisture absorption even after considerable exposure to highly humid conditions. These capacitors are intended to operate, through their full temperature range, at relative humidities up to 95%. However, the terminal materials under high moisture conditions can be subject to ionic migration which can cause capacitor failure.

o AC Operation. When AC operation is required, the peak AC voltage plus any DC bias should not exceed the derated values established by the derating requirements.

o Mounting. These capacitors are used to compensate circuit performance for temperature variations. Therefore, they should be mounted in close proximity to the part (or parts) they are intended to compensate, and isolated from parts that dissipate local heat. Otherwise thermal gradients will defeat the designed in compensation capability.

o Frequency. Since the ceramic dielectric is frequency sensitive, both capacitance and capacitance change with temperature will be different at various measuring frequencies. For extremely accurate compensation, the compensation characteristics should be measured at the proposed operating frequency.

5.2.4.16 MIL-C-39018, CAPACITORS, FIXED, ELECTROLYTIC (ALUMINUM OXIDE) (STYLES CU AND CUR), ESTABLISHED RELIABILITY AND NONESTABLISHED RELIABILITY

5.2.4.16.1 SPECIAL CONSIDERATIONS

o Operating Frequency. These capacitors are recommended for use in the frequency range of 60 to 10,000 Hz.

o Polarization. Type CU15 is nonpolarized; other types (CUR13, CUR17, CUR19, CUR71 and CUR91) are polarized. Therefore, in the applications where reversal of polarity occurs only CU15 should be used. The polarized capacitors (CUR13, CUR17, CUR19, CUR71 and CUR91) should be used only in DC circuits with polarity properly observed. Style CUR13 and CUR17 have a 3-volt reverse voltage limitation for units rated at 10 volts or greater.

Styles CUR19, CUR71 and CUR91 have reverse voltage limitations of 1.5 volts. If AC components are present, the sum of the peak AC voltage plus the applied DC voltage should not exceed the derating value. The proper polarity should be maintained even on negative peaks, to avoid overheating and damage.

o Seal. Even though these capacitors have vents designed to open at dangerous pressures, explosions can occur because of gas pressure buildup or a spark ignition of free oxygen and hydrogen liberated at the electrode. Provisions should be made to protect surrounding parts.

o Environmental Restrictions. These capacitors should not be subjected to low barometric pressures and low temperature. Therefore they should not be used for airborne applications without prior approval by the acquiring activity.

o Surge Voltage. The surge voltage is the maximum voltage to which the capacitor should be subjected. This includes transients and peak ripple at the highest line voltage. For maximum reliability and long life, the DC working voltage should not be more than 80% of the full voltage rating so that surges can be kept within the full rated working voltage. Surge voltage application should not occur more than 30 seconds every 10 minutes.

o Cleaning Solvents. Recommended solvents include those free of halogen or halogen groups, such as toluene, methanol, methylcellosolve, alkinox and water, and naphtha. Chlorinated or fluroinated hydrocarbon solvents should not be used for cleaning these capacitors.

5.2.4.17 MIL-C-39022, CAPACITORS, FIXED, METALLIZED, PAPER PLASTIC FILM OR PLASTIC DIELECTRIC, DIRECT AND ALTERNATING CURRENT (HERMETICALLY SEALED IN METAL CASES), ESTABLISHED RELIABILITY (STYLE CHR)

5.2.4.17.1 SPECIAL CONSIDERATIONS

o Capacitance Tolerance. These capacitors come in tolerances of ±5% and ±10%. However, regardless of the purchase tolerance, the design should be able to tolerate a ±2% change in capacitance value to assure long life reliability in military applications.

o Capacitance-Temperature Characteristics. The capacitors with "Mylar" or polycarbonate dielectric offer very low (on the order of ±1%) capacitance change with temperature over the operating temperature range.

5.2.4.18 MIL-C-55365, CAPACITORS, CHIP, FIXED, TANTALUM, ESTABLISHED RELIABILITY (STYLE CWR)

5.2.4.18.1 SPECIAL CONSIDERATIONS

o Surge Voltage. The surge voltage should not exceed 130% of the steady state voltage derating.

o AC Operation. In AC operation, the sum of the AC plus any DC voltage should not exceed the voltage derating.

o Mounting. These capacitors are designed for mounting by reflow solder or conductive epoxy in circuit substrates. The use of a heat column or controlled hot plate is recommended for reflow procedures. Caution must be exercised to limit temperature to 300°C maximum during reflow or premature degradation of the solid electrolyte will occur. Conductive epoxies and solder paste creams are very useful in production situations because they can be accurately and rapidly screened on to the pads using masks. Also, they have a pre-cure tackiness permitting chip placement before the epoxy is cured. Conductive epoxies have the advantage of low temperature curing; however, the cold temperature cure characteristics of physical strength and conductivity may not be as good as some soft solders. To prevent thermal shock, the substrate with chip capacitors in place should be heated slowly to the reflow temperature.

5.2.4.19 MIL-C-55514, CAPACITORS, FIXED, PLASTIC (OR METALLIZED PLASTIC) DIELECTRIC, DC (IN NON-METAL CASES), ESTABLISHED RELIABILITY (STYLE CFR)

5.2.4.19.1 SPECIAL CONSIDERATIONS - See Notes for MIL-C-39022

5.2.4.20 MIL-C-55681, CAPACITORS, CHIP, MULTILAYER, FIXED, CERMIC DIELECTRIC, ESTABLISHED RELIABILITY (STYLE CDR)

5.2.4.20.1 SPECIAL CONSIDERATIONS

o Capacitance Tolerance. These capacitors are available with capacitance tolerances of ±5%, ±10% and ±20%.

o AC Operation. In AC operations, the sum of the AC and any DC bias should not exceed the rated DC voltage.

o Effect of Mounting. Voltage-temperature limits, resistance to thermal shock, and reliability can be affected as a result of mounting on substrates with dissimilar coefficients of expansion from capacitor material. Care should be taken in the selection of substrate material.

5.2.4.21 DERATING FACTORS

The use of a parts derating technique as a means of enhancing both component and equipment reliability is discussed at length in Section 6.2.1, Volume 2 of this Handbook.

The minimum derating criteria for capacitors are tabulated in Table 5.2.4.21-1.

TABLE 5.2.4.21-1: CAPACITOR DERATING

Type	Spec	Style	Max. % of Rated Voltage (Note 1)	Max. % of Rated Current (Note 2)	Temperature Derating (°C) (Note 3)
Mica	MIL-C-39001	CMR	.5	.7	10
Glass	MIL-C-23269	CYR	.5	.7	10
Tantalum Nonsolid Electrolytic (Note 10)	MIL-C-39006	CLR	.5 (Note 8)	.7	20 (Note 4)
Solid Tantalum Electrolytic	MIL-C-39003	CSR	.6 (Note 6)	.7 (Note 5)	20 (Note 4)
Aluminum Electrolytic	MIL-C-39018	CUR	.8 (Notes 11 and 12)	.7	10
Paper, Plastic & Metallized Dielectric	MIL-C-19978 MIL-C-39022 MIL-C-55514 MIL-C-83421	CQR CHR CFR CHR	.5 .5 (Note 7)	.7 .7	10 10
Ceramic Temperature Compensating	MIL-C-20	CCR	.5	-	10
Ceramic	MIL-C-39014	CKR	.1min,.5 max (Note 9)	.7	10
Ceramic, Variable	MIL-C-81	CV	.5	.7	10
Glass, Variable	MIL-C-14409	PC	.5	.7	10

NOTES:

1) Derated voltage applies to the sum of the DC polarizing voltage and AC peak voltage.

2) Initial surge current and ripple current.

3) Device temperature (ambient and internal temperature rise due to ripple current) should not exceed rated temperature less derating value.

4) The maximum rated voltage for CLR and CSR capacitors must be derated between 85°C and 125°C before applying the derating factors. The formula is:

$$V(\text{Allowed}) = V(85^\circ \text{ Rated}) \left[1 - 0.33 \left(TA - 85/125^\circ - 85\right)\right]$$

where:
V = Voltage Rating at 85°C
TA = Maximum ambient temperature

5) Effective series resistance required, 3 ohm/volt minimum.

6) Reverse voltage should not exceed 2% of rated voltage.

7) Excessive voltage derating is not recommended for metallized film capacitors. Applied voltage should be sufficient (.10 volts or greater and circuit series resistance less than 1K ohm) to support self-healing phenomenon.

8) Polarized CLR styles have extremely low or zero reverse bias limits (examples of the latter are the CLR65 and CLR69). Designers must verify the reverse bias limitations for selected styles and comply with them. Violating reverse bias limits even in transient conditions will lead to rapid catastrophic failure.

9) Avoid combination of high voltage and high humidity due to silver migration.

10) Foil type tantalum electrolytic capacitors styles CLR25, CLR27, CLR35 and CLR37 and wet slug type tantalum electrolytic capacitor style CLR79 are approved for use. The use of all other styles must be justified and approved.

11) Aluminum electrolytic capacitors should not be used without prior approval of their application.

12) Excessive derating of aluminum electrolytic capacitors is not recommended. DC working voltage should be as near to as practical, but not greater than, 0.8 x the surge voltage rating of the capacitor.

5.2.5 MAGNETIC DEVICES

5.2.5.1 INTRODUCTION

There are three categories of magnetic devices - transformers, inductors and coils. Standard magnetic devices are listed in MIL-STD-1286 and are selected from among devices covered by applicable MIL specifications. Most transformers, inductors and coils used in military aerospace applications are custom designed for minimum size and weight or to fit space available in compact equipment. As a result, relatively little standardization of electrical parameters has occurred. However, a family of standard sizes shall be used whenever possible, even if the electrical characteristics of the new devices are unique.

5.2.5.2 DEVICE SELECTION

The selection of a given magnetic device is governed by the criteria depicted in Table 5.2.5.2-1. Selection and usage guidelines are portrayed in Table 5.2.5.2-2.

TABLE 5.2.5.2-1: MAGNETIC DEVICES SELECTION CRITERIA

1. MIL-STD-1286 Transformers, Inductors and Coils, "Selection and Use of"

2. Established Reliability Specifications:

MIL-C-39010	Coil, Fixed, RF, Molded, Established Reliability, General Specification For

3. Other MIL specifications:

MIL-T-27	Transformers and Inductors, Audio, Power and High Power Pulse, General Specification For
MIL-C-15305	Coil, Fixed and Variable, RF, General Specification For
MIL-T-21038	Transformers, Pulse, Low Power, General Specification For
MIL-T-55631	Transformers, IF, RF, and Discriminator, General Specification For
MIL-T-83720	Transformers and Inductors, Nonexplosive, General Specification For
MIL-T-83721	Transformers, Variable, Power, General Specification For

4. Historical test data (from similar applications or other engineering information and/or data that provides assurance that the device is sufficiently rugged and reliable for the application (e.g., previous use in military equipment, comparable application or GFE).

modification and delete the deleted as a result of the

TABLE 5.2.5.2-2: SELECTION AND USAGE GUIDELINES FOR MAGNETIC DEVICES

Military Specifications	Functional Type	Style	Construction Grade	Temperature Class	Max Operating Temperature	Usage Notes
MIL-T-27	Transformer, Power, Step Up/Step Down	Metal Cased or Encapsulated or Open	4 5 6	Q R S T U V	85°C 105 130 155 170 170+	Transformers that drive rectifier circuits with capacitance filters require special consideration since the external load current is the average of the pulsed current from the transformer and the dissipation in the transformer is proportional to the average value of I^2. The result is that small changes in load current result in inordinately large changes in transformer dissipation. Power transformers are designed to operate efficiently over a limited frequency range. Operation outside this range, particularly at lower frequencies will result in overheating.
MIL-T-27	Inductor, Power	Same as above				Power inductors are designed to operate efficiently over a limited frequency range. Operation outside this range, particularly at lower frequencies, will result in overheating. Power inductors used as filters usually carry a large direct current component. If this component exceeds the value specified, the inductance can be reduced because of core saturation.
MIL-T-27	Transformer, Audio Frequency	Same as above				Audio transformers are not normally designed to accommodate any direct current. Small amounts of direct current can cause core saturation effects yielding significant performance degradation, especially at low frequencies.
MIL-T-27 MIL-T-27	Inductor, Audio Frequency Transformers, High Power, Pulse	Same as above				

TABLE 5.2.5.2-2: SELECTION AND USAGE GUIDELINES FOR MAGNETIC DEVICES (Cont'd)

Military Specifications	Functional Type	Style	Construction Grade	Temperature Class	Max Operating Temperature	Usage Notes
MIL-C-15305	Coils, RF Fixed (K) Coils, RF Variable (V)	Immersion or Moisture Resistant or Moisture Resistant or For use in sealed assemblies	1 2 3	O A B C	85°C 105 125 125+	Variable magnetic devices should not be used if fixed devices can meet circuit requirements due to the high failure rates of the variable devices. When a variable device must be used, the travel of the roller or slider used in contact with the conductor shall be limited to prevent its leaving the conductor.
MIL-T-21038	Transformer, Low Power	Metal Cased or Encapsulated	4 and 6 5 and 7	Q R S T U V	85°C 105 130 155 170 170+	
MIL-C-39010	Coils, RF Molded, Established Reliability	Phenolic Core-Iron Sleeve, Iron Core - Iron Sleeve, Ferrite Core - Ferrite Sleeve, Phenolic Core Powdered Iron Core or Ferrite Core	N.A.	A B C	105°C 125 150	Failure Rate Level: M - 1.0%/1000 hrs; P - 0.1%/1000 hrs; R - 0.01%/1000 hrs; S - 0.001%/1000 hrs Inductance Tolerance: J - ±5%; K - ±10%; L - ±20%
MIL-T-55631	Transformer, IF (Type I) or RF (Type II) or Discriminator (Type III)	Immersion or Moisture Resistant or Moisture Resistant or For use in sealed assemblies	1 2 3	O A B C	85°C 105 125 125+	These transformers are used in tuned or untuned intermediate, radio frequency and discriminator circuits. These inductive components should be considered with additional circuit elements, such as capacitors and resistors, that are functionally related to the inductive element for the purpose of coupling, impedance conversion and isolation.
MIL-T-83721	Transformer, Power Variable	Not Applicable		I II	55°C (1) 100 (1)	These transformers consist of tapped and continuously variable transformers. They are either manually operated or motor driven. Also included are variable transformers used for aircraft light dimming. Class I-Transformers exceeding 2 lbs. in weight Class II-Transformers weighing 2 lbs. or less

(1) Maximum Temperature rise above ambient

5.2.5.2.1 PARAMETER VARIATION

Magnetic devices may suffer changes in parameter values over their operational life. Therefore, for long life reliability the equipment design should be able to tolerate parameter shifts as shown in Table 5.2.5.2-3 below:

TABLE 5.2.5.2-3: VARIATIONS DUE TO LIFE AND ENVIRONMENTS OVER SPECIFICATIONS

Parameter	Expected Drift Magnitude		
	MIL-T-27	MIL-C-15305	MIL-T-21038
Inductance	±10%	±5%	±10%
Resistance	±10%	±10%	±10%
Pulse Parameters	±10%		±10%
Q Factor		-50%	

5.2.5.2.2 FAILURE MODES AND MECHANISMS

The failures in magnetic devices fall into three categories: (a) insulation breakdown, (b) open conductors, and (c) magnetic core characteristic changes.

o Insulation Breakdown. Insulation breakdown can result from moisture penetration; poor insulation on conductors, between layers, or to the magnetic core; or as a prolonged "hot spot" or sustained overload. Conduction from one turn to another results in a "shorted turn" effect, causing high power consumption. This additional power is dissipated in the transformer, causing further heat.

o Insulation Breakdown - Inductors, Coils. Insulation breakdown in these devices results in degraded performance, since the impedance is reduced but the power consumption is usually not increased enough to cause open conductors. If the device is a filter inductor, hum or ripple will increase. If it is a radio frequency coil used as a transistor load impedance, the circuit gain may be greatly reduced.

o Open Conductor. This type of failure is almost always catastrophic in nature. Transformers will have no output and coils or inductors will have infinite impedance and resistance.

o Magnetic Core Characteristics. Excessive temperatures can cause changes in magnetic effects resulting in variations in circuit performance.

5.2.5.3 GENERAL APPLICATION CONSIDERATIONS

o Temperature Class. The device must be designed for the proper temperature range in which it is to operate. Excessive hot spot temperatures can cause degradation and aging of insulation materials. The proper "Class" of insulation must be selected for expected operating and hot spot temperature conditions. Hot spot temperature is a critical factor in the MIL-HDBK-217 failure rate prediction. Devices dissipating high power should be mounted on heat sinks or cold platter and/or cooled via forced convection. Similar to resistors, the allowable power rating of these devices decreases with increases in temperature.

o Construction Grade. The devices must be constructed in accordance with the proper military "Grade" for the environment in which they will be applied. Due consideration should be given to the use of immersion and moisture resistance styles/construction grades, since the entrance of moisture and humidity degrades the dielectric properties of the insulating material and could cause corrosion and electrolytic action within the device.

o Resistance Change With Temperature. The temperature coefficient of resistance for copper windings is approximately 0.4%/°C. This change in resistance can be significant in some applications.

o Shielding. Electrostatic or electromagnetic shielding may be required in low level circuits to avoid noise or hum pickup.

5.2.5.3.1 DERATING REQUIREMENTS

Derating criteria for magnetic devices and current limitations for wire size used in the device are provided in Tables 5.2.5.3-1 and 5.2.5.3-2, respectively.

TABLE 5.2.5.3-1: DERATING CRITERIA FOR TRANSFORMERS, INDUCTORS AND COILS

Derating Parameter	Derate to % of Rated
Power	50
Current Density	2 ma/circ. mil wire dia.
Current (Continuous)	60
Current (Surge)	90
Voltage (Continuous)	60
Voltage (Surge)	90
Hot Spot Temperature (Operating)	75
Insulation Breakdown Voltage (Winding to Winding, Winding to Core and Winding to Case)	50

TABLE 5.2.5.3-2: CURRENT DERATING FOR WIRE SIZE USED IN CONSTRUCTION OF TRANSFORMERS, INDUCTORS AND COILS

AWG No.	Max. Amps	AWG No.	Max. Amps
42	.010	20	2.40
40	.025	18	4.40
38	.040	16	5.50
36	.060	14	9.00
34	.100	12	11.0
32	.153	10	15.0
30	.250	8	21.0
28	.400	6	28.0
26	.635	4	38.0
24	1.02	2	52.0
22	1.45		

5.2.6 RELAYS

5.2.6.1 INTRODUCTION

A relay is an electrically controlled device that opens and closes electrical contacts to operate other devices in the same or another electrical circuit. There are two basic categories of relays: electromechanical and solid state. In an electromechanical device mechanical linkages are actuated by an electrical coil which joins or separates electrically conductive mechanical contacts. Solid state relays are divided into two categories: pure solid state and hybrids. Pure solid state relays accomplish their switching function by means of an arrangement of semiconductors and passive circuit devices; hybrid relays are a combination of solid state circuitry and electromechanical linkages in a single package. The solid state circuit drives the electromechanical relay to perform the switching function. Electromechanical relays represent the oldest device design and are by far the most widely used. In general, relays are used to:

- Obtain isolation between input and output circuits.
- Invert the signal sense (from open to closed and vice versa)
- Control numerous output circuits (so as to transfer more than one load)
- Switch loads of different voltage or current ratings
- Retain an input signal
- Interlock circuits
- Provide remote control
- Create remote time delay actions

5.2.6.2 DEVICE SELECTION

Standard relays are specified in MIL-STD-1346. Relay selection should be based upon the function to be performed. Table 5.2.6.2-1 summarizes relay types and their applicability to various functions. Where more than one type of relay can be used in a given application, consideration should be given to cost and availability. Relay selection shall be governed by the criteria of Table 5.2.6.2-2.

TABLE 5.2.6.2-1: SELECTION-FUNCTION GUIDE FOR RELAYS

RELAY FUNCTION	APPLICABLE SPECIFICATION MIL-R-						
	5757	6106	28750	39016	83726	28776	83725
For Electronic and Communication Type Equipment, General Purpose							
DC Operated	X			X			
AC Operated	X						
Sensitive	X			X			
Hybrid						X	
General Purpose							
DC Operated		X					
AC Operated		X					
Electromagnetic, Established Reliability		X		X			
Latching							
DC Operated	X	X		X			
AC Operated		X					
AC/DC Operated		X					
Reed Type							
Dry Reed	X						
Time Delay Type							
Electric and Electronic					X		
Solid State			X				
Vacuum, High Voltage							X

TABLE 5.2.6.2-2: RELAY SELECTION CRITERIA

1. MIL-STD-1346, "Relays, Selection and Use of" (Applicable military specifications are listed in Table 4-13).

2. MIL-STD-454, Notice 1, "Standard General Requirements for Electronic Equipment," Requirement No. 57.

3. MIL-R-39016, "Relays, Electromagnetic, Established Reliability, General Specification for."

4. Other military relay specifications.

5. Historical test data (from similar applications or other engineering information and/or data that provides assurance that the device is sufficiently rugged and reliable for the application (e.g., previous use in military equipment, comparable application or GFE).

Where use of a nonstandard device is necessary, request for approval of this device shall be made to military agencies according to the requirements and procedures of MIL-STD-965.

5.2.6.3 APPLICATION CONSIDERATIONS

Applicable MIL specifications for relays are shown in Table 5.2.6.3-1.

TABLE 5.2.6.3-1: APPLICABLE MIL SPECIFICATIONS FOR RELAYS

- Low current relays (up to 10 amps). Low current relays up to 10 amperes shall conform to MIL-R-5757, MIL-R-39016 or MIL-R-6106. However, relay applications requiring high in-rush current capabilities (i.e., motor and controller functions) may be in accord with MIL-R-6106, as applicable.

- High current relays. Relays used in high current applications shall conform to MIL-R-6106.

- Time delay relays. Electronic, including solid state, time delay relays shall conform to MIL-R-83726.

- Solid state telegraph relay assemblies. Solid state passive telegraph relays shall conform to MIL-R-27777.

- Established reliability relays. Established reliability relays shall conform to MIL-R-39016 or MIL-R-6106.

- Reed relays. Reed relays shall conform to MIL-R-5757 or MIL-R-83516.

- Relay sockets. When relay sockets are required, they shall conform to MIL-S-12883.

- Solid state relays. Solid state relays shall conform to MIL-R-28750. This military specification is for hermetically sealed or encapsulated solid state relays incorporating only semiconductor and passive circuit devices.

5.2.6.3.1 LOADS

o Mechanical Relays. Circuit to be switched should be designed to minimize stresses on the relay contacts. The operating life of a relay is a function of the percent of rated current which it is required to switch as shown in Figure 5.2.6.3-1.

Nonresistive load switching can seriously degrade mechanical relay reliability; therefore, the arc suppression techniques shown in Figure 5.2.6.3-2 should be used to protect the relay contacts. Arc suppression circuitry is usually mounted external to the relay package; however, some relays contain internal arc suppression circuitry.

o Solid State Relays. The same general consideration for loads, found in the mechanical relay section, holds true for solid state relays, but there are some exceptions. Pure solid state relays have no mechanical contacts; instead they have semiconductor junctions. When using nonresistive loads, surge current can create high junction temperatures resulting in degradation or failure of the relay. Hybrid relays combine mechanical and pure solid state construction. Therefore, both mechanical contacts and semiconductor function can be damaged by nonresistive loads if not properly applied.

5.2.6.3.2 ENVIRONMENT

Relay contamination or degradation can occur if the construction of the relay is not matched to its operating environment. Contamination of solid state relays is not a major problem but temperature must be closely controlled in an application in order not to exceed the semiconductor devices' rated junction temperature.

5.2.6.3.3 DERATING

Relays should be derated as a minimum in accordance with Table 5.2.6.3-2.

TABLE 5.2.6.3-2: DERATING FACTORS

PARAMETER	DERATED % OF SPECIFIED VALUE
Contact Current (Continuous)	75 - Resistive Load 40 - Inductive Load 20 - Motor 10 - Filament
Contact Current Peak In-Rush	75 - Capacitive Load
Contact Power	50
Coil Energize Voltage	90 Minimum
Coil Dropout Voltage	110 Maximum
Vibration	75 (including Q of mounting)
Temp (^{o}C) (From Max)	20

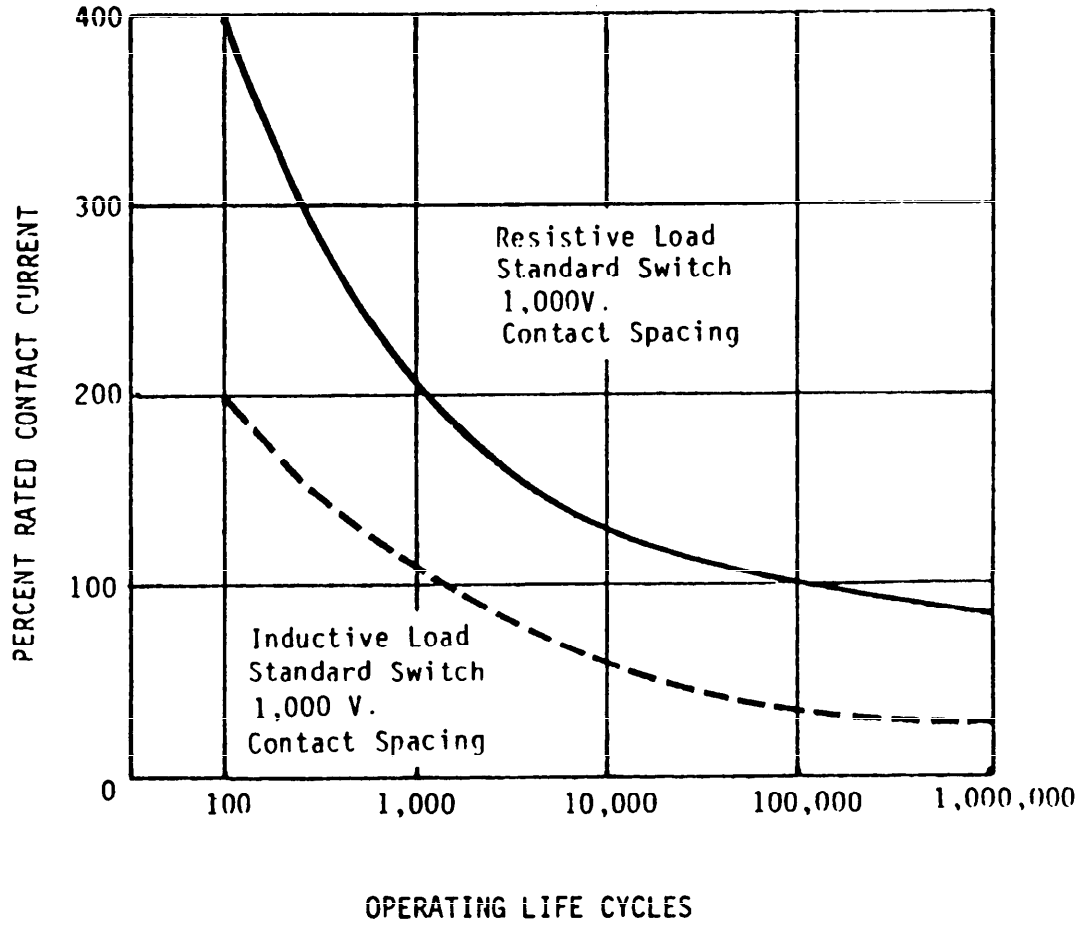


FIGURE 5.2.6.3-1: EFFECT OF CURRENT ON OPERATING LIFE (TYPICAL CHARACTERISTICS)

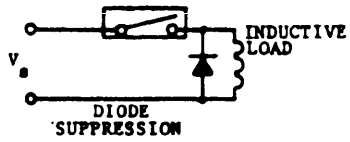
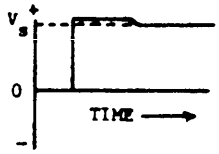
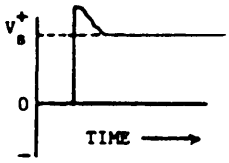
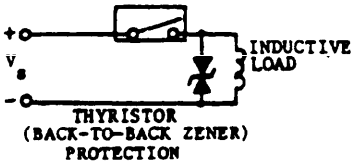
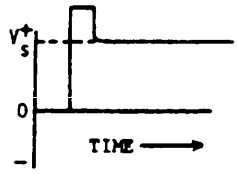
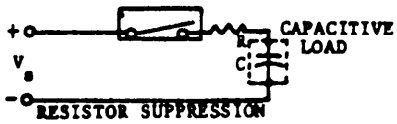
CIRCUIT	WAVEFORM	NOTES
	VOLTAGE ACROSS CONTACTS V_s = DC SOURCE 	Transient voltage is equal to forward drop of diode. Transient time is long. To adequately limit the relay dropout time using this technique clamping voltage should not be less than 1.5 x nominal coil voltage.
		Transient voltage is equal to current at opening x resistance. Transient time is short. Best tradeoff of price vs. performance.
		Transient voltage is equal to thyristor voltage. Transient time is shortest for a given maximum voltage transient.
	N/A	Maximum current transient = $\frac{V_s}{R}$

FIGURE 5.2.6.3-2: DIRECT CURRENT ARC SUPPRESSION TECHNIQUES

o Electromechanical Relay. Derating an electromechanical relay increases the reliability of the relay. For the coil, it reduces the generation of heat, resulting in slower degradation of the insulation, reduction of wire fatigue, and lessening risk of shorts. For the contacts, however, caution must be observed not to derate the contacts to the point where there is not enough current and voltage to break through the thin layer of corrosion usually found on the contacts. If an application requires very low voltage and current, dry circuit relays specifically designed for that application must be used. By derating the contacts properly, however, one can reduce the wear on the contacts caused by arcing.

o Solid State Relays. For pure solid state relays derating the load reduces junction temperatures, thus increasing the relay life. For hybrids it is again a matter of being a combination of both mechanical and pure solid state relays, and the effect of derating is as discussed above.

5.2.6.3.4 MISAPPLICATION CAUTIONS

Misapplication of relays will result in reduced reliability. The following is a list of typical relay misapplications and cautions thereto:

a. Paralleling contacts to increase capacity. Contacts will not make or break simultaneously, and one contact carries all the load under the worst conditions. Redundant contact configurations may be used when high reliability is required. Contacts should be operated in parallel for redundancy only and never to increase the current rating of the relay contacts.

b. Circuit transient surges. Circuit designers should be careful not to expect relays to handle circuit transient surges in excess of their ratings. It should be noted that surge currents greater than ten times the steady state current can result when switching inductive, capacitive and lamp loads. The circuit designer can add small values of series resistance to the circuit to reduce current surges.

c. Using relays under load conditions for which ratings have not been established. Contact ratings should be established for each type of load. Many relays will work from low level to rated load. However, relays should not be used at low level loads after having been tested or used for a short period of time at high level loads.

d. Using relays at higher voltages than those for which they were designed. For example, switching 300 volt power supplies with relays only rated 115 volts maximum.

e. Contact ratings with grounded case. Some relays employing a grounded case have small internal spacing or lack arc barriers. In such cases, derate the contact ratings more than in the ungrounded case mode of operation when switching in excess of 40 volts ac or dc. Typically, the maximum ac rating of a nominally rated 28 Vdc, 2 amp resistive relay, is of the order of 0.150 ampere. Relays with sufficent spacing or arc barriers can be used at full rating at voltages over 40 volts (ac or dc) or 115/200V, 3-

phase ac with case grounded when so rated on the detail military specification. Switching high voltage with the relay case ungrounded results in a potential personnel hazard.

f. Transferring loads between unsynchronized power supplies with inadequately rated contacts. When a load is switched, the voltages can range from being in phase to 180° out of phase; therefore, the relay contact voltage can vary from zero voltage to two times peak voltage and maximum current.

g. Switching polyphase circuits with relays tested and rated for single phase only. A typical misapplication is the use of small multipole relays (whose individual contacts are rated for 115 volts single phase ac) in 115/200 volts three phase ac applications. Phase to phase shorting at rated loads is a strong possibility in these instances, with potentially catastrophic results.

h. Using relays with no established motor ratings to switch motor loads. Caution should be used in applying relays to reverse motors, particularly where the motor can be reversed while running, commonly called "plugging." This results in a condition in which both voltage and current greatly exceed normal. Only power relays rated for "plugging" and reversing service should be utilized in these applications.

i. Using relays rated for 115 Vac only on 28 volt or higher voltage dc applications. If contacts in these devices are of the single break form A type, it may be necessary to derate severely for use on dc applications at 28 volts or higher.

j. Using relays with no established minimum current (contamination test current) capabilities. It should not be assumed that because a relay is used in an application considerably below its rated contact load that the consideration of minimum current (contamination test current) capability can be ignored; this is especially true if there is no established level of minimum current (contamination test current) for the relay.

k. Effects of ambient temperature on coil overdrive. Many users do not realize that more voltage is required to operate a relay at elevated temperatures. A coil operated relay is a current device (ampere turns). Temperature increases the coil resistance at the rate of approximately 0.004 ohm/°C due to the temperature coefficient of copper. Therefore, with a given voltage applied to a relay coil, overdrive decreases at elevated temperatures; if this is not taken into account, misapplication occurs. When rated voltage is specified, an ambient temperature is usually also specified; the user should consider the maximum ambient temperature condition and the effect upon the voltage that is supplied.

l. Relay race circuits. Relay race involves conditions where one relay must operate prior to another in separate drive circuits. Relay race circuits should be avoided; but where they must be used ambient temperature, drive power, operate and release times, coil suppression circuitry, and wear must be carefully considered.

m. A problem is encountered when a relay coil is operated from a slowly rising current. When conditions are right, the relay operates at some point during the increasing drive current. Back electromotive forces (EMFs) are produced when the armature closes to the pole face. This voltage being opposite in polarity to the driving voltage causes the relay to release and then reoperate. This condition prevails until a sufficient amount of drive current is available to overcome the back EMFs.

n. Relays rated for 400 Hz only should not be used at 60 Hz.

o. Using relays to switch inductive loads. While ac inductive circuit requirements and relay capabilities can be properly matched in terms of current, voltage, frequency, and power factor, no such positive comparison method exists for dc inductive circuits. Thus, special care should be exercised in selecting relays to switch dc inductive loads.

p. Using coil transient suppression relays where suppression is not required. Suppressing coil transients can affect load switching capability and relay life. Using maximum possible suppression may increase relay dropout time. Increased dropout time can reduce the amount of current that can be switched and the relay life. Increased dropout time can also adversely affect relay logic circuits.

q. Relays should be located and mounted to minimize the probability of contact chatter due to shock and vibration. The shock from pyrotechnic sources is a significant problem to relays; this can be avoided by the use of solid state relays.

r. Contacts should never be operated in series to "increase voltage rating."

s. Relays which are not designed specifically for load transfer applications should not be used for that purpose.

t. Devices designed specifically for dry circuit applications must always be tested under dry circuit conditions, as they are extremely sensitive to damage due to excessive power.

u. If isolation is a definite requirement but the use of solid state relay is required the hybrid solid state relay will do the job. Pure solid state relays are not totally isolated and can trigger due to circuit transients.

v. Using relays at their rated shock and/or vibration levels with lower than rated coil input. The coil provides the force (via the relay motor circuit) to keep the contacts closed during these environments. At less than rated voltage (or current), this force may be decreased significantly. The results will be excessive chatter of the contacts due to the acceleration forces placed on them.

w. Using a coil energization voltage (or current) below rated value. Using a coil energization voltage (or current) below the rated value may seriously compromise the number of operating cycles of life for a given relay. The life characteristic of a relay is stated for rated energization voltage (or current). Reducing this value significantly will increase the operating time of the unit as well as its arcing time and thereby degrade its capability to meet the required number of cycles.

REFERENCES

1. Anon., Electronic Engineering Times
June 8, 1981
Solid State Relays

2. Anon., Engineer's Relay Handbook (NARM)
Third Edition
Copyright 1980

3. Anon., Machine Design
May 19, 1977

5.2.7 SWITCHES

5.2.7.1 INTRODUCTION

The term "switches" is applied to a wide variety of electromechanical devices whose function is to make or break an electrical circuit. Switches are available in many different configurations, sizes, mechanical and electrical characteristics, and costs. Switches can be grouped into three general types: rotary, nonrotary and sensing. A discussion of the general characteristics of these types is presented below:

o Rotary Switches. These switches are actuated by the rotary motion of a shaft for the selection of any one or more of a number of circuits. Many types of switching arrangements are available for use in varying one or more functions such as voltage, frequency and/or resistance. They are available in open, closed or sealed construction and may be used in AC or DC applications.

o Push Switch. These switches are actuated by a reciprocating plunger and are available as low energy devices or as devices carrying large current loads. The range of complexity may vary from a simple unlighted "SPST" device to a very complex lighted screen matrix containing various circuitry for use in panel displays. All types are available for AC or DC applications.

o Toggle Switches. These switches are actuated by a bat handle and are available as low energy devices or as switches carrying large current loads. Many types of toggle switches are available (each is available in either AC or DC):

a) Single, double, triple, and four pole
b) Single, or double, or triple throw
c) Unsealed, watertight, or hermetic
d) Maintained or momentary action
e) Locking or nonlocking bat handles

o Thermostatic Switches. These switches are actuated by temperature change. They are available in two types of constructions: (1) bimetallic element actuated, used for most AC or DC circuit applications; (2) nonbimetallic element actuated, used for most pneumatic applications. Thermostatic switches are used for temperature protection, accurate temperature control, and as detection devices.

o Pressure Switches. These switches are actuated by pressure changes in liquid or gas applications. The switch mechanism consists of an electrical snap switch actuated through the displacement of a pressure sensing device having an inherent spring rate such that its displacement is proportional to the applied pressure. The pressure sensing devices are of several general types:

a) Piston
b) Bourdon tube
c) Bellows elements
d) Disc spring

5.2.7.2 SELECTION OF SWITCHES

Standard switches are described in MIL-STD-1132. To properly and effectively select switches and their associated hardware, the equipment designer should know the advantages and disadvantages of different types of switches, for example, their behavior under various environmental conditions, switch construction, the effect of the switch upon the circuit, and the effect of the circuit upon the switch. The designer should consider the following characteristics and parameters in determining the most suitable switch design and mounting hardware.

- Application (type of switch)
- Flexibility of circuitry
- Type of action
- Electrical data (contact ratings, etc.)
- Type of contacts
- Environmental capabilities such as shock and vibration
- Mechanical data and safety features
- Quality and reliability

The selection of a specific switch is governed by the criteria depicted in Table 5.2.7.2-1.

TABLE 5.2.7.2-1: SELECTION CRITERIA FOR SWITCHES

1. MIL-STD-1132, "Switches and Associated Hardware, Selection and Use of."

2. Requirements 58 of MIL-STD-454, "Standard General Requirements for Electronic Equipment." MIL-STD-454, Requirement 58 requires that:

   a) Switches and associated hardware shall be selected from MIL-STD-1132 and shall conform to the applicable specifications listed therein.

   b) Switches other than those listed in MIL-STD-1132 shall conform to one of the following specifications:

      MIL-S-12285, Switch, Thermostatic
      MIL-S-15743 Switches, Rotary, Enclosed
      MIL-S-18396, Switches, Meter and Control, Naval Shipyard
      MIL-S-21604, Switches, Rotary, Multipole and Selector Type

3. Historical test data (from similar applications) or other engineering information and/or data that provides assurance that the device is sufficiently rugged and reliable for the application (e.g., previous use in military equipment, comparable application or GFE).

5.2.7.2.1 USAGE

Switch usage and selection guidelines are given in Table 5.2.7.2-2.

TABLE 5.2.7.2-2: USAGE AND SELECTION GUIDELINES FOR SWITCHES

Military Specifications	Type	Styles	Usage Notes	Failure Modes
MIL-S-3786	Rotary Switches	Low Current Capacity	Used primarily for low-power, alternating current (ac) or direct current (dc) switching applications (capable of making and breaking a resistive load of 2 amperes or less). Includes both manually and solenoid actuated switches.	Switches, like relays, are electromechanical devices subject to both electrical and mechanical failure. Some causes of failure are poor contact alignment, deformed, loose, broken, open, contaminated, or pitted contacts, binding of moving parts, poor terminal plating, and loss of resiliency in springs and open coils. Contact failure can result from high inrush or sustained high currents or from the inductive kick when an inductive circuit is opened. High inrush currents occur in loads composed of motors, lamps, heaters, capacitive input filters, or other devices that have low starting resistance compared to operating resistance. These currents may cause intense heat and the possible welding of contacts. Careful consideration should be given to derating in these cases. In selecting a switch for high reliability programs, hermetically sealed units should be used where available. This is particularly true for space programs. These should be sealed by welding, since solder is a source of contamination. Terminals should have a glass seal and be of a solder hook design to provide proper stress relief for the seal. Parts should be of corrosion resistant material with no cadmium or zinc plating. Use of non-metallic materials should be minimized.
MIL-S-6807	Rotary Switches	Selector, Power	Used in power circuits capable of making, carrying, and breaking electrical loads of 10 amperes or less.	
MIL-S-15291		Snap Action	Used in high current circuitry capable of making and breaking 10-200 amperes, 120-250 volts dc, 125-500 volts ac, utilizing snap action positioning mechanism.	
MIL-S-22710		Printed Circuit, Thumbwheel, Inline, and Pushbutton	Used primarily for low power ac or dc switching applications. Thumbwheel switches provide a numerical or other legend readout tied to a particular switch position.	
MIL-S-3950	Toggle Switches	Environmentally sealed	Used where simple make-and-break actions are required in both ac and dc circuits. Not for use in circuits with ratings lower than switch intermediate current.	
MIL-S-8834		Positive break	Used in ac and dc circuits where a positive make-and-break action is required. Positive break actuation causes minimum contact "tease."	
MIL-S-9395	Pressure Switches	Creep and Snap Action	Used primarily to detect changes in pressure; liquid and gas applications. Switches may respond to absolute gauge or differential pressures.	
MIL-S-8805	Push Switches (Snap action)	Sensitive	Use in both ac and dc applications when predetermined; small and accurately controlled characteristics are required. Various means of actuation (i.e., toggle levers, push buttons, cams and other light pressure devices). Use sealed units wherever possible.	

TABLE 5.2.7.2-2: USAGE AND SELECTION GUIDELINES FOR SWITCHES (Cont'd)

Military Specifications	Type	Styles	Usage Notes	Failure Modes
MIL-S-22885	Push-button Switches	Illuminated	Used as panel displays and switching devices in ac and dc applications. Panel displays include various combinations of colors and legends.	See comments on preceding page.
MIL-S-24317		Multistation (Illuminated and non-illuminated)	Used as panel displays and switching device in ac and dc applications.	
MIL-S-24236	Thermostatic Switches	Metallic and Bimetallic	Used primarily in ac and dc applications where temperature protection or accurate temperature control of an enclosure is required.	
MIL-S-28827		Volatile Liquid, Hermetically Sealed	Used primarily in ac and dc applications that require rapid temperature response.	
MIL-S-55433	Reed Switches	Dry Reed	Used in circuits as a separate elements where magnetically-actuated, hermetically sealed switch contacts are required. These reed switches are capable of millions of operations and operations with low-level (dry circuit) loads. For use in communications, electrical and electronic equipment.	
MIL-S-5423	Boots	Dust and water seal	Used on toggle, push-button and rotary switches to protect the switch-actuating mechanism from sand, dust, water, and other contaminants, and to seal the panel on which the switches are mounted.	
MIL-S-83504	Dip Switch	Sealed	A miniture high density for mounting on PCB	
MIL-S-83731	Toggle Switch	Sealed Unsealed	Use where make-and-break action are required in both AC and DC curcuits	

5.2.7.3 APPLICATION CONSIDERATIONS

Application considerations in the selection of switches include the following:

5.2.7.3.1 ENCLOSURES

Many types of enclosures are used to protect switches from varying external conditions, particularly high humidity and dirt. Accordingly, switches may be classified based on the degree of protection offered by the enclosure. Such classifications include the following: open, watertight, dust tight, dripproof, enclosed, environmentally (resilient) and hermetically sealed. With the open construction switch, no effort is made to protect the switch or its parts from atmospheric conditions. The enclosed switch is one in which the contacts are enclosed in a case made of plastic or metal and plastic. The environmentally (resilient) sealed switch contains a completely sealed case where any portion of the seal is a resilient material such as a gasket or a seal. The hermetically sealed switch is made airtight by a sealing process which involves fusing or soldering and does not use gaskets. The hermetically sealed enclosure offers the greatest protection because it insulates against such elements as moisture, harmful gases, and dirt. It also eliminates the increased arcing caused by low atmospheric pressures at high altitudes.

5.2.7.3.2 CONTACTS

The switch electrical contacts can be classified by function, current carrying capacity, and application. The contact arrangements vary in complexity from a simple make-or-break, through make-before-break, break-before-make, make-make, break-break, etc.; from a single throw to multiple throw, single pole to multipole; and various combinations of these features.

o Contact Ratings. Contacts are usually given multiple ratings depending on the type of load being switched. These ratings consist of resistive, low level (dry circuit), lamp, motor, or inductive loads. Most switches are given the resistive load rating and in most instances at least one additional of the above ratings.

o Contact Operate and Bounce Times. In many instances, bounce times of the contact are important. Operate time in a double throw switch is defined as the time it takes the moving contact to separate from the normally closed contact, travel to the normally open contact and make the circuit (this does not include bounce time). Bounce time is the interval between first make of the contact until the uncontrolled making and breaking of the contact ceases. In many electronic circuits, a millisecond is a long time, making operate and bounce times critical parameters.

o Contact Resistance. Contact resistance is the resistance between two mating closed electrical contacts measured at their external terminals. Contact resistance includes the resistance of the contact material, oxide or other film on the surface of the contacts, and the resistance of the elements on which the contacts are mounted (e.g., springs, mounting, and the external terminals and their connections).

in other capacitors, such as mica, plastic, ceramic and glass

o Contact Life - The relationship between contact life and load characteristics is shown in Figure 5.2.7.3-1. It should be understood that contact life may not be the limiting factor in total life of the switch. Spring life or other mechanical factors must be considered.

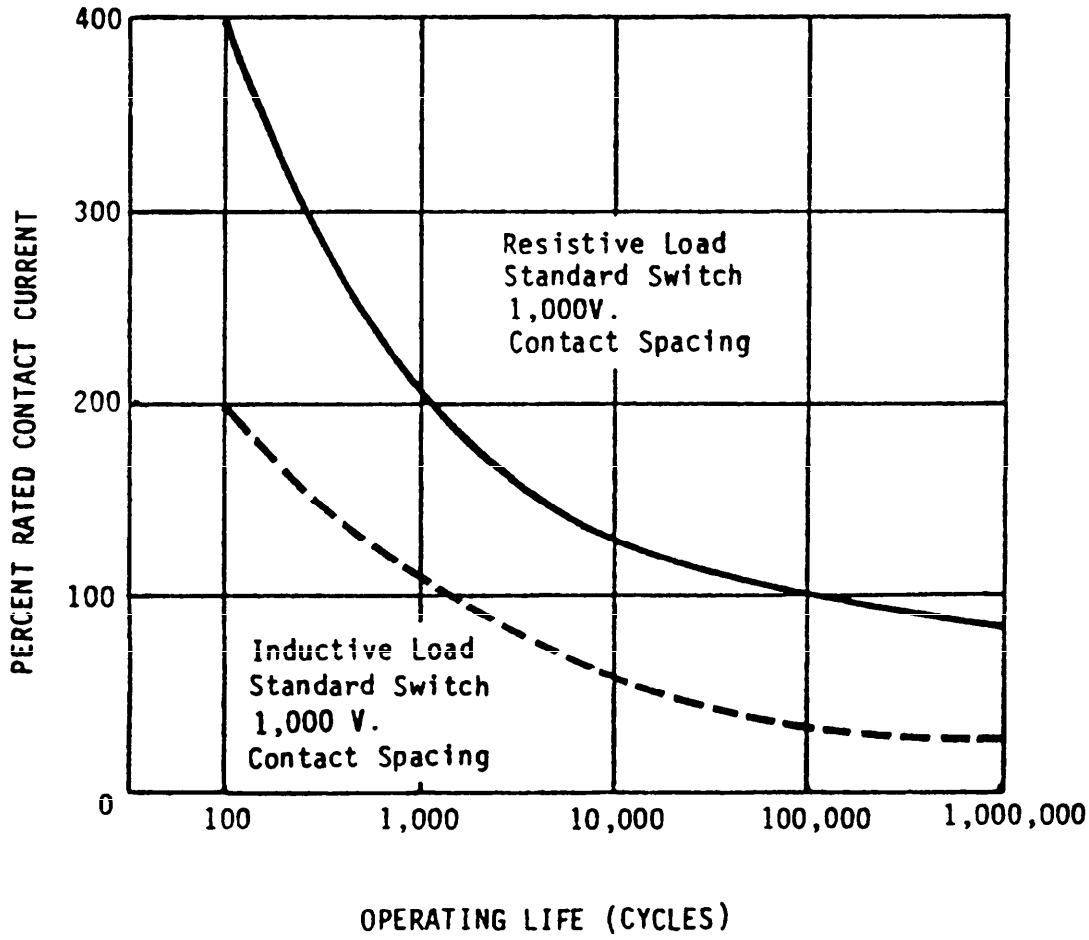


FIGURE 5.2.7.3-1: EFFECT OF CURRENT ON OPERATING LIFE (TYPICAL CHARACTERISTIC)

5.2.7.3.3 LOW LEVEL (DRY CIRCUIT) APPLICATIONS

Dry circuit applications require switch contact resistance ratings based on testing, using an open circuit voltage of 30 millivolts maximum and a test current of 10 milliamperes maximum (e.g., Method 311 of MIL-STD-202). In order to achieve low level load capability,contact materials such as gold, platinum, pallidium (or their alloys) are used to minimize formation of insulating films on the contacts. Switch contacts are designed so that they wipe across each other to remove such films. Other considerations are: to provide internal designs which do not allow rubbing of insulated parts against metal that generates dust particles internally; and to adequately seal the switch contacts from external dust and foreign matter, since foreign particles being deposited on the switch contacts increases contact resistance. Proper test and performance requirements before and after life tests should be the basis for selection of these switches.

5.2.7.3.4 INSULATION RESISTANCE

Insulation resistance is important in high impedance circuits. Low insulation resistance in a high voltage circuit can result in excessive dissipation within the dielectric leading to failure. For application where arc over is a problem, switches should be selected which have a high insulation resistance (1,000 megohms or more and 5 megohms or more as measured immediately after the moisture resistance test). Properly rated insulating materials will not form a conducting surface film buildup after repeated arcs on making and breaking of contacts.

5.2.7.3.5 LIFE OPERATIONS FOR TOTAL LIFE

A careful analysis of the required life of the switch or total number of operations should be made. In some equipment applications, the operational life of the switch can be comparatively short.

5.2.7.4 ENVIRONMENTAL CONSIDERATIONS

o Temperature

(a) Variations in temperature should be considered, as moisture condensation within the switch could develop. In choosing a switch for a wide range of temperatures, the entire temperature range must be considered rather than only one extreme.

(b) Exposure to low temperature may cause certain materials of a switch to contract, causing case cracking or opening. Such failure could result in moisture or other foreign matter entering the switch and causing short circuit, voltage breakdown or corona.

(c) Chemical action of switch materials are accelerated by high temperatures. Insulation resistance between the switch and ground decreases as the temperature increases. High temperature can also affect the insulation from the standpoint of voltage breakdown due to a change in dielectric strength. Also, the increased speed of corrosion of contacts and switching mechanism is affected by high temperature.

o Moisture. Moisture in the dielectric will decrease the dielectric strength, life, and insulation resistance and could cause corrosion by increasing the galvanic action between dissimilar metals in the switch. In general, switches which operate in high humidities should be hermetically sealed, or, if this is not practical, the use of boots, "O" rings, or diaphragms placed over switch openings is recommended to inhibit moisture entry.

o Altitude. With a decrease of atmospheric pressure, the spacings required to prevent flashover increase substantially. Small switches, because of their very close contact spacings, are particularly susceptible to malfunction at high altitudes. Contact life decreases substantially with continued arc over. To compensate for increased arcing at high altitudes, users should derate the voltage and current rating given by the malfunction.

o Shock and Vibration. Switches should be selected that will operate under expected shock and vibration conditions. Those with contact chatter requirements will cover low frequency vibration and shock applications. High frequency vibration will determine the effects of fatigue and resonance of the mechanical construction of the switch contact elements. Contact bounce due to shock or vibration causes arcing, which shortens contact life and could generate electrical noise.

o Acceleration. Some switches are sensitive to acceleration forces arising from use in high speed vehicles or aircraft. Failures are usually due to internal construction which allows normally closed contacts to open and normally open contacts to close under acceleration.

o Sand and Dust. A combination of dust and small amounts of moisture will increase the possibility of voltage breakdown of the insulation between closely spaced terminals. Where low insulation resistance or high leakage currents can cause circuit malfunction, the switch should be capable of passing sand and dust test requirements.

o Explosion. Explosion resistance requires that switches operate in a volatile atmosphere without causing explosion. Whenever possible, switches to be used in an explosive atmosphere should be sealed.

5.2.7.4.1 PRECAUTIONS

(a) Switch contacts should be operated in parallel for redundancy only and never to "increase the current rating."

(b) Switch applications in digital circuits must be carefully reviewed to assure that contact bounce or chatter will not be interpreted as a circuit interruption which will produce logic errors.

(c) Switches are subject to contact chatter in high shock and vibration environments, and these environments may dictate the use of solid state devices. The mounting of switches should be designed to minimize vibration and shock amplification or to provide necessary isolation.

5.2.7.5 DERATING

Derating requirements: Switches should be derated as a minimum in accordance with Table 5.2.7.5-1.

TABLE 5.2.7.5-1: DERATING

Parameter	Derate to % of Specified Value
Contact Current (Continuous)*	75 - Resistive Load 40 - Inductive Load 20 - Motor 10 - Filament
Contact Current (In-Rush)	75 - Capacitive Load
Voltage*	50
Contact Power	50
*Affects MIL-HDBK-217 failure rate.	

5.2.8 ELECTRICAL CONNECTORS

5.2.8.1 INTRODUCTION

Connectors come in a wide variety of shapes, sizes, densities, support hardware, electrical and mechanical characteristics, and environment withstanding properties. The proper determination by the user of which of the numerous connector types and associated hardware is most suitable for his application is one of the most important contributions to equipment reliability that the designer can make.

5.2.8.2 SELECTION OF CONNECTORS

Preferred connectors are specified in MIL-STD-1353. The basic criteria for the selection of connectors for use in military equipment is given in Table 5.2.8.2-1, and usage and selection guidelines coupled with failure mode information is presented in Table 5.2.8.2-2.

TABLE 5.2.8.2-1: CONNECTOR SELECTION CRITERIA

1. MIL-STD-1353, "Selection and Use of Electrical Connectors."
2. Approved style of Military Specification.
3. MIL-STD-454, "Standard General Requirements for Electronic Equipment," Requirement No. 10.
4. MIL-P-11268(EL), "Parts, Materials and Processes Used in Electronic Equipment."
5. Historical test data (from similar applications) or other engineering information and/or data that provides assurance that the device is sufficiently rugged and reliable for the application (e.g., previous use in military equipment, comparable application or GFE).

TABLE 5.2.8.2-2: SELECTION AND USAGE GUIDE FOR CONNECTORS

Military Specification	Type	Style	Usage Notes	Failure Modes
Connectors, Cylindrical, General Data				
MIL-C-5015	"AN"	MS3100's	These connectors have threaded couplings and the soldered contacts range in size from 0 to 16. The allowable temperature range is -65°C to +85°C. Not for use by Navy or Air Force. Used in Army for ground equipment applications only and limited to environmentally protected environments.	There are four basic failure modes common to all types of electrical connectors: (a) Temperature deterioration of insert material. The probability of failure due to temperature deterioration of insert material is a function of the ability of the material to withstand the internal operating temperature of the connector. Glass and ceramic have the highest resistance to damage by heat with the capability in the range of 200°C to 250°C, dependent upon the type of filler. Silicone rubber, teflon and Kel-F all have 250°C capability. Neoprene and polychloroprene should not be used in applications where the internal operating temperature exceeds 125°C. The internal operating temperature is a function of the number of active contacts; the total current passing through the active contacts; the contact resistance, density and geometry; and the amount of conduction cooling available to the connector. (b) Moisture. Moisture failures are due to inadequate sealing of the internal structure of the connector when operating in unprotected and uncontrolled environments. Adequate resistance to high moisture environment requires the use of interfacial seals, peripheral seals on the mating surfaces of the shells, and compression grommets which seal individual wires at the rear of the connector. (c) Damage for probes, misalignment and mismating. The use of the five key polarization or nonsymmetrical shell for proper alignment during the mating operation precludes significant damage during the coupling operation. Closed entry socket contacts or hard dielectric inserts with chamfered entries for housing socket contacts prevents damage from bent pins and test probes. Removable crimp contacts are inherently more damage resistant
		MS3400's	Front release crimp contacts sized from 0 to 16. The temperature range is from -65°C to +200°C. They have threaded couplings and a hi-impact shock shell. Used for Naval shipboard jacketed cable applications only. Not for use in Army or Air Force.	
		MS3450's	Has rear release crimp contacts with sizes ranging from 0 to 16. Army applications are limited to environmentally protected ground equipment with no restrictions on other type equipment. Class W and K are not for use on Naval shipboard jacketed cable applications. For use in the Air Force only when 0, 4 and 8 size contacts are required.	
MIL-C-26482	Environment resisting, quick disconnect, miniature, circular electric connectors	MS3110's (Series I)	Each series contains hermetic receptables. When the two series are intermated they meet the performance requirements of series 1 connectors. The contacts are soldered and the coupling is bayonet. The contact sizes are 16 and 20. The allowable temperature is -55°C to +125°C. Not for use by Navy or Air Force. Used by the Army for ground equipment applications only. For use where water pressurization is a requirement.	
MIL-C-38999	Miniature, high density, quick disconnect, circular, environment resistant, bayonet coupling, electrical connectors	Series I	Capable of continuous operation within a temperature range of -65°C to +200°C. Rear release crimp contacts (hermetic contacts are soldered) sizes 12, 16, 20 and 22. For Army use limited to environmentally protected applications on ground equipment. Not for use in Naval shipboard jacketed cable applications. No restrictions on Air Force applications.	
MIL-C-3899	Same as above	Series II	Same as above except: Not for use by Army or Navy, no restrictions on Air Force use.	

TABLE 5.2.8.2-2: SELECTION AND USAGE GUIDE FOR CONNECTORS (Cont'd)

Military Specification	Type	Style	Usage Notes	Failure Modes
Connectors, Cylindrical, General Data				
MIL-C-83723	Environment resisting, circular, electrical connectors	Series III	These connectors have crimp or solder (Class H only) contacts and are capable of operation within temperature range of -65°C to +200°C. The coupling is threaded and bayonet. Not for use by Navy or in Army ground applications. No restrictions on Air Force use.	due to the high strength termination and, in turn, are less likely to cause damage to other parts of the connector during the fabrication process. (d) Vibration. Connectors operating under conditions of high vibration must have positive screw type coupling mechanisms and adequate support for the cable or wire bundle.
Connectors, Cylindrical, Heavy Duty				
MIL-C-22992	Nonremoval solder contacts	Class C	These connectors are intended for rough service applications; for external electrical interconnection of equipments such as shelters, vans, buildings, missile/space launch sites. Their rated operating temperature range is from -55°C to +125°C.	
		Class R	Same as above except intended use is in protected enclosures where waterproofing (unmated) or pressurization is not required.	
	Front release - rear removable crimp or solder contacts	Class L	These connectors are intended for use in power connections with a current range of 60 to 200 amperes. Used only with the heavy duty jacketed cables specified on the applicable insert standard. Reference MIL-STD-255.	
Connectors, Rack and Panel				
MIL-C-24308	Miniature rectangular connectors	Class G	The contacts are crimp or solder and sizes 20 or 22D. The intended use of these connectors is in nonenvironment-resisting applications where an operating temperature of -55°C to +125°C is experienced.	
		Class N	Same as above except the intended use is in applications where the presence of residual magnetism must be held to very low levels to avoid interference with sensitive instrumentation.	
		Class H	These connectors have solder contacts, size 20. Intended for use in applications wherein atmospheric pressures must be contained by the connectors across the wall or panels on which they are mounted.	

TABLE 5.2.8.2-2: SELECTION AND USAGE GUIDE FOR CONNECTORS (Cont'd)

Military Specification	Type	Style	Usage Notes	Failure Modes
Connectors, Rack and Panel				
MIL-C-28731	Rectangular electrical connectors		Intended for use in electrical and electronic equipment. The type of contact and coupling varies for each specific connector. The contact wire size ranges from 18-26 AWG.	See comments on preceding page.
MIL-C-28748	Standard rectangular connectors		These connectors have size 16 front release crimp contacts. These connectors are for nonenvironmental applications only.	
MIL-C-28804	High density, polarized center jackscrew environment resisting connectors		The intended use of these connectors is for electronic and electrical equipment where residual magnetism must be held to a minimum. They have size 22 rear release crimp removable contacts. The above applies for both Class G and Class E connectors.	
		Class G	Class G connectors are intended for use in nonenvironmental resisting applications where the operating temperature range of -55°C to +125°C is experienced.	
		Class E	Class E connectors are intended for use in environmental resisting applications. Provisions are made for sealing around wire at rear of connectors.	
MIL-C-81659	Rectangular connectors	Series 2	These connectors are environment resisting with one to four inserts per connector. They have rear release removable crimp contacts. Not for use in the Air Force.	
MIL-C-83733	Miniature rectangular connectors		These environmental resisting connectors are designed to operate up to temperatures of 200°C. All the types and classes are intermatable under the same shellsize. They have rear release crimp removable contacts.	
Connectors, Test Point				
MIL-C-39024	Test point, panel or printed wiring electrical connectors		These test points and test jacks have either single or multiple contacts for use on chassis, panels and printed wiring test applications.	

TABLE 5.2.8.2-2: SELECTION AND USAGE GUIDE FOR CONNECTORS (Cont'd)

Military Specification	Type	Style	Usage Notes	Failure Modes
Connectors, Radio Frequency, Coaxial				
MIL-C-39012	Flexible radio frequency cable and coaxial transmission line connectors	Series N	These connectors are for use up to a maximum voltage of 1000 RMS at sea level. They have a threaded coupling for RF cable in the .195 to .870 inch outside dimension (OD) range.	See comments on preceding page.
		Series SC	Same as above	
		Series C	The maximum operating voltage is 500 RMS at sea level. They utilize bayonet couplings for RF cable in the .280 to .870 inch OD range.	
		Series BNC	Same as above except the OD ranges from .160 to .250 and is not for use by Navy or Air Force.	
		Series TNC	These connectors utilize threaded couplings for RF cables in the .100 to .250 inch OD range. The maximum operating voltage is 500 RMS at sea level.	
		Series SMA	Same as above except OD ranges from .071 to .170 inch and maximum voltage is 170 RMS at sea level.	
		Series SMC	Same as above except OD ranges from .071 to .100 inch and the maximum voltage is 250 RMS at sea level.	
		Series SMB	The maximum operating voltage is 250 RMS at sea level. These connectors utilize bayonet couplings for RF cable in the .071 to .170 inch OD range.	
MIL-C-3655	Plug and receptable, electrical (coaxial, series twin) connectors		Standard electrical connectors designed for use with radio frequency cable. Class I are weatherproof and Class II are non-weatherproof.	
Connectors, Printed Wiring Board				
MIL-C-21097	General purpose printed wiring board connector		These connectors are for direct insertion of 1/16 inch printed circuit boards with either double or single side circuitry. Recommended for applications with a minimum of susceptibility to vibration.	

TABLE 5.2.8.2-2: SELECTION AND USAGE GUIDE FOR CONNECTORS (Cont'd)

Military Specification	Type	Style	Usage Notes	Failure Modes
Connectors, Printed Wiring Board				
MIL-C-55302	Printed circuit sub-assembly board connectors		All characteristics are applicable and no restrictions apply.	See comments on preceding page.
Connectors, Power, General Duty				
WC-596	Plug, receptables and cable outlet, electrical power connectors		Connectors are of a grounding type non-armoured, dead-front construction. All connectors are to be used with copper or copperclad aluminum wire only. They have a service voltage between 120 and 600 volts, a current rating up to 60 amperes, and a frequency rating of 60Hz. Special connectors for 400Hz and dc applications are taken into account. Not to be used in hazardous locations.	
Sockets, Plug-In				
MIL-S-83502	Round, TO, plug-in electronic component sockets		These sockets are for use on panel boards, printed circuit boards and microelectronic components.	
MIL-S-83505	Individual lead sockets		These sockets are for insertion through mounting boards or panels.	
MIL-S-83734	Plug-in electronic component sockets Dip Configurations		These sockets are for use on panel boards, printed circuit boards, and microelectronic components.	

In addition, when selecting the proper connector, the following electrical, mechanical and environmental considerations should be taken into account:

5.2.8.2.1 ELECTRICAL

o Voltage and current requirements - low current and low voltage situations, for example, require a plating that will not oxidize because the current may not be able to penetrate an oxide coating.

o Resistance - becomes a critical factor if the connectors are in series and the impedances involved are low.

o Maximum current - determined by the connector and the size of the wires attached to it.

o Maximum voltage - depends on the spacing between contacts and insulating material used.

o Intercontact capacitance - becomes very important when high frequencies are involved.

o Other key electrical parameters include surge current, characteristic impedance, insertion loss, and EMI leakage attenuation.

5.2.8.2.2 MECHANICAL

o The space available for the connectors.

o The number of necessary spare contacts.

o The type of termination required (i.e., crimp or solder).

o The type of connector required: environmental, nonenvironmental, threaded, bayonet, or push-pull.

o Size of contacts (determined by the operating voltages and currents.)

o The type of wire characteristics required: that is, whether contacts for shielded wire are required; whether RFI protection is required; and also the wire material's construction and diameter.

o If crimped removable contacts are used, the direction of removal (i.e., front release rear removable or rear release rear removable).

o The type of receptacle to be employed (i.e., square flange mount or single hole mount).

o The type of support hardware (clamps, caps, etc.) required and mounting provisions to be made.

5.2.8.2.3 ENVIRONMENTAL

o Mechanical Effects. Achieving good electrical contact in a connector is a function of contact surface films (oxides and sulphides), surface roughness, contact area, plastic deformation of the contacting materials and load applied. Since even the best machined, polished and coated surfaces look rough and uneven when viewed microscopically, the common concept of a flat, smooth contact is grossly oversimplified. In reality, the connector interface is basically an insulating barrier with a few widely scattered points of microscopic contact. The performance of the connector is dependent upon the chemical, thermal and mechanical behavior at these contact points.

o Electrical Effects. Current flow between mating metals is constricted at the interface to the small points on the contact surfaces which are in electrical contact. This flow pattern causes differences of potential to exist along the contact interface and causes current bunching at points of lower resistance. As a result, contact resistance and capacitance are introduced into the circuit, and certain chemical effects evolve (see chemical effects).

o Thermal Effects. Since the total contact resistance in a good connector may be small (micro-ohms) and is achieved by the paralleling along the interface of many higher resistance point conducting paths, a series of localized hot spots can develop. When high currents are conducted through multiple pins, the cumulative heat rise in the connector can be appreciable.

o High Temperature Effects. Excessive temperature can cause failure of connectors by breakdown of insulation or by breakdown in the conductivity of the conductors. Either malfunction can be partial or complete. A typical breakdown caused by excessive temperature occurs progressively. As operating temperature increases, insulation tends to become more conductive, and, simultaneously, the resistance of conductors increases. Higher resistance causes the temperature of the conductor and of its insulation to rise further. This pyramiding effect can raise conductors and connector contacts beyond maximum conductor operating temperatures, with resultant damage to contacts and conductive platings. Complete failure will occur if the operating temperature reaches the point where the conductor melts, breaking electrical conductivity, or where the insulation fails, causing a short.

Maximum operating temperatures are the sum of ambient temperature and conductor temperature rise caused by the passage of current. For example, maximum conductor operating temperature of 125°C is based on an ambient temperature of 100°C, plus a rise of 25°C, due to the conductor carrying current. A graph of service life vs. hot spot temperature is given in Figure 5.2.8.2-1.

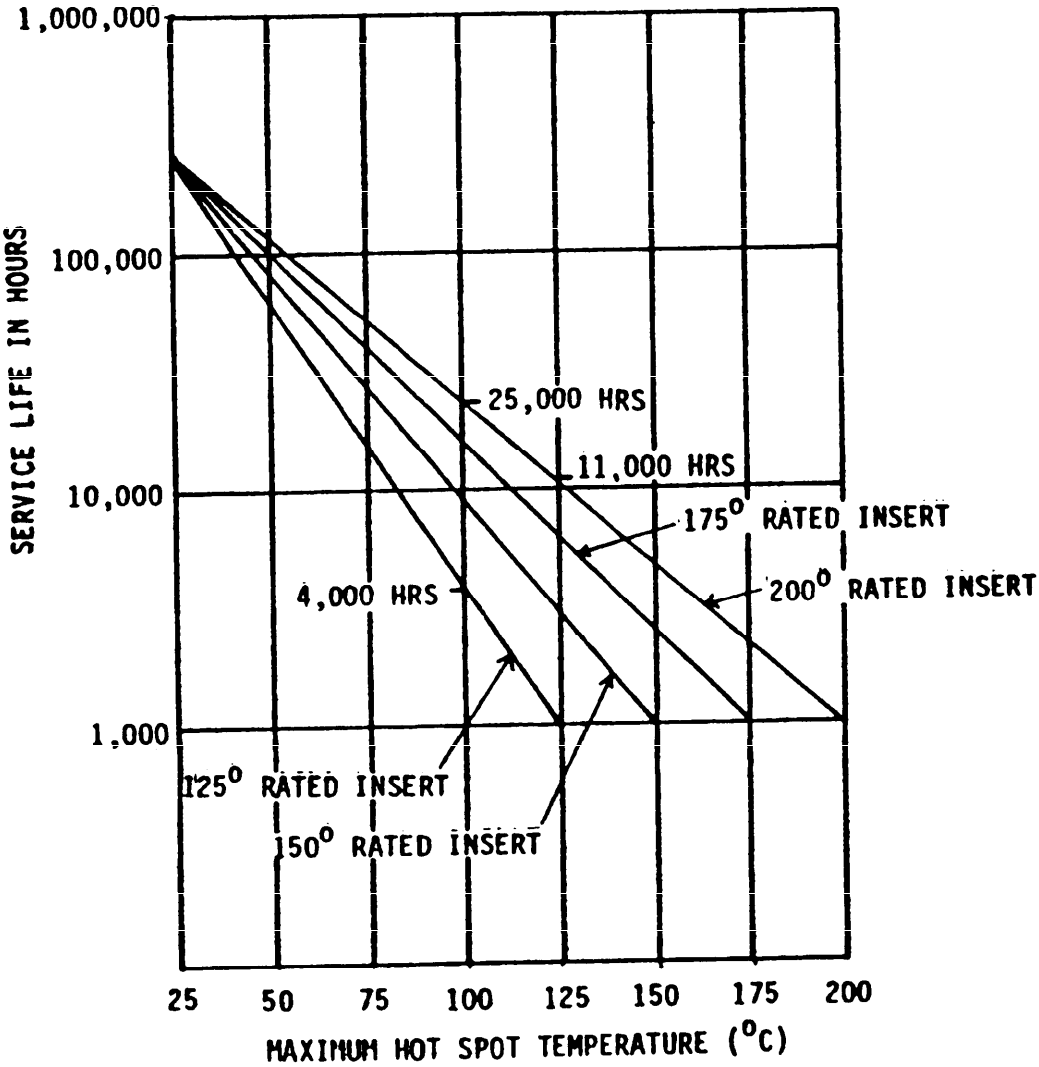


FIGURE 5.2.8.2-1: SERVICE LIFE VS. HOTSPOT TEMPERATURE

o Low Temperature Effects. Metals and nonmetals tend to become brittle and shrink at different rates. How important each characteristic is depends on the application. Most high performance connectors will operate down to -55°C. Operation at lower temperatures may require special materials.

Ambient temperatures below "normal" are not usually the cause of trouble in interconnection systems, so far as conductivity is concerned. (The lower the temperature, the more current can be carried by a given conductor.) However, extremely low ambient temperatures do produce mechanical failures, mostly occurring in the nonmetallic portions of connectors, wires and cables. The coefficient of expansion of most plastics and elastomers are so different from those of the metals used in structural members that they will shrink enough at extremely low temperatures to open seals. An open seal may not cause a malfunction unless moisture and contaminants enter through the opening. If a seal opens after the temperature of a connector falls below the freezing point of the contaminants present and then seals itself before the melting point of the contaminants is reached, foreign matter will never enter. However, if a connector seal opens at a temperature where liquid or gaseous contaminants have not been frozen, they can enter and contaminate the connector.

o Chemical Effects. Most contact failures of connectors are induced by the growth of films at points of contact. These films can cause increased contact resistance or open circuit. (Contact resistance gives rise, as explained above, to interfaces at higher temperatures than the surroundings, thus increasing the chemical activity). Ions in impurities or contamination in the surface pores of contacts will migrate to the points of highest potential, which are frequently the localized hot spots. Ions interfacing with electrons and other constituents at the points of high chemical activity usually generate nonconducting films. There is also a continuous supply of material for the growth of insulating films from environments where there are corrosive elements such as hydrogen sulfide, water vapor, oxygen, ozone, hydrocarbons and various dusts.

o Cycling Effects. The connector plugged to its mate during much of its operational life is characterized by a typical catastrophic failure rate based on the factors described. Many connectors, particularly of the cable type that are repeatedly plugged and unplugged, continuously expose the contacts to a fresh supply of local corrosive contaminants. These cycling effects also create the problem of physical wear on the connecting interfaces. Surface contact points become worn making unsymmetrical contacts and sometimes substituting nonconducting films to replace conducting points in the physical interface. The result is increased interface resistance, higher contact temperature and degradation of the connection. Hence, there is an added failure rate relation between cycling rate of connector contacts (see Figure 5.2.8.2-1).

o Operation in Parallel. When pins are connected in parallel at the connector to increase the current capacity, allow for at least a 25% surplus of pins over that required to meet the 50% derating for each pin, assuming equal current in each, since the currents will not divide equally due to differences in contact resistance. For example, it would take five pins, each rated at one amp, to conduct two amps.

o Protective Measures. During shipment, storage and operation, all unmated connectors should be kept covered with moisture proof or vapor proof caps. Protective caps specified by military specifications or military standards and designed for mating with specific connectors should be used. Where such protective caps are not available, disposable plastic or metallic caps designed for this purpose should be used.

o Potting. When potting is used for environmental protection, extreme care should be given to selection of materials and processes. Potting should not deteriorate in either chemical, physical, or electrical properties under the specified equipment environment.

5.2.8.3 DERATING REQUIREMENTS

o Pin current. Pin current should not exceed 50% of rated.

o Voltage Between Contacts. Voltage between contacts should not exceed 25% of the dielectric withstanding voltage.

o Insert Temperature. The connector insert temperature should be derated a minimum of 25°C from the maximum rated limit.

o Altitude Derating. Connectors intended for operation at reduced barometric pressures should be derated to account for the tendency of voltage flashover. This derating is specified in the military specifications for connectors intended for use at other than sea level barometric pressure. For reliability assurance, the high altitude ratings as given in the military specifications should be further derated to 50%. For nonstandard connectors, derating should be established based on military specification connectors of similar design and construction, especially with regard to dielectric type and contact spacing.

TABLE 5.2.8.3-1: CONNECTOR DERATING (SEA LEVEL)

Connector Type	Stress Parameter	% Stress (Allowed)
R-f Coaxial	Current	50
Multipin	Current	50
Cable	Current	50
All types	Voltage	See Table Below for Nonpressured Systems

TABLE 5.2.8.3-2: VOLTAGE DERATING AT ALTITUDE

Min Air Space	Voltage at Sea Level		
	Rated V (rms)	Working V	
		DC	AC (rms)
< 0.031	600	280	200
0.031	1000	490	350
0.045	1500	700	500
0.062	1800	840	600
0.076	2250	1050	750
	Voltage at 50,000 ft altitude		
< 0.031	225	100	75
0.031	375	190	125
0.045	525	210	175
0.062	675	315	225
0.076	790	360	360
	Voltage at 70,000 ft altitude		
< 0.031	150	70	50
0.031	300	125	90
0.045	375	175	125
0.062	450	210	150
0.076	500	230	165

5.2.9 ELECTRON TUBES

5.2.9.1 INTRODUCTION

While semiconductor devices have taken over many applications formerly accomplished by electron tubes, the latter devices still fill an important role in high power, microwave and millimeter wave applications. Listed below are classes of electron tubes still filling this important need.

(1) Power and gas tubes including pulse modulators, ignitrons and cold cathode tubes.

(2) Microwave tubes including travelling wave tubes, gas discharge, magnetrons and klystron.

(3) Indicator and pick up tubes including graphic indicators, cathode ray tubes and vidicons.

5.2.9.2 ELECTRON TUBE SELECTION CRITERIA

The selection criteria for electron tubes is given in Table 5.2.9.2-1. Appendix B provides a list of failure rates for various classes and types of tubes. This list quotes MIL-HDBK-217 base failure rates which include both random and recurrent failures.

5.2.9.3 FAILURE MODES AND MECHANISMS

The primary failure mechanism for electron tubes is heat, both the heat generated within the tube and external heat from surrounding sources. Four failure modes for electron tubes have been identified as resulting from excessive heat:

(1) deterioration or destruction of the seal

(2) tube gassing

(3) electron emission surface wearout

(4) increased electron emission by surfaces contaminated or damaged by excessive heat

TABLE 5.2.9.2-1: ELECTRON TUBE SELECTION CRITERIA

1. MIL-STD-200, "Electron Tubes, Selection Of."

2. MIL-E-1, "Electron Tubes, General Specification For."

3. MIL-STD-454, "Standard General Requirements for Electronic Equipment," Requirement No. 29.

Appendix B provides a list of failure rates for tubes taken from MIL-HDBK-217. These failure rates are from one to three orders of magnitude greater than semiconductor devices currently in use. These failure rates are provided

Supplier-required final inspection equipment.

TABLE 5.2.9.2-1: ELECTRON TUBE SELECTION CRITERIA (Cont'd)

	provided mainly for comparison and should be used only when no semiconductor device can be found to cover the specific design situation. In the case of high power/high frequency tubes, careful coordination with the tube manufacturers is recommended. Note that tubes, in general, possess much shorter useful life periods than semiconductor devices.
4.	Historical test data (similar applications) or other engineering information and/or data that provides assurance that the device is sufficiently rugged and reliable for the application (e.g., previous use in military equipment, comparable application or GFE).

5.2.10 CABLES

5.2.10.1 INTRODUCTION

This section deals with the many considerations to be employed when selecting cables. The section is divided into the following three major types of cables: coaxial (RF), multiconductor, and cable and wire interconnection.

5.2.10.2 SELECTION

General selection criteria for cables and interconnections are given in Table 5.2.10.2-1.

TABLE 5.2.10.2-1: SELECTION CRITERIA FOR CABLES

1. MIL-STD-454, "Standard General Requirements for Electronic Equipment," Requirements No. 65, 66, 71

2. An approved Military Specification style.

3. Historical data (similar application) test data or other engineering information that provides assurance that the cable is sufficiently rugged and reliable for the application (e.g., previous use in military equipment, comparable application or GFE). NOTE: When the use of a nonstandard cable is considered necessary, request for approval for its use shall be submitted to the military according to the procedures of MIL-STD-965.

The following requirements of MIL-STD-454 apply to the selection of cables:

Solid or stranded. Either solid or stranded conductors may be used - within the restrictions of the particular wire or cable specification - except that (a) only stranded wire shall be used in aerospace applications, and (b) for other applications, stranded wire shall be used when so indicated by the equipment specification. Specifically, stranded wire shall be used for wires and cables which are normally flexed in use and servicing of the equipment, such as cables attached to the movable half of detachable connectors.

Size. Conductors shall be of such cross section, temper, and flexibility as to provide ample and safe current carrying capacity and strength. In general, wire shall not be smaller than size 22. Smaller wire may be used when benefits can be obtained with no loss in performance. Specifically, smaller wire may be used in cables having larger number of wires and adequate support against vibration. Smaller size wire may be used when necessary for welding of electronic interconnections.

o Coaxial (RF) Cables. Selection of coaxial cable shall be in accordance with MIL-C-17, MIL-L-3890, MIL-C-22931, or MIL-C-23806 unless otherwise specified in the detail specification.

o Multiconductor Cable. Selection of multiconductor cable shall be in accordance with: MIL-C-442, MIL-C-3432, MIL-C-7078, MIL-C-13777, MIL-C-19547, MIL-C-21609, MIL-C-23437, MIL-C-27072, MIL-C-55057 unless otherwise specified in the detail specification.

o Interconnection Cable and Wire. Selection of interconnecting wire shall be in accordance with MIL-W-76, MIL-E-5086, MIL-W-7072, MIL-W-8777, MIL-W-16878, MIL-W-19150, MIL-W-22759, MIL-W-25038, MIL-W-81044, MIL-W-81381; selection of interconnecting cable shall be in accordance with: MIL-C-21609, MIL-C-23437, MIL-C-27072, MIL-C-27500, MIL-C-55021 unless otherwise specified in the detail specification.

5.2.10.3 SELECTION AND APPLICATION CONSIDERATIONS

(A) Coaxial (RF) Cable

For critical rf circuits, in addition to the electrical characteristics such as VSWR and capacitance, elements such as environmental requirements, short leads, and grounding shall be considered in design applications.

(B) Multiconductor Cable

o Solid or stranded. Either solid or stranded conductor may be used (within the restrictions of the particular wire or cable specification) except that (a) only stranded wire shall be in aerospace applications, and (b) for other applications stranded wire shall be used when so indicated by the equipment application. Specifically, stranded wire shall be used for wires and cables which are normally flexed in use and servicing of the equipment, such as cables attached to the movable half of detachable connectors.

o Size. Conductors shall be of such cross section, temper, and flexibility as to provide ample and safe current carrying capacity and strength. In general, wire shall not be smaller than size 22. Smaller wire may be used when benefits can be obtained with no loss in performance. Specifically, smaller wire may be used in cables having larger numbers of wires and adequate support against vibration. Smaller size wire may be used when necessary for welding of electronic interconnections.

o Application. Multiconductor cable shall be in accordance with Table 66-I of MIL-STD-454 unless otherwise specified in the detail equipment specification.

o Polyvinyl chloride insulation. Cable using polyvinyl chloride insulation shall not be used in airborne applications.

(C) Interconnect Cable and Wire

o Electrical connections shall be arranged and wired so that no leads are terminated in pins or other exposed contacts which might be accidentally shorted or touched.

o All interconnecting cables carrying pulsed or rf signals shall make use of coaxial cable or waveguides and shall be terminated, when possible, in the characteristic impedance of the transmitting media, except when this requirement conflicts with the detail specification.

o All open wire power and control cables shall be terminated in the lowest impedance practicable for the particular applications.

o The shield of shielded cables shall be connected to a ground lead at least at one point in the circuit.

o Consideration shall be given to weight saving by use of aluminum wires and cables; however, approval for their installation shall be obtained from the procuring activity.

o Selection of wire for interconnection between units shall be in accordance with Table 71-I of MIL-STD-454 unless otherwise specified in the detail equipment specification.

o Selection of flexible or semirigid coaxial cable for interconnection between units shall be in accordance with the applicable coaxial cable requirements.

o Selection of multiconductor cable for interconnection between units shall be in accordance with Table 71-II of MIL-STD-454 unless otherwise specified in the detail equipment specification.

o Cable or wire using polyvinyl chloride insulation shall not be used in airborne applications.

(D) Definitions

o Interconnecting wire. Insulated, single conductor wire used to carry electric current between units. Hookup wire may be used for this purpose providing adequate jacketing is applied to the wire bundle to render it serviceable in the specified environment.

o Interconnecting cable. Two or more insulated conductors contained in a common cover or one or more insulated conductors with a gross metallic shield or outer conductor should be used to carry electrical current between units.

5.2.11 ELECTRO OPTICS/FIBER OPTICS

5.2.11.1 INTRODUCTION

Optical fiber data transmission networks are becoming increasingly attractive, especially where immunity to electromagnetic interference, avoidance of ground loops, or high transmission rates are required. Optical fibers offer the following advantages over conventional wired links which are relevant in a number of important military applications. They are spark free, lightweight and crush resistant and do not require electrical insulation. They are also free of crosstalk and electromagnetic interference problems. Fiber transmission systems controlling remote equipment and transferring data from unit to unit are free from the problems of noise, particularly those caused by motors and relays. Specific examples of benefits afforded by the use of fiber optics are:

- One fiber optic filament several mils in diameter can replace a copper wire several inches in diameter. This savings in size and weight is especially important for mobile military applications.
- Optical cables are safe to use in explosive environments and eliminate the hazards of short circuits in metal wires and cubes. Optical systems can be made to have total electrical isolation.
- Properly designed optical transmission lines and couplers are relatively immune to adverse temperature and moisture conditions - a most important military consideration.

All of the above advantages, along with bandwidth increases, make optical communications very attractive for numerous military applications, including telephones (loops, trunks, terminals and exchanges) computers (internal and external links), space vehicle avionics, ships, submarine cable and special tethers, as well as a host of industrial applications.

When referring to a fiber optic communications link a multicomponent system is implied. Some of the noteworthy components are: the laser or light emitting diode (LED) as the optical transmitter; the optical fiber as the transmission medium; the couplers and the PIN or avalanche photodiode as the optical receiver.

Reliability of such a system will be dependent upon device and fiber lifetime. Mean time to failure (MTTF) for laser diodes and LED's vary between 10^6 and 10^7 hours. The mean time to failure of the fibers has not been established.

It is possible that in the long term stress corrosion factors will present themselves as problems for extended life of fibers and cables, i.e., flaws in the optical fiber propagate and weaken the fiber and cables and, therefore, cables have to be hardened to minimize these effects.

5.2.11.2 SPECIFICATION AND STANDARDS

Unlike most of the electronics parts covered in this Handbook there is a comparative dearth of military specifications and standards relative to fiber optic cable assemblies. What relevant documents exist are listed in Table 5.2.11.2-1. Accordingly, what is presented here is the status of specifications and standards available in 1982 and an expression of the general content of these specifications and standards. These technology areas have not as yet matured to the point where the military is prepared to make specific recommendations relative to standard parts or provide the necessary data for reliability prediction as presented in MIL-HDBK-217. (MIL-HDBK-217C contains only a small section on light emitting diodes (LED), optic electronic couplers, and LED alphanumeric displays).

Some of the documents described below are in a transitional phase and will continue in that manner until the technology matures.

TABLE 5.2.11.2-1: SPECIFICATIONS AND STANDARDS RELEVANT TO MILITARY APPLICATIONS

1. Military Specification DOD-C-85045. Cables, Fiber Optics, General Specification for (Metric).

2. Military Standard DOD-STD-1678 Fiber Optics Test Methods and Instrumentation.

3. Special Publication, NTIA-SP-79-4 Optical Waveguide Communications Glossary, U.S. Department of Commerce, Sept. 1979.

4. Electronics Industries Association (EIA) Standard RS-455 and addendums, Standard Test Procedures for Fiber Optic Fibers, Cables, Transducers, Connecting and Terminating Devices, March 1980 Addendums 1,2,3,May 1980; Feb, 81; May, 1981.

5. MIL-S-19500, Semiconductor Devices, General Specification For.

The dates are included above to indicate the recent and continuing issuance of these documents which to this point have not been amended. Additionally, EIA Standard RS-455 is included because of the serious interest on the part of the military in adopting this industry standard.

o Military Specification DOD-C-85045. This specification covers the general requirements and characteristics for cables employing optical fibers for data transmission. Whenever applicable, this general specification is used in concert with DOD-1678 which describes the test methods identified in Section 4 of DOD-C-85045; the types called out therein will be given in more detail under the discussion of DOD-1678. In DOD-C-85045 qualification requires performance of forty-one tests which are divided into two groups. The entire sample must be subjected to the seven tests

called for in Group 1 inspection. Two to four specimens of the total sample are subjected to the remaining thirty-four tests. One or more failures in qualification testing are cause for refusal of qualification approval. Quality conformance inspection includes Groups A, B, and C, tests. Group A inspection encompasses fourteen tests sampled in accordance with MIL-STD-105, Inspection Level II to a 1.0% AQL. Group B inspection includes six tests sampled in accordance with MIL-STD-105, Inspection Level S-3, to a 1.0% AQL. Group C inspection includes eighteen tests conducted on sample sizes related to lot size as called out in this specification.

o Military Standard DOD-1678. This standard is the oldest of the military documents associated with fiber optic assemblies. The standard provides general physical, electrical and chemical methods for testing fiber optic cables. Measurements and tests included in the standard are:

1. Fiber size and bundle diameter measurement
2. Low temperature flexibility (cold bend method)
3. Impact and twist testing
4. Compressive strength testing
5. Cable tensile loading
6. Power transmission vs. temperature and temperature cycling
7. Dimensional stability and flammability testing
8. Radiant power and radiation power measurements
9. Attenuation measurements
10. Acceptance pattern measurements
11. Pulse spreading and crosstalk measurements
12. Fiber bundle transfer function measurements
13. Refractive index profile
14. Insulating, blocking, wicking and fluid immersion
15. Jacket flow detection and leak testing
16. Fiber and bundle preparation

Most if not all of the above test methods relate to fibers or cables.

o EIA Standard RS-455 and Addendums. While DOD-STD-1678 applies primarily to fiber optic cable test methods, EIA Standard RS-455 test methods apply to connecting or interconnecting devices. Test methods and procedures covered are:

1. Cable Flexing for Fiber Optic Connections
2. Impact Test Measurements
3. Temperature Cycling of Fiber Optic Connectors (Thermal Shock)
4. Fiber Optic Temperature Connector Life
5. Humidity Test Procedures for Fiber Optic Connecting Devices
6. Fiber Optics Bundle Connector Insertion Loss
7. Cable Retention Procedure for Fiber Optic Cable Interconnecting Devices
8. Vibration Test Procedures for Fiber Optic Connection Devices
9. Maintenance Aging
10. Acceleration
11. Impact Testing of Fiber Optic Cables and Cable Assemblies
12. Fiber Tensile Proof Test Methods

o NTIA-SP-79-4 Optical Waveguide Communications Glossary. This document is a technical dictionary containing approximately 300 terms concisely defined for the communications engineer, covering the field of optical fiber waveguide communication. These terms have been borrowed from the discipline of optical physics and communications engineering; others have been coined independently.

REFERENCES

1. Jones, B.E., Optical Fibers and Electro-Optics for Instrumentation Electronics and Power (U.K.) Feb. 81.

2. Military Specification DOD-C-85045 Cables Fiber Optics, General Specification for (Metric).

3. Military Standard - DOD Standard 1678 - Fiber Optics Test Methods and Instrumentation.

4. EIA Standard RS455 and Addendum 1,2,3, Standard Test Procedures for Fiber Optic Fibers, Cables, Transducers, Connecting and Terminating Devices.

5. NTIA-SP-79-4 Optical Waveguide Communications Glossary, U.S. Department of Commerce.

5.2.12 PRINTED CIRCUITRY

5.2.12.1 INTRODUCTION

Applications for printed circuitry continue to expand to meet the ever increasing need for size and weight reduction in military equipment. The applications have become more varied and demanding to keep up with the technological advance in the microcircuit and microprocessor areas, particularly those advances associated with higher speed performance and increased circuit density.

In practice printed circuit assemblies consist of a number of component parts and important associated processes as follows:

(1) printed wiring board or the interconnecting medium of individual parts or microcircuits

(2) component parts to be interconnected and the printed circuit connector for interconnecting other assemblies

(3) integrating of the component parts by manual or automated soldering processes

(4) conformal coating of the assembly to protect it from external environments.

5.2.12.2 PRINTED CIRCUIT DESIGN AND TREATMENT CRITERIA

The manufacture of a printed wiring assembly includes many materials and processes with a variety of military specifications and standards. The design and treatment criteria are governed by the specifications and standards listed in Table 5.2.12.2-1.

TABLE 5.2.12.2-1: DESIGN AND TREATMENT CRITERIA FOR PRINTED CIRCUITRY

1.	MIL-P-81728	Plating Tin-Lead (Electrodeposited)
2.	MIL-P-13949	Plastic Sheet, Laminated Copper Clad for Printed Wiring
3.	MIL-C-21097	Connectors, Electrical, Printed Wiring Board, General Purpose
4.	MIL-P-28809	Printed Wiring Assemblies
5.	MIL-I-46058	Insulating Compound, Electrical (for Coating Printed Circuit Assemblies)
6.	MIL-P-50884	Printed Wiring Flexible, General Specification For

TABLE 5.2.12.2-1: DESIGN AND TREATMENT CRITERIA FOR PRINTED CIRCUITRY (Cont'd)

7.	MIL-P-55110	Printed Wiring Boards
8.	MIL-C-55302	Connectors, Printed Circuit Subassembly and Accessories
9.	IPC-CF-150	Foil, Copper Cladding for Printed Wiring Boards
10.	MIL-P-13949	Plastic Sheet, Thin Laminate, Copper Clad (for Printed Wiring Primarily Multilayer)
11.	MIL-STD-275	Printed Wiring for Electronic Equipment
12.	IPC-T-50B	Terms and Definitions for Interconnecting and Packaging Electronic Circuits
13.	MIL-STD-454	Circuits, Terms and Definitions, Standard General Requirements for Electronic Equipment (Requirements 5 and 17)
14.	MIL-STD-1495	Multilayer Printed Wiring Boards for Electronic Equipment

Abstracts of some of the major documents listed in Table 5.2.12.2-1 are given below:

MIL-STD-275 establishes design principles governing the fabrication of rigid single or double sided printed circuit boards and the mounting of parts (including integrated circuits) and assemblies thereon for use in electronic equipment.

IPC-T-50B establishes terms and definitions which have a specific meaning when applied to printed wiring and printed circuit nomenclature.

MIL-I-46058 covers conformal coatings which are applicable to printed circuit assemblies by dipping, brushing, spraying, or vacuum deposition.

MIL-P-55110 covers printed boards consisting of conductor pattern on the surface of one or two sides of an insulating base and associated interfacial connections and standoff terminals.

Also covers rigid plated through hole multilayer printed boards consisting of three or more conductor patterns on insulating bases separated one from the other by an insulating material and interconnected by a continuous metallic interlayer connections.

MIL-C-21097 covers multiple contact connectors for 1/16, 3/32, and 1/8 inch printed boards and for interconnection between printed boards.
Abstracts of the documents listed in Table 5.2.12.2-2 are given below.

MIL-F-14256 provides requirements concerning the fluxing process for printed wiring assemblies.

QQ-S-571 is a federal specification which covers solders in the form of solid bars, ingots, powder, flux cored ribbon and wire, and solder paste.

MIL-S-45743 covers the manual soldering operation for applications requiring extraordinary control of environment and techniques.

MIL-S-46844 covers automatic solder processes for printed wiring assemblies used in electrical and electronic equipment.

MIL-C-55302 covers connectors (plugs and receptacles) for printed circuit subassemblies and their accessories for use with single sided, double sided, and multilayer printed wiring.

Table 5.2.12.2-2 lists specifications and standards which govern materials and processes applicable to solder connections.

TABLE 5.2.12.2-2: MATERIALS AND PROCESSES CRITERIA FOR SOLDER CONNECTIONS

1.	MIL-F-14256	Flux, Soldering, Liquid (Rosin Base)
2.	QQ-S-571	Solder, Tin Alloy, Tin Lead Alloy, and Lead Alloys
3.	MIL-S-45743	Soldering, Manual Type, High Reliability, Electrical, Electronic, Instrument, Communication and Radar for Aerospace
4.	MIL-S-46844	Solder Bath Soldering of Printed Wiring Assemblies
5.	IPC-T-508	Terms and Definitions for Interconnecting and Packaging Electronic Circuits
6.	MIL-STD-454	Standard General Requirememnts for Electronic Equipment (Requirement 5)

5.2.12.3 COMPONENT MOUNTING (SOLDERING)

Components are inserted into the printed wiring boards either automatically or by hand. Then flux is applied to the appropriate surfaces and the components are soldered into place. Soldering options include hand or wave soldering. Printed wiring assemblies which contain flatpack packaged components generally utilize a reflow soldering operation to secure the components.

o Wave Soldering. In wave soldering, the solder is pumped out of a narrow slot to produce a wave or series of waves. The conveyor should be at a small angle to the horizontal to assist drainage of the solder. Wave soldering systems result in a virtually oxide free solder surface in contact with the component leads. Removal of flux and vapors are also promoted by the flow of solder. It is essential that residues from activated fluxes are removed. The flux residues can result in a weakened solder connection if not entirely removed and flux residues can contaminate the board surface causing short circuits between conductor paths. Integrated wave soldering systems for printed wiring assemblies provide units which can apply the flux, dry and preheat the board, solder components and clean the completed assembly. Some systems employ oil mixed with the solder to aid in the elimination of solder icicles and prevent bridging between conductor paths.

o Hand Soldering. The hand soldering operation requires trained personnel to insure reliable solder connections. Prolonged exposure to the hot soldering iron can result in delamination of the copper foil or unnecessary plated through hole degradation.

o Vapor Phase Soldering. The vapor phase process, a unique approach to soldering, relies on the latent heat of vaporization of a fluid condensing from its saturated vapor phase. This phase change results in extremely rapid and efficient transfer of energy from the vapor to a cooler product immersed in the vapor.

Solder and flux required are applied prior to the product's immersion in the vapor. As the product is lowered into the region of saturated vapor above the boiling heat transfer fluid, the vapor condenses onto all the surfaces of the cooler part, heating the surfaces rapidly and uniformly to the soldering temperature. Since the temperature of a saturated vapor is the same as the boiling point of its fluid, the soldering temperature is thus predetermined by the heat transfer fluid chosen. For any given fluid, this temperature is constant, resulting in a process both precisely and repeatably controlled, simply and without intricate and costly controls.

Furthermore, the amount of energy available for heat transfer can be varied without affecting the temperature. This provides adaptability of the process to a variety of applications, independent of product geometry or configuration.

The heat transfer fluids used are high boiling point perfluorinated inert liquids. The most commonly used fluid has a boiling point of 215°C (419°F), a convenient 32°C (58°F) above the melting point of the tin/lead eutectic alloy. Thus, the process is ideal for reflow of 63Sn/37Pb, 60Sn/40Pb, 62Sn/36Pb/2Ag, and other widely used solder alloys with similar compositions.

The use of the vapor phase soldering technique in the attachment of alumina microcircuit chip carriers to multilayer ceramic substrates is a rapidly growing practice. Mismatch in temperature coefficients prevents the technique from being used in the attachment of ceramic substrates to standard glass epoxy PCBs. However, PCBs made with an Invar metal core (i.e., high Ni constant) or with Kevlar fiber strands have effectively the same temperature coefficient as alumina, and thus make possible the use of the vapor phase soldering process in attaching ceramic substrates to the PCB.

5.2.12.4 PRINTED WIRING BOARD SELECTION

Applications which require high circuit or packaging density are most compatible with multilayer printed wiring boards. Multilayer technology allows printed wiring boards to be manufactured with up to 16 circuit planes and even more in some applications. Other cases exist where neither high circuit or packaging density is required. In these cases, the use of double sided printed wiring boards may prove to be most cost effective. The type of printed wiring board which is most suitable for a particular application must be decided after considering many different factors.

There is a relatively lengthy time interval between design submittal and finished product for multilayer printed wiring boards. This lengthy turn around time coupled with the high demand for printed wiring boards results in the emergence of several alternatives to printed wiring. Alternate types of interconnection assemblies include solderless wrap, clip termination, wrapped and soldered, and discrete wiring with plated through hole connection assemblies.

Usage and selection guidelines for printed wiring boards and several alternate types of interconnection assemblies are given in Table 5.2.12.4-1.

TABLE 5.2.12.4-1: USAGE AND SELECTION GUIDELINES FOR INTERCONNECTION ASSEMBLIES

Type	Specification	Usage Notes	Failure Modes
Single Sided Board	MIL-P-55110	Not intended for application where high packaging density or complex circuitry is required.	Entrapped moisture can cause warping and measling of the board surfaces.
Double Sided Board		Intended for use where only average packaging density is required. Components mounted on this type of board are accessible for repair or replacement. Many standard circuit designs are commercially available on this type of board.	Failure modes for single sided boards apply. Also, poor drilling, or excessive acid etching during the plated through hole cleaning process can lead to imperfections in the barrel wall amplifying the level of axial strain. This additional strain and/or poor ductility of the copper plating can cause open circuits in the plated through hole.
Multilayer Board		Intended for use where very high density is desired. This type of interconnection board is not cost effective in applications where only small production runs are manufactured. Additionally, this type of board should only be used when little or no design changes are anticipated. Repairs to the board and to board mounted components are difficult.	Failure modes for single sided boards and double sided boards apply. Also, poor registration of the plated through hole to an individual copper run on an interior layer can result in an open circuit.
Wirewrap Interconnection Board	MIL-STD-1130	This type of board is optimal for applications where the design is not matured and experimentation is anticipated. Wirewrap boards offer the greatest flexibility for change and are the easiest to repair. Due to the long wirewrap posts, packaging density for wirewrap is the worst among comparable interconnection methods.	Insufficient tension in the wire can result in a poor connection between the wire and the wirewrap post. Additionally, cold flow of wire insulation accelerated by extreme environment conditions can cause a short circuit between adjacent wires. Correct choice of wire insulation can prevent this phenomenon.
Multiwire Interconnection Board	IPC-DW-425	Use in applications where average packaging density and light weight are desired. Use of this type of board can be most cost effective in many applications. Repairs and design changes can tend to be a problem on multiwire boards. Therefore, the use of this type of board is not recommended where many design changes are anticipated.	The points of wire crossover are a potential source of failure. Deformation of the upper wire and insulation can occur under extreme environment conditions. The wire to hole connection can be the source of open circuits if manufacturing precision is not maintained.

5.2.13 STANDARD ELECTRONIC MODULE (SEM) PROGRAM

5.2.13.1 INTRODUCTION

The Standard Electronic Module (SEM) Program is an electronic module standardization program coordinated throughout the Navy by the Naval Electronic Systems Command. The purpose of the SEM Program is to make available a family of high reliability, low cost, functional electronic modules that will reduce the cost and expedite the design and production of military electronic systems. By limiting the continued proliferation of electronic hardware in systems development, the logistical support posture of these system will be significantly improved. The SEM modules are currently (March, 1981) being applied in more than one hundred equipment applications that span virtually all operating environments, resulting in the commitment to service of over five million modules. As the SEM program continues to gain further acceptance, the cost and performance benefits accruable to the Navy, and perhaps to the other Services, should continue.

5.2.13.2 SEM PROGRAM OBJECTIVES

The objectives of the SEM Program are:

- Partition of electronic functions in a manner so as to be common to a majority of users
- Document modules with functional specifications to preclude dependence upon specific vendor design or technology, thereby enabling cost savings through vendor innovation and competition
- Achieve high reliability through stringent quality assurance requirements for module designs and vendors
- Achieve discard upon failure policy
- Provide flexible mechanical packaging requirements which accept various circuit technologies, device packages, and growth increments
- Establish basic requirements compatible with a majority of military systems applications and environments
- Ease the logistics support burden on the congested military supply system by extensive intersystem commonality of a limited number of modules

5.2.13.3 SEM SELECTION AND USE CRITERIA

The selection and use of Standard Electronic Modules are governed by the criteria in Table 5.2.13.3-1.

TABLE 5.2.13.3-1: SELECTION AND USE CRITERIA FOR STANDARD ELECTRONIC MODULES

1.	MIL-STD-1378	"Requirements for Employing Standard Electronic Modules"
2.	MIL-STD-1389	"Design Requirements for Standard Electronic Modules"
3.	MIL-STD-1655	"Module Description for the SEM Program"
4.	MIL-M-28787	"Standard Electronic Modules, General Specification For"
5.	MIL-HDBK-246	"Program Managers' Guide for the Standard Electronic Modules Program"
6.	NAC TP-526	"SEM Program Microprocessor Applications Handbook"
7.	NAC TP-528	"SEM Program Memory Application Handbook"
8.	NAC TP-529	"SEM Thermal Application Handbook"
9.	NAC TP-531	"In Process Module Descriptions Handbook"
10.	TP-532	"SEM Hardware Catalog"
11.	(No Number)	"Program Module Testing"
12.	Report #393-2	"SEM Systems Applications Report"

5.2.13.4 SEM PROGRAM REQUIREMENTS

The SEM Program has adopted a flexible module packaging concept in which form, fit, function, and quality are the controlling parameters.

o Mechanical (Form, Fit). The SEM Program provides multiple module formats and sizes in a disciplined incremental growth approach to accommodate a variety of system packaging alternatives. The basic SEM configuration figuration is the single format, single thickness (1A size) Format A Configuration with overall dimensions of 2.6 inches in width, 1.95 inches in height, and 0.290 inches in thickness. There are provisions for multiple growth increments, permitting modules to increase in span by increments of 3.00 inches and in thickness by increments of 0.300 inches.

o Electrical (Function). In order that the basis for standardization can be affected, each standard module represents a complete function or group of functions, specifiable and testable without another module. Digital modules employ standardized digital logic levels and power supply voltages. Module power supply circuit ground, frame ground, and signal lines have been assigned to specific pins on the module connector.

5.2.13.5 QUALITY AND RELIABILITY

Electronic parts used in SEMs have a demonstrated quality level and environmental performance equivalent to that of available military parts. For example: discrete semiconductors are required to meet the JAN TX requirements of MIL-S-19500 and the applicable detail specifications; integrated circuits are required to meet the requirements of MIL-M-38510, Class B and the applicable detail specifications. Also integrated circuits procured to source control drawings are acceptable provided the manufacturing drawings and screens are the equivalent of Class B requirements.

Two environmental classes have been established for the overall module:

Class 1 is compatable with MIL-E-16400 for shipboard and shore;
Class 2 is compatible with MIL-E-5400 oriented toward avionics.

A third class, Class 3, currently being introduced into the SEM program will incorporate nuclear radiation requirements to the basic Class 2 module category.

REFERENCE

1. Anon., Standard Electronic Modules Program, March 1981

6.0 APPLICATIONS GUIDELINES

6.1 ENVIRONMENTAL CONSIDERATIONS

6.1.1 ENVIRONMENTAL RESISTANCE

In order to realize fully the benefits of a reliability oriented design, consideration must be given early in the design process to the required environmental resistance of the equipment being designed. The environmental resistance, both intrinsic and that provided by specifically directed design features, will singularly determine the ability of the equipment to withstand the deleterious stresses imposed by the environment in which the equipment will be operated. The initial requirement for determining the required environmental resistance is the identification and detailed description of the environments in which the equipment must operate. The next step is then the determination of the performance of the components and materials that comprise the equipment when exposed to the degrading stresses of the environments so identified. When such performance is inadequate or marginal with regard to the equipment reliability goals, corrective measures such as derating, redundancy, protection from adverse environments, or selection of more resistant materials and components are necessary to fulfill the reliability requirements of the equipment.

6.1.2 ENVIRONMENTAL FACTORS

Since reliability is strongly dependent upon the operating conditions that are encountered during the entire life of the equipment, it is important that such conditions are accurately identified at the beginning of the design process. Environmental factors which exert a strong influence on equipment reliability are listed in Table 6.1.2-1 and discussed on the following pages.

6.1.2.1 TEMPERATURE EFFECTS

High temperature imposes a particularly severe stress on most electronic components since it can cause catastrophic failure such as melting of solder joints and burnout of solid state devices. They also can induce slow progressive deterioration of component performance levels due primarily to chemical degradation effects. It is often stated that excessive temperature is the primary cause of poor reliability in military electronic equipment.

In present day electronic systems design, great emphasis is placed on small size and high component part densities. This generally requires a cooling system to provide a path of low thermal resistance from heat producing elements to an ultimate heat sink of reasonably low temperature.

Solid state components are generally rated in terms of maximum junction temperatures, and the thermal resistances from this point to either the case or to free air are usually specified. The specification of maximum ambient temperature for which a component is suitable is generally not a sufficient method for component selection with densely packaged parts

TABLE 6.1.2-1: ENVIRONMENTAL STRESSES, EFFECTS, AND RELIABILITY IMPROVEMENT TECHNIQUES IN ELECTRONIC EQUIPMENT

Environmental Stress	Effects	Reliability Improvement Techniques
High Temperature	Parameters of resistance, inductance, capacitance, power factor, dielectric constant, etc., will vary; insulation may soften; moving parts may jam due to expansion; finishes may blister; devices suffer thermal aging; oxidation and other chemical reactions are enhanced; viscosity reduction and evaporation of lubricants are problems; structural overloads may occur due to physical expansions.	Heat dissipation devices, cooling systems, thermal insulation, heat-withstanding materials.
Low Temperature	Plastics and rubber lose flexibility and become brittle; electrical constants vary; ice formation occurs when moisture is present; lubricants gel and increase viscosity; high heat losses; finishes may crack; structures may be overloaded due to physical contraction.	Heating devices, thermal insulation, cold-withstanding materials.
Thermal Shock	Materials may be instantaneously overstressed causing cracks and mechanical failure; electrical properties may be permanently altered. Crazing, delamination, ruptured seals.	Combination of techniques for high and low temperatures.
Shock	Mechanical structures may be overloaded causing weakening or collapse; items may be ripped from their mounts; mechanical functions may be impaired.	Strengthened members, reduced inertia and moments, shock absorbing mounts.
Vibration	Mechanical strength may deteriorate due to fatigue or overstress; electrical signals may be mechanically and erroneously modulated; materials and structures may be cracked, displaced, or shaken loose from mounts; mechanical functions may be impaired; finishes may be scoured by other surfaces; wear may be increased.	Stiffening, control of resonance.
Humidity	Penetrates porous substances and causes leakage paths between electrical conductors; causes oxidation which leads to corrosion; moisture causes swelling in materials such as gaskets; excessive loss of humidity causes embrittlement and granulation.	Hermetic sealing, moisture-resistant material, dehumidifiers, protective coatings.
Salt Atmosphere and Spray	Salt combined with water is a good conductor which can lower insulation resistance; causes galvanic corrosion of metals; chemical corrosion of metals is accelerated.	Nonmetal protective covers, reduced use of dissimilar metals in contract, hermetic sealing, dehumidifiers.
Electromagnetic Radiation	Causes spurious and erroneous signals from electrical and electronic equipment and components; may cause complete disruption of normal electrical and electronic equipment such as communication and measuring systems.	Shielding, material selection, part type selection.
Nuclear/Cosmic Radiation	Causes heating and thermal aging; can alter chemical, physical and electrical properties of materials; can produce gases and secondary radiation; can cause oxidation and discoloration of surfaces; damages electrical and electronic components especially semiconductors.	Shielding, component selection, nuclear hardening.

TABLE 6.1.2-1: ENVIRONMENTAL STRESSES, EFFECTS, AND RELIABILITY IMPROVEMENT TECHNIQUES IN ELECTRONIC EQUIPMENT (Cont'd)

Environmental Stress	Effects	Reliability Improvement Techniques
Sand and Dust	Finely finished surfaces are scratched and abraded; friction between surfaces may be increased; lubricants can be contaminated; clogging orifices, etc.; materials may be worn, cracked, or chipped; abrasion, contaminates insulations, corona paths.	Air-filtering, hermetic sealing.
Low Pressure (High Altitude)	Structures such as containers, tanks, etc., are overstressed and can be exploded or fractured; seals may leak; air bubbles in materials may explode causing damage; internal heating may increase due to lack of cooling medium; insulations may suffer arcing and breakdown; ozone may be formed; outgassing is more likely.	Increased mechanical strength of containers, pressurization, alternate liquids (low volatility), improved insulation, improved heat transfer methods.

since the surface temperatures of a particular component can be greatly influenced by heat radiation or heat conduction effects from other nearby parts. These effects can lead to overheating above specific maximum safe temperatures even though the ambient temperature reading appears not to be exceeded. It is preferable, therefore, to specify thermal environment ratings such as equipment surface temperatures, thermal resistance paths associated with conduction, convection and radiation effects, and cooling provisions such as air temperature, pressure and velocity. In this manner, the true thermal state of the temperature sensitive internal elements can be determined.

Low temperatures experienced by electronic equipment can also cause reliability problems. These problems are usually associated with mechanical elements of the system and include mechanical stresses produced by differences in the coefficients of expansion (contraction) of metallic and nonmetallic materials, embrittlement of nonmetallic components, mechanical forces caused by freezing of entrapped moisture, stiffening of liquid constituents, etc. Typical examples include cracking of seams, binding of mechanical linkages, and excessive viscosity of lubricants.

Additional stresses are produced when electronic equipment is exposed to sudden changes of temperature or rapidly changing temperature cycling conditions. These conditions generate large internal mechanical stresses in structural elements particularly when dissimilar materials are involved. Effects of the thermal shock induced stresses include cracking of seams, delamination, loss of hermeticity, leakage of fill gasses, separation of encapsulating components from components and enclosure surface leading to the creation of voids, and distortion of support members.

A thermal shock test is generally specified to determine the integrity of solder joints since such a test creates large internal forces due to differential expansion effects. Such a test has also been found to be instrumental in creating segregation effects in solder alloys leading to the formulation of lead rich zones which are susceptible to cracking effects.

6.1.2.2 MECHANICAL SHOCK

Electronic equipment is often subjected to environmental shock and vibration both during normal use and testing. Such environments can cause physical damage to components and structural members when deflections produced cause mechanical stresses which exceed the allowable working stress of the constituent parts.

The natural frequencies of subsystems comprising the equipment are important parameters which must be considered in the design process since a resonant condition can be produced if a natural frequency is within the vibration frequency range. The resonant condition will greatly amplify the deflection of the subsystem and may increase stresses beyond the safe limit.

The vibration environment can be particularly severe for electrical connectors since it may cause relative motion between members of the connector. This motion in combination with other environmental stresses can produce fret corrosion which generates wear debris and causes large variations in contact resistance.

6.1.2.3 HUMIDITY AND SALT

Humidity and salt air environments can cause degradation of equipment performance since they promote corrosion effects in metallic components and can foster the creation of galvanic cells, particularly when dissimilar metals are in contact. Another deleterious effect of humidity and salt air atmospheres is the formation of surface films on nonmetallic parts which cause leakage paths and degrade the insulation and dielectric properties of these materials. Absorption of moisture by insulating materials can also cause a significant increase in volume conductivity and dissipation factor of materials so affected.

6.1.2.4 ELECTROMAGNETIC AND NUCLEAR RADIATION

Electromagnetic and nuclear radiation can cause disruption of performance levels and, in some cases, permanent damage to exposed equipment. It is important, therefore, that such effects be considered in determining the required environmental resistance for electronic equipment that must achieve a specified reliability goal.

Electromagnetic radiation often produces interference and noise effects within electronic circuitry which can impair the functional performance of the system. Sources of these effects include corona discharges, lightning discharges, sparking and arcing phenomena. These may be associated with high voltage transmission lines, ignition systems, brush-type motors, and even the equipment itself. Generally, the reduction of interference effects requires incorporation of filtering and shielding features or the specification of less susceptible components and circuitry.

Nuclear radiation can cause permanent damage by alteration of the atomic or molecular structure of dielectric and semiconductor materials. High energy radiation can also cause ionization effects which degrade the insulation of dielectric materials. The mitigation of nuclear radiation effects typically involves the use of materials and components possessing a higher degree of intrinsic radiation resistance and the incorporation of shielding and hardening techniques.

6.1.2.5 OTHER STRESS FACTORS

In addition to the aforementioned stress factors, other environmental factors may require consideration in the design process to assure that adequate environmental resistance is incorporated into the equipment design. These additional factors include:

- Sand and dust
- Fungus
- Acoustic noise
- Electric fields
- Magnetic fields
- Presence of reactive liquids and gases

Each of these stress factors, if present, requires determination of its impact on the operational and reliability characteristics of the materials and components comprising the equipment being designed and the identification of material, component and packaging techniques that afford the necessary protection against such degrading factors.

In the environmental stress identification process that precedes the selection of environmental resistance techniques, it is essential that stresses associated with all life intervals of the equipment be considered. This also includes not only the operational and maintenance environments but also the preoperational environments when stresses imposed on the parts during manufacturing, assembly, inspection, testing, shipping and installation may have significant impact on the eventual reliability of the equipment. Stresses imposed during the preoperational phase are often overlooked, but they may represent a particularly harsh environment which the equipment must withstand. Often the shock and humidity environments to which commercial and military systems are exposed during shipping and installation are more severe than those it will encounter under normal operating conditions. It is also probable that some of the environmental resistance features that are contained in a system design pertain to conditions that are encountered in the preoperational phase and not in conditions that the equipment experiences after being put into operation.

6.1.3 ENVIRONMENTAL RESISTANCE PROVISIONS

After identification of all environmental stress factors that will be encountered by a particular electronic system, a determination is made of components and elements of the system which will be adversely affected and the effects of this degradation on the apportioned reliability goals. Generally, such a determination will not only identify elements of the proposed design that are totally unsuitable but, also, will identify trade-off situations where incorporation of specific protective features will significantly enhance the achievable reliability.

In these cases, the solution is the specification of components having greater inherent resistance to the identified environmental stresses and the selection of particular protection techniques for reducing these stresses to levels that produce more favorable reliability characteristics.

6.1.3.1 THERMAL PROTECTION

Since excessive temperature is a primary cause of operational and reliability degradation, each proposed system design must be evaluated to establish that its thermal performance is consistent with the required equipment reliability. The preferred method for evaluating the thermal performance of electronic equipment (with respect to reliability) is a parts stress analysis method (see Volume I, Subsection 6.4.4) which determines the maximum safe temperatures for constituent parts. A reduction in the operating temperature of components is a primary method for achieving improved reliability levels. This is generally possible by provision of a thermal design which reduces heat input to minimally achievable levels and provides low thermal resistance

paths from heat producing elements to an ultimate heat sink of reasonably low temperature. The thermal design is often as important as the circuit design in obtaining the necessary performance and reliability characteristics of electronic equipment. Thermal design considerations and procedures are discussed in Section 6.2.2.

The failure rates of electronic system components vary significantly with temperature. Table 6.1.3.1-1 illustrates the reliability improvement potential that is associated with the operation of circuit

TABLE 6.1.3.1-1: RELIABILITY IMPROVEMENT POTENTIAL AT REDUCED TEMPERATURES (EXPRESSED IN FAILURE RATES)

Part Description	λb Failures Per Million Hours Base Failure Rate *		$\Delta T^{\circ}C$	Ratio of High to Low Failure Rate
	High Temperature	Low Temperature		
PNP Silicon Transistors	.063 at 130°C and 0.3 stress	.0096 at 25°C and 0.3 stress	105	7:1
NPN Silicon Transistors	.033 at 130°C and 0.3 stress	.0064 at 25°C and 0.3 stress	105	5:1
Glass Capacitors	.047 at 120°C and 0.5 stress	.001 at 25°C and 0.5 stress	95	47:1
Transformers and Coils MIL-T-27 Class Q	.0267 at 85°C	.0008 at 25°C	60	33:1
Resistors Carbon Comp	.0065 at 100°C and 0.5 stress	.0003 at 25°C and 0.5 stress	75	22:1

*Taken from MIL-HDBK-217C

elements at reduced temperatures. A consideration of life cycle costs will generally indicate that the cost of designing and implementing adequate thermal performance into equipment is fully recovered by savings in maintenance costs early in the operational life of the equipment. A suitable thermal design will also minimize temperature excursions of components when environmental temperatures or power dissipation vary, resulting in further reliability benefits.

The part stress analysis method for evaluating system thermal performance is based on a determination of the maximum allowable temperature for each component which is consistent with the equipment reliability and the failure rate allotted to that component. Once these maximum allowable temperatures are assigned and the power dissipated by each component is ascertained, a heat flow network can be established from each component to available heat sinks or coolants for analysis of the system thermal performance. In situations where surface temperatures must be related to maximum allowable internal temperatures, such as junction temperatures of semiconductor devices, a knowledge of the internal thermal resistance of these components is required to calculate the corresponding surface temperatures for the particular operating conditions of the component.

A step by step procedure for evaluating thermal performance of proposed designs includes the following activities:

o Establish the maximum and minimum environmental temperatures of anticipated heat sinks and coolants.

o Characterize the available cooling techniques such as forced air convection, liquid or vaporization cooling.

o Develop a heat flow network using electrical analog techniques for the conditions of maximum allowable component temperatures and maximum environmental heat sink or coolant temperatures; determine the thermal resistance requirements from parts to heat sinks.

o Select packaging approaches and component placements that will fulfill the thermal resistance requirements in terms of the available and permissible cooling techniques.

o Determine the suitability of simple cooling techniques such as free or forced air cooling for satisfying the heat concentration and thermal resistance requirements of the proposed design. If insufficient, proceed to higher level cooling techniques until optimum cooling method is identified.

o Evaluate the penalties associated with the selected cooling method and perform trade-off analyses to identify alternative approaches and refinements if possible.

Further specifics of the parts stress thermal analysis and design techniques are described in NAVSEA 0967-LP-597-1011 Parts Application and Reliability Manual for Navy Electronic Equipment, October 1980.

Although each proposed system design requires a thermal performance analysis based on its specific characteristics, there are a number of general rule-of-thumb approaches associated with specific components that are beneficial for obtaining suitable thermal performance. Guidelines to achieve reliable design through temperature reduction of specific components are itemized in Table 6.1.3.1-2.

6.1.3.2 MECHANICAL PROTECTION

Protection against mechanical abuse environments is generally achievable by use of suitable packaging, mounting and structural techniques. The reliability impact of mechanical protection techniques is generally singular in that these measures do or do not afford the required protection against the identified mechanical abuse stresses. In most cases, trade-off situations between the level of protection and reliability improvements are not as pronounced as in the case of thermal protection. The one exception may be in the case of fatigue damage where the level of protection would have a significant impact on reliability if in fact fatigue was a primary failure mechanism in the normal life of the equipment.

Table 6.1.3.1-2: DESIGN GUIDELINES TO REDUCE COMPONENT OVERHEATING

Semiconductor Devices

a) Minimize thermal contact resistance between device and its mounting by using large area, smooth contacting surfaces and specifying thermal gaskets or compounds as required.

b) Locate remote from high temperature parts.

c) Use heat sinks with fins positioned vertically and in direction of air or coolant flow. Use painted or coated surfaces to improve radiation characteristics.

Capacitors

a) Locate remote from heat sources.

b) Insulate thermally from other heat sources.

Resistors

a) Locate for favorable convection.

b) Provide mechanical clamping or encapsulating material for improved heat transfer to heat sinks.

c) Use short leads whenever possible.

Transformers and Inductors

a) Provide heat conduction paths for transfer of heat from these devices.

b) Locate favorably for convection cooling

c) Provide cooling fins where appropriate.

Printed Wiring Boards

a) Specify larger area conductors where practicable.

b) Segregate heat producing elements from heat sensitive components.

c) Use intermediate metal core layers in multi layer systems and provide good conduction paths from these layers to support members and intermediate heat sinks.

d) Use protective coatings and encapsulants for improving heat transfer to lower temperature supports and heat sinks.

6.1.3.3 SHOCK AND VIBRATION PROTECTION

The environmental resistance required to protect against specified shock and vibration stresses is generally by an analysis which evaluates the deflections and mechanical stresses produced by these environmental factors. This generally involves the determination of natural frequencies and evaluation of the mechanical stresses within components and materials produced by the shock and vibration environment. If the mechanical stresses so produced are below the allowable safe working stress of the materials involved, no direct protection methods are required. If, on the other hand, the stresses exceed the safe levels, corrective measures such as stiffening, reduction of inertia and bending moment effects, and incorporation of further support members are required. If such approaches do not reduce the stresses below the safe levels, further reduction is usually possible by the use of shock absorbing mounts.

6.1.3.4 HUMIDITY, SALT AIR, SAND AND DUST PROTECTION

It is often mandatory to provide protection of the system elements against dust, dirt, contamination, humidity, salt spray and other mechanical abuse environments of this type. Although trade-off situations generally do not exist in terms of potential reliability improvements, this protection does significantly impact the operational and reliability levels of the equipment.

Possible protection methods against this class of environmental stresses include hermetic sealing, desiccants, and protective coatings. Hermetic sealing is often required when components such as solid state devices must be operated in a controlled atmosphere. The technical considerations involved in the selection of the hermetic seal system are its effects on the thermal performance of the system and its resistance to cracking during thermal shock conditions.

There are many insulating compounds that can be applied as coatings on electronic component assemblies. Among these are epoxies, silicones, polyurethanes, polystyrenes and varnishes. Generally, these are selected in accordance with MIL-I-46058 for military applications. Technical considerations for selection of suitable protective coatings are insulation resistance under the expected humidity and temperature conditions, dissipation factor, dielectric constant, mechanical flexibility, resistance to cracking during thermal shock, removal ease for repair work, ease of application, and its ability to prevent the migration of corrosion products.

6.1.3.5 RADIATION PROTECTION

Radiation protection generally must be specifically designed for the noise and interference fields against which protection is required. This usually involves the specification of shielding and filtering that are effective in the frequency range of concern.

Nuclear radiation protection generally consists of the use of specific components having an intrinsic hardness and the incorporation of shielding features that impact the required level of hardness to the system. Again, the provision of nuclear protection schemes is usually a go/no-go proposition since few trade-off situations are apparent.

6.1.4 GENERAL PACKAGING CONSIDERATIONS

The selection of a suitable packaging method for electronic equipment requires consideration of many trade-off factors in addition to the environmental protection factors described above. Characteristics that influence the choice of a packaging method include cost, size, producibility, maintainability, repairability and reliability. In many cases, the system requirements are conflicting, and the selection process becomes one of identifying a packaging approach offering the best compromise of the many divergent requirements.

In military electronic systems, size, weight, and reliability are prime considerations, and the choice of packaging materials must reflect the priority of these factors. System packaging approaches are generally concentrated on microelectronic packaging systems because of the size reduction and reliability benefits associated with semiconductor devices. Semiconductor integrated circuits not only offer reliability improvements because of their inherent properties but also because of the reduced number of interconnections that are needed. Further improvements result from the highly controlled fabrication processes and techniques utilized in the manufacture of such devices.

Table 6.1.4-1 illustrates a general ranking of trade-offs associated with electronic packaging techniques. For particular systems, these ranking factors will vary depending upon the specific requirements of the system. However, the general order of ranking is believed to be appropriate for a large population of systems, although large variations will occur.

TABLE 6.1.4-1: PACKAGING TRADE-OFFS

Type of Packaging	Characteristics					
	Size	Cost	Throw Away Cost	Reliability	Maintenance Repair	Logistics/ Spares
Soldered Modules on Boards	P	F	G	P	F	F
Welded Modules on Boards	P	P	F	P	F	F
Hybrid Modules (with integrated circuits)	F	P	F	F	F	F
Hybrid Compartmentalized	F	P	F	F	F	F
Etched Circuits	F	P	F	F	F	F
Pluggable Flat-Pack Modules	F	F	G	P	G	F
Flat-Pack Integrated Circuits Printed Wiring Board	G	G	G	F	G	G
Welded Flat-Pack IC Stack	G	P	P	F	P	F
Thin Film Circuits	G	G	F	F	P	F
IC Chips	G	G	P	G	P	P
Large-Scale Integration (LSI)	G	G	P	G	P	P
MOS Devices	G	G	P	G	P	P

G = Good
F = Fair
P = Poor

6.1.5 PRODUCTION ENVIRONMENTAL STRESS

A major contributor to reduced quality and reliability of components is the production environment. This affects semiconductor devices and integrated circuits to a large degree because the surfaces of these devices are sensitive to environments and there are many processing steps involved in their manufacture. The production environment can be further subdivided into the processing facility environment including chemical processing and the human factors involvement in device manufacture.

Overall control of the environment is critical to semiconductor processing since dust and dirt detract from the quality and reliability of semiconductor devices during physical and chemical processing steps of the wafer or chip prior to encapsulation. Airborne particles produce defects in semiconductor devices and integrated circuits. Temperature and humidity control are generally practiced within the overall production facility while dust control may be practiced on either an overall or a localized basis. Many prefer "white room" cleanliness where personnel are fitted with special clothing, hair and foot coverings. In other phases of device processing local controls are applied whereby all operations are done under positive pressure hoods in which tight environmental controls are maintained.

Chemicals used in semiconductor manufacture are highly refined products that exceed the purity requirements for reagent grade. "Electronic grade" chemicals having very low levels of particulate impurities affecting the electronic properties of processed devices are used in the manufacture of semiconductor devices. Perhaps the most important chemical used in semiconductor and integrated circuit production is water, which is characterized as deionized water.

While the physical and chemical environment can be controlled by proper monitoring of these influences, the control of human environmental influence on quality and reliability of devices is much more difficult. Six major steps are essential to the manufacture of semiconductor devices and circuits. These are: (1) basic design, (2) wafer or front end processing, (3) assembly, (4) packaging, (5) preconditioning and testing, and (6) failure analysis. Of the six steps, two are particularly vulnerable to the human interface (i.e., wafer or front end processing and assembly).

In the wafer processing phase the many steps requiring wafer handling subject this fragile element to potential damage. For example, physical damage may occur from tweezer handling in removal of wafers from diffusion furnace boats for subsequent photolithography or additional diffusion operations. In the assembly process the fragile wafer is subjected to potential handling damage in wafer die cutting which yields individual semiconductors or integrated circuits; wire and chip bonding are subject to the human error of the operator, and operator training and working stress can seriously affect the quality of the operation performed, which in turn affects the quality and reliability of the end product.

A major thrust by the semiconductor industry in the 1980's is the elimination of the human interface during the processing and manufacture of devices. This is to be accomplished by an increased use of automated wafer and assembly processing methods.

6.1.6 ELECTROSTATIC DISCHARGE CONTROL (ESD)

6.1.6.1 INTRODUCTION

When two substances, solid, liquid or gas make contact, no matter how gentle, their surfaces are crushed on the atomic level and electrons pass back and forth between them. On separation, one substance always becomes negatively charged and the other positively charged. The polarity of these charges depends to some degree on the relative position of the substances in the triboelectric series (DOD-HDBK-263). The magnitude of charge "Q" and the voltage level "V" that is developed are dependent primarily on the relative humidity, the composition and the conductivity of the charged substances. Nonconductive materials such as common plastics can easily build up static voltages in excess of 20,000 volts but with low values of "Q". Electrostatic charges can also be induced on sections of objects (e.g., polarization) due to the proximity of a charged object. This is due to the electrostatic force field emanating from a charged body.

Static is brought into work areas by people and generated during their normal movements. Clothing and articles of common plastic such as cigarette and candy wrappers, styrofoam cups, device trays and bins, tool handles, packaging containers, finished or waxed floors, work surfaces, chairs, processing machinery, and numerous other articles are prime sources of static charges. These electrostatic charges can be high enough to damage or cause the malfunction of electronic parts, assemblies and equipment during discharge to ground or to an object at a lower potential.

Usually, the smaller the part the more likely it is to be damaged by an electrostatic discharge (ESD). Certain parts are considered highly susceptible and their chances for damage are great. These include metal oxide semiconductor (MOS) parts with a direct access to the MOS junction, high frequency parts produced by the Schottky barrier process, many bipolar and field effect microcircuits like RAMs, ROMs and PROMs utilizing small active area junctions, thin dielectrics, metallization crossovers, and N+ guard ring structures, precision film resistors and similar parts. A detailed list of electrostatic discharge sensitive (ESDS) parts and their voltage sensitivity ranges are provided in DOD-STD-1686 and DOD-HDBK-263.

6.1.6.2 ESDS PART FAILURE TYPE, FAILURE MODES AND FAILURE MECHANISMS

6.1.6.2.1 INTERMITTENT (UPSET) FAILURE

ESD can cause intermittent or upset failures as well as hard or catastrophic failures of electronics. Intermittent or upset failures of digital parts and equipment are usually characterized by a loss of information or temporary distortion of functions. No apparent hardware damage occurs and proper operation resumes automatically after the ESD exposure.

Upset transients can be the result of an ESD spark in the vicinity of a part or equipment.

Parts which are very susceptible to ESD upset are any logic families that require small energies to switch states or small changes of voltage in high impedance lines. Examples of families that are sensitive would be NMOS, PMOS, CMOS, low power TTL and Schottky TTL. Linear circuits with high impedance and high gain inputs would also be highly susceptible along with RF amplifiers and other RF parts at the equipment level. These parts are very susceptible to erroneous signals generated by an ESD spark.

6.1.6.2.2 CATASTROPHIC (HARD) FAILURE

While upset failures occur when the equipment is in operation, catastrophic or hard failures can occur at any time. Such failures are characterized by the degradation of electrical parameters beyond specification limits. These hard failures can be the result of electrical overstress of parts caused by an ESD. Other failures may not be catastrophic but result in slight degradation of key electrical parameters such as increased leakage current, lower reverse breakdown voltages of P-N junctions or softening of the knee of the V-I curve of P-N junctions in the forward direction. Some ESDS part failures are more subtle and can remain latent until additional operating stress causes further degradation and ultimate catastrophic failure. For example, an ESD overstress can produce a dielectric breakdown of a self healing nature. When this occurs the part can retest good but contain a hole in the gate oxide. With use, metal will eventually migrate through the puncture, resulting in a direct short through this oxide layer.

6.1.6.3 FAILURE MODES AND MECHANISMS

ESD related failure mechanisms typically include:

o Thermal Secondary Breakdown (avalanche degradation) - For very small active area junctions (e.g., emitter-base junction of a transistor), thermal time constants of semiconductor materials are generally large compared with transient times associated with an ESD pulse. There is little diffusion of heat from the areas of power dissipation, and large temperature gradients can form in the parts, resulting in a localized junction melting.

The ESDS part types that commonly fail due to avalanche breakdown are:

(a) Discrete MOS Field Effect Transistors (FETs)
(b) Diodes (PN, PIN, Schottky)
(c) Bipolar transistors
(d) Junction Field Effect Transistors (JFETs)
(e) Thyristors
(f) Bipolar ICs, digital and linear
(g) Input protection circuits on MOS ICs

Some common failure modes for these parts include high leakage current between gate to source and gate to drain for JFETs, degradation of beta and soft reverse characteristics for bipolar transistors, and no output or latch up of outputs for digital and analog circuits.

protective measures such as stitton ... the stresses exceed the safe levels, comp

o Metallization Melt - Failures can also occur when ESD pulses increase part temperature sufficiently to melt metal or fuse bond wires. This can occur where the metal strips have reduced cross-sections as they cross oxide steps or on nonuniform areas resulting in localized current crowding and resultant hot spots in the metallizations.

ESDS part types sensitive to metallization failure are:

(a) Hybrid ICs
(b) Monolithic ICs
(c) Multiple Finger Overlay Switching and High Frequency Transistors

A common failure mode for metallization melt type failures is an open circuit on a metallization stripe.

o Dielectric Breakdown - When a potential difference is applied across a dielectric region in excess of the region's inherent breakdown characteristics, a puncture of the dielectric occurs. Depending on pulse energy, this can result in either total or limited degradation of the part.

ESDS part types utilizing MOS structures are most susceptible to dielectric breakdown. These are:

(a) MOS FET (Discrete)
(b) MOS ICs
(c) Semiconductors with metallization crossovers:
  Digital ICs
  Linear ICs
(d) MOS Capacitors:
  Hybrids
  Linear ICs

Typical failure mode for these part types is an electrical short (high leakage) between gate and drain or gate and source.

o Gaseous Arc Discharge - For parts with closely spaced, unpassivated, thin electrodes, gaseous arc discharge can cause degraded performance. The arc discharge condition causes melting and fusing of electrode metal.

The ESDS part types affected by this failure mechanism are:

(a) Surface Acoustic Wave (SAW) devices
(b) Thin metal unpassivated, unprotected semiconductors and microcircuits

o Surface Breakdown - For perpendicular junctions the surface breakdown is explained as a localized avalanche multiplication process caused by narrowing of the junction space charge layer at the surface. The destruction mechanism of surface breakdown results in a high leakage path around the junction, nullifying the junction. Another mode of surface failure is the occurrence of an arc around the insulating material. This phenomenon resembles metallization to metallization gaseous discharge, except in this case discharge is between metallization and semiconductor.

ESDS parts utilizing shallow junctions can be damaged as a result of surface breakdown.

o Bulk Breakdown - Bulk breakdown results from changes in junction parameters due to high local temperature within the junction area. This effect is usually preceded by thermal secondary breakdown.

The ESDS part types that commonly fail from thermal secondary breakdown are also candidates for bulk breakdown failure.

o Others - Film resistors (e.g., thick and thin film resistors of hybrid ICs, monolithic IC thin film resistors, encapsulated discrete film resistors) are noted to have failed as a result of dielectric breakdown, metallization or both. The failure is indicated by a shift in resistance, increase in degree of instability and change in temperature coefficient.

A different type of failure mechanism is noticed for crystal oscillators. Crystal fracture results from mechanical forces when excessive voltage is applied, as occurs during a high voltage ESD.

6.1.6.4 ESD SENSITIVITY TESTING (VZAP TESTS)

Although the subject is currently addressed by both DOD-STD-1686 and DOD-HDBK-263 the coverage is not yet adequate. Only the human ESD model is addressed. The charged device model and the field induced model are both totally ignored. A thorough treatment of the subject should treat each of these models. VZAP tests are presently required in some MIL-M-38510 detailed specification.

6.1.6.5 ESD PROTECTIVE MATERIALS AND EQUIPMENT

The protection of electronic ESD sensitive parts, assemblies and equipment can be provided through the implementation of low cost ESD controls, many of which have been used in the ordnance industry for decades. ESD sensitive parts are susceptible to damage during processing, assembly, inspection, handling, packaging, shipping, storage, testing, installation and maintenance throughout the equipment life cycle, both at the manufacturer's and user's facility. An effective ESD control program, therefore, will utilize the following protective materials and equipment to prevent such damage to ESD sensitive items.

(1) Wrist Straps. Wrist straps are the first line of defense in the battle against electrostatic discharge. The purpose of the wrist strap is to provide a permanent path to ground for the individual operator in order to prevent unsafe static charge levels from being generated during ordinary work related movements. The wrist strap provides prompt and effective removal of these charges. All ESD prevention programs should utilize wrist straps even if no other precautions are available.

(2) Protective Work Surfaces. The purpose of an ESD protective work surface or bench is to drain static charges out of an operator's general working area.

After wrist straps, protective work surfaces are the most important defense against ESD damage. There are a considerable number of different generic types of ESD protective work surfaces presently available with new ones coming on to the market continually. In selecting the most effective work surface for a given application, a number of factors, in addition to cost, must be considered. These factors include:

(a) Electrical conductivity
(b) Life, durability or wear resistance
(c) Chemical compatibility
(d) Surface hardness
(e) Operator comfort
(f) Grounding method

ESD protective materials are defined by DOD-HDBK-263 into three surface resistivity ranges as follows:

Conductive material = 10^5 ohms per square max

Static dissipative material = 10^5 to 10^9 ohms per square

Antistatic material = 10^9 to 10^{14} ohms per square

Static dissipative material is the optimum material for protective work surface use because it presents a compromise between being too conductive and being too resistive.

(3) Protective Packaging. ESD protective packaging encompasses an array of different items rather than a single entity. The various protective packaging items include:

(a) Protective bags
(b) Antistatic cushioned packing materials
(c) Conductive foams
(d) Conductive shunts or shorting plugs
(e) DIP sticks or magazines and IC carriers
(f) Tote boxes, bin and trays

An effective ESD control program should utilize all of these items in the battle against ESD.

To be completely effective, however, electrostatic protective packaging requires the application of three separate and distinct principles. These three principles are: a) equipotential bonding, b) the prevention of charge generation caused by triboelectric contact and separation, and c) protection from strong electrostatic fields by Faraday cage shielding.

o Equipotential Bonding. Bonding is the process of connecting two or more conductive objects together by means of a conductor. There is practically no potential difference between two metallic objects that are connected by a bond wire because the current through a bond wire is generally quite small. However, the situation may be different with an object

that is connected to ground. "Grounding (earthing)", is the process of connecting one or more objects to ground and is a specific form of bonding. An object that is connected to ground may, under heavy current flow, develop a high potential difference with respect to ground (E = I x R).

Thus, when all the terminals of an electronics device are bonded together (but not grounded) it is virtually immune to ESD. However, a bonded device that is charged might be subject to damage if suddenly grounded.

ESD sensitive devices are equipotential bonded by inserting the devices into conductive foam or a similar substance. Equipotential bonding of modules and printed circuit cards containing ESD sensitive parts is accomplished by the use of shorting plugs or conductive shunts on printed circuit card edge connectors to assure that during shipping and handling all of the circuitry on the card is maintained at the same potential.

o Triboelectric Charging. When any two materials are placed in intimate contact and then separated a triboelectric charge is generated. The magnitude of this charge is a function of the relative separation between the two materials in the triboelectric series (Table 6.1.6.5-1). The triboelectric series also establishes which material will become positively charged and which material will become negatively charged. Another way of visualizing static electrification via a triboelectric series chart is that it is a listing of materials by their relative electron densities. As long as there is a difference in electron density, charges will be transferred at each encounter. Triboelectric charging can be reduced in three ways. First, by the proper selection of packing material, i.e., those materials which are not too widely separated on the triboelectric series form the external material of the item to be protected. The second method is by the use of packing materials with sufficient conductivity to allow any such charges to be quickly bled away and dissipated before they can build up to damaging levels. The third method is by the introduction of a lubricant or other surface contamination between the materials to reduce the intimacy of their contact. Antistats in particular, when deposited on the surface of a material, act in such a way as to prevent charge generation.

o Faraday Cage Shielding. Charges placed on an insulated hollow conductive object reside entirely on its outer surface. Because of this no charge is apparent inside the conductive object. Michael Faraday carried out experiments to prove this. He built a large metal covered box which he mounted on insulating supports and charged with a powerful electrostatic generator. Faraday wrote of his experiment: "I went into the cube and lived in it, and using lighted candles, electrometers, and other tests of electrical states, I could not find the least influence upon them...though all the time the outside of the cube was very powerfully charged, and large sparks and brushes were darting off from every part of its outer surface."

It is this behavior that enables conductive bags to protect ESD sensitive devices from external charges and electrostatic fields. More importantly it illustrates the need to have devices enclosed in a conductive enclosure to be protected.

TABLE 6.1.6.5-1: SAMPLE TRIBOELECTRIC SERIES

Positive +	Air Human Hands Asbestos Rabbit Fur Glass Mica Human Hair Nylon Wool Fur Lead Silk Aluminum Paper Cotton Steel Wood Amber Sealing Wax Hard Rubber Nickel, Copper Brass, Silver Gold, Platinum Sulfur Acetate Rayon Polyester Polyethylene Polypropylene PVC (Vinyl) KEL F Silicon
Negative -	Teflon

o Higher Assembly Considerations. Assembly of an ESD sensitive device into a higher level assembly does not render it insensitive. Because of their greater electrical capacitance, printed circuit boards (PCB) can store much more charge than the device itself.

In some cases, then, the device is more vulnerable to ESD damage when it is installed on a PCB than the device would be itself. In additon, the circuit paths themselves on the PCB can act as antennae and intensify the potential to which the device is subjected when the PCB is exposed to an electrostatic field. Thus, the same or comparable precautions must be taken with higher level assemblies. For example, PCB's containing ESD sensitive parts must be handled as ESD sensitive assemblies, and finished products containing ESD sensitive parts should be shipped with shorting plugs attached to protect the sensitive circuits therein.

Each of the three principles; equipotential bonding, prevention of triboelectric charging and Faraday cage shielding, apply individually and they cannot be interchanged one for another. Unfortunately, no single package scheme incorporates all three principles. Therefore, the proper ESD packaging will usually be a two or three step process in order to incorporate all three principles.

o Air Ionizers. Wrist straps and protective work surfaces are effective in eliminating electrostatic charges on conductive items. Wrist straps and protective work surfaces are not, however, effective in eliminating electrostatic charges on nonconductive items such as clothing and nonconductive tote trays. Air ionizers can neutralize static charges on nonconductive items by supplying them with a constant stream of both positive and negative air ions. The charged object attracts the oppositely charged ions, thereby neutralizing itself in situ. The unused ions or those having the same sign as the charged surface are repelled and eventually recombined with other ions or are themselves neutralized by contact with grounded conductive surfaces.

o Electrostatic Detectors, Voltmeters and Monitors. Electrostatic detectors are used to determine the presence or absence of electrostatic charges in the work area. They may be used to determine the polarity and the relative magnitude of the charge. They are not, however, designed to make accurate measurements of electrostatic charges or measure the decay rate of electrostatic charges. These types of measurements require the use of the more elaborate laboratory grade electrostatic voltmeters. A third class of instruments, electrostatic monitors, are used for the continuous automatic surveillance of excessive electrostatic potentials in the work area. They are used to record the event, notify the operator and/or actuate ancillary equipments such as air ionizers.

o Conductive Floors, Floor Mats and Footwear. Conductive floor, floor mats and footwear are a rather specialized form of ESD protection. Although they may not be required in every instance, they do fulfill a definite role in the arsenal of ESD protective weapons. Their primary

role is in those areas where, for whatever the reason, it is not possible to employ all of the previously discussed ESD protective tools. For example, wrist straps may not be used near moving conveyor belts and in wave solder operations. In this type of application conductive floors or floor mats and conductive footwear should be utilized.

Conductive floor or floor mats alone, without conductive footwear, are of limited use in providing ESD protection. The conductivity of normal footwear varies greatly depending upon materials and construction. High quality leather soled shoes may well provide adequate conductivity with the floor; however, manmade shoe materials seldom provide adequate conductivity. Therefore, it is essential that heel straps or similar means be used to provide conductivity between the operator and the conductive floor or floor mat.

Chairs and stools used in conjunction with conductive floors should also be conductive, both the legs which make contact with the floor and the seat surface itself, to assure that the operator remains properly grounded even with his or her feet off of the floor.

For operator safety, as with the protective work surfaces and wrist straps, conductive floors and floor mats must be grounded through a current limiting resistor of between 250K ohms and 1 megohm.

o Garments/Clothing. Usually specific garments or clothing are not specified for ESD control, however, some exceptions do exist. Shop or lab coats and smocks are probably the most important example. Where these type of garments are required to be worn it is essential the ESD protection also be considered.

o Topical Antistats. Topical antistats may also be a powerful weapon in the battle against ESD. They function in two different ways. First, they reduce the materials' coefficient of friction by increasing surface lubricity. This tends to reduce the maximum potential charge that can be generated in a frictional or triboelectric situation. Secondly, they increase surface conductivity, thus allowing any charges to be bled off and dissipated more rapidly.

Topical antistats are typically used in applications such as:

(a) Cleaning of work surfaces and floors
(b) Surface treatment of items which are not amenable to other ESD control techniques, such as the exposed common plastic surfaces of CRT displays, computer terminals and other equipment found in the work area.

6.1.6.5.1 SUMMARY

"Caveat emptor", let the buyer beware, is especially germane to the purchase of ESD protective materials. For maximum quality assurance, substantial purchases should be made only after a thorough review of the market, the implementation of a formal product qualification program, and lot sample testing to assure consistent quality.

used as deionized water

6.1.6.6 DESIGN PRECAUTIONS FOR ESD

o Built-In Protective Networks. Various protection networks have been developed to protect sensitive MOS but not for bipolar devices. These circuit protection networks provide limited protection against ESD. Many of the protection networks designed into MOS devices reduce the susceptibility to ESD to a maximum of 800 volts. MIL-M-38510 V-ZAP test voltages for CMOS, for example, vary from 150 to 800 volts. Protection circuitry of some devices is improving and protection to 4,000 volts appears to be achievable for some MOS devices. However, electrostatic potentials of tens of thousands of volts can be generated in uncontrolled environments.

The protection afforded by specific protection circuitry is limited to a maximum voltage and a minimum pulse width. ESDS beyond these limits can subject the part's constituents to damage or damage the protection circuitry constituents themselves which are also often made of moderately or marginally sensitive parts. Damage to the protection circuitry constituents could result in degradation in part performance or make the ESDS part more susceptible to subsequent ESDS. The degradation, for example, could be a change in speed characteristics of the ESDS part or an increase in leakage current of the ESDS part. Multiple ESDS at voltages below the single ESD pulse sensitivity voltage or energy level can also weaken or cause failure of the part performance or protection circuitry constituents resulting in degradation or failure of the ESDS parts. Loss of protective circuitry may not be apparent after an ESD.

In summary, protection networks reduce but do not eliminate the susceptibility of a part to ESD. This reduction in ESD sensitivity, however, results in a lower incidence of ESD part failure.

The sensitivity of the same type of ESDS part can vary from manufacturer to manufacturer. Similarly, the design and the effectiveness of protection circuitry also varies from manufacturer to manufacturer.

o Specific Design Precautions. Various design techniques have been employed in reducing the susceptibility of parts and assemblies to ESD. Diffused resistors and limiting resistors provide some protection, but are limited in the amount of voltage they can handle. Zeners require greater than 5 nanoseconds to switch and may not be fast enough to protect an MOS gate. Furthermore, Zener schemes, diffused resistors and limiting resistors reduce the performance characteristics of the part which in many instances are the primary considerations for which that part was designed.

Additional assembly level design precautionary procedures would include:

(a) Latchup in CMOS, with the exception of analog switches, can be avoided by limiting output current. One solution is to isolate each output from its cable line with a resistor and clamp the lines to V_{DD} and V_{SS} with two high speed switching diodes. The use of long input cables poses the possibility of noise pickup. In such cases filter networks should be used.

(b) Additional protection can be obtained for MOS by adding external series resistors to each input.

(c) Where practicable, an RC network consisting of a relatively large value resistor and a capacitor of at least 100 pF should be used for sensitive inputs on bipolar parts to reduce effects from ESD. However, if circuit performance dictates, two parallel diodes clamping to a half volt in either polarity can be used to shunt the input to ground. This reduces disturbances to the input characteristics.

(d) Leads of sensitive parts mounted on PCBs should not be connected directly to connector terminals without series resistance, shunts, clamps or other protective means. Assembly designs containing ESDS items should be reviewed for incorporation of protective circuitry.

(e) Systems incorporating keyboards, control panels, manual controls, or key locks should be designed to dissipate personnel static charges directly to chassis ground, bypassing ESDS parts.

6.1.6.7 ESD CONTROL PROGRAM

Based upon the problems caused by the lack of uniform and complete ESD controls, the Naval Sea Systems Command (NAVSEA), Department of the Navy, for the Department of Defense (DOD) has prepared DOD-STD-1686 to define the requirements for a standardized ESD control program. The intent of DOD-STD-1686 is to provide minimum requirements needed to provide an effective ESD control program.

DOD-STD-1686 contains the following basic requirements:

(a) ESDS item identification and classification
(b) ESD design protection
(c) ESD protected areas
(d) ESD handling procedures
(e) ESD protective covering
(f) ESDS equipment installation site
(g) ESD training
(h) ESD marking on documentation
(i) ESD marking on hardware
(j) Quality assurance provisions, audits and reviews
(k) ESD packaging for delivery

DOD-HDBK-263 has also been prepared to provide guidance for establishing, implementing and monitoring elements of the DOD-STD-1686 ESD control program. This handbook includes guidance in: the identification of causes and effects of ESD on electronic parts, assemblies, and equipment; establishing and implementing ESD program controls; selection and application considerations for ESD protective materials and equipment; design and construction of ESD protected areas; design of protection networks; the preparation of ESD handling, packaging, and marking procedures; development of ESD personnel training programs; certification of ESD protected areas and monitoring of ESD control program requirements.

6.1.6.8 SOURCE MATERIAL

Publications dealing with the problems caused by electrical overstress/electrostatic discharge (EOS/ESD) and the means commonly employed to resolve them are available from the Reliability Analysis Center, RADC/RBRAC, Griffiss AFB, NY 13441. These publications include the Proceedings of the annual EOS/ESD Symposium (beginning with the first symposium held in 1979) and a bibliography of technical reports, talks and papers produced in the subject area since 1969.

REFERENCES

1. NAVSEA 0967-LP-597-1011 Parts Application and Reliability Manual for Navy Electronic Equipment, October 1980.

2. Anderson, R.T., et al. "Reliability Design Handbook," IIT Research Institute, March 1976.

3. DOD-STD-1686, "Electrostatic Discharge Control Program for Protection of Electrical and Electronic Parts, Assemblies and Equipment (Excluding Electrically Initiated Explosive Devices)," "METRIC."

4. DOD-HDBK-263, "Electrostatic Discharge Handbook for Protection of Electrical and Electronic Parts, Assemblies and Equipment (Excluding Electrically Initiated Explosive Devices)," "METRIC."

6.2 DESIGN GUIDELINES FOR RELIABLE CIRCUITS

6.2.1 ELECTRICAL DERATING

The guidelines in the preceding section on parts selection and control assume that the parts are inherently reliable and capable of withstanding the stresses to which they will be subjected.

Additional improvement in part and, ultimately, equipment reliability can be realized by applying the techniques of derating. Derating can be defined as the operation of a part at less severe stresses than those for which it is rated. In practice, derating can be accomplished by either reducing stresses or by increasing the strength of the part. Selecting a part of greater strength is usually the most practical approach.

Derating is effective because the failure rate of most parts tends to decrease as the applied stress levels are decreased below the rated value. The reverse is also true: the failure rate increases when a part is subjected to higher stresses and temperature. The failure rate model of most parts is stress and temperature dependent. This dependence is discussed more fully in the subsection following:

o Temperature-Stress Factors. The temperature-stress effect can best be observed by studying MIL-HDBK-217 failure rate models. For example, the parts failure model for discrete semiconductors is expressed as follows:

$$\lambda_p = \lambda_b(\pi_E \times \pi_A \times \pi_{S2} \times \pi_C \times \pi_Q \times \pi_R)$$

where

λ_p is the part failure rate

λ_b is the base failure rate

π_E environment--accounts for influence of environmental factors other than temperature

π_A application--accounts for effect of application in terms of circuit function

π_{S2} voltage stress--adjusts model for a second electrical stress (application voltage) in addition to wattage included within

π_C complexity--accounts for effect of multiple devices in a single package

π_Q quality--accounts for effects of different quality levels

π_R rating--accounts for effect of maximum power and current rating

development of ... semiconductors, resistors, and capacitors which

The equation for the base failure rate, λ_b, is:

$$\lambda_b = A \exp\left[\frac{N_T}{273 + T + (\Delta T)S}\right] \quad \exp\left[\frac{273 + T + (\Delta T)S}{T_M}\right]^P$$

where

A is a failure rate scaling factor

N_T, T_M and P are shaping parameters

T is the operating temperature in degrees C, ambient or case, as applicable.

ΔT is the difference between maximum allowable temperature with no junction current or power (total derating) and the maximum allowable temperature with full rated junction current or power.

S is the stress ratio of operating electrical stress to rated electrical stress.

The values for the shaping parameters and constraints shown in Table 6.2.1-1 and the resulting base failure rate (λ_b) for an Si, NPN transistor shown in Table 6.2.1-2 are taken from MIL-HDBK-217. Figure 6.2.1-1 is derived from Table 6.2.1-2. It is evident that the only variables of the equation for the base failure rate (λ_b) are T, the operating temperature, ΔT, the difference between maximum temperatures in de-energized and energized state and S, the electrical stress ratio.

Table 6.2.1-2 and Figure 6.2.1-1 show how λ_b varies with temperature and stress. The data presented is based on the typical maximum junction temperature of 175°C (fully derated) and 25°C for the maximum temperature at which full rated operation is permitted.

TABLE 6.2.1-1: DISCRETE SEMICONDUCTOR BASE FAILURE RATE PARAMETERS

Group	Part Type	λ_b Constants				
		A	N_T	T_M	P	ΔT
Transistors						
I	Si, NPN	0.13	-1052	448	10.5	150
	Si, PNP	0.45	-1324	448	14.2	150
	Ge, PNP	6.5	-2142	373	20.8	75
	Ge, NPN	21.	-2221	373	19.0	75
II	FET	0.52	-1162	448	13.8	150
III	Unijunction	3.12	-1779	448	13.8	150
Diodes						
IV	Si, Gen. Purp.	0.9	-2138	448	17.7	150
	Ge, Gen. Purp.	126	-3568	373	22.5	75
V	Zener/Avalanche	0.04	-800	448	14	150
VI	Thyristors	0.82	-2050	448	9.6	150
VII	Microwave					
	Ge, Detectors	0.33	-477	343	15.6	45
	Si, Detectors	0.14	-392	423	16.6	125
	Si, Schottky Det.	0.005	-392	423	16.6	125
	Ge, Mixers	0.56	-477	343	15.6	45
	Si, Mixers	0.19	-394	423	15.6	125
VIII	IMPATT, Gunn, Varactor, PIN, Step Recovery & Tunnel	.93	-1162	448	13.8	150
Transistors IX	Microwave	(Section 2.2.9 of MIL-HDBK-217C)				
X Opto-Electronic	LED's, Isolators and Displays	126	-3734	398	22.5	100

lation shall not be used in airborne applications

TABLE 6.2.1-2: BASE FAILURE RATES FOR GROUP I TRANSISTORS (SILICON, NPN)

T (°C)	S 0.1	0.2	0.3	0.4	0.5	0.6	0.7	0.8	0.9	1.0
0	0.0034	0.0041	0.0048	0.0057	0.0067	0.0079	0.0096	0.011	0.014	0.018
10	0.0038	0.0044	0.0054	0.0064	0.0075	0.0089	0.010	0.013	0.017	0.023
20	0.0043	0.0051	0.0060	0.0071	0.0084	0.010	0.012	0.015	0.020	0.029
25	0.0046	0.0054	0.0064	0.0075	0.0089	0.010	0.013	0.017	0.023	0.033
30	0.0049	0.0057	0.0067	0.0079	0.0095	0.011	0.014	0.018	0.025	
40	0.0054	0.0064	0.0075	0.0089	0.010	0.013	0.017	0.023	0.033	
50	0.0060	0.0071	0.0084	0.010	0.012	0.015	0.020	0.029		
55	0.0064	0.0075	0.0089	0.010	0.013	0.017	0.023	0.033		
60	0.0067	0.0079	0.0095	0.011	0.014	0.018	0.025			
65	0.0071	0.0084	0.010	0.012	0.015	0.020	0.029			
70	0.0075	0.0089	0.010	0.013	0.017	0.023	0.033			
75	0.0079	0.0095	0.011	0.014	0.018	0.025				
80	0.0084	0.010	0.012	0.015	0.020	0.029				
85	0.0089	0.010	0.013	0.017	0.023	0.033				
90	0.0095	0.011	0.014	0.018	0.025					
95	0.010	0.012	0.015	0.020	0.029					
100	0.010	0.013	0.017	0.023	0.033					
105	0.011	0.014	0.018	0.025						
110	0.012	0.015	0.020	0.029						
115	0.013	0.017	0.023	0.033						
120	0.014	0.018	0.025							
125	0.015	0.020	0.029							
130	0.017	0.023	0.033							
135	0.018	0.025								
140	0.020	0.029								
145	0.023	0.033								
150	0.025									
155	0.029									
160	0.033									

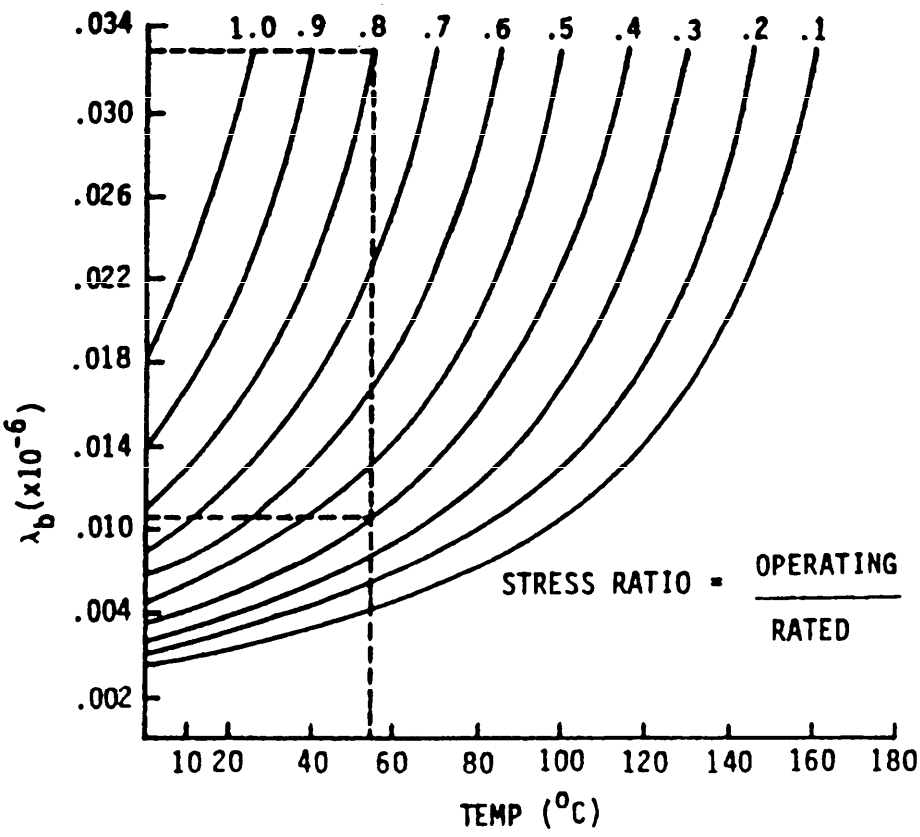


FIGURE 6.2.1-1: STRESS/TEMPERATURE PLOT FOR GROUP I TRANSISTORS (SILICON, NPN)

The data show that at higher temperatures (≥100°C) and at electrical stress higher than 40% (even at lower temperatures) the slopes of the curves (and the failure rate) increase drastically.

Since semiconductors as well as most electronic parts are sensitive to temperature, the thermal analysis of any design should accurately provide the ambient temperatures needed for proper application of the part. Of course, lower temperatures produce better reliability but can also produce increased penalties in terms of added loads (or constraints) on controlling the system's environment. Thermal analysis should be part of the design process and included in all the trade-off studies covering equipment performance, reliability, weight, volume, environmental control requirements, and, above all, cost.

Derating procedures vary with different types of parts and their application. Resistors are derated by decreasing the ratio of operating power to rated power. Capacitors are derated by maintaining the applied voltage at a lower value than the voltage for which the part is rated. Semiconductors are derated by keeping the power dissipation below the rated level.

The first step in the procedure for derating electronic parts involves the use of derating curves, which usually relate derating levels to some critical environmental or physical factor. Such curves are typically included in the part specification. A typical derating curve for semiconductors is shown in Figure 6.2.1-2.

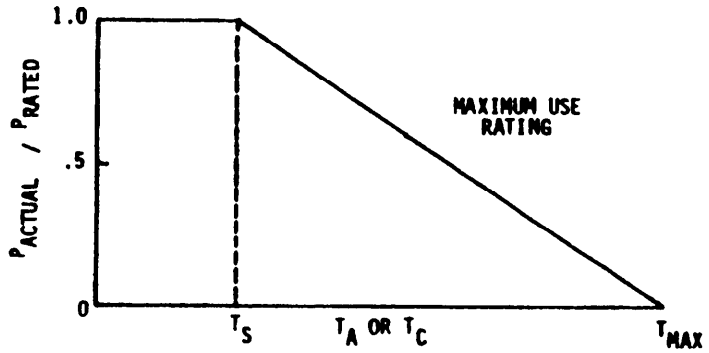


FIGURE 6.2.1-2: TYPICAL DERATING GRAPH

In Figure 6.2.1-2,

T_S is the temperature derating point (usually 25°C)

T_{MAX} is the maximum junction temperature

T_A is the ambient temperature

T_C is the case temperature

Maximum junction temperature (T_{MAX}) is normally 175°C for silicon and 100°C for germanium devices. Although usually 25°C, T_S can be other values of temperature.

This conventional derating approach makes the approximate assumption that the thermal resistance, from ambient or case to junction is a constant and that the junction temperature is:

$$T_J = T_A + \theta_{JA}P_J$$

or

$$T_J = T_C + \theta_{JC}P_J$$

where

T_J is junction temperature

T_A is ambient temperature

T_C is case temperature

θ_{JA} is thermal resistance (ambient to junction, °C per watt)

θ_{JC} is thermal resistance (case to junction, °C per watt)

P_J is power (watts) dissipated at junction.

These equations indicate that operation anywhere along the derating line between T_S and T_{MAX} will result in a junction temperature equal to T_{MAX} and that the thermal resistance (θ) is constant at a value:

$$\theta = \frac{T_{MAX} - T_S}{P_{(rating)}} \quad {}^{o}C/watt$$

where

$P_{(rating)}$ is power rating (watts at temperature T_S).

This assumption of constant thermal resistance is approximate. For many common transistors, the assumption is close and conservative because their actual thermal resistance has only a slightly negative slope as a function of the temperature of the bulk semiconductor material. An actual curve of constant junction temperature for these devices resembles Figure 6.2.1-3.

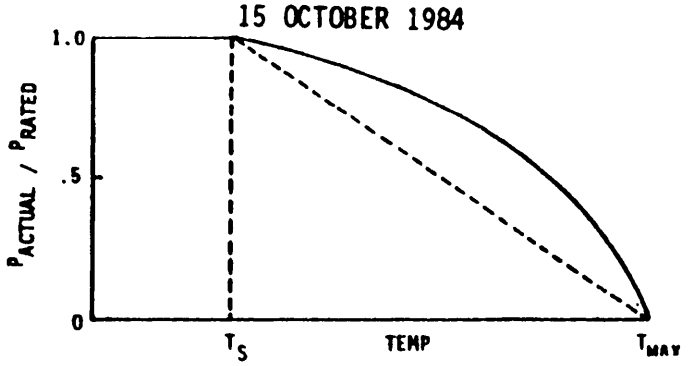


FIGURE 6.2.1-3: ACTUAL CONSTANT JUNCTION TEMPERATURE CURVE

As shown in Figure 6.2.1-3, if the curvature of T_J - T_{MAX} curve is large, then the assumption of the dotted straight line can lead to appreciable error. The fact that the curvature of T_J = T_{MAX} can be different for the two cases of referencing θ_{JA} or θ_{JC} is one reason why differences may be obtained in using these two ratings in prediction computations.

This assumption error may be very large for some devices. This is recognized by suppliers who specify a multipoint derating curve to approximate more closely the extreme curvature in the constant T_S - T_{MAX} curve. An example is the derating curve for the 1N3263 power diode, Figure 6.2.1-4, where the three rating points are 160 amps at 125°C, 120 amps at 150°C, 0 amps at 175°C. As shown in Figure 6.2.1-4, the two point linear derating assumption from 160 amps 125°C would have resulted in an 80 amps rating at 150°C instead of the actual rating of 120 amps. This would have caused a third or more of the device capability to be wasted at 150°C.

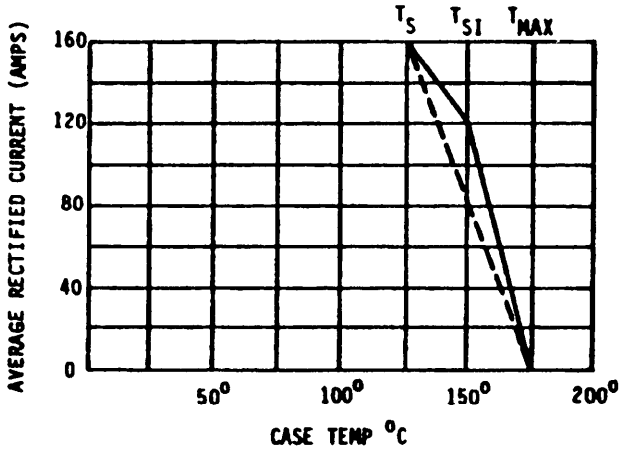


FIGURE 6.2.1-4: MULTIPOINT DERATING CURVE FOR 1N3263 POWER DIODE

Occasionally in military specifications, the derating instructions are presented as notes relative to the maximum ratings. The slash sheets appended to MIL-S-19500 contain numerous examples of derating instructions for discrete semiconductor devices.

contacts (see figure 5.7.8.2.1) connector c

o Specific Derating Guidelines. Section 5.2 of the Handbook provides specific guidelines for derating component parts used in electronic equipment. These guidelines represent a composite summary of derating policies employed presently by firms within the electronics industry who specialize in military applications.

As a general rule, specific derating guidelines should not be conservative to the point where costs rise excessively (e.g., higher than necessary part rating are selected). Neither should the derating criteria be so loose as to render reliable part application ineffective. Optimum derating occurs at or below the point on the stress/temperature curve where a rapid increase in failure rate is noted for a small increase in temperature or stress. This may be visualized by referring back to Figure 1 (when considering a silicon NPN transistor).

Consider that the transistor is used at 55°C ambient temperature rated for 500 mW at 25°C and sees two different stress levels: 400 mW = 80% and 200 mW = 40%. Referring to Figure 6.2.1-1, at a stress of 80% and a temperature of 55°C, the failure λ_b is 0.033 x 10^{-6}. It can also be seen that 80% stress or 400 mW is the maximum allowable power dissipation at 55°C for this transistor. If, however, the transistor is stressed only 40% at 55°C, the failure rate λ_b decreases drastically to 0.010 x 10^{-6}. A reliability improvement of 3.3 to 1 has been achieved.

6.2.2 THERMAL DESIGN

The development of new electronic equipments offering improved sophistication, versatility and expanded capabilities has resulted in rapid and continued increases in the role of electronics in all phases of military/defense organizations. The need for improved capabilities are limited by a number of system constraints including size, weight, power, etc. A large number of these constraints may be met simply by reducing the size of the equipment. As a result, many innovative packaging techniques have been developed which increase the "density" of the components. Unfortunately, these size reductions are often implemented with little or no regard for the thermal requirements of the system. All too often, thermal design is evaluated only after a thermal problem is identified. Proper thermal design is only achieved by implementation of a thermal design program which parallels the electrical design of the equipment, from inception through production and retrofit. As with any program, successful management of a thermal design effort requires investigation of the alternatives, optimization of the design consistent with specific goals, and a means of monitoring to insure that proper rules and procedures are adhered to.

The following discussion will review the basics of heat transfer, discuss thermal impact on system performance, and consider the requirements for effective management of thermal designs.

6.2.2.1 RELIABILITY IMPLICATIONS OF TEMPERATURE

Before discussing the theory and implementation of thermal control systems, a summary of the various ways in which temperature can influence the reliability of an electrical or electronic device follows.

Thermal energy, quantified as temperature, may be directly linked to a number of physical and/or chemical processes which are generally detrimental to the reliability and/or performance of electrical devices and equipment. These processes may be loosely grouped into two categories: thermally dependent phenomena and thermally induced phenomena. Thermally induced phenomena may be further categorized as being attributed to static or dynamic thermal stresses.

Failure mechanisms attributable to static thermal stresses usually involve a threshold temperature which must be exceeded before any detrimental effects occur. One common example of this is a change of state (i.e., melting). These types of failures, when they occur, are usually considered to be due to overstress. It is the responsibility of the thermal designer to insure that no part ever be subjected to temperature in excess of the maximum rated temperature for that part, even under worst case conditions. Organic materials are often vulnerable to thermal overstress due to their relatively low glass transition temperatures.

Another common type of device failure mechanism attributable to static thermal stress results from the mismatch of thermal expansion coefficients of interfacing materials. In such conditions, the mechanical stress or strain at the interface will be a function of the temperature and the difference in the thermal expansion coefficients of the materials involved. When the force due to thermal mismatch exceeds the strength of bonding material at the interface, a failure will occur. Common examples of failures of this type are microcircuit chip bond failures, package seal failures in ceramic dual-in-line packages (DIPs), and copper delamination on printed circuit boards.

Dynamic thermal stress, or temperature cycling, produces failures at a rate dependent on the number of temperature cycles as well as on the range over which the temperature is cycled. When the rate of change of temperature is relatively slow (the typical case), temperature cycling induced defects are usually attributed either to work hardening of the material (due to repeated expansion/contraction cycles) or to the cumulative effects of mass transport due to repeated occurrence of cycles extending to temperature high enough to result in plastic flow. Work hardening effects are often observed in microcircuit wirebonds. Work hardening of the aluminum wires tends to make them brittle and susceptible to cracking.

Voiding of chip bonds in microcircuits is a typical example of the net transport of mass due to temperature cycling effects. This occurs when the temperature during a particular cycle stresses to the bonding material in excess of the elastic limit of the material. (The stress is

a result of thermal expansion mismatch between the chip and the substrate.) The temperature need not be high enough to cause a failure, only just high enough to result in plastic flow of the bonding material. The net mass transport occurring during one temperature cycle is usually insignificant. However, the effects are cumulative. Furthermore, since in most microcircuits the primary means of conducting heat away from the chip itself is through the chip bond, the progressive voiding of the bonding material increases the thermal resistance, which results in still higher temperatures, which again results in further voiding. The end result is usually a failure, although the cause of the failure is not always correctly identified.

When the rate of change of temperature is very fast, as in thermal shock tests, failures are usually catastrophic and appear as cracks or breaks in the material. Thermal shock places severe stress on any material having a relatively large thermal coefficient of expansion. With rapid temperature changes, one end of the material may be at the maximum temperature of the cycle while the other end is still at the minimum temperature. As a result, even homogeneous materials may fail under such severe conditions. Thermal shock is typically used in component test labs as an accelerated test intended to simulate the long term effects of temperature cycling. The extrapolation of thermal shock test results back to thermal cycling conditions is a controversial procedure. Fortunately the occurrence of thermal shock conditions in actual equipment is rare.

Examples of temperature dependent failure mechanisms include solid state diffusion and most chemical reactions. Typical examples of these are the formation of intermetallics (such as purple plague) and corrosion of metals, respectively. For such failure mechanisms, the effects of thermal energy are cumulative with time, that is, a function of the time temperature integral. In theory, such mechanisms occur continuously (except at zero Kelvin). Temperature merely influences the rate at which the mechanisms proceed. For a large number of these mechanisms, the thermal dependence has been shown to be adequately predicted by the Arrhenius model;

$$\lambda = A \exp\left[\frac{E_a}{kT}\right],$$

where A is a normalization constant, k is Boltzmann's Constant (8.63×10^{-5} eV/^{o}K), T is the temperature in degrees Kelvin, and E_a is the activation energy of the specific mechanism in question (in electron volts).

Failure mechanisms for microcircuits range from below 0.1eV to above 1.1eV, with many of the common mechanisms exhibiting activation energies of about 0.7eV. Quantitatively, a mechanism having an activation energy of 0.7eV will, at 50^{o}C, proceed at a rate over eight times the rate at 25^{o}C. To look at it another way, the probability of survival of a component having a failure mechanism of activation energy 0.7eV is eight times better at 25^{o}C than at 50^{o}C. Clearly the potential reliability improvements to be gained through thermal controls justify their development and implementation.

6.2.2.2 HEAT AND HEAT TRANSFER THEORY

Since electrical components are never 100% efficient, the generation of thermal energy is an inherent by-product of electrical circuits and equipments. The difference between the input power and the output power of a device is due to the amount of heat dissipated by the device per unit time.

One technique for reducing the thermal problems in a system involves minimizing the heat generated. This is usually accomplished by judicious component selection and the use of efficient circuit designs. One common example of this might be the switching power supply. For high power applications a transistor operates much more efficiently as a switch than in the linear mode. By capitalizing on this fact, switching supplies operate at considerably greater efficiencies and thus develop less thermal energy than their linear counterparts.

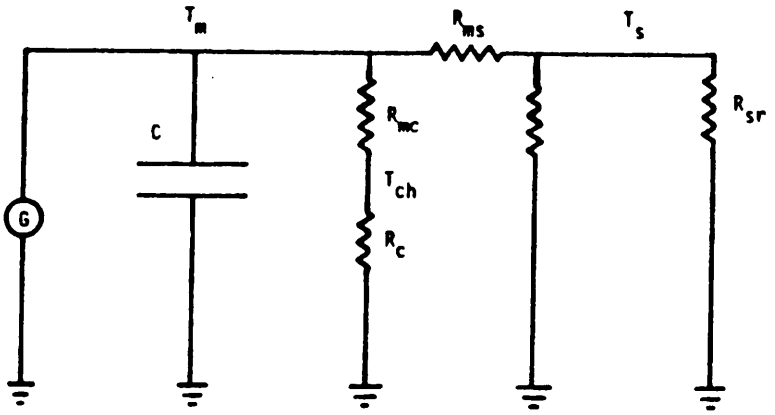
Unfortunately, optimization of circuit design is seldom adequate to eliminate all thermal problems. In most instances it is necessary to transfer the heat away from the source and dissipate it into some thermal sink.

o Conduction - Heat conduction is considered to be effected through molecular oscillations in solids and elastic impact in liquids and gases. When heat is transferred by conduction the heat flow relationships are analogous to Ohm's law for electrical current flow; that is, the rate of heat transferred is analogous to current flow, the temperature differences are analogous to voltage drops, and the thermal resistance to heat transfer is analogous to electrical resistance.

o Convection - The process of heat transfer from the surface of a solid to moving masses of fluids, either gaseous or liquid, is known as convection. This mode of heat transfer is brought about through circulation of the fluid.

o Radiation - All bodies continuously emit thermal radiation in the form of electromagnetic waves, ranging in wavelength from the long infrared to the short ultraviolet. Radiation emitted from a body can travel undiminished through a vacuum or through gases with relatively little absorption. When radiation is intercepted by a second body, part may be absorbed as thermal energy, part may be reflected from the surface and part may be transmitted, still in electromagnetic wave form, through the body as in the case of glass.

Based on the above discussion an equivalent thermal circuit for a discrete electronic part is presented in Figure 6.2.2.2-1.



G = constant current generator with Q internal heat dissipation
C = thermal capacity of the part
R_{mc} = thermal resistance, material to chassis
R_c = thermal resistance, chassis to heat sink
R_{ms} = thermal resistance, heat source to surface
R_{sc} = thermal resistance due to convective cooling
R_{sr} = thermal resistance due to radiation
T_m = temperature of the material
T_{ch} = temperature of the chassis
T_s = temperature of the surface
T_e = environmental temperature

FIGURE 6.2.2.2-1: EQUIVALENT THERMAL CIRCUIT OF A PART

Thermal controls in a circuit are usually achieved by minimizing the resistance in one or more of the "resistive" paths to thermal ground. This may be accomplished by any of several means, including the provision of thermal paths to ground with high thermal conductance, maximizing heat transfer at interfaces by use of polished surfaces, thermal grease, etc., and minimizing the number of thermal interfaces.

Most thermal designs are based on optimization of one of the three basic heat transfer techniques (radiative, convective, conductive). A summary of commonly used techniques follows.

Conduction cooling is capable of handling all but the most severe thermal design problems. A very low thermal impedance path is provided from the heat source to an appropriate thermal reservoir. Thermal resistance of the conductive paths may be closely controlled by appropriate material selection. Since thermal conductivity is a bulk material property, it is relatively immune to degradation, unlike convective and radiative techniques which are strongly dependent on the surface conditions and therefore subject to degradation over time.

Convection cooling is often adequate where thermal densities are moderate. The most common convective medium is air, with air flow resulting from either forced air or natural convection currents. Natural convection refers to the flow of air created by the existence of thermal gradients. The efficiency of natural convection cooling may be optimized by proper selection of air flow paths. When natural convection is insufficient to achieve proper thermal conditions, fans or electrostatic wind generators may be used to increase the air flow and consequently increase the amount of thermal energy transferred to the air per unit time.

Radiation based techniques are seldom used except in space applications where convective and conductive techniques are impractical. Control of thermal radiation may be achieved by use of radiation shields and appropriate surface coatings. For most military systems, radiative heat transfer is seldom a significant factor in the overall thermal characterization of an equipment.

In some instances it is practical or necessary to employ a thermal design based on a combination of the above methods. A common example of this is the component heat sink. Consider the thermal circuit of Figure 6.2.2.2-2. By employing a heat sink, a low thermal resistance path is provided from the component to the air. Heat is conducted from the component to the heat sink and the heat sink is then cooled by convection, with air serving as the thermal reservoir.

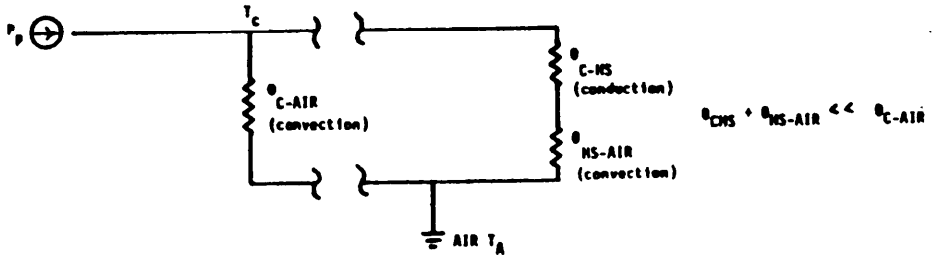


FIGURE 6.2.2.2-2: THERMAL CIRCUIT OF A HEAT SINK

Systems exhibiting very high thermal densities often require special cooling techniques, such as heat pipes, cold plates, refrigerants and others. Each of these techniques has specific strengths and limitations which must be considered before selection of an optimum technique can be made.

6.2.3 GUIDELINES FOR ACHIEVING RELIABLE THERMAL DESIGNS

6.2.3.1 LIMITATIONS ON COOLING TECHNIQUES

This portion of the guide presents limitations on cooling techniques discussed above.

Cooling techniques are limited primarily by the dissipation density of the electronic equipment (i.e., the ratio of the dissipation to the volume of the box in which the equipment is packaged).

Table 6.2.3.1-1 lists maximum dissipation per unit area for common cooling techniques. Table 6.2.3.1-2 lists limitations for forced air cooled module microelectronic parts. Table 6.2.3.1-3 lists limitations of other cooling techniques.

TABLE 6.2.3.1-1: MAXIMUM DISSIPATION PER UNIT AREA FOR COMMON COOLING TECHNIQUES

	Maximum Dissipation Per Unit Heat Transfer Area	
Cooling Technique	W/m^2	W/in^2
Free convection in ambient air and radiation to surroundings	800	0.5
Impingment (forced air)	3,000	2
Air-cooled plate	16,000	10
Free convection to a liquid	500*	0.3*
Liquid-cooled plate	160,000	1000
Evaporation	5×10^7	30000

*Per ^oC temperature difference between surface and liquid

TABLE 6.2.3.1-2: LIMITATIONS ON FORCED-AIR COOLING TECHNIQUES FOR MODULE MICROELECTRONIC PARTS

	Maximum Cooling Capacity	
Cooling Technique	W/m^2	W/in^2
Impingement	800	0.5
Coldwall	1500	1
Flow-through	3400	2

TABLE 6.2.3.1-3: LIMITATIONS ON VARIOUS COOLING TECHNIQUES

Thermoelectric Coolers
Heat-sink temperature $\leq$ 100°C
Cooling load $\leq$300 W
Vapor-Cycle Refrigeration
Power requirement = 250-1000 W per 1000 W of refrigeration
Ambient temperature $\leq$ 71°C ($\leq$200°C for specially designed vapor-cycle equipment)
Expendable Evaporant Cooling
Heat sink temperature $\geq$ 93°C
Duration of operation $\leq$ 3 hrs.

6.2.3.2 PLACEMENT/LAYOUT OF PARTS

Operating temperatures are affected by the arrangement of the parts within the equipment. Thus the equipment's reliability depends on the parts' placement and layout. "Do's and dont's" of parts placement/layout for maximum reliability follow.

(1) Provide as much separation as possible between dissipating parts.

(a) Within a forced air cooled unit, try to spread the dissipating parts uniformly along the coldwall.

(b) Do not place thermally sensitive or high dissipation parts close to each other.

(c) Do not place thermally sensitive parts next to hot spots.

(d) With free convention cooled equipment, do not place parts directly above high dissipating parts. Instead stagger them horizontally, as shown in Figure 6.2.3.2-1.

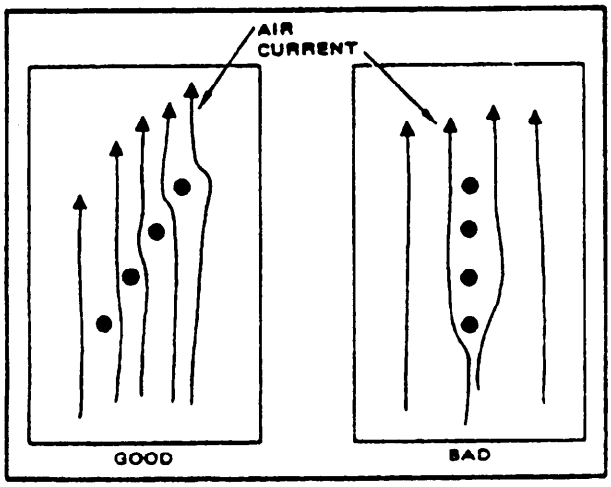


FIGURE 6.2.3.2-1: WITH FREE CONVECTION COOLED EQUIPMENT, DO NOT PLACE PARTS DIRECTLY ABOVE HIGH DISSIPATING PARTS

(2) Lay out parts so that the temperature sensitive parts are in the coolest region, the order to maximize the reliability of the assembly.

(a) With forced convection cooled equipment, place the temperature sensitive parts near the coolant inlet side and the less sensitive parts on the outlet side, as shown in Figure 6.2.3.2-2.

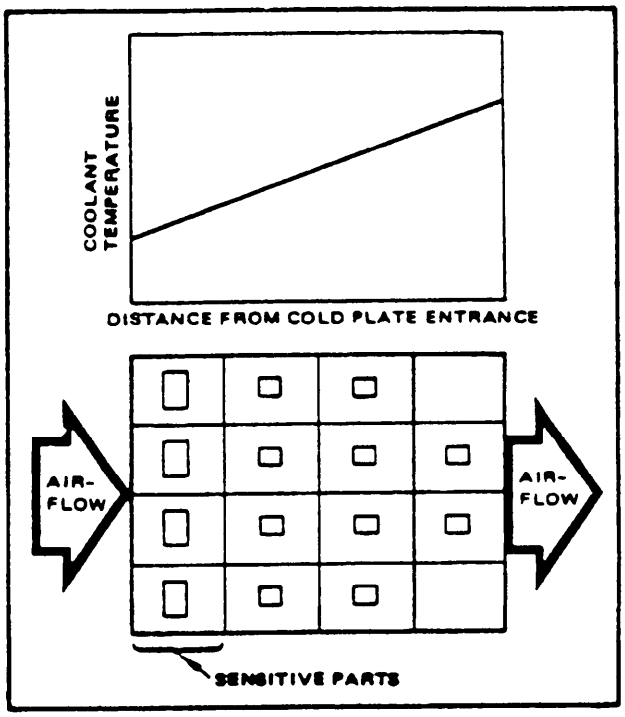


FIGURE 6.2.3.2-2.

(b) With free convection cooled equipment, locate temperature sensitive parts at the bottom and the others above them, as shown in Figure 6.2.3.2-3.

(c) With coldwall cooled circuit cards, place sensitive parts close to card edge.

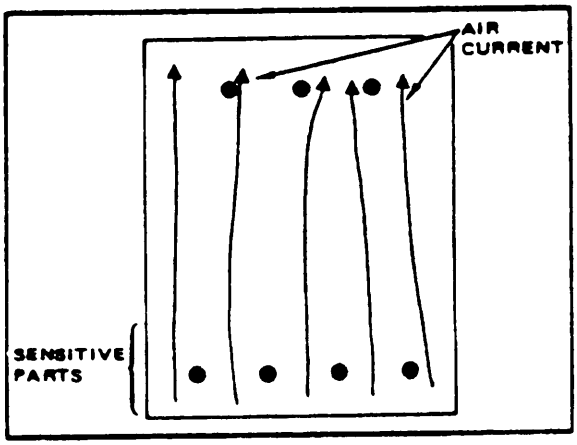


FIGURE 6.2.3.2-3.

6.2.3.3 MOUNTING PARTS

The thermal design objective in mounting parts is to minimize the thermal resistance between the case and a sink. Specific guidelines are given below:

(1) Use short paths in order to minimize the thermal resistance to conduction.

(a) For cold plate cooled equipment, mount the parts directly to the cold plate whenever possible.

(b) Minimize the thickness of adhesive bonds used to attach parts to a module or cold plate.

(2) Use large mounting areas in order to minimize the thermal resistance.

(a) Do not mount parts so that the only conduction path to the heat sink is through the leads.

(b) To increase the heat transfer area, mount high power hybrid microcircuit chips on molybdenum tabs having a larger area than the chip, as shown in Figure 6.2.3.3-1.

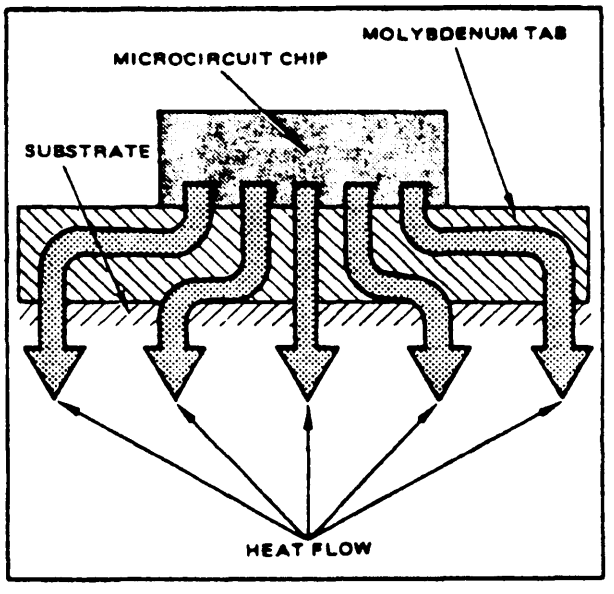


FIGURE 6.2.3.3-1.

(c) To increase the area of conduction path, mount high power parts cooled by free convection and radiation or by impingment cooling on heat transfer fins, as shown in Figure 6.2.3.3-2.

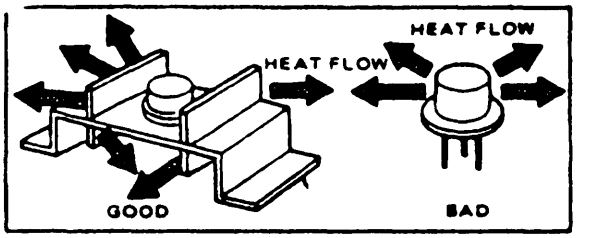


FIGURE 6.2.3.3-2.

(d) Do not use tightly spaced fins for free convection cooling. Do not use more than four fins per inch, and do not use fins higher than 1 inch.

(e) Maximize the areas of all conduction paths and interfaces between the parts and the sink.

(3) Use materials having high thermal conductivity in order to minimize the thermal resistance to conduction.

(a) Use metals such as copper and aluminum for heat conduction paths and mounting brackets.

(b) With spacecraft and high altitude avionic equipment where free convection is nonexistent or very small, fill all gaps along the heat flow path with thermally conductive compounds, as shown in Figure 6.2.3.3-3.

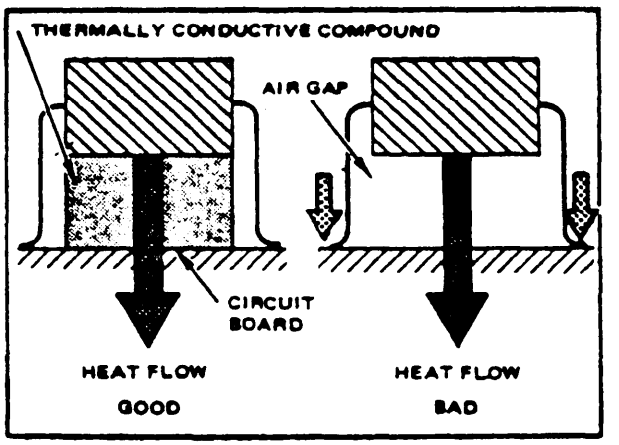


FIGURE 6.2.3.3-3.

(c) With flow through modules comprised of multilayer printed wiring boards, use plated through holes to reduce the thermal resistance to conduction through the board. These copper plated holes are thermal paths called thermal vias, as shown in Figure 6.2.3.3-4.

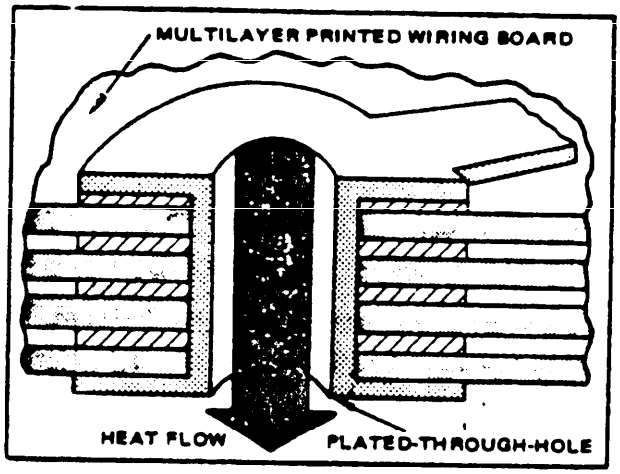


FIGURE 6.2.3.3-4.

(d) Minimize the use of interfaces between contacting surfaces as thermal paths.

(4) When contact interfaces are used, the following practices will minimize the contact thermal resistance.

(a) Use as much contact area as possible.

(b) Ensure that the contacting surfaces are flat and smooth.

(c) Use soft contacting materials.

(d) Torque all bolts to achieve a high contact pressure.

(e) Use enough fasteners to assure a uniform contact pressure.

(f) With coldwall cooled cards, do not use spring loaded card guides to provide contact pressure between the card guide and the card edge. Instead use something positive (e.g., wedge clamps or cam operated guides, as shown in Figure 6.2.3.3-5.

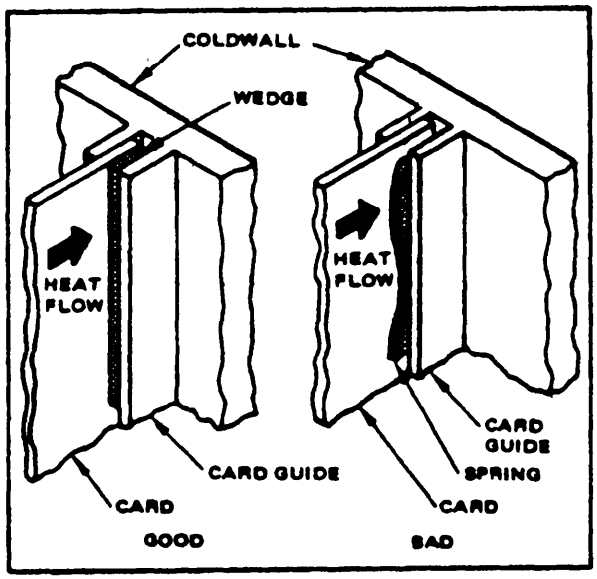


FIGURE 6.2.3.3-5.

6.2.4 MANAGEMENT OF THERMAL DESIGNS

The importance of thermal design in the achievement of predictable and reliable system operation coupled with the importance of selecting the optimum thermal control technique from a multitude of alternatives emphasizes the necessity of implementing a thermal design management program. A flow chart of a typical thermal management program is presented in Figure 6.2.4-1. From this figure it may be deduced that proper management of a thermal design program requires the existence of a number of monitoring procedures to insure adherence to accepted guidelines and specifications including thermal design evaluation criteria, optimization criteria, and testing procedures useful for evaluating thermal designs.

As with any design program, the first order of business is the determination of system constraints and optimization criteria. System constraints may include physical limitations on size, weight, power consumption, reliability requirements, thermal requirements, and any number of requirements relating to the ultimate operational environment of the system. In addition, a set of optimization criteria must be identified in order to permit ranking of alternatives. Typical optimization criteria relate to reliability, life cycle costs, warranty costs, etc. Based on the above considerations, a specific cooling technique may be chosen and a preliminary design developed.

Evaluation of a particular thermal design should include both qualitative and quantitative analyses. Qualitative analysis should evaluate the soundness of the basic design, with particular attention to the suitability of the cooling technique(s) for the particular system and operating environment. For example, the use of noisy cooling fans in an office environment may be unacceptable. The use of convection cooling techniques in dirty environments should be avoided, as the

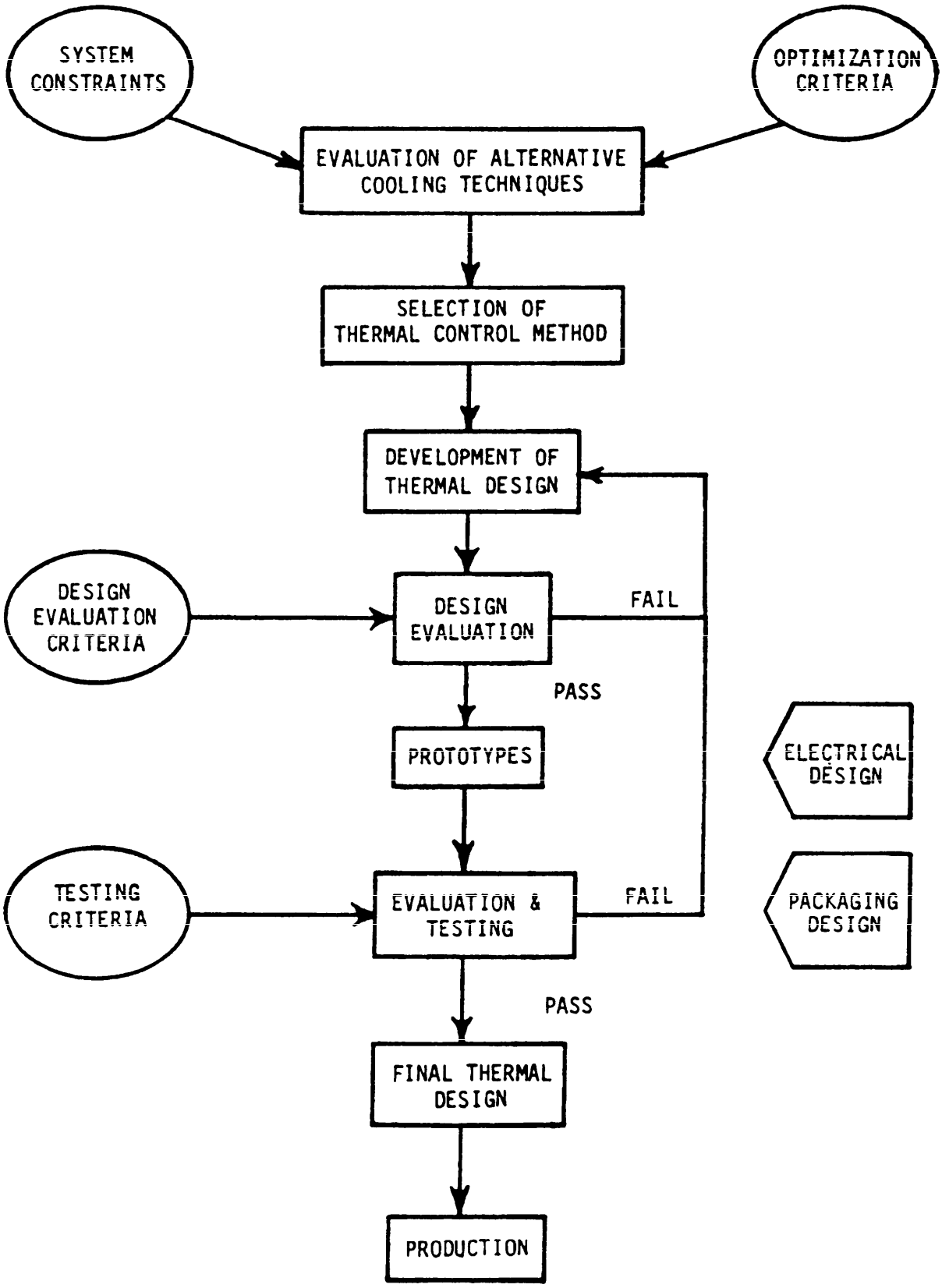


FIGURE 6.2.4-1: FLOW CHART OF THERMAL SYSTEMS MANAGEMENT PROGRESS

gradual accumulation of dirt on internal components results in degraded transfer of heat to the cooling air. Convection systems should be carefully scrutinized when used in avionic systems; changing air pressures over a mission profile may result in inadequate cooling or condensation of moisture under certain conditions. The use of heat pipes may be undesirable in systems which will experience high inertial forces, due to the decreased capillary action resulting from such forces.

Once the suitability of the basic cooling approach has been verified, a thorough quantitative analysis of the thermal design should be performed, as temperature is the ultimate measure of effectiveness of thermal design. For all but the simplest systems, the most efficient means of quantitatively evaluating a thermal design is by use of a computer program designed specifically for that purpose. There are a number of such programs in existence, including NATA (Numerical Analysis Thermal Applications), CINDA (Chrysler Improved Numerical Differencing Analyzer), THTD (Transient Heat Transfer - Version D), and others. Most of these programs draw heavily on the mathematically analogous nature of thermal and electrical circuits. Proper utilization of these programs will provide a detailed description of the thermal profile of an equipment which will compare very favorably with measured temperatures in a prototype system.

Of specific interest to the reliability engineer would be the temperature of the various components and devices in the system. These temperatures should be compared to the temperatures originally assumed in the performance of the reliability prediction. Where the projected temperatures differ from the original assumptions, a new prediction of the reliability of that device should be performed. The cumulative effects of these revisions should then be evaluated to insure compliance with the original reliability requirements for the equipment.

6.2.5 LIMITATIONS OF CURRENT STATE-OF-THE-ART

o Thermal Impact on Reliability - The models of MIL-HDBK-217, Reliability Prediction of Electronic Equipment, are widely recognized as representing the state-of-the-art in reliability prediction methodology. The usefulness of these models for evaluation of thermal designs is very limited, however, due to the fact that the explicit functional relationships between temperature and failure rate are not addressed. Instead, the thermal effects on reliability are typically buried in a complex mathematical expression containing a temperature factor and a number of other parameters, some of which may themselves be temperature dependent. Consequently, the quantitative impact of alternative thermal designs on the reliability of a particular equipment is very difficult to assess.

Another limitation of MIL-HDBK-217 results from inaccuracies induced by using ambient temperature, T_A, as an indicator of component temperature as is done in several of the models. Ambient air temperature is a useful indicator of component temperature if internal convection is the only source of cooling for the equipment. Component cooling by use of

conduction or other more sophisticated techniques (such as heat pipes and refrigerants) will not be accurately reflected by air temperature, with the result that the full reliability benefits resulting from the use of such techniques are not always identified. A careful study of the models involved will be conducted and specific recommendations for their improvement will be made.

o Thermal Design - A great deal of work has been performed in recent years relative to the design of thermal systems. Unfortunately, reports on this work were prepared by, and intended for, thermal design experts. Emphasis is on theory and implementation of efficient thermal designs, rather than on the evaluation or comparison of thermal designs. The information required is certainly available, but it is usually integrated into a lengthy and detailed report. Much effort is required on the part of the reliability engineer to extract a relatively small amount of useful information.

o Thermal Management - Relatively little information has been published on the management of thermal designs. The best existing document identified to date is MIL-HDBK-251, "Reliability/Design Thermal Applications," prepared for the U. S. Navy by Thermal Technology Labs. This document provides a very comprehensive review of the various aspects of thermal design. Although it does contain a wealth of information useful in the management of a thermal design program, it does not specifically address thermal management. Once again, the information is available, but it must be extracted from documents not specifically addressing the problems of managing and/or monitoring thermal designs.

REFERENCES

MacDiarmid, P., (RADC-TR-82-172, GAFB, NY), "Thermal Guide for Reliability Engineers," May 1982.

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7.0 SPECIFICATION AND CONTROL DURING ACQUISITION

7.1 PART SCREENING

As discussed in Volume I, Section 5.3.1 of this Handbook, virtually all manufactured devices exhibit a life characteristic which may best be represented by the bathtub curve shown in Figure 7.1-1. This section of Volume 2 deals with the first segment of the curve, namely, the "infant mortality" or the "early failure" period of the equipment's life.

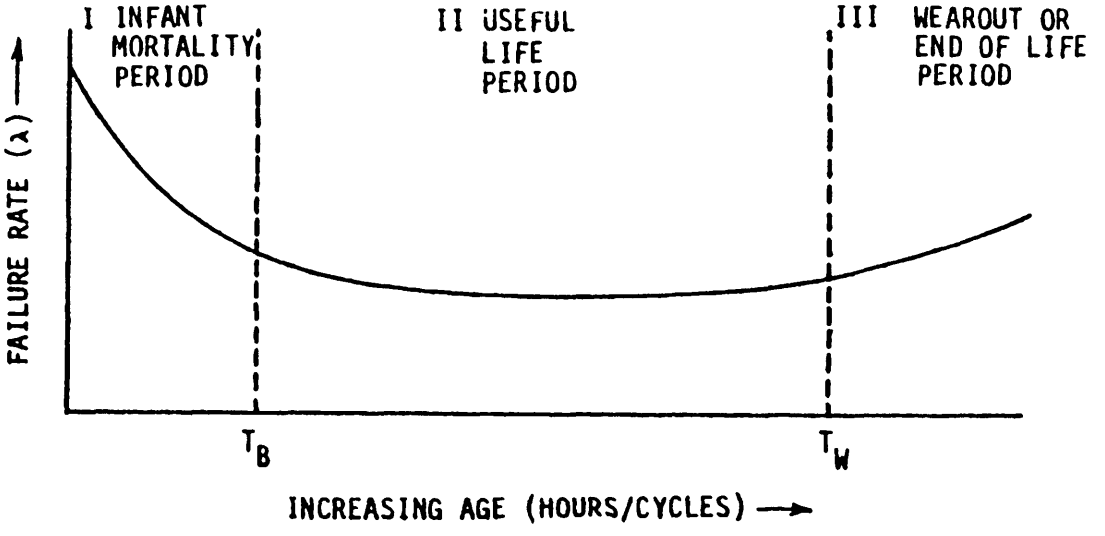


FIGURE 7.1-1: LIFE CHARACTERISTIC CURVE

Experience shows that a newly constructed equipment fails more often during its early life (i.e., during assembly and testing) than later during use in the field. This indicates that piece parts received from suppliers contain a certain number of weak devices which tend to fail during initial testing of subassemblies or complete equipments.

7.1.1 THEORY AND PURPOSE OF SCREENING

In order to eliminate the incipient failures from the manufacturing process, quality and screening tests can be employed. The quality tests are those that reduce the number of defective devices from production lines by means of inspection and conventional testing. The screens are those which remove inferior devices and reduce the hazard rate by means of stress application.

The purpose of reliability screening is to compress the early failure period and reduce the failure rate to acceptable levels as quickly as possible. Figure 7.1.1-1 illustrates the application of a time stress at the part level and shows, comparatively, how reliability screening can improve the part failure rate. It also shows that, by applying a higher temperature stress of 125°C instead of 100°C, comparable failure rate levels can be achieved in 100 hours instead of 240 hours.

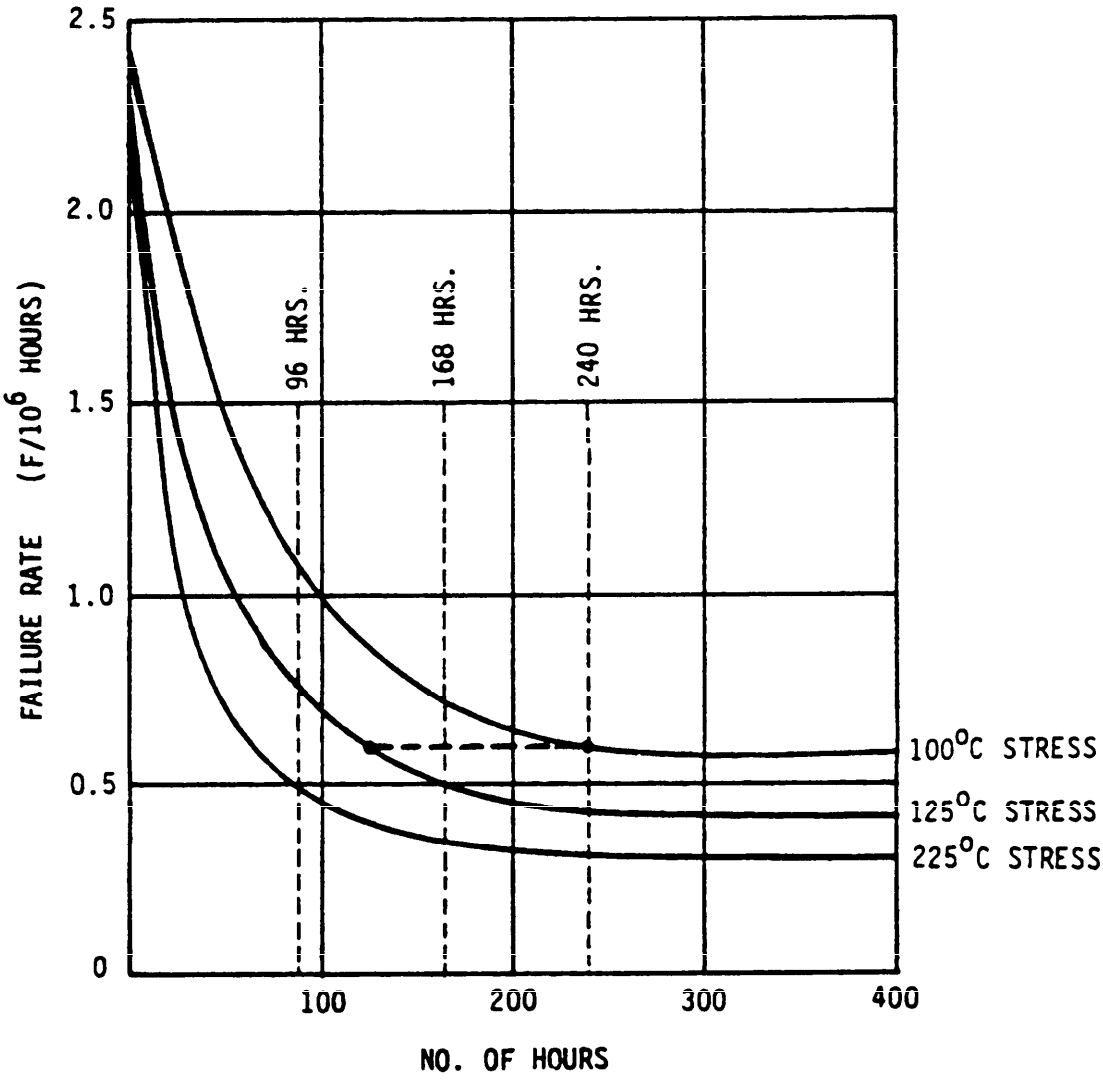


FIGURE 7.1.1-1: RELIABILITY SCREENS

The term "screening" can be said to mean the application to an electronic device of a stress test, or tests, which will reveal inherent weaknesses (and thus incipient failures) of the device without destroying the integrity of the device. This procedure, when applied equally to a group of similar devices manufactured by the same processes, is used to identify sub-par members of the group without impairing the structure or functional capability of the "good" members of the group.

The rationale for such action is that the inferior devices will fail and the superior devices will pass, provided the tests and stress levels are properly selected. If the failed units are removed from the group, the remaining devices are those which have demonstrated the ability to withstand stress, and therefore their reliability under normal rated operating conditions can therefore be assumed.

Screening can be done (a) by the part manufacturer, (b) by the user in his own facilities, or (c) by an independent testing laboratory. No matter which agency is employed to do the screen tests, the user should first acquaint himself with the efficacy of the screening tests used by the vendor in normal production. If such screens exist and are effective, screens can be designed to supplement the vendor's tests; if the vendor's tests are unsatisfactory, the screening program may have to be a comprehensive one.

When particular failure modes or mechanisms are known or suspected to be present, a specific screen should be selected to detect these unreliable elements.

7.1.2 DESIGN OF COMPONENT SCREENS

Since every part drawing which requires special nonstandard screening processes adds greatly to the equipment program logistic(s) burden, every effort should be made to use standard screening processes.

Much money and effort has been expended by DOD agencies and industry in developing reliability screening processes and requirements for the major types of parts used in military equipment. These requirements have been detailed for these parts. There are three different ways in which the reliability screening levels (also referred to as quality or product assurance levels) are specified for three distinct categories of military parts: (1) screened military grade passive electrical parts (e.g., relays, coils, connectors, resistors and capacitors) are procureable to Established Reliability (ER) Military Specifications categorized as to ER failure rate level (L through T); (2) screened military grade semiconductor devices are procureable to MIL-S-19500 and its detailed slash sheets and are categorized as JANTX, JANTXV, and JANS screening levels; (3) screened military grade SSI, MSI and some LSI microcircuits are procureable to MIL-M-38510, are labeled JAN, and categorized as to screening class (i.e., S, B).

Commercial grade, military grade, military ER and JAN grade parts are generally physically and functionally interchangeable, with the basic difference being their failure rate levels which can vary in the order of magnitudes.

7.1.2.1 ESTABLISHED RELIABILITY (ER) PASSIVE PARTS

ER passive electrical parts are procureable in accordance with ER military specifications to various failure rate levels from manufacturers qualified and certified to those levels by government inspectors. Such manufacturers are listed on Qualified Parts Lists (QPLs). ER specifications presently exist for many types of capacitors, resistors, relays, and RF coils.

ER parts procured to ER military specifications exhibit failure rates demonstrated under the controlled test conditions specified in these specifications. These failure rates are expressed as percent failures per thousand hours (%/1,000 hrs). The failure rate levels usually* included in these ER military specifications are:

MIL Symbol	Failure Rate (% Failures/1,000 hrs)
L	2.0
M	1.0
P	0.1
R	0.01
S	0.001
T	0.0001

Parts procured to ER military specifications are also subjected to special process controls, lot acceptance testing, screening, and extended life tests.

In order to achieve and maintain QPL listing, manufacturers of ER parts must establish and implement a reliability assurance program in accordance with MIL-STD-790 that is evaluated and monitored by a government qualifying activity.

ER components are 100% screened in accordance with the applicable test methods and conditions of MIL-STD-202 as required by the individual ER specification.

Failure rates and failure rate levels of ER parts are statistically established during life testing at 60% or 90% confidence levels (as required in the ER part military specifications) and in accordance with failure rate sampling plans and procedures of MIL-STD-690. These failure rates are established for laboratory conditions at rated electrical stress. Failure rate levels at derated application stress levels and actual equipment environments can be estimated using MIL-HDBK-217. ER parts with failure rate levels of P or better (i.e., R, S or T) should be used in the design of military equipment when available.

* Failure rate levels vary for different parts and different ER specifications; e.g., "L" level failure rate for MIL-C-39022 capacitors is 5.0% per 1,000 hours.

TABLE 7.1.2.1-1: LISTING OF MIL-STD-202 TEST METHODS

Method No.	Title
	Environmental Tests (100 Class)
101D	Salt Spray (corrosion)
103B	Humidity (steady state)
104A	Immersion
105C	Barometric pressure (reduced)
106D	Moisture resistance
107D	Thermal shock
108A	Life (at elevated ambient temperature)
109D	Explosion
110A	Sand and dust
111A	Flammability (external flame)
112B	Seal
	Physical Characteristics Tests (200 Class)
201A	Vibration
202D	Shock (specimens weighing not more than 4 pounds) (Superseded by Method 213)
203B	Random drop
204C	Vibration, high frequency
205E	Shock, medium impact (Superseded by Method 213)
206	Life (rotational)
207A	High-impact shock
208C	Solderability
209	Radiographic inspection
210A	Resistance to soldering heat
211A	Terminal strength
212A	Acceleration
213B	Shock (specified pulse)
214	Random vibration
215	Resistance to solvents
	Electrical Characteristics Tests (300 Class)
301	Dielectric withstanding voltage
302	Insulation resistance
303	DC resistance
304	Resistance-temperature characteristic
305	Capacitance
306	Quality factor (Q)
307	Contact resistance
308	Current-noise test for fixed resistors
309	Voltage coefficient of resistance determination procedure
310	Contact-chatter monitoring
311	Life, low level switching
312	Intermediate current switching

7.1.2.2 JAN, JANTX, JANTXV, AND JANS SEMICONDUCTORS

Military grade high reliability screened semiconductors are procureable in accordance with MIL-S-19500 and designated as JANTX, JANTXV and JANS quality levels, depending upon the type and amount of screening performed on the semiconductor. The prefix JAN of a semiconductor type designation refers to the military standardization program for semiconductors. These semiconductors have been tested to and have passed the minimum qualification tests specified by MIL-S-19500. The TX suffix to JAN designates "Testing Extra," (i.e., screening). JANTX parts, in addition to JAN processing, undergo specific process and power conditioning tests on a 100% basis (depending upon the detail specification) in addition to the JAN sampling tests to enable further elimination of defective parts. JANTXV quality level semiconductors require all testing performed on JANTX semiconductor devices plus an internal visual PRECAP inspection which further eliminates defective parts and provides greater reliability in the surviving lot. JANS quality level semiconductors, while requiring all the tests performed on JANTXV parts, also requires Particle Impact Noise Detection (PIND) Testing, Failure Analysis, Serialization and traceability to a wafer lot. A diagram depicting the processing and screening for the JAN, JANTX, JANTXV and JANS are shown in Figures 7.1.2.2-1, 7.1.2.2-2, and 7.1.2.2-3.

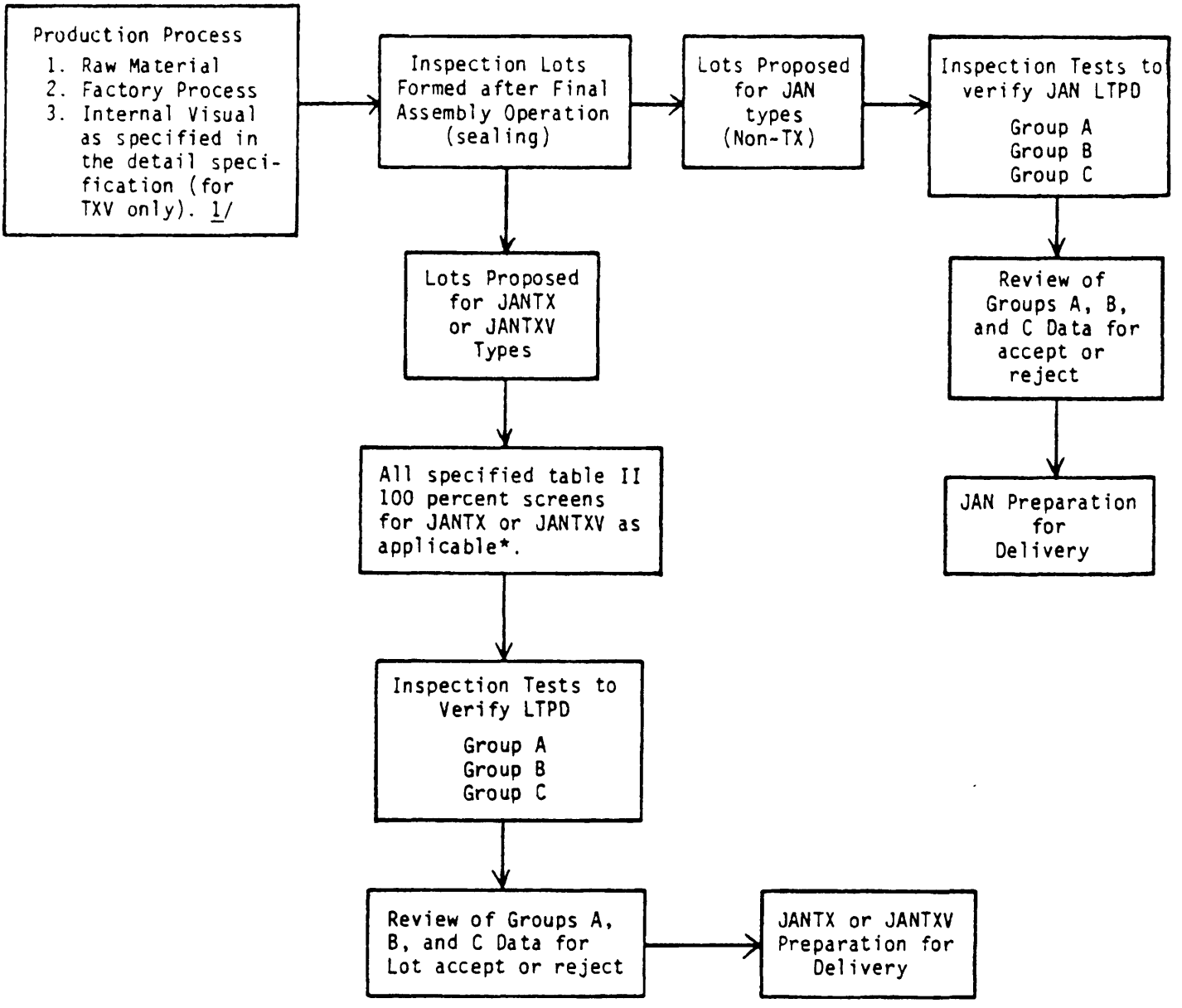
The sampling procedure and acceptance requirement for JAN testing is in accordance with the Lot Tolerance Percent Defective (LTPD) as defined in MIL-STD-105 and as specified in basic MIL-S-19500 specification and in the detailed specification sheets. Tests methods used in screening of semiconductors are in accordance with MIL-STD-750 for tests specified in the detail specification.

Relative failure rates for various types of semiconductors for a given temperature and electrical stress level and based upon JAN as 1.0 are given in Table 7.1.2.2-1. A listing of these tests is provided in Table 7.1.2.2-2.

TABLE 7.1.2.2-1: RELATIVE FAILURE RATE DIFFERENCES

Screening Level	All Semiconductors Except Microwave	Microwave Detectors and Mixers (Si & Ge)
JANS	.05	.05
JANTXV	.1	.1
JANTX	.2	.3
JAN	1.0	1.0
Lower*	5.0	5.0

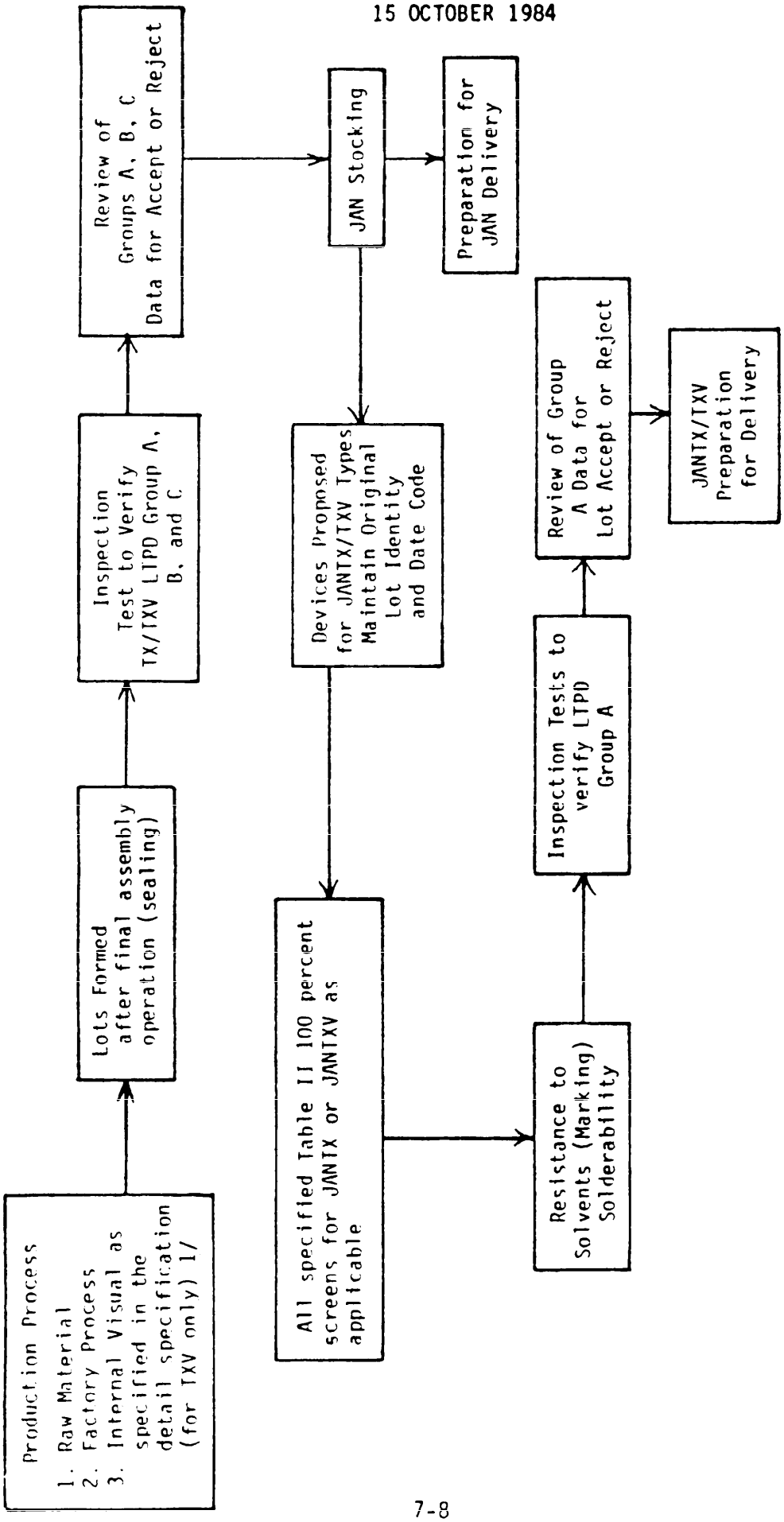
*Hermetic packaged devices



* Order of the tests shall be performed as specified in MIL-S-19500, Table II.

1/ All products to be proposed for JANTXV processing must have been subjected to and passed JANTXV internal visual 100 percent screening at this step (except for clear glass JANTXV diodes which shall be subjected to internal visual inspection prior to painting or marking).

FIGURE 7.1.2.2-1: ORDER OF PROCEDURE DIAGRAM FOR JAN, JANTX, AND JANTXV DEVICE TYPES



* Order of the tests in the blocks shall be performed as specified in MIL-S-19500

1/ See footnote 1/ from FIGURE 7.1.2.2-1

FIGURE 7.1.2.2-2: ALTERNATE ORDER OF PROCEDURE DIAGRAM FOR JAN, JANTX, AND JANTXV TYPES

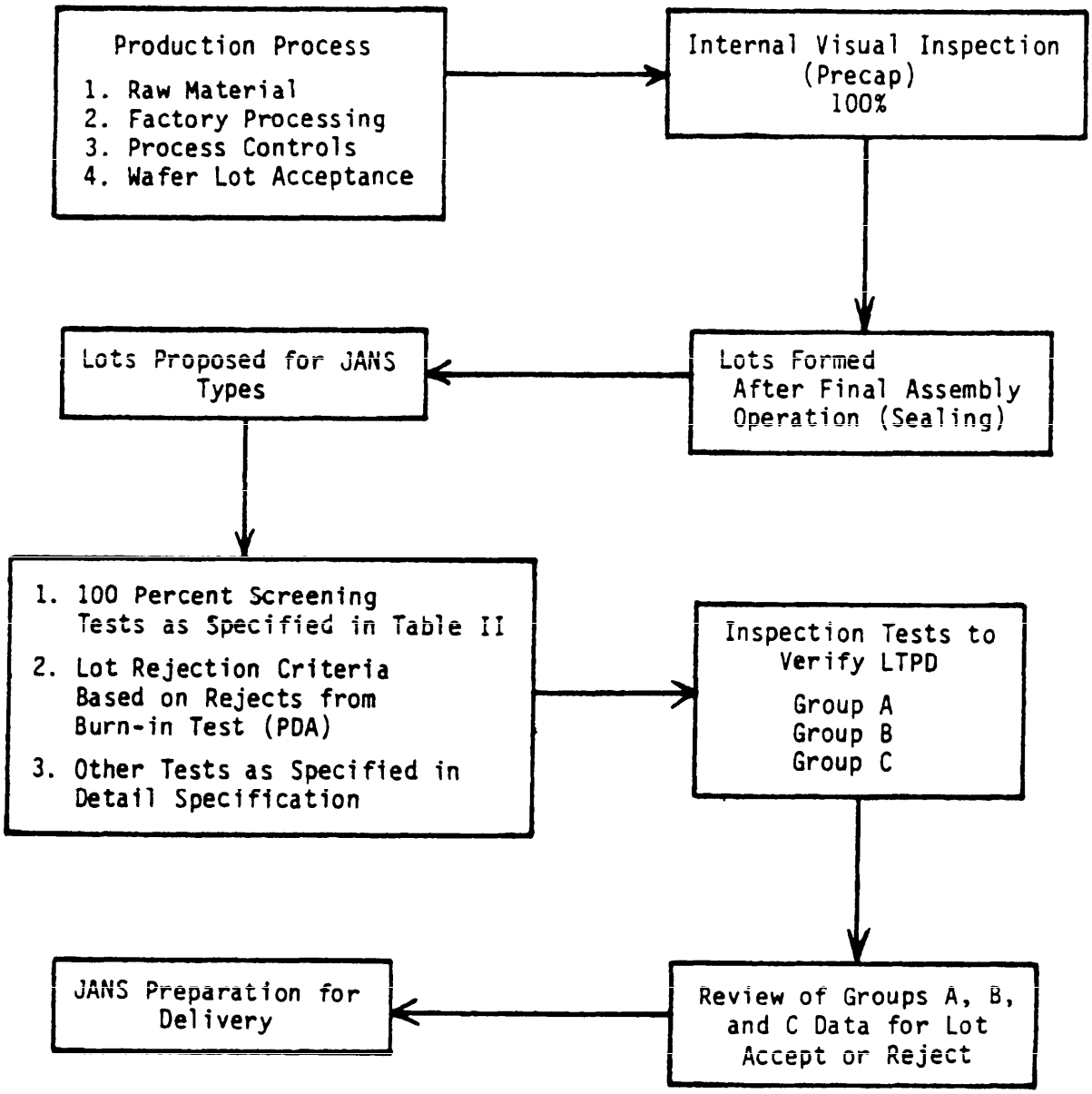


FIGURE 7.1.2.2-3: ORDER OF PROCEDURE DIAGRAM FOR CLASS JANS

TABLE 7.1.2.2-2: MIL-STD-750 TEST METHODS FOR DISCRETE SEMICONDUCTOR DEVICES

Method No.	Environmental Tests (100 Class)
1001.1	Barometric pressure (reduced)
1011	Immersion
1016	Insulation resistance
1017	Neutron irradiation
1021.1	Moisture resistance
1022	Resistance to solvents
1026.3	Steady-state operation life
1027.1	Steady-state operation life (LTPD)
1031.4	High-temperature life (non-operating)
1032.1	High-temperature (non-operating) life (LTPD)
1036.3	Intermittent operation life
1037	Intermittent operation life (LTPD)
1038	Burn-in (for diodes and rectifiers)
1039	Burn-in (for transistors)
1040	Burn-in (for thyristors (controlled rectifiers))
1041.1	Salt atmosphere (corrosion)
1046.2	Salt spray (corrosion)
1051.1	Thermal shock (temperature cycling)
1056.1	Thermal shock (glass strain)
1061.1	Temperature measurement, case and stud
1066.1	Dew point
1071.1	Hermetic seal
	Mechanical Characteristics Test (2000 Class)
2005	Axial lead tensile test
2006	Constant acceleration
2016.2	Shock
2026.3	Solderability
2031.1	Soldering heat
2036.3	Terminal strength
2037	Bond strength
2046.1	Vibration fatigue
2051.1	Vibration noise
2052	Particle impact noise detection (PIND)
2056	Vibration, variable frequency
2057.1	Vibration, variable frequency (monitored)
2066	Physical dimensions
2071	Visual and mechanical examination
2072	Internal visual (precap) inspection
2073	Visual inspection for die (semiconductor diode)
2074	Internal visual inspection (discrete semiconductor diodes)
2075	Decap internal visual design verification

TABLE 7.1.2.2-2: MIL-STD-750 TEST METHODS FOR DISCRETE SEMICONDUCTORS (Cont'd)

Method No.	Mechanical Characteristics Test (2000 Class) (Cont'd)
2076	Radiographaic inspection
2081	Forward instability, shock (FIST)
2082	Backward instability, vibration (BIST)
	Electrical-Characteristics Tests (for Transistors) (3000 Series)
3001.1	Breakdown voltage, collector to base
3005.1	Burnout by pulsing
3011.1	Breakdown voltage, collector to emitter
3015	Drift
3020	Floating potential
3026.1	Breakdown voltage, emitter to base
3030	Collector to emitter voltage
3036.1	Collector to base cutoff current
3041.1	Collector to emitter cutoff current
3051	Safe operating area (continuous dc)
3052	Safe operating area (pulsed)
3053	Safe operating area (switching)
3061.1	Emitter to base cutoff current
3066.1	Base emitter voltage (saturated or non-standard)
3071	Saturation voltage and resistance
3076.1	Forward-current transfer ratio
3086.1	Static input resistance
3092.1	Static transconductance
	Circuit-Performance and Thermal Resistance Measurements (3100 Series)
3126	Thermal resistance (collector-cutoff-current method)
3131.1	Thermal resistance (emitter to base forward voltage, emitter-only, switching method)
3132	Thermal resistance (dc forward voltage drop, emitter base, continuous method)
3136	Thermal resistance (forward voltage drop, collector to base, diode method)
3141	Thermal response time
3146.1	Thermal time constant
3151	Thermal resistance, general

TABLE 7.1.2.2-2: MIL-STD-750 TEST METHODS FOR DISCRETE SEMICONDUCTORS (Cont'd)

Method No.	
	Low Frequency Tests (3200 Series)
3201.1	Small-signal short-circuit input impedance
3206.1	Small-signal short-circuit forward-current transfer ratio
3211	Small-signal open-circuit reverse-voltage transfer ratio
3216	Small-signal open-circuit output admittance
3221	Small-signal short-circuit input admittance
3231	Small-signal short-circuit output admittance
3236	Open circuit output capacitance
3240.1	Input capacitance (output open-circuited or short-circuited)
3241	Direct interterminal capacitance
3246.1	Noise figure
3251.1	Pulse response
3255	Large-signal power gain
3256	Small-signal power gain
3261.1	Extrapolated unity gain frequency
3266	Real part of small-signal short-circuit input impedance
	High Frequency Tests (3300 Series)
3301	Small-signal short-circuit forward-current transfer-ratio cutoff frequency
3306.2	Small-signal short-circuit forward-current transfer ratio
3311	Maximum frequency of oscillation
	Field-Effect Transistor Electrical Tests (3400 Series)
3401	Breakdown voltage, gate to source
3403	Gate to source voltage or current
3405	Drain to source "on"-state voltage
3407	Breakdown voltage, drain to source
3411	Gate reverse current
3413	Drain current
3415	Drain reverse-current
3421	Static drain to source "on"-state resistance
3423	Small-signal, common-source, short-circuit, input capacitance
3431	Small-signal, common source, short-circuit, input capacitance

TABLE 7.1.2.2-2: MIL-STD-750 TEST METHODS FOR DISCRETE SEMICONDUCTORS (Cont'd)

Method No.	
	Field-Effect Transistor Electrical Tests (3400 Series) (Cont'd)
3433	Small-signal, common-source, short-circuit, reverse-transfer capacitance
3453	Small-signal, common-source, short-circuit, forward transadmittance
3457	Small-signal, common-source, short-circuit, reverse transfer admittance
3459	Pulse response (FET)
3461	Small-signal, common-source, short-circuit, input admittance
	Electrical-Characteristics Tests for Diodes (4000 Series)
4001.1	Capacitance
4011.4	Forward voltage
4016.3	Reverse current leakage
4021.2	Breakdown voltage (diodes)
4022	Breakdown voltage (voltage regulators and voltage-reference diodes)
4026.2	Forward recovery voltage and time
4031	Reverse recovery time
4036.1	"Q" for voltage variable capacitance diodes
4041.2	Rectification efficiency
4046.1	Reverse current, average
4051.3	Small-signal reverse breakdown impedance
4056.2	Small-signal forward impedance
4061.1	Stored charge
4066.2	Surge current
4071	Temperature coefficient of breakdown voltage
4076.1	Saturation current
4081.1	Thermal resistance for signal diodes, rectifier diodes, and thyristors
	Microwave Diodes (4100 Series)
4101.3	Conversion loss
4102	Microwave diode capacitance
4106	Detector power deficiency
4111.1	Figure of merit (current sensitivity)
4116.1	Intermediate frequency (IF) impedance
4121.2	Output noise ratio
4126.2	Overall noise figure and noise figure of the IF amplifier

TABLE 7.1.2.2-2: MIL-STD-750 TEST METHODS FOR DISCRETE SEMICONDUCTORS (Cont'd)

Method No.	
	Microwave Diodes (4100 Series) (Cont'd)
4131.1	Video resistance
4136.1	Standing wave ratio
4141.1	Burnout by repetitive pulsing
4146.1	Burnout by single pulse
4151	Rectified microwave diode current
	Thyristor (Controlled Rectifiers) (4200 Series)
4201.2	Holding current
4206.1	Forward blocking current
4211.1	Reverse blocking current
4216	Pulse response
4219	Reverse gate current
4221.1	Gate-trigger voltage or gate-trigger current
4223	Gate-controlled turn-on time
4224	Circuit-commutated turn-off time
4225	Gate-controlled turn-off time
4226.1	Forward "on" voltage
4231.2	Exponential rate of voltage rise
	Tunnel Diodes (4300 Series)
4301	Junction capacitance
4306.1	Static characteristics of tunnel diodes
4316	Series inductance
4311	Negative resistance
4326	Series resistance
4331	Switching time

7.1.2.3 QUALITY/RELIABILITY LEVELS OF MICROCIRCUITS

High quality level microcircuits should be procured per MIL-M-38510. This specification establishes the design, quality, reliability assurance and vendor qualification, and certification requirements for monolithic, multichip and hybrid microcircuits. There are two classes of screening provided for military JAN microcircuits: MIL-M-38510 JAN Classes S, and B, with S being the highest quality level and B the lowest quality level. Only microcircuits procured per MIL-M-38510 may have the "JAN" designation. The MIL-M-38510 Class S, and B microcircuits require screening tests in accordance with MIL-STD-883 Method 5004 (for monolithic) or Method 5008 (for hybrid) devices except for interim electrical parameter testing. Manufacturers of microcircuits per Classes S, and B of MIL-M-38510 must meet specific qualification requirements to acquire and maintain listing on the QPL. This qualification requires a manufacturer certification (including a government approved Product Assurance Program Plan), production line certification, and qualification and quality conformance inspection testing per Method 5005 (for monolithic) or Method 5008 (for hybrid microcircuits) of MIL-STD-883.

Many microcircuits are procured to MIL-STD-883 Class S, and B screening. These devices may have been subjected to the tests of MIL-STD-883 Method 5004 (for monolithic) or Method 5008 (for hybrid microcircuits) but have not been qualified to MIL-M-38510 nor had the in-process controls required by MIL-M-38510. They generally exhibit higher failure rates than MIL-M-38510. There are also various vendor equivalents, "vendor classes," and lower grade commercial parts which exhibit much higher failure rates than both the MIL-M-38510 and MIL-STD-883 Method 5004 or Method 5008 screened microcircuits. A listing of the product assurance qualification, inspection and screening requirements tests required by MIL-M-38510 and MIL-STD-883 Method 5004 or Method 5008 are shown in Table 7.1.2.3-1. MIL-M-38510 Class B or S quality levels are required for all microcircuits used in the new design of military equipment.

Electrical performance tests for testing various types of microcircuits are specified in the detailed microcircuit military specification and are performed in accordance with the applicable test methods of MIL-STD-883. A listing of MIL-STD-883 test methods is provided in Table 7.1.2.3-1.

TABLE 7.1.2.3-1: MIL-STD-883 TEST METHODS FOR MICROCIRCUITS

Method No.	Environmental Tests
1001	Barometric pressure, reduced (altitude operation)
1002	Immersion
1003	Insulation resistance
1004.2	Moisture resistance
1005.2	Steady state life
1006	Intermittent life
1007	Agree life
1008.1	High temperature storage
1009.2	Salt temperature (corrosion)
1010.3	Temperature cycling
1011	Thermal shock
1012	Thermal characteristics
1013	Dew point
1014.3	Seal
1015.2	Burn-in screen
1016	Life/reliability characterization tests
1017.1	Neutron irradiation
1018.1	Internal water-vapor content
1019	Steady state total dose irradiation procedure
1020	Radiation-induced latchup test procedure
	Mechanical Tests
2001.2	Constant acceleration
2002.2	Shock
2003.2	Solderability
2004.2	Lead integrity
2005.1	Vibration fatigue
2006.1	Vibration noise
2007.1	Vibration, variable frequency
2008.1	Visual and mechanical
2009.2	External visual
2010.4	Internal visual (precap)
2011.3	Bond strength
2012.3	Radiography
2013.1	Internal visual
2014	Internal visual and mechanical
2015.2	Resistance to solvents
2016	Physical dimensions
2017.1	Internal visual (hybrid)
2018	Scanning electron microscope (SEM) inspection of metallization
2019.1	Die shear strength
2020.1	Particle impact noise detection test
2021	Glassivation layer integrity

TABLE 7.1.2.3-1: MIL-STD-883 TEST METHODS FOR MICROCIRCUITS (Cont'd)

Method No.	
	Mechanical Tests (Cont'd)
2022	Memiscograph solderability
2023	Non-destructive bond pull
2024	Lid torque for glass-frit-sealed packages
	Electrical Tests (Digital)
3001.1	Drive source, dynamic
3002.1	Load conditions
3003.1	Propagation delay
3004.1	Delay and transition time measurements
3005.1	Power supply current
3006.1	High level output voltage
3007.1	Low level output voltage
3008.1	Breakdown voltage, input or output
3009.1	Input current, low level
3010.1	Input current, high level
3011.1	Output short circuit current
3012.1	Terminal capacitance
3013.1	Noise margin measurements for microelectronic logic gating circuits
3014	Functional testing
	Electrical Tests (Linear)
4001	Input offset voltage and current and bias current
4002	Phase margin and slew rate measurements
4003	Common mode input voltage range Common mode rejection ratio Supply voltage rejection ratio
4004	Open loop performance
4005	Output performance
4006	Power gain and noise figure
4007	Automatic gain control range
	Miscellaneous Tests
5001	Parameter mean value control
5002	Parameter distribution control
5003	Failure analysis procedures for microcircuits
5004.4	Screening procedures
5005.6	Qualification and quality conformance procedures
5006	Limit testing
5007.3	Water lot acceptance
5008	Test procedures for hybrid and multichip microcircuits

7.1.3 SCREENING COST EFFECTIVENESS

A detailed understanding of the device's operating characteristics and the materials, packaging and fabrication techniques employed in its construction is essential in selecting a meaningful screen at reasonable cost. Devices that perform the same function may be fabricated with different materials (e.g., aluminum leads instead of gold on an integrated circuit). The effectiveness of a screen is material dependent. For example, the wirebond stress level that is effective for gold may be ineffective for aluminum because of the difference in mass. The X-ray screen is effective for gold, but aluminum and silicon are transparent to X-rays. Some screens are effective for p-n isolated integrated circuits but ineffective for dielectrically isolated devices. Only a thorough knowledge of the device to be screened and the effectiveness and limitations of the various tests can produce a useful and reliable screening procedure.

Screening tests are particularly well-suited to discrete semiconductor and microelectronic devices due to their material/process dependency. MIL-STD-883 forms the basis for selecting meaningful screening tests for microelectronic devices. Note that JANTX semiconductors are screened and burned-in in a manner comparable to MIL-STD-883.

Tables 7.1.3-1 and 7.1.3-2, reproduced from MIL-HDBK-175, provide a listing of microcircuit defects/screens and a comparison of screening methods, respectively.

The criticality of the component part application and the required level of reliability has an important bearing on the stress levels and number of tests that should be included in the overall part screening procedure. The part screen procedure must also be cost effective and must meet time and funding constraints. A cost effective screen requires consideration of two important factors: the criticality of application and the cost of a failure at various levels of assembly.

Criticality of application is dependent on several items, including the accessibility/repairability of the item, safety considerations, and the criticality of the component to mission success. If, for example, the component is to be used on a satellite (non-repairable) and the particular item is critical to mission success, then the cost of failure is essentially the loss of the mission. If the component is to be used in a video game, the item is readily repairable, replacement is inexpensive, the function is noncritical and the cost of failure is minimal. Finally, a microprocessor used as a safety interlock control on a piece of heavy equipment may be easily accessible and inexpensive to replace, but a failure could result in loss of life of the operator, so the application is safety-critical.

Obviously, in order to develop a cost-effective screen, the cost of a failure at the various levels of assembly (component, board, system, field) must be considered.

TABLE 7.1.3-1: MICROCIRCUIT DEFECTS/SCREENS

Point at Which a Reliability-Influencing Variable is Introduced	Failure Mechanism	Failure Mode	Failure Detection Method
Slice Preparation	Dislocations and stacking faults	Degradation of junction characteristics	Initial electrical test; operational-life tests
	Nonuniform resistivity	Unpredictable component values	Initial electrical test; operational-life tests
	Irregular surface	Improper electrical performance and/or shorts, opens, etc.	Initial electrical test; operational-life tests
	Cracks, chips, scratches (general handling damage)	Opens, possible shorts in subsequent metallization	Initial electrical test; visual (pre-cap); thermal cycling
	Contamination	Degradation of junction characteristics	Visual (pre-cap); thermal cycling; high temperature storage; reverse bias
Passivation	Cracks and pin holes	Electrical breakdown in oxide layer between metallization and substrate; shorts caused by faulty oxide diffusion mask	High-temperature storage; thermal cycling; high-voltage test; operating-life test; visual (pre-cap)
	Nonuniform thickness	Low breakdown and increased leakage in the oxide layer	High-temperature storage; thermal cycling; high-voltage test; operating-life test; visual (pre-cap)
Masking	Scratches, nicks, blemishes in the photo mask	Opens and/or shorts	Visual (pre-cap); initial electrical test
	Misalignment	Opens and/or shorts	Visual (pre-cap); initial electrical test
	Irregularities in photoresist patterns (line widths, spaces, pinholes)	Performance degradation caused by parameter drift, opens, or shorts	Visual (pre-cap); initial electrical test
Etching	Improper removal of oxide	Opens and/or shorts or intermittents	Visual (pre-cap); initial electrical test; operational-life test
	Undercutting	Shorts and/or opens in metallization	Visual (pre-cap); initial electrical test
	Spotting (etch splash)	Potential shorts	Visual (pre-cap); thermal cycling; high-temperature storage; operational-life test
	Contamination (photoresist, chemical residue)	Low breakdown; increased leakage	Visual (pre-cap); initial electrical test; thermal cycling; high-temperature storage; operational-life test
Diffusions	Improper control of doping profiles	Performance degradation resulting from unstable and faulty passive and active components	High-temperature storage; thermal cycling; operational-life test; initial electrical test

TABLE 7.1.3-1: MICROCIRCUIT DEFECTS/SCREENS (Cont'd)

Point at Which a Reliability-Influencing Variable is Introduced	Failure Mechanism	Failure Mode	Failure Detection Method
Metallization	Scratched or smeared metallization (handling damage)	Opens, near opens, shorts, near shorts	Visual, (pre-cap); thermal cycling; operational-life test
	Thin metallization to insufficient deposition or oxide steps	Opens and/or high-resistance intraconnections	Initial electrical test; operational-life test; thermal cycling
	Corrosion (chemical residue)	Opens in metallization	Visual (pre-cap); high-temperature storage; thermal cycling; operational-life test
	Misalignment and contaminated contact areas	High contact resistance or opens	Visual (pre-cap); initial electrical test; high-temperature storage; thermal cycling; operational-life test
	Improper alloying temperature or time	Open metallization, poor adhesion, or shorts	Initial electrical test; high-temperature storage; thermal cycling; operational-life tests
Die Separation	Improper die separation resulting in cracked or chipped dice	Opens and potential opens	Visual (pre-cap); thermal cycling; vibration; mechanical shock; thermal shock
Die Bonding	Voids between header and die	Performance degradation caused by overheating	X-ray; operational-life; acceleration, mechanical shock; vibration
	Overspreading and/or loose particles of eutectic solder	Shorts or intermittent shorts	Visual (pre-cap); X-ray; monitored vibration; monitored shock
	Poor die-to-header bond	Cracked or lifted die	Visual (pre-cap); acceleration; shock, vibration
	Material mismatch	Lifted or cracked die	Thermal cycling; high-temperature storage; acceleration
Wire Bonding	Overbonding and underbonding	Wire weakened and breaks or is intermittent; lifted bond; open	Acceleration; shock; vibration
	Material incompatibility or contaminated bonding pad	Lifted lead bond	Thermal cycling; high-temperature storage; acceleration, shock, vibration
	Plague formation	Open bonds	High-temperature storage; thermal cycling; acceleration, shock, vibration
	Insufficient bonding pad area or spacings	Opens or shorted bonds	Operational-life test; acceleration, shock, vibration; visual (pre-cap)

between conductor paths. Integrated board surface causing short circuits

TABLE 7.1.3-1: MICROCIRCUIT DEFECTS/SCREENS (Cont'd)

Point at Whith a Reliability-Influencing Variable is Introduced	Failure Mechanism	Failure Mode	Failure Detection Method
Wire Bonding (continued)	Improper bonding procedure or control	Opens, shorts, or intermittent operation	Visual (pre-cap); initial electrical test; acceleration, shock, vibration
	Improper bond alignment	Opens and/or shorts	Visual (pre-cap); initial electrical test
	Cracked or chipped die	Open	Visual (pre-cap); high-temperature storage; thermal cycling; acceleration, shock vibration
	Excessive loops, sags or lead length	Shorts to case, substrate, or other leads	Visual (pre-cap); X-ray; acceleration, shock, vibration
	Nicks, cuts, and abrasions on leads	Broken leads causing opens or shorts	Visual (pre-cap); acceleration, shock vibration
	Unremoved pigtails	Shorts or intermittent shorts	Visual (pre-cap); acceleration, shock, vibration; X-ray
Final Seal	Poor hermetic seal	Performance degradation; shorts or opens caused by chemical corrosion or moisture	Leak tests
	Incorrect atmosphere sealed in package	Performance degradation caused by inversion and channeling	Operational-life test; reverse bias, high-temperature storage, thermal cycling
	Broken or bent external leads	Open circuit	Visual; lead fatigue tests
	Cracks, voids in kovar-to-glass seals	Shorts and/or opens in the metallization caused by a leak	Leak test; electrical test; high-temperature storage; thermal cycling; high-voltage test
	Electrolytic growth of metals or metallic compounds across glass seals between leads and metal case	Intermittent shorts	Low-voltage shorts
	Loose conducting particles in package	Intermittent shorts	Acceleration; monitored vibration; X-ray; monitored shock
	Improper marking	Completely inoperative	Electrical test

TABLE 7.1.3-2: COMPARISON OF SCREENING METHODS

Screen	Defects	Effectiveness	Cost	Comments
Internal visual inspection	Lead dress Metallization Oxide Particle Die Bond Wire Bond Contamination Corrosion Substrate		Inexpensive to moderate	This is a mandatory screen for high-reliability devices. Cost will depend upon the depth of the visual inspection.
Infrared	Design (thermal)	Very good	Expensive	For use in design evaluation only.
X-ray	Die bond Lead dress (gold) Particle Manufacturing (gross errors) Seal Package Contamination	Excellent Good Good Good Good Good Good	Moderate	The advantage of this screen is that the die-to-header bond can be examined and some inspection can be performed after encapsulation. However, some materials are transparent to X-rays (i.e., Al and Si) and the cost may be as high as six times that of visual inspection, depending upon the complexity of the test system.
High temperature storage	Electrical (stability) Metallization Bulk silicon Corrosion	Good	Very inexpensive	This is a highly desirable screen.
Temperature cycling	Package Seal Die Bond Wire Bond Cracked substrate Thermal mismatch	Good	Very inexpensive	This screen may be one of the most effective for aluminum lead systems.
Thermal shock	Package Seal Die Bond Wire Bond Cracked substrate Thermal mismatch	Good	Inexpensive	This screen is similar to temperature cycling but induces higher stress levels.
Constant acceleration	Lead dress Die Bond Wire Bond Cracked substrate	Good	Moderate	At 20,000 G stress levels, the effectiveness of this screen for aluminum is questionable.
Shock (unmonitored)	Lead dress	Poor	Moderate	The drop-shock test is considered inferior to constant acceleration. However, the pneumopactor shock test may be more effective. Shock tests may be destructive.
Shock (monitored)	Particles Intermittent short Intermittent open	Poor Fair Fair	Expensive	Visual or X-ray inspection is preferred for particle detection.
Vibration fatigue	Lead dress Package Die Bond Wire Bond Cracked substrate	Poor	Expensive	This test may be destructive. Except for work hardening, it is without merit.
Vibration variable frequency (unmonitored)	Package Die Bond Wire Bond Substrate	Fair	Expensive	
Vibration variable frequency (monitored)	Particles Lead dress Intermittent open	Fair Good Good	Very expensive	The effectiveness of this screen for detecting particles is part-dependent.

TABLE 7.1.3-2: COMPARISON OF SCREENING METHODS (Cont'd)

Screen	Defects	Effectiveness	Cost	Comments
Random vibration (unmonitored)	Package Die Bond Wire Bond Substrate	Good	Expensive	This is a better screen than VVF (unmonitored) especially for space-launch equipment, but it is more expensive.
Random vibration (monitored)	Particles Lead dress Intermittent open	Fair Good Good	Very Expensive	This is one of the most expensive screens; when combined with only fair effectiveness for particle detection, it is not recommended except in very special situations.
Helium leak test	Package Seals	Good	Moderate	This screen is effective for detecting leaks in the range of 10^{-8} to 10^{-10} Atm. cc/sec.
Radiflo leak test	Package Seals	Good	Moderate	This screen is effective for leaks in the range of 10^{-8} to 10^{-12} Attm cc/sec.
Nitrogen bomb test	Package Seals	Good	Inexpensive	This test is effective for detecting leaks between the gross-and-fine-leak-detection ranges.
Gross-leak test	Package Seals	Good	Inexpensive	Effectiveness is volume-dependent. Detects leaks greater than 10 Atm. cc/sec.
High-voltage test	Oxide	Good	Inexpensive	Effectiveness is fabrication dependent.
Isolation resistance	Lead dress Metallization Contamination	Fair	Inexpensive	
Intermittent operation life	Metallization Bulk silicon Oxide Inversion/ channeling Design Parameter drift Contamination	Good	Expensive	Probably no better than ac operating life.
Ac operating life	Metallization Bulk silicon Oxide Inversion/ channeling Design Parameter Contamination	Very good	Expensive	
Dc operating life	Essentially the same as intermittent life.	Good	Expensive	No mechanisms are activated that could not be better activated by ac life tests.
High-temperature ac operating life	Same as ac operating life	Excellent	Very expensive	Temperature acts to accelerate failure mechanisms. This is probably the most expensive screen and one of the most effective.
High-temperature reverse-bias	Inversion/ channeling	Poor	Expensive	

A commonly used rule of thumb for military systems assumes that the cost of replacement increases an order of magnitude for each higher level of assembly. The chart below gives the relative cost of a failure at component board, system, and field levels for consumer, industrial, military and space application.

	Consumer	Industrial	Military	Space
Component	$ 2	$ 4	$ 7	$ 15
Board	$ 5	$ 25	$ 50	$ 75
System	$ 5	$ 45	$ 120	$300
Field	$50	$215	$1000	$200M

As an illustration of how this may be used in a cost-effective screening study, consider the following example:

o Suppose that on the average, 5% of each 1,000 lot of ICs, or 50 out of 1,000, are defective when they reach the equipment manufacturer's plant. If only a rudimentary go/no-go test is applied in the receiving room, perhaps 20 of the defective ICs might be caught. Subsequent tests during production might catch another 15 defective devices at the subsystem level, and perhaps 10 more might be detected at the system level. But the remaining five would be installed and shipped, only to be discovered once the equipment went into field use.

o If this were military equipment, the cost of replacing the ICs at the receiving stage would be $7 x 20, or $140, at the subsystem stage $50 x 15 or $750, at system stage $120 x 10 or $1,200, and in the field $1,000 x 5, or $5,000. In sum, the defective ICs would cost $7,090 to replace. This $7,000 or so is what could be spent on an effective screening program of the incoming 1,000 ICs - that is, about $7 could be spent on each. From a practical standpoint, however, about $4 to $5 per IC is a better estimate, since that allows for unexpected repairs.

Figure 7.1.3-1 shows relative cost estimates for various part classes. It can be seen that the most effective screen is class B of MIL-STD-883.

Table 7.1.3-3 lists all the required screens for classes S, B and C of MIL-STD-883, Method 5004. (Note that a burn-in test is required for classes S and B only.) The effectiveness of these screens is shown in Table 7.1.3-4. Finally, the cost ranges of screening tests for class B devices are listed in Table 7.1.3-5.

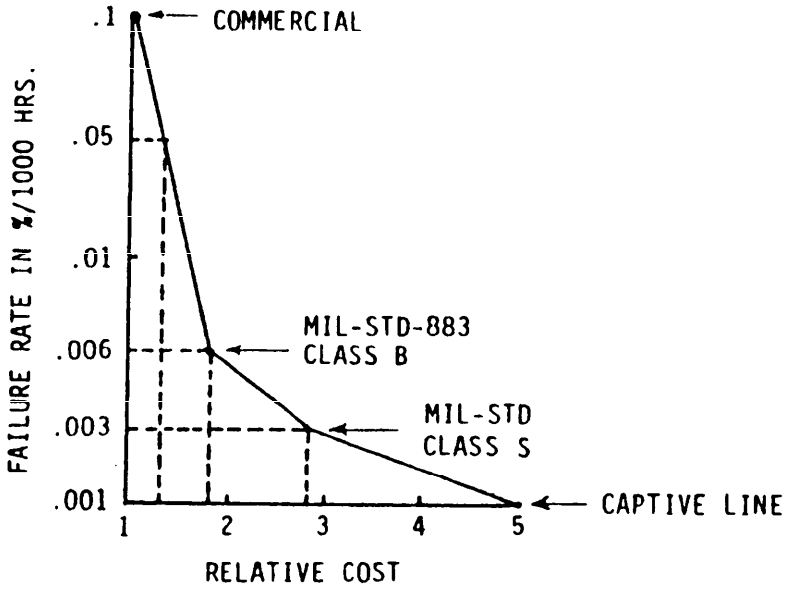


FIGURE 7.1.3-1: SCREENING COST EFFECTIVENESS

TABLE 7.1.3-3: SCREENING SEQUENCE - METHOD 5004 - MIL-STD-883

Screen	S	B
Internal Visual	Condition A	Condition B
Stabilization Bake	24 hrs	24 hrs
Temperature Cycling	10 cycles	10 cycles
Constant Acceleration	30,000 g	30,000 g
Particle Impact Noise Detection	yes	no
Hermeticity (Fine and Gross)	yes	yes
Interim Electrical Parameters	yes	no
Burn-in	168 + 72 hrs	168 hrs
Final Electrical Parameters @ 55°C	yes	yes
Final Electrical Parameters @ Max. and Min. Temperature	yes	no
X-Ray Radiograph	yes	no
External Visual	yes	yes

High quality level microcircuits should be procured per MIL-M-38510. This

TABLE 7.1.3-4: FALLOUT FROM MIL-STD-883 TESTS

Screen	Average % Fallout	Range (%)
Precap Visual	15	2.0-24
Hermeticity	5	0.1-10
Burn-in	3	0.1-20
Electrical Testing	5	1.3-12
External Visual	4	0.1- 8

TABLE 7.1.3-5: SCREENING TEST COST FOR CLASS B DEVICES

MIL-STD-883 Method	Cost in Dollars ($)		
	Min.	Typical	Max.
1) Precap Visual Inspection Condition B	0.15	0.25	3.00
2) High-Temperature Storage	0.01	0.05	0.10
3) Temperature Cycling	0.05	0.10	0.10
4) Constant Acceleration	0.05	0.10	0.25
5) Fine Leak	0.05	0.10	0.25
6) Gross Leak	0.05	0.10	0.20
7) Burn-in	0.25	0.50	5.00
8) Final Electrical	0.25	0.50	2.00
Total Class B	0.86	1.70	10.90

Note that Table 7.1.3-5 screening costs are provided for comparative purposes only. The intent is to illustrate relative cost differences (up to 20 to 1) for screening tests on devices of varying complexity. For a simple integrated circuit logic gate, screening tests will be lower. For LSI devices, the cost will approach the maximum indicated.

7.2 MICROCIRCUIT TESTING

Integrated circuit testing is necessary to insure that a circuit operates as specified. Testing is necessary at all stages of design, implementation and use. As with most engineering tools, it is usually necessary to optimize a test sequence based on a set of objectives such as throughput, cost, test efficiency, etc. As a result, one will hear references to screening tests, environmental tests, acceptance tests, characterization tests, etc; each optimized for a specific purpose.

Testing of analog microcircuits is relatively straightforward in most instances. Functionality is easily tested, and performance and quality may be inferred by measuring voltage levels, leakage and drift parameters, thermal characteristics, etc. In the case of linear circuits procured to military specifications, important parameters to be tested may be found on the detailed specification sheets in MIL-M-38510. Designs which depend on circuit parameters not specified in MIL-M-38510 should be avoided.

7.2.1 TESTING CONCEPTS

In a general sense, testing consists of applying a sequence of inputs to a circuit under controlled conditions, observing the output sequence and comparing it with an expected output sequence. Any discrepancy is called an error, and the cause of this error is denoted a physical fault. Faults can be broadly classified as logical, parametric or pattern sensitive.

A logical fault is one which causes a device to appear to implement a logic function other than the intended one. A common example of a logical fault is the "stuck at" model, wherein circuit signals become stuck at logical one (s-a-1) or logical zero (s-a-0). The "stuck-at" model is only capable of modeling static faults. Dynamic and/or intermittent faults are not addressed by this model.

A parametric fault results from a change in the magnitude of a circuit parameter, thereby altering some performance characteristic such as circuit speed, current or voltage. Parametric faults typically occur due to temperature, humidity, leakage, and/or aging.

Pattern sensitive faults are due to topological considerations in that physically adjacent logic elements on a chip interact destructively, resulting in improper outputs. These effects may occur when metallization lines run too close together, when polysilicon insulators are marginally fabricated, etc. Pattern sensitivity is tested for by applying a stimulus to a particular gate or cell, then monitoring physically adjacent gates or cells for undesirable interaction. Pattern sensitivity is somewhat more of a problem in memory chips than in random logic chips.

Classical methods of testing digital microcircuits were developed during the era of small scale integration (SSI). Each component contained a few logic gates. Sufficient pins were available so that complete tests

could be accomplished by applying a stimulus and measuring the response. As medium scale integration (MSI) became common, functional units such as adders, registers and multiplexers were integrated on a single chip. Adequate testing required carefully designed tests and exhaustive testing was becoming impractical.

With the advent of large scale integration (LSI) and very large scale integration (VLSI), exhaustive testing became not only impractical, but in many cases impossible. The problems of testing a single VLSI microcircuit are analogous to the problems of testing a complex system when only the imputs and outputs are accessible. In many cases, proper operation cannot be observed but only inferred.

Test time, data storage requirements and testing effectiveness make it impractical to apply classical test techniques to LSI and VLSI devices. Three basic approaches have evolved for testing these complex devices: logic integrity tests, A.C. (dynamic) tests, and D.C. (static) tests.

7.2.1.1 LOGIC INTEGRITY TESTS

Logic integrity tests are intended to verify that the device is indeed implementing the proper logic functions. Logic integrity testing may be algorithmic, worst case, or exhaustive in nature. Algorithmic tests rely on an algorithm to generate the test vectors. While acceptable for structural logic such as memory arrays, these tests are generally slow and ineffective for random logic devices.

Worst case testing is theoretically sound but difficult or impossible to implement, since no one seems to know what worst case really is. In principle, one could adequately test a device by testing only the worst case conditions. Since worst case conditions are not known with certainty however, the results of such tests are often questionable.

Exhaustive testing involves subjecting a device to all possible combinations of inputs, environmental conditions, etc. While thorough and effective, the extremely long test times involved make this test method relatively cost ineffective. It is seldom used for complex devices.

7.2.1.2 A.C. TESTS

A.C. or dynamic testing represents a compromise between logic integrity tests and D.C. (static) tests both in terms of speed and effectiveness. Dynamic tests typically check for timing and status faults, since they are somewhat more sensitive to circuit anomalies than static parameters.

7.2.1.3 D.C. (STATIC) TESTS

Static tests are the slowest and least effective in terms of identifying bad devices. The static test is only capable of stressing the first few logic levels nearest the package pin; logic gates "internal" to the chip are never stressed and therefore are not tested. In spite of these

limitations, static tests are sometimes useful for monitoring process control and testing for certain types of failure mechanisms such as surface contamination, which typically manifests itself through excessive leakage currents.

Due to differences in function and implementation, different testing techniques have developed for memory arrays than for random logic devices such as microprocessors. For this reason memory testing and LSI logic testing will be addressed separately in the following paragraphs.

7.2.2 MEMORY TESTING

The fact that memory circuits are usually implemented as structured arrays makes these devices well suited to tests implemented by algorithmic generation of test patterns. For example, by simply incrementing the address counter, a test signal may be sequentially routed to each cell of a memory device. Structured logic, coupled with the fact that memories have relatively few logic gates between input and output, allow for a high degree of testability in memories. The following is a brief summary of the common test algorithms for microcircuit memory devices:

o Write/Read Ones and Zeros (N Type). This is the simplest of all memory test patterns, and, though widely used, it is of limited value. A memory array could conceivably have totally nonfunctional decoders with only one cell permanently selected and still pass this test. For this test, starting at location #1, write a one into the location, then read the contents of the location back to insure that it is indeed a one. Proceed through each cell of the memory in this fashion. Then starting back at location #1, write a zero into each location then read it back to insure that it is indeed a zero.

Alternatively, all memory cell locations can be written to one, then all locations read to insure that each contains a one, and conversely all locations are written to zero, then read to insure that all are in fact zero.

An interesting use for this test algorithm has recently been found in failure analysis using SEM voltage contrast techniques.

o Walking Ones and Zeros. All memory locations are written to a background pattern of zeros. Then, starting with the first location, a test word of one is written in. The rest of the memory is scanned to make sure every other location still contains a zero. The test word one is read, then written back to zero. The test word one is now written in the second location and the sequence repeated. After the last location has been tested, a background pattern of ones is written, a zero is used as a test word at each location, and the entire process is repeated. Overall this results in $2(N^2 + 4N)$ tests, (i.e., this is an N^2 test, since for N large the N^2 term will dominate). This test is good for checking DC pattern sensitivity, proper address operation and functionality but is not a good test of access time, since data transitions during the read cycles are infrequent.

o Marching Ones & Zeros (N Type). The memory is first written to an all 0's state; then, sequentially, a zero is read and a one is written and read at each address. After the last location is reached, and starting at the last location, a one is read and a zero is written. This is continued backward to the first location. Then the sequence is repeated with the data reversed.

This algorithm will check for device functionality including correct operation of the addressing circuitry, along with some limited testing for transition sensitivity.

o Galloping Ones and Zeros (GALPAT) (N^2 -Type). Initially all locations are written to background patterns of zeros. Then, starting with the first location, a test word of one is written, followed by a sequence of read location two, read location one, read location 3, read location one, etc., through the entire memory. When this is complete, the test word is moved to the second location, etc. When the entire memory has been checked in this manner, the data pattern is reversed and the process is repeated.

GALPAT is one test pattern that includes testing all possible addresses. The alternating data output during successive read cycles allows for access time measurements. In fact, GALPAT is a very fine overall testing algorithm, its major limitation being the excessive time and cost required to carry out the testing, since this test is of the N^2 type.

o Checkerboard (N-Type). The memory is filled by writing in alternate ones and zeros. The contents of the memory are read twice, once by rows, once by columns. The inverse checkerboard pattern is written and the reads are repeated.

o Full Ping-Pong (N^2 - Type). Starting with a field of zeros, the test bit (one) is written into the first location. A ping-pong fashion read is then performed between the test bit and every other location of the memory. Upon completion the test location is returned to zero and the next location in the memory is written to a one. The read cycle is repeated. This process is continued until the entire memory is tested. The entire process is then repeated for a test bit of zero in a background of ones.

o Row/Column Ping-Pong ($N^{3/2}$ - Type). A modification of full ping-pong wherein only those memory elements in the same row or column as the test bit are included in the read cycle. This significantly reduces the length of each read cycle, with (presumably) no loss in test rigor, the assumption being that the probability of pattern sensitivity between a given bit and any other bit not having the same X or Y coordinate is significantly less than that of a location falling in the same row or column as the test bit due to physical location and the underlying mechanism of pattern sensitivity faults.

This test, or modification of it, has been found by some to offer the optimum in a test rigor vs. test cost conflict. This has proven to be the case in actual testing.

The following table (adapted from MD100 Field Application Notes, Macrodata Co.) provides a summary of the relative strengths of some of the more common test methods.

TABLE 7.2.2-1: COMPARISON OF TEST METHODS

	Function-ality	Addressing	Multiple Selection	dc Pattern	Access	Write Recovery	Test Type	Comments
Write/Read 1's/0's	no	no	no	no	no	no	N	better than no test
Marching 1's/0's (read/write forward/backward)	yes	good	poor	poor	poor	poor	N	minimal test, very fast: useful for debugging
Walking 1's/0's (ripple)	yes	good	poor	yes	poor	poor	N^2	most widely used test
Galloping 1's/0's (GALPAT)	yes	excellent	excellent	yes	excellent	poor	N^2	all possible transitions: read-read
Checkerboard	poor	poor	poor	poor	poor	poor	N	standard core memory test
Full Ping Pong	yes	excellent	excellent	yes	excellent	poor	N^2	essentially same as GALPAT
Row/Column Ping Pong	yes	excellent	excellent	yes	excellent	poor	$N^{3/2}$	optimized N^2 type test - same test quality - decrease test time

This list, while not complete, does include most of the more popular algorithms in use at the present time. While the choice of tests must depend on a variety of factors which will vary from case to case, some conclusions can be drawn at the outset:

(1) It is generally agreed that the N^2 algorithms have little to offer in terms of added reliability, as compared with the $N^{3/2}$ type algorithms, with the serious disadvantage of increased test time. These $N^3/2$ methods are often considered optimized versions of the N^2 tests. The following table presents the results of a quantitative study of the cost/effectiveness tradeoffs of the various test types. (They further state that if the N^2 type test were to be considered, they would consume 99% of the total electrical test time with no significant improvement in "hit rate" over the $N^{3/2}$ tests.)

TABLE 7.2.2-2: COMPARISON OF TEST TYPE WITH HIT RATE

Figure of Merit	Complex $N^{3/2}$ (type) Optimized Function/AC	Simple N (type) Cross Function	DC Parametrics
Percent of faulty units found (Hit Rate)	95-97	90	3-5
Percent of total test time utilized	70	5	25

(2) It should be noted that for the smaller memory devices tested at high clock speeds, the handling and socket insertion times can easily exceed the electrical test times and is often the major stumbling block to increased throughput. Thus, the choice of an appropriate test algorithm is only one factor in the development of a screening program which will meet the required standards for testing costs and device throughput. A successful screening program requires evaluation at the system level; the system is no better than its weakest link.

7.2.3 TESTING OF LSI RANDOM LOGIC

LSI technology has provided the means for implementing entire systems on a single chip. The problem of testing a single LSI device is analogous to testing a complex system when only the system inputs and outputs are available. The stimulus must often pass through many logic levels before being observed at an output pin. In some instances the desired outputs may not be observable, but only inferred. Another problem encountered when testing VLSI packages is their generality; the voltage on a particular pin is dependent on past and present inputs to the device. Thus a test consists of getting the device into a particular state, inputting the proper stimulus and monitoring the response.

Testing of LSI and VLSI may be broadly divided into two areas; generation of the tests to be applied, and actual application of the tests. Test vector generation is considered beyond the scope of this treatise. For additional information the reader is referred to the references at the end of this section. Test application techniques will be discussed in the following paragraphs.

Test Application Techniques for LSI/VLSI

o Stored Stimulus - Known Good Device. This test feeds data simultaneously to two devices, the device under test (DUT) and a known good device. The outputs of the two devices are then compared to determine the functionality of the DUT. Two problems with this test are: How is the "goodness" of the known good device determined? How does one insure that it remains "good"? In spite of these problems, this is a commonly used method of testing LSI random logic devices, and has been found useful by OEMs as an inexpensive yet efficient method for testing small to medium quantities of devices. It has the added advantage of versatility in that to change from one device to another requires little more than to change to a new known good device reference chip. Unfortunately this test is not effective for detectng dynamic faults, and also has a tendency to reject many devices which are actually within specifications. Dynamic (A.C.) testing is particularly difficult by this technique.

o Stored Stimulus - Stored Response. In this type of testing a data stream is applied to the input of the DUT, and the output is compared to a "reference" output stored in the memory of the test equipment. This is somewhat similar to the "stored stimulus - known good device" test, except that the reference device has been replaced by the equivalent output of a reference device as stored in memory. This eliminates the problems of insuring that the reference device is and remains "good." The great majority of military components are tested using this technique. While an effective and reliable test, there is a high initial cost involved due to programming, test vector definitions and hardware.

o Signature Testing. In signature testing, the DUT is fed a stimulus generated by a pseudo random bit sequence (PRBS) generator. Outputs of the device are then fed to a feedback shift register as shown in Figure 7.2.3-1. This results in data compression, thereby greatly reducing memory/storage requirements for the tester. By adjusting the size of the shift register, the probability of an undetected fault may be reduced to an acceptable level. The probability of an undetected error is

$$\left(\frac{1}{2^n-1}\right)$$

where n is the number of bits in shift register. This technique has seen much popularity recently, and is being routinely used by companies such as Hewlett Packard in their own warranty repair diagnostic and test equipment.

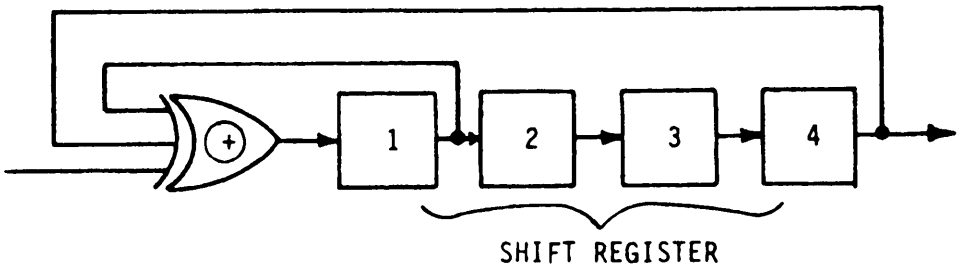


FIGURE 7.2.3-1: TYPICAL SIGNATURE GENERATING ALGORITHM

Algorithmic Testing. In this method, a predetermined sequence of defined patterns is generated by a high speed pattern generator under software control. This allows for significant reductions in memory requirements for the test equipment. Unfortunately the structure of random logic LSI is such that algorithmic patterns tend to be slow and relatively ineffective for testing LSI logic. (These tests are very acceptable for memories however, due to their structural layout.)

Operational Testing. This test method is particularly popular among the smaller OEMs producing limited quantities of uP based systems and faced with tight budgets for reliability/screening tests. Normally this consists of putting the completed system through an exercise cycle which attempts to insure complete functionality. The logic here is "If the system functions properly, then each component must be functioning properly."

This test is cheap and in many cases has proven to be adequate, but it does have several drawbacks. If the system is subject to later modification, it is possible that the modifications will invoke certain steps or memory manipulations which may be at fault but which were never detected, since they were never used in the original system design.

One improvement on this basic test scheme which can be used to advantage is to dedicate an end product system for final testing by adding worst case voltage supplies and a heat chamber. If a ROM serves for program storage, possibly a RAM may be substituted which will exercise all instructions, not just those in the intended application program.

A major disadvantage in this type of testing is the high cost of a failure. As already explained, the cost of a failure can go up as much as an order of magnitude at each level of assembly. The detection of a failure at a system level is more expensive than an efficient screen of incoming components.

REFERENCES

1. Gumaste, U.V. and R.M. Mattheyses. "A Survey of LSI Test Methodology," Rome Air Development Center, RADC-R-79-85, May 1979.

read is then performed between the test bit and every other location of

7.3 MANAGEMENT FOR RELIABLE COMPONENTS

The achievement of reliable military equipment is, in the long run, the result of a successful cooperative effort between the contracting agency whose responsibility it is to clearly define and specify the required reliability, test and operational performance levels of the equipment and the contractor who is responsible for fulfilling the contract goals. An essential ingredient of any successful reliability program is the management procedures employed in the selection and control of electronic parts.

Parts must be properly selected and subsequently controlled to meet the performance and contractural requirements of the program. A weak parts' selection and control activity is frequently the first and most obvious defective element found in a critical evaluation of a contractor's product. When specific parts selection criteria have not been written into the applicable specifications and contract, part selection problems can cause program chaos. It is essential that specific part selection and application guideline documents be referenced in the specification or contract.

During the contract negotiation, phase component reliability requirements must be established and written into the contract. The terms of the contract can best be established by using standard documents (or specifications) to form a basis of understanding during the negotiation phase. Component reliability must be written into the contract at this stage as other elements such as maintainability, safety, logistic supportability, and standardization often will be, especially when a program has as a prior constraint a low life cycle cost.

7.3.1 PART SELECTION AND CONTROL

There are many standard documents which have been prepared for and have grown up with the burgeoning and increasingly complex electronics technologies. There are "standards" that have been written by industry, by or for NASA, by or for the FAA, with the endorsement of and for use in joint NATO efforts, or, perhaps most commonly, those written for DOD efforts. MIL-M-38510, "Microcircuit General Specification," is one of the most widely cited documents of this kind for electronic equipment contractors. Another widely used document is MIL-HDBK-217, "Reliability Prediction of Electronic Equipment," which greatly aids in estimating the field use reliability, given the electronic components to be used and the operating environment, as minimum conditions.

7.3.2 RELIABILITY PROGRAMS

MIL-STD-785, "Reliability Program for Systems and Equipment, Development and Production" provides general requirements and specific tasks for reliability programs during the development, production, and initial deployment of equipment and systems for the Department of Defense. MIL-STD-785 sets forth a number of tasks; all of the tasks or elements thereof may be tailored to meet the needs of a specific program. Included in the tasks of MIL-STD-785 are those unique to the control of all parts, including electronic parts. Two of these tasks are deemed of outstanding importance and should be specified in the acquisition of military equipment and systems. The following description highlights some of the managerial aspects of these two tasks:

o Task 207 relates to a parts control program governing the control, selection and use of both standard and nonstandard parts. Task 207 describes the requirements for establishing a parts control program in accordance with MIL-STD-965, Parts Control Program. The statement of work, SOW, for a given program should include some or all of the details specified below:

(1) Identification of MIL-STD-965 procedure (procedure I or II). Procedure I is preferred by some Service elements; other Service elements prefer Procedure II, particularly as applied to large weapons systems programs. Both procedures relate to the mechanics of parts control when the acquisition contract is awarded.

(2) Identification of the Procurement Activity's part approval procedures and, in particular, times required by both contractor and government elements in submitting and reviewing standard and nonstandard part submissions.

(3) Identification of review procedures with the design activity.

(4) Identification of detailed design guidelines including:

- Order of preference of part quality, reliability and/or screening levels.

- Documentation of prohibited parts and/or materials list.

(5) Contractor/Supplier participation in the GIDEP Program.

o Task 208, Reliability Critical Items provides for the identification and control of those items requiring "special attention" because of high cost, complexity, application of advanced state-of-the-art techniques, and the impact of potential failures on safety, system readiness, mission success or demand for maintenance/logistics support. In accordance with Task 208, the SOW for a given program should include specific identification of reliability critical items such as:

(a) A failure item which: critically affects system safety; causes the system to become unavailable; or causes extensive/expensive maintenance and repair.

(b) A failure which prevents evaluation data from being obtained on system safety, availability, mission success, or the need for maintenance or repair.

(c) An item which has stringent performance requirements relative to the available state-of-the-art.

(d) An item whose sole failure causes overall system failure.

(e) An item stressed in excess of derating guidelines.

(f) An item having a known limited life under shelf, operating or environmental conditions, thus warranting additional control surveillance.

(g) An item requiring special handling, transportation, or test precautions.

(h) An item that is difficult to procure or manufacture relative to the state-of-the-art.

(i) An item that has exhibited unsatisfactory operating history.

(j) An item which does not have sufficient history of its own or sufficient similarity to other items having demonstrated high reliability in order to provide confidence in its reliability.

(k) An item whose past history, nature, function, or processing has a difficiency warranting total traceability.

(l) An item used in large quantities (typically at least 10% of the configured electronic part count).

The incorporation of these two tasks can significantly enhance the reliability management of parts, both electronic and mechanical.

MIL-STD-1635, "Reliability Growth Testing," is another vehicle for defining and monitoring an important element of a reliability program that may be written into a contract. Growth testing techniques often need to be performed for years after a device has been fielded, and thus, monitoring of this growth must be performed as well. Though this activity is often performed above the component level, all that is necessary for component evaluations is a breakdown of the device into homogenous lots.

The parts selection and control program must be required of subcontractors as well as the prime contractor in order to insure proper integration and reliable system performance.

In general, management and control of reliability must be based on a recognition of the component's life cycle; beginning at concept, extending through design and production and ending at removal of the equipment (which contains the component) from inventories. The ultimate objective of the management effort is to achieve acceptable field reliability. Thus, the achievement of an acceptable field reliability for any given system involves numerous tasks which must occur prior to field use:

(a) Accurately predicting and analyzing reliability by developing and applying a reliability model that accounts for design, production and field application factors.

(b) Forcing out defects through a strong aggressive reliability growth program.

(c) Simulating field conditions in R&M performance and demonstration tests.

8.0 LOGISTIC SUPPORT

During the development and production phase of an equipment's life cycle the focus of attention is upon the selection, documentation and application of parts for the purpose of assuring the fabrication of end item equipment which will operate with a high degree of reliability.

However, another aspect of parts control comes to the forefront once the equipment is delivered to the user, namely, those considerations which relate to the logistic support of the equipment. In essence the two factors which most directly affect logistic support are:

(a) the effects of storage on parts
(b) parts provisioning methods

8.1 STORAGE

It has often been assumed in the making of reliability predictions that the failure rate of an electronic equipment and/or it constituent parts is insignificantly small or even zero during the times when the equipment is switched off, deenergized or otherwise nonoperational. Evidence in the field shows otherwise and experimental data indicates that the failure rates of many components are still very significant even when no electrical stresses are applied. This results from the fact that when the electrical stresses are removed, many other stresses such as temperature, acceleration, shock, corrosive influences, humidity, etc., are still present. For example, with semiconductors, temperature has a very marked influence; even at room temperatures, the temperature dependent failure mechanisms within the items are continually active.

For many items, it is possible to extrapolate the electrical stress dependent relationship down to zero stress to obtain a storage failure rate. The results of storage tests tend to verify this fact. For some components, the storage failure rate is even greater than the operating failure rate at the lower stress levels. This is the case for some types of resistors (eg. carbon composition) where, under storage conditions, there is no internal heat generation to eliminate humidity effects. It is also well known that certain types of electrolytic capacitor need a reforming process after a long period of storage. MIL-STD-1131, "Storage Shelf Life and Reforming Procedures for Aluminum Electrolytic Fixed Capacitors," covers the procedures to follow in determining and prolonging the serviceability of aluminum electrolytic capacitors during storage.

Electronic components age and deteriorate over long storage periods due to numerous failure mechanisms. In particular, the electrical contacts of relays, switches, and connectors are susceptible to the formation of oxide or contaminant films or the attraction of particulate matter that adheres to the contact surface, even during normal operation. During active use, the mechanical sliding or wiping action of the contacts is effective in rupturing the films or dislodging the foreign particles in a manner which

produces a manner which produces a generally stable contact surface. However over a long period of nonoperational storage, the contaminant films and/or the diversity of foreign particles may have increased to such an extent that the mechanical wiping forces are insufficient for producing a low resistance contact.

The formation of contaminant films on contact surfaces is dependent on the reactivity of the control material, its history, and the mechanical and chemical properties of the surface regions of the material. Gold is normally used whenever maximum reliability is required, primarily because gold is almost completely free of contaminant oxide films. Even gold, however, is susceptible to the formation of contaminant films by simple condensation of organic vapors, and the deposition of particulate matter. Silver is highly susceptible to the sulfide contaminants that abound in the atmosphere, as are alloys of copper and nickel. Shipping and storage of these systems in paper boxes should be avoided because of the effects of sulfur containing paper. Particulate contamination can also lead to corrosive wear of the contact surfaces when the particle is hygroscopic. With this condition, water will be attracted to the contact surface and can lead to deterioration through corrosive solutions or localized galvanic action. The source of such particles can be directly deposited airborne dust or wear debris from previous operations.

Another failure mode which may become significant after long term storage is the deterioration of lubricants used on the bearing surfaces of relays and solenoids. Lubricants can oxidize and form contamination products. Similarly, lubricants can also attract foreign particles, particularly when exposed to airborne dust, and can lead to lubrication failures and excessive wear.

Over a period of time, many plastics (such as these used in the fabrication of electronic components, i.e., integrated circuits, capacitors, resistors, transistors, etc.) lose plasticizers or other constituents, which may evaporate from the plastic, causing it to become brittle, and possibly shrink. This can cause seals to leak, insulation to break down under electrical/mechanical stress, and other changes conducive to fatigue and failures. Additionally, plastics may continue to polymerize after manufacture. That is, the structure of the molecules may change, without any accompanying change in chemical composition. This will result in change in characteristics and physical properties.

Many materials slowly oxidize, combine with sulfur or other chemicals, or break down, chemically, over a period of time. These changes may take effect when component materials are exposed to condensed moisture, or high humidity conditions, and through a leaching process lose essential ingredients such as fire retardant additives, thereby causing a hazard to slowly develop.

resistance of the conductive paths may be closely controlled by

Many component parts and assemblies are sensitive to contaminants and, thus, are sealed during manufacture. These seals will often leak, partly as a result of flexing due to changing temperature and atmospheric pressure, allowing air, moisture and other contaminants to reach the active portions of the component. This leakage can be so slow that the effects may not be discernible for years, but, ultimately, significant changes can occur.

Finally, the methods/materials of preservation, packaging and packing (PP&P) used in the storage of components and equipment, i.e., cardboards, plastic bags, polystryenes, etc., themselves may react with the items of storage, and cause decomposition and deterioration when left dormant for long durations.

Rough handling during shipment and depot operations, and aging and deterioration mechanisms as discussed above, can, if uncontrolled, lead to a variety of component failure modes. A summary of some of the failure modes encountered with electronic components during storage is given in Table 8.1-1. Protective measures must be applied to isolate the components from these deteriorative influences in order to eliminate or reduce failure modes such as listed in Table 8.1-1.

TABLE 8.1-1: FAILURE MODES ENCOUNTERED WITH ELECTRONIC COMPONENTS DURING STORAGE

COMPONENT	FAILURE MODES
Batteries	Dry batteries have limited shelf life. They become unusable at low temperatures and deteriorate rapidly at temperatures above 35°C. The output of storage batteries drops as low as 10 percent at very low temperatures.
Capacitors	Moisture permeates solid dielectrics and increases losses which may lead to breakdown. Moisture on plates of an air capacitor changes the capacitance.
Coils	Moisture causes changes in inductance and loss in Q. Moisture swells phenolic forms. Wax coverings soften at high temperatures.
Connectors	Corrosion causes poor electrical contact and seizure of mating members. Moisture causes shorting at the ends.

TABLE 8.1-1: FAILURE MODES ENCOUNTERED WITH ELECTRONIC COMPONENTS DURING STORAGE (Cont'd)

COMPONENT	FAILURE MODES
Relays and Solenoids	Corrosion of metal parts causes malfunctioning. Dust and sand damage the contacts. Fungi grows on coils.
Resistors	The values of composition-type fixed resistors drift, and these resistors are not suitable at temperatures above 85°C. Enameled and cement-coated resistors have small pinholes which bleed moisture, accounting for eventual breakdown. Precision wire-wound fixed resistors fail rapidly when exposed to high humidities and to temperatures at about 125°C.
Diodes, Transistors, Microcircuits	Plastic encapsulated devices offer poor hermetic seal resulting in shorts, or opens caused by chemical corrosion or moisture.
Motors, Blowers, and Dynamotors	Swelling and rupture of plastic parts and corrosion of metal parts. Moisture absorption and fungus growth on coils. Sealed bearings are subject to failure.
Plugs, Jacks, Dial-Lamp Sockets, etc.	Corrosion and dirt produce high resistance contacts. Plastic insulation absorbs moisture.
Switches	Metal parts corrode, and plastic bodies and wafers warp owing to moisture absorption.
Transformers	Windings corrode, causing shorts or open circuits.

8.1.1 GENERAL STORAGE CONSIDERATIONS FOR PARTS

The most important environmental forcing functions, or stresses, in storage are mechanical, chemical and low thermal. Mechanical stresses occur due to thermal mechanical interactions and residual stresses. Chemical stresses result from contaminants such as residual process chemicals and environmental gases which are introduced through improper or failed seals. Although purely thermal stresses have much less prominence in storage than in operating environments, certain low temperature reaction rates and diffusion processes are temperature dependent.

o The synergism of the three primary storage stresses is critical. Any one of the three acting alone may not be particularly damaging but the combined effect of two or three forcing functions acting together is likely to cause device failures.

o Environmental extremes for military equipment (for example, missiles) in storage have included temperatures of -50°C to +75°C, twice daily cycling to 70°C, 100 percent relative humidity, direct sea spray, industrial pollutants, some mechanical shock and fungus. Climatic extremes in which military equipment is designed to operate, or to withstand in a non-operating mode, are specified in MIL-STD-210.

o The failure mechanisms of greatest importance in storage have been identified as those related to various marginal manufacturing mistakes, corrosion processes and mechanical fracture. Electrical or potential current induced degradation processes are not important in the storage environment. Moisture within a package is probably the most important contributing factor for both corrosion and mechanically induced failures in storage. Chemicals, including moisture trapped within a package due to improper cleaning or because of evolution from materials such as polymers, are a critical concern for long term reliability. The package seal is critical for keeping out atmospheric contaminants. Thermal mechanical stresses aided by chemical agents can cause crack propagation in seals, passivation layers, bonds, metallization layers and the silicon chip.

o The presence of defects such as impurities, dislocations, microcracks, interfacial faults and grain boundaries in the materials of a microcircuit structure can result in failure due to low temperature atomic diffusion processes.

o Particulate matter within the microcircuit enclosure is one of the dominant concerns as a storage failure mechanism.

o The hermeticity of microelectronic packages is an important concern for long term storage conditions. The MIL-STD-883 screen test for determining the effectiveness of hermeticity of package seals includes a fine leak rate test. The maximum allowable leak rate specified for this test should be lowered to 10^{-10} atm/cm^3/sec^{-1} for devices that are expected to be stored because of the exchange of gases between the initial package ambient and the external storage environment in packages with a finite size leak.

o The fields across a thin gate oxide in MOS devices can often approach the dielectric strength of the oxide. However, because of various factors that are not easily controlled the breakdown voltages have a range of values. Consequently, any application of potentials to the gate electrode can be a possible cause of oxide breakdown, particularly when static charging is not avoided or if there are voltage transients present in ground test equipment.

o Whenever polymeric materials are employed for die attach within hybrid microcircuit packages, they must be proved compatible with all enclosed electronic materials. No chlorine or other halogen containing materials should be sealed in any circuitry components. Polymers used should be simple hydrocarbons or compounds of carbon, hydrogen and oxygen. Nitrogen containing polymers should be considered with skepticism. The responsibility for proof of compatibility should be with the hybrid device manufacturer for specific epoxies and circuit element combinations.

o Equipment placed in storage should never contain electronic parts employing polymers for package seals. Polymers will transmit moisture and other gases.

o Screening and accelerated testing procedures for electronic equipment must be based upon consideration of potential part storage failure processes.

o There is widespread controversy about the optimum number of cycles in a temperature cycling screen test. Opinions vary from 25-300 cycles for effective screening. The use of only 10 cycles is not considered to be of any value.

o High temperature burn-in is a relatively effective screen for failure modes having high activation energies. For oxide defects the failure mode has a much lower activation energy. The high temperature burn-in is then not particularly useful. An over voltage stress is recommended for screening MOS devices for oxide defects.

o All microcircuit packages should be vacuum baked at 150^{o}C for at least 4 hours and sealed in dry nitrogen without ever being exposed to moisture containing gases such as air. The moisture content of the nitrogen sealing chamber should be less than 100 ppm.

8.1.2 MICROCIRCUIT STORAGE CHARACTERISTICS

Data shows that the incidence of failure of devices in a stored, nonoperating condition is considerably higher in those devices which incorporate different metals in their metallization layer and in their lead wires. In particular, the aluminum (Al) metallization, gold (Au) wire device is much more subject to wirebond failure than is the Al metallization, Al wire device.

Storage data which includes field data from four missile programs and one laboratory environment test exists; this data was recorded from 1967 through 1970, and represents identifiable information on monolithic digital devices fabricated with aluminum metallization and gold wires (Al/Au) and devices with gold metallization and gold wire (Au/Au).

Out of 2.7 billion part storage hours, 85 failures were reported for the Al/Au devices. No failure modes or mechanisms are known other than the fact that the failures were catastrophic and not drift related. More recent data is available on Al/Au hybrid devices showing the same relatively high failure rate with wire bonds being the major problem.

Table 8.1.2-1 illustrates the principal failure mechanisms and their relative frequency of occurrence for both the Al/Al and the Al/Au type monolithic, digital and linear microcircuits.

TABLE 8.1.2-1: PRINCIPAL FAILURE MECHANISMS FOR DIGITAL AND LINEAR DEVICES

(Aluminum Metallization, Aluminum Wire, Gold Post)	
Mode or Mechanism	%
Oxide Defects	31
Wire Bond	19
Diffusion Defects	16
Surface Inversion	13
Al/Au Post Bond	12
Die Bond	3
Lead Failures	6
(Aluminum Metallization, Gold Wire, Gold Post)	
Mode or Mechanism	%
Wire Bond	76
Resistive Output	15
Oxide Defects	4
Die Bond	2
Wire Shore	2
Cracked Die	2

Tables 8.1.2-2 and 8.1.2-3 show failure modes and mechanisms and their incidence of occurrence for MOS SSI/MSI devices and memory/LSI devices, respectively.

TABLE 8.1.2-2: MOS SSI/MSI DEVICE REPORTED FAILURE MODES & MECHANISMS

Mode or Mechanism	%
Drift	9.4
Open	18.9
Short	1.9
Field Oxide Short	1.9
Gate Oxide Short	3.8
Lid Seal Defective	1.9
Al Wire Bond Defects	3.8
Au Ball Bond Defects	10.8
Al/Au Kirkendall Voids	3.8
Die Bond Defect	1.9
Resistive Junction	1.9
Contamination	34.2
Foreign Particles	3.8

TABLE 8.1.2-3: MEMORY/LSI REPORTED FAILURE MODES AND MECHANISMS

Device Type	Mode or Mechanism	%
RAMS/LSI - Al Metal/Al Wire	Oxide Pinhole	3.4
	Gate Oxide Pinhole	30.6
	Field Oxide Pinhole	1.7
	Contamination	3.4
RAMS/LSI - Al Metal/Au Wire	Gate Oxide Pinhole	3.4
	Field Oxide Pinhole	1.7
	Contamination	52.7
ROMS/LSI - Al Metal/Al Wire	Wire Bond Defects	3.4
ROMS/LSI - Al Metal/Au Wire	None Reported	0.0

8.1.3 DISCRETE SEMICONDUCTORS STORAGE CHARACTERISTICS

Discrete transistors and diodes have failure modes and mechanisms similar to those discussed above for microcircuits. They also have in common the same causes, accelerating environments and detection methods for failure modes and mechanisms. However, there are differences between discrete devices and microcircuits which affect their nonoperating failure rates.

As in the case with all semiconductors, transistors do not appear to have failure mechanisms inherent to the concept of the device. All of the mechanisms are initiated by deficiencies in the materials and fabrication processes used during manufacture of the devices.

The difference between discrete transistors and integrated circuits lies in the physical size and number and complexity of manufacturing processes. Compared to the average integrated circuit, a transistor is a relatively simple device. There are fewer numbers of functions and leads. The distances between different parts of the device are larger. The manufacturing processes are fewer and simpler. Although the failure mechanisms are similar to those in integrated circuits, the above differences tend to shift their emphasis. Bulk defects are more common due to the larger blocks of silicon required, thus increasing the probability of crystal imperfections. Imperfections collect mobilized contaminants resulting in breakdown, leakage, gain failures and, in high power devices, thermal runaway. Diffusion defects are not as critical due to the lower density of diffusions. Oxide and metallization defects are not as pronounced as in integrated circuits because the metallization patterns are much simpler.

A large percentage of transistor failures are the result of die and wire bonding defects. Contamination, both ambient and within the material, is also a serious problem in transistors.

As noted before, the failure mechanisms, causes, accelerating environments and detection methods of diodes are similar to those found in transistors. In addition to those mechanisms, alloy bonded and point contact diodes can develop intermetallic compounds at the junction; however, this has not been observed to be a severe problem. Loss of contact is also a potential problem in spring loaded contacts. This happens when the contact material loses its compression strength or slips off the contact.

8.1.4 RESISTOR STORAGE ENVIRONMENTS

o Failure Mechanisms. Most resistors are encapsulated in a molded plastic case or conformally coated to provide moisture protection. However, plastic does not provide hermetic sealing, so moisture is a reliability consideration for most resistors. A carbon composition resistor will usually keep itself dry during operation because of its self generated heat and heat from adjacent components. Long time storage of carbon composition resistors without operation in a humid atmosphere will result in an appreciable increase of resistance. Also, long time storage in a very dry atmosphere will result in the reverse resistance change. These effects are reduced or eliminated if the composition resistors are potted or hermetically sealed into higher order assemblies.

The effect of moisture on film resistors varies according to type. Corrosion or electrolytic action involving impurities or surface contaminants is a major cause of open circuits in the film or between the film and end cap connections. Reduced resistance from this effect prior to final malfunction is frequently hard to detect because of the common localized nature of the effect. Moisture absorbed during nonoperating storage frequently does not cause serious trouble until after a period of operation with voltage applied to stimulate electrolysis.

Moisture in wirewound resistors is frequently a cause for leakage between turns and between layers which ultimately results in insulation breakdown and shorts. Corrosion and electrolytic action results in open wires or in openings between resistor wire and end cap connections.

Potentiometers cannot be sealed in a completely encapsulated jacket. Even where the resistor element is encased in a plastic or vitreous case there must be a portion of each turn exposed for contact with the wiper arm. This provides many possible points (which can seldom be fully sealed) for the entrance of moisture.

Operator adjusted potentiometers must have movable shafts which protrude through the case and front panel. This opens the interior of the potentiometer to the exterior environment. Various types of shaft seals such as Elastomer "O" rings are at best imperfect moisture seals.

Interior mounted trimmer potentiometers are given some shelter and moisture protection by the external case, but even these can seldom be potted or hermetically sealed inside a higher order assembly unit.

Potentiometers have additional failure modes relating to the wiper which are affected by moisture. Precision potentiometers may degrade in linearity or noise as a result of moisture absorption and corrosion.

8.1.5 CAPACITOR STORAGE CHARACTERISTICS

Capacitors are susceptible to water vapor. Even in hermetically sealed units, moisture present during manufacturer can lead to deterioration of insulation or dielectric materials. This can be a more serious consideration in certain poorer grade capacitors.

The entrance of moisture through cracks in the seals can be minimized in several ways. Capacitors with seal cracks prior to installation in equipment should be screened out and removed from manufacturing stock. Cracks developed during assembly into equipment can be prevented by careful process control and sometimes can be screened out by final assembly inspection. Cracks which develop during use in later life of the equipment can sometimes be traced to low quality seals or stresses placed on the leads during equipment manufacture. Certain seal cracks are traceable to a combination of these causes plus stress resulting from operation.

Electrolytic capacitors have experienced problems in storage. Table 8.1.5-1 summarizes the predominant failure mechanism associated with solid tantalum capacitors. Table 8.1.5-2 summarizes those for wet tantalum capacitors. Electrolyte leakage in the wet tantalum capacitor has been the major source of problems, while impurities in the solid tantalum capacitor has caused problems. Most of the failure mechanisms associated with these capacitors are accelerated to failure by a temperature cycling environment. Continuing R&D on these devices in recent years has brought about a significant increase in reliability.

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TABLE 8.1.5-1: FAILURE MECHANISM ANALYSIS, SOLID TANTALUM CAPACITORS

Failure Mechanism	Cause	Accelerating Environment	Failure Mode	Detection Method
Oxide Defects	Impurities in starting tantalum impede oxide growth at sites during anodization.	Temperature cycling, burn in, surge test	Out-of-tolerance	High leakage currents, or outliers
	Abrasions of sintered pellets expose impurities prior to anodization.			
	Binder or die impurities on sintered pellet.			
	Handling damage during anodization processes and assembly.			
	Crystalline tantalum pentoxide.			
	Oxide shorts due to excessive power surges under flicker or scintillation conditions.	Surge test	Short	Short circuits
	Thin MnO_2 pr silver paint penetrating MnO_2 and preventing healing or defect sites.	Temperature cycling, burn in, surge test	Out-of-tolerance	High leakage currents, or outliers. High dissipation factor.
Poor Slug Adhesion	Inadequate wetting of solder to silver paint.	Temperature cycling, burn in	Out-of-tolerance	Dissipating, capacitance, radiographic inspection
	Silver paint dissolving into the solder.			
	Low solder level, poor anchorage of slug to case, flux between solder and paint.	Temperature cycling, burn in		Radiographic inspection
Solder Reflow	Excessive heat applied during assembly of capacitor into circuit.			Radiographic inspection
Mechanical Defects	Solder distributions, voids, slugs canted in case, bent risers, etc.	Shock, vibration	Out-of-tolerance, open, shorts	Radiographic inspection

TABLE 8.1.5-2: FAILURE MECHANISM ANALYSIS, TANTALUM FOIL CAPACITORS

Failure Mechanism	Cause	Accelerating Environment	Failure Mode	Detection Method
Electrolyte Leakage	Leakage past center of seal causing electrolyte to bridge between internal nickel wire and case.	Temperature cycling, burn in	Shorts, open capacitance, leakage	Visual inspection, electrical test
Insulation Defects	Metallic contamination in mylar sleeving, improperly cured epoxy compound	Temperature cycling, burn in	Short, dissipation factor	Electrical Test
Foil Separation	Reactive impurities in electrolyte or in paper spacer	Temperature cycling, burn in	Capacitance, dissipation factor	Electrical Test
Faulty Lead to Foil Welds	Machine and operator errors cause inadequate welds	Temperature cycling, burn in	Open	Visual, electrical test

8.1.6 INDUCTIVE DEVICE STORAGE CHARACTERISTICS

o Failure Modes. The most common failure modes for inductive devices are shorts and opens. Shorts usually are the result of breakdown of insulation. During operation, breakdown of insultion is normally the result of over voltage and current developing hot spots. This leads to embrittlement and degradation resulting in ultimate breakdown. During storage, this is the result of chemical changes and deterioration accelerated by temperature, humidity and reactions with atmosphere gases.

Opens result from the breaking of fine winding wire. Unless caused by mechanical shock or stresses opens are normally associated with manufacturing problems such as stress in relief loops, wire nicks, and soldering of lead wires to the windings.

Failure modes are also accelerated by use conditions. The effects of various use and storage conditions on coils and transformers are summarized in Table 8.1.6-1.

FIGURE 8.1.6-1: FAILURE MODES AFFECTED BY VARIOUS USE AND STORAGE CONDITIONS

Component	Vibration Effects	Shock Effects	Temperature Effects	Humidity Effects	Salt Spray Effects	Storage Effects
Transformers	Shorts: opens; modulation of output	Shorts; opens; modulation of output	Reduced dielectric; opens; shorts; hot spots; malformation	Corrosion; fungus shorts; opens	Corrosion; shorts;	Deterioration of potting and dielectric
Coils	Loss of sensitivity detuning; breaking of parts, leads, and connectors	Lead breakage; detuning; loss of sensitivity	Warping, melting; instability; change in dielectric properties	Electrolysis; corrosion	Corrosion; electrolysis	

quartz dielectric cylinders and metal tubing ... construction of glass or

8.1.7 PRINTED CIRCUIT STORAGE CHARACTERISTICS

o Failure Mechanisms. Printed circuits have a dominant failure mechanism which imposes a definite limitation on life. It is caused by the difference in the thermal coefficient of expansion of the substrate and the plated copper. The copper yields to accomodate temperature changes, but eventually a fatigue failure causes an open circuit, usually in one of the plated through holes. Use of very pure copper and control of the cross section help to extend the life.

The operational failure rate of a multilayer board with 100 holes, in a ground environment, is 100 failures per billion hours on the average.

8.1.8 PROTECTION METHODS

Proper protection against damage and deterioration to components and equipment during shipment and storage involves the evaluation of a large number of interactive factors and the use of tradeoff analysis to arrive at a cost effective combination of protective controls. These factors can be grouped into three major control parameters: (1) the level of preservation, packaging and packing (PP&P) applied during the preparation of material items for shipment and storage; (2) the actual storage environment; and (3) the need and frequency of in-storage cyclic inspection. These parameters must be evaluated and balanced to meet the specific characteristics of the individual equipment and materiel items. The significance of each of the three parameters is as follows:

(1) Preservation, packaging and packing (PP&P) is the protection provided in the preparation of materiel items for shipment and long term storage. Preservation is the process of treating the corrosible surfaces of a material with an unbroken film of oil, grease, or plastic to exclude moisture. Packaging provides physical protection and safeguards the preservative. In general, sealed packaging should be provided for equipment, spare parts, and replacement units shipped and placed in storage. Packing is the process of using the proper exterior container to ensure safe transportation and storage.

Various levels of PP&P can be applied, ranging from complete protection against direct exposure to all extremes of climatic, terrain, operational, and transportation environments (without protection other than that provided by the PP&P) to protection against damage only under favorable conditions of shipment, handling, and storage. A military package as defined per MIL-E-17555 is the degree of preservation and packing which will afford adequate protection against corrosion, deterioration, and physical damage during shipment, handling, indeterminate storage, and world wide redistribution. A minimum military package is the degree of preservation and packaging which will afford adequate protection against corrosion, deterioration and physical damage during shipment from supply source to the first receiving activity, for immediate use or controlled humidity storage. Many times a minimum military package conforms to the supplier's commercial practice.

(2) The storage environment can vary widely in terms of protection afforded. However, whenever possible electronic hardware should be stored in dry, well ventilated warehouses, where the temperature of the air surrounding the equipment can be regulated so that it does not fall to dewpoint values at night. Storage in controlled temperature/humidity buildings is of course ideal. If parts or equipment are stored in bins, it is important that the bins be placed above floor level. The military has several types of storage areas. These include warehouse space with complete temperature and humidity control, warehouse space with no humidity and temperature control, sheds, and open ground areas that are simply designated for storage.

(3) In-storage scheduled cyclic inspection is the key to assuring the actual reliability of components and equipment during storage. In-storage cycling inspections are designed to detect performance degradation, deterioration, and other deficiencies caused by extended periods of storage and improper storage methods. The inspections are to identify those items which require corrective packaging (or further storage control) or condition reclassification to a lesser degree of serviceability. The inspections are performed at intervals derived from shelf life periods and the level of protective packaging and storage afforded to material items. It should be noted that all items when originally placed in storage are ready for issue and that all applicable preservation, packaging and packing (PP&P) requirements have been met. In-storage cycling inspection is part of the depot's overall inspection system that includes inspection of items at receipt as well as prior to use.

In general, shipment and storage degradation can be controlled in terms of the above mentioned three parameters. The planning and specification of shipment and storage requirements for new component and equipment items (as well as the reestablishment of requirements for existing items in storage) must take into account economic choices between the various factors within these parameters to arrive at the most cost effective balance that meets reliability and readiness objectives.

8.2 SPARE PARTS PROVISIONING

During the operational phase of the equipment/system life cycle, spare and repair parts are necessary to insure that prompt repairs can be made to a subassembly, assembly or end item equipment. It is imperative, therefore, that when repair is made, the spare and repair parts used are of at least the same quality and reliability as those used during the development and production phase.

8.2.1 CONTROL OF PARTS IN MILITARY DEPLOYED EQUIPMENT/SYSTEMS

In most military equipment/systems deployed in the field, the Defense Electronics Supply Center, DESC, Dayton, Ohio, purchases the bulk of electronic spare and repair parts for all Services. Notable exceptions to this policy are those electronic parts which are repairable, are classified for security reasons, or are parts particularly unique to a given service. In the Navy Department, for example, electronic parts peculiar to Navy applications are procured by Navy Ships Parts Control Center, Mechanicsburg, PA.

In the procurement of electronic spare and repair parts, DESC invokes Defense Contract Administration Services or DCAS inspection requirements for many electronic parts. In the case of discrete semiconductor devices, DESC has an in-house capability and performs incoming Group A inspection to a given Lot Tolerance Percent Defective, LTPD, required under the MIL-S-19500 specification slash sheet for the particular device. Additionally, a similar incoming audit is also applied to all microcircuits procured to MIL-M-38510 specification slash sheets.

DESC, therefore, acts as the focal point in procuring electronic, spare and repair parts with the exceptions previously noted. Field repair activities and depots in turn requisition the needed field spare and repair parts from DESC. This procedure provides assurance that electronic spare and repair parts are of the quality and reliability levels paralleling closely those depicted in drawings and specifications during the development and production phase.

8.2.1.1 CONTROL OF PARTS IN MAJOR WEAPONS SYSTEMS

Some major weapons systems having high reliability requirements and controlled by a Project Manager or Strategic Project Office (SPO) may apply parts control during deployment under the control and direction of these offices. In order to insure that spare and repair parts are procured to the hi-reliability specifications of the major weapons systems program, the following options are applied:

(1) Spare and repair parts can be procured from the equipment/system producer to the quality, reliability and levels of preconditioning and burn-in specified in the original procurement.

(2) Spare and repair parts can be procured through the Project Office, and a government activity or installation may perform the pre-conditioning and burn-in necessary to insure reliable field performance.

In either of the above cases parts assurance control is maintained by these special activites.

8.2.1.2 AIR FORCE SPARES REQUIREMENTS

Requirements for spares and spare parts within the Air Force supply system are given in AFLC Manual 800-1, Chapter 31. This chapter stipulates that there are two channels through which spares are acquired by new procurement, contingent upon the type of support authorized for the item(s) involved: initial spare parts support or replenishment spares support. Initial spares (except initial GFAE spares) are procured from the contractor producing the system or end item of equipment to be supported and include items the contractor fabricates plus those obtained from his subcontractors and vendors. Procurement of replenishment spares (except items of GFAE procured on separate contract) will be procured competitively from the commodity industry to the maximum extent practicable, except when the total package procurement concept is utilized.

o Initial Spares/Repair Parts. Initial spares/repair parts (except items of GFAE procured on separate contract) are selected, identified, and procured against the production contract. The provisioning process includes the technique of obtaining documentation, data, drawings, etc., from the contractor in a prescribed form for use in the identification of items and the determination of initial spares/repair parts required to support the production item during its initial phase of service.

A Provisioning Plan and a Statement of Provisioning Policy are included in the request for proposal (RFP), invitation for bid (IFB) or request for quote (RFQ) and incorporated into the contract at the time of the contract award. These contractual items permit the contractor, together with the contracting agency to plan and execute the provisions, terms and requirements of the contractual provisioning documents included in the contract. In addition, the contractor is provided a programming checklist which reflects the programming data for the end item under contract. This data permits the contractor to intelligently forecast an interim release to production and procurement, or recommend for procurement, items and quantities required for logistics support during the initial deployment phase.

o Replenishment Spares. Replenishment spares are normally procured on separate AFLC contracts. These spares requirements cover support beyond the initial support period, and are progressively computed throughout the program life of the system or end item of equipment.

Recoverable type items are computed against programs tailored to fit the exact application of the items. Programs consider the total projected inventory of a specific system or end item of equipment resulting from the input of all production contracts as opposed to the initial spares program which only considers the input of a specific contract quantity.

Projected programs used in computations are in quarterly increments by fiscal year. The elements of programs used are operating hours, population or inventory, missile months, launches, overhauls, and recoveries. Individual items are related to the specific element of programming which is the major cause of item usage.

Computations are made on a scheduled cycle basis with annual procurement made to cover one year's operating support where necessary.

Nonrecoverable items (items which are consumed in their use or items whose physical characteristics and/or unit cost make it uneconomical to return to the depot system for repair) are under an economic order and stockage program with procurement made of economic order quantities. No elements of projected activity are used in computing requirements although management considerations are given to any sharp program trend, such as phaseout of end article on which the item is used, before release of procurement is made. The dollar value of the average annual demands for the item determines the level of procurement.

8.2.2 SPARES PROVISIONING TECHNIQUES

Spares provisioning is a complicated procedure which is influenced by many considerations, such as cost of spares, level of maintenance required, the type of system which the spare parts support (i.e., whether the equipment uses a high percentage of complex ICs or a high percentage of discrete parts), modular or nonmodular construction, the number of systems to be supported, and in particular, the mission of the system.

It is quite obvious, for example, that spares provisioning for equipment used in nuclear submarines during whose 4-5 month underseas voyages no repair work is undertaken and equipment failure is overcome by the replacement of complete assemblies or modules, or for unmanned space vehicles where neither replacement nor repair of equipment is possible, differs from that for land based equipment which is easily accessible for repair. It is also apparent that the level of replacement or repair required (i.e., whether it be for a failed assembly, module or part) and the need for and availability of automatic test equipment, are all factors which have a strong influence on the spares provisioning methods and levels that are used.

Techniques for determining the most desirable levels of spares provisioning vary according to the complexity of the system support problem and the costs associated therewith. The following material demonstrates not only the complexity of a spares problem (and its inextricable connection with an adequate repair facility) but also provides an example of an effective, cost sensitive technique for dealing with it.

8.2.2.1 OPTIMIZATION OF SPARES AND MAINTENANCE FACILITIES

Hard on the heels of the question "Can we afford to buy it?" comes the question "If we buy it, can we afford to keep it?" When the Life Cycle Cost (LCC) of military avionic equipment is added up, the upkeep cost invariably exceeds the equipment purchase cost. If the LCC is considered in three areas: cost to purchase, cost to operate and cost to maintain; estimation of the first two cost areas can be made with reasonably close tolerances whereas the cost to maintain is often subject to wide variance. This is due in part to the uncertainty attached to the estimated number of unscheduled maintenance actions, but is mostly due to the servicing policy options.

Among the military, the cost saving achievable by optimizing the servicing policy is fully appreciated, and studies have developed techniques for trading off possible servicing policy options. Factors in the tradeoff include the number of equipments in service, total expected life, failure rate of replaceable parts and cost of spares.

The following discussion deals with just two of the factors contributing to the LCC, namely, the cost of providing an adequate spares backing and the cost of providing an adequate repair facility. The definition of "adequate" is itself a significant factor in the LCC.

8.2.2.1.1 THE PROBLEM

To tie the techniques presented below to a practical application, consider an airborne radar set designed for ease of maintenance comprising the plug-in assemblies shown, together with their associated failure rates, in Table 8.2.2.1.1-1. For convenience, the mean-time-between-failures (MTBF) is given, being the reciprocal of the failure rate.

TABLE 8.2.2.1.1-1: RADAR MAIN ASSEMBLIES

Main Assembly	QTY	MTBF
Unit 1	1	4000 hours
Unit 2	1	1000 hours
Unit 3	1	200 hours
Unit 4	1	250 hours
Unit 5	1	400 hours
Unit 6	1	223 hours
Unit 7	1	2000 hours
Unit 8	1	4000 hours
Unit 9	1	2000 hours
RADAR (Total)		54 hours

Within the main assemblies, the design concept is plug-in modules. The large majority of these are printed wiring boards (PWB), and the greater number of PWBs contain digital, SSI, MSI and LSI microcircuits.

The boards fall roughly into three groups:

Group A, mostly SSI and some MSI
Group B, mostly MSI and some LSI
Group C, mostly LSI (memory arrays, microprocessors, etc.)

Table 8.2.2.1.1-2 gives the quantities and MTBF of each group.

TABLE 8.2.2.1.1-2: DIGITAL PWB QUANTITIES

Group	QTY	MTBF (each)
A	65	50,000 hours
B	45	17,000 hours
C	10	5,000 hours

The total number of aircraft in service is 400 and the equipment life is 10 years, during which time it will accumulate 8000 operating hours.

The aircraft will be operated from ten airfields, with 40 aircraft at each field. The servicing policy is described in Table 8.2.2.1.1-3.

TABLE 8.2.2.1.1-3: SERVICING POLICY

Location	Diagnosis	Action
Aircraft Dispersal Point	BITE, GTE	Remove and replace assembly. Send failed unit to airfield repair.
Airfield Repair Section	ATE, hand tools	Remove and replace module, send failed unit to Central MU.
Central Maintenace Unit	ATE, hand tools	Remove and replace failed component OR return failed item to manufacturer.
Manufacturer	Production test gear	Repair or remake failed unit.

BITE, Built-In Test Equipment (in the radar)
GTE, Ground Test Equipment (plug-in to aircraft, or carry-on)
ATE, Automatic Test Equipment (in workshops)

Thus the majority of radar failures will give rise to three repair actions:

- at FIRST LINE (aircraft dispersal point), where a "black box" is changed
- at SECOND LINE (airfield repair section), where a module is replaced
- at THIRD LINE (central maintenance unit) or FOURTH LINE (manufacturers' plant) where a component part is replaced

Figure 8.2.2.1.1-1 shows that each repair location must be supported by a supply of spare units. But whereas the supply at First Line needs to hold spares for only the one aircraft type it is supporting, at Second Line the spares must cover all the aircraft types on the airbase, and at Third Line the supply must extend its coverage to spares for all types in service. Similarly, the repair workshops at Second and Third Line become a shared facility.

The commitments of each line are shown in Figure 8.2.2.1.1-2.

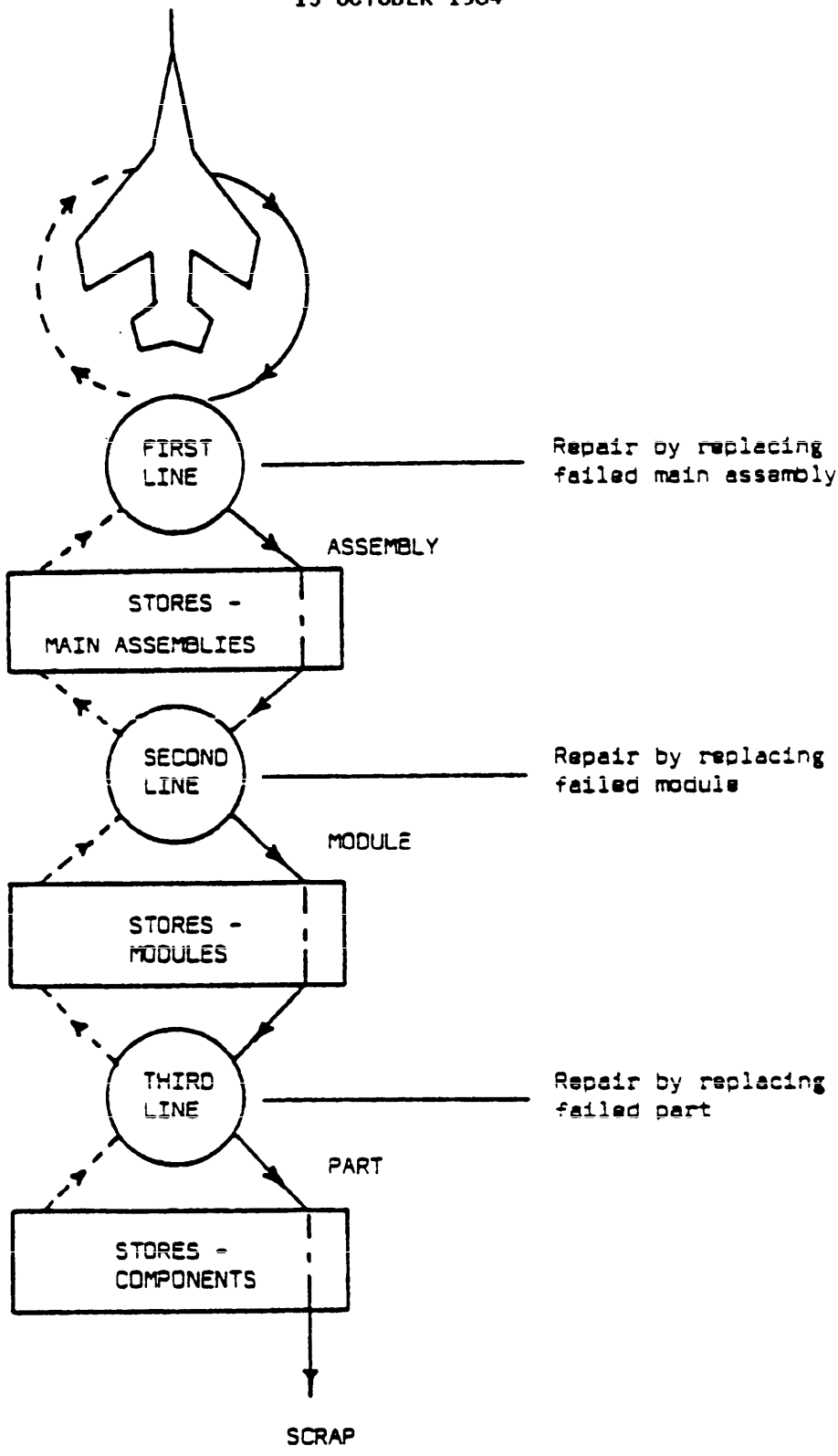
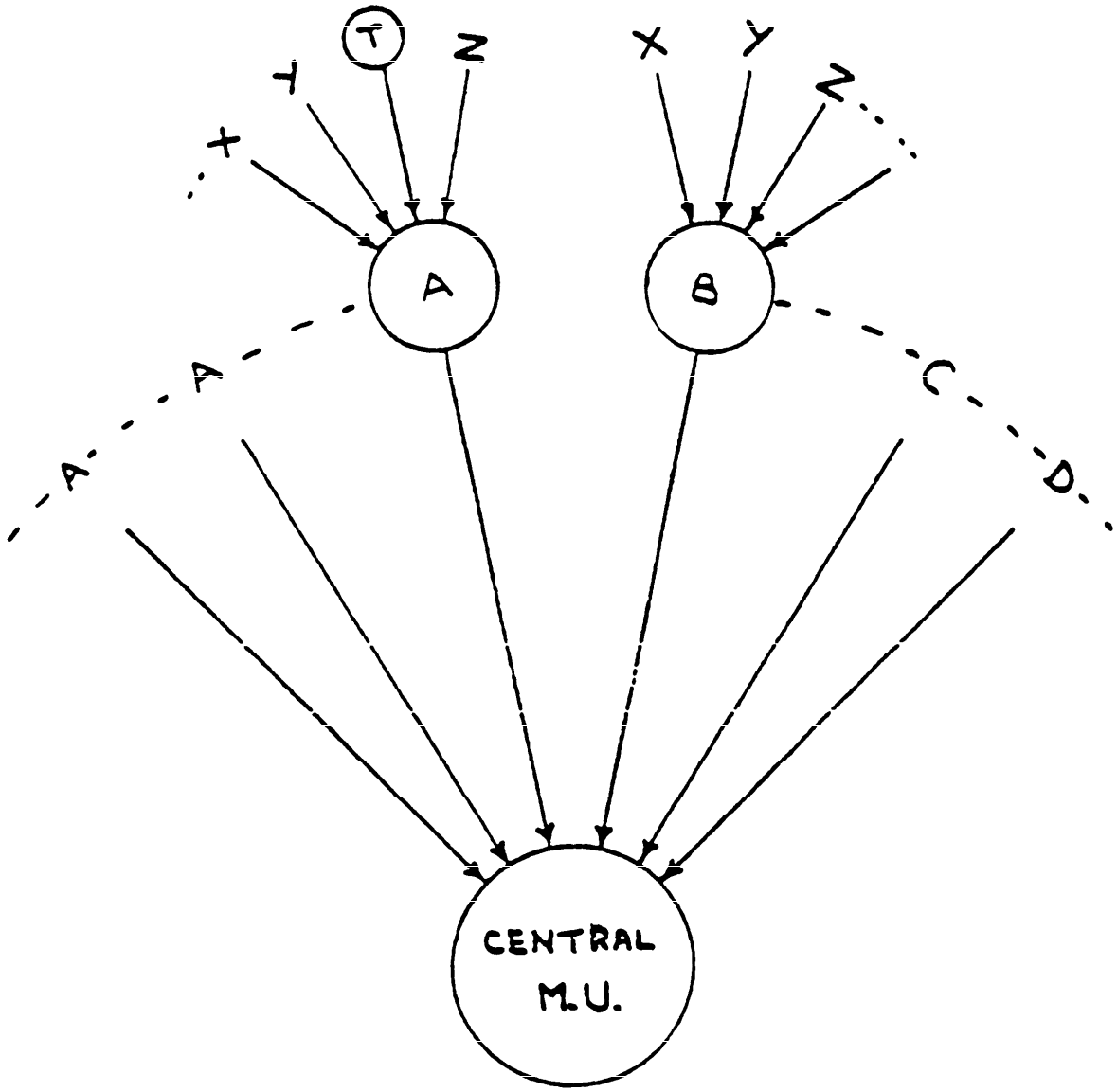


FIGURE 8.2.2.1.1-1: SERVICING POLICY



LEGEND

T	Aircraft type "T"
XYZ	Other aircraft types
A	Airfields with type "T" aircraft
BCD	Other airfields

FIGURE 8.2.2.1.1-2: REPAIR LINE COMMITMENTS

8.2.2.1.2 DEALING WITH THE PROBLEM

First we must define "adequate" in the context of an adequate spares holding and adequate repair facilities. The ideal is, of course, never to be out of stock. This is achievable by gross overstocking, but since this is wasteful in terms of capital tied up in spares collecting dust on the store shelves, the user must declare an acceptable stock-out risk. The repair facility must be geared to maintaining a stock of serviceable spare units at a level compatible with the accepted risk.

If the time between successive withdrawals from the supply depot is a fixed constant, and if the time between successive inputs of repaired units to the depot is also constant, then provided the output rate does not exceed the input rate, no stock-out risk exists. The risk arises because both inputs and outputs are aperiodic. The problem is illustrated in Figure 8.2.2.1.2-1, where D_1 is the distribution of the times between outputs about a mean value t_1, and D_2 is the distribution of times between inputs about a mean value t_2. Although t_2 is less than t_1, in the overlap region (cross hatched), the value of D_2 is greater than the value of D_1. When this occurs, the stock level decreases by one, so if the stock level is already zero, stock-out occurs.

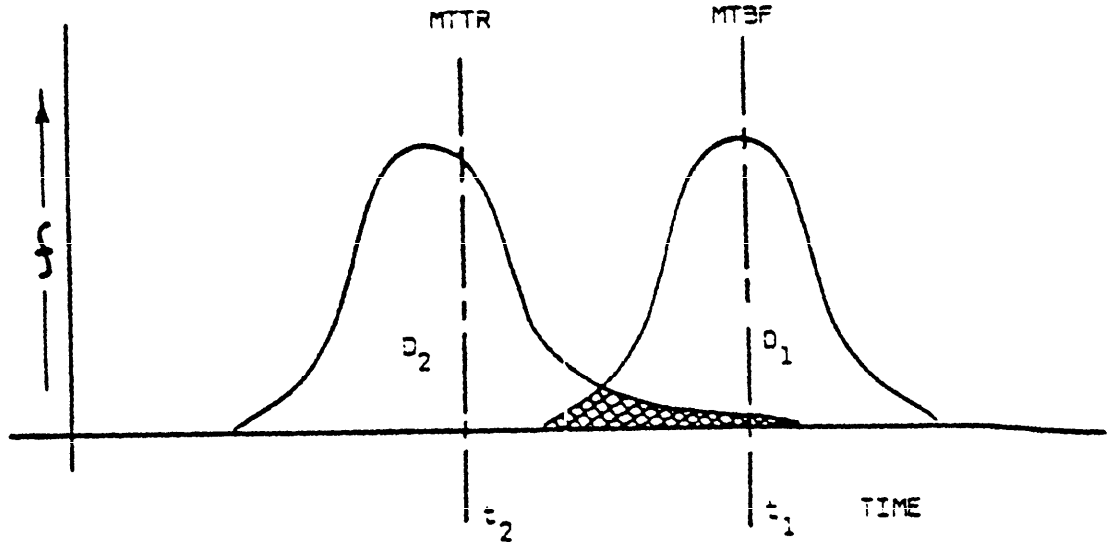


FIGURE 8.2.2.1.2-1: OVERLAP REGION OF D_1 AND D_2

o Distributions. The probability of an equipment failing in the time period T is

$$1 - \exp\left(-\frac{T}{M}\right)$$

where M is the MTBF of the equipment. The times between failures are therefore exponentially distributed, which means that the events follow a Poisson distribution. An event is an equipment failure, and each failure means a withdrawal of a spare from the supply depot. When the depot is supplying spares to a large number of aircraft, 40 in this case, the demand pattern is a large number of superimposed Poisson distributions, which add up to a normal distribution.

The distribution of the times to repair are less easy to model. Intuitively one feels that there is a finite minimum time to effect a repair, a small spread covering most cases and a long tail covering the defiant few. It would look like the curve shown in Figure 8.2.2.1.2-2.

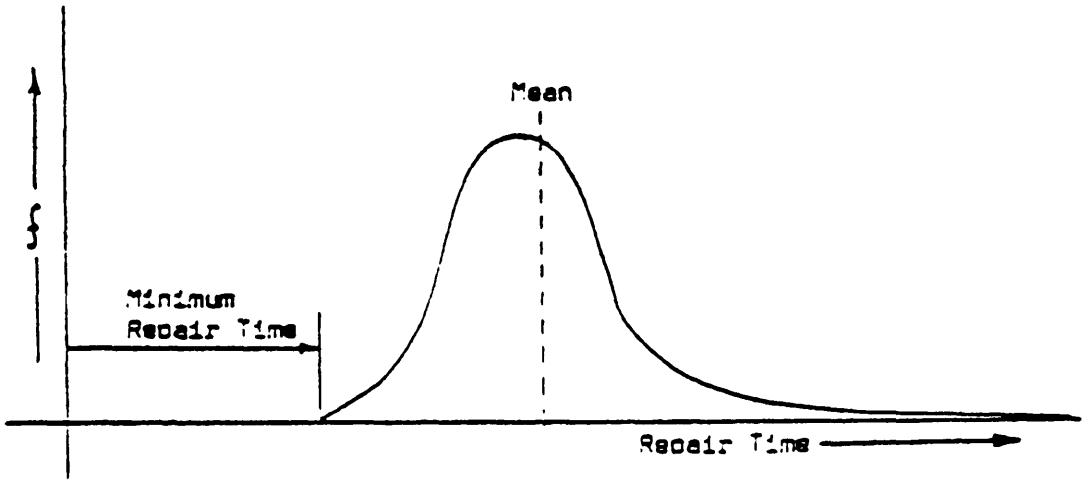


FIGURE 8.2.2.1.2-2: DISTRIBUTION OF TIMES TO REPAIR

The slope approximates to log-normal, but the shaping parameters are unknown and for estimation purposes when field data to support the log-normal distribution supposition is not available, no great error accrues if we assume the times to repair to be exponentially distributed and the events, i.e., repair complete, to follow a Poisson distribution. At Third and Fourth line there may be sufficient multiplication of repair facilities to provide an output of repaired items distributed in time approximately normally, but at Second line the number of superimpositions is unlikely to be large enough to approximate the distribution to normal.

o Mathematical Techniques.

(1) Markov Process

Notation

S system state
λ failure rate
μ repair rate
P probability
Pii probability of system remaining in Si
Pij probability of system changing state from Si to Sj

Consider a simple arrangement with one equipment in service and one spare equipment in stock. There are three possible states:

S_1 both units serviceable, one in service and one in supply
S_2 one unit serviceable, one unserviceable undergoing repair
S_3 both units unserviceable

For any given time interval, the system may remain in one state or change state once, twice or more times, depending on the length of time chosen. If we consider a time interval where initially the system is in state S_1, all the possibilities can be shown diagramatically thus:

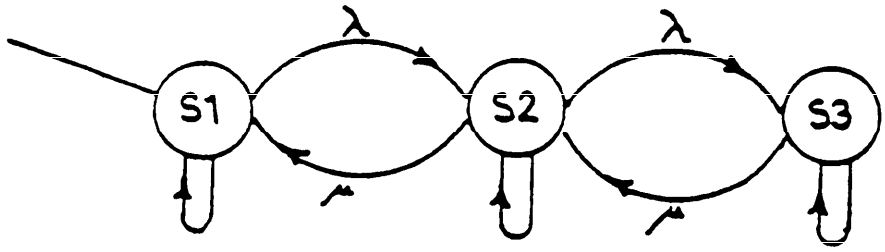


FIGURE 8.2.2.1.2-3: MARKOV PROCESS

The self-loops represent no change of state.

If we consider the system over some arbitrary time interval $(t, t + \Delta t)$ and, assuming a Poisson distribution, allowing one event (i.e., one change of state) only, the matrix in Table 8.2.2.1.2-1 is valid.

TABLE 8.2.2.1.2-1: TRANSITION MATRIX

Initial States	Final States		
	$S_1(t + \Delta t)$	$S_2(t + \Delta t)$	$S_3(t + \Delta t)$
$S_1(t)$	P_{11}	P_{12}	P_{13}
$S_2(t)$	P_{21}	P_{22}	P_{23}
$S_3(t)$	P_{31}	P_{32}	P_{33}

The probability of failure is $\lambda\Delta t$ and probability of repair is $\mu\Delta t$. Since only one event is possible in time Δt, $P_{13} = P_{31} = 0$. Given initial conditions at $t = 0$, there are various methods of solving for the steady state probabilities.

Although this method automatically suggests itself since the Poisson process assumed so far is a special case of the Markov process, a major drawback is that it rapidly becomes cumbersome as the number of states increases.

(2) Queueing Theory

Elementary queueing theory is briefly discussed here to assess extent of facilities required, and stock-out risk.

Poisson failure and exponential repair distributions are again assumed although other laws can be accommodated where more appropriate. Results are used here without proof but proof is readily available (see references).

The following parameters are used:

λ mean failure rate
$1/\mu$ mean repair time
ρ traffic intensity
n support needed
$Q(x)$ queue length distribution
$P(S)$ probability of stock-out $\equiv$ stock out risk

The traffic intensity is equal to λ/μ and for a queue to be manageable it is required that $\rho < 1$.

For a single server queue the distribution of x, the number of units in the queue, is geometric and is given by:

$$Q(x) = (1 - \rho)\,\rho^{x} \quad \ldots\ldots\ldots\ldots\ldots\ldots \quad (1)$$

which has mean and variance of $\rho/(1 - \rho)$ and $\rho/(1 - \rho)^2$, respectively.

Thus any servicing facility will function effectively if $\rho < 1$, although care has to be taken to ensure that the correct depth of maintenance is used in what we have defined as repair time. For example, at first line the repair time might be 30 minutes but the turn around time for a failed unit could be 5 days; the former is the first line repair time, the latter the second line repair time. (Naturally these levels are related.)

The stock-out risk can also be calculated. Consider a base with one spare transmitter and a total support need of n units. Taking λ as the individual transmitter mean failure rate and $1/\mu$ as the mean turn around time for a failed transmitter let us assume we have only one spare.

Since the individual transmitter failures are distributed Poisson (mean λ), the total support need failures are Poisson (mean $n\lambda$).

This situation is analogous to a single server queue (because there is one spare) and $\rho = n\lambda$.

Stock-out occurs if the queue exceeds one. From (1), stock-out risk is given by:

$$P(S) = \text{Prob.}\ (x > 1) = 1 - (1 - \rho) \sum_{i=0}^{1} \rho i$$

Thus if $\rho = 0.1$ and $n = 1$,

$$P(S) = 1 - 0.9\ (1 + 0.1) = 0.01 \text{ or } 1\%$$

For the radar system described earlier and under the single spare transmitter assumption, given 800 hour/year for each of the 40 aircraft, the transmitter stock-out risk is naturally high (approx. 19%).

A typical pattern of traffic for a First Line supply depot is shown in Figure 8.2.2.1.2-4, where the inputs are arrivals of repaired main assemblies from Second Line. The fluctuations in supply levels are shown, and it is thus possible to add the time intervals horizontally for any given stock level to arrive at the fraction of the total time interval under consideration. A stock level of -1 means that the demand cannot be met, stock-out has occurred.

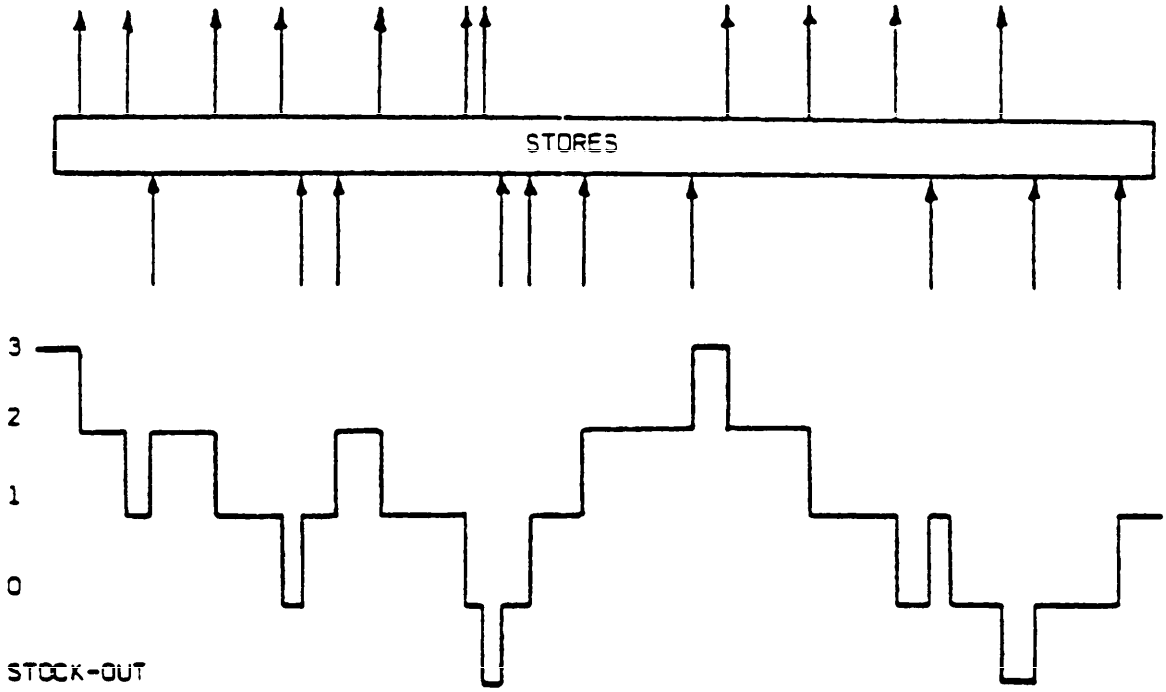


FIGURE 8.2.2.1.2-4: TRAFFIC PATTERN AND STOCK LEVEL

8.2.2.1.3 THE REPAIR FACILITIES

o Second Line Repair. The airbase repair section will receive, from the 40 aircraft we are concerned with, approximately 592 main assemblies for repair per year. This calculation is based on 800 operating hours per year and 54 hours MTBF per radar set. If the mean active repair time (MART) at Second Line is 2 hours, then one man should average 3 repairs per day. This is an adequate repair rate, but for assessment of the stock-out risk, the MART is only part of the mean time to repair (MTTR) which is defined as the total elapsed time that an equipment is out of service. As far as the First Line stock holding is concerned, the MTTR is the elapsed time between sending a failed black box to Second Line and receiving it back in a serviceable condition. Due to the inevitable variability in the Second Line work-load, the MTTR is, typically, 2-5 days.

Consider now the least reliable main assembly, the transmitter with a MTBF of 200 hours. For the 40 aircraft, the average number of transmitter changes per year will be 160, so clearly a 2-day turnaround (best case) means that at least one spare transmitter is needed to keep the pipeline filled to capacity. In the following diagram, the time from A to B is 2 days and the rate of withdrawal from supply is more than one transmitter every 2 days, so the supply is a buffer to absorb the variabilities in the input and output rates. It is axiomatic that the number of spares provided to support the need cannot be less than the number of units in the pipeline (see Figure 8.2.2.1.3-1)..

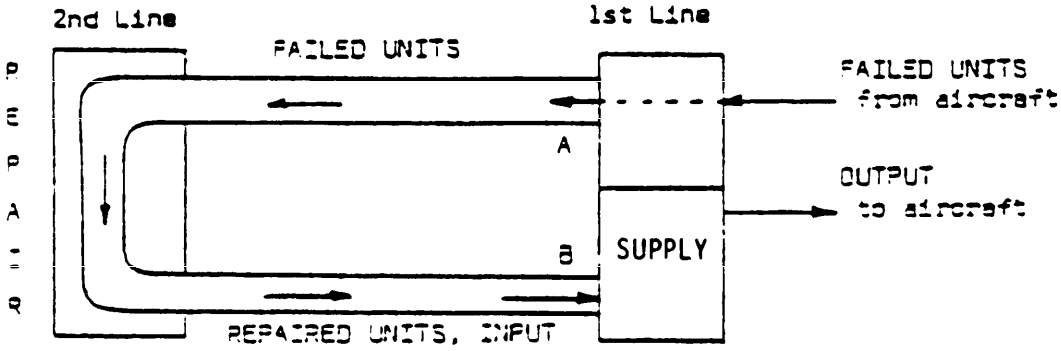


FIGURE 8.2.2.1.3-1: SUPPLY PIPELINE

In a peacetime situation, assuming an 8-hour day and a 250 day year, transmitters will be withdrawn from supply at the rate of 160 ÷ 250 = .64 per day. If the pipeline is 2 days long, the number of units in the pipeline will be 2 x .64 = 1.28. If the pipeline is 5 days long, number in the pipeline will be 5 x .64 = 3.2. In practical terms this means 2, 3 or 4 spares. Application of queuing theory enables us to quantify the stock-out risk in each case.

If the situation changes and the flying hours are suddenly doubled, the stock-out risk rises, and can be quantified. The risk can be reduced by increasing the spares holding or by reducing the repair time by increasing the repair facilities, for example. The tradeoff to optimize the best risk vs. cost solution can be made by simply varying the factors in the equation.

o Third Line Repair. At Third Line, the problem is slightly different. Although the MART for a PWB may be relatively short, in the order of 4-6 hours, the MTTR is likely to be long, perhaps 10-20 days. This comes about because of the time spent in transit and the load on the central MU which arrives from all airbases. Moreover, the 10-20 days will not be distributed about a mean. The turnaround time will slowly increase or slowly decrease, but since the MART is swamped by the non-active time the turnaround time may be taken as a constant for any short term.

Reverting to the example, with a total of 400 radar sets in service, and with 120 PWBs per set, or 48,000 total, the problem at Third Line is to provide repair facilities such that the turnaround time is compatible with the level of PWB spares held at Second Line. Again there is a tradeoff to determine the best strategy - increased level of spare PWBs at Second Line or increased repair facilities at Third Line. Because of the large number of different types of PWB that have to be held at Second Line, the decision is likely to go towards increased repair facilities. At this point it is worth noting that if it were possible to design the radar with multiples of standard PWBs, the optimum solution would almost certainly be to increase the level of spares held. The argument for standardization or "variety reduction" here is at its strongest.

o Availability of Test Equipment. Finally, some consideration must be given to the availability of test equipment at Second and Third Line. The active repair time is the sum of the time to diagnose the fault, time to rectify the fault and the time to retest. The advent of Automatic Test Equipment (ATE) for test and fault diagnosis of digital PWBs and higher assemblies has drastically reduced the MART for these units. But ATE is expensive, and being itself a complex piece of mainly digital electronics, will have a failure rate comparable with some of the major assemblies it is programmed to test and considerably higher than the PWBs it tests. It is important therefore to define a servicing policy for the ATE, to determine what level of ATE spares should be held, and where. The availability of the ATE must affect the turnaround time. What happens when the ATE is unserviceable? If all work stops

until it is fixed, then the MTTR figure for the ATE must be determined and factored into the turnaround time. If it is possible to continue the repair service with manually operated test equipment, then the MART under these conditjons must be considered. Thus if the ATE availability is 90%, MART using ATE is 3 hours and the MART using manual equipment is 8 hours, the factored overall MART is

$$100 \div \left(\frac{90}{3} + \frac{10}{8}\right) = 3.2 \text{ hrs.}$$

If work stops until the ATE is fixed, then the factored MART is:

$$100 \div \left(\frac{90}{3}\right) = 3.33 \text{ hrs.}$$

Once again the cost saving possibilities in standardization are in evidence. At Third Line, a general purpose ATE is needed to cope with the wide variety of units handled. The economic justification for purchasing additional sets of ATE will depend on the numbers of types of PWBs and higher assemblies designed for ATE testing. As the number of ATEs grows, the maintenance cost per ATE falls, provided of course, that standardization has been extended to the purchasing of ATE and is inherent in the ATE design.

REFERENCES

1. Cox, D.R., and W.L. Smith Queues, Chapman and Hall, 1971.

2. Dey, K.A. and H.E. Fox, "Optimization of Spares Holding and Maintenance Facilities," Marconi-Elliott Avionic Systems Ltd., U.K., 1978.

3. Doyon, L.R., Solving Reliability Models of Nuclear Systems, Proc., 1977 Annual R&M Symposium.

4. Shooman, M.L., Probabilistic Reliability: An Engineering Approach, McGraw-Hill, 1968.

9.0 FAILURE REPORTING AND ANALYSIS

9.1 FAILURE REPORTING

Failure reporting and analysis is a necessary operation to insure that a product's reliability and maintainability will be achieved and sustained. The Failure Reporting, Analysis and Corrective Action Systems (FRACAS) program is a key element in "failure recurrence" control for newly developed and production equipment. A FRACAS program includes provisions to assure that failures are accurately reported and thoroughly analyzed and that corrective actions are taken on a timely basis to reduce or prevent recurrence.

The reasons for electronic equipment operational malfunctions can be classified into four major areas:

(1) Design problems

(2) Quality of parts, materials, and processes used in equipment construction

(3) Misapplication

(4) Lack of proper maintenance

Data on electronic equipment malfunctions can be obtained from any or all of the following types of data sources:

(1) Design verification tests

(2) Preproduction tests

(3) Production tests

(4) Subcontractor tests

(5) Field data

9.1.1 CLOSED LOOP FAILURE REPORTING/CORRECTIVE ACTIONS SYSTEMS

For military programs, MIL-STD-785, Task 104 calls for the establishment of a FRACAS program. The purpose of this task is to establish a closed loop failure reporting system, procedures to determine cause, and documentation for recording corrective action taken. It requires the contractor to have a system that collects, analyzes and records failures that occur for specified levels of assembly prior to acceptance of the hardware by the procuring activity.

As shown in Figure 9.1.1-1, a typical FRACAS consists of the following fourteen steps:

(1) A failure is observed during some operation or test

(2) The observed failure is fully documented, including, as a minimum:

(a) Location of failure
(b) Date and time of failure
(c) Part number of the failed system/equipment
(d) Serial number of the failed system/equipment
(e) Model number of the failed system/equipment
(f) Observed failure symptoms
(g) Name of the individual who observed the failure
(h) All significant conditions which existed at the time of the observed failure

(3) Failure verification (i.e., reconfirmation of the validity of the initial failure observation)

(4) Failure isolation (i.e., localization of the failure to the lowest replaceable defective item within the system/equipment)

(5) Replacement of the suspected defective item with a known good item and retest of the system/equipment to provide assurance that the replacement item does in fact correct the originally reported failure

(6) Retest of the suspect item at the system/equipment level or at a lower level to verify that the suspect item is defective

(7) Failure analysis (see Section 9.2, Volume 2) of the defective item to establish the internal failure mechanism responsible for the observed failure or failure mode

(8) A search of existing data to uncover similar failure occurrences in this or related items (i.e., establishing the historical perspective of the observed failure mode/failure mechanism)

(9) Utilizing the data derived from steps 7 and 8, determine the antecendent or root cause of the observed failure

(10) Determine the necessary corrective action, design change, process change, procedure change, etc. to prevent future failure recurrence. The decision regarding the appropriate corrective action should be made by an interdisciplinary design team

(11) Incorporation of the recommended corrective action into the original test system/equipment

(12) Retest of the system/equipment with the proposed corrective action modification incorporated

(13) After suitable retest and review of all applicable data, establish the effectiveness of the proposed corrective action

(14) After the effectiveness of the proposed corrective action has been proven, the corrective action is then incorporated into the deliverable systems/equipment

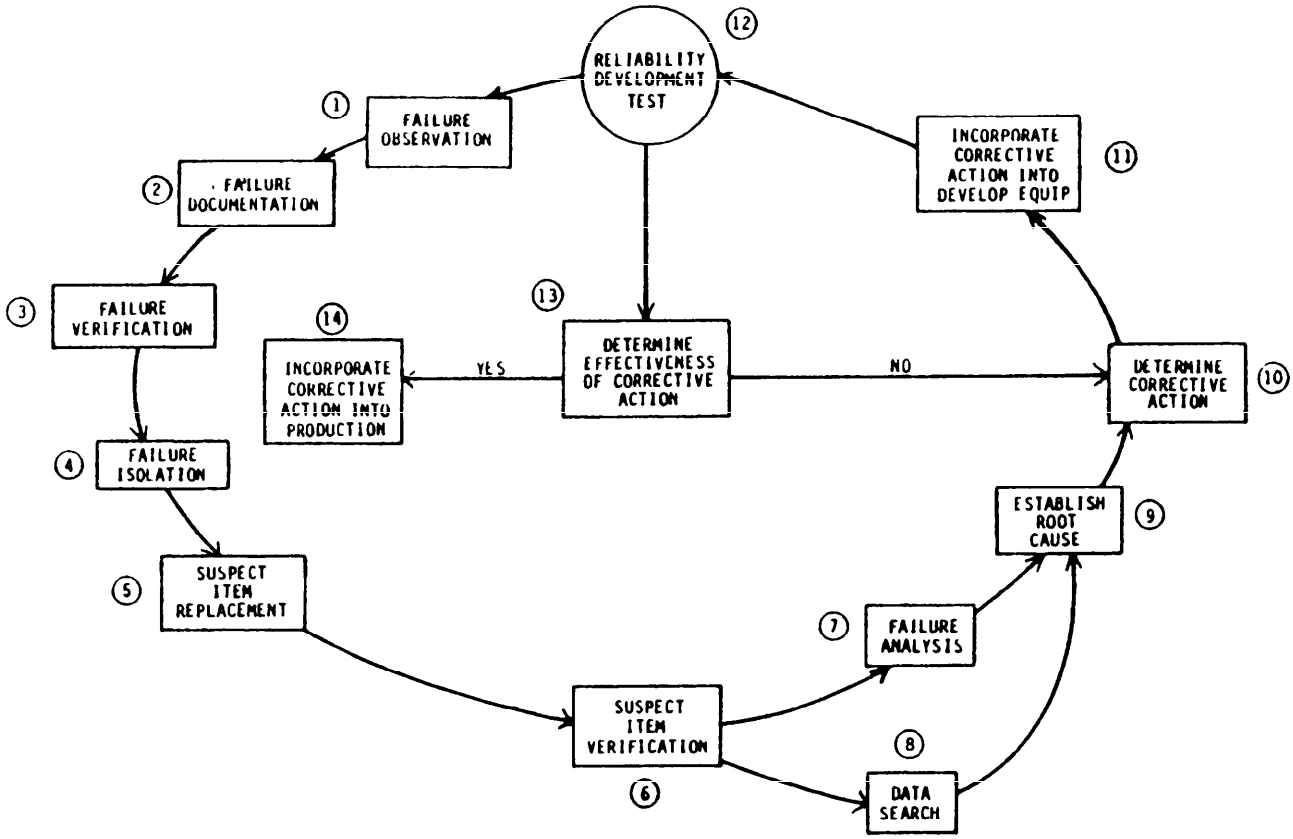


FIGURE 9.1.1-1: CLOSED LOOP FAILURE REPORTING AND CORRECTIVE ACTION SYSTEM

The contractor's program plan should clearly describe his proposed FRACAS. Furthermore it should identify those provisions incorporated therein to assure that effective corrective actions are taken on a timely basis. The applicable statement of work (SOW) should identify the extent to which the contractor's FRACAS must be compatible with the procuring agency's data system. It should also identify the levels of assembly and test to be addressed by the FRACAS, give definitions for each of the failure cause categories, identify the applicable logistics support requirements and identify the data items required for delivery.

9.1.2 FAILURE REPORTING SYSTEMS

Normally a manufacturer's reliability engineering organization is responsible for instituting and managing FRACAS. They establish policy, provide direction, and monitor the status of FRACAS investigations. The cognizant inspection and testing organizations, including reliability and quality engineering are responsible for initiating failure reports promptly as they are observed. The project management office generally reviews recommendations, coordinates analyses and test activities with the government, authorizes the implementation of acceptable fixes or corrective measures and provides direction relative to continuation of tests. The quality assurance organization transmits reports to the government and coordinates implementation of corrective actions.

tion problems can ... the applicable specifications and contract ... part selec

9.1.3 FAILURE REPORTING FORMS

It is imperative that failure reporting and resultant corrective actions be documented. Therefore, failure reporting and corrective actions forms must be designed to meet the needs of the individual system development and production program as well as the organizational responsibilities, requirements, and constraints of the manufacturer. The forms in Figures 9.1.3-1, 9.1.3-2 and 9.1.3-3 are examples of a Failure Reporting Form, Failure Analysis Report Form, and Corrective Action Request Form. The example in Figure 9.1.3-1 indicates entries for part identification data, conditions under which failures occurred, operating parameters indicating degradation, replacement part(s), repair times, references to applicable plans and procedures, and complete details leading up to or surrounding the failure incident. In the example of Figure 9.1.3-2 the complete description of the part(s) is given, including manufacturer and lot production code. Along with a complete failure analysis a determination is made whether or not to proceed with corrective action. In the example of Figure 9.1.3-3 relating to corrective action it is incumbent on the reliability organization to describe the problem and make recommendations for corrective action. The report is then forwarded to the quality assurance department which indicates actions taken to correct the problem. The report is then returned to the reliability organization. The sample forms of Figures 9.1.3-1, 9.1.3-2 and 9.1.3-3 can be adjusted or modified to meet the manufacturer's specific program.

9.1.4 DATA COLLECTION AND RETENTION

Maintaining accurate and up-to-date records through the implementation of the data reporting, analysis and corrective action system described above provides a dynamic, expanding experience base. This experience base, consisting of test failures and corrective actions, is not only useful in tracking current programs but can also be applied to the development of subsequent hardware development programs. Furthermore, the experience data can be used to:

- o assess and track reliability
- o perform comparative analysis and assessments
- o determine the effectiveness of quality and reliability activities
- o identify critical components and problem areas
- o Compute historical part failure rates (for new design reliability prediction in lieu of generic failure rates found in MIL-HDBK-217)

9.1.4.1 CUSTOMER DATA REPORTING SYSTEMS

With the deployment of the systems/equipments by the customer, the customer's data reporting system comes into effect. Most military data reporting systems are based upon logistic considerations rather than design considerations. The following paragraphs contain brief descriptions of some of these major DOD data reporting systems.

Military Maintenance Data Collection (MDC) systems are designed to inform commanders of the availability of airborne, shipside and ground support electronic equipment. The programs are also essential to logisticians in order to procure spare parts for the maintenance inventory. Examples of these programs are:

FAILURE REPORT FR

(1) System _____
Project No. _____ Product Order No. _____

(2) Report No. _____
Date _____

(3) Assembly _____ Subassembly _____ Component _____
_____
_____ No _____ No _____ No _____

(4) Date of Occurence _____
Time _____
Total Oper. Time _____ Hrs.

(5) Failure Discovered During

☐ Design Verification Test (Explain)

_____

_____

☐ Pre-Production system component test

☐ Reliability Growth ☐ Reliability Demo
☐ Development ☐ Other
☐ Qualification Describe _____

_____

☐ Production Test

☐ Acceptance
☐ Inprocess
☐ Receiving

(6)
Test Procedure No. _____
Paragraph No. _____

Test Equipment -- Serial Number

_____ _____
_____ _____
_____ _____

(7) Disposition (Failed test hardware)
Authorized by _____
Date _____
to prod control for repair ☐
Order No. _____
Scrap ☐
Hold for MRB Review ☐
Hold pending failure analysis/correction action ☐

(8) Failure Description (where appropriate describe test & environmental conditions)

_____

_____

_____

Effect on _____
System Operation _____

(9) Test Operator Signature _____ Date _____

Below for Engineering Reliability Use

Preliminary Investigation Description

(10) _____

_____

_____

Further Analysis Required Yes ☐ (FAR Req'd) No ☐ Failure Considered Closed

Maintenance action taken to restore system/component to operation

_____

_____

Replacement Item(s) _____ Adjustment(s) _____

_____

Downtime
Diagnostic _____
Remove/Replace/Checkout _____
Delay _____
Total _____

Date/Time System/Component returned to test _____

(11) Failure Classification
Relevant ☐ Non Relevant ☐
Chargeable ☐ Non Chargeable ☐

(12) Human Initiated Failure ☐

(13) Reliability Engineering Signature Date

FIGURE 9.1.3-1: FAILURE REPORTING FORM (SAMPLE)

FAILURE ANALYSIS REPORT FAR	① REFERENCE FAILURE REPORT NO.
③ REPAIR RECORD, REPLACEMENT PARTS	② DATE

I.D. PART NO.	MFG.	MFG. PART NO.	CK1 SYMBOL	PART SER NO.	PART LOT CODE	PROD ORD NO.

ADJUSTMENTS

④ DESCRIPTION OF ANALYSIS (USE ADDITION SHEETS IF NECESSARY)

⑤ CORRECTIVE ACTION TO BE REQUESTED YES ☐ NO ☐	⑥ SIGNATURE	DATE

FIGURE 9.1.3-2: FAILURE ANALYSIS REPORT FORM (SAMPLE)

REFERENCE FAILURE REPORT

CORRECTIVE ACTION REQUEST CAR

REPORT NO.
DATE

TO: _____ DEPARTMENT _____

DESCRIPTION OF PROBLEM

RECOMMENDATION

SIGNATURES: REL. MGR. _____ DATE _____
ENGINEERING MGR. _____ DATE _____
PROGRAM MGR. _____ DATE _____

ACTION TAKEN

SIGNATURE _____ DATE _____

RETURN COMPLETED FORM TO RELIABILITY BY _____ (DATE)

ENGINEERING
CHANGE
ORDER NO.

SIGNATURE
DATE

FIGURE 9.1.3-3: CORRECTIVE ACTION REQUEST FORM
(SAMPLE)

o AIR FORCE

Systems Effectiveness Data System (SEDS). The Reliability and Maintainability data acquisition, storage and retrieval and analysis system used by Air Force Systems Command (AFSC) during the Development, Test and Evaluation (DT & E).

Maintenance Experience Data (AFM 66-1). The Maintenance Data Collection (MDC) system was designed primarily as a base level production credit and management information system.

Standard Aerospace Vehicle and Equipment Inventory, Status and Utilization Reporting (AFM 65-110). This system delineates standard equipment status, inventory and utilization reporting procedures for all USAF, Air National Guard, Air Force Reserve and government plant representatives.

Data Products (D056). D056 data products are computerized reports derived from AFM 66-1 data residing in computers at base, command and HQ AFLC Wright Patterson AFB, OH.

Examples of these reports are:

- Summarized Maintenance Actions for Selected Work Unit Codes, RCS: LOG-MMO(AR)7169
- Aborts and Degraded Alerts, RCS: LOG-MMO(AR)7171.
- Materiel Safety Deficiency Report, RCS: LOG-MMO(AR)7178.
- System, Subsystem Corrosion Summary, RCS: LOG-MMO(AR)7180.
- Failure Rate Data for Selected Work Unit Codes, RCS: LOG-MMO(AR)7184.
- Maintenance Manhours per Flying Hours by Weapon, Command and System, RCS: LOG-MMO(AR)7185.
- Selected Part Number Action Summary, RCS: LOG-MMO(AR)7188.
- Parts Replaced During Field or Depot Repair, RCS: LOG-MMO(AR)7190.

Increase Reliability of Operation Systems (IROS). The objective of the USAF IROS program is to identify those subsystems, components and items of equipment which are disproportionate resource consumers, high contributors to system nonavailability or potential safety problems based on their reliability or maintainability performance.

Maintenance Management Information and Control System (MMICS). The MMICS is a large, dynamic, on-line system used at base level to manage maintenance equipment and personnel resources. It also provides much of the data needed by major commands, HQ AFLC, HQ USAF and other agencies to manage and track maintenance resources worldwide.

o ARMY

The Army Equipment Record System (TAERS). The TAERS is designed to provide field commanders, commodity command managers, project managers and top level headquarters with problem solving data for improved material readiness. It is an official Army method for reporting information necessary for control of operation and maintenance support of Army equipment.

The Army Maintenance Management System (TAMMS). The objective is to record the minimum amount of data while recording all that are required for control, operation and maintenance of equipment at each level of command. The sample data collection program has been established to provide for collecting more detailed maintenance and operational performance data on individual approved items of equipment.

Reliability, Availability, Maintainability (RAM). This program has been for several years in conceptual stages and is ready for coordination. RAM is required during all phases of material life cycle, including development and operational testing, production testing and deployment. RAM data are required to evaluate the performance of material systems and subsystems, provide a foundation for future development programs and provide for logistic support information.

o NAVY

Ships Maintenance Material Management (3M). The Navy Ship 3M is composed of two subsystems. The Planned Maintenance Subsystem (PMS) and the Maintenance Data Collection Subsystem (MDCS). PMS details procedural instructions to be followed in performing routine maintenance and periodic operational checks. MDCS is the means by which maintenance personnel report correction maintenance actions on specific categories of equipment. Submarines report corrective maintenance actions on all equipment.

Avionic Maintenance Material Management (3M). The Navy Avionic Maintenance Data Collection System (MDCS) are data recorded from these levels of maintenance: Organizational (on equipment), Intermediate (off equipment) and Depot. Data products prepared are similar to AFM 66-1.

Fleet Reliability Assessment Program (FRAP). The purpose of FRAP is to test the feasibility of reducing life cycle costs and improving fleet readiness through an organized program of controlled observation of samples of newly deployed operational systems followed by early reliability improvements based on these observations. (Reports are available through the Defense Technical Information Center (DTIC)).

o MARINE CORPS

Marine Corps Integrated Maintenance Management Systems (MIMMS). MIMMS is an automated information system which is designed to assist commanders at all command levels in both the operating forces and supporting establishments of the Marine Corps in the execution of the ground equipment maintenance functions. Inputs to the system are prepared at the information source by maintenance, supply and operational personnel.

o RELIABIITY IMPROVEMENT WARRANTIES (RIW)

Air Force. RIW is a contracting technique currently being applied to Air Force contracts on a trial basis. The objective of the RIW is to motivate contractors to design and produce systems/equipment which will have a low failure rate as well as low repair cost after failure due to field/operational use. In each case where failures occur, the contractor is required to verify the failures and possibly perform a failure analysis.

Army. RIW is an acquisition concept designed to reduce life cycle costs and to improve operational reliability of military equipment. RIW provides an incentive for contractors to produce reliable equipment because the contractor, for a fixed fee, must repair or replace all equipment returned to his plant for a three to six year period. Therefore, the contractor is required to process, test, repair or replace, add reliability changes, and package all the equipment returned. His RIW is priced on the expected field reliability, repair costs, expected operating hours and overhead costs.

o DEPARTMENT OF DEFENSE (DOD)

Reliability Analysis Center (RAC). The overall objective of RAC is to aid government, industrial and commercial engineers in improving the reliability of electronic equipment. The services of the Center are designed to provide users with faster and more effective methods of reliability improvement. This is accomplished through ready access to failure and reliability data on microelectronic, electronic and nonelectronic parts used in the design of electronic equipment/systems.

Government Industrial Data Exchange Program (GIDEP). GIDEP provides the only comprehensive no-charge data exchange in the United States. Its products include environmental test reports and procedures, reliability specifications, failure analysis data, and other technical information related to application, reliability, quality assurance and testing of parts.

The two aforementioned DoD services are readily available to the government, industrial and academic community. Although the RAC has a fee for its services, its analyses are tailored to the users queries, while the GIDEP prepares a bibliography of reports covering a broad spectrum of quality assurance activities. With regard to failure analysis information and failure rate data, RAC has a computerized system to prepare statistical failure rates on numerous electronic and nonelectronic device types and electronic equipment. RAC also publishes annually updated compendia of analyzed data reflecting the reliability history of these devices and equipments.

The Maintenance Data Collection (MDC) systems prepared by military agencies are not available to everyone. Since the data prepared are considered to be For Official Use Only, for the most part, personnel at contracted electronic equipment production facilities may acquire data through their local Air Force Plant Representative Office (AFPRO) or Naval Plant Representative Office (NAVPRO). A manufacturer can access MDC system data on systems/equipment he has produced. In other instances where there is a competitive bid on a system/equipment production the bidders can access field maintenance data on the subject system/equipment.

Since the MDC system contains only maintenance actions where replaced parts are recorded, the user of the data should be cautioned that failure rates cannot be applied directly to the data. There is no verification of failures (parts replaced); therefore, a very careful analysis of the replaced parts should be performed. Studies such as performed by Fiorentino (RADC/RBET)[1] and Kern (Hughes Aircraft)[2] are recommended.

9.2 FAILURE ANALYSIS

Failure analysis is a post-mortem examination of a failed item employing electrical measurements and analytical techniques of physics, metallurgy and chemistry in order to verify the reported failure and identify the mode or mechanism of failure, as applicable. The failure analysis procedure should be sufficient to adequately support conclusions as to the cause or relevancy of failure, for initiating corrective actions in device application, production processing, device design or device testing, and to eliminate the cause or prevent the recurrence of the failure mode or mechanism reported.

Because the art of failure analysis is intimately related to device fabrication technology, the reader's attention is directed to two documents which are major sources of information on the problems (and the steps and techniques employed to overcome them) encountered in the manufacture, test, application, fault isolation, failure reporting and failure analysis of microcircuits. These documents are:

o "Microcircuit Manufacturing Control Handbook, Volume I" which was prepared jointly by the Integrated Circuit Engineering (ICE) Corporation and Rome Air Development Center (RADC). This document is designed to serve as a reference guide to microcircuit manufacturing process engineers and is primarily concerned with the portrayal of semiconductor processing steps, their critical parameters and potential problem areas. Copies of this document are available from ICE Corporation, 15022 N. 75th Street, Scottsdale, AZ 85260.

o "Microelectronics Failure Analysis Techniques, A Procedural Guide," which was prepared jointly by the General Electric Company, Electronics Laboratory, the Rome Air Development Center (RADC) and the Reliability Analysis Center (RAC). This document is intended to serve as a useful tool for the beginning failure analyst as well as a convenient reference source for the experienced failure analyst and other quality, reliability and project engineers in the semiconductor manufacturing or user industries. It represents a collection of the failure analysis techniques most used by industry leaders in this growing field. The guidebook provides the failure analyst with a general technical discussion of each major failure analysis technique currently in use together with samples or suggestions on its use in performing failure analysis on semiconductor devices. Copies are available from the Reliability Analysis Center, RADC/RBRAC, Griffiss AFB, NY 13441.

The following information relates to, and is couched in terms of, the analysis of the cause of failure of microelectronic devices. However, many of the analytical procedures, techniques and tools discussed are applicable to the failure analysis of both active and passive discrete parts.

9.2.1 GENERAL CONSIDERATIONS IN FAILURE ANALYSIS

o Classification of Failures. There are specific terms used in failure analysis which have developed in concert with semiconductors and microcircuits. Observations made during failure analysis should determine whether the failure is primary or secondary and, if a primary failure, whether it can be classified as surface, bulk, or mechanically related failure. Some of the commonly used terms in failure analysis are given below:

(1) Failure Mode is the particular manner in which a failure occurred; the electrical or mechanical manifestation of failure. Examples of failure modes in semiconductor devices are open bonds or metallization.

(2) Failure Mechanism is the fundamental chemical or physical effect responsible for a particular failure mode. For example, the failure mechanism associated with an open bond failure mode could be "purple plague."

(3) Primary Failure occurs when the part itself is the intrinsic cause of failure when operating within specification. When a number of parts have failed simultaneously it will be necessary to identify and isolate the part causing primary failure.

(4) Secondary Failure occurs when it has been determined that part failure was caused by a stimulus outside its operating specification. A shorted resistor may cause a secondary transistor failure manifested by an open emitter wire.

(5) Bulk Defect is an inherent imperfection in the basic silicon material which is intrinsic to the material or introduced during device processing

(6) Surface Defect is an imperfection at the surface of the device related to improper processing

(7) Mechanical Defect is one resulting from the effects of external environment on the device such as shock, vibration, thermal cycling, fatigue, etc.

o Failure Analysis Flow Sequence. The actual failure analysis flow sequence employed by the analyst will be largely dependent on the type of device, expected failure mechanisms, observed failure modes, package construction, and technology used. Figure 9.2.1-1 illustrates the general steps of an orderly failure analysis. This simplified flow diagram is presented in order to stress the importance of establishing the potential failure mechanisms, based on all data available, prior to any actual analytical steps, either destructive or nondestructive.

A more detailed version of a generalized failure analysis flow diagram is given in Figure 9.2.1-2 to illustrate what is a recommended sequence for specialized failure analysis techniques. This should not preclude the use of some specialized technique in a different place in the analysis based on unique circumstances which apply to a particular failure mechanism.

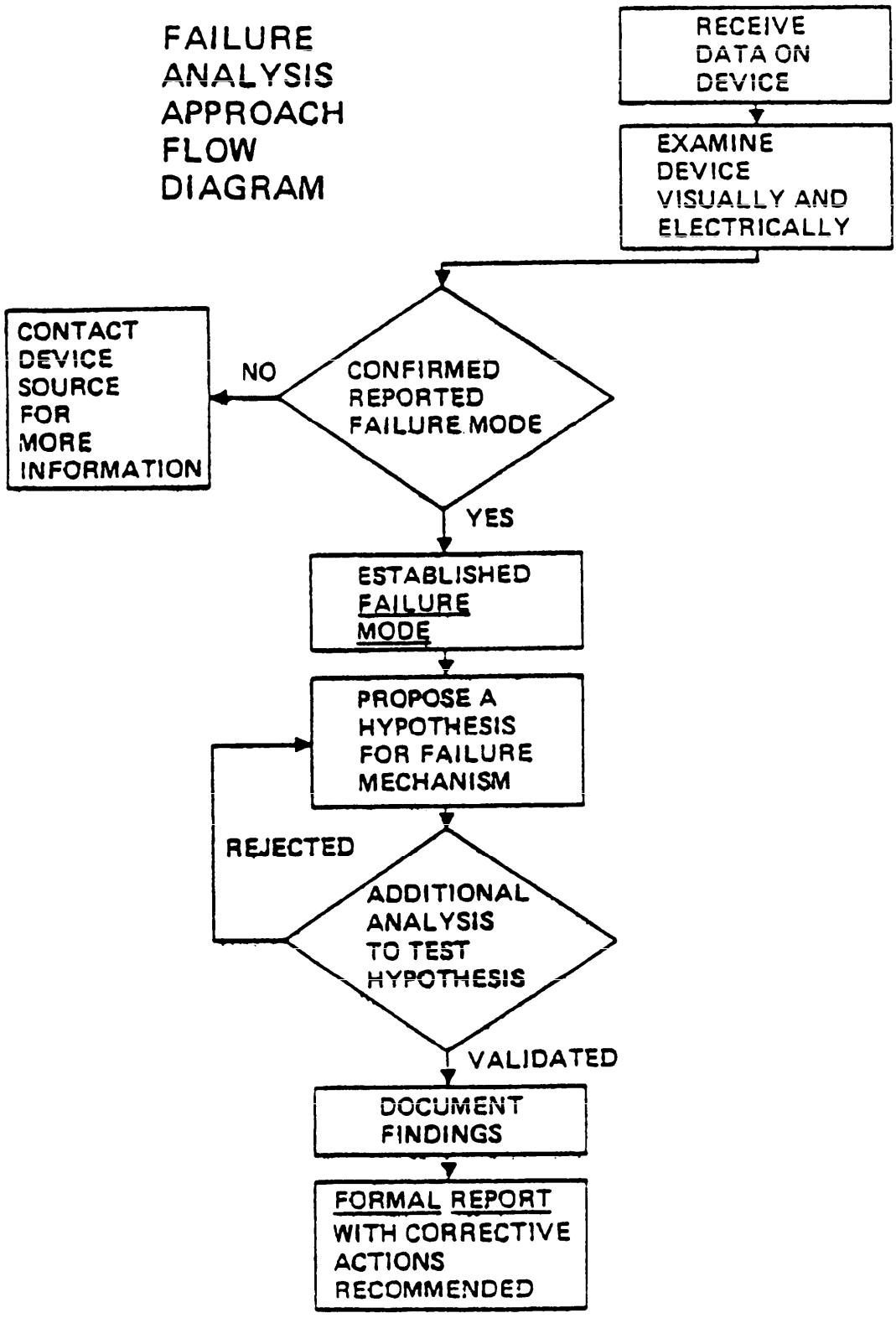


FIGURE 9.2.1-1: FAILURE ANALYSIS APPROACH FLOW DIAGRAM

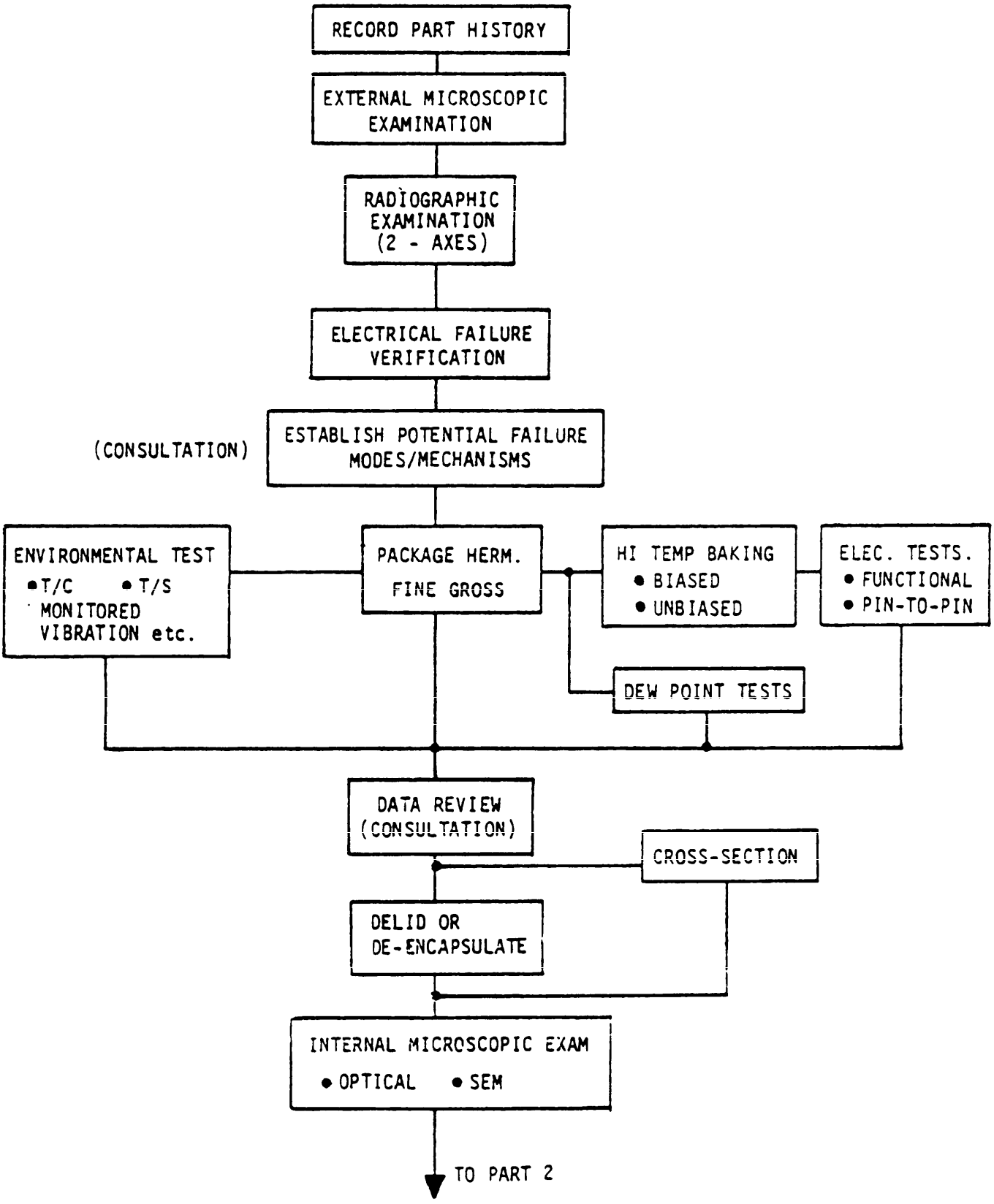


FIGURE 9.2.1-2: GENERALIZED FAILURE ANALYSIS FLOW DIAGRAM

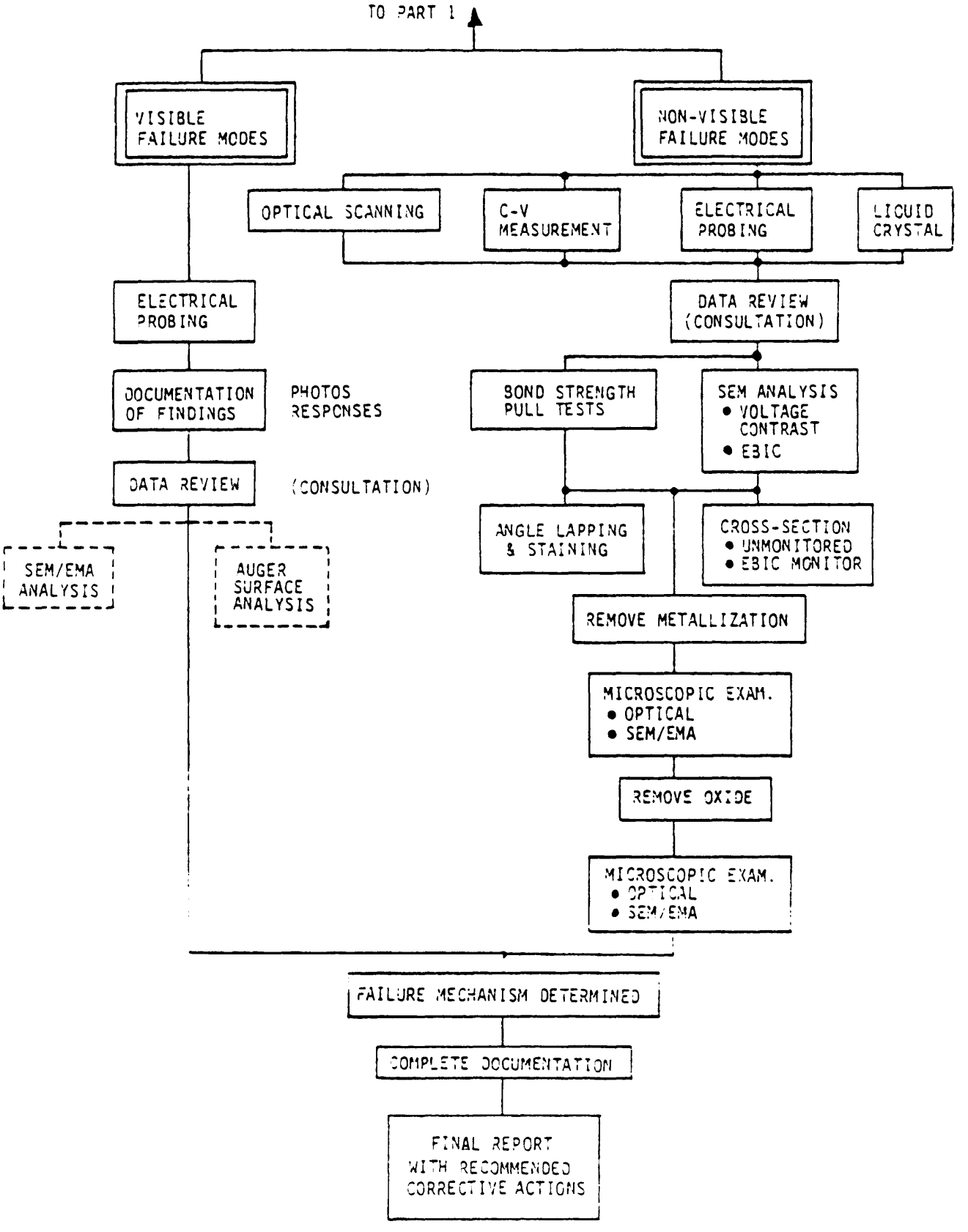


FIGURE 9.2.1-2: GENERALIZED FAILURE ANALYSIS FLOW DIAGRAM (CONT'D)

9.2.2 FAILURE ANALYSIS APPARATUS

Apparatus required for failure analysis depends upon the degree and depth to which the analysis is performed. The high reliability of integrated circuits, the very small dimensions involved, and the extremely small amounts of contaminants required to cause integrated circuits to malfunction have led to the need for sophisticated analytical equipment to determine causes of failure (see Section 7.2.2 for a discussion of automatic test equipment). On the other hand, however, many failures can be diagnosed merely by examining the package under proper magnification or examining the chip or die under a microscope.

The variety of test equipment available to the failure analyst in today's market is virtually unlimited. Most analysts, however, have to start out with only a modest equipment budget and build up a capability over a number of years. Table 9.2.2-1 contains a list of the minimum equipments necessary to equip a beginning Failure Analysis Laboratory for the analysis of microelectronic devices.

TABLE 9.2.2-1: BEGINNING FAILURE ANALYSIS LABORATORY

Item	Approx. Cost 1981
1. Curve Tracer	$5K - 10K
2. Digital V-O-M	$750 - 1.5K
3. Stereo Binocular Microscope (10X-100X)	$750 - 1K
4. Package Opening Tools	$200
5. Miscellaneous Hand Tools	$500
6. Set of Three Microprobes	$200 - 500
Total	$7.4 - $13.7K

A more complete list of apparatus required for complete failure analysis includes:

(1) Test equipment capable of complete electrical characterization of device being analyzed

(2) Optical microscopes capable of making usual observations at adequate magnification

(3) Photographic equipment capable of being used with the optical microscope to record regions which might be related to device failure

(4) Micromanipulations capable of point-to-point probing on the surface of the device die or substrate to further localize cause of failure

(5) X-ray radiography to determine the presence of foreign material in the device enclosure or verify the indication of open or shorted leads from previous electrical measurements

(6) Electron microscopes capable of providing examination at extremely high levels of magnification to examine metallizations or bulk features

(7) Fine and gross leak apparatus for determining package integrity relative to hermeticity

9.2.3 INFORMATION OBTAINED FROM FAILURE ANALYSIS

The following is a partial list of failure modes and mechanisms which are obtained from failure analysis using the equipment listed above:

(1) Device electrical abuse due to overstress conditions from internal or external transient overvoltages

(2) Device parameter degradation, both static and dynamic

(3) Open and shorted leads or metallization; poor band placement; lead dress; corroded metals within package; cracked die or substrate

(4) Metal migration; oxide contamination; mask misregistration; dielectric shorts

(5) Quality of junctions, diffusions

(6) Lack or loss of hermeticity

From the user's point of view the purpose of failure analysis is to determine the failure mode and eliminate it by associating the failure mode with the failure mechanism.

9.2.4 COMMON CAUSES OF PARTS FAILURE

One of the major causes of semiconductor device or microcircuit failure is device electrical abuse. Damage may be caused by overvoltages on the inputs during testing, handling or troubleshooting, or perhaps by weaknesses inherent in the system design, or when the system interfaces with external power sources. Transient electrical voltage may result from external power sources leading to degradation or catastrophic failures. Electrostatic discharge during device fabrication or higher level assembly may also cause device degradation or failure, particularly with sensitive device structures, both bipolar or metal-oxide-semiconductor (MOS).

Another major contribution to device failure is poor workmanship mostly from photoresist and lead bonding operation, since these are operator intensive. These workmanship failure causes are being reduced as processing facilities become more automated.

9.2.5 FAILURE CATEGORIES

Device failures can be divided into two distinct groups. One is the comparatively high number of devices which do not meet specification upon arrival at the users facility. Some of these failures are brought about by human error committed either in the screening or marking procedures utilized by the supplier; other failures result from device degradation during shipment and storage prior to use or from infant mortality. The second group of failures occur during the operational cycle of the equipment and result from electrical overload, environmental effects and continued internal degradation of the device.

REFERENCES

1. Fiorentino, E. (RADC, GAFB, NY). "The Use of Air Force Field Maintenance Data for R & M Assessments of Ground Electronic Systems," (RADC-TR-79-103) April, 1979 (AD/A049-920).

2. Kern, G.A., T.M. Tine. "Operational Influences on Reliability," (RADC-TR-76-366), April 1974 (AD/A035-016).

3. J.E. Arsenault, & J.A. Roberts, Editors. Reliability and Maintainability of Electronic Systems, Computer Science Press.

4. Integrated Circuit Engineering (ICE) Basic Technology.

5. "Microcircuit Manufacturing Control Handbook, Volume I," ICE Corp. and RADC, July 1975.

6. Doyle, Edgar A., Jr. (RADC, GAFB, NY) and W.L. Morris (GE Co. Electronic Laboratory, Syracuse, NY), Editors. "Microelectronics Failure Analysis Techniques Procedural Guide," July 1981.

APPENDIX A

FACTORS AFFECTING FAILURE RATES OF PARTS

The following tables give the factors affecting the failure rates of electrical/electronic parts. As given in MIL-HDBK-217 the part failure rate is a function of these factors (designated as "π" factors). (An asterisk appearing in any column indicates that those factors do not contribute to the failure rate of that particular part type):

For example, the part selection failure rate λ_p for fixed resistors is given by:

$$\lambda_p = \lambda_b (\pi_E \times \pi_R \times \pi_Q)$$

where

λ_b = base failure rate (a function of temperature and stress)

π_E = environmental factor

π_R = resistance factor

π_Q = quality factor

TABLE 1: FACTORS AFFECTING FAILURE RATE

Device Type	Temperature	Environment	Quality Level	Stress** Ratio
Resistors	X	X	X	X
Capacitors	X	X	X	X
Semiconductor	X	X	X	X
Microcircuit	X	X	X	*
Relays	X	X	X	X
Connectors	X	X	*	*
Switches	X	X	*	X
Inductive Devices	X	X	X	*

* Due to lack of statistical data MIL-HDBK-217 failure rates do not consider all the electrical parameters affecting part failure rate. Also MIL-HDBK-217 does not consider the effect of transients on failure rate.

** Power for resistors
Voltage for capacitors
Power (current) for semiconductor devices
Contact current (continuous) for relays
Contact current and voltage for switches

TABLE 2(a): RESISTORS

Resistor Type	Resistance1/ Value	Number of Taps on Potentiometer	Voltage Factor	Construction	Number of Resistors in Use
Fixed	X				
Variable	X	X	X		
Variable (Styles RP and RR only)	X	X	X	X	
Resistor Network (Style RZ)					X

1/ The higher the resistance value, the higher the failure rate.

TABLE 2(b): CAPACITORS

Capacitance values -	all styles except CV, PC, CT and CG. (The higher the capacitance value, the higher the failure rate.)
Series circuit resistance -	for type CSR only. (The higher the series circuit resistance, the lower the failure rate.)
Construction -	for type CLR only.
Configuration -	for type CG only.

TABLE 2(c): RELAYS, SWITCHES AND CONNECTORS

Device Type	Number of Contacts	Time Rate of Actuation	Contact Load	Construction and Application
Relays	X	X	X	X
Switches	X	X	X	
Connectors	X	X		

TABLE 3: ADDITIONAL FAILURE RATE FACTORS FOR SEMICONDUCTOR DEVICES

Semiconductor Device Type	Application	Device Rating	Voltage Stress	Circuit Complexity	Frequency and Peak Operating Power Factor	Type of Matching Network	Construction
Conventional Transistors	X	X	X	X			
Diodes, General Purpose	X	X	X	X			X
FET	X			X			
Zener/Avalanche Diodes	X						
Thyristors		X					
Microwave Transistors	X				X	X	
Opto-electronic Devices				X			

TABLE 4: ADDITIONAL FAILURE RATE FACTORS FOR MONOLITHIC AND HYBRID MICROCIRCUITS

A. Monolithic Microcircuits

Production status of the device

Circuit complexity

Number of pins (not applicable to monolithic bipolar and MOS linear devices).

B. Hybrid Microcircuits

Number of each particular component

Failure rates of individual components

Number of interconnections and density of interconnections

Failure rate of hybrid package

Circuit function (i.e., linear, digital, or linear-digital)

TABLE 5: LEARNING FACTORS/FAILURE RATE MULTIPLIERS FOR MICROCIRCUITS

The learning factor π_L is 10 under any of the following conditions:

(1) New device in initial production

(2) Where major changes in design or process have occurred

(3) Where there has been an extended interruption in production or a change in line personnel (radical expansion)

The factor of 10 can be expected to apply until conditions and controls have been stabilized. This period can extend for as much as six months of continuous production.

π_L is equal to 1.0 under all production conditions not stated in (1), (2) and (3) above.

tive action. The report is then forwarded to the quality assurance depa

APPENDIX B

BASE FAILURE RATES FOR ELECTRON TUBES (INCLUDES BOTH RANDOM AND WEAROUT FAILURES)

TUBE TYPE	($F/10^6/hr$)
RECEIVING	
Triode, Tetrdoe, Pentode	5
Power Rectifier	10
CATHODE RAY TUBE	15
THYRATRON	50
CROSSED FIELD AMPLIFIER	
QK 681	260
SFD261	150
PULSED GRIDDED	
2041	140
6952	390
7835	140
TRANSMITTING	
Triode Peak Power 200kw	75
Tetrode Avg. Power 2kw	100
Pentode Freq. 200Mhz	100
For Tubes with Power, Freq. Exceeded	250
TRAVELLING WAVE TUBES	
M5768	310
MA 2001 A	170
VA 138D	50
VA 643	90
VTR 5210A1	150
WJ 3751	90
ZM 3167	90
For TXTs not listed above, use:	
Peak Power 10 watts	20
Peak Power 10 watts 100watts	50
Peak Power 100 watts 10,000 watts	150
Peak Power 10,00 watts	
TWYSTRON (HYBRID TWT-KLYSTRON)	
VA 144	850
VA 145E	450
VA 145H	490
VA 913A	230

APPENDIX B (Cont'd)

BASE FAILURE RATES FOR ELECTRON TUBES
(INCLUDES BOTH RANDOM AND WEAROUT FAILURES)

TUBE TYPE	($F/10^6/hr$)
MAGNETRON	
5586	500
6344	340
7256	520
8798	380
400615	450
QK 327A	430
QK 338A	460
For magnetrons not listed above use:	
Peak Power 10RW	300
Peak Power 10kw	450
KLYSTRON	
Low Power (e.g., local oscillator)	30
CONTINUOUS WAVE TYPE (CW)	
3k3000 LQ	9
3k50000 LF	54
3k21000 LQ	150
3kM300 LA	64
3kM3000 LA	19
3kM500000 PA	110
3kM500000 PA1	120
3KM500000 PA2	150
4k3 CC	610
4k3 SK	29
4k50000 LQ	30
4kM50 LB	28
4kM50 LC	15
4kM50 SJ	38
4kM50 SK	37
4kM3000 LR	140
4kM50000 LQ	79
4kM50000 LR	57
4kM170000 LA	15
8824	130
8825	120
8826	280
VA 800 E	70
VA 853	220
VA 856 B	65
VA 888 E	230